

Compal Confidential

Model Name : ZIVY0

File Name : LA-A921PR03

BOM P/N:4319xxxxxx -- ZIVY0

Compal Confidential

ZIVY0 M/B Schematics Document

Intel SharyBay ULT Processor

2013-12-01

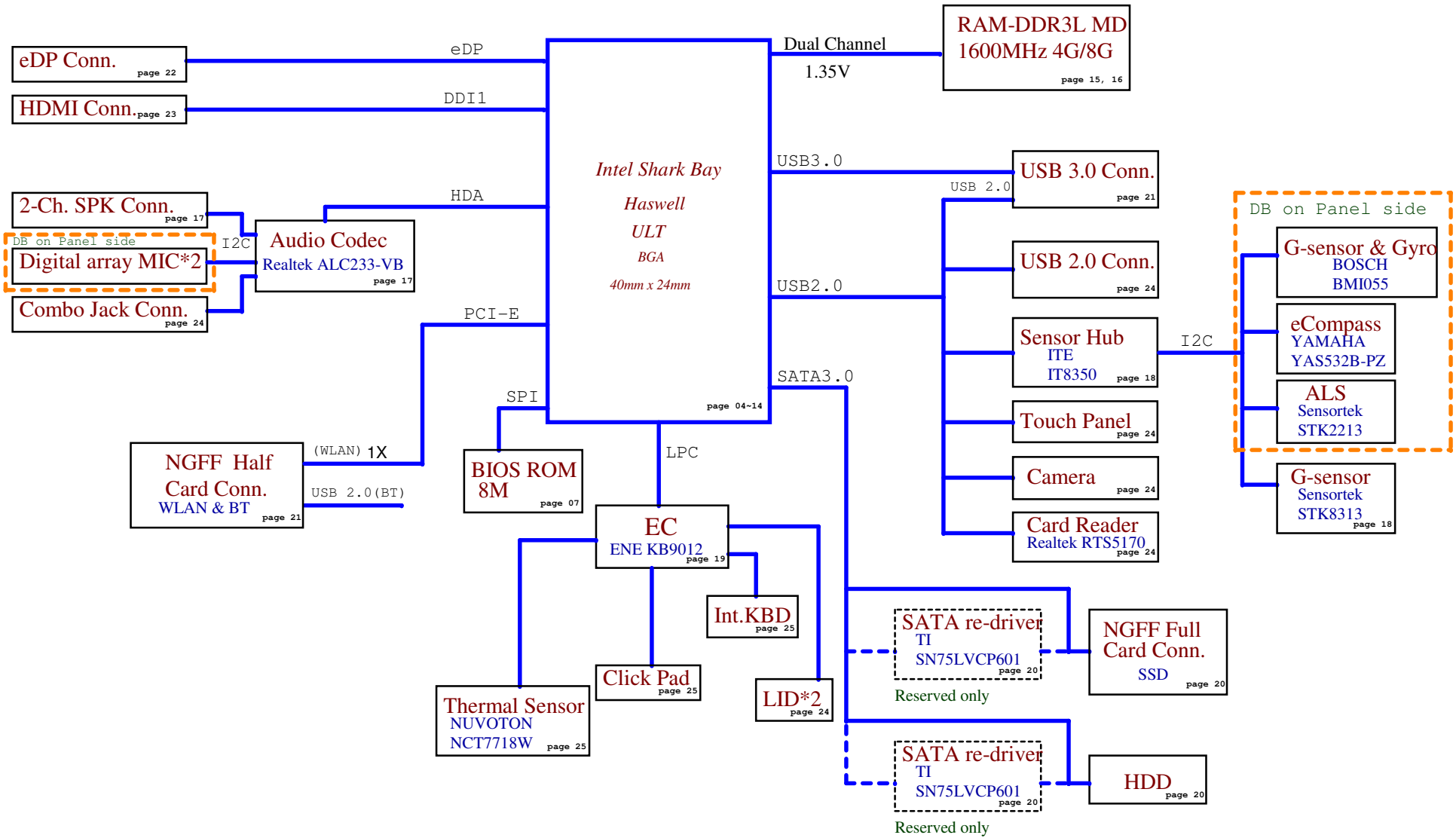
REV:1.0

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Model Name : ZIVY0
File Name : LA-A921P



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				MB Block Diagram	
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Voltage Rails

power plane	B+	+5VALW	+1.35V	+5VS +3VS +1.5VS +1.05VS_VTT +CPU_CORE +0.675VS
State		+3VALW		
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	✗	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

STATE	SIGNAL	SLP_S0#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

BOM Structure Table

BTO Item	BOM Structure
Connector	ME@
76 LEVEL	X76@
Unpop	@
CPU OPTION	CPU1@ ~ CPU5@
DRAM Option	H4G@ E4G@ S4G@ M4G@ S8G@ E8G@ H8G@ H8G@
KB9012	9012@
KB9022	9022@
No Re-driver	NR@
TI Re-driver	TI@
PARADE Re-driver	8520C@
Segate HDD	HDDSG@
WD HDD	HDDWD@
EMI PART	EMI@
ESD PART	ESD@
SSD-SATA	SSDSATA@

BOARD ID Table

Board ID	PCB Revision
0	1.0
1	0.3
2	0.2
3	0.1
4	
5	
6	
7	

USB 2.0 Port Table

Port	USB 2.0 Port	2 External USB Port
0		USB 2.0 Port (I/O Board)
1		USB 3.0/2.0 Port (MB)
2		
3		Card Reader
4		Touch Screen (reserve)
5		Camera
6		Mini Card (WLAN/BT)
7		Sensor Fusion

USB 3.0 Port Table

Port	USB 3.0 Port
1	
2	USB 3.0 Port (MB)
3	
4	

PCIe Port Table

Port	Lane	PCIe Port
1		
2		
3		
4		WLAN
5	0	
	1	
	2	
	3	
6	0	
	1	
	2	
	3	

SATA Port Table

Port	SATA Port
3	NGFF SSD(SATA)
2	
1	
0	HDD

EC SM Bus1 address

Device	Address
Smart Battery	
Charger	
Home Key Button	01100000

EC SM Bus2 address

Device	Address
Thermal Sensor NCT7718W	1001100x
SharkBay ULT SML1	

CPU SM Bus address

Device	Address
Touch Pad	

CPU SML0 Bus address

Device	Address

SMBUS Control Table

	HOST	Changer	BATT	KB9022	CPU	HomeKey	Touch Pad	Thermal sensor NCT7718W
EC_SMB_CK1	KB9022	✓	✓	✗	✗	✓	✗	✗
EC_SMB_DA1	+3VLP	+3VLP	+3VLP	✗	✗	+3VLP	✗	✗
EC_SMB_CK2	KB9022	✗	✗	✗	✓	✗	✗	✓
EC_SMB_DA2	+3VS				+3VS			+3VS
SMBCLK	CPU	✗	✗	✗	✗	✗	✓	✗
SMBDATA	+3VALW						+3VS	
SML0CLK	CPU	✗	✗	✗	✗	✗	✗	✗
SML0DATA	+3VALW							
SML1CLK	CPU	✗	✗	✓	✗	✗	✗	✓
SML1DATA	+3VS			+3VS				+3VS

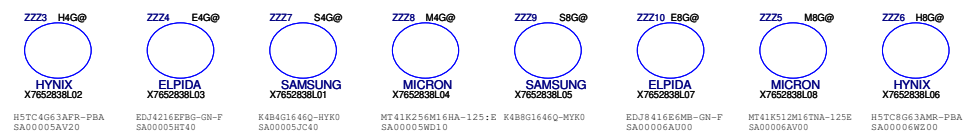
CPU part



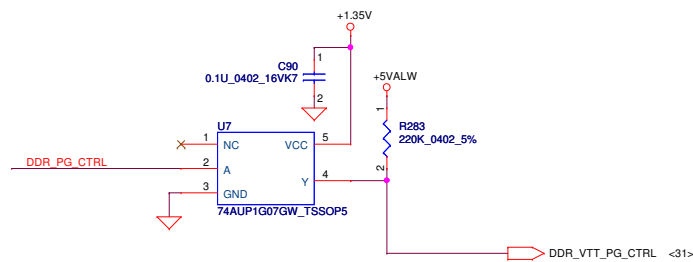
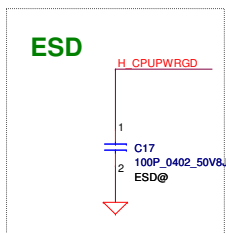
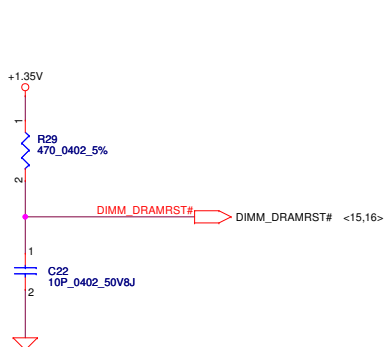
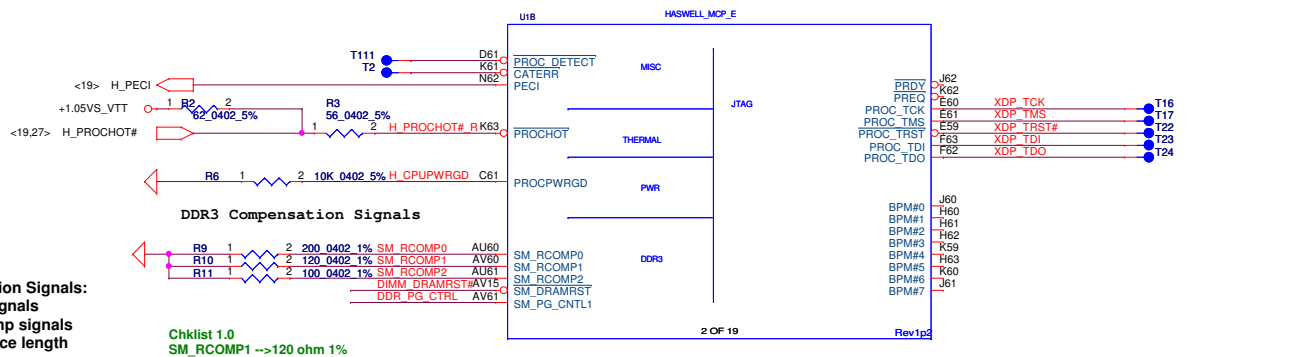
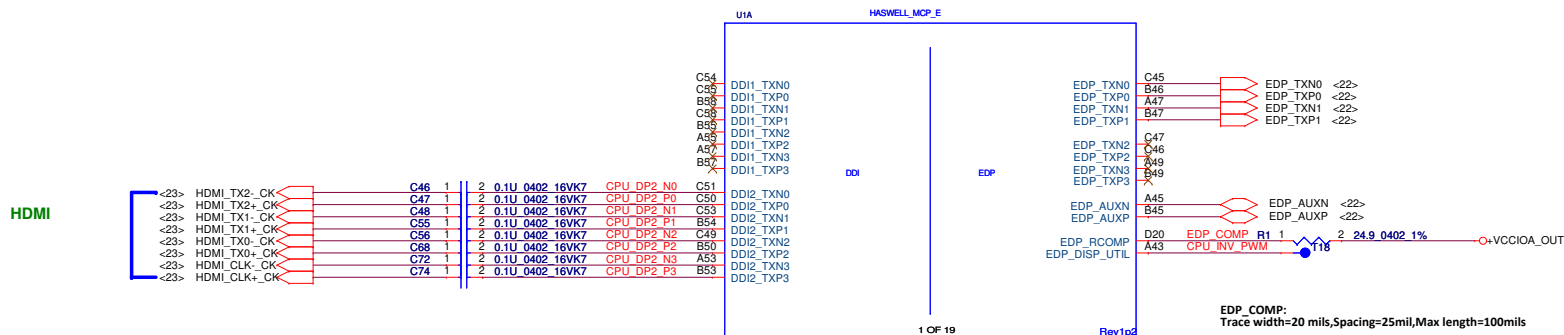
PCB part



DRAM



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Issued Date	2013/07/24	Deciphered Date	2015/07/24	Title	HSW MCP(1/11) DDI,MSIC,XDP
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				LA-A921PRO1	1.0
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<15> DDR_A_D[0..63]

<15> DDR_A_MA[0..15]

<15> DDR_A_DQS[0..7]

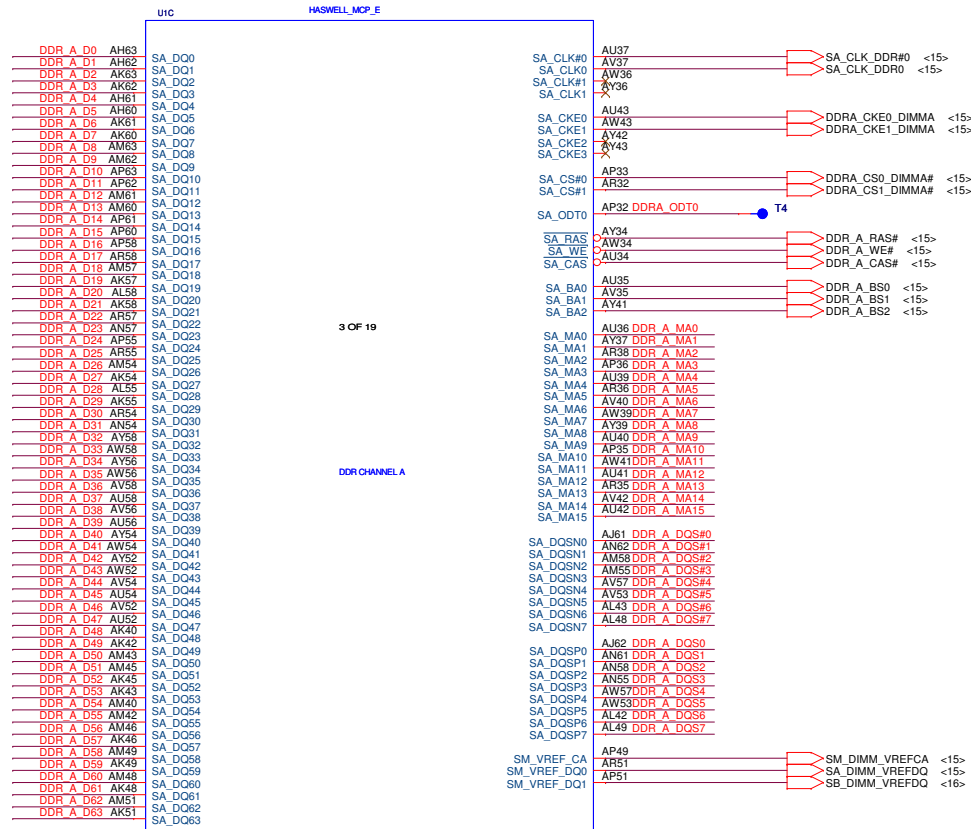
<15> DDR_A_DQS[0..7]

<16> DDR_B_D[0..63]

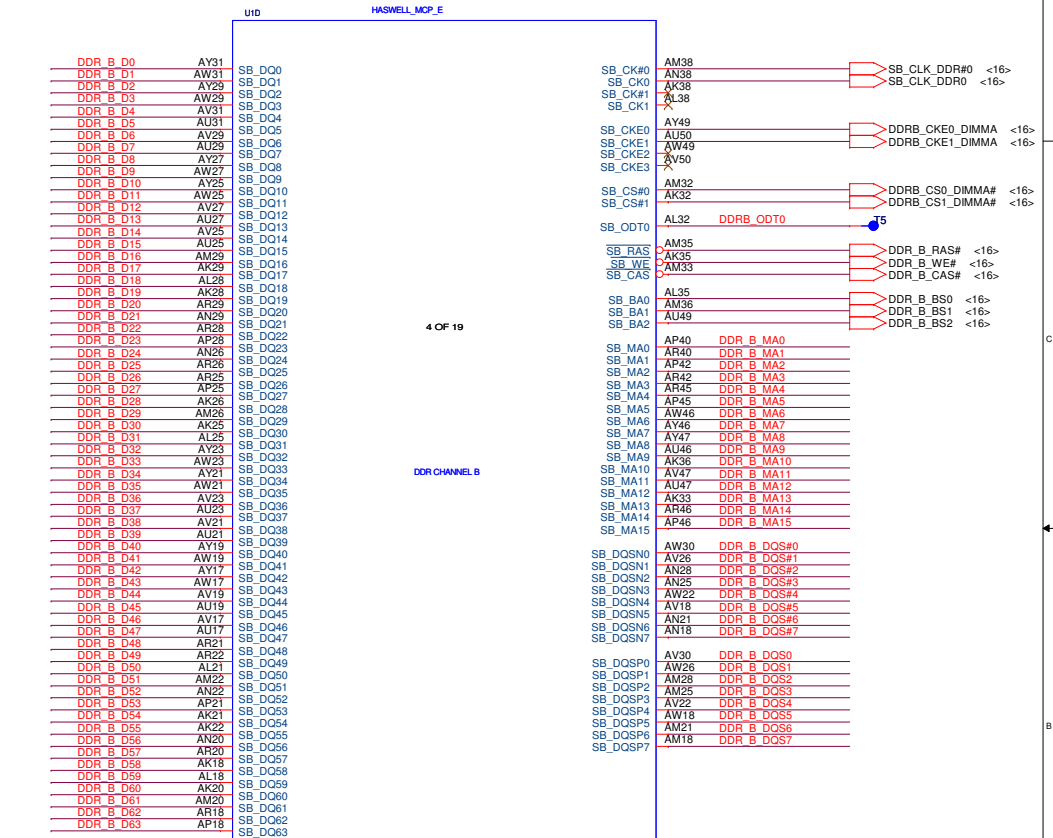
<16> DDR_B_MA[0..15]

<16> DDR_B_DQS[0..7]

<16> DDR_B_DQS[0..7]

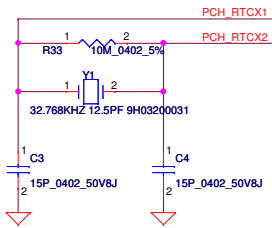


Rev1p2

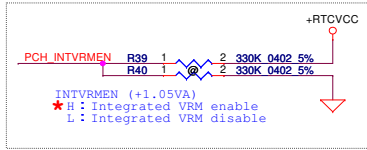
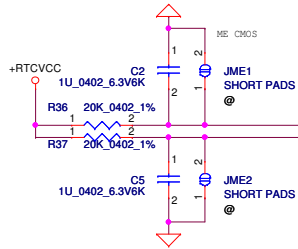


Rev1p2

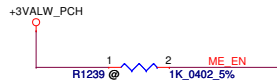
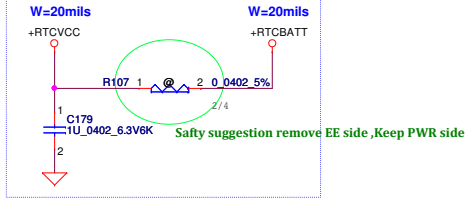
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Issued Date	2013/07/24	Deciphered Date	2015/07/24	Title HSW MCP(2/11) DDRIII	
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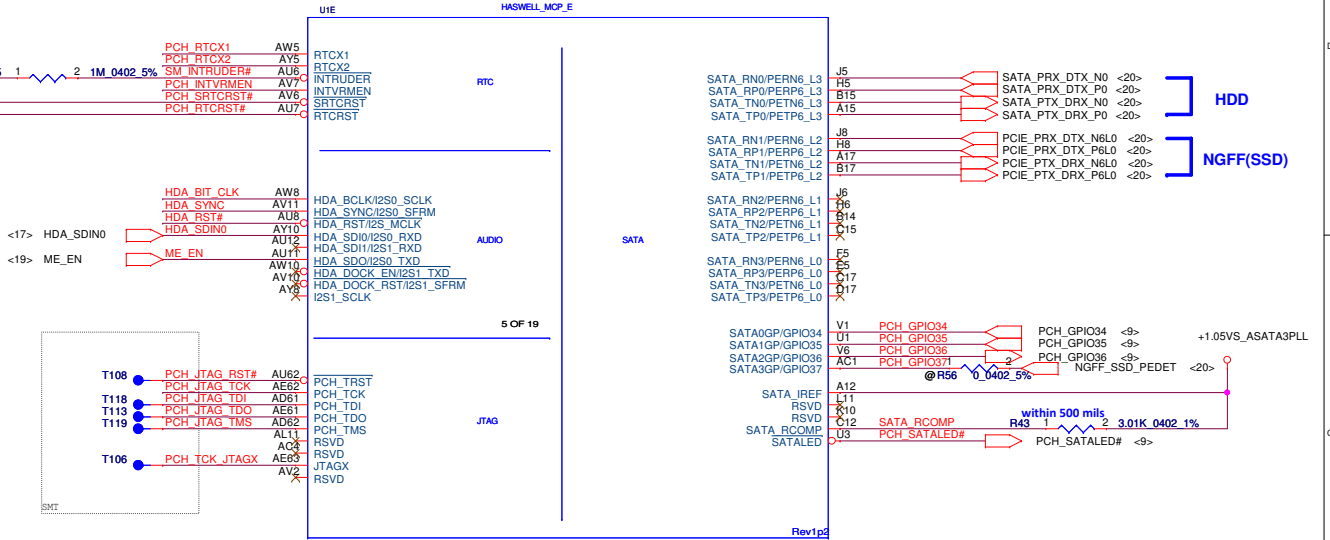
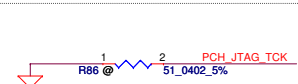
JME2 Short PAD placement to Bottom side.



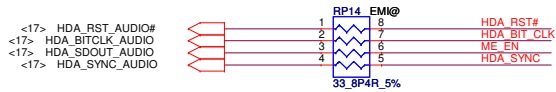
RTC Battery



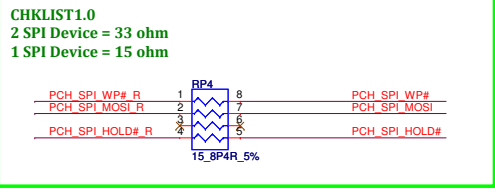
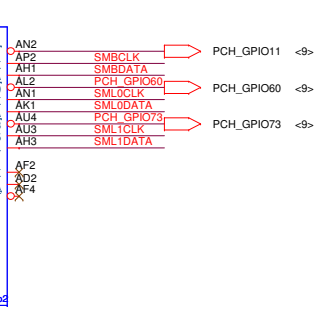
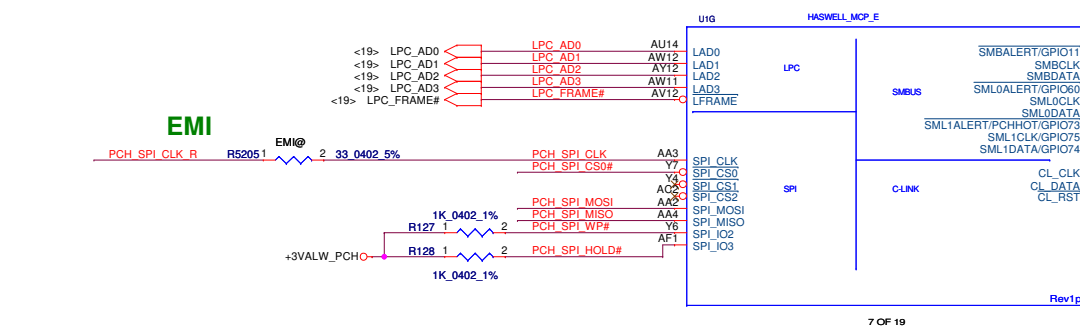
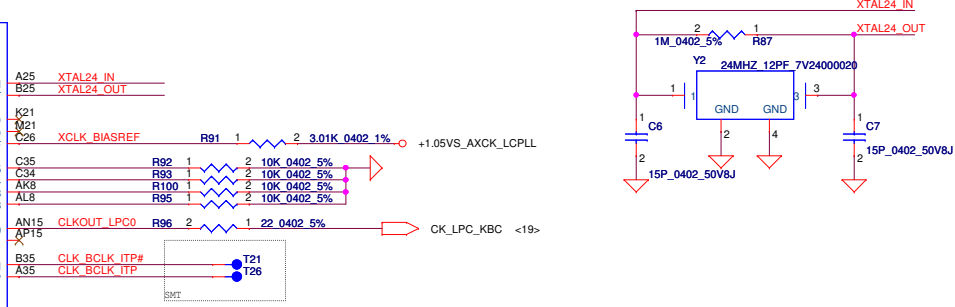
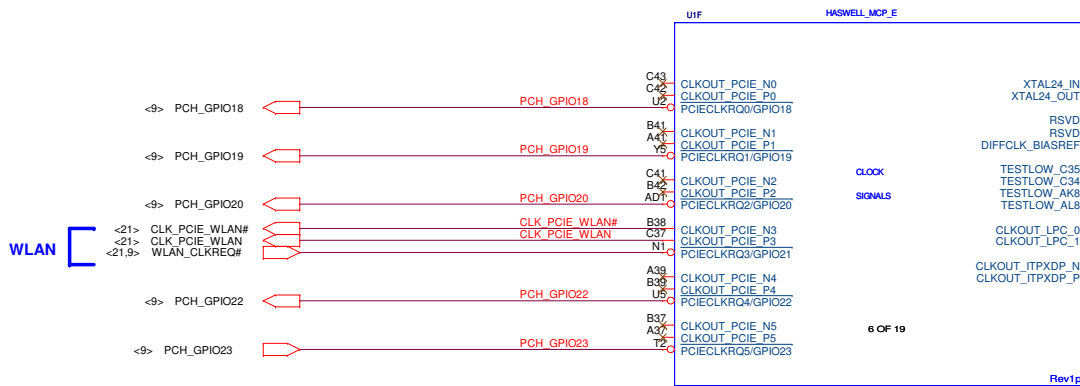
ME_EN
ME debug mode, this signal has a weak internal PD
* Low = Disabled (Default)
High = Enabled [Flash Descriptor Security Override]



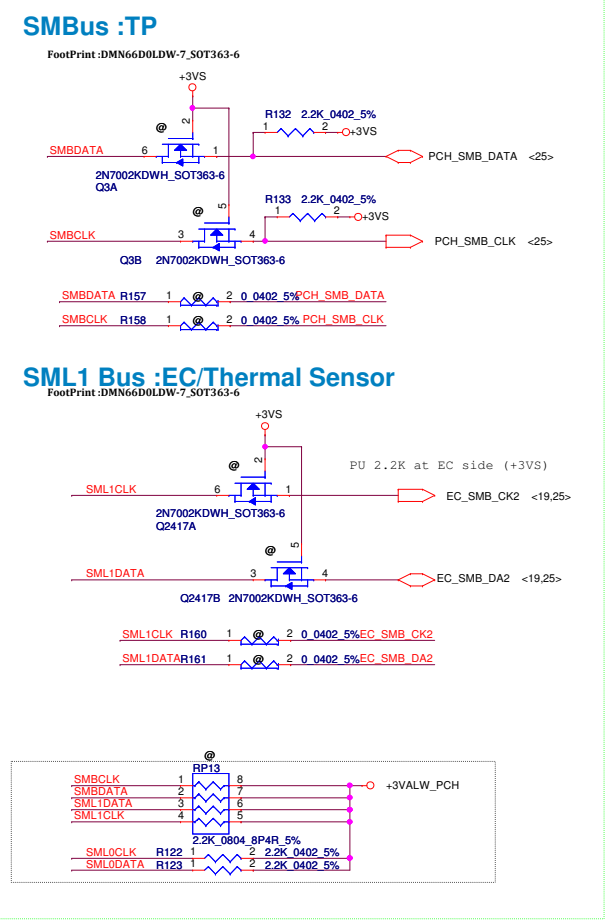
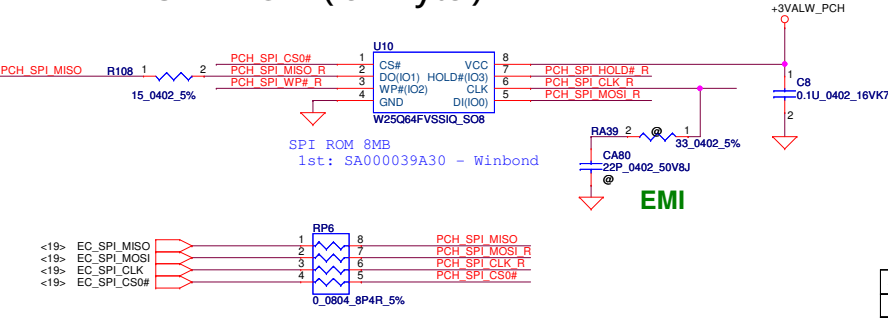
EMI



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SPI1 ROM (8MByte)



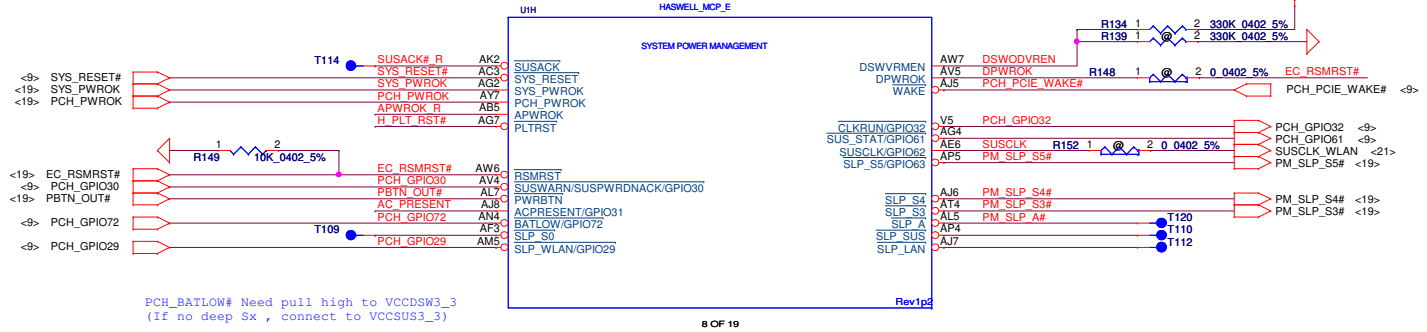
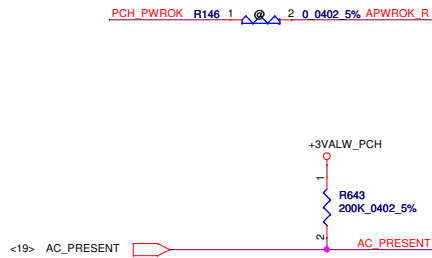
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Note: SUSACK# and SUSWARN# can be tied together if EC does not want to involve in the handshake mechanism for the Deep Sleep state entry and exit

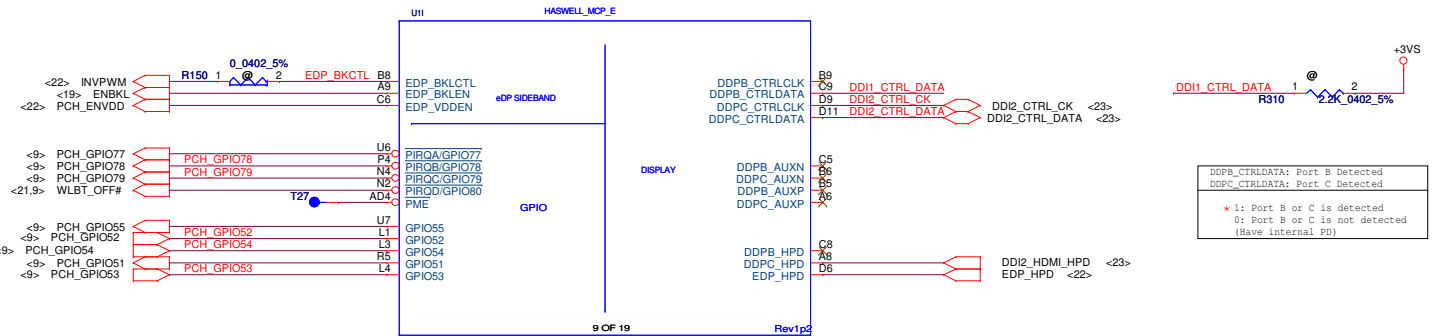
CAN be NC ,if not support Deep Sx

DPWROK: Tired together with RSMRST# that do not support Deep Sx

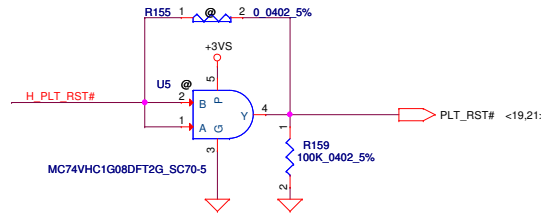
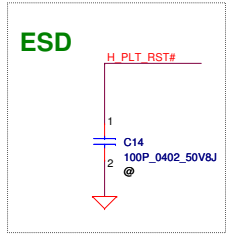
DSWODVREN - On Die DSW VR Enable
 * H : Enable (DEFAULT)
 L : Disable



PCH_BATLOW# Need pull high to VCCDSW3_3 (If no deep Sx , connect to VCCSUS3_3)

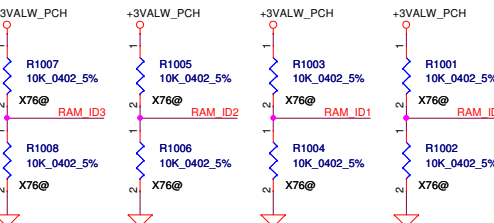
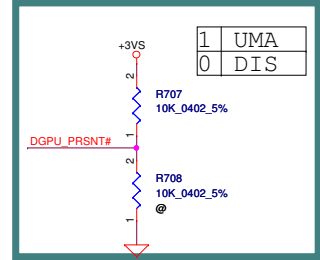
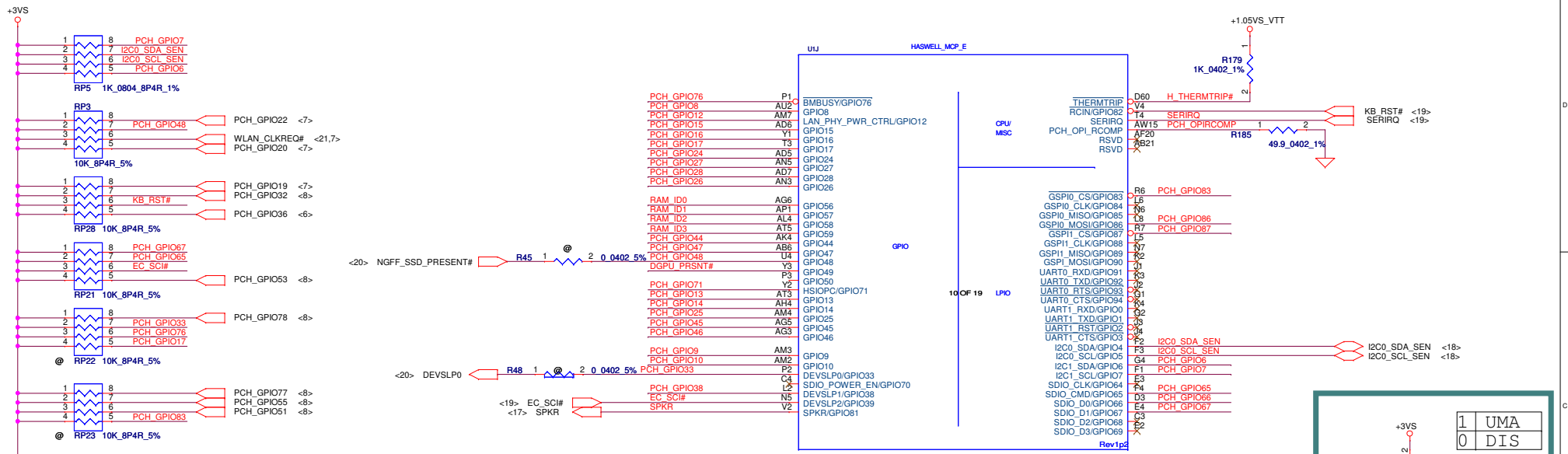


DDPB_CTRLDATA: Port B Detected
 DDPC_CTRLDATA: Port C Detected
 * 1: Port B or C is detected
 0: Port B or C is not detected (Have internal PD)



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RAM_ID3	RAM_ID2	RAM_ID1	RAM_ID0	RAM P/N
GPIO59	GPIO58	GPIO57	GPIO56	
0	0	0	0	HYNIX H5TC4G63AFB-PBA
0	0	0	1	SAMSUNG K4B4G1646Q-HYK0
0	0	1	0	MICRON MT41K256M16HA-125:E
0	0	1	1	ELPIDA EDJ4216EFBG-GN-F
0	1	0	0	SAMSUNG K4B8G1646Q-MYK0
0	1	0	1	ELPIDA EDJ8416E6MB-GN-F
0	1	1	0	MICRON MT41K512M16TNA-125:E
0	1	1	1	HYNIX H5TC8G63AMR-PBA
1	0	0	0	TBD
1	0	0	1	TBD
1	0	1	0	TBD
1	0	1	1	TBD
1	1	0	0	TBD
1	1	0	1	TBD
1	1	1	0	TBD
1	1	1	1	TBD

GPIO0_MOSI / GPIO86 : Boot BIOS Strap

1: LPC BUS

* 0: SPI BUS (Have internal PD)

SDIO_D0 / GPIO66 : Top-Block Swap Override

1: DISABLED

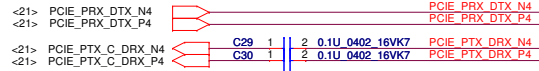
* 0: ENABLED (Have internal PD)

GPIO15 : TLS Confidentiality

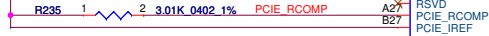
1: Intel ME TLS with confidentiality

* 0: Intel ME TLS with no confidentiality (Have internal PD)

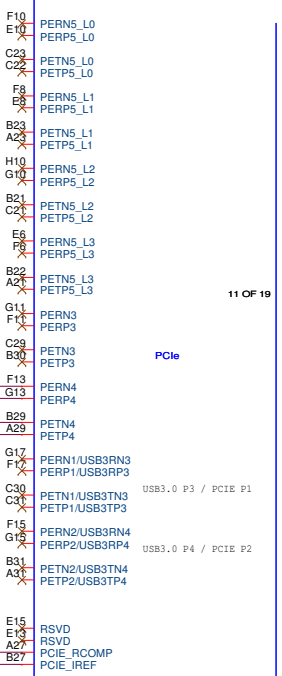
WLAN



+1.05VS_AUSB3PLL



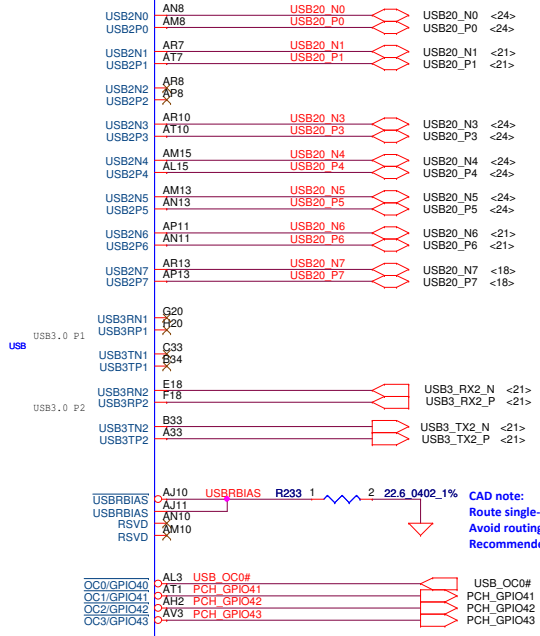
UKK HASWELL_MCP_E



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PCIE

USB



- USB2 IO (Sub Board)
- USB2/3 IO (Main Board)
- Card Reader
- Touch Screen
- Camera
- Mini Card(WLAN+BT)
- Sensor

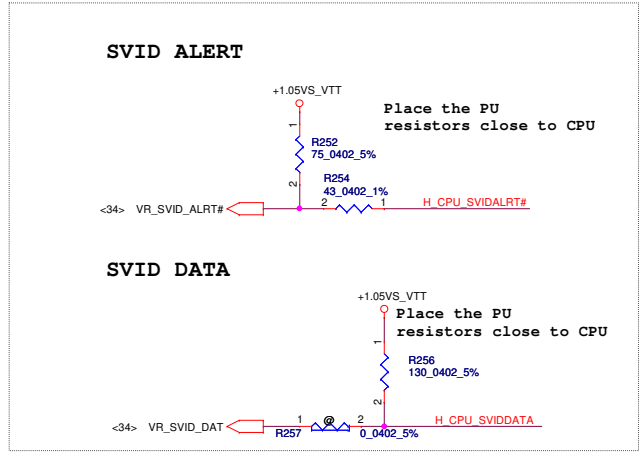
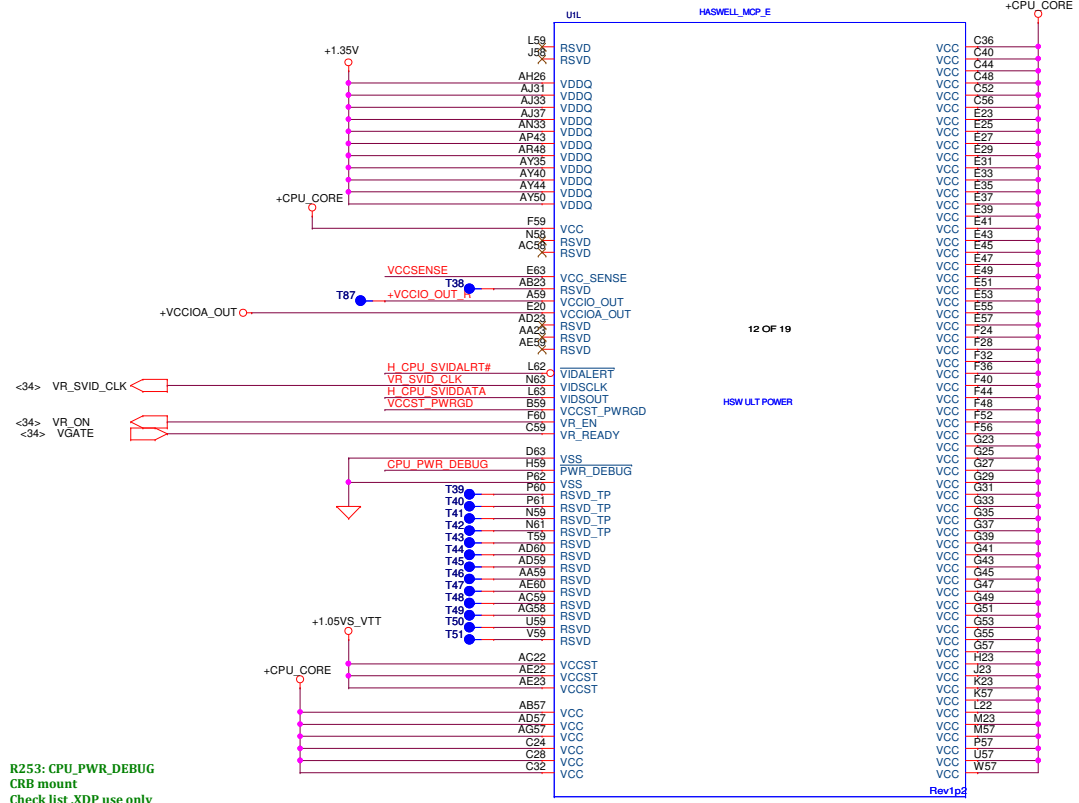
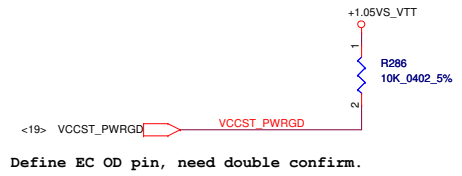
USB2/3 (Main Board)

CAD note:
Route single-end 50-ohms and max 450-mils length.
Avoid routing next to clock pins or under stitching capacitors.
Recommended minimum spacing to other signal traces is 15 mils

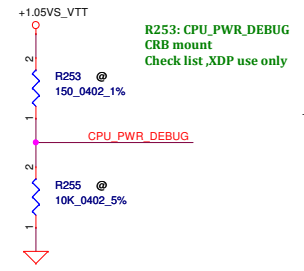
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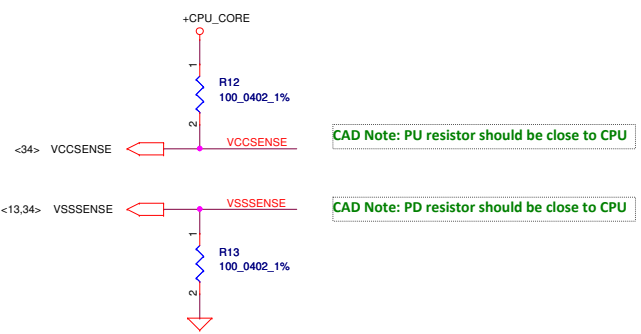


R256:
CRB r0.7 changed from 130 Ohms to 110 Ohms



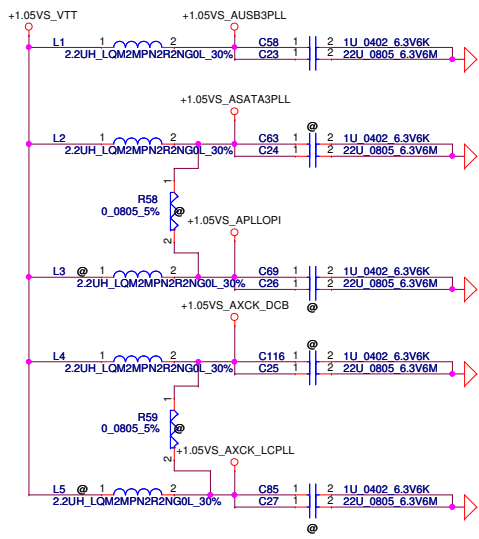
VDDQ DECOUPLING

CRB:
+1.35V: 470UF/2V/7343 *2 (Un-mount)
10UF/6.3V/0603 * 6
2.2UF/6.3V/0402 * 4



Security Classification	Compal Secret Data		Title	
Issued Date	2013/07/24	Deciphered Date	2015/07/24	HSW MCP(8/11) Power
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Check Power Source Close to N8
 +1.05VS_VTT @ C53 1 2 1U 0402 6.3V6K



Close to K9, M9
 +1.05VS_VTT @ C49 1 2 1U 0402 6.3V6K
 C50 1 2 1U 0402 6.3V6K

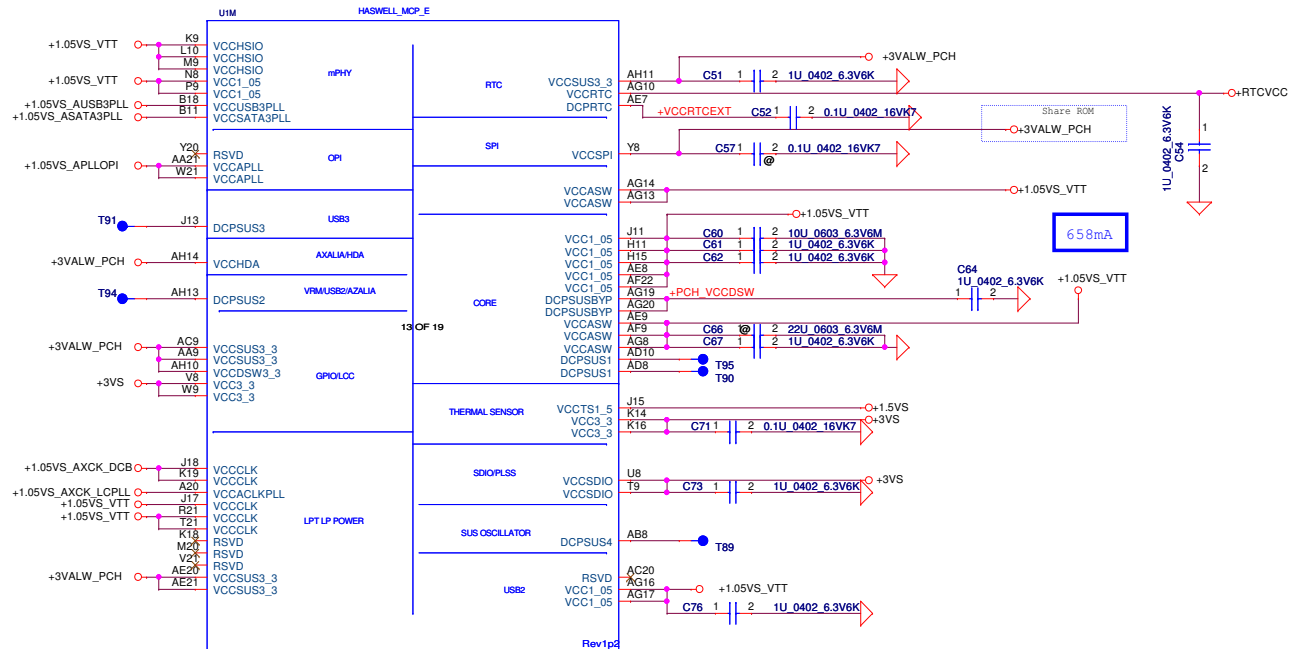
Close to AC9/AA9/AE20/AE21
 +3VALW_PCH @ C78 1 2 22U 0603 6.3V6M

Close to V8
 +3VS @ C82 1 2 22U 0603 6.3V6M

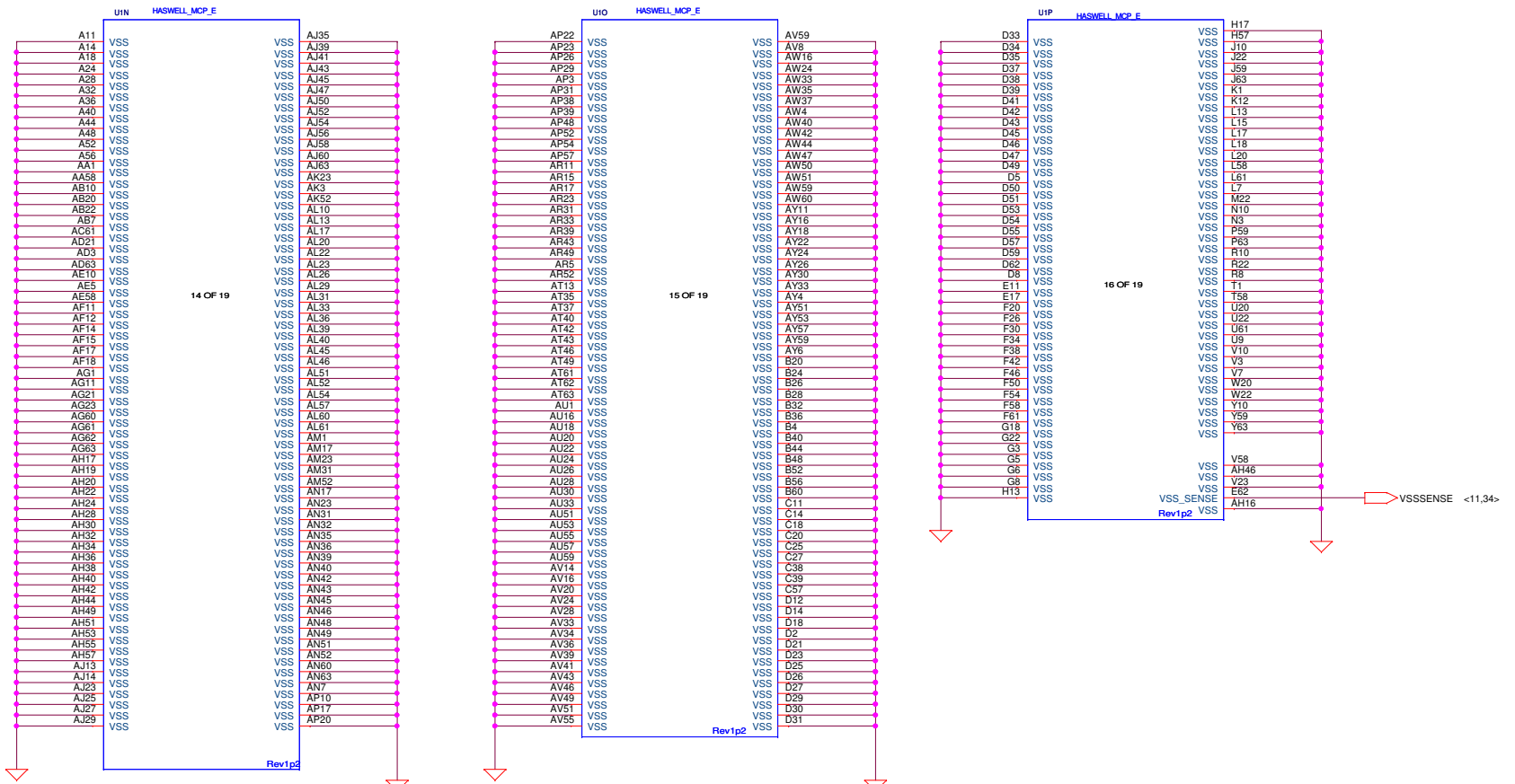
Close to J17
 +1.05VS_VTT @ C87 1 2 1U 0402 6.3V6K

Close to R21
 +1.05VS_VTT @ C88 1 2 1U 0402 6.3V6K

Close to AH14
 +3VALW_PCH @ C75 2 1 1U 0402 6.3V6K

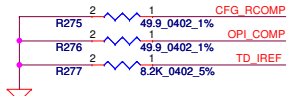
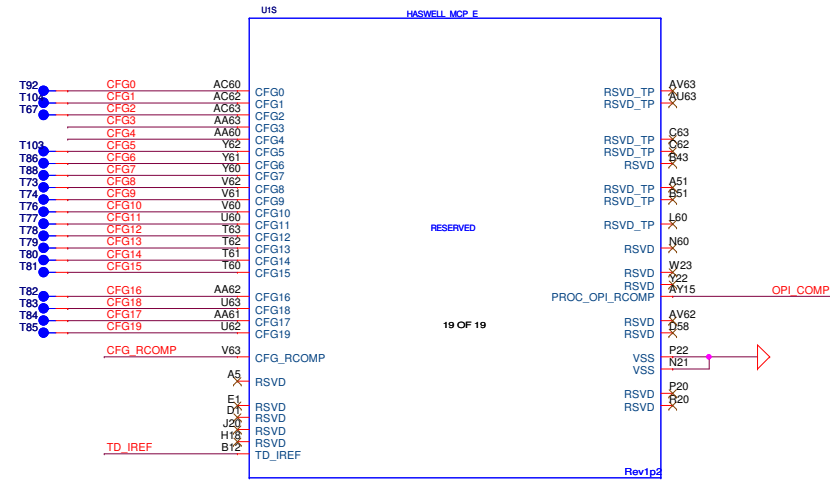
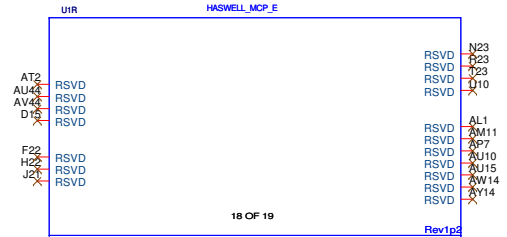
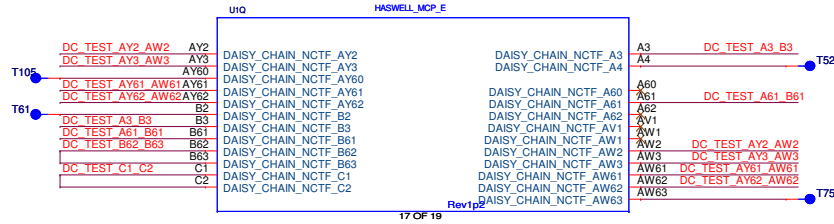


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			Date: Tuesday, December 17, 2013	Sheet	12 of 38

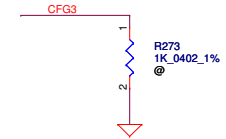


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Issued Date	2013/07/24	Deciphered Date	2015/07/24	Title
				HSW MCP(10/11) GND
<small>THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE COMPANY OR REPRODUCED IN ANY MANNER WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</small>				Document Number LA-A921PR01 Date: Tuesday, December 17, 2013
				Rev 1.0
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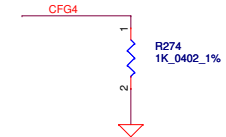
WWW.VIETAX.VN



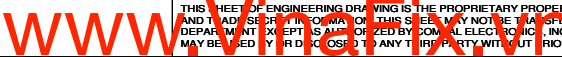
CFG Straps for Processor






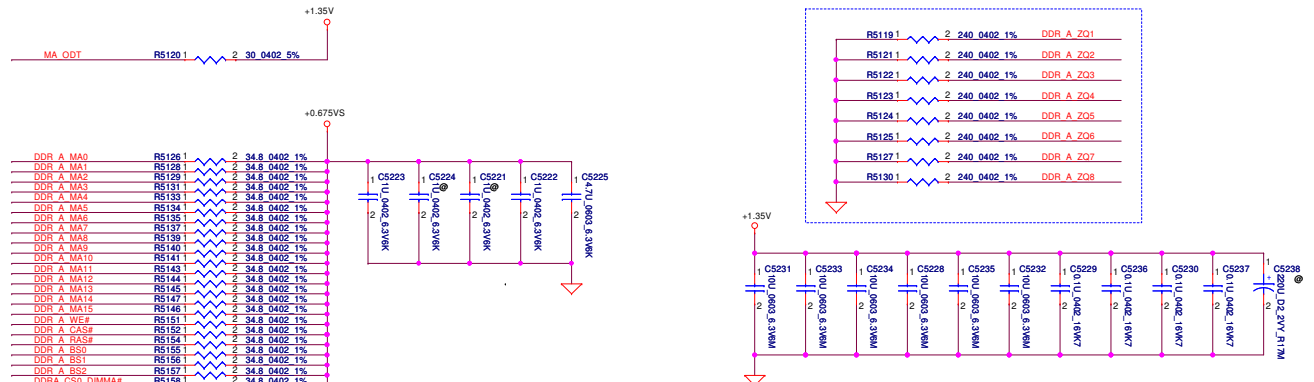
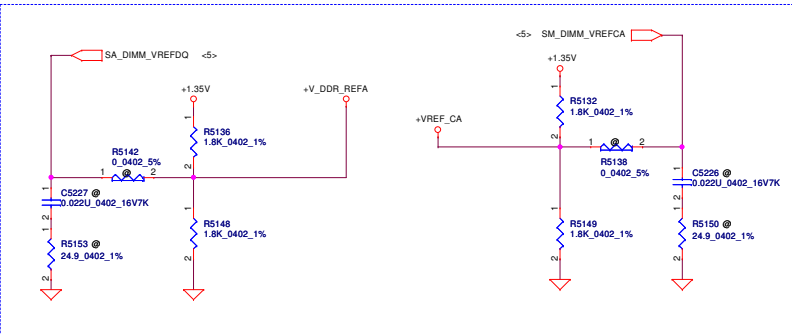
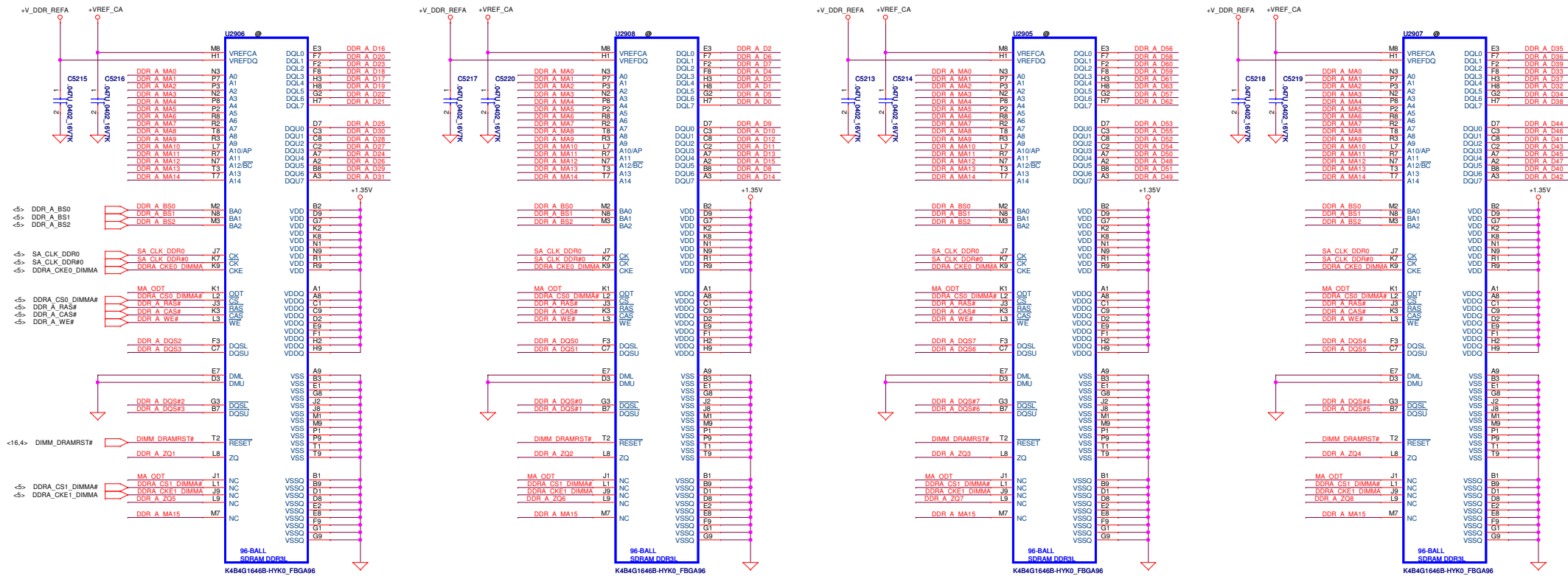
Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port



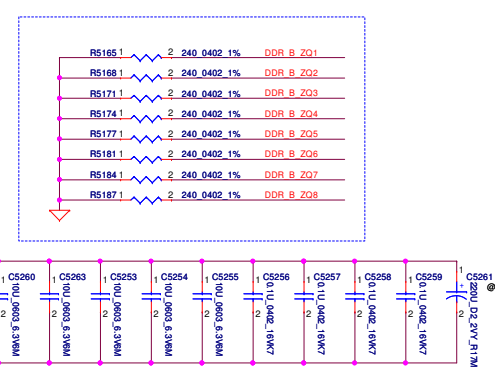
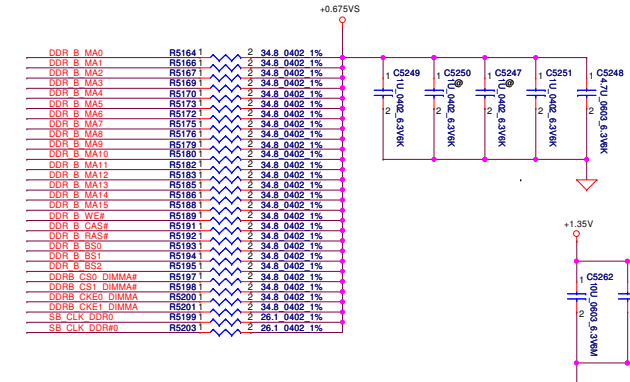
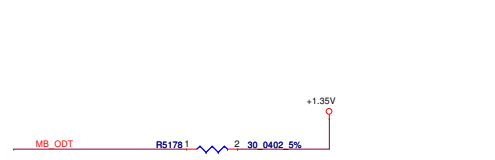
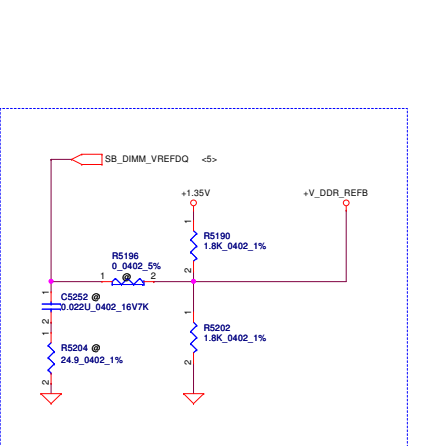
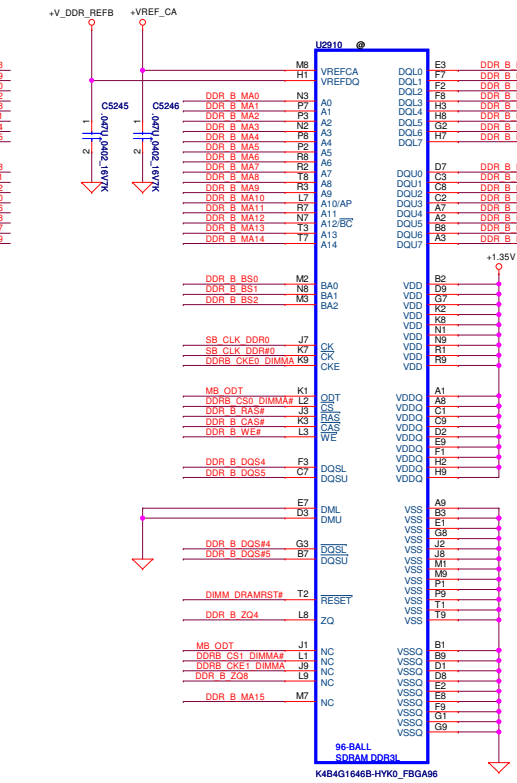
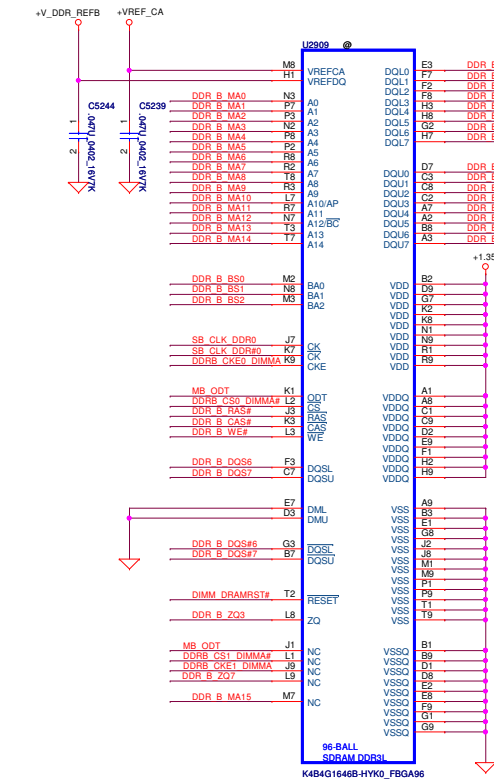
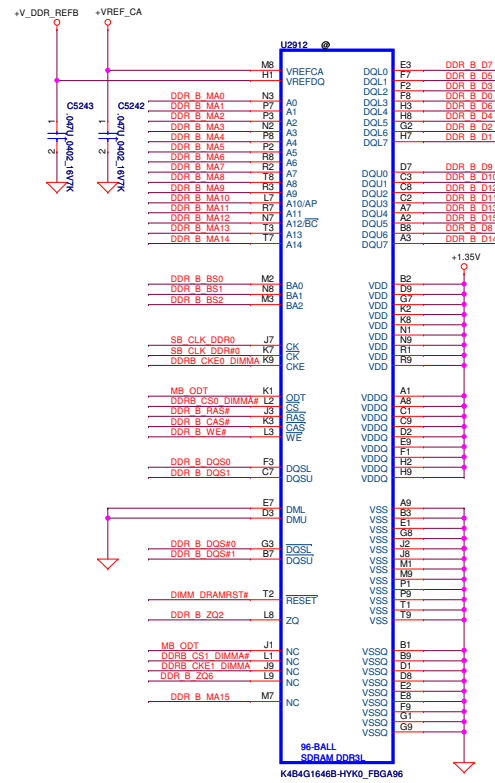
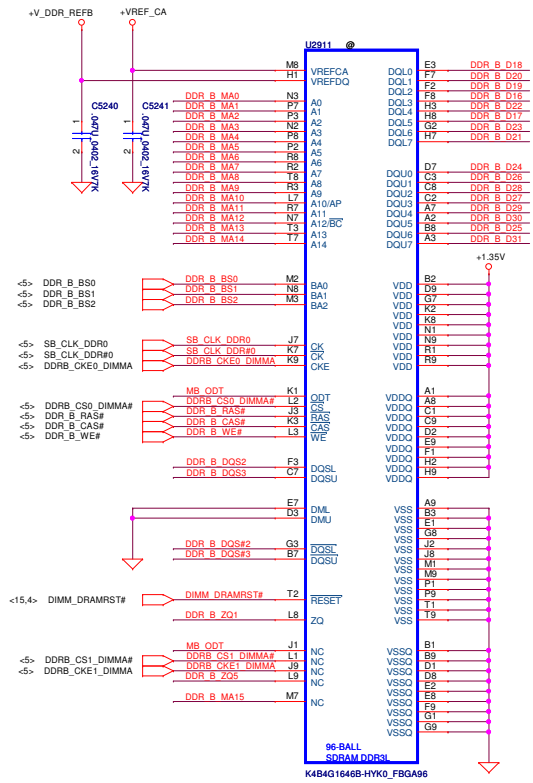
- <S> DDR_A_MA[0..15]  DDR A MA[0..15]
- <S> DDR_A_DQS[0..7]  DDR A DQS[0..7]
- <S> DDR_A_DQS[0..7]  DDR A DQS[0..7]
- <S> DDR_A_D[0..63]  DDR A D[0..63]



DDR_A_MA0	R5126 1	2	34.8	0402	1%
DDR_A_MA1	R5126 1	2	34.8	0402	1%
DDR_A_MA2	R5129 1	2	34.8	0402	1%
DDR_A_MA3	R5131 1	2	34.8	0402	1%
DDR_A_MA4	R5131 1	2	34.8	0402	1%
DDR_A_MA5	R5134 1	2	34.8	0402	1%
DDR_A_MA6	R5135 1	2	34.8	0402	1%
DDR_A_MA7	R5137 1	2	34.8	0402	1%
DDR_A_MA8	R5139 1	2	34.8	0402	1%
DDR_A_MA9	R5140 1	2	34.8	0402	1%
DDR_A_MA10	R5141 1	2	34.8	0402	1%
DDR_A_MA11	R5143 1	2	34.8	0402	1%
DDR_A_MA12	R5144 1	2	34.8	0402	1%
DDR_A_MA13	R5145 1	2	34.8	0402	1%
DDR_A_MA14	R5147 1	2	34.8	0402	1%
DDR_A_MA15	R5148 1	2	34.8	0402	1%
DDR_A_WE#	R5151 1	2	34.8	0402	1%
DDR_A_CAS#	R5152 1	2	34.8	0402	1%
DDR_A_BS0	R5153 1	2	34.8	0402	1%
DDR_A_BS1	R5154 1	2	34.8	0402	1%
DDR_A_BS2	R5157 1	2	34.8	0402	1%
DDR_A_CS0_DIMMA#	R5158 1	2	34.8	0402	1%
DDR_A_CS1_DIMMA#	R5159 1	2	34.8	0402	1%
DDR_A_CKE1_DIMMA	R5160 1	2	34.8	0402	1%
DDR_A_CKE2_DIMMA	R5161 1	2	34.8	0402	1%
SA_CLK_DDR#0	R5162 1	2	26.1	0402	1%
SA_CLK_DDR#0	R5163 1	2	26.1	0402	1%

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				Sheet	15 of 38

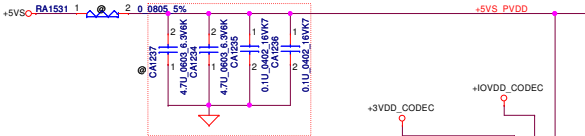
- <5> DDR_B_MA[0..15] ↔ DDR_B_MA[0..15]
- <5> DDR_B_DQS[0..7] ↔ DDR_B_DQS[0..7]
- <5> DDR_B_DQ[0..7] ↔ DDR_B_DQ[0..7]
- <5> DDR_B_DQ[8..31] ↔ DDR_B_DQ[8..31]



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			Size	DDRIII ON BOARD
			Customer	LA-A921PR01
			Date	Tues, December 17, 2013
			Sheet	16 of 38

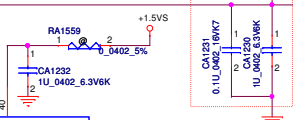
600ohms @100MHz 2A
P/N: SM01000EE00

Place near Pin41 & 46

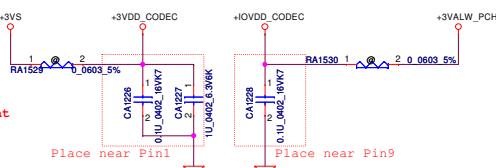


+5VDDA_CODEC

Place near Pin26



Place LA41 on AGND/DGND moat



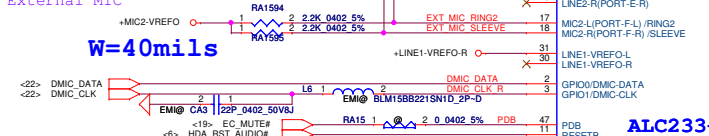
Place near Pin1

Place near Pin9

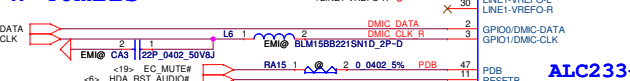
For EMI



External MIC
W=40mils



W=40mils



PC BEEP



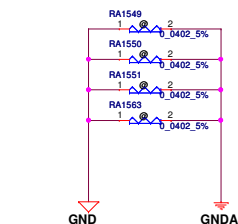
For ALC233-VB



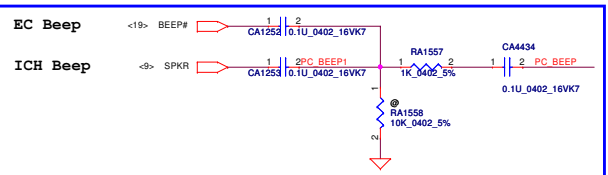
ALC233-CG

ALC233-VB2_MQFN48_6X6

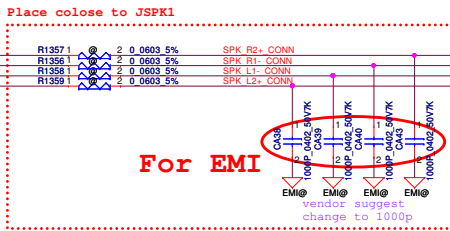
Place close to UAI



PC BEEP

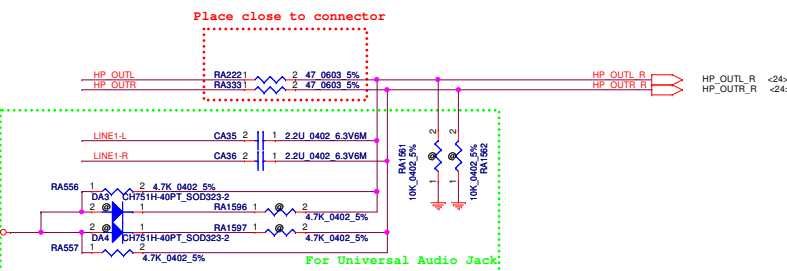


W=40mils



For EMI

Place close to JSPK1



Place close to connector

Place close to connector

Place close to connector

Place close to connector

Place close to connector

Place close to connector

Place close to connector

Place close to connector

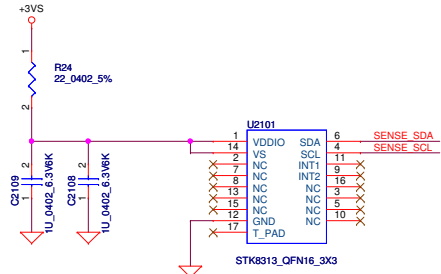
Place close to connector

Place close to connector

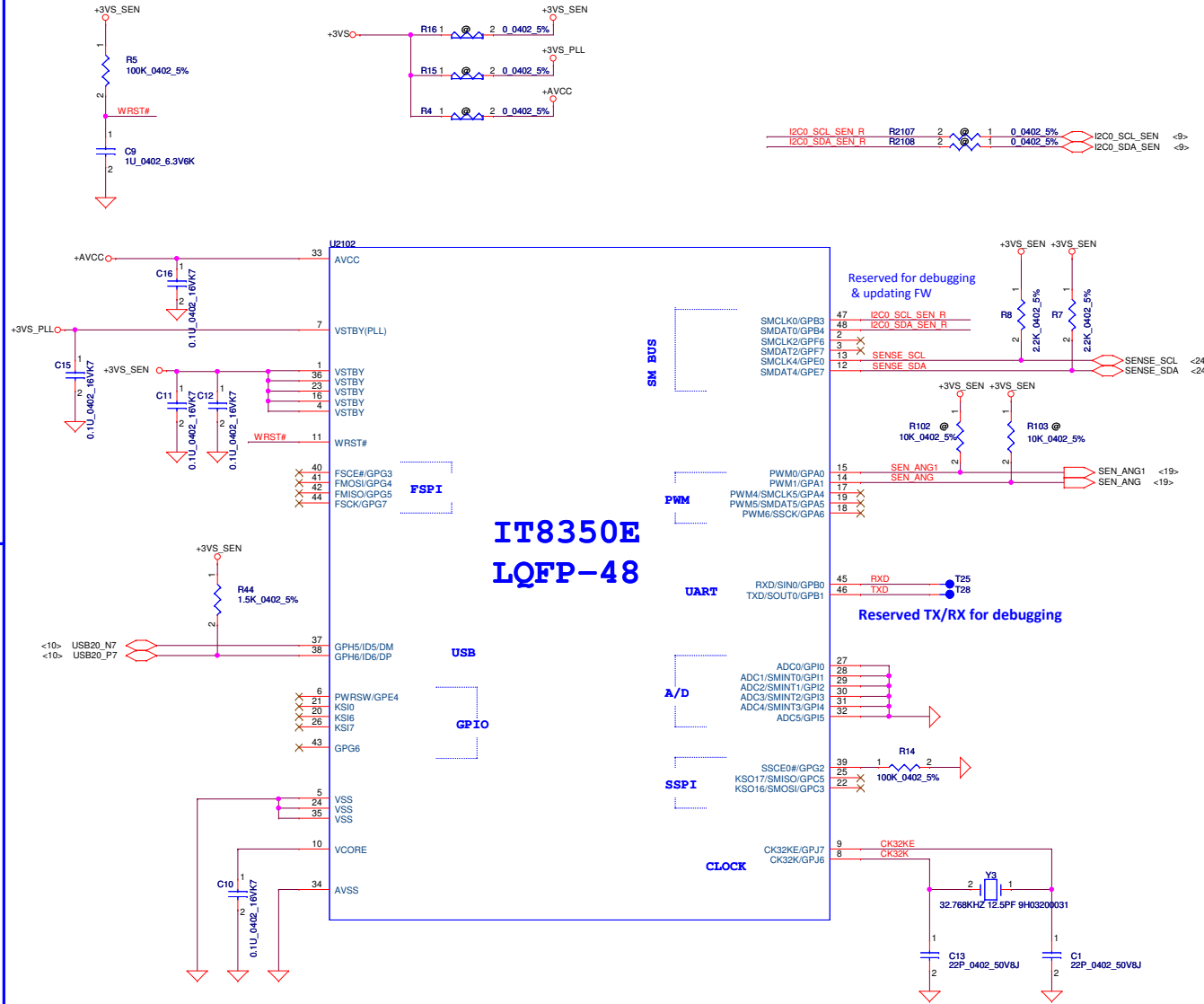
Place close to connector

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2nd G-sensor



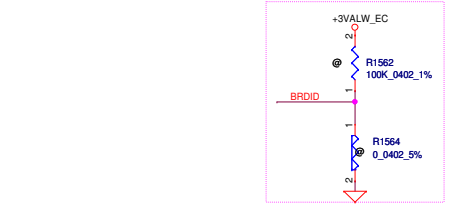
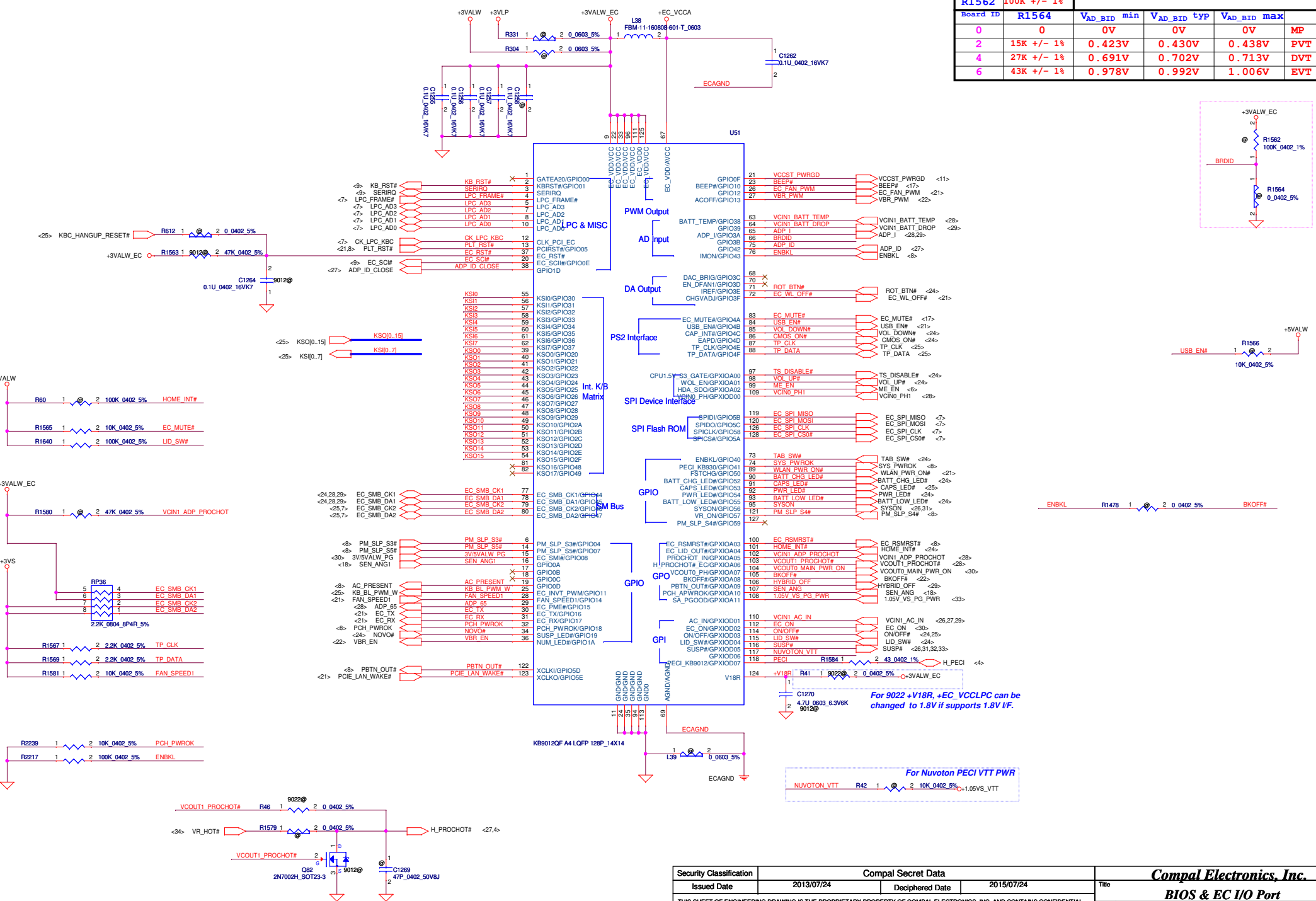
Sensor Hub



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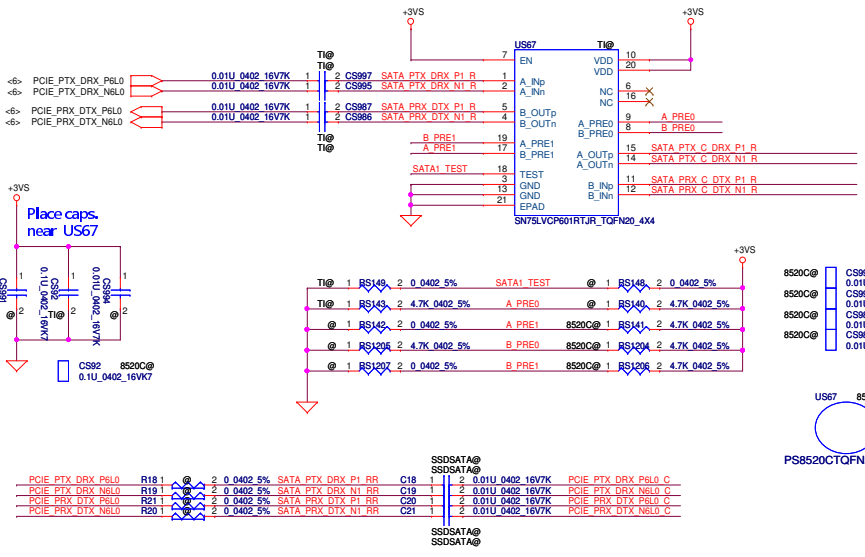
Vcc	3.3V				
R1562	100K +/- 1%	V _{AD_BID} min	V _{AD_BID} typ	V _{AD_BID} max	
0	0	0V	0V	0V	MP
2	15K +/- 1%	0.423V	0.430V	0.438V	PVT
4	27K +/- 1%	0.691V	0.702V	0.713V	DVT
6	43K +/- 1%	0.978V	0.992V	1.006V	EVT



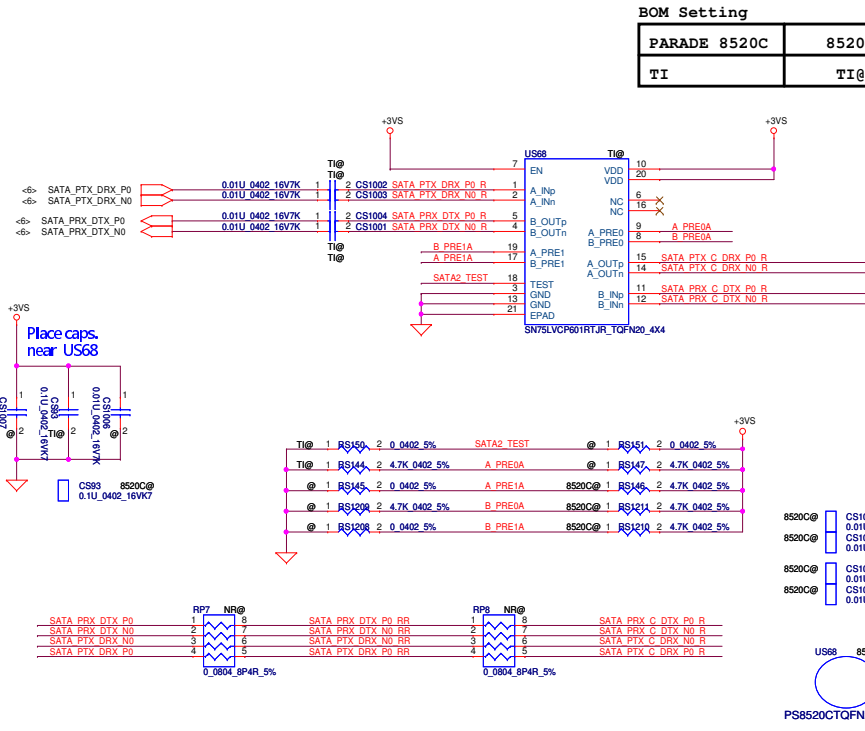
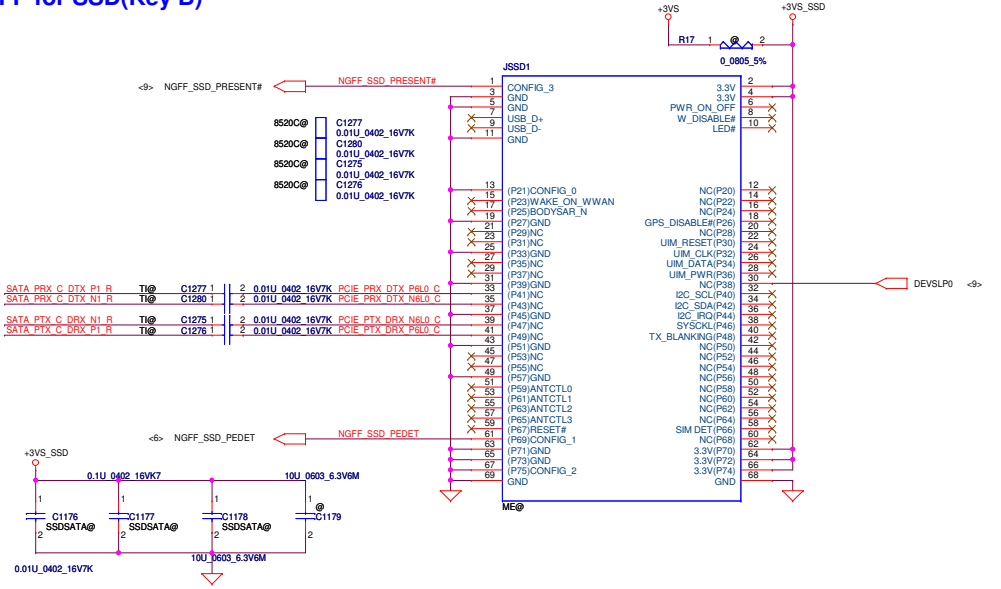
For 9022 +V18R, +EC_VCC_LPC can be changed to 1.8V if supports 1.8V I/F.

For Nuvoton PECE VTT PWR

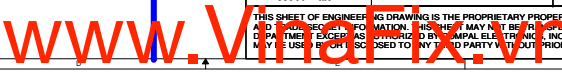
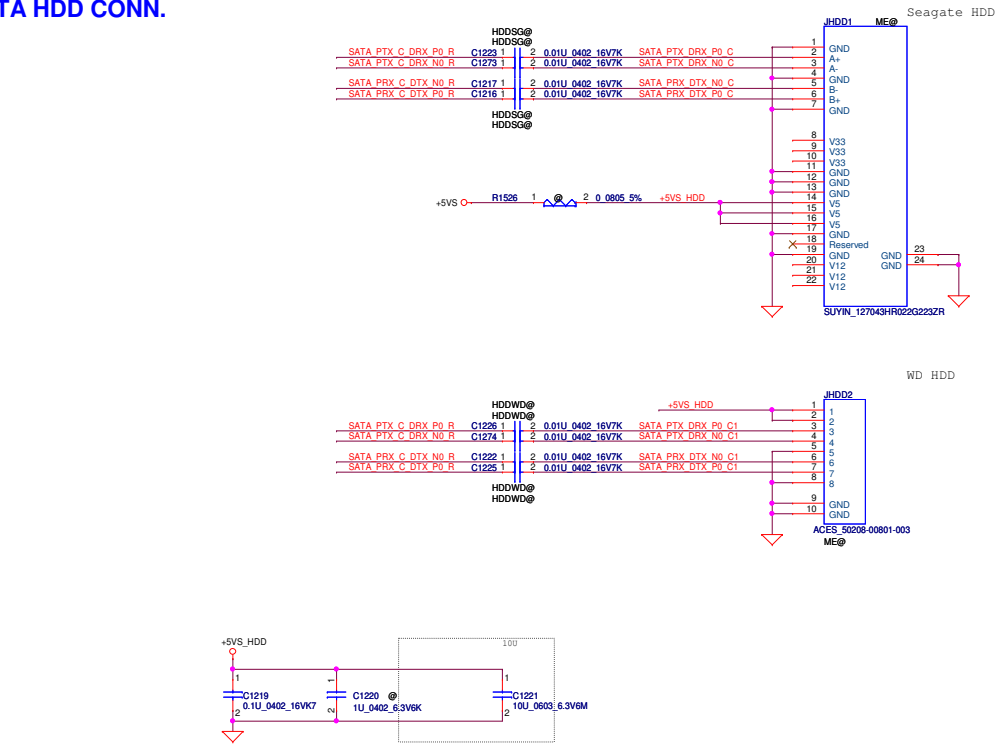
Security Classification		Compal Secret Data		Title	
Issued Date	2013/07/24	Deciphered Date	2015/07/24	BIOS & EC I/O Port	
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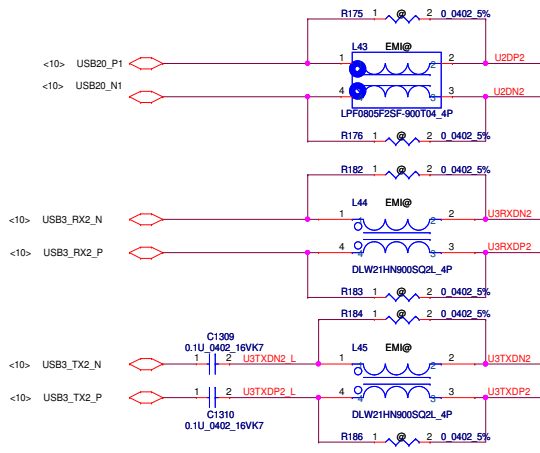
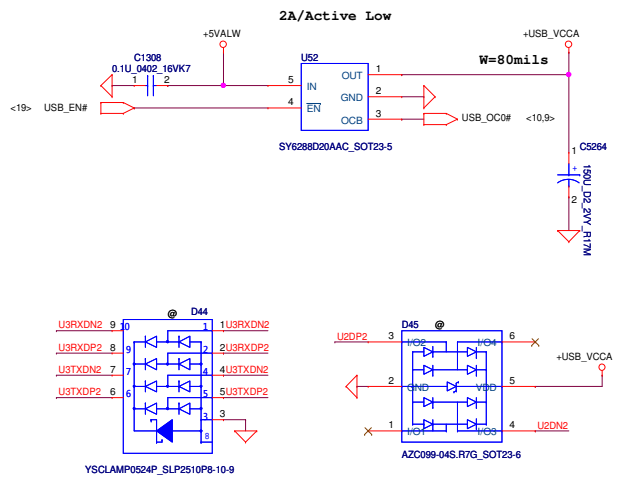
NGFF for SSD(Key B)



SATA HDD CONN.

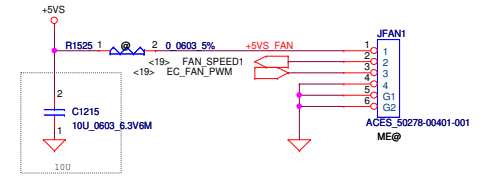


USB 3.0 Conn.

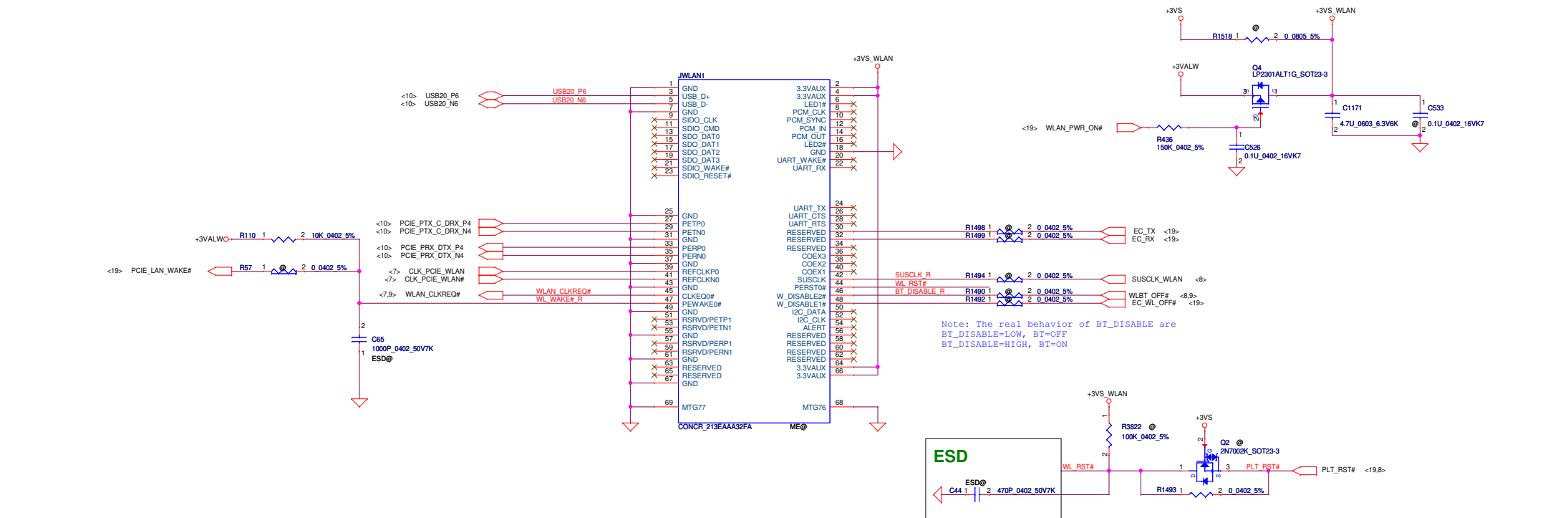


Place TX AC coupling Cap (C843-C850). Close to connector

FAN CONN.

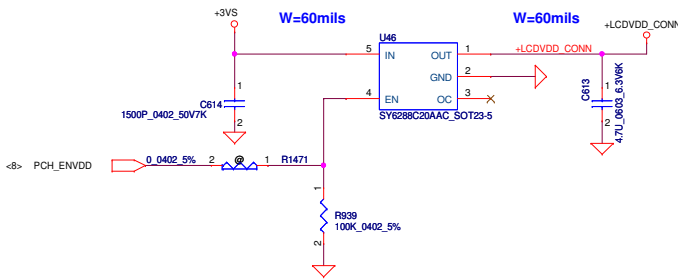


NGFF for WLAN(Key E)

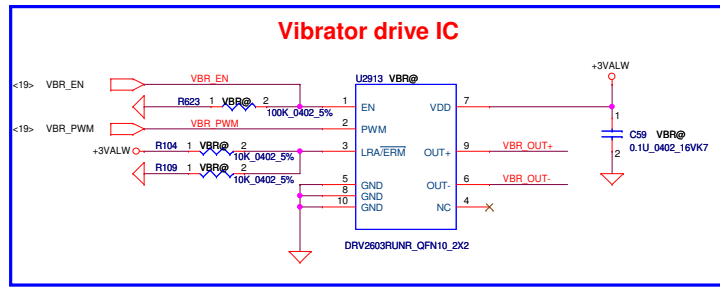


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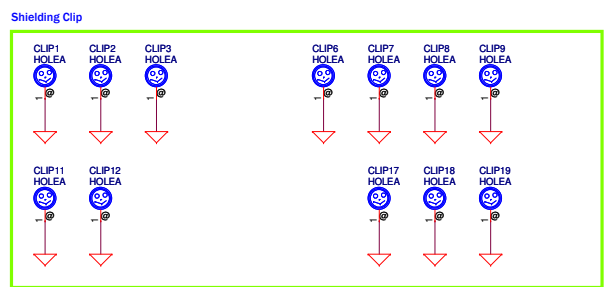
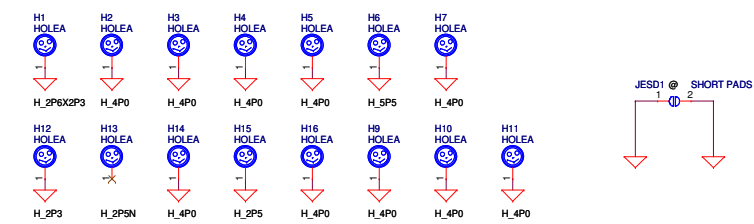
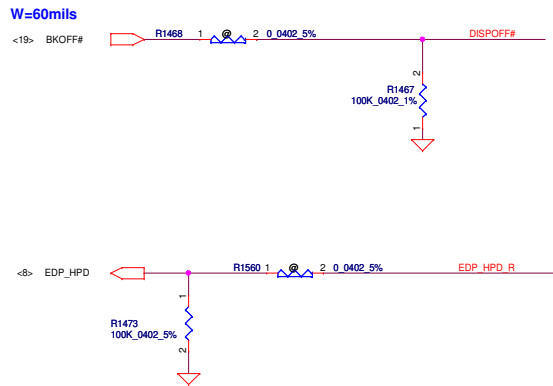
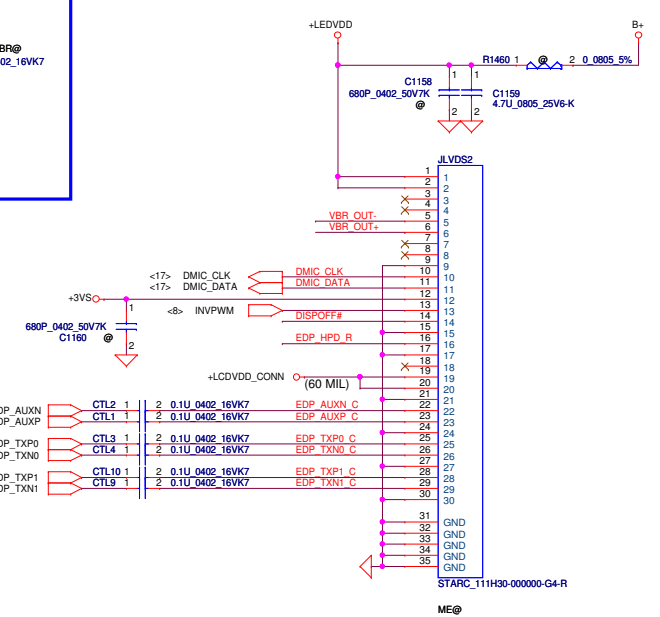
LCD POWER CIRCUIT



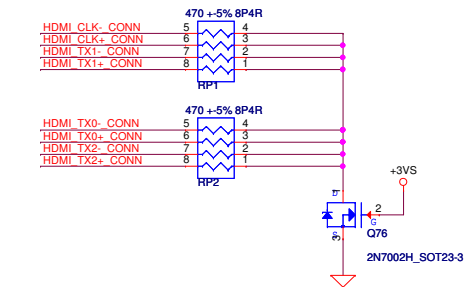
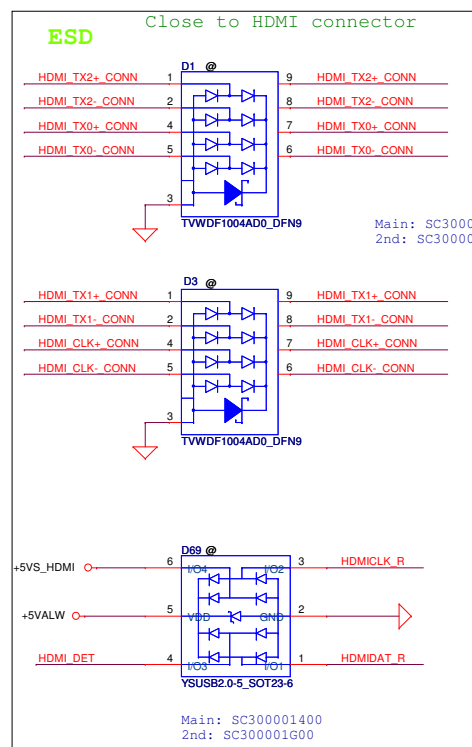
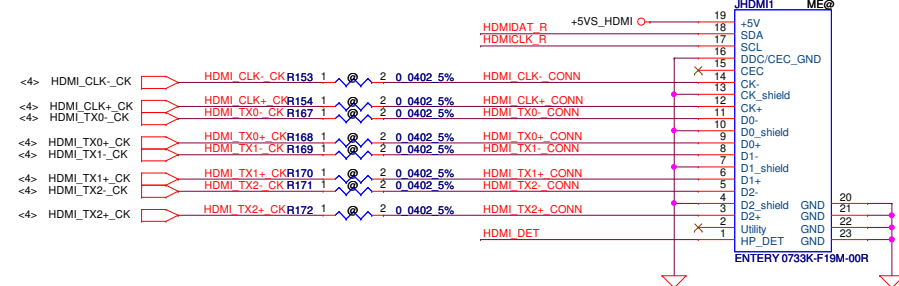
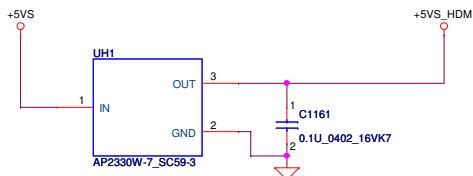
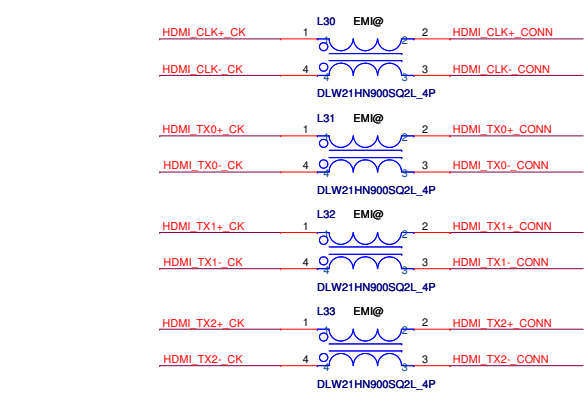
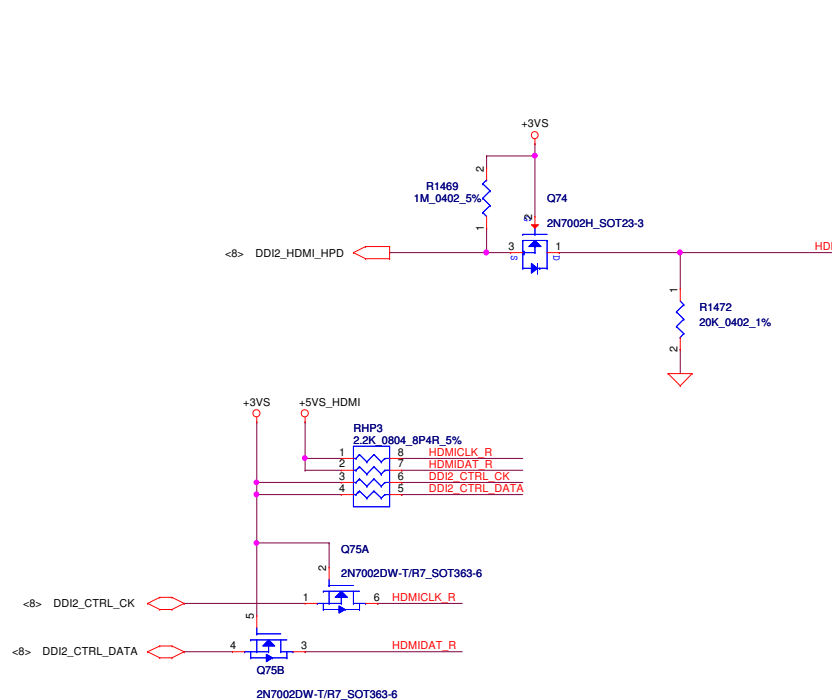
RTD2132R Internal load switch for +LCD_VCC



eDP PANEL BD. Conn.



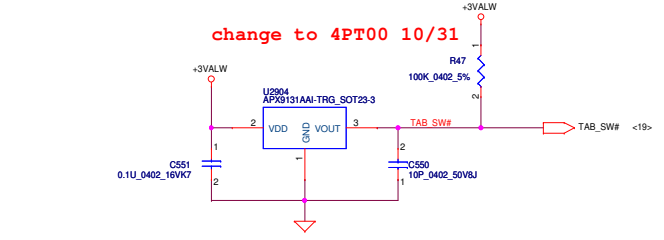
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				Customer	LA-A921PR01	1.0
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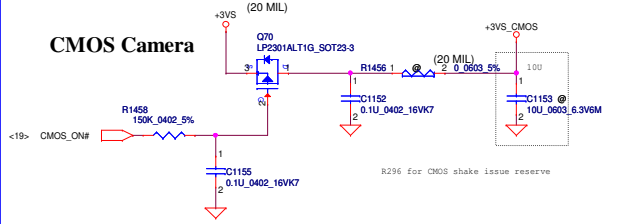
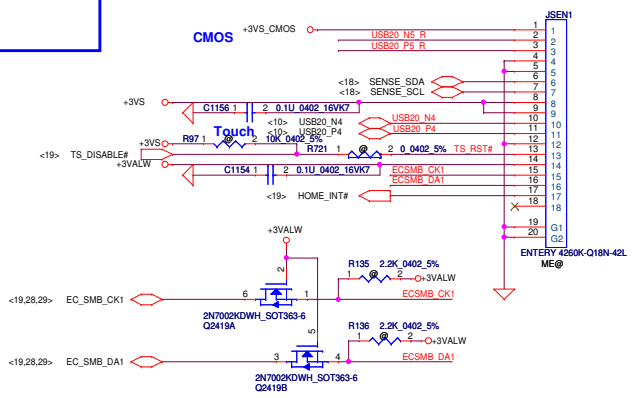
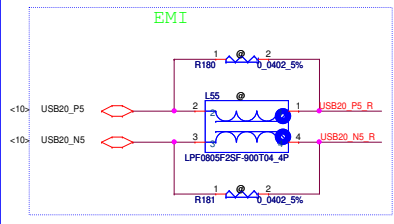
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Issued Date	2013/07/24	Deciphered Date	2015/07/24	Title
				HDMI CONN
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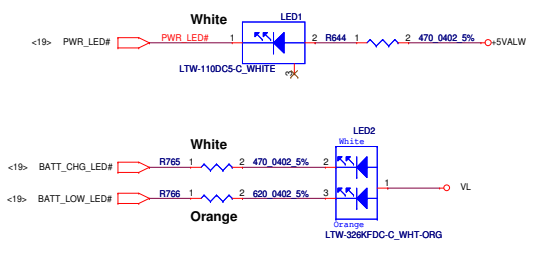
Lid SW (Tablet Mode)



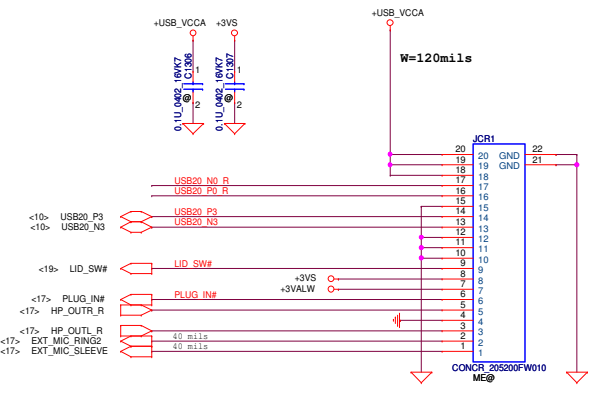
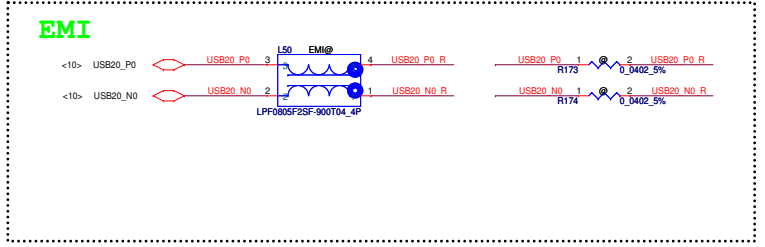
Touch & CMOS Conn



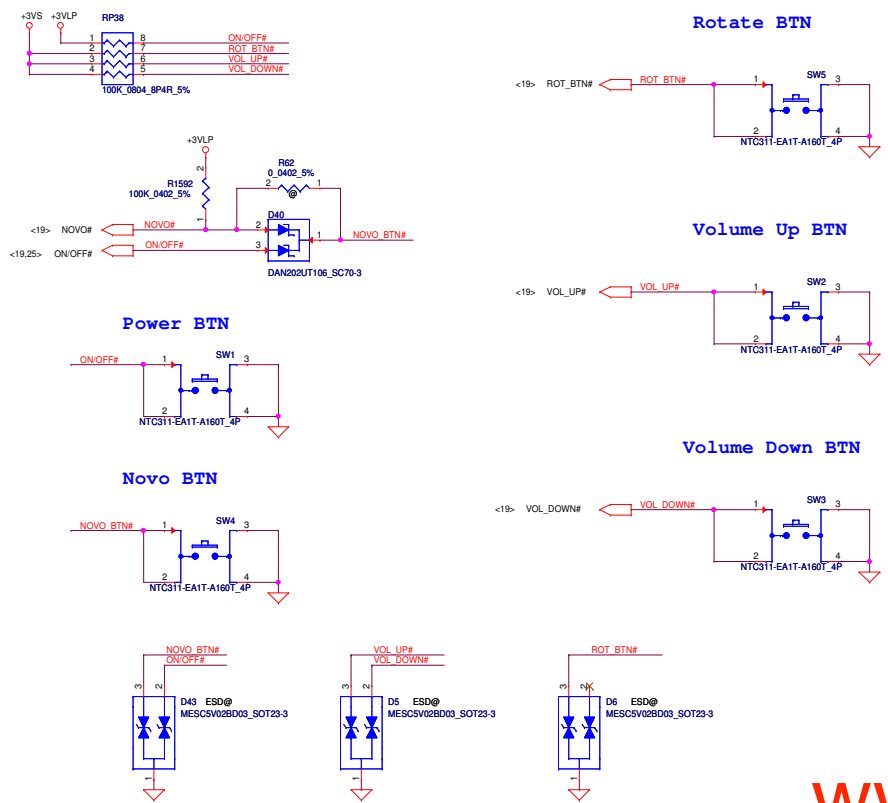
LED



I/O Board

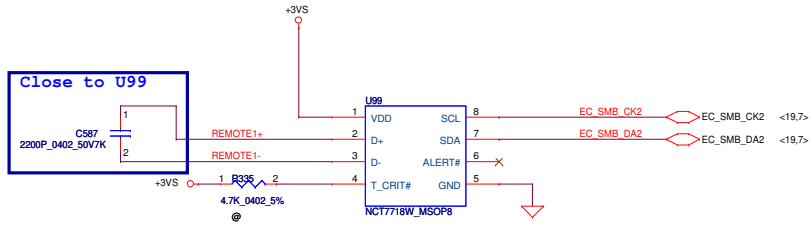


BUTTON

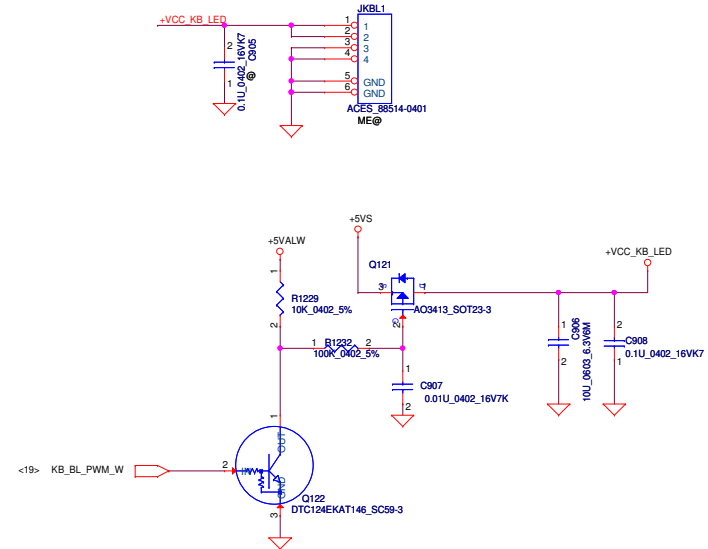


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Issued Date	2013/07/24	Deciphered Date	2015/07/24	Daughter board/LED/BTN/LID	
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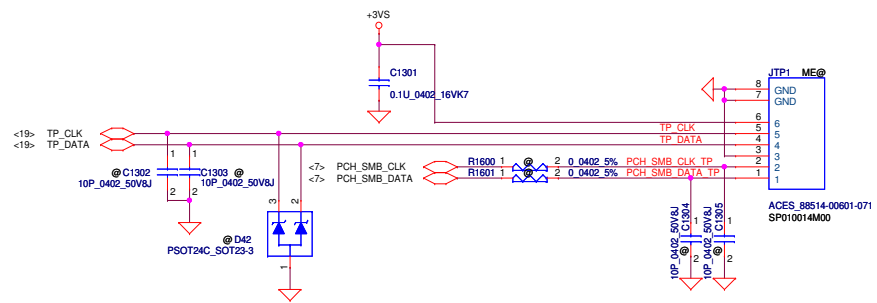
Thermal Sensor



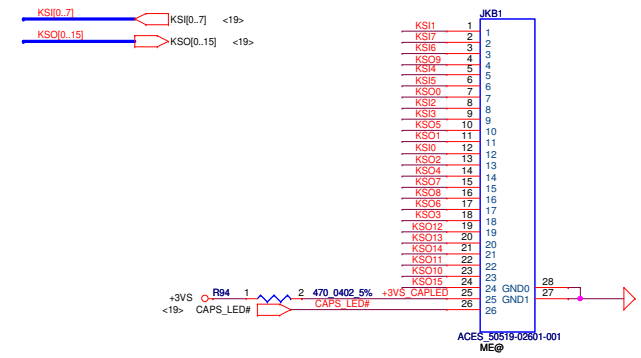
Keyboard Backlight



Click Pad

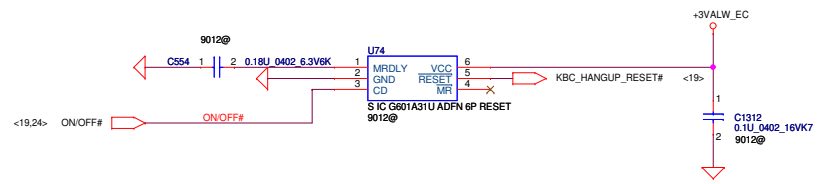


Keyboard



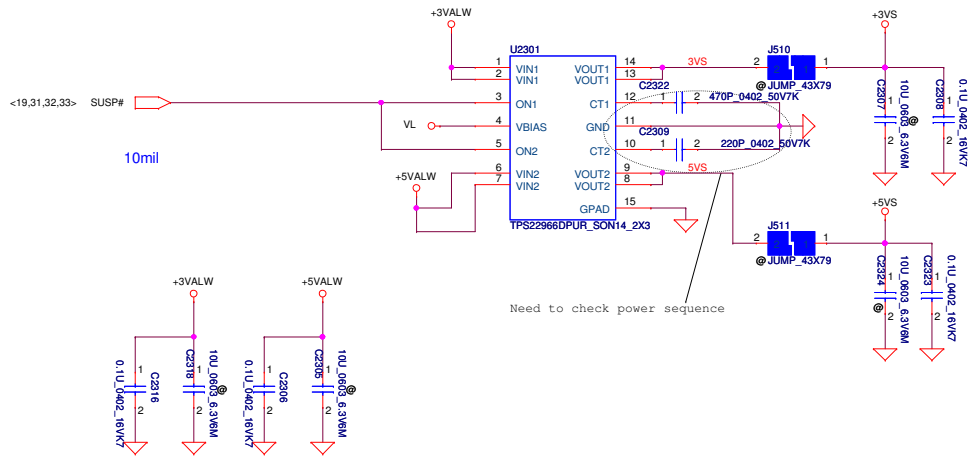
EC Reset IC

EC RESEST function

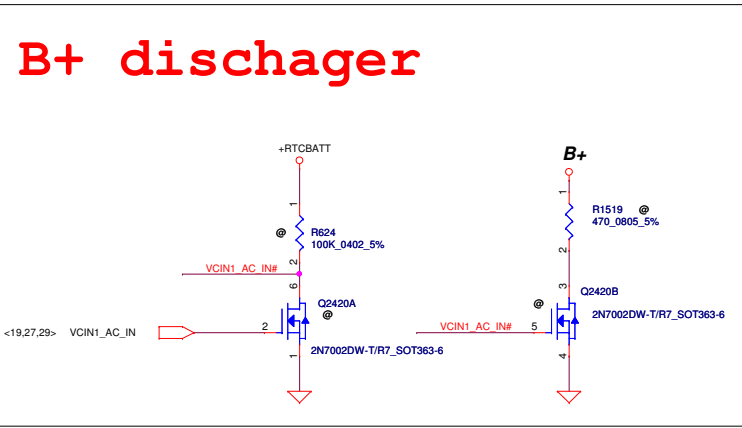
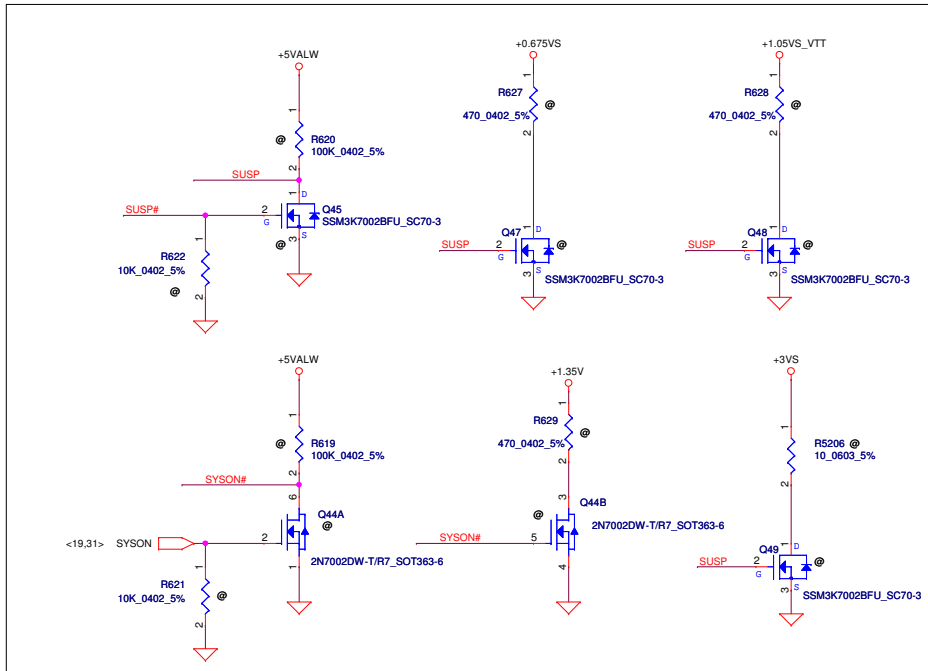
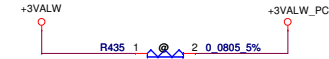


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Issued Date	2013/07/24	Deciphered Date	2015/07/24	KB/TP/Thermal Sensor
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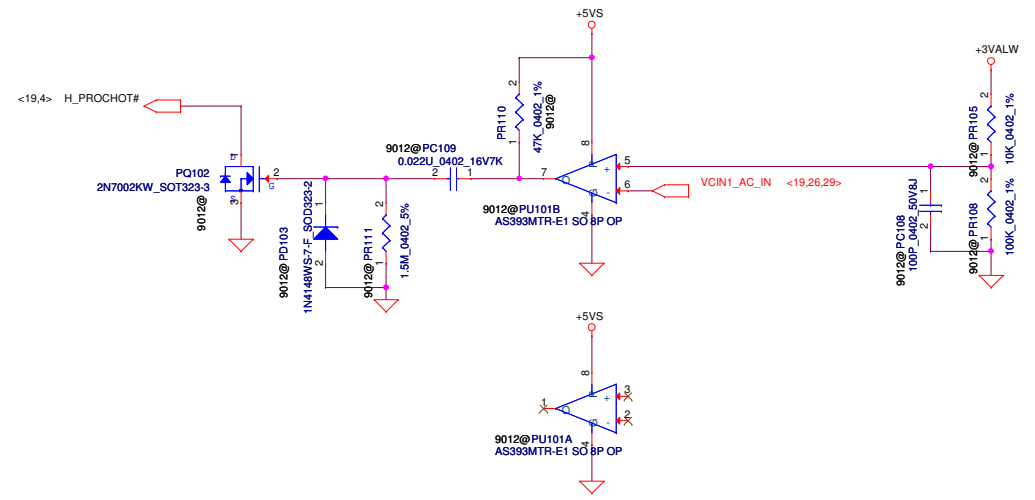
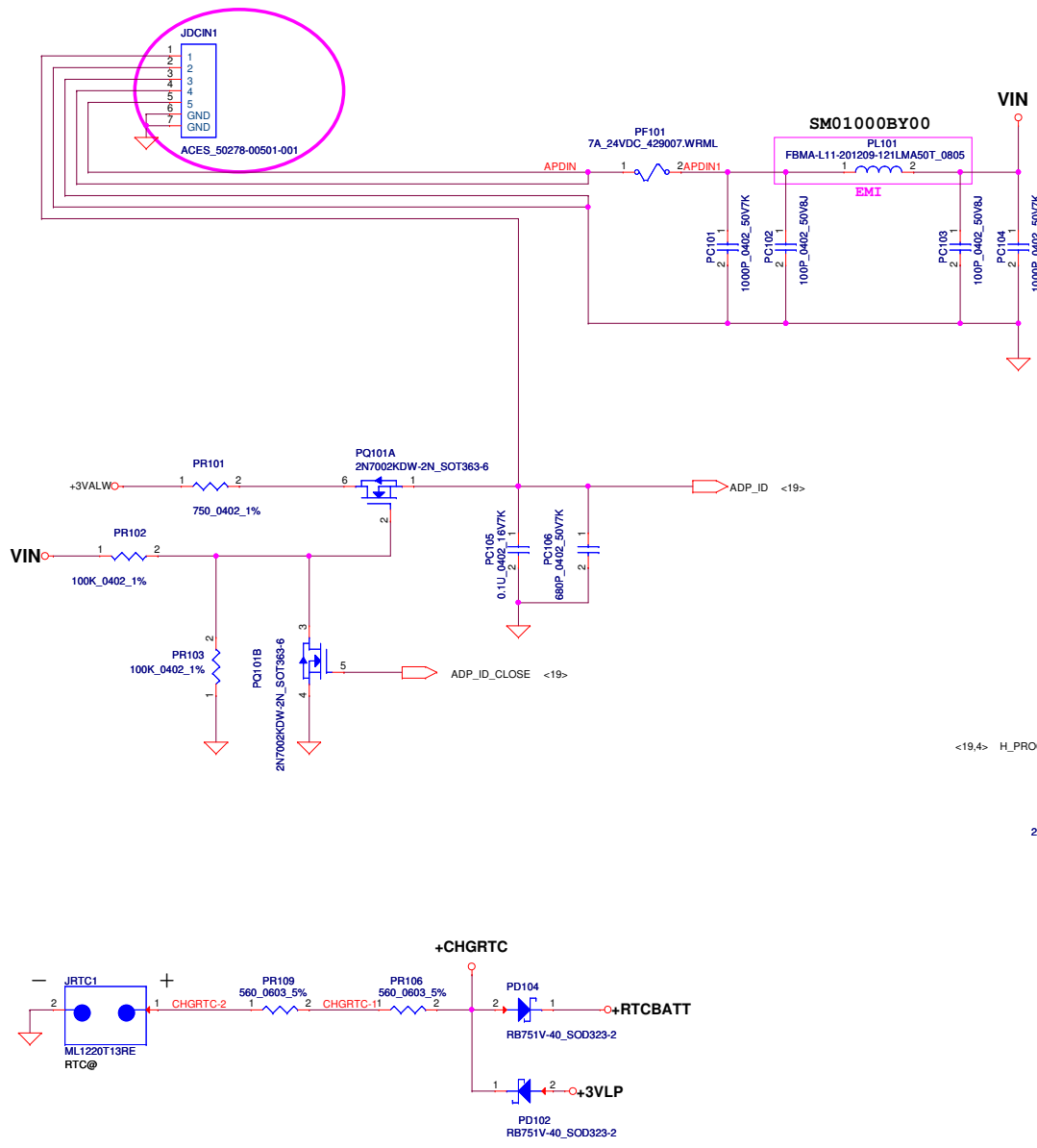
+5VALW TO +5VS
+3VALW TO +3VS



+3VALW TO +3VALW(PCH AUX Power)
+5VALW TO +5VALW(PCH AUX Power)



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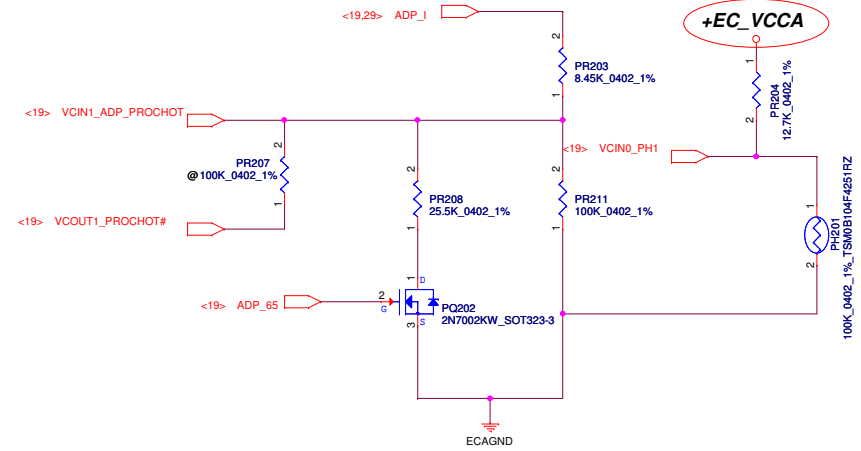
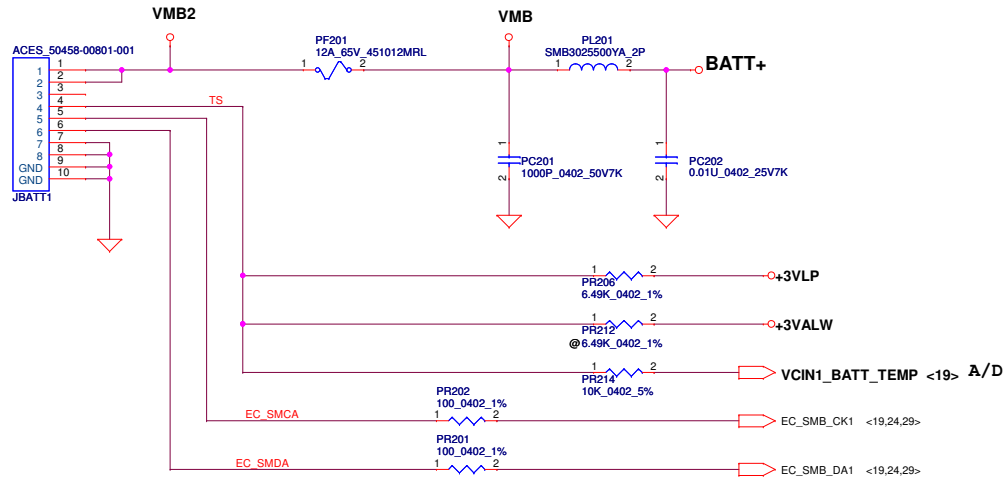


For KB9012 : Keep PU101 One-shot circuit
 For KB9022 : Remove PU101 One-shot circuit

PH201 under CPU bottom side :
 CPU thermal protection at 93 +/-3 degree C
 Recovery at 56 +/-3 degree C

65W(UMA): 85W active W recovery

20120314
 Change to +EC_VCCA from +3VLP



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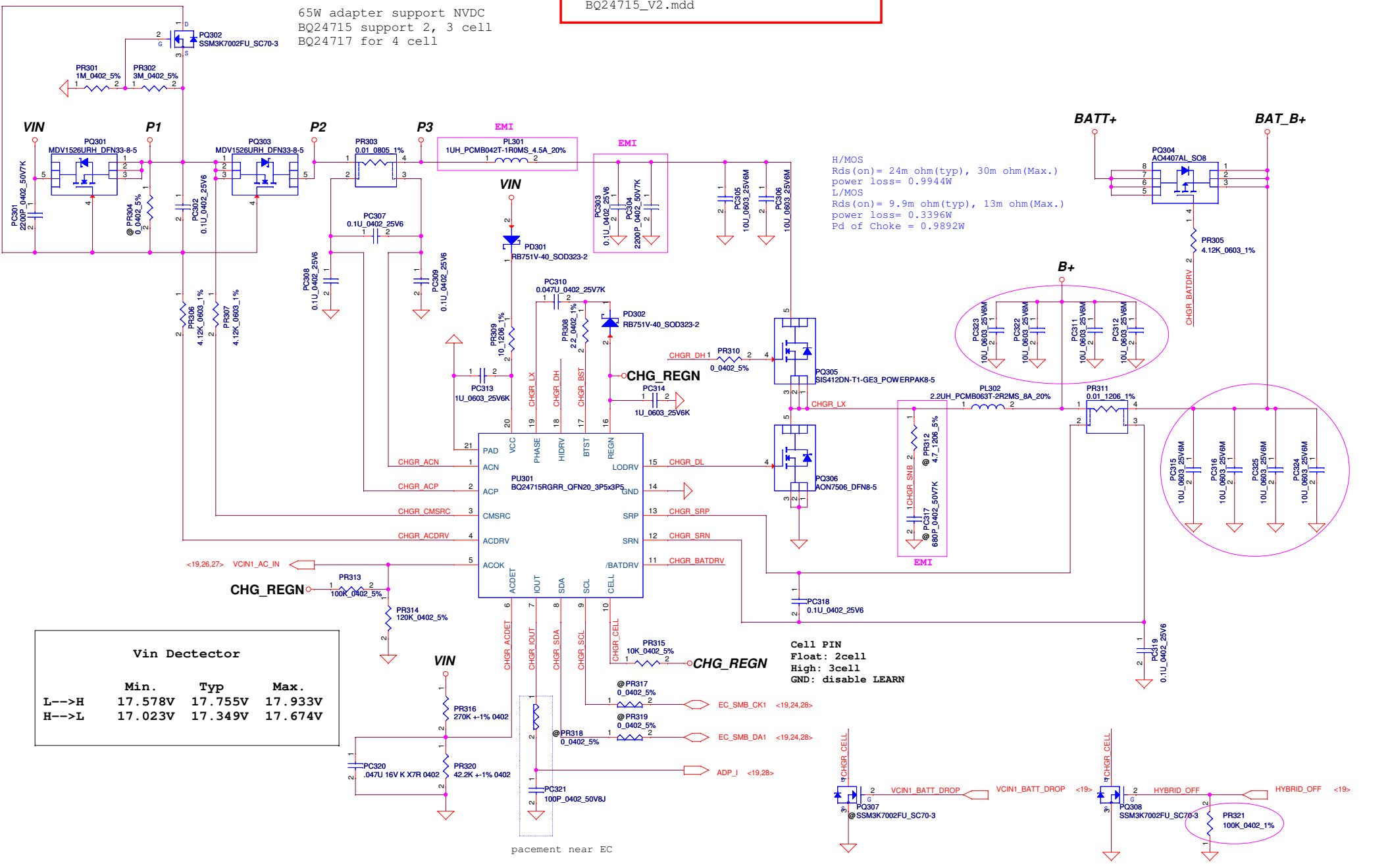
Module model information
BQ24715_V2.mdd

65W adapter support NVDC
BQ24715 support 2, 3 cell
BQ24717 for 4 cell

H/MOS
Rds(on) = 24m ohm(typ), 30m ohm(Max.)
power loss = 0.9944W
L/MOS
Rds(on) = 9.9m ohm(typ), 13m ohm(Max.)
power loss = 0.3396W
Pd of Choke = 0.9892W

Vin Detector

	Min.	Typ	Max.
L-->H	17.578V	17.755V	17.933V
H-->L	17.023V	17.349V	17.674V



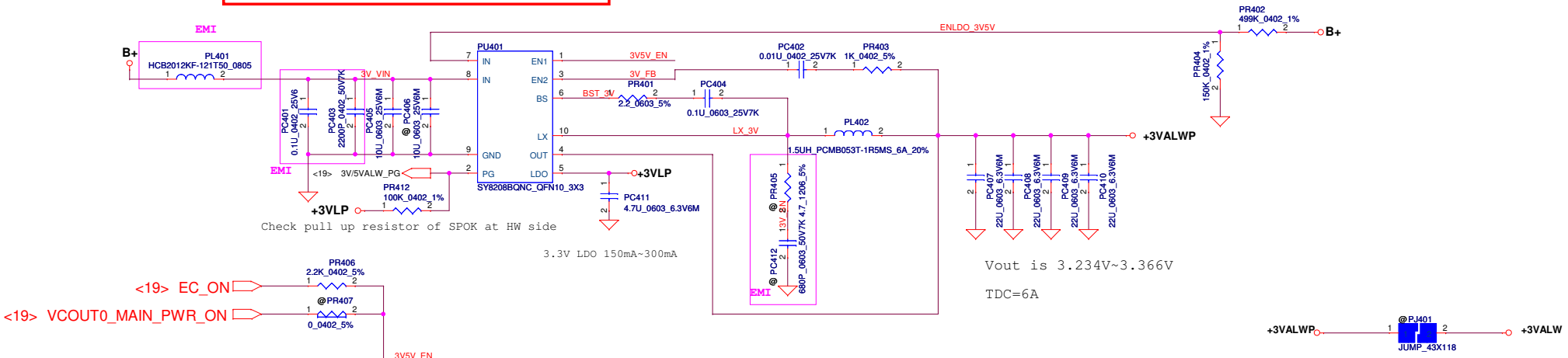
placement near EC

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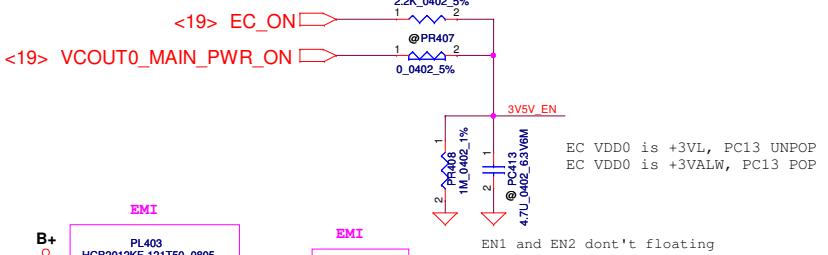
Module model information

SY8208E_V2.mdd

EN1 and EN2 don't floating

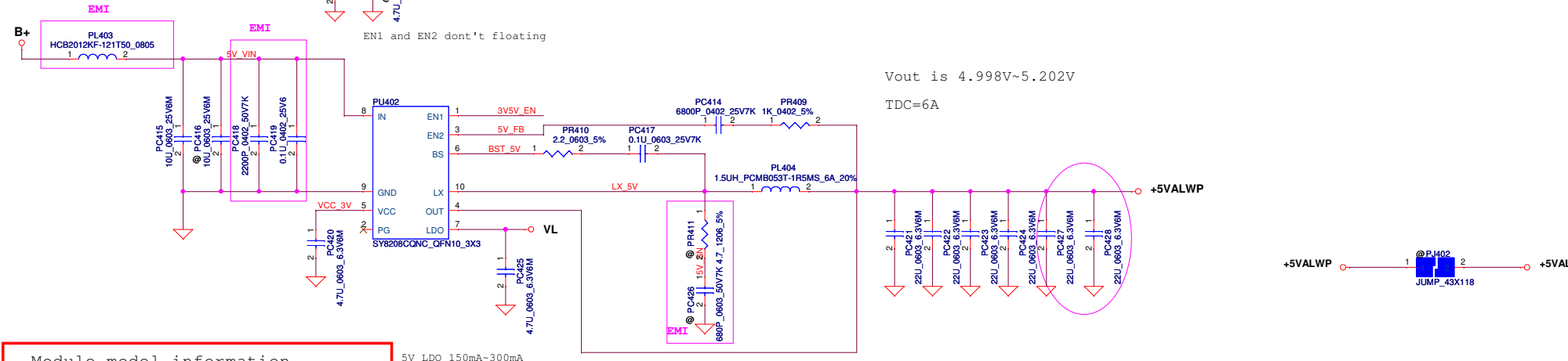


Vout is 3.234V~3.366V
TDC=6A



EC VDD0 is +3VL, PC13 UNPOP
EC VDD0 is +3VALW, PC13 POP

EN1 and EN2 don't floating



Vout is 4.998V~5.202V
TDC=6A



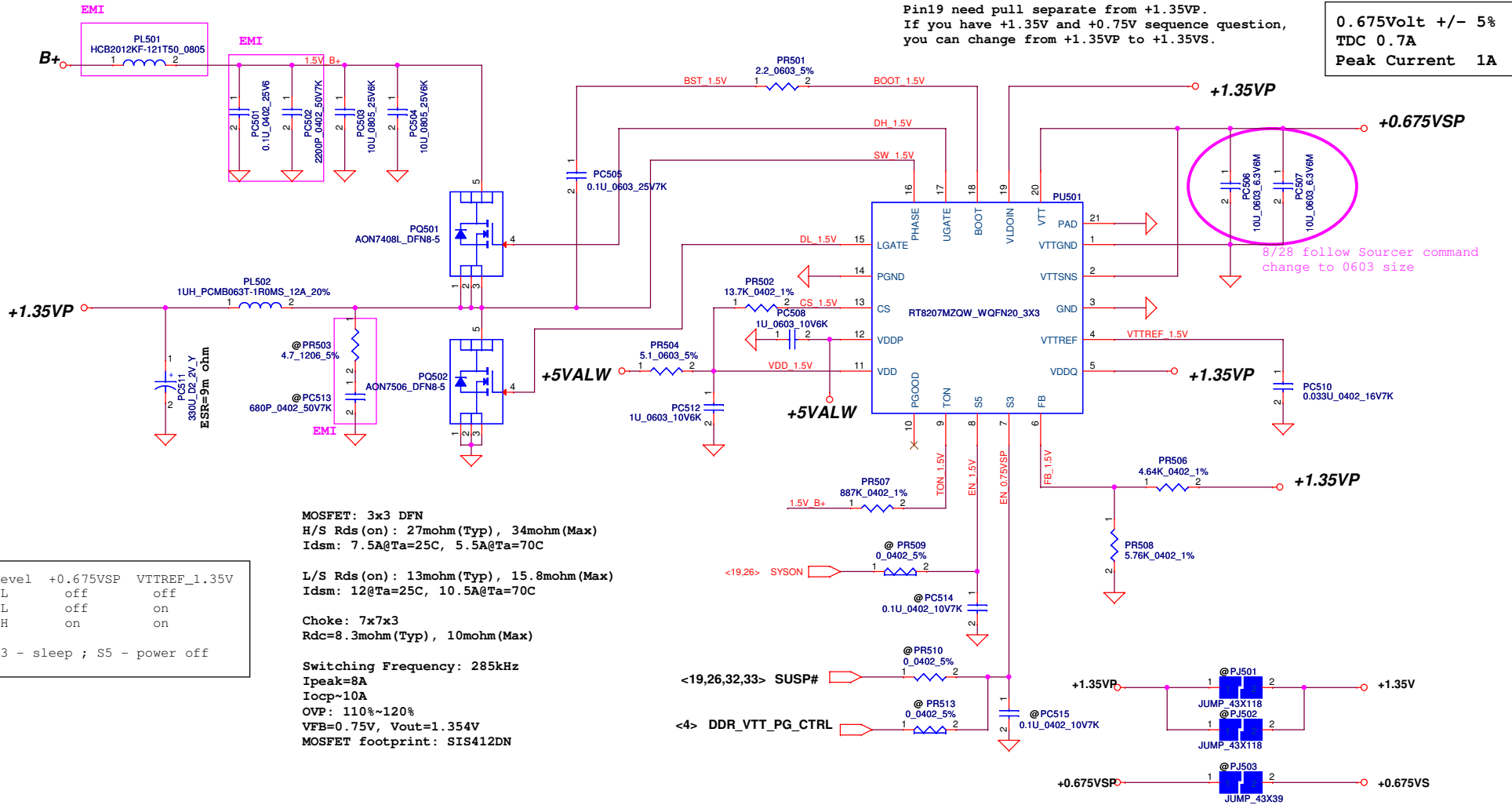
Module model information

SY8208C_V2.mdd

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				+3VALW/+5VALW
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Module model information

RT8207M_v1.mdd For Single layer
RT8207M_v2.mdd For Dual layer



Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.75V sequence question,
you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

8/28 follow Sourcer command
change to 0603 size

MOSFET: 3x3 DFN
H/S Rds (on): 27mohm (Typ), 34mohm (Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds (on): 13mohm (Typ), 15.8mohm (Max)
Idsm: 12@Ta=25C, 10.5A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm (Typ), 10mohm (Max)

Switching Frequency: 285kHz
Ipeak=8A
Iocp~10A
OVP: 110%~120%
VFB=0.75V, Vout=1.354V
MOSFET footprint: SIS412DN

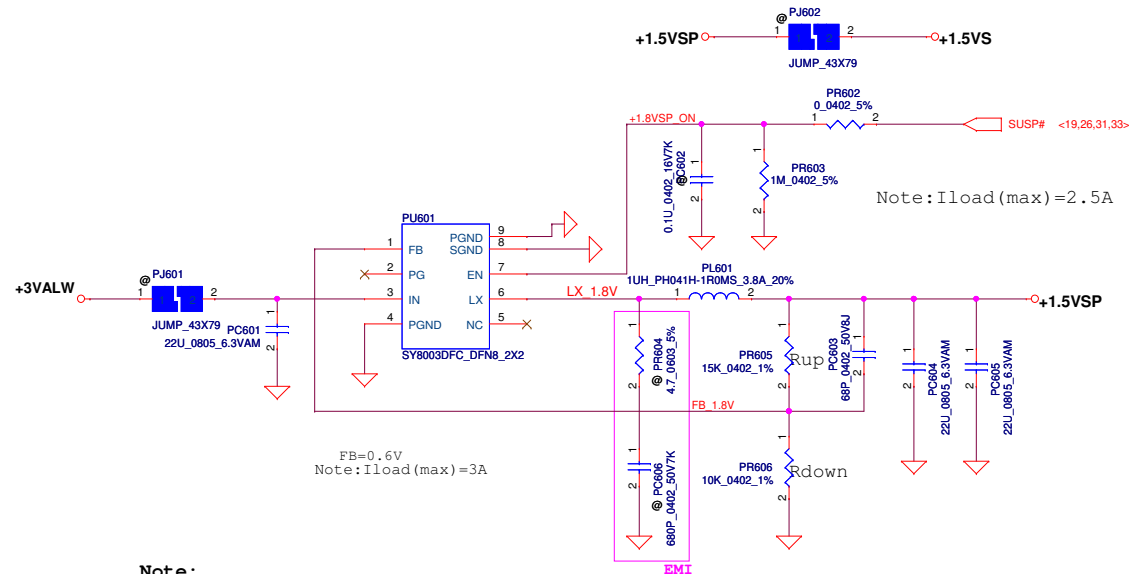
Mode	Level	+0.675VSP	VTTREF_1.35V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

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				+1.35VSP/+0.675VSP	
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Module model information

SY8003_V1.mdd



FB=0.6V
Note:Iload(max)=3A

Note:Iload(max)=2.5A

Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

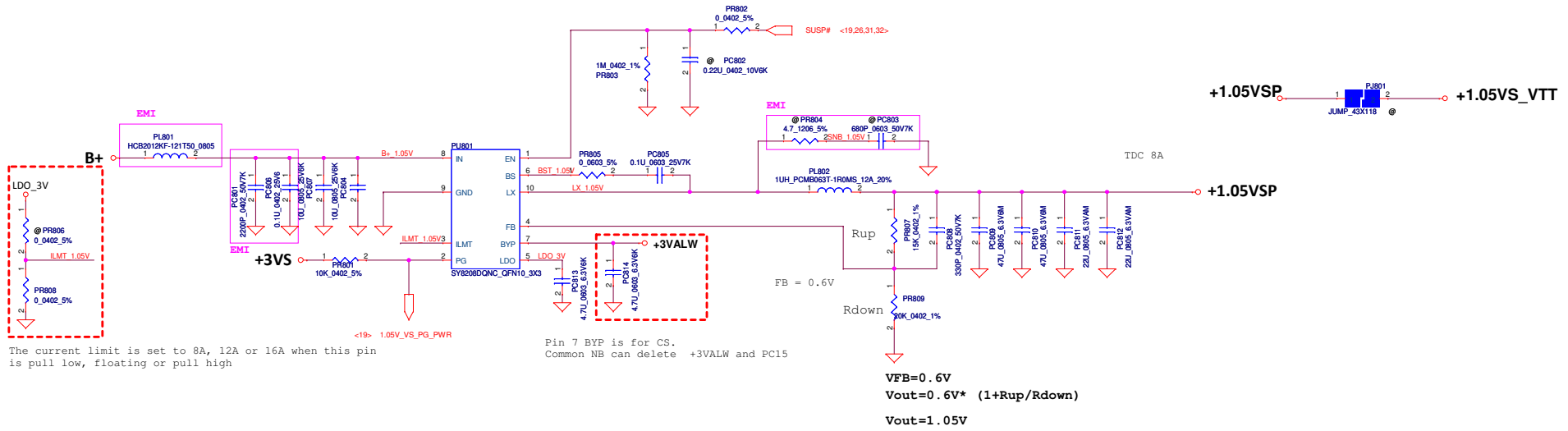
$$V_{out} = 0.6V * (1 + R_{up}/R_{down})$$

$$V_{out} = 1.5V$$

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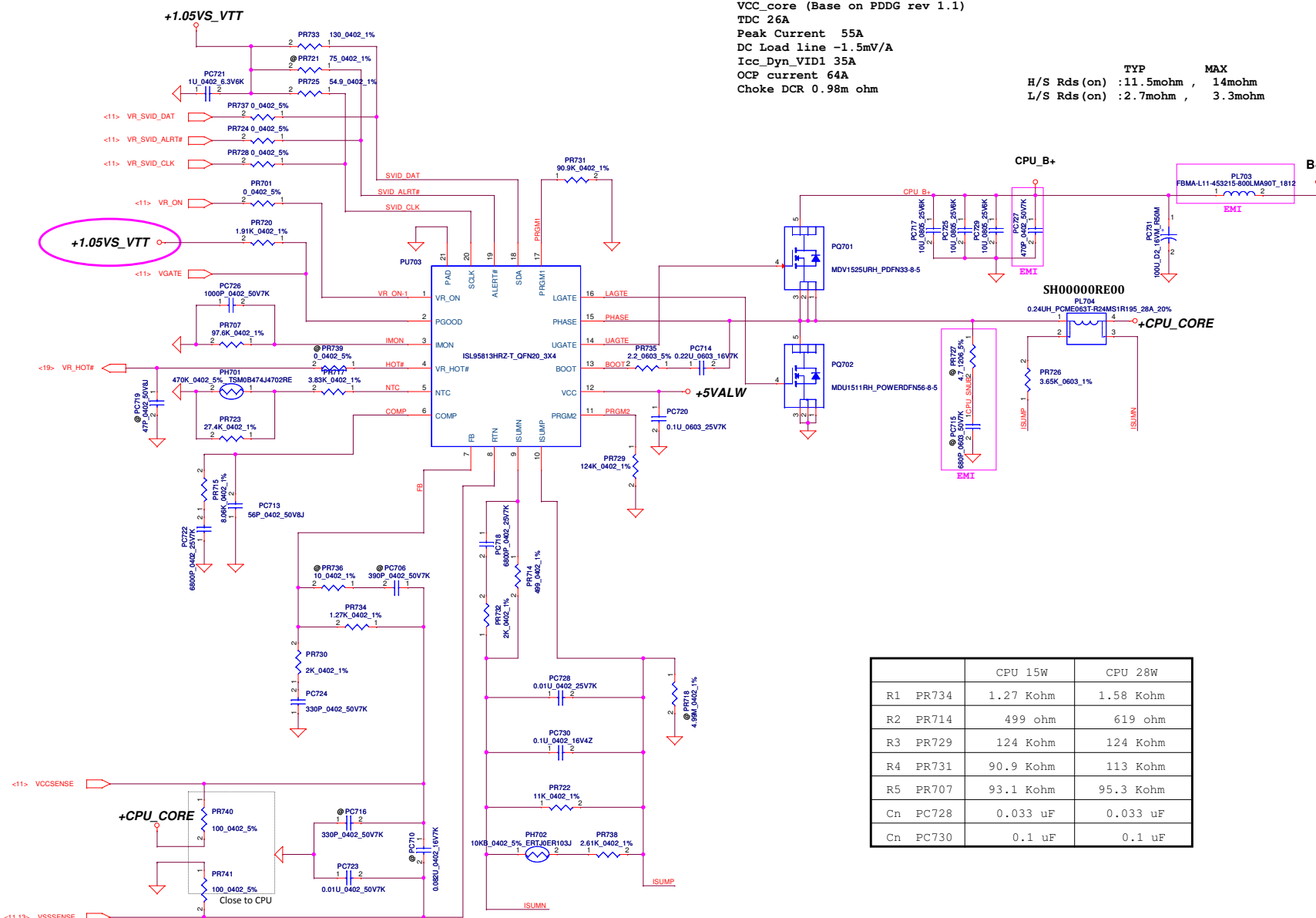
Module model information
SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



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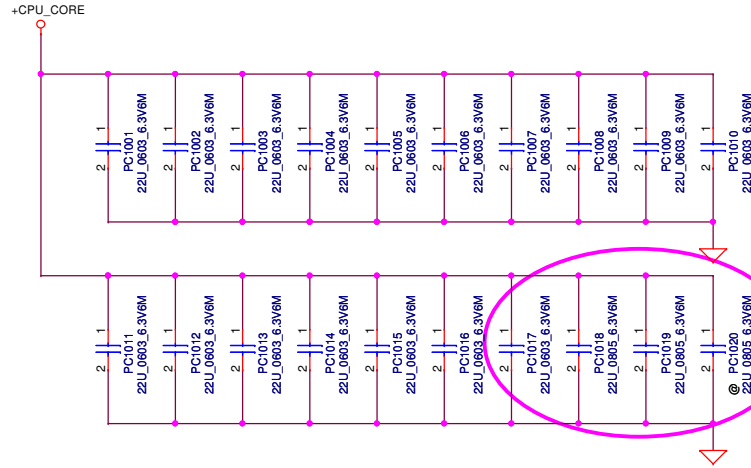
VCC_core (Base on PDDG rev 1.1)
 TDC 26A
 Peak Current 55A
 DC Load line -1.5mV/A
 Icc_Dyn_VID1 35A
 OCP current 64A
 Choke DCR 0.98m ohm

TYP MAX
 H/S Rds (on) :11.5mohm , 14mohm
 L/S Rds (on) :2.7mohm , 3.3mohm

	CPU 15W	CPU 28W
R1 PR734	1.27 Kohm	1.58 Kohm
R2 PR714	499 ohm	619 ohm
R3 PR729	124 Kohm	124 Kohm
R4 PR731	90.9 Kohm	113 Kohm
R5 PR707	93.1 Kohm	95.3 Kohm
Cn PC728	0.033 uF	0.033 uF
Cn PC730	0.1 uF	0.1 uF

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				CPU COREP
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CPU_CORE output cap-->36.4



30 X 22uF 0805
 2012/10/23
 check the output cap Qty!!!
 2012/10/24
 23 pcs 22uF and reserve 7 pcs
 2013/01/14
 22uF*15; reserve 22uF*5

2013/09/6 22U_0603x17 + 22U_0805x2

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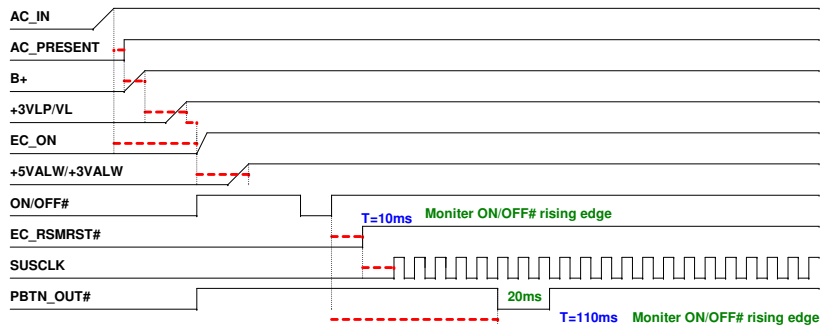
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Item	Reason for change	PG#	Modify List	Phase
1	For ME design change	21,23	JHDMI1,JUSB1 change connector type	EVT
2	For ME design change	24	SW1,SW2,SW3,SW4,SW5 change type	EVT
3	For ME design change	24,25	JCR1,JKB1 change connector type	EVT
4	For EC pin common design	19	EC pin 25,27,38,86,123 control pin change	EVT
5	Follow EC power plane for EC_Reset	25	Change U74 power plan	EVT
6	For DVT phase MB ID	19	R1564 change from 43K to 27K	EVT
7	For BDW HDMI request	23	RP1,RP2 change value from 680ohm to 470ohm	EVT
8	For Audio vender recommend	17	1. Un-mount RA19,RA22 2. Mount RA1551,RA1563 3. Add CA1,CA2	EVT
9	For EMI request	17	R55 change to Bead	EVT
10	For Compal component policy	9,21	U52,U4 change type	EVT
11	For touch vennder recommend	24	1. JSEN1 pin 13 add 10K pull high 2. JSEN1 pin 14 change to +3VALW	EVT
12	For SPEC change	6,20	Delete SSD PCIE interface component	EVT
13				
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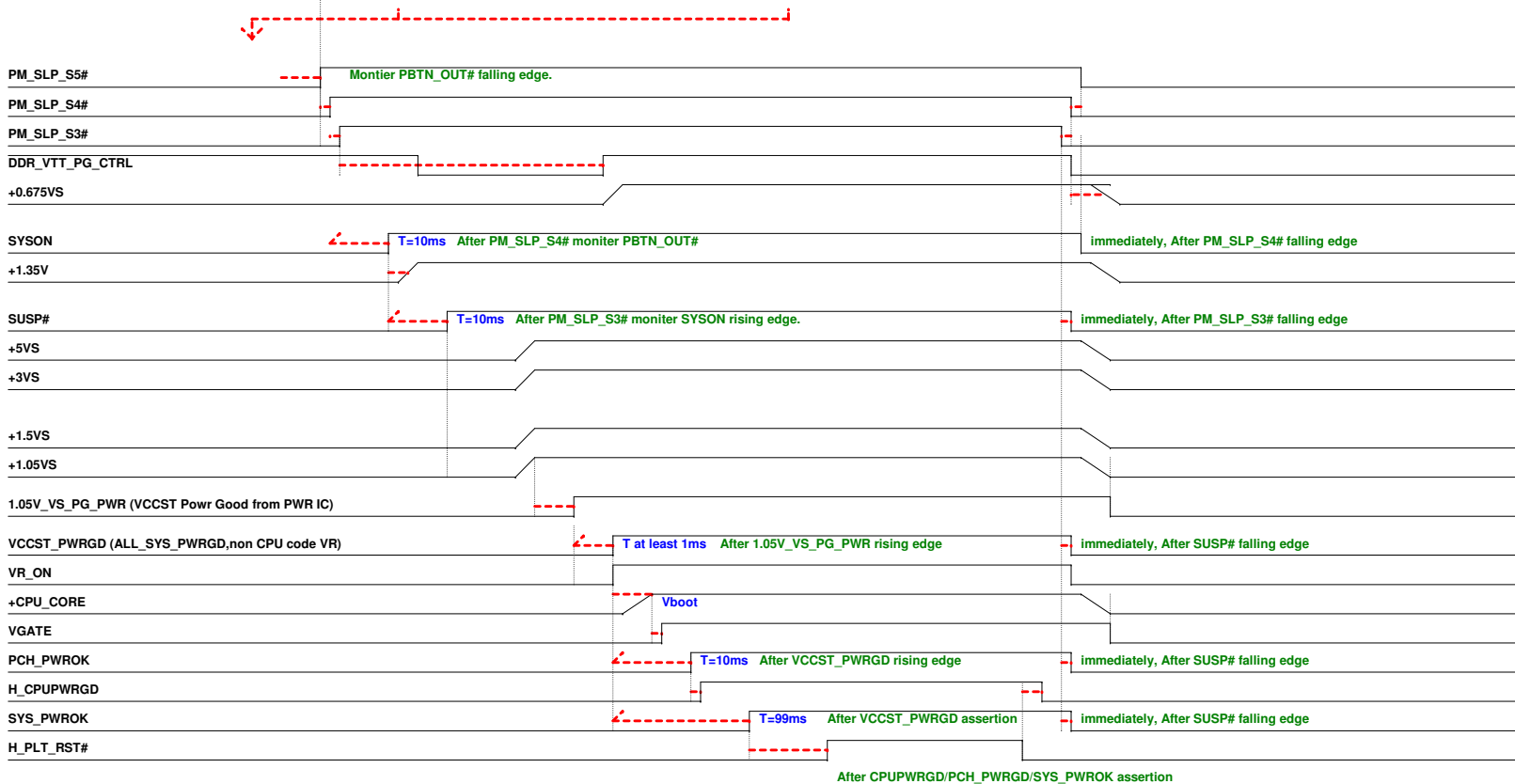
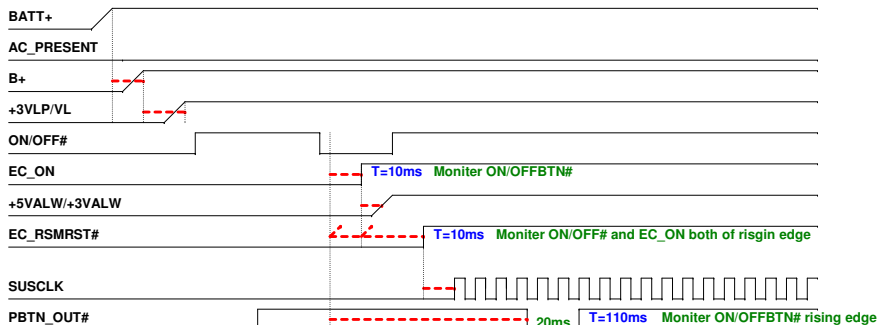
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