

Compal Confidential

Schematics Document

Arrandale/Clarksville

with Intel IBEX PEAK-M core logic

NIWBA

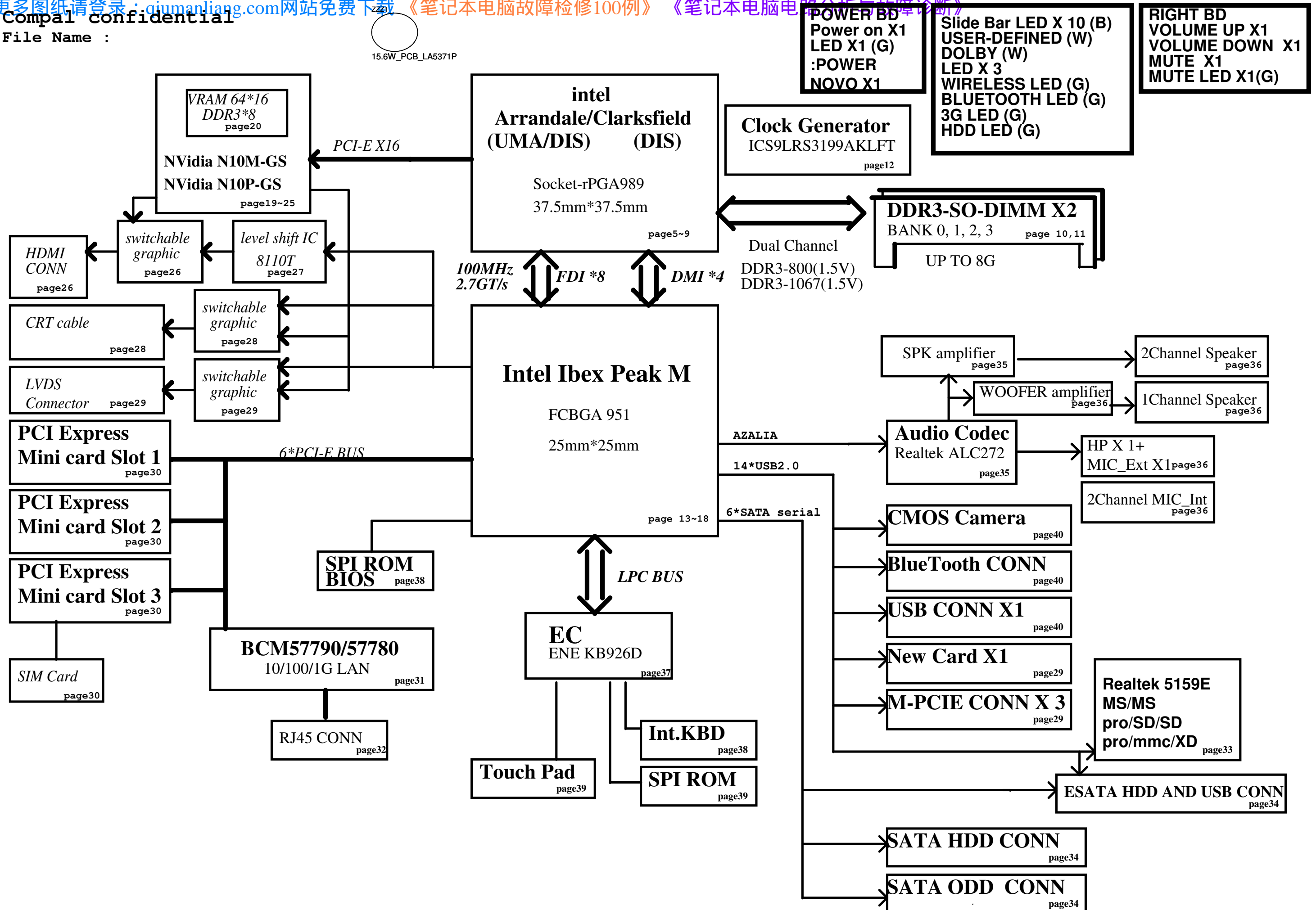
REV: 0.1

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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title	Cover Sheet
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File Name :



15.6W_PCB_LA5371P



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power plane	+B	+5VALW +3VALW	+1.5V	+5VS
				+3VS
State				+1.5VS
				+VCCP
				+CPU_CORE
				+VGA_CORE
				+1.8VS
				+0.75VS
				+1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	RAM M2	BATT	KE926	SODIMM	CLK CHIP	WLAN WWAN	N10x Thermal Sensor	N10x	Cap sensor board	NEW CARD	PCH
SMB_EC_CK1	KB926	X	V	X	X	X	X	X	X	X	X	X
SMB_EC_DA1	+3VALW		+3VALW									
SMB_EC_CK2	KB926	X	X	X	X	X	X	X	X	X	X	V
SMB_EC_DA2	+3VALW											+3VALW
SMBCLK	PCH	V	X	X	V	V	X	X	X	X	V	X
SMBDATA	+3VALW	+3VALW			+3VS	+3VS					+3VS	
SML0CLK	PCH	X	X	X	X	X	X	X	X	X	X	X
SML0DATA	+3VALW											
SML1CLK	PCH	X	X	V	X	X	X	V	X	V	X	X
SML1DATA	+3VALW			+3VALW				+3VS		+3VS		

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
DDR SO-DIMM 1	A4	10100100
CLOCK GENERATOR (EXT.)	D2	11010010

@ FUNCTION

EVT		NON-USE	
45@	(45 BOM)		
GIGA@	(GIGA LAN)	100@	(100 LAN)
NO TVSW@	(NON TV POWER SW)	TVSW@	(TV POWER SW)
ARRAY@	(ARRAY MIC)	MONO@	(MONO MIC)
S512@	FOR X76 BOM		
H512@	FOR X76 BOM		
S1024@	FOR X76 BOM		
H1024@	FOR X76 BOM		
X76@	(X76 BOM)		
M1@	(DDR M1 MODE)		
3G@	(3G MODE)		
10M@	FOR 10M CHIP		
10P@	FOR 10P CHIP		
UMA@	FOR Auberndale		
DIS@	FOR Auberndale/Clarksville		
VGA@	FOR NVIDIA PART		

PORT	DEVICE
1	NEW CARD
2	WLAN
3	LAN
4	3G
5	
6	TV TUNNER
7	
8	

PORT	DEVICE
0	LEFT SIDE
1	RIGHT SIDE
2	CMOS
3	
4	RIGHT SIDE
5	CARD READER
6	
7	
8	WIRELESS
9	TV TUNNER
10	NEW CARD
11	BT
12	
13	3G

VGA and DDR3 Voltage Rails (N10x GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	Hot plug detect for IFP link C
GPIO2	OUT	H	Panel Back-Light brightness(PWM capable)
GPIO3	OUT	H	Panel Power Enable
GPIO4	OUT	H	Panel Back-Light On/Off (PWM)
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	GPU VID2
GPIO8	I/O	L	Thermal Catastrophic Overtemp
GPIO9	OUT	L	Thermal Alert
GPIO10	OUT		Memory VREF switch
GPIO11	I/O	L	SLI raster sync
GPIO12	IN	-	AC power detect pin
GPIO13	OUT	-	MEM_VID or Power supply control
GPIO14	OUT	-	Power supply control
GPIO15	IN	-	Hot plug detect for IFP Link E
GPIO16	OUT	-	Programmable Fan Control
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	Hot plug detect for IFP Link D
GPIO20	IN	-	
GPIO21	IN	-	Hot plug detect for IFP link F
GPIO22	IN	-	SLI swap ready signal
GPIO23	I/O		

GPIO6	GPIO5	N10M-GS	N10P-GS
GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	1	0.9V	0, 10

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

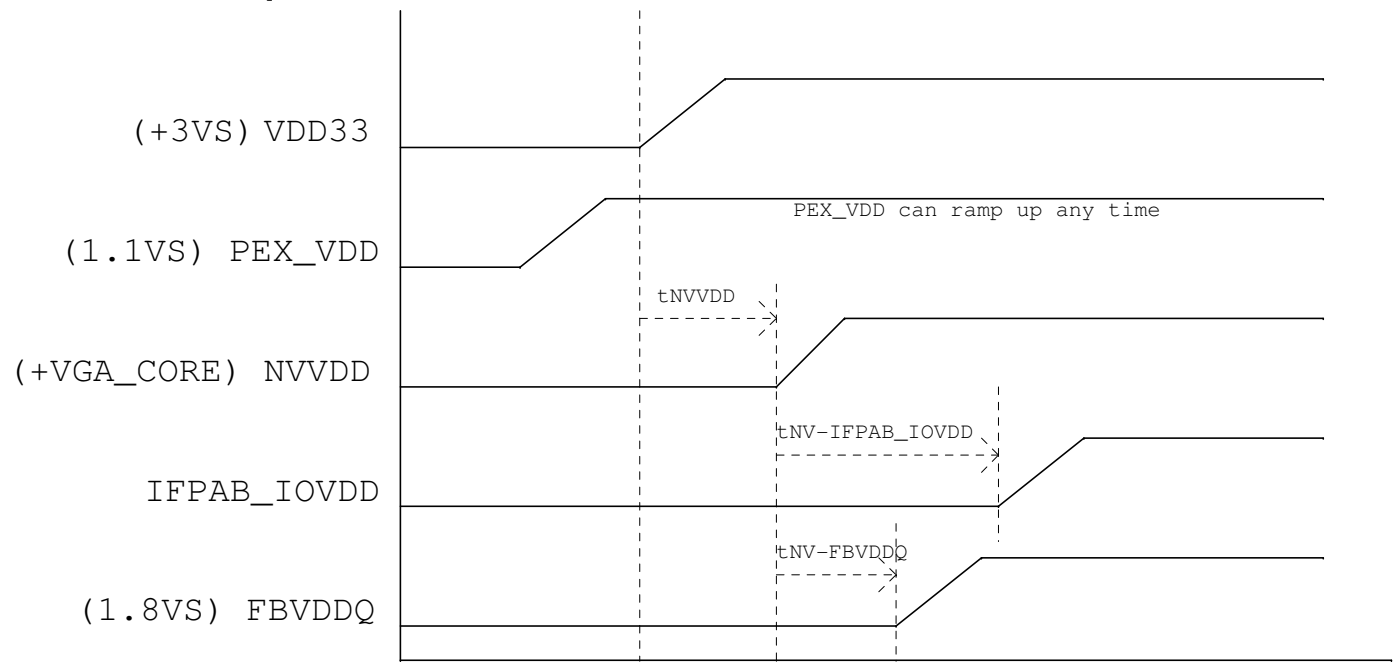
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK (MHz)	NVVDD			FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10P-GS 128bit 1024MB DDR3	21.07	6.67	TBD	TBD	18.25	17.34	2.06	3.09	4.09	6.14	850	0.89	75	0.14	63	0.07	55	0.18
N10P-GE 128bit 1024MB DDR3	20.97	6.73	TBD	TBD	19.17	17.25	2.03	3.05	4.09	6.14	840	0.88	75	0.14	63	0.07	55	0.18
N10P-LP 128bit 1024MB DDR3	15.48	6.44	TBD	TBD	13.95	11.86	1.90	2.85	3.99	5.99	810	0.85	75	0.14	63	0.07	55	0.18

Performance Mode P0 TDP at Tj = 102 C* (DDR3)

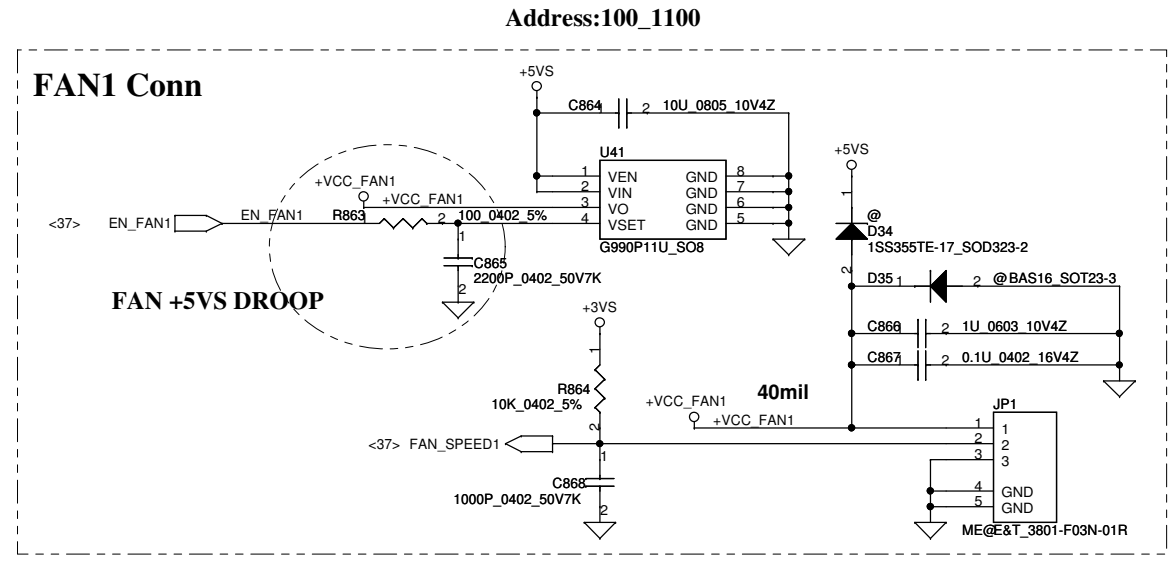
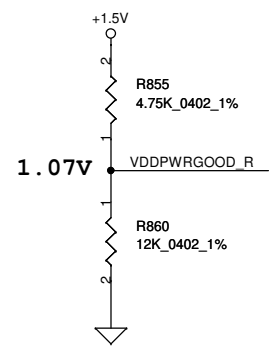
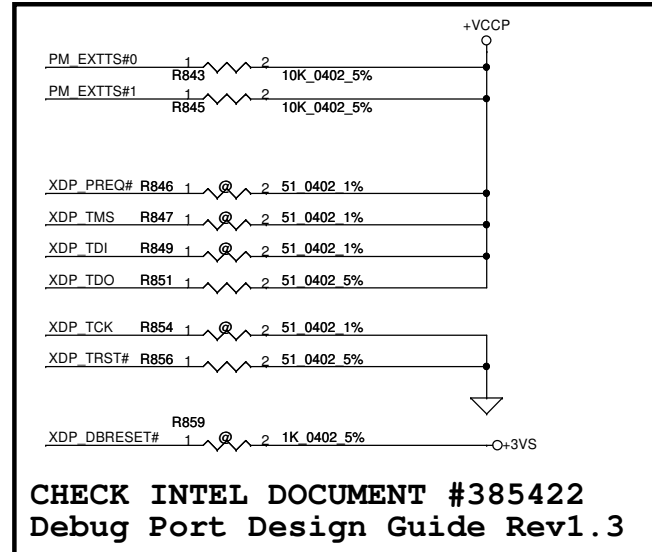
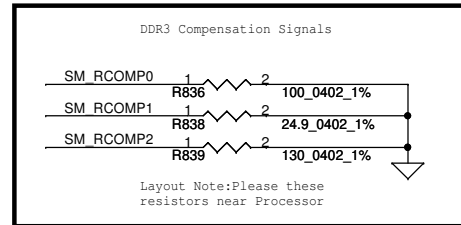
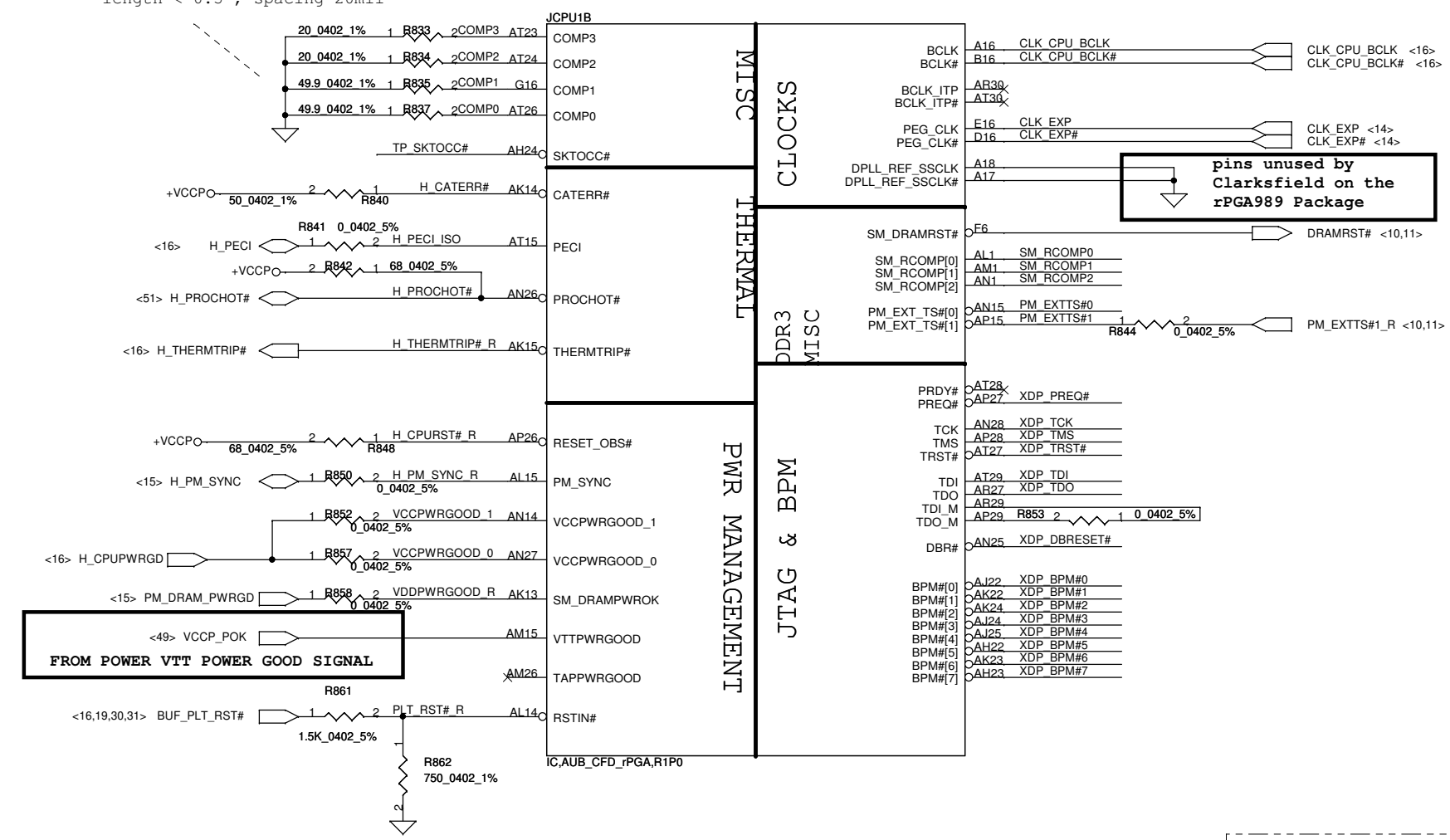
Products	GPU (4)	Mem (1,5)	NVCLK /MCLK (MHz)	NVVDD			FBVDD (1.5V)		FBVDDQ (GPU+Mem) (1.5V)		PCI Express (1.05V) (6)		I/O and PLLVDD (1.8V)		I/O and PLLVDD (1.05V)		Other (3.3V)	
	(W)	(W)	(MHz)	(V)	(A)	(W)	(A)	(W)	(A)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)	(mA)	(W)
N10M-GE 64bit 512MB DDR3	13.36	2.93	TBD	TBD	11.89	10.70	0.66	0.99	2.16	3.24	792	0.83	75	0.14	63	0.07	100	0.33
N10M-GS 64bit 512MB DDR3	14.29	3.10	TBD	TBD	11.53	11.53	0.70	1.05	2.28	3.42	817	0.86	75	0.14	63	0.07	100	0.33
N10M-LP 64bit 512MB DDR3	8.28	2.91	TBD	TBD	6.60	5.61	0.62	0.93	2.20	3.3	782	0.82	75	0.14	63	0.07	100	0.33

Power Sequence

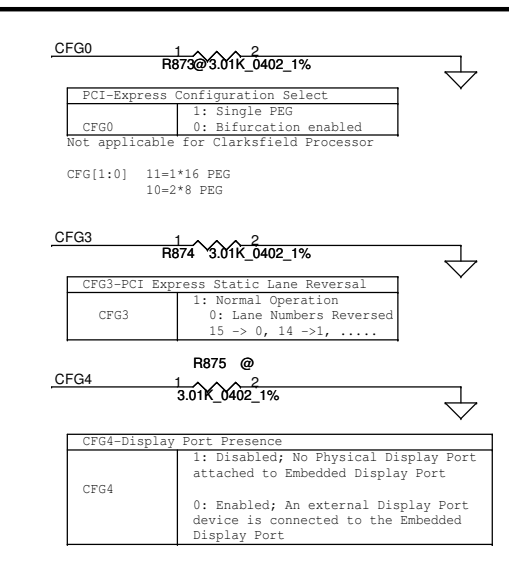
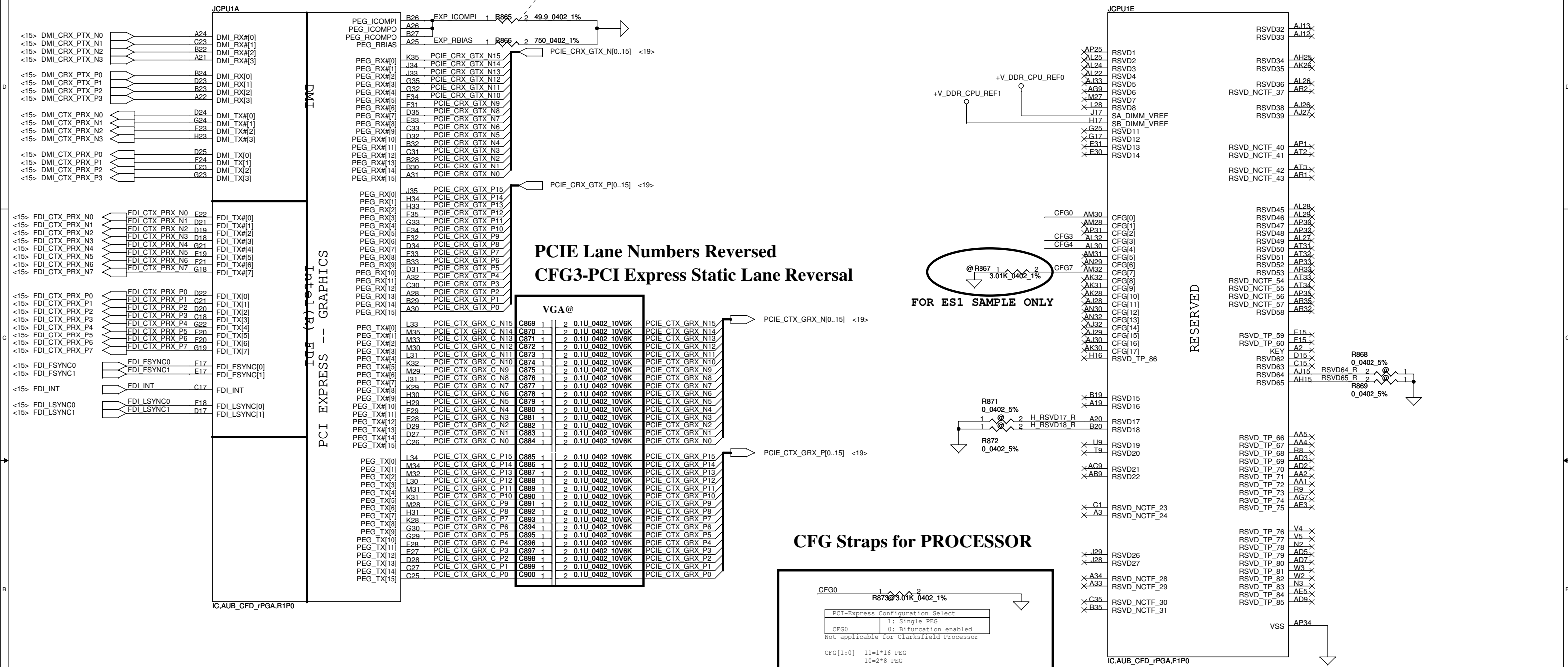
The ramp time for any rail must be more than 40us



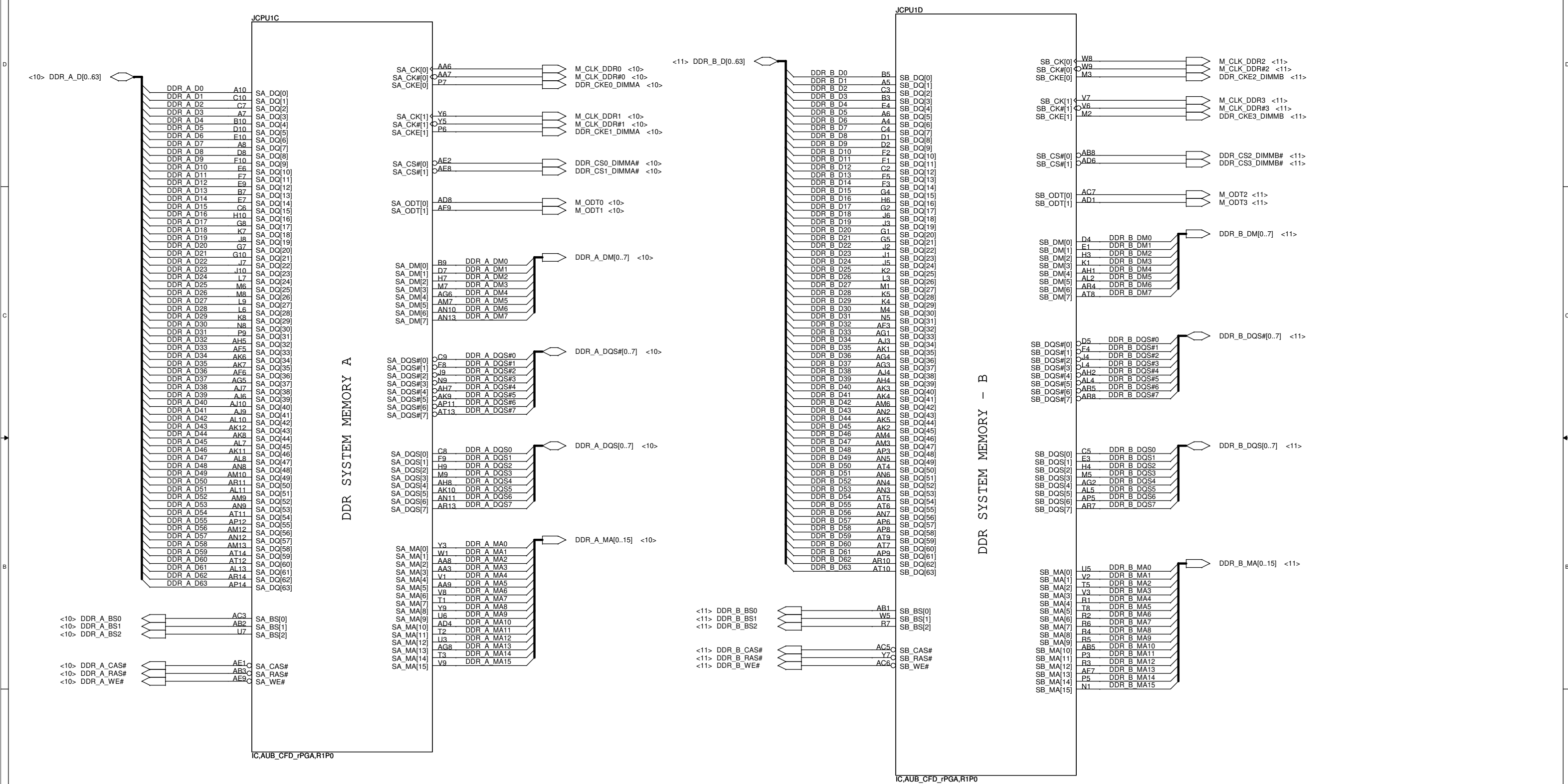
Layout rule: 10mil width trace
length < 0.5", spacing 20mil



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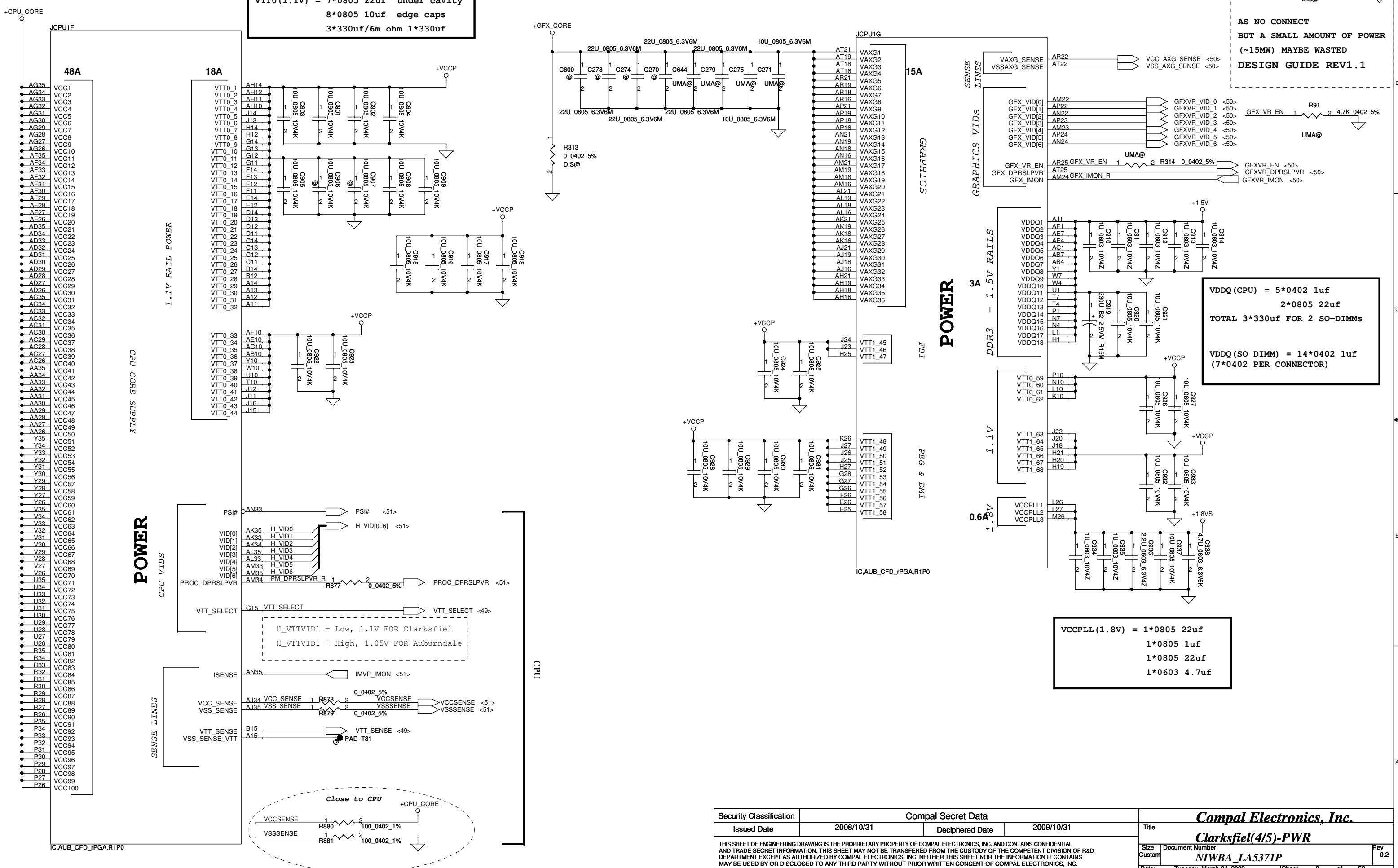
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VTT0(1.1V) = 7*0805 22uf under cavity
 8*0805 10uf edge caps
 3*330uf/6m ohm 1*330uf

AS NO CONNECT
 BUT A SMALL AMOUNT OF POWER
 (~15MW) MAYBE WASTED
 DESIGN GUIDE REV1.1

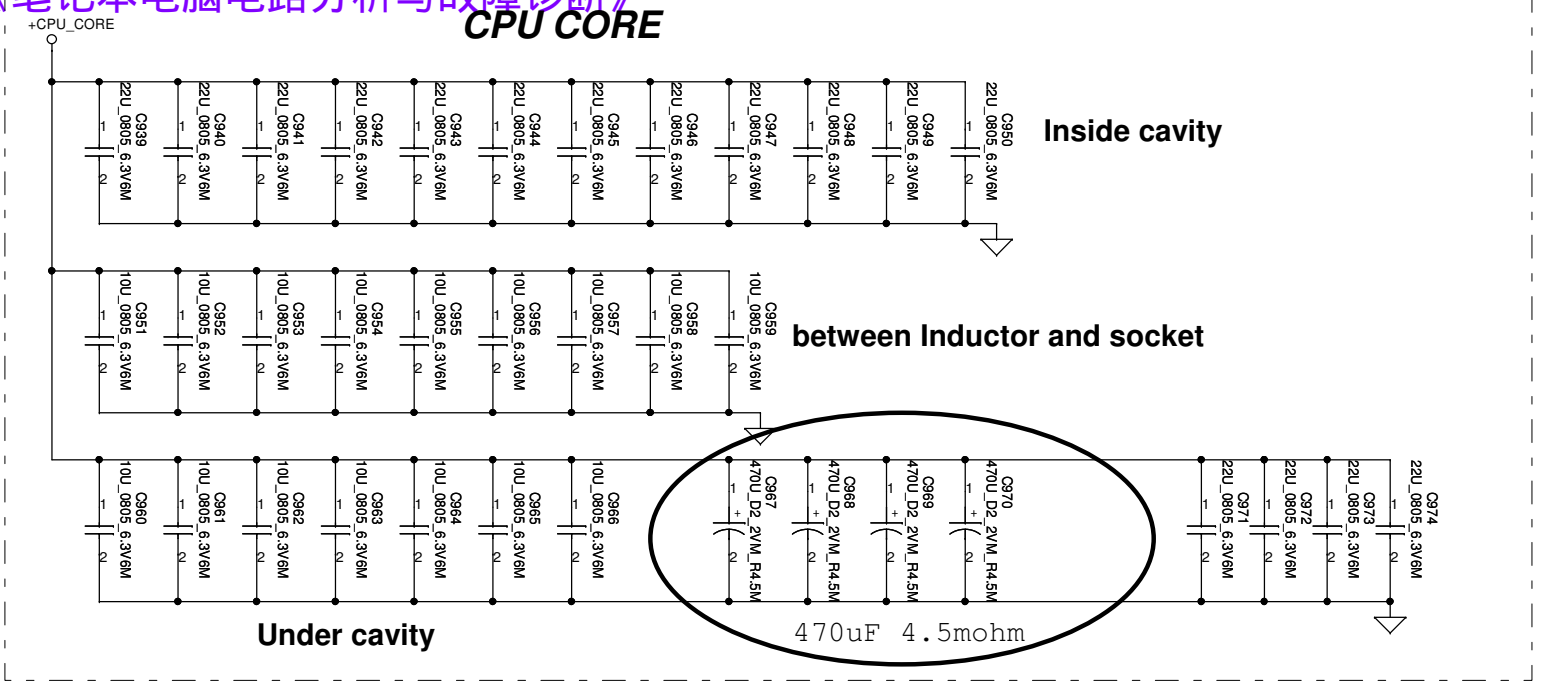
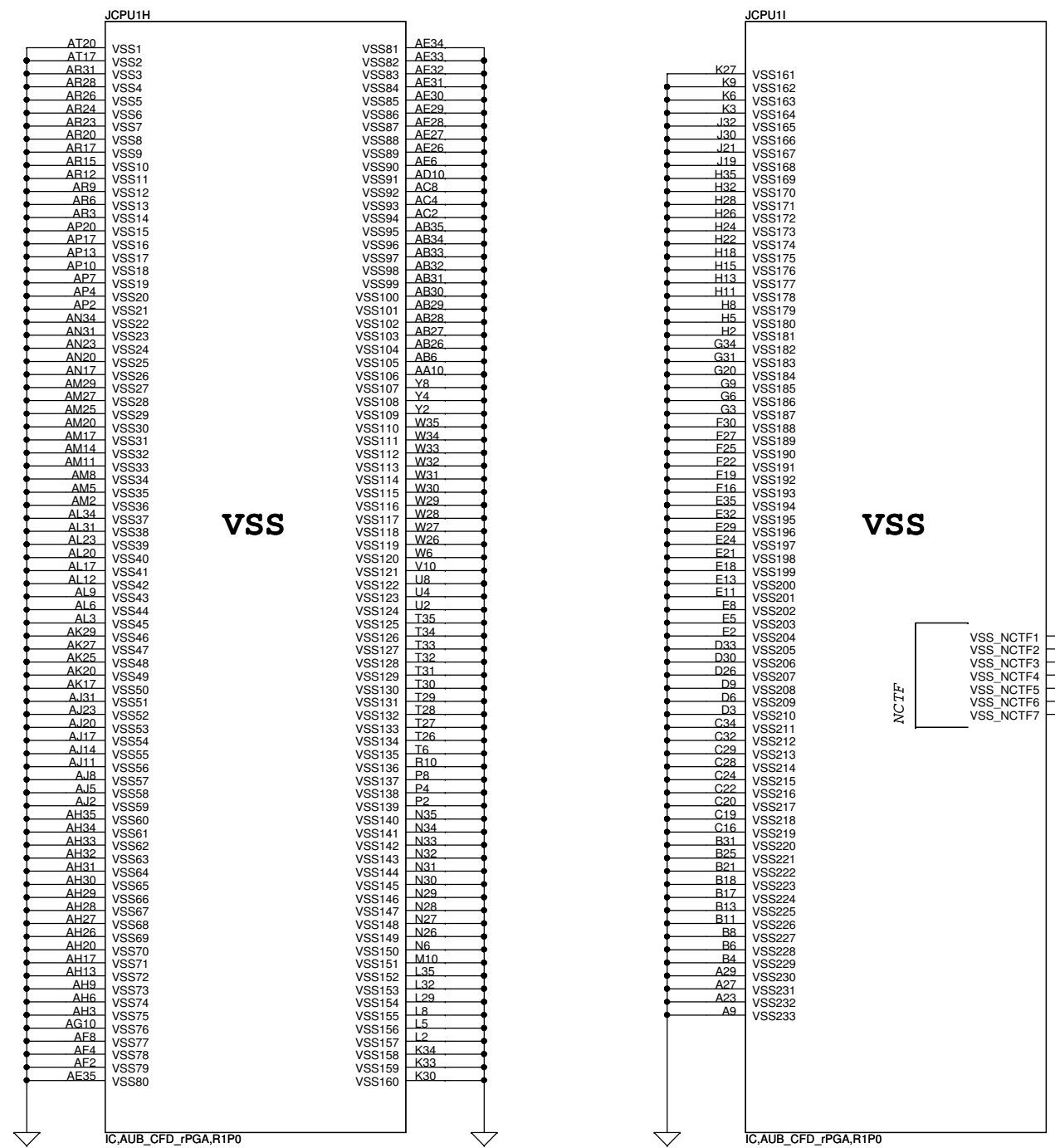


VDDQ(CPU) = 5*0402 1uf
 2*0805 22uf
 TOTAL 3*330uf FOR 2 SO-DIMMs

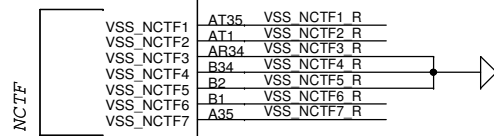
VDDQ(SO DIMM) = 14*0402 1uf
 (7*0402 PER CONNECTOR)

VCCPLL(1.8V) = 1*0805 22uf
 1*0805 1uf
 1*0805 22uf
 1*0603 4.7uf

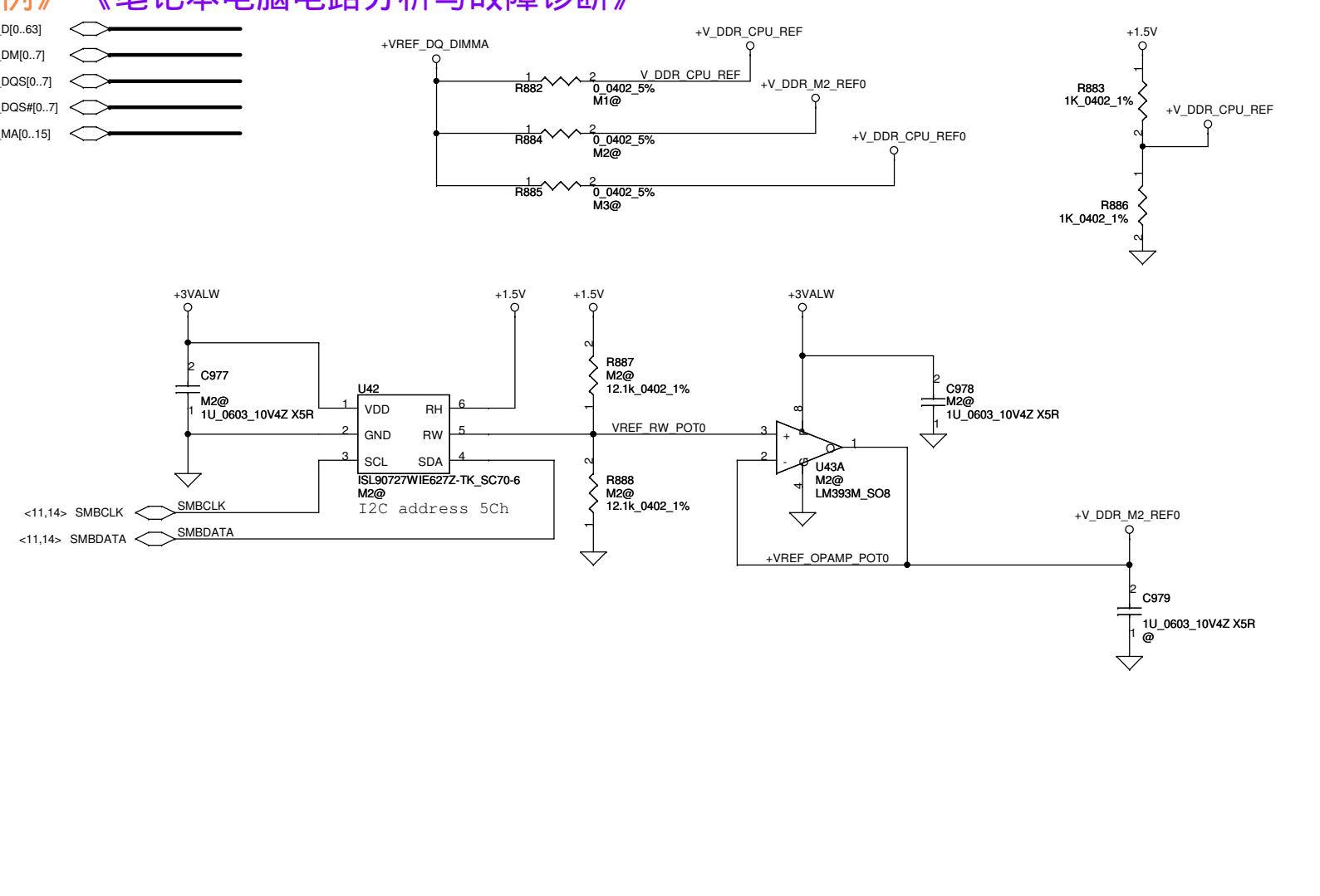
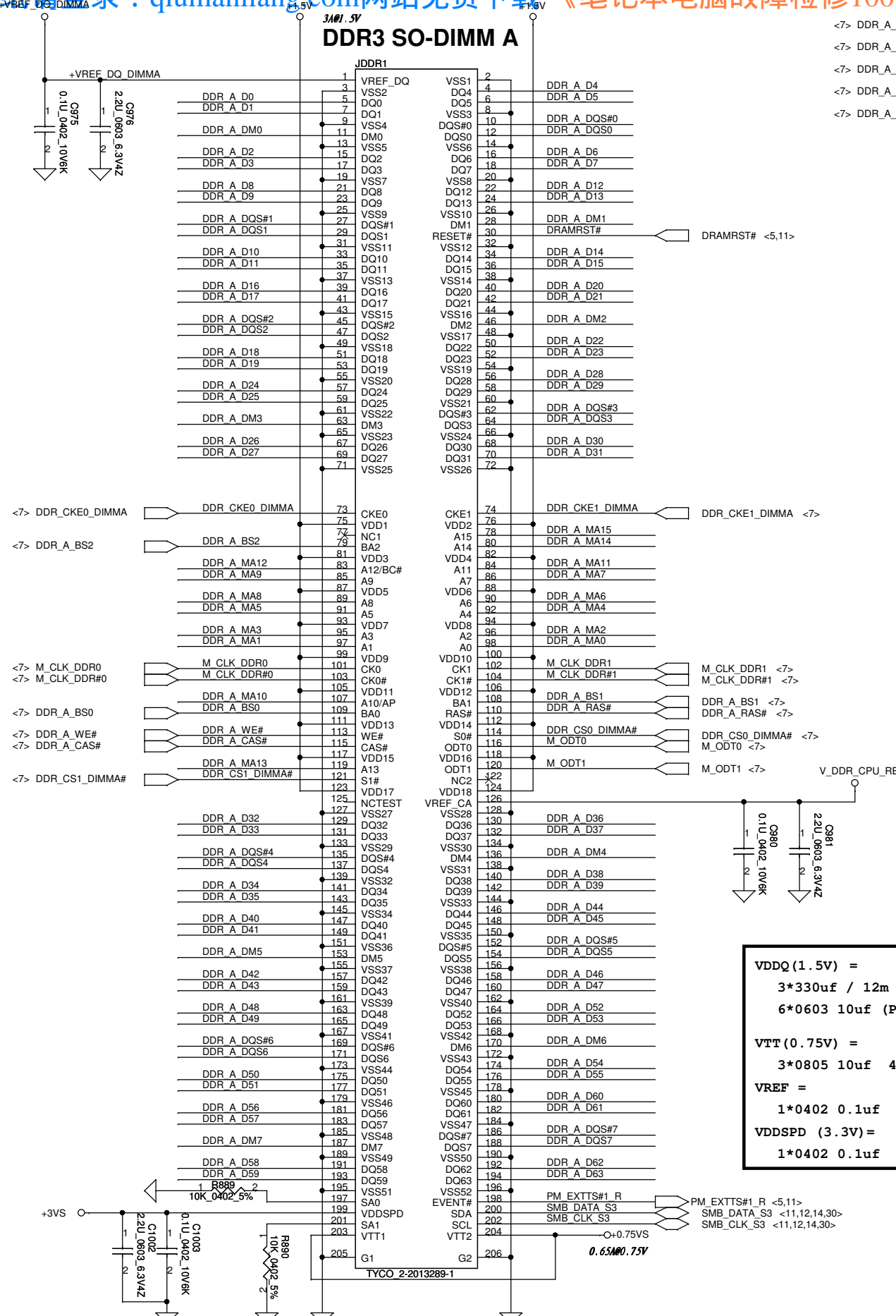
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+CPU_CORE = 12*0805 22uf INSIDE CAVITY
7*0805 10uf UNDER CAVITY AND 9*0805 10uf BETWEEN INDUCTOR AND SOCKET ON TOP LAYER
4*470uf/4m ohm 2*470uf



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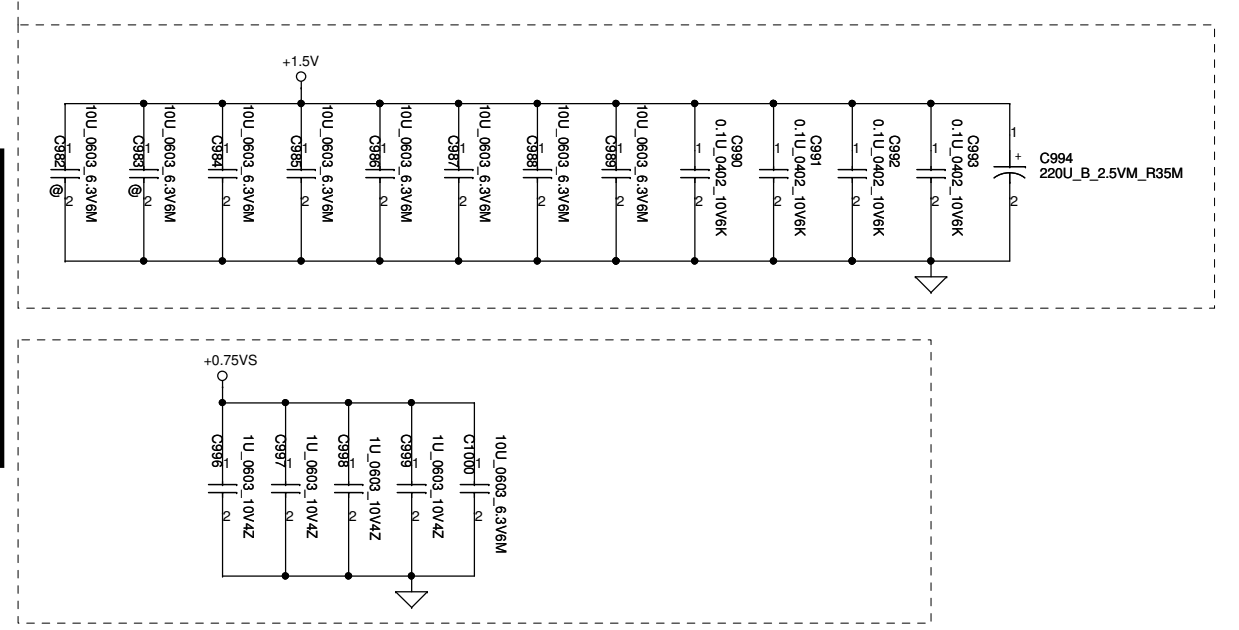
Layout Note:
Place near DIMM

VDDQ (1.5V) =
3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
6*0603 10uf (PER CONNECTOR)

VTT (0.75V) =
3*0805 10uf 4*0402 1uf

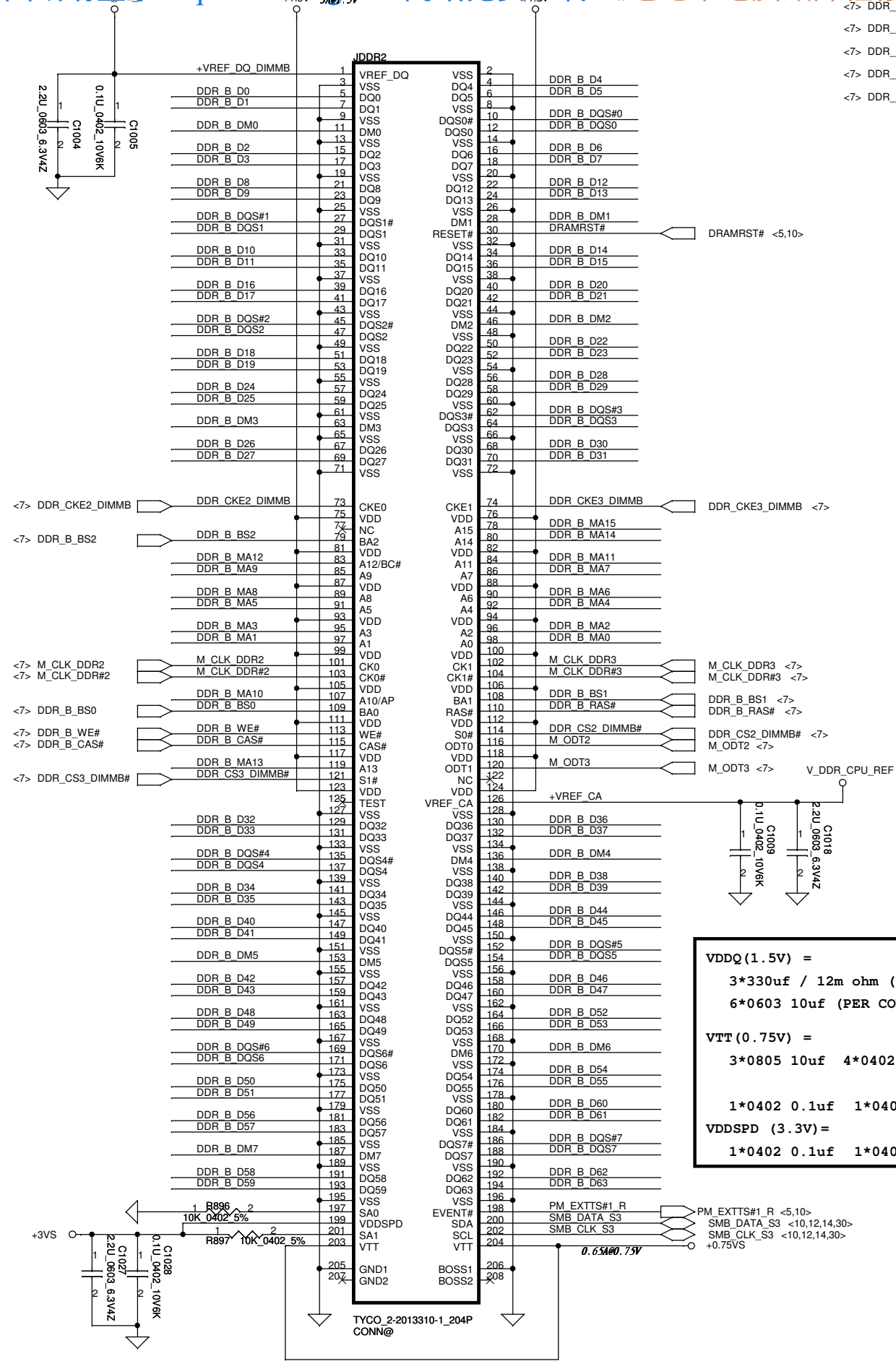
VREF =
1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V) =
1*0402 0.1uf 1*0402 2.2uf

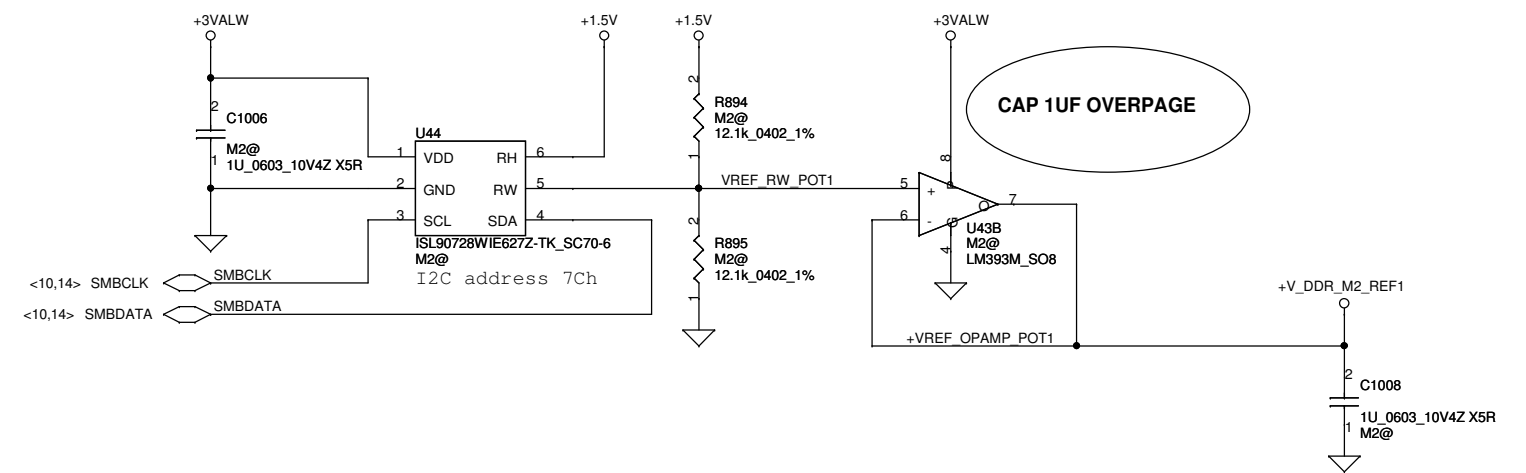
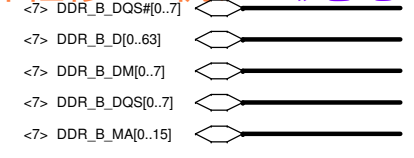


TOP SLOT

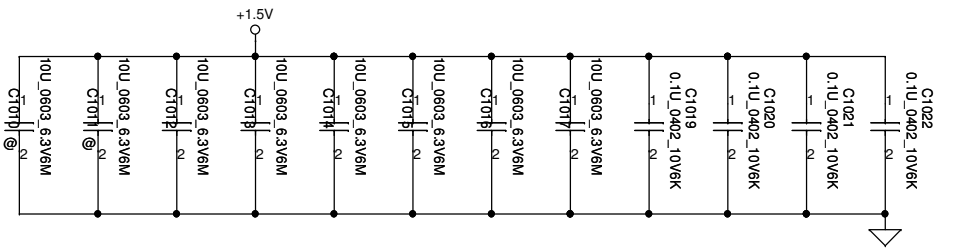
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Size	Document Number	Rev		0.2	
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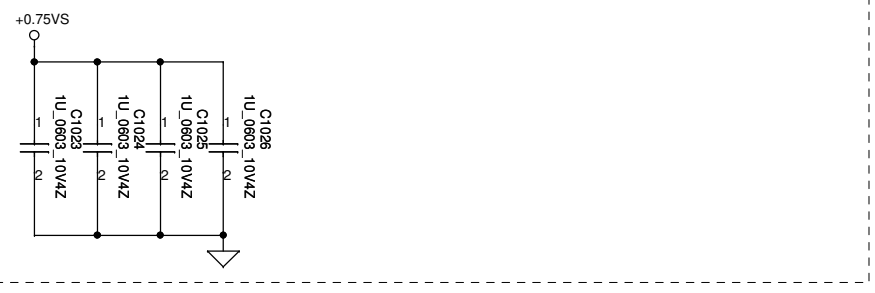
BOT SLOT



Layout Note:
Place near DIMM



Layout Note:
Place near DIMM



VDDQ (1.5V) =
 3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
 6*0603 10uf (PER CONNECTOR)

VTT (0.75V) =
 3*0805 10uf 4*0402 1uf

VDDSPD (3.3V) =
 1*0402 0.1uf 1*0402 2.2uf

VDDSPD (3.3V) =
 1*0402 0.1uf 1*0402 2.2uf

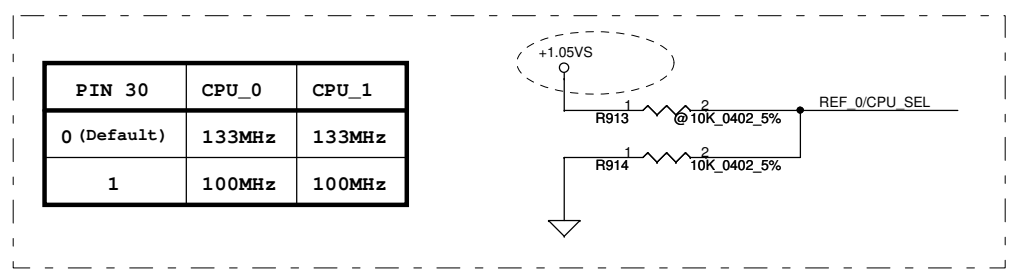
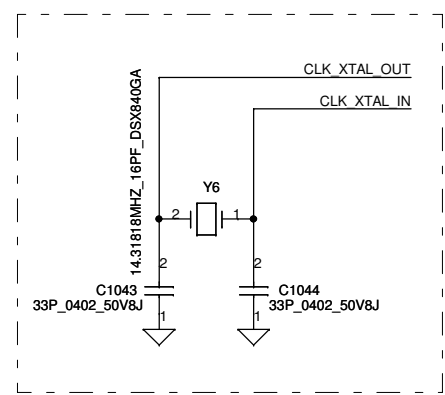
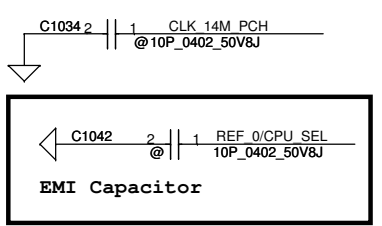
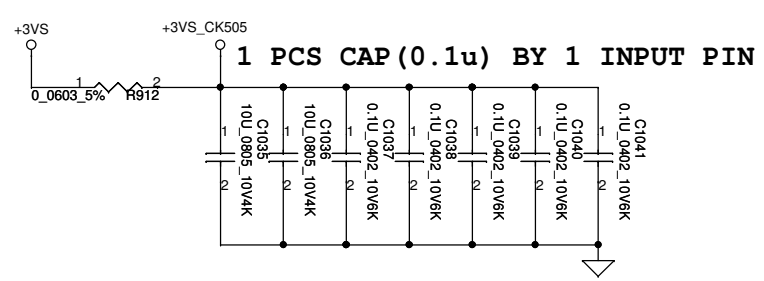
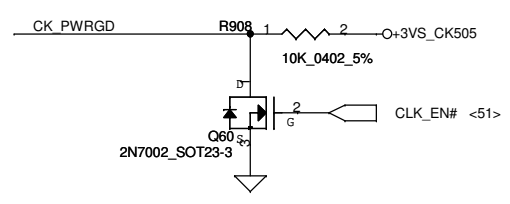
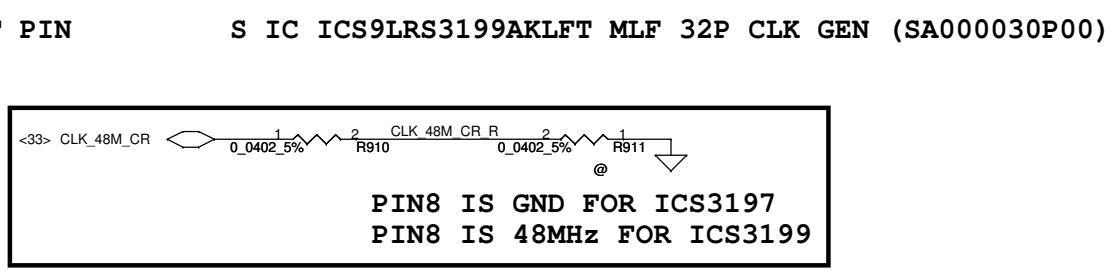
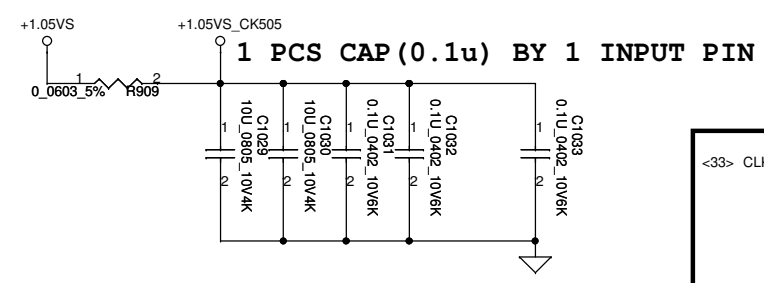
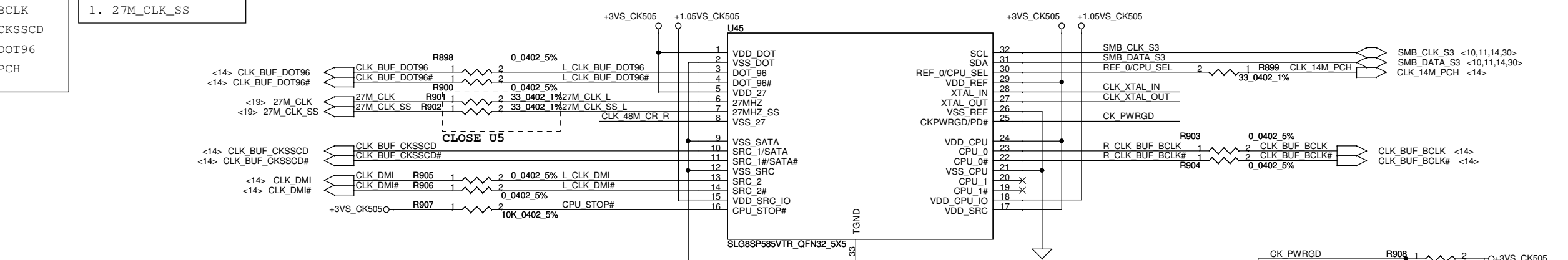
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				DDR3-SODIMM SLOT2	
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- CLK GEN TO PCH**

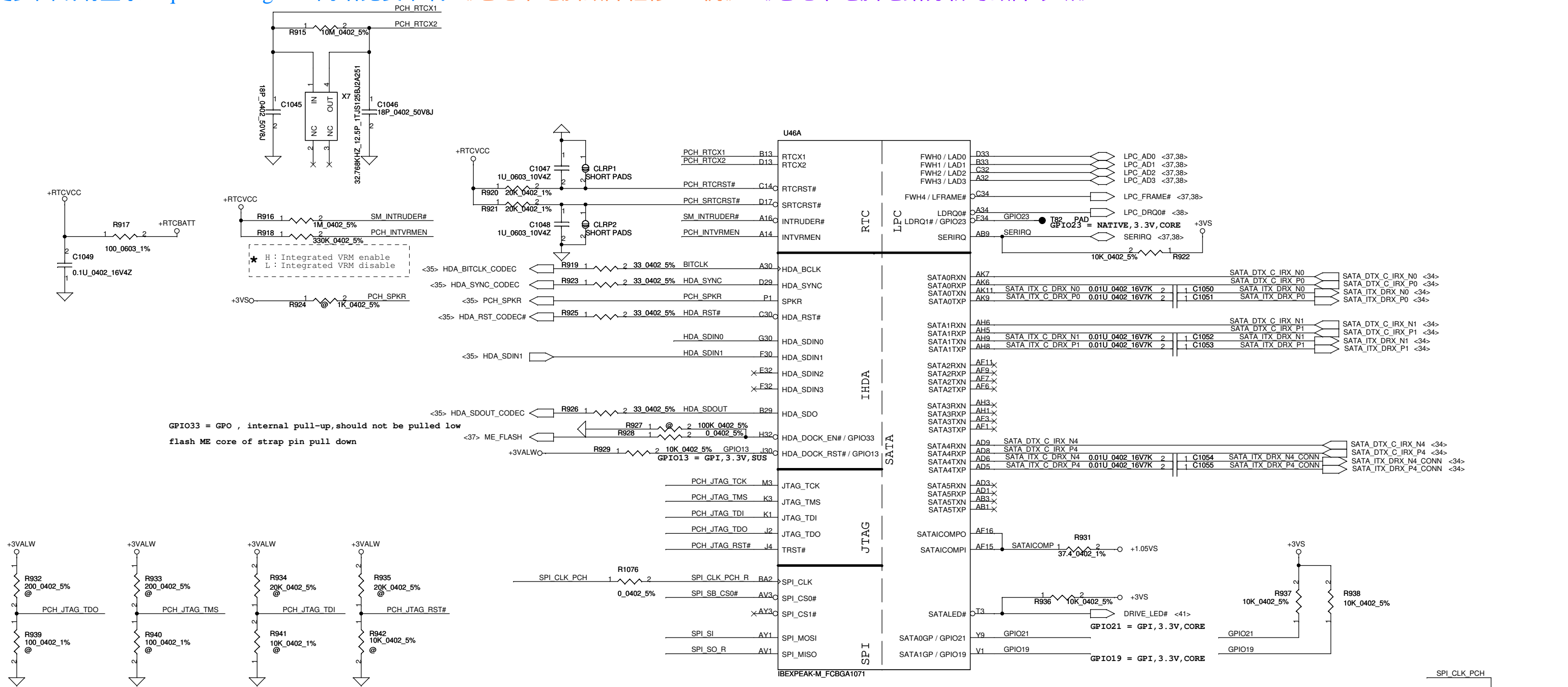
 1. CLK_DMI
 2. CLK_BUF_BCLK
 3. CLK_BUF_CKSSCD
 4. CLK_BUF_DOT96
 5. CLK_14M_PCH

CLK GEN TO VGA

 1. 27M_CLK
 1. 27M_CLK_SS

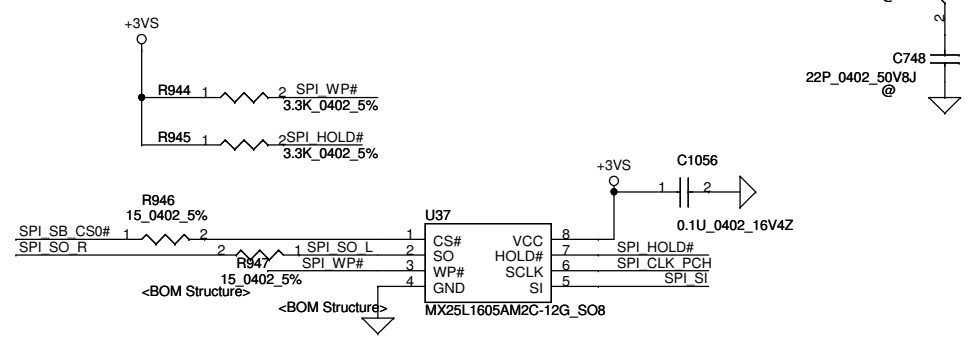


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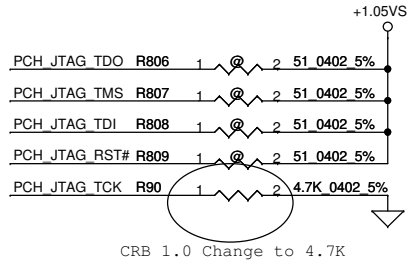
GPIO33 = GPO, internal pull-up, should not be pulled low
flash ME core of strap pin pull down

SPI ROM on ME



PCH Pin	RefDes	PCH JTAG Enable		PCH JTAG Disable	
		ES1	ES2	ES1	ES2
PCH_JTAG_TDO	R104	No Install	200ohm	No Install	No Install
	R108	No Install	100ohm	No Install	No Install
PCH_JTAG_TMS	R105	200ohm	200ohm	No Install	No Install
	R109	100ohm	100ohm	No Install	No Install
PCH_JTAG_TDI	R106	200ohm	200ohm	20Kohm	No Install
	R110	100ohm	100ohm	10Kohm	No Install
PCH_JTAG_TCK	R97	51ohm	51ohm	51ohm	51ohm
	R107	20Kohm	20Kohm	No Install	No Install
PCH_JTAG_RST#	R110	10Kohm	10Kohm	No Install	No Install

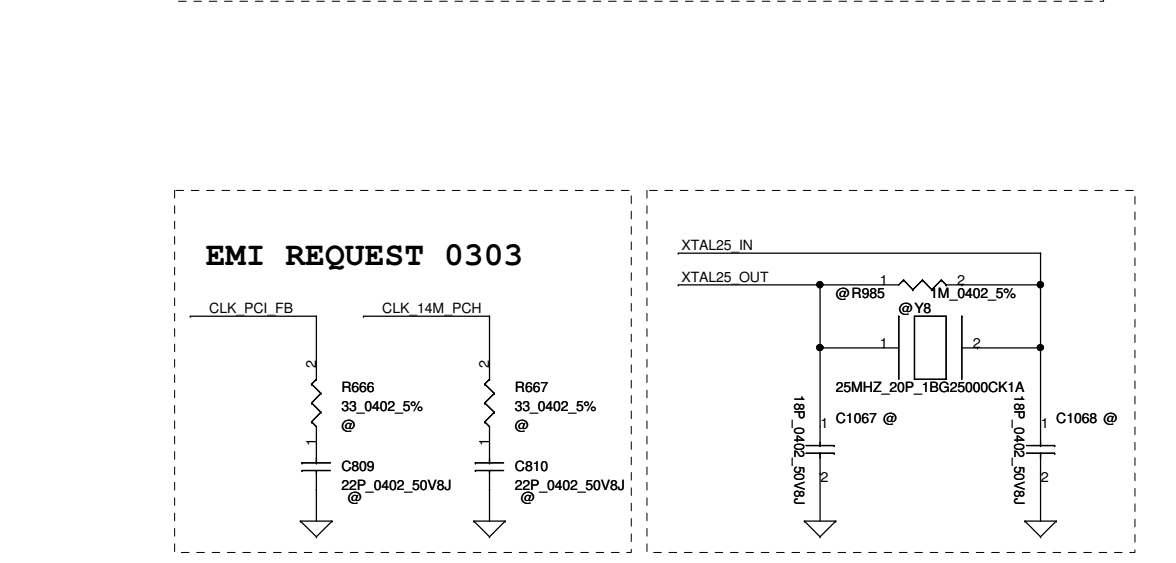
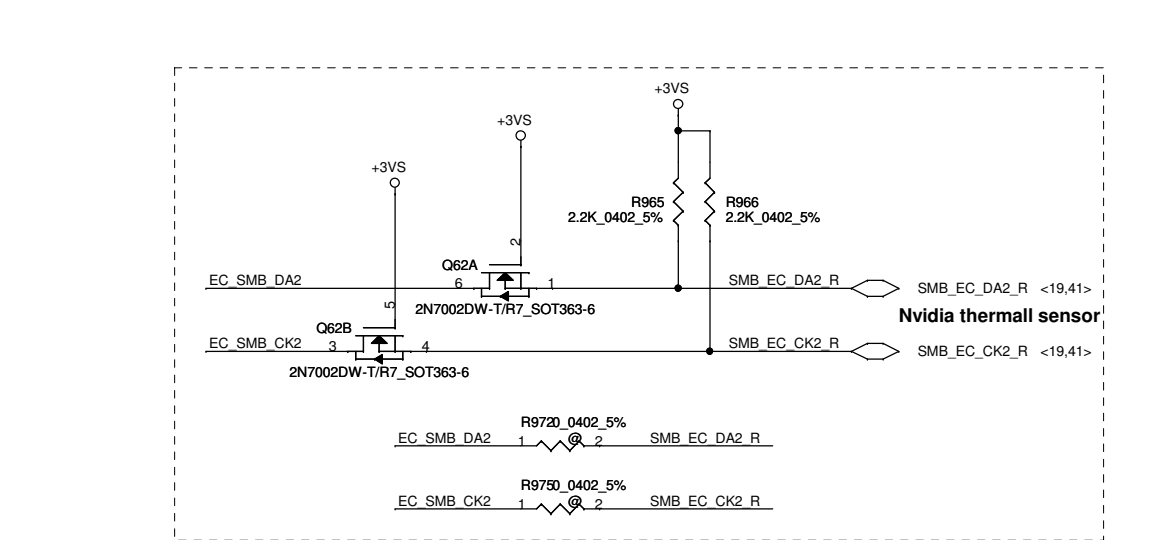
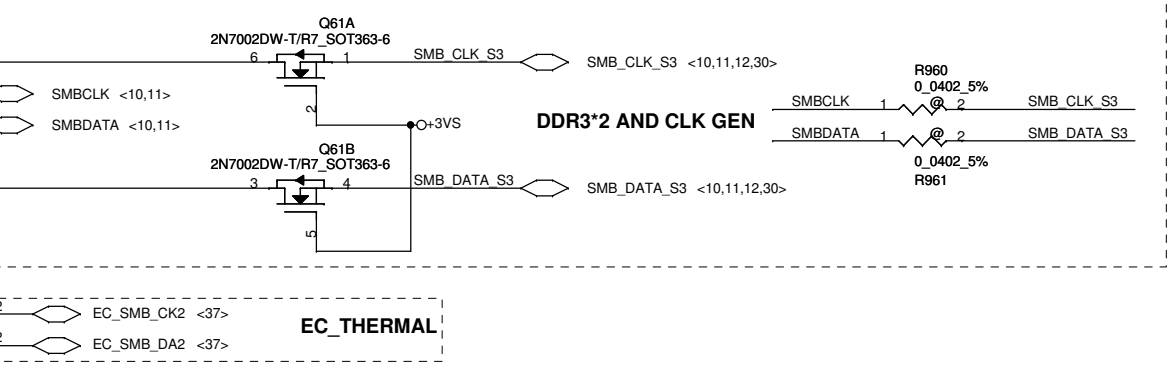
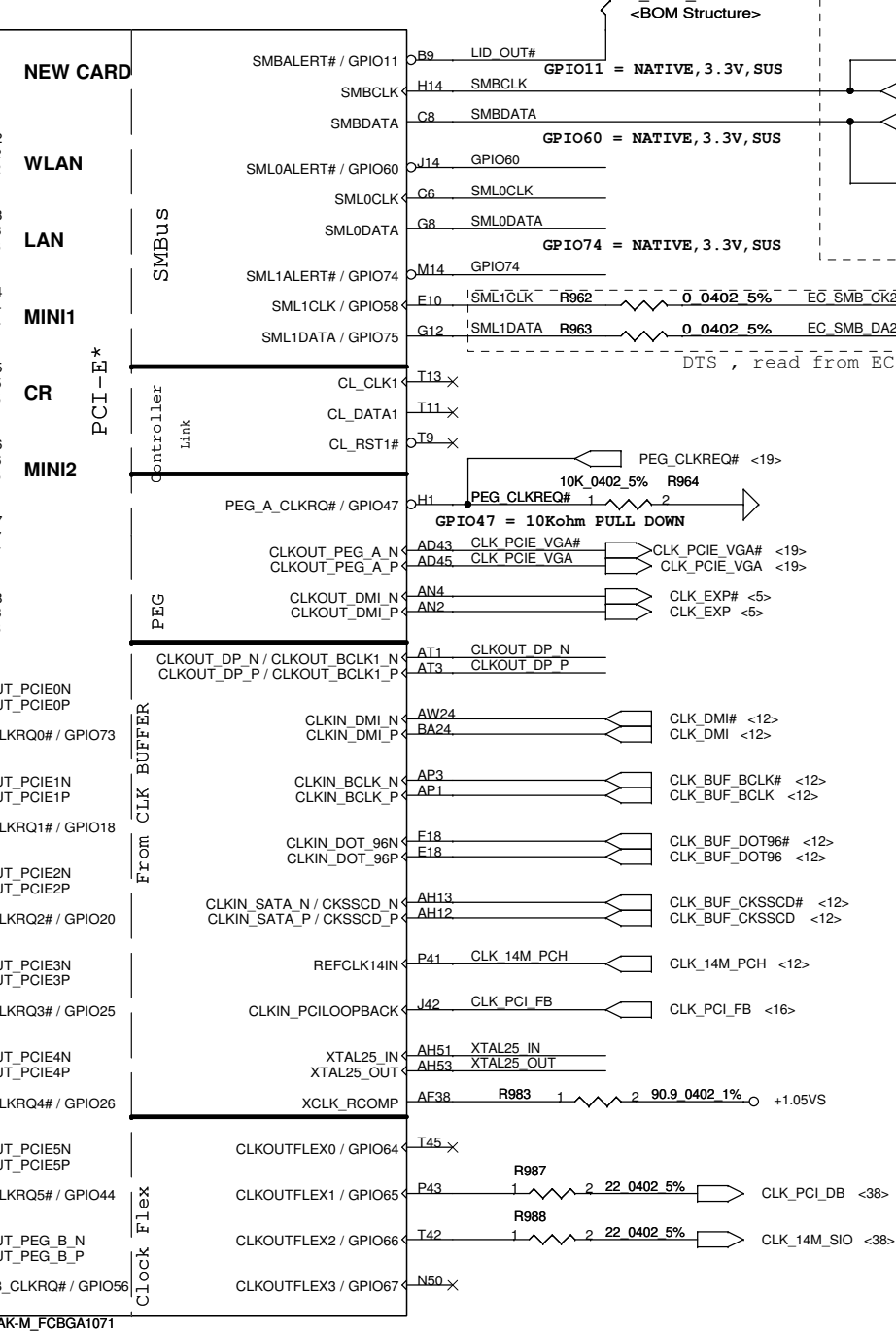
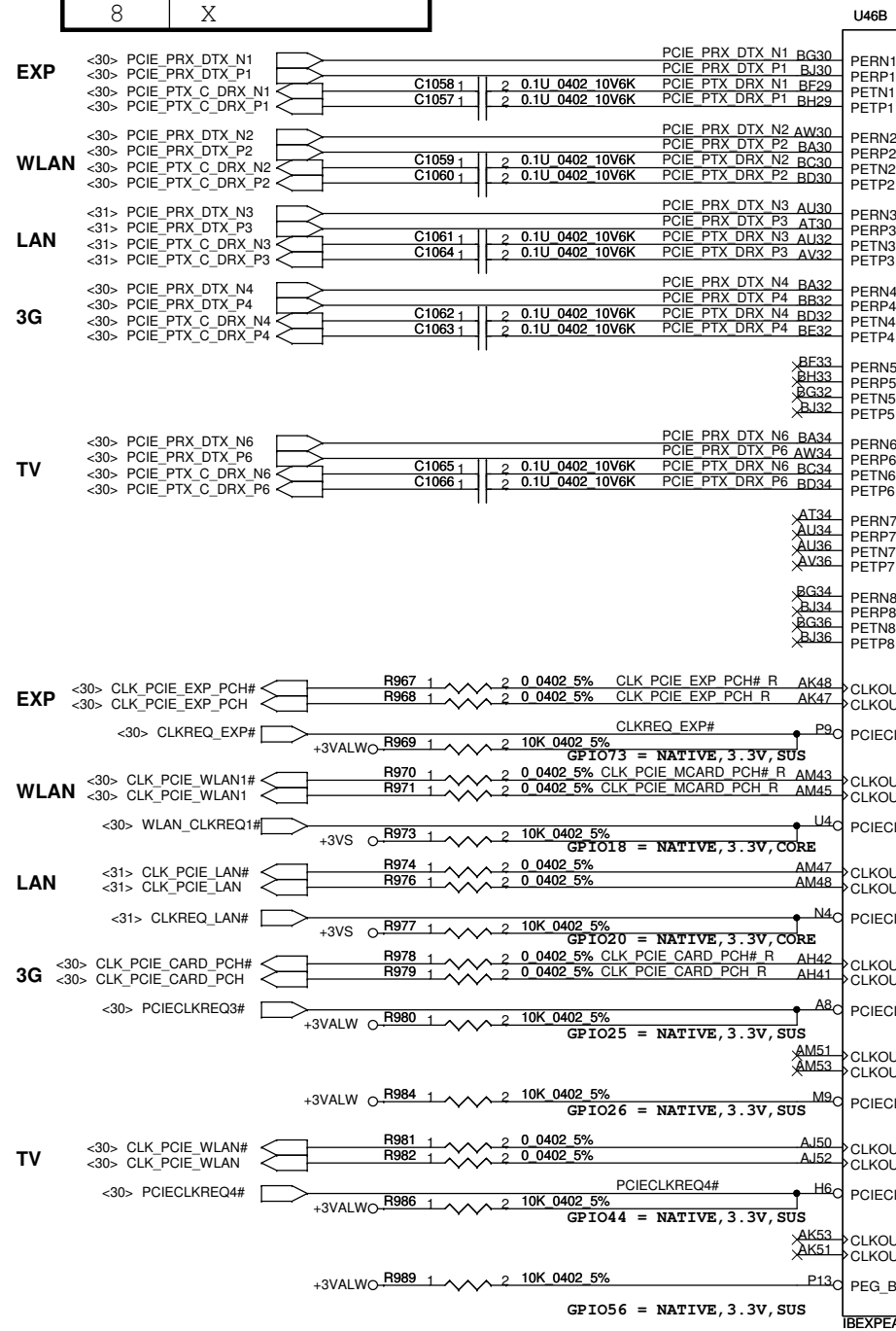
FOR EVT



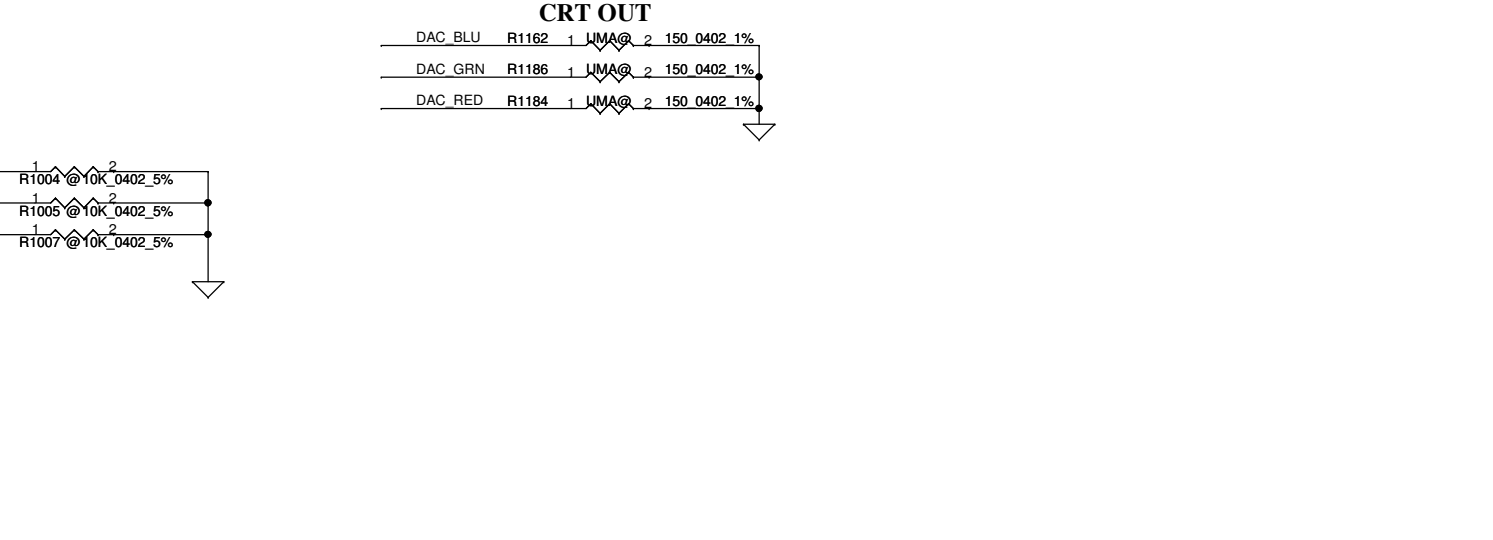
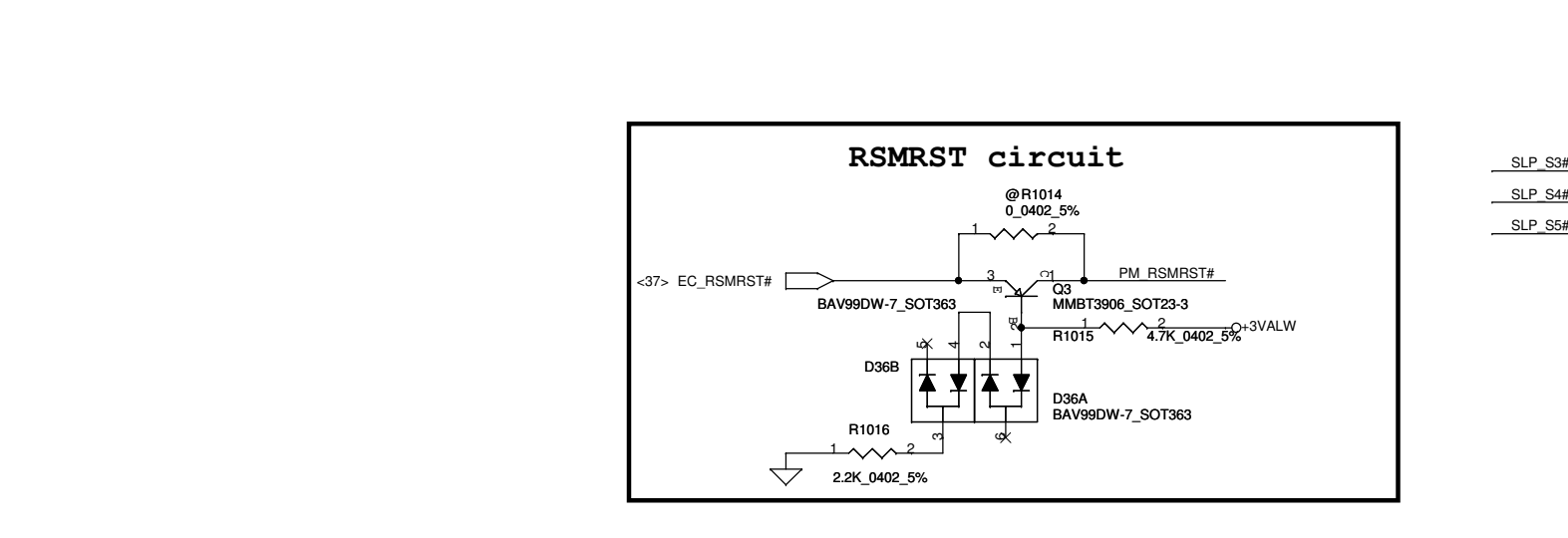
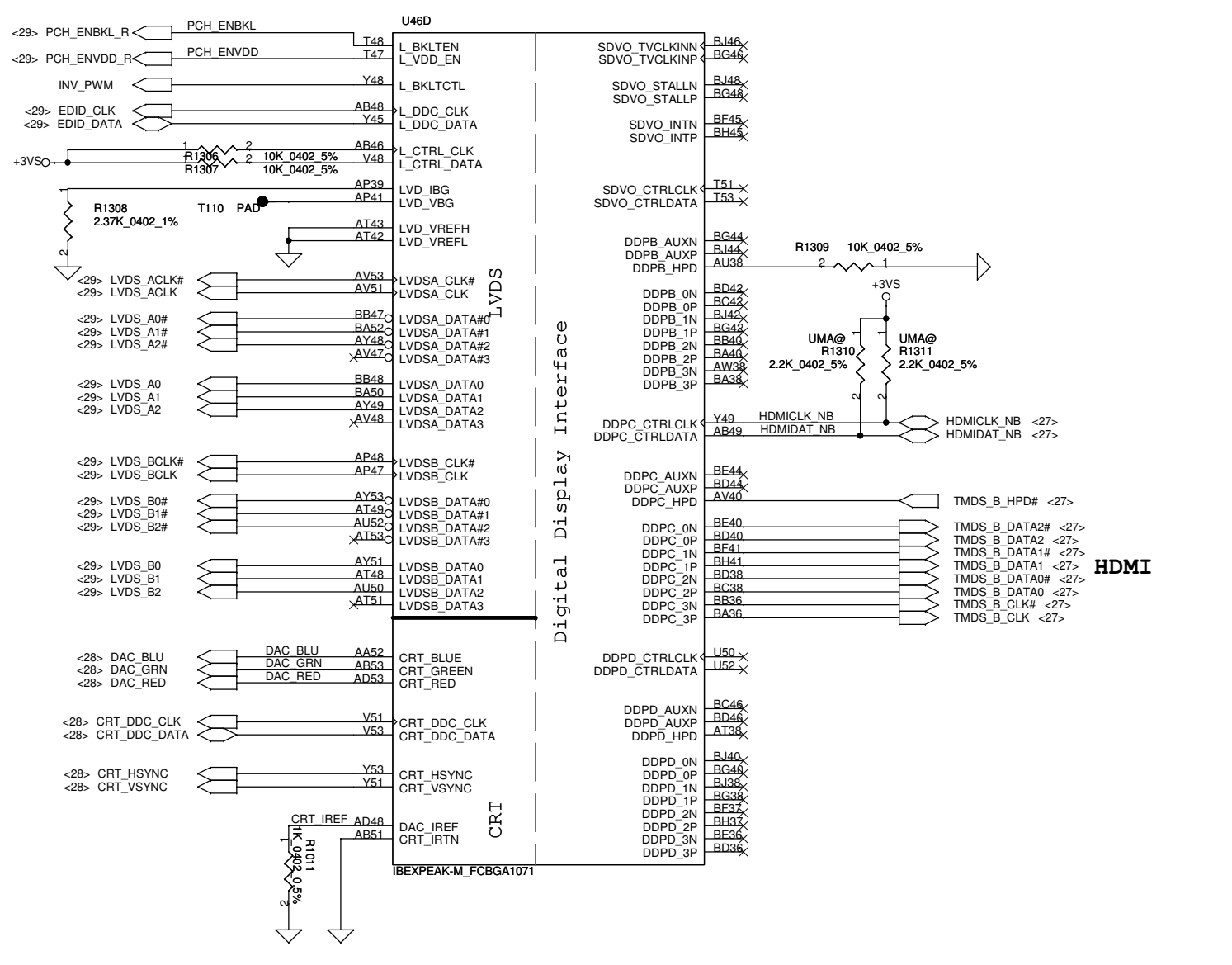
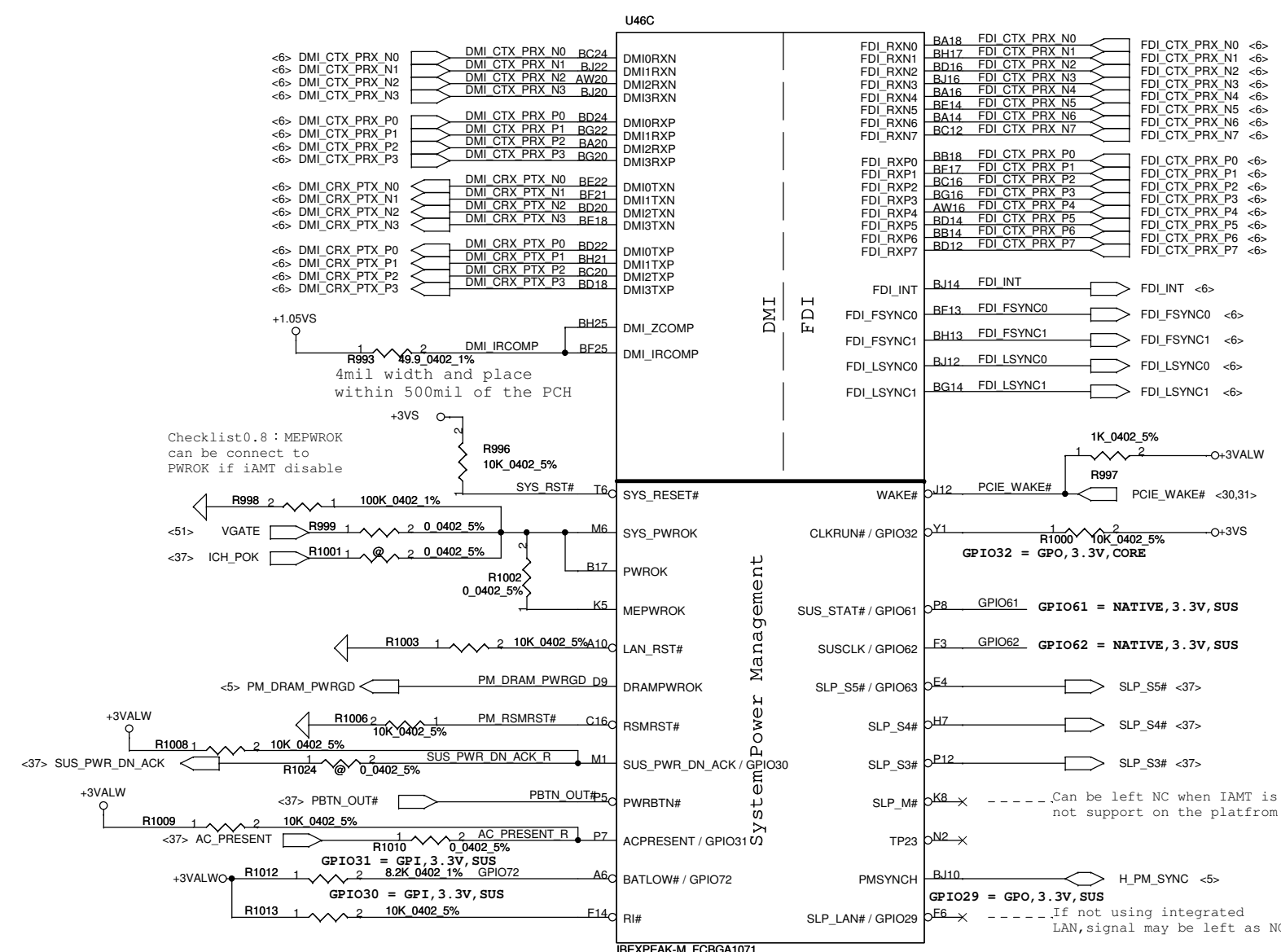
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Size	Custom	Document Number	NIWBA_LA537IP	Rev
Date:	Tuesday, March 24, 2009	Sheet	13 of 52	0.2

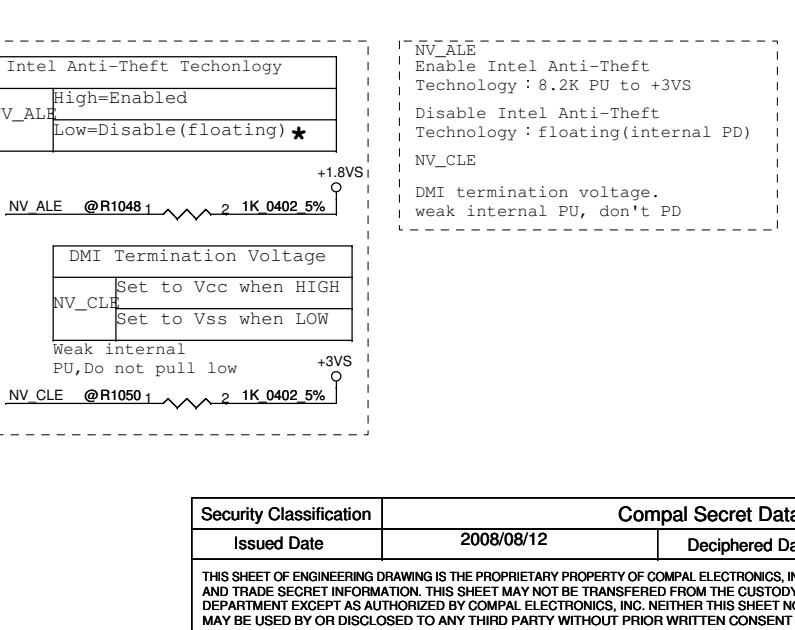
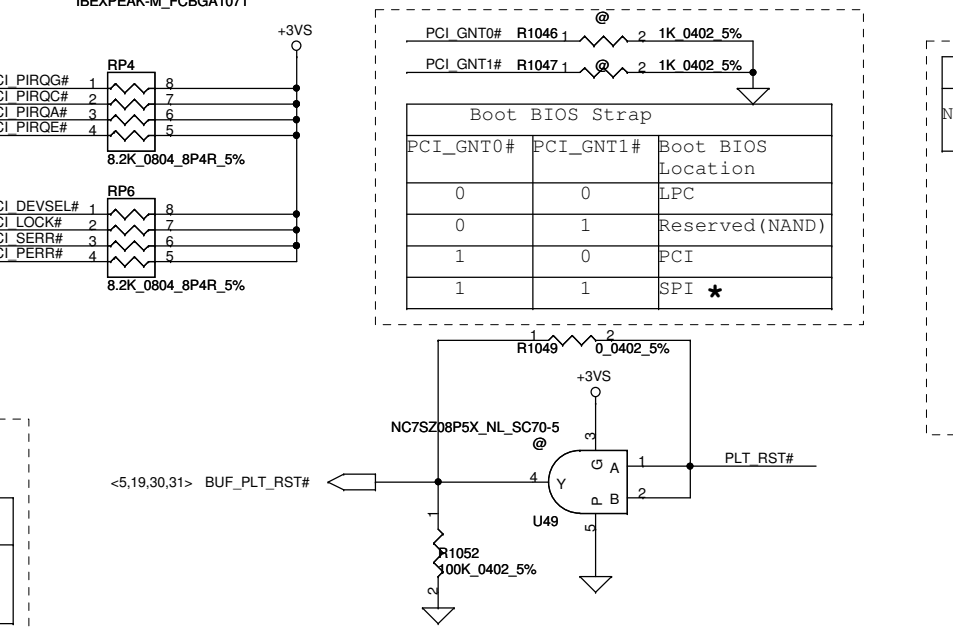
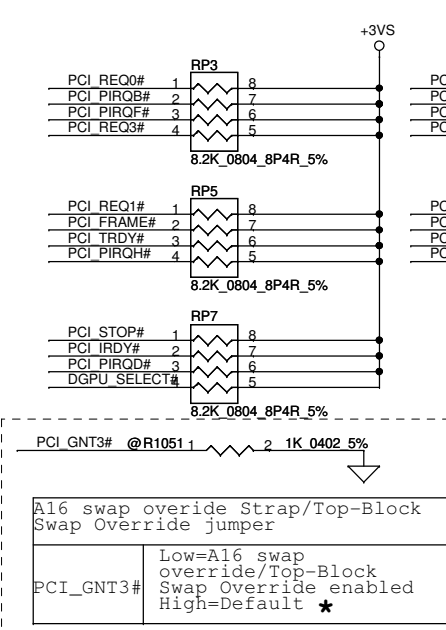
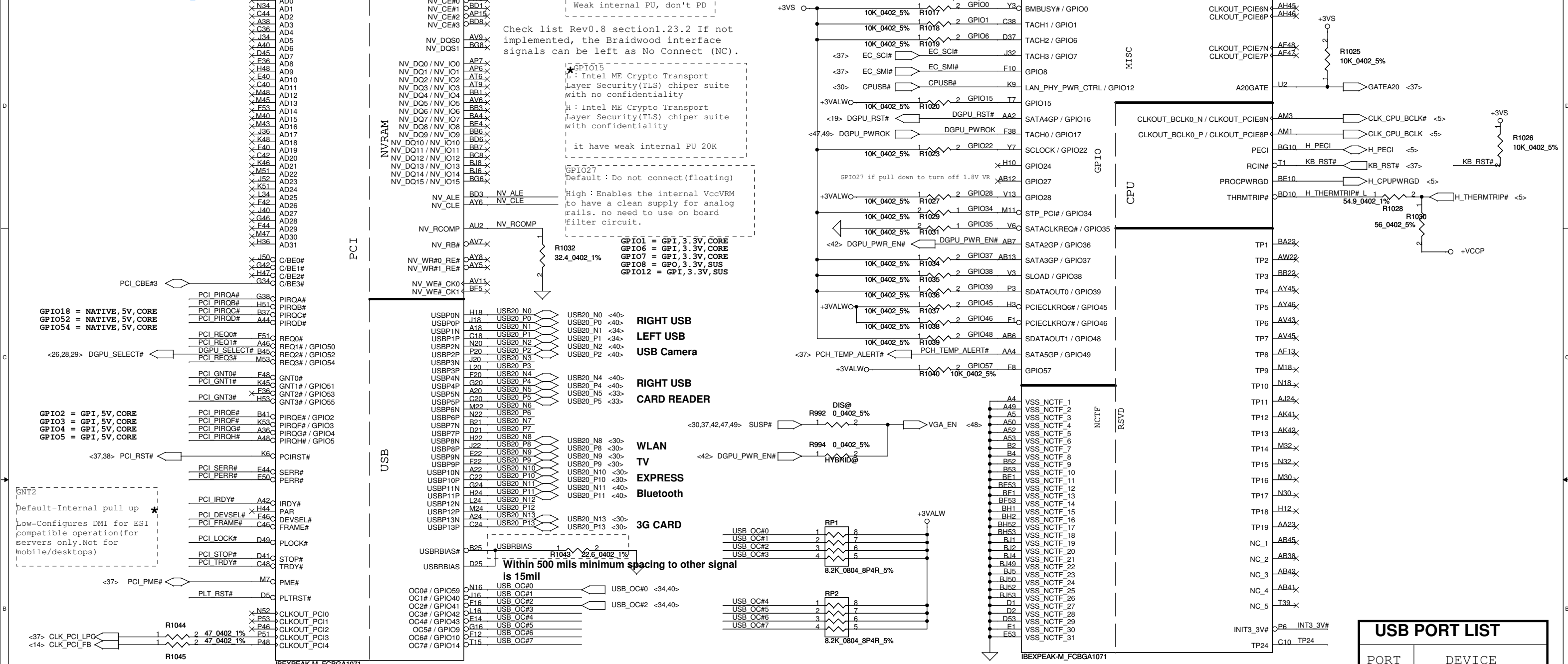
PORT	DEVICE
1	NEW CARD
2	WLAN
3	LAN
4	3G
5	X
6	TV TUNNER
7	X
8	X



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Size	Custom	Document Number	NIWBA_LA537IP		Rev
Date:	Tuesday, March 24, 2009	Sheet	15	of	52

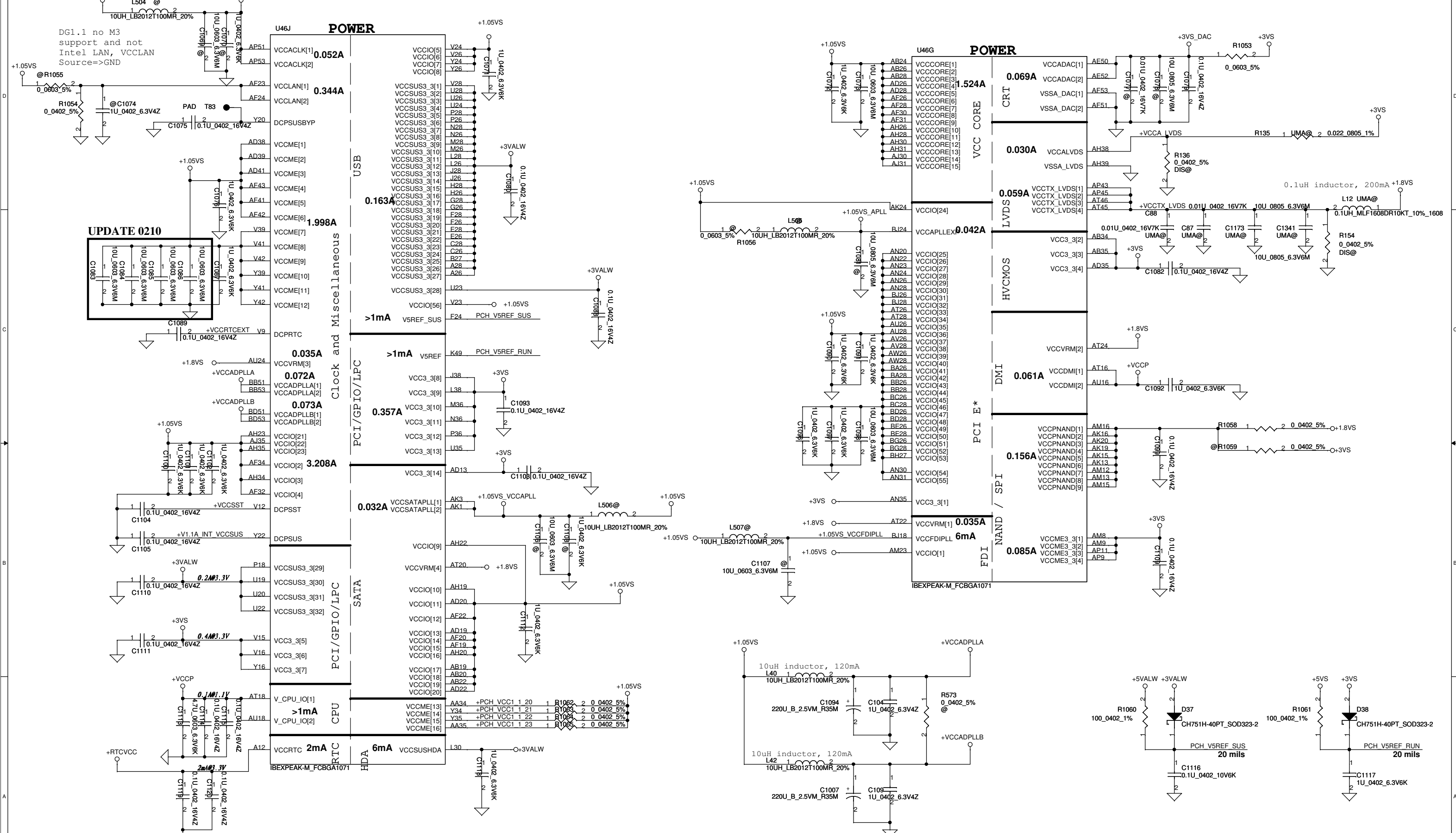


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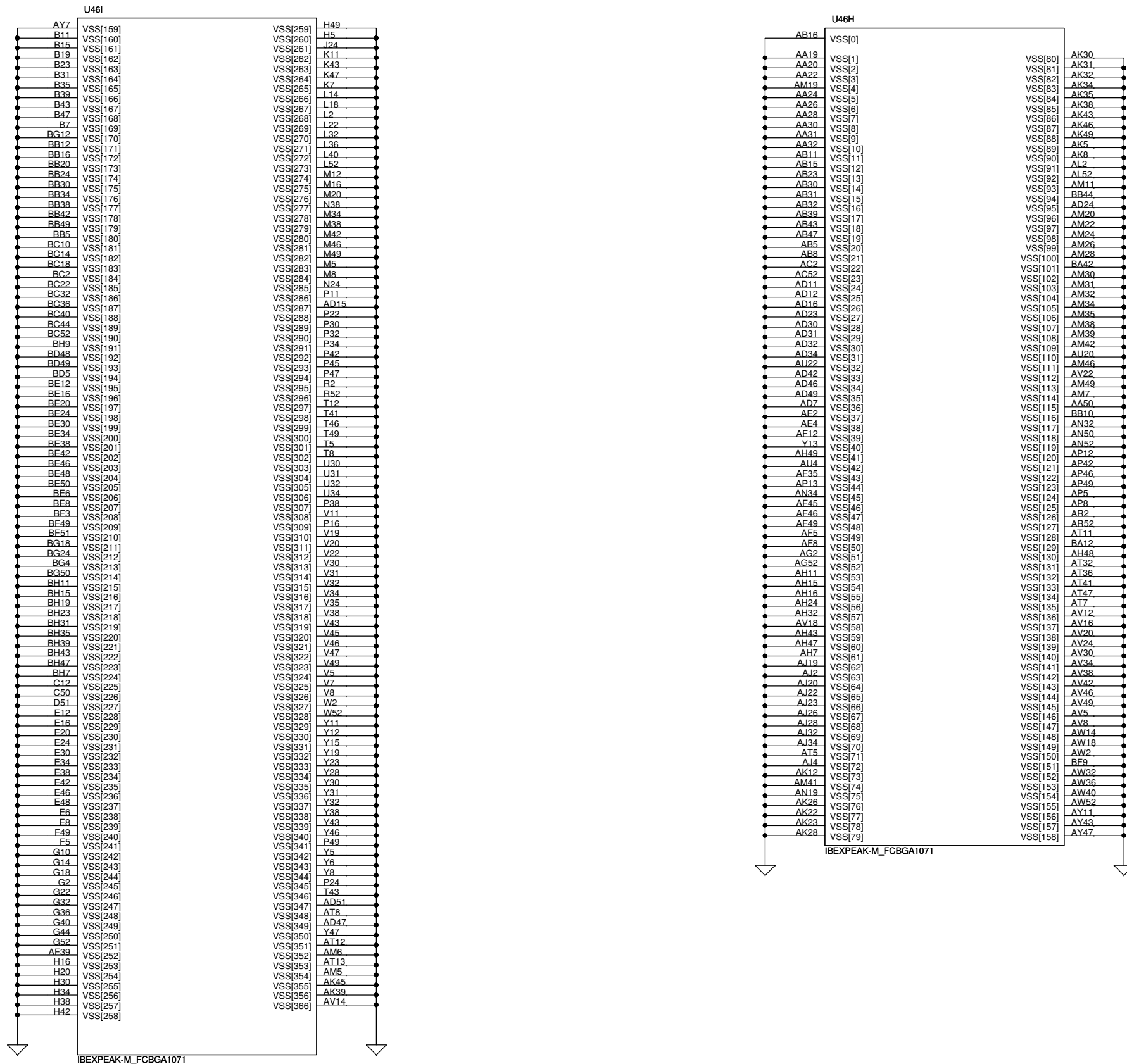
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Size Custom Document Number **NIWBA_LA5371P** Rev 0.1

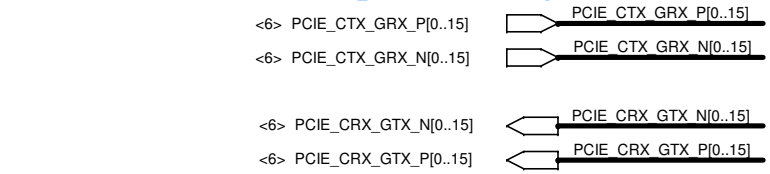
Date: Tuesday, March 24, 2009 Sheet 16 of 52



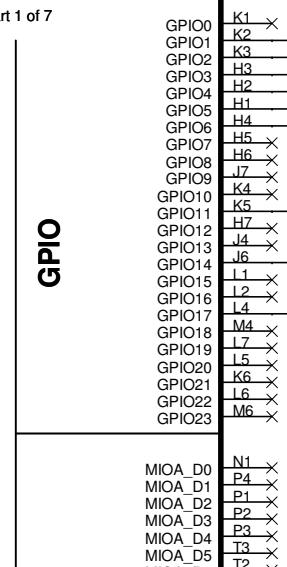
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Issued Date	2008/08/12	Deciphered Date	2009/08/12	IBEX-M(5/6)-PWR	
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				Date:	Tuesday, March 24, 2009
				Sheet	17 of 52



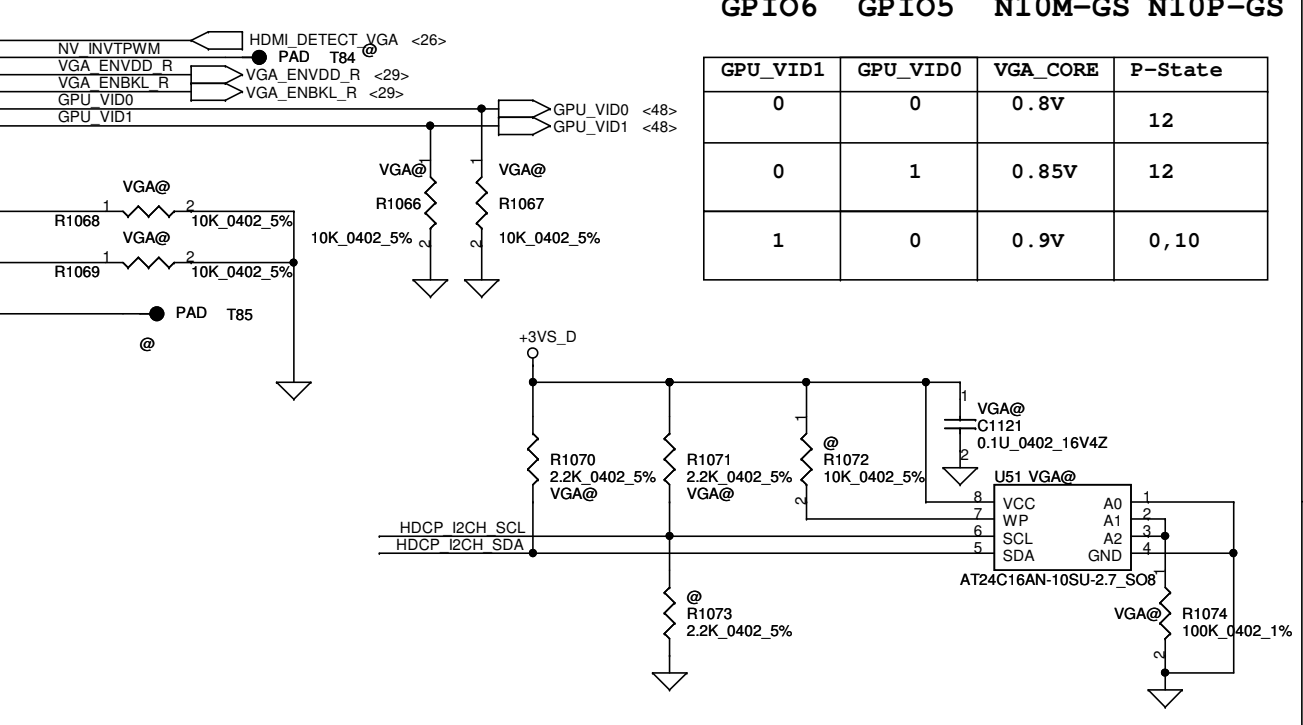
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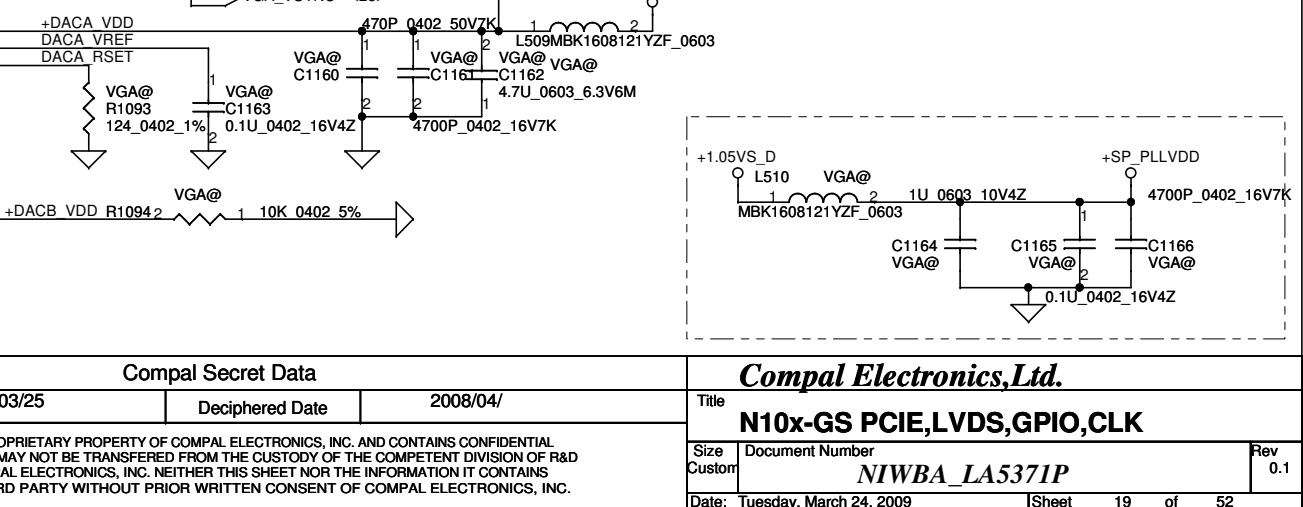
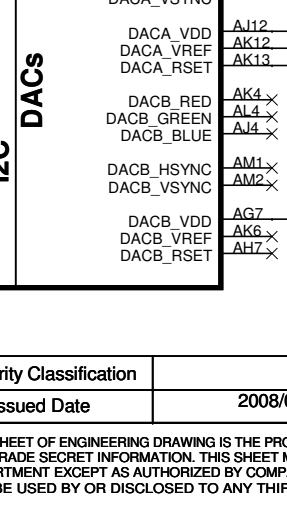
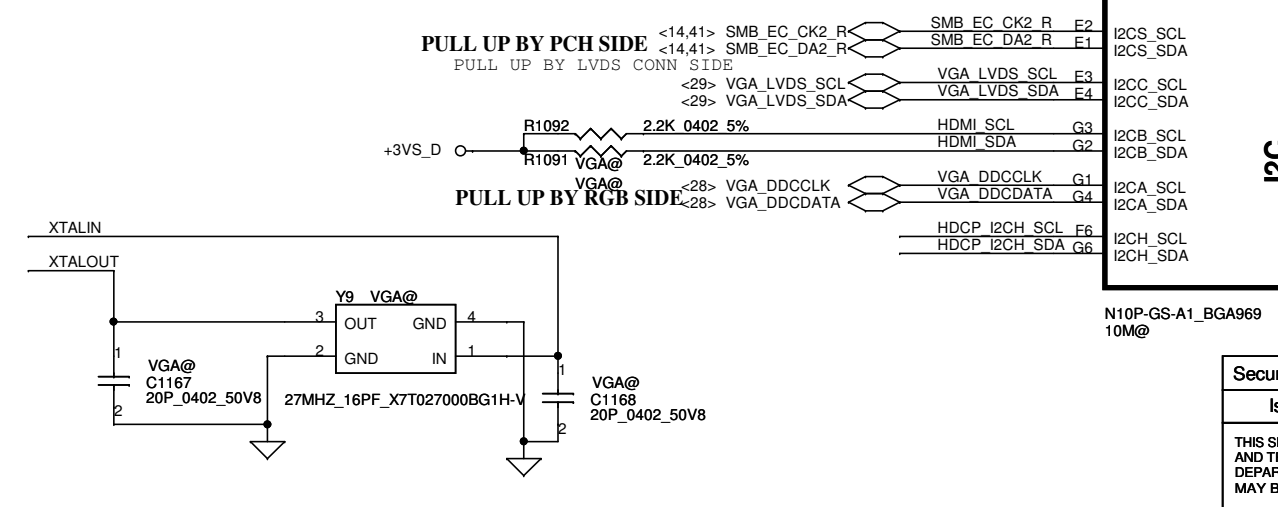
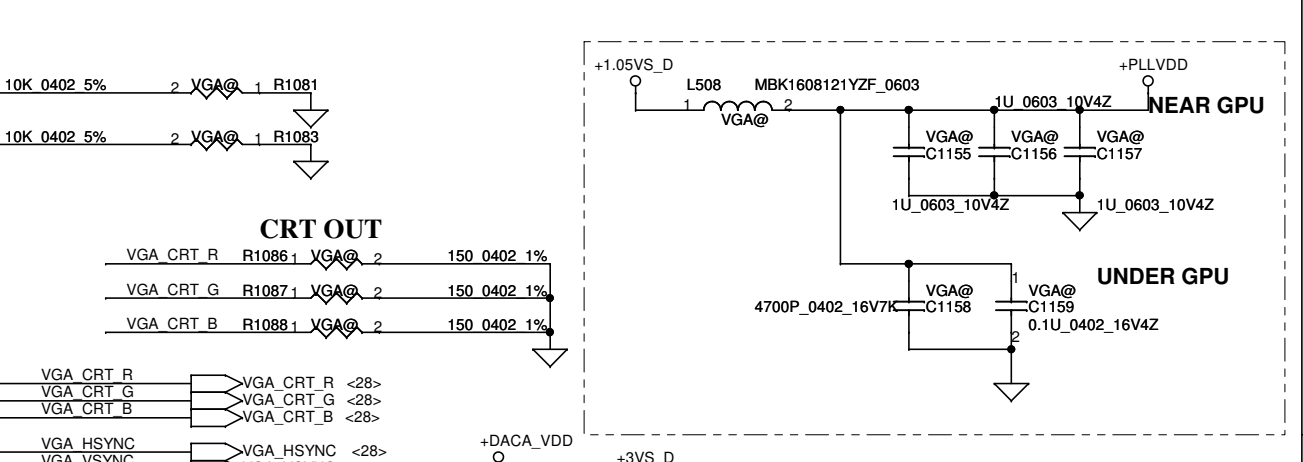
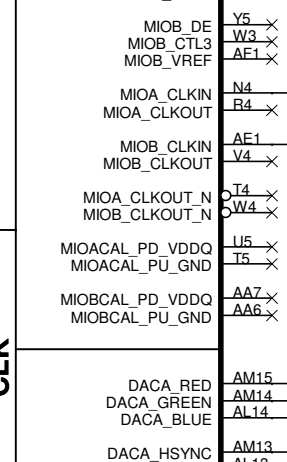
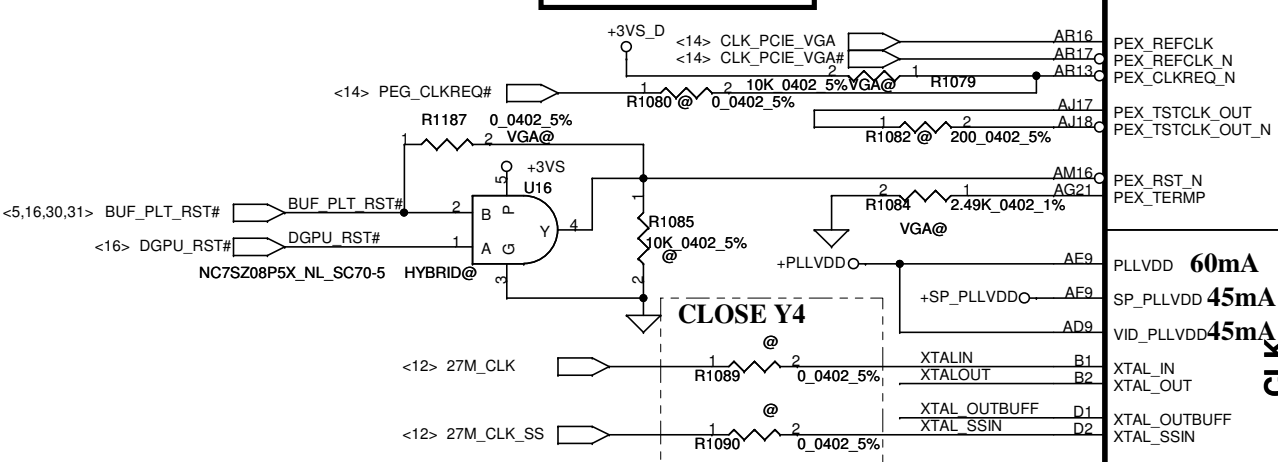
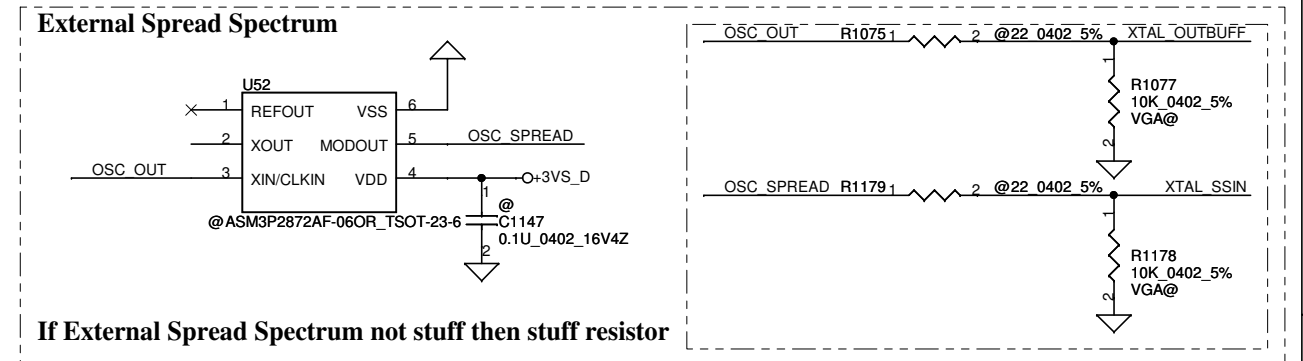
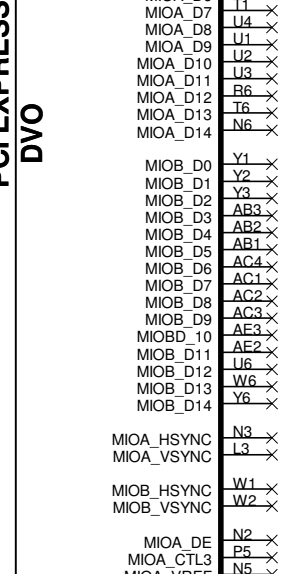
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PCIE CTX GRX P2	AR19	PEX_RX2	PCIE CTX GRX N2	AR19	PEX_RX2_N
PCIE CTX GRX P3	AP20	PEX_RX3	PCIE CTX GRX N3	AN20	PEX_RX3_N
PCIE CTX GRX P4	AN22	PEX_RX4	PCIE CTX GRX N4	AN22	PEX_RX4_N
PCIE CTX GRX P5	AR22	PEX_RX5	PCIE CTX GRX N5	AR22	PEX_RX5_N
PCIE CTX GRX P6	AP23	PEX_RX6	PCIE CTX GRX N6	AN23	PEX_RX6_N
PCIE CTX GRX P7	AN25	PEX_RX7	PCIE CTX GRX N7	AN25	PEX_RX7_N
PCIE CTX GRX P8	AR25	PEX_RX8	PCIE CTX GRX N8	AR25	PEX_RX8_N
PCIE CTX GRX P9	AP26	PEX_RX9	PCIE CTX GRX N9	AN26	PEX_RX9_N
PCIE CTX GRX P10	AN28	PEX_RX10	PCIE CTX GRX N10	AN28	PEX_RX10_N
PCIE CTX GRX P11	AR28	PEX_RX11	PCIE CTX GRX N11	AR28	PEX_RX11_N
PCIE CTX GRX P12	AP29	PEX_RX12	PCIE CTX GRX N12	AN29	PEX_RX12_N
PCIE CTX GRX P13	AN31	PEX_RX13	PCIE CTX GRX N13	AN31	PEX_RX13_N
PCIE CTX GRX P14	AR31	PEX_RX14	PCIE CTX GRX N14	AR31	PEX_RX14_N
PCIE CTX GRX P15	AP34	PEX_RX15	PCIE CTX GRX N15	AN34	PEX_RX15_N



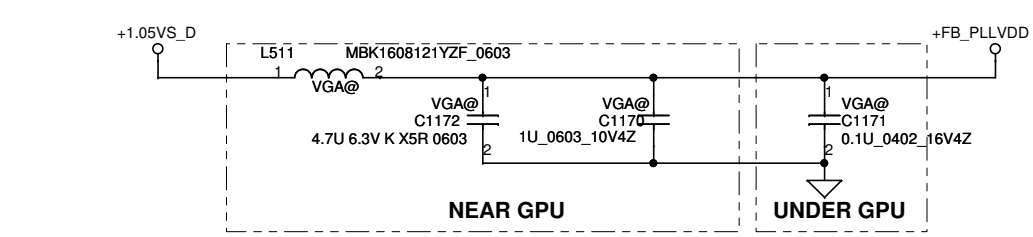
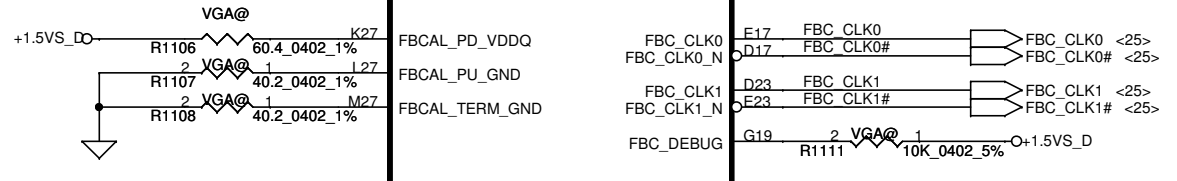
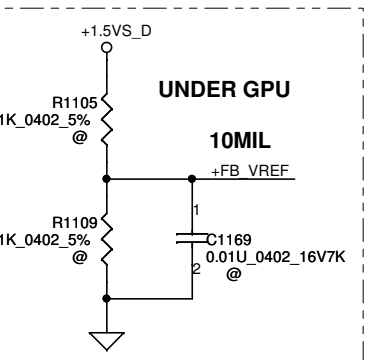
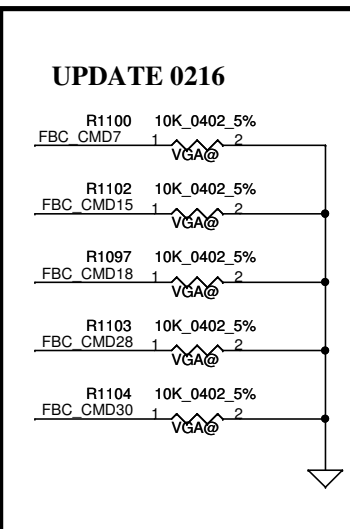
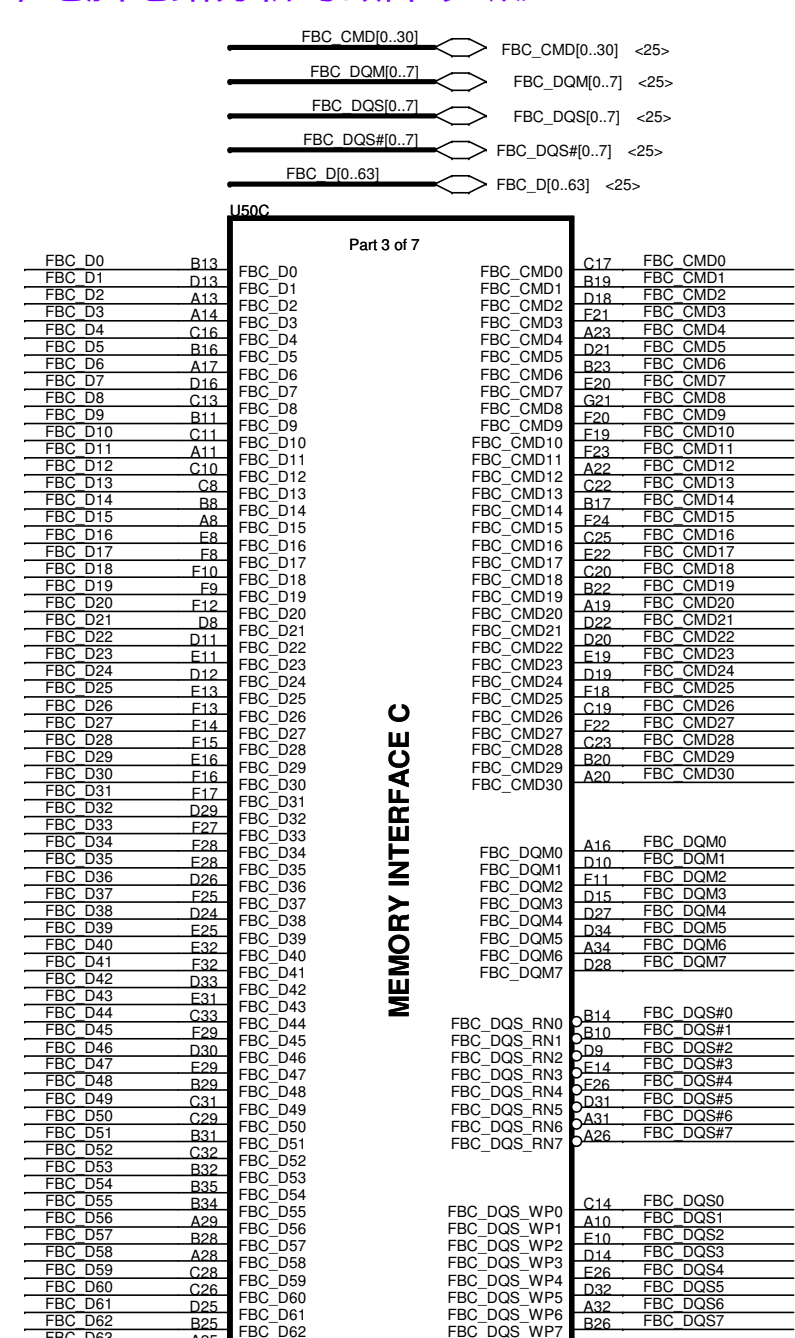
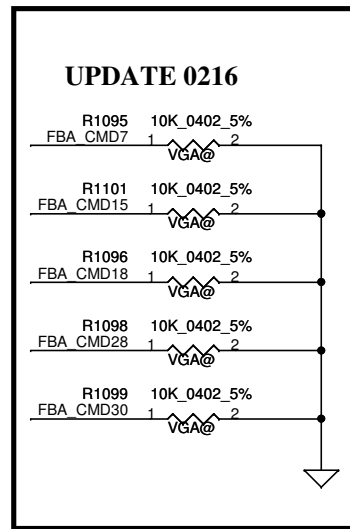
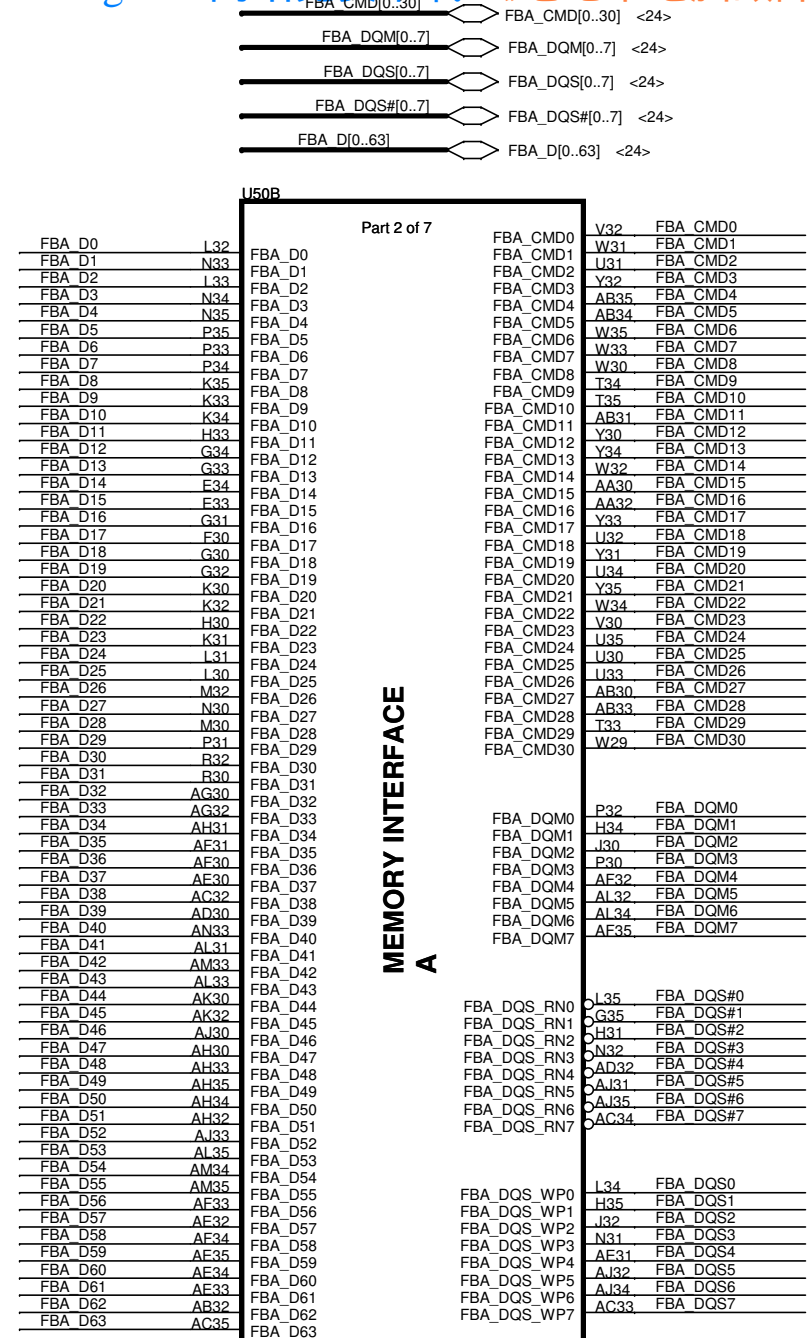
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GPU_VID1	GPU_VID0	VGA_CORE	P-State
0	0	0.8V	12
0	1	0.85V	12
1	0	0.9V	0,10



PCIE CRX GTX P0	C1122	2	0.1U	0402	10V6K	PCIE CRX GTX C P0	AL17	PEX_TX0
PCIE CRX GTX N0	C1123	2	0.1U	0402	10V6K	PCIE CRX GTX C N0	AM17	PEX_TX0_N
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PCIE CRX GTX N1	C1125	2	0.1U	0402	10V6K	PCIE CRX GTX C N1	AM18	PEX_TX1_N
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PCIE CRX GTX N2	C1127	2	0.1U	0402	10V6K	PCIE CRX GTX C N2	AK19	PEX_TX2_N
PCIE CRX GTX P3	C1128	2	0.1U	0402	10V6K	PCIE CRX GTX C P3	AL20	PEX_TX3
PCIE CRX GTX N3	C1129	2	0.1U	0402	10V6K	PCIE CRX GTX C N3	AM20	PEX_TX3_N
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PCIE CRX GTX N7	C1137	2	0.1U	0402	10V6K	PCIE CRX GTX C N7	AM24	PEX_TX7_N
PCIE CRX GTX P8	C1138	2	0.1U	0402	10V6K	PCIE CRX GTX C P8	AL25	PEX_TX8
PCIE CRX GTX N8	C1139	2	0.1U	0402	10V6K	PCIE CRX GTX C N8	AK25	PEX_TX8_N
PCIE CRX GTX P9	C1140	2	0.1U	0402	10V6K	PCIE CRX GTX C P9	AL26	PEX_TX9
PCIE CRX GTX N9	C1141	2	0.1U	0402	10V6K	PCIE CRX GTX C N9	AM26	PEX_TX9_N
PCIE CRX GTX P10	C1142	2	0.1U	0402	10V6K	PCIE CRX GTX C P10	AM27	PEX_TX10
PCIE CRX GTX N10	C1143	2	0.1U	0402	10V6K	PCIE CRX GTX C N10	AM27	PEX_TX10_N
PCIE CRX GTX P11	C1144	2	0.1U	0402	10V6K	PCIE CRX GTX C P11	AL28	PEX_TX11
PCIE CRX GTX N11	C1145	2	0.1U	0402	10V6K	PCIE CRX GTX C N11	AK28	PEX_TX11_N
PCIE CRX GTX P12	C1146	2	0.1U	0402	10V6K	PCIE CRX GTX C P12	AK29	PEX_TX12
PCIE CRX GTX N12	C1147	2	0.1U	0402	10V6K	PCIE CRX GTX C N12	AL29	PEX_TX12_N
PCIE CRX GTX P13	C1149	2	0.1U	0402	10V6K	PCIE CRX GTX C P13	AM29	PEX_TX13
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Size	Custom	Document Number	NIWBA_LA5371P	Rev
Date:	Tuesday, March 24, 2009	Sheet	19	of 52

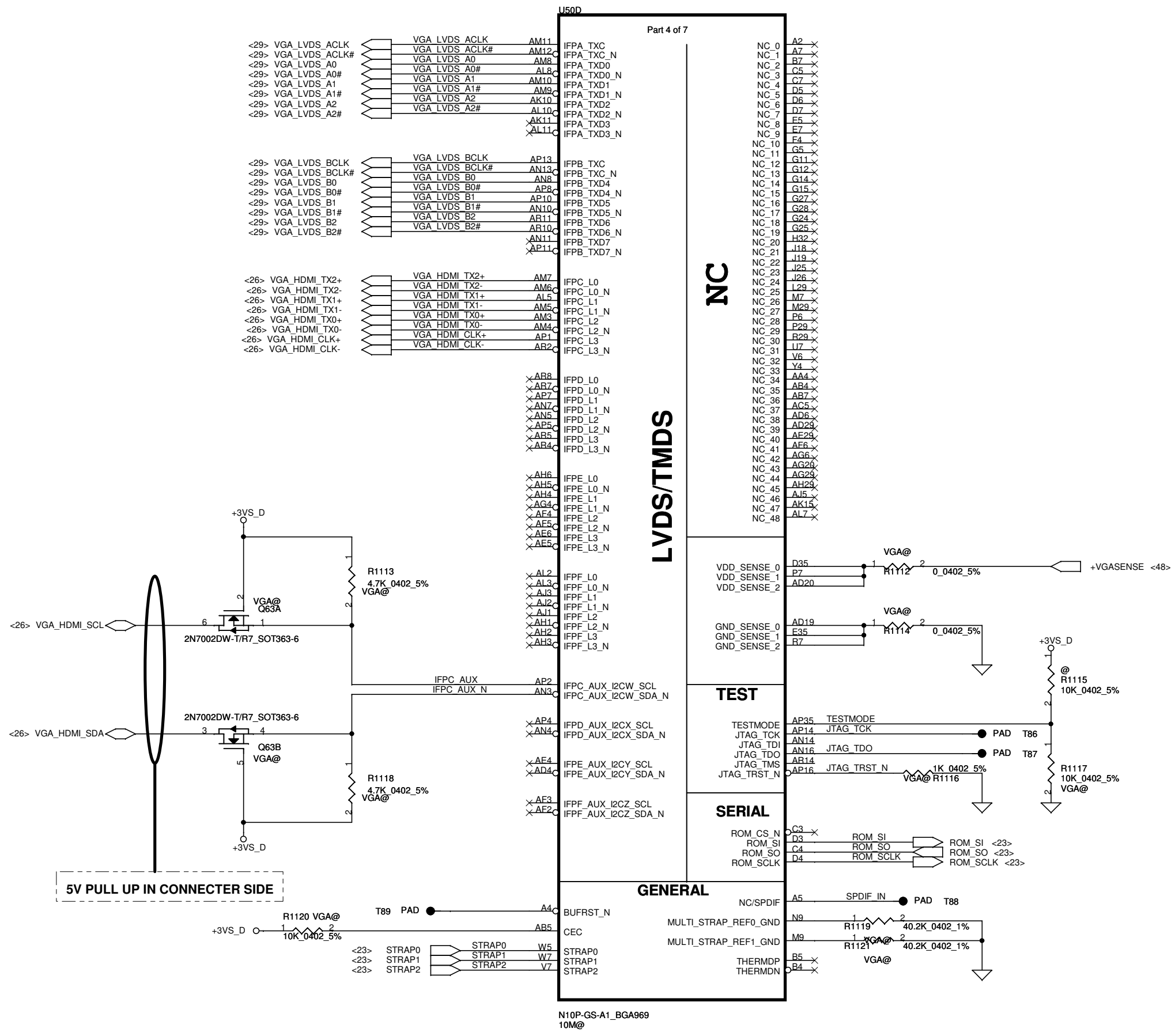


Place Components Close to BGA

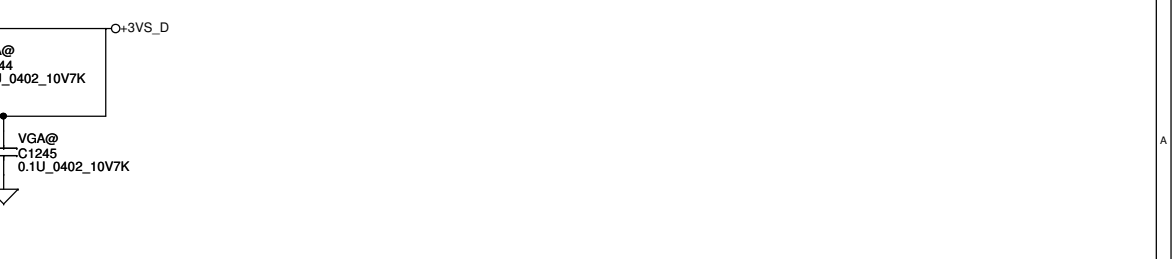
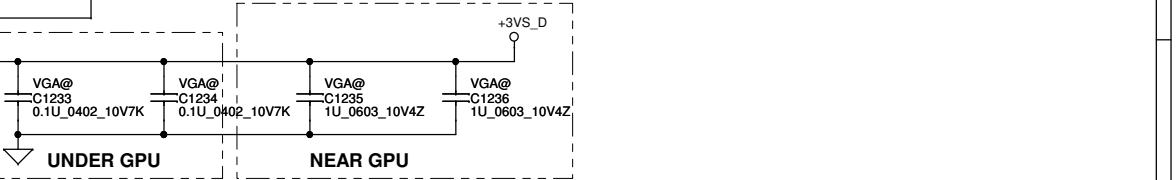
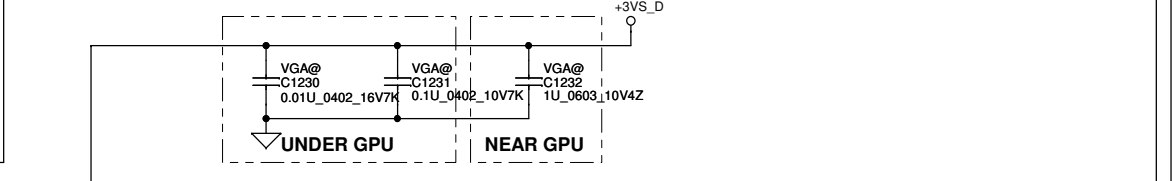
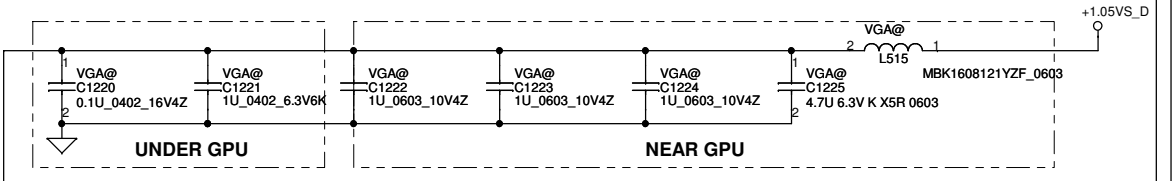
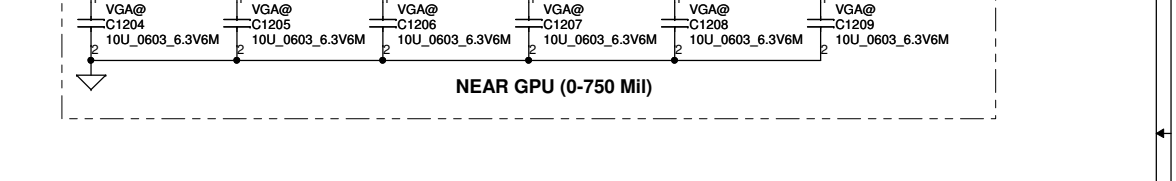
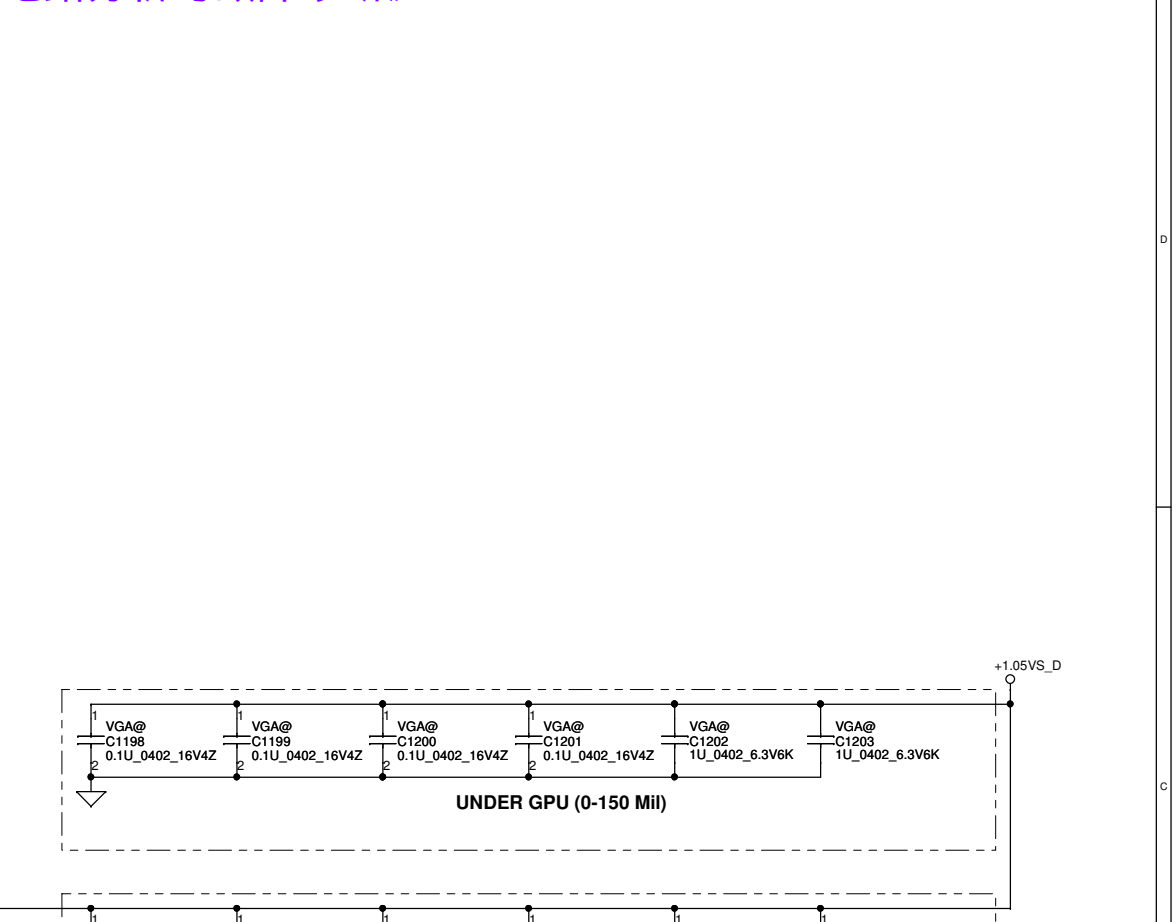
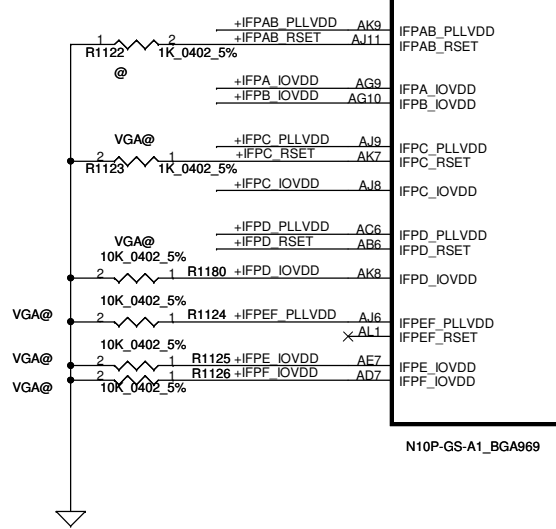
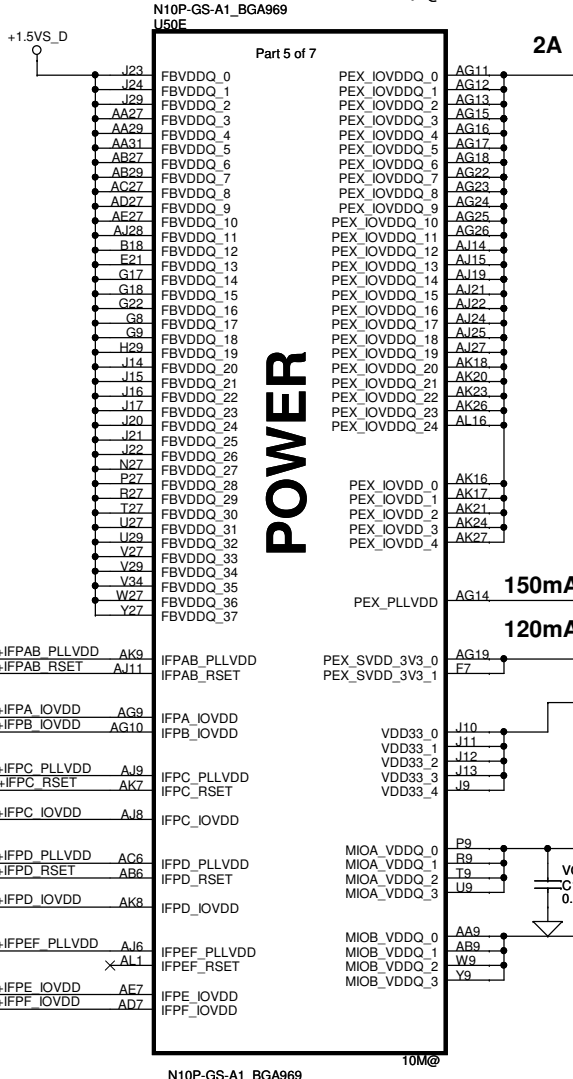
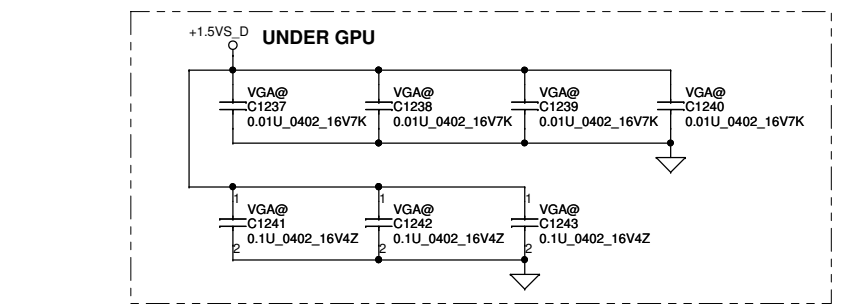
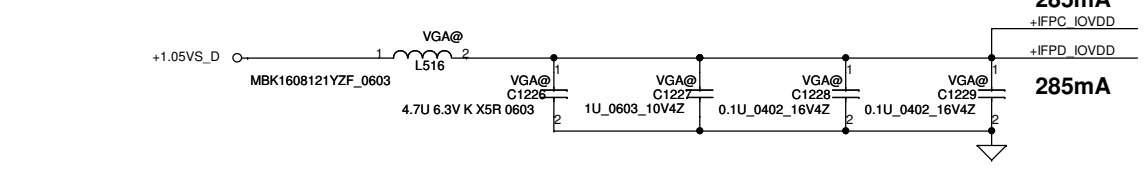
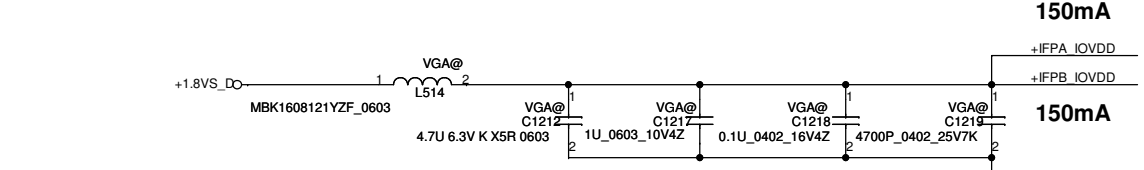
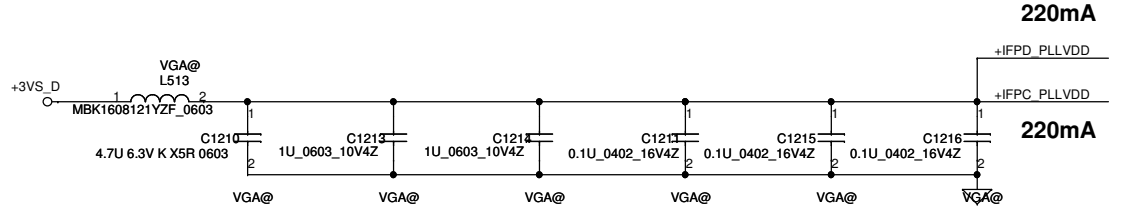
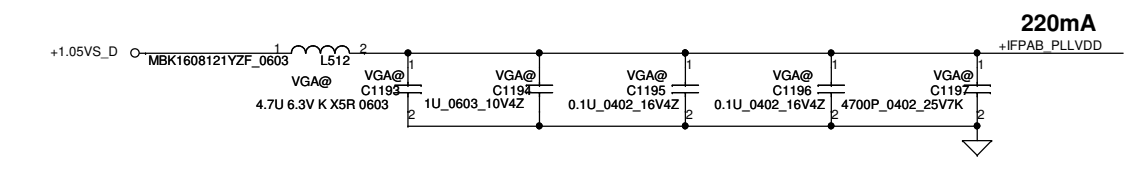
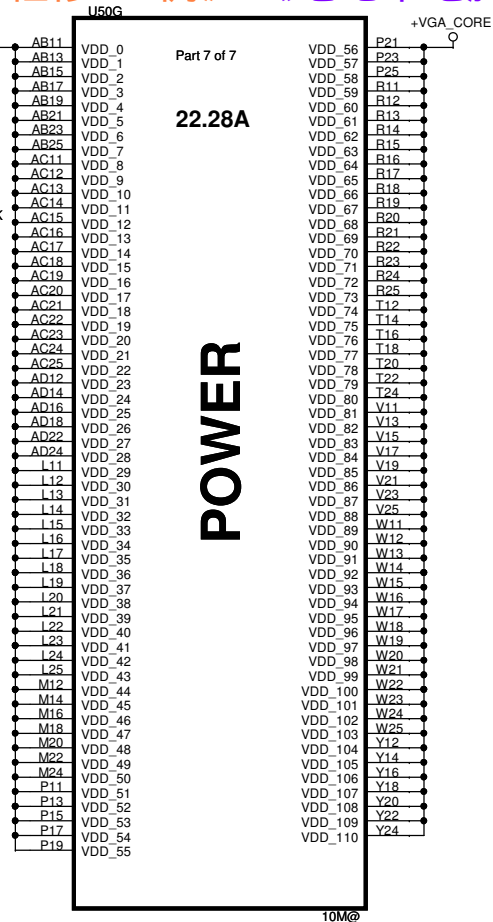
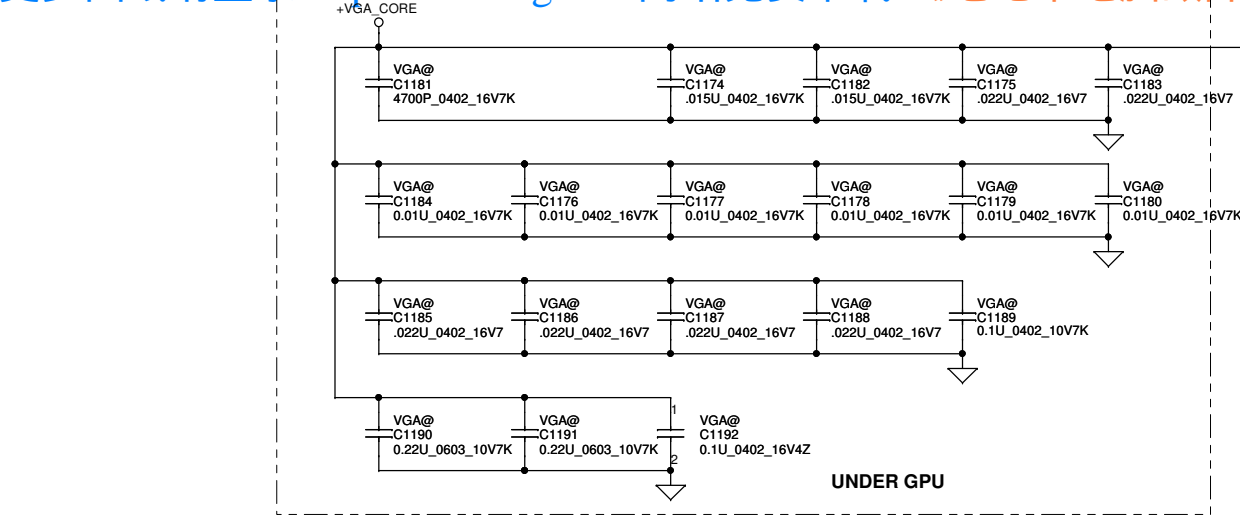
Memory/PKG	FBVDDQ	FBCAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
DDR3	+1.5VS	40.2 ohm	60.4 ohm	40.2 ohm
GDDR3	+1.8VS	40.2 ohm	60.4 ohm	40.2 ohm

Must be used 1% resistor for driver calibration

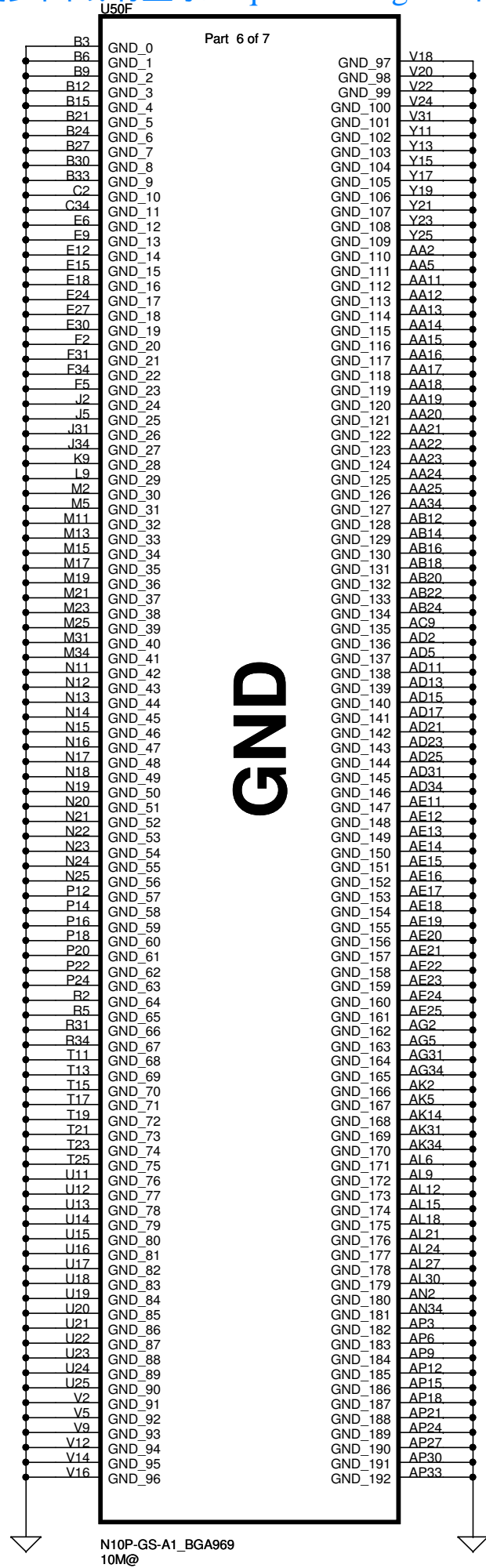
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Title
				N10x-GS Memory
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			Custom	0.1
			Document Number	
			NIWBA_LA5371P	
			Date:	Tuesday, March 24, 2009
			Sheet	20 of 52



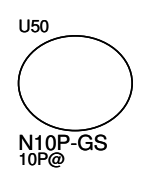
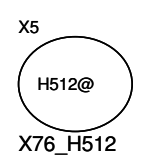
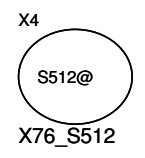
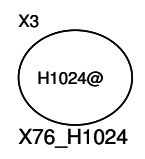
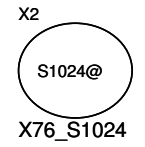
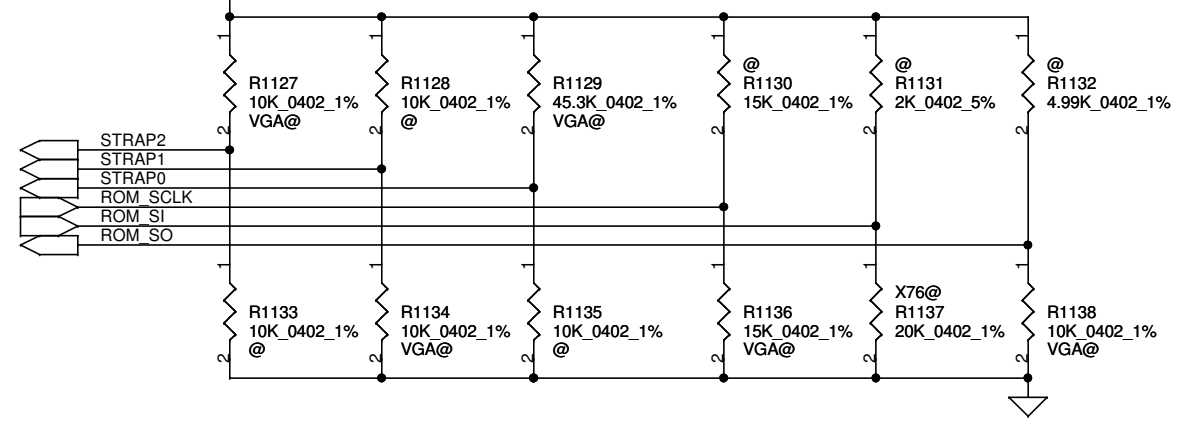
Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	Compal Electronics, Inc.
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Size	Custom	Document Number	Rev	0.1
Date: Tuesday, March 24, 2009		Sheet 21 of 52		



Security Classification	Compal Secret Data		Title Compal Electronics, Inc. N10x-GS POWER
Issued Date	2007/10/15	Deciphered Date	
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			Document Number NIWBA_LA5371P
			Rev 0.1
			Date: Tuesday, March 24, 2009
			Sheet 22 of 52



<21> STRAP2
<21> STRAP1
<21> STRAP0
<21> ROM_SCLK
<21> ROM_SI
<21> ROM_SO

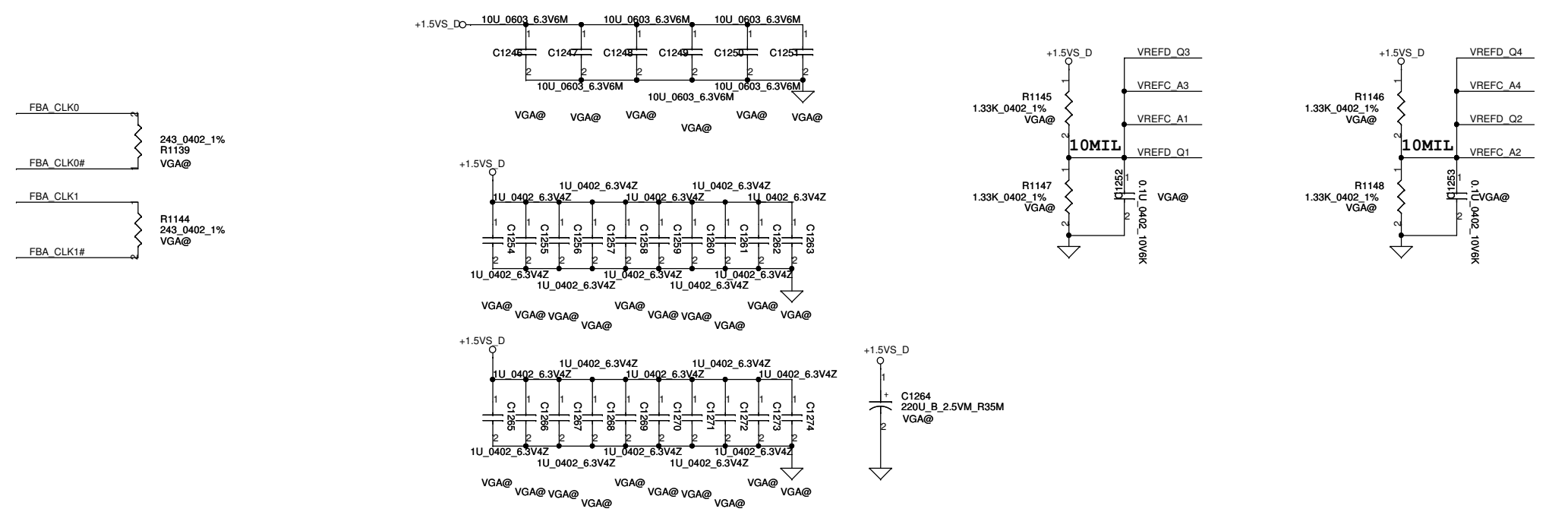
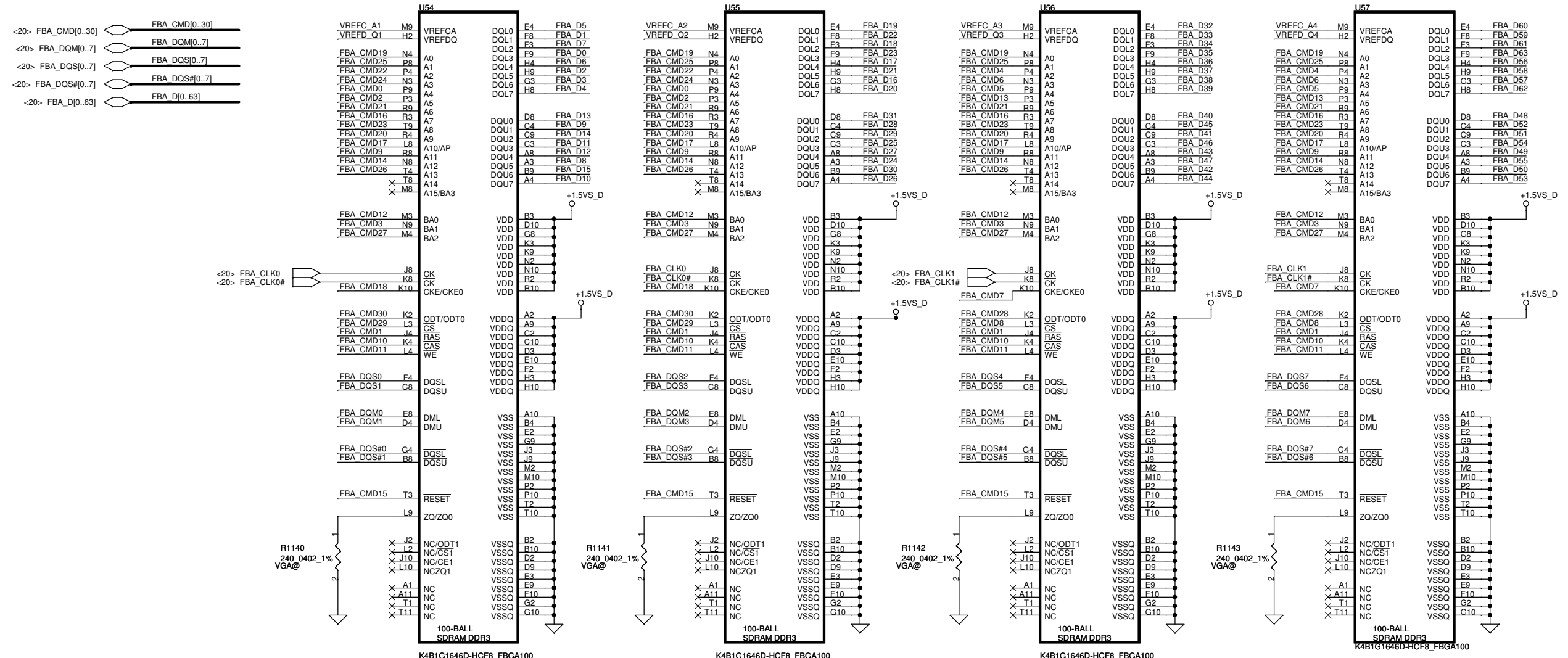


GB1 Family GPU Strap Options

GPU	FB Memory	GPU DEVID RAM_CFG GPU DEVID						
		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0	
N10P-GS (0xA34)	Samsung	64Mx16	PD 10K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K
N10M-GS (0xA74)	Samsung	64Mx16	PD 10K	PD 15K	PD 20K	PU 10K	PD 10K	PU 45K
	Hynix	64Mx16	PD 10K	PD 15K	PD 15K	PU 10K	PD 10K	PU 45K

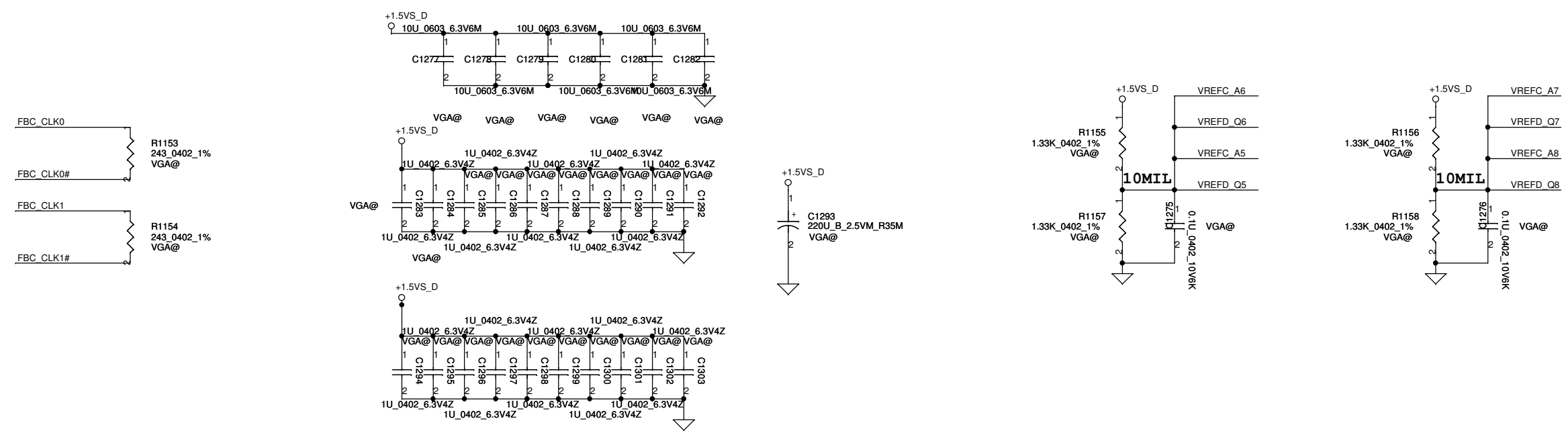
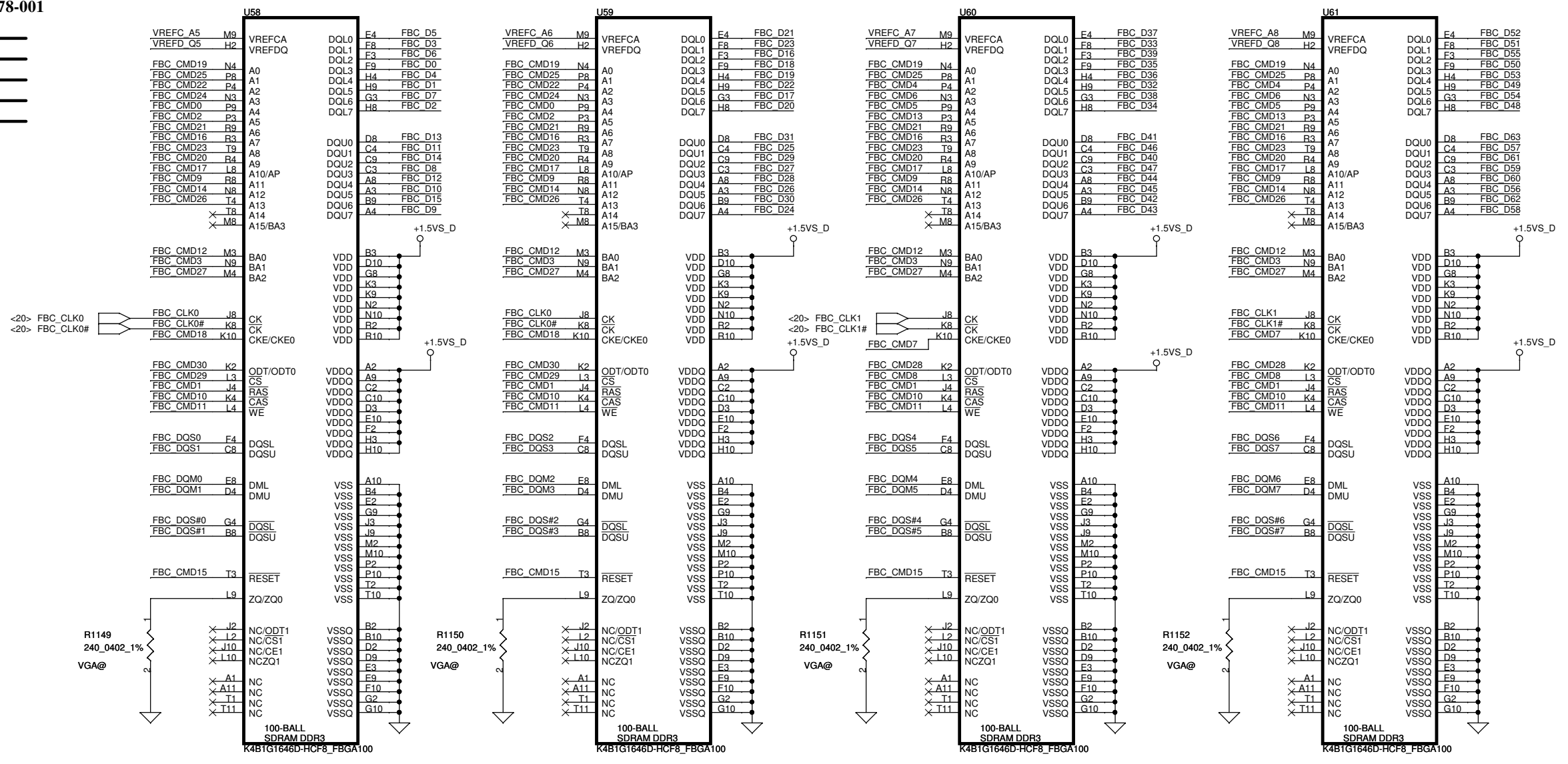
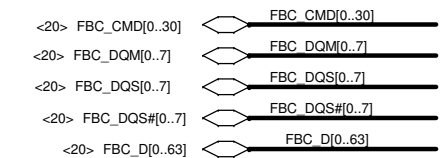
Security Classification	Compal Secret Data		Compal Electronics, Ltd.	
Issued Date	2008/03/25	Deciphered Date	2008/04/	Title
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				Size Custom
				NIWBA_LA5371P
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N10x 40nm DDR3 MAPPING
NVIDIA DOCUMENT FOR DA-3978-001



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Issued Date	2007/10/15	Deciphered Date	
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			Document Number NIWBA_LA5371P
			Rev 0.1
			Date: Tuesday, March 24, 2009
			Sheet 24 of 52

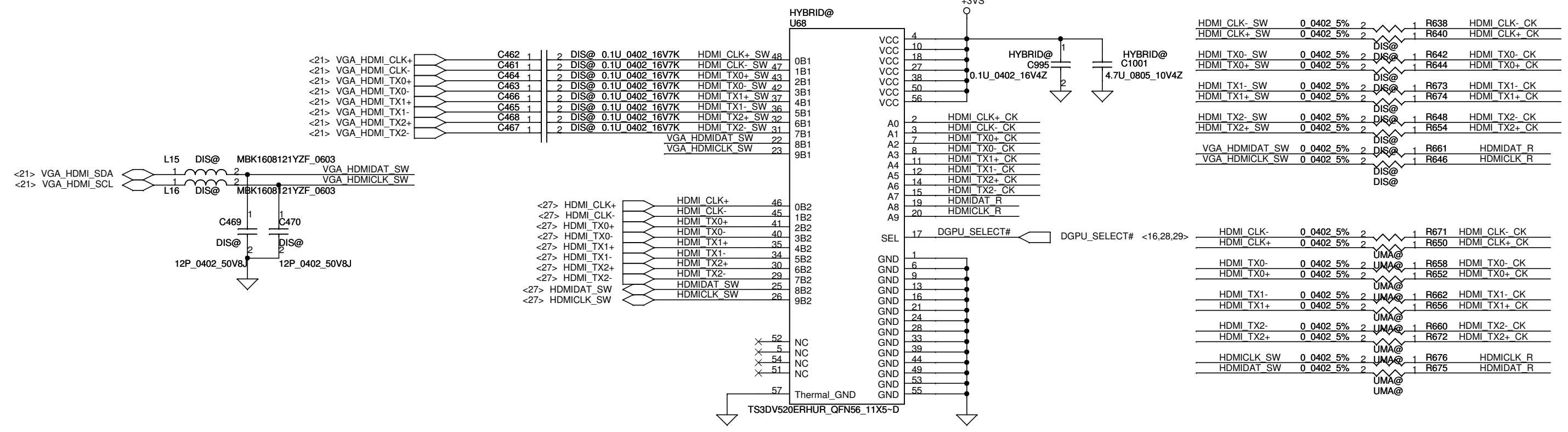
NVIDIA DOCUMENT FOR DA-3978-001



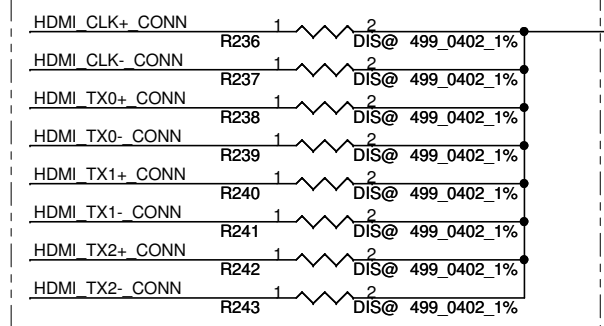
Security Classification	Compal Secret Data		Title	
Issued Date	2007/10/15	Deciphered Date	2008/10/15	VRAM DDRA
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Date: Tuesday, March 24, 2009				Sheet 25 of 52

Compal Electronics, Inc.
VRAM DDRA
 NIWBA_LA5371P
 Rev 0.1

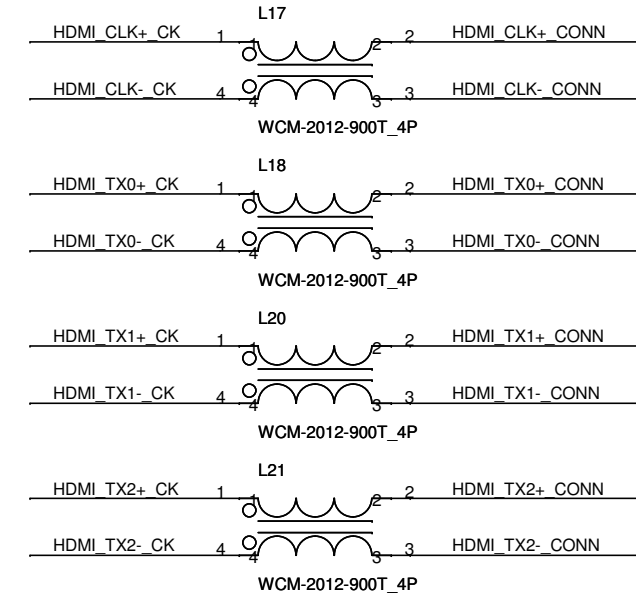
HDMI switch



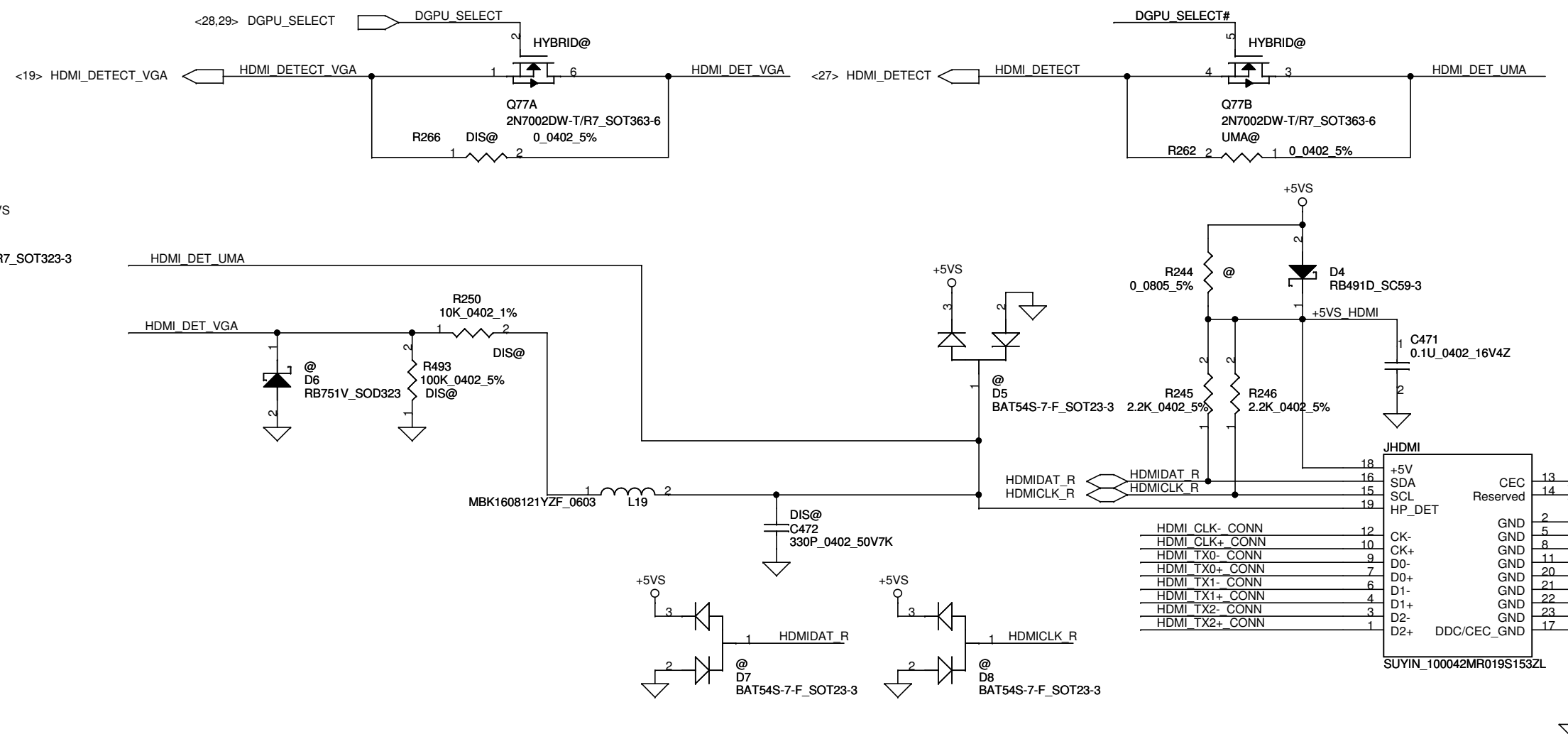
TMDS pull down (500ohm) resistors G9x only



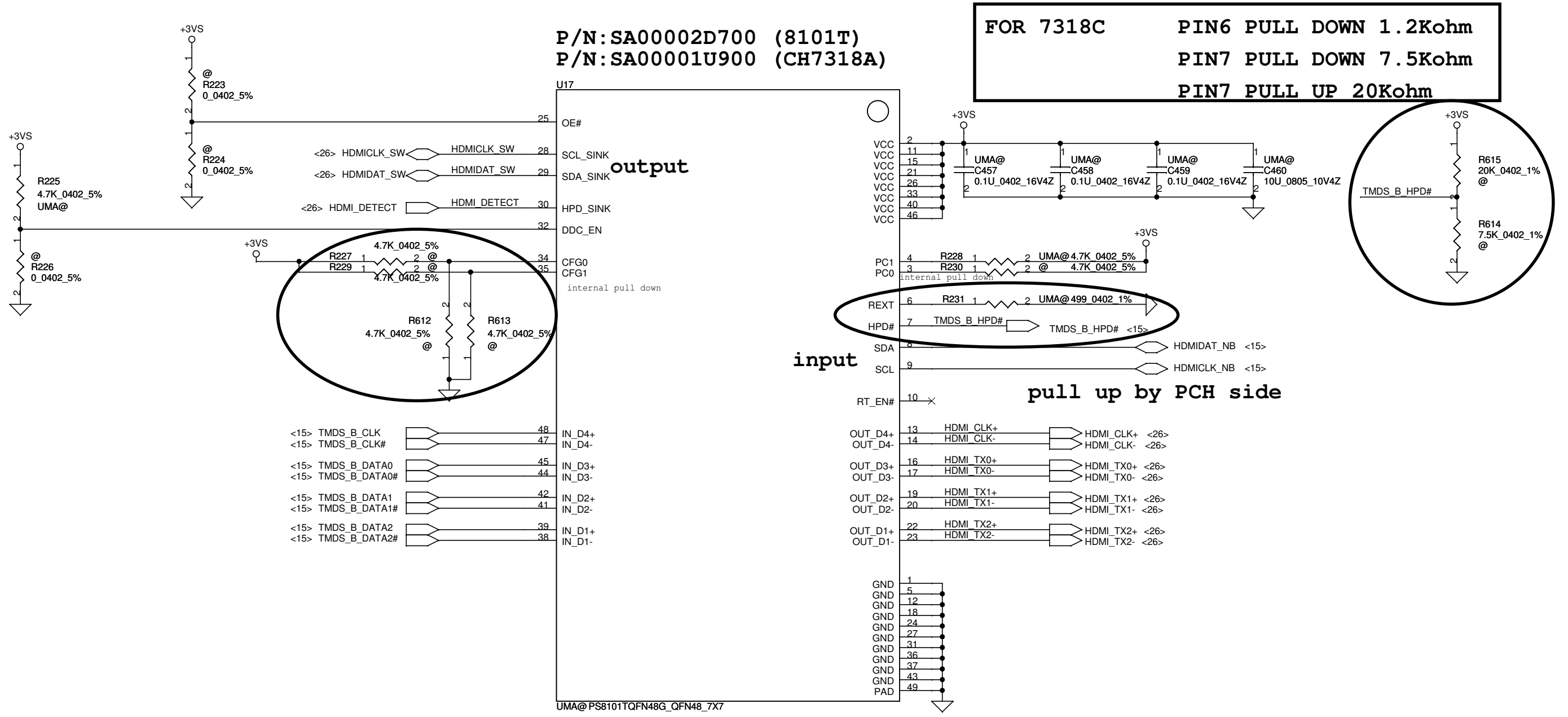
NEAR CONNECT



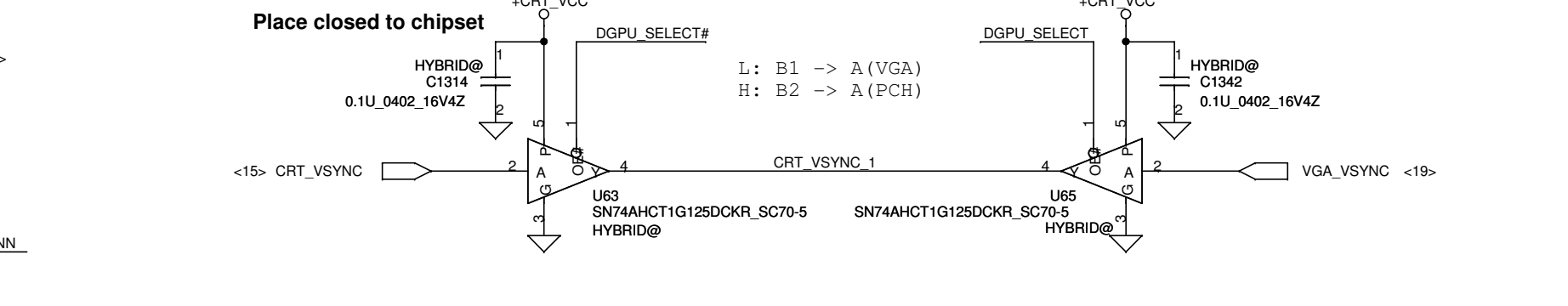
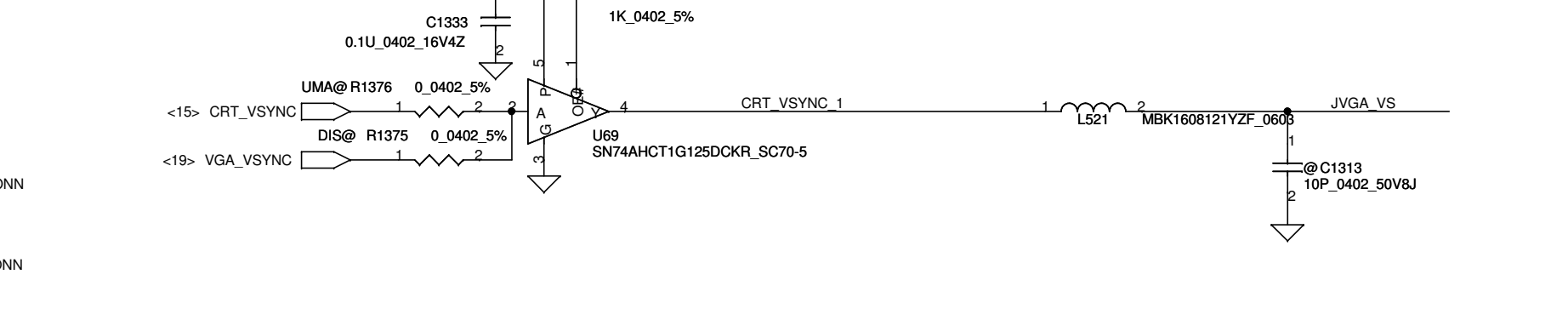
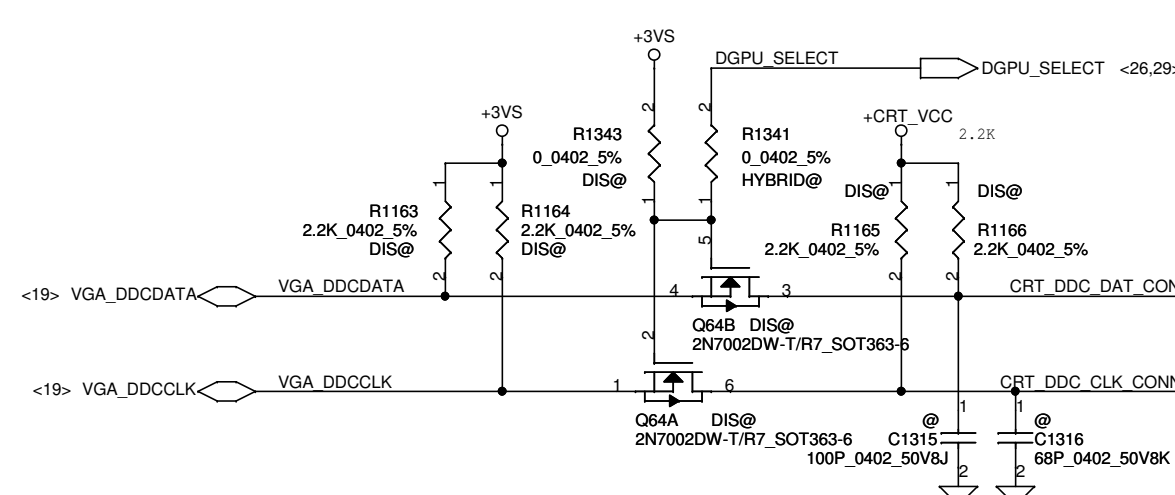
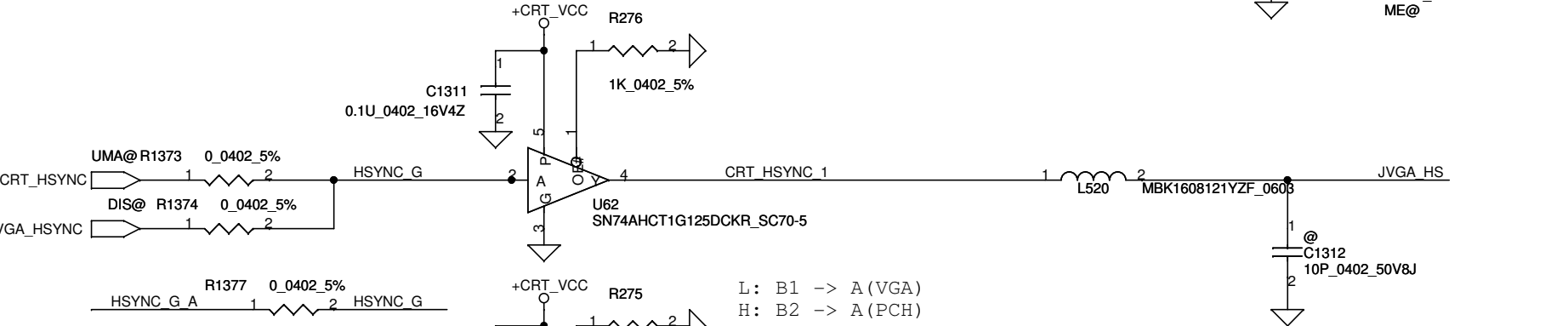
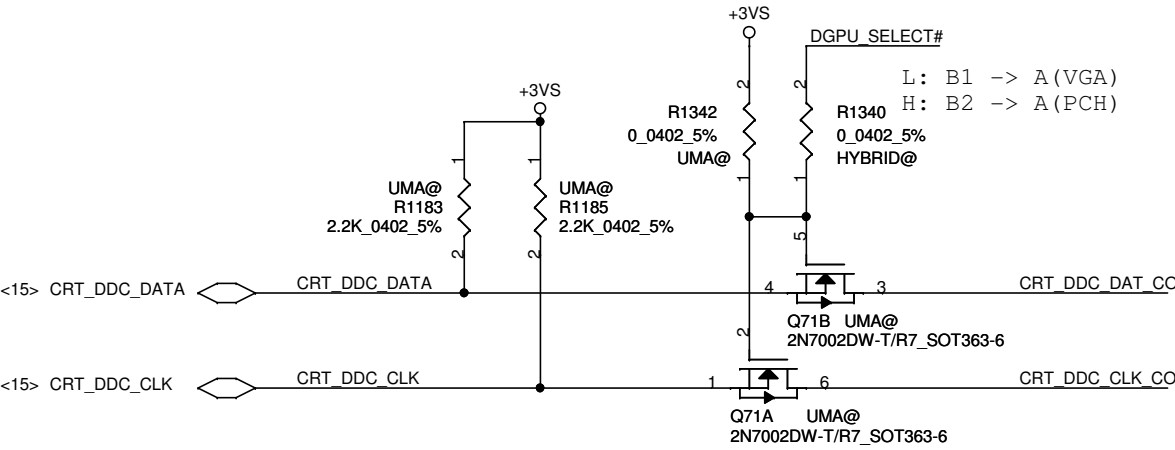
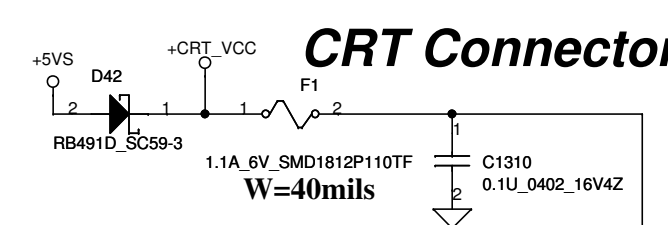
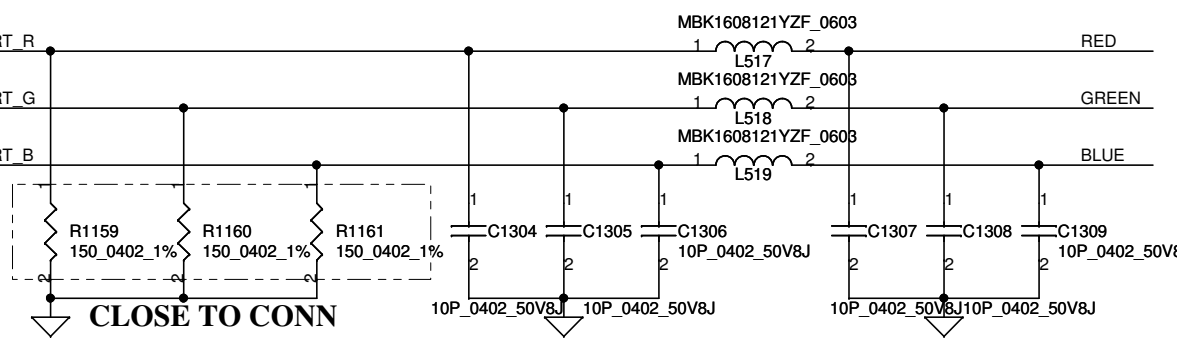
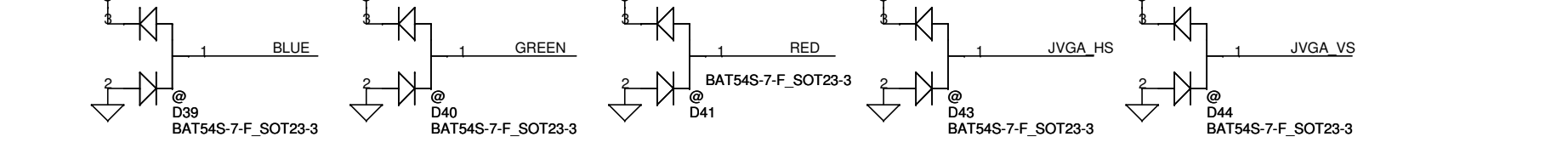
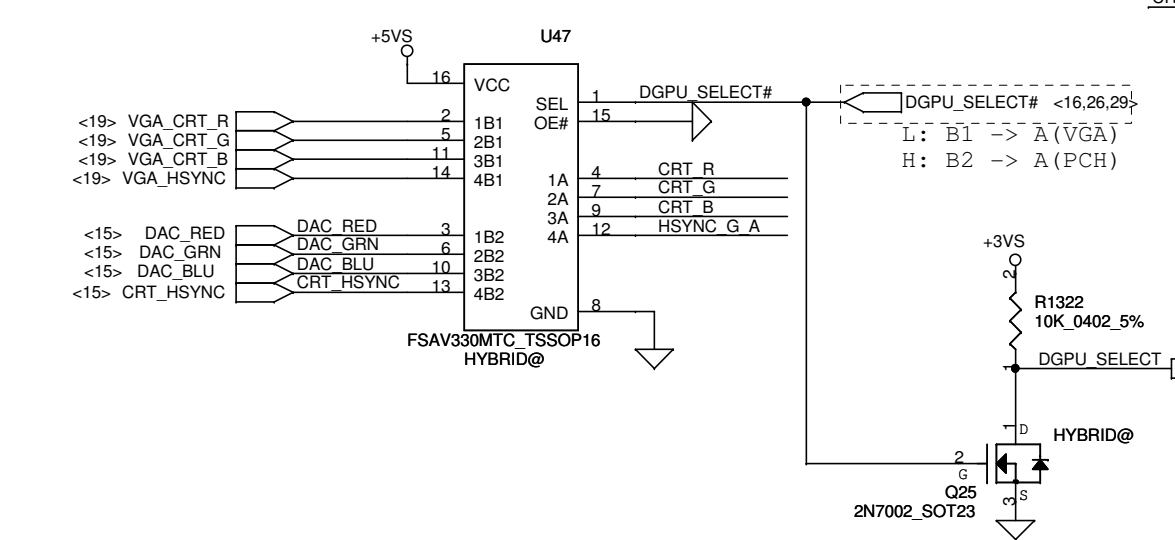
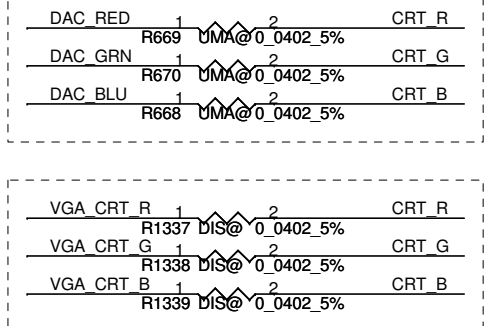
HDMI CLK+ CK	R251	1	@	2	0	0402	5%	HDMI CLK+ CONN
HDMI CLK- CK	R252	1	@	2	0	0402	5%	HDMI CLK- CONN
HDMI TX0+ CK	R253	1	@	2	0	0402	5%	HDMI TX0+ CONN
HDMI TX0- CK	R254	1	@	2	0	0402	5%	HDMI TX0- CONN
HDMI TX1+ CK	R255	1	@	2	0	0402	5%	HDMI TX1+ CONN
HDMI TX1- CK	R256	1	@	2	0	0402	5%	HDMI TX1- CONN
HDMI TX2+ CK	R257	1	@	2	0	0402	5%	HDMI TX2+ CONN
HDMI TX2- CK	R258	1	@	2	0	0402	5%	HDMI TX2- CONN



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Size	Custom	Document Number	Rev	0.1
		KIWB1/B2_LA4601P		
Date:	Tuesday, March 24, 2009	Sheet	26	of 52

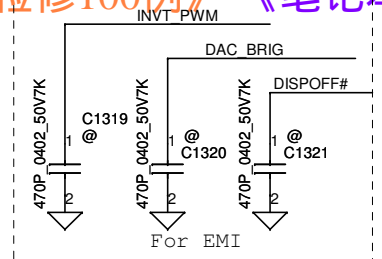
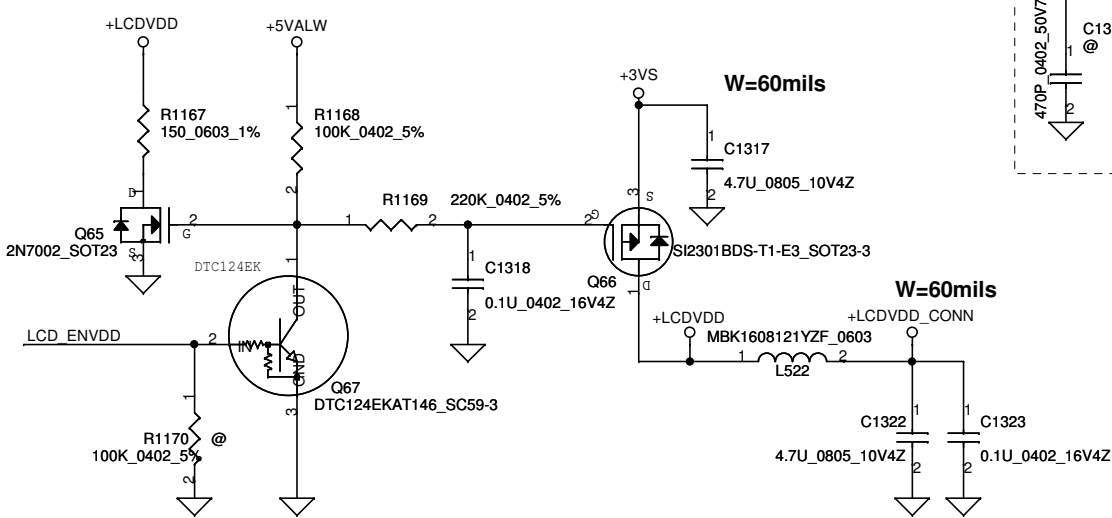


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Issued Date	2008/03/25	Deciphered Date	2008/04/	Title Level Shifter_PS8101T
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				Document Number KIWB1/B2_LA4601P
Date: Tuesday, March 24, 2009			Sheet 27 of 52	

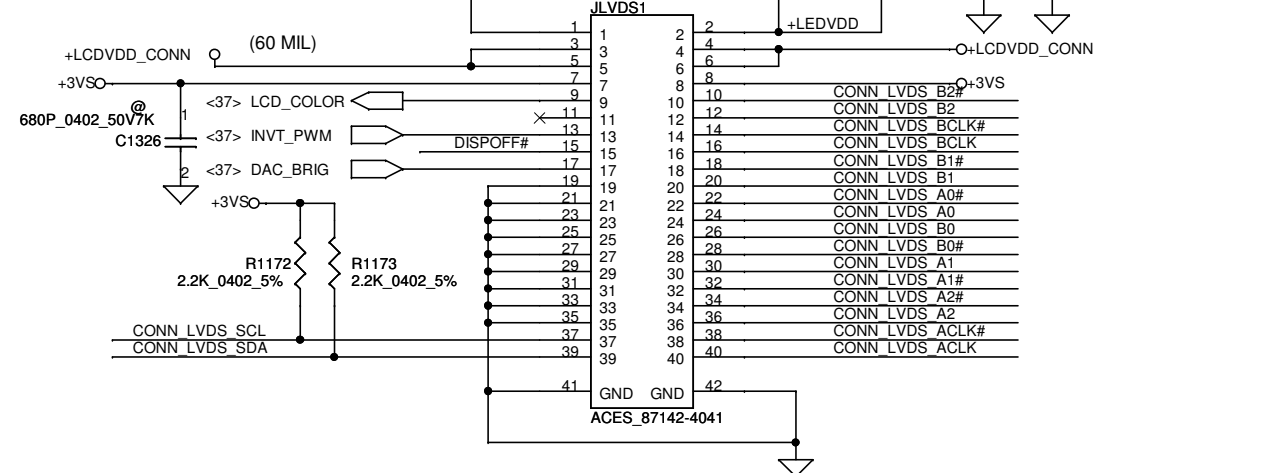


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Size	Document Number	Rev		
Custom	NIWBA_LA5371P	0.1		
Date:	Tuesday, March 24, 2009	Sheet	28 of 52	

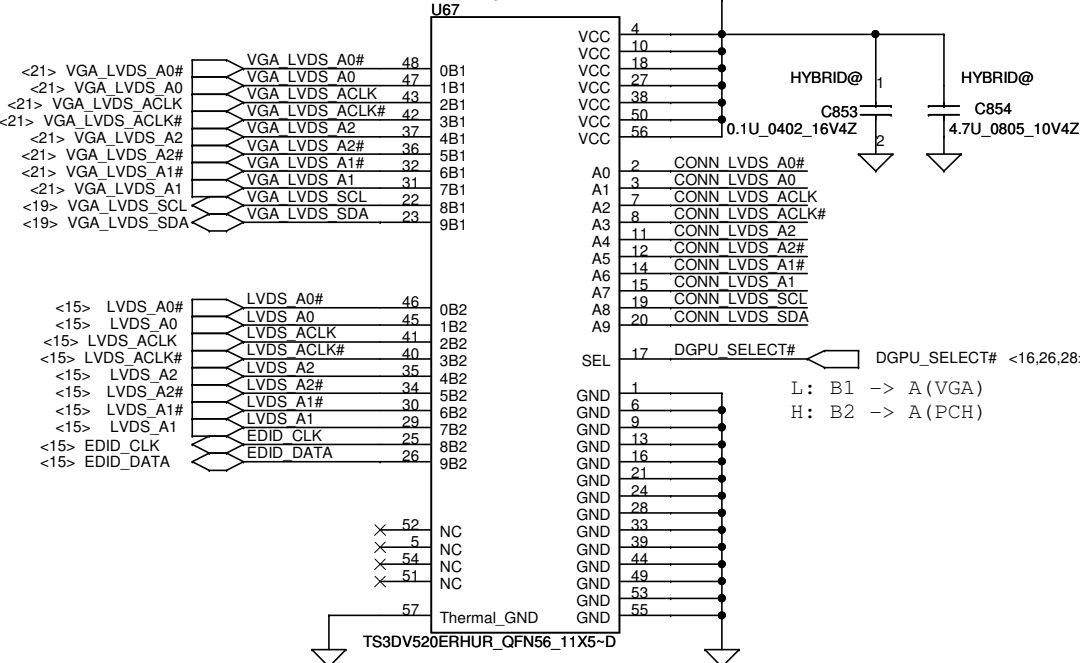
LCD POWER CIRCUIT



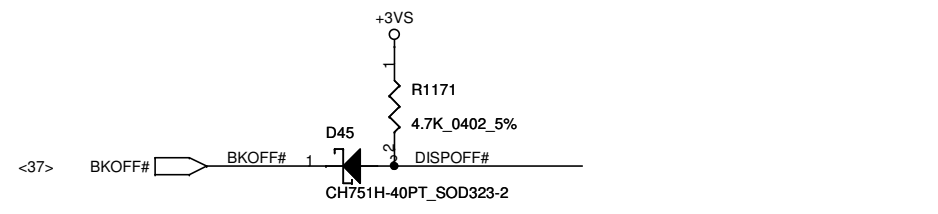
VGA LCD/PANEL BD. Conn.



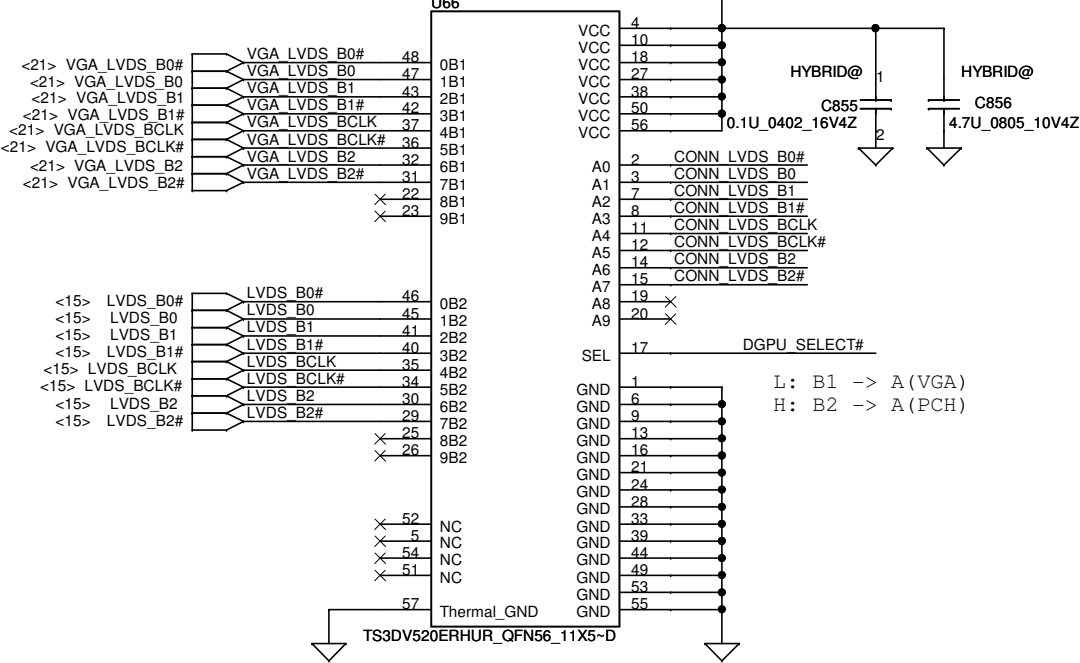
LVDS switch1



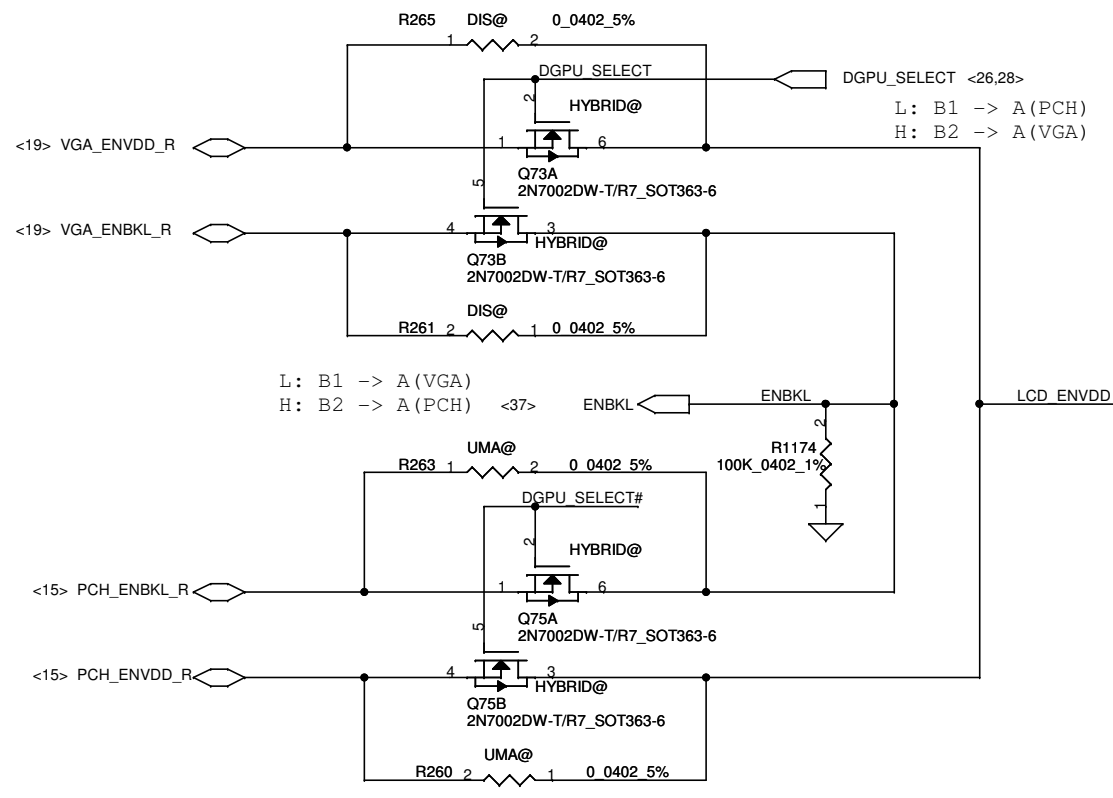
VGA LVDS SCL	0	0402_5%	2	DIS@	1	R1360	CONN LVDS SCL
VGA LVDS SDA	0	0402_5%	2	DIS@	1	R1361	CONN LVDS SDA
VGA LVDS A0	0	0402_5%	2	DIS@	1	R1344	CONN LVDS A0
VGA LVDS A0#	0	0402_5%	2	DIS@	1	R1345	CONN LVDS A0#
VGA LVDS A1	0	0402_5%	2	DIS@	1	R1358	CONN LVDS A1
VGA LVDS A1#	0	0402_5%	2	DIS@	1	R1359	CONN LVDS A1#
VGA LVDS A2	0	0402_5%	2	DIS@	1	R1346	CONN LVDS A2
VGA LVDS A2#	0	0402_5%	2	DIS@	1	R1348	CONN LVDS A2#
VGA LVDS ACLK	0	0402_5%	2	DIS@	1	R1355	CONN LVDS ACLK
VGA LVDS ACLK#	0	0402_5%	2	DIS@	1	R1347	CONN LVDS ACLK#
VGA LVDS B0	0	0402_5%	2	DIS@	1	R1356	CONN LVDS B0
VGA LVDS B0#	0	0402_5%	2	DIS@	1	R1349	CONN LVDS B0#
VGA LVDS B1	0	0402_5%	2	DIS@	1	R1350	CONN LVDS B1
VGA LVDS B1#	0	0402_5%	2	DIS@	1	R1351	CONN LVDS B1#
VGA LVDS B2	0	0402_5%	2	DIS@	1	R1352	CONN LVDS B2
VGA LVDS B2#	0	0402_5%	2	DIS@	1	R1353	CONN LVDS B2#
VGA LVDS BCLK	0	0402_5%	2	DIS@	1	R1354	CONN LVDS BCLK
VGA LVDS BCLK#	0	0402_5%	2	DIS@	1	R1357	CONN LVDS BCLK#



LVDS switch2



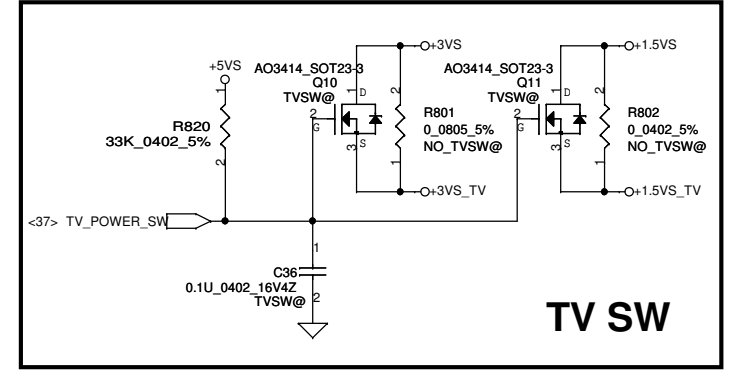
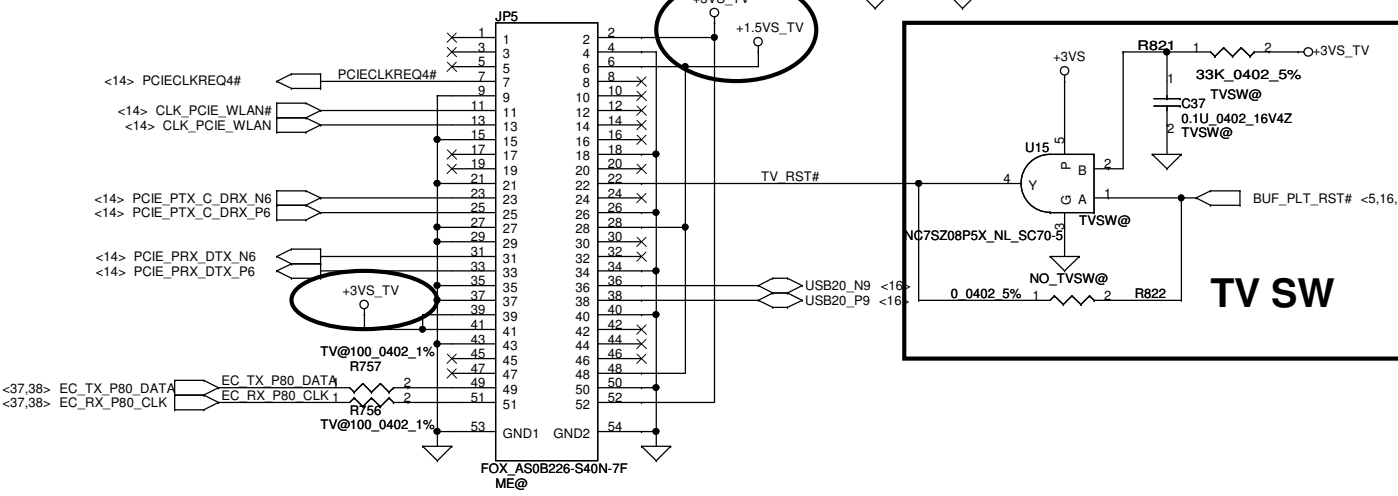
EDID CLK	0	0402_5%	2	UMA@	1	R630	CONN LVDS SCL
EDID DATA	0	0402_5%	2	UMA@	1	R636	CONN LVDS SDA
LVDS A0	0	0402_5%	2	UMA@	1	R629	CONN LVDS A0
LVDS A0#	0	0402_5%	2	UMA@	1	R633	CONN LVDS A0#
LVDS A1	0	0402_5%	2	UMA@	1	R634	CONN LVDS A1
LVDS A1#	0	0402_5%	2	UMA@	1	R635	CONN LVDS A1#
LVDS A2	0	0402_5%	2	UMA@	1	R637	CONN LVDS A2
LVDS A2#	0	0402_5%	2	UMA@	1	R639	CONN LVDS A2#
LVDS ACLK	0	0402_5%	2	UMA@	1	R641	CONN LVDS ACLK
LVDS ACLK#	0	0402_5%	2	UMA@	1	R643	CONN LVDS ACLK#
LVDS B0	0	0402_5%	2	UMA@	1	R645	CONN LVDS B0
LVDS B0#	0	0402_5%	2	UMA@	1	R647	CONN LVDS B0#
LVDS B1	0	0402_5%	2	UMA@	1	R649	CONN LVDS B1
LVDS B1#	0	0402_5%	2	UMA@	1	R651	CONN LVDS B1#
LVDS B2	0	0402_5%	2	UMA@	1	R653	CONN LVDS B2
LVDS B2#	0	0402_5%	2	UMA@	1	R655	CONN LVDS B2#
LVDS BCLK	0	0402_5%	2	UMA@	1	R657	CONN LVDS BCLK
LVDS BCLK#	0	0402_5%	2	UMA@	1	R659	CONN LVDS BCLK#



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Date: Tuesday, March 24, 2009		Sheet 29 of 52		Size B Document Number Rev 0.1	

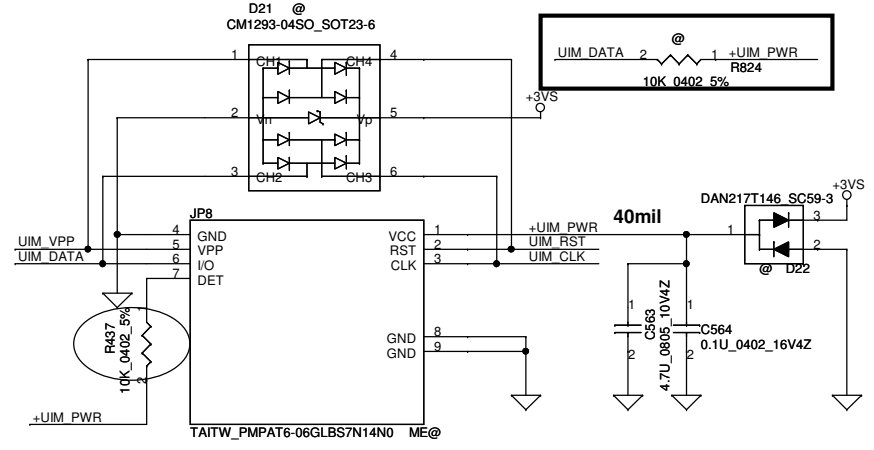
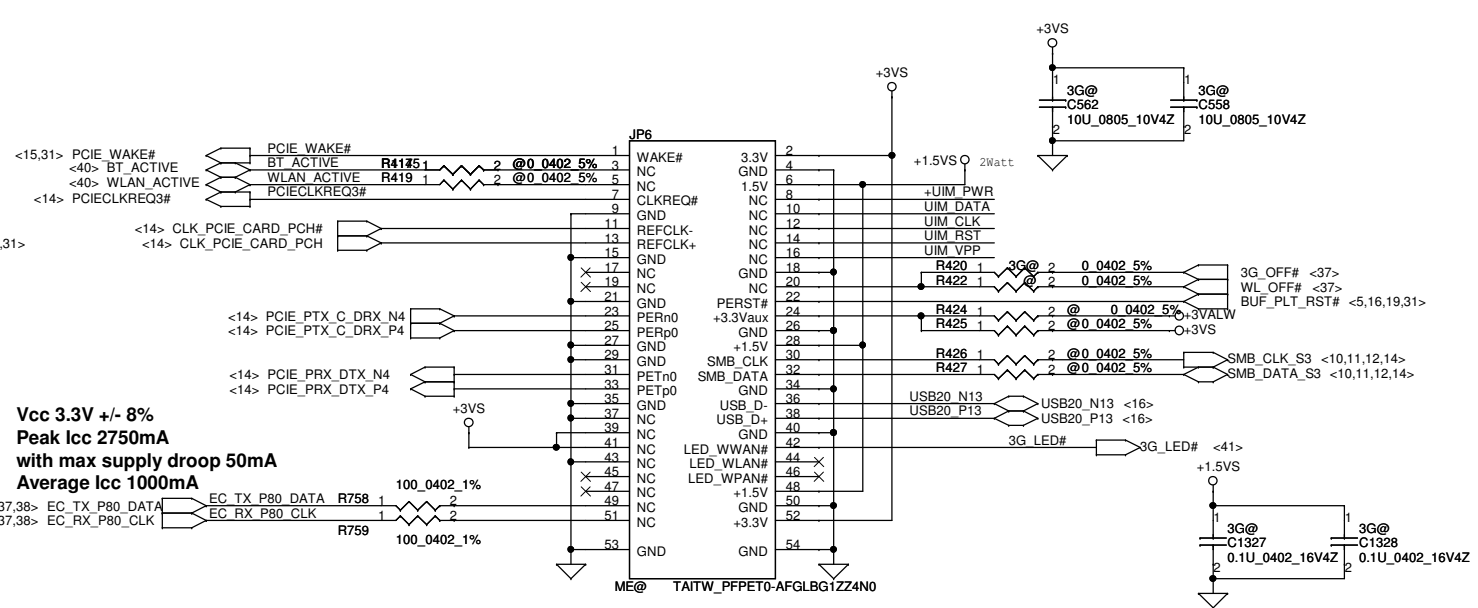
Mini-Express Card for WLAN

Mini-Express Card(Slot 1-TV TUNNER) 4.0mm high

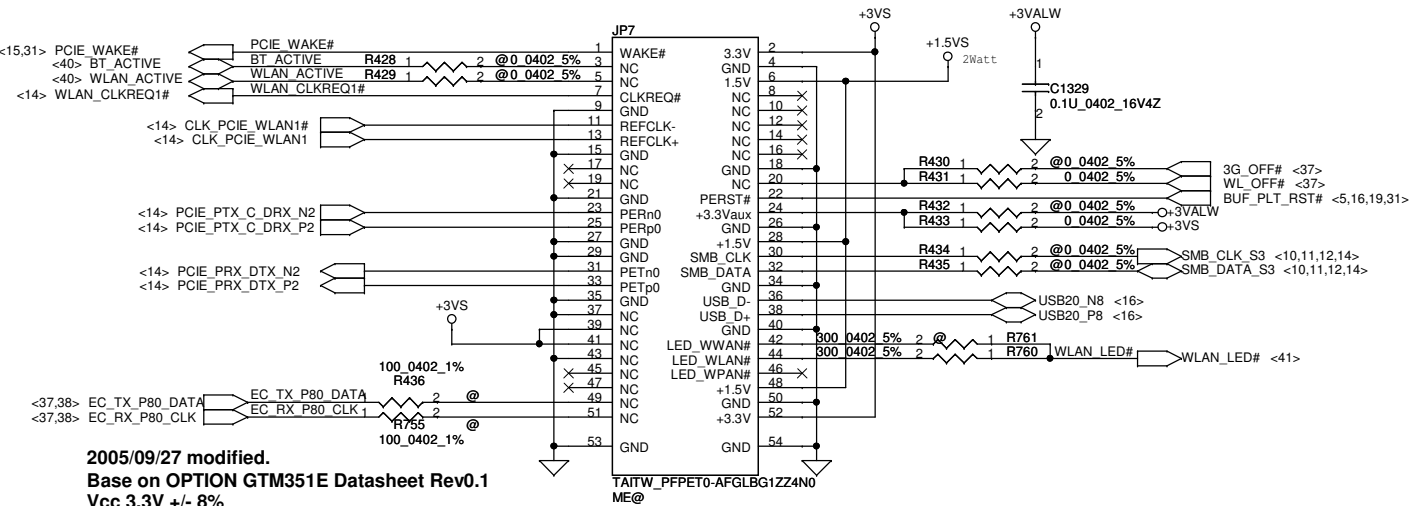


Mini-Express Card(Slot 3-WWAN 3G)

5.6mm high

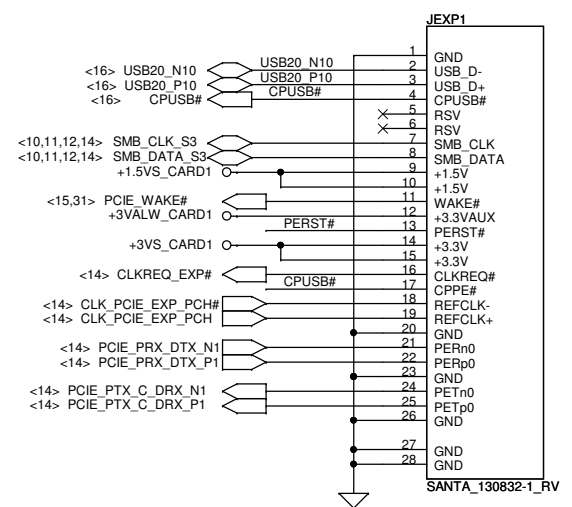


Mini-Express Card(Slot 2-WIRELESS) 5.6mm high

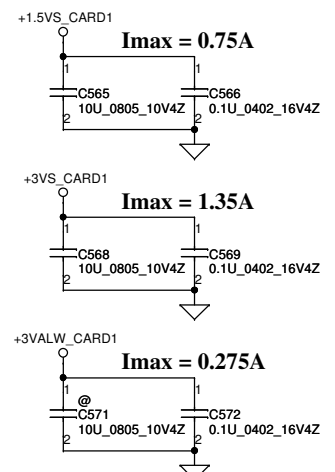
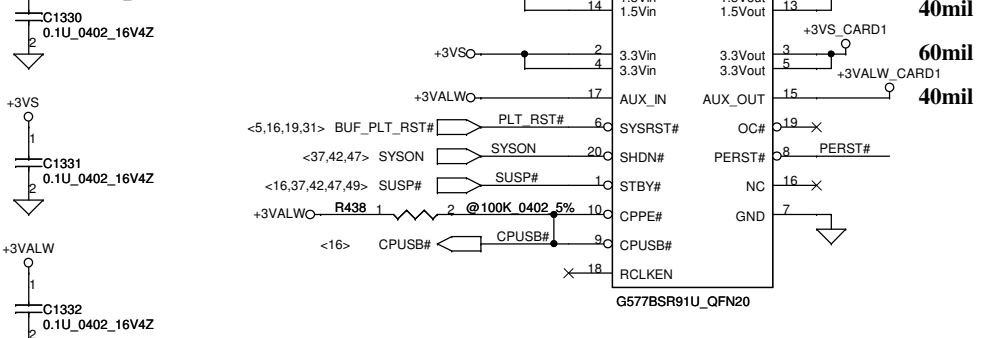


2005/09/27 modified.
Base on OPTION GTM351E Datasheet Rev0.1
Vcc 3.3V +/- 8%
Peak Icc 2750mA
with max supply droop 50mA
Average Icc 1000mA

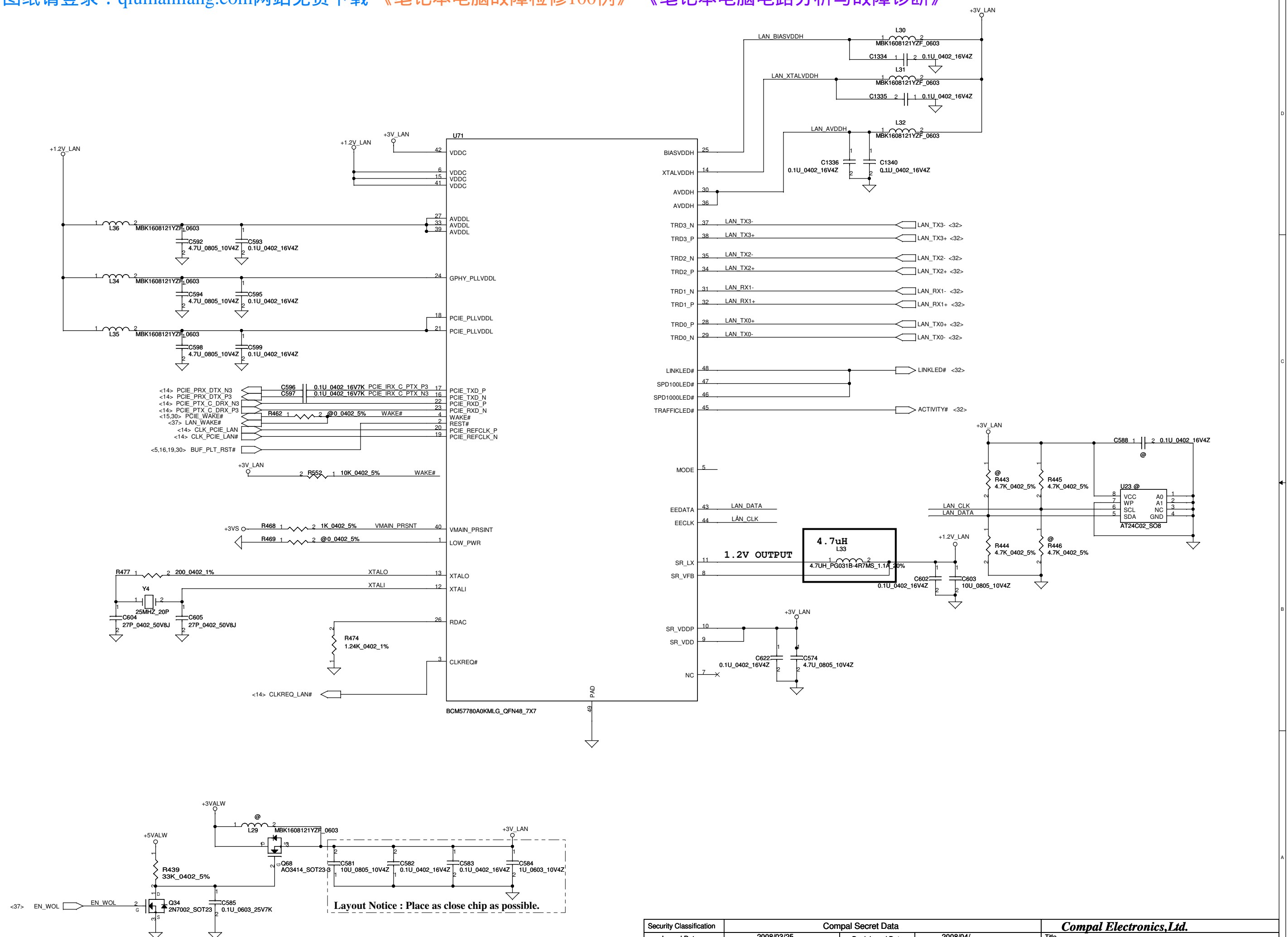
New Card 34mm Socket (Left/TOP)



Express Card Power Switch

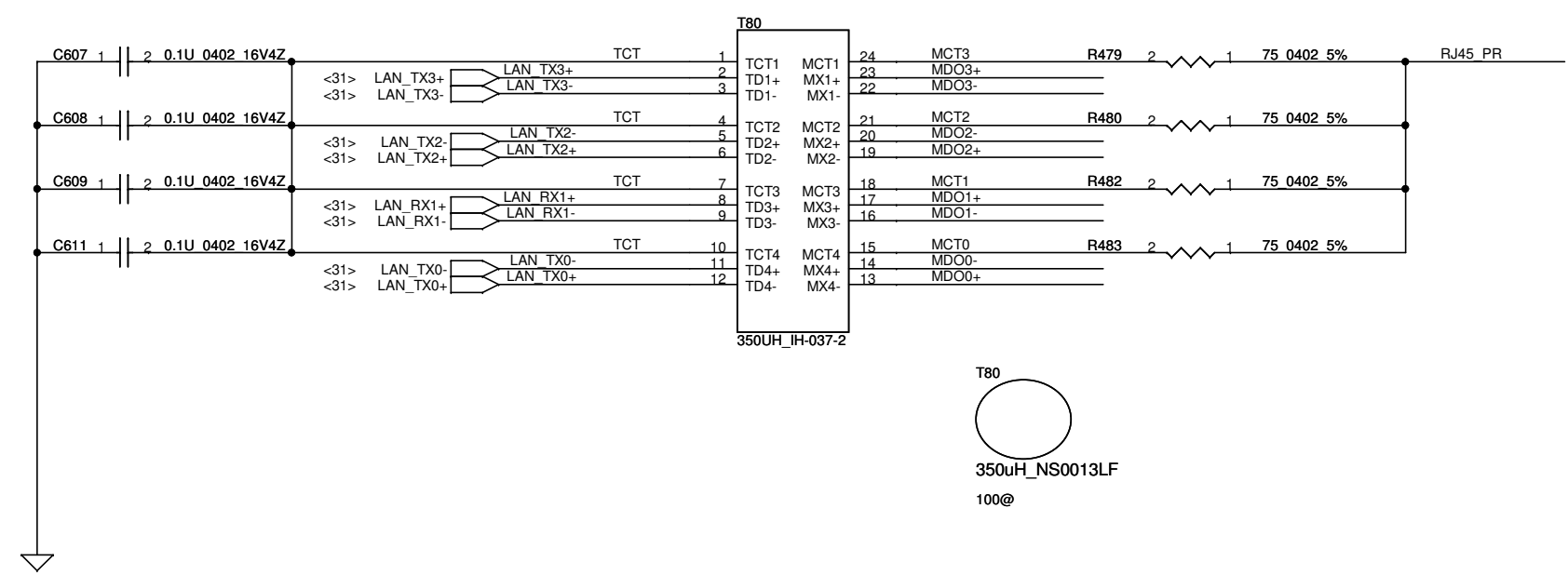


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Issued Date	2007/10/15	Deciphered Date	
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Size	Document Number	Rev	
	NIWBA_LA5371P	0.1	
Date:	Tuesday, March 24, 2009	Sheet	30 of 52

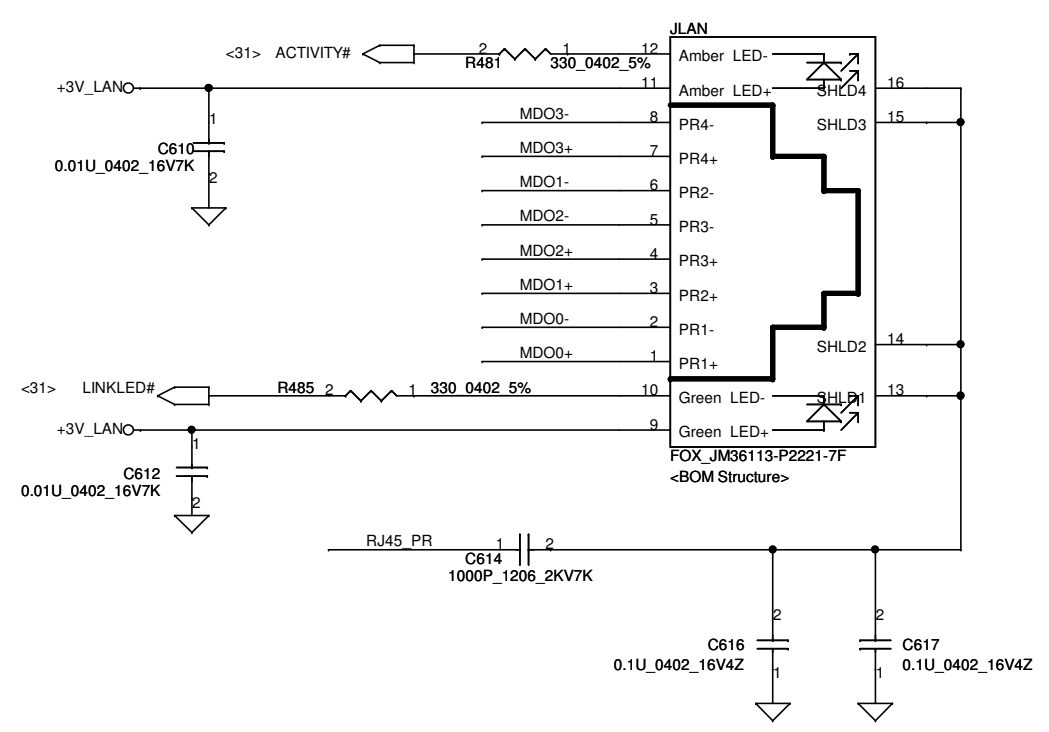


Layout Notice : Place as close chip as possible.

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Issued Date	2008/03/25	Deciphered Date	
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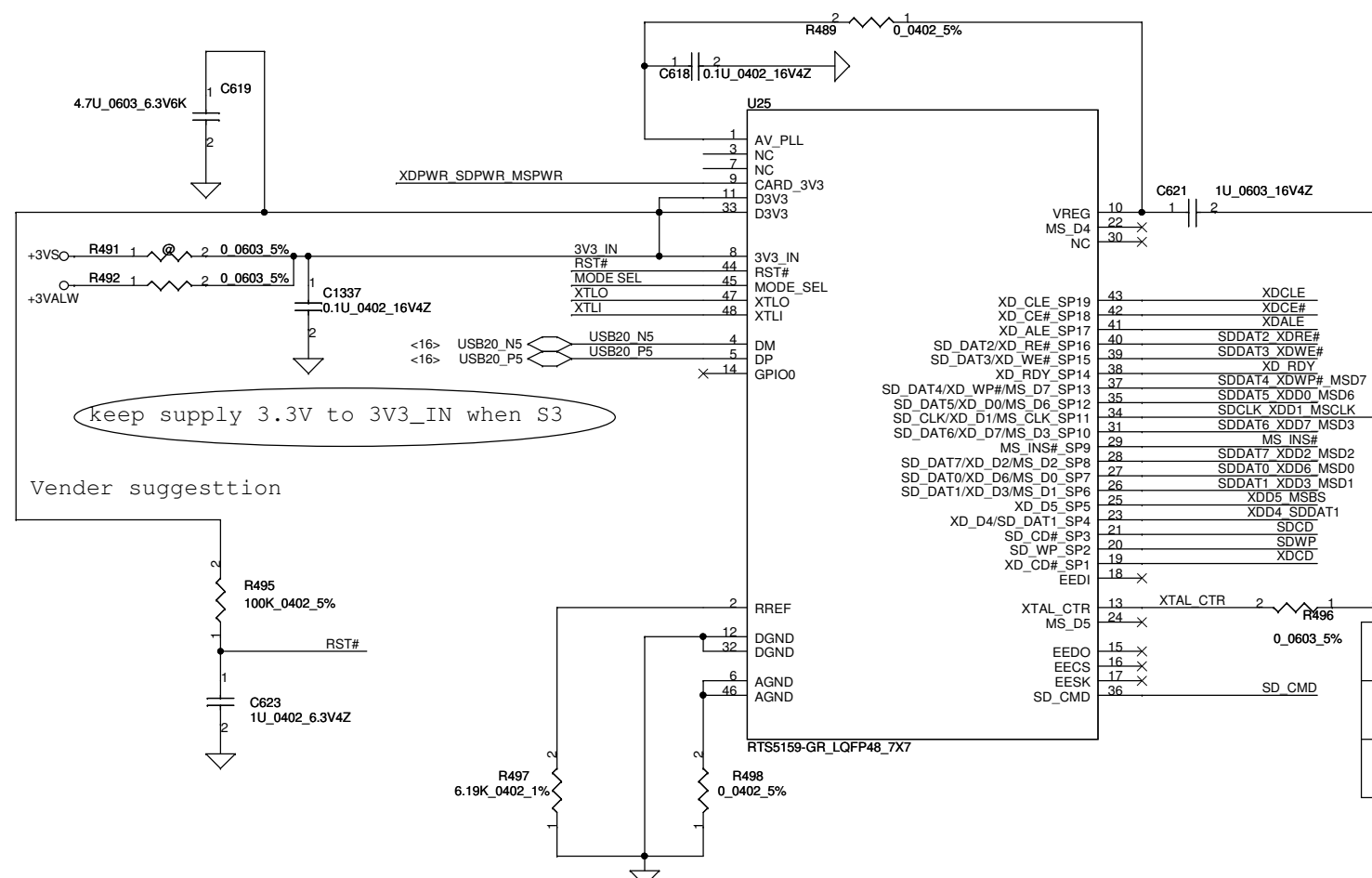


RJ11+RJ45 CONN

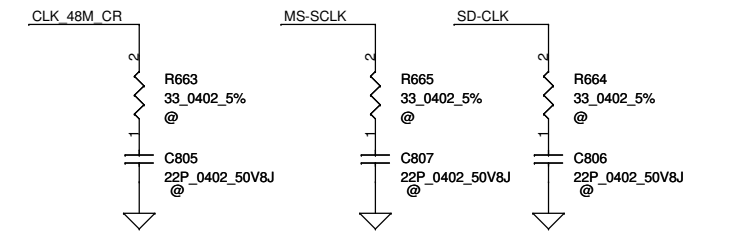
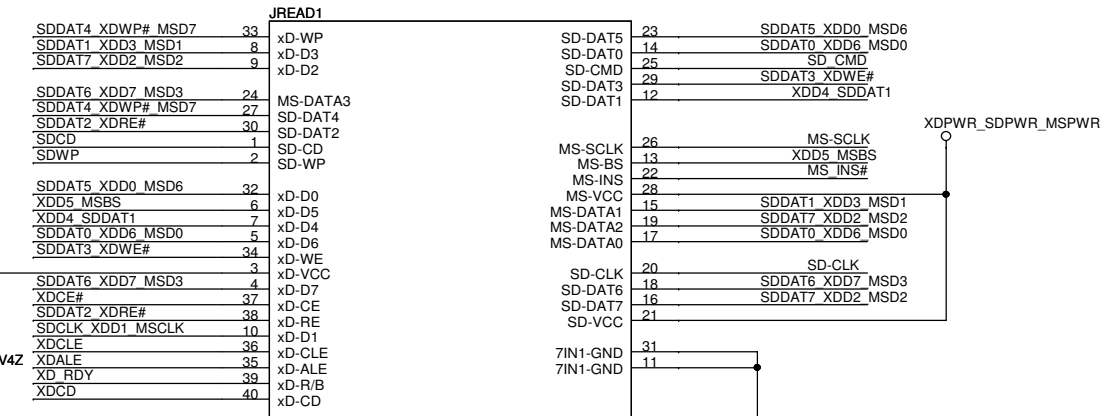


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				Rev	
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0513 : CARD_3V3 旁路电阻 100K change to 4.7u CAP==>預留
 0521 : change C79 form 4.7u to 0.1u, add R47 100K ohm, change C526 form 1u to 4.7u

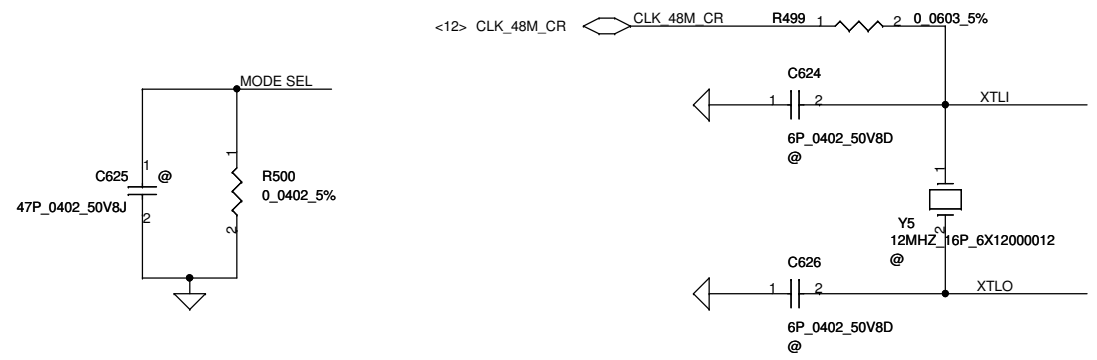


pin 13 (XTAL CTL)	CLOCK SOURCE	REMARK
FLOATING	12MHZ CRYSTAL INPUT	
PULL HIGH	CLOCK GENERATOR'S 48MHZ INPUT	INPUT TO PIN48

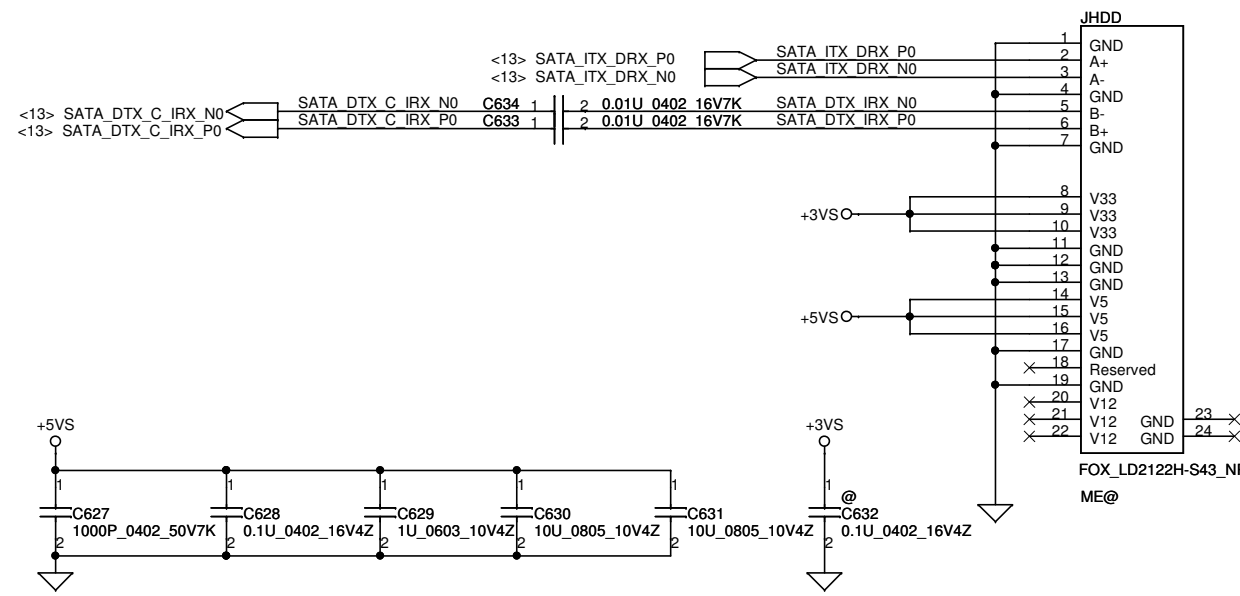


MSCLK and SDCLK 該二電阻是預留給EMI solution使用, (但請靠近RTS5158E側).

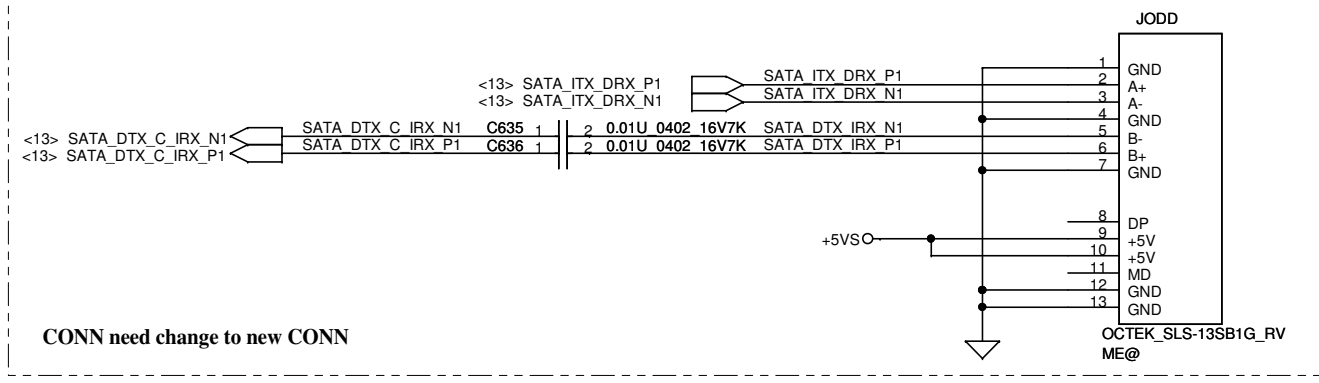
將SD_DAT1 連接到RTS5158E的pin23



SATA HDD Conn.

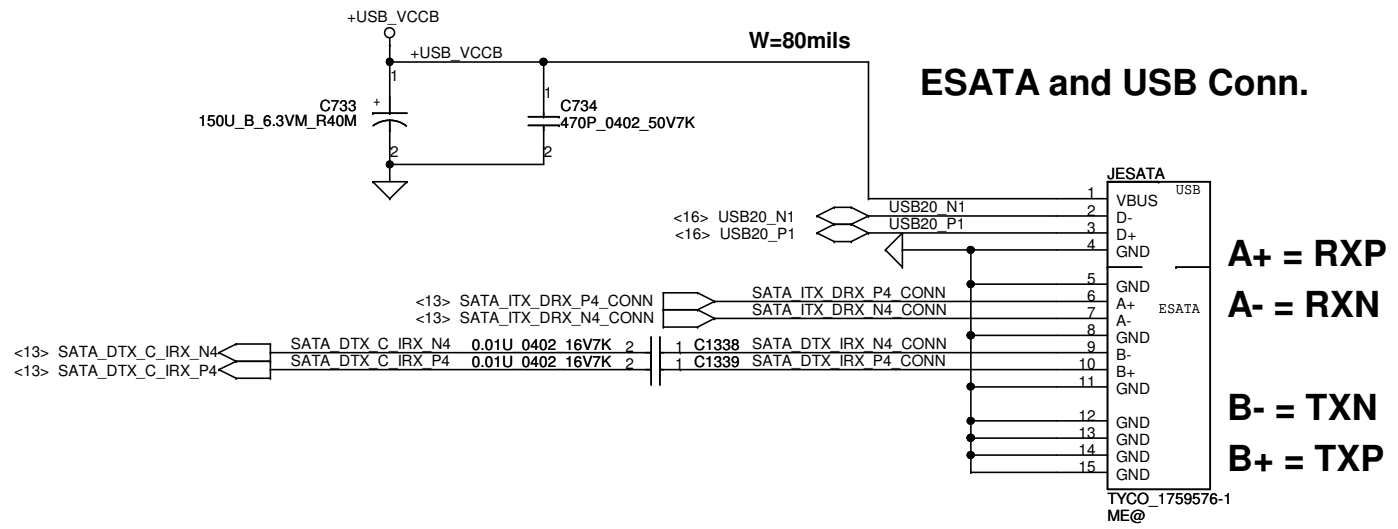


SATA ODD Conn.

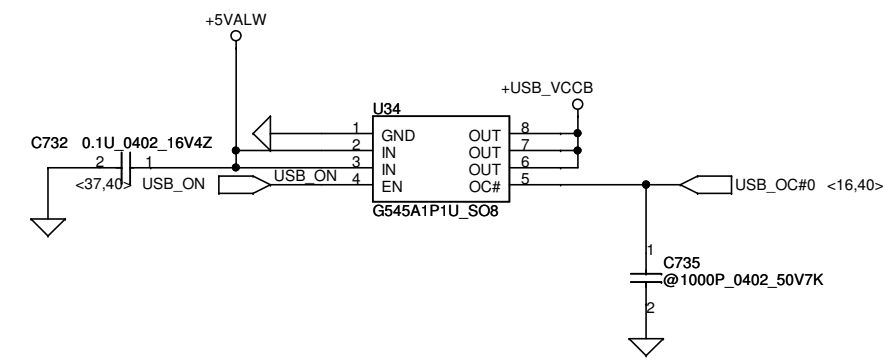


CONN need change to new CONN

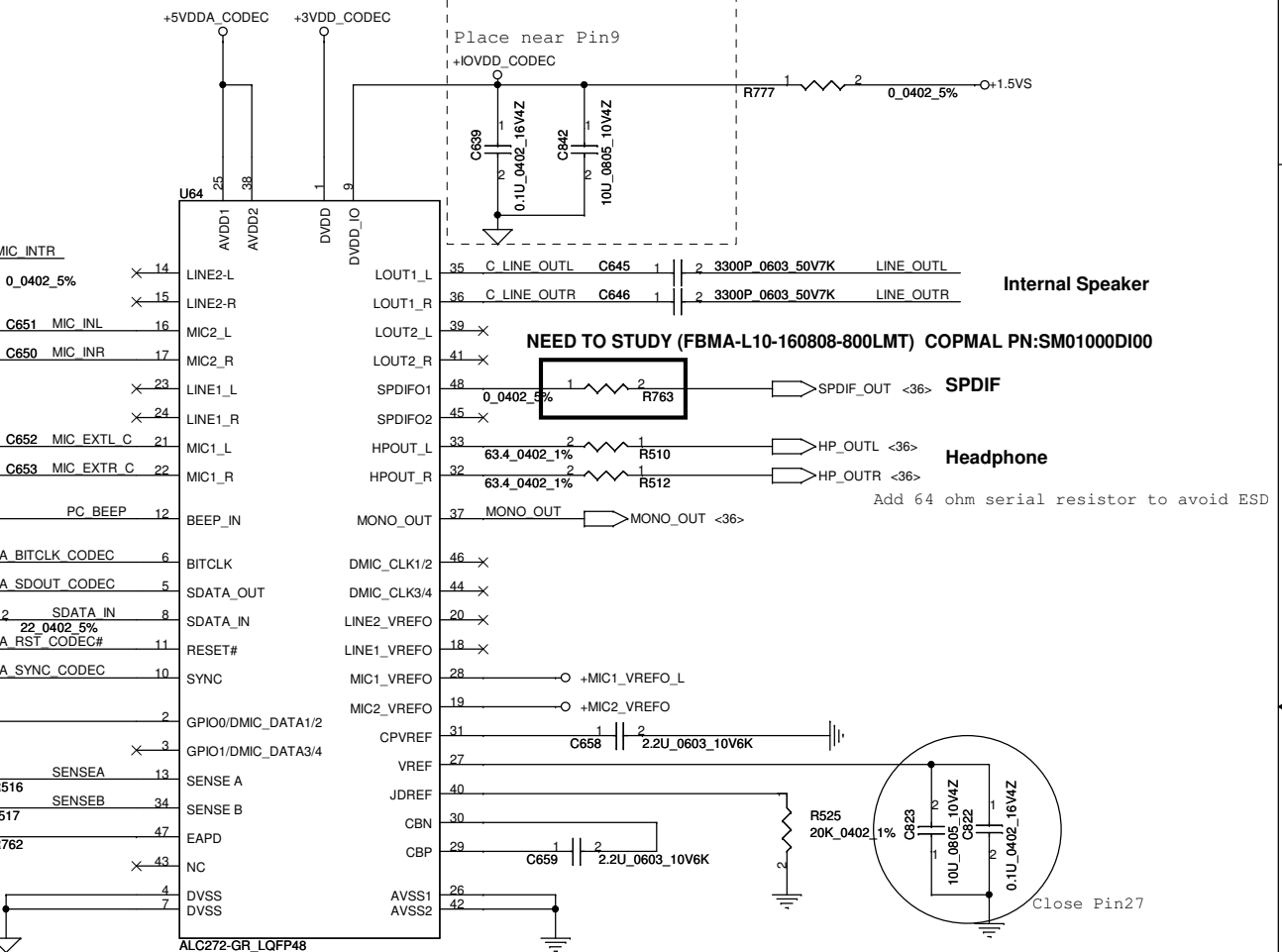
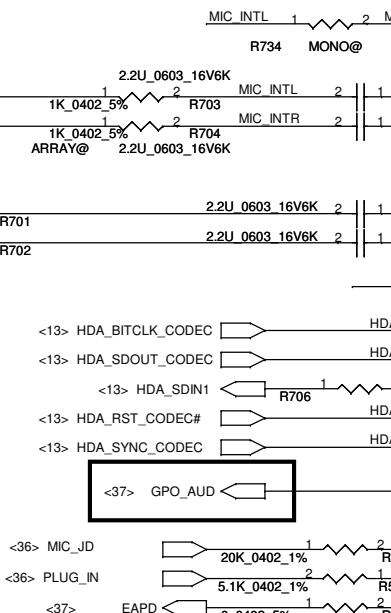
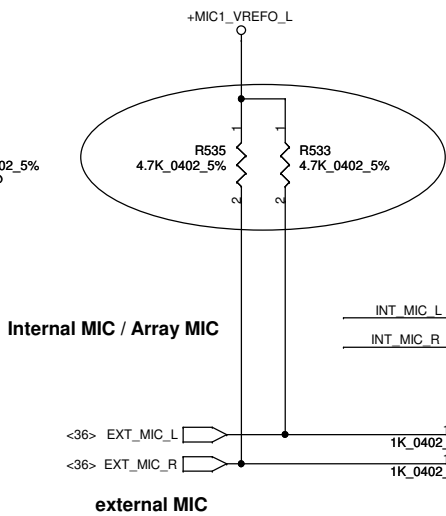
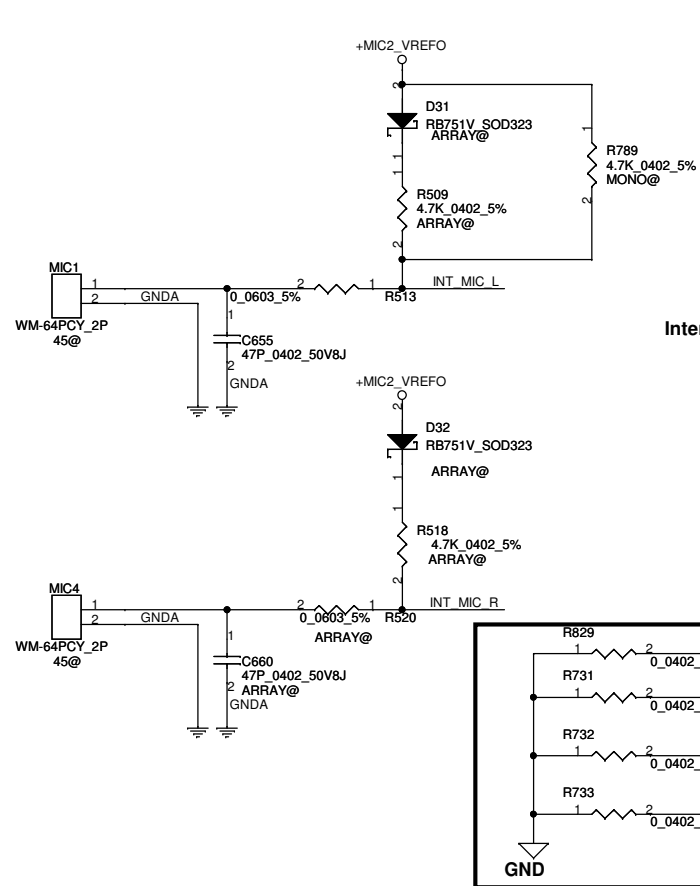
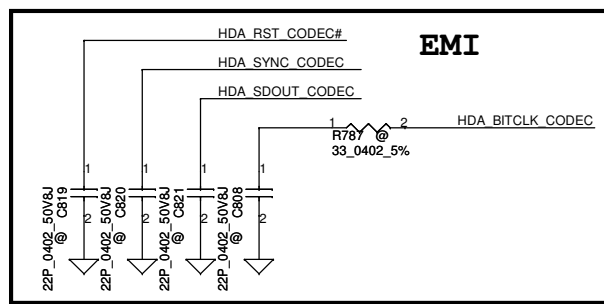
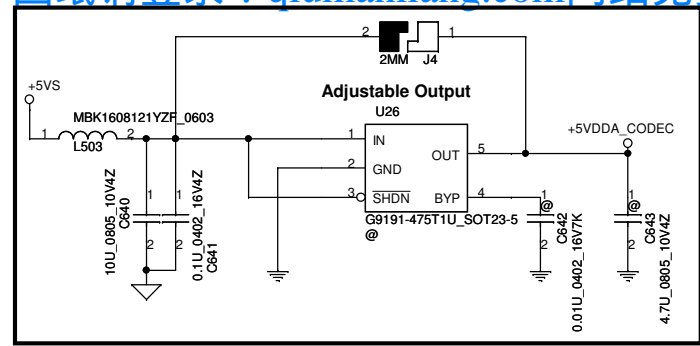
ESATA and USB Conn.



A+ = RXP
A- = RXN
B- = TXN
B+ = TXP

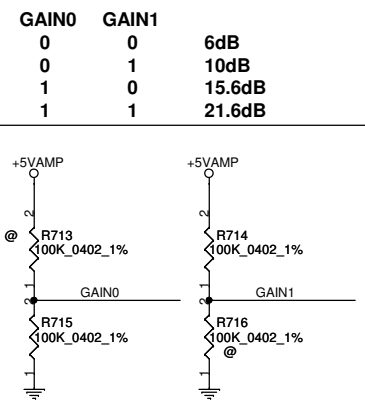
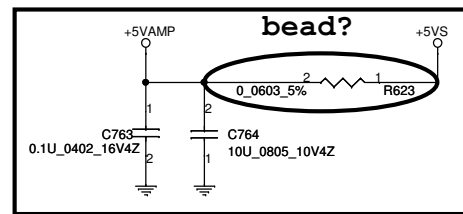
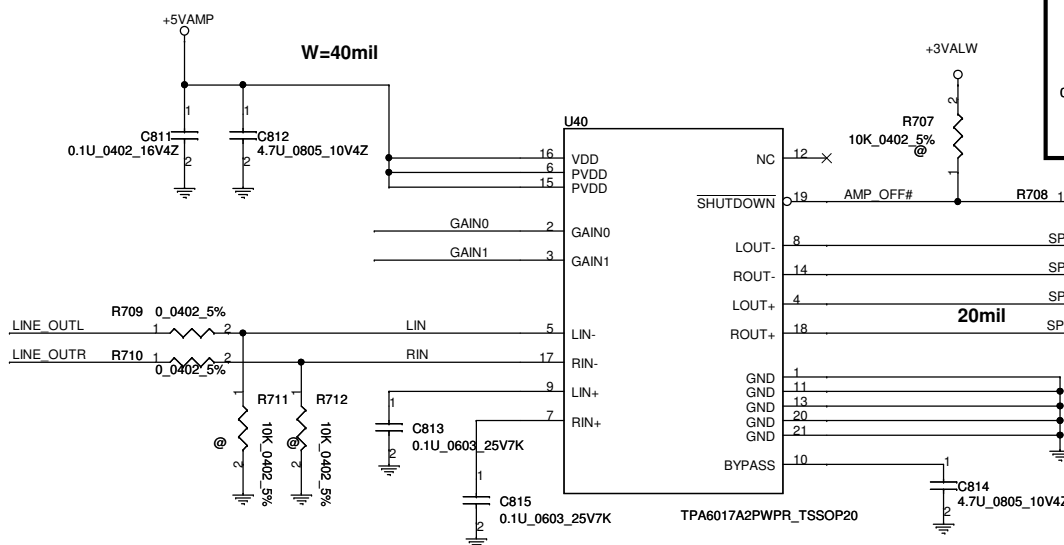
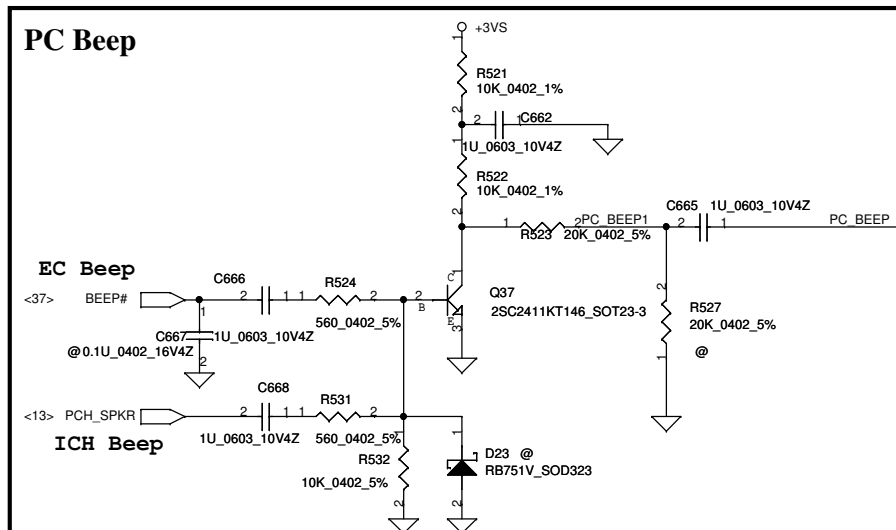


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MIC Sense
R516 place near pin13
Capless HP Sense
R517 place near pin34

Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1 (Pin21/22)	External	Mic in
MONO-OUT (Pin37)	Internal	Internal Subwoofer
MIC2 (Pin16/17)	Internal	Internal Mic

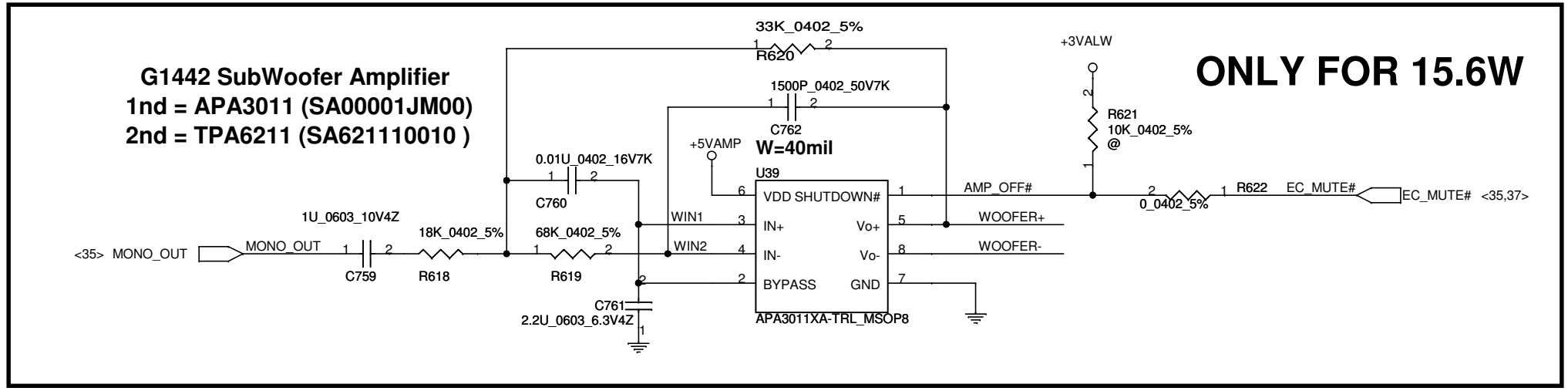
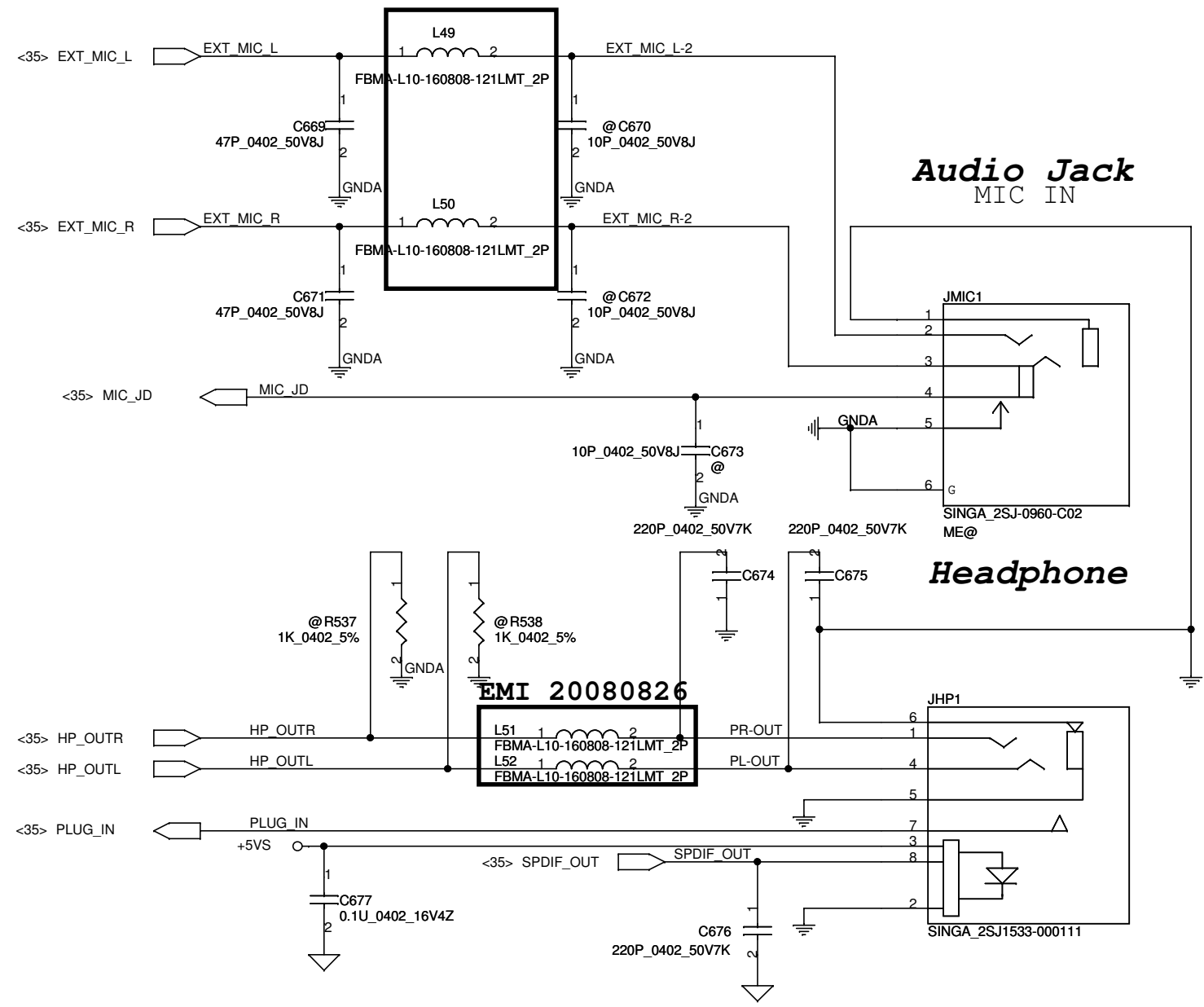
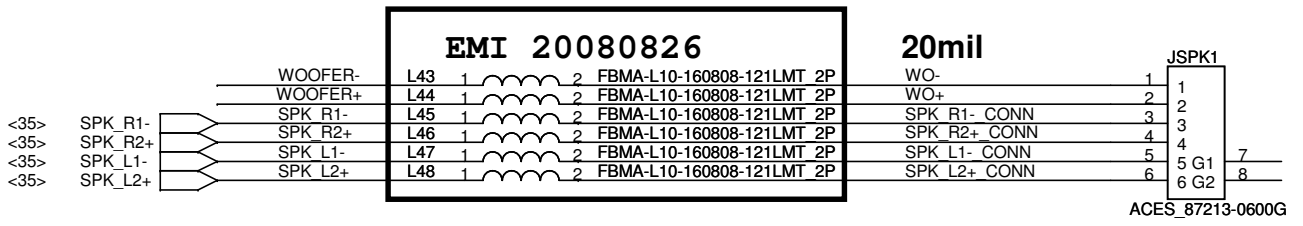


GAIN0	GAIN1	Gain
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

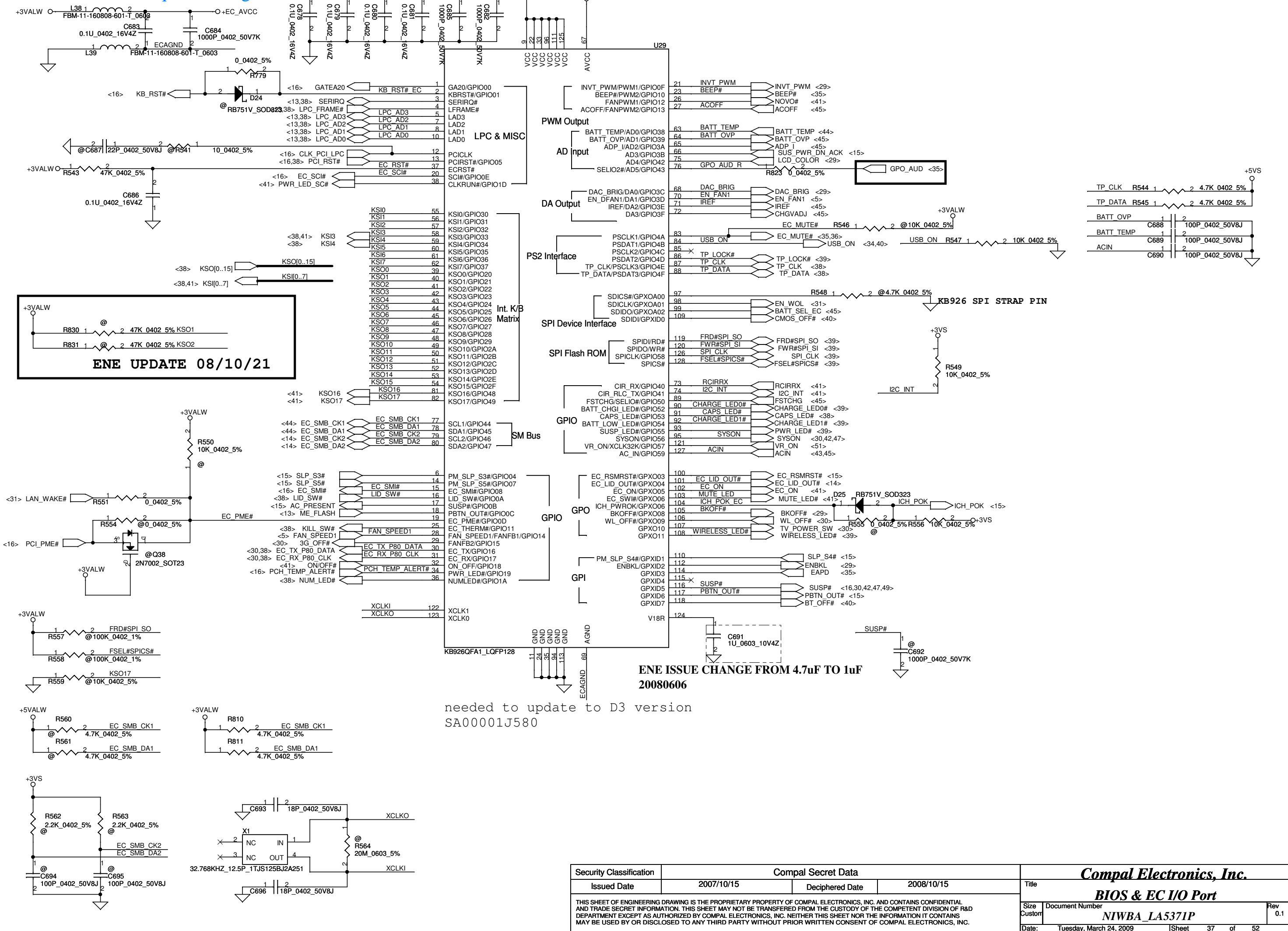
Audio Jack

EMI 20080826

SubWoofer Conn. Speaker Connector



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Size Custom	Document Number	Rev	
	KIWB1/B2_LA4601P	0.1	
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ENE UPDATE 08/10/21

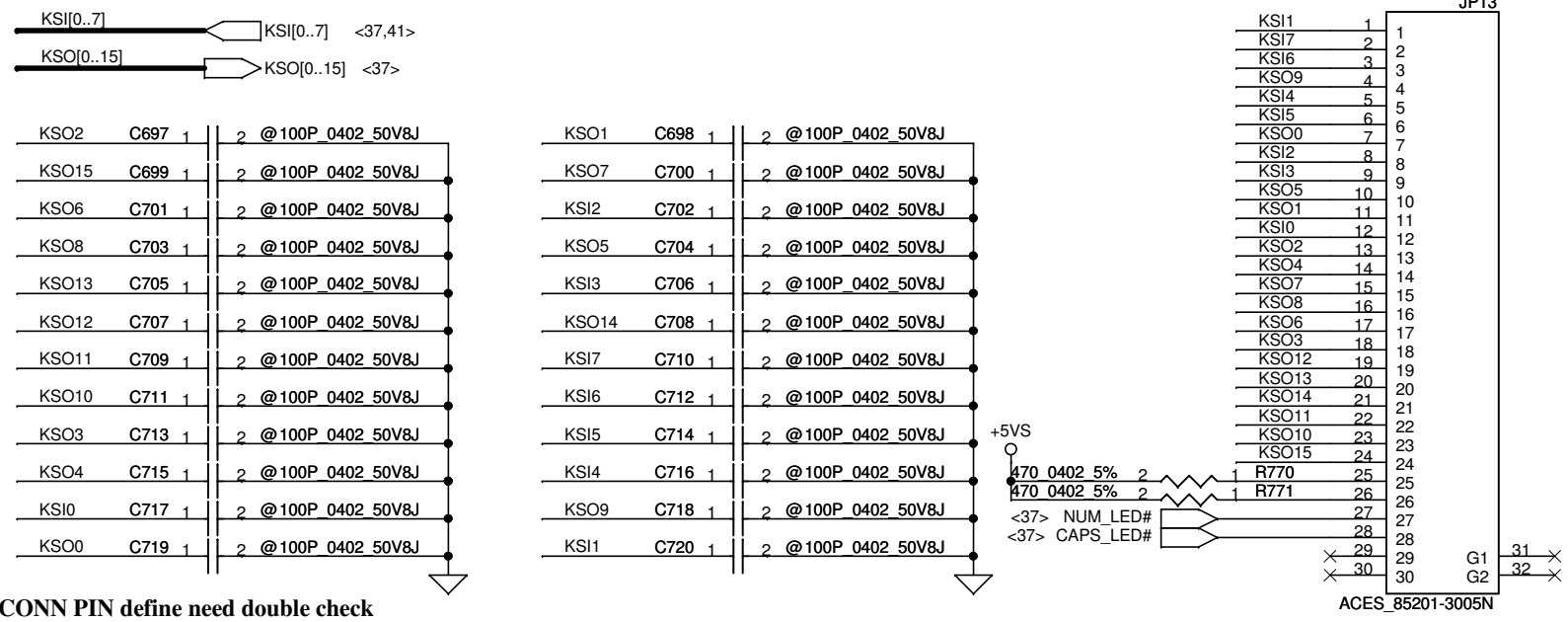
**ENE ISSUE CHANGE FROM 4.7uF TO 1uF
20080606**

needed to update to D3 version
SA00001J580

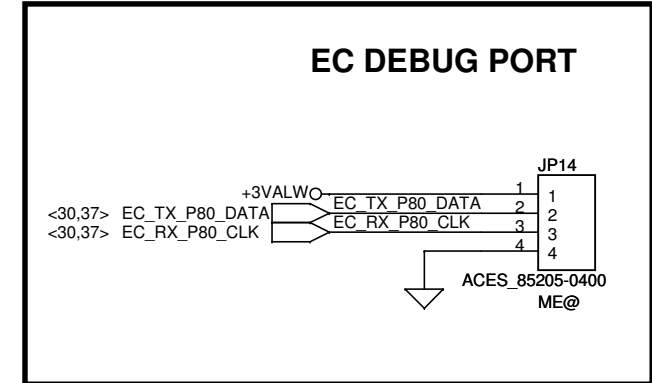
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Issued Date	2007/10/15	Deciphered Date	
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Compal Electronics, Inc.
BIOS & EC I/O Port
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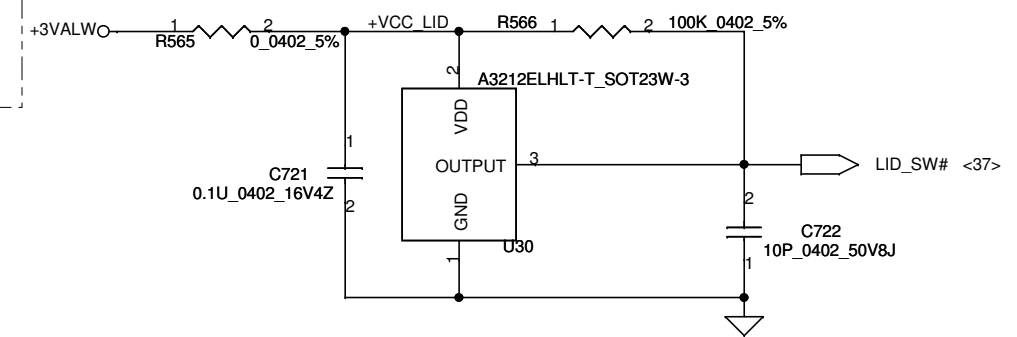
INT_KBD Conn.



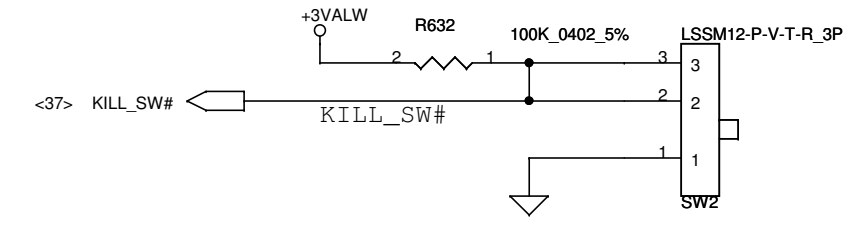
CONN PIN define need double check



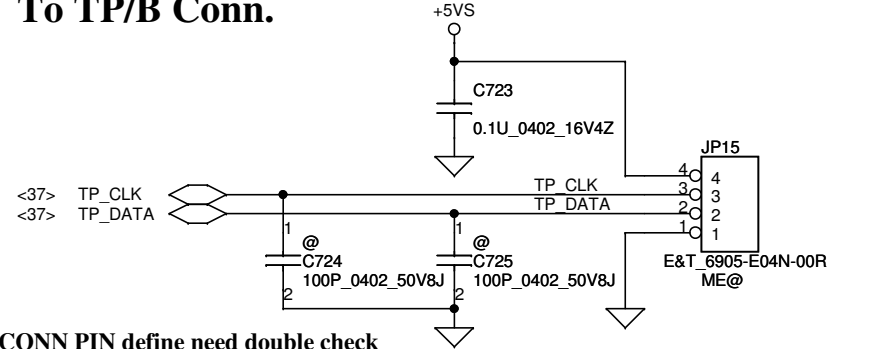
Lid Switch



Kill Switch

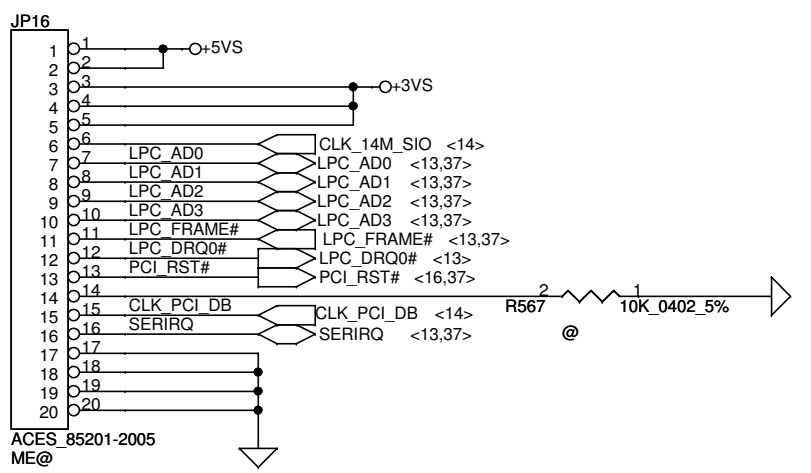


To TP/B Conn.



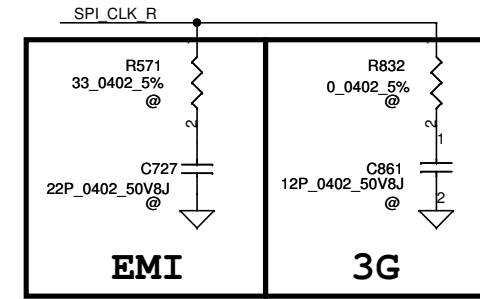
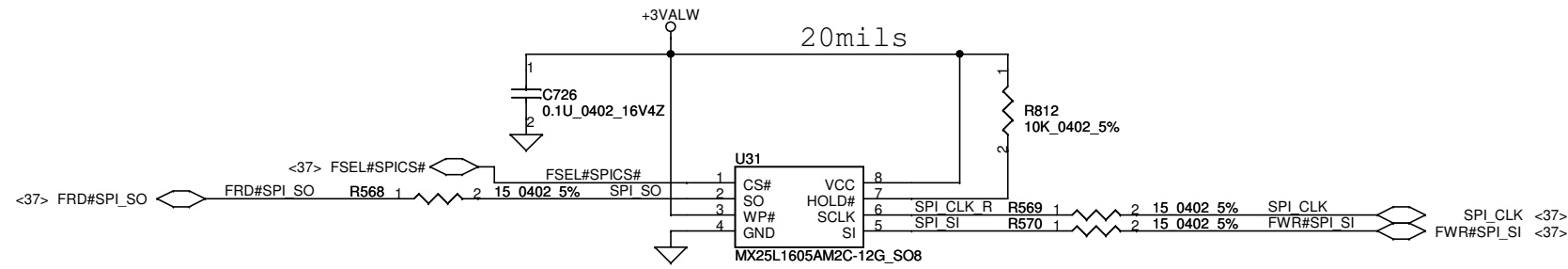
CONN PIN define need double check

FOR LPC SIO DEBUG PORT



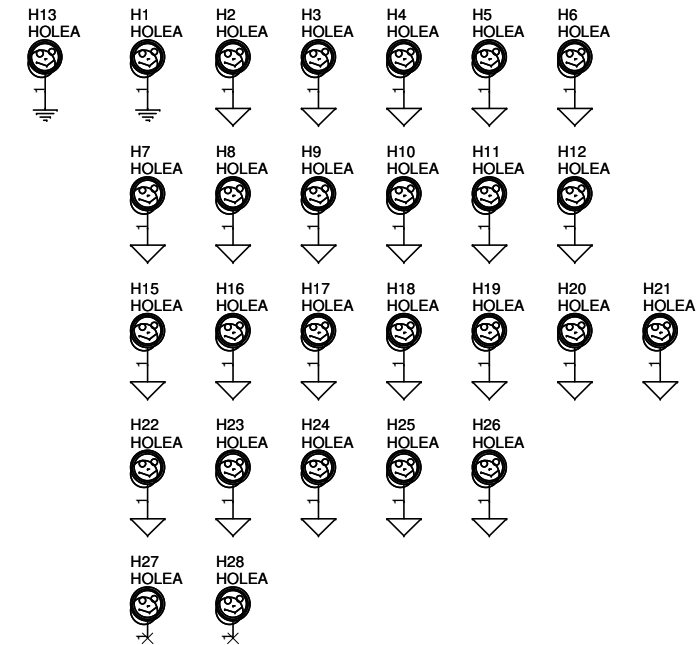
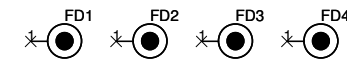
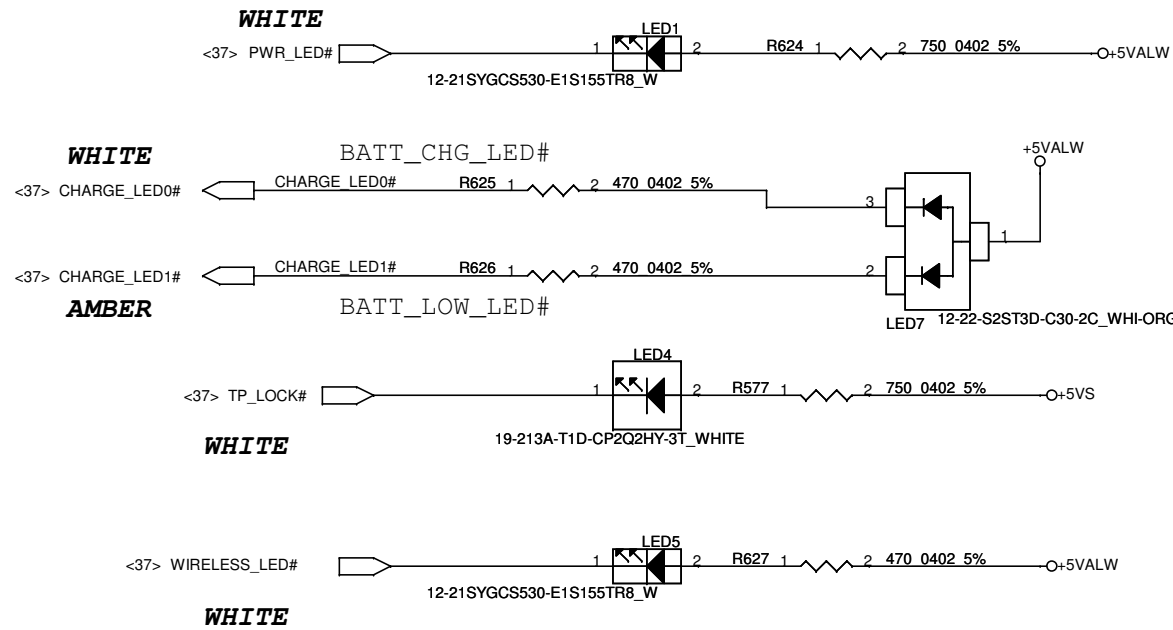
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FOR EC 16M SPI ROM



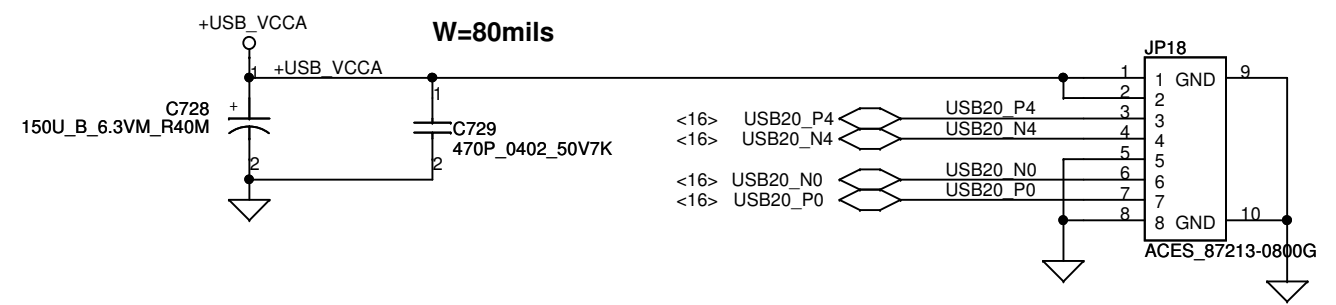
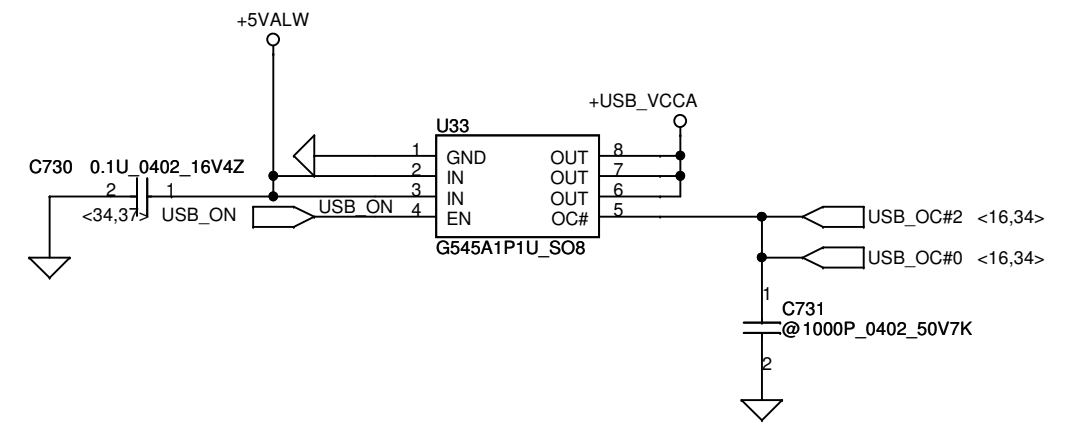
LED

SC500005B00, If=5mA, Vf=2.7V~3.15V, R=460~390ohm

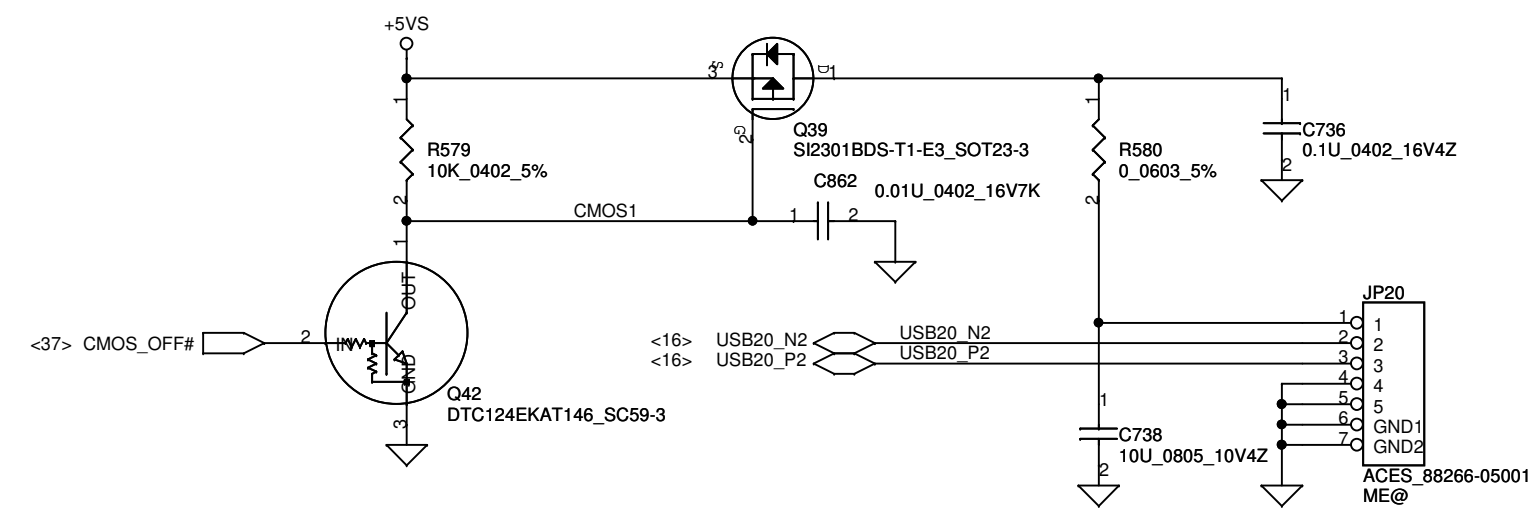


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				Size B
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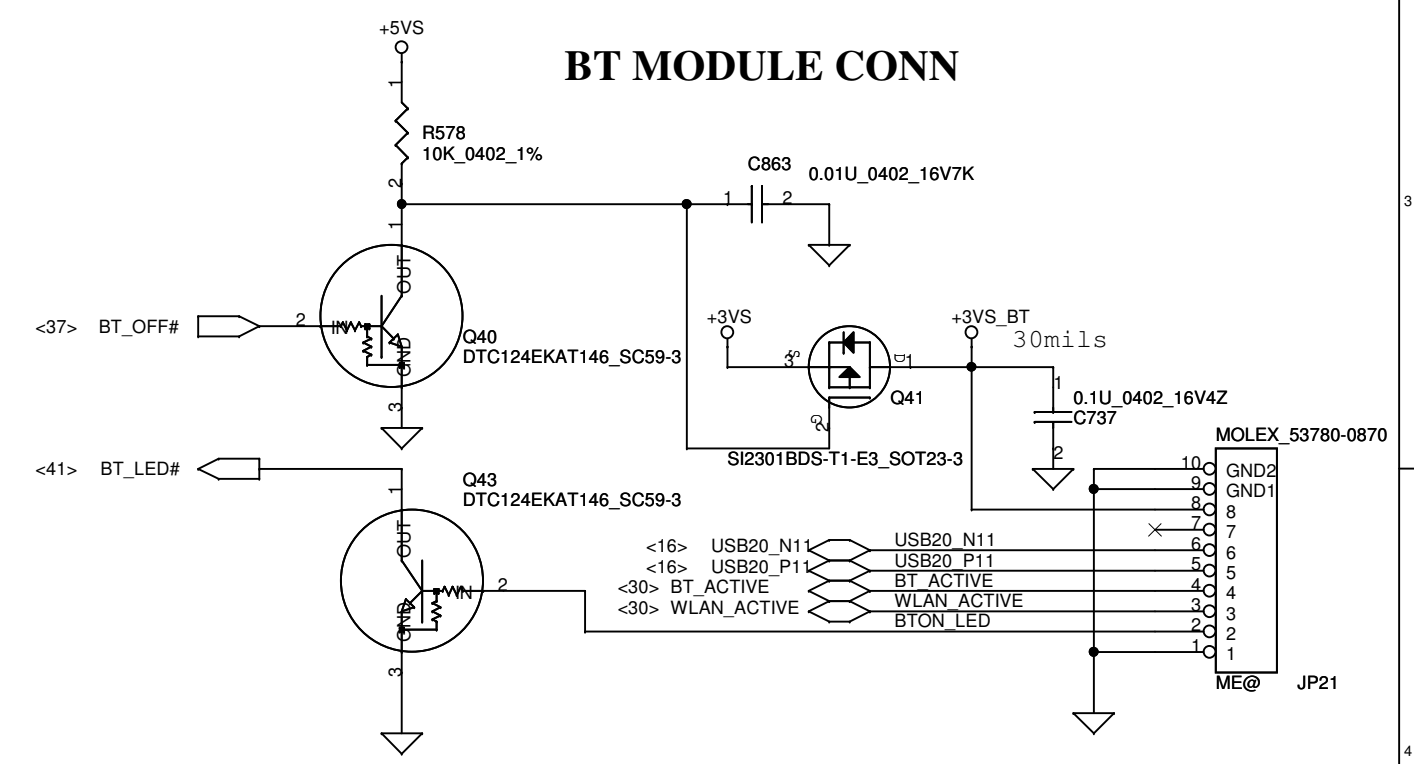
USB Board Conn. 10 pin



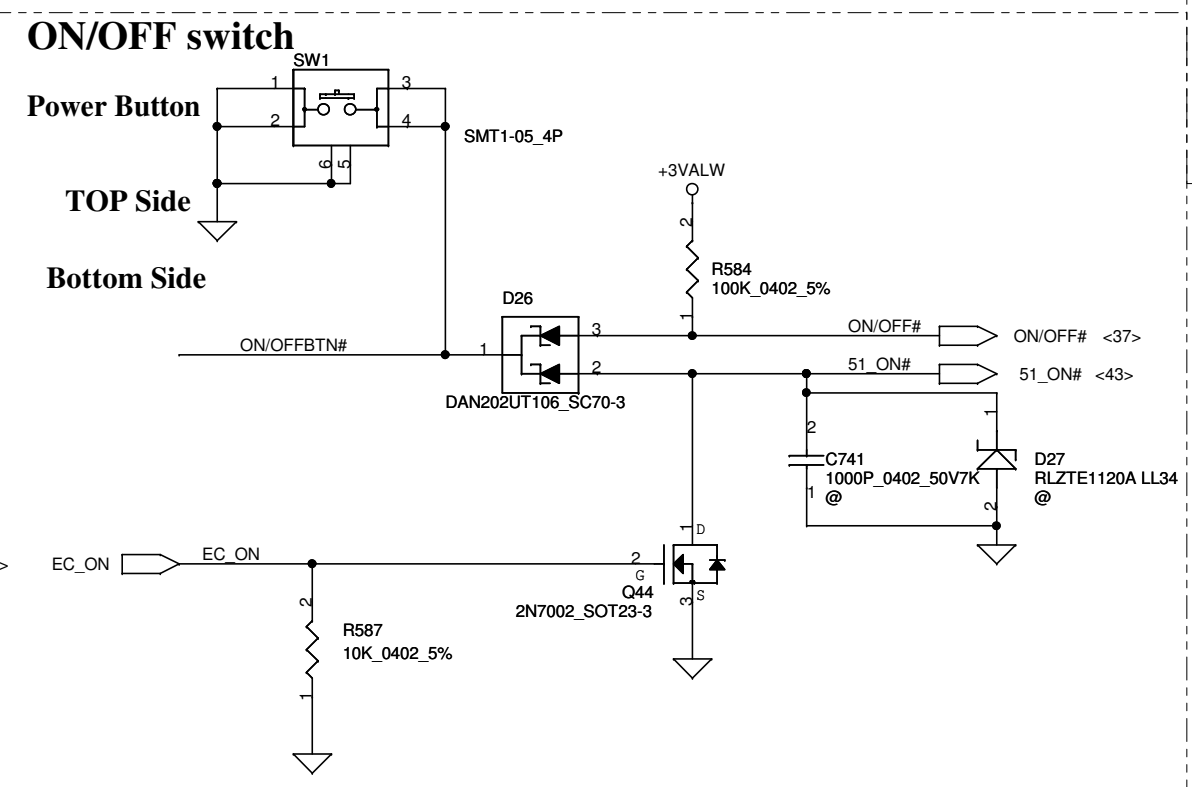
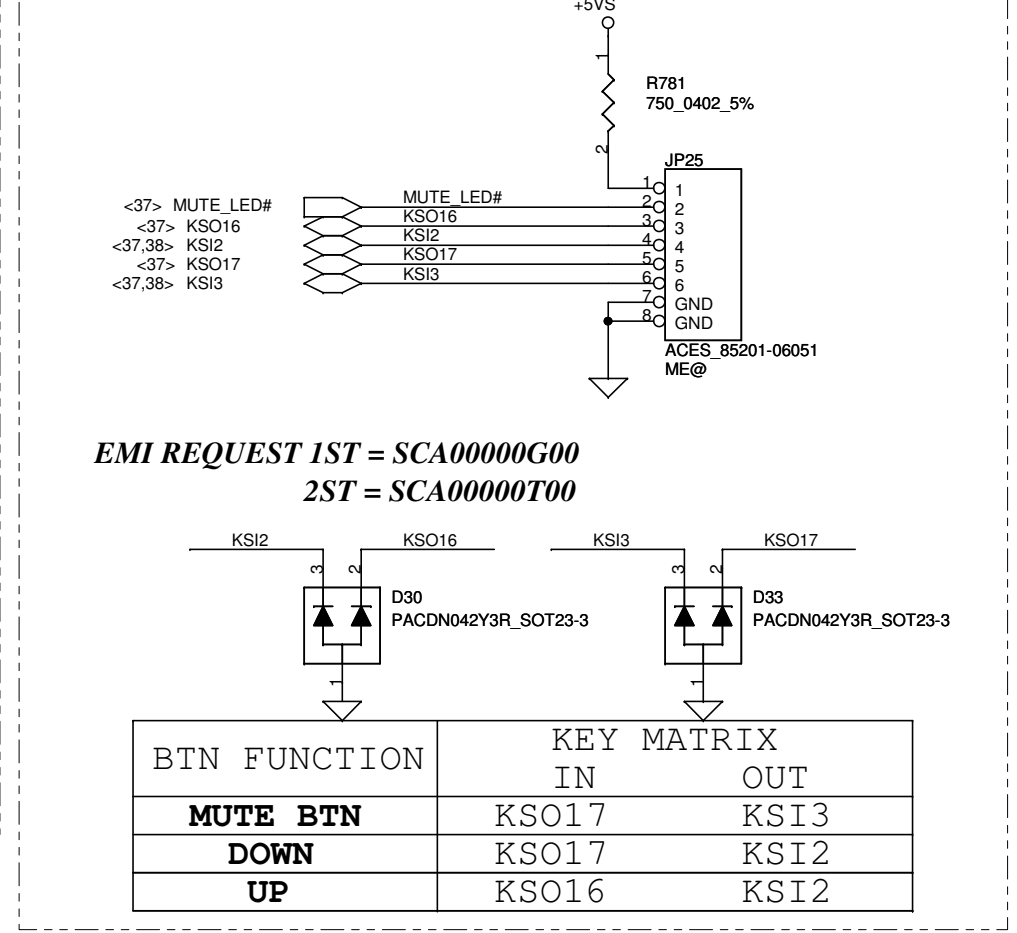
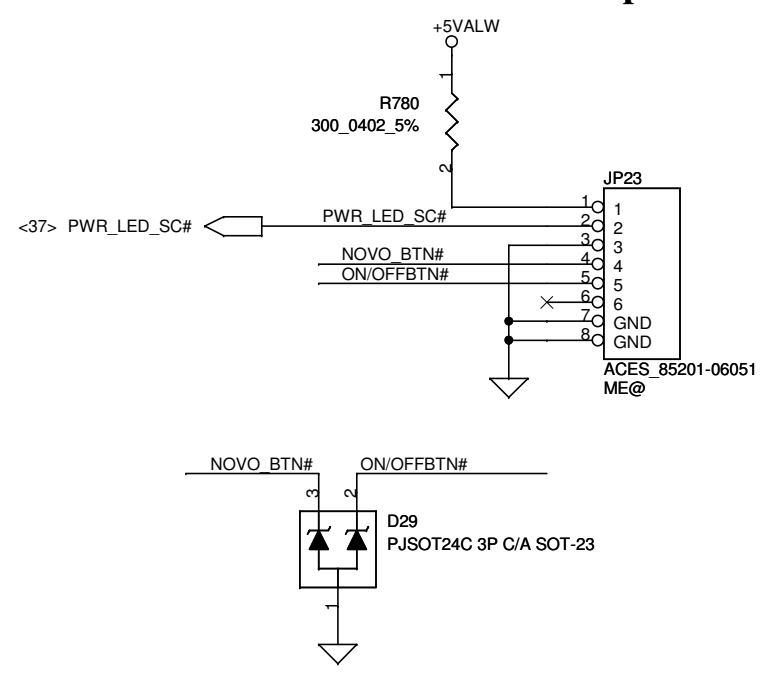
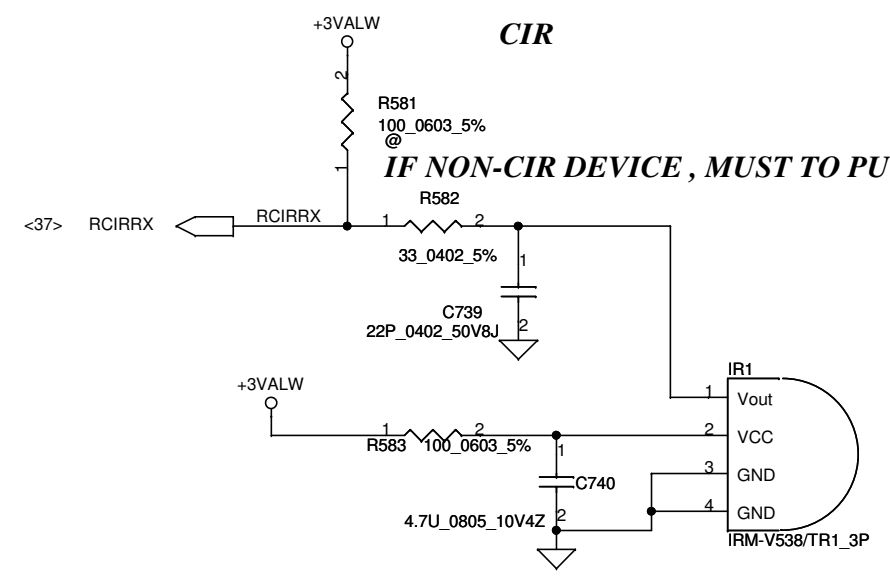
CMOS Camera Conn



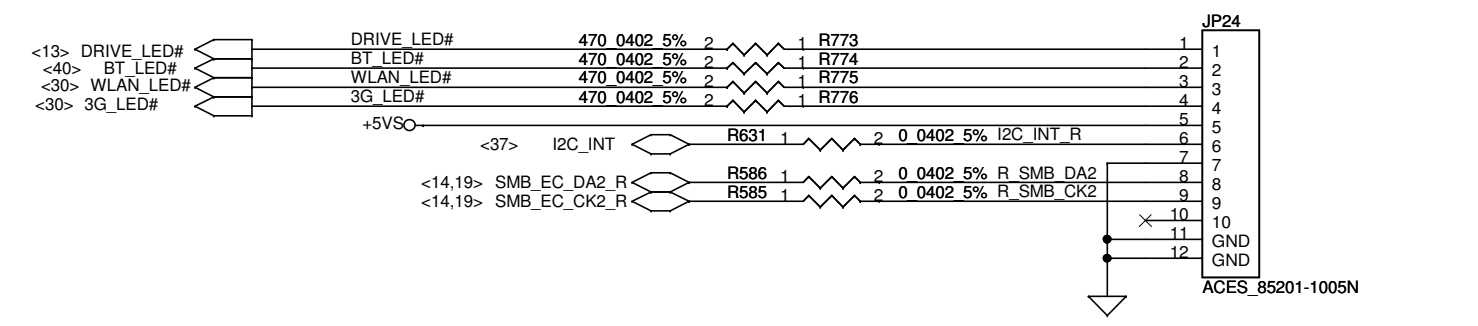
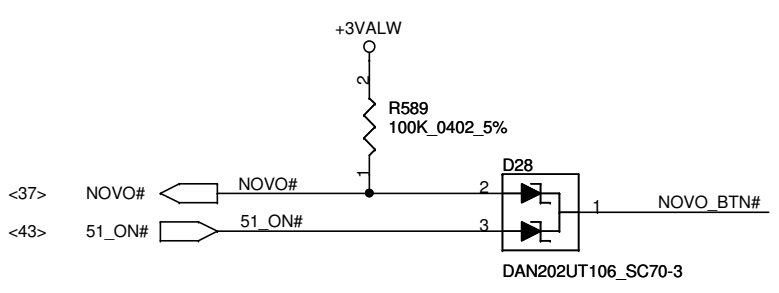
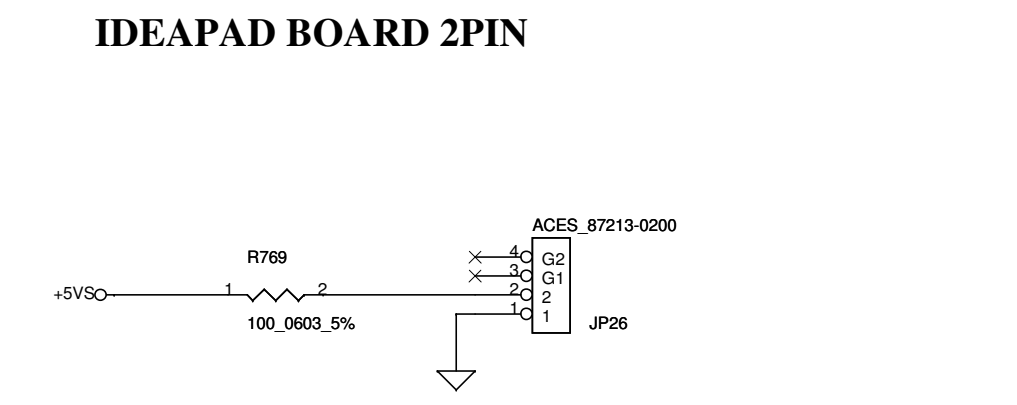
BT MODULE CONN



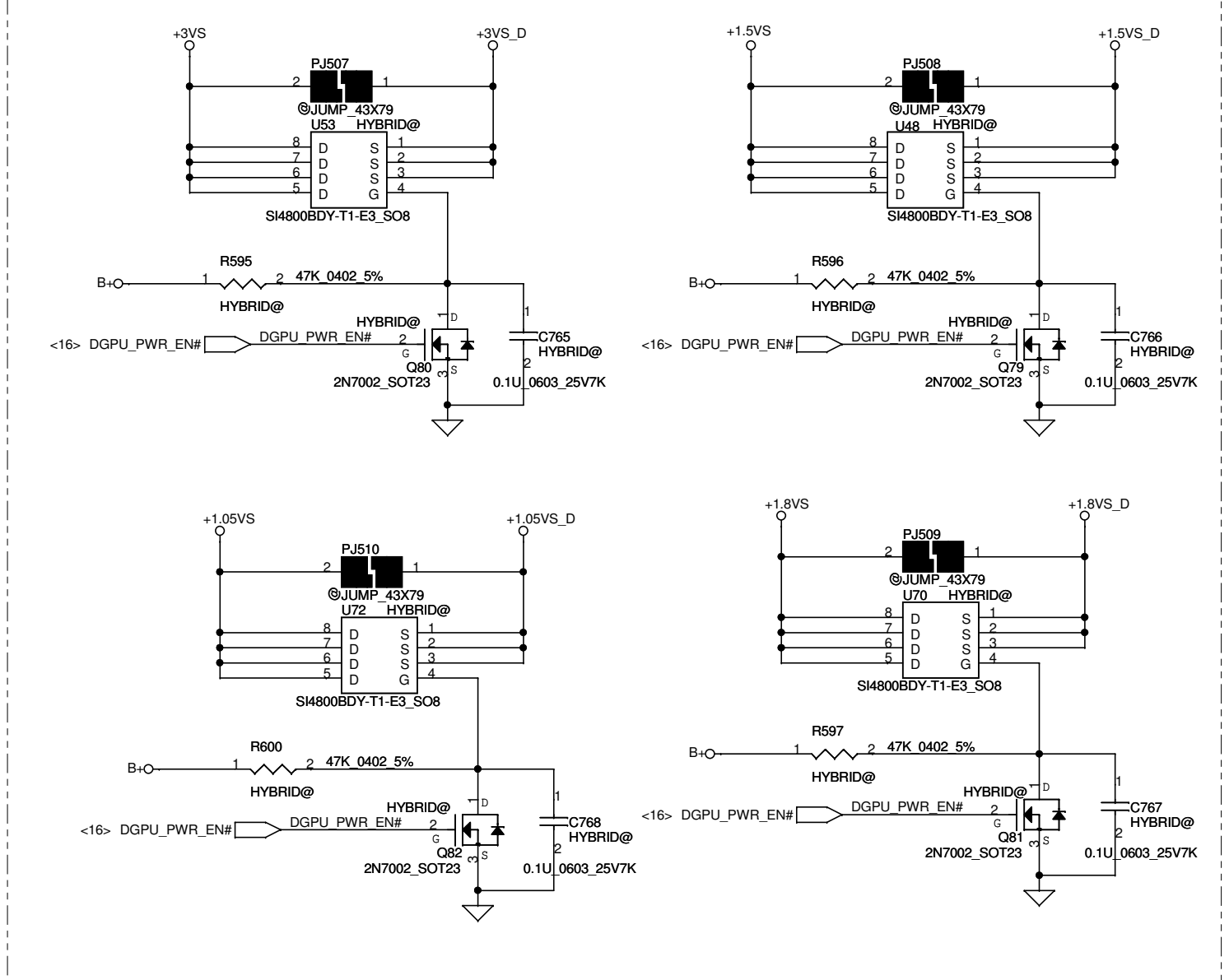
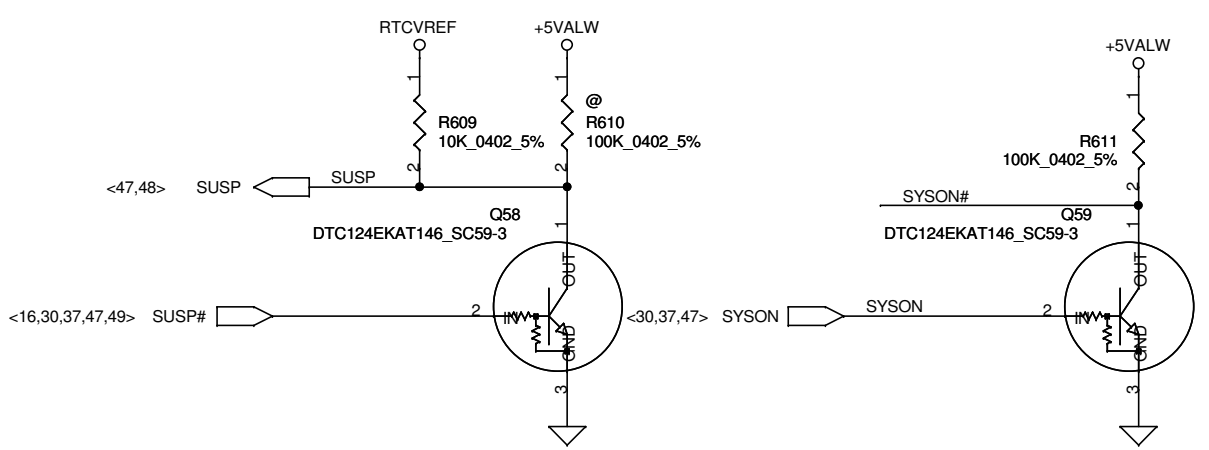
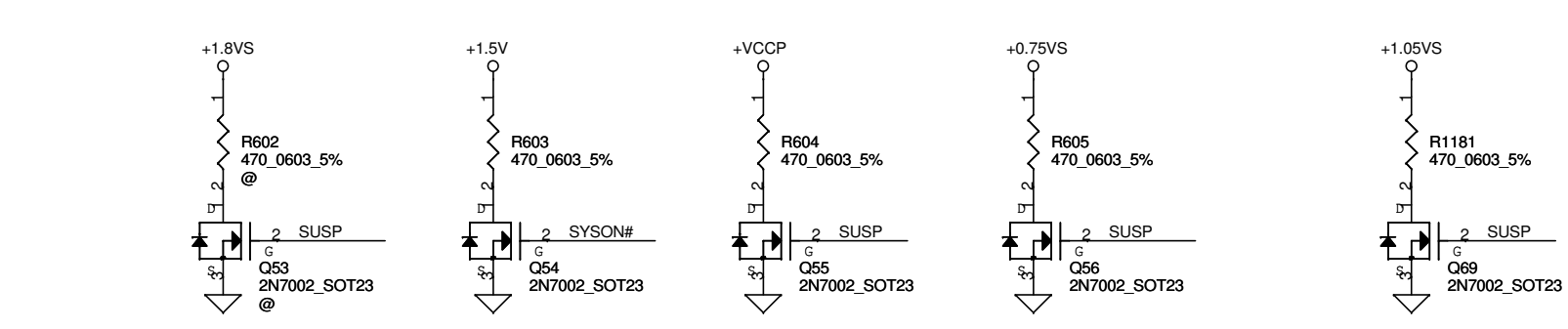
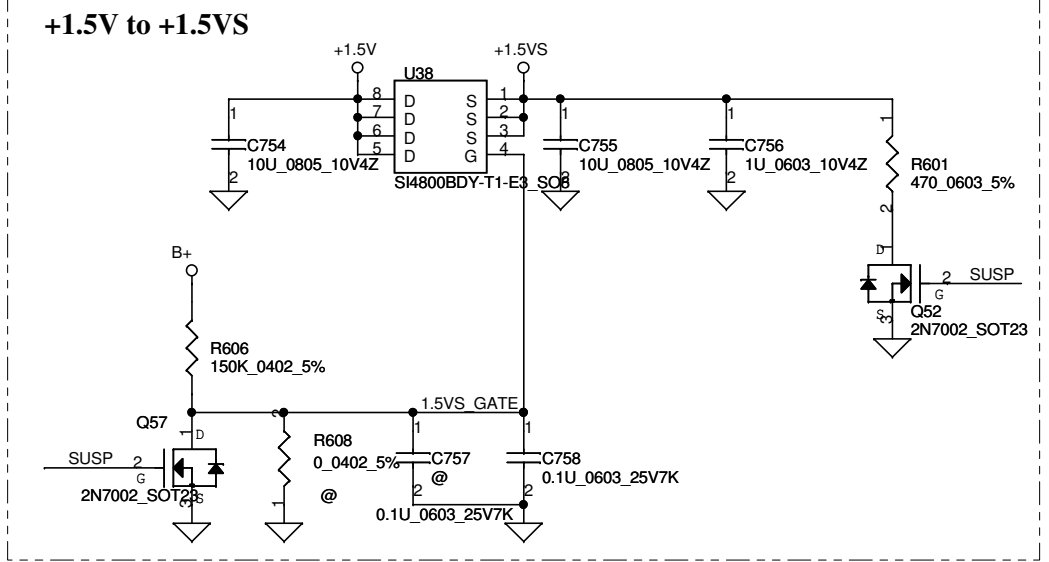
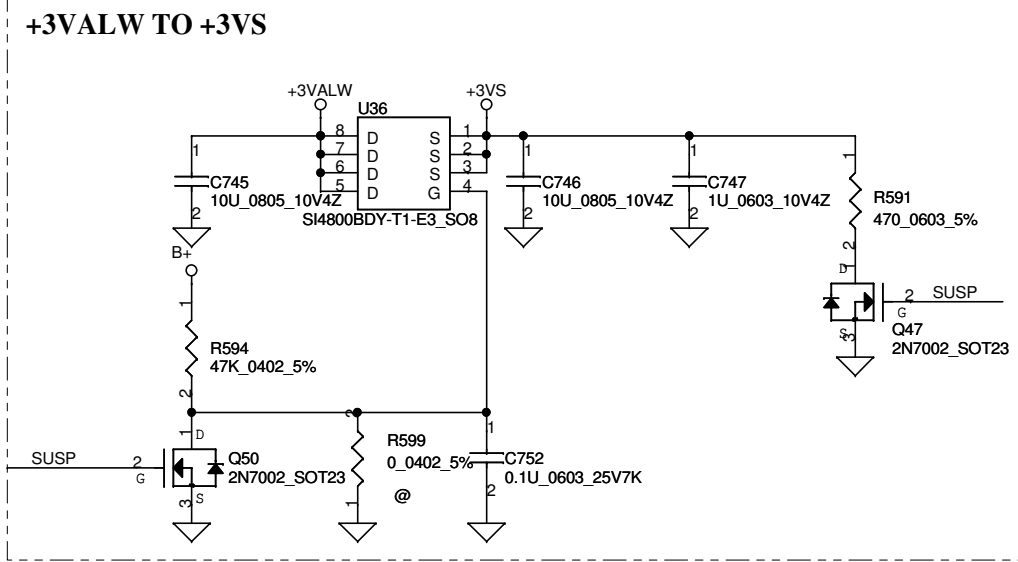
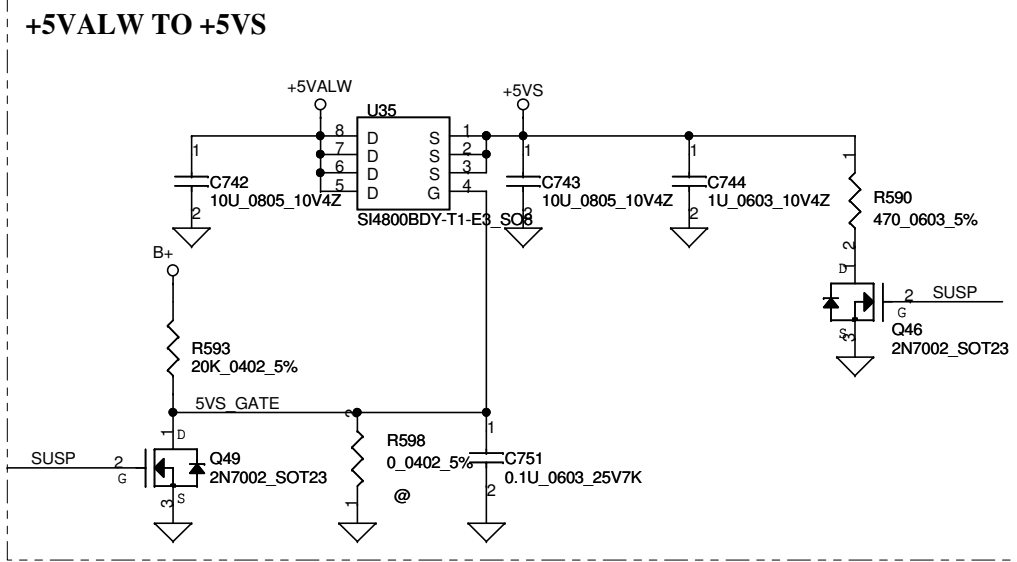
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Size Custom		Document Number		Rev
		NIWBA_LA5371P		0.1
Date:	Tuesday, March 24, 2009	Sheet	40 of 52	



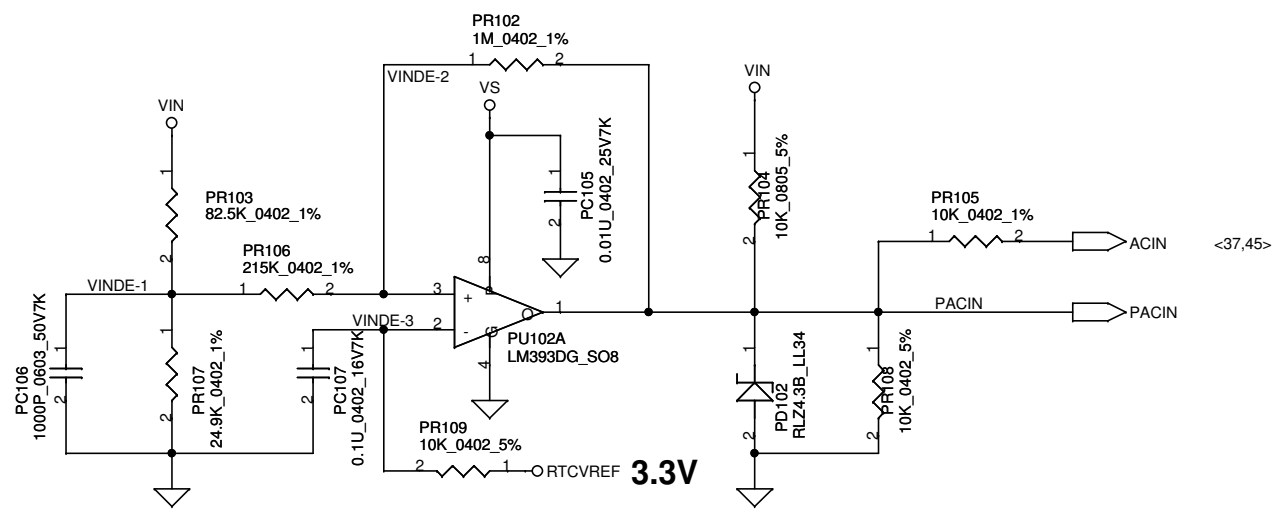
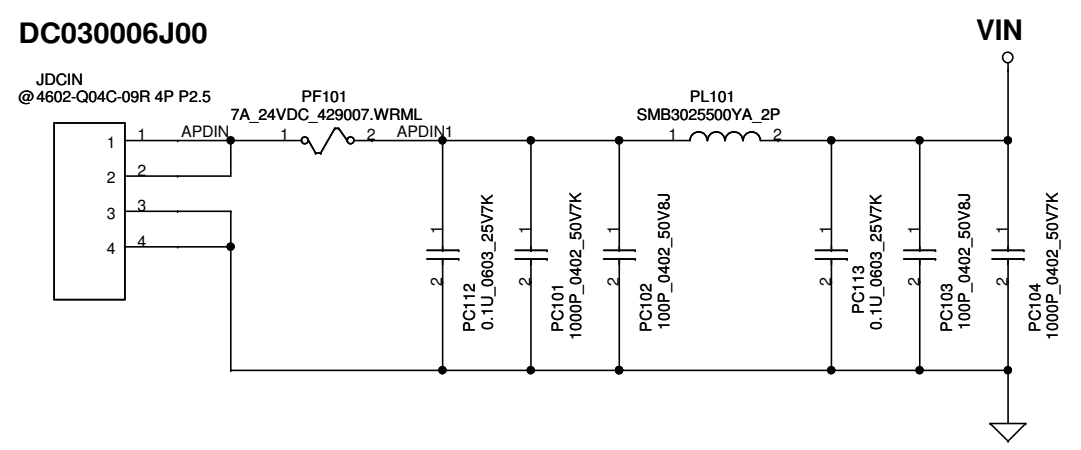
EMI REQUEST 1ST = SCA00000E00
2ST = SCA00000R00



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				Size Custort
				NIWBA_LA5371P
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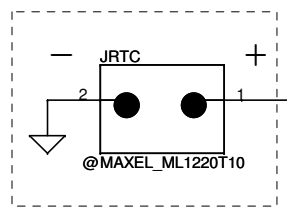


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				Size	Document Number
				NIWBA_LA5371P	
				Date:	Tuesday, March 24, 2009
				Sheet	42 of 52

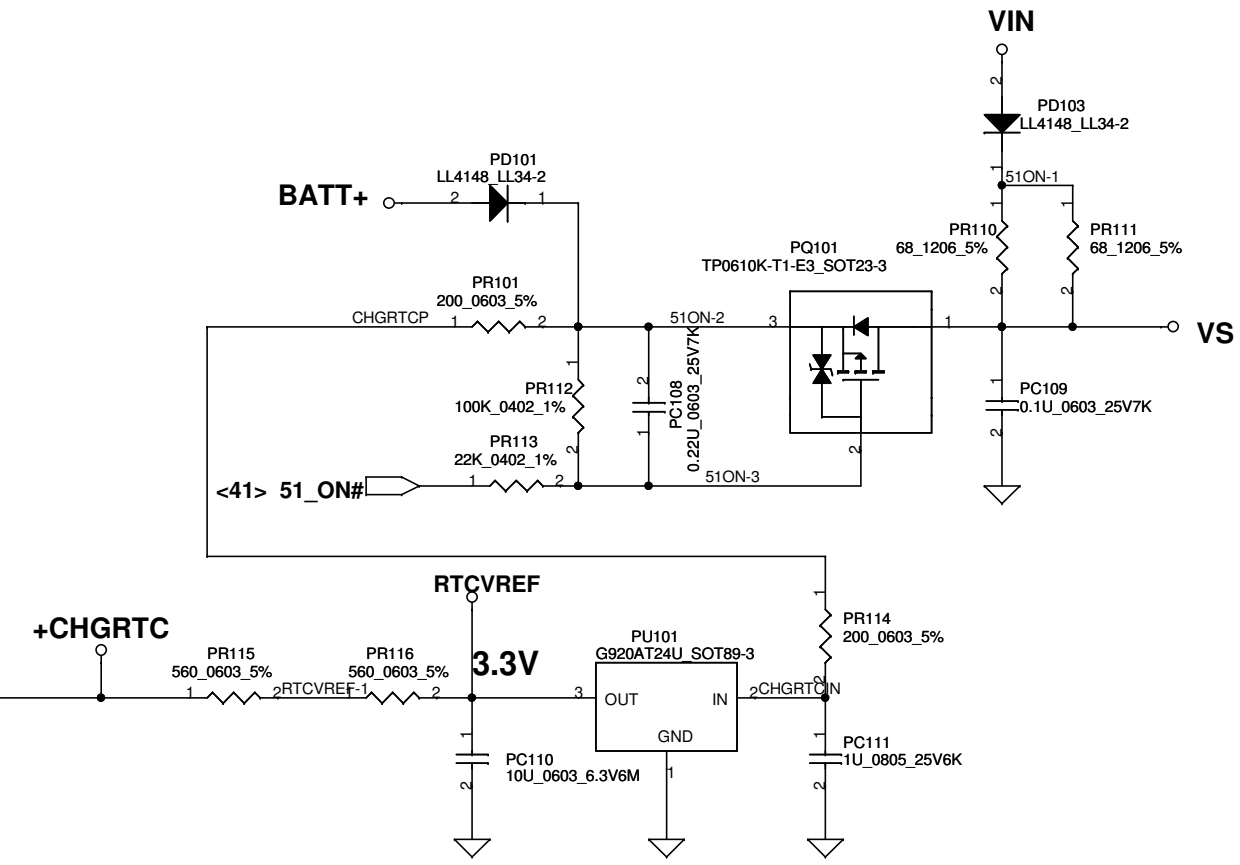


Vin Detector		
High	18.135	17.566
Low	14.866	14.063

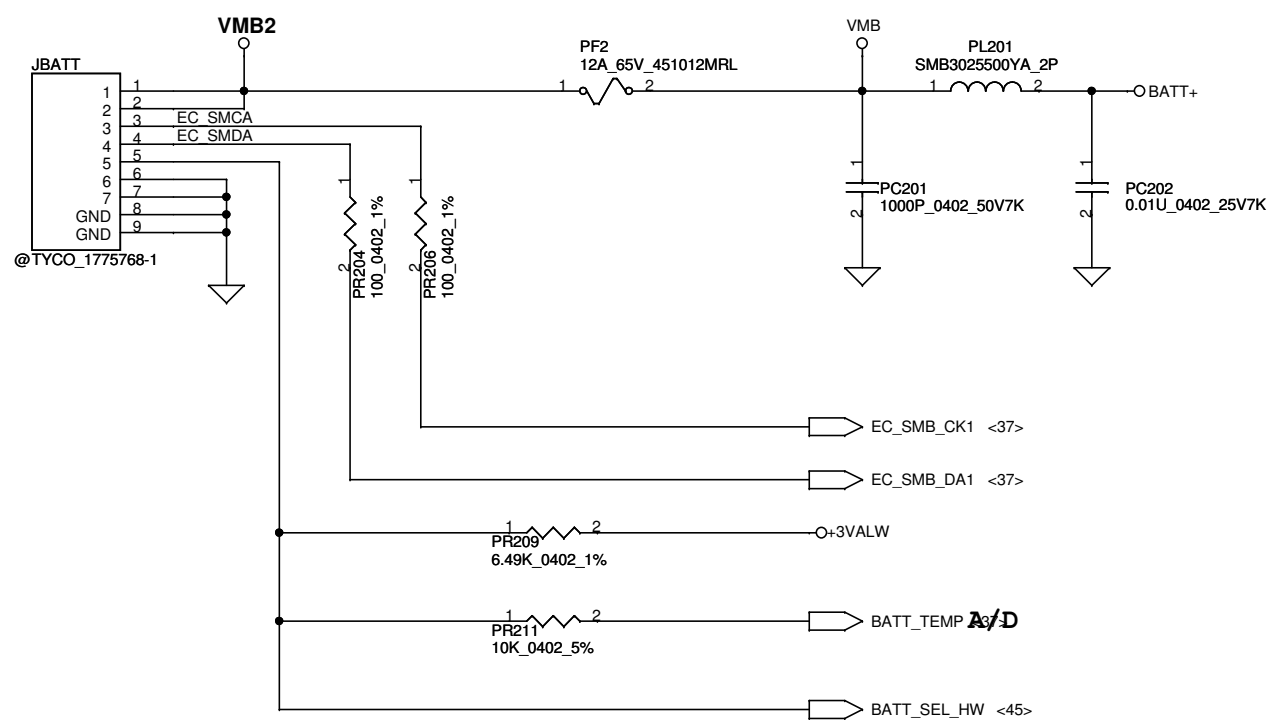
RTC Battery



SP093MX0000

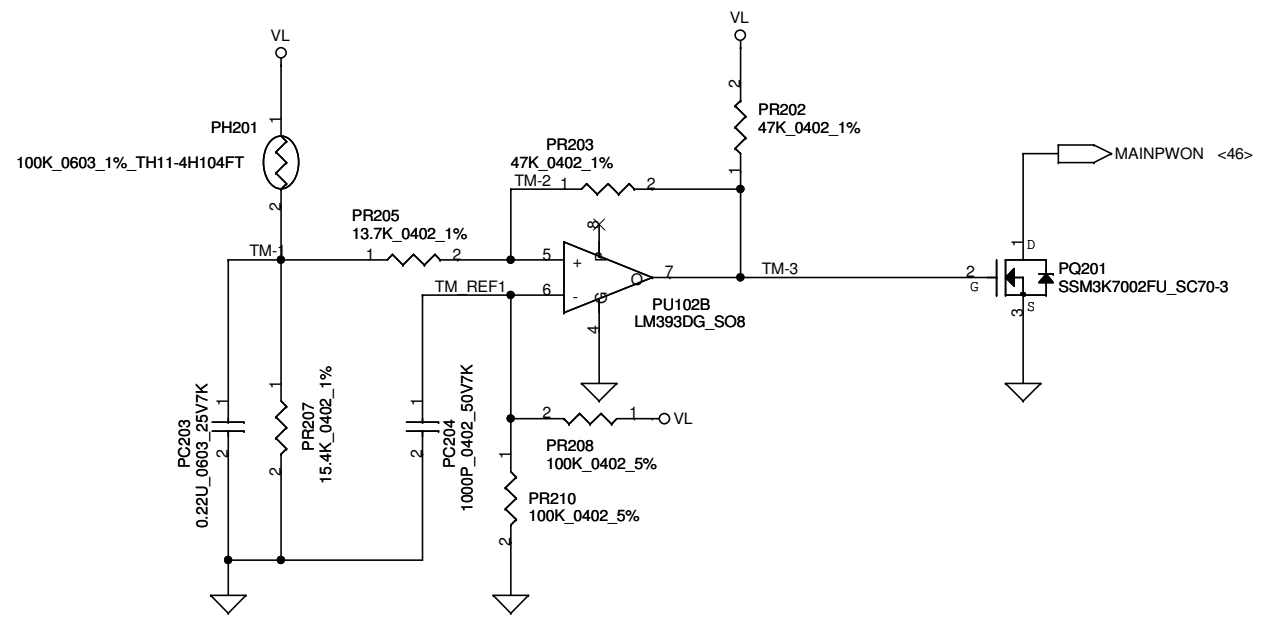


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Date: Tuesday, March 24, 2009			Sheet 43 of 52	Rev 0.1

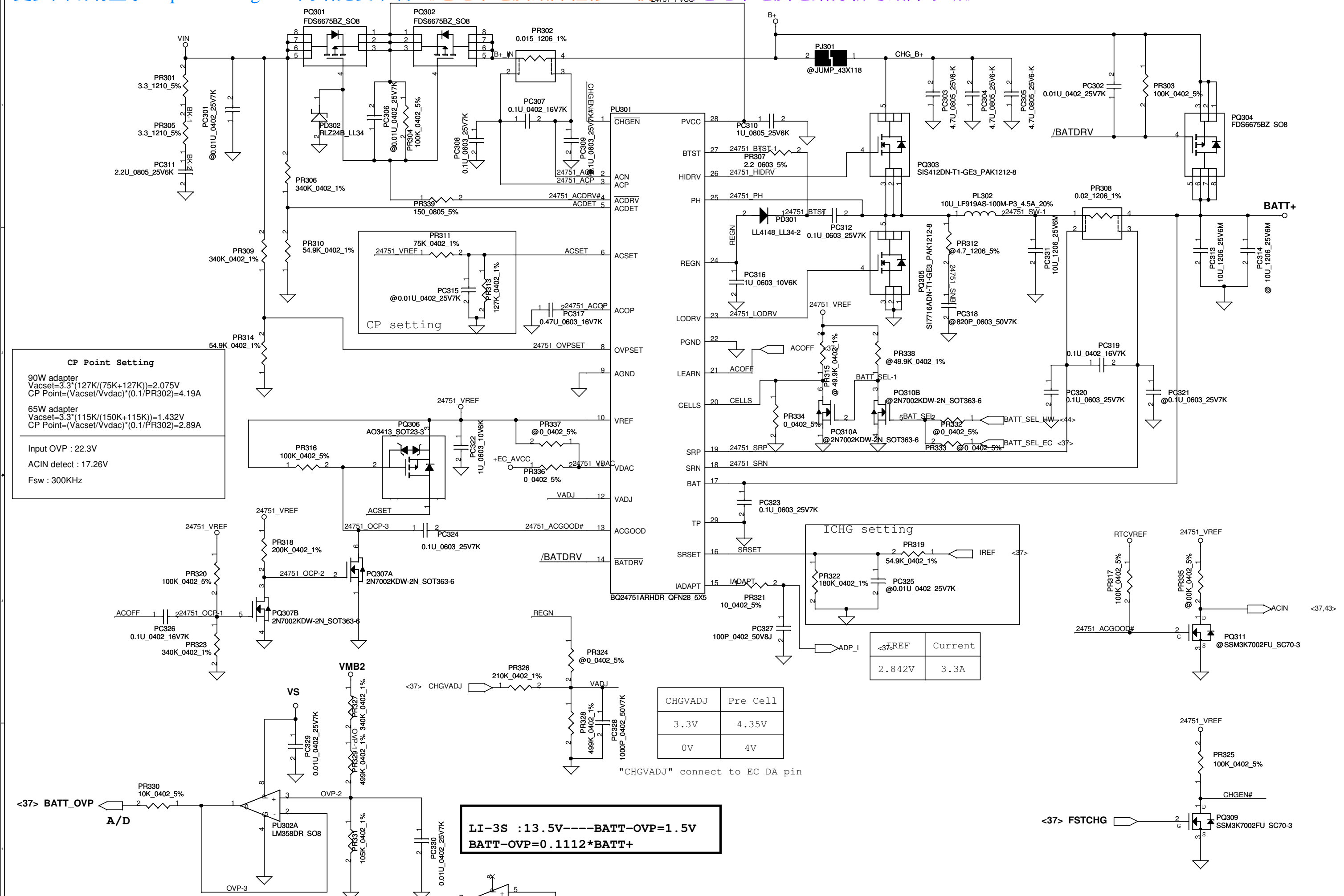


PH1 under CPU botten side :

CPU thermal protection at 92 degree C
Recovery at 56 degree C



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				Size
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CP Point Setting

90W adapter
 $V_{acset} = 3.3 * (127K / (75K + 127K)) = 2.075V$
 $CP\ Point = (V_{acset} / V_{vdac}) * (0.1 / PR302) = 4.19A$

65W adapter
 $V_{acset} = 3.3 * (115K / (150K + 115K)) = 1.432V$
 $CP\ Point = (V_{acset} / V_{vdac}) * (0.1 / PR302) = 2.89A$

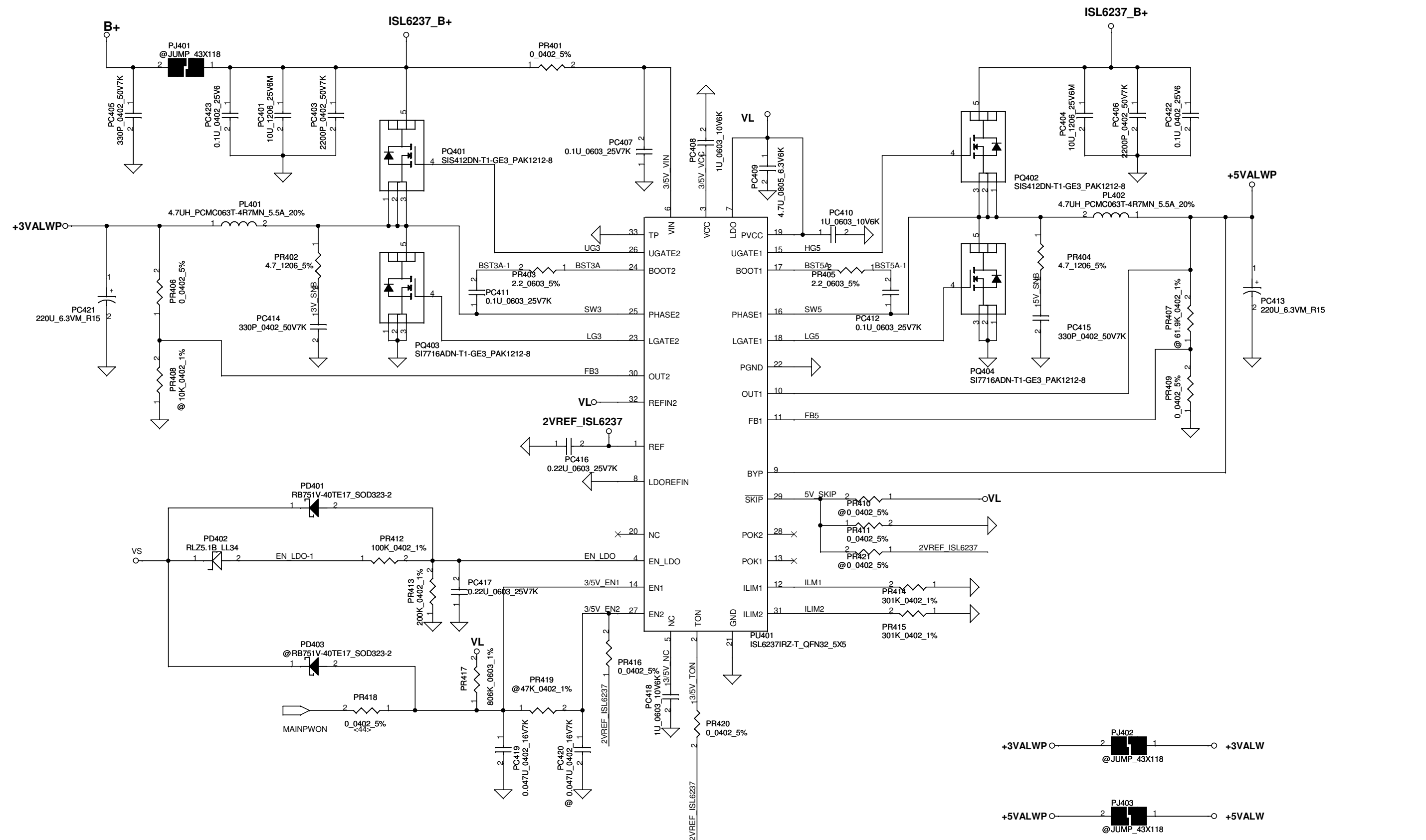
Input OVP : 22.3V
 ACIN detect : 17.26V
 Fsw : 300KHz

ICHG setting

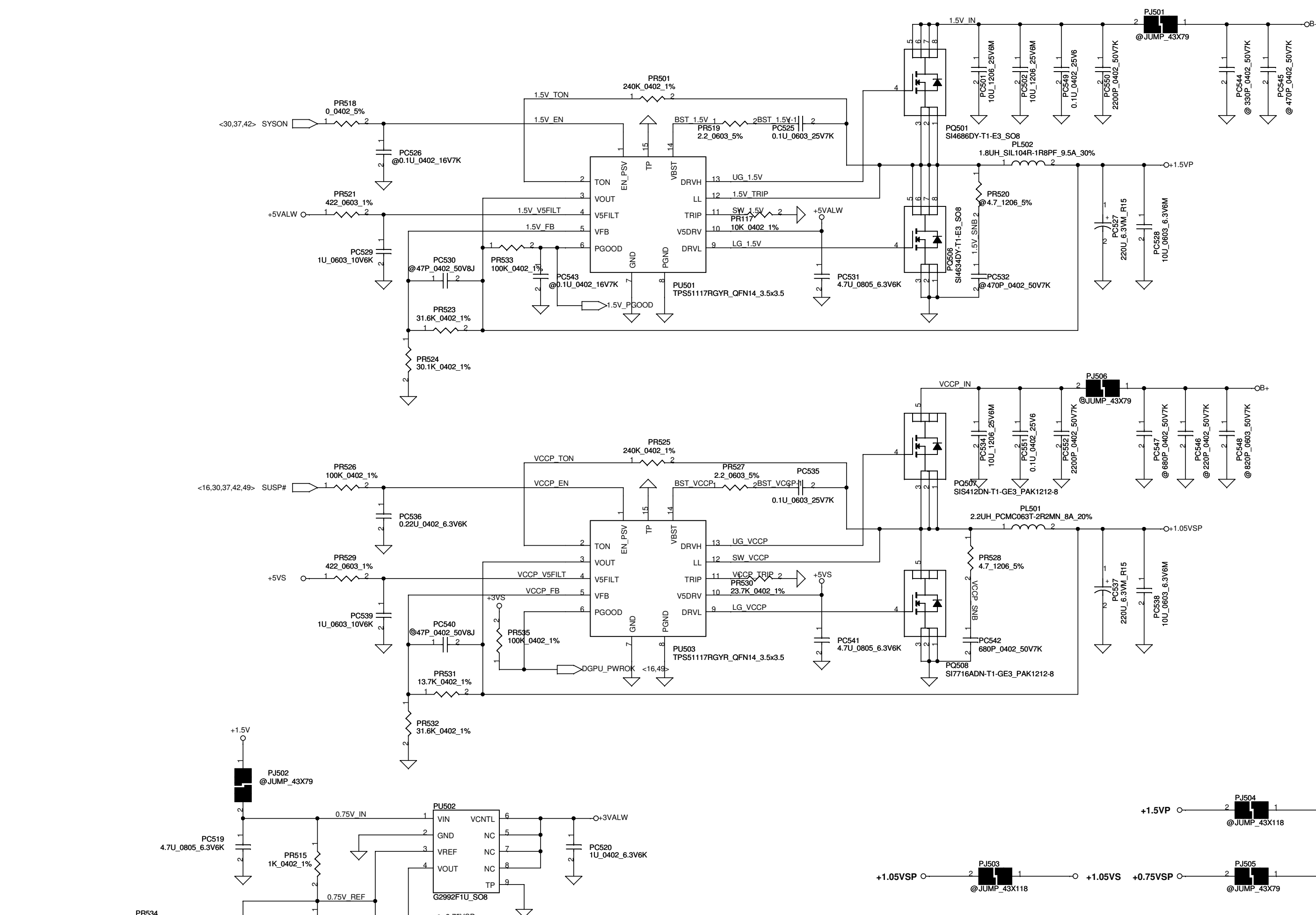
<37>REF	Current
2.842V	3.3A

CHGVADJ	Pre Cell
3.3V	4.35V
0V	4V

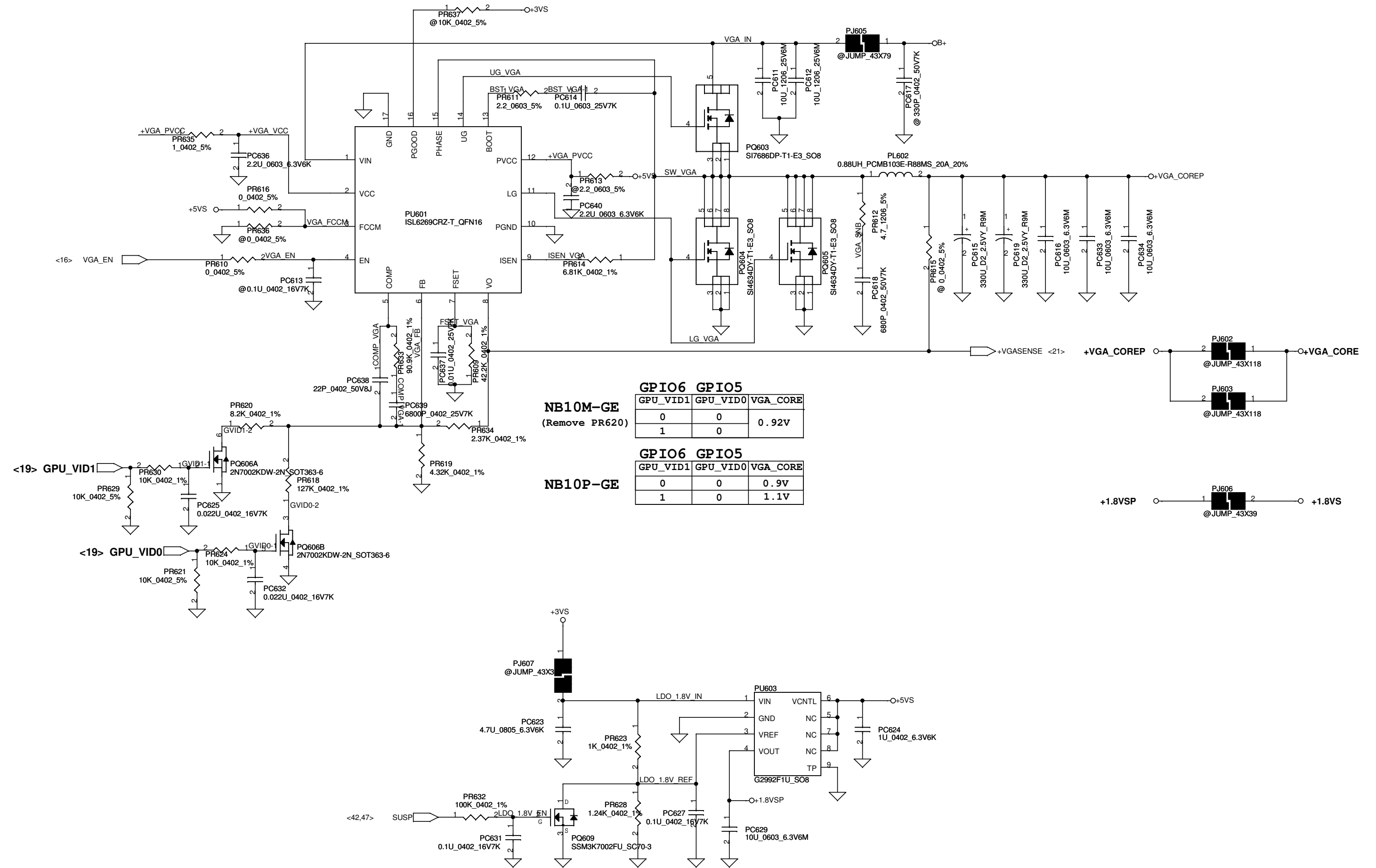
LI-3S : 13.5V ---- BATT-OVP=1.5V
BATT-OVP=0.1112*BATT+



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				0.1	

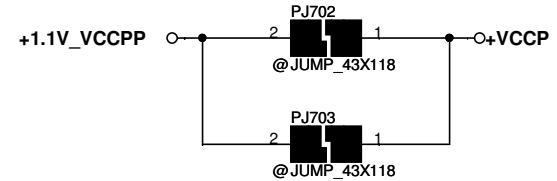
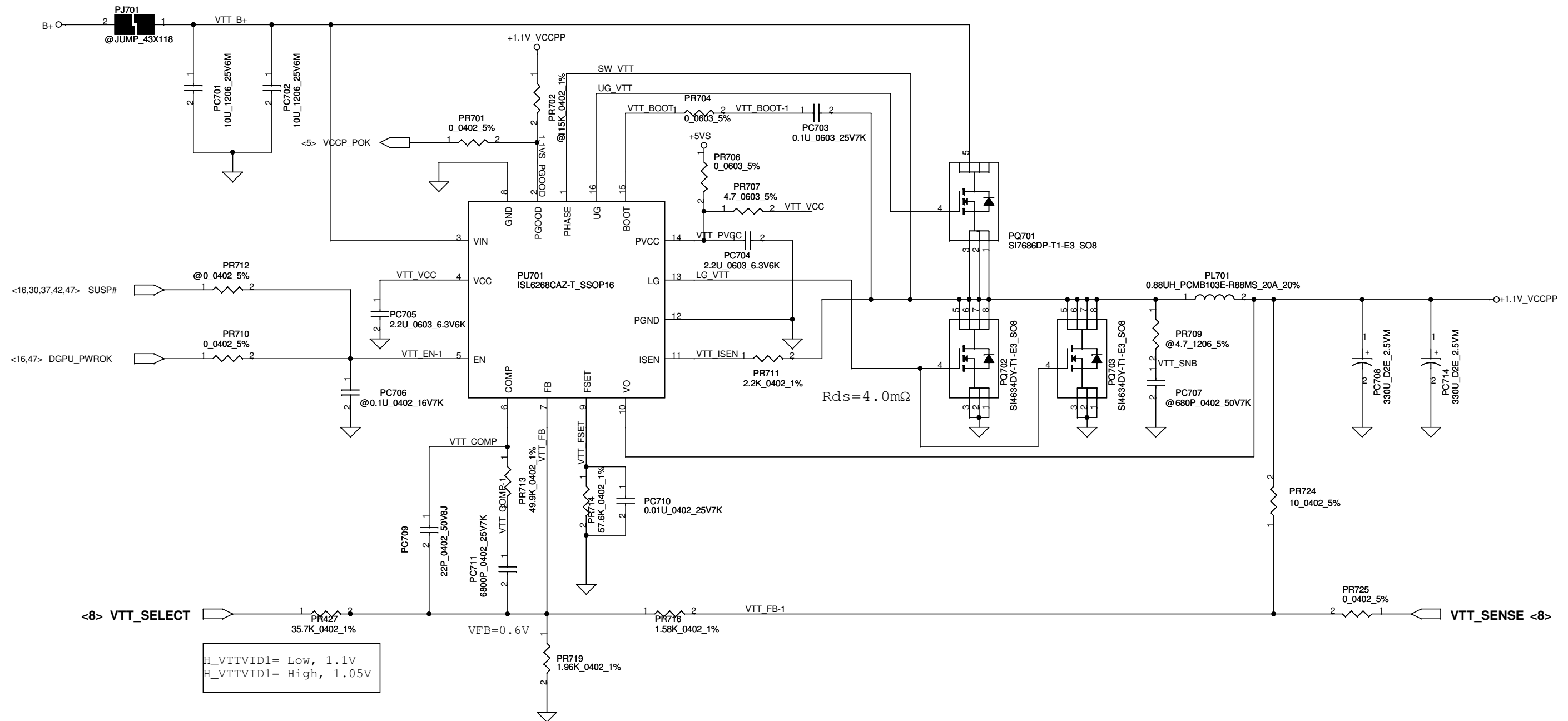


NB10M-GE
(Remove PR620)

GPIO6	GPIO5	VGA_CORE
0	0	0.92V
1	0	0.92V

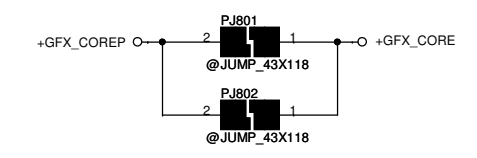
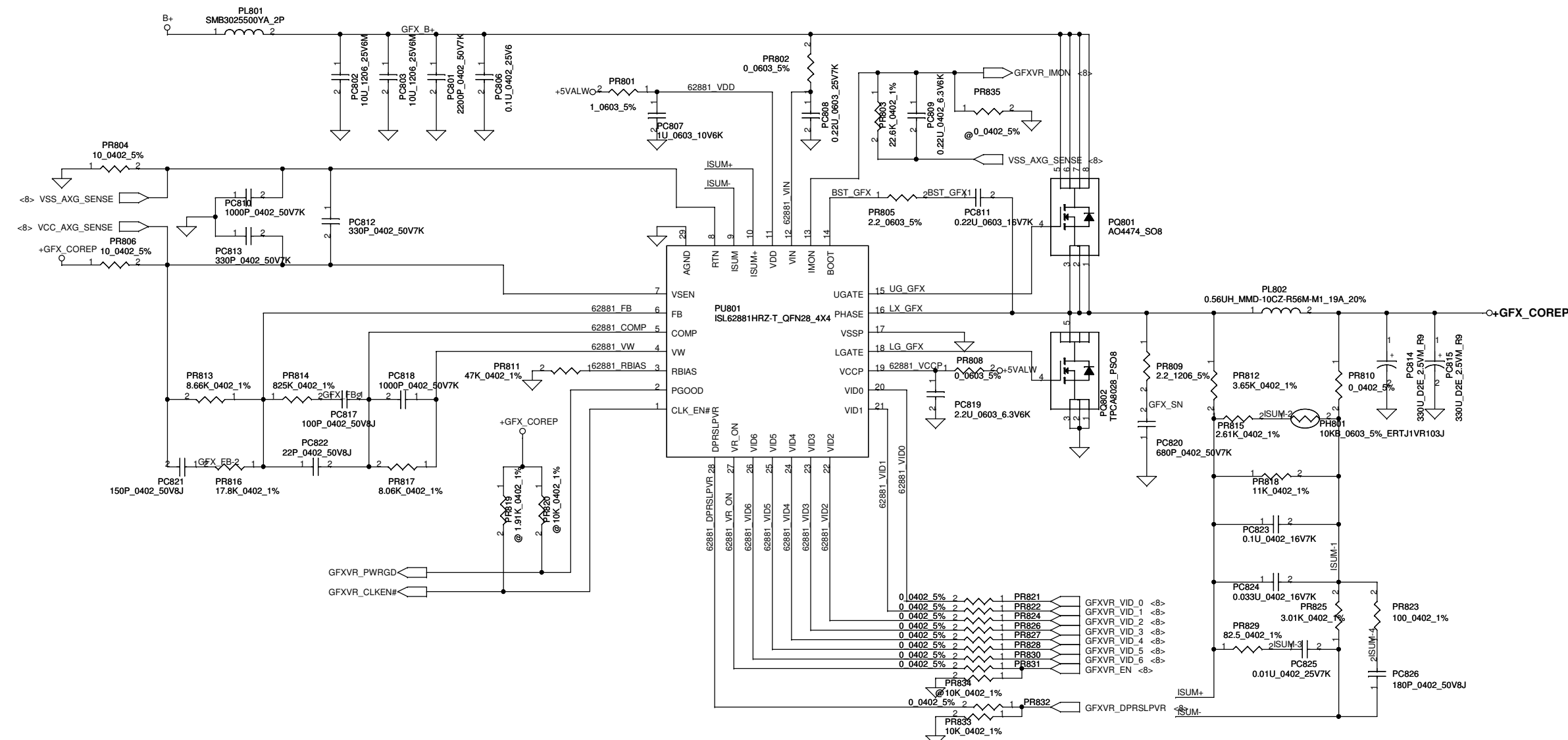
NB10P-GE

GPIO6	GPIO5	VGA_CORE
0	0	0.9V
1	0	1.1V

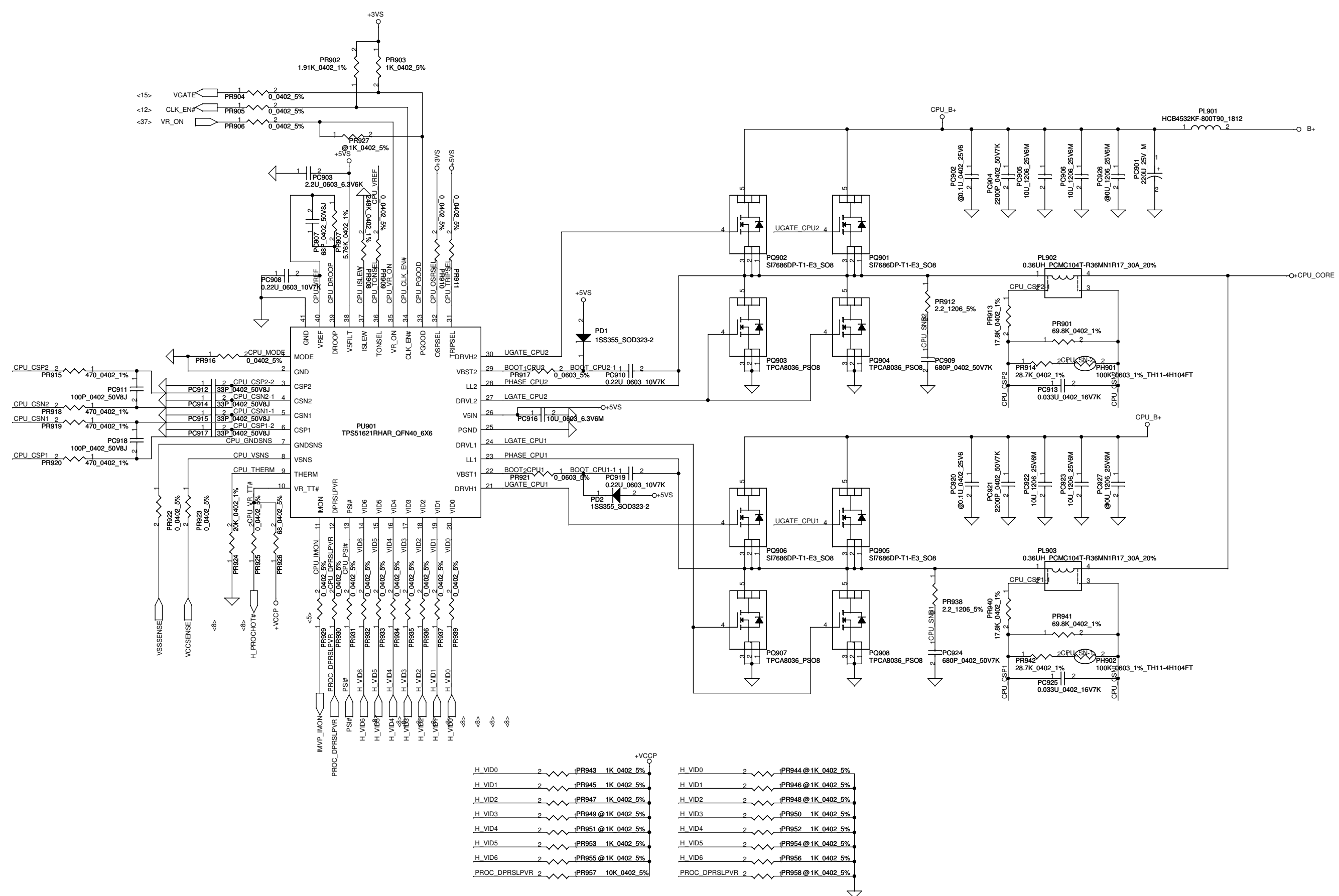


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				Custom
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+1.1VS_VTT		Rev
Document Number		0.1



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H_VID0	2	PR943	1K_0402_5%	H_VID0	2	PR944	@1K_0402_5%
H_VID1	2	PR945	1K_0402_5%	H_VID1	2	PR946	@1K_0402_5%
H_VID2	2	PR947	1K_0402_5%	H_VID2	2	PR948	@1K_0402_5%
H_VID3	2	PR949	@1K_0402_5%	H_VID3	2	PR950	1K_0402_5%
H_VID4	2	PR951	@1K_0402_5%	H_VID4	2	PR952	1K_0402_5%
H_VID5	2	PR953	1K_0402_5%	H_VID5	2	PR954	@1K_0402_5%
H_VID6	2	PR955	@1K_0402_5%	H_VID6	2	PR956	1K_0402_5%
PROC_DPRSPLVVR	2	PR957	10K_0402_5%	PROC_DPRSPLVVR	2	PR958	@1K_0402_5%

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17				20081022	

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				Size Custom
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