

Compal Confidential

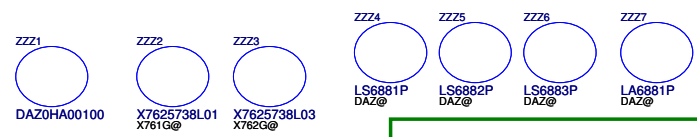
PIQY0 M/B Schematics Document

Intel Sandy Bridge Processor with DDRIII + Cougar Point PCH
nVIDIA N12P-GT

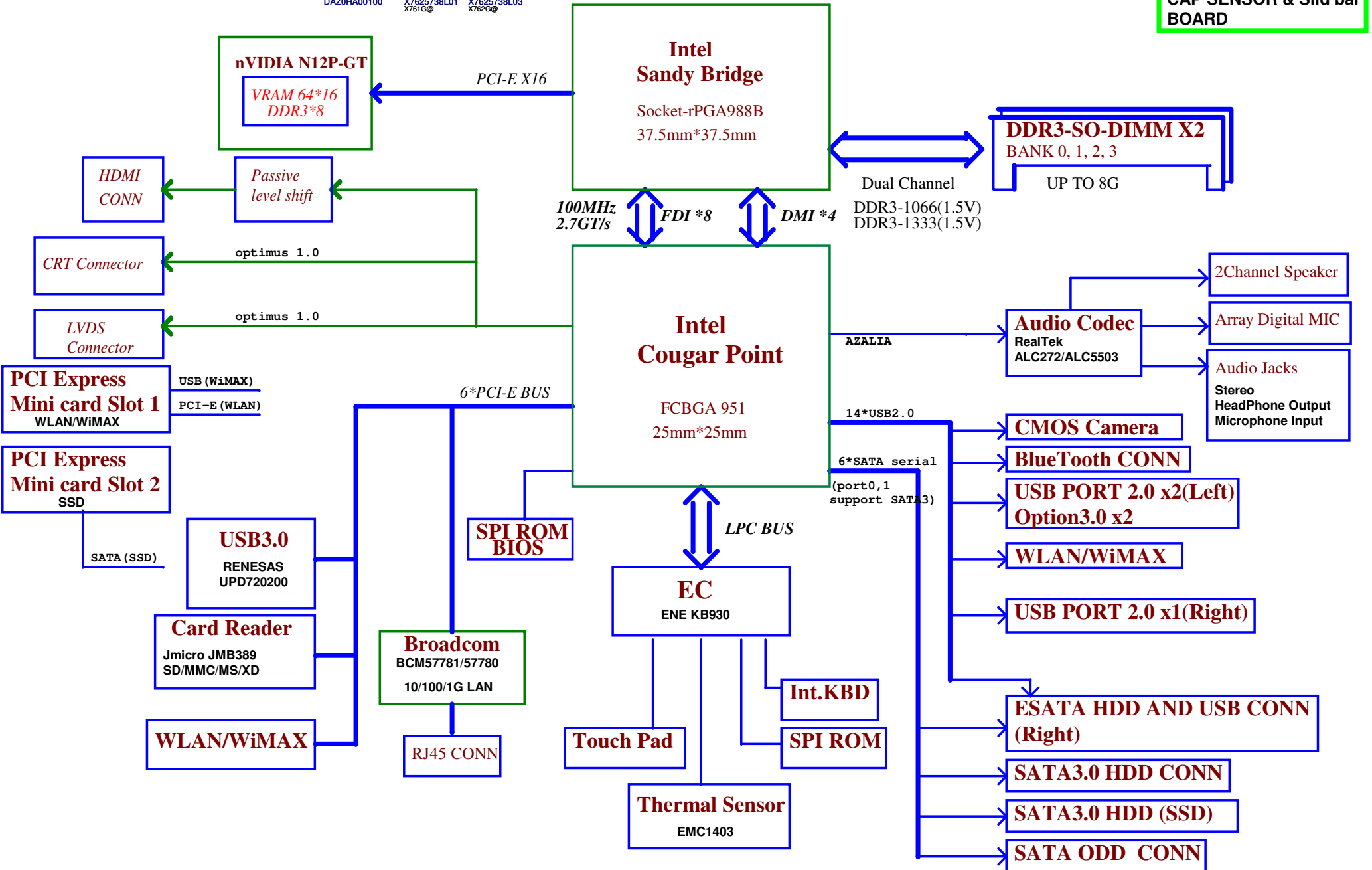
2010-12-30

REV: 1.0

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POWER & ALS BOARD
CAP SENSOR & Slid bar BOARD



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				MB Block Diagram		
				Rev 1.0		

Voltage Rails

power plane	+B	+5VALW	+1.5V	+3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +GFX_CORE +1.8VS +0.75VS +1.05VS
State				
S0	○	○	○	○
S3	○	○	○	✗
S5 S4/AC	○	○	✗	✗
S5 S4/ Battery only	○	✗	✗	✗
S5 S4/AC & Battery don't exist	✗	✗	✗	✗

SMBUS Control Table

	SOURCE	VGA	BATT	KB930	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB930 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB930 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b

EC SM Bus2 address

Device	Address
Thermal Sensor EMC1403-2	1001_101Xb

PCH SM Bus address

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	
2	
3	
4	
5	
6	
7	

USB Port Table

USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB/Cable (Right Side)
		1	USB Port (Right Side COMBO)
	UHCI1	2	USB/B (Left Side)
		3	USB/B (Left Side)
	UHCI2	4	
		5	Camera
EHCI2	UHCI3	6	
		7	
	UHCI4	8	
		9	Mini Card(WLAN)
	UHCI5	10	
		11	
		12	
UHCI6	13	Blue Tooth	

BOM Structure Table

BTO Item	BOM Structure
UMA	
UMA Only	UMA_ONLY@
Optimus	OPTI@
VRAM	X76@
HDMI	HDMI@
Blue Tooth	BT@
USB3.0	USB30@
ESATA	ESATA@
USB Charger	USB_CHG@
No USB Charger	NO_CHG@
Unpop	@
Codec ALC272	272@
Codec ALC5503	5503@
LAN 57781	57781@
LAN 57780	57780@
Ventura Feature	VENTURA@
Camera	CMOS@

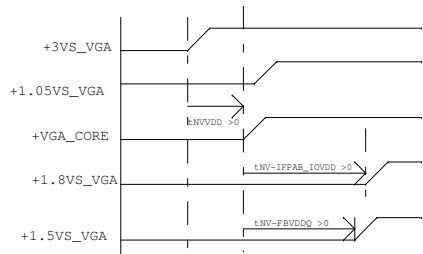
VRAM BOM Config

X761G@: X7625738L01	Samsung 1GB
Sub: X7625738L02	Hynix 1GB
X762G@: X7625738L03	Samsung 2GB
Sub: X7625738L04	Hynix 2GB

GPU BOM Config

N12P SKU:	OPTI@
GS SKU:	GS@
GT SKU:	GT@

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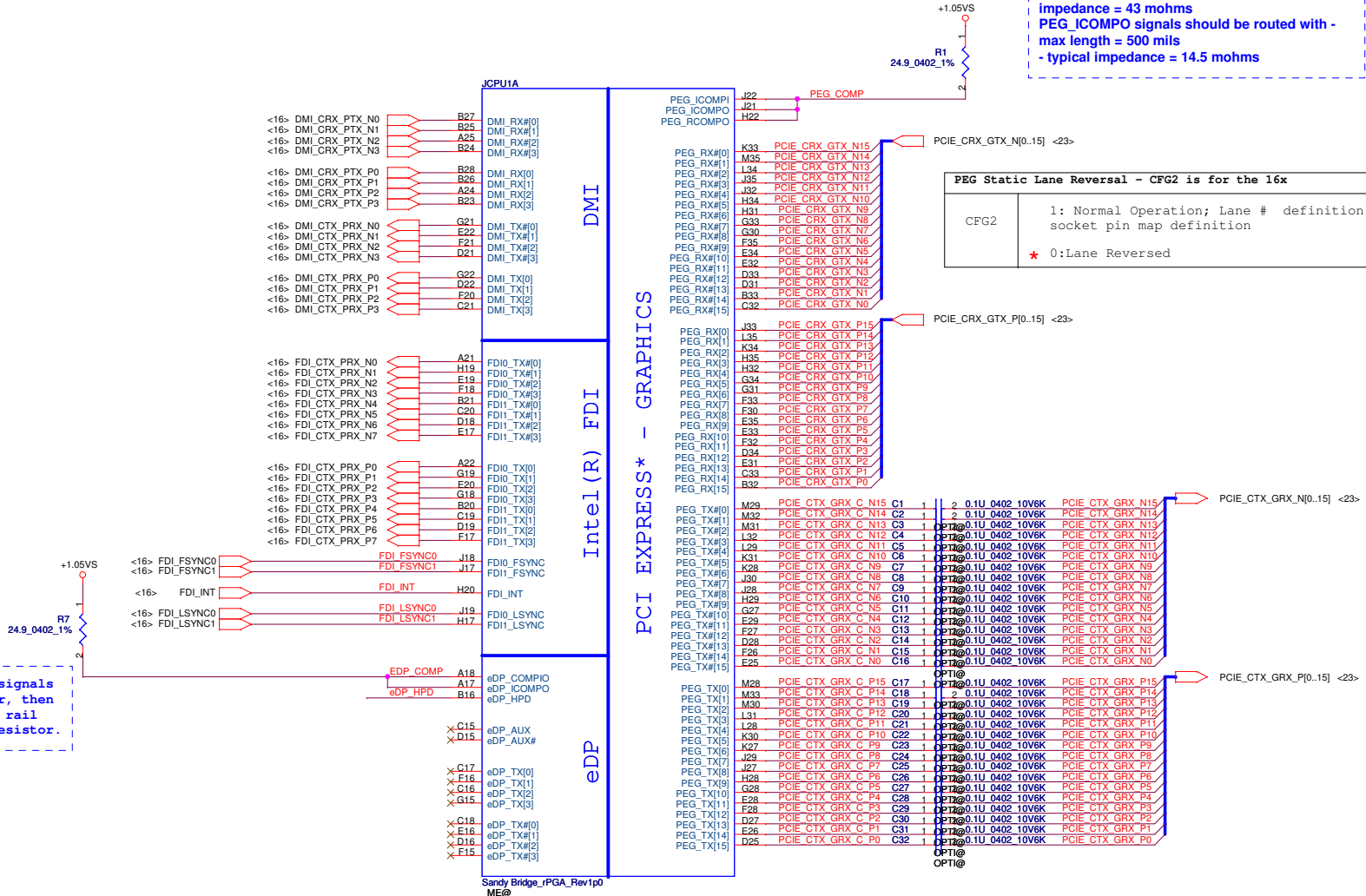


1. The ramp rate for any rail must be more than 40us.
2. +VGA_CORE <= +3VS_VGA +0.5V
3. +1.5VS_VGA <= +3VS_VGA +0.5V
4. Optimus follows power sequencing rules specified in discrete GPU design guide.

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2010/11/30		2011/08		VGA Notes List	
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eDP_COMPIO and ICOMPO signals should be tied together, then connected to the VCCIO rail via a single 24.9ohm resistor.

PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms
 PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 mohms



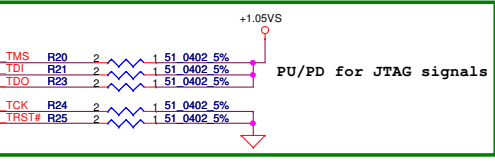
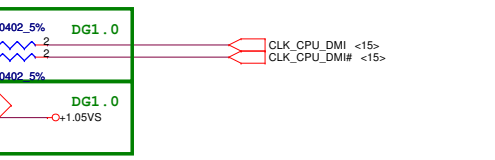
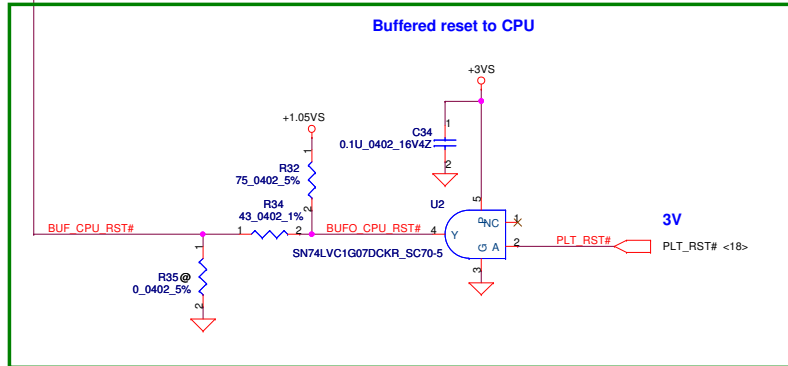
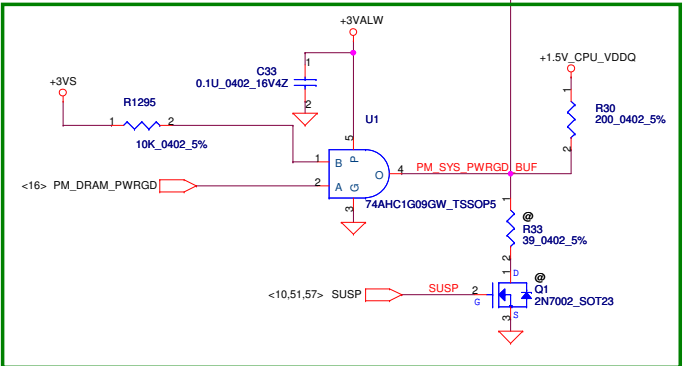
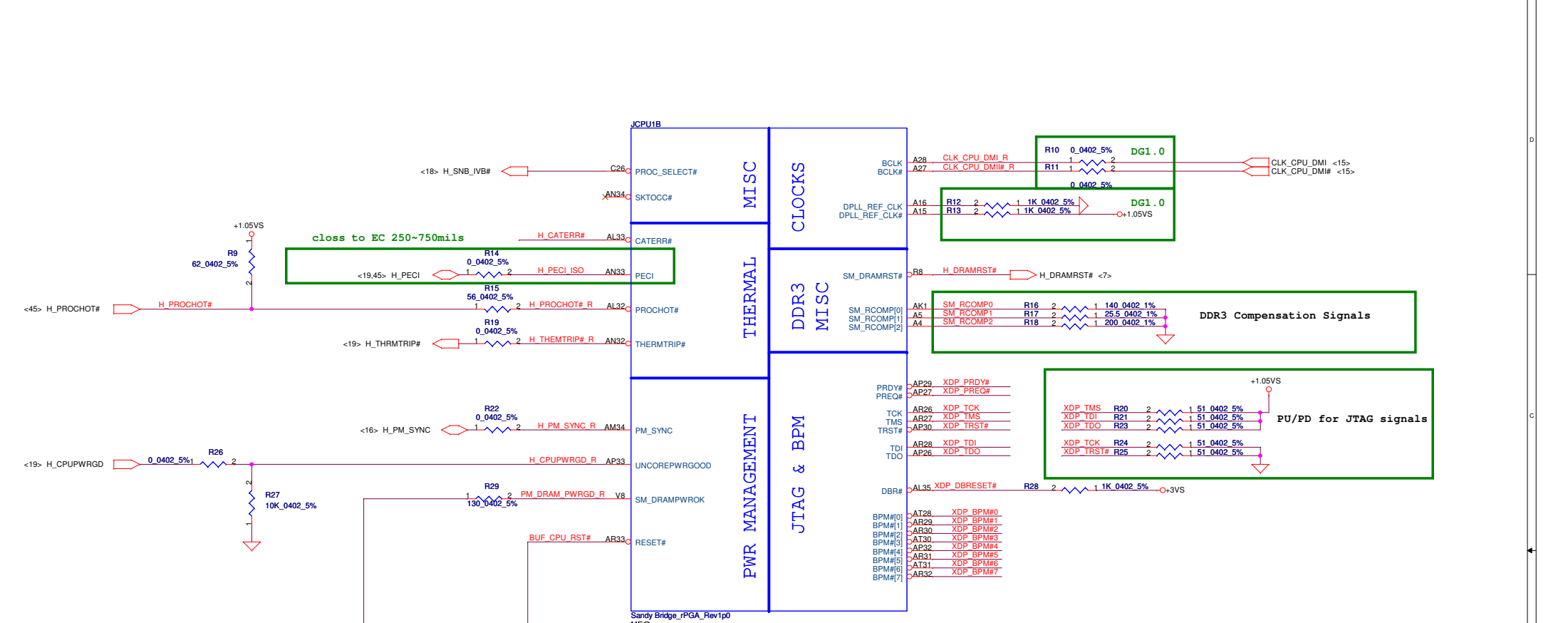
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	Definition
1	Normal Operation; Lane # definition matches socket pin map definition
* 0	Lane Reversed

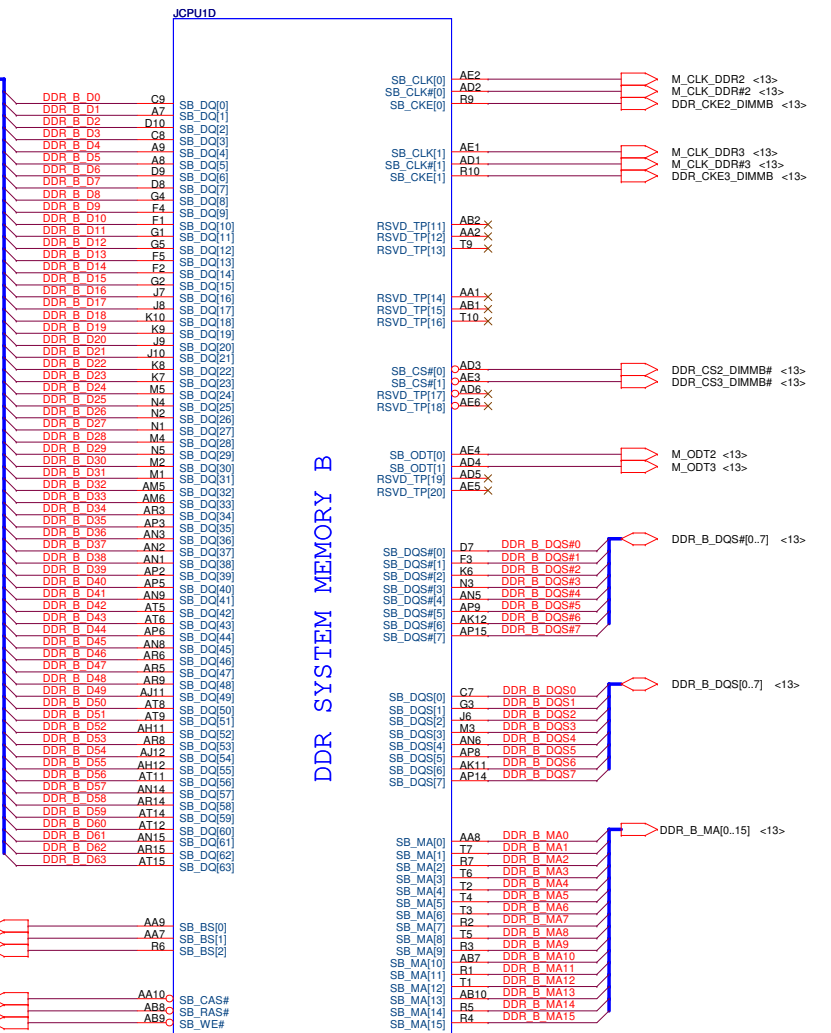
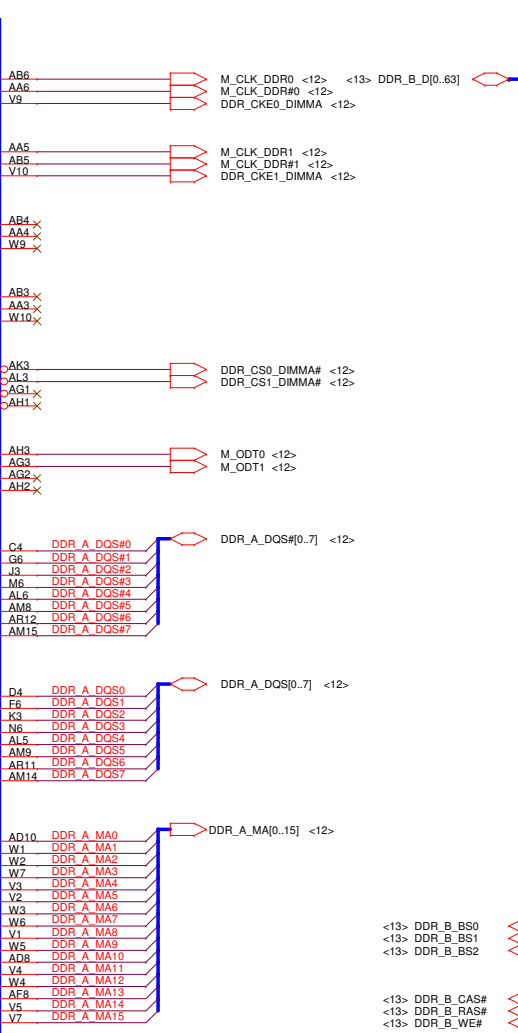
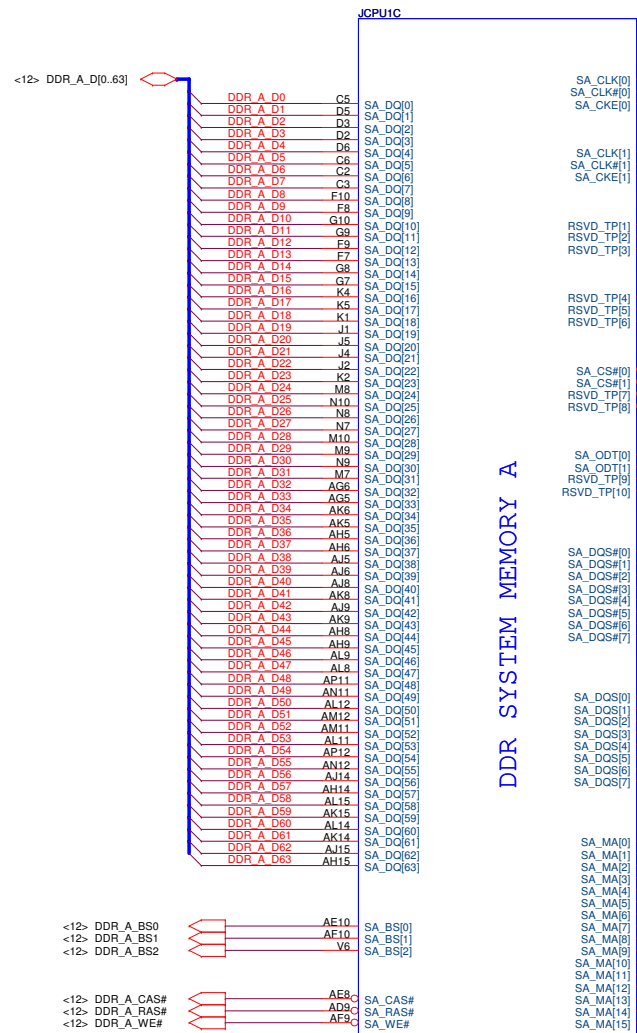
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Title PROCESSOR(I7) DMI,FDI,PEG		
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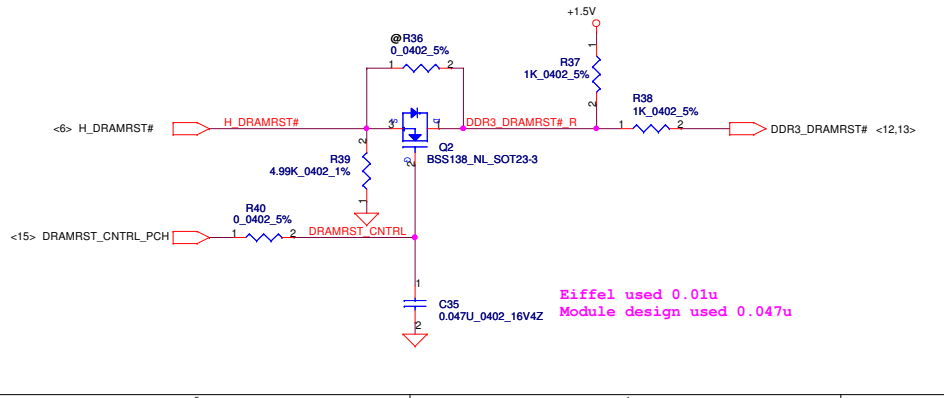


DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B

Sandy Bridge_rPGA_Rev1p0
ME@

Sandy Bridge_rPGA_Rev1p0
ME@

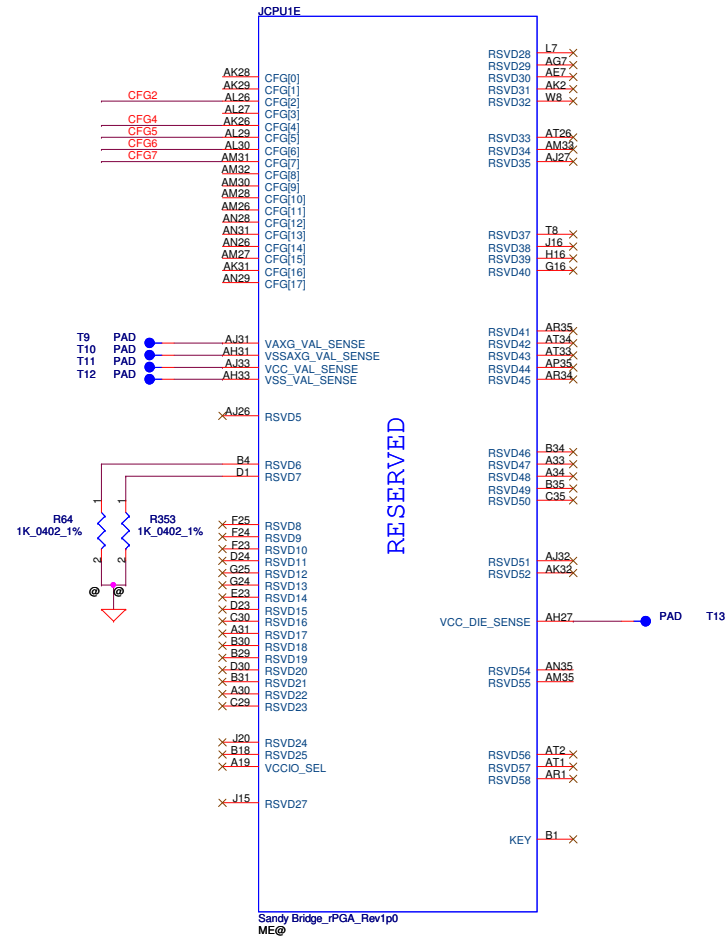


Eiffel used 0.01u
Module design used 0.047u

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Title PROCESSOR(3/7) DDRIII	
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CFG Straps for Processor



PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition * 0: Lane Reversed
------	--

Display Port Presence Strap

CFG4	* 1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port
------	--

PCIE Port Bifurcation Straps

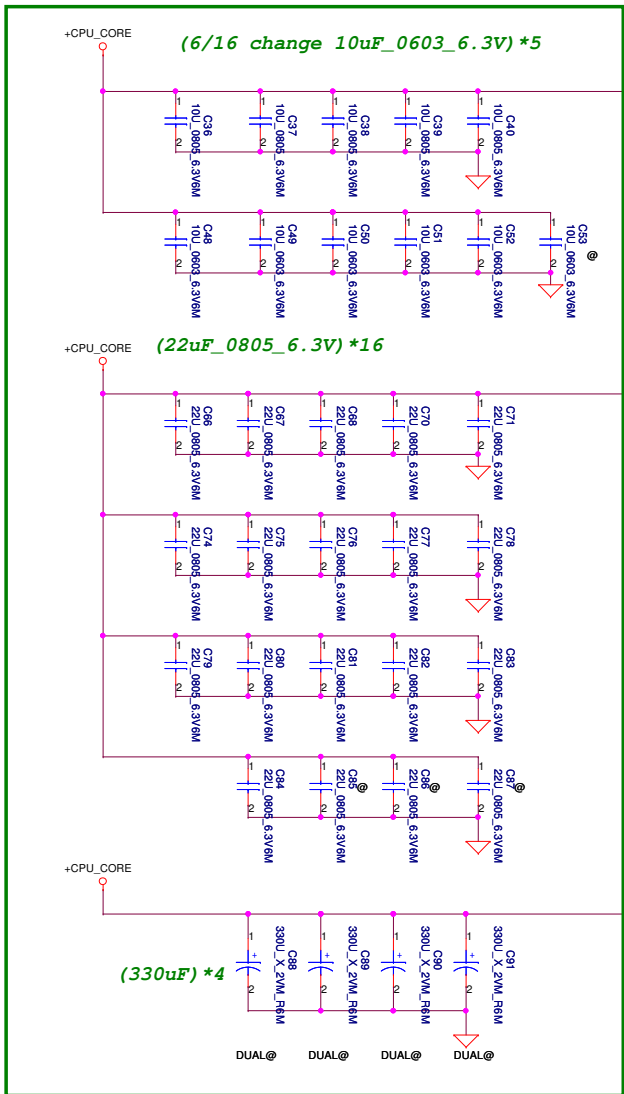
CFG[6:5]	* 11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
----------	--

PEG DEFER TRAINING

CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
------	---

POWER

JCPU1F



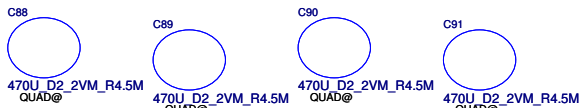
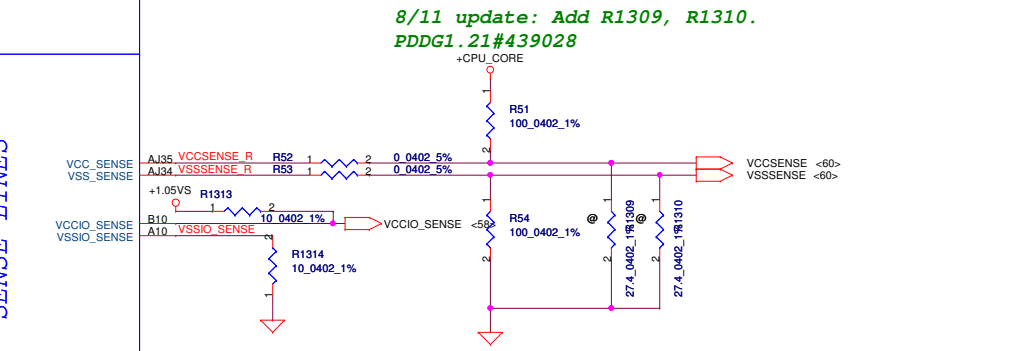
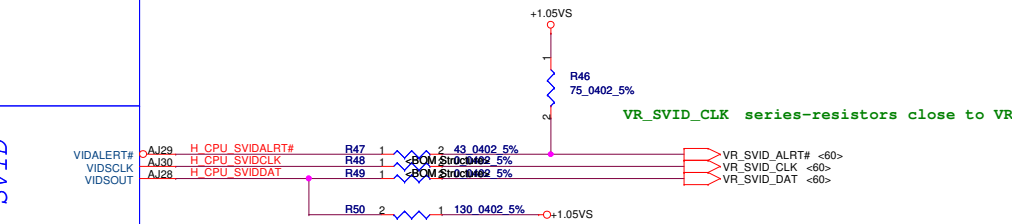
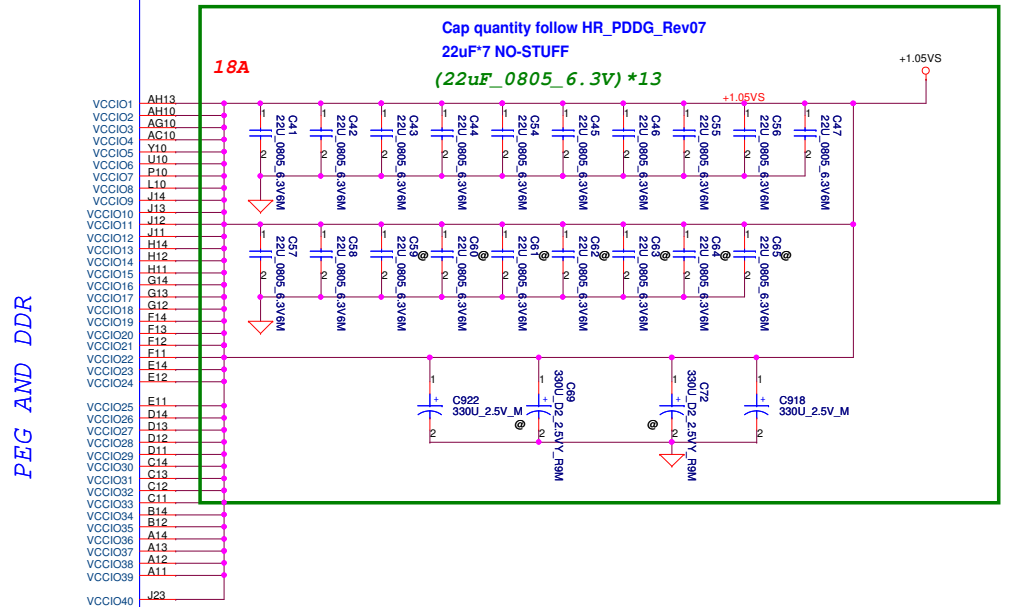
QC=94A
DC=53A

- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AF26 VCC20
- AD35 VCC21
- AD34 VCC22
- AD33 VCC23
- AD32 VCC24
- AD31 VCC25
- AD30 VCC26
- AD29 VCC27
- AD28 VCC28
- AD27 VCC29
- AD26 VCC30
- AC35 VCC31
- AC34 VCC32
- AC33 VCC33
- AC32 VCC34
- AC31 VCC35
- AC30 VCC36
- AC29 VCC37
- AC28 VCC38
- AC27 VCC39
- AC26 VCC40
- AA35 VCC41
- AA34 VCC42
- AA33 VCC43
- AA32 VCC44
- AA31 VCC45
- AA30 VCC46
- AA29 VCC47
- AA28 VCC48
- AA27 VCC49
- AA26 VCC50
- Y35 VCC51
- Y34 VCC52
- Y33 VCC53
- Y32 VCC54
- Y31 VCC55
- Y30 VCC56
- Y29 VCC57
- Y28 VCC58
- Y27 VCC59
- Y26 VCC60
- V35 VCC61
- V34 VCC62
- V33 VCC63
- V32 VCC64
- V31 VCC65
- V30 VCC66
- V29 VCC67
- V28 VCC68
- V27 VCC69
- V26 VCC70
- U35 VCC71
- U34 VCC72
- U33 VCC73
- U32 VCC74
- U31 VCC75
- U30 VCC76
- U29 VCC77
- U28 VCC78
- U27 VCC79
- U26 VCC80
- U25 VCC81
- R35 VCC82
- R34 VCC83
- R33 VCC84
- R32 VCC85
- R31 VCC86
- R30 VCC87
- R29 VCC88
- R28 VCC89
- R27 VCC90
- R26 VCC91
- R25 VCC92
- R24 VCC93
- R23 VCC94
- P33 VCC95
- P32 VCC96
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- P28 VCC99
- P27 VCC100
- P26 VCC100

CORE SUPPLY

SVIID

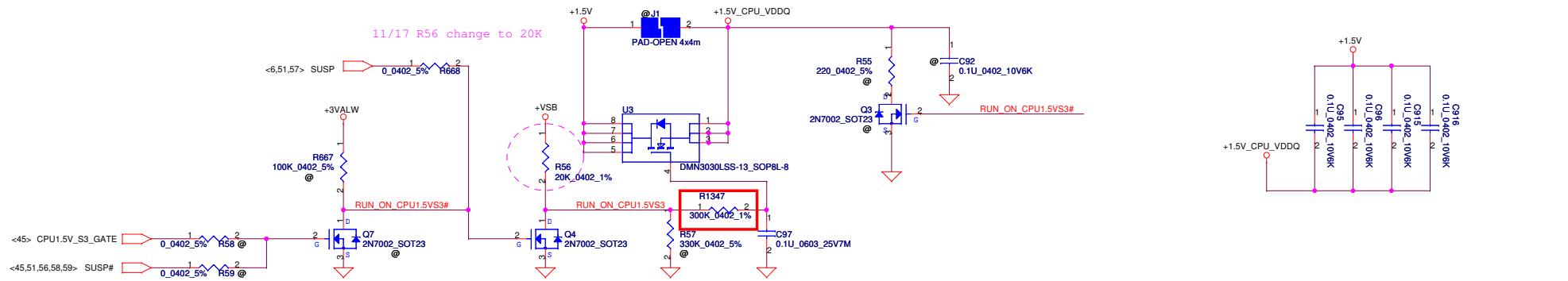
SENSE LINES



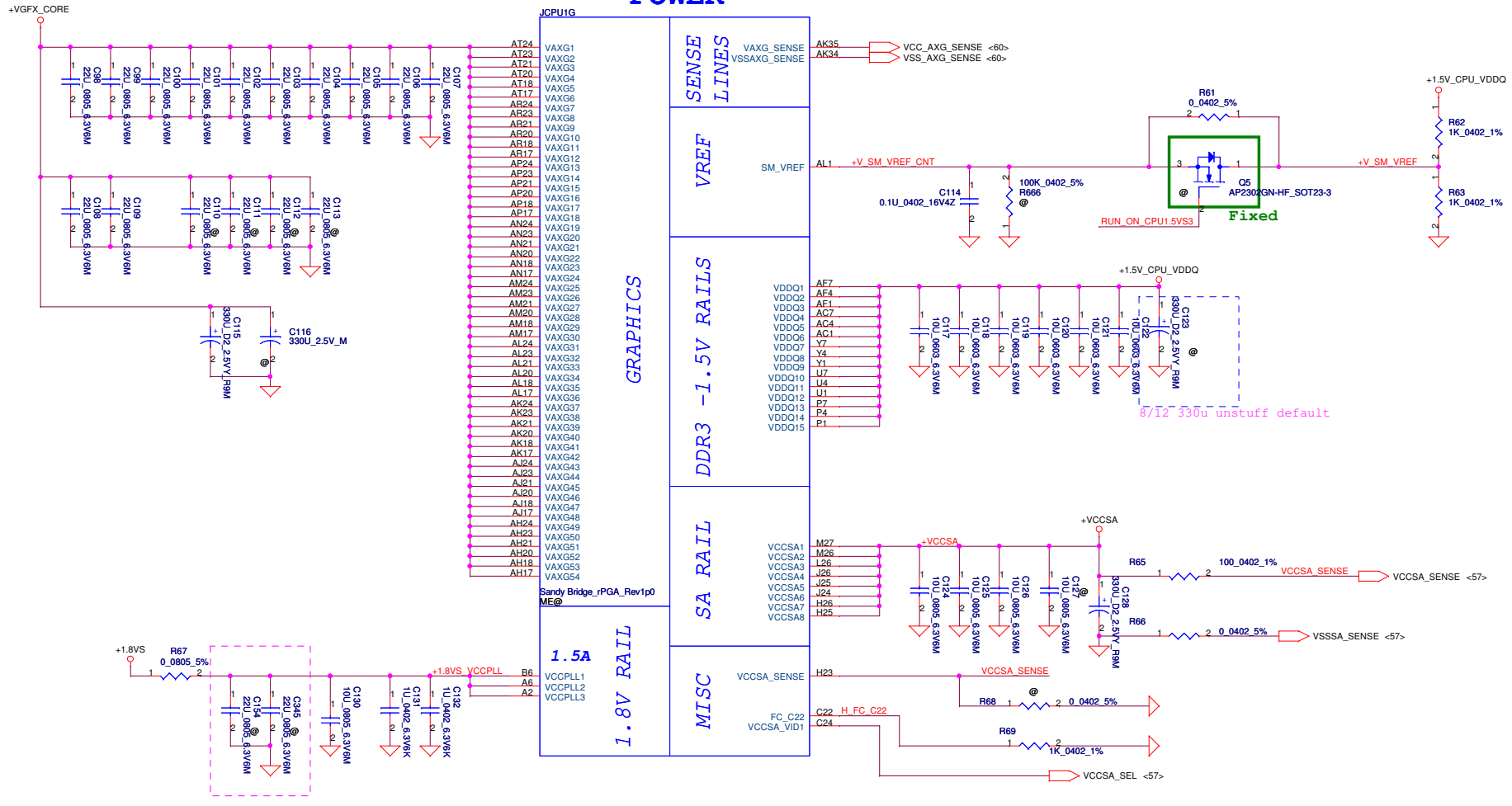
Sandy Bridge_PPGA Rev1A ME@

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PROCESSOR(S/7) PWR,BYPASS			
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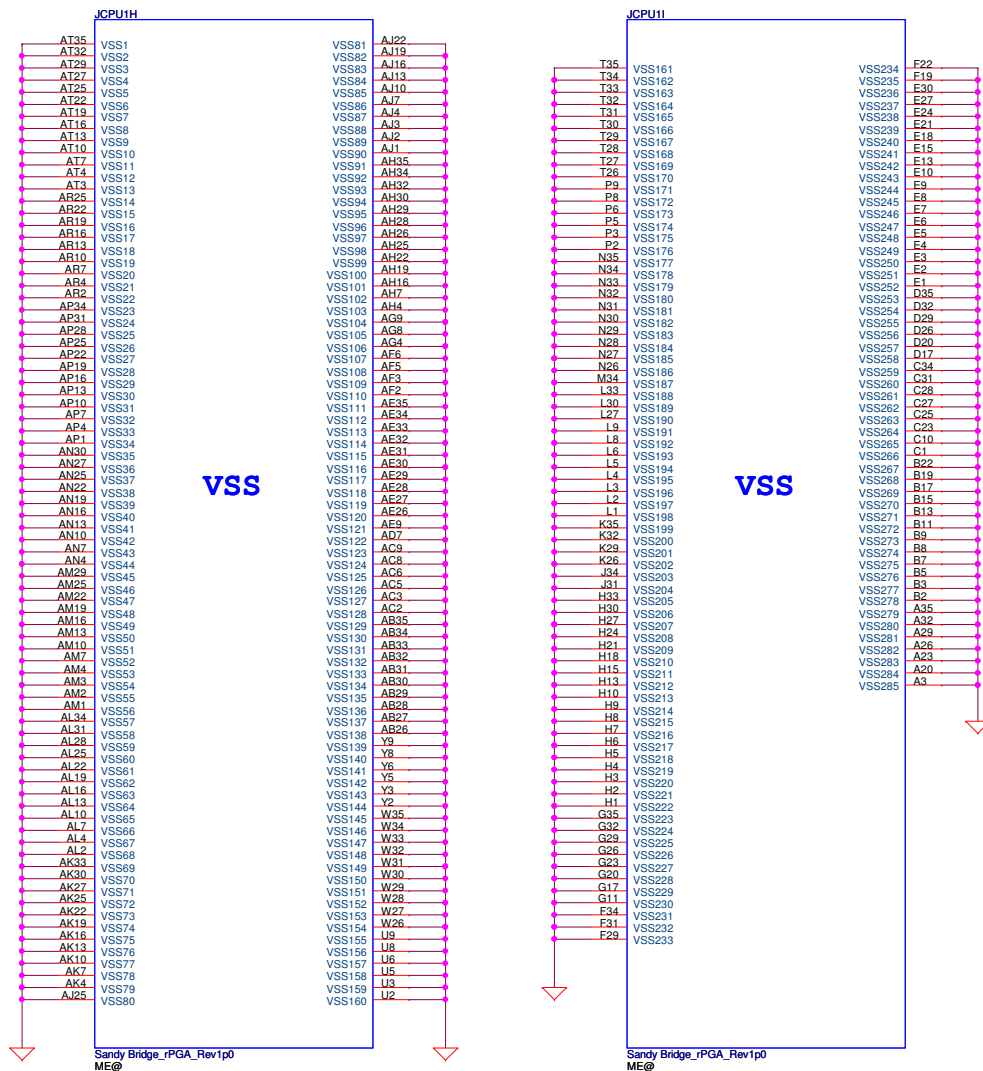
POWER



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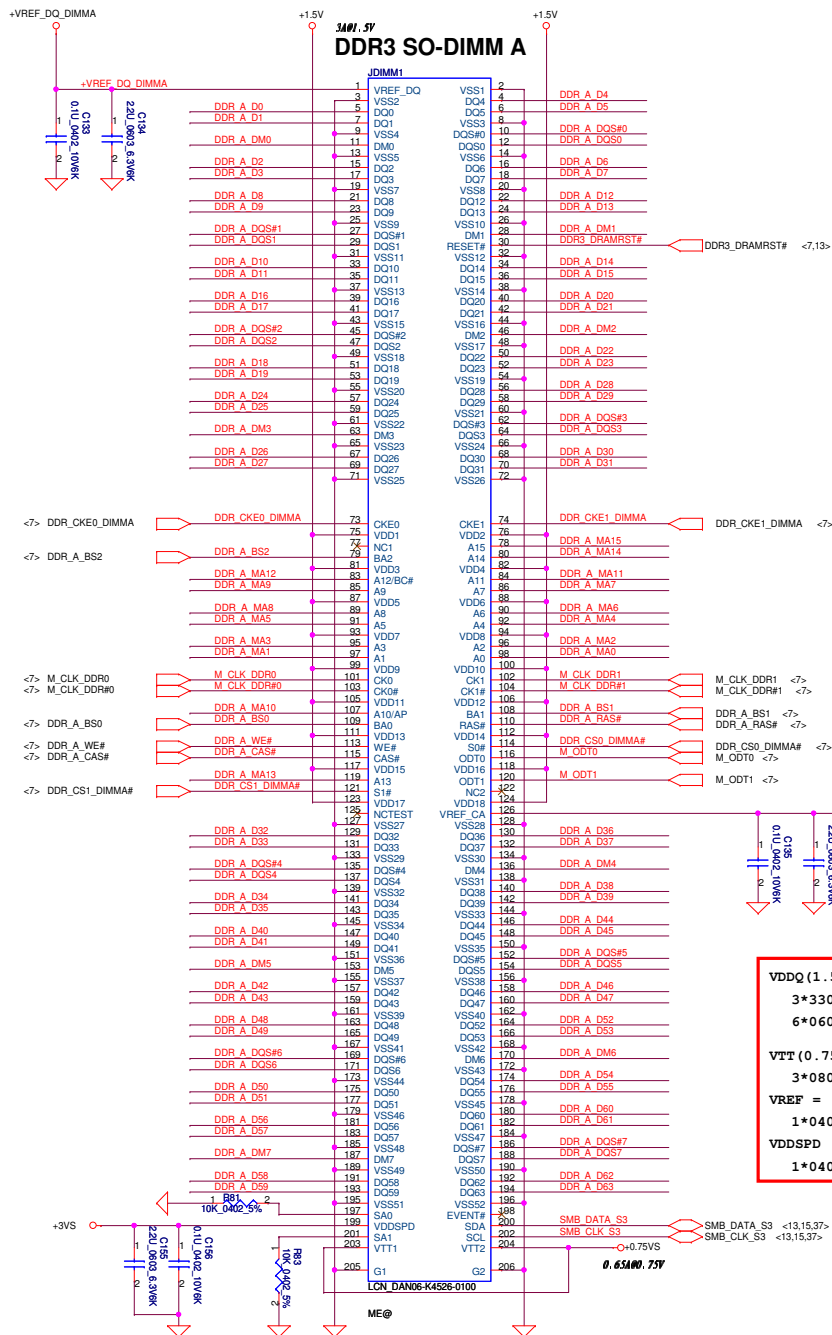
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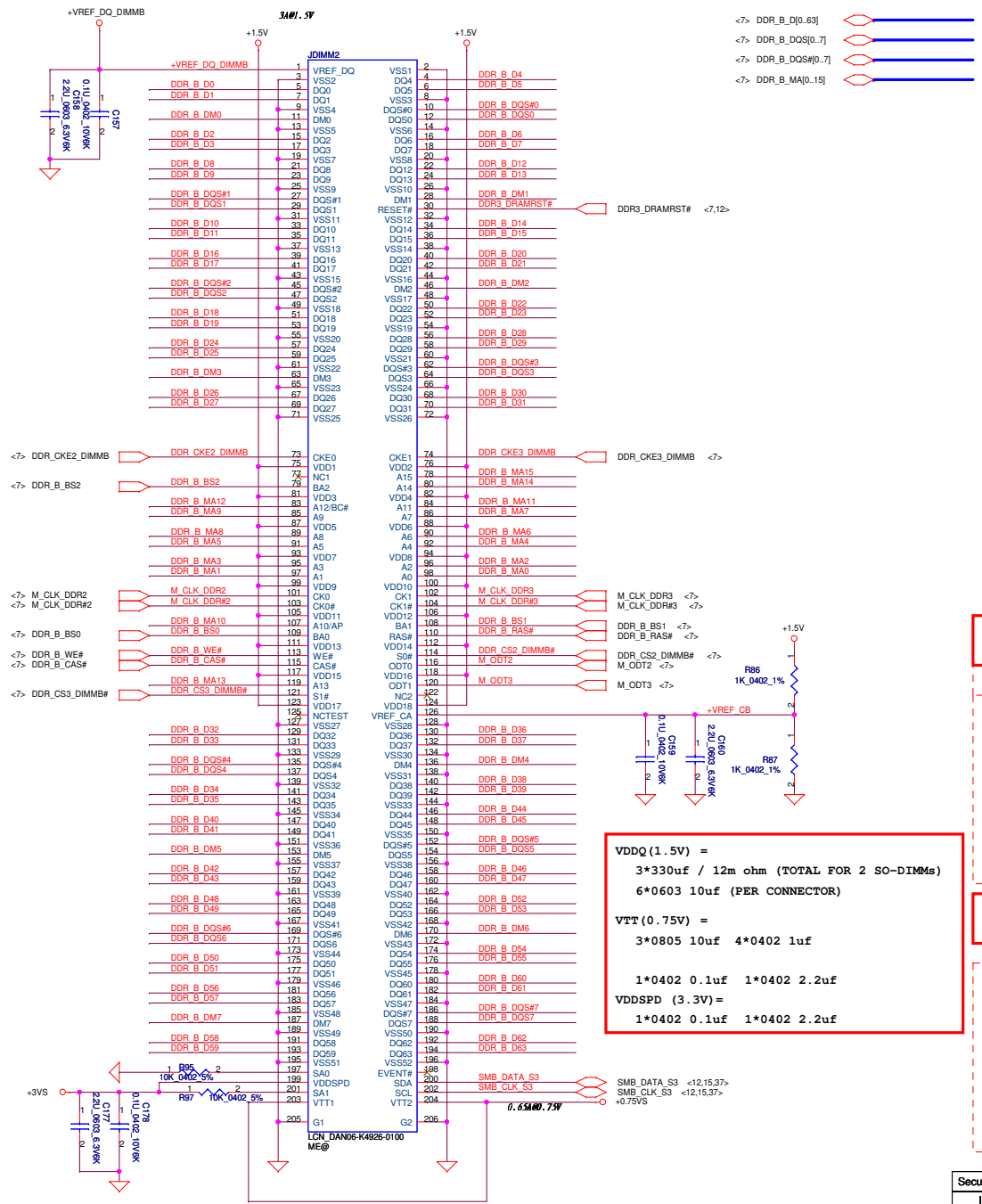


Sandy Bridge_rPGA_Rev1p0
ME@

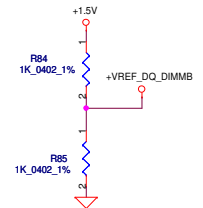
Sandy Bridge_rPGA_Rev1p0
ME@

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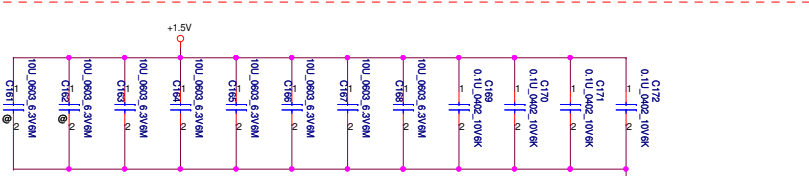




For Arranale only +VREF_DQ_DIMMB supply from a external 1.5V voltage divide circuit.
07/17/2009



Layout Note: Place near DIMM
(10uF_0603_6.3V) * 8
(0.1uF_402_10V) * 4



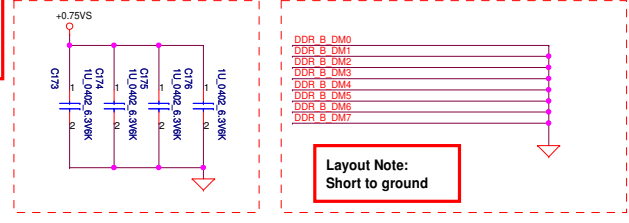
VDDQ (1.5V) =
3*330uF / 12m ohm (TOTAL FOR 2 SO-DIMMS)
6*0603 10uF (PER CONNECTOR)

VTT (0.75V) =
3*0805 10uF 4*0402 1uF

1*0402 0.1uF 1*0402 2.2uF

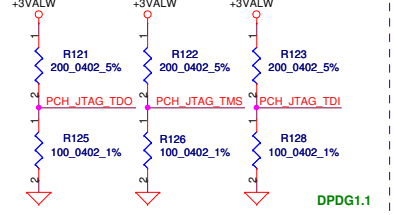
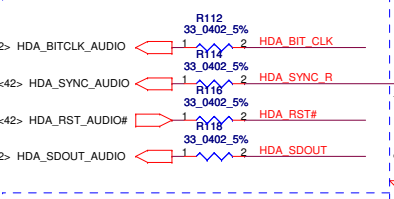
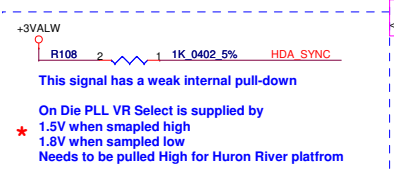
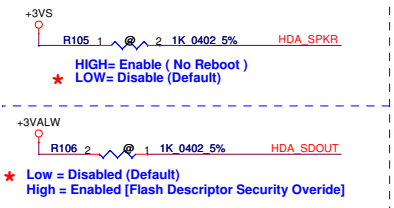
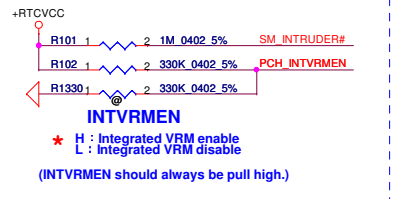
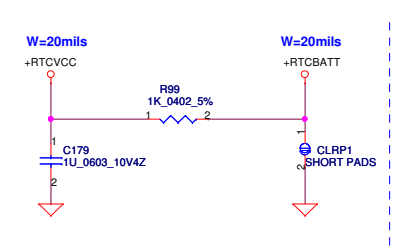
VDDSPD (3.3V) =
1*0402 0.1uF 1*0402 2.2uF

Layout Note: Place near DIMM

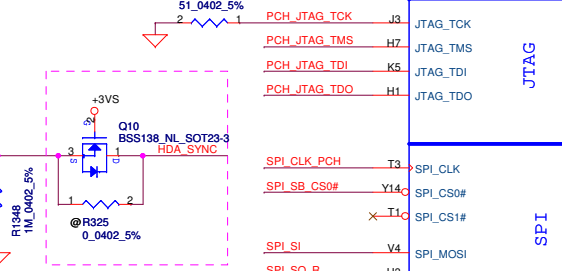
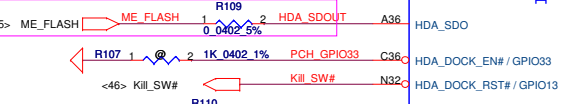
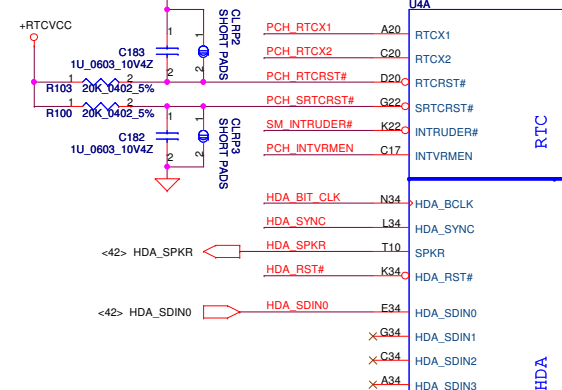
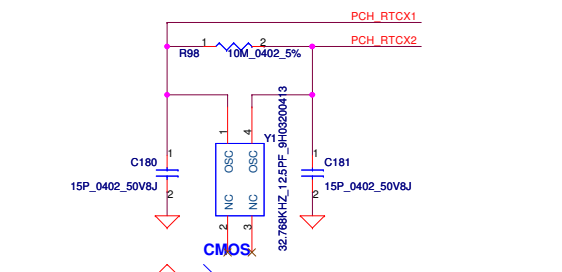


Layout Note: Short to ground

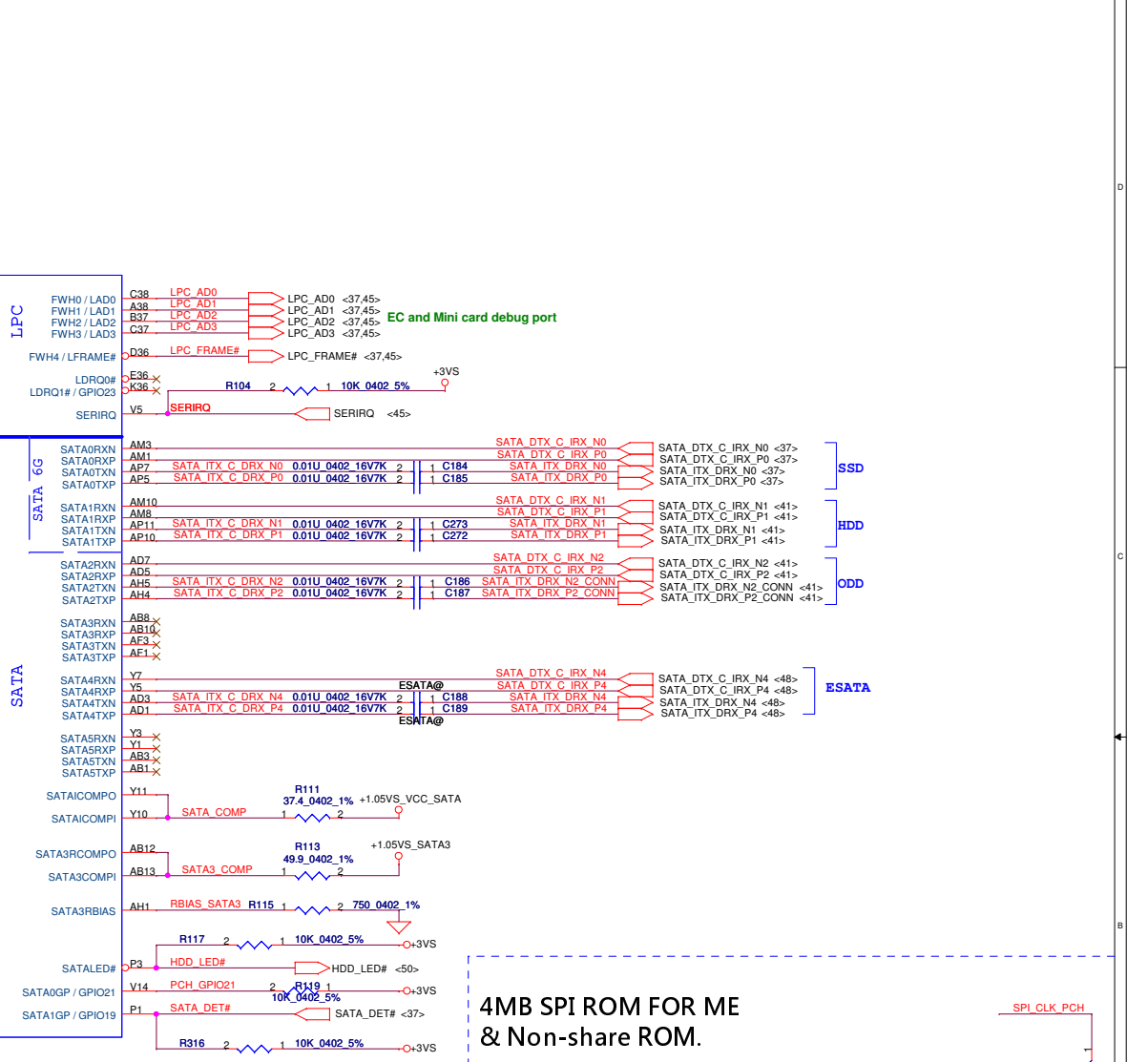
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Issued Date	2010/11/30	Deciphered Date	2011/08	
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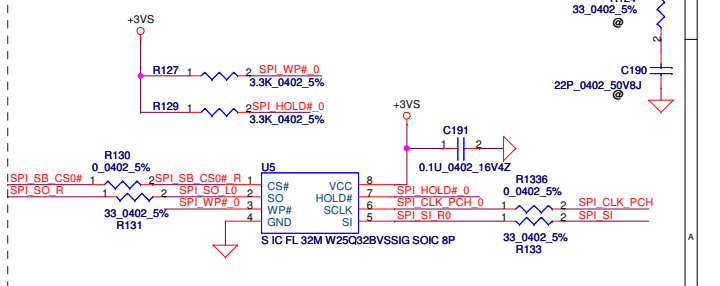
6/30 update R121, R122, R123



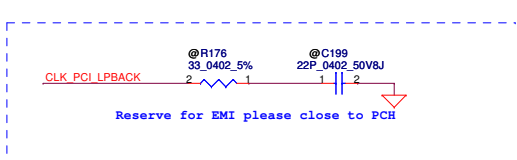
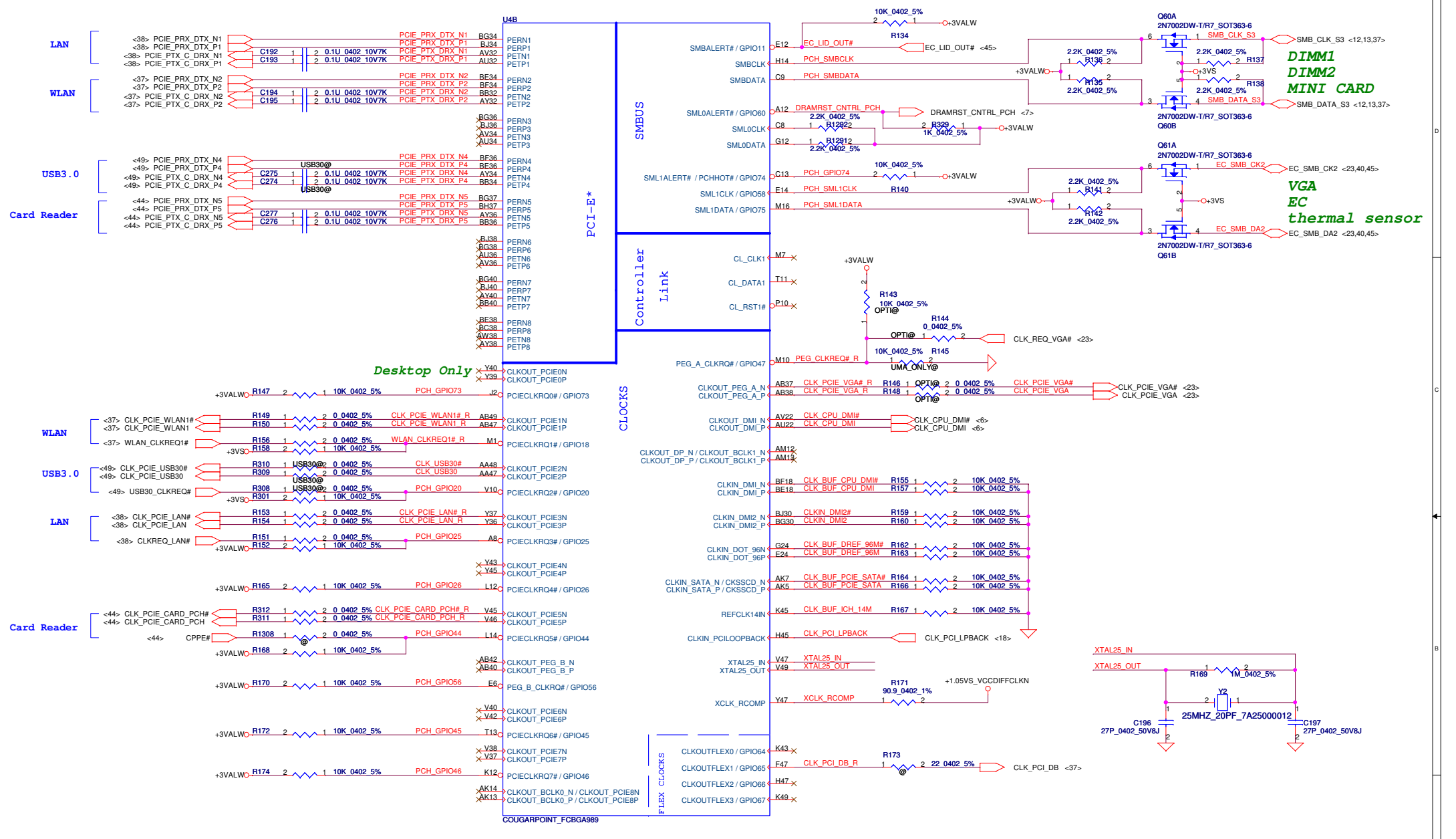
6/17 follow module design



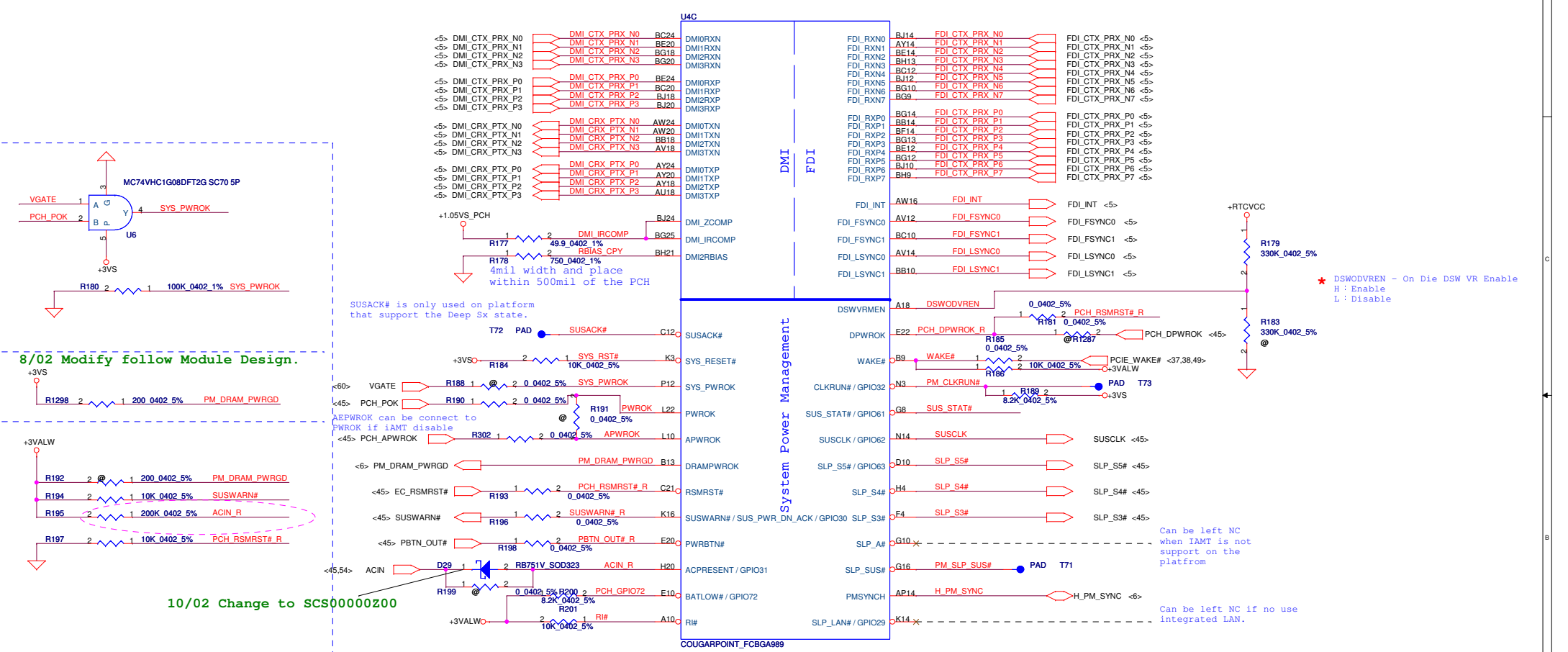
4MB SPI ROM FOR ME & Non-share ROM.



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				Sheet	of
				14	63



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				Date	Wednesday, January 05, 2011
				Sheet	15 of 63



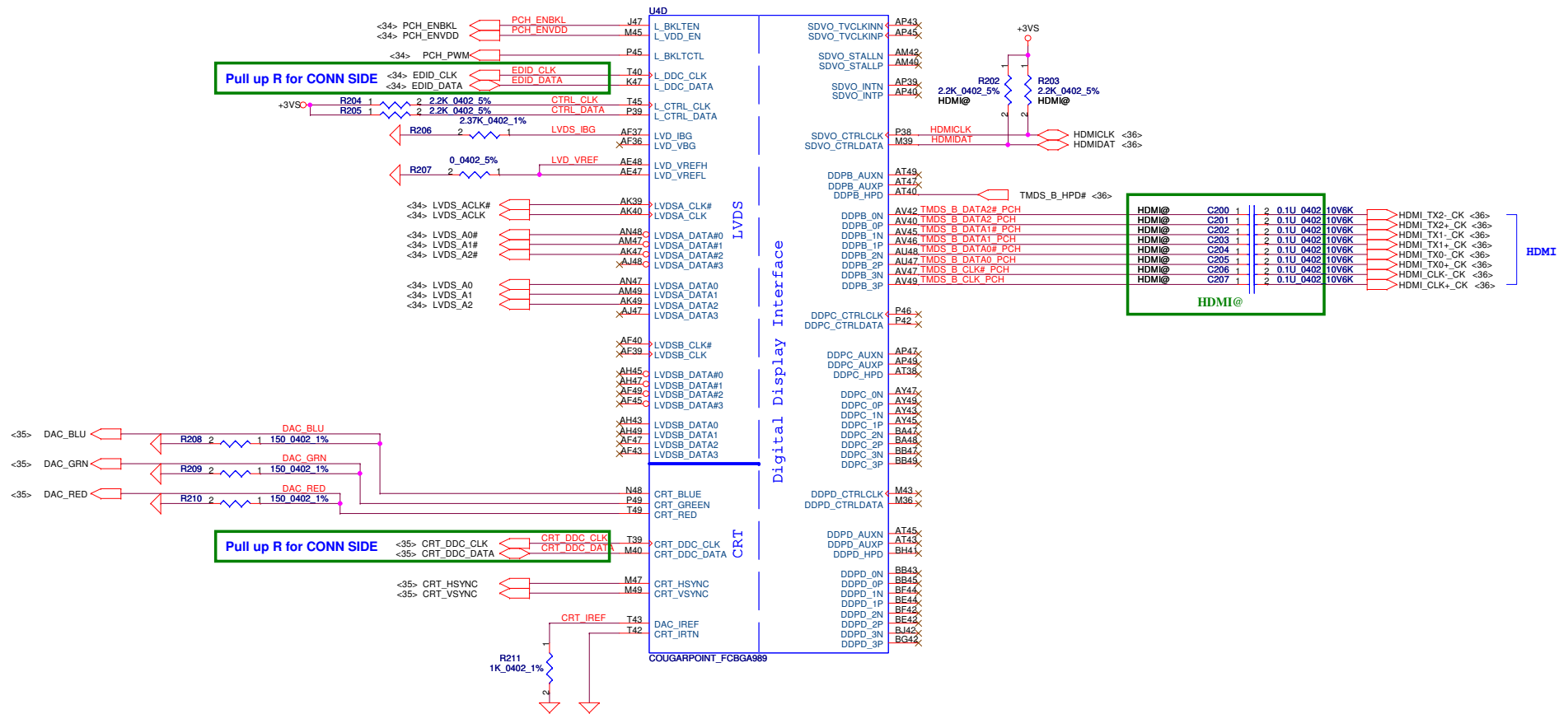
Security Classification		Compal Secret Data		Title	
Issued Date	2010/11/30	Deciphered Date	2011/08	PCH (3/8) DMI, FDI, PM,	
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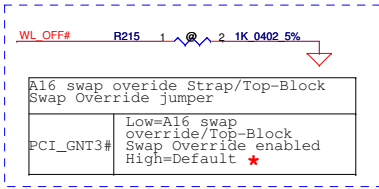
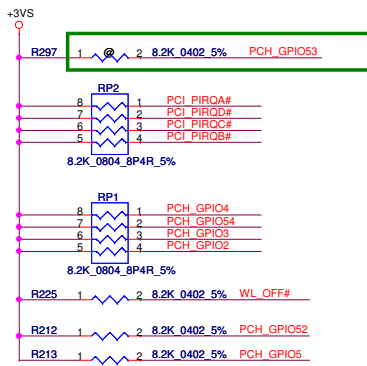
PCH (3/8) DMI, FDI, PM,

PIQYO LA6881P

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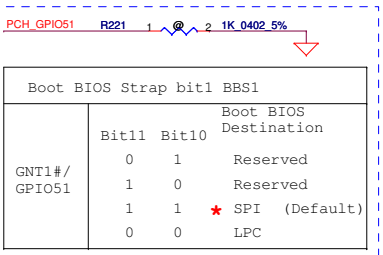


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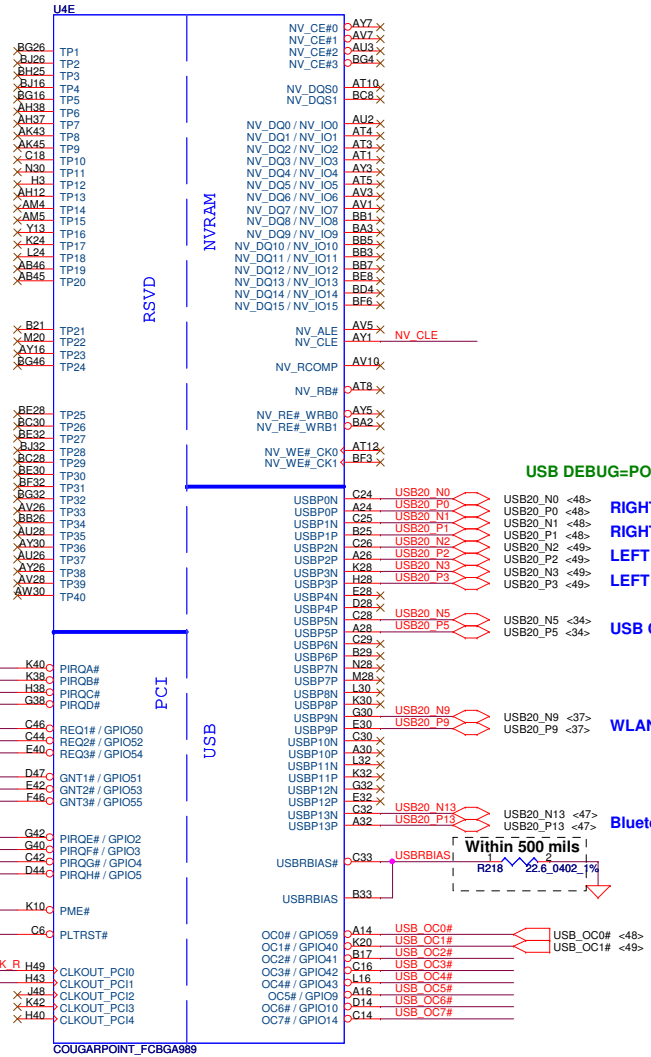


A16 swap override Strap/Top-Block Swap Override jumper		
PCI_GNT1#	Low=A16 swap override/Top-Block Swap Override enabled	High=Default

GPIO53=This Signal has a weak internal pull-up.
NOTE: The internal pull-up is disabled after PLTRST# deasserts.



Boot BIOS Strap bit1 BBS1			
	Bit11	Bit10	Boot BIOS Destination
GNT1# / GPIO51	0	1	Reserved
	1	0	Reserved
	1	1	* SPI (Default)
	0	0	LPC



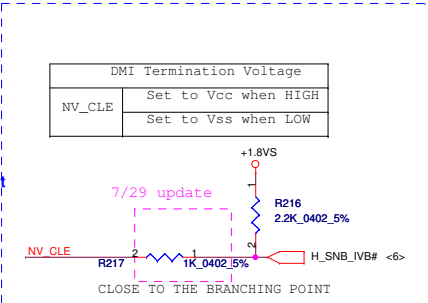
USB DEBUG=PORT1 AND PORT9

RIGHT USB (CABLE) for SW request
RIGHT USB (COMBO)
LEFT USB
LEFT USB

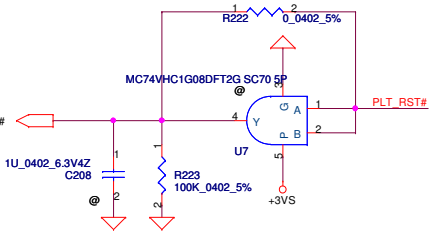
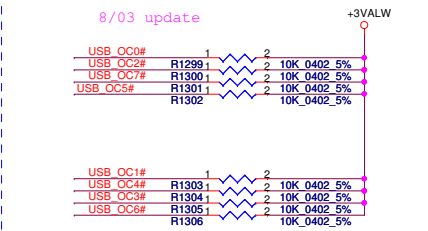
USB Camera

WLAN

Bluetooth



DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW



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PCH (5/9) PCI, USB			
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6/24 Change to @ follow module design and double check on module design meeting

ICC_EN#
Integrated Clock Chip Enable
H ; Disable
L ; Enable
★ ; Enable
R235 1 @ 2 1K 0402 5% EC_SMI# <37,38,44> DEVICE_RST#
Weak internal pull-high

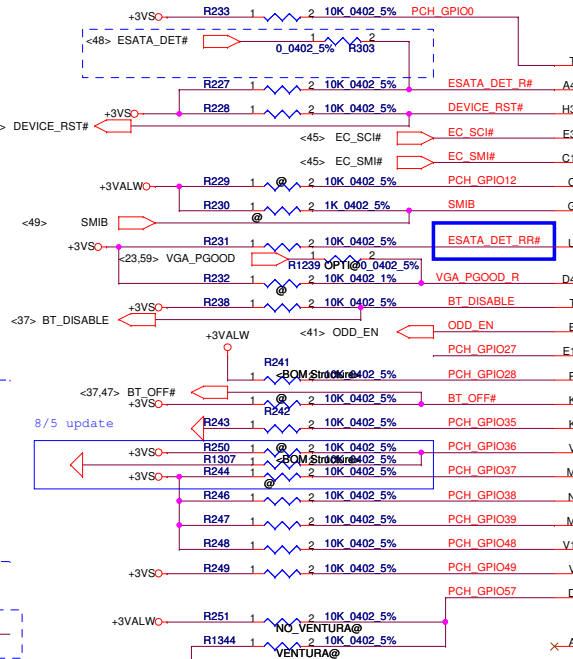
GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
★ H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable
R240 1 @ 2 1K 0402 5% PCH_GPIO28

PCH_GPIO27 (Have internal Pull-High)
★ High: VCCVRM VR Enable
Low: VCCVRM VR Disable
R245 1 @ 2 10K 0402 5% PCH_GPIO27

7/29 update for ESATA detect
R1294 1 @ 2 10K 0402 5% ESATA_DET_RR#
ESATA_DET#

0812 Checklist Rev.1.2
When Unused as GPIO or SATA*GP - Use 8.2K-10K pull-down to ground.
R1311 1 @ 2 10K 0402 5% PCH_GPIO37

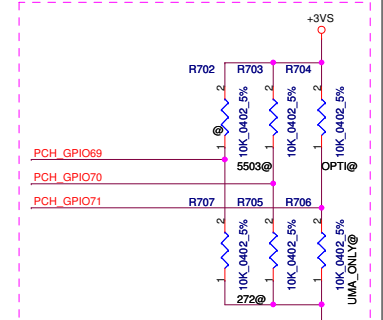
7/29 update for ESATA detect



8/5 update

GPIO		CPU/MISC		NCTF	
UJF	BMBUS# / GPIO0	TACH4 / GPIO68	C40	PCH_GPIO68	
	TACH1 / GPIO1	TACH5 / GPIO69	B41	PCH_GPIO69	
	TACH2 / GPIO6	TACH6 / GPIO70	C41	PCH_GPIO70	
	TACH3 / GPIO7	TACH7 / GPIO71	A40	PCH_GPIO71	
	GPIO8				
	LAN_PHY_PWR_CTRL / GPIO12				
	GPIO15				
	SATA4GP / GPIO16				
	TACH0 / GPIO17				
	SCLOCK / GPIO22				
	GPIO24 / MEM_LED				
	GPIO27				
	GPIO28				
	STP_PCIF# / GPIO34				
	GPIO35				
	SATA2GP / GPIO36				
	SATA3GP / GPIO37				
	SLOAD / GPIO38				
	SDATAOUT0 / GPIO39				
	SDATAOUT1 / GPIO48				
	SATA5GP / GPIO49				
	GPIO57				
	VSS_NCTF_1		BG2		
	VSS_NCTF_2		BG48		
	VSS_NCTF_3		BH3		
	VSS_NCTF_4		BH47		
	VSS_NCTF_5		BH4		
	VSS_NCTF_6		BJ44		
	VSS_NCTF_7		BJ45		
	VSS_NCTF_8		BJ46		
	VSS_NCTF_9		BJ5		
	VSS_NCTF_10		BJ6		
	VSS_NCTF_11		C2		
	VSS_NCTF_12		C48		
	VSS_NCTF_13		D1		
	VSS_NCTF_14		D49		
			E1		
			E49		
			F1		
			F49		

COUGARPOINT_FCBGA989

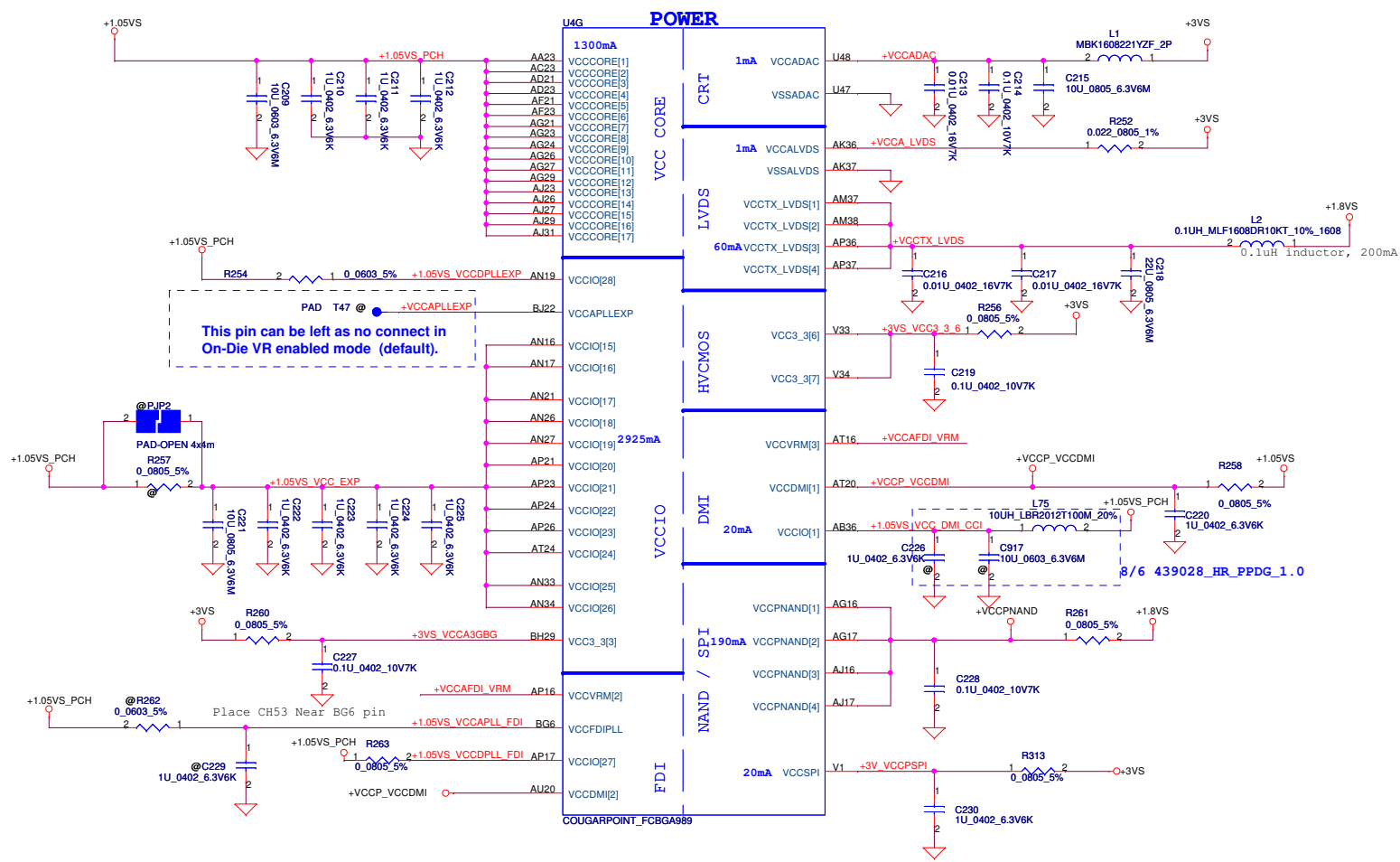


6/23 update for MB ID

INIF3_BV
This signal has weak internal BU, can't pull low.
Intel schematic review recommend.

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Compal Electronics, Inc.		
Title PCH (6/9) GPIO, CPU, MISC		
Size	Document Number	Rev
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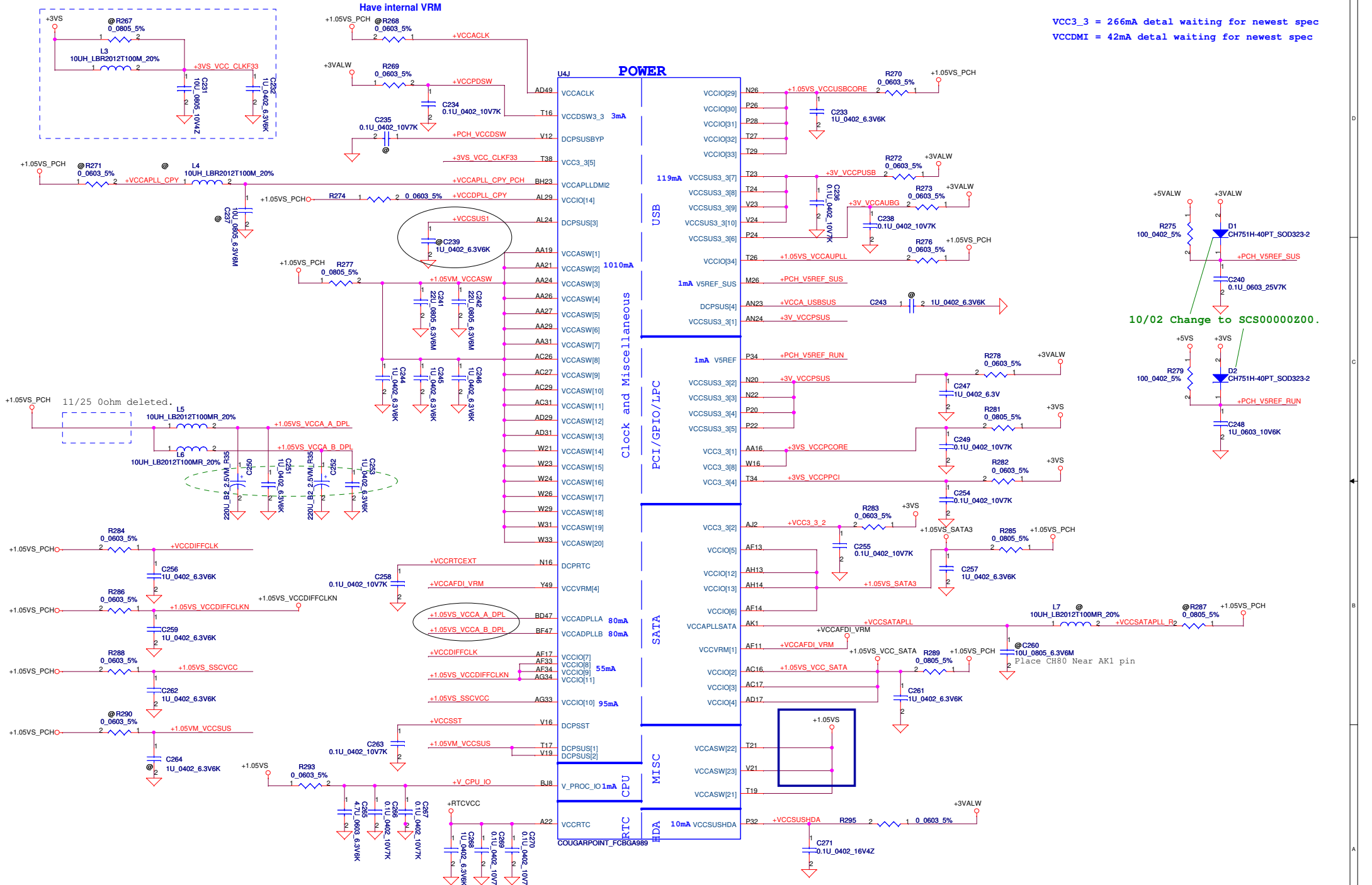
PAD T47 @ **-VCCAPLLEXP**
 This pin can be left as no connect in On-Die VR enabled mode (default).

+1.5VS **+VCCAFDI_VRM**
 R265 0.0603 5%
 Intel HR_PDDG_1.21
 1.5S rail. Default is to populate to enable VccVRM.
 VCCVRM = 160mA detail waiting for newest spec

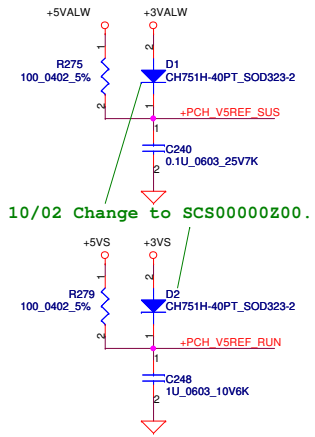
PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLLA	1.05	0.08
VccADPLLB	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

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PCH (719) PWR
 Document Number: **PIQY0 LA6881P**
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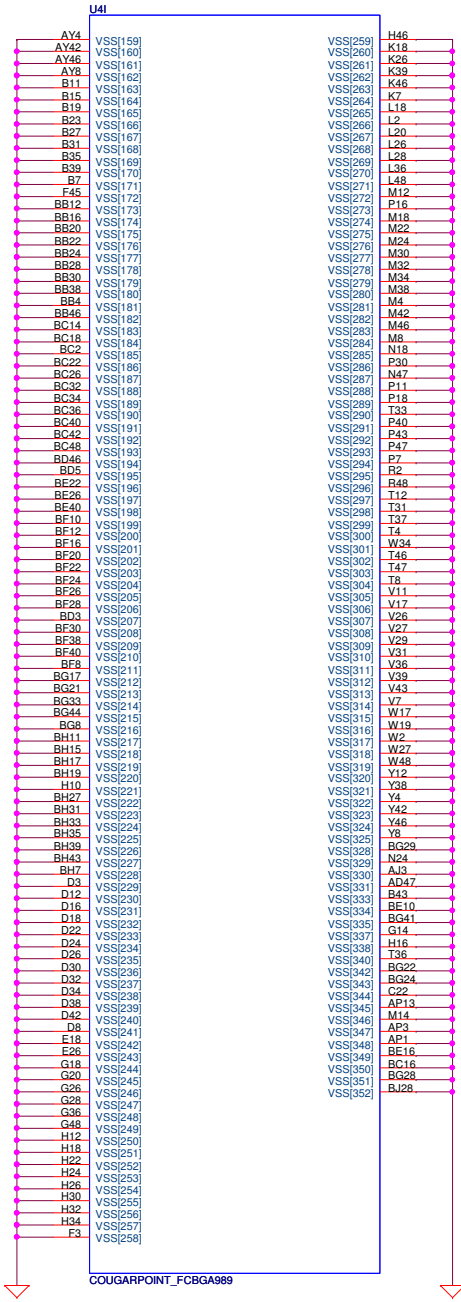
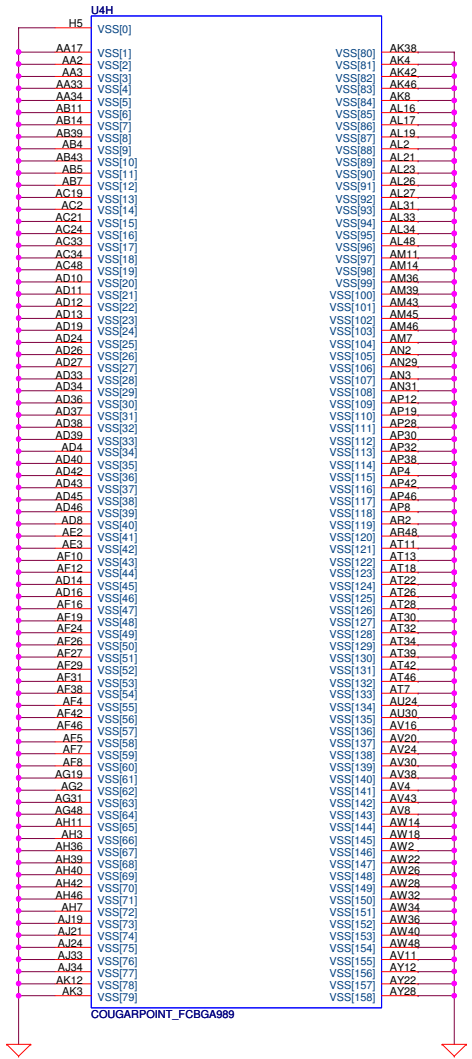


VCC3_3 = 266mA detail waiting for newest spec
 VCCDMI = 42mA detail waiting for newest spec

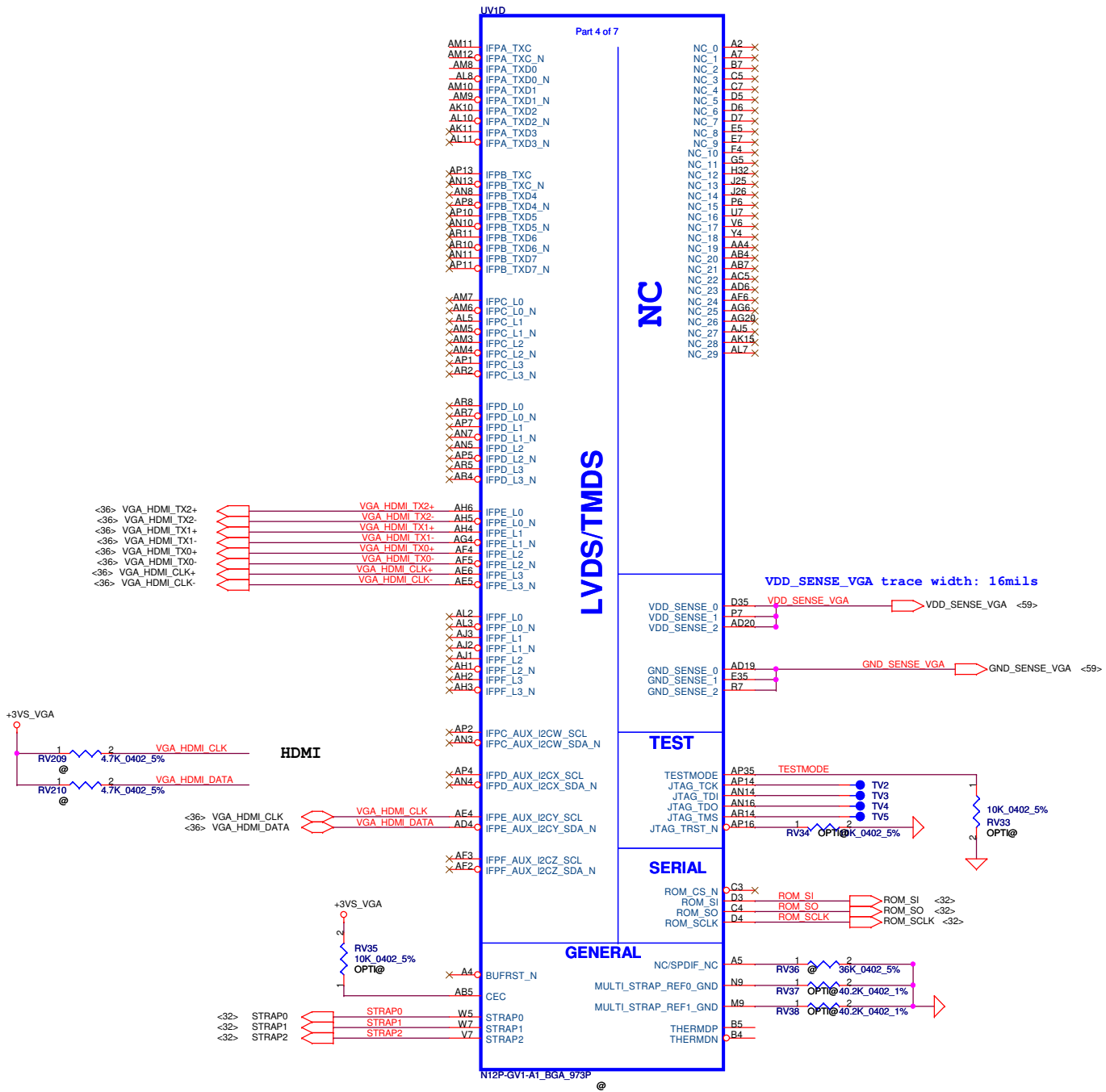


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Title			PCH (8/9) PWR	
Size	Document Number	Rev		
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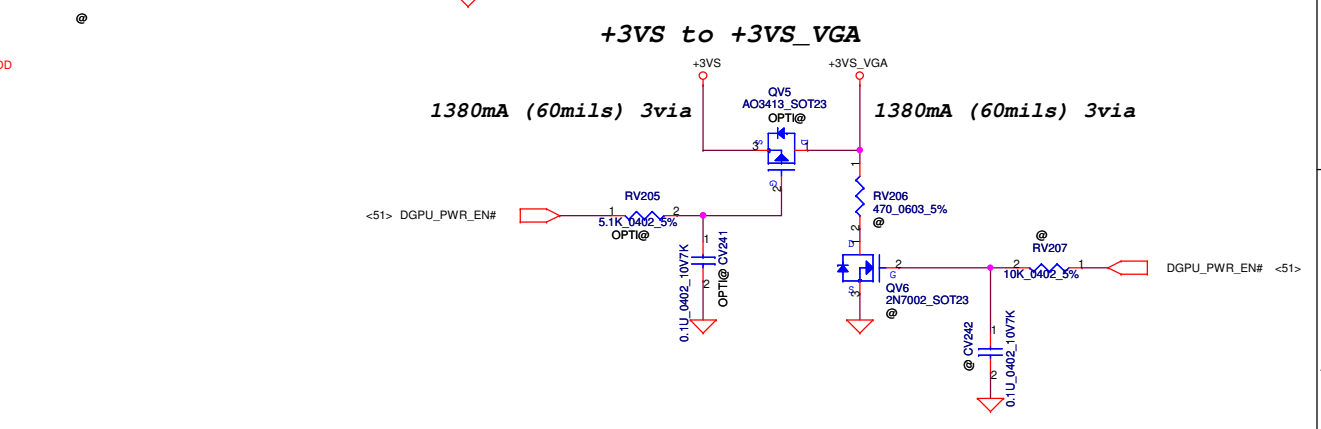
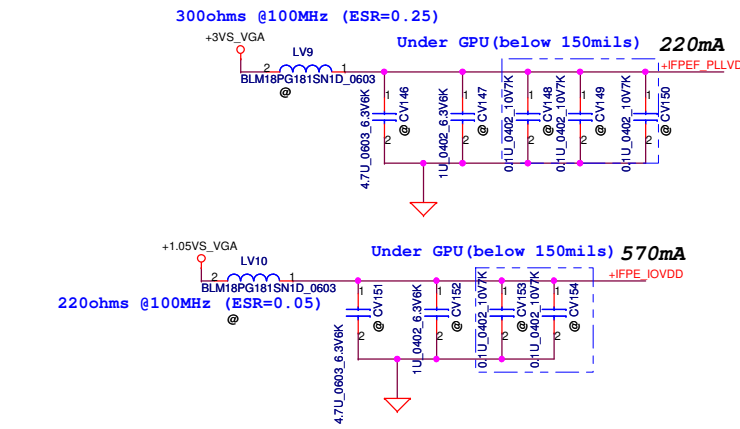
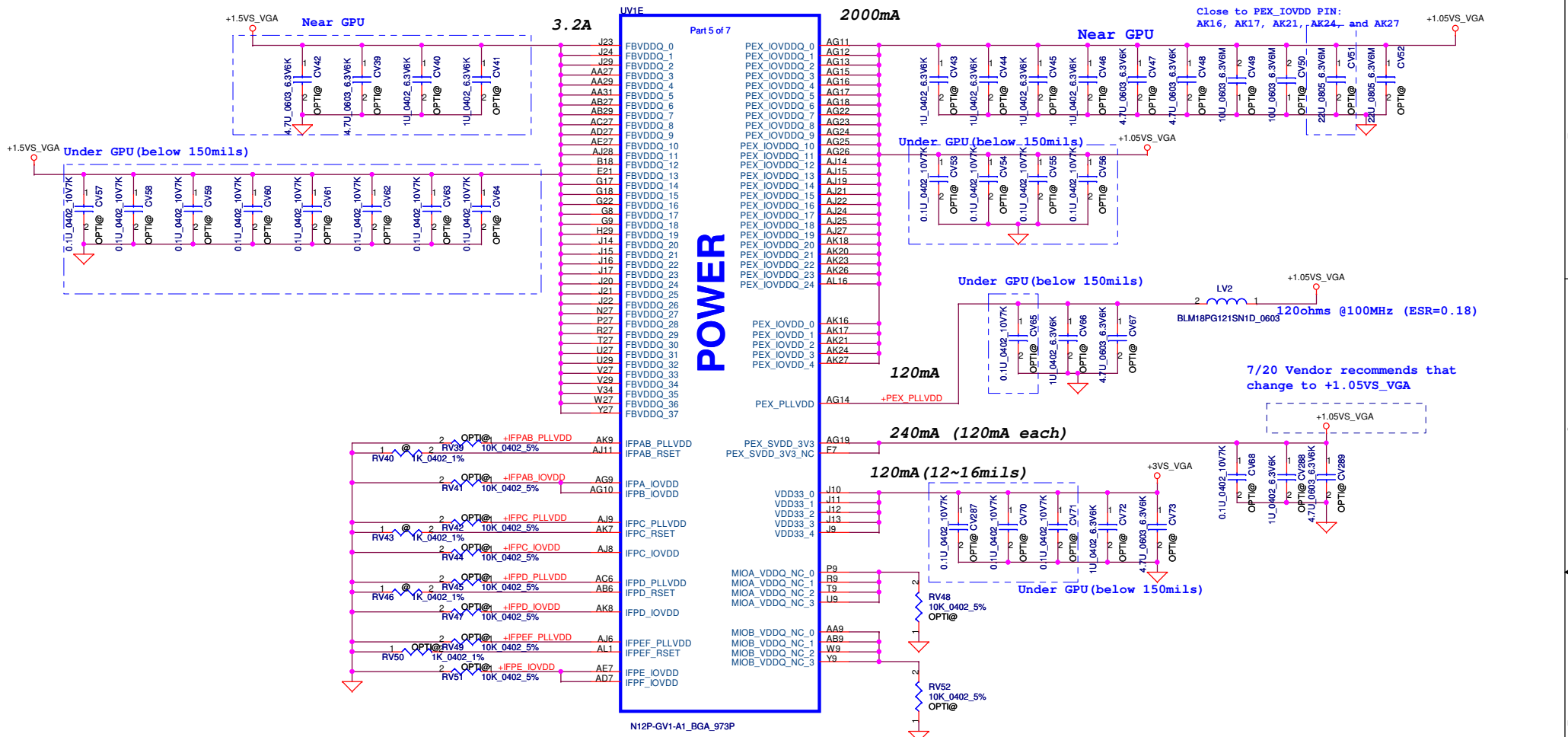


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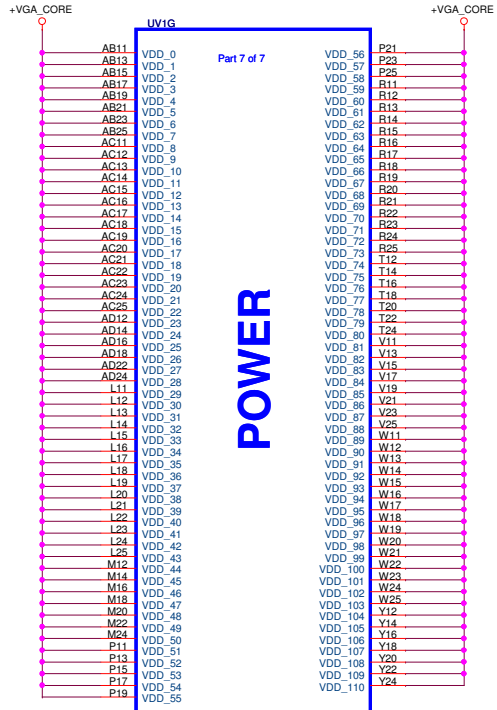
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Title		
N12P-LVDS/HDMI/DP/THM		
Size	Document Number	Rev
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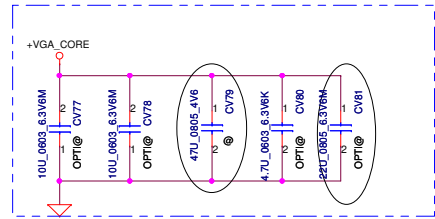
Security Classification	Compal Secret Data		Title	
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30.54A (41.02A Peak)

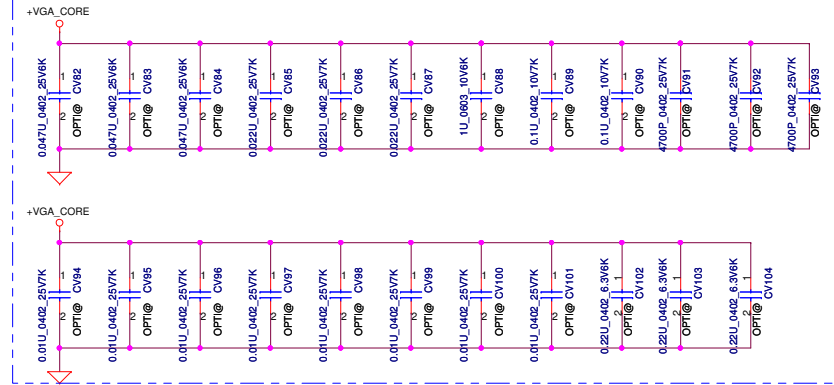


N12P-GV1-A1_BGA_973P

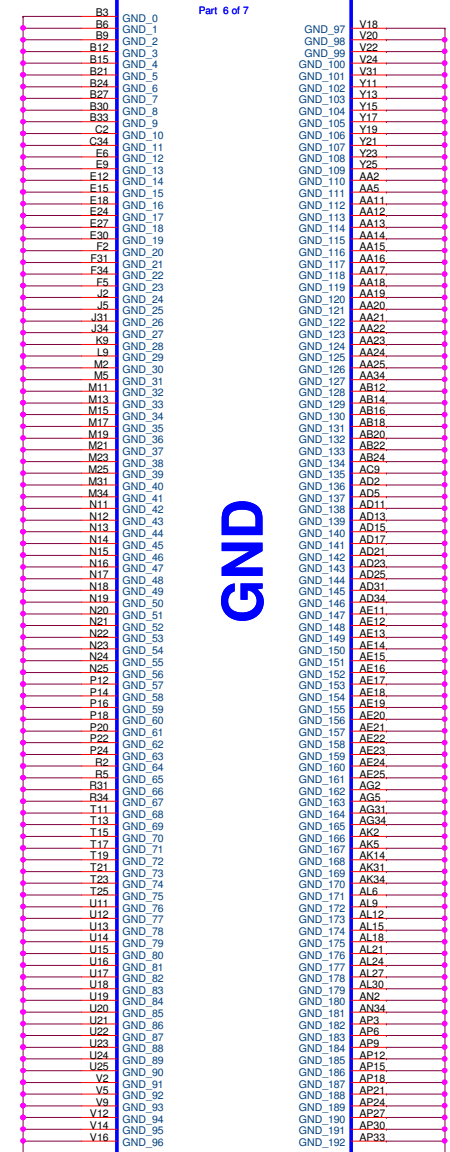
Near GPU



Under GPU

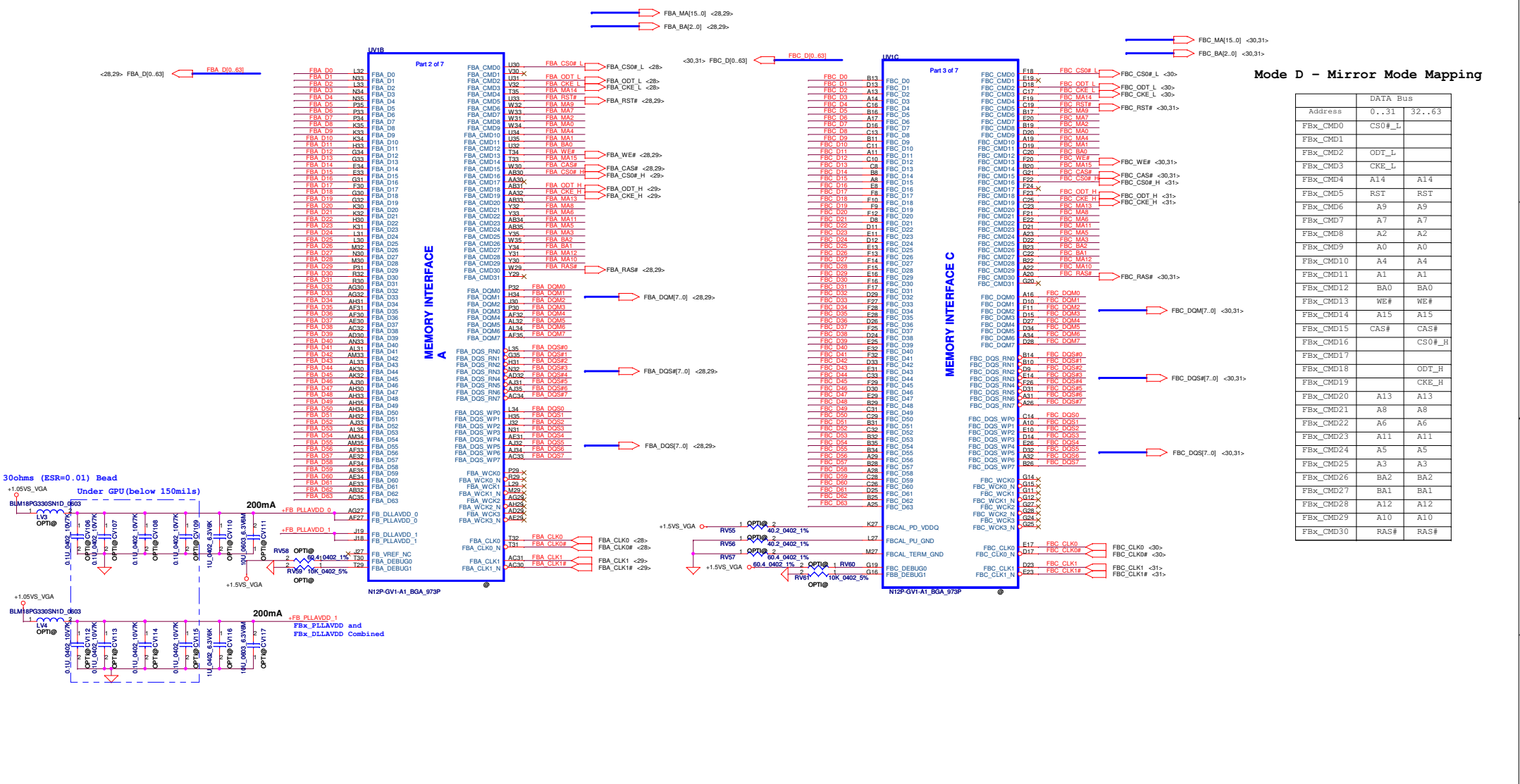


UVIF



N12P-GV1-A1_BGA_973P

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				Date:	Wednesday, January 05, 2011
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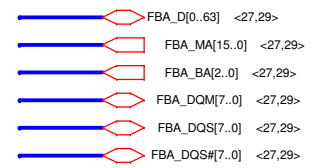


Mode D - Mirror Mode Mapping

Address	DATA Bus
0..31	32..63
FBx_CMD0	CS0#_L
FBx_CMD1	
FBx_CMD2	ODT_L
FBx_CMD3	CKE_L
FBx_CMD4	A14 A14
FBx_CMD5	RST RST
FBx_CMD6	A9 A9
FBx_CMD7	A7 A7
FBx_CMD8	A2 A2
FBx_CMD9	A0 A0
FBx_CMD10	A4 A4
FBx_CMD11	A1 A1
FBx_CMD12	BA0 BA0
FBx_CMD13	WE# WE#
FBx_CMD14	A15 A15
FBx_CMD15	CAS# CAS#
FBx_CMD16	CS0#_H
FBx_CMD17	
FBx_CMD18	ODT_H
FBx_CMD19	CKE_H
FBx_CMD20	A13 A13
FBx_CMD21	A8 A8
FBx_CMD22	A6 A6
FBx_CMD23	A11 A11
FBx_CMD24	A5 A5
FBx_CMD25	A3 A3
FBx_CMD26	BA2 BA2
FBx_CMD27	BA1 BA1
FBx_CMD28	A12 A12
FBx_CMD29	A10 A10
FBx_CMD30	RAS# RAS#

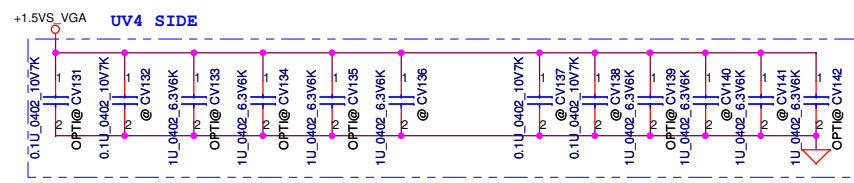
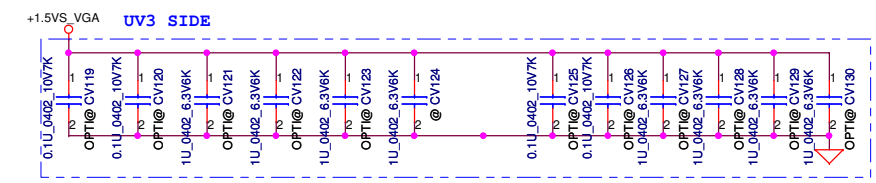
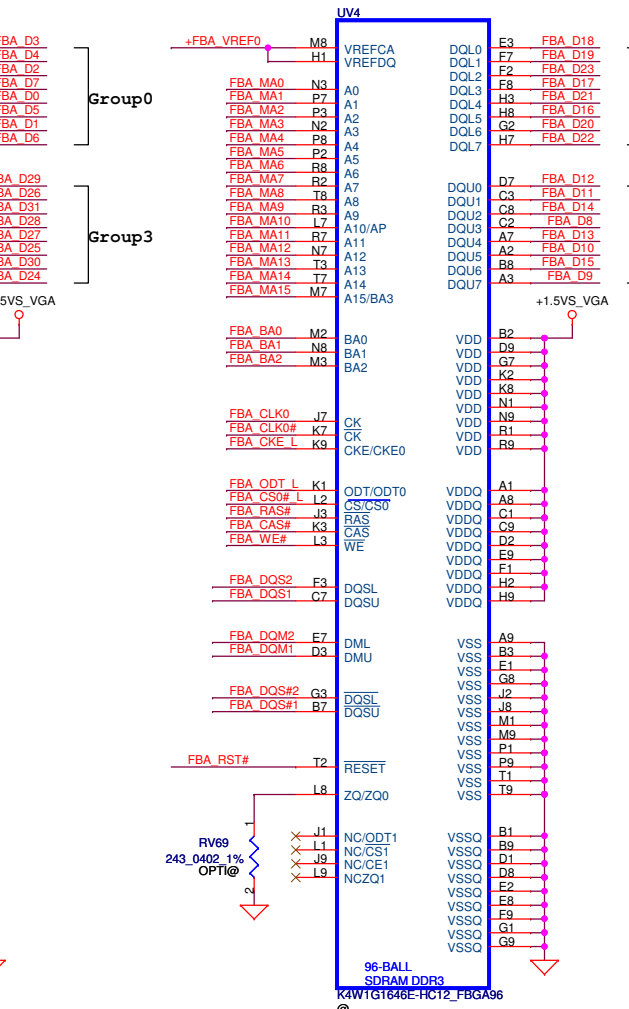
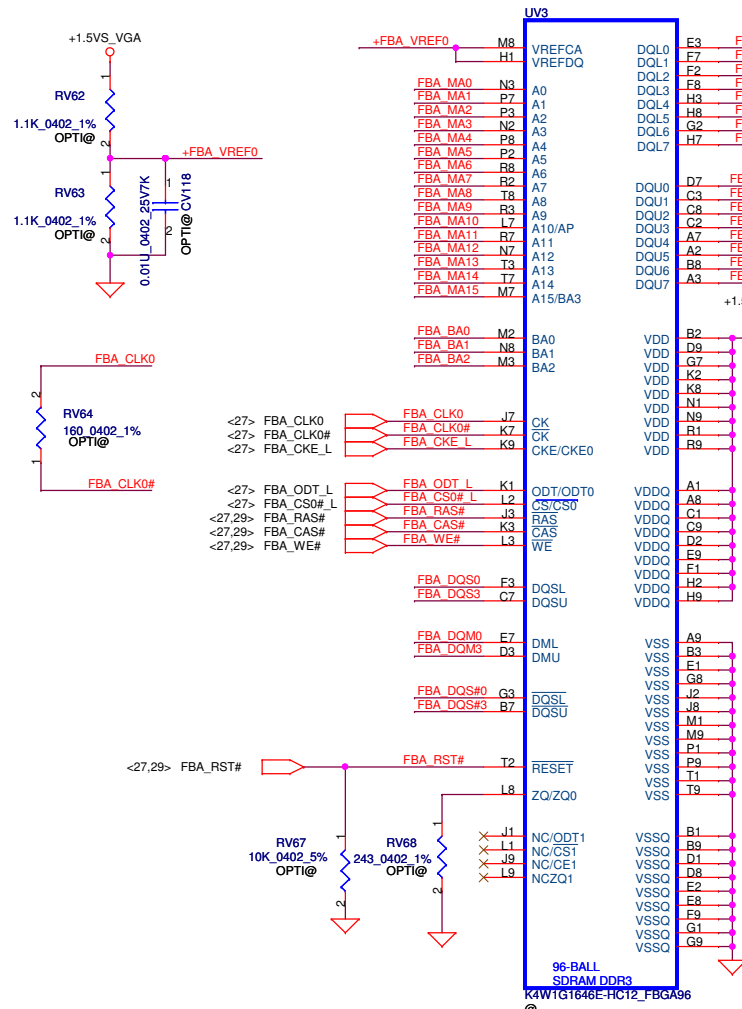
Security Classification	Compal Secret Data		Title N12P-MEM Interface
Issued Date	2010/11/30	Deciphered Date	
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			Date: Wednesday, January 05, 2011 Sheet 27 of 63

Memory Partition A - Lower 32 bits



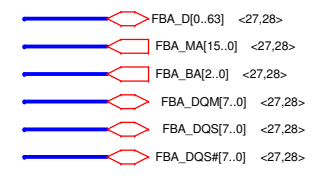
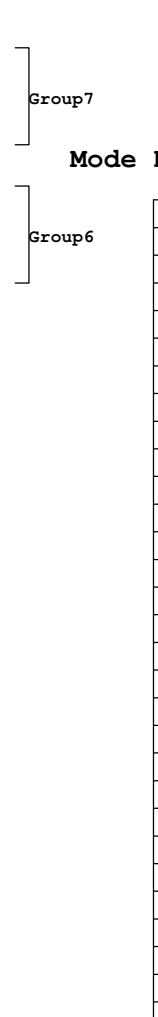
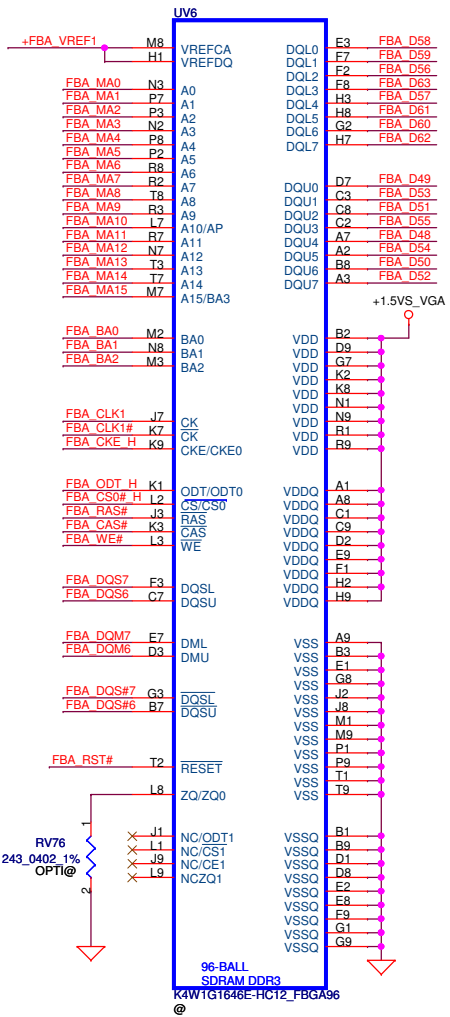
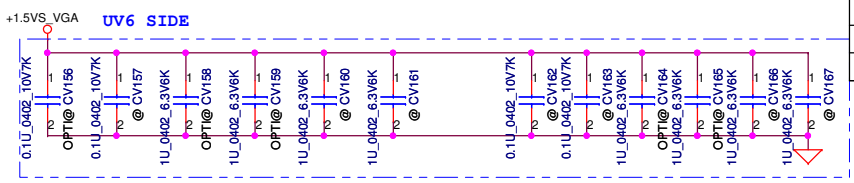
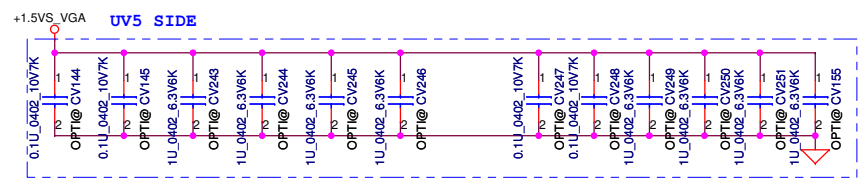
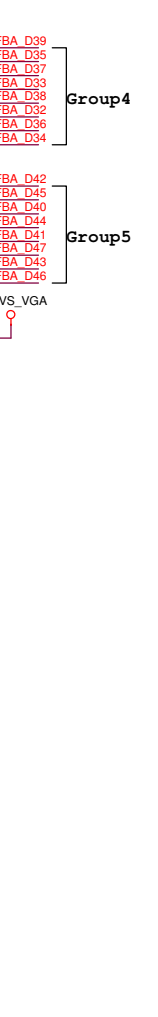
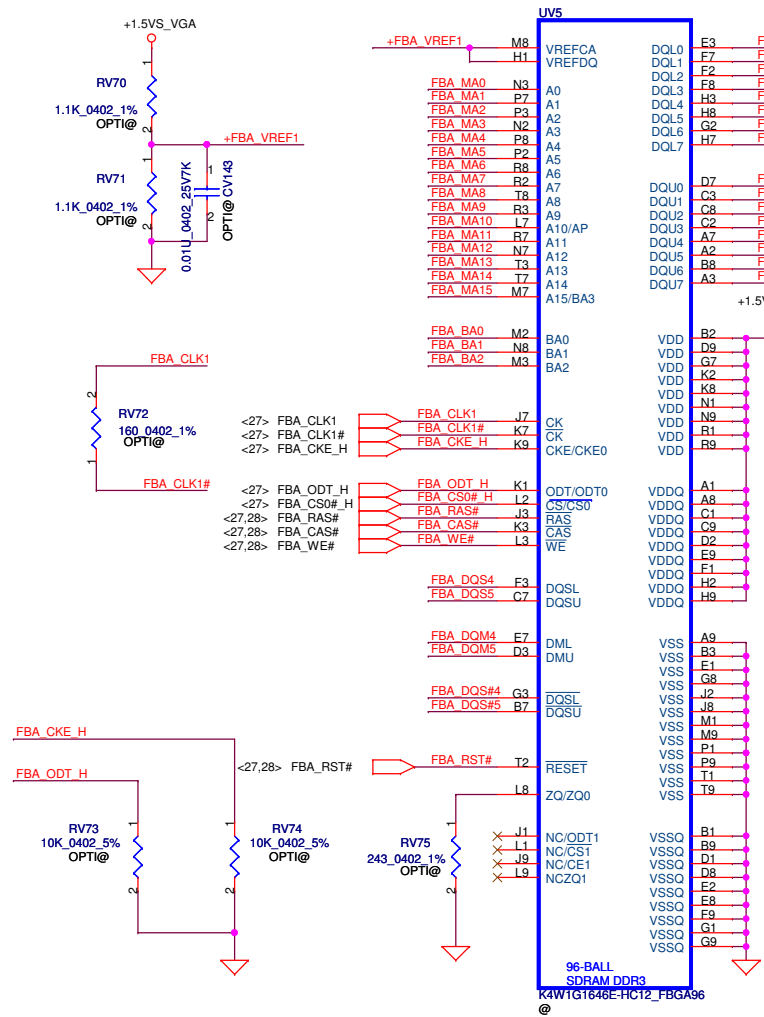
Mode D - Mirror Mode Mapping

DATA Bus		
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



Security Classification		Compal Secret Data		Title	
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				PIQY0 LA6881P	
				Date:	Wednesday, January 05, 2011
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Memory Partition A - Upper 32 bits

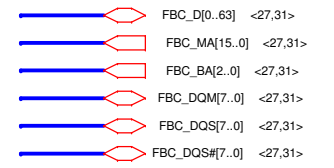


Mode D - Mirror Mode Mapping

Address	DATA Bus	
FBx_CMD0	CS0#_L	32..63
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#

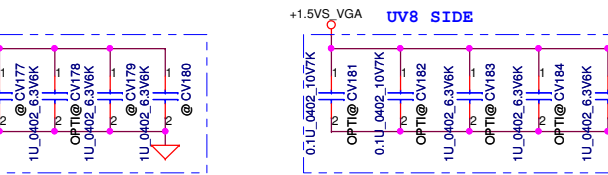
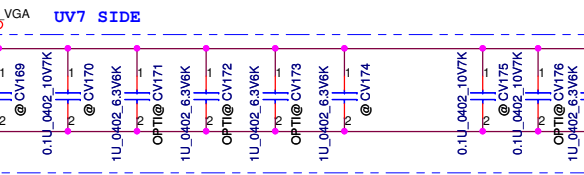
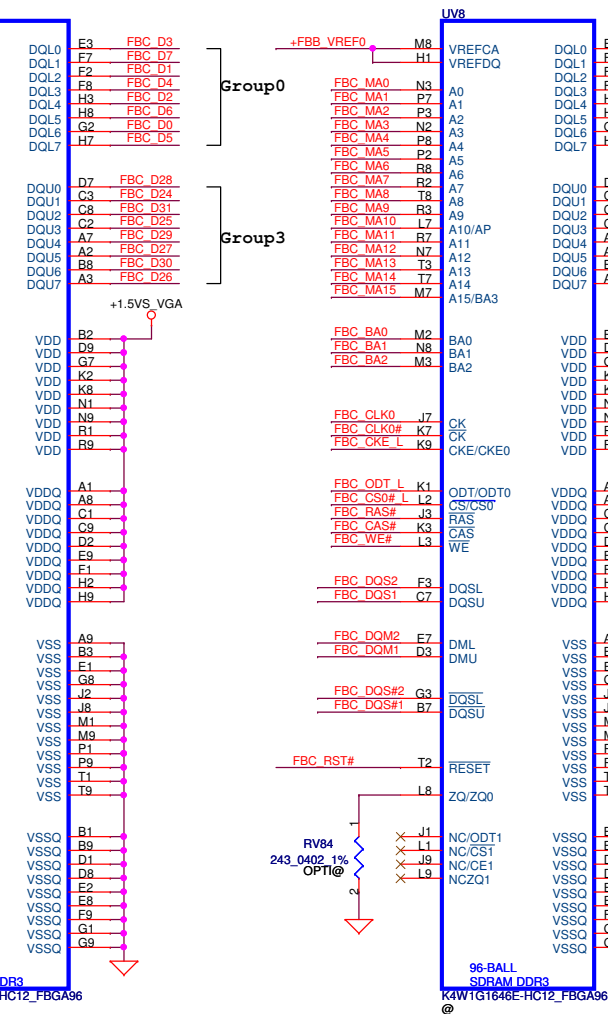
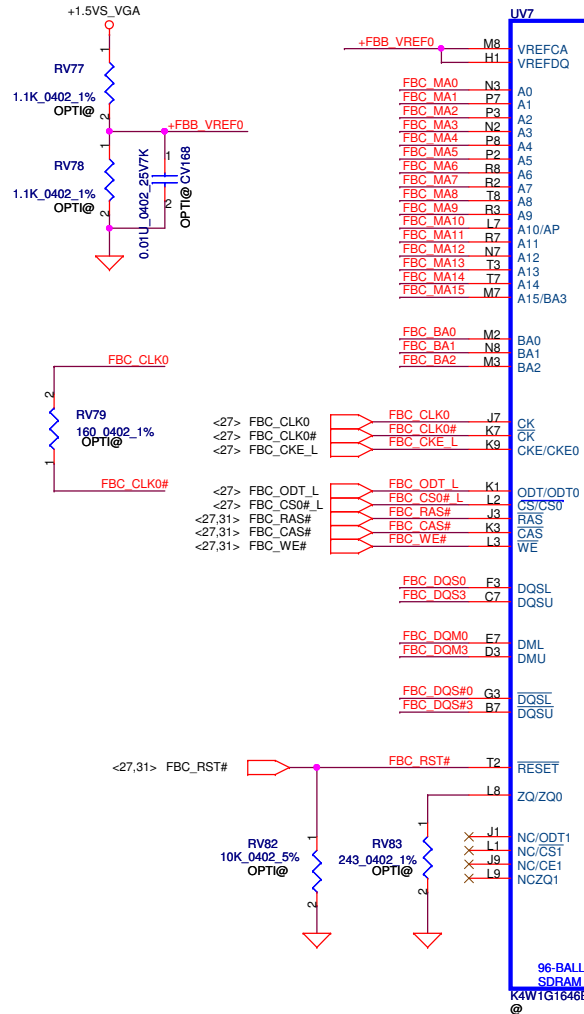
Security Classification		Compal Secret Data		Compal Electronics, Inc. Title: N12P-VRAM A Upper Size: Document Number: PIQY0 LA6881P Date: Wednesday, January 05, 2011	
Issued Date	2010/11/30	Deciphered Date	2011/08		
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Date: Wednesday, January 05, 2011		Sheet 29 of 63			

Memory Partition C - Lower 32 bits



Mode D - Mirror Mode Mapping

	DATA Bus	
Address	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18		ODT_H
FBx_CMD19		CKE_H
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



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Issued Date	2010/11/30	Deciphered Date
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Compal Electronics, Inc.

N12P-VRAM C Lower

PIQY0 LA6881P

Date: Wednesday, January 05, 2011

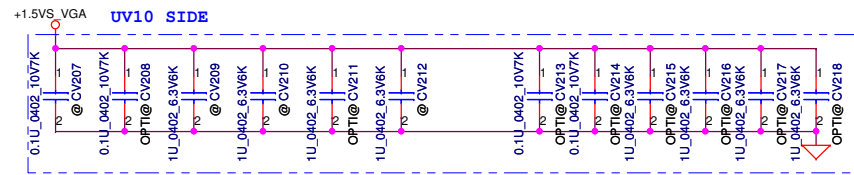
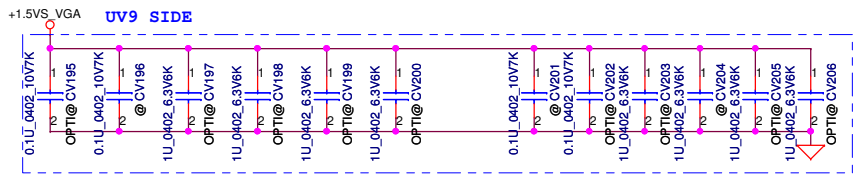
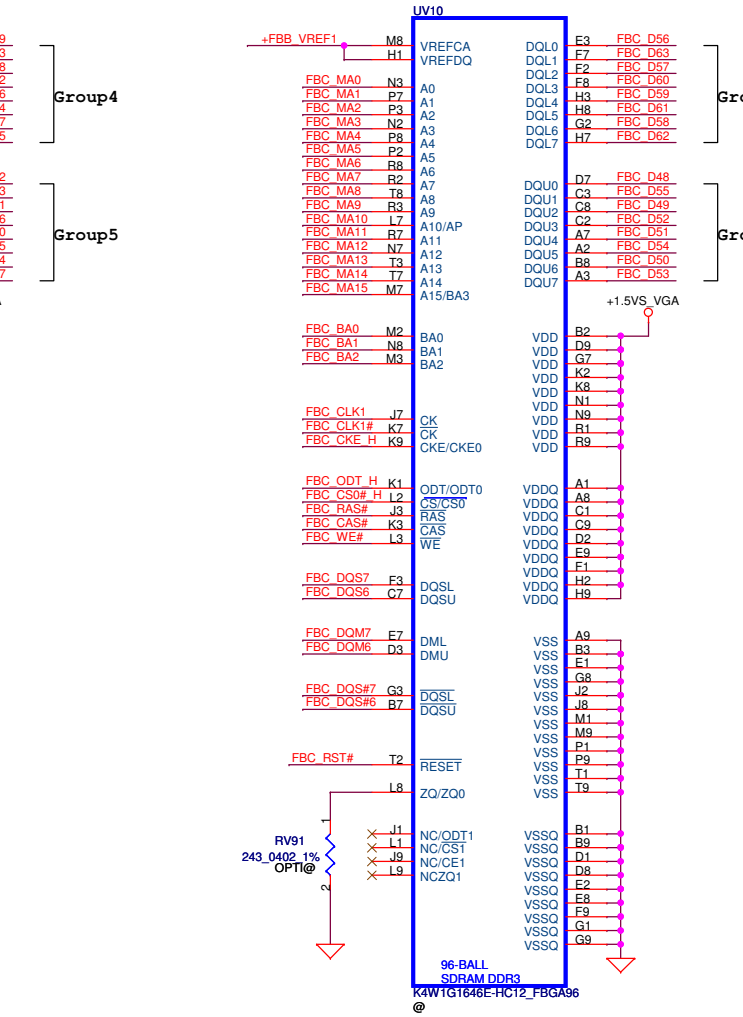
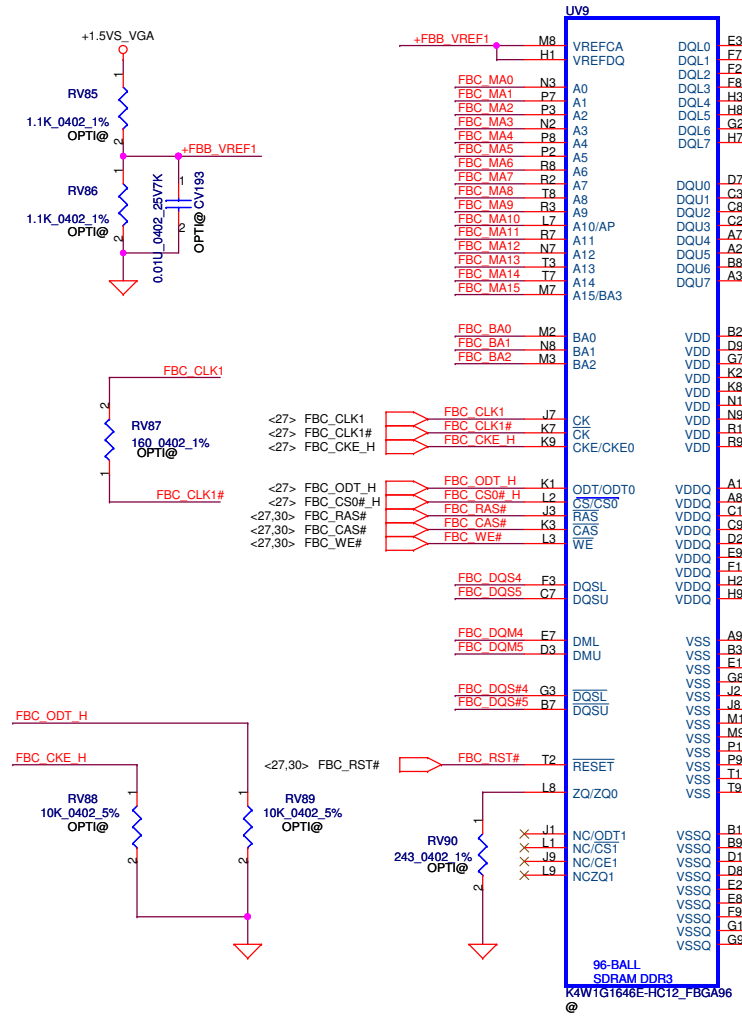
Rev 1.0

Memory Partition C - Upper 32 bits

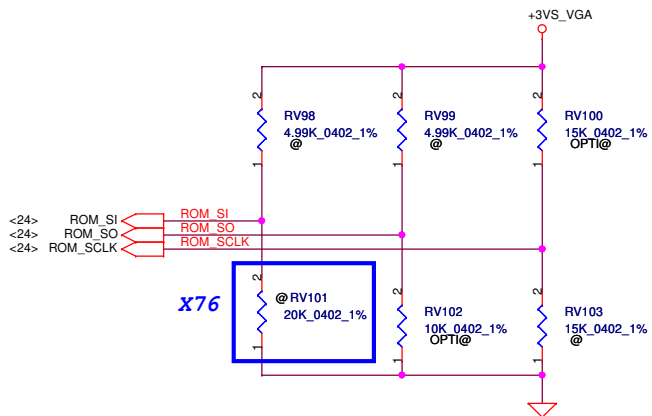
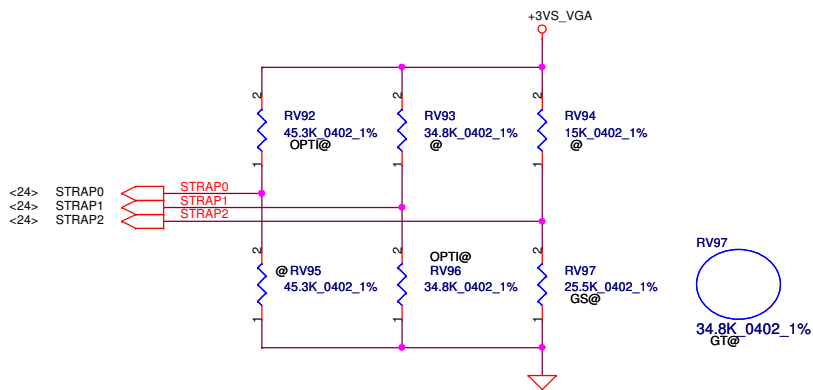
- FBC_D[0..63] <27,30>
- FBC_MA[15..0] <27,30>
- FBC_BA[2..0] <27,30>
- FBC_DQM[7..0] <27,30>
- FBC_DQS[7..0] <27,30>
- FBC_DQS# [7..0] <27,30>

Mode D - Mirror Mode Mapping

Address	DATA Bus	
	0..31	32..63
FBx_CMD0	CS0#_L	
FBx_CMD1		
FBx_CMD2	ODT_L	
FBx_CMD3	CKE_L	
FBx_CMD4	A14	A14
FBx_CMD5	RST	RST
FBx_CMD6	A9	A9
FBx_CMD7	A7	A7
FBx_CMD8	A2	A2
FBx_CMD9	A0	A0
FBx_CMD10	A4	A4
FBx_CMD11	A1	A1
FBx_CMD12	BA0	BA0
FBx_CMD13	WE#	WE#
FBx_CMD14	A15	A15
FBx_CMD15	CAS#	CAS#
FBx_CMD16		CS0#_H
FBx_CMD17		
FBx_CMD18	ODT_H	
FBx_CMD19	CKE_H	
FBx_CMD20	A13	A13
FBx_CMD21	A8	A8
FBx_CMD22	A6	A6
FBx_CMD23	A11	A11
FBx_CMD24	A5	A5
FBx_CMD25	A3	A3
FBx_CMD26	BA2	BA2
FBx_CMD27	BA1	BA1
FBx_CMD28	A12	A12
FBx_CMD29	A10	A10
FBx_CMD30	RAS#	RAS#



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Size	Custom	Document Number	PIQY0 LA6881P		Rev 1.0
Date:	Wednesday, January 05, 2011			Sheet	31 of 63



ROM_SO : PD-10K
 ROM_SCLK : PH-15K
 ROM_SI : PD20K (Samsung)
 Strap 2 : N12P-GS, PD-25K,
 N12P-GT, PD35K,
 Strap 1 : PD-35K
 Strap 0 : PH-45K

	DeviceID	ROM_SCLK	STRAP2
N12P-GS	0x0DF4	Pull up 15K	Pull down 25K
N12P-GT	0x0DF6	Pull up 15K	Pull down 35K

Physical Strapping pin	Power Rail	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0
ROM_SO	+3VS_VGA	XLCK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VS_VGA	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	+3VS_VGA	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
STRAP2	+3VS_VGA	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	+3VS_VGA	3GIO_PAD_CFG_ADR[3]	3GIO_PAD_CFG_ADR[2]	3GIO_PAD_CFG_ADR[1]	3GIO_PAD_CFG_ADR[0]
STRAP0	+3VS_VGA	USER[3]	USER[2]	USER[1]	USER[0]

Resistor Values	Pull-up to +3VS_VGA	Pull-down to Gnd
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111

SUB_VENDOR	
0	No VBIOS ROM
1	BIOS ROM is present (Default)

XLCK_417	
0	277MHz (Default)
1	Reserved

FB_0_BAR_SIZE	
0	256MB (Default)
1	Reserved

USER Straps	
User [3:0]	
1000-1100	Customer defined

3GIO_PADCFG	
3GIO_PADCFG[3:0]	
0110	Notebook Default

PEX_PLL_EN_TERM	
0	Disable (Default)
1	Enable

SLOT_CLK_CFG	
0	GPU and MCH don't share a common reference clock
1	GPU and MCH share a common reference clock (Default)

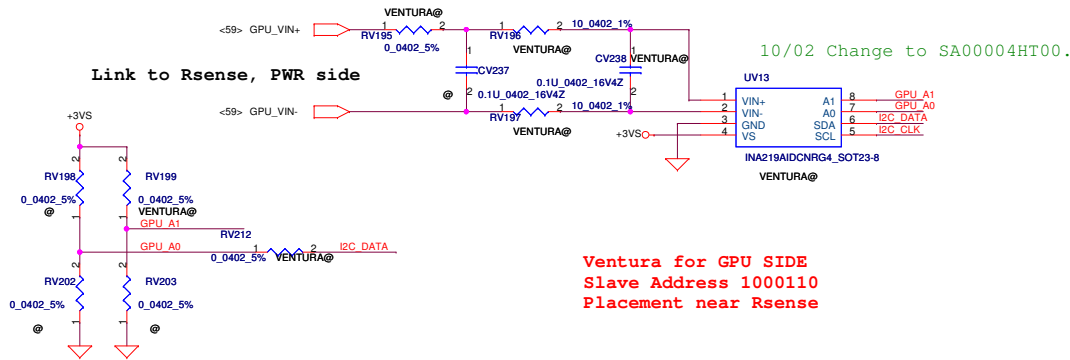
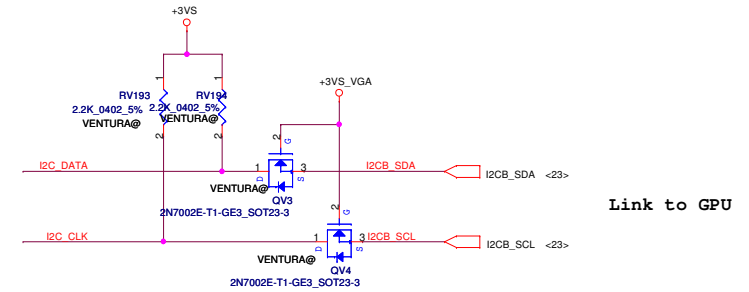
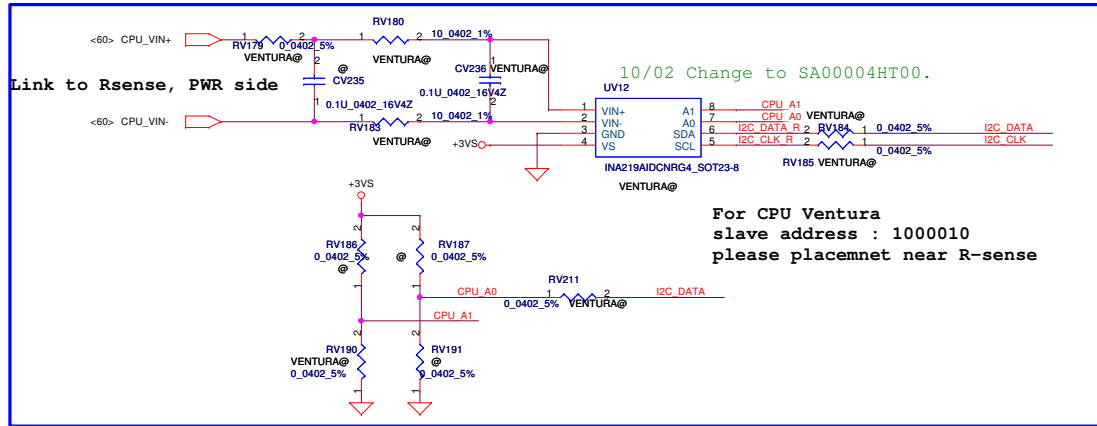
SMBUS_ALT_ADDR	
0	0x9E (Default)
1	0x9C (Multi-GPU usage)

VGA_DEVICE	
0	3D Device (Class Code 302h)
1	VGA Device (Default)

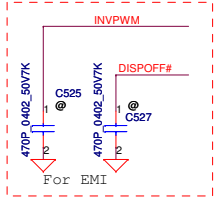
Hynix H5TQ1G63BFR-12C	64Mx16	0010	PD 15K	SA000041S30
	128Mx16	0110	PD 35K	SA00003Y000
Samsung K4W1G1646E-HC12	64Mx16	0011	PD 20K	SA000041T10
	128Mx16	0111	PD 45K	SA000047Q10

Security Classification	Compal Secret Data		Title	
Issued Date	2010/11/30	Deciphered Date	2011/08	Compal Electronics, Inc. N12P_MISC
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				Document Number PIQY0 LA6881P
				Rev 1.0
				Date: Wednesday, January 05, 2011
				Sheet 32 of 63

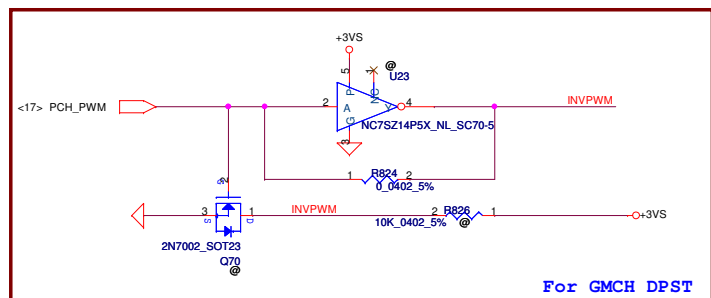
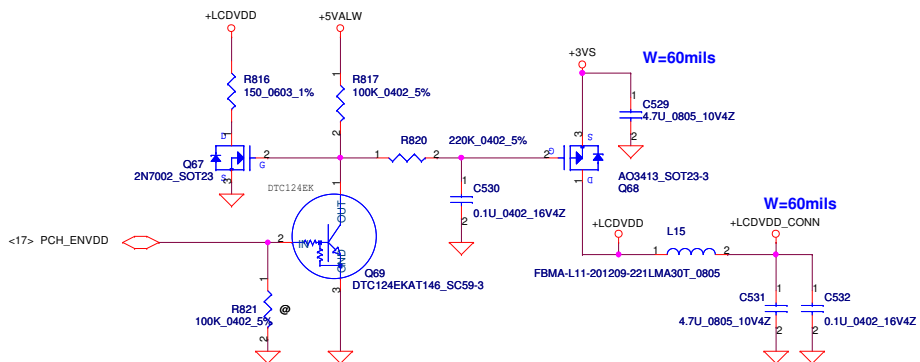
TOP side (under inductor)



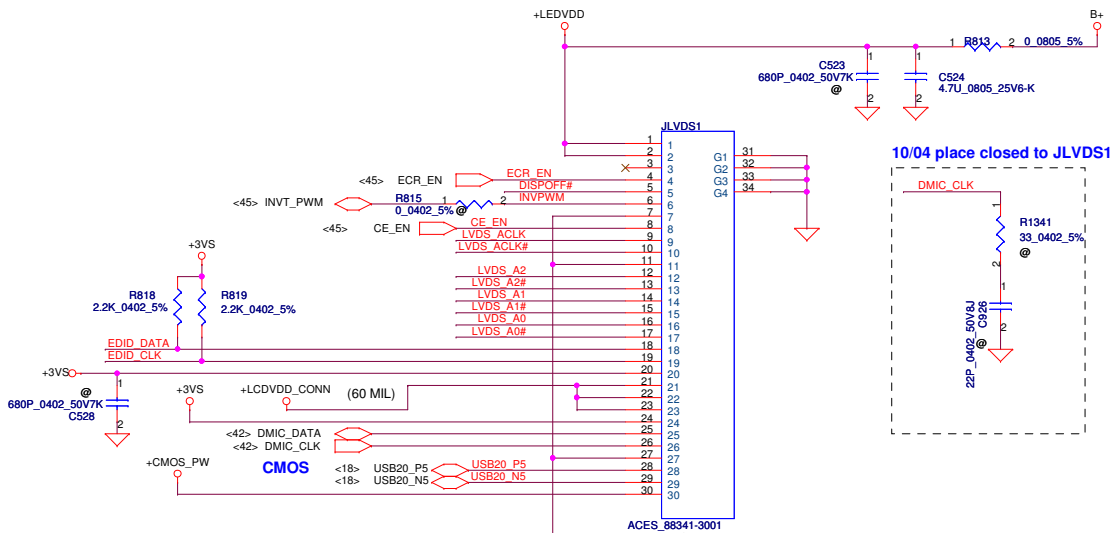
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			N12P_VENTURA	
			PIQY0 LA6881P	
			Date:	Wednesday, January 05, 2011
			Sheet	33 of 63
			Rev	1.0



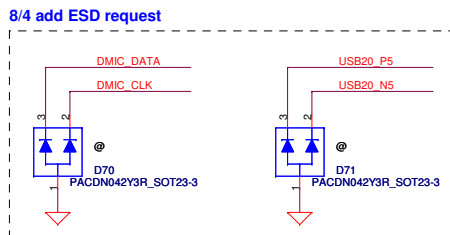
LCD POWER CIRCUIT



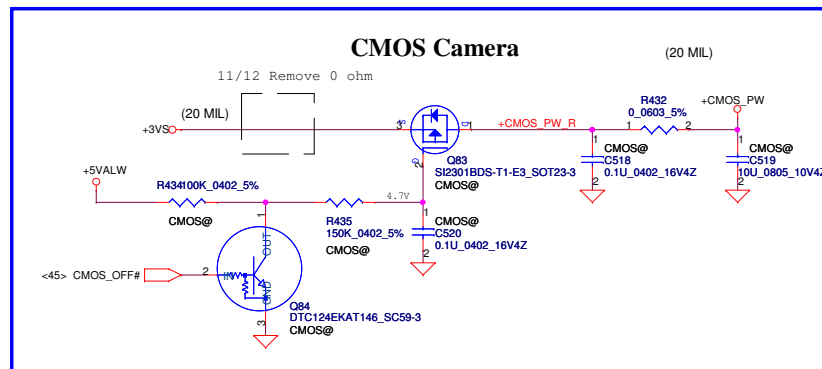
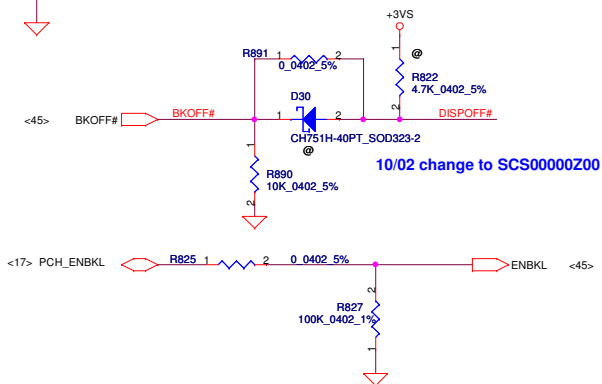
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- <17> EDID_DATA <=> EDID_DATA
- <17> LVDS_A0 <=> LVDS_A0
- <17> LVDS_A0# <=> LVDS_A0#
- <17> LVDS_A1 <=> LVDS_A1
- <17> LVDS_A1# <=> LVDS_A1#
- <17> LVDS_A2 <=> LVDS_A2
- <17> LVDS_A2# <=> LVDS_A2#
- <17> LVDS_ACLK <=> LVDS_ACLK
- <17> LVDS_ACLK# <=> LVDS_ACLK#



9/21 Rev0.2 update from 40 to 30 pin.

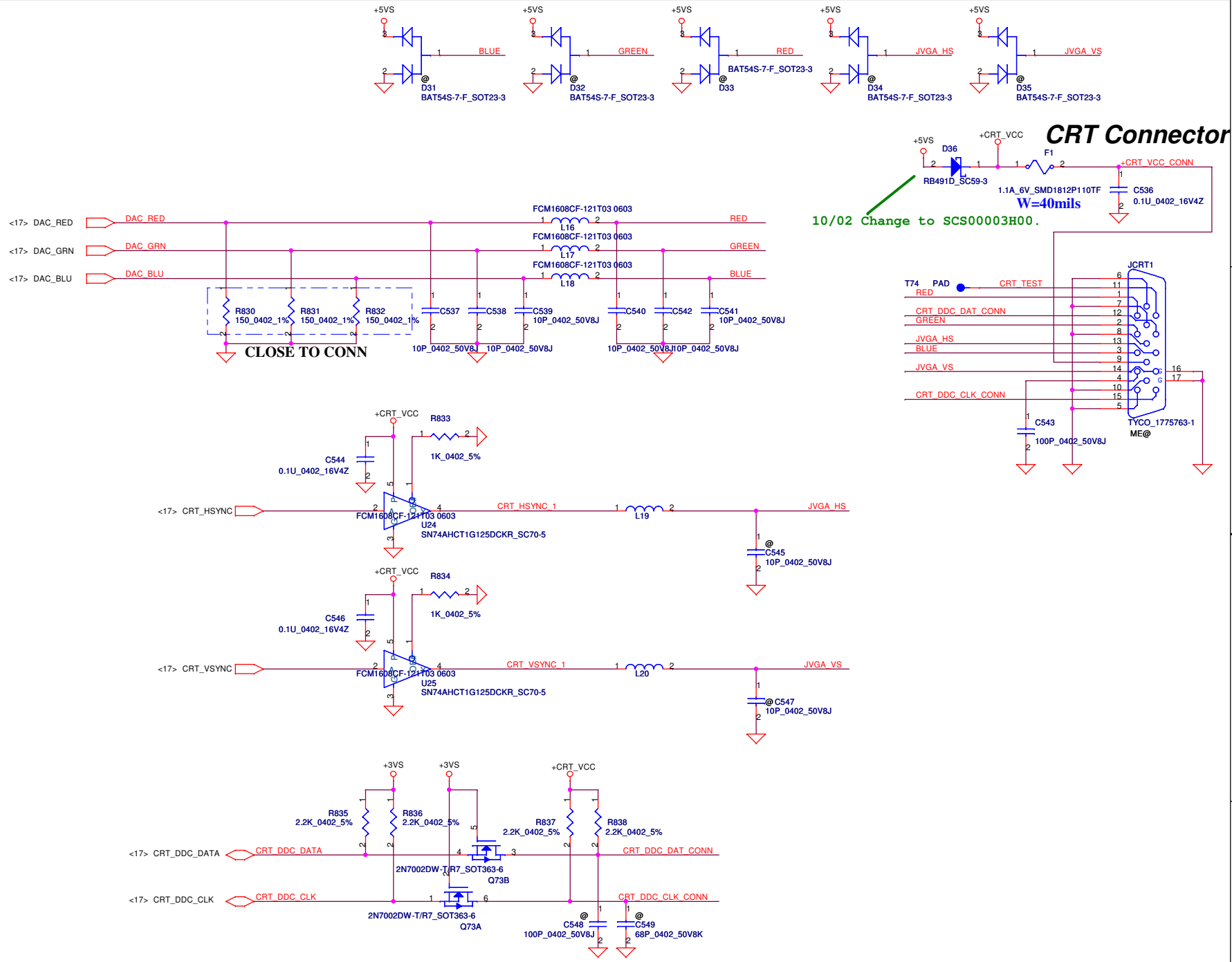


8/4 add ESD request

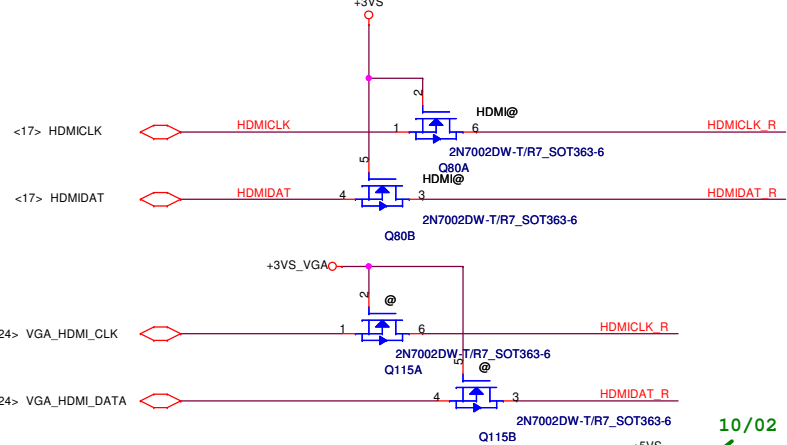
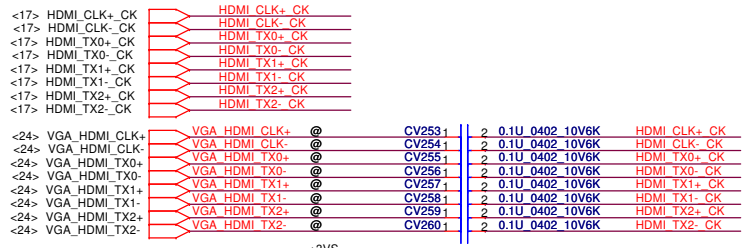
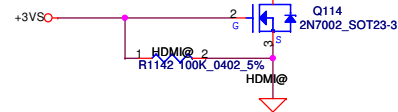
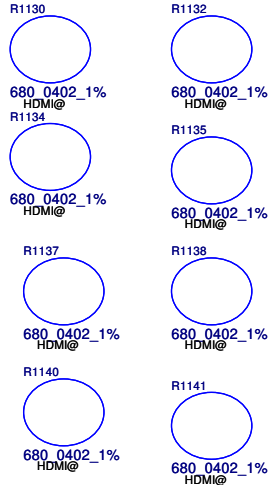
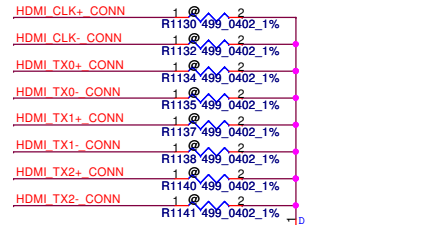


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Issued Date	2010/11/30	Deciphered Date	2011/08	Compal Electronics, Inc.	
				LVDS/CAMERA	
				Size B	Document Number
				PIQYO LA6881P	
				Date:	Wednesday, January 05, 2011
				Sheet	34 of 63
				Rev	1.0

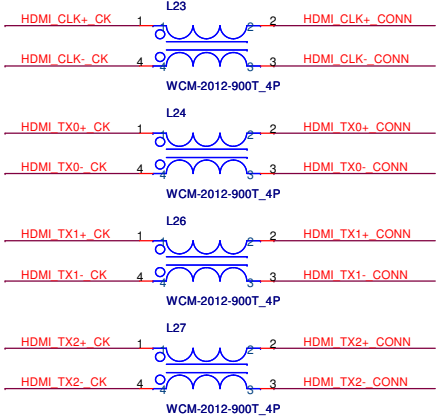
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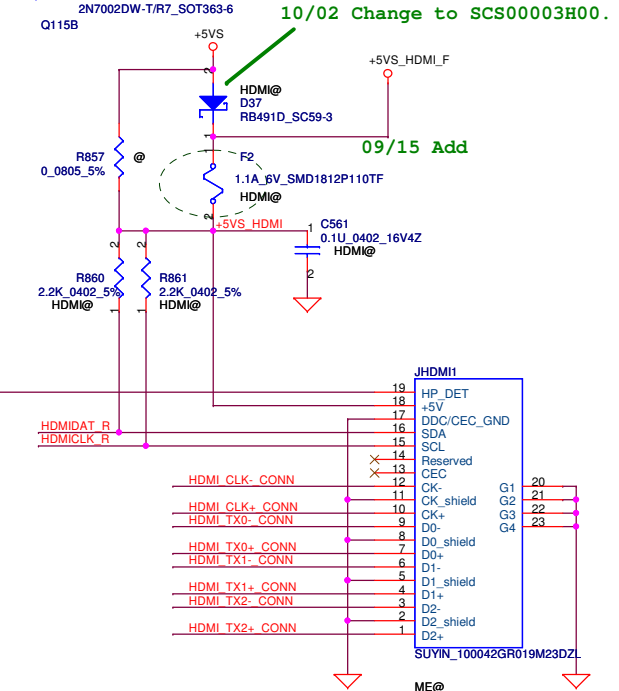
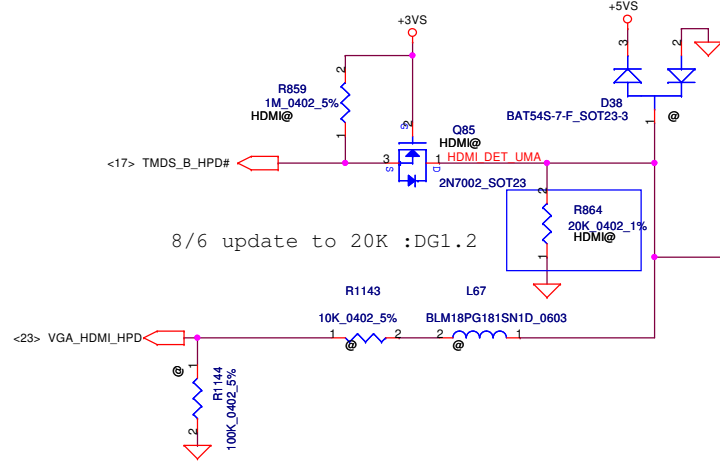
Security Classification		Compal Secret Data		Title	
Issued Date	2010/11/30	Deciphered Date	2011/08	Compal Electronics, Inc.	
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Size	Document Number	Rev		1.0	
Custom	PIQY0 LA6881P	Date:		Wednesday, January 05, 2011 Sheet 35 of 63	



DVT, Change to SM070000I00 for EMI request.



HDMI CLK+ CK	R885	1	2	0	0402_5%	HDMI CLK+ CONN
HDMI CLK- CK	R886	1	2	0	0402_5%	HDMI CLK- CONN
HDMI TX0+ CK	R887	1	2	0	0402_5%	HDMI TX0+ CONN
HDMI TX0- CK	R888	1	2	0	0402_5%	HDMI TX0- CONN
HDMI TX1+ CK	R889	1	2	0	0402_5%	HDMI TX1+ CONN
HDMI TX1- CK	R870	1	2	0	0402_5%	HDMI TX1- CONN
HDMI TX2+ CK	R871	1	2	0	0402_5%	HDMI TX2+ CONN
HDMI TX2- CK	R872	1	2	0	0402_5%	HDMI TX2- CONN



10/02 Change to SCS00003H00.

09/15 Add

Security Classification		Compal Secret Data		Title		HDMI CONN	
Issued Date	2010/11/30	Deciphered Date	2011/08	Size	Document Number	Date	Rev
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				Date		Sheet	36 of 63

Compal Electronics, Ltd.

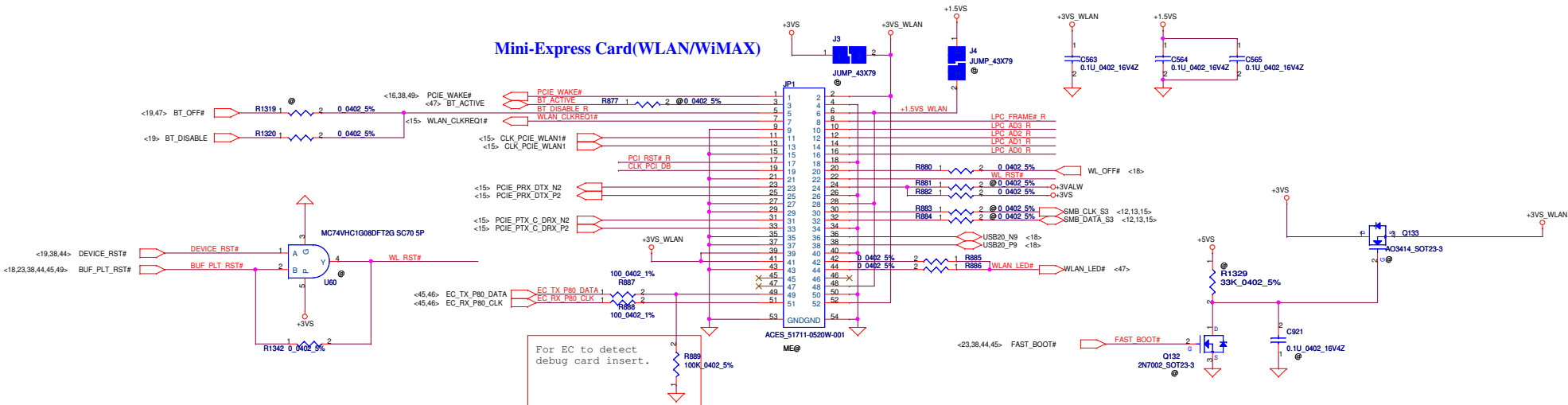
ME@

Mini-Express Card for WLAN/WiMAX(Half) Mini-Express Card for SSD(Full)

Reserve for SW mini-pcie debug card.
Series resistors closed to KBC side.

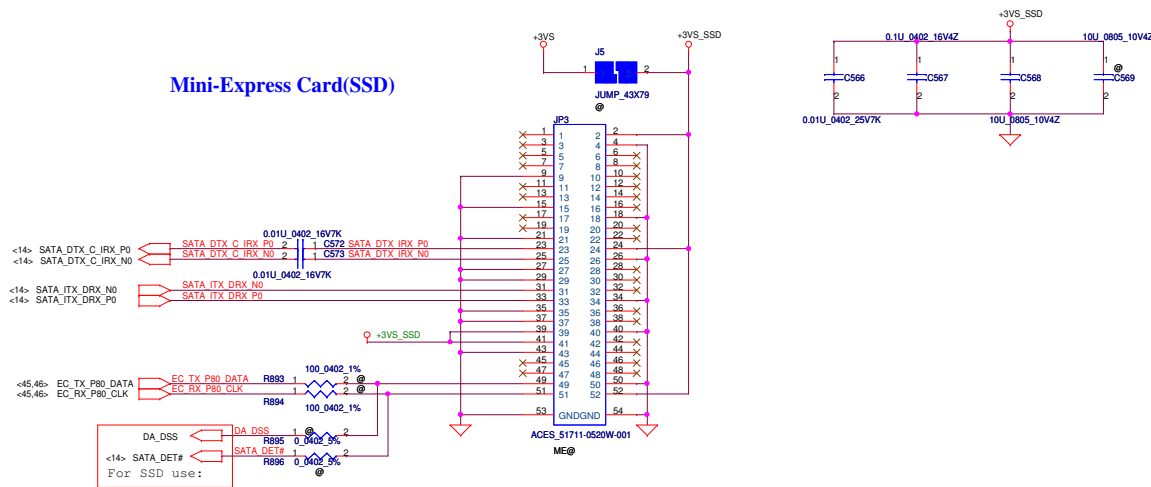
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LPC_AD3 R	R874	1	2	0.0402_5%	LPC_AD3	LPC_AD3	<14,45>
LPC_AD2 R	R875	1	2	0.0402_5%	LPC_AD2	LPC_AD2	<14,45>
LPC_AD1 R	R876	1	2	0.0402_5%	LPC_AD1	LPC_AD1	<14,45>
LPC_AD0 R	R877	1	2	0.0402_5%	LPC_AD0	LPC_AD0	<14,45>
PCI_RST# R	R878	1	2	0.0402_5%	PCI_RST#	PCI_RST#	<14,45>
CLK_PCT_DS	R879	1	2	0.0402_5%	CLK_PCT_DS	CLK_PCT_DS	<15>

Mini-Express Card(WLAN/WiMAX)

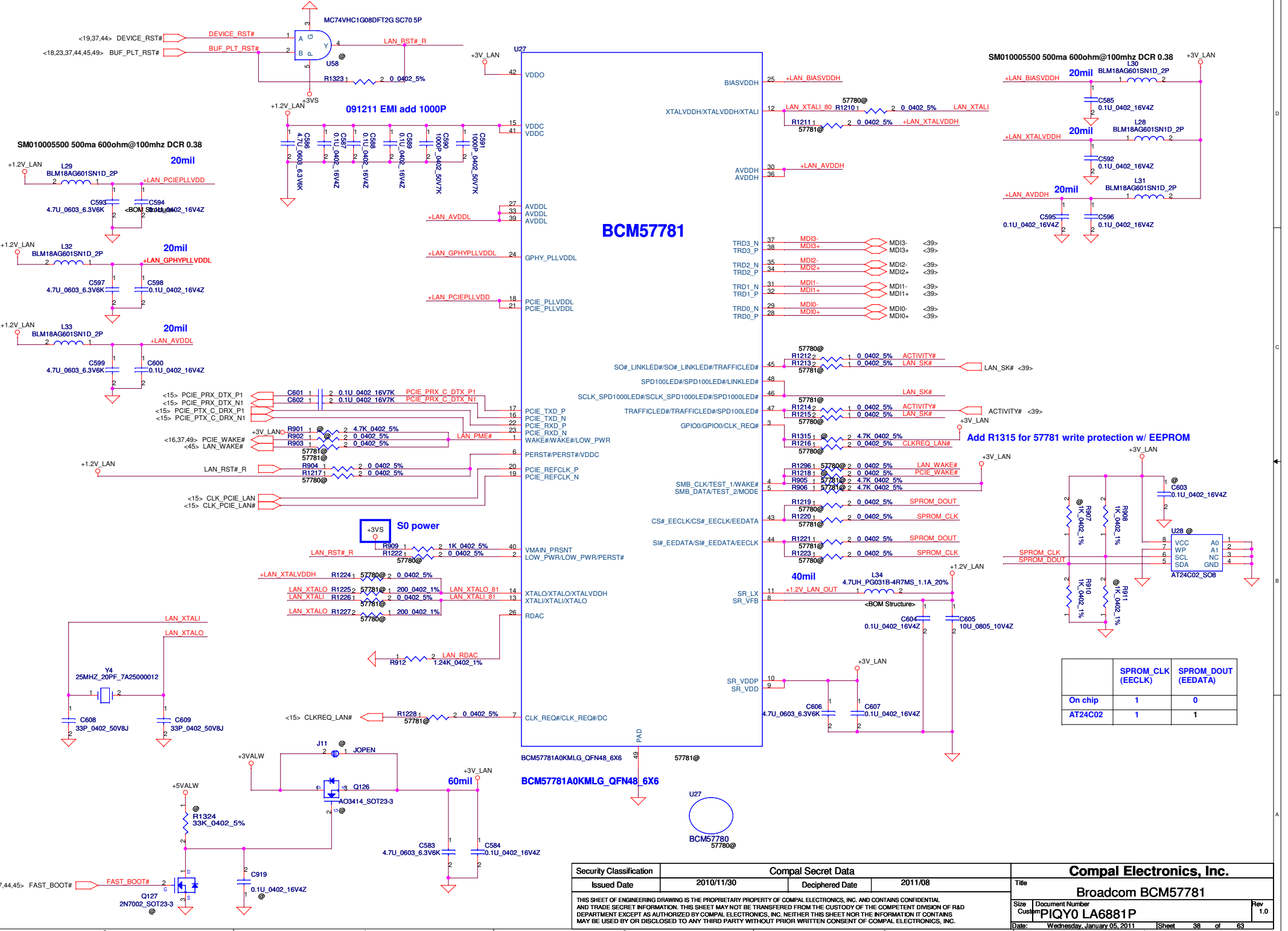


SSD Active:0.22W(0.06A)

Mini-Express Card(SSD)



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Size	Document Number	PIQY0 LA6881P		Rev 1.0
Date	Wednesday, January 05, 2011	Sheet	37	of 63



BCM57781

BCM57781A0KMLG_QFN48_6X6

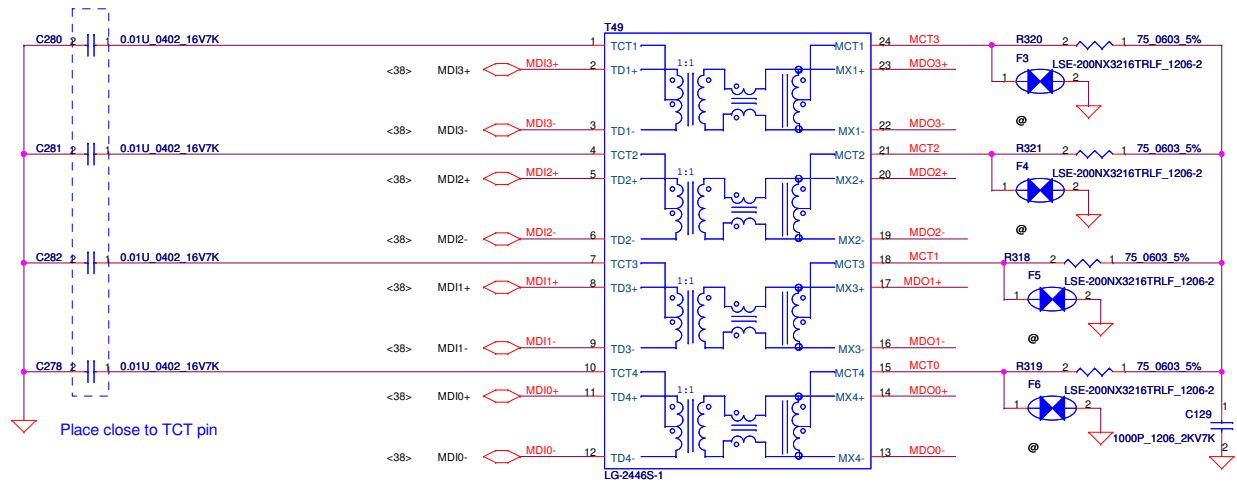


	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

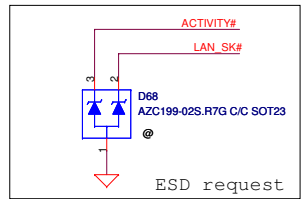
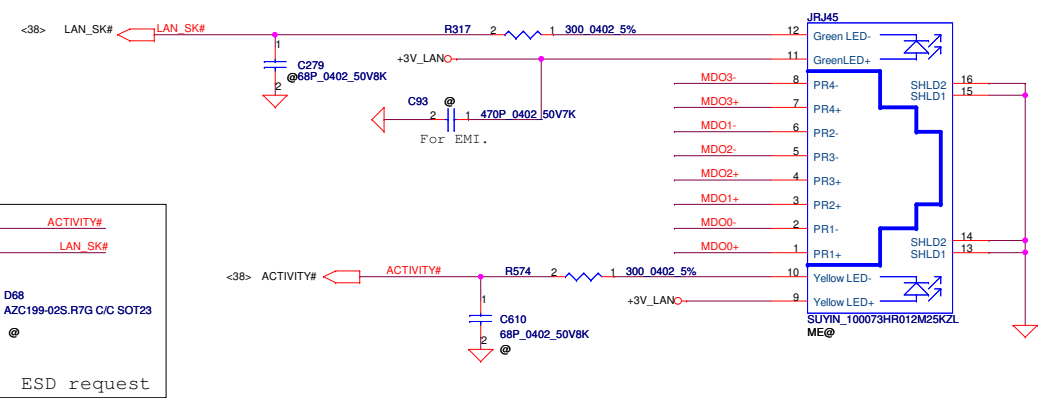
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Issued Date	2010/11/30	Deciphered Date	2011/08	
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Compal Electronics, Inc.				
Broadcom BCM57781				
Size	Document Number			Rev
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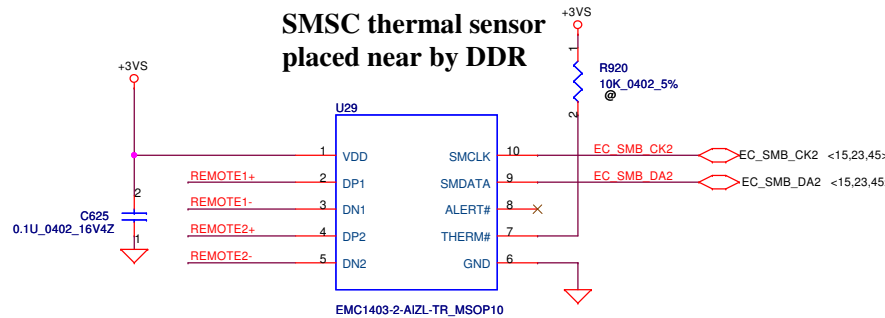
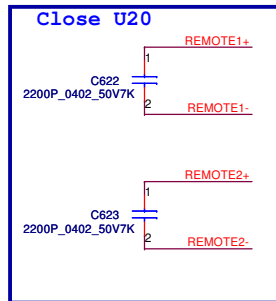
Close to T14



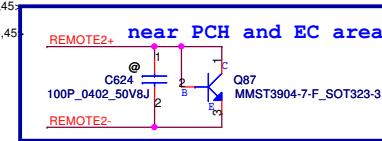
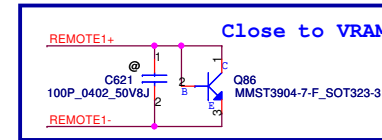
RJ45 Conn.



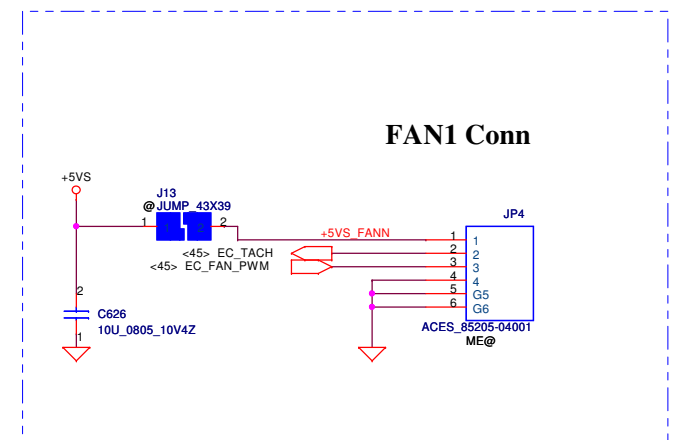
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/11/30	Deciphered Date	2011/08	Title	
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Size	Document Number	Rev			
Custom	PIQY0 LA6881P	1.0			
Date:	Wednesday, January 05, 2011	Sheet	39	of	63



Address 1001_101xb
8/02 Change PN to SA000046C00, Fintek.

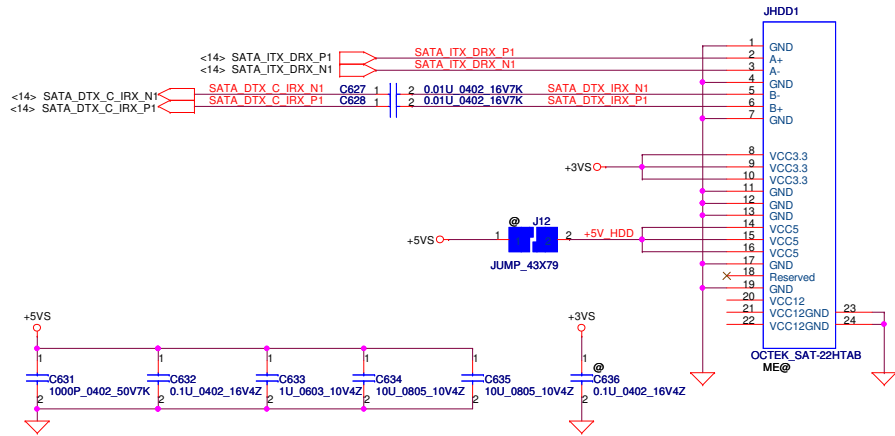


REMOTE1, 2+/-:
Trace width/space: 10/10 mil
Trace length: <8"

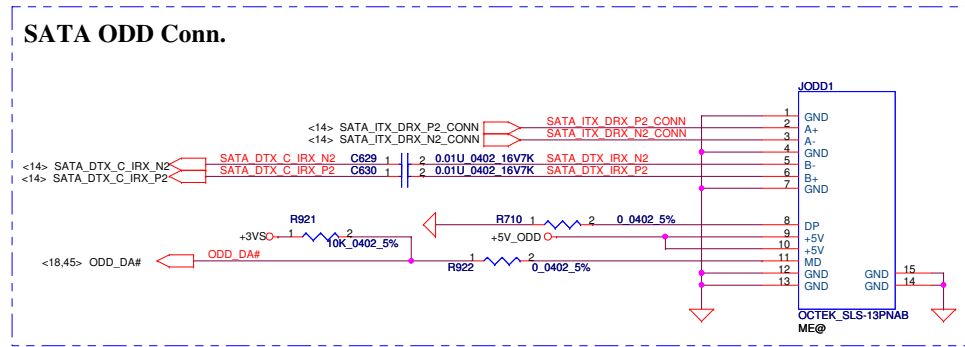


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				Date: Wednesday, January 05, 2011	Rev 1.0
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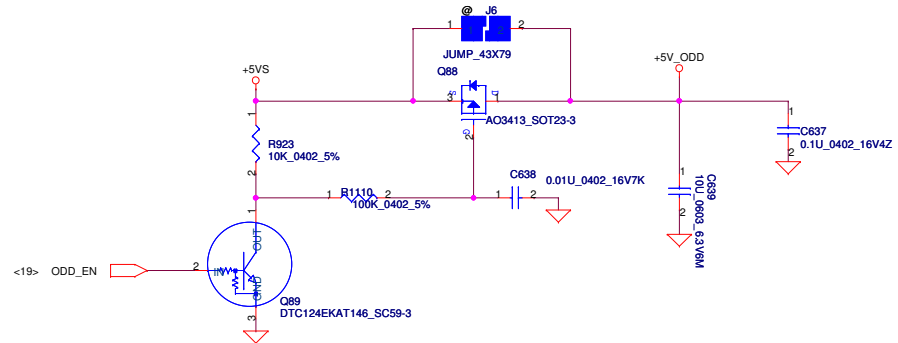
SATA HDD Conn.



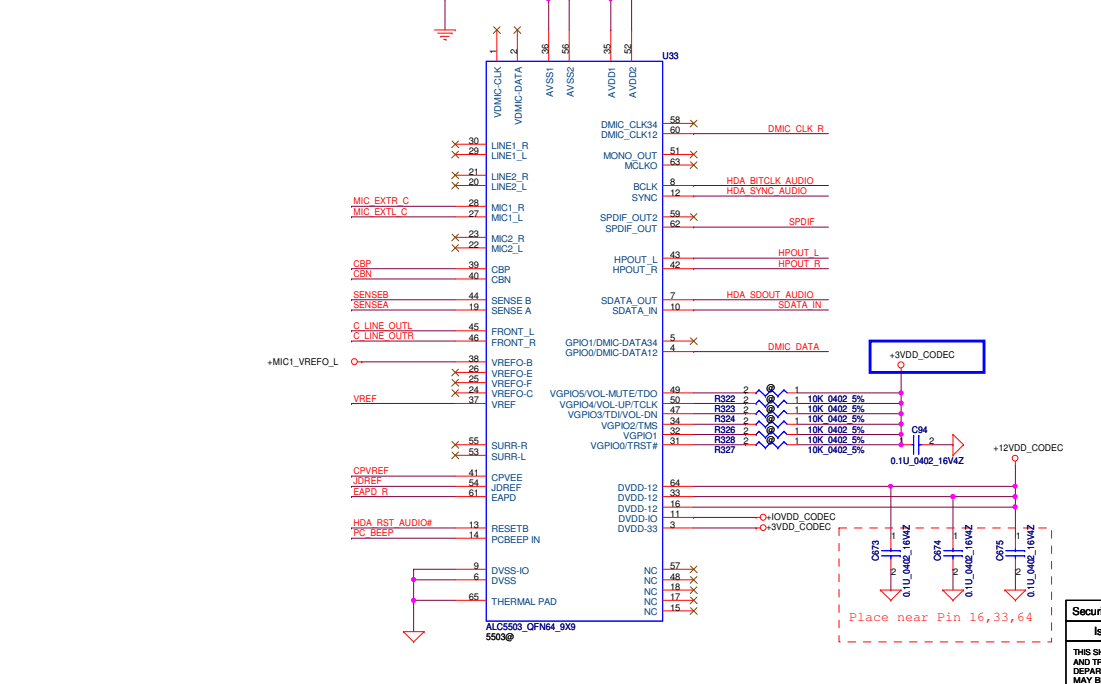
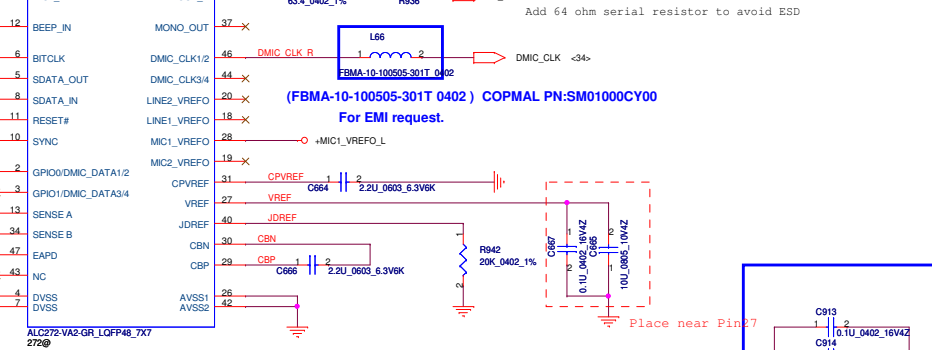
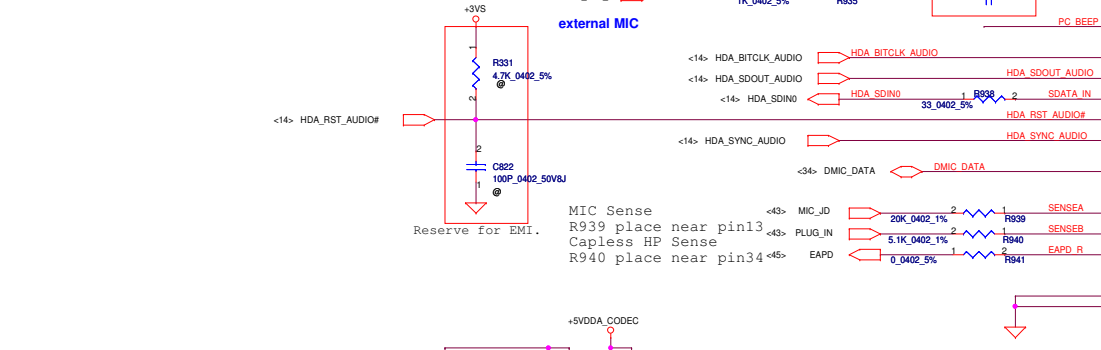
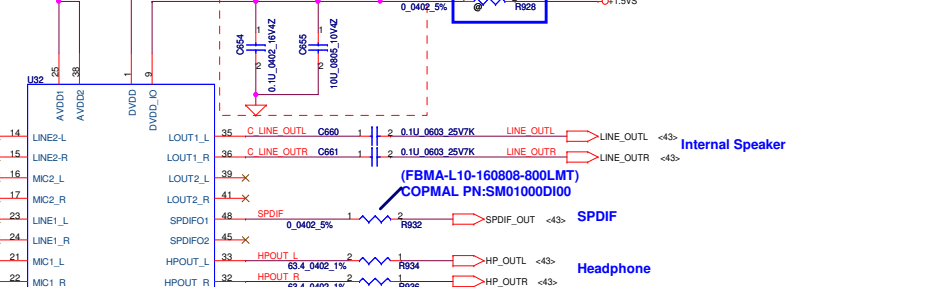
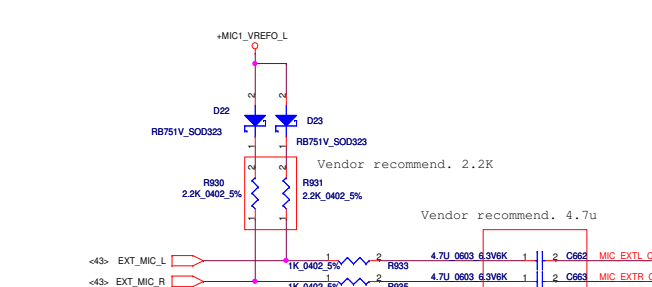
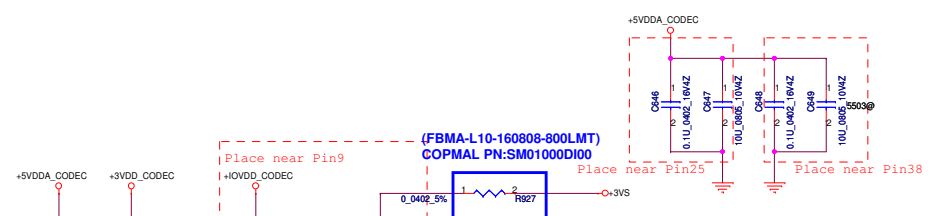
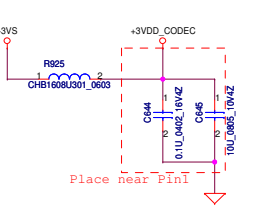
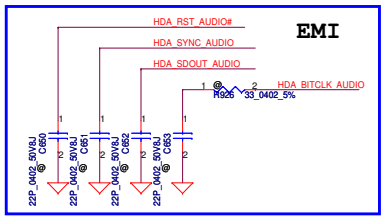
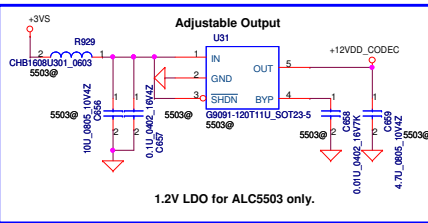
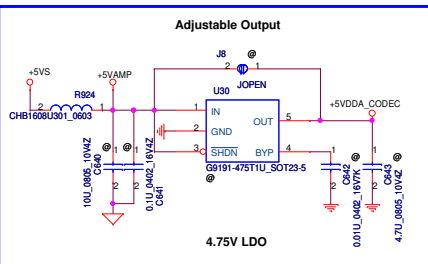
SATA ODD Conn.



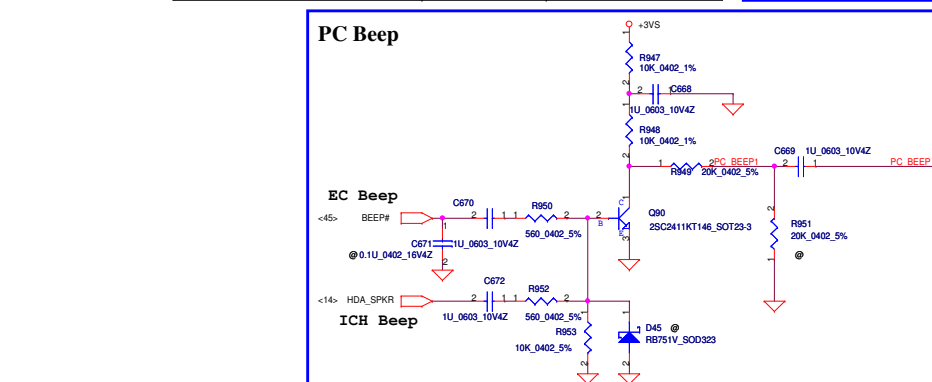
ODD Power Control



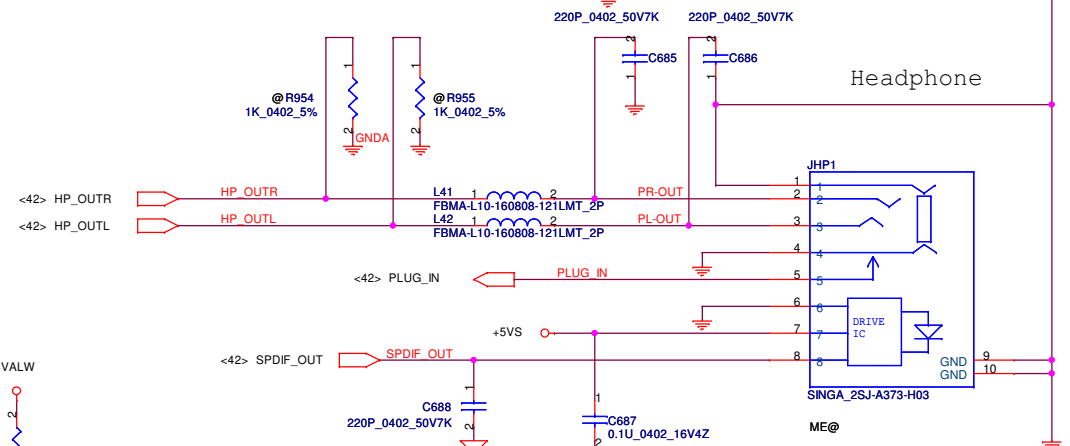
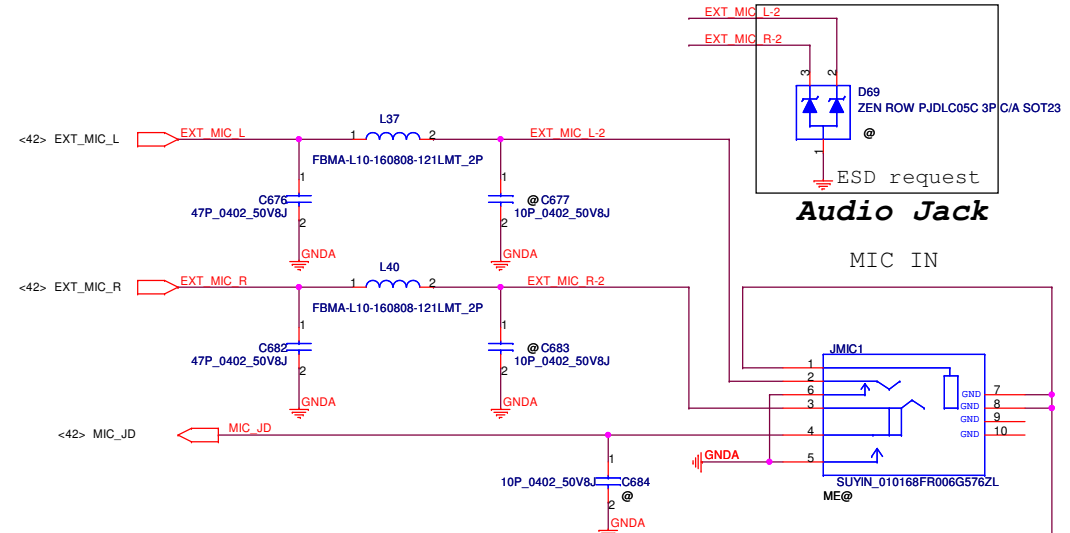
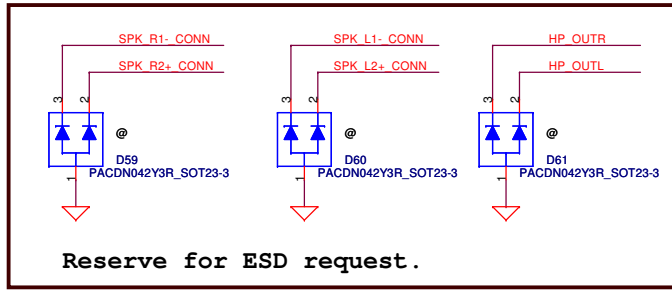
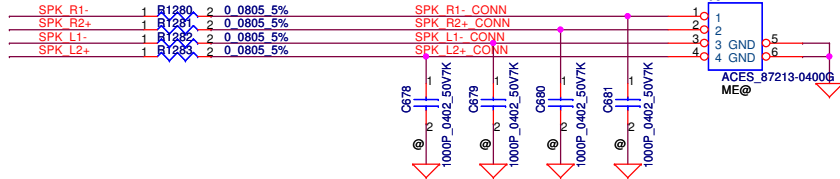
Security Classification	Compal Secret Data			Title		
Issued Date	2010/11/30	Deciphered Date	2011/08	Compal Electronics, Inc.		
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				Size B	Document Number	Rev 1.0
				PIQY0 LA6881P		
Date: Wednesday, January 05, 2011				Sheet	41	of 63



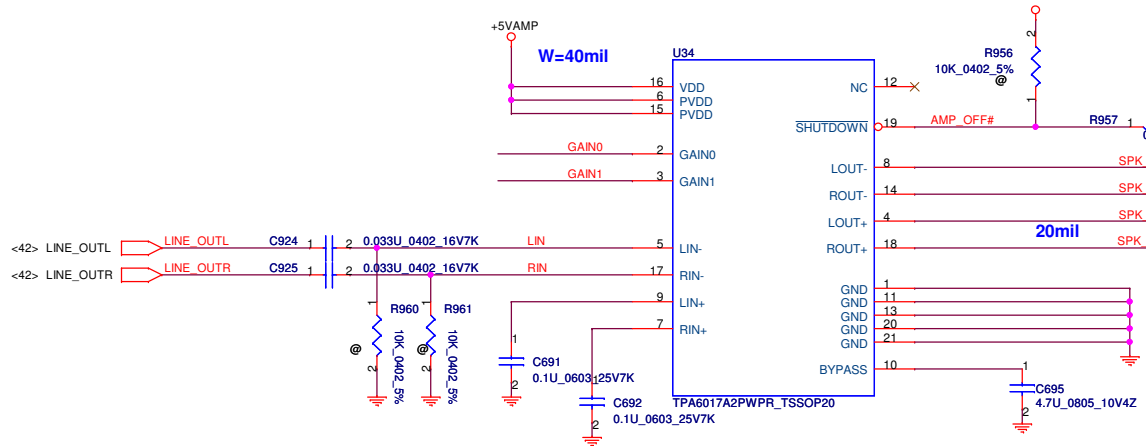
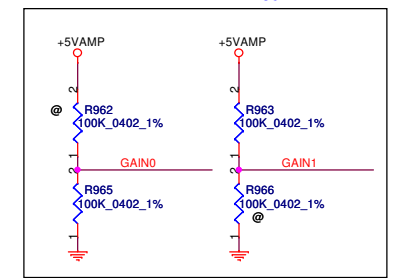
Pin Assignment	Location	Function
LINE-OUT (Pin35/36)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
LINE1 (Pin23/24)	External	Line in
MIC1 (Pin21/22)	External	Mic in
MIC2 (Pin16/17)	Internal	Internal Mic



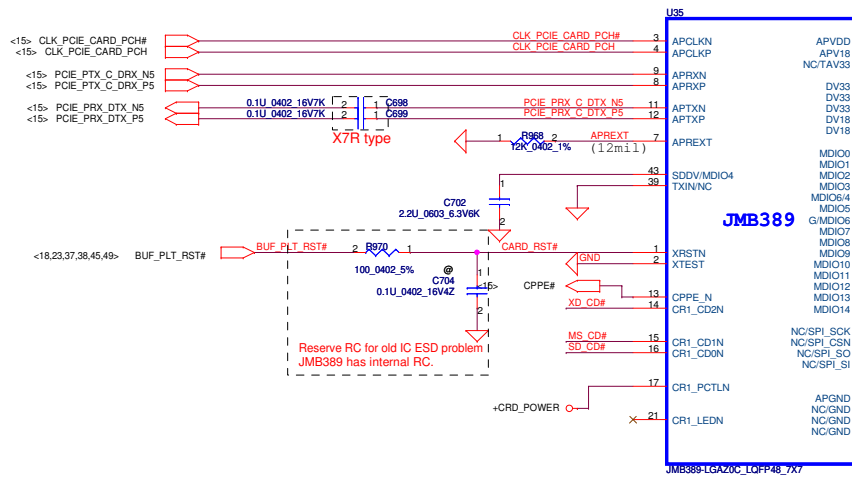
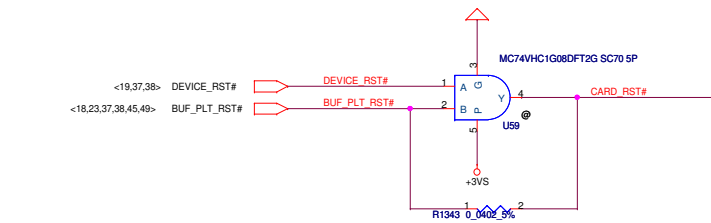
wide 20MIL



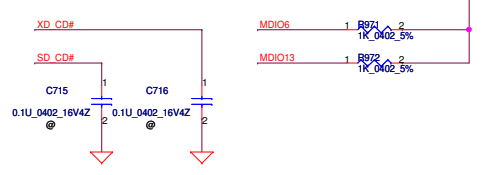
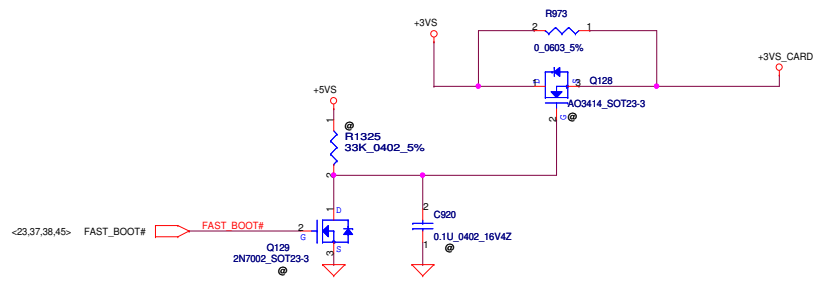
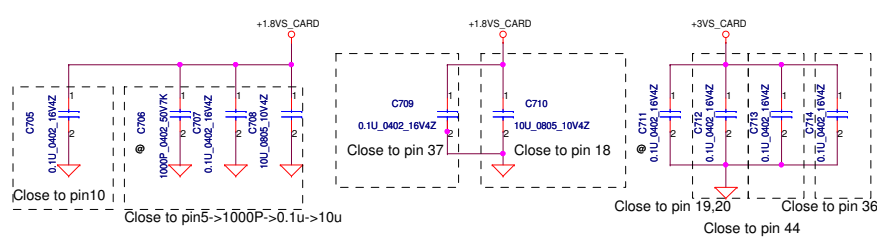
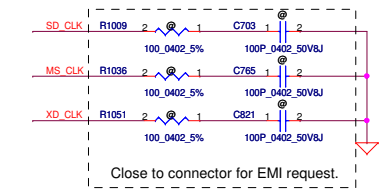
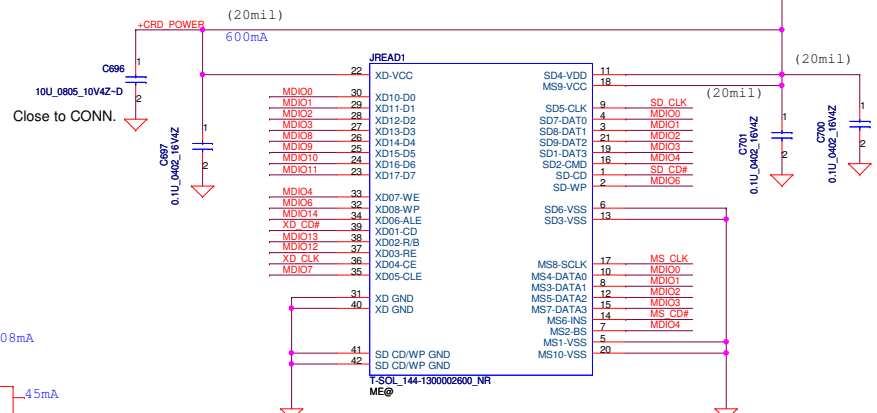
GAIN0	GAIN1	Gain
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB



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Size	Custom	Document Number	KIWB1/B2_LA4601P	Rev	1.0
Date	Wednesday, January 05, 2011	Sheet	43	of	63

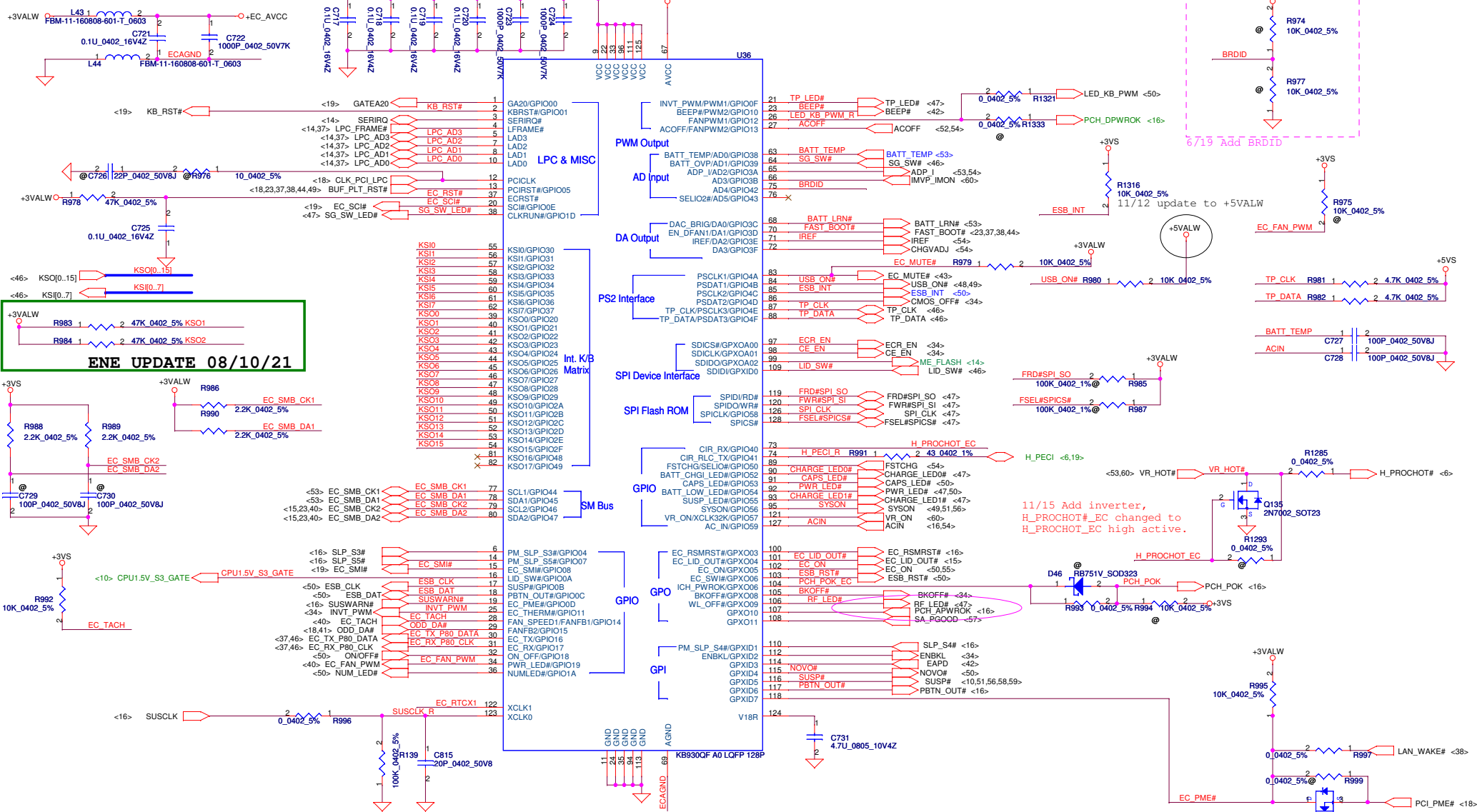


Reserve RC for old IC ESD problem
JMB389 has internal RC.

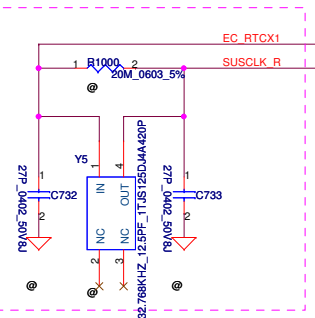


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Issued Date	2010/11/30	Deciphered Date	2011/08	Carder JMB389	
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Size	Document Number	Rev	PIQY0 LA6881P		
Date:	Wednesday, January 05, 2011	Sheet	44	of	63

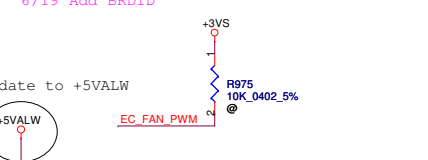
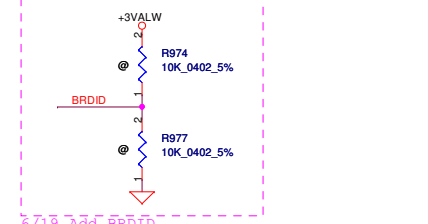
10/02 Change to SM01000550.



ENE UPDATE 08/10/21



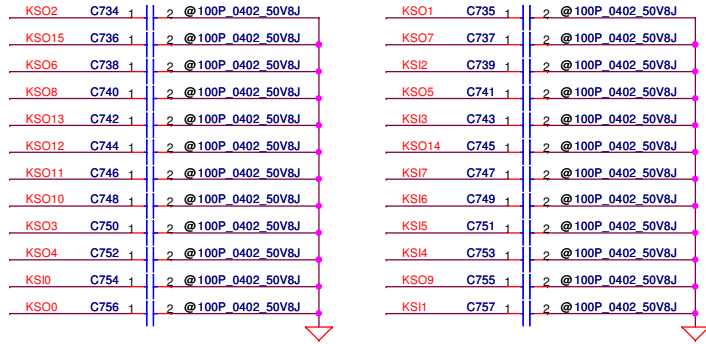
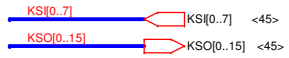
6/15 add XTAL



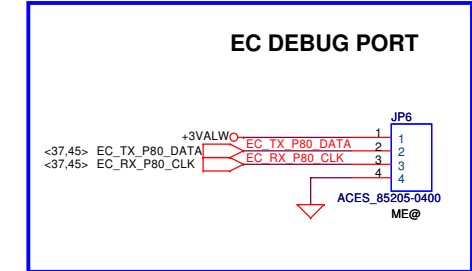
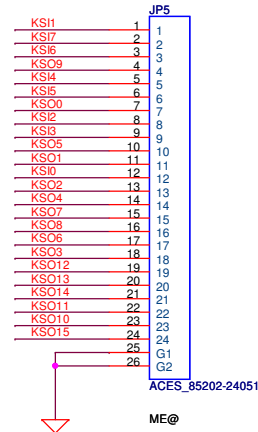
11/15 Add inverter, H_PROCHOT#_EC changed to H_PROCHOT# high active.

Security Classification		Compal Secret Data		Title	
Issued Date	2010/11/30	Deciphered Date	2011/08	BIOS & EC I/O Port	
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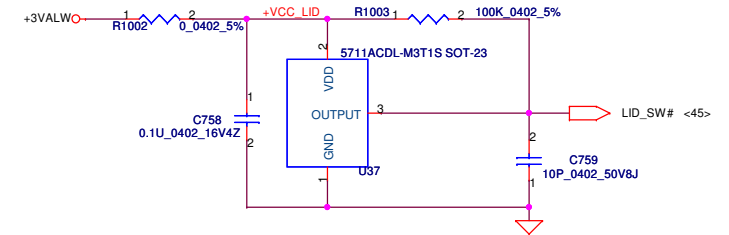
INT_KBD Conn.



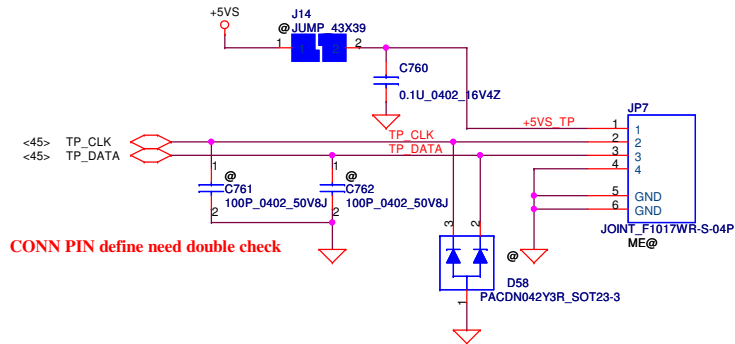
CONN PIN define need double check



Lid Switch

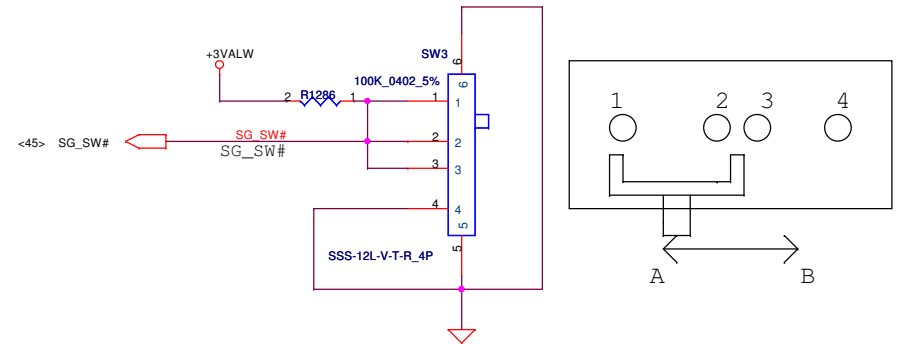
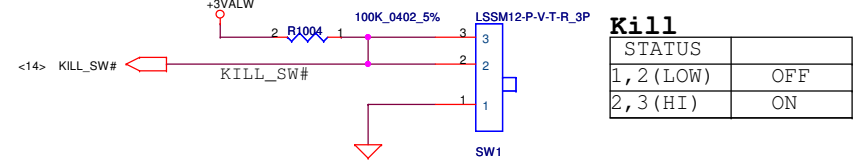


To TP/B Conn.



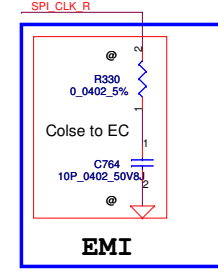
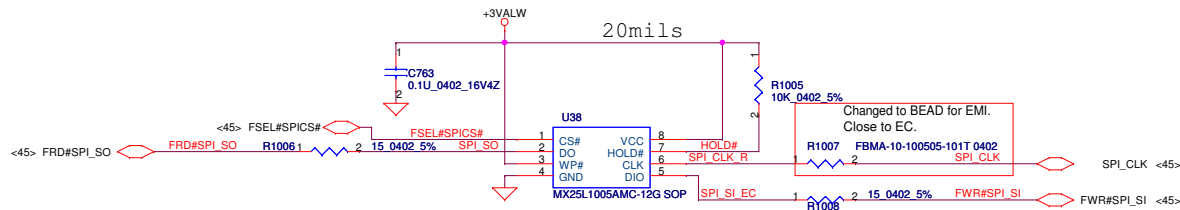
CONN PIN define need double check

Kill Switch

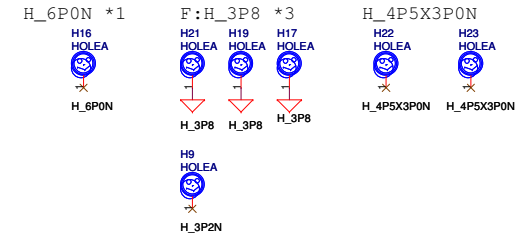
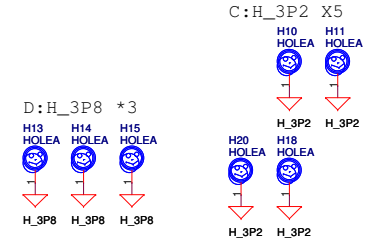
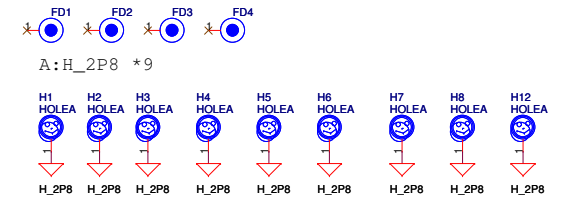
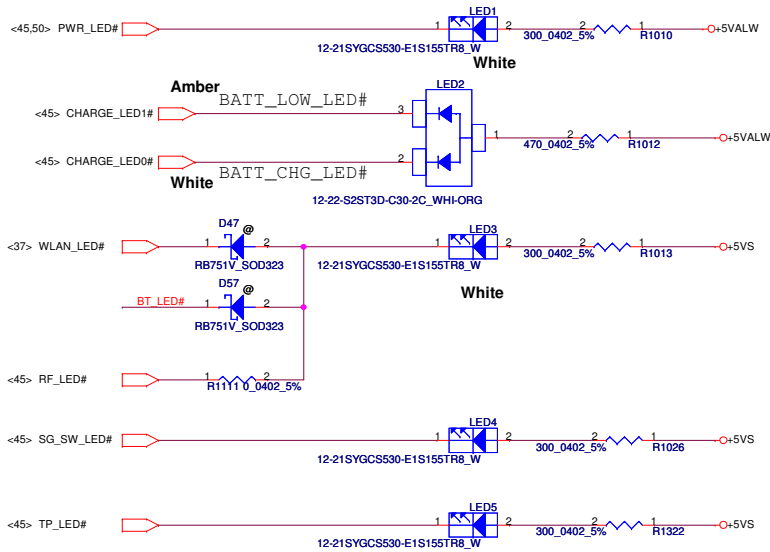


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Size	Document Number	Date		Rev
B	PIQY0 LA6881P	Wednesday, January 05, 2011		1.0
		Sheet	46	of 63

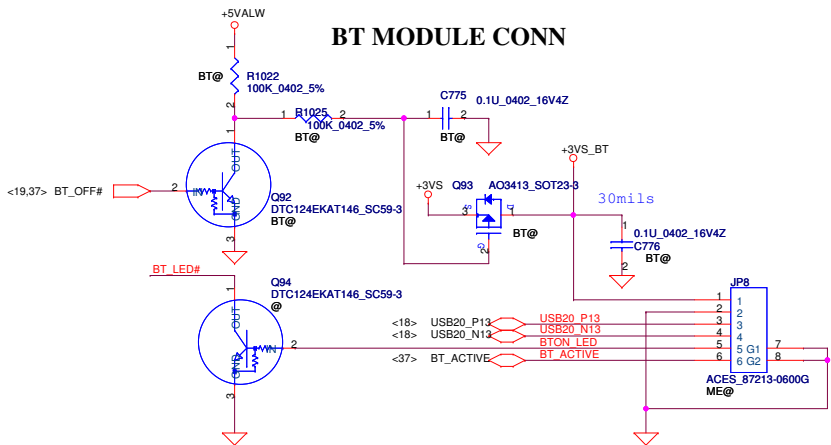
**FOR EC 128KB SPI ROM
(150mil PACKAGE)
P/N : SA00002C100**



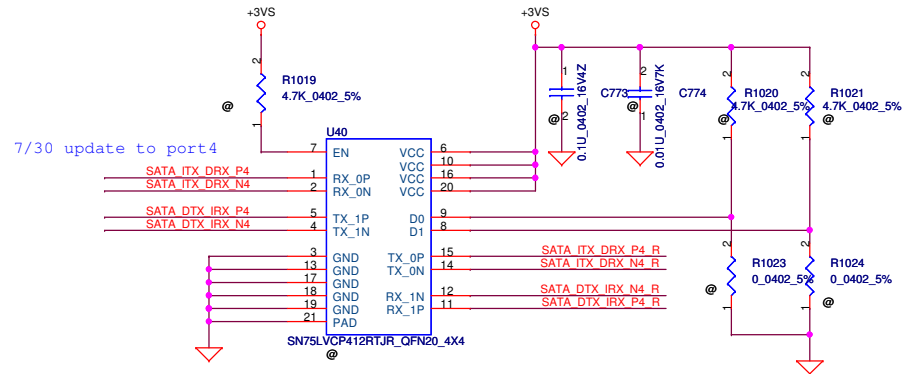
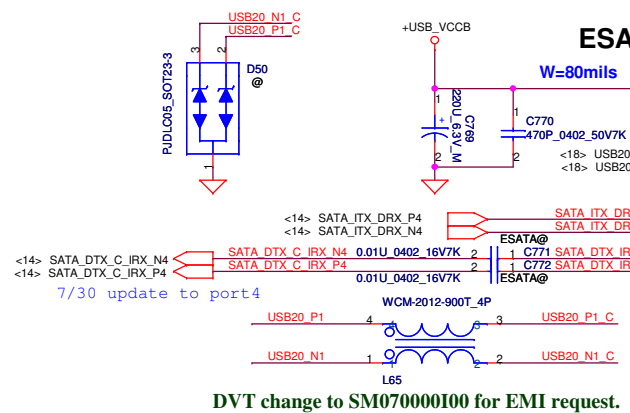
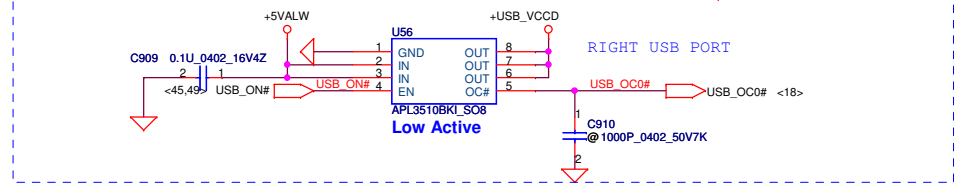
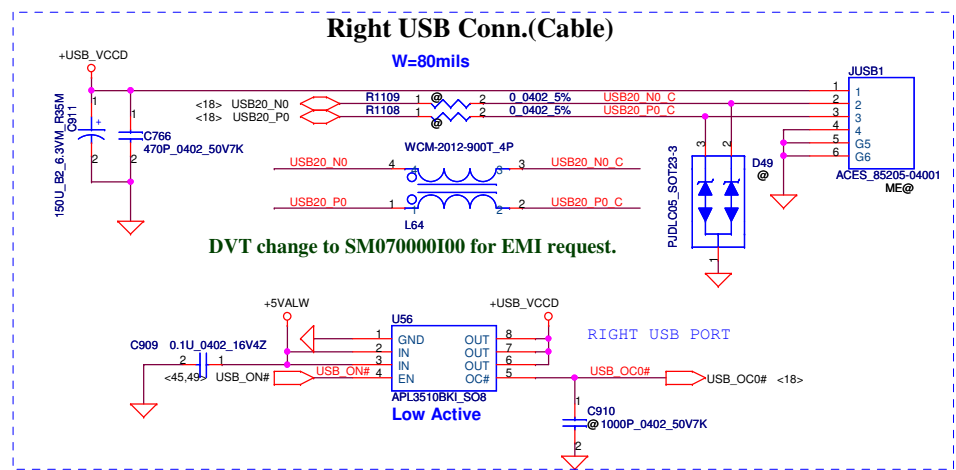
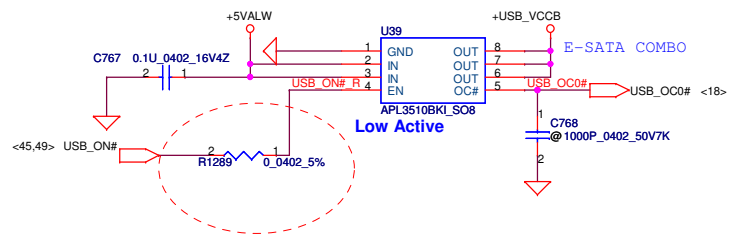
LED



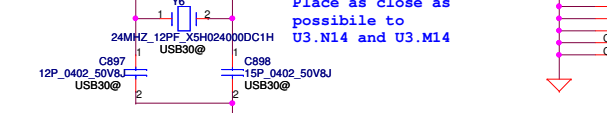
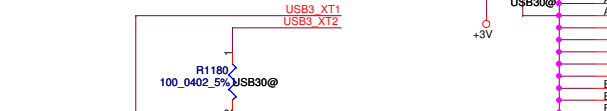
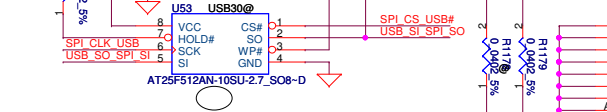
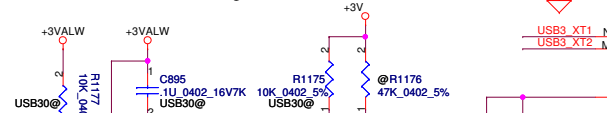
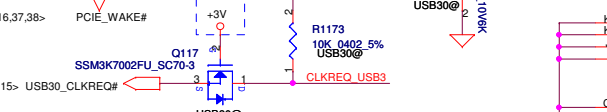
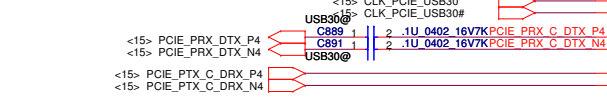
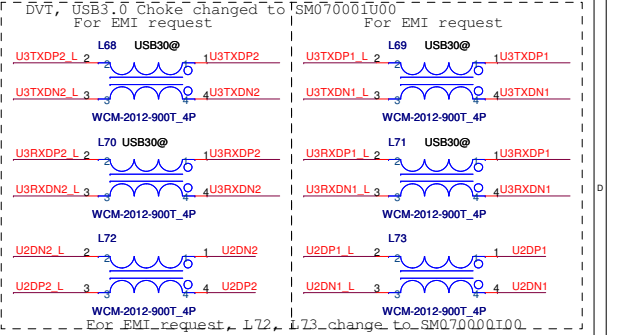
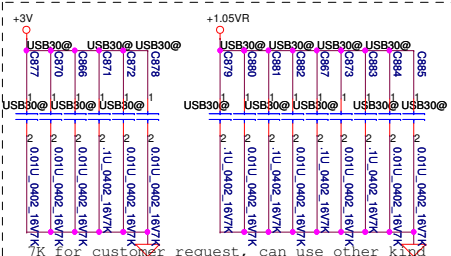
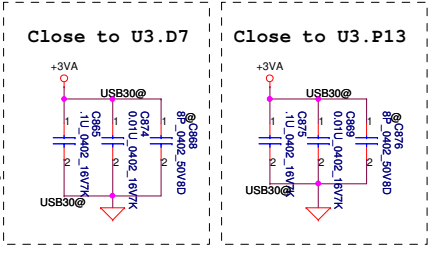
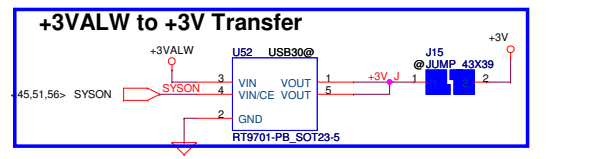
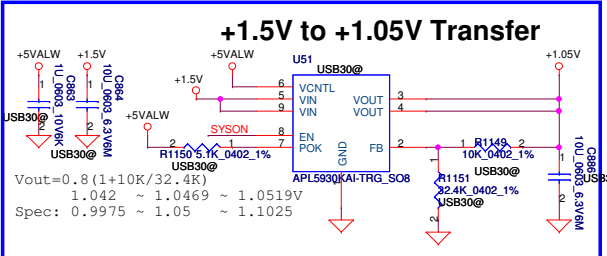
BT MODULE CONN



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						Custom	PIQY0 LA6881P
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Pin compare table for support USB remote wakeup or not

	AUXDET(Pin J2)	CSEL(Pin P6)	CLK
Support USB remote wakeup	pull high 10k to VDD33	Tied to GND	Must use 24MHz crystal: mount Y1,R19,C40,C41
Not support USB remote wakeup	Tied to GND	pull high to VDD33	Can use either 48MHz or 24MHz When use 48MHz clock: mount R22,R25

SPEC Max: +3V---200mA; +1.05V---800mA
Idle mode: 0.489W;
+3V---43mA; +1.05V---328mA
D3 mode: 0.066W;
+3V---5.4mA; +1.05V---45mA

Can be attach to EC, either.

PCI Express/ExpressCard select signal (others: Express Card or Mini card)

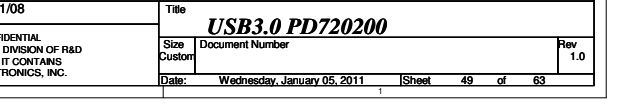
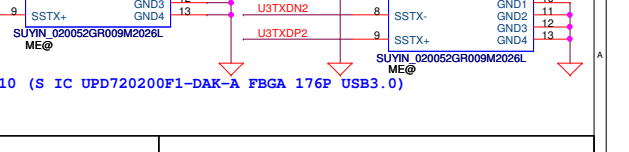
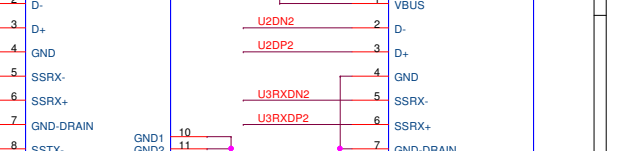
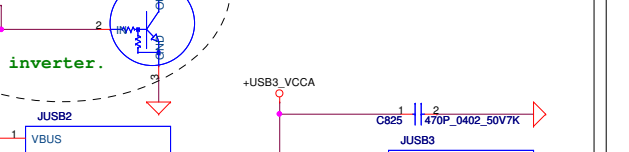
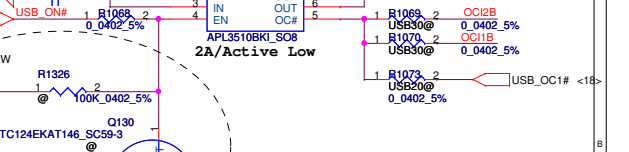
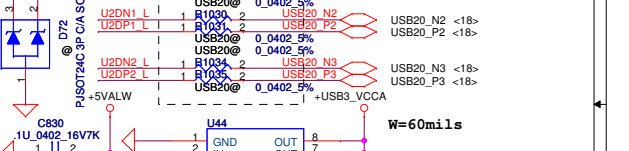
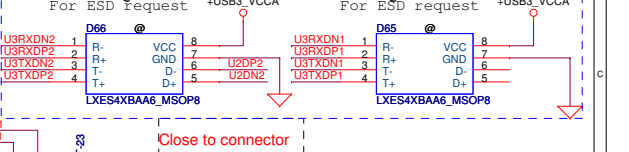
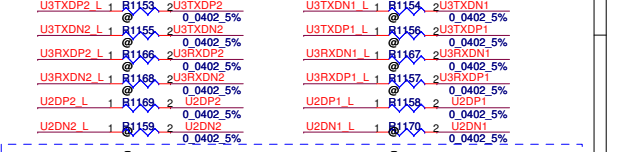
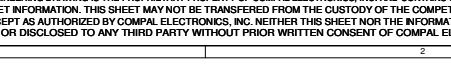
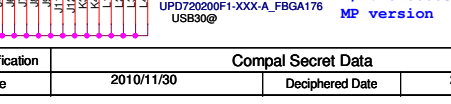
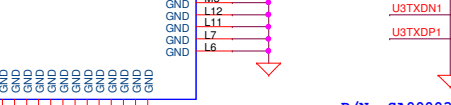
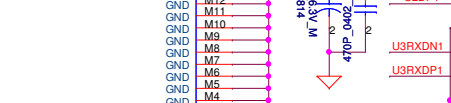
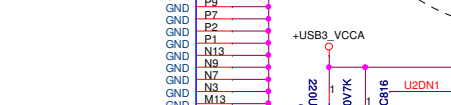
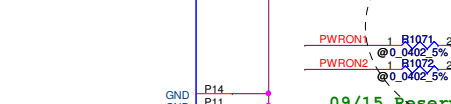
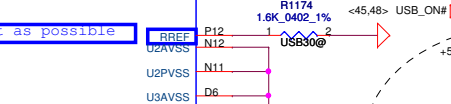
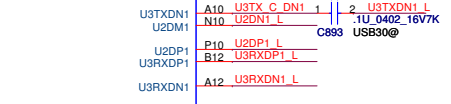
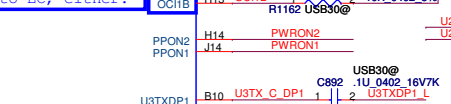
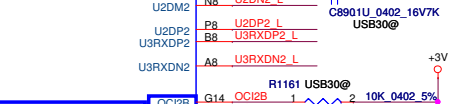
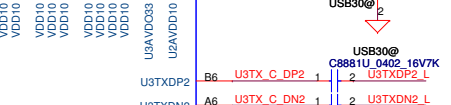
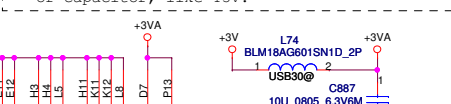
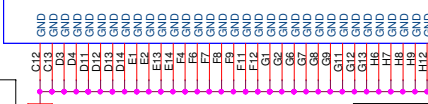
As short as possible

Place as close as possible to U3.N14 and U3.M14

W=60mils

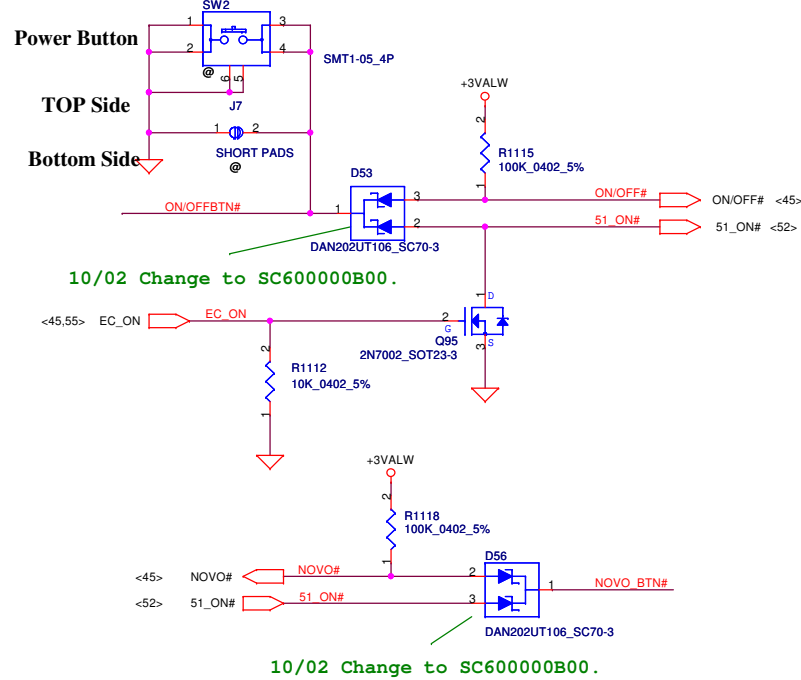
09/15 Reserve inverter.

P/N: SA00033W10 (S IC UPD720200F1-DAK-A FBGA 176P USB3.0) MP version

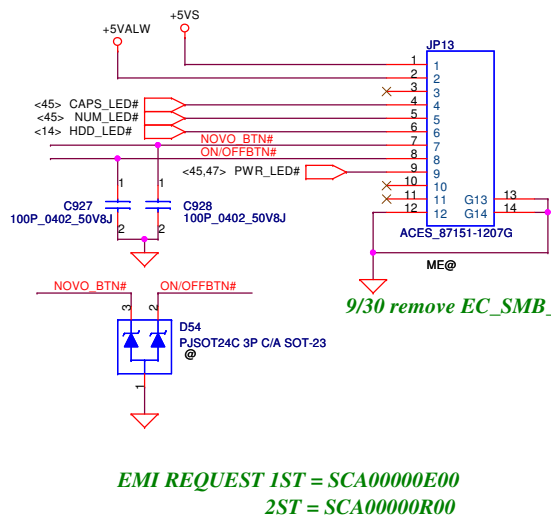


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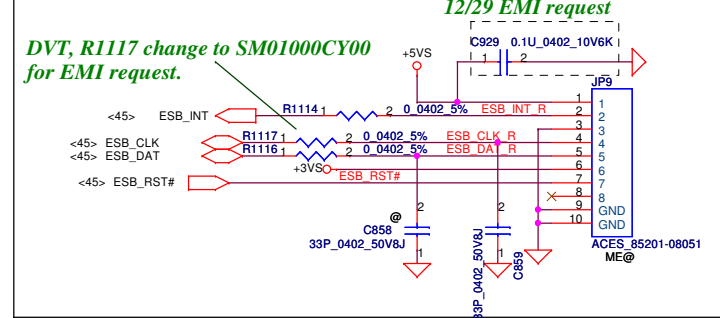
ON/OFF switch



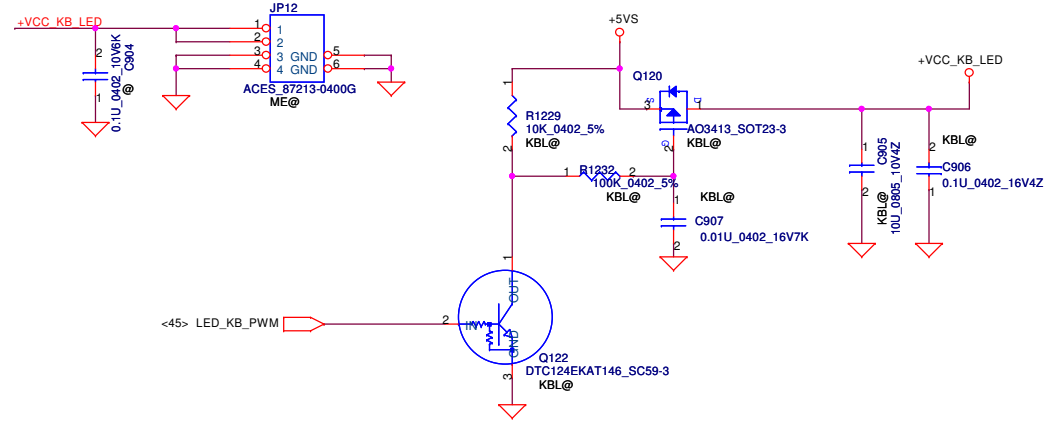
Power Bottom Board Conn. 10pin



Slider Bar Board Mdule Conn. 6pin

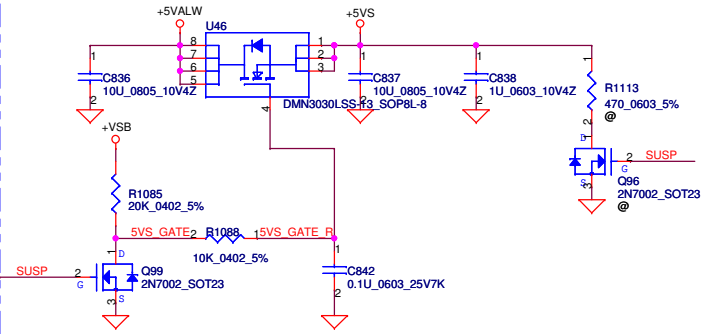


KB Lighting CONN.4pin

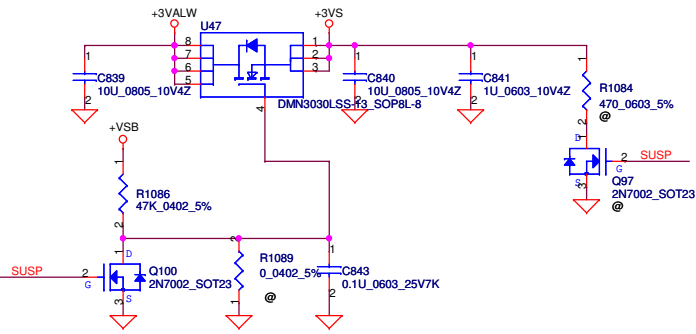


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Size Custom	Document Number	PIQY0 LA6881P		Rev 1.0
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+5VALW TO +5VS

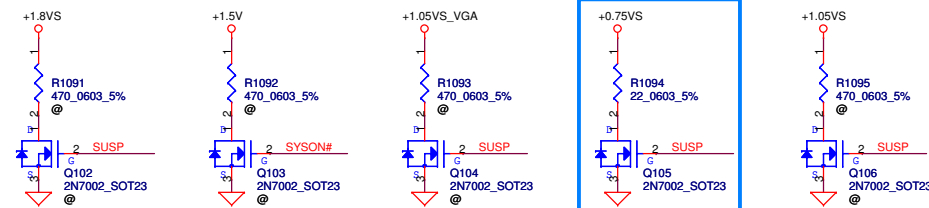
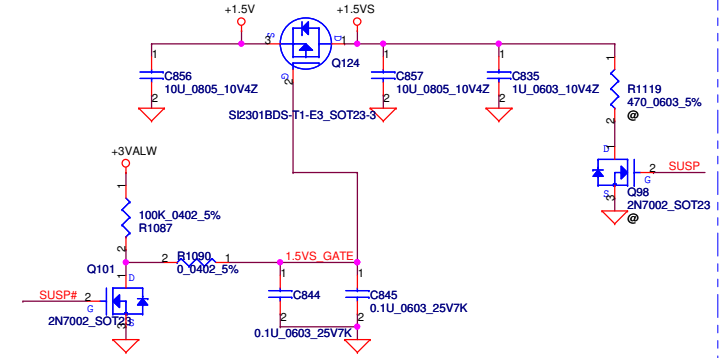


+3VALW TO +3VS

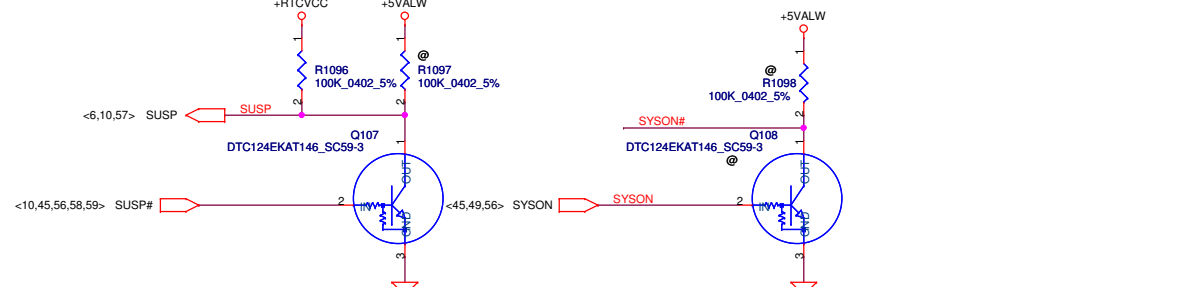


+1.5V to +1.5VS

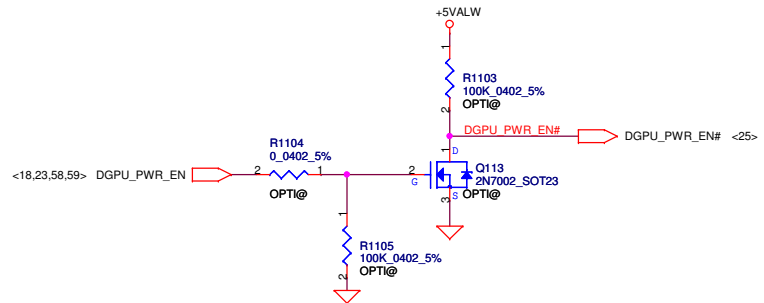
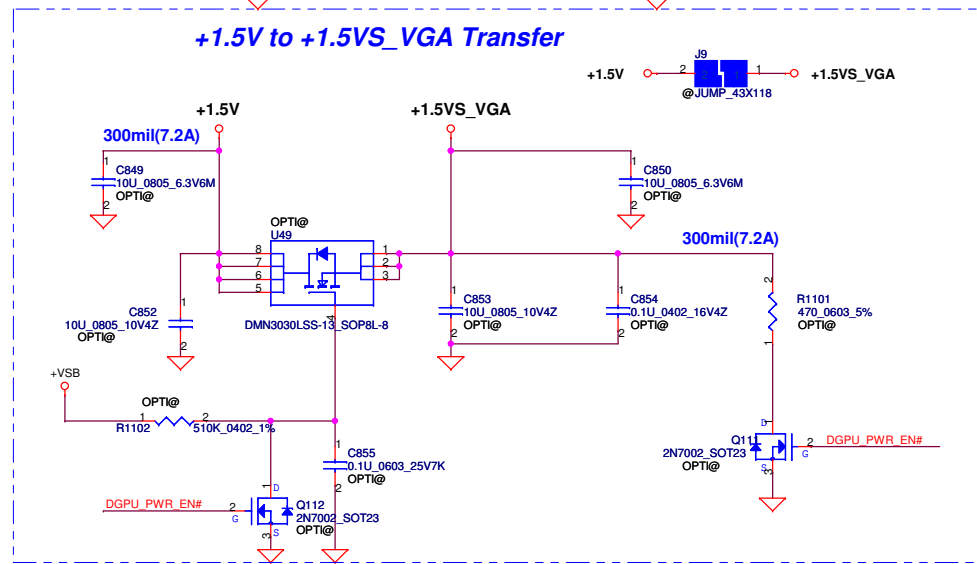
7/26 change SI4800 to SI2301



For Intel S3 Power Reduction.

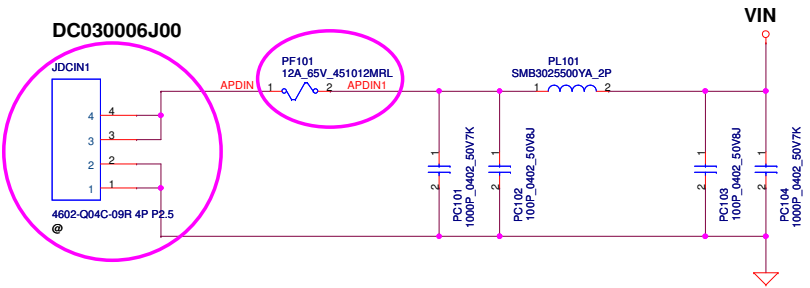


+1.5V to +1.5VS_VGA Transfer

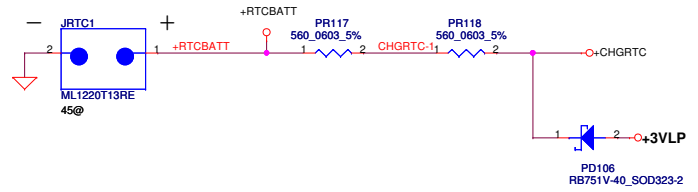
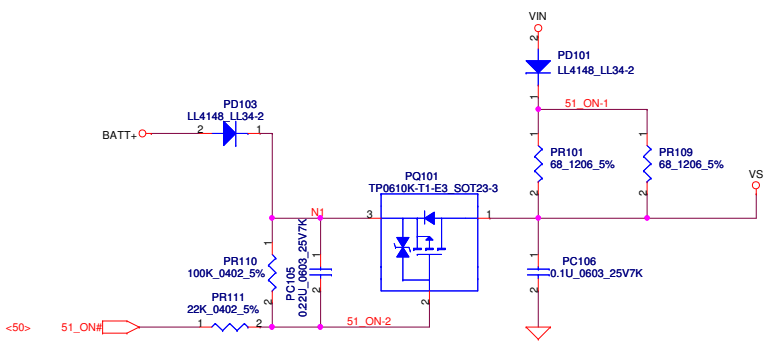
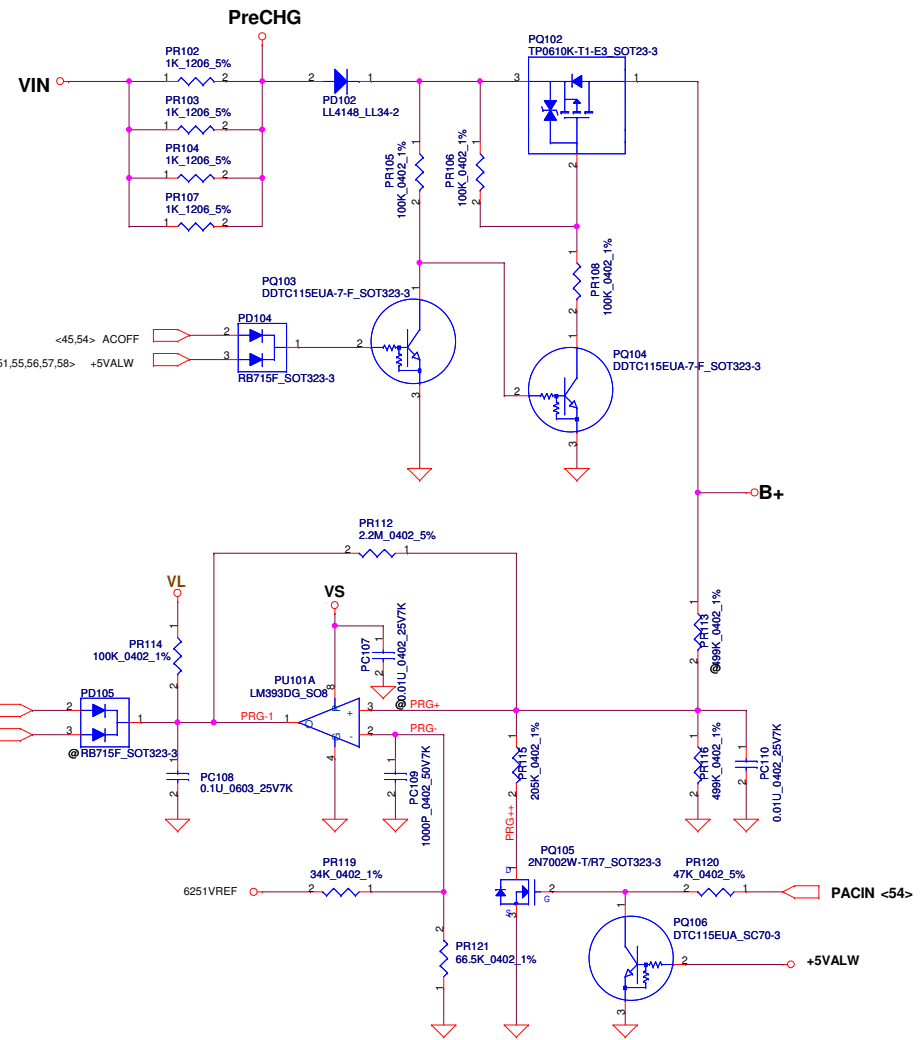


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				of	63

DC030006J00



**Precharge detector
15.97V/14.84V FOR
ADAPTOR**



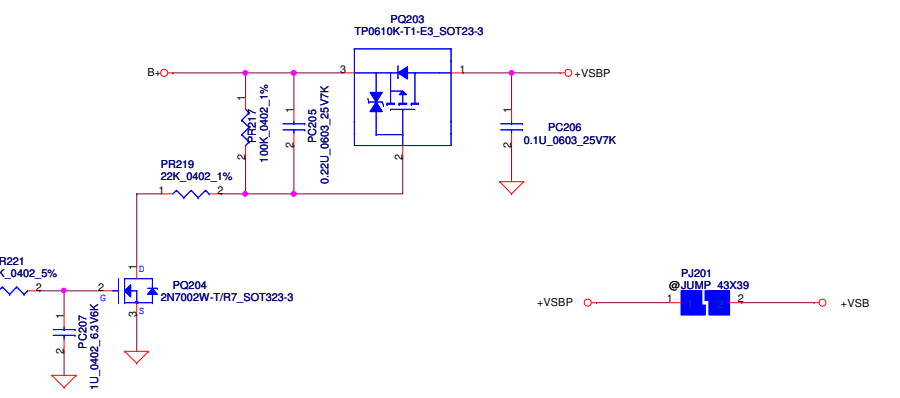
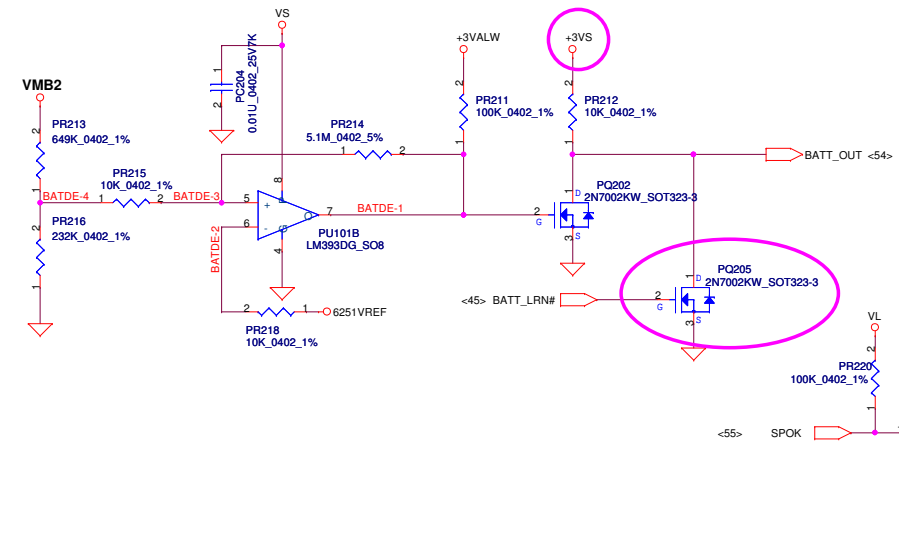
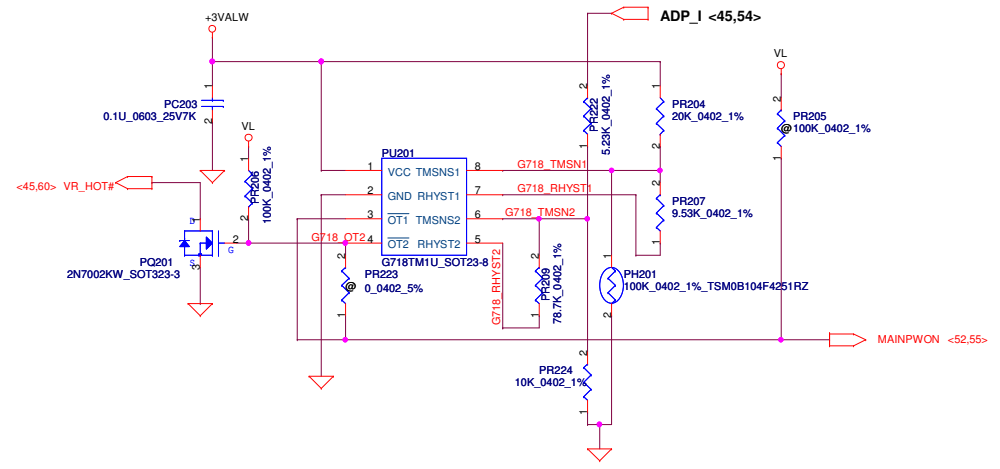
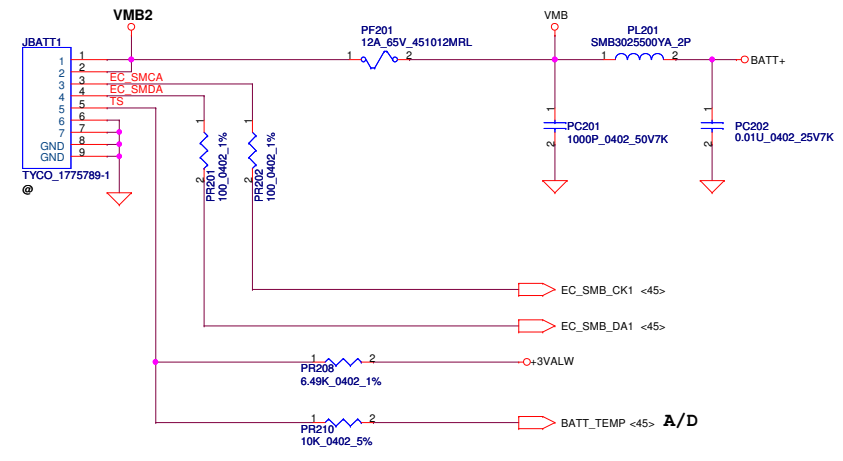
ACIN

Precharge detector			
Min.	typ.	Max.	
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

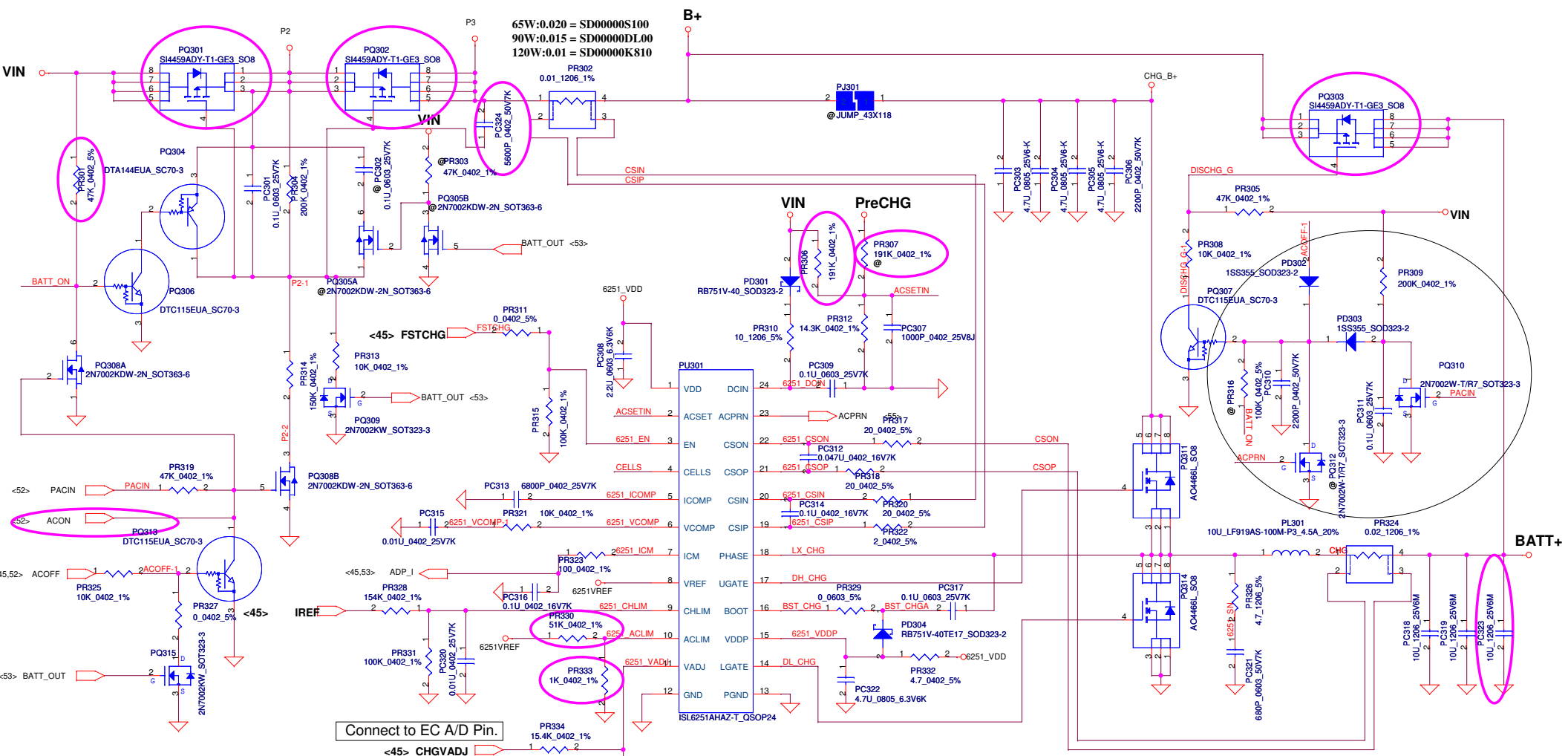
BATT ONLY

Precharge detector			
Min.	typ.	Max.	
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V

PH201 under CPU bottom side :
 CPU thermal protection at 95 degree C
 Recovery at 56 degree C



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Connect to EC A/D Pin.

CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A-3A
 IREF=1.016*Icharge
 IREF=0.254V-3.048V
 VCHLIM need over 95mV

65W Adapter
 $V_{aclim}=2.39*(1.96K/(1.96K+16.9K))=0.2484V$
 $I_{input}=(1/0.02)((0.05*V_{aclim})/2.39+0.05)$
 where $V_{aclim}=0.2484V$, $I_{input}=2.76A$

90W Adapter
 $V_{aclim}=2.39*(2.87K/(2.87K+16.9K))=0.347V$
 $I_{input}=(1/0.015)((0.05*V_{aclim})/2.39+0.05)$
 where $V_{aclim}=0.347V$, $I_{input}=3.82A$

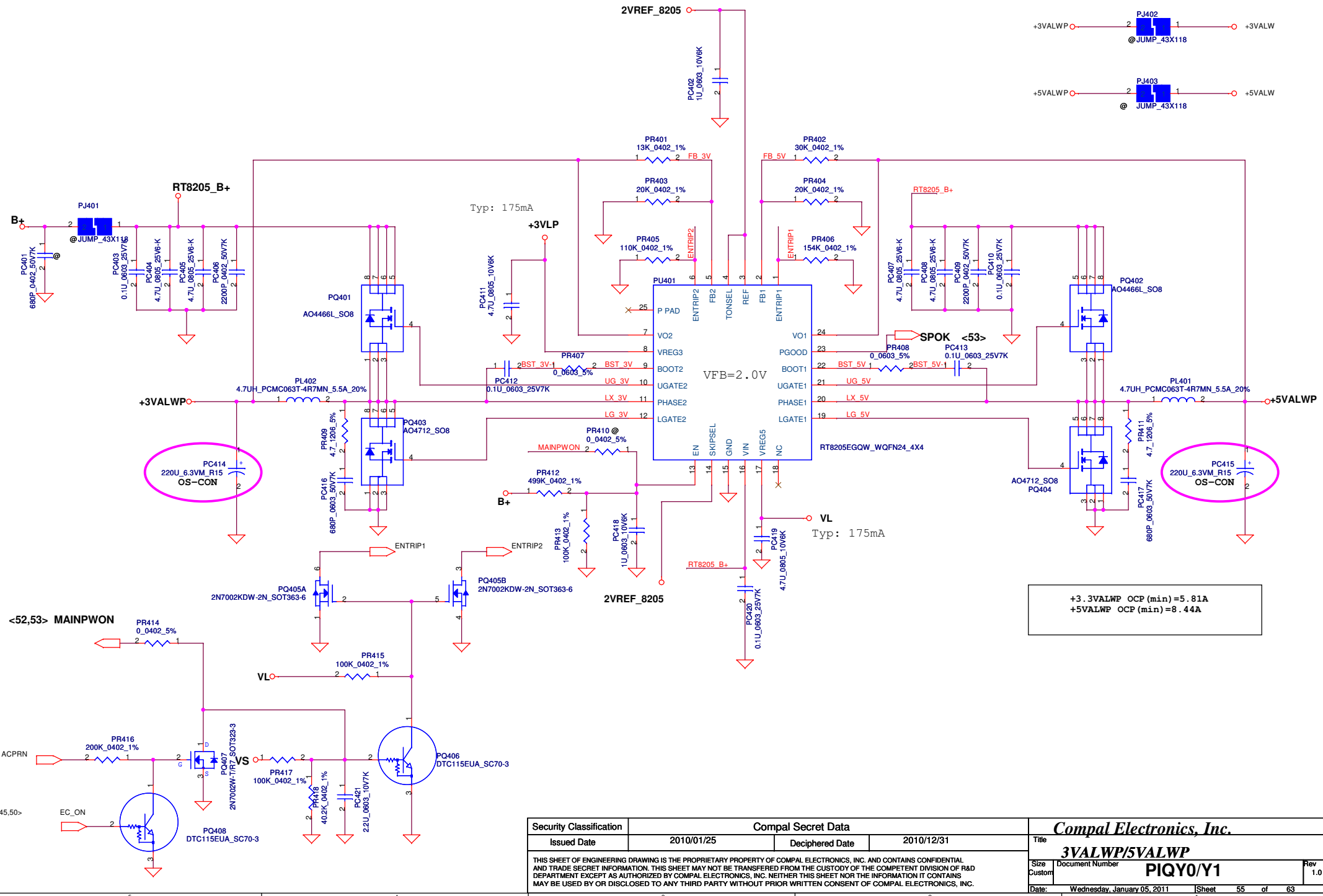
120W Adapter
 $V_{aclim}=2.39*(1K/(1K+50K))=0.047V$
 $I_{input}=(1/0.01)((0.05*V_{aclim})/2.39+0.05)$
 where $V_{aclim}=0.047V$, $I_{input}=5.1A$

65W : PR330=16.9K, PR333=1.96K
 90W : PR330=16.9K, PR333=2.87K
 120W : PR330=50K, PR333=1K

3cell : GND
 4cell : VDD

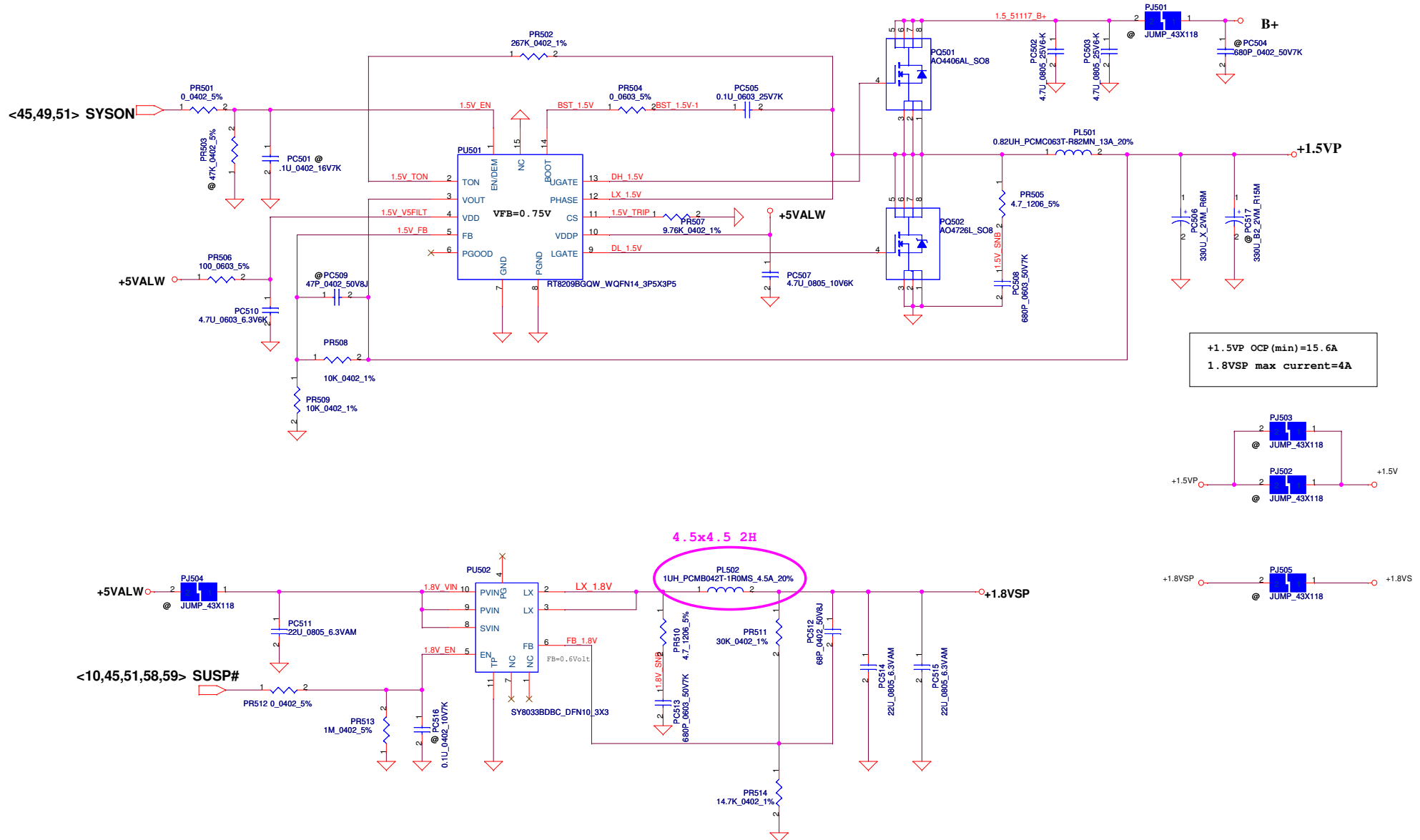
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Issued Date	2010/01/13	Deciphered Date	2011/01/13	Title
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				Document Number
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				1.0
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Note:
 Use TPS51125 IC can remove RTC referenece LDO
 Use TPS51427 IC must keep RTC referenece LDO



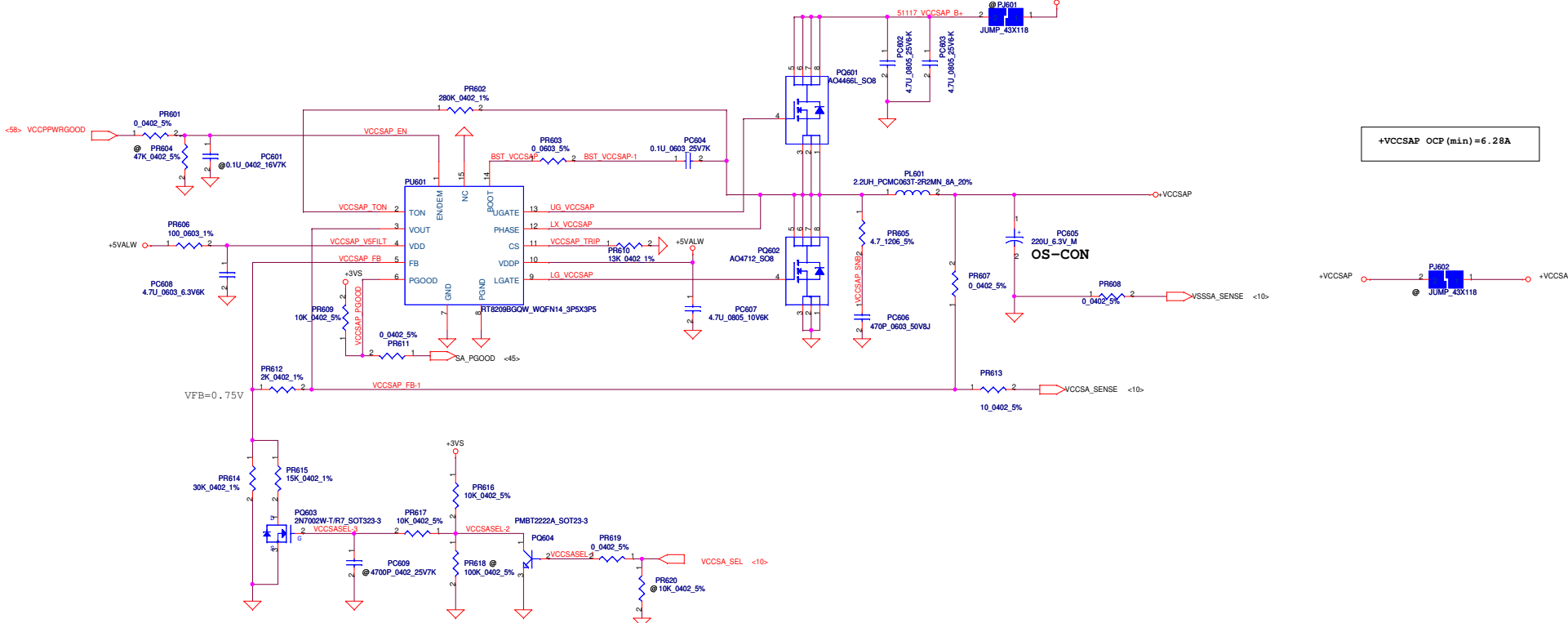
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Compal Electronics, Inc.			
Title	3VALWP/5VALWP		
Size	Document Number	PIQY0/Y1	
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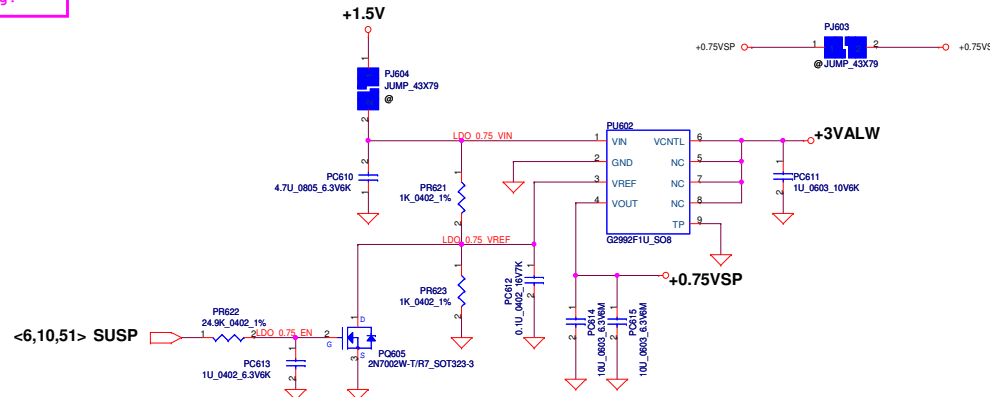
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/01/25	Deciphered Date	2010/12/31	Title	PWR-+1.5VP/+1.8VSP
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Customer				Rev	1.0
Date:	Wednesday, January 05, 2011	Sheet	56	of	63

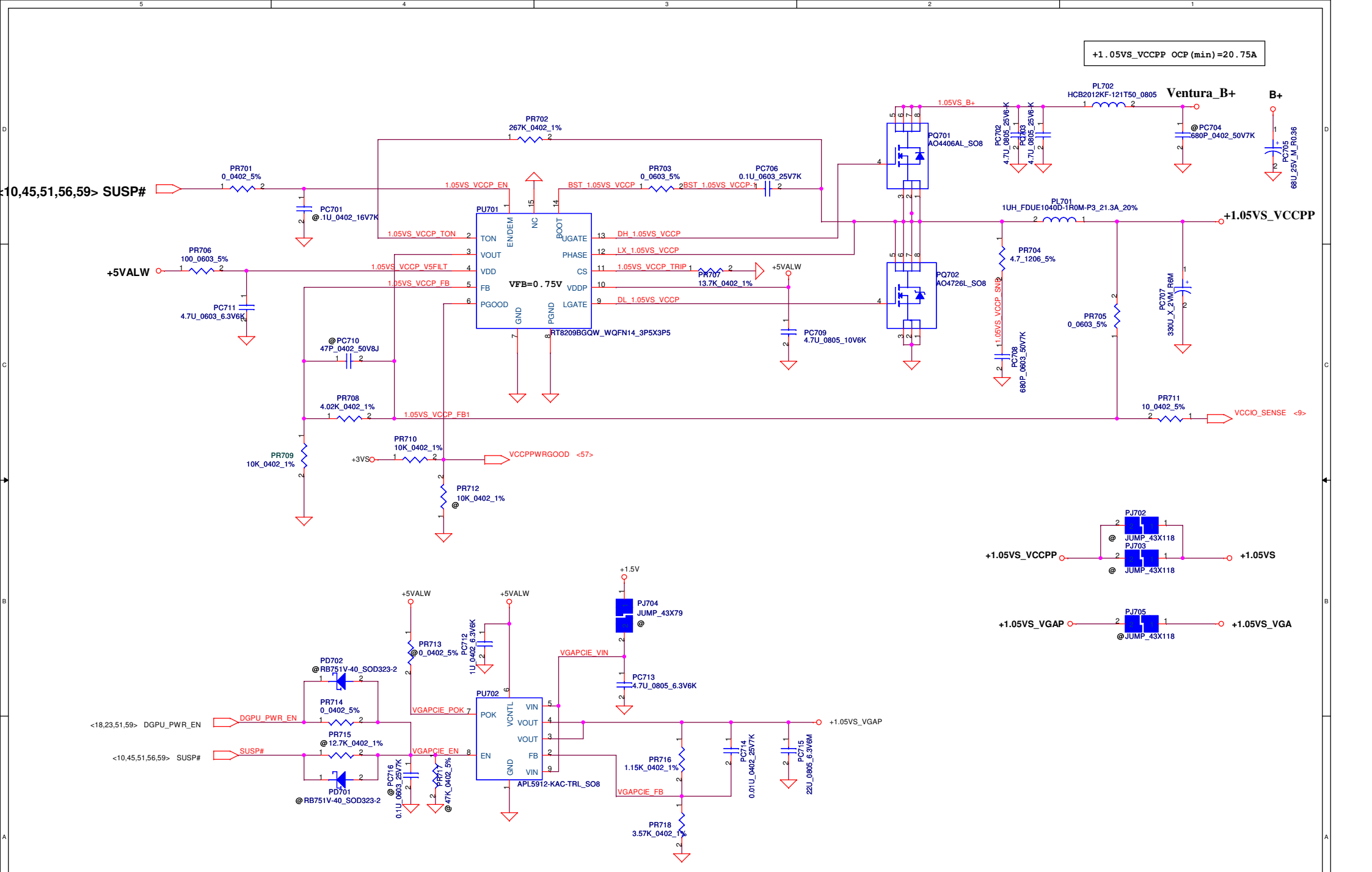
Ventura_B+



VID[0]	VID[1]	VCCSA Vout	Require on 2011/ 2012 Required
0	0	0.9 V	Yes/Yes
0	1	0.8 V	Yes/Yes
1	1	0.75V	No/Yes
1	1	0.65V	No/Yes

Note: Use VCCSA_SEL to switch High & Low Level for VID[1] (ie. VCCSA_SEL) due to the VID[0] is don't care for this setting.





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Compal Electronics, Inc.			
Title PWR +1.05VS_VCCPP/1.05VS_VGA			
Size Custom	Document Number PIQY0/Y1	Rev 1.0	
Date	Wednesday, January 05, 2011	Sheet	58 of 63

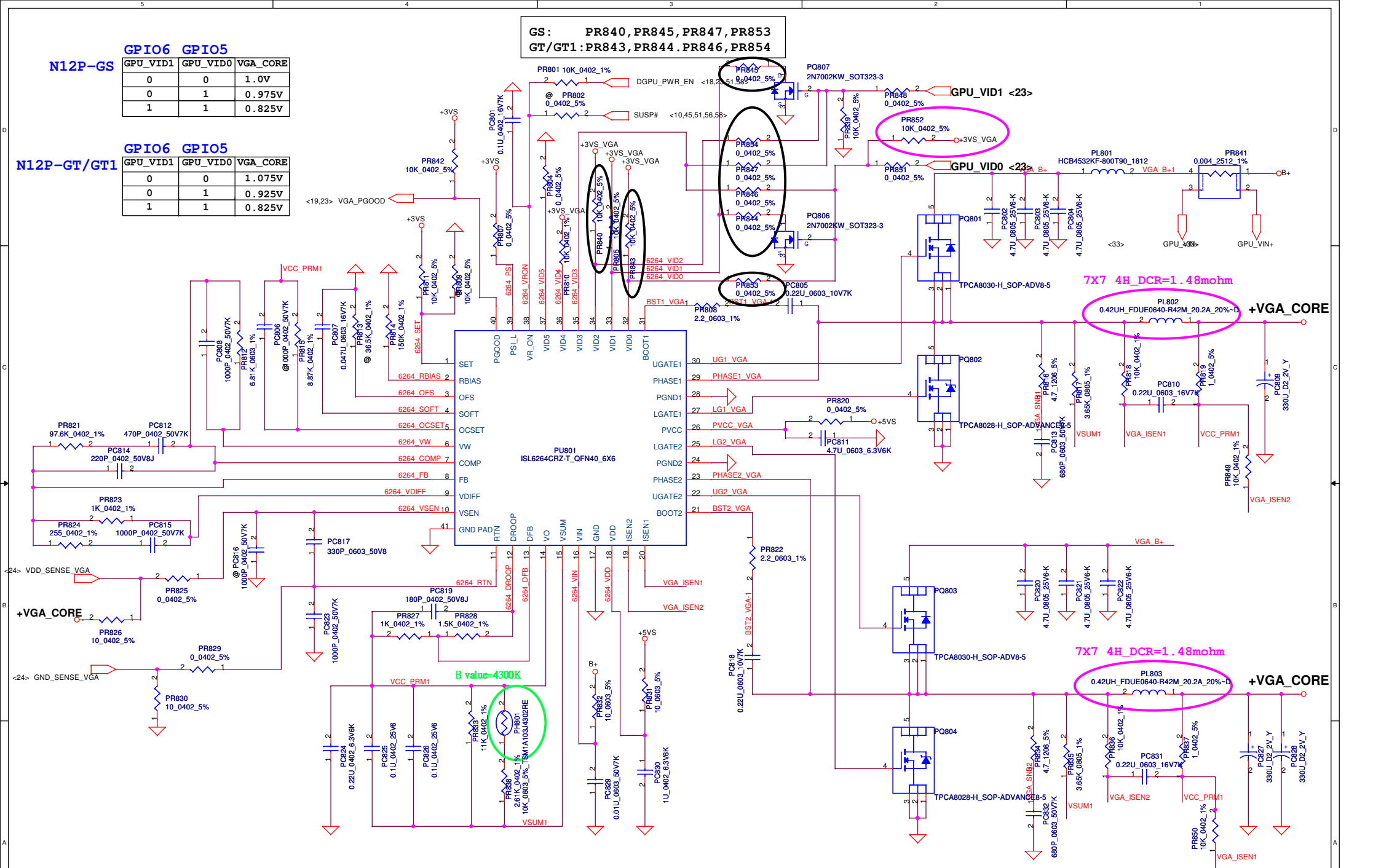
GS: PR840, PR845, PR847, PR853
 GT/GT1: PR843, PR844, PR846, PR854

N12P-GS

GPIO6	GPIO5	VGA_CORE
0	0	1.0V
0	1	0.975V
1	1	0.825V

N12P-GT/GT1

GPIO6	GPIO5	VGA_CORE
0	0	1.075V
0	1	0.925V
1	1	0.825V

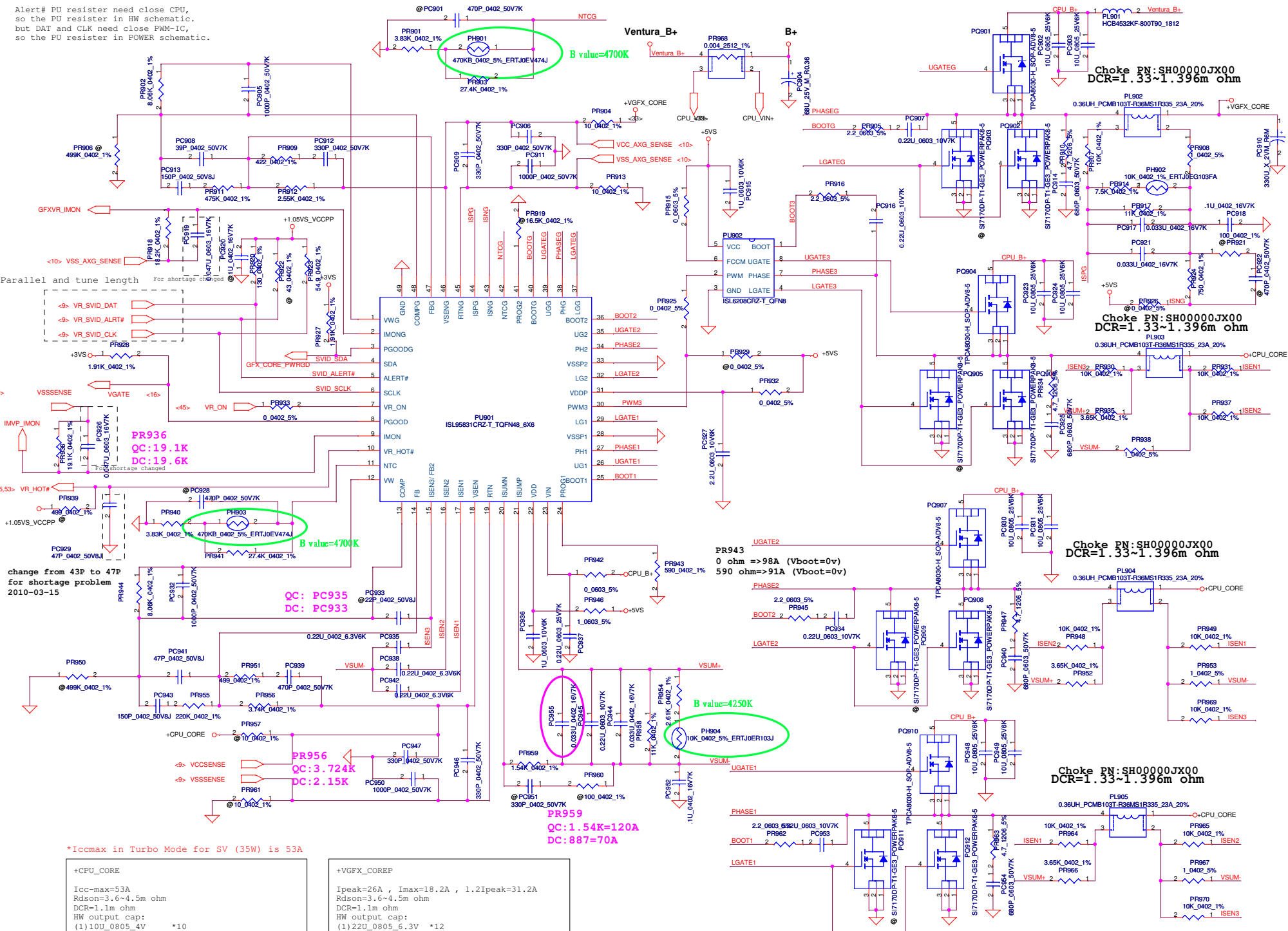


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		2007/12/12

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Title			Compal Electronics, Inc.
Size			Power-VGA_CORE
Document Number	PIQY0/Y1		Rev
Custom			1.0
Date:	Wednesday, January 05, 2011	Sheet	59 of 63

Alert# PU resistor need close CPU,
so the PU resistor in HW schematic.
but DAT and CLK need close PWM-IC,
so the PU resistor in POWER schematic.



Parallel and tune length
For shortage changed

- <-> VR_SVID_DAT
- <-> VR_SVID_ALRT#
- <-> VR_SVID_CLK

change from 43P to 47P
for shortage problem
2010-03-15

QC: 19.1K
DC: 19.6K

QC: PC935
DC: PC933

PR956
QC: 3.724K
DC: 2.15K

*Iccmax in Turbo Mode for SV (35W) is 53A

+CPU_CORE
Icc-max=53A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1) 10U_0805_4V *10
(2) 22U_0805_6.3V *15
(3) 470U_D2_2V *4 (ESR=4.5m ohm)

*OCP setting value=71.5A

+VGFX_COREP
Ipeak=26A, Imax=18.2A, 1.2Ipeak=31.2A
Rdson=3.6~4.5m ohm
DCR=1.1m ohm
HW output cap:
(1) 22U_0805_6.3V *12
(2) 470U_D2_2V *2 (ESR=4.5m ohm)

*OCP setting value=37A

PR943
0 ohm => 98A (Vboot=0v)
590 ohm=> 91A (Vboot=0v)

PR959
QC: 1.54K=120A
DC: 887=70A

Security Classification	Compal Secret Data	
Issued Date	2010/01/25	Deciphered Date
		2010/12/31

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Compal Electronics, Inc.
Title: PWR +CPU_CORE/+VGFX_CORE

Size	Document Number	PIQY0/Y1	Rev	1.0
Customer				
Date:	Wednesday, January 05, 2011	Sheet	60	of
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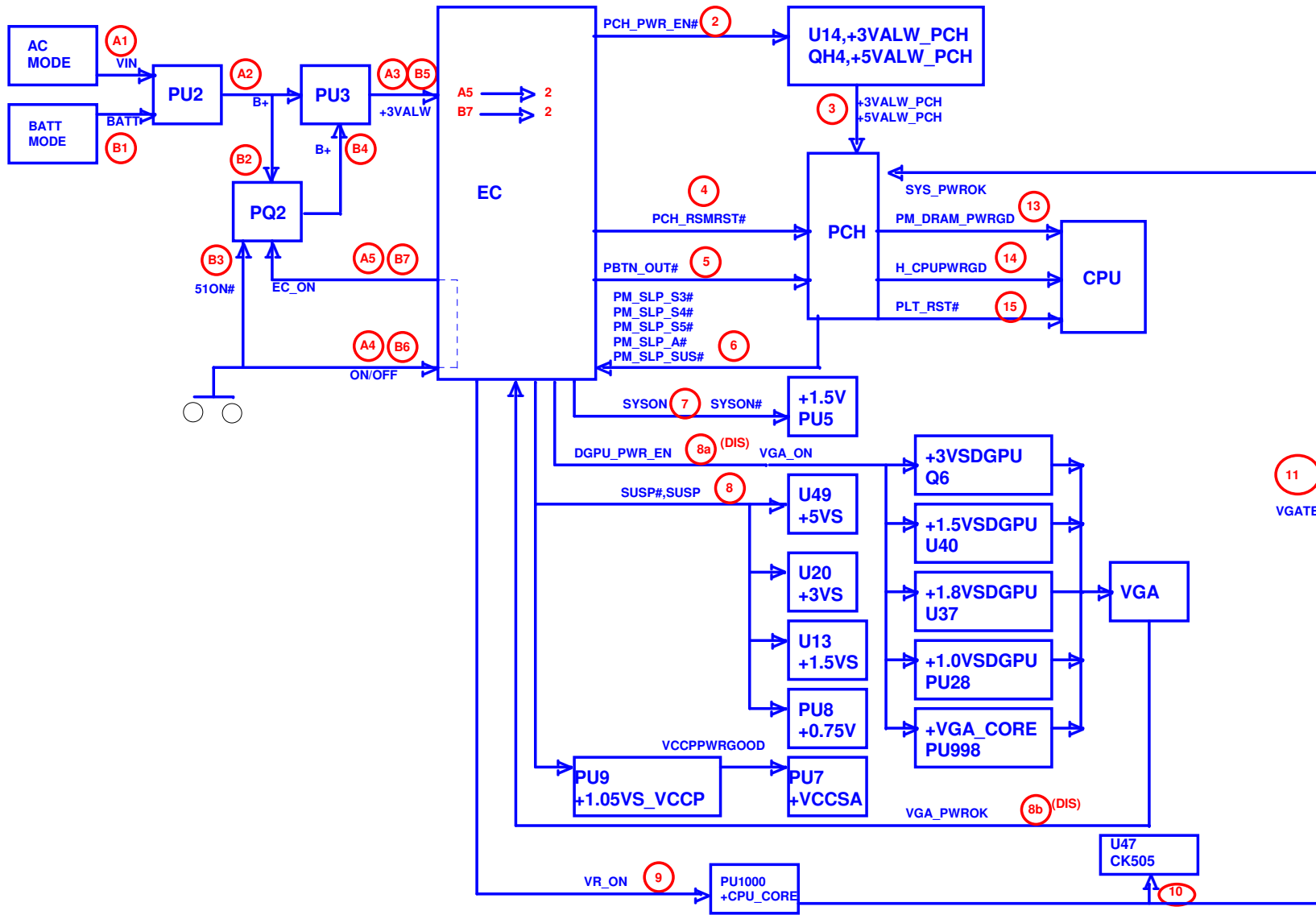
Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification		Compal Secret Data		Title	
Issued Date	2009/01/06	Deciphered Date	2009/01/06	PIR (PWR)	
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				Rev	1.0

PIQY0 HW PIR List

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
----- DVT TO DVT				
1		P18	Reserve R297	Reserve pull down for PCH GP1053.
2		P18	Exchange SATA port0 & port1	For fast boot function.
3		P50	Change KB light control circuit	Change KB light control from PWM to on/off.
			Delete U55, C908, R1233, R1235, R1236, 1238, R1230, R1231, Q121	
4		P36	Add F2 (poly-fuse)	For HDMI port diode protection.
5		P19	Stuff R303, unstuff R340	Change ESATA_DET# to GP101.
6		P49	Stuff R1068, reserve R1326, Q130	Reserve USB3.0 power swith control inverter circuit.
7		P48	Add R1327	For CHG_ON# pull down.
8		P45	Stuff R996, R139, C815, unstuff R1000, C732, C733, Y5	Change EC CLK from crystal to SUSCLK.
9		P37	Add U60, Q132, C921, R1329, Q133, R1328	Add WLAN power switch circuit
10		P34	Modify JLVDS1	Modify connector from 40pin to 30pin.
11		P09	Add C922	Add C922 to place at CPU sdie.
12		P21	Add R1330	Add for INTVREN control
13		P41	Modify C639	Modify type from 0805 to 0603
14		P45	Modify TP_LED#, PCH_DPWROK and LED_KB_PWM link	Change LED_KB_PWM to U36. pin26 GP1012.
15		P18	Delete EN_CARD_PW#, EN_WOL#	Add FAST_BOOT# to replace EN_CARD_PW# and EN_WOL#
16		P48		Remove USB charger function
17		P42	Change C660, C661 from 3300p to 0.1u	For 100Hz High Pass filter
18		P43	Replace R958, R959 to C924, C925 0.033u	For 100Hz High Pass filter
19		P14	Add one more SPI-ROM circuit	For dual BIOS function
20		P50	Remove EC_SMB_CK2, EC_SMB_DA2 link to JP13	Remove light sensor function
21		P14	Add Q134, R1345, R1346	Add for Fast boot SPI ROM selection by EC.
22		P34	Add R1341, C926	Added for EMI request
23		P37, P44	Add R1342, R1343	Added for WLAN and CARD reader Reset signal.
24		P19	Add R1344	Added for VENTURA detection.
----- DVT TO PVT				
1		P10	Add R1347, Change R56 to 20K,	Modify S3 1.5V reduction sequence.
2		P45	Add Q135	Modify PROCHOT control circuit.
			Modify R980 link to +5VALW	Change USB_ON PU power rail
----- PVT TO SVT				
1		P23, P45	FAST_BOOT#	Link FAST_BOOT# to VGA GP1012
2		P50	Add C929	EMI Request
2		P14	Add R1348	INTEL Design Guide update

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				Date	Wednesday, January 05, 2011	Sheet 63 of 63