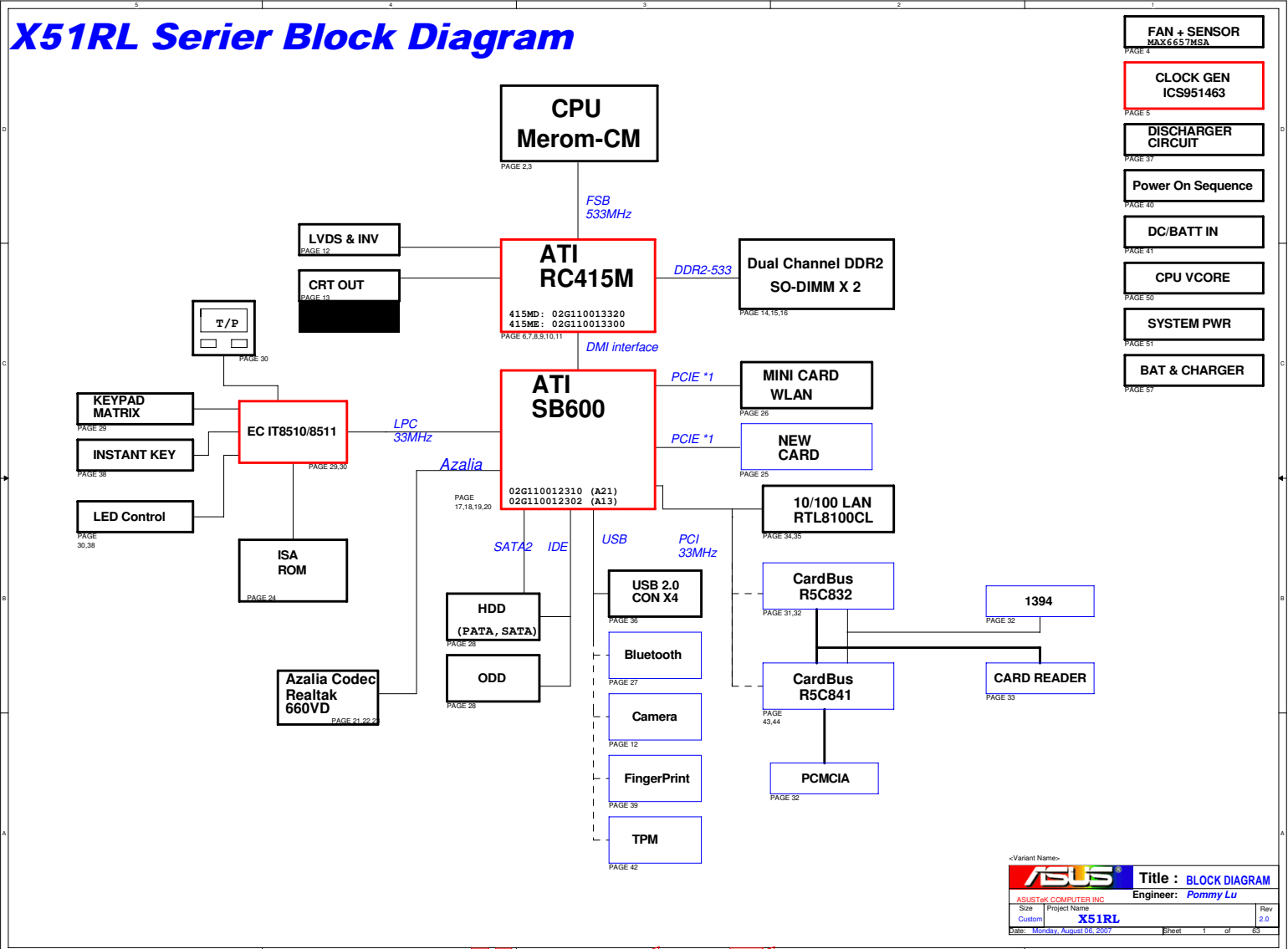


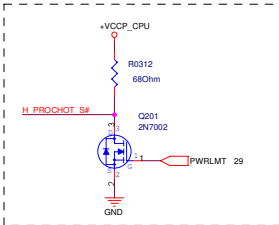
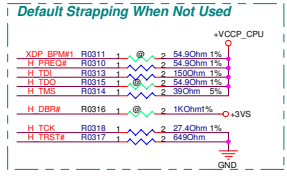
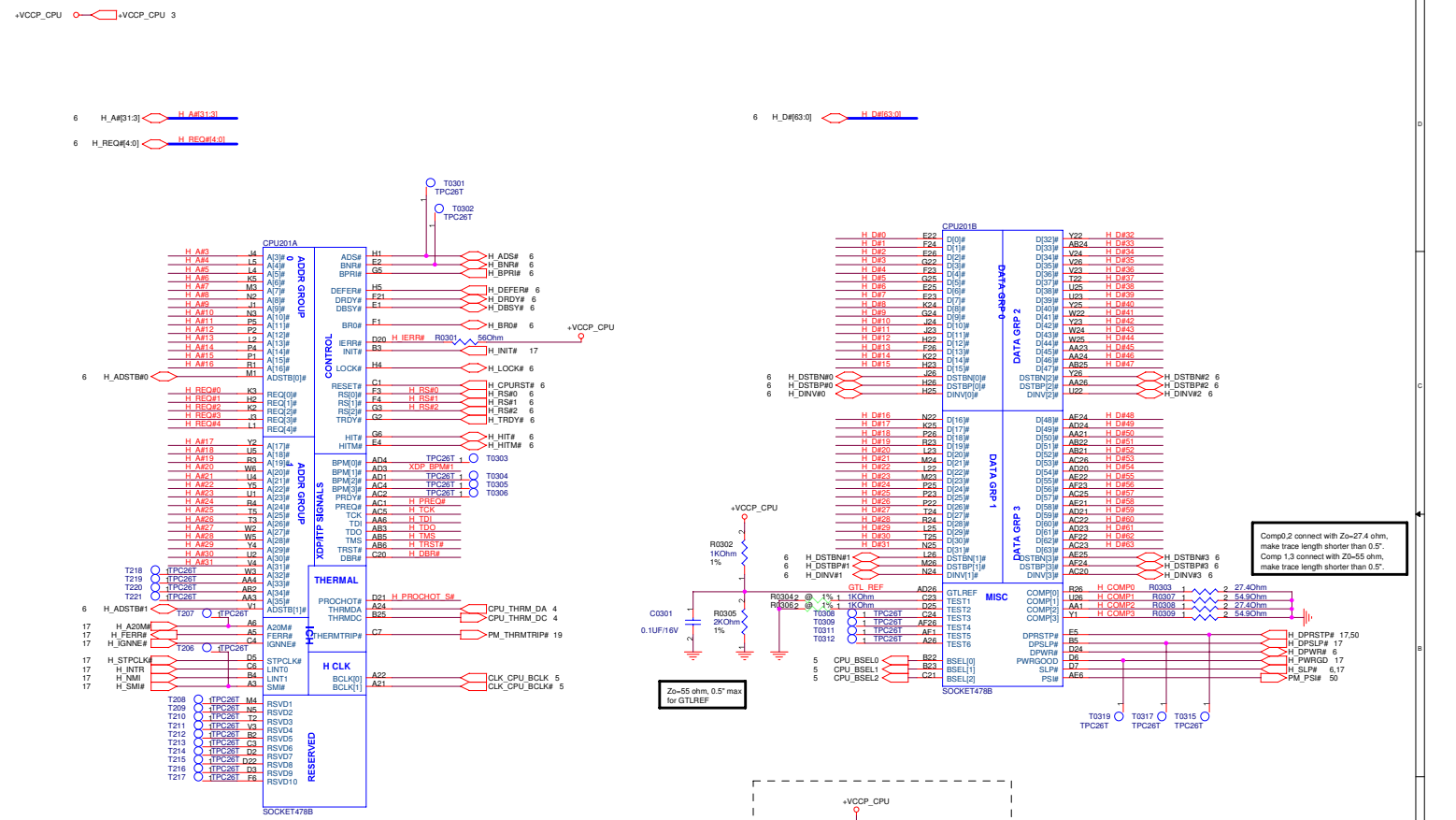
X51RL Serier Block Diagram



<Variant Name>

ASUS		Title : BLOCK DIAGRAM	
ASUSTeK COMPUTER, INC.			
Size	Project Name	Engineer:	Rev
Custom	X51RL	Pommy Lu	2.0
Date: Monday, August 06, 2007	Sheet	1	of 83

<< Kennedy_Zhang >>

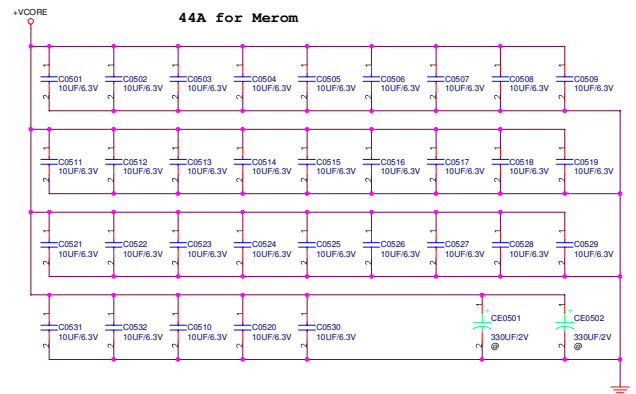
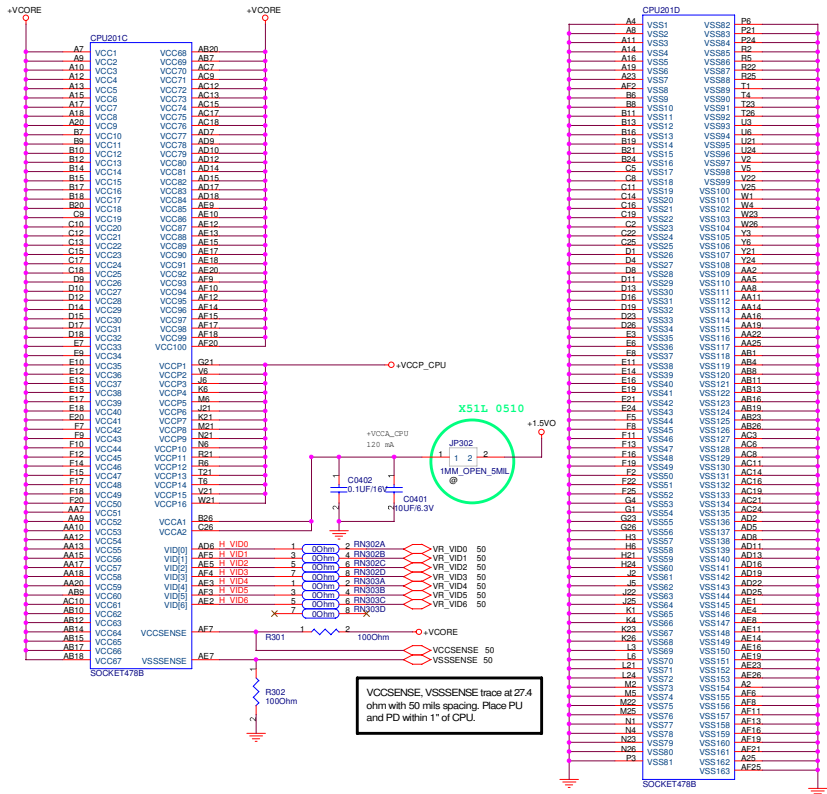
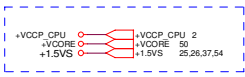


ASUS
ASUSTeK COMPUTER INC.
Project Name: X51RL
Date: Tuesday, July 03, 2007

Title : MEROM CPU (1)
Engineer: Pommy Lu

Size	Custom	Rev	2.0
Date	Tuesday, July 03, 2007	Sheet	2 of 83

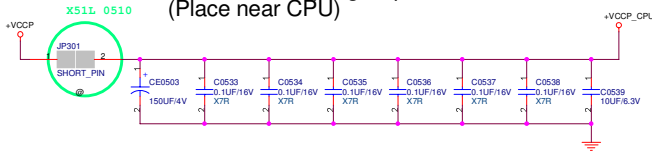
<< Kennedy_Zhang >>



Decoupling guide from INTEL

- VCCP 22uF/10V * 32pcs
- 330uF/2V * 6pcs
- VCCP 0.1uF * 6pcs for CPU
- 150uF * 1pcs for CPU

+VCCP Decoupling Capacitor (Place near CPU)



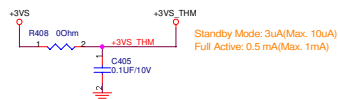
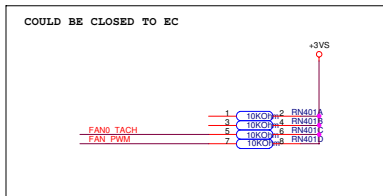
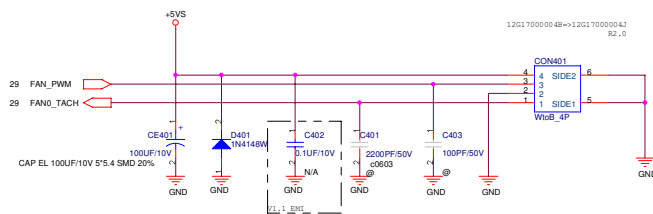
VCCSENSE, VSSSENSE traces at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.

ASUS		Title : MEROM CPU (2)
ASUSTeK COMPUTER INC		Engineer: Pommy Lu
Size	Project Name	Rev
Custom	XS1RL	2.0
Date: Tuesday, July 30, 2007	Sheet	3 of 8

<< Kennedy_Zhang >>

Fan Speed Control

KBC will issue a analog (a voltage level) signal.
 SW: FAN DA1 must be low during S3



Route H_THERMDA and H_THERMDC on the same layer

-----OTHER SIGNALS

12 mils
 =====GND

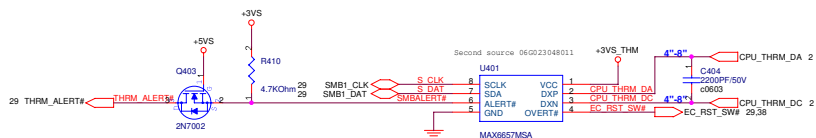
10 mils
 =====H_THERMDA(10 mils)

10 mils
 =====H_THERMDC(10 mils)

10 mils
 =====GND

12 mils
 -----OTHER SIGNALS

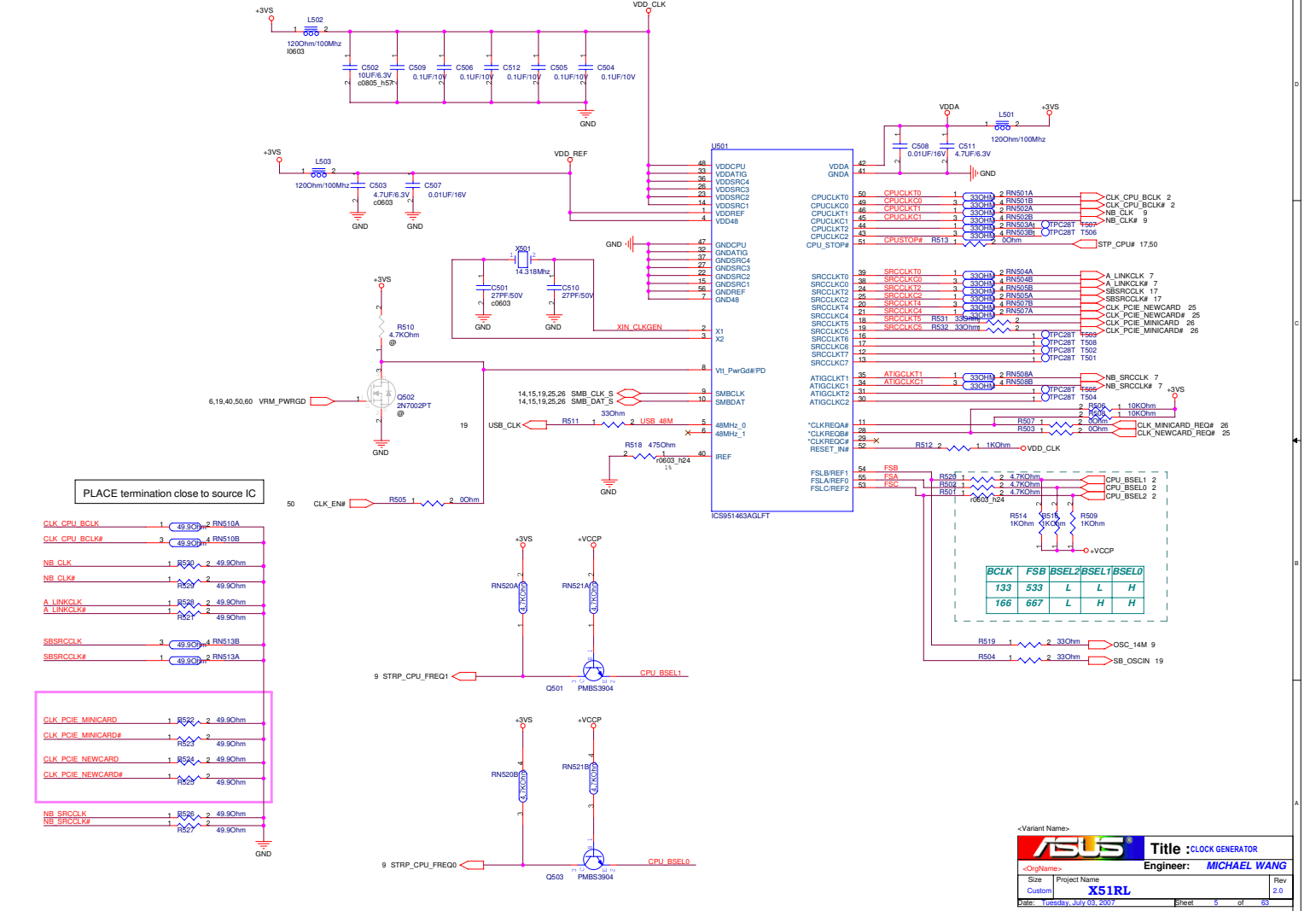
Avoid BPSB,Power



<Variant Name>

ASUS		Title : THER-SENSOR,FAN	
ASUSTek COMPUTER INC		Engineer: MICHAEL WANG	
Size	Project Name	Rev	
Custom	X51RL	2.0	
Date: Tuesday, July 03, 2007	Sheet	4	of 63

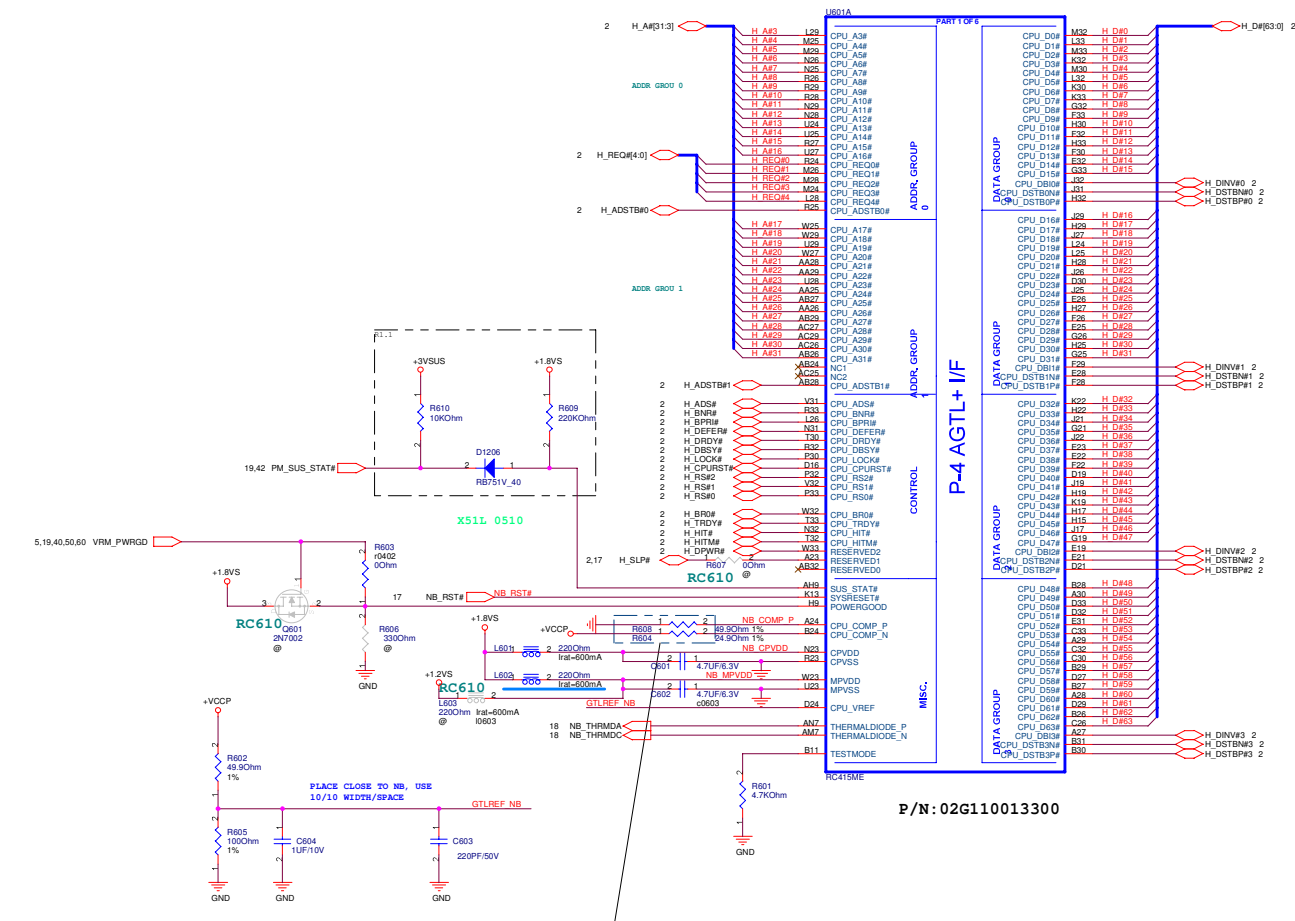
<< Kennedy_Zhang >>



ASUS Title :CLOCK GENERATOR
 Engineer: MICHAEL WANG
 Project Name: X51RL
 Date: Tuesday, July 03, 2007

<< Kennedy_Zhang >>

+1.2V/S 7.9,10,20,37,61
 +1.8V/S 5,10,37,54,91
 +VCCP 3,5,10,17,19,20,52



P/N: 02G110013300

Variant Name:

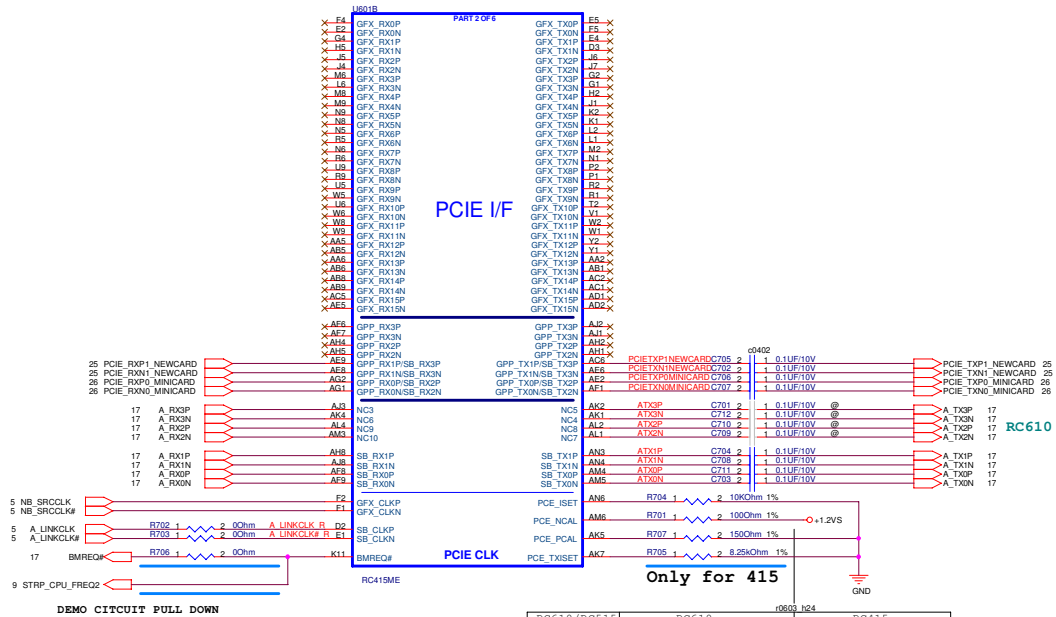
ASUS Title : NBRC415M(HOST) Engineer:

ASUSTeK COMPUTER INC. NB1

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 6 of 83

<< Kennedy_Zhang >>



Only for 415

RC610/RC515	RC610	RC415
R0704	1.47K (10G21*****)	10K (10G213100213030)
R0701	2K (10G21*****)	100 (10G213100013010)
R0707	562 (10G21*****)	150 (10G213150013030)

<Variant Name>

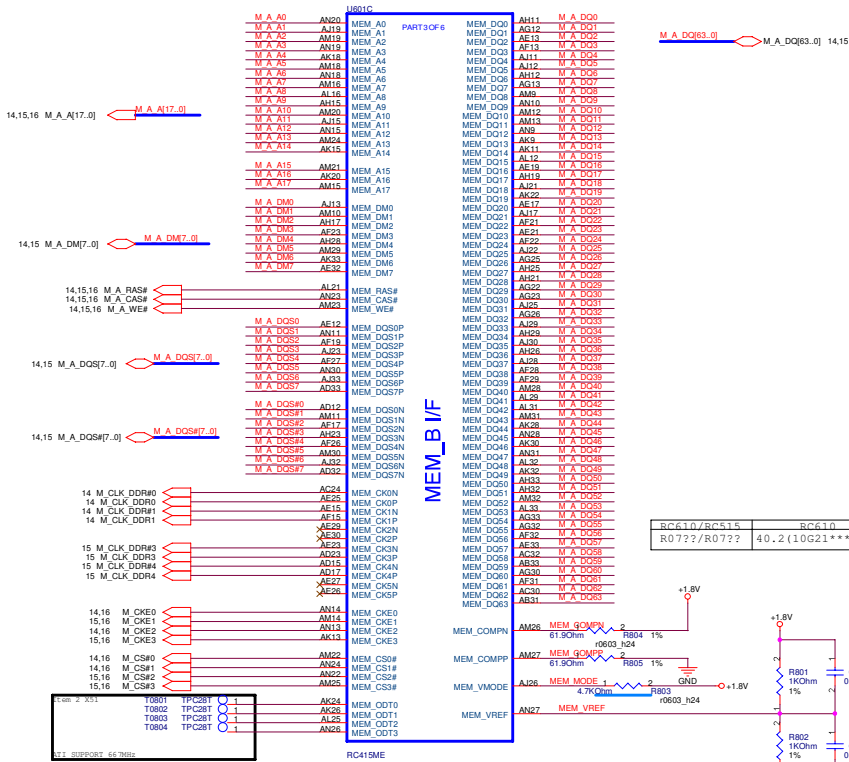
ASUS Title : NB-945PM(DMI & CFG)

ASUSTeK COMPUTER INC. NB1 Engineer: MICHAEL WANG

Size Custom Project Name **X51RL** Rev 2.0

Date: Tuesday, July 03, 2007 Sheet 7 of 83

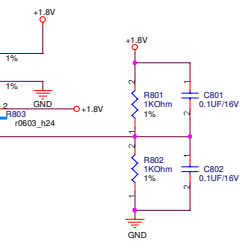
<< Kennedy_Zhang >>



mem_2_X51

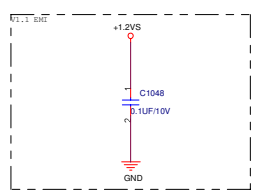
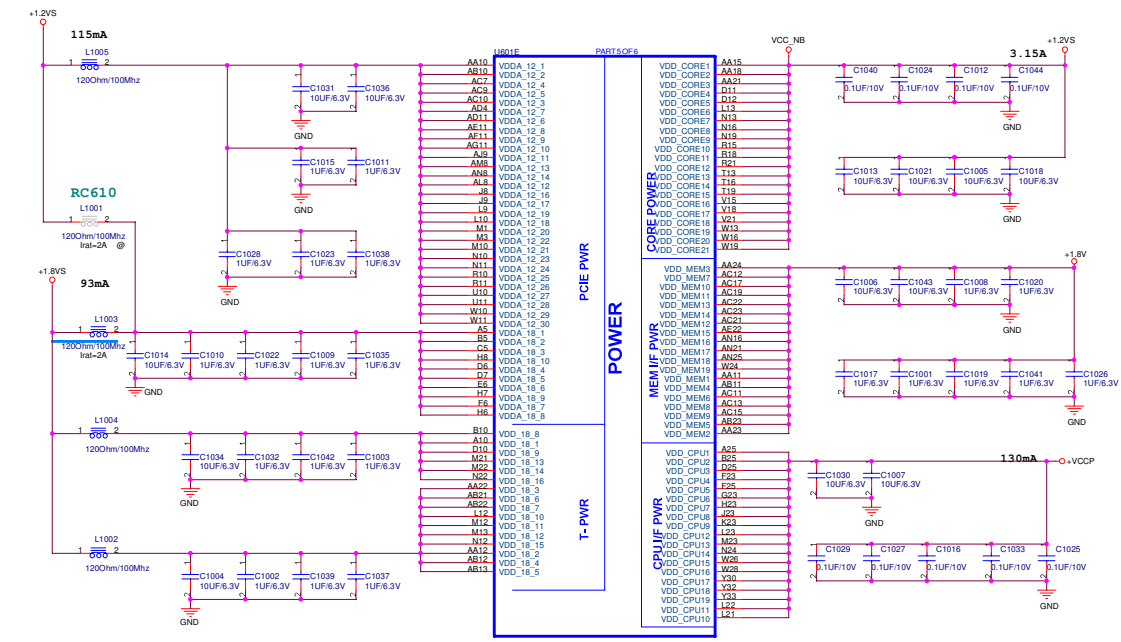
T0801	TPC28T	0	1
T0803	TPC28T	0	1
T0804	TPC28T	0	1

111 SUPPORT 457698



<< Kennedy_Zhang >>

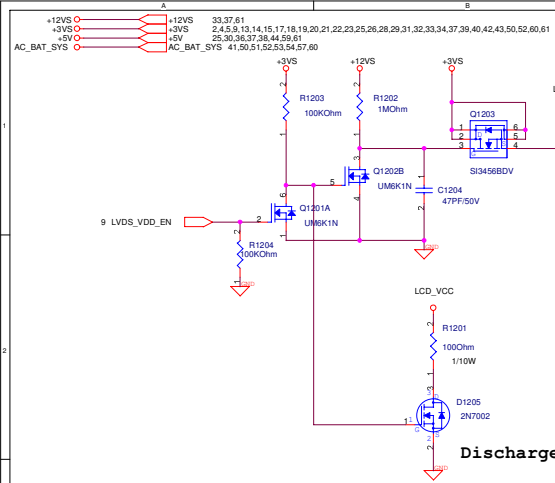
+1.2VS 6.7,9,20,37,61
+1.8VS 6,9,37,54,61
+VCCP 3,5,6,17,19,20,52



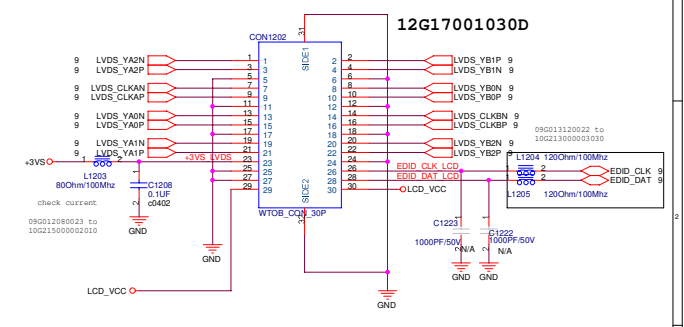
PART 6 OF 6		PART 7 OF 7	
A2	VSS2	N15	VSS75
A9	VSS7	N18	VSS76
A10	VSS8	N2	VSS77
A11	VSS9	N27	VSS78
A20	VSS14	N33	VSS79
A21	VSS15	N34	VSS80
A22	VSS16	N35	VSS81
A23	VSS17	N36	VSS82
A24	VSS18	N37	VSS83
A25	VSS19	N38	VSS84
A26	VSS20	N39	VSS85
A27	VSS21	N40	VSS86
A28	VSS22	N41	VSS87
A29	VSS23	N42	VSS88
A30	VSS24	N43	VSS89
A31	VSS25	N44	VSS90
A32	VSS26	N45	VSS91
A33	VSS27	N46	VSS92
A34	VSS28	N47	VSS93
A35	VSS29	N48	VSS94
A36	VSS30	N49	VSS95
A37	VSS31	N50	VSS96
A38	VSS32	N51	VSS97
A39	VSS33	N52	VSS98
A40	VSS34	N53	VSS99
A41	VSS35	N54	VSS100
A42	VSS36	N55	VSS101
A43	VSS37	N56	VSS102
A44	VSS38	N57	VSS103
A45	VSS39	N58	VSS104
A46	VSS40	N59	VSS105
A47	VSS41	N60	VSS106
A48	VSS42	N61	VSS107
A49	VSS43	N62	VSS108
A50	VSS44	N63	VSS109
A51	VSS45	N64	VSS110
A52	VSS46	N65	VSS111
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A55	VSS49	N68	VSS114
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A59	VSS53	N72	VSS118
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A66	VSS60	N79	VSS125
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A83	VSS77	N96	VSS142
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A91	VSS85	N104	VSS150
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A94	VSS88	N107	VSS153
A95	VSS89	N108	VSS154
A96	VSS90	N109	VSS155
A97	VSS91	N110	VSS156
A98	VSS92	N111	VSS157
A99	VSS93	N112	VSS158
A100	VSS94	N113	VSS159
A101	VSS95	N114	VSS160
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A338</			

<Variant Name>		
		Title : HISTORY
ASUSTek COMPUTER INC.		Engineer: MICHAEL WANG
Size	Project Name	Rev
Custom	X51RL	2.0
Date: Wednesday, May 16, 2007		Sheet 11 of 83

<< Kennedy_Zhang >>

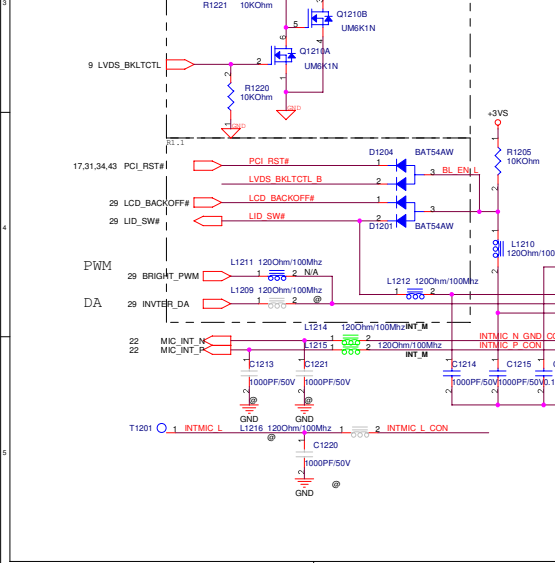


LCD LVDS Interface

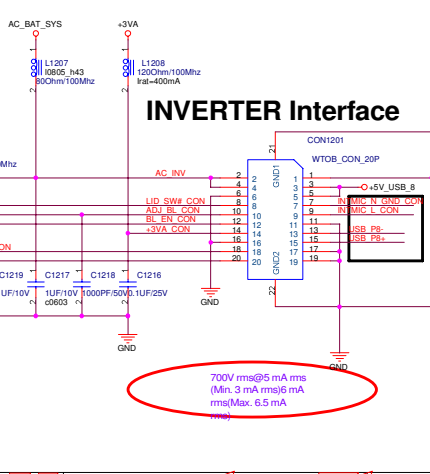


LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

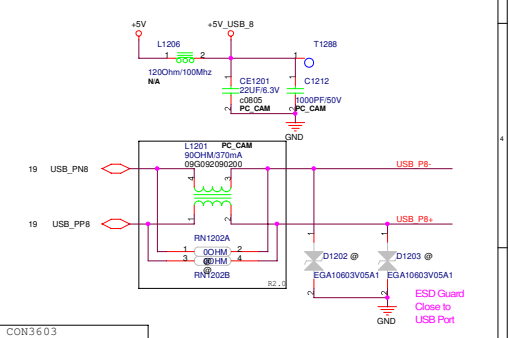


Inverter Board built in 14.1W LCD Panel



700V rms@5 mA rms
(Min. 3 mA rms)@6 mA rms(Max. 6.5 mA rms)

USB for CMOS Camera- 1W/5V



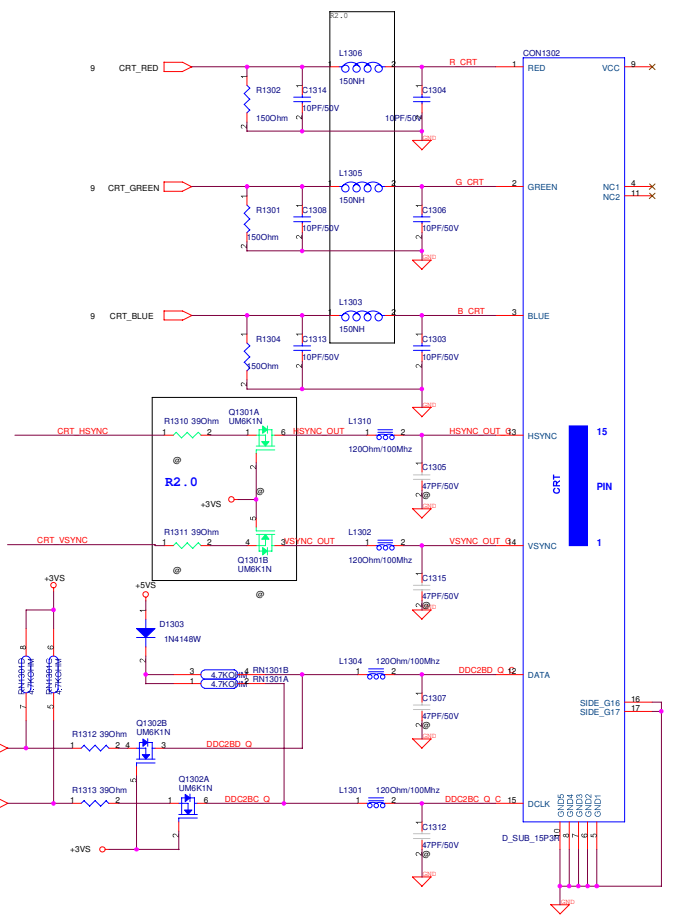
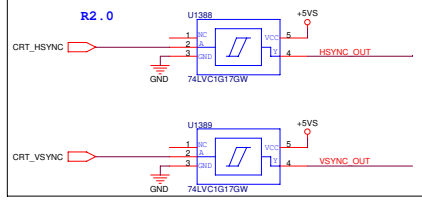
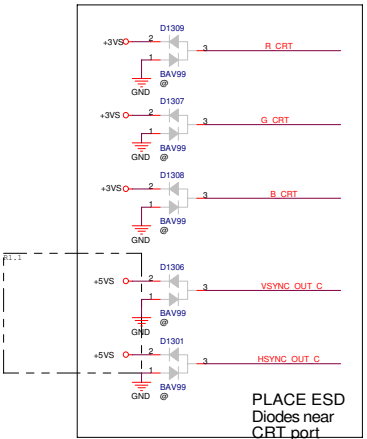
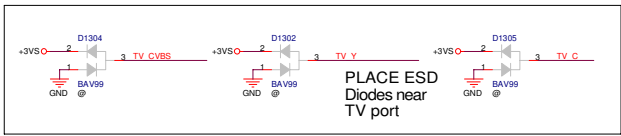
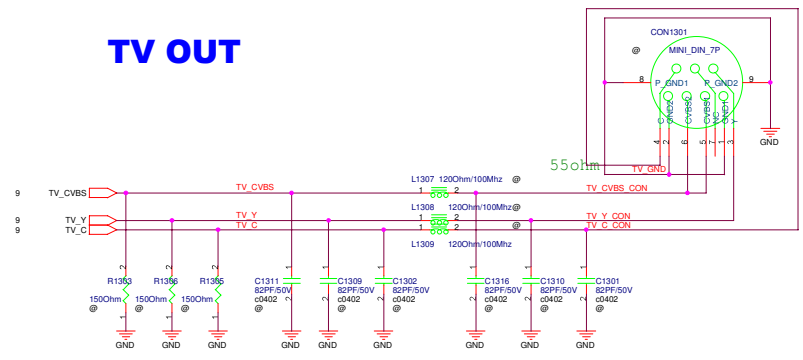
ISB_P0	CON3603
ISB_P1	
ISB_P2	BT
ISB_P3	NEW_CARD
ISB_P4	CON3601
ISB_P5	CON3601
ISB_P6	CON3602
ISB_P7	
ISB_P8	PC_CAM
ISB_P9	FINGER

ASUS		Project Name	X51RL
ASUSTeK COMPUTER INC.		Engineer:	MICHAEL WANG
Size	Custom	Title :	LCD CON
Date:	Tuesday, July 03, 2007	Sheet	12 of 89

<< Kennedy_Zhang >>

12G141011076

TV OUT



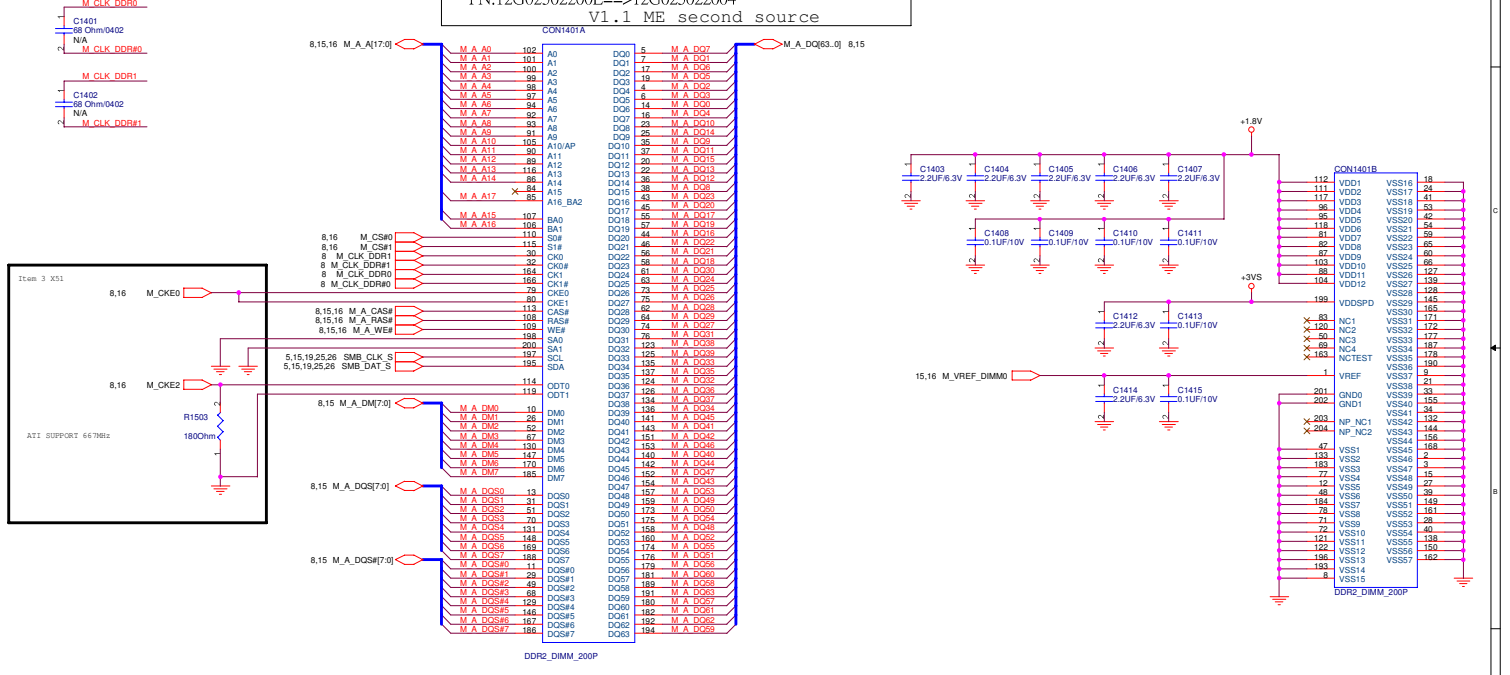
<Variant Name>

ASUS		Project Name	X51RL
ASUSTek COMPUTER INC.		Engineer:	MICHAEL WANG
Size	Custom	Title :	CRT PORT
Date:	Tuesday, July 03, 2007	Rev	2.0
		Sheet	19 of 69

<< Kennedy_Zhang >>

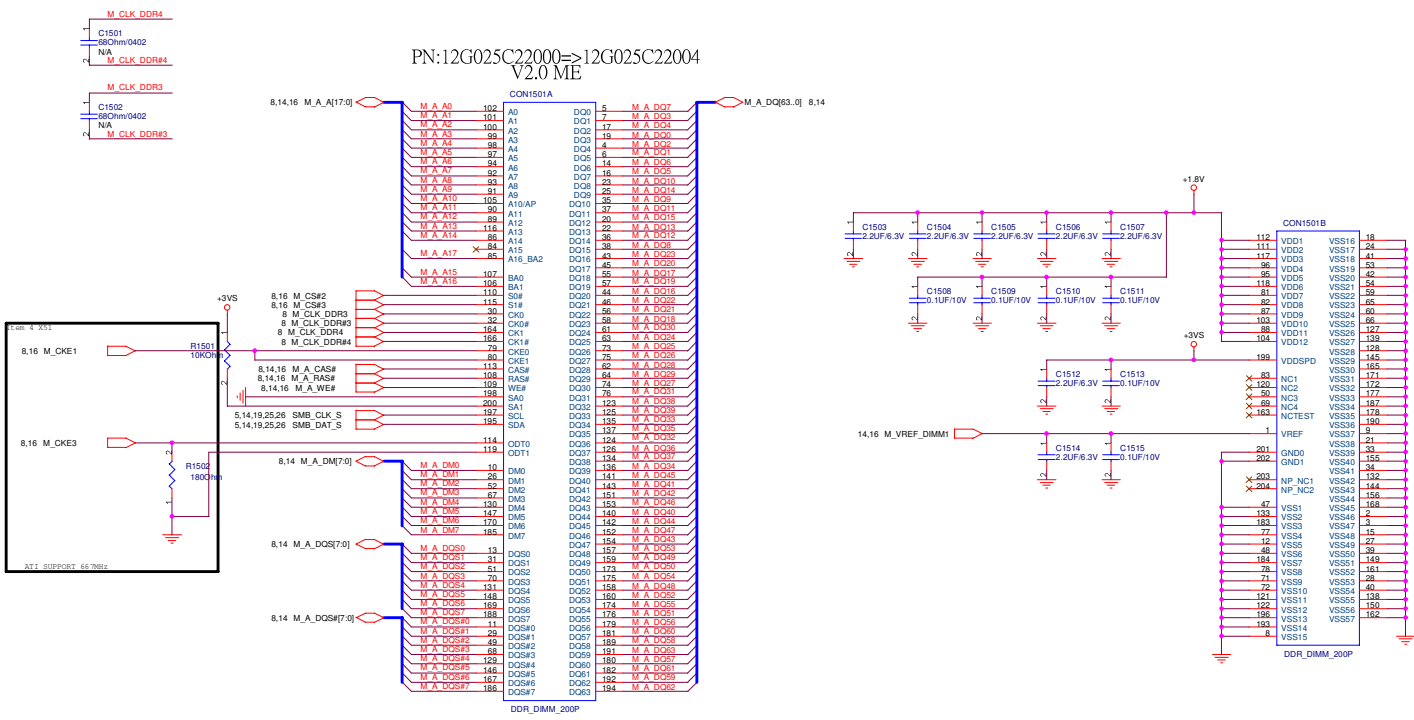
FRON

PN:12G02502200E=>12G025022004
V1.1 ME second source



ASUS Title : DDR2 SO-DIMM
 ASUSTeK COMPUTER INC. NBI Engineer: MICHAEL WANG
 Size Project Name
 Custom X51RL
 Date: Tuesday, July 03, 2007 Sheet 14 of 89

<< Kennedy_Zhang >>

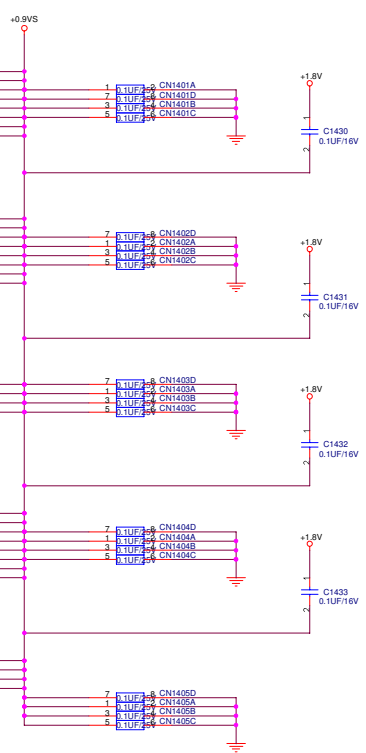
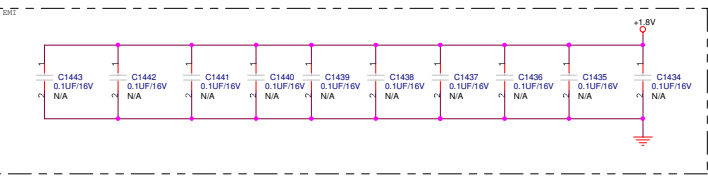
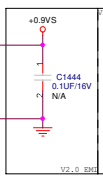
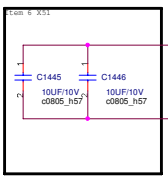
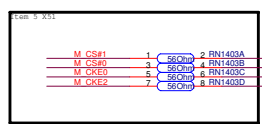
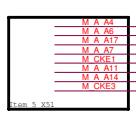
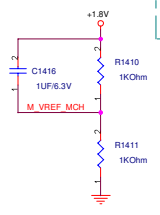
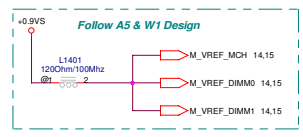


<Variant Names>
ASUS Title: **DDR2 SO-DIMM1**
 ASUSTeK COMPUTER INC. NB1 Engineer: **MICHAEL WANG**
 Size Project Name **X51RL**
 Date: Tuesday, July 03, 2007 Sheet 15 of 89

<< Kennedy_Zhang >>

+0.9VS 37.53

8.14.15 M_A_[17:0]



<Variant Name>

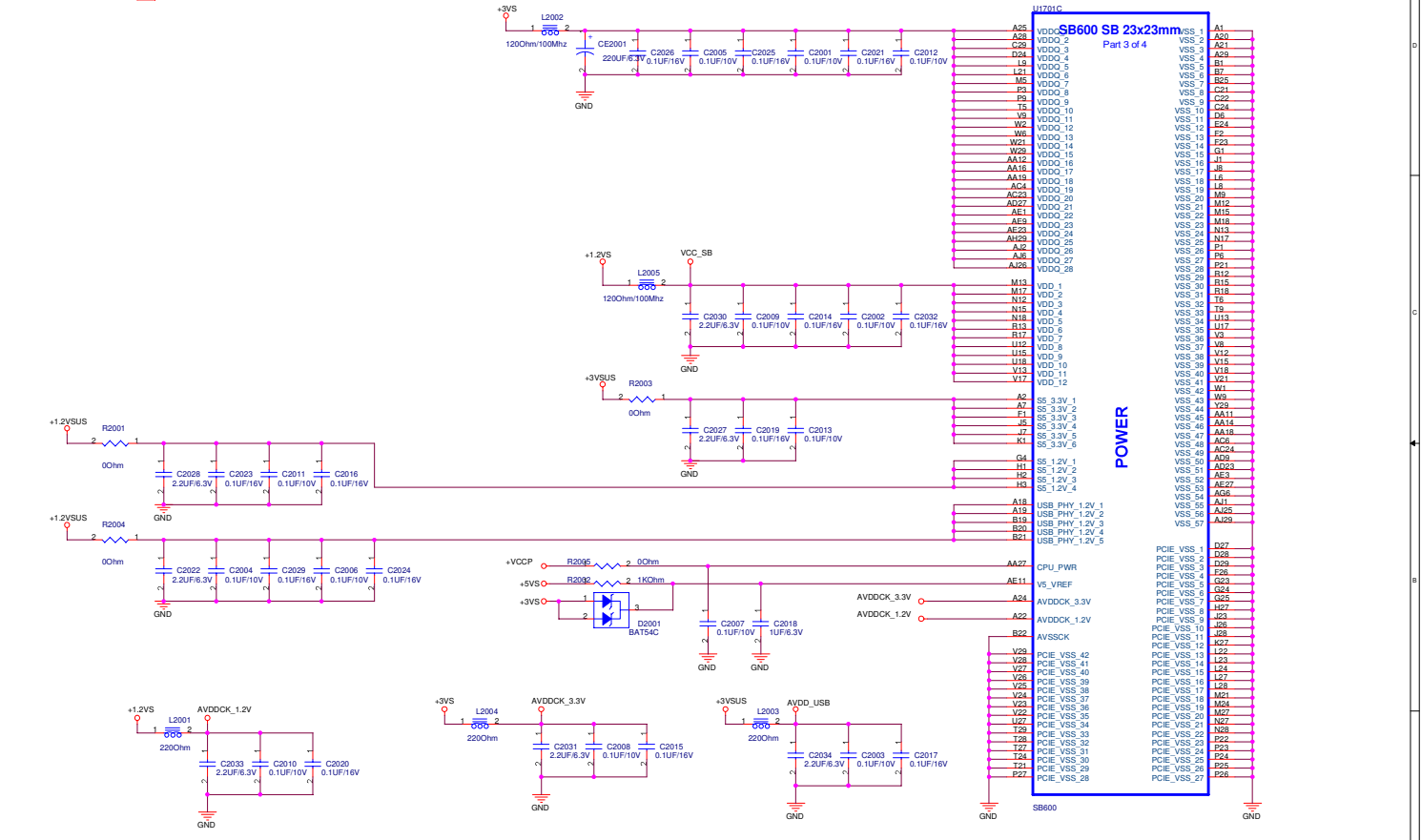
ASUS Title : **DDR2 TERMINATION**

ASUSTeK COMPUTER INC. NB1 Engineer : **MICHAEL WANG**

Size	Project Name	Rev
Custom	X51RL	2.0
Date: Tuesday, July 03, 2007	Sheet	16 of 89

<< Kennedy_Zhang >>

+3VSUS 6,17,19,23,25,29,34,40,51
 +3VS 2,4,5,9,12,13,14,15,17,18,19,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
 +VCP C
 AVDD_USB 19
 VCC_SB 17,18
 +1,2VSUS 82
 +5VS 4,13,22,23,28,29,30,37,38,50,61



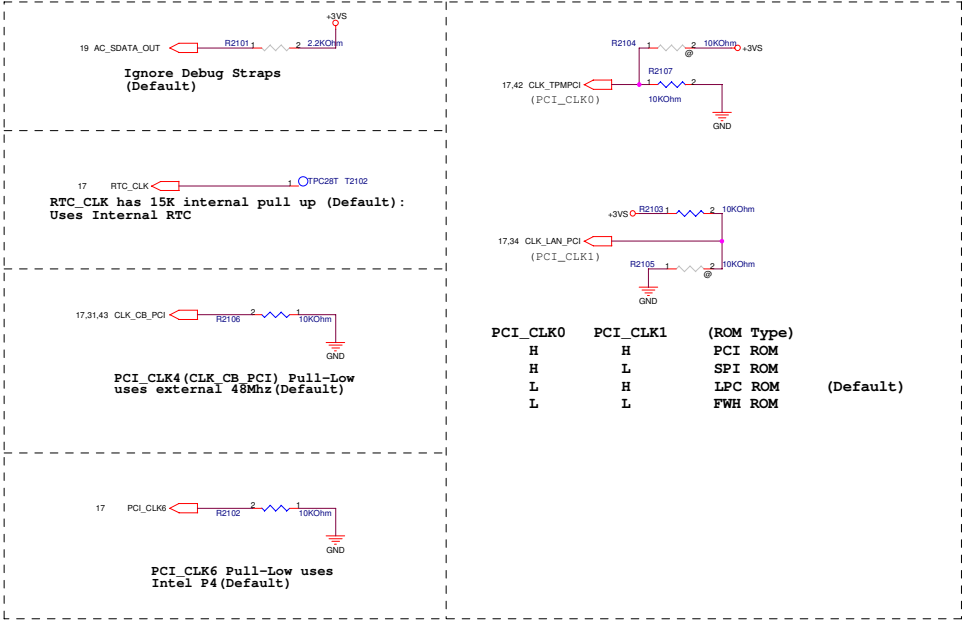
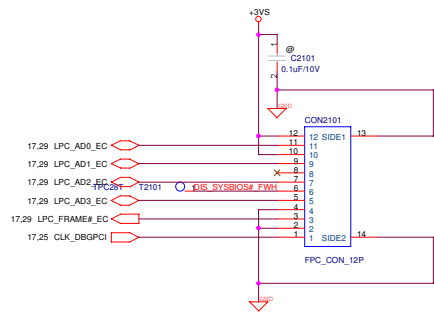
<Variant Name>

ASUS Title : SB-ICH7M(PWR)
 ASUSTeK COMPUTER INC. NBI Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 20 of 83

<< Kennedy_Zhang >>



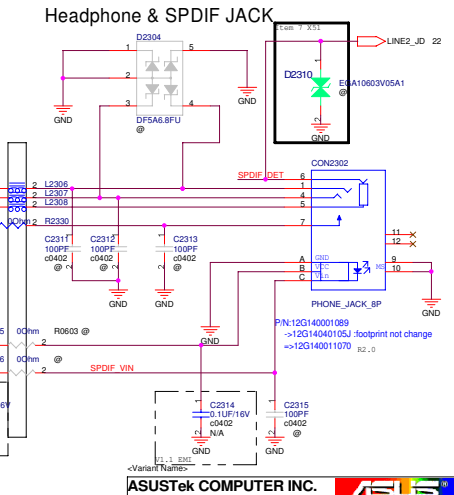
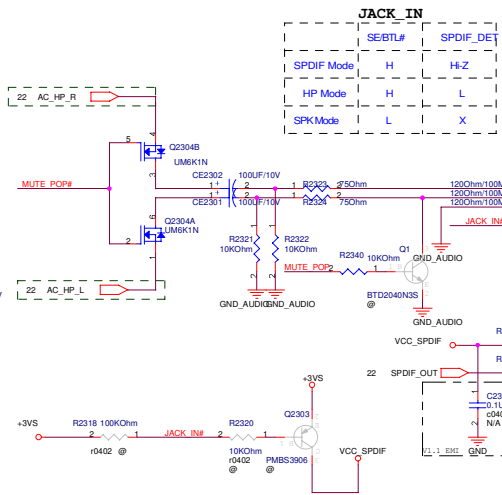
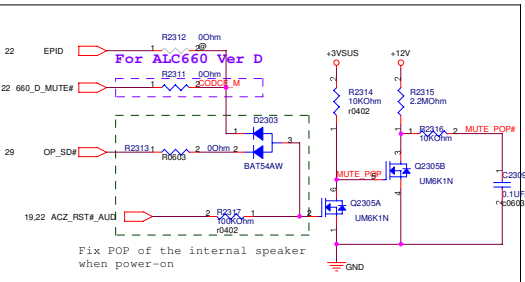
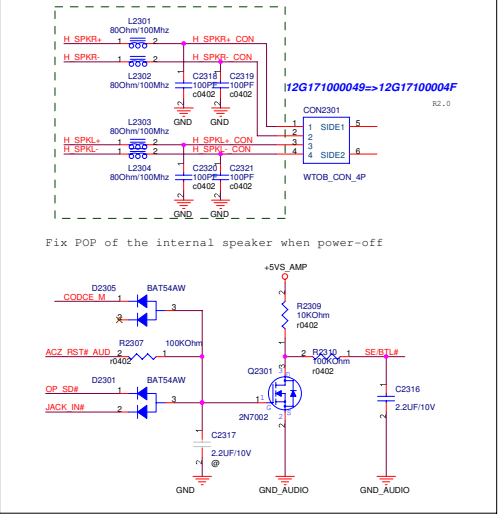
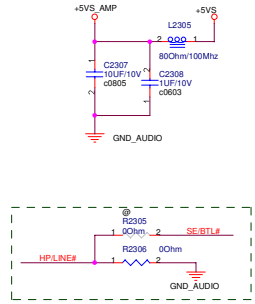
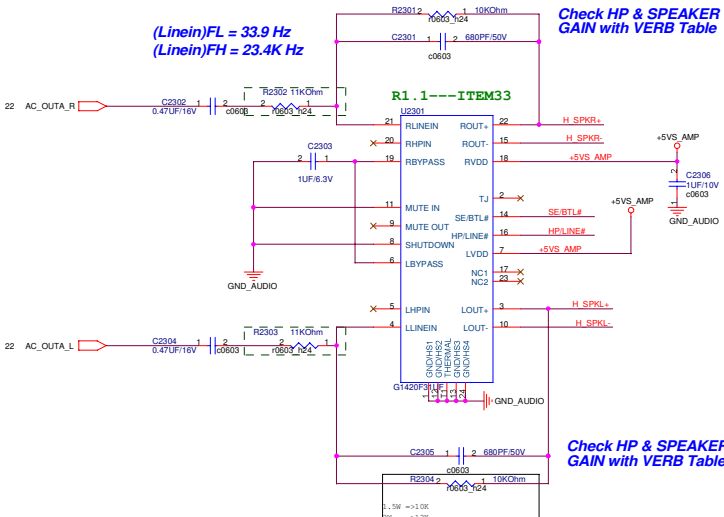
<Variant Name>

ASUS Title : **BLOCK DIAGRAM**

Engineer:

Size	Project Name	Rev
Custom	X51RL	2.0
Date: Tuesday, July 03, 2007	Sheet	21 of 89

<< Kennedy_Zhang >>



DIGITAL AREA

+3VS	0	2,4,5,9,12,13,14,15,17,18,19,20,21,22,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
+5VS	0	4,13,26,22,28,29,30,37,38,50,61
+5V_AUDIO	0	22
+3VSUS	0	6,17,19,20,25,29,34,40,51
+12V	0	36,37,54,61

ASUSTek COMPUTER INC. MICHAEL WAN@Ta Hsi-Paiou, Taipei, Taiwan, ROC

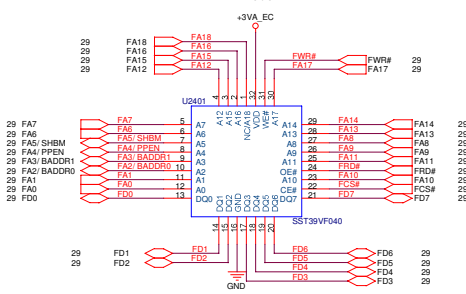
Audio AMP

File: X51RL
 Size: Document Number: X51RL
 Date: Tuesday, July 03, 2007
 Sheet: 23 of 83

<< Kennedy_Zhang >>

+3VA_EC @ +3VA_EC 26,29

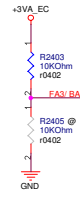
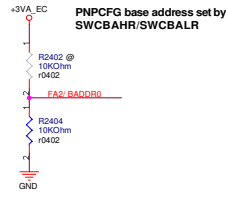
ISA ROM



EC Hardware Strap

Strap value sampled after VSTBY power up reset

PNPCFG base address set by SWCBAHR/SWCBALR



BADDR[1:0]

No pull up:
Ext 10K up on BADDR0:
Ext 10K up on BADDR1:

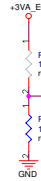
The register pair to access PNPCFG is 002Eh and 002Fh.
The register pair to access PNPCFG is 004Eh and 004Fh.
The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

Share Memory



SHBM

No pull up: Disable shared memory with host BIOS
Ext 10K up: Enable shared memory with host BIOS



PPEN

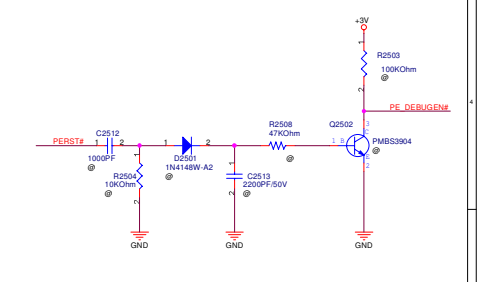
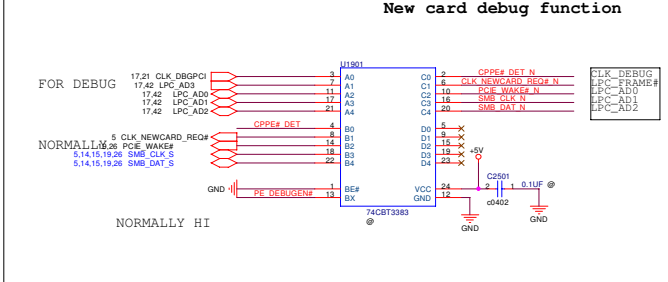
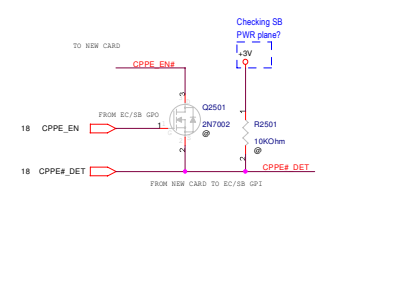
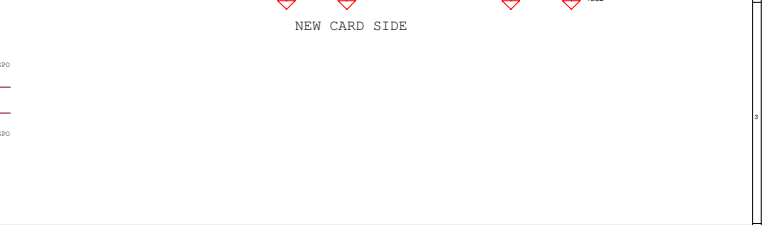
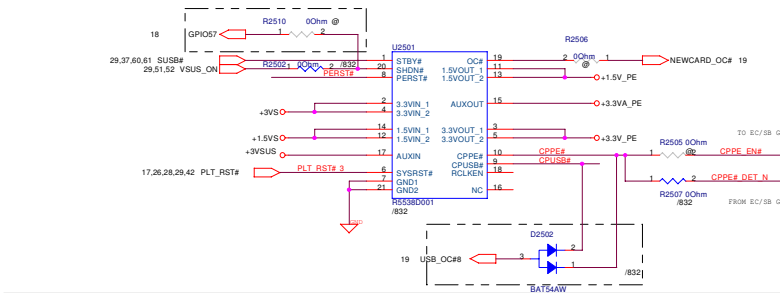
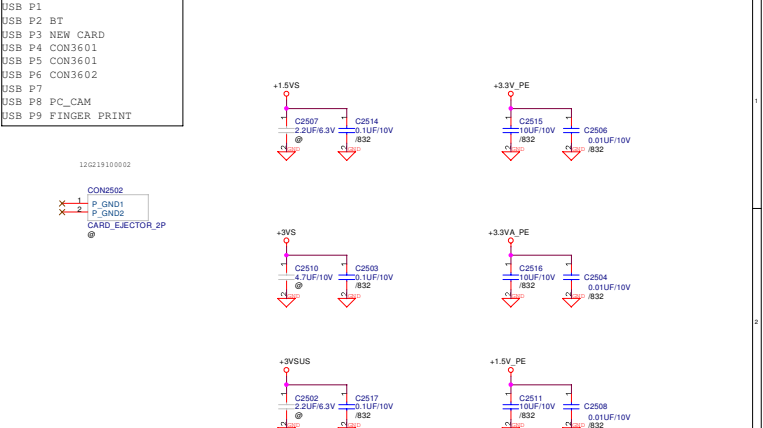
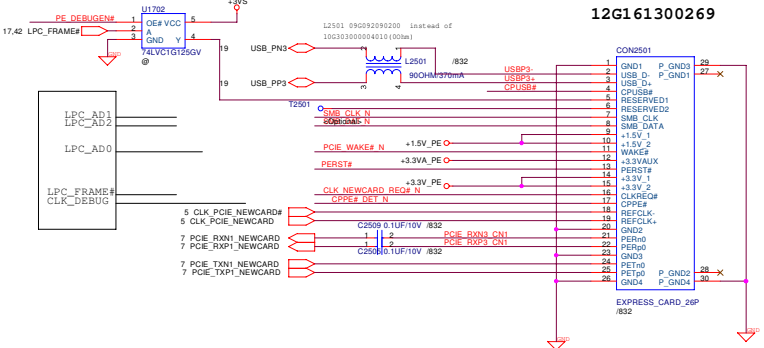
No pull up: Normal
Ext 10K up: KBS interface pins are switched to parallel port interface for in-system programming.



<Variant Name>

ASUS		Title : ISA ROM	
ASUSTeK COMPUTER INC.		Engineer: MICHAEL WANG	
Size	Project Name	Rev	
Custom	X51RL	2.0	
Date	Tuesday, July 03, 2007	Sheet	24 of 63

<< Kennedy_Zhang >>



Reserve to remove PCIE debug function

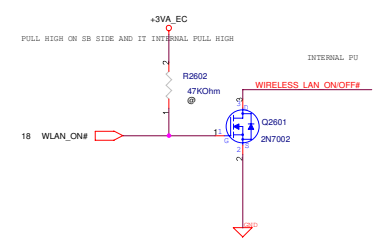
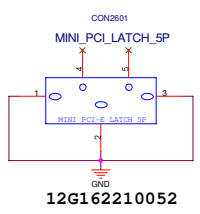
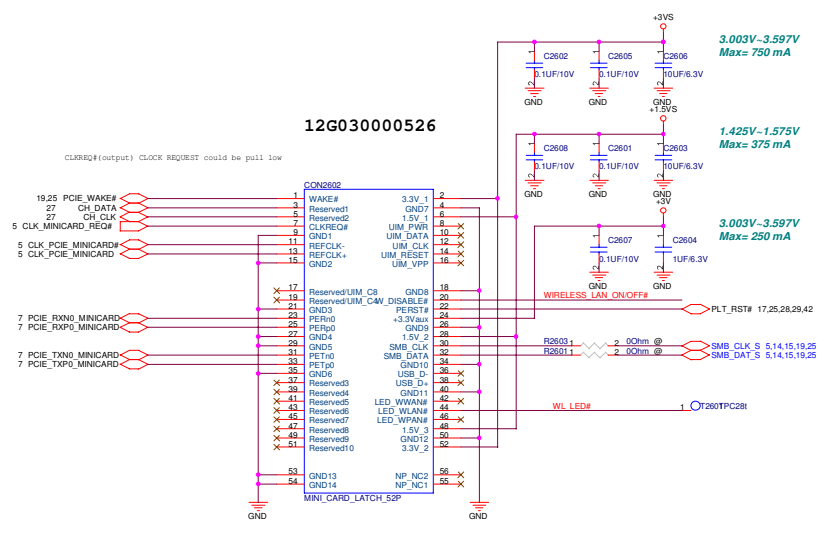
CLK_NEWCARD_REQ#	0Ohm	2	RN1901A	CLK_NEWCARD_REQ# N
P2E_WAKE#	0Ohm	4	RN1901B_NA	P2E_WAKE# N
SMB_CLK_S	0Ohm	1	RN1902A_NA	SMB_CLK_N
SMB_DAT_S	0Ohm	4	RN1902B_NA	SMB_DAT_N
				NA

ASUS Project Name: **X51RL**
 ASUSTek COMPUTER INC. Engineer: **MICHAEL WANG**
 Title: **New Card**
 Date: Tuesday, July 03, 2007 Sheet 25 of 83

<< Kennedy_Zhang >>

+3V O 17,25,27,31,35,37,42,43,44,61
 +3VS O 2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
 +1.5VS O 1,1.5VS 25,37,54
 +3VA_EG O +3VA_EG 24,29

12G030000526

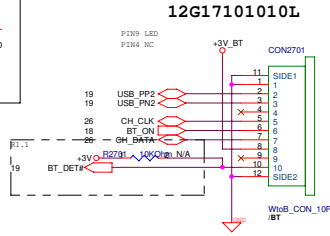
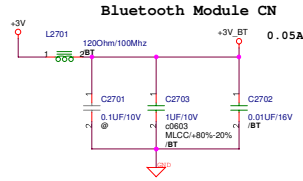
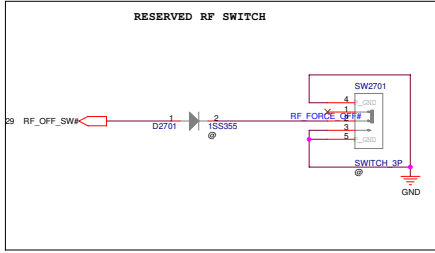


<Variant Name>

ASUS		Project Name	XS1RL
ASUSTek COMPUTER INC.		Engineer:	MICHAEL WANG
Size	Custom	Title :	MINI PCI
Date:	Tuesday, July 03, 2007	Sheet	26 of 63

<< Kennedy_Zhang >>

For Bluetooth



- USB P0 CON3603
 - USB P1
 - USB P2 BT
 - USB P3 NEW CARD
 - USB P4 CON3601
 - USB P5 CON3601
 - USB P6 CON3602
 - USB P7
 - USB P8 PC_CAM
 - USB P9 FINGER
- PRINT

<Variant Names>

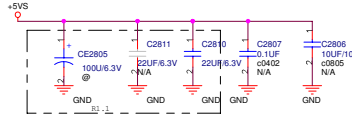
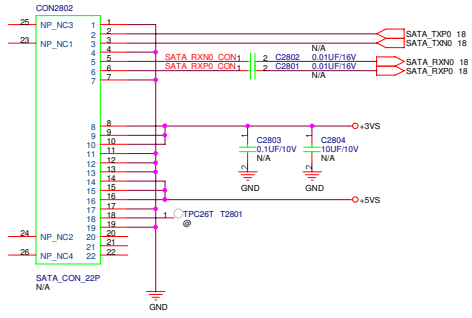
ASUS		Title : Blue Tooth
ASUSTeK COMPUTER INC		Engineer: MICHAEL WANG
Size	Project Name	Rev
Custom	X51RL	2.0
Date: Tuesday, July 03, 2007	Sheet	27 of 83

<< Kennedy_Zhang >>

SATA HDD

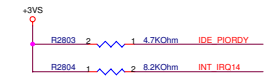
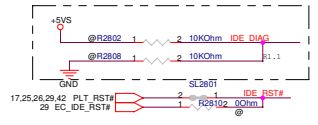
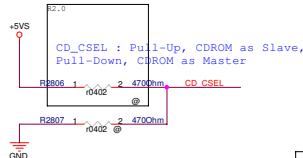
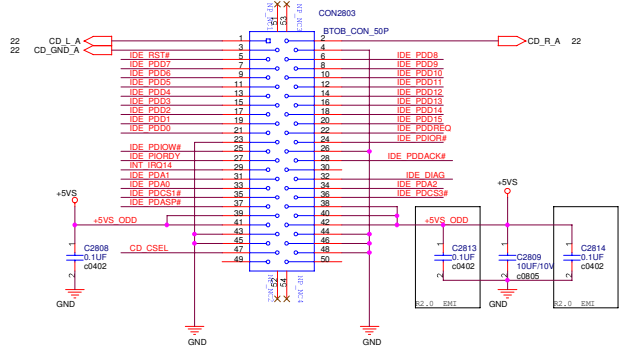
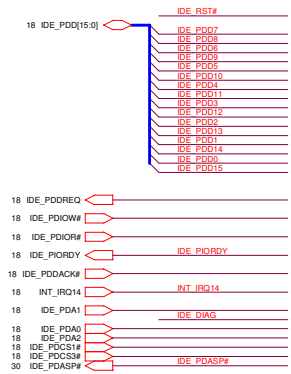


12G15100022F



CD-ROM

12G161210504



ASUS Logo

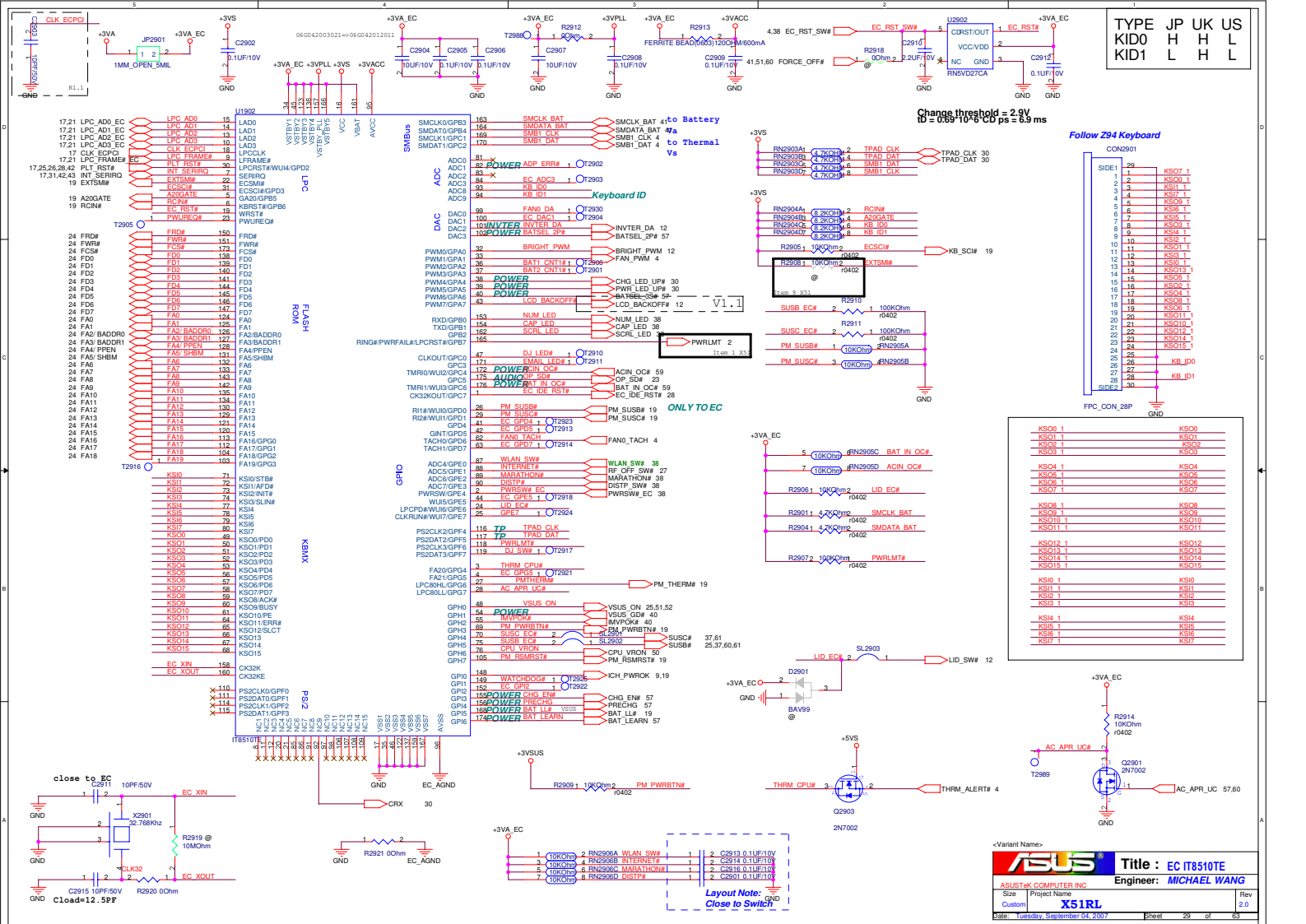
Title : PATA-SATA & ODD

ASUSTeK COMPUTER INC. NB1 **Engineer:**

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Monday, August 06, 2007 Sheet 29 of 89

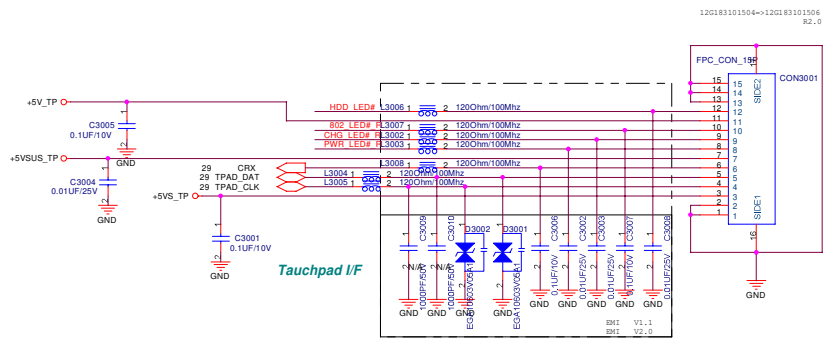
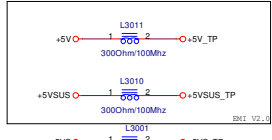
<< Kennedy_Zhang >>



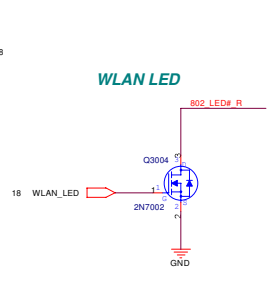
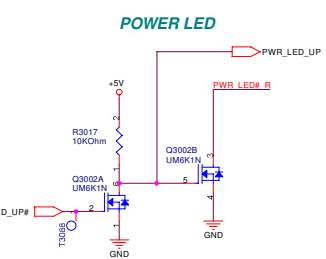
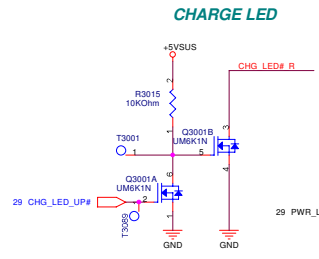
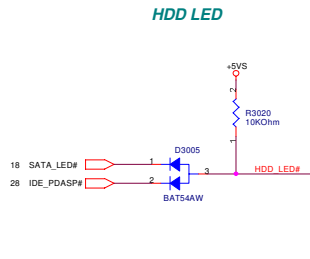
<Variant Name>

ASUS Title: EC IT8510TE
ASUSTek COMPUTER INC. Engineer: MICHAEL WANG
Size: Project Name: X51RL Rev: 2.0
Custom: X51RL
Date: Tuesday, September 04, 2007 Sheet: 29 of 83

<< Kennedy_Zhang >>



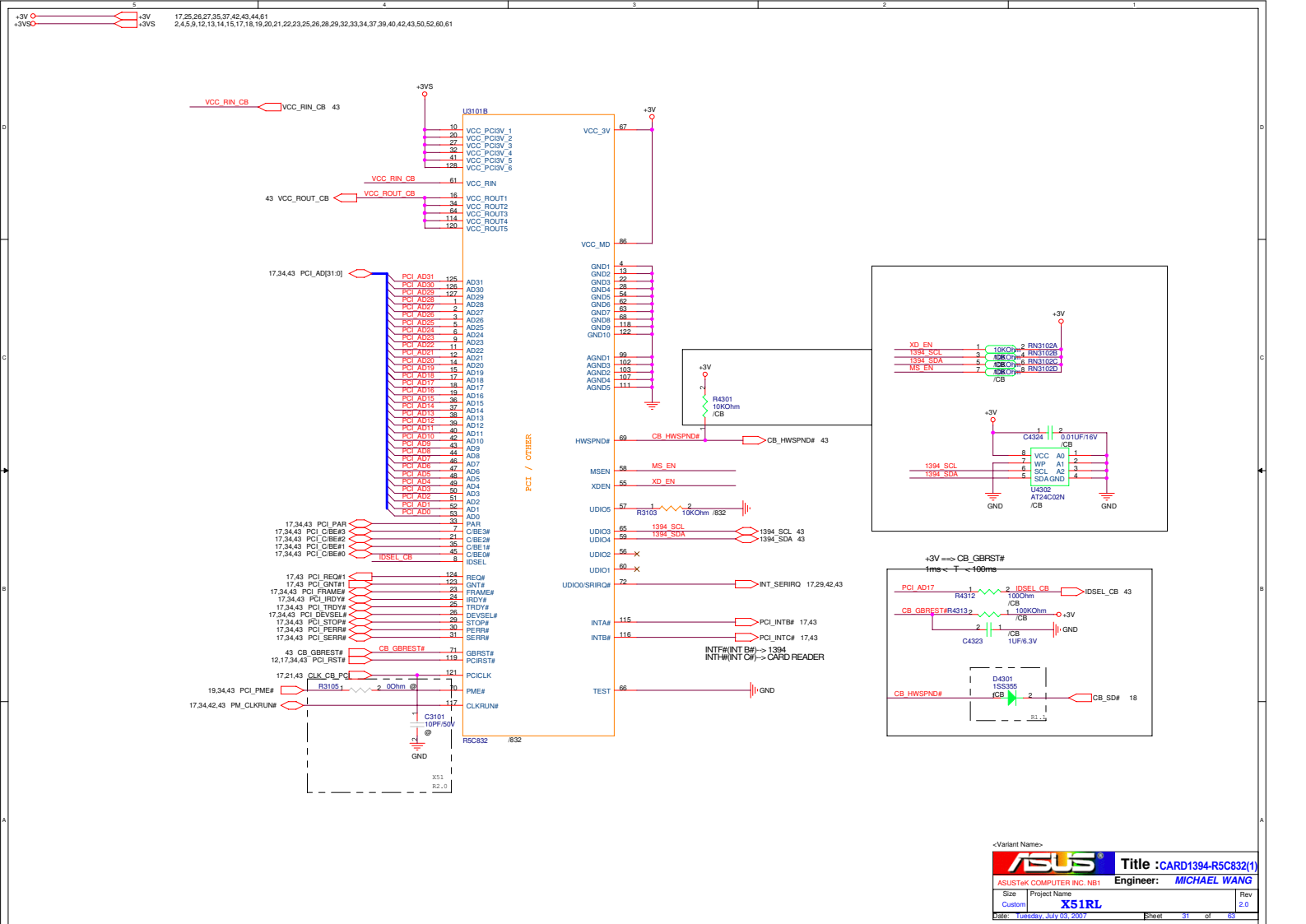
Touchpad



<-Variant Name:->

ASUS		Title : EC IT8510TE(2/2)
ASUSTeK COMPUTER INC		Engineer: MICHAEL WANG
Size	Project Name	Rev
A3	X51RL	2.0
Date: Tuesday, July 03, 2007	Sheet	30 of 63

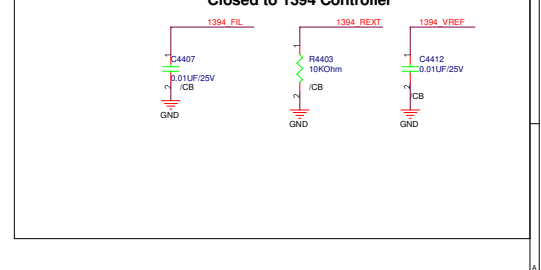
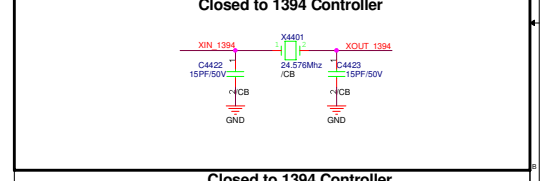
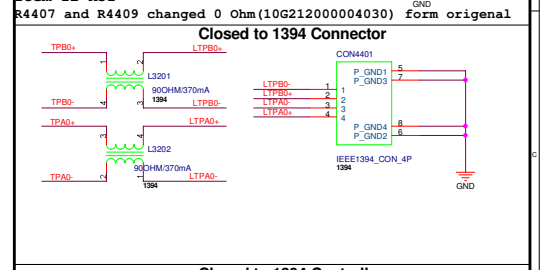
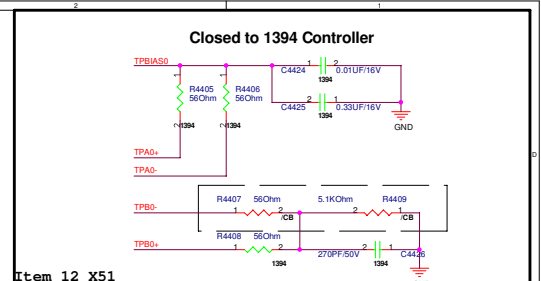
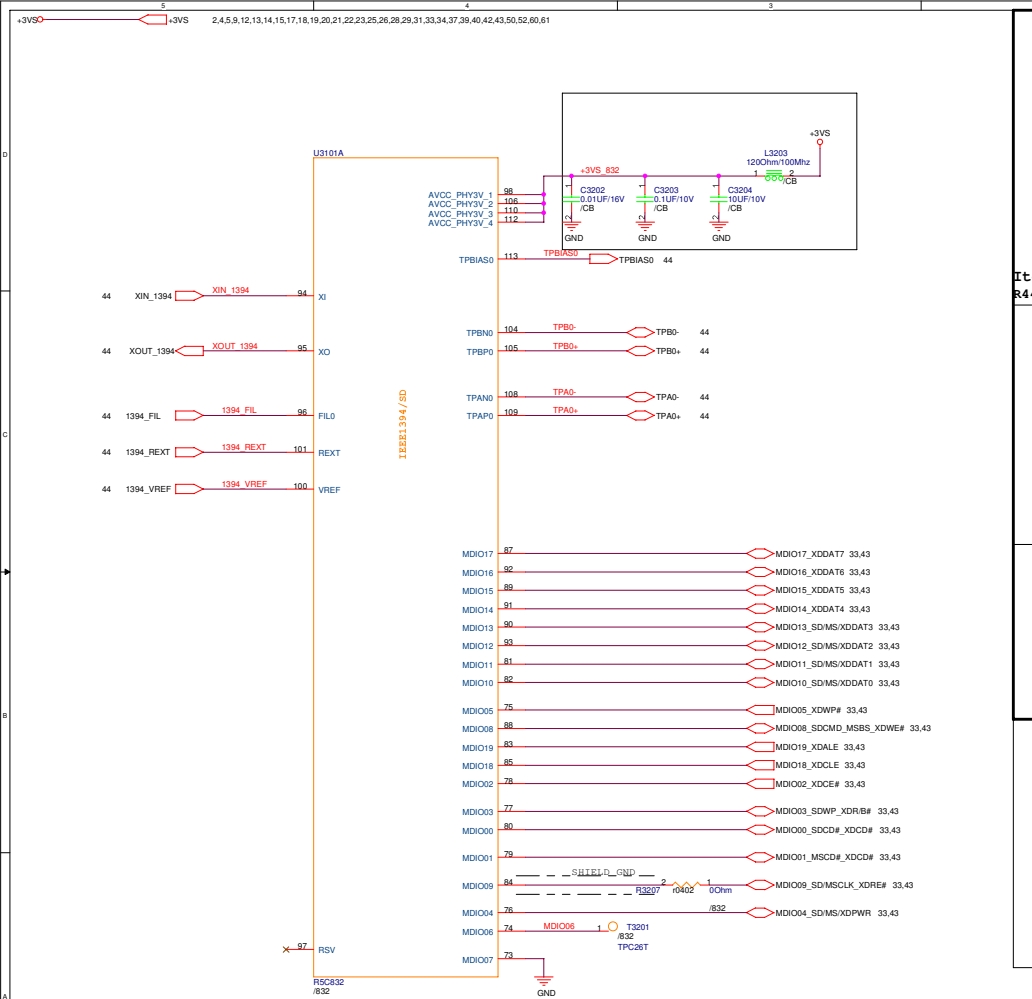
<< Kennedy_Zhang >>



<Variant Name>

ASUS		Title :CARD1394-R5C832(1)
ASUSTeK COMPUTER INC. NB1		Engineer: MICHAEL WANG
Size	Project Name	Rev
Custom	X51RL	2.0
Date: Tuesday, July 03, 2007	Sheet	81 of 89

<< Kennedy_Zhang >>



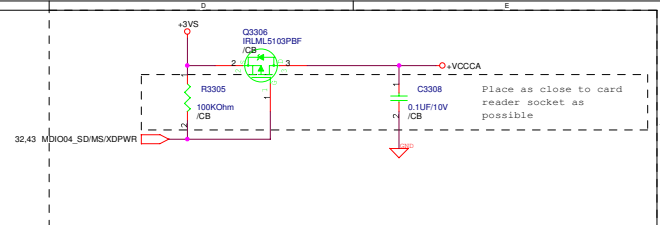
<Variant Name>

ASUS		Title : CARD1394-R5C832(2)	
ASUSTeK COMPUTER INC. NB1		Engineer: MICHAEL WANG	
Size	Project Name	Rev	
Custom	X51RL	2.0	
Date: Tuesday, July 03, 2007	Sheet	89	of 89

<< Kennedy_Zhang >>

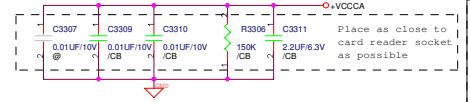
Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU

MDIO00-->	SD Card Detect
MDIO01-->	MS Card Detect
MDIO03-->	SD Write Protect
MDIO04-->	SD Card Power0 Control/MS Power Control
MDIO08-->	SD Command/MS Bus State
MDIO09-->	SD Clock/MS Clock
MDIO10-->	SD Data 0/MS Data 0
MDIO11-->	SD Data 1/MS Data 1
MDIO12-->	SD Data 2/MS Data 2
MDIO13-->	SD Data 3/MS Data 3

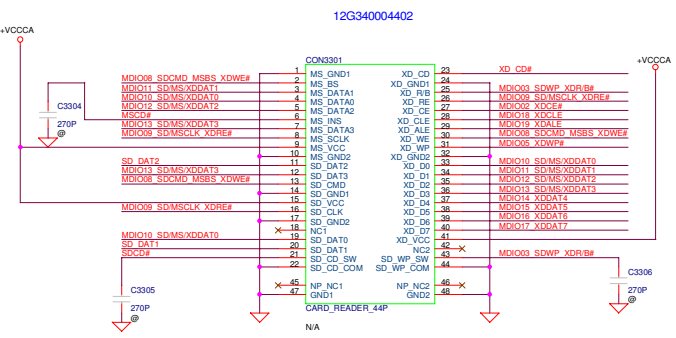
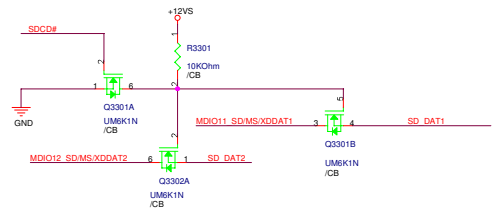


SD/MMC/MS/MS-PRO Card Reader Socket

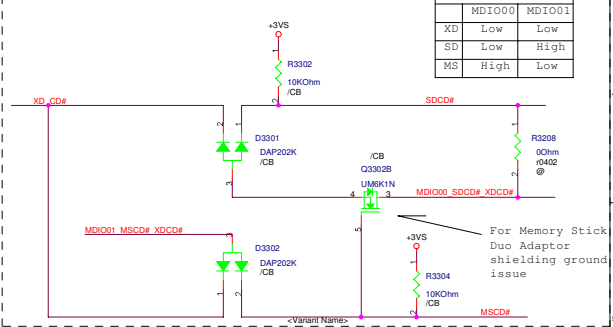
- 32.43 MDIO17_XDDAT7 <--> MDIO17_XDDAT7
- 32.43 MDIO16_XDDAT6 <--> MDIO16_XDDAT6
- 32.43 MDIO15_XDDAT5 <--> MDIO15_XDDAT5
- 32.43 MDIO14_XDDAT4 <--> MDIO14_XDDAT4
- 32.43 MDIO13_SDM/SDWP# <--> MDIO13_SDM/SDWP#
- 32.43 MDIO12_SDM/SDWP# <--> MDIO12_SDM/SDWP#
- 32.43 MDIO11_SDM/SDWP# <--> MDIO11_SDM/SDWP#
- 32.43 MDIO10_SDM/SDWP# <--> MDIO10_SDM/SDWP#
- 32.43 MDIO09_SDM/SDWP# <--> MDIO09_SDM/SDWP#
- 32.43 MDIO08_SDCMD_MSSB_XDWE# <--> MDIO08_SDCMD_MSSB_XDWE#
- 32.43 MDIO07_XDALE <--> MDIO07_XDALE
- 32.43 MDIO06_XDCLE <--> MDIO06_XDCLE
- 32.43 MDIO05_XDCE# <--> MDIO05_XDCE#
- 32.43 MDIO03_SDWP_XDRB# <--> MDIO03_SDWP_XDRB#
- 32.43 MDIO00_SDCD_XDCD# <--> MDIO00_SDCD_XDCD#
- 32.43 MDIO01_MSCD_XDCD# <--> MDIO01_MSCD_XDCD#
- 32.43 MDIO09_SDM/SDWP# <--> MDIO09_SDM/SDWP#



To correct the problem when MS Duo adaptor is in use.



	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low

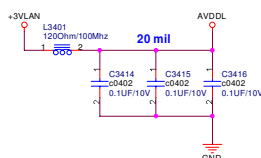
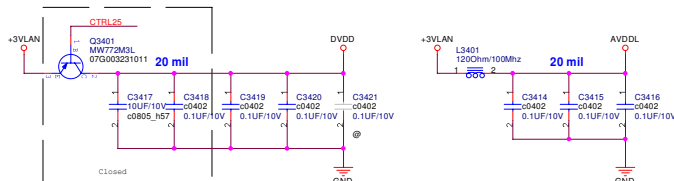
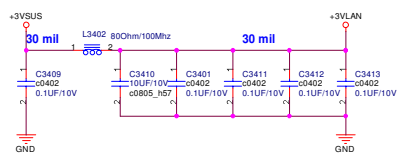
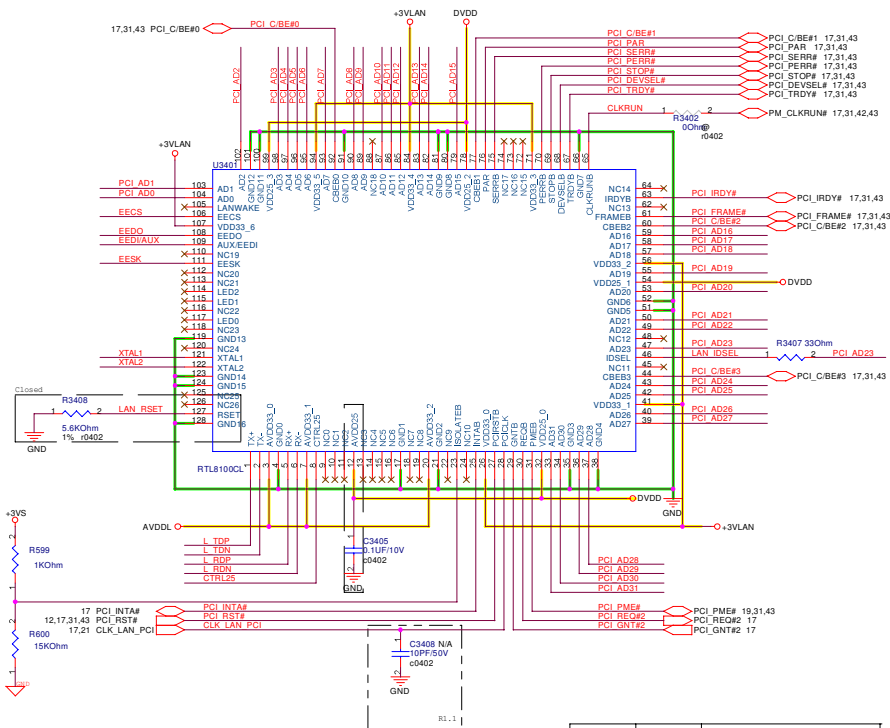
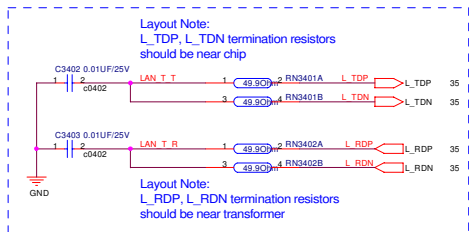
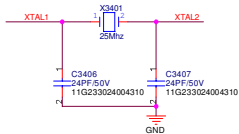
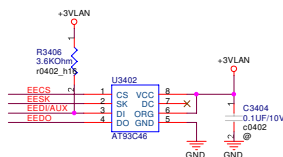


ASUS		Project Name	X51RL
ASUSTeK COMPUTER INC.		Engineer:	MICHAEL WANG
Size	Custom	Title :	CardReader
Date:	Tuesday, July 03, 2007	Sheet	33 of 33

<< Kennedy_Zhang >>

+3VSUS 6,17,19,20,23,25,29,40,51

PCI_AD[0:31] 17,31,43



	RTL8100C	
V_12P	2.5AVDD	PIN 12
AVDDL	3.3AVDD	PIN 3/7/20
VDD	3.3VDD	PIN 26/41/56/71/84/94/107
DVDD	2.5VDD	PIN 32/54/78/99

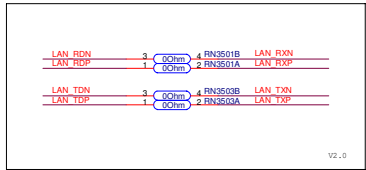
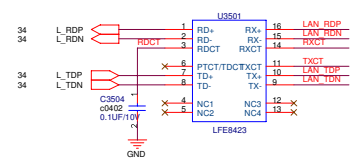
<65mA 3.3V
<25mA 2.5V

ASUS Title: LAN RTL8100CL
 ASUSTeK COMPUTER INC Engineer: MICHAEL WANG
 Size Project Name
 Custom X51RL
 Date: Tuesday, July 03, 2007 Sheet 34 of 63

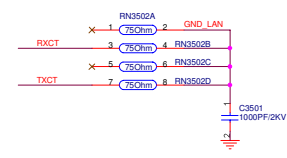
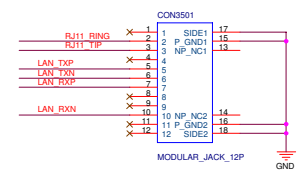
<< Kennedy_Zhang >>

LAN PORT

17,25,26,27,31,37,42,43,44,61

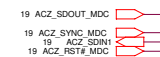
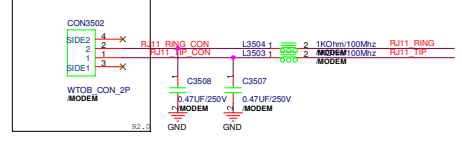


12G14211120

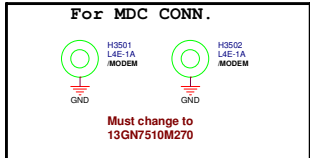
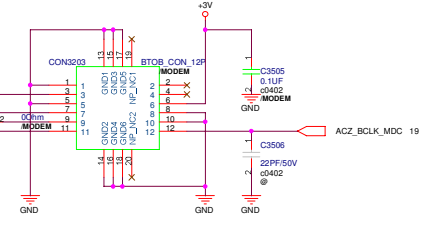


MDC CONNECTOR

12G1700002B=>12G17100002C

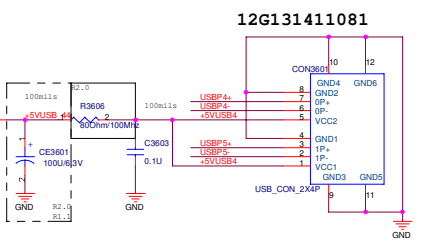
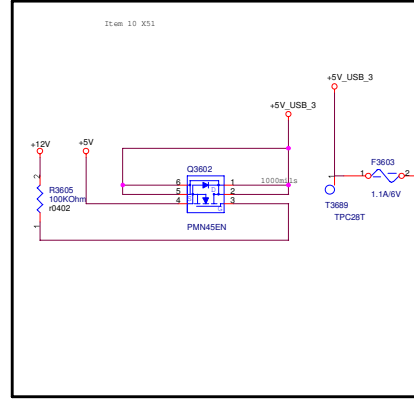
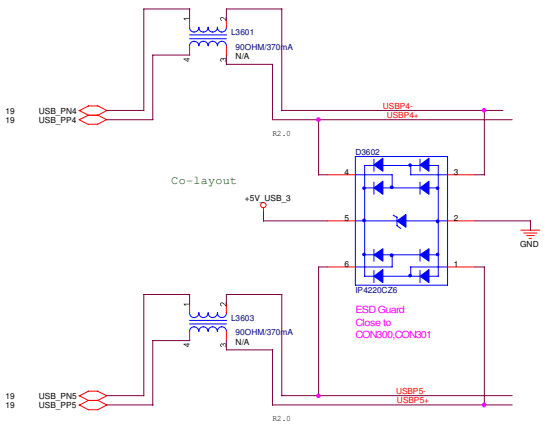
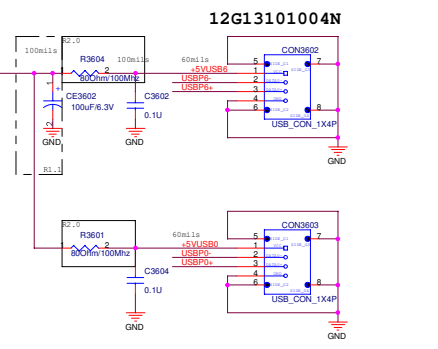
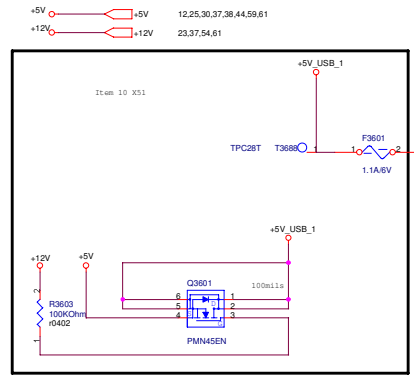
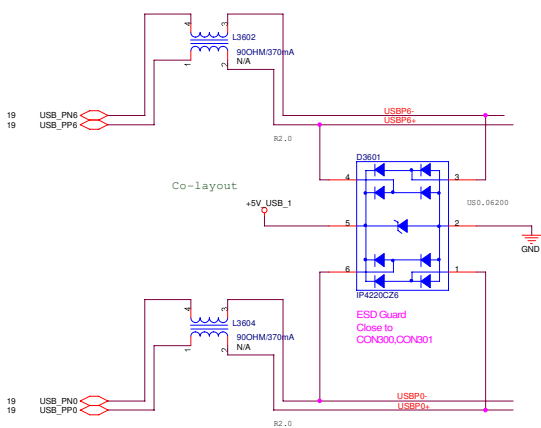


12G161200124



<Variant Name>
ASUS Title: RJ11/45 & MDC
 ASUSTek COMPUTER INC Engineer: MICHAEL WANG
 Size Project Name
 Custom XS1RL Rev
 Date: Tuesday, July 03, 2007 Sheet 55 of 63

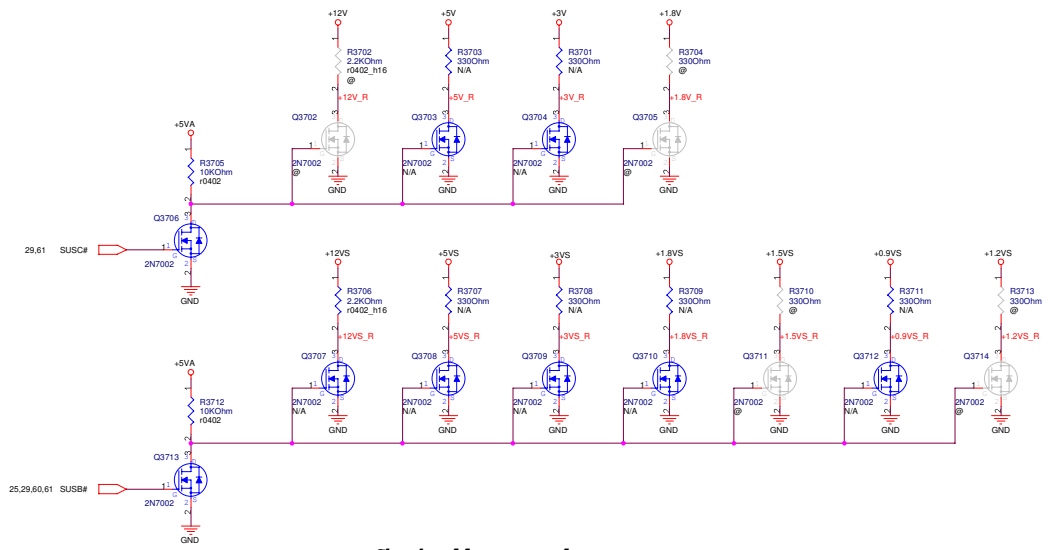
<< Kennedy_Zhang >>



<Variant Name>

ASUS	Project Name	X51RL
ASUSTek COMPUTER INC.	Engineer:	MICHAEL WANG
Size	Title :	USB CONN & +5V DC JACK
Custom	Date:	Tuesday, July 03, 2007
		Sheet 36 of 89
		Rev 2.0

<< Kennedy_Zhang >>



Check all power plan

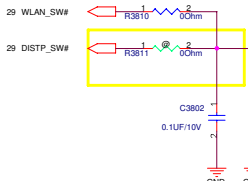
<Variant Name>

ASUS		Title : Discharge Circuit
ASUSTeK COMPUTER INC.		Engineer: MICHAEL WANG
Size	Project Name	Rev
Custom	X51RL	2.0
Date: Tuesday, July 03, 2007	Sheet	37 of 83

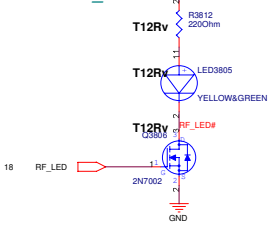
<< Kennedy_Zhang >>

Main Board SW & LED

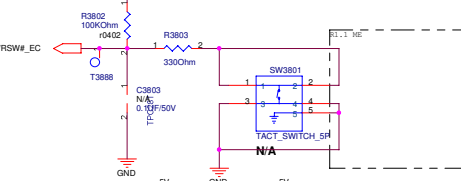
RF/Touchpad Disable



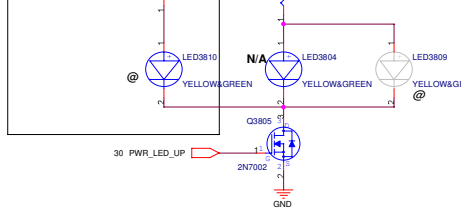
RF_TP LED



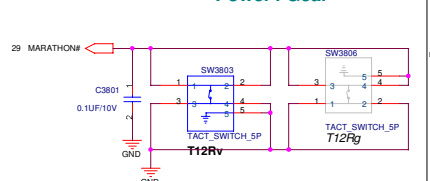
Power Switch



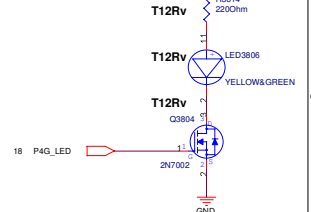
Power LED



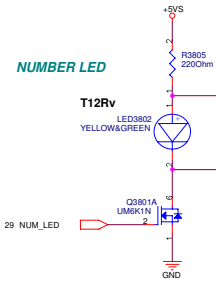
Power4 Gear



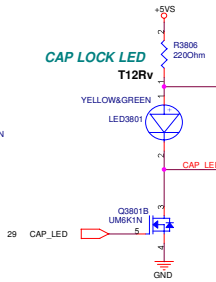
Power 4 Gear LED



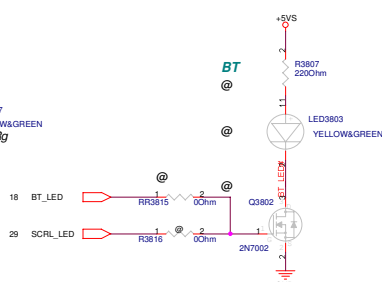
NUMBER LED



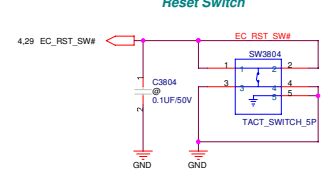
CAP LOCK LED



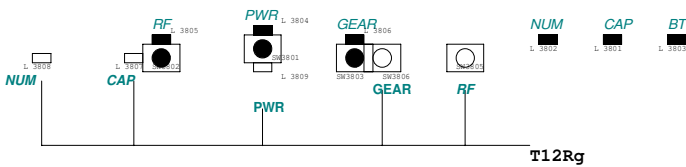
BT



Reset Switch



Placement LED&SW



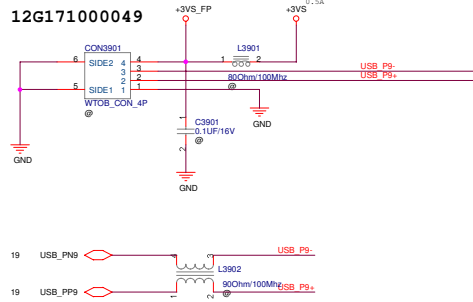
ASUS		Title :SW/LED
ASUSTeK COMPUTER INC.		Engineer: MICHAEL WANG
Size	Project Name	Rev
Custom	X51RL	2.0
Date: Tuesday, July 03, 2007	Sheet	38 of 83

<< Kennedy_Zhang >>

FINGER PRINT Reserved

```

USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER
PRINT
    
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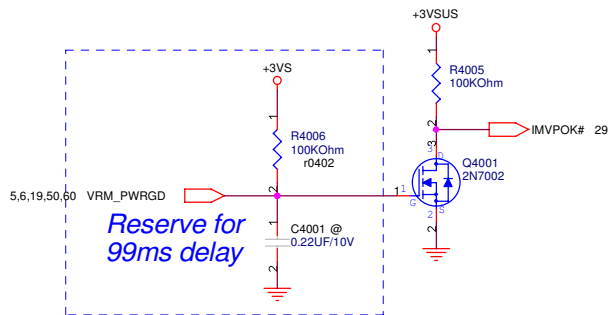
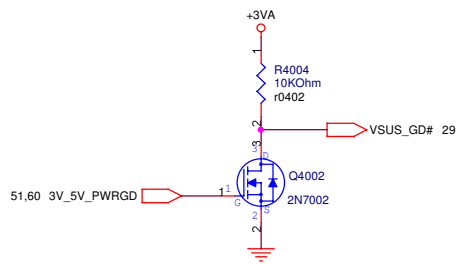


<Variant Name>

ASUS		Title : FINGER PRINT
ASUSTEK COMPUTER, INC.		Engineer: MICHAEL WANG
Size	Project Name	Rev
Custom	X51RL	2.0
Date: Tuesday, July 03, 2007	Sheet	39 of 63

<< Kennedy_Zhang >>

+3VA	○	+3VA	12,17,29,38,54,57,59,63
+3VS	○	+3VS	2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,42,43,50,52,60,61
+3VSUS	○	+3VSUS	6,17,19,20,23,25,29,34,51



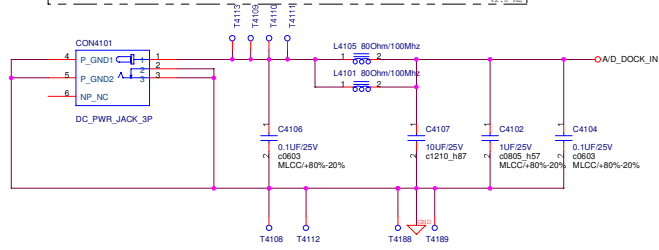
<Variant Name>

ASUS		Title : POWER-ON SEQ.
ASUSTeK COMPUTER INC		Engineer: MICHAEL WANG
Size A4	Project Name X51RL	Rev 2.0
Date: Tuesday, July 03, 2007		Sheet 40 of 63

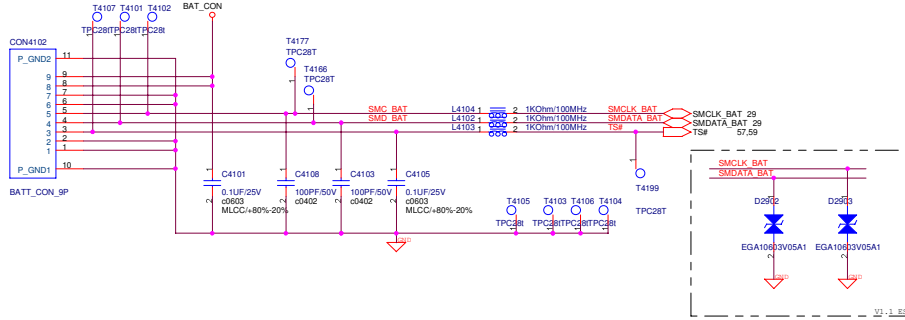
<< Kennedy_Zhang >>

A/D_DOCK_IN A/D_DOCK_IN 57.59
 BAT_CON BAT_CON 57
 AC_BAT_SYS AC_BAT_SYS 12.50,51,52,53,54,57,60

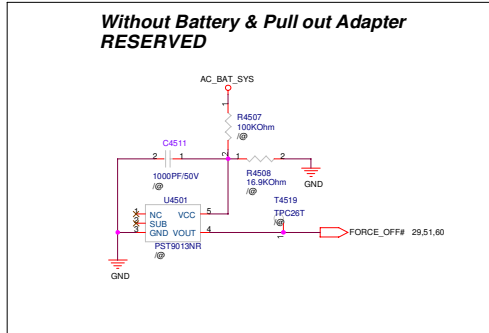
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 V2-0.85



12G20001090G



Without Battery & Pull out Adapter
RESERVED

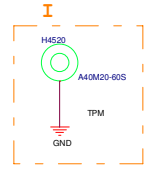
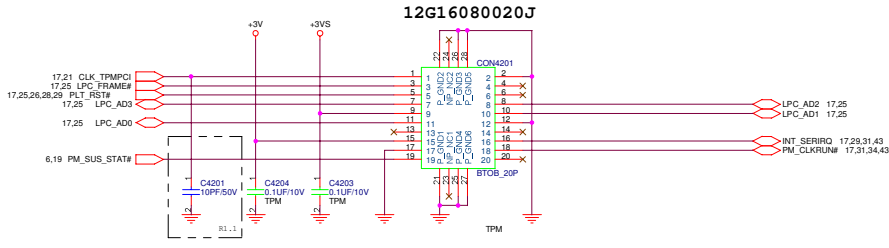


ASUS		Project Name	XS1RL
ASUSTeK COMPUTER INC.		Engineer:	MICHAEL WANG
Size	Custom	Title :	DC IN
Date:	Tuesday, July 03, 2007	Sheet	41 of 89

<< Kennedy_Zhang >>

+3VS ○ ——— ○ +3VS 2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,43,50,52,60,61
 +3V ○ ——— ○ +3V 17,25,26,27,31,35,37,43,44,61

TPM Module CON RESERVED

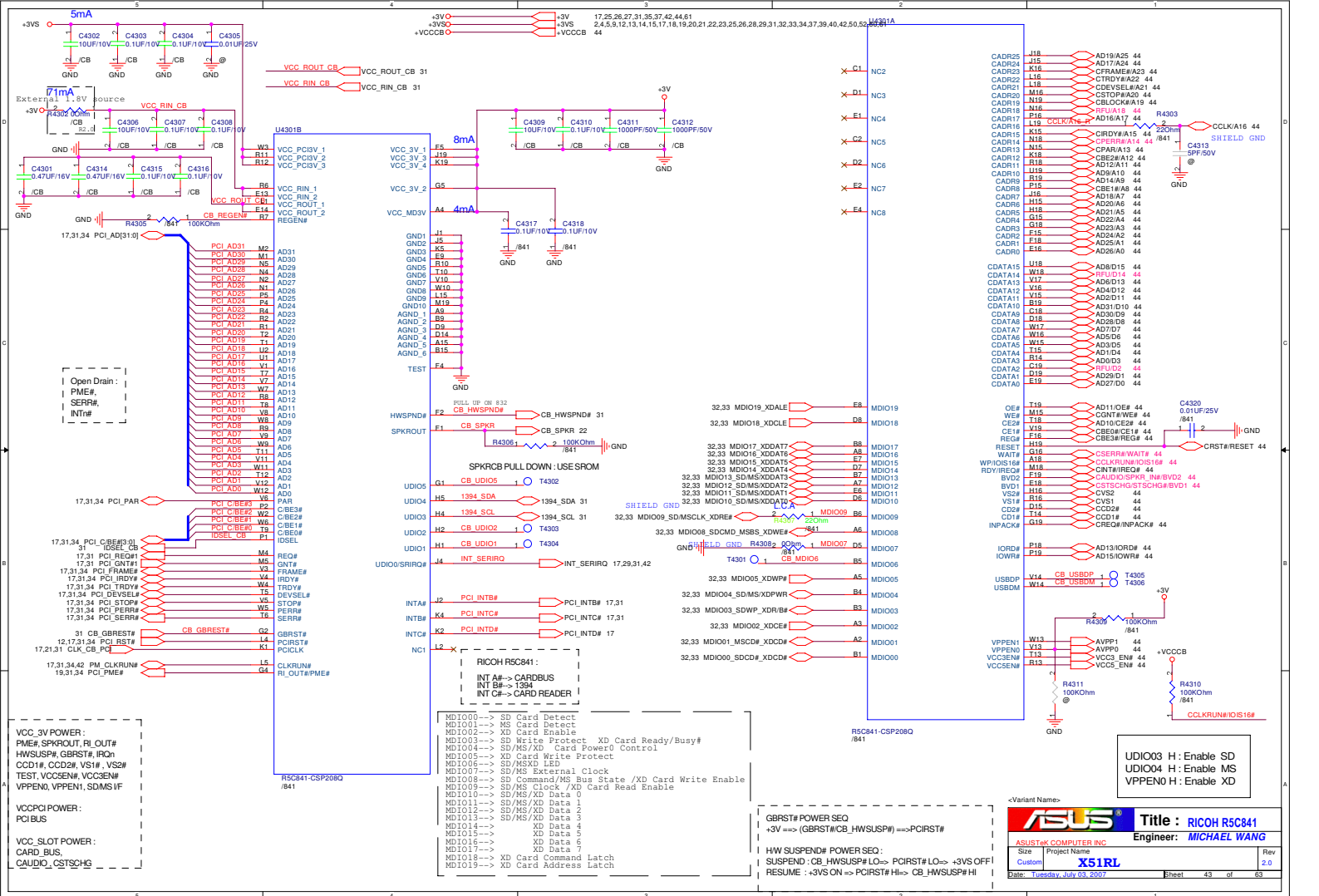


For TPM CONN.

<Variant Name>

ASUS		Project Name	XS1RL
ASUSTeK COMPUTER INC.		Engineer:	MICHAEL WANG
Size	Custom	Title :	TPM 1.2
Date:	Tuesday, July 03, 2007	Sheet	42 of 63

<< Kennedy_Zhang >>

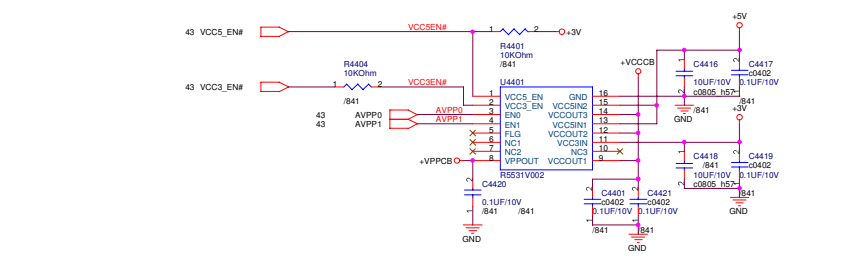
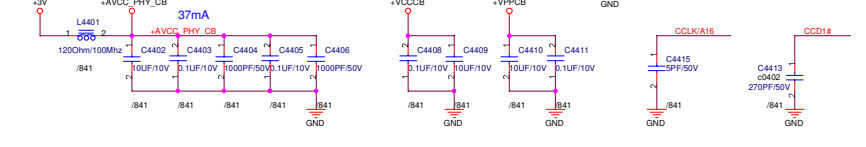
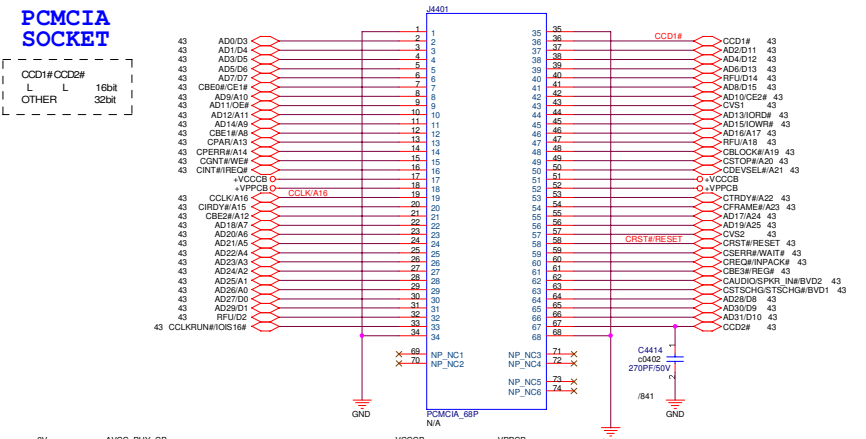
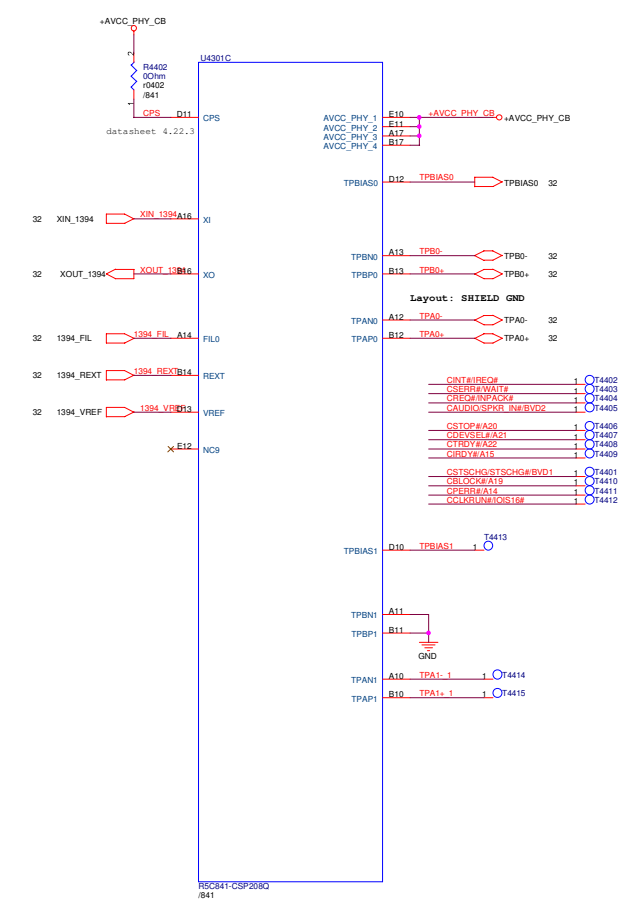


<< Kennedy_Zhang >>

ASUS Title : RICOH R5C841
 ASUSTeK COMPUTER INC. Engineer: MICHAEL WANG
 Size Project Name
 Custom X51RL
 Date: Tuesday, July 03, 2007 Sheet 43 of 83

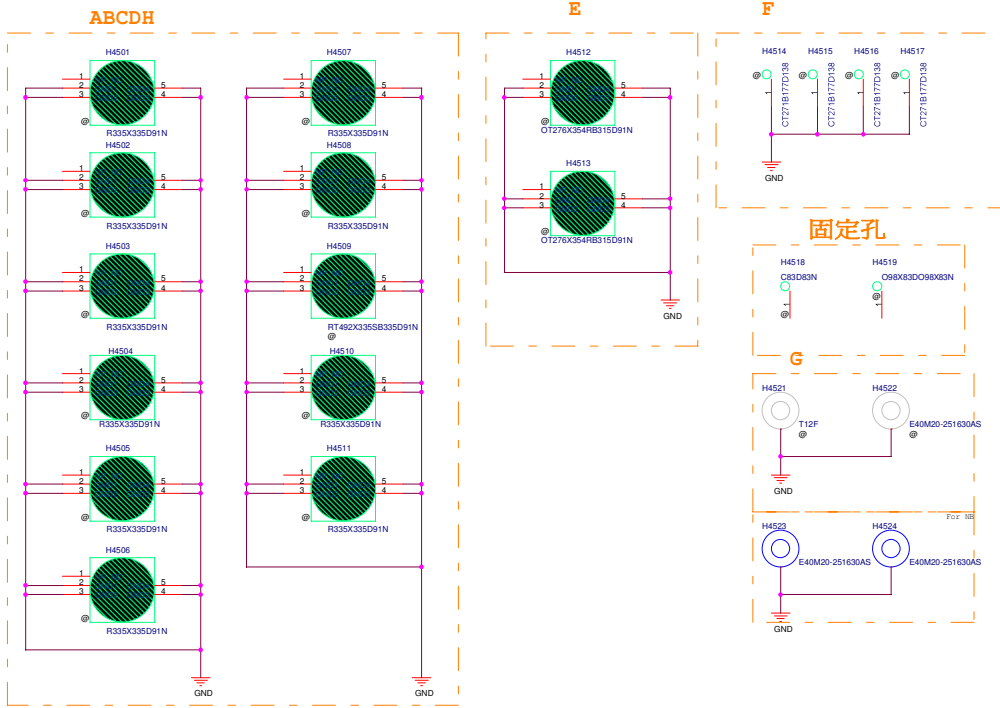
PCMCIA SOCKET

CCD1# CCD2#
 L L 16bit
 OTHER 32bit



ASUS Title: CARBUS SOCKET
 ASUSTek COMPUTER INC Engineer: MICHAEL WANG
 Size Project Name
 Custom X51RL Rev 2.0
 Date: Tuesday, September 04, 2007 Sheet 44 of 55

<< Kennedy_Zhang >>



固定孔

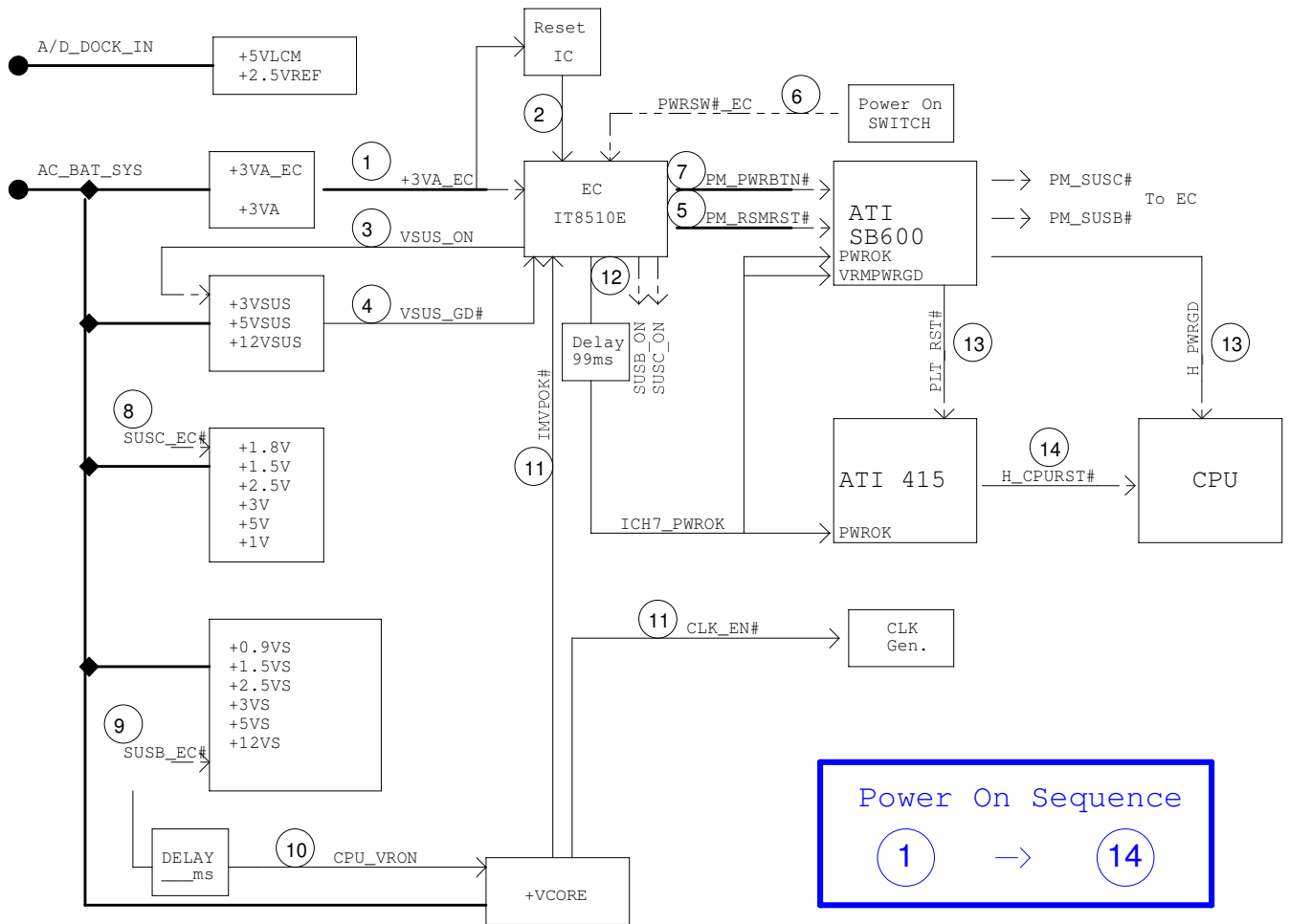
<Variant Name>

ASUS		Title : SCREW HOLE
ASUSTeK COMPUTER INC		Engineer: MICHAEL WANG
Size	Project Name	Rev
Custom	XS1RL	2.0
Date: Wednesday, May 16, 2007	Sheet	45 of 63

<< Kennedy_Zhang >>

ASUS		Title : HISTORY	
ASUSTek COMPUTER INC		Engineer: MICHAEL WANG	
Size	Project Name	Rev	
Custom	X51RL	2.0	
Date	Wednesday, May 16, 2007	Sheet	46 of 63

<< Kennedy_Zhang >>



Power On Sequence
 1 → 14

ASUS		Title: FLOWCHART	
ASUSTek COMPUTER INC		Engineer: MICHAEL WANG	
Size	Project Name	Rev	
Custom	X51RL	2.0	
Date: Wednesday, May 16, 2007	Sheet 47 of 83		

<< Kennedy_Zhang >>

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	O	48	GPH0	VSUS_ON	O
33	PWM1/GPA1	FAN_PWM	O	54	GPH1	VSUS_GD#	I
36	PWM2/GPA2	/	/	55	GPH2	IMVPOK#	I
37	PWM3/GPA3	/	/	69	GPH3	PM_PWRSTN#	O
38	PWM4/GPA4	CHG_LED_UP#	O	70	GPH4	SUSC_EC#	O
39	PWM5/GPA5	PWR_LED_UP#	O	75	GPH5	SUSB_EC#	O
40	PWM6/GPA6	BATSEL_SS#	O	76	GPH6	CRU_VRON	O
43	PWM7/GPA7	LCD_BACKOFF#	O	105	GPH7	PM_RSMRST#	O
153	RXD/GPB0	NUM_LED	O	148	GP0	ICH7_PWR0K	O
154	TXD/GPB1	CAP_LED	O	149	GP1	WATCH_DOG#	O
162	GPB2	SCRL_LED	O	152	GP2	/	/
163	SMCLK0/GPB3	SMCLK_BAT	I/O	155	GP3	CHG_EN#	O
164	SMDAT0/GPB4	SMDATA_BAT	I/O	156	GP4	PRECHG	O
5	GA20/GPB5	A20GATE	O	168	GP5	BAT_LL#	O
6	KBRST#/GPB6	RC_IN#	O	174	GP6	BAT_LEARN	O
165	GPB7	THRO_CPU	O	0	GPL0	WLAN_ON#	O
169	SMCLK1/GPC1	SMB1_CLK	I/O	11	GPL1	BT_ON#	O
170	SMDAT1/GPC2	SMB1_DAT	I/O	12	GPL2	RF_OFF_SW#	I
171	GPC3	/	/	20	GPL3	RF_LED	O
172	TMIR0/WUI2/GPC4	ACIN_OC#	I	92	CRX	CRX	I/O
175	GPC5	OP_SD#	O				
176	TMIR1/WUI3/GPC6	BAT_IN_OC#	I				
1	CK32KOUT/GPC7	/	O				
26	RT1#WUI0/GPD0	PM_SUSB#	I				
29	RT2#WUI1/GPD1	PM_SUSC#	I				
30	LPC_RST#WUI4/GPD2	PLT_RST#	I				
31	ECSW#/GPD3	EXT_SC#	I				
41	OPD	/	O				
42	GNT/GPD5	/	I				
62	TACH0/GPD6	FAN0_TACH	I				
63	TACH1/GPD7	/	O				
87	ADC4/GPE0	WLAN_SW#	I				
88	ADC5/GPE1	/	I				
89	ADC6/GPE2	MARATHON#	I				
90	ADC7/GPE3	DISP_SW#	I				
2	PWRSW/GPE4	PWRSW_EC	I				
44	WUI5/GPE5	/	I				
24	LPCPD#WUI6/GPE6	LID_EC#	I				
25	CLKRUN#WUI7/GPE7	/	O				
110	PS2CLK0/GPF0	/	/				
111	PS2DAT0/GPF1	/	/				
114	PS2CLK1/GPF2	/	I/O				
115	PS2DAT1/GPF3	/	I/O				
116	PS2CLK2/GPF4	TP_CLK	/				
117	PS2DAT2/GPF5	TP_DAT	/				
118	PS2CLK3/GPF6	PWRLMT#	/				
119	PS2DAT3/GPF7	/	I				
113	FA16/GPG0	FA16	/				
112	FA17/GPG1	FA17	/				
104	FA18/GPG2	FA18	/				
103	FA19/GPG3	/	/				
3	FA20/GPG4	THRM_CPU#	I				
4	FA21/GPG5	/	/				
27	LPCSHL/GPG6	PMTHERM#	O				
28	LPCSOLL/GPG7	AC_APR_UC#	I				

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BI_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REG#	PCI_REG#	I
G8	GPIO02/PREQ#	PCI_INT#	I
F7	GPIO03/PREQ#	PCI_INT#	I
F3	GPIO04/PREQ#	PCI_INT#	I
G7	GPIO05/PREQ#	PCI_INT#	I
AC21	GPIO6	BT_LED	I/O
AC18	GPIO7	/	I
E21	GPIO8	EXTSM#	I
A20	GPIO9	SATA_DET#0	O
E20	GPIO10	/	I
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SC#	I
E19	GPIO13	/	I
R4	GPIO14	/	I
E22	GPIO15	WLAN_LED#	I/O
AC22	GPIO16	PM_DPRSPLV#	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP#	/	I
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP#	/	I
A13	GPIO22/REG#	PCI_REG#4	I
AA5	LDRQ1#/GPIO23	LPC_DRQ#1	I/O
R3	GPIO24	P4G_LED#	I
D20	GPIO25	CB_SD#	O
A21	GPIO26/EL_RSVD	BT_DET#	I
B21	GPIO27/EL_STATE0	/	I
E23	GPIO28/EL_STATE1	/	I
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	/	O
U2	GPIO34/AZ_DOCK_RST#	/	O
AD21	GPIO35	ICH_GPIO35	O
AH19	GPIO36/SATA2GP#	/	I
AE19	GPIO37/SATA3GP#	PCB_ID0	I/O
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIe Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

ASUS Title : GPIO Setting
 Project Name: X51RL
 Engineer: MICHAEL WANG
 Date: Wednesday, May 18, 2005
 Page: 48 of 63

<< Kennedy_Zhang >>

T12R V1.1 History

- Page 17, del U1702 and R1726 delete PCI_RST# Buffer.
- Page 18, added R1802
- Page 43&42, D4301 and L1201R footprint
- Page 6, delete D1204 and added R601 R609 to avoid can not boot.
- Page 17, Mount R1703, U1703 option changed reset path
- Page 43, Mount R4302 for R5C841 internal LDO input
- Page 9, un-mount L306 C314 , these for 610 only
- All PCI clock added 6.8 pF to decrease skew.
- PWM connected to EC and back-light connected to NB
- D1306 D1301 connected to +SVs, let these signal have the same PWR plan. For ESD
- page 19, added BT_DET# to detect BT.
- Page 19, adjust USB OC ping to correspond USB port
- Page 25, modification NEW CARD debug circuit to correspond new debug card
- page 28, we used correctly capacity for customer request.
- page 36, we used LDO with over current protect IC
- page 41, DC in connector add 2nd source.

SE modify

- ODD 内部 0.4mm
- BATT 内部 0.23mm
- 增加 内部 0.23mm
- 增加 内部 0.23mm

6.DDR2 added 2nd source
P/N :15G015022004
DDR2 DIMM 200P,1.5V,H:4mm,STD
FOXCONN/AS0A426-N4SN-1

- add led 1 pcs LED3810 and del. SW3807(option)
- 实际图修改

T12Rg V1.0 modify from T12R V2.0

- To modify BOM include LED(colorsplacement), SW(placement), HDD(PATA TO SATA), FCCM(unmount), internal MIC(unmount) and R5C841(added 1394 cardreader and PCMCIA).

T12Rg V2.0

- Page 12, L1203 0 Ohm to bead, EMI request.
- Page 12, L1204 and L1205 0 Ohm to bead and mount C1222 C1223, EMI request.
- Page 12, mount L1214 L1215 Ohm for added internal speaker.
- Page 12, mount L1206, EMI request.
- Page 6, R2301 and R2304 10K to 12K for 2W speaker..
- Page 6, modify BOM, unmount R2908.

T12R V2.1/ X51 V1.0 modify from T12R V2.0

- Page 6, support DDRII 667, modify DOR schematic(CKE OFD)
- Page 6, replacement SB A20 form A13
- Page 6, modify BOM, delete R2908.
- Page 6, added D2910 for EMI.
- Page 6, to support 3S1P, added some circuit EC to H_PROCHOT_S#.
- Page 6,modify BOM include LED, SW, HDD(DEL PATA), FCCM and R5C841(added).

T12R V2.0 Modify History

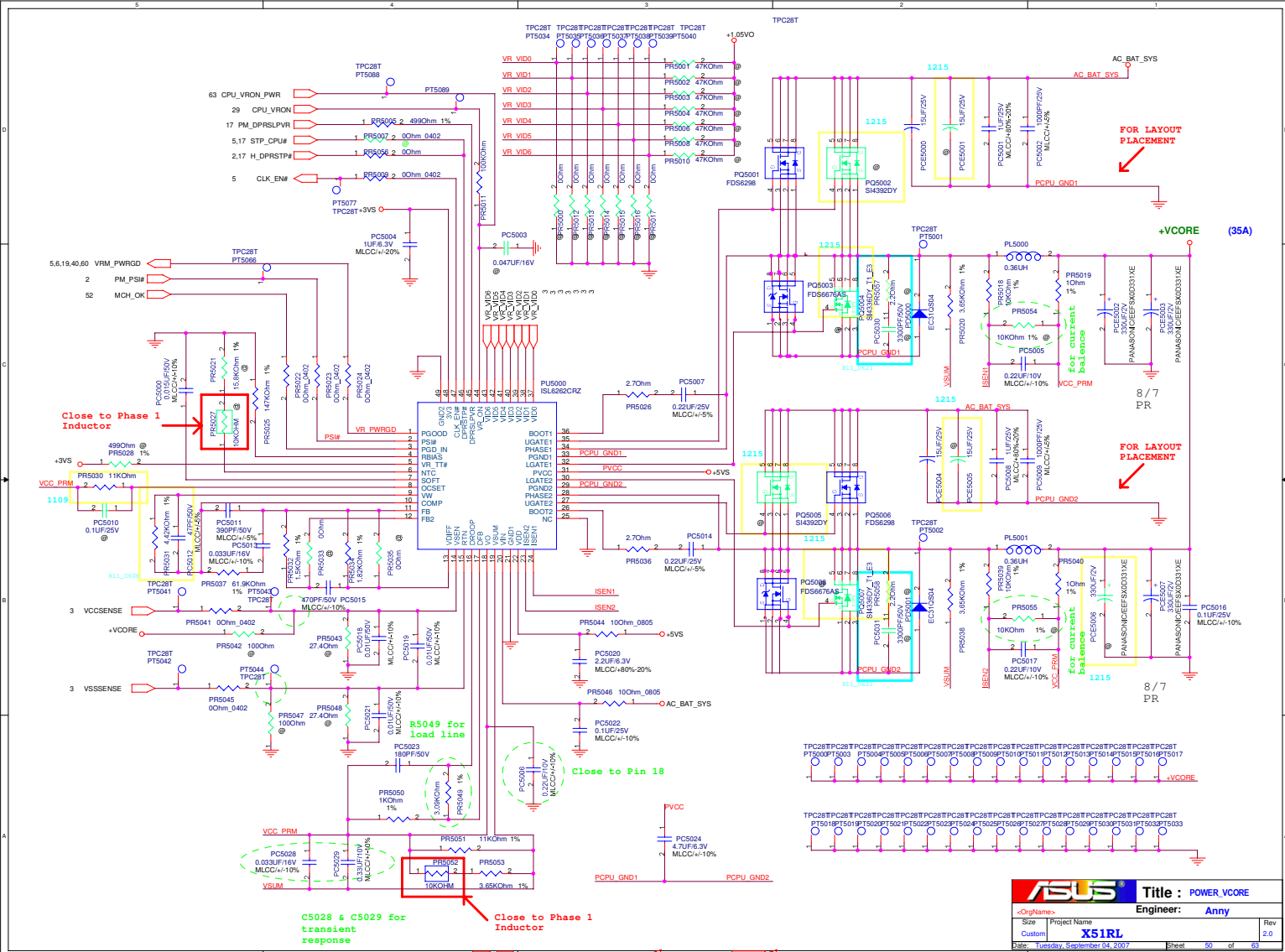
- Page 6, R609 replacement 220K by 10K
- Page 12, RML203 replacement C.M chock by 00hm for EMI.
- For DDRII connector(H=4mm) replacement 12G025022004 by original.
- For DDRII connector(H=9mm) replacement 12G025C22004 by original.
- For DC IN jack replacement 12G14530103R by original(long core).
- Page 22 for audio micro phone low quality issue, it need to changed larger capacitor 10U (replace 10U with 1U).
- Page 29, we changed new EC 8511.
- Page 38, to increase LED brightness, we replace 07G015200485 by original
- page 30, for EMI request, we added L3010 and L3011 and mount C3002 C3003 and C3006-3010
- Page 35, for EMI request, we added 00hm before LAN jack for option CM chock.

	X51	T12RG	T12R
NB	415ME	415ME	415MD
SB	SB600_A21	SB600_A21	SB600_A13
AUDIO	660VD	660VD	660VD
SPDIF	N/A	N/A	N/A
R5C832	N/A	N/A	N/A
R5C841	OK	OK	N/A
1394	N/A	OK	N/A
CARD READER	OK	OK	N/A
PCMCIA	OK	OK	N/A
NEW CARD	N/A	N/A	N/A
TPM	N/A	OK	N/A
BT	OK	N/A	N/A
PC_CAM	N/A	N/A	OK
TNT - MIC	N/A	OK	OK
MODEN	OK	N/A	N/A
TV	N/A	N/A	N/A
SPEAKER	1.5W	2W	1.5W



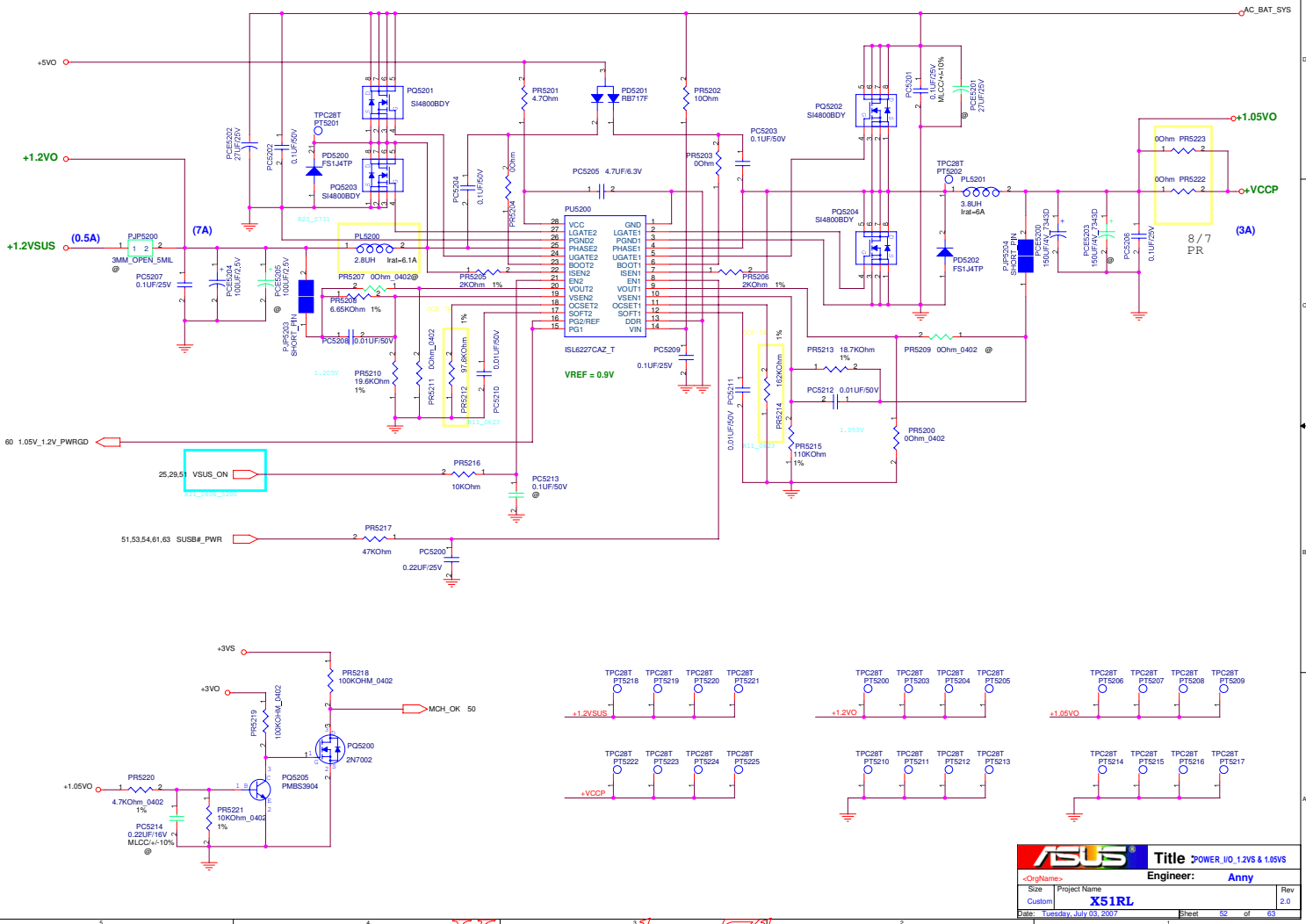
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Engineer: [Signature]
Date: [Blank]

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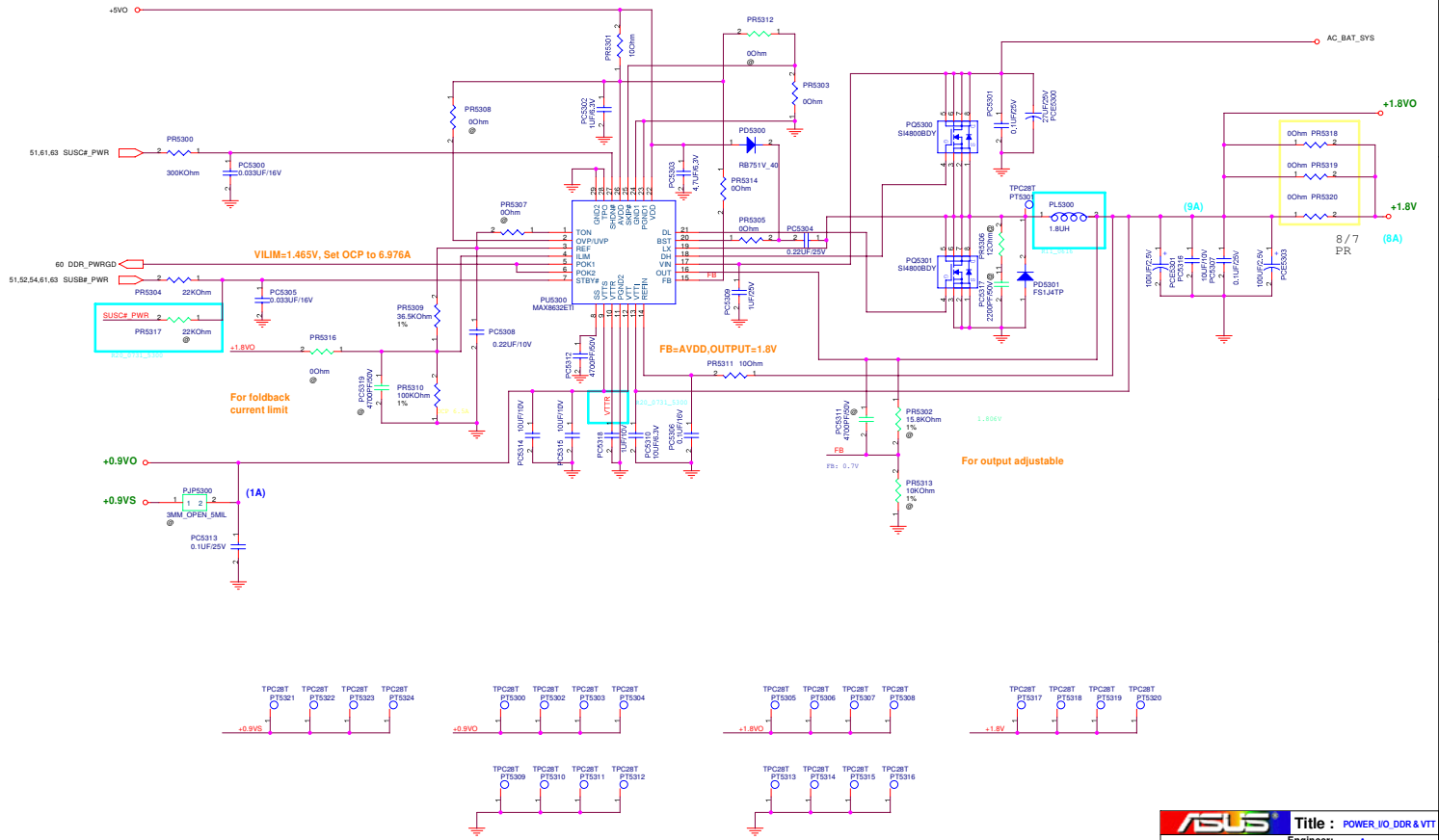
ASUS		Title : POWER_VCORE	
-<OrigName>		Engineer: Anny	
Size	Project Name		
Custom	X51RL		
Date: Tuesday, September 04, 2007	Sheet	60	of 83
Rev	2.0		

<< Kennedy_Zhang >>



ASUS		Title POWER_IO_1.2VS & 1.05VS	
<OrigName>	Size	Project Name	Engineer: Anny
Custom	2.0	X51RL	Rev
Date: Tuesday, July 03, 2007	Sheet	68	of 83

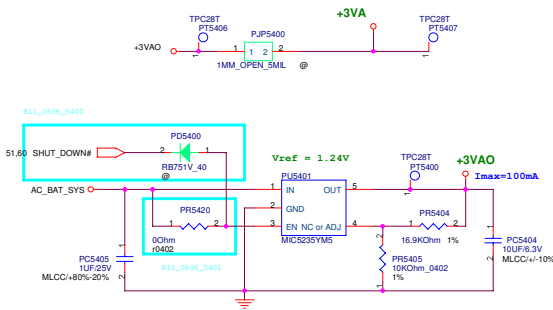
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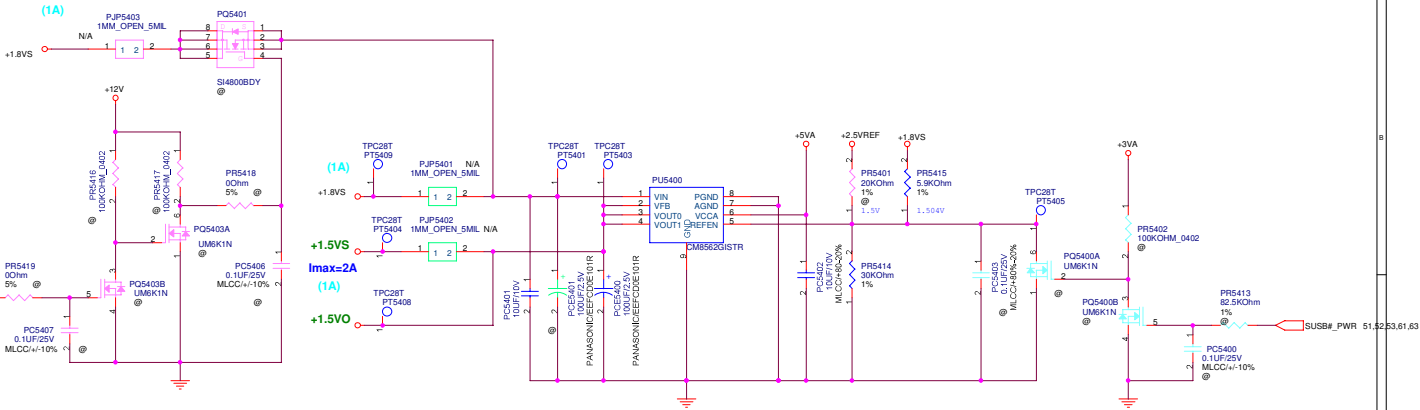
ASUS		Title : POWER_IO_DDR&VTT
OrigName:	Project Name	Engineer: Anny
Size	Customer	Rev
Custom	XS1RL	2.0
Date: Tuesday, July 03, 2007	Sheet	53 of 65

<< Kennedy_Zhang >>

+3VAO



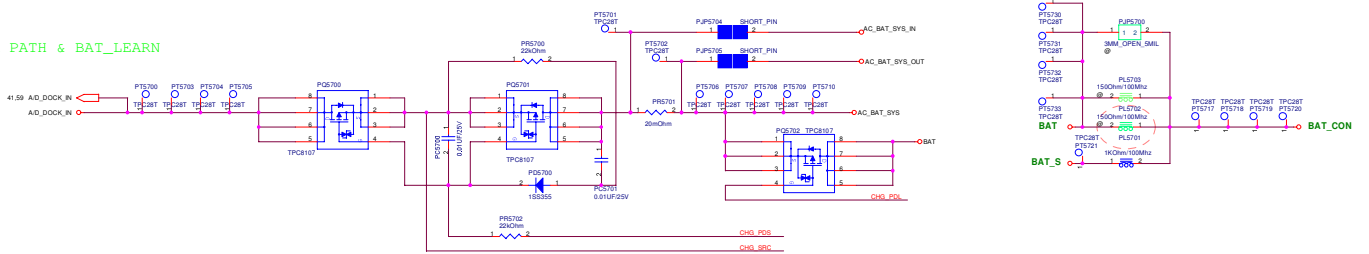
+2.5VS



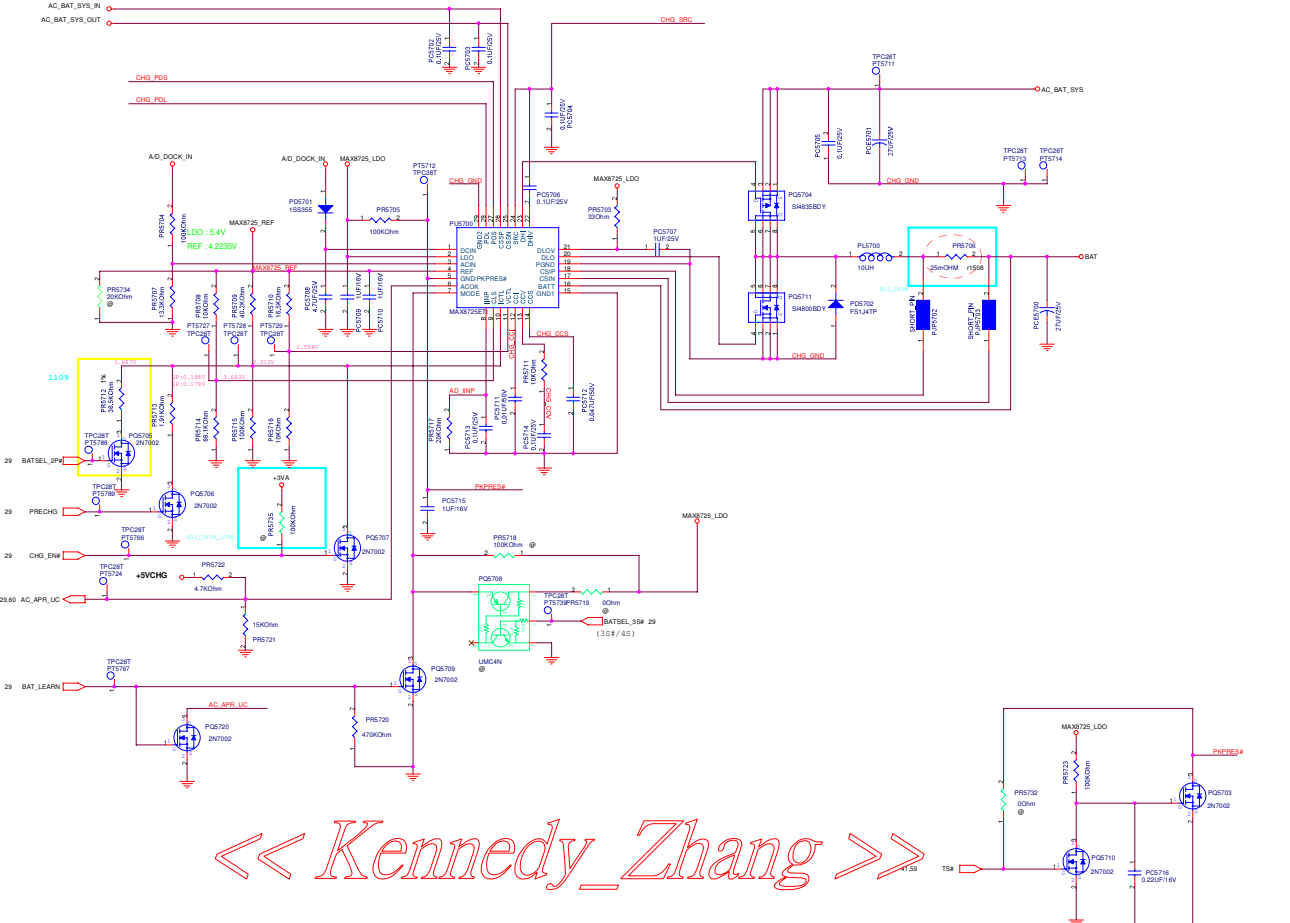
ASUS		Title : POWER_IO_+3VA & +2.5V	
Size	Project Name	Engineer:	Anny
Custom	X51RL	Rev	2.0
Date:	Tuesday, July 03, 2007	Sheet	54 of 83

<< Kennedy_Zhang >>

POWER PATH & BAT_LEARN



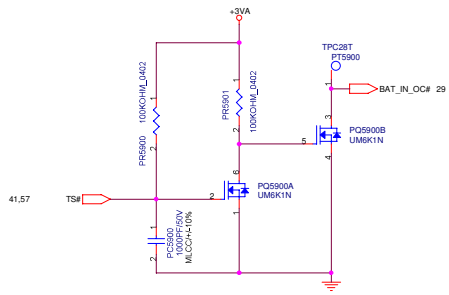
- AC_IN Threshold 2.04Vmax AD_DOCK_IN
 => 17.6V active
 Adapter (Vmax) = (0.075V/Rsense/ADH)[VCLS/VREF]
 Resense(ADH) = 0.02 ohm
 VCLS = 3.62V
 => Vmax = 3.62V / 0.02A
 => Constant Power = 19 * 1.27 = 62.13W
 => RSense = 0.02A
- Charge Current Ichg = (B.075V/Rsense/CHG)[VCLS/0.6V]
 Resense(CHG) = 0.025 ohm
 VCLS = 3.512V => Ichg = 2.51A
 VCLS = 1.687V => Ichg = 1.4A
- Vbat = Cell * (Vbat - (VCTL - 1.9V) / 9.52)
 VCTL = 1.98V
 => Vbat = 4.2V (4.20188V)
- Mode pin : Vinode = 2.58V (in 0.100 ohm) => 4.0mA
 2.0 * Vinode = 1.8V (Reading) => 3.0mA
 2.5 * Vinode (in 0.100 ohm) => Learning mode
- VCTL < 0.8V or DCIN < 7V => Charger Disable
- Precharge current = 150mA
 VCTL_pre2p = 0.188V => Ichg = 157mA
 VCTL_pre1p = 0.179V => Ichg = 148mA



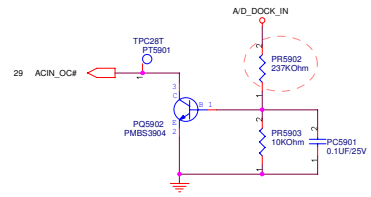
<< Kennedy_Zhang >>

ASUS		Title : POWER CHARGER	
<OrigName>	Project Name	Engineer:	Anny
Size	Custom		
	Customer		
	Model Name		
	Part No.		
	Rev		
	Size		

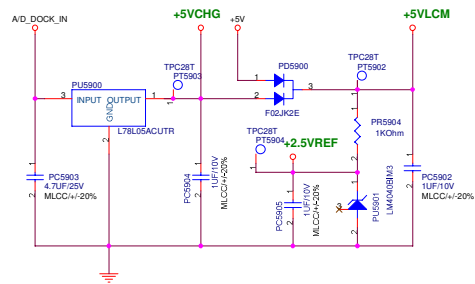
BATTERY IN DETECT



ADAPTER IN DETECT

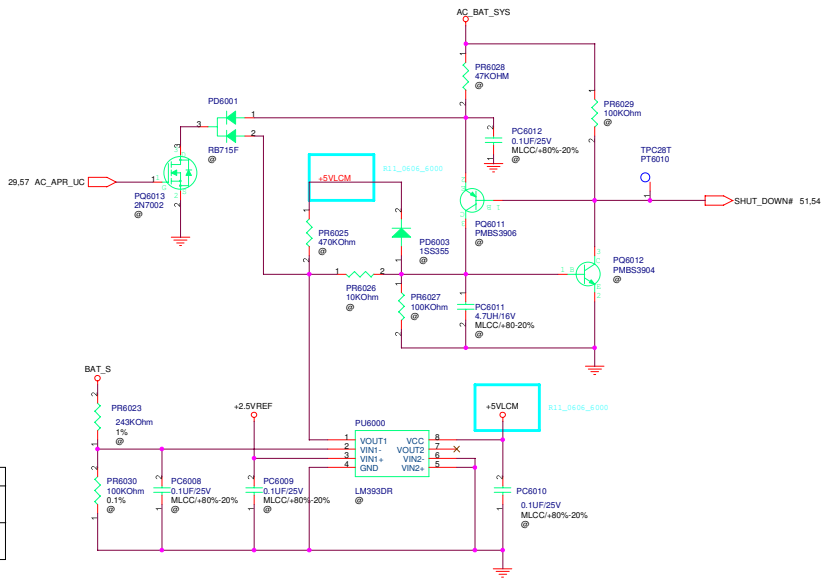


+5VLCM, +5VCHG & +2.5VREF



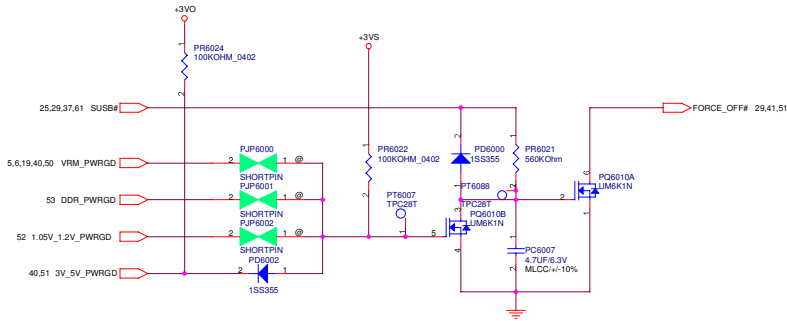
ASUS		Title : POWER_DETECT	
--CrtName--		Engineer: Anny	
Size	Project Name		Rev
Custom	X51RL		2.0
Date: Tuesday, July 03, 2007		Sheet	59 of 63

<< Kennedy_Zhang >>



	8.575V	11.625V
86023	243KOhm 10G211243113030 1%	365KOhm 10G21365313010 1%
86024	100KOhm 10G21100323010 5%	100KOhm 10G21100323010 5%

POWER GOOD DETECTOR

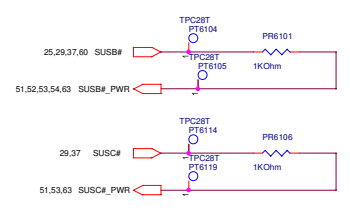
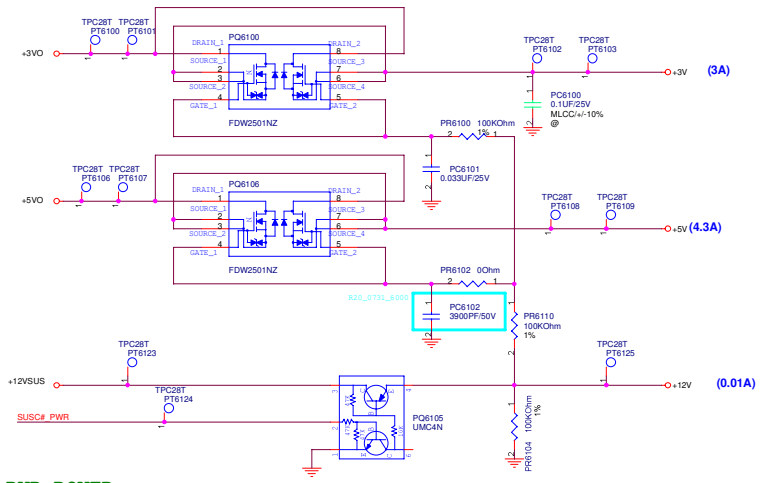


- TPC28T PT6003 1 VRM_PWRGD
- TPC28T PT6004 1 DDR_PWRGD
- TPC28T PT6005 1 3V_5V_PWRGD
- TPC28T PT6006 1 1.05V_1.2V_PWRGD

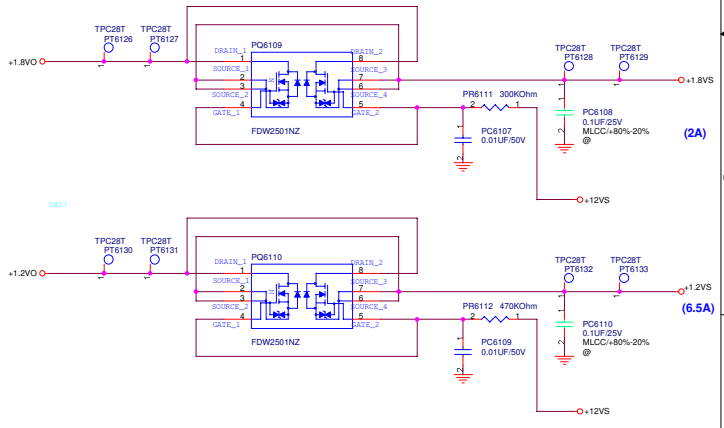
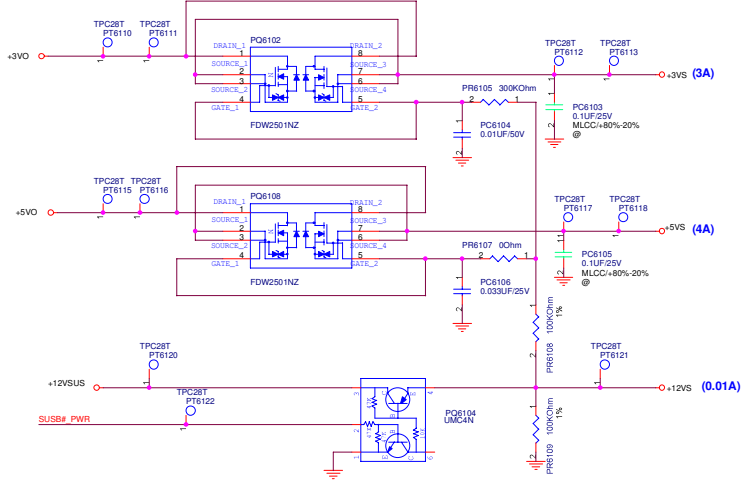
ASUS		Title : POWER_PROTECT	
Size	Project Name	Engineer:	Anny
Custom	X51RL		
Date:	Tuesday, July 03, 2007	Sheet	60 of 83

<< Kennedy_Zhang >>

SUSC#_PWR POWER



SUSB#_PWR POWER

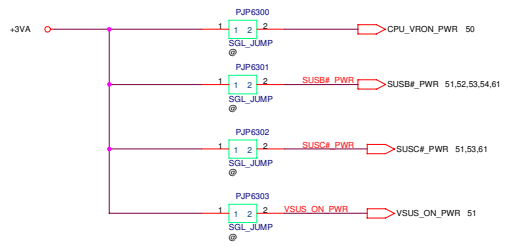


ASUS		Title : POWER_LOAD_SWITCH	
<OrigName>	Project Name	Engineer:	Anny
Size	Custom	X51RL	Rev 2.0
Date:	Tuesday, July 03, 2007	Sheet	61 of 83

<< Kennedy_Zhang >>



FOR POWER TEST



ASUS		Title : POWER_SIGNAL	
-<OrigName>		Engineer: Anny	
Size	Project Name		Rev
Custom	X51RL		2.0
Date:	Tuesday, July 03, 2007	Sheet	63 of 63

<< Kennedy_Zhang >>

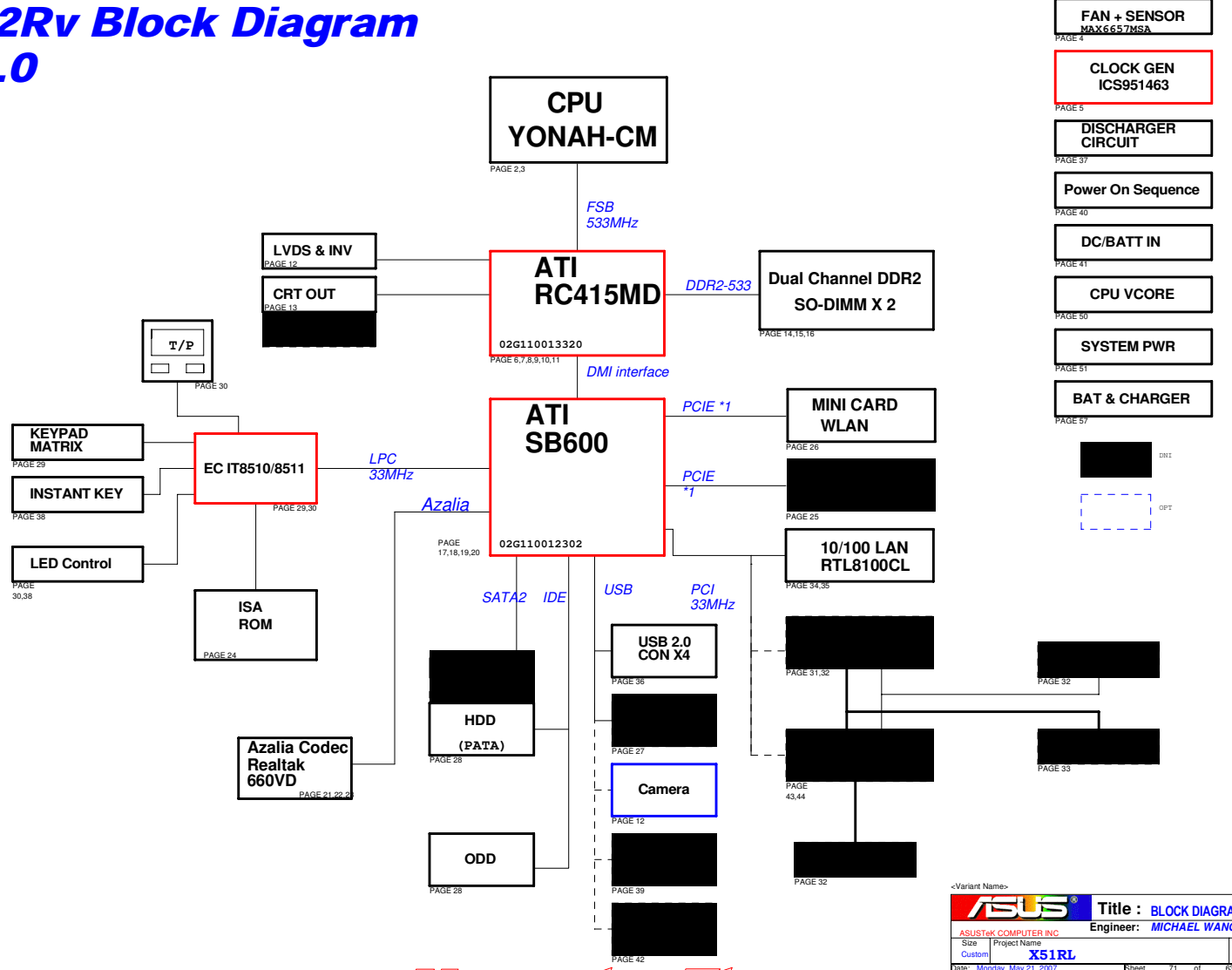
R2.0

Item	Before	After	Reason	Owner	Date
R20_1109_30		Add PCB5001 PCB5005, PQ5002, PQ5004, PQ5005 and PQ5007	VCORE:CPU upgrade to merom reflash		2006.11.09
R20_1109_36	9.31K	11K	VCORE: PR5030 modify to 11K to Increase OCP.		2006.11.09
R20_1109_37	PR5712 and PQ5705 were unmounted	PR5712:36.5K and PQ5705 was mounted.	Charger: Modify PR5712 and PQ5705 for 3S1P select.		2006.11.09

		Title : POWER PIC	
<OrigName>		Engineer:	
Size	Project Name		Rev
Custom	X51RL		2.0
Date: Monday, May 21, 2007		Sheet	64 of 83

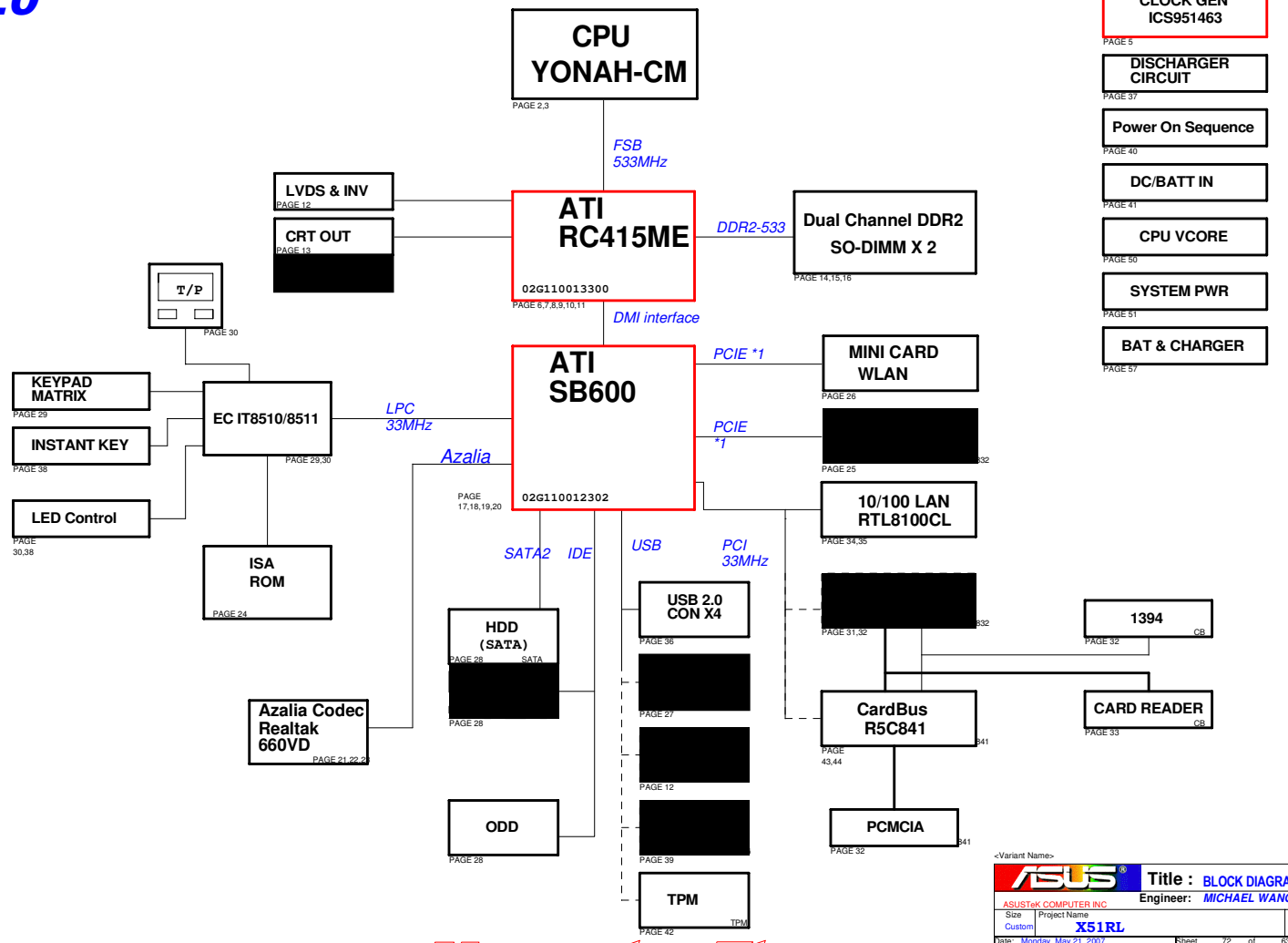
<< Kennedy_Zhang >>

T12Rv Block Diagram V2.0



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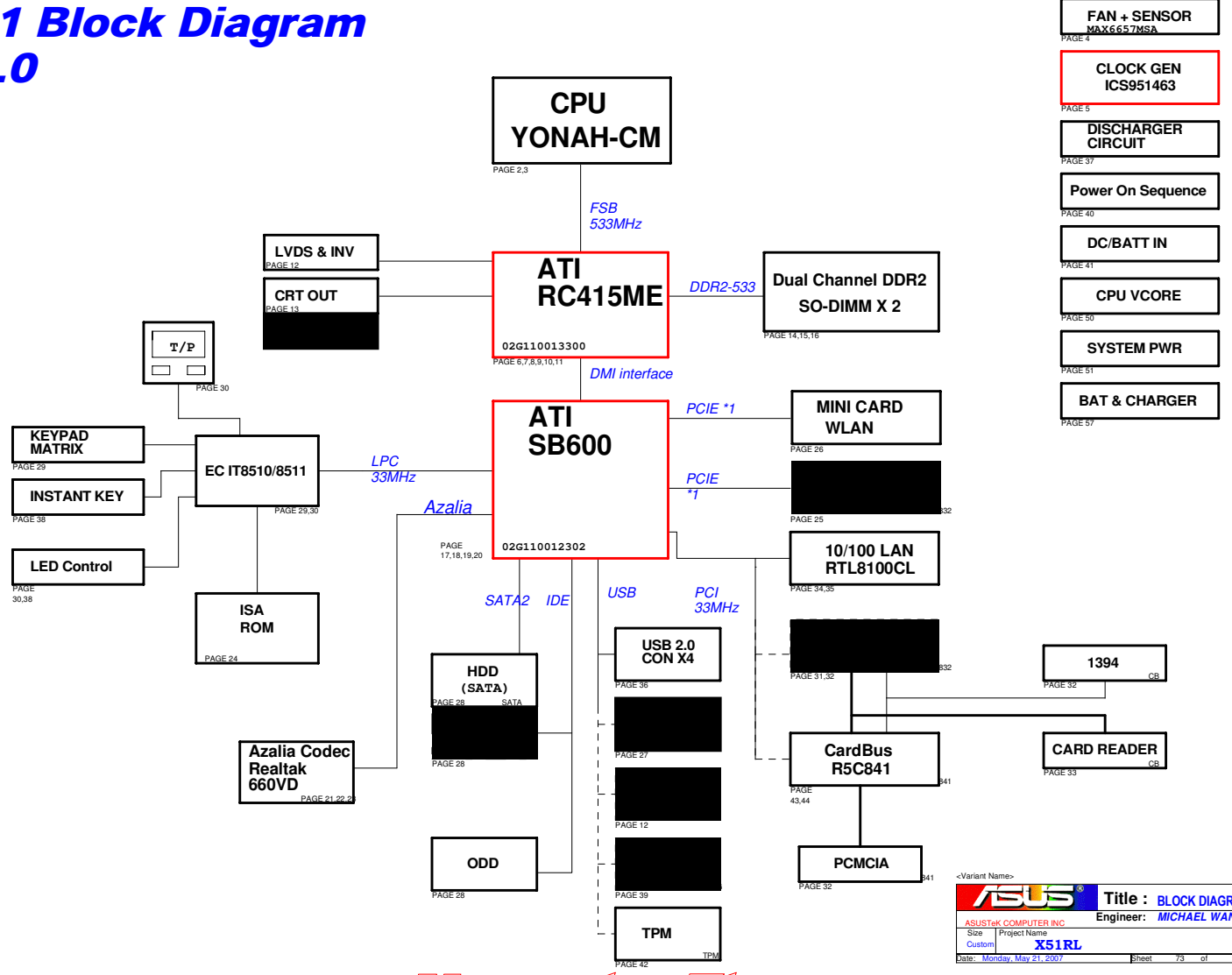
T12Rg Block Diagram V2.0



ASUS
 ASUSTEK COMPUTER INC
 Size: Custom Project Name: X519L
 Date: Monday, May 21, 2007 Sheet 72 of 85
 Title: BLOCK DIAGRAM
 Engineer: MICHAEL WANG
 Rev: 2.0

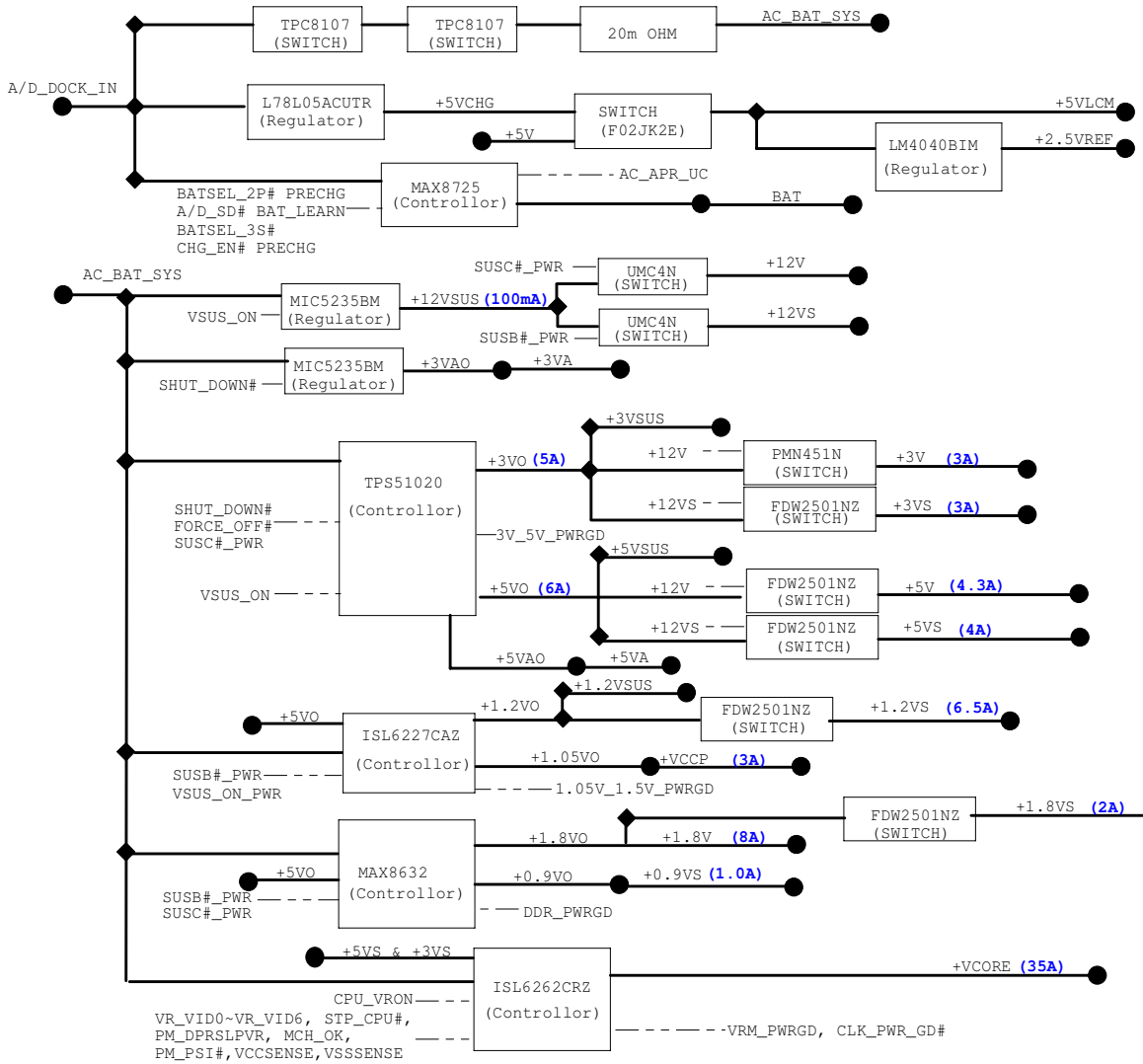
<< Kennedy_Zhang >>

X51 Block Diagram V2.0



ASUS		Title : BLOCK DIAGRAM	
ASUSTek COMPUTER INC	Size	Project Name	Engineer: MICHAEL WANG
Custom		X51RL	Rev 2.0
Date: Monday, May 21, 2007			Sheet 73 of 83

<< Kennedy_Zhang >>



ASUS		Title : POWER_FLOWCHART	
Size	Project Name	Engineer:	Anny
Custom	X51RL	Rev	2.0
Date:	Monday, May 21, 2007	Sheet	87 of 88

<< Kennedy_Zhang >>