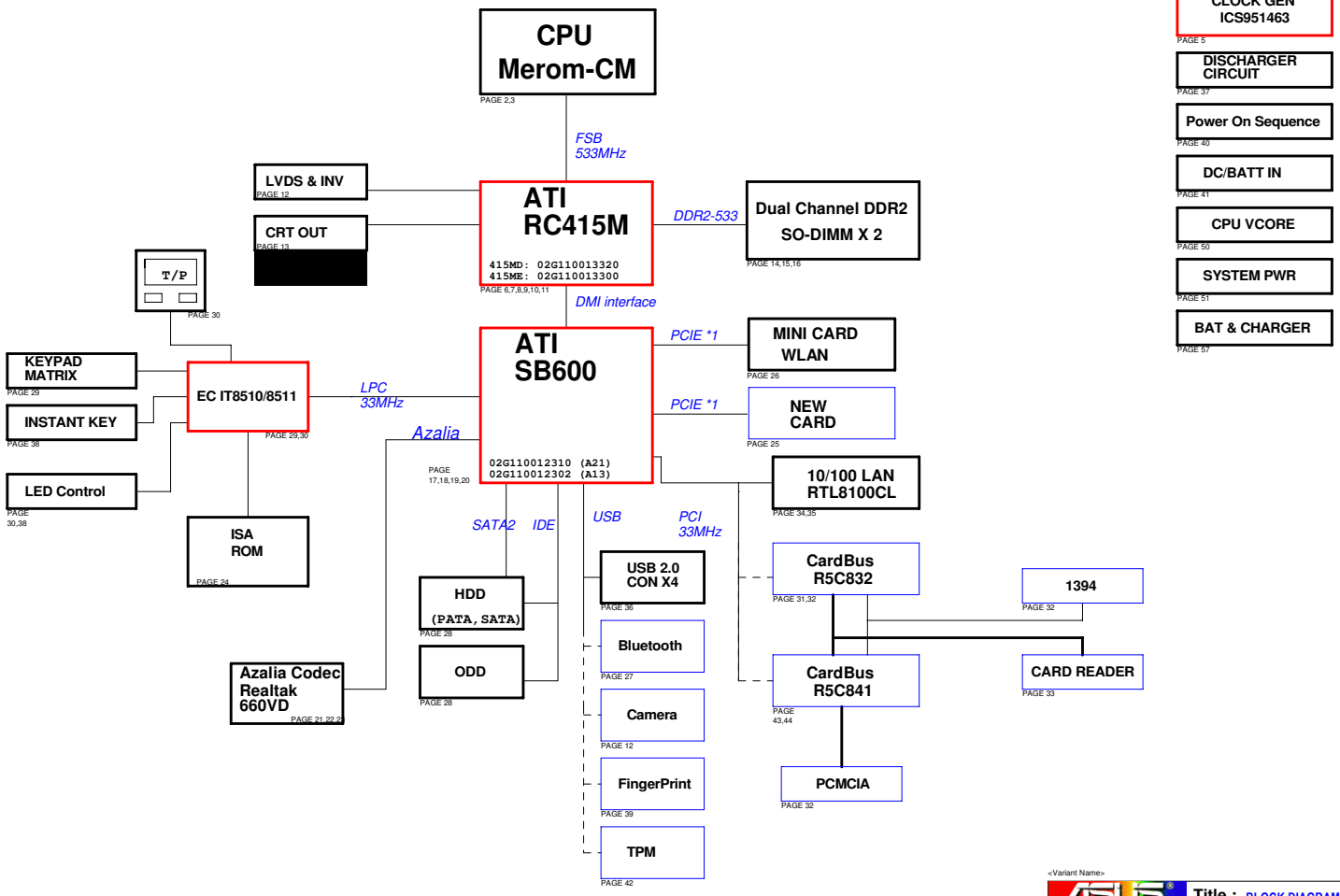
X51RL Serier Block Diagram



<Variant Name>

Title : BLOCK DIAGRAM

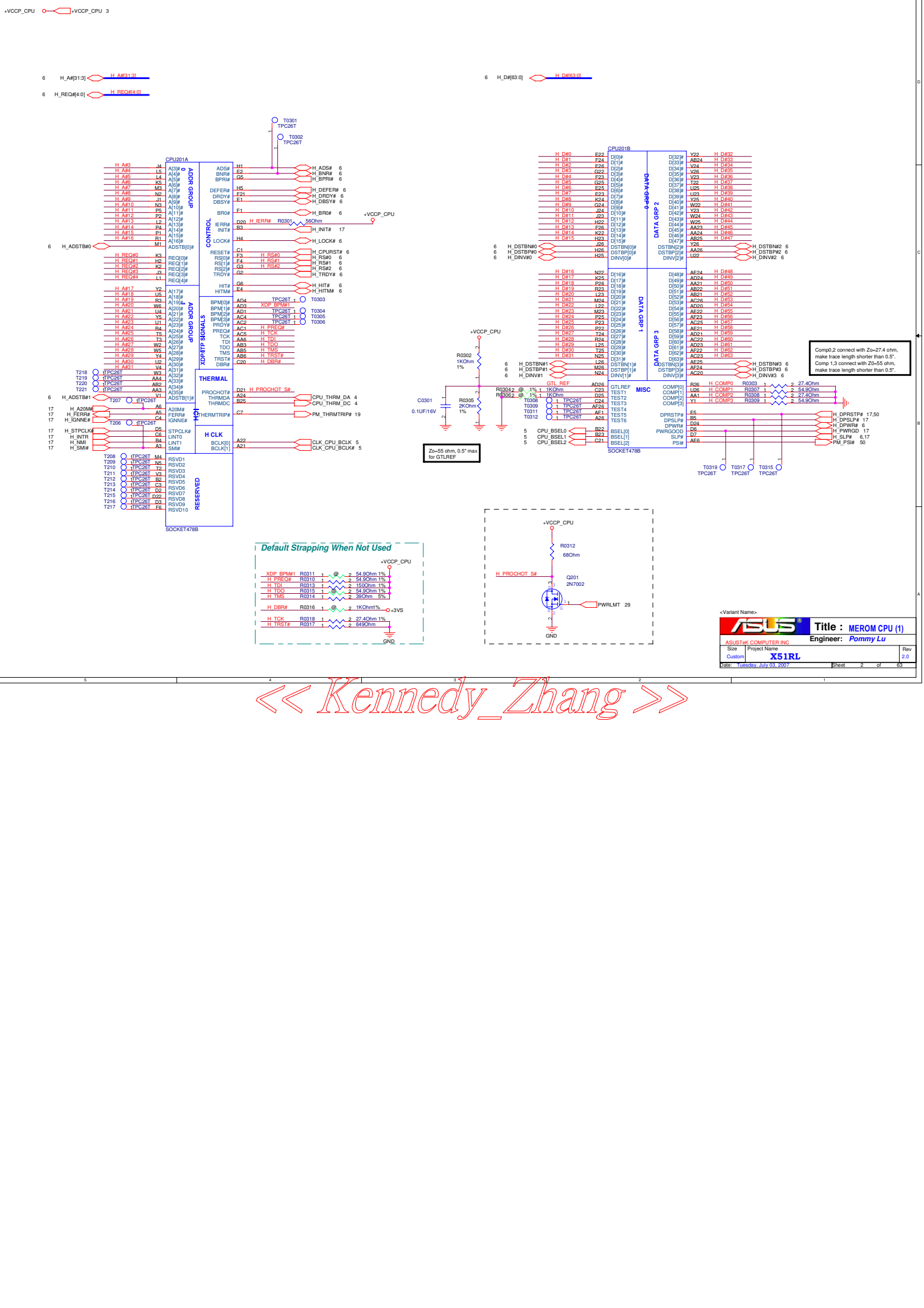
ASUSTeK COMPUTER INC

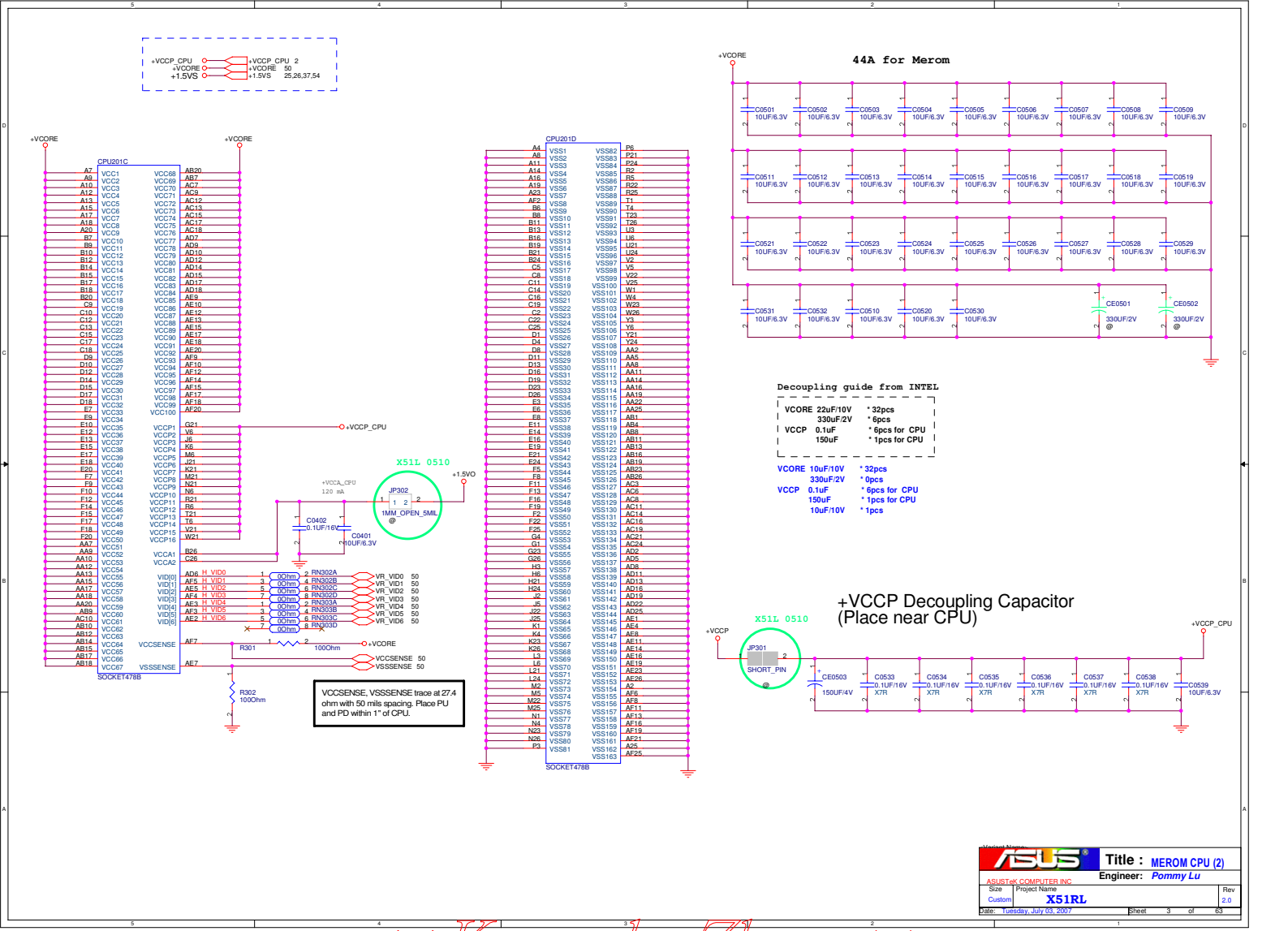
Engineer: Pommy Lu

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Monday, August 06, 2007 Sheet 1 of 63

<< Kennedy_Zhang >>





<< Kennedy_Zhang >>

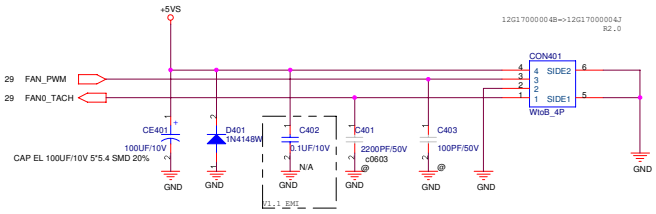
+5VS
+3VS

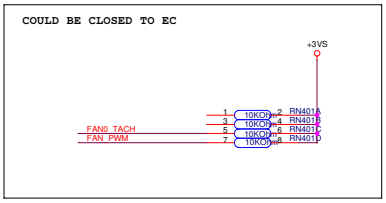
+5VS 13,20,22,23,28,29,30,37,38,50,61
+3VS 2,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61

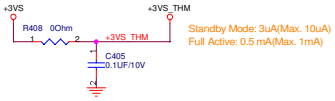
Fan Speed Control

KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3



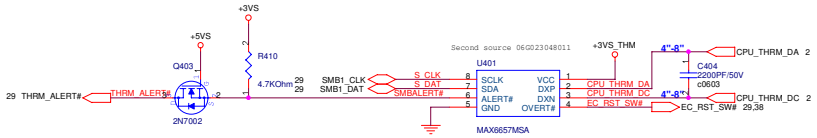




Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
=========H_THERMDA(10 mils)
10 mils
=========H_THERMDC(10 mils)
10 mils
=========GND
12 mils
----------OTHER SIGNALS

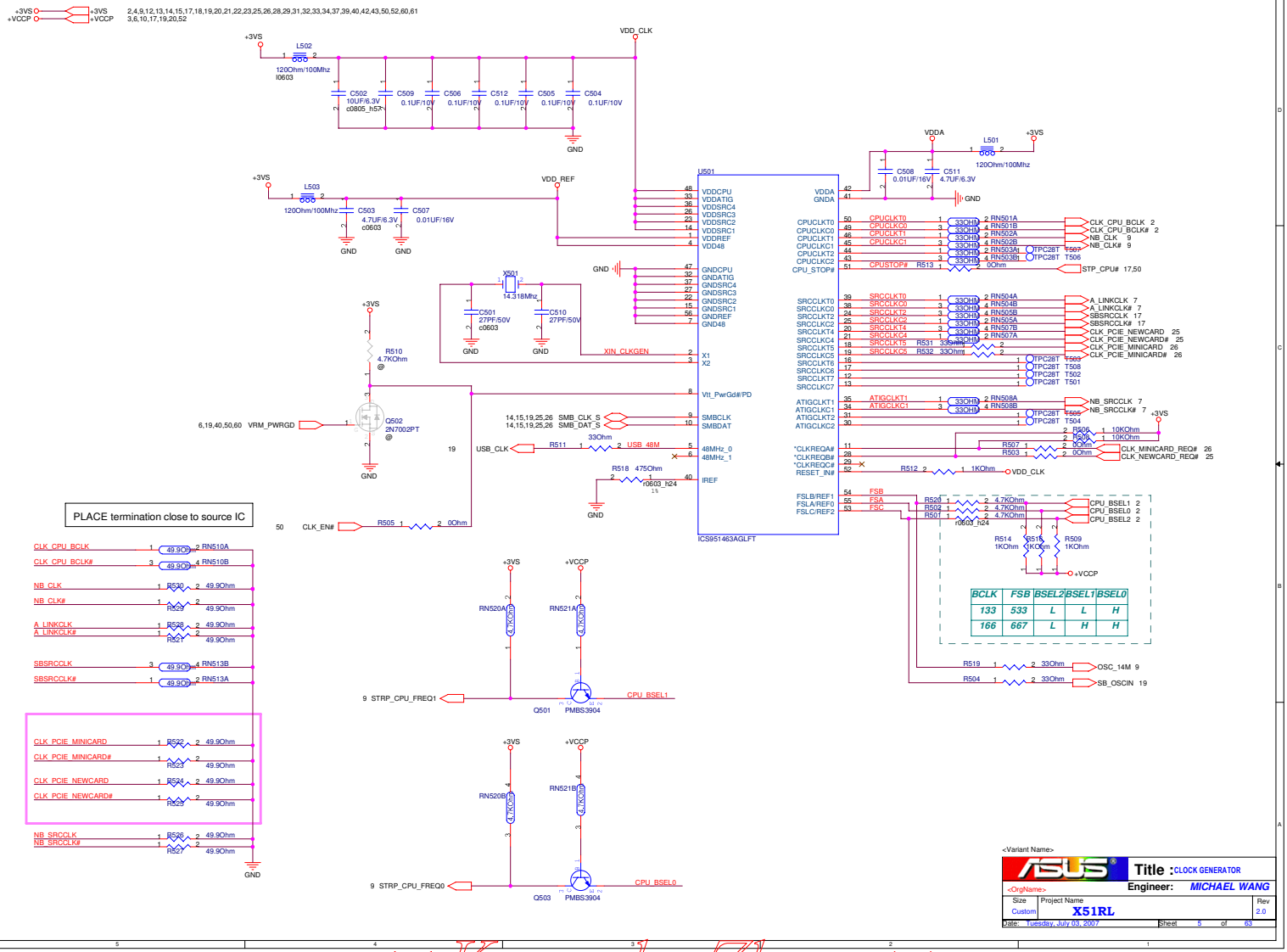
Avoid BPSB,Power



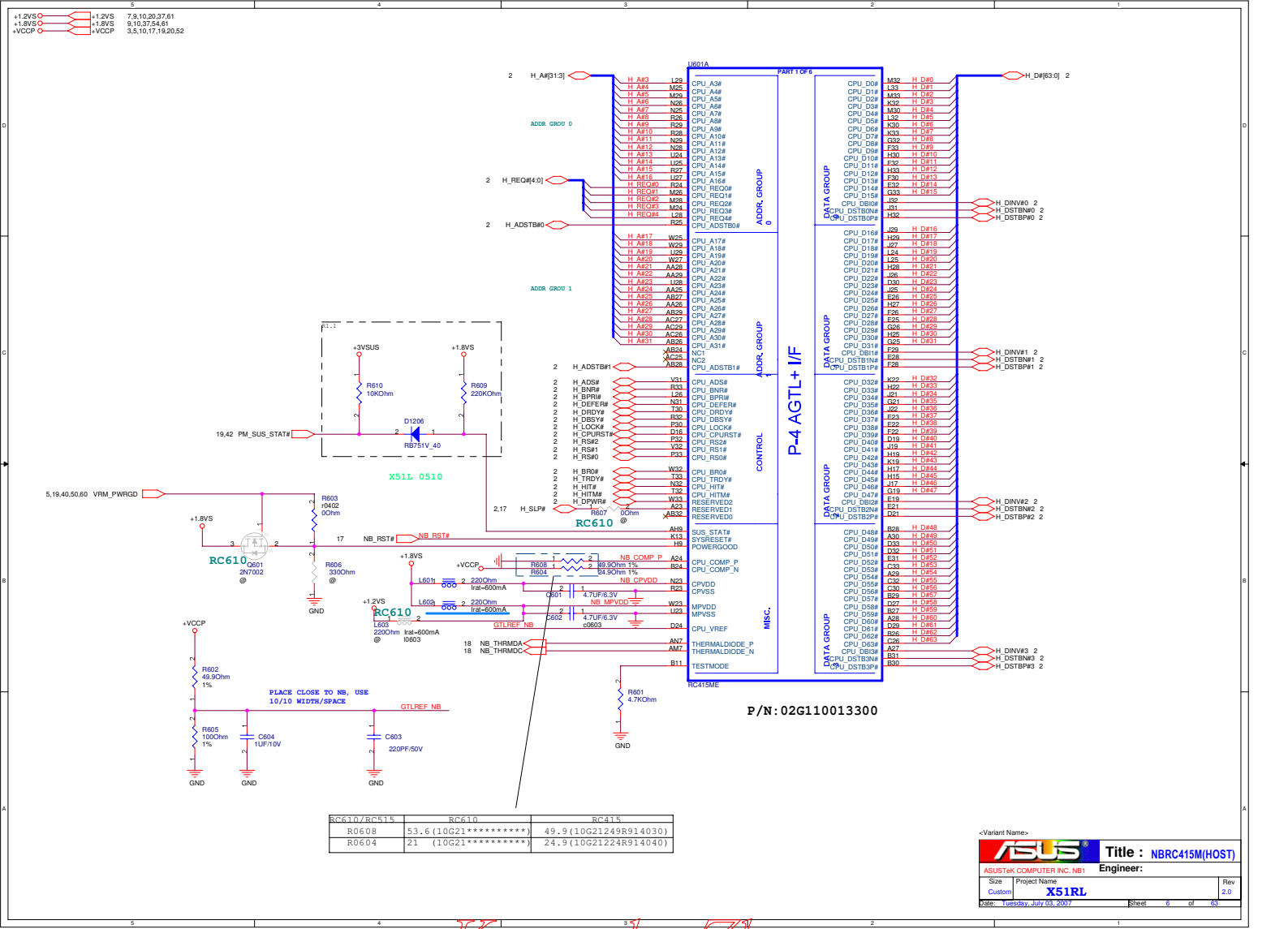
<Variant Name>

Title :	THER-SENSOR,FAN	
Engineer:	MICHAEL WANG	
ASUSTeK COMPUTER INC		
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 4 of 63	

<< Kennedy_Zhang >>



<< Kennedy_Zhang >>



P/N:02G110013300

RC610/RC515	RC610	RC415
R0608	53.6(10G21**********)	49.9(10G21249R914030)
R0604	21 (10G21**********)	24.9(10G21224R914040)

<Variant Name>

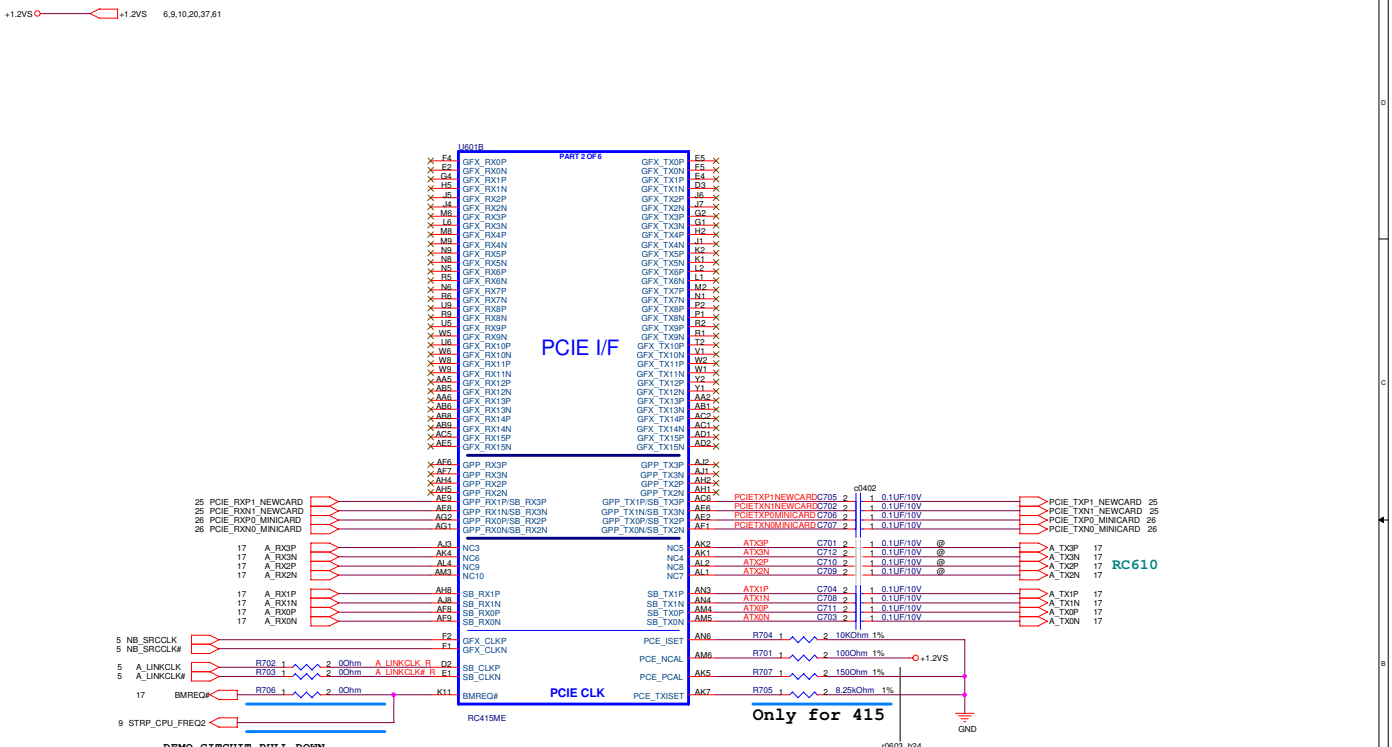
Title : NBRC415M(HOST)

ASUSTeK COMPUTER INC. NB1 Engineer:

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 6 of 63

<< Kennedy_Zhang >>



RC610/RC515	RC610	RC415
R0704	1.47K(10G21**********)	10K(10G213100213030)
R0701	2K (10G21**********)	100(10G213100013010)
R0707	562 (10G21**********)	150(10G213150013030)

<Variant Name>

ASUSTeK COMPUTER INC. NB1

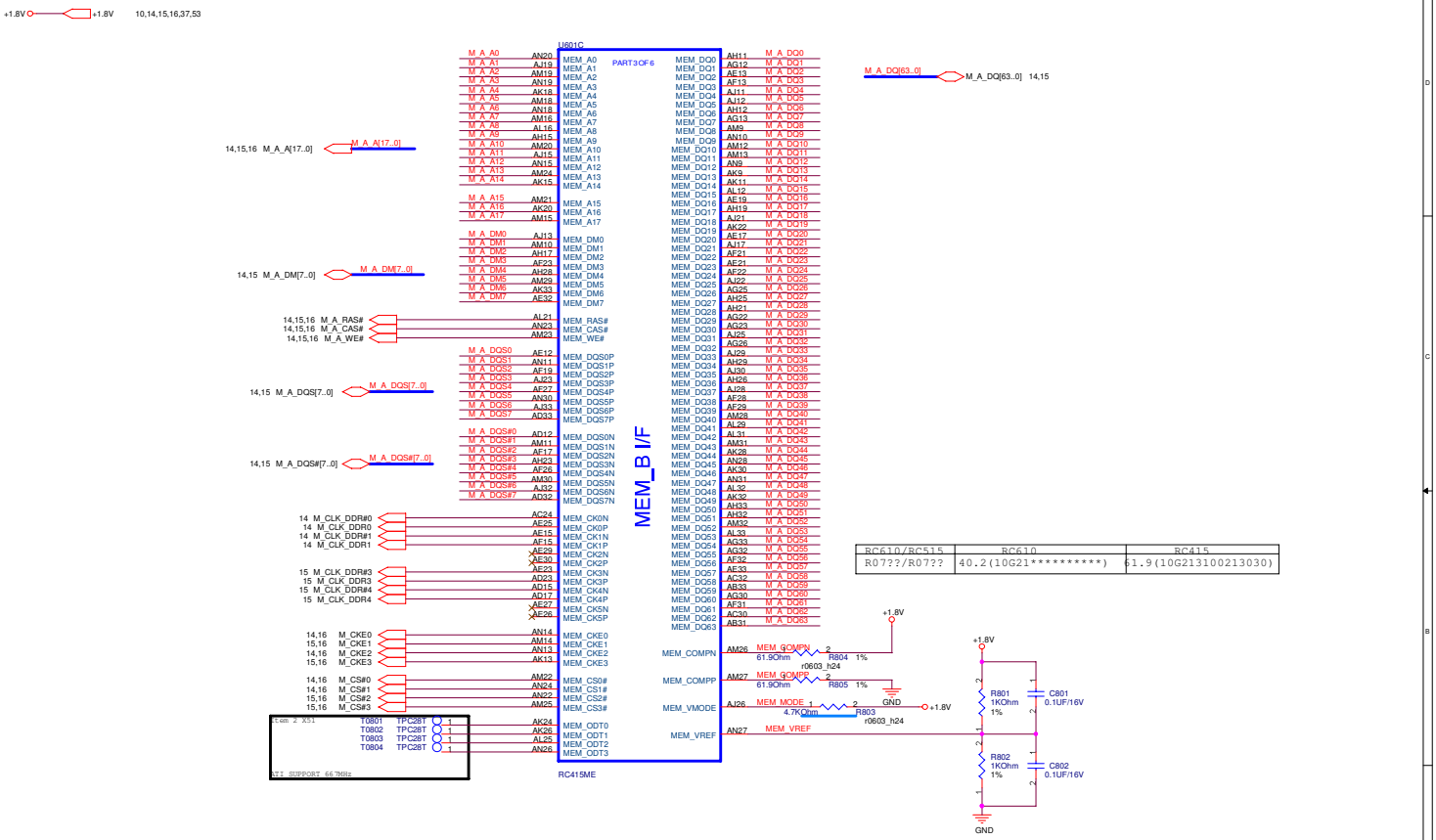
Title : NB-945PM(DMI & CFG)

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 7 of 63

<< Kennedy_Zhang >>

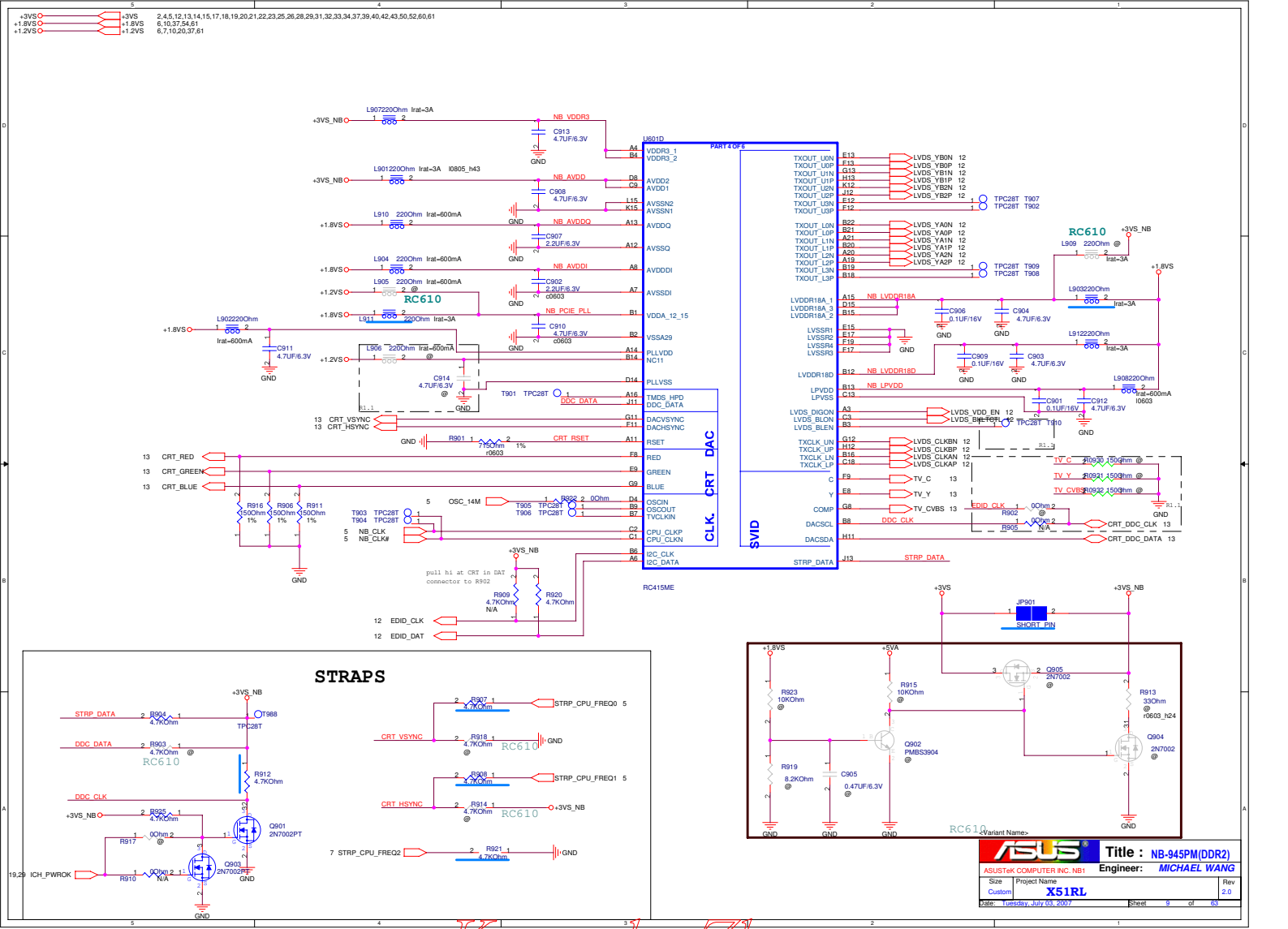


RC610/RC515	RC610	RC415
R07??/R07??	40.2(10G21*********)	61.9(10G213100213030)

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : NB_945PM(PCI-E)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 8 of 63	

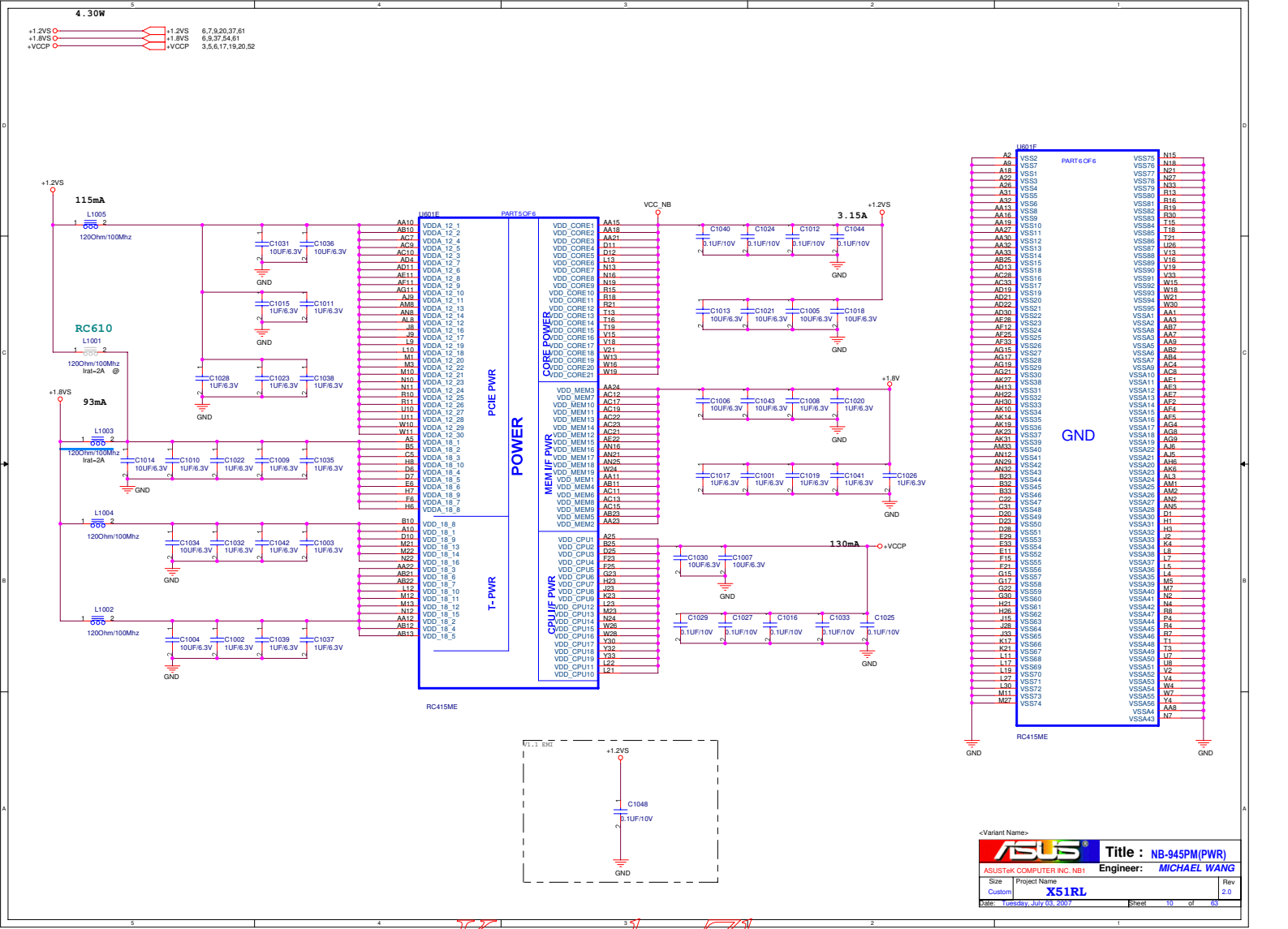
<< Kennedy_Zhang >>



STRAPS

ASUSTeK COMPUTER INC. NB1	Title : NB-945PM(DDR2)		
	Engineer: MICHAEL WANG		
Size: Custom	Project Name: X51RL		Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 9 of 63		

<< Kennedy_Zhang >>



<Variant Name>

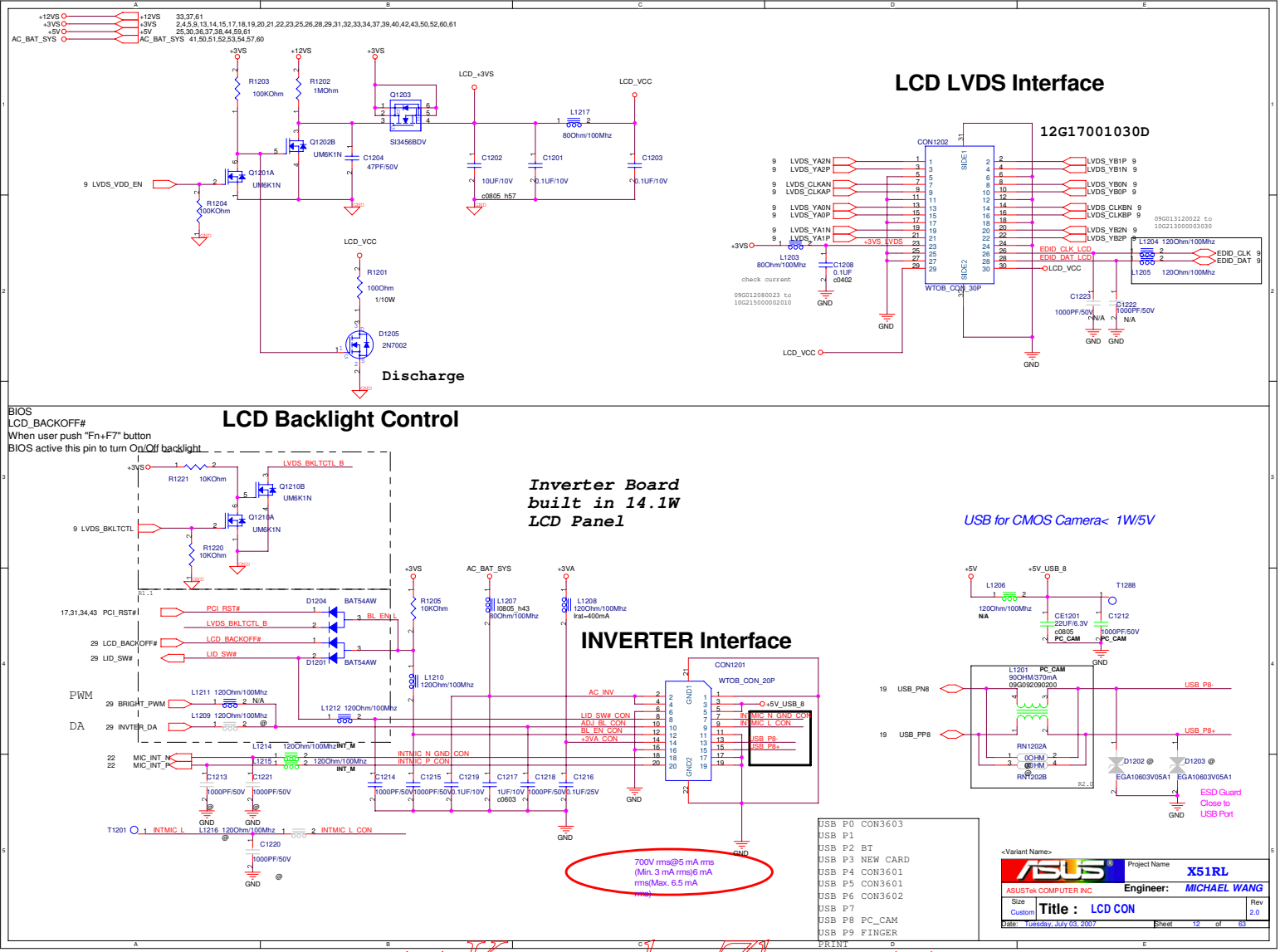
Title : HISTORY

ASUSTeK COMPUTER INC

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Wednesday, May 16, 2007 Sheet 11 of 63



BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER
PRINT

<Variant Name>

ASUSTek COMPUTER INC	Project Name	X51RL
	Engineer:	MICHAEL WANG
Size: Custom	Title : LCD CON	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 12 of 63	

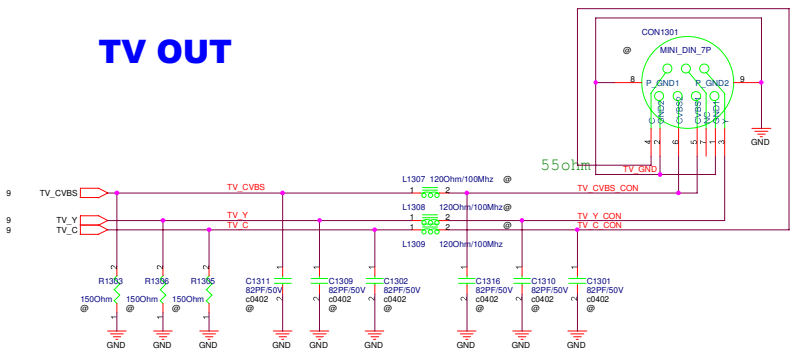
<< Kennedy_Zhang >>

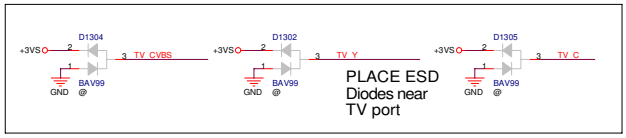
+5VS
+3VS
+5VS
+3VS
4,20,22,23,28,29,30,37,38,50,61
2,4,5,9,12,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61

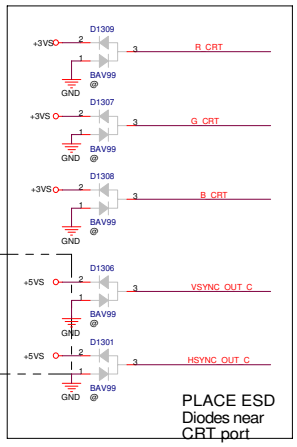
12G101102152
=>12G10110215A
R2.0

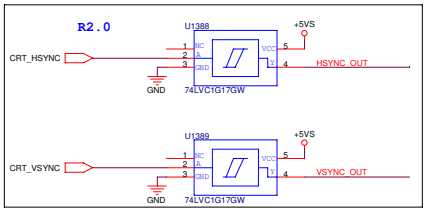
12G141011076

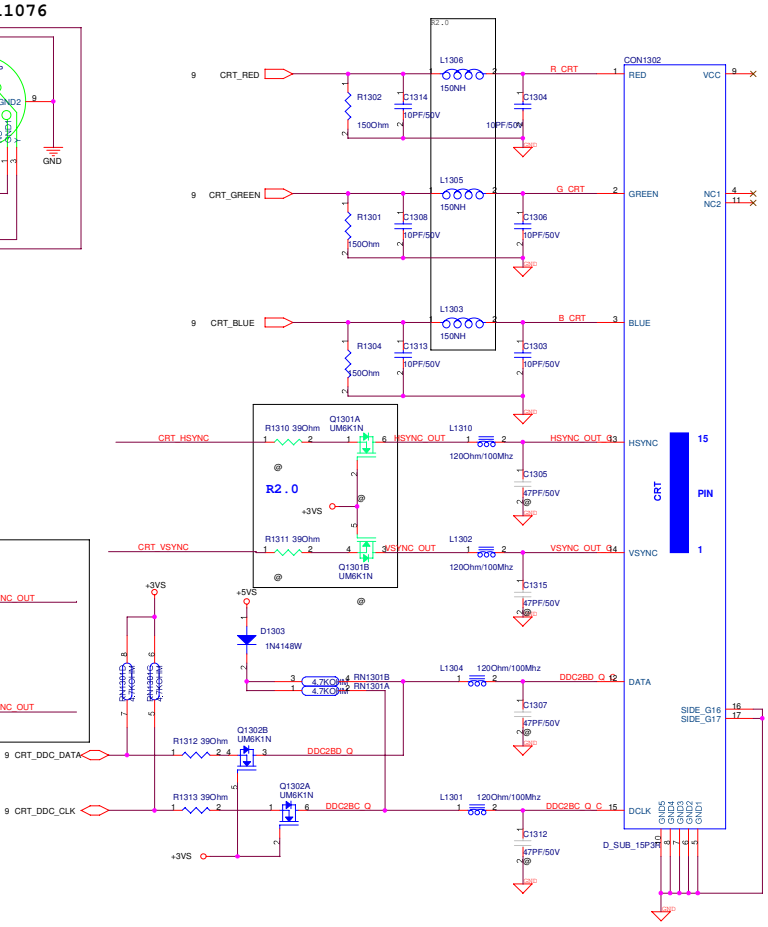
TV OUT











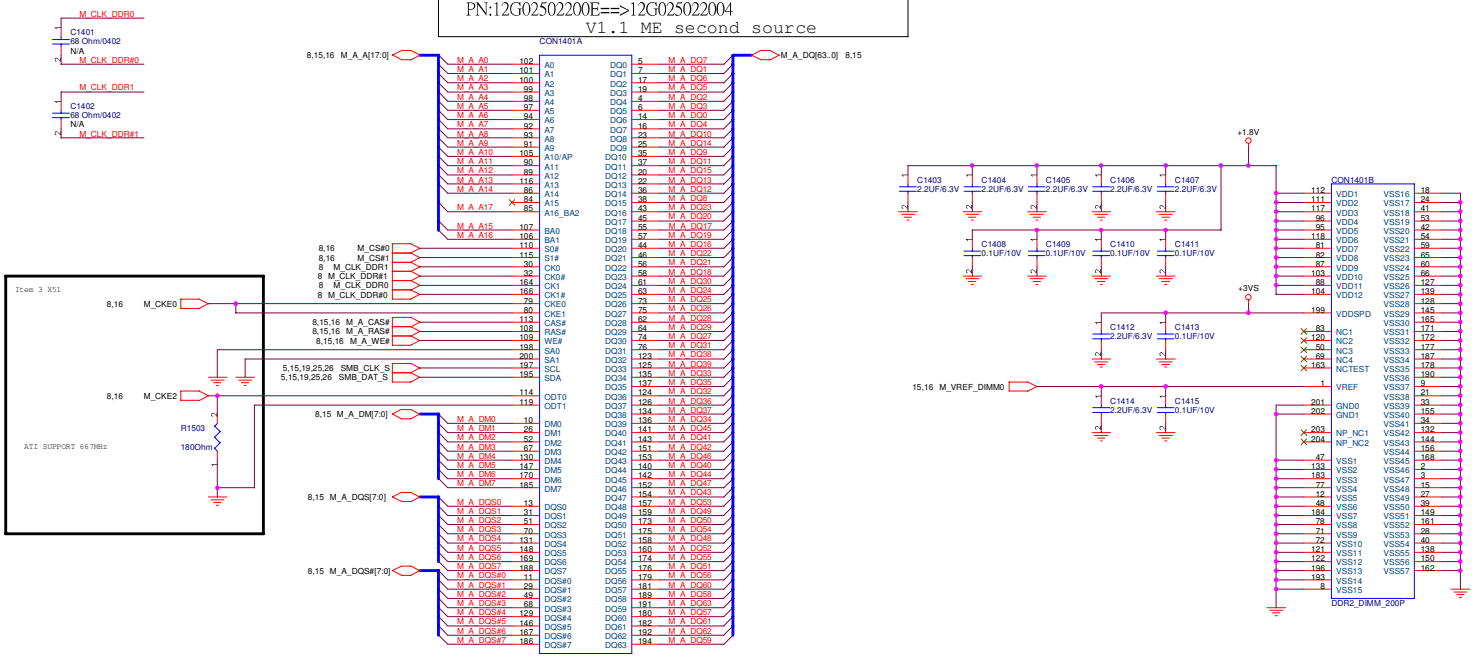
<Variant Name>

ASUSTek COMPUTER INC	Project Name	X51RL
	Engineer:	MICHAEL WANG
Size: Custom	Title : CRT PORT	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 13 of 63	

+3VS +1.8V → +3VS +1.8V 2,4,5,9,12,13,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
8,10,15,16,37,53

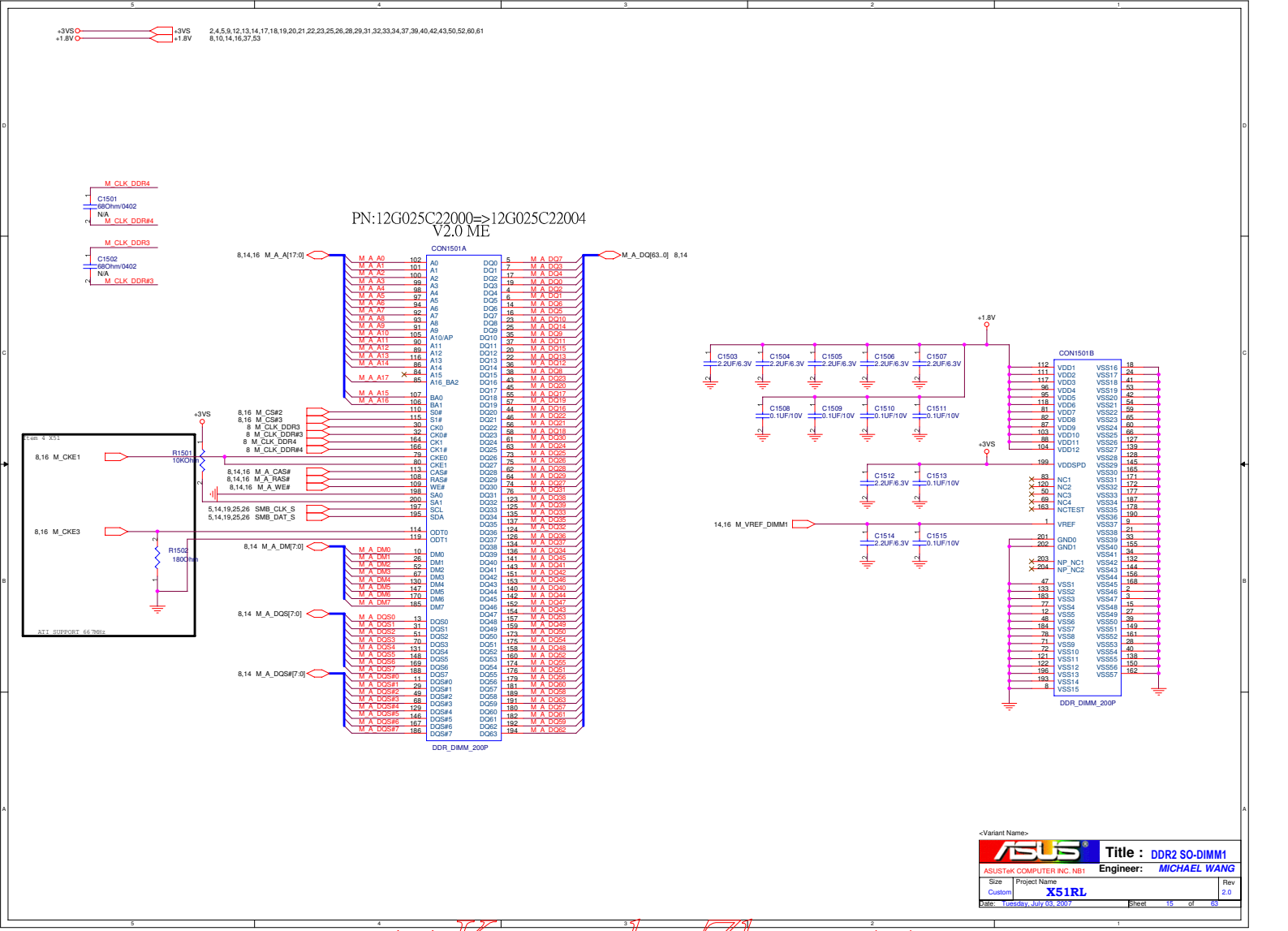
FRON

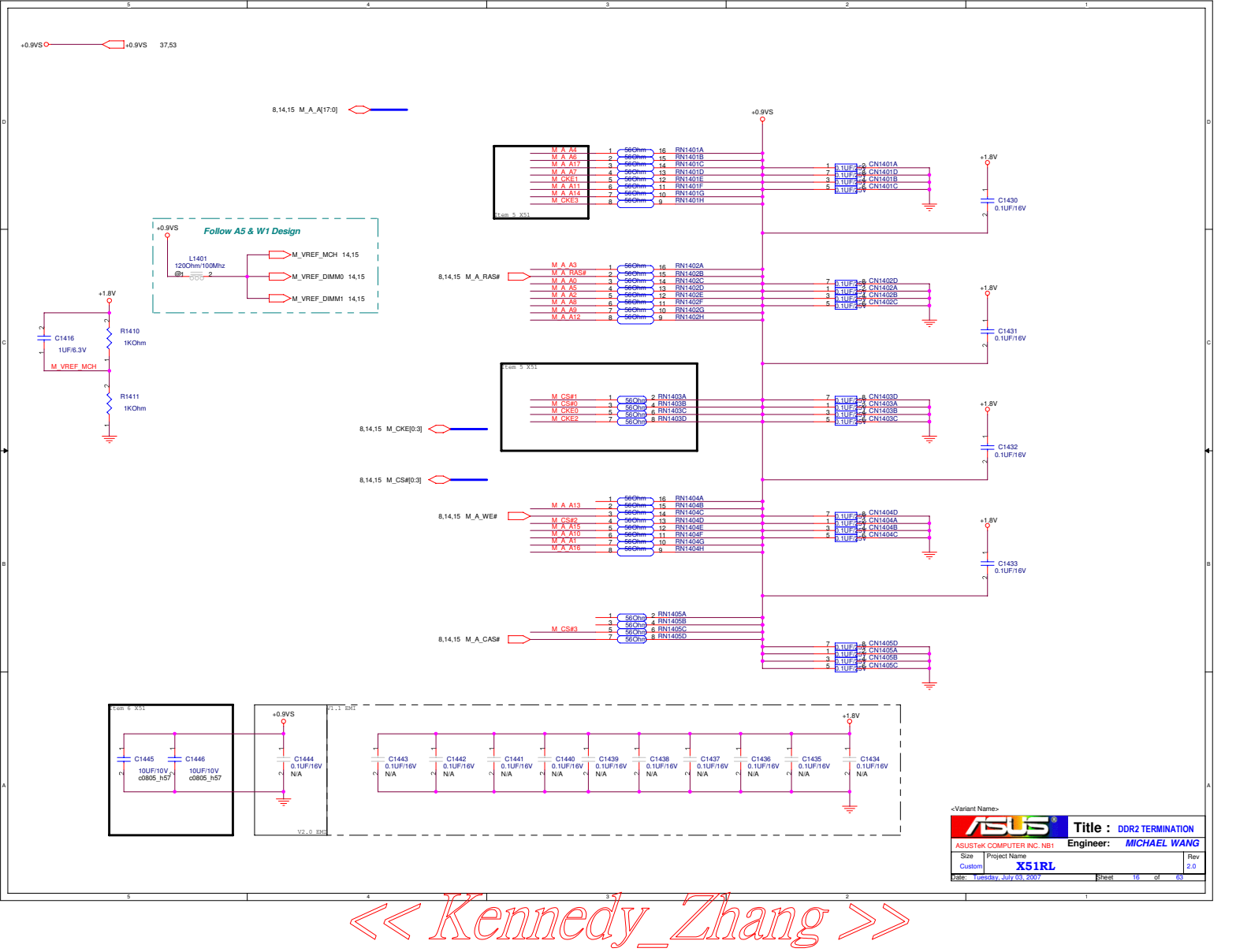
PN:12G02502200E==>12G025022004
V1.1 ME second source

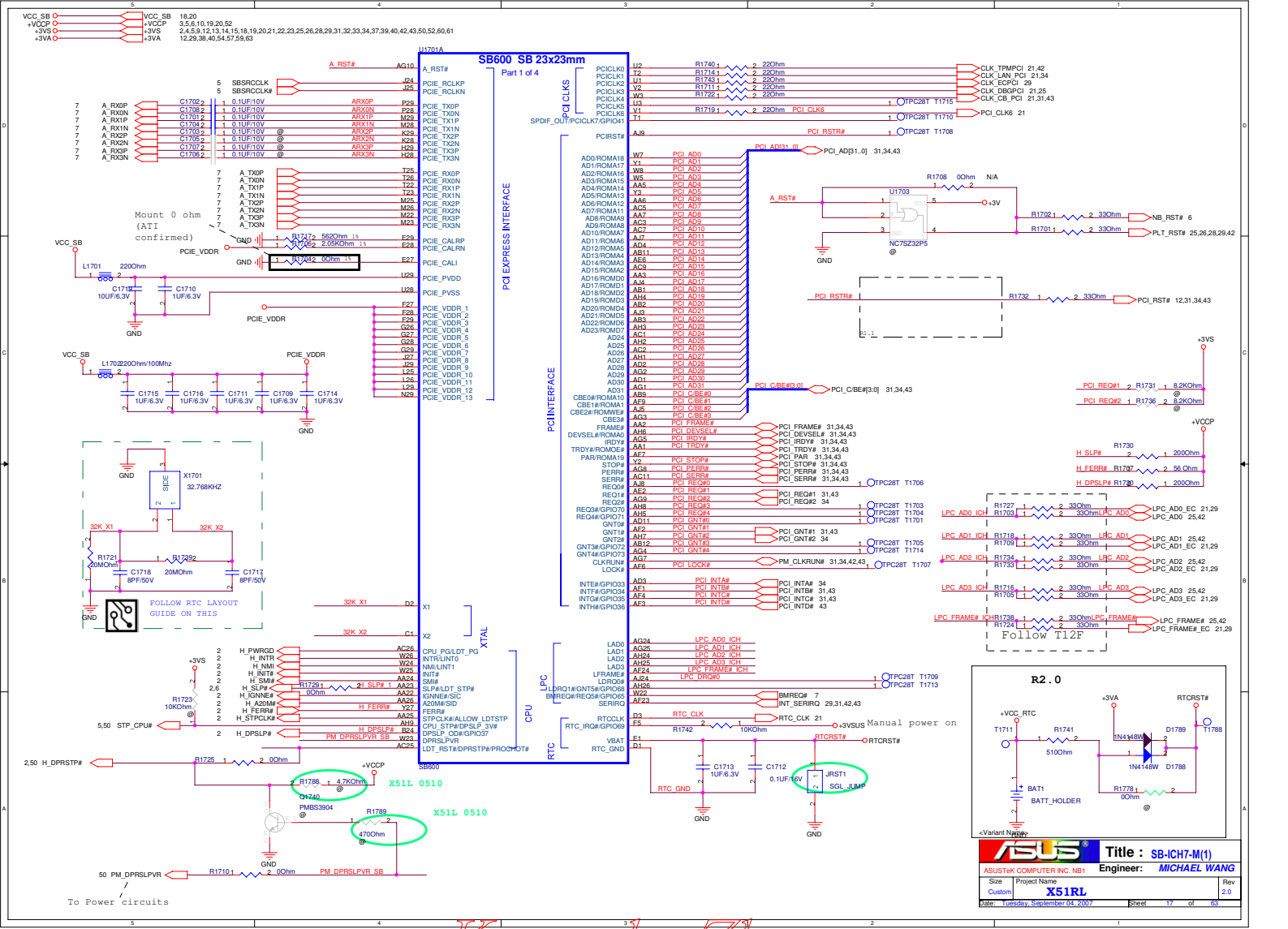


<Variant Name>

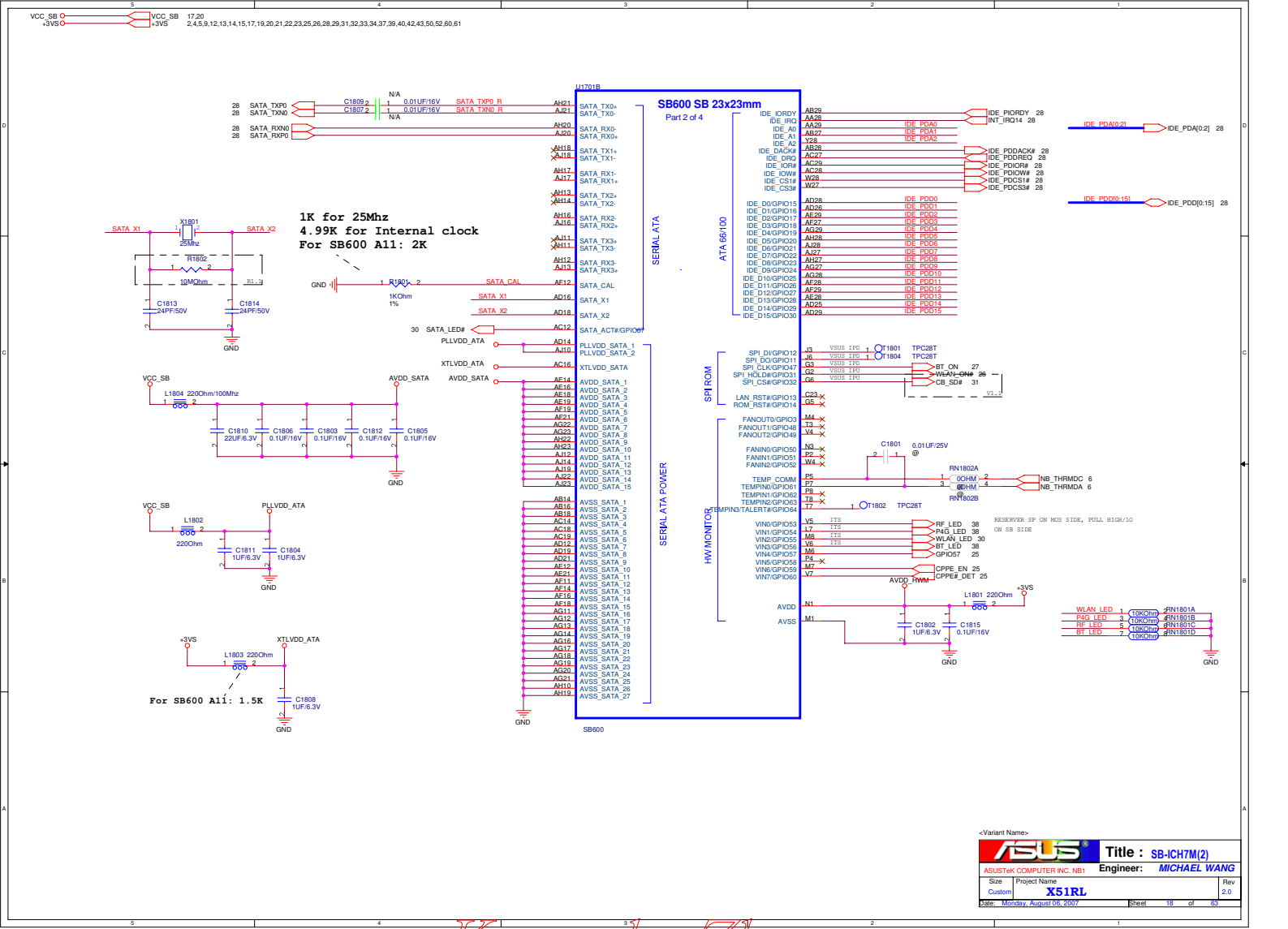
ASUSTeK COMPUTER INC. NB1	Title : DDR2 SO-DIMM1	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 14 of 63	





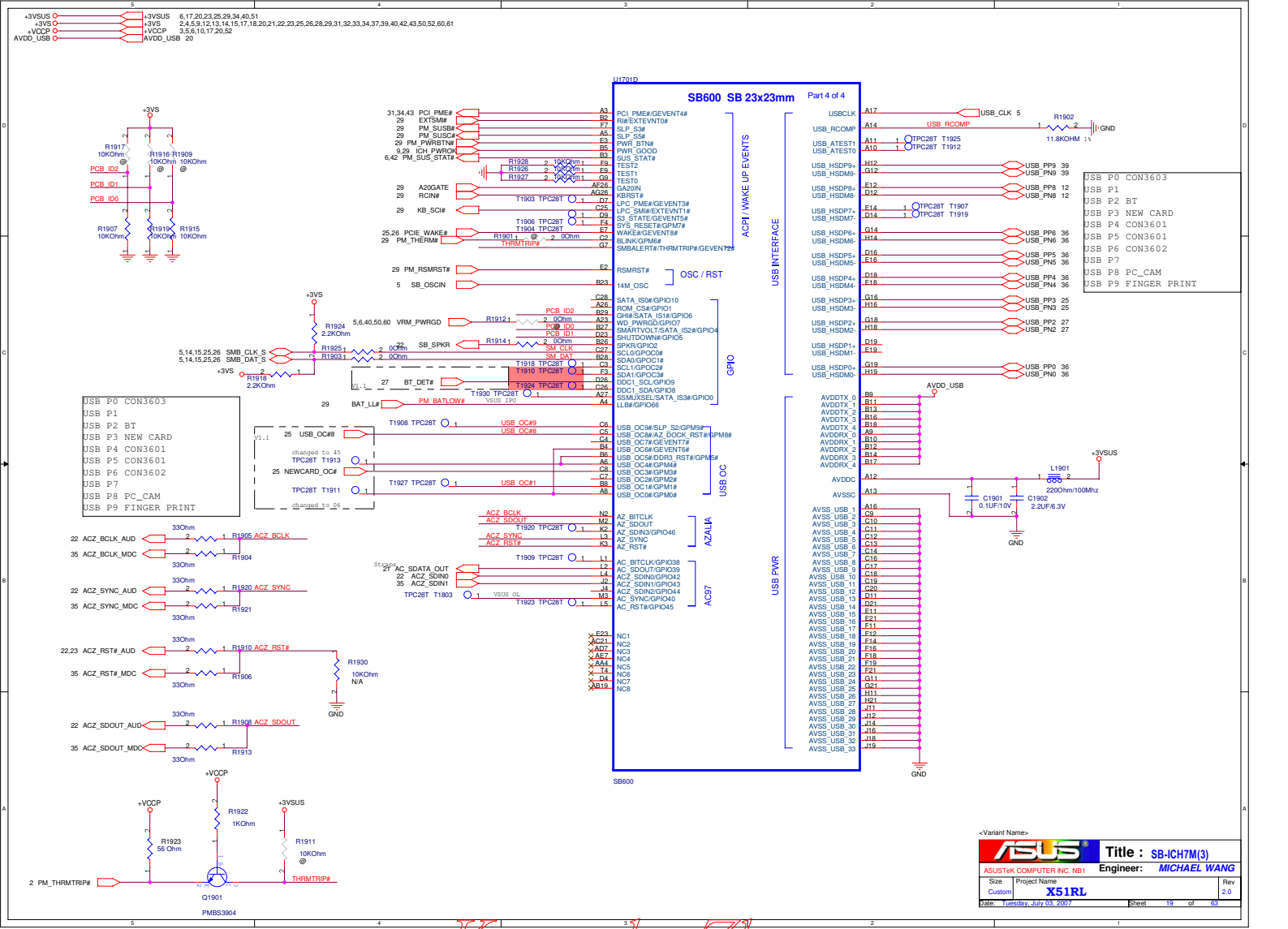


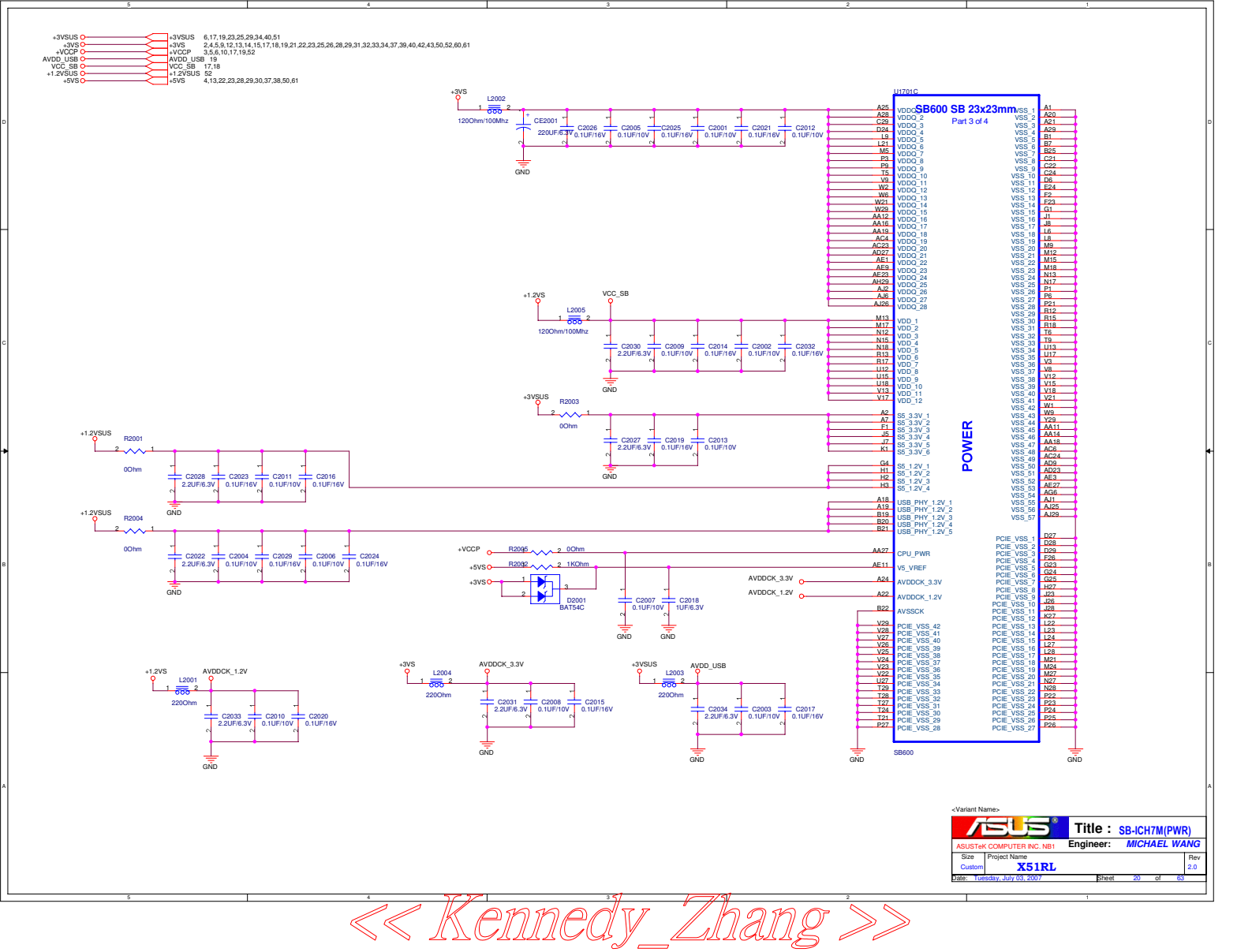
<< Kennedy_Zhang >>

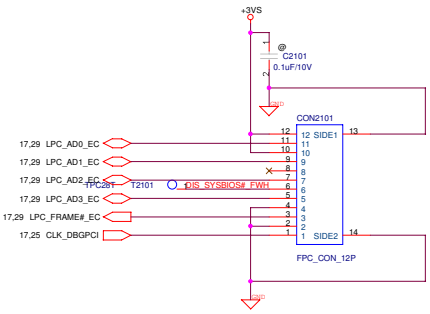


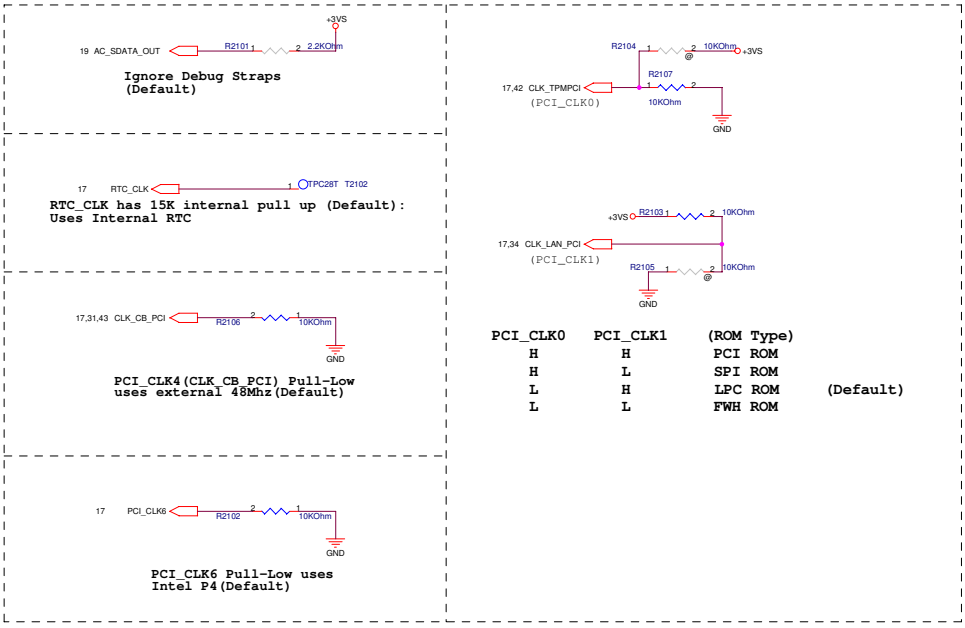
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : SB-ICH7M(2)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Monday, August 06, 2007	Sheet 18 of 63	









PCI_CLK0	PCI_CLK1	(ROM Type)	
H	H	PCI ROM	
H	L	SPI ROM	
L	H	LPC ROM	(Default)
L	L	FWH ROM	

<Variant Name>

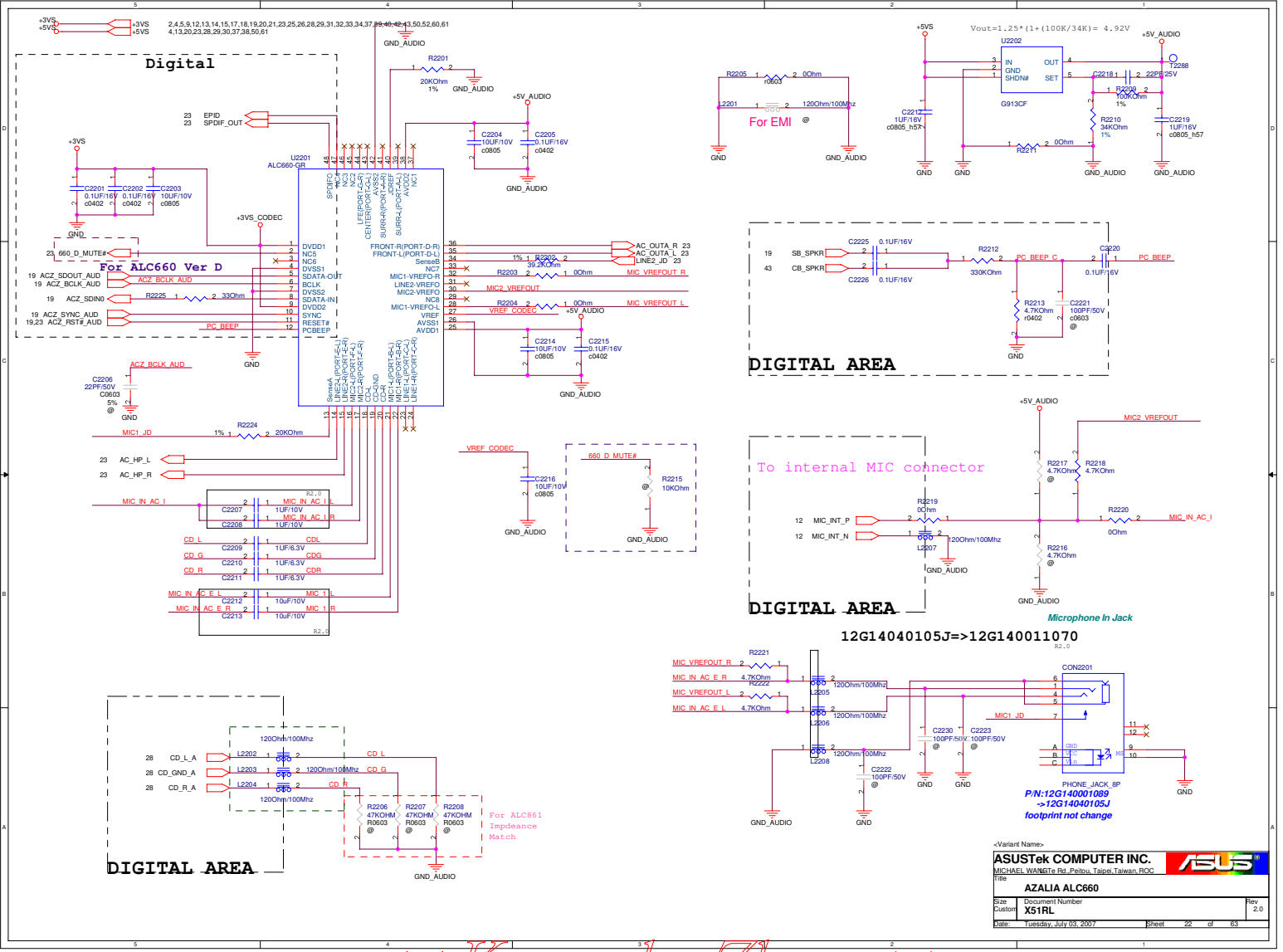
Title : BLOCK DIAGRAM

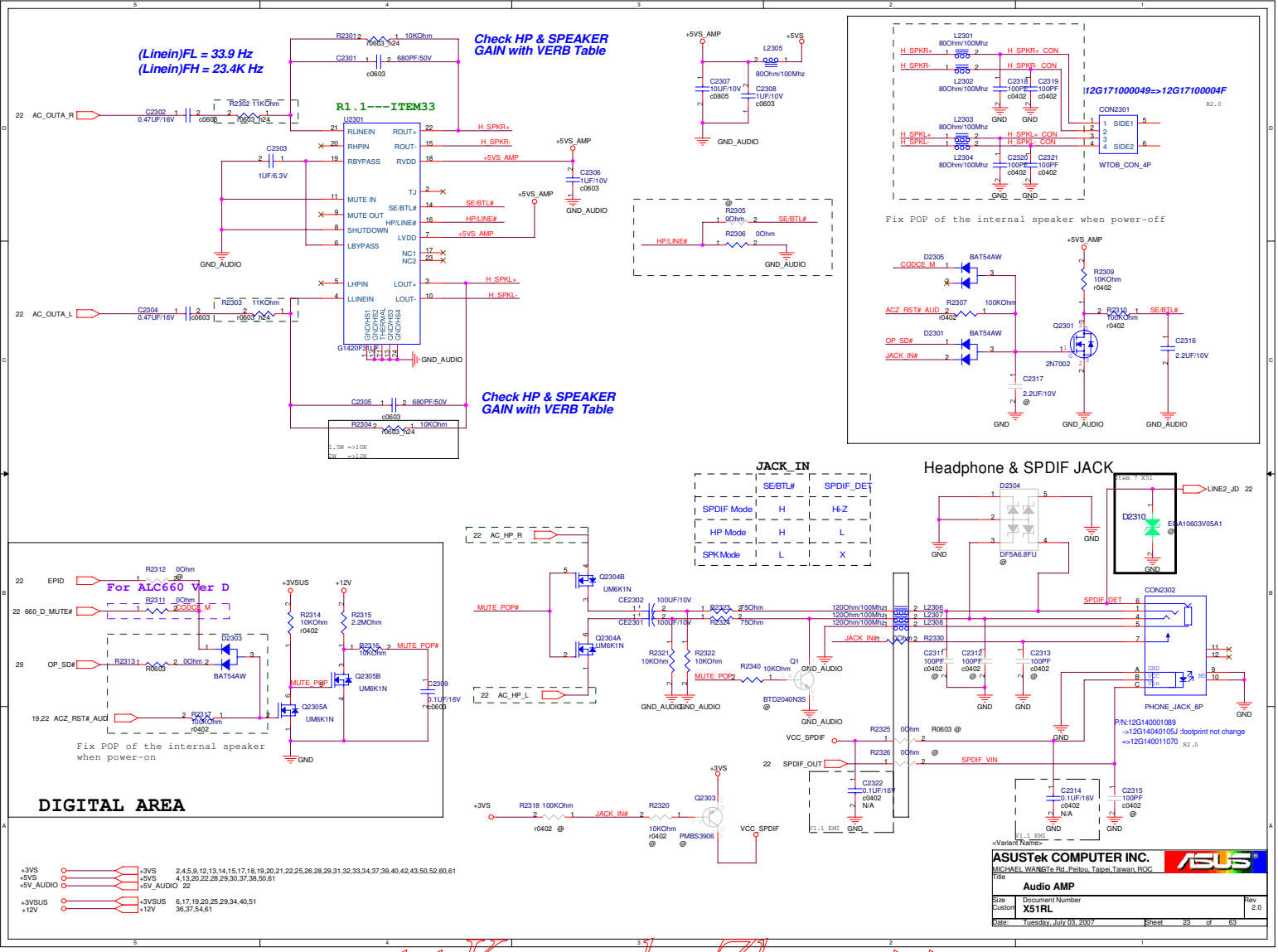
<OrgName> Engineer:

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 21 of 63

<< Kennedy_Zhang >>



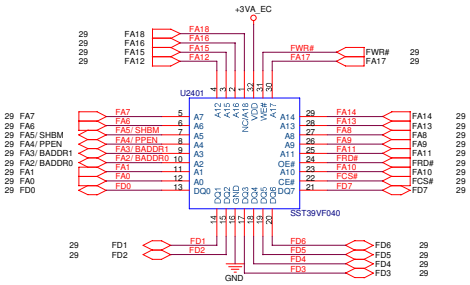


<< Kennedy_Zhang >>

+3VA_EC +3VA_EC 26,29

ISA ROM

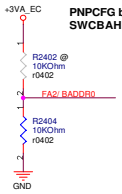
0.01A

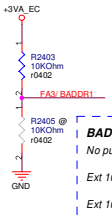


EC Hardware Strap

Strap value sampled after VSTBY power up reset

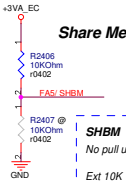
PNPCFG base address set by SWCBAHR/SWCBALR





BADDR[1:0]

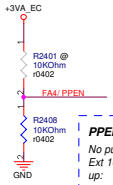
No pull up:	*The register pair to access PNPCFG is 002Eh and 002Fh.*
Ext 10K up on BADDR0:	*The register pair to access PNPCFG is 004Eh and 004Fh.*
Ext 10K up on BADDR1:	*The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.*



Share Memory

SHBM

No pull up:	*Disable shared memory with host BIOS*
Ext 10K up:	*Enable shared memory with host BIOS*

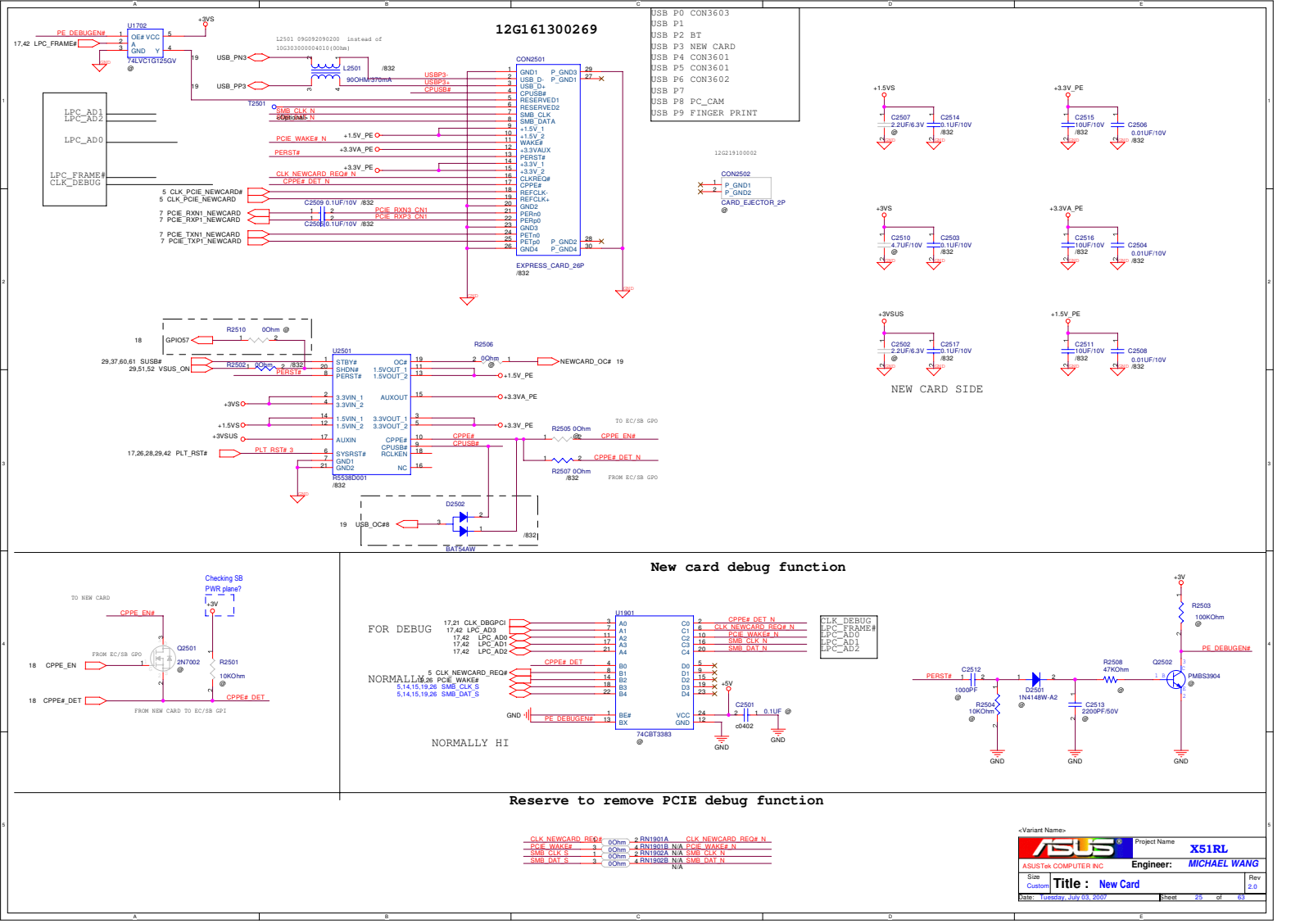


PPEN

No pull up:	*Normal*
Ext 10K up:	*KBS interface pins are switched to parallel port interface for in-system programming.*

<Variant Name>

ASUSTeK COMPUTER INC	Title : ISA ROM	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 24 of 63	



New card debug function

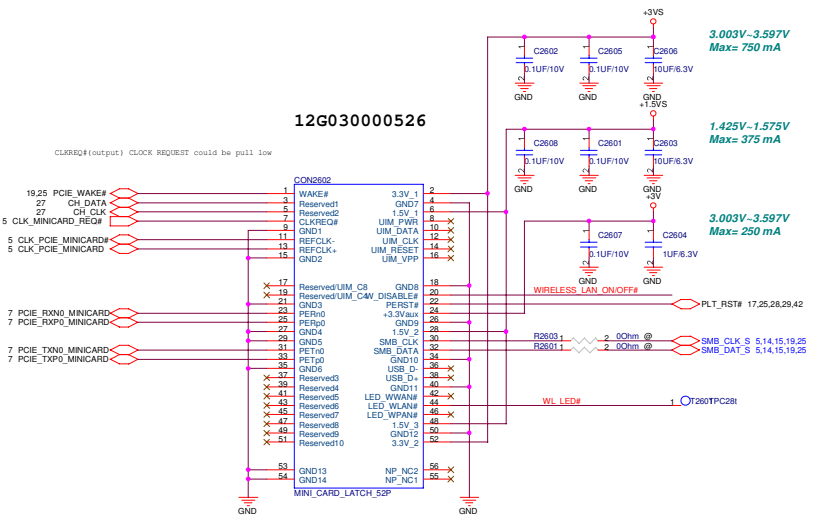
Reserve to remove PCIE debug function

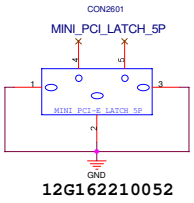
<Variant Name>

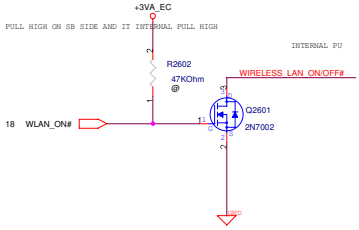
Project Name	X51RL
ASUSTek COMPUTER INC	Engineer: MICHAEL WANG
Size: Custom	Title : New Card
Rev	2.0
Date: Tuesday, July 03, 2007	Sheet 25 of 63

<< Kennedy_Zhang >>

+3V +3V 17,25,27,31,35,37,42,43,44,61
+3VS +3VS 2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61
+1.5VS +1.5VS 25,37,54
+3VA_EC +3VA_EC 24,29







<Variant Name>

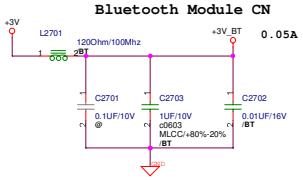
ASUSTek COMPUTER INC	Project Name: X51RL	
	Engineer: MICHAEL WANG	
Size: Custom	Title : MINI PCI	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 26 of 63	

<< Kennedy_Zhang >>

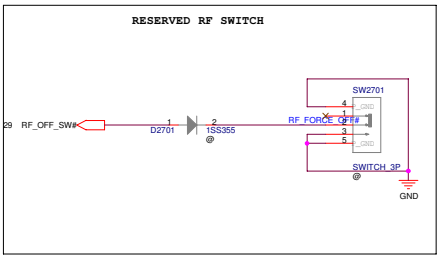
+3V +3V 17,25,26,31,35,37,42,43,44,61

For Bluetooth

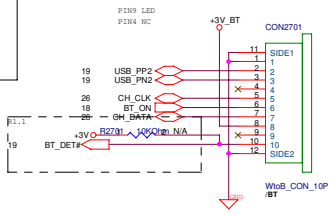
Bluetooth Module CN



RESERVED RF SWITCH



12G17101010L




```
USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER
PRINT
```

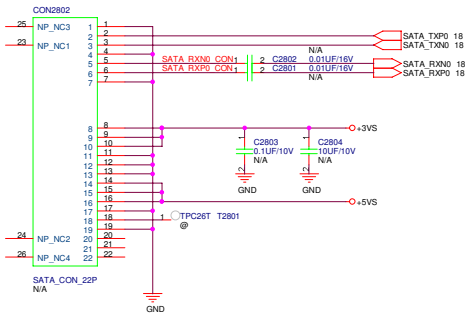
<Variant Name>

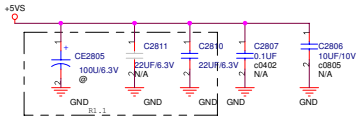
ASUSTeK COMPUTER INC	Title : Blue Tooth	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 27 of 63	

+3VS +3VS 2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,29,31,32,33,34,37,39,40,42,43,50,52,60,61
+5VS +5VS 4,13,20,22,23,29,30,37,38,50,61

SATA HDD

12G15100022F



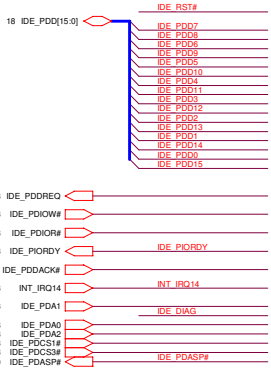


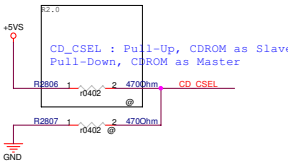
Item 8 X51

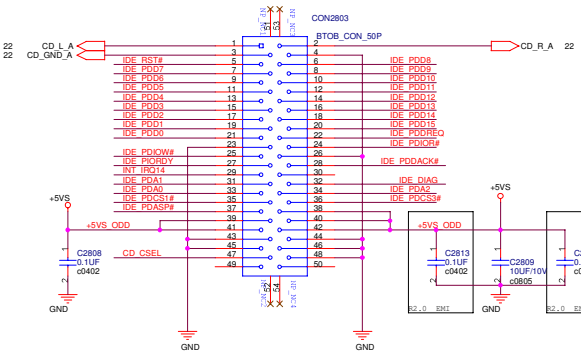
Dtlete PATA HDD

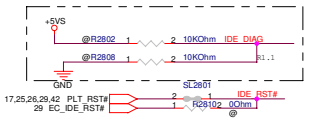
CD-ROM

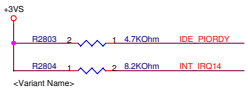
12G161210504







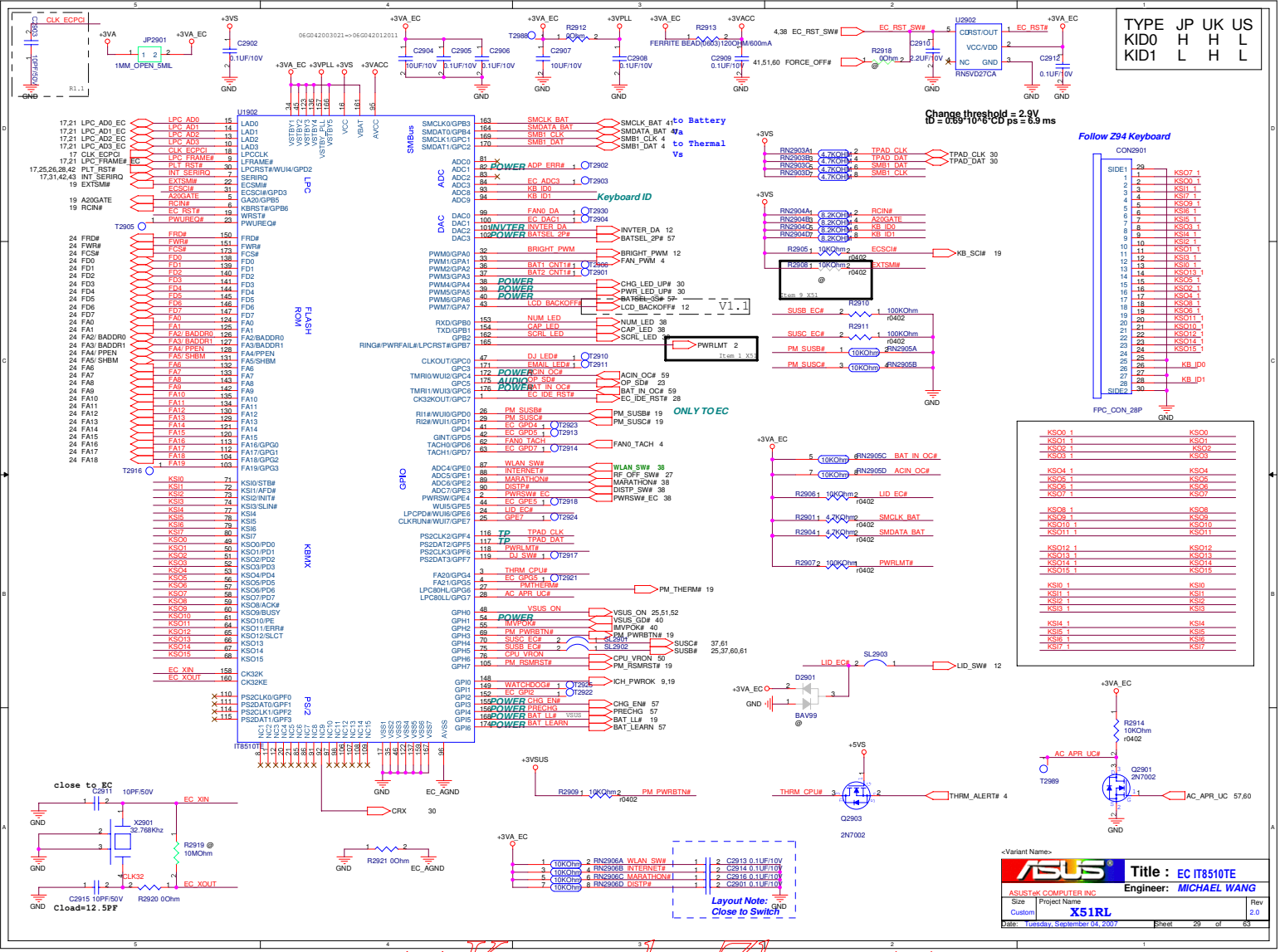




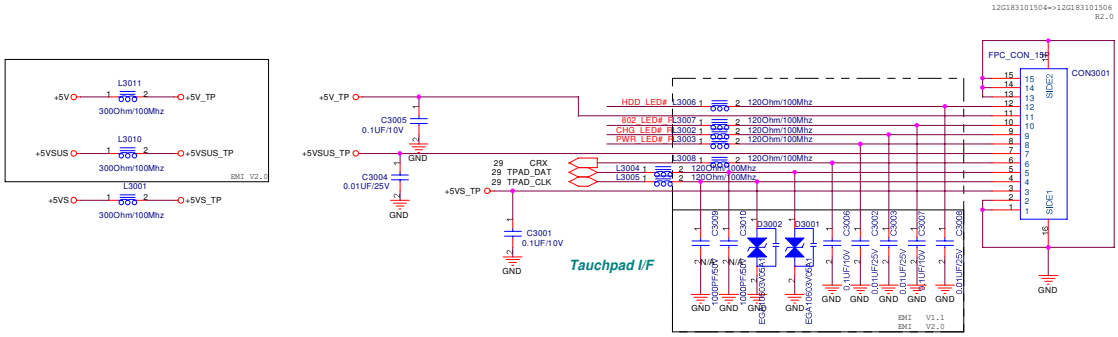
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : PATA-SATA & ODD	
	Engineer:	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Monday, August 06, 2007	Sheet 28 of 63	

<< Kennedy_Zhang >>



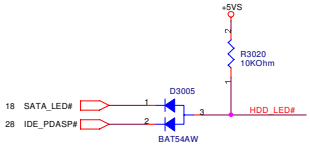
<< Kennedy_Zhang >>



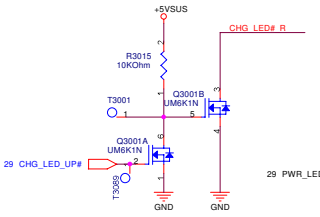
Touchpad

Tauchpad I/F

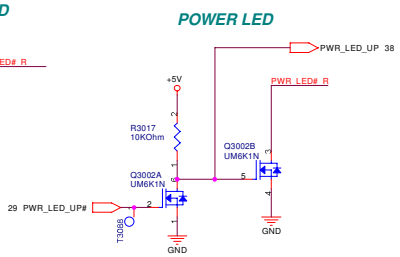
HDD LED



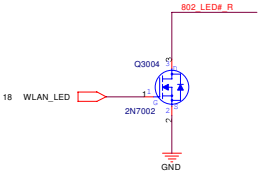
CHARGE LED



POWER LED



WLAN LED



<Variant Name>

ASUSTeK COMPUTER INC

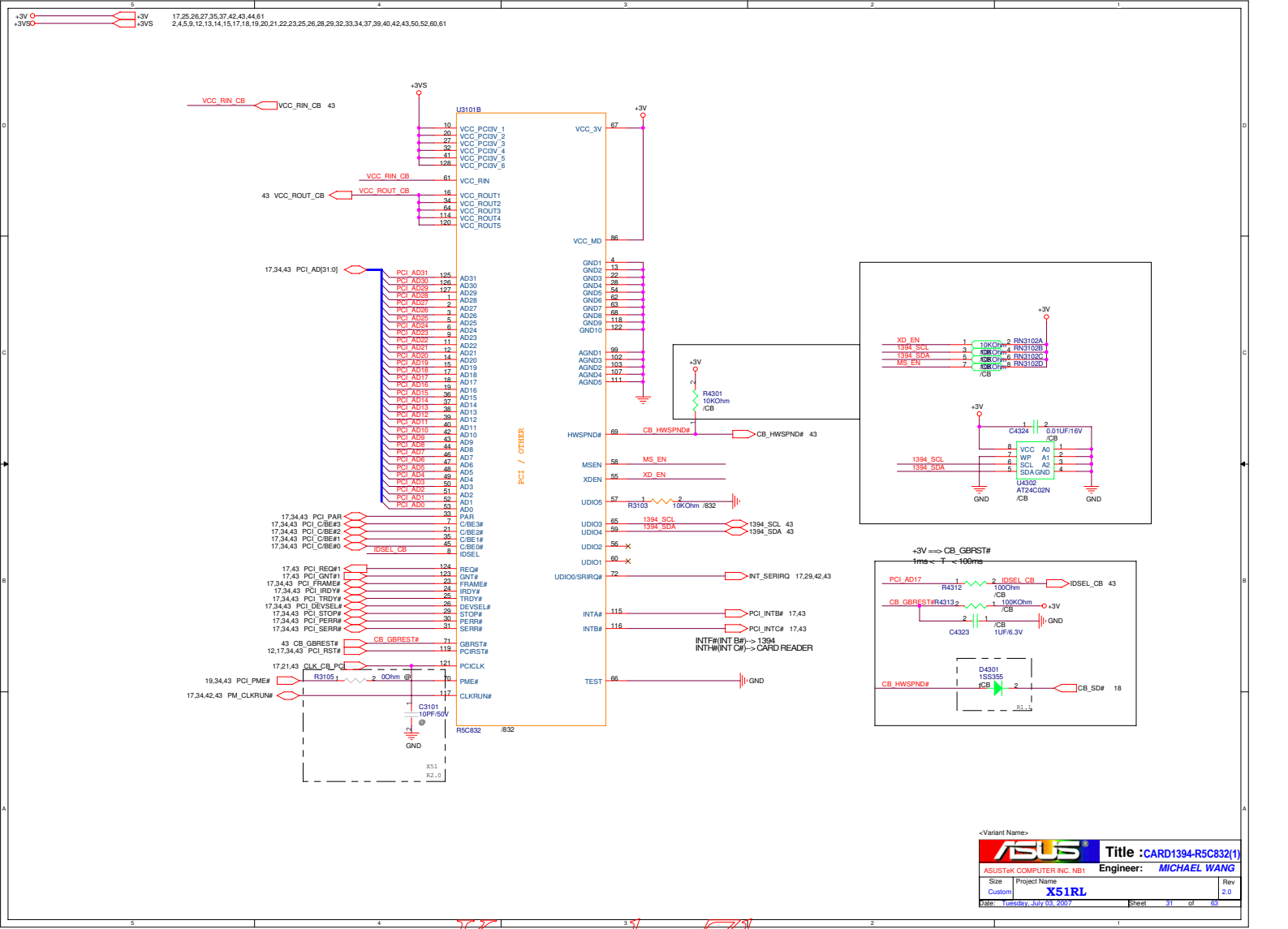
Title : EC IT8510TE(2/2)

Engineer: MICHAEL WANG

Size	Project Name	Rev
A3	X51RL	2.0

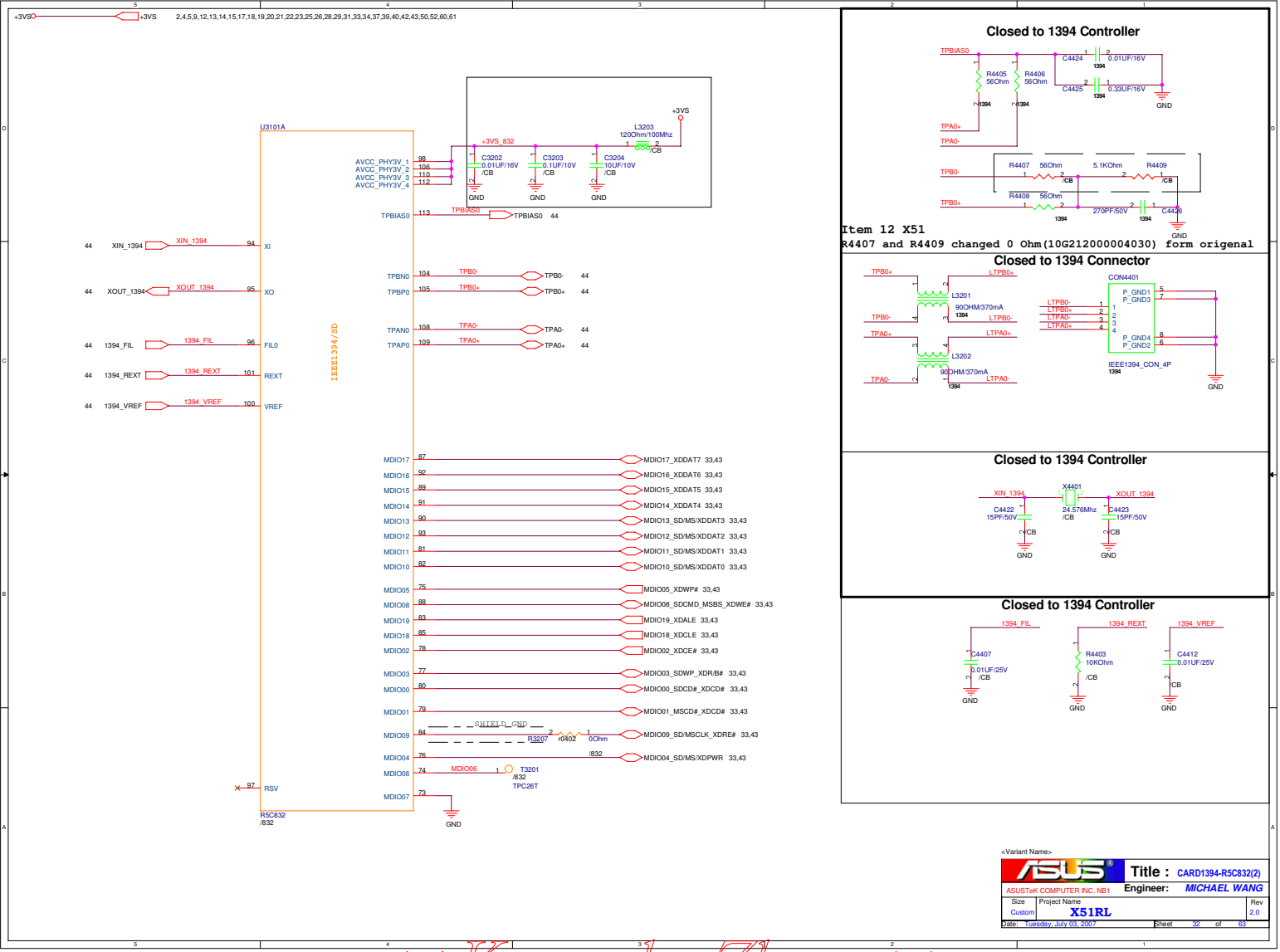
Date: Tuesday, July 03, 2007 Sheet 30 of 63

<< Kennedy_Zhang >>



<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C832(1)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 31 of 63	



Item 12 X51
R4407 and R4409 changed 0 Ohm(10G212000004030) form origenal

<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : CARD1394-R5C832(2)	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 32 of 63	

<< Kennedy_Zhang >>

Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU

MDIO000--> SD Card Detect
MDIO001--> MS Card Detect
MDIO003--> SD Write Protect
MDIO004--> SD Card Power0 Control/ MS Power Control
MDIO008--> SD Command/MS Bus State
MDIO009--> SD Clock/MS Clock
MDIO010--> SD Data 0/MS Data 0
MDIO011--> SD Data 1/MS Data 1
MDIO012--> SD Data 2/MS Data 2
MDIO013--> SD Data 3/MS Data 3

MDIO002--> xDCE#
MDIO005--> SD Power Control 1 / xDWP
MDIO006--> xD/MS/SD LED Control
MDIO014--> xD Data
MDIO015--> xD Data
MDIO016--> xD Data
MDIO017--> xD Data
MDIO018--> xD CLE
MDIO019--> xD ALE

SD/MMC/MS/MS-PRO Card Reader Socket

32,43 MDIO17_XDDAT7 — MDIO17_XDDAT7
32,43 MDIO16_XDDAT6 — MDIO16_XDDAT6
32,43 MDIO15_XDDAT5 — MDIO15_XDDAT5
32,43 MDIO14_XDDAT4 — MDIO14_XDDAT4
32,43 MDIO13_SD/MS/XDDAT3 — MDIO13_SD/MS/XDDAT3
32,43 MDIO12_SD/MS/XDDAT2 — MDIO12_SD/MS/XDDAT2
32,43 MDIO11_SD/MS/XDDAT1 — MDIO11_SD/MS/XDDAT1
32,43 MDIO10_SD/MS/XDDAT0 — MDIO10_SD/MS/XDDAT0

32,43 MDIO05_XDWP# — MDIO05_XDWP#
32,43 MDIO08_SDCMD_MSBS_XDWE# — MDIO08_SDCMD_MSBS_XDWE#
32,43 MDIO19_XDALE — MDIO19_XDALE
32,43 MDIO18_XDCLE — MDIO18_XDCLE
32,43 MDIO02_XDCE# — MDIO02_XDCE#

32,43 MDIO03_SDWP_XDR/B# — MDIO03_SDWP_XDR/B#
32,43 MDIO00_SDCD#_XDCD# — MDIO00_SDCD#_XDCD#
32,43 MDIO01_MSCD#_XDCD# — MDIO01_MSCD#_XDCD#
32,43 MDIO09_SD/MSCLK_XDRE# — MDIO09_SD/MSCLK_XDRE#

12G340004402

+VCCCA
C3304 270P @
C3305 270P @
C3306 270P @

CON3301 CARD_READER_44P

1	MS_GND1	XD_CD	23	XD_CD#	
2	MS_BS	XD_GND1	24		
3	MS_DATA1	XD_R/B	25	MDIO03_SDWP_XDR/B#	
4	MS_DATA0	XD_RE	26	MDIO09_SD/MSCLK_XDRE#	
5	MS_DATA2	XD_CE	27	MDIO02_XDCE#	
6	MS_INS	XD_CLE	28	MDIO18_XDCLE	
7	MS_DATA3	XD_ALE	29	MDIO19_XDALE	
8	MS_SCLK	XD_WE	30	MDIO08_SDCMD_MSBS_XDWE#	
9	MS_VCC	XD_WP	31	MDIO05_XDWP#	
10	MS_GND2	XD_GND2	32		
11	SD_DAT2	XD_D0	33	MDIO10_SD/MS/XDDAT0	
12	SD_DAT3	XD_D1	34	MDIO11_SD/MS/XDDAT1	
13	SD_CMD	XD_D2	35	MDIO12_SD/MS/XDDAT2	
14	SD_GND1	XD_D3	36	MDIO13_SD/MS/XDDAT3	
15	SD_VCC	XD_D4	37	MDIO14_XDDAT4	
16	SD_CLK	XD_D5	38	MDIO15_XDDAT5	
17	SD_GND2	XD_D6	39	MDIO16_XDDAT6	
18	NC1	XD_D7	40	MDIO17_XDDAT7	
19	SD_DAT0	XD_VCC	41		
20	SD_DAT1	NC2	42		
21	SD_CD_SW	SD_WP_SW	43	MDIO03_SDWP_XDR/B#	
22	SD_CD_COM	SD_WP_COM	44		
45	NP_NC1	NP_NC2	46		
47	GND1	GND2	48		

MDIO08_SDCMD_MSBS_XDWE#
MDIO11_SD/MS/XDDAT1
MDIO10_SD/MS/XDDAT0
MDIO12_SD/MS/XDDAT2
MSCD#
MDIO13_SD/MS/XDDAT3
MDIO09_SD/MSCLK_XDRE#
SD_DAT2
MDIO13_SD/MS/XDDAT3
MDIO08_SDCMD_MSBS_XDWE#
MDIO09_SD/MSCLK_XDRE#
MDIO10_SD/MS/XDDAT0
SD_DAT1
SDCD#

N/A

+3VS
Q3306 IRLML5103PBF /CB
+VCCCA
R3305 100KOhm /CB
C3308 0.1UF/10V /CB
Place as close to card reader socket as possible
32,43 MDIO04_SD/MS/XDPWR

+VCCCA
C3307 0.01UF/10V @
C3309 0.01UF/10V /CB
C3310 0.01UF/10V /CB
R3306 150K /CB
C3311 2.2UF/6.3V /CB
Place as close to card reader socket as possible

To coorect the problem when MS Duo adaptor is in use.

+12VS
R3301 10KOhm /CB
SDCD#
Q3301A UM6K1N /CB
GND
MDIO11_SD/MS/XDDAT1
Q3301B UM6K1N /CB
SD_DAT1
MDIO12_SD/MS/XDDAT2
Q3302A UM6K1N /CB
SD_DAT2

Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low

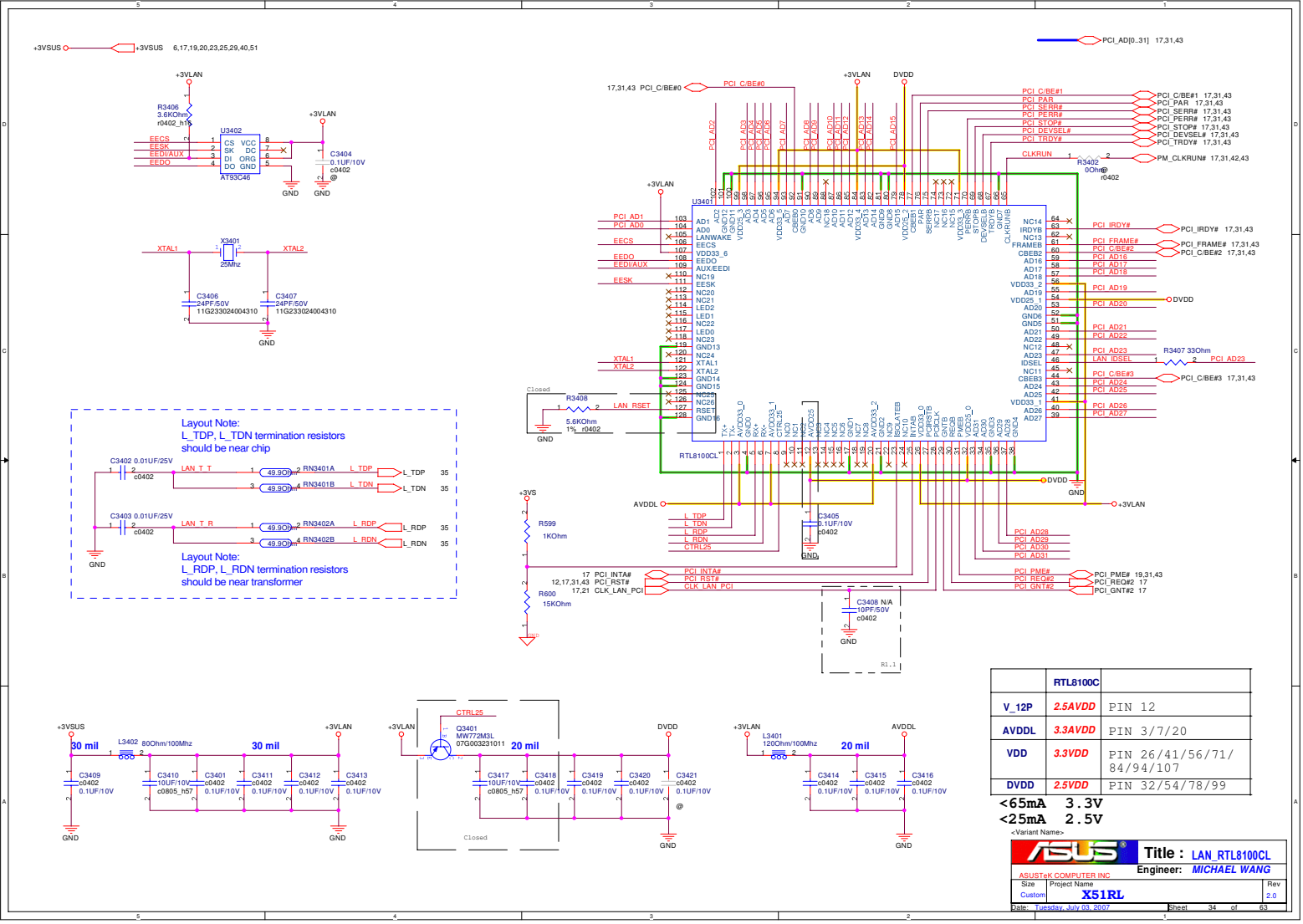
+3VS
R3302 10KOhm /CB
XD_CD#
SDCD#
D3301 DAP202K /CB
/CB
Q3302B UM6K1N
R3208 0Ohm r0402 @
MDIO00_SDCD#_XDCD#
MDIO01_MSCD#_XDCD#
D3302 DAP202K /CB
+3VS
R3304 10KOhm /CB
MSCD#
For Memory Stick Duo Adaptor shielding ground issue

<Variant Name>

ASUSTeK COMPUTER INC
Project Name: X51RL
Engineer: MICHAEL WANG
Size: Custom
Title : CardReader
Rev: 2.0
Date: Tuesday, July 03, 2007
Sheet 33 of 63

+12VS — +12VS 12,37,61
+3VS — +3VS 2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,34,37,39,40,42,43,50,52,60,61

<< Kennedy_Zhang >>



	RTL8100C	
V_12P	2.5AVDD	PIN 12
AVDDL	3.3AVDD	PIN 3/7/20
VDD	3.3VDD	PIN 26/41/56/71/84/94/107
DVDD	2.5VDD	PIN 32/54/78/99

<65mA 3.3V
<25mA 2.5V
<Variant Name>

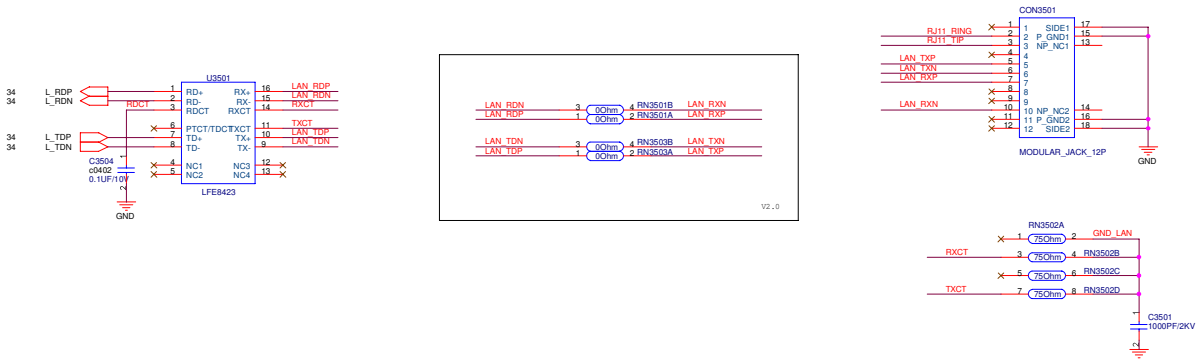
ASUSTeK COMPUTER INC
Title : LAN_RTL8100CL
Engineer: MICHAEL WANG
Size: Custom
Project Name: X51RL
Rev: 2.0
Date: Tuesday, July 03, 2007
Sheet 34 of 63

<< Kennedy_Zhang >>

+3V +3V 17,25,26,27,31,37,42,43,44,61

LAN PORT

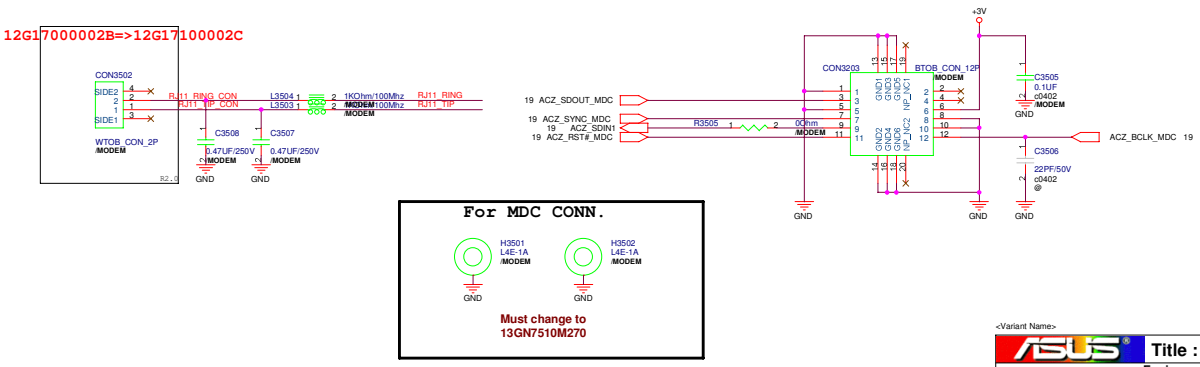
12G142111120



MDC CONNECTOR

12G17000002B=>12G17100002C

12G161200124



<Variant Name>

Title : RJ11/45 & MDC

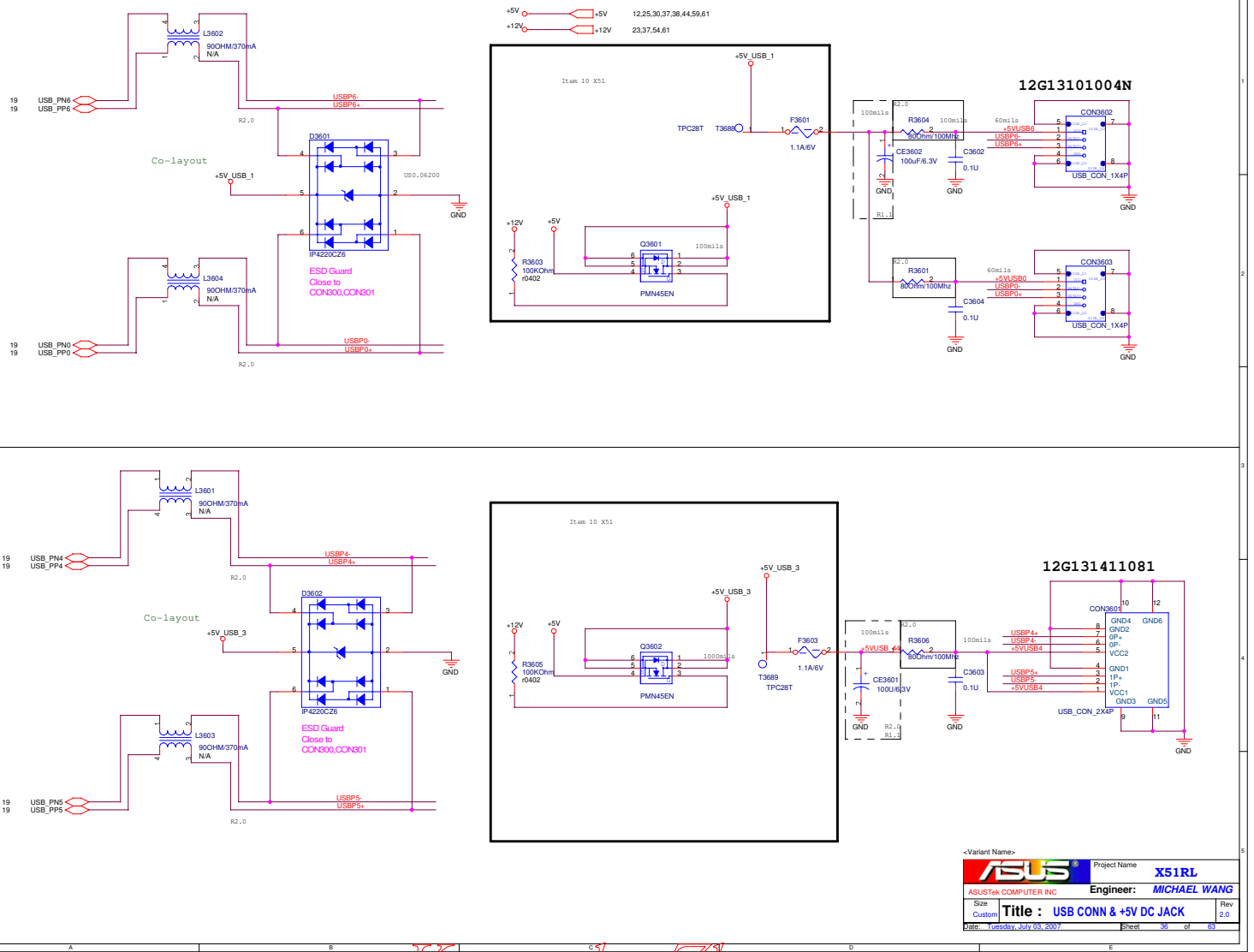
Engineer: MICHAEL WANG

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 35 of 63

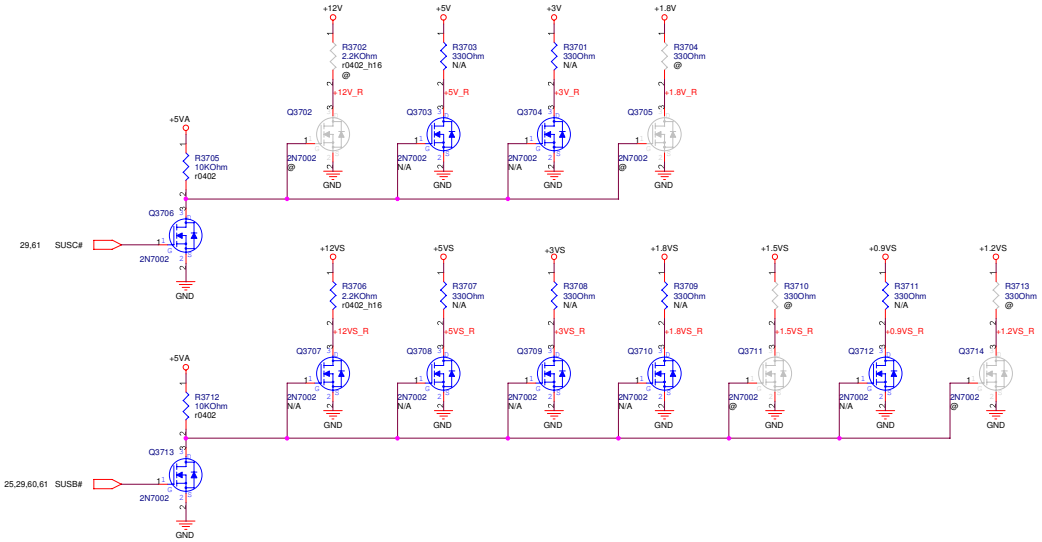
<< Kennedy_Zhang >>



<Variant Name>

ASUSTek COMPUTER INC	Project Name: X51RL	
	Engineer: MICHAEL WANG	
Size: Custom	Title : USB CONN & +5V DC JACK	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 36 of 63	

<< Kennedy_Zhang >>

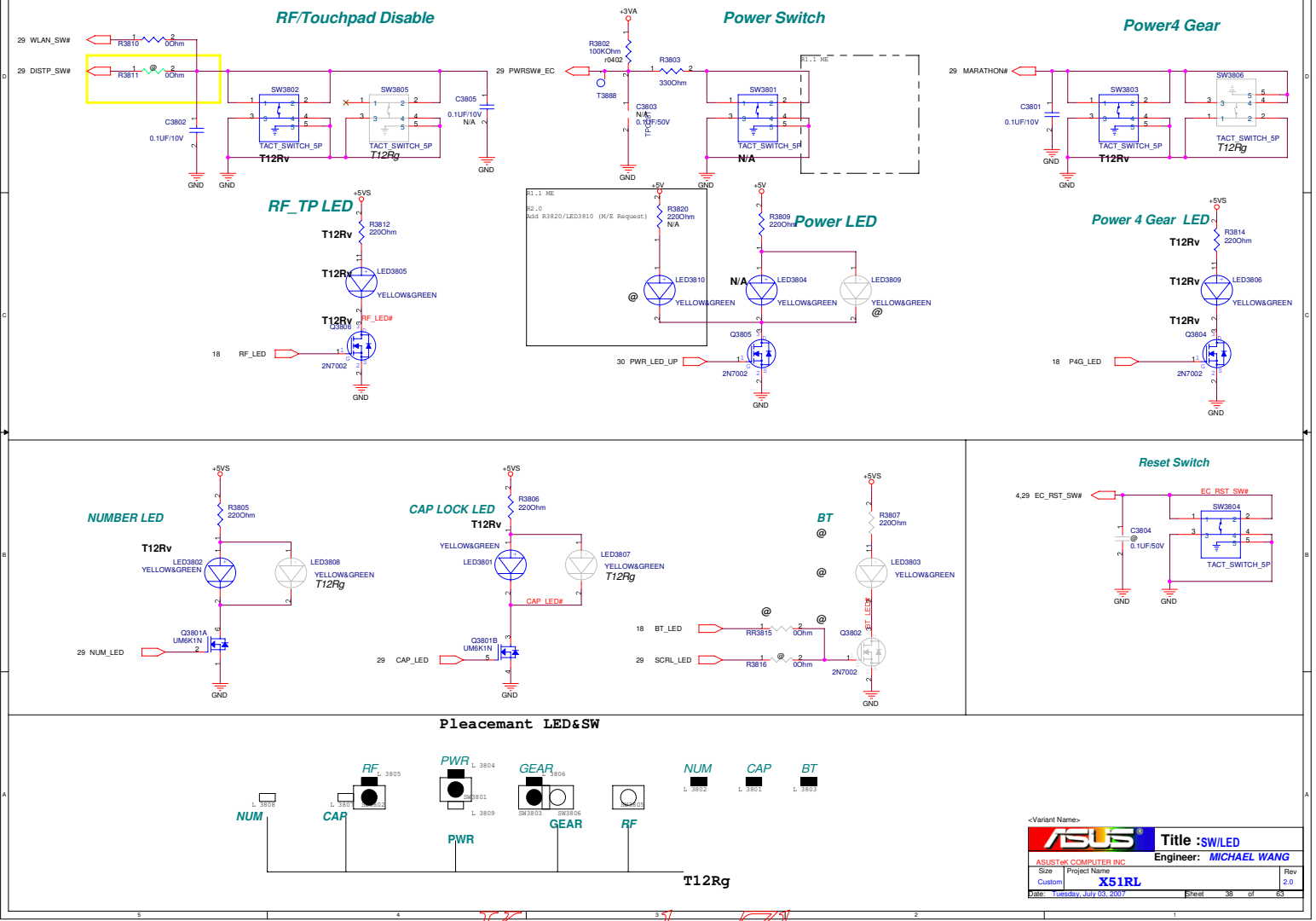


Check all power plan

<Variant Name>

ASUSTeK COMPUTER INC	Title : Discharge Circuit	
	Engineer: MICHAEL WANG	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 37 of 63	

Main Board SW & LED



Pleacemant LED&SW

<Variant Name>

ASUSTeK COMPUTER INC

Title : SW/LED

Engineer: MICHAEL WANG

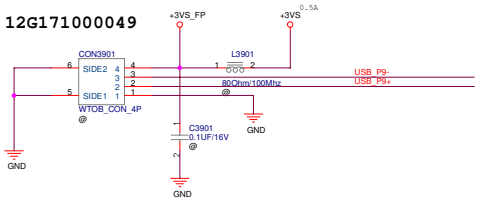
Size	Project Name	Rev
Custom	X51RL	2.0

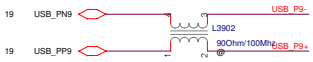
Date: Tuesday, July 03, 2007 Sheet 38 of 63

+3VS +3VS 2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,40,42,43,50,52,60,61

FINGER PRINT
Reserved

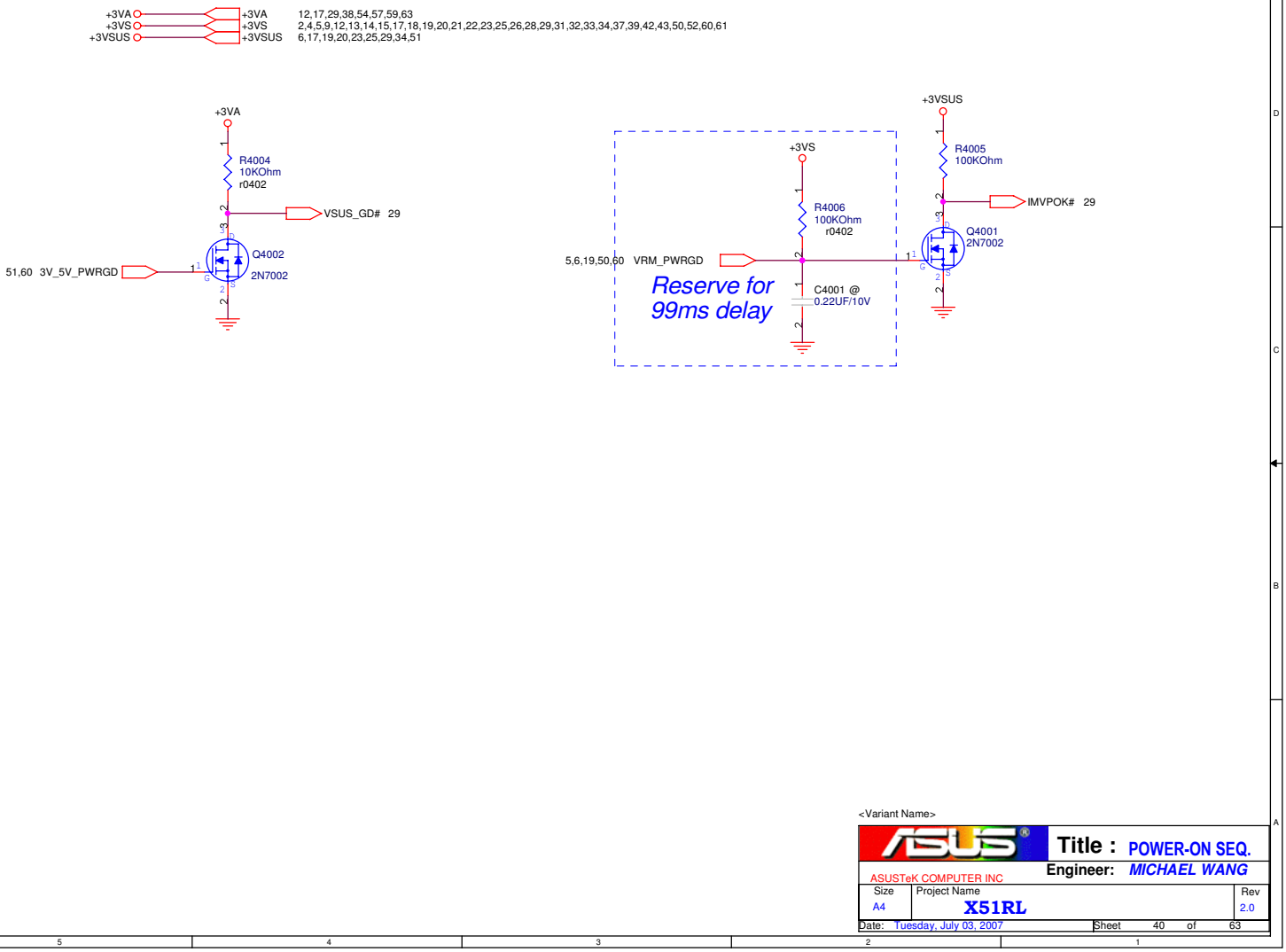
USB P0 CON3603
USB P1
USB P2 BT
USB P3 NEW CARD
USB P4 CON3601
USB P5 CON3601
USB P6 CON3602
USB P7
USB P8 PC_CAM
USB P9 FINGER PRINT





<Variant Name>

Title : FINGER PRINT
ASUSTeK COMPUTER INC
Engineer: MICHAEL WANG
Size: Custom
Project Name: X51RL
Rev: 2.0
Date: Tuesday, July 03, 2007
Sheet 39 of 63



<Variant Name>

ASUSTeK COMPUTER INC

Title : POWER-ON SEQ.

Engineer: MICHAEL WANG

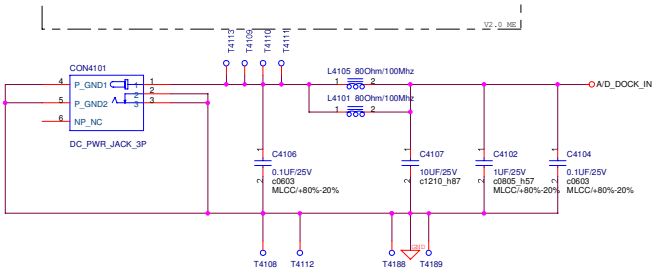
Size	Project Name	Rev
A4	X51RL	2.0

Date: Tuesday, July 03, 2007 Sheet 40 of 63

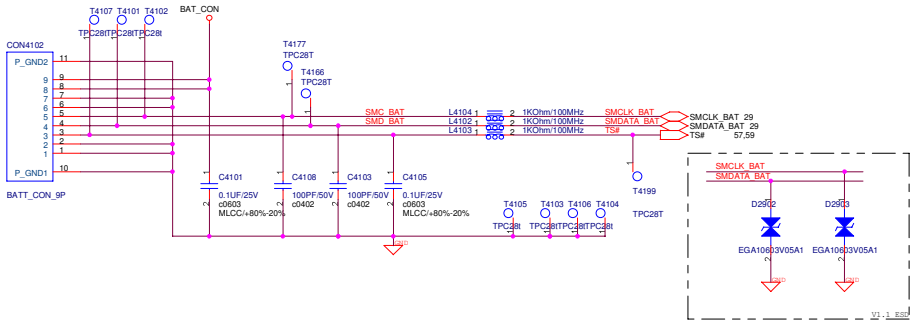
<< Kennedy_Zhang >>

A/D_DOCK_IN — A/D_DOCK_IN 57,59
BAT_CON — BAT_CON 57
AC_BAT_SYS — AC_BAT_SYS 12,50,51,52,53,54,57,60

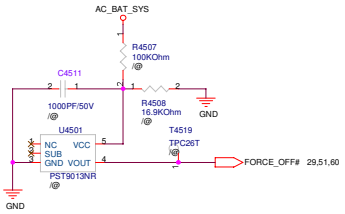
12G145002034=>12G14530103E=>12G14530103V



12G20001090G



Without Battery & Pull out Adapter
RESERVED



<Variant Name>

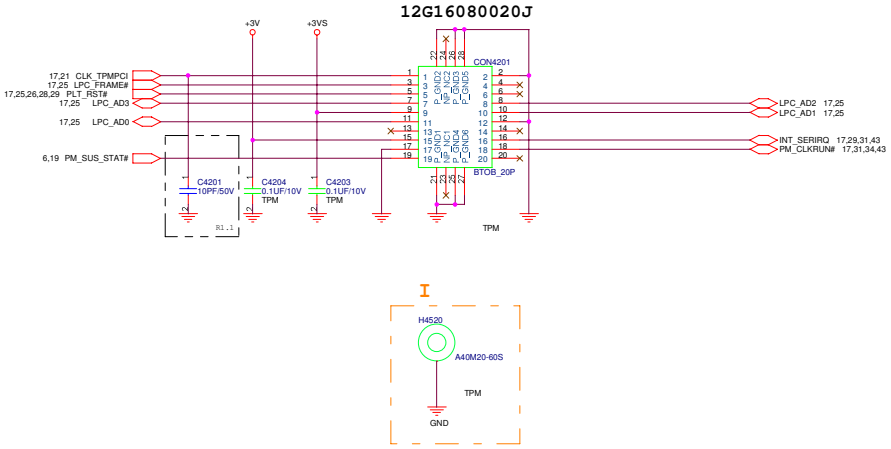
ASUSTek COMPUTER INC	Project Name	X51RL
	Engineer:	MICHAEL WANG
Size: Custom	Title : DC IN	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 41 of 63	

<< Kennedy_Zhang >>

+3VS → +3VS 2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,43,50,52,60,61

+3V → +3V 17,25,26,27,31,35,37,43,44,61

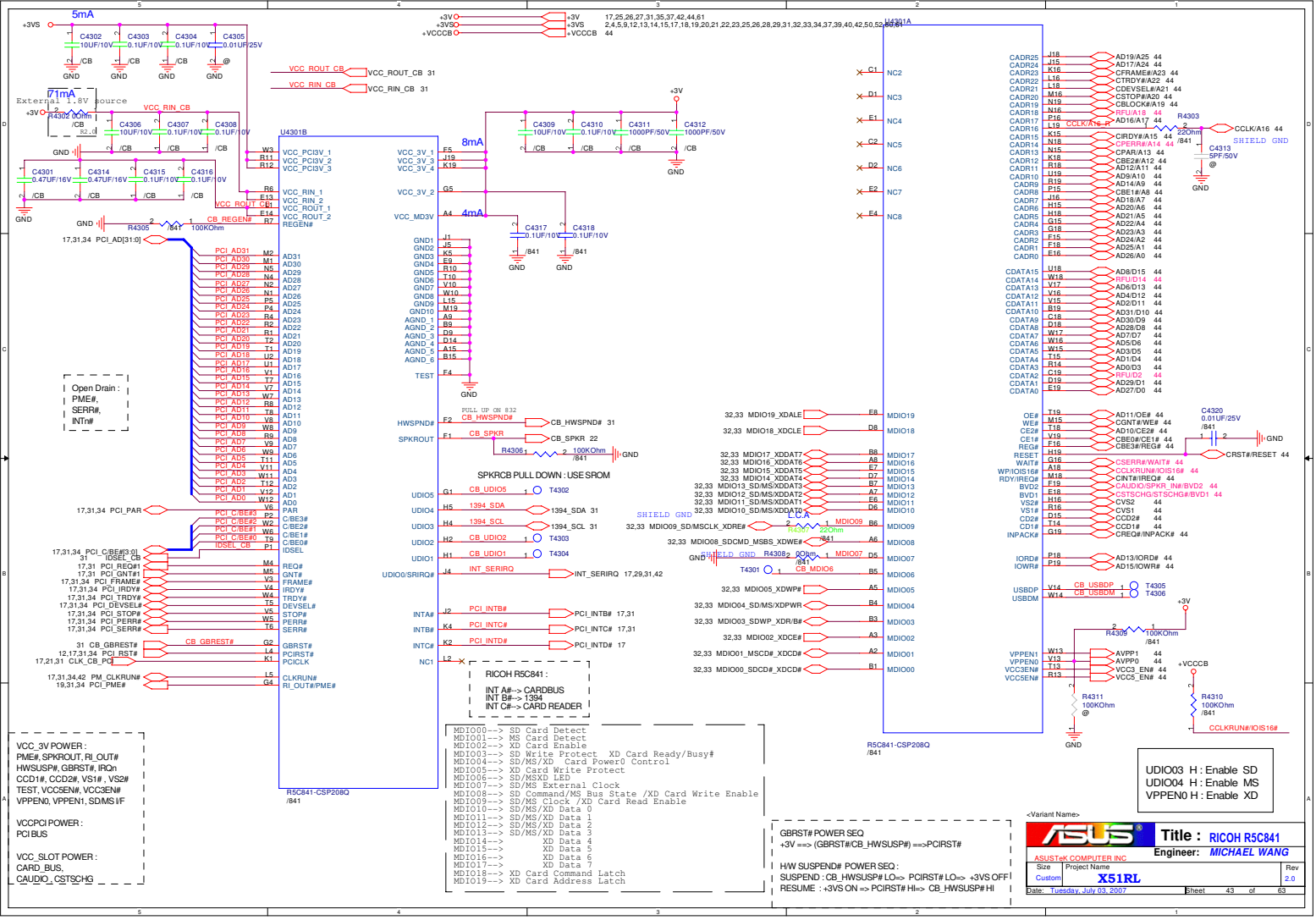
TPM Module CON
RESERVED



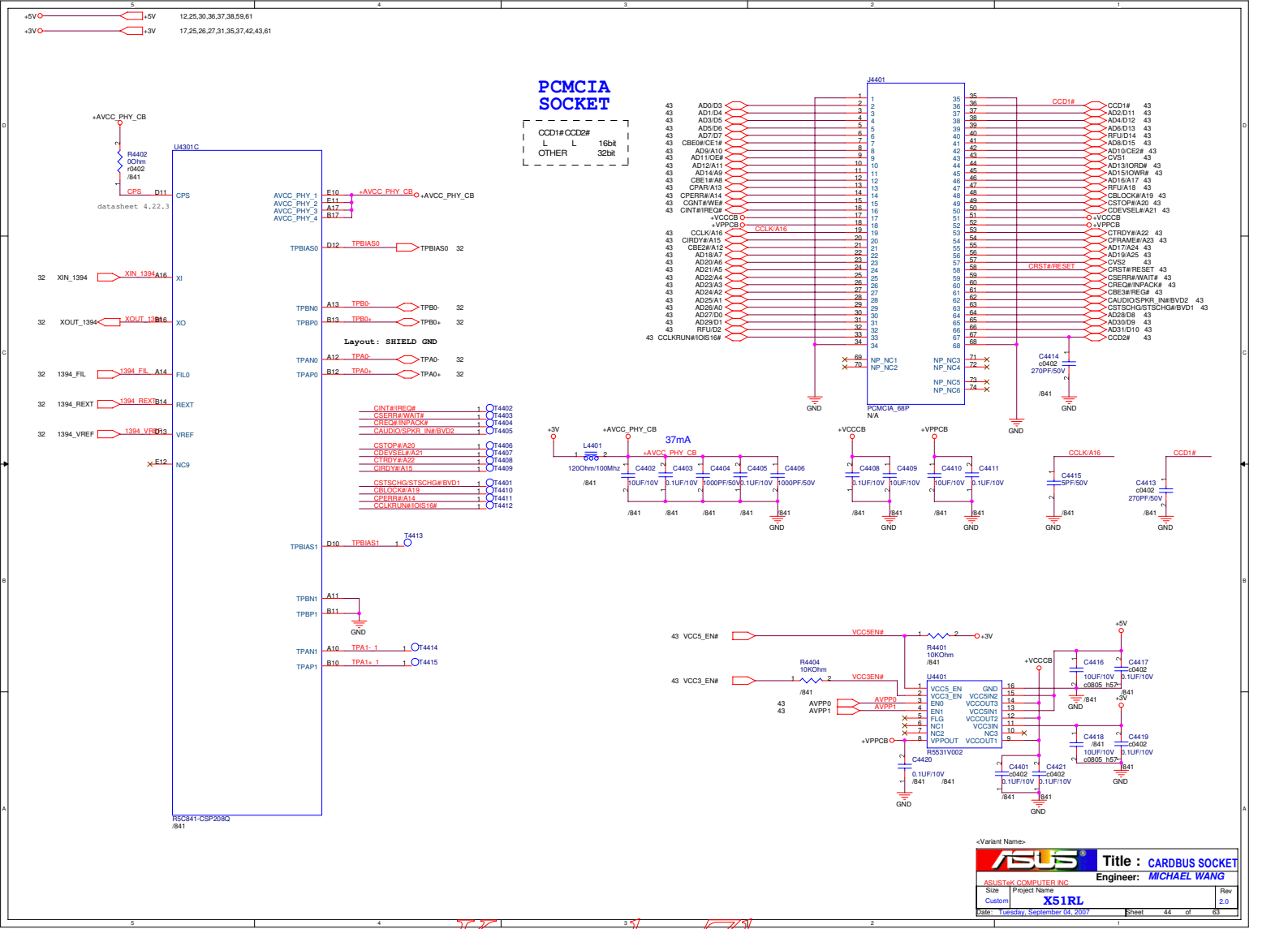
For TPM CONN.

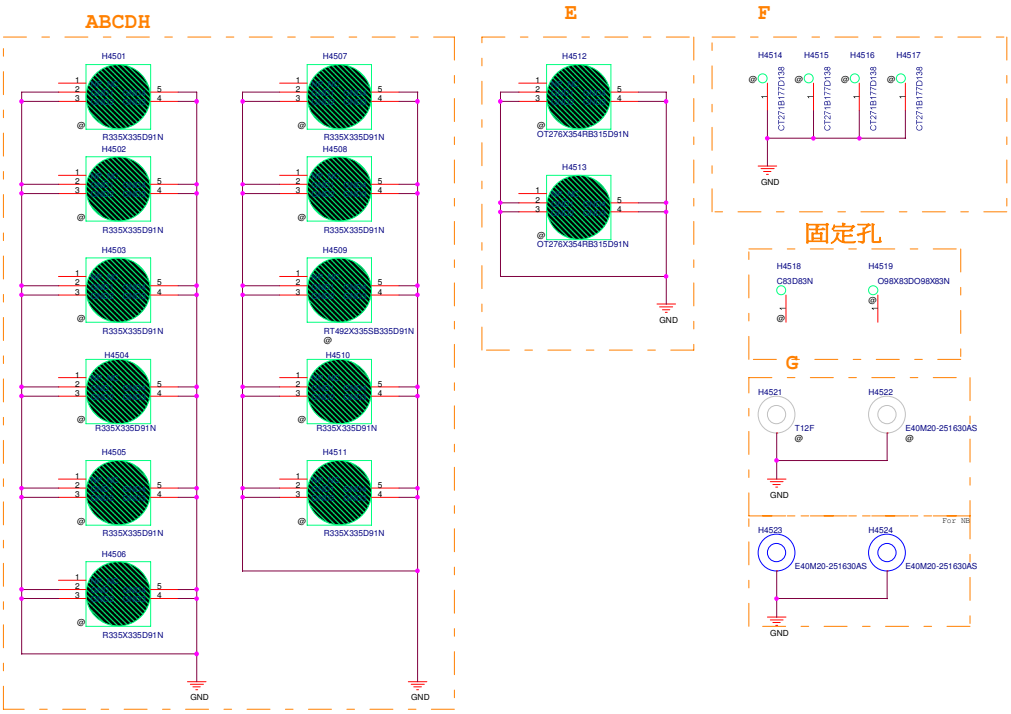
<Variant Name>

ASUSTek COMPUTER INC	Project Name: X51RL	
	Engineer: MICHAEL WANG	
Size: Custom	Title : TPM 1.2	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 42 of 63	



<< Kennedy_Zhang >>





<Variant Name>

Title : SCREW HOLE

Engineer: MICHAEL WANG

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Wednesday, May 16, 2007 Sheet 45 of 63

<< Kennedy_Zhang >>

<Variant Name>

Title : HISTORY

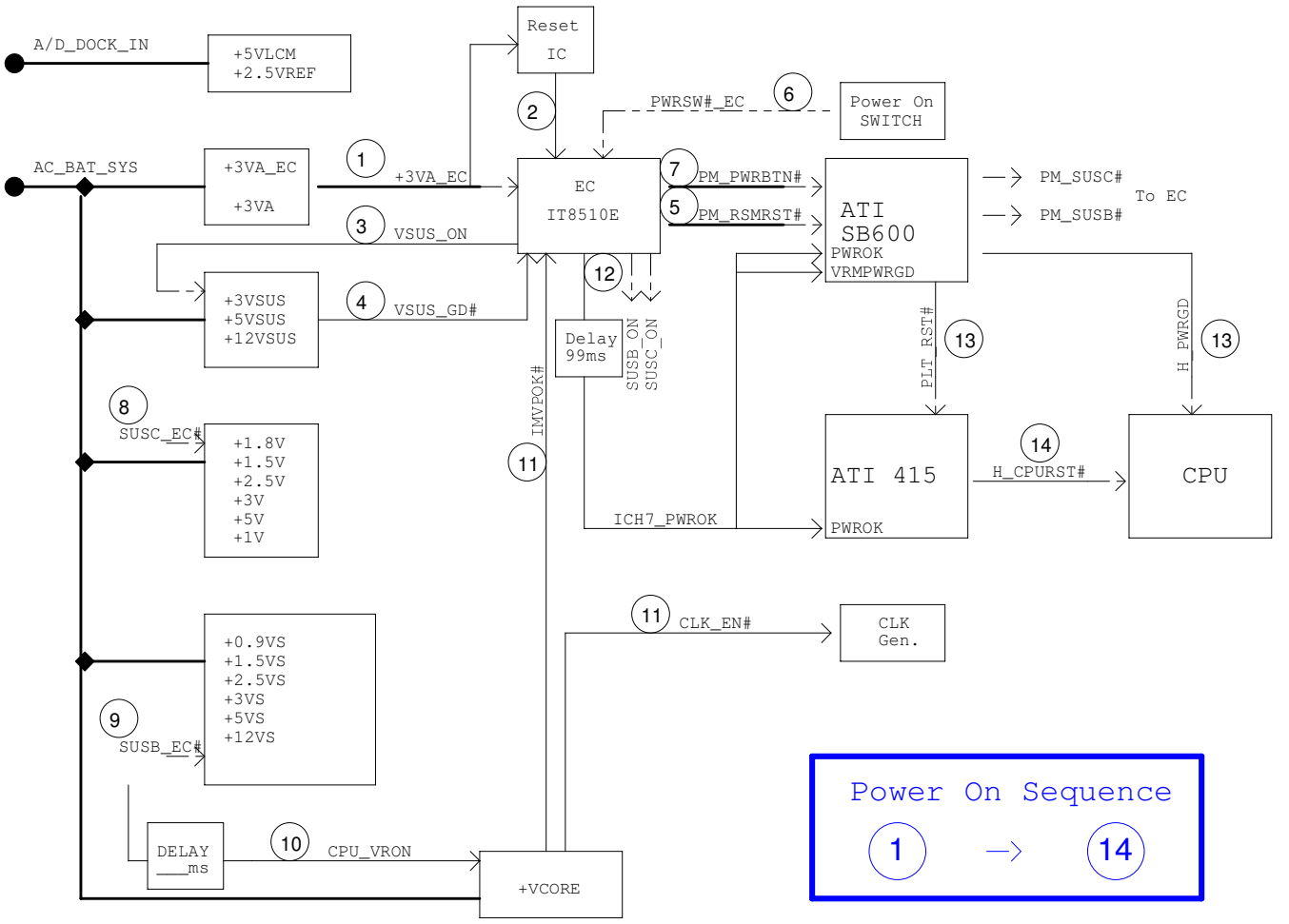
Engineer: MICHAEL WANG

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Wednesday, May 16, 2007 Sheet 46 of 63

<< Kennedy_Zhang >>



<Variant Name>

ASUSTeK COMPUTER INC

Title : FLOWCHART

Engineer: MICHAEL WANG

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Wednesday, May 16, 2007 Sheet 47 of 63

<< Kennedy_Zhang >>

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM		48	GPH0	VSUS_ON	O
33	PWM1/GPA1	FAN_PWM	O	54	GPH1	VSUS_GD#	I
36	PWM2/GPA2	/		55	GPH2	IMVPOK#	I
37	PWM3/GPA3	/		69	GPH3	PM_PWRBTN#	O
38	PWM4/GPA4	CHG_LED_UP#	O	70	GPH4	SUSC_EC#	O
39	PWM5/GPA5	PWR_LED_UP#	O	75	GPH5	SUSB_EC#	O
40	PWM6/GPA6	BATSEL_3S#		76	GPH6	CPU_VRON	O
43	PWM7/GPA7	LCD_BACKOFF#	O	105	GPH7	PM_RSMRST#	O
153	RXD/GPB0	NUM_LED	O	148	GPI0	ICH7_PWROK	O
154	TXD/GPB1	CAP_LED	O	149	GPI1	WATCH_DOG#	O
162	GPB2	SCRL_LED	O	152	GPI2	/	
163	SMCLK0/GPB3	SMCLK_BAT	I/0	155	GPI3	CHG_EN#	O
164	SMDAT0GPB4	SMDATA_BAT	I/0	156	GPI4	PRECHG	O
5	GA20/GPB5	A20GATE	O	168	GPI5	BAT_LL#	O
6	KBRST#/GPB6	RC_IN#	O	174	GPI6	BAT_LEARN	O
165	GPB7	THRO_CPU	O				
				8	GPL0	WLAN_ON#	O
169	SMCLK1/GPC1	SMB1_CLK	I/0	11	GPL1	BT_ON#	O
170	SMDAT1/GPC2	SMB1_DAT	I/0	12	GPL2	RF_OFF_SW#	I
171	GPC3	/		20	GPL3	RF_LED	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I	92	CRX	CRX	I/0
175	GPC5	OP_SD#	O				
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I				
1	CK32KOUT/GPC7	/	O				
26	RI1#/WUI0/GPD0	PM_SUSB#	I				
29	RI2#/WUI1/GPD1	PM_SUSC#	I				
30	LPCRST#/WUI4//GPD2	PLT_RST#	I				
31	ECSCI#/GPD3	EXT_SCI#	O				
41	GPD4		I				
42	GINT/GPD5	/					
62	TACH0/GPD6	FAN0_TACH	I				
63	TACH1/GPD7	/	O				
87	ADC4/GPE0	WLAN_SW#	I				
88	ADC5/GPE1	/	I				
89	ADC6/GPE2	MARATHON#	I				
90	ADC7/GPE3	DISTP_SW#	I				
2	PWRSW/GPE4	PWRSW#_EC	I				
44	WUI5/GPE5	/					
24	LPCPD#/WUI6/GPE6	LID_EC#	I				
25	CLKRUN#/WUI7/GPE7		O				
110	PS2CLK0/GPF0	/					
111	PS2DAT0/GPF1	/					
114	PS2CLK1/GPF2	/	I/0				
115	PS2DAT1/GPF3	/	I/0				
116	PS2CLK2/GPF4	TP_CLK					
117	PS2DAT2/GPF5	TP_DAT					
118	PS2CLK3/GPF6	PWRLMT#					
119	PS2DAT3/GPF7	/	I				
113	FA16/GPG0	FA16					
112	FA17/GPG1	FA17					
104	FA18/GPG2	FA18					
103	FA19/GPG3	/					
3	FA20/GPG4	THRM_CPU#	I				
4	FA21/GPG5	/					
27	LPC80HL/GPG6	PMTHERM#	O				
28	LPC80LL/GPG7	AC_APR_UC#	I				

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I
C8	GPIO01/REQ5#	PCI_REQ#5	I
G8	GPIO02/PIRQE#	PCI_INTE#	I
F7	GPIO03/PIRQF#	PCI_INTF#	I
F8	GPIO04/PIRQG#	PCI_INTG#	I
G7	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	BT_LED	I/O
AC18	GPIO07	/	I
E21	GPIO08	EXTSMI#	I
E20	GPIO09	SATA_DET#0	I
A20	GPIO10	/	O
B23	SMBALERT#/GPIO11	SMB_ALERT#	I
F19	GPIO12	KBC_SCI#	I
E19	GPIO13	/	
R4	GPIO14	/	
E22	GPIO15	WLAN_LED#	I/O
AC22	GPIO16	PM_DPRSLPVR	O
D8	GPIO17/GNT5#	PCI_GNT#5	O
AC20	GPIO18/STP_PCI#	STP_PCI#	O
AH18	GPIO19/SATA1GP	/	I
AF21	GPIO20/STP_CPU#	STP_CPU#	O
AE19	GPIO21/SATA0GP	/	I
A13	GPIO22/REQ4#	PCI_REQ#4	I
AA5	LDRQ1#/GPIO23	LPC_DRQ#1	I/O
R3	GPIO24	P4G_LED#	
D20	GPIO25	CB_SD#	
A21	GPIO26/EL_RSVD	BT_DET#	
B21	GPIO27/EL_STATE0		I
E23	GPIO28/EL_STATE1		
C3	GPIO29/OC#5	USB_OC_5#	I
A2	GPIO30/OC#6	NEWCARD_OC#	I
B3	GPIO31/OC#7	USB_OC_7#	I
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O
AC19	GPIO33/AZ_DOCK_EN#	/	O
U2	GPIO34/AZ_DOCK_RST#	/	
AD21	GPIO35	ICH_GPIO35	O
AH19	GPIO36/SATA2GP	/	
AE19	GPIO37/SATA3GP	PCB_ID0	I/O
AD20	GPIO38	PCB_ID1	I
AE20	GPIO39	PCB_ID2	I
A14	GNT4#/GPIO48	PCI_GNT#4	O
AG24	GPIO49/CPUPWRGD	H_PWRGD	O

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

<Variant Name>

Title : GPIO Setting

Engineer: MICHAEL WANG

ASUSTeK COMPUTER INC

Size	Project Name	Rev
Custom	X51RL	2.0

Date: Wednesday, May 16, 2007 Sheet 48 of 63

<< Kennedy_Zhang >>

T12R V1.1 History

1. Page 17, del U1702 and R1726 delete PCI_RST# Buffer.
3. Page 18, added R1802
4. Page 43&12, D4301 and L1201改footprint
5. Page 6, delete D1204 and added R601 R609 to avoid can not boot.
6 Page 17, Mount R1708, U1703 option changed reset path
7. Page 43, Mount R4302 for R5C841 internal LDO input
8. Page 9, un-mount L906 C914 , these for 610 only

9. All PCI clock added 6.8 pF to decrease skew.
10. PWM connected to EC and back-light connected to NB
11. D1306 D1301 connected to +5VS, let these signal have the same PWR plan. For ESD
12. page 19, added BT_DET# to detect BT.
13. Page 19, adjust USB OC ping to correspond USB port
14. Page 25, modification NEW CARD debug circuit to correspond new debug card
15. page 28, we used correctly capacity for customer request.
16. page 36, we used LDO with over current protect IC
17. page 41, DC in connector add 2nd source.

ME modify
1.ODD往板外移0.4mm
2
3.BATT 往板內移0.23mm
4.增加螺絲鎖付記號

6.DDR2 added 2nd source
P/N :12G025022004
DDR2 DIMM 200P,1.8V,H:4mm,STD
FOXCONN/AS0A426-N4SN-1
7.add led 1 pcs LED3810 and del. SW3807(option)
8.遮版圖修改

T12R V2.0 Modify History

1. Page 6, R609 repleacement 220K by 10K
2. Page 12, RN1203 repleacement C.M chock by 0Ohm for EMI.
3. For DDRII connector(H=4mm) repleacement 12G025022004 by original.
4. For DDRII connector(H=9mm) repleacement 12G025C22004 by original.
5. For DC IN jack repleacement 12G14530103E by original(long core).
6. Page 22, for audio micro phone low quility issue, it need to changed larger cappator 10U (replace 100 with 1U).
7. Page 29, we changed new EC 8511.
8. Page 38, to increase LED brightness, we replace 07G015200485 by original
9. page 30, for EMI request, we added L3010 and L3011 and mount C3002 C3003 and C3006~3010
10 Page 35, for EMI requestion, we added 0Ohm before LAN jack for option CM chock.

T12Rg V1.0 modify from T12R V2.0

1. To modify BOM include LED(color&placement), SW(placement), HDD(PATA TO SATA), PCCAM(unmount), internal MIC(unmount) and R5C841(added 1394 cardreader and PCMCIA).

T12Rg V2.0

1. Page 12, L1203 0 Ohm to bead, EMI request.
2. Page 12, L1204 and L1205 0 Ohm to bead and mount C1222 C1223, EMI request.
3. Page 12, mount L1214 L1215 Ohm for added internal speaker.
4. Page 12, mount L1206, EMI request.
5. Page 6, R2301 and R2304 10K to 12K for 2W speaker..
6. Page 6, modify BOM, unmount R2908.

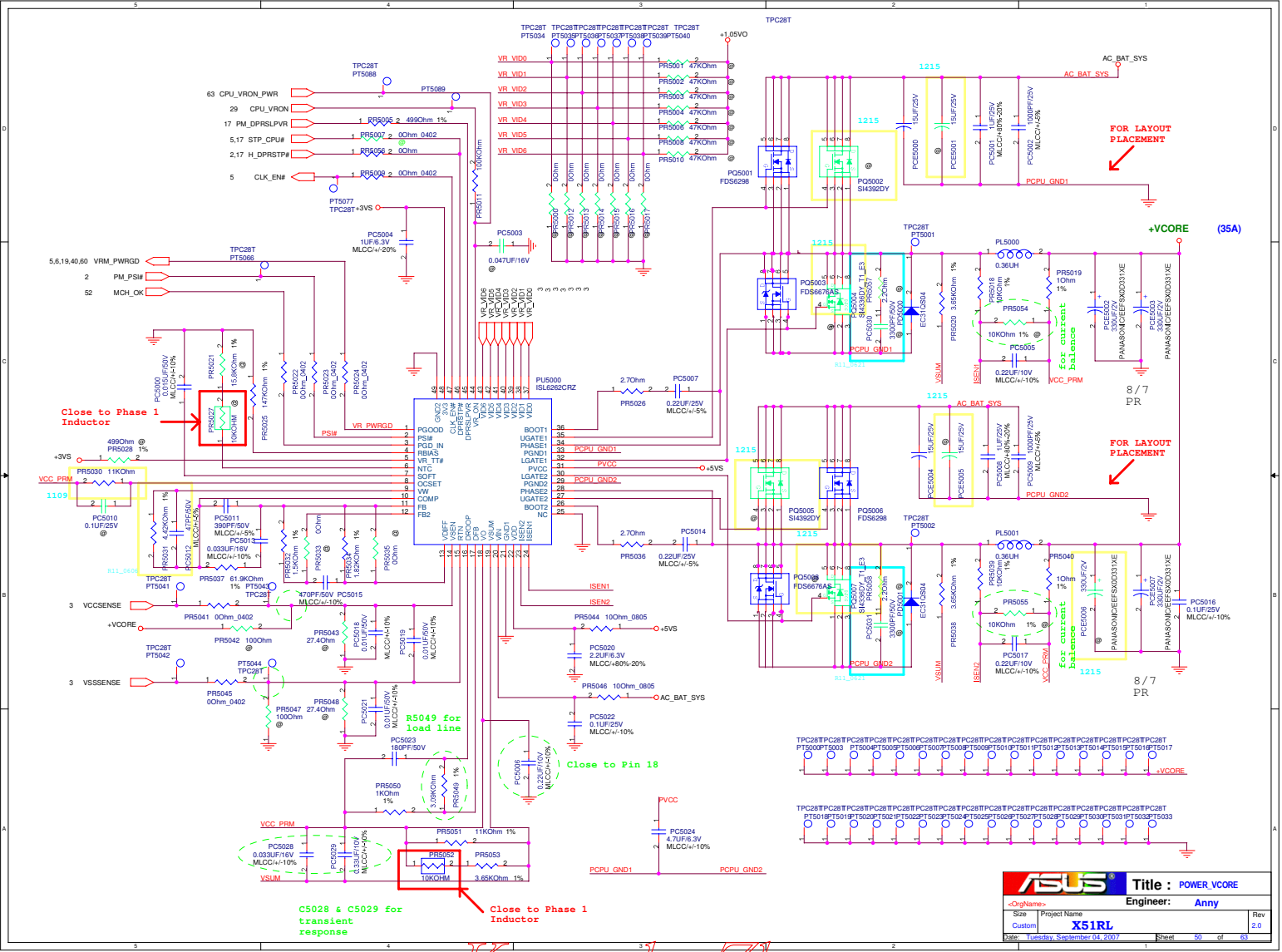
T12R V2.1/ X51 V1.0 modify from T12R V2.0

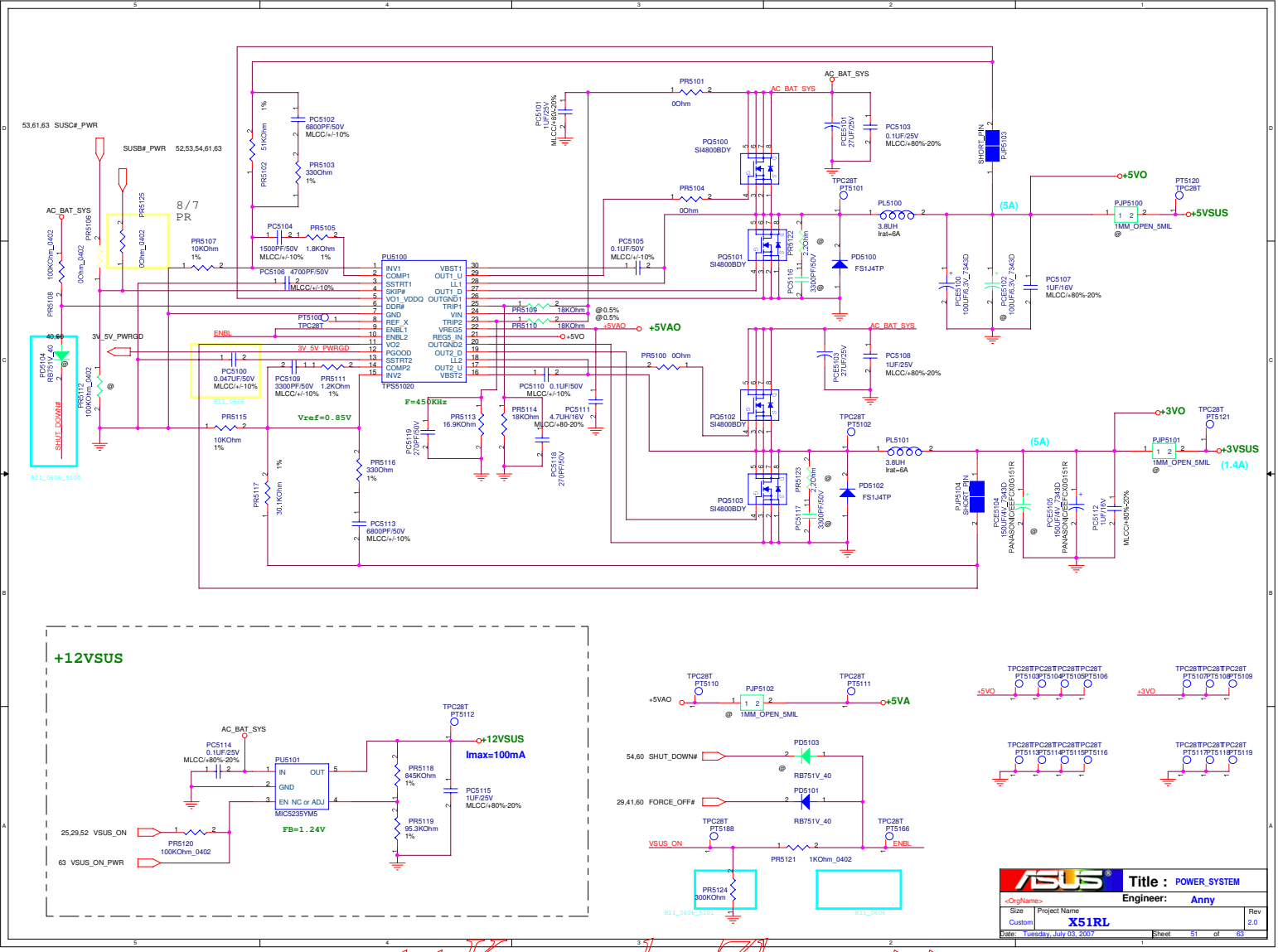
1. Page 6, support DDRII 667, modify DDR sechematic(CKE OTD)
1. Page 6, replacment SB A20 form A13
1. Page 6, modify BOM, delete R2908.
1. Page 6, added D2910 for EMI.
1. Page 6, to support 3S1P, added some circuit EC to H_PROCHOT_S#.

1. Page 6,modify BOM include LED, SW, HDD(DEL PATA), PCCAM and R5C841(added).

	X51	T12RG	T12R
NB	415ME	415ME	415MD
SB	SB600 A21	SB600 A21	SB600 A13
AUDIO	660VD	660VD	660VD
SPDIF	N/A	N/A	N/A
R5C832	N/A	N/A	N/A
R5C841	OK	OK	N/A
1394	N/A	OK	N/A
CARD READER	OK	OK	N/A
PCMCIA	OK	OK	N/A
NEW CARD	N/A	N/A	N/A
TPM	N/A	OK	N/A
BT	OK	N/A	N/A
PC_CAM	N/A	N/A	OK
INT. MIC.	N/A	OK	OK
MODEN	OK	N/A	N/A
TV	N/A	N/A	N/A
SPEAKER	1.5W	2W	1.5W

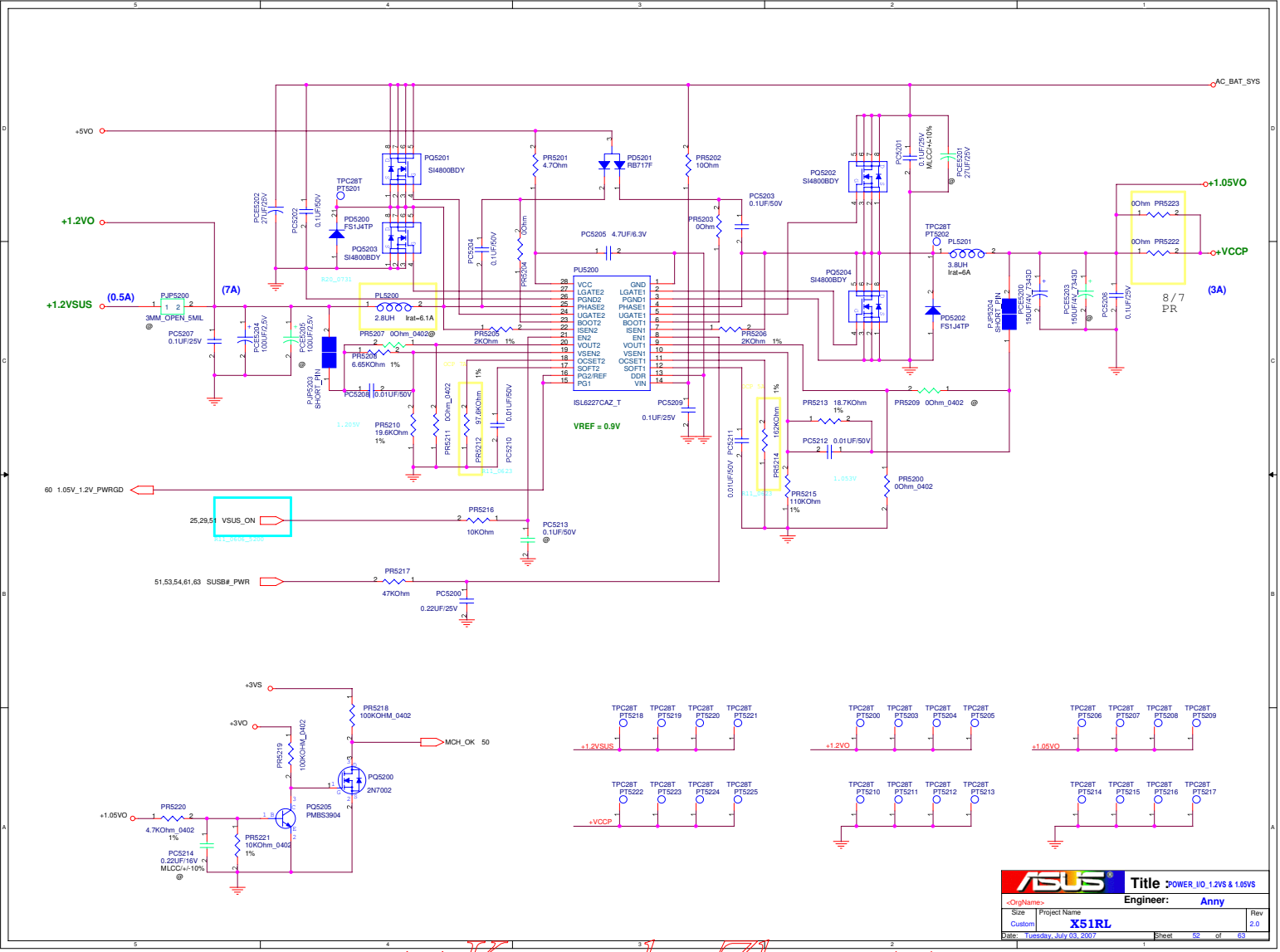
Title : HISTORY
Engineer:
Project Name: X51RL

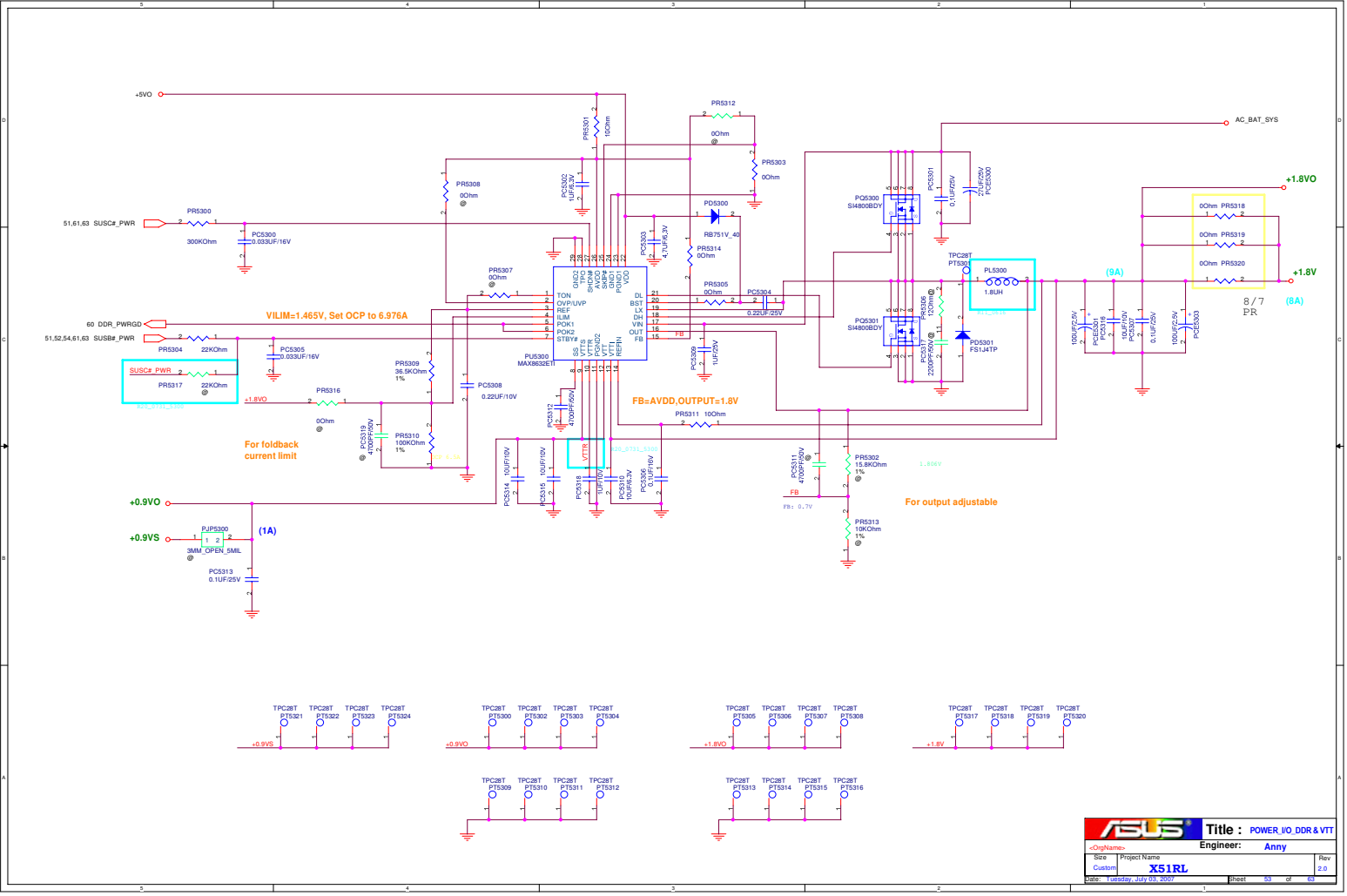




Title : POWER_SYSTEM
<OrgName> Engineer: Anny
Size: Custom | Project Name: X51RL | Rev: 2.0
Date: Tuesday, July 03, 2007 | Sheet 51 of 63

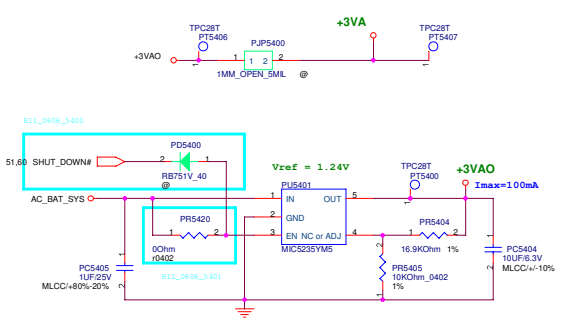
<< Kennedy_Zhang >>



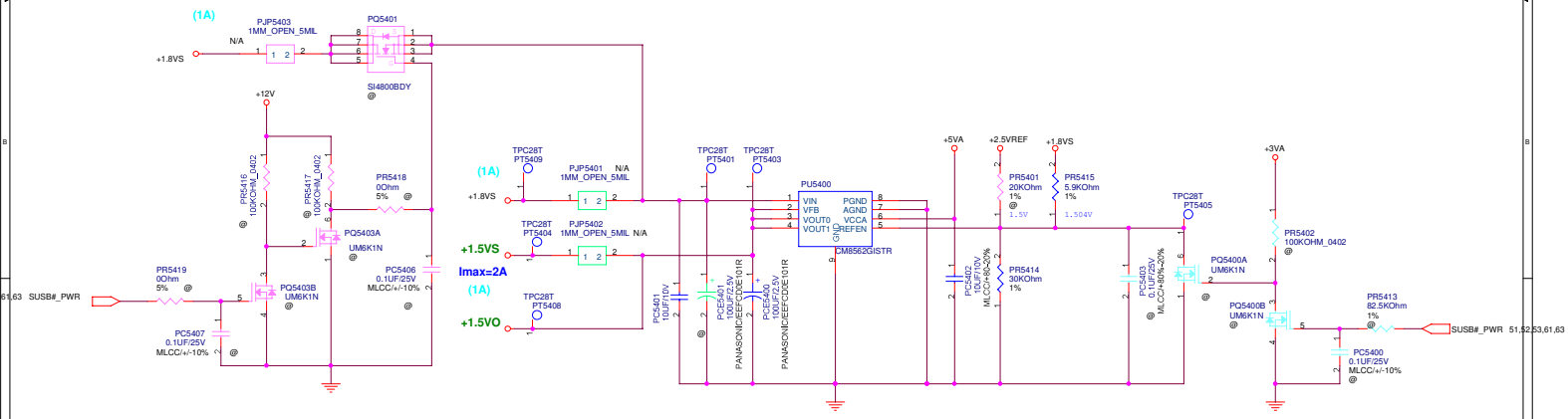


<< Kennedy_Zhang >>

+3VAO

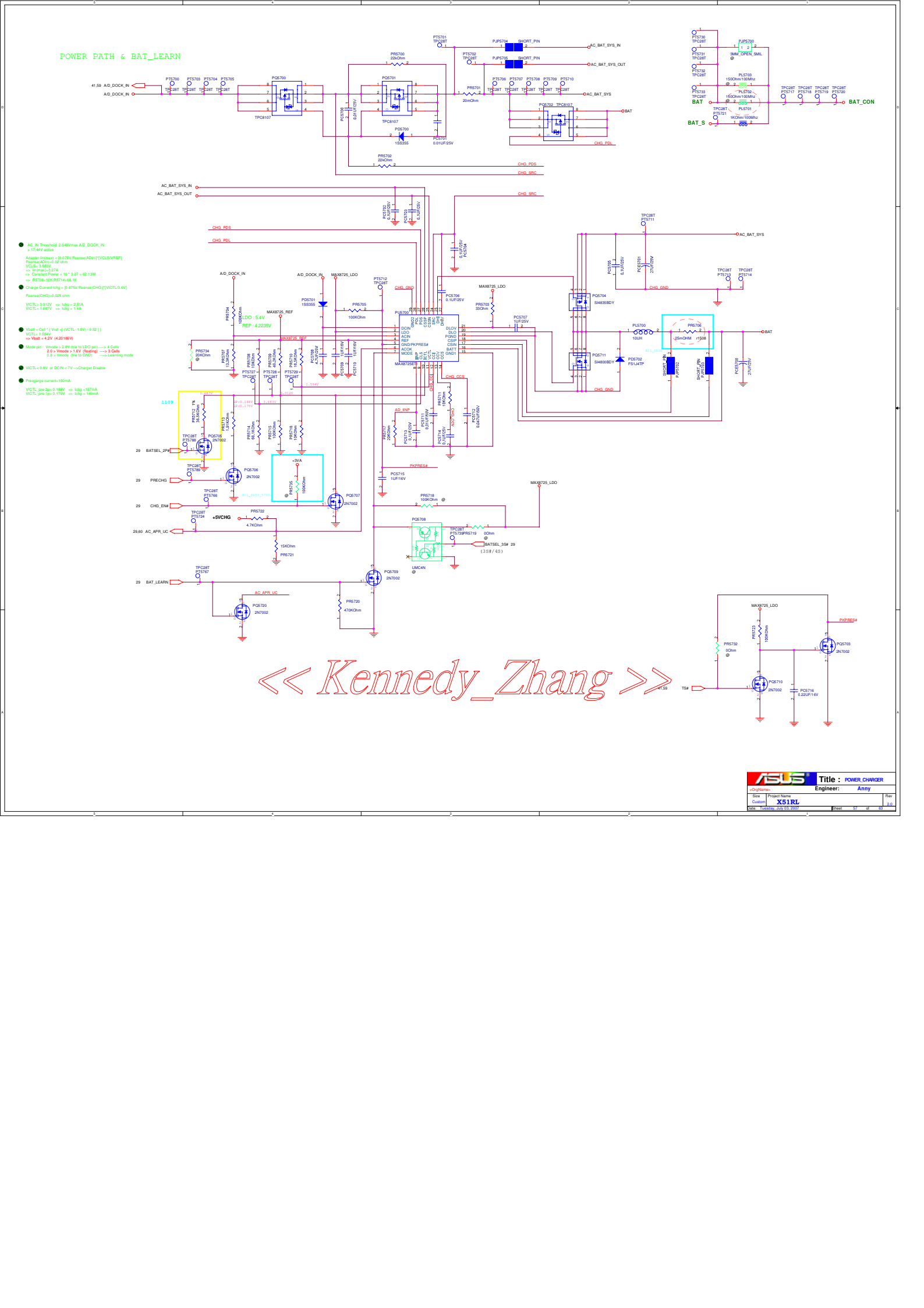


+2.5VS



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer: Anny	
Size: Custom	Project Name: X51RL	Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 54 of 63	

<< Kennedy_Zhang >>



- AC_IN Threshold 2.048Vmax A/D_DOCK_IN
  > 17.44V active

  Adapter Iin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
  Rsense(ADin)=0.02 ohm
  VCLS= 3.683V
  => Iin(max)=3.27A
  => Constant Power = 19 * 3.27 = 62.13W
  => R5708=10K,R5714=68.1K
- Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]

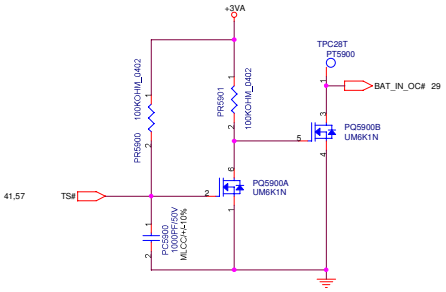
  Rsense(CHG)=0.025 ohm

  VICTL= 3.012V => Ichg = 2.51A
  VICTL= 1.687V => Ichg = 1.4A
- Vbatt = Cell * [Vref =[(VCTL- 1.6V) / 9.52]]
  VCTL= 1.584V
  => Vbatt = 4.2V (4.20186V)
- Mode pin : Vmode >.2.8V (Irie to LDO pin) ----> 4 Cells
  2.0 > Vmode >1.6V (floating) ----> 3 Cells
  0.8 > Vmode (Irie to GND) ----> Learning mode
- VICTL< 0.8V or DCIN < 7V ->Charger Disable
- Precgarge current=150mA

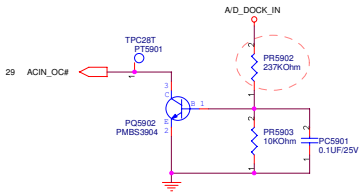
  VICTL_pre-2p= 0.188V => Ichg =157mA
  VICTL_pre-1p= 0.179V => Ichg = 149mA

ASUS	Title : POWER_CHARGER		
<OrgName>	Engineer: Anny		
Size: Custom	Project Name: X51RL		Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 57 of 60		

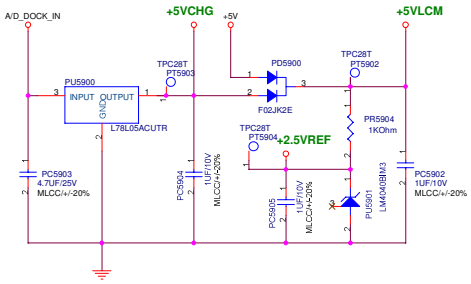
BATTERY IN DETECT



ADAPTER IN DETECT

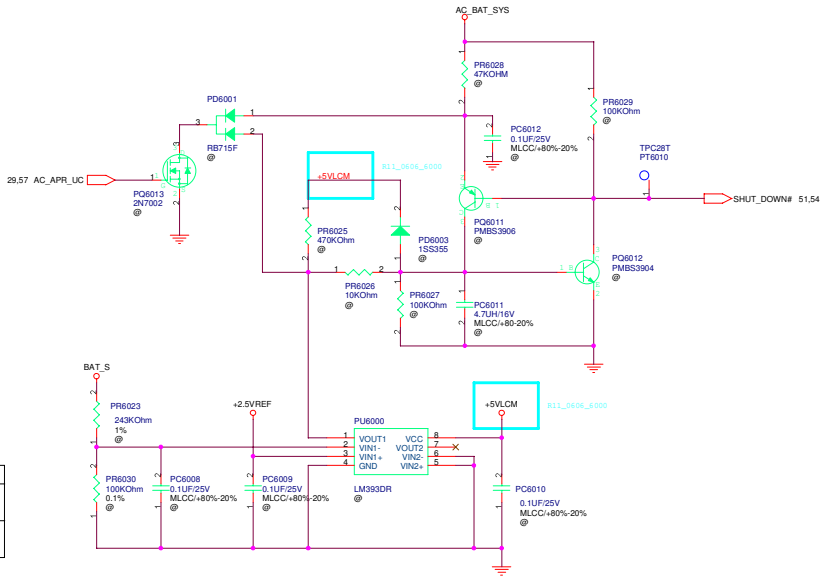


+5VLCM, +5VCHG & +2.5VREF



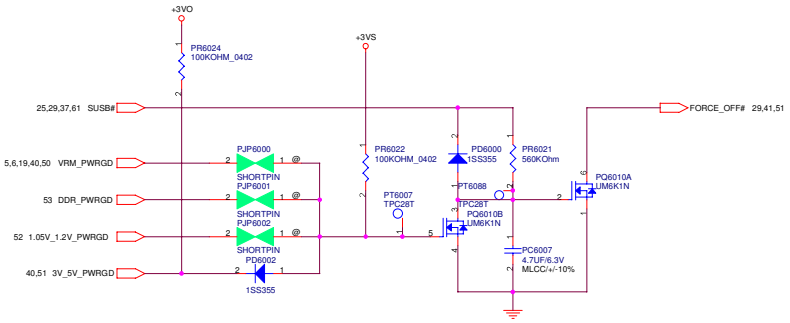
ASUS	Title : POWER_DETECT		
<OrgName>	Engineer: Anny		
Size: Custom	Project Name: X51RL		Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 59 of 63		

<< Kennedy_Zhang >>



	8.575V	11.625V
R6023	243KOhm 10G2132433130 30 1%	365KOhm 10G2133653130 10 1%
R6024	100KOhm 10G2131003230 10 0.1%	100KOhm 10G2131003230 10 0.1%

POWER GOOD DETECTER

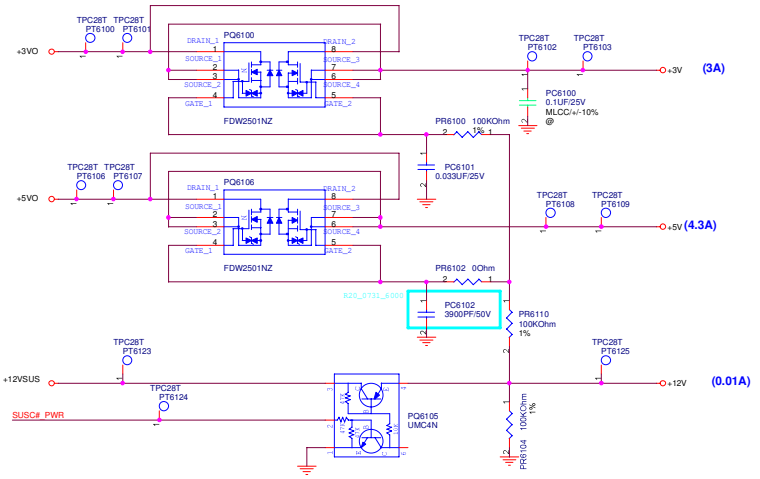


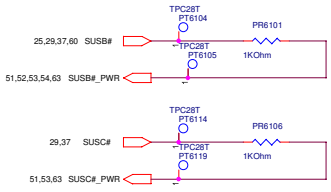
TPC28T PT6003 1 VRM_PWRGD
TPC28T PT6004 1 DDR_PWRGD
TPC28T PT6005 1 3V_5V_PWRGD
TPC28T PT6006 1 1.05V_1.2V_PWRGD

Title : POWER_PROTECT			
<OrgName>	Engineer: Anny		
Size: Custom	Project Name: X51RL		Rev: 2.0
Date: Tuesday, July 03, 2007	Sheet 60 of 63		

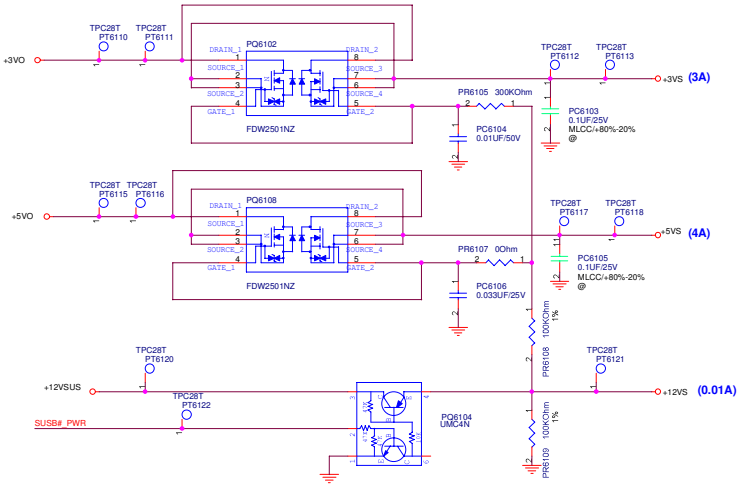
<< Kennedy_Zhang >>

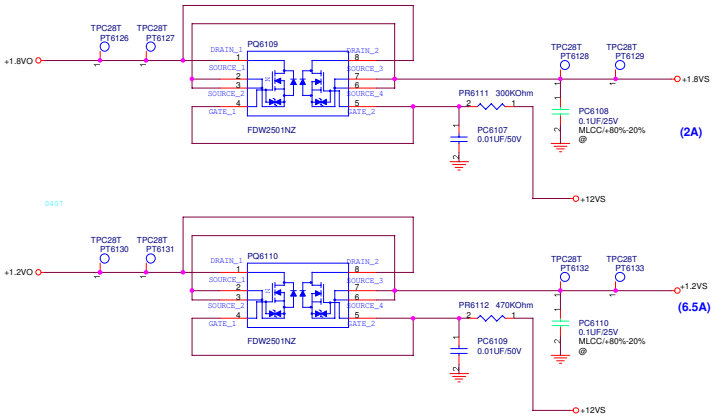
SUSC#_PWR POWER





SUSB#_PWR POWER





Title : POWER_LOAD SWITCH			
<OrgName>	Engineer: Anny		
Size: Custom	Project Name: X51RL		Rev: 2.0
Date: Tuesday, July 03, 2007		Sheet 61 of 63	

AC_BAT_SYS
+3VA
+5VA
+5VO
+3VO
+3VSUS
+5VSUS
+3V
+3VS

+12VSUS
+12V
+12VS

+5V
+5VS

+1.2VO
+1.2VSUS
+1.2VS
+1.8VO
+1.8V

+VCCP

+0.9VS
BAT
+5VCHG
+5VLCM
+2.5VREF
+VCORE

BAT_CON

AC_BAT_SYS 12,41,50,51,52,53,54,57,60
+3VA 12,17,29,38,40,54,57,59
+5VA 9,37,51,54
+5VO 51,52,53,61
+3VO 51,52,60,61
+3VSUS 6,17,19,20,23,25,29,34,40,51
+5VSUS 30,51
+3V 17,25,26,27,31,35,37,42,43,44,61
+3VS 2,4,5,9,12,13,14,15,17,18,19,20,21,22,23,25,26,28,29,31,32,33,34,37,39,40,42,43,50,52,60,61

+12VSUS 51,61
+12V 23,36,37,54,61
+12VS 12,33,37,61

+5V 12,25,30,36,37,38,44,59,61
+5VS 4,13,20,22,23,28,29,30,37,38,50,61

+1.2VO 52,61
+1.2VSUS 20,52
+1.2VS 6,7,9,10,20,37,61
+1.8VO 53,61
+1.8V 8,10,14,15,16,37,53

+VCCP 3,5,6,10,17,19,20,52

+0.9VS 16,37,53
BAT 57
+5VCHG 57,59
+5VLCM 59,60
+2.5VREF 54,59,60
+VCORE 3,50

BAT_CON 41,57

FOR POWER TEST

+3VA

PJP6300
1 2 2
SGL_JUMP
@
CPU_VRON_PWR 50

PJP6301
1 2 2
SUSB#_PWR
SGL_JUMP
@
SUSB#_PWR 51,52,53,54,61

PJP6302
1 2 2
SUSC#_PWR
SGL_JUMP
@
SUSC#_PWR 51,53,61

PJP6303
1 2 2
VSUS_ON_PWR
SGL_JUMP
@
VSUS_ON_PWR 51

Title : POWER_SIGNAL
<OrgName> Engineer: Anny
Size: Custom | Project Name: X51RL | Rev: 2.0
Date: Tuesday, July 03, 2007 | Sheet 63 of 63

<< Kennedy_Zhang >>

R2.0

Item	Before	After	Reason	Owner	Date
R20_1109_50		Add PCE5001 PCE5005, PQ5002, PQ5004, PQ5005 and PQ5007	VCORE:CPU upgrade to merom reflash		2006.11.09
R20_1109_50	9.31K	11K	VCORE: PR5030 modify to 11K to Increase OCP.		2006.11.09
R20_1109_57	PR5712 and PQ5705 were unmounted	PR5712:36.5K and PQ5705 was mounted.	Charger: Modify PR5712 and PQ5705 for 3S1P select.		2006.11.09

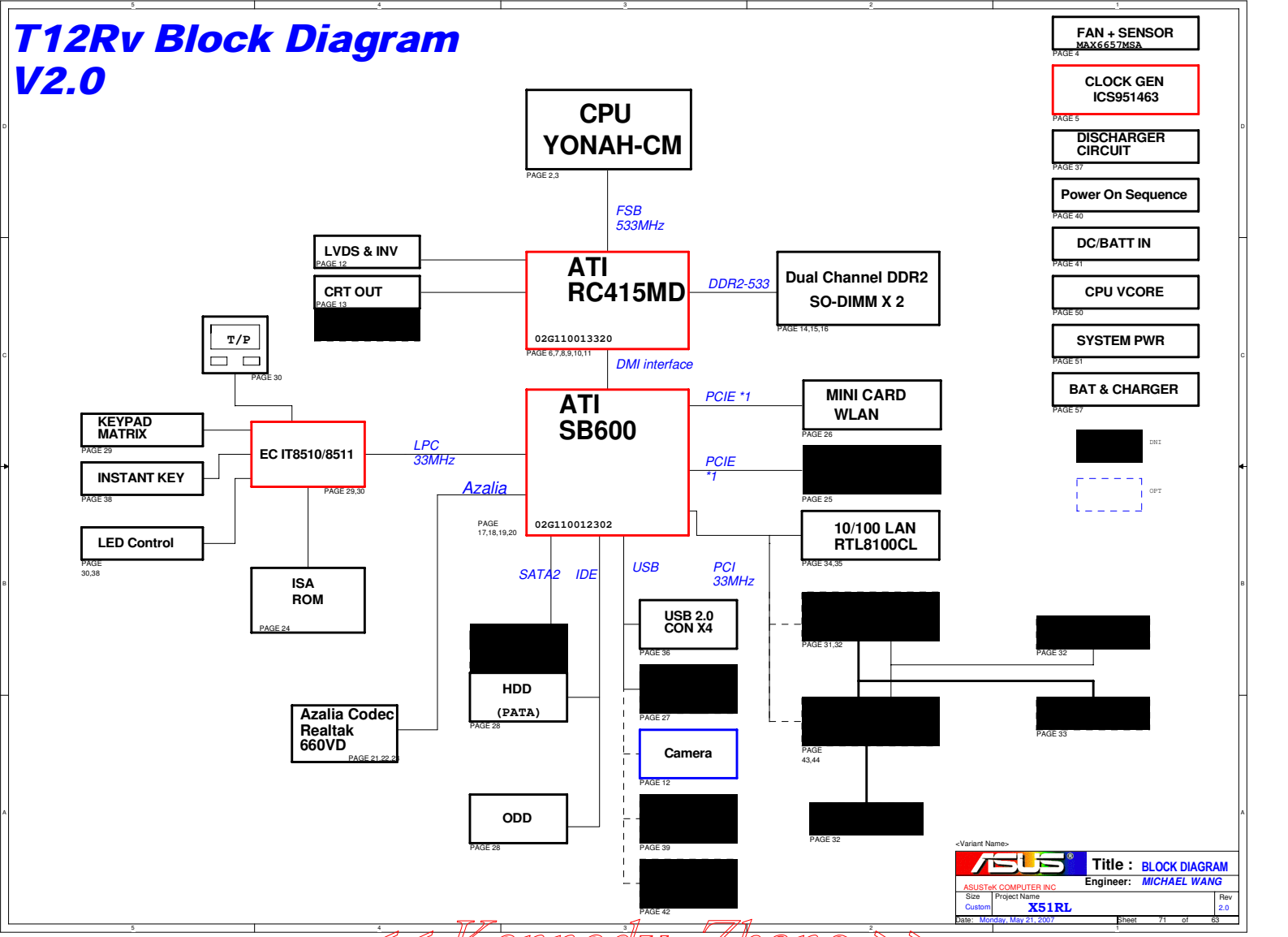
Title : POWER_PIC

<OrgName> Engineer:

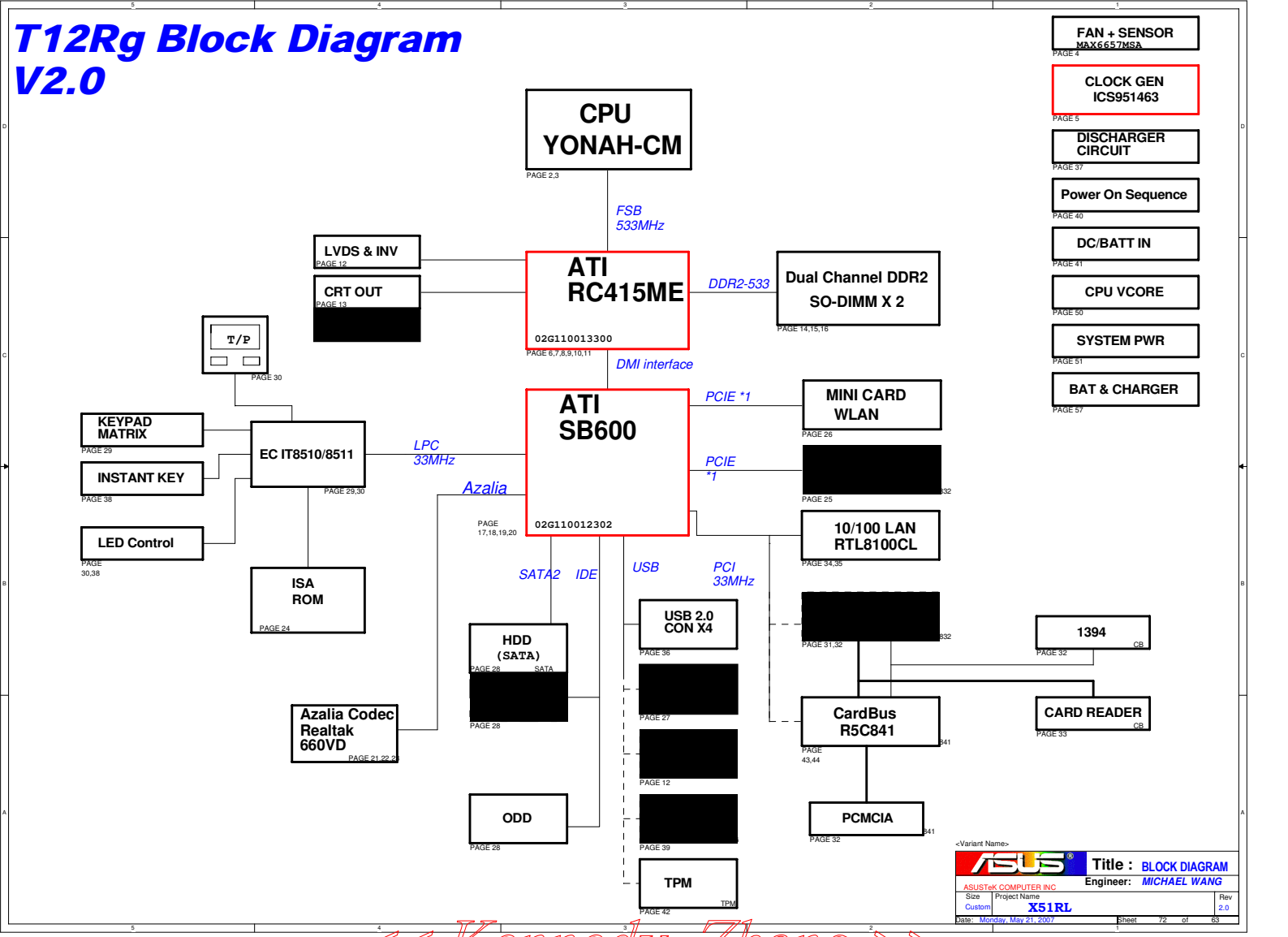
Size	Project Name	Rev
Custom	X51RL	2.0

Date: Monday, May 21, 2007 Sheet 64 of 63

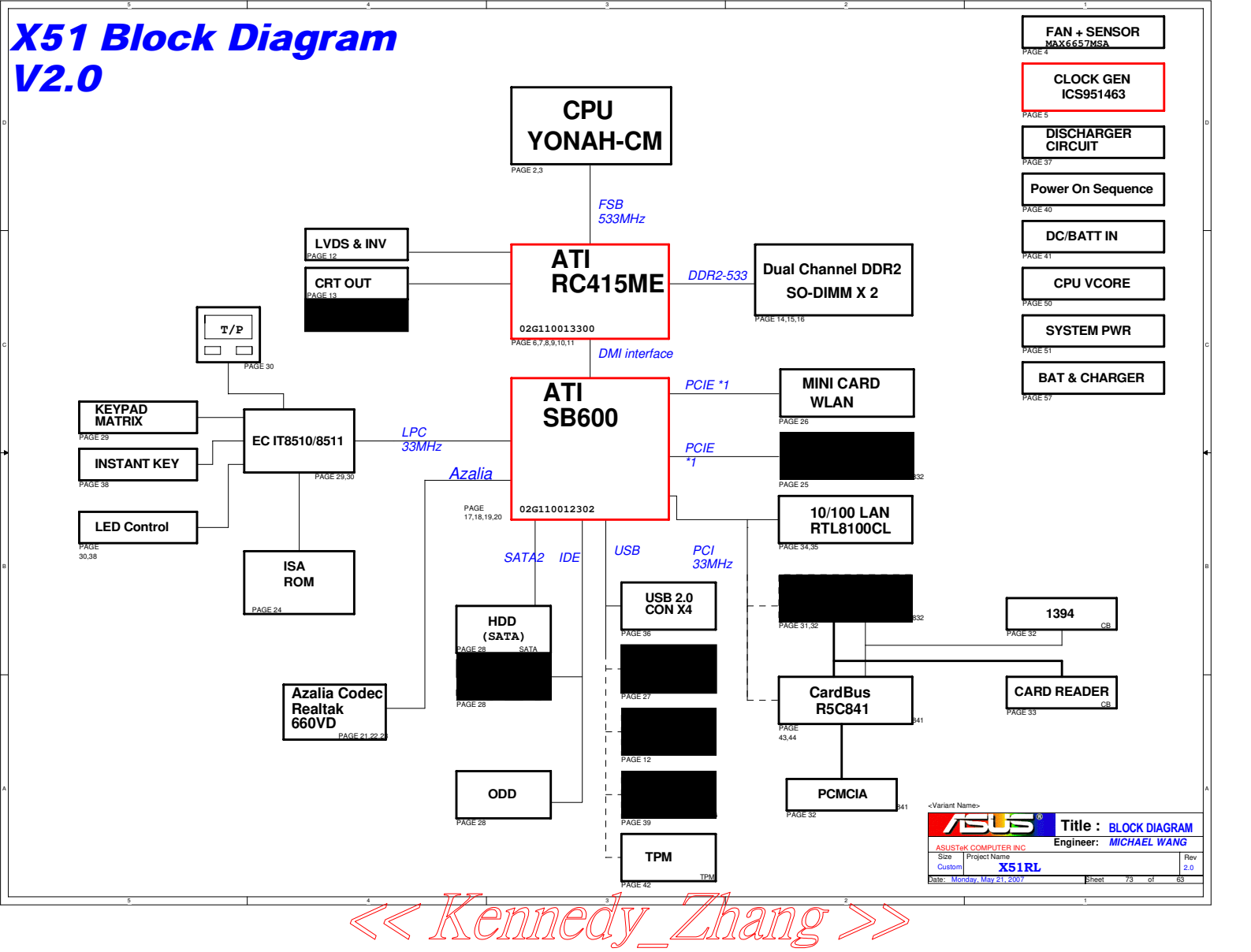
T12Rv Block Diagram V2.0



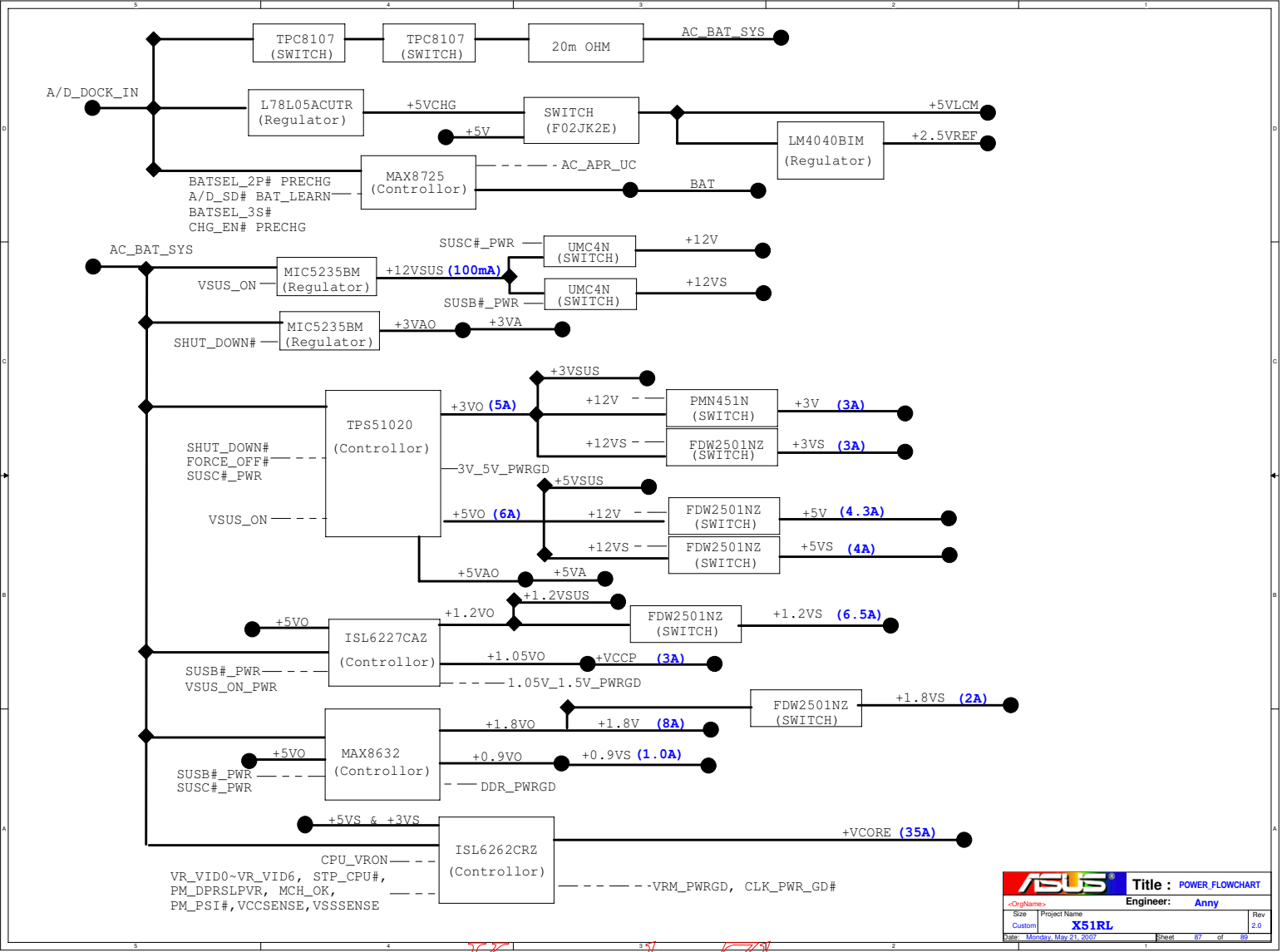
T12Rg Block Diagram V2.0



X51 Block Diagram V2.0



<< Kennedy_Zhang >>



<< Kennedy_Zhang >>