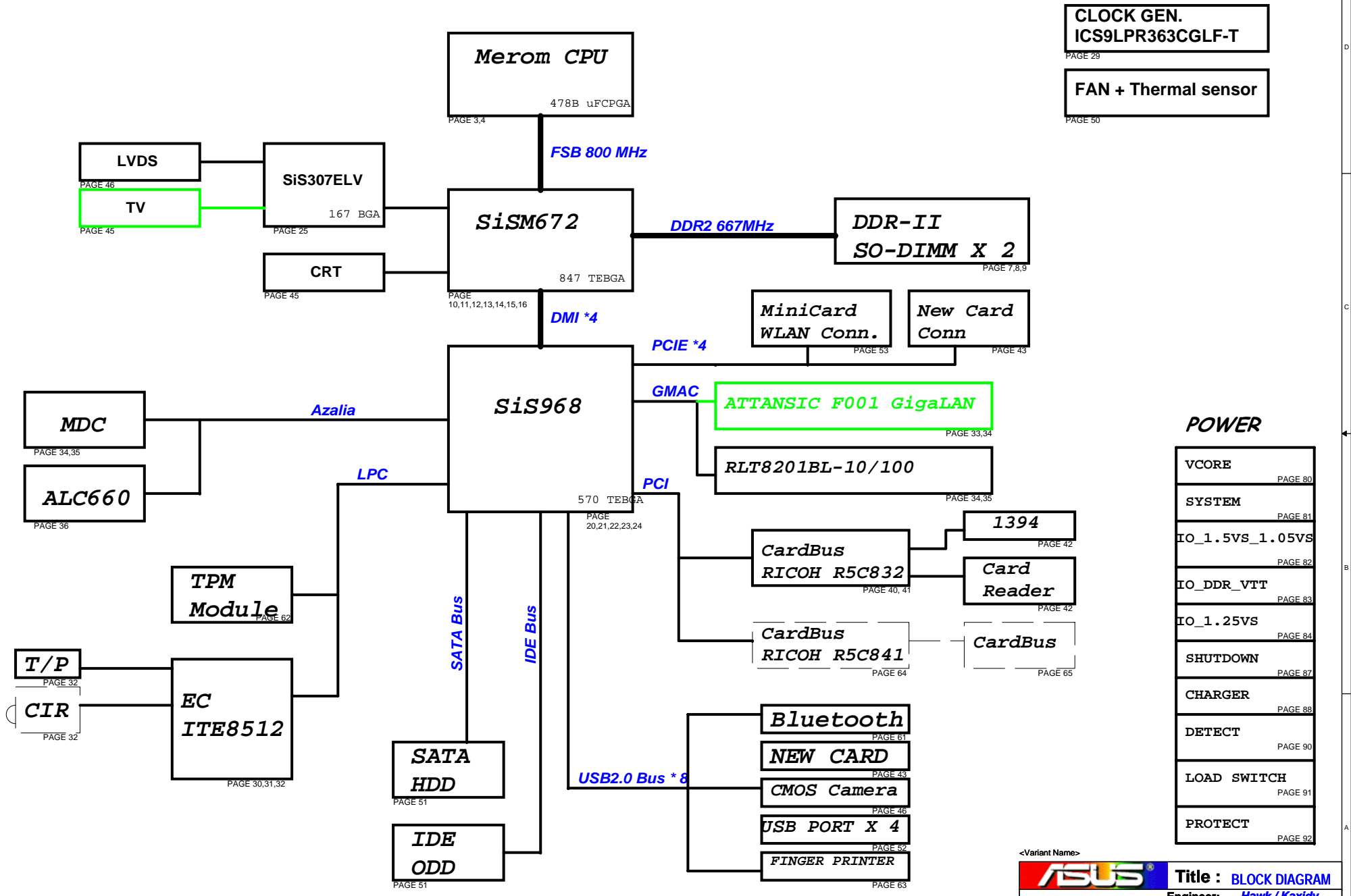


X51C Main BD. R1.0 BLOCK DIAGRAM

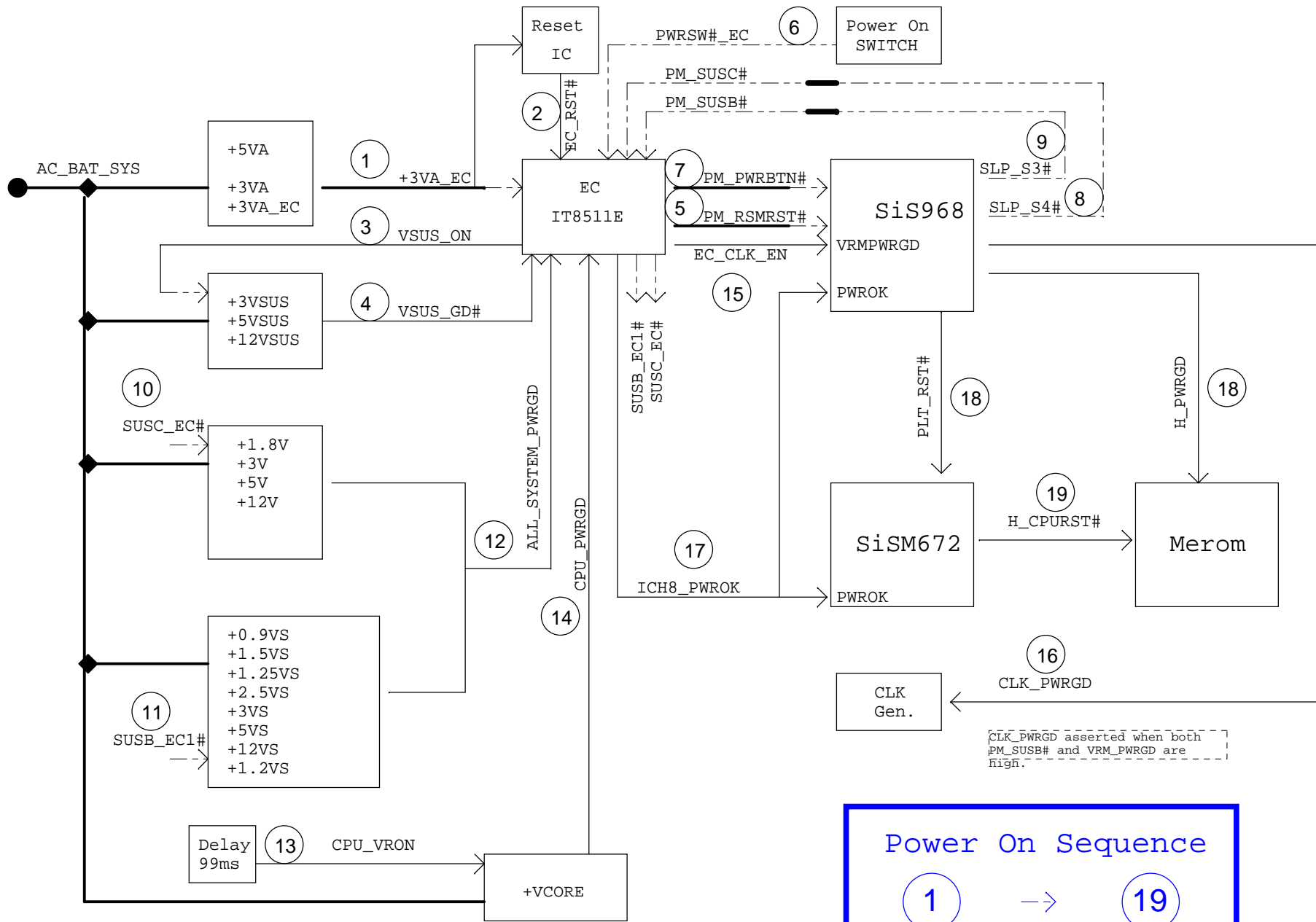


CLOCK GEN.
ICS9LPR363CGLF-T
PAGE 29

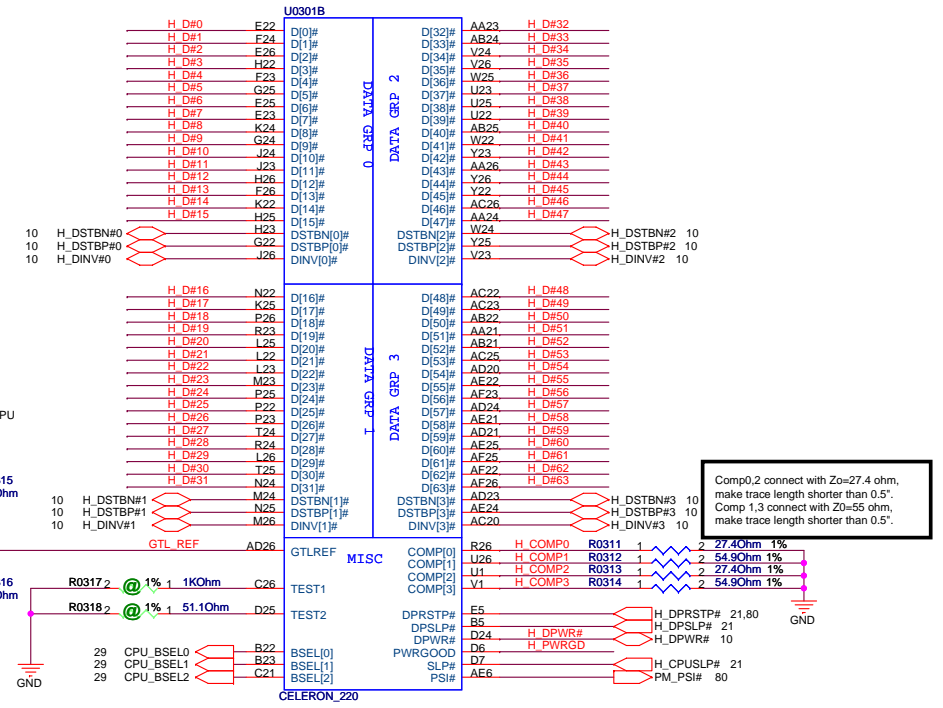
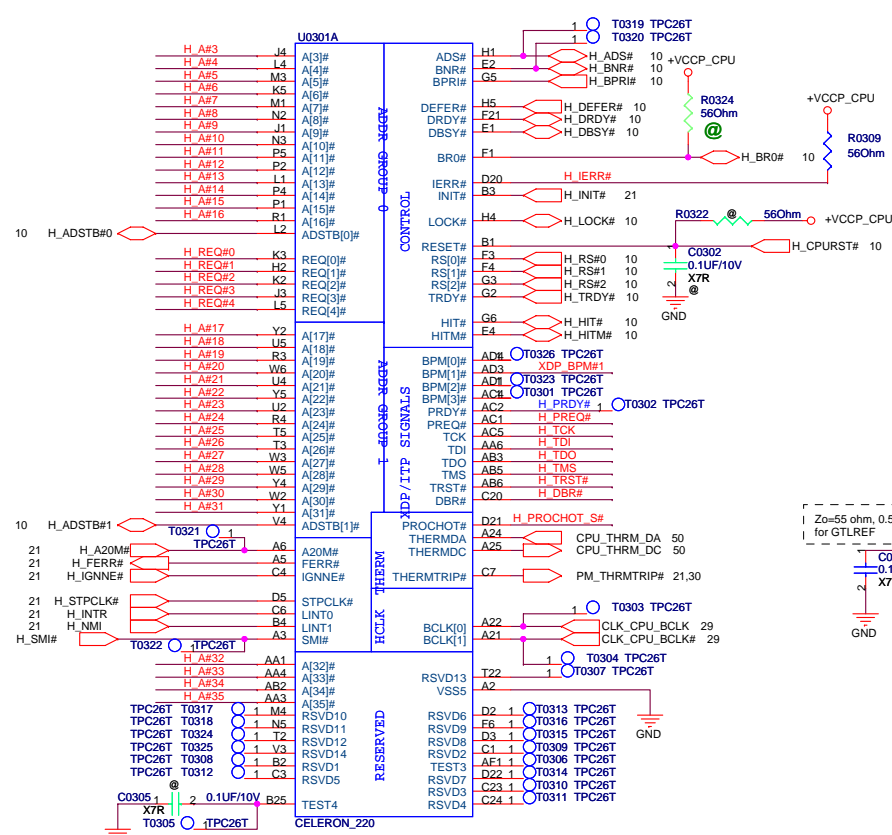
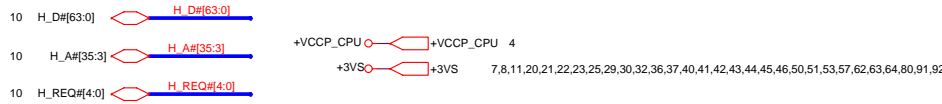
FAN + Thermal sensor
PAGE 50

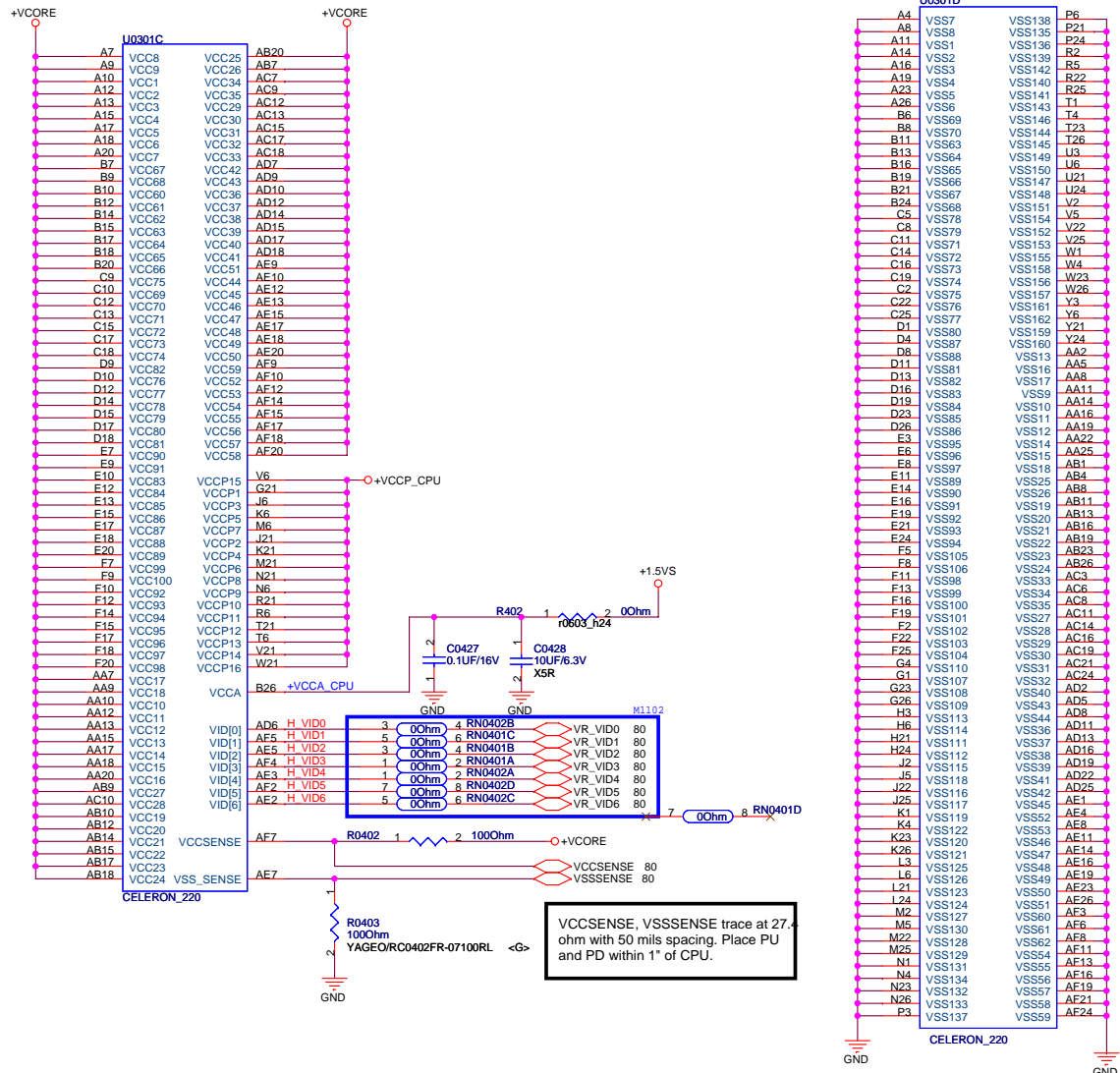
POWER

VCORE	PAGE 80
SYSTEM	PAGE 81
IO_1.5VS_1.05VS	PAGE 82
IO_DDR_VTT	PAGE 83
IO_1.25VS	PAGE 84
SHUTDOWN	PAGE 87
CHARGER	PAGE 88
DETECT	PAGE 90
LOAD SWITCH	PAGE 91
PROTECT	PAGE 92



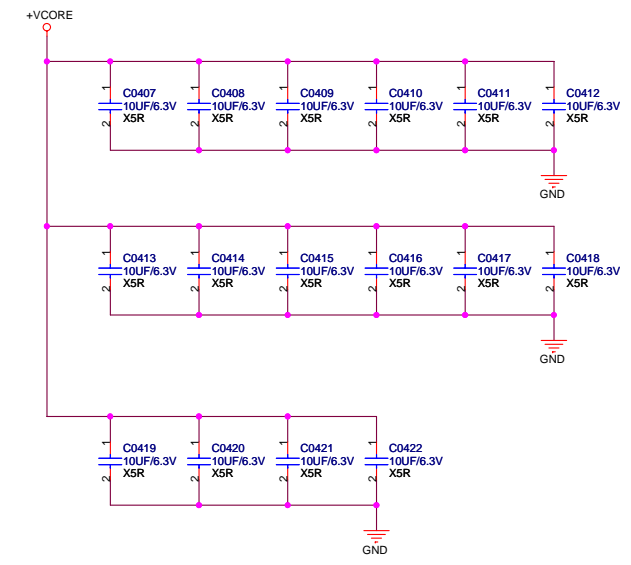
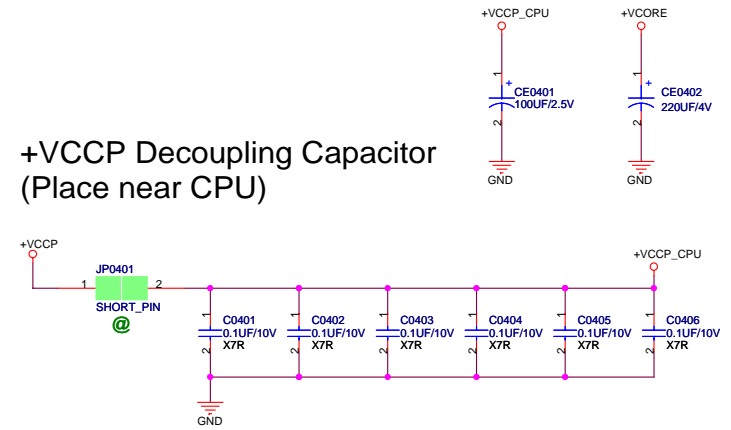
Power On Sequence
1 → 19





VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.

+VCCP Decoupling Capacitor (Place near CPU)



5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>



Title : NULL

ASUSTeK COMPUTER INC

Engineer: Hawk / Kaxidy

Size	Project Name	Rev
A	T12C	1.1

Date: Monday, August 13, 2007

Sheet 5 of 94

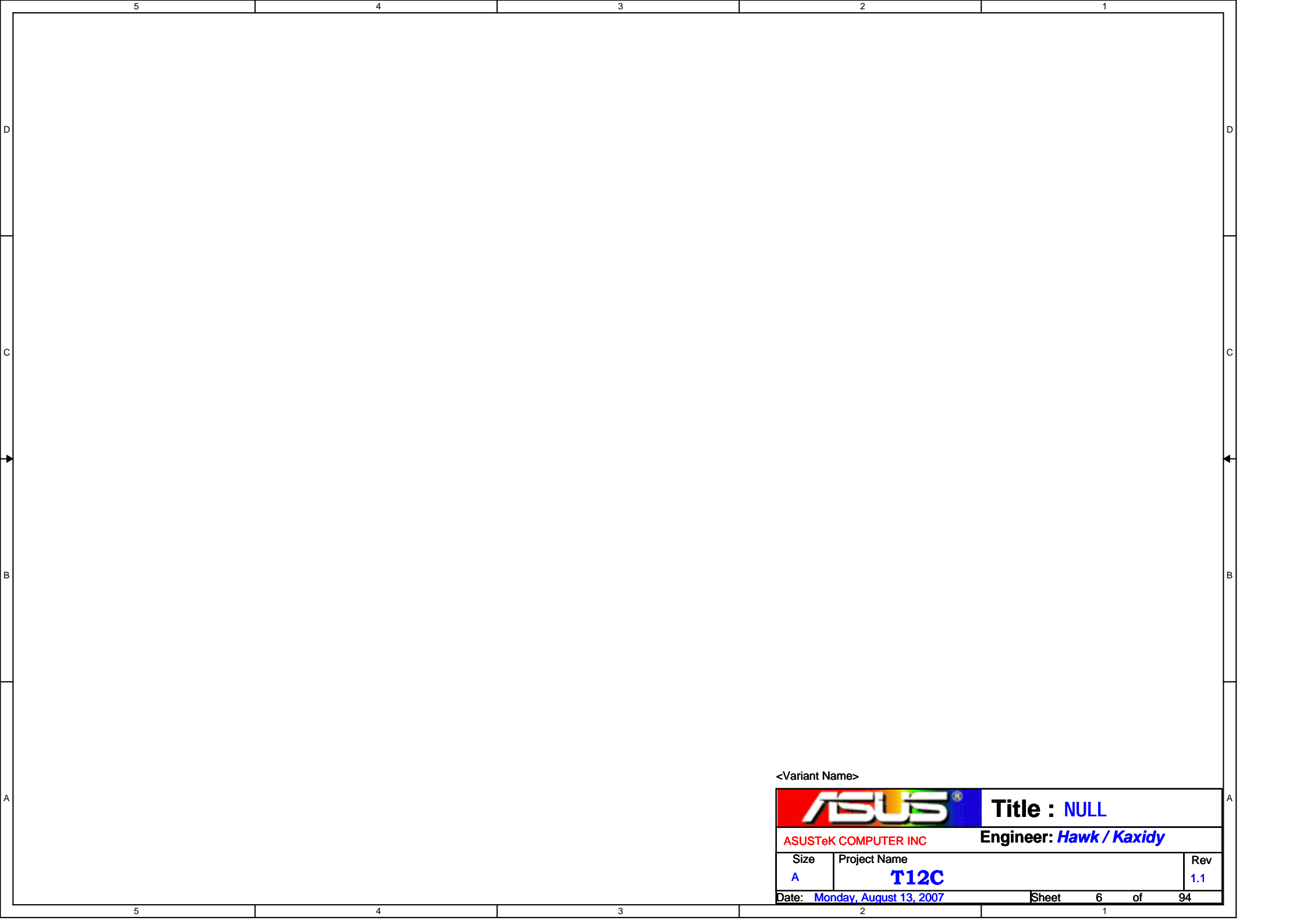
5

4


3

2

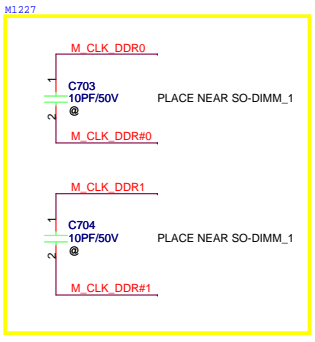
1



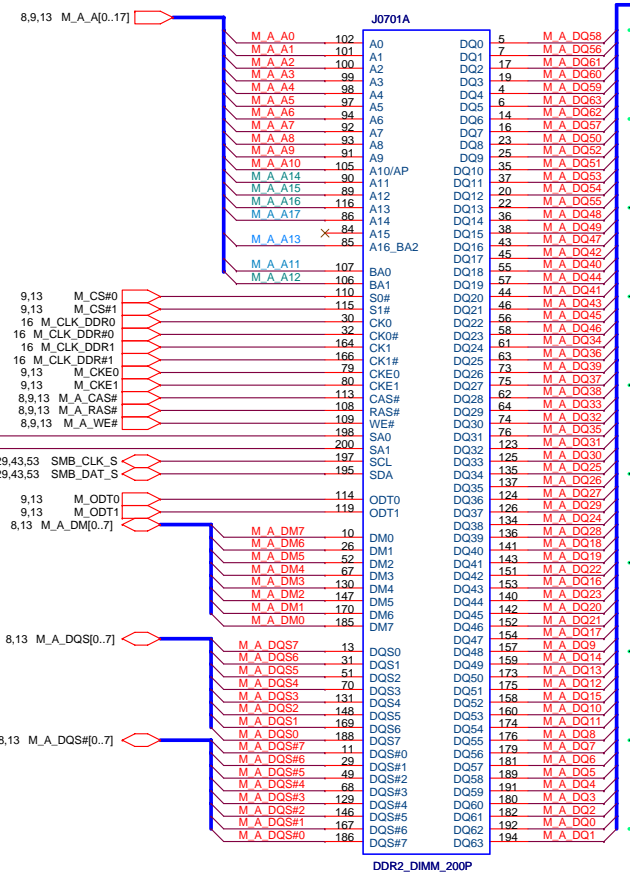
<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy
Size	Project Name	Rev
A	T12C	1.1
Date: Monday, August 13, 2007		Sheet 6 of 94

P/N: 12G025022004
(T12F) 4.0mm, STD

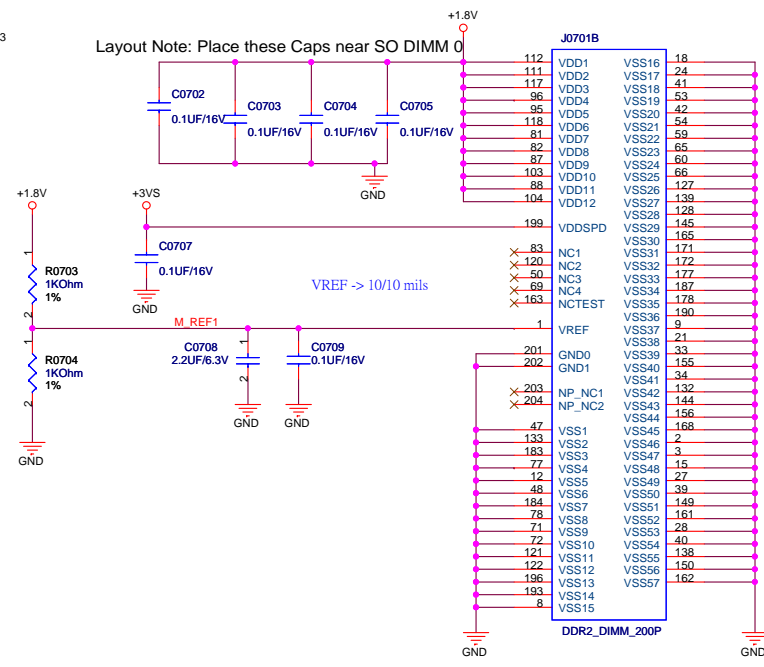


SMBus Slave Address: A0H

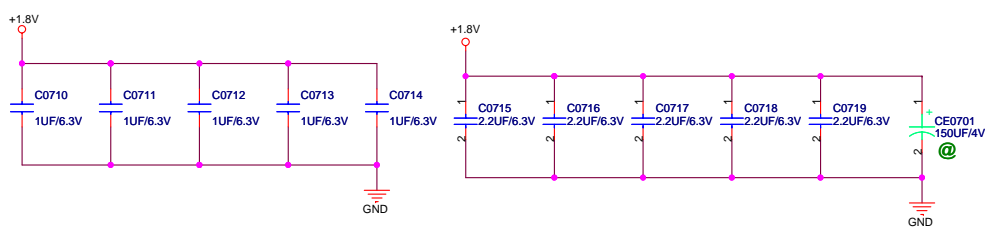


SO-DIMM 0 is placed farther from the GMCH than SO-DIMM 1

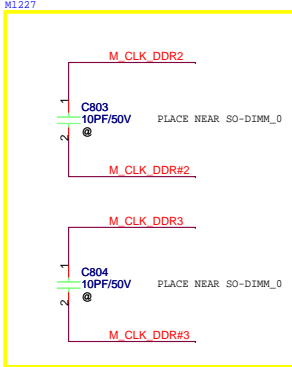
Layout Note: Place these Caps near SO DIMM 0



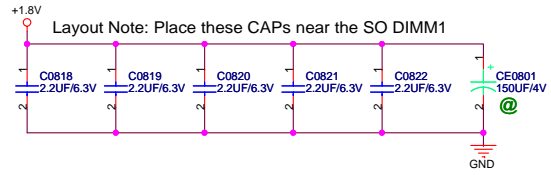
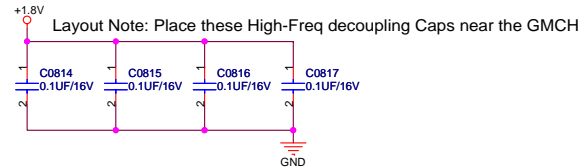
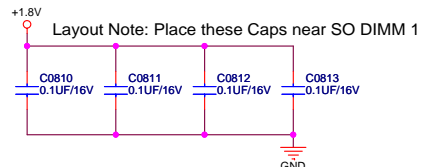
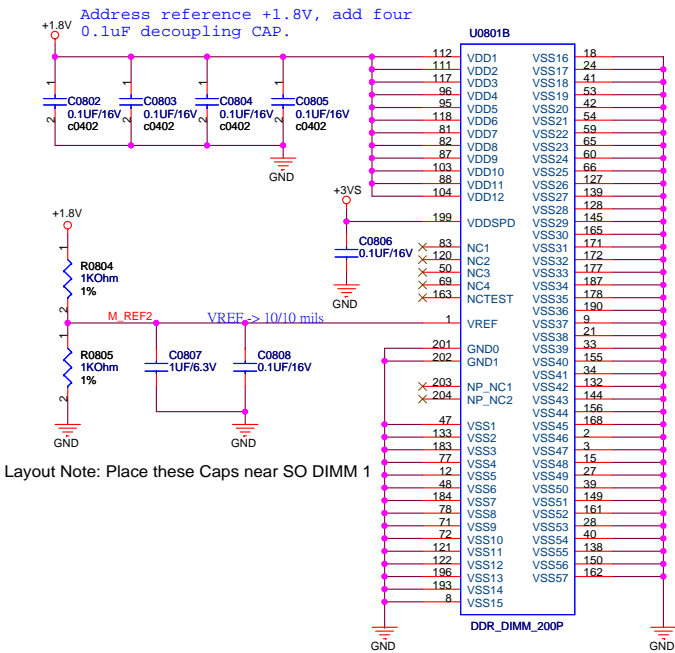
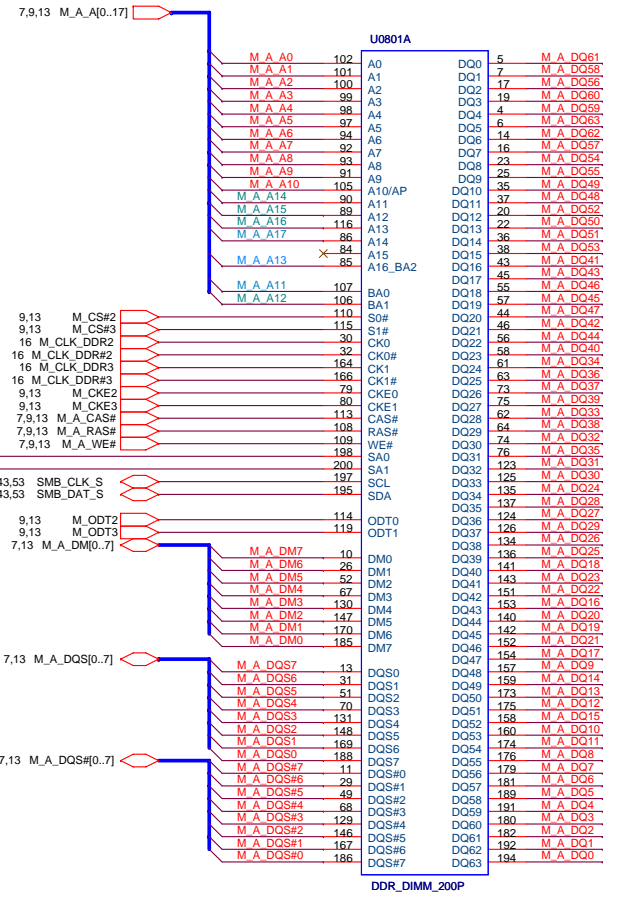
Layout Note: Place these Caps near SO DIMM 0

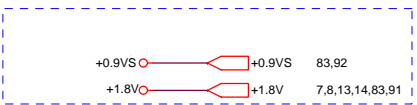
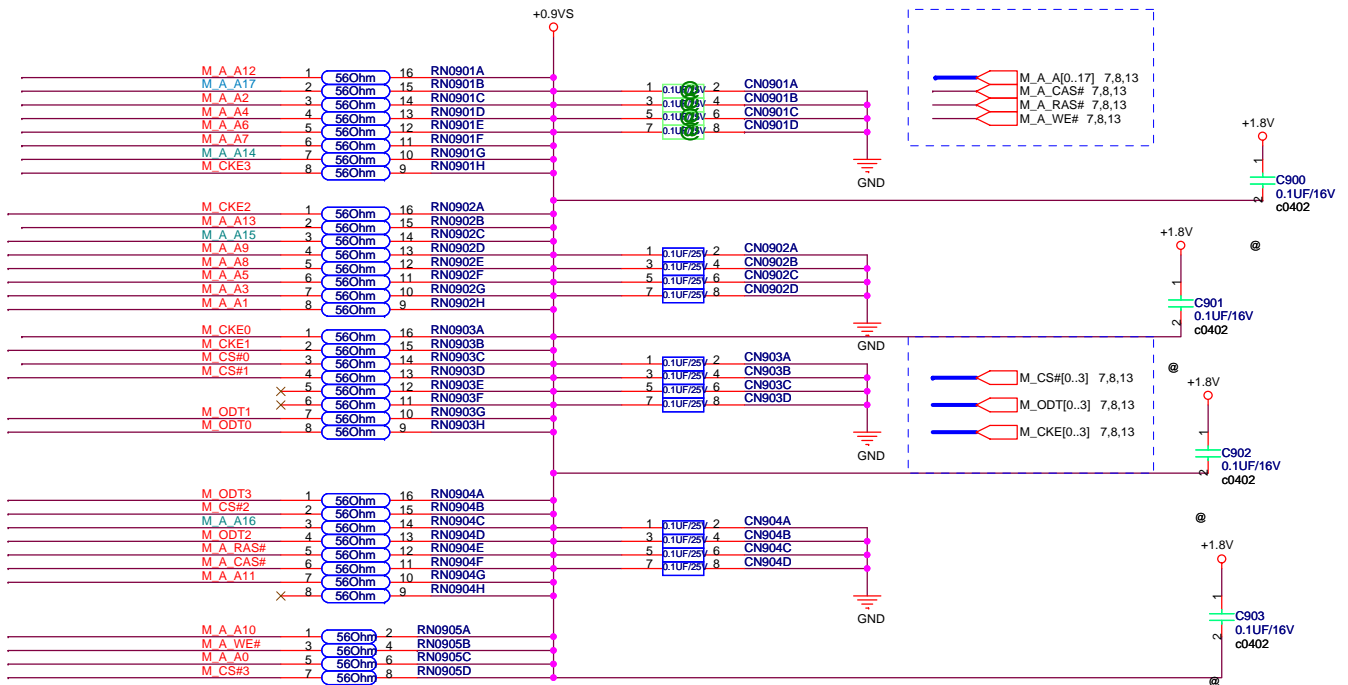


<Variant Name>



P/N: 12G025C22000 S:12G025C22004
(T12F) 9.2mm, STD



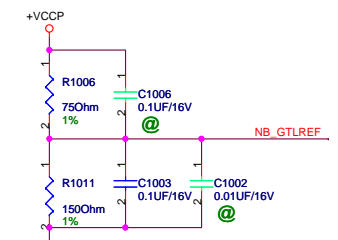


Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS

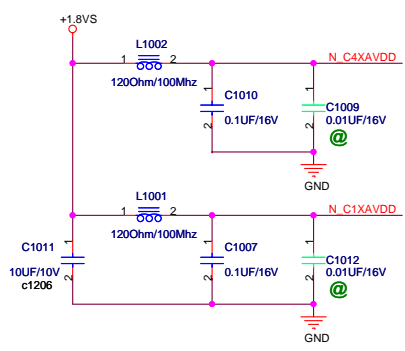
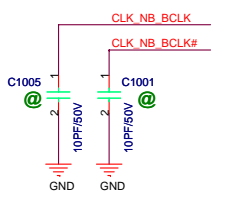
<Variant Name>

ASUS		Title : DDR2 TERM	
ASUSTeK COMPUTER INC.ETD		Engineer: <i>Hawk / Kaxidy</i>	
Size Custom	Project Name T12C	Date: Tuesday, February 26, 2008	Rev 1.1
Date: Tuesday, February 26, 2008		Sheet	9 of 94

+VCCP $\frac{\circ}{\text{---}}$ +VCCP 4.14,21,23,29,57,83,92
 +1.8VS $\frac{\circ}{\text{---}}$ +1.8VS 11,13,14,16,20,21,22,23,25,91



Layout Note:
0.1uF should be placed 100mils or less from NB pin.

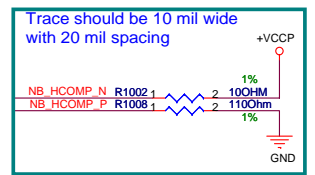
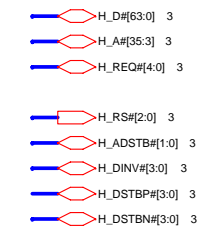


Total Power mW (Max)		
1.8VS	N_C1XAVDD	10mA
	N_C4XAVDD	1.2mA

10mA N_C1XAVDD B16
 1.2mA N_C4XAVDD A17

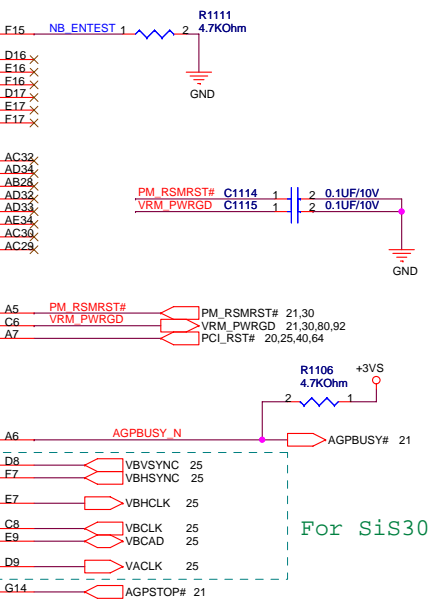
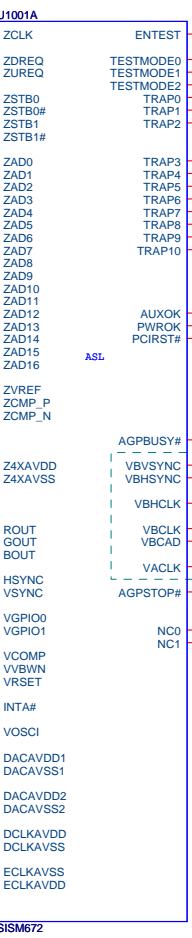
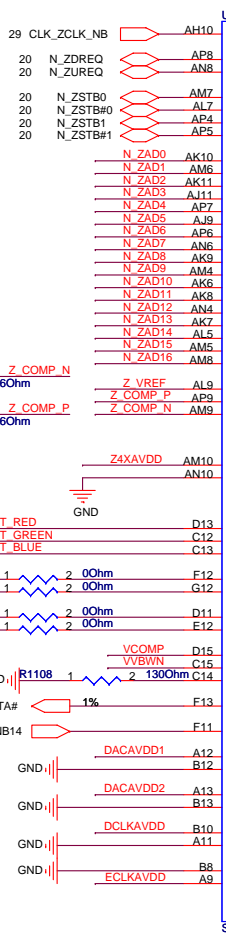
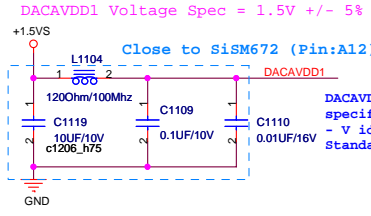
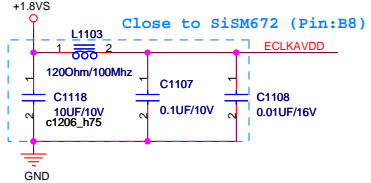
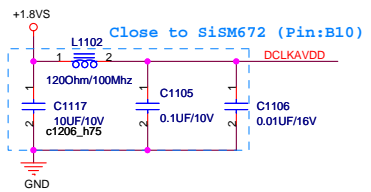
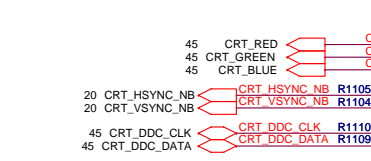
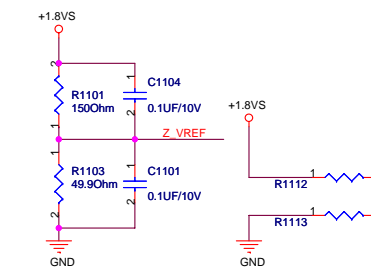
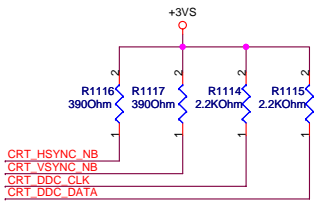
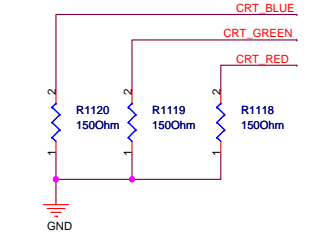
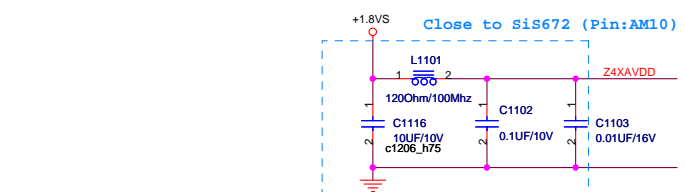
U1001C

C1XAVDD	B16	HD0#	H D#0
C1XAVSS	C17	HD1#	M30 H D#1
C4XAVDD	A17	HD2#	M28 H D#2
C4XAVSS	B18	HD3#	L30 H D#3
HVREF1	W24	HD4#	L29 H D#4
HVREF2	U24	HD5#	K28 H D#5
HVREF3	R24	HD6#	K31 H D#6
HVREF4	N24	HD7#	K30 H D#7
HVREF5	L21	HD8#	H31 H D#8
		HD9#	G34 H D#9
		HD10#	H32 H D#10
		HD11#	G32 H D#11
		HD12#	K32 H D#12
		HD13#	F34 H D#13
		HD14#	F33 H D#14
		HD15#	F32 H D#15
		HD16#	H28 H D#16
		HD17#	J30 H D#17
		HD18#	H30 H D#18
		HD19#	G29 H D#19
		HD20#	J29 H D#20
		HD21#	G30 H D#21
		HD22#	F30 H D#22
		HD23#	D33 H D#23
		HD24#	D34 H D#24
		HD25#	B32 H D#25
		HD26#	B33 H D#26
		HD27#	C34 H D#27
		HD28#	D31 H D#28
		HD29#	A31 H D#29
		HD30#	A32 H D#30
		HD31#	C31 H D#31
		HD32#	B30 H D#32
		HD33#	C30 H D#33
		HD34#	A30 H D#34
		HD35#	D28 H D#35
		HD36#	G28 H D#36
		HD37#	C29 H D#37
		HD38#	C28 H D#38
		HD39#	E28 H D#39
		HD40#	E27 H D#40
		HD41#	C27 H D#41
		HD42#	G26 H D#42
		HD43#	E26 H D#43
		HD44#	D26 H D#44
		HD45#	B26 H D#45
		HD46#	A26 H D#46
		HD47#	C26 H D#47
		HD48#	C24 H D#48
		HD49#	C24 H D#49
		HD50#	A25 H D#50
		HD51#	B24 H D#51
		HD52#	C25 H D#52
		HD53#	A24 H D#53
		HD54#	E23 H D#54
		HD55#	E25 H D#55
		HD56#	G24 H D#56
		HD57#	D22 H D#57
		HD58#	E22 H D#58
		HD59#	E22 H D#59
		HD60#	C23 H D#60
		HD61#	A23 H D#61
		HD62#	A22 H D#62
		HD63#	B22 H D#63
		DBI0#	J32 H DINV#0
		DBI1#	E32 H DINV#1
		DBI2#	F27 H DINV#2
		DBI3#	F23 H DINV#3
		HDSTB#0	H33 H DSTB#0
		HDSTB#1	E31 H DSTB#1
		HDSTB#2	B28 H DSTB#2
		HDSTB#3	D24 H DSTB#3
		HDSTB#0	H34 H DSTB#0
		HDSTB#1	D32 H DSTB#1
		HDSTB#2	A28 H DSTB#2
		HDSTB#3	E24 H DSTB#3
		HPCOMP	A21 NB_HCOMP P
		HNCOMP	C21 NB_HCOMP N



N_ZAD[16:0] 20

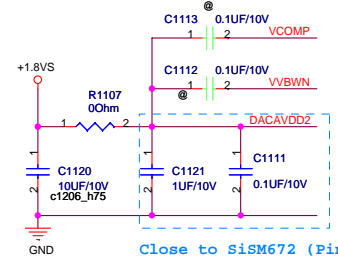
+1.8VS → +1.8VS 10,13,14,16,20,21,22,23,25,91
 +3VS → +3VS 3,7,8,20,21,22,23,25,29,30,32,36,37,40,41,42,43,44,45,46,50,51,53,57,62,63,64,80,
 +1.5VS → +1.5VS 4,43,53,57,83



For SiS307 Only

Total Power mW(Max)		
1.8VS	Z4XAVDD	10mA
1.8VS	DCLKAVDD	5mA
1.8VS	ECLKAVDD	5mA
1.5VS	DACA VDD1	73mA
1.8VS	DACA VDD2	73mA

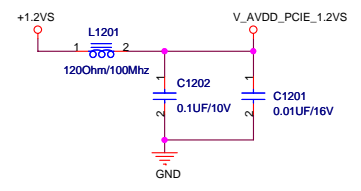
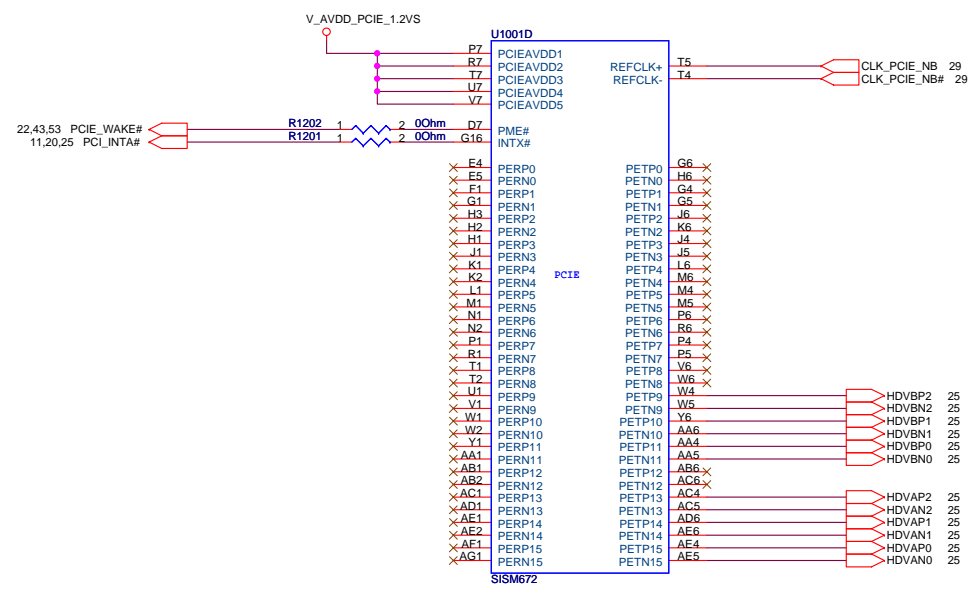
For improving ripple noise

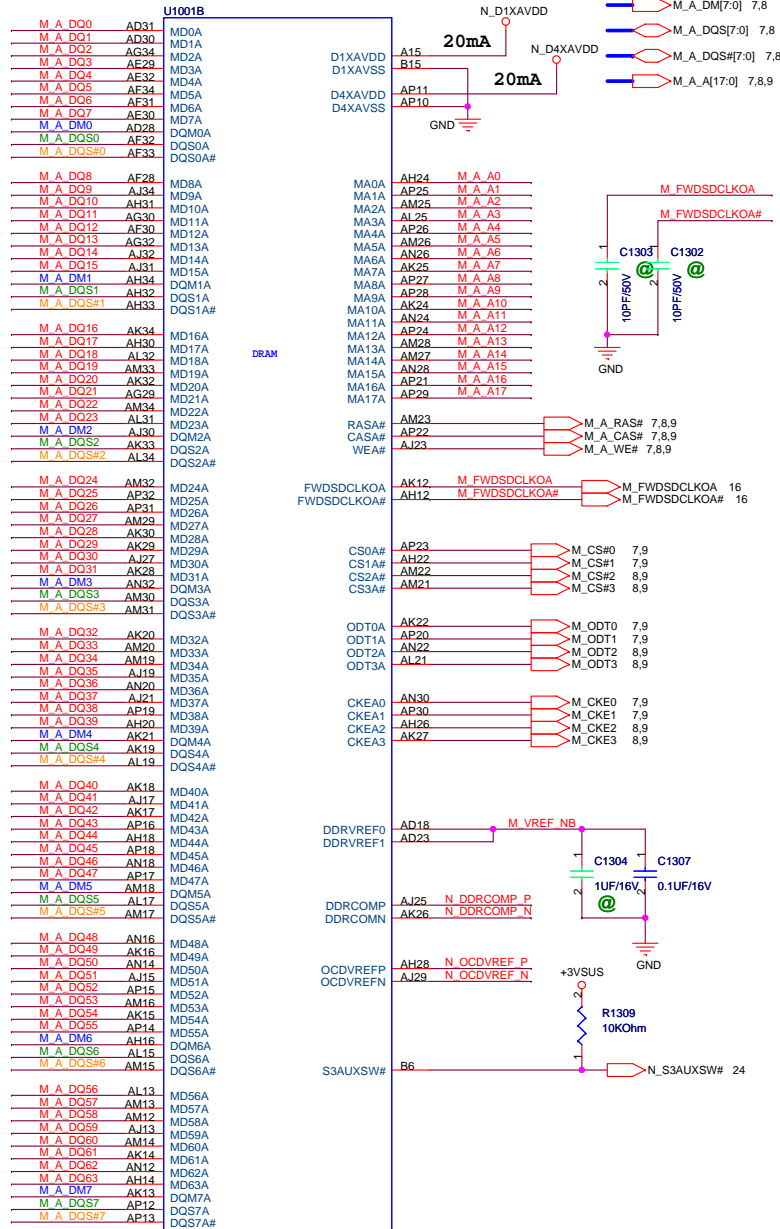


<Variant Name>

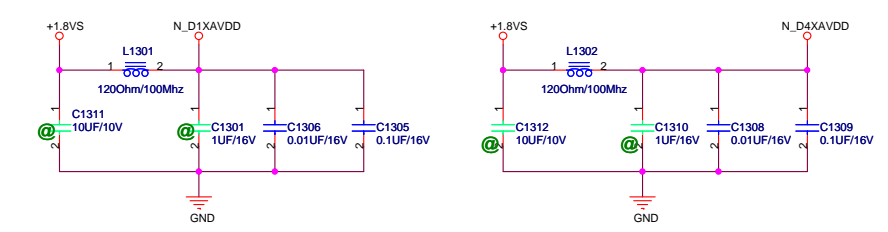
+1.2VS  +1.2VS 14.83,91

Total Power mW(Max)		
1.2V	V_AVDD_PCIE_1.2V	190mA

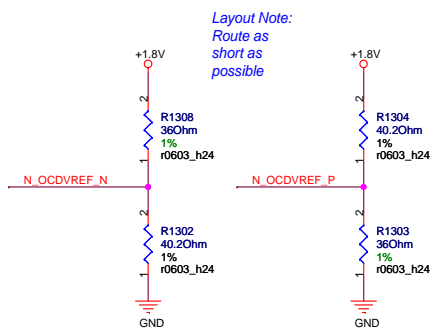
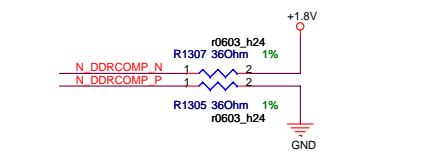
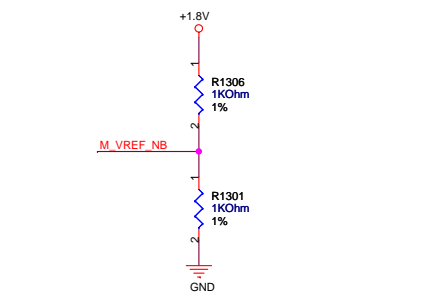




+3VSUS	+3VSUS	21,22,23,24,30,33,35,43,53,81,83,92
+1.8VS	+1.8VS	10,11,14,16,20,21,22,23,25,91
+1.8V	+1.8V	7,8,9,14,83,91



Total Power mW(Max)		
1.8VS	N_D1XAVDD	7mA
1.8VS	N_D4XAVDD	10mA



Layout Note:
Route as short as possible

SISM672

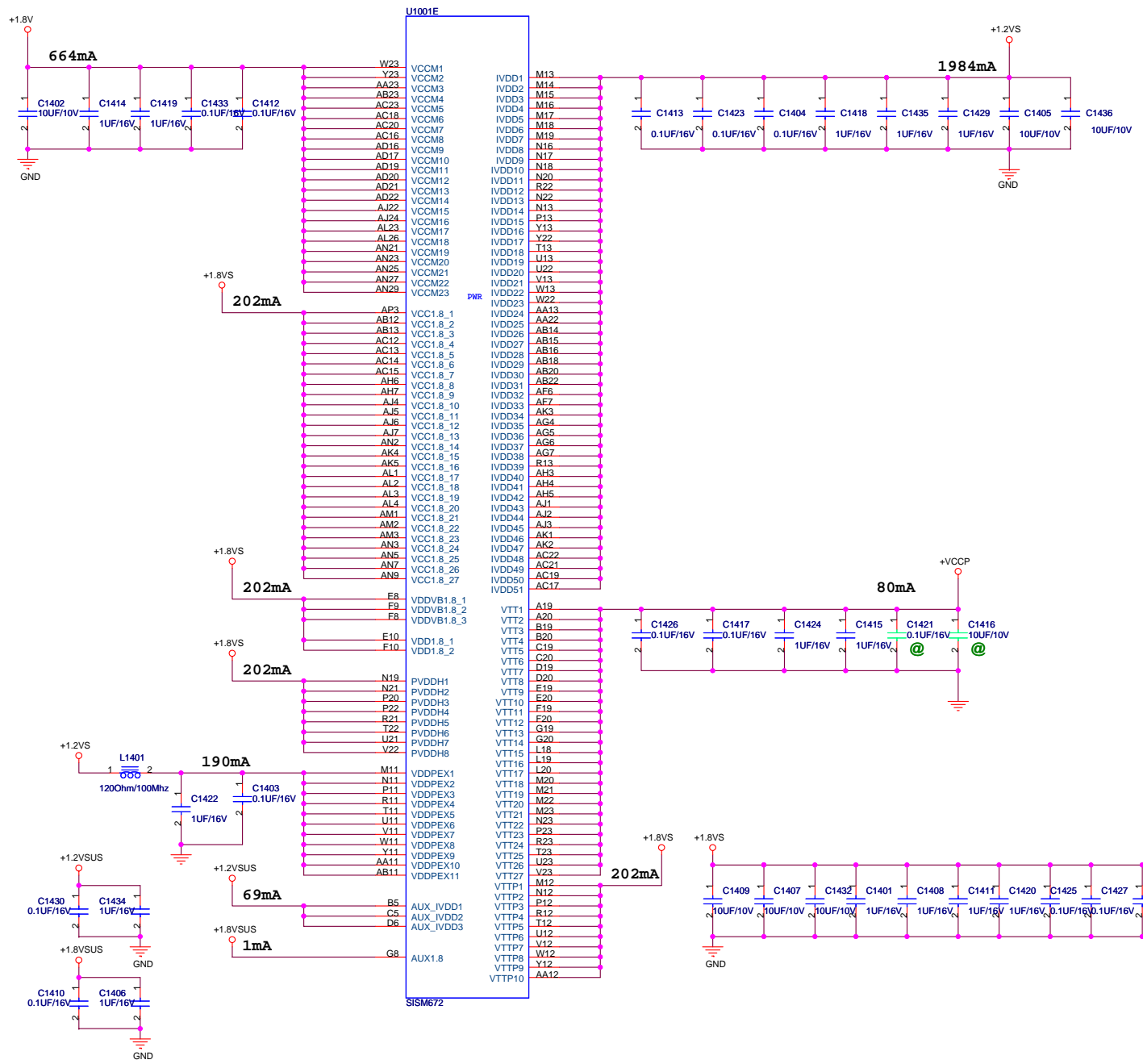
<Variant Name>

Title : NB-SISM672 (DDR2)

ASUSTeK COMPUTER INC. NB Engineer: **Hawk / Kaxidy**

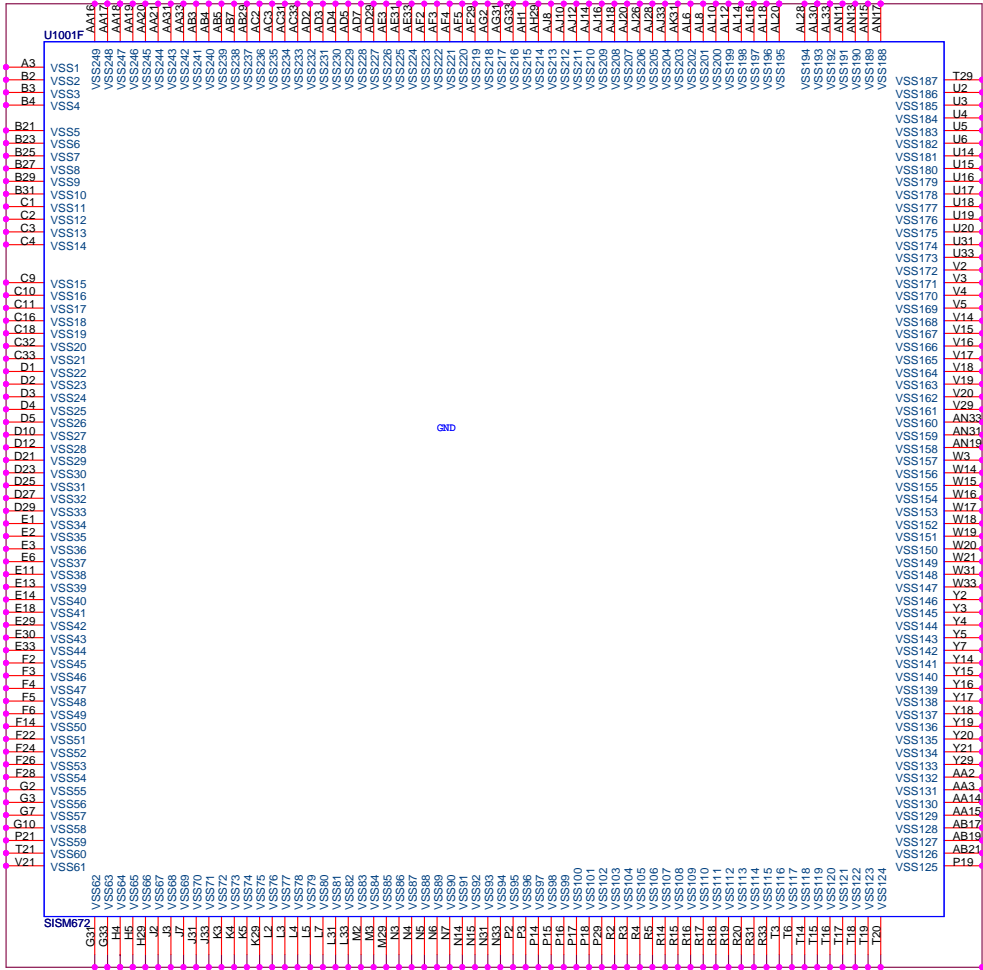
Size	Project Name	Rev
Custom	T12C	1.1

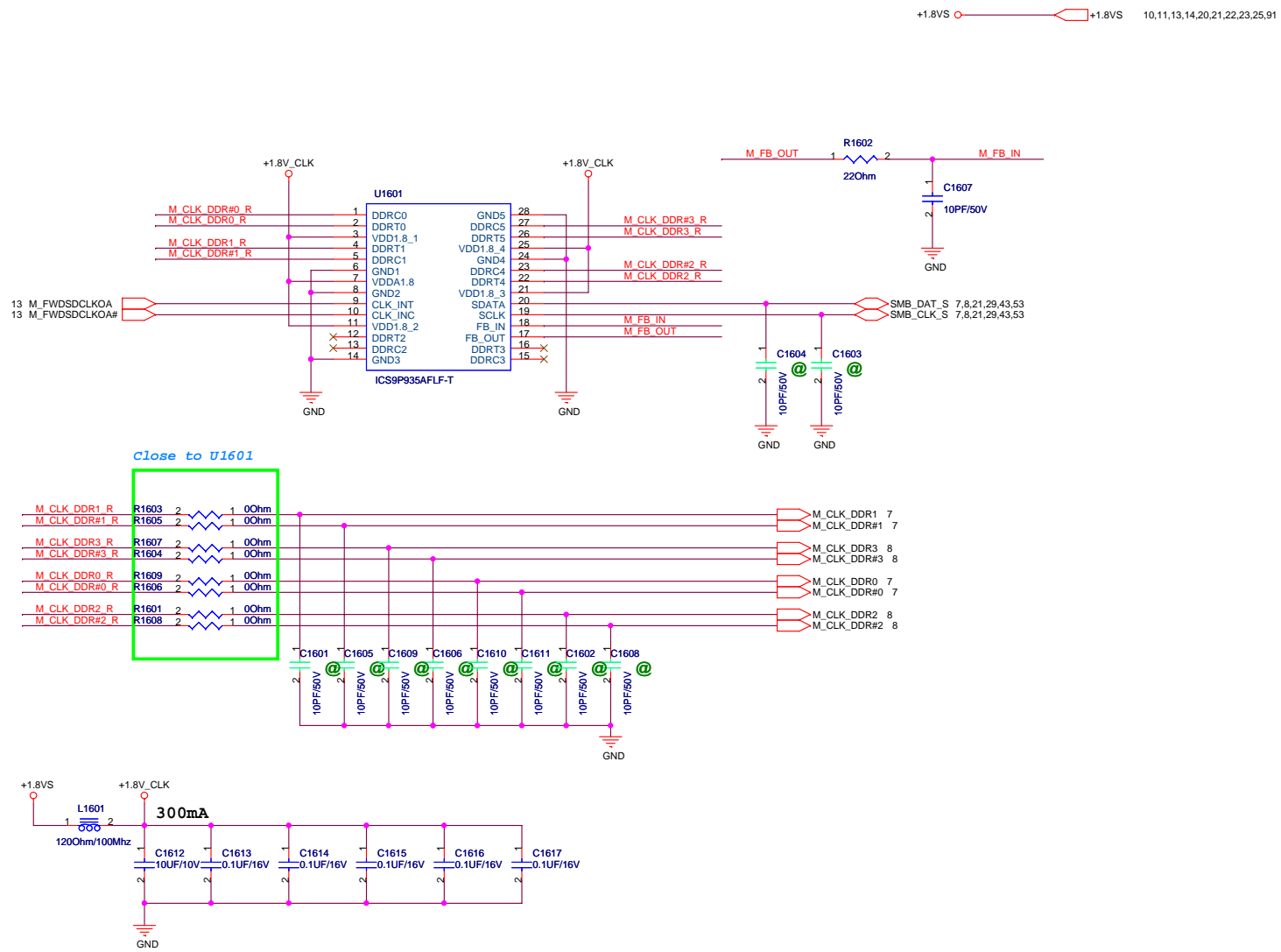
Date: Friday, August 17, 2007 Sheet 13 of 94



- +1.8VS +1.8VS 10,11,13,16,20,21,22,23,25,91
- +1.8V +1.8V 7,8,9,13,83,91
- +1.2VS +1.2VS 12,83,91
- +VCCP +VCCP 4,10,21,23,29,57,83,92
- +1.2VSUS +1.2VSUS 82
- +1.8VSUS +1.8VSUS 21,22,23,82

SiSM672 Total Power 4664mW (3D Mode)		
1.2VS	+1.2VS_NB	1984mA
1.8V	VCCM1-23	64mA
1.8VS	VCC1.8/VDDVB1.8/ VDD1.8/PVDDH/VTTP	202mA
+VCCP	VTT1-27 VDDPEX1-11	80mA 190mA





5

4

3

2

1

D

D

C

C


B

B

A

A

<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC.NB		Engineer: Hawk / Kaxidy
Size	Project Name	Rev
B	T12C	1.1
Date: <u>Monday, August 13, 2007</u>		Sheet 17 of 94

5

4

3

2

1

5

4

3

2

1

D

D

C

C


B

B

A

A

<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC .NB		Engineer: Hawk / Kaxidy
Size	Project Name	Rev
A	T12C	1.1
Date: Monday, August 13, 2007		Sheet 18 of 94

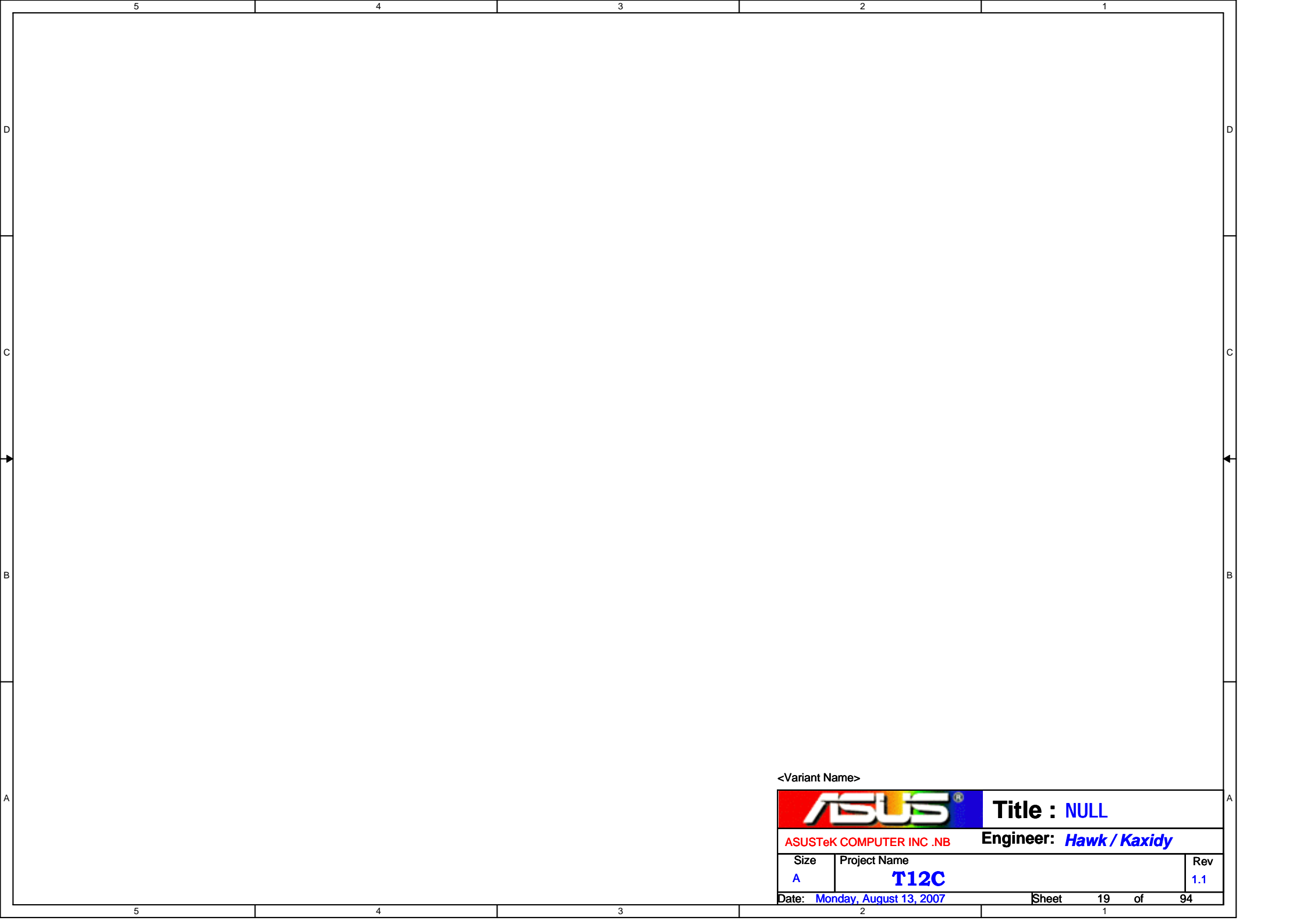
5

4


3

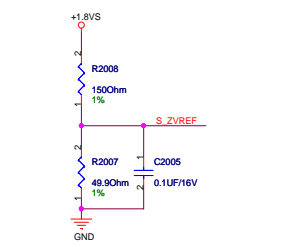
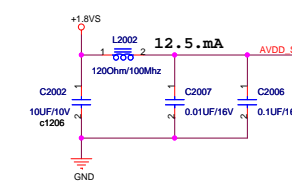
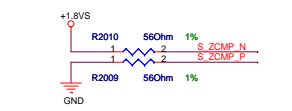
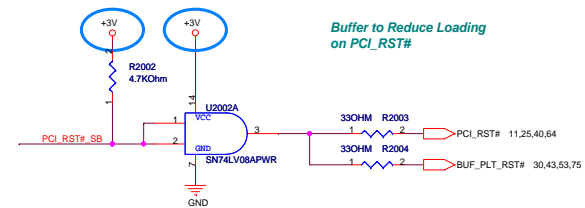
2

1



<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC .NB		Engineer: <i>Hawk / Kaxidy</i>
Size A	Project Name T12C	Rev 1.1
Date: <u>Monday, August 13, 2007</u>		Sheet 19 of 94



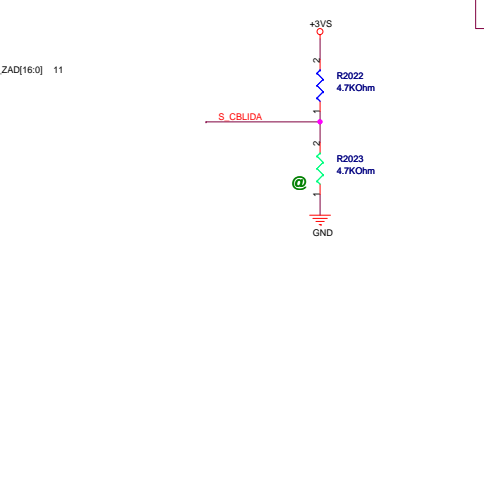
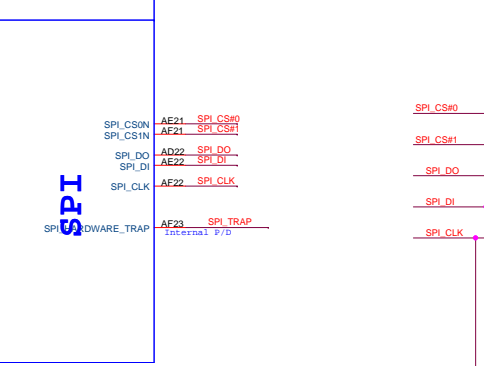
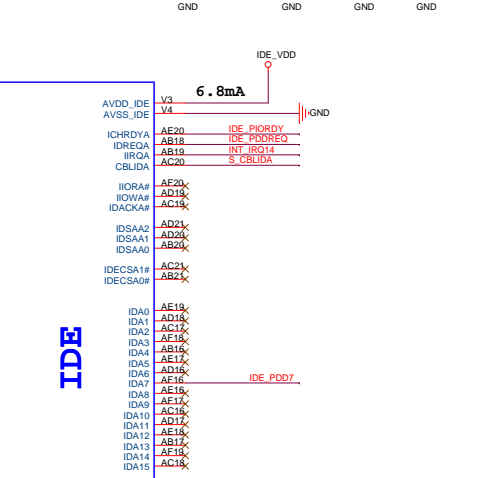
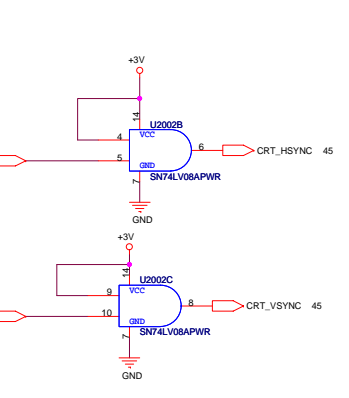
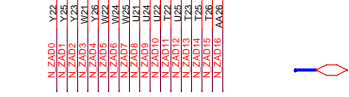
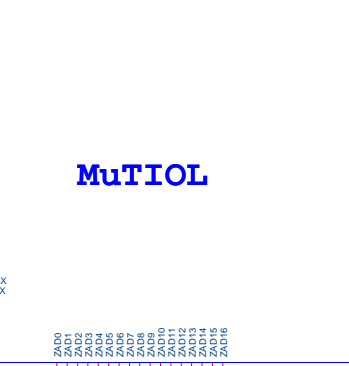
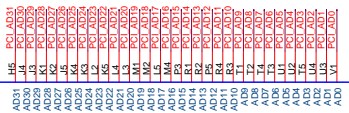
Buffer to Reduce Loading on PCI_RST#

- 40.64 PCI_RST# SB
- 40.64 PCI_REQ#0
- 40.64 PCI_GNT#0
- 40.64 PCI_CBE#3
- 40.64 PCI_CBE#2
- 40.64 PCI_CBE#1
- 40.64 PCI_CBE#0
- 11,12,25 PCI_INTA#
- 25,40,64 PCI_INTB#
- 40.64 PCI_INTC#
- 64 PCI_INTD#
- 40.64 PCI_FRAME#
- 40.64 PCI_IRDY#
- 40.64 PCI_TRDY#
- 40.64 PCI_STOP#
- 40.64 PCI_SERR#
- 40.64 PCI_PAR
- 40.64 PCI_DEVSEL#
- 29 CLK_SBPCL
- 29 CLK_ZCLK_SB
- 11 N_ZSTB0
- 11 N_ZSTB#0
- 11 N_ZSTB1
- 11 N_ZSTB#1
- 11 N_ZUREQ
- 11 N_ZDREQ
- 11 N_ZAD0
- 11 N_ZAD1
- 11 N_ZAD2
- 11 N_ZAD3
- 11 N_ZAD4
- 11 N_ZAD5
- 11 N_ZAD6
- 11 N_ZAD7
- 11 N_ZAD8
- 11 N_ZAD9
- 11 N_ZAD10
- 11 N_ZAD11
- 11 N_ZAD12
- 11 N_ZAD13
- 11 N_ZAD14
- 11 N_ZAD15
- 11 N_ZAD16
- 11 N_ZAD17
- 11 N_ZAD18
- 11 N_ZAD19

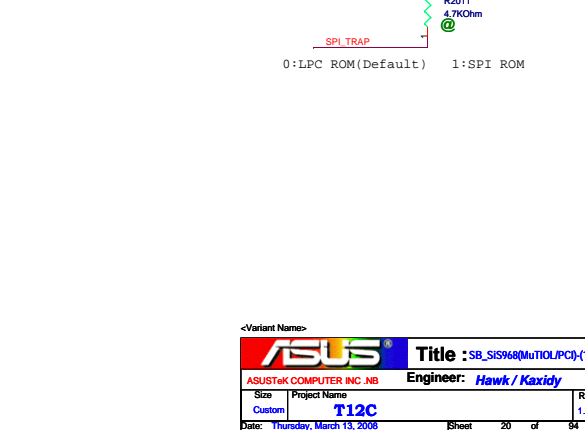
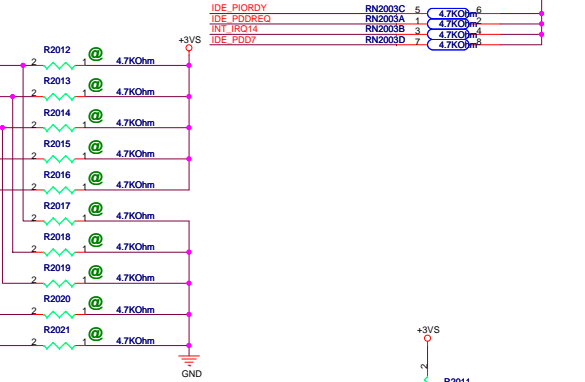
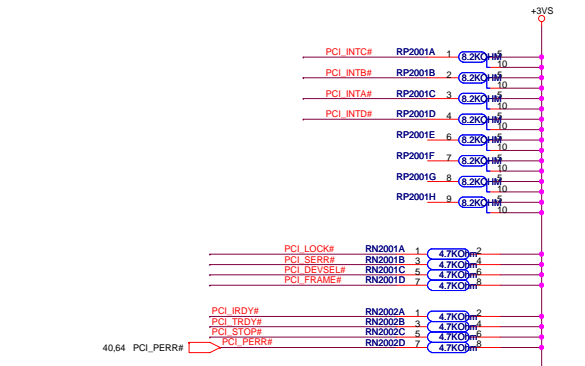
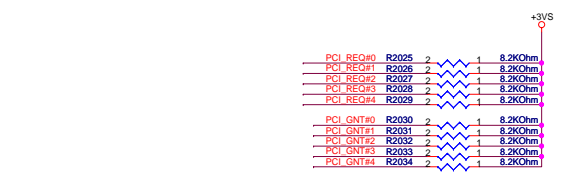
- 40.64 PCI_REQ#4
- 40.64 PCI_REQ#3
- 40.64 PCI_REQ#2
- 40.64 PCI_REQ#1
- 40.64 PCI_REQ#0
- 40.64 PCI_GNT#4
- 40.64 PCI_GNT#3
- 40.64 PCI_GNT#2
- 40.64 PCI_GNT#1
- 40.64 PCI_GNT#0
- 40.64 PCI_CBE#3
- 40.64 PCI_CBE#2
- 40.64 PCI_CBE#1
- 40.64 PCI_CBE#0
- 40.64 PCI_INTA#
- 40.64 PCI_INTB#
- 40.64 PCI_INTC#
- 40.64 PCI_INTD#
- 40.64 PCI_FRAME#
- 40.64 PCI_IRDY#
- 40.64 PCI_TRDY#
- 40.64 PCI_STOP#
- 40.64 PCI_SERR#
- 40.64 PCI_PAR
- 40.64 PCI_DEVSEL#
- 40.64 PCI_LOCK#
- 29 CLK_SBPCL
- 29 CLK_ZCLK_SB
- 11 N_ZSTB0
- 11 N_ZSTB#0
- 11 N_ZSTB1
- 11 N_ZSTB#1
- 11 N_ZUREQ
- 11 N_ZDREQ
- 11 N_ZAD0
- 11 N_ZAD1
- 11 N_ZAD2
- 11 N_ZAD3
- 11 N_ZAD4
- 11 N_ZAD5
- 11 N_ZAD6
- 11 N_ZAD7
- 11 N_ZAD8
- 11 N_ZAD9
- 11 N_ZAD10
- 11 N_ZAD11
- 11 N_ZAD12
- 11 N_ZAD13
- 11 N_ZAD14
- 11 N_ZAD15
- 11 N_ZAD16
- 11 N_ZAD17
- 11 N_ZAD18
- 11 N_ZAD19

- 40.64 PCI_REQ#4
- 40.64 PCI_REQ#3
- 40.64 PCI_REQ#2
- 40.64 PCI_REQ#1
- 40.64 PCI_REQ#0
- 40.64 PCI_GNT#4
- 40.64 PCI_GNT#3
- 40.64 PCI_GNT#2
- 40.64 PCI_GNT#1
- 40.64 PCI_GNT#0
- 40.64 PCI_CBE#3
- 40.64 PCI_CBE#2
- 40.64 PCI_CBE#1
- 40.64 PCI_CBE#0
- 40.64 PCI_INTA#
- 40.64 PCI_INTB#
- 40.64 PCI_INTC#
- 40.64 PCI_INTD#
- 40.64 PCI_FRAME#
- 40.64 PCI_IRDY#
- 40.64 PCI_TRDY#
- 40.64 PCI_STOP#
- 40.64 PCI_SERR#
- 40.64 PCI_PAR
- 40.64 PCI_DEVSEL#
- 40.64 PCI_LOCK#
- 29 CLK_SBPCL
- 29 CLK_ZCLK_SB
- 11 N_ZSTB0
- 11 N_ZSTB#0
- 11 N_ZSTB1
- 11 N_ZSTB#1
- 11 N_ZUREQ
- 11 N_ZDREQ
- 11 N_ZAD0
- 11 N_ZAD1
- 11 N_ZAD2
- 11 N_ZAD3
- 11 N_ZAD4
- 11 N_ZAD5
- 11 N_ZAD6
- 11 N_ZAD7
- 11 N_ZAD8
- 11 N_ZAD9
- 11 N_ZAD10
- 11 N_ZAD11
- 11 N_ZAD12
- 11 N_ZAD13
- 11 N_ZAD14
- 11 N_ZAD15
- 11 N_ZAD16
- 11 N_ZAD17
- 11 N_ZAD18
- 11 N_ZAD19

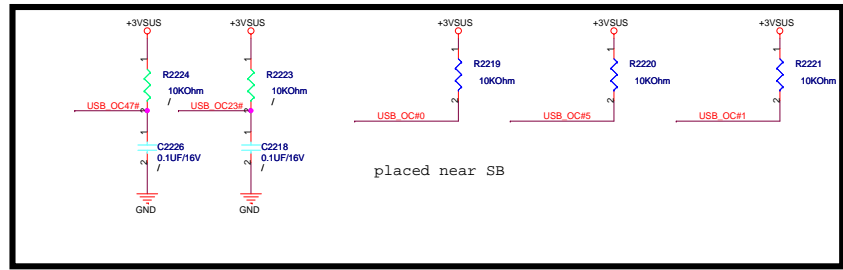
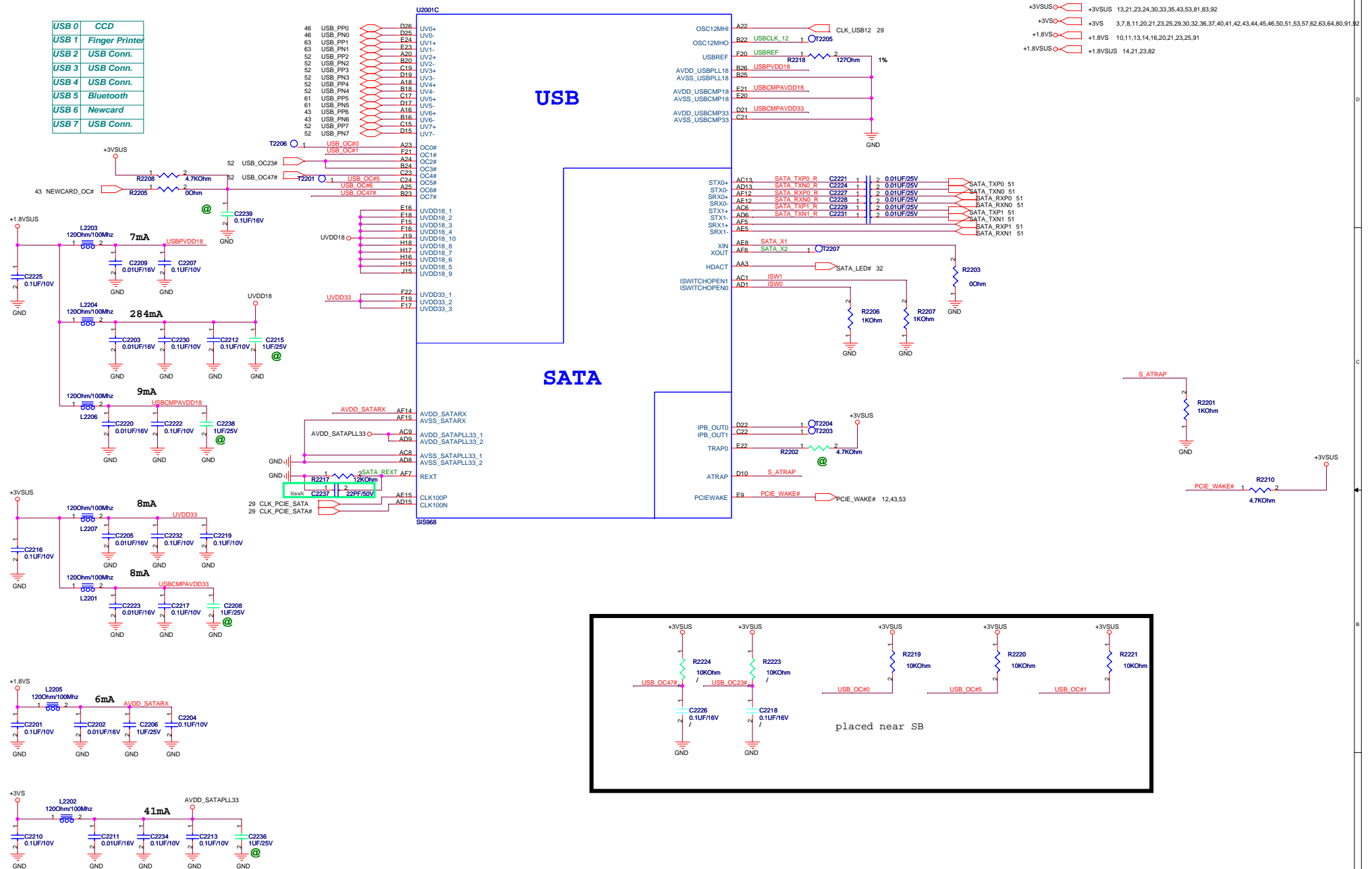
- 40.64 PCI_REQ#4
- 40.64 PCI_REQ#3
- 40.64 PCI_REQ#2
- 40.64 PCI_REQ#1
- 40.64 PCI_REQ#0
- 40.64 PCI_GNT#4
- 40.64 PCI_GNT#3
- 40.64 PCI_GNT#2
- 40.64 PCI_GNT#1
- 40.64 PCI_GNT#0
- 40.64 PCI_CBE#3
- 40.64 PCI_CBE#2
- 40.64 PCI_CBE#1
- 40.64 PCI_CBE#0
- 40.64 PCI_INTA#
- 40.64 PCI_INTB#
- 40.64 PCI_INTC#
- 40.64 PCI_INTD#
- 40.64 PCI_FRAME#
- 40.64 PCI_IRDY#
- 40.64 PCI_TRDY#
- 40.64 PCI_STOP#
- 40.64 PCI_SERR#
- 40.64 PCI_PAR
- 40.64 PCI_DEVSEL#
- 40.64 PCI_LOCK#
- 29 CLK_SBPCL
- 29 CLK_ZCLK_SB
- 11 N_ZSTB0
- 11 N_ZSTB#0
- 11 N_ZSTB1
- 11 N_ZSTB#1
- 11 N_ZUREQ
- 11 N_ZDREQ
- 11 N_ZAD0
- 11 N_ZAD1
- 11 N_ZAD2
- 11 N_ZAD3
- 11 N_ZAD4
- 11 N_ZAD5
- 11 N_ZAD6
- 11 N_ZAD7
- 11 N_ZAD8
- 11 N_ZAD9
- 11 N_ZAD10
- 11 N_ZAD11
- 11 N_ZAD12
- 11 N_ZAD13
- 11 N_ZAD14
- 11 N_ZAD15
- 11 N_ZAD16
- 11 N_ZAD17
- 11 N_ZAD18
- 11 N_ZAD19

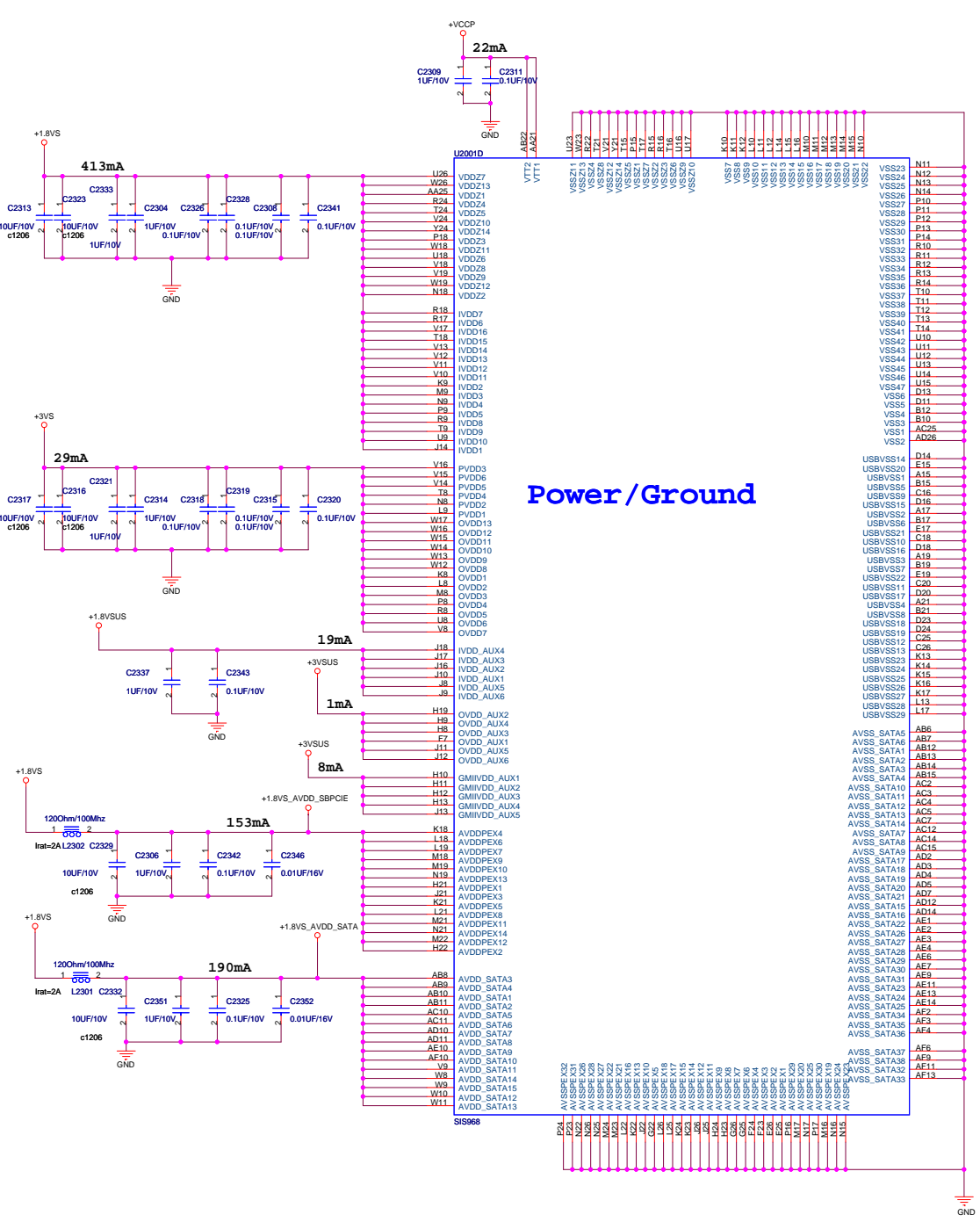


- +1.8VS
- +3VS
- +3VO



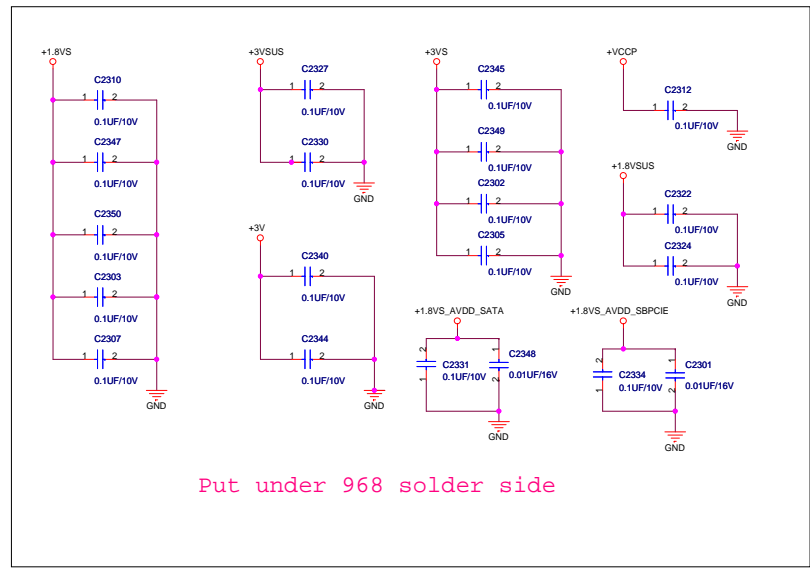
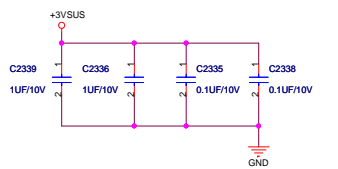
USB 0	CCD
USB 1	Finger Printer
USB 2	USB Conn.
USB 3	USB Conn.
USB 4	USB Conn.
USB 5	Bluetooth
USB 6	Newcard
USB 7	USB Conn.



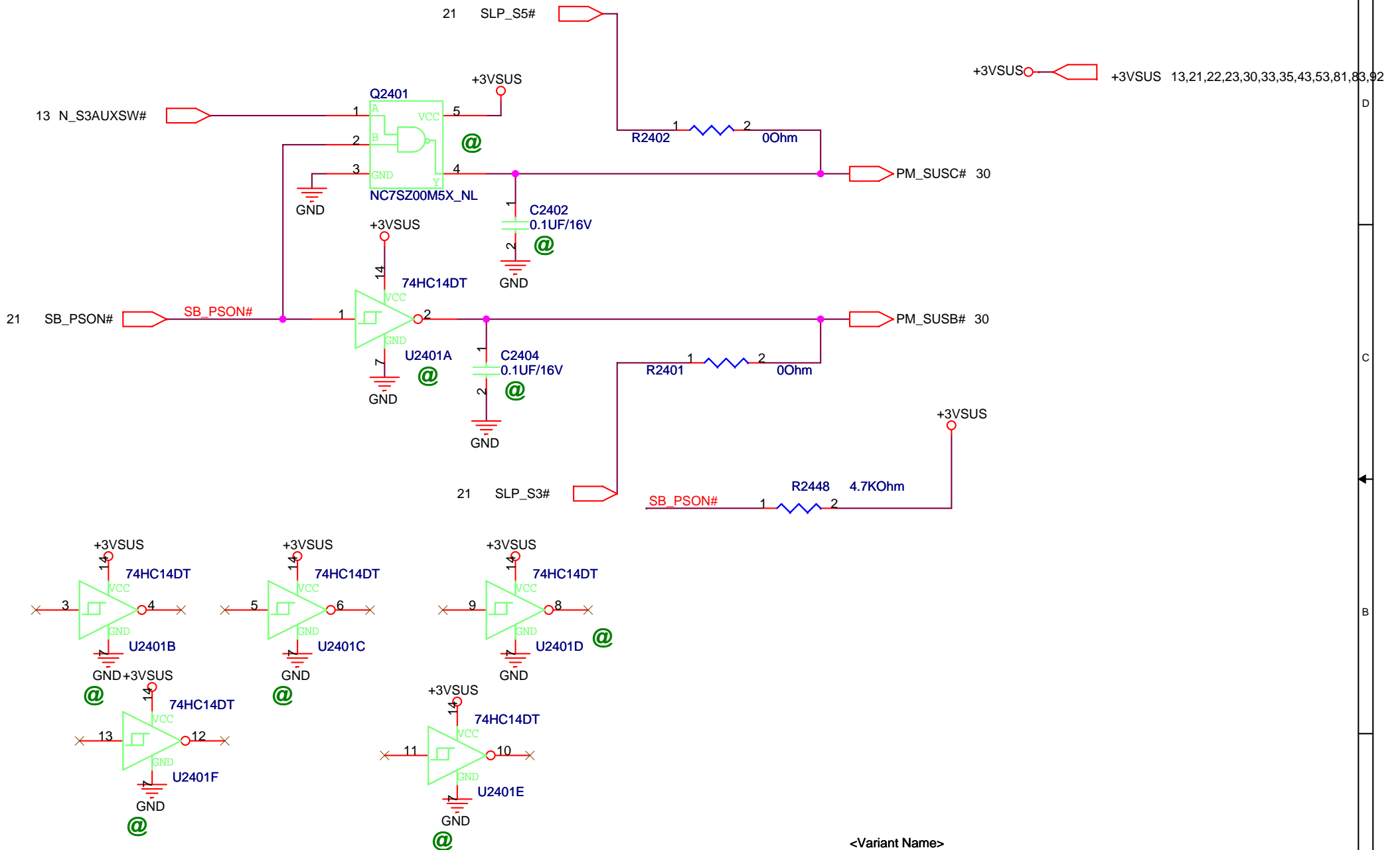


Power / Ground

- +3VSUS ○ +3VSUS 13,21,22,24,30,33,35,43,53,81,83,92
- +1.8VSUS ○ +1.8VSUS 14,21,22,82
- +1.8VS ○ +1.8VS 10,11,13,14,16,20,21,22,25,91
- +3VS ○ +3VS 3,7,8,11,20,21,22,25,29,30,32,36,37,40,41,42,43,44,45,46,50,51,53,57,62,63,64,80,91,92
- +3V ○ +3V 20,35,40,46,53,57,61,62,64,65,91
- +VCCP ○ +VCCP 4,10,14,21,29,57,83,92

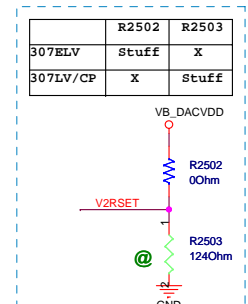
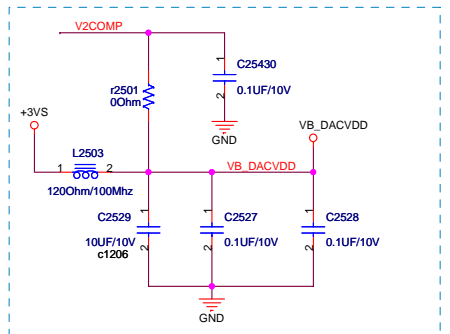
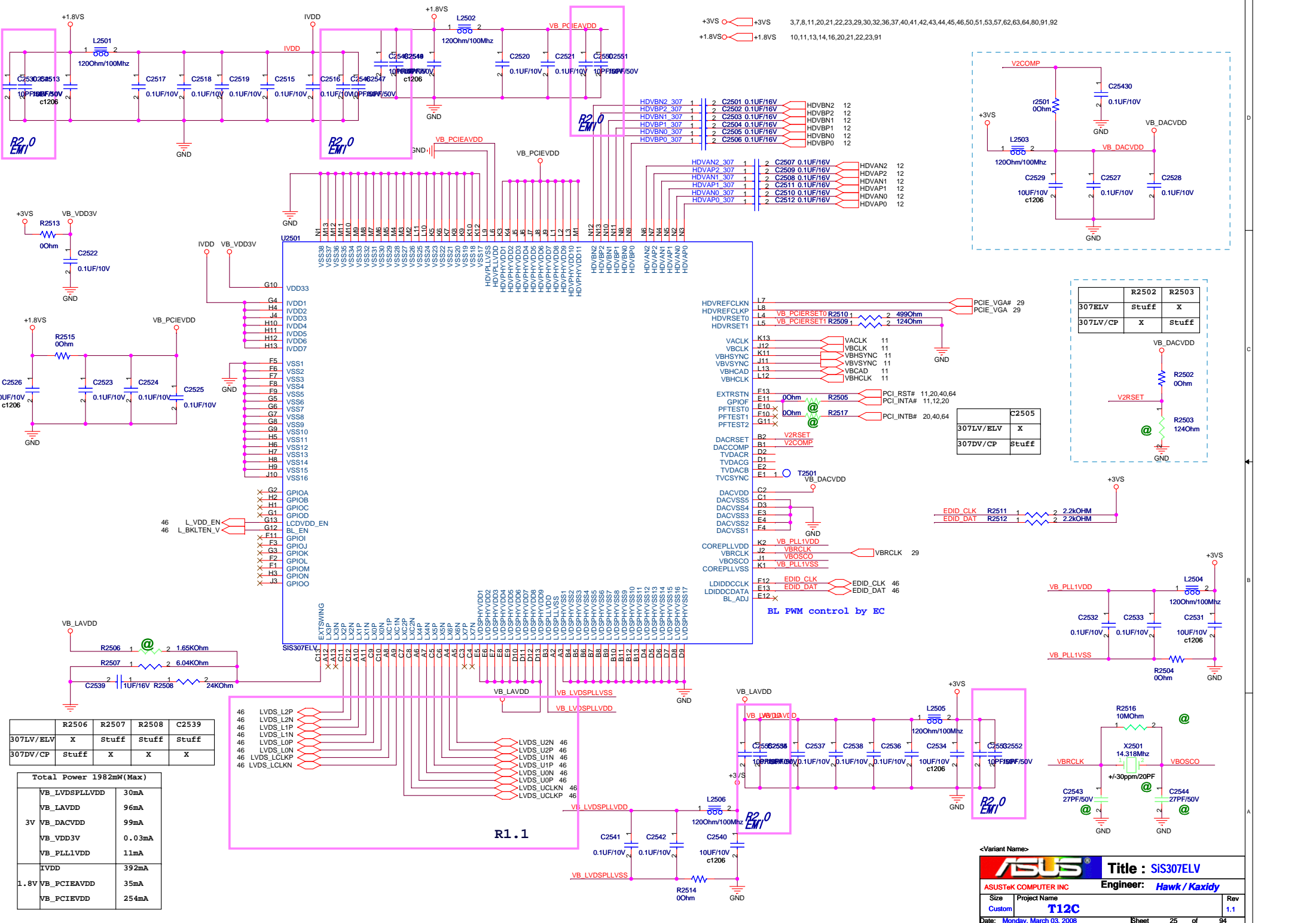


Put under 968 solder side



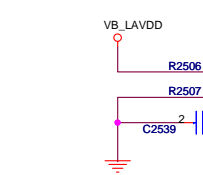
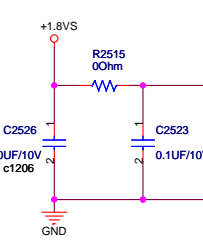
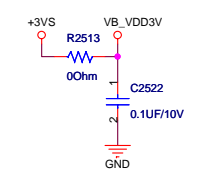
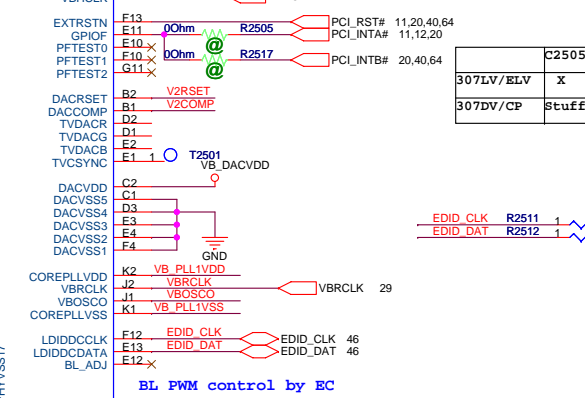
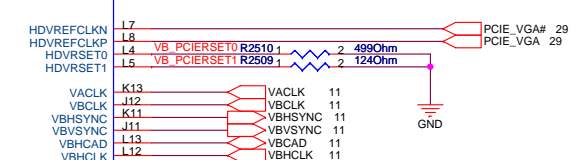
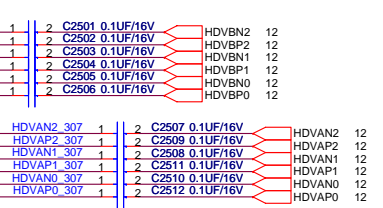
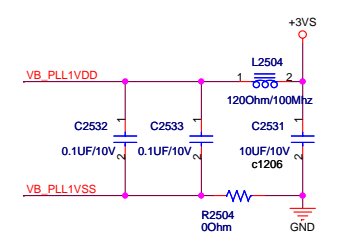
<Variant Name>

		Title : Si968 (STRAPING)
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy
Size A	Project Name T12C	Rev 1.1
Date: Friday, August 17, 2007		Sheet 24 of 94



307LV/BLV	Stuff	X
307LV/CP	X	Stuff

307LV/BLV	X
307DV/CP	Stuff




R2506	R2507	R2508	C2539
307LV/BLV	X	Stuff	Stuff
307DV/CP	Stuff	X	X

Total Power 1982mW(Max)	
VB_LVDSPLLVD	30mA
VB_LAVDD	96mA
VB_DACVDD	99mA
VB_VDD3V	0.03mA
VB_PLL1VDD	11mA
IVDD	392mA
1.8V VB_PCIEAVDD	35mA
VB_PCIEVDD	254mA

	5	4	3	2	1
D					
C					
B					
A					

<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC .NB		Engineer: <i>Hawk / Kaxidy</i>
Size	Project Name	Rev
A	T12C	1.1
Date: <u>Monday, August 13, 2007</u>		Sheet 26 of 94

	5	4	3	2	1
D					
C					
B					
A					

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>



Title : NULL

ASUSTeK COMPUTER INC

Engineer: Hawk / Kaxidy

Size	Project Name	Rev
A	T12C	1.1

Date: Monday, August 13, 2007

Sheet 27 of 94

5

4

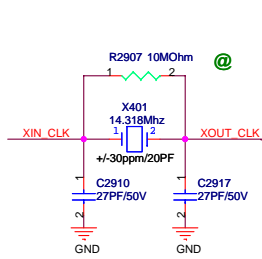
3

2

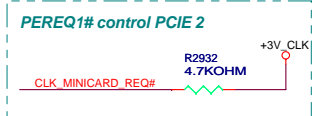
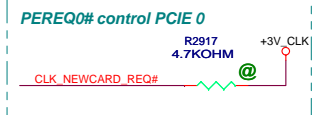
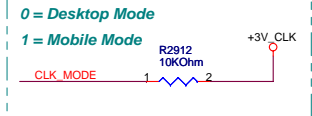
1



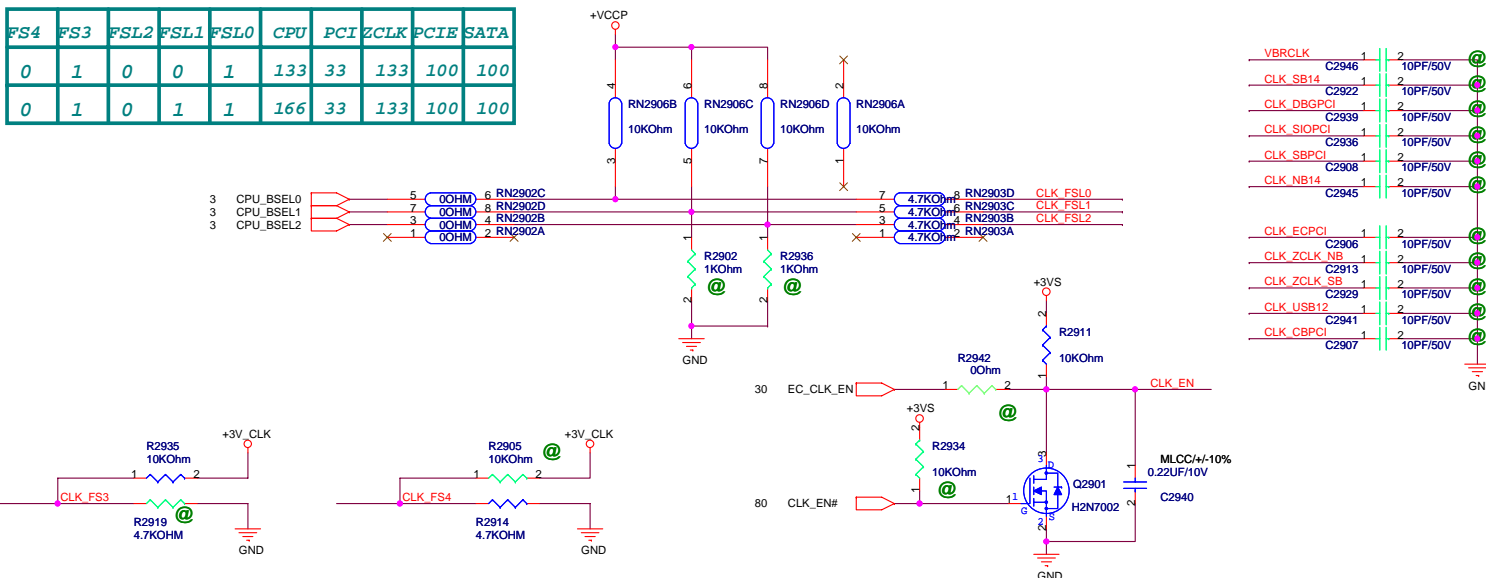
<Variant Name>		ASUS ®		Title : NULL	
ASUSTek COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>			
Size	Project Name			Rev	
Custom	T12C			1.1	
Date: Monday, August 13, 2007		Sheet	28	of	94



CLK_MODE



FS4	FS3	FSL2	FSL1	FSL0	CPU	PCI	ZCLK	PCIE	SATA
0	1	0	0	1	133	33	133	100	100
0	1	0	1	1	166	33	133	100	100



+3VSO $= +3V$ 3,7,8,11,20,21,22,23,25,30,32,36,37,40,41,42,43,44,45,46,50,51,53,57,62,63,64,80,91,92
+VCCPO $= +VCCP$ 4,10,14,21,23,57,83,92

<Variant Name>

Title : CLOCK GEN

ASUSTeK COMPUTER INC Engineer: Hawk / Kaxidy

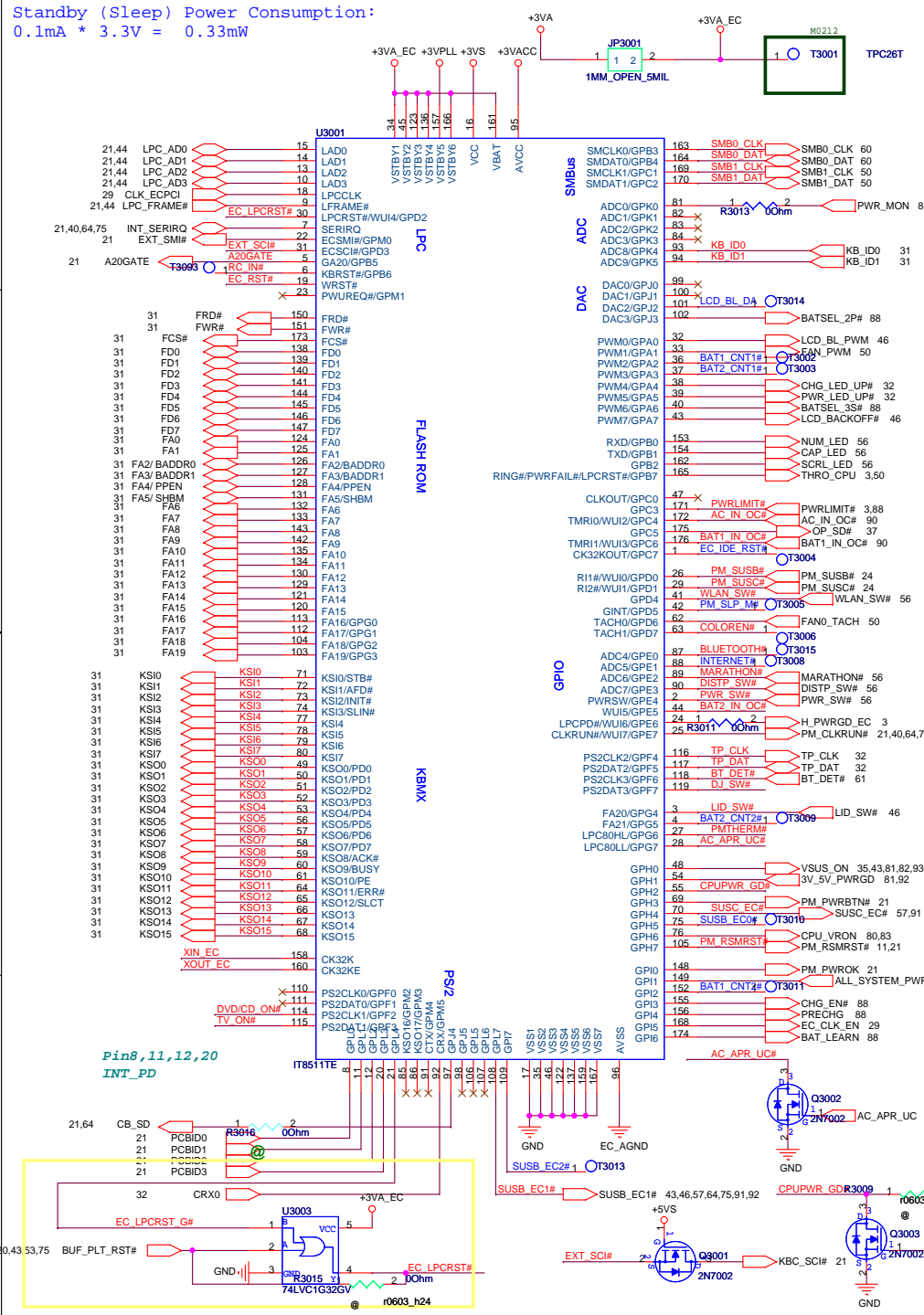
Size Project Name
Custom T12C

Date: Friday, March 07, 2008 Sheet 29 of 94

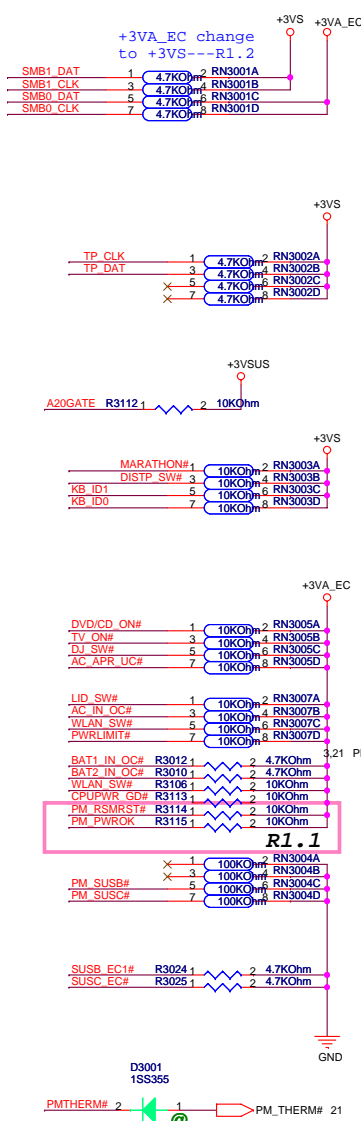
Rev 1.1

For IT8511 Core IC

Standby (Sleep) Power Consumption:
0.1mA * 3.3V = 0.33mW

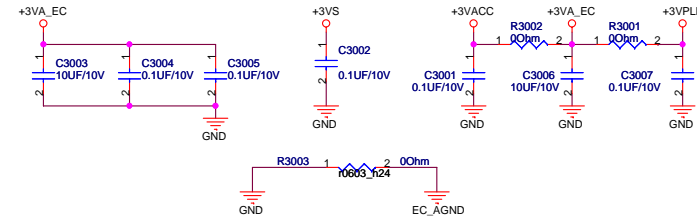


For Pull-up/Pull-down

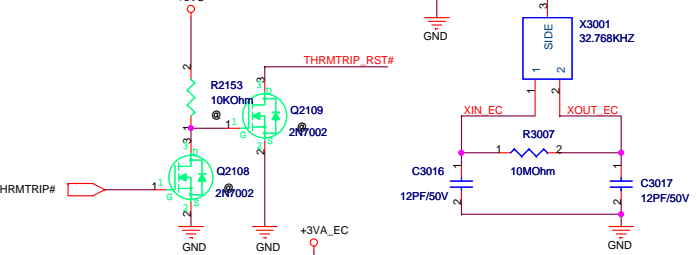


+3VA → +3VA 21,46,50,56,57,81,93
+3VS → +3VS 3,7,8,11,20,21,22,23,25,29,32,36,37,40,41,42,43,44,45,46,50,51,53,57,62,63,64,80,91,92
+5VS → +5VS 21,32,36,37,38,45,50,51,56,57,80,91
+3VA_EC → +3VA_EC 31,46

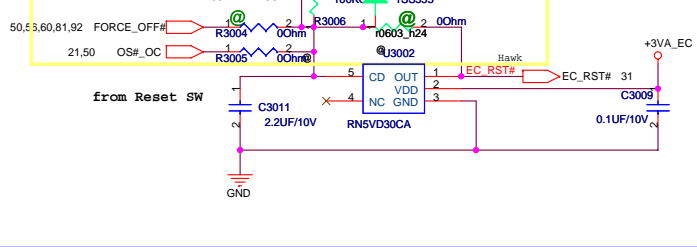
For IT8511 Power



For Xtal



For EC reset



For EC Hardware Strap

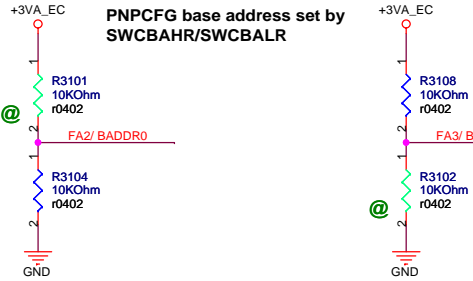
I/O Base Address	Share Memory	PP Enable
Note: It can be programmable by EC firmware	Note: It can be programmable by EC firmware	Note: Default Internal Pull-Low
-<Variant Name>		
Title : EC-ITE8511 (2)		
ASUSTek COMPUTER INC Engineer: Hawk / Kaxidy		
Size	Project Name	Rev
Custom	T12C	1.1
Date: Friday, March 07, 2008	Sheet	30 of 94

EC Hardware Strap

Strap value sampled after VSTBY power up reset

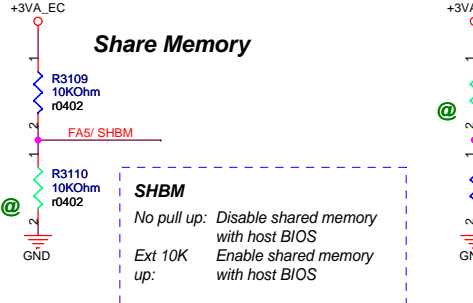
+3VA_ECO +3VA_EC 30,46

PNPCFG base address set by SWCBAHR/SWCBALR



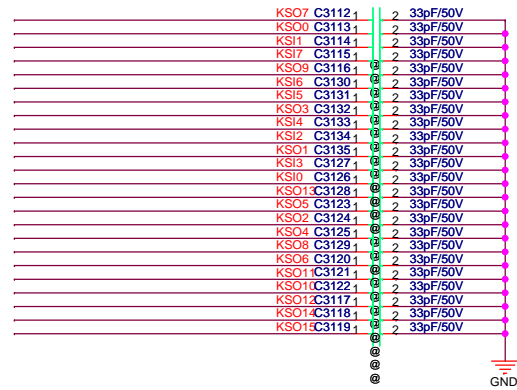
BADDR[1:0]
 No pull up: The register pair to access PNPCFG is 002Eh and 002Fh.
 Ext 10K up on BADDR0: The register pair to access PNPCFG is 004Eh and 004Fh.
 Ext 10K up on BADDR1: The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

Share Memory



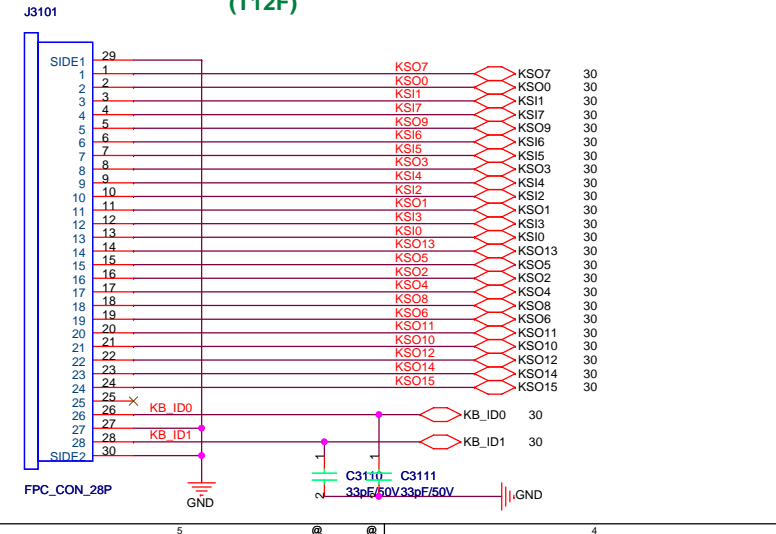
SHBM
 No pull up: Disable shared memory with host BIOS
 Ext 10K up: Enable shared memory with host BIOS

PPEN
 No pull up: Normal
 Ext 10K up: KBS interface pins are switched to parallel port interface for in-system programming.



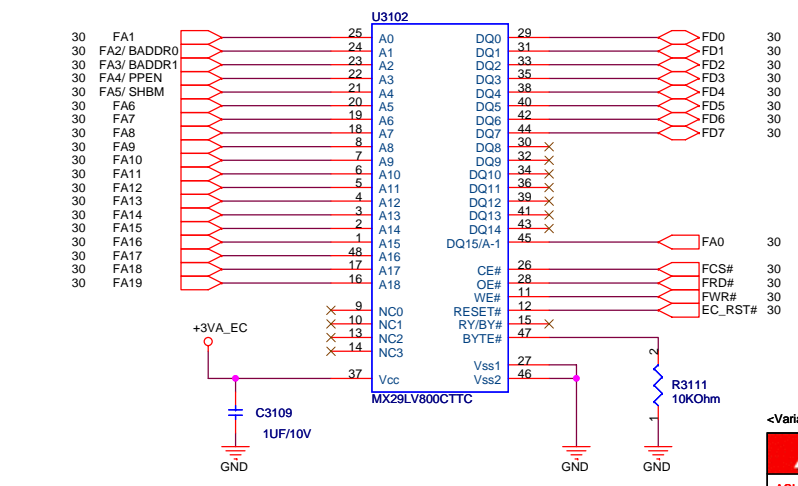
Keyboard Conn.

P/N: 12G182402806 (T12F)



For 8M bits SPI ROM

8M TSOP



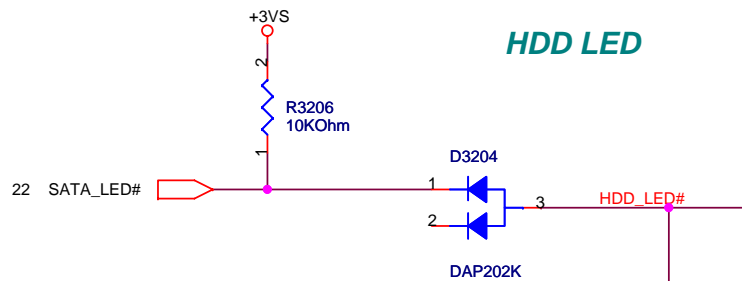
<Variant Name>

Title : EC-ITE8511(2)
 ASUSTeK COMPUTER INC.ETD Engineer: Hawk / Kaxidy

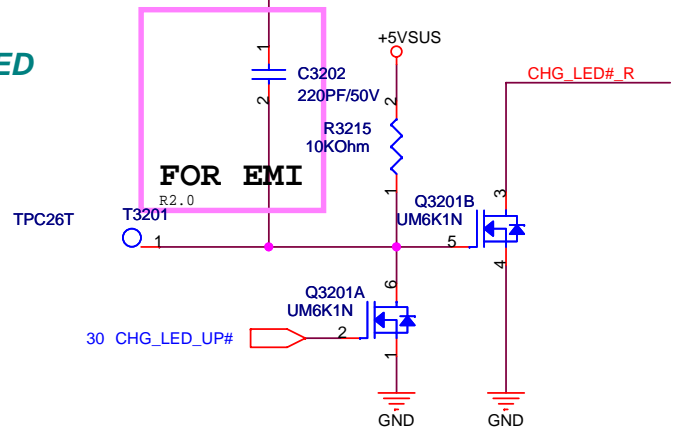
Size	Project Name	Rev
Custom	T12C	1.1
Date: Friday, August 17, 2007	Sheet 31 of 94	

Touchpad

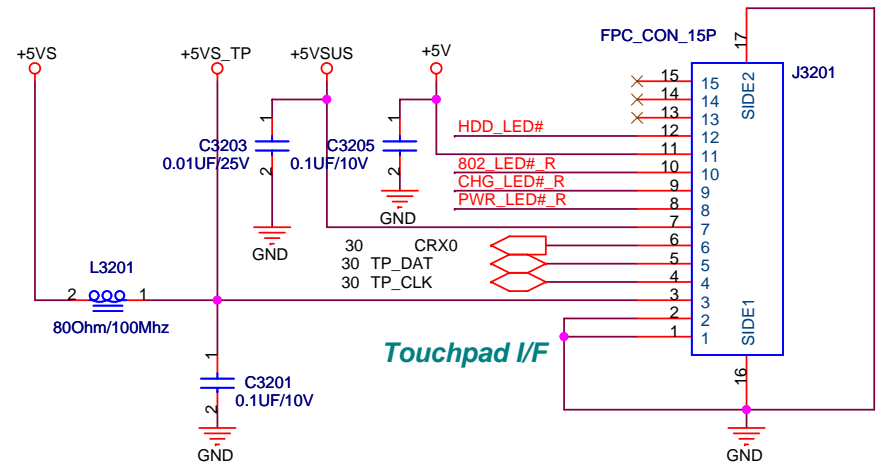
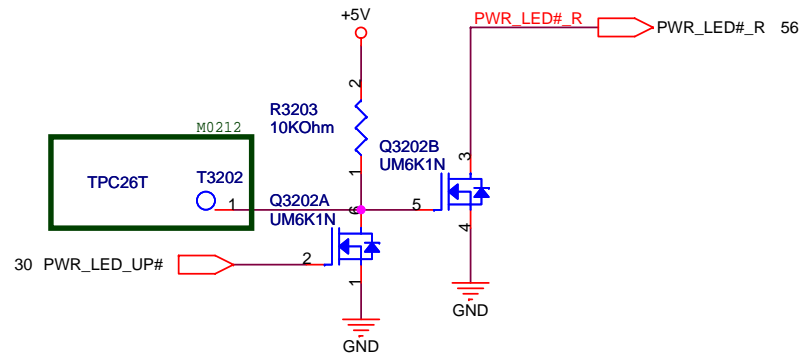
- +5VSUS ○ +5VSUS 33,81
- +5VS ○ +5V 21,30,36,37,38,45,50,51,56,57,80,91
- +3VS ○ +3VS 3,7,8,11,20,21,22,23,25,29,30,36,37,40,41,42,43,44,45,46,50,51,53,57,62,63,64,80,91,92
- +5V ○ +5V 37,46,52,56,57,65,91



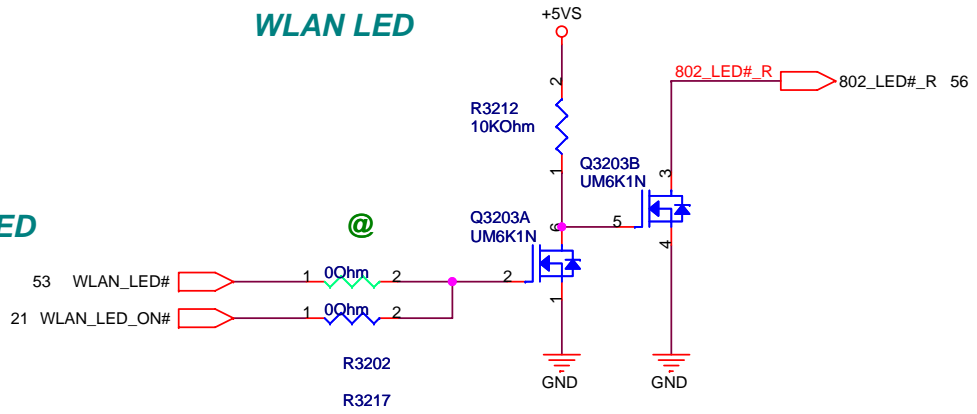
CHARGE LED



POWER LED



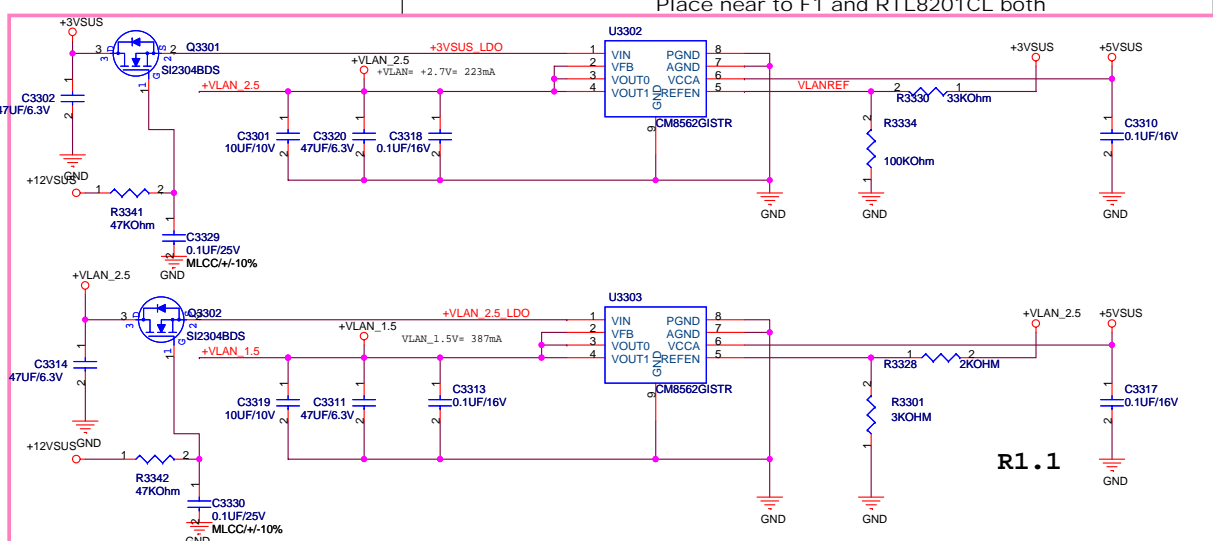
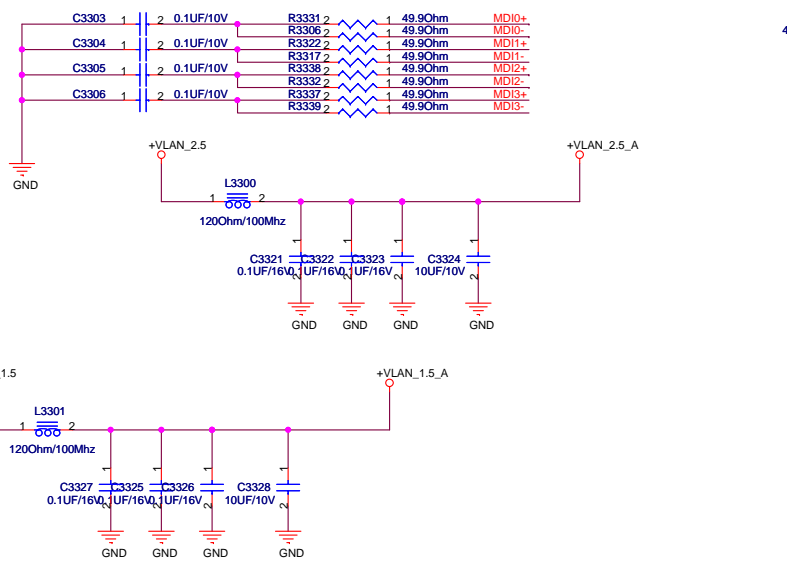
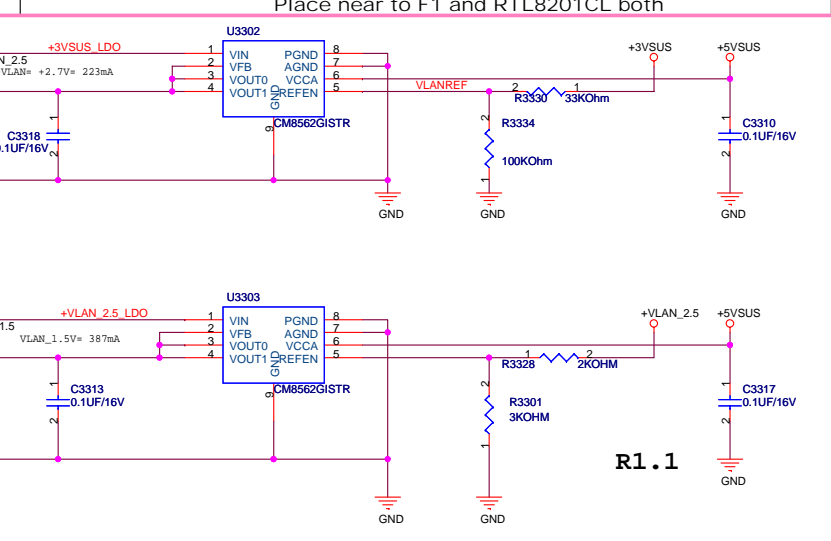
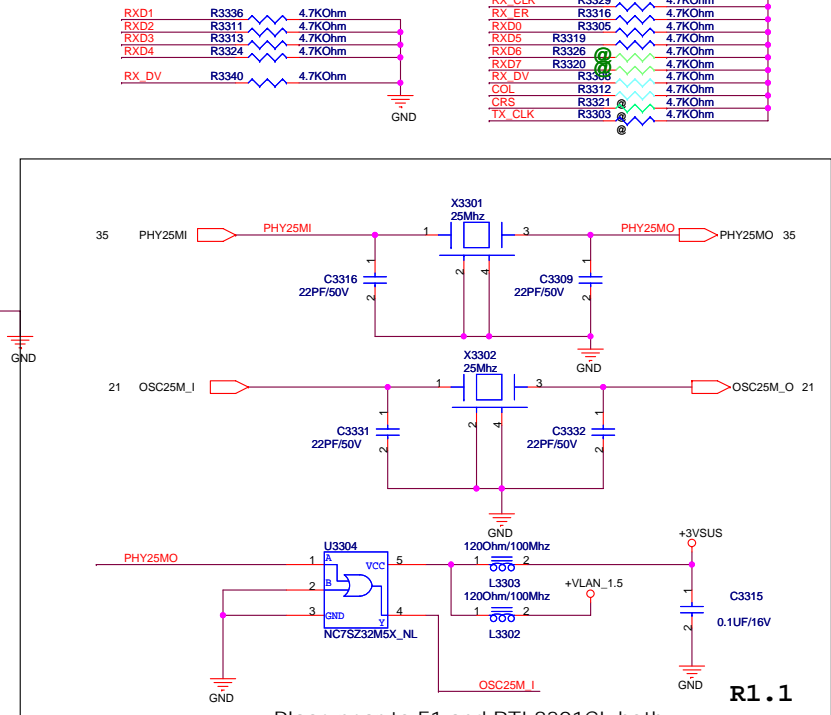
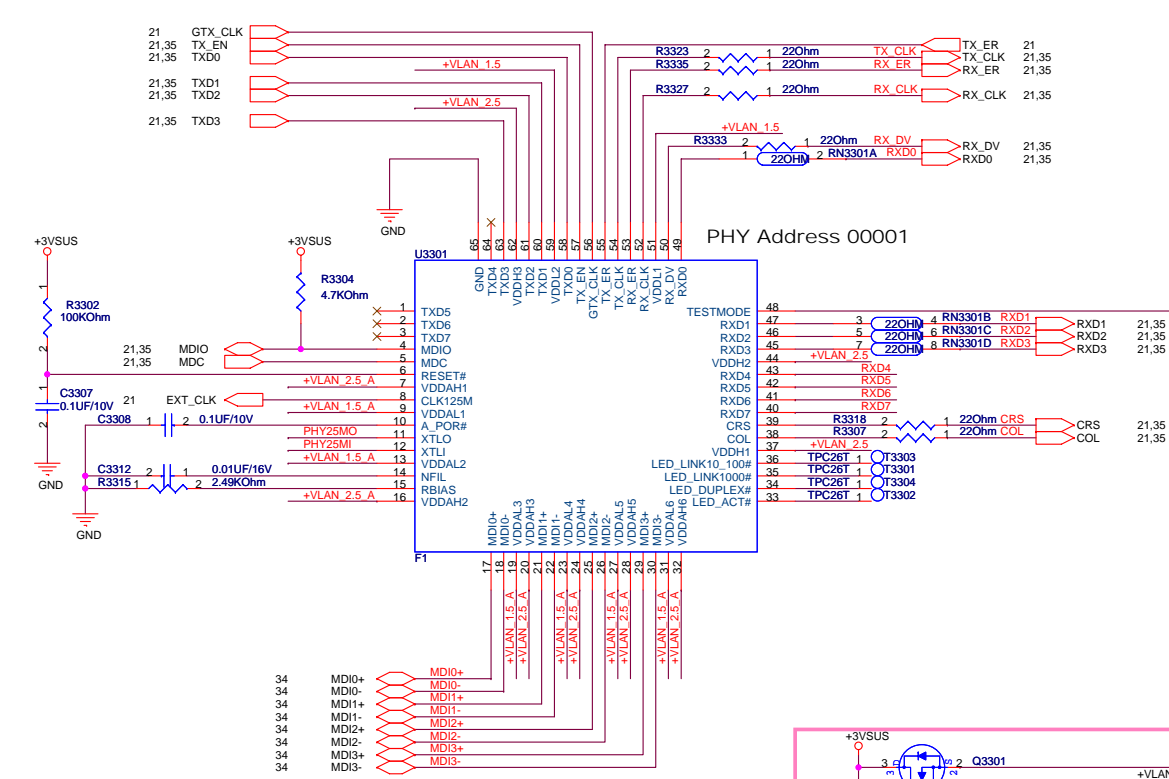
WLAN LED

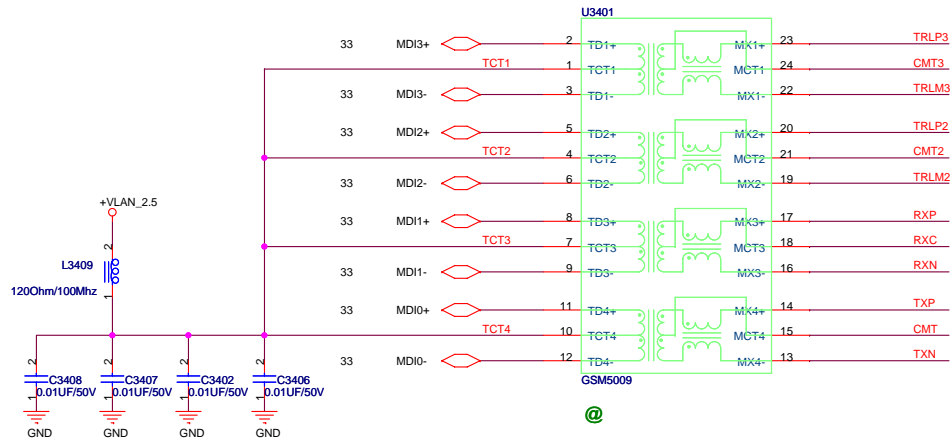


T12
12G183101506

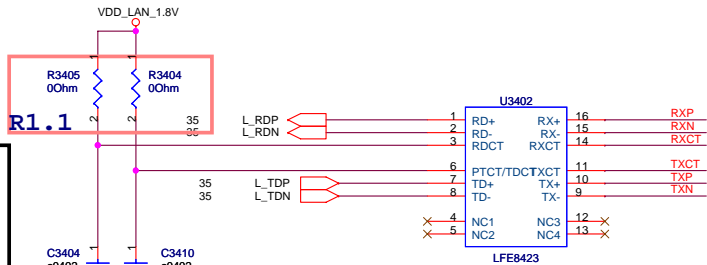
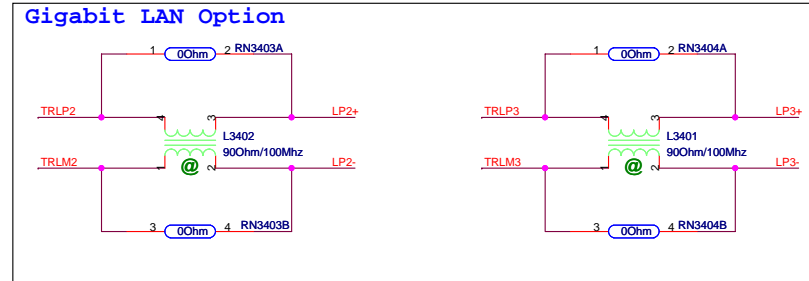
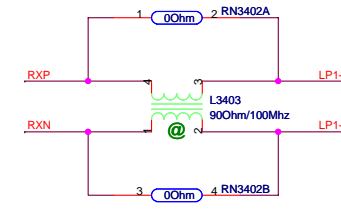
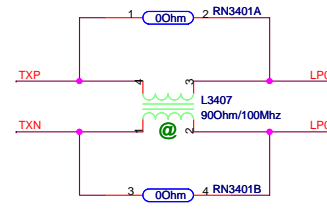
<Variant Name>	
ASUS	
Title : TouchPad	
ASUSTeK COMPUTER INC	
Engineer: Hawk / Kaxidy	
Size	Project Name
Custom	T12C
Date: Tuesday, March 04, 2008	Rev 1.1
Sheet 32	of 94

VDD_LAN_1.8V ○ VDD_LAN_1.8V 34,35
 +VLAN_2.5 ○ +VLAN_2.5 21,34
 +3VSUS ○ +3VSUS 13,21,22,23,24,30,35,43,53,81,83,92
 +5VSUS ○ +5VSUS 32,81
 +5VO ○ +5V 32,37,46,52,56,57,65,91

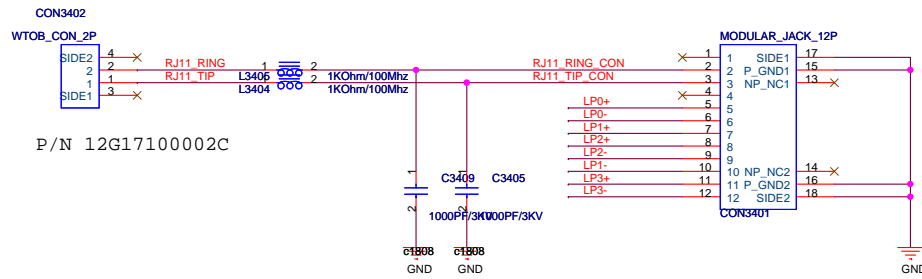
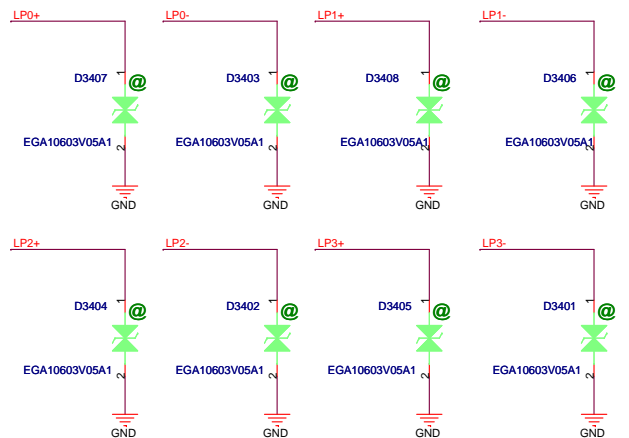
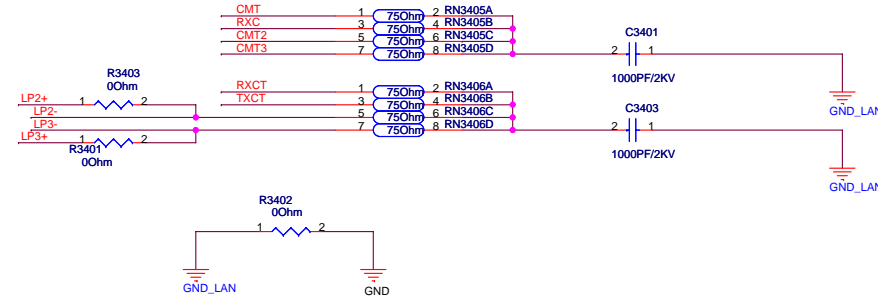
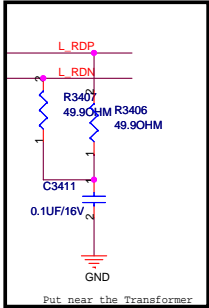


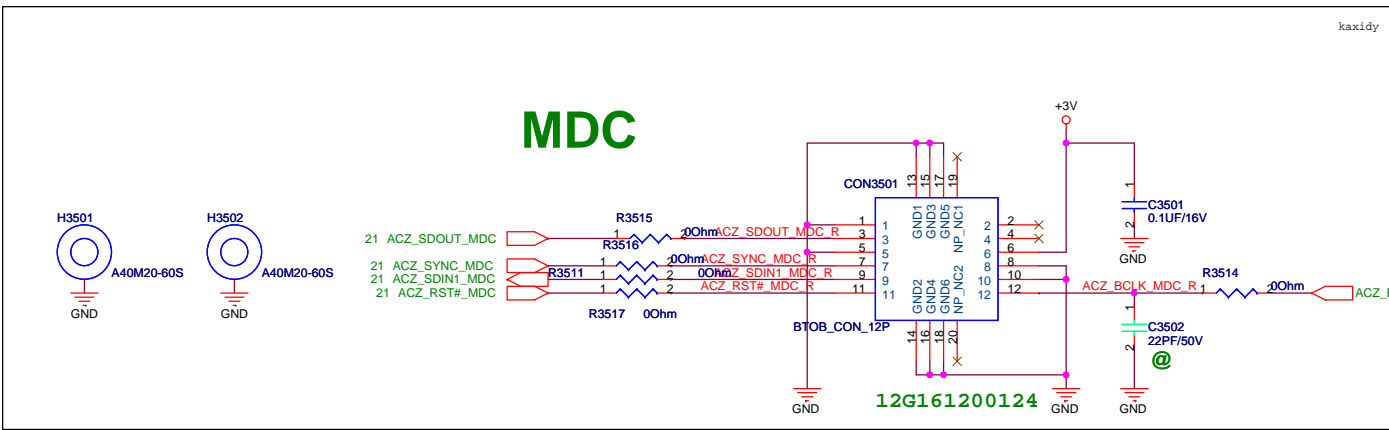
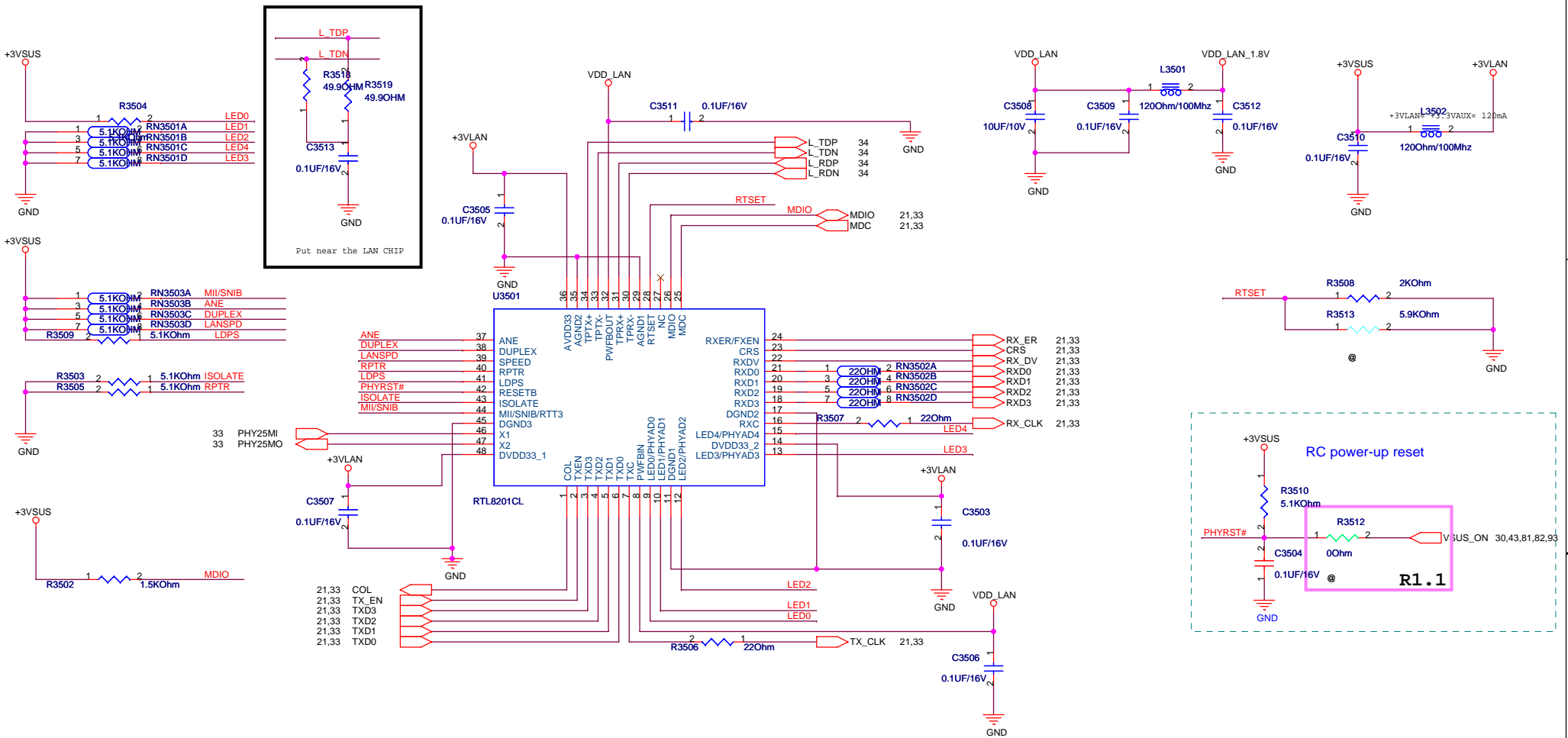


VDD_LAN_1.8V \rightarrow VDD_LAN_1.8V 35
 +VLAN_2.5 \rightarrow +VLAN_2.5 21,33



U3402 place under U3401
 Co-lay 10/100 BOM Option





<Variant Name>

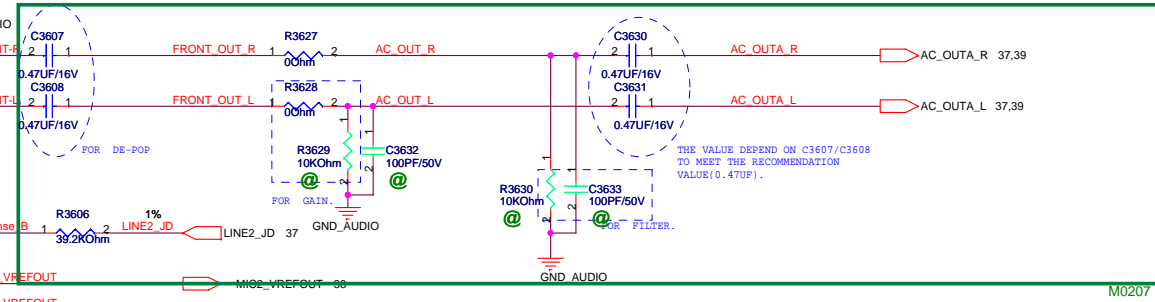
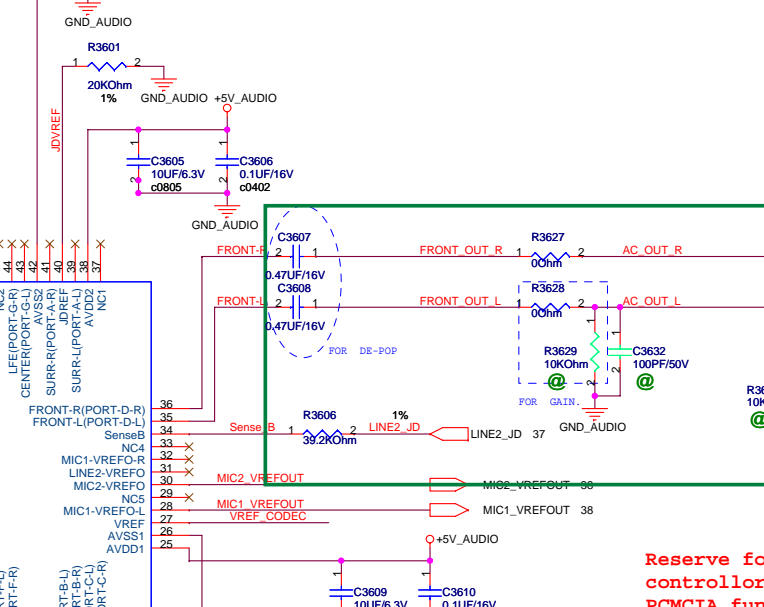
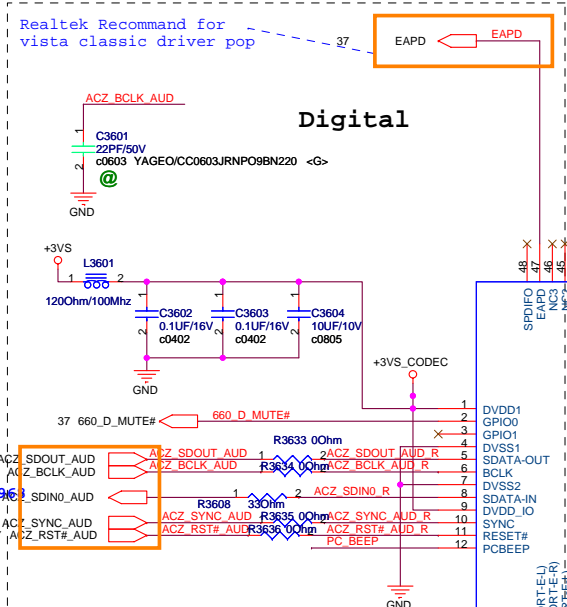
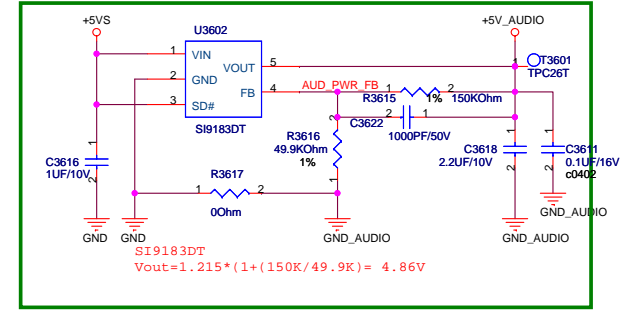
ASUS		Title : RTL8201BL 10/100 & MDC	
ASUSTeK COMPUTER INC. NB		Engineer: Hawk / Kaxidy	
Size	Project Name	Rev	
Custom	T12C	1.1	
Date: Friday, August 17, 2007	Sheet	35	of 94

CODEC ALC660 REV:D

+5VS \rightarrow +5VS 21,30,32,37,38,45,50,51,56,57,80,91
 +5V_AUDIO \rightarrow +5V_AUDIO 38

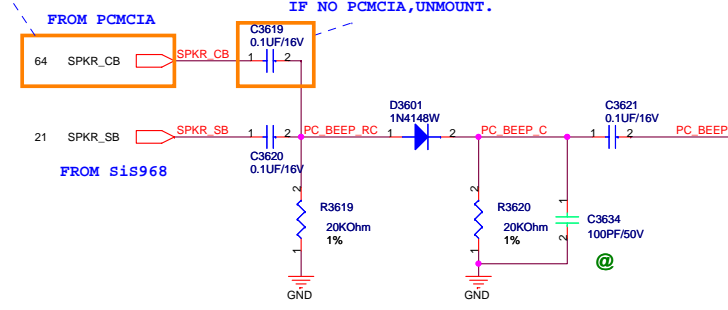
AUDIO POWER

M0207

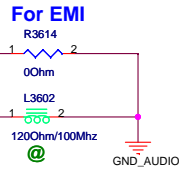


PC BEEP

Reserve for Cardbus controller that has PCMCIA function.

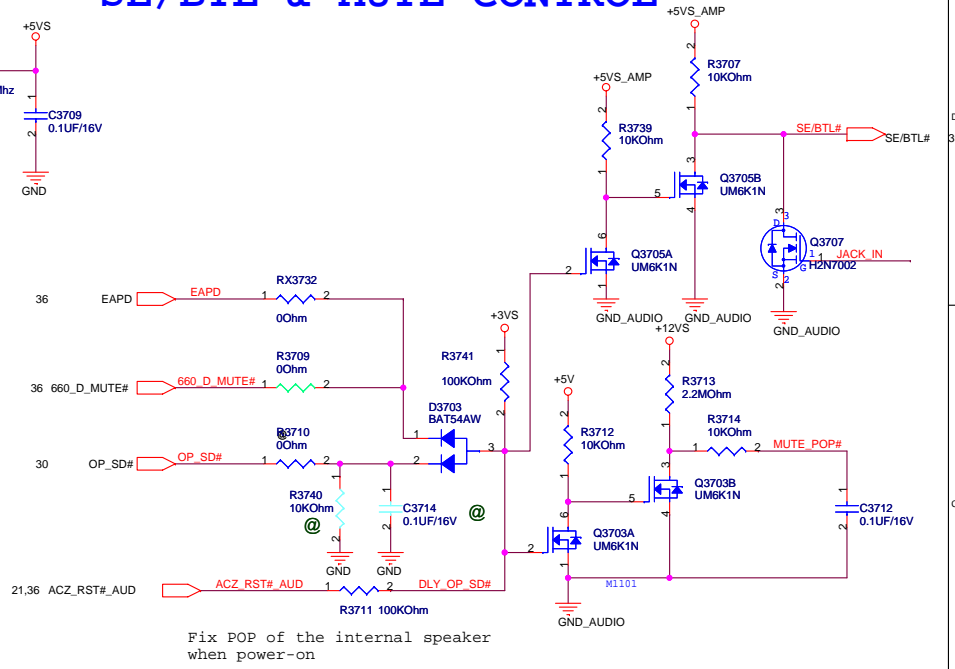
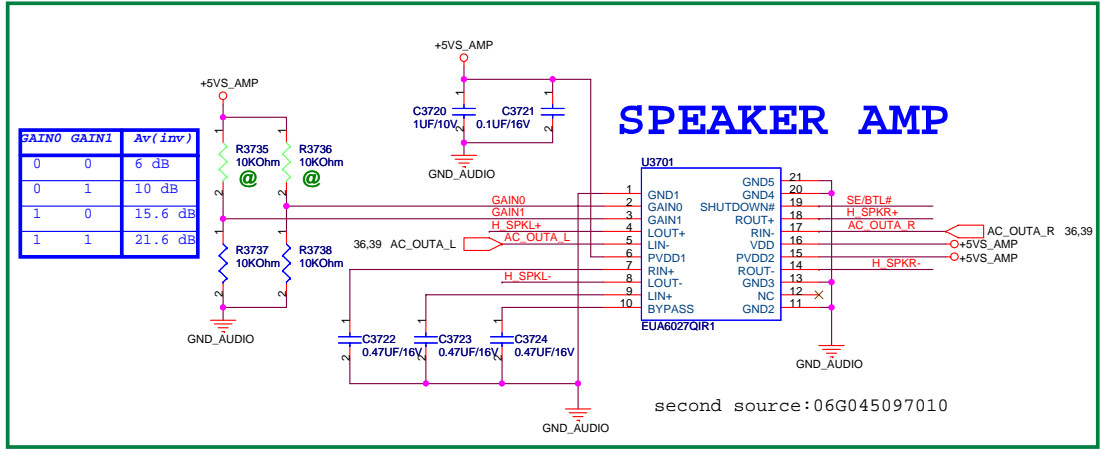
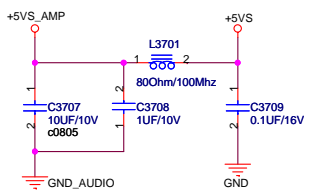


Input impedance: 64K ohm(Typical)

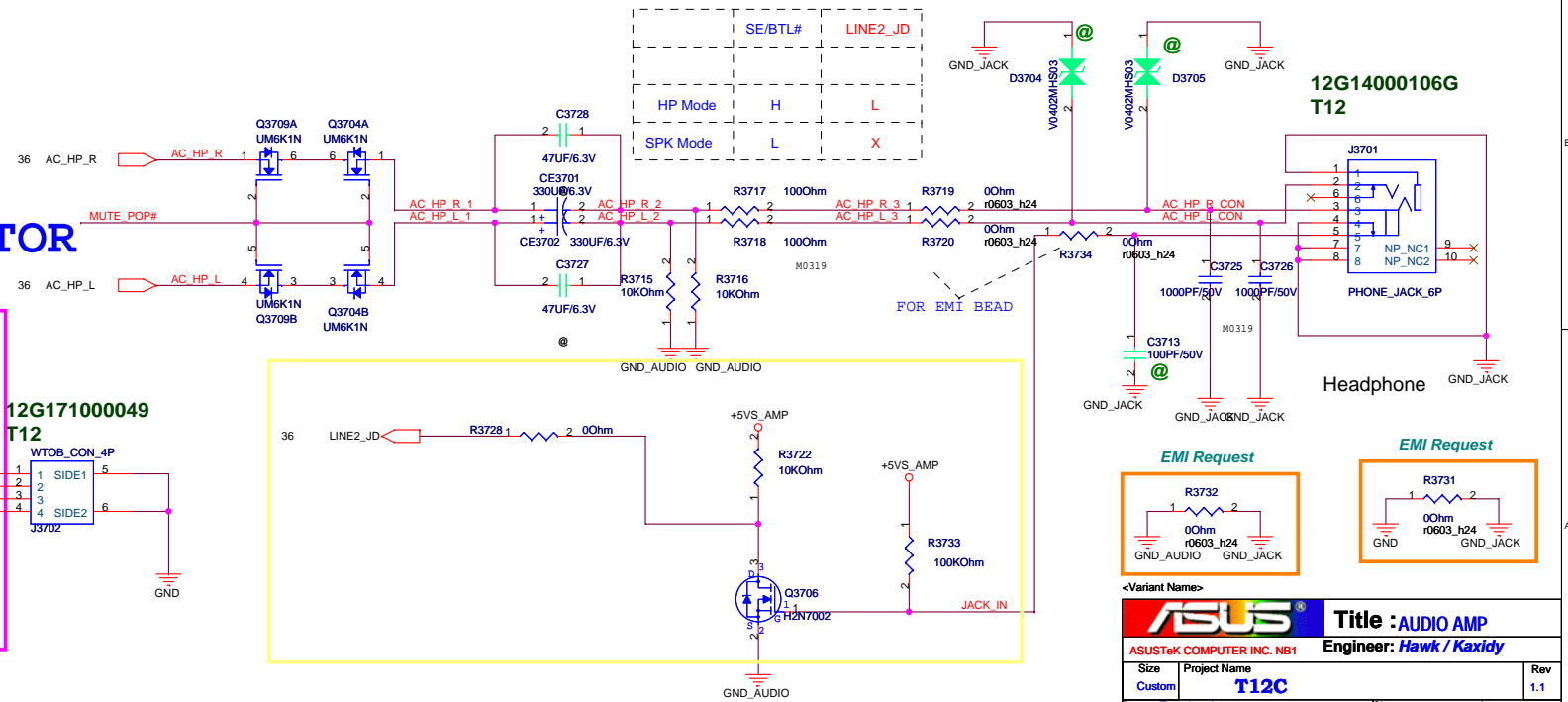


AMP POWER SE/BTL & MUTE CONTROL

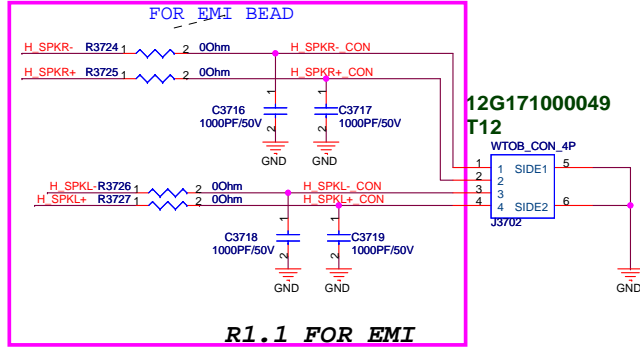
+5VS_AMP $= +5VS_AMP 39$
 +5VS $= +5VS 21,30,32,36,38,45,50,51,56,57,80,91$



HP CONN

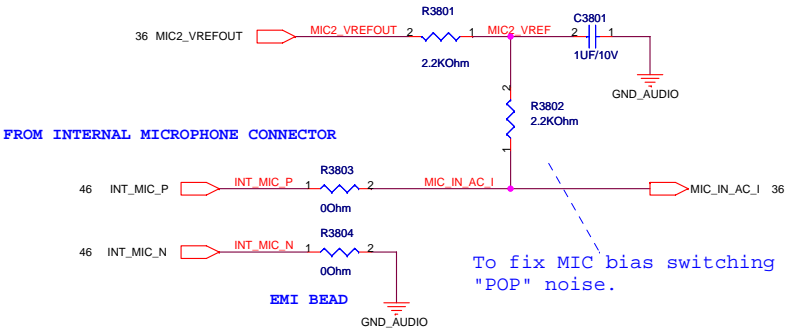


SPEAKER CONNECTOR

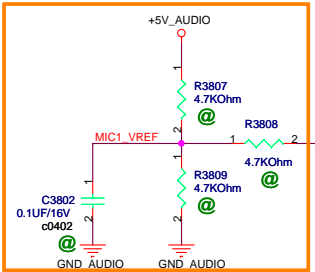
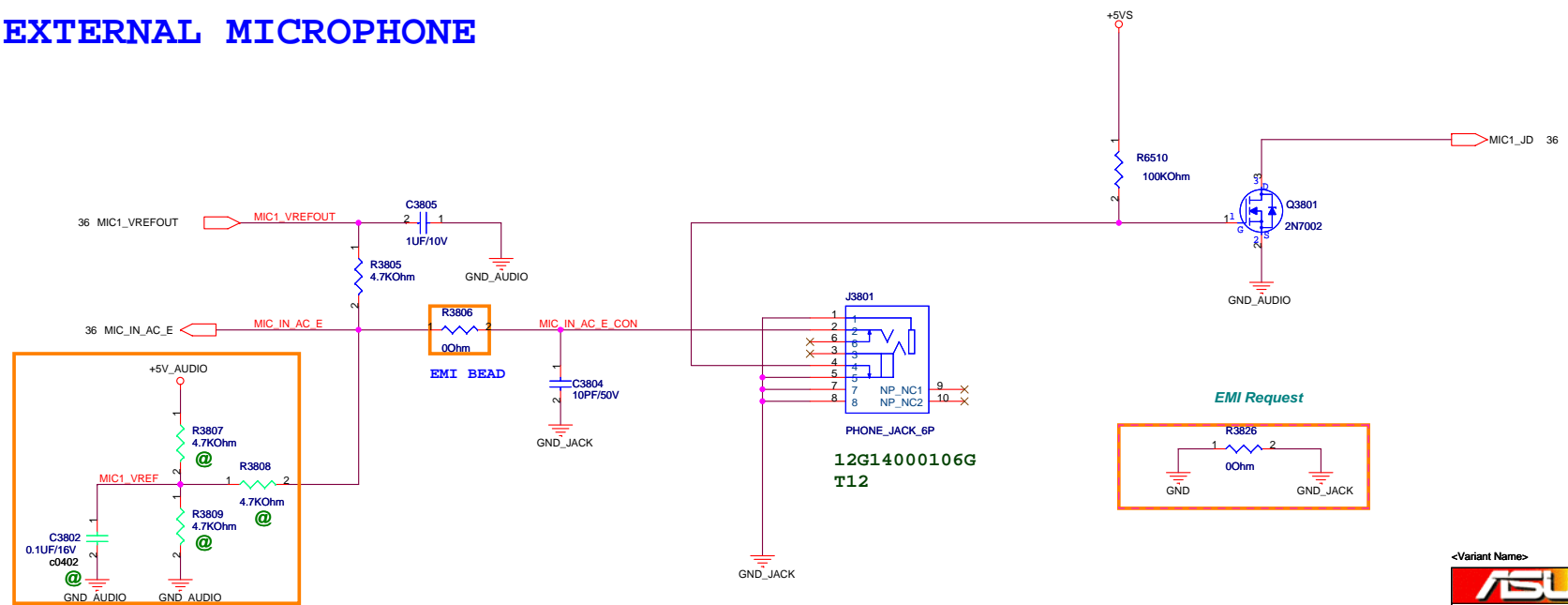


INTERNAL MICROPHONE

+5V_AUDIO ○ +5V_AUDIO 36
 +5VS ○ +5VS 21,30,32,36,37,45,50,51,56,57,80,91



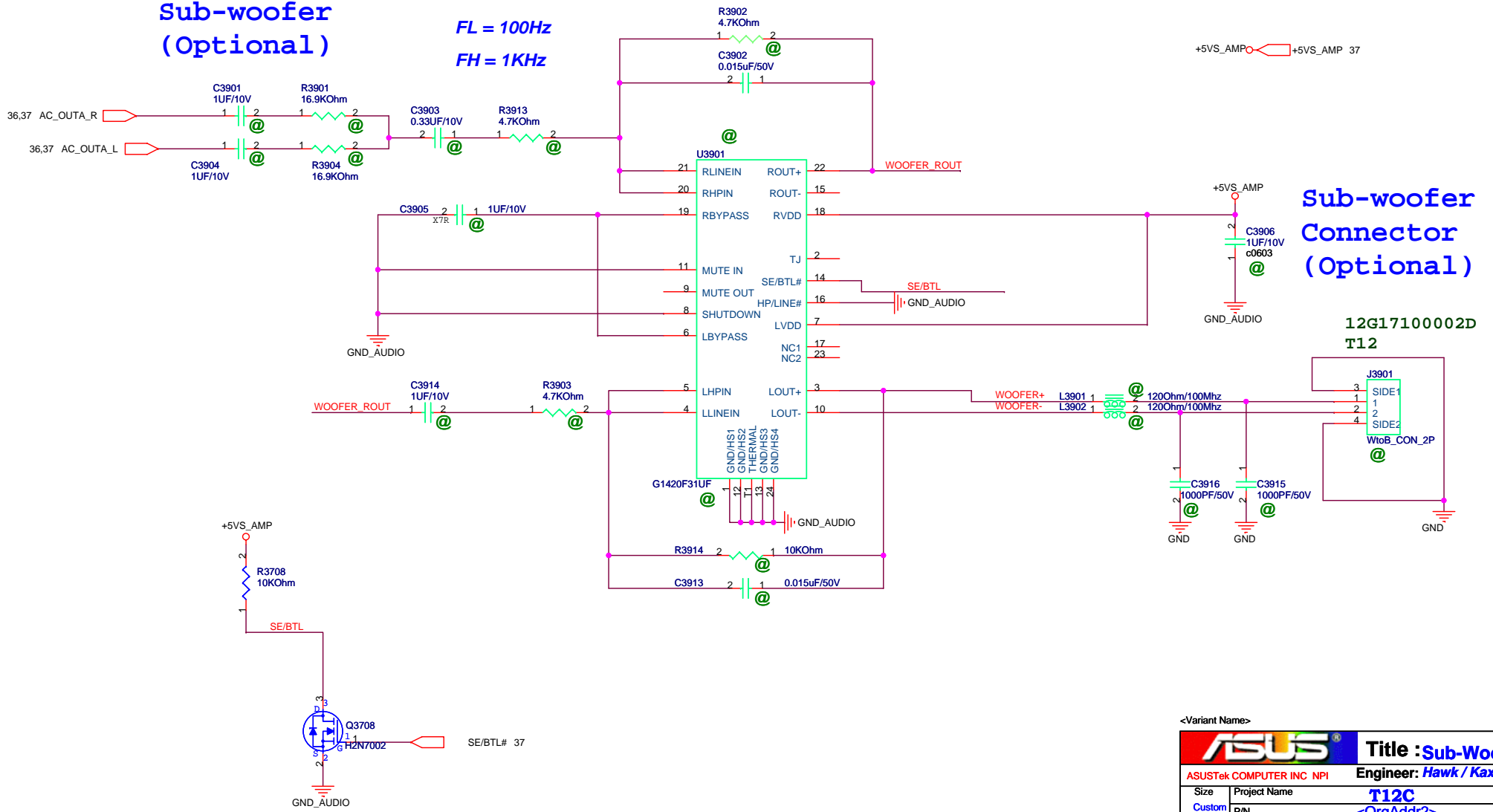
EXTERNAL MICROPHONE



Reserved the external MIC bias(T filter).

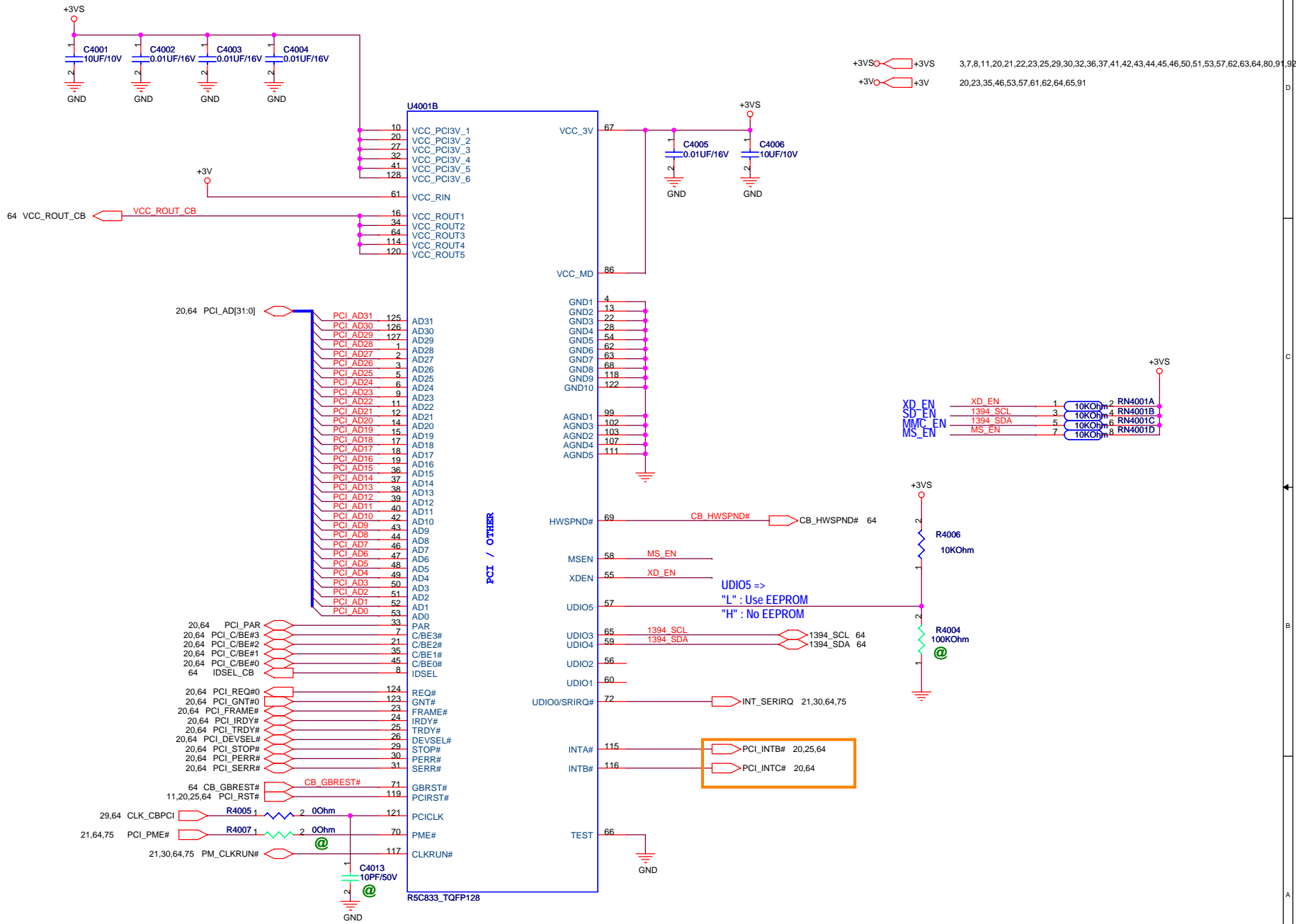
Sub-woofer (Optional)

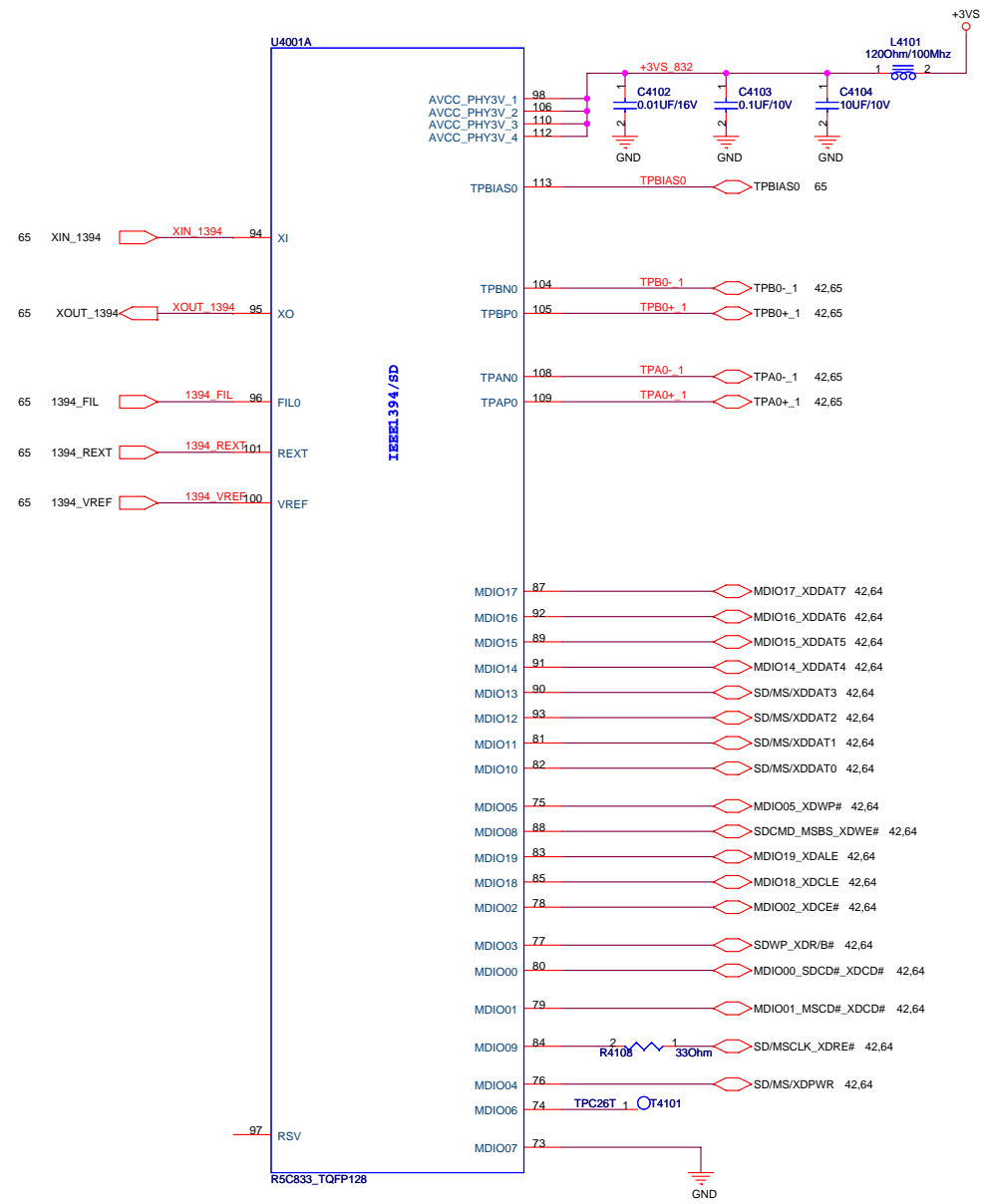
FL = 100Hz
FH = 1KHz



<Variant Name>

		Title : Sub-Woofier	
ASUSTek COMPUTER INC NPI		Engineer: Hawk / Kaxidy	
Size	Project Name	T12C	Rev
Custom	P/N	<OrgAddr2>	1.1
Date: Friday, August 17, 2007		Sheet 39 of 94	

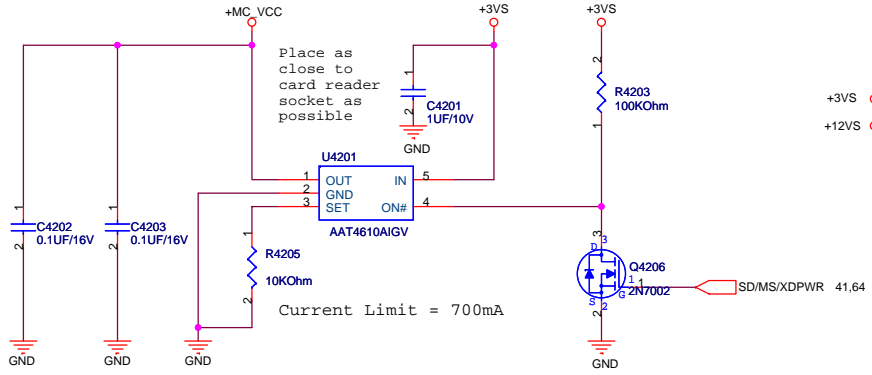




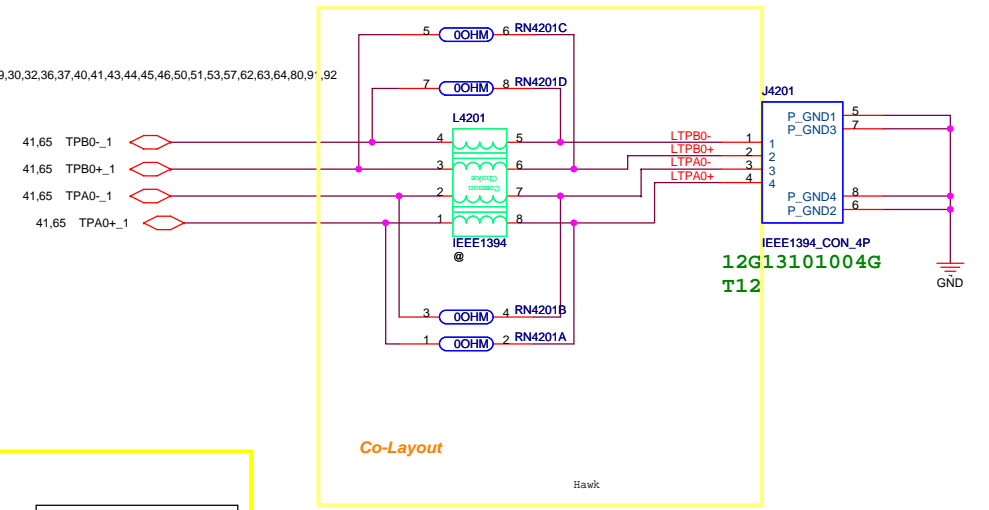
+3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,42,43,44,45,46,50,51,53,57,62,63,64,80,91,92

MDIO00--> SD Card Detect
 MDIO01--> MS Card Detect
 MDIO03--> SD Write Protect
 MDIO04--> SD Card Power0 Control/
 MS Power Control
 MDIO08--> SD Command/MS Bus State
 MDIO09--> SD Clock/MS Clock
 MDIO10--> SD Data 0/MS Data 0
 MDIO11--> SD Data 1/MS Data 1
 MDIO12--> SD Data 2/MS Data 2
 MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
 MDIO05--> SD Power Control 1 / xDWP
 MDIO06--> xD/MS/SD LED Control
 MDIO14--> xD Data
 MDIO15--> xD Data
 MDIO16--> xD Data
 MDIO17--> xD Data
 MDIO18--> xD CLE
 MDIO19--> xD ALE

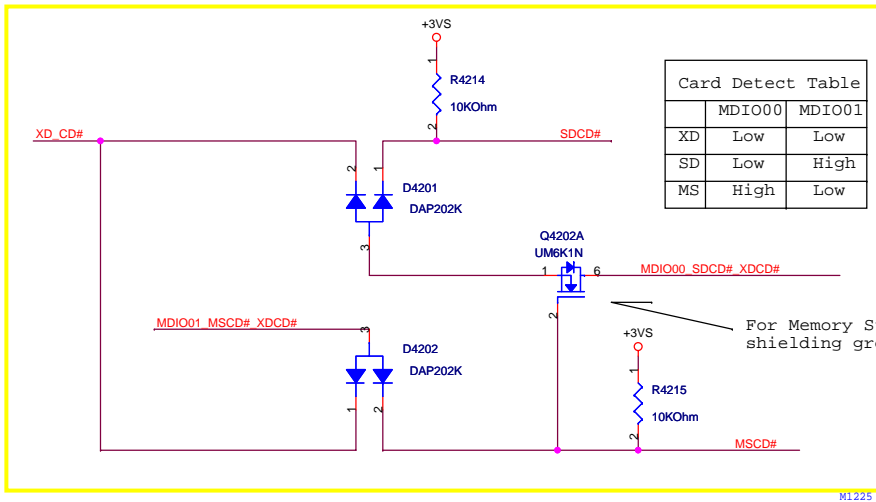
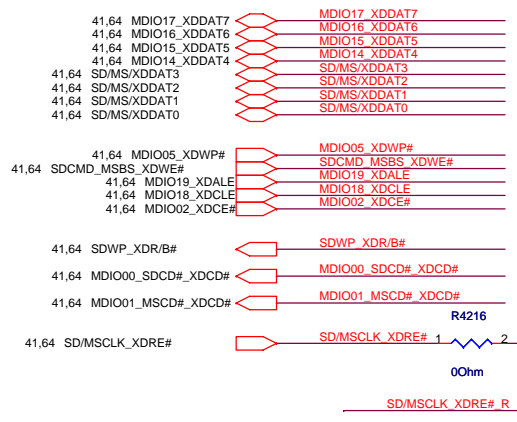


+3VS +3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,41,43,44,45,46,50,51,53,57,62,63,64,80,91,92
 +12VS +12VS 37,46,83,91



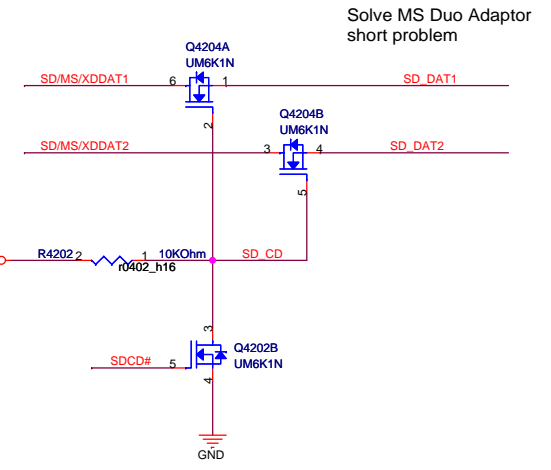
Co-Layout

Hawk

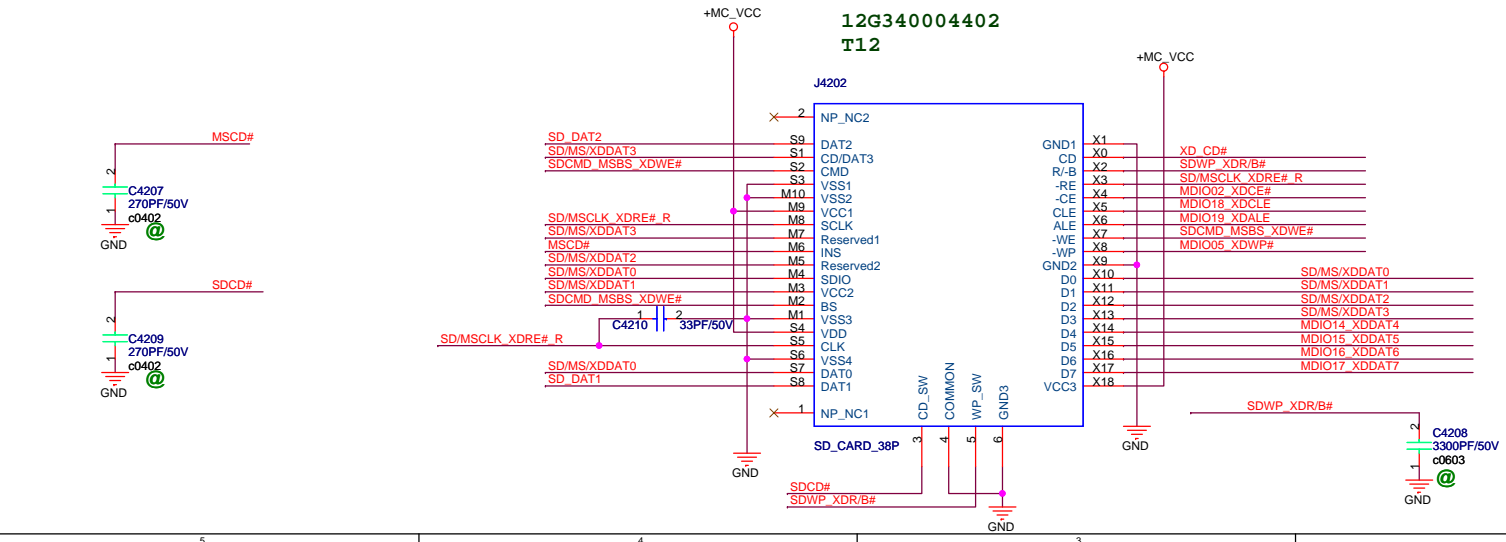


Card Detect Table

	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low



Solve MS Duo Adaptor short problem



<Variant Name>

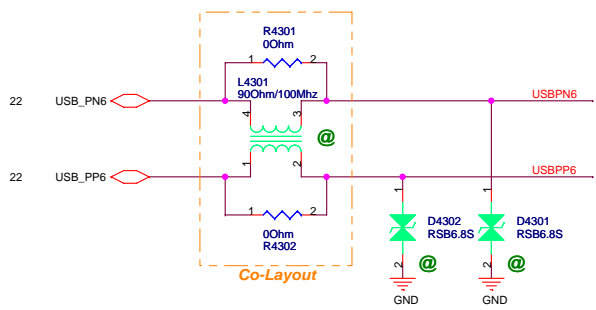
Title : 1394 & CardReader CON

ASUSTek COMPUTER INC Engineer: Arthur & Bruce

Size	Project Name	Rev
Custom	T12C	1.1

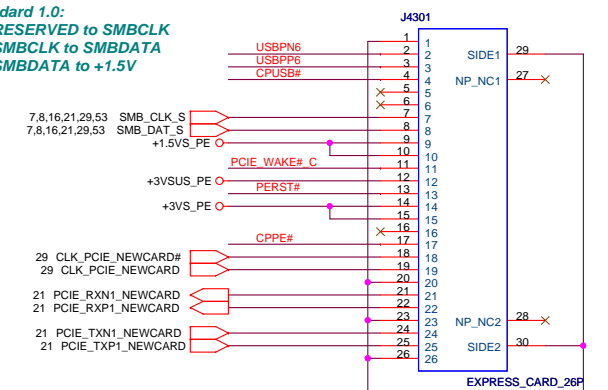
Date: Friday, March 07, 2008 Sheet 42 of 94

Layout: SHIELD GND

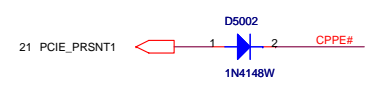
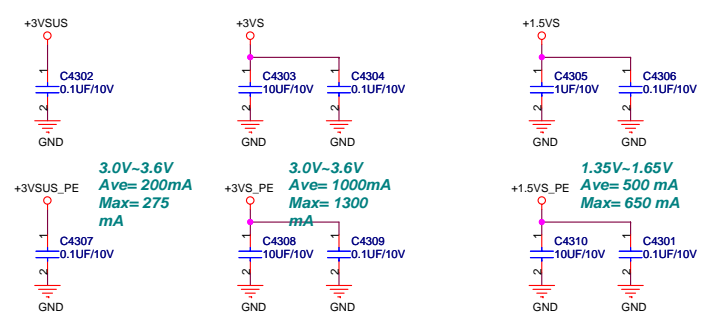
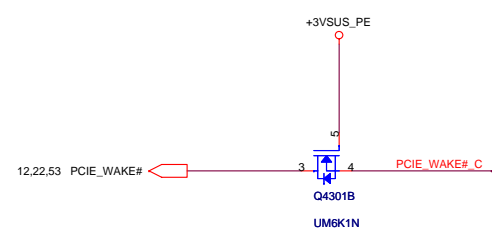
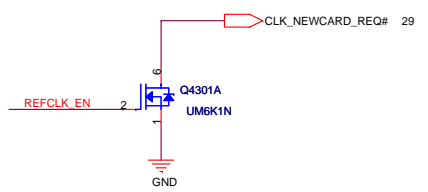
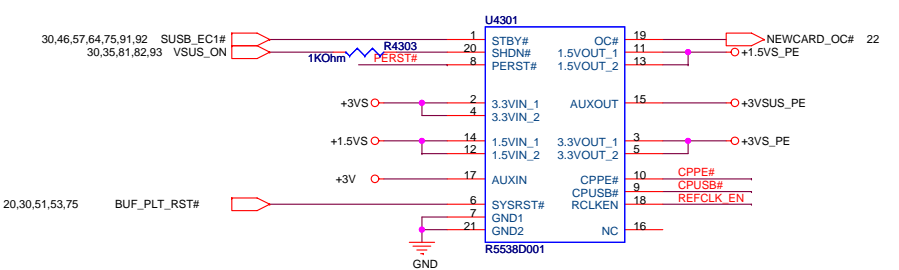


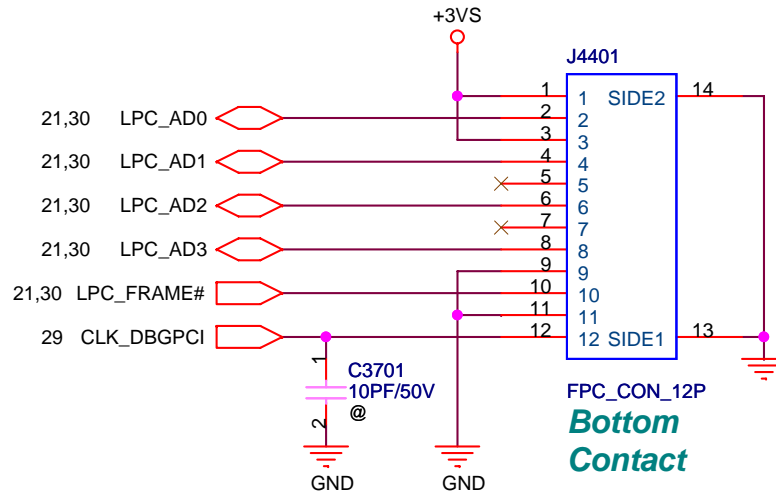
!! ExpressCard Standard 1.0:
 Change Pin7 from RESERVED to SMBCLK
 Change Pin8 from SMBCLK to SMBDATA
 Change Pin9 from SMBDATA to +1.5V

NewCard Header



J4301
 12G161300269
 T12
 J4302
 12G219100002
 T12

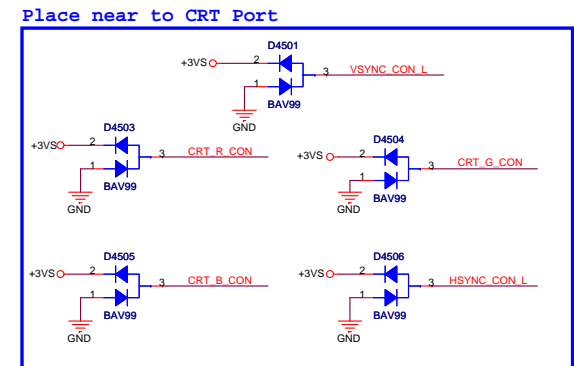
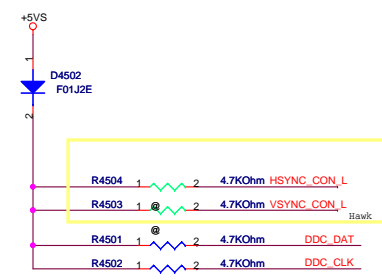
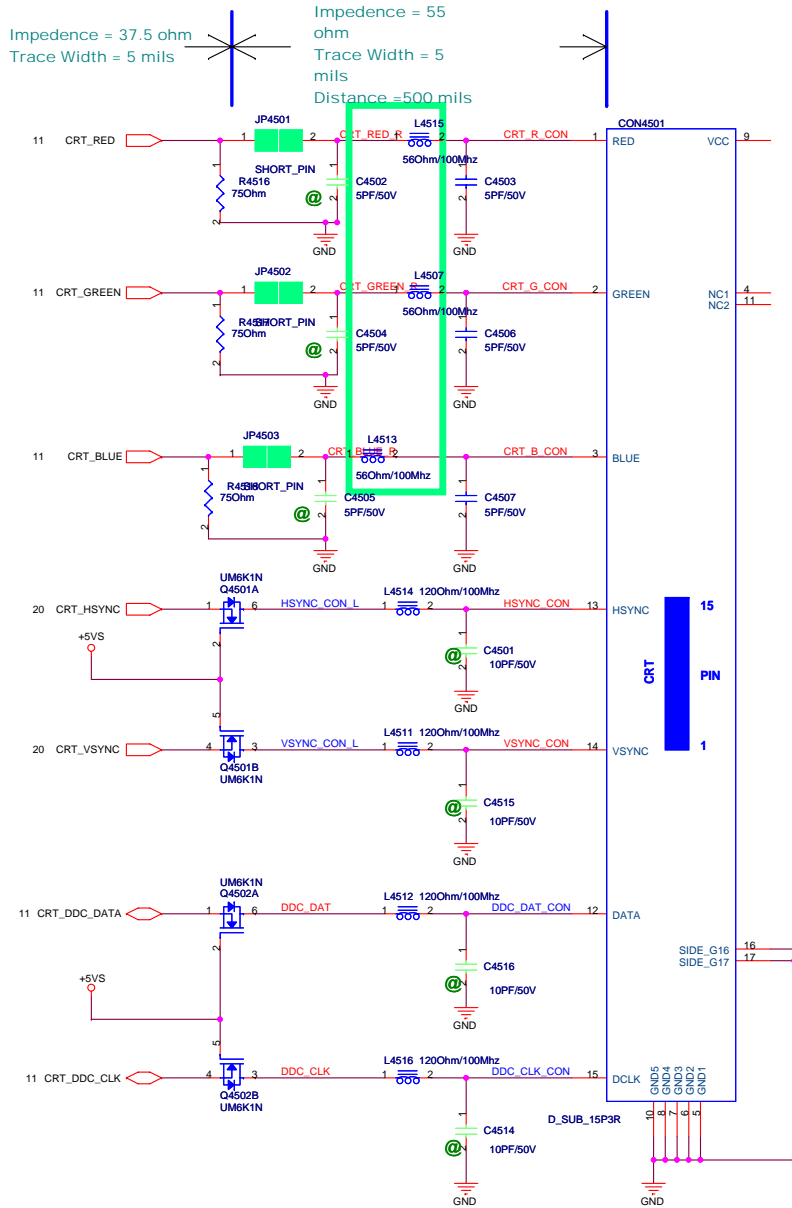




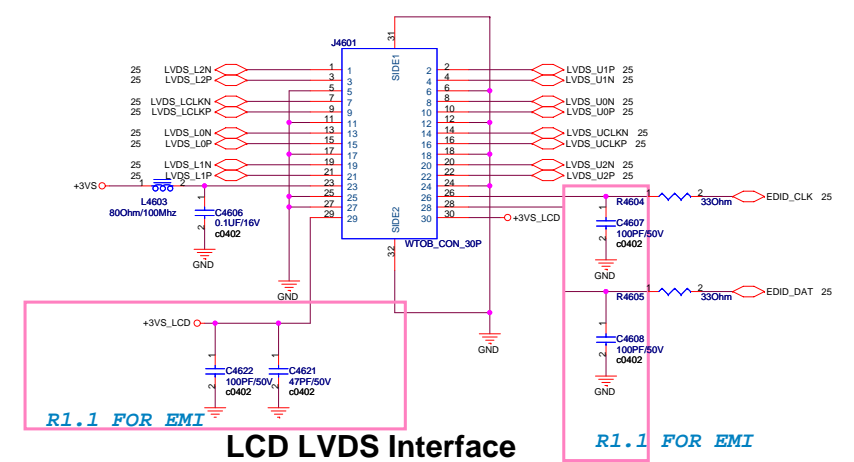
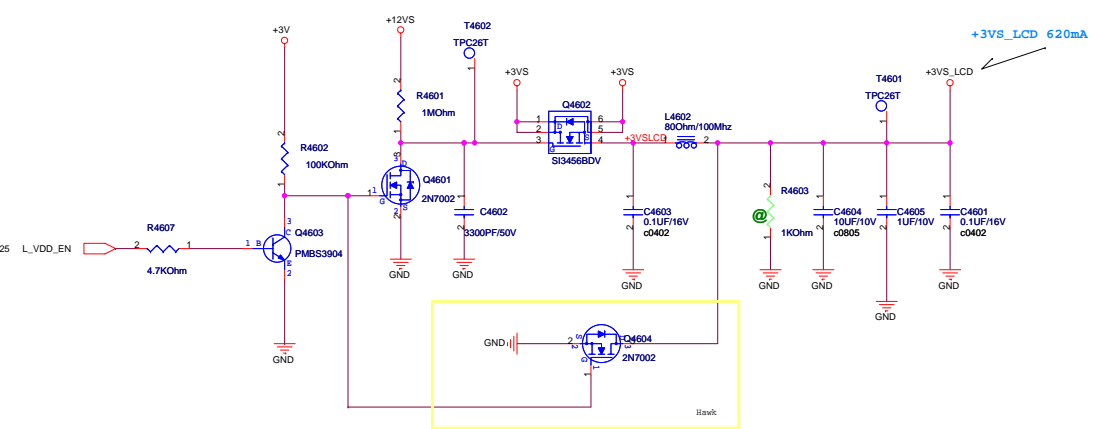
<Variant Name>

		Title :DEBUG
ASUSTeK COMPUTER INC. NB		Engineer: <i>Hawk / Kaxidy</i>
Size A	Project Name T12C	Rev 1.1
Date: Tuesday, February 26, 2008		Sheet 44 of 94

CRT Connector

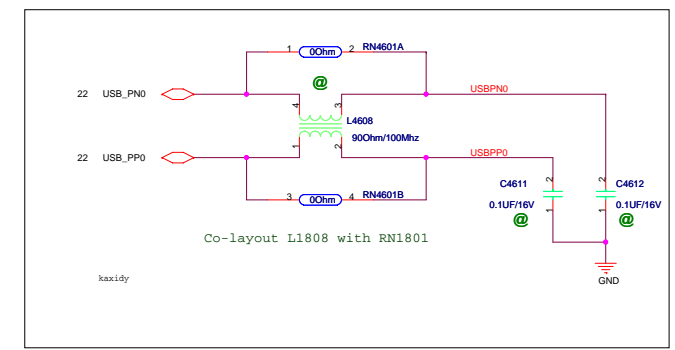
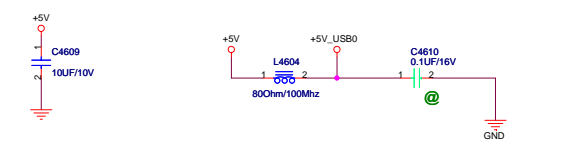
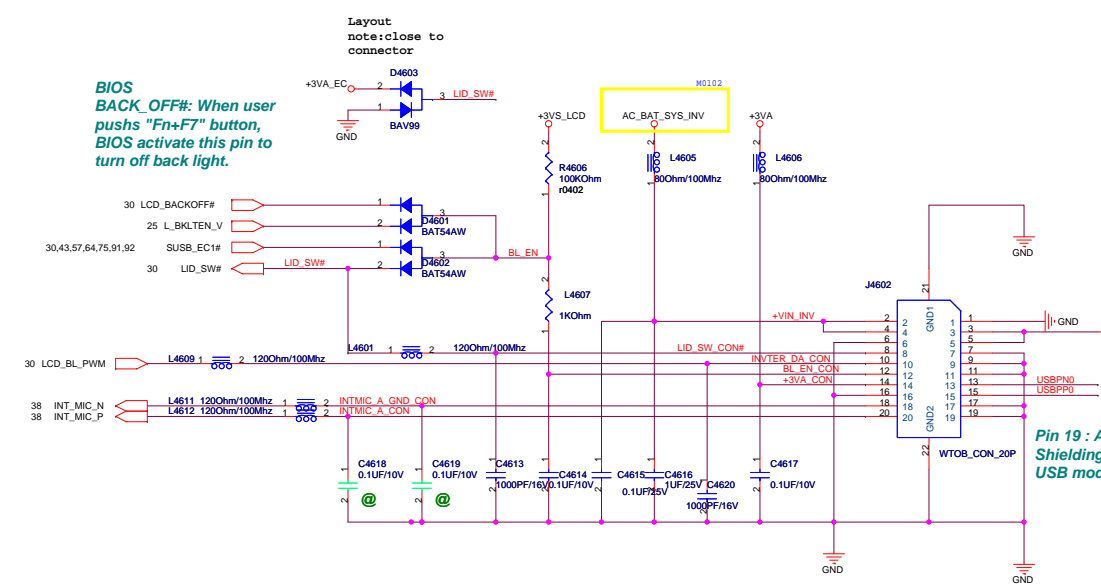


+5VS 21,30,32,36,37,38,50,51,56,57,80,91
 +3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,41,42,43,44,46,50,51,53,57,62,63,64,80,91,92




LCD LVDS Interface

BIOS BACK_OFF#: When user pushes "Fn+F7" button, BIOS activate this pin to turn off back light.

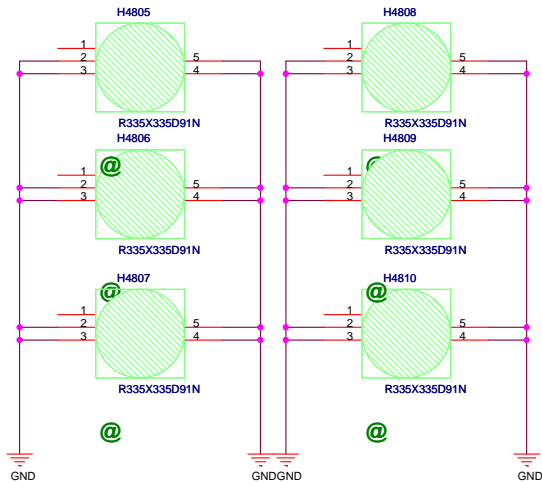


	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

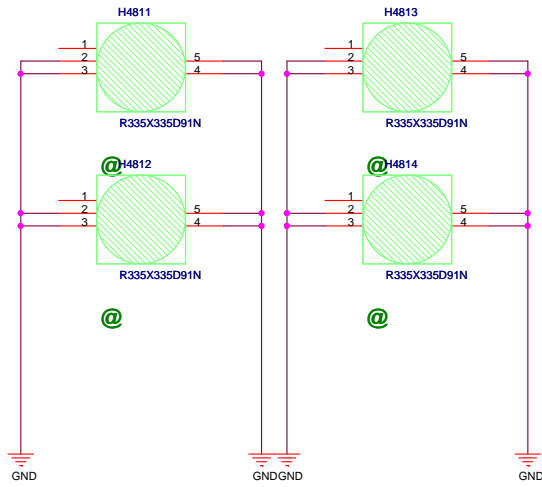
<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy	
Size	Project Name	Rev	
A	T12C	1.1	
Date: Monday, August 13, 2007		Sheet	47 of 94

A Hole / TOP Side



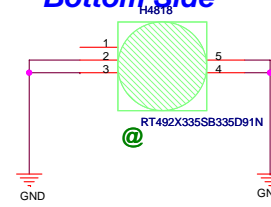
A Hole / Bottom Side



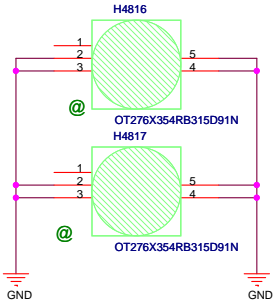
Drill Hole for Fix



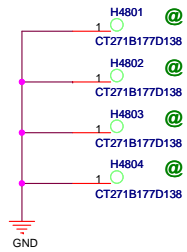
A Hole Special / Bottom Side



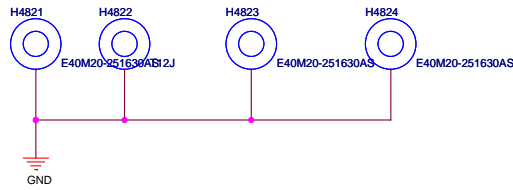
E Hole for Main board fix



F Hole for CPU




銅柱 Hole for VGA 13GNJ510M170-1



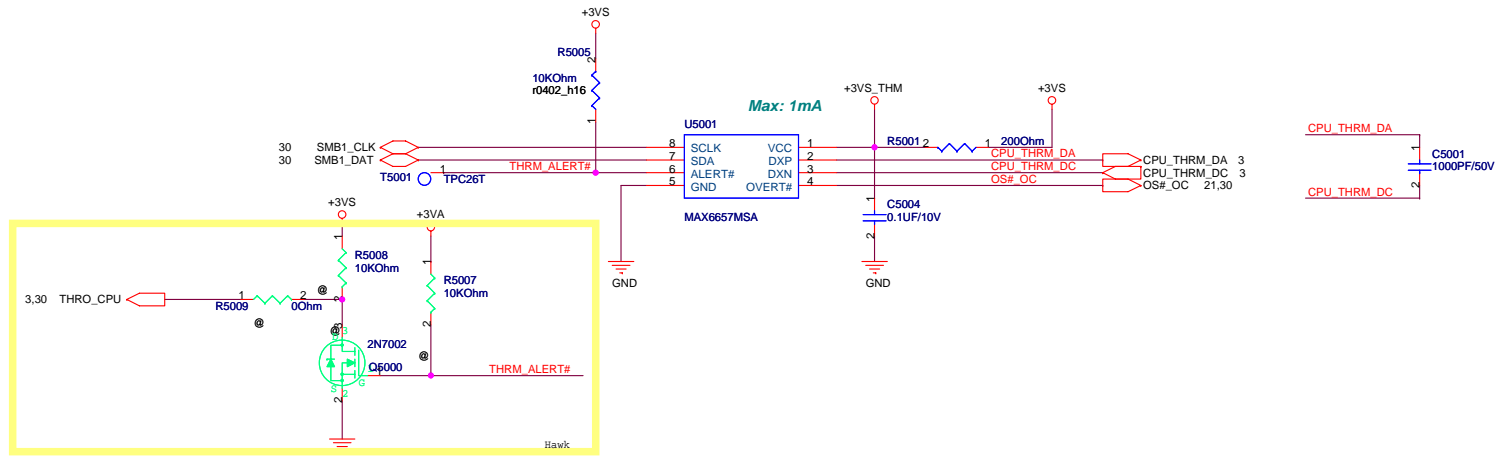
	5	4	3	2	1
D					
C					
B					
A					

<Variant Name>

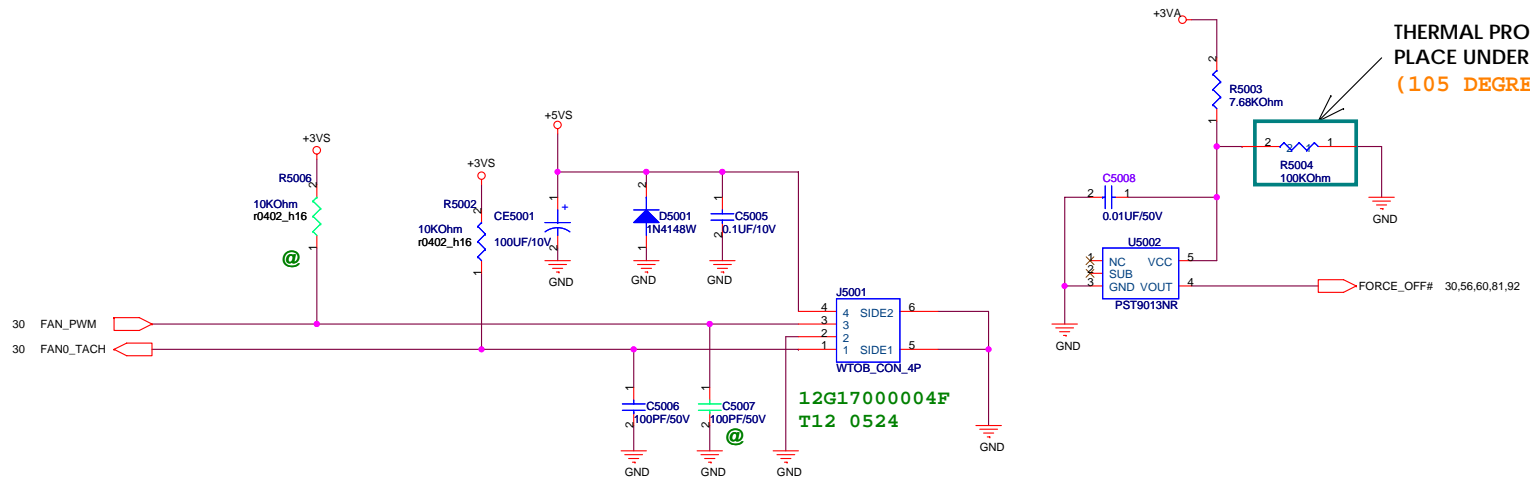
		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>
Size A	Project Name T12C	Rev 1.1
Date: Monday, August 13, 2007		Sheet 49 of 94

	5	4	3	2	1
D					
C					
B					
A					

Thermal Sensor

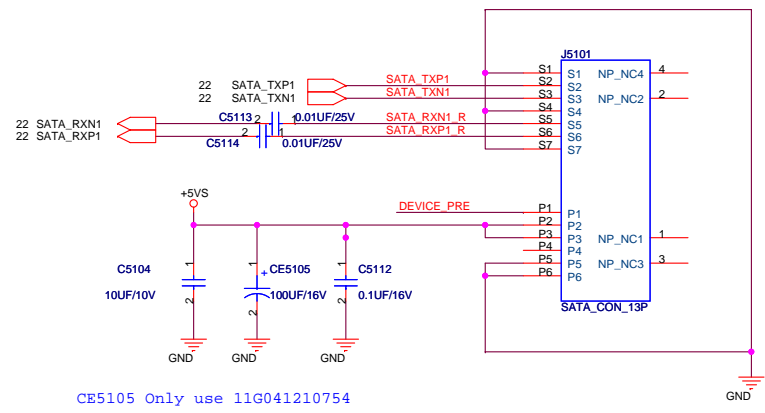
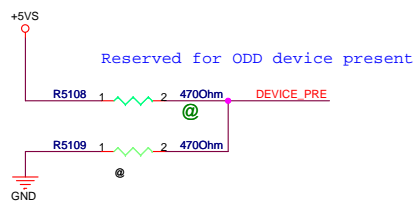
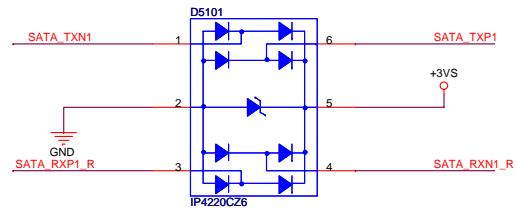
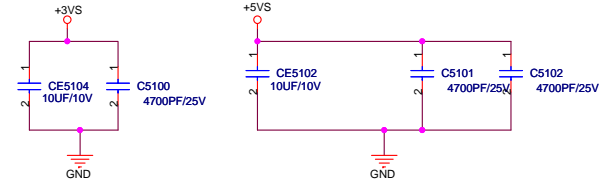
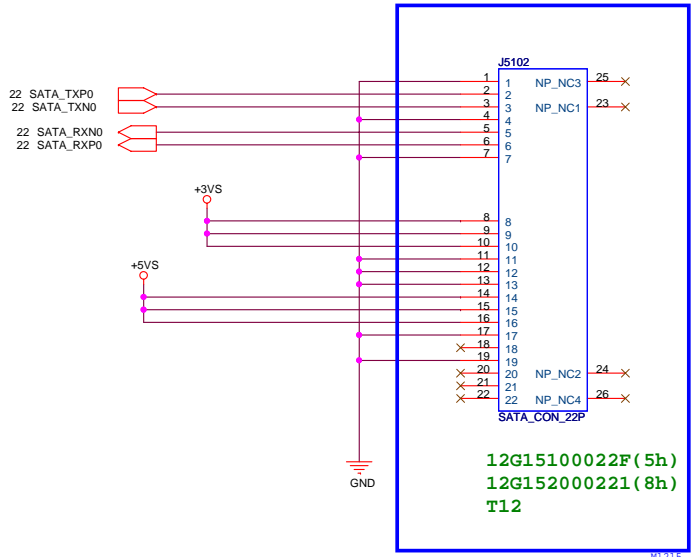


DC FAN Control

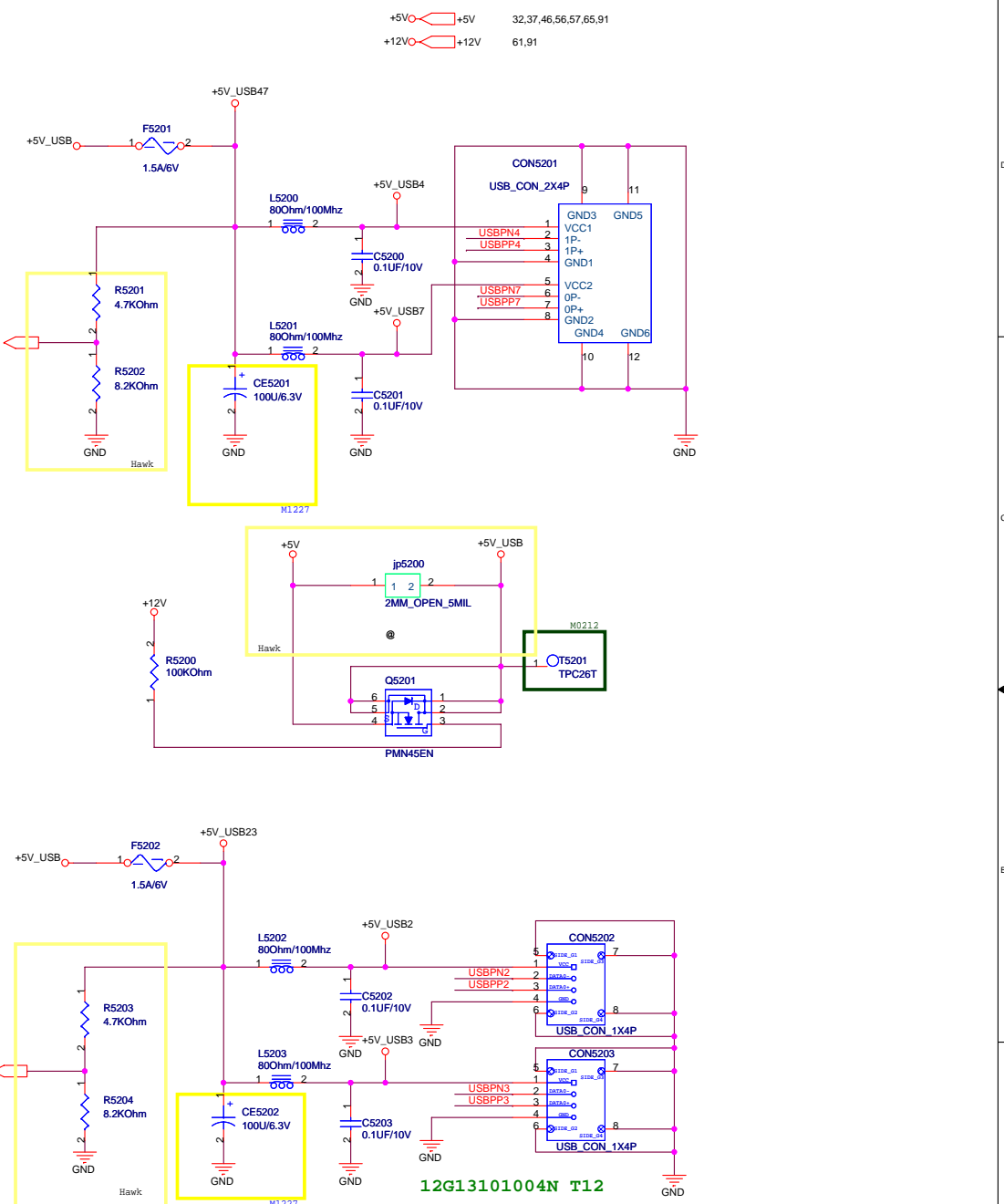
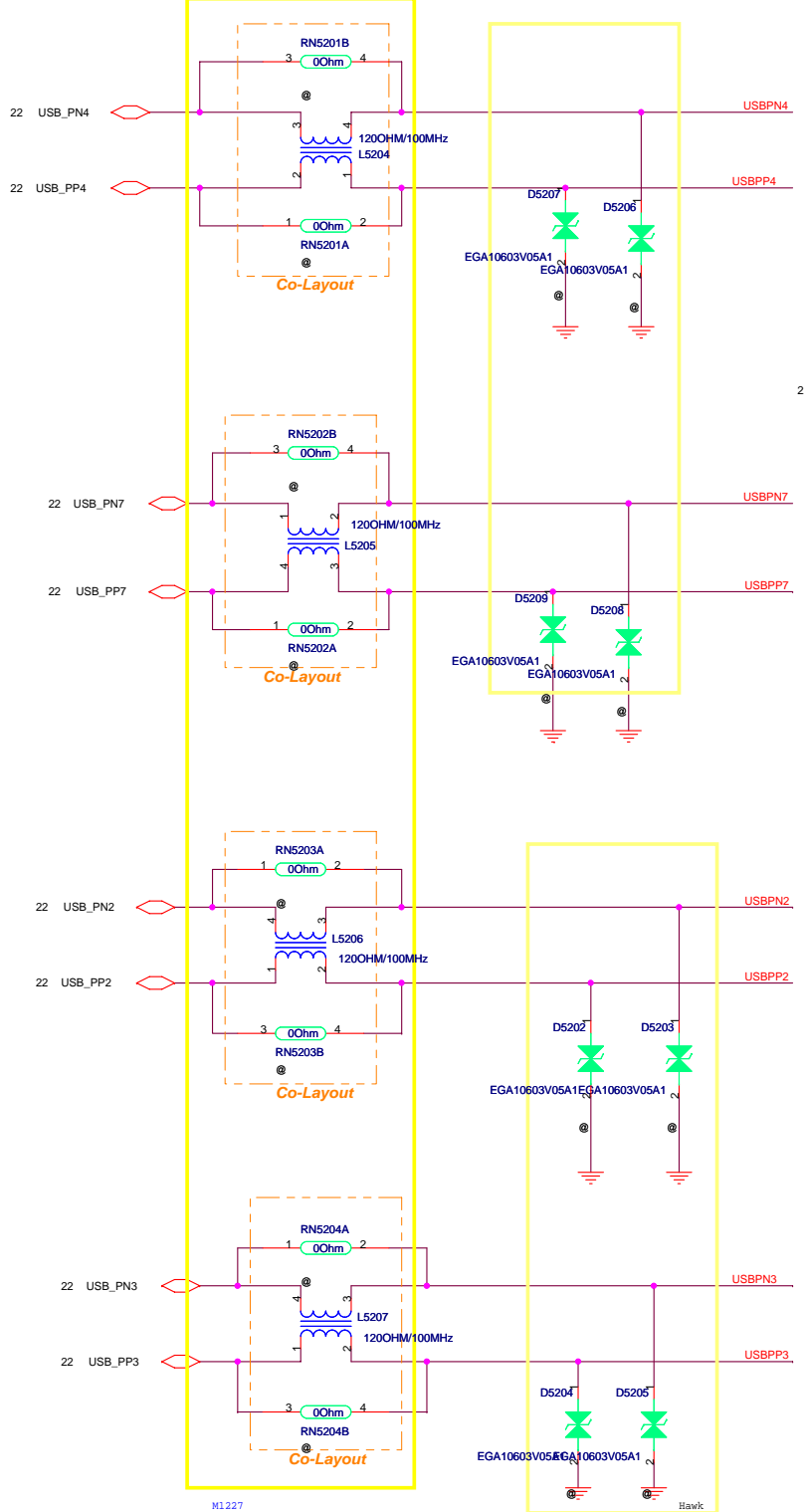


SATA HDD

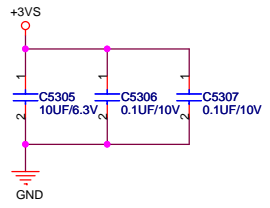
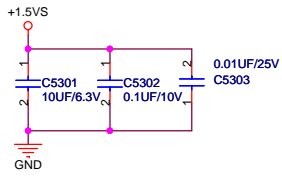
+3VS +3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,41,42,43,44,45,46,50,53,57,62,63,64,80,91,92
 +5VS +5VS 21,30,32,36,37,38,45,50,56,57,80,91



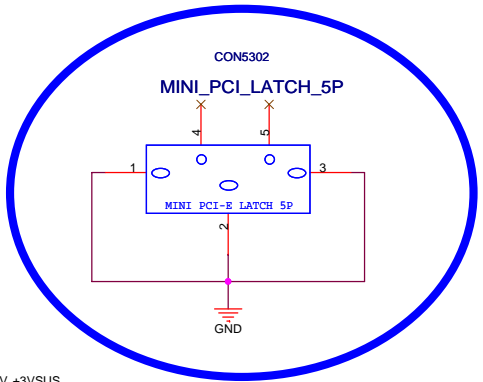
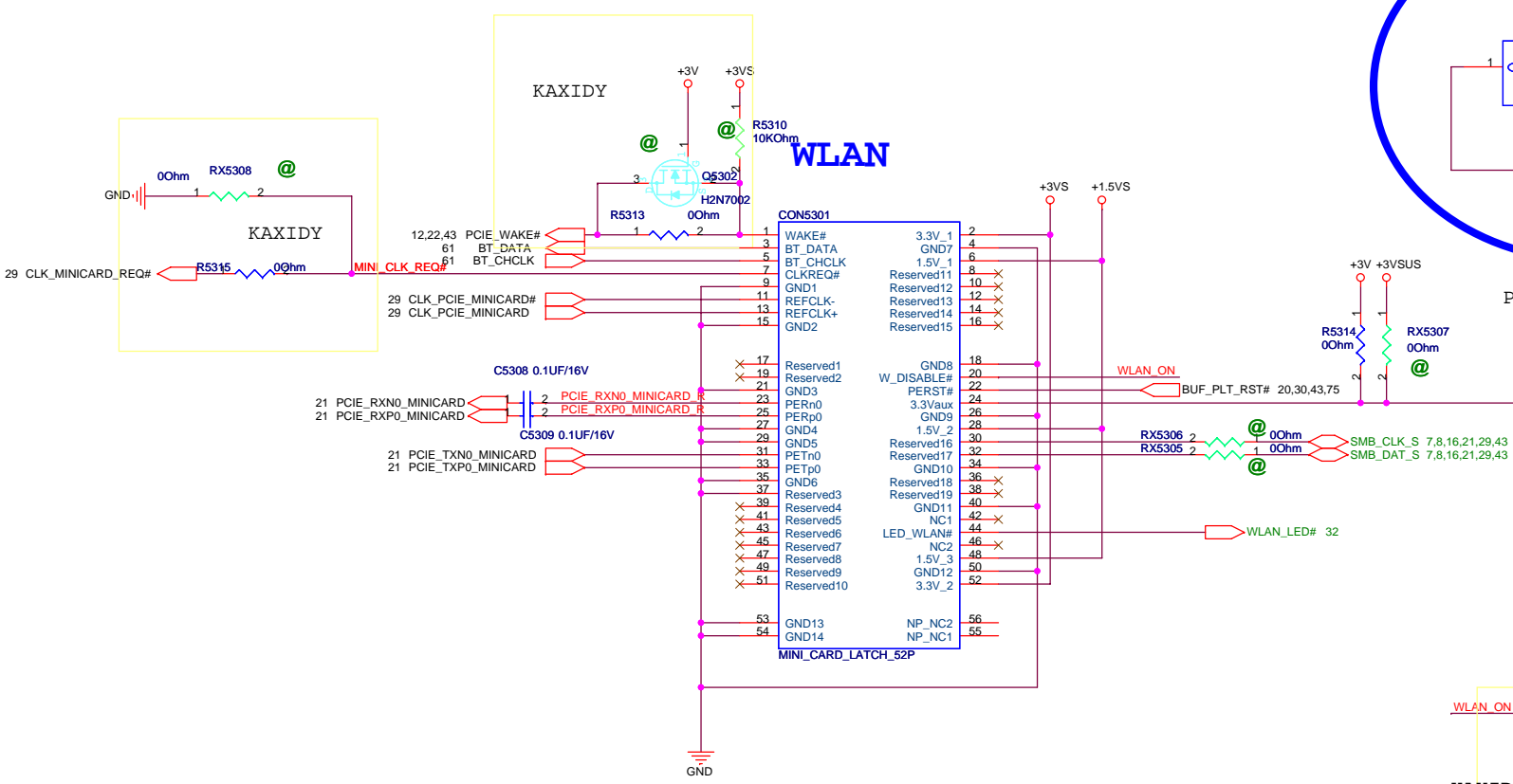
CE5105 Only use 11G041210754



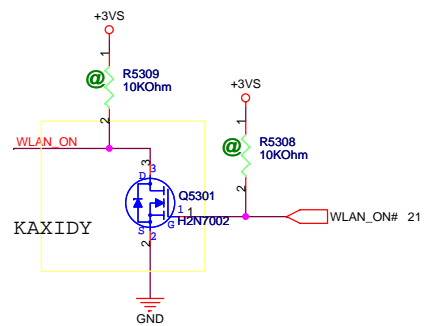
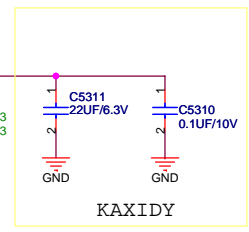
+5V \rightarrow +5V 32,37,46,56,57,65,91
 +12V \rightarrow +12V 61,91



- +3VS \rightarrow +3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,41,42,43,44,45,46,50,51,57,62,63,64,80,91,92
- +3V \rightarrow +3V 20,23,35,40,46,57,61,62,64,65,91
- +1.5VS \rightarrow +1.5VS 4,11,43,57,83



P/N: 12G162210052



<Variant Name>

ASUS		Title : MINICARD	
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy	
Size	Project Name		Rev
Custom	T12C		1.1
Date: Friday, March 07, 2008		Sheet	53 of 94

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>



Title : NULL

ASUSTeK COMPUTER INC

Engineer: Hawk / Kaxidy

Size	Project Name	Rev
A	T12C	1.1

Date: Monday, August 13, 2007

Sheet 54 of 94

5

4

3

2

1

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>



Title : NULL

ASUSTeK COMPUTER INC

Engineer: *Hawk / Kaxidy*

Size	Project Name	Rev
A	T12C	1.1

Date: Monday, August 13, 2007

Sheet 55 of 94

5

4

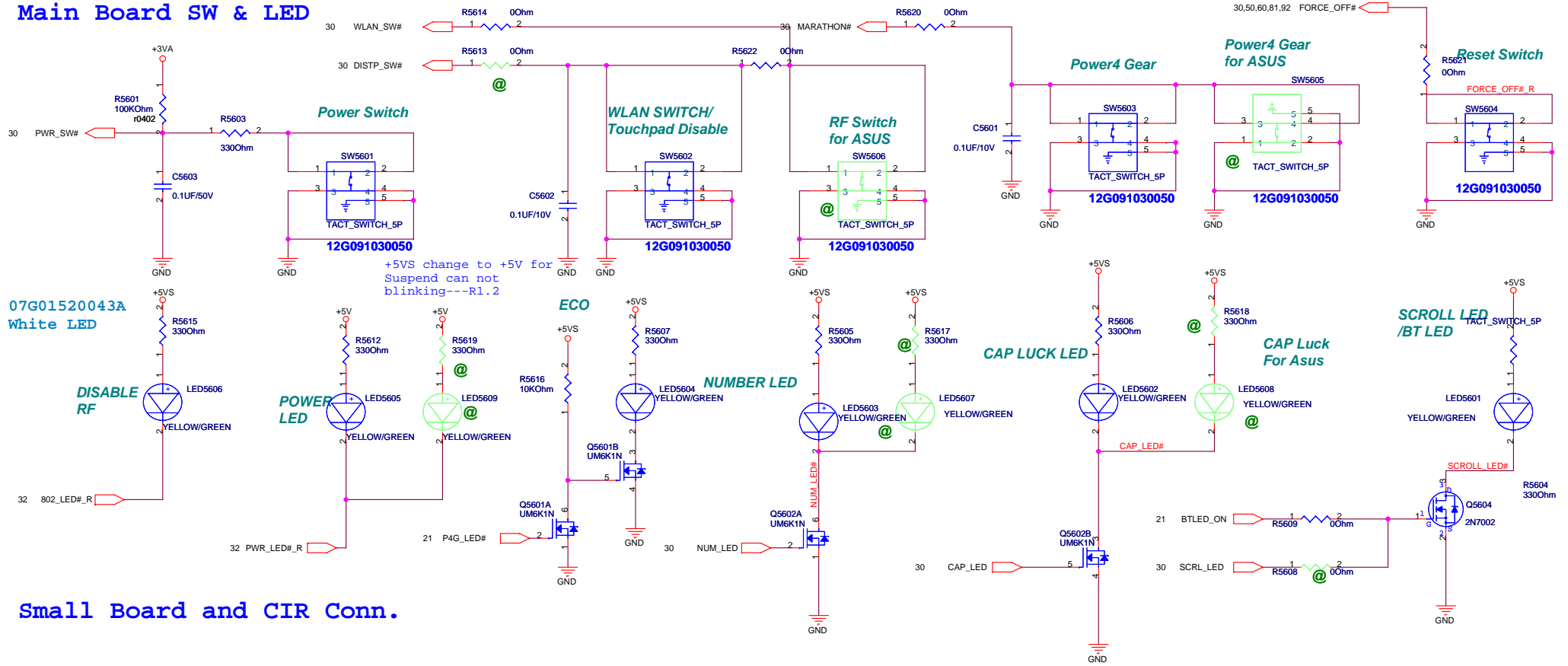
3

2

1

+5V +5V 32,37,46,52,57,65,91
 +5VS +5VS 21,30,32,36,37,38,45,50,51,57,80,91
 +3VA +3VA 21,30,46,50,57,81,93







Main Board SW & LED

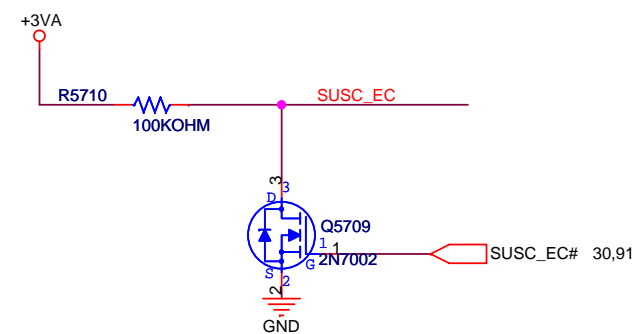
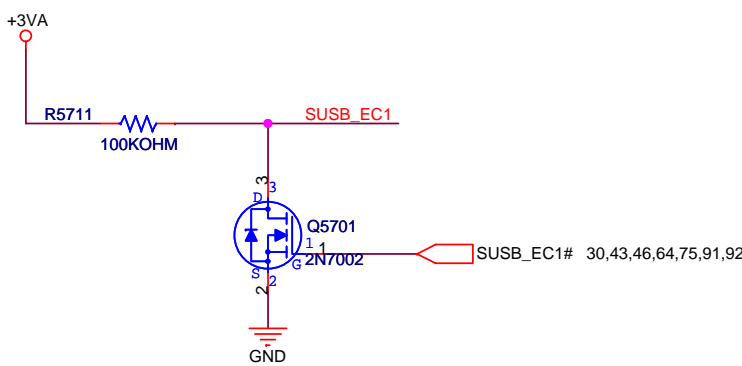
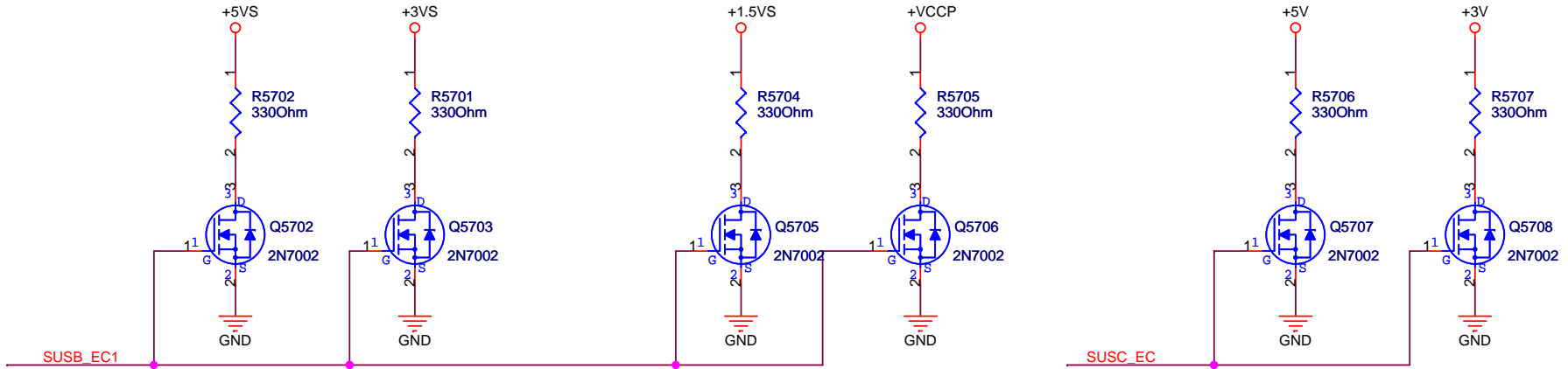



+5VS change to +5V for Suspend can not blinking---R1.2

07G01520043A
White LED

Small Board and CIR Conn.

- +3V  +3V 20,23,35,40,46,53,61,62,64,65,91
- +5V  +5V 32,37,46,52,56,65,91
- +VCCP  +VCCP 4,10,14,21,23,29,83,92
- +1.5VS  +1.5VS 4,11,43,53,83
- +3VS  +3VS 3,7,8,11,20,21,22,23,25,29,30,32,36,37,40,41,42,43,44,45,46,50,51,53,62,63,64,80,91,92
- +5VS  +5VS 21,30,32,36,37,38,45,50,51,56,80,91



		Title :DISCHARGE	
ASUSTeK COMPUTER INC. NB		Engineer: <i>Hawk / Kaxidy</i>	
Size	Project Name	Rev	
Custom	T12C	1.1	
Date: Tuesday, March 04, 2008	Sheet 57 of 94		

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>



Title : NULL

ASUSTeK COMPUTER INC

Engineer: Hawk / Kaxidy

Size	Project Name	Rev
A	T12C	1.1

Date: Monday, August 13, 2007

Sheet 58 of 94

5

4


3

2

1

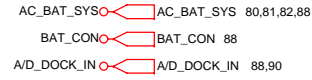
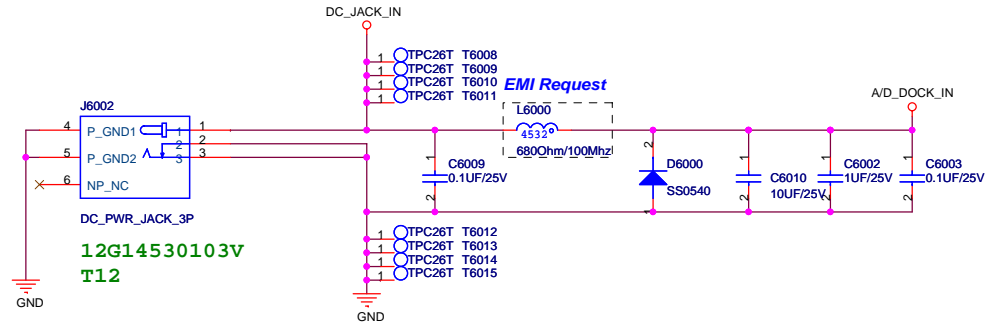
	5	4	3	2	1
D					
C					
B					
A					

<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: Hawk / Kaxidy
Size	Project Name	Rev
A	T12C	1.1
Date: Monday, August 13, 2007		Sheet 59 of 94

	5	4	3	2	1
--	---	---	---	---	---

DC-IN



For Battery

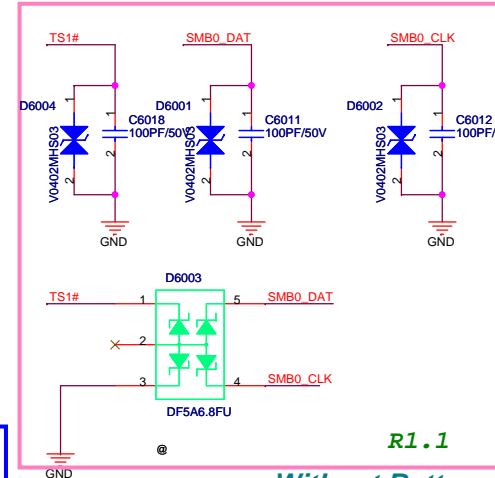
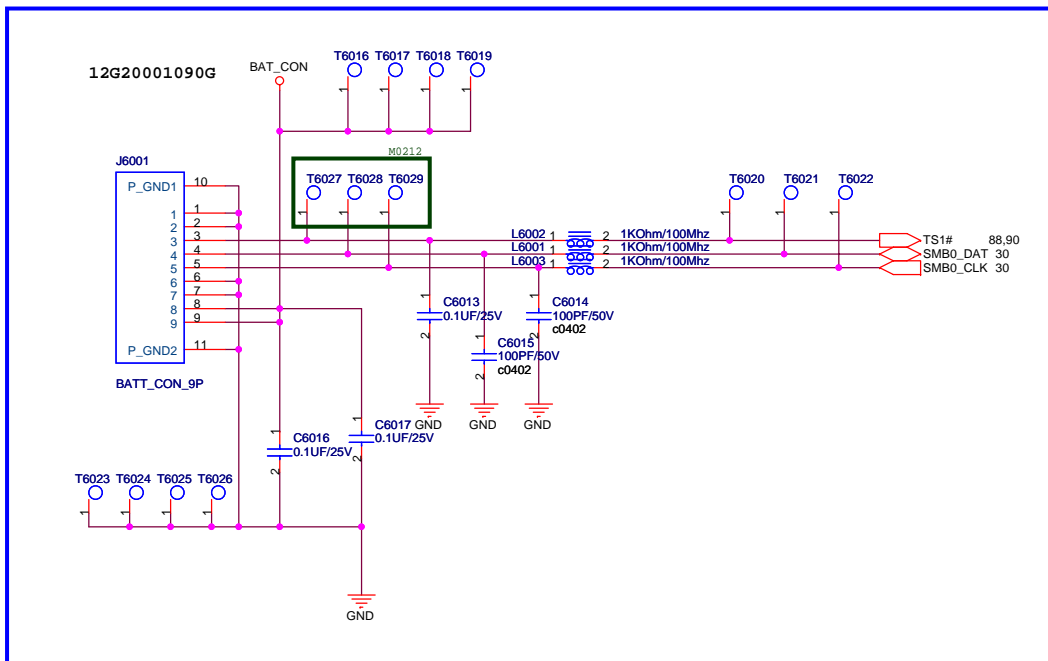
Single Battery

BAT1_CNT1#, BAT1_CNT2#,
 BAT2_CNT1#, BAT2_CNT2#
 don't connect to Battery
 Connector.

Dual Battery

BAT1_CNT1#, BAT1_CNT2#,
 BAT2_CNT1#, BAT2_CNT2#
 must connect to Battery
 Connector.

Battery Connector

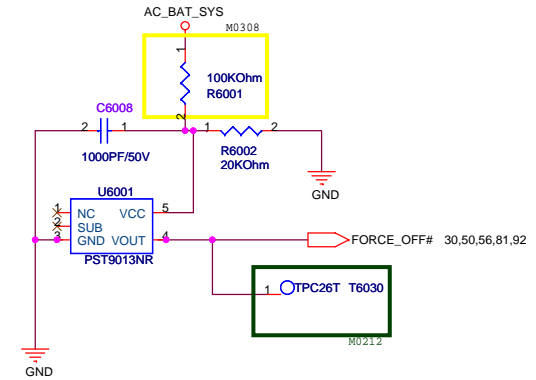


Note:

When we plug in or plug out the battery, it may cause a spike to damage the EC and gas gauge. It needed to add these varistors to protect those pins.

close to connector

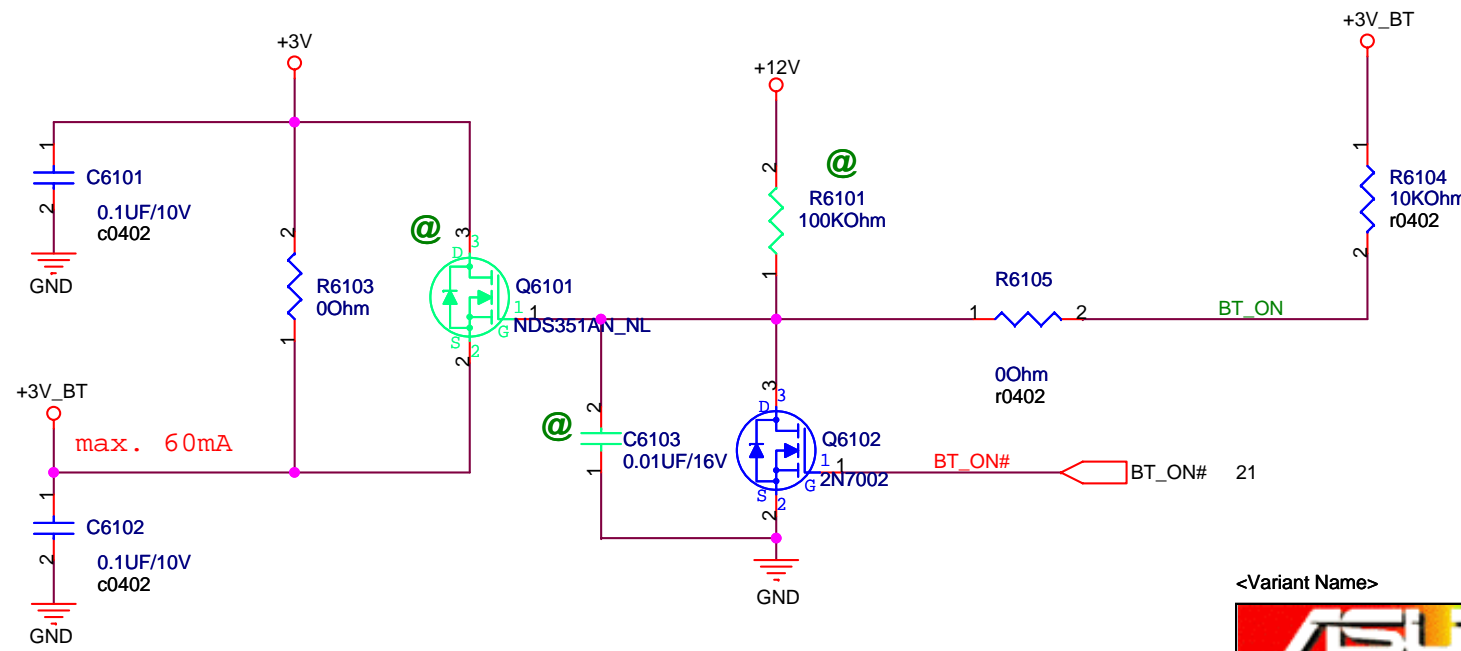
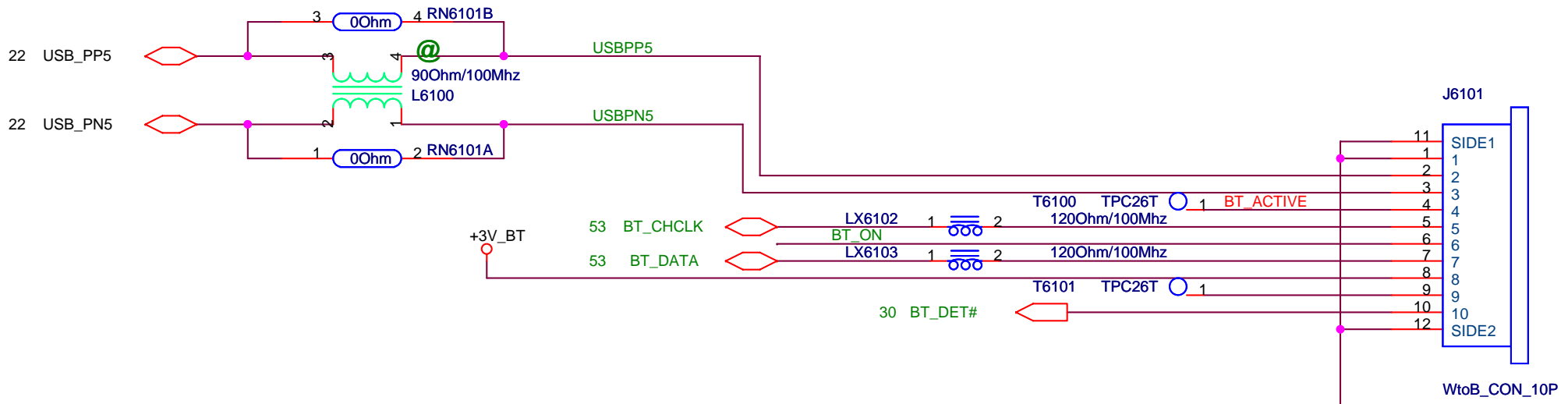
Without Battery & Pull out Adapter



<Variant Name>

ASUS		Title : DCIN/Batt conn.	
ASUSTeK COMPUTER INC. NB		Engineer: Hawk / Kaxidy	
Size	Project Name		Rev
Custom	T12C		1.1
Date: Friday, August 17, 2007	Sheet	60	of 94

BLUETOOTH CONNECTOR




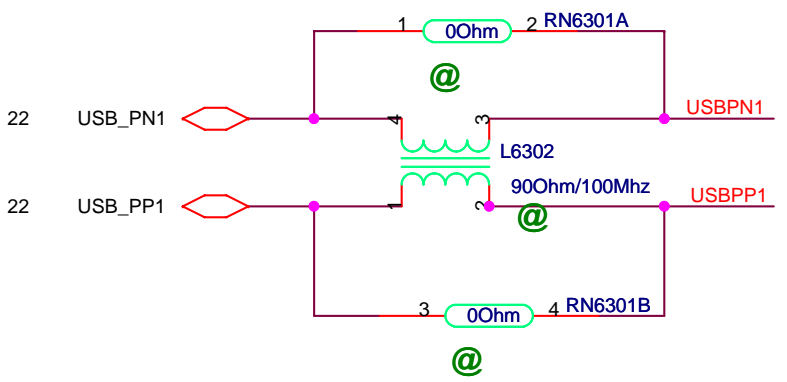
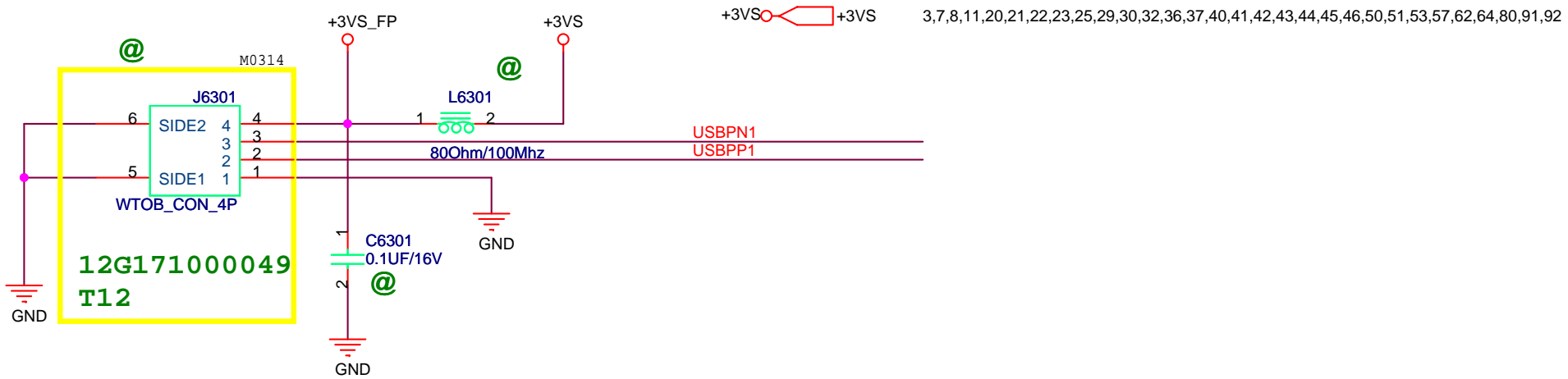
<Variant Name>

		Title : Blue Tooth
ASUSTeK COMPUTER INC .NB		Engineer: Hawk / Kaxidy
Size A	Project Name T12C	Rev 1.1
Date: Friday, August 17, 2007		Sheet 61 of 94

TPM Connector

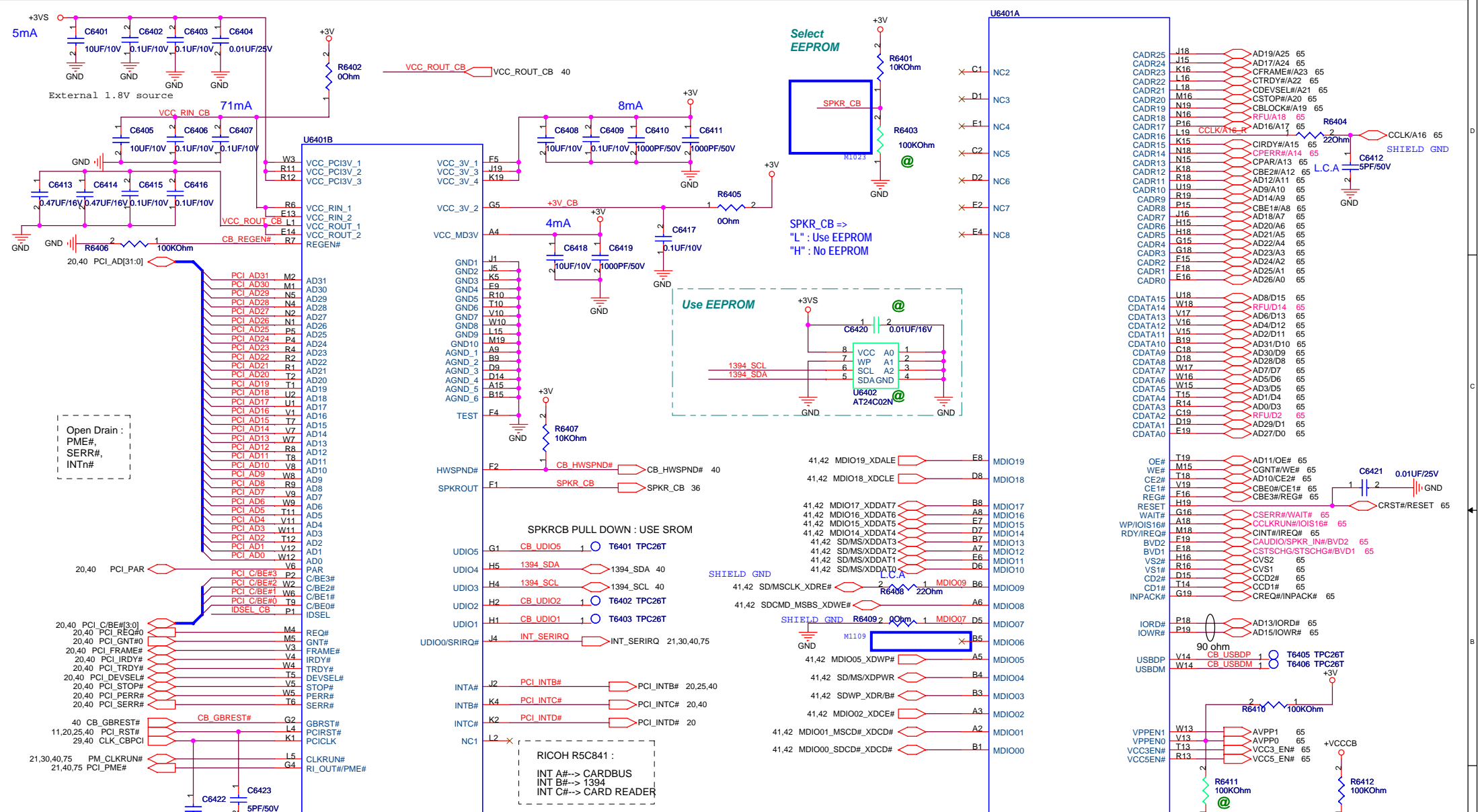
<Variant Name>

		Title : TPM
ASUSTeK COMPUTER INC. NB		Engineer: Hawk / Kaxidy
Size A	Project Name T12C	Rev 1.1
Date: Tuesday, March 04, 2008		Sheet 62 of 94

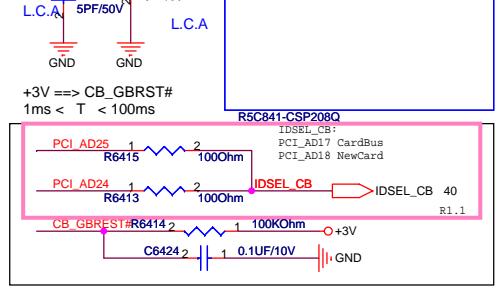


<Variant Name>

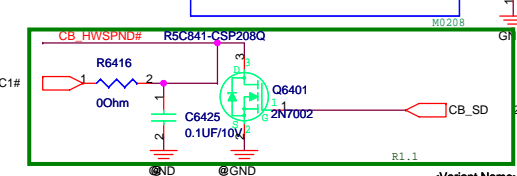
		Title :Finger Print
ASUSTeK COMPUTER INC. NB		Engineer: <i>Hawk / Kaxidy</i>
Size A	Project Name T12C	Rev 1.1
Date: Friday, August 17, 2007		Sheet 63 of 94



Open Drain :
PME#,
SERR#,
INTn#

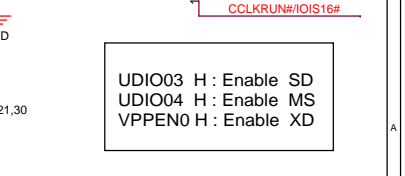


RICOH R5C841 :
INT A#--> CARDBUS
INT B#--> 1394
INT C#--> CARD READER



GBRST# POWER SEQ
+3V ==> (GBRST#/CB_HWSUSP#) ==> PCIRST#

H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO=> PCIRST# LO=> +3VS OFF
RESUME : +3VS ON => PCIRST# HI=> CB_HWSUSP# HI



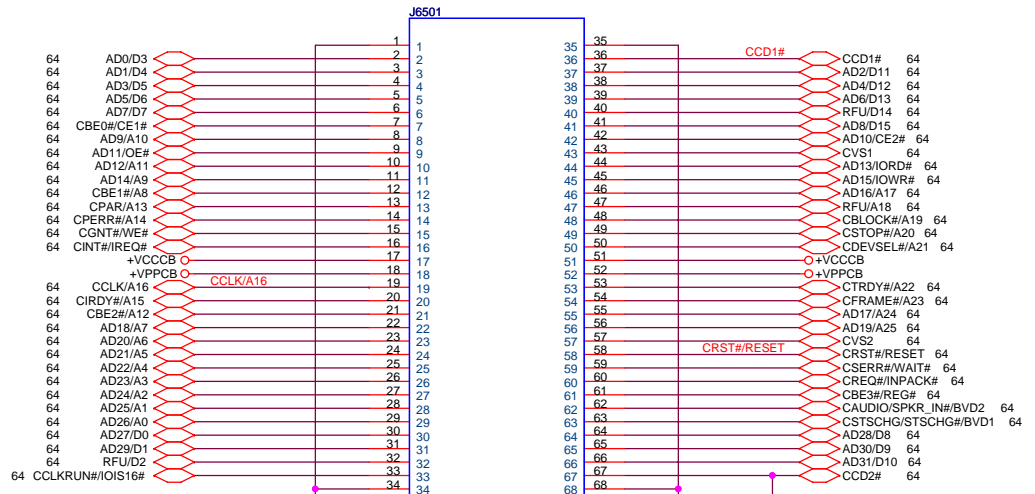
ASUS Title : **RICOH R5C841**
ASUSTek COMPUTER INC Engineer : **Hawk / Kaxidy**

Size Project Name
Custom T12C

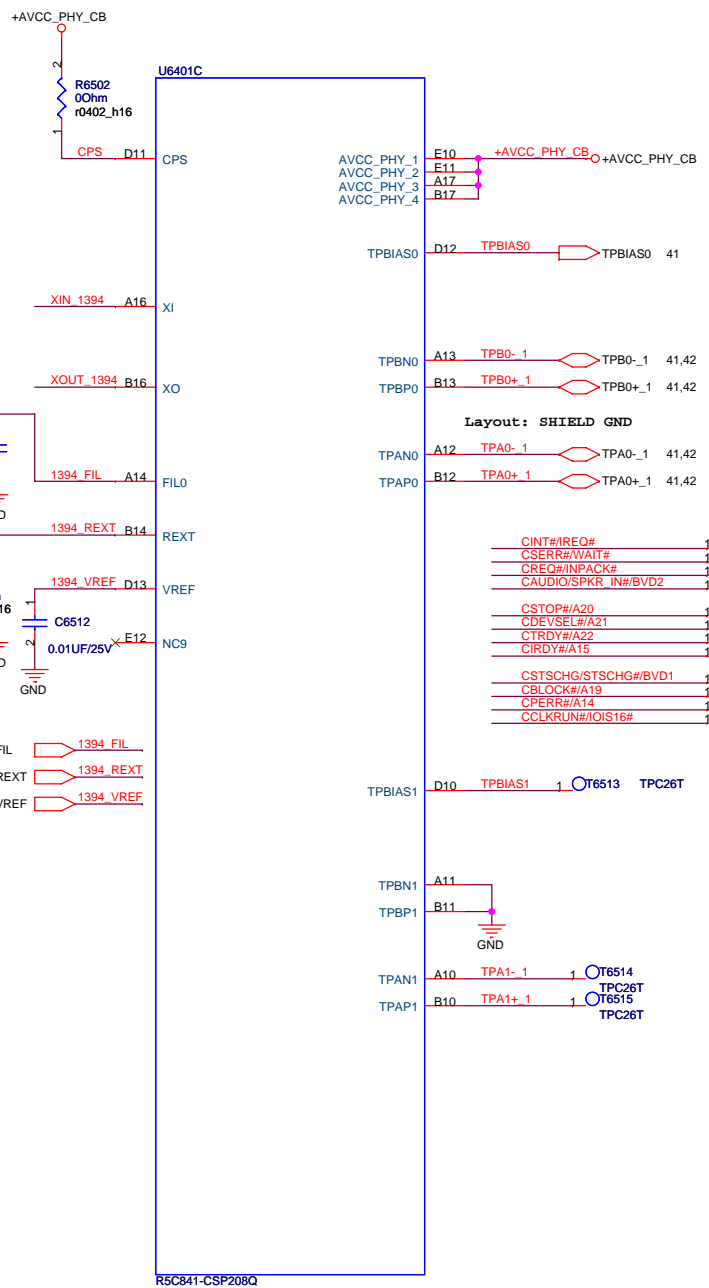
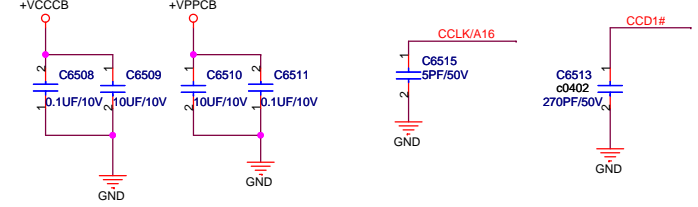
Date: **Tuesday, March 04, 2008** Sheet **64** of **94**

PCMCIA SOCKET

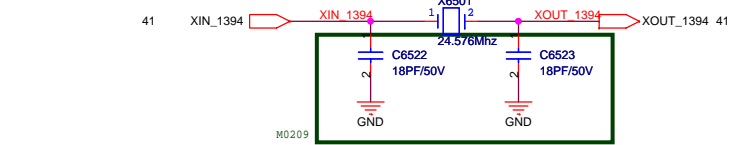
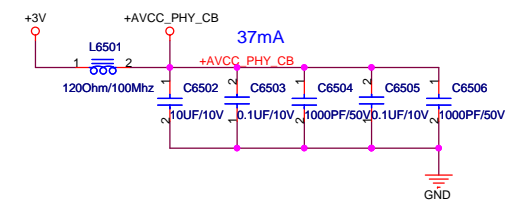
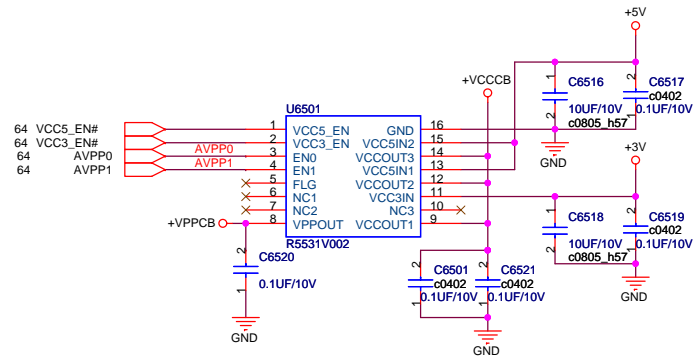
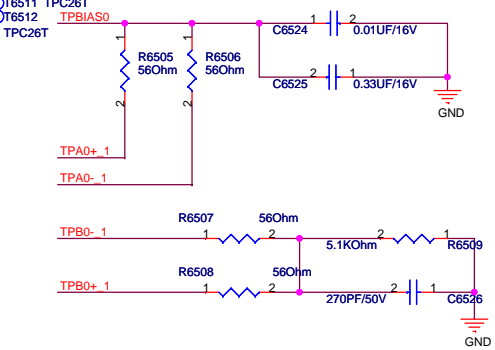
CCD1# CCD2#
L L 16bit
OTHER 32bit



12G160420683



- CINT#/IREQ# 1 T6502 TPC26T
- CSERR#/WAIT# 1 T6503 TPC26T
- CREQ#/INPACK# 1 T6504 TPC26T
- AUDIO/SPKR_IN#/BVD2 1 T6505 TPC26T
- CSTOP#/A20 1 T6506 TPC26T
- CDEVSEL#/A21 1 T6507 TPC26T
- CTRDY#/A22 1 T6508 TPC26T
- CIRDY#/A15 1 T6509 TPC26T
- CSTSCHG#/STSCHG#/BVD1 1 T6501 TPC26T
- CBLOCK#/A19 1 T6510 TPC26T
- CPERR#/A14 1 T6511 TPC26T
- CCLKRUN#/IOIS16# 1 T6512 TPC26T



<Variant Name>

Title : CARDBUS SOCKET
Engineer: Hawk / Kaxidy

ASUSTeK COMPUTER INC	Project Name	Rev
A3	T12C	1.1
Date: Friday, August 17, 2007	Sheet	65 of 94

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>

		Title :eSATA	
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>	
Size Custom	Project Name T12C	Rev 1.1	
Date: Monday, August 13, 2007		Sheet	66 of 94

PCI Device	IDSEL#	REQ/GNT#	Interrupts
LAN	AD15	2	D
1394 (R5C841)	AD17	1	B
CARD READER (R5C841)	AD17	1	C
CARDBUS (R5C841)	AD17	1	D
1394 (R5C832)	AD18	1	B
CARD READER (R5C832)	AD18	1	C

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor (MAX6657)	1001100x (98)
SDVO to DVI (SIL1362A)	0111000x (70)

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>



Title : NULL

ASUSTeK COMPUTER INC

Engineer: Hawk / Kaxidy

Size	Project Name	Rev
A	T12C	1.1

Date: Monday, August 13, 2007

Sheet 68 of 94

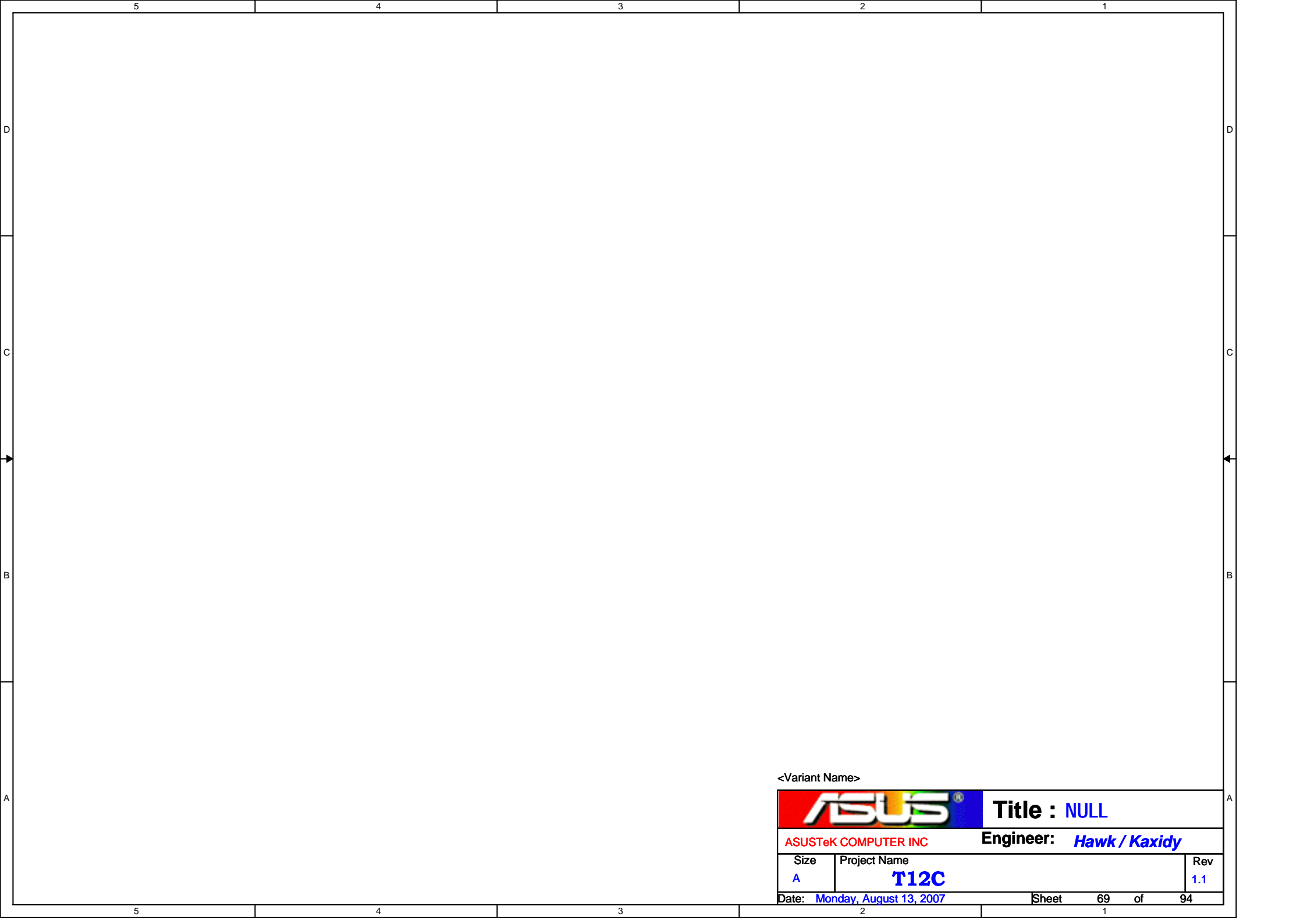
5

4


3

2

1



<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>
Size A	Project Name T12C	Rev 1.1
Date: Monday, August 13, 2007		Sheet 69 of 94

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>
Size	Project Name	Rev
A	T12C	1.1
Date: Monday, August 13, 2007		Sheet 70 of 94

5

4


3

2

1

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>	
Size	Project Name	Rev	
A	T12C	1.1	
Date: Monday, August 13, 2007		Sheet	71 of 94

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>
Size A	Project Name T12C	Rev 1.1
Date: Monday, August 13, 2007		Sheet 72 of 94

5

4

3

2

1

D

D

C

C


B

B

A

A

<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>
Size A	Project Name T12C	Rev 1.1
Date: Monday, August 13, 2007		Sheet 73 of 94

5

4

3

2

1

5

4

3

2

1

D

D

C

C


B

B

A

A

<Variant Name>

		Title : NULL
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>
Size	Project Name	Rev
A	T12C	1.1
Date: Monday, August 13, 2007		Sheet 74 of 94

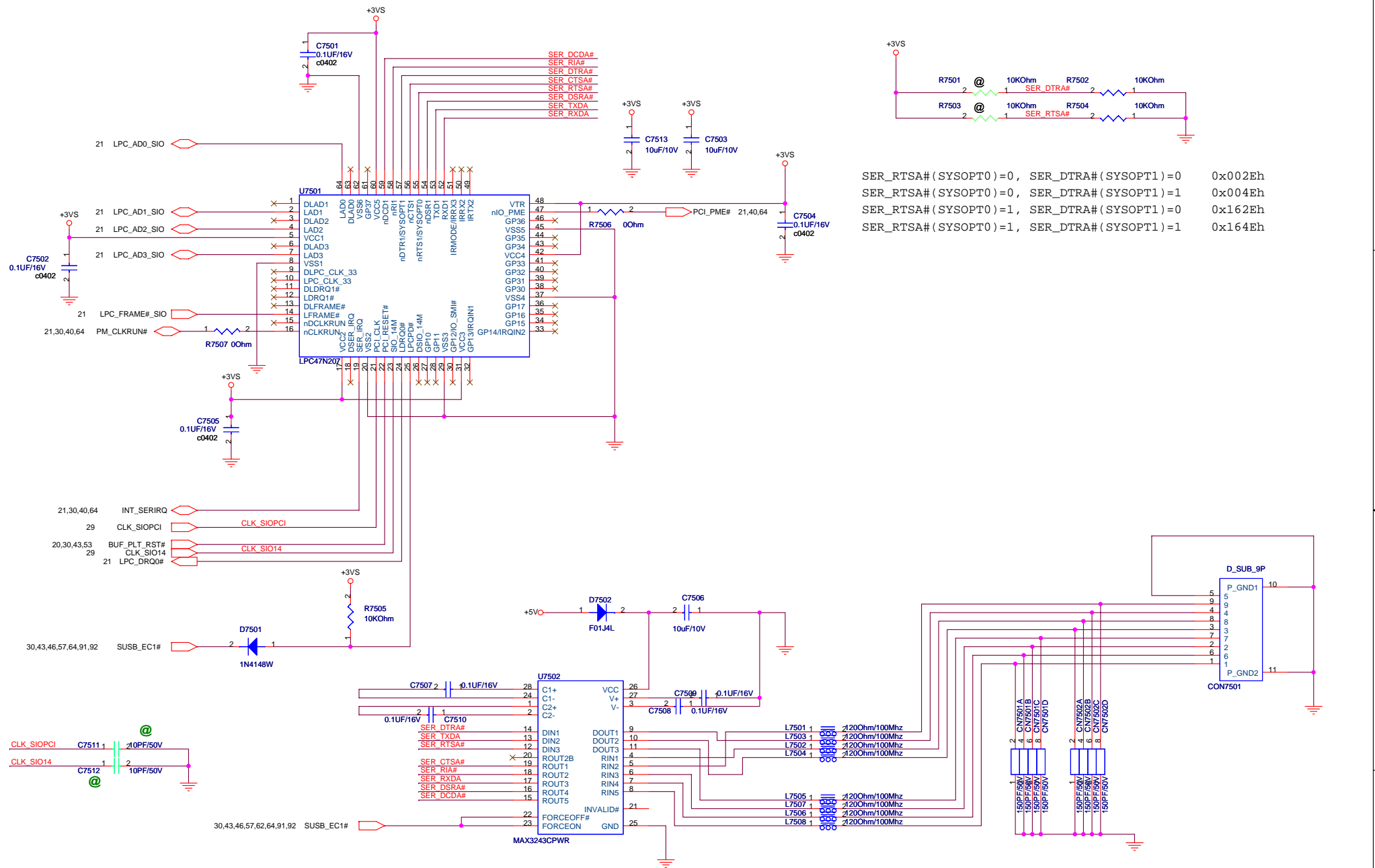
5

4

3

2

1



```

SER_RTSA#(SYSOPT0)=0, SER_DTRA#(SYSOPT1)=0 0x002Eh
SER_RTSA#(SYSOPT0)=0, SER_DTRA#(SYSOPT1)=1 0x004Eh
SER_RTSA#(SYSOPT0)=1, SER_DTRA#(SYSOPT1)=0 0x162Eh
SER_RTSA#(SYSOPT0)=1, SER_DTRA#(SYSOPT1)=1 0x164Eh

```

5

4

3

2

1

D

D

C

C

B

B

A

A

		Title : Null	
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>	
Size	Project Name		Rev
Custom	T12C		1.1
Date: Tuesday, February 26, 2008		Sheet	76 of 94

5

4

3

2

1

5

4

3

2

1

D

D

C

C


B

B

A

A

<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>	
Size	Project Name	Rev	
A	T12C	1.1	
Date: Monday, August 13, 2007		Sheet	77 of 94

5

4

3

2

1

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>



Title : NULL

ASUSTeK COMPUTER INC

Engineer: Hawk / Kaxidy

Size	Project Name	Rev
A	T12C	1.1

Date: Monday, August 13, 2007

Sheet 78 of 94

5

4

3

2

1

Change Note:

R1.1 :

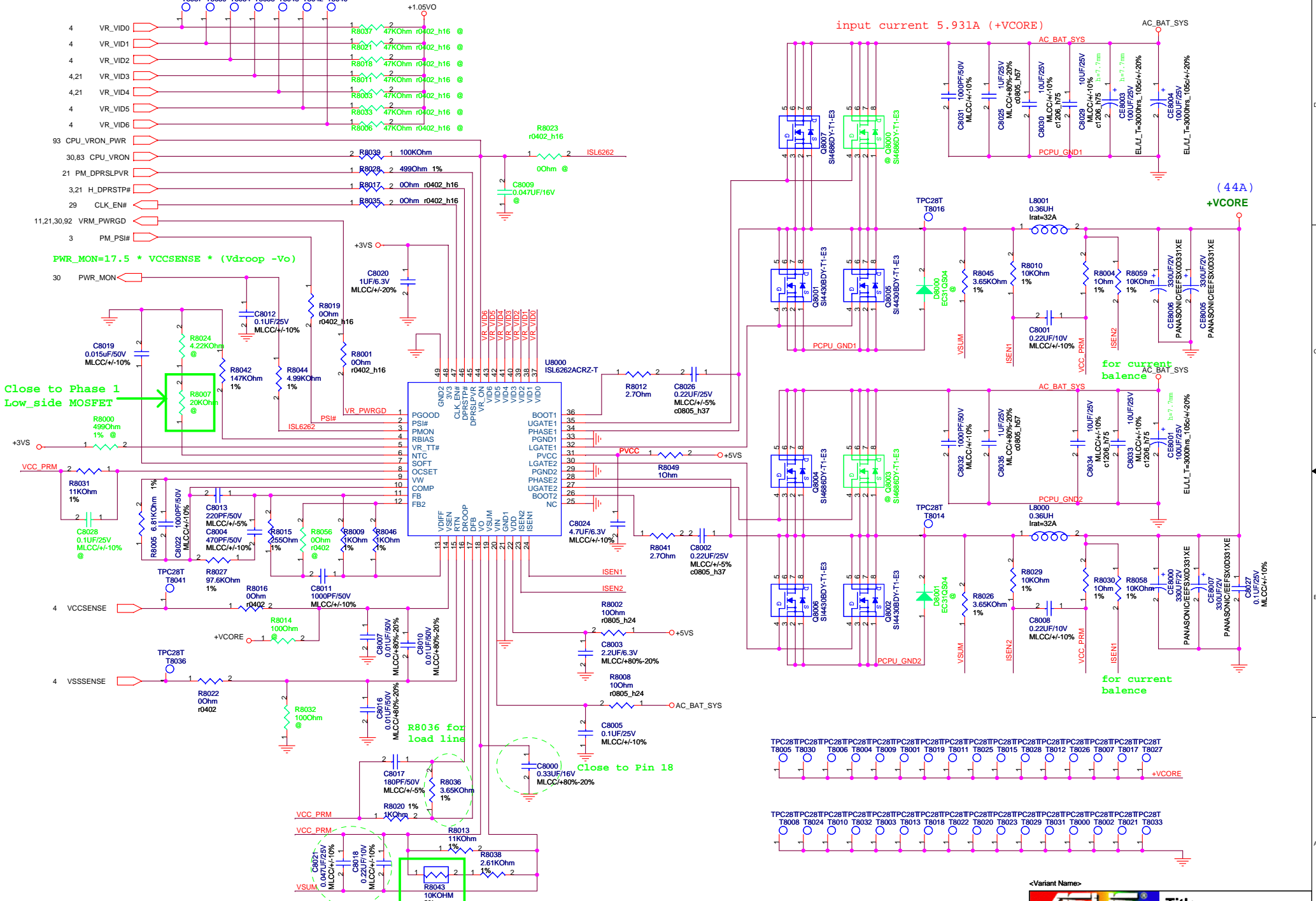
1. Reserve LVDS Up and Low channel of VGA side.
2. Change R3404 R3405 to 0ohm for LAN disconnect issue.
3. Change U3302 U3303 for new part.
4. Add D6004/D6003 for optional
5. Add R3114,R3115
6. Add Q3301,Q3302,R3341,R3342, C3329,C3330
7. Change IDSEL_CB to AD24/AD25. p64
8. add R6416 to CE_HWSPND#. P65
9. add Q3709 for depop issue. P37
9. change Q9203 TO Q3705B for ref error.

R2.0 :

1. Add C3202/C4210 /R4216 for EMI
2. Add R4607 and change Q4603 for LCD VCC
3. Add C2530,C2545,C2546,C2547,C2548,C2549,C2550,C2551,C2552,C2553,C2554,C2555

<Variant Name>

		Title : NULL	
ASUSTeK COMPUTER INC		Engineer: <i>Hawk / Kaxidy</i>	
Size	Project Name	Rev	
Custom	T12C	1.1	
Date: <i>Friday, August 17, 2007</i>		Sheet	79 of 94



$PWR_MON = 17.5 * VCCSENSE * (Vdroop - V_o)$

Close to Phase 1 Low_side MOSFET

Close to Pin 18

Close to Phase 1 Inductor

C8021 & C8018 for transient response

input current 5.931A (+VCORE)

AC_BAT_SYS

PCPU_GND1

PCPU_GND2

VSUM

VCC_PRM

ISEN1

ISEN2

ISEN3

ISEN4

ISEN5

ISEN6

ISEN7

ISEN8

ISEN9

ISEN10

ISEN11

ISEN12

ISEN13

ISEN14

ISEN15

ISEN16

ISEN17

ISEN18

ISEN19

ISEN20

ISEN21

ISEN22

ISEN23

ISEN24

ISEN25

ISEN26

ISEN27

ISEN28

ISEN29

ISEN30

ISEN31

ISEN32

ISEN33

ISEN34

ISEN35

ISEN36

ISEN37

ISEN38

ISEN39

ISEN40

ISEN41

ISEN42

ISEN43

ISEN44

ISEN45

ISEN46

ISEN47

ISEN48

ISEN49

ISEN50

ISEN51

ISEN52

ISEN53

ISEN54

ISEN55

ISEN56

ISEN57

ISEN58

ISEN59

ISEN60

ISEN61

ISEN62

ISEN63

ISEN64

ISEN65

ISEN66

ISEN67

ISEN68

ISEN69

ISEN70

ISEN71

ISEN72

ISEN73

ISEN74

ISEN75

ISEN76

ISEN77

ISEN78

ISEN79

ISEN80

ISEN81

ISEN82

ISEN83

ISEN84

ISEN85

ISEN86

ISEN87

ISEN88

ISEN89

ISEN90

ISEN91

ISEN92

ISEN93

ISEN94

ISEN95

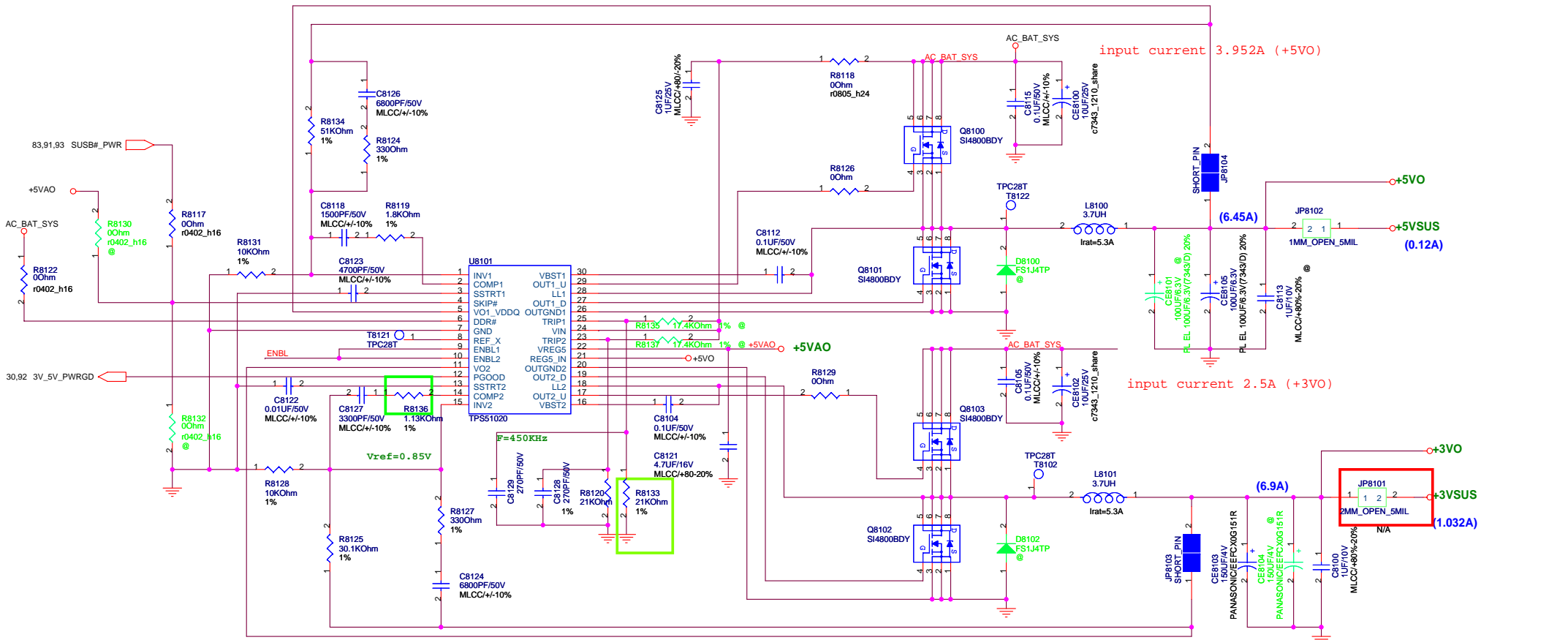
ISEN96

ISEN97

ISEN98

ISEN99

ISEN100

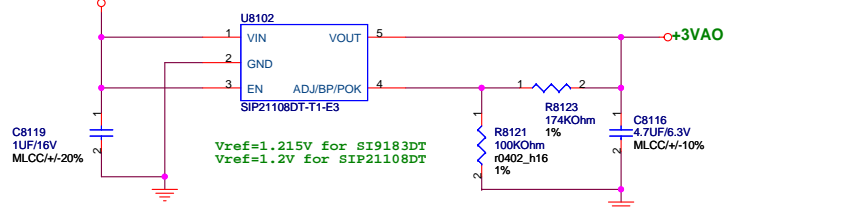


+3VAO

BOM need add second source:
SI9183 (06G007055114)

For SI9183DT:
 3.329V(TYP), 3.473V(Max), 3.178V(min)

For SIP21108DT:
 3.288V(TYP), 3.413V(Max), 3.163V(min)

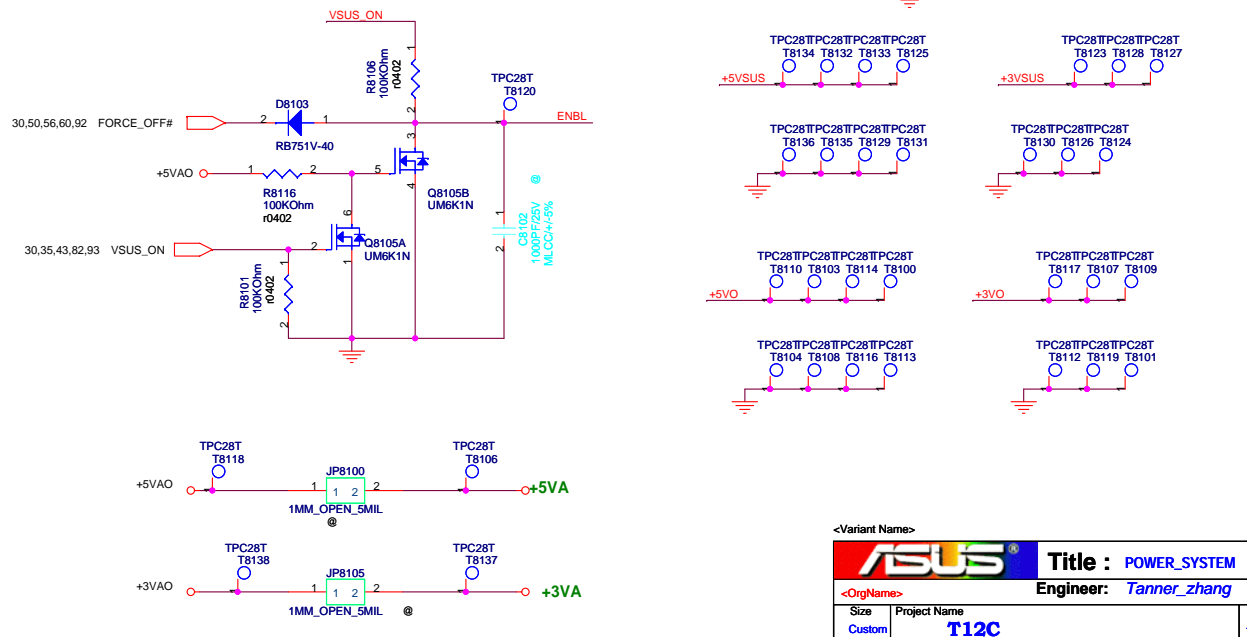
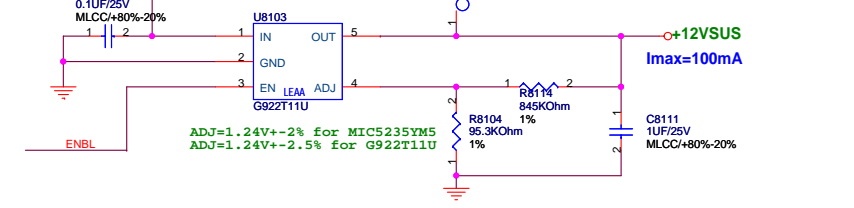


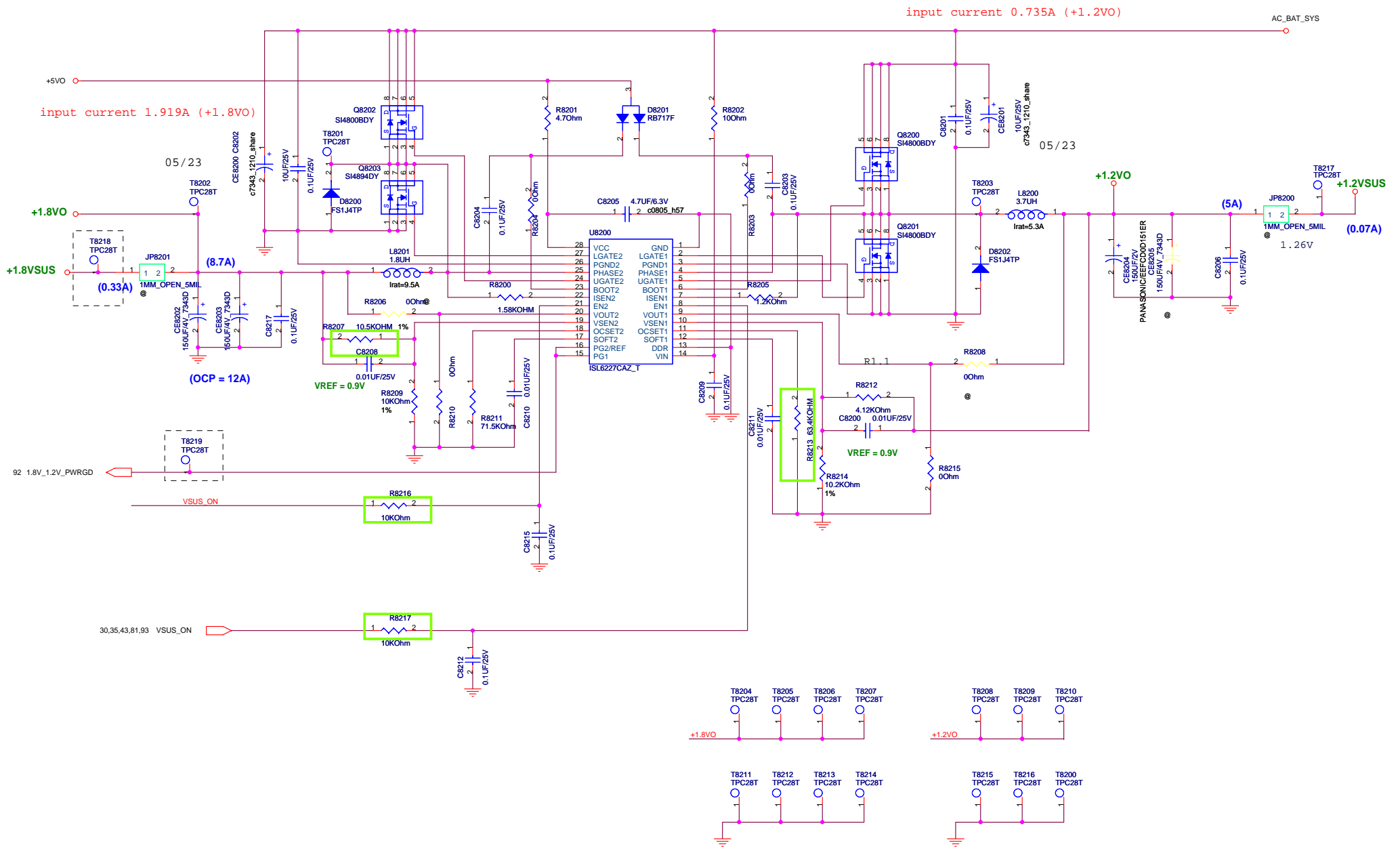
+12VSUS

BOM need add second source:
MIC5235YM5 (06G007137020)

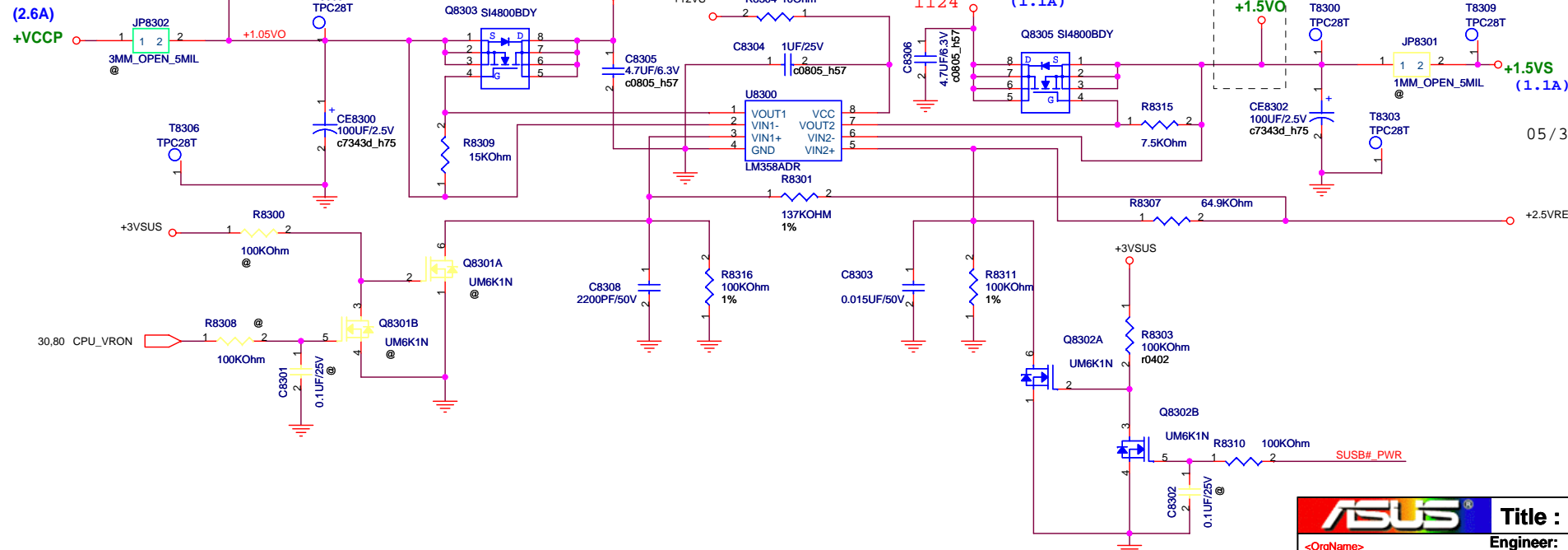
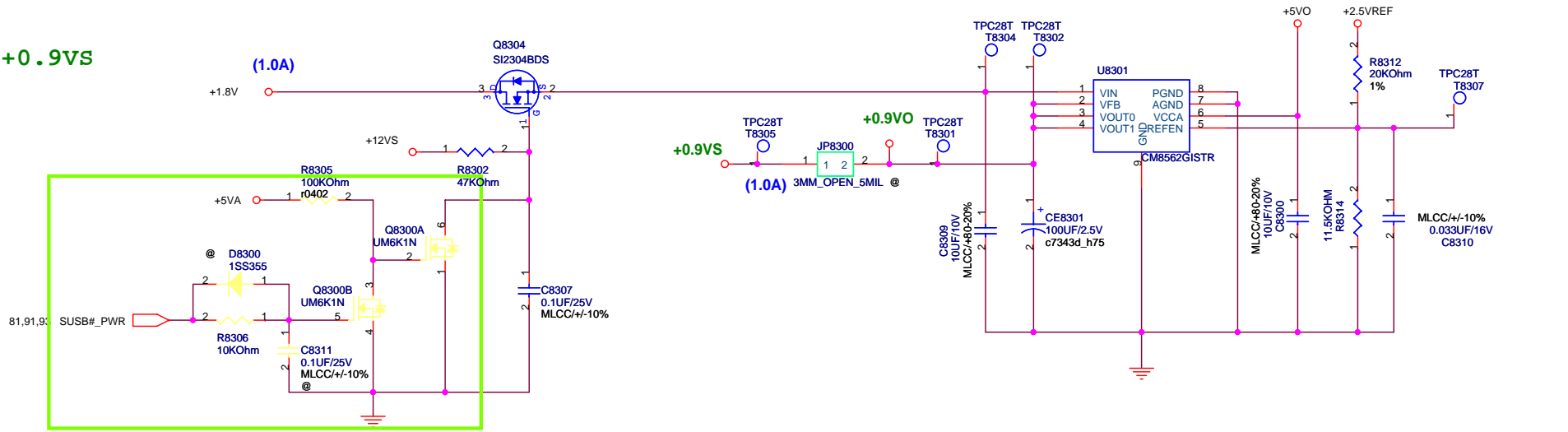
For MIC5235YM5:
 12.235V(TYP), 12.706V(Max), 11.777V(min)

For G922T11U:
 12.235V(TYP), 12.768V(Max), 11.717V(min)





+0.9VS



05/30

		Title : 1.05V & +0.9VS	
<OrgName>		Engineer: <i>Tanner_zhang</i>	
Size	Project Name		Rev
B	T12C		1.1
Date: Tuesday, March 11, 2008		Sheet	83 of 94

5

4

3

2

1

D

D

C

C

B

B

A

A

<Variant Name>



<OrgName> Engineer: *Tanner_Zhang*

Size	Project Name	Rev
Custom	T12C	1.0

5

4

3

2

1

b

b

c

c


b

b

a

a

<Variant Name>



Title : POWER_VGA_CORE & RAM

<OrgName> **Engineer:** *Tanner_zhang*

Size	Project Name	Rev
C	T12C	1.0

Date: *Tuesday, March 11, 2008* Sheet **85** of **94**

5

4

3

2

1

5

4

3

2

1

D

D

C

C


B

B

A

A

<Variant Name>

		Title : N/A
<OrgName>		Engineer: Tanner_zhang
Size	Project Name	Rev
B	T12C	1.0
Date: Tuesday, March 11, 2008		Sheet 86 of 94

5

4

3

2

1

5

4

3

2

1

D

D

C

C


B

B

A

A

<Variant Name>

		Title : <i>N/A</i>	
<OrgName>		Engineer: <i>Tanner_zhang</i>	
Size	Project Name	Rev	
Custom	T12C	1.0	
Date: <i>Tuesday, March 11, 2008</i>		Sheet <i>87</i> of <i>94</i>	

5

4

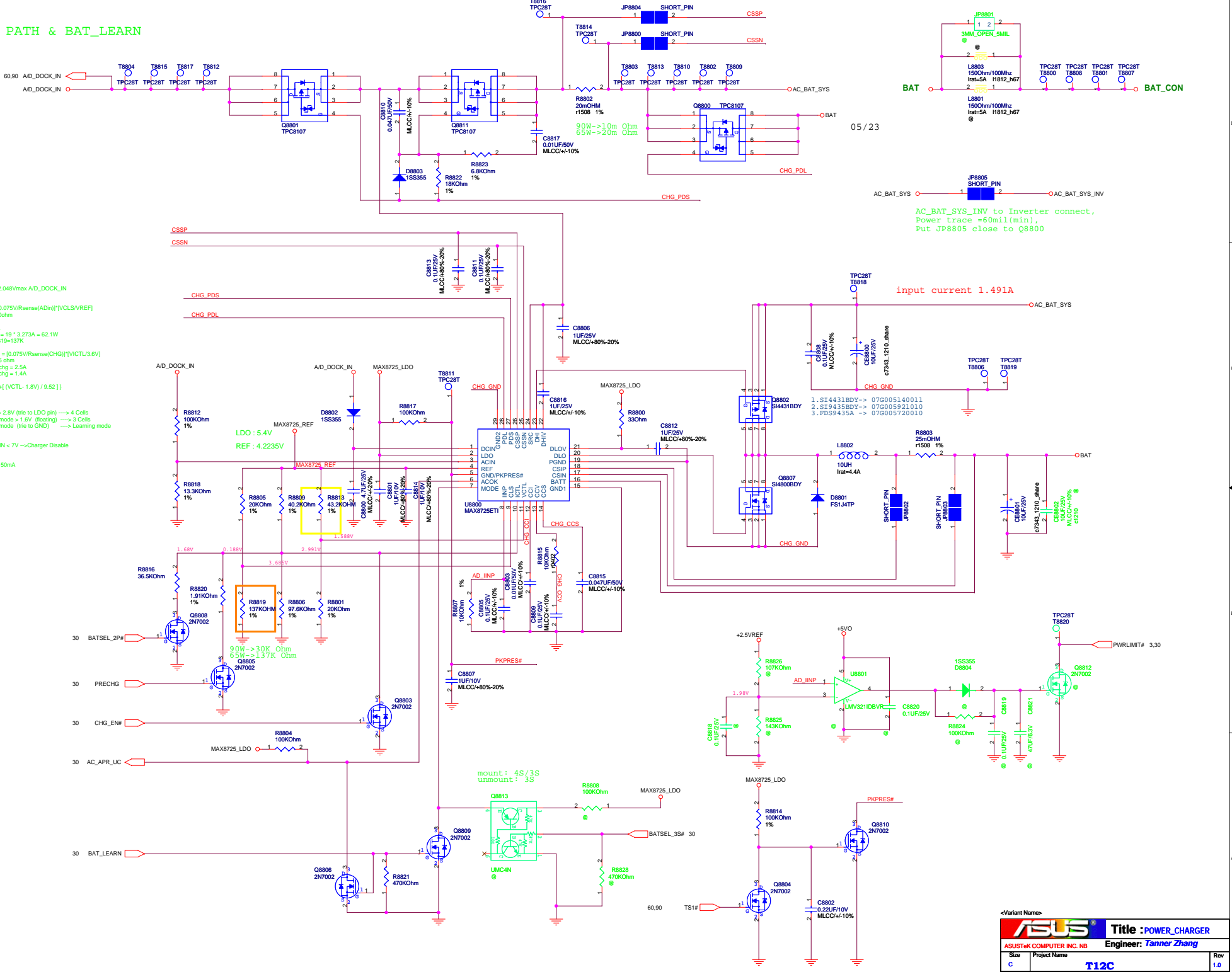
3

2

1

POWER PATH & BAT_LEARN

AC_IN Threshold 2.048Vmax A/D_DOCK_IN > 17.44V active
 Adapter lin(max) = [0.075V/Rsense(ADin)]*[VCLS/VREF]
 Rsense(ADin)=0.010ohm
 VCLS=3.685V
 => lin(max)=3.273A
 => Constant Power = 19 * 3.273A = 62.1W
 => R8805=20K, R8819=137K
 Charge Current Ichg = [0.075V/Rsense(CHG)]*[VICTL/3.6V]
 Rsense(CHG)=0.025ohm
 VICTL= 3V => Ichg = 2.5A
 Vbatt = 1.68V => Ichg = 1.4A
 Vbatt = Cell * (Vref - (VICTL - 1.8V) / 9.52)
 VCTL = 1.588V
 => Vbatt = 4.2V
 Mode pin : Vmode > 2.8V (tie to LDO pin) ----> 4 Cells
 2.0 > Vmode = 1.5V (floating) ----> 3 Cells
 0.8 > Vmode (tie to GND) ----> Learning mode
 VICTL < 0.8V or DCIN < 7V -> Charger Disable
 Precharge current=150mA



AC_BAT_SYS_INV to Inverter connect,
 Power Trace =60mil(min),
 Put JP8805 close to Q8800

input current 1.491A

5

4

3

2

1

D

D

C

C


B

B

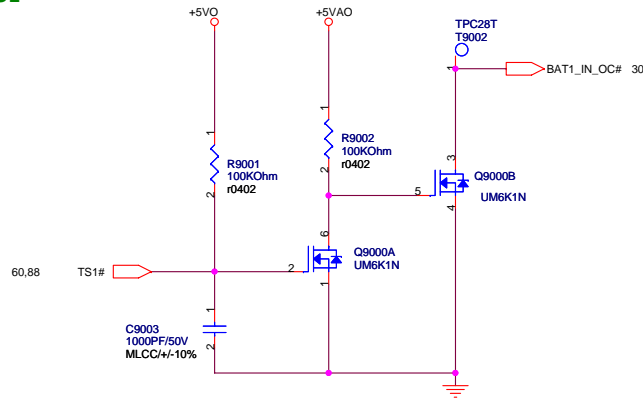
A

A

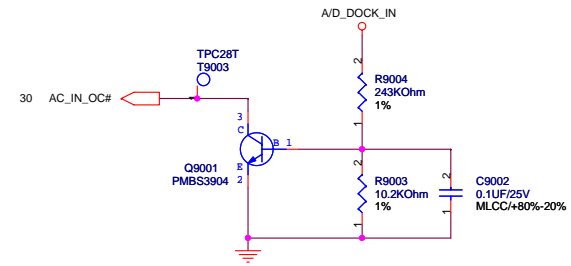
<Variant Name>

		Title : <i>N/A</i>	
<OrgName>		Engineer: <i>Tanner</i>	
Size	Project Name	Rev	
Custom	T12C	1.0	
Date: <i>Tuesday, March 11, 2008</i>		Sheet	89 of 94

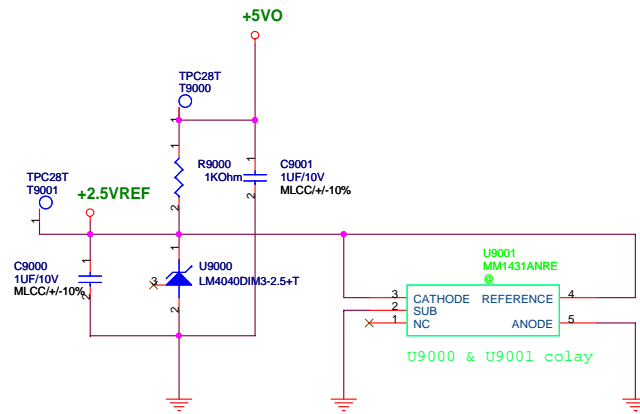
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF



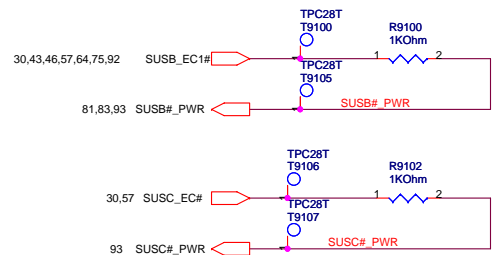
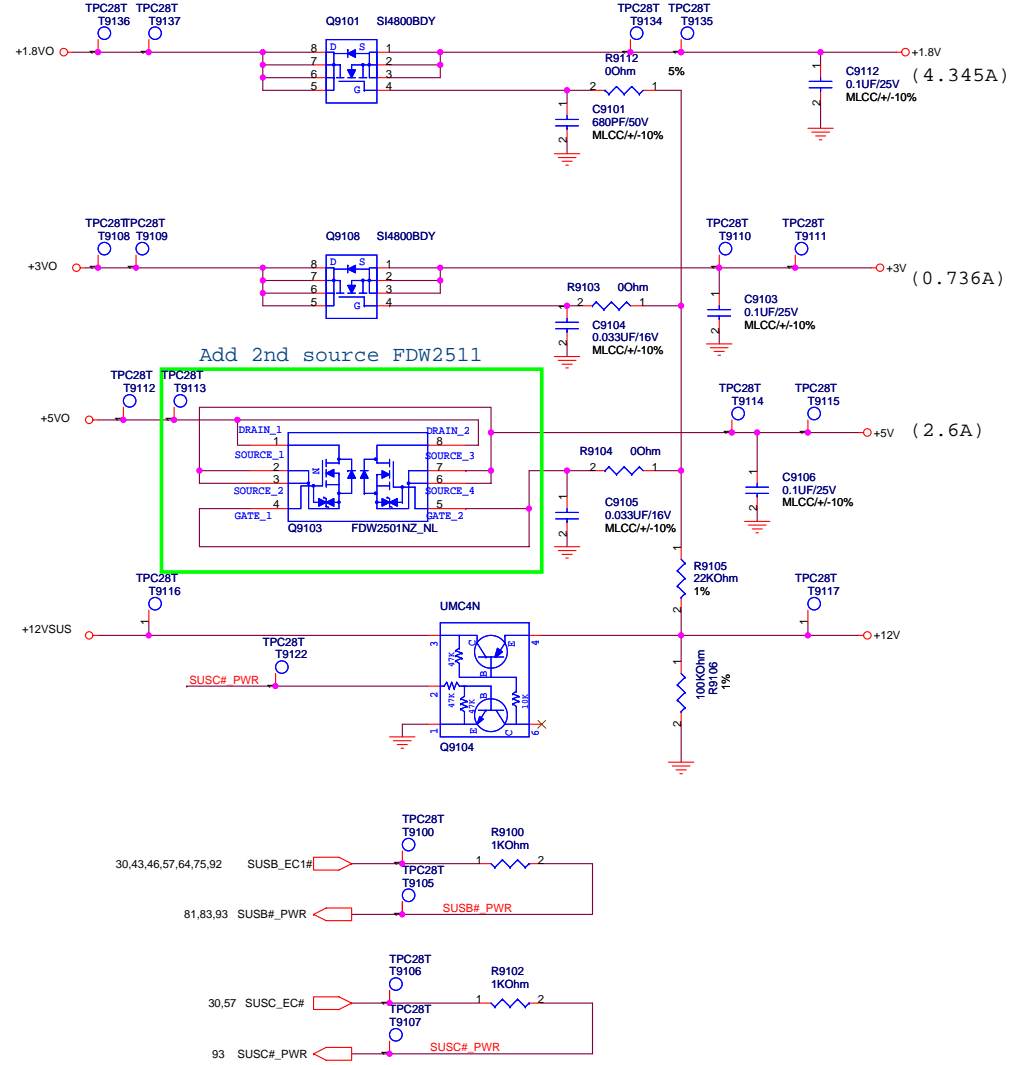
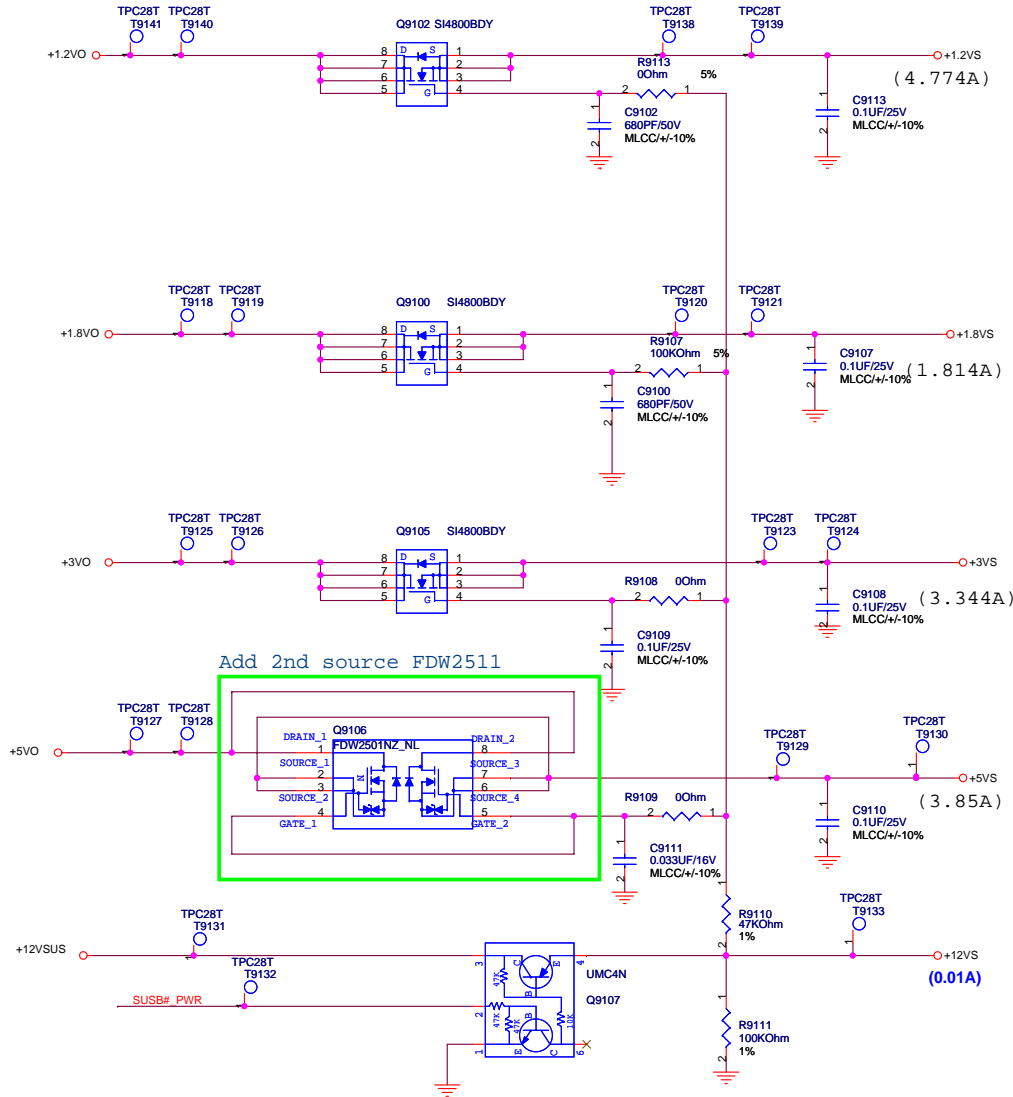
U9000 Main source change to 06G006002414(tolerance:1%).
 Add second source 06G006002610 (tolerance:1%),
 06G006002412 (tolerance:0.2%) and
 06G006002020 (tolerance:0.2%)

<Variant Name>

		Title :POWER_DETECT	
<OrgName>		Engineer: tanner	
Size	Project Name	Rev	
Custom	T12C	1.0	
Date: Tuesday, March 11, 2008	Sheet	90	of 94

SUSC#_STAGE POWER

SUSB#_STAGE POWER



POWER GOOD DETECTOR

