D/M Note Block Diagram -- Intel Huron River ULV

PCB STACK UP 8L

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT

POWER

- DC/DC — 3V_PCU, 5V_PCU, +15V — Page 31
- REGULATOR (DDR3) — 1.5V_SUS, 0.75V_DDR_VTT — Page 32
- REGULATOR — 1.05V&1.8V — Page 33
- REGULATOR — VCCSA — Page 34
- CPU Core — Page 35
- Charger — Page 36
- RUN POWER SW/Discharge — 5V_SUS, 3V_S5, 5V_S5 +3V, +5V — Page 37

DDR3 SO-DIMM 1 (STD) Page 13

DDR3 SO-DIMM 2 (RVS) Page 14

Intel Huron River Sandy Bridge
31mmX24mm, BGA
2 Core 18Watt
Page 3, 4, 5, 6

Environment temperature Thermal Sensor Page 26

Charger temperature Thermal Sensor Page 26

DDR Thermal Sensor Page 13

FDI

X4 DMI

Cougar Point
HM65
25mmX25mm, BGA
PCH 3.9Watt
Page 7, 8, 9, 10, 11, 12

USB — Card Reader Realtek RTS5209 Page 21 — 4 in 1 Socket SD/SDHC/SDXC/MMC Page 21

PCI-e/USB — Mini PCIe Slot Page 22 — WLAN Module Page 22

PCI-e/USB — Mini PCIe Slot Page 23 — WWAN Module Page 23 — SIM Card Page 23

PCI-e — 10/100/1G Ethernet AR8151-BL1A-R++ Page 17 — RJ-45 Page 17

HD Audio — HDA CODEC CX20671-21Z Page 18 — HP/Mic Audio Jack Page 18

HDA CODEC — Internal MIC Page 18

HDA CODEC — Internal SPK Page 18

SPI Flash (4MB) Page 8

SATA — 2.5" HDD /SSD Module (Option) Page 19

LVDS — 11.6" HD (1366x768) LCD Page 15

RGB — CRT Page 16

HDMI — HDMI Page 16

32.768KHz

LPC BUS

SPI Flash (512K) Page 28

IT8518 Page 28

TPM (for M-note) Page 25

USB — Camera Conn Page 15 — Camera Module Page 15

USB — Bluetooth Page 25

USB — USB PORT X 3 Page 20

USB — Fingerprint (for M-note) Page 24

Accelerometer (APS) Page 25

Int. KB Page 24

T/P Page 24

Battery Page 36

Charger Page 36

Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	System Block Diagram	1A

Date: Monday, January 31, 2011 Sheet 1 of 43

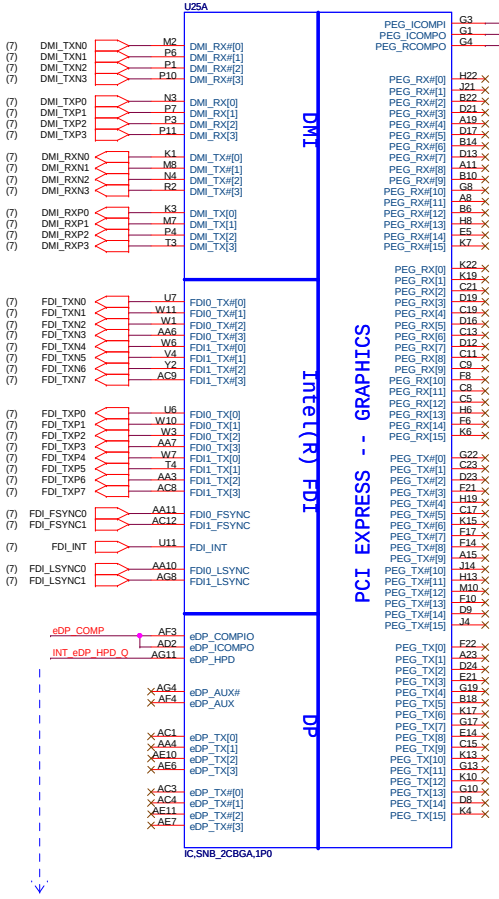
Table of Contents

Power States

POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	15,31,32,33,34,35,36,37	MAIN POWER		S0~S5
+3V_RTC	+3.0V~+3.3V	7,8,11,28	RTC		S0~S5
3VPCU	+3.3V	8,15,16,17,20,27,28,31,33,36,37	IT8518/19 POWER	3V5V_EN	S0~S5
5VPCU	+5V	15,29,31,32,33,34,36,37	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	15,25,31,32,37	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	17,37	LAN POWER	LAN_ON	
5V_S5	+5V	11,20,37	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	3,7,8,9,10,11,22,25,27,28,37	Sys Management,PCH Resume Well, USB,WLAN,WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	15,27,35,37	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	32,37	SLP_S4# CTRLD POWER	SUSON	S0~S3
+1.5VSUS	+1.5V	3,11,13,14,32,37	DDR3 SODIMM POWER	SUSON	S0~S3
+0.75V_DDR_VTT	+0.75V	13,14,32,37	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	7,8,11,15,16,18,19,24,26,28,29,37	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	3,7,8,9,10,11,13,14,15,16,17,18,19,21,22,23 24, 25,26,27,28,29	SLP_S3# CTRLD POWER	MAINON	S0
+VCC_GFX		5,35,37	VGA CORE POWER	MAINON	S0
+VCCSA	+0.8V~+0.9V	5,34,37	Sandy Bridge Power	MAINON	S0
+1.8V	+1.8V	5,8,11,33,37	LVDS,NVM POWER	MAINON	S0
+1.05V	+1.05V	3,5,7,8,9,11,33,37	Sandy Bridge VTT POWER/PCH CORE POWER	MAINON	S0
+VCC_CORE		5,6,35,37	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	15	LCD Power	ENVDD	S0
+3V_HDD	+3V	19	ODD Power	ODD_5V_ON	S0
+5V_HDD	+5V	19	HDD Power	MAINON#	S0
BAT-V	+10V~+17V	36	MAIN BATTERY	CHG_PBATT	S0~S5
+1.5V_CPU	+1.5V	3,5,32,37	DDR3 1.5V Rails	PS_S3CNTRL	S0

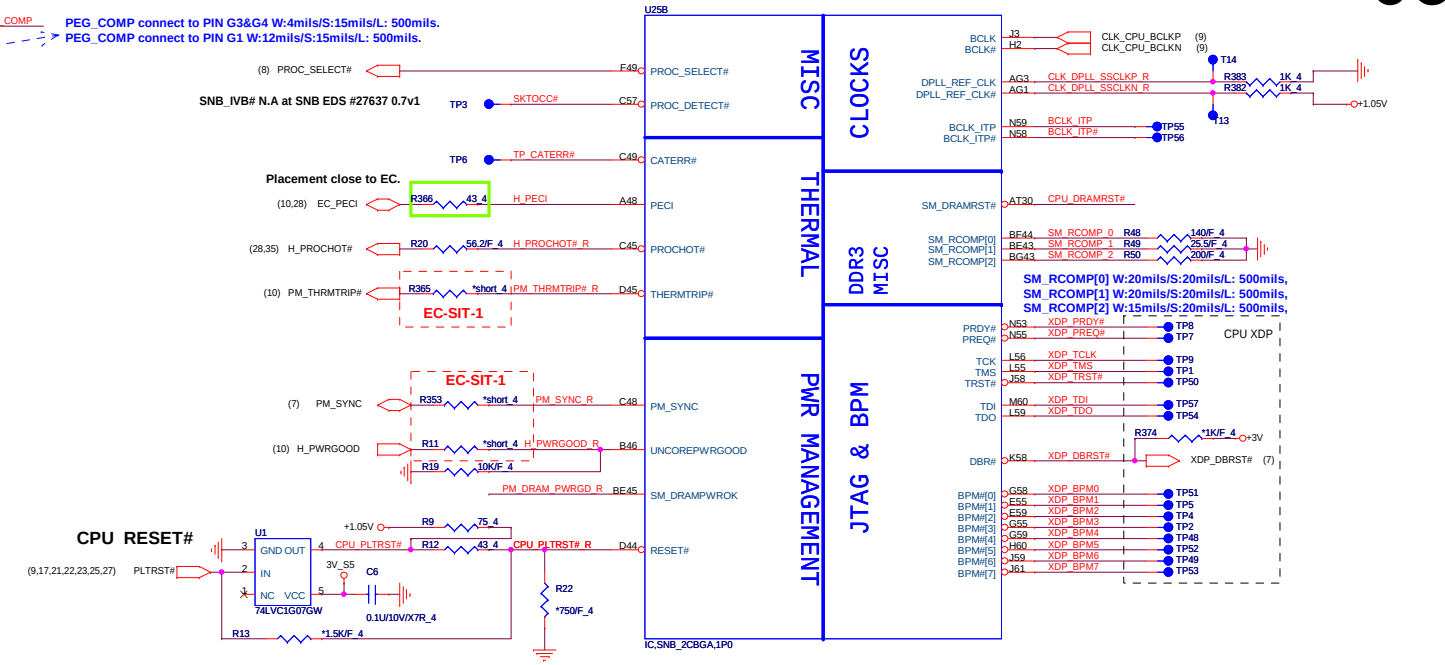
Sandy Bridge Processor (DMI,PEG,FDI)

Sandy Bridge Processor (CLK,MISC,JTAG)



PEG_COMP connect to PIN G3&G4 W:4mils/S:15mils/L: 500mils.
PEG_COMP connect to PIN G1 W:12mils/S:15mils/L: 500mils.

eDP_COMP connect to PIN AF3 W:4mils/S:15mils/L: 500mils.
eDP_COMP connect to PIN AD2 W:12mils/S:15mils/L: 500mils.



SM_RCOMP[0] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[1] W:20mils/S:20mils/L: 500mils,
SM_RCOMP[2] W:15mils/S:20mils/L: 500mils,

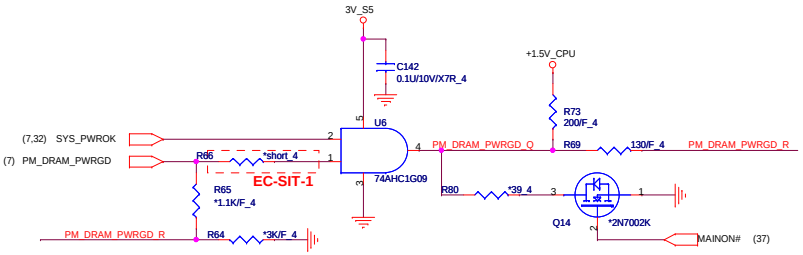
SNB_IVB# N.A at SNB EDS #27637 0.7v1

Placement close to EC.

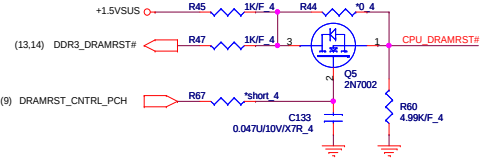
EC-SIT-1

CPU RESET#

SM_DRAMPWROK Processor Input.

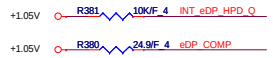


DDR3 DRAM RESET

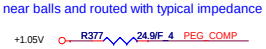


+1.5VSUS (11,13,14,29,32,37)
+1.05V (5,7,8,9,11,29,33,37)
+1.5V_CPU (5,29,32,37)
3V_S5 (7,8,9,10,11,22,25,28,37)
+3V (7,8,9,10,11,13,14,15,16,18,19,21,22,23,24,25,26,27,28,29,31,32,33,34,35,37)

DP & PEG Compensation

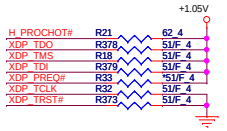


eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



PEG_ICOMPI and RCOMPO signals should be routed within 500 mils typical impedance = 43 mohms PEG_ICOMPO signals should be routed within 500 mils typical impedance = 14.5 mohms

Processor pull-up (CPU)



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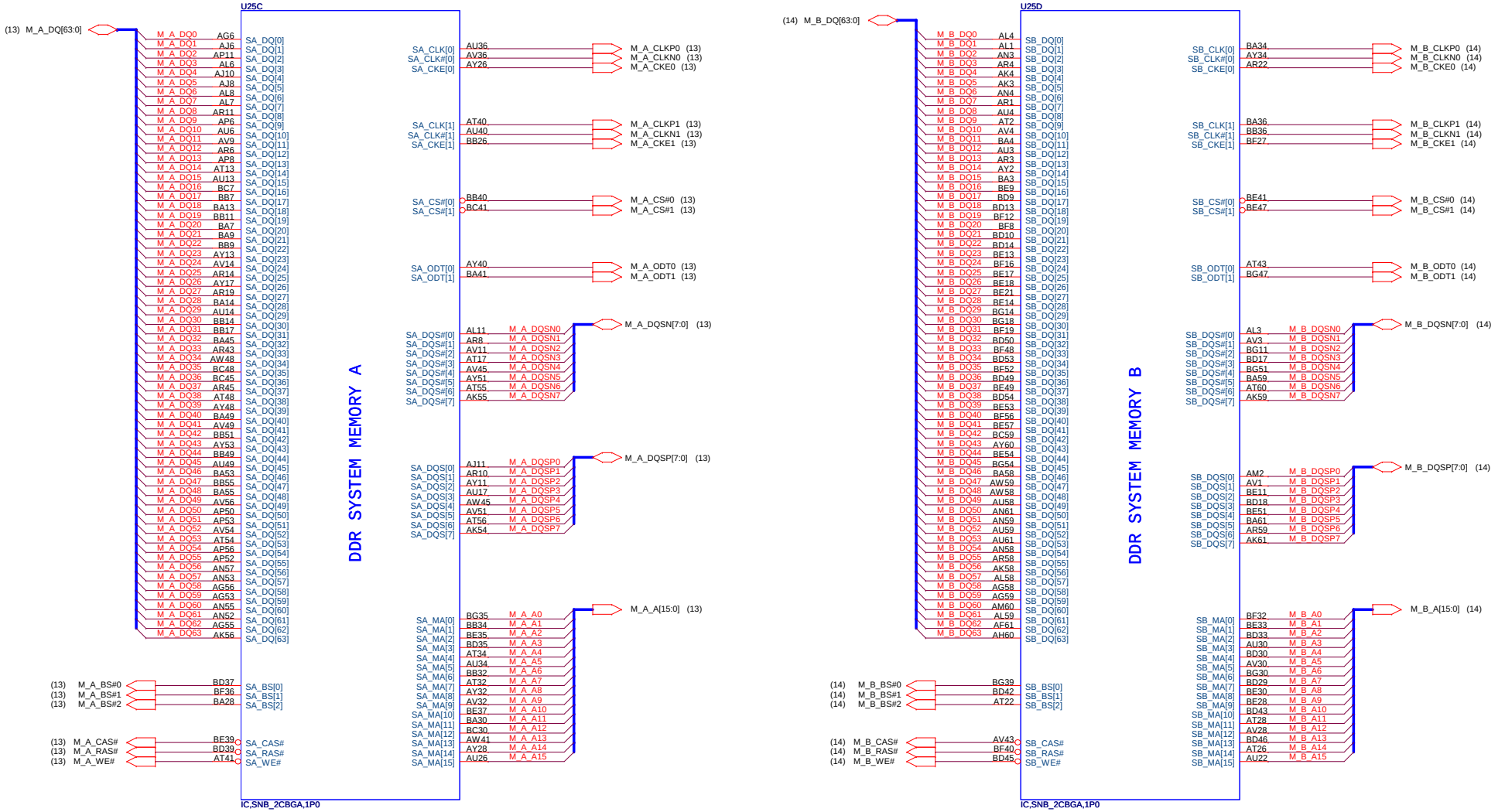
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	Custom SNB 1/4 (PCIE&DMI&FDI)	1A
Date: Monday, January 31, 2011	Sheet 3 of 43	

Sandy Bridge Processor (DDR3)



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PROJECT D/M NOTE INTEL HURON RIVER			
Size	Document Number		Rev
	Custom	SNB 2/4 (DDR3 I/F)	1A
Date: Monday, January 31, 2011		Sheet 4 of 43	

Sandy Bridge Processor (POWER)

330uF locate power side

8.5A

CPU Core Power

SNB:21.5A

+VCC_CORE

U25F

POWER

CORE SUPPLY

PEG AND DDR

3.3V_SUS?(PDDG p127)

QUIET RAILS

SVID

SENSE LINES

IC,SNB_2CBGA,1P0

Sandy Bridge Processor (GRAPHIC POWER)

05

12A

+VCC_GFX

U25G

POWER

GRAPHICS

DDR3 - 1.5V RAILS

1.8V RAIL

SA RAIL

QUIET RAILS

SENSE LINES

1.2A

SNB:6A

+VCCSA

+VDDR_REF_CPU

CAD Note: +VDDR_REF_CPU should have 10 mil trace width

SM_VREF

5A

EC-DV-02

SNB_IVB# N.A at SNB EDS #27637 0.7v1

If +1.5V_CPU will be implemented, have to change the two divided resistor as 100-ohm 1%

IC,SNB_2CBGA,1P0

SVID CLK

Layout note: need routing together and ALERT need between CLK and DATA.

Place PU resistor close to VR

EC-SIT-1

SVID DATA

Place PU resistor close to CPU

Place PU resistor close to VR

EC-SIT-1

SVID ALERT

Place PU resistor close to CPU

EC-SIT-1

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PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	Custom SNB 3/4 (POWER)	1A
Date: Monday, January 31, 2011	Sheet 5 of 43	

Sandy Bridge Processor (GND)

Sandy Bridge Processor (RESERVED, CFG)

06

U25H

VSS

IC,SNB_2CBGA,1P0

U25I

VSS

NCTF

IC,SNB_2CBGA,1P0

U25E

RESERVED

IC,SNB_2CBGA,1P0

+VCC_CORE

R26 *51/F_4

R31 *51/F_4

R25 *51/F_4

R30 *51/F_4

VCC_VAL_SENSE

VSS_VAL_SENSE

VAXG_VAL_SENSE

VSSAXG_VAL_SENSE

VCC_DIE_SENSE

CPU_RSVD6

CPU_RSVD7

CFG5 R357 *1K/F_4

CFG6 R358 *1K/F_4

CFG[6:5] (PCIE Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled

10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled

01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)

00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

CFG2 R370 *1K/F_4

CFG3 R369 *1K/F_4

CFG4 R356 *1K/F_4

CFG7 R27 *1K/F_4

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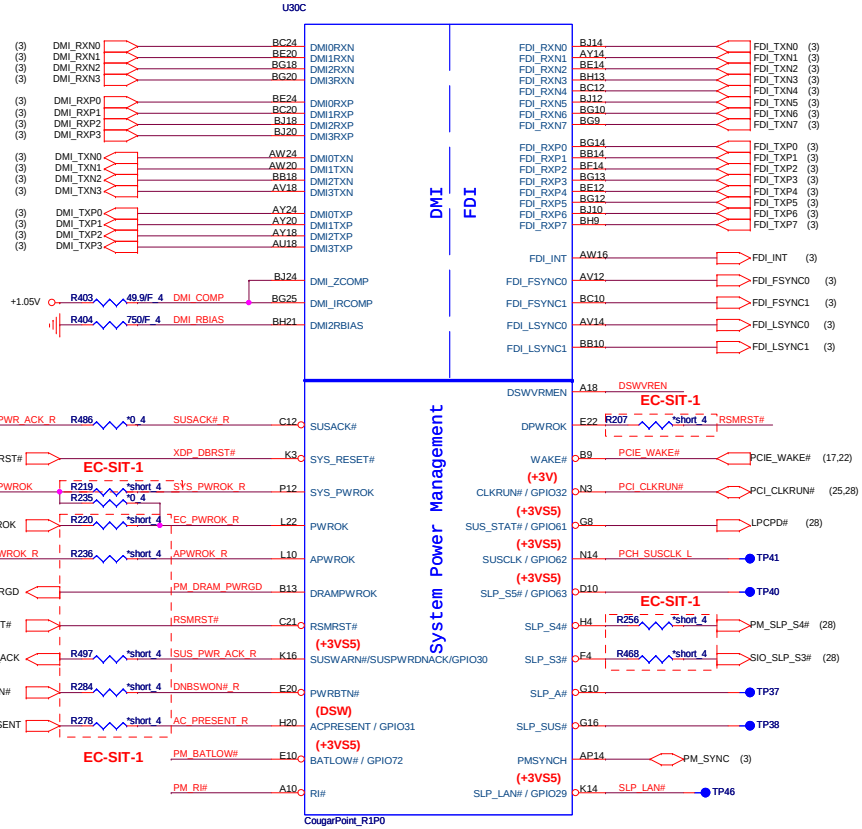
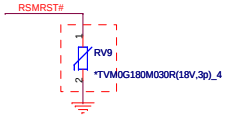
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	Custom SNB 4/4 (GND)	1A
Date: Monday, January 31, 2011	Sheet 6 of 43	

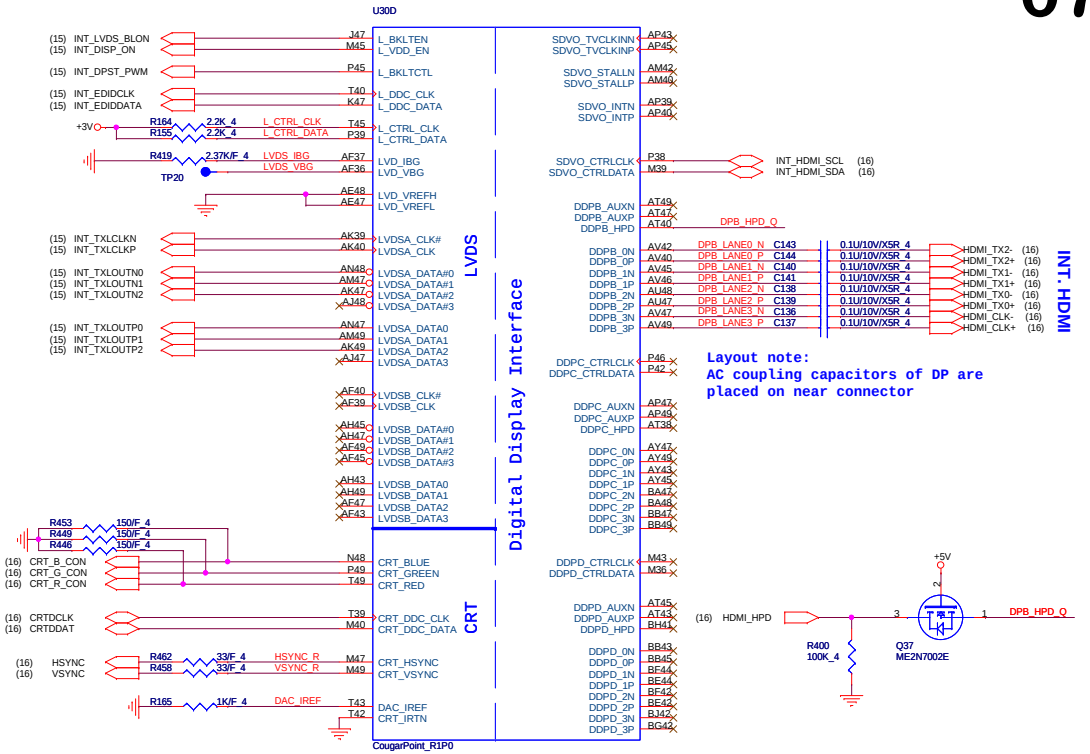
Cougar Point (DMI,FDI,PM)





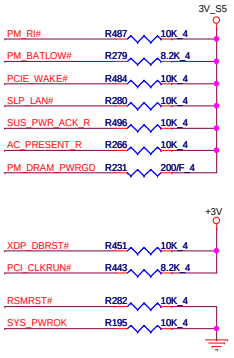
EC-DV-09

Cougar Point (LVDS,DDI)

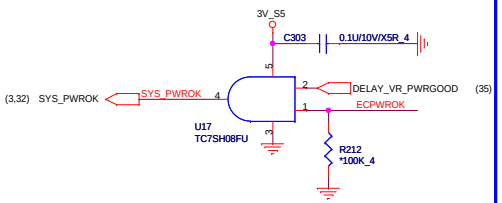


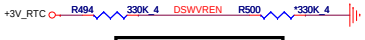
07

PCH Pull-high/low(CLG)



System PWR_OK(CLG)





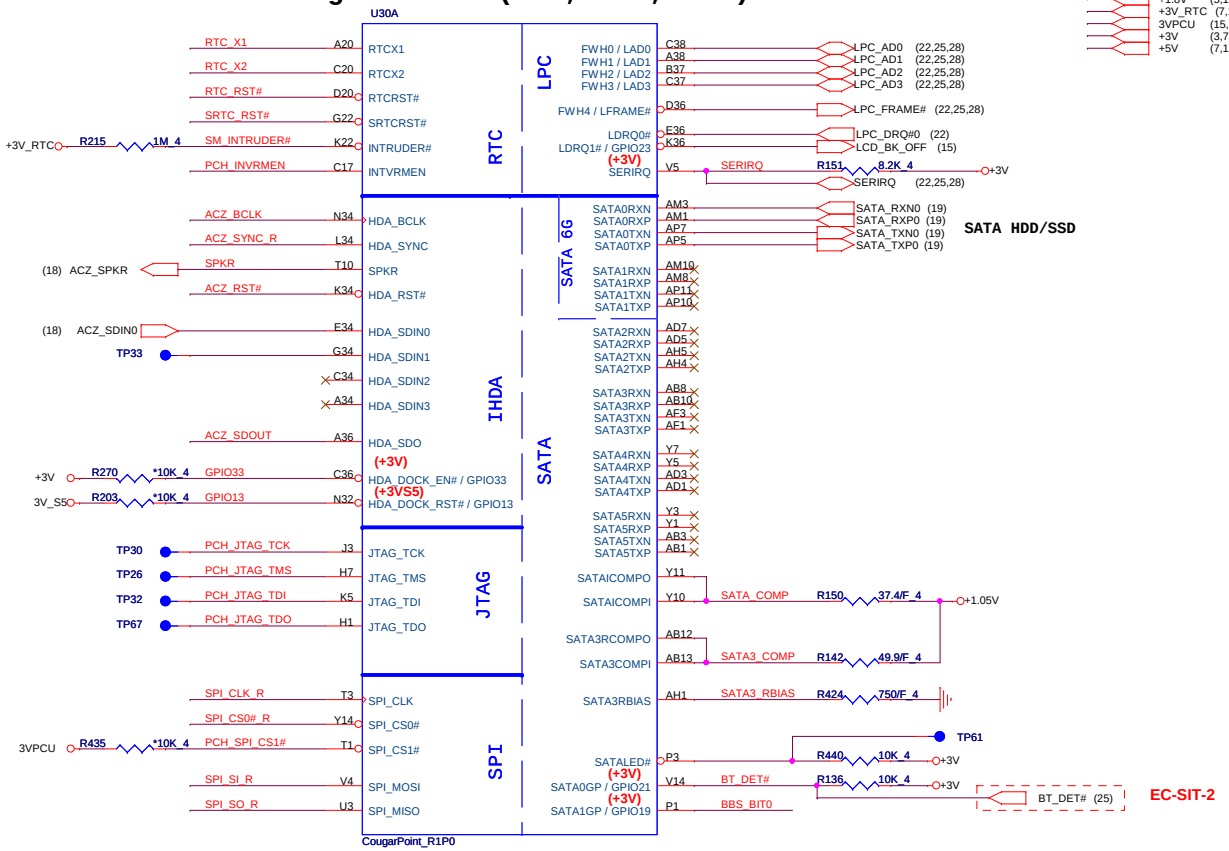
On Die DSW VR Enable
High = Enable (Default) Low = Disable

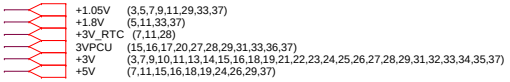
+1.05V (3,5,8,9,11,29,33,37)
+3V_RTC (8,11,28)
3V_S5 (3,8,9,10,11,22,25,28,37)
+3V (3,8,9,10,11,13,14,15,16,18,19,21,22,23,24,25,26,27,28,29,31,32,33,34,35,37)
+5V (11,15,16,18,19,24,26,29,37)

Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER

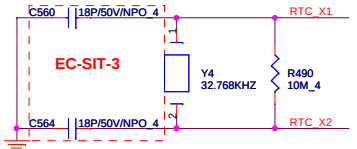
Size	Document Number	Rev
	PCH 1/6 (DMI/FDI/VIDEO)	1A
Date: Monday, January 31, 2011	Sheet 7 of 43	

Cougar Point (HDA,JTAG,SATA)



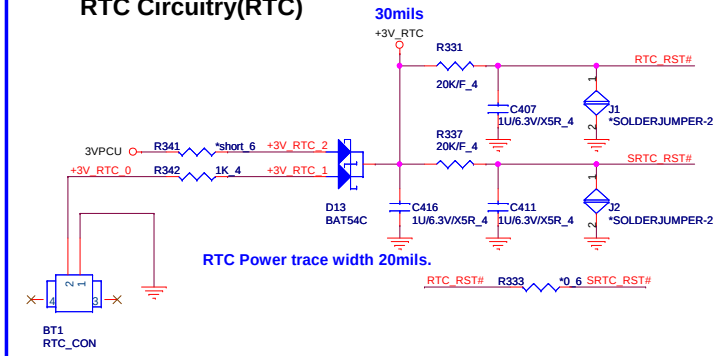


RTC Clock 32.768KHz

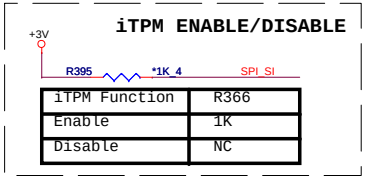


08

RTC Circuitry(RTC)

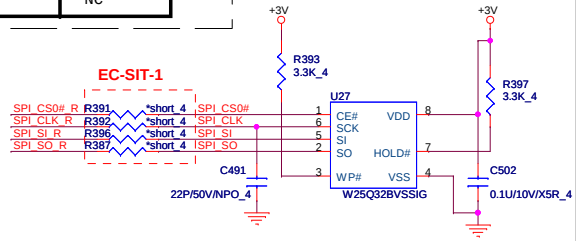


iTPM ENABLE/DISABLE

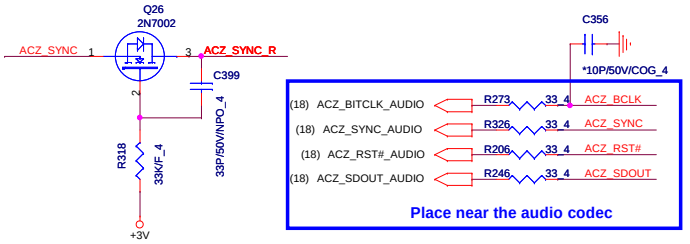


iTPM Function	R366
Enable	1K
Disable	NC

For PCH
32Mbit (4M Byte), SPI



HDA Bus(CLG)



if default boot destination is SPI, no external pull-up/-down resistors on the board are necessary

PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR Different from Capella	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R172 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R482 *1K_4, R477 10K_4, +3V, PCI_GNT3# (9) — Bios request, for can't boot Capella 4/23.
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R488 330K_4 +3V_RTC
HDA_SDO	Flash Descriptor Security Only for Interposer	PWROK	0 = effective(Default: weak pull down) 1 = Override	ACZ_SDOUT R224 *1K_4 3V_S5
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	GNT1# / GNT0# / Boot Location: 1 1 SPI; 1 0 LPC	[Need external pull-down for LPC BIOS]
GPIO19 Different from Capella	Boot BIOS Selection 0 [bit-0]	PWROK		R442 *1K_4 BBS_BIT0, R481 *1K_4 BBS_BIT1 (9)
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
DF_TVS	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V, R416 2.2K_4, R418 1K_4, (3) PROC_SELECT#, DF_TVS (10) — N.A at CPT EDS 0.7
HDA_SYNC	**On-Die PLL VR Voltage Select**	**RSMRST**	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S5, R201 1K_4, ACZ_SYNC_R
GPIO15				(10) GPIO15, GPIO15 R466 1K_4 3V_S5
GPIO28 Different from Capella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	R192 *1K_4 PLL_ODVR_EN (10)
DSWVREN	0: disable 1: enable			

Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	PCH 2/6 (SATA/HDA/SPI)	1A
Date: Monday, January 31, 2011	Sheet 8 of 43	

Cougar Point-M (PCI,USB,NVRAM)

Cougar Point-M (PCI-E,SMBUS,CLK)

09

PCI/USBOC# Pull-up(CLG)

PLTRST#(CLG)

SMBus/Pull-up(CLG)

CLK_REQ/Strap Pin(CLG)

PCIE Clock

Layout note:
PCIE_CLKREQ_LAN# layout adjacent
to CLK_PEGA_REQ#

SMBus/Pull-up(CLG)

CLOCK TERMINATION for FCIM

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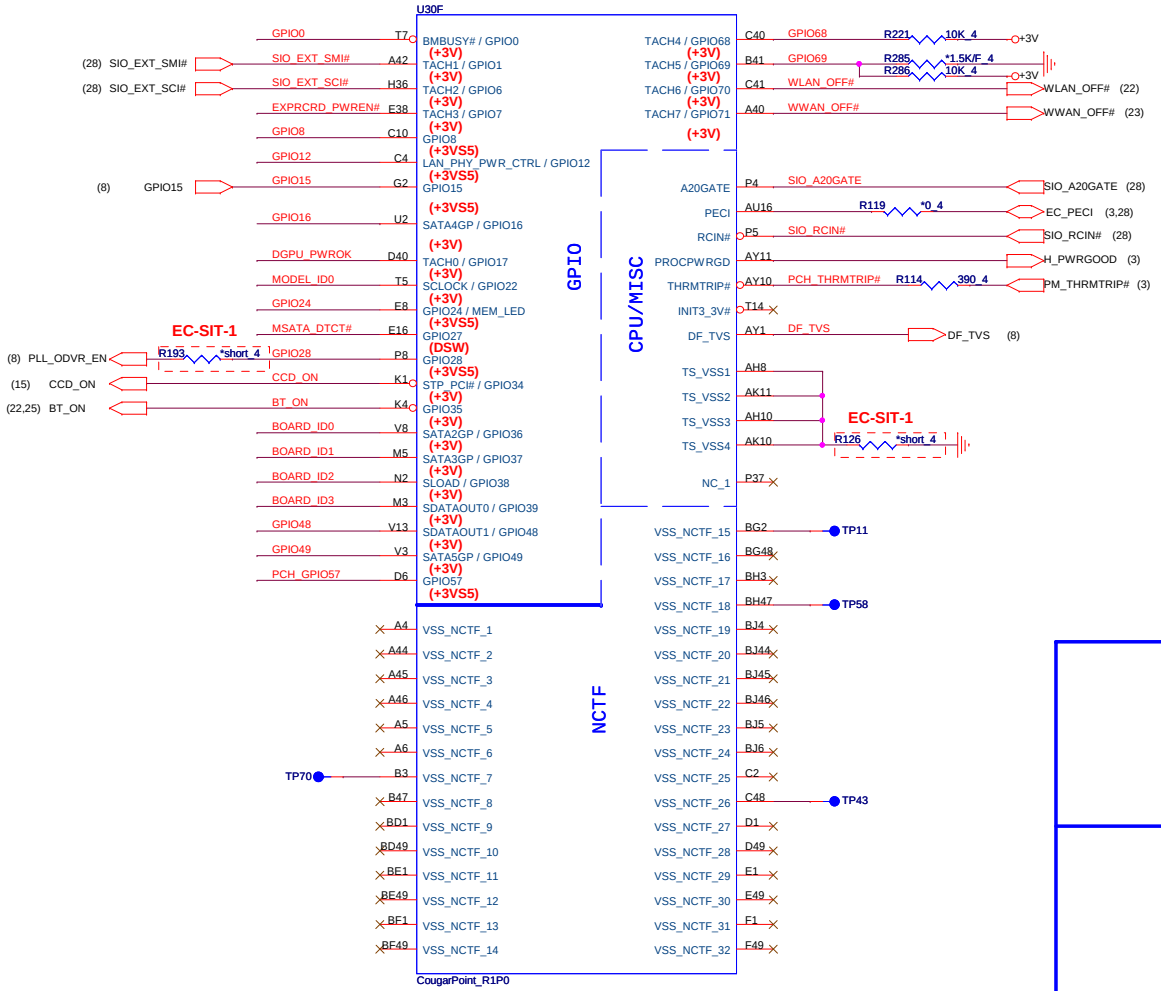
PROJECT D/M NOTE INTEL HURON RIVER

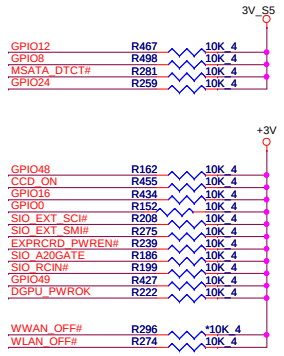
Size	Document Number	Rev
	PCH 3/6 (PCIE/USB/CLK)	1A
Date: Monday, January 31, 2011	Sheet 9 of 43	

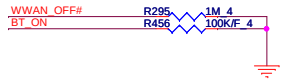
Cougar Point (GPIO,VSS_NCTF,RSVD)



3V_S5 (3,7,8,9,11,22,25,28,37)
+3V (3,7,8,9,11,13,14,15,16,18,19,21,22,23,24,25,26,27,28,29,31,32,33,34,35,37)

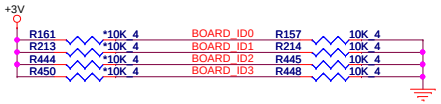
GPIO Pull-up/Pull-down(CLG)



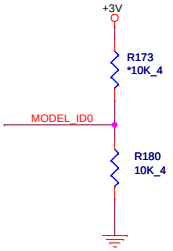


BOARD ID SETTING

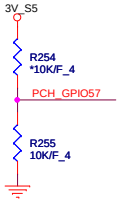
Board ID For Function	ID3 GPIO39	ID2 GPIO38	ID1 GPIO37	ID0 GPIO36
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	0	1	1
SOVP	0	1	0	0



Model ID	MODEL_ID0
INTEL	0
AMD	1



TPM physical presence	
PCH_GPIO57	Low: Default

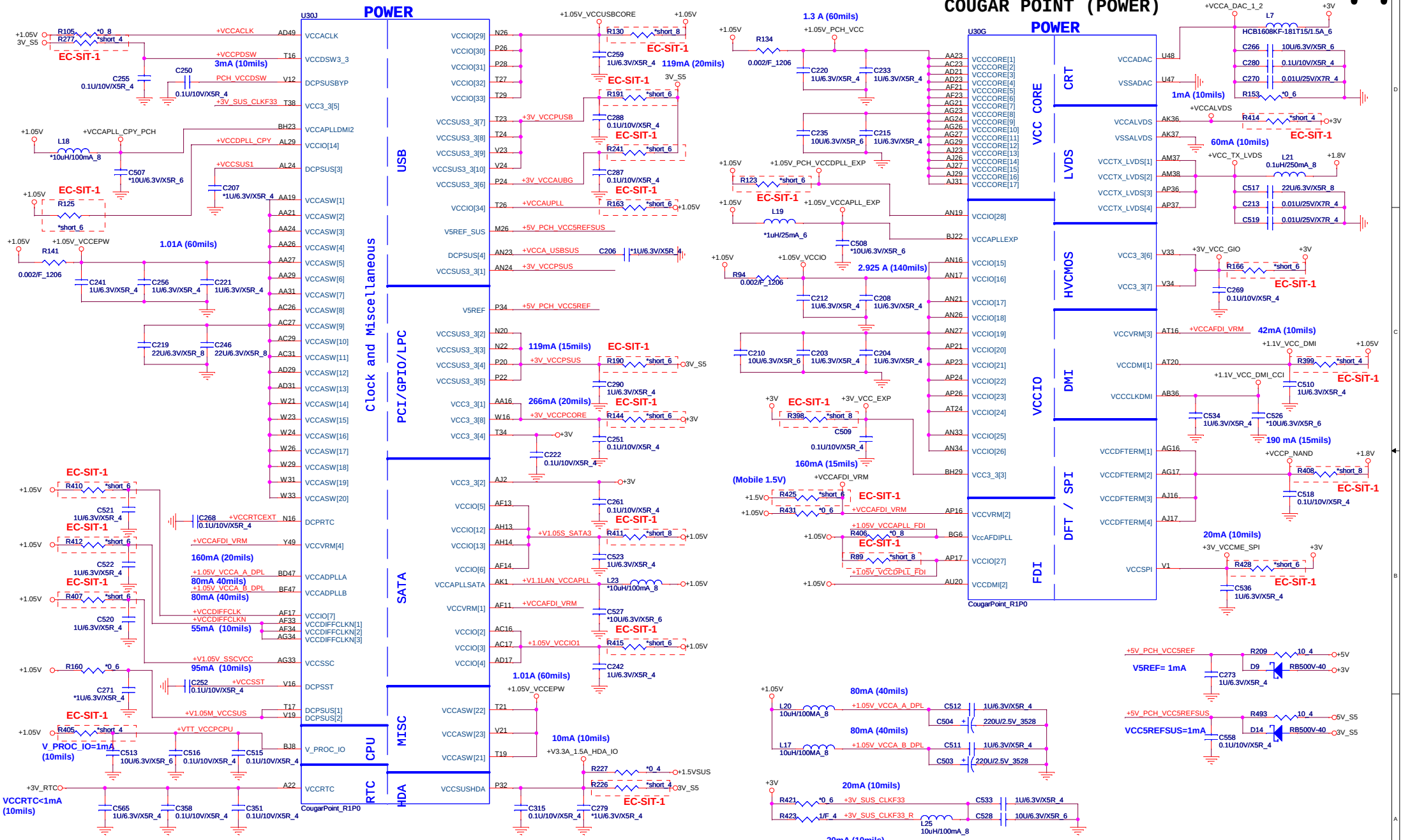


Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	PCH 4/6 (GPIO/MISC)	1A

Date: Monday, January 31, 2011 Sheet 10 of 43

Cougar Point-M (POWER)

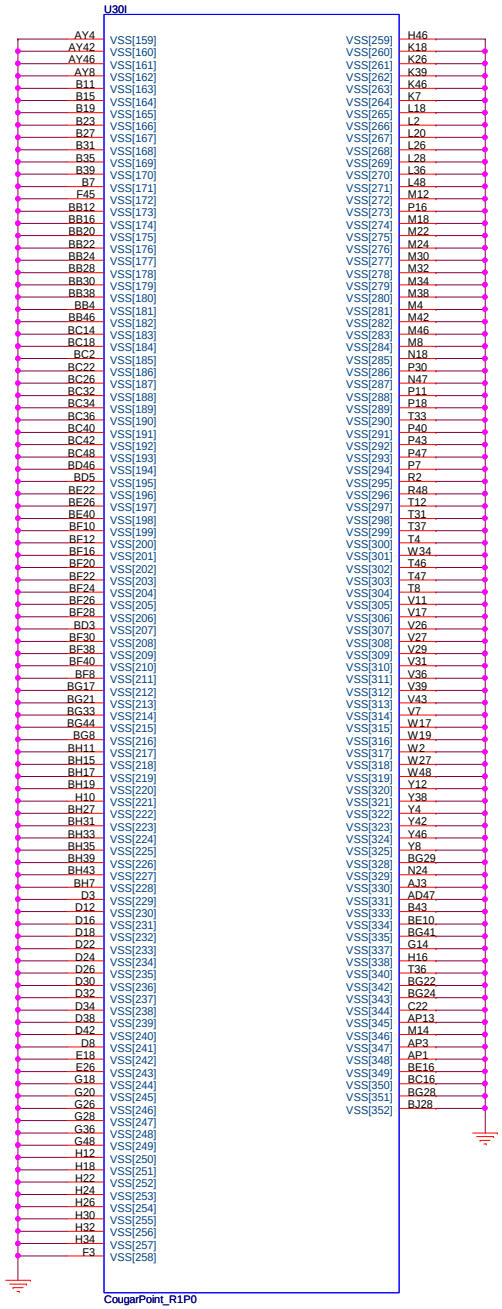


+3V_RTC (7,8,28)
3V_S5 (3,7,8,9,10,22,25,28,37)
+3V (3,7,8,9,10,13,14,15,16,18,19,21,22,23,24,25,26,27,28,29,31,32,33,34,35,37)
5V_S5 (20,37)
+5V (7,15,16,18,19,24,26,29,37)
+1.05V (3,5,7,8,9,29,33,37)
+1.5VSUS (3,13,14,29,32,37)
+1.8V (5,8,33,37)

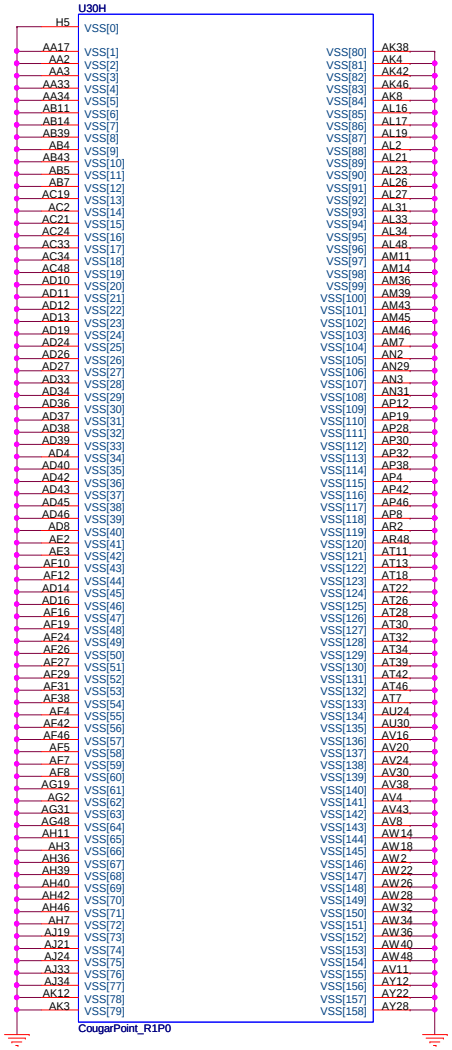
Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	PCH 5/6 (POWER)	1A
Date: Monday, January 31, 2011	Sheet 11 of 43	

IBEX PEAK-M (GND)



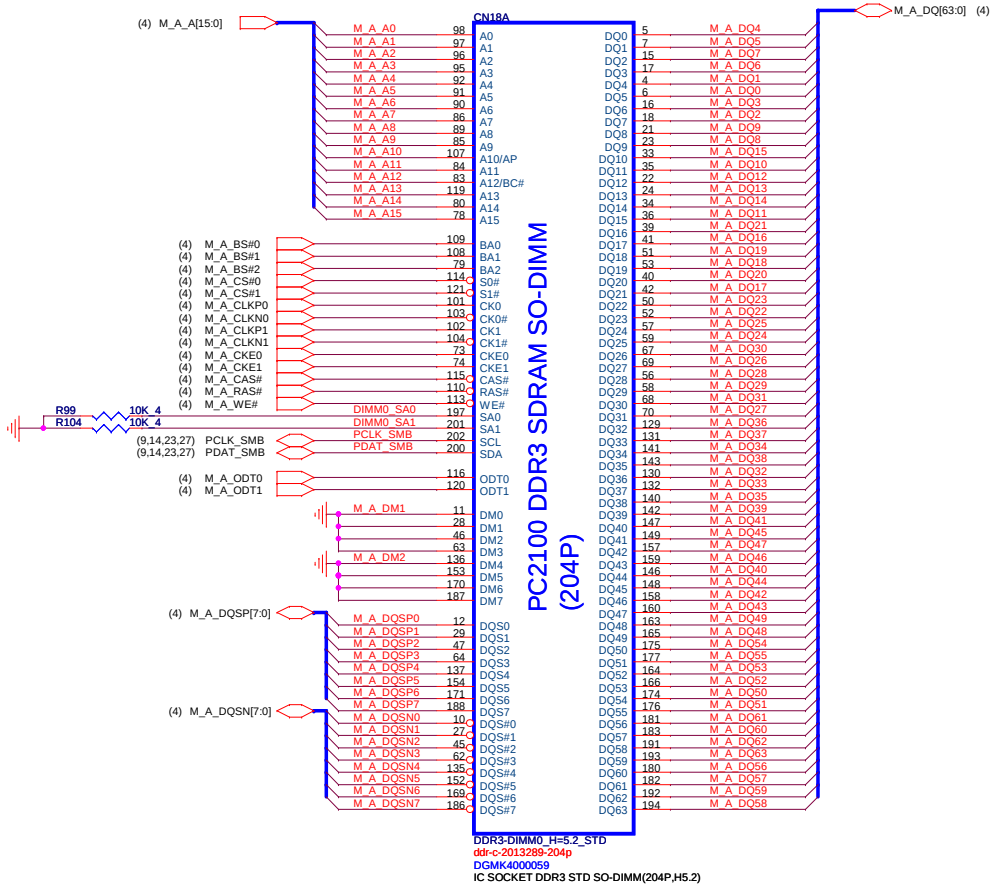
IBEX PEAK-M (GND)

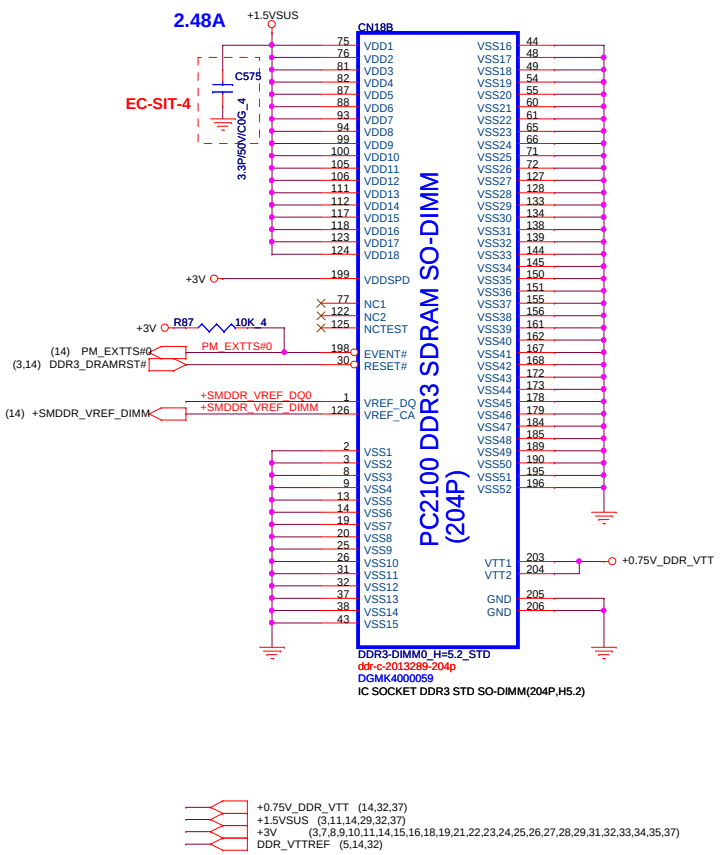


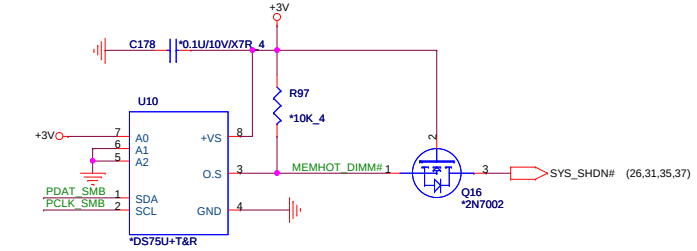
Quanta Computer Inc.

PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	PCH 6/6 (GND)	1A
Date: Monday, January 31, 2011	Sheet 12 of 43	

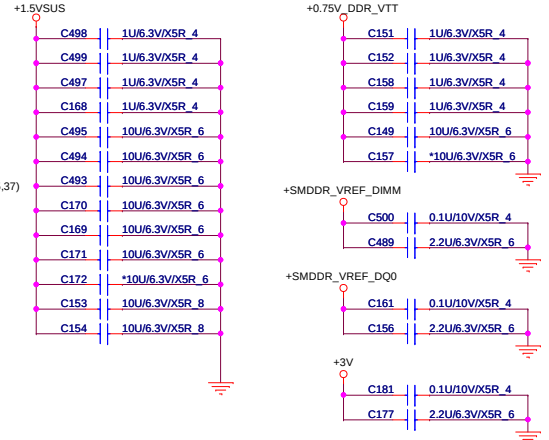






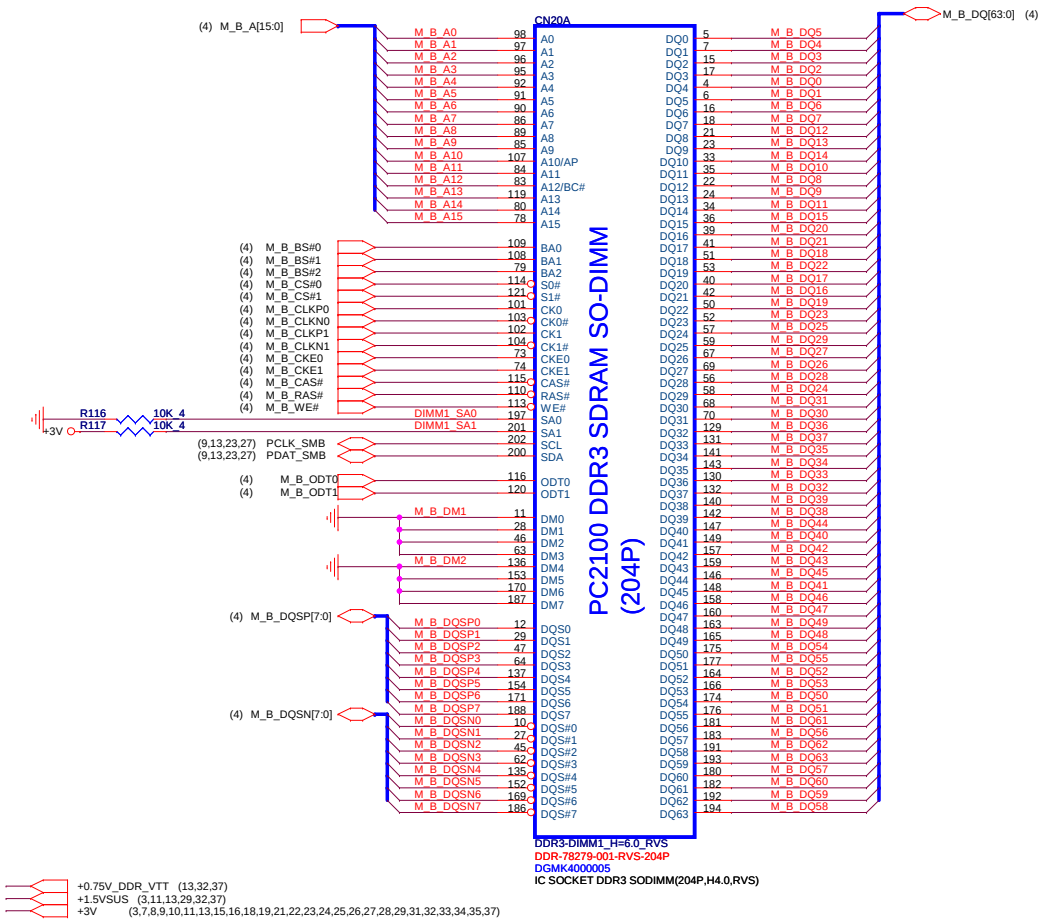
ADDRESS: 92H Close DDR3 socket CN22,CN23

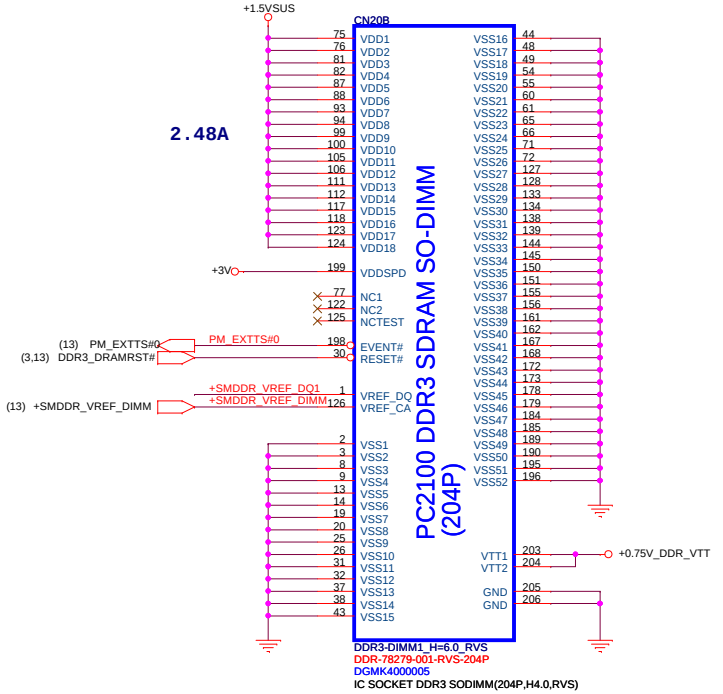
Place these Caps near So-Dimm0.



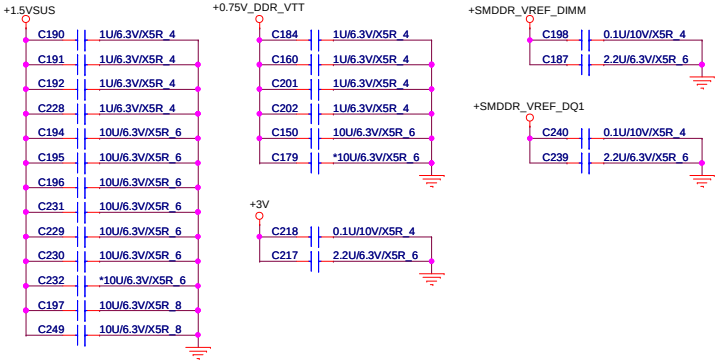
VREF DQ0 M1 Solution

Quanta Computer Inc.		
PROJECT D/M NOTE INTEL HURON RIVER		
Size	Document Number Custom	Rev 1A
	DDR3 DIMM0-STD (5.2H)	
Date: Monday, January 31, 2011	Sheet 13 of 43	

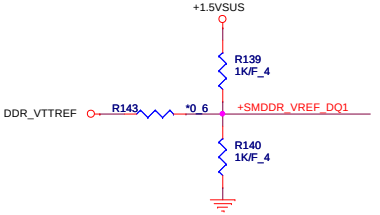




Place these Caps near So-Dimm1.



VREF DQ1 M1 Solution



Quanta Computer Inc.

PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	Custom DDR3 DIMM1-RVS (4.0H)	1A
Date: Monday, January 31, 2011	Sheet 14 of 43	

+3V (3,7,8,9,10,11,13,14,16,18,19,21,22,23,24,25,26,27,28,29,31,32,33,34,35,37)
3VPCU (8,16,17,20,27,28,29,31,33,36,37)
+15V (25,31,32,37)
+5V (7,11,16,18,19,24,26,29,37)
VIN (29,31,32,33,34,35,36,37)
5VSUS (27,35,37)
5VPCU (29,31,32,33,34,36,37)

LCDVCC

+15V, +3V, +LCDVCC
R345 330K_4
Q30 AO3404
R343 22_8
C417 10U/6.3V/X5R_8
LCDVCC_ON
C422 0.022U/25V/X7R_6
5VPCU
Q32 2N7002W
Q31 2N7002W
R347 100K_4
Q33 PDTC144EU
(7) INT_DISP_ON
R346 10K_4

Back light

3VPCU, +3V
R10 10K_4
R359 *4.7K_4
(16,28) LID#
D1 RB500V-40
D2 RB500V-40
DISPON
SC4 *0.1U/10V/X5R_4
C19 0.1U/10V/X5R_4
For ESD
R16 100K_4
C21 *47P/50V/NPO_4
(7) INT_LVDS_BLON
R372 2.2K_4
R371 10K_4
C426 *1U/10V/X5R_6
Q36 PDTC144EU
LCD_BK_OFF (8)

EC-SIT-1

(7) INT_DPST_PWM
R17 *short_4
VADJ_PWM
C22 *47P/50V/NPO_4

EC-SIT-1

GFX_PWR_SRC
C419 0.1U/25V/X7R_6
C421 0.1U/25V/X7R_6
C418 *10U/25V/X6S_12
R344 *short_8
VIN

For ESD

SC1 *0.1U/10V/X5R_4
C420 2.2U/6.3V/X5R_6
LVD-A30SFYG+
+LCDVCC
+3V
(7) INT_EDIDCLK
(7) INT_EDIDDATA
(7) INT_TXLOUTN0
(7) INT_TXLOUTP0
R520 0_4
R521 0_4
INT_EDIDCLK
INT_EDIDDATA
INT_TXLOUTN0_R
INT_TXLOUTP0_R
(7) INT_TXLOUTN1
(7) INT_TXLOUTP1
R522 0_4
R523 0_4
INT_TXLOUTN1_R
INT_TXLOUTP1_R
(7) INT_TXLOUTN2
(7) INT_TXLOUTP2
R524 0_4
R525 0_4
INT_TXLOUTN2_R
INT_TXLOUTP2_R
(7) INT_TXLCLKN
(7) INT_TXLCLKP
R526 0_4
R527 0_4
INT_TXLCLKN_R
INT_TXLCLKP_R
(27) LOGO_LED_A#
5VSUS
LOGO_LED_A#
+CAM_VCC
USBP3+_R
USBP3-_R
VADJ_PWM
DISPON
GFX_PWR_SRC
CN1

For RF

EC-SIT-5

For EMI

INT_TXLCLKN
INT_TXLCLKP
C8 6.8P/50V/X7R_4
C9 6.8P/50V/X7R_4

For ESD / For EMI

INT_EDIDCLK
INT_EDIDDATA
SC2 *0.1U/10V/X5R_4
C10 2200P/50V/X7R_4
SC3 *0.1U/10V/X5R_4
C11 2200P/50V/X7R_4
For ESD
For EMI
For ESD

LOGO_LED_A#

*Clamp-Diode_4
C15

LOGO_LED_A# / For EMI

C7 2200P/50V/X7R_4

+3V
C13 *47P/50V/NPO_4
C12 *47P/50V/NPO_4
close to CN2

+3V
R6 2.2K_4
R5 2.2K_4
INT_EDIDCLK
INT_EDIDDATA

LVDS (11.6") (1024x600, 1366x768)

FOR ESD

(9) USBP3-
(9) USBP3+
R3 *short_4
CML1
*DLW21HN900SQ2L
R4 *short_4
USBP3-_R
USBP3+_R
U24
IO1 VIN
IO2 GND
*PJSR05
+CAM_VCC

CAMERA VCC Control

+5V
R349 10K_4
R350 10K_4
Q35 AOS3413
R348 *0_6
(10) CCD_ON
Q34 CHDTC144EUPT
C425 2200P/50V/X7R_6
+CAM_VCC
C424 1U/6.3V/X5R_4
C423 0.1U/10V/X7R_4

Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	LCD/CAMERA	1A
Date: Monday, January 31, 2011	Sheet 15 of 43	

(8,15,17,20,27,28,29,31,33,36,37) 3VPCU
(3,7,8,9,10,11,13,14,15,18,19,21,22,23,24,25,26,27,28,29,31,32,33,34,35,37) +3V
(7,11,15,18,19,24,26,29,37) +5V

(7) CRT_R_CON
(7) CRT_G_CON
(7) CRT_B_CON

L3 BLM18BA470SN1 VGA_RED_L
L2 BLM18BA470SN1 VGA_GRE_L
L1 BLM18BA470SN1 VGA_BLU_L

C20 5.6P/50V/COG_4
C5 5.6P/50V/COG_4
C3 5.6P/50V/COG_4
C16 5.6P/50V/COG_4
C14 5.6P/50V/COG_4
C4 5.6P/50V/COG_4

EC-SIT-6

For ESD

+5V
SC5 *0.1U/10V/X5R_4
SC6 *0.1U/10V/X5R_4

CRT@88511-1401

VGA_RED_L
VGA_GRE_L
VGA_BLU_L

3VPCU +3V
(15,28) LID#
(7) HSYNC
(7) VSYNC
(7) CRTDCLK
(7) CRTDDAT

R2 *2.2K_4
R1 *2.2K_4

CN2

+3V

EC-DV-01

R82 499/F_4 HDMI_TX2+
R81 499/F_4 HDMI_TX2-
R78 499/F_4 HDMI_TX1+
R77 499/F_4 HDMI_TX1-
R74 499/F_4 HDMI_TX0+
R71 499/F_4 HDMI_TX0-
R68 499/F_4 HDMI_CLK+
R62 499/F_4 HDMI_CLK-

HDMI_LF

+5V
Q11 2N7002K-T1-E3

+3V
R56 2.2K_4
R55 2.2K_4

(7) INT_HDMI_SCL
(7) INT_HDMI_SDA

Q9 FDV301N
Q12 FDV301N

+5V
R63 2.2K_4
R72 2.2K_4

+5V
F2 FUSE1A6V_POLY

HDMIC_5V
HP_DET

HDMI_DDC_CLK
HDMI_DDC_DAT

(7) HDMI_TX2+
(7) HDMI_TX2-
(7) HDMI_TX1+
(7) HDMI_TX1-
(7) HDMI_TX0+
(7) HDMI_TX0-
(7) HDMI_CLK+
(7) HDMI_CLK-

CN16
SHELL1
D2+
D2 Shield
D2-
D1+
D1 Shield
D1-
D0+
D0 Shield
D0- GND
CK+
CK Shield GND
CK-
CE Remote
NC
DDC CLK
DDC DATA
GND
+5V
HP DET
SHELL2

SP@HDMI

U7 *RClamp0514M_AG
U5 *RClamp0514M_AG
U4 *RClamp0514M_AG

HDMI_TX2+ HDMI_TX2-
HDMI_TX1+ HDMI_TX1-
HDMI_TX0+ HDMI_TX0-
HDMI_CLK+ HDMI_CLK-
HDMI_DDC_DAT HDMI_DDC_CLK
HDMIC_5V HP_DET

VCC GND

For ESD
Layout note:Place close to HDMI Conn

EMI reserve for HDMI

HDMI_TX2+ R83 *100/F_4
HDMI_TX2-
HDMI_TX1+ R79 *100/F_4
HDMI_TX1-
HDMI_TX0+ R76 *100/F_4
HDMI_TX0-
HDMI_CLK+ R70 *100/F_4
HDMI_CLK-

+3V
R75 10K_4
(7) HDMI_HPD
Q13 2N7002K-T1-E3

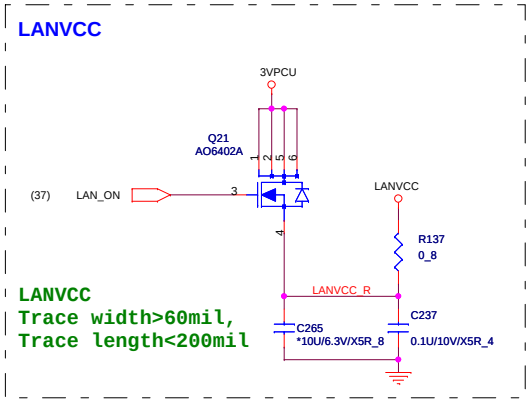
+3V
R54 10K_4
Q6 2N7002K-T1-E3
HP_DET
R59 20K/F_4

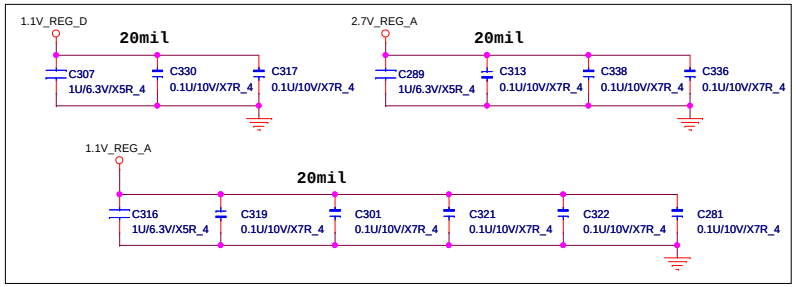
HDMIC_5V
C485 220P/50V/X7R_4
For EMI

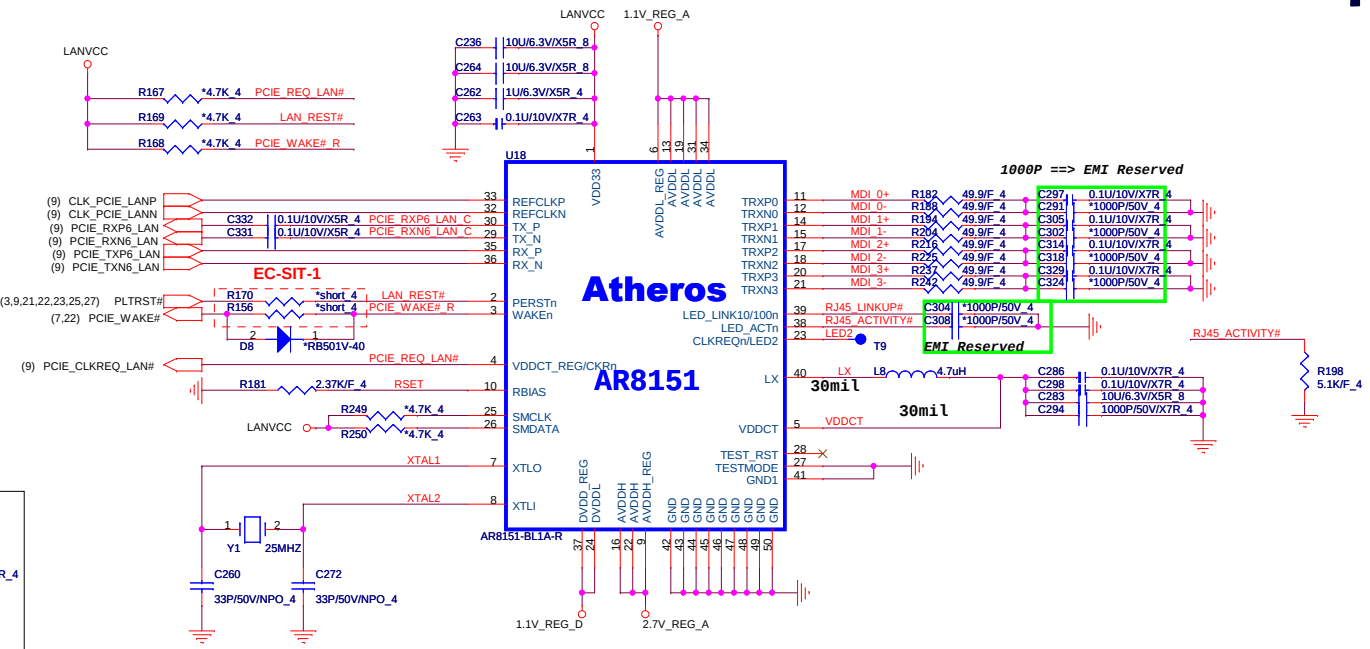
Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER

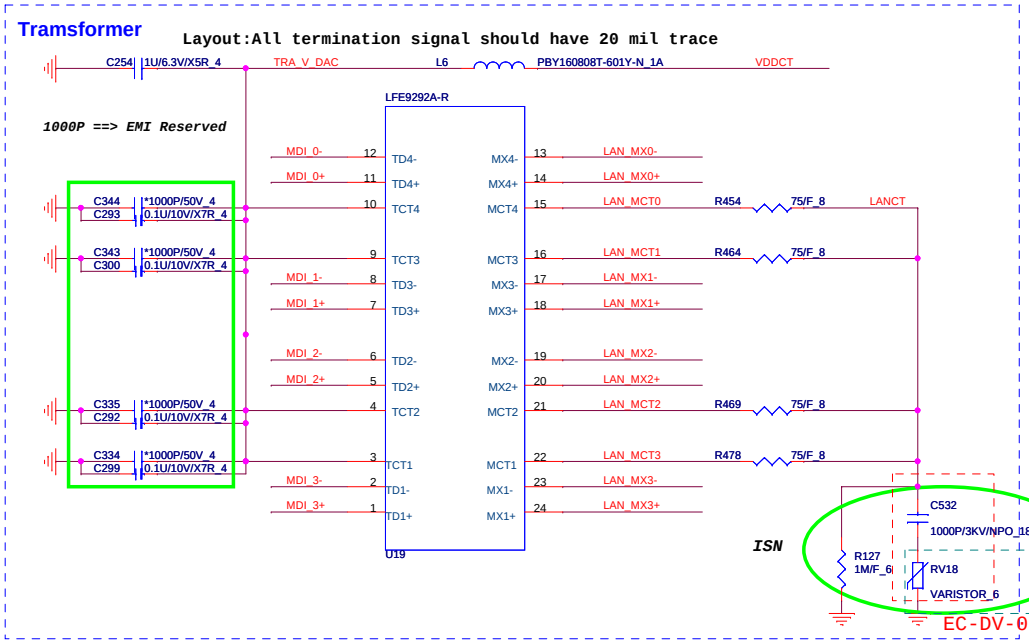
Size	Document Number	Rev
Custom	<Doc> CRT/HDMI CONN	1A
Date: Monday, January 31, 2011	Sheet 16 of 43	

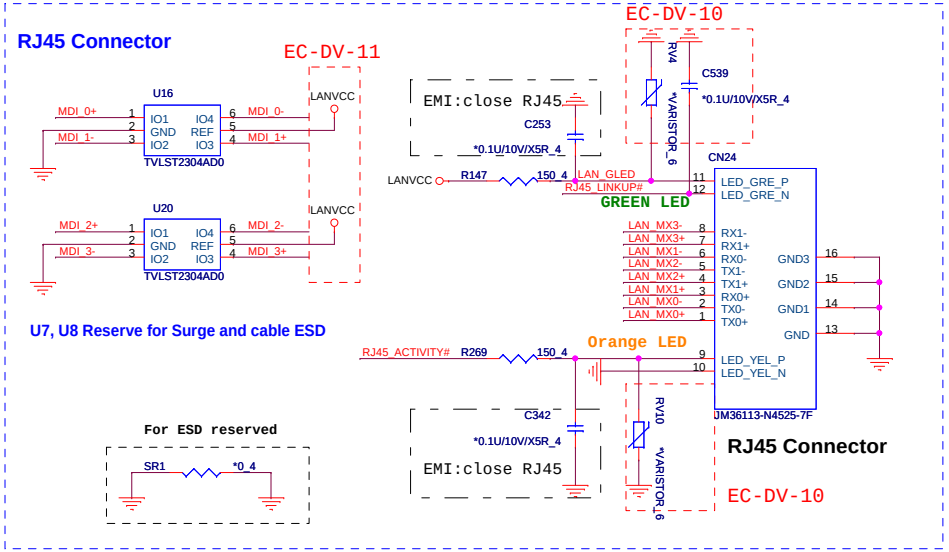
LAN: AR8151-BL1A-R











Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER
Size Custom
Document Number LAN_AR8151-BL1A-R++
Rev 1A
Date: Monday, January 31, 2011
Sheet 17 of 43

Note:
To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 pins must be powered by a rail that is not removed unless AC power is removed.

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.

+3V (3,7,8,9,10,11,13,14,15,16,19,21,22,23,24,25,26,27,28,29,31,32,33,34,35,37)
+5V (7,11,15,16,19,24,26,29,37)

HD Audio Bus

DIGITAL_MIC

For ESD reserved

For EMI

For ESD reserved

INT Speaker

PC BEEP CONTROL

Close to codec

From EC

From SB

EMI Reserved

Port Configuration

Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal analog mono or stereo MIC.
Port C: Microphone jack
Port G: Internal stereo speakers
Port J: Optional Internal stereo digital mic
Port H: S/PDIF (jack shared with headphone)

Sense For MIC/ Headphone out combo

External MIC/ Headphone out combo

Mount R57 (20K)
Vendor suggestion

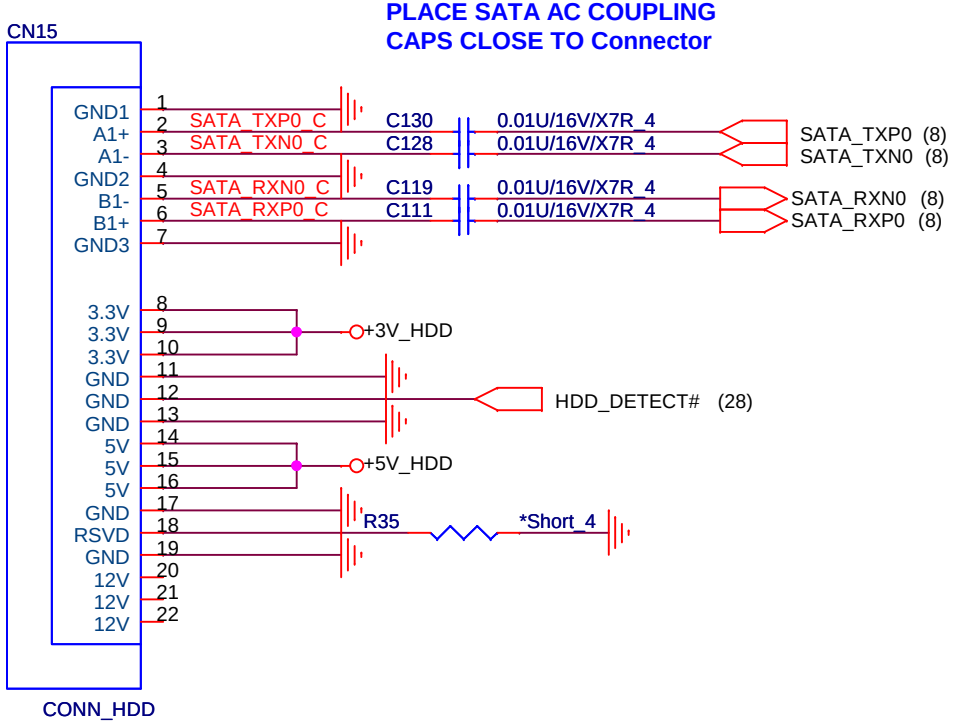
ESD Reserved

Quanta Computer Inc.			
PROJECT D/M NOTE INTEL HURON RIVER			
Size	Document Number		Rev
	AUDIO (CX20671, SPK)		1A
Date: Monday, January 31, 2011		Sheet 18 of 43	

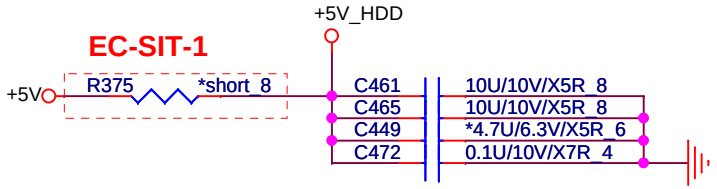
HDD

+3V (3,7,8,9,10,11,13,14,15,16,18,21,22,23,24,25,26,27,28,29,31,32,33,34,35,37)
+5V (7,11,15,16,18,24,26,29,37)

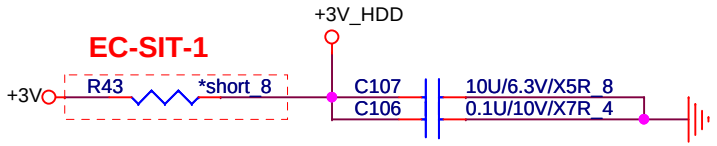
PLACE SATA AC COUPLING CAPS CLOSE TO Connector



DC Current rating: 2 A (MAX)



DC Current rating: 3 A (MAX)

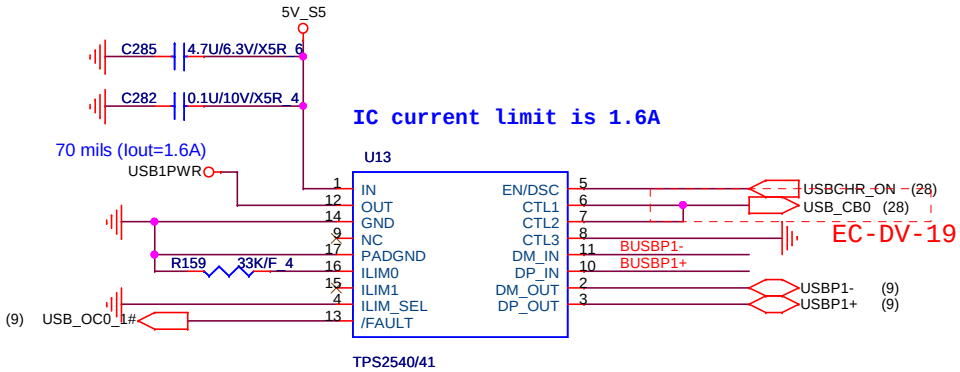


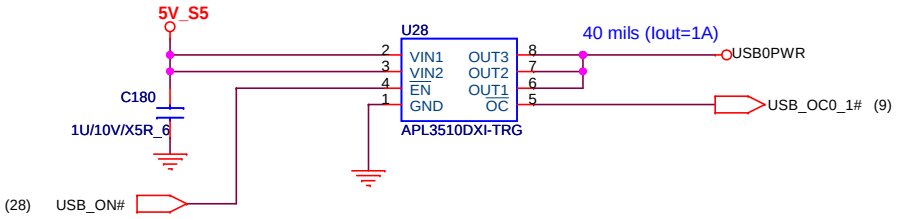
Quanta Computer Inc.		
PROJECT D/M NOTE INTEL HURON RIVER		
Size	Document Number: SATA	Rev: 1A
Date: Monday, January 31, 2011	Sheet 19 of 43	

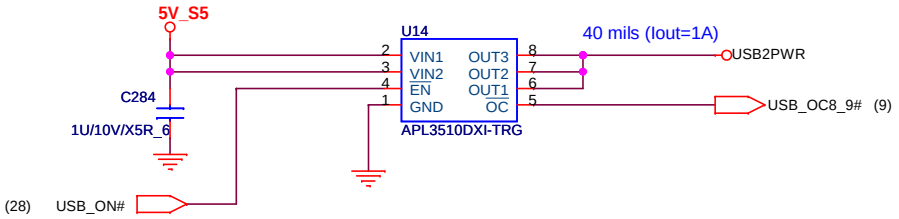
TPS2541 table

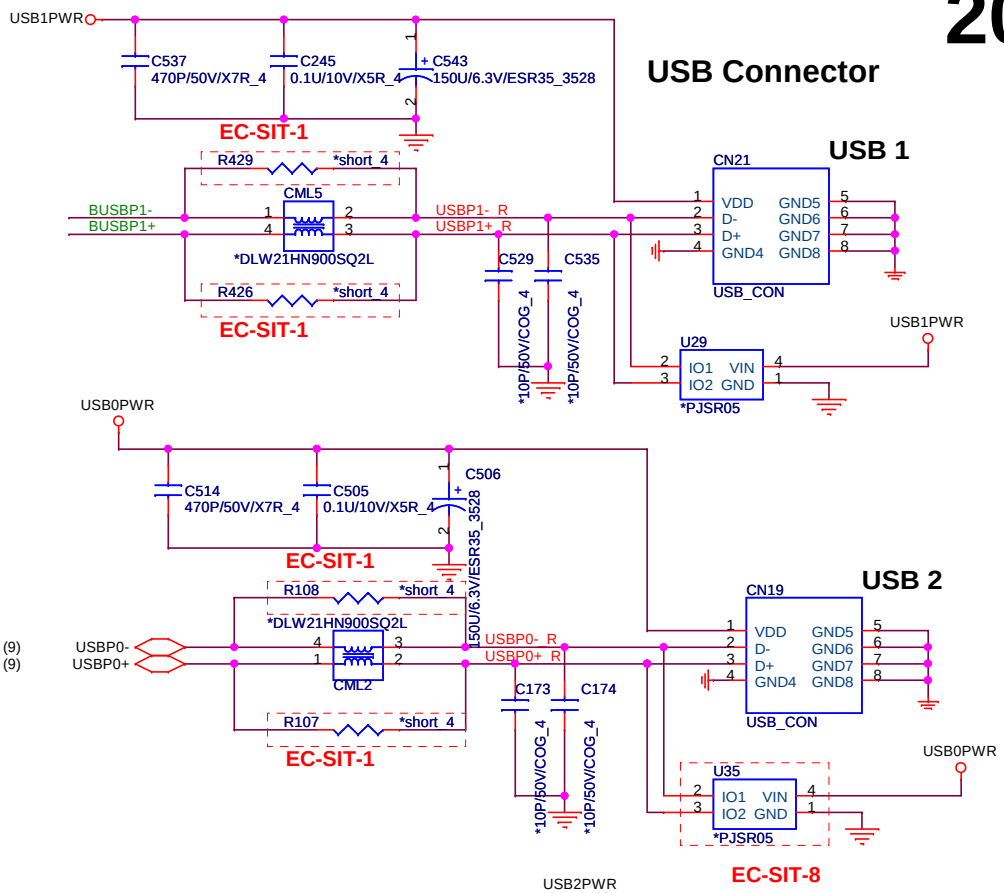
CTL1	CTL2	CTL3	Mode
0	0	X	Dedicated Charging Port, Auto-detect
0	1	X	Dedicated Charging Port, BC Specification 1.1 Only
1	0	X	Dedicated Charging Port, Apple Only
1	1	0	Standard Downstream Port, USB 2.0 Mode
1	1	1	Charging Downstream Port, BC Specification 1.1

Table 3 – TPS2541 Control Truth Table









5V_S5 (11,37)
3VPCU (8,15,16,17,27,28,29,31,33,36,37)

Quanta Computer Inc.

PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	USB x 3	1A
Date: Monday, January 31, 2011	Sheet 20 of 43	

+3V (3,7,8,9,10,11,13,14,15,16,18,19,22,23,24,25,26,27,28,29,31,32,33,34,35,37)

EC-SIT-1

(3,9,17,22,23,25,27) PLTRST# R480 *short_4 PLTRST#_R

(9) PCIE_CLKREQ_CARD# R476 *short_4

+3V R465 0_8 +3V_R

C552 0.1U/10V/X5R_4

R475 6.2K/F_4 RREF

SD_CD#

SD_WP

U33

RREF 48 | 3V3_IN 47 | CLK_REQ# 46 | PERST# 45 | EEDO 44 | EECS 43 | EESK 42 | GPIOVEEDI 41 | MS_INS# 40 | SD_CD# 39 | SP15 38 | SP14 37

(9) PCIE_TXP3 PCIE_TXP3 1 HSIP

(9) PCIE_TXN3 PCIE_TXN3 2 HSIN

(9) CLK_PCIE_CARD 3 REFCLKP

(9) CLK_PCIE_CARD# 4 REFCLKN

AV12 5 AV12

C546 4.7U/10V/X5R_6 (9) PCIE_RXP3 PCIE_RXP3 C549 0.1U/10V/X5R_4 PCIE_RXP3_C 6 HSOP

(9) PCIE_RXN3 PCIE_RXN3 C548 0.1U/10V/X5R_4 PCIE_RXN3_C 7 HSON

GND 8 GND

DV12 C547 0.1U/10V/X5R_4 9 DV12

Card1_3V3 10 Card1_3V3

+3V 11 3V3_IN

12 Card2_3V3

C550 10U/10V/X5R_6 C551 0.1U/10V/X5R_4

SP13 36 | SP12 35 | SP11 34 | SP10 33 | SP9 32 | SP8 31 | SP7 30 | SP6 29 | SP5 28

DV12_S 27 DV12_S_R R509 0_4 DV12_S

GND 26 GND C572 4.7U/10V/X5R_6 C571 0.1U/10V/X5R_4

SD_D2 25 SD_D2_R R508 0_4 SD_D2

XD_CD# 13 | DV33_18 14 | GND 15 | SP1 16 | SP2 17 | SP3 18 | SP4 19 | SD_D1 20 | SD_D0 21 | SD_CLK 22 | SD_CMD 23 | SD_D3 24

SD_D3_R R505 0_4 SD_D3

SD_CMD_R R504 0_4 SD_CMD

SD_CLK_R R499 0_4 SD_CLK

C568 *22P/50V/NPO_4

SD_D0_R R495 0_4 SD_D0

SD_D1_R R489 0_4 SD_D1

DV33_18

C559 0.1U/10V/X5R_4 C557 *4.7U/10V/X5R_6

GND

AV12 L27 DV12 *0_8

R4~R9,C28 close to chip pin

It is recommended that mismatch trace length between CLK and DATA trace is 100 mils with maximum

RTS5209

4 IN 1 CARD READER

CN11

SD-DAT3	1	SD_D3
SD-CMD	2	SD_CMD
GND1	3	
SD-VCC	4	
SD-CLK	5	SD_CLK
GND2	6	
SD-DAT0	7	SD_D0
SD-DAT1	8	SD_D1
SD-DAT2	9	SD_D2
SD-CD	10	SD_CD#
SD-WP	11	SD_WP
SHIELD1-GND	12	
SHIELD2-GND	13	
SHIELD3-GND	14	
SHIELD4-GND	15	

VDD_SD

CARD READER SOCKET
DFHD11MR014
sdcard-cs1s-245-h-n-11p

Memory Card Power Supply

VDD_SD 800mA R511 0_8 Card1_3V3

C569 0.01U/16V/X7R_4 C570 0.1U/16V/X7R_4 C573 10U/6.3V/X5R_6

Use 0805 type and Trace width = 40 mil" at Card1_3V3

Note:

	SD/MMC	MS
SP1	SD_D7	
SP2	SD_D6	
SP3	SD_D5	
SP4	SD_D4	
SP5		MS_BS
SP6		
SP7		MS_D1
SP8		
SP9		MS_D0
SP10		MS_D2
SP11		
SP12		MS_D3
SP13		
SP14		MS_CLK
SP15	SD_WP	

Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	GC8F Card Reader	1A
Date: Monday, January 31, 2011	Sheet 21 of 43	

MiniCard WLAN connector

+3V (3,7,8,9,10,11,13,14,15,16,18,19,21,23,24,25,26,27,28,29,31,32,33,34,35,37)
+1.5V (11,23,32)
3V_S5 (3,7,8,9,10,11,25,28,37)

PCI-Express TX and RX direct to connector

CN23

(23) MINICARD_PME#	MINICARD_PME#	1 WAKE#	2 3.3V_1
(25) BBC0EX1		3 RESERVED_1	4 GND0
(25) BBC0EX2		5 RESERVED_2	6 1.5V_1
(9) PCIE_CLKREQ_WLAN#		7 CLKREQ#	8 UIM_PWR
		9 GND1	10 UIM_DATA
(9) CLK_PCIE_WLANN		11 REFCLK-	12 UIM_CLK
(9) CLK_PCIE_WLANP		13 REFCLK+	14 UIM_RESET
		15 GND2	16 UIM_VPP
		17 UIM_C8	18 GND3
		19 UIM_C4	20 W_DISABLE#
		21 GND4	22 PERST#
(9) PCIE_RXN2		23 PERn0	24 3.3VAUX1
(9) PCIE_RXP2		25 PERp0	26 GND5
		27 GND6	28 1.5V_2
		29 GND7	30 SMB_CLK
(9) PCIE_TXN2		31 PETn0	32 SMB_DATA
(9) PCIE_TXP2		33 PETp0	34 GND8
		35 GND9	36 USB_D-
		37 RESERVED_3	38 USB_D+
		39 RESERVED_4	40 GND10
		41 RESERVED_5	42 LED_WWAN#
		43 RESERVED_6	44 LED_WLAN#
		45 RESERVED_7	46 LED_WPAN#
		47 RESERVED_8	48 1.5V_3
		49 RESERVED_9	50 GND11
(10,25) BT_ON		51 RESERVED_10	52 3.3V_2

ACS-88911-5204

+3.3V_WLAN +3.3V_WLAN +1.5V

LPC_FRAME# (8,25,28)
LPC_AD0 (8,25,28)
LPC_AD1 (8,25,28)
LPC_AD2 (8,25,28)
LPC_AD3 (8,25,28)

EC-SIT-1
(8,25,28) SERIRQ — R420 *short_4 — T15

EC-SIT-1
WLAN_OFF_R# — R138 *short_4 — PLTRST# (3,9,17,21,23,25,27)

EC-SIT-1
R492 *short_4 — PCLK_DEBUG (9)
R491 *short_4 — LPC_DRQ#0 (8)

USBP4- C — R176 *Short_4 — USBP4- (9)
USBP4+ C — R175 *Short_4 — USBP4+ (9)

T8

3V_S5 — R409 *10K_4 — Q38 *PDTC144EU@NC
(7,17) PCIE_WAKE# — MINICARD_PME#

WLAN_OFF_R# — D7 RB500V-40 — WLAN_OFF# (10)
R129 *0_4

USBP4- C
USBP4+ C
U15 *PJSR05 (IO1, VIN, IO2, GND)
+3.3V_WLAN

+3.3V_WLAN +3V
R459 0_8

+1.5V
C563 0.01U/16V/X7R_4
C248 0.1U/10V/X5R_4
C209 10U/6.3V/X5R_8
C193 *47P/50V/NPO_4
close to CN22

+3.3V_WLAN
Place caps close to connector.
close to CN22
C545 0.1U/10V/X5R_4
C183 0.047U/10V/X7R_4
C238 0.1U/10V/X5R_4
C562 0.047U/10V/X7R_4
C223 4.7U/6.3V/X5R_6
C561 *47P/50V/NPO_4

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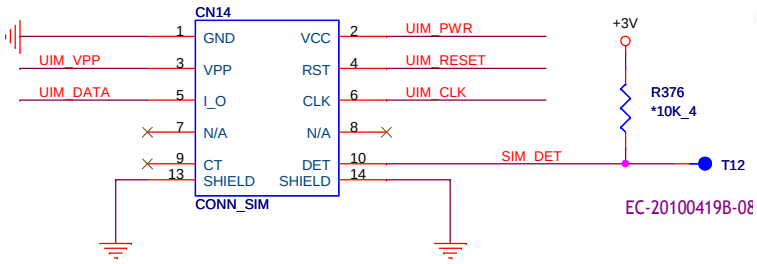
PROJECT D/M NOTE INTEL HURON RIVER

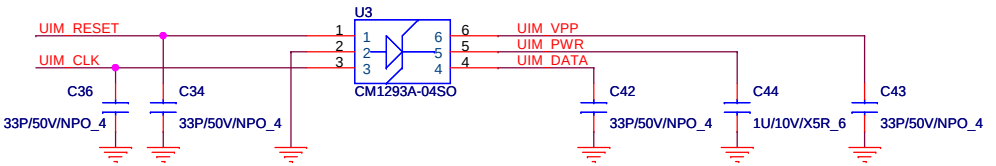
Size	Document Number	Rev
	WLAN	1A
Date: Monday, January 31, 2011	Sheet 22 of 43	

SIM Card CONN

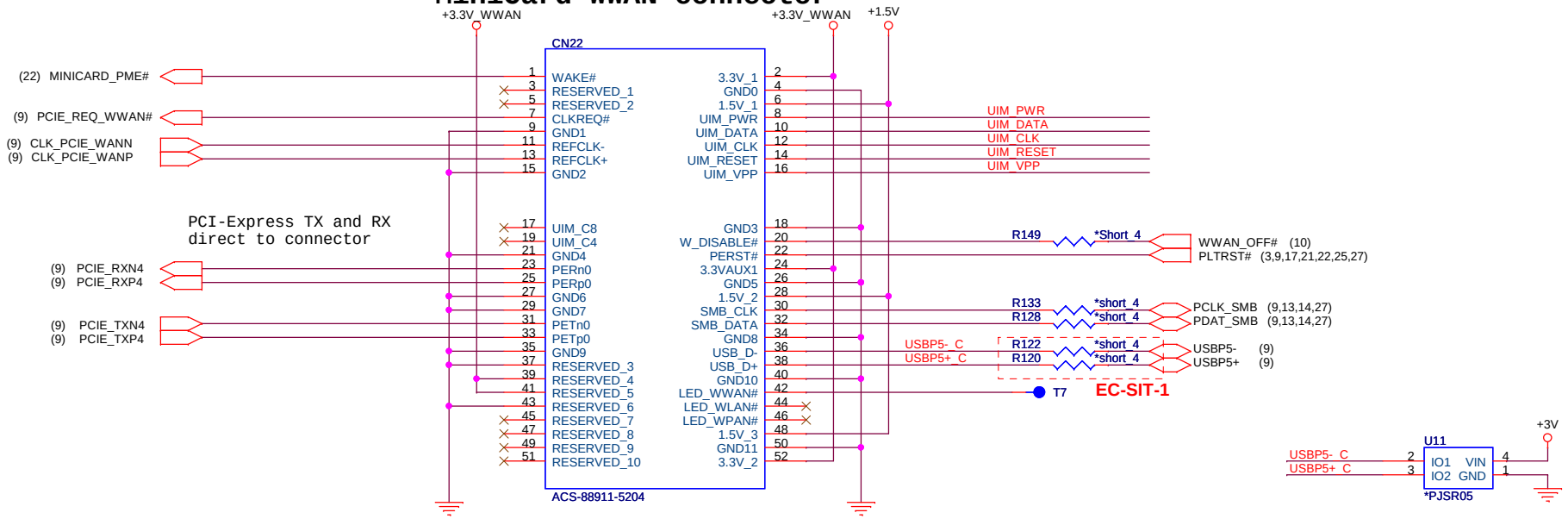


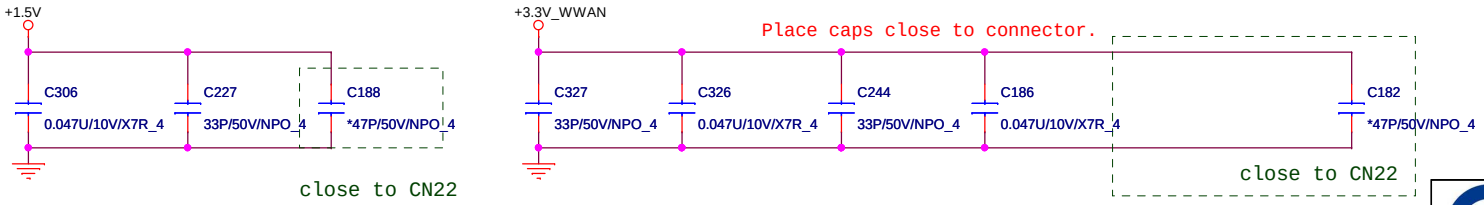
Layout Note:
UIM_RESET,UIM_CLK,UIM_DATA routting as short as possible

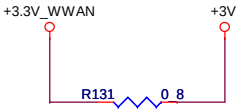
+3V (3,7,8,9,10,11,13,14,15,16,18,19,21,22,24,25,26,27,28,29,31,32,33,34,35,37)
+1.5V (11,22,32)



MiniCard WWAN connector



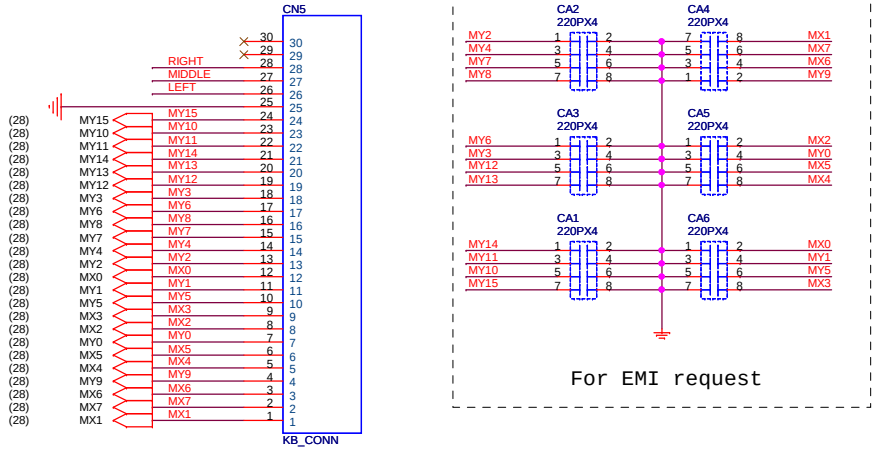




Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER

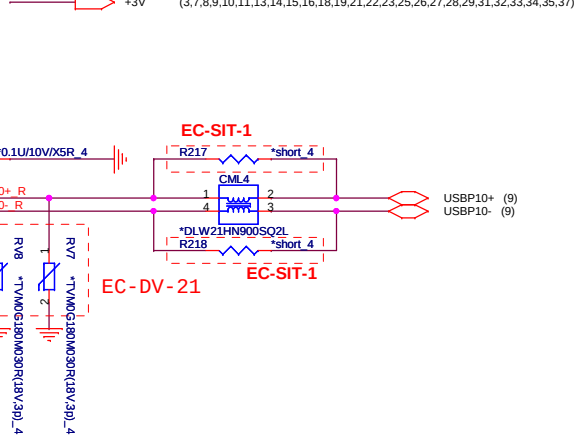
Size	Document Number	Rev
	WWAN	1A
Date: Monday, January 31, 2011	Sheet 23 of 43	

KEYBOARD

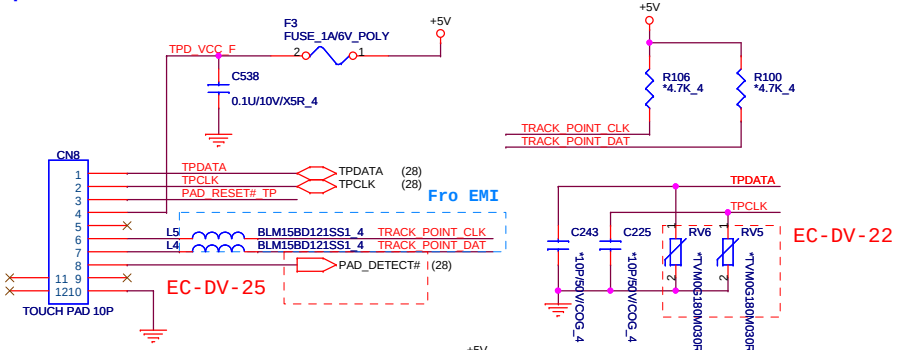


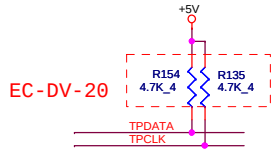
For EMI request

FINGER PRINTER for M NOTE

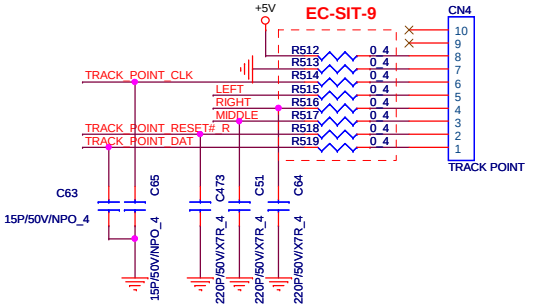


Touch pad

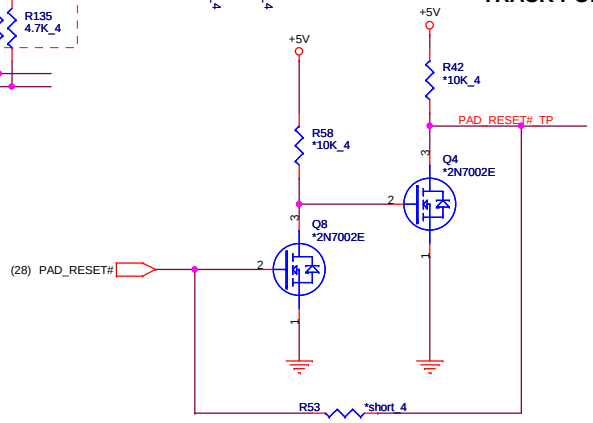


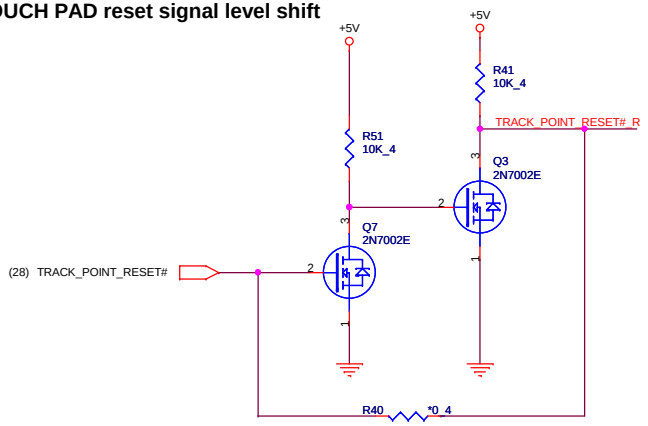


TRACK POINT



TRACK POINT/TOUCH PAD reset signal level shift



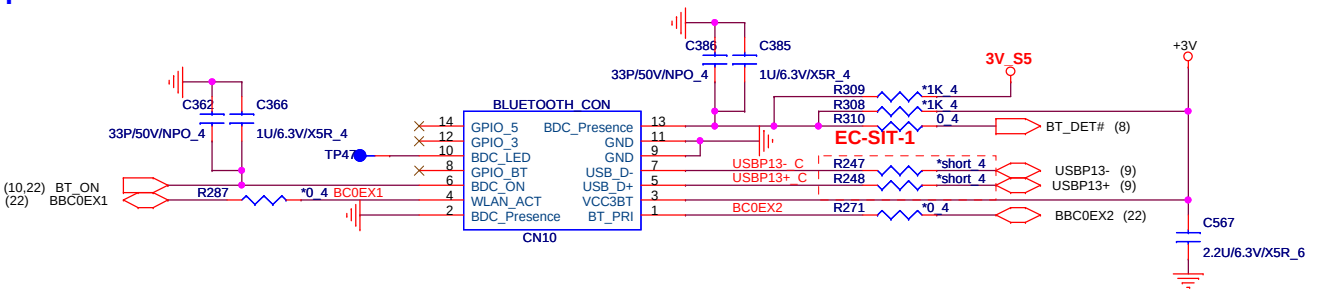


Quanta Computer Inc.

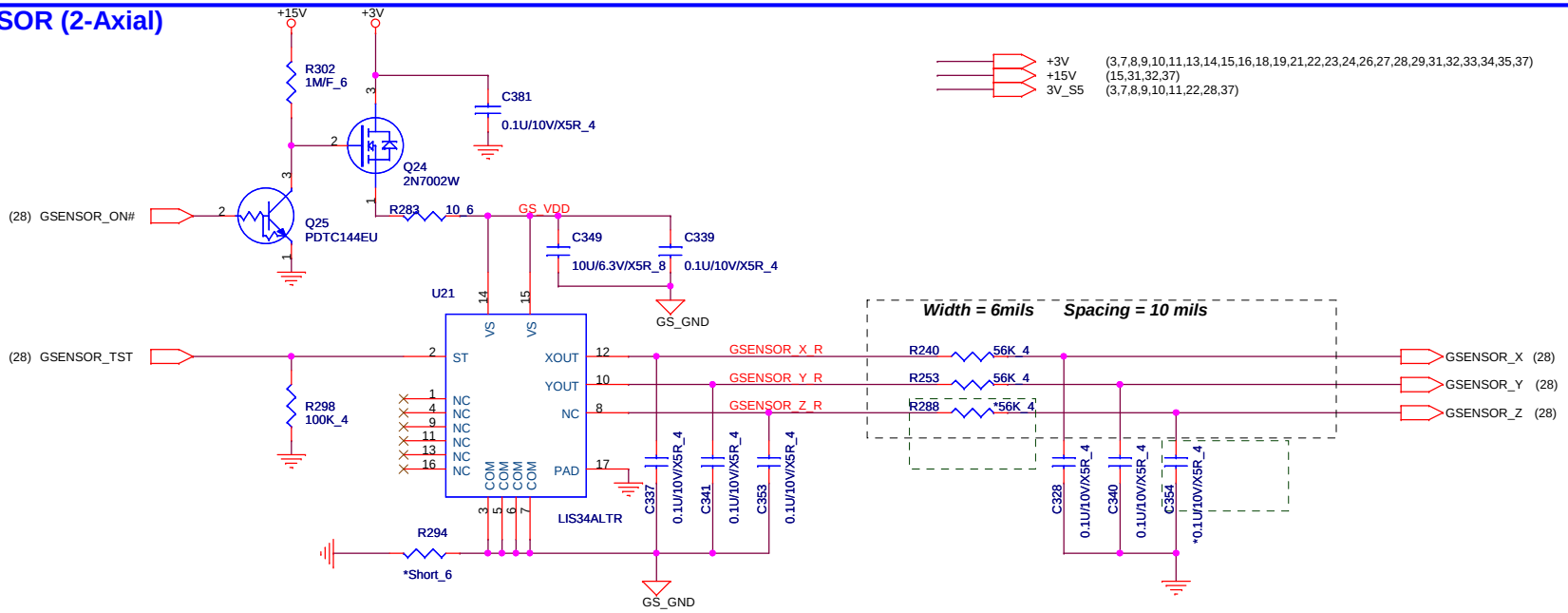
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	KB/TP	1A
Date: Monday, January 31, 2011	Sheet 24 of 43	

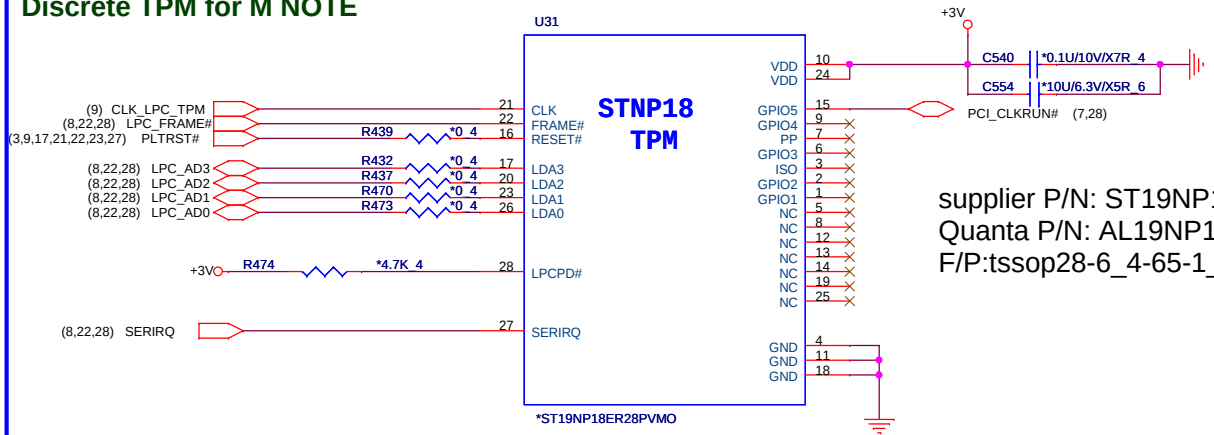
BLUETOOTH



G-SENSOR (2-Axial)



Discrete TPM for M NOTE

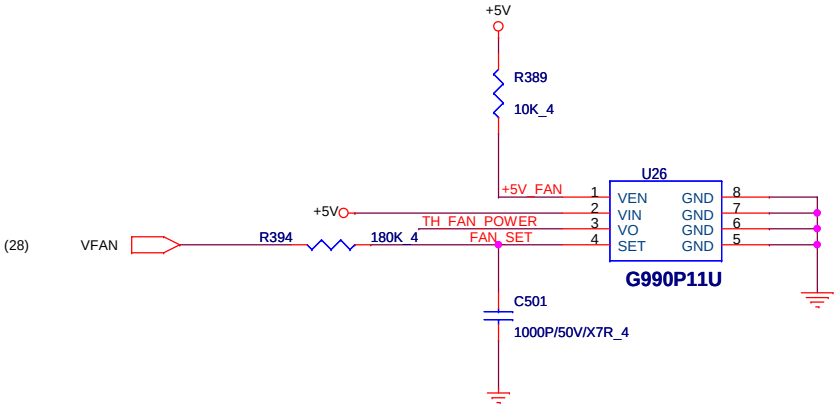


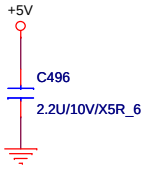
supplier P/N: ST19NP18ER28PVMO
Quanta P/N: AL19NP18K29
F/P:tssop28-6_4-65-1_2h

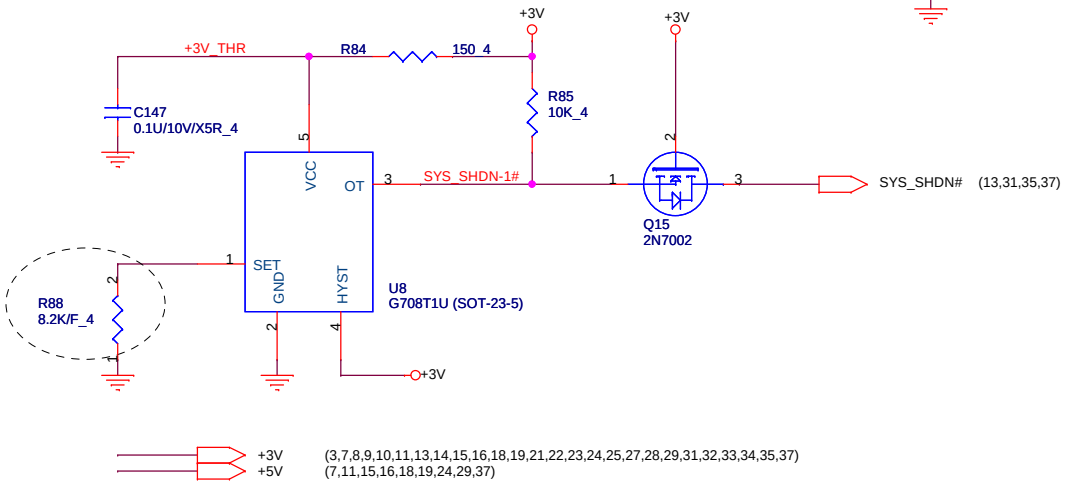
Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	BT/G-SENSOR/TPM	1A
Date: Monday, January 31, 2011	Sheet 25 of 43	

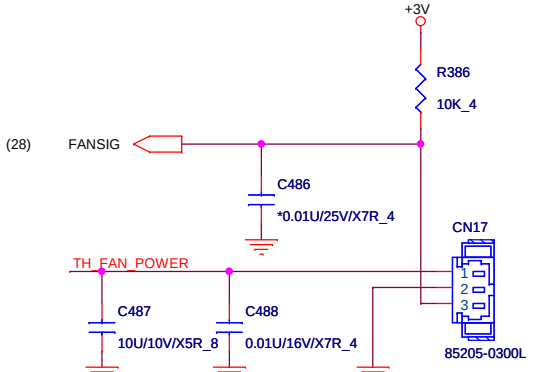
FANPWR = 1.6*VSET

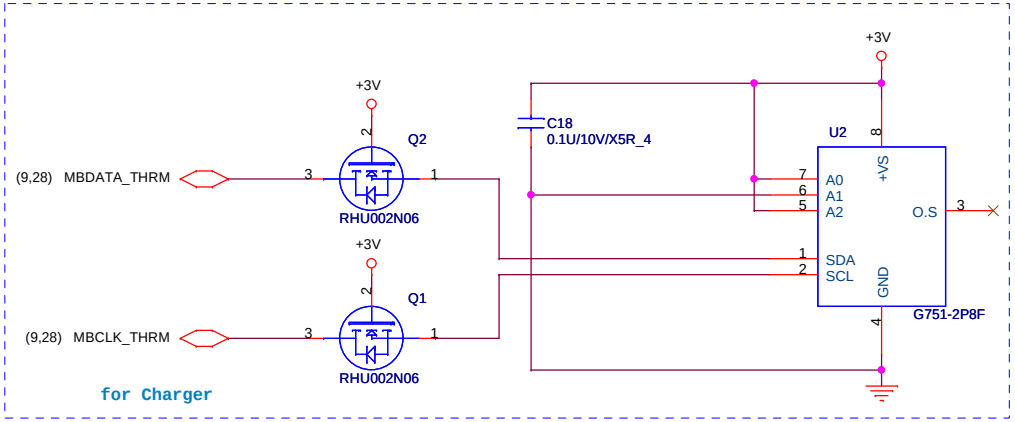






+3V (3,7,8,9,10,11,13,14,15,16,18,19,21,22,23,24,25,27,28,29,31,32,33,34,35,37)
+5V (7,11,15,16,18,19,24,29,37)





ADDRESS: 9AH

ADDRESS

1	0	0	1	A2	A1	A0	0

MSB LSB

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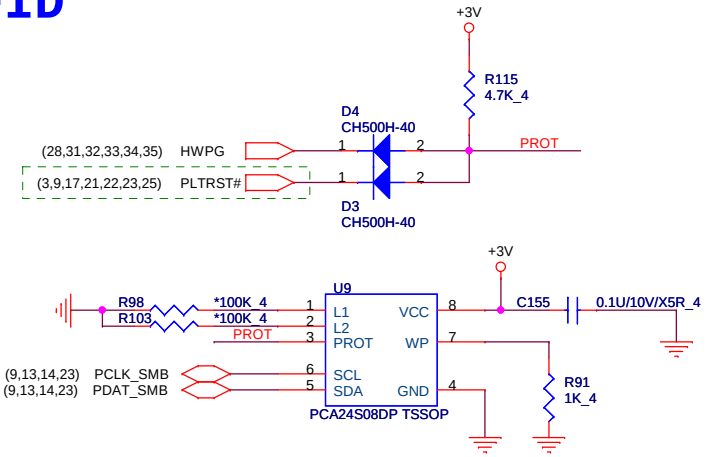
PROJECT D/M NOTE INTEL HURON RIVER

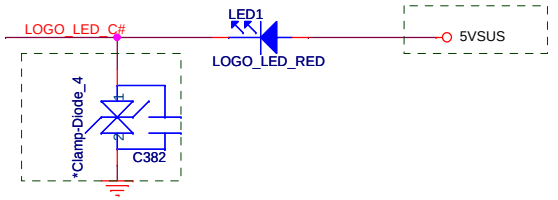
Size	Document Number	Rev
	FAN/Thermal	1A
Date: Monday, January 31, 2011	Sheet 26 of 43	

+3V (3,7,8,9,10,11,13,14,15,16,18,19,21,22,23,24,25,26,28,29,31,32,33,34,35,37)
3VPCU (8,15,16,17,20,28,29,31,33,36,37)
3V_S5 (3,7,8,9,10,11,22,25,28,37)
5VSUS (15,35,37)

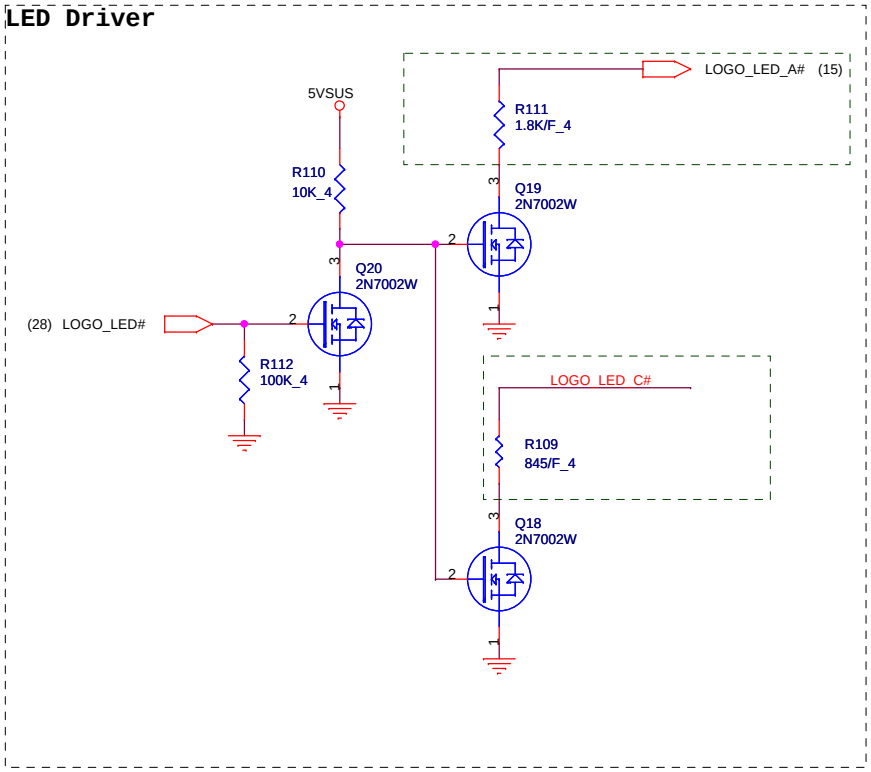
RFID



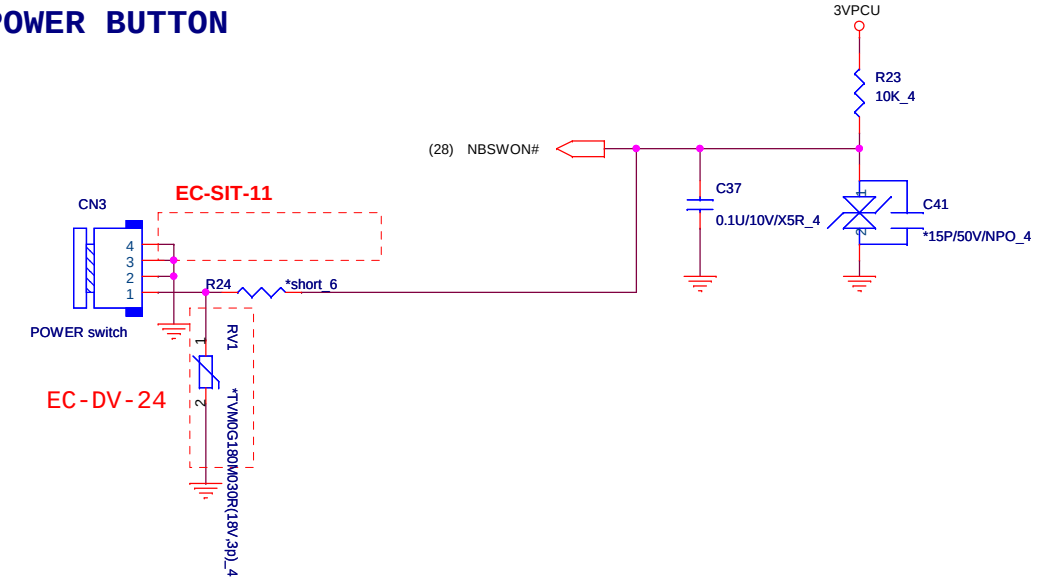
EC-SIT-10



LED Driver



POWER BUTTON



Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	SW/LED/RFID_EEPROM	1A
Date: Monday, January 31, 2011	Sheet 27 of 43	

(3,7,8,9,10,11,13,14,15,16,18,19,21,22,23,24,25,26,27,29,31,32,33,34,35,37) +3V
(8,15,16,17,20,27,29,31,33,36,37) 3VPCU
(7,8,11) +3V_RTC

IT8518

EC-SIT-1

RTC_VCC — R177 *0_4 — +3V_RTC
C275 *short_4

Layout Note:
Place all capacitors close to IT8512.

3VPCU
C211 0.1U/10V/X5R_4
C310 0.1U/10V/X5R_4
C214 0.1U/10V/X5R_4
C309 0.1U/10V/X5R_4
C323 0.1U/10V/X5R_4
C544 0.1U/10V/X5R_4

(9) PCLK_591 — PCLK_591 — C247 *15P/50V/NPO_4

EMI suggestion:
Add a 15p bypass CAP on CLK_PCI_8512

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

Layout Note:
Place this test point on top side

3VPCU — R148 470K_4 — WRST_8512# — C234 0.1U/10V/X5R_4 — TP21

IT8512_AVCC — L24 10_6 — 3VPCU
L9 BLM18AG121SN1D — 3VPCU
C530 1000P/16V/X7R_4
C531 1U/6.3V/X5R_4
C357 0.1U/10V/X5R_4
L26 BLM18AG121SN1D
(For PLL Power)

IT8512_VSTBY

+3V — 3VPCU — RTC_VCC
C267 0.1U/10V/X5R_4

U12
IT8518&19

TRACK_POINT_RESET — TP60 TP59 — TRACK_POINT_RESET# (24)
TP19 — ECPWROK (7)
G_SENSOR_ID — TP65 — DCIN_LED# (20)
USBCHR_ON (20)
R461 *Short_4 — PCI_CLKRUN# (7,25)

LPC
(8,22,25) LPC_AD0
(8,22,25) LPC_AD1
(8,22,25) LPC_AD2
(8,22,25) LPC_AD3
(15,16) LID#
PCLK_591
(8,22,25) LPC_FRAME#
(7) LPCPD#
(10) SIO_A20GATE
(8,22,25) SERIRQ
(10) SIO_EXT_SMI#
(10) SIO_EXT_SCI#
WRST_8512#
(10) SIO_RCIN#
D11 RB500V-40
D6 RB500V-40
D5 RB500V-40
D12 RB500V-40
TP22

GPIO
L80/HLAT/BAQ/WUI24/GPE3(DI)
L80LLA7/WUI7/GPE7(UP)
HMOSI/GPH6/ID6(Dn)
HMISO/GPH5/ID5(Dn)
HSCK/GPH4/ID4(Dn)
HSCE#/WUI19/GPH3/ID3(Dn)
CLKRUN#/WUI16/GPH0/ID0(Dn)

SM BUS
SMCLK0/GPB3(X) — MBCLK (36)
SMDAT0/GPB4(X) — MBDATA (36)
SMCLK1/GPC1(X) — MBCLK_THRM (9,26)
SMDAT1/GPC2(X) — MBDATA_THRM (9,26)
SMDAT2/WUI23/GPF7(Up) — VOLMUTE# (18)

PS/2
PS2CLK0/TMB0/GPF0(Up) — TP63
PS2DAT0/TMB1/GPF1(Up) — TP62
PS2CLK2/WUI20/GPF4(Up) — TPCLK (24)
PS2DAT2/WUI21/GPF5(Up) — TPDATA (24)

CIR
CRX0/GPC0(Dn)
CTX0/TMA0/GPB2(Dn)

PWM
PWM0/GPA0(Up) — PWR_BLUE# — TP74 — LOGO_LED# (27)
PWM1/GPA1(Up) — VFAN (26)
PWM2/GPA2(Up) — SUSPEND_LED# — TP71 — GSENSOR_ON# (25)
PWM3/GPA3(Up) — PCBEEP_AD (18)
PWM4/GPA4(Up)
PWM5/GPA5(Up)

TACH0A/GPD6(Dn) — H_PROCHOT_EC — FANSIG (26)
TACH1A/TMA1/GPD7(Dn)
TMRI0/WUI2/GPC4(Dn) — R232 *0_4 — TEMP_MBAT — HWPG — HWPG (27,31,32,33,34,35)
TMRI1/WUI3/GPC6(Dn) — C311 *1U/10V/X5R_4

UART port
DAC4/DCD0#/GPJ4(X)
DSR0#/GPG6(X)
GINT/CTS0#/GPD5(Up)
PS2DAT1/RTS0#/GPF3(Up)
DAC5/RIG0#/GPJ5(X)
PS2CLK1/DTR0#/GPF2(Up)
TXD/SOUT0/GPB1(Up)
RXD/SIN0/GPB0(Up)

(7) DNBSWON# — D10 RB500V-40 — DNBSWON_R
(20) USB_ON#
(7) ICH_RSMRST#
(20) USB_CB0
(7) AC_PRESENT
TP72 — BATLED_AMBER_LED#
TP73 — BATLED_GREEN_LED#

WAKE UP
PWRSW/GPE4(Up) — NBSWON# — NBSWON# (27), SIO_SLP_S3# (7), ACIN (36)
RI1#/WUI0/GPD0(Up)
RI2#/WUI1/GPD1(Up)
RING#/PWRFAIL#/CK32KOUT/LPCRST#/GPB7(Dn) — MAINON (32,33,34,37)

(25) GSENSOR_Z
(36) ACDC_ID
(7) PM_SLP_S4#
TP12

ADC5/DCD1#/WUI29/GPI5(X)
ADC6/DSR1#/WUI30/GPI6(X)
ADC7/CTS1#/WUI31/GPI7(X)
RTS1#/WUI5/GPE5(Dn)
PWM7/RIG1#/GPA7(Up)
DTR1#/SBUSY/GPG1/ID7(Dn)
CTX1/WUI18/SOUT1/GPH2/SMDAT3/ID2(Dn)
CRX1/WUI17/SIN1/SMCLK3/GPH1/ID1(Dn)

(24) PAD_DETECT#
(25) GSENSOR_TST
(37) SS_ON
(32,37) SUSON

EXTERNAL SERIAL FLASH
8512_SCK
8512_SCE#
8512_SI
8512_SO
FSCK
FSCE#
FMOSI
FMISO

A/D D/A
ADC0/GPI0(X) — R422 *short_4 — TEMP_MBAT (36)
ADC1/GPI1(X) — MBATV (36)
ADC2/GPI2(X) — AD_ID (36)
ADC3/GPI3(X) — GSENSOR_Y (25)
ADC4/WUI28/GPI4(X) — GSENSOR_X (25)

TACH2/GPJ0(X) — HDD_DETECT# (19)
GPJ1(X) — SIO_EXT_WAKE# (9)
DAC2/TACH0B/GPJ2(X) — BLC# — BLC# (36)
DAC3/TACH1B/GPJ3(X) — TP64

EC-DV-19

(24) PAD_RESET#
(35,37) VRON
TP13

KSO16/SMOSI/GPC3(Dn)
KSO17/SMISO/GPC5(Dn)
PWM6/SSCK/GPA6(Up)

SPI ENABLE
SSCE0#/GPG2(X)
SSCE1#/GPG0(X)

R229 100K_4 — (7) SUS_PWR_ACK

KBMX
KSO0/PD0
KSO1/PD1
KSO2/PD2
KSO3/PD3
KSO4/PD4
KSO5/PD5
KSO6/PD6
KSO7/PD7
KSO8/ACK#
KSO9/BUSY
KSO10/PE
KSO11/ERR#
KSO12/SLCT
KSO13
KSO14
KSO15

(24) MY[0..15]
MY0 MY1 MY2 MY3 MY4 MY5 MY6 MY7 MY8 MY9 MY10 MY11 MY12 MY13 MY14 MY15

(24) MX[0..7]
MX0 MX1 MX2 MX3 MX4 MX5 MX6 MX7

KSI0/STB#
KSI1/AFD#
KSI2/INIT#
KSI3/SLIN#
KSI4
KSI5
KSI6
KSI7

CLOCK
CK32KE/GPJ7 — IT8512_CK32KE
CK32K/GPJ6 — IT8512_CK32K
Y2 *32.768KHZ
C295 0_4
C296 *10P/50V/NPO_4

VSS VSS VSS VSS VSS VSS AVSS VCORE
C258 *1U/6.3V/X5R_4
C257 0.1U/10V/X5R_4

R101	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

EC-SIT-1

H_PROCHOT# Q — R95 *short_4 — H_PROCHOT# (3,35)
H_PROCHOT_EC — R101 100K_4
Q17 ME2N7002E

3V_SS
PWR_BLUE# — R132 *10K_4
BATLED_AMBER_LED# — R463 *10K_4
BATLED_GREEN_LED# — R230 *10K_4

3VPCU
MBCLK_THRM — R257 4.7K_4
MBDATA_THRM — R258 4.7K_4
MBCLK — R452 4.7K_4
MBDATA — R457 4.7K_4
PAD_RESET# — R102 10K_4
BLC# — R433 *10K_4
HDD_DETECT# — R430 100K_4
TRACK_POINT_RESET — R438 *10K_4
TEMP_MBAT — R196 *100K/F_4
+3V
HWPG — R233 10K_4

for EUP Lot6

EC-DV-06

G-sensor ID select
+3V — R251 *10K_4 — G_SENSOR_ID — R228 *10K_4

POWER SWITCH/ CARE BUTTON
3VPCU — R234 10K_4 — NBSWON# — C312 0.1U/10V/X5R_4

4Mbit (512k Byte), SPI

Winbond AKE37FN0N01
MAX AKE37FP0Z02

3VPCU
R510 10K_4
R506 10K_4
U34
8512_SCE# — CE#
8512_SCK — R503 47_4 — 8512_SCK1 — SCK
8512_SI — R502 47_4 — 8512_SI1 — SI
8512_SO — R501 15_4 — 8512_SO1 — SO
VDD HOLD# WP# VSS
W25X40BVSSIG
C566 0.1U/10V/X5R_4

For ESD

MBCLK
MBDATA
SC20 *0.1U/10V/X5R_4
SC21 *0.1U/10V/X5R_4
close battery connector

Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	KBC IT8518/19	1A
Date: Monday, January 31, 2011	Sheet 28 of 43	

Hole for CPU support

HOLE13 *H-C142D142N
HOLE15 *H-C142D142N
HOLE12 *H-C142D142N
HOLE14 *H-C142D142N

MiniCard WWAN

HOLE18 H-TC217BIC142D102P2

MiniCard WLAN

HOLE17 H-TC217BIC142D102P2

BLUETOOTH

HOLE8 H-TC217BC59I99D59PT

CRT

Spad1 *Spad1

Keyboard

HOLE7 *O-FL7C-2

SB

HOLE16 H-TC5_5BC4I3D3P2
HOLE20 H-TC5_5BC4I3D3P2

EC-DV-03

HOLE2 *h-c197I117d87p2

Boundary Hole

HOLE4 *H-C71d71n
HOLE1 *HG-C197D91P2
HOLE5 *H-o106x87d106x87n

Boundary Hole

HOLE11 *HG-C217D87P2
HOLE10 *HG-C217D87P2
HOLE9 *HG-C217D87P2
HOLE6 *HG-C217D87P2
HOLE3 *HG-C217D91P2

Fro ESD

+1.5V_CPU: SC10 SC11
3VPCU: SC12 SC13 SC14 SC15
+VCC_GFX: SC16 SC17 SC18 SC19
*0.1U/10V/X5R_4

Fro ESD

VIN — C31 *0.1U/10V/X5R_4 — +VCC_CORE
+3V — C145 *0.1U/10V/X5R_4 — +1.05V

EMI

+1.5VSUS: C131 C216 C185 C176 C320 C274 C395
+3V: C175 C490 C2 C325 C200 C359 C1 C405
+5V: C409 C226 C484 C466 C35 C17 C355
2200P/50V/X7R_4
1U/6.3V/X5R_4

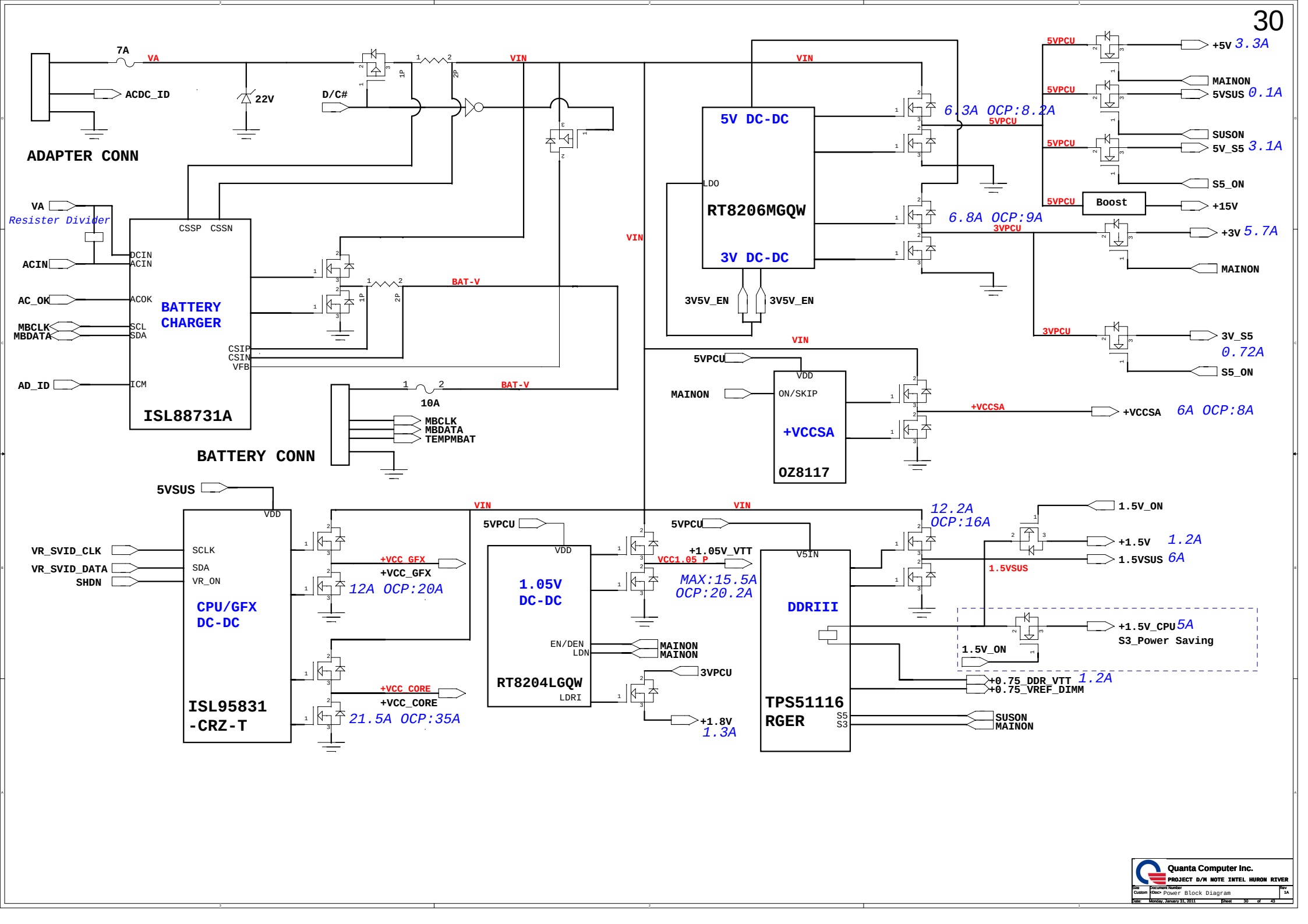
Fro EMI

5VPCU: C276 C277 C278
C276 1000P/50V/X7R_4
C277 1U/6.3V/X5R_4
C278 1U/6.3V/X5R_4

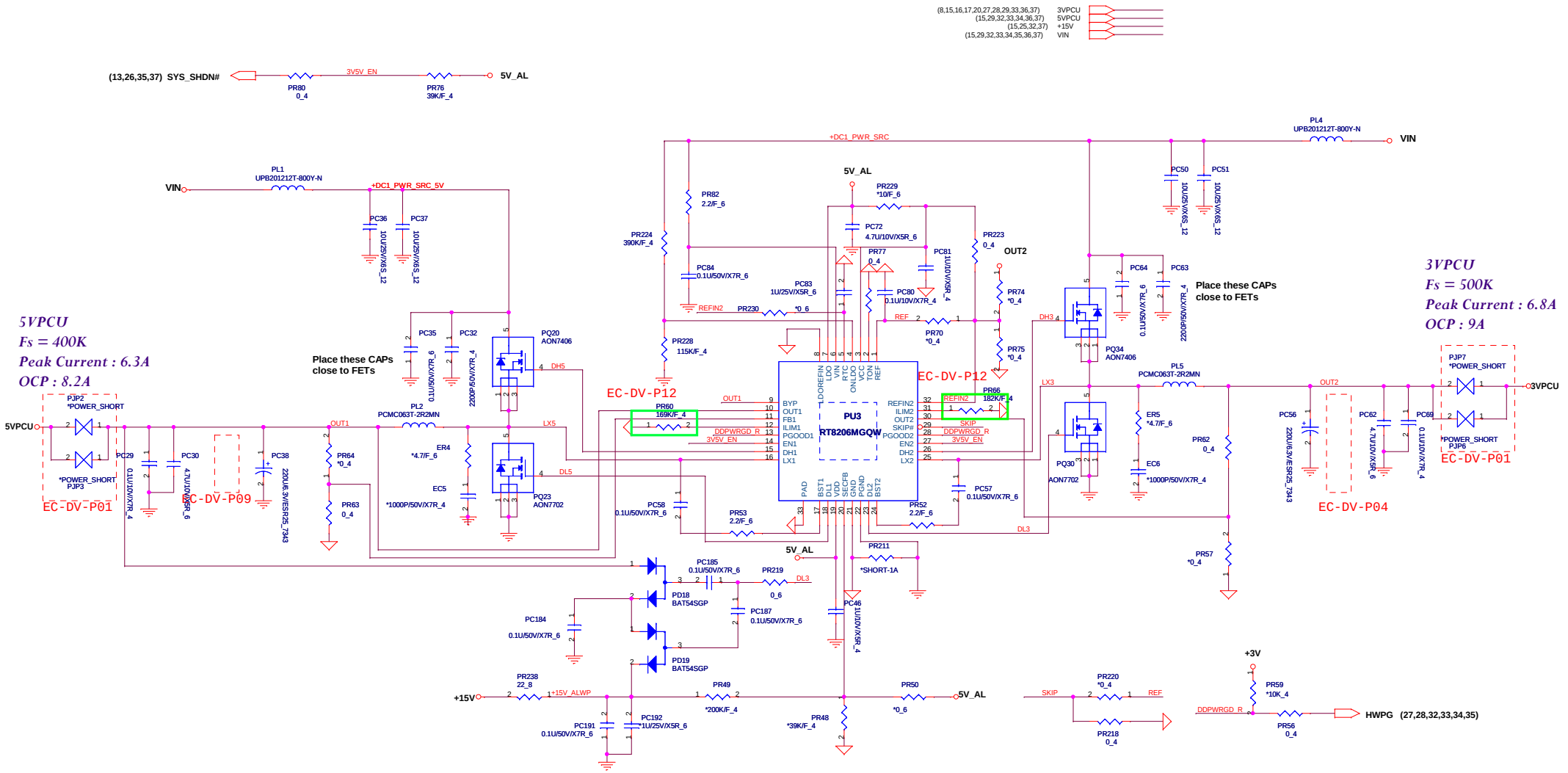
+1.5V_CPU (3,5,32,37)
3VPCU (8,15,16,17,20,27,28,31,33,36,37)
+VCC_GFX (5,35,37)
+3V (3,7,8,9,10,11,13,14,15,16,18,19,21,22,23,24,25,26,27,28,31,32,33,34,35,37)
+5V (7,11,15,16,18,19,24,26,37)
+1.5VSUS (3,11,13,14,32,37)
5VPCU (15,31,32,33,34,36,37)
VIN (15,31,32,33,34,35,36,37)
+VCC_CORE (5,6,35,37)
+1.05V (3,5,7,8,9,11,33,37)

Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	Screw Hole/EMI	1A
Date: Monday, January 31, 2011	Sheet 29 of 43	



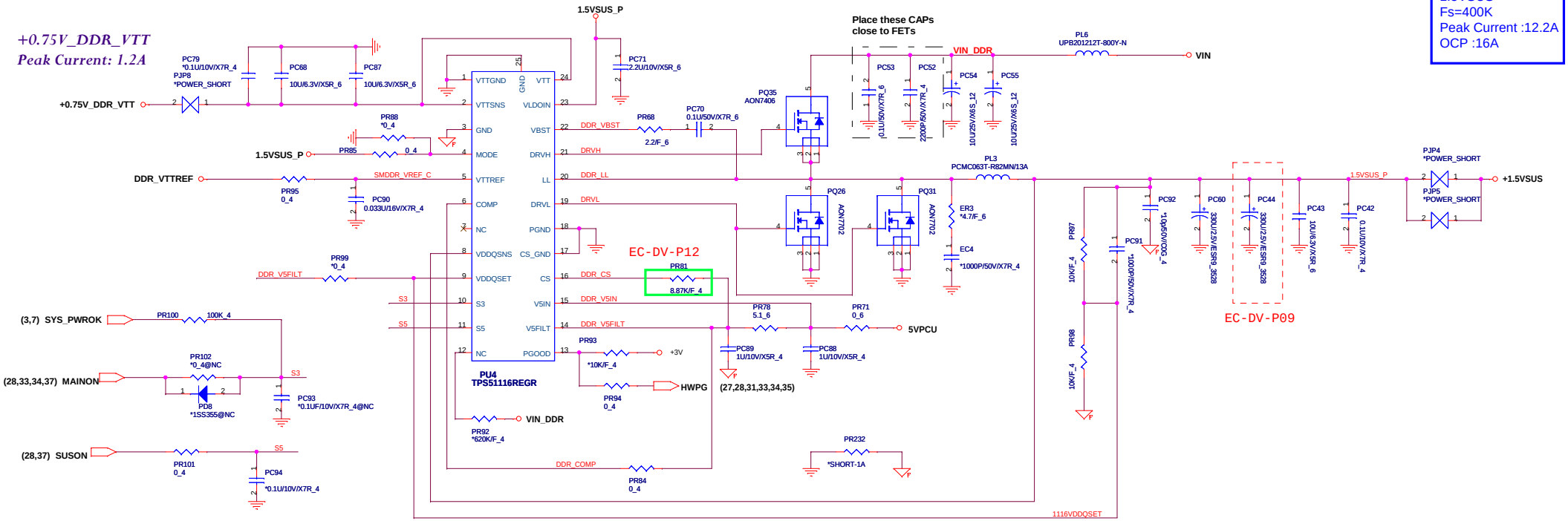
Quanta Computer Inc.
PROJECT D/N NOTE INTEL HURON RIVER
Size: Custom | Document Number: <Doc> Power Block Diagram | Rev: 1A
Date: Monday, January 31, 2011 | Sheet 30 of 43



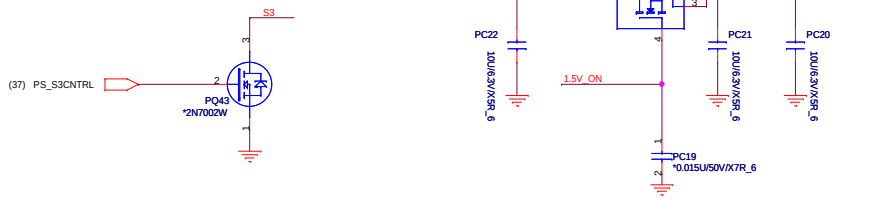
Quanta Computer Inc.			
PROJECT D/M NOTE INTEL HURON RIVER			
Size: Custom	Document Number: <Doc> POWER_3V/5V (RT8206MGQW)		Rev: 1A
Date: Monday, January 31, 2011	Sheet 31 of 43		

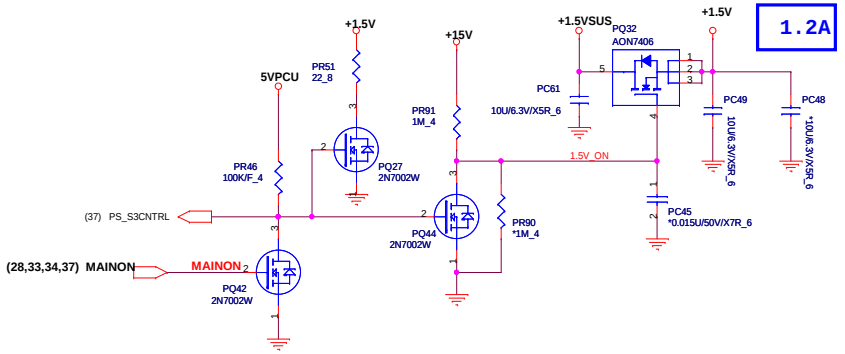
1.5VSUS
Fs=400K
Peak Current :12.2A
OCP :16A

+0.75V_DDR_VTT
Peak Current: 1.2A



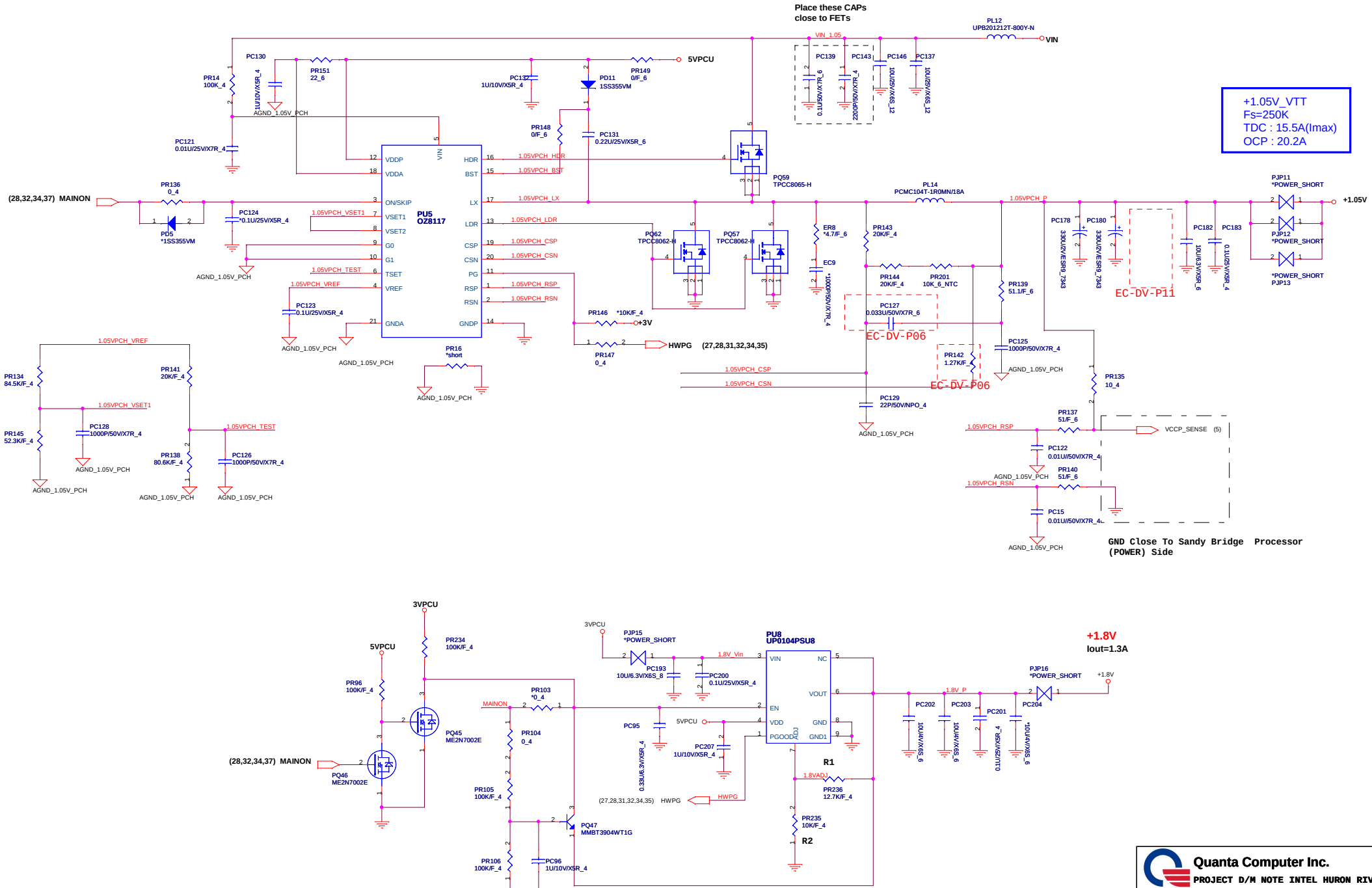
For S3 Power Saving



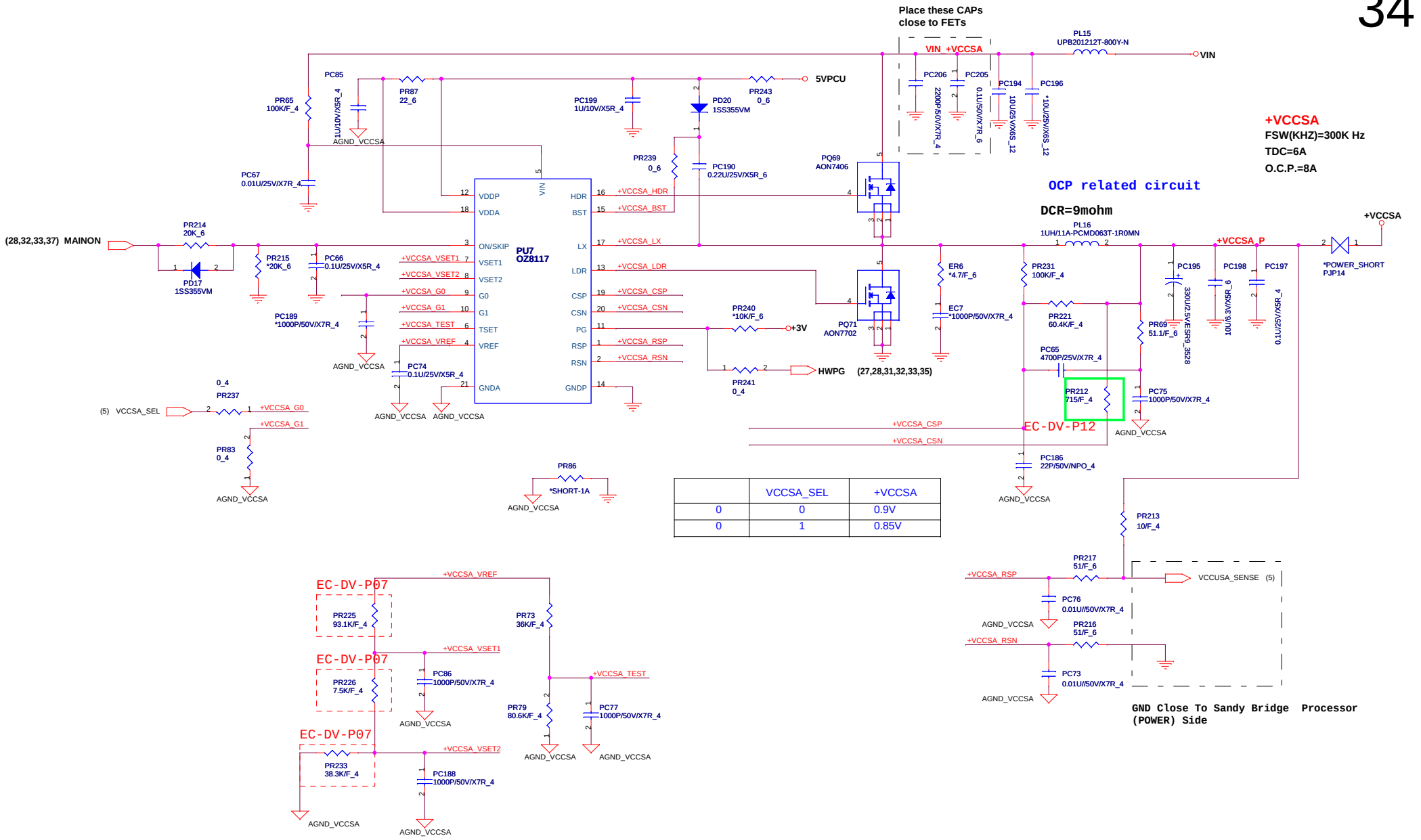


Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
Custom	<Doc> POWER_DDR3 (TPS51116)	1A
Date: Monday, January 31, 2011	Sheet 32 of 43	



Quanta Computer Inc.	
PROJECT D/M NOTE INTEL HURON RIVER	
Size: Custom	Document Number: <Doc> POWER_1.05V&1.8V(OZ8117)
Rev: 1A	
Date: Monday, January 31, 2011	Sheet 33 of 43



	VCCSA_SEL	+VCCSA
0	0	0.9V
0	1	0.85V

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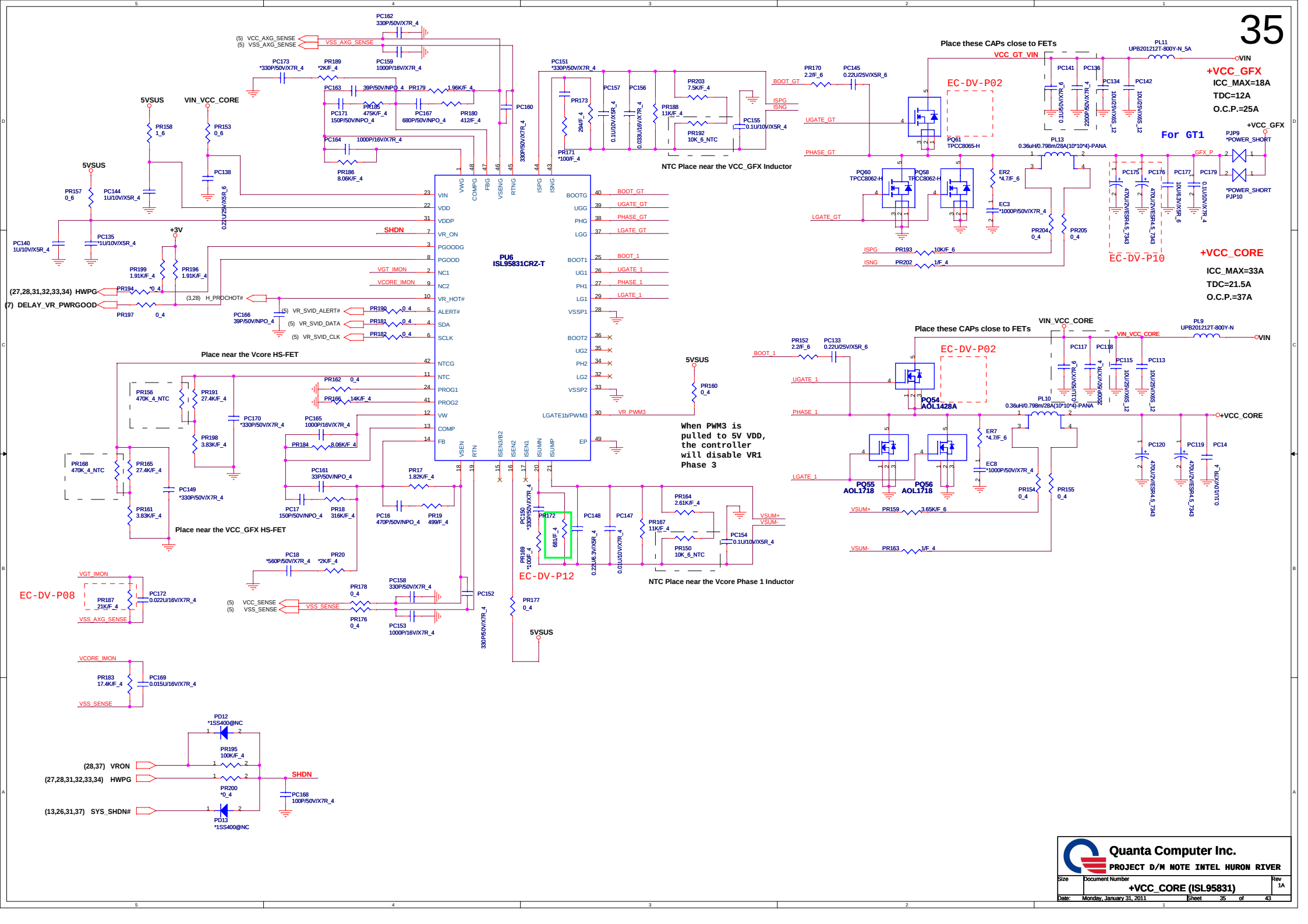
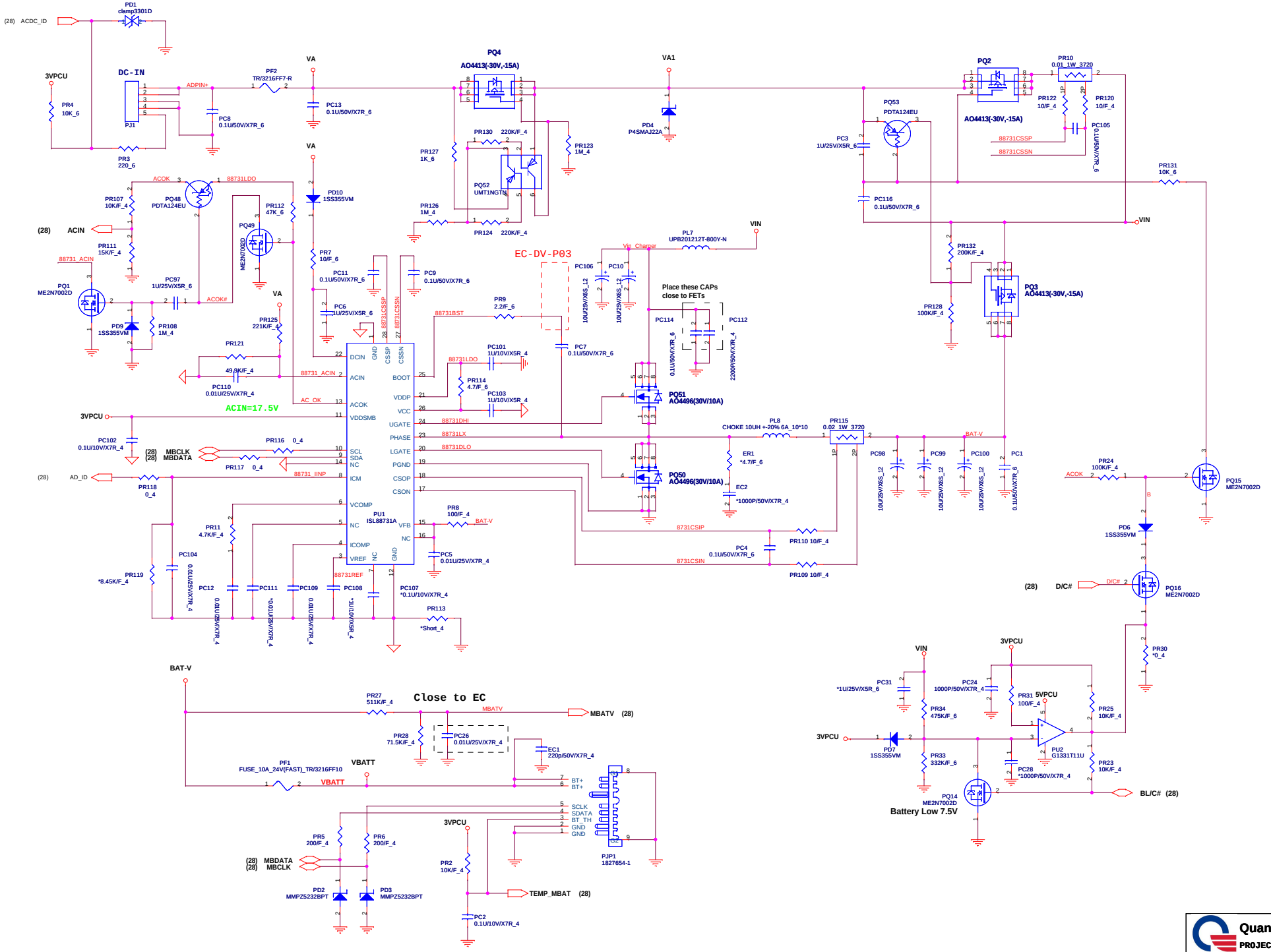
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	VCCSA (OZ8117)	1A
Date: Monday, January 31, 2011	Sheet 34 of 43	



Quanta Computer Inc.			
PROJECT D/M NOTE INTEL HURON RIVER			
Size	Document Number		Rev
	+VCC_CORE (ISL95831)		1A
Date: Monday, January 31, 2011		Sheet 35 of 43	



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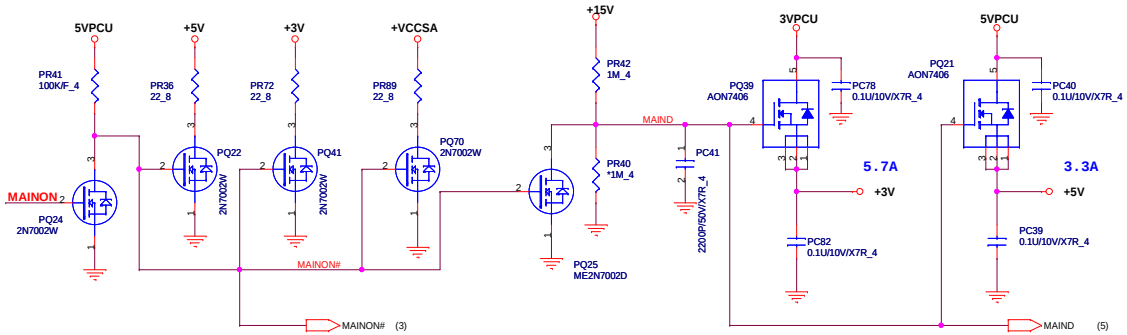
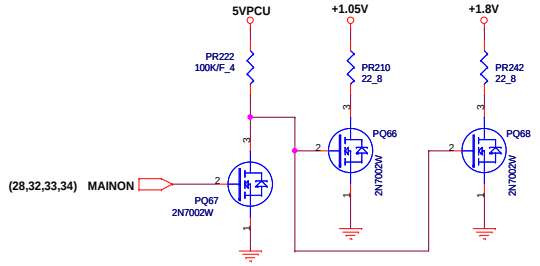
PROJECT D/M NOTE INTEL HURON RIVER

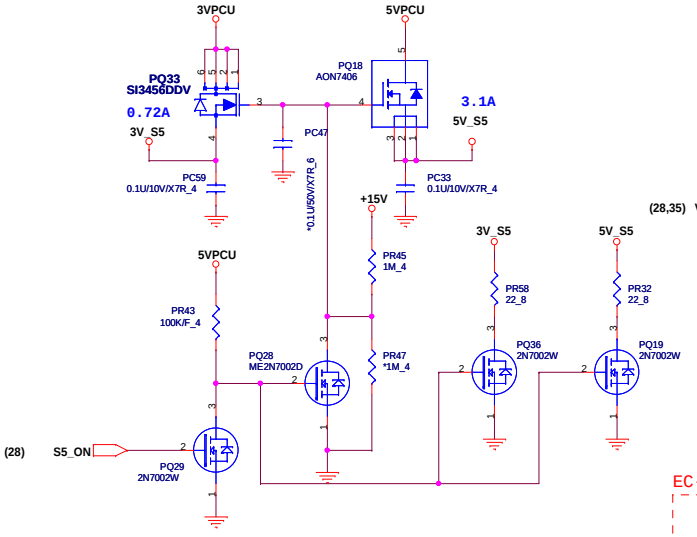
Size	Document Number	Rev
Custom	<Doc> POWER_Charger (ISL88731A)	1A
Date: Monday, January 31, 2011	Sheet 36 of 43	

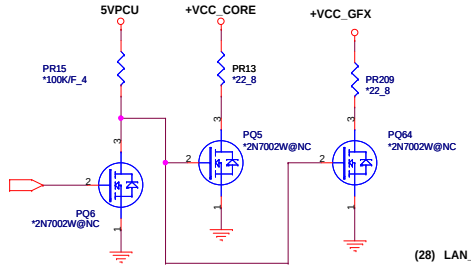
+3.3V, +5V



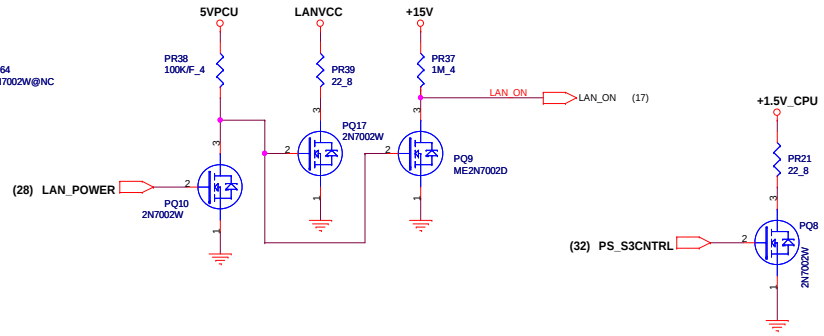


3V_S5, 5V_S5

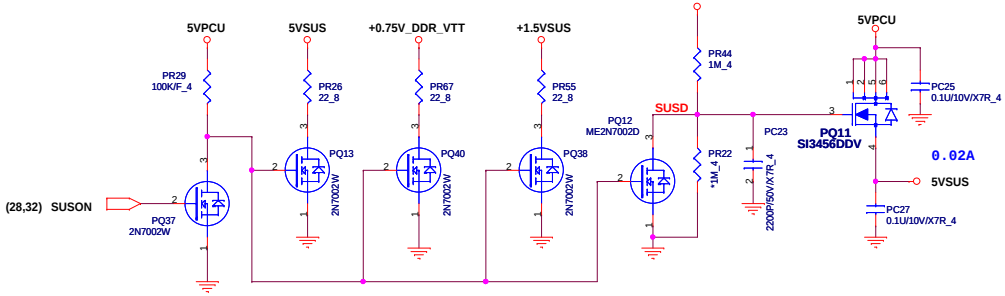


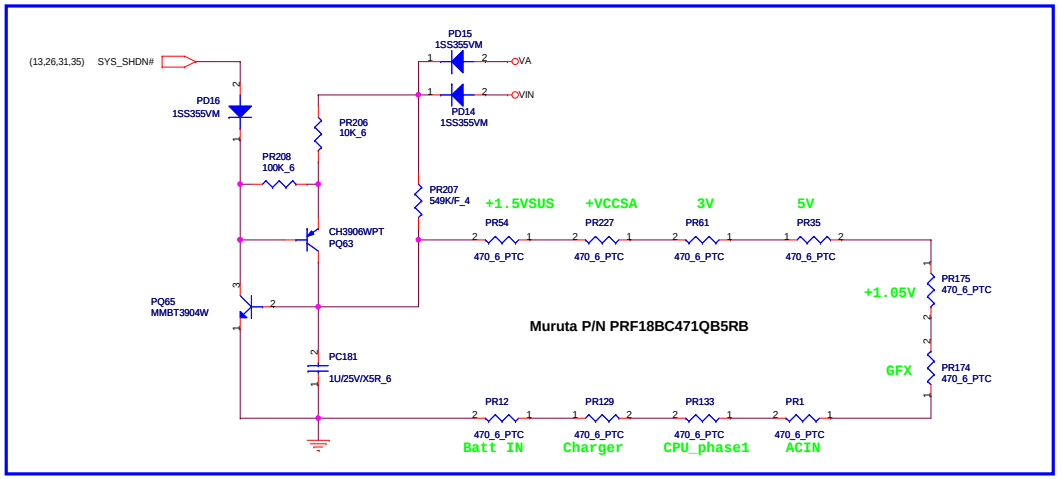


LANVCC



EC-DV-P05 5VSUS

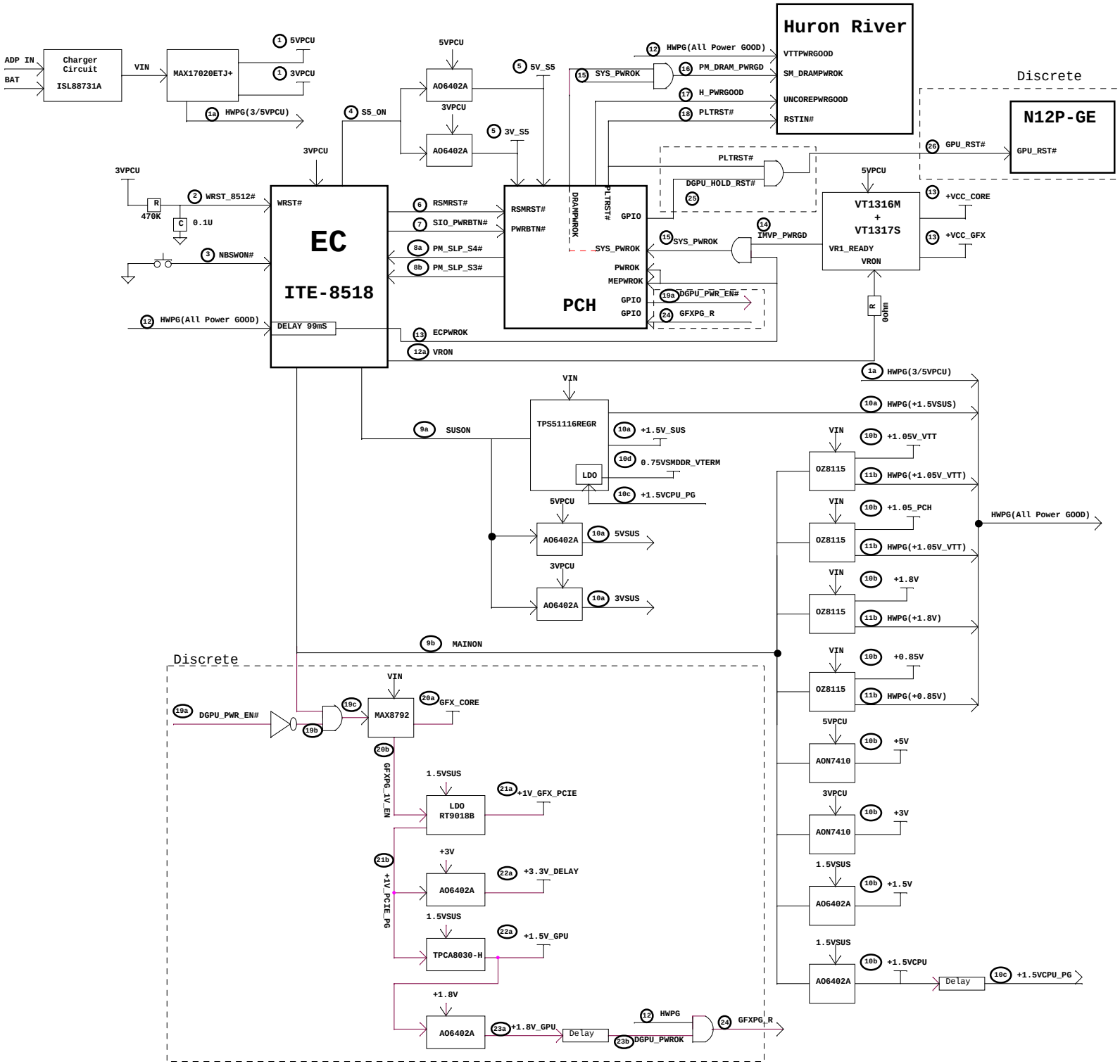




Quanta Computer Inc.

PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	Discharge/+3V_MAINON	1A
Date: Monday, January 31, 2011	Sheet 37 of 43	



Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
Custom	<Doc>	1A

Date: Monday, January 31, 2011 Sheet 38 of 43

D-NOTE SKU TABLE

Location					

M-NOTE SKU TABLE

Location					Page

Revision History

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
A1A		DV	Initial release	2010/12/03	2010/12/03

Schematic Value Explanation Description :

RESISTOR

Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005)					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K_6	5%		0603 (1608)				POP	1K ohm 5% SMD 0603 package and POP
1K_8	5%			0805 (2125)			POP	1K ohm 5% SMD 0805 package and POP
1K_12	5%				1206 (3216)		POP	1K ohm 5% SMD 1206 package and POP
1K_1210	5%					1210 (3225)	POP	1K ohm 5% SMD 1210 package and POP

CAPACITOR

Value	Voltage	Material	6				*	Description
*0.1U/10V/X5R_4	10V	X5R	0402 (1005)				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7R_6	25V	X7R	0603 (1608)				POP	0.1UF 25V X7R SMD 0603 package POP

DM NOTE Schematic EC Tracking Record DV (for DV)XXXX. XX, 2010

EC #	Page	Date	Part Affected	Description
EC-DV-01	16	2010/11/17	U2000 and related schematic	Remove level shift and related schematic
EC-DV-02	05	2010/11/17	R11256	Follow Intel power delivery to add 10m ohm pull-up at VDDCQ
EC-DV-03	29	2010/11/17	HOLE10	Change HOLE10 footprint
EC-DV-04	20	2010/11/17	CN23	Change USB BTB connector to FFC type
EC-DV-05	17	2010/11/17	C11242	Change C11242 from 10P to 1000P and series with ESD part for ISN
EC-DV-06	28	2010/11/18	EC Pin#98, R11264, R11265	G-sensor ID select
EC-DV-07	17	2010/11/18	RV19	Change RV19 pop for ESD solution
EC-DV-08	18	2010/11/19	R916, R11216, R11266	Delete R916 and R11216, because AGND connect with DGND in GND layer
EC-DV-09	07	2010/11/22	RV8	Reserse for ESD
EC-DV-10	17	2010/11/22	RV17, RV18, C11243, C11246	Reserse for ESD
EC-DV-11	17	2010/11/22	U11005, U11006	Pin#5 connect LANVCC for ESD's request
EC-DV-12	18	2010/11/22	R281	reference CX20371-21Z CRB schematic to delete it
EC-DV-13	18	2010/11/22	R330	reference CX20371-21Z CRB schematic to delete it
EC-DV-14	18	2010/11/22	C11247	reference CX20371-21Z CRB schematic to add it
EC-DV-15	18	2010/11/22	R1283, C7373	reference Conexant combo jack latest CRB schematic to delete C7373 and change R1283 to 4.7K
EC-DV-16	18	2010/11/22	R11269	reference Conexant combo jack latest CRB schematic to add it
EC-DV-17	18	2010/11/22	R1290, C11248	reference Conexant combo jack latest CRB schematic to add C11248 and change R1290 to 200
EC-DV-18	18	2010/11/22	R11267, R11268	EMI request
EC-DV-19	20,28	2010/11/23	U47.6, U47.7, U15.79	EC can combine USB charger IC CB[0:1] pin to one signal CB[0]
EC-DV-20	24	2010/11/23	R209, R201	Change to 4.7K
EC-DV-21	24	2010/11/22	RV9, RV10	Reserse for ESD
EC-DV-22	24	2010/11/22	RV11, RV12	Reserse for ESD
EC-DV-23	27	2010/11/22	RV13, RV14, RV15	Reserse for ESD
EC-DV-24	27	2010/11/22	RV16	Reserse for ESD
EC-DV-25	24	2010/11/29	CN9	CN9 PIN8 connect to EC
EC-DV-26	27	2010/11/29	C12000	Add C12000 for Audio vendor suggestion

EC #	Page	Date	Part Affected	Description
EC-DV-P01	31	11/09	PJP2, PJP3, PJP6, PJP7	Add short pad for DV test
EC-DV-P02	35	11/09	PQ23, PQ27	Remove reserved component
EC-DV-P03	36	11/09	PD13	Remove reserved component
EC-DV-P04	31	11/15	PC18	Remove reserved component
EC-DV-P05	37	11/17	PR235, PQ74, PQ70, PC201, PC202	Remove 3VSUS reserved component
EC-DV-P06	33	11/30	PR142, PC127	O2 FAE recommend change value for DC/DC 1.05V
EC-DV-P07	34	11/30	PR225, PR226, PR233	O2 FAE recommend change value for DC/DC VCCSA
EC-DV-P08	35	11/30	PR187	Intersil FAE recommend change value for DC/DC VCC_CORE
EC-DV-P09	31	1/10	PC34	Remove reserved component
EC-DV-P10	35	1/10	PC175, PC176	Intersil FAE recommend change value for DC/DC VCC_GFX
EC-DV-P11	33	1/10	PC174	Remove component for cost down
EC-DV-P12	31	1/10	PR60, PR66	Change for OCP setting
	32	1/10	PR81	
	34	1/10	PR212	
	35	1/10	PR172	

Quanta Computer Inc.
PROJECT D/M NOTE INTEL HURON RIVER
Size | Document Number: EC Tracking Record DV | Rev: 1A
Date: Monday, January 31, 2011 Sheet 42 of 43

DM NOTE Schematic EC Tracking Record DV (for SIT)01.26.2011

EC #	Page	Date	Part Affected	Description
EC-SIT-1	3,5,7,8,9,10, 11,15,17,18, 19,20,22,23, 24,25,27,28	11/01/26	R365,R353,R11,R66,R362,R8,R351,R219,R220, R236,R497,R284,R278,R207,R256,R468,R391, R392,R396,R387,R243,R193,R126,R277,R125, R410,R412,R407,R405,R226,R415,R411,R144, R190,R163,R241,R191,R130,R123,R398,R425, R89,R417,R428,R408,R399,R166,R414,R17, R170,R156,R301,R375,R43,R429,R426,R108, R107,R145,R146,R480,R476,R420,R138,R492, R491,R122,R120,R217,R218,R247,R248,R275, R95	Change some 0 ohm to short Pad
EC-SIT-2	8	11/01/19	U30	Change BT_DET# from U30.E40 GPIO54 to U30.V14 GPIO21
EC-SIT-3	8	11/01/25	C560,C564	vender advise to change from 15p to 18p, let XTAL more accuracy
EC-SIT-4	13	11/01/19	C575	Add 33p capacitor for RF requirement
EC-SIT-5	15	11/01/19	C520,C521,C522,C523,C524,C525,C526,C527	Reserve 0 ohm resistor for RF requirement
EC-SIT-6	16	11/01/24	C20,C5,C3,C16,C14,C4	Change 10P to 5.6P for signal quality
EC-SIT-7	18	11/01/19	C576,C577	Add 33p capacitor near IC for RF requirement
EC-SIT-8	20	11/01/19	RV2, RV3, RV17, U35	Replace RV2,RV3,RV17 to U35 for ESD requirement
EC-SIT-9	24	11/01/19	R512,R513,R514,R515,R516,R517,R518,R519	Reserve 0 ohm resistor for EMI requirement
EC-SIT-10	27	11/01/20	LED2,LED3,R313,R299,RV14,RV12,RV13,R314, R315,R311	Delete Battery and Suspend LED related schematic
EC-SIT-11	27	11/01/26	R15,R14,C32,C30	Delete Power Button LED related schematic