


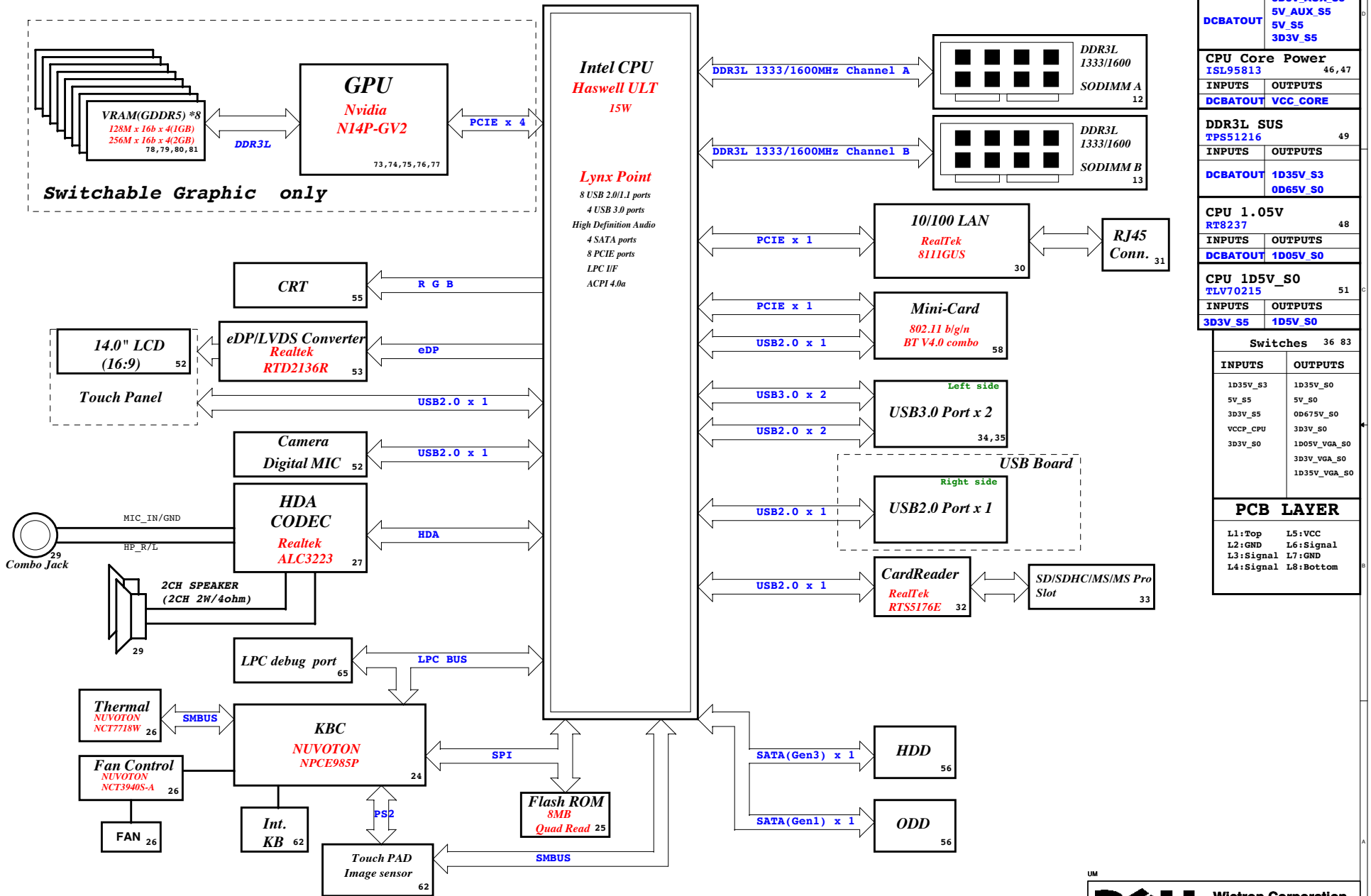
Latitude3000 Schematic Haswell-ULT

2013-3-15
REV : X00

DY : None Installed
UMA: UMA only installed
OPS: DISCRTE OPTIMUS installed

UM		
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Cover Page		
Size A3	Document Number Latitude300 Haswell	Rev X00
Date: Friday, March 15, 2013	Sheet 1	of 104


Latitude3000 Block Diagram



CHARGER		44
BQ24717		
INPUTS	OUTPUTS	
AD+	DCBATOUT	
BT+		
SYSTEM DC/DC		45
TPS51225		
INPUTS	OUTPUTS	
DCBATOUT	3D3V_AUX_S5 5V_AUX_S5 5V_S5 3D3V_S5	
CPU Core Power		46,47
ISL95813		
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	
DDR3L SUS		49
TPS51216		
INPUTS	OUTPUTS	
DCBATOUT	1D35V_S3 0D65V_S0	
CPU 1.05V		48
RT8237		
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0	
CPU 1D5V_S0		51
TLV70215		
INPUTS	OUTPUTS	
3D3V_S5	1D5V_S0	
Switches 36 83		
INPUTS	OUTPUTS	
1D35V_S3	1D35V_S0	
5V_S5	5V_S0	
3D3V_S5	0D675V_S0	
VCCP_CPU	3D3V_S0	
3D3V_S0	1D05V_VGA_S0	
	3D3V_VGA_S0	
	1D35V_VGA_S0	
PCB LAYER		
L1:Top	L5:VCC	
L2:GND	L6:Signal	
L3:Signal	L7:GND	
L4:Signal	L8:Bottom	

(Blanking)

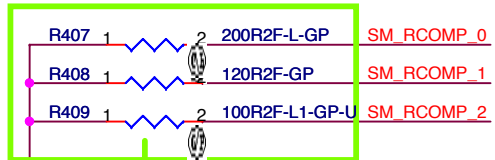
UM

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
(Reserved)		
Size	Document Number	Rev
A3	Latitude300 Haswell	X00
Date: Friday, March 15, 2013	Sheet 3	of 104

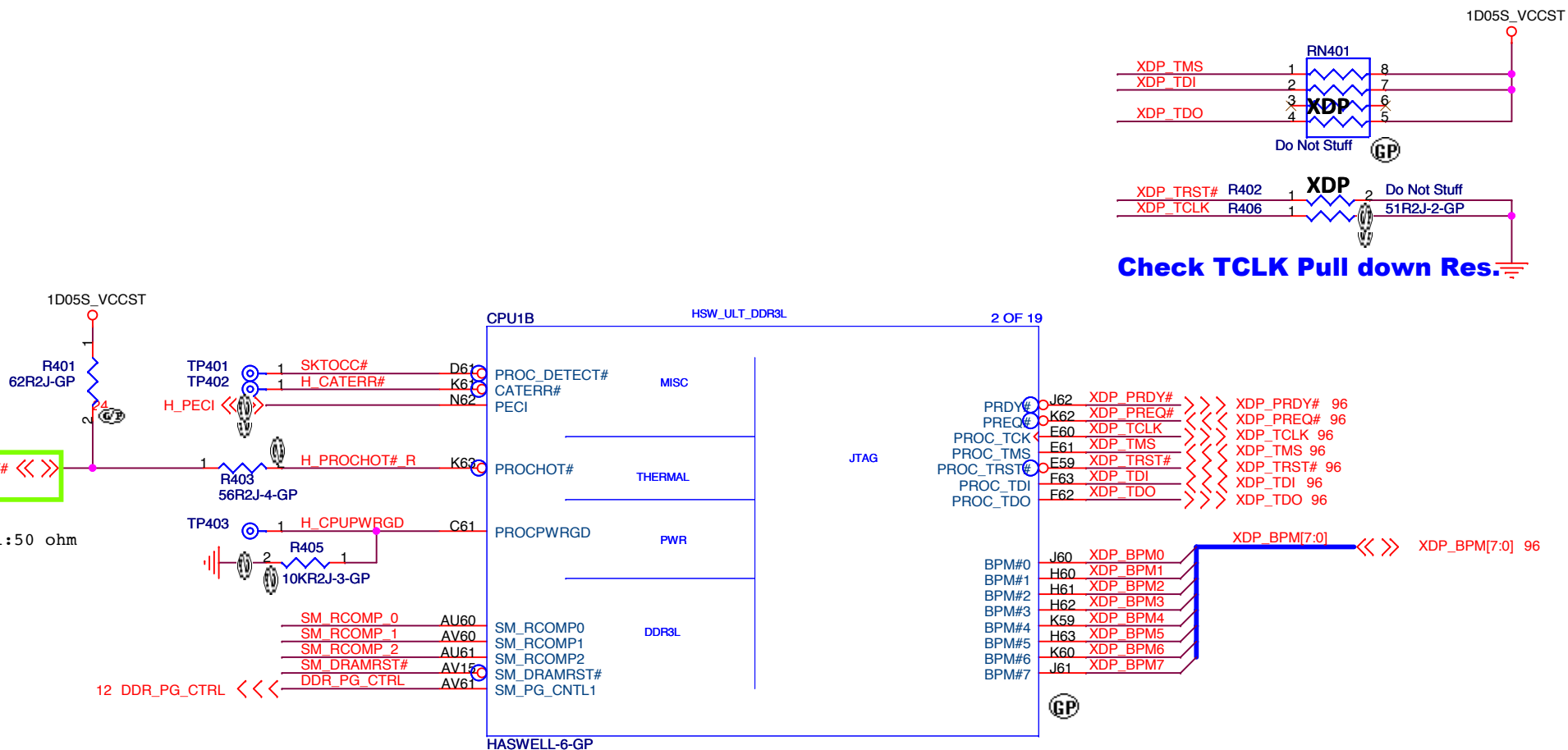
SSID = CPU

24,42,44,46 H_PROCHOT# <<<>>

Layout Note:
Impedance control:50 ohm



Layout Note:
Design Guideline:
SM_RCOMP keep routing length less than 500 mils.



Check TCLK Pull down Res.

Layout Note:
Place close to DIMM

UM

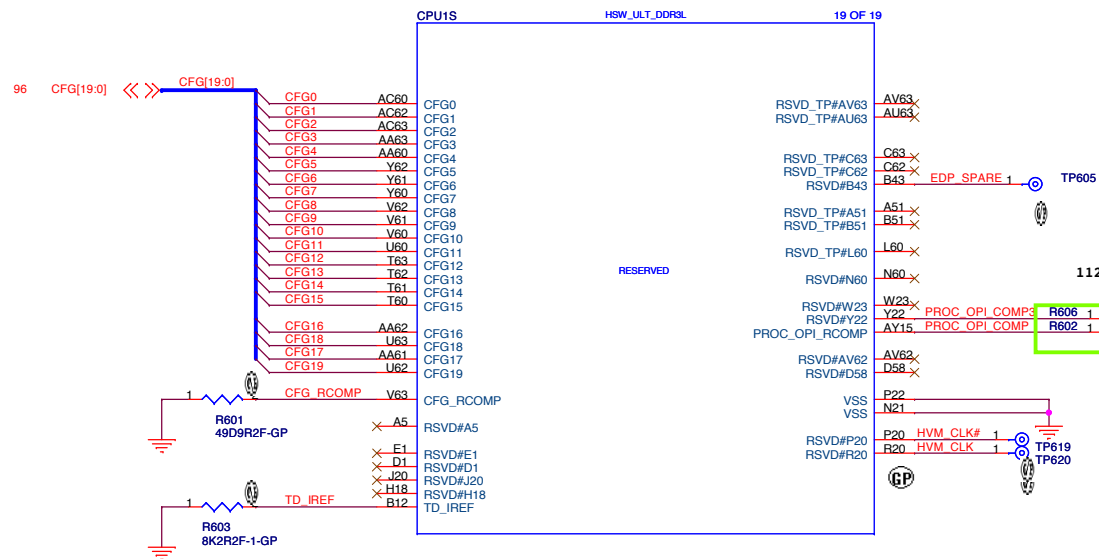
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
CPU (THERMAL/MISC/PM)

Size A4	Document Number Latitude300 Haswell	Rev X00
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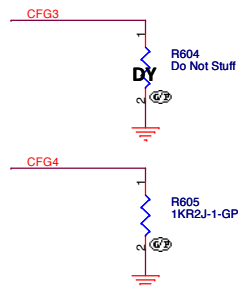
Date: Friday, March 15, 2013 Sheet 4 of 104

SSID = CPU



Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12-15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG[3]	0 : ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR
	1 : DISABLED

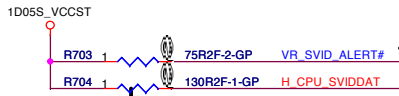
DISPLAY PORT PRESENCE STRAP	
CFG[4]	0 : ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT
	1 : DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT

UM



Title		
CPU (RESERVED)		
Size	Document Number	Rev
A3	Latitude300 Haswell	X00
Date:	Friday, March 15, 2013	Sheet 6 of 104

SSID = CPU

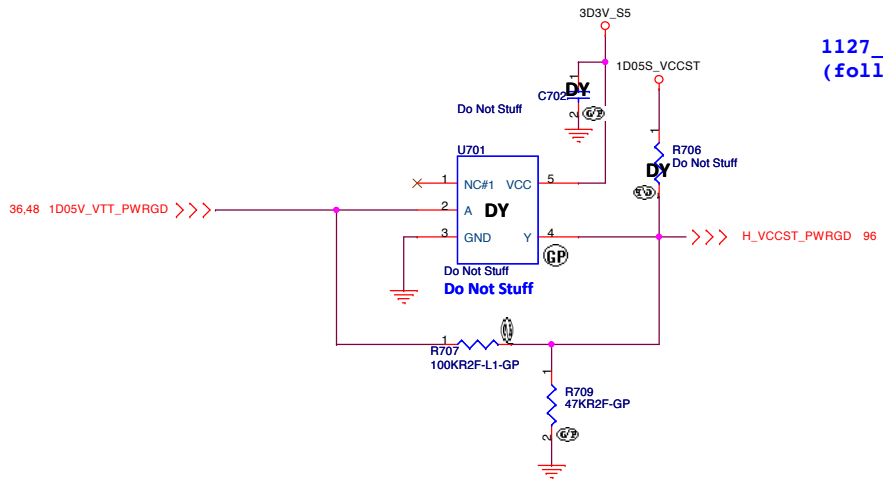


1127 130R change to 110R
1203 110R change to 130R

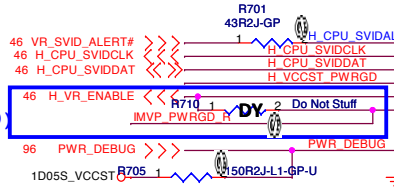
1127 Change net name of R703.2
from VR_SVID_ALERT# to
H_CPU_SVIDALRT#

Layout Note:

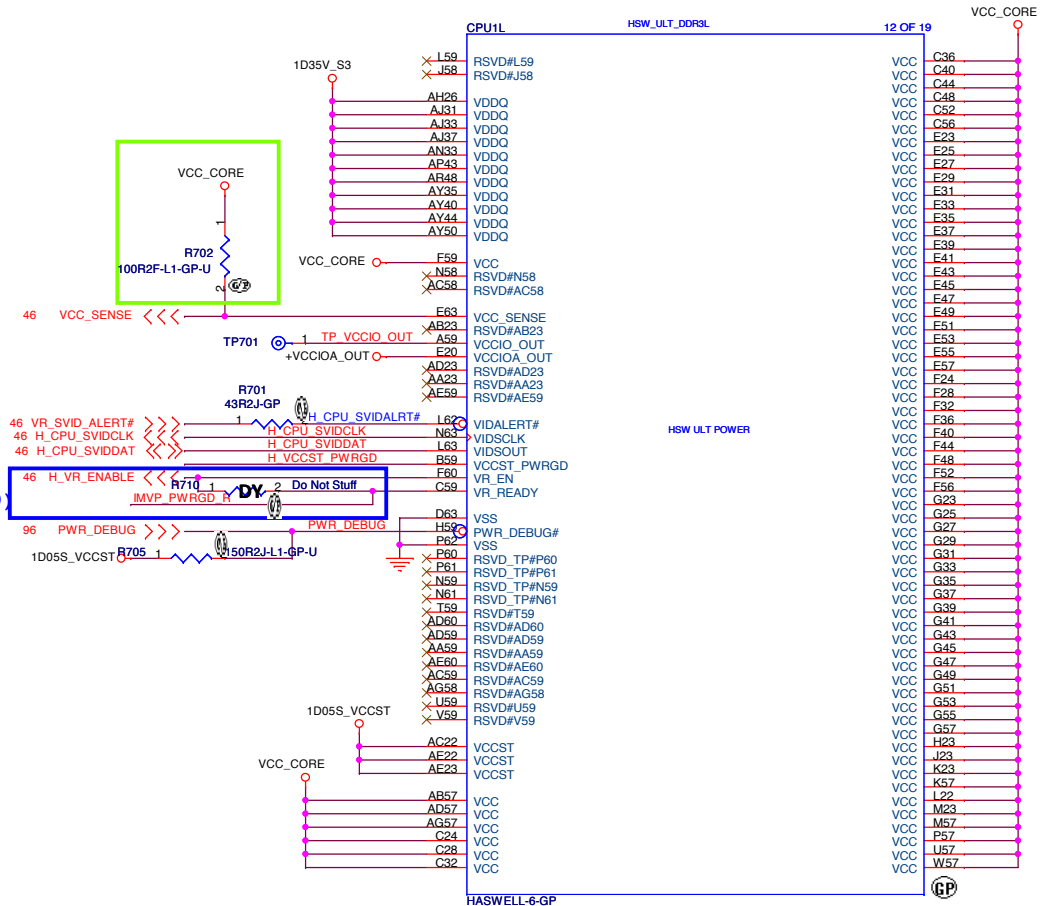
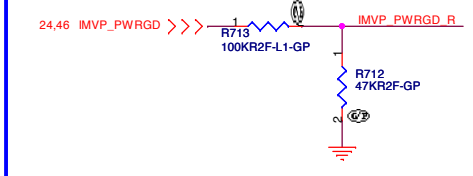
1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Lwnlth match<25mml



1127 modify
(follow EA40)



1205 Add



UM

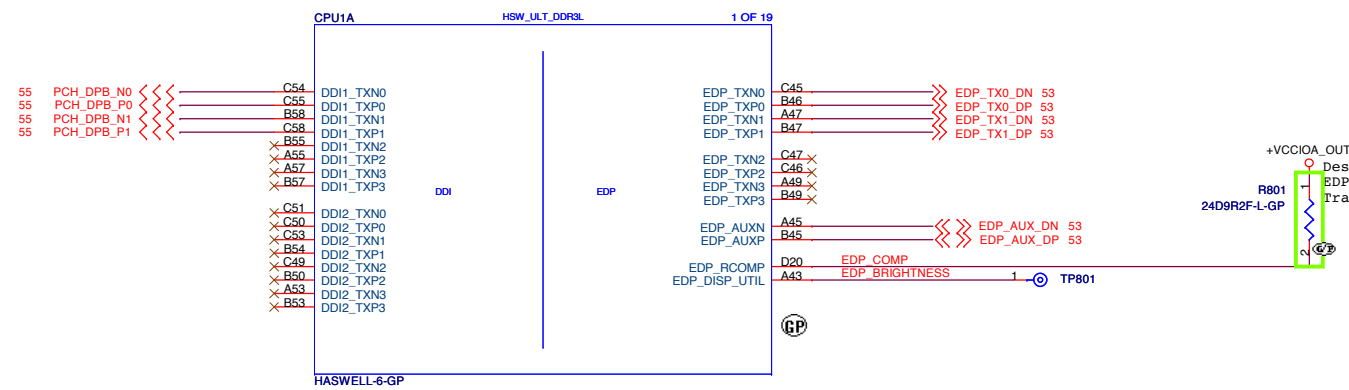
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (VCC CORE)**

Size A3	Document Number	Rev
	Latitude300 Haswell	X00
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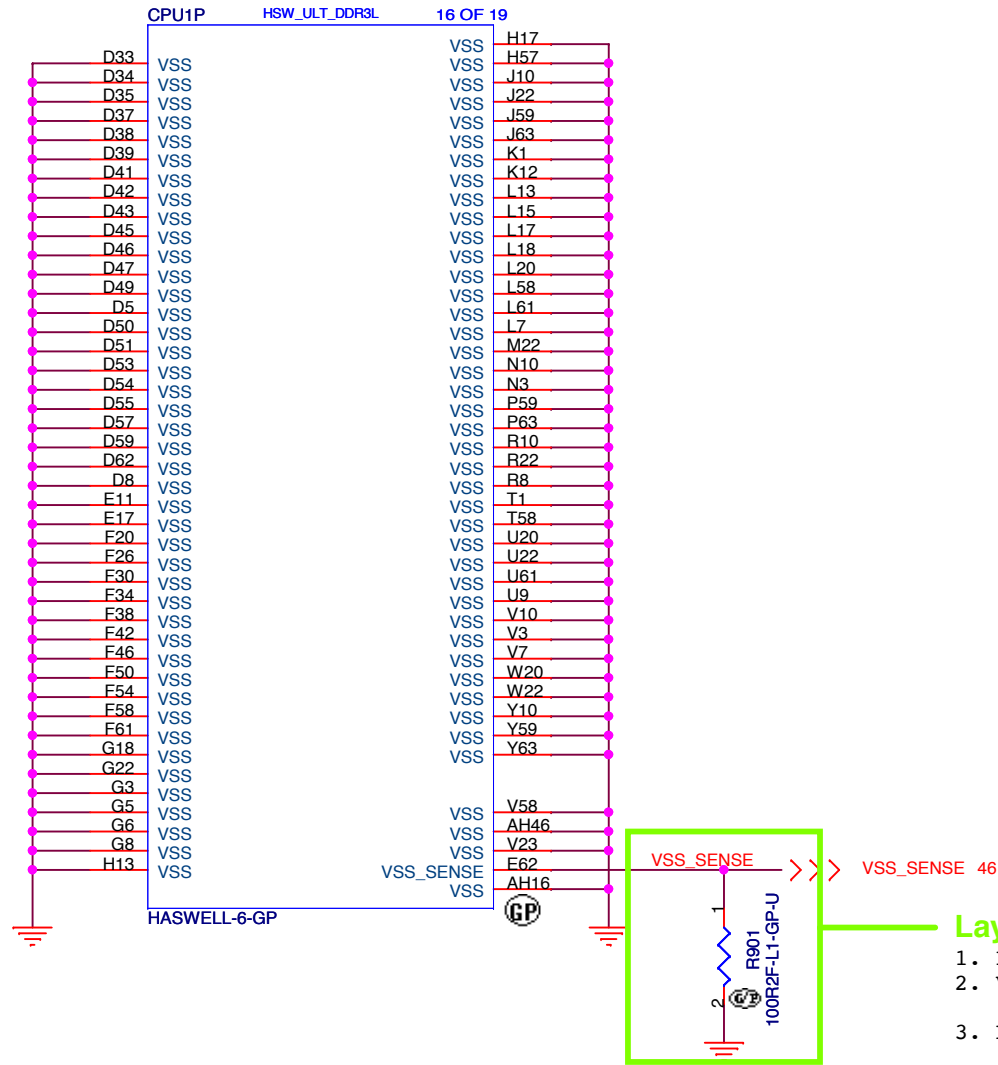
SSID = CPU

CRT



Design Guideline:
EDP_COMP keep routing length max 100 mils.
Trace Width:20 mils.


SSID = CPU



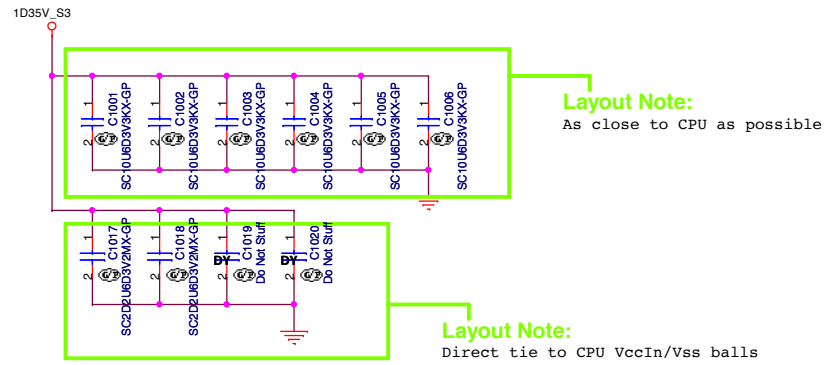
Layout Note:

1. Place close to CPU
2. VCC_SENSE/ VSS_SENSE impedance=50 ohm
3. Lwngth match<25mil

UM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <h2 style="text-align: center;">CPU (VSS)</h2>	
Size A4	Document Number <h2 style="text-align: center;">Latitude300 Haswell</h2>	Rev X00	
Date: Friday, March 15, 2013		Sheet 9 of 104	

SSID = CPU



UM

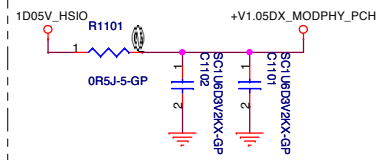
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Reserved**

Size: A3	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet: 10	of: 104

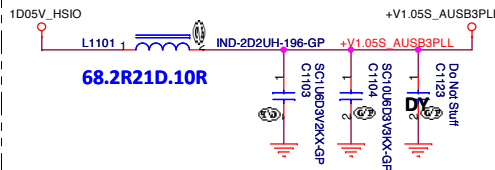
MAX: 1.92A

1.838A



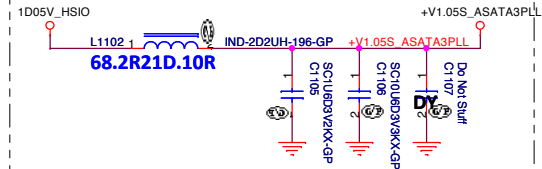
CAP need close to pin K9 L10

41mA



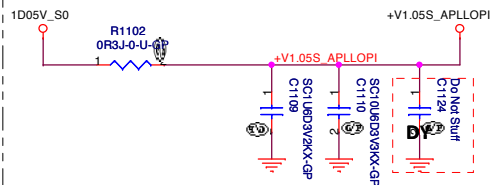
CAP need close to pin B18

42mA



CAP need close to pin B11

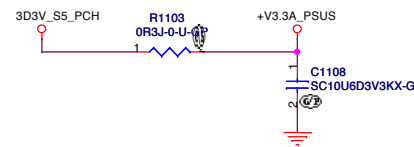
57mA



CAP need close to pin AA21

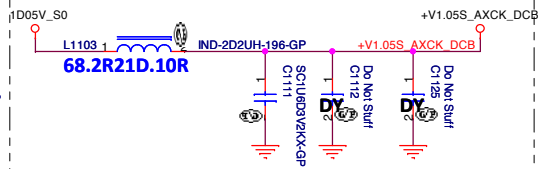
1205 Add

62mA



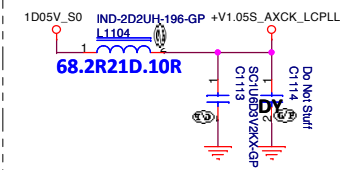
CAP need close to pin AC9

200mA



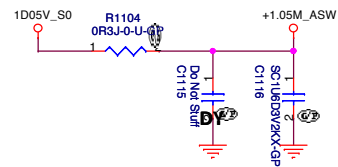
CAP need close to pin J18

31mA



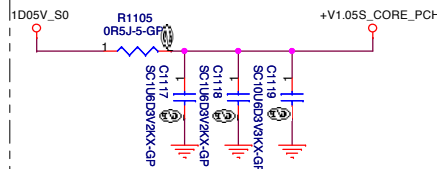
CAP need close to pin A20

658mA



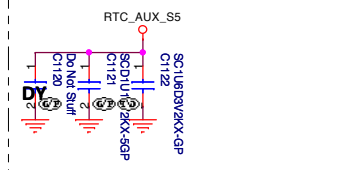
CAP need close to pin AE9

1.632A



CAP need close to pin AE8 J11

1mA



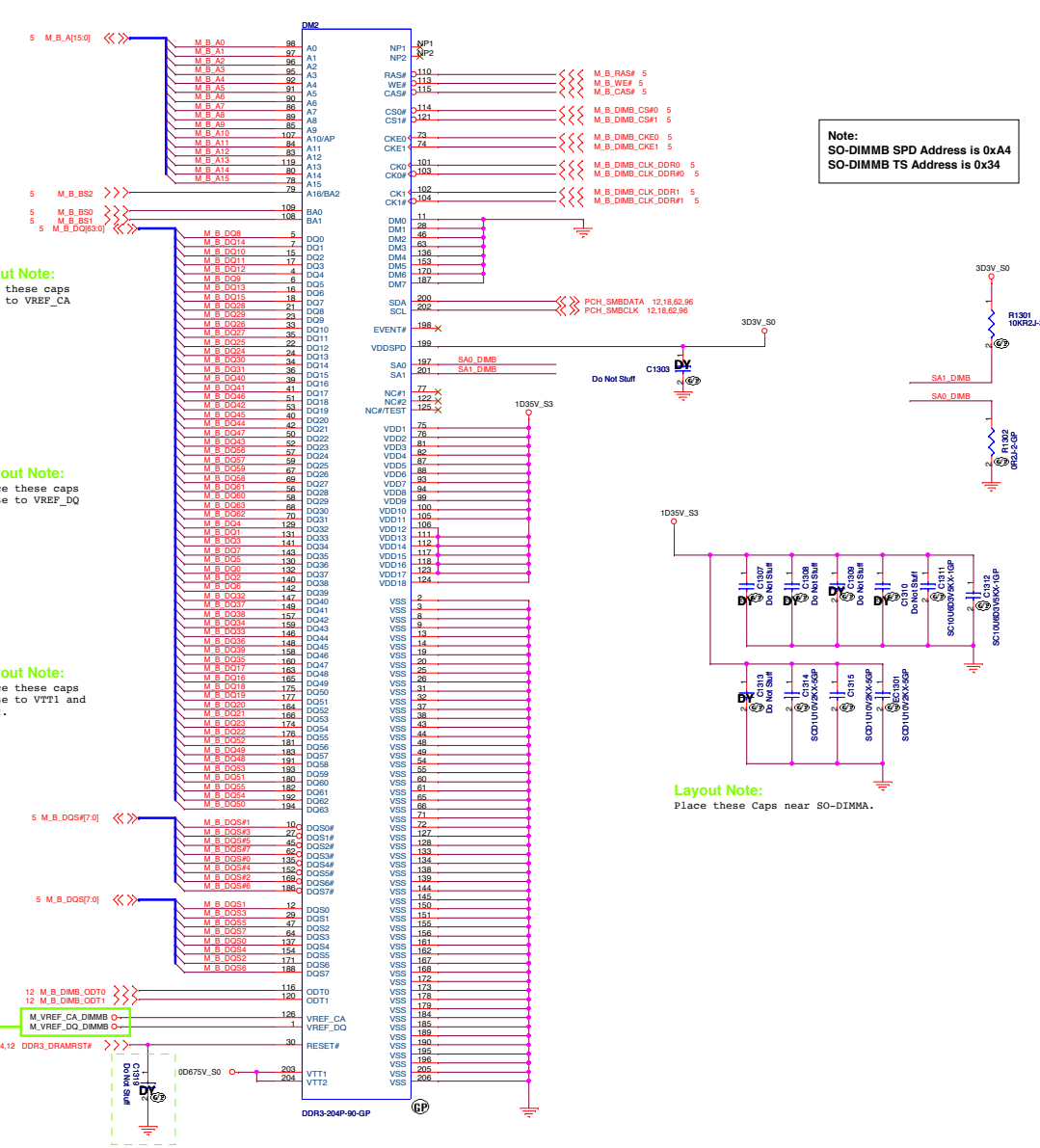
CAP need close to pin AG10

UM



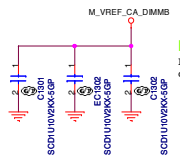
Title		
Reserved		
Size	Document Number	Rev
A3	Latitude300 Haswell	X00
Date:	Friday, March 15, 2013	Sheet 11 of 104

SSID = MEMORY

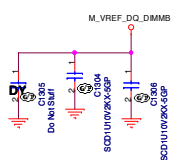


Note:
SO-DIMM SPD Address is 0x44
SO-DIMM TS Address is 0x34

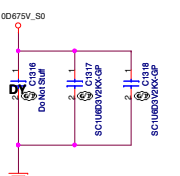
Layout Note:
Place these caps close to VREF_CA



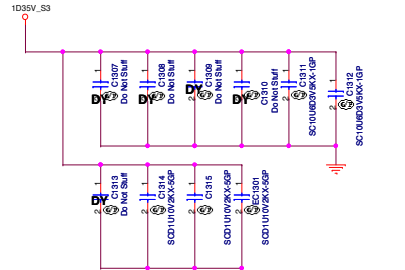
Layout Note:
Place these caps close to VREF_DQ



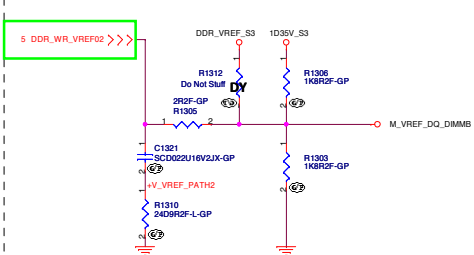
Layout Note:
Place these caps close to VTT1 and VTT2.



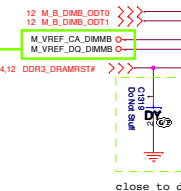
Layout Note:
Place these Caps near SO-DIMMA.

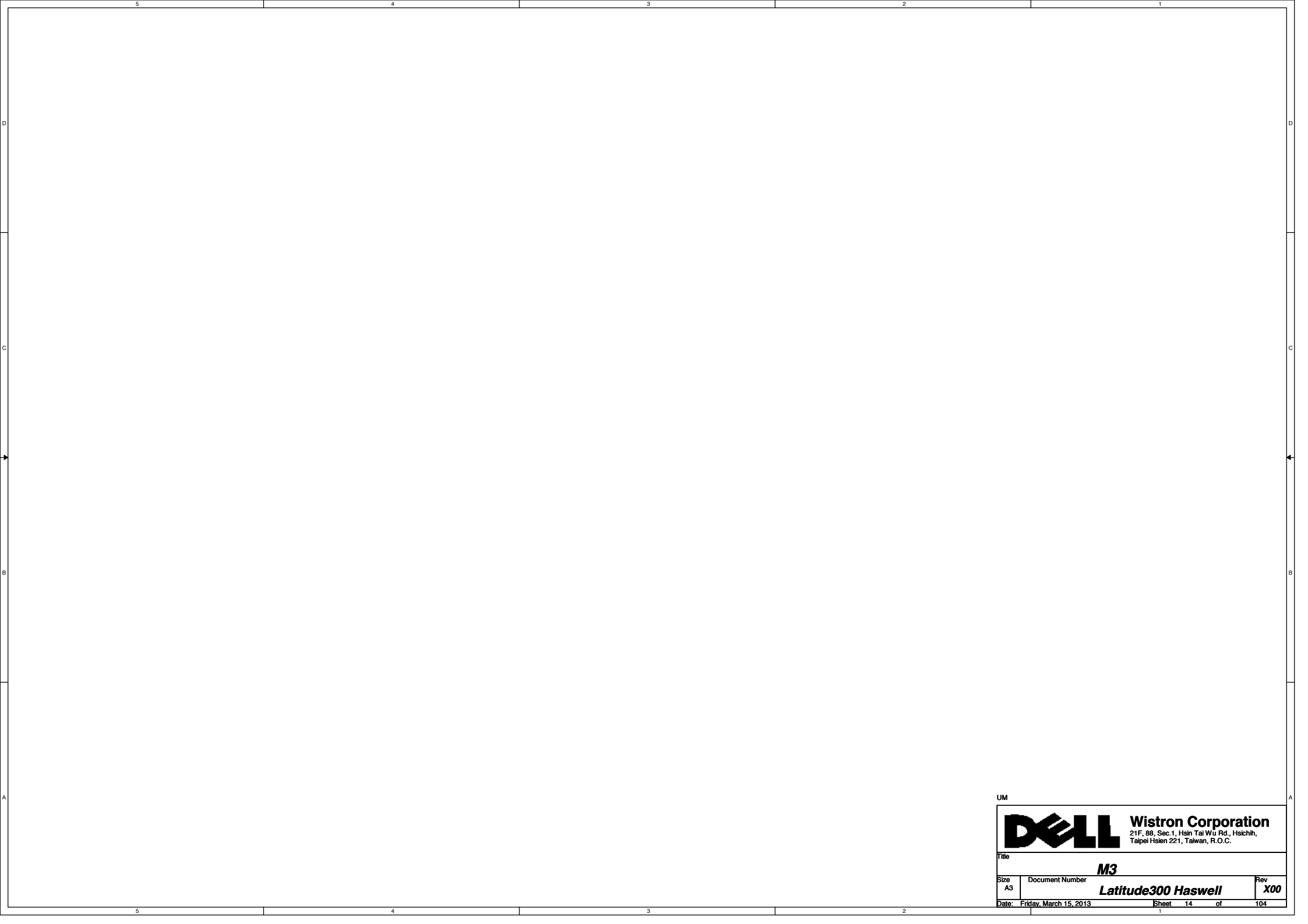


Layout Note:
Place Close SO-DIMMA.



Layout Note:
All VREF traces should have width=20mil; spacing=20 mil



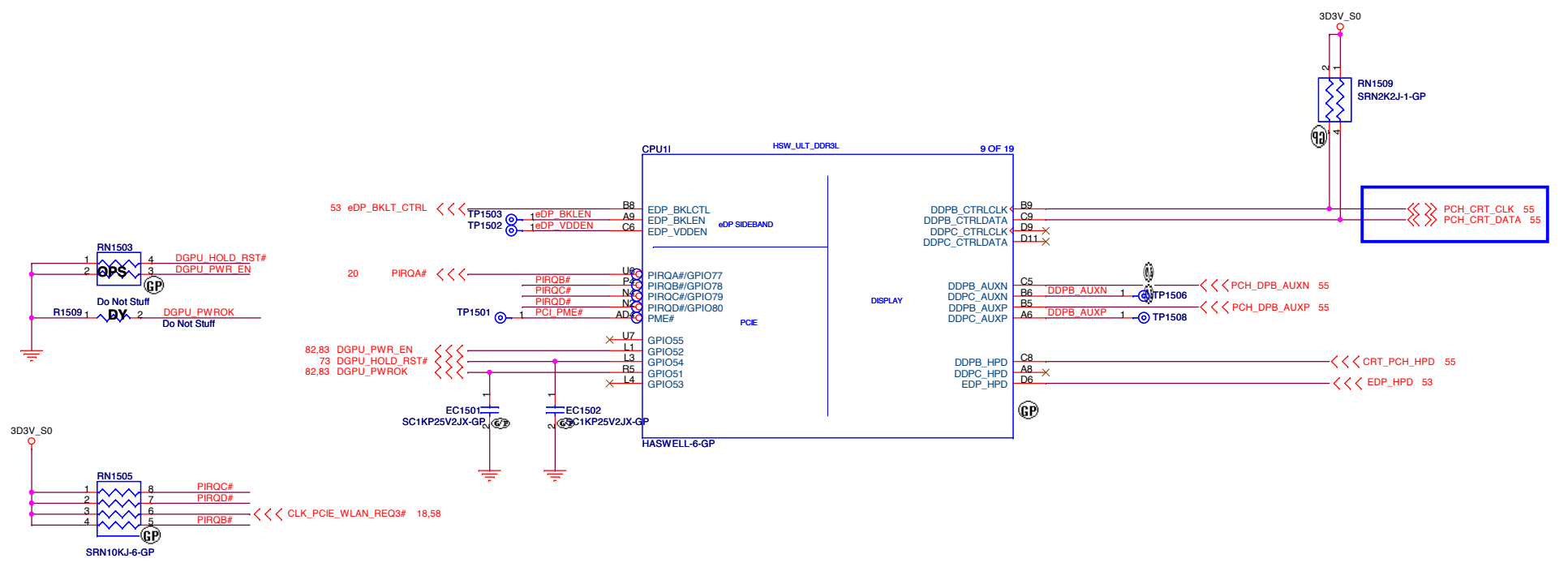


UM



Title		
M3		
Size	Document Number	Rev
A3	Latitude300 Haswell	X00
Date: Friday, March 15, 2013	Sheet 14 of 104	

SSID = CPU



UM

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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (EDP/GPIO/DDI)**

Size: A3	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet: 15	of: 104

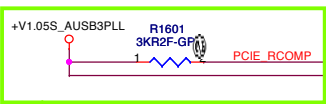
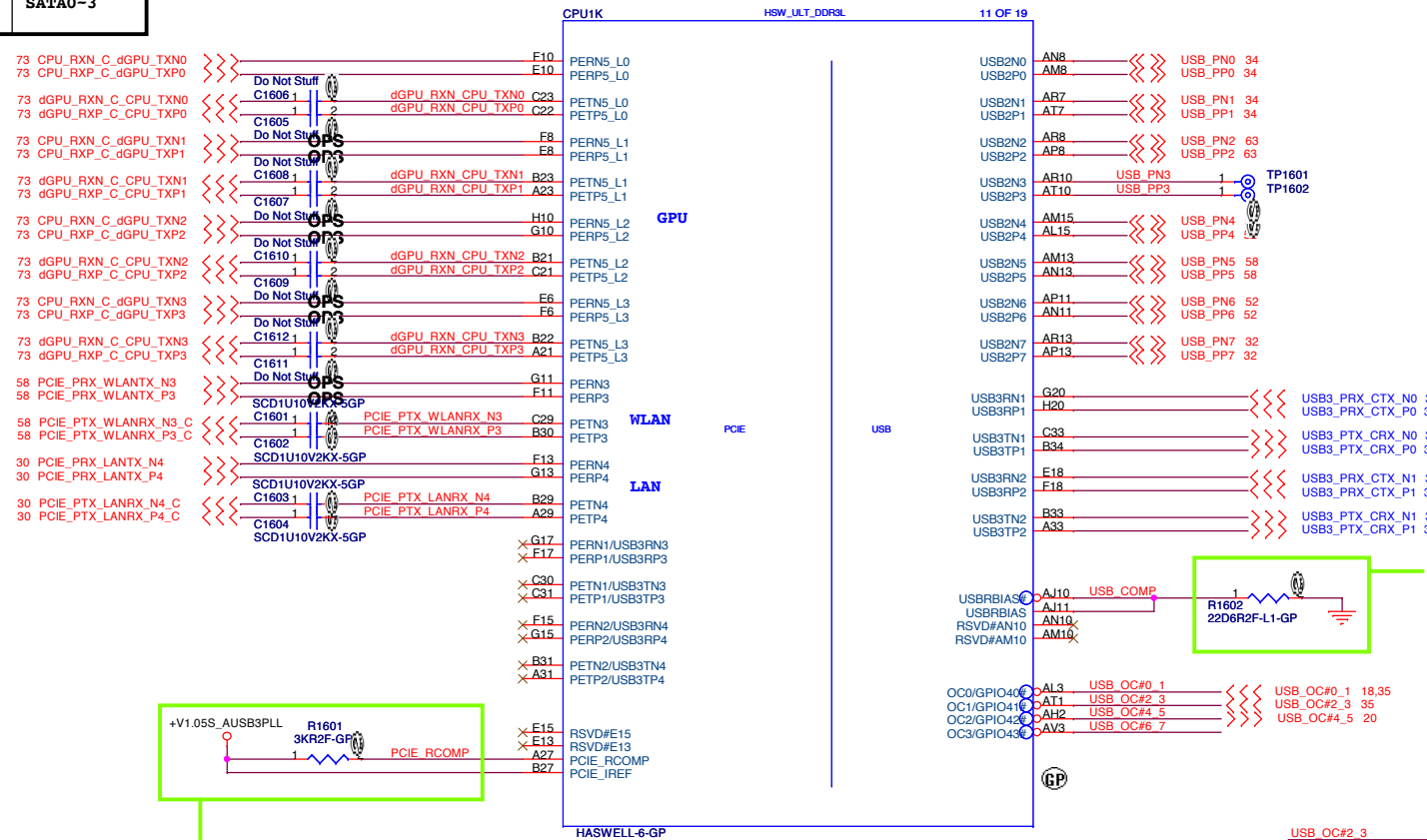
SSID = PCH

PCIe Table

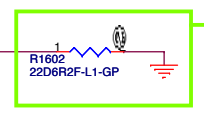
Port	Device	Share BUS
1	TBD	USB3.0_3
2	TBD	USB3.0_4
3	WLAN	
4	LAN	
5 (4lane)	GPU	
6 (4lane)	TBD	SATA0-3

USB 2.0 Table

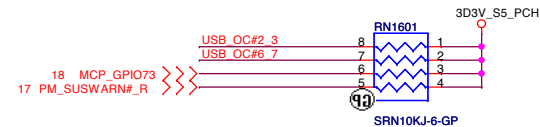
Pair	Device
0	USB3.0 port1
1	USB3.0 Port2
2	USB2.0 Port3
3	TBD
4	CAMERA
5	WLAN
6	Touch Panel
7	Card Reader



Layout Note:
 1. PCIe_RCOMP/ PCIE_IREF trace width=12-15mil
 2. Isolation Spacing: 12mil
 3. Total trace length<500mil



Layout Note:
 1. USB_COMP using 50 ohm single-ended impedance
 2. Isolation Spacing :15mil
 3. Total trace length<500mil



UM

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 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

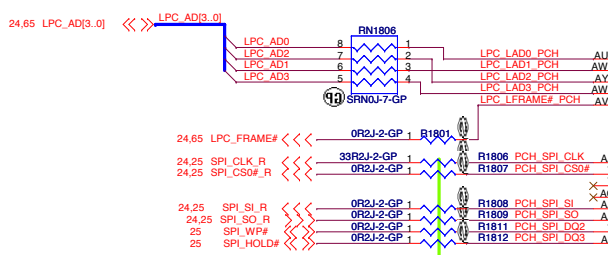
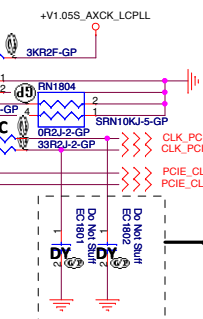
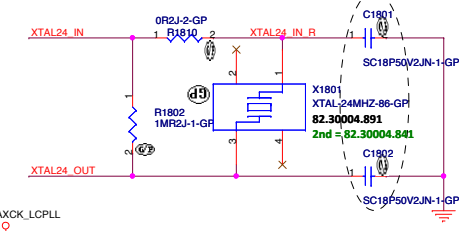
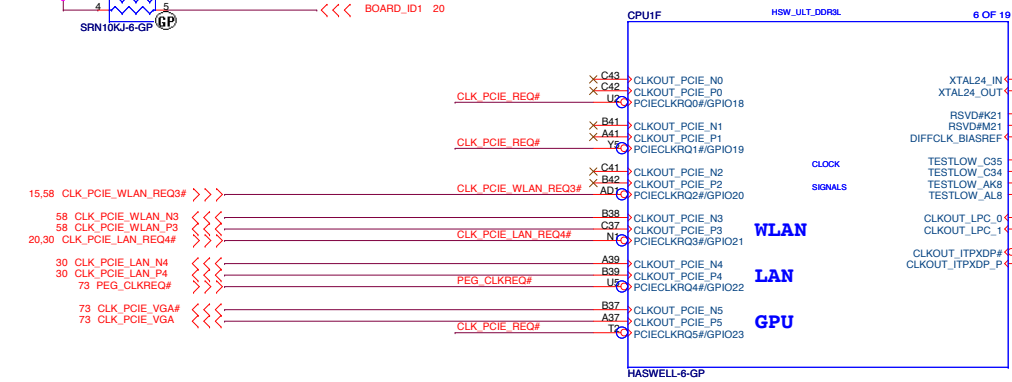
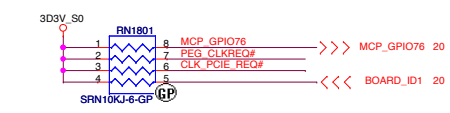
Title: **PCH (PCIe/USB)**

Size A3 | Document Number: **Latitude300 Haswell** | Rev: **X00**

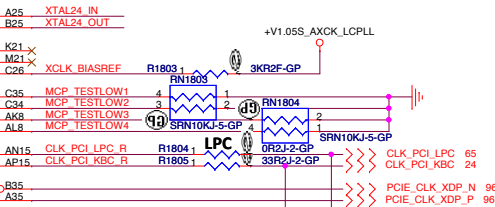
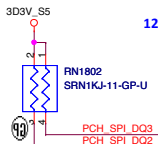
Date: Friday, March 15, 2013 | Sheet 16 of 104

SSID = PCH

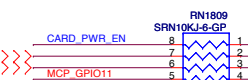
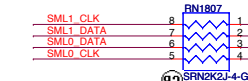
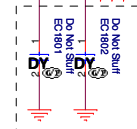
X01 3/7 Change value from test report



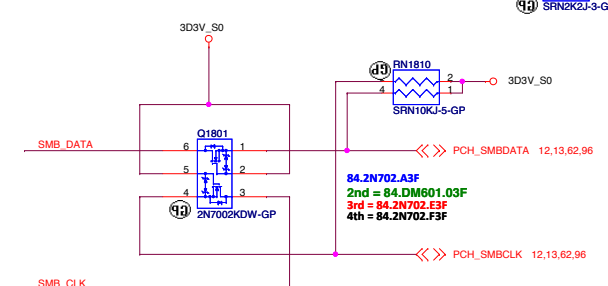
1203 R1806 change to 33R



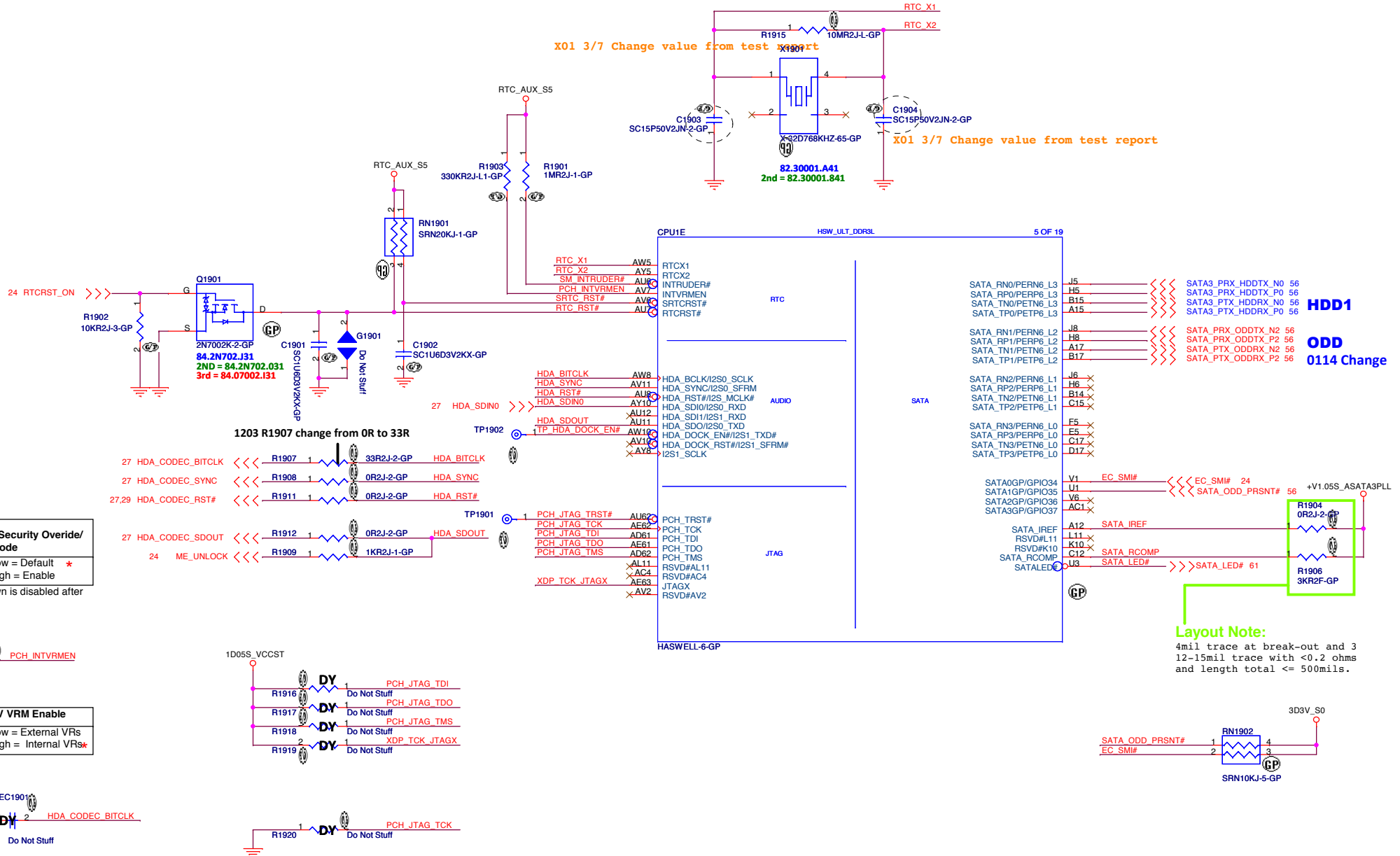
1128 Add EC1801 EC1802(DY)



16.35 USB_OC#0_1
20.24 EC_SCI#



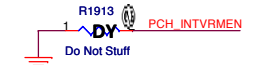
SSID = CPU



**Flash Descriptor Security Override/
Intel ME Debug Mode**

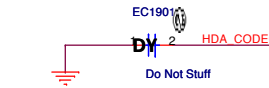
HDA_SDOUT	Low = Default * High = Enable
-----------	----------------------------------

The internal pull-down is disabled after PLTRST# deasserts



Integrated SUS 1V VRM Enable

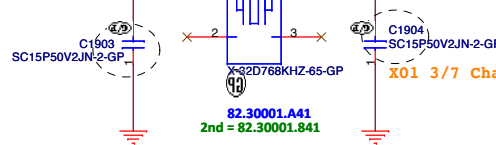
INTVRMEN	Low = External VRs High = Internal VRs*
----------	--



1203 R1907 change from 0R to 33R



X01 3/7 Change value from test report



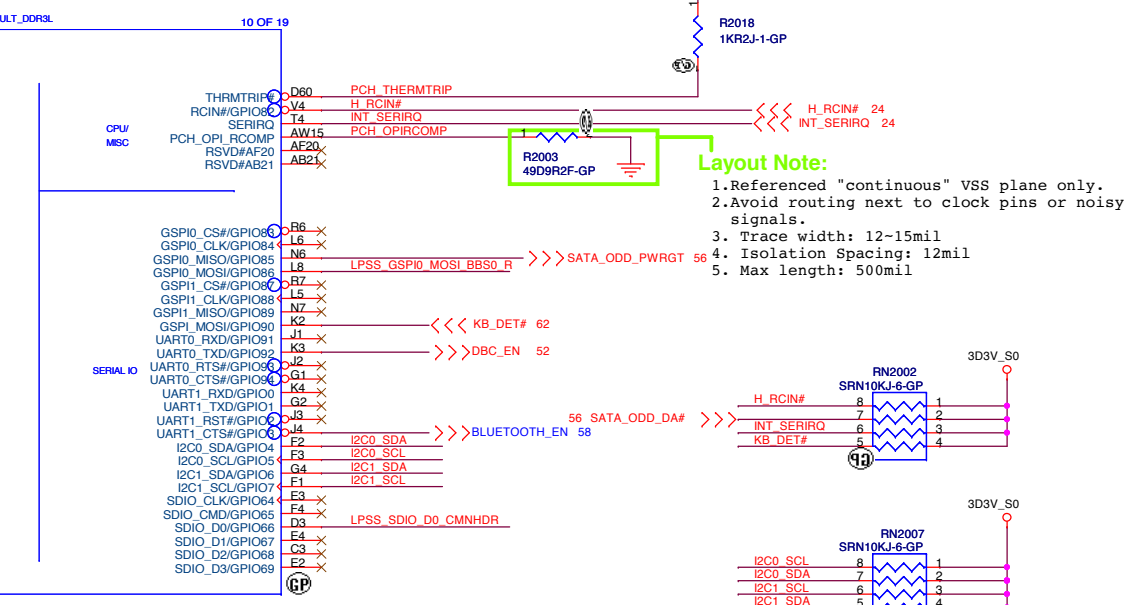
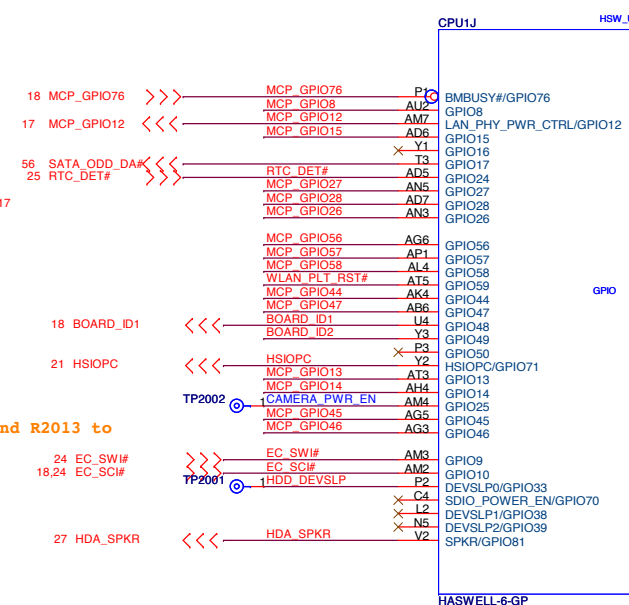
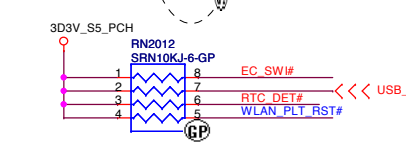
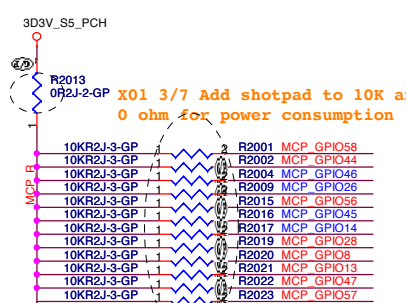
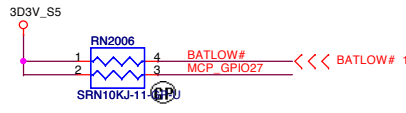
X01 3/7 Change value from test report

HDD1
ODD
0114 Change

Layout Note:
4mil trace at break-out and 3
12-15mil trace with <0.2 ohms
and length total <= 500mils.



SSID = CPU



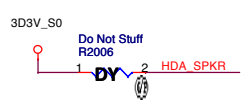
Layout Note:

1. Referenced "continuous" VSS plane only.
2. Avoid routing next to clock pins or noisy signals.
3. Trace width: 12~15mil
4. Isolation Spacing: 12mil
5. Max length: 500mil

PCH strap pin:

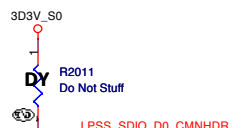
18,30 NO REBOOT	
HDA_SPKR	* Low = Disable (Default) High = Enable

The internal pull-down is disabled after PLTRST# deasserts



Top-Block Swap Override mode	
SDIO_D0 / GPIO66	High = Enable "Top-Block swap" mode (Default) * Low = Disable "Top-Block swap" mode

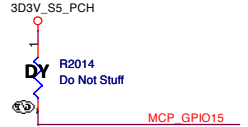
The internal pull-down is disabled after PLTRST# deasserts



Need SW double confirm if that's needed Top-Block swap

TLS Confidentiality	
GPIO15	* Low = Disable Intel ME Crypto TLS High = Enable Intel ME Crypto TLS

The internal pull-down is disabled after RSMRST# deasserts.



Boot BIOS Strap Bit BBS	
Boot BIOS Destination	* Low = SPI High = LPC

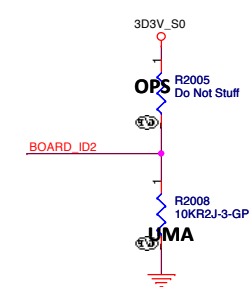
The internal pull-down is disabled after PLTRST# deasserts



Need double confirm, GPIO table set to GPI if that's needed PH or PL

BIOS strap pin:

BIOS UMA/DIS Strap pin		
	BOARD_ID1	BOARD_ID2
UMA	1	0
DIS	1	1



UM

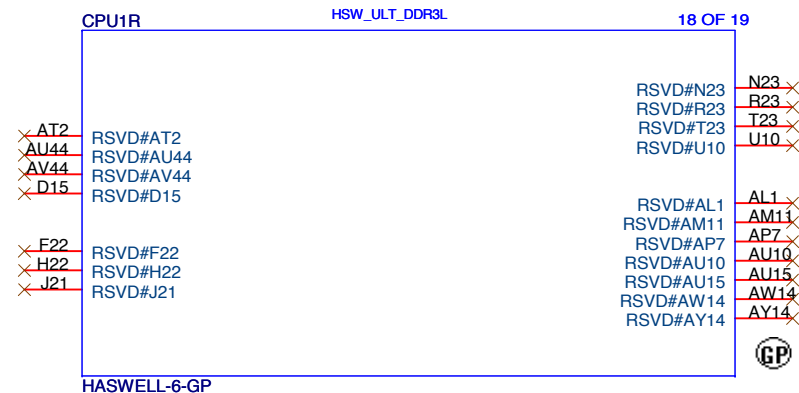
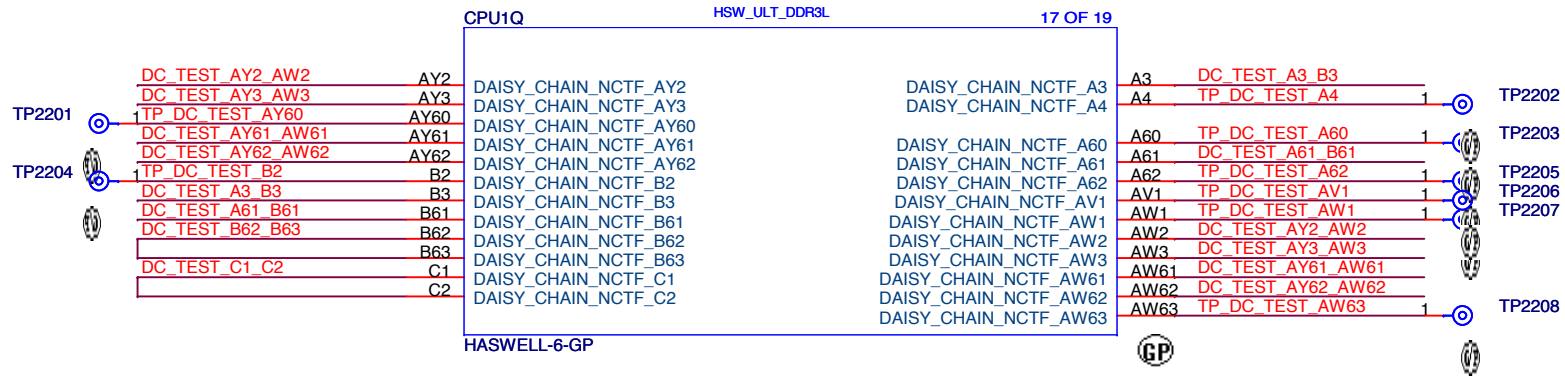
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (GPIO/CPU)**

Size A3 Document Number: **Latitude300 Haswell** Rev **X00**


Date: Friday, March 15, 2013 Sheet 20 of 104

SSID = PCH

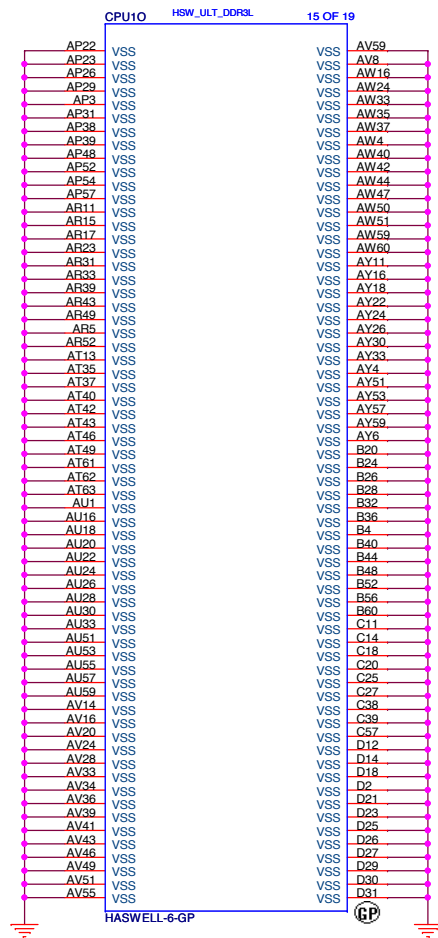
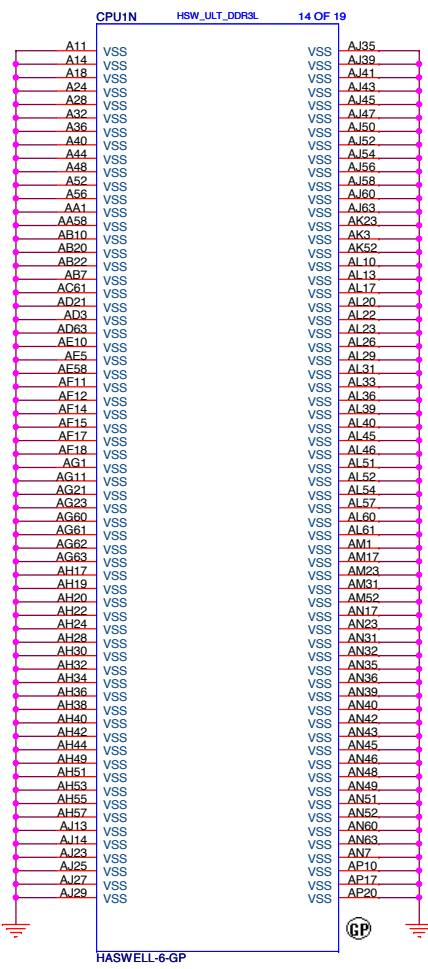


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UM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title (Reserved)			
Size A4	Document Number Latitude300 Haswell		Rev X00
Date: Friday, March 15, 2013	Sheet 22	of	104

SSID = PCH

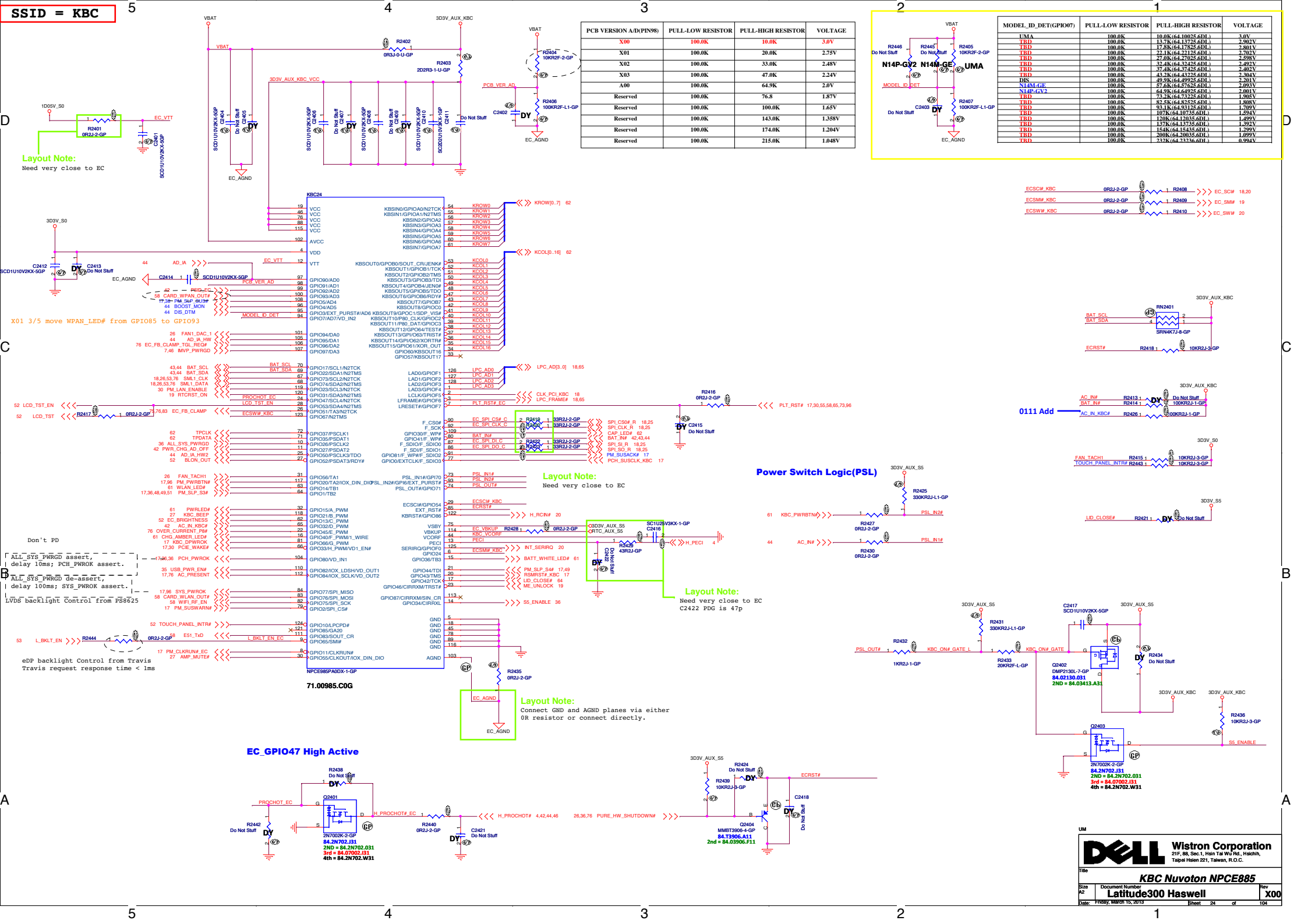


UM

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **(Reserved)**

Size: A3	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet: 23	of 104



SSID = KBC

PCB VERSION A/D(PIN#)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
X00	100.0K	10.0K	3.0V
X01	100.0K	20.0K	2.75V
X02	100.0K	33.0K	2.48V
X03	100.0K	47.0K	2.24V
A00	100.0K	64.9K	2.0V
Reserved	100.0K	76.8	1.87V
Reserved	100.0K	100.0K	1.65V
Reserved	100.0K	143.0K	1.358V
Reserved	100.0K	174.0K	1.204V
Reserved	100.0K	215.0K	1.048V

MODEL_ID_DET(GPIO07)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
L1M4	100.0K	10.0K(64.10075.6D1)	3.0V
TRD	100.0K	13.7K(64.13725.6D1)	2.902V
TRD	100.0K	17.8K(64.17825.6D1)	2.801V
TRD	100.0K	22.1K(64.22125.6D1)	2.700V
TRD	100.0K	27.0K(64.27025.6D1)	2.598V
TRD	100.0K	32.4K(64.32425.6D1)	2.495V
TRD	100.0K	37.4K(64.37425.6D1)	2.402V
TRD	100.0K	43.2K(64.43225.6D1)	2.300V
TRD	100.0K	49.9K(64.49925.6D1)	2.201V
TRD	100.0K	57.6K(64.57625.6D1)	2.092V
TRD	100.0K	64.9K(64.64925.6D1)	2.000V
TRD	100.0K	73.2K(64.73225.6D1)	1.905V
TRD	100.0K	82.5K(64.82525.6D1)	1.808V
TRD	100.0K	93.1K(64.93125.6D1)	1.709V
TRD	100.0K	107K(64.10735.6D1)	1.594V
TRD	100.0K	129K(64.12935.6D1)	1.500V
TRD	100.0K	157K(64.15735.6D1)	1.392V
TRD	100.0K	184K(64.18435.6D1)	1.299V
TRD	100.0K	200K(64.20035.6D1)	1.099V
TRD	100.0K	232K(64.23235.6D1)	0.994V

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC

Layout Note:
Need very close to EC
C2422 PDG is 47p

Layout Note:
Connect GND and AGND planes via either 0R resistor or connect directly.

EC GPIO47 High Active

Power Switch Logic(PSL)

Don't PD

ALL_SYS_PWRGD assert,
delay 10ms; PCH_PWROK assert.
All_SYS_PWRGD de-assert,
delay 100ms; SYS_PWROK assert.
LVDS backlight Control from P98625

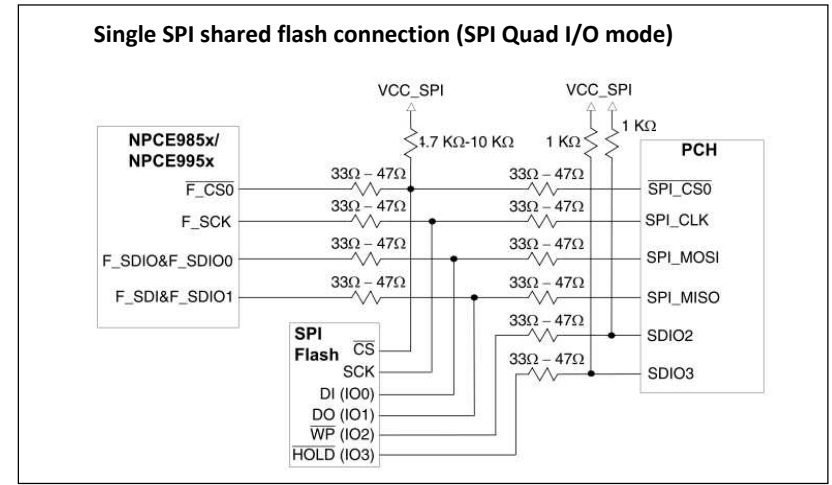
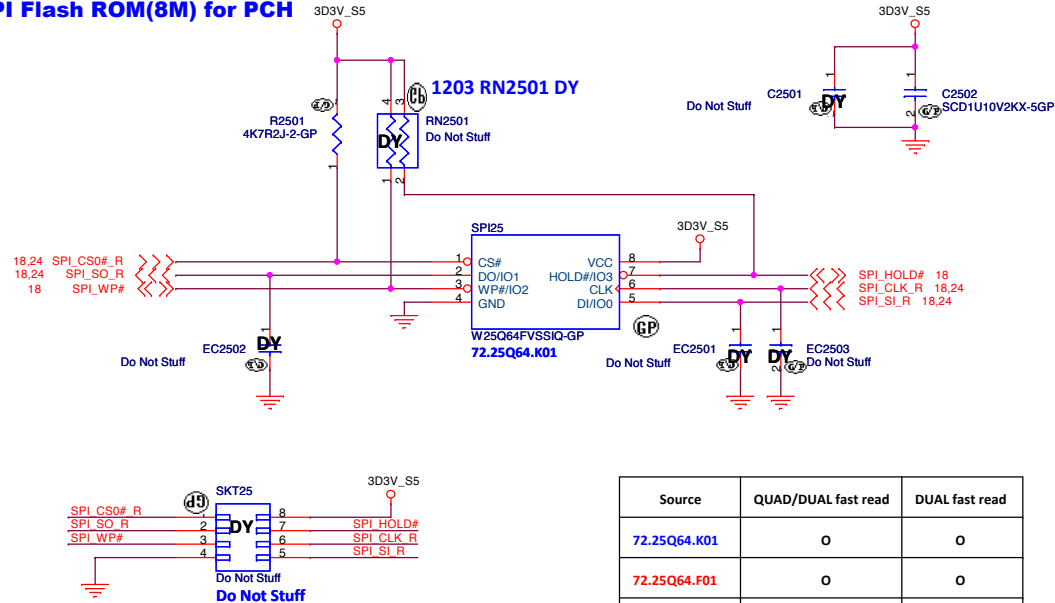
eDP backlight Control from Travis
Travis request response time < 1ms



Part Number: **KBC Nuvoton NPCE885**
 Document Number: **84.2N702.J31**
 Latitude300 Haswell
 Date: Friday, March 15, 2013 Sheet 24 of 104

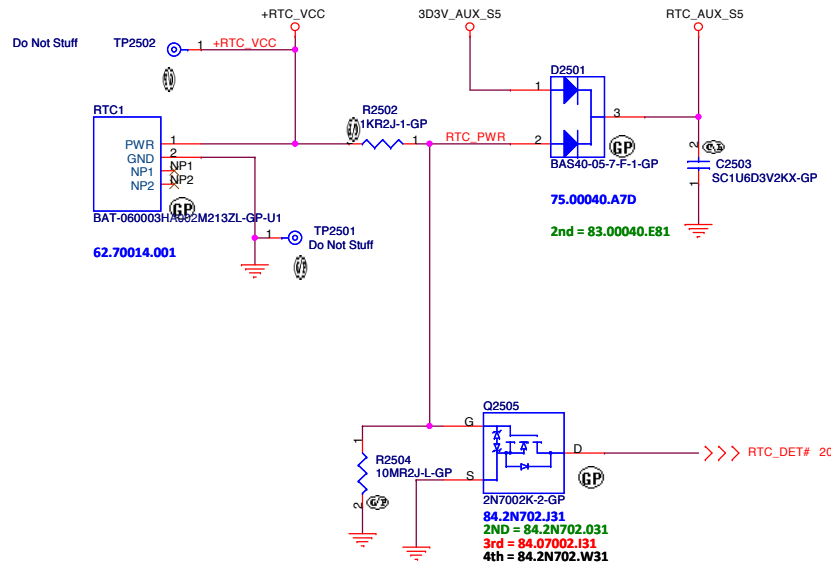
SSID = Flash.ROM

SPI Flash ROM(8M) for PCH



Refer to "NPCE985x/ NPCE995x board design reference guide"

SSID = RBATT



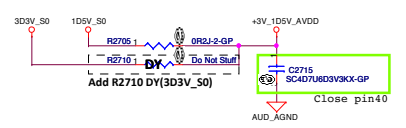
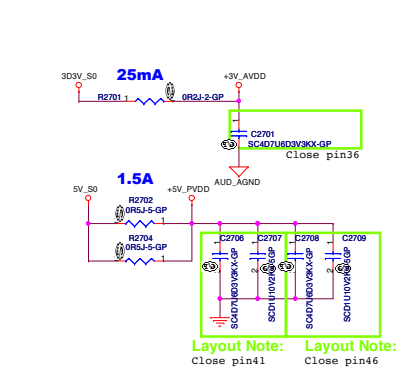
UM

Wistron Corporation
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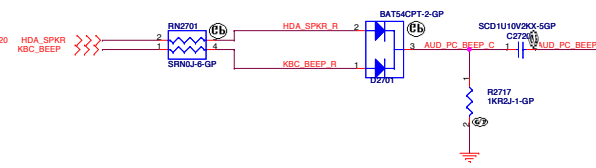
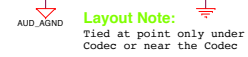
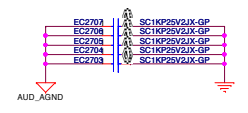
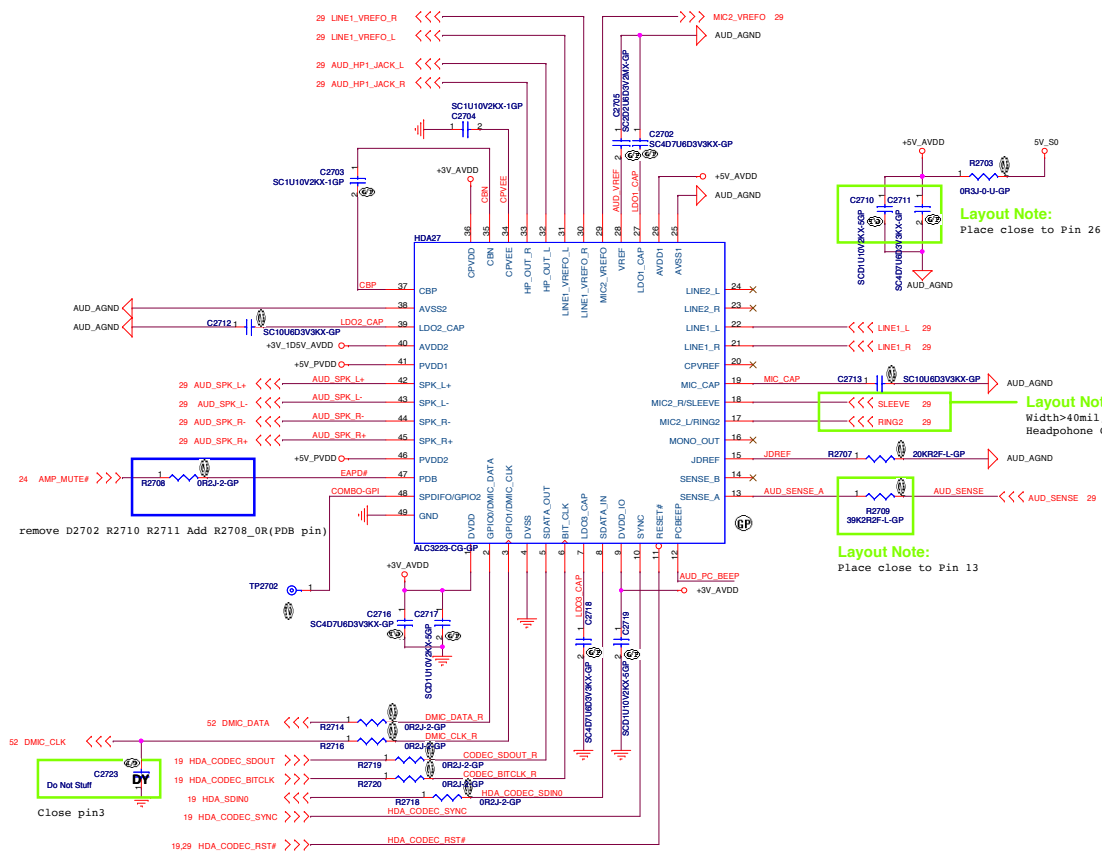
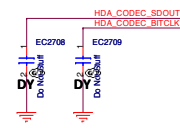
Title: **Flash/RTC**

Size A3	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet 25 of 104	

SSID = AUDIO



Alzalia I/F EMI



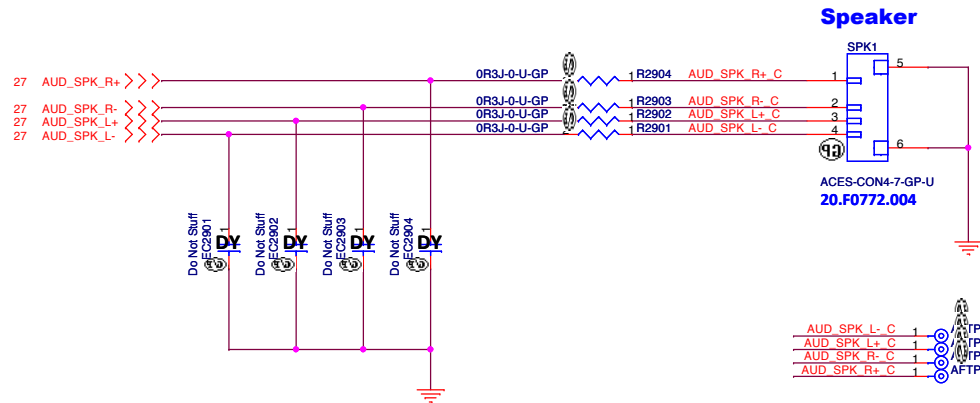
(Blanking)

UM

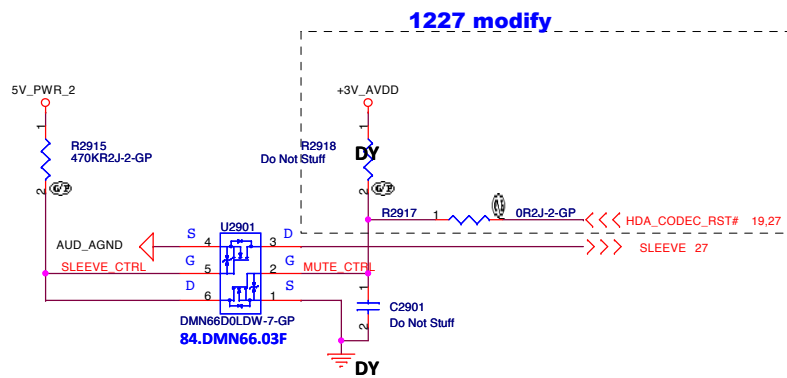
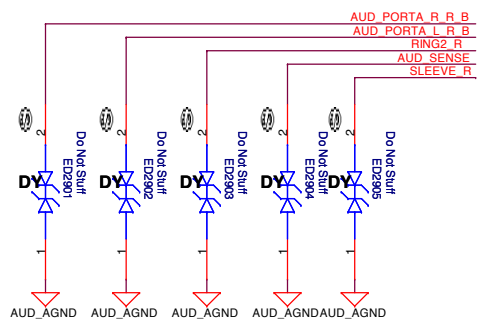
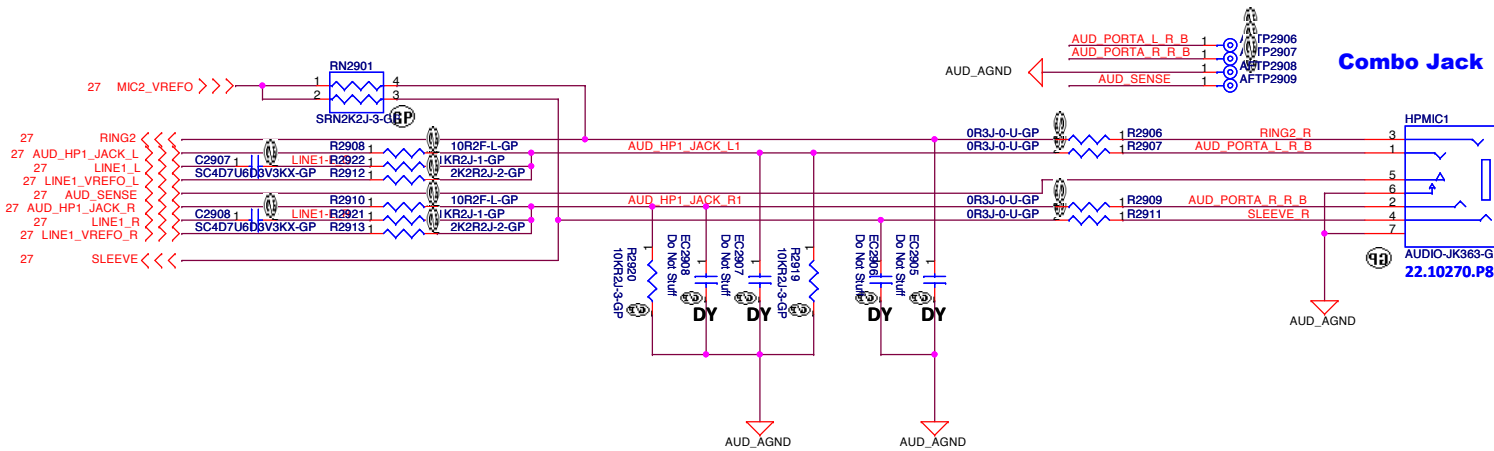
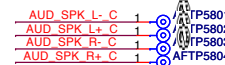


Title		
Reserved		
Size	Document Number	Rev
A3	Latitude300 Haswell	X00
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SSID = AUDIO



CONN Pin	Net name
Pin1	SPK_R+
Pin2	SPK_R-
Pin3	SPK_L+
Pin4	SPK_L-



UM

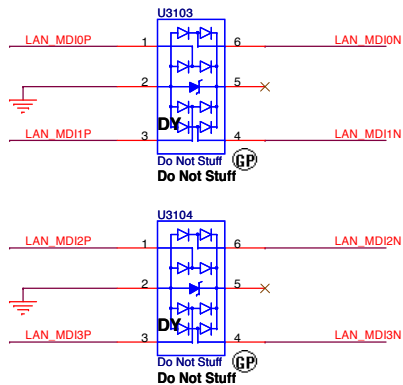
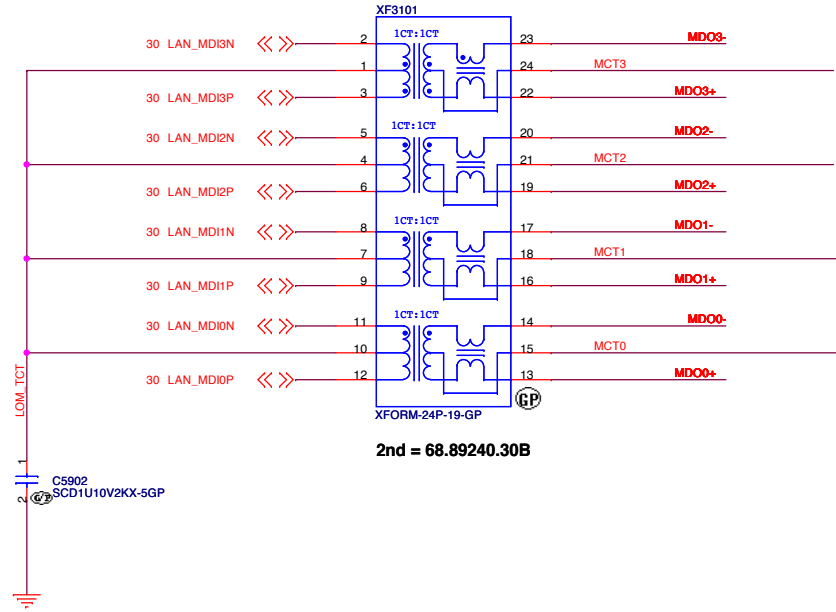
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Thermal NCT7718W/Fan Controller P2793**

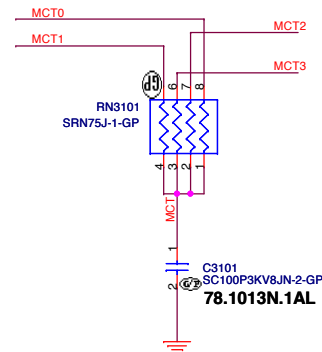
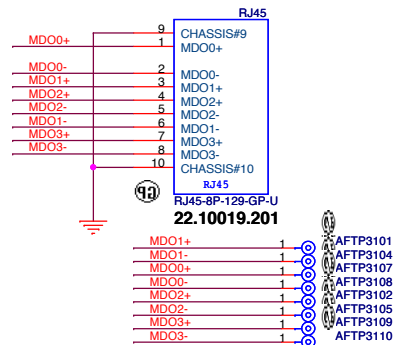
Size A3	Document Number	Rev X00
Date: Friday, March 15, 2013	Latitude300 Haswell	Sheet 29 of 104

SSID = LOM

100/GIGA LAN Transformer



RJ45 CONN



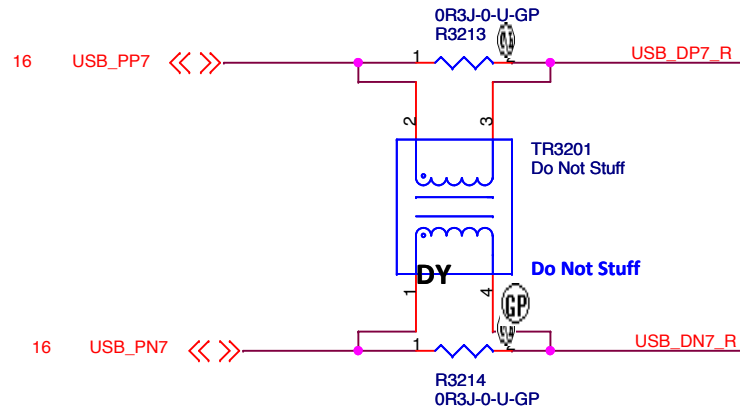
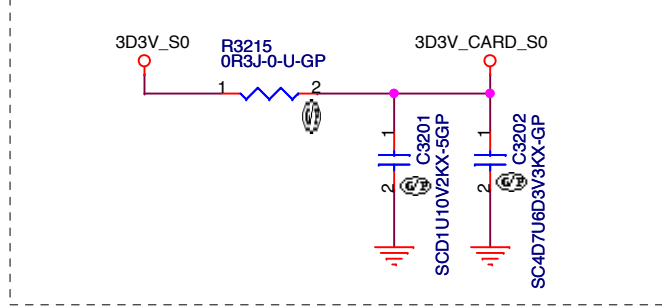
UM

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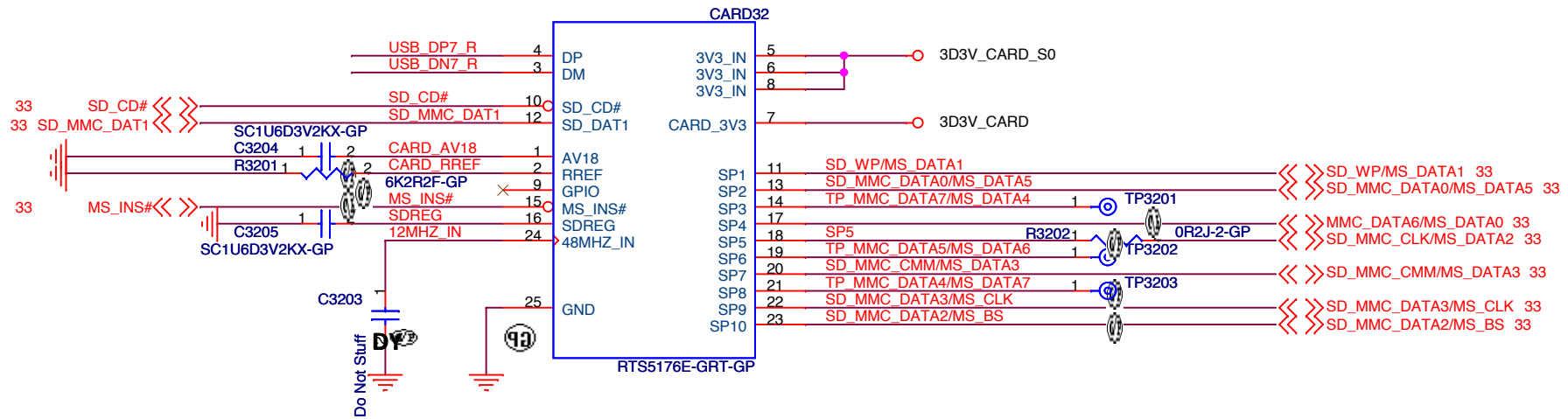
Title: **XFOM&RJ45**

Size: A3	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet: 31	of: 104

1121 remove Switch(No support D3 cold)



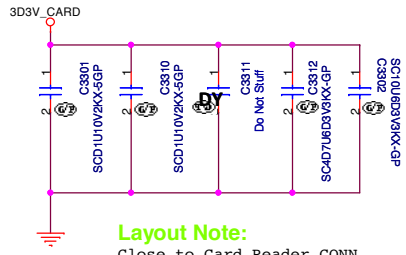
Pin name	Net name
SD_DAT1	SD_MMC_DAT1
SP1	SD_WP/MS_DATA1
SP2	SD_MMC_DATA0/MS_DATA5
SP3	MMC_DATA7/MS_DATA4
SP4	MMC_DATA6/MS_DATA0
SP5	SD_MMC_CLK/MS_DATA2
SP6	MMC_DATA5/MS_DATA6
SP7	SD_MMC Command/MS_DATA3
SP8	MMC_DATA4/MS_DATA7
SP9	SD_MMC_DATA3/MS_CLK
SP10	SD_MMC_DATA2/MS_BS



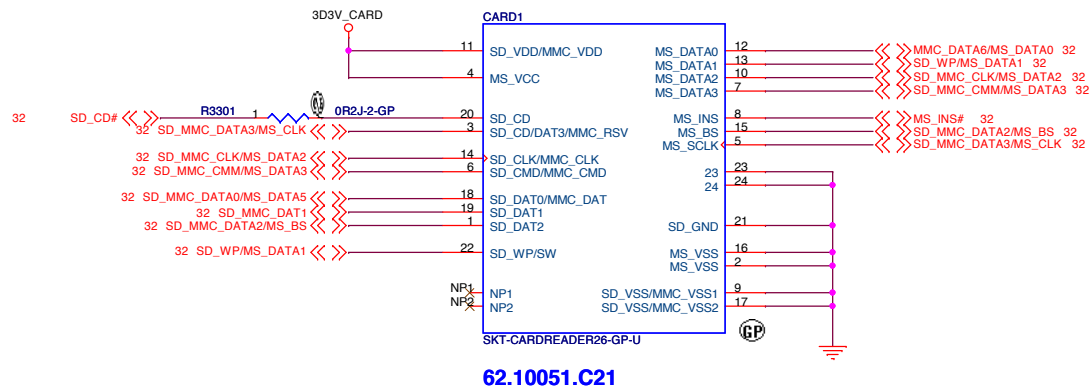
UM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <h3>Card Reader-RTS5176</h3>	
Size A4	Document Number Latitude300 Haswell	Rev X00	
Date: Friday, March 15, 2013		Sheet 32	of 104

SSID = SDIO

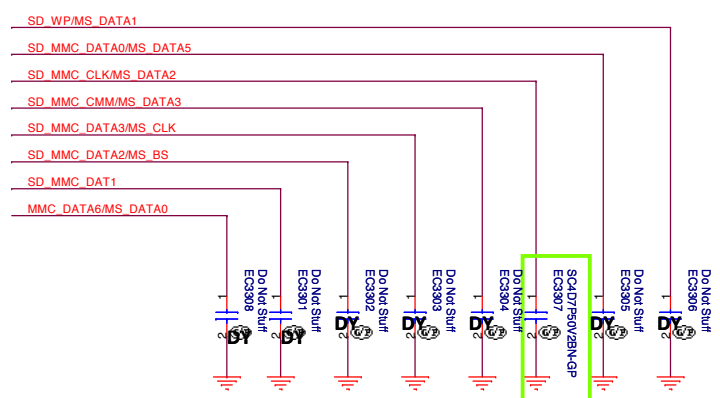


SD/MS/MMC Card Connector



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For EMI Reserved



Layout Note:
please close U3201

1203 modify 10P change to 4.7P

UM

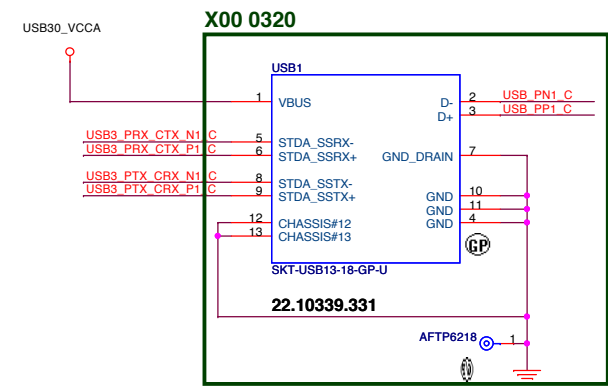
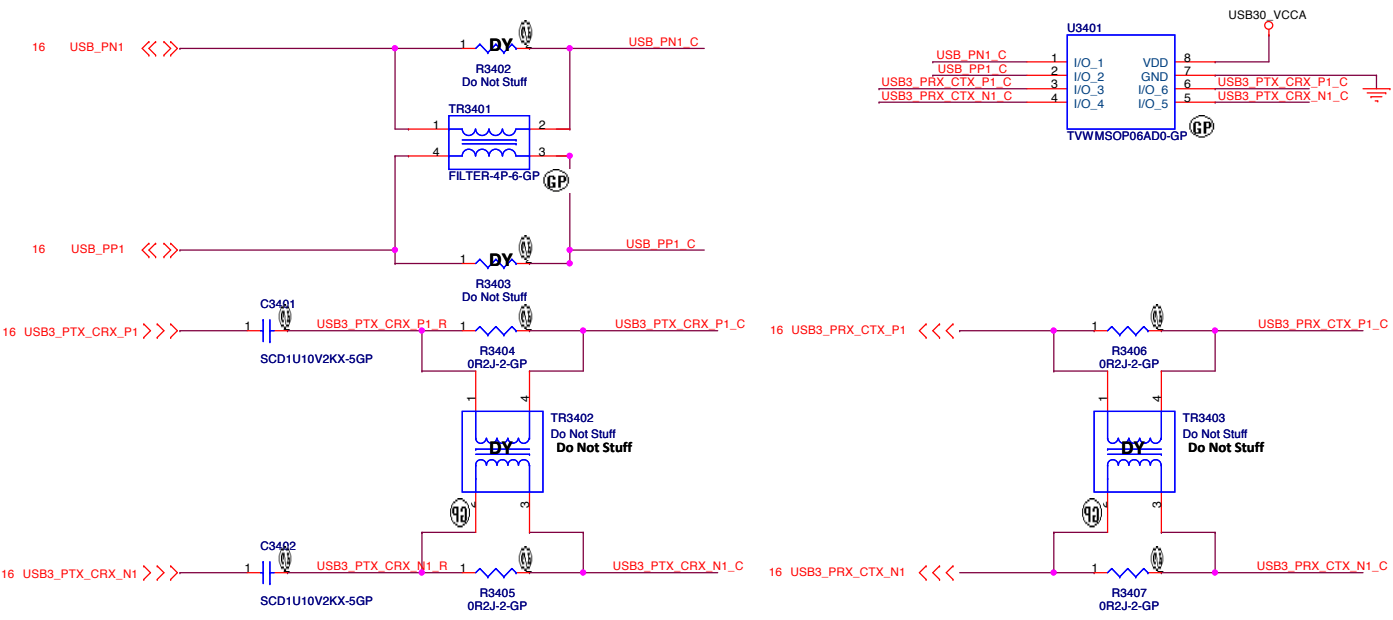
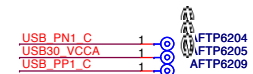
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **SD/XD/MS/MMC Card CONN**

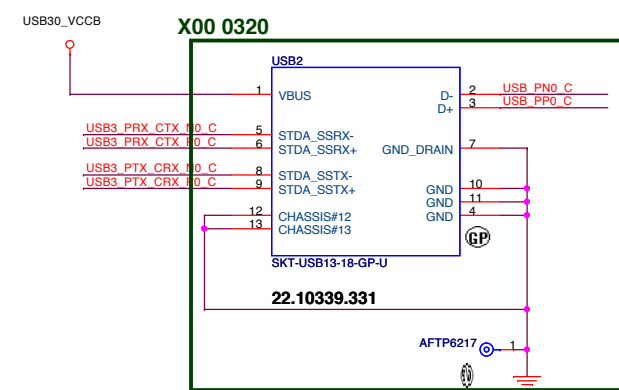
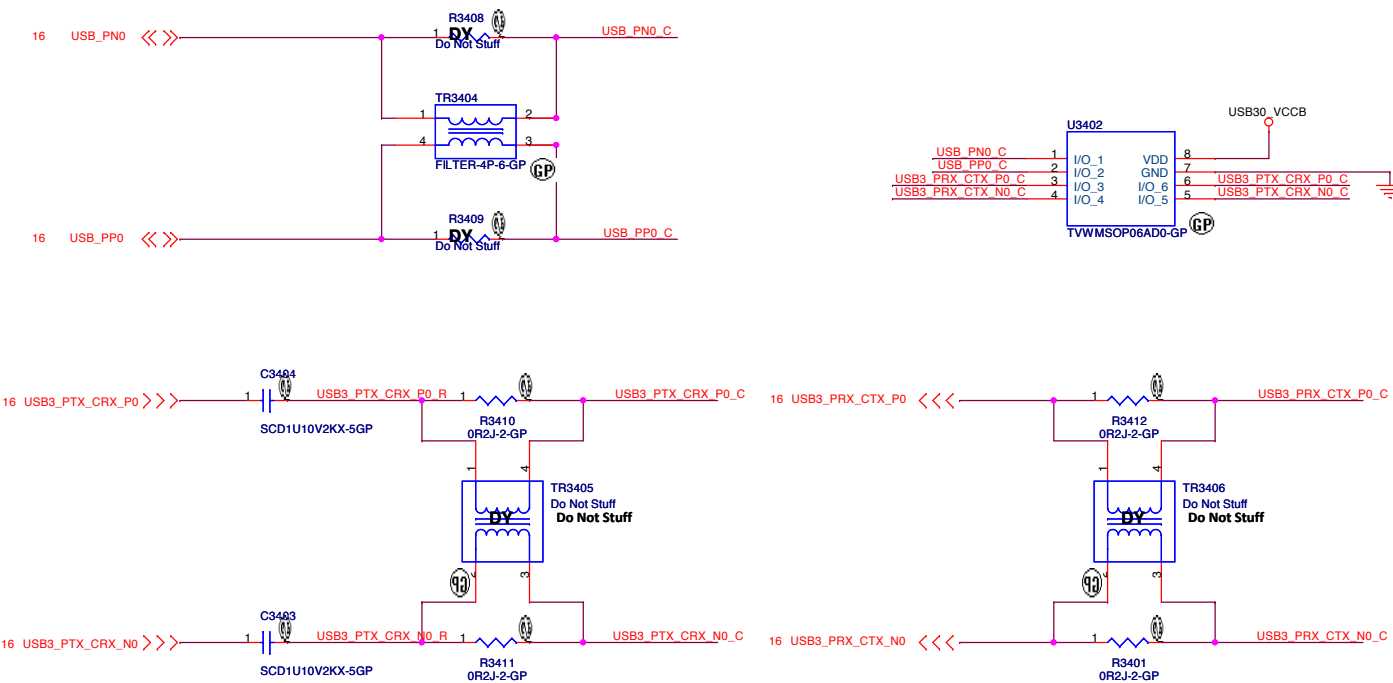
Size A3	Document Number Latitude300 Haswell	Rev X00
Date: Friday, March 15, 2013	Sheet 33 of 104	

SSID = USB

USB3.0 Port1



USB3.0 Port2

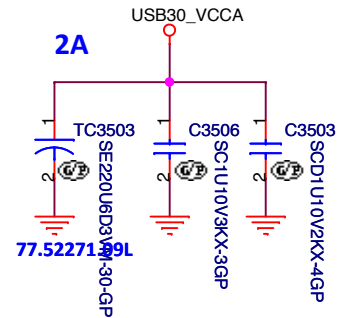
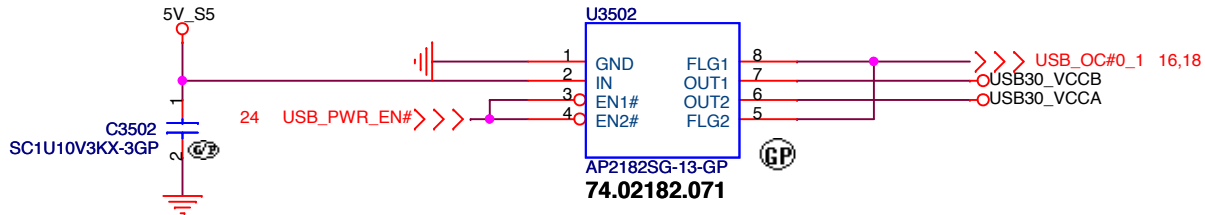


UM

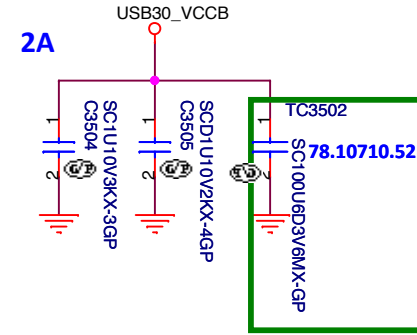
DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB 3.0**

Size: A3	Document Number: Latitude300 Haswell	Rev: X00
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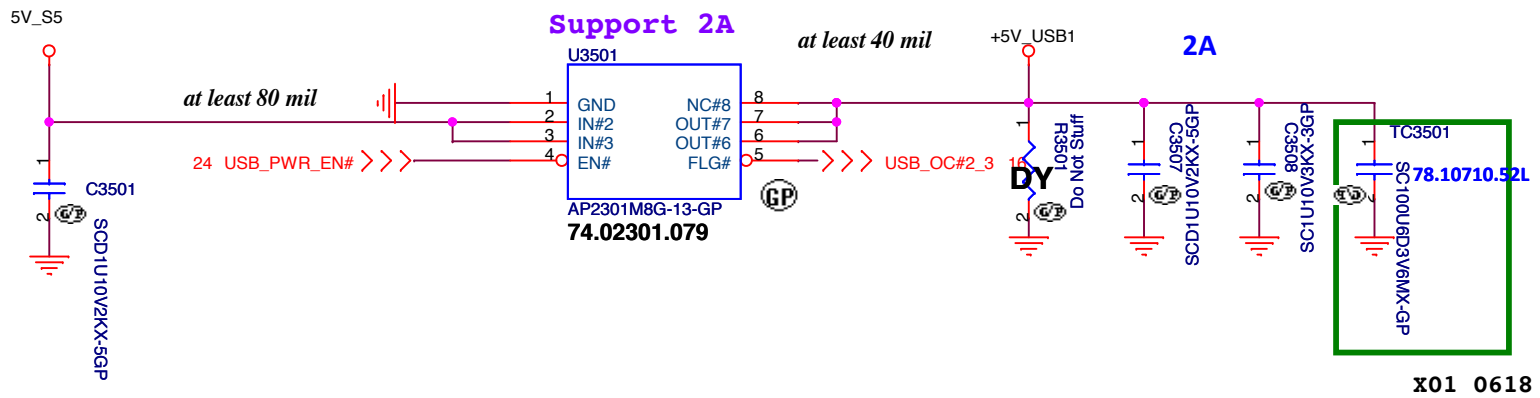


USB3.0 Port1



USB3.0 Port2

Right USB Power x1



X01 0618

UM

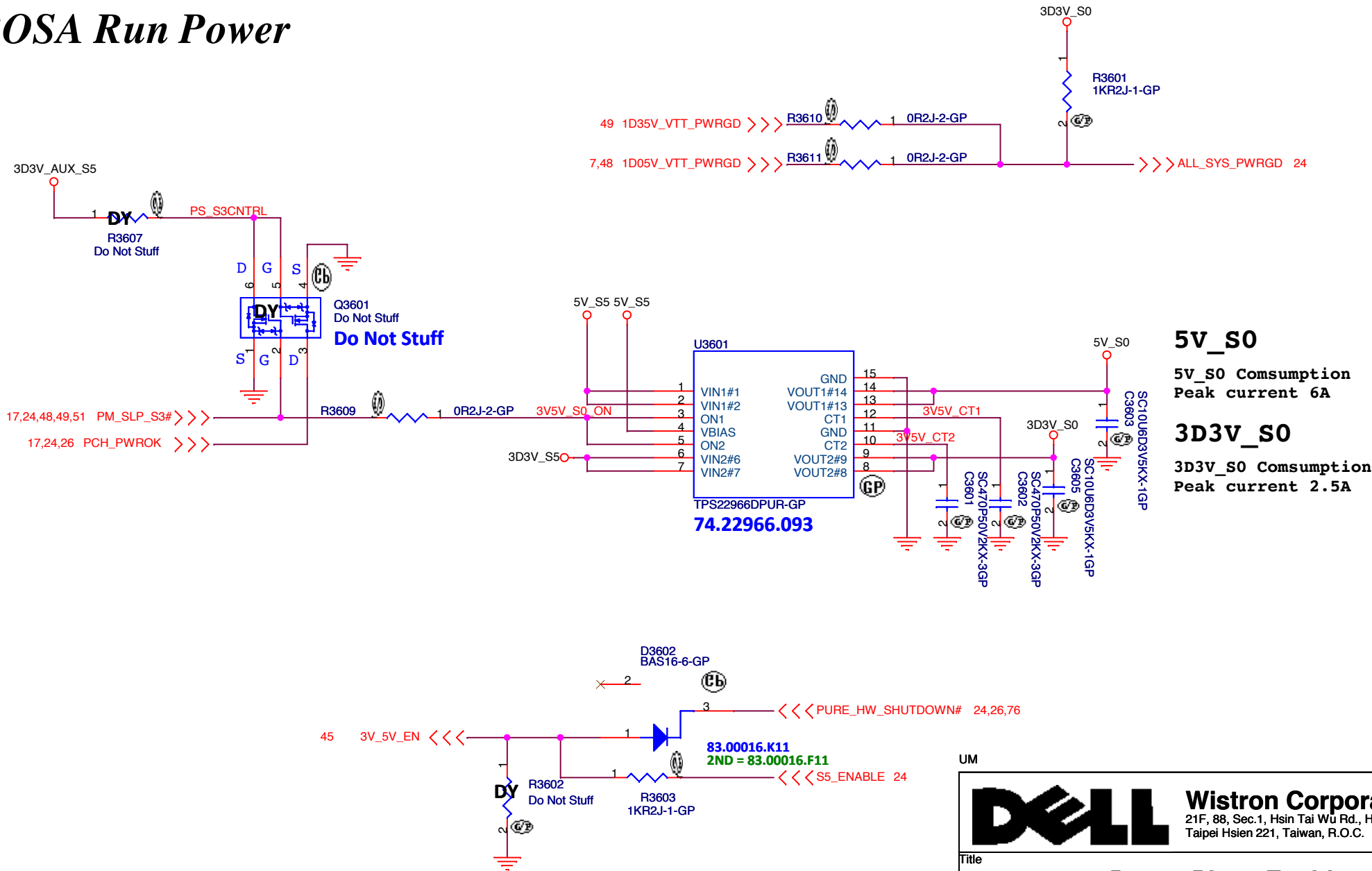
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title		
USB Power SW		
Size	Document Number	Rev
	Latitude300 Haswell	X00
Date:	Friday, March 15, 2013	Sheet 35 of 104

SSID = Reset.Suspend

Power Good

ROSA Run Power



UM

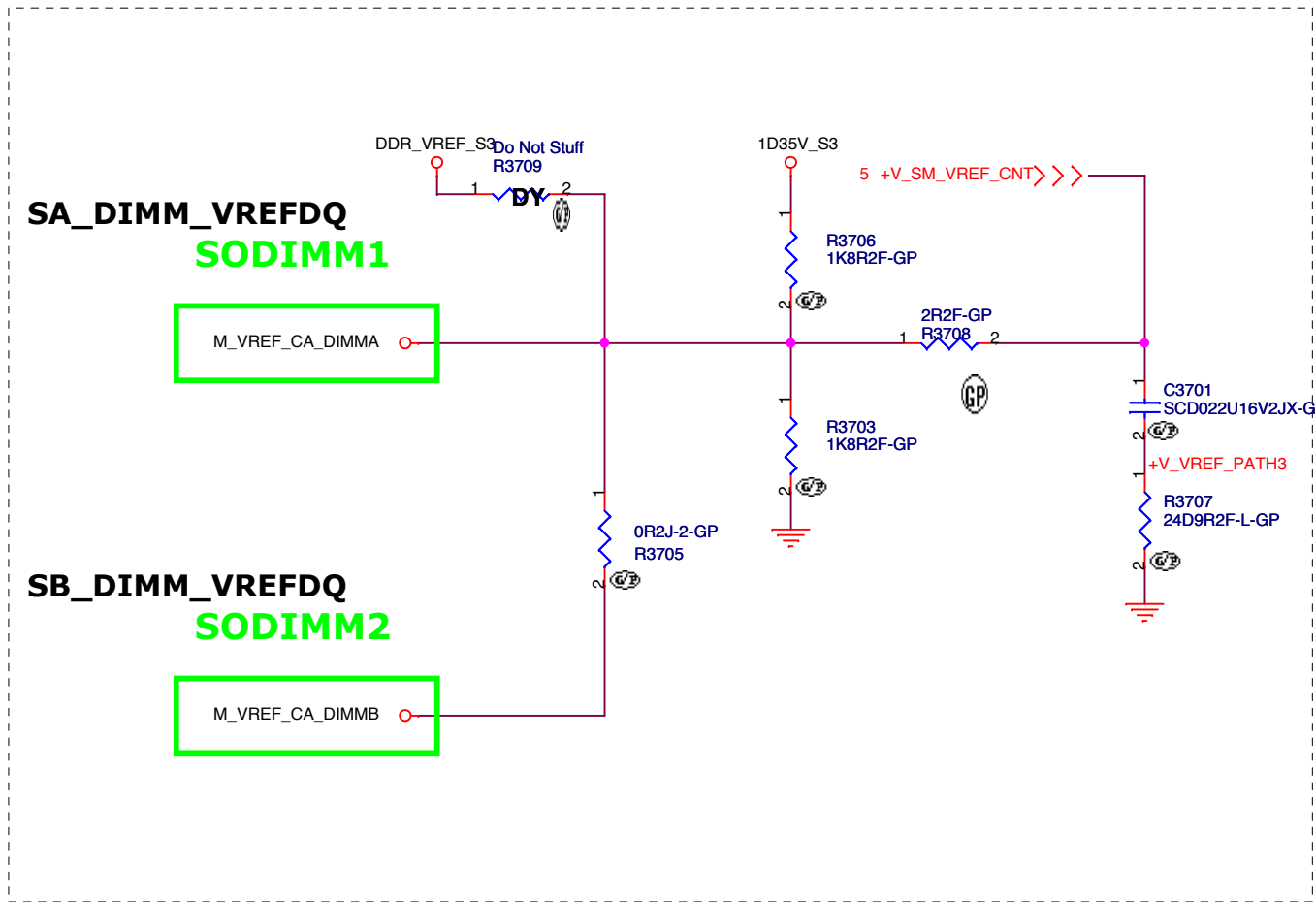
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Power Plane Enable

Size A4	Document Number Latitude300 Haswell	Rev X00
Date: Friday, March 15, 2013		Sheet 36 of 104

Layout Note:

Place Close SO-DIMM



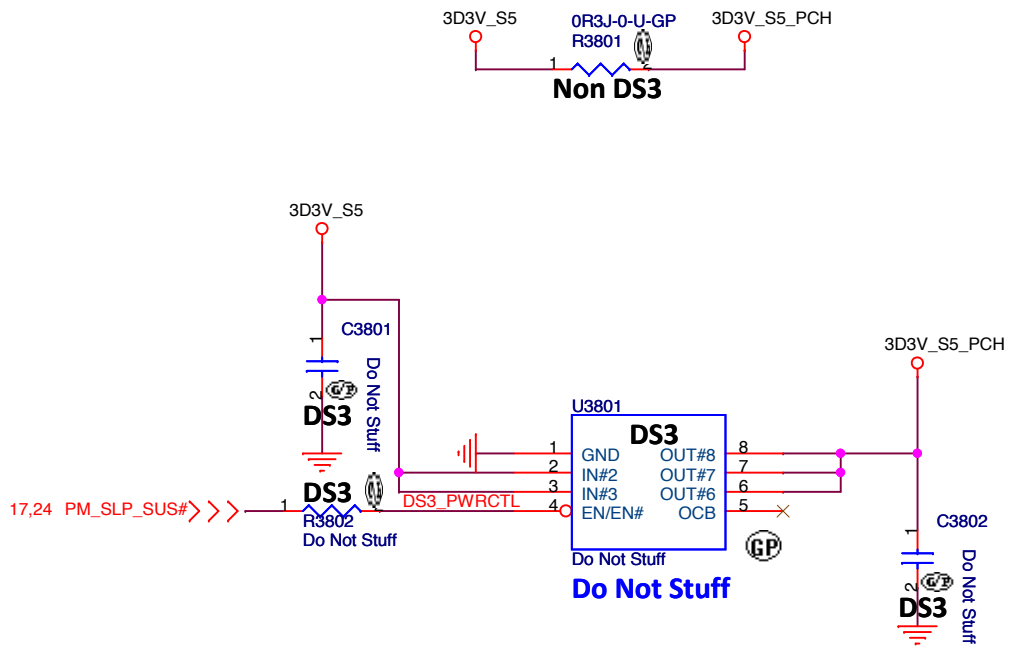
UM



Title **S3 Reduction Circuit**


Size A4 Document Number **Latitude300 Haswell** Rev **X00**

Date: Friday, March 15, 2013 Sheet 37 of 104



1210 change power switch (RdsON:100m ohm)

UM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title DSW	
Size A4	Document Number Latitude300 Haswell	Rev X00	
Date: Friday, March 15, 2013		Sheet 38 of 104	

SSID = CPU

UM


		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
CPU (POWER1)			
Size	Document Number	Rev	
Custom	Latitude300 Haswell	X00	
Date:	Friday, March 15, 2013	Sheet	39 of 104

UM

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
<i>Reserved</i>					
Size	Document Number				Rev
A3	<i>Latitude300 Haswell</i>				<i>X00</i>
Date:	Friday, March 15, 2013	Sheet	40	of	104

(Blanking)

UM

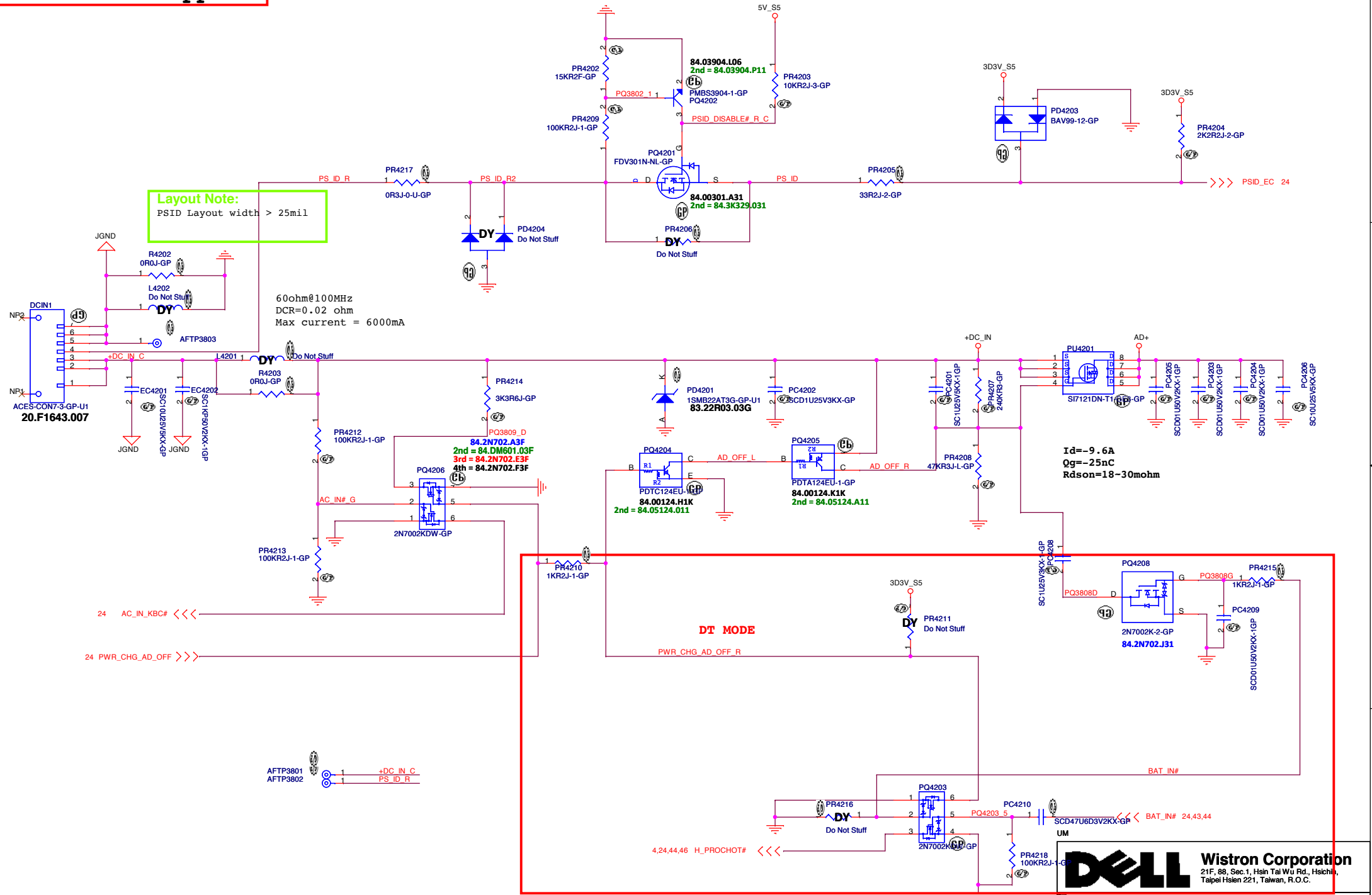
		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Latitude300 Haswell	Rev X00
Date: Friday, March 15, 2013	Sheet 41	of 104

SSID = PWR.Support

Layout Note:
PSID Layout width > 25mil

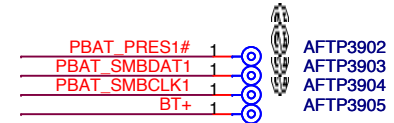
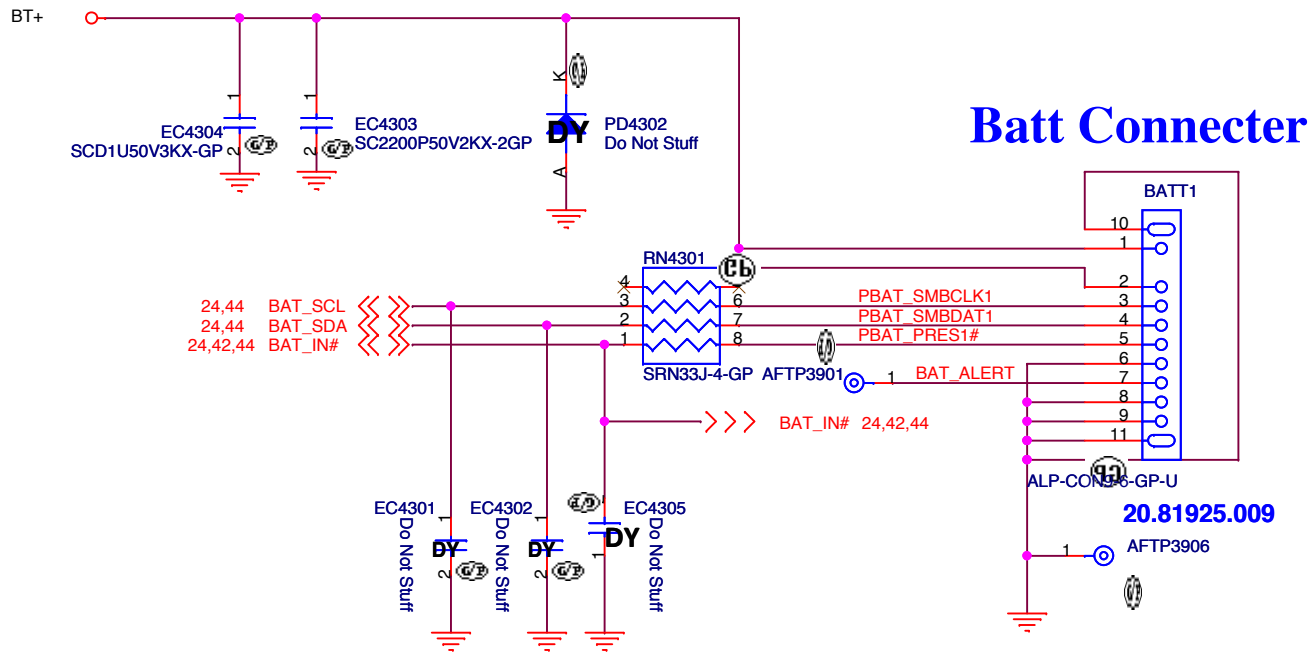
60ohm@100MHz
DCR=0.02 ohm
Max current = 6000mA

DT MODE
PWR_CHG_AD_OFF_R

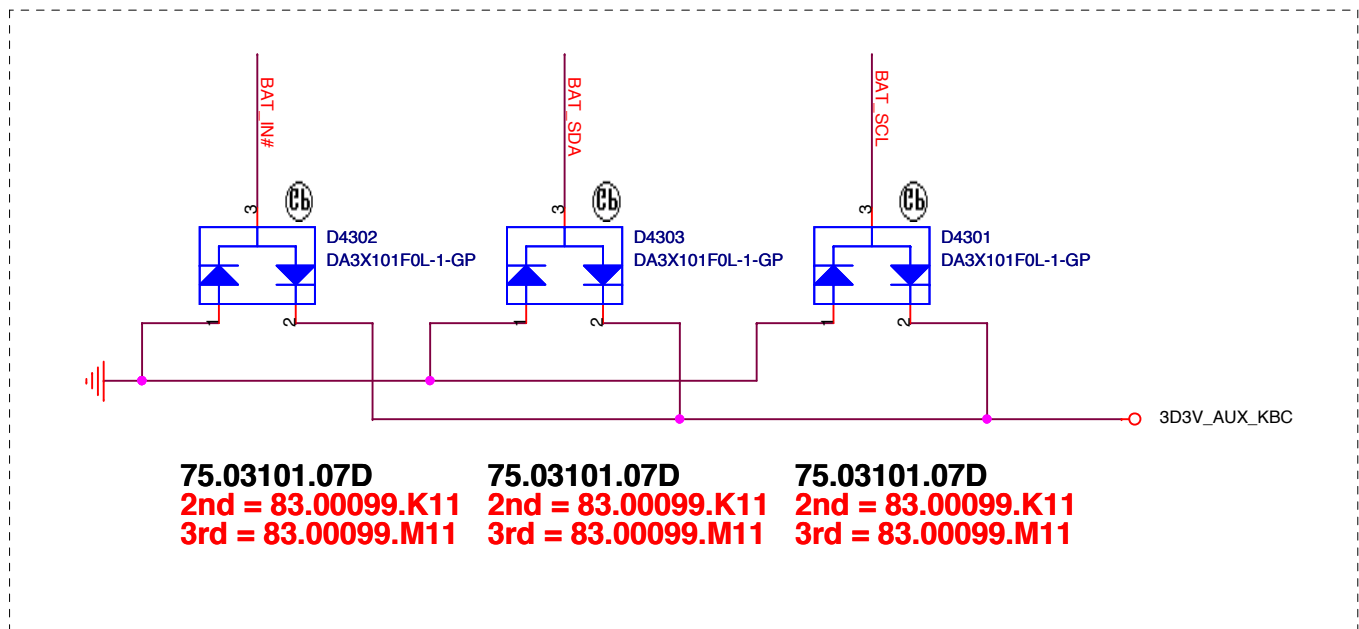


Title		DCIN	
Size	Document Number	Rev	
A3	Latitude300 Haswell	X00	
Date:	Friday, March 15, 2013	Sheet	42 of 104

SSID = PWR.Support



Placement: Close to Batt Connector

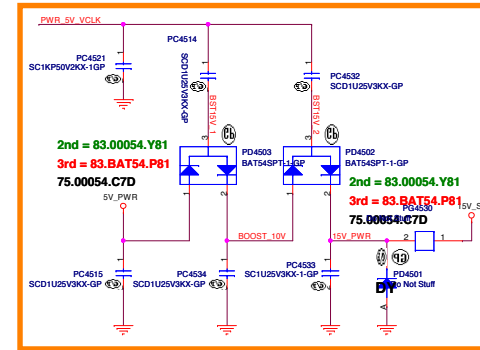
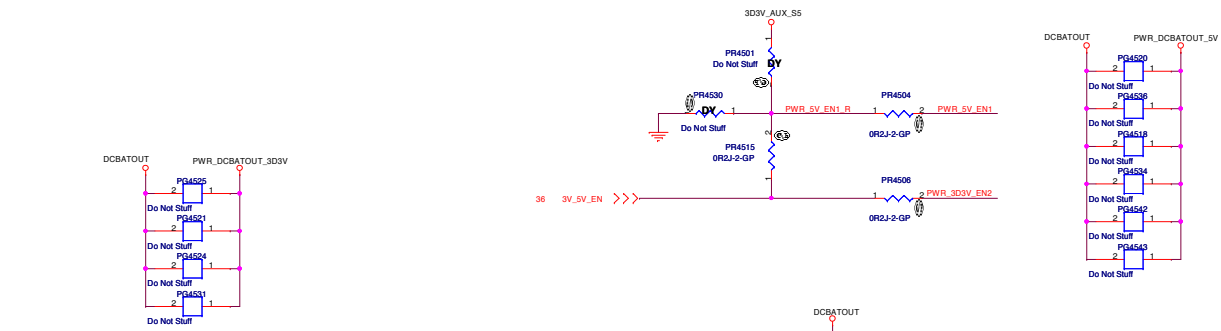


75.03101.07D 75.03101.07D 75.03101.07D
 2nd = 83.00099.K11 2nd = 83.00099.K11 2nd = 83.00099.K11
 3rd = 83.00099.M11 3rd = 83.00099.M11 3rd = 83.00099.M11

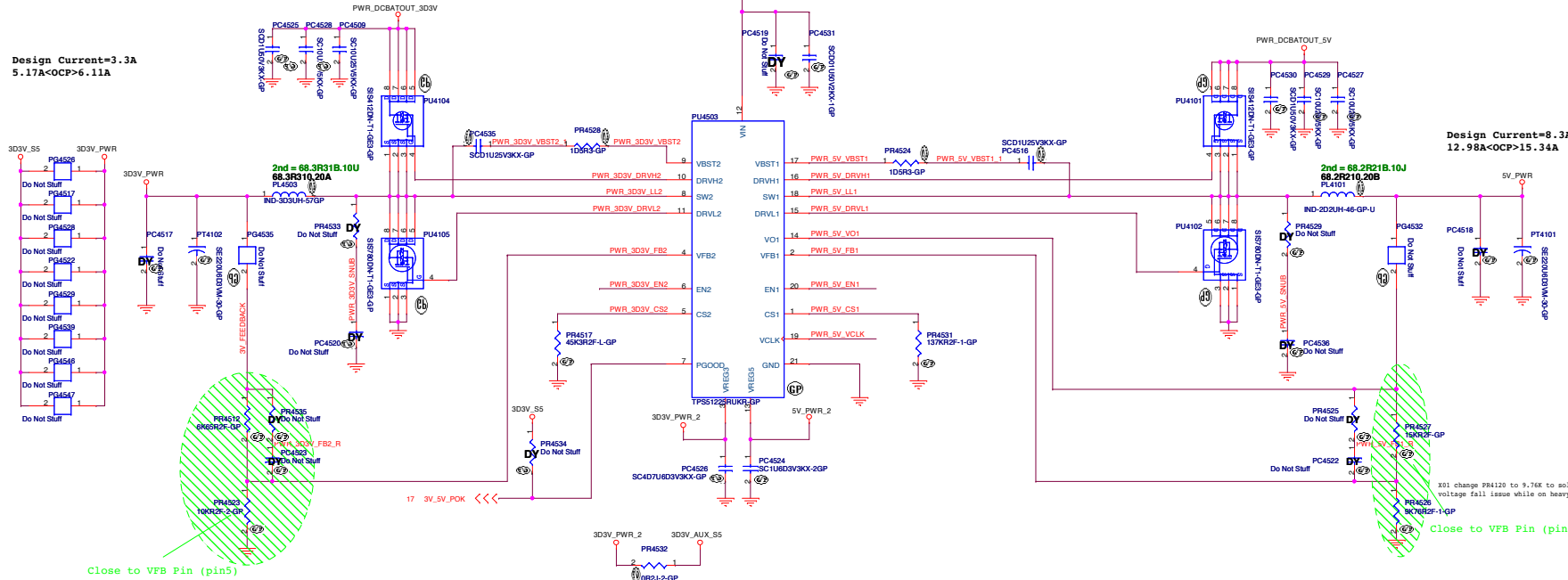
UM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		BATT CONN	
Title	Document Number		Rev
Size A4	Latitude300 Haswell		X00
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SSID = PWR.Plane.Regulator_5v3p3v



Design Current=3.3A
5.17A<OCP>6.11A



Design Current=8.3A
12.98A<OCP>15.34A

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cynotec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
H/S:SIS412 / 24mOhm/30mOhm*4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm*4.5Vgs / 84.00780.037

TPS51225 & TPS51285 Co-lay

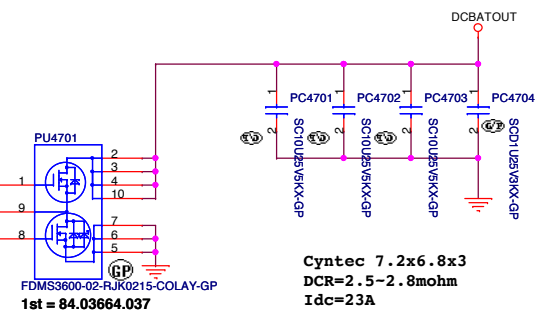
	TPS51225	TPS51285
PR4510	45.3KK	9.09K
PR4511	110K	22.1K

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18mohm/20mohm Isat =14Arms 68.2R210.20B
O/P cap:CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuki/ 17mOhm / 77.52271.09L
H/S:SIS412 / 24mOhm/30mOhm*4.5Vgs / 84.00412.037
L/S:SIS780 / 14.5mOhm/17.5mOhm*4.5Vgs / 84.00780.037

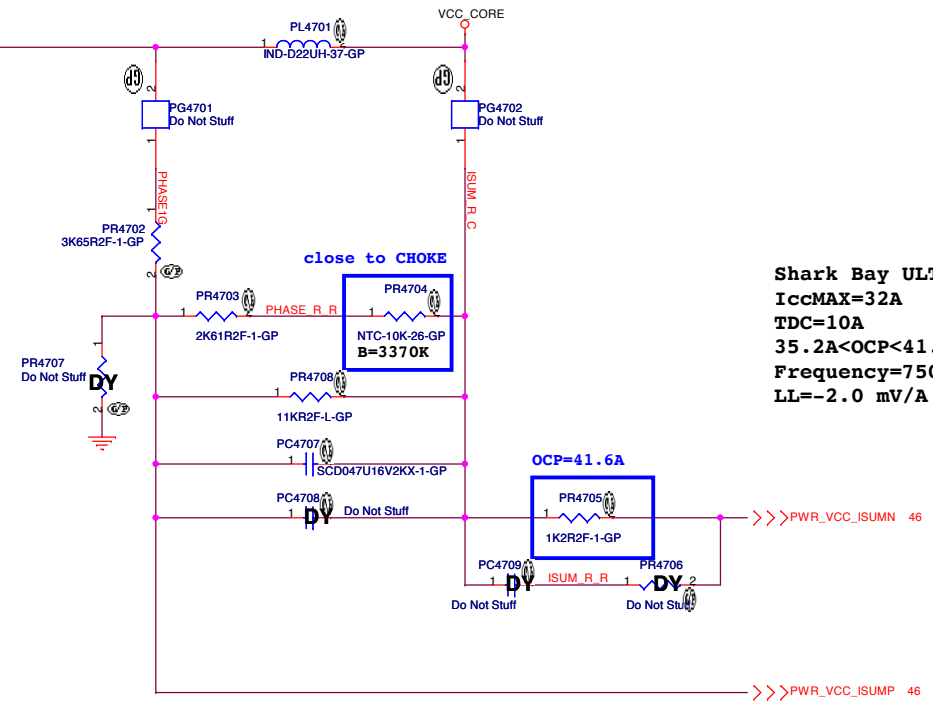
301 change PR4120 to 9.76K to solve 5V voltage fall issue while on heavy loading
Close to VFB Pin (pin2)

46 PWR_VCC_UG >>>
 46 PWR_VCC_BOOT >>>
 46 PWR_VCC_LG >>>

46 PWR_VCC_PHASE >>>



Cyntec 7.2x6.8x3
 DCR=2.5~2.8mohm
 Idc=23A

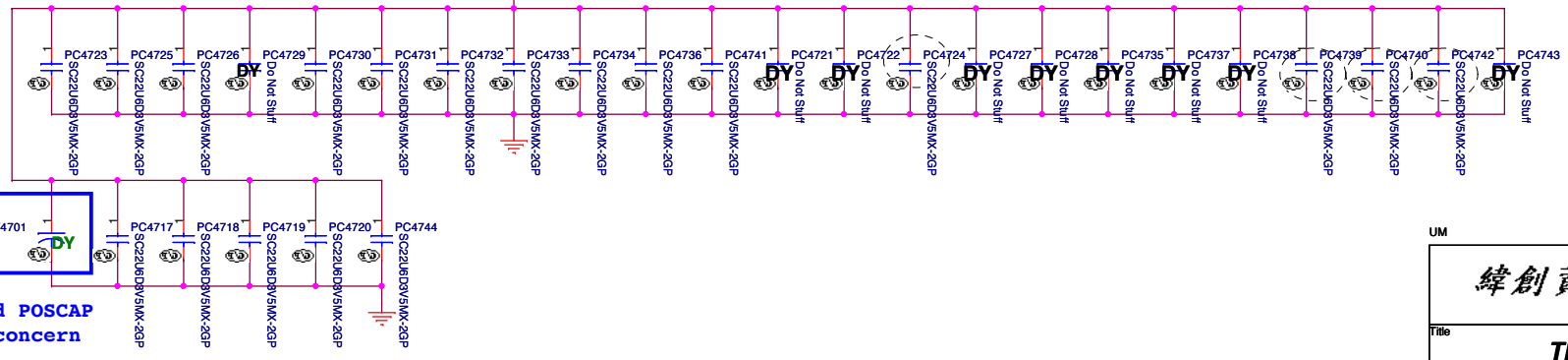


Shark Bay ULT 15W CPU
 IccMAX=32A
 TDC=10A
 35.2A<OCP<41.6A
 Frequency=750KHZ
 LL=-2.0 mV/A

OCP=41.6A

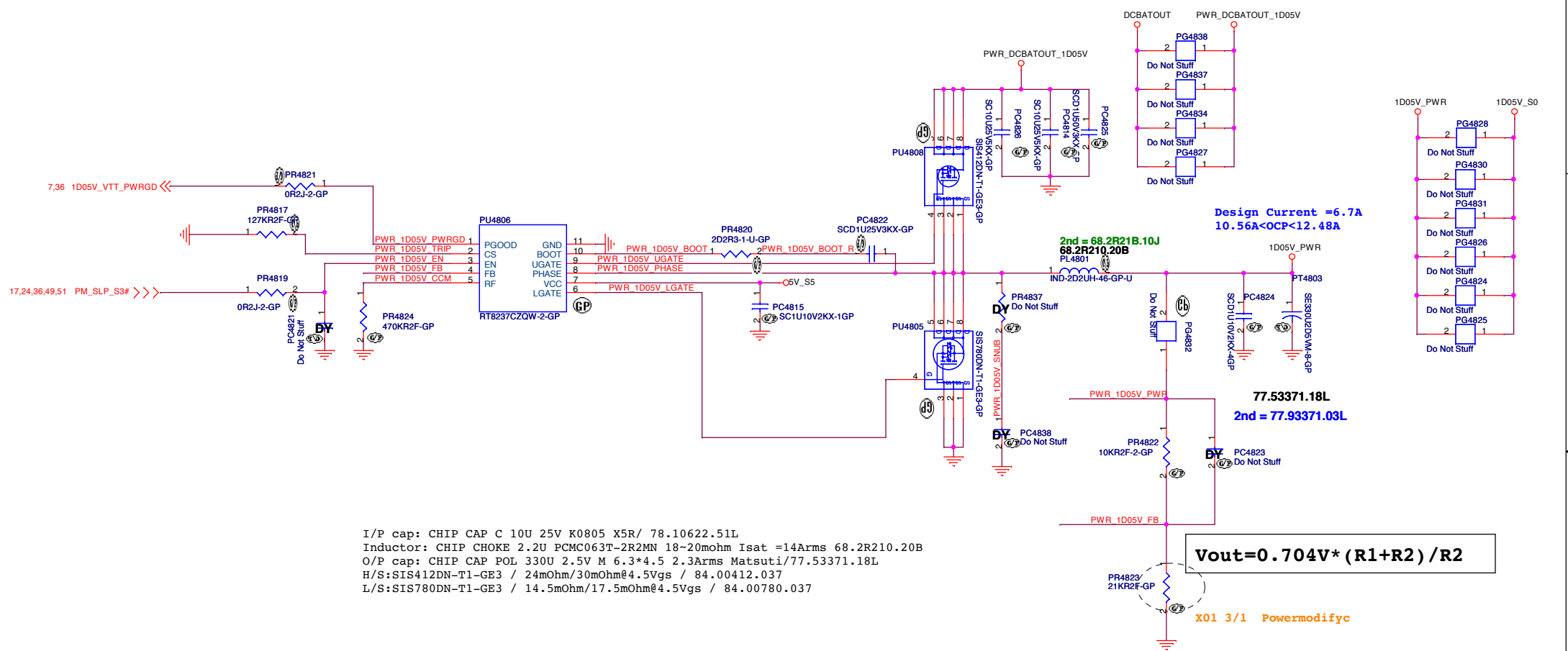
22uF/6.3V/0805*13
 330uF/2.5V/6.3*4.5/12mohm*1

X01 3/1 Power for pass transient spec



Don't need POSCAP
 If space concern

緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title TPS1622 CPUCORE(2/2)		
Size A3	Document Number Latitude300 Haswell	Rev X00
Date: Friday, March 15, 2013		Sheet 47 of 104

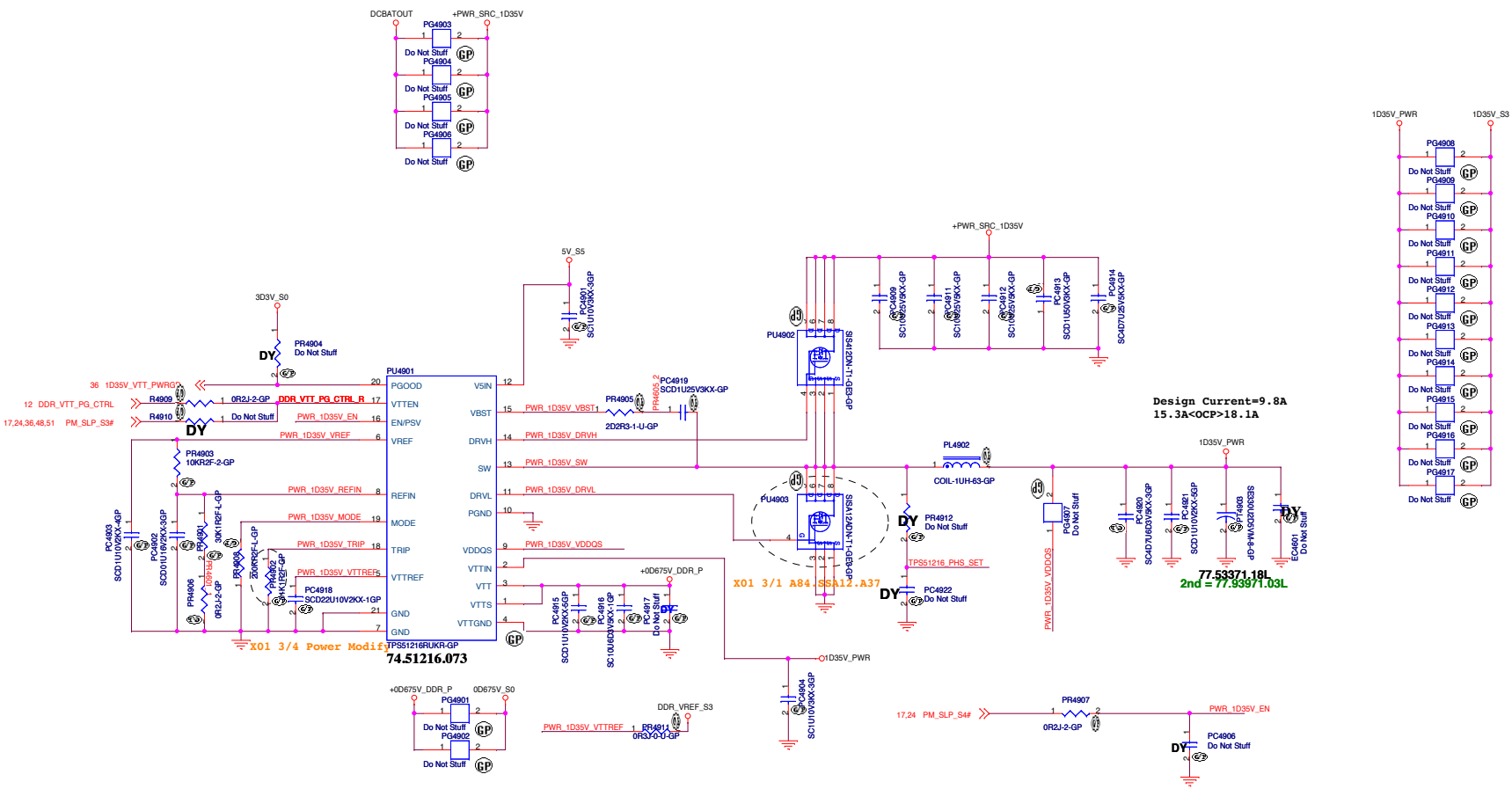


I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP CHOKE 2.2U PCMC063T-2R2MN 18~20mohm Isat =14Arms 68.2R210.20B
 O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
 H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
 L/S:SIS780DN-T1-GE3 / 14.5mOhm/17.5mOhm@4.5Vgs / 84.00780.037

$$V_{out} = 0.704V * (R1 + R2) / R2$$

X01 3/1 Powermodifyc

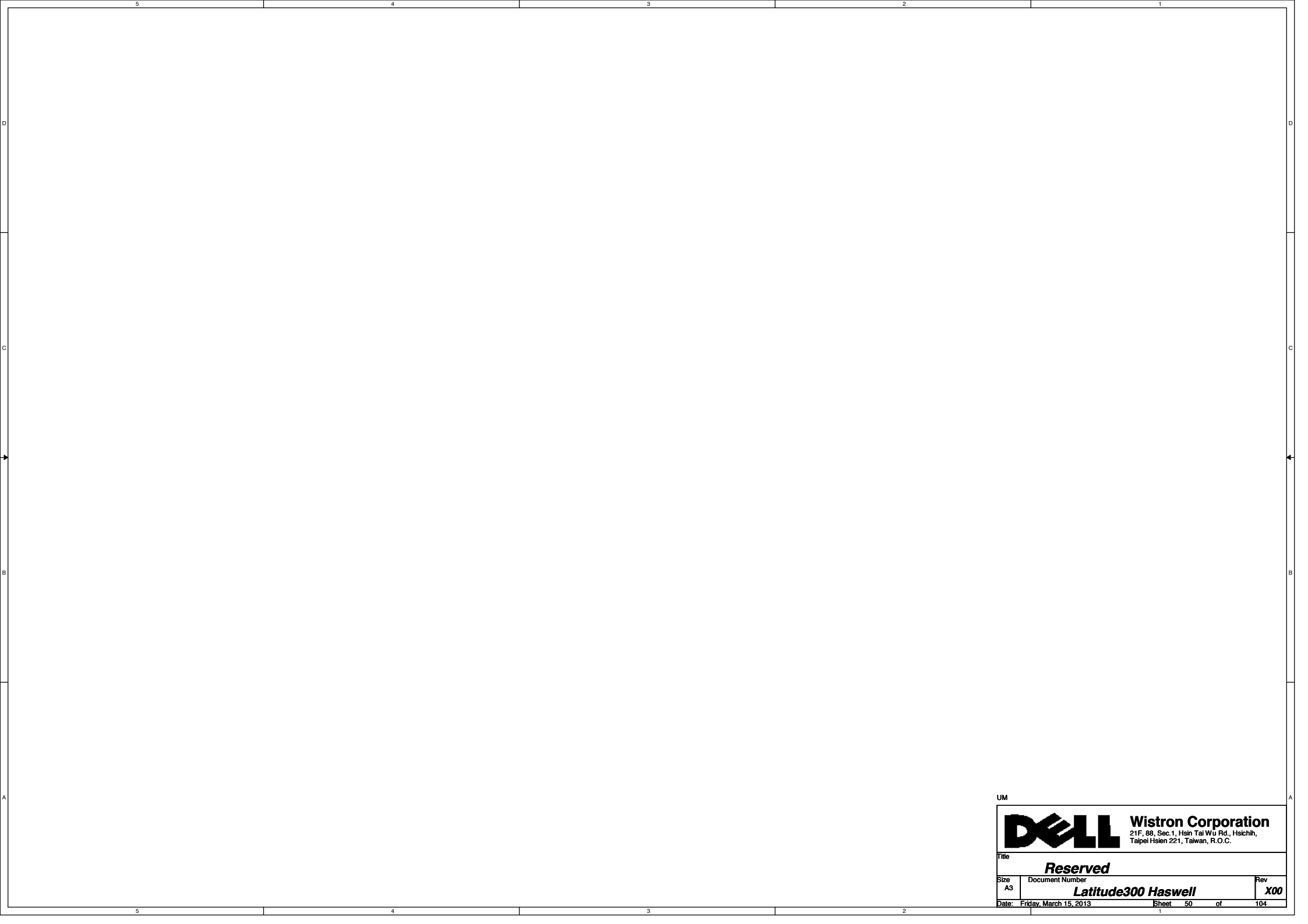
SSID = PWR.Plane.Regulator_lp35v0p675v



State	S3	S5	VDDR	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off(Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

MODE	Frequency	Discharge Mode
PR4608	400kHz	Tracking Discharge
200k ohm	400kHz	
100k ohm	300kHz	
68k ohm	300kHz	Non-tracking Discharge
47k ohm	400kHz	

I/P cap: 10U 25V K0805 X5R/ 78.10622.51L
 Inductor: CHIP IND 0.1UH M PCMC063T-R10MN 1.5-1.7mohm Isat =60Arms 68.R1010.10T
 O/P cap: CHIP CAP POL 330U 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L
 H/S MOS: FET MOS SIS412DN-T1-GE3 NC 8P / 84.00412.037 / Rds(on)=24-30mohm @Vgs=4.5V
 L/S MOS: FET MOS SIS780DN-T1-GE3 NC POWERPAK 121 / 84.00780.037 / Rds(on)=14.5-17.5mohm @Vgs=4.5V



UM

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A3

Document Number

Latitude300 Haswell

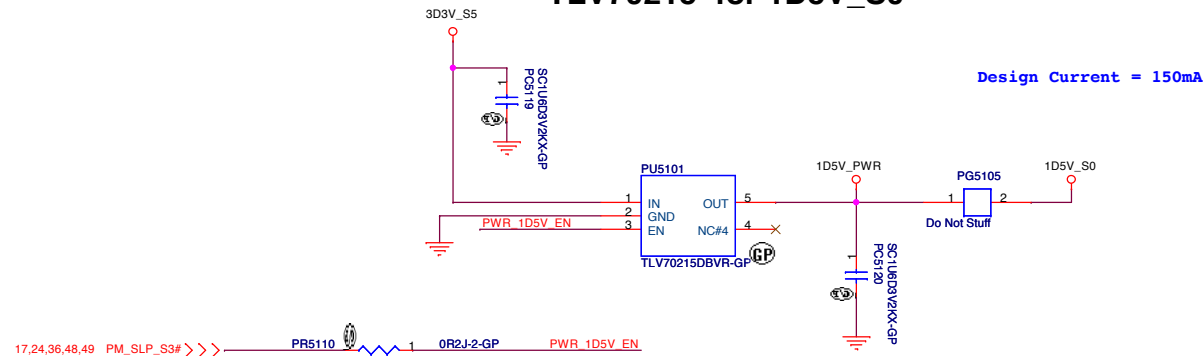
Rev

X00

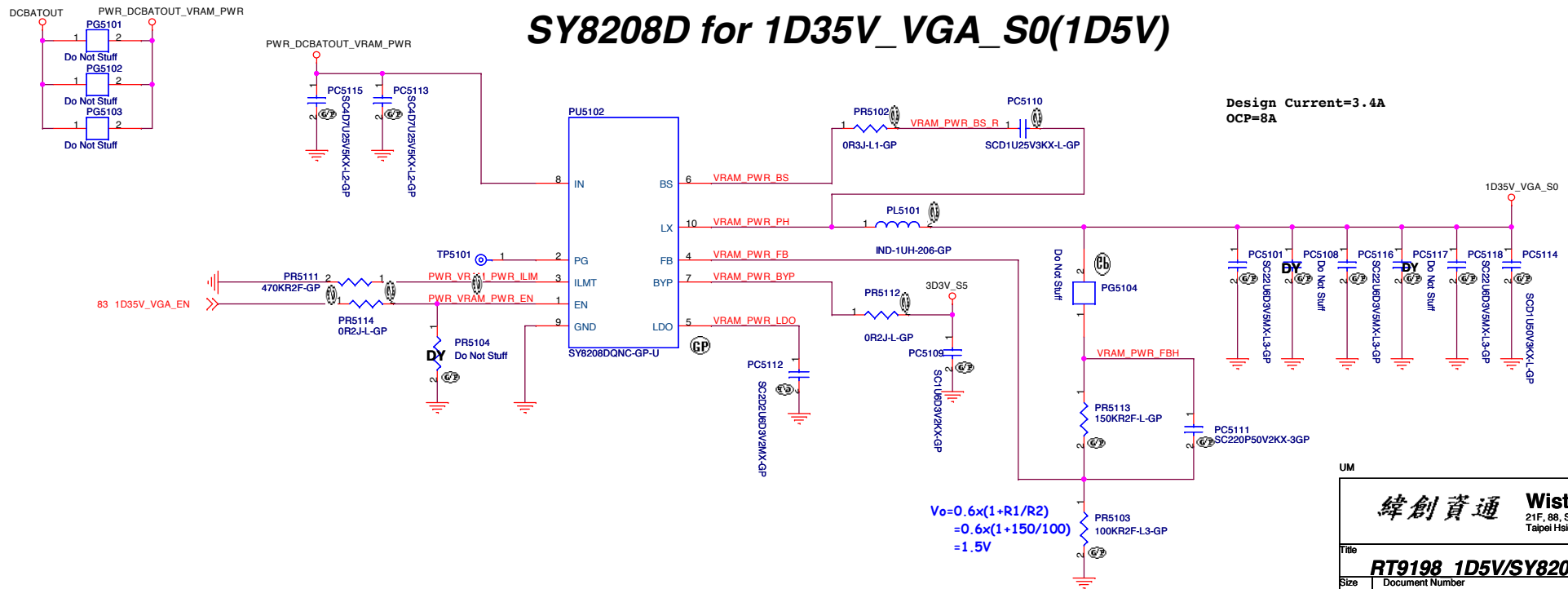
Date: Friday, March 15, 2013

Sheet 50 of 104

TLV70215 for 1D5V_S0



SY8208D for 1D35V_VGA_S0(1D5V)



$$V_o = 0.6 \times (1 + R1/R2) = 0.6 \times (1 + 150/100) = 1.5V$$

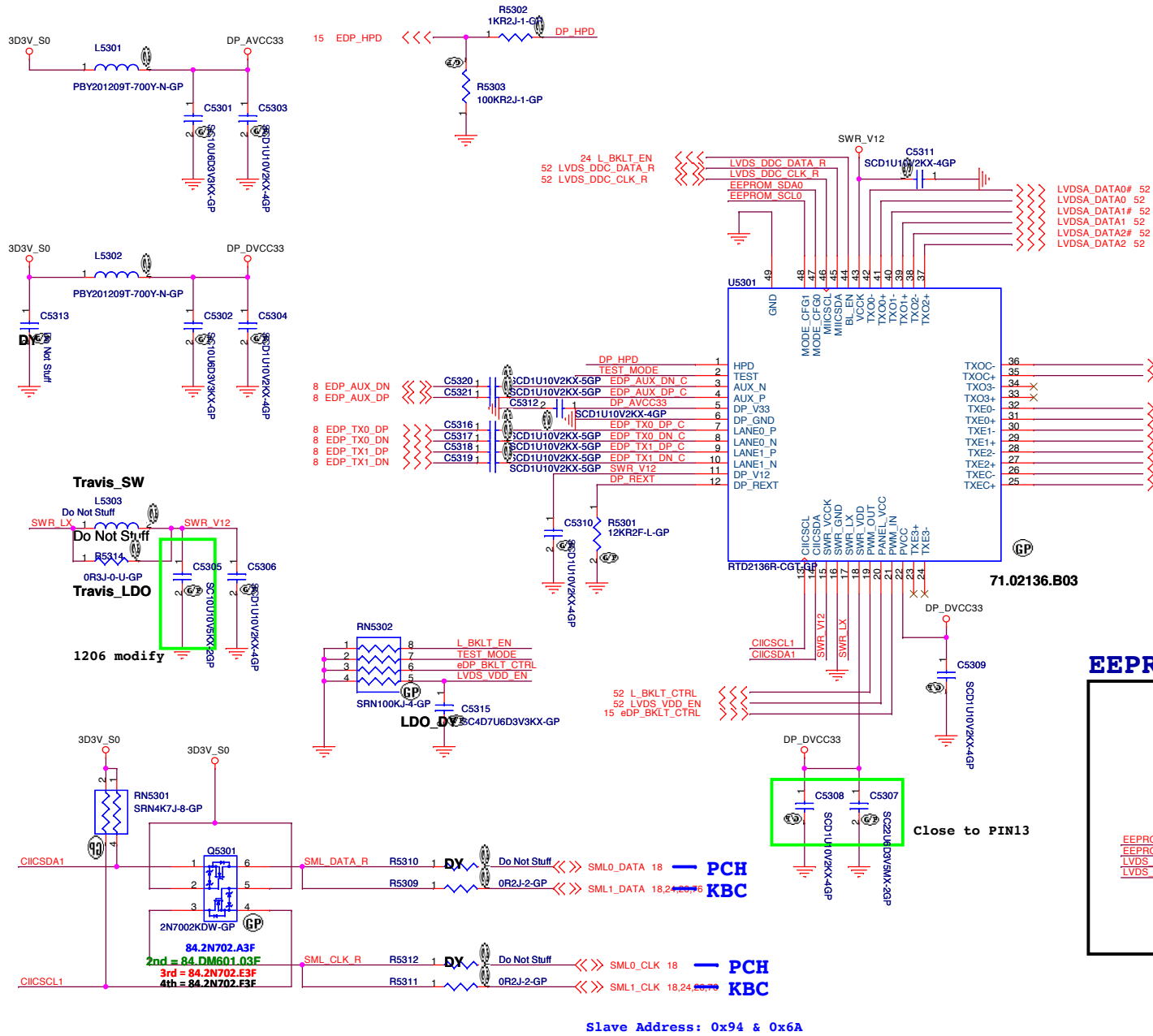
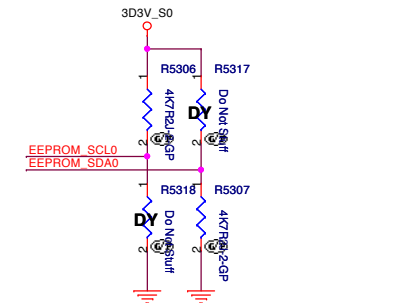
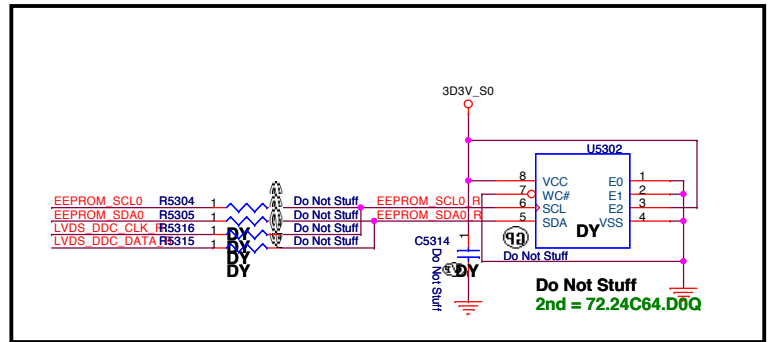


Table 2 Operation Mode Table

		PIN47	
		0	1
PIN48	0	X	EP Mode
	1	ROM	EEPROM



EEPROM



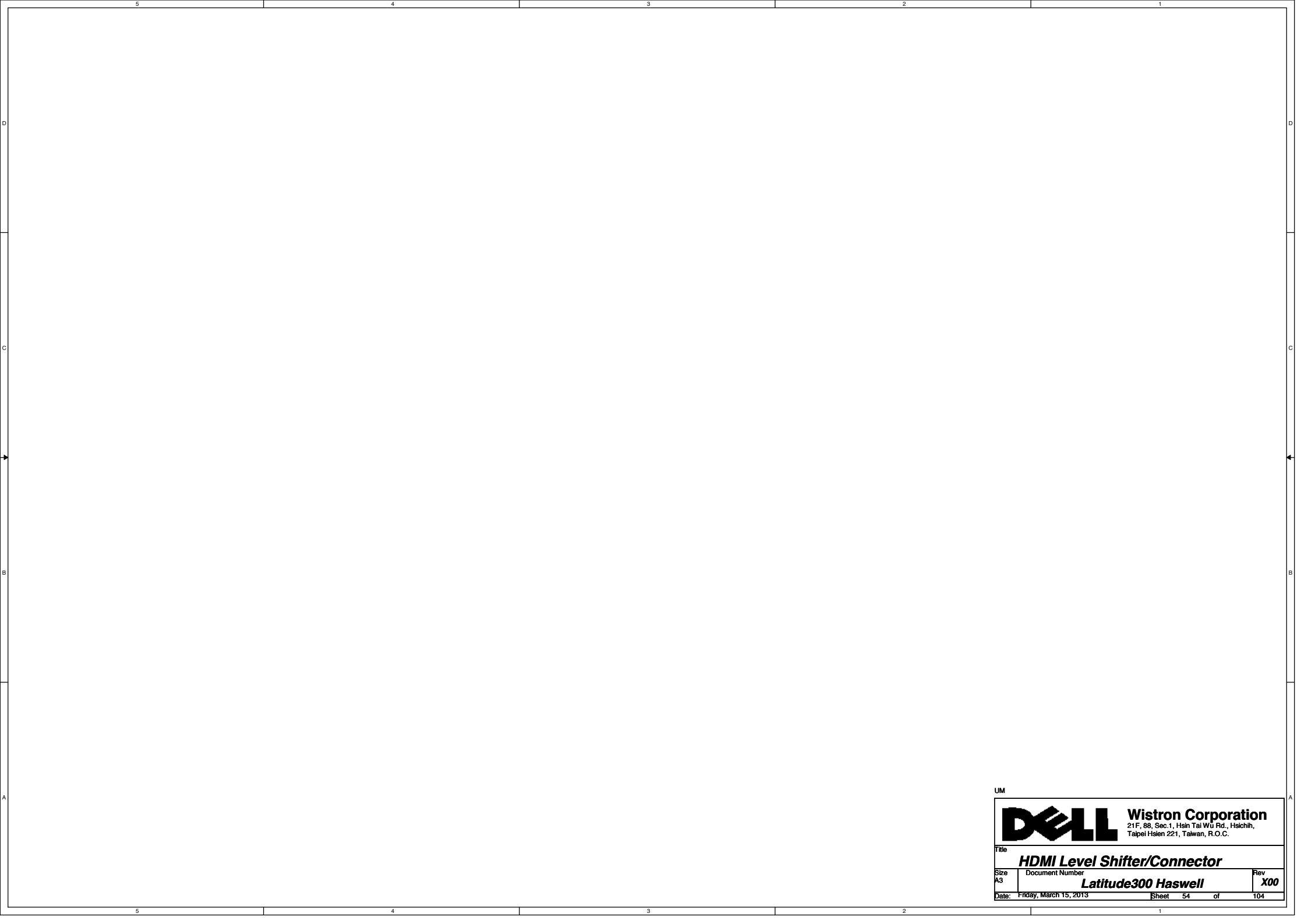
Close to PIN13

UM

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Title: **LVDS Switch**

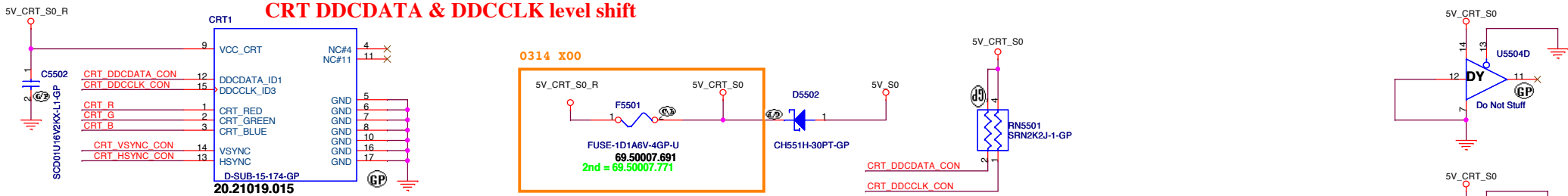
Size: A3	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet: 53 of 104	



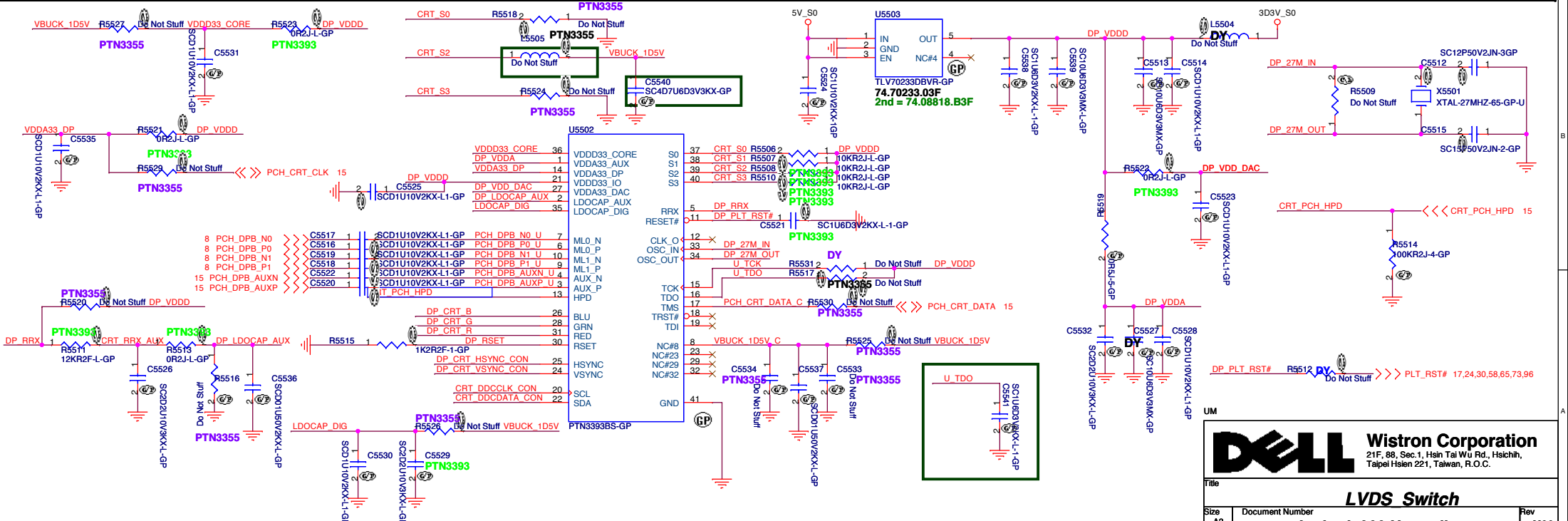
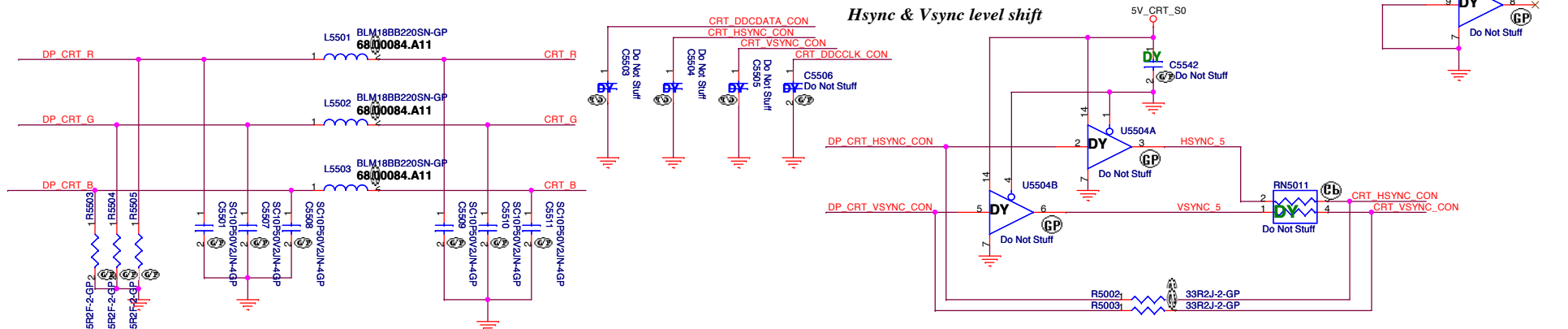
UM

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Title			
HDMI Level Shifter/Connector			
Size	Document Number	Rev	
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Date:	Friday, March 15, 2013	Sheet	54 of 104

CRT DDCDATA & DDCCLK level shift



Hsync & Vsync level shift



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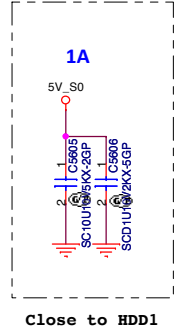
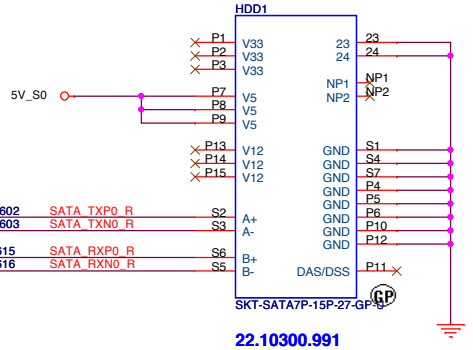
Document Number: **Latitude300 Haswell**

Rev: **X00**

Date: Friday, March 15, 2013 Sheet 55 of 104

SSID = SATA

SATA HDD Connector



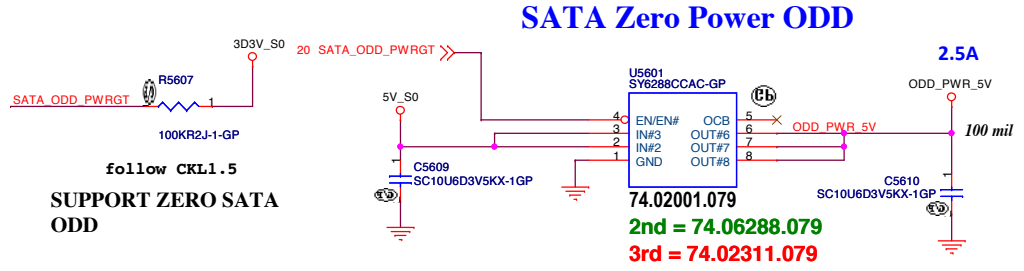
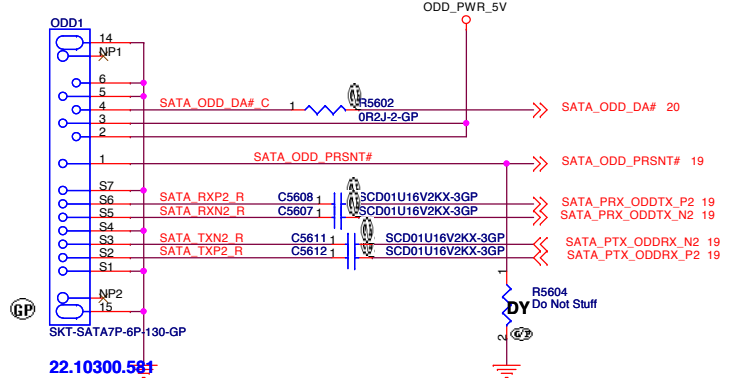
19 SATA3_PTX_HDDR_X_P0 >>> SCD01U16V2KX-3GP

19 SATA3_PTX_HDDR_X_N0 >>> SCD01U16V2KX-3GP

19 SATA3_PRX_HDDR_X_P0 >>> SCD01U16V2KX-3GP

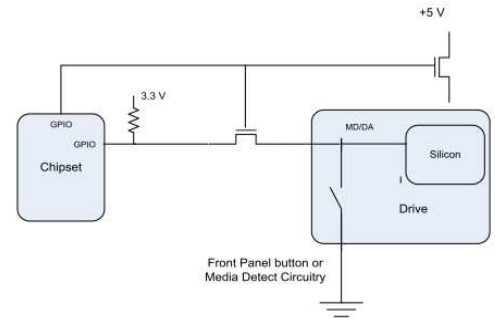
19 SATA3_PRX_HDDR_X_N0 >>> SCD01U16V2KX-3GP

ODD Connector



follow CKL1.5
SUPPORT ZERO SATA
ODD


Current limit
Active High
typ => 2.5A



SSID = ESATA

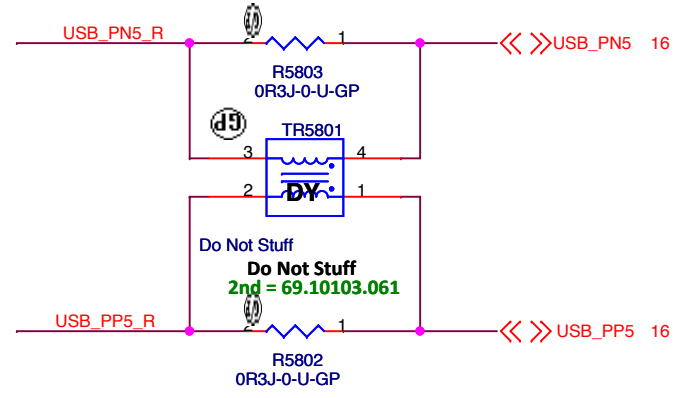
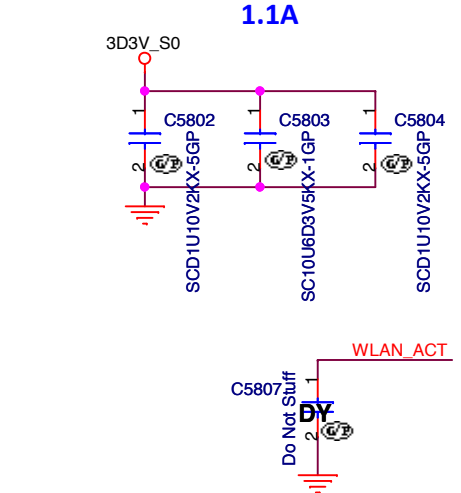
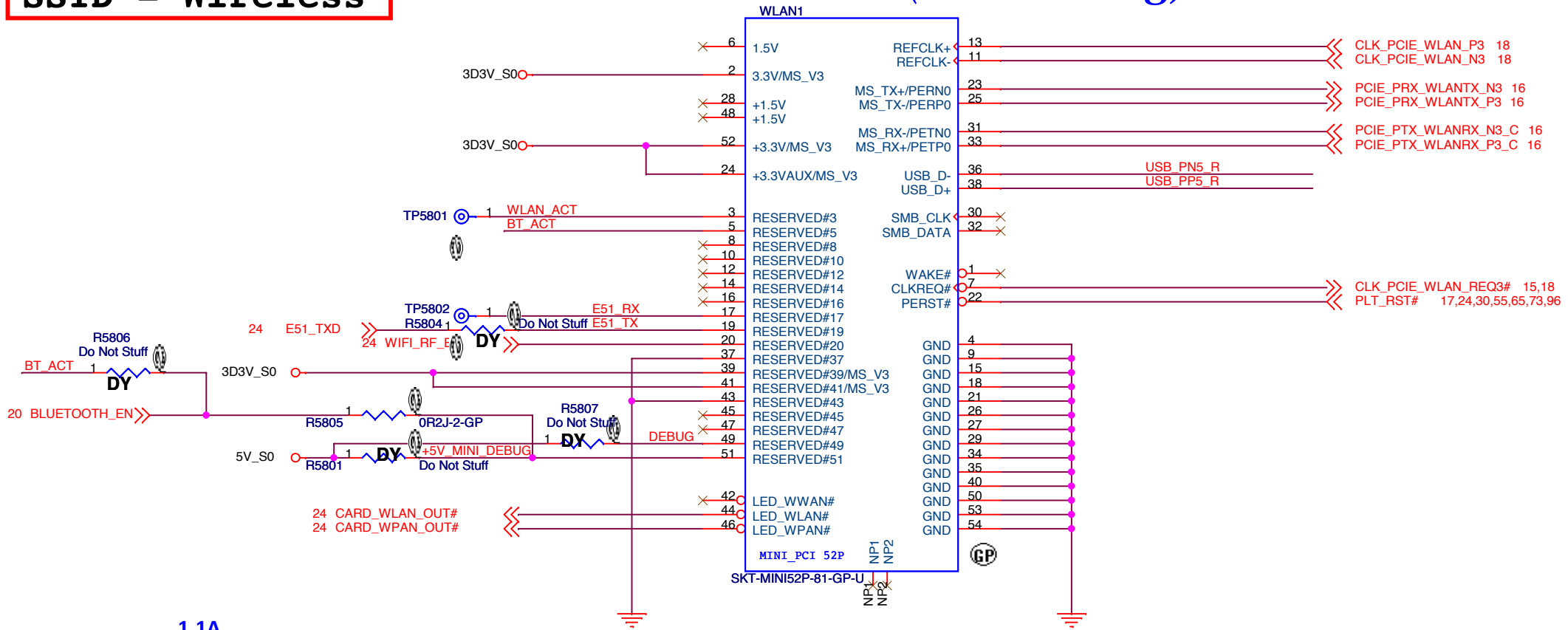
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UM

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Title		ESATA
Size A3	Document Number Latitude300 Haswell	Rev X00
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SSID = Wireless

Mini Card Connector(802.11a/b/g)



UM


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Title: **MINICARD(WLAN)/TP CONN**

Size: A4	Document Number: Latitude300 Haswell	Rev: X00
Date: Friday, March 15, 2013	Sheet: 58	of 104

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Title		
Reserved		
Size A3	Document Number Latitude300 Haswell	Rev X00
Date: Friday, March 15, 2013	Sheet 59	of 104

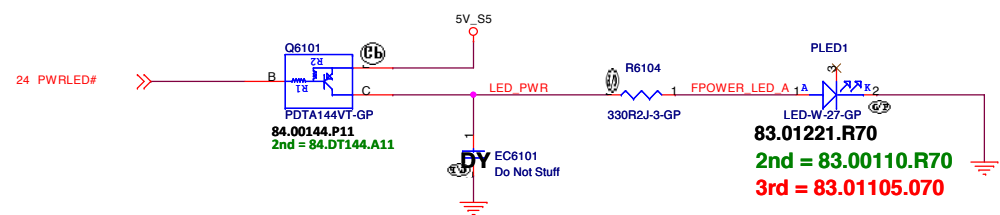
SSID = PCH

UM

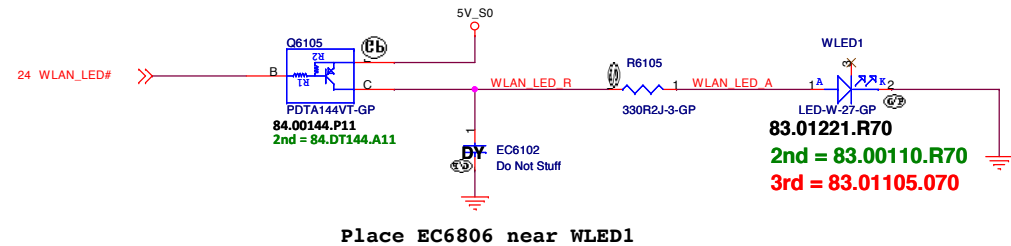
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title (Reserved)		
Size A4	Document Number Latitude300 Haswell	Rev X00
Date: Friday, March 15, 2013	Sheet 60 of	104

SSID = User.Interface

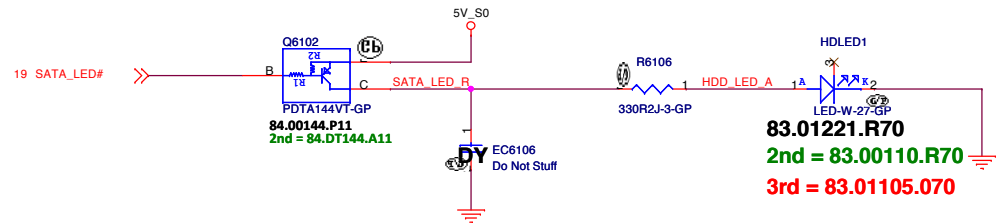
FRONT POWER LED
Low actived from KBC GPIO



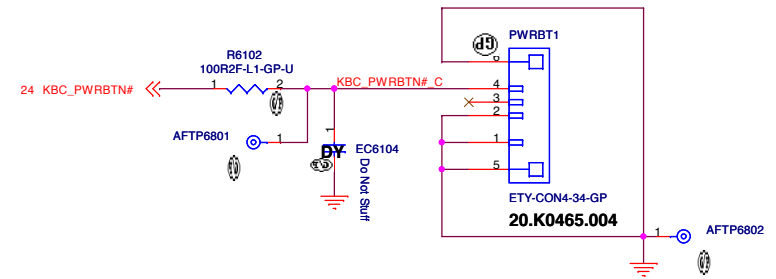
Wireless LED
Low actived from KBC GPIO



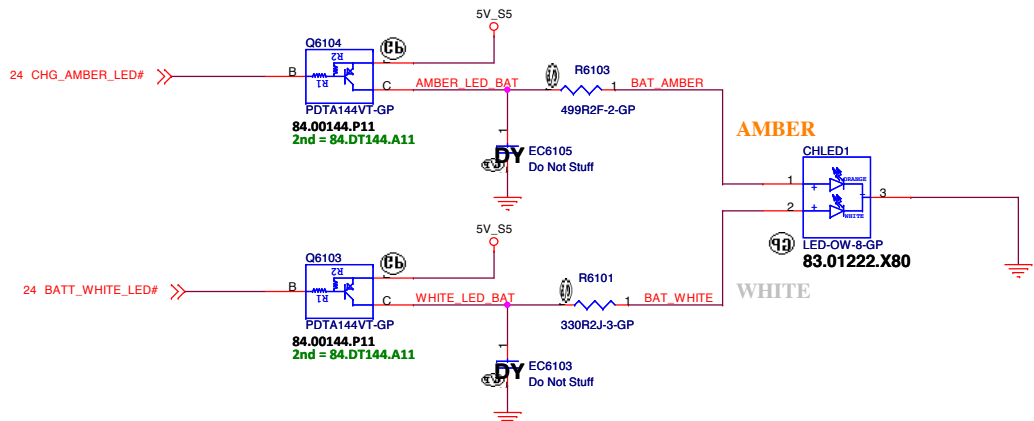
SATA HDD LED(White)
Low actived from PCH GPIO



Power button



Battery LED1 (AMBER_LED)
Low actived from KBC GPIO



Battery LED2 (WHITE_LED)
Low actived from KBC GPIO

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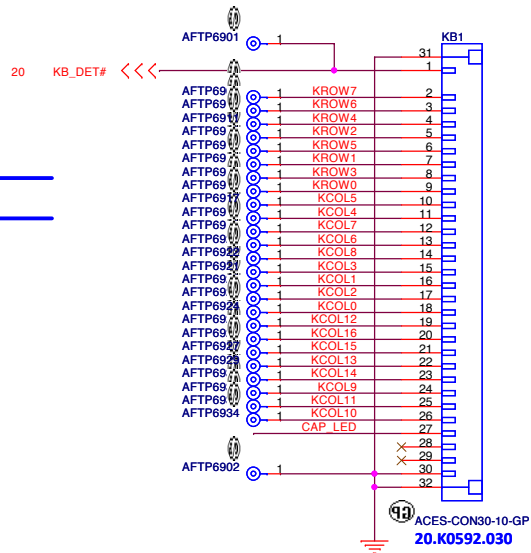
Title: **LED Bard/Power Button**

Size A3 Document Number **Latitude300 Haswell** Rev **X00**

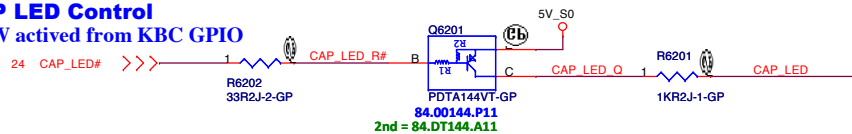
Date: Friday, March 15, 2013 Sheet 61 of 104

SSID = KBC

Internal Keyboard Connector

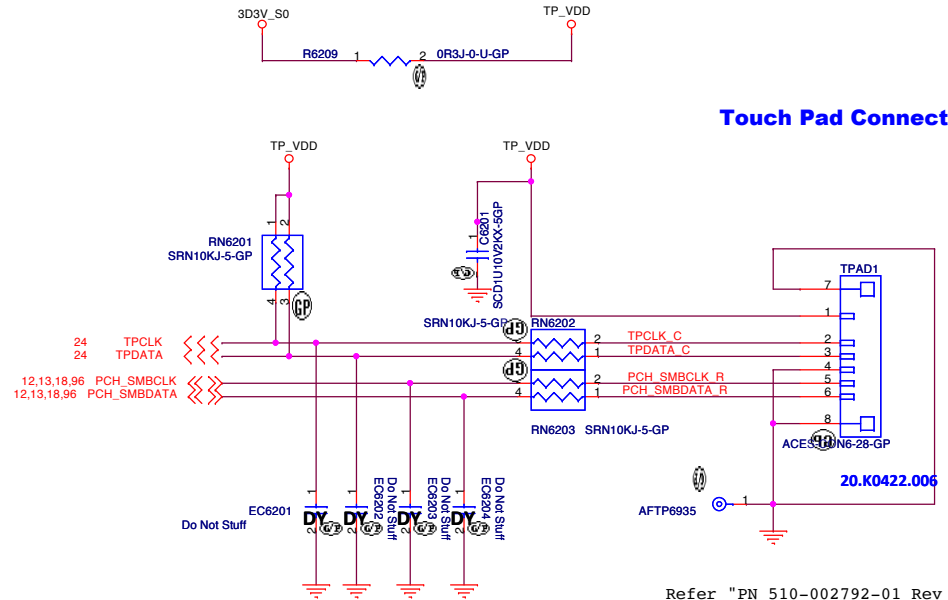


CAP LED Control
LOW acted from KBC GPIO



SSID = Touch.Pad

Touch Pad Connector



Refer "PN 510-002792-01 Rev 2" module spec

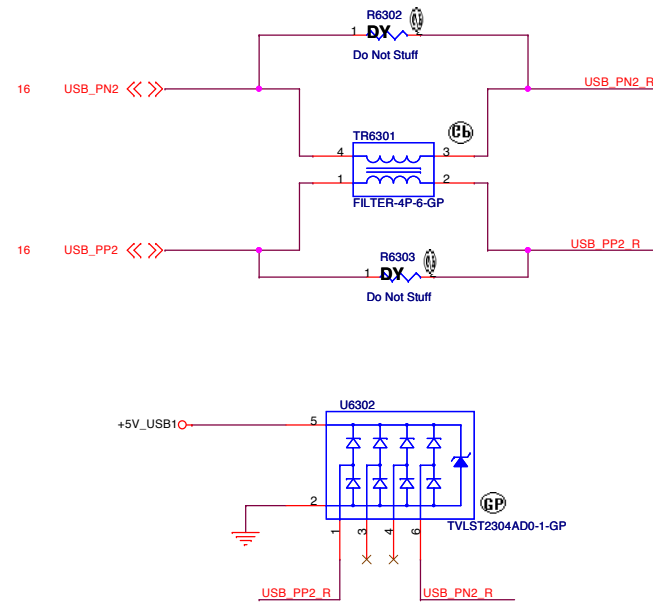
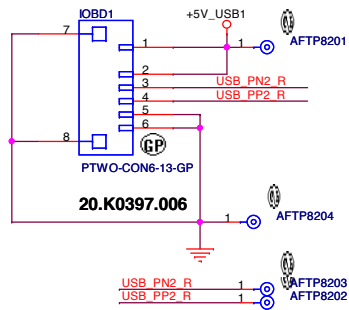
Pin number	Pin name
1	VDD
2	PS2_CLK
3	PS2_DATA
4	GND
5	SMBUS_CLK
6	SMBUS_DATA

UM



Title Key Board/Touch Pad		
Size A3	Document Number Latitude300 Haswell	Rev X00
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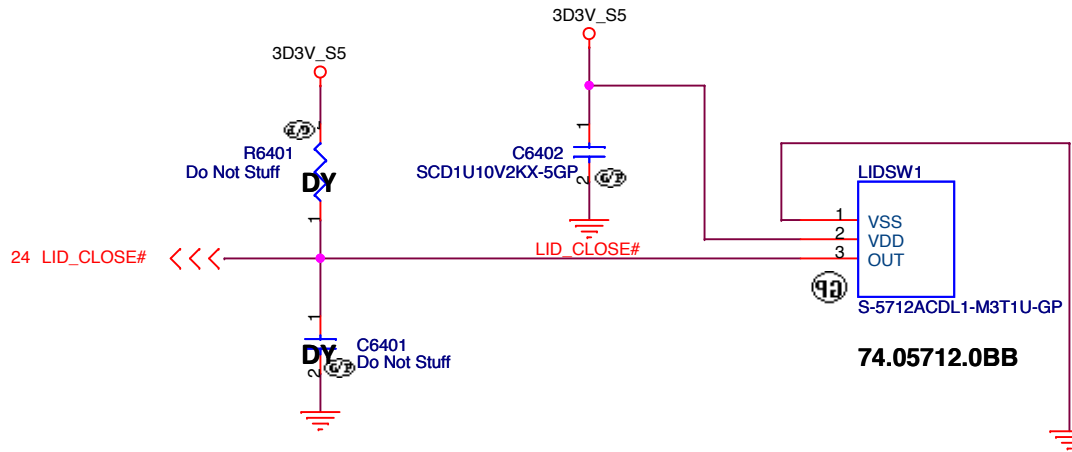
SSID = User.Interface




UM

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		21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
IO Board Connector			
Size	Document Number	Rev	
A3	Latitude300 Haswell	X00	
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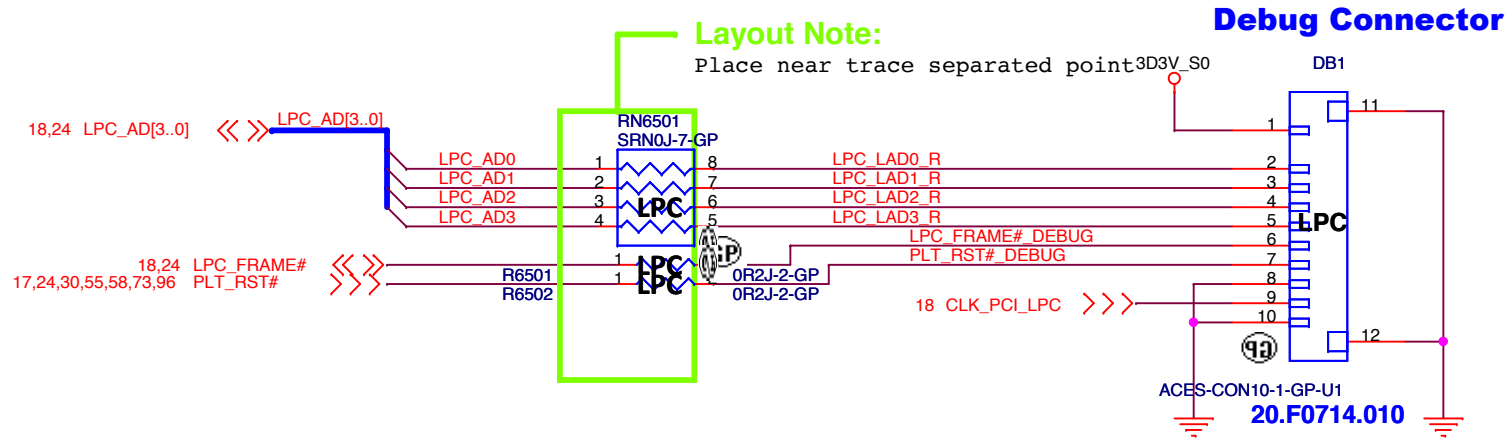
SSID = User.Interface



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Title Hall Sensor		
Size A4	Document Number Latitude300 Haswell	Rev X00
Date: Friday, March 15, 2013	Sheet 64 of 104	

SSID = DEBUG PORT




UM

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Title			
Dubug connector			
Size A4	Document Number Latitude300 Haswell		Rev X00
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Title		
Reserved		
Size A3	Document Number Latitude300 Haswell	Rev X00
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UM

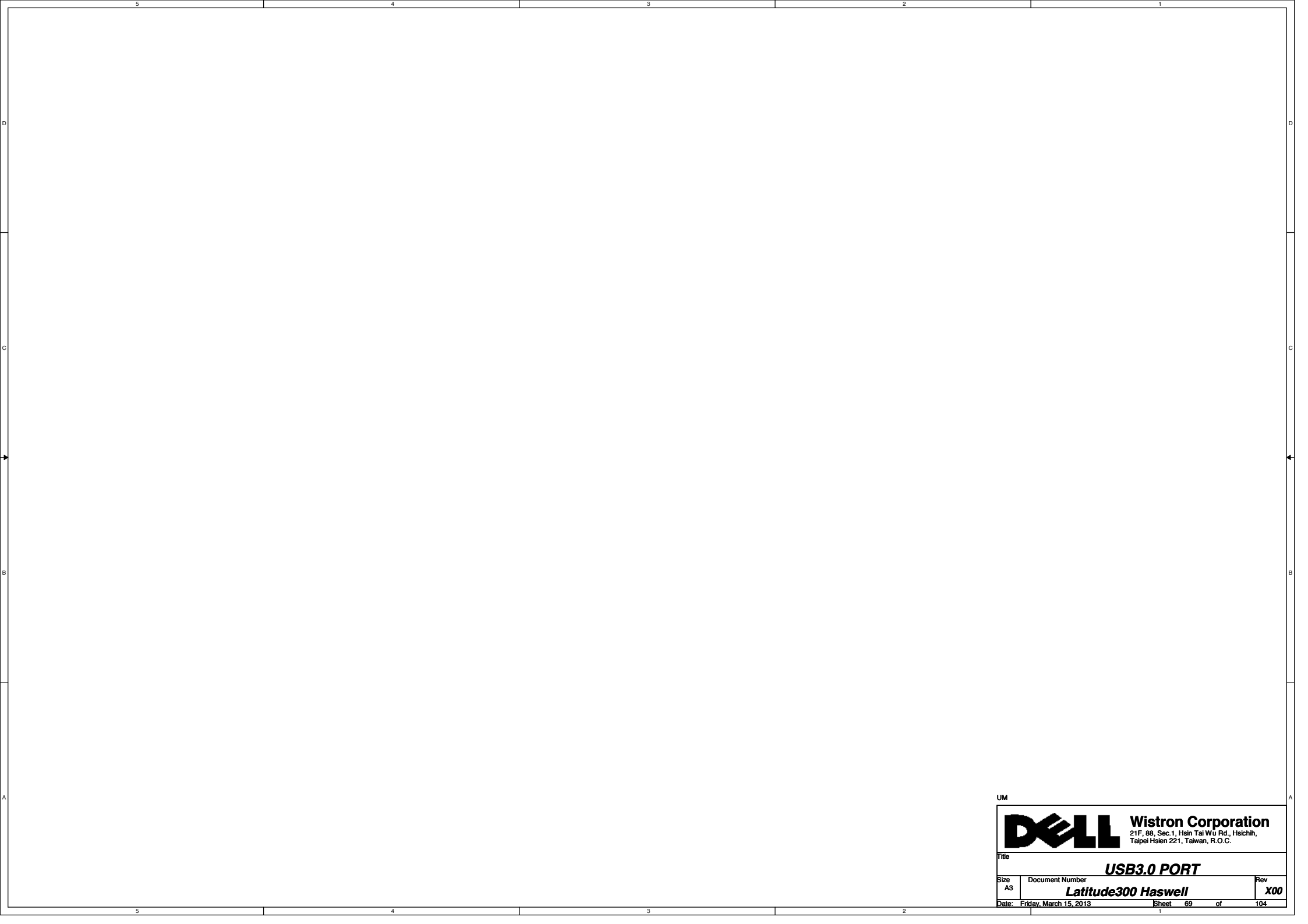


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Size	Document Number	Rev
A3	Latitude300 Haswell	X00
Date: Friday, March 15, 2013	Sheet 67	of 104


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UM

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Title		
RESERVED		
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UM

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB3.0 PORT			
Size	Document Number	Rev	
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UM

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Title		
Reserved		
Size A3	Document Number Latitude300 Haswell	Rev X00
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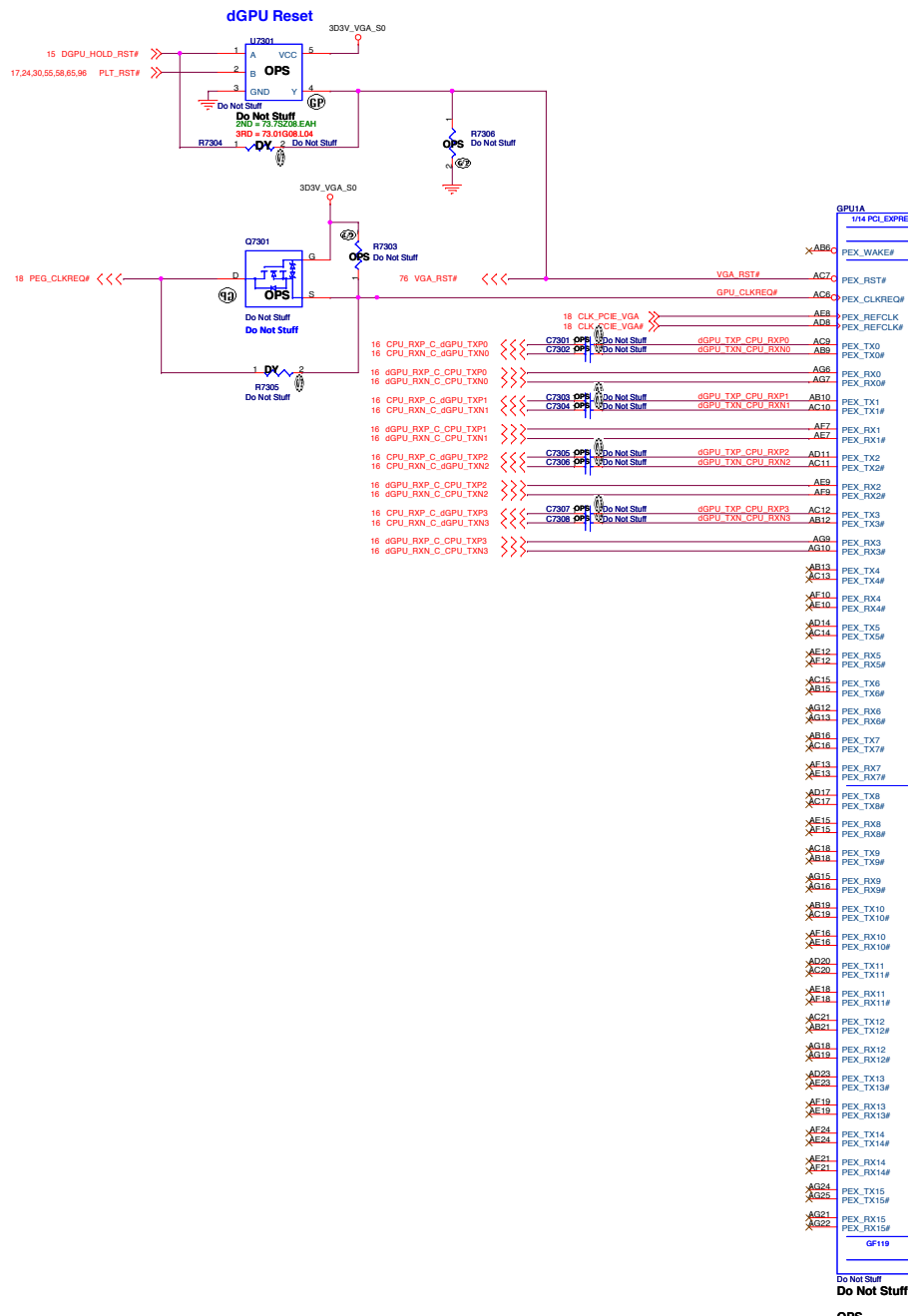
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Reserved		
Size A3	Document Number Latitude300 Haswell	Rev X00
Date: Friday, March 15, 2013	Sheet 71	of 104

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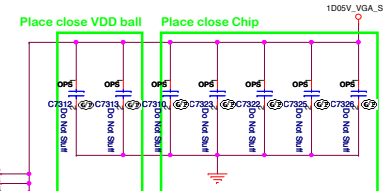
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		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
Reserved		
Size A3	Document Number Latitude300 Haswell	Rev X00
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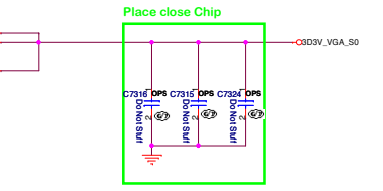
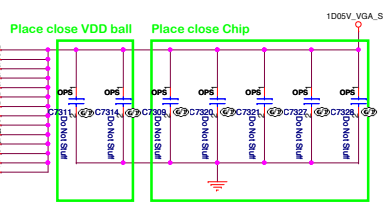


GPU1A	104 PCL_EXPRESS	1 OF 14
XABB	GPU_WAKE#	NC
AC7C	PEX_RST#	NC
AC8C	GPU_CLKREQ#	NC
AE8	PEX_REFCLK#	NC
AD8	PEX_REFCLK#	NC
AC9	PEX_TX0	NC
AB9	PEX_TX0#	NC
AG8	PEX_RX0	NC
AG7	PEX_RX0#	NC
AB10	PEX_TX1	NC
AC10	PEX_TX1#	NC
AE7	PEX_RX1	NC
AE7	PEX_RX1#	NC
AD11	PEX_TX2	NC
AC11	PEX_TX2#	NC
AE9	PEX_RX2	NC
AE9	PEX_RX2#	NC
AC12	PEX_TX3	NC
AB12	PEX_TX3#	NC
AG9	PEX_RX3	NC
AG10	PEX_RX3#	NC
AB13	PEX_TX4	NC
AC13	PEX_TX4#	NC
AE10	PEX_RX4	NC
AE10	PEX_RX4#	NC
AD14	PEX_TX5	NC
AC14	PEX_TX5#	NC
AE12	PEX_RX5	NC
AE12	PEX_RX5#	NC
AC15	PEX_TX6	NC
AB15	PEX_TX6#	NC
AG12	PEX_RX6	NC
AG13	PEX_RX6#	NC
AB16	PEX_TX7	NC
AC16	PEX_TX7#	NC
AE13	PEX_RX7	NC
AE13	PEX_RX7#	NC
AD17	PEX_TX8	NC
AC17	PEX_TX8#	NC
AE15	PEX_RX8	NC
AE15	PEX_RX8#	NC
AC18	PEX_TX9	NC
AB18	PEX_TX9#	NC
AG15	PEX_RX9	NC
AG16	PEX_RX9#	NC
AB19	PEX_TX10	NC
AC19	PEX_TX10#	NC
AE16	PEX_RX10	NC
AE16	PEX_RX10#	NC
AD20	PEX_TX11	NC
AC20	PEX_TX11#	NC
AE18	PEX_RX11	NC
AE18	PEX_RX11#	NC
AC21	PEX_TX12	NC
AB21	PEX_TX12#	NC
AG18	PEX_RX12	NC
AG19	PEX_RX12#	NC
AD23	PEX_TX13	NC
AE19	PEX_TX13#	NC
AE19	PEX_RX13	NC
AE19	PEX_RX13#	NC
AE24	PEX_TX14	NC
AE24	PEX_TX14#	NC
AE21	PEX_RX14	NC
AE21	PEX_RX14#	NC
AG24	PEX_TX15	NC
AG25	PEX_TX15#	NC
AG21	PEX_RX15	NC
AG22	PEX_RX15#	NC
GF119	GF117	NC
GF119	GF108	NC

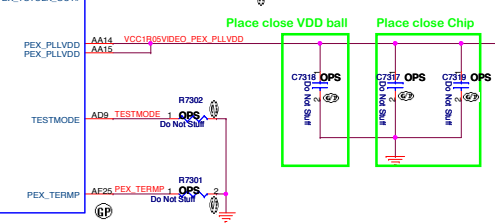
Do Not Stuff
Do Not Stuff
OPS



1.05V +/- 30mV
3.3A

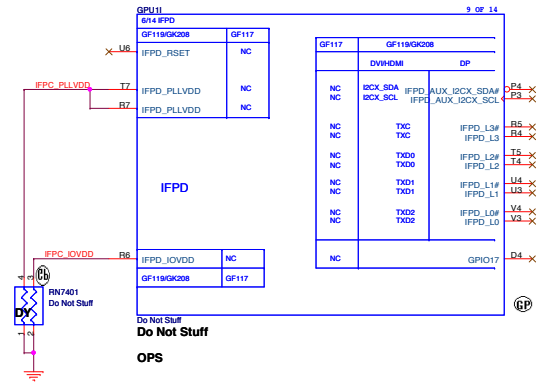
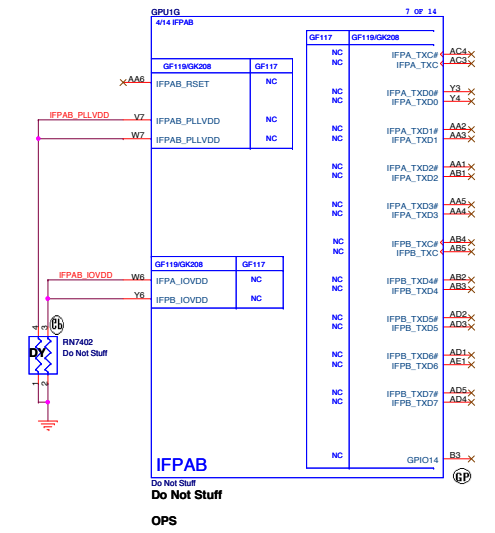


3.3V +/- 5%
210mA

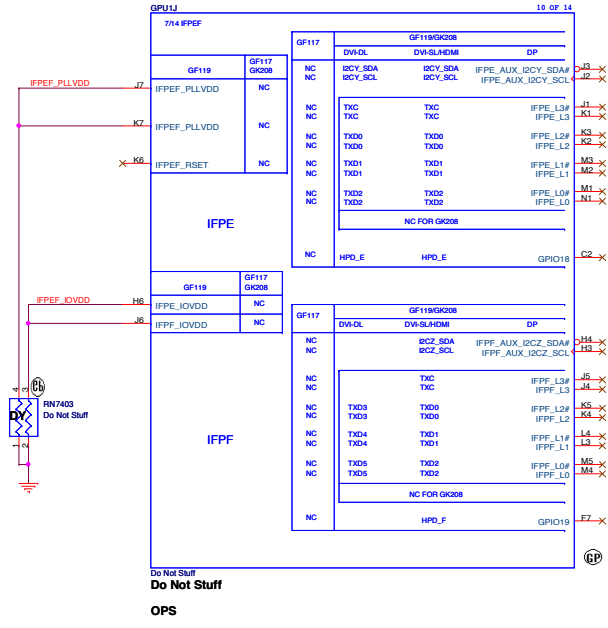
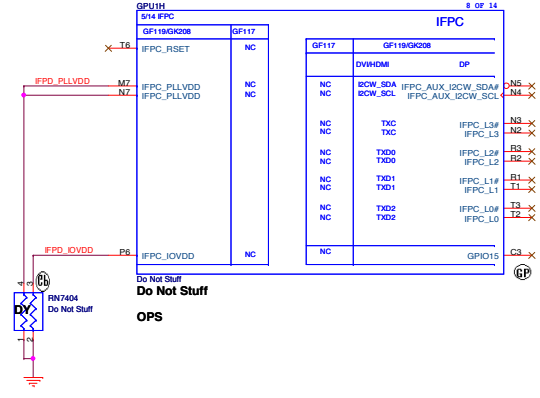


1.05V +/- 30mV
150mA

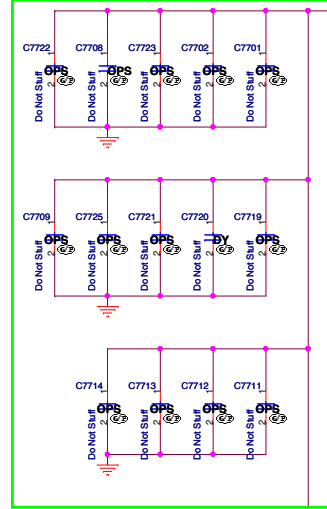
LVDS Interface



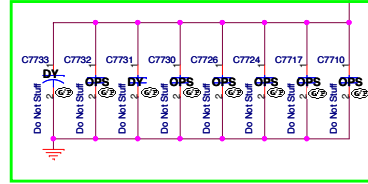
HDMI Interface



Under GPU

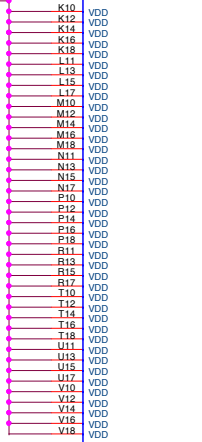


Near GPU



VGA_CORE

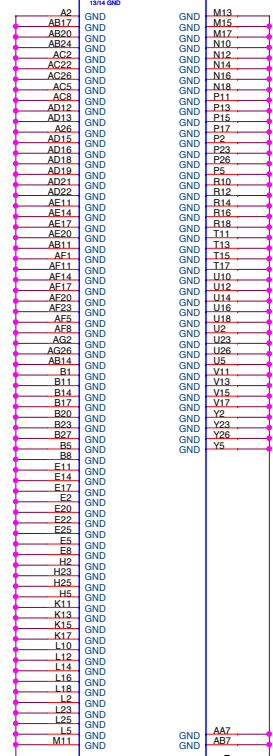
GPU1E 5 OF 14



Do Not Stuff

OPS

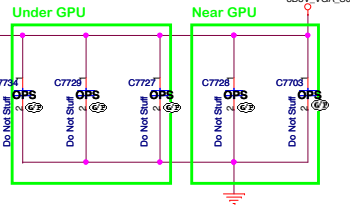
GPU1F 6 OF 14



Do Not Stuff

OPS

3.3V +/- 5%
85mA



303V_VGA_S0

GPU1C 3 OF 14



- X AD10 NCFAD10
- X AD7 NCFAD7
- X B19 NCFB19
- F11 3V3AUX
- V5 NCFV5
- V6 NCFV6
- G1 NCF#G1
- G2 NCF#G2
- G3 NCF#G3
- G4 NCF#G4
- G5 NCF#G5
- G6 NCF#G6
- G7 NCF#G7
- V1 NCF#V1
- V2 NCF#V2
- W1 NCF#W1
- W2 NCF#W2
- W3 NCF#W3
- W4 NCF#W4

Do Not Stuff

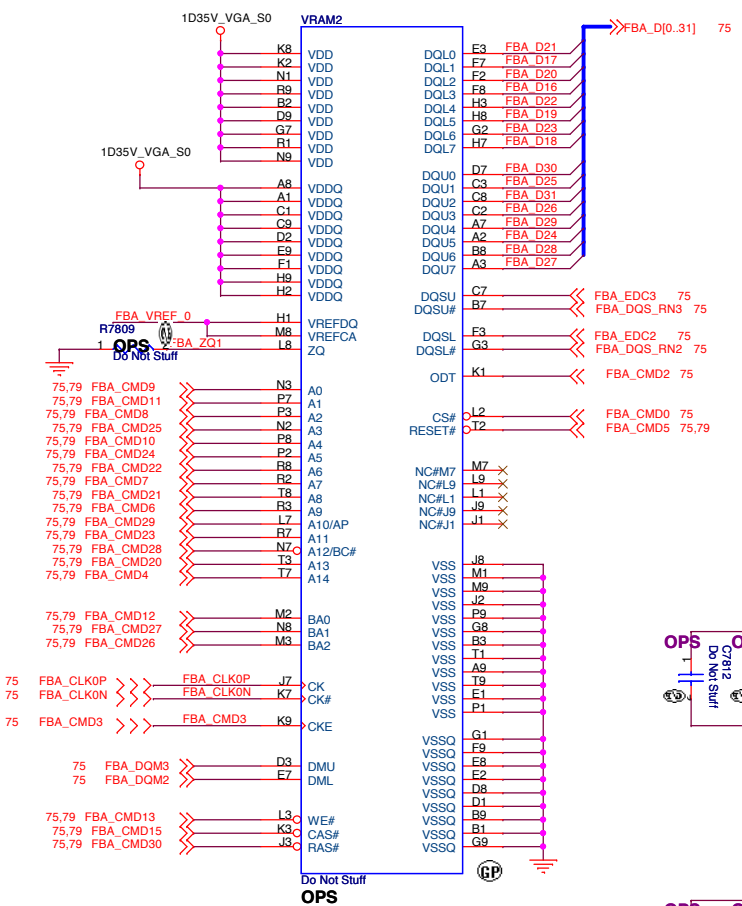
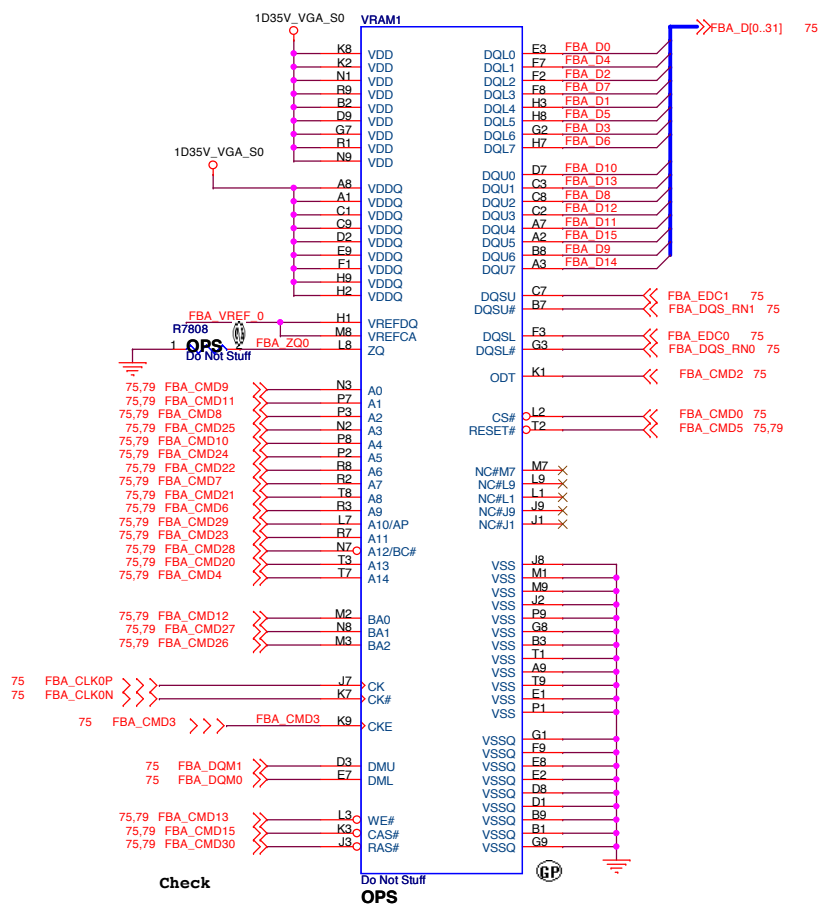
Do Not Stuff

OPS

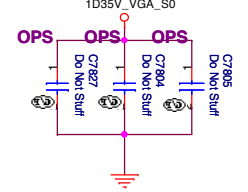
UM

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Taipei Hsien 221, Taiwan, R.O.C.

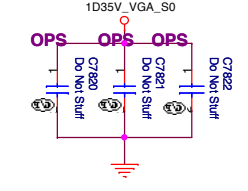
Title GPU_DPPWR/GND(5/5)		
Size	Document Number	Rev
Custom	Latitude300 Haswell	X00
Date: Friday, March 15, 2013	Sheet 77	of 104



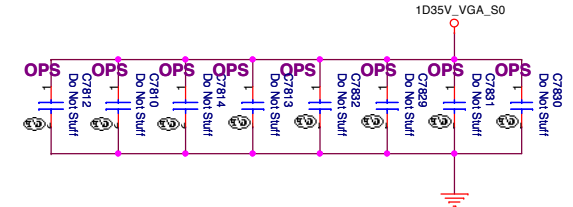
Place close VRAM1 VDD ball



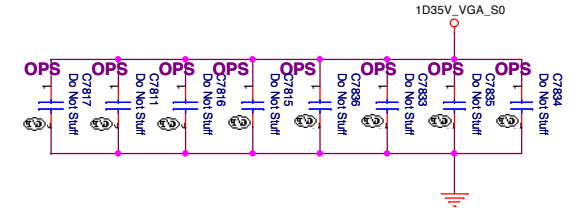
Place close VRAM2 VDD ball



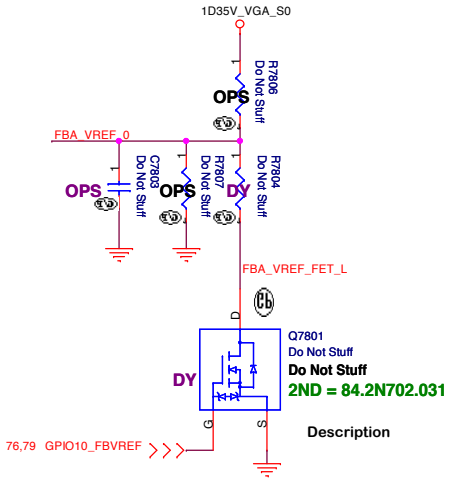
Place close VRAM1VDDQ ball



Place close VRAM1VDDQ ball



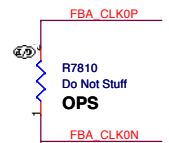
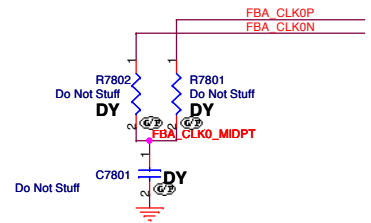
Frame Buffer Partition A-Lower Half



FBVREF Termination

Type	FBVREF%	Voltage	GPU_GPIO10
Un-termination	50%	0.749V	High
Termination	70%	1.0617V	Low

FBCLK Termination place on VRAM side

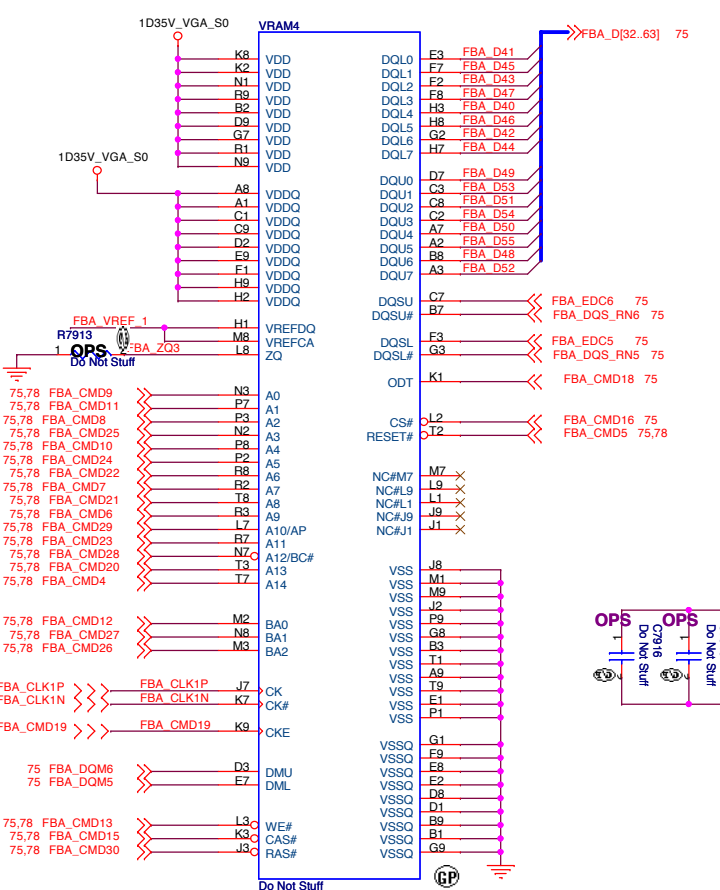
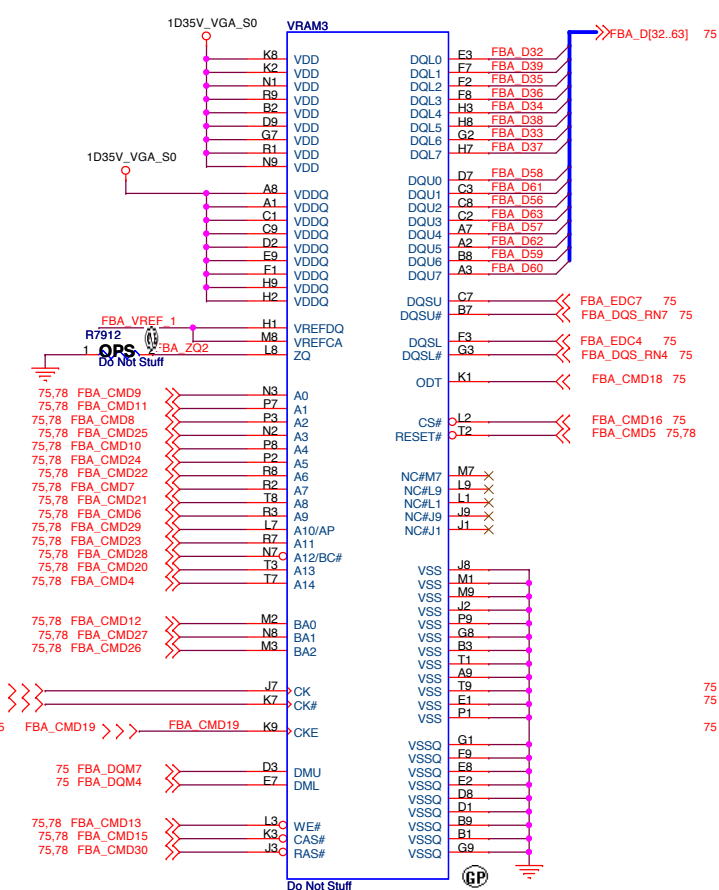


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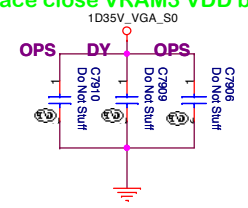
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Title: **GPU-VRAM1,2 (1/4)**

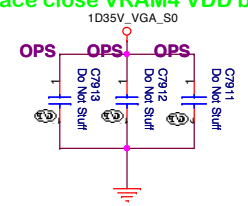
Size A3	Document Number	Rev
Date: Friday, March 15, 2013	Latitude300 Haswell	X00
Sheet 78 of 104		



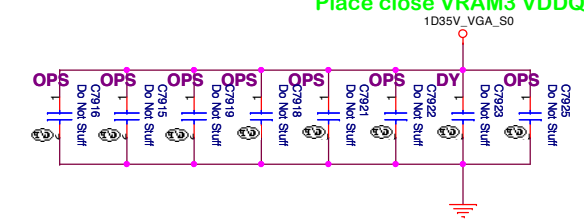
Place close VRAM3 VDD ball



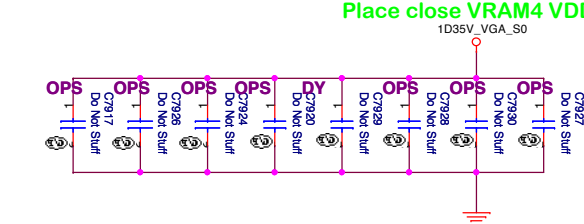
Place close VRAM4 VDD ball



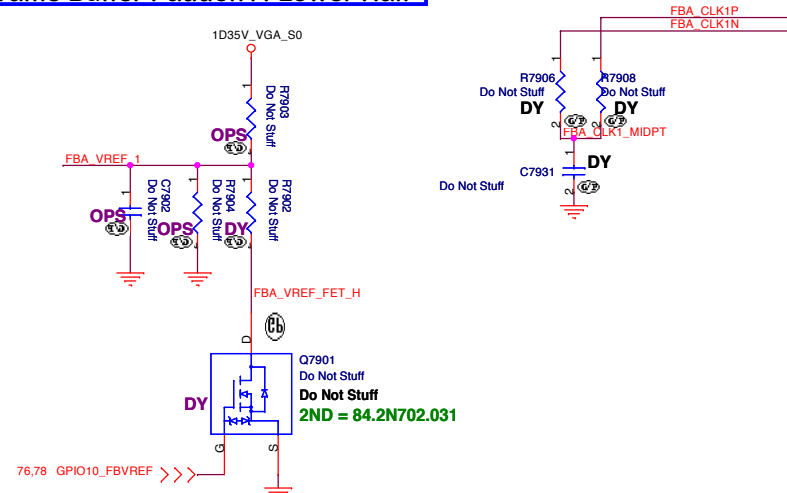
Place close VRAM3 VDDQ ball



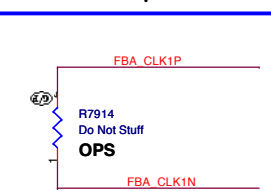
Place close VRAM4 VDDQ ball



Frame Buffer Partition A-Lower Half



FBCLK Termination place on VRAM side



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Title: **GPU-VRAM3,4 (2/4)**

Size A3	Document Number	Rev
	Latitude300 Haswell	X00
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Title			
GPU-VRAM5,6 (3/4)			
Size	Document Number	Rev	
A3	Latitude300 Haswell	X00	
Date: Friday, March 15, 2013		Sheet 80	of 104

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Title		
GPU-VRAM7,8 (4/4)		
Size	Document Number	Rev
A3	Latitude300 Haswell	X00
Date: Friday, March 15, 2013	Sheet 81	of 104

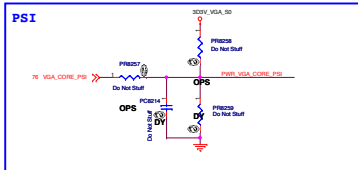
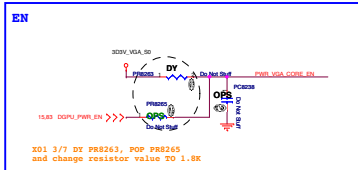
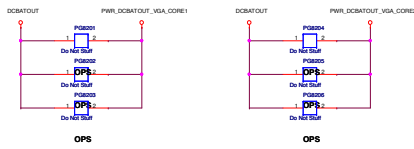
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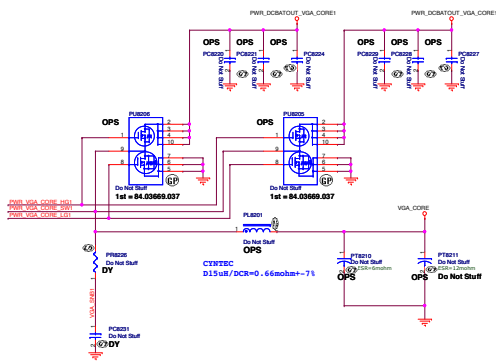
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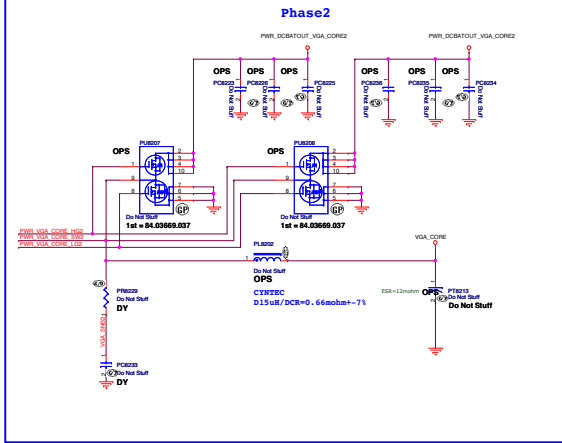
1



Phase1

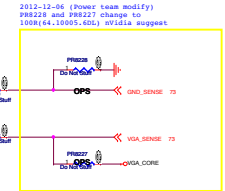
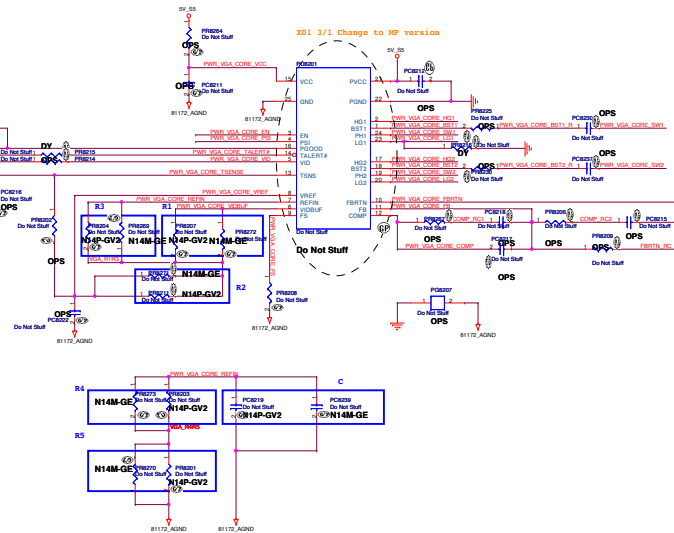


I/P caps: 100 25V K8085 XSR/ 78.10622.511
 MOS: Q1: Id=10A, Rds(on)=8.13.2 mohm ; Q2: Id=17A, Rds(on)=3.6-5.2mohm 84.03669.037
 Inductor: CHIP CHOKER 0.22uH PCMB0637-R22MS 2.5-3mohm Isat=34Arms 68.R2210.20C
 O/P caps: CHIP CAP POL 3300 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L



I/P caps: 100 25V K8085 XSR/ 78.10622.511
 MOS: Q1: Id=10A, Rds(on)=8.13.2 mohm ; Q2: Id=17A, Rds(on)=3.6-5.2mohm 84.03669.037
 Inductor: CHIP CHOKER 0.22uH PCMB0637-R22MS 2.5-3mohm Isat=34Arms 68.R2210.20C
 O/P caps: CHIP CAP POL 3300 2.5V M 6.3*4.5 2.3Arms Matsuti/77.53371.18L

X01 3/1 Change to MP version



2012-12-06 (Power team modify)
 PWR021 and PWR027 change to
 100R(4.1000V,60K) W516A suggest

EDC=45A
 EDP=72A

TYPE	config	IDC	EDP	OCF	R1/PR8207	R2/PR8211	R3/PR8204	R4/PR8205	R5/PR8201	C/PC8219
N14M-GE	C	35A	41A		39kohm	30kohm	3kohm	24kohm	3kohm	1.8nF
N14P-GV2	B	32A	55A		20kohm	20kohm	2kohm	18kohm	0ohm	2.7nF
N14P-GT	B	45A	75A		20kohm	20kohm	2kohm	18kohm	0ohm	2.7nF

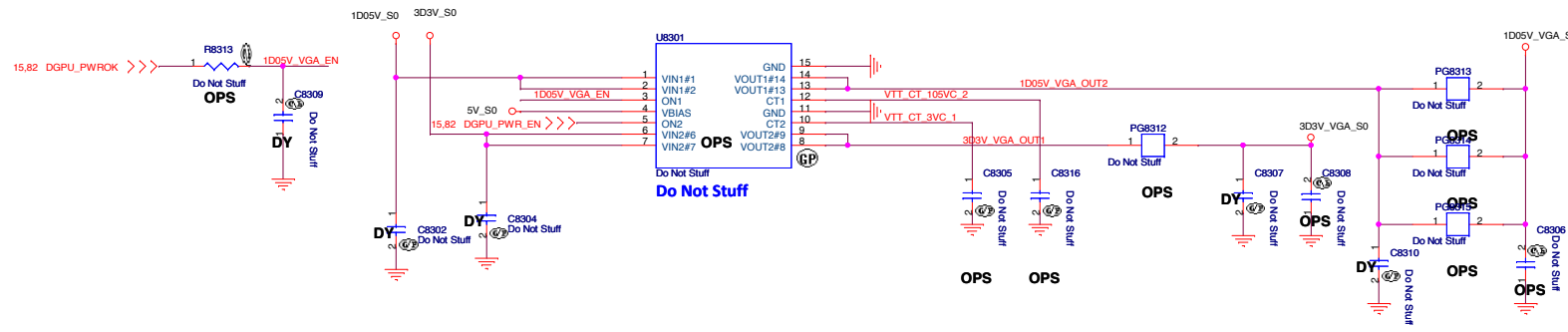
Table 1. PWM-VID Spec and Component Values

PWM-VID Spec	Config A	Config B	Config C
V _{min}	0.6	0.6	0.65
V _{max}	1.2	1.2	1.15
V _{boot}	0.875	0.9	0.9
Voltage Step V _{step}	mV 6.25	6.25	6.25
Number of Voltage Levels N	96	96	96
PWM Frequency F _{PWM}	MHz 1.125	1.125	0.676
PWM Minimum Pulse Width T _{min}	ns 9.26	9.26	74
VID Transient Time T	us <100	<100	<100
Component Value			
R1 (1%)	kΩ 39	20	39
R2 (1%)	kΩ 30	20	30
R3 (1%)	kΩ 1.5	2	3
R4 (1%)	kΩ 30	18	24
R5 (1%)	kΩ 1.5	0	3
C	nF 1.5	2.7	1.8

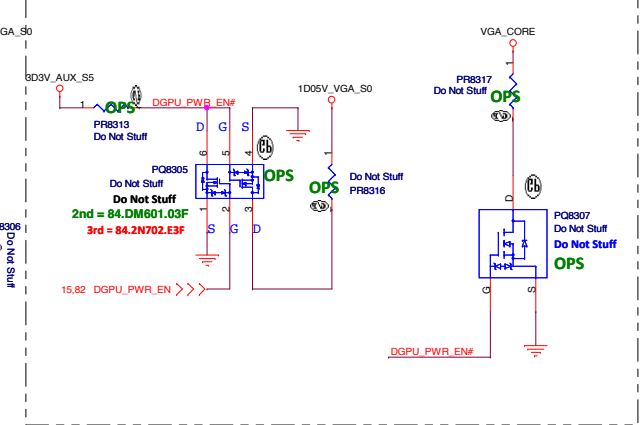
3D3V_VGA_S0 1D05V_VGA_S0

3D3V_VGA_S0 should ramp-up before VGA_Core
VGA_Core should ramp-up before 1D05V_VGA_S0
1D35V_VGA_S0 should ramp-up before 1D05V_VGA_S0

3D3V_S0 to 3D3V_VGA_S0 1D05V_S0 to 1D05V_VGA_S0

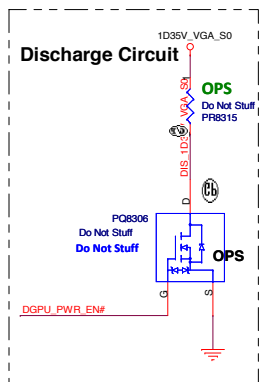
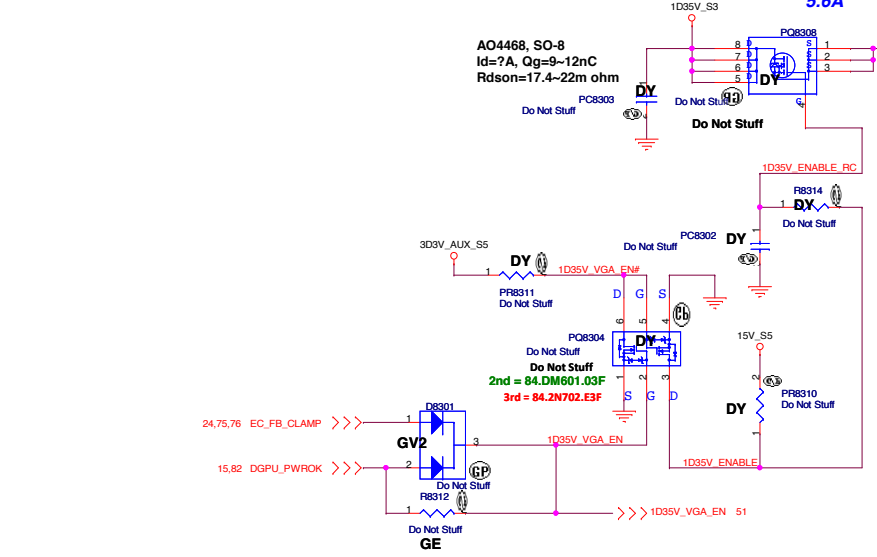


0307 Add Discharge Circuit



www.vinafix.vn

1D35V_VGA_S0



CTx (pF)	Rise Time (µs) 10% - 90%, COUT = 0.1µF @ VIN; VOUT=0 ohm load							
	Typical values @ 25°C, 25V X7R 10% ceramic cap							
	5V	3.3V	1.8V	1.5V	1.2V	1.05V	1V	0.8V
0	107	72	46	41	36	34	33	29
220	425	276	146	122	103	91	88	74
270	489	316	172	139	121	107	104	84
470	774	487	272	224	181	159	154	123
680	1108	708	375	317	242	221	213	168
1000	1561	1007	546	441	364	314	299	234
2200	3600	2289	1240	1019	817	681	665	539
4700	7757	5092	2674	2203	1808	1592	1516	1177
10000	15700	10310	5601	4659	3674	3401	3197	2562

Table 1. Rise time vs. CTx value

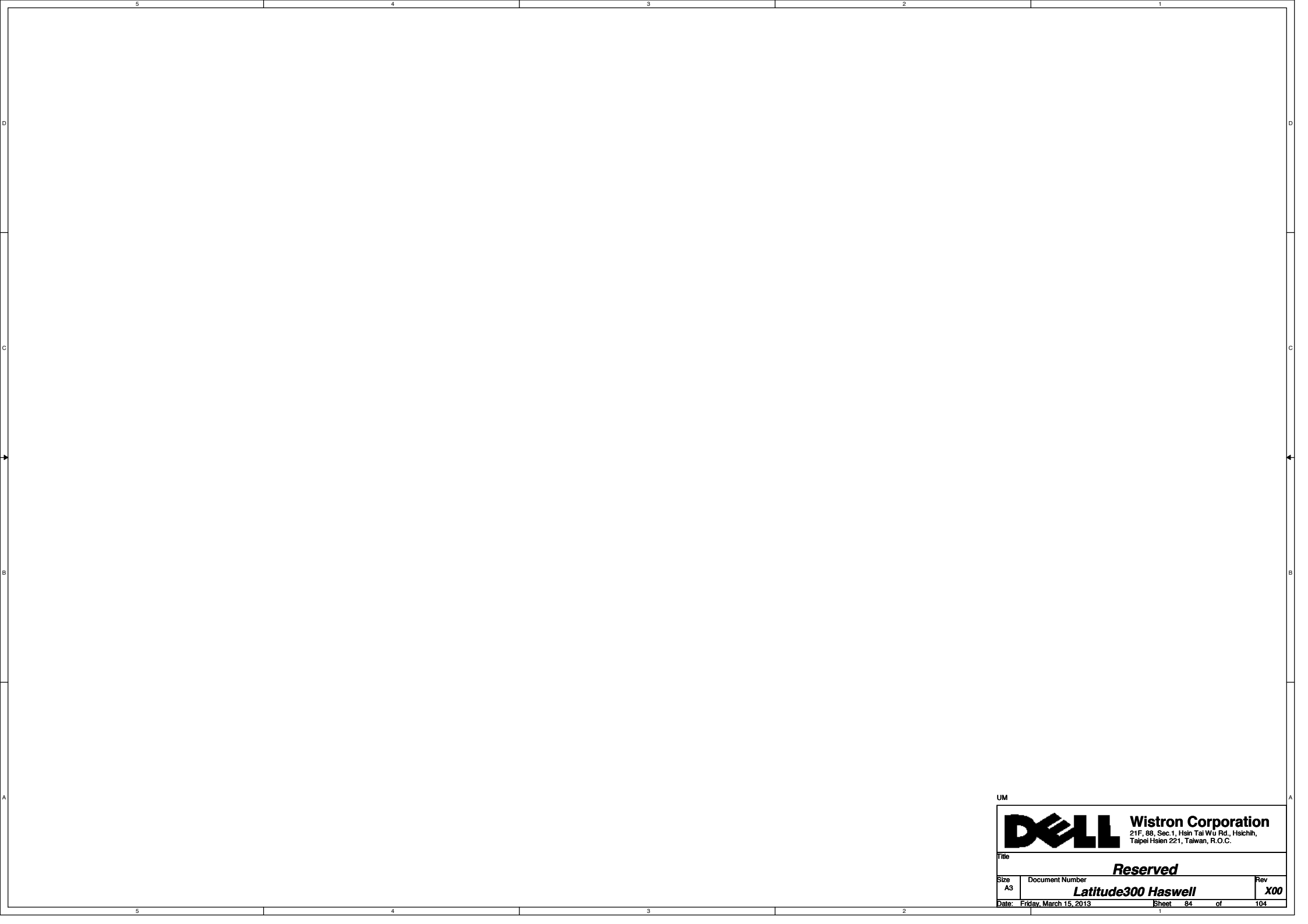
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Title: **DISCRETE VGA POWER**

Size: Custom Document Number: **Latitude300 Haswell** Rev: **X00**

Date: Tuesday, March 19, 2013 Sheet: 83 of 104




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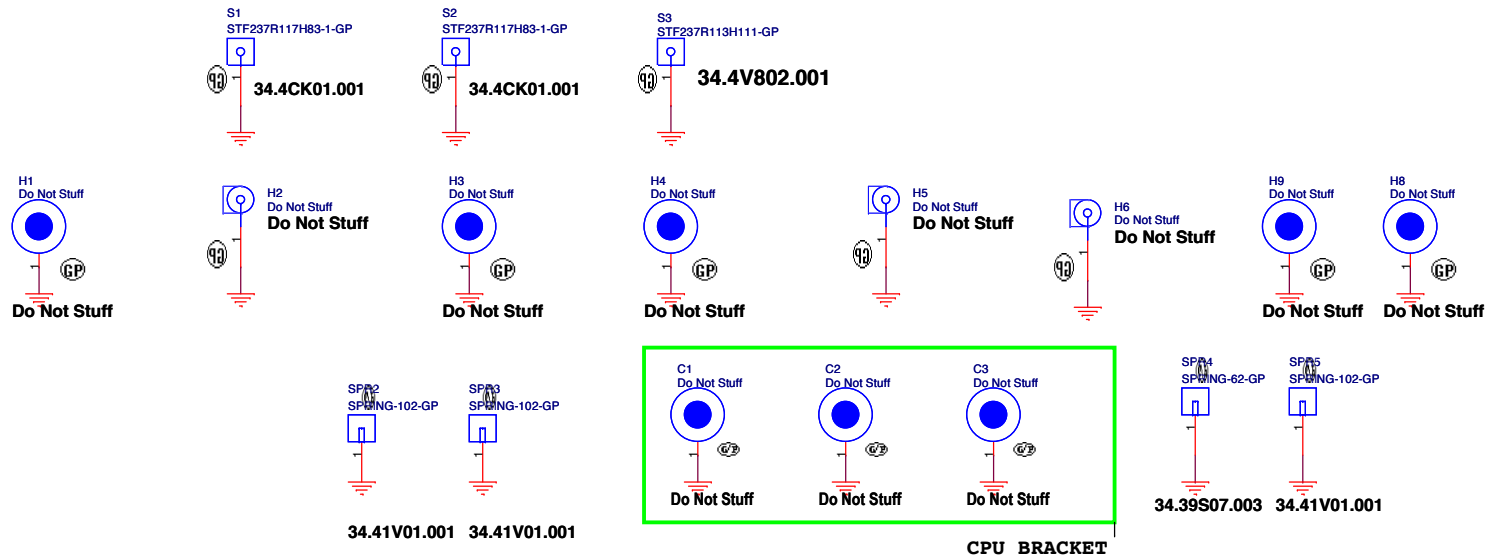
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Reserved		
Size	Document Number	Rev
A3	Latitude300 Haswell	X00
Date: Friday, March 15, 2013	Sheet 84 of	104

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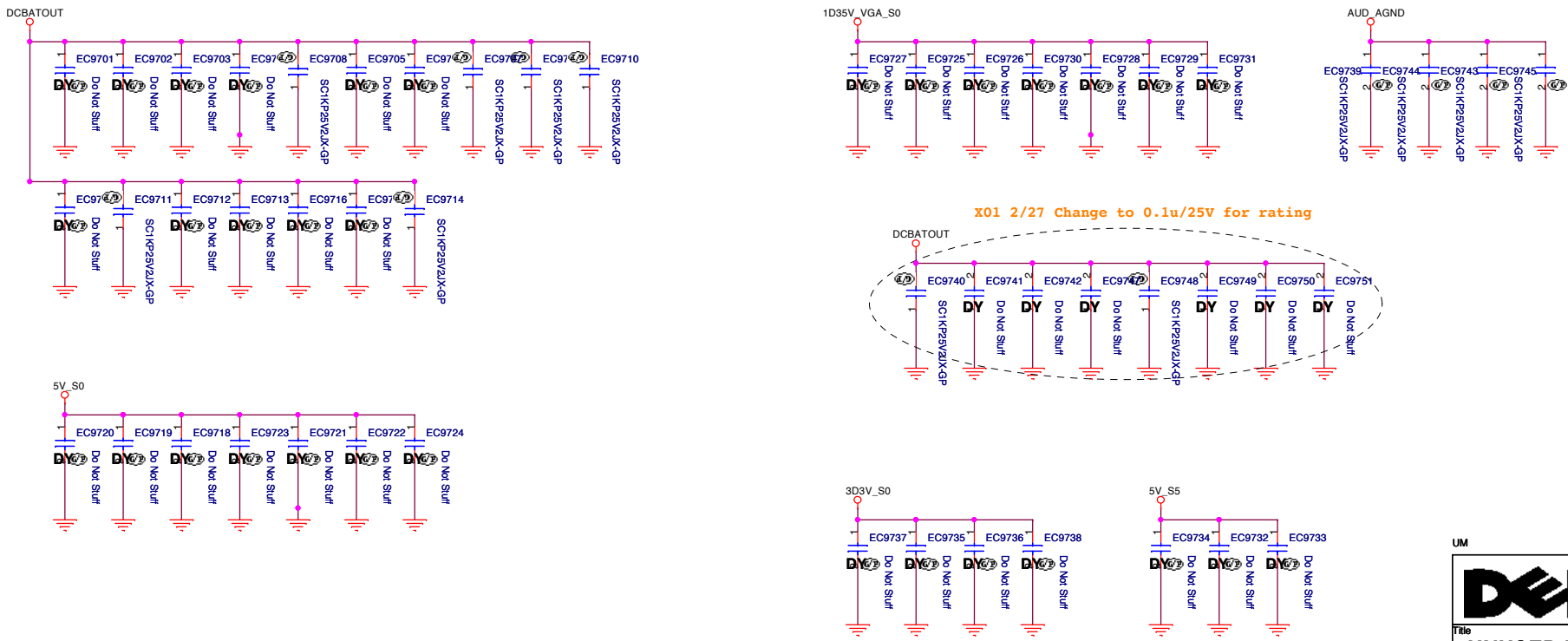
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Reserved		
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SSID = Mechanical



SSID = EMI



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Title: **UNUSED PARTS/EMI Capacitors**

Size A3	Document Number	Rev
Date: Friday, March 15, 2013	Latitude300 Haswell	X00
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Title		
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Title		
Reserved		
Size A3	Document Number Latitude300 Haswell	Rev X00
Date: Friday, March 15, 2013	Sheet 88	of 104


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Reserved		
Size A3	Document Number Latitude300 Haswell	Rev X00
Date: Friday, March 15, 2013	Sheet 89	of 104


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Title		
Free Fall Sensor		
Size	Document Number	Rev
A3	Latitude300 Haswell	X00
Date: Friday, March 15, 2013	Sheet 90	of 104


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UM

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Title		
Reserved		
Size A3	Document Number Latitude300 Haswell	Rev X00
Date: Friday, March 15, 2013	Sheet 91	of 104

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Title		
Reserved		
Size A3	Document Number Latitude300 Haswell	Rev X00
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Title			
Express Card			
Size	Document Number	Rev	
A3	Latitude300 Haswell	X00	
Date: Friday, March 15, 2013		Sheet 93	of 104

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Title		
LVDS Switch		
Size	Document Number	Rev
A3	Latitude300 Haswell	X00
Date: Friday, March 15, 2013	Sheet 94	of 104

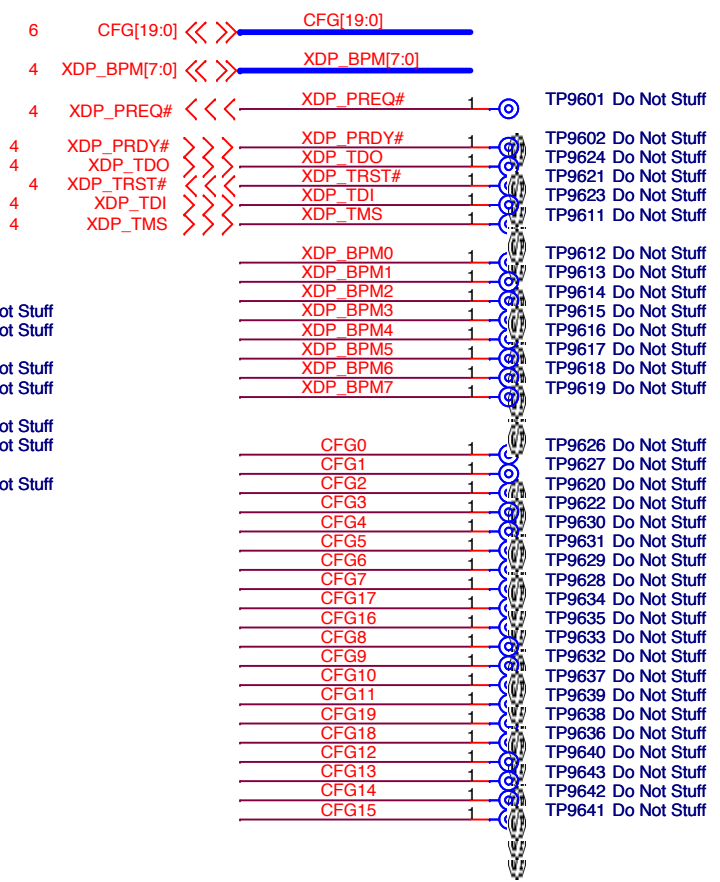
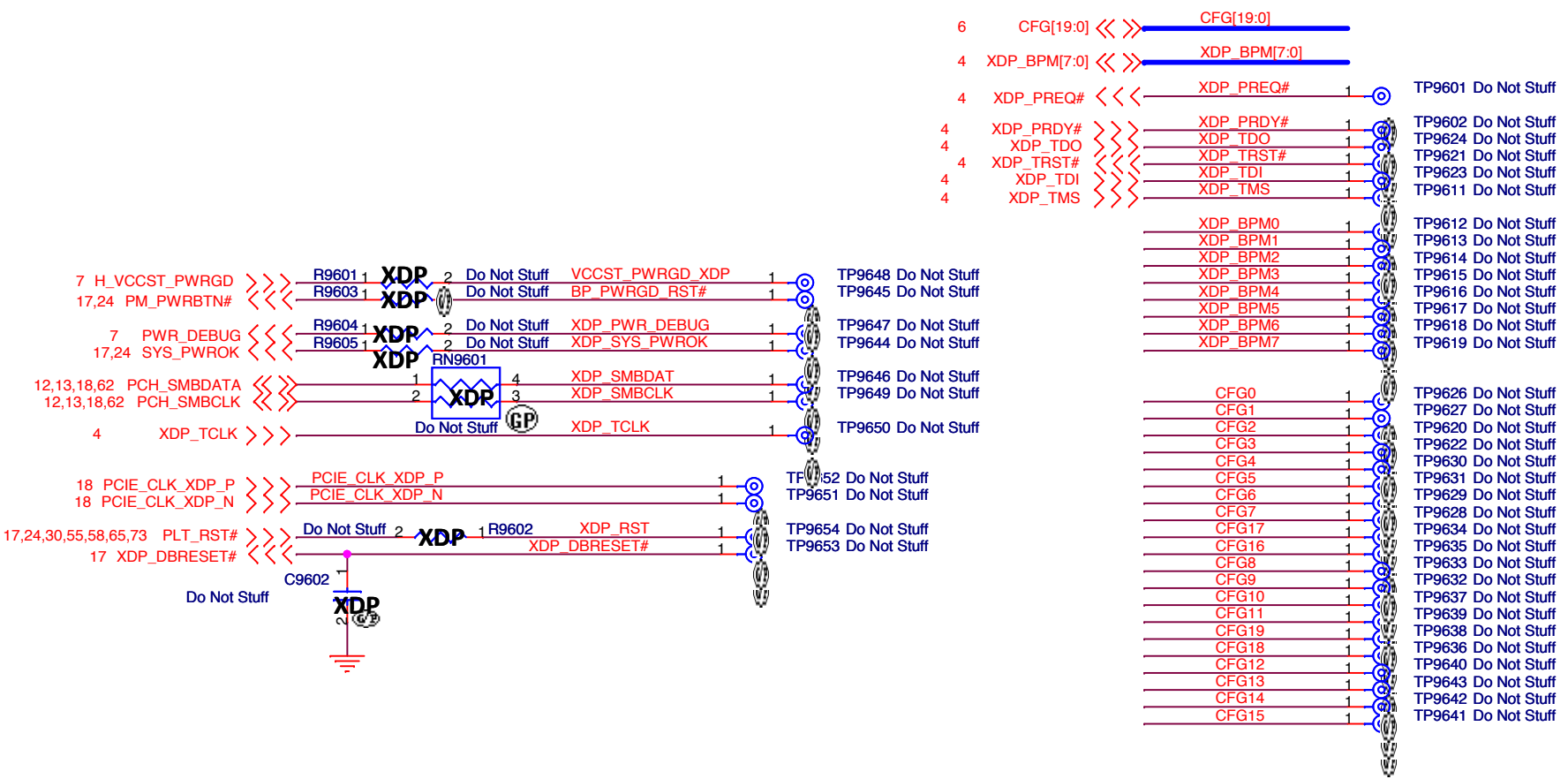
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
CRT Switch		
Size	Document Number	Rev
A3	Latitude300 Haswell	X00
Date: Friday, March 15, 2013	Sheet 95 of	104

SSID = XDP

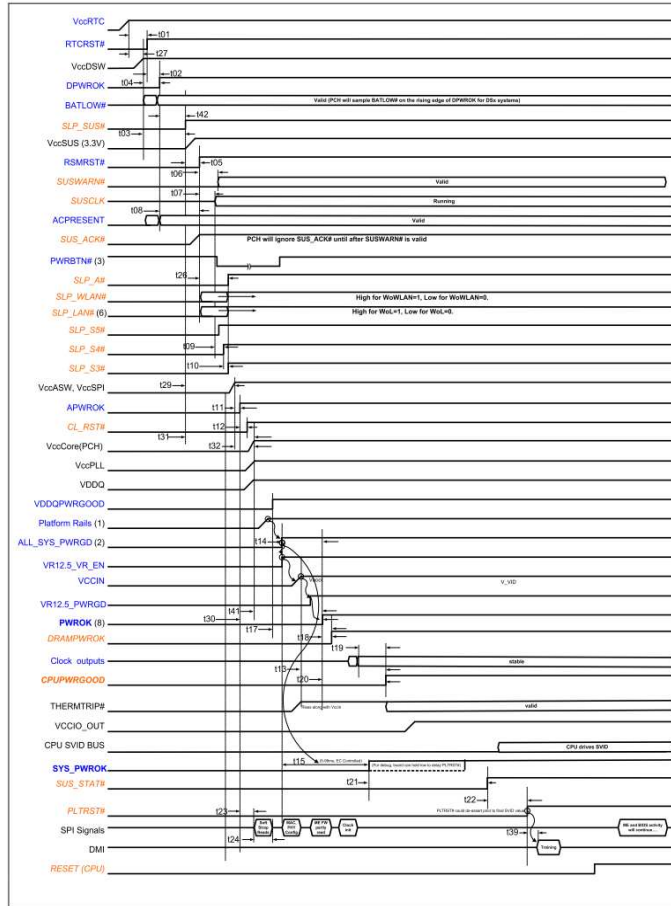
CPU XDP



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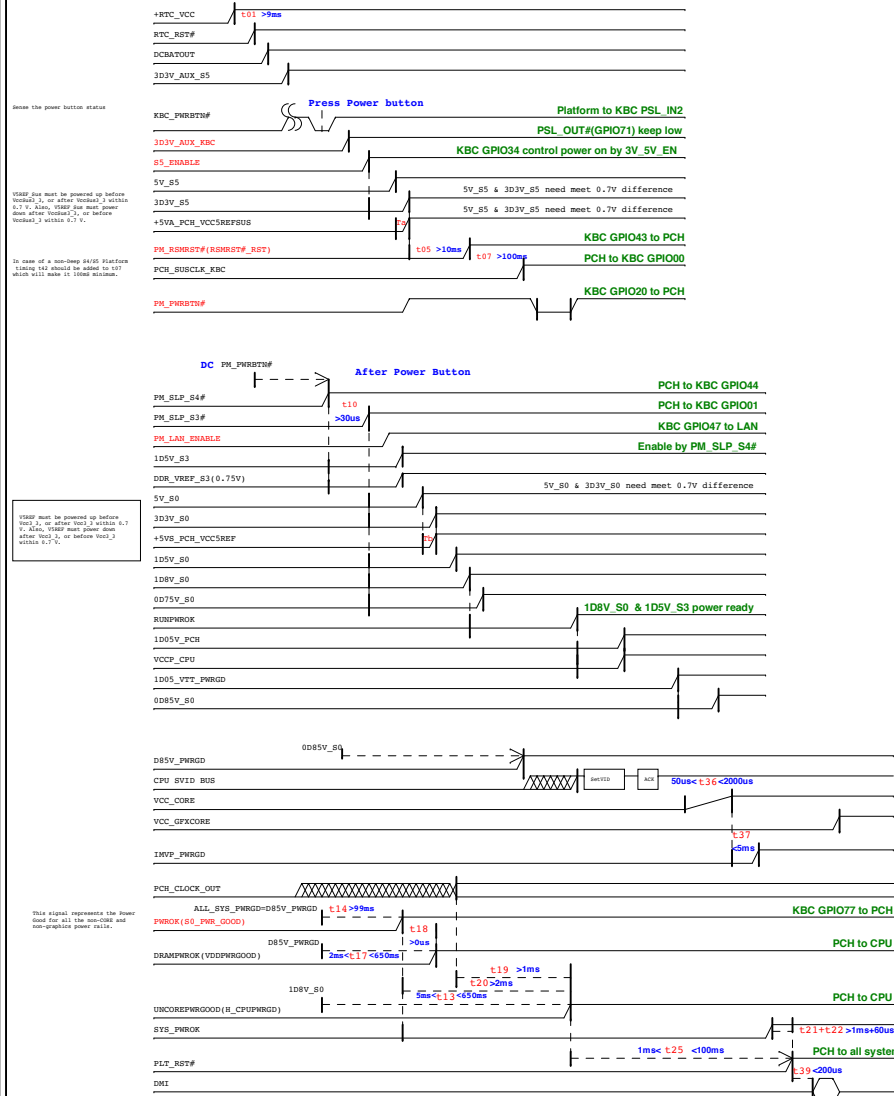
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
		Title <h3 style="text-align: center;">TOUCH PANEL</h3>	
Size A4	Document Number Latitude300 Haswell	Rev X00	
Date: Friday, March 15, 2013	Sheet 96	of 104	

Shark Bay Platform Power Sequence

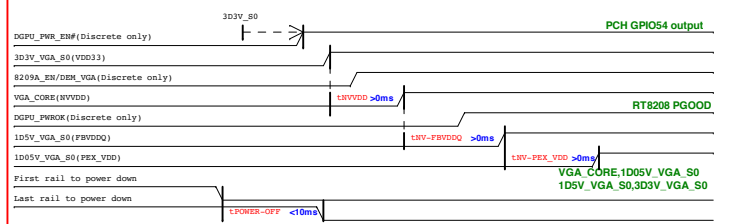


(DC mode)

Red Words: Controlled by RC GPIO

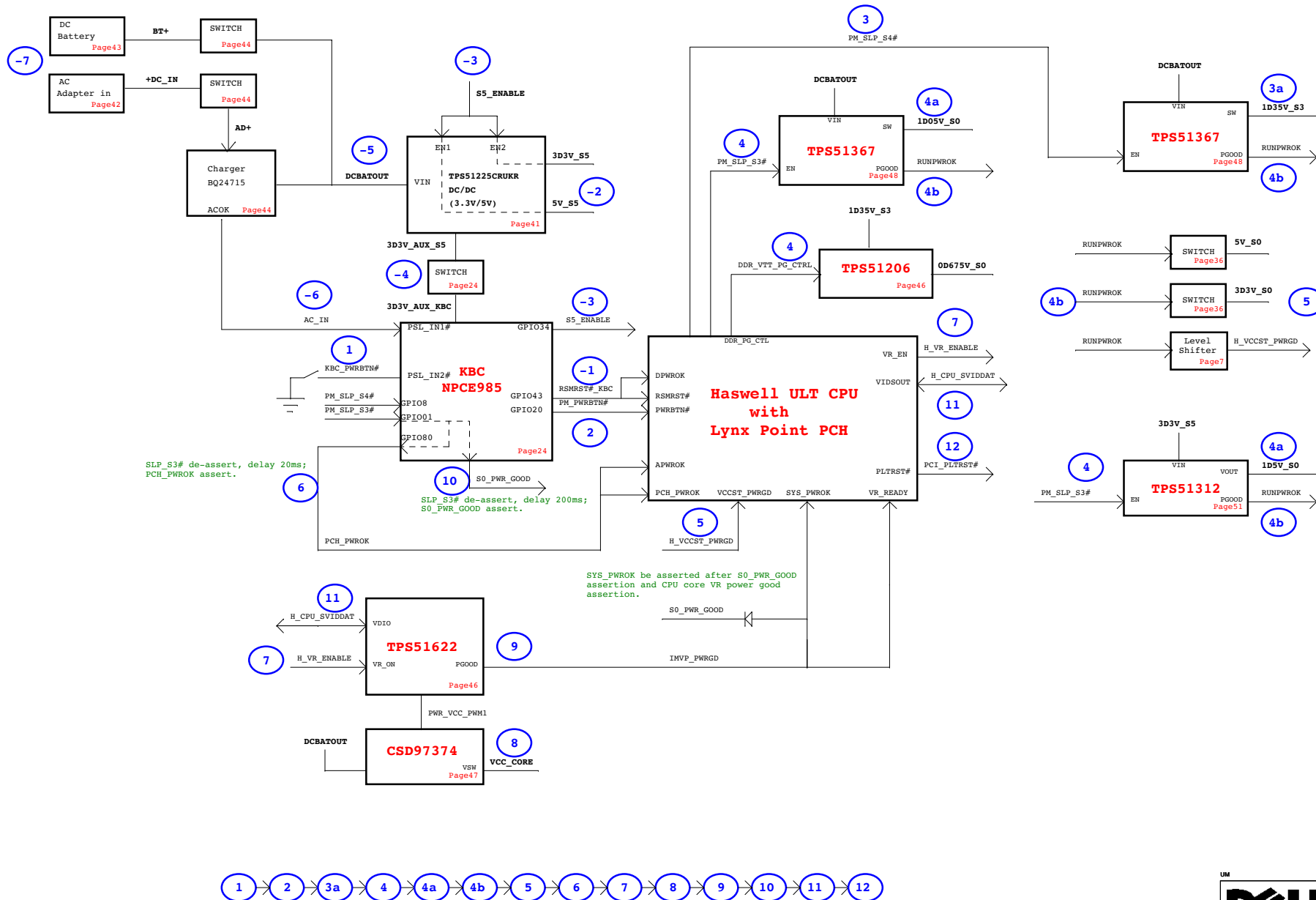


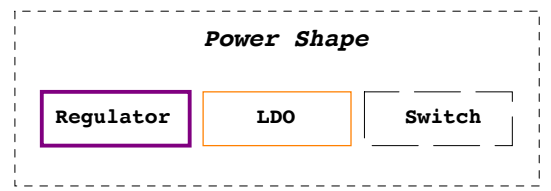
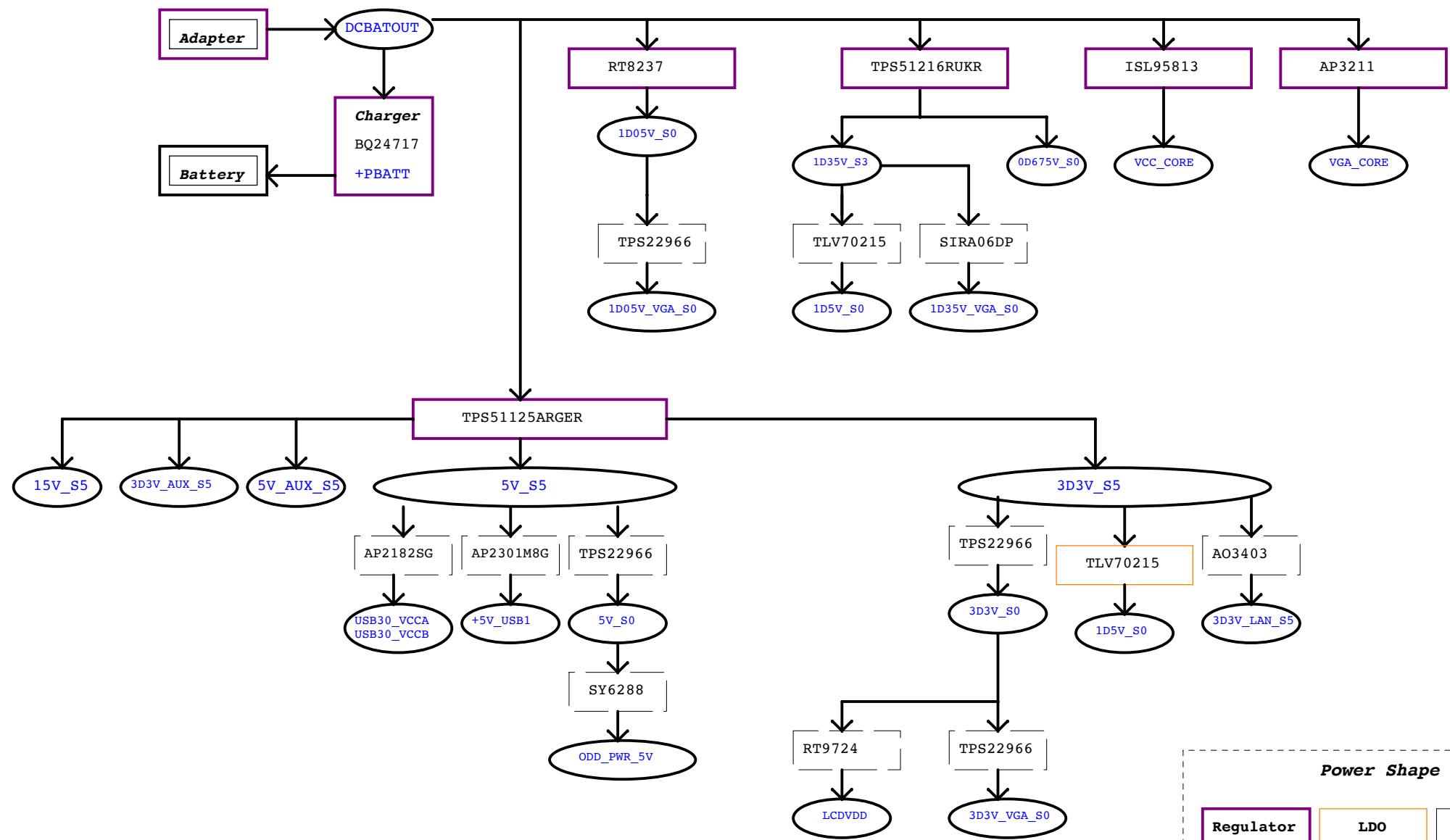
N14P-GT Power-Up/Down Sequence



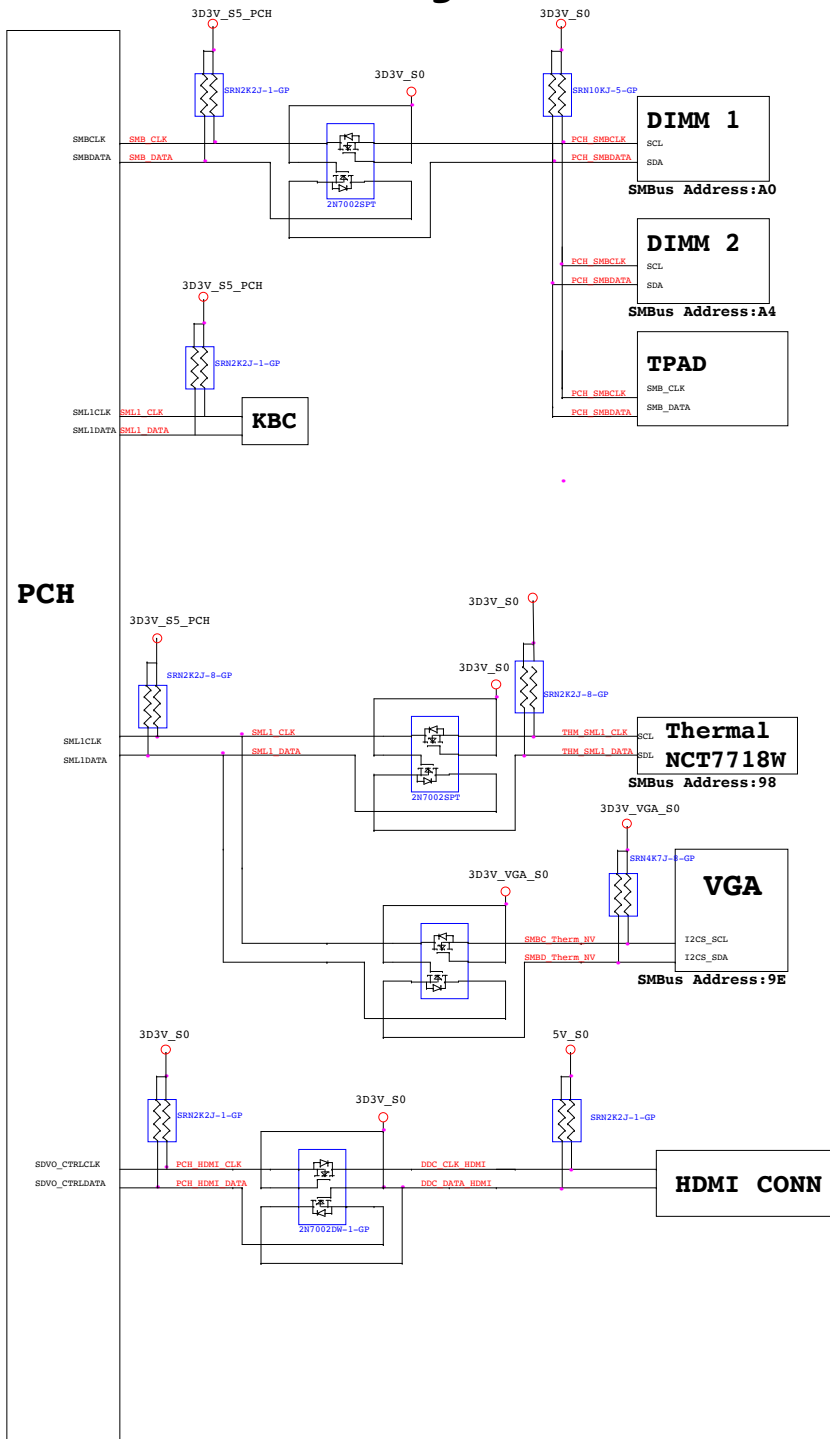
For power-down, reversing the ramp-up sequence is recommended.

Wistron SHARK BAY POWER UP SEQUENCE DIAGRAM

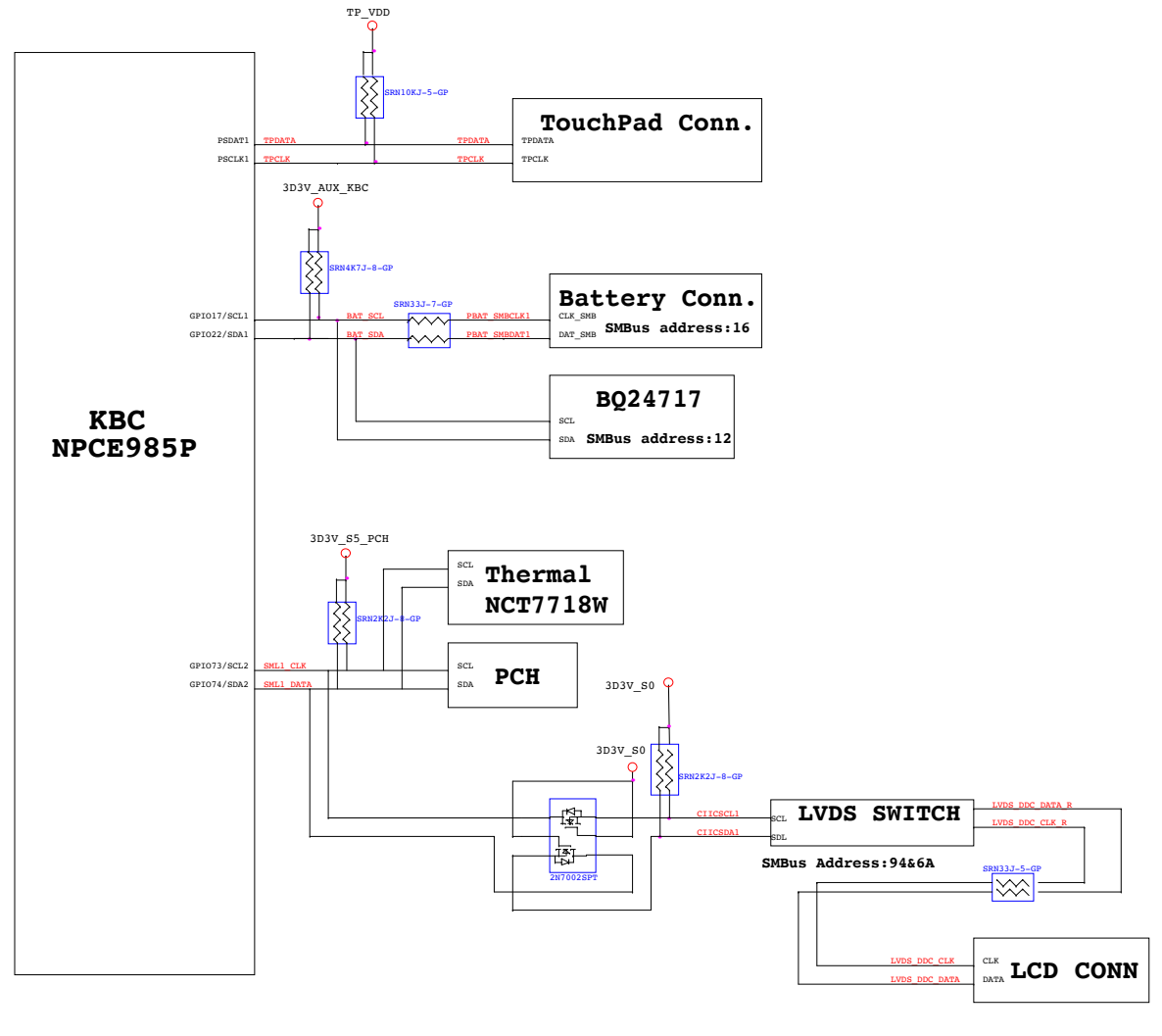




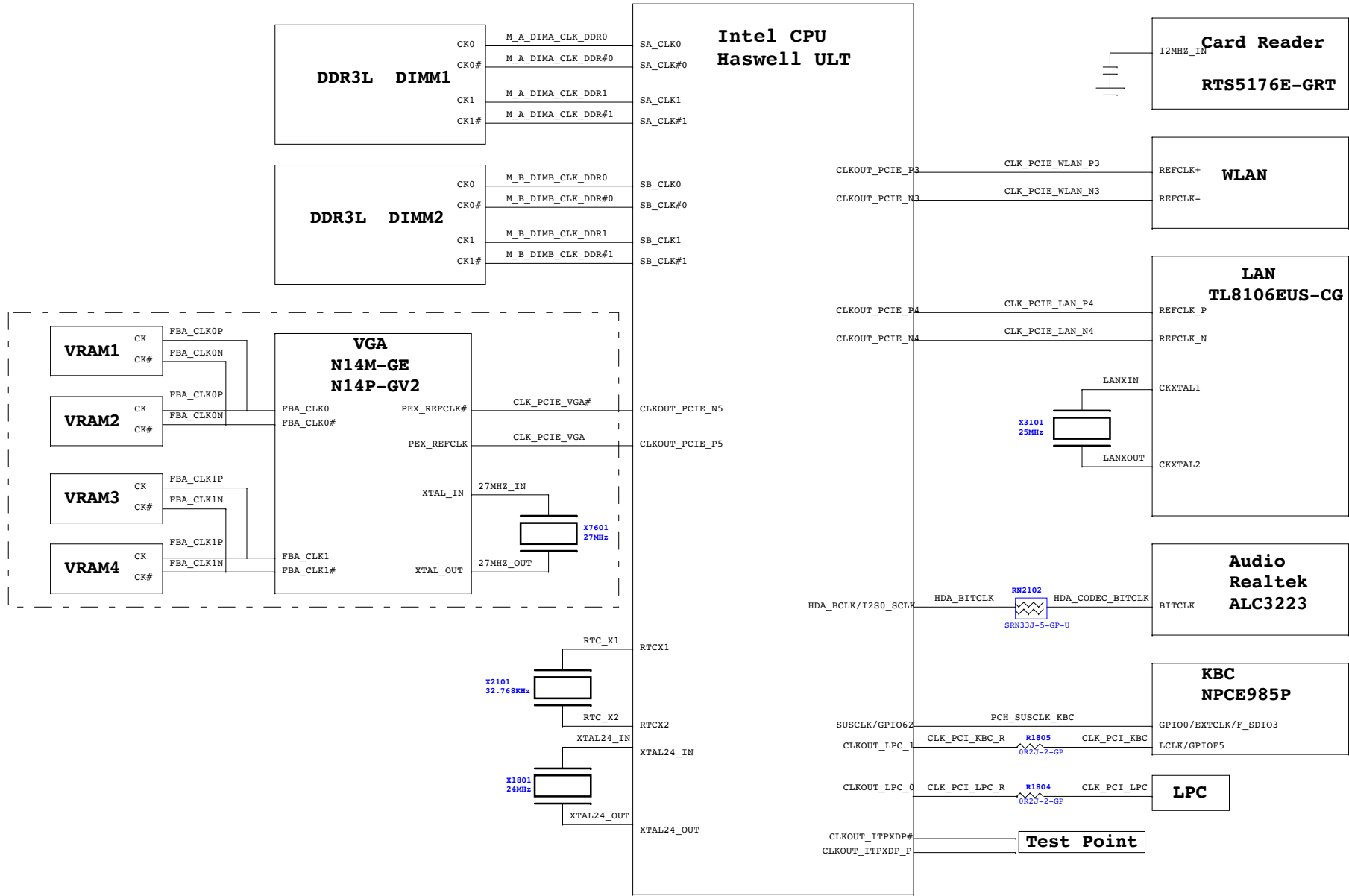
PCH SMBus Block Diagram



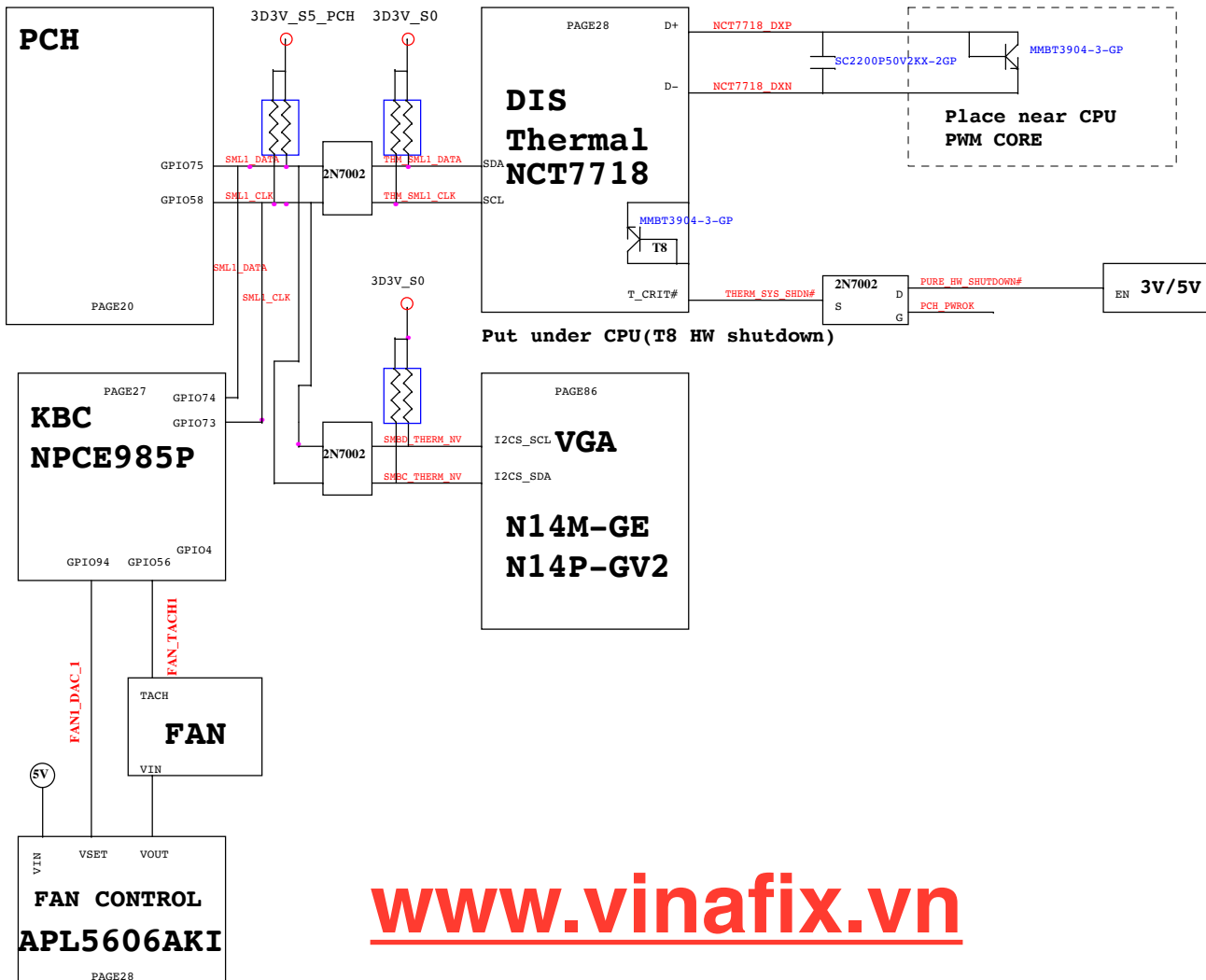
KBC SMBus Block Diagram



OAK Haswell CLK Block Diagram

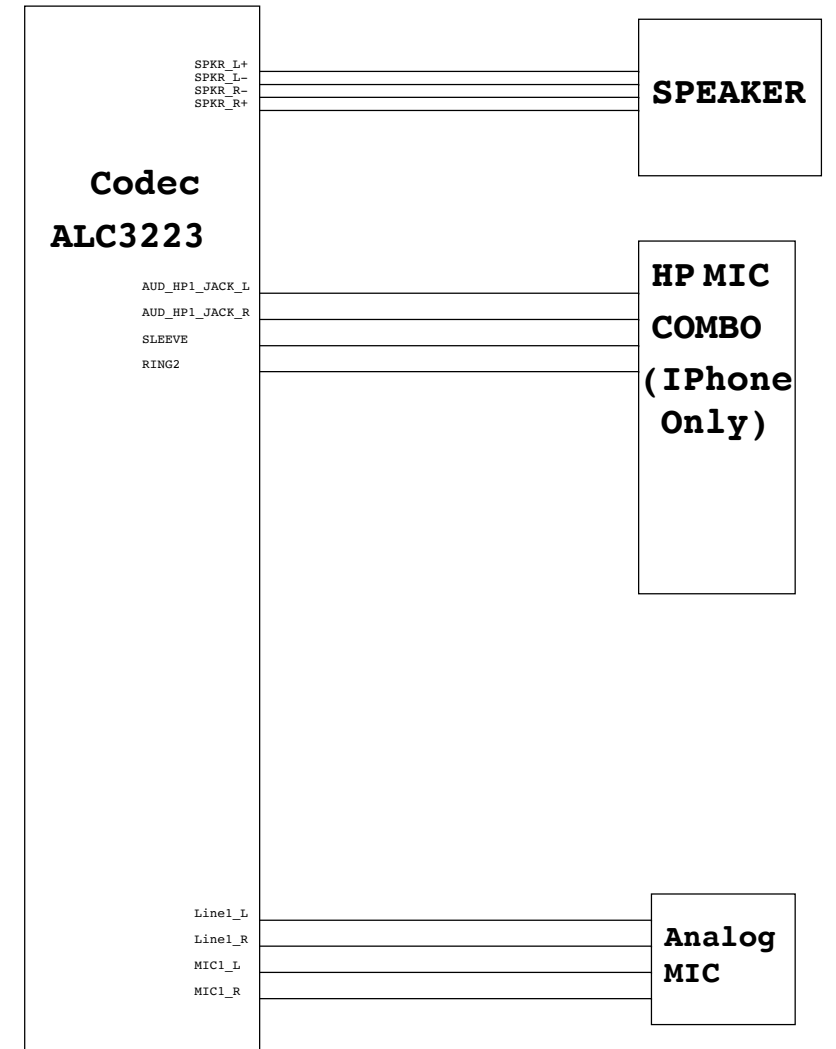


Thermal Block Diagram




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Audio Block Diagram



VERSION	DATA	PAGE	Change Item
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UM

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Title <p align="center">Change History</p>		
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