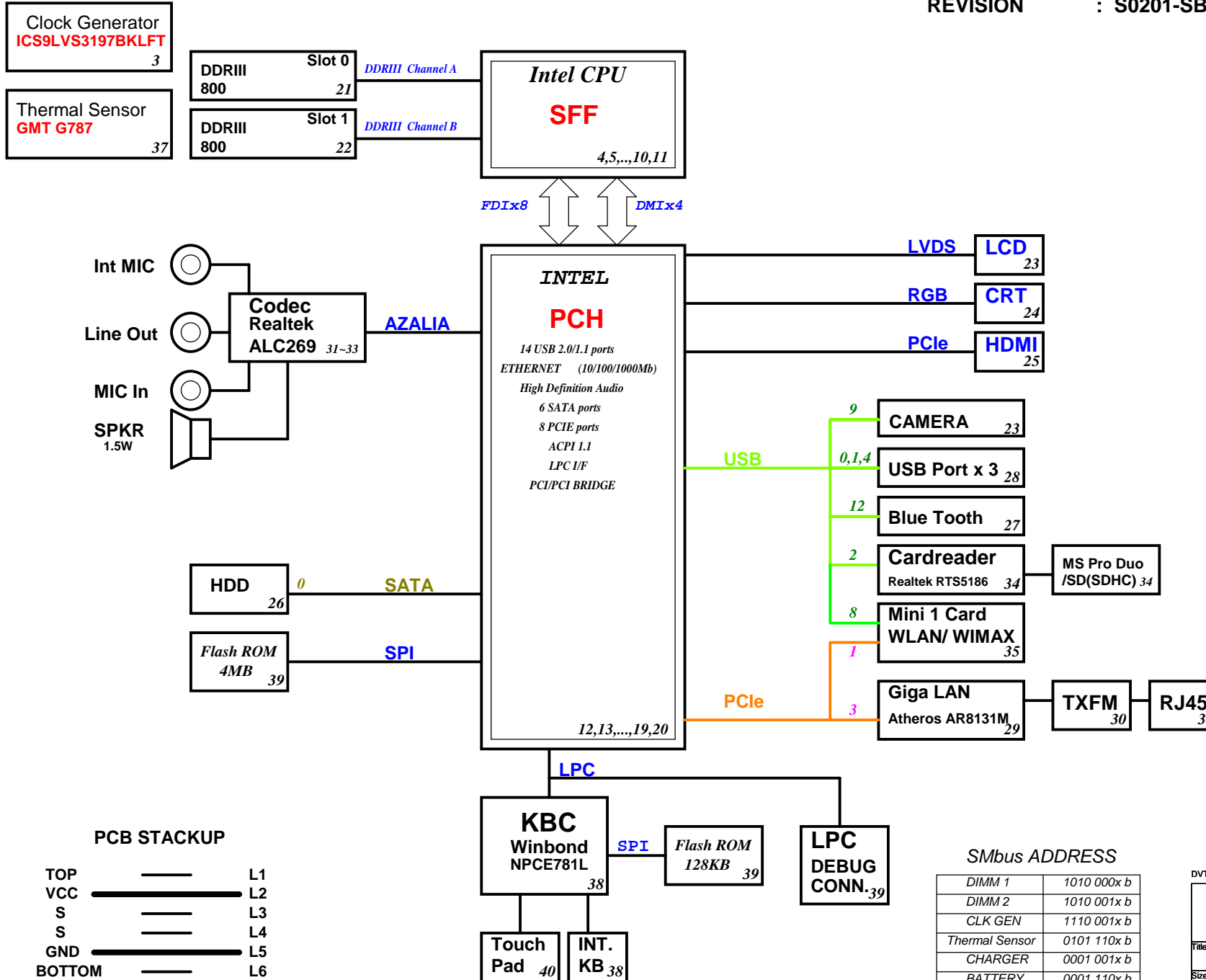


TUCANA Block Diagram

PROJECT CODE : 91.4KK01.001
 PCB P/N : 48.4KK01.0SB
 REVISION : S0201-SB



SMbus ADDRESS

DIMM 1	1010 000x b
DIMM 2	1010 001x b
CLK GEN	1110 001x b
Thermal Sensor	0101 110x b
CHARGER	0001 001x b
BATTERY	0001 110x b

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Title: **BLOCK DIAGRAM**

Size A3 Document Number: **TUCANA** Rev: **SB**

Date: Wednesday, July 07, 2010 Sheet 1 of 56

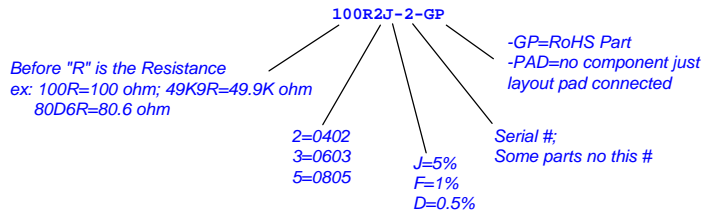
PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

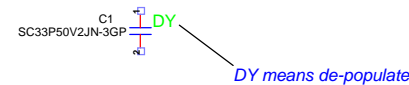
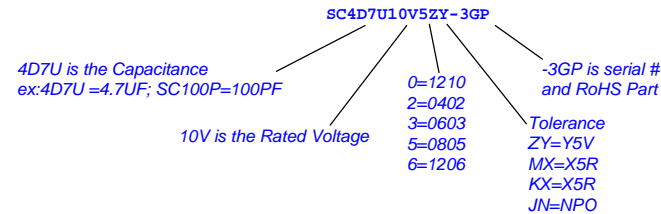
Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (xPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

Resistor

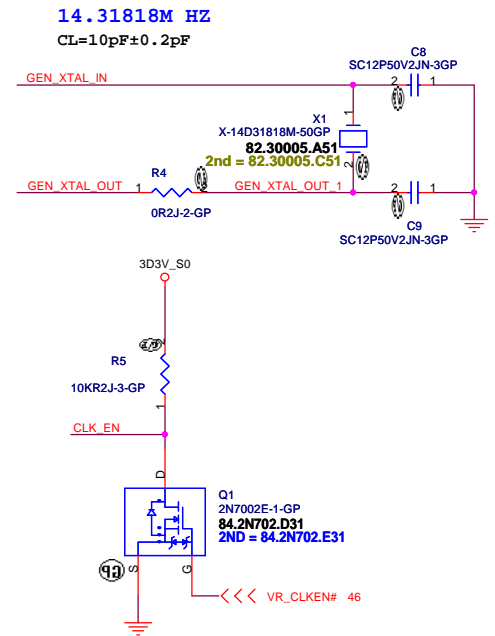
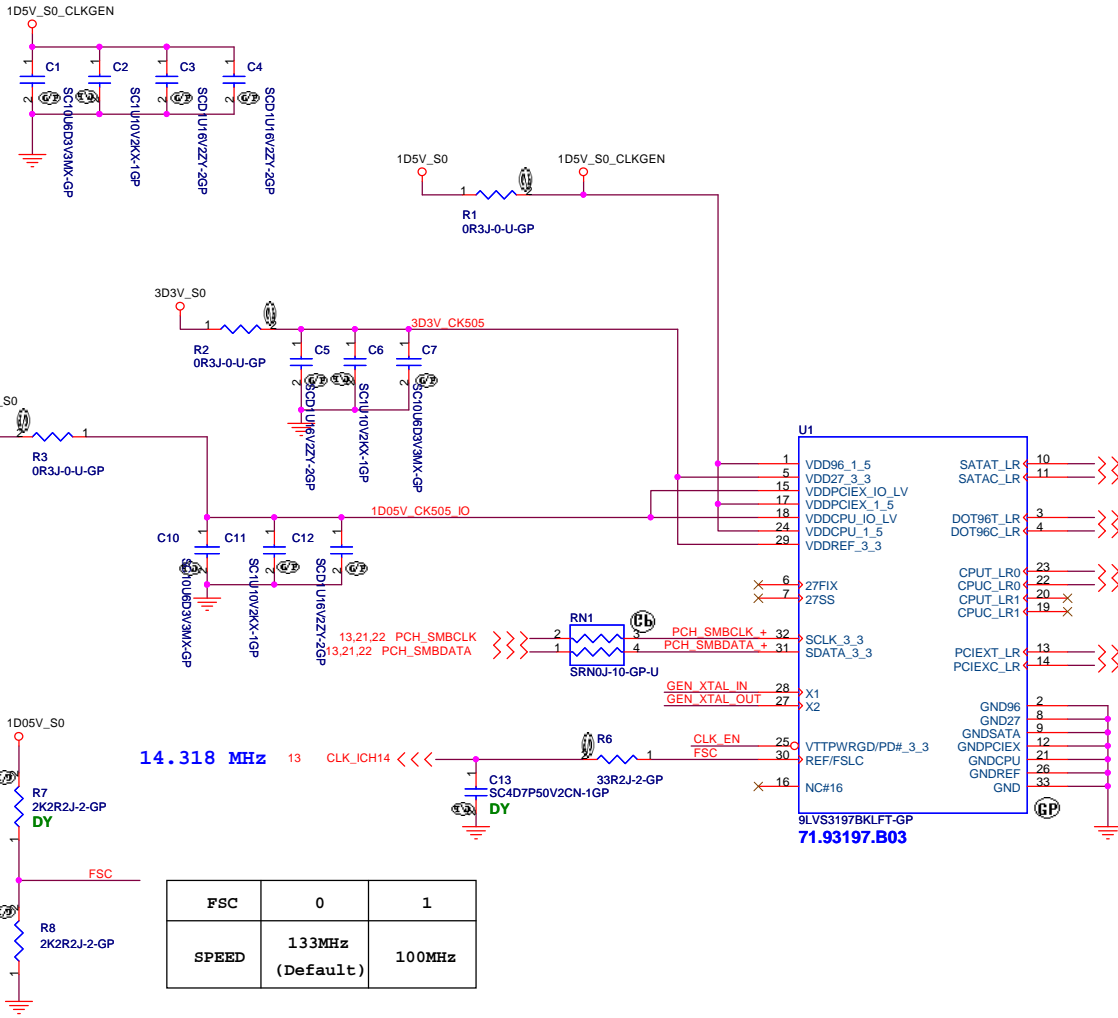


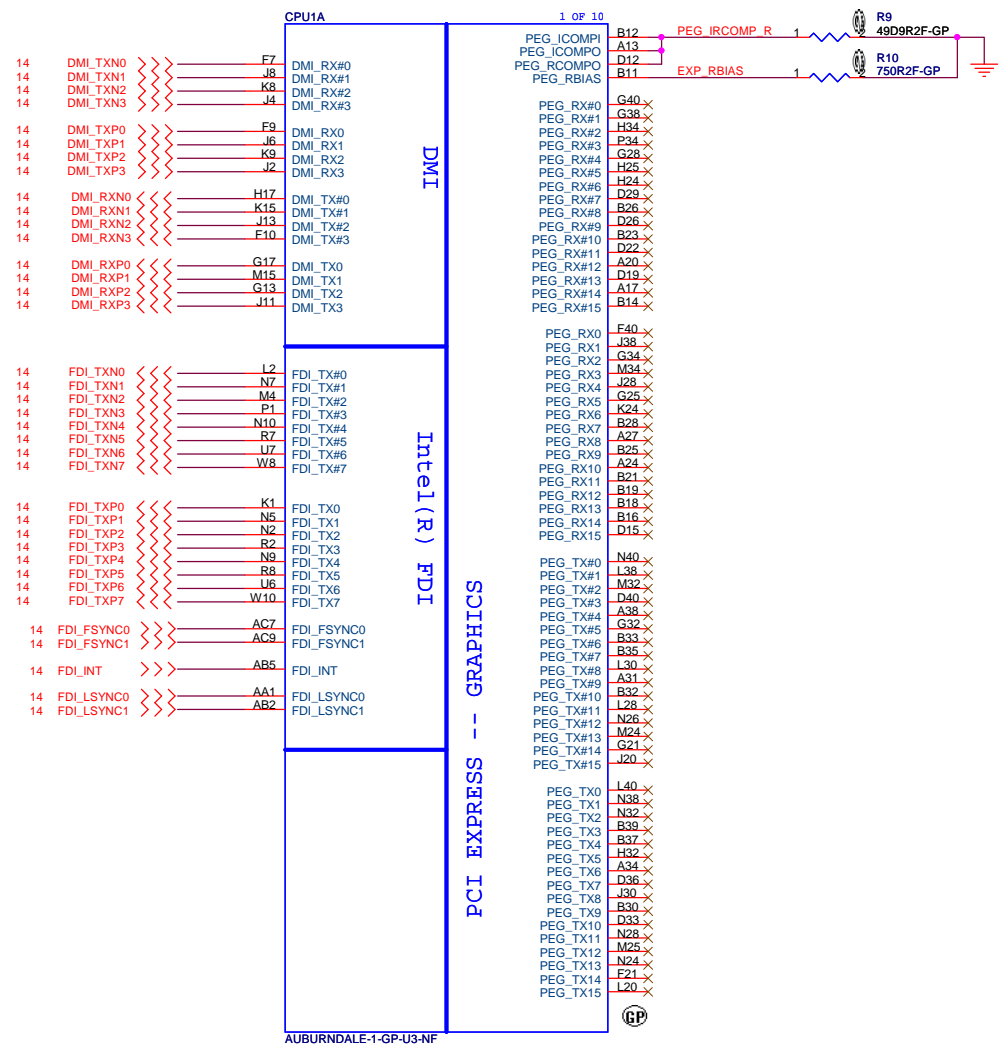
Capacitor



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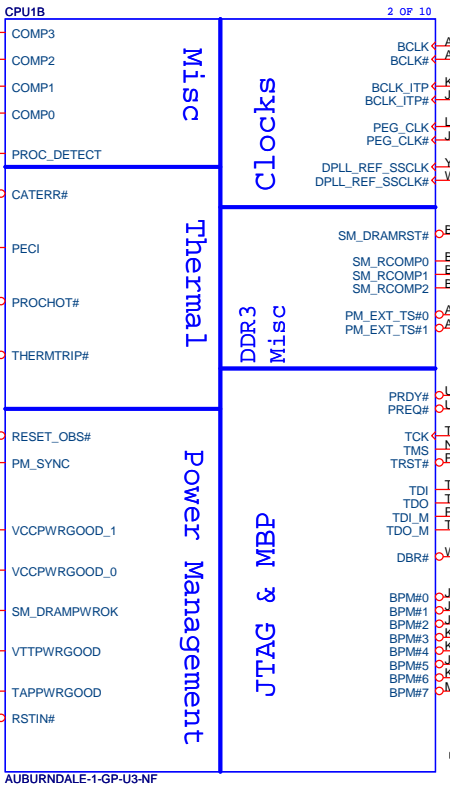
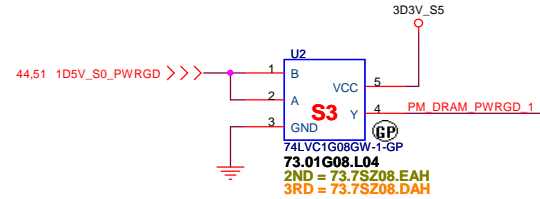
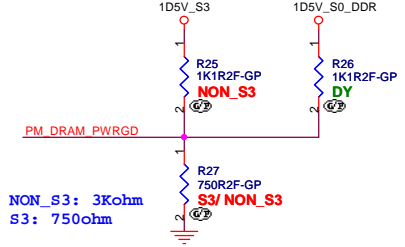
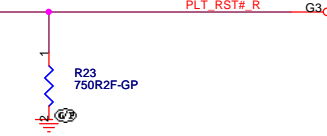
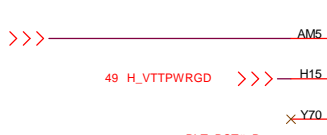
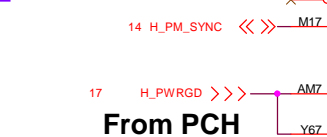
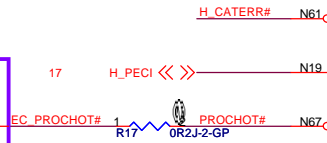
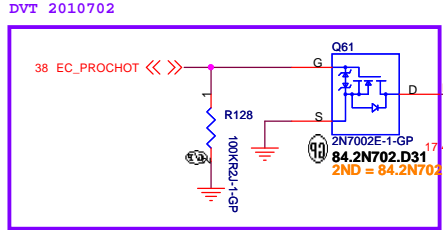
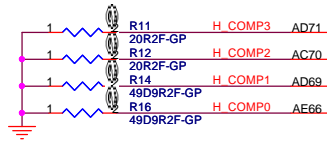
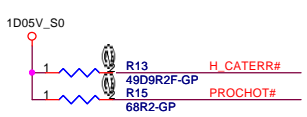
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Reference			
Size A3	Document Number	TUCANA	Rev SB
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Title CPU SFF 1 of 8(DMI/FDI/PEG)			
Size	Document Number	Rev	
A3	TUCANA	SB	
Date: Wednesday, July 07, 2010		Sheet	4 of 56

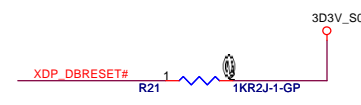
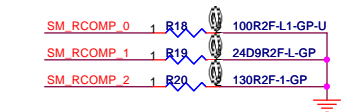


Clocks

DDR3 Misc

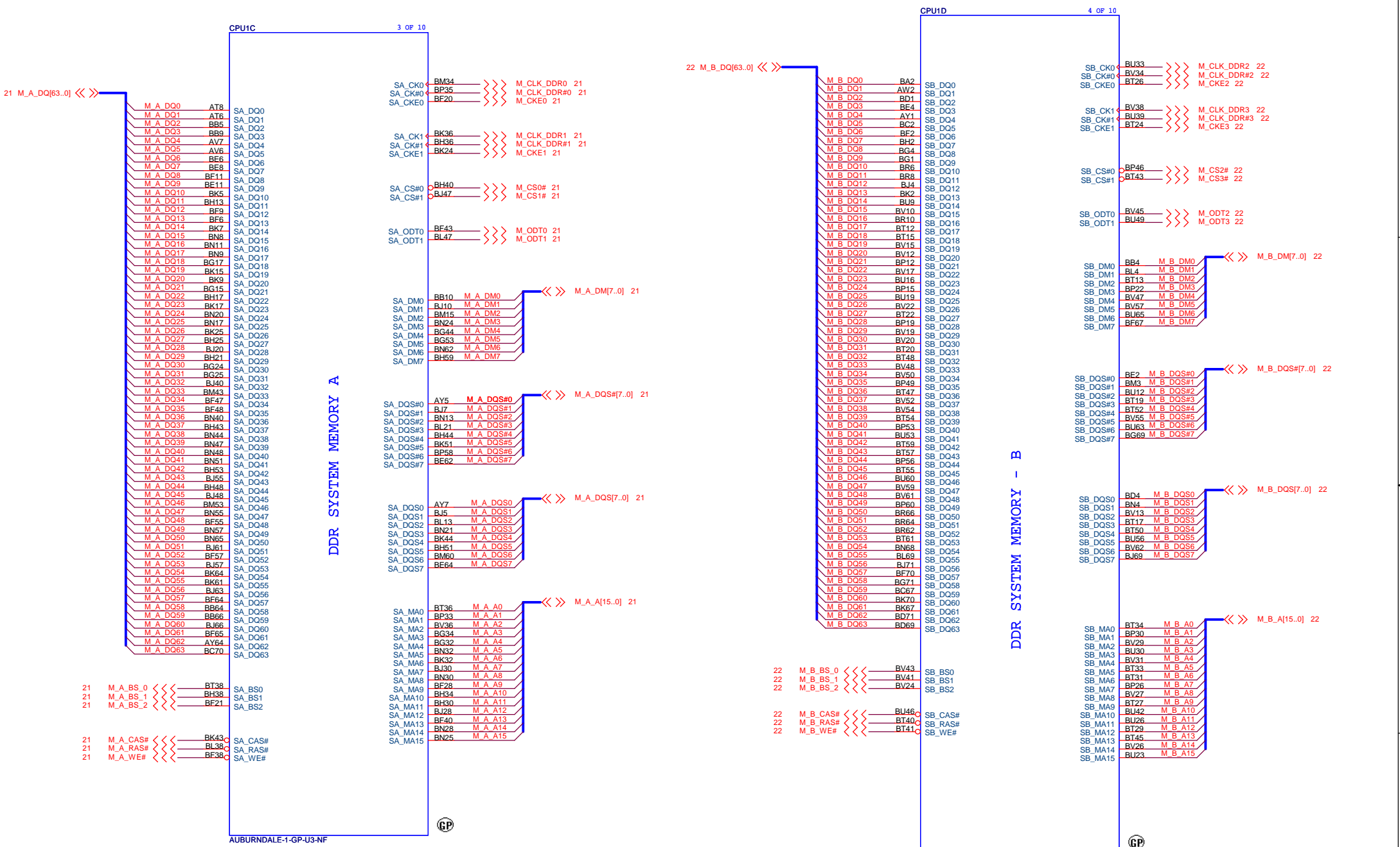
JTAG & MBP

If supports integrated graphics but without Embedded DisplayPort(eDP), these pins can also be connected to GND directly.



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CPU SFF 2 of 8(CLK/Thermal)	
Title CPU SFF 2 of 8(CLK/Thermal)	Rev SB
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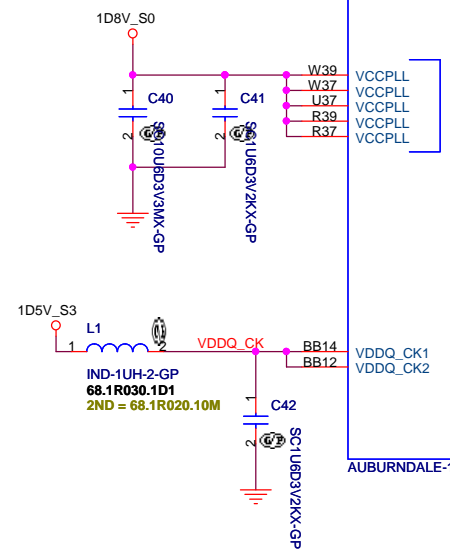
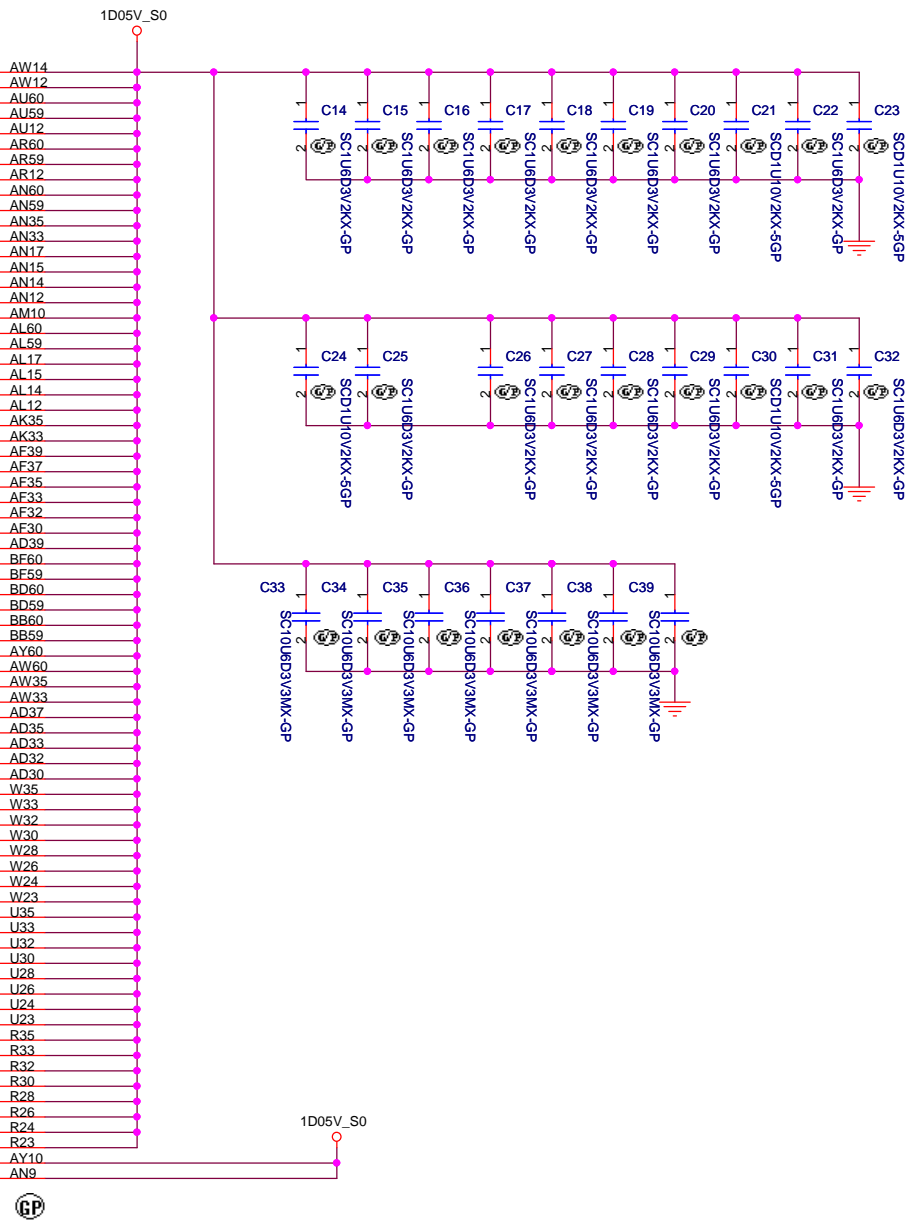
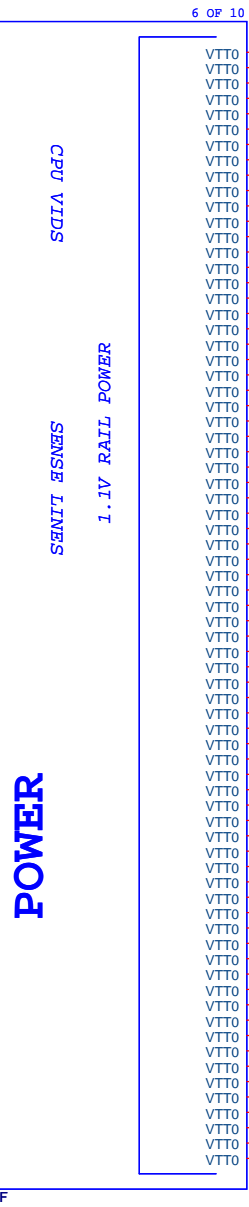
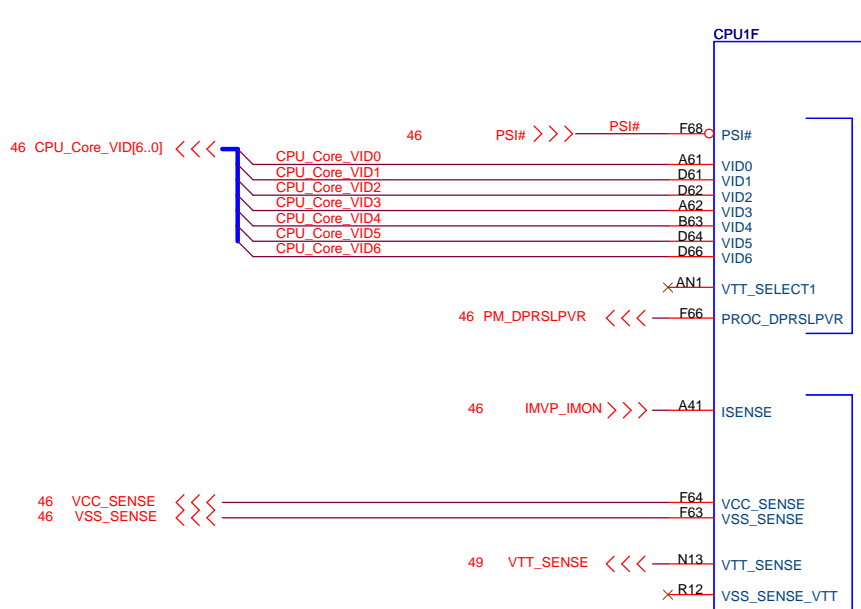


AUBURDALE-1-GP-U3-NF

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CPU SFF 3 of 8(DDR)	
Title	SB
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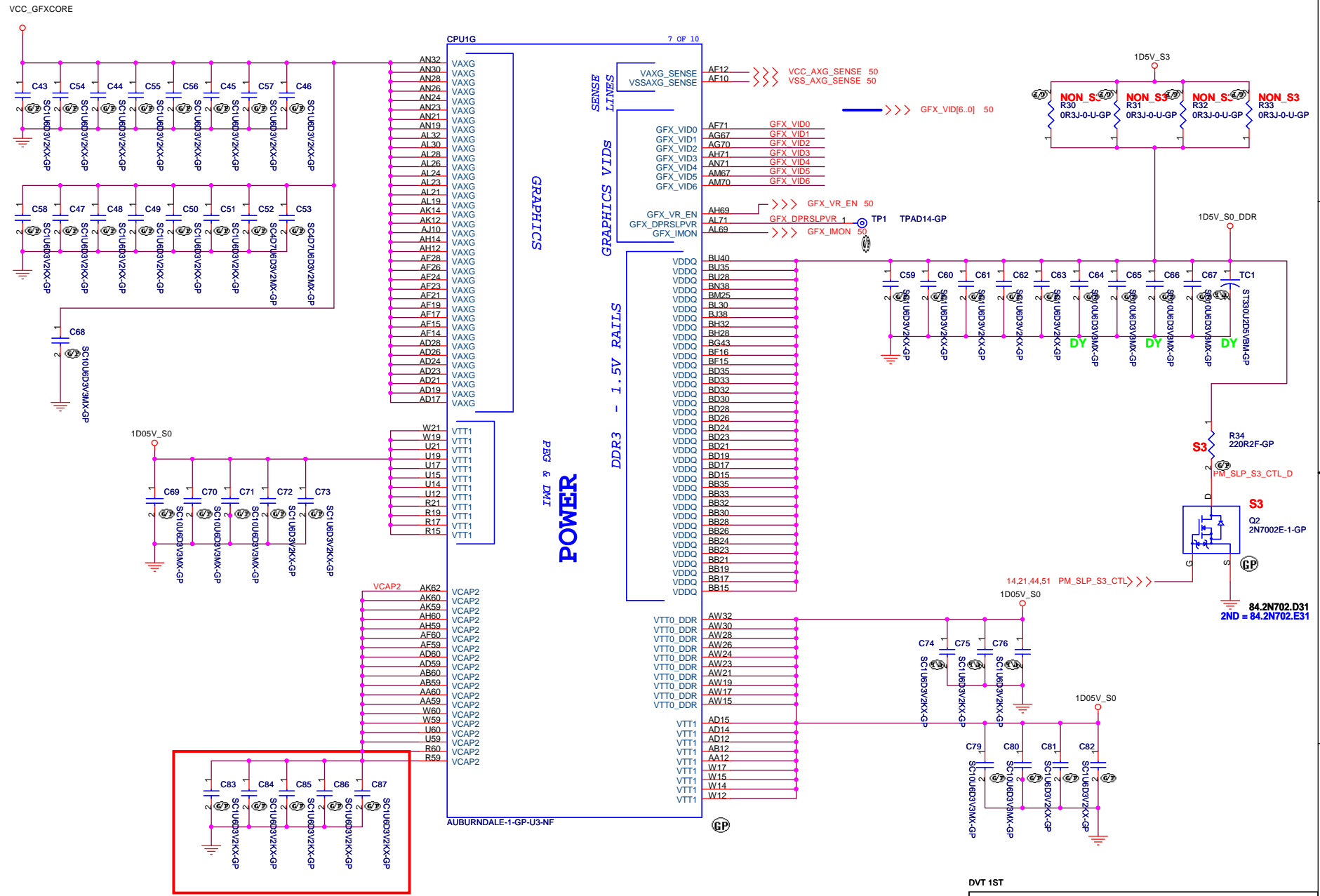
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V

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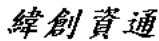
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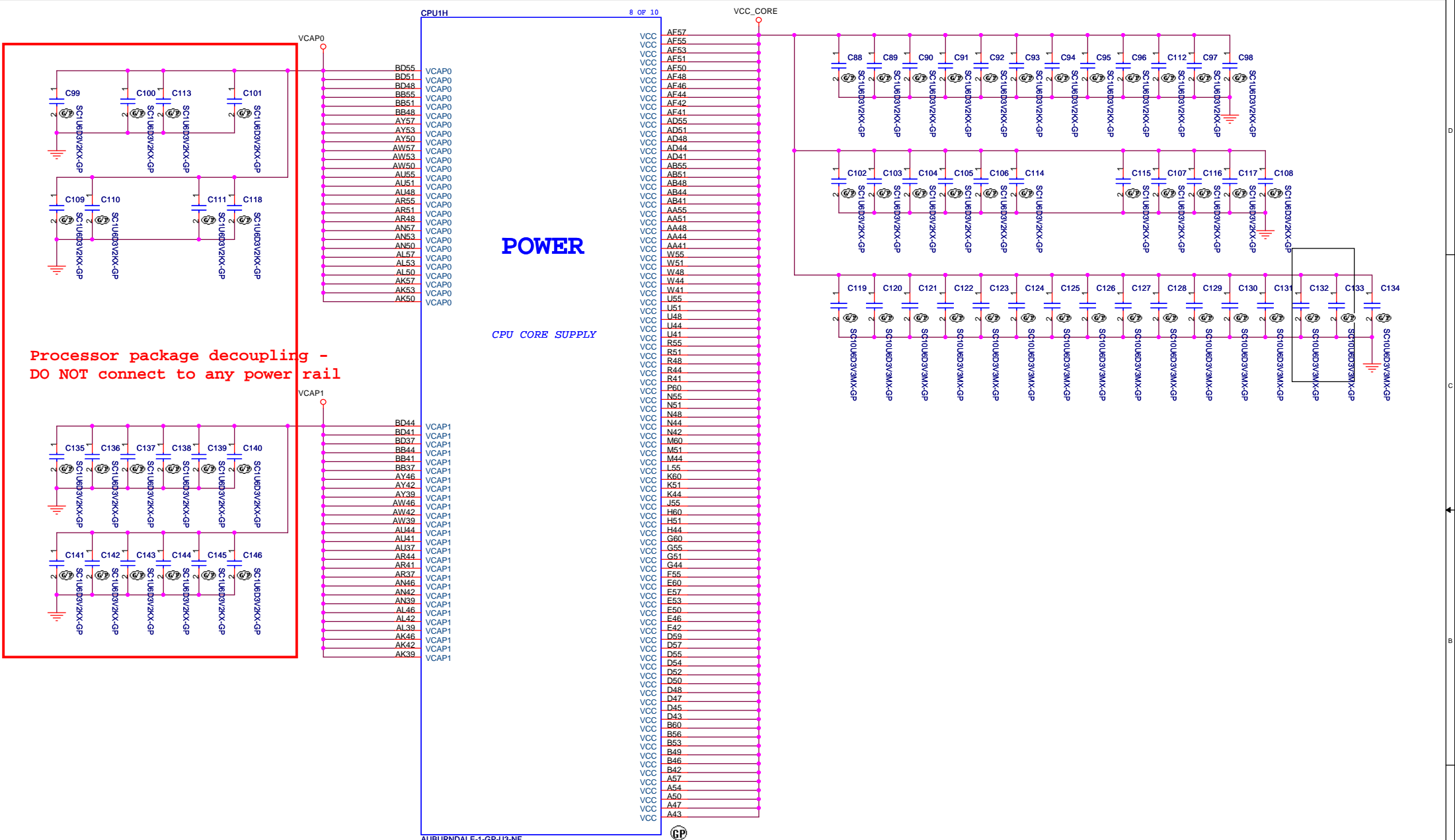
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Do not dummy these CAPS

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Title CPU SFF 5 of 8(PWR/DDR/GFX)		
Size A3	Document Number TUCANA	Rev SB
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**Processor package decoupling -
DO NOT connect to any power rail**

POWER
CPU CORE SUPPLY

AUBURNDALE-1-GP-U3-NF



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CPU SFF 6 of 8(CPUCORE)			
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- CFG0 AL4
- CFG1 AM2
- CFG2 AK1
- CFG3 AK2
- CFG4 AK4
- CFG5 AJ2
- CFG6 AT2
- CFG7 AG7
- CFG8 AF4
- CFG9 AG2
- CFG10 AH1
- CFG11 AC2
- CFG12 AC4
- CFG13 AE2
- CFG14 AD1
- CFG15 AF8
- CFG16 AF6
- CFG17 AB7

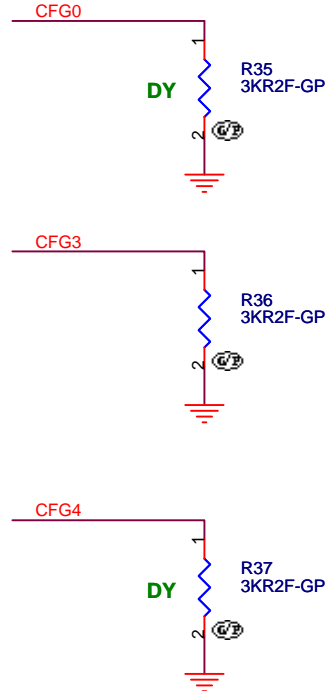
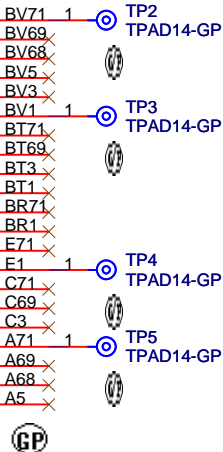
- RSVD#W66 W66
- RSVD#W64 W64
- RSVD#AC69 AC69
- RSVD#AC71 AC71
- RSVD#AA71 AA71
- RSVD#AA69 AA69
- RSVD#R66 R66
- RSVD#R64 R64
- RSVD_NCTF#BT5 BT5
- RSDV_NCTF#BR5 BR5
- RSDV_NCTF#BV6 BV6
- RSDV_NCTF#BV8 BV8
- RSVD#AV69 AV69
- RSVD#AK71 AK71
- RSVD#AN69 AN69
- RSVD#AP66 AP66
- RSVD#AH66 AH66
- RSVD#AK66 AK66
- RSVD#AR71 AR71
- RSVD#AM66 AM66
- RSVD#AK69 AK69
- RSVD#AU71 AU71
- RSVD#AT70 AT70
- RSVD#AR69 AR69
- RSVD#AU69 AU69
- RSVD#AT67 AT67

RESERVED

- RSVD_TP0 AU1
- RSVD#T4 T4
- RSVD#T2 T2
- RSVD#U1 U1
- RSVD#V2 V2
- RSVD#AV71 AV71
- RSVD#AW70 AW70
- RSVD#AY69 AY69
- RSVD#BB69 BB69
- RSVD#D8 D8
- RSVD#B7 B7
- RSVD#A10 A10
- RSVD#B9 B9
- RSVD_NCTF#C5 C5
- RSVD_NCTF#A6 A6
- RSVD_NCTF#E3 E3
- RSVD_NCTF#F1 F1

NCTF TEST PIN:
A5, A68, A69, A71, C3, C71, E1, E71, BR1, BR71,
BT1, BT71, BV1, BV3, BV5, BV68, BV69, BV71

- NCTF_DC_TEST#BV71 BV71
- NCTF_DC_TEST#BV69 BV69
- NCTF_DC_TEST#BV68 BV68
- NCTF_DC_TEST#BV5 BV5
- NCTF_DC_TEST#BV3 BV3
- NCTF_DC_TEST#BV1 BV1
- NCTF_DC_TEST#BT71 BT71
- DC_TEST_BT69 BT69
- DC_TEST_BT3 BT3
- NCTF_DC_TEST#BT1 BT1
- NCTF_DC_TEST#BR71 BR71
- NCTF_DC_TEST#BR1 BR1
- NCTF_DC_TEST#E71 E71
- NCTF_DC_TEST#E1 E1
- NCTF_DC_TEST#C71 C71
- DC_TEST_C69 C69
- NCTF_DC_TEST#C3 C3
- NCTF_DC_TEST#A71 A71
- NCTF_DC_TEST#A69 A69
- NCTF_DC_TEST#A68 A68
- NCTF_DC_TEST#A5 A5



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

DVT 1ST

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CPU SFF 7 of 8(REERVED)	
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CPU1I

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BU62	VSS	AY24
BU58	VSS	AY23
BU55	VSS	AY21
BU51	VSS	AY19
BU48	VSS	AY17
BU44	VSS	AY15
BU37	VSS	AY14
BU32	VSS	AY12
BU25	VSS	AY8
BU21	VSS	AY4
BU18	VSS	AW67
BU14	VSS	AW62
BU11	VSS	AW59
BU7	VSS	AW55
BP42	VSS	AW51
BN64	VSS	AW48
BN6	VSS	AW44
BM70	VSS	AW41
BM51	VSS	AW37
BM44	VSS	AV9
BM32	VSS	AV7
BM24	VSS	AU70
BM17	VSS	AU62
BL57	VSS	AU57
BL55	VSS	AU53
BL48	VSS	AU50
BL40	VSS	AU46
BL28	VSS	AU42
BL20	VSS	AU39
BK63	VSS	AU35
BK60	VSS	AU33
BK53	VSS	AU32
BK34	VSS	AU30
BK10	VSS	AU28
BJ64	VSS	AU26
BJ21	VSS	AD53
BJ9	VSS	AD50
BJ1	VSS	AD46
BH70	VSS	AD42
BH57	VSS	AD4
BH55	VSS	AC67
BH47	VSS	AC64
BH24	VSS	AC10
BH20	VSS	AC5
BH15	VSS	AC1
BG51	VSS	AB70
BG36	VSS	AB62
BF62	VSS	AB57
BF30	VSS	AB53
BF13	VSS	AB50
BF8	VSS	AB46
BE70	VSS	AB42
BE55	VSS	AB39
BE9	VSS	AB37
BE1	VSS	AB35
BD57	VSS	AB33
BD53	VSS	AB32
BD50	VSS	AB30
BD46	VSS	AB28
BD42	VSS	AB26
BD39	VSS	AB24
BD14	VSS	AB23
BB71	VSS	AB21
BB62	VSS	AB19
BB57	VSS	AB17
BB53	VSS	AB15
BB50	VSS	AB14
BB46	VSS	AB9
BB42	VSS	AA66
BB39	VSS	AA64
BB7	VSS	AA62
BB1	VSS	AA67
BA70	VSS	AA53
AY71	VSS	AA50
AY66	VSS	AA46
AY62	VSS	AA42
AY59	VSS	AA41
AY55	VSS	AA37
AY51	VSS	AA35
AY48	VSS	AA33
AR42	VSS	AA32
AR39	VSS	AA30
AR35	VSS	AA28
AR33	VSS	AA26
AR32	VSS	AA24
AR30	VSS	AA23
AR28	VSS	AA22
AR26	VSS	AA21
AR24	VSS	AA19
AR23	VSS	AH62
AR21	VSS	AH57
AR19	VSS	AH55
AR17	VSS	BV66
AR15	VSS	E30
AR14	VSS	ET68
AR4	VSS	E16
AR1	VSS	E12
AP70	VSS	D41
AP64	VSS	D38
AN62	VSS	D34
AN55	VSS	D31
AY44	VSS	BN1
AY41	VSS	BN71
AY37	VSS	BN1
AY35	VSS	BL71
AY33	VSS	D27
AY32	VSS	D24
AY30	VSS	D21
AY28	VSS	D20
AY26	VSS	H71
		F71
		E69
		E68
		A66
		A64
		E5
		C68

VSS

AUBURNDALE-1-GP-U3-NF



CPU1J

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AH53	VSS	A40
AH51	VSS	A36
AH50	VSS	A33
AH48	VSS	A29
AH46	VSS	A26
AH44	VSS	A22
AH42	VSS	A19
AH41	VSS	A15
AH39	VSS	A12
AH37	VSS	A8
AH35	VSS	B62
AH33	VSS	B58
AH32	VSS	B55
AH30	VSS	B51
AH28	VSS	B48
AH26	VSS	B44
AH24	VSS	A59
AH23	VSS	A55
AH21	VSS	A52
AH19	VSS	A48
AH17	VSS	A45
AH15	VSS	AA17
AH4	VSS	AA15
AG64	VSS	AA14
AG9	VSS	AA4
AG6	VSS	W89
AF69	VSS	W62
AF62	VSS	W57
AF1	VSS	W53
AE70	VSS	W50
AE64	VSS	W46
AD62	VSS	W42
AD57	VSS	W6
AD53	VSS	W1
AD50	VSS	V70
AD46	VSS	U64
AD42	VSS	U62
AD4	VSS	U57
AC67	VSS	U53
AC64	VSS	U50
AC10	VSS	U46
AC5	VSS	U42
AC1	VSS	U39
AB70	VSS	U9
AB62	VSS	U4
AB57	VSS	T1
AB53	VSS	R70
AB50	VSS	R62
AB46	VSS	R57
AB42	VSS	R53
AB39	VSS	R50
AB37	VSS	R46
AB35	VSS	R42
AB33	VSS	R5
AB32	VSS	P4
AB30	VSS	N63
AB28	VSS	N57
AB26	VSS	N53
AB24	VSS	N50
AB23	VSS	N46
AB21	VSS	N30
AB19	VSS	N21
AB17	VSS	N15
AB15	VSS	M53
AB14	VSS	M42
AB9	VSS	M36
AA66	VSS	M1
AA64	VSS	L70
AA62	VSS	L57
AA67	VSS	L48
AA53	VSS	L47
AA50	VSS	L13
AA46	VSS	K64
AA42	VSS	K53
AA39	VSS	K43
AA37	VSS	K36
AA35	VSS	K34
AA33	VSS	K32
AA32	VSS	K25
AA30	VSS	K17
AA28	VSS	K11
AA26	VSS	K6
AA24	VSS	K4
AA23	VSS	J65
AA21	VSS	J57
AJ70	VSS	J48
F20	VSS	J47
F4	VSS	J40
E37	VSS	J9
E33	VSS	H53
E30	VSS	H43
ET68	VSS	H36
E16	VSS	H1
E12	VSS	G70
D41	VSS	G57
D38	VSS	G53
D34	VSS	G48
D31	VSS	G47
BN1	VSS	G43
BN71	VSS	G30
BL71	VSS	G24
D27	VSS	G20
D24	VSS	G15
D21	VSS	F61
D17	VSS	F48
D13	VSS	F47
D10	VSS	F28
D6	VSS	
A66	VSS	
A64	VSS	
E5	VSS	
C68	VSS	

VSS

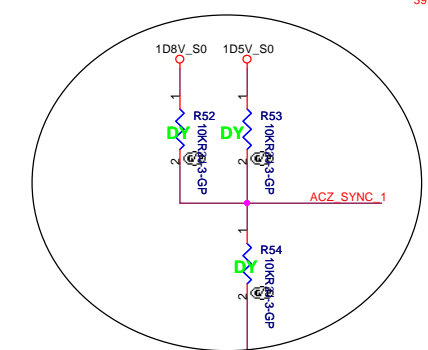
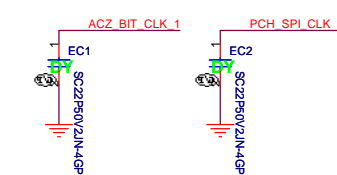
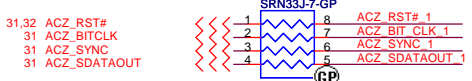
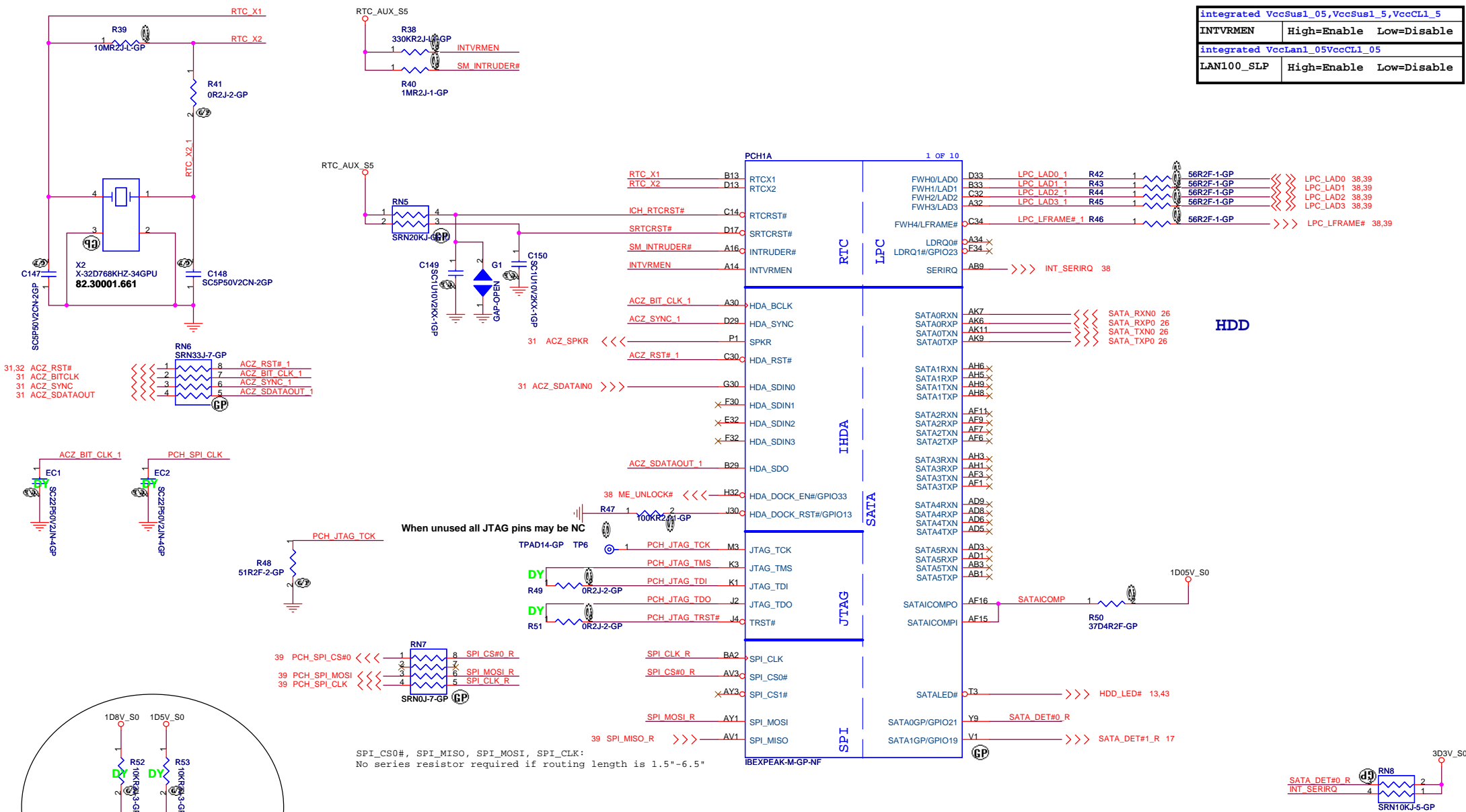
AUBURNDALE-1-GP-U3-NF



DVT 1ST

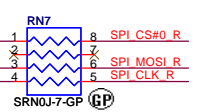
緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
CPU SFF 8 of 8(VSS)			
Title			
Size A3	Document Number	TUCANA	Rev SB
Date: Wednesday, July 07, 2010	Sheet	11	of 56

Integrated VccSus1_05,VccSus1_5,VccCLI_5		
INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCLI_05		
LAN100_SLP	High=Enable	Low=Disable

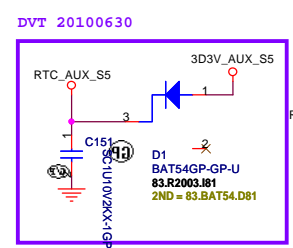


If reserve 1.5/1.8V option for VCCVRM. Not Power plan change only.
Please refer figure2.HDA_SYNC will be strap to define VCCVRM is 1.5 or 1.8V source.
Means need have Pull high/low resistor to option,
P/H voltage base on HAD Link is 1.5V or 3.3V(Figure 3).

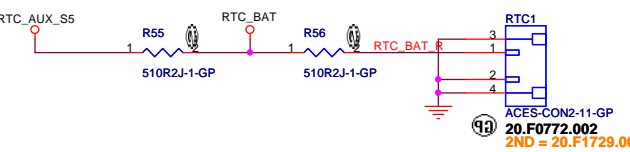
When unused all JTAG pins may be NC



SPI_CS#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"



RTC CONN



DVT 1ST

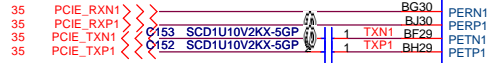
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH 1 of 9(SATA/RTC/HDA)**

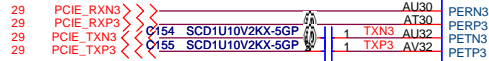
Size: A3 Document Number: **TUCANA** Rev: **SB**

Date: Wednesday, July 07, 2010 Sheet 12 of 56

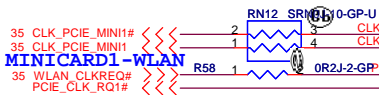
MINICARD1-WLAN



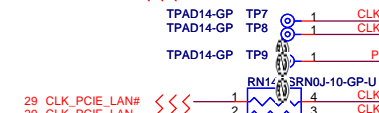
LAN



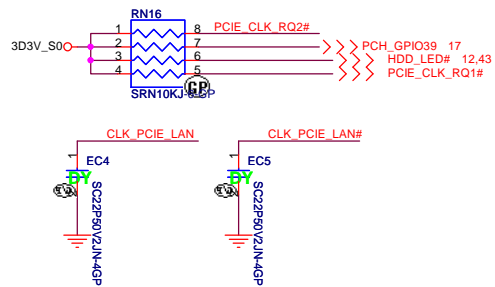
MINICARD1-WLAN



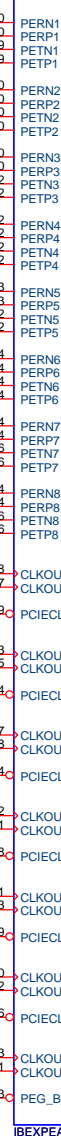
LAN



PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.
 PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).



PCH1B



PCI-E*



PEG



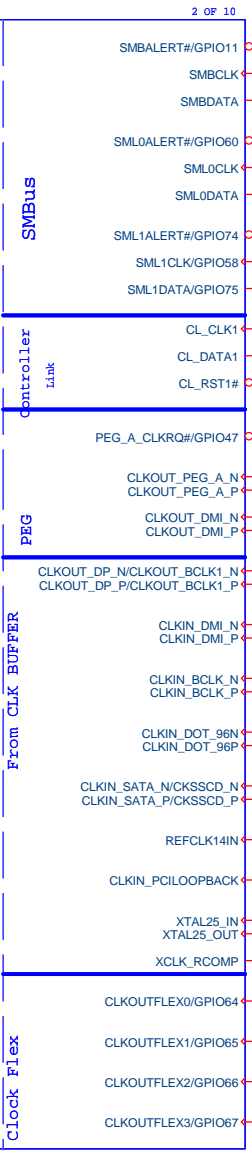
From CLK BUFFER



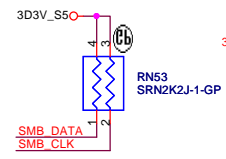
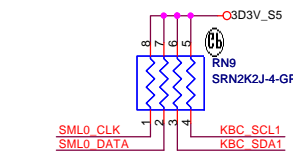
Clock Flex



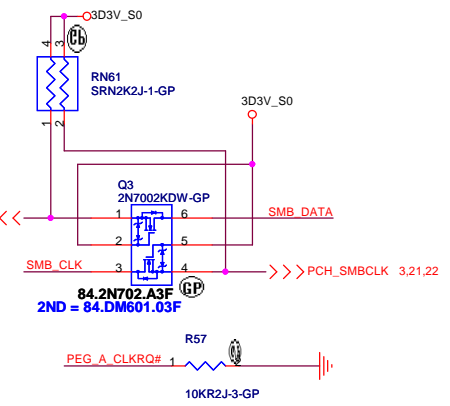
IBXPEAK-M-GP-NF



EC_SW# 14,38



3.21,22 PCH_SMBDATA <<<



CLK_DMI# 3

CLK_CPU_BCLK# 3

DREFCLK# 3

CLK_SATA# 3

CLK_ICH14 3

CLK_PCIE_FB 16

XTAL25_IN

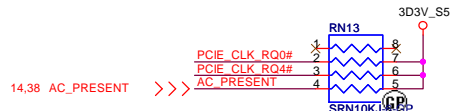
3.3MHZ

3.3MHZ

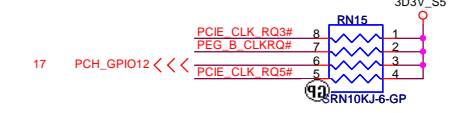
3.3MHZ

4.8MHZ

3.3MHZ

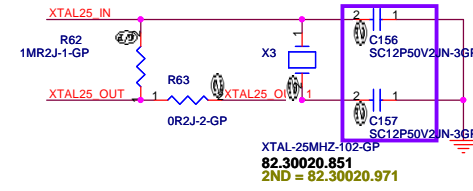


14,38 AC_PRESENT >>>



17 PCH_GPI012 <<<

DVT 20100625
 Change C156, C157 to 12pF
 for Crystal vendor Test



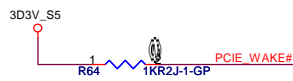
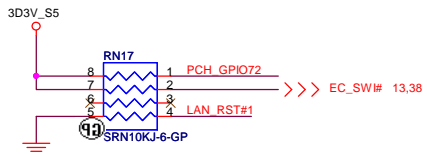
<Core Design>

緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

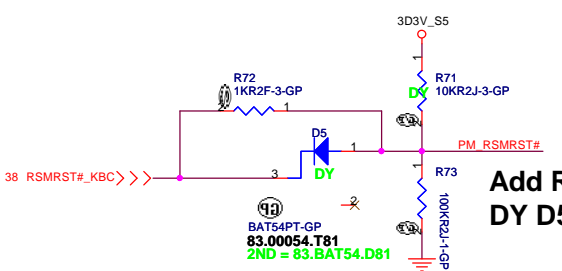
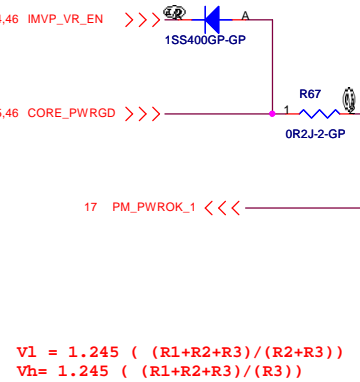
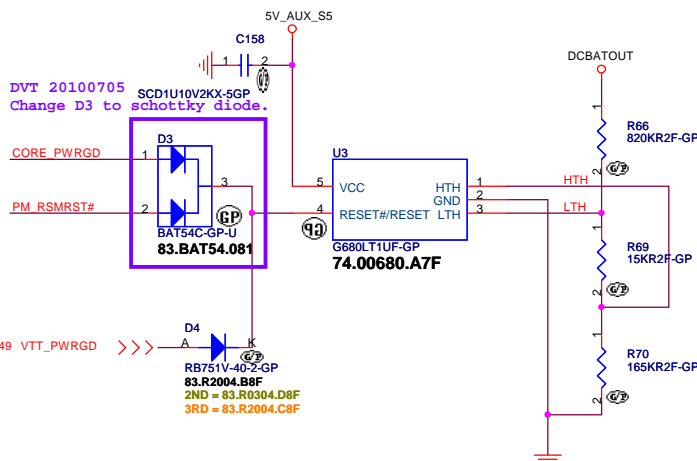
Title: PCH 2 of 9(PCIE/CLK/SMB)

Size: A3 Document Number: TUCANA Rev: SB

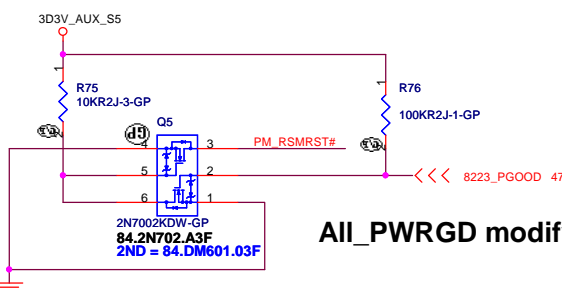
Date: Wednesday, July 07, 2010 Sheet: 13 of 56



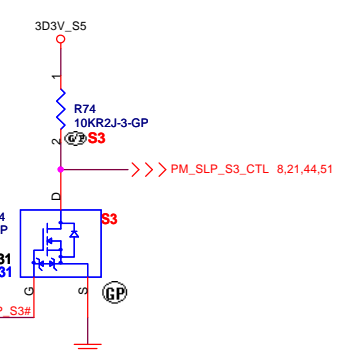
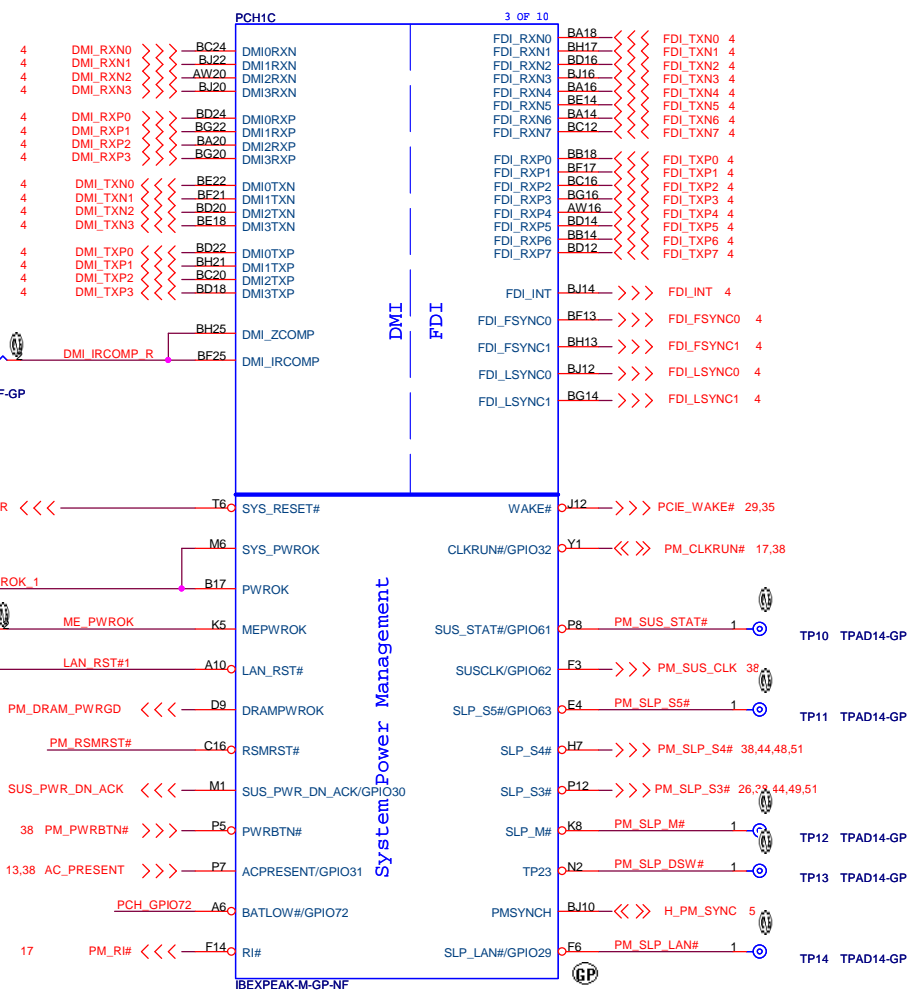
Delete PM_PWRBTN# pull high



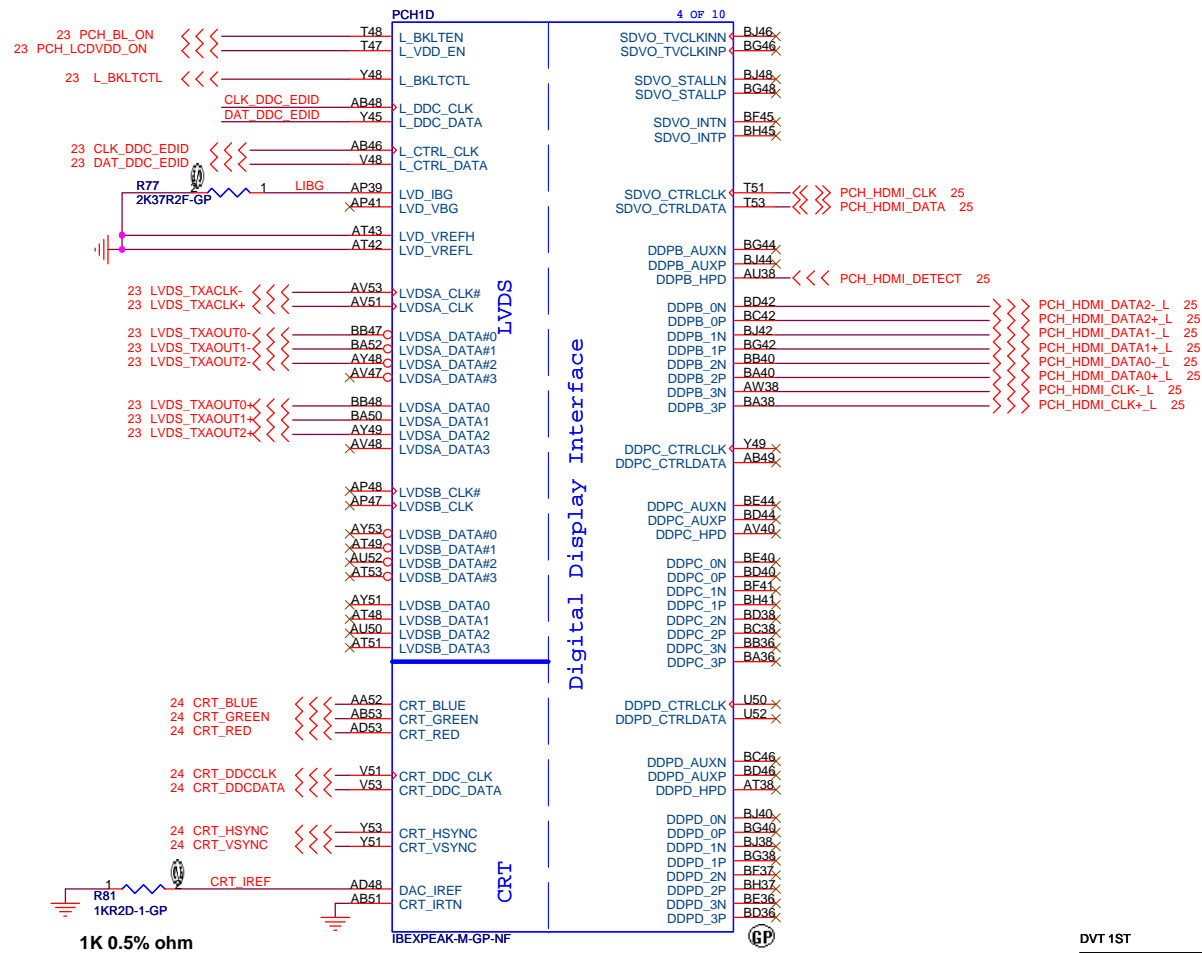
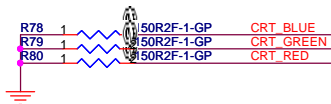
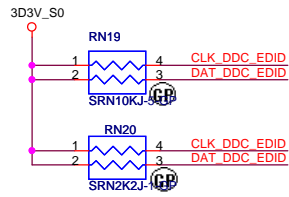
Add RTC Data lose function
DY D5



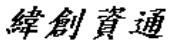
All_PWRGD modify 51123_PGOOD from 3V/5V power

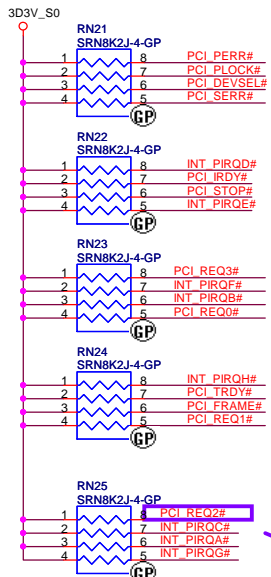


Panel backlight enable control for LVDS -
used to gate power into the backlight circuit



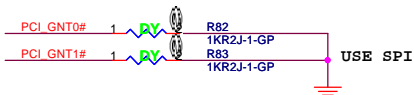
DVT 1ST

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title PCH 4 of 9(LVDS/CRT/DP)	
Size Custom	Document Number TUCANA
Date: Wednesday, July 07, 2010	Rev SB



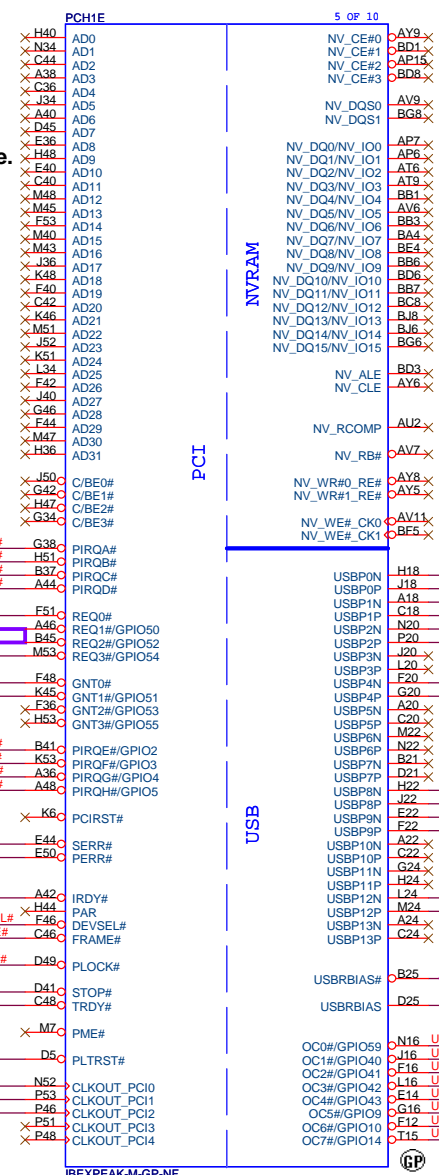
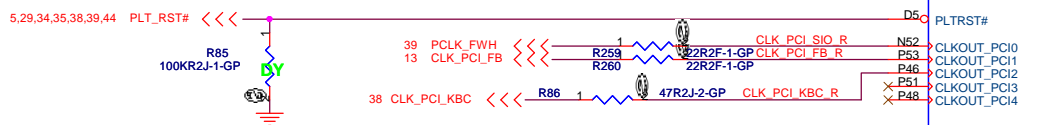
These pins are left as NC, because the function is disable.

These pins are left as NC, because the function is disable.



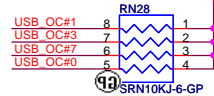
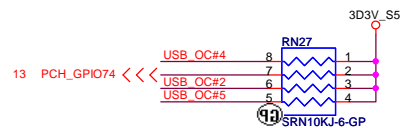
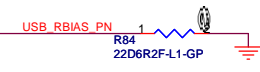
DVT 20100621
Add PCI_REQ2# Pull-High to 3D3V_S5
by hang-up issue

BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI



USB Table

Pair	Device
0	External #0
1	External #1
2	CardReader
3	NC
4	External #2
5	NC
6	NC
7	NC
8	WLAN/WiMAX
9	CAMERA (HS)
10	NC
11	NC
12	BLUETOOTH (FS)
13	NC



DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH 5 of 9(PCI/USB)**

Size A3 Document Number **TUCANA** Rev **SB**

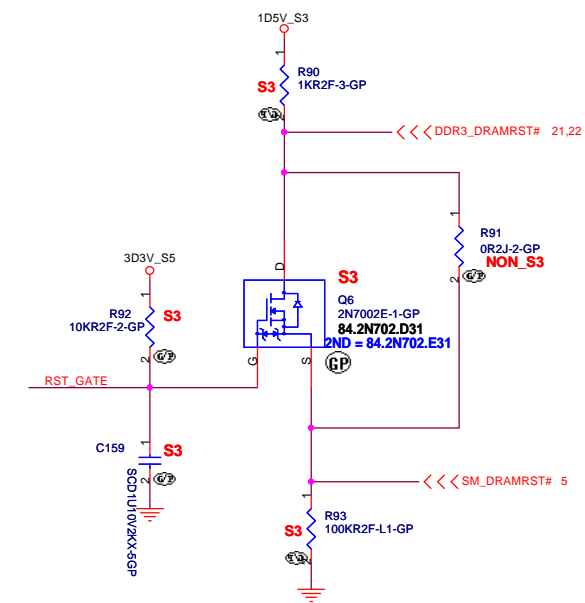
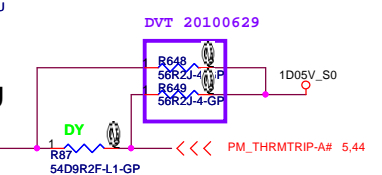
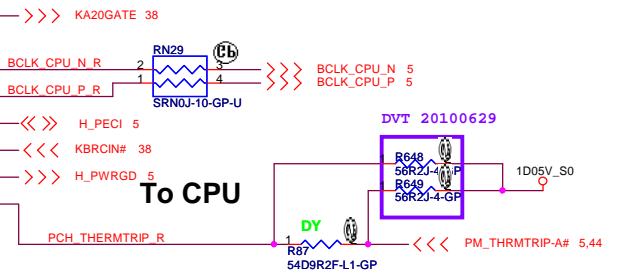
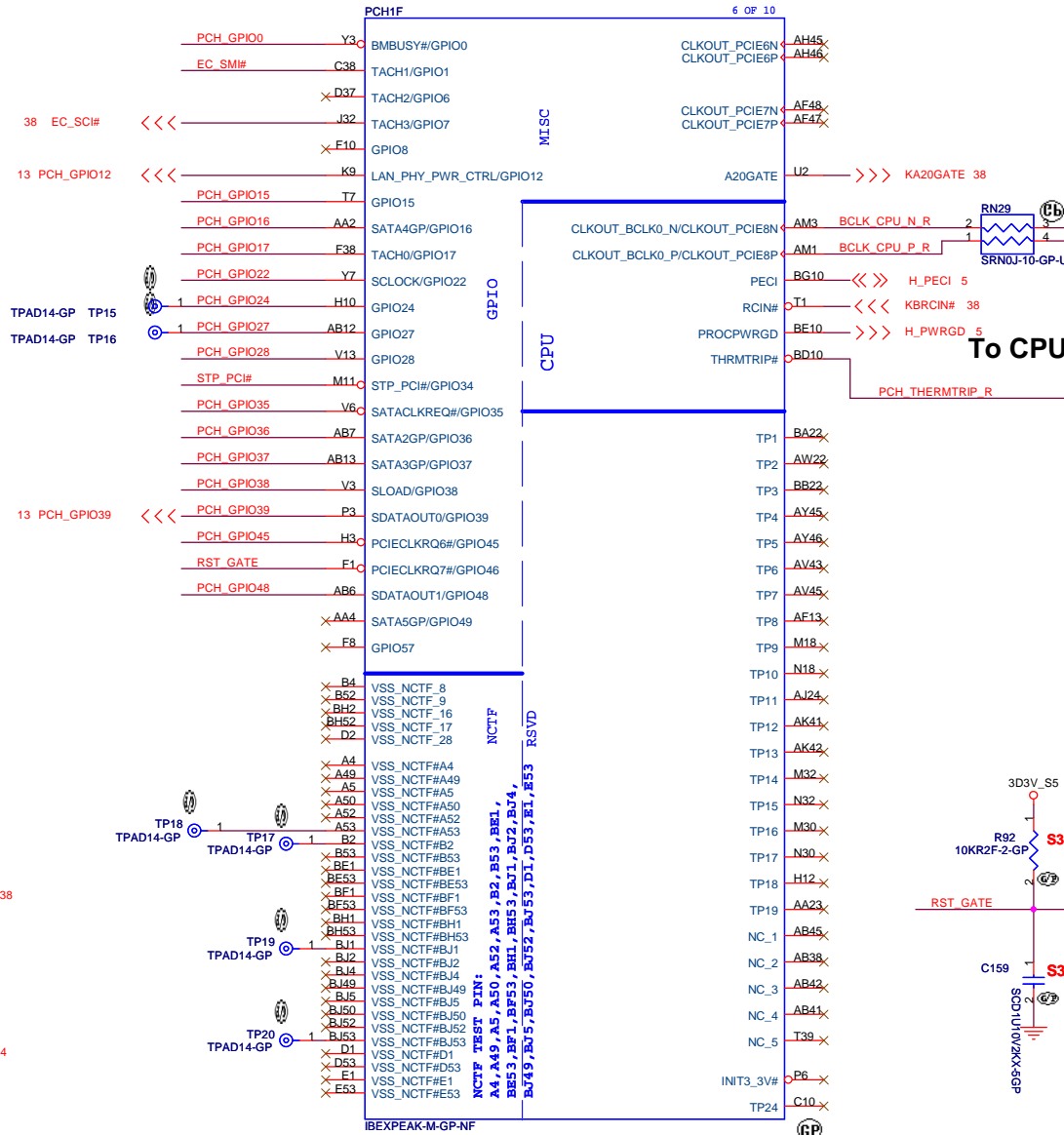
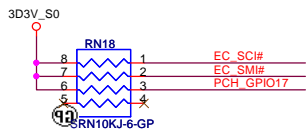
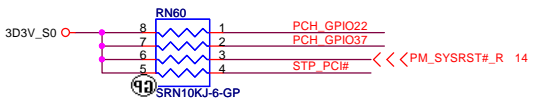
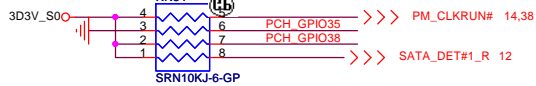
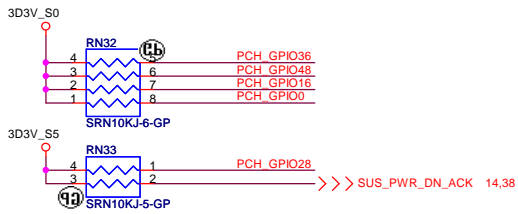
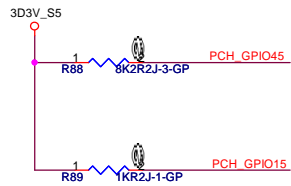
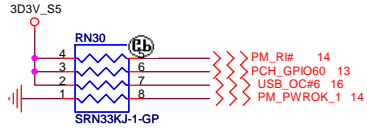
Date: Wednesday, July 07, 2010 Sheet 16 of 56

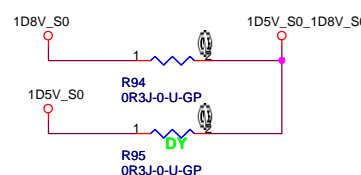
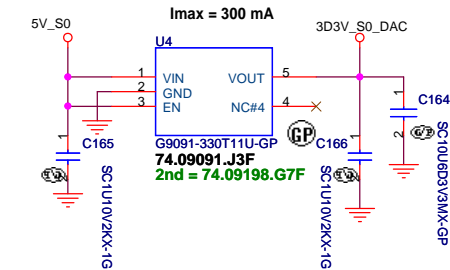
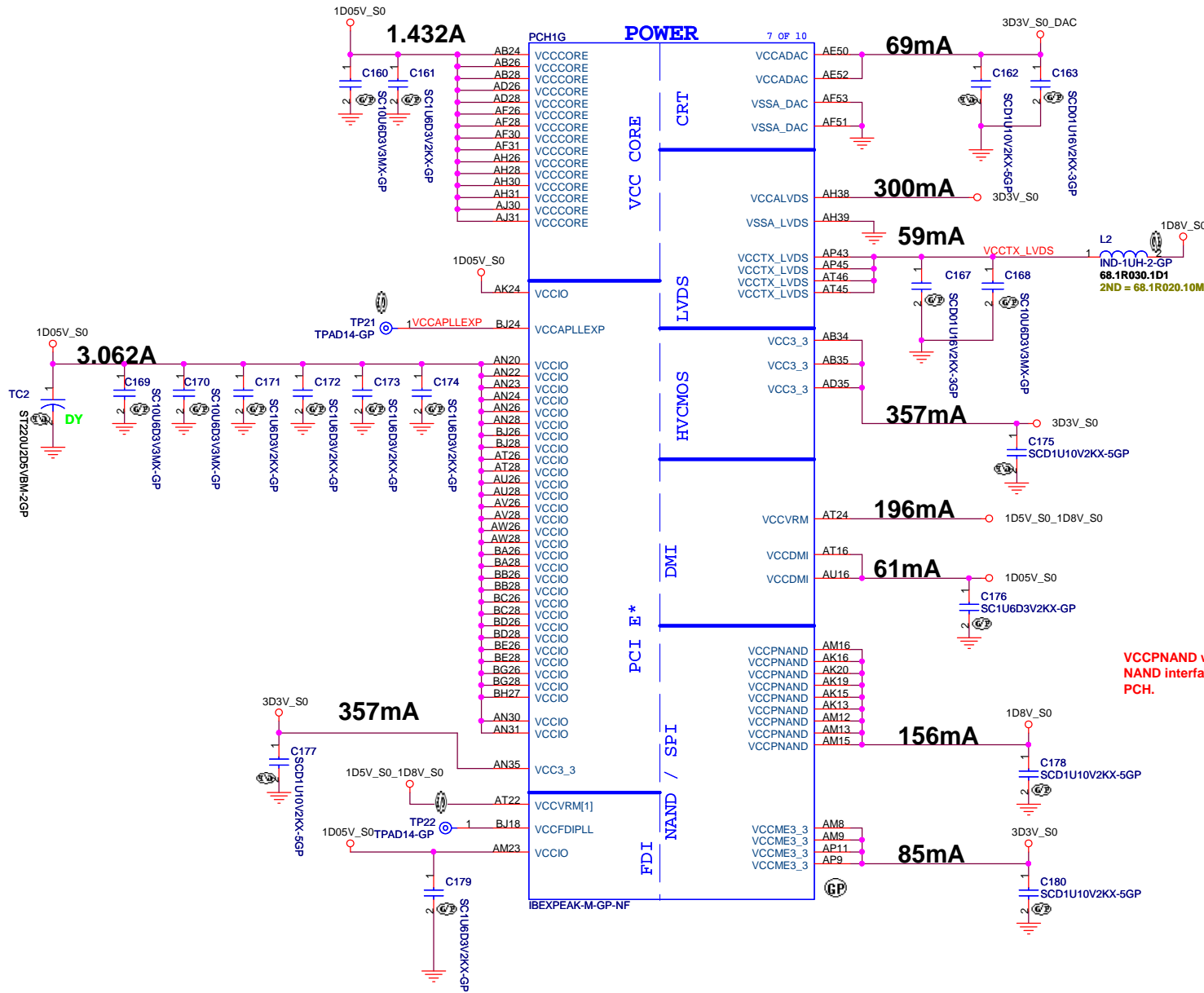
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.

Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.





VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.

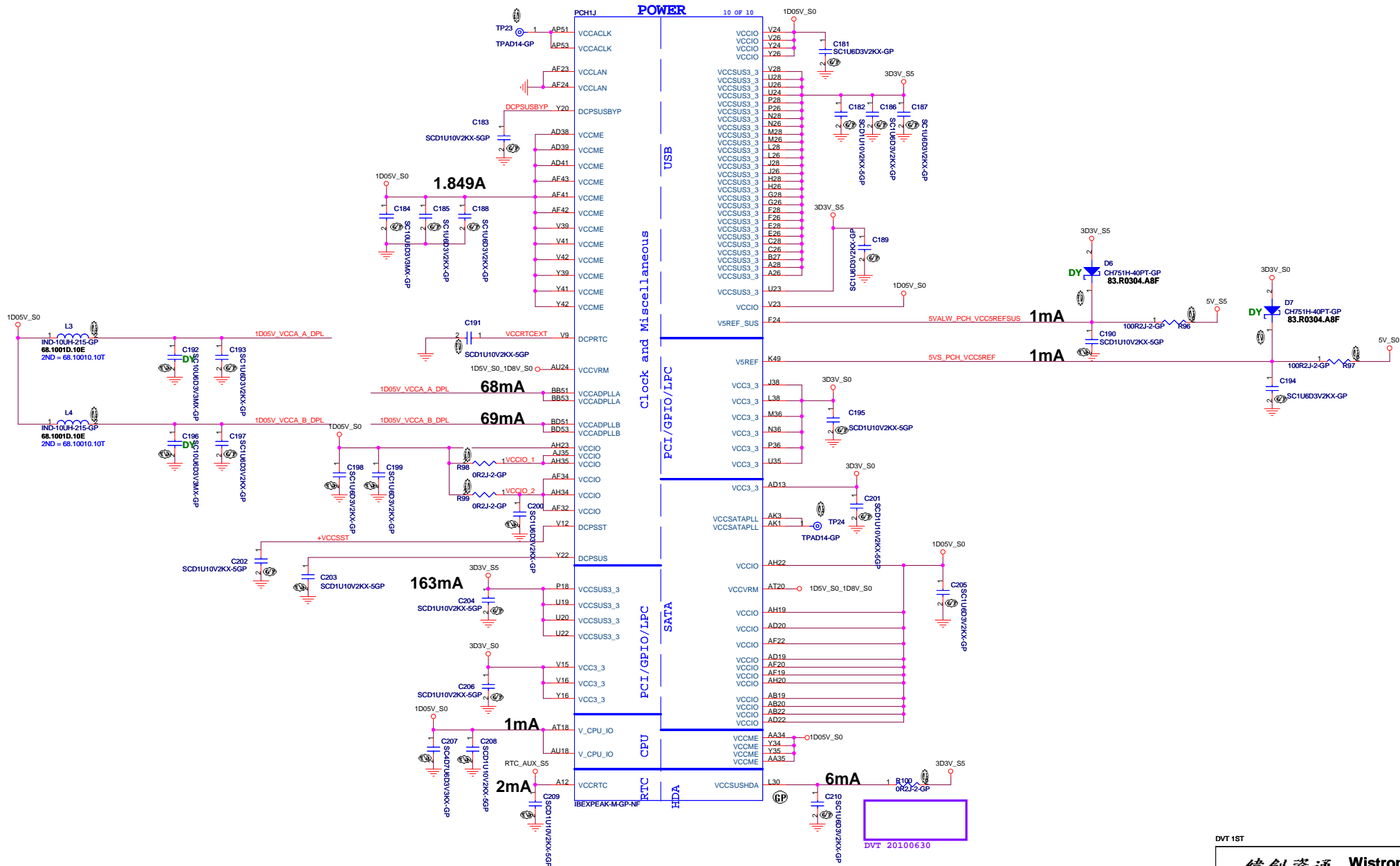
DVT 1ST

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title **PCH 7 of 9(PWR/CORE/LVDS)**

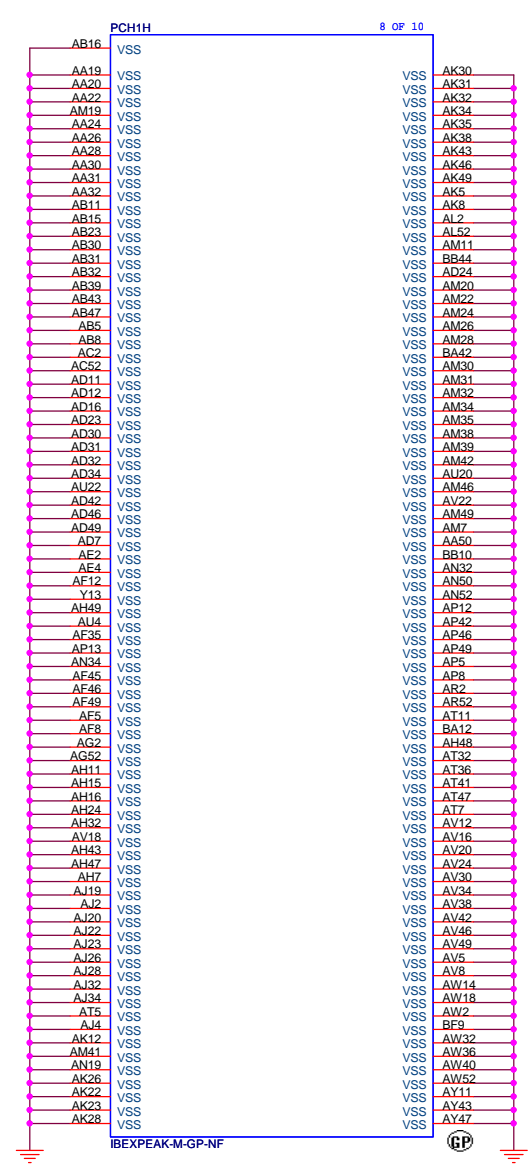
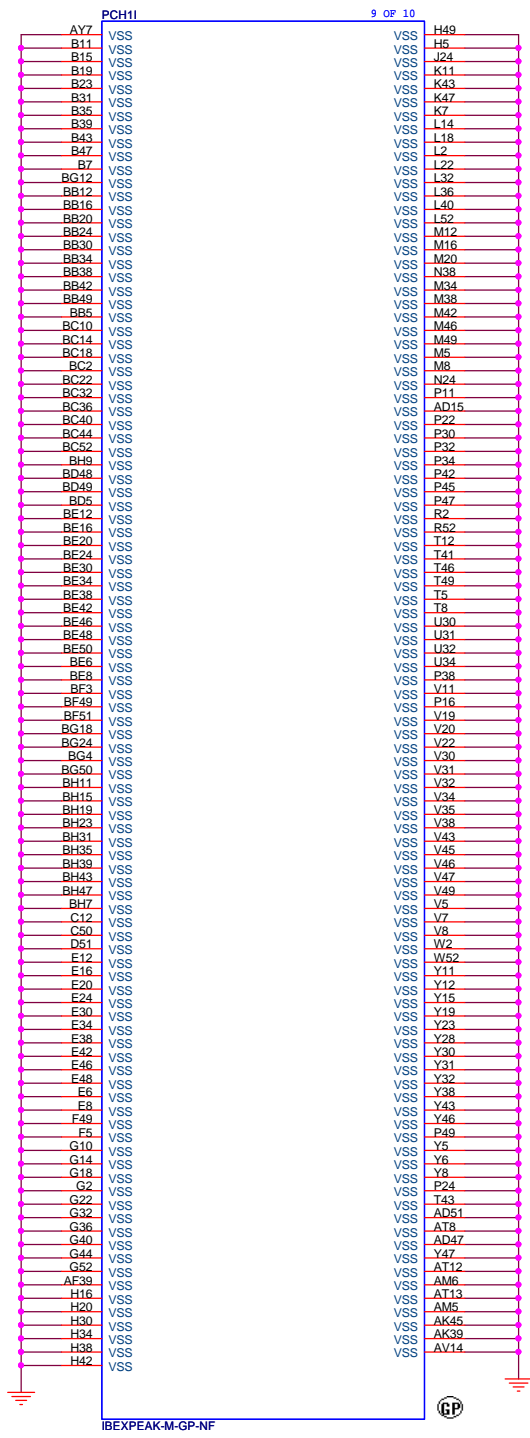
Size	Document Number	Rev
Custom	TUCANA	SB

Date: Wednesday, July 07, 2010 Sheet 18 of 56



DVT 1S1

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hei Tai Wu Rd., Hsiehshih, Taipei Hsein 221, Taiwan, R.O.C.	
Title PCH 8 of 9(PWRISATAUSB)			
Size Custom	Document Number	TUCANA	Rev SB
Date: Wednesday, July 07, 2010		Sheet 19	of 56



DVT 1ST

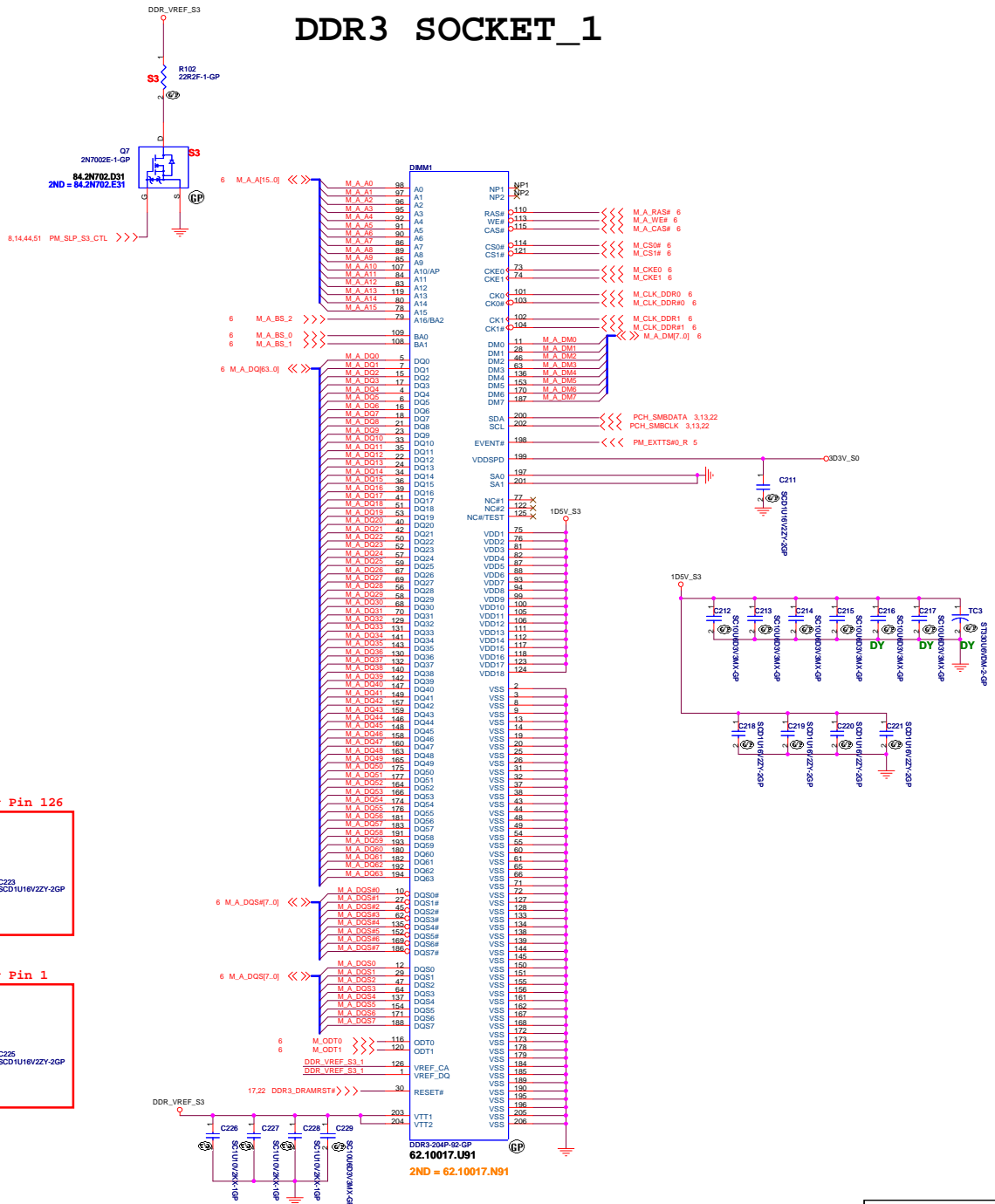
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title **PCH 9 of 9(VSS)**

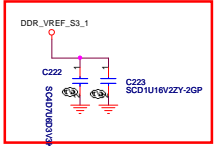
Size A3	Document Number TUCANA	Rev SB
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Date: Wednesday, July 07, 2010 Sheet 20 of 56

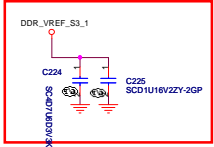
DDR3 SOCKET_1



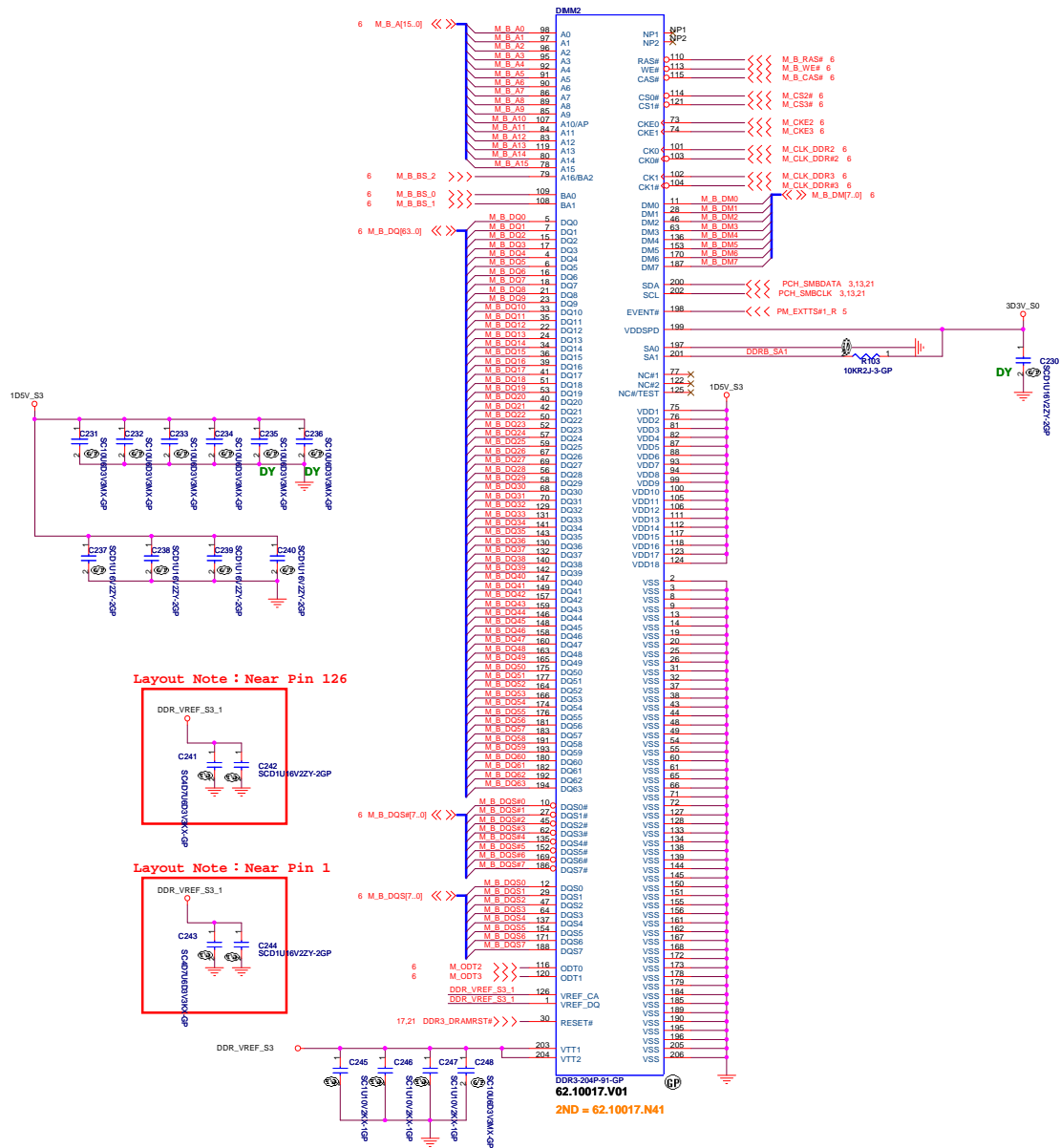
Layout Note : Near Pin 126



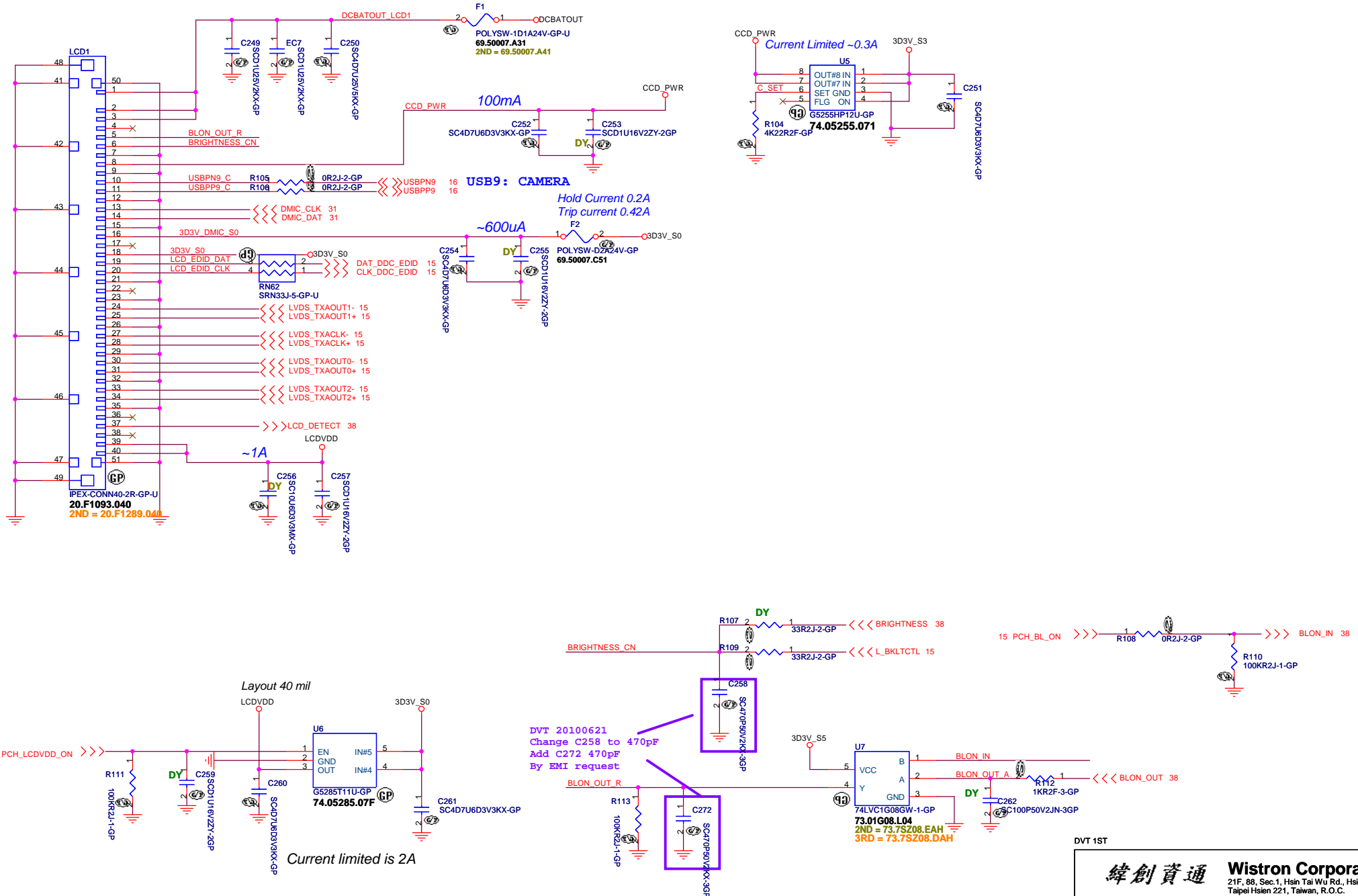
Layout Note : Near Pin 1



DDR3 SOCKET_2



LCD/CCD CONN



Layout 40 mil

Current limited is 2A

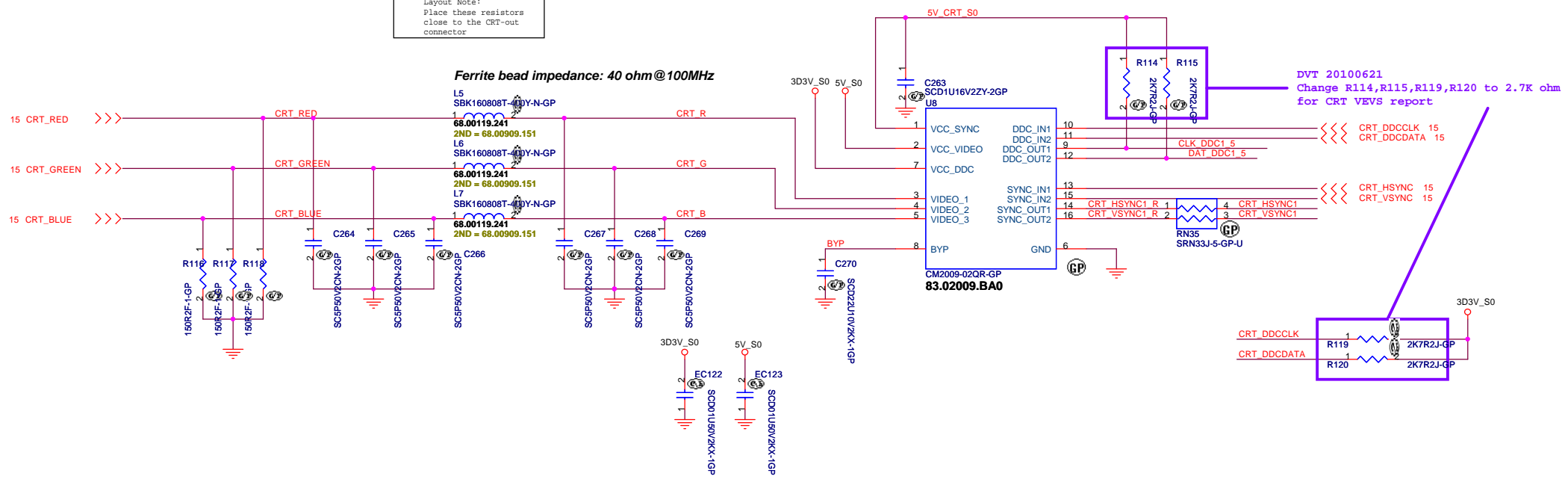
DVT 20100621
Change C258 to 470pF
Add C272 470pF
By EMI request

DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

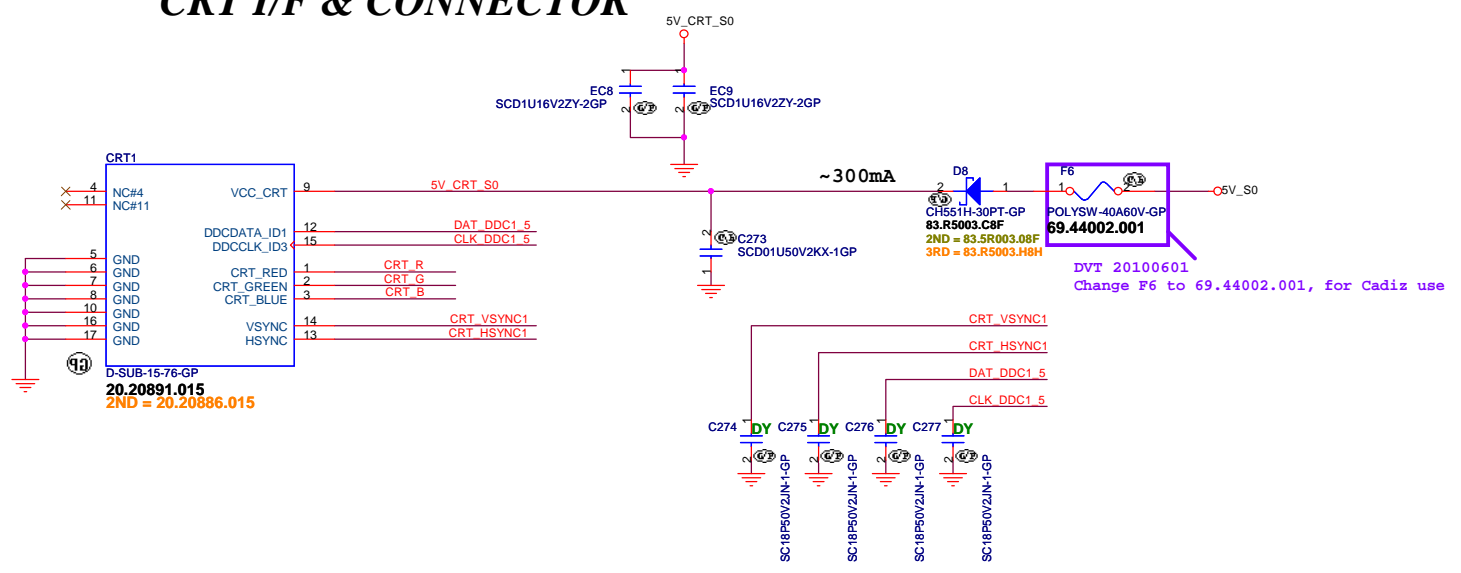
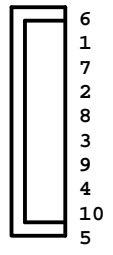
Title	LCD CONN	
Size	Document Number	Rev
	TUCANA	SB
Date:	Wednesday, July 07, 2010	Sheet 23 of 56

Layout Note:
Place these resistors
close to the CRT-out
connector



Layout Note:
* Must be a ground return path between this ground and the ground on the VGA connector.
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR



DVT 1ST

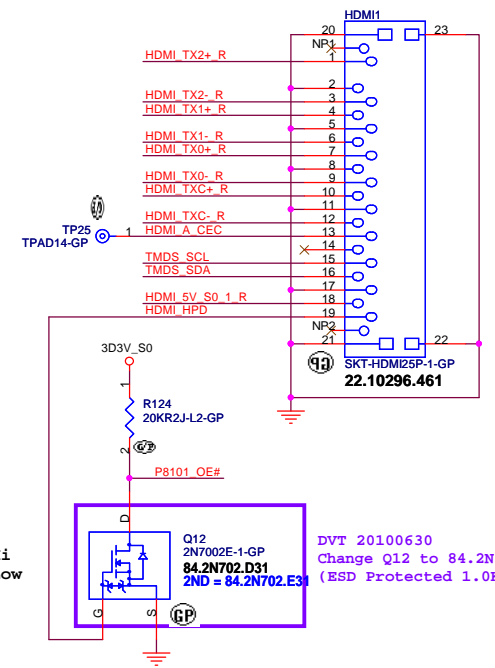
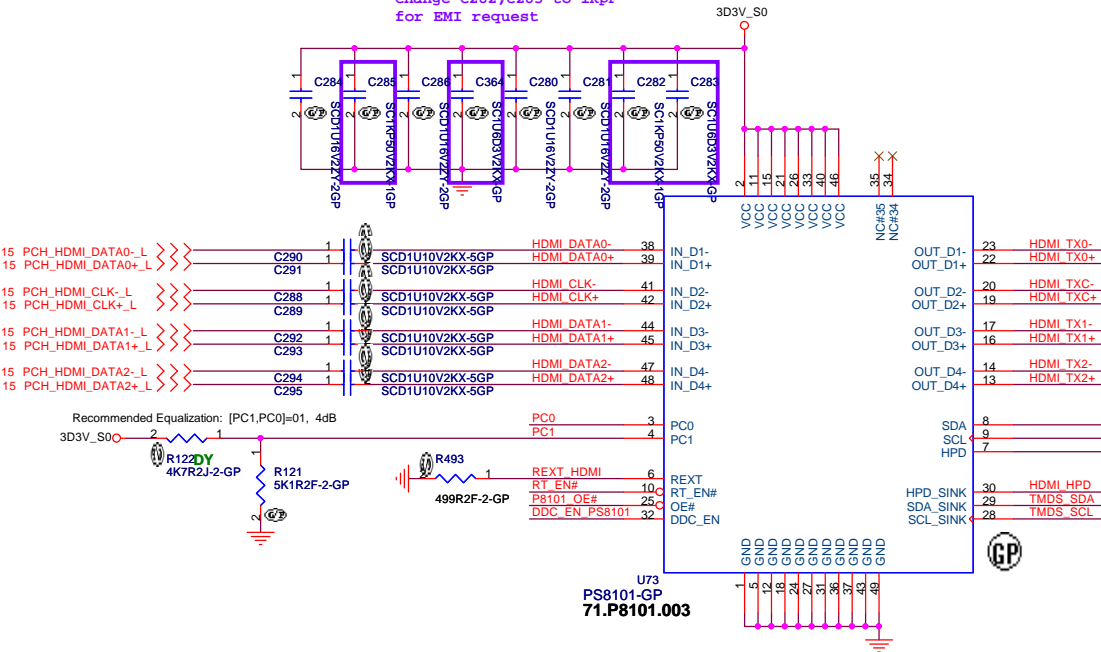
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT CONN**

Size: Document Number: **TUCANA** Rev: **SB**

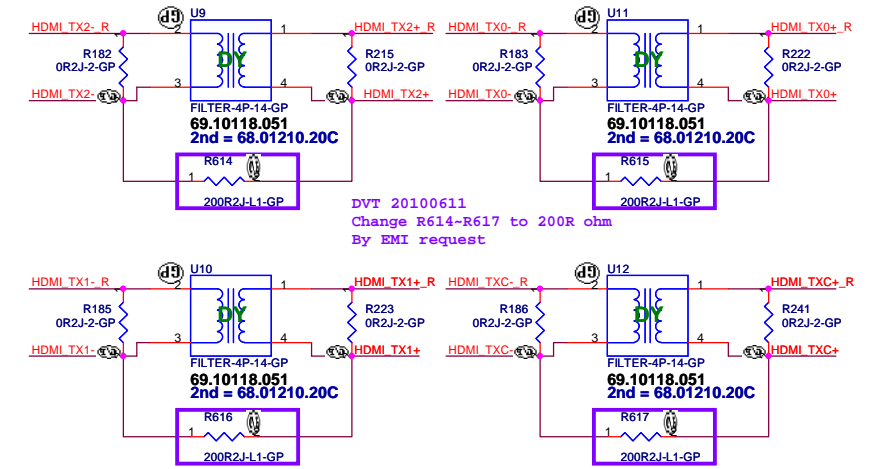
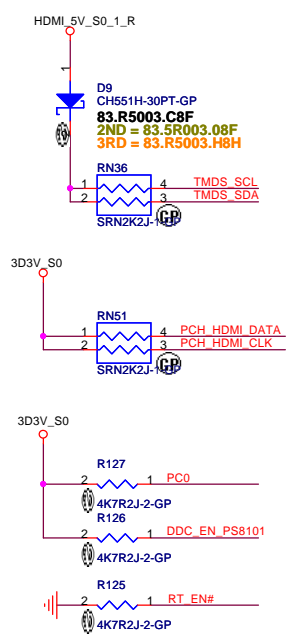
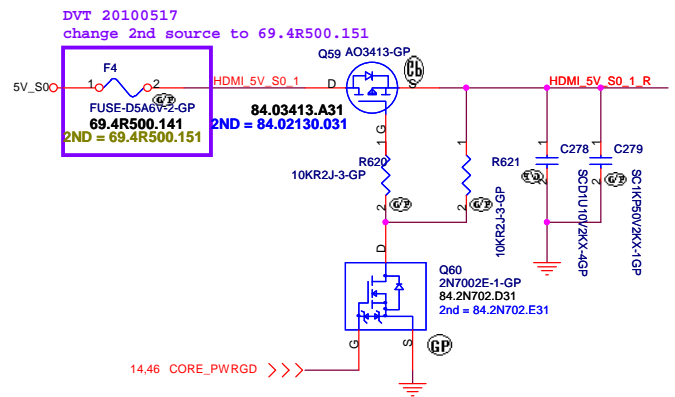
Date: Wednesday, July 07, 2010 Sheet 24 of 56

DVT 20100611
 Change C283,C364 to 1uF
 Change C282,C285 to 1KpF
 for EMI request



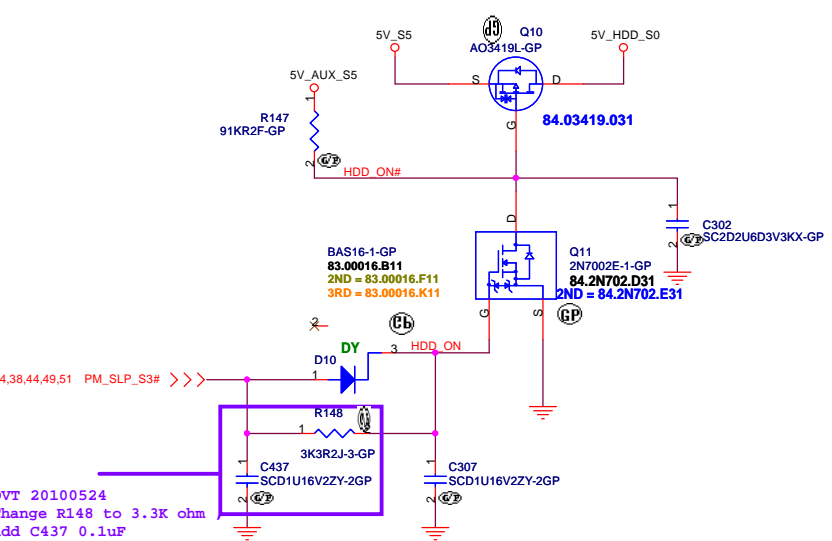
HDMI in : Hi
 HDMI out : Low

DVT 20100630
 Change Q12 to 84.2N702.D31
 (ESD Protected 1.0KV)



DVT 1ST

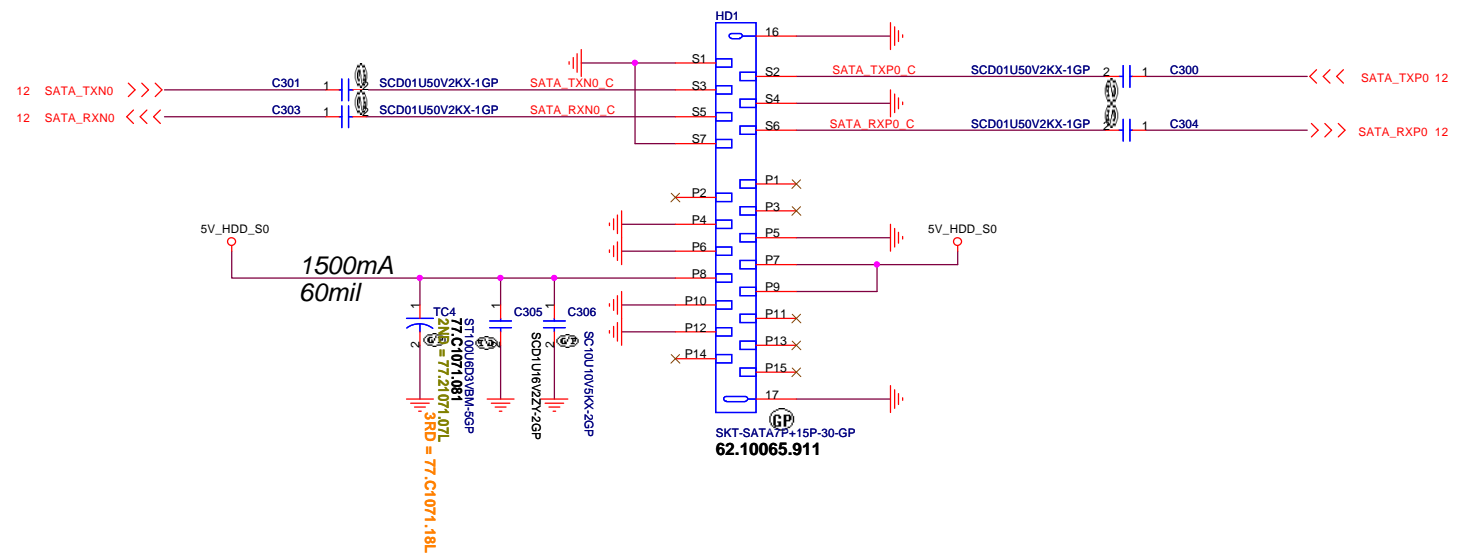
緯創資通 Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
HDMI CONN	
File	TUCANA
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Date: Wednesday, July 07, 2010	Rev SB
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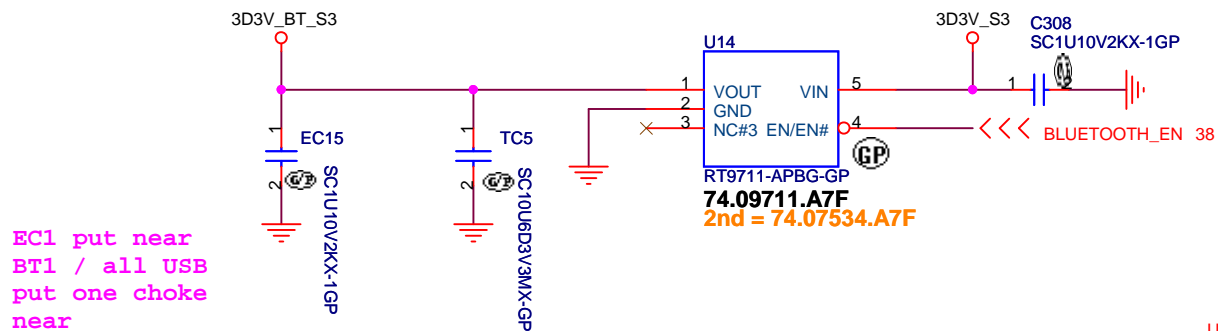
DVT 20100524
Change R148 to 3.3K ohm
add C437 0.1uF

Delay HDD power off timing for 400ms after SATA controller shut down. Control the C307 and R148 to finally tune delay timing between 500ms and 400ms.

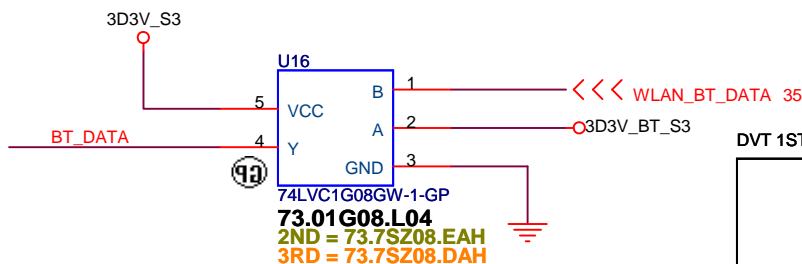
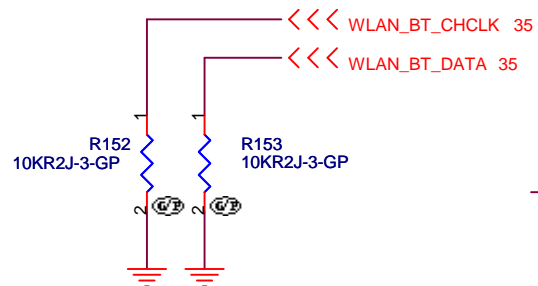
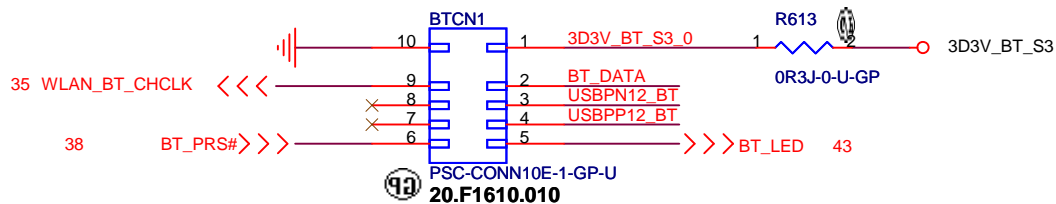
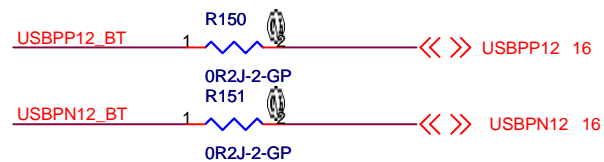
SSD SATA Connector




Bluetooth

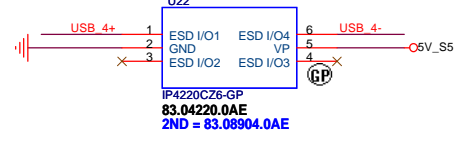
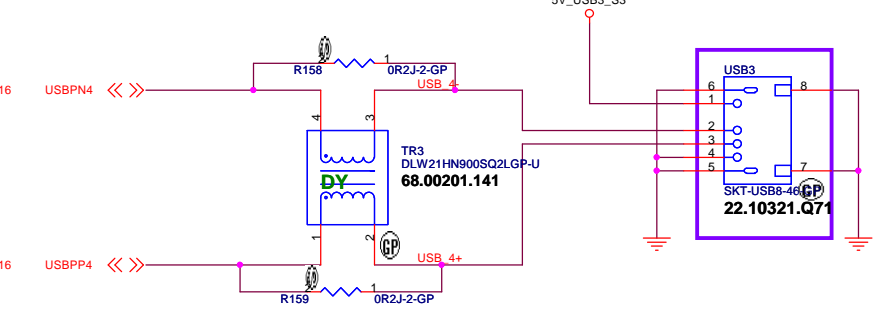
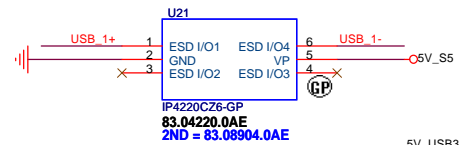
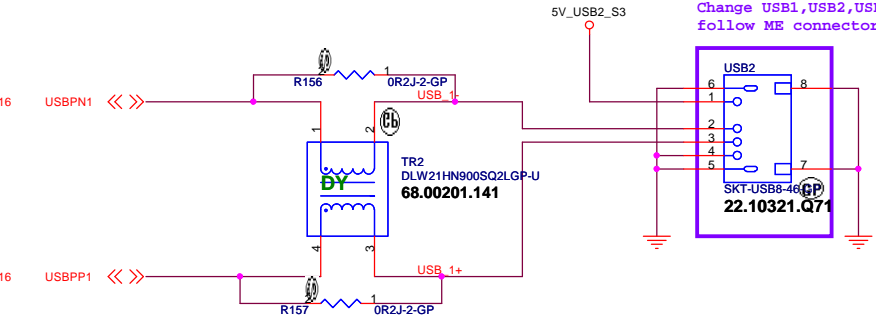
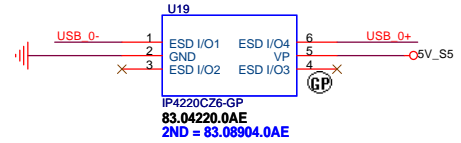
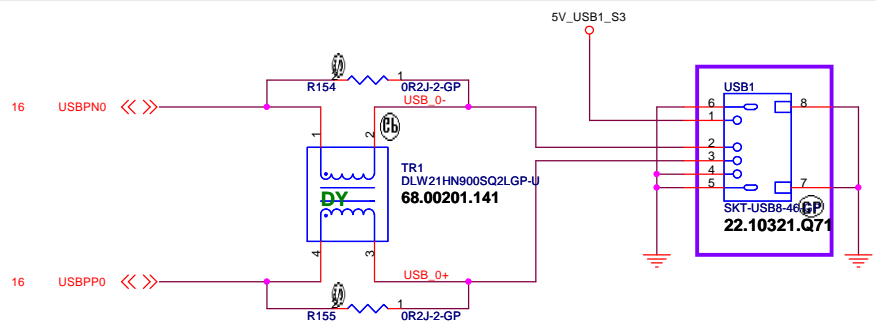


EC1 put near BT1 / all USB put one choke near connector by EMI request

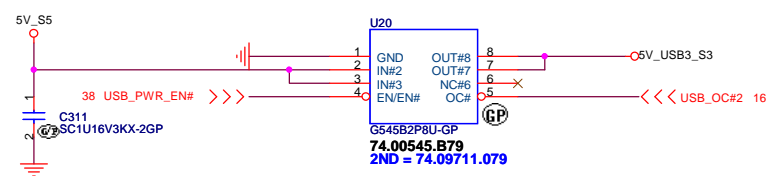
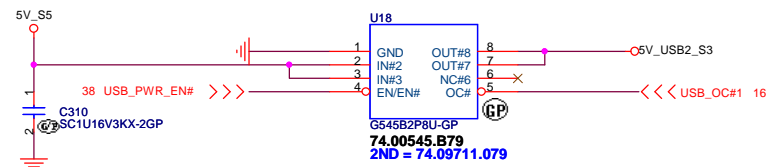
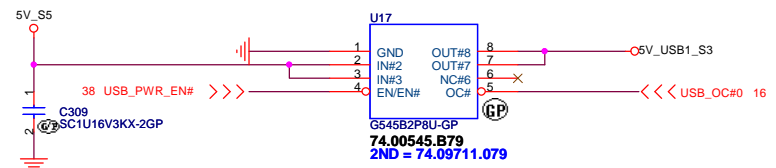


DVT 1ST

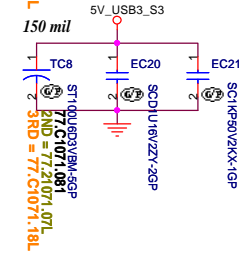
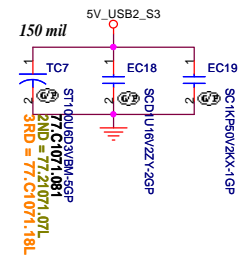
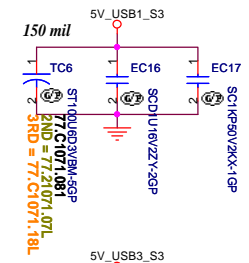
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Bluetooth		
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DVT 20100604
Change USB1,USB2,USB3 to 22.10321.Q71
follow ME connector list.

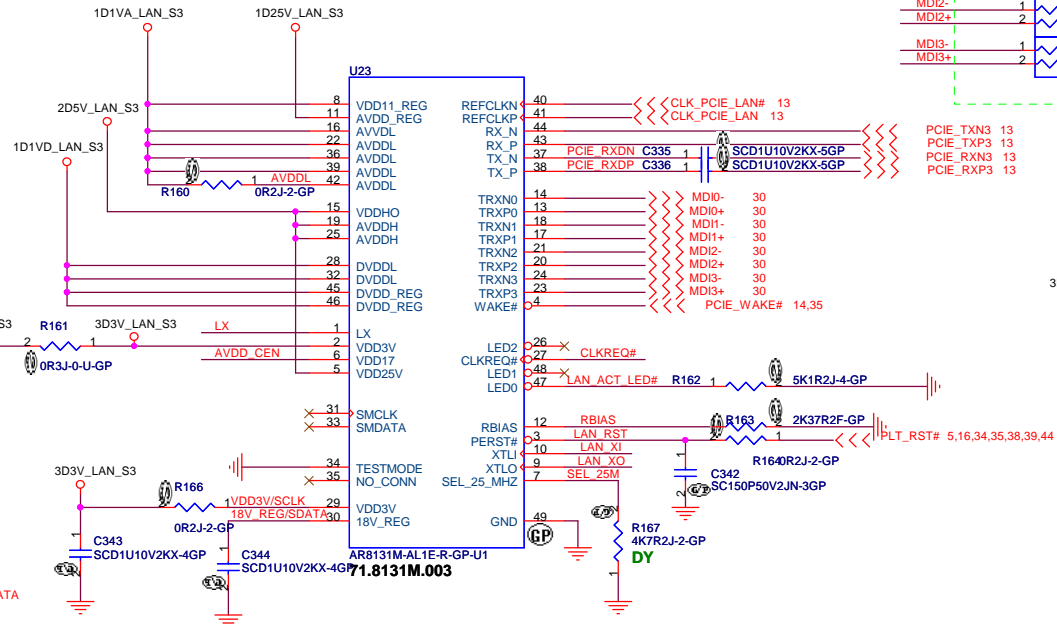
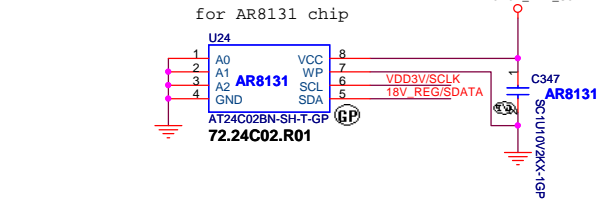
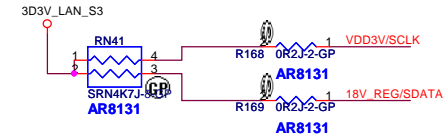
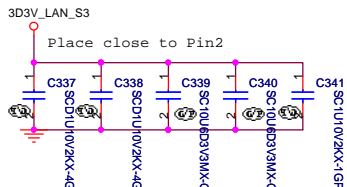
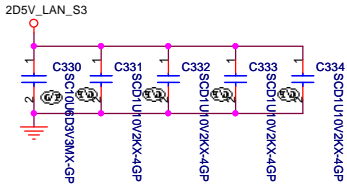
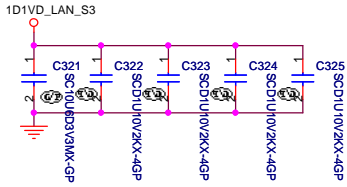
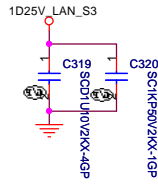
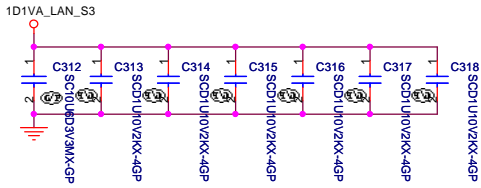


U17,U18,U20 Current Limit 1.5A

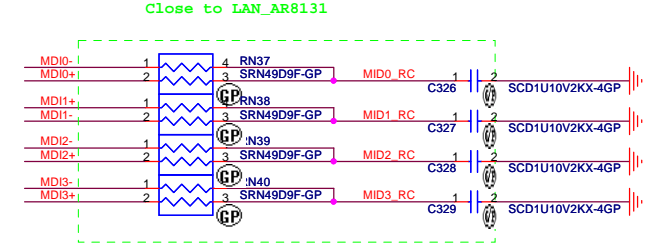
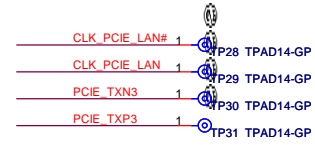


DVT 1ST

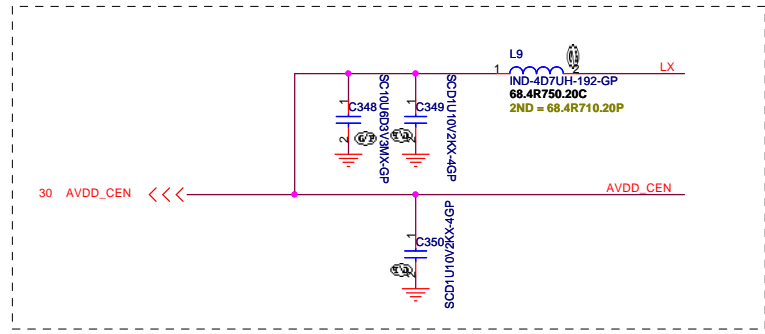
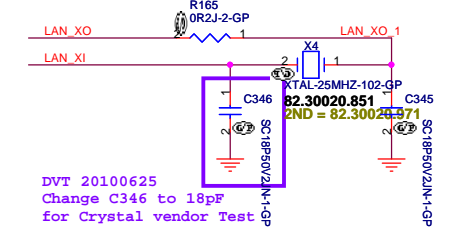
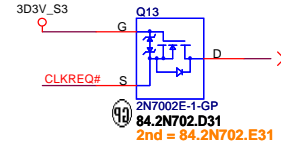
緯創資通 Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
USB CONN	
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For AR8131: RN41,R168,R169,U24,C347 are need to stuff.
 For AR8131M: RN41,R168,R169,U24,C347 are DY



Close to LAN_AR8131



Close to U3

DVT 1ST

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Title: **AR8131M**

Size: Document Number: **TUCANA** Rev: **SB**

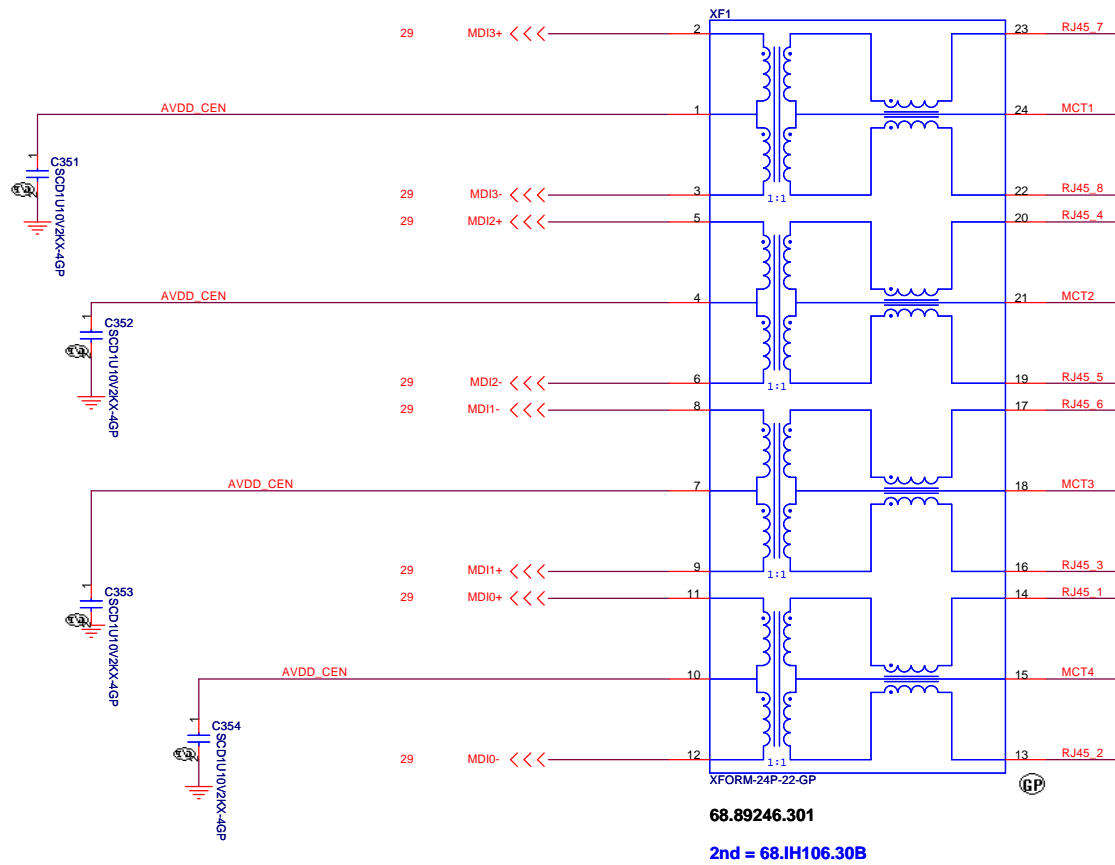
Date: Wednesday, July 07, 2010 Sheet 29 of 56

1. route on bottom as differential pairs.
2. Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3. No vias, No 90 degree bends.
4. pairs must be equal lengths.
5. 6mil trace width, 12mil separation.
6. 36mil between pairs and any other trace.
7. Must not cross ground moat, except RJ-45 moat.

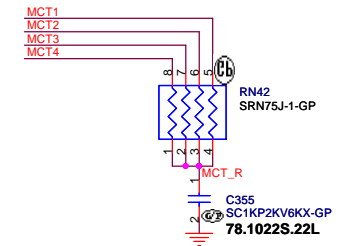
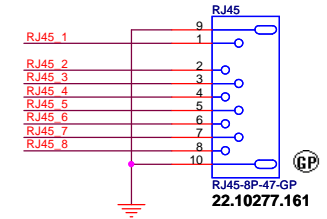
LAN Transformer

AVDD_CEN 29

GIGA Lan Transformer

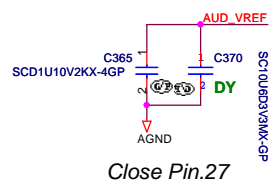
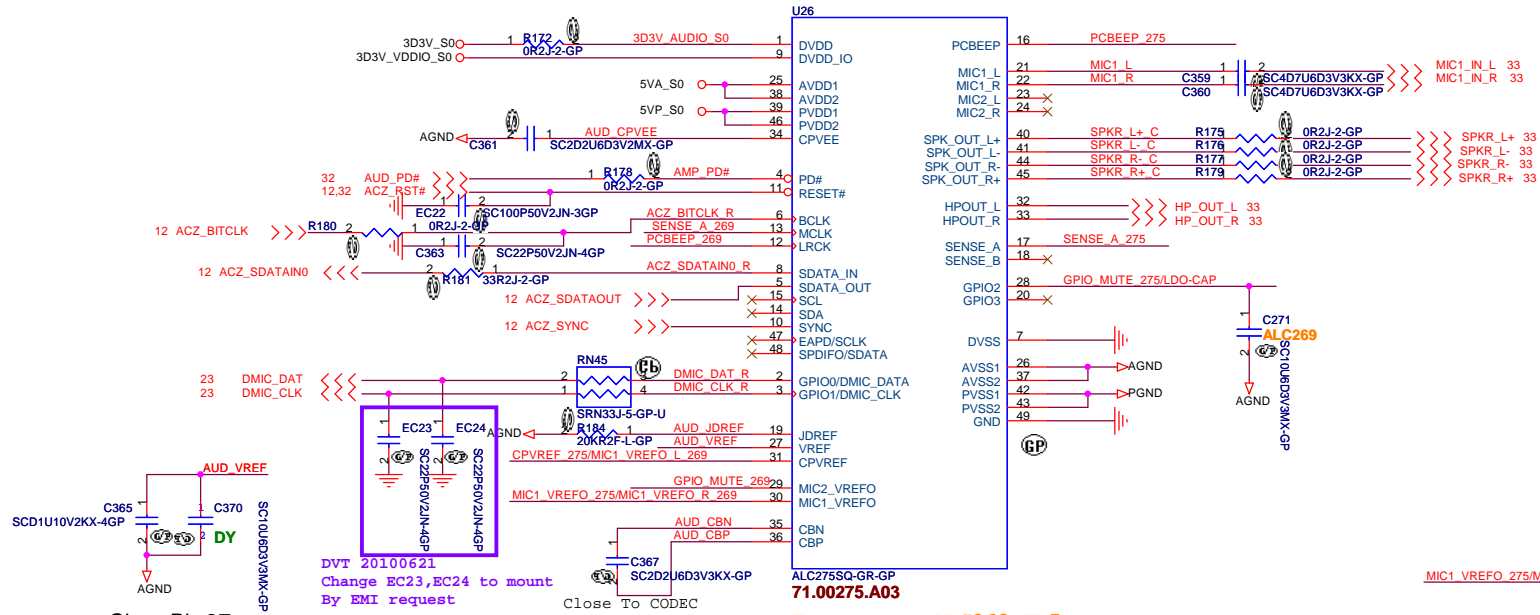
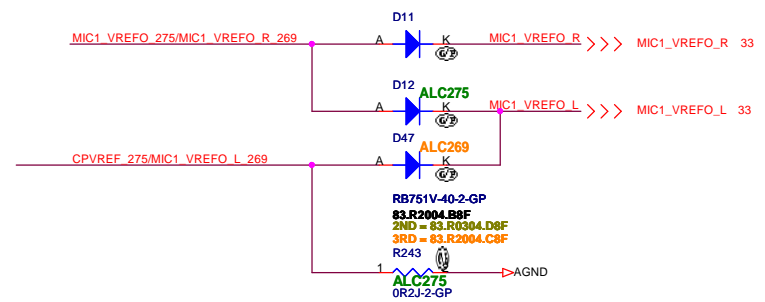
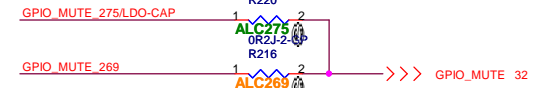
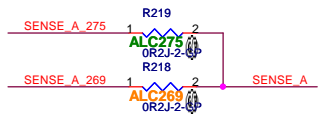
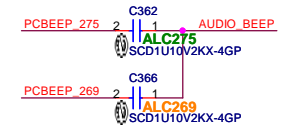
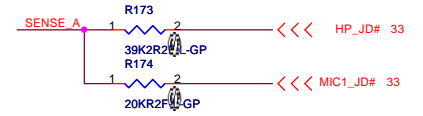
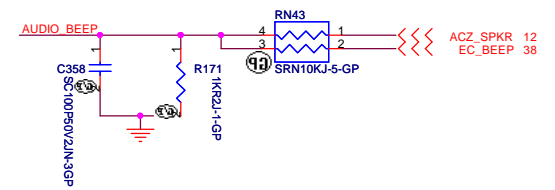
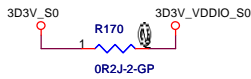
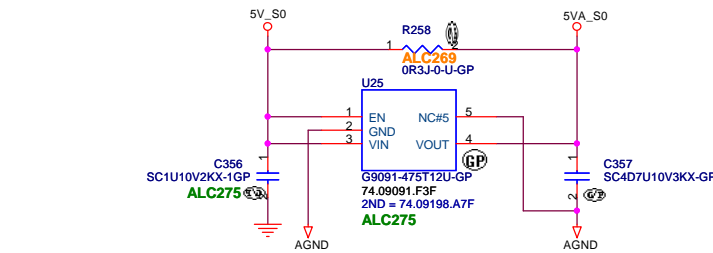


LAN Connector



DVT 1ST

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LAN CONN			
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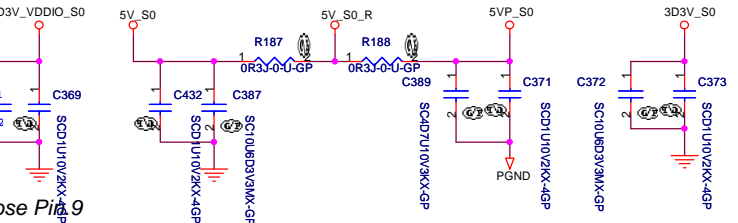


DVT 20100621
Change EC23, EC24 to mount
By EMI request

Tucana use ALC269-VB5
71.00275.A03

Close Pin.27

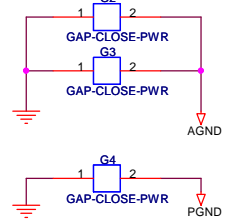
Close To CODEC



Close Pin.39 and Pin.46

Close Pin.1

1. BOTTOM CLOSE TO CODEC
2. TOP CLOSE TO BTB CONNECTOR



DVT 1ST

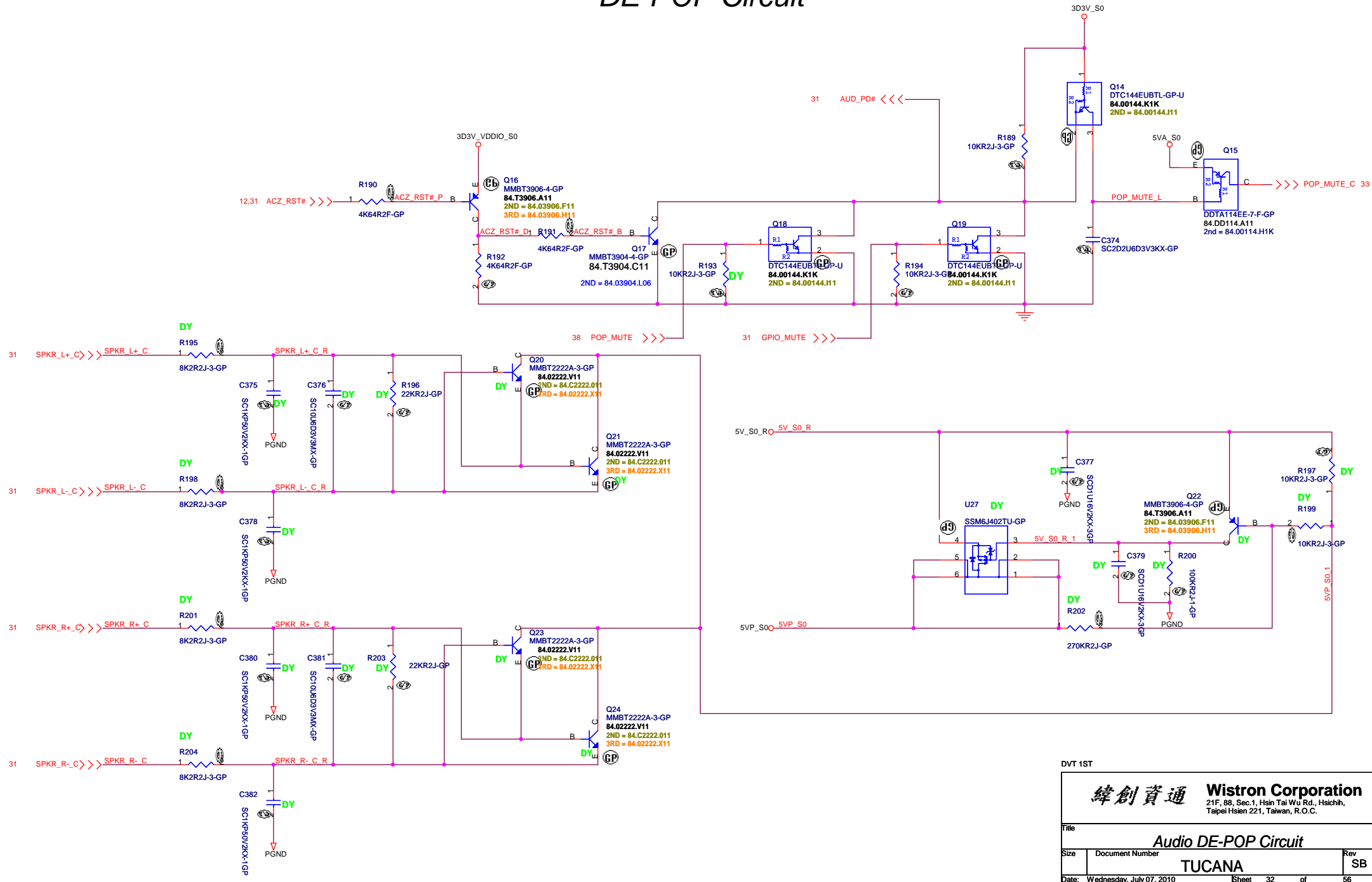
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CODEC REALTEK ALC269**

Size: Document Number: **TUCANA** Rev: **SB**

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DE-POP Circuit



DVT 1ST

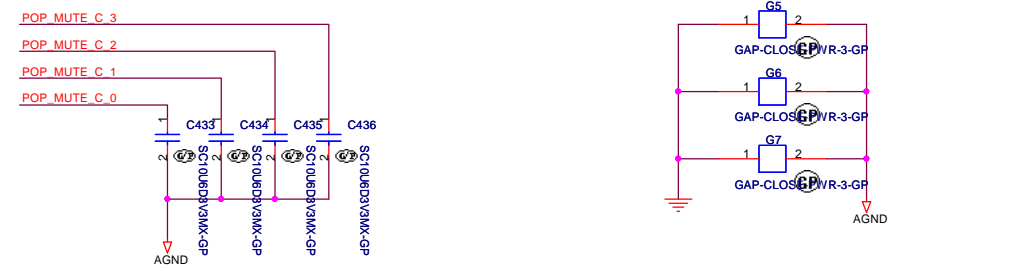
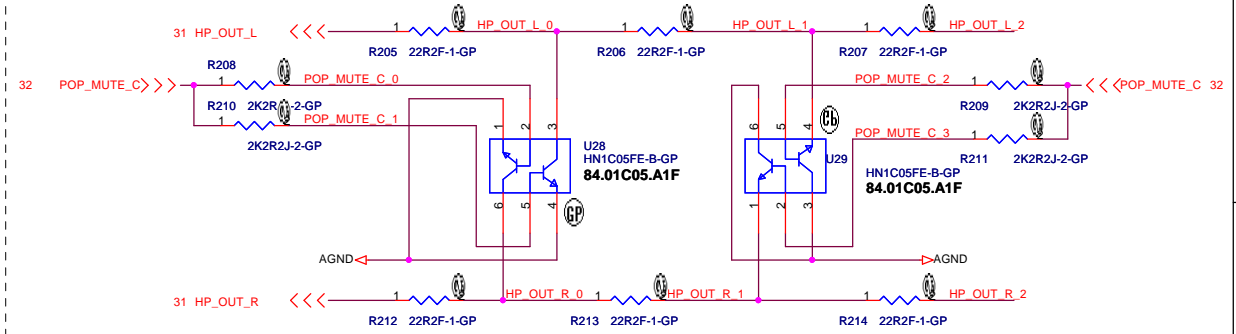
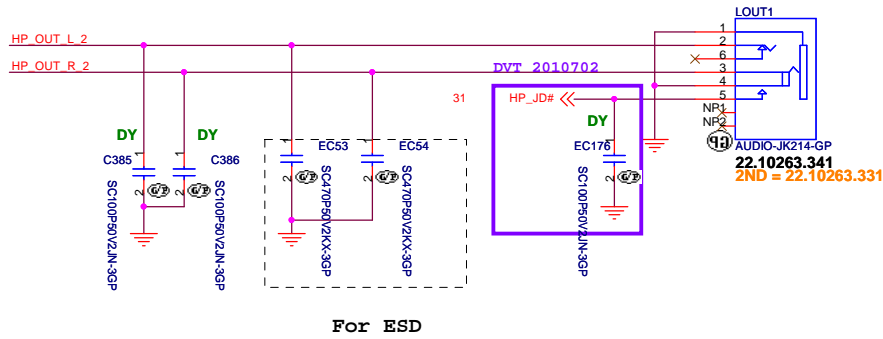
緯創資通 Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio DE-POP Circuit**

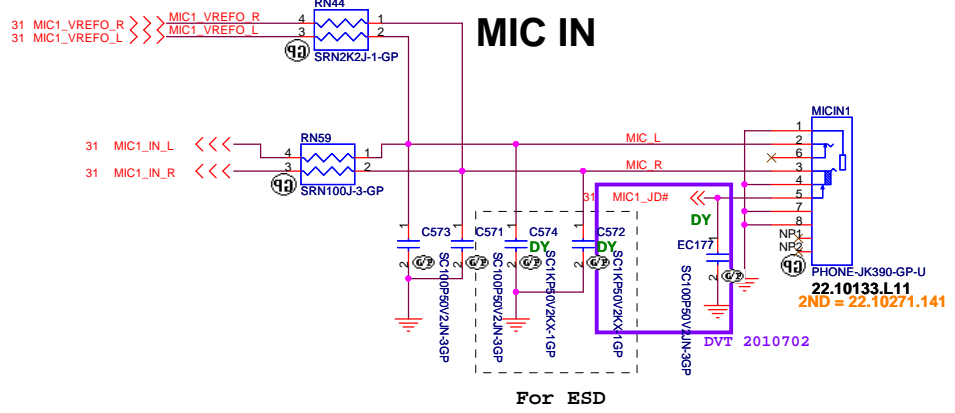
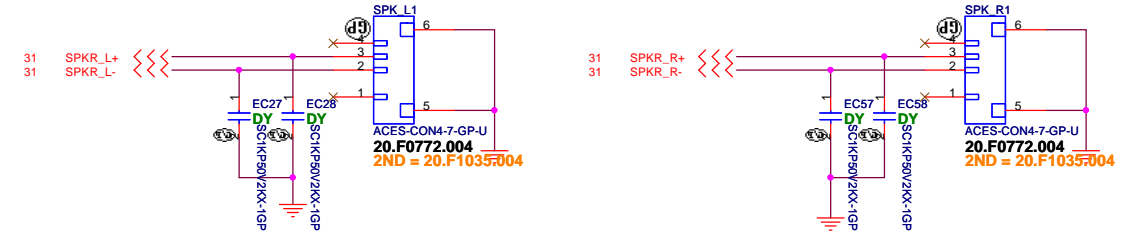
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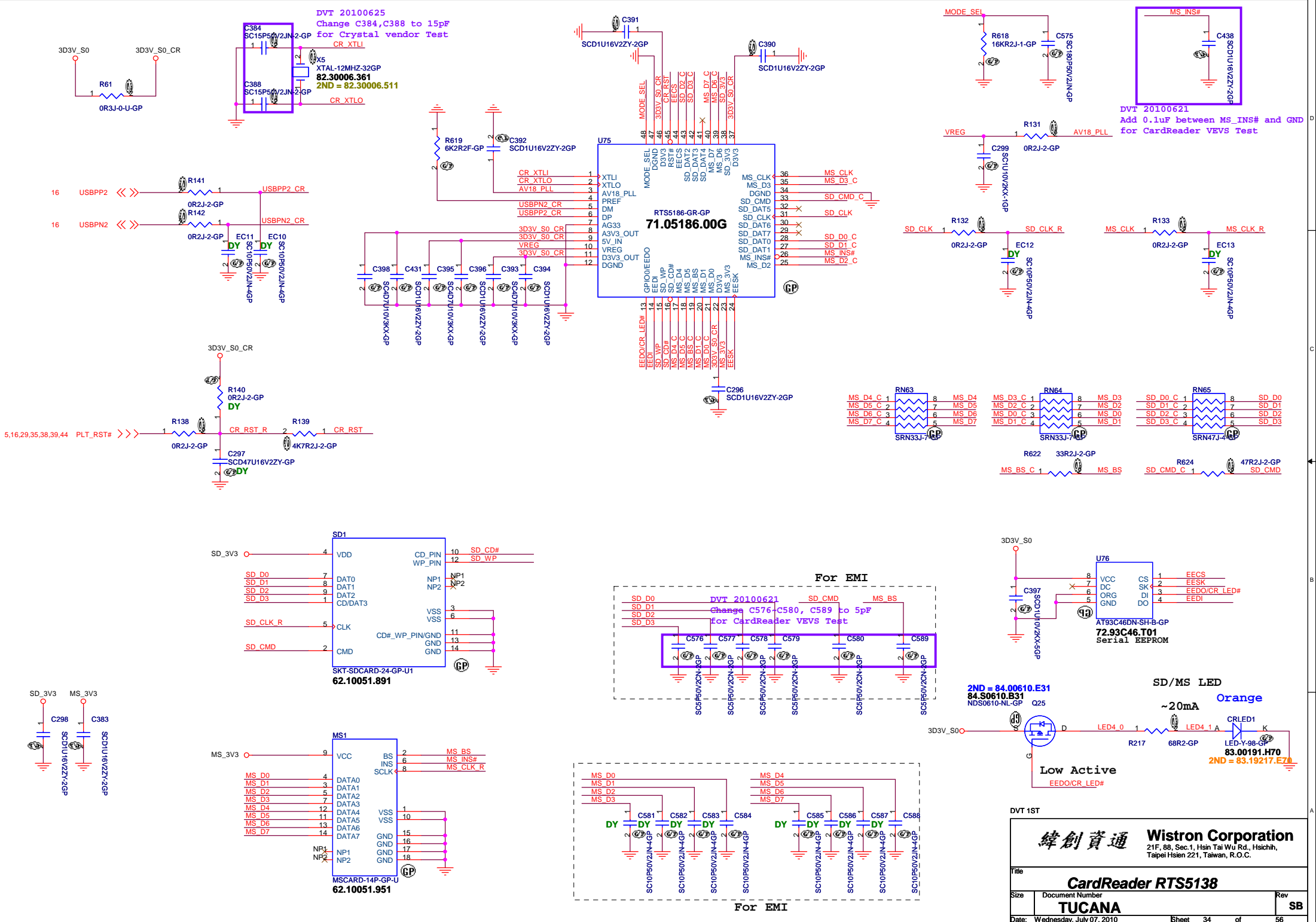
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LINE OUT



Internal Speaker CONN





緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

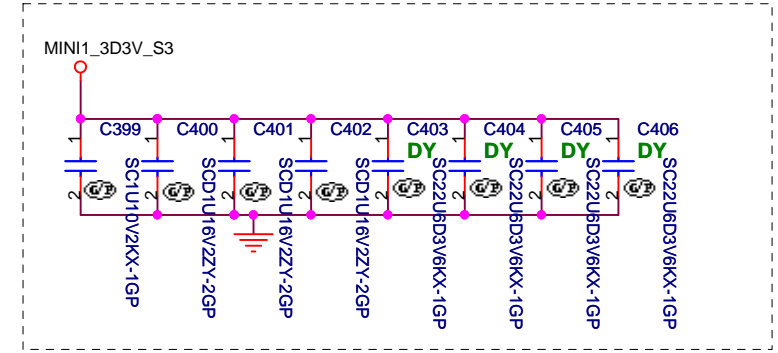
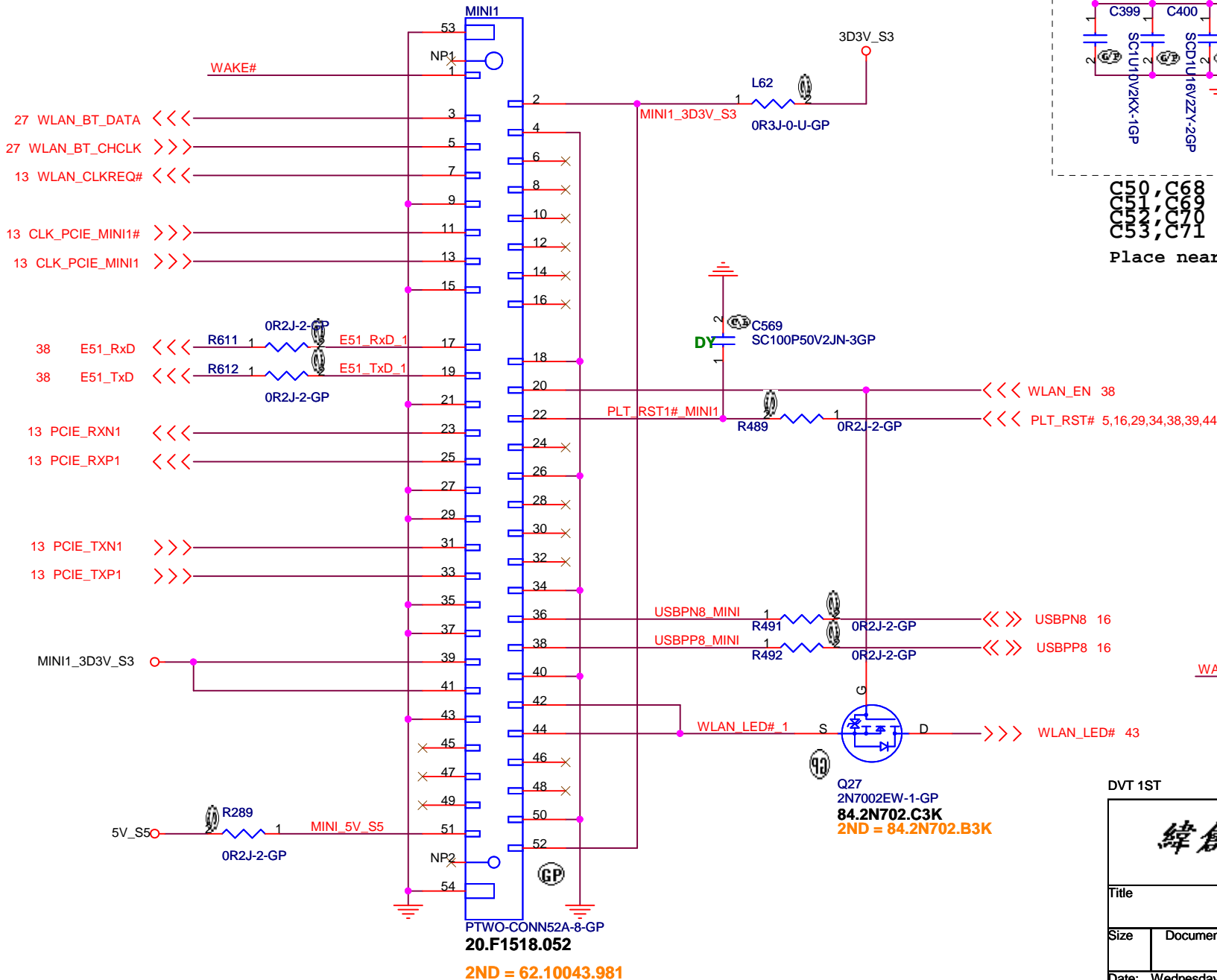
CardReader RTS5138

TUCANA

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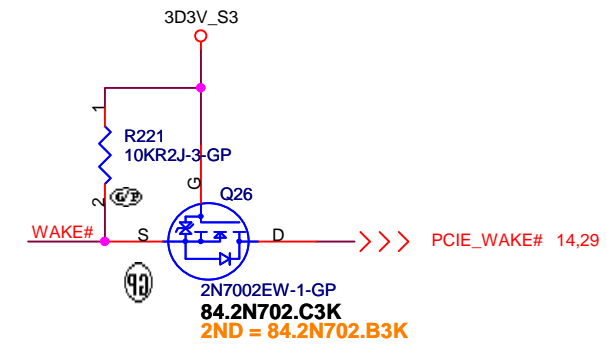
Mini Card Connector(WLAN)

WLAN_EN:
 Low: disable the radio
 High: enable the radio



C50, C68 bypass MINI1 pin2
 C51, C69 bypass MINI1 pin3
 C52, C70 bypass MINI1 pin4
 C53, C71 bypass MINI1 pin5

Place near MINI1

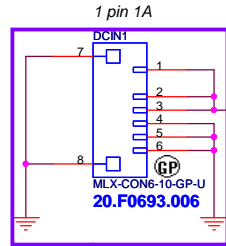


DVT 1ST

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
MINI CARD CONN			
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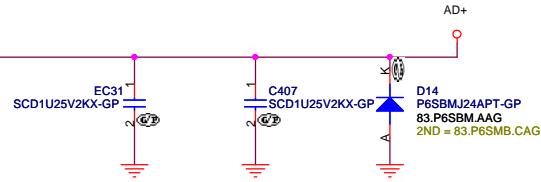
2ND = 62.10043.981

DC IN Connector

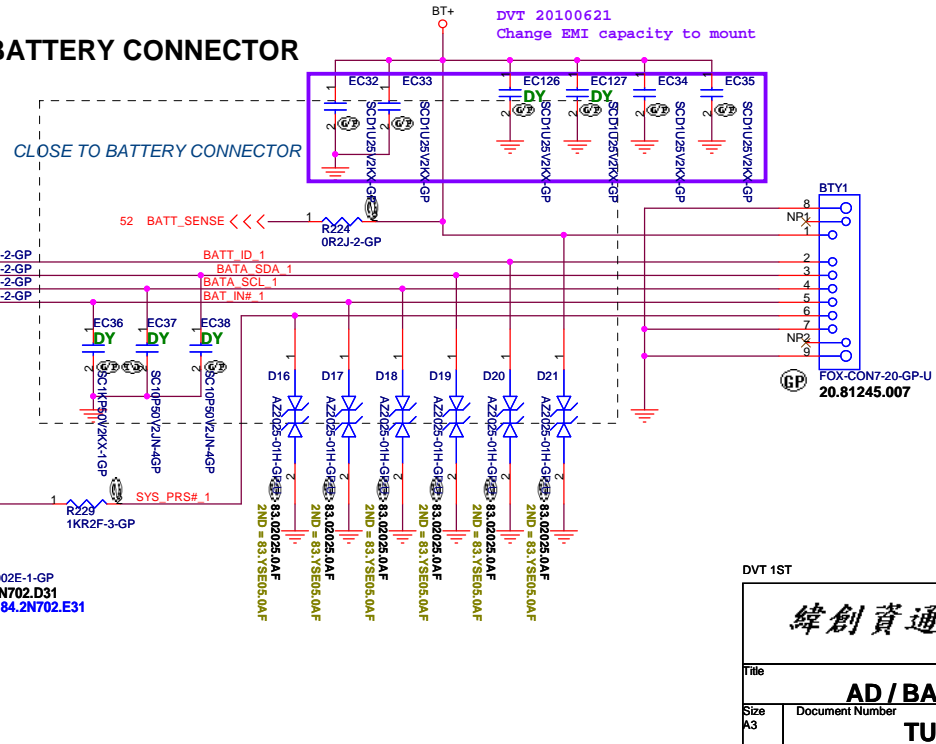


DVT 20100610
Change DCIN1 to 20.F0693.006
(follow connector list)

Adaptor in to generate DCBATOUT

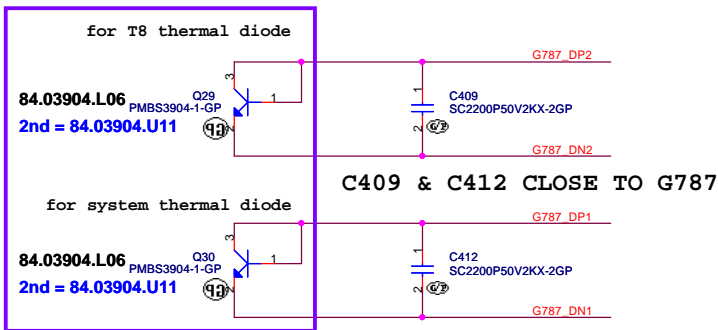


BATTERY CONNECTOR

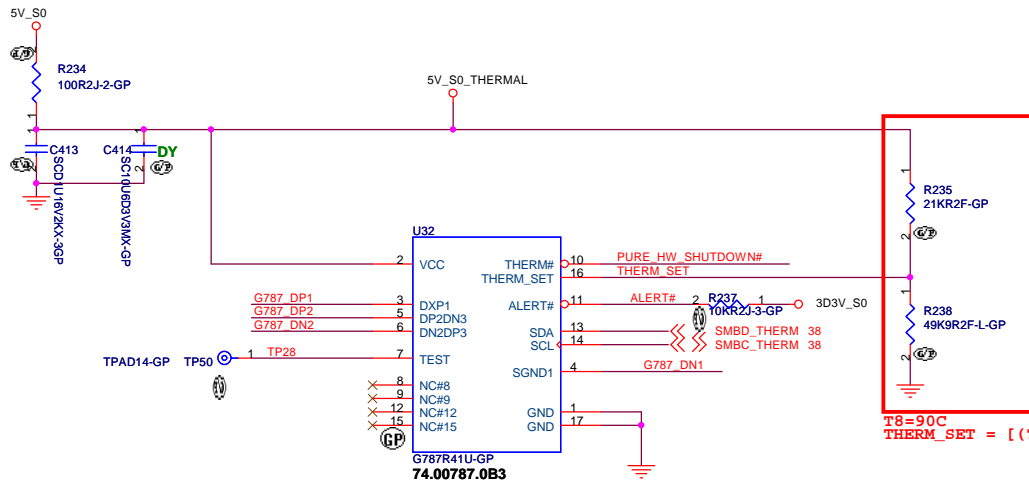
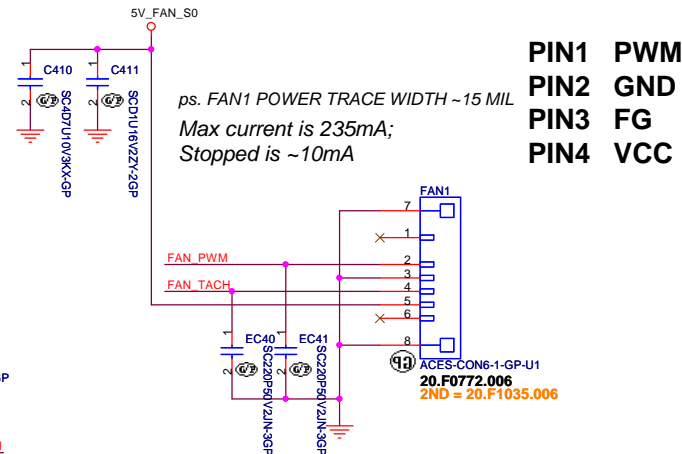
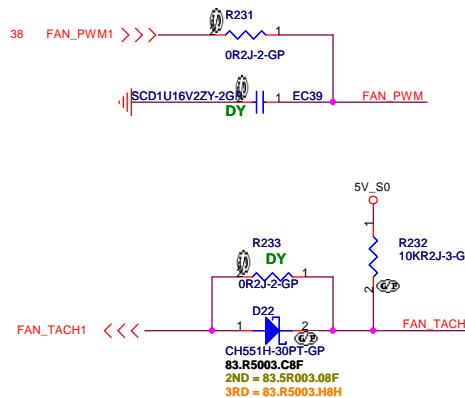


DVT 1ST

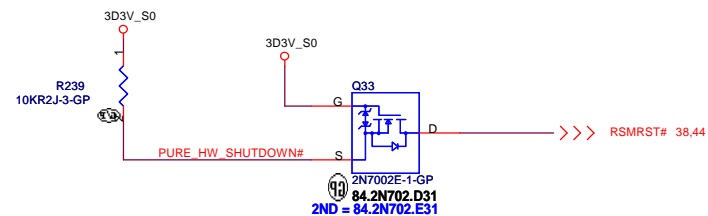
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
AD / BATT CONN	
Size A3	Document Number TUCANA
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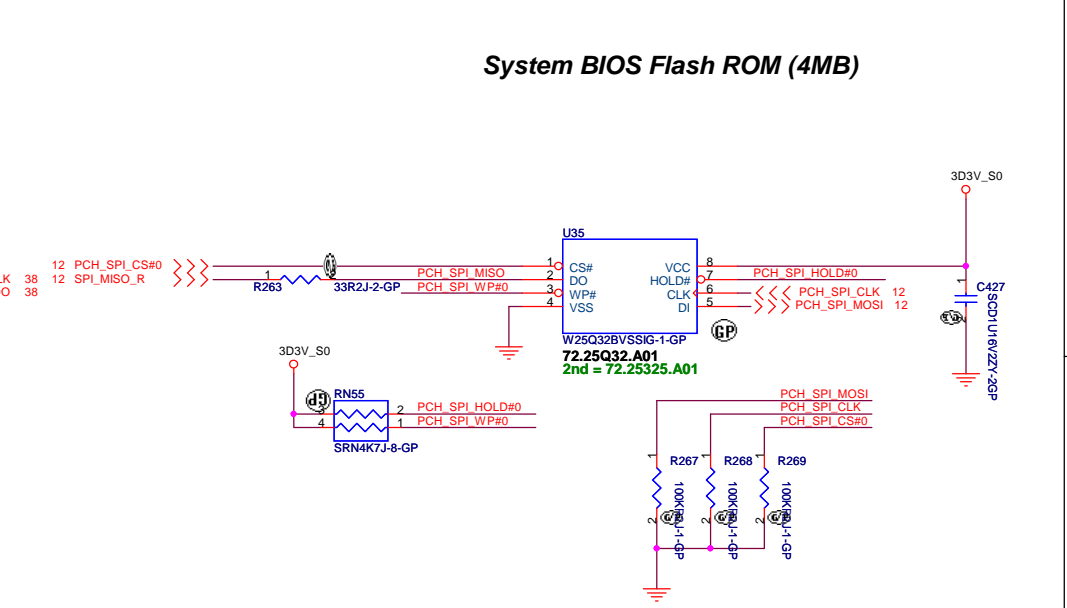
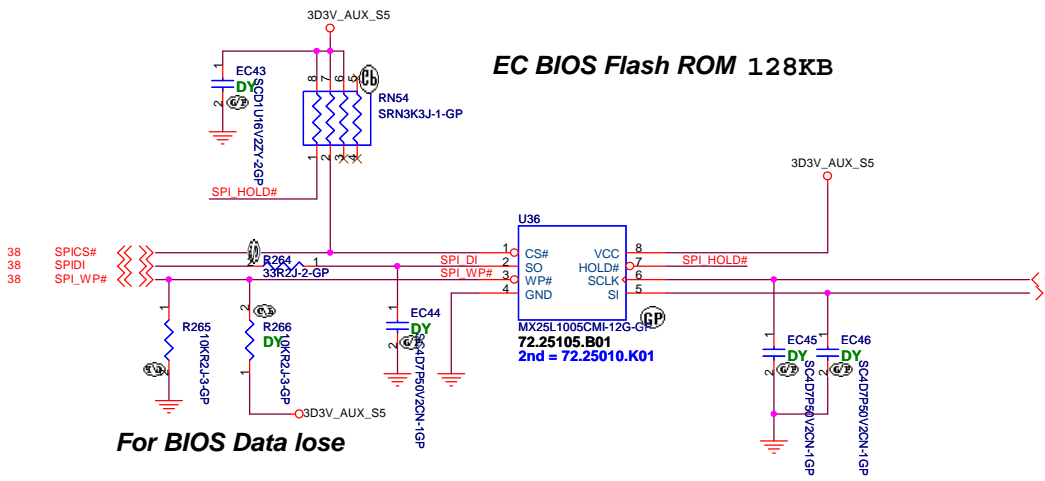
DVT 20100705
Delete Q29,Q30 main source 84.T3904.C11, follow CARAVEL-CP design



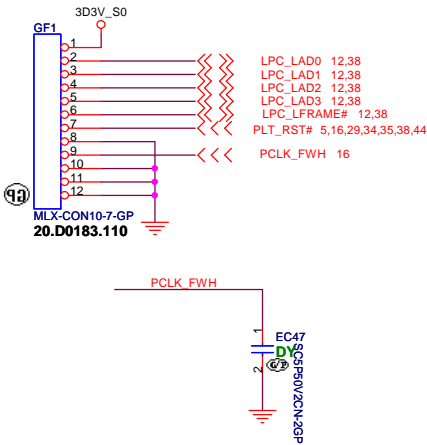
T8=90C
THERM_SET = [(Tset-72) x 0.02+0.34] x VCC



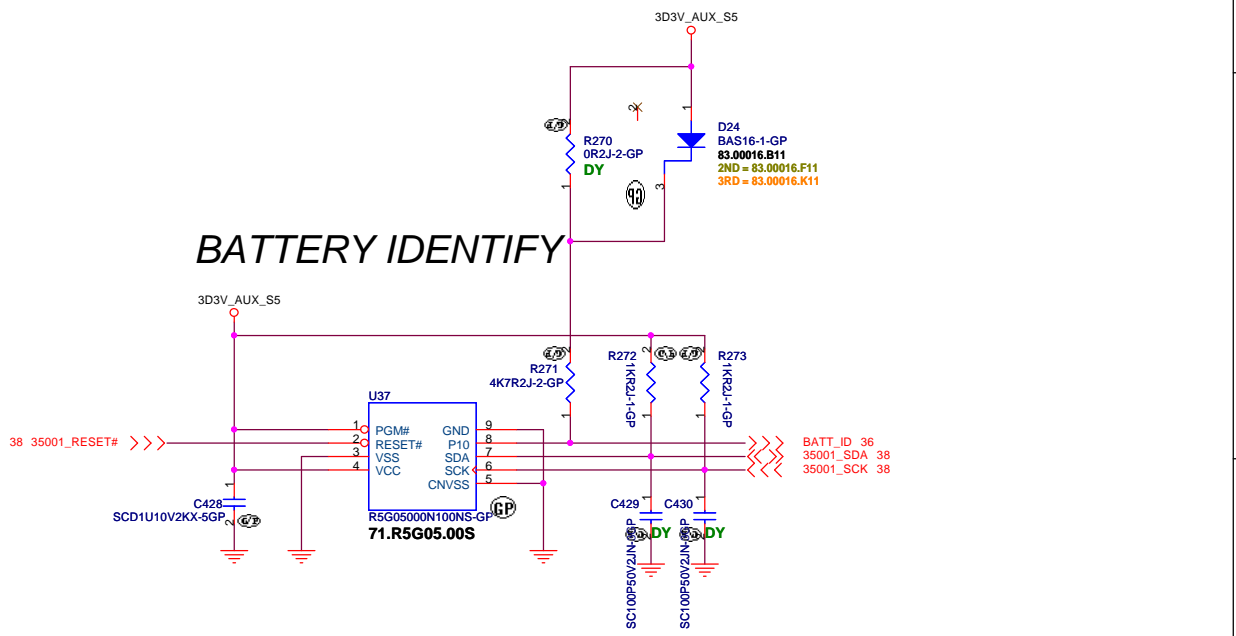
DVT 1ST

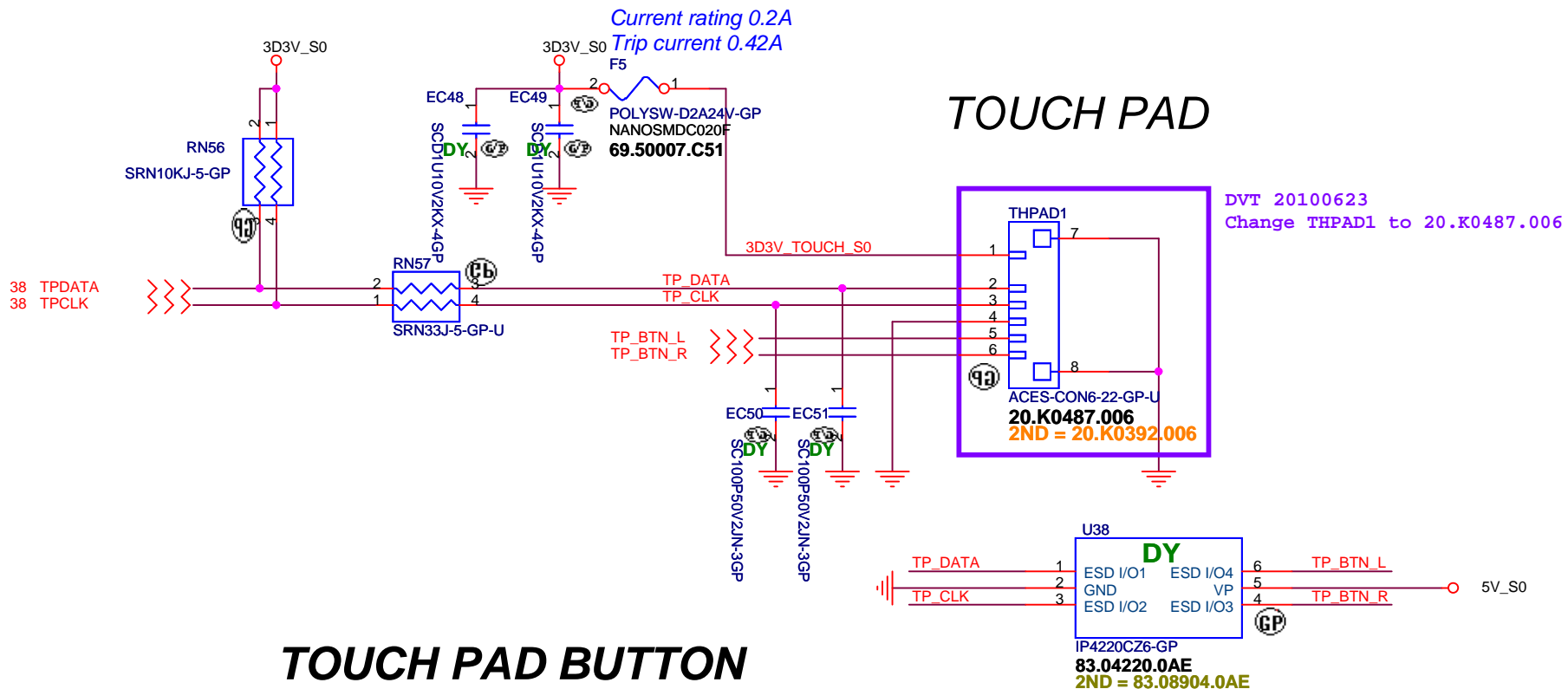


GOLDEN FINGER FOR DEBUG BOARD CONNECTOR (only install it on EVT)



BATTERY IDENTIFY



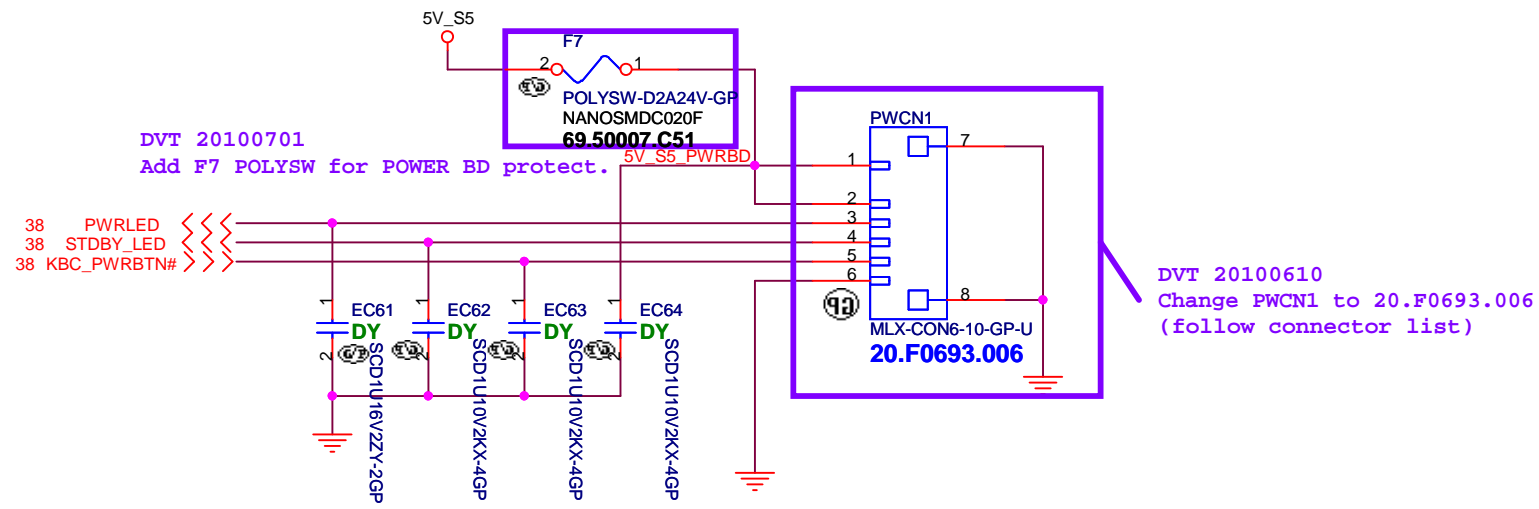


DVT 1ST

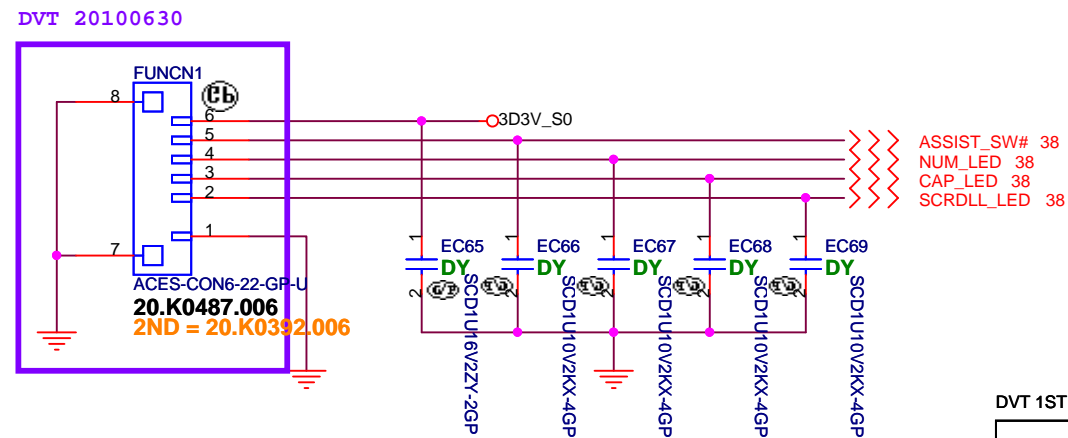
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	

Title			
TouchPad			
Size	Document Number		Rev
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POWER BUTTON BD CONN



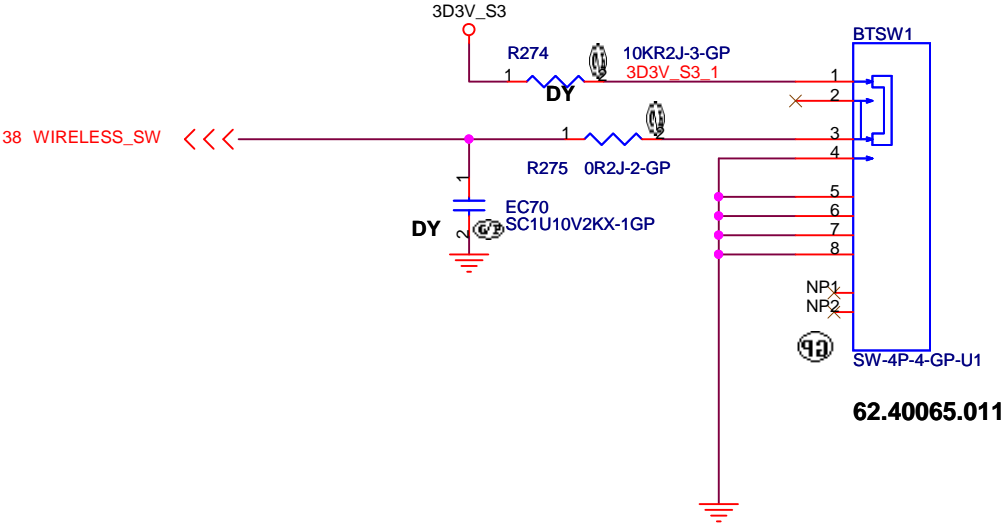
FUNCTION BD CONN



DVT 1ST

 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
FUNCTION BD & POWER BD	
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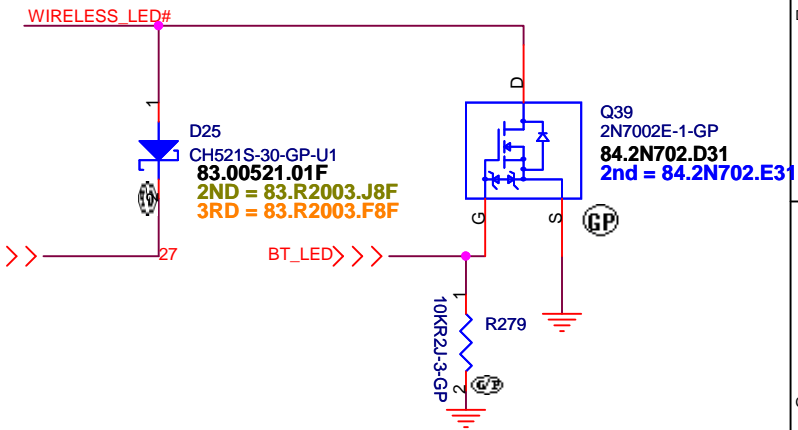
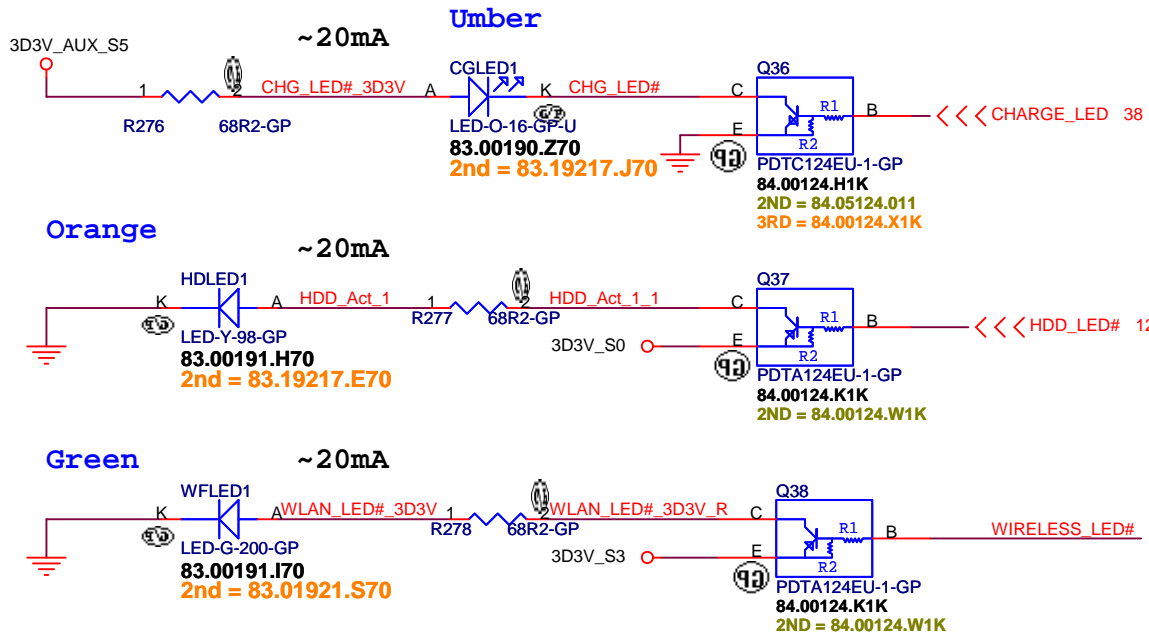
WLAN SWITCH



DVT 1ST

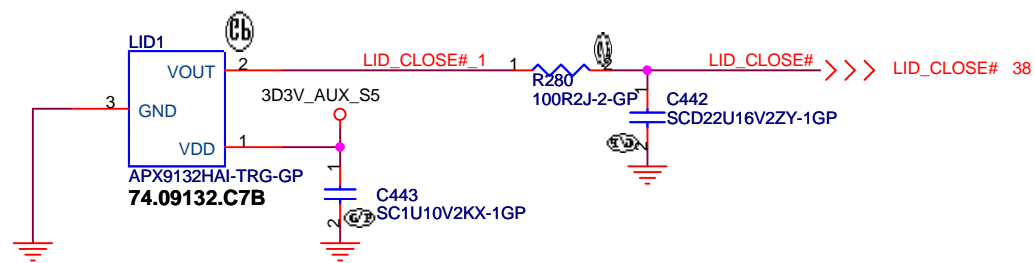
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Switch			
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LED



	active	High	Low
WWAN(W_DISABLE#)		ON	OFF
WLAN(WLAN_LED#)		OFF	ON
Bluetooth(BT_LED)		ON	OFF

Cover Up Switch



Common wireless SW(mechanical)	ON							
WLAN SW(software)	ON	OFF	ON	OFF	ON	OFF	ON	OFF
WWAN SW(software)	ON	ON	OFF	OFF	ON	ON	OFF	OFF
Bluetooth SW(software)	ON	ON	ON	ON	OFF	OFF	OFF	OFF
LED	TURN ON							OFF

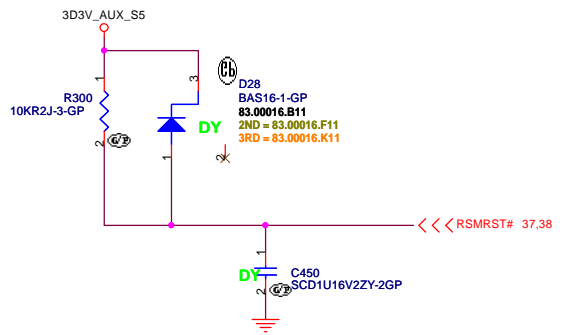
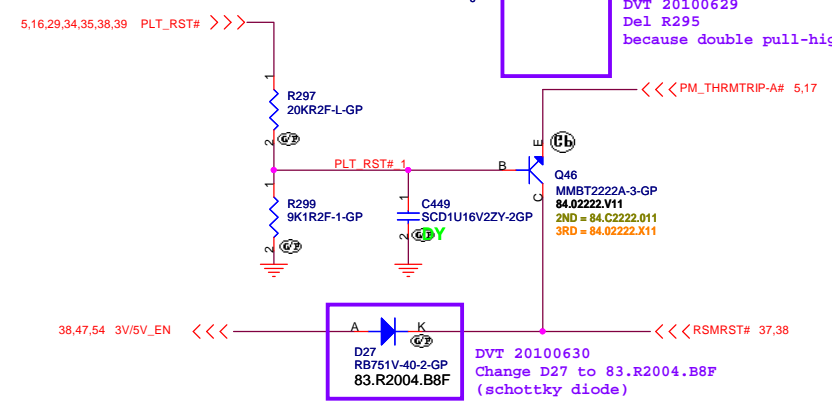
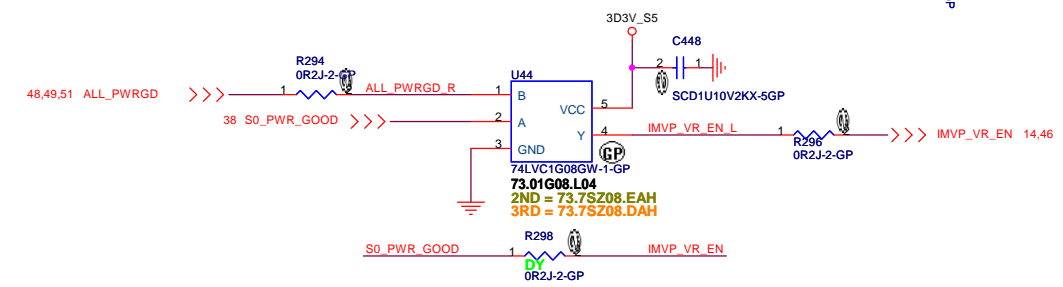
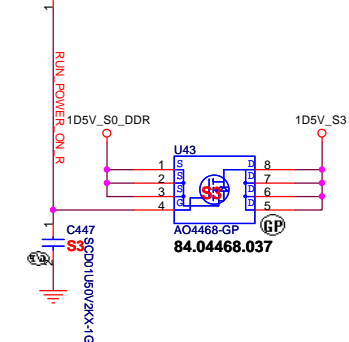
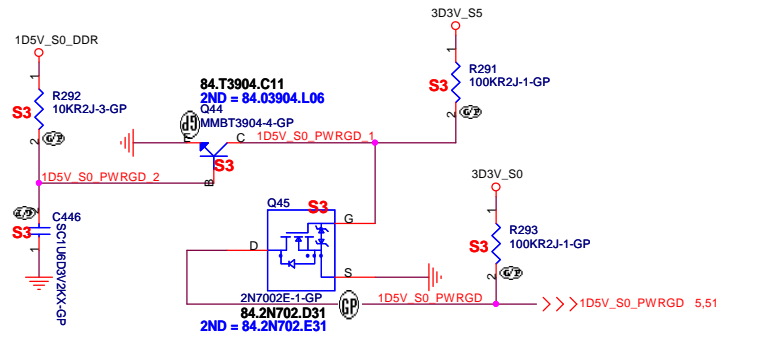
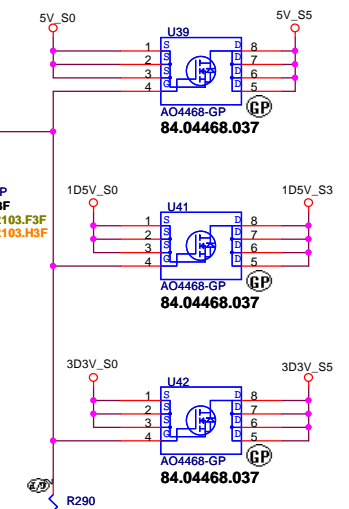
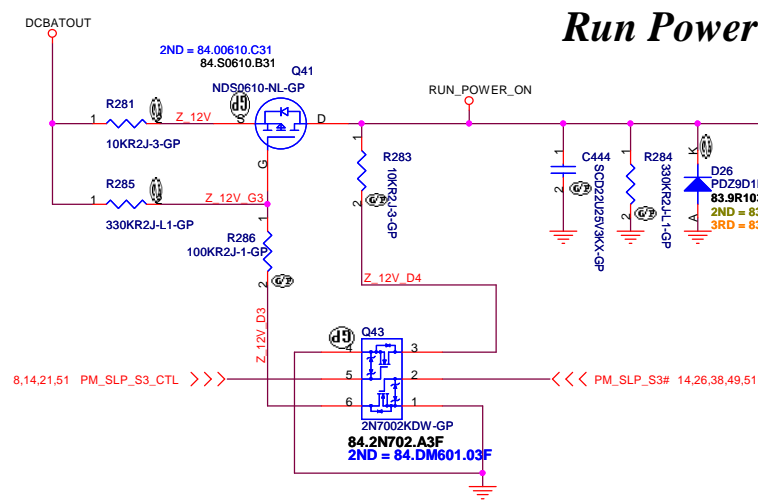
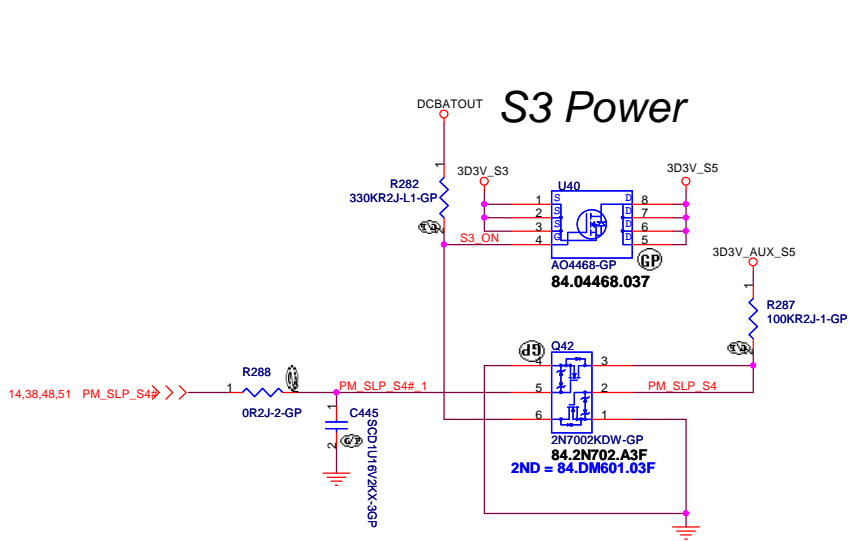
DVT 1ST

緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Lid Switch & LED**

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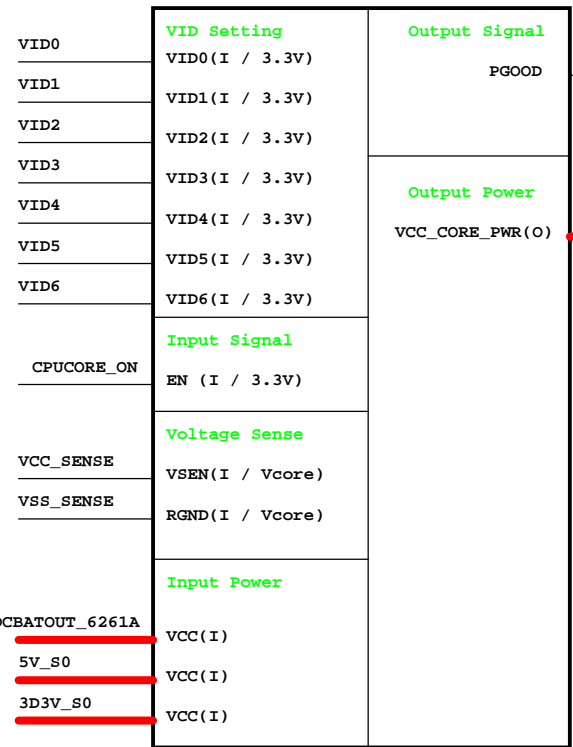
DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

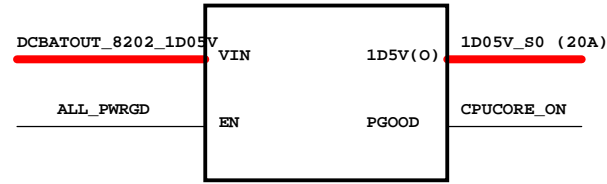
RUN POWER

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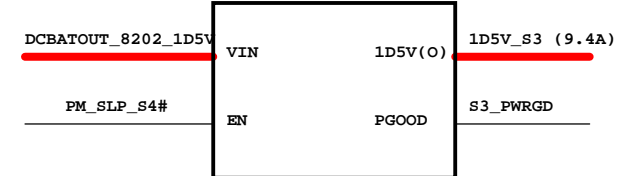
**CPU_CORE
ADP3211**



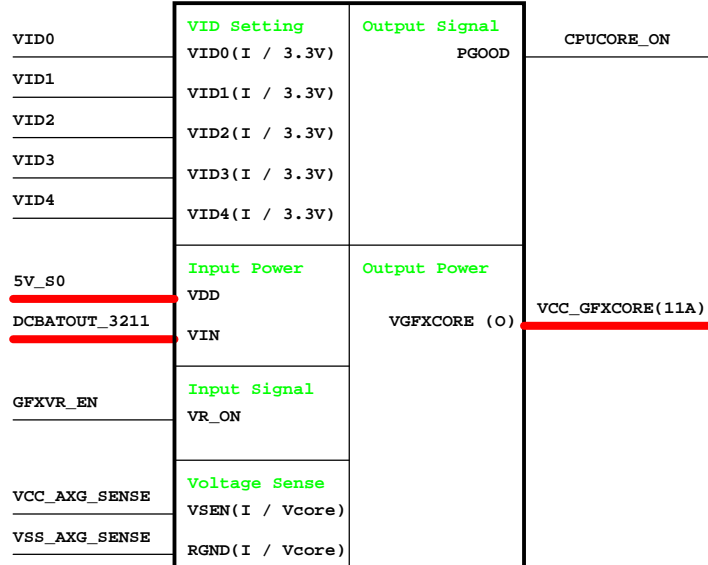
RT8209 1D05V_S0



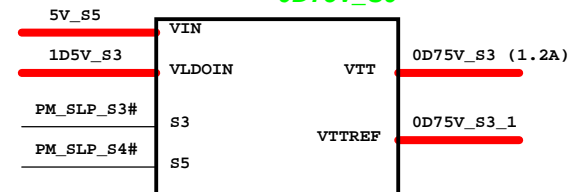
RT8209 1D5V_S3



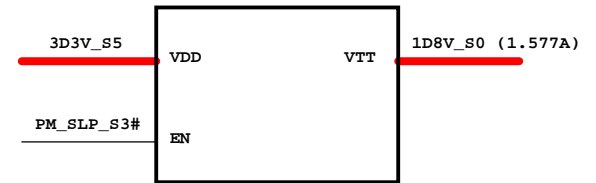
**GFX_CORE/ VGA_CORE
ADP3211**



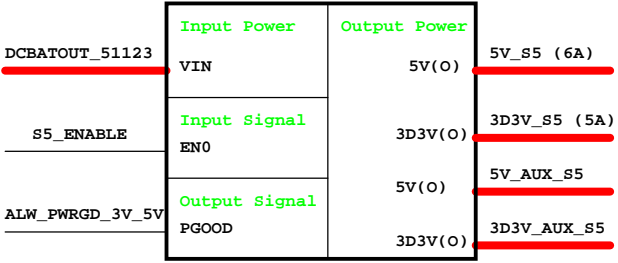
RT9026 0D75V_S0



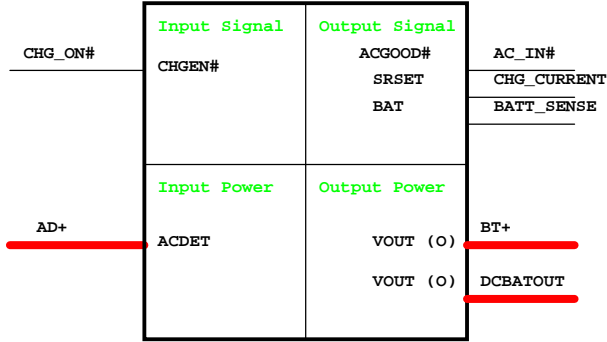
RT8015 1D8V_S0



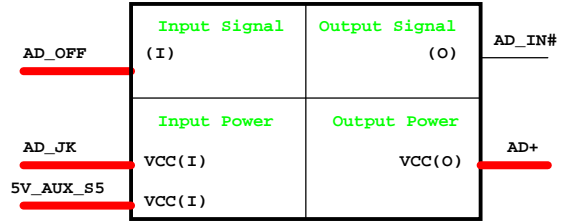
**5V/3D3V
RT8223**



Charger BQ24751

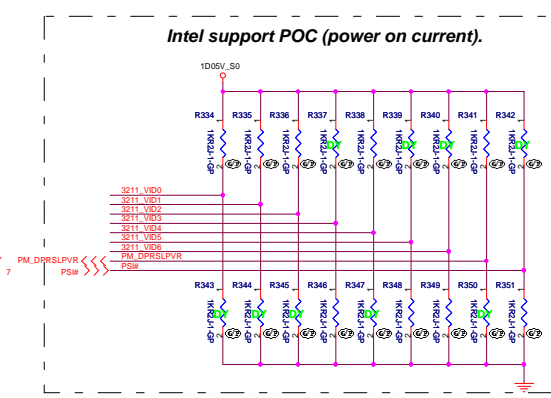
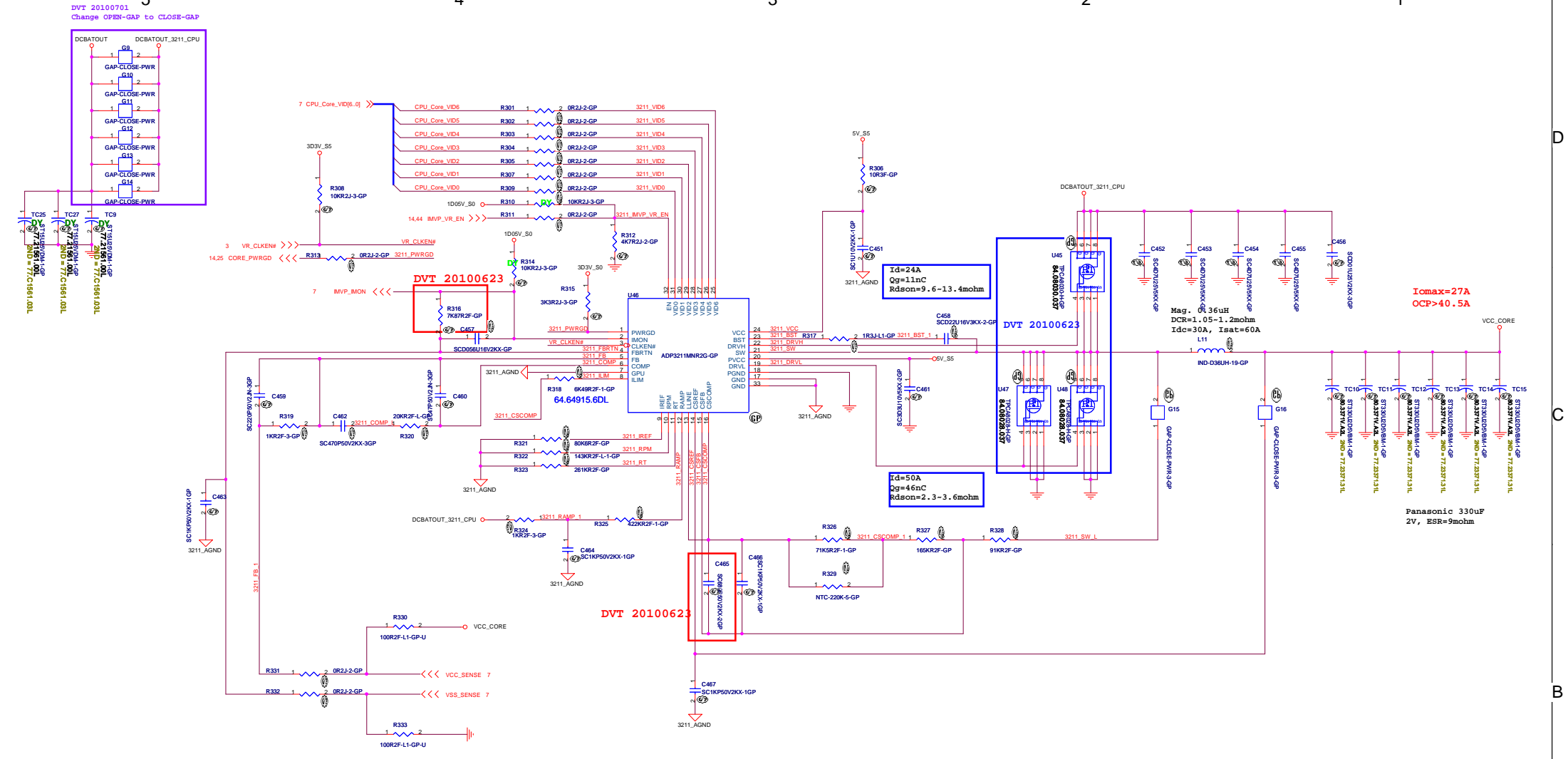


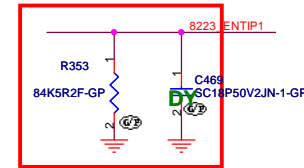
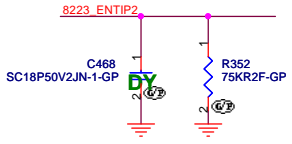
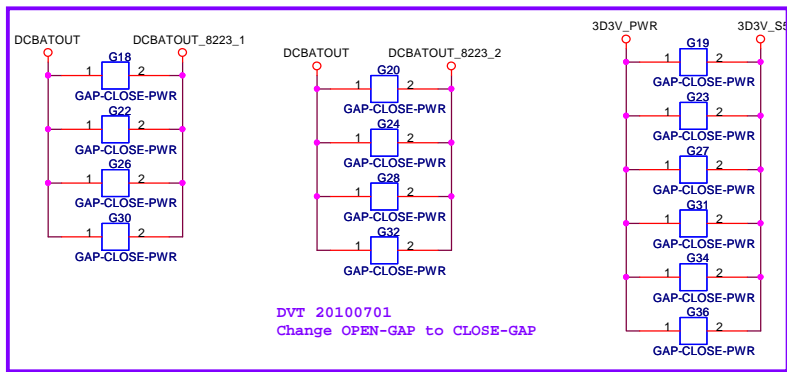
Adapter



DVT 1ST

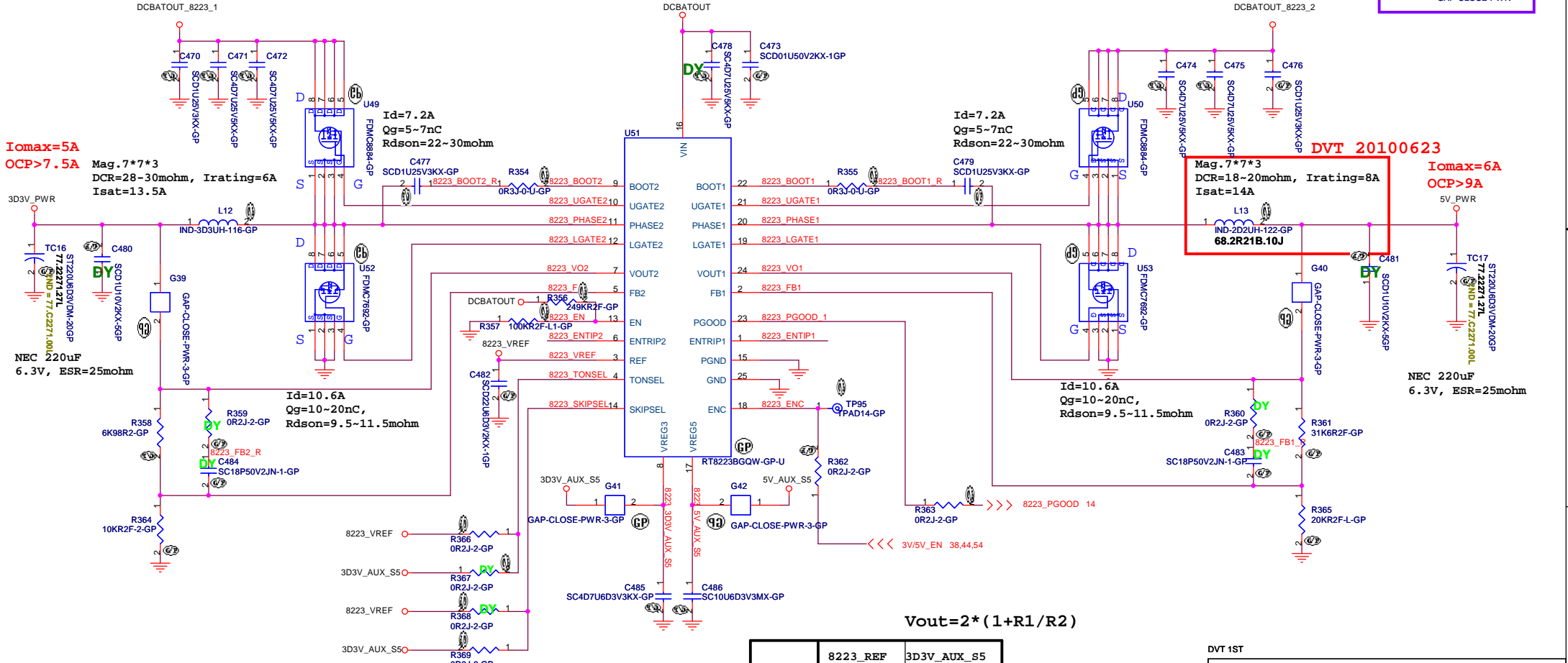
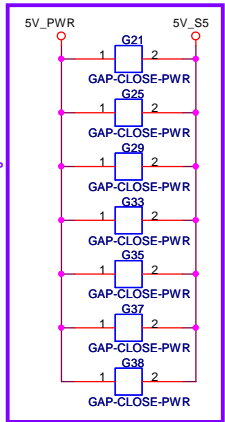
緯創資通		Wistron Corporation	
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Power Sequence Logic			
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DVT 20100623

DVT 20100701
Change OPEN-GAP
to CLOSE-GAP



	8223_REF	3D3V_AUX_S5
SKIPSEL	PWM	00A AUTOSKIP
TONSEL	245k/CH1 305k/CH2	300k/CH1 375k/CH2

DVT 1ST

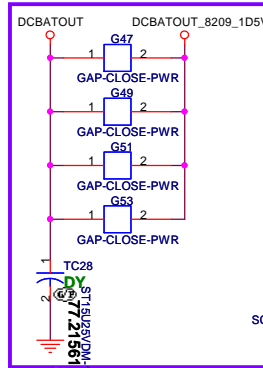
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8223 5V/3D3V**

Size: Document Number: **TUCANA** Rev: **SA**

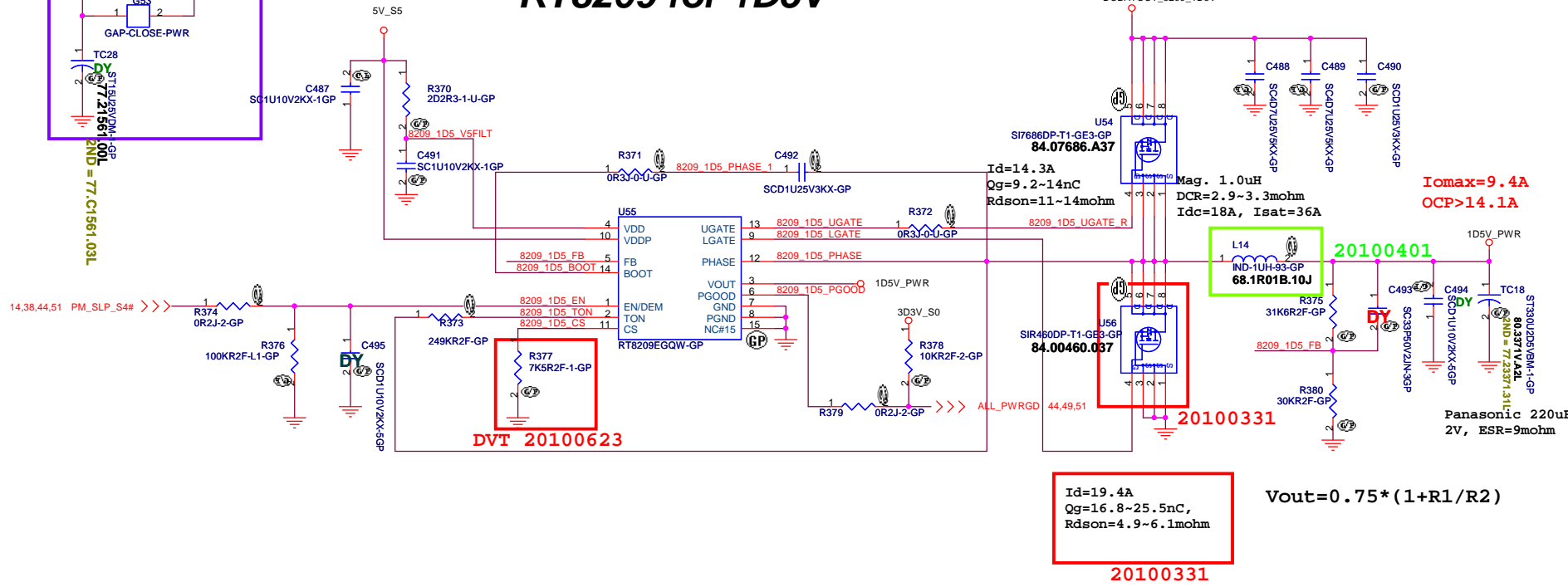
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DVT 20100701
Change OPEN-GAP to
CLOSE-GAP



ST1E1295W1-1-GP
80.371V.A4L
RND = 77. C1561.03L

RT8209 for 1D5V



DVT 20100623

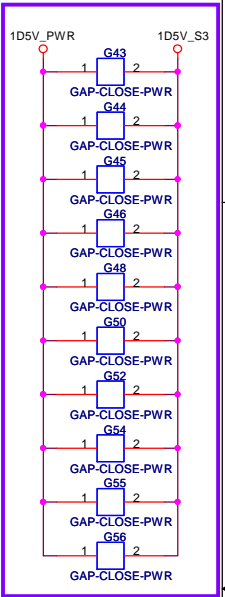
Id=19.4A
Qg=16.8~25.5nC,
Rdson=4.9~6.1mohm

20100331

Iomax=9.4A
OCP>14.1A

$$V_{out} = 0.75 * (1 + R1/R2)$$

DVT 20100701
Change OPEN-GAP to
CLOSE-GAP



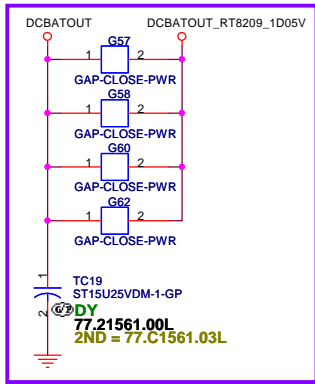
DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RT8209 1D5V**

Size: Document Number: **TUCANA** Rev: **SB**

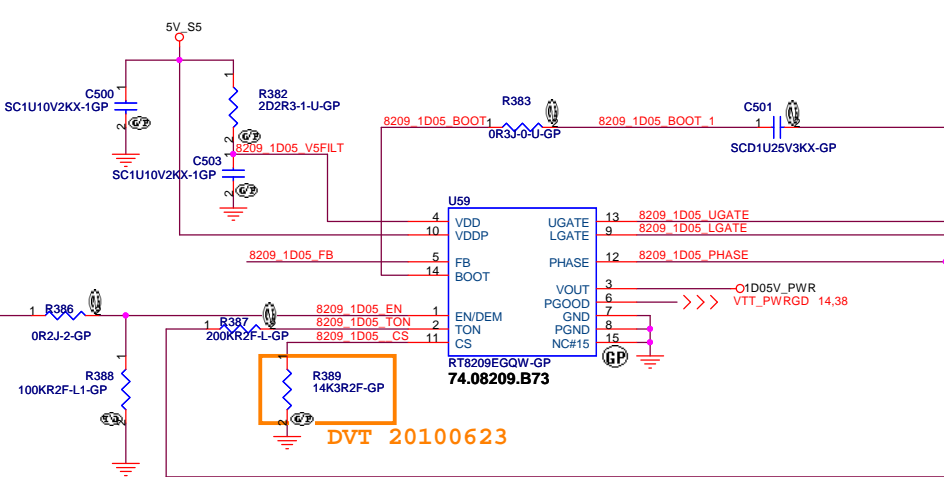
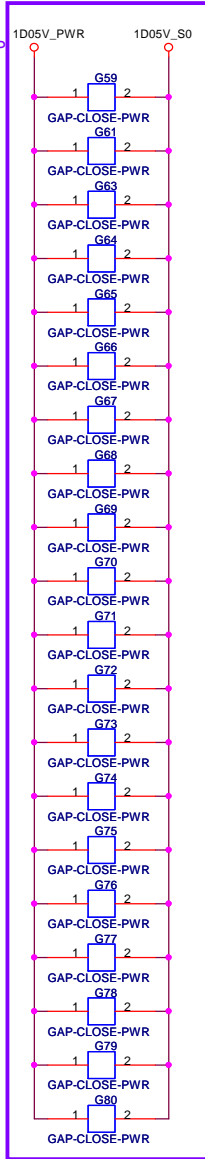
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DVT 20100701
Change OPEN-GAP to
CLOSE-GAP

RT8209 1D05V

DVT 20100701
Change OPEN-GAP to
CLOSE-GAP



Id=24A
Qg=11nC
Rdson=9.4~13.5mohm

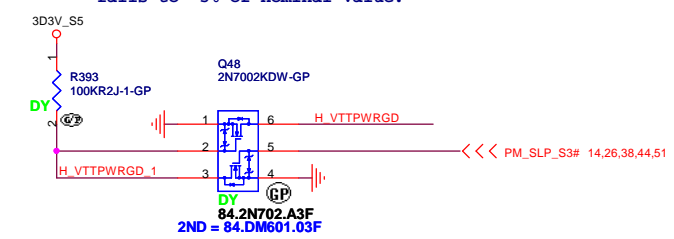
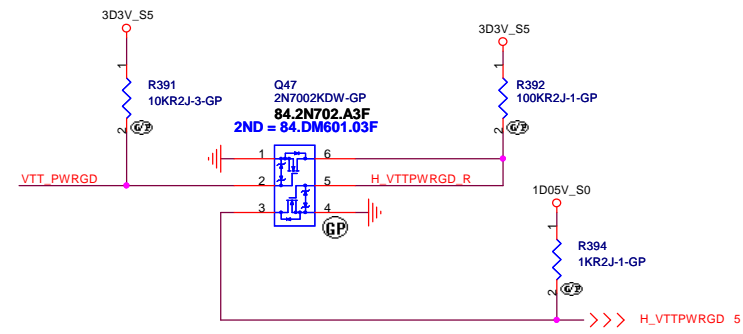
DVT 20100623
Mag. 0.56uH
DCR=1.6~1.8mohm
Idc=25A, Isat=40A

Iomax=20A
OCP>30A

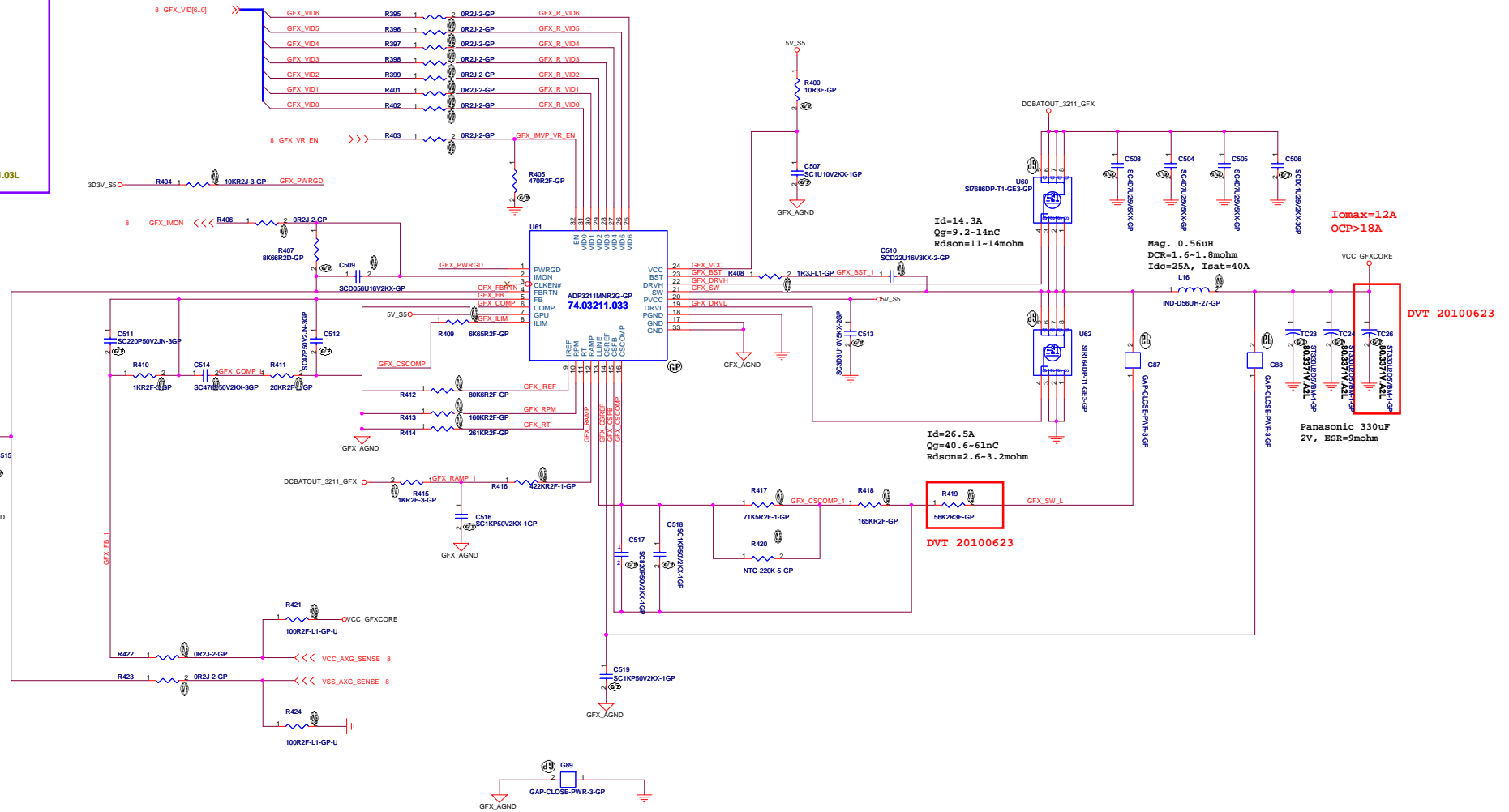
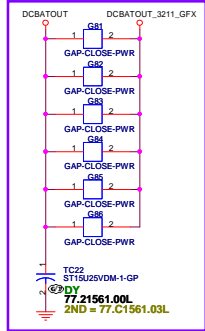
Id=50A
Qg=46nC,
Rdson=2.3~3.6mohm

$$V_{out} = 0.75 * (1 + R1/R2)$$

The processor needs to be warned about the VTT rails shutdown at least 100 ns before the VTT rail falls to -5% of nominal value.



DVT 20100701
 Charge OPEN-GAP to
 CLOSE-GAP

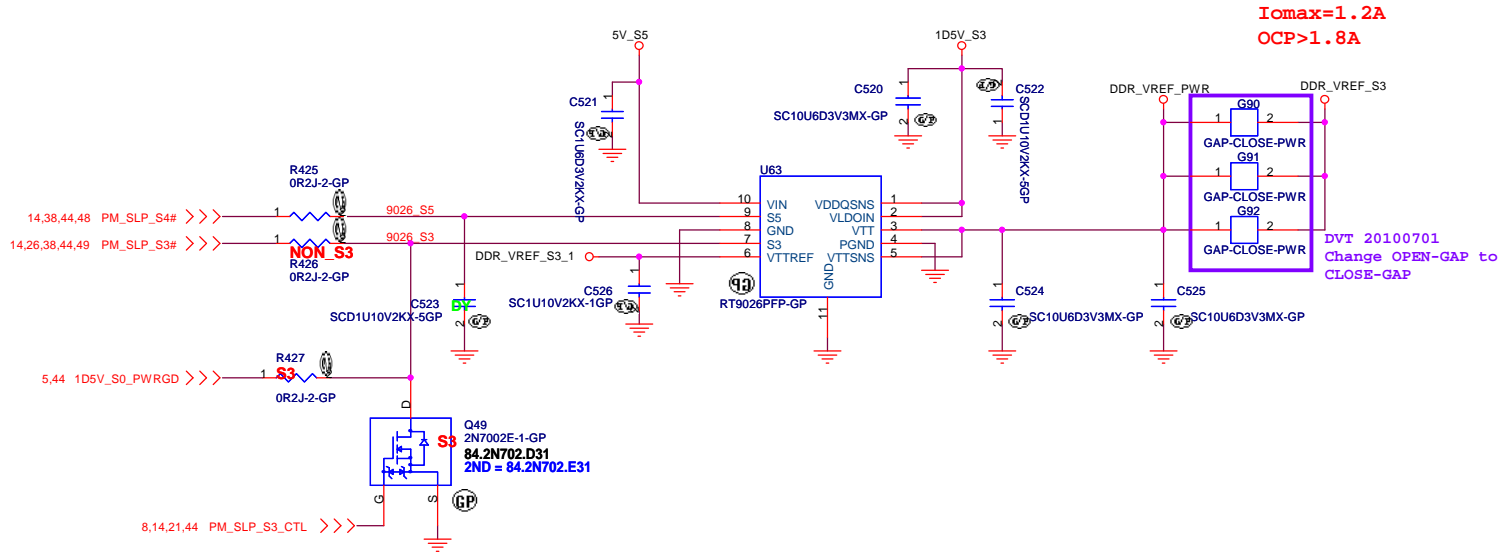


I_{omax}=12A
 OCP>18A

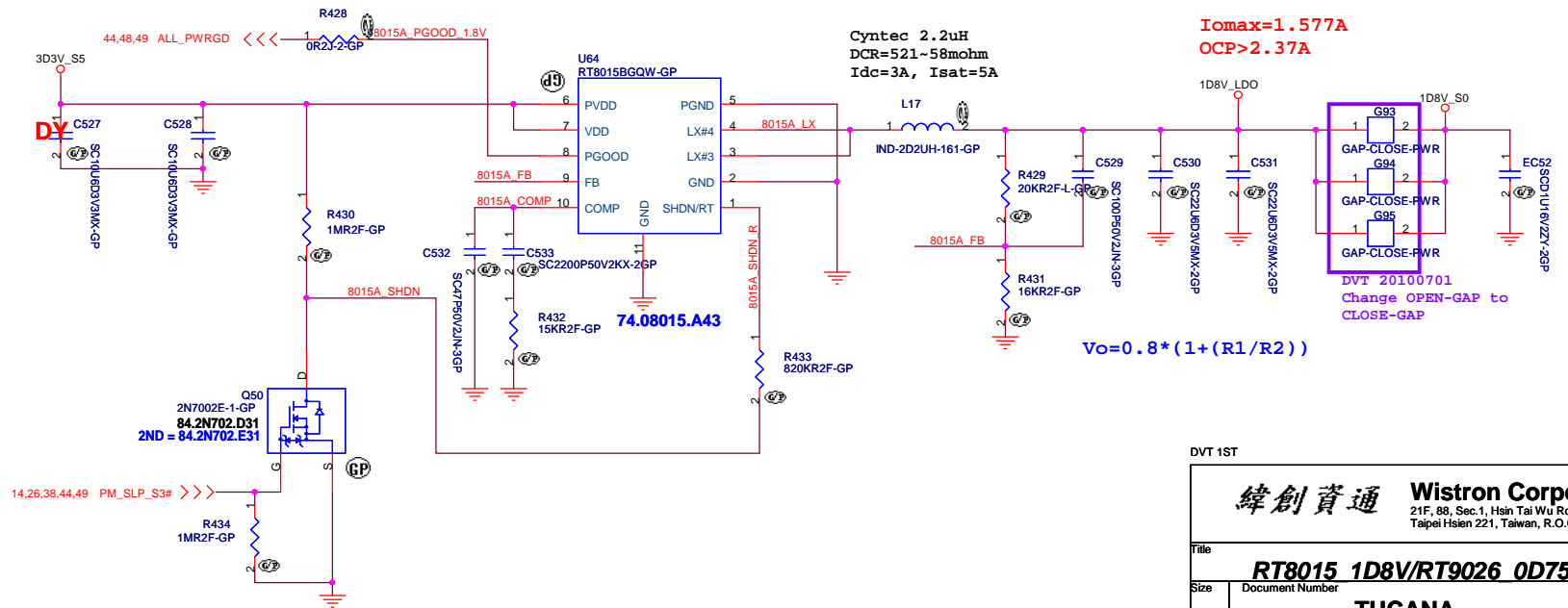
DVT 20100623

DVT 20100623

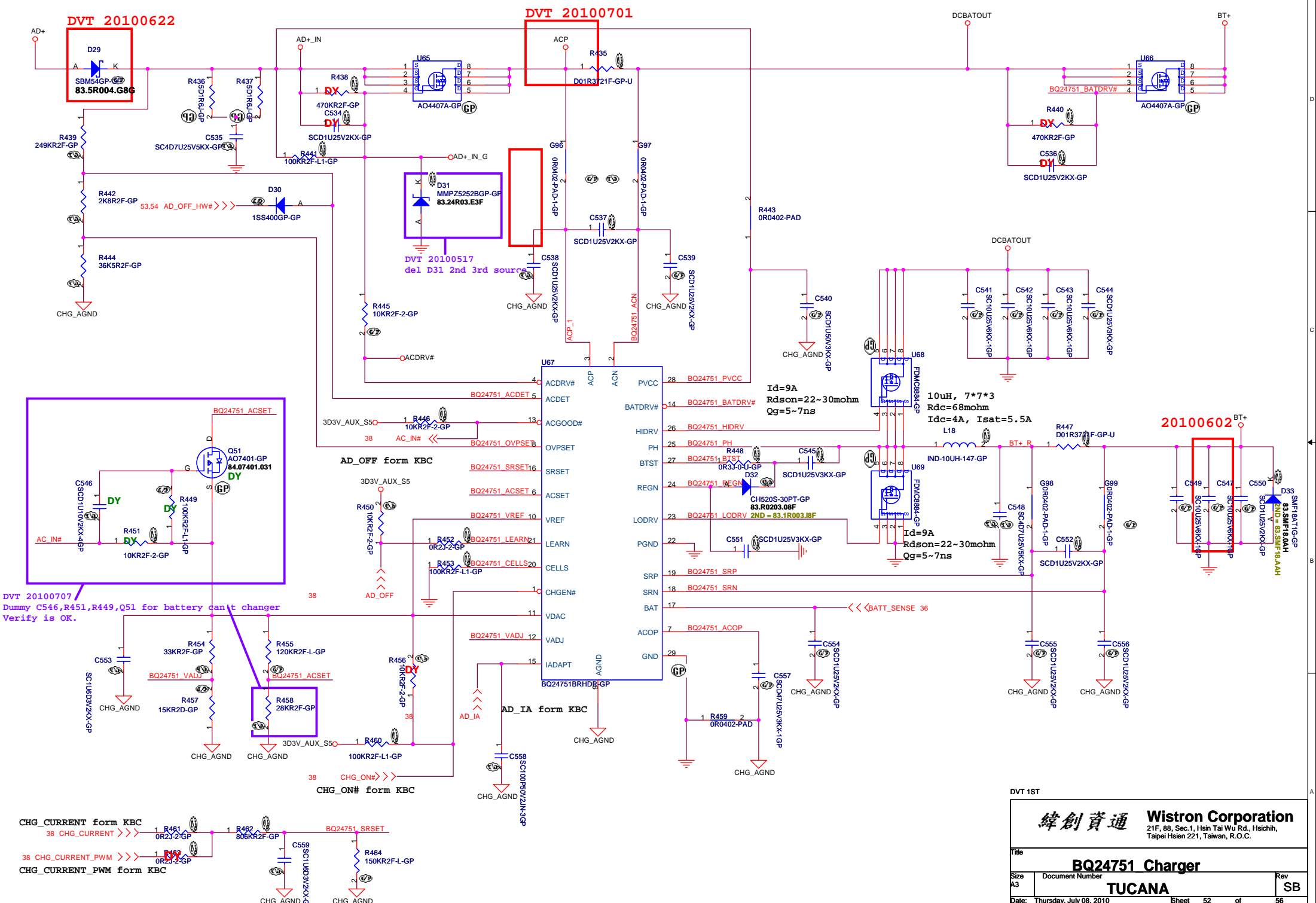
RT9026 for 0D75V_S3



RT8015 for 1D8V_S0



DVT 1ST



DVT 20100707
 Dummy C546, R451, R449, Q51 for battery can't charger
 Verify is OK.

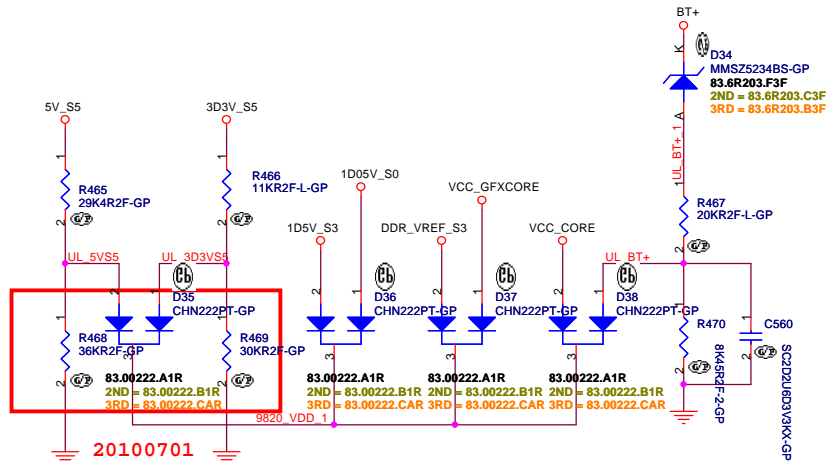
Id=9A
 Rds(on)=22~30mohm
 Qg=5~7ns
 10uH, 7*7*3
 Rdc=68mohm
 Idc=4A, Isat=5.5A

DVT 1ST

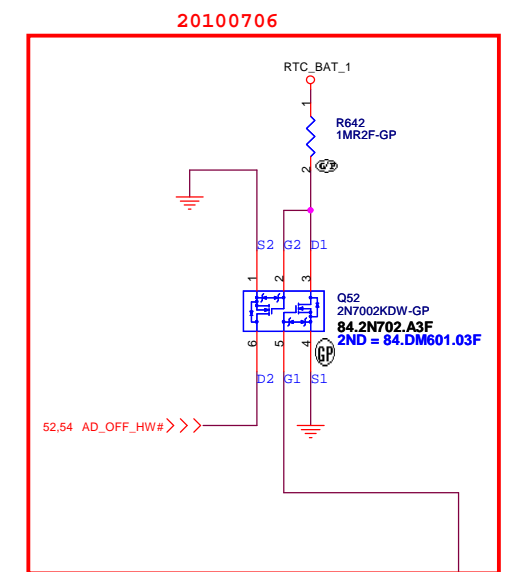
緯創資通 Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **BQ24751 Charger**

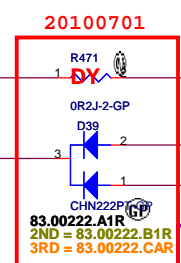
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20100701

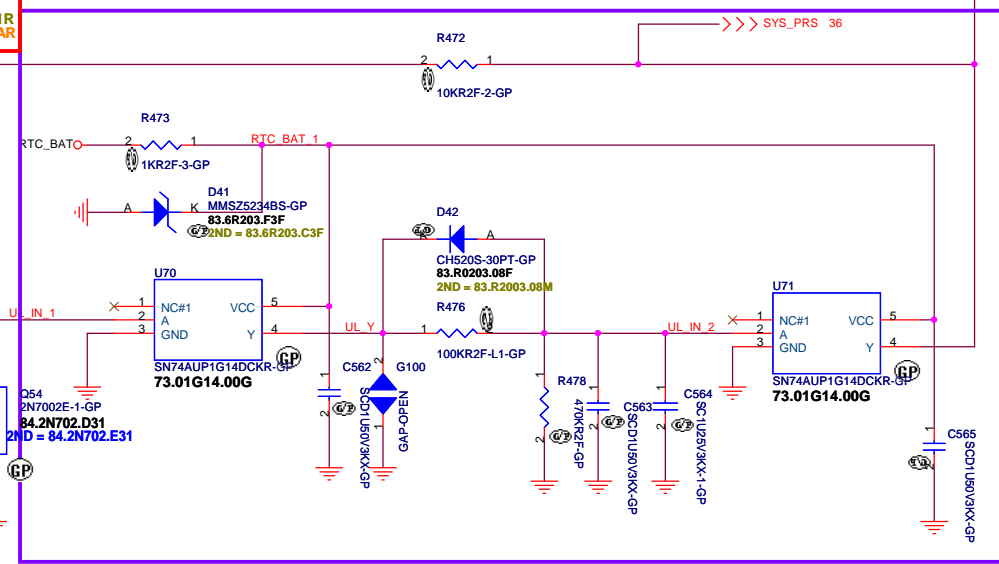
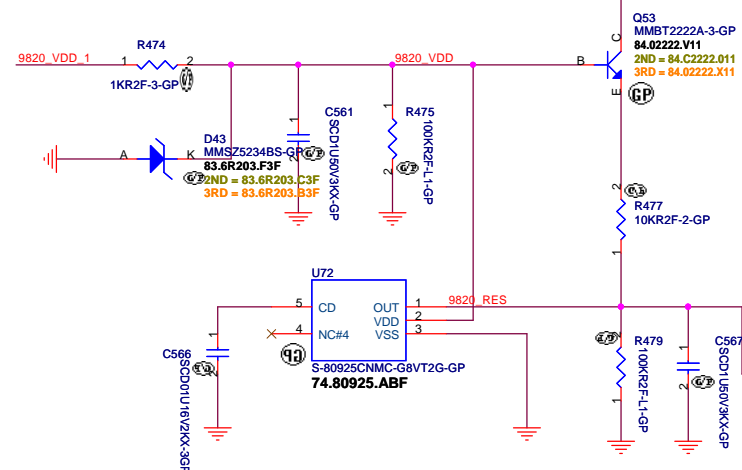


20100706



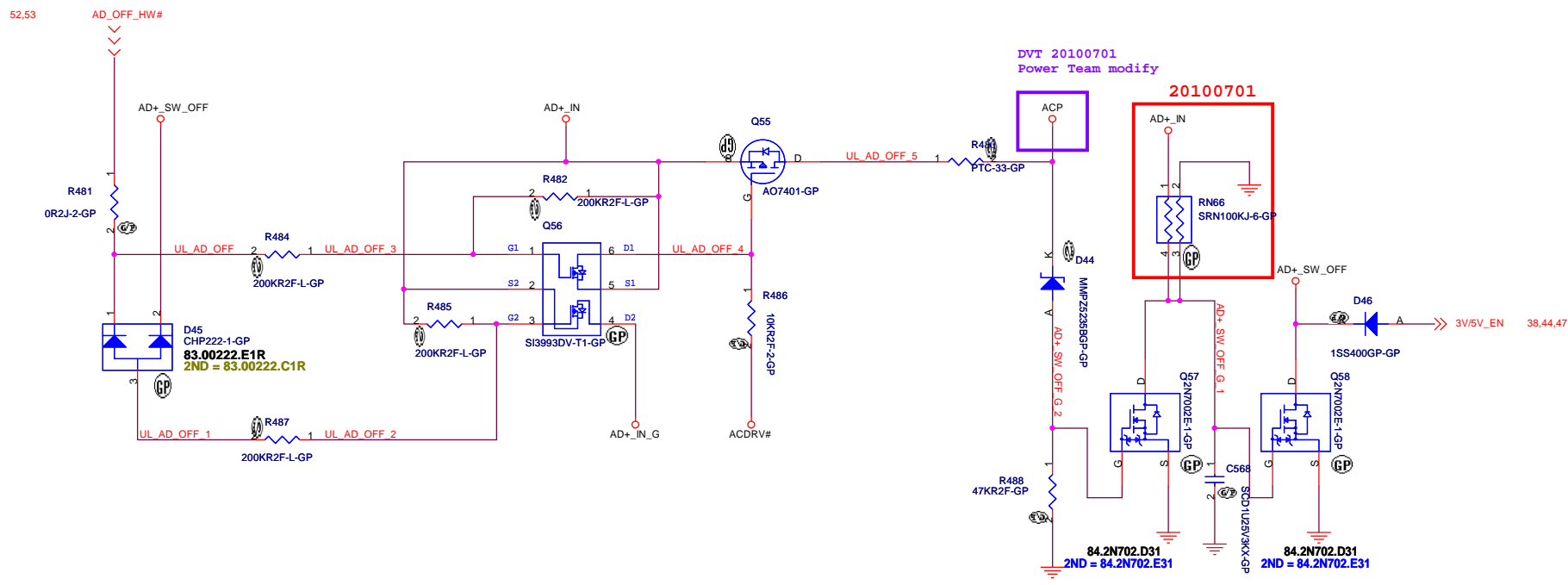
20100701

DVT 20100701
Power Team modify



DVT 1ST

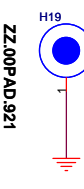
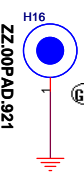
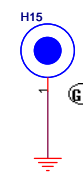
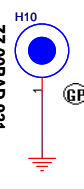
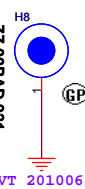
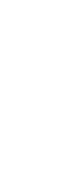
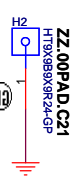
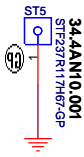
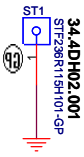
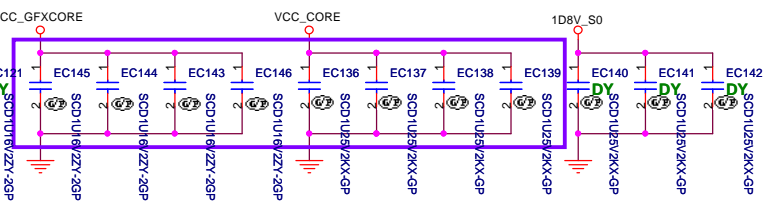
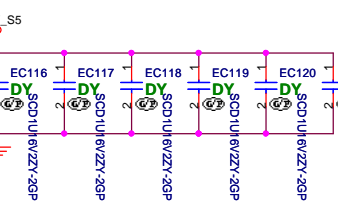
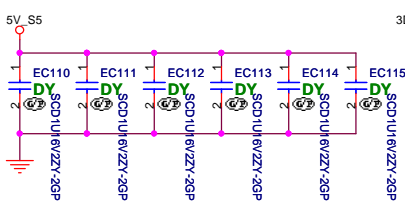
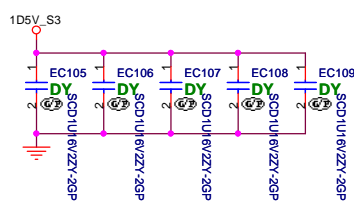
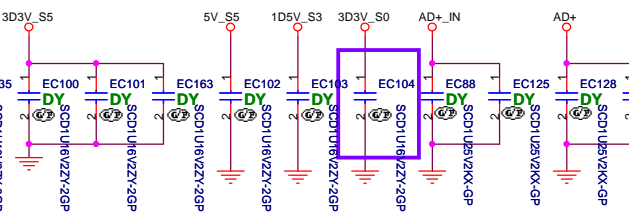
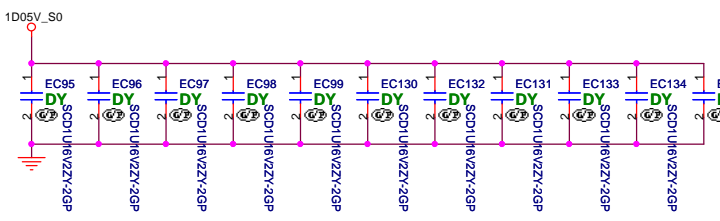
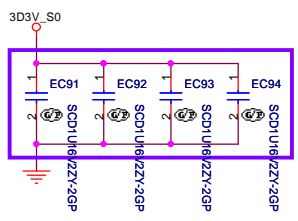
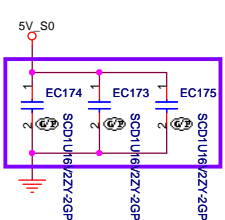
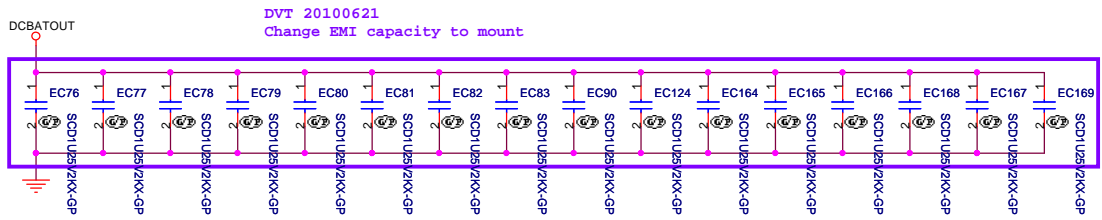
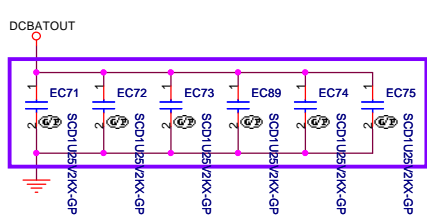
緯創資通 Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
UL circuit		
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Power Team modify

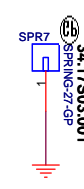
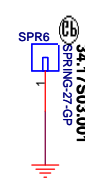
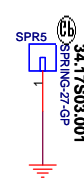
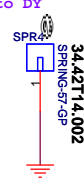
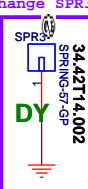
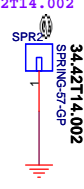
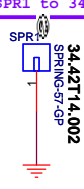
DVT 1ST

Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
UVP Protect	
Title TUCANA	Document Number Rev SB
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DVT 20100702 Change SPR1 to 34.42T14.002

DVT 20100623 Change SPR3 to DY



DVT 1ST

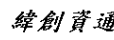
緯創資通 Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			Rev
EMI/Spring/Boss			
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EVT

2010/5/17	P.52[BQ24751_Charger]	Del D31 2nd 3rd source	2010/7/2	P.38[KBC_NPCE781L / KB]	Rename H_PROCHOT# to EC_PROCHOT
2010/5/17	P.25[HDMI CONN_PS8101]	Change 2nd source to 69.4R500.151		P.5[CPU SFF(2 of 8)-CLK/Thermal]	Add R128 for EC_PROCHOT pull-low to Gnd
2010/5/24	P.26[HDD Connector]	Change R148 to 3.3K ohm ,add C437 for PM_SLP_S3# Delay		P.5[CPU SFF(2 of 8)-CLK/Thermal]	Add Q61 for EC_PROCHOT to PROCHOT#
2010/5/27	P.38[KBC_NPCE781L / KB]	Add LCD_DETECT pull-high to 3D3V_S5		P.33[Audio Jack]	Add EC176 for HP_JD# to GND , Set Dummy for ESD.
2010/5/31	P.52[BQ24751_Charger]	Mount C546,R451,R449,Q51 for battery can't Charger			Add EC177 for MICT_JD# to GND , Set Dummy for ESD.
2010/6/1	P.24[CRT CONN]	Change F6 to 69.44002.001, for Cadiz use		P.55[EMI/Spring/Boss]	Change SPR1 to 34.42T14.002
2010/6/4	P.33[Audio Jack]	Change MICIN1 to 20.10133.L11 , follow connector list	2010/7/5	P.14[PCHE (3 of 9)-DMI/FDI]	Change D3 to schottky diode.
	P.28[USB]	Change USB1,USB2,USB3 connector to 22.10321.Q71 [follow ME connector list]		P.37[Thermal / Fan Controllor]	Delete Q29,Q30 main source 84.T3904.C11, follow CARAVEL-CP design
2010/6/10	P.36[AD / BATT CONN]	Change DCIN1 to 20.F0693.006 (follow connector list)	2010/7/6	P.53[UL CIRCUIT]	Rename R642 Pin1 contact to RTC_BAT_1 (Old use RTC_BAT),follow CARAVEL-CP
	P.41[FUNCTION BD & POWER BD]	Change PWCN1 to 20.F0693.006 (follow connector list)			
2010/6/11	P.41[FUNCTION BD & POWER BD]	Del FUNCN2 connector by ME request			
	P.38[KBC_NPCE781L / KB]	Change R240 to 20K ohm SB version.			
	P.25[HDMI CONN_PS8101]	Change R614~R617 to 200R2J , Set mount. [for EMI request]			
	P.25[HDMI CONN_PS8101]	Change C283,C364 to 1uF [for EMI request]			
	P.25[HDMI CONN_PS8101]	Change C282,C285 to 1KpF [for EMI request]			
2010/6/21	P.16[PCH (5 of 9)-PCI/USB]	Add PCI_REQ2# Pull-High to 3D3V_S0 by hang-up issue			
	P.31[Audio Codec ALC269]	Change EC23,EC24 to mount [for EMI request]			
	P.55[EMI/Spring/Boss]	Change DCBATAOUT capacity to mount (EC71~83,EC89,EC90,EC124,EC164~169) [for EMI request]			
		Change 5V_S0 capacity to mount (EC173-EC175) [for EMI request]			
		Change 3D3V_S0 capacity to mount (EC91~94,EC104) [for EMI request]			
		Change 3D3V_S3 capacity to mount (EC84~87) [for EMI request]			
		Change VCC_GFXCORE capacity to mount (EC142~146) [for EMI request]			
		Change VCC_CORE capacity to mount (EC136~139) [for EMI request]			
	P.36[AD / BATT CONN]	Change BT+ capacity to mount (EC32~35) [for EMI request]			
	P.23[LCD CONN]	Change C258 to 470pF (BRIGHTNESS_CN) [for EMI request]			
		Add C272 between BLON_OUT_R and Gnd [for EMI request]			
	P.34[CardReader RTS5186]	Change C576~580,C589 to 5pF [CardReader VEVs test]			
		Add 0.1uF between MS_INS# and GND [CardReader VEVs test]			
	P.24[CRT CONN]	Change R114,R115,R119,R120 to 2.7K ohm [CRT VEVs report]			
2010/6/22	P.53[UL CIRCUIT]	UL Circuit modify. [Prevent the RTC_BAT keep protecting.]			
2010/6/23	P.40[TouchPad]	Change THPAD1 to 20.K0487.006 [Follow ME connector list]			
	P.55[EMI/Spring/Boss]	Change SPR3 to DY [for EMI request]			
	P.53[UL CIRCUIT]	Add D42(83.00400.D1F), D41(83.00400.D1F) components. [Reduce the RTC_BAT discharge]			
		connect R467 pin1 to D41 and D42 pin k. [Reduce the RTC_BAT discharge]			
		connect D42 pin A to AD+_in. [Reduce the RTC_BAT discharge]			
	P.46[ADP3211_CPU CORE]	connect D41 pin A to ACP_UVP [Reduce the RTC_BAT discharge]			
		Change U45 to 84.08030.037 [Improve High side Vgs induce voltage]			
		Change U47 to 84.08028.037 [Improve High side Vgs induce voltage]			
		Change U48 to 84.08028.037 [Improve High side Vgs induce voltage]			
		add these statements. [follow Power Team design]			
		Change R316 to 7.87K ohm (old use 7.32K ohm) [Tune CPU Imon value]			
		Change C465 to 680pF (old use 560pF) [Tune CPU load line value]			
	P.47[RT8223_5V/3D3V]	Change R353 to 84.5K ohm (old use 97.6K ohm) [Adjust OCP value]			
		Change L13 to 2.2uH (old use 3.3uH) [IC needs higher sensing voltage to detect it.]			
	P.48[RT8209_1D5V]	Change R377 to 7.5K ohm (old use 11.5K ohm) [Adjust OCP value]			
	P.49[RT8209_1D05V]	Change R389 to 14.3K ohm (old use 10.2K ohm) [Adjust OCP value]			
		Change L15 to 0.56uH (old use 0.45uH) [Reduce the output ripple voltage]			
	P.50[ADP3211_GFX_CORE]	Change R419 to 56.2K ohm (old use 53.6K ohm) [Tune GFX load line value]			
		Change TC26 to mount.(old Dummy) [Improve under-shoot voltage phenomenon]			
2010/6/25	P.13[PCH (2 of 9)-PCIE/CLK/SMB]	Change C156,C157 to 12pF [for Crystal vendor Test]			
	P.29[LAN AR8131M]	Change C346 to 18pF [for Crystal vendor Test]			
	P.34[CardReader RTS5186]	Change C384,C388 to 15pF [for Crystal vendor Test]			
2010/6/29	P.17[PCH (6 of 9)-GPIO/RSVD]	Change RN31 to R648,R649 (56 ohm) for pull-high 1.05V_S0			
		Del R295 , because double pull-high			
2010/6/30	P.41[FUNCTION BD & POWER BD]	Change pin define of the FUNCN1 connector [follow the way of FFC folder for ME]			
	P.19[PCH (8 of 9)-PWR\SATA\USB]	Del R101 , only use 3D3V_S5			
	P.12[PCH (1 of 9)-SATA/RTC/HDA]	Change D1 to 83.R2003.I81 (SCHOTTKY DIODE)			
	P.25[HDMI CONN_PS8101]	Change Q12 to 84.2N702.D31 (ESD Protected 1.0KV)			
	P.44[RUN POWER]	Change D27 to 83.R2004.B8F (schottky diode)			
2010/7/1	P.46[ADP3211_CPU CORE]	Change OPEN-GAP to CLOSE-GAP (G9~14)			
	P.47[RT8223_5V/3D3V]	Change OPEN-GAP to CLOSE-GAP (G18,G22,G26,G30,G20,G24,G28,G32)			
		Change OPEN-GAP to CLOSE-GAP (G19,G23,G27,G31,G34,G36)			
		Change OPEN-GAP to CLOSE-GAP (G21,G25,G29,G33,G35,G37,G38)			
	P.48[RT8209_1D5V]	Change OPEN-GAP to CLOSE-GAP (G47,G49,G51,G53)			
		Change OPEN-GAP to CLOSE-GAP (G43~46,G48,G50,G52,G54~56)			
	P.49[RT8209_1D05V]	Change OPEN-GAP to CLOSE-GAP (G57,G58,G60,G62)			
		Change OPEN-GAP to CLOSE-GAP (G59,G61,G63~80)			
	P.50[ADP3211_GFX_CORE]	Change OPEN-GAP to CLOSE-GAP (G81~86)			
	P.51[RT8015_1D8V/ RT9026_0D75]	Change OPEN-GAP to CLOSE-GAP (G90~95)			
	P.41[FUNCTION BD & POWER BD]	Add F7 POL YSW for POWER BD 5V_S5 protect.			
	P.54[UVP Protect]	Delete R483 and add RN66. (RN66 part number is 66.10436.04L)			
		Connect AD+_IN to RN66 pin 1.			
		Connect RN66 pin2 to GND.			
		Connect RN66 pin3 and pin4 to AD+_SW_OFF_G_1			
	P.53[UL CIRCUIT]	Change R468 part number to the 64.36025.6DL			
		Change R469 to the part number 64.30025.6DL			
		Cummy R471 and mount D39.			
		Delete D40 and RN58.			
		Add R642. (Part number is 64.10045.6DL)			
		Connect R642 pin 1 to RTC_BAT.			
		Connect R642 pin2 to Q52 pin 2 and pin3.			
		Connect ACP to R435 pin 1.			
	P.52[BQ24751_Charger]	UPDATE BTCN1 PCB LAYOUT (REMOVE THE NPTH)			
	P.27[Bluetooth]				

<Core Design>

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HISTORY EVT	
Title	Rev
Size	SB
A2	68
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