Cathedral Peak II Block Diagram

Project code: 91.4K801.001
PCB P/N : 48.4K801.0SB
REVISION : 08219-SB

CLK GEN.
ICS 9LPRS365BKLFT (71.09365.A03)
RTM 875N-606-LFT (71.00875.C03)
3

Mobile CPU
Penryn 479
4, 5

THERMAL EMC2102
21

HOST BUS 667/800/1067MHz@1.05V

CRT 15
LCD 14

DDR2 DIMM1
667/800 MHz
12

DDR2 DIMM2
667/800 MHz
13

667/800MHz
667/800MHz

Cantiga
AGTL+ CPU I/F
DDR Memory I/F
INTEGRATED GRAHPICS
LVDS, CRT I/F
6,7,8,9,10,11

X4 DMI 400MHz
C-Link0

INT.MIC 16

Codec ALC268 28
AZALIA

MIC In 29

OP AMP APA2057 29
29 INT.SPKR

29 Line Out (NO SPDIF)

RJ11
MODEM MDC Card 23

ICH9M
6 PCIe ports
PCI/PCI BRIDGE
ACPI 2.0
4 SATA
12 USB 2.0/1.1 ports
ETHERNET (10/100/1000MbE)
High Definition Audio
LPC I/F
Serial Peripheral I/F
Matrix Storage Technology(DO)
Active Managemnet Technology(DO)
17,18,19,20

PCIex1 LAN Giga LAN 88E8071 25 → TXFM 26 → RJ45 26
PCIex1 New card 27 → PWR SW TPS2231 27
PCIex1 Mini Card Kedron a/b/g/n 27

LPC BUS
KBC ENE3310 30
BIOS Winbond W25X16 16M Bits 31
LPC DEBUG CONN 31
Launch Buttom 16

USB
Blue Tooth (USB) 23
Camera (USB) 14
Touch Pad 30
INT. KB 30

SATA
HDD SATA 22
ODD SATA 22
SATA

USB 3 Port 23
USB
CardReader Realtek RTS5158E 24
MS/MS Pro/xD /MMC/SD 5 in 1 24

Launch Board
LED Board
16

PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC TPS51125 35

INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC TPS51124 37

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 1D8V_S3

RT9026 36

1D8V_S3	DDR_VREF_S0 DDR_VREF_S3

RT9018A 36

1D8V_S3	1D5V_S0

CFXCORE DC/DC ISL6263 38

INPUTS	OUTPUTS
DCBATOUT	VGFXCORE 0.7~1.25V

CPU DC/DC ISL6266A 34

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0.35~1.5V

CHARGER BQ24745 39

INPUTS	OUTPUTS
DCBATOUT	BT+ DCBATOUT

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ICH9M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h). This signal has weak internal pull-down
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#/ GPIO53	PCIE config2 bit2, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#/ GPIO55	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#: SPI_CS1#/ GPIO58	Boot BIOS Destination Selection 0:1. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
SPI_MOSI	Integrated TPM Enable, Rising Edge of CLPWROK	Sample low: the Integrated TPM will be disabled. Sample high: the MCH TPM enable strap is sampled low and the TPM Disable bit is clear, the Integrated TPM will be enable.
GPIO49	DMI Termination Voltage, Rising Edge of PWROK.	The signal is required to be low for desktop applications and required to be high for mobile applications.
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH9 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be enabled in manufacturing environments using an external pull-up resister.

ICH9M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
CL_CLK[1:0]	PULL-UP 20K
CL_DATA[1:0]	PULL-UP 20K
CL_RST0#	PULL-UP 20K
DPRSLPVR/GPIO16	PULL-DOWN 20K
ENERGY_DETECT	PULL-UP 20K
HDA_BIT_CLK	PULL-DOWN 20K
HDA_DOCK_EN#/GPIO33	PULL-UP 20K
HDA_RST#	PULL-DOWN 20K
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GLAN_DOCK#	The pull-up or pull-down active when configured for native GLAN_DOCK# functionality and determined by LAN controller
GNT[3:0]#/GPIO[55,53,51]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
GPIO[49]	PULL-UP 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 20K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#/GPIO58/CLGPIO6	PULL-UP 20K
SPI_MOSI	PULL-DOWN 20K
SPI_MISO	PULL-UP 20K
SPKR	PULL-DOWN 20K
TACH_[3:0]	PULL-UP 20K
TP[3]	PULL-UP 20K
USB[11:0][P,N]	PULL-DOWN 15K

Cantiga chipset and ICH9M I/O controller Hub strapping configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	000 = FSB1067 011 = FSB667 010 = FSB800 others = Reserved
CFG[4:3] CFG8 CFG[15:14] CFG[18:17]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG6	iTPM Host Interface	0= The iTPM Host Interface is enabled(Note2) **1=The iTPM Host Interface is disalbed(default)**
CFG7	Intel Management engine Crypto strap	0 = Transport Layer Security (TLS) cipher suite with no confidentiality **1 = TLS cipher suite with confidentiality (default)**
CFG9	PCIE Graphics Lane	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG10	PCIE Loopback enable	0 = Enable (Note 3) **1= Disabled (default)**
CFG[13:12]	XOR/ALL	00 = Reserve 10 = XOR mode Enabled 01 = ALLZ mode Enabled (Note 3) **11 = Disabled (default)**
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG19	DMI Lane Reversal	**0 = Normal operation(Default): Lane Numbered in Order** 1 = Reverse Lanes DMI x4 mode[MCH -> ICH]:(3->0,2->1,1->2and0->3) DMI x2 mode[MCH -> ICH]:(3->0,2->1)
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	**0 = Only Digital Display Port or PCIE is operational (Default)** 1 =Digital display Port and PCIe are operting simulataneously via the PEG port
SDVO_CTRLDATA	SDVO Present	**0 =No SDVO Card Present (Default)** 1 = SDVO Card Present
L_DDC_DATA	Local Flat Panel (LFP) Present	**0 = LFP Disabled (Default)** 1= LFP Card Present; PCIE disabled

NOTE:
1. All strap signals are sampled with respect to the leading edge of the (G)MCH Power OK (PWROK) signal.
2. iTPM can be disabled by a 'Soft-Strap' option in the Flash-decriptor section of the Firmware. This 'Soft-Strap' is activated only after enabling iTPM via CFG6.
Only one of the CFG10/CFG/12/CFG13 straps can be enabled at any time.

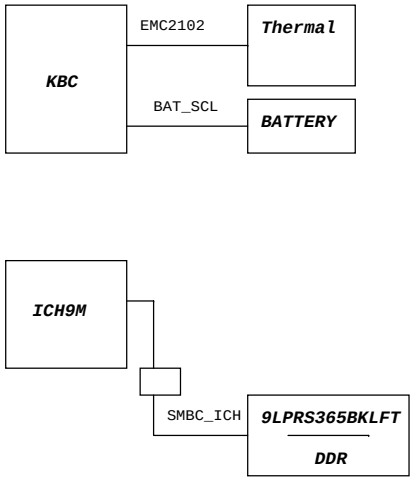
PCIE Routing

LANE1	LAN MARVELL 88E8071
LANE2	MiniCard WLAN
LANE3	*NC*
LANE4	*NC*
LANE5	NewCard
LANE6	*NC*

USB Table

USB	
Pair	*Device*
0	*USB1*
1	*NC*
2	*USB2*
3	*NC*
4	*USB3*
5	*Bluetooth*
6	*NC*
7	*MINIC1*
8	*WEBCAM*
9	*NEW1*
10	Card Reader
11	*NC*

SMBus



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Title: Reference

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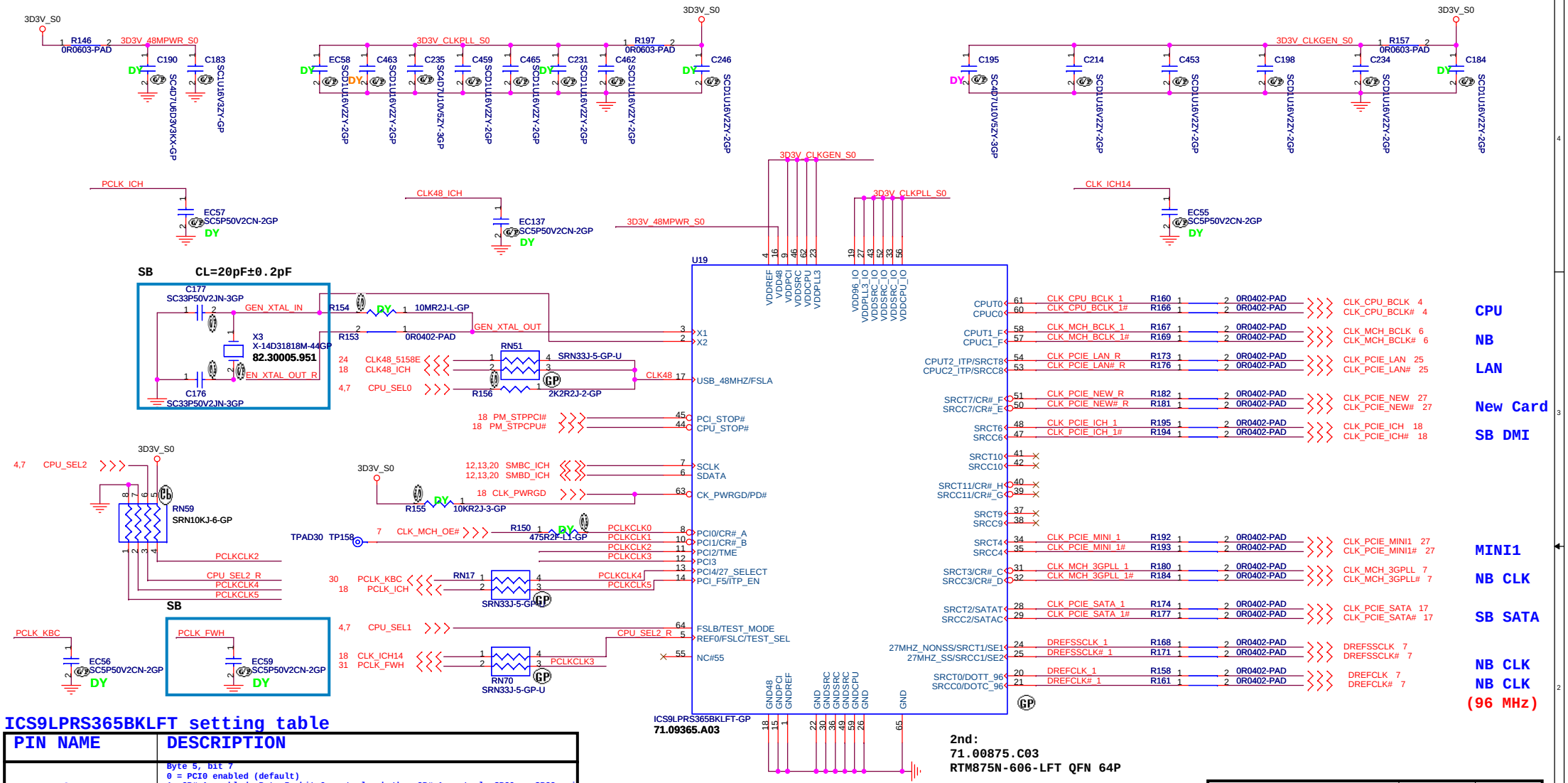

ICS9LPRS365BKLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	3.3V PCI clock output
PCI4/27M_SEL	0 = Pin24 as SRC-1, Pin25 as SRC-1#, Pin20 as DOT96, Pin21 as DOT96# 1 = Pin24 as 27MHz, Pin25 as 27MHz_SS, Pin20 as SRC-0, Pin21 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#
SRCT3/CR#_C	Byte 5, bit 3 0 = SRC3 enabled (default) 1= CR#_C enabled. Byte 5, bit 2 controls whether CR#_C controls SRC0 or SRC2 pair Byte 5, bit 2 0 = CR#_C controls SRC0 pair (default), 1= CR#_C controls SRC2 pair

PIN NAME	DESCRIPTION
SRCC3/CR#_D	Byte 5, bit 1 0 = SRC3 enabled (default) 1= CR#_D enabled. Byte 5, bit 0 controls whether CR#_D controls SRC1 or SRC4 pair Byte 5, bit 0 0 = CR#_D controls SRC1 pair (default) 1= CR#_D controls SRC4 pair
SRCC7/CR#_E	Byte 6, bit 7 0 = SRC7# enabled (default) 1= CR#_F controls SRC6
SRCT7/CR#_F	Byte 6, bit 6 0 = SRC7 enabled (default) 1= CR#_F controls SRC8
SRCC11/CR#_G	Byte 6, bit 5 0 = SRC11# enabled (default) 1= CR#_G controls SRC9
SRCT11/CR#_H	Byte 6, bit 4 0 = SRC11 enabled (default) 1= CR#_H controls SRC10

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1066M

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Title	Clock Generator	
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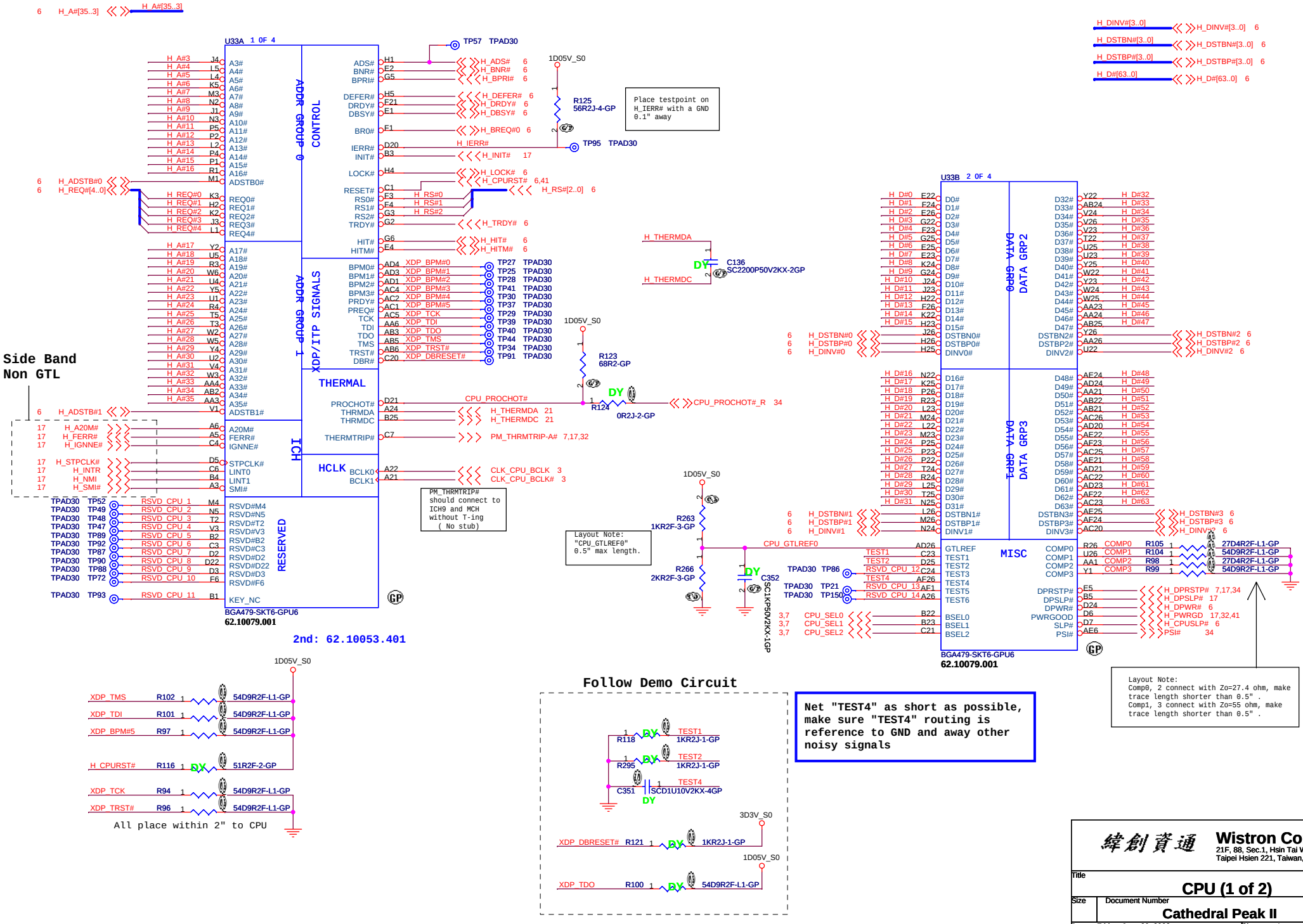
Side Band
Non GTL
U33A 1 OF 4
ADDR GROUP 0
ADDR GROUP 1
CONTROL
XDP/ITP SIGNALS
THERMAL
HCLK
ICH
RESERVED
BGA479-SKT6-GPU6
62.10079.001
2nd: 62.10053.401
U33B 2 OF 4
DATA GRP2
DATA GRP0
DATA GRP1
DATA GRP3
MISC
BGA479-SKT6-GPU6
62.10079.001
Follow Demo Circuit
Net "TEST4" as short as possible, make sure "TEST4" routing is reference to GND and away other noisy signals
All place within 2" to CPU
Place testpoint on H_IERR# with a GND 0.1" away
PM_THRMTRIP# should connect to ICH9 and MCH without T-ing (No stub)
Layout Note: "CPU_GTLREF0" 0.5" max length.
Layout Note: Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter than 0.5" . Comp1, 3 connect with Zo=55 ohm, make trace length shorter than 0.5" .
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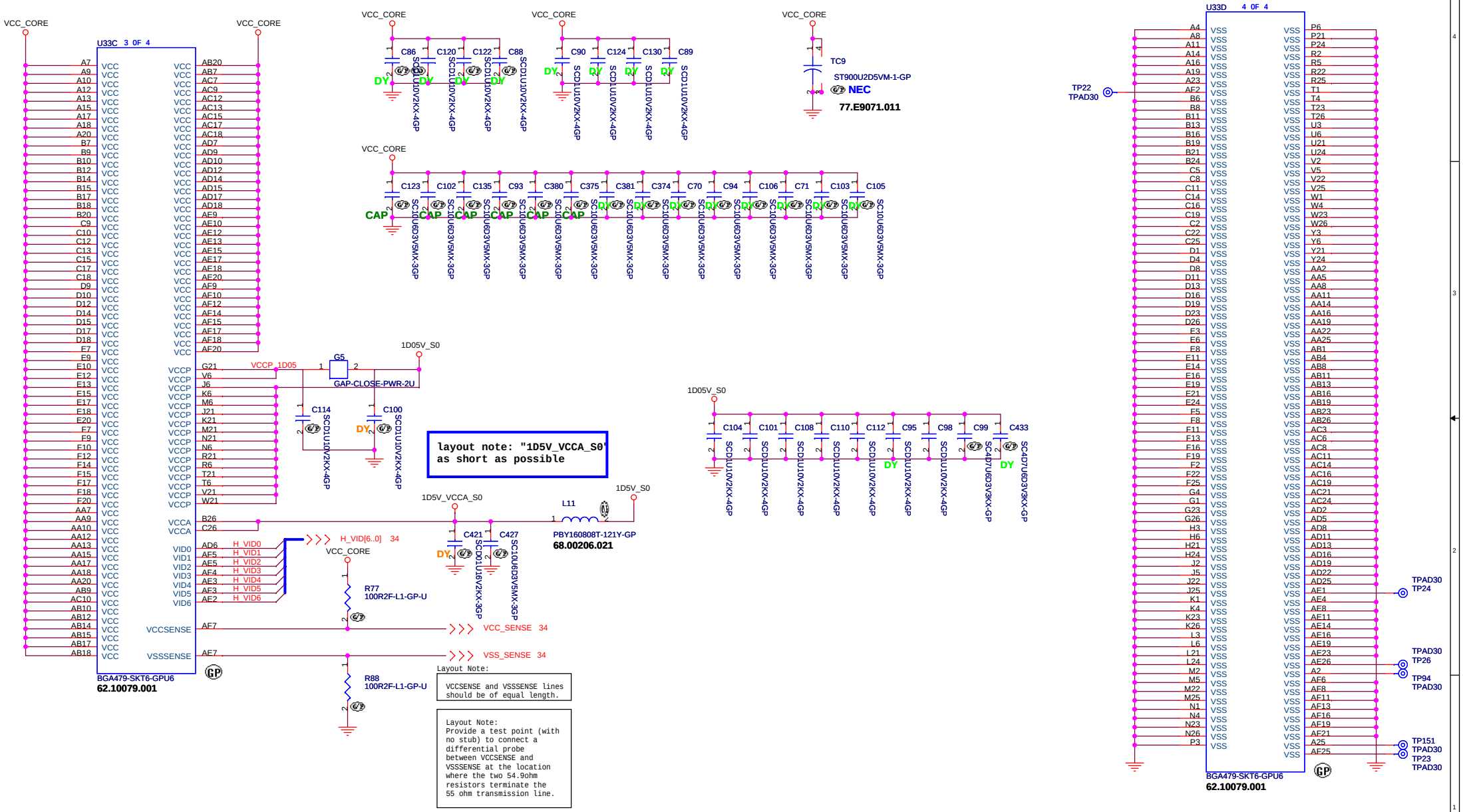

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Title	**CPU (2 of 2)**	
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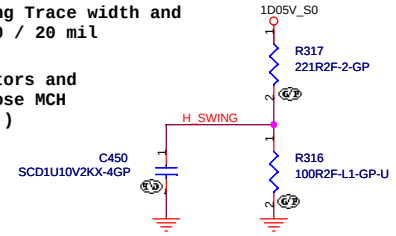
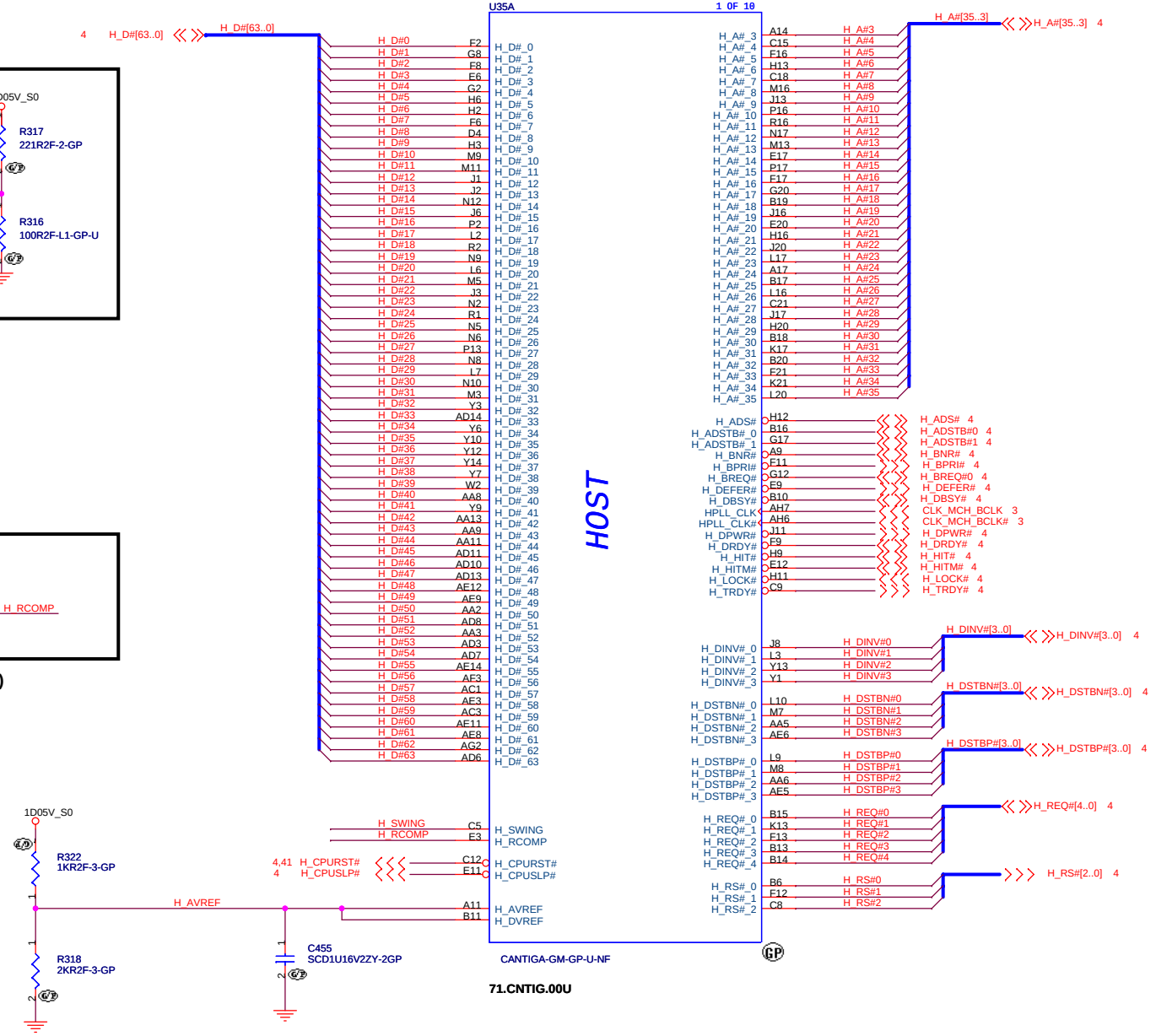
H_SWING routing Trace width and Spacing use 10 / 20 mil

H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil

Place them near to the chip (< 0.5")



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Title: Cantiga (1 of 6)	
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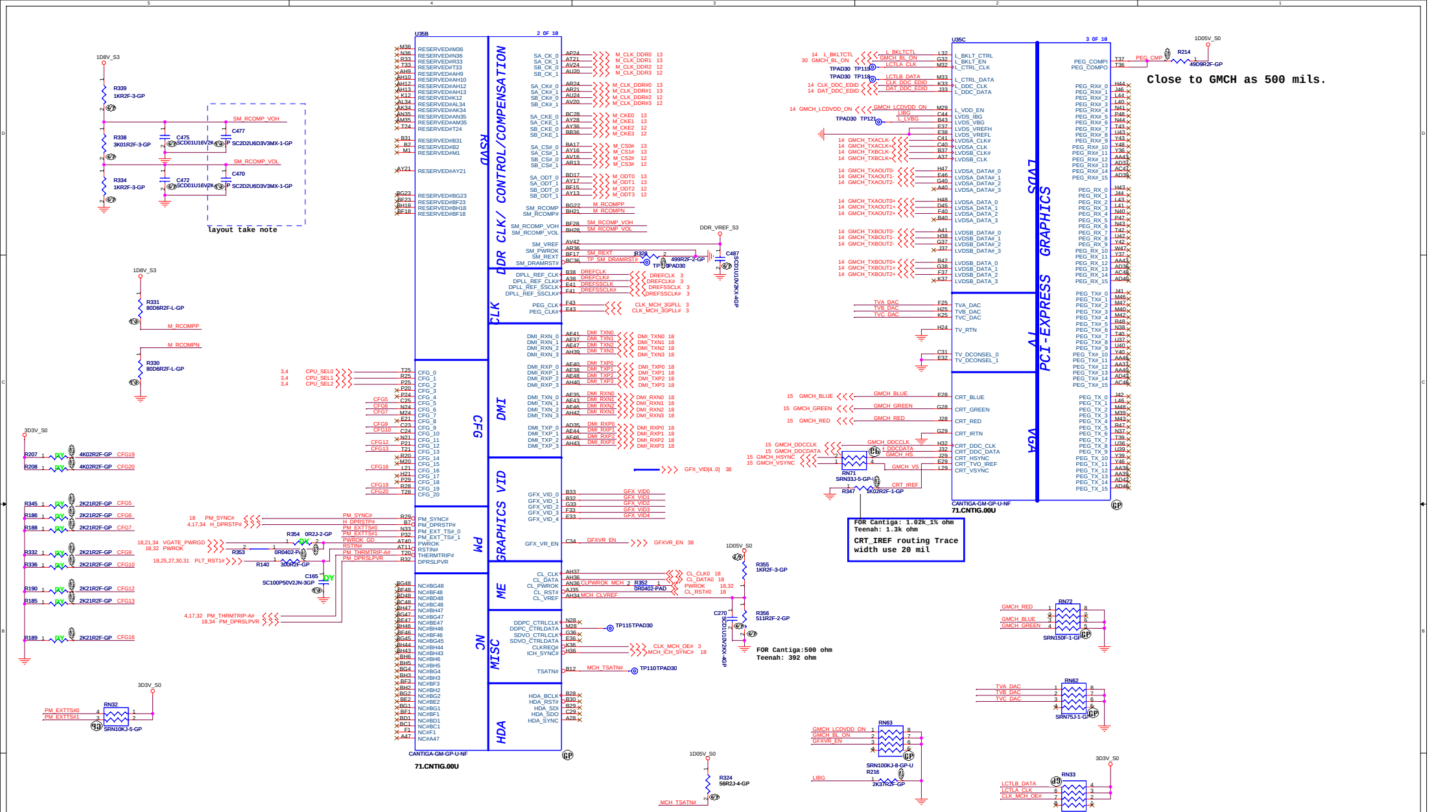

Pin Name	Strap Description	Configuration
CFG20	Digital DisplayPort (SDVO/DP/HDMI) Concurrent with PCIE	Low = Only digital DisplayPort (SDVO/DP/HDMI) or PCIE is operational (default) High = Digital DisplayPort (SDVO/DP/HDMI) and PCIE are operating simultaneously via the PEG port

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Title	Cantiga (2 of 6)	
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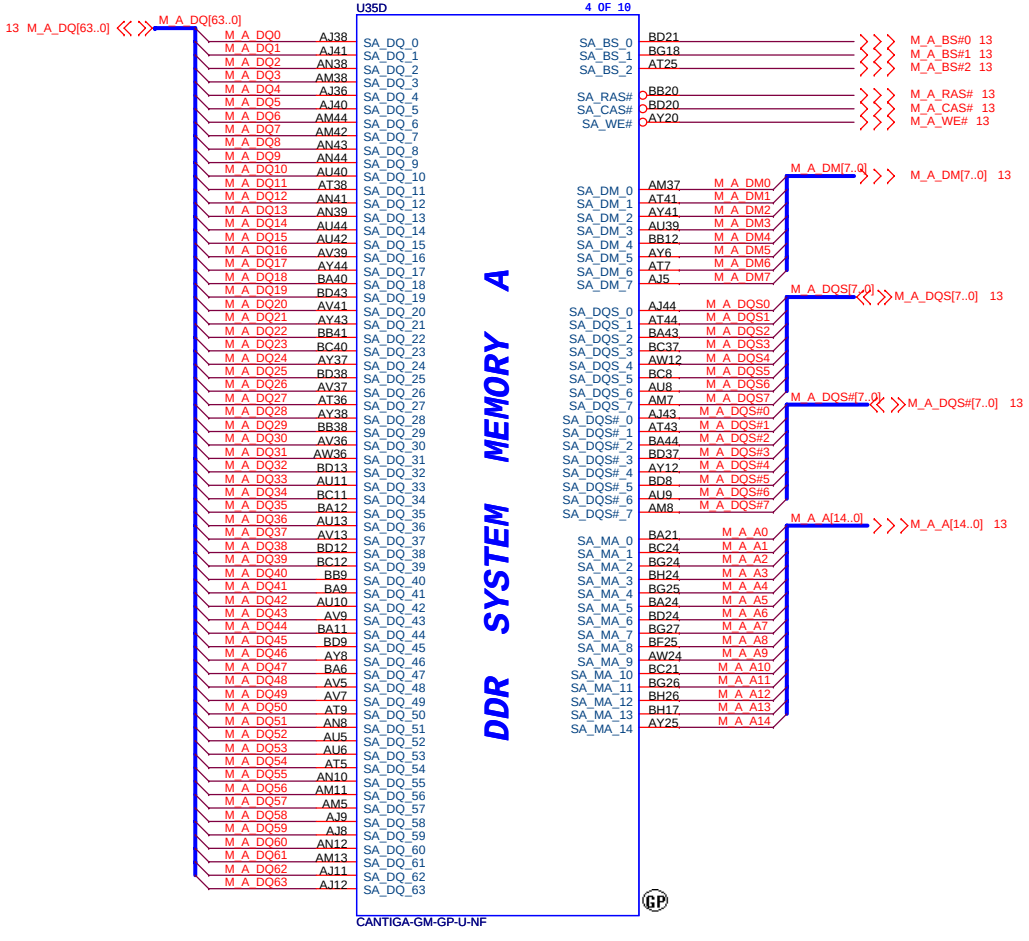

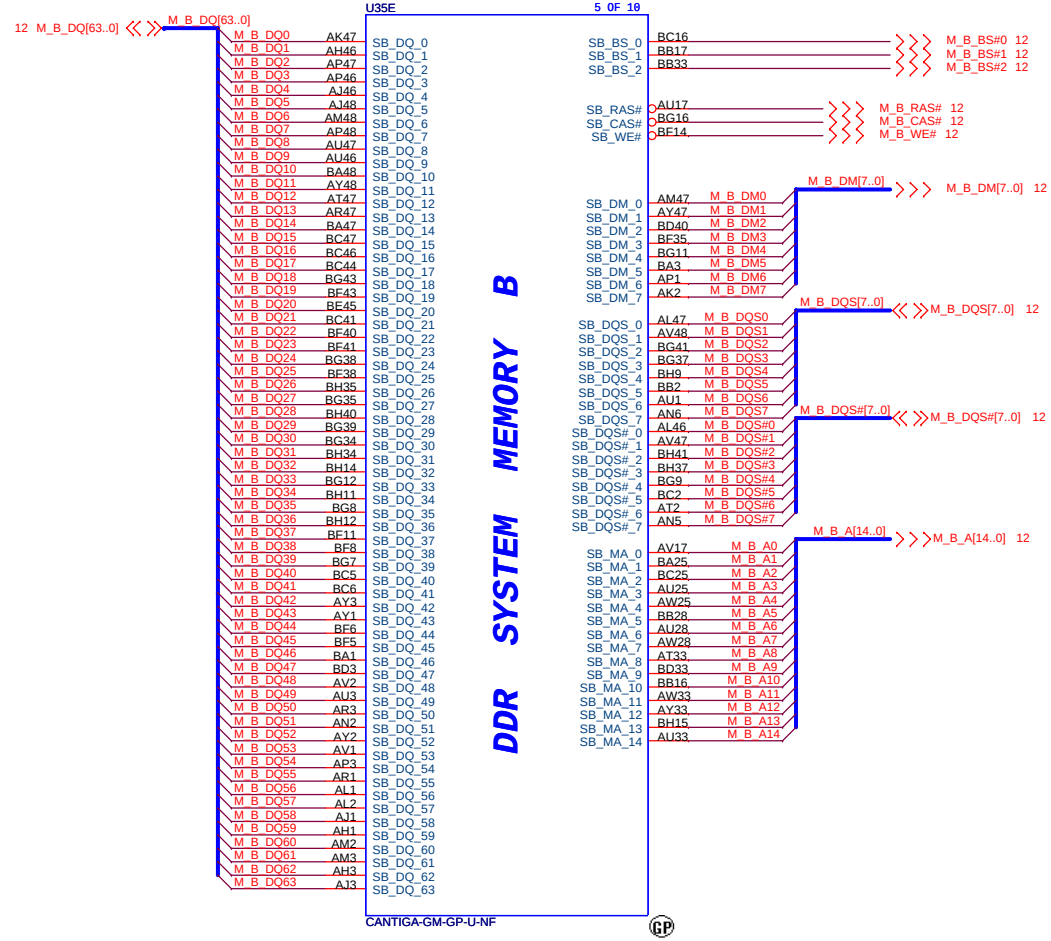

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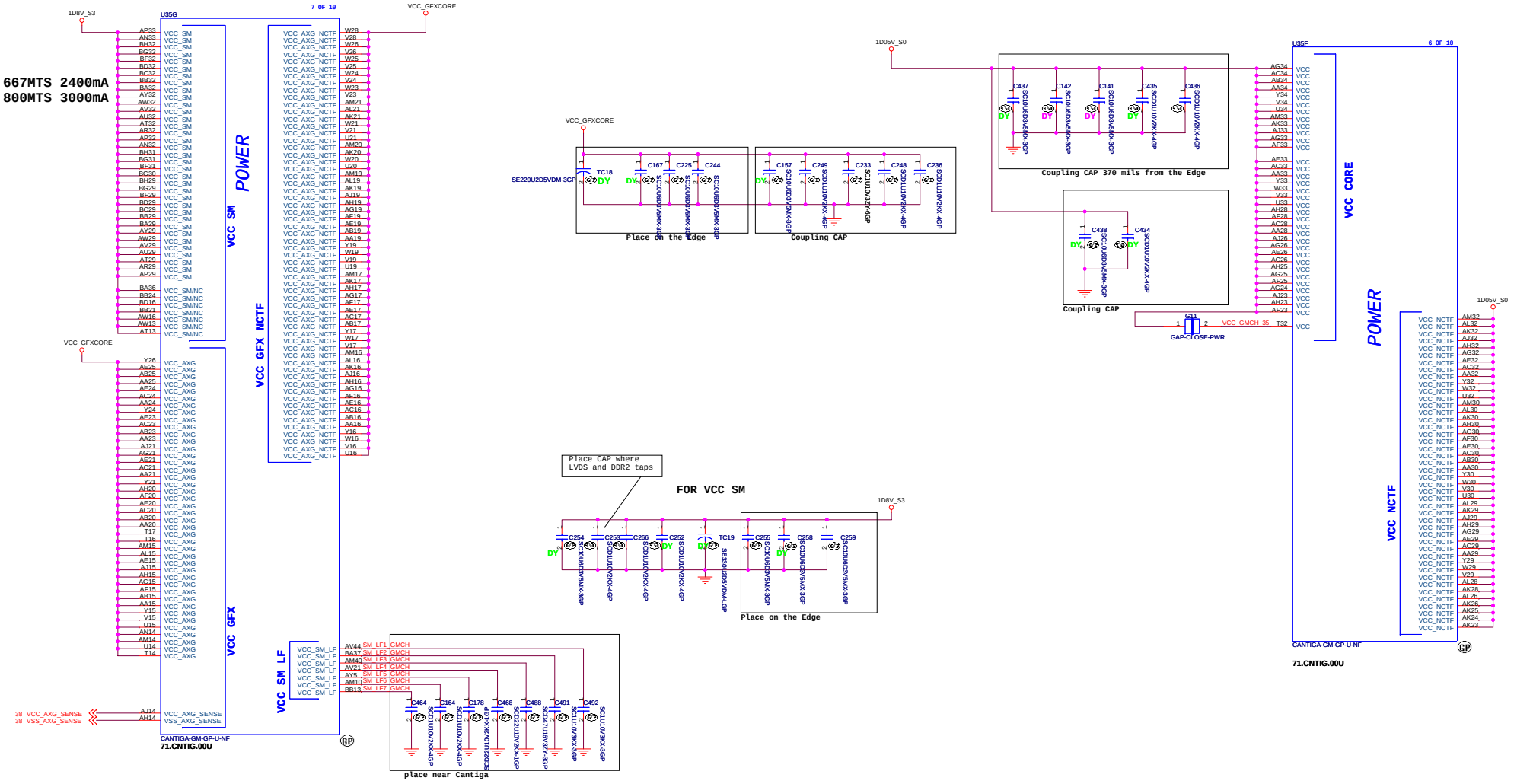
667MTS 2400mA
800MTS 3000mA



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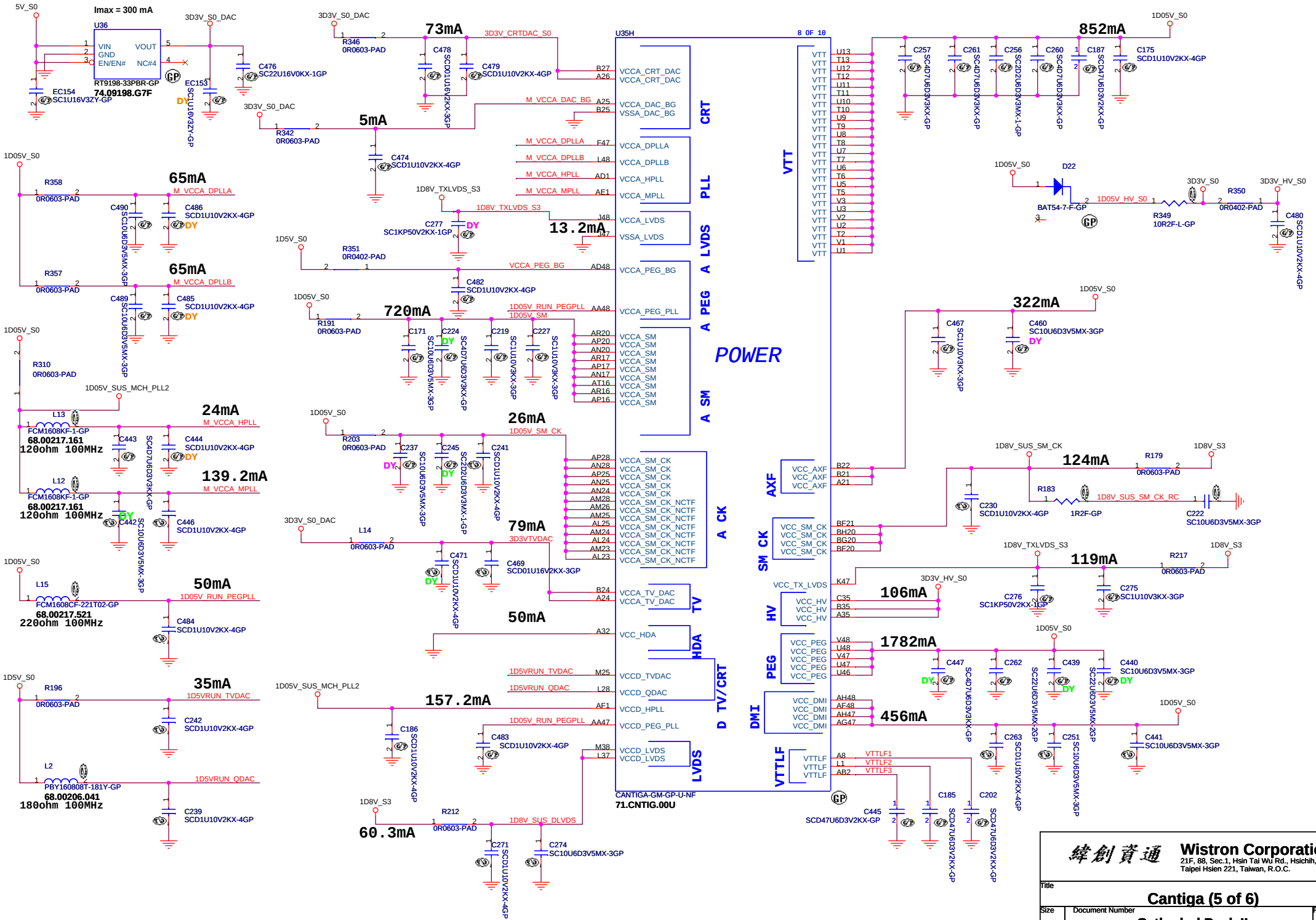

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Title: Cantiga (5 of 6)	
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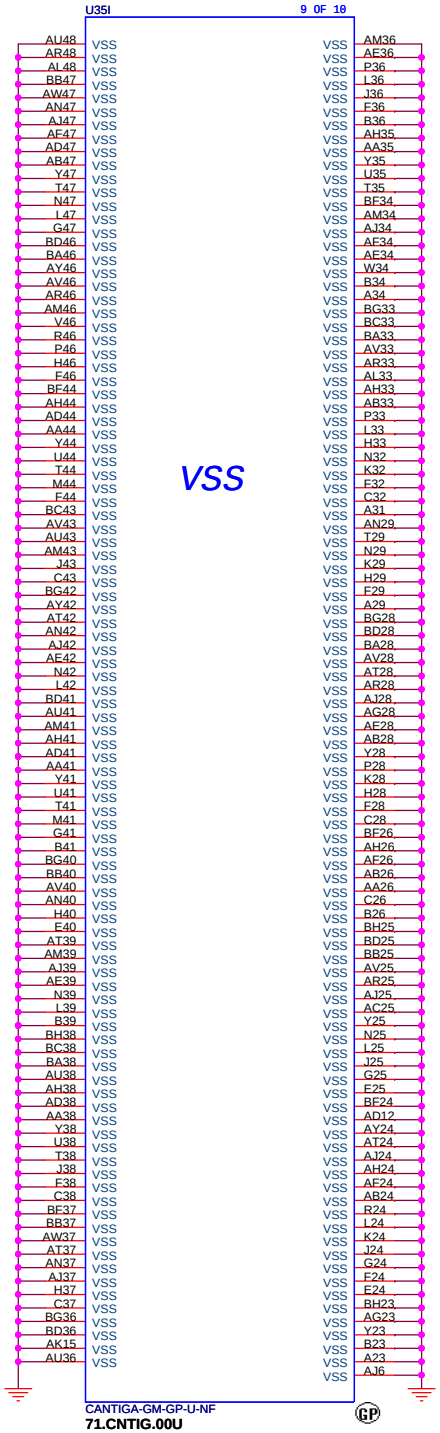

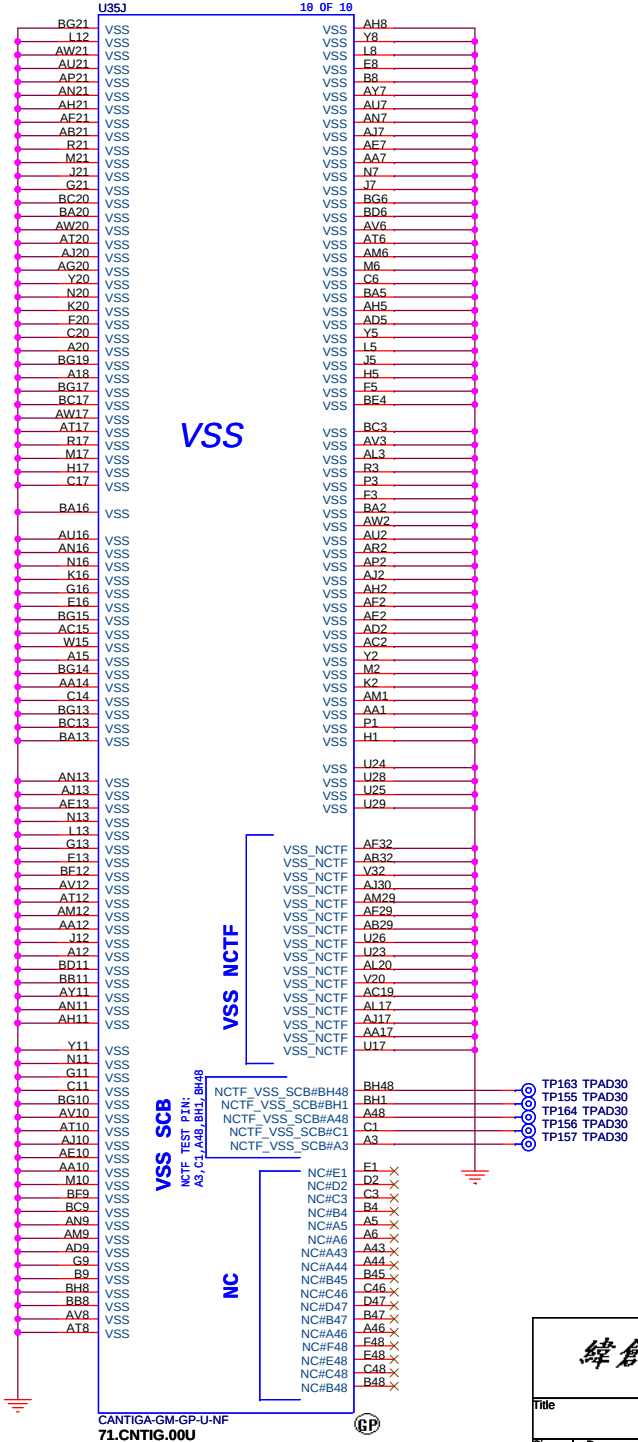

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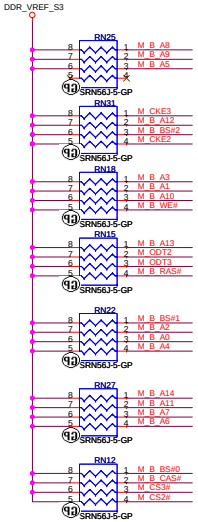
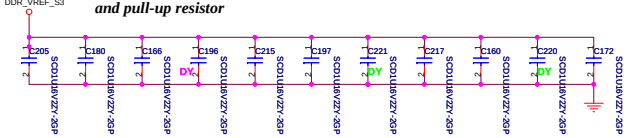
PARALLEL TERMINATION

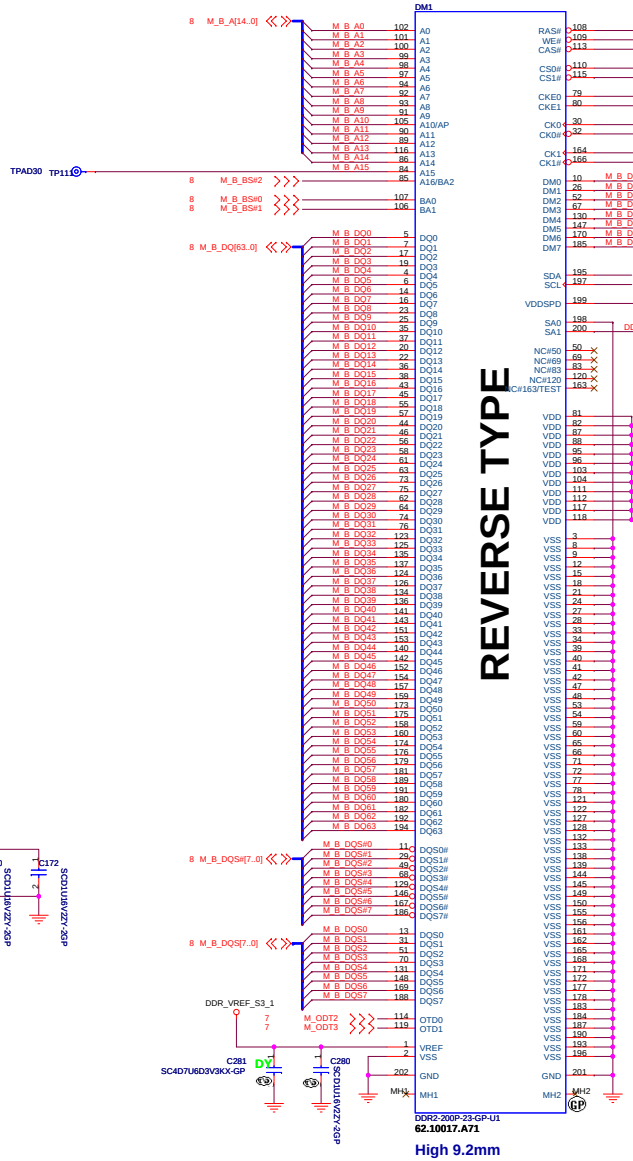
Put decap near power(0.9V) and pull-up resistor

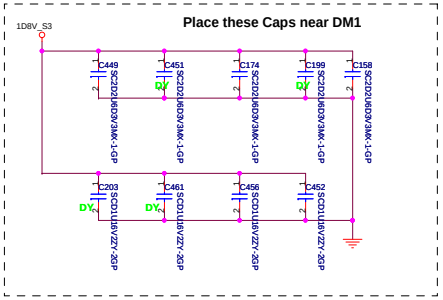


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor







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Title: **DDR2 Socket 0 (DM1)**

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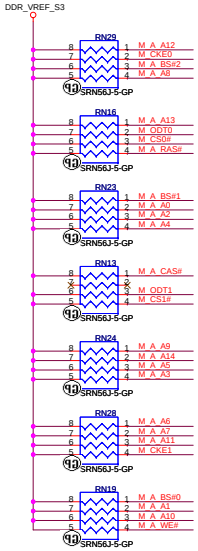
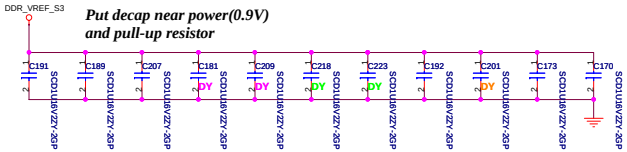
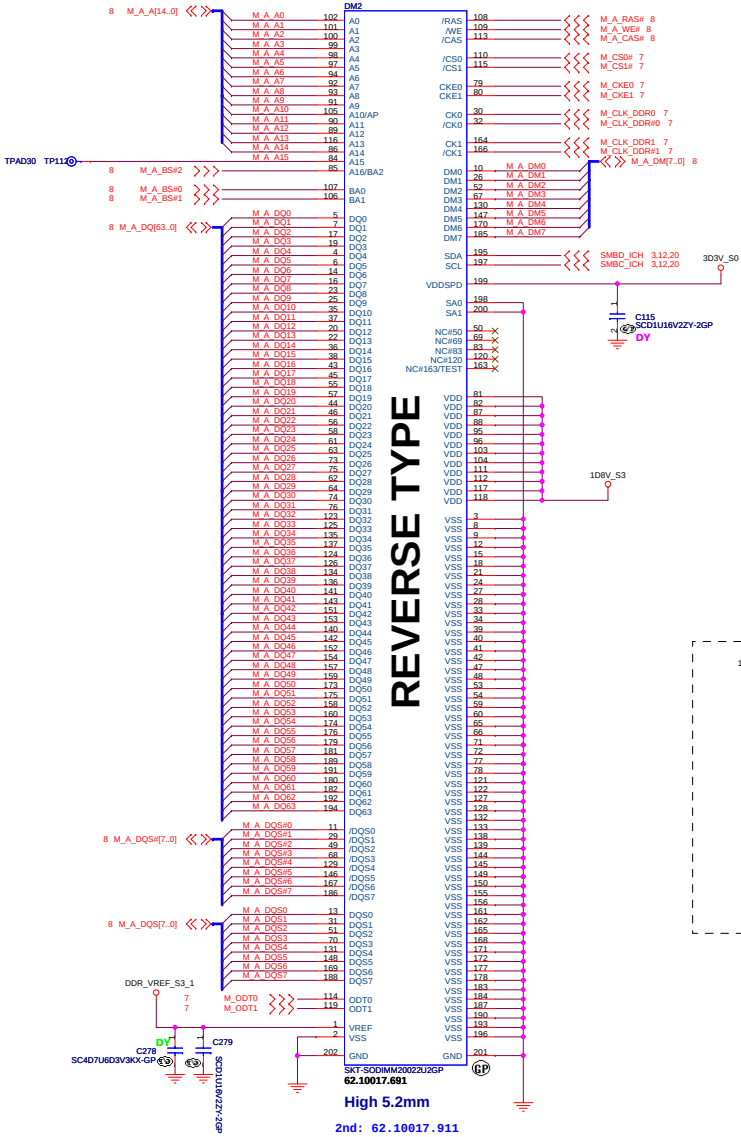
PARALLEL TERMINATION

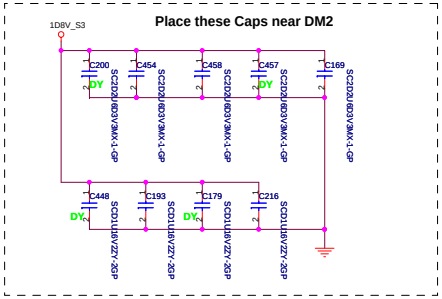
Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor







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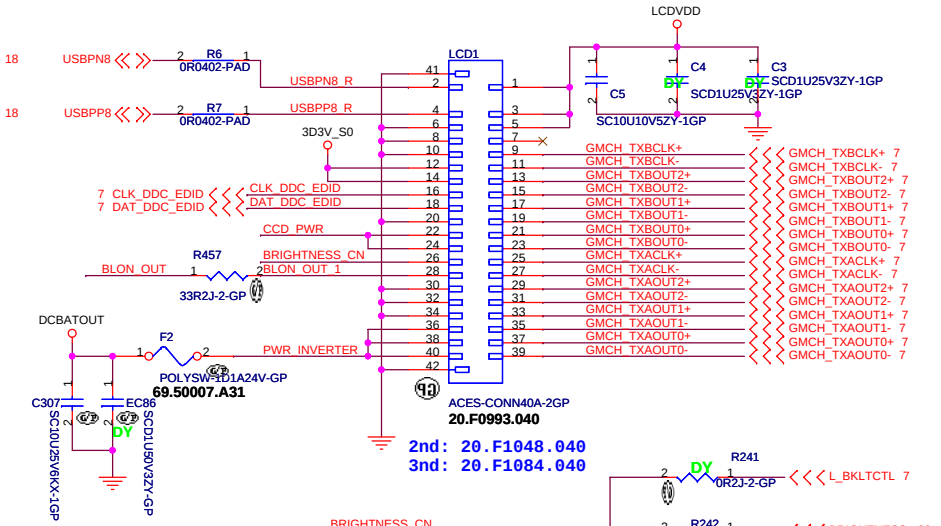
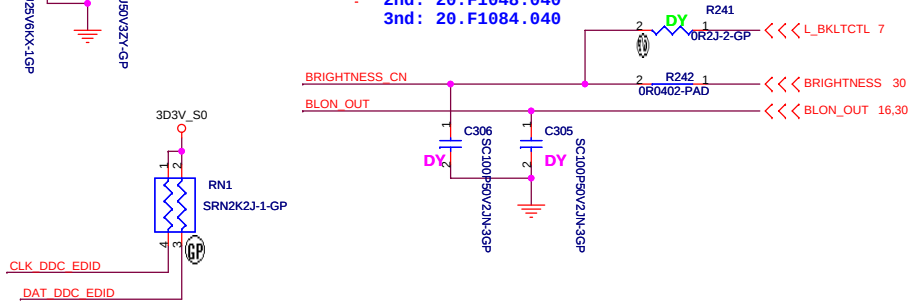
Title: DDR2 Socket 1 (DM2)

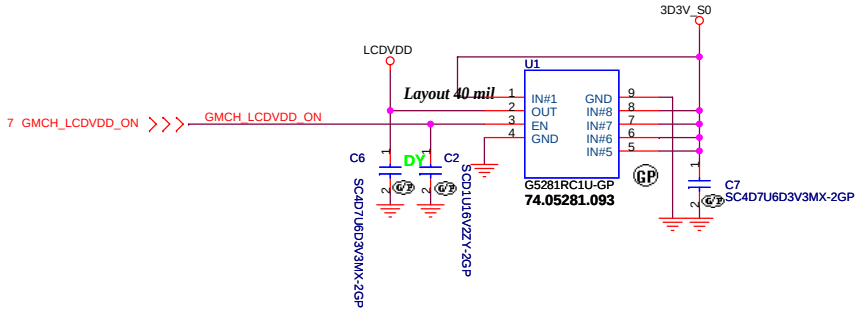
Size | Document Number: Cathedral Peak II | Rev: SB

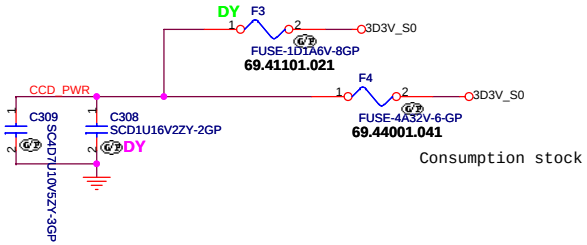
Date: Friday, June 20, 2008 | Sheet 13 of 43

LCD/INVERTER/CCD CONN







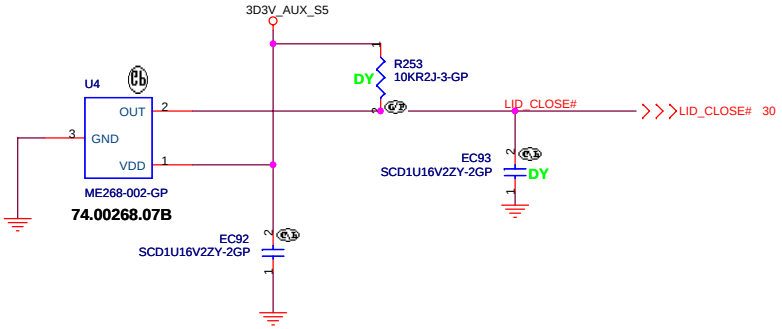


Consumption stock

Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

Cover Up Switch



74.00268.A7B
74.00268.C7B

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Title		
LCD CONN		
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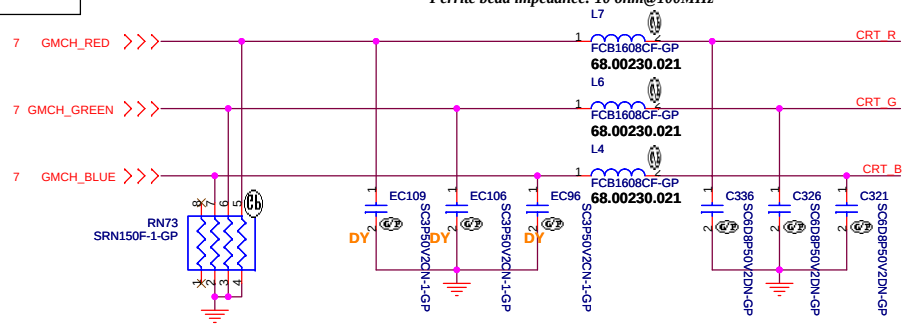
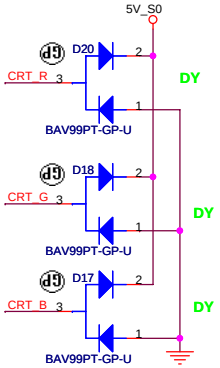
Layout Note:
Place these resistors close to the CRT-out connector

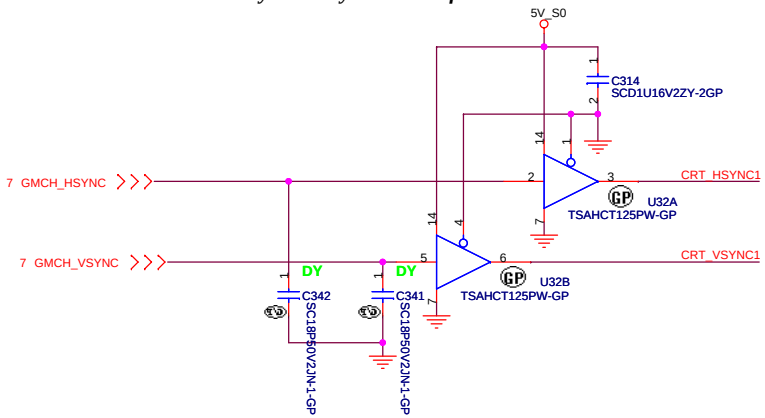
Ferrite bead impedance: 10 ohm@100MHz



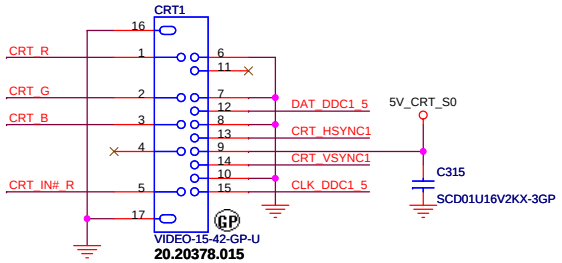


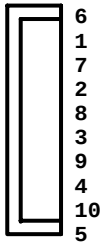
Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

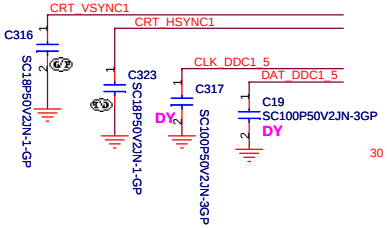
Hsync & Vsync level shift

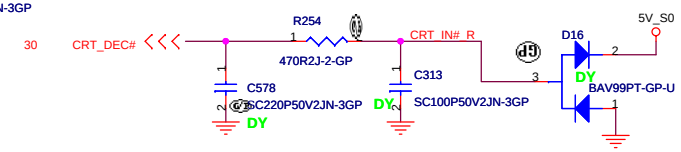


CRT I/F & CONNECTOR

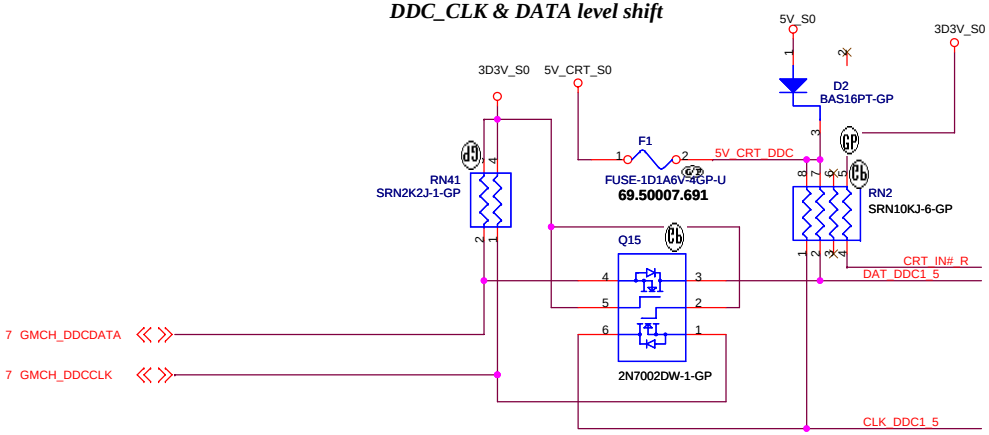








DDC_CLK & DATA level shift



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Title: CRT Connector		
Size	Document Number: Cathedral Peak II	Rev: SB
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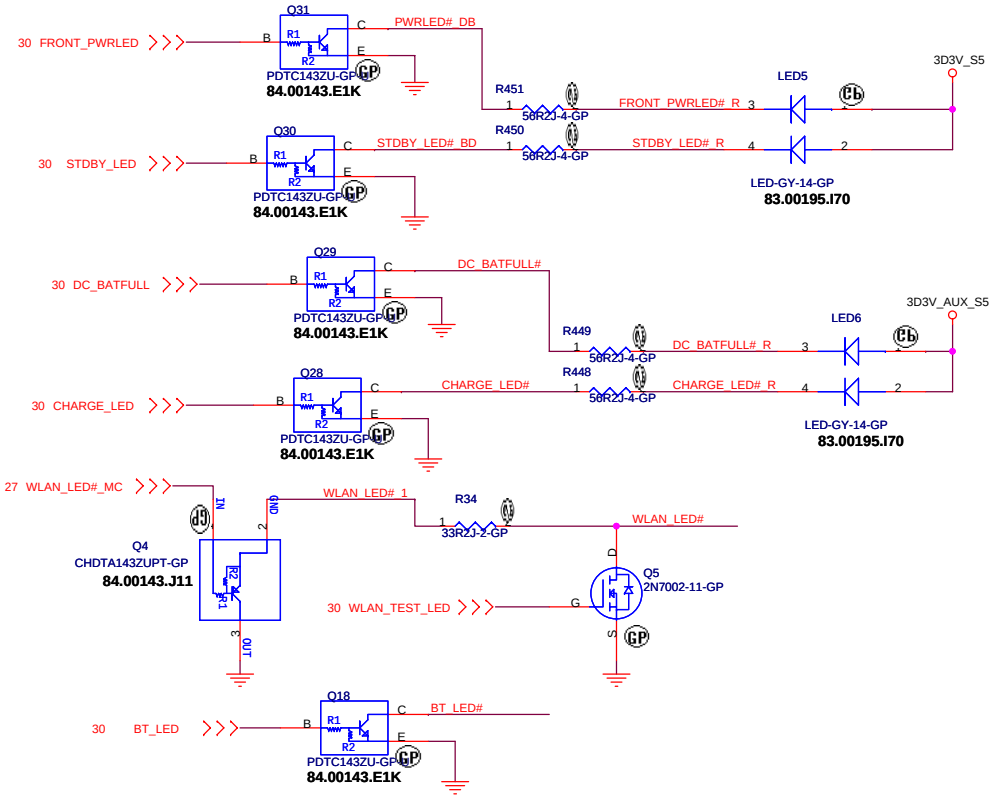
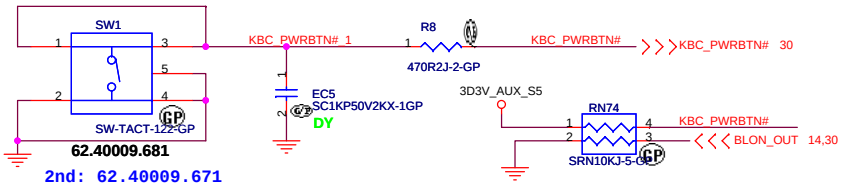
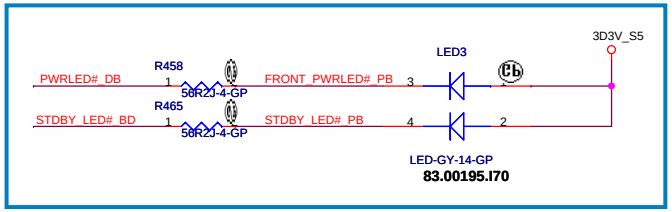


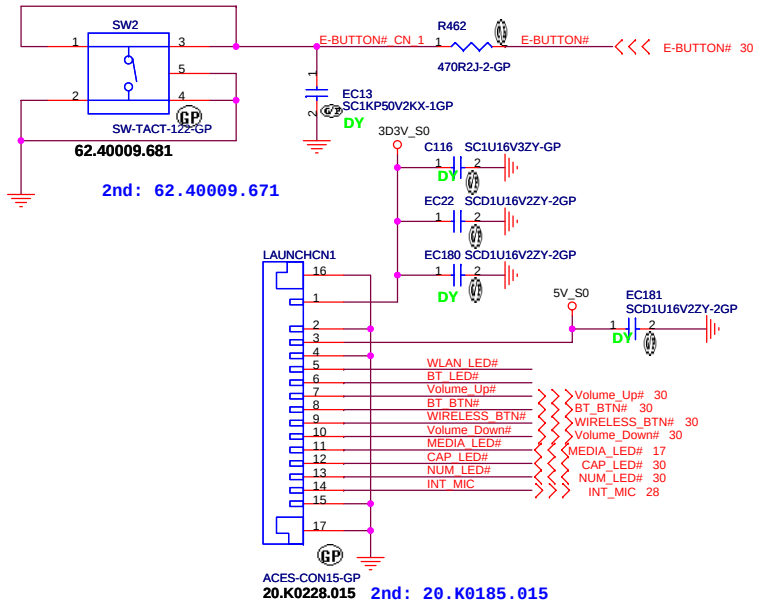
Power Button

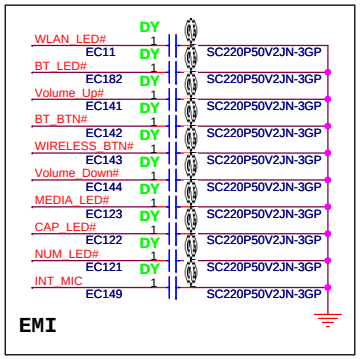


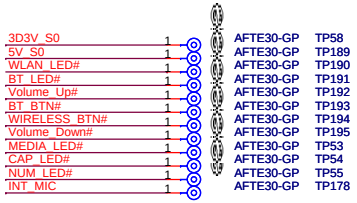
SB



E Power Button







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Title: POWER /LAUNCH/LED BOARD

Size | Document Number: Cathedral Peak II | Rev: SB

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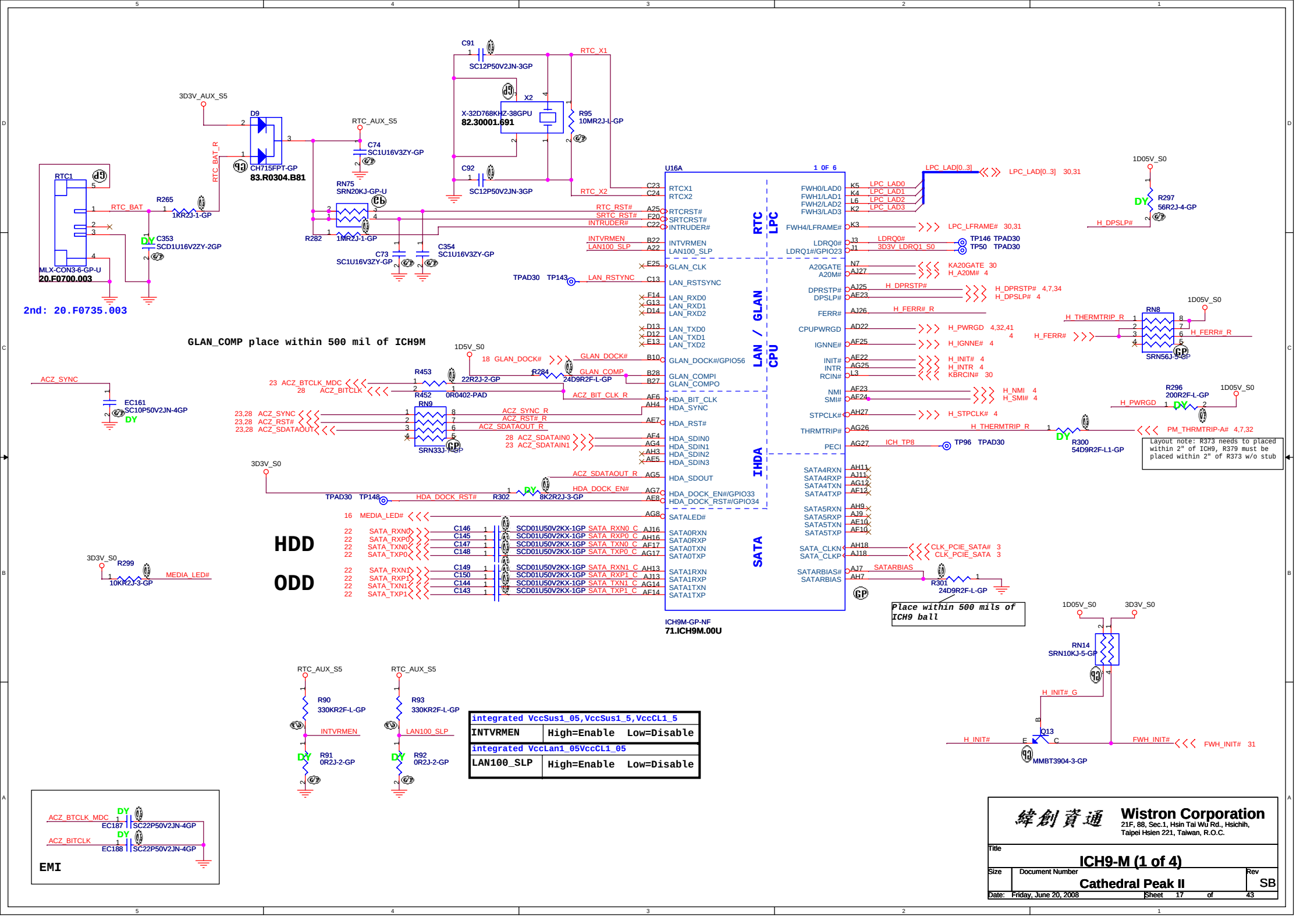
RTC1
MLX-CON3-6-GP-U
20.F0700.003
2nd: 20.F0735.003
RTC_BAT
RTC_BAT_R
R265
1KR2J-1-GP
D9
CH715FPT-GP
83.R0304.B81
3D3V_AUX_S5
RTC_AUX_S5
C74
SC1U16V3ZY-GP
C353
SCD1U16V2ZY-2GP
C91
SC12P50V2JN-3GP
X2
X-32D768KHZ-38GPU
82.30001.691
R95
10MR2J-L-GP
C92
SC12P50V2JN-3GP
RTC_X1
RTC_X2
RN75
SRN20KJ-GP-U
R282
1MR2J-1-GP
C73
SC1U16V3ZY-GP
C354
SC1U16V3ZY-GP
INTVRMEN
LAN100_SLP
RTC_RST#
SRTC_RST#
INTRUDER#
TPAD30
TP143
LAN_RSTSYNC
GLAN_COMP place within 500 mil of ICH9M
U16A
1 OF 6
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO56
GLAN_COMPI
GLAN_COMPO
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
PECI
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
LPC_LAD[0..3]
LPC_LFRAME#
H_A20M#
H_DPRSTP#
H_DPSLP#
H_FERR#
H_PWRGD
H_IGNNE#
H_INIT#
H_INTR
KBRCIN#
H_NMI
H_SMI#
H_STPCLK#
H_THERMTRIP_R
ICH_TP8
TP96
TP146
TP50
TP30
ICH9M-GP-NF
71.ICH9M.00U
ACZ_SYNC
EC161
SC10P50V2JN-4GP
R453
22R2J-2-GP
R452
0R0402-PAD
R284
24D9R2F-L-GP
RN9
SRN33J-7-GP
ACZ_BTCLK_MDC
ACZ_BITCLK
ACZ_SDATAOUT
ACZ_SYNC_R
ACZ_RST#_R
ACZ_SDATAOUT_R
ACZ_BIT_CLK_R
GLAN_DOCK#
GLAN_COMP
HDA_DOCK_RST#
HDA_DOCK_EN#
R302
8K2R2J-3-GP
MEDIA_LED#
R299
10KR2J-3-GP
HDD
ODD
SCD01U50V2KX-1GP
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
SATA_RXN1_C
SATA_RXP1_C
SATA_TXN1_C
SATA_TXP1_C
R90
330KR2F-L-GP
R91
0R2J-2-GP
R93
330KR2F-L-GP
R92
0R2J-2-GP
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
EMI
EC187
EC188
SC22P50V2JN-4GP
1D05V_S0
3D3V_S0
R297
56R2J-4-GP
RN8
SRN56J-3-GP
R296
200R2F-L-GP
R300
54D9R2F-L1-GP
PM_THRMTRIP-A#
Layout note: R373 needs to placed within 2" of ICH9, R379 must be placed within 2" of R373 w/o stub
R301
24D9R2F-L-GP
SATARBIAS
Place within 500 mils of ICH9 ball
RN14
SRN10KJ-5-GP
H_INIT# G
Q13
MMBT3904-3-GP
FWH_INIT#
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Title
ICH9-M (1 of 4)
Size
Document Number
Cathedral Peak II
Rev
SB
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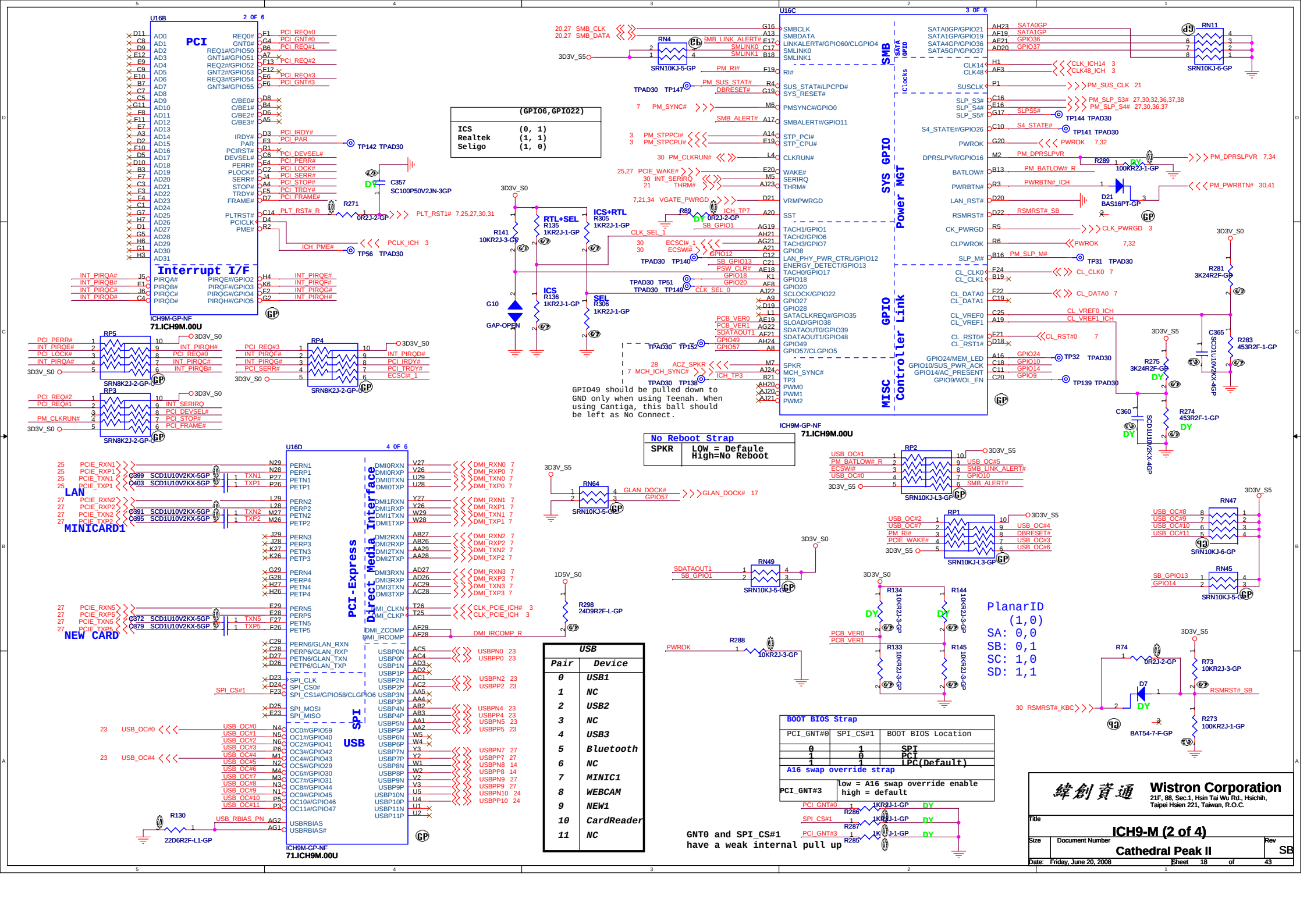
U16B
2 OF 6
PCI
Interrupt I/F
ICH9M-GP-NF
71.ICH9M.00U
(GPIO6,GPIO22)
ICS (0, 1)
Realtek (1, 0)
Seligo (0, 1)
U16C
3 OF 6
SMB
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
ICH9M-GP-NF
71.ICH9M.00U
GPIO49 should be pulled down to GND only when using Teenah. When using Cantiga, this ball should be left as No Connect.
No Reboot Strap
SPKR LOW = Defaule
High=No Reboot
U16D
4 OF 6
PCI-Express
Direct Media Interface
SPI
USB
LAN
MINICARD1
NEW CARD
ICH9M-GP-NF
71.ICH9M.00U
USB
Pair Device
0 USB1
1 NC
2 USB2
3 NC
4 USB3
5 Bluetooth
6 NC
7 MINIC1
8 WEBCAM
9 NEW1
10 CardReader
11 NC
GNT0 and SPI_CS#1 have a weak internal pull up
BOOT BIOS Strap
PCI_GNT#0 SPI_CS#1 BOOT BIOS Location
0 1 SPI
1 0 PCI
1 1 LPC(Default)
A16 swap override strap
PCI_GNT#3 low = A16 swap override enable
high = default
PlanarID (1,0)
SA: 0,0
SB: 0,1
SC: 1,0
SD: 1,1
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Title
ICH9-M (2 of 4)
Size
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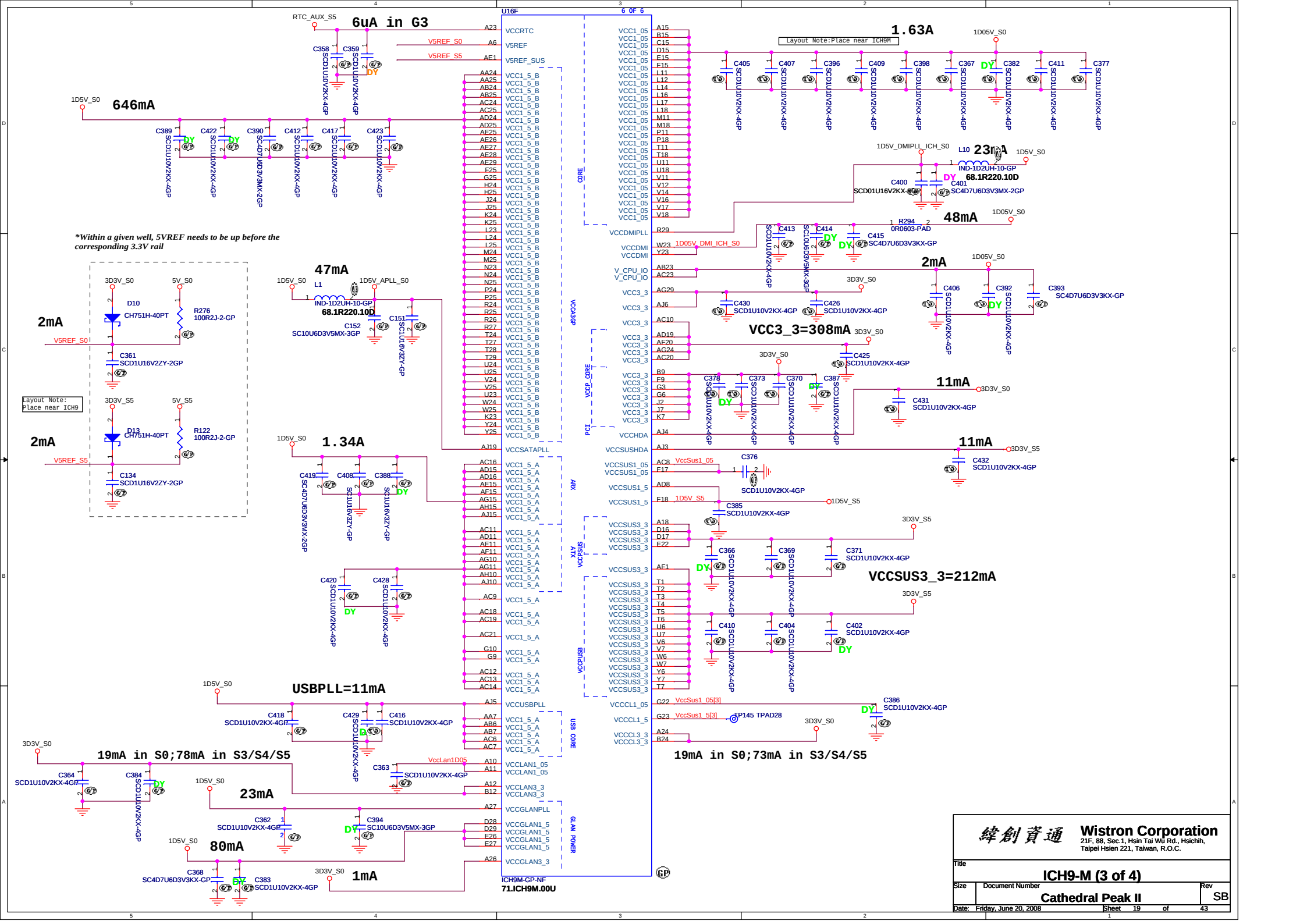
6uA in G3
646mA
1.63A
23mA
48mA
2mA
47mA
1.34A
VCC3_3=308mA
11mA
VCCSUS3_3=212mA
USBPLL=11mA
19mA in S0;78mA in S3/S4/S5
23mA
80mA
1mA
19mA in S0;73mA in S3/S4/S5
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
Layout Note:Place near ICH9M
Layout Note: Place near ICH9
U16F
6 OF 6
ICH9M-GP-NF
71.ICH9M.00U
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ICH9-M (3 of 4)
Cathedral Peak II
SB
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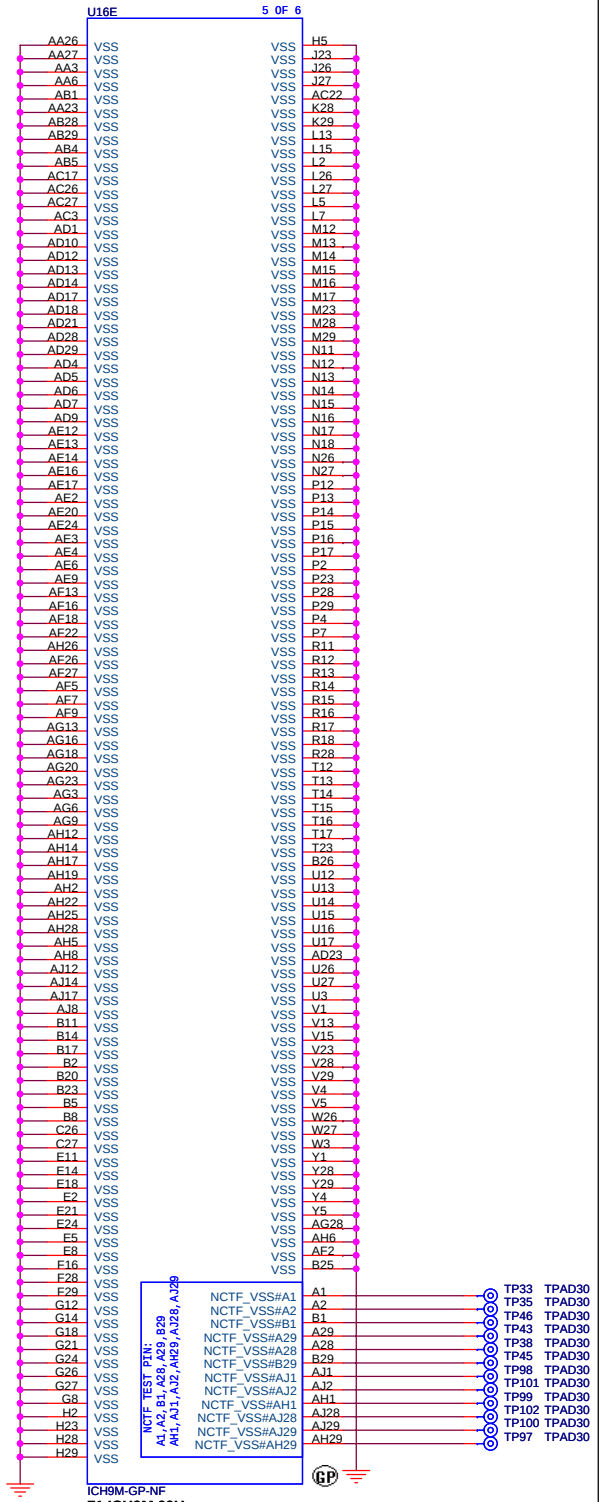

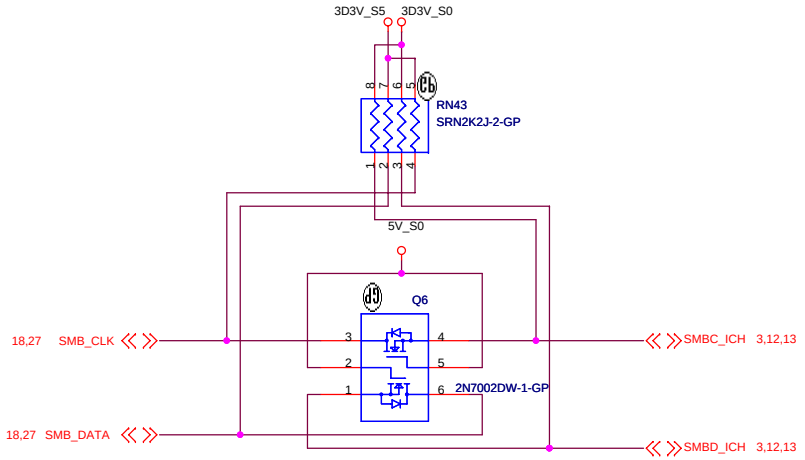

SMBUS

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Title	**ICH9-M (4 of 4)**	
Size	Document Number: **Cathedral Peak II**	Rev: SB
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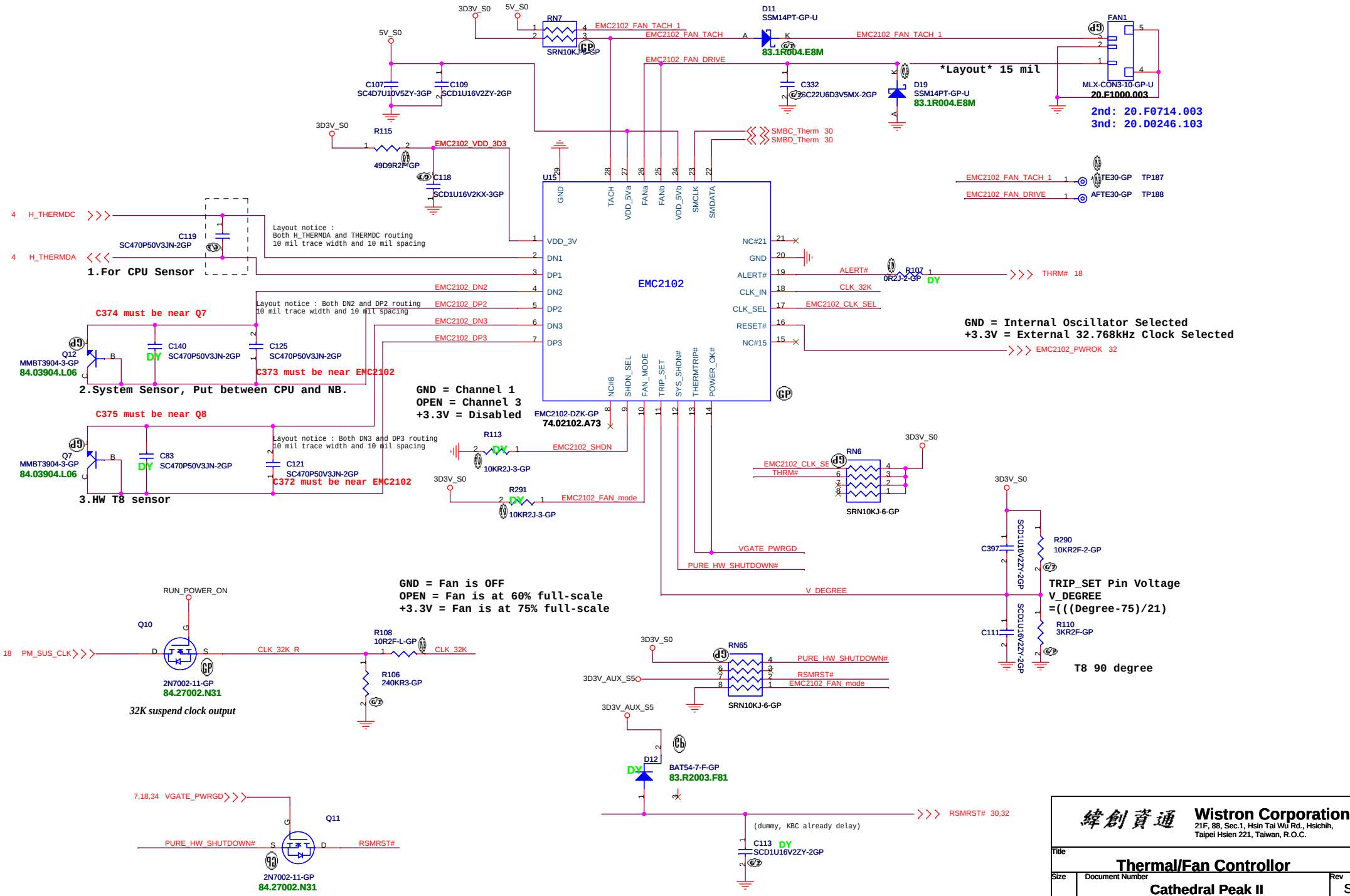

緯創資通 **Wistron Corporation**
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Title: **Thermal/Fan Controllor**

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	Cathedral Peak II	SB

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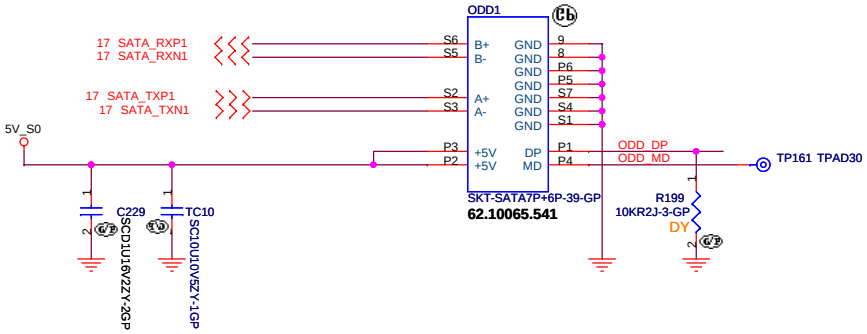
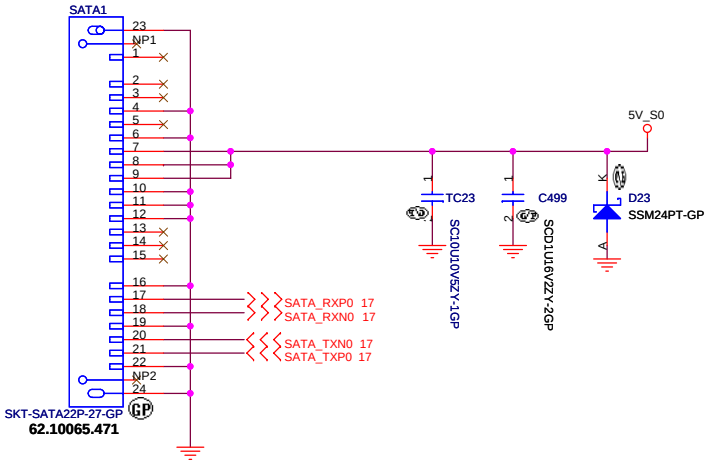
SATA ODD Connector



SATA Connector



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**HDD & CDROM**	
Size	Document Number **Cathedral Peak II**	Rev SB
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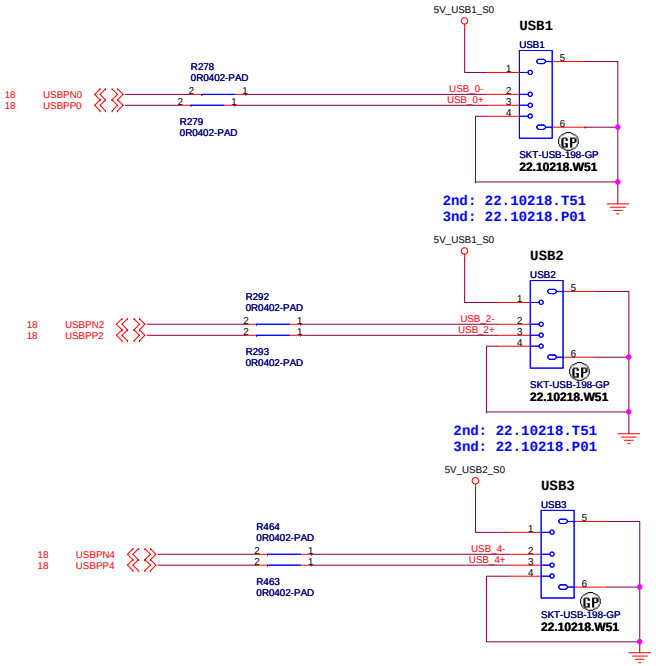
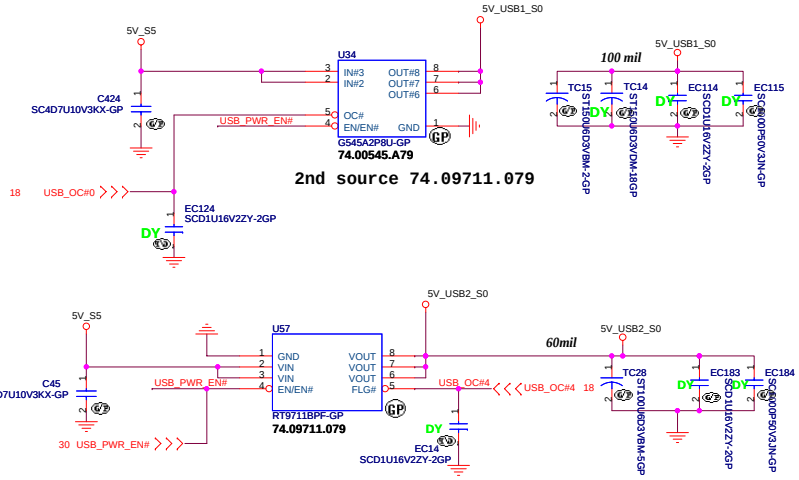
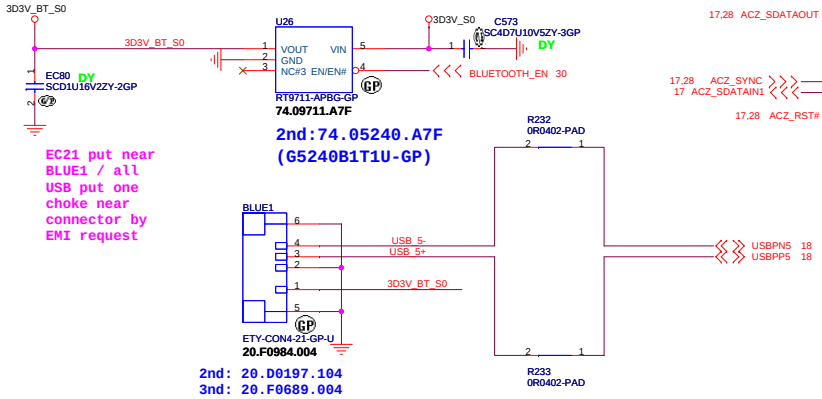


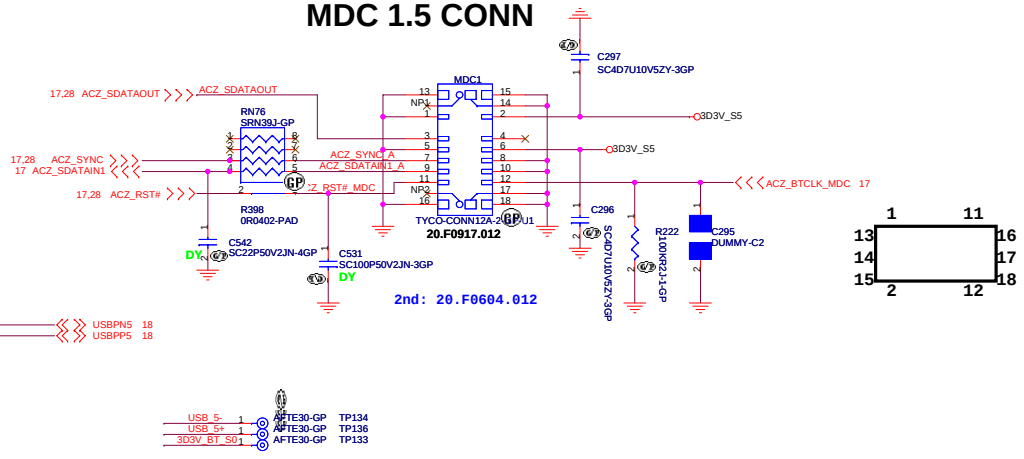


BLUETOOTH MODULE

1.5A / High Active Voltage 2V



MDC 1.5 CONN



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	USB/BLUETOOTH/MDC	
Size	Document Number: Cathedral Peak II	Rev: SB
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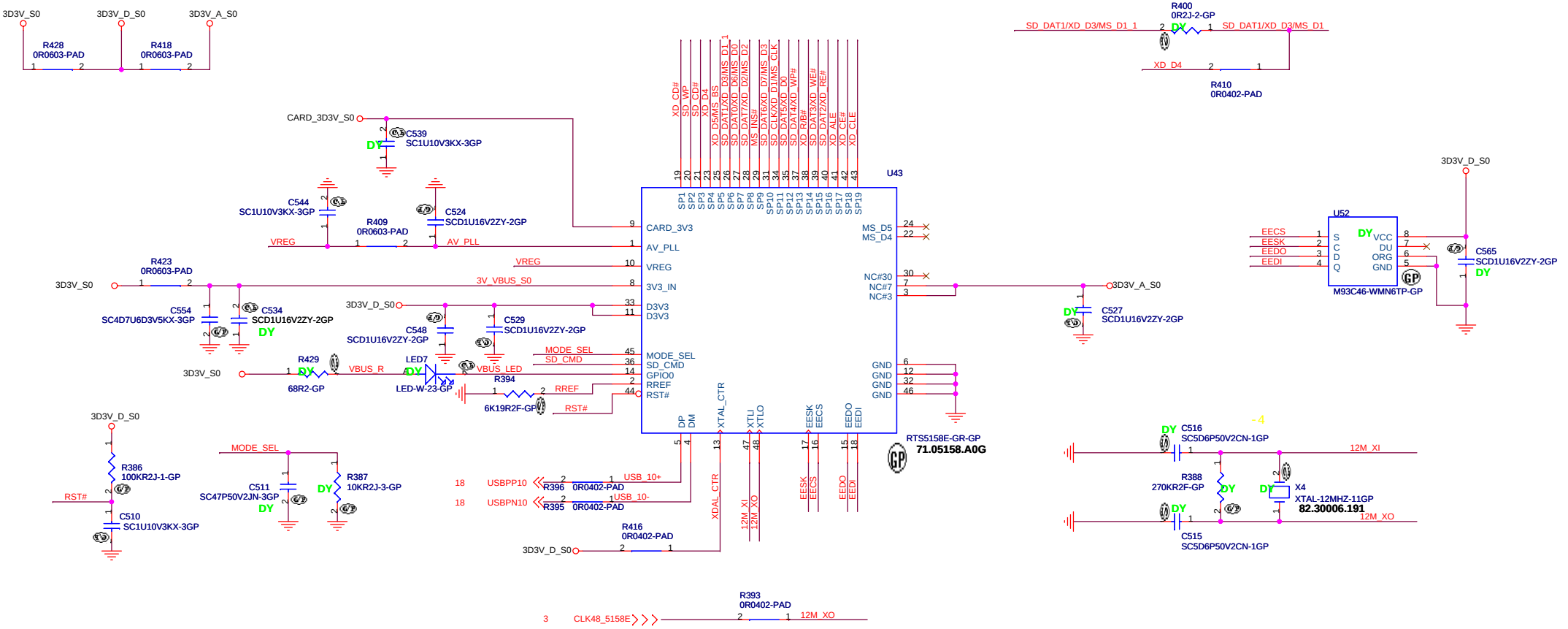
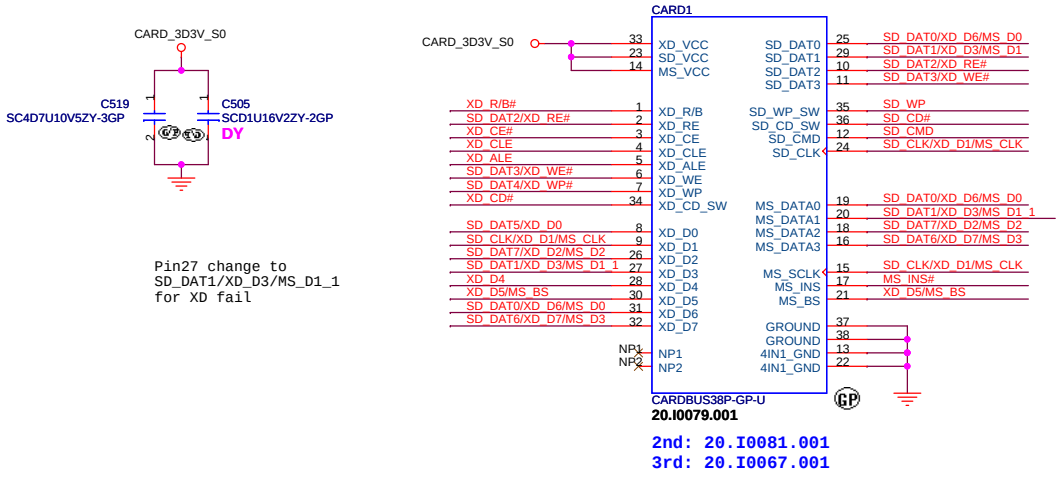


5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CARDREADER- RTS5158E

Size	Document Number	Rev
	Cathedral Peak II	SB

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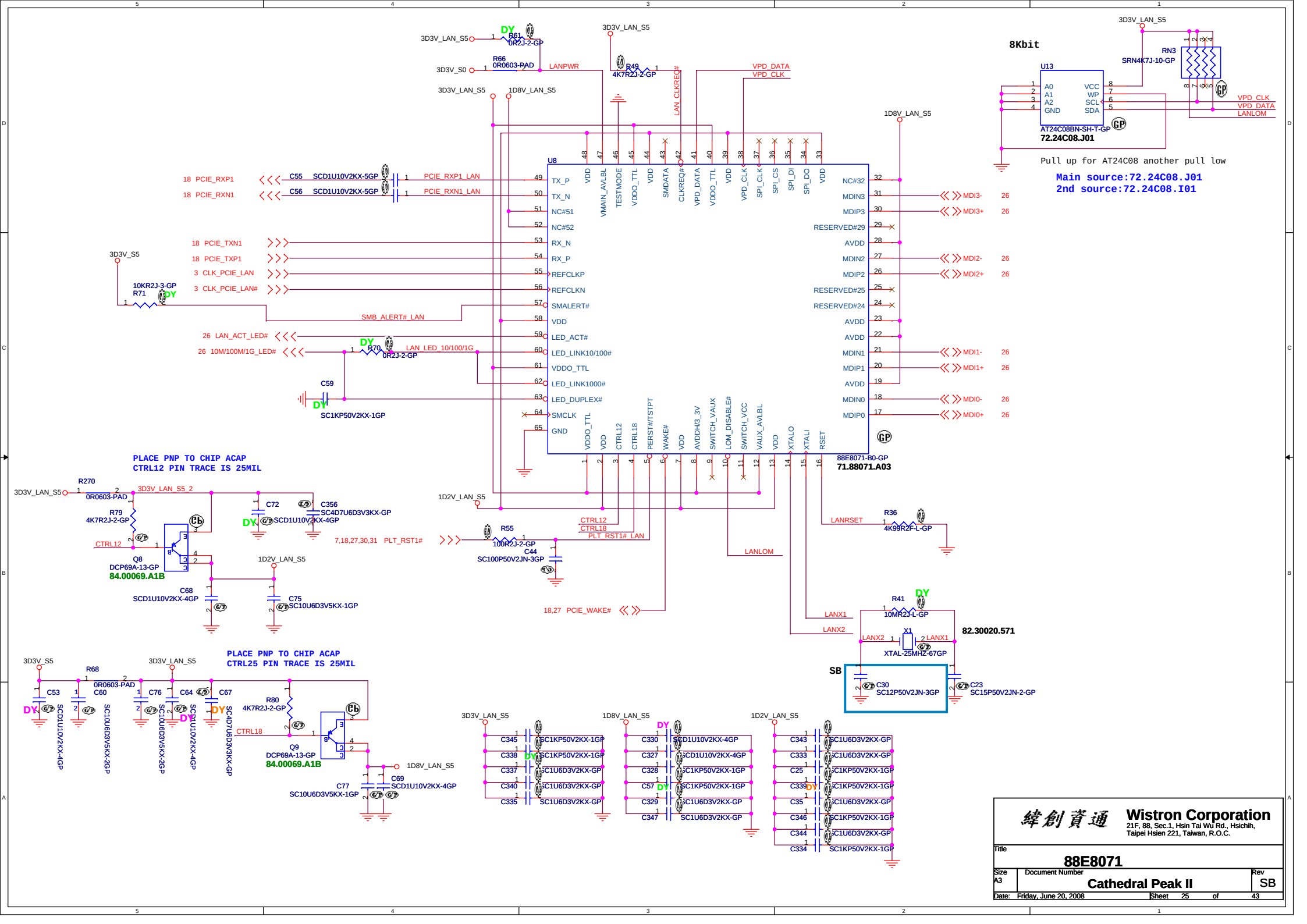
8Kbit
U13
AT24C08BN-SH-T-GP
72.24C08.J01
Pull up for AT24C08 another pull low
Main source:72.24C08.J01
2nd source:72.24C08.I01
U8
88E8071-B0-GP
71.88071.A03
PLACE PNP TO CHIP ACAP
CTRL12 PIN TRACE IS 25MIL
PLACE PNP TO CHIP ACAP
CTRL25 PIN TRACE IS 25MIL
82.30020.571
SB
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
88E8071
Size A3
Document Number
Cathedral Peak II
Rev SB
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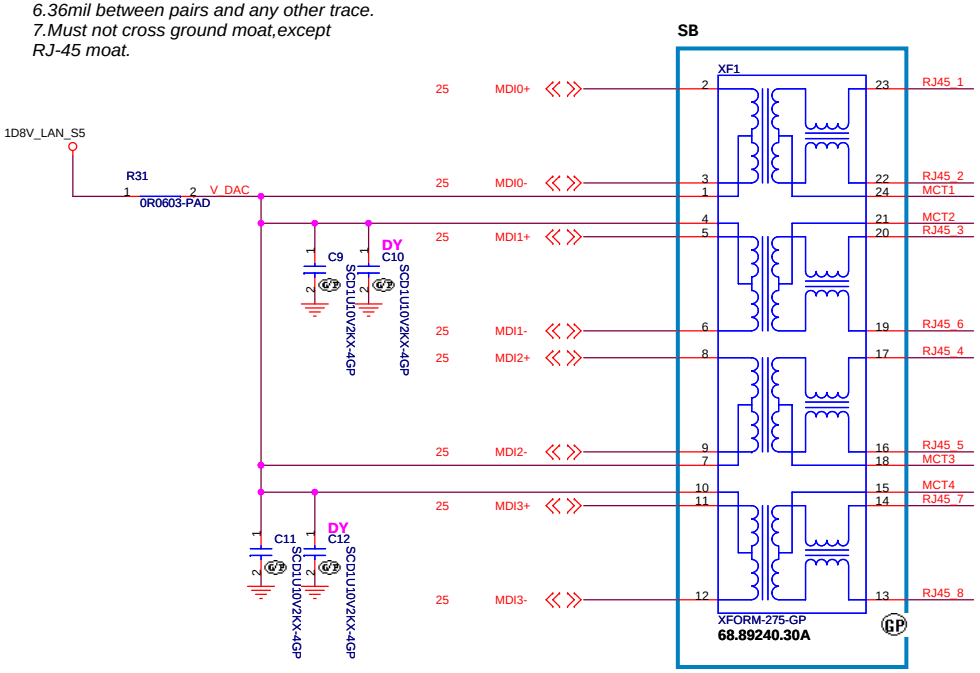
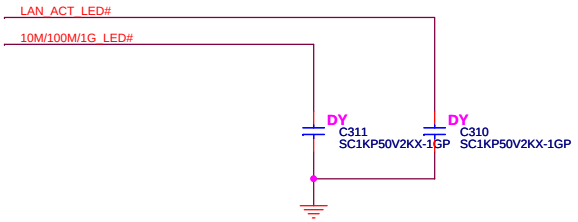
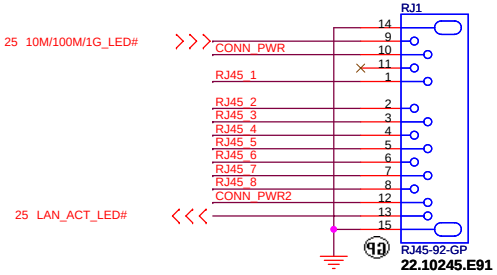
LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.





LAN Connector

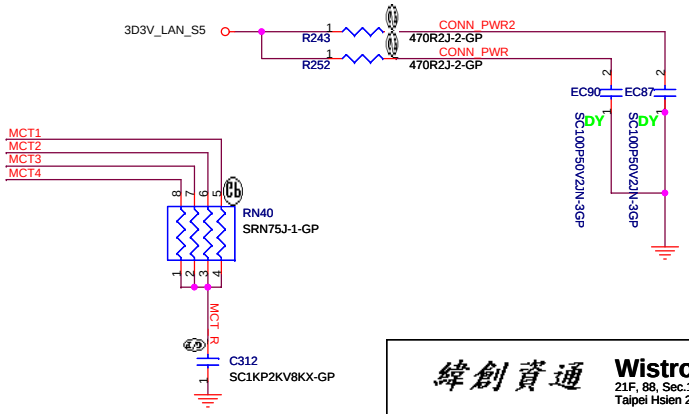


9:GREEN
13:Orange

LAN Link: Green(9), behavior is the same for 10/100/1000 bits

LAN Data: Yellow(13), when LAN is transfering data.

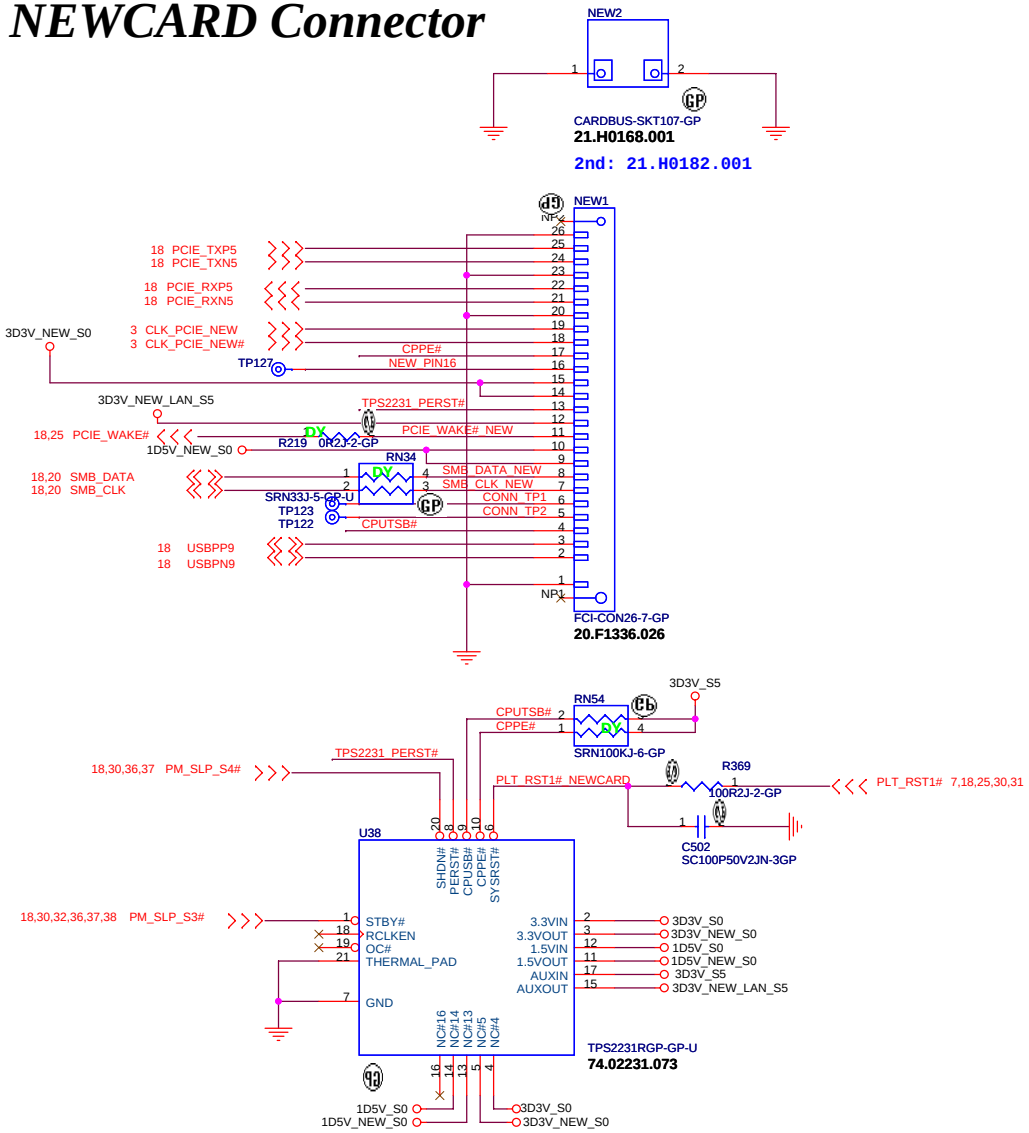
DOC_TIP,DOC_RING,TIP,RING:
W/S : 10/100 @ Surface layers
10/20 @ Inner layers



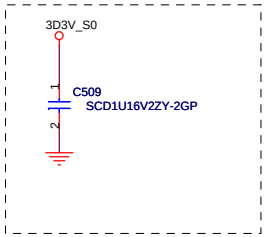
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN CONN**		
Size: A3	Document Number: **Cathedral Peak II**	Rev: SB
Date: Friday, June 20, 2008	Sheet 26 of 43	

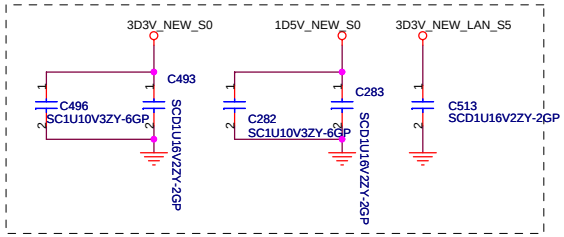
NEWCARD Connector



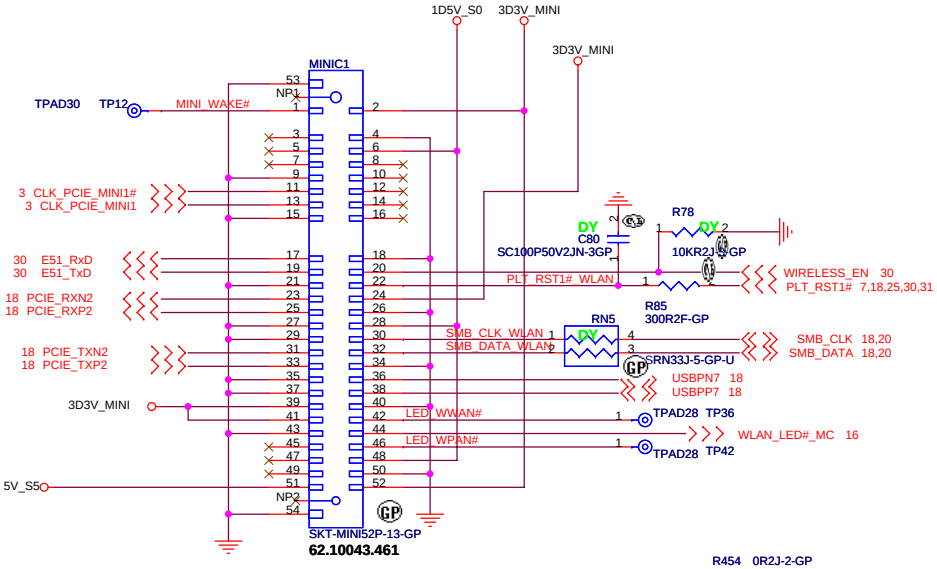
Place them Near to Chip

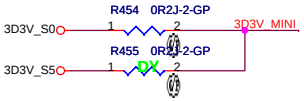


Place them Near to Connector

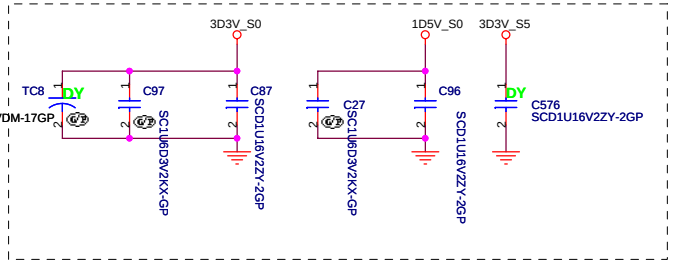


Mini Card Connector(WLAN)

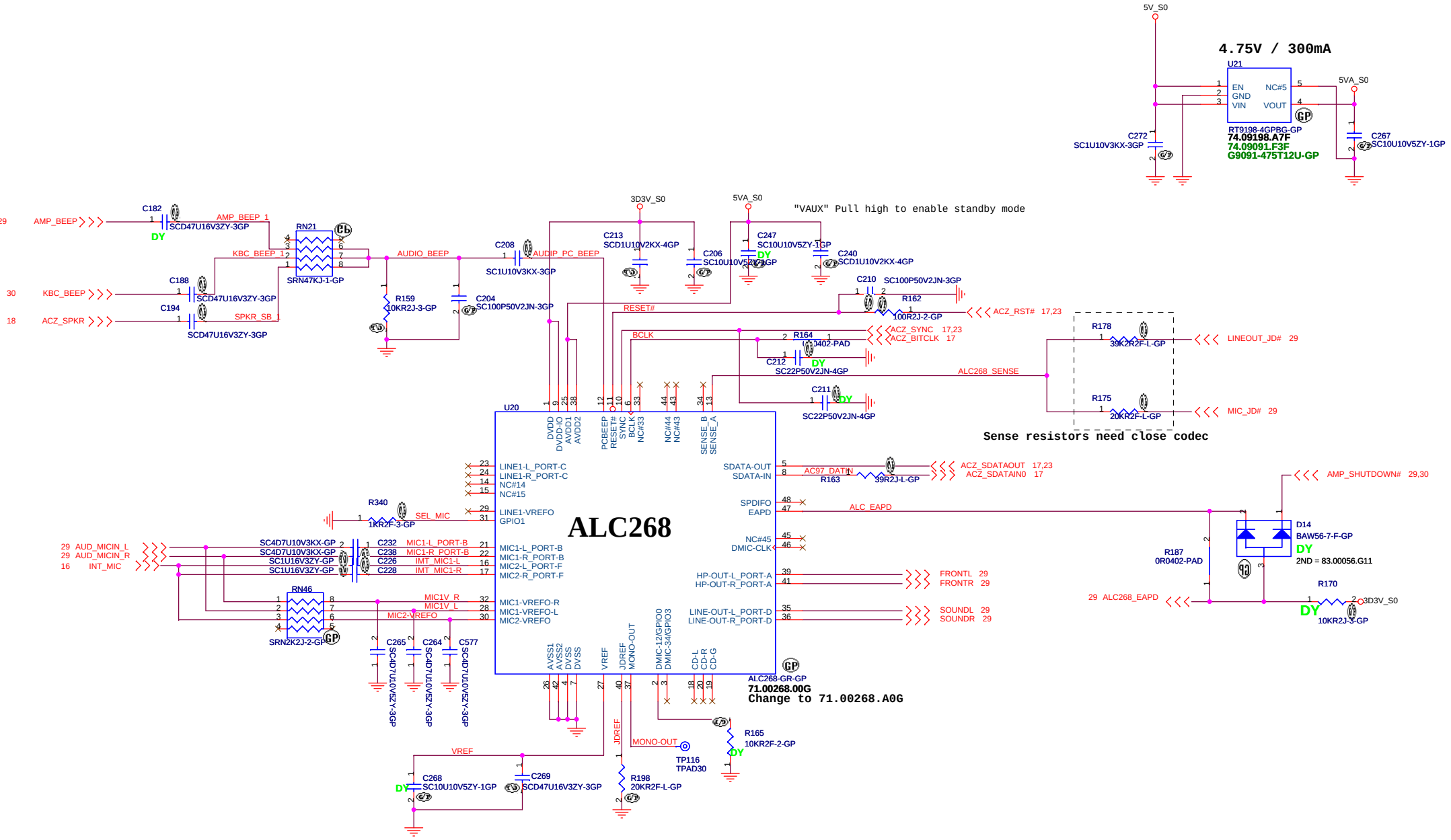




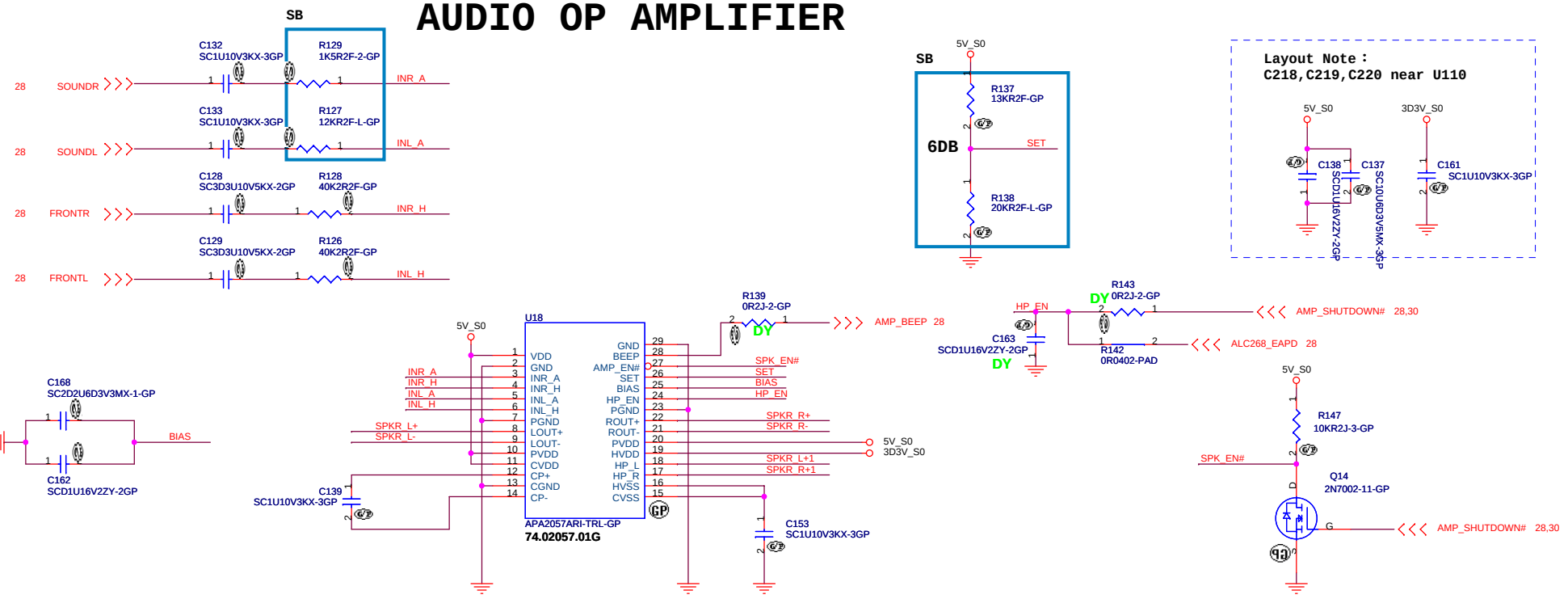
Place near MINIC1



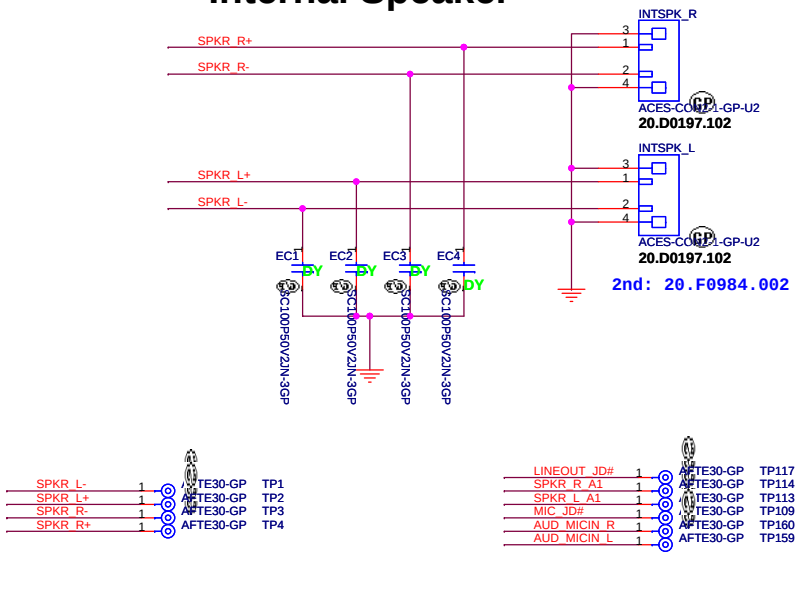
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**NEW CARD/MINI CARD**	
Size	Document Number **Cathedral Peak II**	Rev SB
Date: Friday, June 20, 2008	Sheet 27 of 43	


4.75V / 300mA
U21
RT9198-4GPBG-GP
74.09198.A7F
74.09091.F3F
G9091-475T12U-GP
"VAUX" Pull high to enable standby mode
Sense resistors need close codec
U20
ALC268
ALC268-GR-GP
71.00268.00G
Change to 71.00268.A0G
D14
BAW56-7-F-GP
2ND = 83.00056.G11
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Azalia codec ALC268
Cathedral Peak II
Friday, June 20, 2008

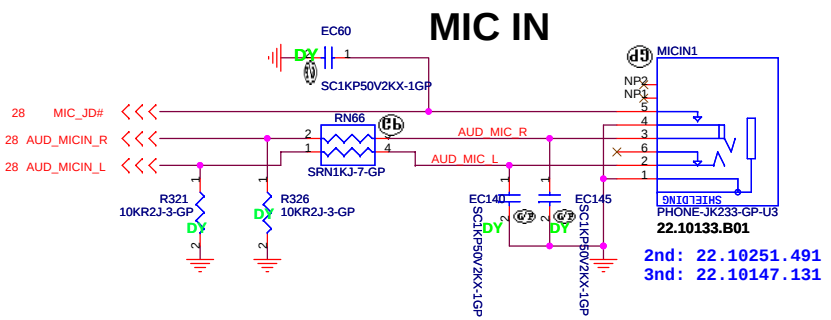
AUDIO OP AMPLIFIER



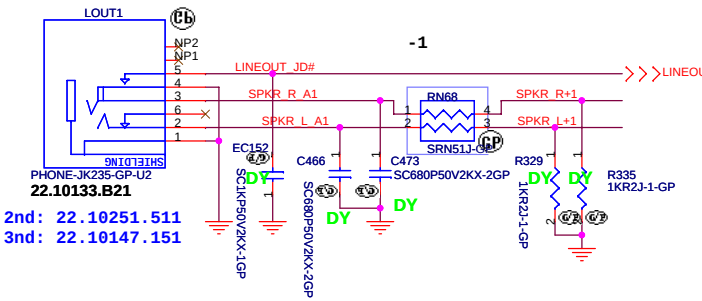
Internal Speaker



MIC IN

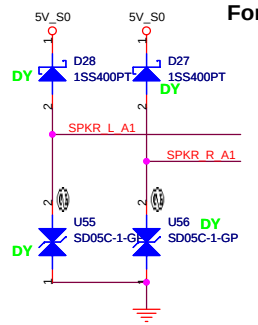


LINE OUT



Analog Int. Mic

remove to LED Board



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO AMP AND JACK		
Size	Document Number: Cathedral Peak II	Rev: SB
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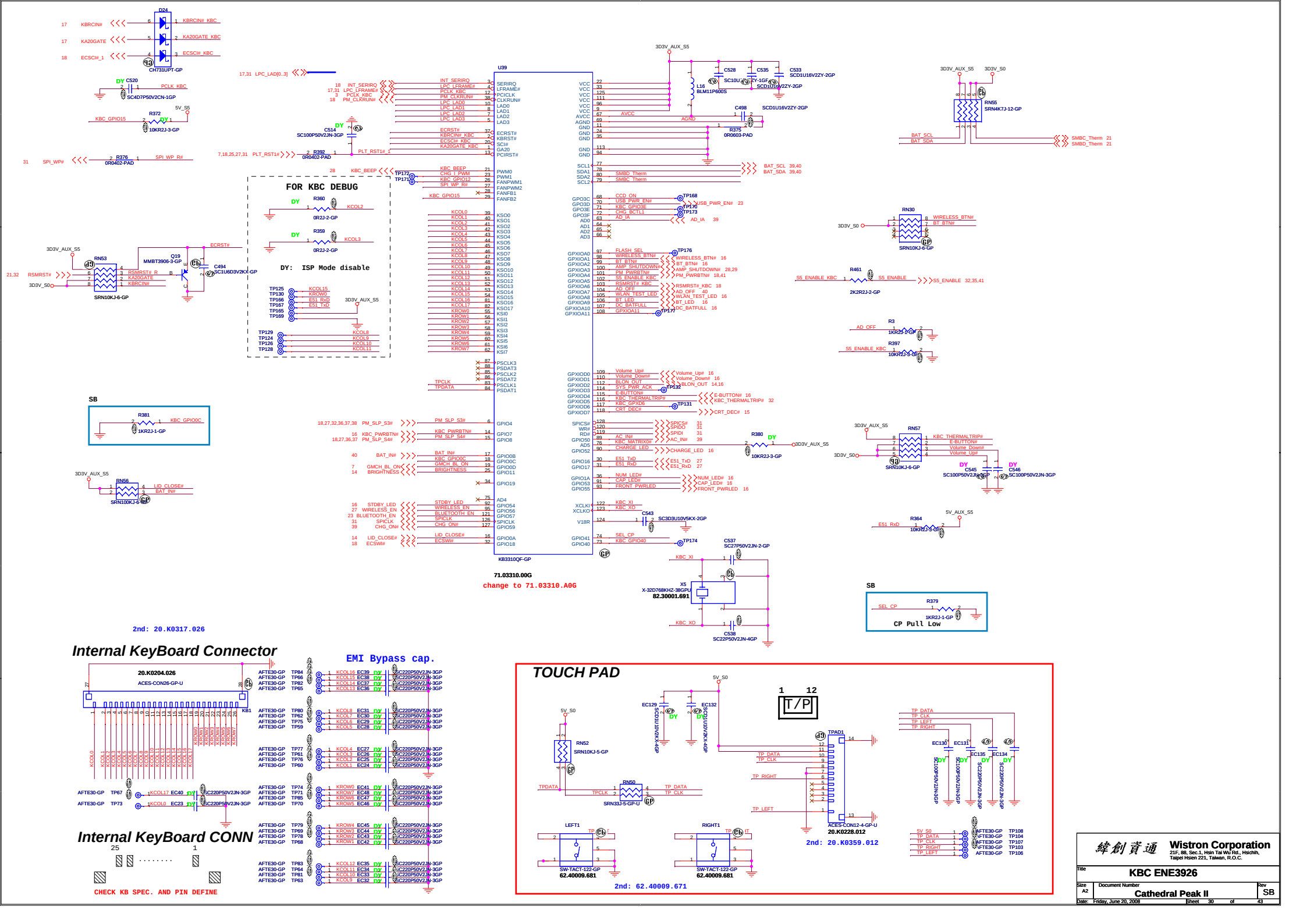
U39
KB3310QF-GP
71.03310.00G
change to 71.03310.A0G
FOR KBC DEBUG
DY: ISP Mode disable
SB
CP Pull Low
2nd: 20.K0317.026
Internal KeyBoard Connector
20.K0204.026
ACES-CON26-GP-U
EMI Bypass cap.
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
TOUCH PAD
T/P
ACES-CON12-4-GP-U
20.K0228.012
2nd: 20.K0359.012
2nd: 62.40009.671
62.40009.681
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC ENE3926
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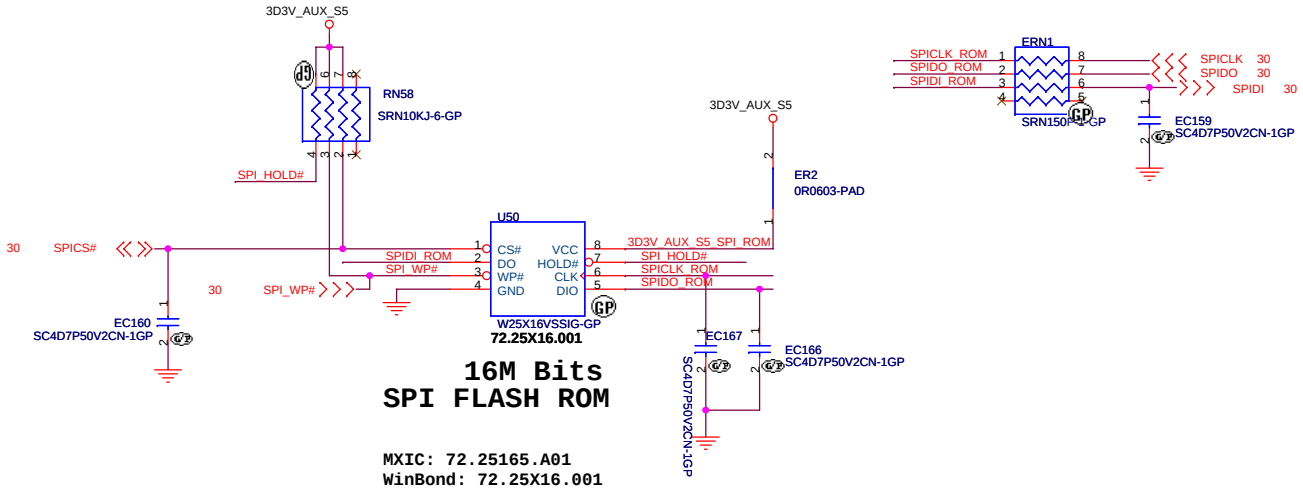
30
43



16M Bits
SPI FLASH ROM

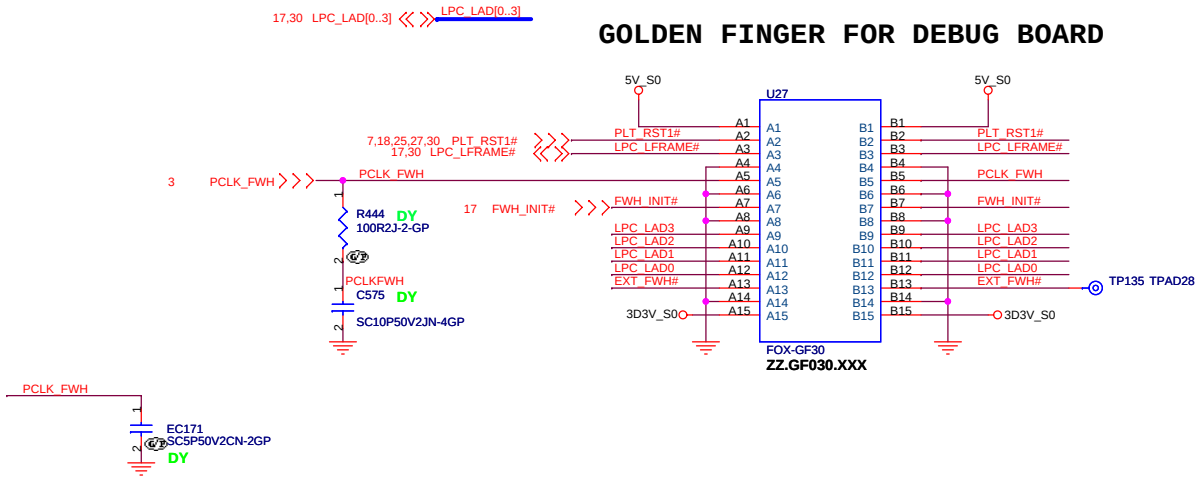
MXIC: 72.25165.A01
WinBond: 72.25X16.001

TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

GOLDEN FINGER FOR DEBUG BOARD



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**BIOS/GOLDEN FINGER**	
Size	Document Number **Cathedral Peak II**	Rev SB
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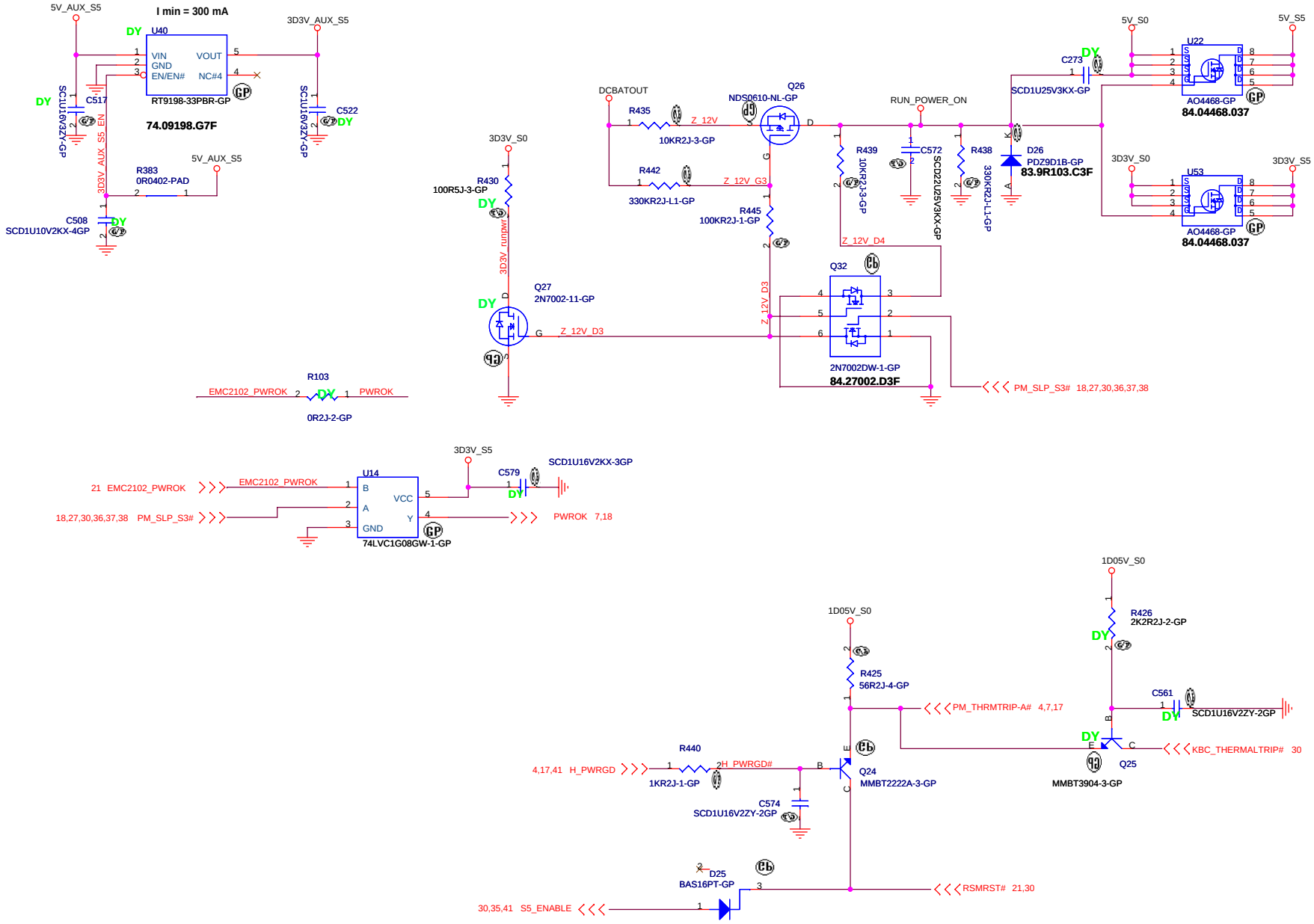
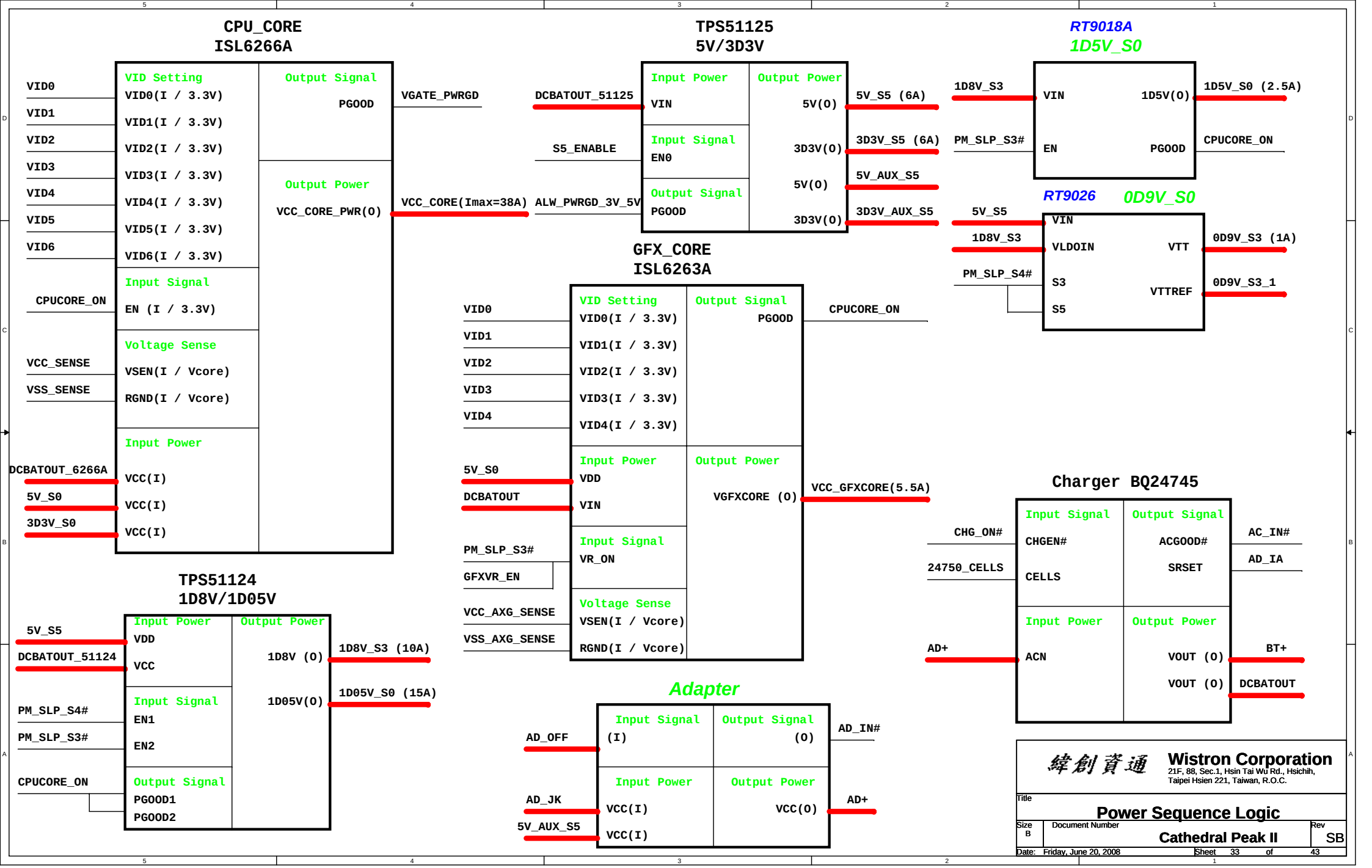
Aux Power 3D3V_AUX_S5

Run Power



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: RUN POWER and 3D3V_AUX_S5		
Size	Document Number: Cathedral Peak II	Rev: SB
Date: Friday, June 20, 2008	Sheet 32 of 43	


CPU_CORE
ISL6266A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)
VID6(I / 3.3V)
Input Signal
EN (I / 3.3V)
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Input Power
VCC(I)
VCC(I)
VCC(I)
Output Signal
PGOOD
Output Power
VCC_CORE_PWR(O)
VID0
VID1
VID2
VID3
VID4
VID5
VID6
CPUCORE_ON
VCC_SENSE
VSS_SENSE
DCBATOUT_6266A
5V_S0
3D3V_S0
VGATE_PWRGD
VCC_CORE(Imax=38A)
TPS51125
5V/3D3V
Input Power
VIN
Input Signal
EN0
Output Signal
PGOOD
Output Power
5V(O)
3D3V(O)
5V(O)
3D3V(O)
DCBATOUT_51125
S5_ENABLE
ALW_PWRGD_3V_5V
5V_S5 (6A)
3D3V_S5 (6A)
5V_AUX_S5
3D3V_AUX_S5
RT9018A
1D5V_S0
VIN
EN
1D5V(O)
PGOOD
1D8V_S3
PM_SLP_S3#
1D5V_S0 (2.5A)
CPUCORE_ON
RT9026
0D9V_S0
VIN
VLDOIN
S3
S5
VTT
VTTREF
5V_S5
1D8V_S3
PM_SLP_S4#
0D9V_S3 (1A)
0D9V_S3_1
GFX_CORE
ISL6263A
VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
Input Power
VDD
VIN
Input Signal
VR_ON
Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)
Output Signal
PGOOD
Output Power
VGFXCORE (O)
VID0
VID1
VID2
VID3
VID4
5V_S0
DCBATOUT
PM_SLP_S3#
GFXVR_EN
VCC_AXG_SENSE
VSS_AXG_SENSE
CPUCORE_ON
VCC_GFXCORE(5.5A)
Charger BQ24745
Input Signal
CHGEN#
CELLS
Input Power
ACN
Output Signal
ACGOOD#
SRSET
Output Power
VOUT (O)
VOUT (O)
CHG_ON#
24750_CELLS
AD+
AC_IN#
AD_IA
BT+
DCBATOUT
TPS51124
1D8V/1D05V
Input Power
VDD
VCC
Input Signal
EN1
EN2
Output Signal
PGOOD1
PGOOD2
Output Power
1D8V (O)
1D05V(O)
5V_S5
DCBATOUT_51124
PM_SLP_S4#
PM_SLP_S3#
CPUCORE_ON
1D8V_S3 (10A)
1D05V_S0 (15A)
Adapter
Input Signal
(I)
Input Power
VCC(I)
VCC(I)
Output Signal
(O)
Output Power
VCC(O)
AD_OFF
AD_JK
5V_AUX_S5
AD_IN#
AD+
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Power Sequence Logic
Size
B
Document Number
Cathedral Peak II
Rev
SB
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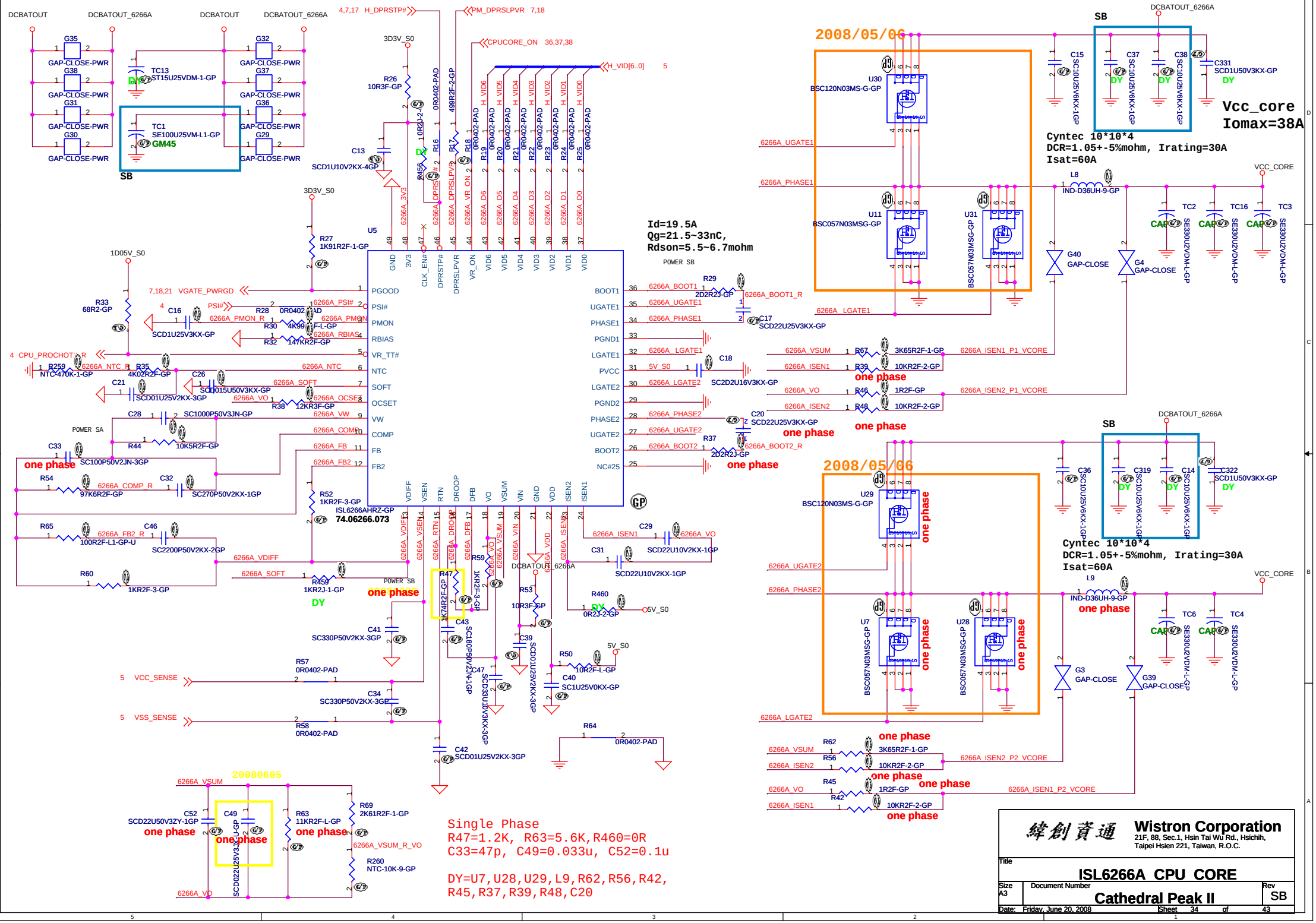
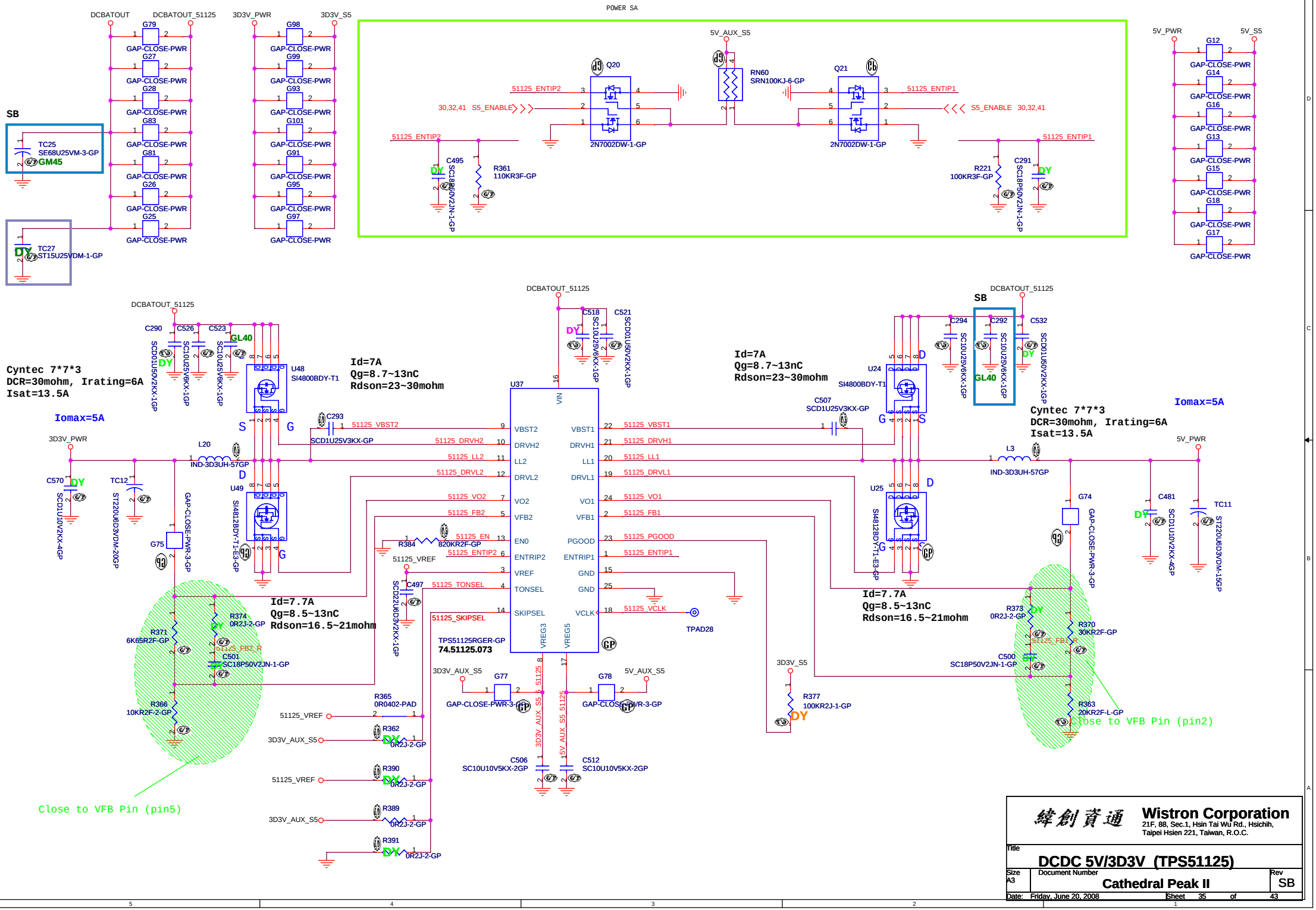

U5
ISL6266AHRZ-GP
74.06266.073
2008/05/06
U30
U11
U31
U29
U7
U28
SB
Vcc_core
Iomax=38A
Cyntec 10*10*4
DCR=1.05+-5%mohm, Irating=30A
Isat=60A
Id=19.5A
Qg=21.5~33nC,
Rdson=5.5~6.7mohm
one phase
DY
20080605
Single Phase
R47=1.2K, R63=5.6K,R460=0R
C33=47p, C49=0.033u, C52=0.1u
DY=U7,U28,U29,L9,R62,R56,R42,
R45,R37,R39,R48,C20
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6266A CPU CORE
Cathedral Peak II
Friday, June 20, 2008
Sheet 34 of 43



緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DCDC 5V/3D3V (TPS51125)**

Size	Document Number	Rev
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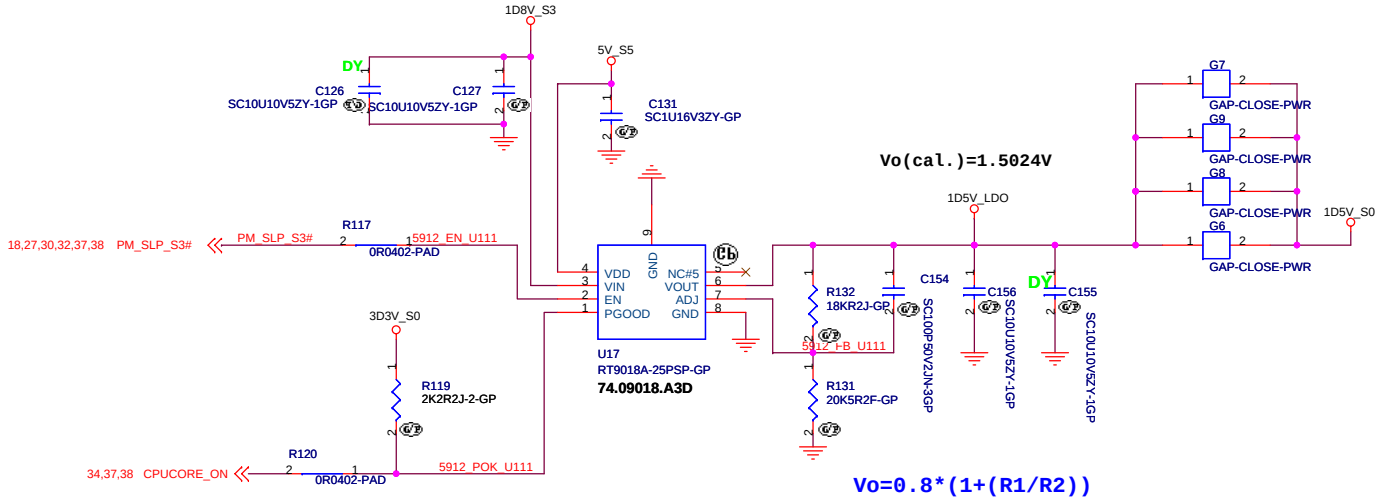
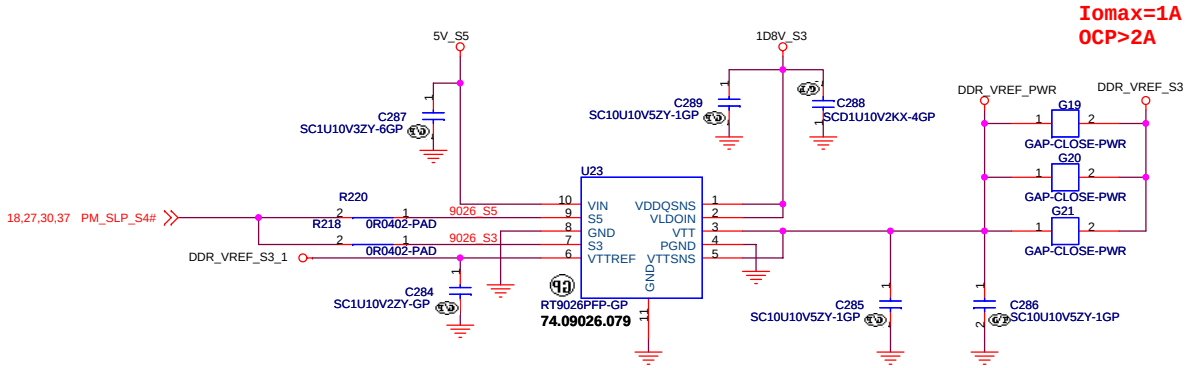
1D5V_S0
Iomax=2.5A





緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 1D5V & 0D9V		
Size: A3	Document Number: Cathedral Peak II	Rev: SB
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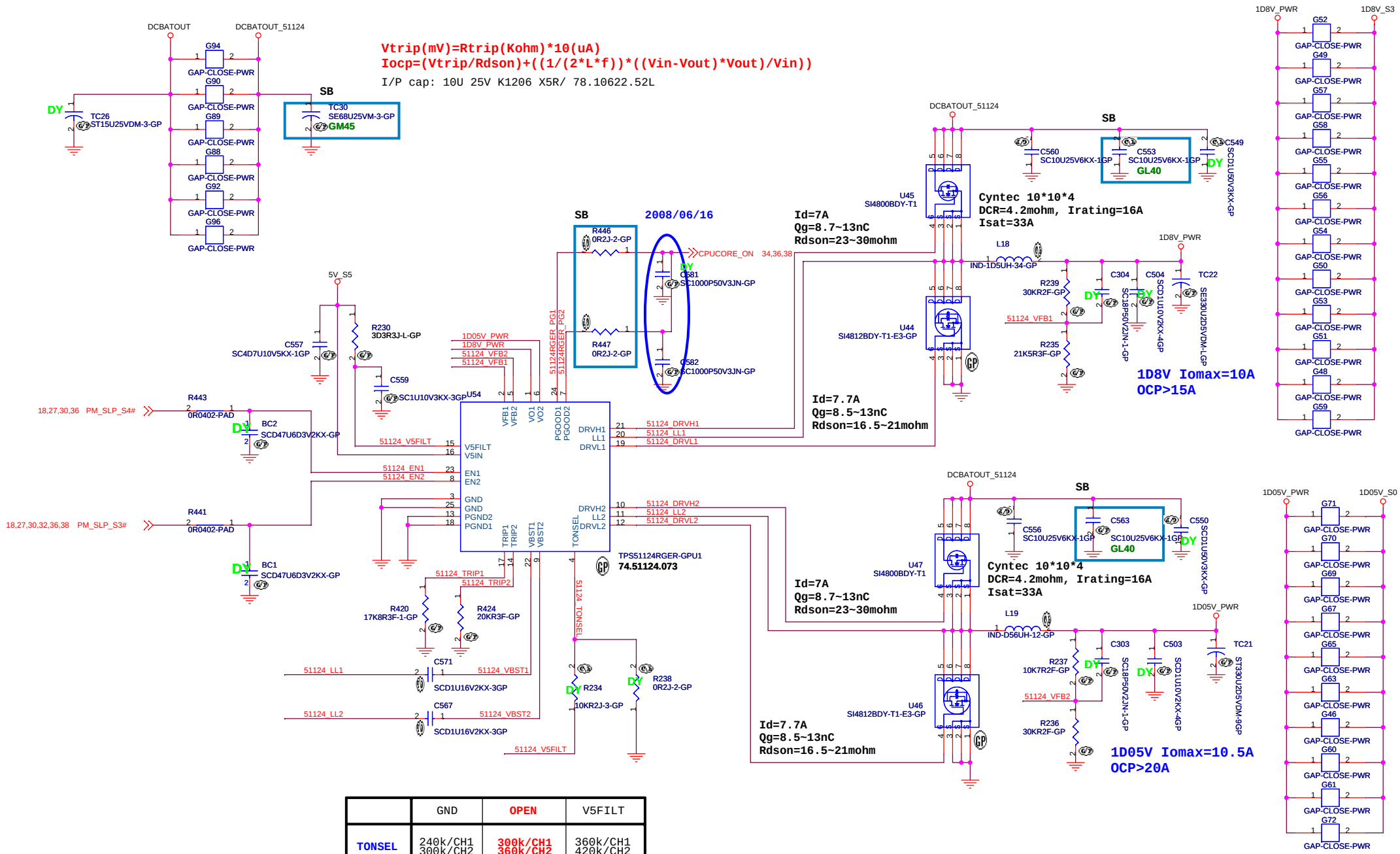
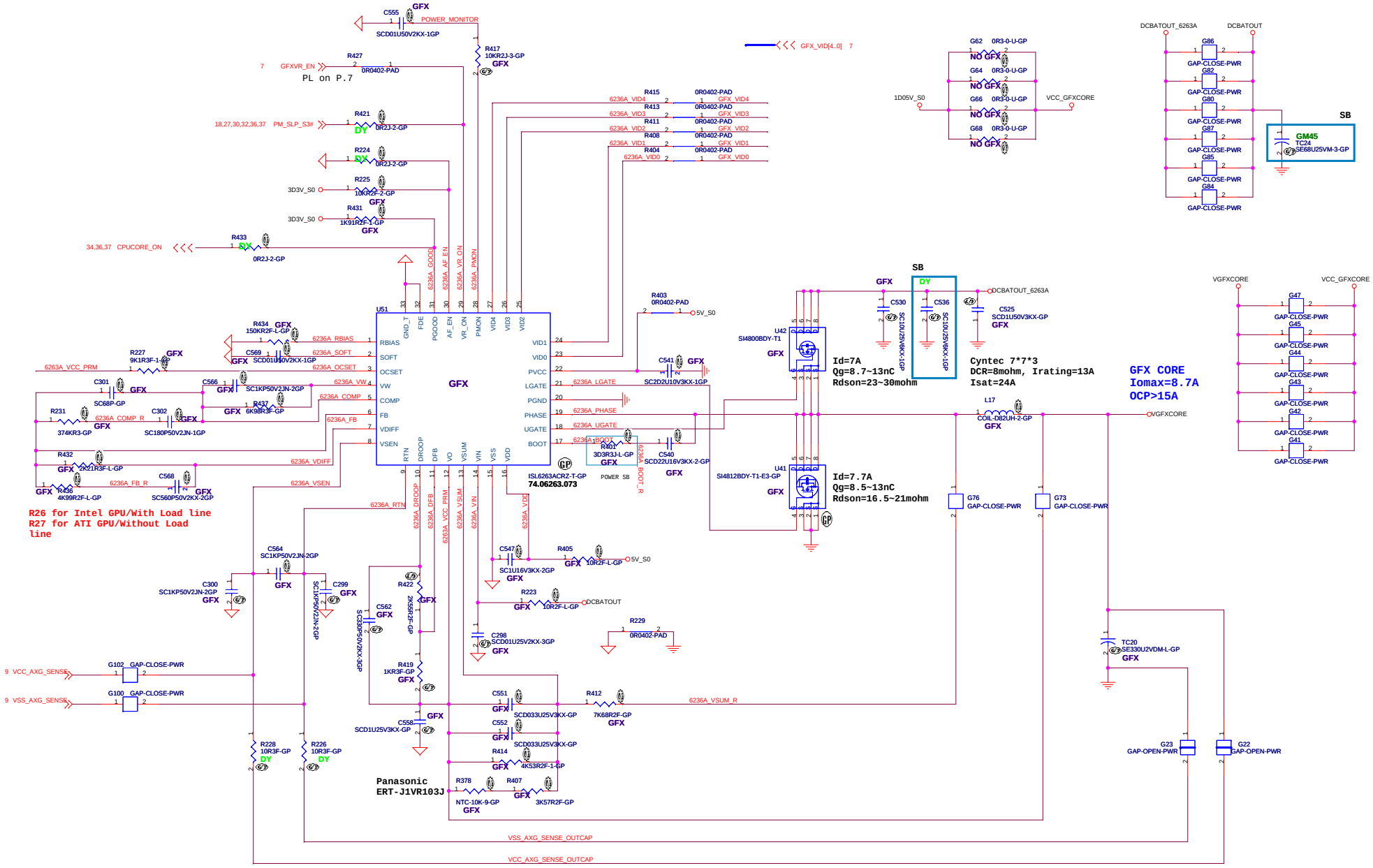


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2



Cathedral Peak II

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6263A_GFX CORE

Size: C | Document Number: Cathedral Peak II | Rev: SB

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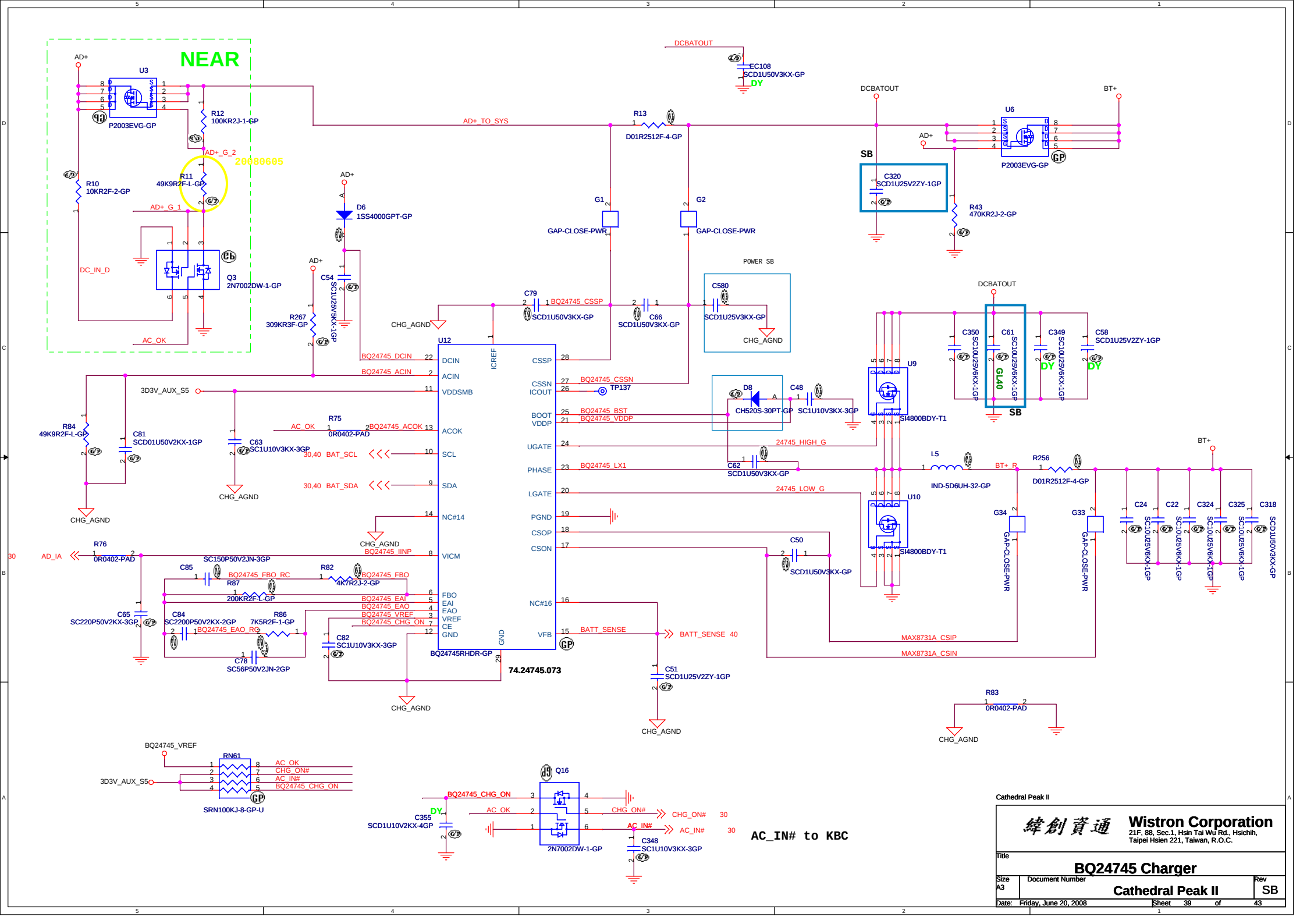

Cathedral Peak II

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **BQ24745 Charger**

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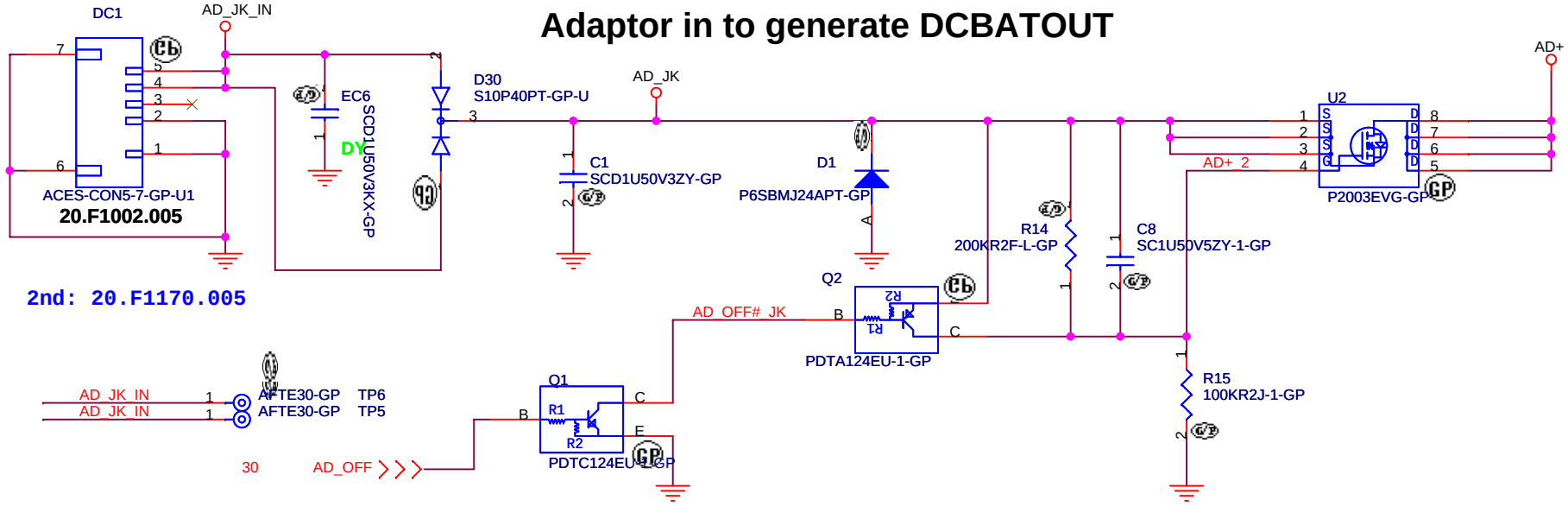
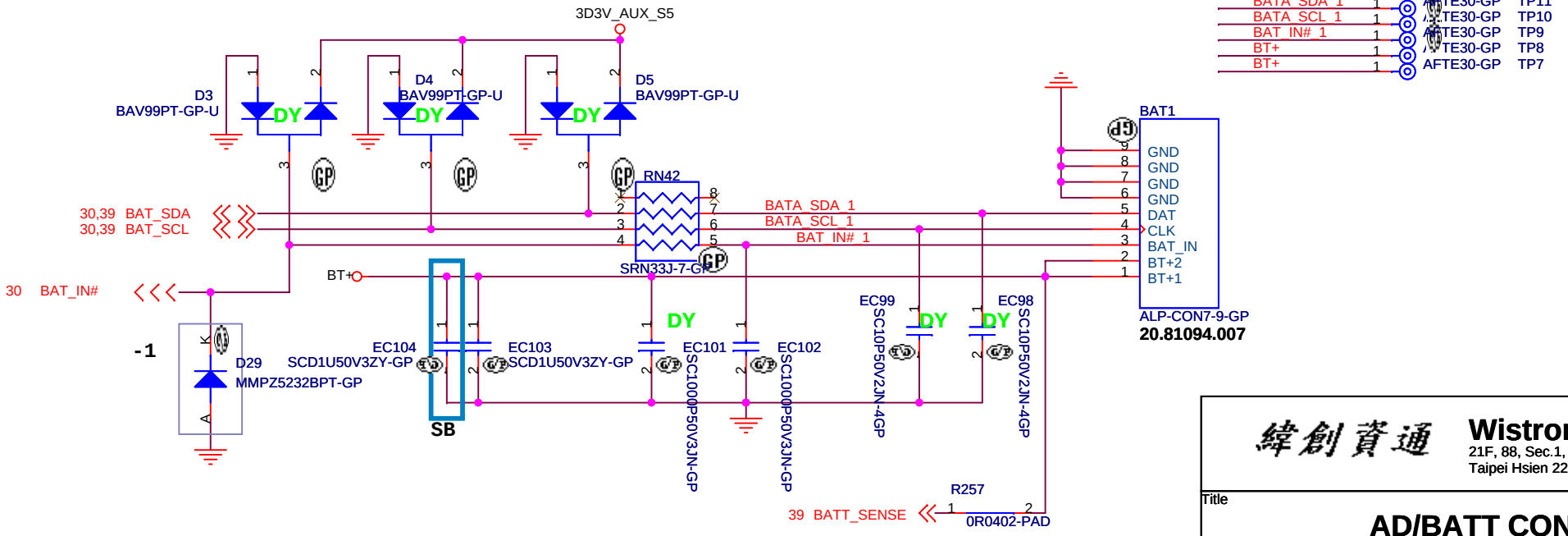
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD/BATT CONN**

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	Cathedral Peak II	SB

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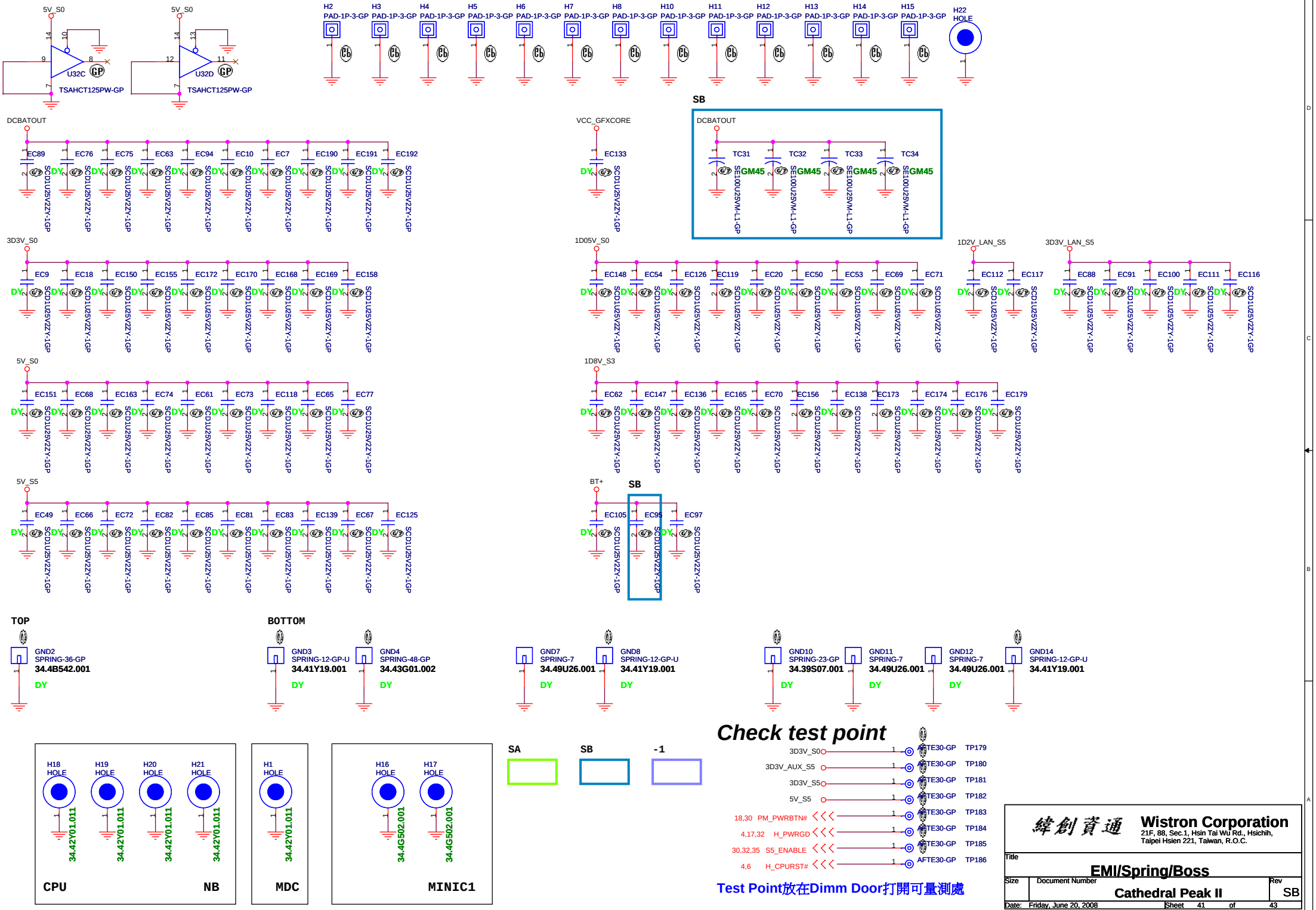
5V_S0
U32C
GP
TSAHCT125PW-GP
5V_S0
U32D
GP
TSAHCT125PW-GP
H2 PAD-1P-3-GP
H3 PAD-1P-3-GP
H4 PAD-1P-3-GP
H5 PAD-1P-3-GP
H6 PAD-1P-3-GP
H7 PAD-1P-3-GP
H8 PAD-1P-3-GP
H10 PAD-1P-3-GP
H11 PAD-1P-3-GP
H12 PAD-1P-3-GP
H13 PAD-1P-3-GP
H14 PAD-1P-3-GP
H15 PAD-1P-3-GP
H22 HOLE
DCBATOUT
EC89 EC76 EC75 EC63 EC94 EC10 EC7 EC190 EC191 EC192
SCD1U25V2ZY-1GP
SB
DCBATOUT
TC31 TC32 TC33 TC34
SE100U2SVM-L1-GP
GM45
VCC_GFXCORE
EC133
3D3V_S0
EC9 EC18 EC150 EC155 EC172 EC170 EC168 EC169 EC158
1D05V_S0
EC148 EC54 EC126 EC119 EC20 EC50 EC53 EC69 EC71
1D2V_LAN_S5
EC112 EC117
3D3V_LAN_S5
EC88 EC91 EC100 EC111 EC116
5V_S0
EC151 EC68 EC163 EC74 EC61 EC73 EC118 EC65 EC77
1D8V_S3
EC62 EC147 EC136 EC165 EC70 EC156 EC138 EC173 EC174 EC176 EC179
5V_S5
EC49 EC66 EC72 EC82 EC85 EC81 EC83 EC139 EC67 EC125
BT+
SB
EC105 EC95 EC97
TOP
GND2
SPRING-36-GP
34.4B542.001
DY
BOTTOM
GND3
SPRING-12-GP-U
34.41Y19.001
DY
GND4
SPRING-48-GP
34.43G01.002
DY
GND7
SPRING-7
34.49U26.001
DY
GND8
SPRING-12-GP-U
34.41Y19.001
DY
GND10
SPRING-23-GP
34.39S07.001
DY
GND11
SPRING-7
34.49U26.001
DY
GND12
SPRING-7
34.49U26.001
DY
GND14
SPRING-12-GP-U
34.41Y19.001
DY
H18 HOLE
H19 HOLE
H20 HOLE
H21 HOLE
34.42Y01.011
CPU
NB
H1 HOLE
34.42Y01.011
MDC
H16 HOLE
H17 HOLE
34.4G502.001
MINIC1
SA
SB
-1
Check test point
3D3V_S0
3D3V_AUX_S5
3D3V_S5
5V_S5
18,30 PM_PWRBTN#
4,17,32 H_PWRGD
30,32,35 S5_ENABLE
4,6 H_CPURST#
AFTE30-GP
TP179
TP180
TP181
TP182
TP183
TP184
TP185
TP186
Test Point放在Dimm Door打開可量測處
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
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SA to SB
1.No Power.
change KBC to BO (71.03310.A0G)
2.XD Card function fail
Cut CARD1 pin27. connect to R400 pin2
3.leakage
GFX power VDD connect to S0
4.Gain=8db.1.83W R137=16K.R138=30K
5.Int_MIC voice to small
add VREF C577=4.7U
6.Realtek Audio report
change R327=68 ohm.R333=68 ohm.merge to RN68
7.SIV reset
R140=300,R55=100.C44=100p,R398=0,R369=100.C502=100p,R85=300,R162=100.C210=100p,R392=0,
8.SIV Azalia
DY C542
BITCLK rise and fall time fail RN10 change to R453=22ohm(MDC).R452=0ohm(codec)
9.add MINICard power option for customer ask
R454.R455
10.interfere HDD
C390.C401.C419. change 0603 4.7U
11.power team
R38=12K.R47=2.74K .R361=110K.R221=100K.R237=10.7K .R424=20K.R420=17.8K .R227=10.5K
R48=10K.R29=2.2 .R37=2.2 .R401=3.3 .C49=0.1u.add R456.add C580.D8=83.R0203.08F .
TC11 change to 77.C2271.00L
TC9 change to 77.E9071.001 (power ripple)
add R458=1K.R459=1k.R460
12.Oscillation
C30=15p.C23=15P.C537=27p.C538=22p
13.audio S3.S4 resume bobo sound
R143 DY. R187 0ohm pad
14.AC mode have hight frequency noise
R390 DY.R389 0ohm pad
15.ESD issue
BAT_IN# series 33 ohm
RN42 change to 8p4r
add R457.D27.D28.D29.U55.U56.C578.R457.
16.noise
DY C523.TC25 change to 77.C1561.01L
20.LED brightness
R2.R1.R4.R5.R451.R450.R449.R448=56

EMI
1.EC23 ~~EC48.EC134.EC135.EC167.EC121.EC122.EC123.
2.EC89.EC12.EC8.EC119.EC156.EC173.
3.EC174~~~EC179.
4.GND13.GND14.

Merge
1.R313.R314.R315.R319.R320.R149. change to RN59
2.RN6.RN46. change to RN6
3.R341.R343.R344 change to RN46
4.R385 change to 100K merge R382 to RN56
5.RN53.RN56. change to RN53
6.Q20.Q21 change to Q21. Q21.Q23 change to Q21.
7.R367.R368 change to RN60
8.Q16.Q17 change to Q16
9.R262.R264.R268.R277 change to RN61
10.R205.R204.R206 change to RN62
11.RN33.R215 change to RN33
12.R209.R210.R348 change to RN63
13.R280=10K.merge R269 to RN64
14.R109.R112.R111.R290 change to RN65
15.R325.R323 change to RN66
16.R304.R307 change to RN67
17.U14 change to 73.01G08.L04 .add C579
18.R51.R399 vhange to RN69.

0 Ohm change to PAD
R427.R403.R415.R413.R411.R408.R404.R146.R197.R157.R153.R353.R352.R358.R357.R310.R196.R346.R342.R351.
R191.R203.L14.R212.R350.R179.R217.R6.R7.R242.R294.R278.R279.R292.R293.R232.R233.R410.R393.
R416.R250.R251.R248.R249.R246.R247.R244.R245.R129.R127.R376.ER2.R383.R28.R16.R19.R20.R21.
R22.R23.R24.R25.R57.R58.R365.R164.

05/05
Page16: merge LAUNCHCN1 LEDCN1 to LAUNCHCN1 15pins

Page15: change CRT1 from 20.20717.015 to 20.20378.015

Page26: change RJ1 from 22.10277.011 to 22.10245.E91

Page23: change BLUE1 from 20.D0197.004 to 20.F0984.004

Page24: change CARD1 from 20.I0081.001 to 20.I0067.001

Page21: change FAN1 from 20.F0714.003 to 20.F1000.003

Page27: change MINIC1 from 20.F1049.052 to 62.10043.331

Page30: change TPAD1 from 20.K0286.012 to 20.K0174.012

Page34: change U29 U30 from 84.07686.037 to 84.12003.A37 and change U7 U11 U28 U31 from 84.04634.037 to 84.57N03.A37

Page16: delete LED1 LED2 R1 R2 R4 R5

05/07
Page17: change RTC1 from 62.70001.011 to 20.F0700.003

Page41: delete EC51

Page10: delete C159

Page25: change U13 from 72.24256.R01 to 72.24C08.J01

05/08
Page30: change KB1 from 20.K0127.026 to 20.K0204.026

Page26: delete RN36 RN37 RN38 RN39

Page23: change TC28 from 80.15715.34L to 77.C1071.081

Page26: change TC15 from 80.15715.34L to 80.15715.12L

Page23: delete R244 R245 R246 R247 R248 R249 R250 R251

Page24: change CARD1 from 20.0067.001 to 20.I0079.001

05/09
Page41: delete GND13

05/12
Page24: add EC127 EC128 EC185 EC186

Page35: change TC27 from 77.C1561.01L to 77.C1561.03L

Page40: change BAT1 from 20.80697.007 to 20.80906.007

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05/013
Page16: change pin1 pin2 of LED6 from 3D3V_S5 to 3D3V_AUX_S5

05/014
Page17: add EC187 EC188

Page16: add EC189 TP189~TP195

Page30: change TPAD1 from 20.K0174.012 to 20.K0228.012

Page41: add EC190~EC195

05/015
Page17: change U15 pin13 pin14 from pull high 3D3V_S0 to VGATE_PWRGD

Page17: change Q11 G from 3D3V_S0 to VGATE_PWRGD

Page40: change D1 from 83.P4SSM.BAM to 83.P6SBM.AAG

SB
05/015
Page30: change KBC_GPIO0C from pull-high 3D3V_AUX_S5 with 10K to pull-low GND with 1K

06/06
Page3: change C176 C177 from 78.27034.1FL (27p) to 78.33034.1FL (33p)

Page22: delete D15

Page29: change R127 R129 from 0ohm pad to 12K 1K5 and change R137 R138 from 16K 30K to 13K 20K

Page34: change TC1 from 77.C1561.01L (15u) to 79.10712.L02 (100u) and C14 C37 C38 C319 dummy

Page35: change TC25 from 77.C1561.01L (15u) to 79.68612.30L (68u) and change C292 to dummy

Page37: add TC30 79.68612.30L (68u) and change C553 C563 to dummy

Page38: change C536 to dummy and change TC24 from 77.C1561.01L (15u) to 79.68612.30L (68u)

Page39: change C61 to dummy

Page41: add TC31 TC32 TC33 TC34 and delete GND9

06/09
Page16: add LED3 R458 R465

06/11
Page30: change R379 from 10K to 1K

06/13
Page3: add EC59 DY

06/13
Page37: change R446 R447 from 0ohm pad to 0ohm resistor

Page26: change XF1 from 68.69241.301 to 68.89240.30A

06/17
Page39: C320 mount

Page40: EC104 mount

Page41: EC95 mount

Page39: change R11 from 10K to 49K9

Page34: change C49 from 47nF to 22nF and change R47 from 2.74K to 1.74K

Page37: add C581 C582

Page41: delete GND6

06/20
Page25: change C30 from 15p to 12p

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