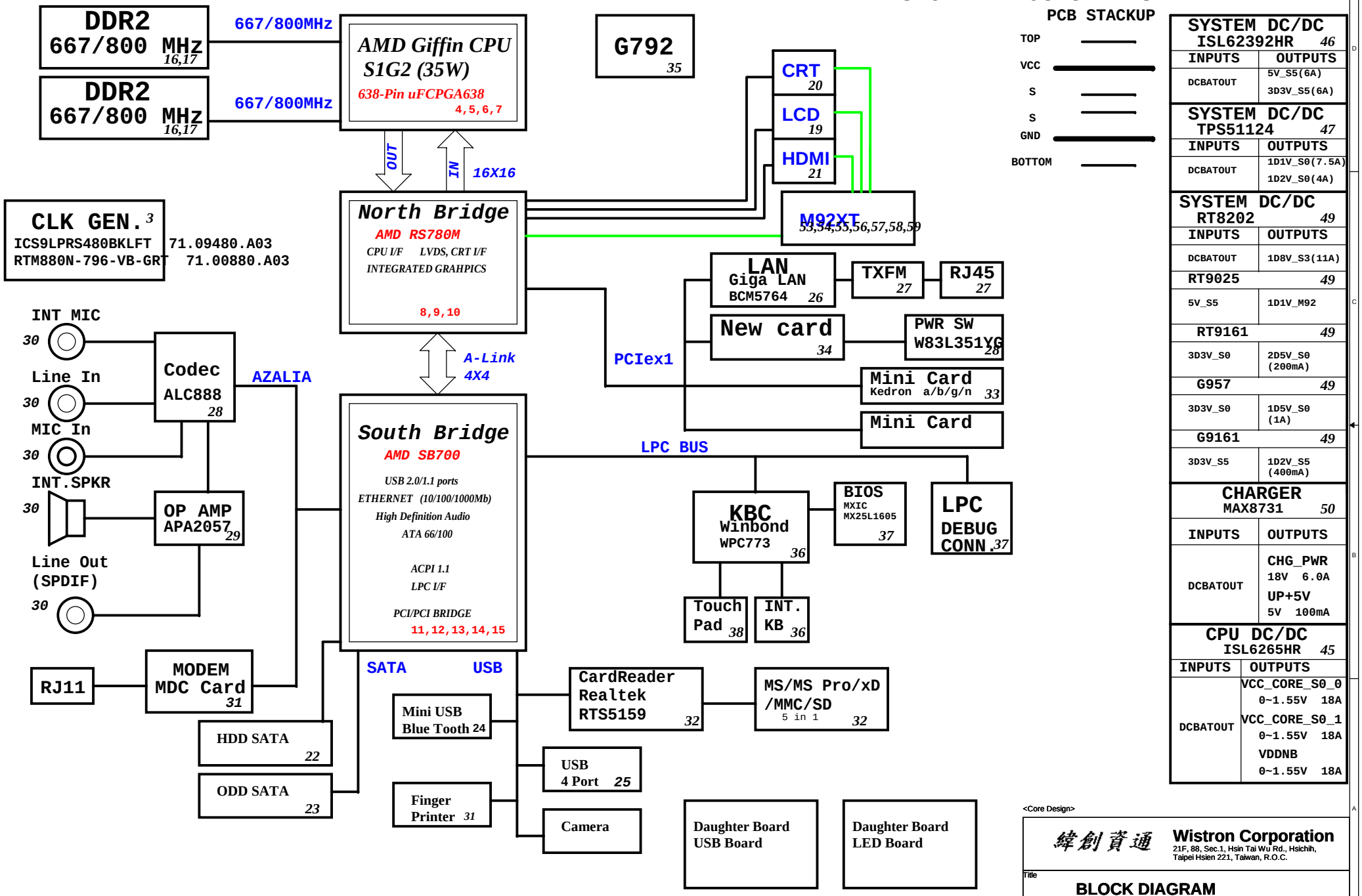
JV50-PU Block Diagram

Project code: 91.4CH01.001
PCB P/N : 48.4C901.001
REVISION :08252- -SB



PCB STACKUP

TOP	
VCC	
S	
S	
GND	
BOTTOM	

SYSTEM DC/DC ISL62392HR 46	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(6A)

SYSTEM DC/DC TPS51124 47	
INPUTS	OUTPUTS
DCBATOUT	1D1V_S0(7.5A) 1D2V_S0(4A)

SYSTEM DC/DC RT8202 49	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3(11A)
RT9025 49	
5V_S5	1D1V_M92
RT9161 49	
3D3V_S0	2D5V_S0 (200mA)
G957 49	
3D3V_S0	1D5V_S0 (1A)
G9161 49	
3D3V_S5	1D2V_S5 (400mA)

CHARGER MAX8731 50	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 6.0A UP+5V 5V 100mA

CPU DC/DC ISL6265HR 45	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0_0 0~1.55V 18A VCC_CORE_S0_1 0~1.55V 18A VDDNB 0~1.55V 18A

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BLOCK DIAGRAM

Size	Document Number	Rev
A3	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 1 of 61

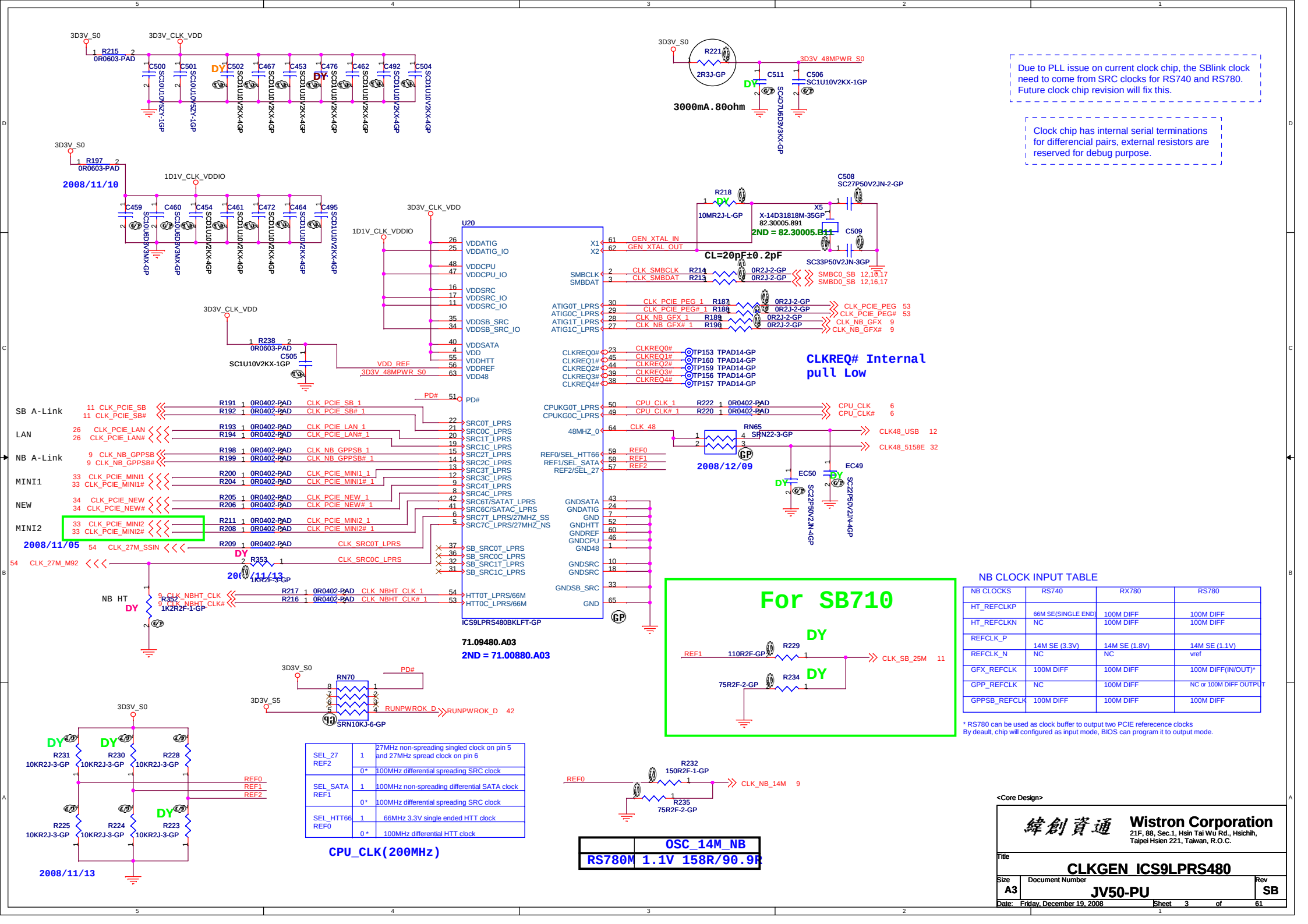
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **USB/PCIE Routing**

Size	Document Number	Rev
A3	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 2 of 61



NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SINGLE END)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	NC	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.

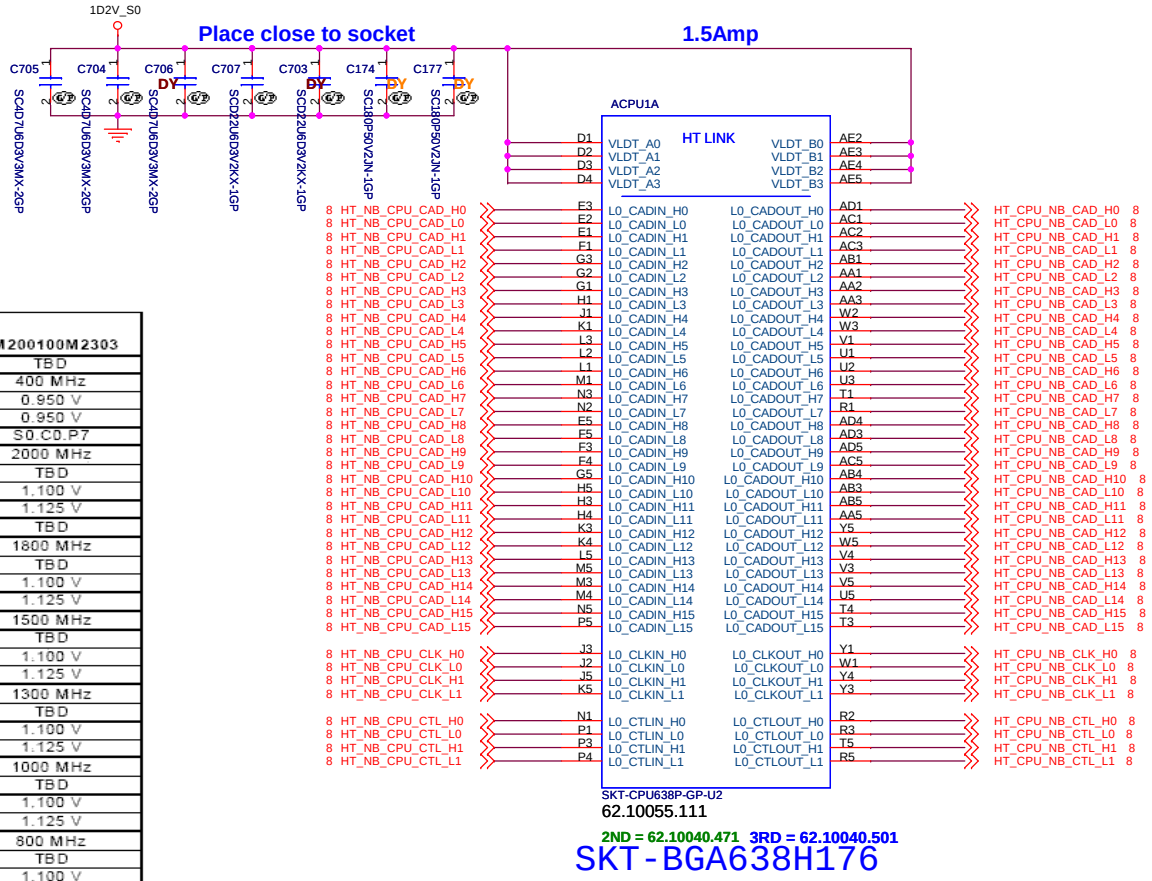
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CLKGEN_ICS9LPRS480

Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 3 of 61



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

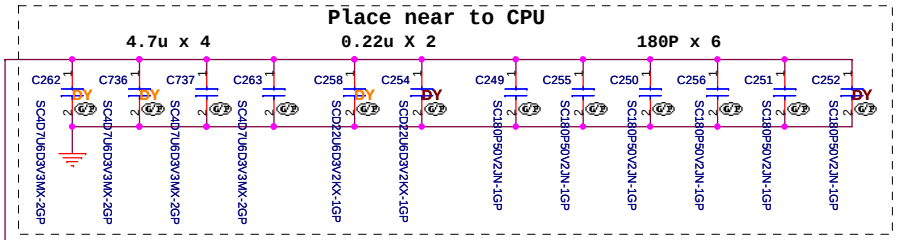
<Core Design>

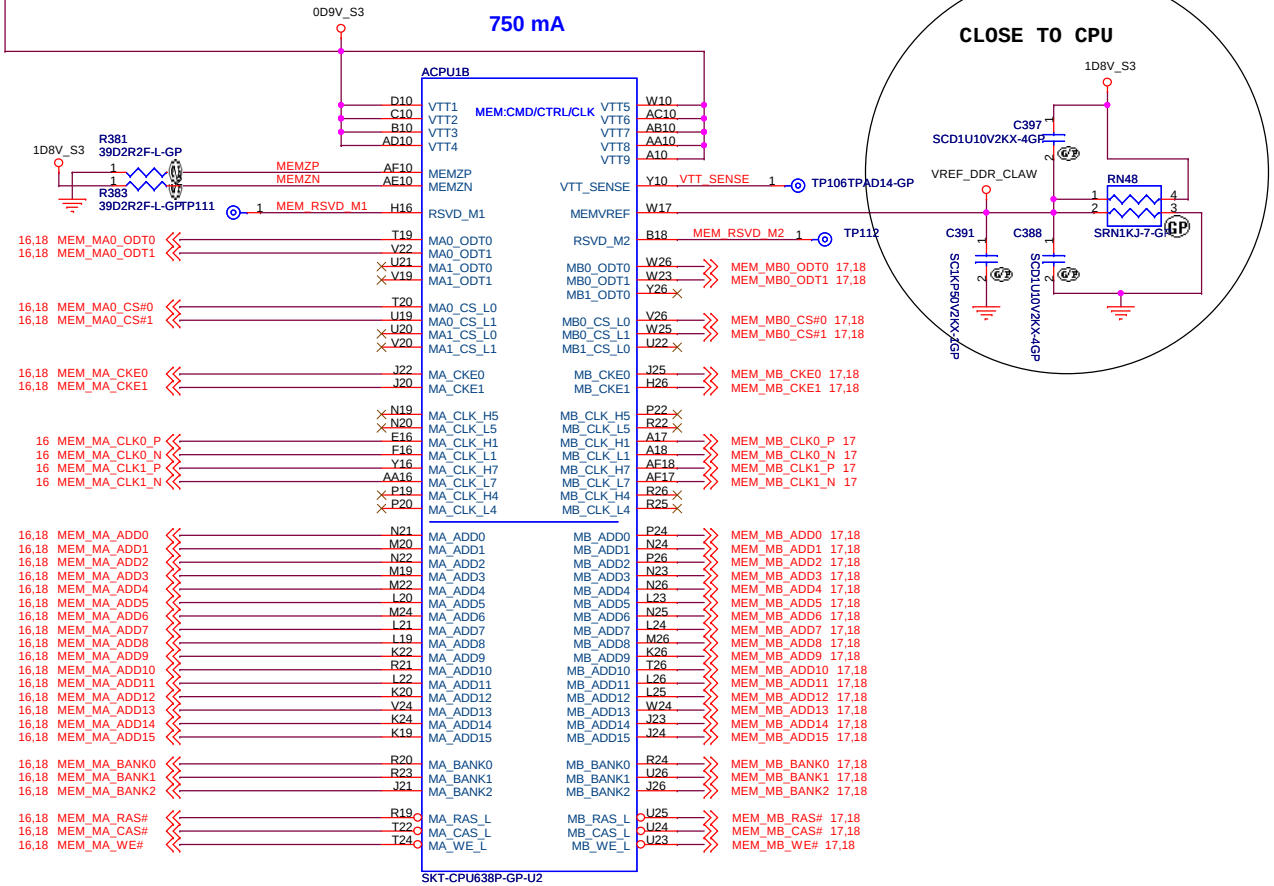
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

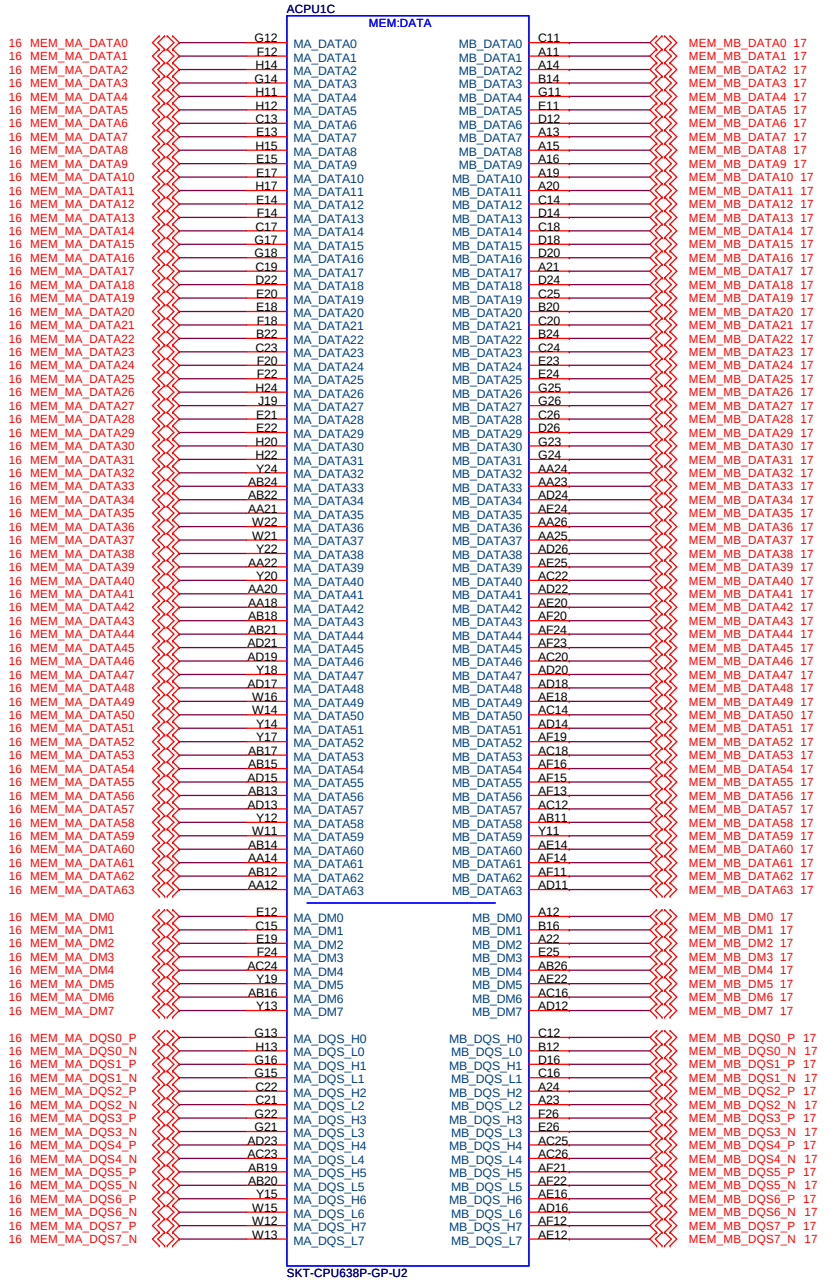
Title: CPU_HT_LINK I/F (1/4)

Size	Document Number	Rev
A3	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 4 of 61







<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR (2/4)

Size	Document Number	Rev
A3	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 5 of 61

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

Cloce To CPU

For HDT DBG

2008/11/03

2008/11/05

2008/11/11

internal pull high 300 ohm

For leverage S1g3, please reserve 300 ohm resistor pullup to VDDIO.

For leverage S1g3, please reserve 300 ohm resistor pulldown to VSS

SA

Near CPU PIN

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

CPU exceeds to 125℃

HDT Connectors

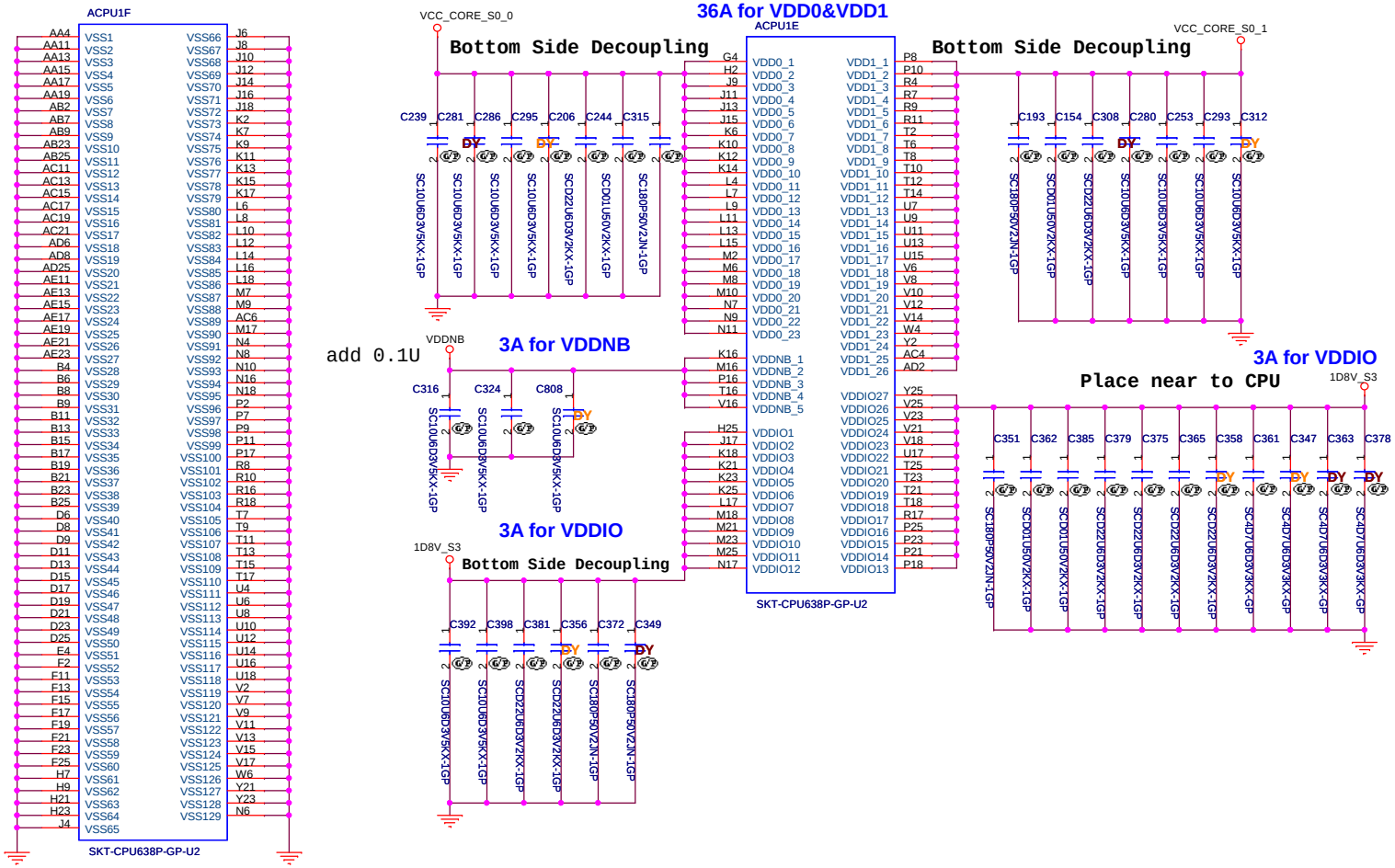
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Core Design>

Title: CPU_Control&Debug_(3/4)

Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 6 of 61



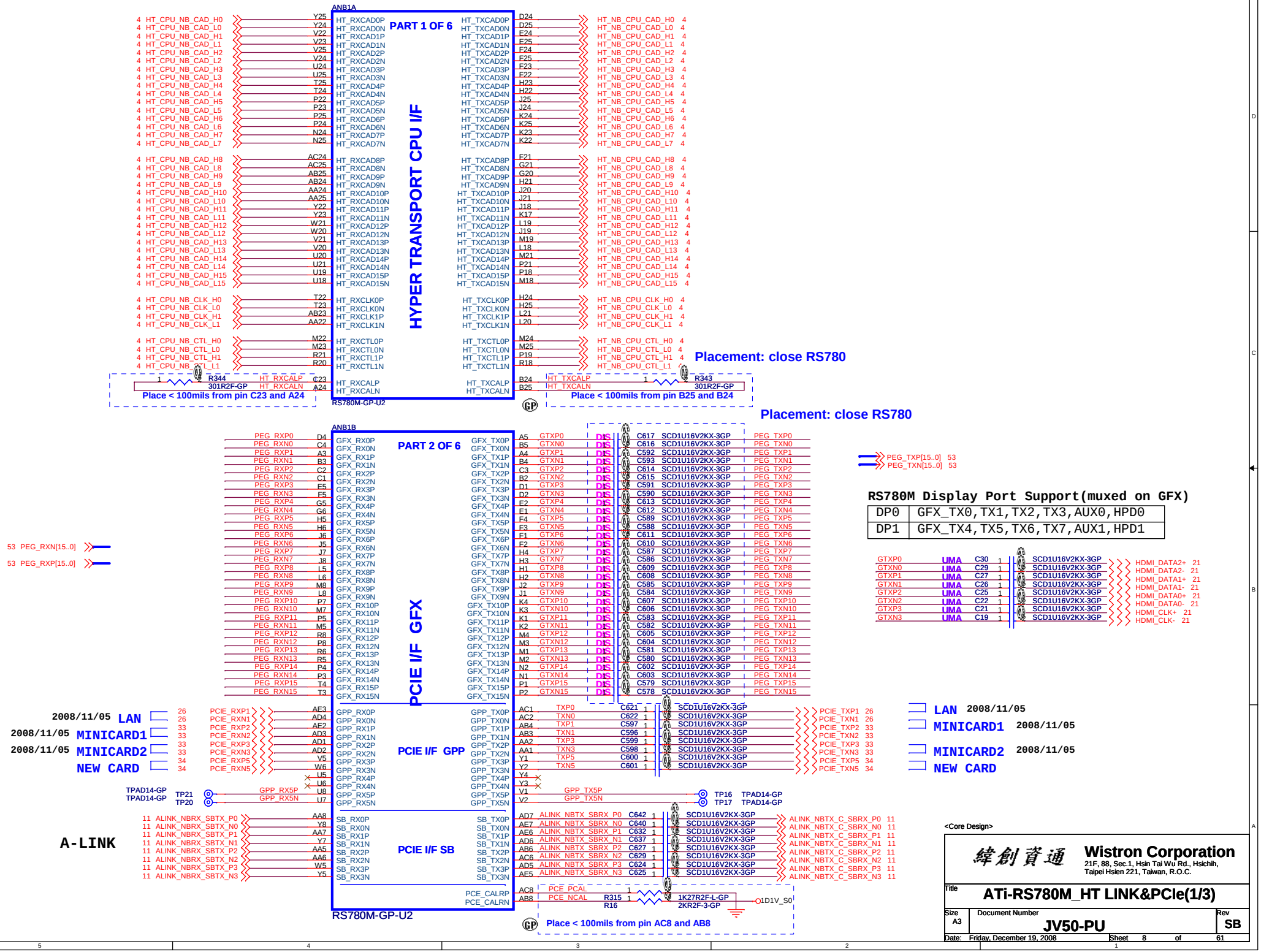
<Core Design>

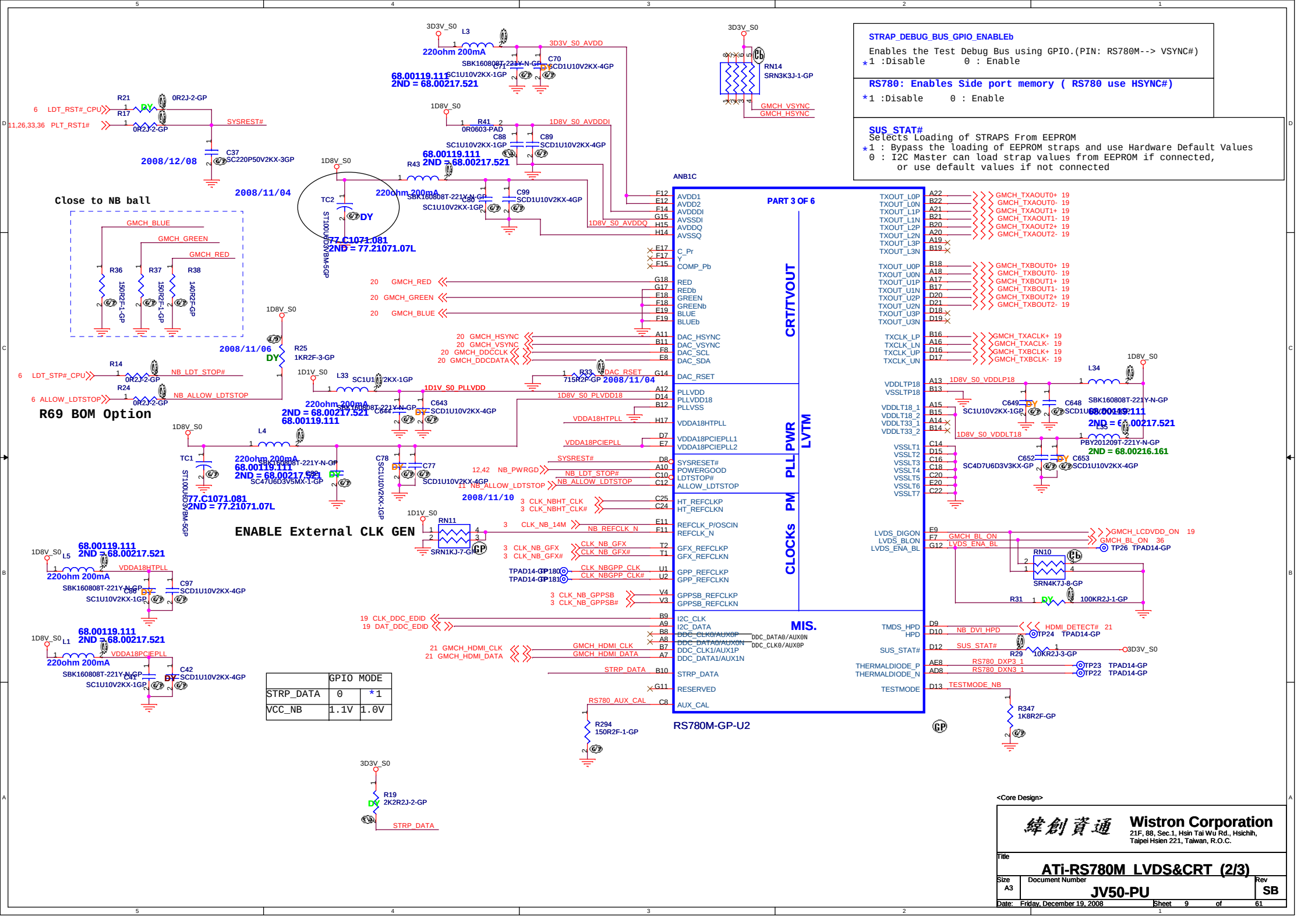
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

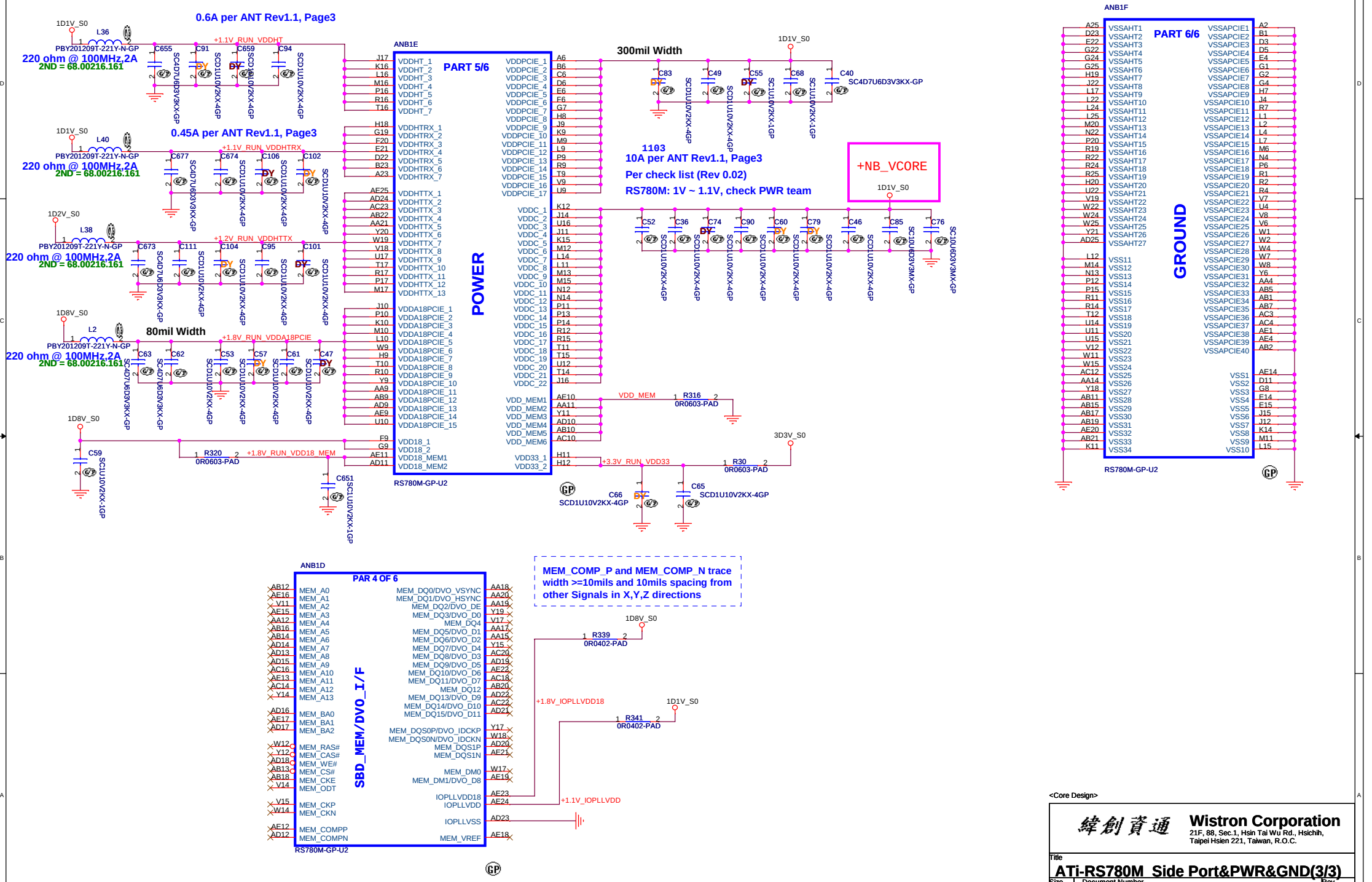
Title: CPU_Power_(4/4)

Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 7 of 61

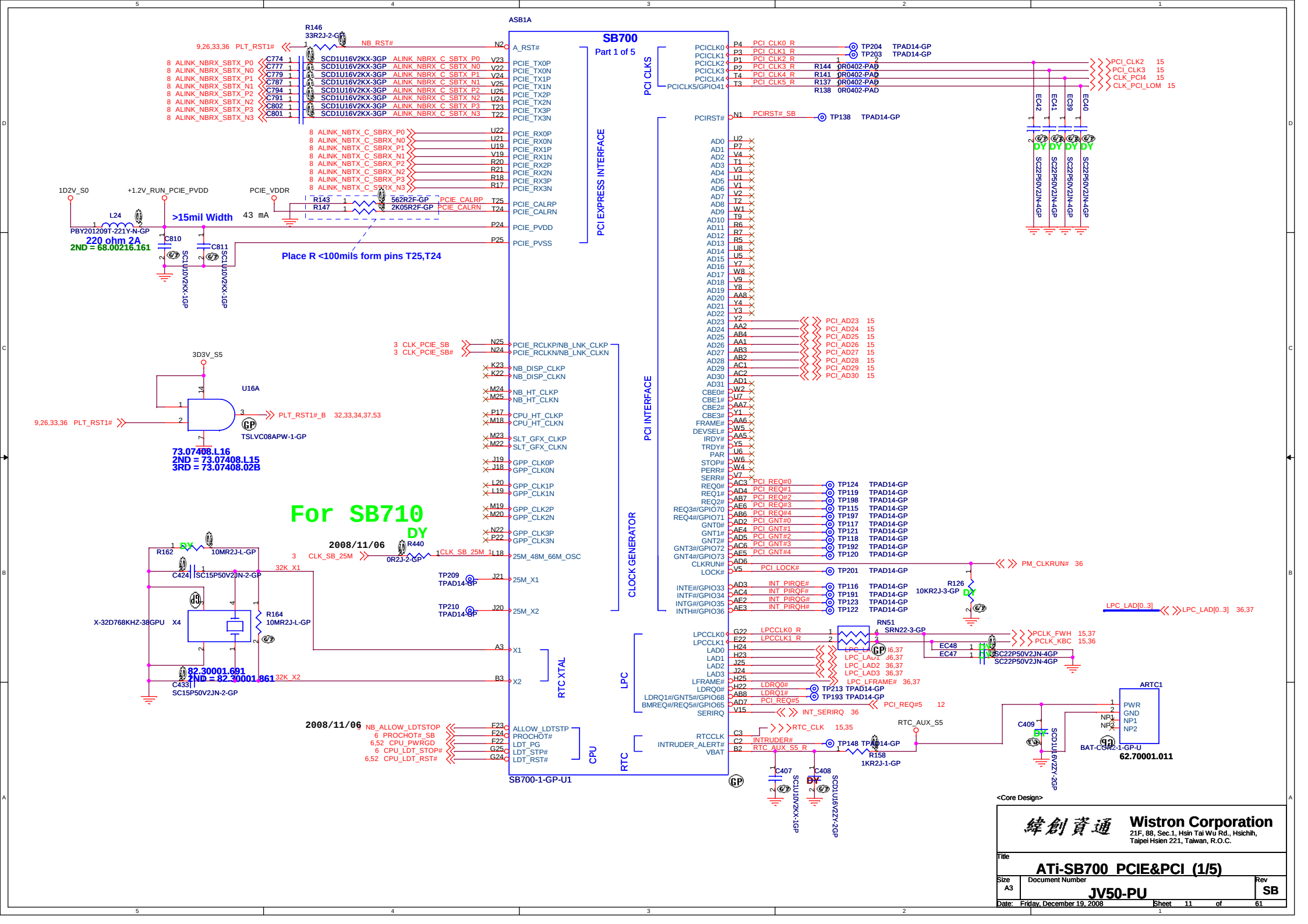

ANB1A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
Placement: close RS780
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
R344 301R2F-GP
R343 301R2F-GP
ANB1B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780M-GP-U2
Place < 100mils from pin AC8 and AB8
R315 1K27R2F-L-GP
R16 2KR2F-3-GP
RS780M Display Port Support(muxed on GFX)
DP0 GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1 GFX_TX4,TX5,TX6,TX7,AUX1,HPD1
2008/11/05 LAN
2008/11/05 MINICARD1
2008/11/05 MINICARD2
NEW CARD
A-LINK
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS780M_HT LINK&PCIe(1/3)
Size A3
Document Number JV50-PU
Rev SB
Date: Friday, December 19, 2008
Sheet 8 of 61

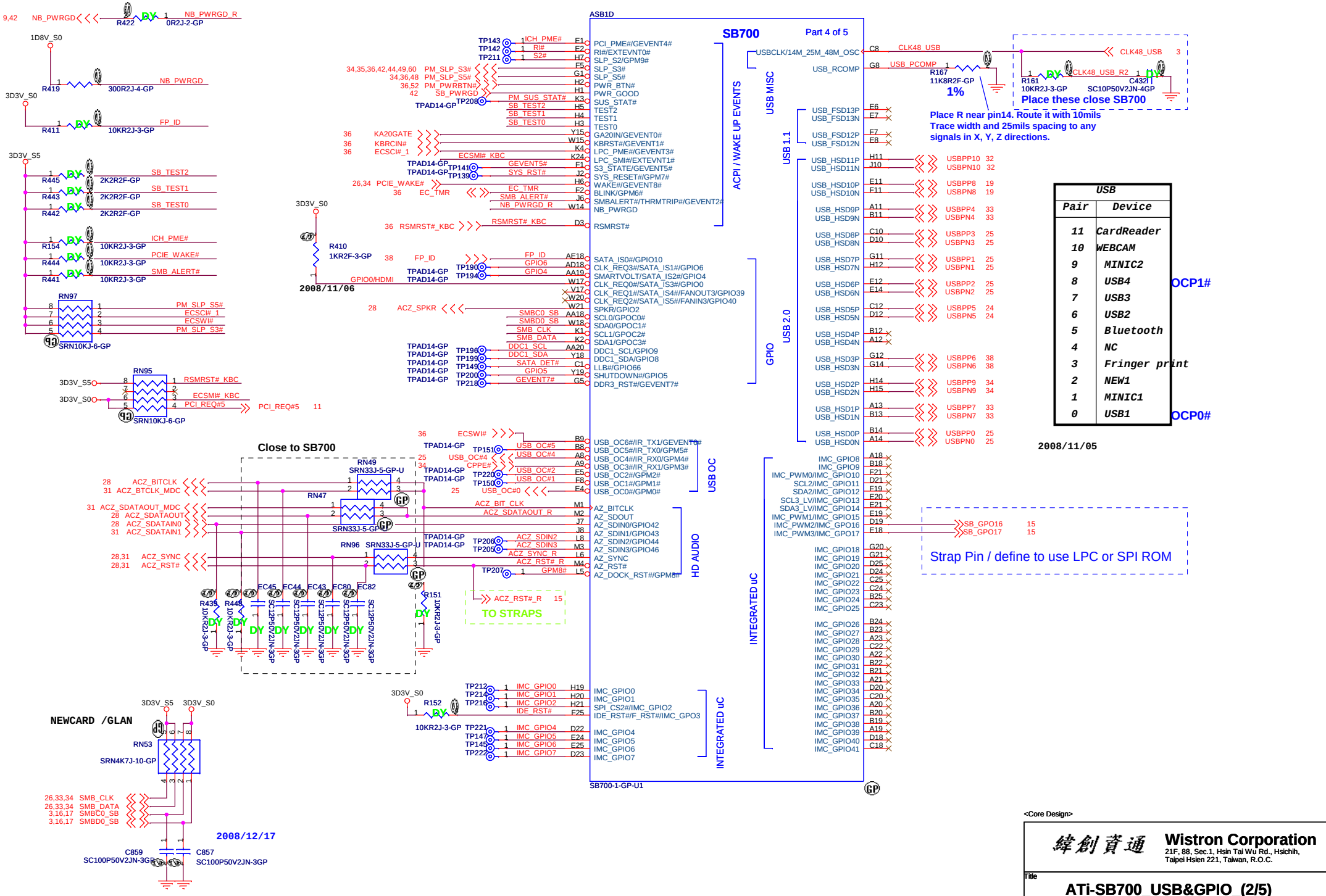

STRAP_DEBUG_BUS_GPIO_ENABLEb
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC#)
*1 :Disable 0 : Enable
RS780: Enables Side port memory (RS780 use HSYNC#)
*1 :Disable 0 : Enable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
Close to NB ball
R69 BOM Option
ENABLE External CLK GEN
ANB1C
PART 3 OF 6
RS780M-GP-U2
CRT/TVOUT
LVTM
PLL/PWR
CLOCKs
PM
MIS.
AVDD1
AVDD2
AVDDDI
AVSSDI
AVDDQ
AVSSQ
C_Pr
Y
COMP_Pb
RED
REDb
GREEN
GREENb
BLUE
BLUEb
DAC_HSYNC
DAC_VSYNC
DAC_SCL
DAC_SDA
DAC_RSET
PLLVDD
PLLVDD18
PLLVSS
VDDA18HTPLL
VDDA18PCIEPLL1
VDDA18PCIEPLL2
SYSRESET#
POWERGOOD
LDTSTOP#
ALLOW_LDTSTOP
HT_REFCLKP
HT_REFCLKN
REFCLK_P/OSCIN
REFCLK_N
GFX_REFCLKP
GFX_REFCLKN
GPP_REFCLKP
GPP_REFCLKN
GPPSB_REFCLKP
GPPSB_REFCLKN
I2C_CLK
I2C_DATA
DDC_CLK0/AUX0P
DDC_DATA0/AUX0N
DDC_CLK1/AUX1P
DDC_DATA1/AUX1N
STRP_DATA
RESERVED
AUX_CAL
TXOUT_L0P
TXOUT_L0N
TXOUT_L1P
TXOUT_L1N
TXOUT_L2P
TXOUT_L2N
TXOUT_L3P
TXOUT_L3N
TXOUT_U0P
TXOUT_U0N
TXOUT_U1P
TXOUT_U1N
TXOUT_U2P
TXOUT_U2N
TXOUT_U3P
TXOUT_U3N
TXCLK_LP
TXCLK_LN
TXCLK_UP
TXCLK_UN
VDDLTP18
VSSLTP18
VDDLT18_1
VDDLT18_2
VDDLT33_1
VDDLT33_2
VSSLT1
VSSLT2
VSSLT3
VSSLT4
VSSLT5
VSSLT6
VSSLT7
LVDS_DIGON
LVDS_BLON
LVDS_ENA_BL
TMDS_HPD
HPD
SUS_STAT#
THERMALDIODE_P
THERMALDIODE_N
TESTMODE
3D3V_S0
1D8V_S0
1D1V_S0
1V_S0
1D8V_S0_AVDDQ
1D8V_S0_PLVDD18
1D1V_S0_PLLVDD
VDDA18HTPLL
VDDA18PCIEPLL
GMCH_BLUE
GMCH_GREEN
GMCH_RED
GMCH_HSYNC
GMCH_VSYNC
GMCH_DDCCLK
GMCH_DDCDATA
DAC_RSET
NB_PWRGD
NB_LDT_STOP#
NB_ALLOW_LDTSTOP
CLK_NBHT_CLK
CLK_NBHT_CLK#
CLK_NB_14M
NB_REFCLK_N
CLK_NB_GFX
CLK_NB_GFX#
CLK_NBGPP_CLK
CLK_NBGPP_CLK#
CLK_NB_GPPSB
CLK_NB_GPPSB#
CLK_DDC_EDID
DAT_DDC_EDID
GMCH_HDMI_CLK
GMCH_HDMI_DATA
STRP_DATA
RS780_AUX_CAL
GMCH_TXAOUT0+ 19
GMCH_TXAOUT0- 19
GMCH_TXAOUT1+ 19
GMCH_TXAOUT1- 19
GMCH_TXAOUT2+ 19
GMCH_TXAOUT2- 19
GMCH_TXBOUT0+ 19
GMCH_TXBOUT0- 19
GMCH_TXBOUT1+ 19
GMCH_TXBOUT1- 19
GMCH_TXBOUT2+ 19
GMCH_TXBOUT2- 19
GMCH_TXACLK+ 19
GMCH_TXACLK- 19
GMCH_TXBCLK+ 19
GMCH_TXBCLK- 19
GMCH_LCDVDD_ON 19
GMCH_BL_ON 36
HDMI_DETECT# 21
NB_DVI_HPD
SUS_STAT#
RS780_DXP3_1
RS780_DXN3_1
TESTMODE_NB
	GPIO MODE	
STRP_DATA	0	*1
VCC_NB	1.1V	1.0V
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-RS780M LVDS&CRT (2/3)
Size A3
Document Number JV50-PU
Rev SB
Date: Friday, December 19, 2008
Sheet 9 of 61



<Core Design>

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	ATi-RS780M_Side Port&PWR&GND(3/3)
Size: A3	Document Number: JV50-PU
Rev: SB	
Date: Friday, December 19, 2008	Sheet 10 of 61


ASB1A
SB700
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
SB700-1-GP-U1
R146 33R2J-2-GP
NB_RST#
9,26,33,36 PLT_RST1#
A_RST#
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_CALRP
PCIE_CALRN
PCIE_PVDD
PCIE_PVSS
R143 562R2F-GP PCIE_CALRP
R147 2K05R2F-GP PCIE_CALRN
1D2V_S0
+1.2V_RUN_PCIE_PVDD
PCIE_VDDR
L24 PBY201209T-221Y-N-GP
220 ohm 2A
2ND = 68.00216.161
>15mil Width
43 mA
C810
C811
SC10U10V2KX-1GP
Place R <100mils form pins T25,T24
3D3V_S5
U16A
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
PLT_RST1#_B 32,33,34,37,53
For SB710
DY
2008/11/06
R162 DY 10MR2J-L-GP
R440 0R2J-2-GP
CLK_SB_25M
CLK_SB_25M_1
C424 SC15P50V2JN-2-GP
32K_X1
X-32D768KHZ-38GPU X4
R164 10MR2J-L-GP
82.30001.691
2ND = 82.30001.861
C433 SC15P50V2JN-2-GP
32K_X2
TP209 TPAD14-GP
TP210 TPAD14-GP
25M_48M_66M_OSC
25M_X1
25M_X2
X1
X2
2008/11/06
NB_ALLOW_LDTSTOP
6 PROCHOT#_SB
6,52 CPU_PWRGD
6 CPU_LDT_STOP#
6,52 CPU_LDT_RST#
ALLOW_LDTSTP
PROCHOT#
LDT_PG
LDT_STP#
LDT_RST#
PCICLK0
PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5/GPIO41
PCI_CLK0_R
PCI_CLK1_R
PCI_CLK2_R
PCI_CLK3_R
PCI_CLK4_R
PCI_CLK5_R
TP204 TPAD14-GP
TP203 TPAD14-GP
R144 0R0402-PAD
R141 0R0402-PAD
R137 0R0402-PAD
R138 0R0402-PAD
PCI_CLK2 15
PCI_CLK3 15
CLK_PCI4 15
CLK_PCI_LOM 15
EC42 EC41 EC39 EC40
SC22P50V2JN-4GP
PCIRST#
PCIRST# SB
TP138 TPAD14-GP
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31
PCI_AD23 15
PCI_AD24 15
PCI_AD25 15
PCI_AD26 15
PCI_AD27 15
PCI_AD28 15
PCI_AD29 15
PCI_AD30 15
CBE0# CBE1# CBE2# CBE3# FRAME# DEVSEL# IRDY# TRDY# PAR STOP# PERR# SERR#
REQ0# REQ1# REQ2# REQ3#/GPIO70 REQ4#/GPIO71 GNT0# GNT1# GNT2# GNT3#/GPIO72 GNT4#/GPIO73 CLKRUN# LOCK#
PCI_REQ#0
PCI_REQ#1
PCI_REQ#2
PCI_REQ#3
PCI_REQ#4
PCI_GNT#0
PCI_GNT#1
PCI_GNT#2
PCI_GNT#3
PCI_GNT#4
PCI_LOCK#
TP124 TPAD14-GP
TP119 TPAD14-GP
TP198 TPAD14-GP
TP115 TPAD14-GP
TP197 TPAD14-GP
TP117 TPAD14-GP
TP121 TPAD14-GP
TP118 TPAD14-GP
TP192 TPAD14-GP
TP120 TPAD14-GP
TP201 TPAD14-GP
PM_CLKRUN# 36
R126 10KR2J-3-GP DY
INTE#/GPIO33 INTF#/GPIO34 INTG#/GPIO35 INTH#/GPIO36
INT_PIRQE#
INT_PIRQF#
INT_PIRQG#
INT_PIRQH#
TP116 TPAD14-GP
TP191 TPAD14-GP
TP123 TPAD14-GP
TP122 TPAD14-GP
LPC_LAD[0..3]
LPC_LAD[0..3] 36,37
RN51 SRN22-3-GP
LPCCLK0 LPCCLK1 LAD0 LAD1 LAD2 LAD3 LFRAME# LDRQ0# LDRQ1#/GNT5#/GPIO68 BMREQ#/REQ5#/GPIO65 SERIRQ
LPCCLK0_R
LPCCLK1_R
LPC_LAD0 36,37
LPC_LAD1 36,37
LPC_LAD2 36,37
LPC_LAD3 36,37
LPC_LFRAME# 36,37
LDRQ0#
LDRQ1#
PCI_REQ#5
TP213 TPAD14-GP
TP193 TPAD14-GP
PCI_REQ#5 12
INT_SERIRQ 36
PCLK_FWH 15,37
PCLK_KBC 15,36
EC48 EC47 DY
SC22P50V2JN-4GP
RTCCLK INTRUDER_ALERT# VBAT
RTC_CLK 15,35
INTRUDER#
RTC_AUX_S5_R
TP148 TPAD14-GP
R158 1KR2J-1-GP
RTC_AUX_S5
ARTC1
PWR GND NP1 NP2
BAT-CON2-1-GP-U
62.70001.011
C409 DY SCD1U16V2ZY-2GP
C407 SC1U10V2KX-1GP
C408 DY SCD1U16V2ZY-2GP
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700 PCIE&PCI (1/5)
Size A3
Document Number
JV50-PU
Rev SB
Date: Friday, December 19, 2008
Sheet 11 of 61



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700 USB&GPIO (2/5)

Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 12 of 61

PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700

SATA HDD

SATA ODD

SB700
Part 2 of 5

ASB1B

SERIAL ATA

ATA 66/100/133

2008/11/06

SPI ROM

SATA PWR

HW MONITOR

SB700-1-GP-U1

2008/12/11

Very Close to SB700

82.30020.A31
2ND = 82.30020.851

93 mA

>15mil Width

Dummy CKG select

CLK_ID
(1,0)
ICS: 0,0
SEG: 0,1
RTM: 1,0

Layout connect to Cap then GND

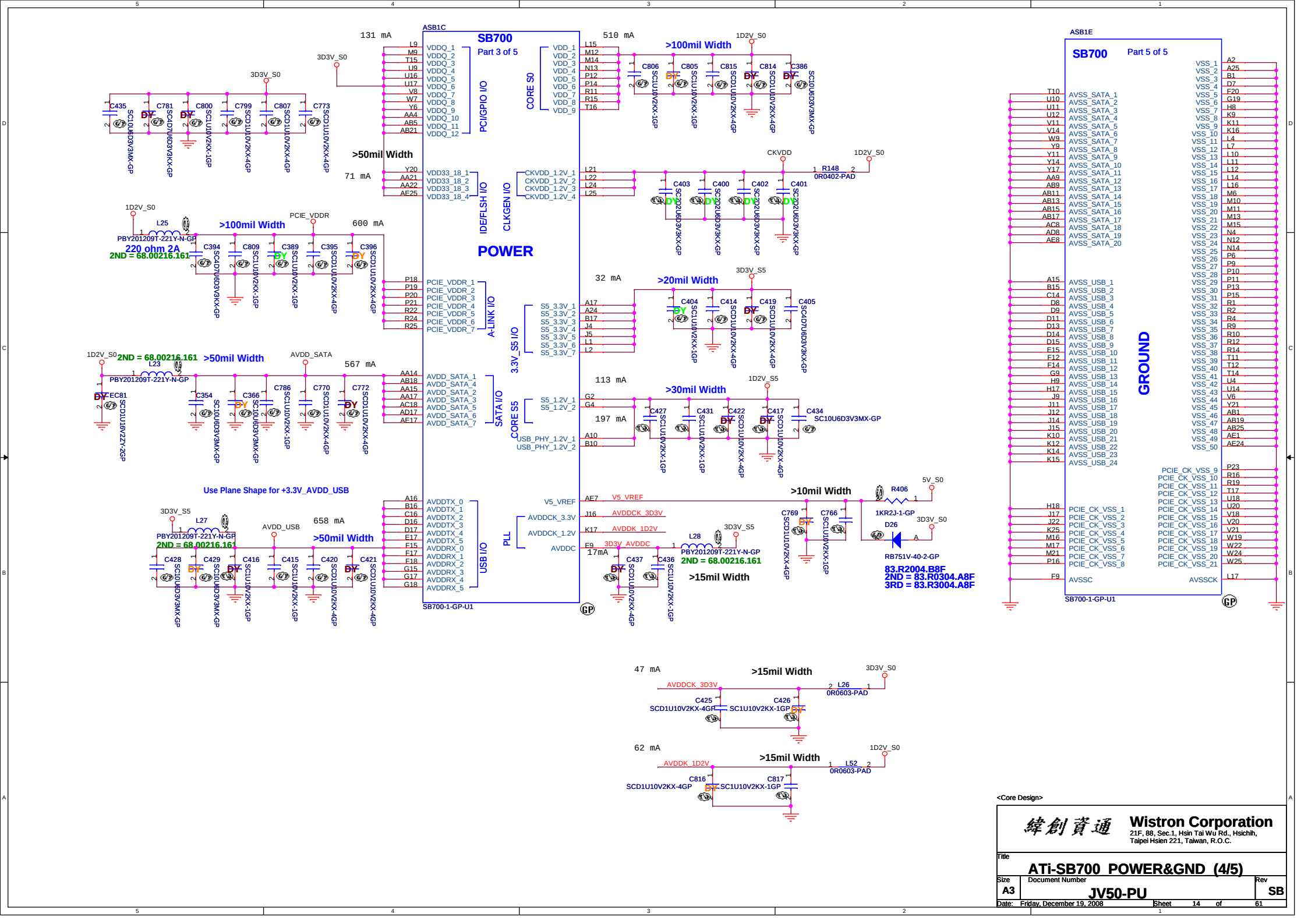
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700 SATA-IDE (3/5)

Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 13 of 61



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

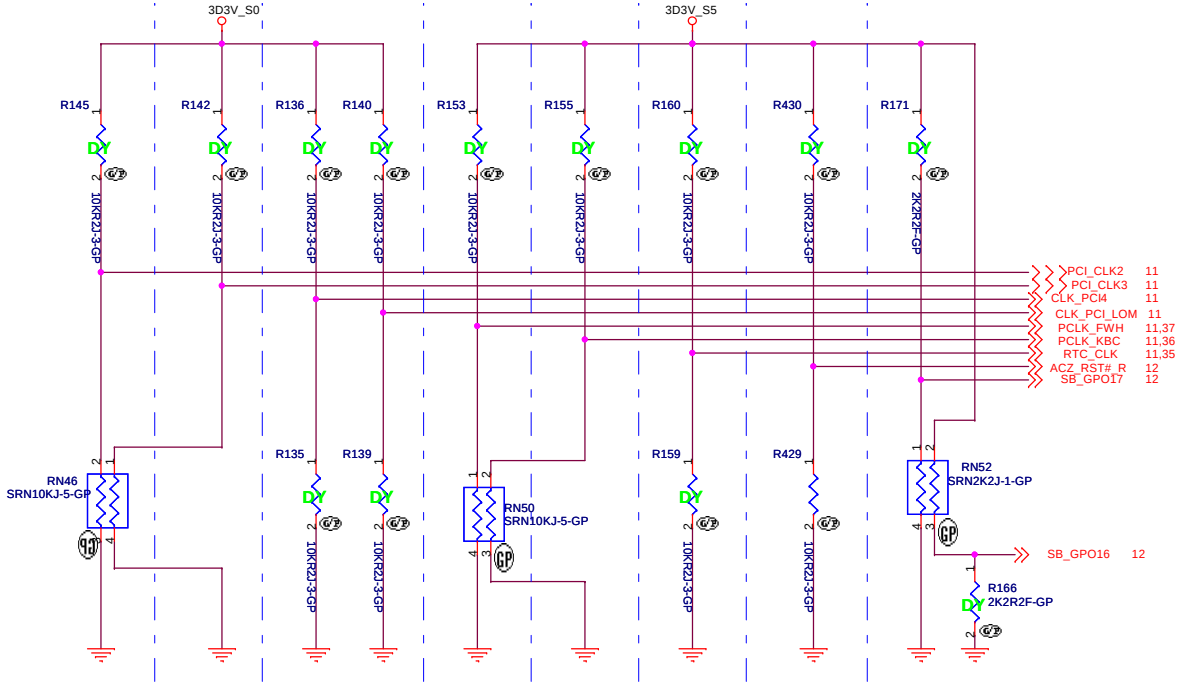
Title: ATi-SB700 POWER&GND (4/5)

Size	Document Number	Rev
A3	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 14 of 61

REQUIRED STRAPS

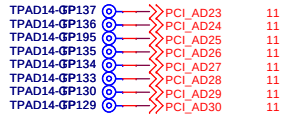
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

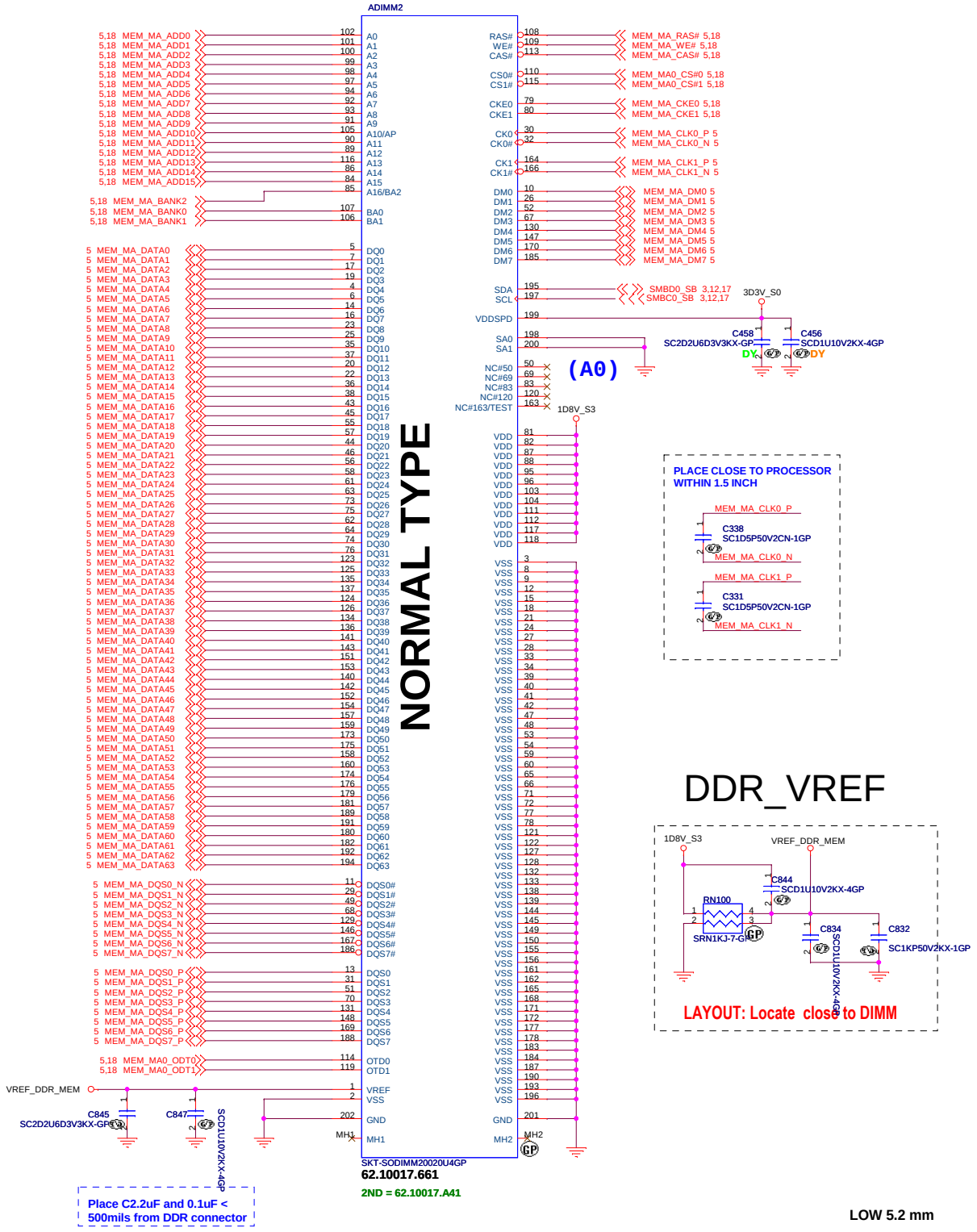
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700 STRAPPING (5/5)

Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 15 of 61



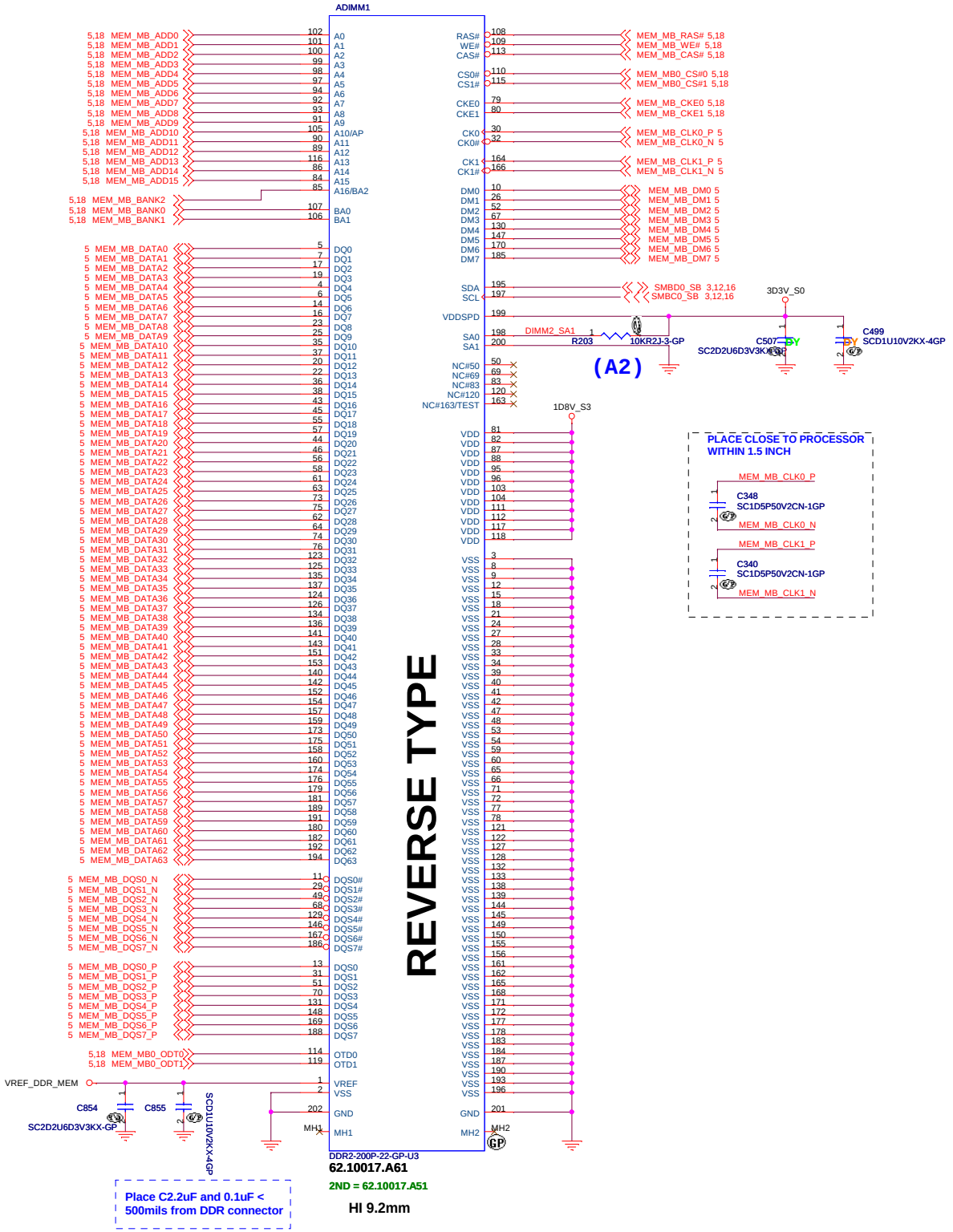
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_SO-DIMM SKT_1

Size: Custom | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 16 of 61



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

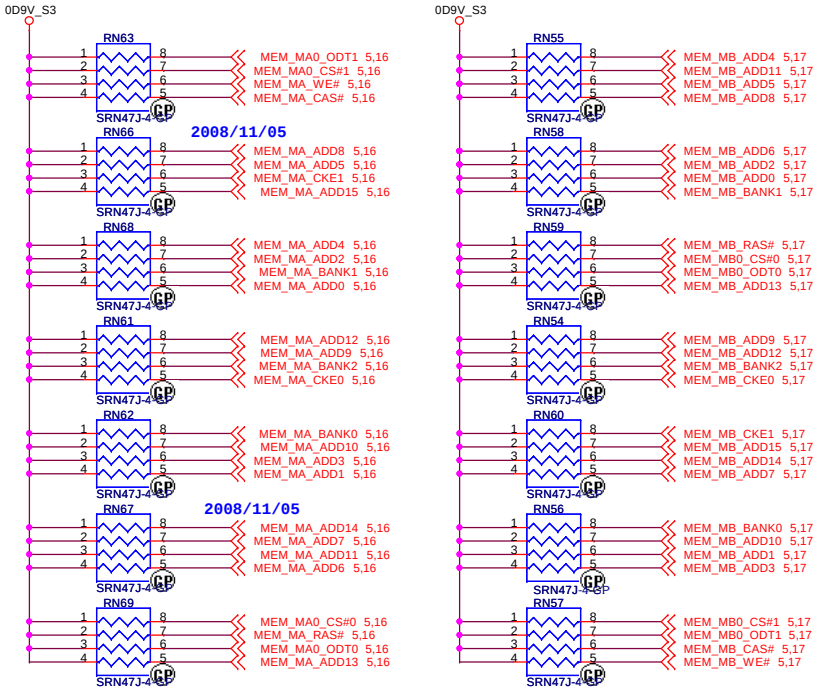
Title: DDR_SO-DIMM SKT_2

Size: Custom | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 17 of 61

PARALLEL TERMINATION

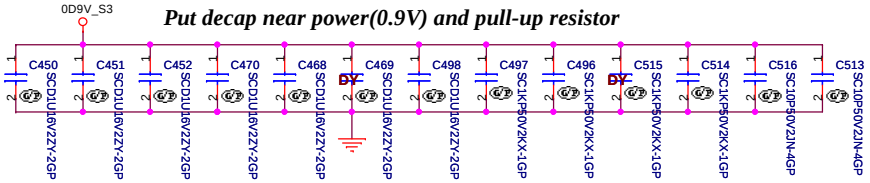
Put decap near power(0.9V) and pull-up resistor



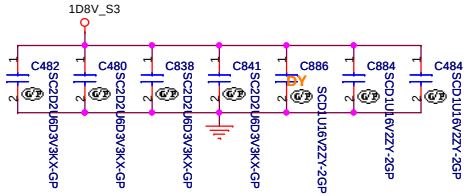
Do not share the Term resistor between the DDR addess and Control Signals.

Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

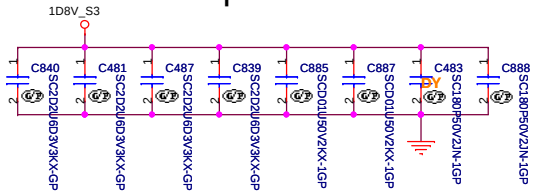


Place these Caps near DM1



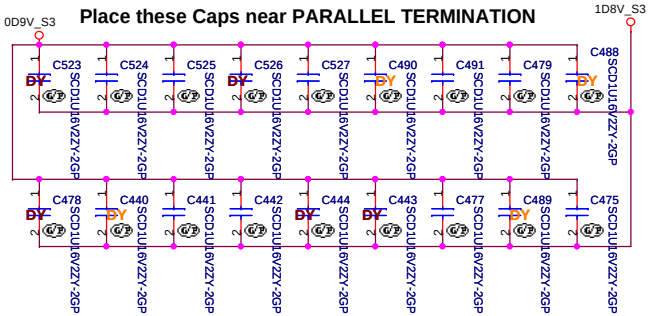
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



<Core Design>

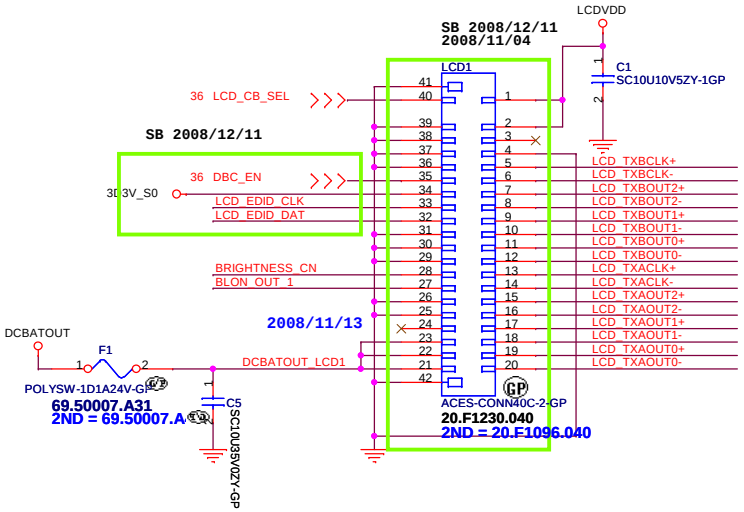
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

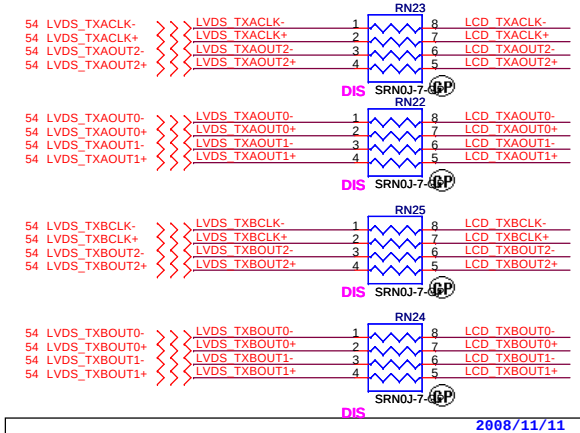
Title: **DDR_DAMPING & TERMINATION**

Size	Document Number	Rev
A3	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 18 of 61

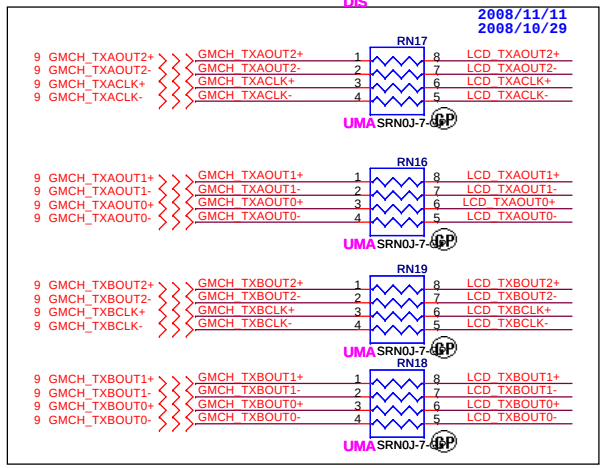
LCD/INVERTER/CCD CONN



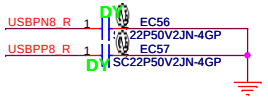


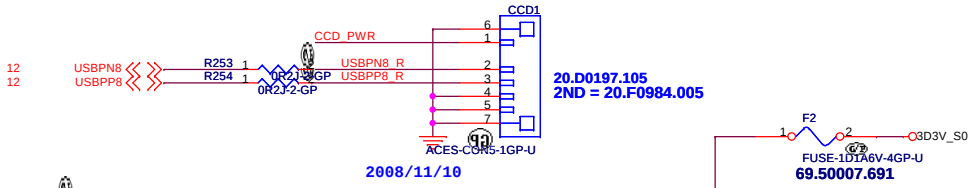
Inverter Pin	
Pin	Symbol
1	Vin
2	Vin
3	Brightness
4	BLON
5	GND
6	GND

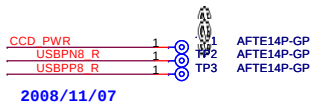
CCD Pin	
Pin	Symbol
1	CCD_PWR
2	USB-
3	USB+
4	GND
5	GND

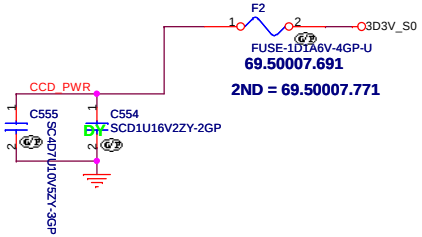


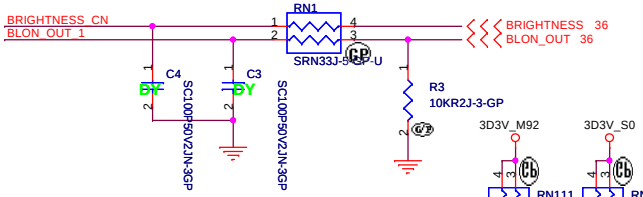
CCD

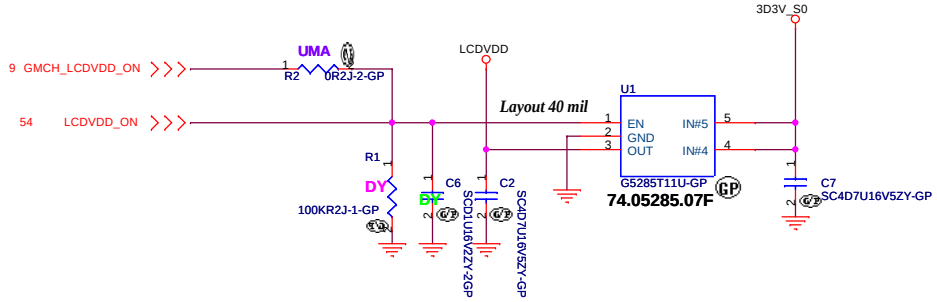


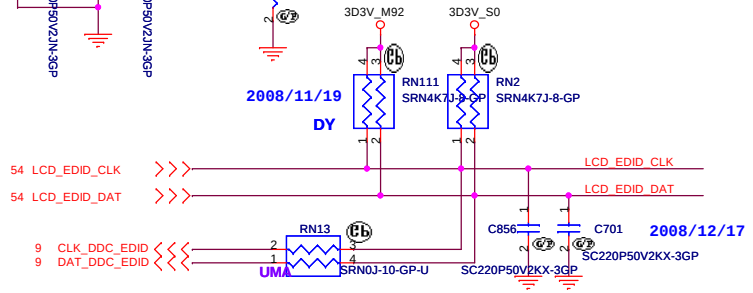












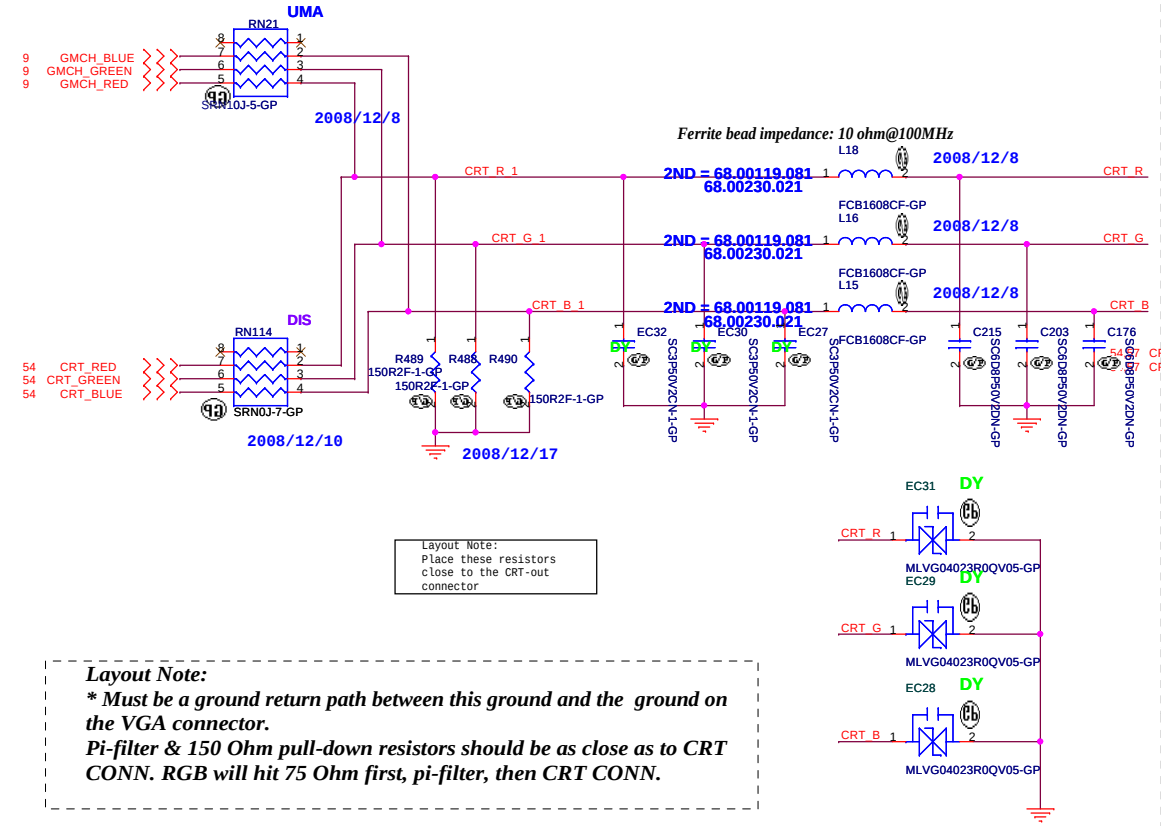
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

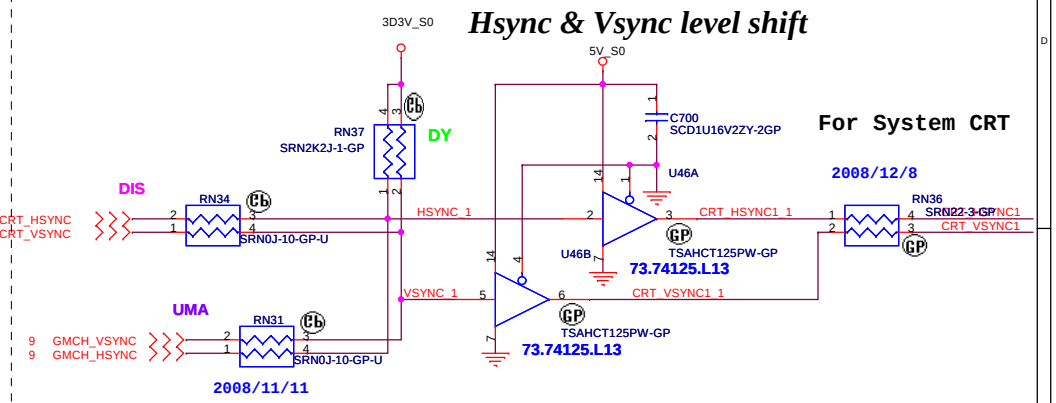
Title: LCD CONN

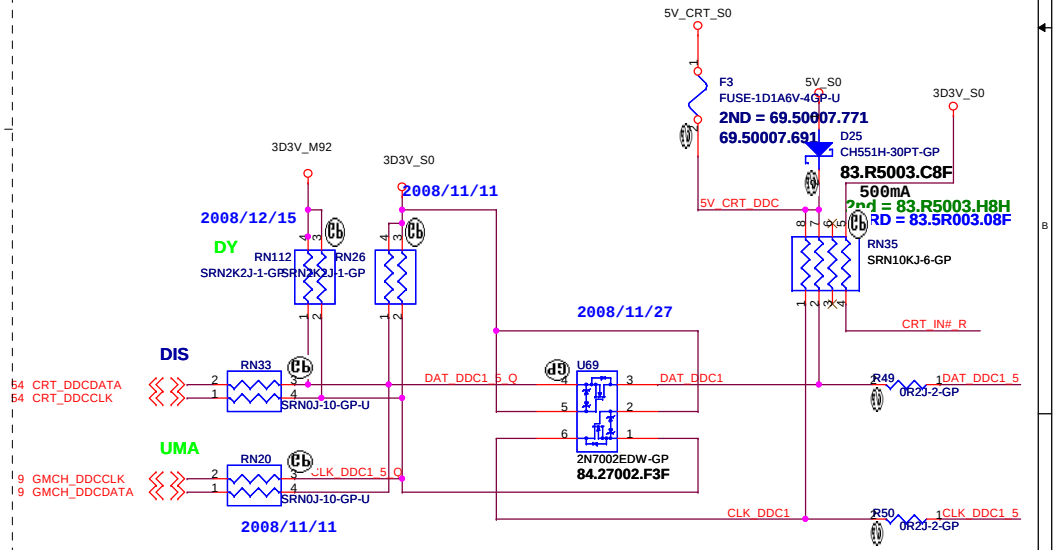
Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 19 of 61

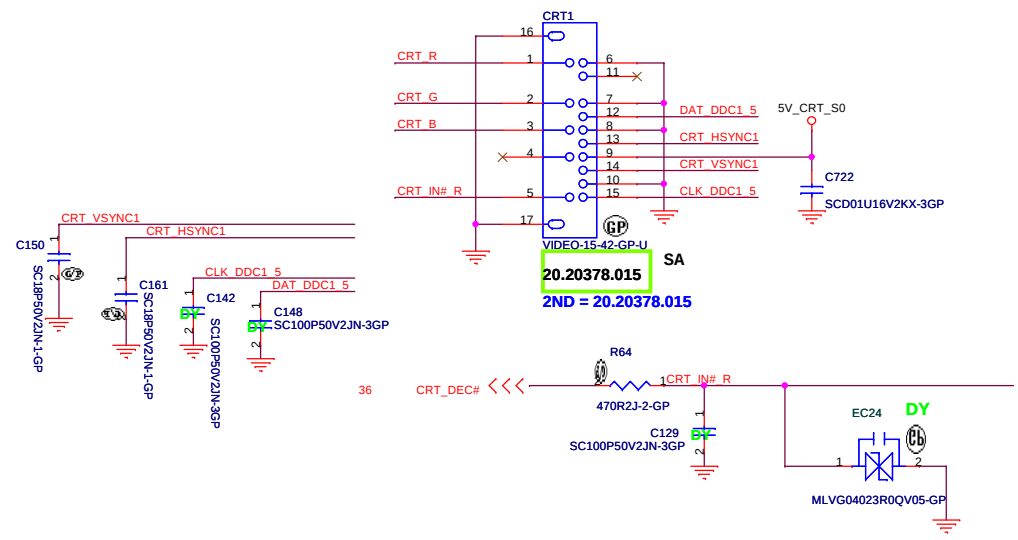


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.





CRT I/F & CONNECTOR



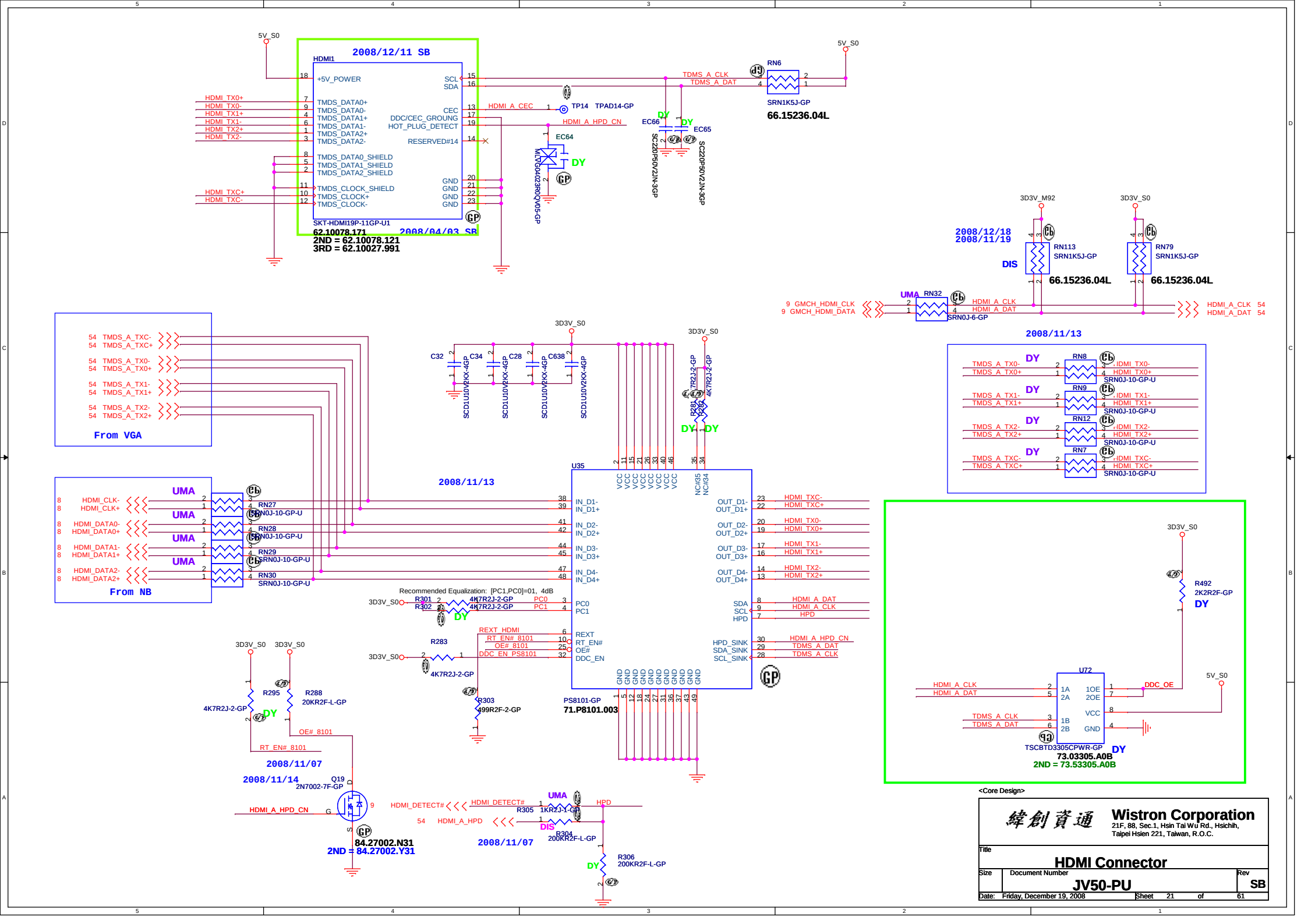
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**

Size	Document Number	Rev
	JV50-PU	SB

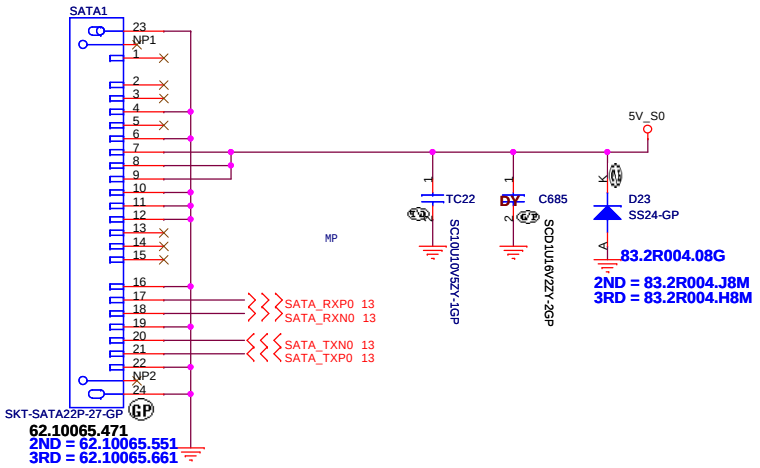
Date: Friday, December 19, 2008 Sheet 20 of 61



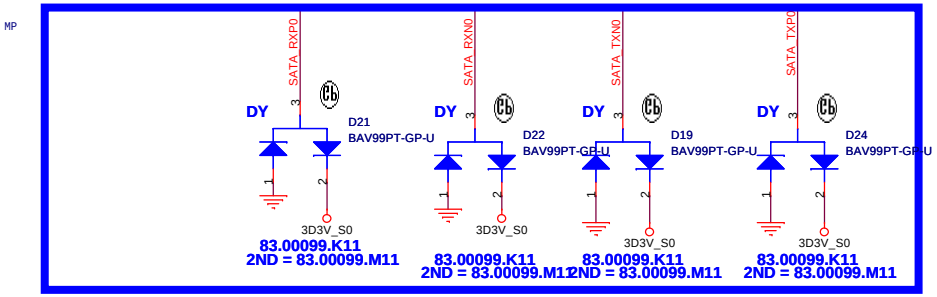
<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**HDMI Connector**	
Size	Document Number **JV50-PU**	Rev **SB**
Date: Friday, December 19, 2008	Sheet 21 of 61	

SATA Connector



2008/12/17



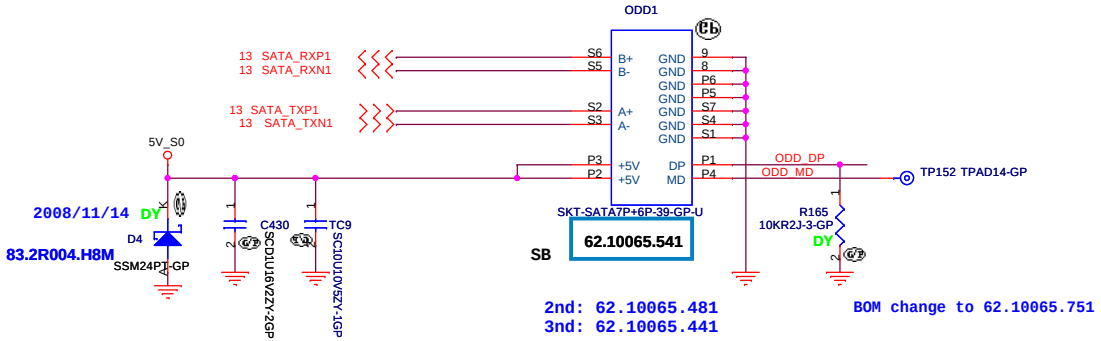
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

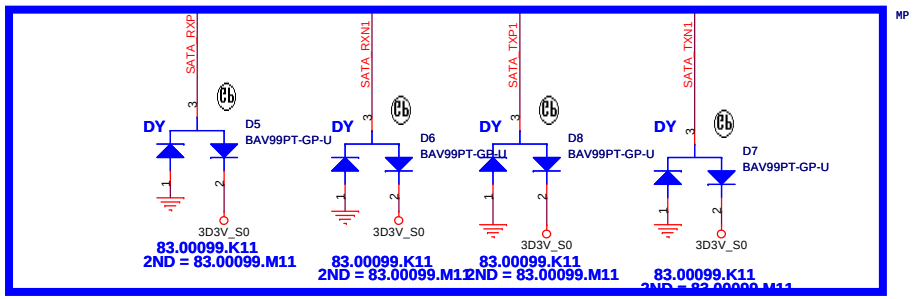
Title	HDD	
Size	Document Number JV50-PU	Rev SB
Date: Friday, December 19, 2008	Sheet 22 of 61	

SATA ODD Connector

2008/11/12



2008/12/17



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

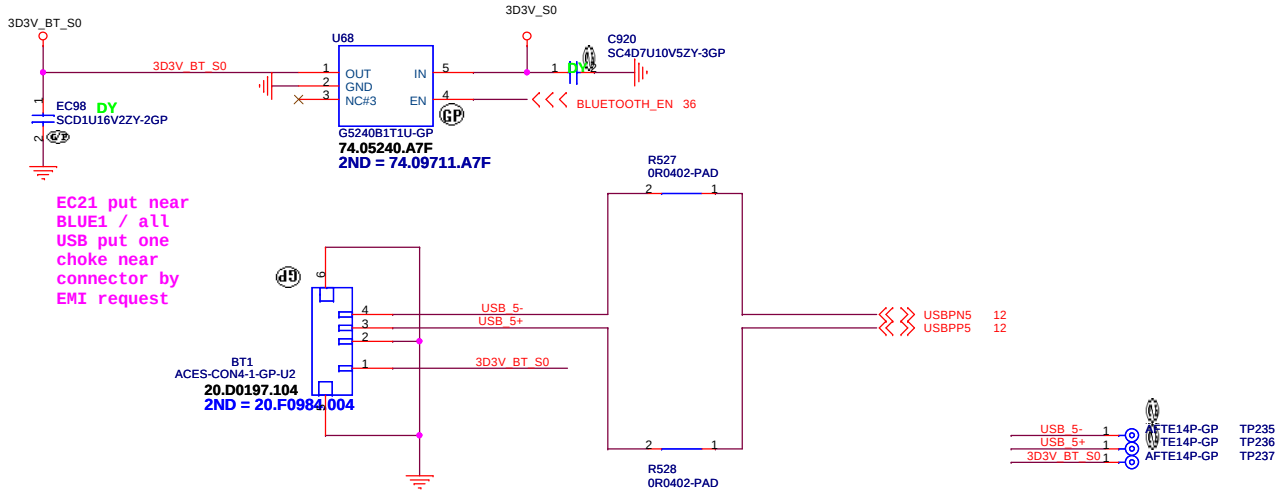
Title: ODD

Size | Document Number: JV50-PU | Rev: SB

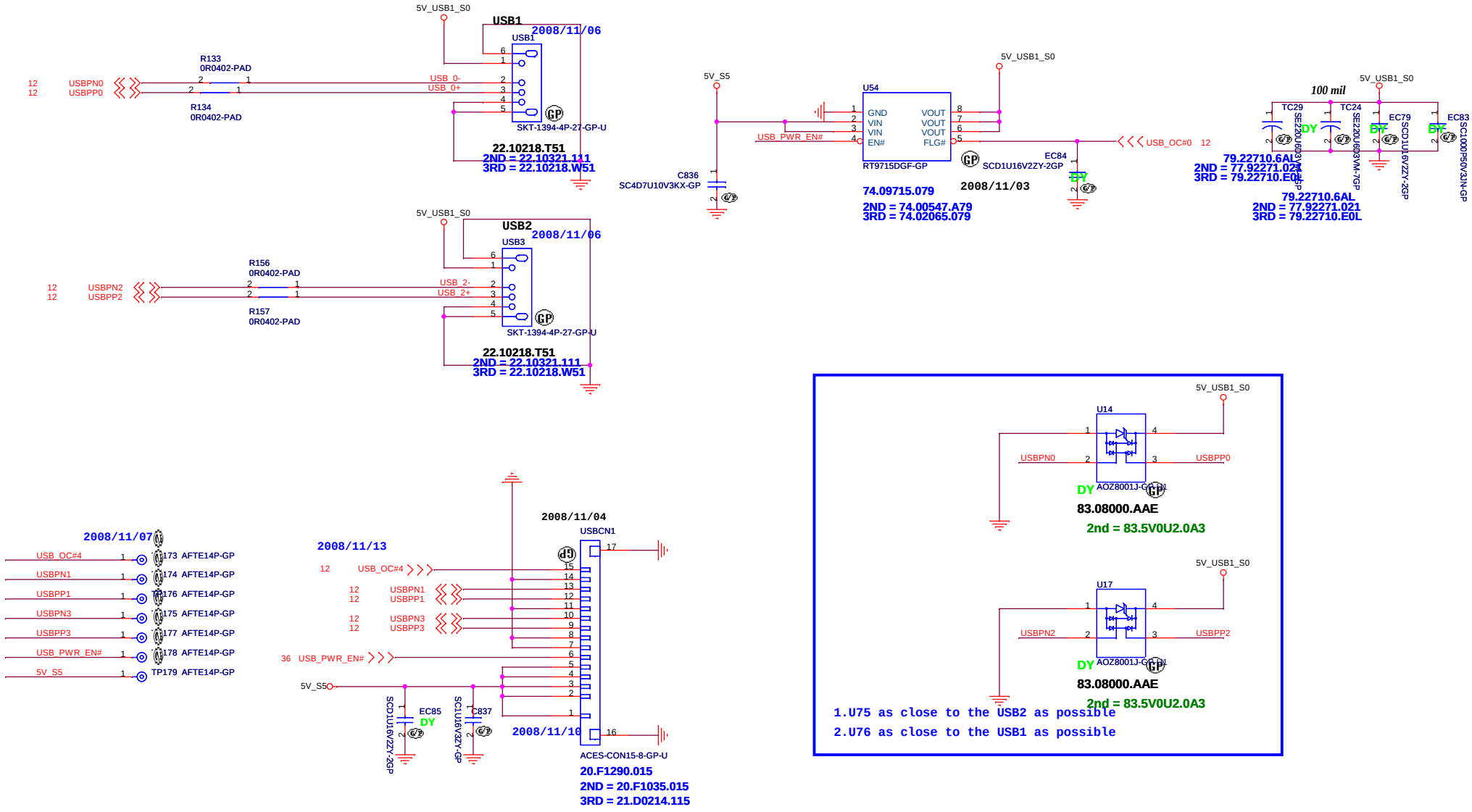
Date: Friday, December 19, 2008 | Sheet 23 of 61

BLUETOOTH MODULE

1.5A / High Active Voltage 2V



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: BLUETOOTH		
Size	Document Number: JV50-PU	Rev: SB
Date: Friday, December 19, 2008	Sheet 24 of 61	



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**USB**	
Size	Document Number **JV50-PU**	Rev **SB**
Date: Friday, December 19, 2008	Sheet 25 of 61	

CO-Layout BCM5764 and BCM5784
modify BOM :71.05784.003

2008/10/28

Place PLLVDD/AVDDL
CKT as close to chip as
possible

U4
BCM5764MKMLG-GP
71.05764.M01
2ND = 71.05784.003

U3
AT45DB011D-SH-T-GP
72.45011.B01

82.30020.A31
2ND = 82.30020.B51

2008/11/13

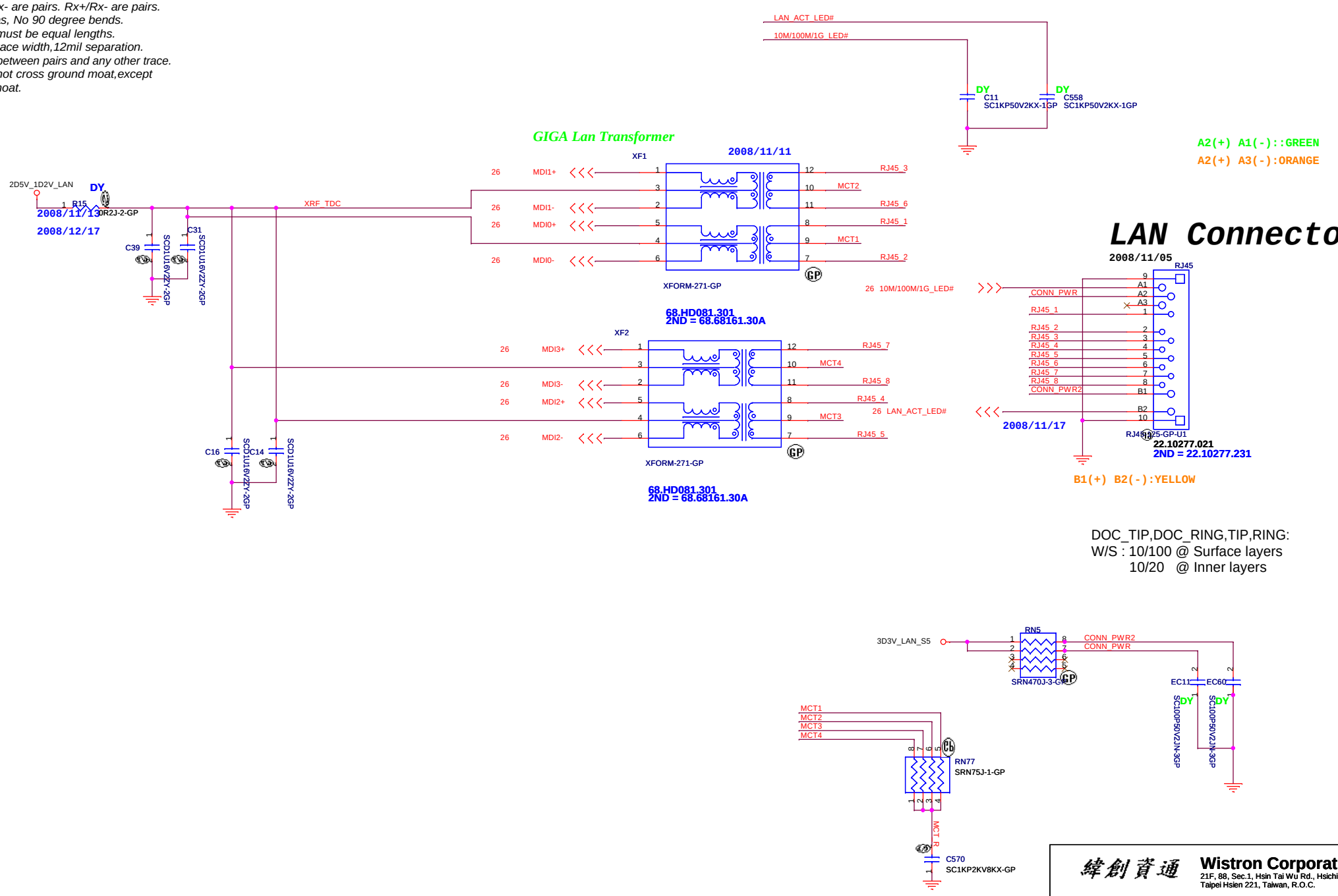
84.00069.B1B
2ND = 84.DCP69.01B
3RD = 84.00069.A1B

2008/11/13

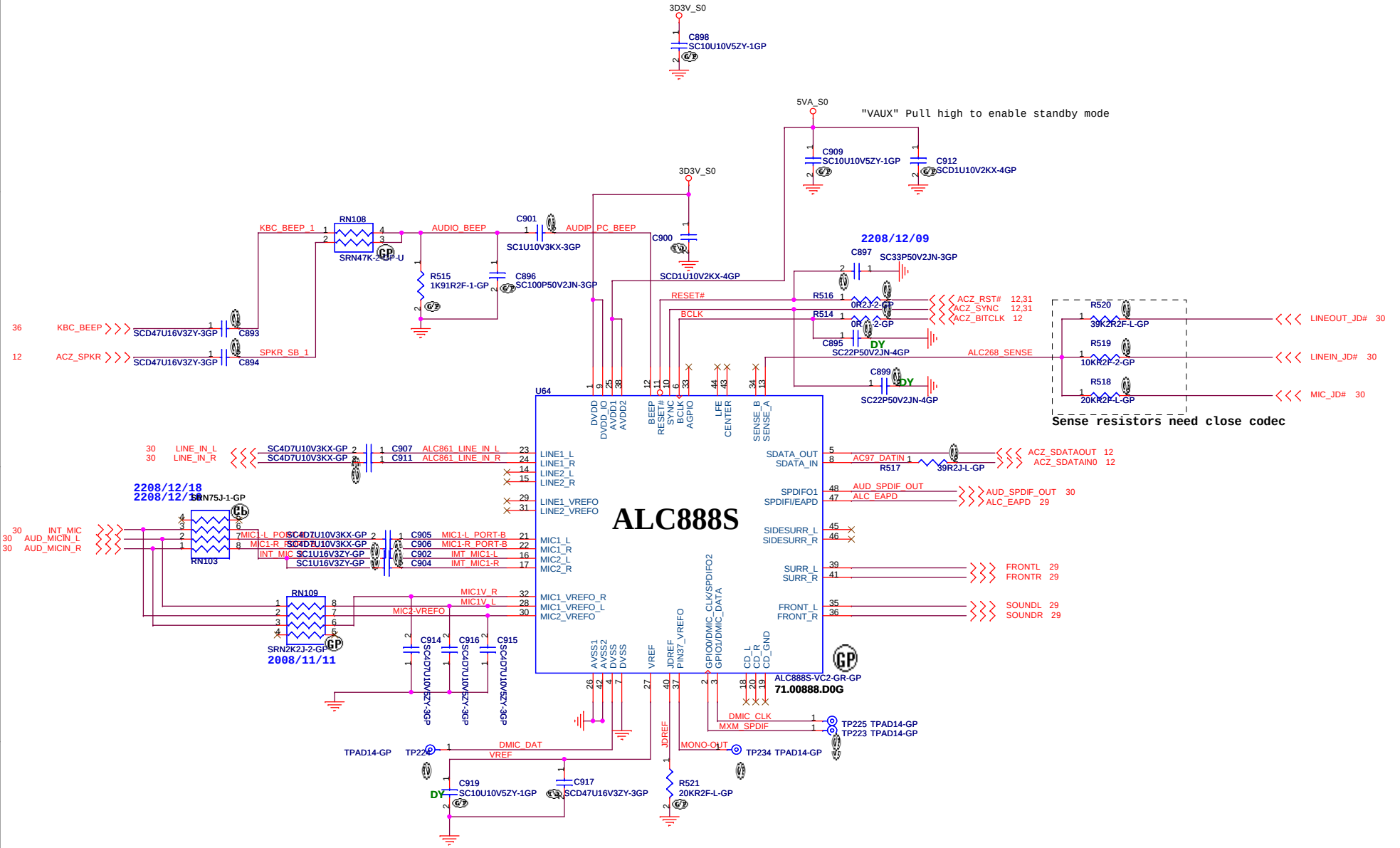
Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: BCM5764MKMLG	
Size: A3	Document Number: JV50-PU
Rev: SB	
Date: Friday, December 19, 2008	Sheet 26 of 61

LAN Connector

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**LAN CONN**	
Size: A3	Document Number: **JV50-PU**	Rev: **SB**
Date: Friday, December 19, 2008	Sheet 27 of 61	



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Azalia codec ALC888**	
Size A3	Document Number **JV50-PU**	Rev **SB**
Date: Friday, December 19, 2008	Sheet 28 of 61	

SB 2008/11/15

Close to U53.8 Close to U53.18

60ohm 100MHz
3000mA 0.05ohm DC

Close to Pin9

SB 2008/11/15

2008/12/31

GAIN SETTING

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Signal inverter for speaker shutdown

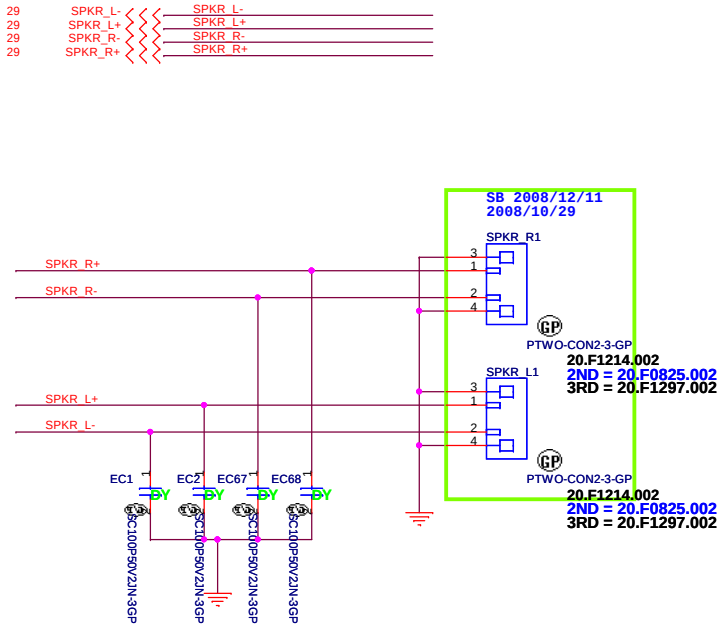
Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	

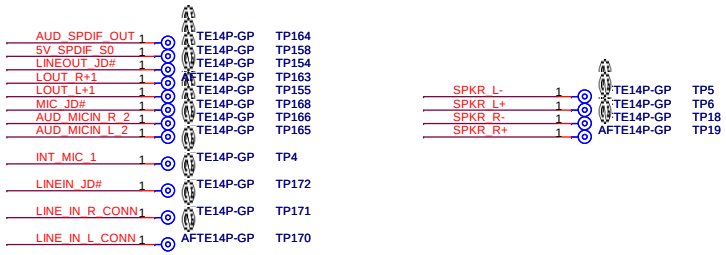
Title: AUDIO AMP

Size: | Document Number: JV50-PU | Rev: SB

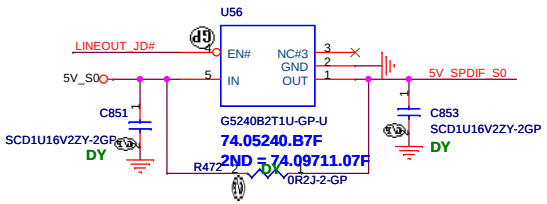
Date: Friday, December 19, 2008 Sheet 29 of 61

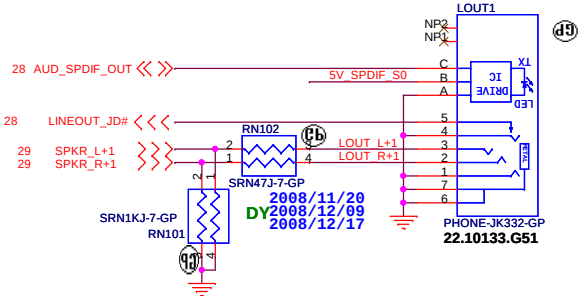
Internal Speaker



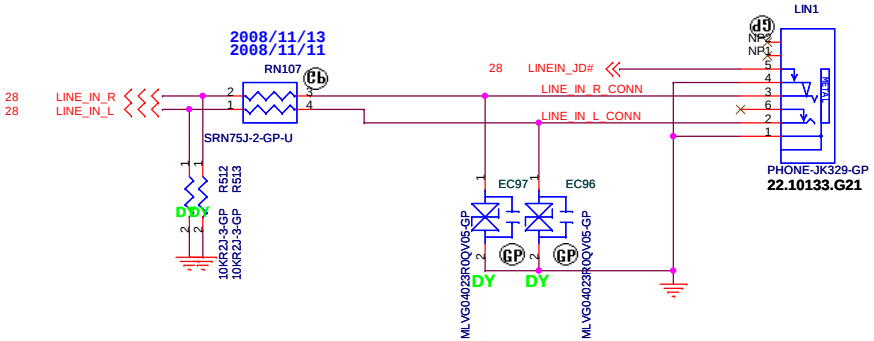


LINE OUT

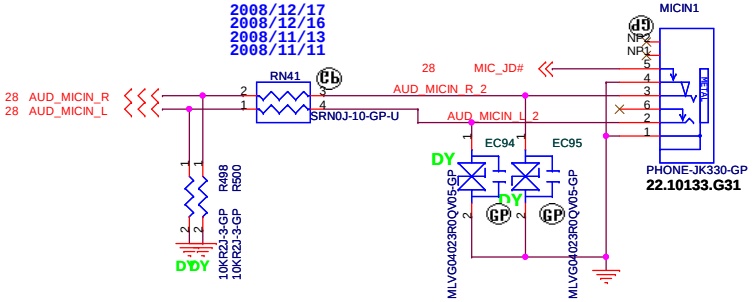




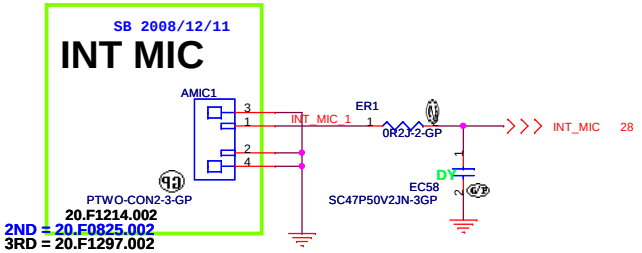
LINE IN



MIC IN



INT MIC



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO JACK		
Size	Document Number: JV50-PU	Rev: SB
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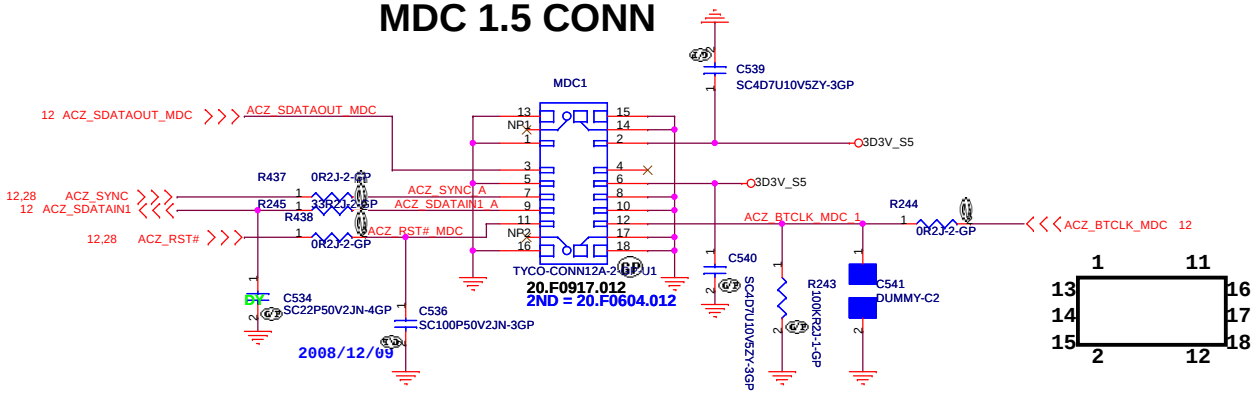
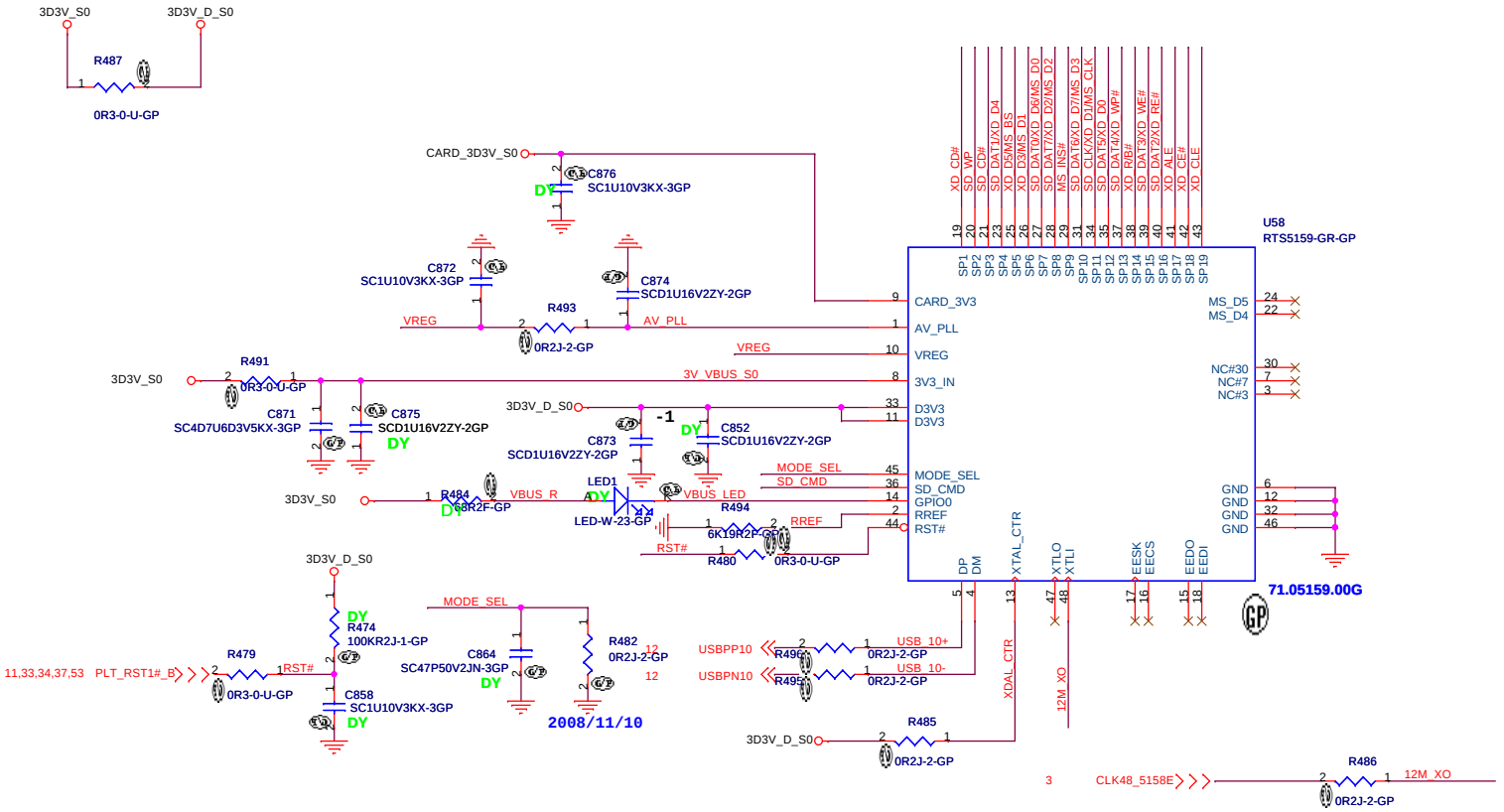
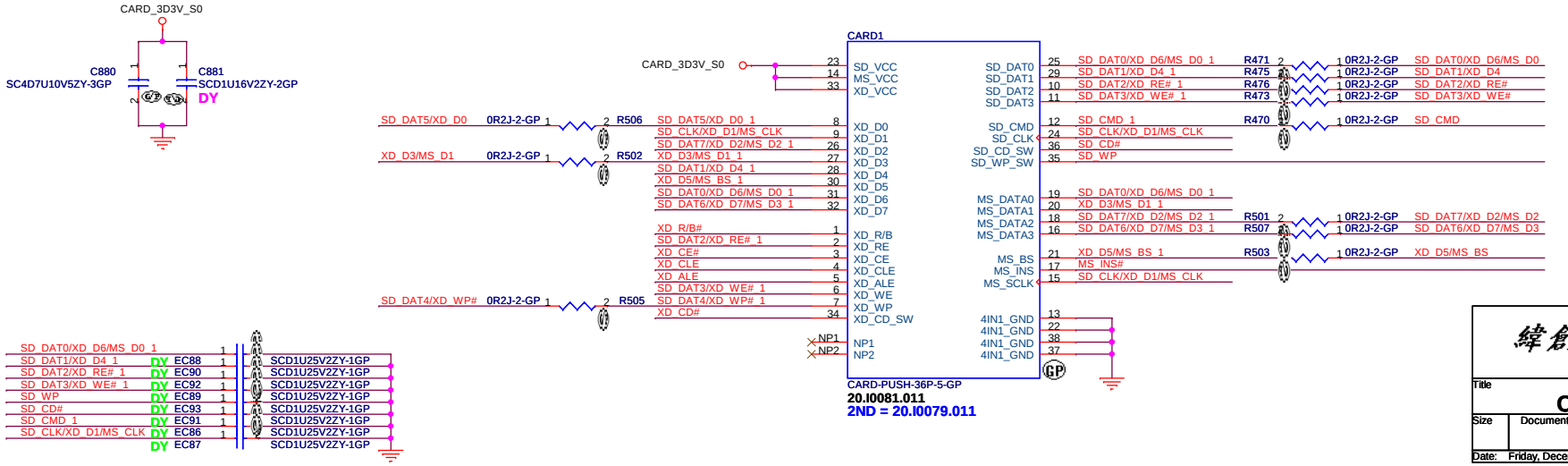
MDC 1.5 CONN



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MDC		
Size	Document Number: JV50-PU	Rev: SB
Date: Friday, December 19, 2008	Sheet 31 of 61	



5 IN1 CARD-READER (SD/MMC/MS/MS PRO/XD)



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CARDREADER- RTS5159

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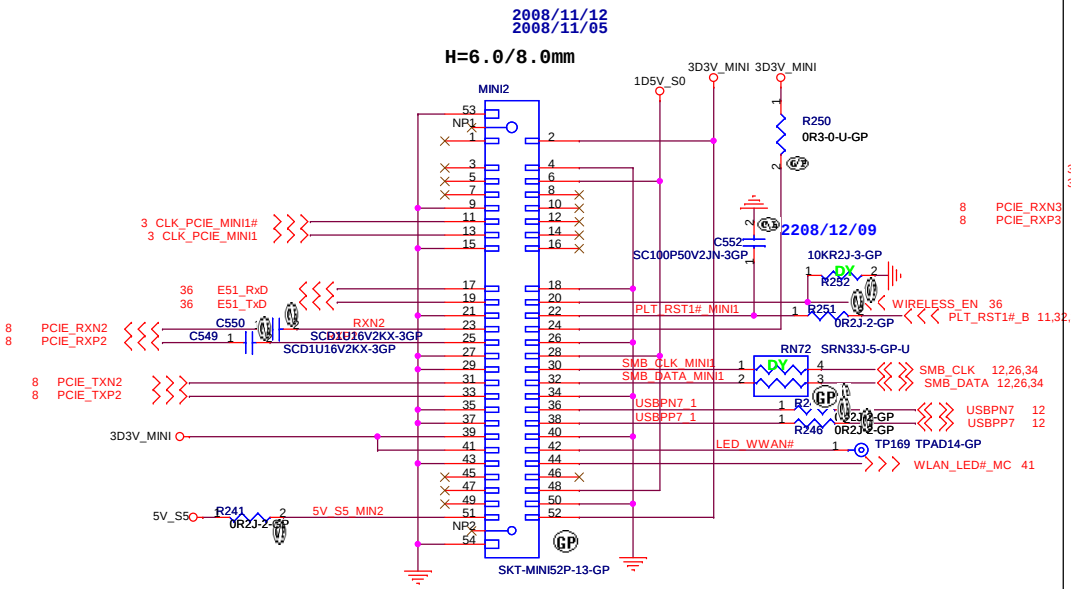
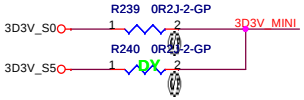
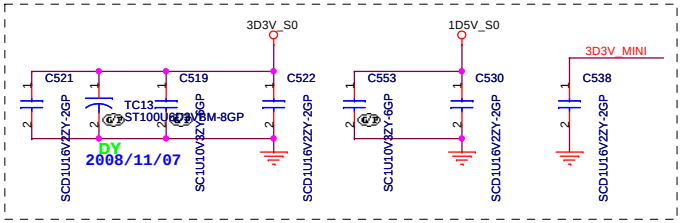
Mini Card Connector(WLAN)

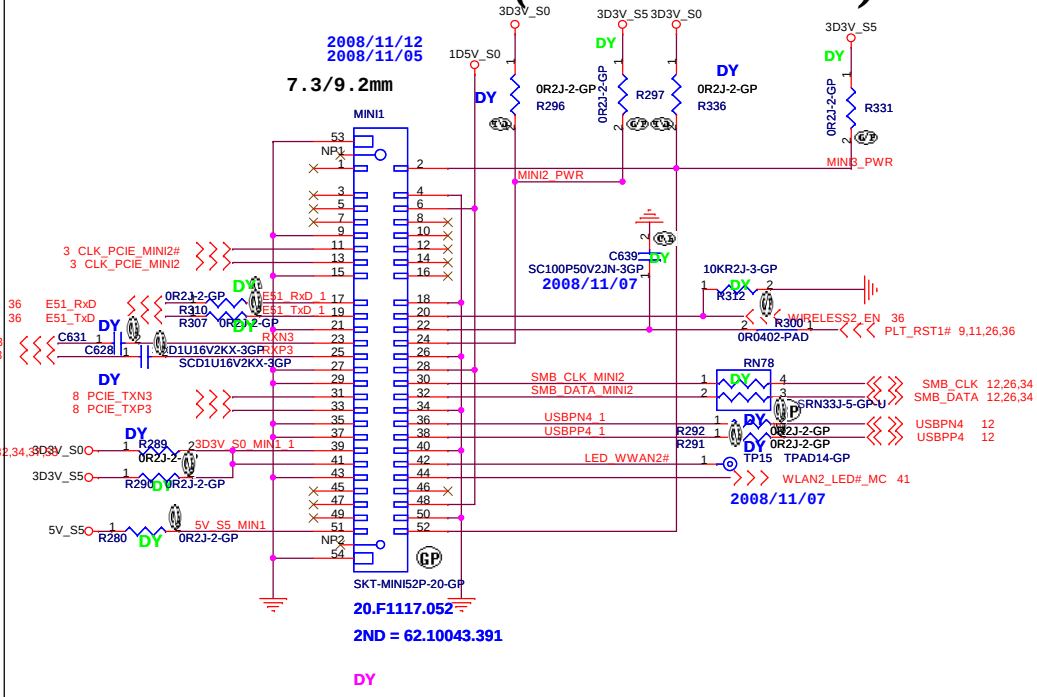




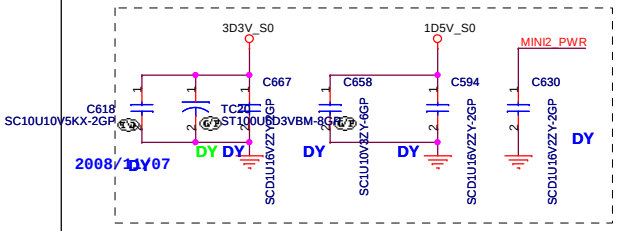
Place near MINI2



Mini Card Connector(Robson2 and 3G)



Place near MINI1



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**MINI CARD**	
Size	Document Number **JV50-PU**	Rev **SB**
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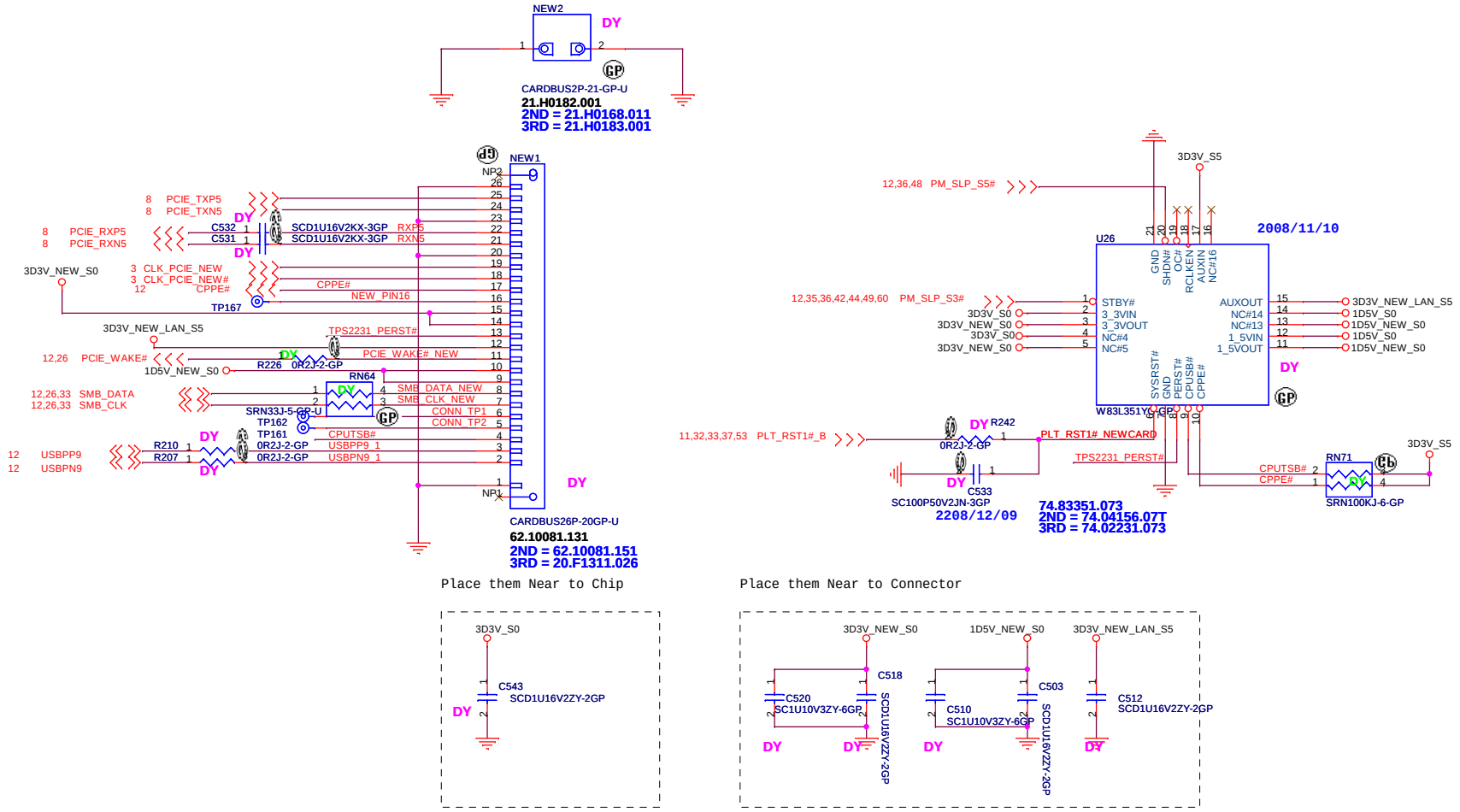
NEWCARD Connector



Place them Near to Chip

Place them Near to Connector

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**NEW CARD**	
Size	Document Number **JV50-PU**	Rev **SB**
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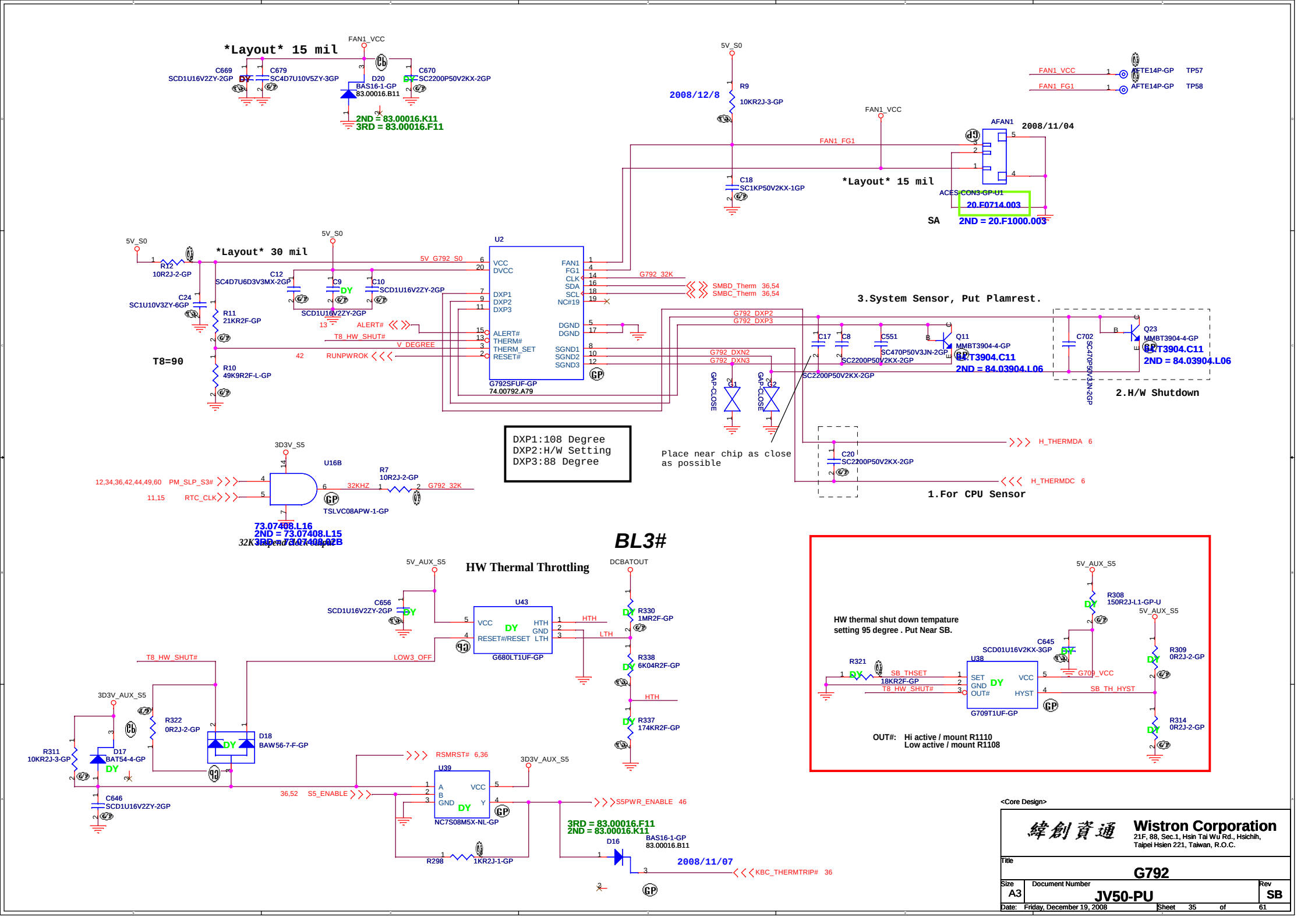
Layout 15 mil
FAN1_VCC
C669 SCD1U16V2ZY-2GP
C679 SC4D7U10V5ZY-3GP
D20 BAS16-1-GP 83.00016.B11
C670 SC2200P50V2KX-2GP
2ND = 83.00016.K11
3RD = 83.00016.F11
5V_S0
R9 10KR2J-3-GP
2008/12/8
FAN1_FG1
C18 SC1KP50V2KX-1GP
Layout 15 mil
AFAN1
2008/11/04
ACES_CON3-GP-U1
20.F0714.003
SA
2ND = 20.F1000.003
FAN1_VCC AFTE14P-GP TP57
FAN1_FG1 AFTE14P-GP TP58
Layout 30 mil
R12 10R2J-2-GP
C24 SC1U10V3ZY-6GP
R11 21KR2F-GP
R10 49K9R2F-L-GP
T8=90
C12 SC4D7U6D3V3MX-2GP
C9 DY
C10 SCD1U16V2ZY-2GP
SCD1U16V2ZY-2GP
5V_G792_S0
U2
G792SFUF-GP
74.00792.A79
FAN1
FG1
CLK
SDA
SCL
NC#19
DGND
SGND1
SGND2
SGND3
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
G792_32K
SMBD_Therm 36,54
SMBC_Therm 36,54
ALERT#
T8_HW_SHUT#
V_DEGREE
RUNPWROK
42
13
3.System Sensor, Put Plamrest.
G792_DXP2
G792_DXP3
G792_DXN2
G792_DXN3
C17
C8
C551 SC470P50V3JN-2GP
SC2200P50V2KX-2GP
Q11 MMBT3904-4-GP
MMBT3904.C11
2ND = 84.03904.L06
C702 SC470P50V3JN-2GP
Q23 MMBT3904-4GP
MMBT3904.C11
2ND = 84.03904.L06
2.H/W Shutdown
GAP-CLOSE
G1
G2
SC2200P50V2KX-2GP
C20 SC2200P50V2KX-2GP
H_THERMDA 6
H_THERMDC 6
1.For CPU Sensor
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close as possible
3D3V_S5
U16B
TSLVC08APW-1-GP
12,34,36,42,44,49,60 PM_SLP_S3#
11,15 RTC_CLK
R7 10R2J-2-GP
32KHZ
G792_32K
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
32K suspend clock output
BL3#
HW Thermal Throttling
5V_AUX_S5
DCBATOUT
C656 SCD1U16V2ZY-2GP
U43
G680LT1UF-GP
VCC
RESET#/RESET
HTH
GND
LTH
R330 1MR2F-GP
R338 6K04R2F-GP
R337 174KR2F-GP
T8_HW_SHUT#
LOW3_OFF
3D3V_AUX_S5
R322 0R2J-2-GP
D18 BAW56-7-F-GP
R311 10KR2J-3-GP
D17 BAT54-4-GP
C646 SCD1U16V2ZY-2GP
RSMRST# 6,36
36,52 S5_ENABLE
U39
NC7S08M5X-NL-GP
A
B
GND
VCC
Y
S5PWR_ENABLE 46
3RD = 83.00016.F11
2ND = 83.00016.K11
D16 BAS16-1-GP 83.00016.B11
R298 1KR2J-1-GP
2008/11/07
KBC_THERMTRIP# 36
HW thermal shut down tempature setting 95 degree . Put Near SB.
R321 18KR2F-GP
SB_THSET
T8_HW_SHUT#
U38
G709T1UF-GP
SET
GND
OUT#
VCC
HYST
C645 SCD01U16V2KX-3GP
G709_VCC
SB_TH_HYST
R308 150R2J-L1-GP-U
R309 0R2J-2-GP
R314 0R2J-2-GP
OUT#: Hi active / mount R1110
Low active / mount R1108
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G792
Size A3
Document Number JV50-PU
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Date: Friday, December 19, 2008
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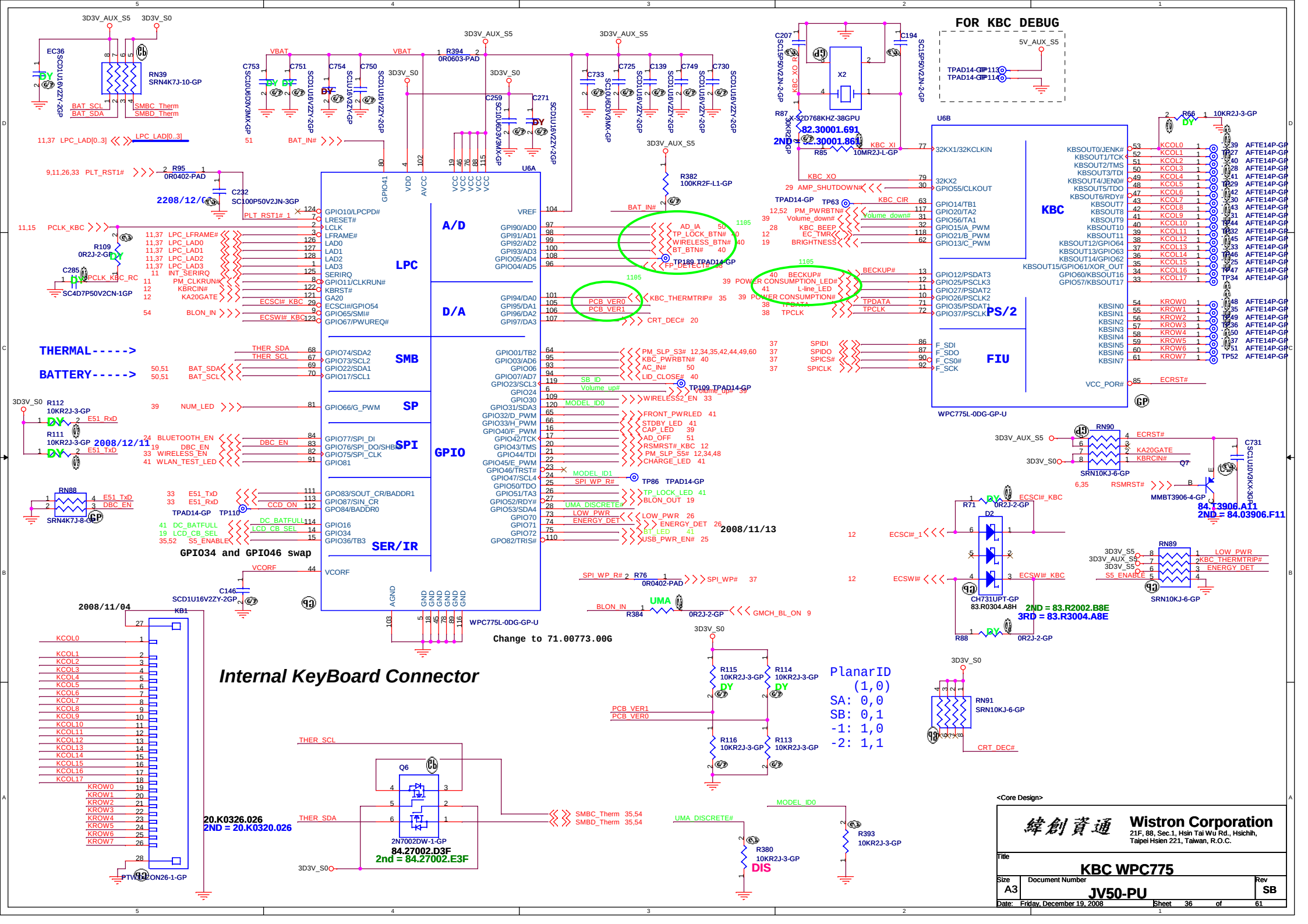
FOR KBC DEBUG
U6A
WPC775L-0DG-GP-U
U6B
WPC775L-0DG-GP-U
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
KBC
PS/2
FIU
THERMAL----->
BATTERY----->
GPIO034 and GPIO046 swap
2008/12/11
2008/11/04
2008/11/13
Change to 71.00773.00G
Internal KeyBoard Connector
UMA
DIS
PlanarID
(1,0)
SA: 0,0
SB: 0,1
-1: 1,0
-2: 1,1
82.30001.691
2ND = 82.30001.861
84.T3906.A11
2ND = 84.03906.F11
2ND = 83.R2002.B8E
3RD = 83.R3004.A8E
20.K0326.026
2ND = 20.K0320.026
84.27002.D3F
2nd = 84.27002.E3F
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC775
JV50-PU
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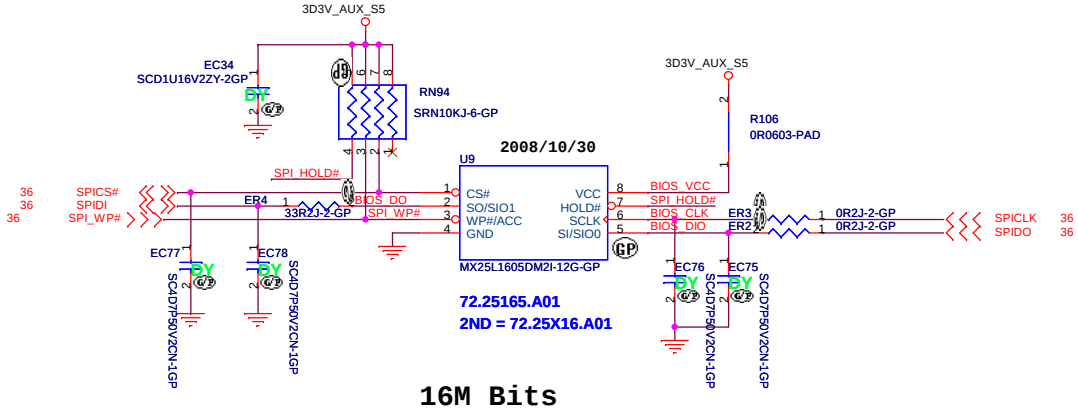
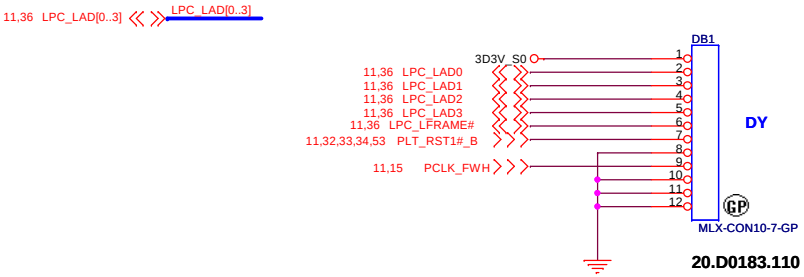


16M Bits
SPI FLASH ROM

GOLDEN FINGER FOR DEBUG BOARD



<Core Design>

緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS		
Size: A3	Document Number: JV50-PU	Rev: SB
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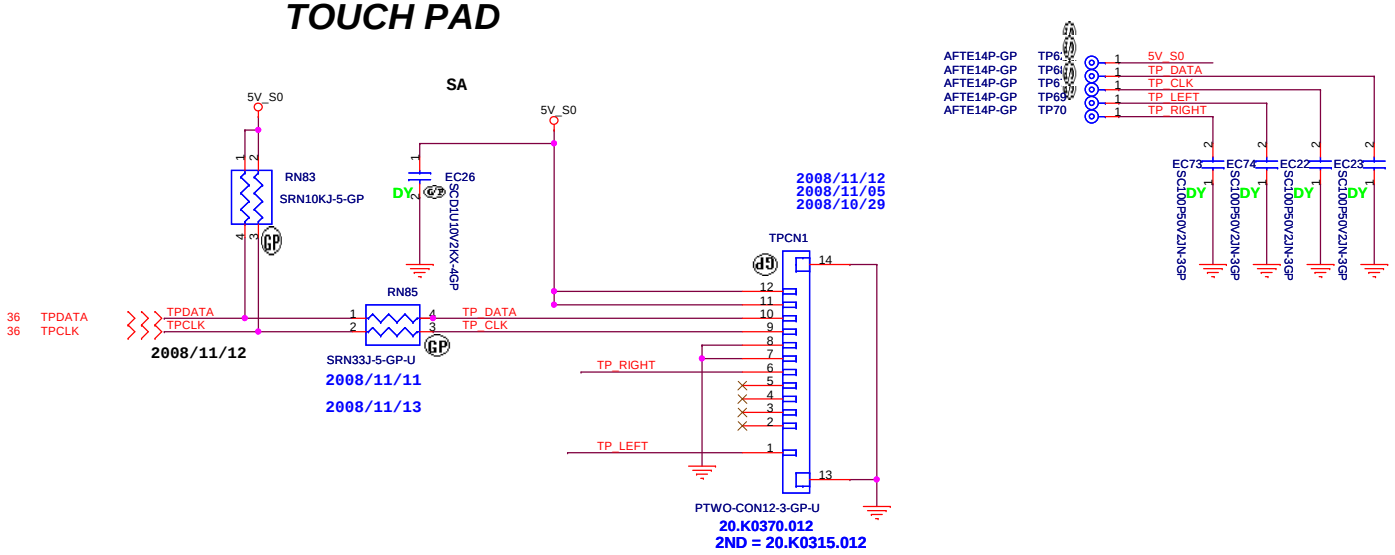
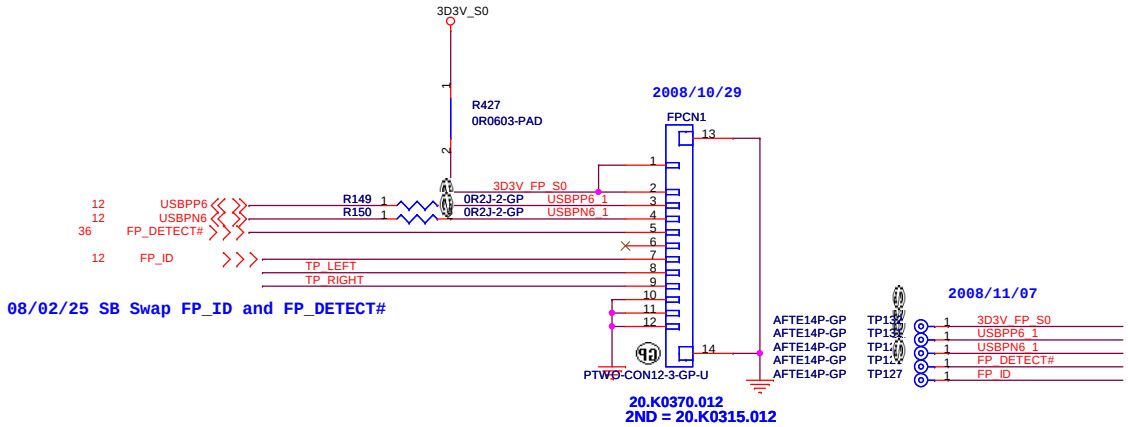
TOUCH PAD



Finger printer



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: Touch PAD/Finger printer

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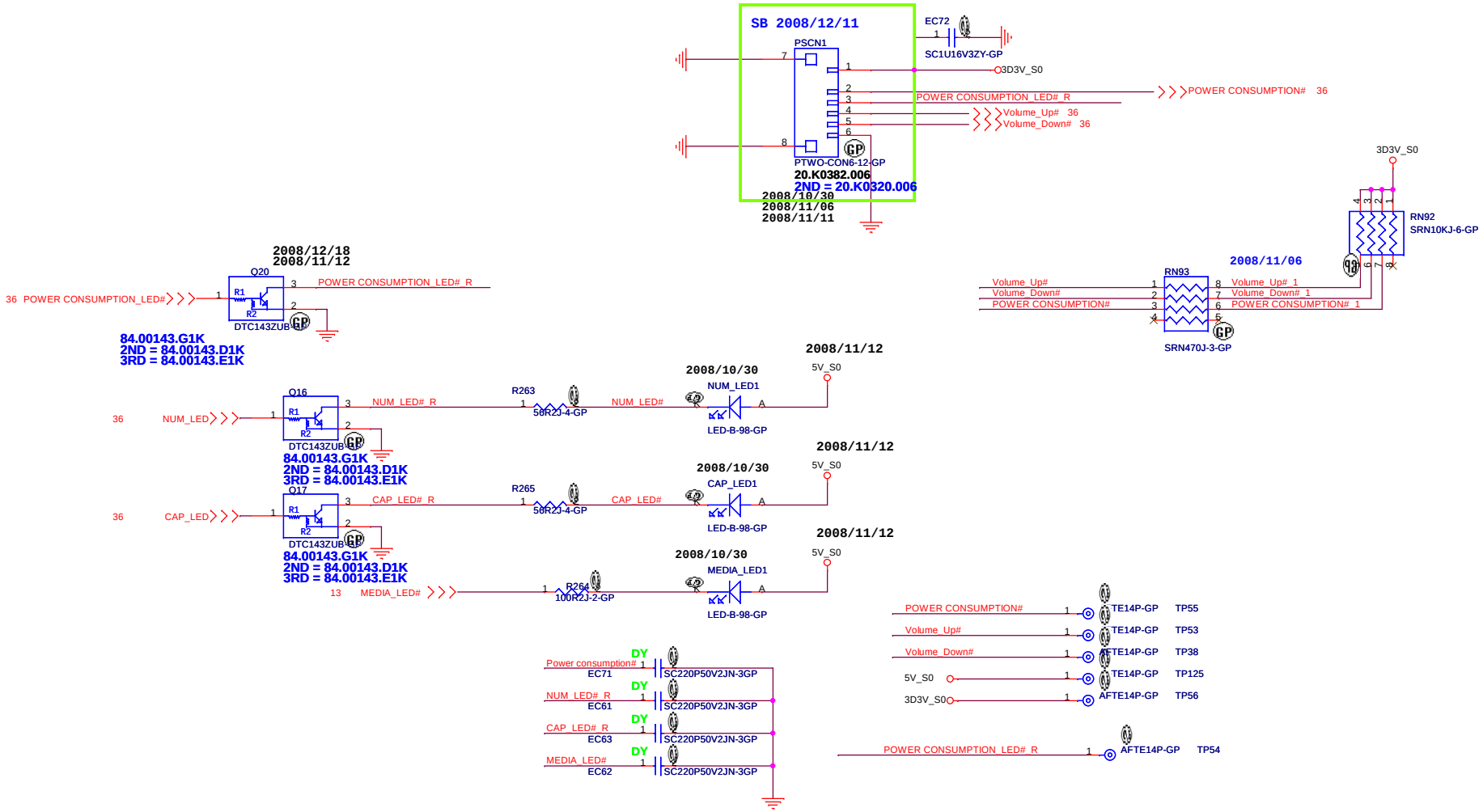

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: LAUNCH BOARD		
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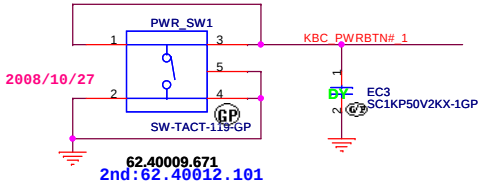
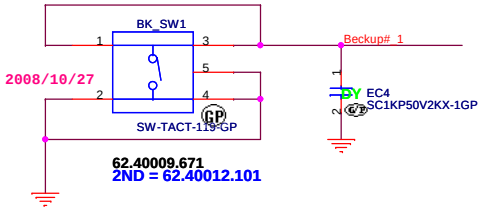
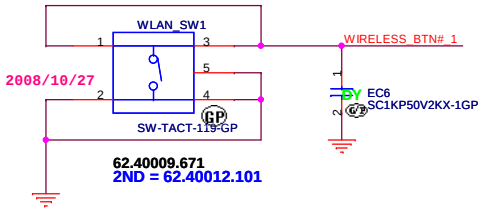
Power Button



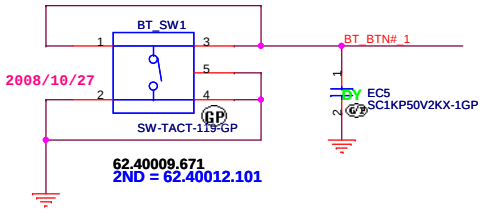
Beckup Button



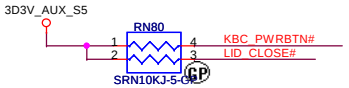
WIRELESS Button

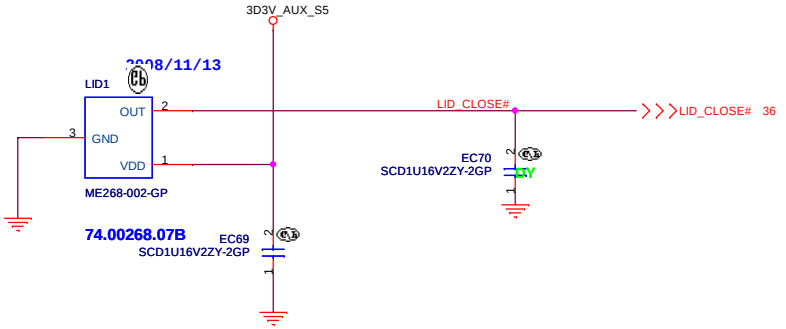


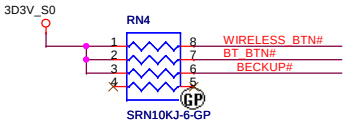
BT/3G Button

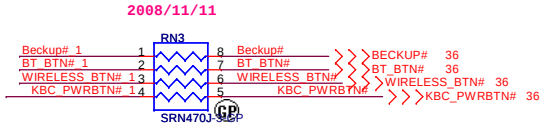


Cover Up Switch

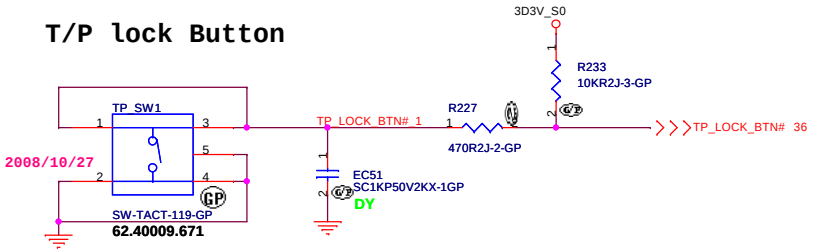








T/P lock Button



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: SWITCH		
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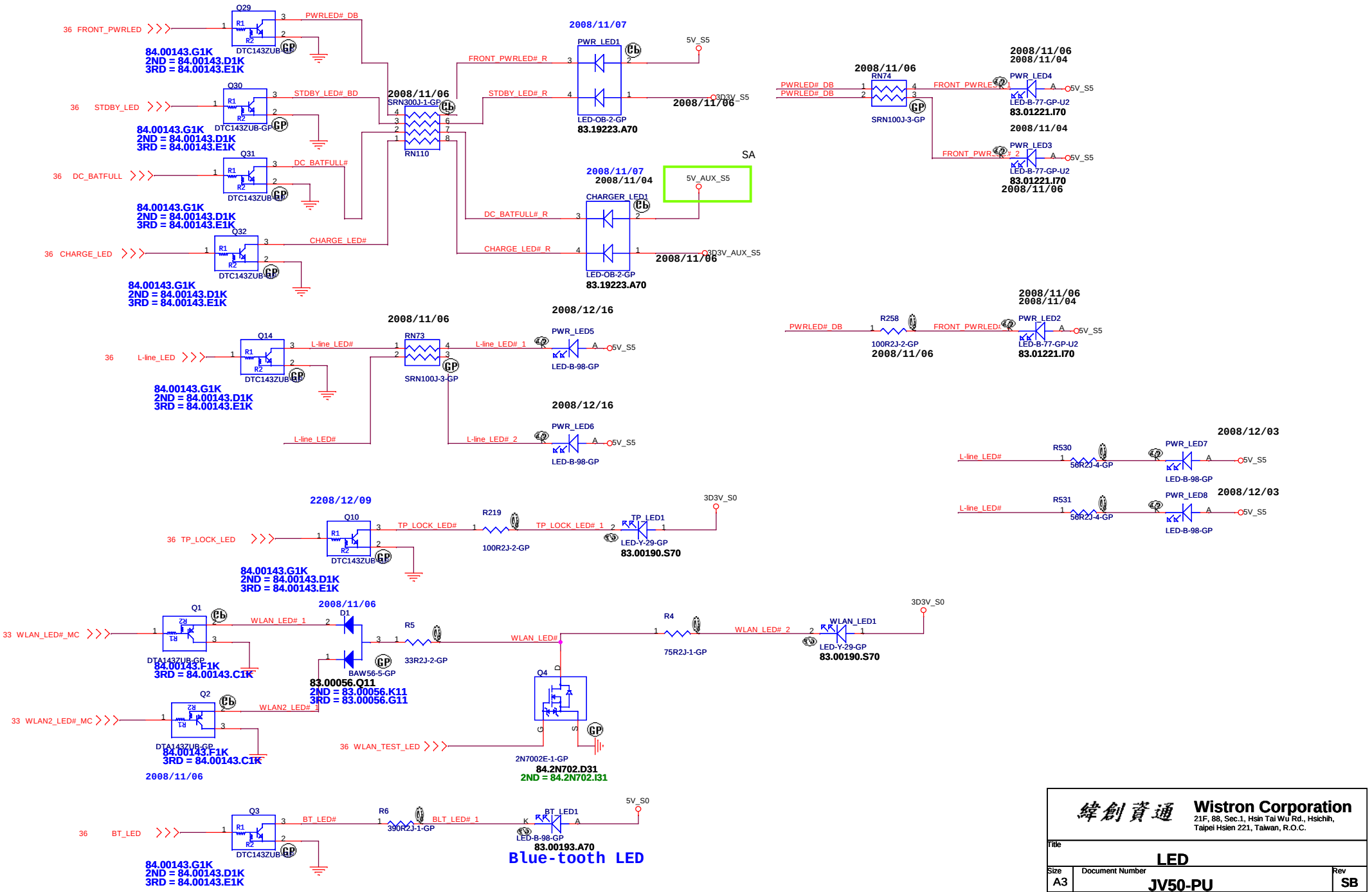

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: LED		
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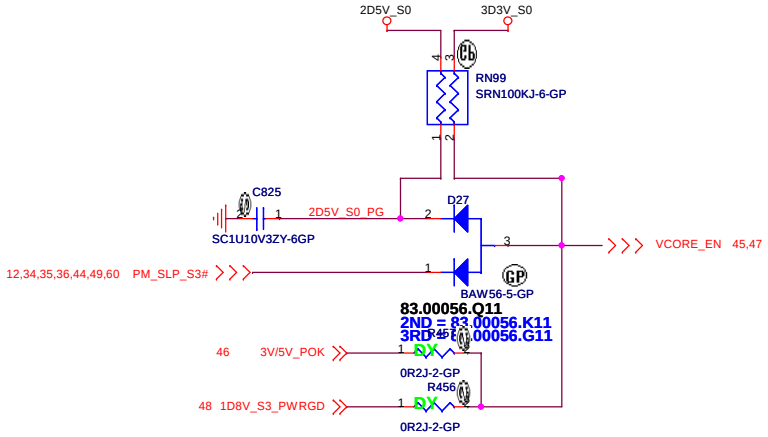
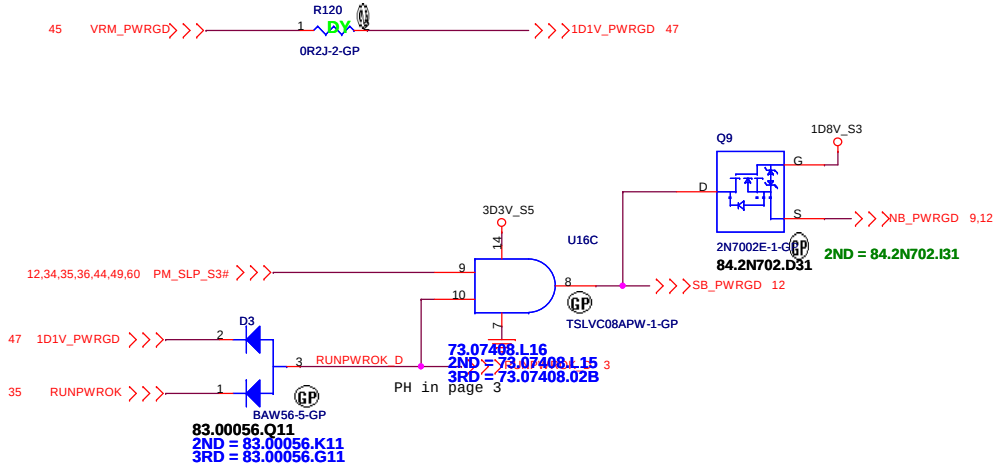


P/H @ 1D8V_S3 PAGE



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	POWER ON LOGIC	
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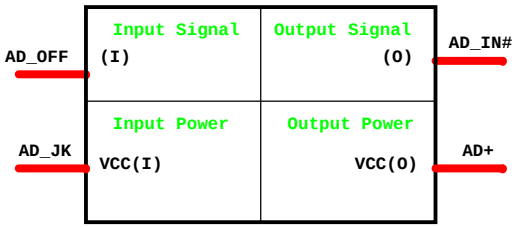
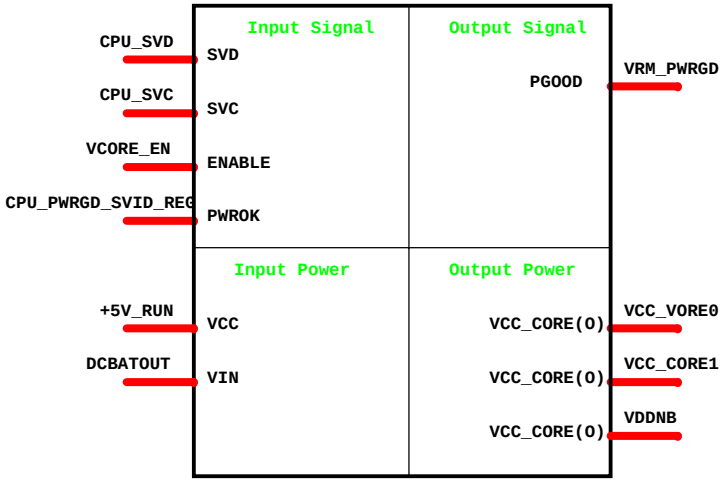
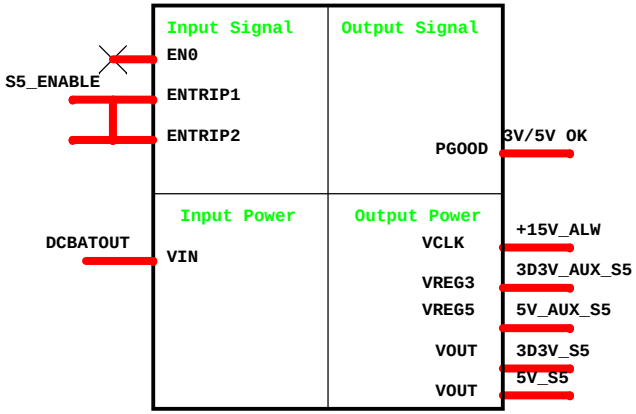
Adapter



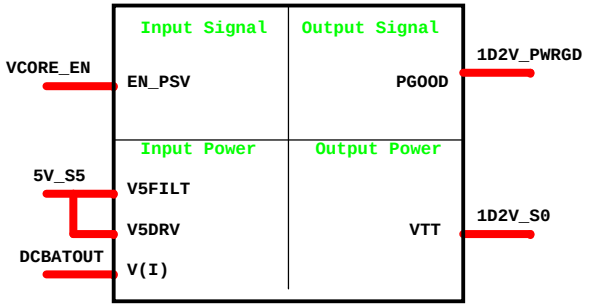
CPU_CORE
ISL6265HRTZ



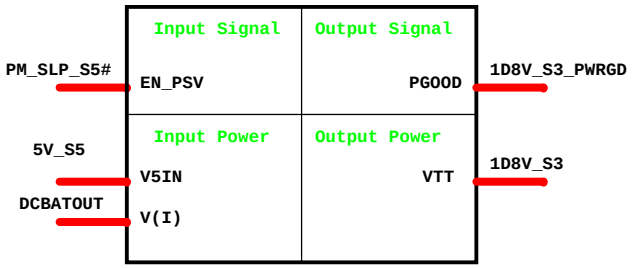
DCDC 5V/3D3V(TPS51125)



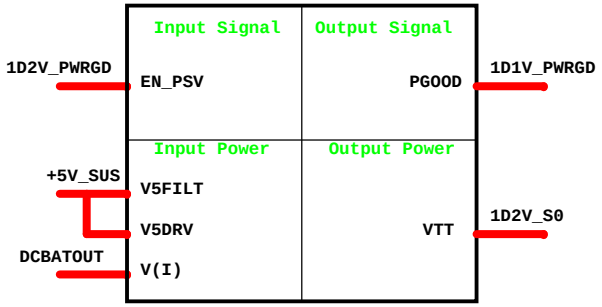
DCDC 1D2V(RT8202)



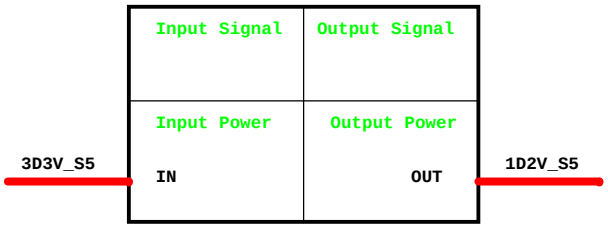
DCDC 1D8V(RT8202)



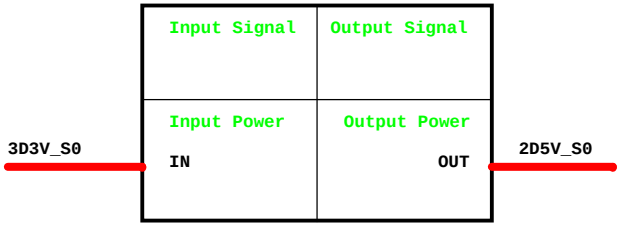
DCDC 1D1V(RT8202)



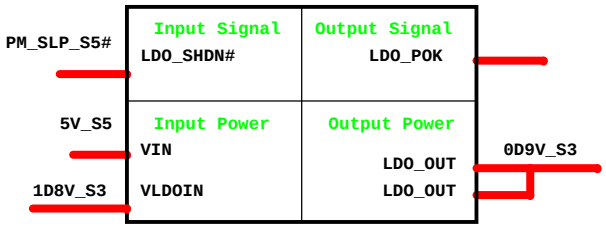
1D2V LDO G9161



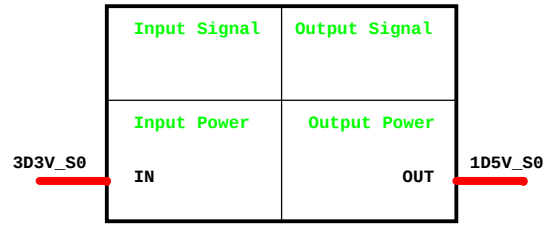
2D5V LDO R9161



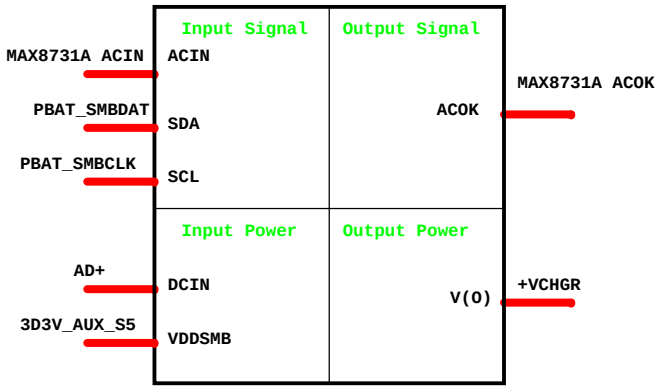
0D9V LDO RT9026



1D5V LDO G9571



CHARGER MAX8731



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
A3	JV50-PU	SB

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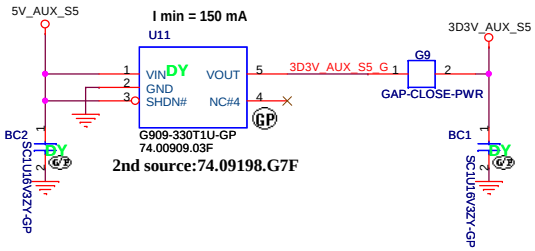
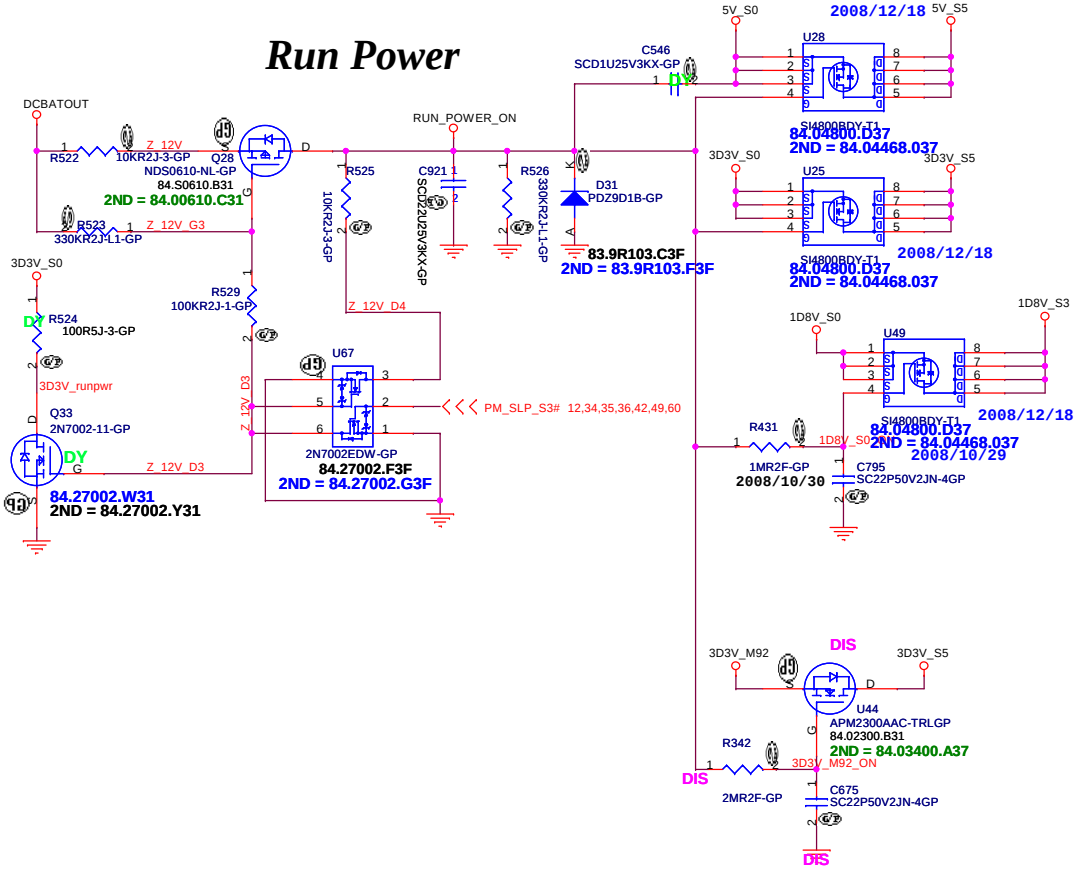
Aux Power 3D3V_AUX_S5



Run Power



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN AND AUX POWER**

Size	Document Number	Rev
A3	JV50-PU	SB

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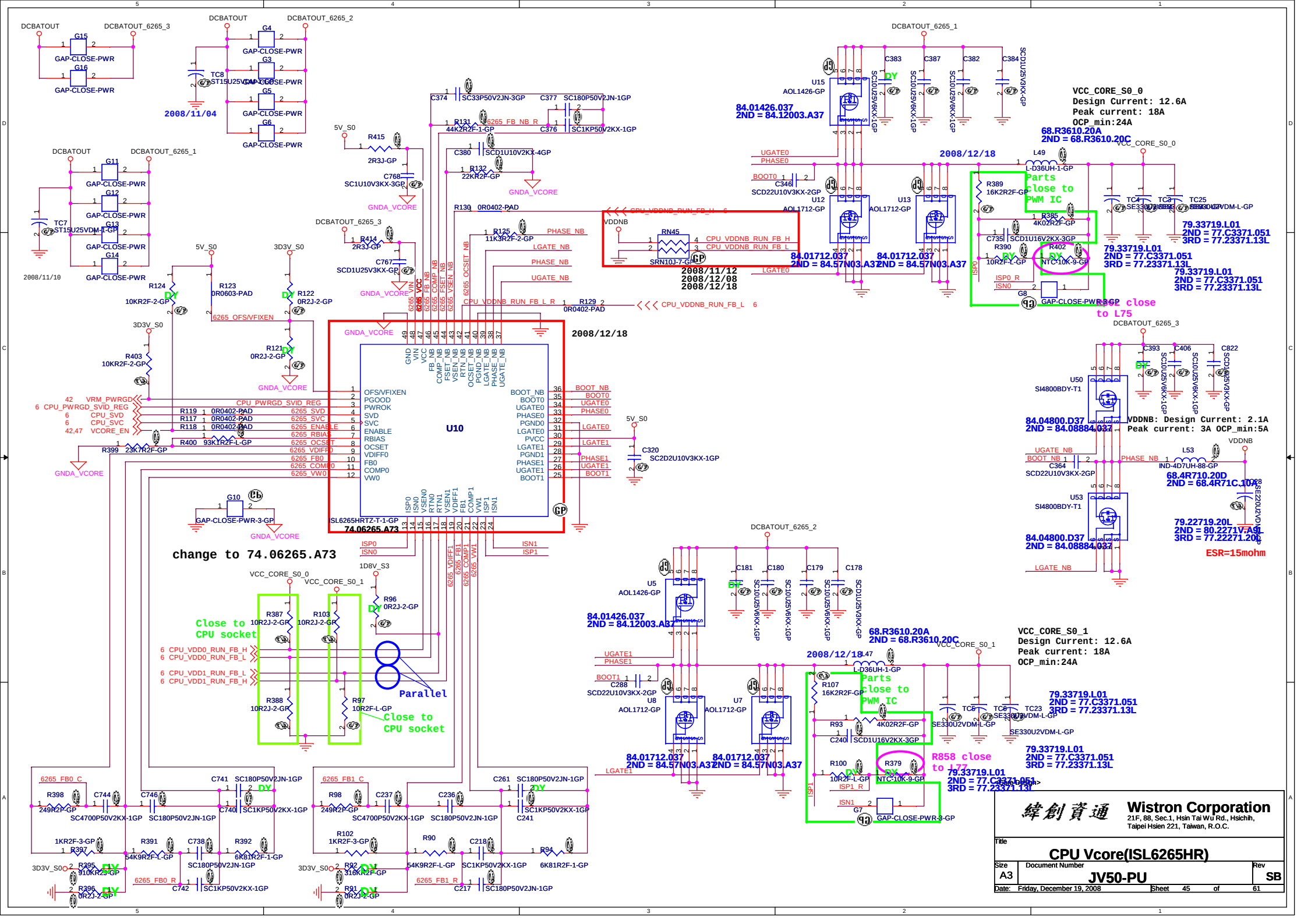
U10
SL6265HRTZ-T-1-GP
74.06265.A73
change to 74.06265.A73
U15
AOL1426-GP
U12
AOL1712-GP
U13
AOL1712-GP
U5
AOL1426-GP
U8
AOL1712-GP
U7
AOL1712-GP
U50
SI4800BDY-T1
U53
SI4800BDY-T1
VCC_CORE_S0_0
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VCC_CORE_S0_1
Design Current: 12.6A
Peak current: 18A
OCP_min:24A
VDDNB: Design Current: 2.1A
Peak current: 3A OCP_min:5A
2008/12/18
2008/11/04
2008/11/10
2008/11/12
2008/12/08
2008/12/18
Close to CPU socket
Parallel
Parts close to PWM IC
R858 close to L77
R3610 close to L75
ESR=15mohm
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CPU Vcore(ISL6265HR)
JV50-PU
Size A3
Rev SB
Date: Friday, December 19, 2008
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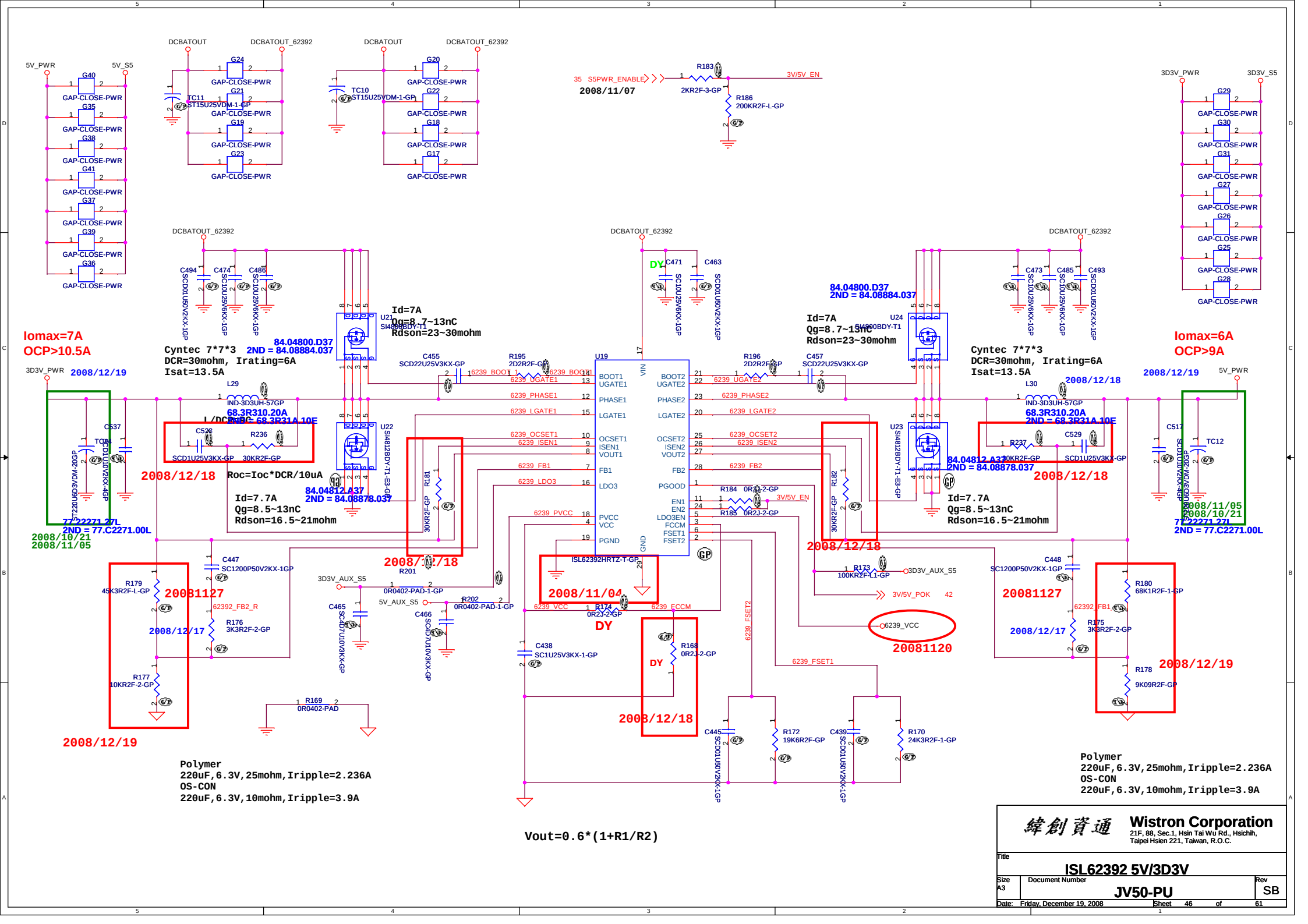
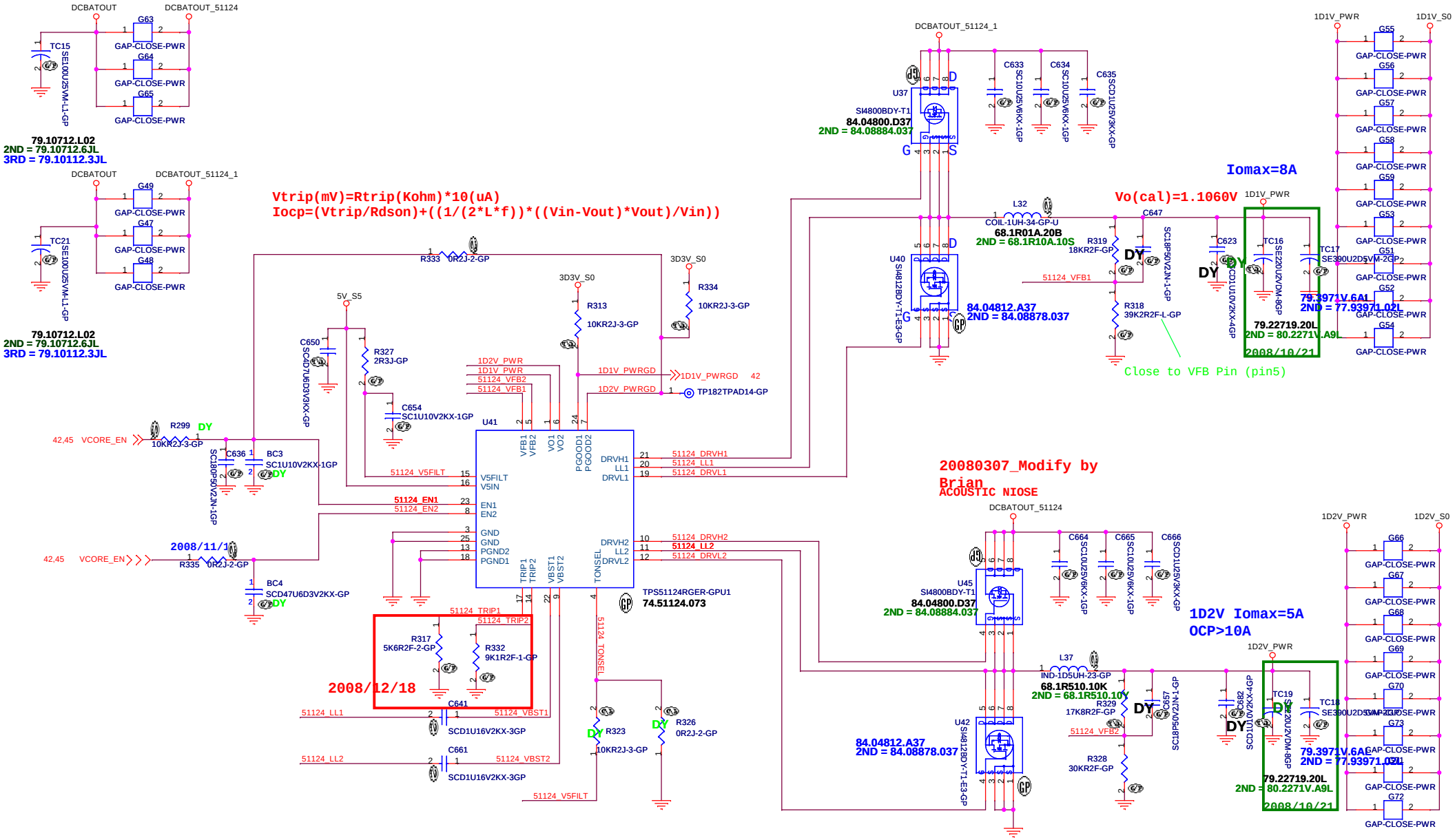

5V_PWR
5V_S5
DCBATOUT
DCBATOUT_62392
GAP-CLOSE-PWR
35 S5PWR_ENABLE
2008/11/07
R183
2KR2F-3-GP
3V/5V_EN
R186
200KR2F-L-GP
3D3V_PWR
3D3V_S5
Iomax=7A
OCP>10.5A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
84.04800.D37
2ND = 84.08884.037
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
L29
IND-3D3UH-57GP
68.3R310.20A
2ND = 68.3R31A.10E
2008/12/19
2008/12/18
Roc=Ioc*DCR/10uA
Id=7.4A
Qg=8.5~13nC
Rdson=16.5~21mohm
84.04812.A37
2ND = 84.08878.037
77.22271.27L
2ND = 77.C2271.00L
2008/10/21
2008/11/05
ISL62392HRTZ-T-GP
U19
BOOT1
UGATE1
PHASE1
LGATE1
OCSET1
ISEN1
VOUT1
FB1
LDO3
PVCC
VCC
PGND
BOOT2
UGATE2
PHASE2
LGATE2
OCSET2
ISEN2
VOUT2
FB2
PGOOD
EN1
EN2
LDO3EN
FCCM
FSET1
FSET2
VIN
GND
6239_BOOT1
6239_UGATE1
6239_PHASE1
6239_LGATE1
6239_OCSET1
6239_ISEN1
6239_FB1
6239_LDO3
6239_PVCC
6239_BOOT2
6239_UGATE2
6239_PHASE2
6239_LGATE2
6239_OCSET2
6239_ISEN2
6239_FB2
3V/5V_EN
6239_VCC
6239_FCCM
6239_FSET1
3V/5V_POK
42
20081127
2008/12/17
2008/12/19
2008/11/04
DY
20081120
3D3V_AUX_S5
5V_AUX_S5
Vout=0.6*(1+R1/R2)
Polymer
220uF,6.3V,25mohm,Iripple=2.236A
OS-CON
220uF,6.3V,10mohm,Iripple=3.9A
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL62392 5V/3D3V
Size
A3
Document Number
JV50-PU
Rev
SB
Date: Friday, December 19, 2008
Sheet 46 of 61



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

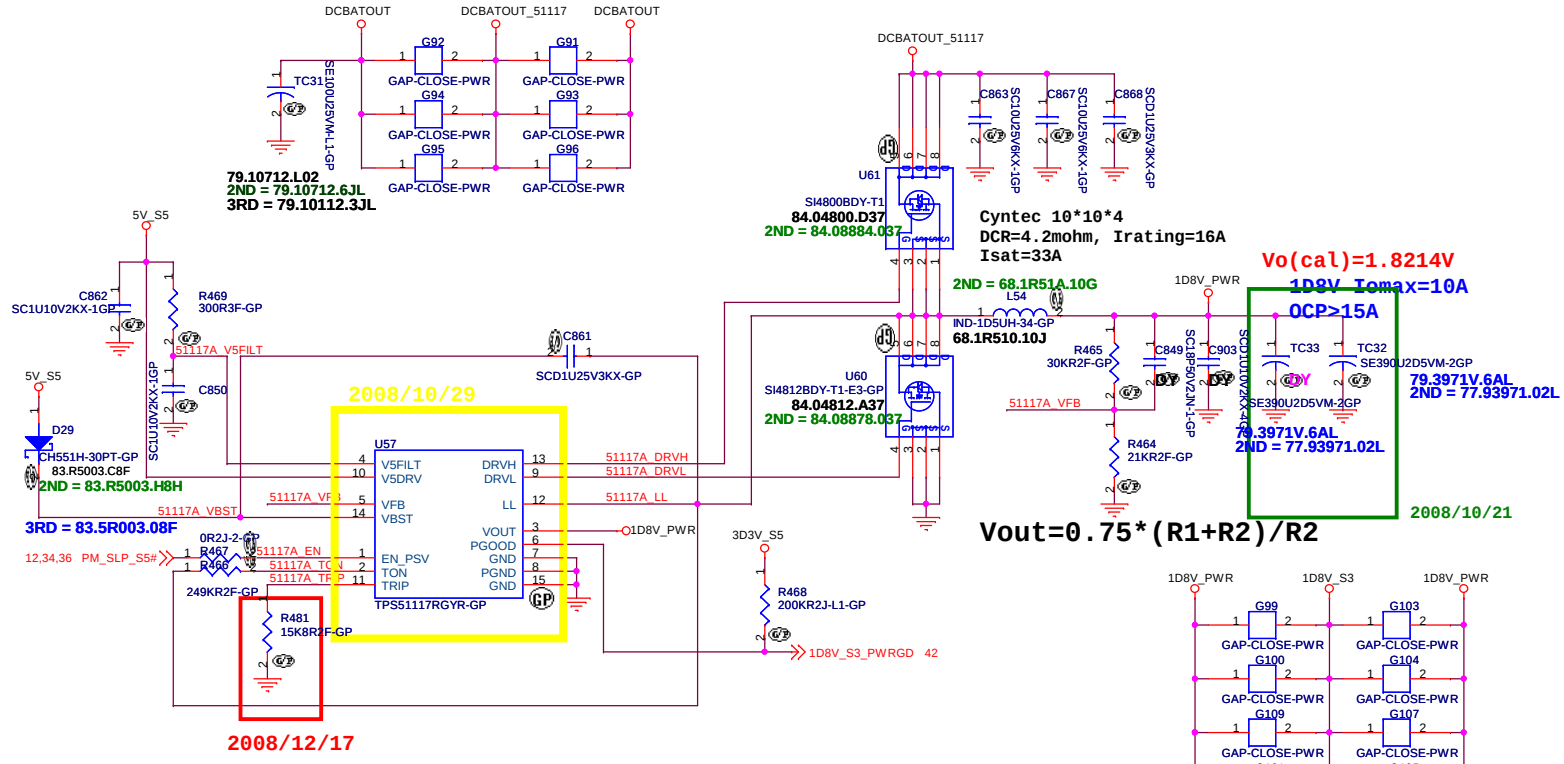
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D1V_1D2V

Size	Document Number	Rev
A3	JV50-PU	SB

Date: Friday, December 19, 2008 Sheet 47 of 61



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DCDC_1D8V_TPS51117/LDO_0D9V

Size	Document Number	Rev
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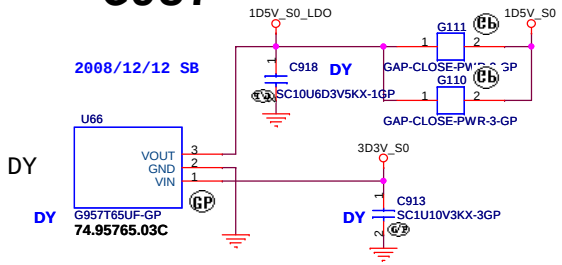
Date: Friday, December 19, 2008 Sheet 48 of 61

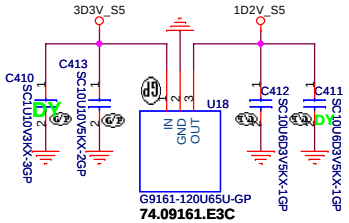
1D5V_S0
Iomax=1A

G957



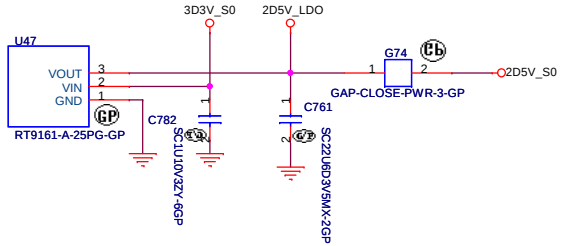
For MINI Card.NEW Card power SW

1D2V_S5
Iomax=400mA



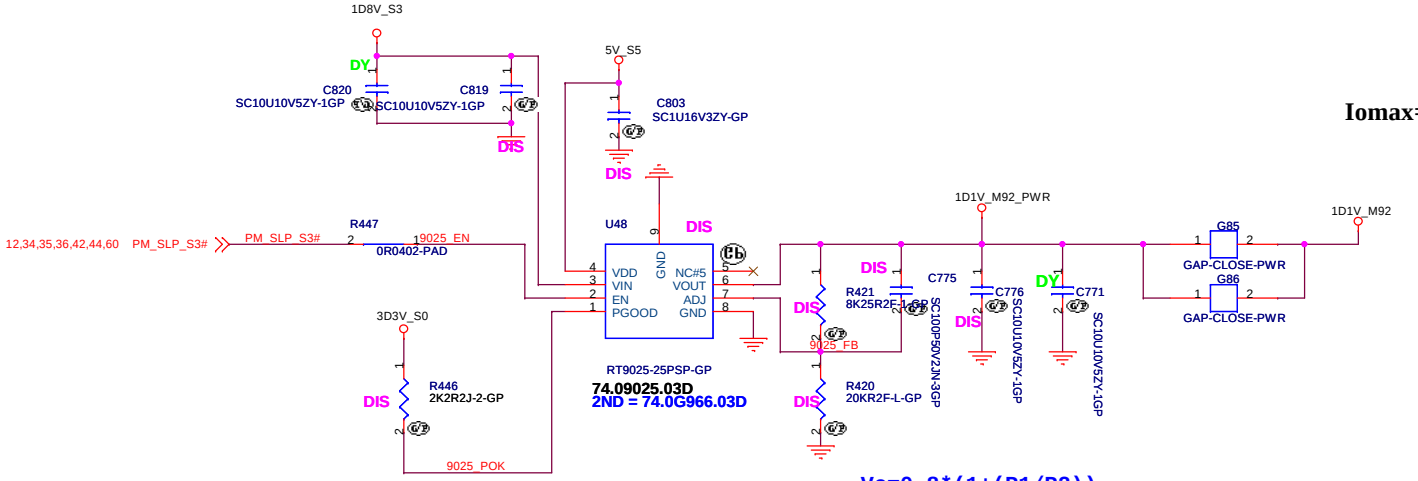
Place near to SB700

2D5V
Iomax=0.2A



Place near to CPU

Iomax=0.8A



Vo=0.8*(1+(R1/R2))

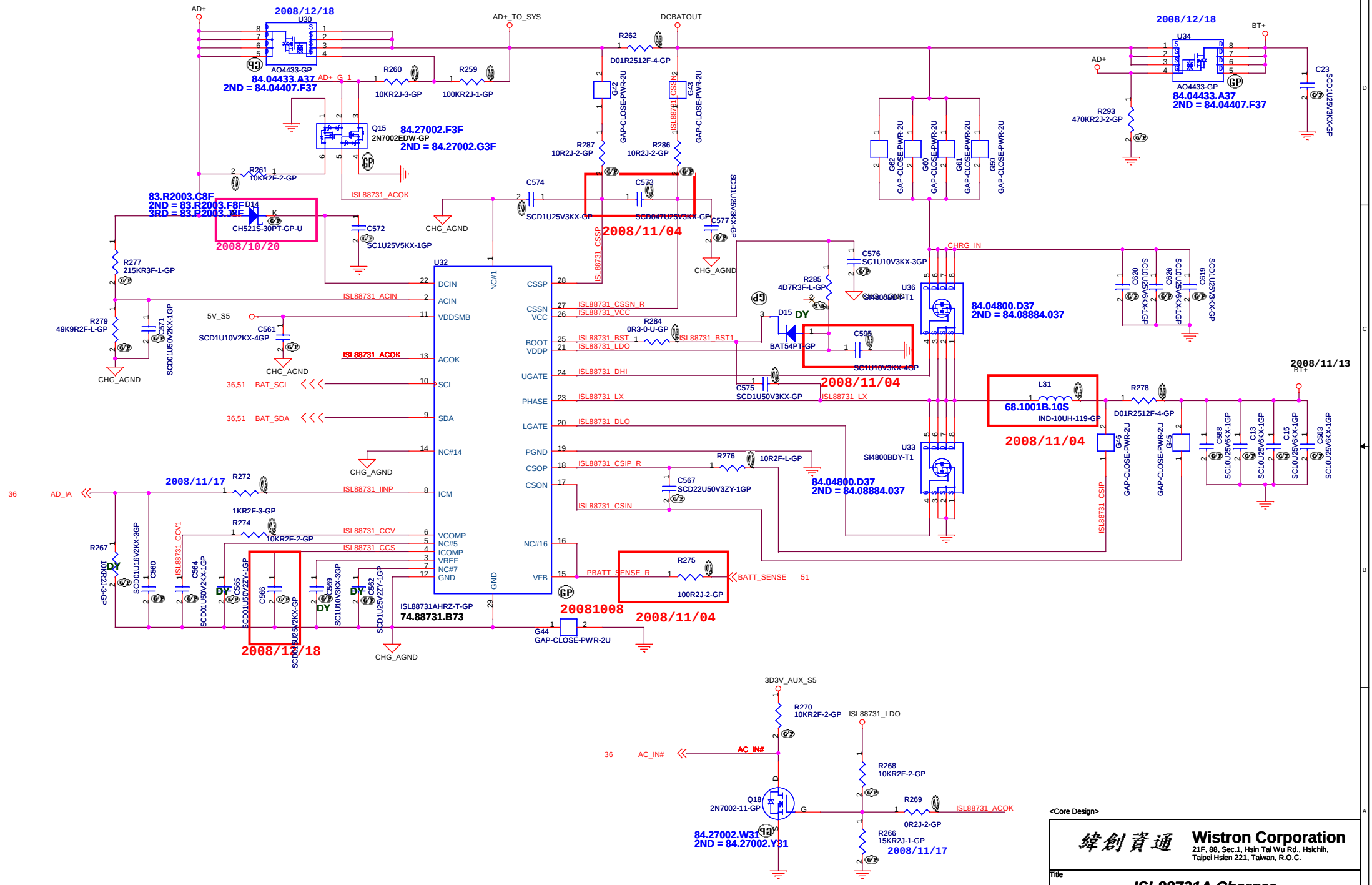
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LDO 2D5V/1D5V/1D2V_S5

Size: A3 | Document Number: JV50-PU | Rev: SB

Date: Friday, December 19, 2008 | Sheet 49 of 61


AD+
2008/12/18
U30
AO4433-GP
84.04433.A37
2ND = 84.04407.F37
AD+_TO_SYS
DCBATOUT
R262
D01R2512F-4-GP
R260
10KR2J-3-GP
R259
100KR2J-1-GP
Q15
2N7002EDW-GP
84.27002.F3F
2ND = 84.27002.G3F
R261
10KR2F-2-GP
ISL88731_ACOK
83.R2003.C8F
2ND = 83.R2003.F8F
3RD = 83.R2003.J8F
D14
CH521S-30PT-GP-U
2008/10/20
C572
SC1U25V5KX-1GP
CHG_AGND
C574
SCD1U25V3KX-GP
C573
SCD047U25V3KX-GP
C577
R287
10R2J-2-GP
R286
10R2J-2-GP
2008/11/04
G42
G43
GAP-CLOSE-PWR-2U
ISL88731_CSSP
ISL88731_CSSN
R277
215KR3F-1-GP
R279
49K9R2F-L-GP
C571
SCD01U50V2KX-1GP
5V_S5
C561
SCD1U10V2KX-4GP
U32
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
NC#1
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ISL88731AHRZ-T-GP
74.88731.B73
ISL88731_ACIN
ISL88731_CSSN_R
ISL88731_VCC
ISL88731_BST
ISL88731_BST1
ISL88731_LDO
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
ISL88731_IINP
ISL88731_CCV
ISL88731_CCS
PBATT_SENSE_R
BAT_SCL
BAT_SDA
R284
0R3-0-U-GP
R285
4D7R3F-L-GP
D15
DY
BAT54PT-GP
C575
SCD1U50V3KX-GP
C576
SC1U10V3KX-3GP
C595
SC1U10V3KX-4GP
CHRG_IN
U36
SI4800BDY-T1
U33
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
2008/11/04
L31
68.1001B.10S
IND-10UH-119-GP
R278
D01R2512F-4-GP
2008/11/13
BT+
C568
C13
C15
C563
SC10U25V6KX-1GP
R276
10R2F-L-GP
C567
SCD22U50V3ZY-1GP
R275
100R2J-2-GP
BATT_SENSE
51
20081008
2008/11/04
G44
GAP-CLOSE-PWR-2U
R272
1KR2F-3-GP
R274
10KR2F-2-GP
R267
10KR2J-3-GP
DY
SCD01U16V2KX-3GP
C560
C564
SCD01U50V2KX-1GP
C565
SCD01U50V2ZY-1GP
C566
SCD1U25V2KX-GP
C569
SC1U10V3KX-3GP
C562
SCD1U25V2ZY-1GP
2008/12/18
CHG_AGND
AD_IA
36
ISL88731_CCV1
3D3V_AUX_S5
R270
10KR2F-2-GP
AC_IN#
36
R268
10KR2F-2-GP
Q18
2N7002-11-GP
R269
0R2J-2-GP
R266
15KR2J-1-GP
84.27002.W31
2ND = 84.27002.Y31
2008/11/17
U34
AO4433-GP
84.04433.A37
2ND = 84.04407.F37
R293
470KR2J-2-GP
C23
SCD1U25V3KX-GP
G62
G60
G61
G50
GAP-CLOSE-PWR-2U
C620
C626
C619
SCD1U25V3KX-1GP
G46
G45
GAP-CLOSE-PWR-2U
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A Charger
Size
A3
Document Number
JV50-PU
Rev
SB
Date: Friday, December 19, 2008
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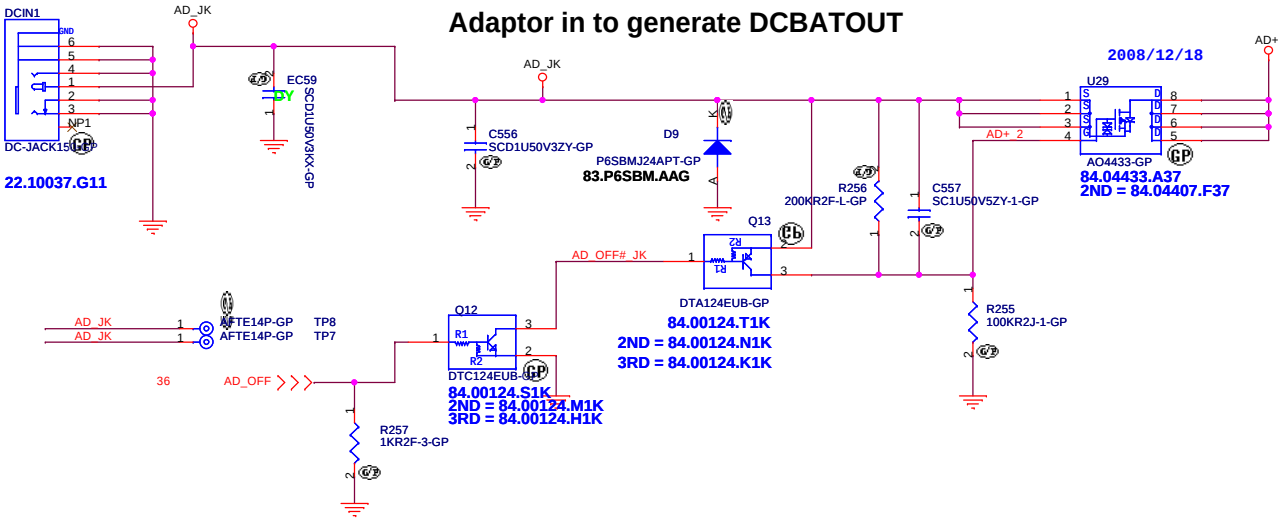
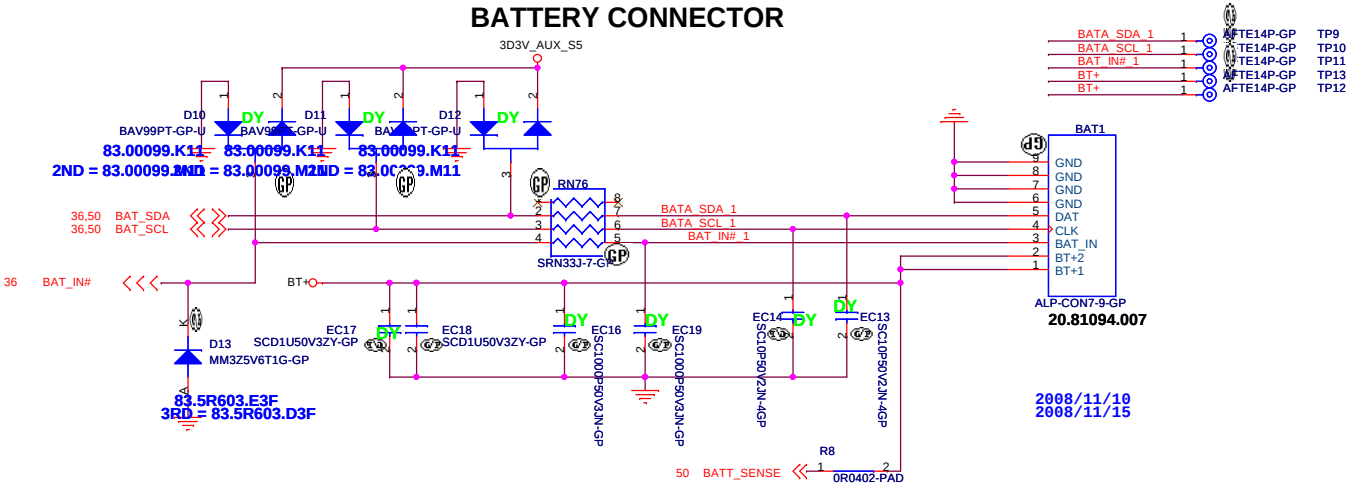
2008/11/06
2008/10/29

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	AD/BATT CONN	
Size	Document Number JV50-PU	Rev SB
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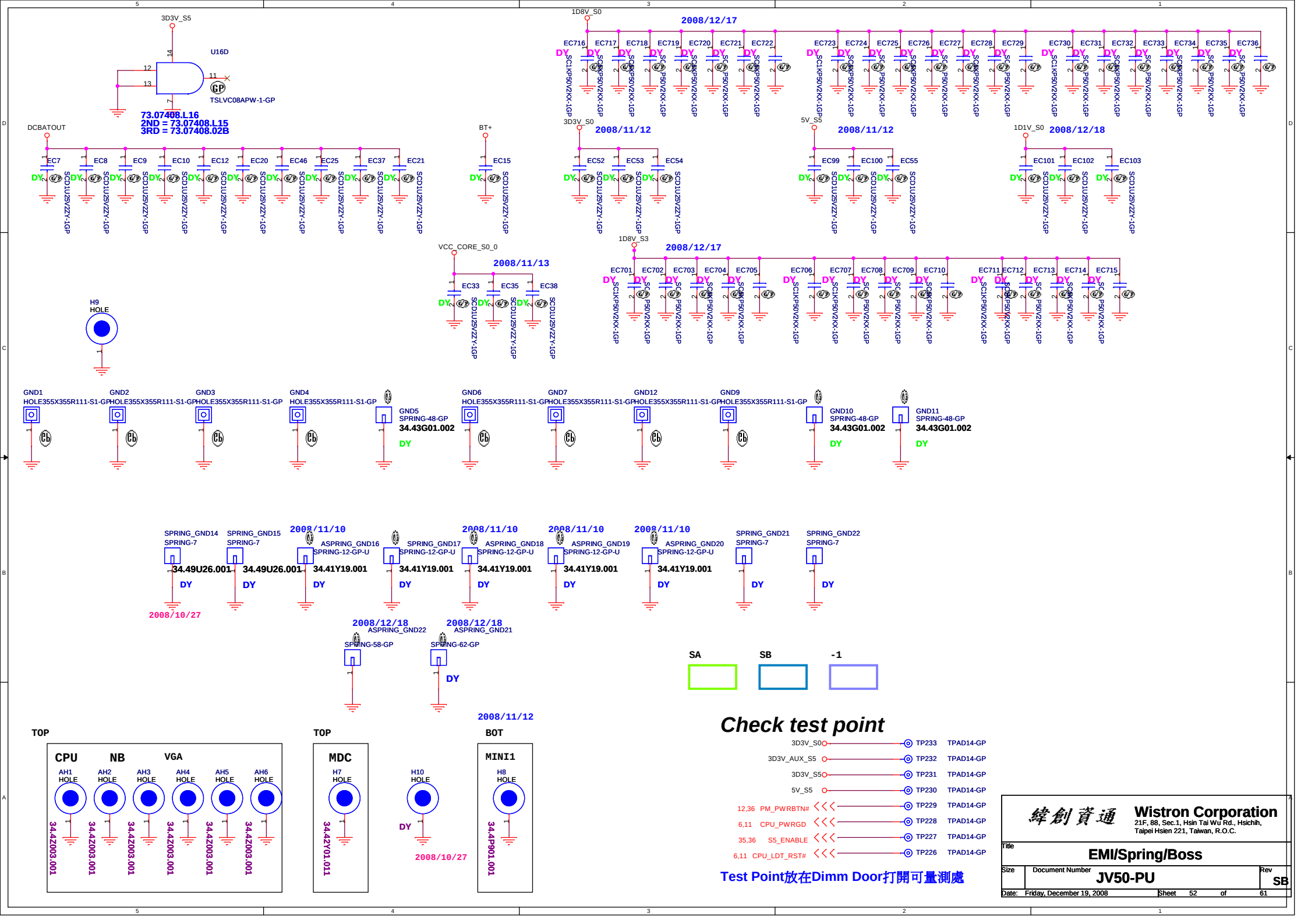
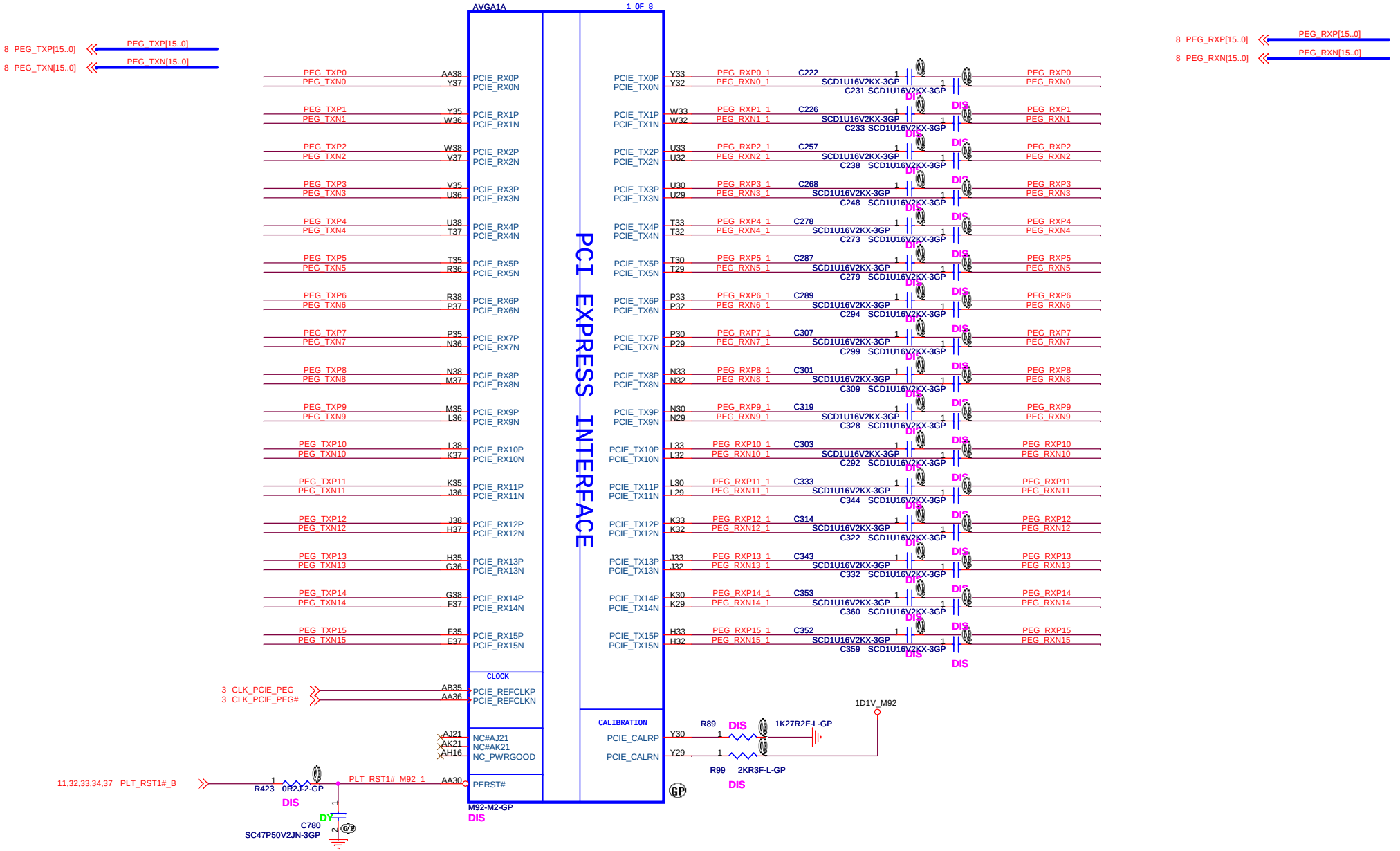

3D3V_S5
U16D
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
1D8V_S0
2008/12/17
EC716 EC717 EC718 EC719 EC720 EC721 EC722
EC723 EC724 EC725 EC726 EC727 EC728 EC729
EC730 EC731 EC732 EC733 EC734 EC735 EC736
SC1KP50V2KX-1GP
SC4K7P50V2KX-1GP
DCBATOUT
EC7 EC8 EC9 EC10 EC12 EC20 EC46 EC25 EC37 EC21
SCD1U25V2ZY-1GP
BT+
EC15
3D3V_S0
2008/11/12
EC52 EC53 EC54
5V_S5
2008/11/12
EC99 EC100 EC55
1D1V_S0
2008/12/18
EC101 EC102 EC103
VCC_CORE_S0_0
2008/11/13
EC33 EC35 EC38
SCD1U25V2ZY-1GP
1D8V_S3
2008/12/17
EC701 EC702 EC703 EC704 EC705 EC706 EC707 EC708 EC709 EC710 EC711 EC712 EC713 EC714 EC715
SC1KP50V2KX-1GP
SC4K7P50V2KX-1GP
H9
HOLE
GND1
HOLE355X355R111-S1-GP
GND2
HOLE355X355R111-S1-GP
GND3
HOLE355X355R111-S1-GP
GND4
HOLE355X355R111-S1-GP
GND5
SPRING-48-GP
34.43G01.002
DY
GND6
HOLE355X355R111-S1-GP
GND7
HOLE355X355R111-S1-GP
GND12
HOLE355X355R111-S1-GP
GND9
HOLE355X355R111-S1-GP
GND10
SPRING-48-GP
34.43G01.002
DY
GND11
SPRING-48-GP
34.43G01.002
DY
SPRING_GND14
SPRING-7
34.49U26.001
DY
2008/10/27
SPRING_GND15
SPRING-7
34.49U26.001
DY
2008/11/10
ASPRING_GND16
SPRING-12-GP-U
34.41Y19.001
DY
SPRING_GND17
SPRING-12-GP-U
34.41Y19.001
DY
2008/11/10
ASPRING_GND18
SPRING-12-GP-U
34.41Y19.001
DY
2008/11/10
ASPRING_GND19
SPRING-12-GP-U
34.41Y19.001
DY
2008/11/10
ASPRING_GND20
SPRING-12-GP-U
34.41Y19.001
DY
SPRING_GND21
SPRING-7
DY
SPRING_GND22
SPRING-7
DY
2008/12/18
ASPRING_GND22
SPRING-58-GP
2008/12/18
ASPRING_GND21
SPRING-62-GP
DY
2008/11/12
SA
SB
-1
TOP
CPU
NB
VGA
AH1 HOLE
AH2 HOLE
AH3 HOLE
AH4 HOLE
AH5 HOLE
AH6 HOLE
34.4Z003.001
TOP
MDC
H7 HOLE
34.42Y01.011
H10 HOLE
DY
2008/10/27
BOT
MINI1
H8 HOLE
34.4P901.001
Check test point
3D3V_S0 TP233 TPAD14-GP
3D3V_AUX_S5 TP232 TPAD14-GP
3D3V_S5 TP231 TPAD14-GP
5V_S5 TP230 TPAD14-GP
12,36 PM_PWRBTN# TP229 TPAD14-GP
6,11 CPU_PWRGD TP228 TPAD14-GP
35,36 S5_ENABLE TP227 TPAD14-GP
6,11 CPU_LDT_RST# TP226 TPAD14-GP
Test Point放在Dimm Door打開可量測處
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
JV50-PU
Rev
SB
Date: Friday, December 19, 2008
Sheet 52 of 61



M92

緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: M92 PCIE		
Size: A3	Document Number: JV50-PU	Rev: SB
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Layout notice:
It should be pleace near HDMI connector

DVPDATA [3:2:1:0] for VRAM type selection H/W strap
Should provide VRAM Table for VBios request

2008/10/27

DVPDATA [3:0]
0100 512MB Hynix-H5PS1G63EFR-20L (500MHz)
1000 512MB Samsung-K4N1G164QE-HC20 (500MHz)
1100 512MB QIMONDA HYB18T1G161C2F-20 (500MHz)

2008/11/07
2008/11/05

2008/11/04

2008/11/03

2008/11/10

2008/11/12

2008/12/17
2008/12/18

It's strap for GDDR3-136ball
Need to Clarify

Back Bias (body bias) which minimizes power consumption in battery modes.
PD = Disable
PU = Enable

VREFG VOLTAGE DIVIDER IS
(VREFG = VDDR4,5(1.8V) / 3 = 0.6V)

Depending on OSC used select voltage divider resist values R25 R70 to ensure XTALIN voltage level of 1.8V

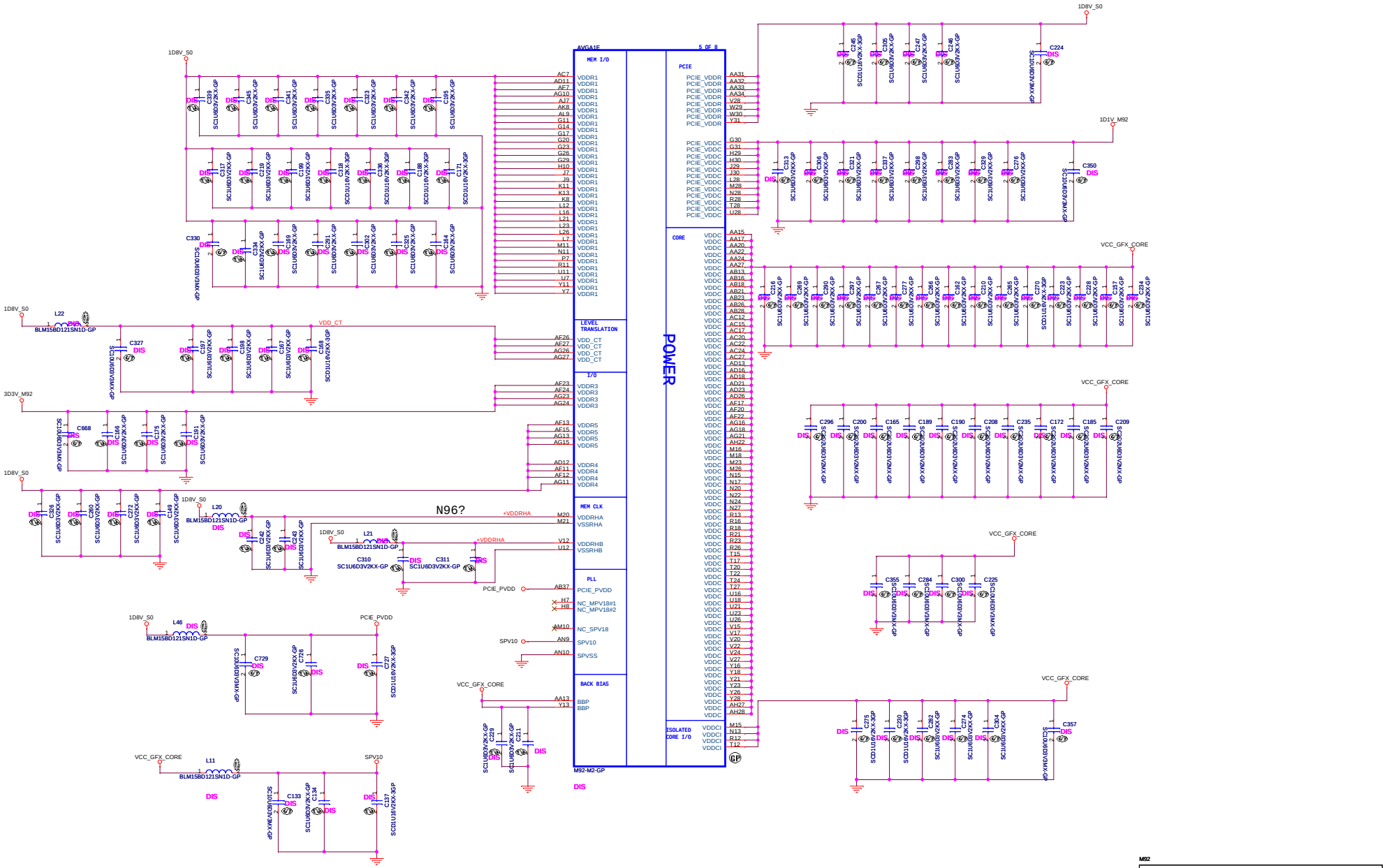
2008/12/17
2008/12/17
2008/12/17
For Thermal sensor

2008/12/17 SB

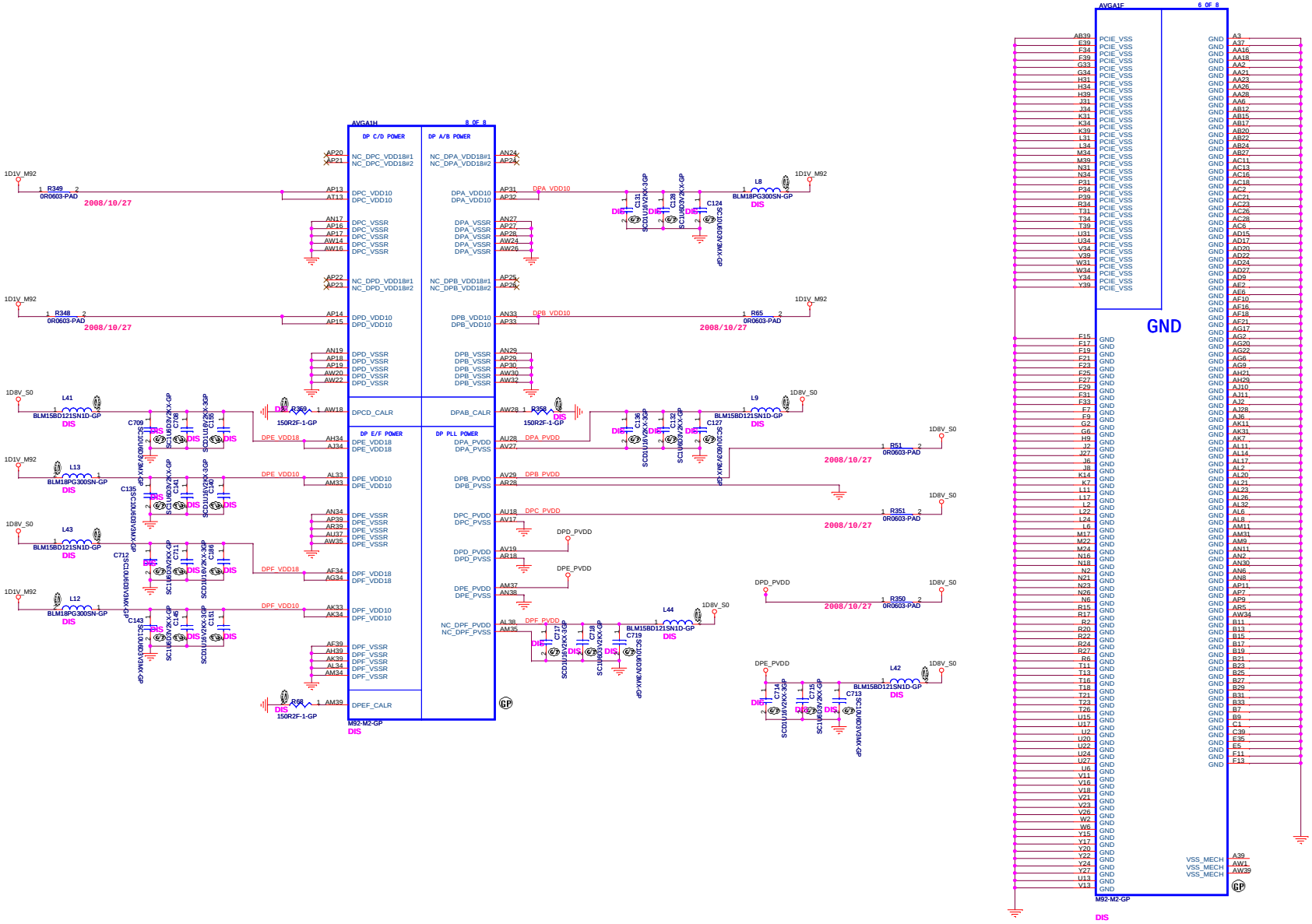
84.2N702.D31
2ND = 84.2N702.I31

84.T3904.C11
2ND = 84.03904.L06

Wistron Corporation	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	M92 IO
Size A2	Document Number JV50-PU
Rev	SB
Date: Friday, December 19, 2008	Sheet 54 of 61



M92			
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title	M92 POWER		
Size A2	Document Number JV50-PU		Rev SB
Date: Friday, December 19, 2008	Sheet 55 of 61		



M92

緯創資通	**Wistron Corporation**	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**DP POWER_GND**	
Size A2	Document Number **JV50-PU**	Rev **SB**
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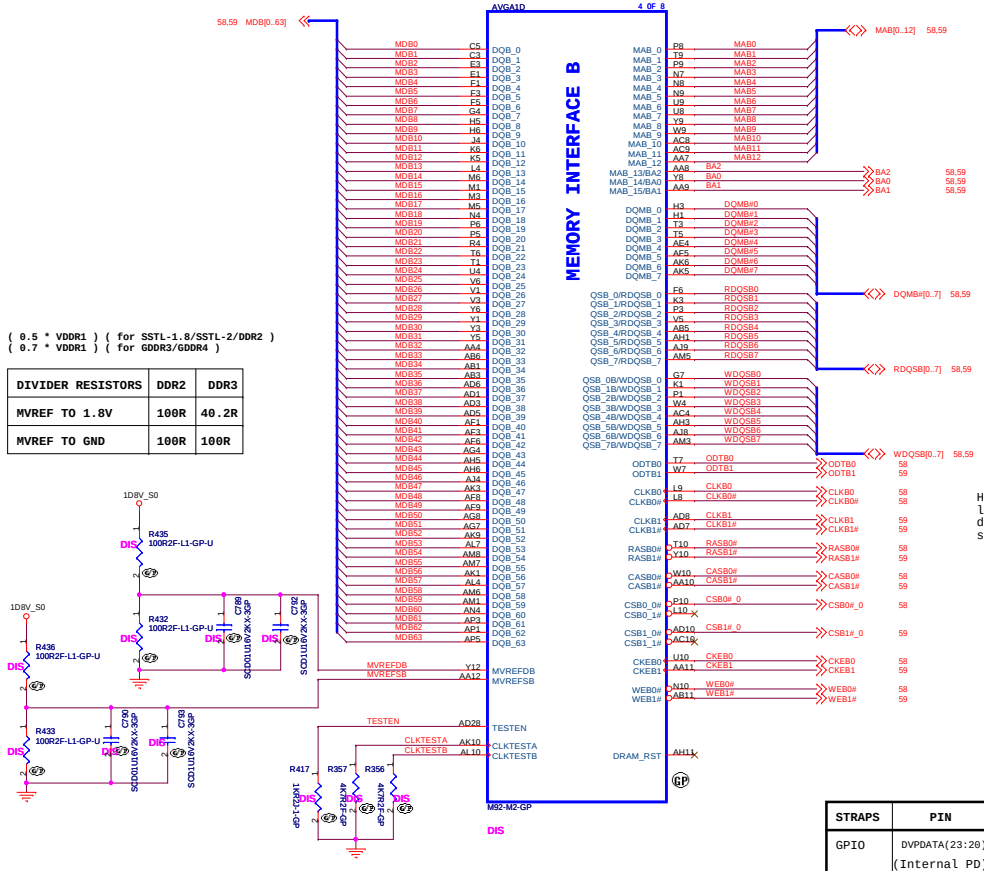
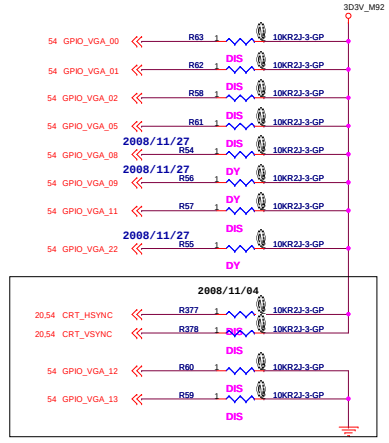
M92-M2 uses memory group B only



DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R



HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0=DO NOT INSTALL RESISTOR 1=INSTALL 10K RESISTOR X=DESIGN DEPENDANT NA=NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

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Title: Memory / Straps

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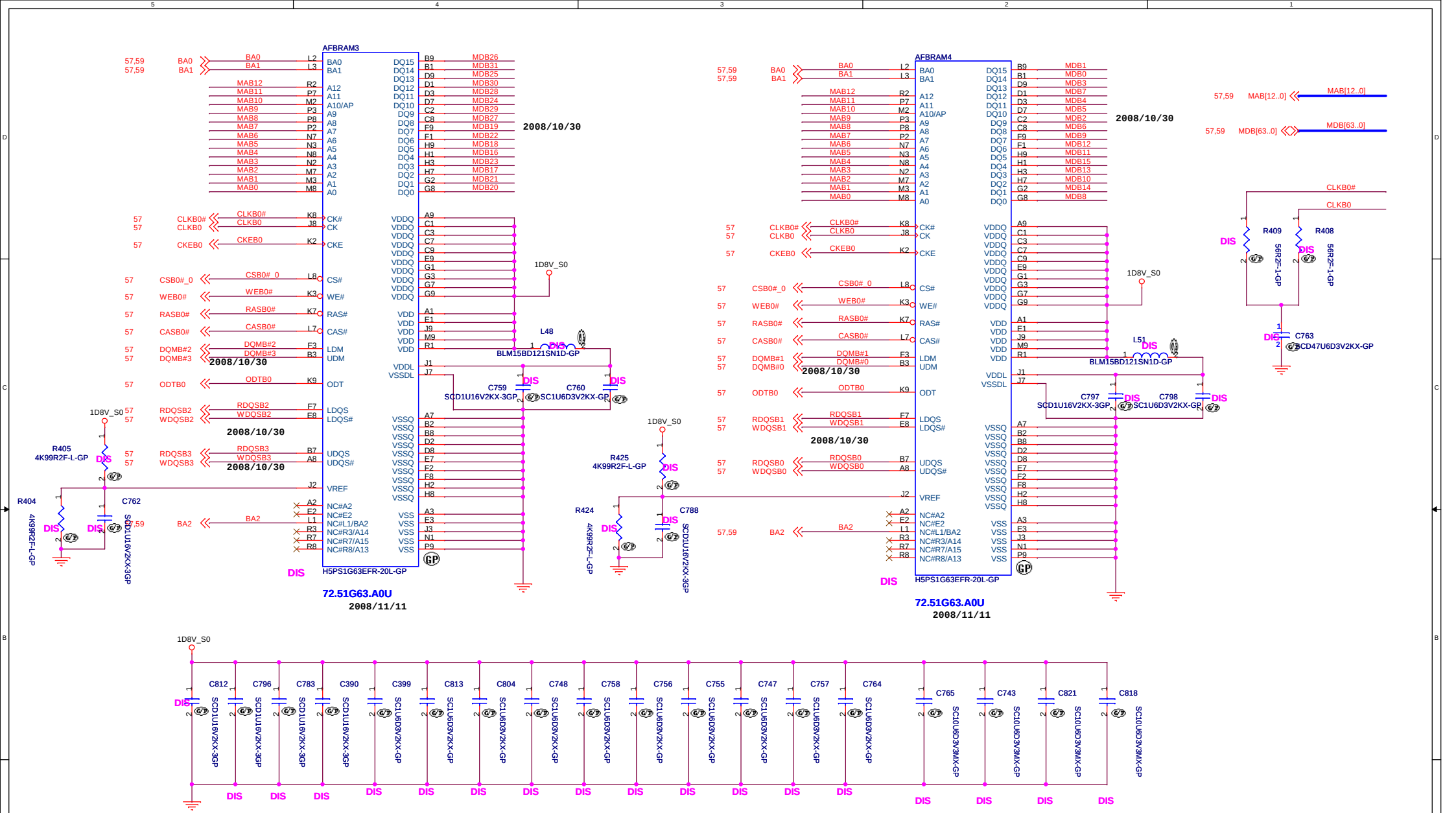
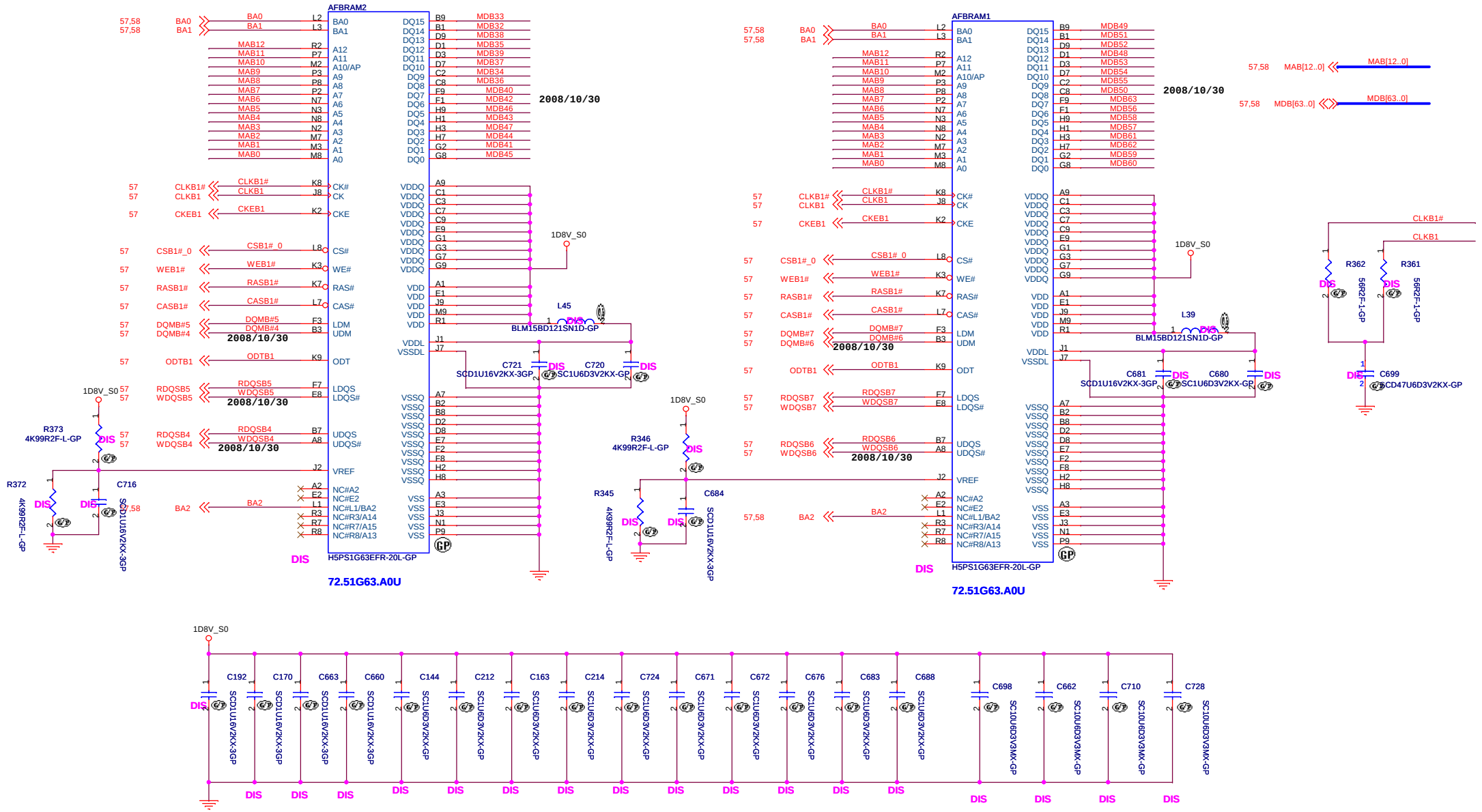


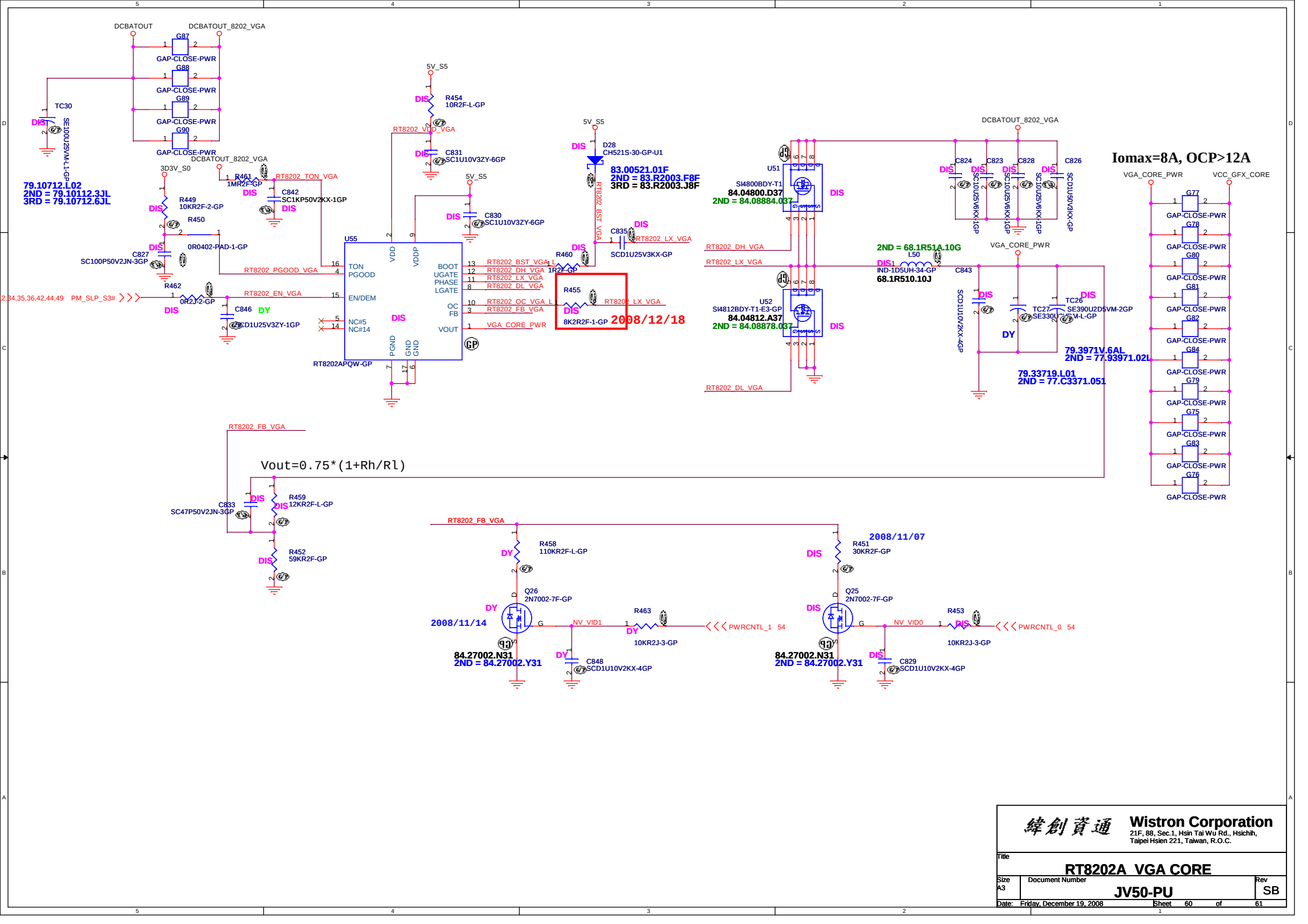
M92

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**DDR2 B0**
Size A3	Document Number **JV50-PU** Rev **SB**
Date: Friday, December 19, 2008	Sheet 58 of 61



M92

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**M92 DDR2 B1**	
Size: A3	Document Number: **JV50-PU**	Rev: **SB**
Date: Friday, December 19, 2008	Sheet 59 of 61	



緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	RT8202A VGA CORE	
Size A3	Document Number JV50-PU	Rev SB
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<Core Design>

緯創資通 **Wistron Corporation**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

HISTORY

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