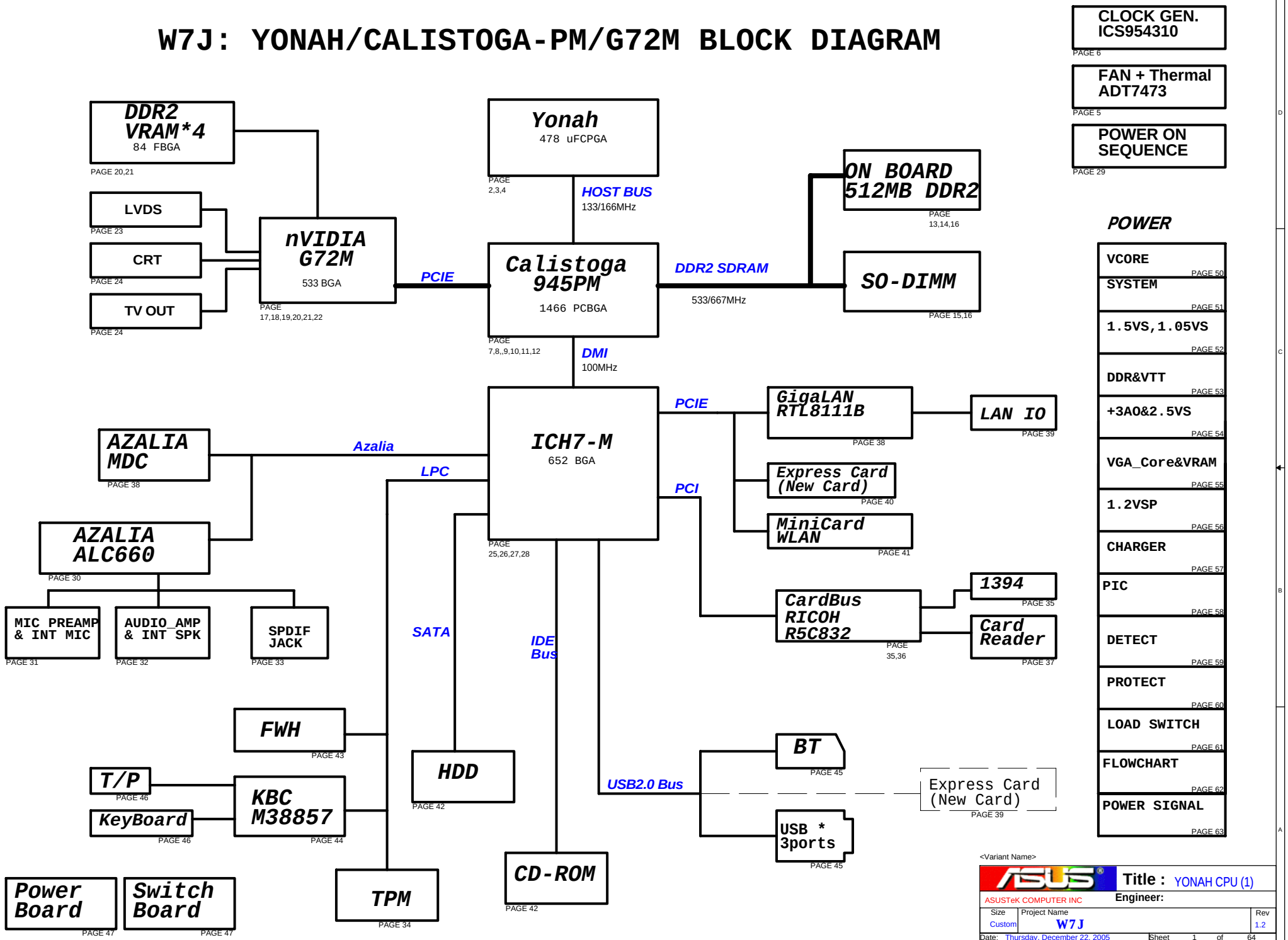
W7J: YONAH/CALISTOGA-PM/G72M BLOCK DIAGRAM



<Variant Name>

ASUSTeK COMPUTER INC

Title : YONAH CPU (1)

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 1 of 64

7 H_A#[31:3] H_A#[31:3]

7 H_REQ#[4:0] H_REQ#[4:0]

7 H_D#[63:0] H_D#[63:0]

U43A

U43B

BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H

Zo=55 ohm, 0.5" max for GTLREF

Comp0,2 connect with Zo=27.4 ohm, make trace length shorter than 0.5". Comp 1,3 connect with Z0=55 ohm, make trace length shorter than 0.5".

+VCORE +VCORE 3,4,5,44,50

+VCCP +VCCP 3,4,6,7,8,10,11,12,25,28,52

Note: Don't need for NAPA platform.But,it is exist on Alviso platform

<Variant Name>

ASUSTeK COMPUTER INC

Title : YONAH CPU (1)

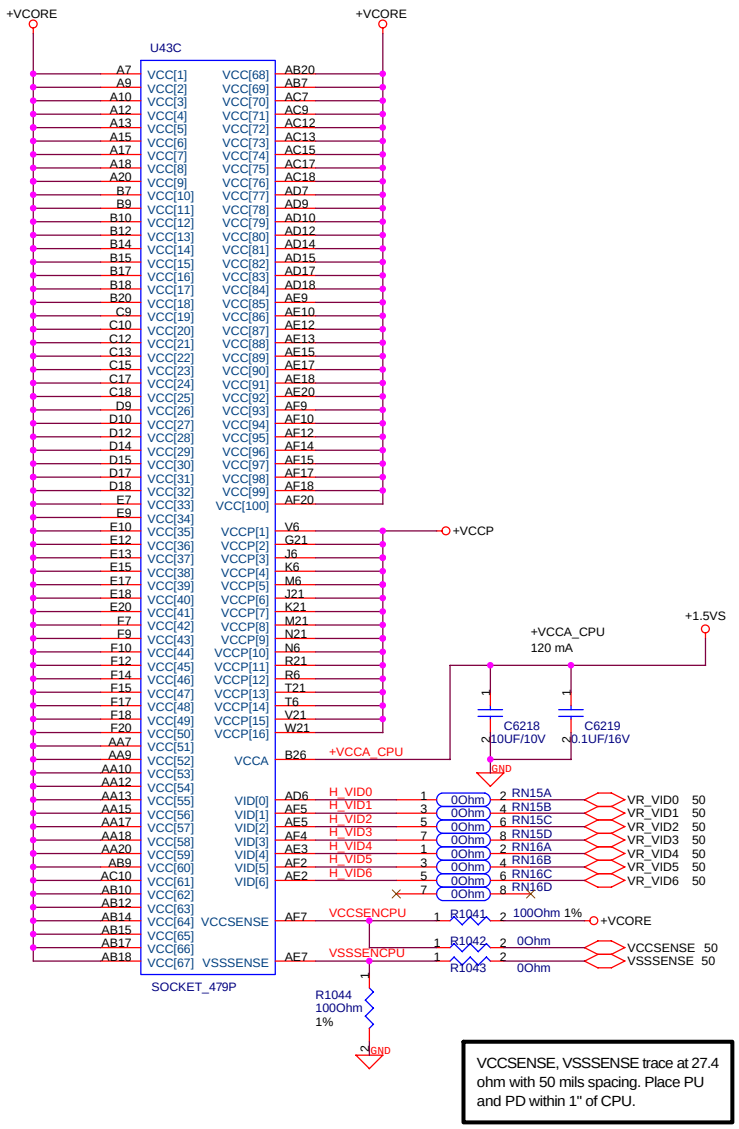
Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

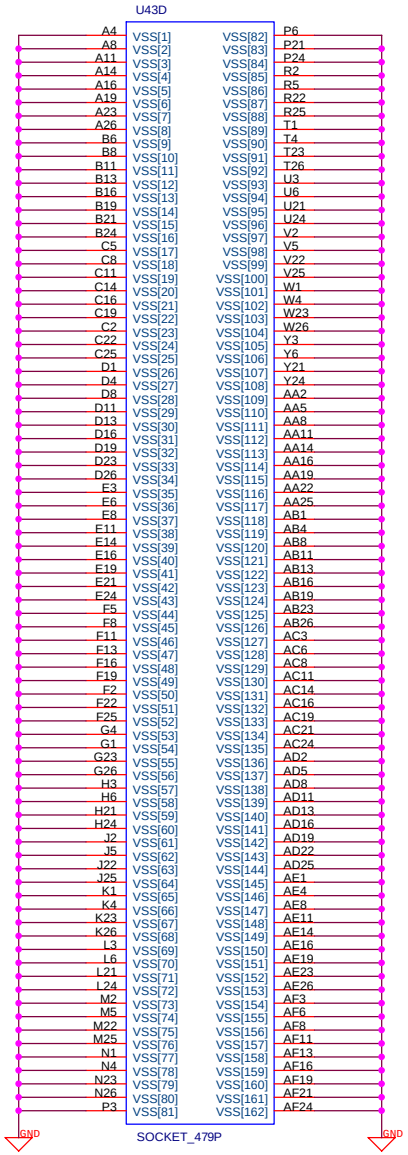
Date: Thursday, December 22, 2005 Sheet 2 of 64

YUNAH FSB667			
	LFM	TYP	HFM
VCC	1.14V	1.2V	1.356V
	C4	C3	C0
ICC	0.9A	7.59A	27A

YUNAH FSB667			
	Min	Typ	Max
VCCP	0.997V	1.05V	1.102V
	Min	Typ	Max
ICCP			2.5A



VCCSENSE, VSSSENSE trace at 27.4 ohm with 50 mils spacing. Place PU and PD within 1" of CPU.



<Variant Name>

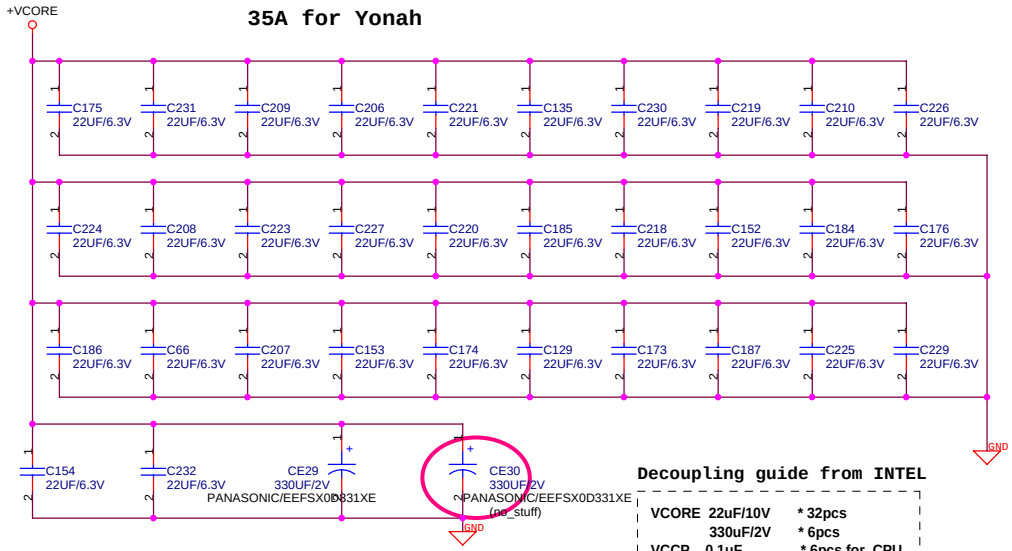
ASUSTeK COMPUTER INC

Title : YONAH CPU (2)

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

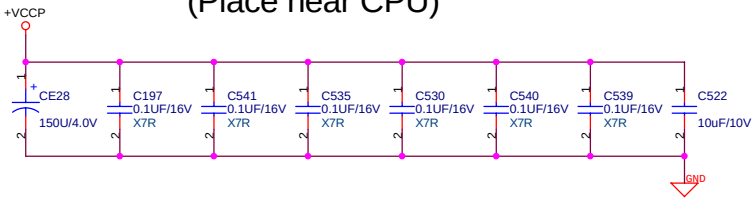
Date: Thursday, December 22, 2005 Sheet 3 of 64



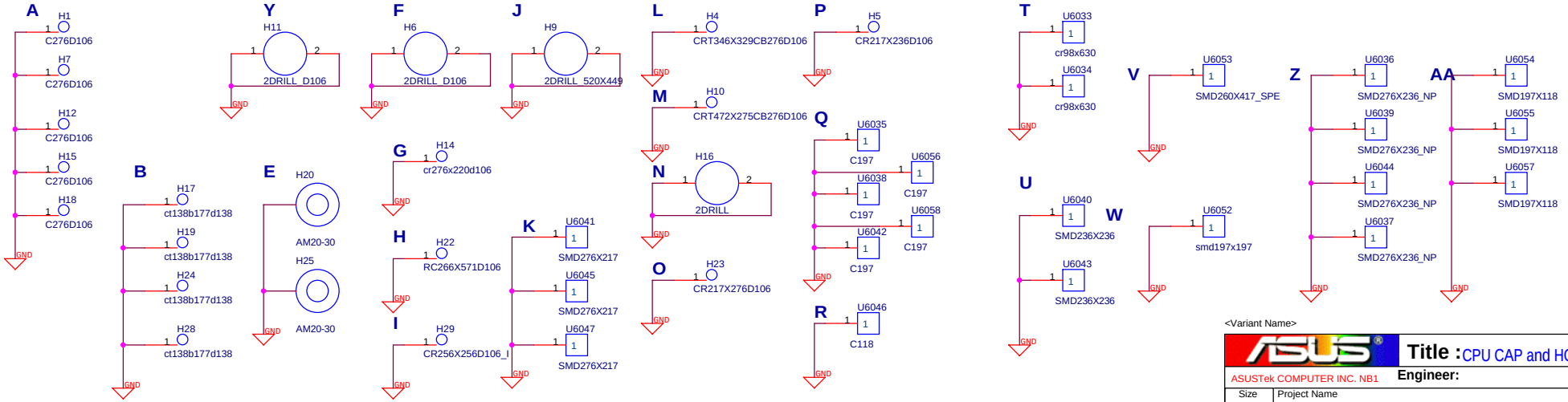
Decoupling guide from INTEL

VCORE	22uF/10V	* 32pcs
	330uF/2V	* 6pcs
VCCP	0.1uF	* 6pcs for CPU
	150uF	* 1pcs for CPU

+VCCP Decoupling Capacitor (Place near CPU)



SCREW HOLE



<Variant Name>

ASUSTek COMPUTER INC. NB1

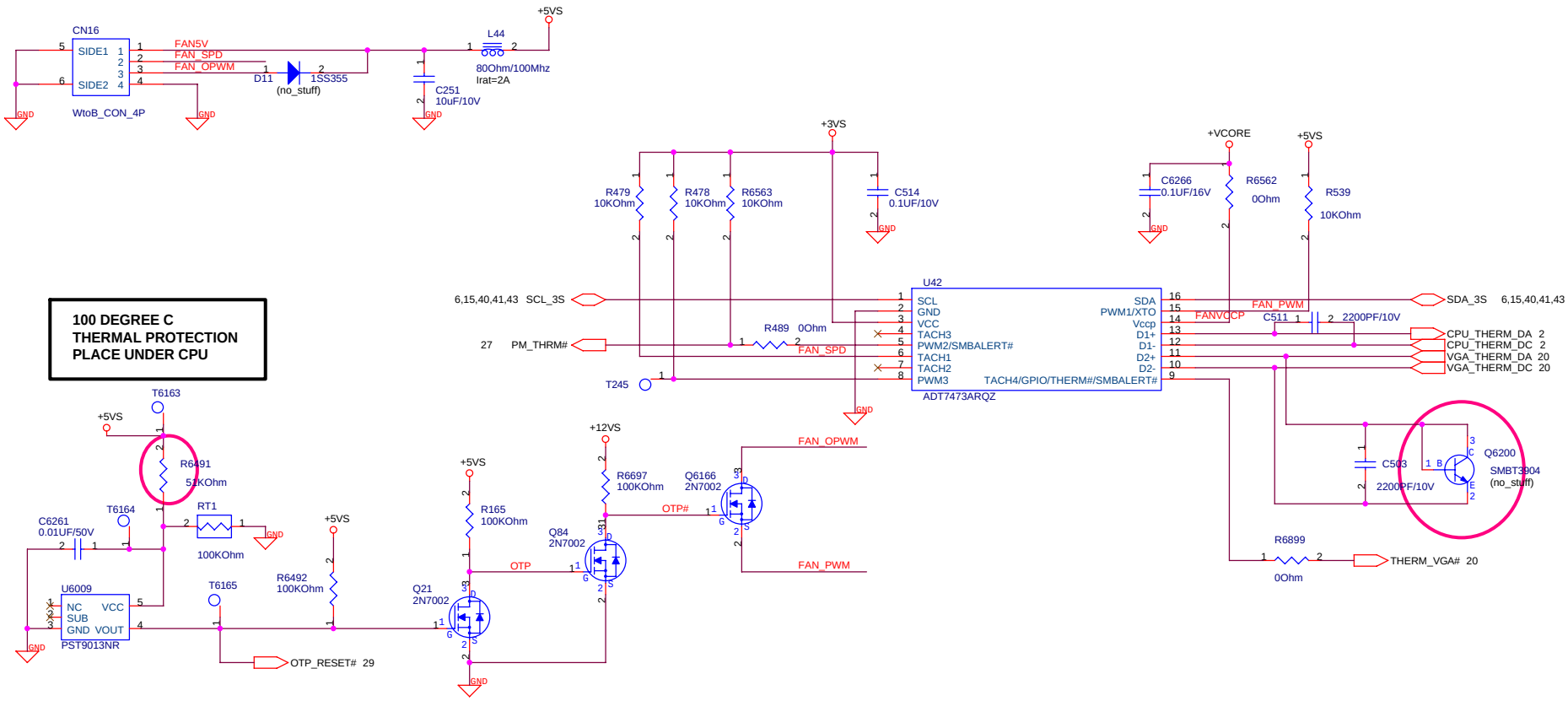
Title : CPU CAP and HOLES

Engineer:

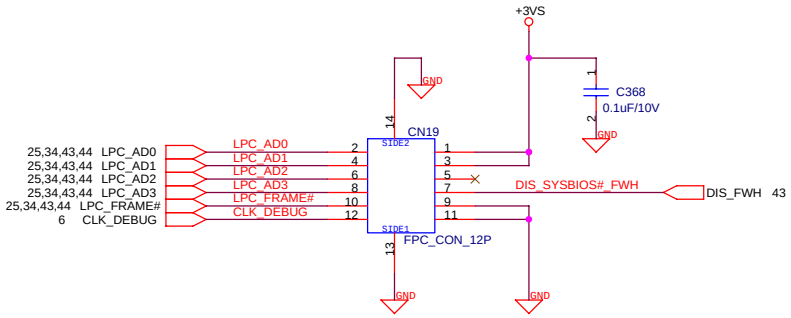
Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 4 of 64

FAN & THERMAL CONTROLLER

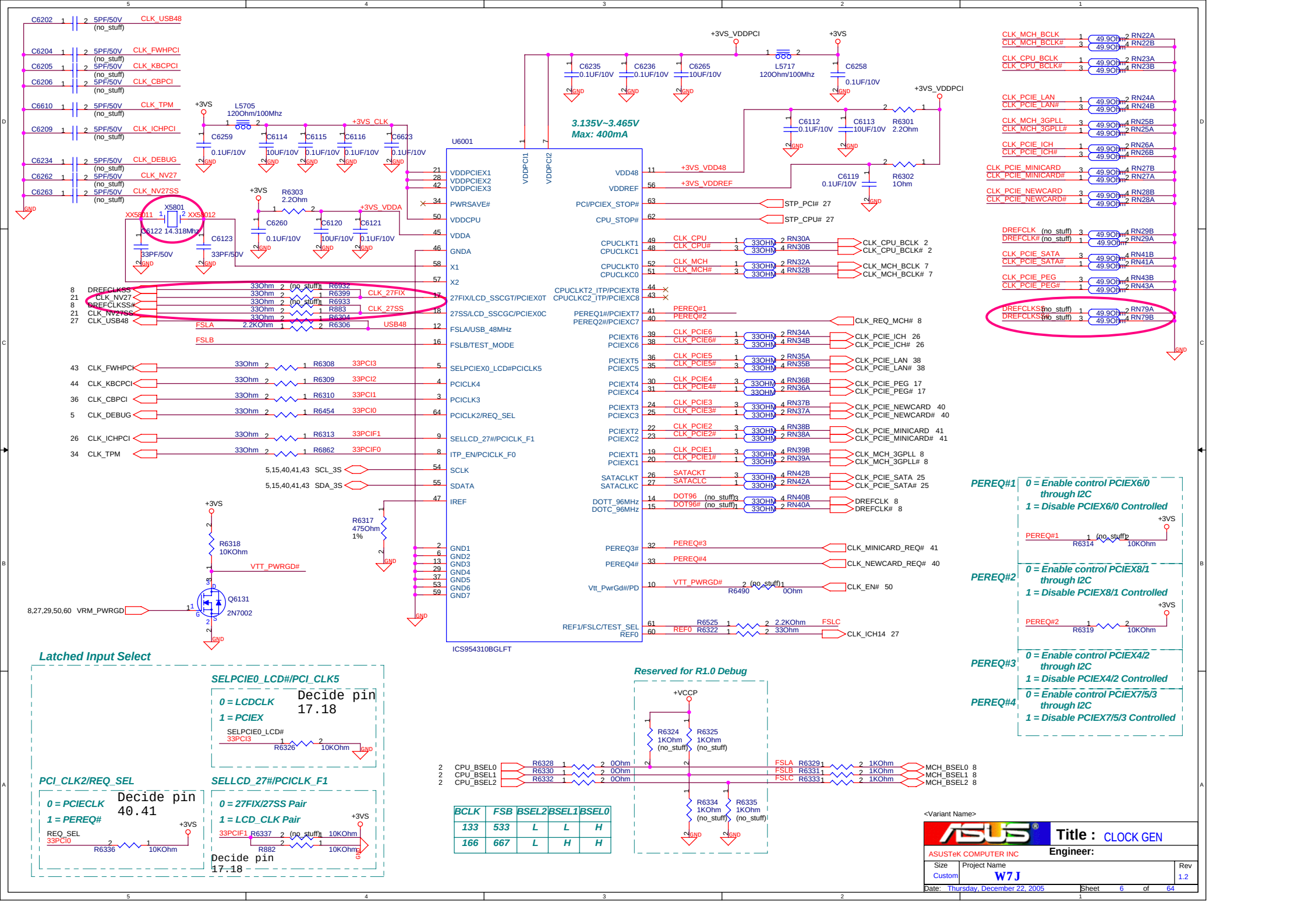


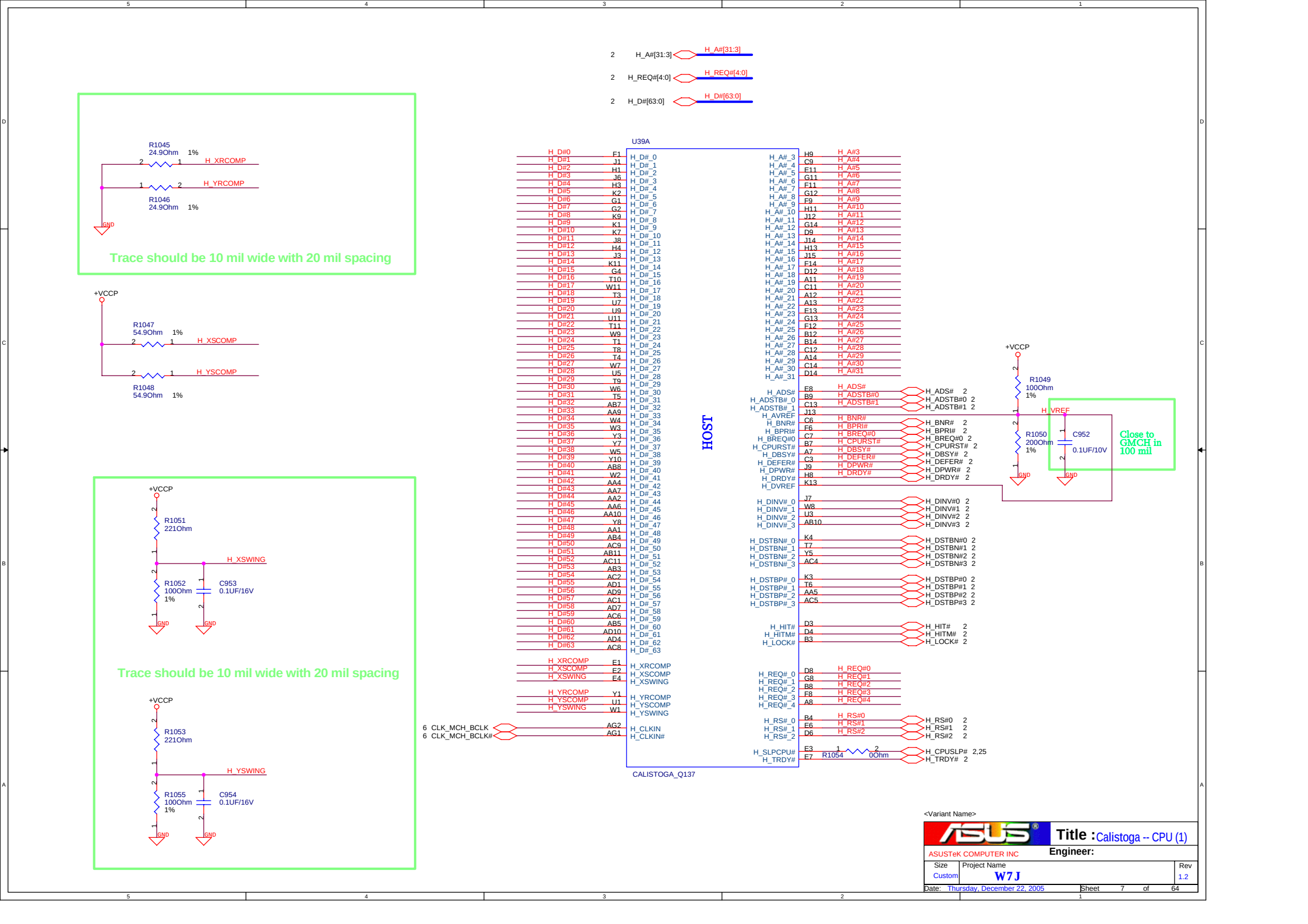
LPC DEBUG PORT

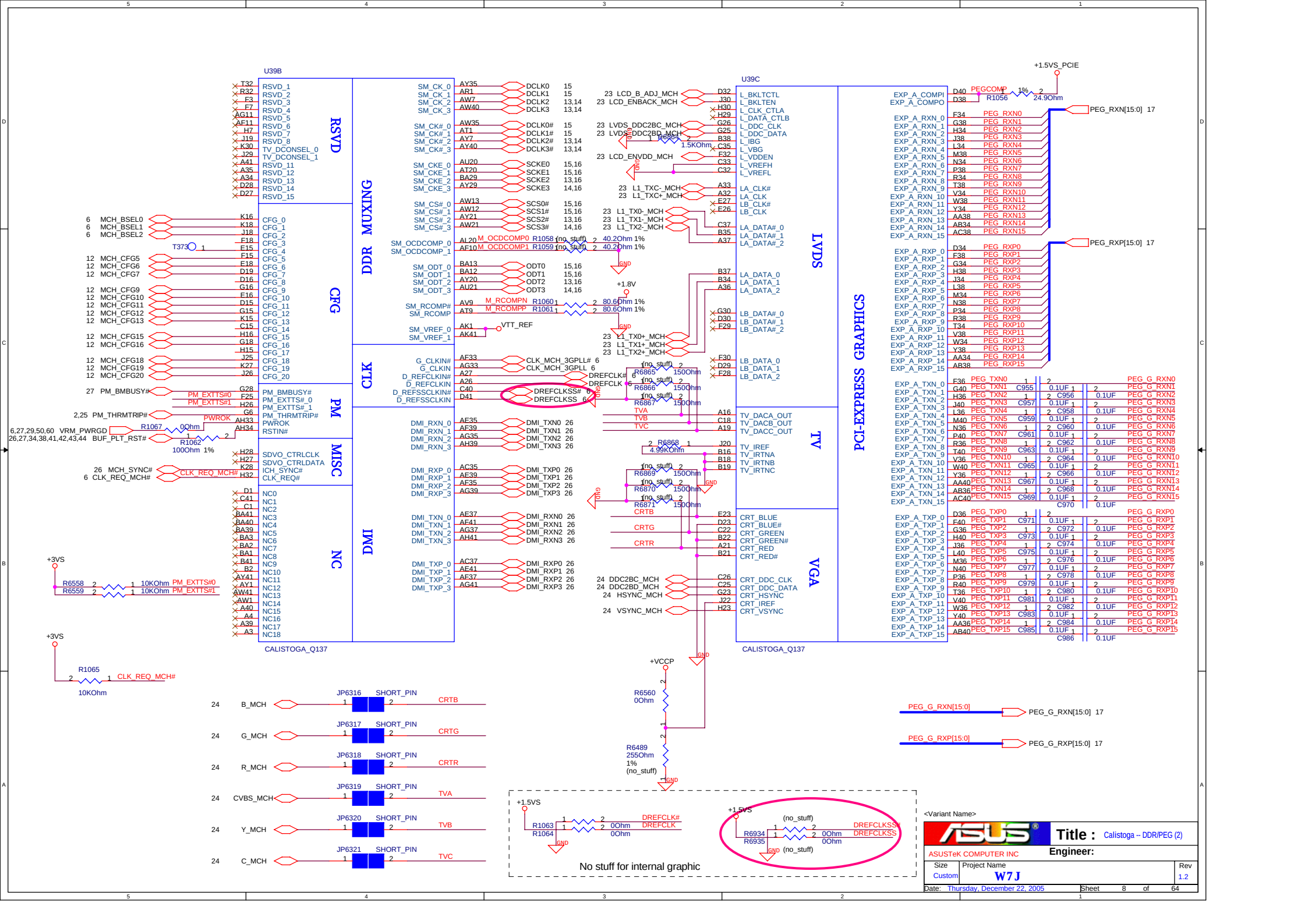


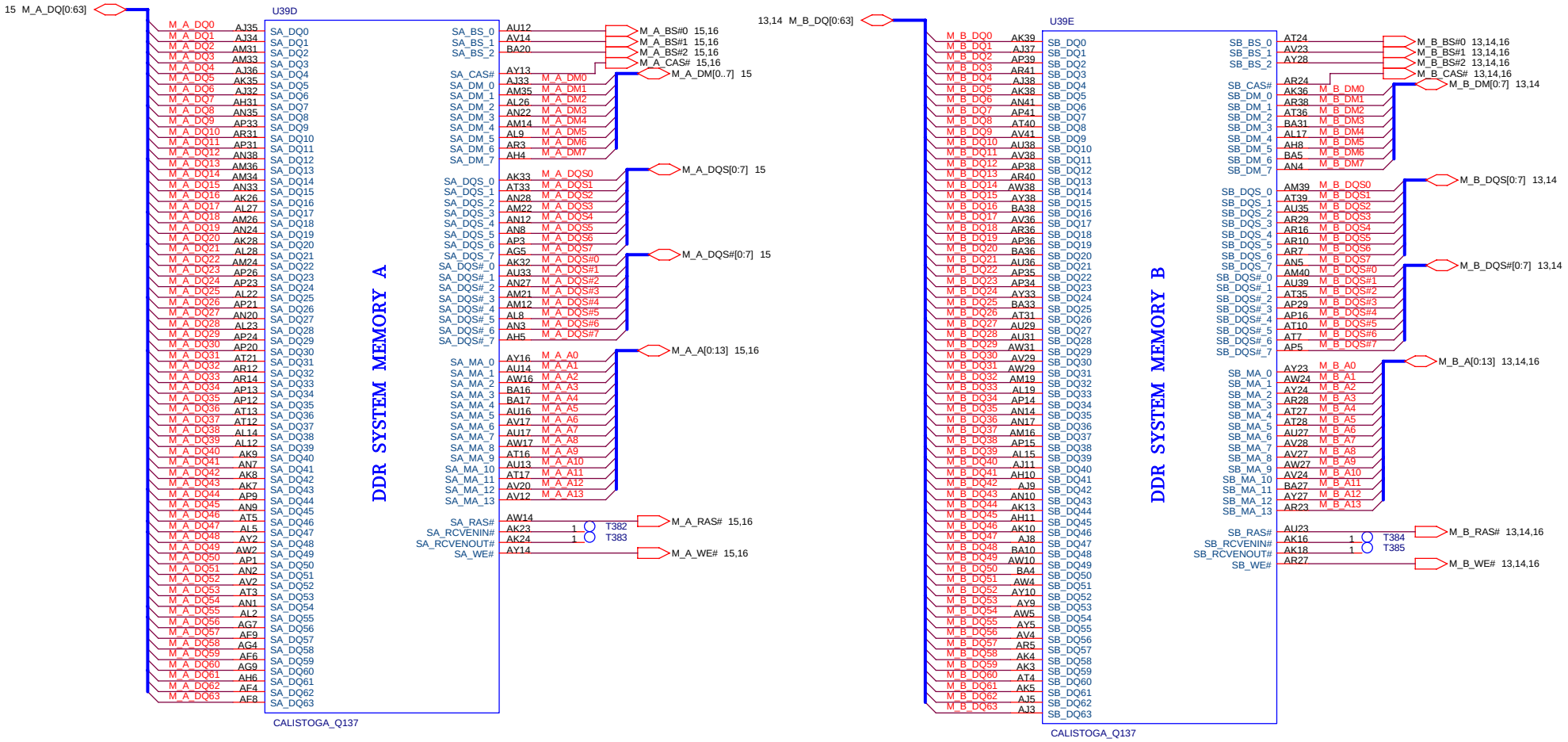
<Variant Name>

ASUSTeK COMPUTER INC	Title : FAN & debug port	
	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 5 of 64	


U6001
ICS954310BGLFT
3.135V~3.465V
Max: 400mA
Latched Input Select
SELPCIE0_LCD#/PCI_CLK5
0 = LCDCLK
1 = PCIEX
Decide pin 17.18
PCI_CLK2/REQ_SEL
0 = PCIECLK
1 = PEREQ#
Decide pin 40.41
SELLCD_27#/PCICLK_F1
0 = 27FIX/27SS Pair
1 = LCD_CLK Pair
Decide pin 17.18
Reserved for R1.0 Debug
PEREQ#1
0 = Enable control PCIEX6/0 through I2C
1 = Disable PCIEX6/0 Controlled
PEREQ#2
0 = Enable control PCIEX8/1 through I2C
1 = Disable PCIEX8/1 Controlled
PEREQ#3
0 = Enable control PCIEX4/2 through I2C
1 = Disable PCIEX4/2 Controlled
PEREQ#4
0 = Enable control PCIEX7/5/3 through I2C
1 = Disable PCIEX7/5/3 Controlled
BCLK FSB BSEL2 BSEL1 BSEL0
133 533 L L H
166 667 L H H
Title : CLOCK GEN
ASUSTeK COMPUTER INC
Engineer:
Project Name W7J
Rev 1.2
Date: Thursday, December 22, 2005
Sheet 6 of 64


2 H_A#[31:3] H_A#[31:3]
2 H_REQ#[4:0] H_REQ#[4:0]
2 H_D#[63:0] H_D#[63:0]
R1045 24.9Ohm 1%
H_XRCOMP
H_YRCOMP
R1046 24.9Ohm 1%
GND
Trace should be 10 mil wide with 20 mil spacing
+VCCP
R1047 54.9Ohm 1%
H_XSCOMP
H_YSCOMP
R1048 54.9Ohm 1%
+VCCP
R1051 221Ohm
H_XSWING
R1052 100Ohm 1%
C953 0.1UF/16V
GND
Trace should be 10 mil wide with 20 mil spacing
+VCCP
R1053 221Ohm
H_YSWING
R1055 100Ohm 1%
C954 0.1UF/16V
GND
U39A
HOST
CALISTOGA_Q137
6 CLK_MCH_BCLK
6 CLK_MCH_BCLK#
H_CLKIN
H_CLKIN#
H_XRCOMP
H_XSCOMP
H_XSWING
H_YRCOMP
H_YSCOMP
H_YSWING
H_ADS# 2
H_ADSTB#0 2
H_ADSTB#1 2
H_BNR# 2
H_BPRI# 2
H_BREQ#0 2
H_CPURST# 2
H_DBSY# 2
H_DEFER# 2
H_DPWR# 2
H_DRDY# 2
H_DINV#0 2
H_DINV#1 2
H_DINV#2 2
H_DINV#3 2
H_DSTBN#0 2
H_DSTBN#1 2
H_DSTBN#2 2
H_DSTBN#3 2
H_DSTBP#0 2
H_DSTBP#1 2
H_DSTBP#2 2
H_DSTBP#3 2
H_HIT# 2
H_HITM# 2
H_LOCK# 2
H_RS#0 2
H_RS#1 2
H_RS#2 2
H_CPUSLP# 2,25
H_TRDY# 2
R1054 0Ohm
+VCCP
R1049 100Ohm 1%
H_VREF
R1050 200Ohm 1%
C952 0.1UF/10V
GND
Close to GMCH in 100 mil
<Variant Name>
Title : Calistoga -- CPU (1)
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 1.2
Date: Thursday, December 22, 2005
Sheet 7 of 64


U39B
RSVD
DDR MUXING
CFG
PM
MISC
CLK
DMI
NC
CALISTOGA_Q137
U39C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
CALISTOGA_Q137
+1.5VS_PCIE
PEG_RXN[15:0] 17
PEG_RXP[15:0] 17
PEG_G_RXN[15:0] 17
PEG_G_RXP[15:0] 17
+3VS
+1.8V
+VCCP
GND
VTT_REF
JP6316 SHORT_PIN CRTB
JP6317 SHORT_PIN CRTG
JP6318 SHORT_PIN CRTR
JP6319 SHORT_PIN TVA
JP6320 SHORT_PIN TVB
JP6321 SHORT_PIN TVC
No stuff for internal graphic
<Variant Name>
Title : Calistoga -- DDR/PEG (2)
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 1.2
Date: Thursday, December 22, 2005
Sheet 8 of 64



<Variant Name>

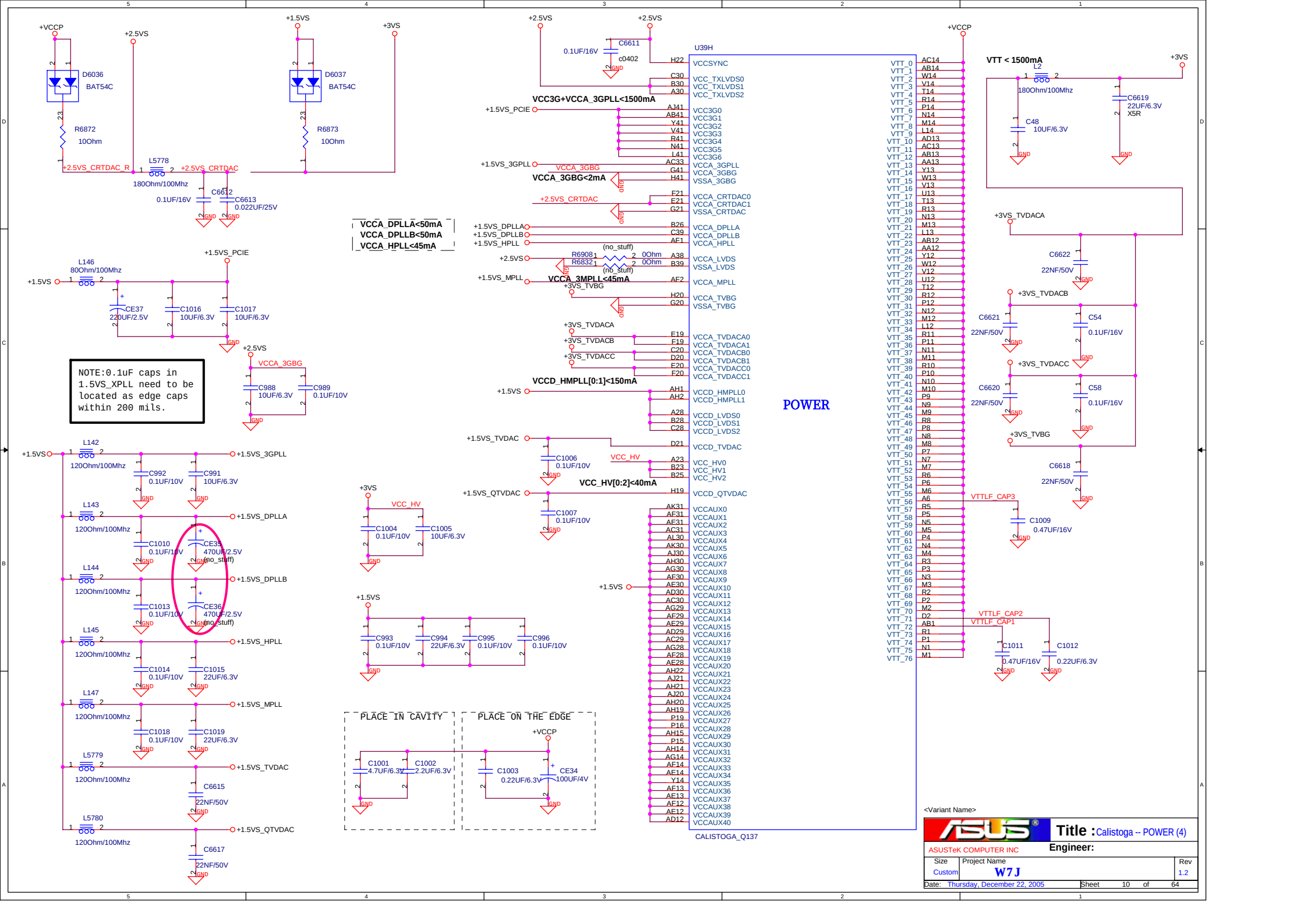
ASUSTeK COMPUTER INC

Title : Calistoga -- DDR bus (3)

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 9 of 64


+VCCP
+2.5VS
+1.5VS
+3VS
D6036
BAT54C
D6037
BAT54C
R6872
10Ohm
R6873
10Ohm
+2.5VS_CRTDAC_R
L5778
180Ohm/100Mhz
+2.5VS_CRTDAC
C6612
0.1UF/16V
C6613
0.022UF/25V
GND
L146
80Ohm/100Mhz
+1.5VS_PCIE
CE37
220UF/2.5V
C1016
10UF/6.3V
C1017
10UF/6.3V
VCCA_3GBG
C988
10UF/6.3V
C989
0.1UF/10V
NOTE:0.1uF caps in 1.5VS_XPLL need to be located as edge caps within 200 mils.
L142
120Ohm/100Mhz
+1.5VS_3GPLL
C992
0.1UF/10V
C991
10UF/6.3V
L143
+1.5VS_DPLLA
C1010
0.1UF/10V
CE35
470UF/2.5V
(no_stuff)
L144
+1.5VS_DPLLB
C1013
0.1UF/10V
CE36
470UF/2.5V
(no_stuff)
L145
+1.5VS_HPLL
C1014
0.1UF/10V
C1015
22UF/6.3V
L147
+1.5VS_MPLL
C1018
0.1UF/10V
C1019
22UF/6.3V
L5779
+1.5VS_TVDAC
C6615
22NF/50V
L5780
+1.5VS_QTVDAC
C6617
22NF/50V
VCC_HV
C1004
0.1UF/10V
C1005
10UF/6.3V
C993
0.1UF/10V
C994
22UF/6.3V
C995
0.1UF/10V
C996
0.1UF/10V
PLACE IN CAVITY
PLACE ON THE EDGE
C1001
4.7UF/6.3V
C1002
2.2UF/6.3V
C1003
0.22UF/6.3V
CE34
100UF/4V
VCCA_DPLLA<50mA
VCCA_DPLLB<50mA
VCCA_HPLL<45mA
C6611
0.1UF/16V
c0402
U39H
VCCSYNC
VCC_TXLVDS0
VCC_TXLVDS1
VCC_TXLVDS2
VCC3G+VCCA_3GPLL<1500mA
+1.5VS_PCIE
VCC3G0
VCC3G1
VCC3G2
VCC3G3
VCC3G4
VCC3G5
VCC3G6
+1.5VS_3GPLL
VCCA_3GPLL
VCCA_3GBG<2mA
VCCA_3GBG
VSSA_3GBG
+2.5VS_CRTDAC
VCCA_CRTDAC0
VCCA_CRTDAC1
VSSA_CRTDAC
+1.5VS_DPLLA
+1.5VS_DPLLB
+1.5VS_HPLL
VCCA_DPLLA
VCCA_DPLLB
VCCA_HPLL
R6908
R6832
0Ohm
(no_stuff)
VCCA_LVDS
VSSA_LVDS
+1.5VS_MPLL
VCCA_3MPLL<45mA
VCCA_MPLL
+3VS_TVBG
VCCA_TVBG
VSSA_TVBG
+3VS_TVDACA
+3VS_TVDACB
+3VS_TVDACC
VCCA_TVDACA0
VCCA_TVDACA1
VCCA_TVDACB0
VCCA_TVDACB1
VCCA_TVDACC0
VCCA_TVDACC1
VCCD_HMPLL[0:1]<150mA
VCCD_HMPLL0
VCCD_HMPLL1
VCCD_LVDS0
VCCD_LVDS1
VCCD_LVDS2
+1.5VS_TVDAC
VCCD_TVDAC
C1006
0.1UF/10V
VCC_HV
VCC_HV0
VCC_HV1
VCC_HV2
VCC_HV[0:2]<40mA
+1.5VS_QTVDAC
VCCD_QTVDAC
C1007
0.1UF/10V
VCCAUX0
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCAUX15
VCCAUX16
VCCAUX17
VCCAUX18
VCCAUX19
VCCAUX20
VCCAUX21
VCCAUX22
VCCAUX23
VCCAUX24
VCCAUX25
VCCAUX26
VCCAUX27
VCCAUX28
VCCAUX29
VCCAUX30
VCCAUX31
VCCAUX32
VCCAUX33
VCCAUX34
VCCAUX35
VCCAUX36
VCCAUX37
VCCAUX38
VCCAUX39
VCCAUX40
CALISTOGA_Q137
POWER
VTT_0
VTT_1
VTT_2
VTT_3
VTT_4
VTT_5
VTT_6
VTT_7
VTT_8
VTT_9
VTT_10
VTT_11
VTT_12
VTT_13
VTT_14
VTT_15
VTT_16
VTT_17
VTT_18
VTT_19
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VTT_64
VTT_65
VTT_66
VTT_67
VTT_68
VTT_69
VTT_70
VTT_71
VTT_72
VTT_73
VTT_74
VTT_75
VTT_76
VTT < 1500mA
L2
180Ohm/100Mhz
C48
10UF/6.3V
C6619
22UF/6.3V
X5R
C6622
22NF/50V
C6621
22NF/50V
C54
0.1UF/16V
C6620
22NF/50V
C58
0.1UF/16V
C6618
22NF/50V
VTTLF_CAP3
C1009
0.47UF/16V
VTTLF_CAP2
VTTLF_CAP1
C1011
0.47UF/16V
C1012
0.22UF/6.3V
<Variant Name>
Title : Calistoga -- POWER (4)
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
W7J
Rev
1.2
Date: Thursday, December 22, 2005
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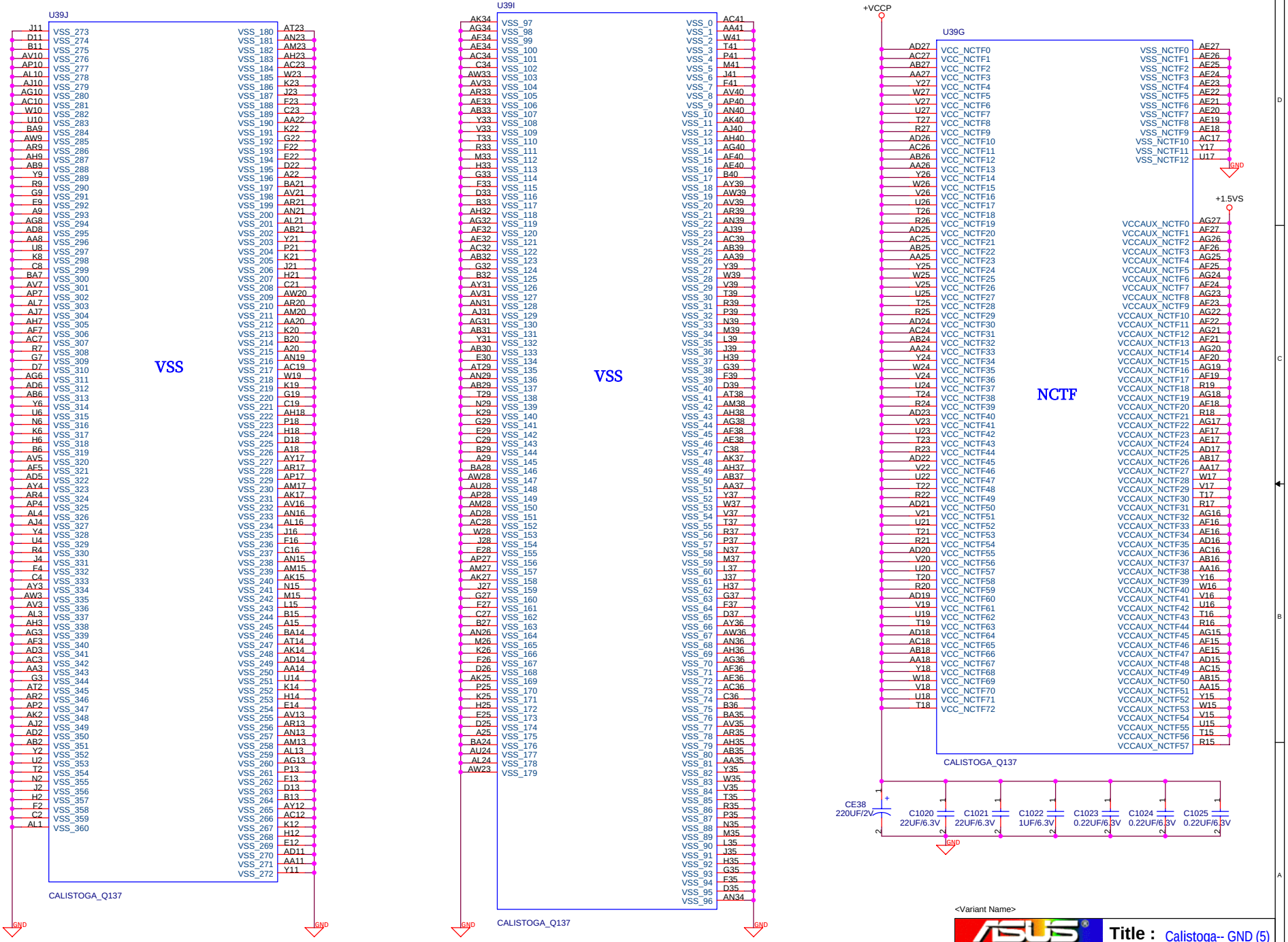


<Variant Name>

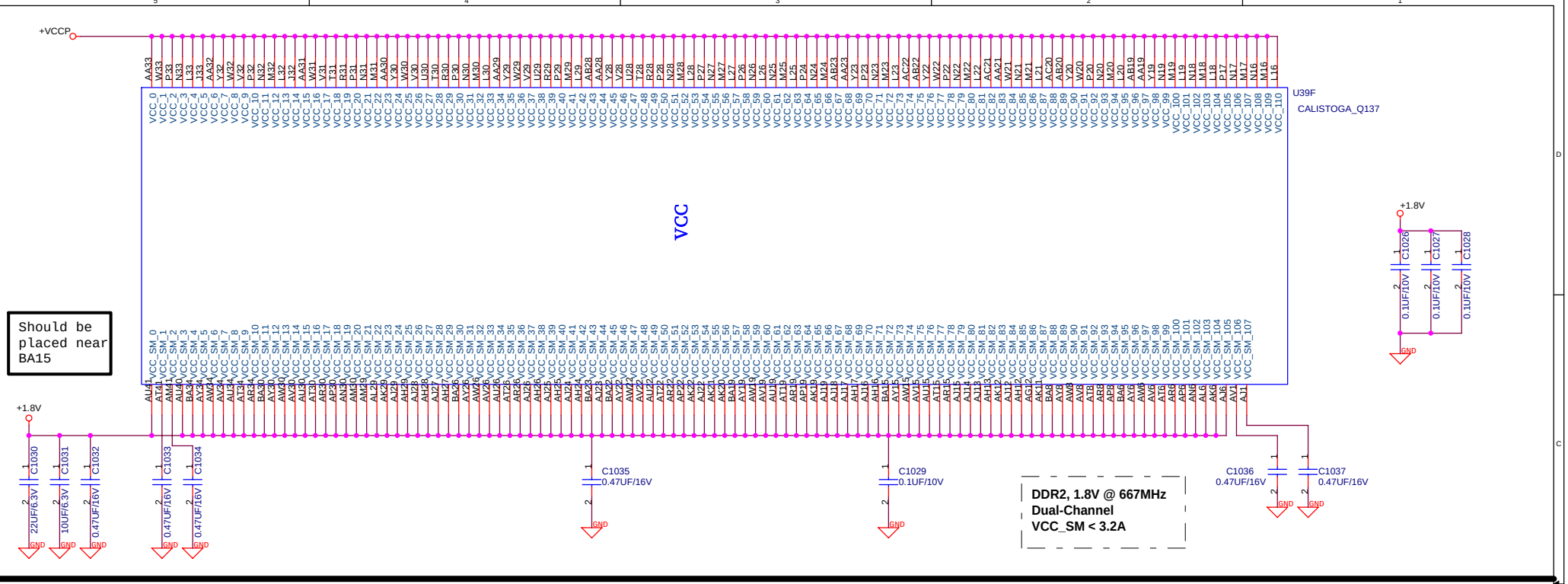
ASUSTeK COMPUTER INC

Title : Calistoga-- GND (5)

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 11 of 64



8 MCH_CFG5 — R1069 2.2KOhm (no_stuff)

CFG5 : DMI STRAP
LOW = DMI X 2
HIGH = DMI X 4 (Default)

8 MCH_CFG9 — R1077 2.2KOhm

CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)

8 MCH_CFG15 — R1078 2.2KOhm (no_stuff)

CFG15 :ICH RESET DISABLE
LOW = ICH RESET DISABLE
HIGH = NORMAL OPERATION

8 MCH_CFG12 — R1076 2.2KOhm (no_stuff)
8 MCH_CFG13 — R1072 2.2KOhm (no_stuff)

8 MCH_CFG6 — R6479 2.2KOhm (no_stuff)

CFG6 : DDR STRAP
LOW = Moby Dick
HIGH = Calistoga (Default)

8 MCH_CFG10 — R1070 2.2KOhm (no_stuff)

CFG10: HOST PLL VCO SELECT
LOW = RESERVED
HIGH = MOBILITY

8 MCH_CFG16 — R1071 2.2KOhm (no_stuff)

CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)

CFG19 : DMI LANE REVERSAL
LOW = NORMAL
HIGH = LANES REVERSED

+3VS — R1079 1KOhm (no_stuff) — 8 MCH_CFG19

8 MCH_CFG7 — R1075 2.2KOhm (no_stuff)

CFG7 : CPU STRAP
LOW = RSVD
HIGH = Mobile CPU (Default)

8 MCH_CFG11 — R1073 2.2KOhm (no_stuff)

CFG11 : PSB 4X CLK ENABLE
LOW = Reserved
HIGH = Calistoga (Default)

CFG18 : GMCH Core Voltage Level
LOW = 1.05V (Default)
HIGH = 1.5V

+3VS — R1074 1KOhm (no_stuff) — 8 MCH_CFG18

CFG20 : PCIE Backward Interpoerability mode
LOW = only SDVO or PCIE*1 isoperational (default)
HIGH = SDVO and PCIE*1 are operating simulaneously via the PEG port

+3VS — R6480 1KOhm (no_stuff) — 8 MCH_CFG20

<Variant Name>

ASUSTeK COMPUTER INC

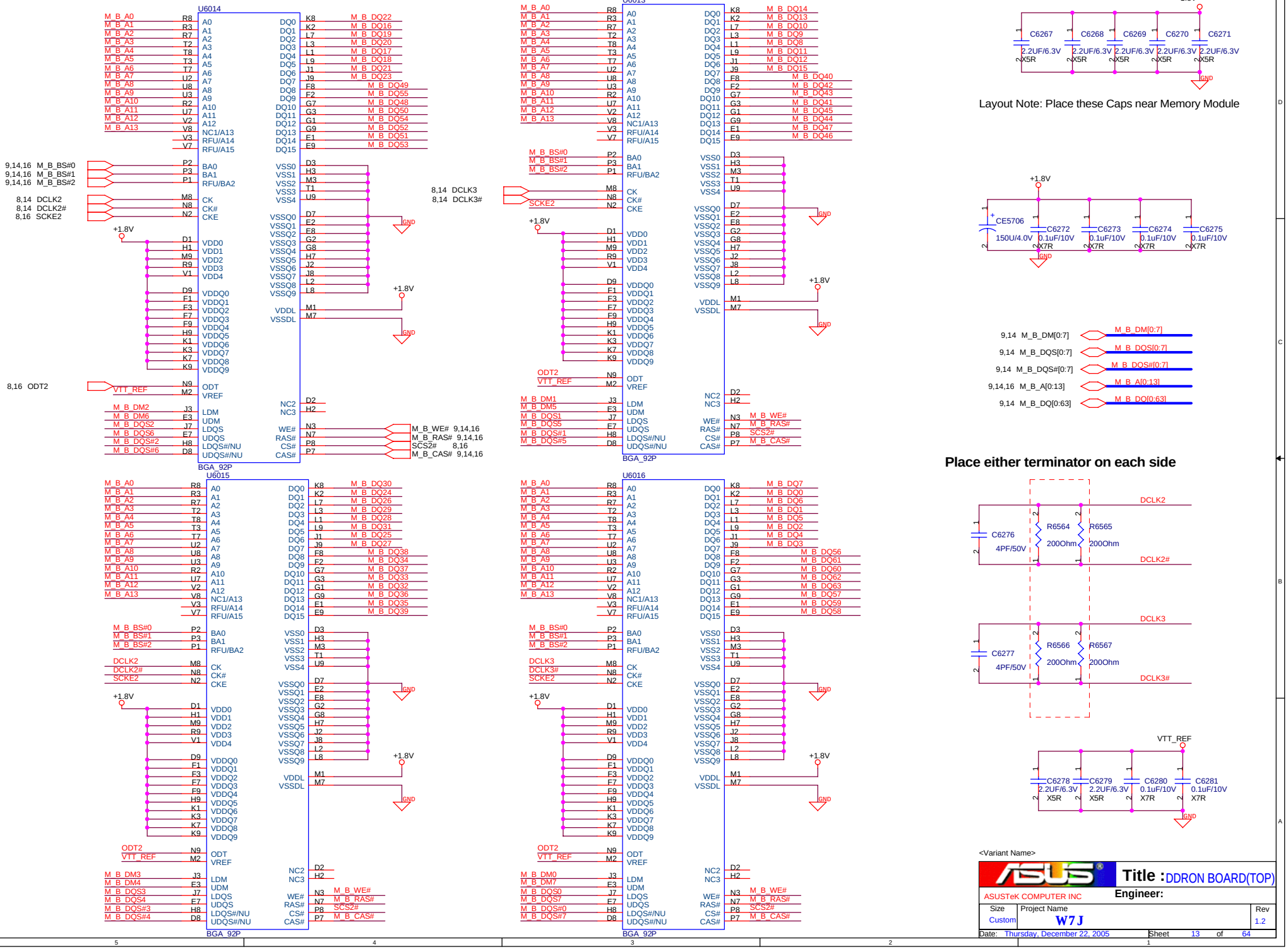
Title : Calistoga-- GND (6)

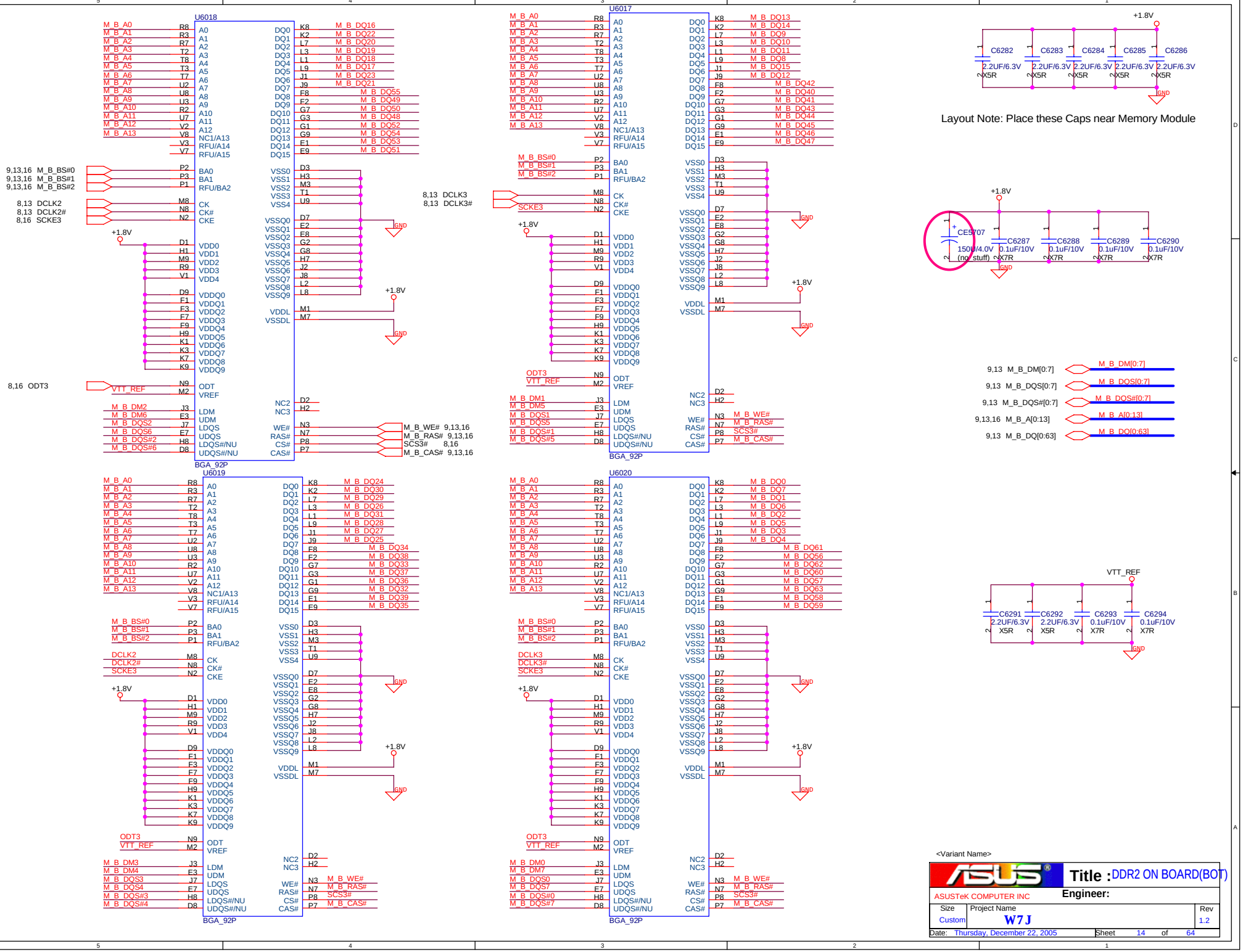
Engineer:

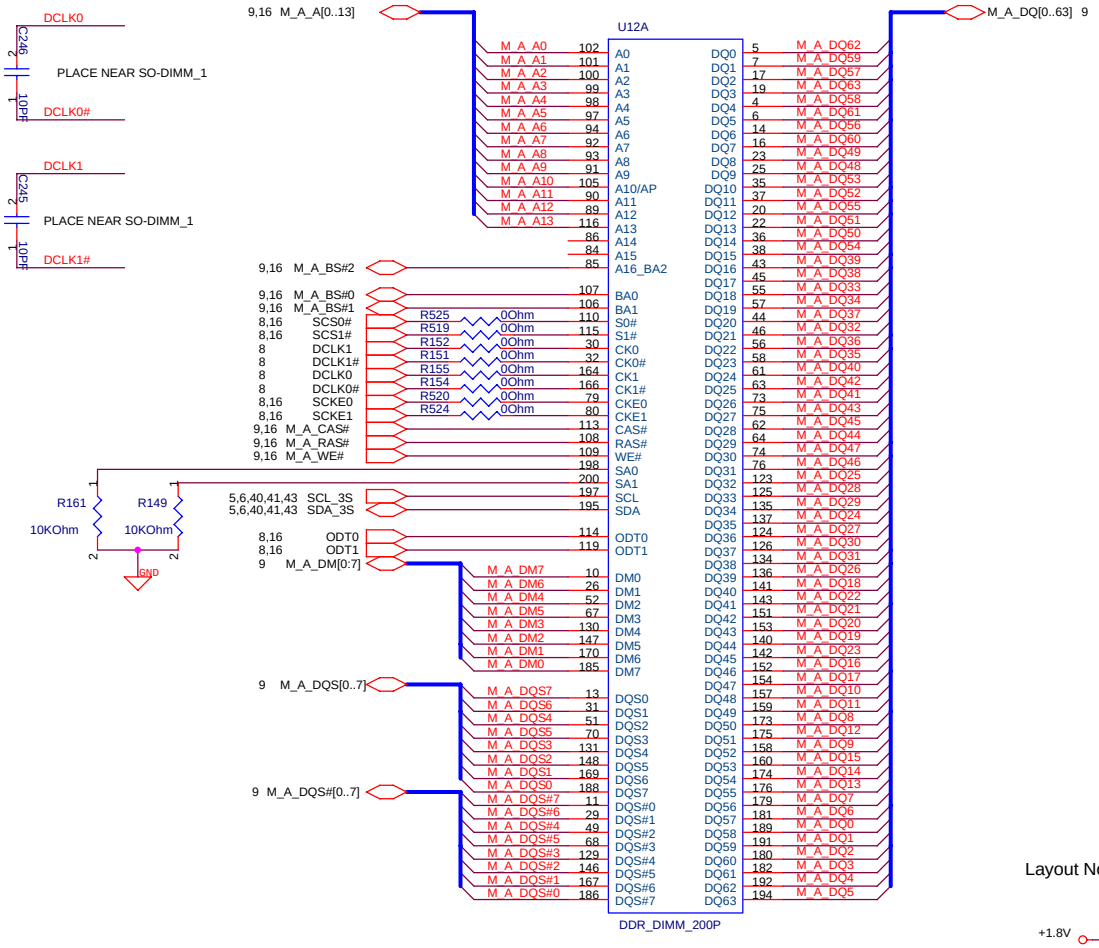
Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 12 of 64

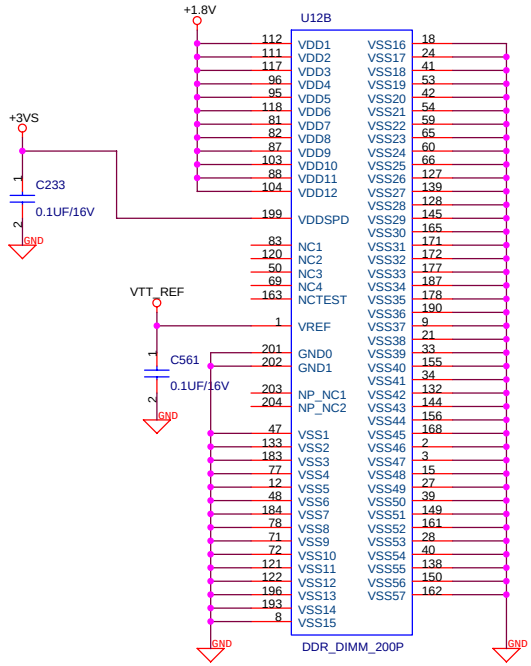
HIGH = LANES REVERSED


U6014
U6013
U6015
U6016
BGA_92P
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_B_A13
M_B_BS#0
M_B_BS#1
M_B_BS#2
DCLK2
DCLK2#
DCLK3
DCLK3#
SCKE2
M_B_DM2
M_B_DM6
M_B_DQS2
M_B_DQS6
M_B_DQS#2
M_B_DQS#6
M_B_DM3
M_B_DM4
M_B_DQS3
M_B_DQS4
M_B_DQS#3
M_B_DQS#4
M_B_DM1
M_B_DM5
M_B_DQS1
M_B_DQS5
M_B_DQS#1
M_B_DQS#5
M_B_DM0
M_B_DM7
M_B_DQS0
M_B_DQS7
M_B_DQS#0
M_B_DQS#7
ODT2
VTT_REF
M_B_WE#
M_B_RAS#
M_B_CAS#
SCS2#
+1.8V
GND
8,14 DCLK3
8,14 DCLK3#
M_B_WE# 9,14,16
M_B_RAS# 9,14,16
SCS2# 8,16
M_B_CAS# 9,14,16
C6267
C6268
C6269
C6270
C6271
2.2UF/6.3V
X5R
Layout Note: Place these Caps near Memory Module
CE5706
150U/4.0V
C6272
C6273
C6274
C6275
0.1uF/10V
X7R
9,14 M_B_DM[0:7]
9,14 M_B_DQS[0:7]
9,14 M_B_DQS#[0:7]
9,14,16 M_B_A[0:13]
9,14 M_B_DQ[0:63]
Place either terminator on each side
C6276
4PF/50V
R6564
R6565
200Ohm
C6277
R6566
R6567
C6278
C6279
C6280
C6281
<Variant Name>
Title : DDRON BOARD(TOP)
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
W7J
Rev
1.2
Date: Thursday, December 22, 2005
Sheet 13 of 64

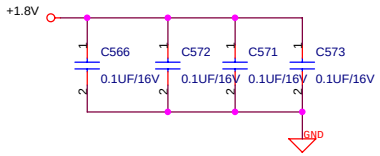

U6018
U6017
U6019
U6020
BGA_92P
M_B_A0
M_B_A1
M_B_A2
M_B_A3
M_B_A4
M_B_A5
M_B_A6
M_B_A7
M_B_A8
M_B_A9
M_B_A10
M_B_A11
M_B_A12
M_B_A13
M_B_BS#0
M_B_BS#1
M_B_BS#2
DCLK2
DCLK2#
SCKE3
DCLK3
DCLK3#
ODT3
VTT_REF
M_B_DM2
M_B_DM6
M_B_DQS2
M_B_DQS6
M_B_DQS#2
M_B_DQS#6
M_B_DM3
M_B_DM4
M_B_DQS3
M_B_DQS4
M_B_DQS#3
M_B_DQS#4
M_B_DM1
M_B_DM5
M_B_DQS1
M_B_DQS5
M_B_DQS#1
M_B_DQS#5
M_B_DM0
M_B_DM7
M_B_DQS0
M_B_DQS7
M_B_DQS#0
M_B_DQS#7
M_B_WE#
M_B_RAS#
SCS3#
M_B_CAS#
+1.8V
GND
VDD0
VDD1
VDD2
VDD3
VDD4
VDDQ0
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9
VSS0
VSS1
VSS2
VSS3
VSS4
VSSQ0
VSSQ1
VSSQ2
VSSQ3
VSSQ4
VSSQ5
VSSQ6
VSSQ7
VSSQ8
VSSQ9
VDDL
VSSDL
NC1/A13
RFU/A14
RFU/A15
RFU/BA2
LDM
UDM
LDQS
UDQS
LDQS#/NU
UDQS#/NU
M_B_DQ16
M_B_DQ22
M_B_DQ20
M_B_DQ19
M_B_DQ18
M_B_DQ17
M_B_DQ23
M_B_DQ21
M_B_DQ55
M_B_DQ49
M_B_DQ50
M_B_DQ48
M_B_DQ52
M_B_DQ54
M_B_DQ53
M_B_DQ51
M_B_DQ13
M_B_DQ14
M_B_DQ9
M_B_DQ10
M_B_DQ11
M_B_DQ8
M_B_DQ15
M_B_DQ12
M_B_DQ42
M_B_DQ40
M_B_DQ41
M_B_DQ43
M_B_DQ44
M_B_DQ45
M_B_DQ46
M_B_DQ47
M_B_DQ24
M_B_DQ30
M_B_DQ29
M_B_DQ26
M_B_DQ31
M_B_DQ28
M_B_DQ27
M_B_DQ25
M_B_DQ34
M_B_DQ38
M_B_DQ33
M_B_DQ37
M_B_DQ36
M_B_DQ32
M_B_DQ39
M_B_DQ35
M_B_DQ0
M_B_DQ7
M_B_DQ1
M_B_DQ6
M_B_DQ2
M_B_DQ5
M_B_DQ3
M_B_DQ4
M_B_DQ61
M_B_DQ56
M_B_DQ62
M_B_DQ60
M_B_DQ57
M_B_DQ63
M_B_DQ58
M_B_DQ59
9,13,16 M_B_BS#0
9,13,16 M_B_BS#1
9,13,16 M_B_BS#2
8,13 DCLK2
8,13 DCLK2#
8,16 SCKE3
8,13 DCLK3
8,13 DCLK3#
8,16 ODT3
M_B_WE# 9,13,16
M_B_RAS# 9,13,16
SCS3# 8,16
M_B_CAS# 9,13,16
C6282
C6283
C6284
C6285
C6286
2.2UF/6.3V
X5R
Layout Note: Place these Caps near Memory Module
CE5707
150UF/4.0V
(no_stuff)
C6287
C6288
C6289
C6290
0.1uF/10V
X7R
C6291
C6292
C6293
C6294
9,13 M_B_DM[0:7]
9,13 M_B_DQS[0:7]
9,13 M_B_DQS#[0:7]
9,13,16 M_B_A[0:13]
9,13 M_B_DQ[0:63]
<Variant Name>
Title : DDR2 ON BOARD(BOT)
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
W7 J
Rev
1.2
Date: Thursday, December 22, 2005
Sheet 14 of 64



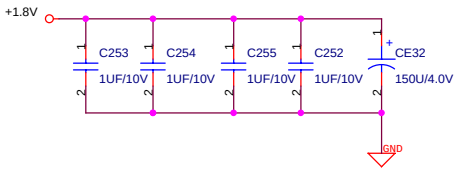
Top SO-DIMM:
12-025122005



Layout Note: Place these Caps near SO DIMM 1



Layout Note: Place these Caps near SO DIMM 1



TOP SIDE:
Channel A

<Variant Name>

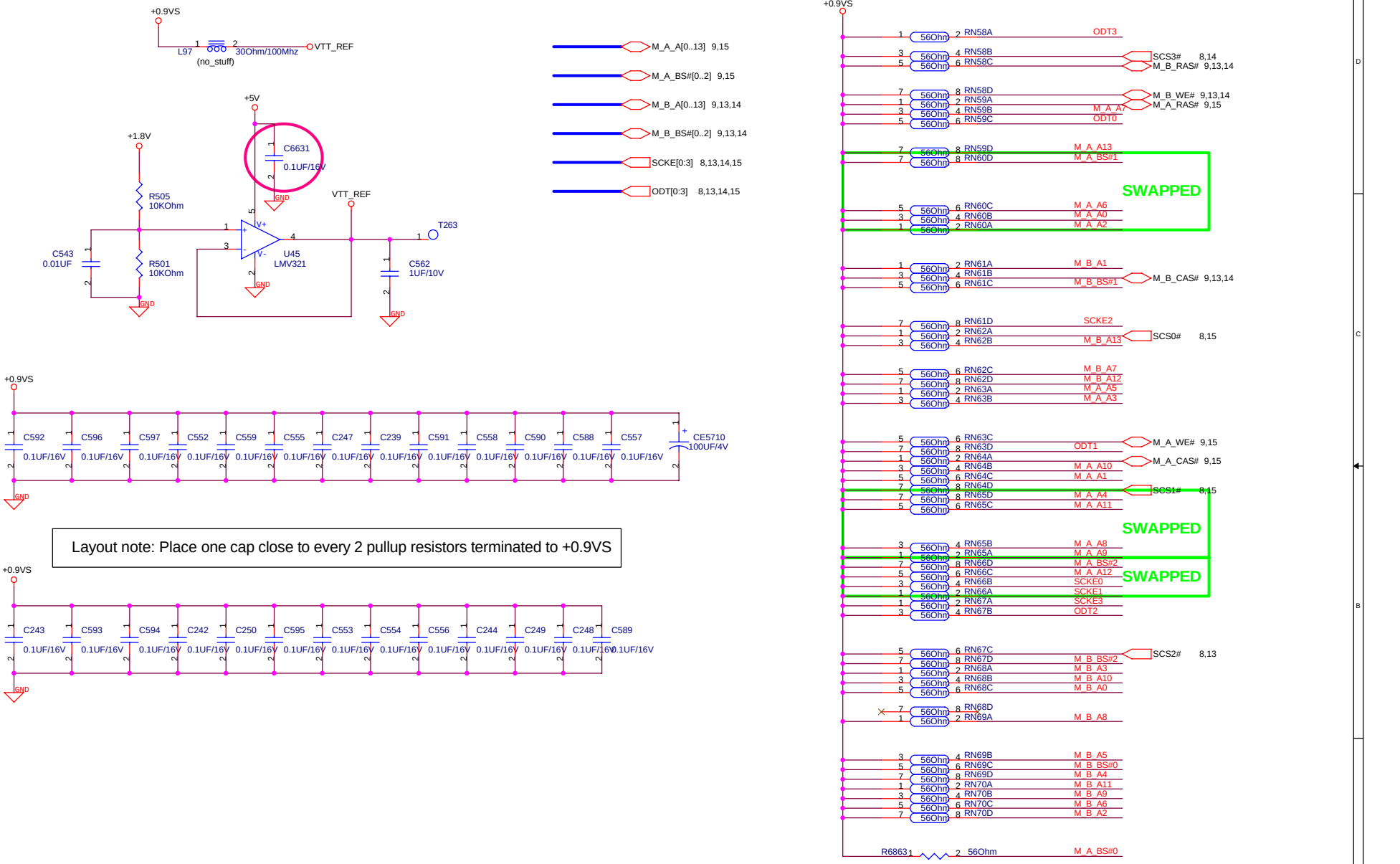
Title : DDR2 SO-DIMM

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 15 of 64



<Variant Name>

ASUSTeK COMPUTER INC

Title : DDR2 ADDR TERM

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 16 of 64

Escape use difference wire trace

PCIE LAN REVERSE

U6028A
G72MG3

26 PLT_RST#

6 CLK_PCIE_PEG
6 CLK_PCIE_PEG#

8 PEG_RXP[0..15]
8 PEG_RXN[0..15]

8 PEG_G_RXP[0..15]
8 PEG_G_RXN[0..15]

PLACE NEAR BALLS

PLACE NEAR GPU

PLACE NEAR BALLS

PLACE NEAR BALLS

PLACE NEAR GPU

PLACE NEAR GPU

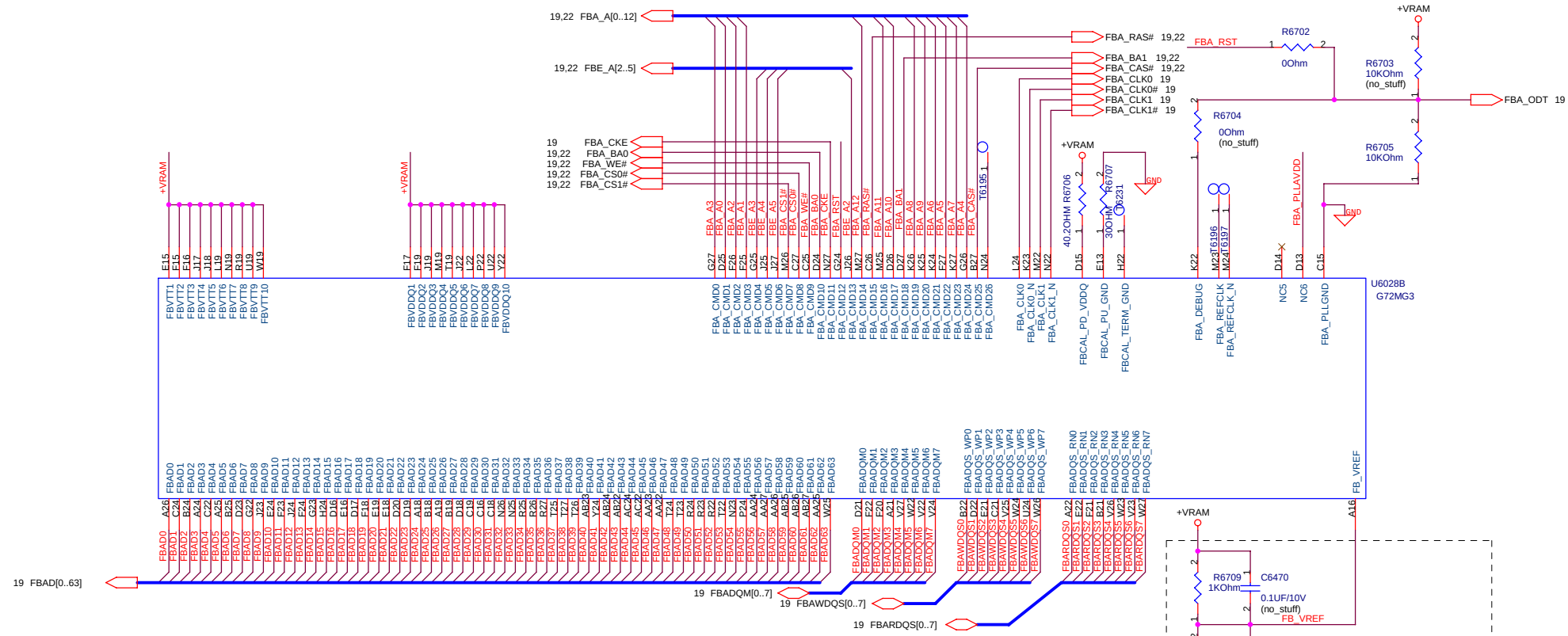
PLACE NEAR BALLS

PLACE NEAR BALLS

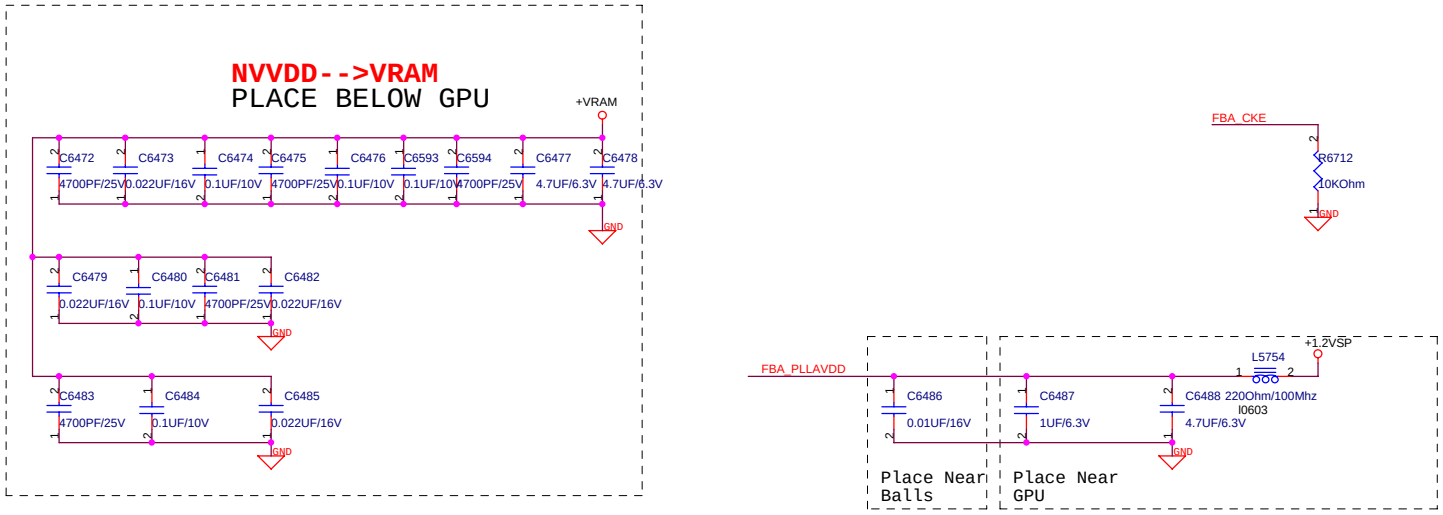
Power Seq.
+3VS --> +NV_VDD
+3VS --> +FBVDDQ(1.9VS)
+NV_VDD --> +FBVDDQ(2.0VS)
+3VS --> +1.2VS

<Variant Name>

PROJECT: W7J	REVISION 1.2	DATE: Thursday, December 22, 2005	DESCRIPTION: G72M64: PCIE	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 17 OF 64		RELEASE DATE :	

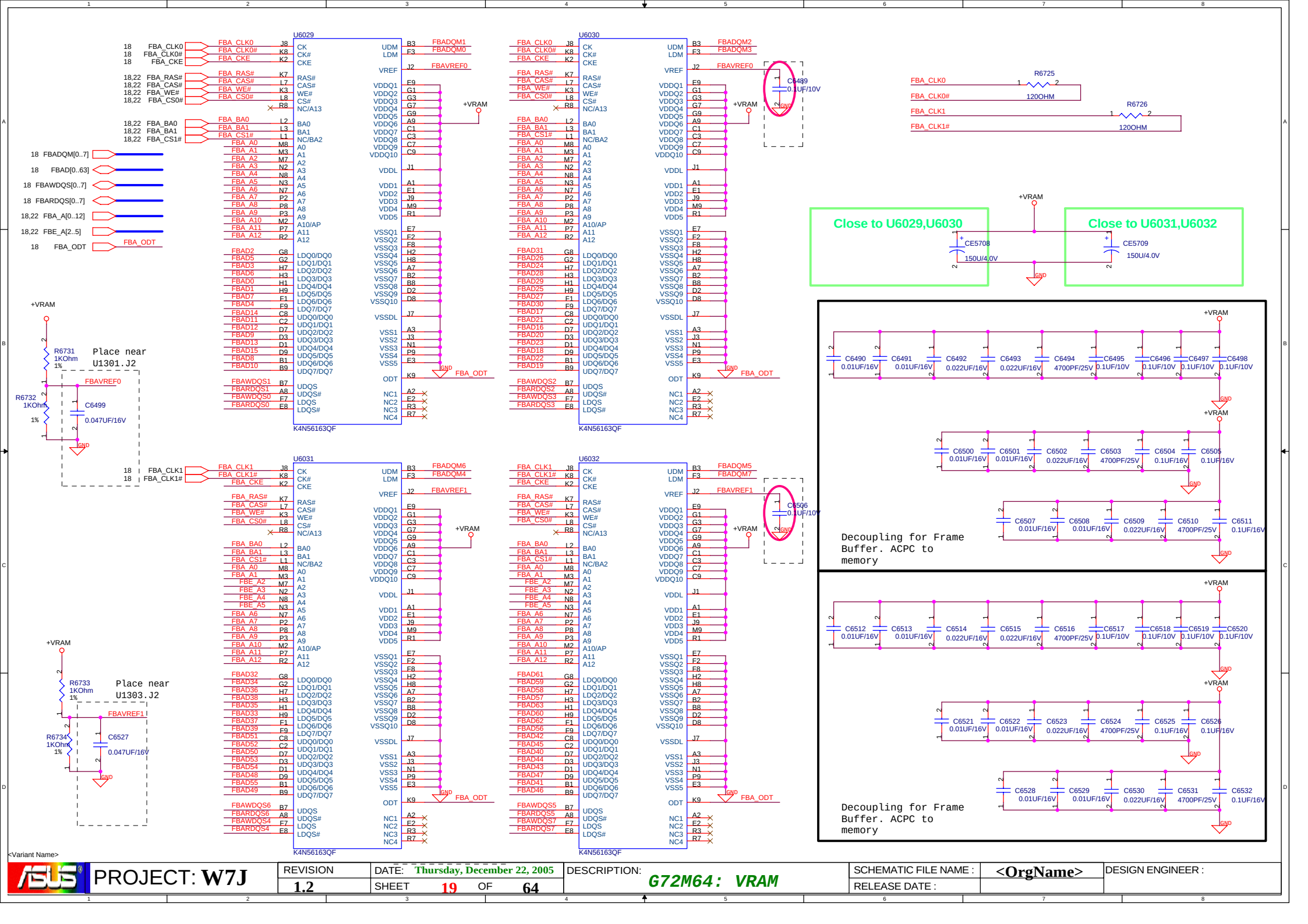


GDDR2 16x16 FBVDDQ 1.8V 84PIN



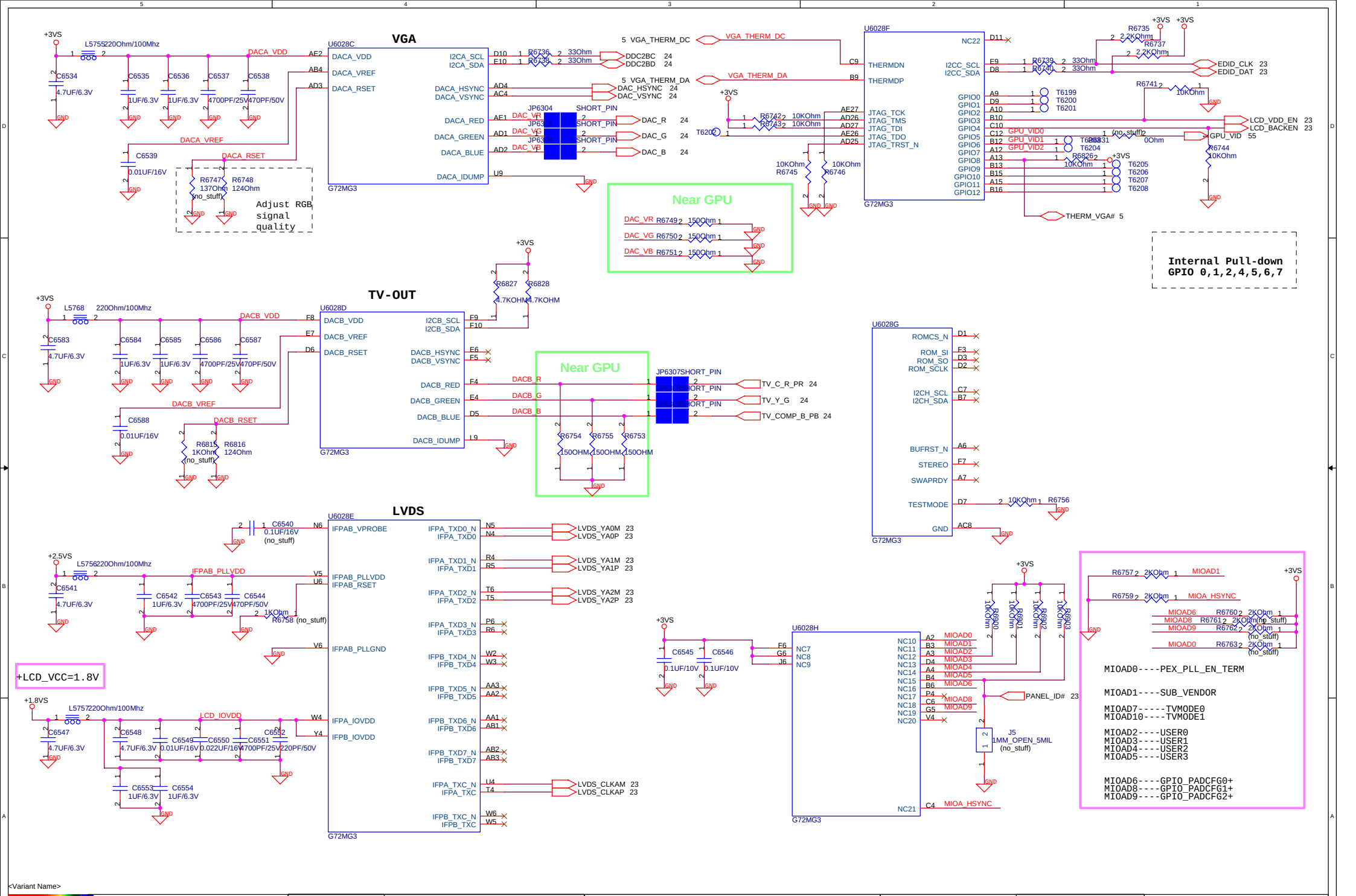
<Variant Name>

PROJECT: W7J	REVISION 1.2	DATE: Thursday, December 22, 2005	DESCRIPTION: G72M64: FB	SCHEMATIC FILE NAME : RELEASE DATE :	<OrgName> DESIGN ENGINEER :
		SHEET 18 OF 64			



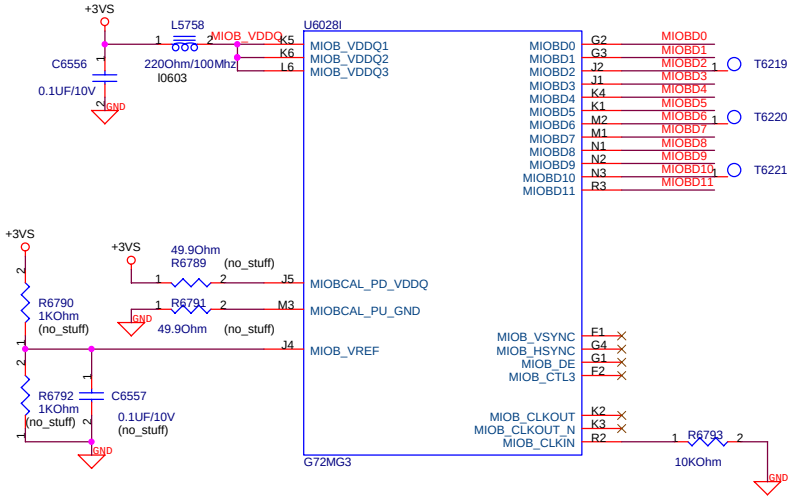
<Variant Name>

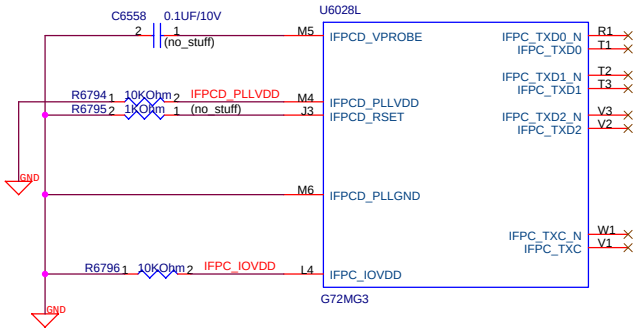
PROJECT: W7J	REVISION 1.2	DATE: Thursday, December 22, 2005	DESCRIPTION: G72M64: VRAM	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 19 OF 64		RELEASE DATE :	

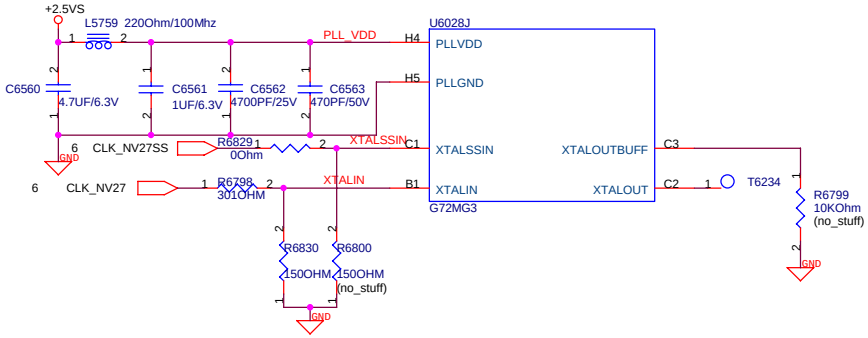


<Variant Name>

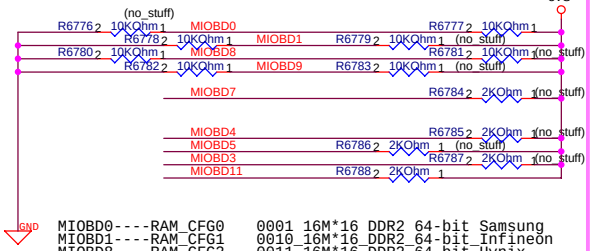
PROJECT: W7J	REVISION 1.2	DATE: Thursday, December 22, 2005	DESCRIPTION: G72M64: RGB/LCD/ROM/GPIO	SCHEMATIC FILE NAME : <OrgName>	DESIGN ENGINEER :
		SHEET 20 OF 64		RELEASE DATE :	



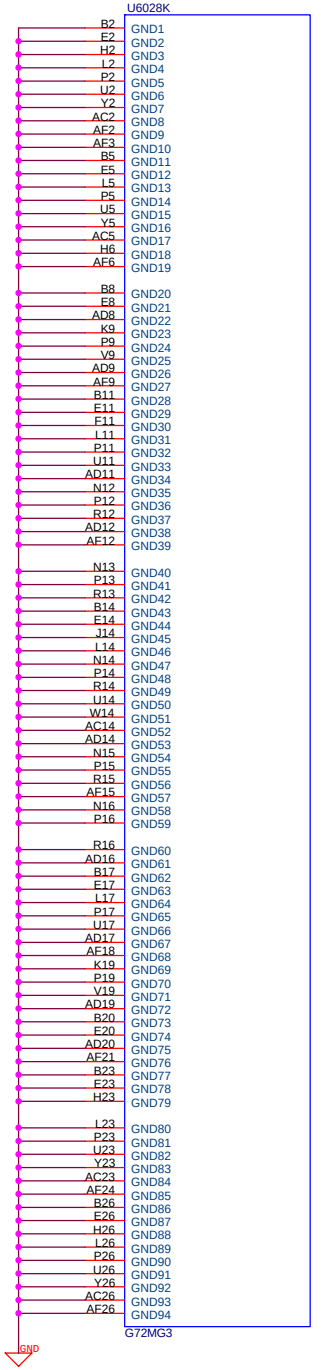




STRAP



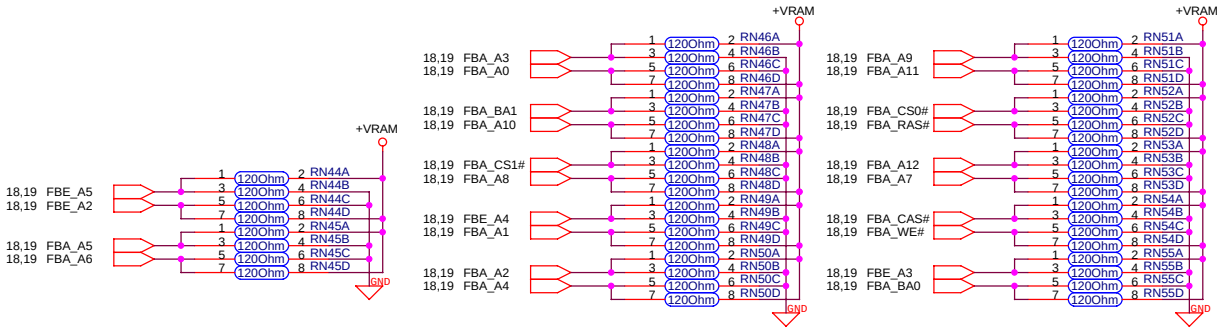

```
MIOBD0----RAM_CFG0    0001 16M*16 DDR2 64-bit Samsung
MIOBD1----RAM_CFG1    0010 16M*16 DDR2 64-bit Infineon
MIOBD8----RAM_CFG2    0011 16M*16 DDR2 64-bit Hynix
MIOBD9----RAM_CFG3
                      0101 32M*16 DDR2 64-bit Samsung
                      0110 32M*16 DDR2 64-bit Infineon
                      0111 32M*16 DDR2 64-bit Hynix


MIOBD9----RAM_CFG3    0 Full width of the frame buffer
                      1 Half width of the frame buffer


MIOBD2----CRYSTAL0    00,13.5MHZ
MIOBD6----CRYSTAL1    01,14.318MHZ
                      10,27MHZ(Default)
                      11,RESERVED

MIOBD4----PCI_DEVID0  0111 G72MV
MIOBD5----PCI_DEVID1  1000 G72M
MIOBD3----PCI_DEVID2
MIOBD11---PCI_DEVID3


MIOBD10----ROMTYPE0   00,PARALLEL
MIOB_VSYNC-ROMTYPE1   01,SERIAL_AT25F
                      10,RESERVED
                      11,LPC

MIOBD7----MOBILE_MODE
```



<Variant Name>

PROJECT: **W7J**	REVISION **1.2**	DATE: **Thursday, December 22, 2005**	DESCRIPTION: ***G72M64: MIOB/CRYSTAL/TMDS***	SCHEMATIC FILE NAME :	**<OrgName>**	DESIGN ENGINEER :
		SHEET **21** OF **64**		RELEASE DATE :		

FBA CMD/ADDR Termination



<Variant Name>

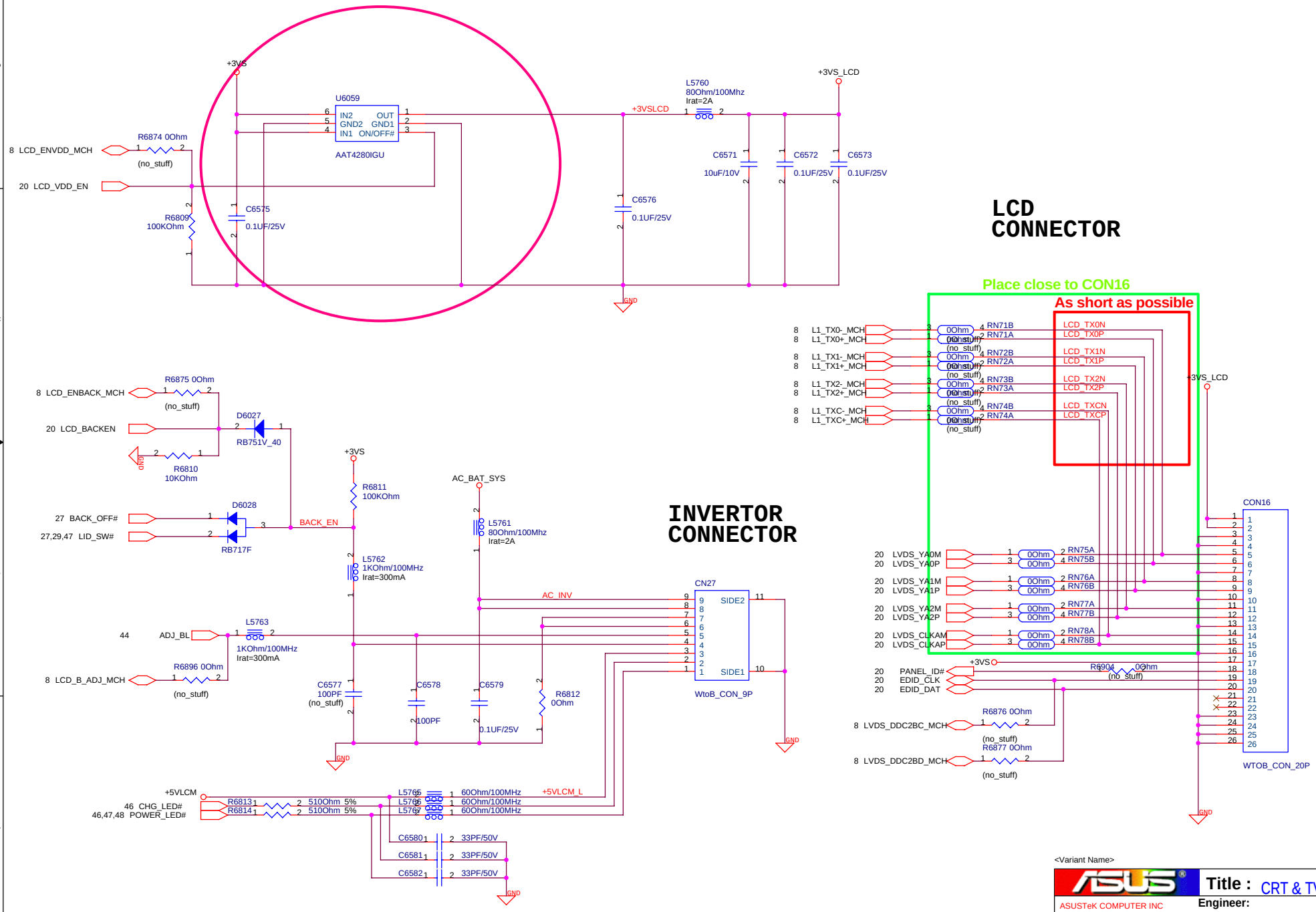
Title : G72M-Terminator

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 22 of 64



<Variant Name>

ASUSTeK COMPUTER INC

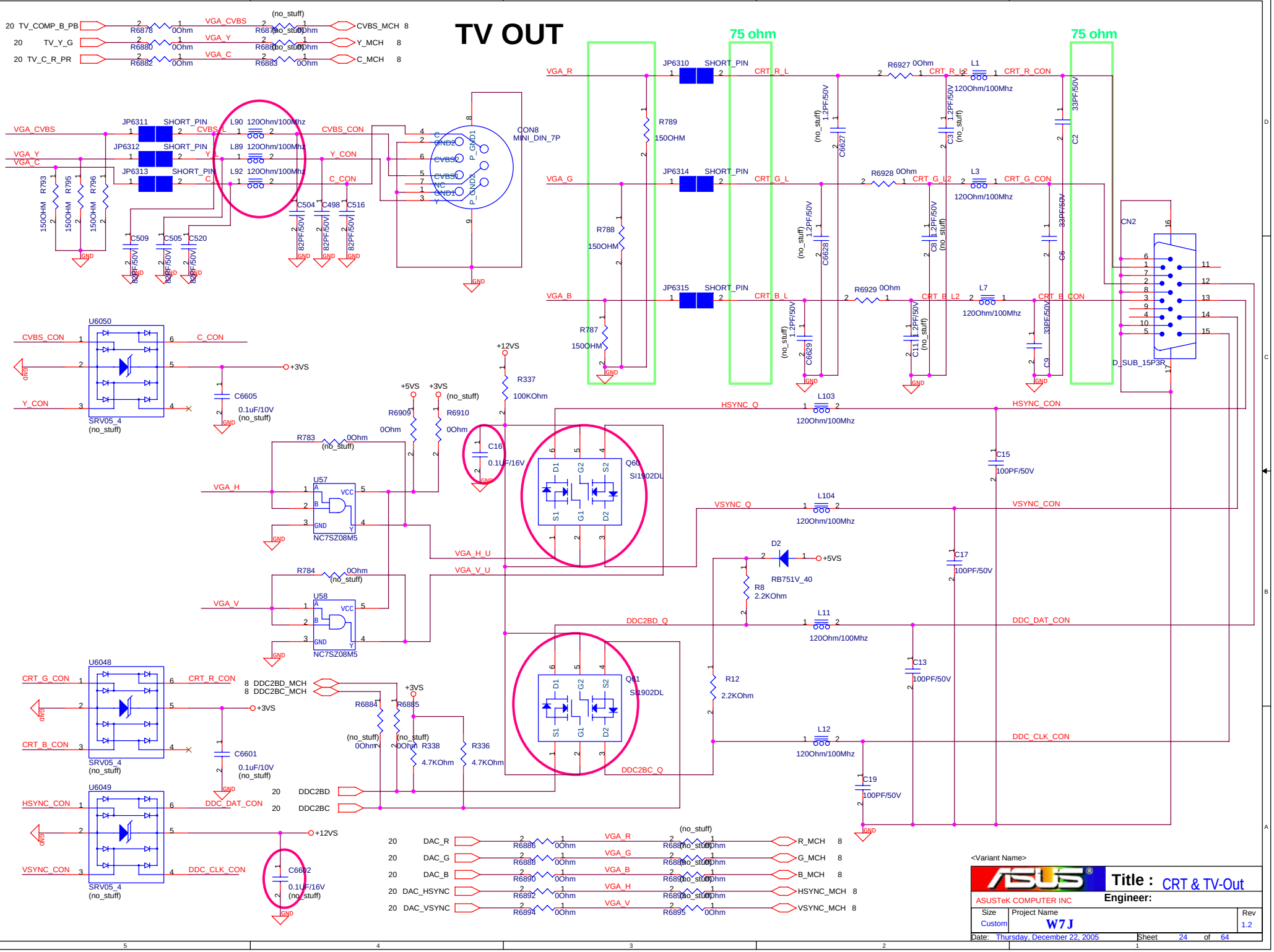
Title : CRT & TV-Out

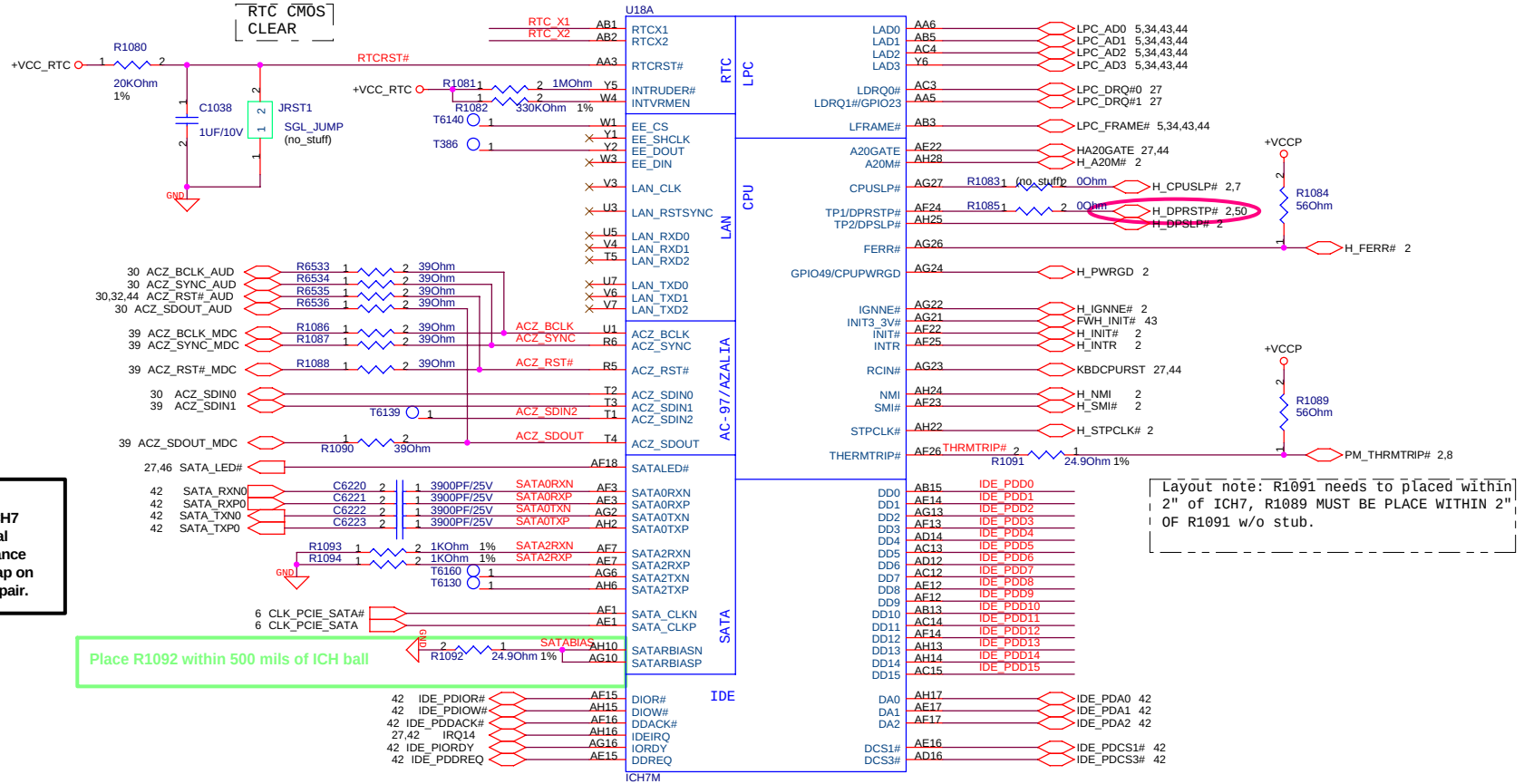
Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 23 of 64

TV OUT


75 ohm
75 ohm
CON8
MINI_DIN_7P
D_SUB_15P3R
SRV05_4
NC7SZ08M5
SI1902DL
RB751V_40
<Variant Name>
Title : CRT & TV-Out
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
W7J
Rev
1.2
Date: Thursday, December 22, 2005
Sheet 24 of 64



<Variant Name>

ASUSTeK COMPUTER INC

Title : ICH7-M (1)

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 25 of 64

ICH7 Boot BIOS select

		GNT#5	GNT#4	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

GNT#3 without PD, if NOT top-block swap(inter high)

36 PCI_AD[0..31] — PCI_AD[0..31]

U18B — ICH7M

PCI: PCI_AD0 E18, PCI_AD1 C18, PCI_AD2 A16, PCI_AD3 F18, PCI_AD4 E16, PCI_AD5 A18, PCI_AD6 E17, PCI_AD7 A17, PCI_AD8 A15, PCI_AD9 C14, PCI_AD10 E14, PCI_AD11 D14, PCI_AD12 B12, PCI_AD13 C13, PCI_AD14 G15, PCI_AD15 G13, PCI_AD16 E12, PCI_AD17 C11, PCI_AD18 D11, PCI_AD19 A11, PCI_AD20 A10, PCI_AD21 F11, PCI_AD22 F10, PCI_AD23 E9, PCI_AD24 D9, PCI_AD25 B9, PCI_AD26 A8, PCI_AD27 A6, PCI_AD28 C7, PCI_AD29 B6, PCI_AD30 E6, PCI_AD31 D6

REQ0# D7 — PCI_REQ#0 27,36
GNT0# E7 — PCI_GNT#0 36
REQ1# C16 — PCI_REQ#1 27 — T6133
GNT1# D16 — T6170
REQ2# C17 — PCI_REQ#2 27
GNT2# D17 — R6403 1KOhm (no_stuff)
REQ3# E13 — PCI_REQ#3 27
GNT3# F13
REQ4#/GPIO22 A13 — PCI_REQ#4 27 — T6135
GNT4#/GPIO48 A14
GPIO1/REQ5# C8 — PCI_REQ#5 27 — T6136
GPIO17/GNT5# D8

C/BE0# B15 — PCI_C/BE#0 36
C/BE1# C12 — PCI_C/BE#1 36
C/BE2# D12 — PCI_C/BE#2 36
C/BE3# C15 — PCI_C/BE#3 36

IRDY# A7 — PCI_IRDY# 27,36
PAR E10 — PCI_PAR 36
PCIRST# B18 — PCI_RST#_ICH
DEVSEL# A12 — PCI_DEVSEL# 27,36
PERR# C9 — PCI_PERR# 27,36
PLOCK# E11 — PCI_LOCK# 27
SERR# B10 — PCI_SERR# 27,36
STOP# F15 — PCI_STOP# 27,36
TRDY# F14 — PCI_TRDY# 27,36
FRAME# F16 — PCI_FRAME# 27,36

PLTRST# C26 — PLT_RST#_SB
PCICLK A9 — CLK_ICHPCI 6
PME# B19

+3VSUS — R6568 10KOhm

Interrupt I/F:
27 PCI_INTA# A3 — PIRQA# G8 — PCI_INTE# 27,36
27 PCI_INTB# B4 — PIRQB# F7 — PCI_INTF# 27,36
27 PCI_INTC# C5 — PIRQC# F8 — PCI_INTG# 27
27 PCI_INTD# B5 — PIRQD# G7 — PCI_INTH# 27

GPIO2/PIRQE#, GPIO3/PIRQF#, GPIO4/PIRQG#, GPIO5/PIRQH#

MISC:
T400 1 AE5 — RSVD_1
T403 1 AD5 — RSVD_2
T406 1 AG4 — RSVD_3
T409 1 AH4 — RSVD_4
T411 1 AD9 — RSVD_5
RSVD_6 AE9 1 T401
RSVD_7 AG8 1 T404
RSVD_8 AH8 1 T407
RSVD_9 F21 1 T410
MCH_SYNC# AH20 — MCH_SYNC# 8

pull up to +3VS by internal pull-up resistor

U18D — ICH7M

PCI-Express / Direct Media Interface:
40 PCIE_RXN1 — 0.1UF/10V — C1047 — PETN1 — F26 PERn1
40 PCIE_RXP1 — 0.1UF/10V — C1048 — PETP1 — F25 PERp1
40 PCIE_TXN1 — E28 PETn1
40 PCIE_TXP1 — E27 PETp1
38 PCIE_RXN2 — 0.1UF/10V — C1049 — PETN2 — H26 PERn2
38 PCIE_RXP2 — 0.1UF/10V — C1050 — PETP2 — H25 PERp2
38 PCIE_TXN2 — G28 PETn2
38 PCIE_TXP2 — G27 PETp2
41 PCIE_RXN3 — 0.1UF/10V — C1051 — PETN3 — K26 PERn3
41 PCIE_RXP3 — 0.1UF/10V — C1052 — PETP3 — K25 PERp3
41 PCIE_TXN3 — J28 PETn3
41 PCIE_TXP3 — J27 PETp3
M26 PERn4
M25 PERp4
L28 PETn4
L27 PETp4
P26 PERn5
P25 PERp5
N28 PETn5
N27 PETp5
T25 PERn6
T24 PERp6
R28 PETn6
R27 PETp6

DMI0RXN V26 — DMI_RXN0 8
DMI0RXP V25 — DMI_RXP0 8
DMI0TXN U28 — DMI_TXN0 8
DMI0TXP U27 — DMI_TXP0 8
DMI1RXN Y26 — DMI_RXN1 8
DMI1RXP Y25 — DMI_RXP1 8
DMI1TXN W28 — DMI_TXN1 8
DMI1TXP W27 — DMI_TXP1 8
DMI2RXN AB26 — DMI_RXN2 8
DMI2RXP AB25 — DMI_RXP2 8
DMI2TXN AA28 — DMI_TXN2 8
DMI2TXP AA27 — DMI_TXP2 8
DMI3RXN AD25 — DMI_RXN3 8
DMI3RXP AD24 — DMI_RXP3 8
DMI3TXN AC28 — DMI_TXN3 8
DMI3TXP AC27 — DMI_TXP3 8
DMI_CLKN AE28 — CLK_PCIE_ICH# 6
DMI_CLKP AE27 — CLK_PCIE_ICH 6
DMI_ZCOMP C25
DMI_IRCOMP D25 — DMICOMP — R1099 24.9Ohm 1% — +1.5VS
Place within 500 mils of ICH

SPI_CLK — R2
SPI_CS# — P6
SPI_ARB — P1
SPI_MOSI — P5
SPI_MISO — P2

+3V — RN18A 10KOhm (no_stuff) — RN18B 10KOhm (no_stuff) — RN18C 10KOhm (no_stuff) — RN18D 10KOhm (no_stuff)

USB:
USBP0N E1 — USB_PN0 40
USBP0P F2 — USB_PP0 40
USBP1N G4 — USB_PN1 45
USBP1P G3 — USB_PP1 45
USBP2N H1 — USB_PN2 47
USBP2P H2 — USB_PP2 47
USBP3N J4 — USB_PN3 45
USBP3P J3 — USB_PP3 45
USBP4N K1 — USB_PN4 45
USBP4P K2 — USB_PP4 45
USBP5N L4 — USB_PN5 45
USBP5P L5 — USB_PP5 45
USBP6N M1
USBP6P M2
USBP7N N4 — T405
USBP7P N3 — T408
USBRBIAS# D2 — USBBIAS — R1100 22.6Ohm 1% — GND
USBRBIAS D1
Place within 500 mils of ICH

OC0# D3 — USB_OC#0 27,40
OC1# C4
OC2# D5 — USB_OC#2 27
OC3# D4 — USB_OC#13 27,45
OC4# E5 — USB_OC#4 27,45
OC5#/GPIO29 C3 — USB_OC#5 27
OC6#/GPIO30 A2 — USB_OC#6 27
OC7#/GPIO31 B3 — USB_OC#7 27

U68D 74HC08 — 8,27,34,38,41,42,43,44 BUF_PLT_RST# — PLT_RST#_SB — +3V — C1056 0.01UF (no_stuff)

U68A 74HC08 — 36,40,42 PCI_RST# — PCI_RST#_ICH — C1053 0.1UF/16V — +3V

U68C 74HC08 — 17 PLT_RST# — R6408 0Ohm (no_stuff) — PLT_RST#_SB — R1104 0Ohm (no_stuff) — SW_RST# 27 — R1106 0Ohm — R1102 10KOhm — C1054 0.1UF/16V — +3V

U69 74LVC1G32GV — PCI_RST# — 44 SET_PCIRSTNS# — R1108 10KOhm — R1109 47KOhm — C1057 0.01UF — C1055 0.1UF/16V — +3V — PCI_RSTNS# 36,44

Can be issue SCI or SMI List: GPIO0~GPIO15
Resume Power Well GPIO List: GPIO8,11,13,14,15,24,25,27,28

Only GPI Pin: GPI0~8,11~15,26,29,30,31,40(5V),41
Only GPO Pin: GPIO16~17,19,21,23,48
Can be GPIO: GPIO24,25,27,28,33,34
Resume Power Input Pin List:
BATLOW#,AC_SDIN[0:1],LAN_RST#,
OC[7:0]#,PME#,PWRBTN#,RI#,SMBALERT#,SYS_RESET#,USBRBIAS#

<Variant Name>

ASUSTeK COMPUTER INC

Title : ICH7-M (2)

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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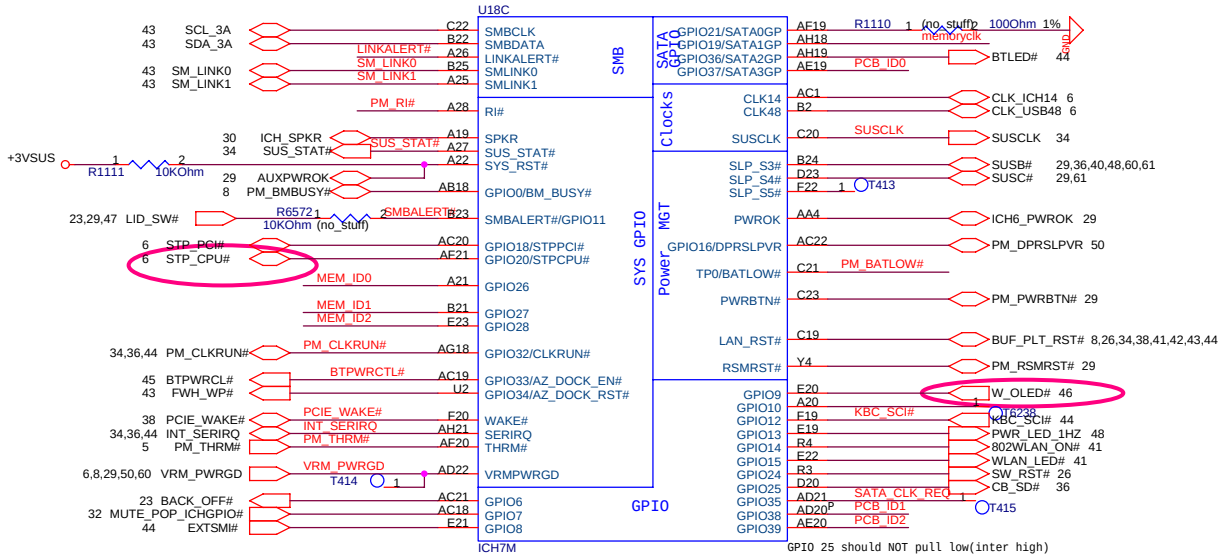
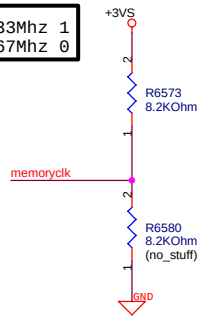
The signal has a weak internal pull down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot" mode.

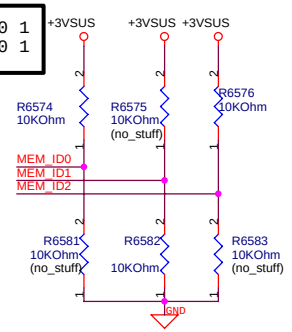


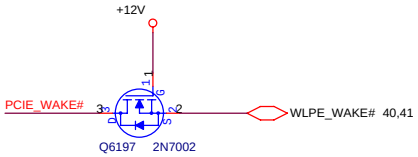
GPIO 16 should NOT pull high(inter low)

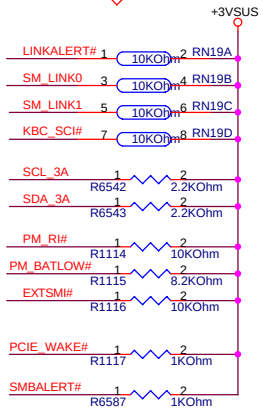
533Mhz 1
667Mhz 0

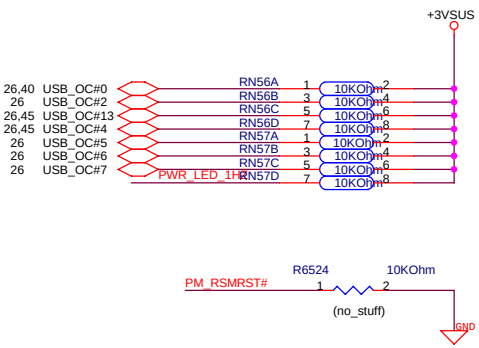


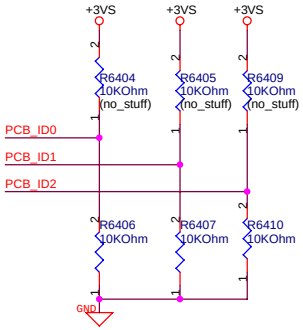
512M 1 0 1
256M 0 0 1

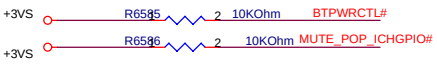


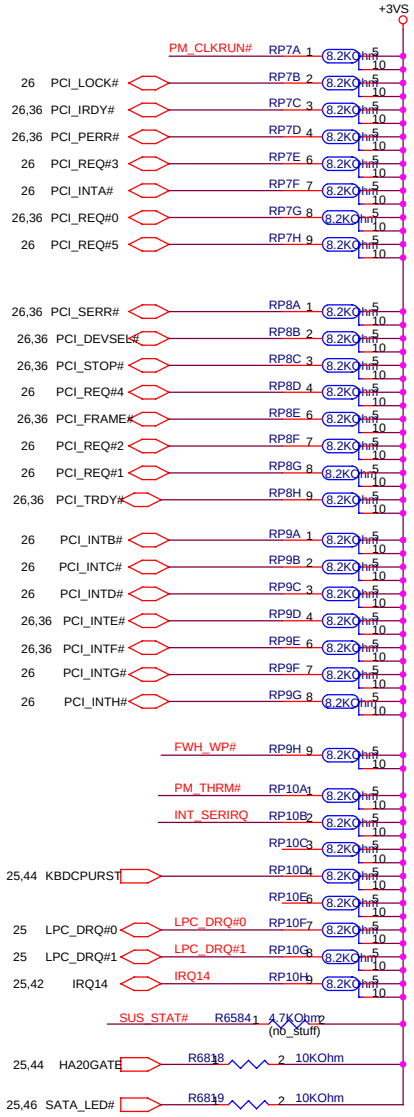






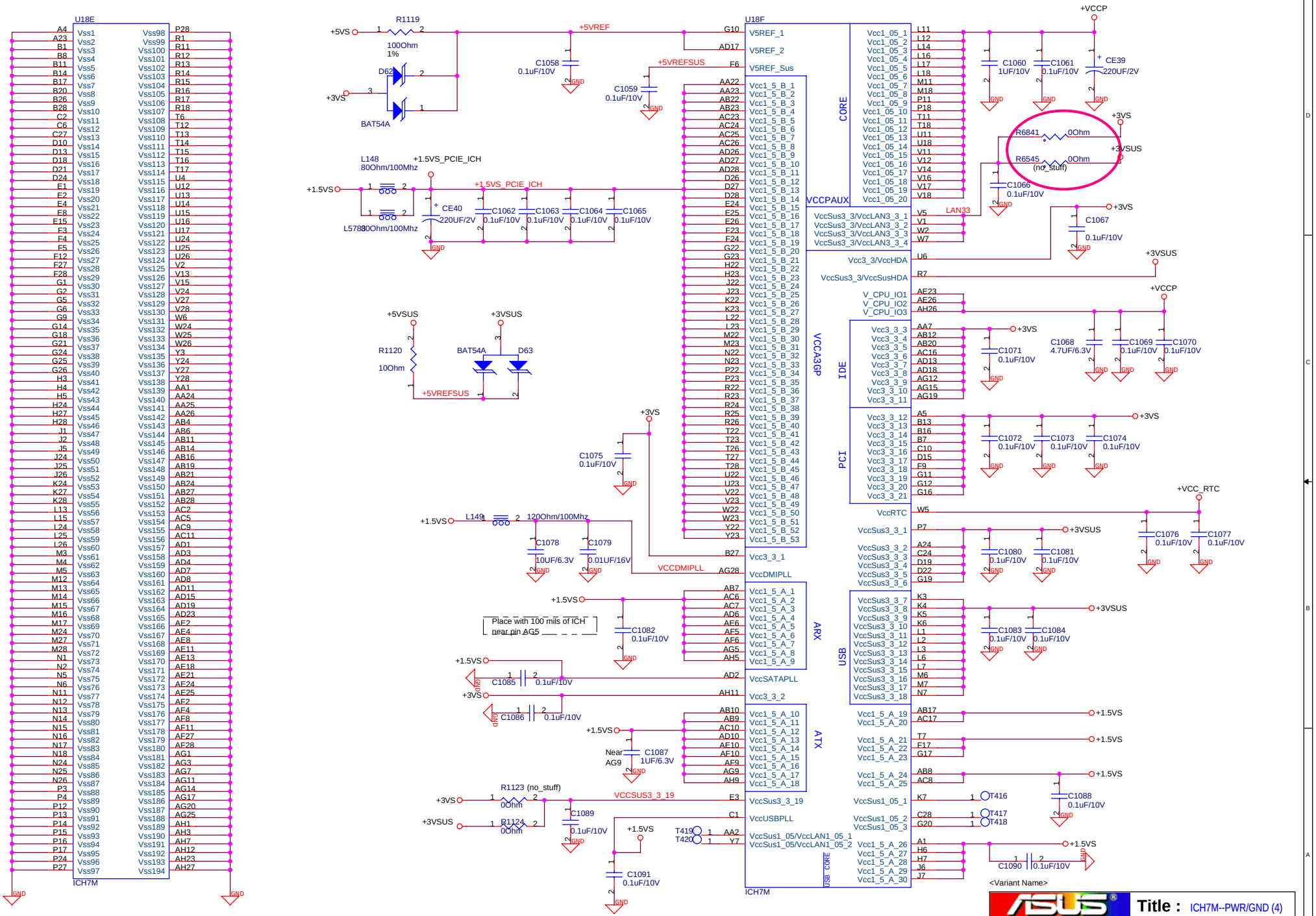






<Variant Name>

ASUSTeK COMPUTER INC	Title : ICH7M--(3)	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 27 of 64	


U18E
ICH7M
U18F
ICH7M
R1119
100Ohm
1%
BAT54A
D62
+5VS
+3VS
+5VREF
+5VREFSUS
C1058
0.1uF/10V
C1059
0.1uF/10V
L148
80Ohm/100Mhz
L57
+1.5VS_PCIE_ICH
CE40
220UF/2V
C1062
C1063
C1064
C1065
0.1uF/10V
R1120
10Ohm
BAT54A
D63
+5VSUS
+3VSUS
C1075
0.1uF/10V
L149
120Ohm/100Mhz
C1078
10UF/6.3V
C1079
0.01UF/16V
VCCDMIPLL
Place with 100 mils of ICH
near pin AG5
C1082
0.1uF/10V
C1085
C1086
C1087
1UF/6.3V
Near
AG9
R1123 (no_stuff)
0Ohm
R1124
0Ohm
VCCSUS3_3_19
C1089
C1091
T419
T420
CORE
VCCPAUX
VCCA3GP
IDE
PCI
LAN33
ARX
ATX
USB
C1060
1UF/10V
C1061
C1066
C1067
CE39
220UF/2V
R6841
0Ohm
R6545
0Ohm
(no_stuff)
C1068
4.7UF/6.3V
C1069
C1070
C1071
C1072
C1073
C1074
C1076
C1077
C1080
C1081
C1083
C1084
C1088
C1090
T416
T417
T418
VCC_RTC
<Variant Name>
Title : ICH7M--PWR/GND (4)
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
W7J
Rev
1.2
Date: Thursday, December 22, 2005
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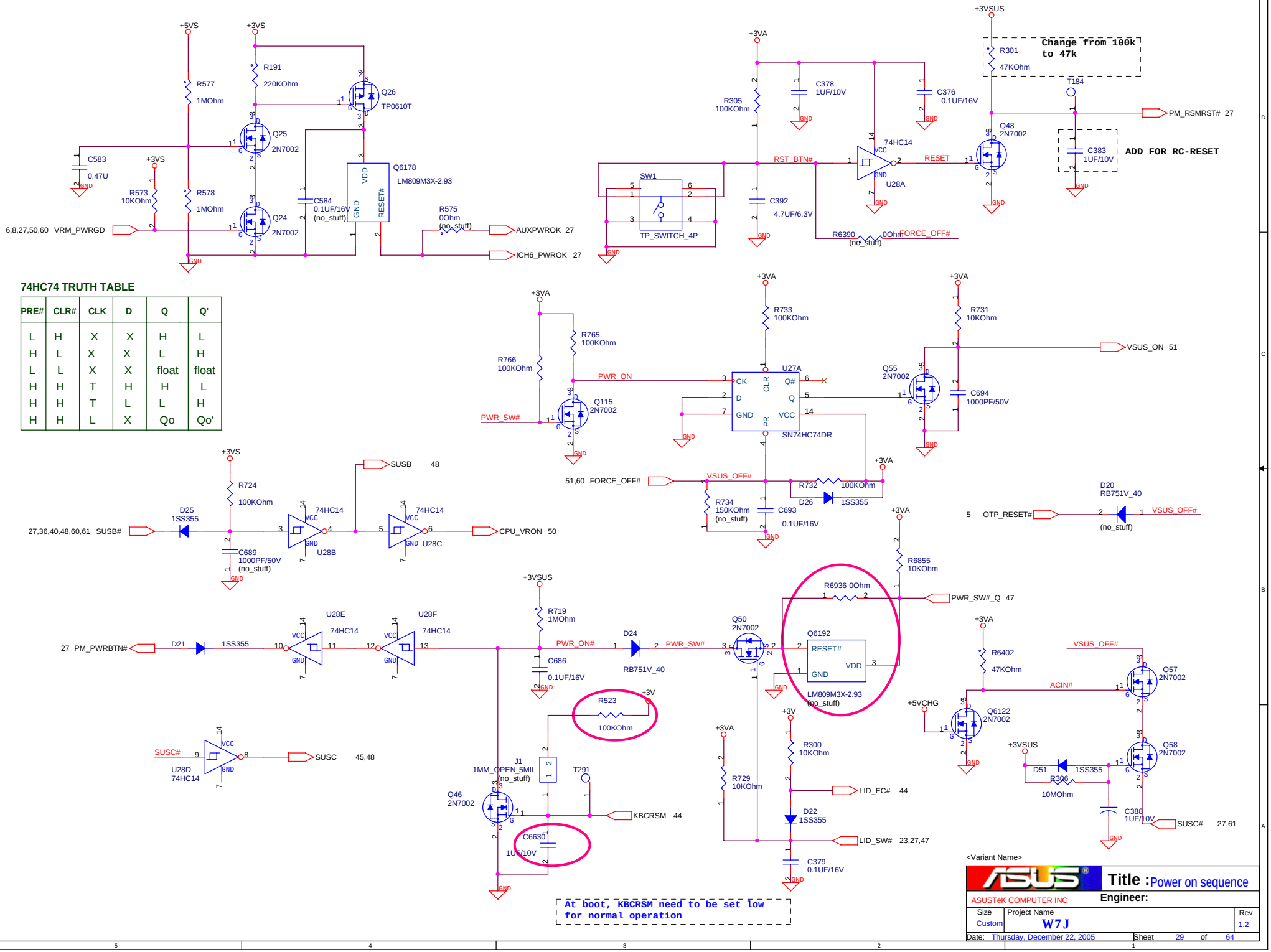
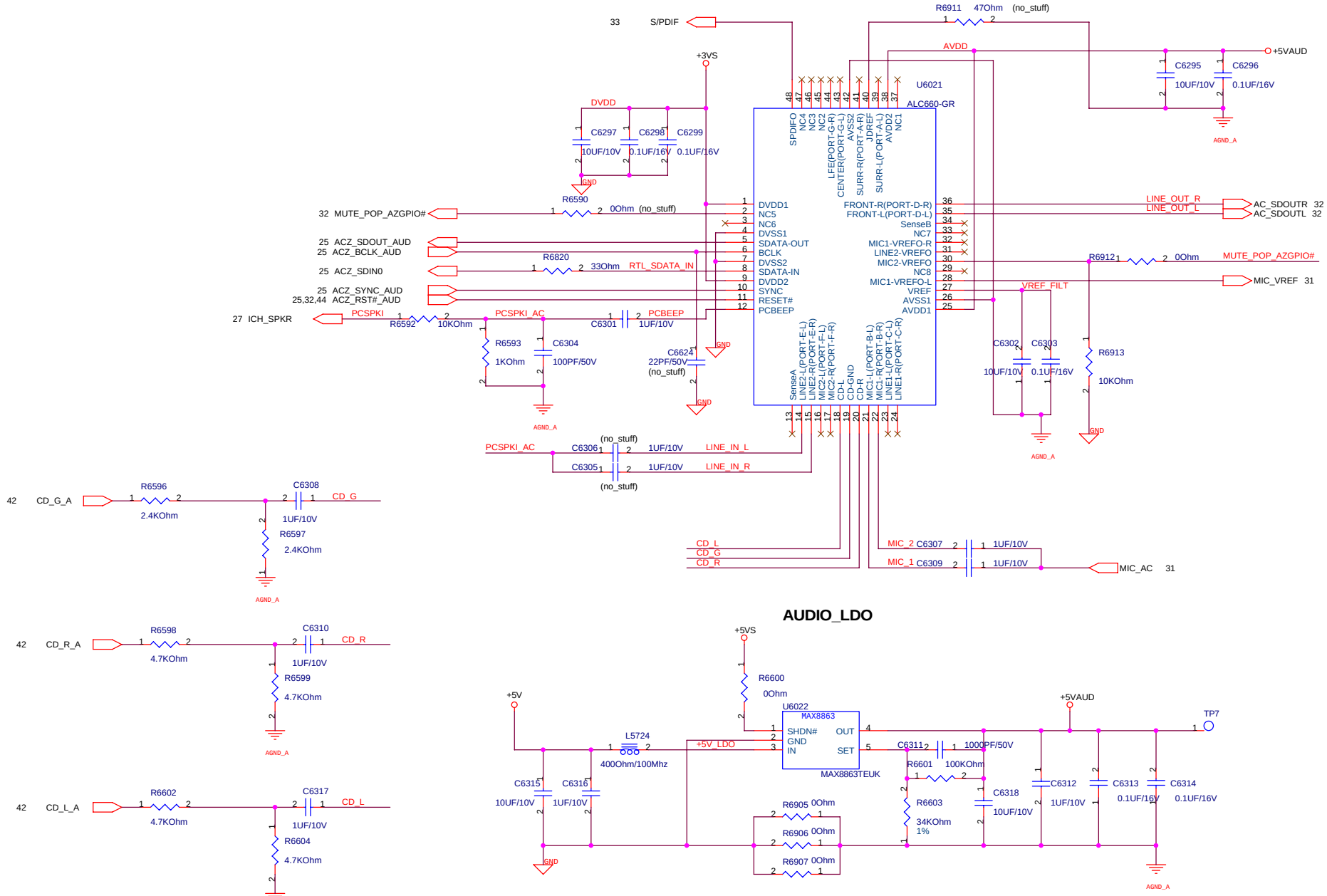

+5VS
+3VS
R577
1MOhm
R191
220KOhm
Q26
TP0610T
Q25
2N7002
C583
0.47U
R573
10KOhm
R578
1MOhm
Q24
2N7002
C584
0.1UF/16V
(no_stuff)
Q6178
LM809M3X-2.93
VDD
GND
RESET#
R575
0Ohm
(no_stuff)
6,8,27,50,60 VRM_PWRGD
AUXPWROK 27
ICH6_PWROK 27
+3VA
R305
100KOhm
C378
1UF/10V
C376
0.1UF/16V
SW1
TP_SWITCH_4P
RST_BTN#
74HC14
U28A
RESET
C392
4.7UF/6.3V
R6390
0Ohm
(no_stuff)
FORCE_OFF#
+3VSUS
R301
47KOhm
Change from 100k
to 47k
T184
PM_RSMRST# 27
Q48
2N7002
C383
1UF/10V
ADD FOR RC-RESET
74HC74 TRUTH TABLE
PRE# CLR# CLK D Q Q'
L H X X H L
H L X X L H
L L X X float float
H H T H H L
H H T L L H
H H L X Qo Qo'
+3VA
R765
100KOhm
R766
100KOhm
PWR_ON
PWR_SW#
Q115
2N7002
R733
100KOhm
U27A
CK
D
GND
CLR
PR
Q#
Q
VCC
SN74HC74DR
R731
10KOhm
Q55
2N7002
C694
1000PF/50V
VSUS_ON 51
51,60 FORCE_OFF#
VSUS_OFF#
R734
150KOhm
(no_stuff)
C693
0.1UF/16V
R732
100KOhm
D26
1SS355
+3VS
R724
100KOhm
SUSB 48
D25
1SS355
27,36,40,48,60,61 SUSB#
74HC14
U28B
U28C
C689
1000PF/50V
(no_stuff)
CPU_VRON 50
D20
RB751V_40
(no_stuff)
5 OTP_RESET#
VSUS_OFF#
+3VSUS
R719
1MOhm
U28E
U28F
74HC14
27 PM_PWRBTN#
D21
1SS355
PWR_ON#
D24
RB751V_40
PWR_SW#
C686
0.1UF/16V
R523
100KOhm
+3V
SUSC# 9
U28D
74HC14
SUSC 45,48
J1
1MM_OPEN_5MIL
(no_stuff)
T291
Q46
2N7002
KBCRSM 44
C6630
1UF/10V
Q50
2N7002
Q6192
RESET#
VDD
GND
LM809M3X-2.93
(no_stuff)
R6936 0Ohm
R6855
10KOhm
PWR_SW#_Q 47
+3VA
R729
10KOhm
R300
10KOhm
LID_EC# 44
D22
1SS355
LID_SW# 23,27,47
C379
0.1UF/16V
R6402
47KOhm
ACIN#
+5VCHG
Q6122
2N7002
Q57
2N7002
Q58
2N7002
D51
1SS355
R306
10MOhm
C388
1UF/10V
SUSC# 27,61
At boot, KBCRSM need to be set low
for normal operation
<Variant Name>
Title : Power on sequence
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 1.2
Date: Thursday, December 22, 2005
Sheet 29 of 64



<Variant Name>

ASUSTeK COMPUTER INC

Title : AZALIA_ALC660

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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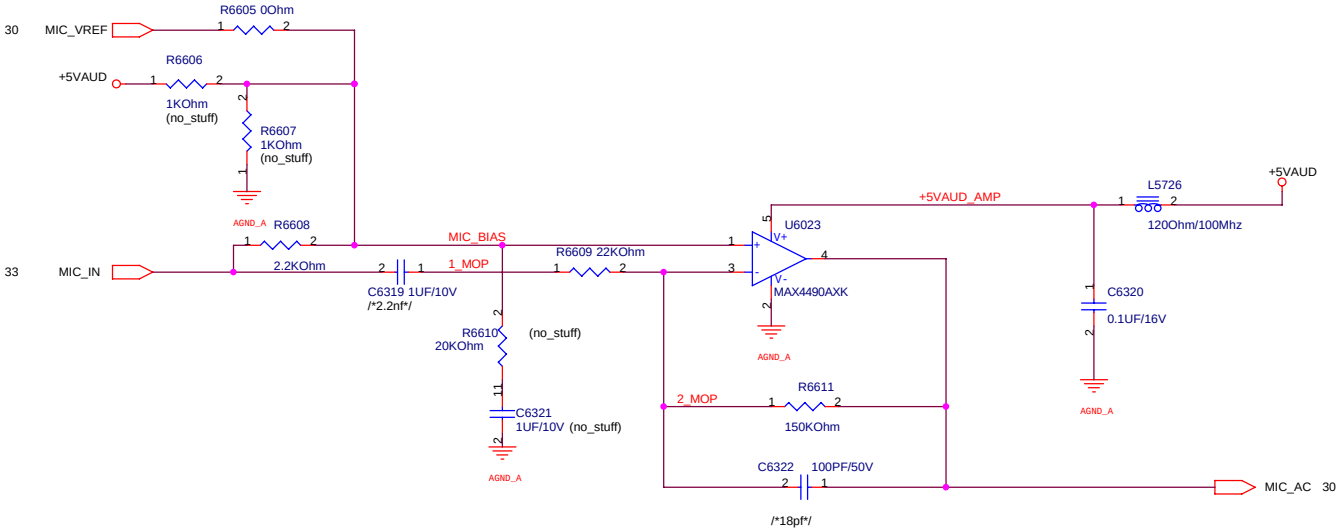
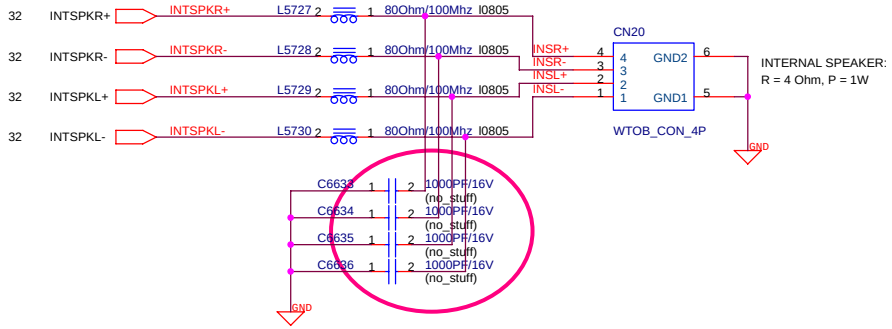
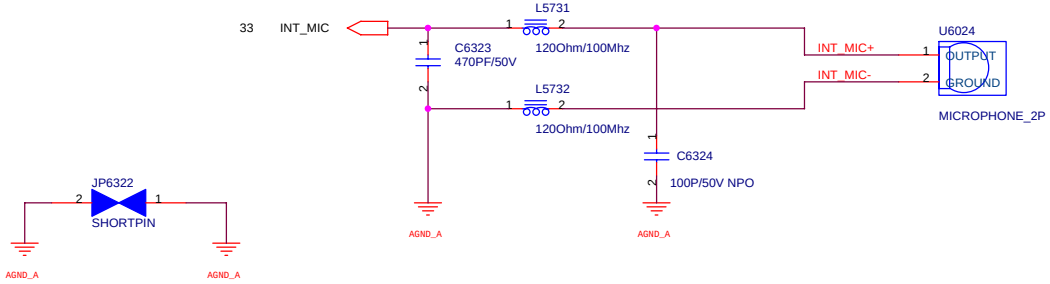
MIC PreAmp & Mic Jack







<Variant Name>

Title : MIC PREAMP & INT MIC

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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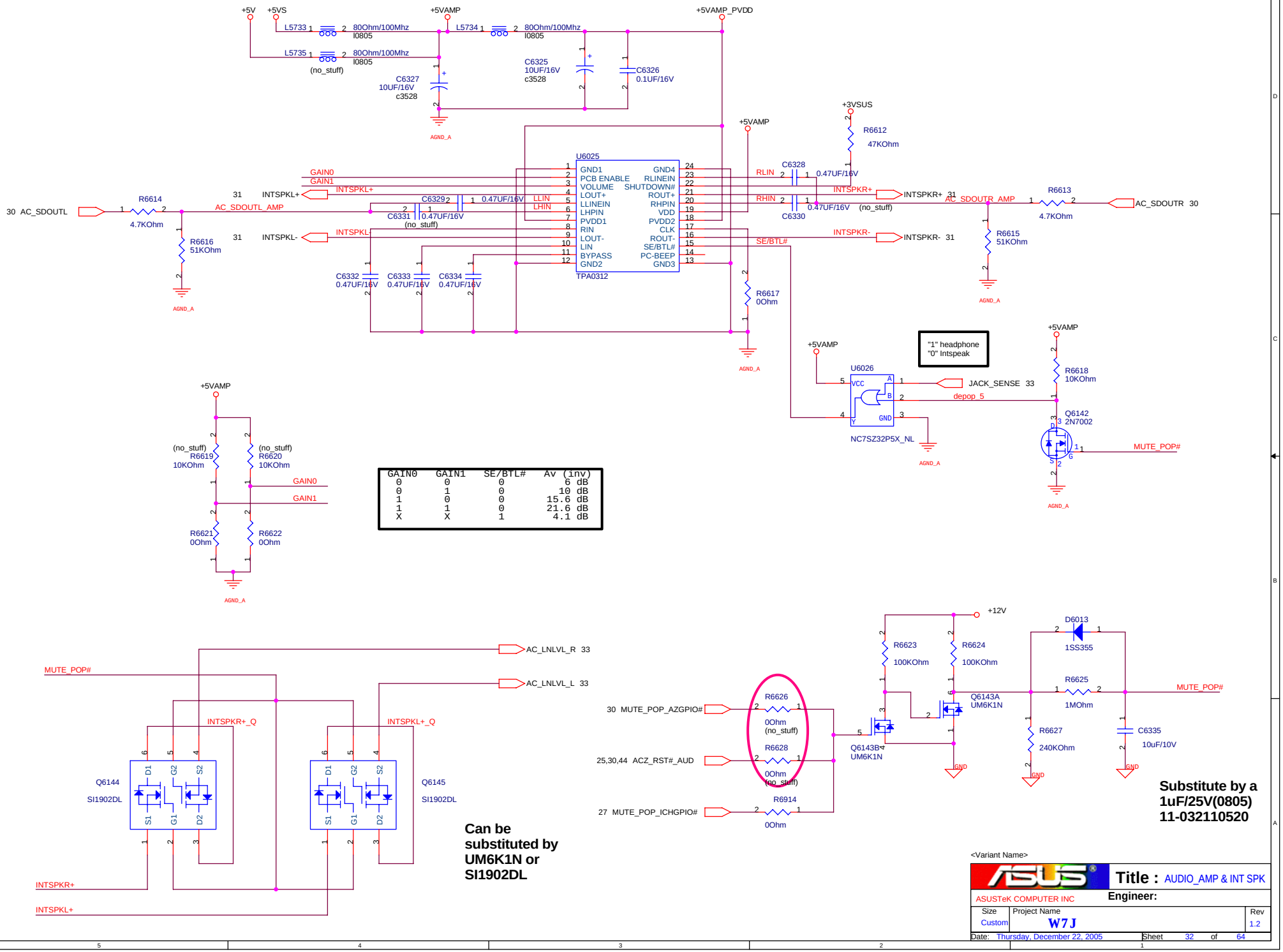

<Variant Name>

ASUSTeK COMPUTER INC

Title : AUDIO_AMP & INT SPK

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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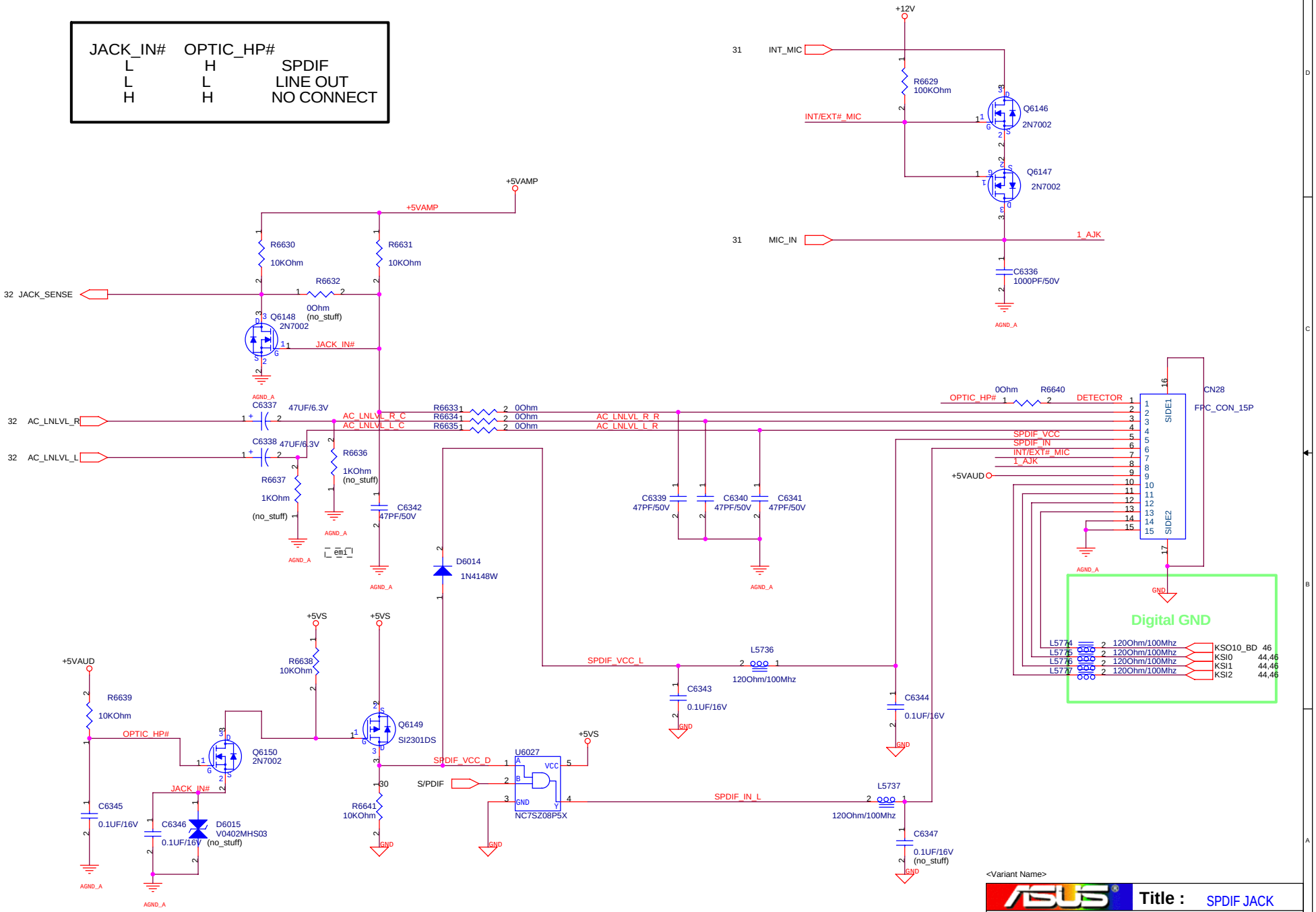
JACK_IN#	OPTIC_HP#	
L	H	SPDIF
L	L	LINE OUT
H	H	NO CONNECT



<Variant Name>

Title : SPDIF JACK

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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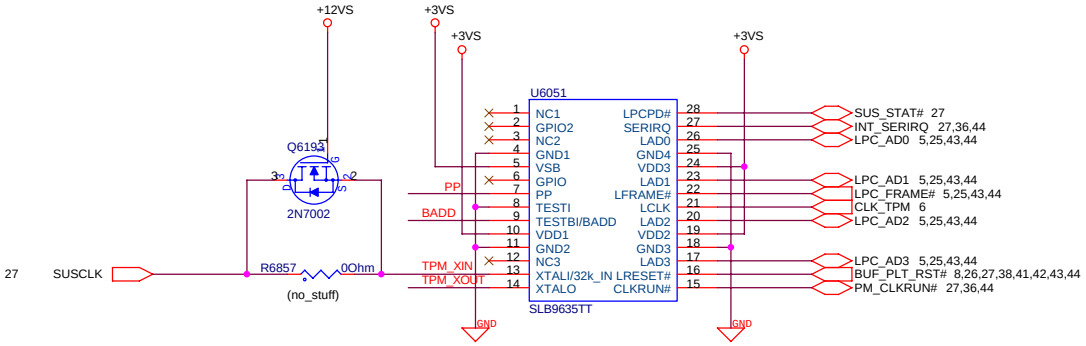
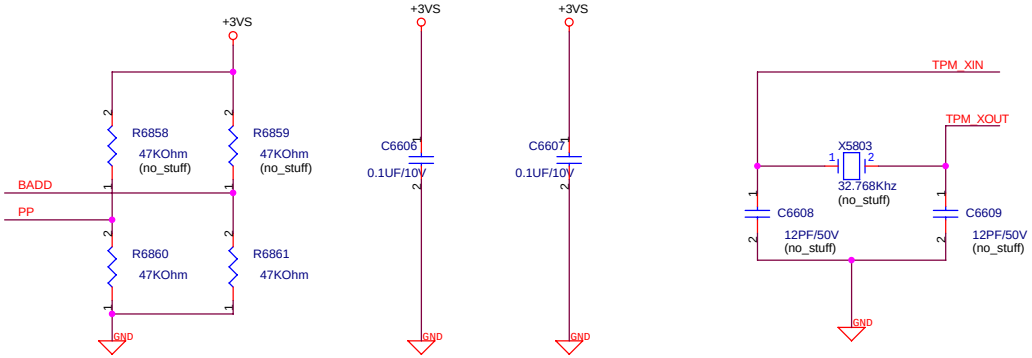
TESTBI/BADD PIN LPC ADDRESS SELETE High 4E h, LOW 2E h.
TEST PIN For normal operation, connect TESTI to GND.
PP PIN is connected to VDD, some special commands are enabled.





<Variant Name>

Title : TPM 1.2

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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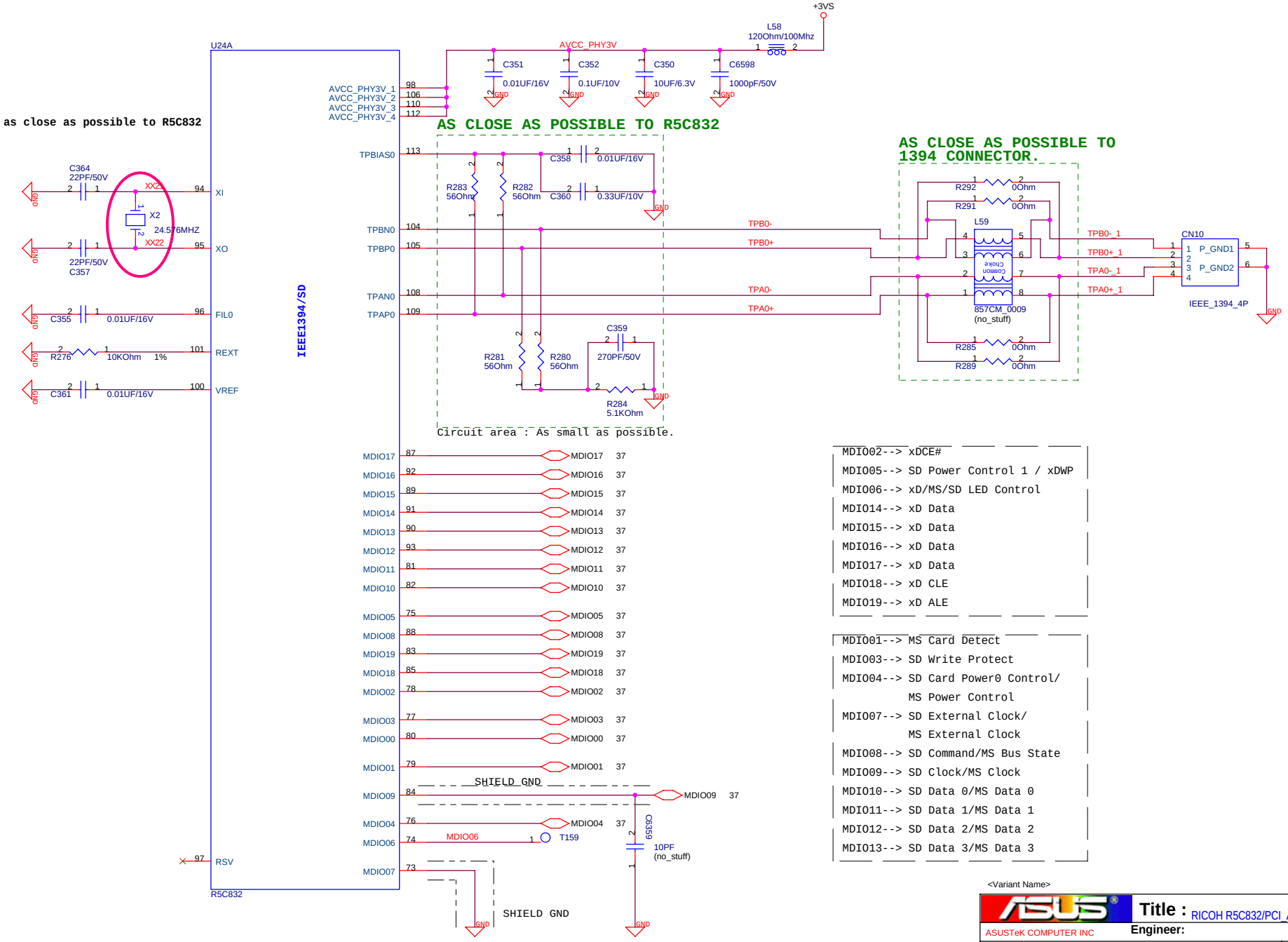
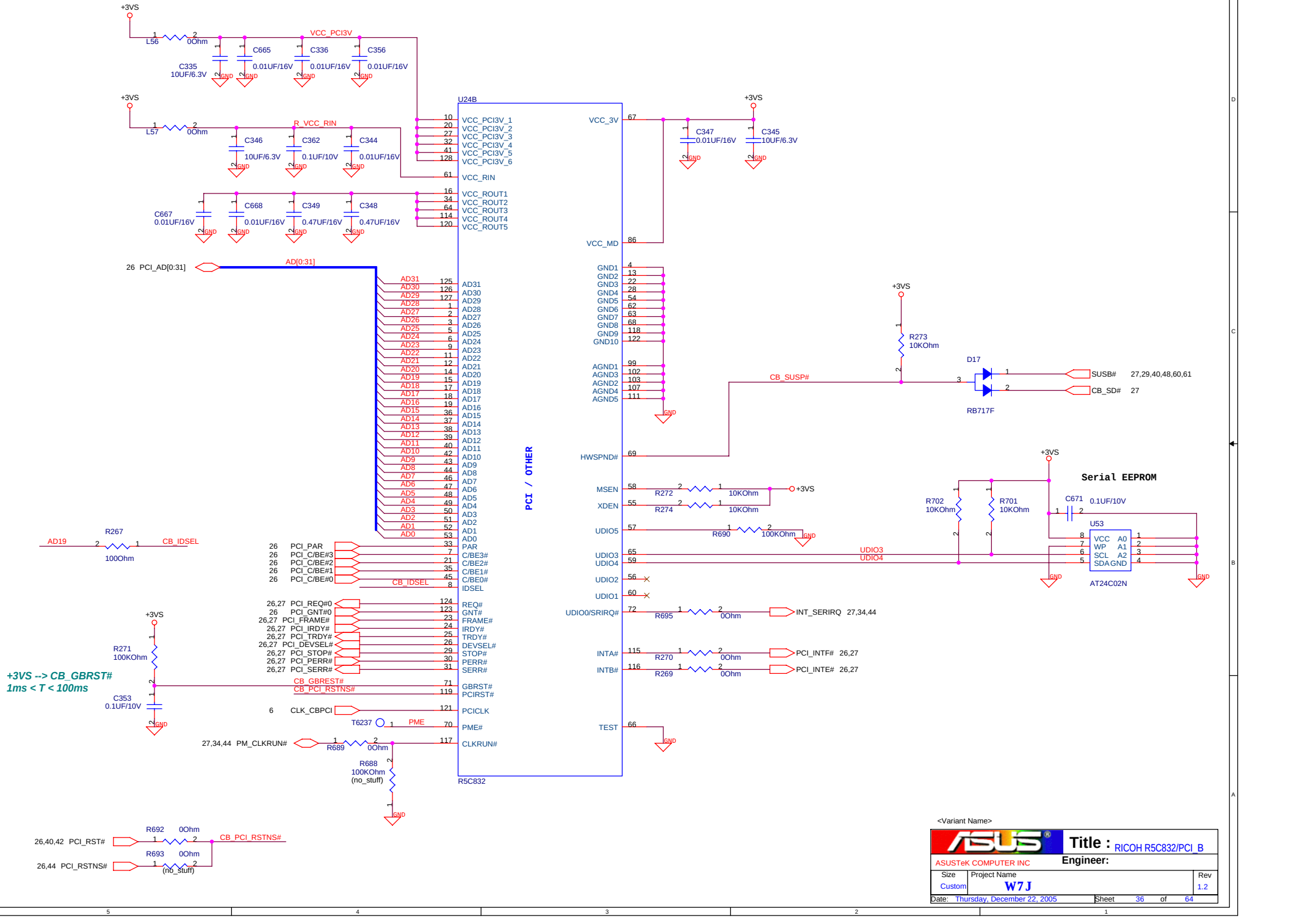

as close as possible to R5C832
U24A
IEEE1394/SD
R5C832
C364
22PF/50V
XX21
X2
24.576MHZ
XX22
22PF/50V
C357
C355
0.01UF/16V
R276
10KOhm
1%
C361
0.01UF/16V
XI
XO
FIL0
REXT
VREF
RSV
AVCC_PHY3V_1
AVCC_PHY3V_2
AVCC_PHY3V_3
AVCC_PHY3V_4
AVCC_PHY3V
+3VS
L58
120Ohm/100Mhz
C351
0.01UF/16V
C352
0.1UF/10V
C350
10UF/6.3V
C6598
1000pF/50V
AS CLOSE AS POSSIBLE TO R5C832
TPBIAS0
C358
0.01UF/16V
R283
56Ohm
R282
56Ohm
C360
0.33UF/10V
TPBN0
TPBP0
TPAN0
TPAP0
TPB0-
TPB0+
TPA0-
TPA0+
R281
56Ohm
R280
56Ohm
C359
270PF/50V
R284
5.1KOhm
Circuit area : As small as possible.
AS CLOSE AS POSSIBLE TO
1394 CONNECTOR.
R292
0Ohm
R291
0Ohm
L59
Common Choke
857CM_0009
(no_stuff)
R285
0Ohm
R289
0Ohm
TPB0-_1
TPB0+_1
TPA0-_1
TPA0+_1
CN10
P_GND1
P_GND2
IEEE_1394_4P
MDIO17
MDIO16
MDIO15
MDIO14
MDIO13
MDIO12
MDIO11
MDIO10
MDIO05
MDIO08
MDIO19
MDIO18
MDIO02
MDIO03
MDIO00
MDIO01
MDIO09
MDIO04
MDIO06
MDIO07
SHIELD GND
T159
C6359
10PF
(no_stuff)
SHIELD GND
MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO07--> SD External Clock/
MS External Clock
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3
<Variant Name>
Title : RICOH R5C832/PCI_A
ASUSTeK COMPUTER INC
Engineer:
Size
Custom
Project Name
W7 J
Rev
1.2
Date: Thursday, December 22, 2005
Sheet 35 of 64


+3VS
L56 0Ohm
VCC_PCI3V
C335 10UF/6.3V
C665 0.01UF/16V
C336 0.01UF/16V
C356 0.01UF/16V
L57 0Ohm
R_VCC_RIN
C346 10UF/6.3V
C362 0.1UF/10V
C344 0.01UF/16V
C667 0.01UF/16V
C668 0.01UF/16V
C349 0.47UF/16V
C348 0.47UF/16V
U24B
VCC_PCI3V_1
VCC_PCI3V_2
VCC_PCI3V_3
VCC_PCI3V_4
VCC_PCI3V_5
VCC_PCI3V_6
VCC_RIN
VCC_ROUT1
VCC_ROUT2
VCC_ROUT3
VCC_ROUT4
VCC_ROUT5
VCC_3V
VCC_MD
C347 0.01UF/16V
C345 10UF/6.3V
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
AGND1
AGND3
AGND2
AGND4
AGND5
26 PCI_AD[0:31]
AD[0:31]
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
PAR
C/BE3#
C/BE2#
C/BE1#
C/BE0#
IDSEL
PCI / OTHER
R273 10KOhm
D17
RB717F
SUSB# 27,29,40,48,60,61
CB_SD# 27
CB_SUSP#
HWSPND#
MSEN
XDEN
UDIO5
UDIO3
UDIO4
UDIO2
UDIO1
UDIO0/SRIRQ#
INTA#
INTB#
TEST
R272 10KOhm
R274 10KOhm
R690 100KOhm
R695 0Ohm
INT_SERIRQ 27,34,44
R270 0Ohm
PCI_INTF# 26,27
R269 0Ohm
PCI_INTE# 26,27
Serial EEPROM
R702 10KOhm
R701 10KOhm
C671 0.1UF/10V
U53
VCC
WP
SCL
SDA
A0
A1
A2
GND
AT24C02N
R267 100Ohm
AD19
CB_IDSEL
26 PCI_PAR
26 PCI_C/BE#3
26 PCI_C/BE#2
26 PCI_C/BE#1
26 PCI_C/BE#0
CB_IDSEL
26,27 PCI_REQ#0
26 PCI_GNT#0
26,27 PCI_FRAME#
26,27 PCI_IRDY#
26,27 PCI_TRDY#
26,27 PCI_DEVSEL#
26,27 PCI_STOP#
26,27 PCI_PERR#
26,27 PCI_SERR#
REQ#
GNT#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PERR#
SERR#
R271 100KOhm
+3VS --> CB_GBRST#
1ms < T < 100ms
C353 0.1UF/10V
CB_GBREST#
CB_PCI_RSTNS#
GBRST#
PCIRST#
6 CLK_CBPCI
PCICLK
T6237
PME
PME#
27,34,44 PM_CLKRUN#
R689 0Ohm
CLKRUN#
R688 100KOhm (no_stuff)
R5C832
R692 0Ohm
26,40,42 PCI_RST#
CB_PCI_RSTNS#
R693 0Ohm
26,44 PCI_RSTNS#
(no_stuff)
<Variant Name>
Title : RICOH R5C832/PCI_B
ASUSTeK COMPUTER INC
Engineer:
Size Custom
Project Name W7J
Rev 1.2
Date: Thursday, December 22, 2005
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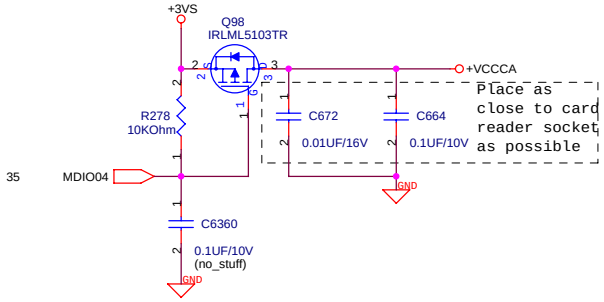
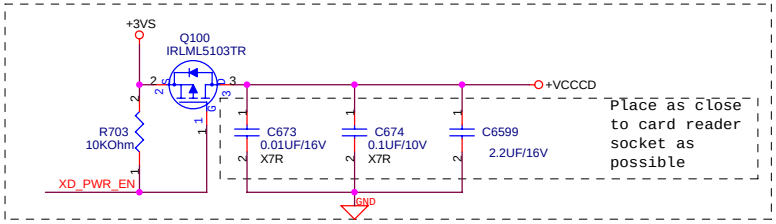
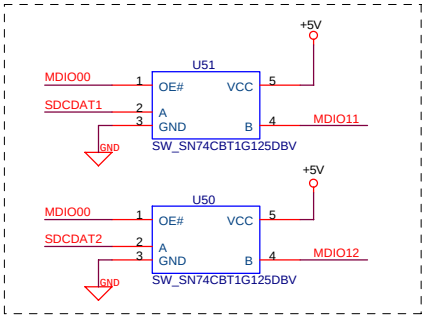


To correct the problem when MS Duo adaptor is in use.

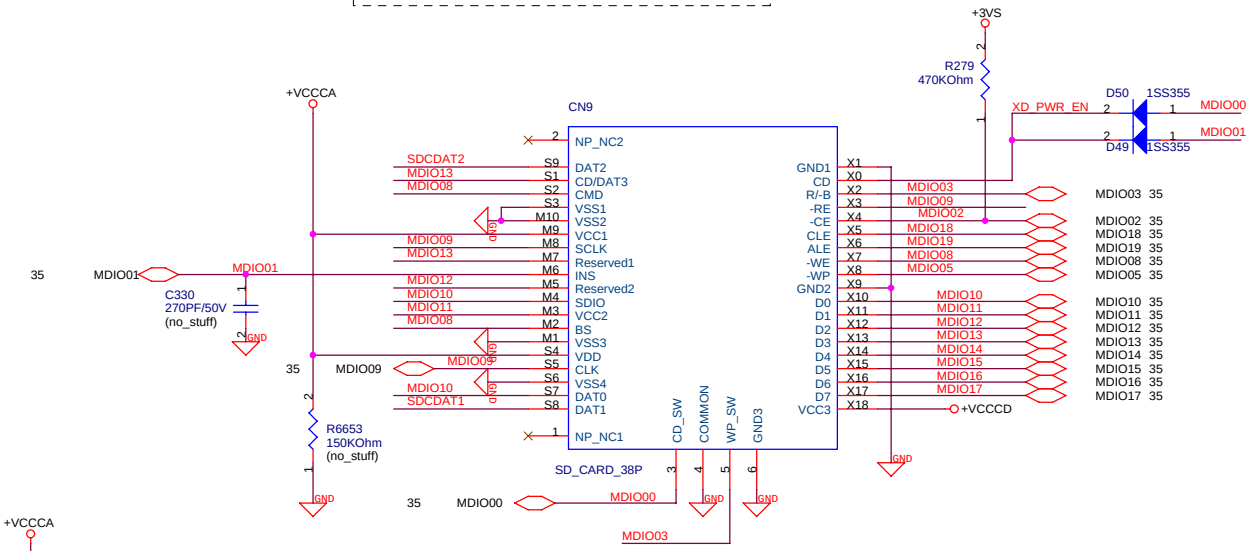


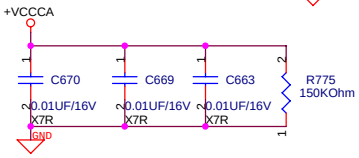
SD/MMC/MS/MS-PRO Card Reader Socket



MDIO00--> SD Card Detect
MDIO01--> MS Card Detect
MDIO03--> SD Write Protect
MDIO04--> SD Card Power0 Control/
MS Power Control
MDIO08--> SD Command/MS Bus State
MDIO09--> SD Clock/MS Clock
MDIO10--> SD Data 0/MS Data 0
MDIO11--> SD Data 1/MS Data 1
MDIO12--> SD Data 2/MS Data 2
MDIO13--> SD Data 3/MS Data 3

MDIO02--> xDCE#
MDIO05--> SD Power Control 1 / xDWP
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data
MDIO15--> xD Data
MDIO16--> xD Data
MDIO17--> xD Data
MDIO18--> xD CLE
MDIO19--> xD ALE

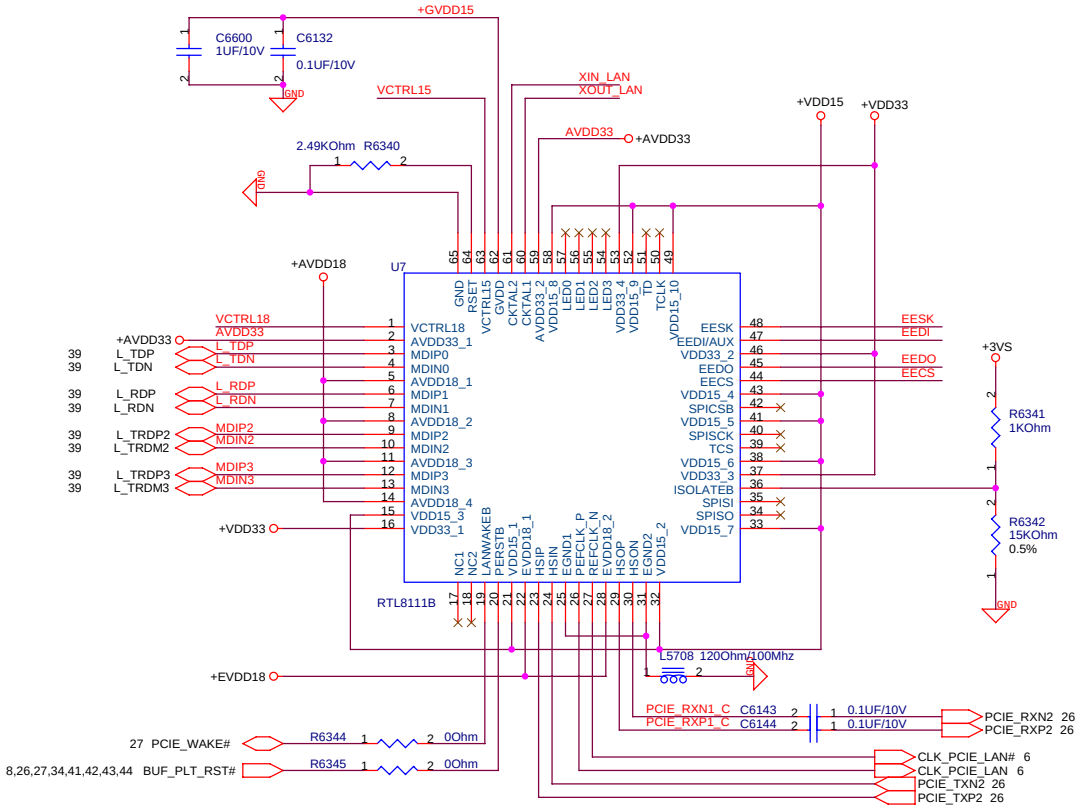


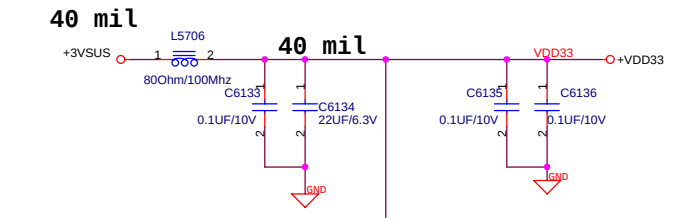


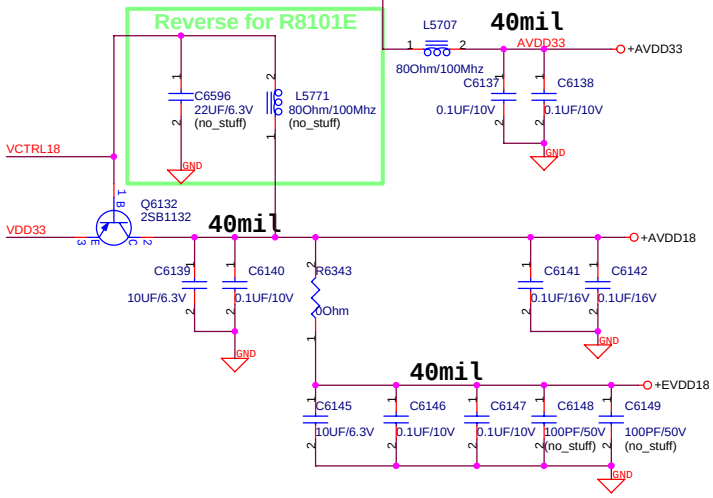
<Variant Name>

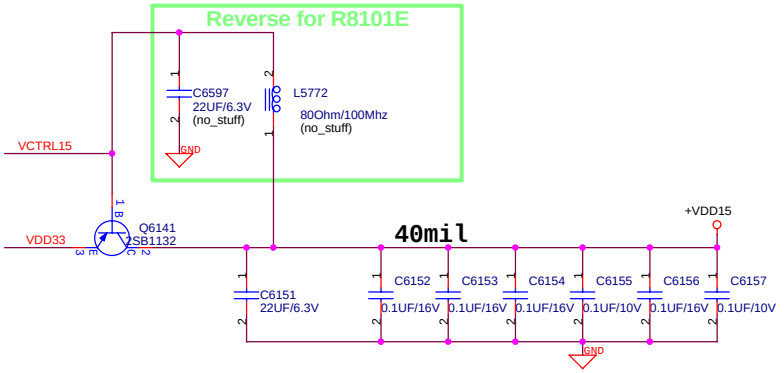
ASUSTeK COMPUTER INC	Title : CardReader	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 37 of 64	

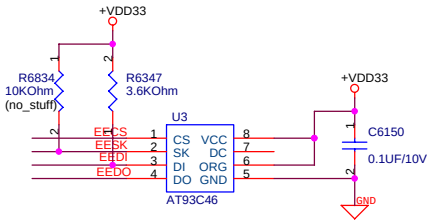
Average supply current
VDD33 103mA
AVDD18+EVDD18 198mA
VDD15 367mA

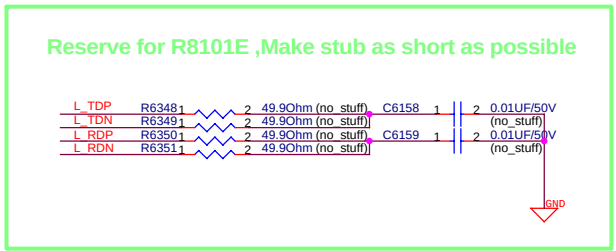


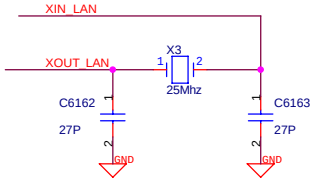


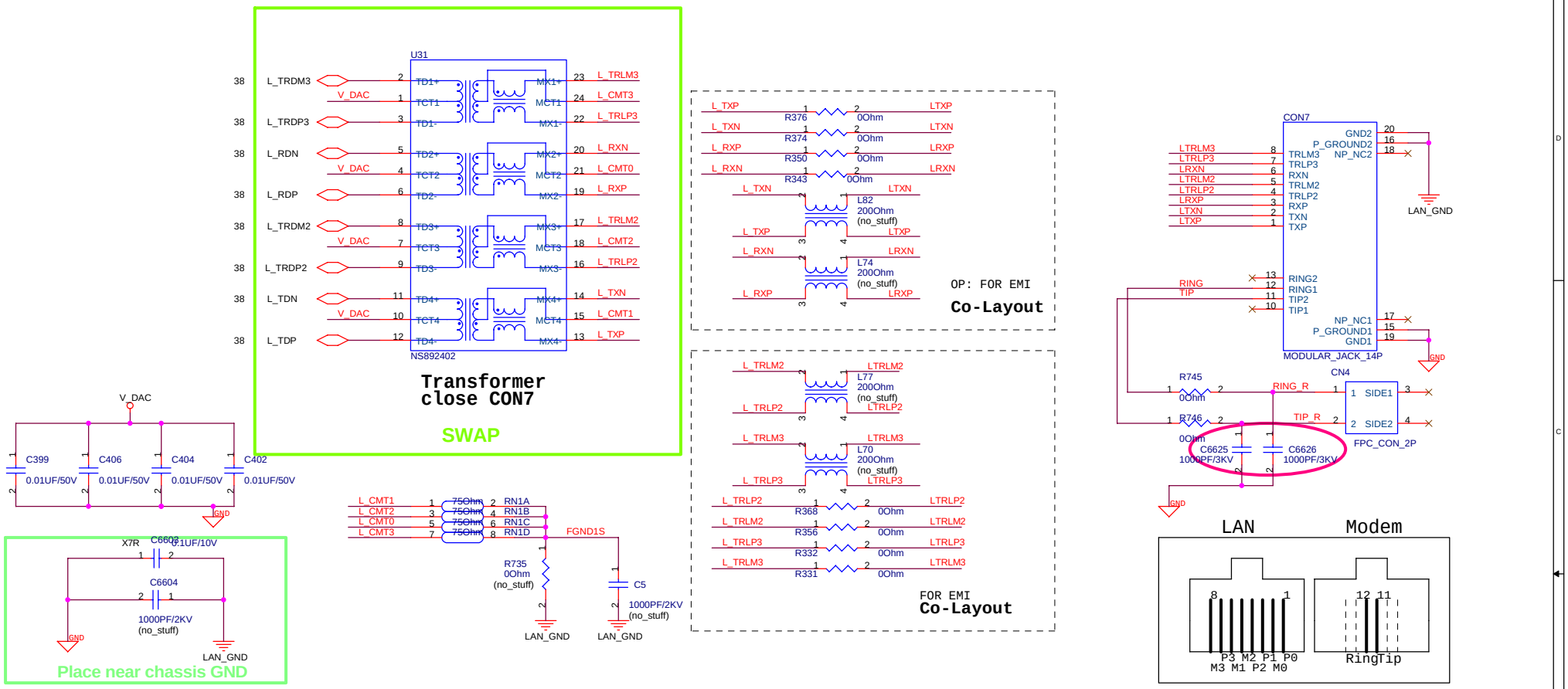




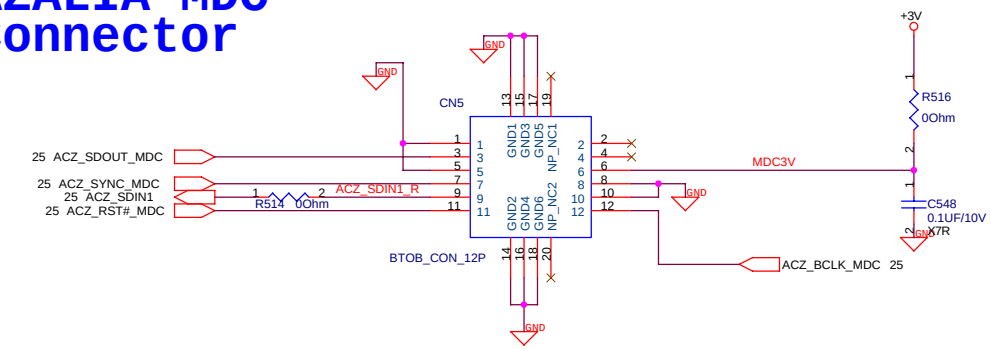






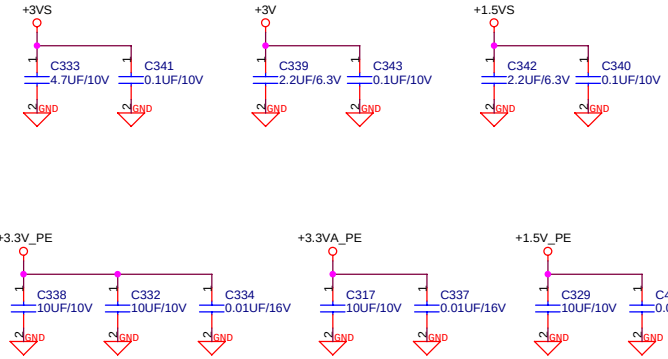


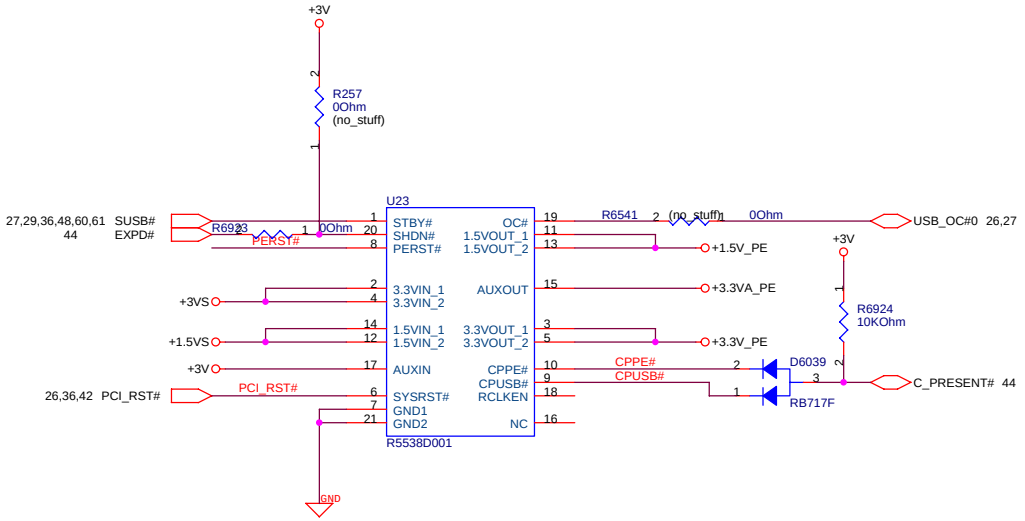
AZALIA MDC Connector

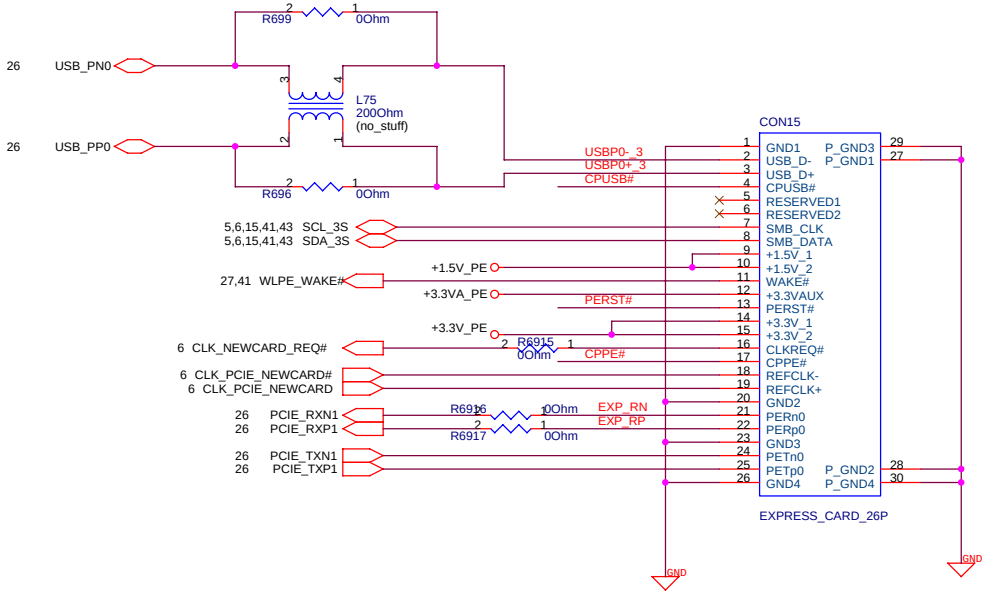


<Variant Name>

ASUSTeK COMPUTER INC	Title : RJ11+45 , MDC	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 39 of 64	

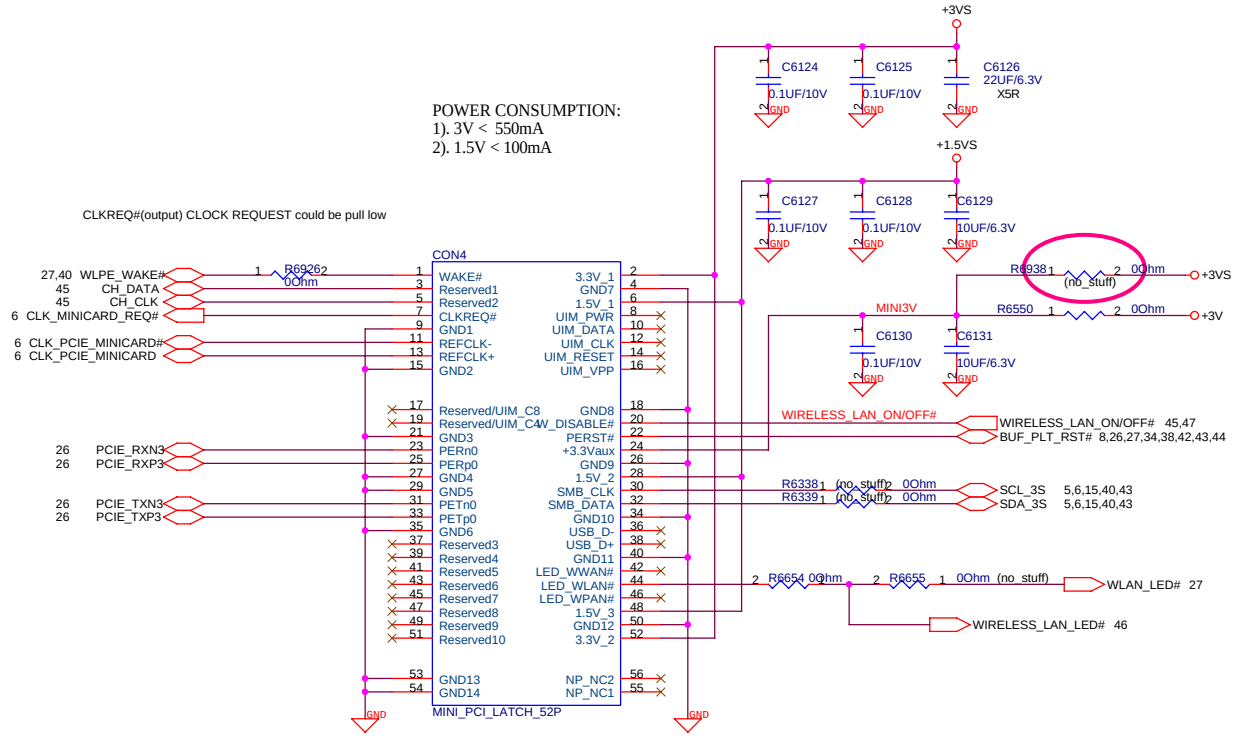




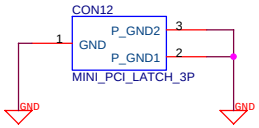


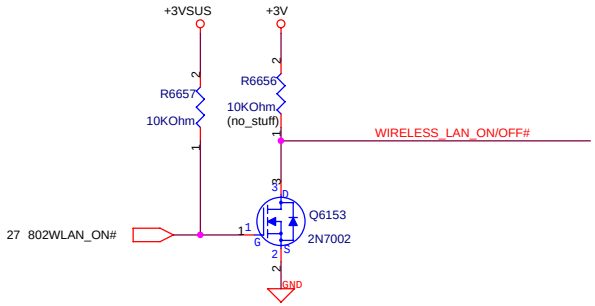
<variant_name>

ASUSTeK COMPUTER INC	Title : Express Card	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 40 of 64	



Mini Card Latch





<Variant Name>

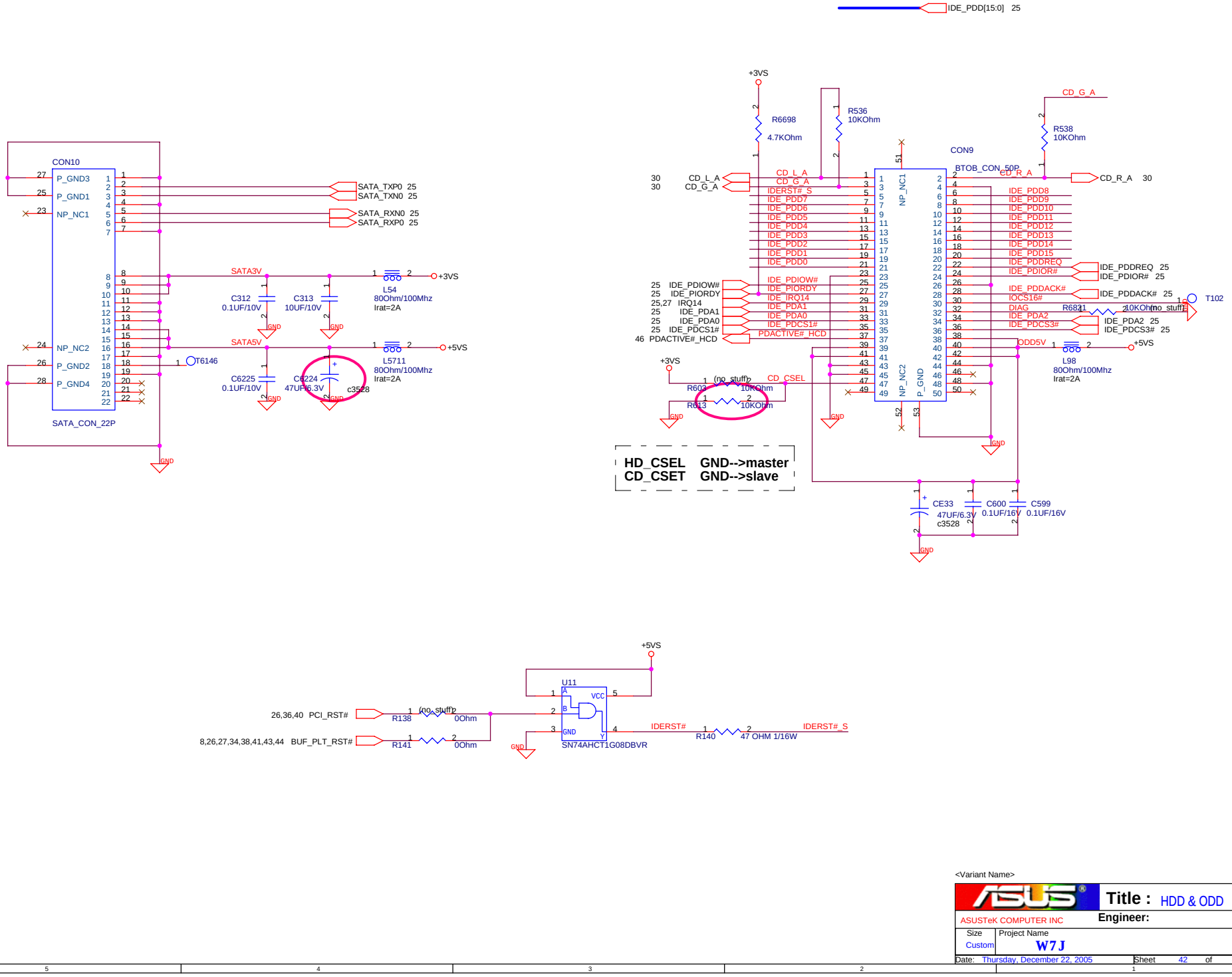
Title : MINICARD (802.11)

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 41 of 64



<Variant Name>

Title : HDD & ODD

ASUSTeK COMPUTER INC

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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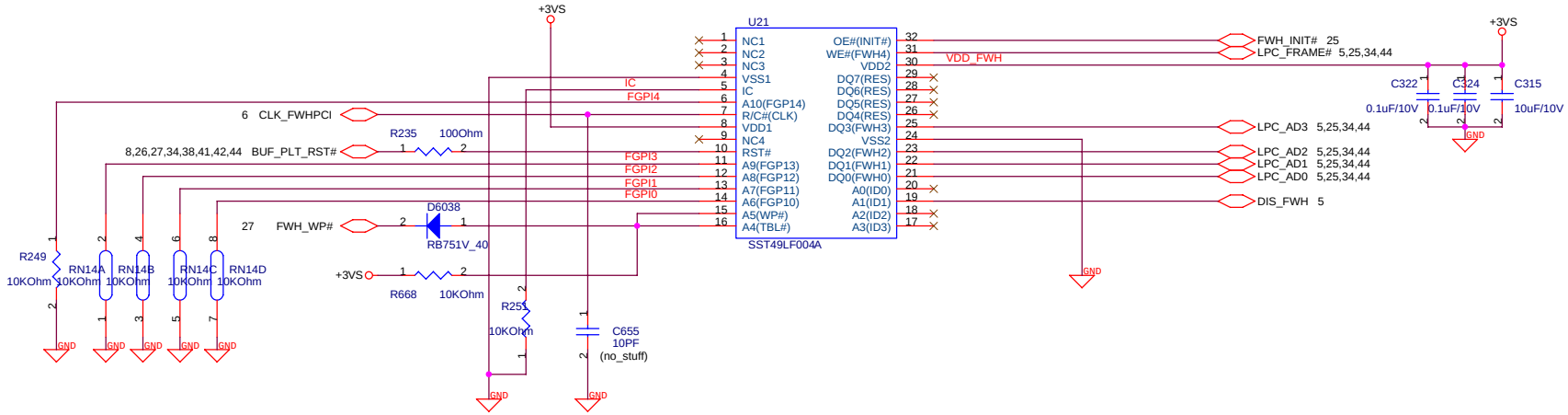

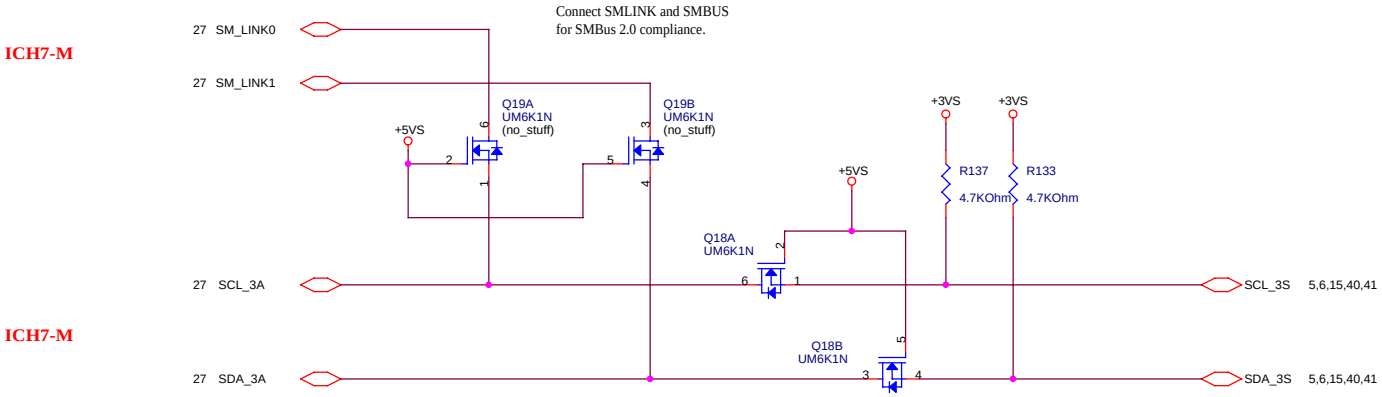

Termal Sensor,
Clock Generator
DDR2 SO-DIMM
EXPRESS CARD
MINI-CARD

<Variant Name>

ASUSTeK COMPUTER INC	Title : FWH , SM BUS	
	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 43 of 64	

KEYBOARD CNT

P2.1 Low : Power Button Override disable

Input Event only at P54, P55, P60 - P67

P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode

EC should set OP_SD low in S3, keep from leakage.

P54,P55,P43,P50 are wake-up event inputs when KBC in standby mode

KID1	KID0	Matrix
0	0	US
1	1	UK
0	1	JP

U46

M38857

80mA

<Variant Name>

ASUSTeK COMPUTER INC

Title : KBC M38857

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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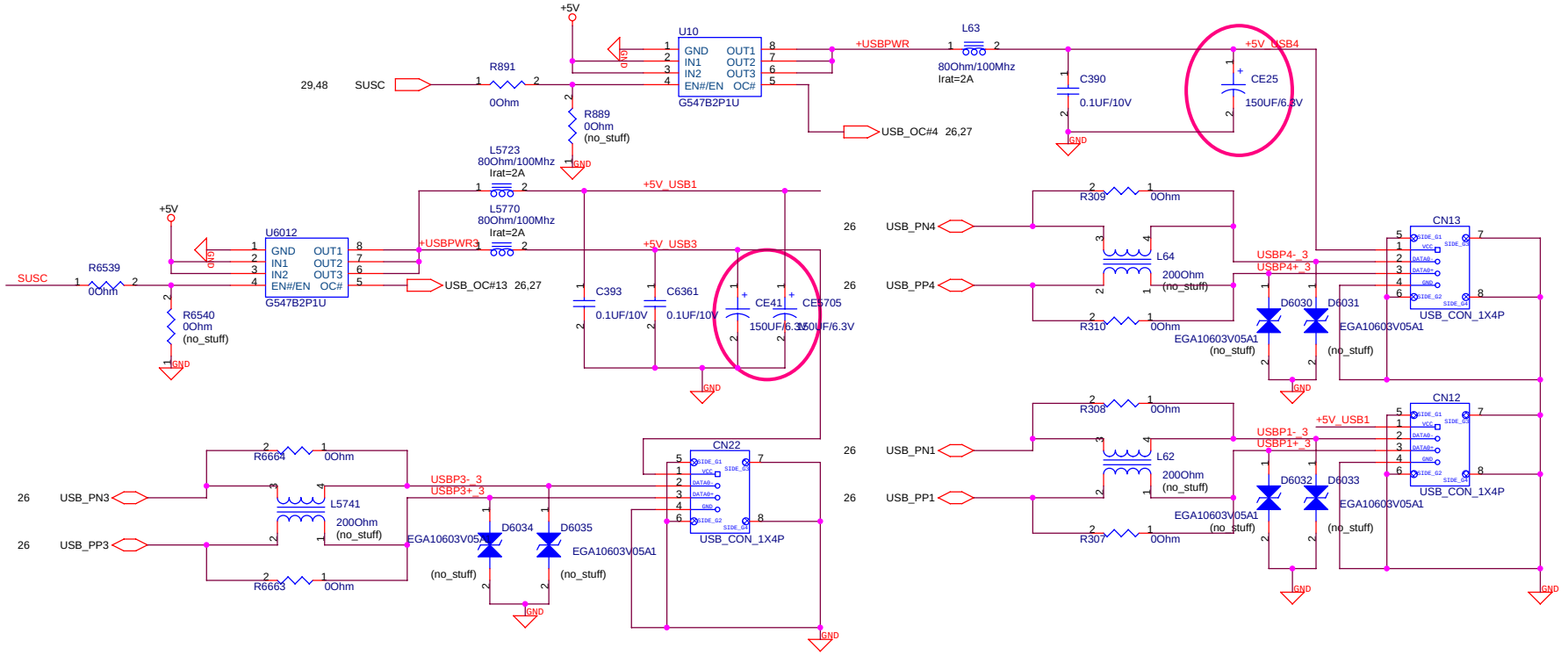
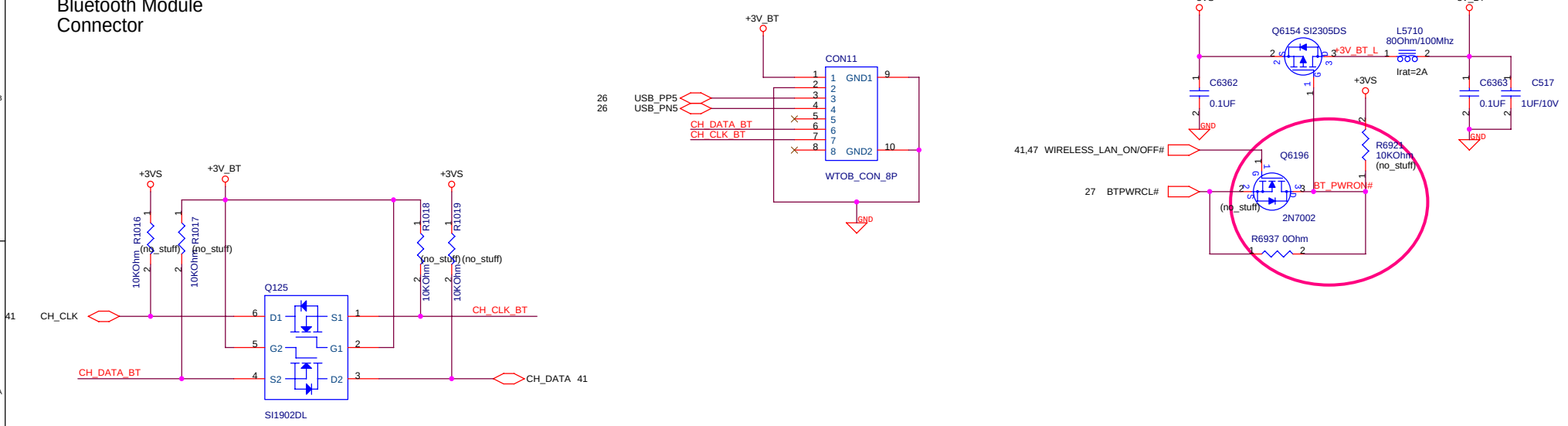


Bluetooth Module Connector



<Variant Name>

ASUSTeK COMPUTER INC

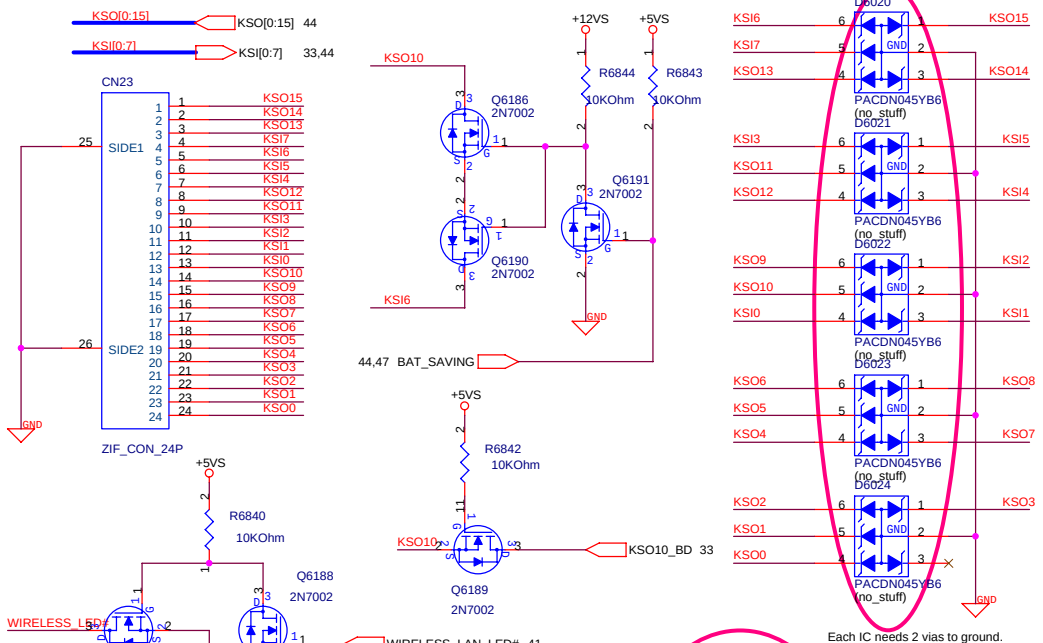
Title : USB * 3ports & BT

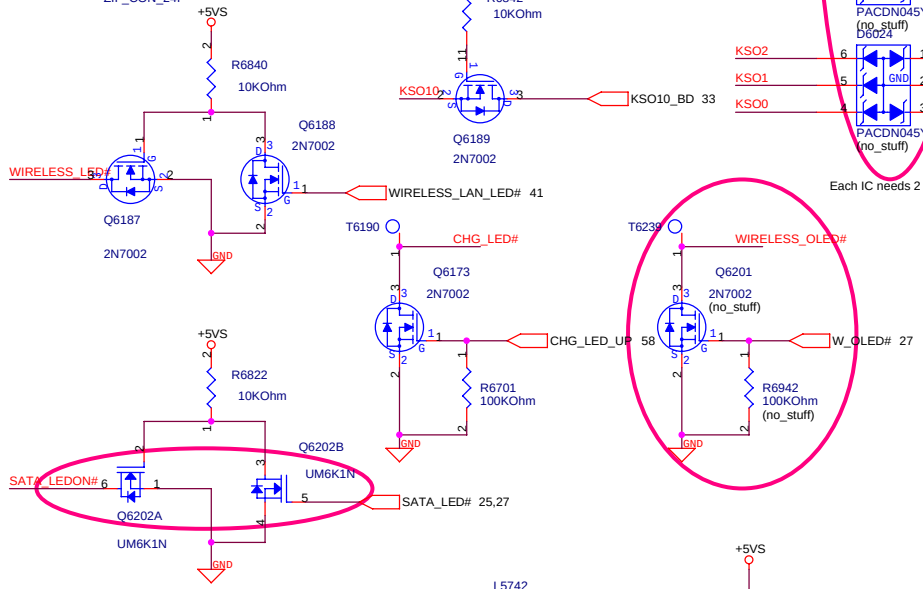
Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

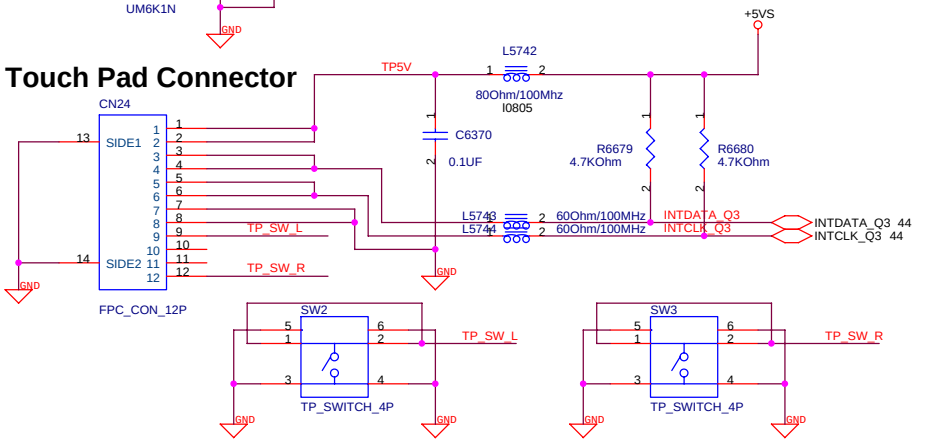
Date: Thursday, December 22, 2005 Sheet 45 of 64

Internal Keyboard Connector

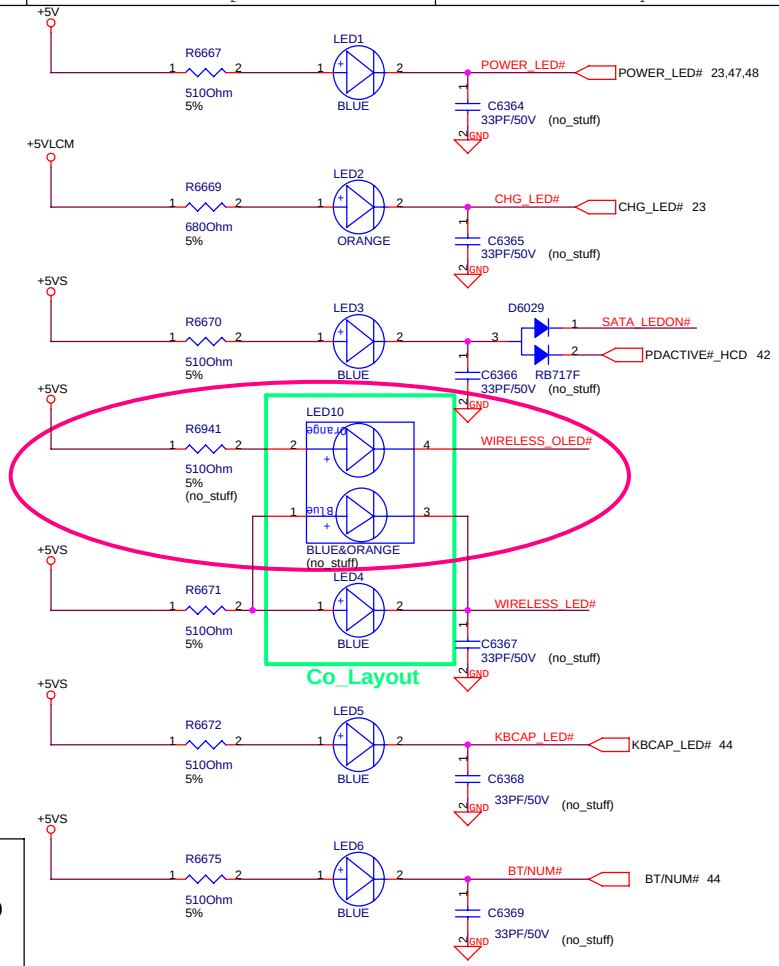




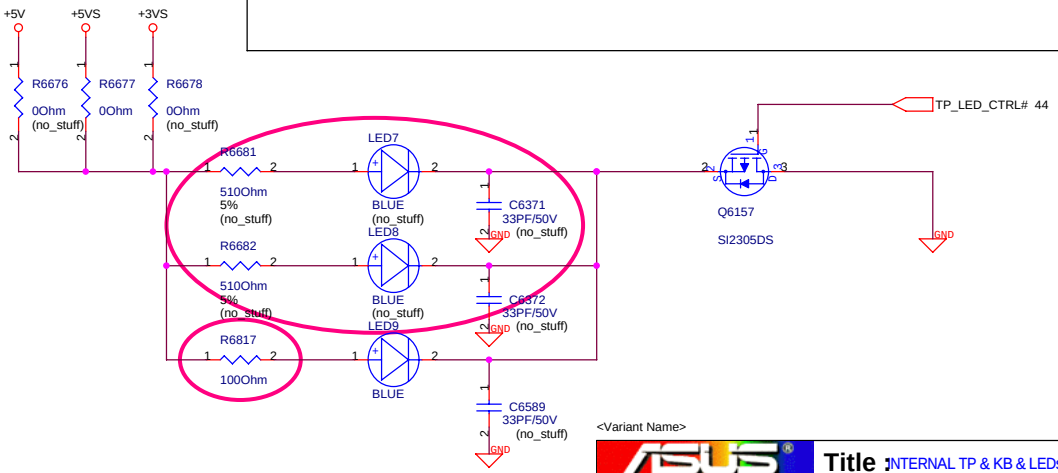
Touch Pad Connector



LEDs



Touch Pad LED



<Variant Name>

ASUSTeK COMPUTER INC

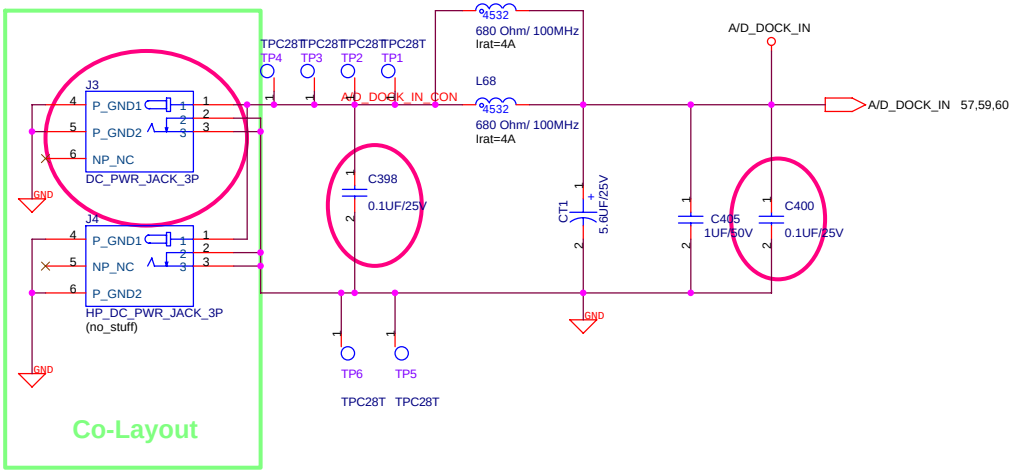
Title : INTERNAL TP & KB & LEDs

Engineer:

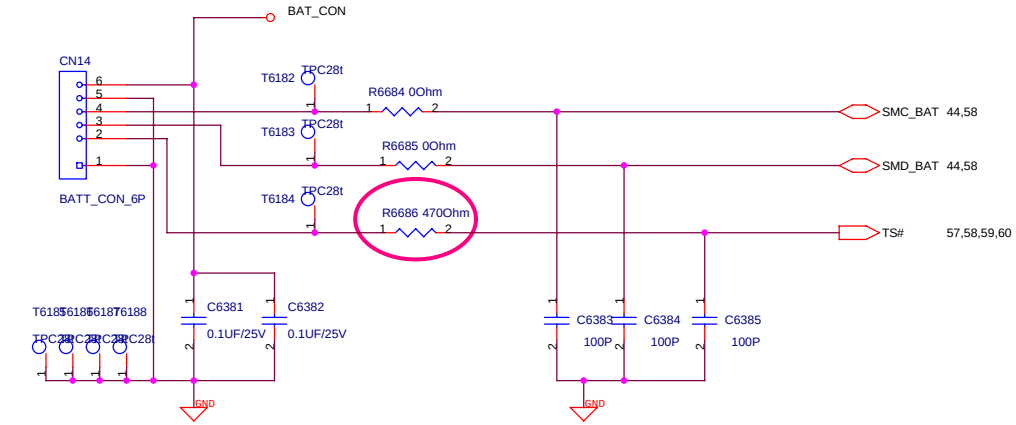
Size	Project Name	Rev
Custom	W7J	1.2

Date: Thursday, December 22, 2005 Sheet 46 of 64

DC-IN

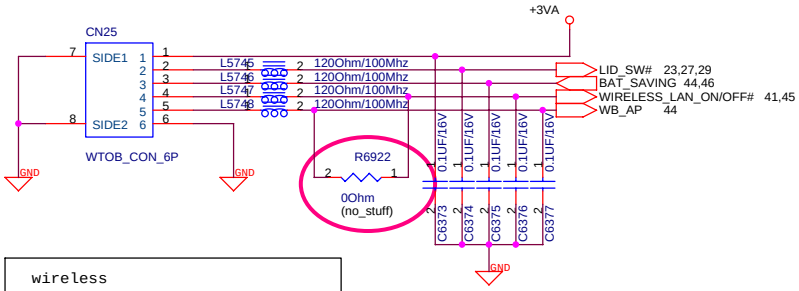


Battery Connector



EXT BOARD

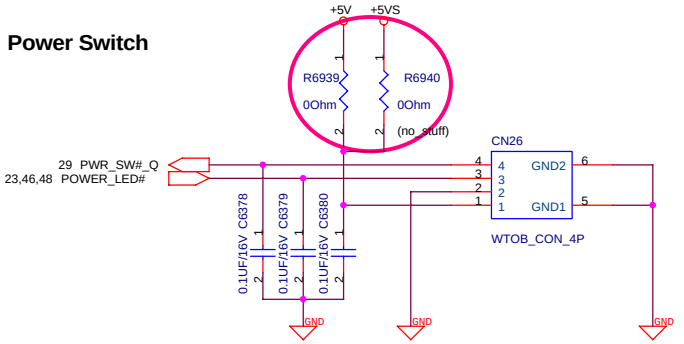
LID_SW_BD CN



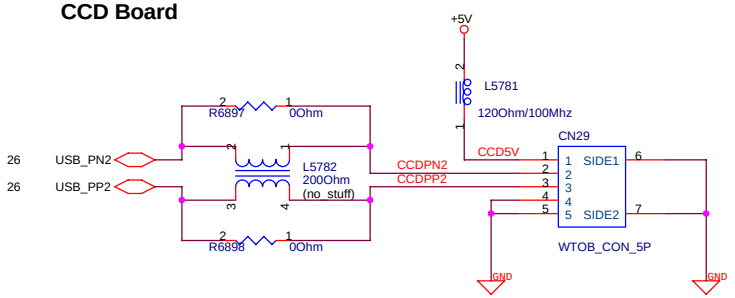

```
wireless
-----------------------------
right on ---> active high
left off ---> active low

WB_AP
-----------------------------
right off ---> active high
left  on  ---> active low
```

Power Switch



CCD Board



<Variant Name>

ASUSTeK COMPUTER INC

Title : DC IN,BATT CON,EXT BOARD

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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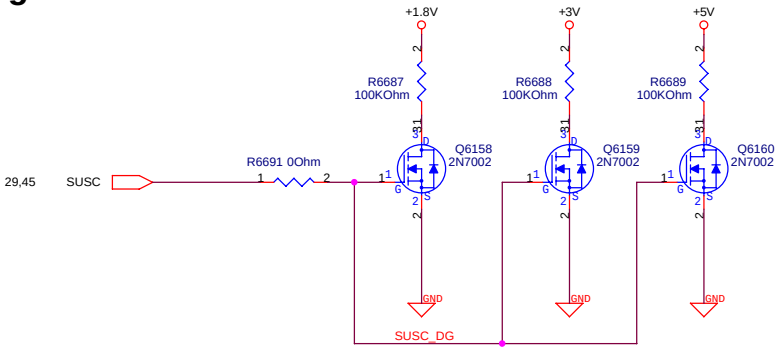
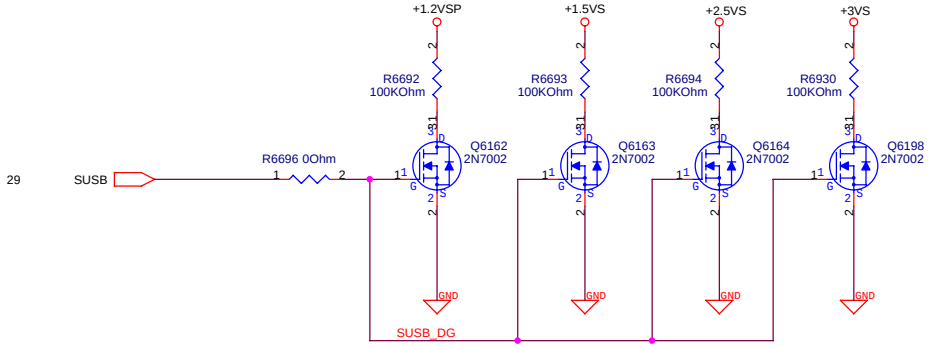
Discharge



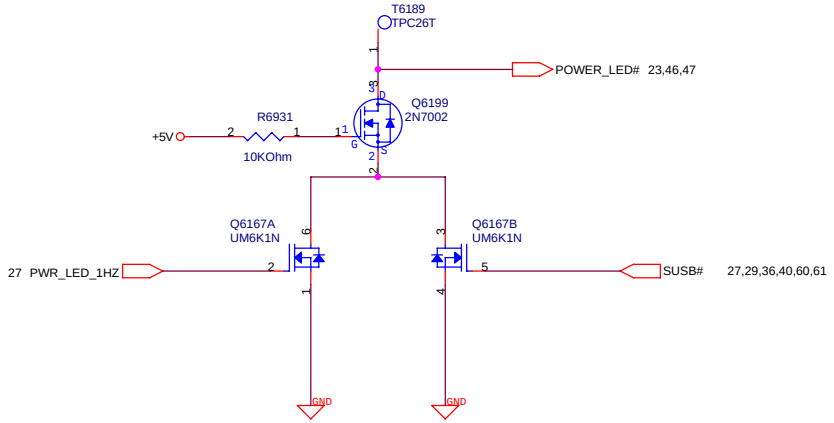


Poewr List

+3VA	+3VA	25,29,47,54,63
+3VSUS	+3VSUS	26,27,28,29,32,38,41,51
+5VA	+5VA	51,54,60
+5VSUS	+5VSUS	28,51,60
+3V	+3V	26,29,39,40,41,44,54,61
+5V	+5V	16,30,32,37,44,45,46,47,59,61
+12V	+12V	27,32,33,61
+3VS	+3VS	5,6,8,10,12,15,17,20,21,23,24,27,28,29,30,34,35,36,37,38,40,41,42,43,44,45,46,50,52,60,61
+5VS	+5VS	5,24,28,29,30,32,33,42,43,44,46,47,50,61
+12VS	+12VS	5,24,34,46,61
+VCORE	+VCORE	3,4,5,44,50
+VCCP	+VCCP	2,3,4,6,7,8,10,11,12,25,28,52
+1.2VSP	+1.2VSP	17,18,56
+2.5VS	+2.5VS	10,20,21,54
+1.8VS	+1.8VS	20,61
+0.9VS	+0.9VS	16,53
+1.5VS	+1.5VS	3,8,10,11,26,28,40,41,52
+VCC_RTC	+VCC_RTC	25,28
+1.8V	+1.8V	8,12,13,14,15,16,53
VTT_REF	VTT_REF	8,13,14,15,16
A/D_DOCK_IN	A/D_DOCK_IN	47,57,59,60
+VGA_VCORE	+VGA_VCORE	17,55

GND

Power LED On



<Variant Name>

Discharge,Power Rail & Power LED On

ASUSTeK COMPUTER INC

Title :

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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PCI Device	IDSEL#	REQ/GNT#	Interrupts
Chipset (Host to PCI)	AD30 (Internal)		
CARD READER	AD19	0	E
1394	AD19	0	F

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
Thermal Sensor	0101110x (2E)
PIC	1001001x (92)
Express Card	TBD
Mini Card	TBD

ICH7-M GPIO	W7J
GPIO 0	PM_BMBUSY#
GPIO 1	PCI_REQ#5
GPIO 2	PCI_INTE#
GPIO 3	PCI_INTF#
GPIO 4	PCI_INTG#
GPIO 5	PCI_INTH#
GPIO 6	BACK_OFF#
GPIO 7	MUTE_POP_ICHGPIO#
GPIO 8	EXTSMI#
GPIO 9	W_OLED#
GPIO 10	(PWRLMT#)
GPIO 11	SMBALERT#
GPIO 12	KBC_SCI#
GPIO 13	PWR_LED_1HZ
GPIO 14	WLAN_ON#
GPIO 15	802_LED_EN#
GPIO 16	DPRSLPVR
GPIO 17	GNT5#
GPIO 18	STP_PCI#
GPIO 19	Memoryclk
GPIO 20	STP_CPU#
GPIO 21	
GPIO 22	PCI_REQ#4
GPIO 23	LPC_DRQ#1
GPIO 24	SW_RST#
GPIO 25	CB_SD#
GPIO 26	MEM ID0
GPIO 27	MEM ID1
GPIO 28	MEM ID2
GPIO 29	USB_OC#5
GPIO 30	USB_OC#6
GPIO 31	USB_OC#7
GPIO 32	CLKRUN#
GPIO 33	BT_ON#
GPIO 34	FWH_WP#
GPIO 35	SATACLKREQ#
GPIO 36	BT_LED_EN#
GPIO 37	PCB_ID0
GPIO 38	PCB_ID1
GPIO 39	PCB_ID2
GPIO 48	GNT4#
GPIO 49	CPUPWRGD

KBC GPIO	W7J
P23	
P22	BAT_LEARN
P21	
P20	KBCRSM
P42	WATCHDOG
P43	
P44	xKBRC
P45	GA20
P46	KBDSCI
P47	CLKRUN#
P50	BAT_LLOW#
P51	TP_LED_CTRL#
P52	
P53	EXPD#
P54	LID_EC#
P55	BAT_IN#
P56	CPU_FAN_PWM
P57	ADJ_BL
P67	WB_AP
P66	M_MODE#
P65	
P64	ACIN#
P63	EOC#_LED
P62	C_PRESENT#
P61	ACZ_RST#_AUD
P60	
P75	KBDCLK_5S
P74	MOUSECLK_5S
P73	INTCLK_Q3
P72	KBDDATA_5S
P71	MOUSEDATA_5S
P70	INTDATA_Q3
P77	SMC_KBC
P76	SMD_KBC
P27	SCROLL_LED#
P26	NUM_LED#
P25	CAP_LED#
P24	SET_RSTNS#
P40	EXT_SMI#
P41	

<Variant Name>

Title : System Resource

ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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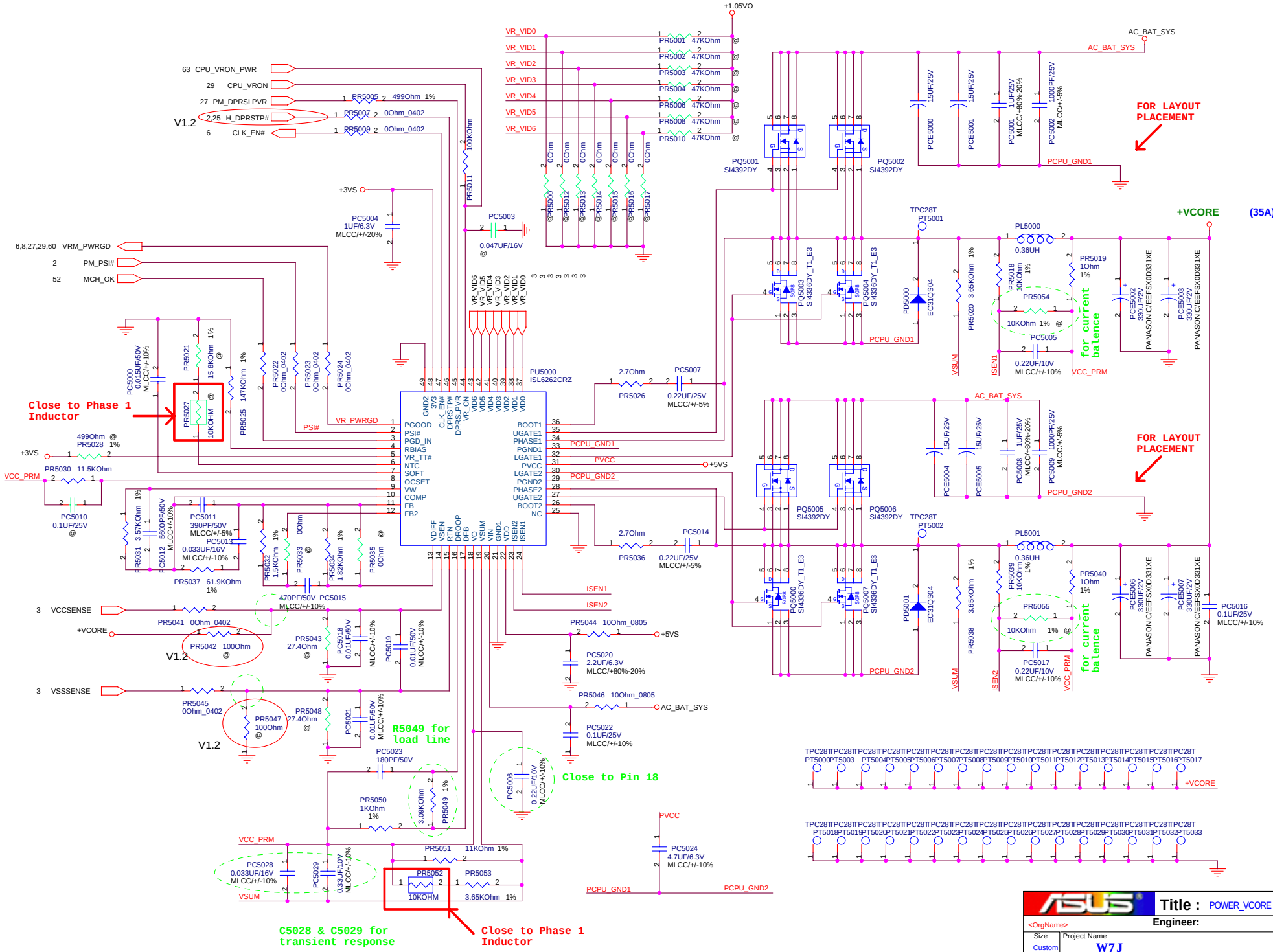
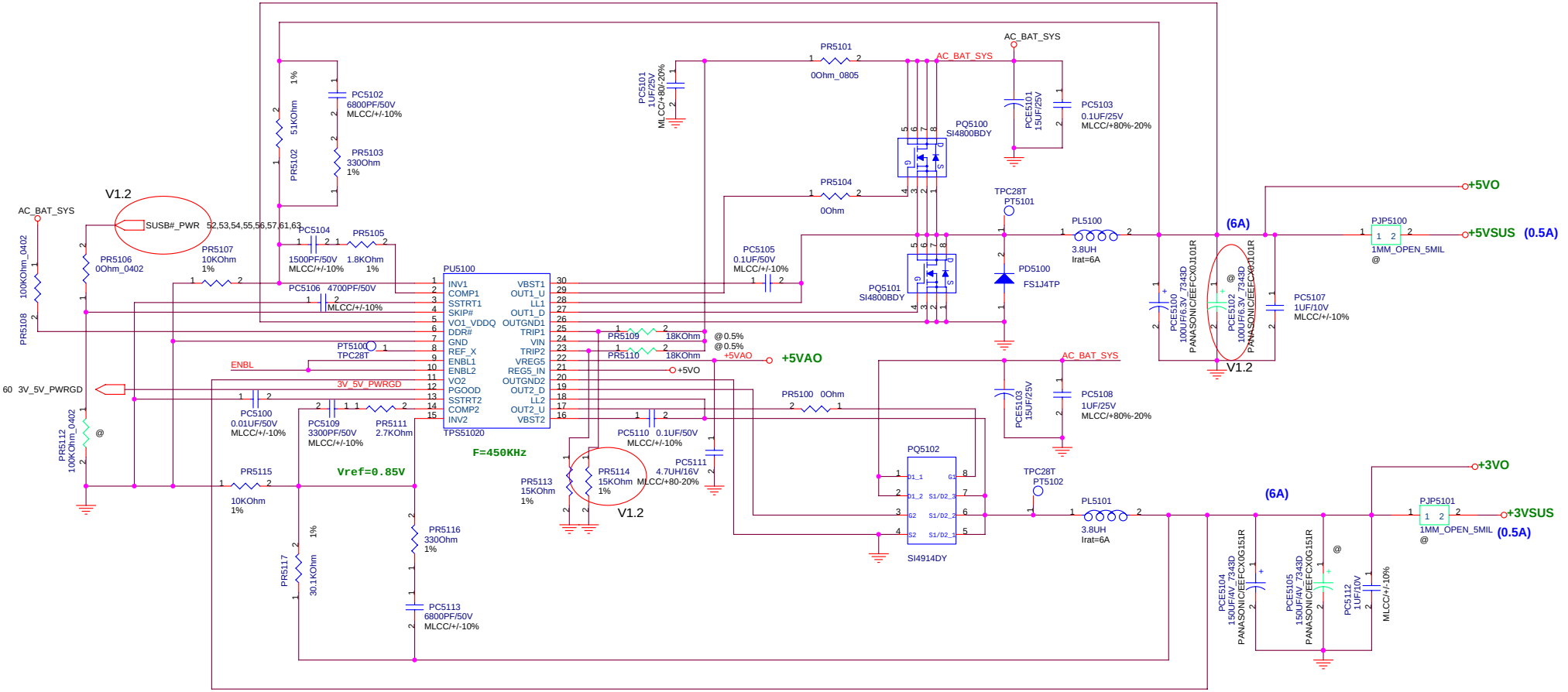
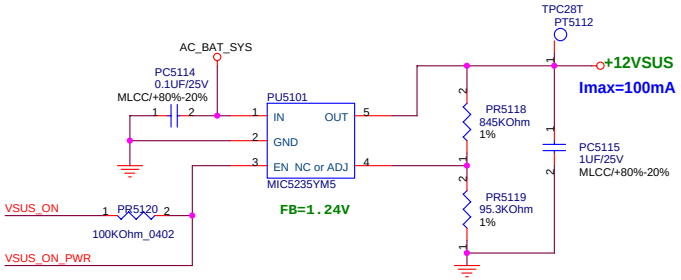
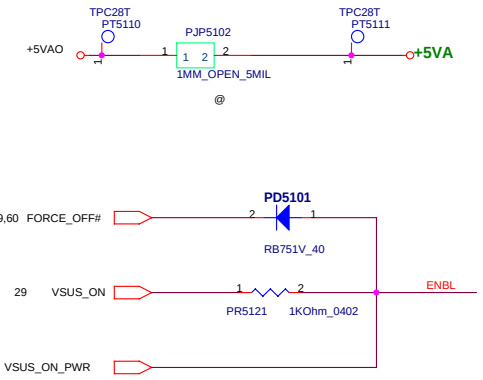


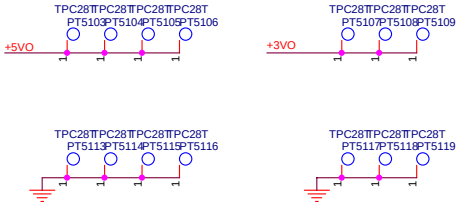
ASUS	Title : POWER_VCORE		
<OrgName>	Engineer:		
Size: Custom	Project Name: W7 J		Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 50 of 64		



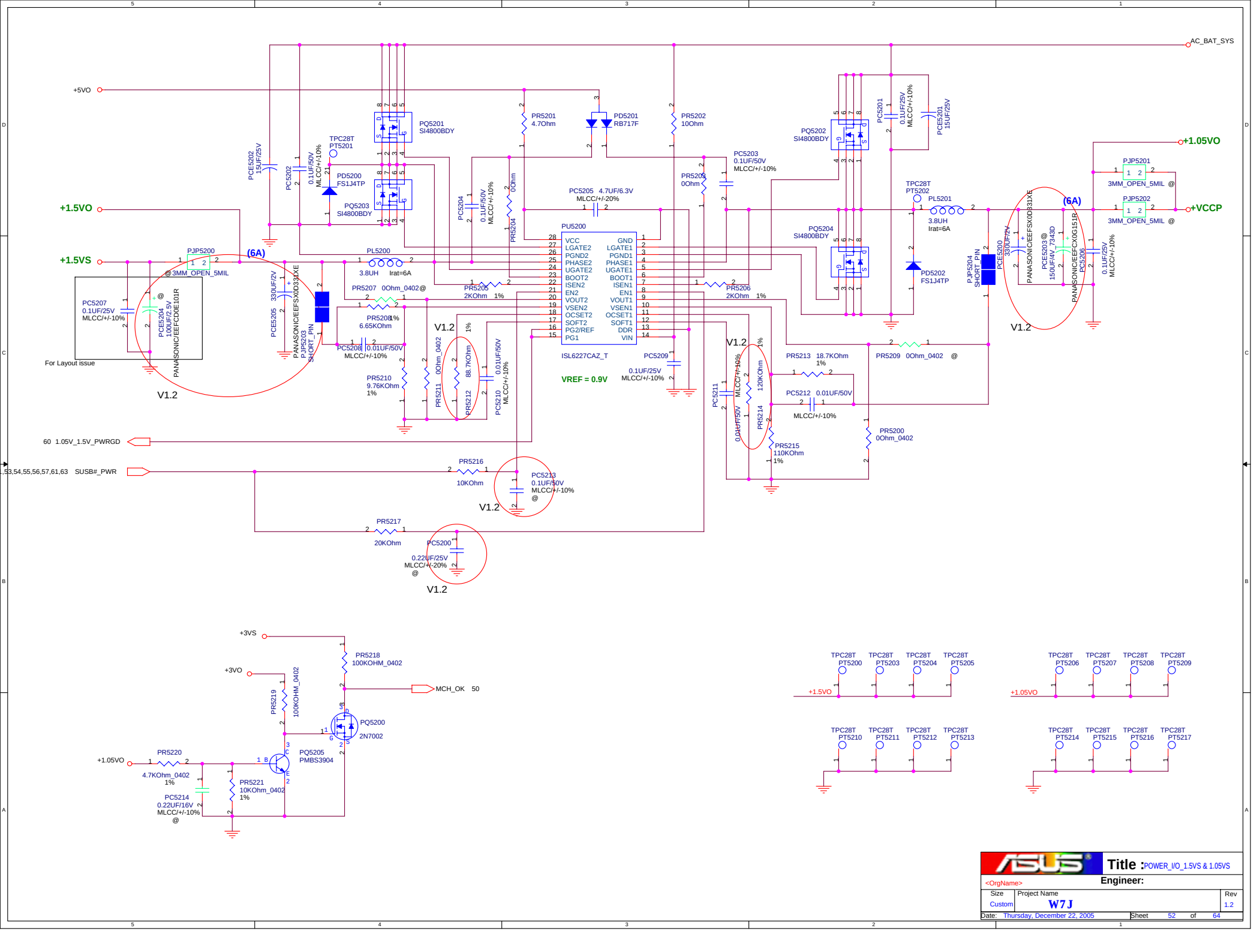
+12VSUS







ASUS	Title : POWER_SYSTEM	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 51 of 64	


AC_BAT_SYS
+5VO
+1.5VO
+1.5VS
+1.05VO
+VCCP
PU5200
ISL6227CAZ_T
VREF = 0.9V
PQ5201 SI4800BDY
PQ5202 SI4800BDY
PQ5203 SI4800BDY
PQ5204 SI4800BDY
PD5201 RB717F
PD5200 FS1J4TP
PD5202 FS1J4TP
PL5201 3.8UH Irat=6A
PL5200 3.8UH Irat=6A
PJP5200 @3MM_OPEN_5MIL
PJP5201 3MM_OPEN_5MIL @
PJP5202 3MM_OPEN_5MIL @
PJP5203 SHORT_PIN
PJP5204 SHORT PIN
PR5201 4.7Ohm
PR5202 10Ohm
PR5203 0Ohm
PR5204 0Ohm
PR5205 2KOhm 1%
PR5206 2KOhm 1%
PR5207 0Ohm_0402@
PR5208 6.65KOhm 1%
PR5209 0Ohm_0402 @
PR5210 9.76KOhm 1%
PR5211 0Ohm_0402
PR5212 88.7KOhm 1%
PR5213 18.7KOhm 1%
PR5214 120KOhm 1%
PR5215 110KOhm 1%
PR5216 10KOhm
PR5217 20KOhm
PR5218 100KOHM_0402
PR5219 100KOHM_0402
PR5220 4.7KOhm_0402 1%
PR5221 10KOhm_0402 1%
PR5200 0Ohm_0402
PC5201 15UF/25V
PCE5201 15UF/25V
PC5202 0.1UF/50V MLCC/+/-10%
PCE5202 15UF/25V
PC5203 0.1UF/50V MLCC/+/-10%
PC5204 0.1UF/50V MLCC/+/-10%
PC5205 4.7UF/6.3V MLCC/+/-20%
PC5207 0.1UF/25V MLCC/+/-10%
PCE5204 100UF/2.5V 1EEFCD0E101R
PCE5205 330UF/2V PANASONIC/EEFSX0D331XE
PC5208 0.01UF/50V MLCC/+/-10%
PC5209 0.1UF/25V MLCC/+/-10%
PC5210 0.01UF/50V MLCC/+/-10%
PC5211 0.01UF/50V MLCC/+/-10%
PC5212 0.01UF/50V MLCC/+/-10%
PC5213 0.1UF/50V MLCC/+/-10% @
PC5214 0.22UF/16V MLCC/+/-10% @
PC5200 0.22UF/25V MLCC/+/-20% @
PCE5200 330UF/2V PANASONIC/EEFSX0D331XE
PCE5203 @ 150UF/4V_7343D PANASONIC/EEFCX0G151R
PC5206 0.1UF/25V MLCC/+/-10%
TPC28T PT5201
TPC28T PT5202
For Layout issue
V1.2
(6A)
60 1.05V_1.5V_PWRGD
53,54,55,56,57,61,63 SUSB#_PWR
+3VS
+3VO
MCH_OK 50
PQ5200 2N7002
PQ5205 PMBS3904
TPC28T PT5200
TPC28T PT5203
TPC28T PT5204
TPC28T PT5205
TPC28T PT5206
TPC28T PT5207
TPC28T PT5208
TPC28T PT5209
TPC28T PT5210
TPC28T PT5211
TPC28T PT5212
TPC28T PT5213
TPC28T PT5214
TPC28T PT5215
TPC28T PT5216
TPC28T PT5217
Title : POWER_I/O_1.5VS & 1.05VS
<OrgName>
Engineer:
Size Custom
Project Name W7 J
Rev 1.2
Date: Thursday, December 22, 2005
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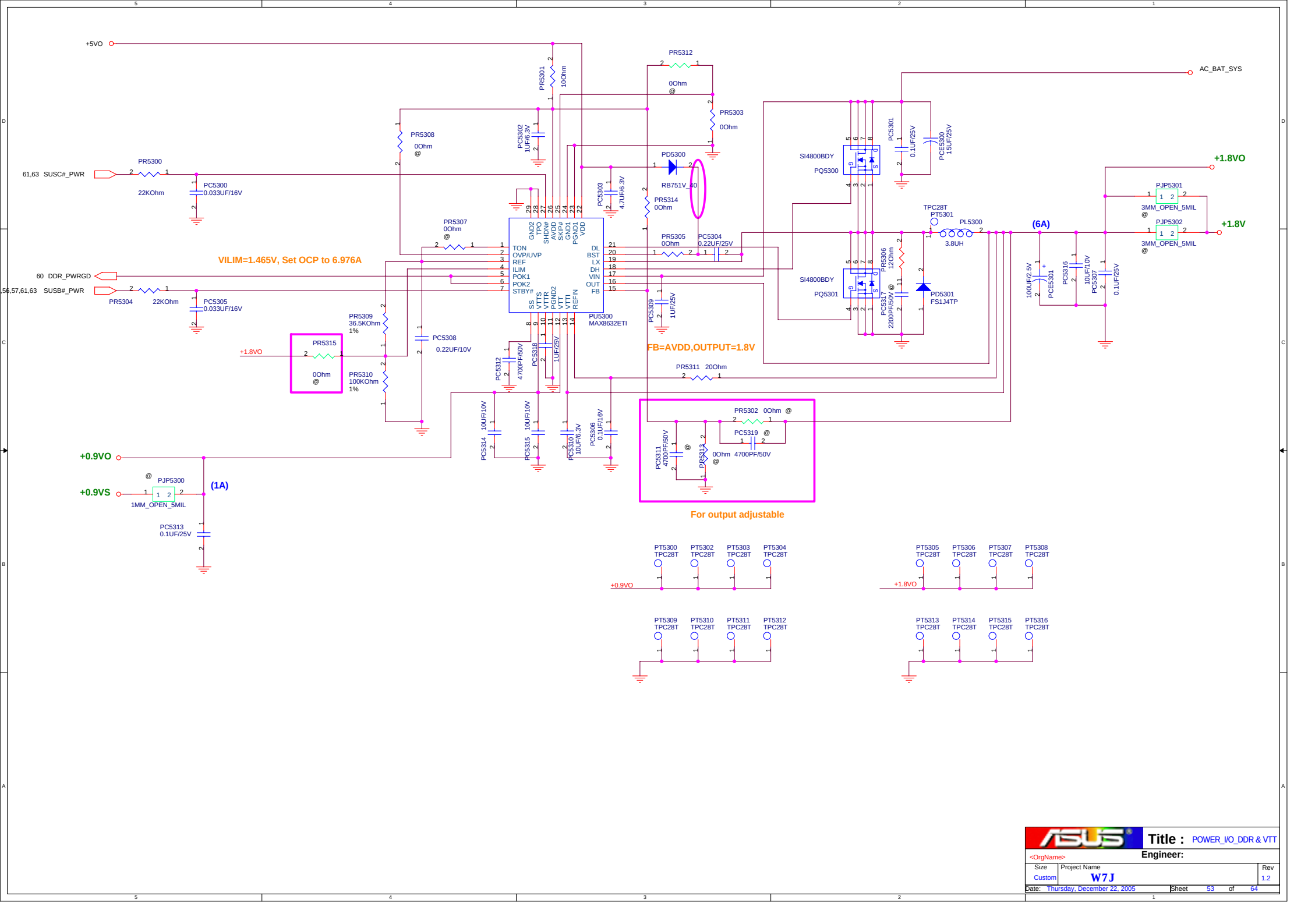
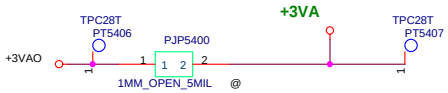
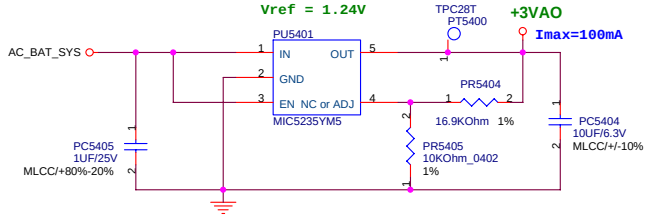


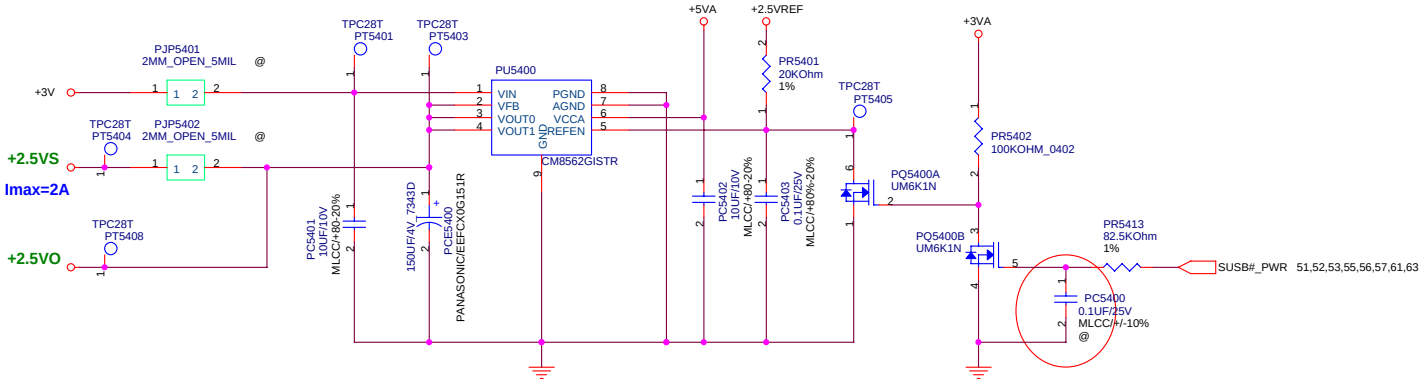
ASUS	Title : POWER_I/O_DDR & VTT	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 53 of 64	

+3VA0

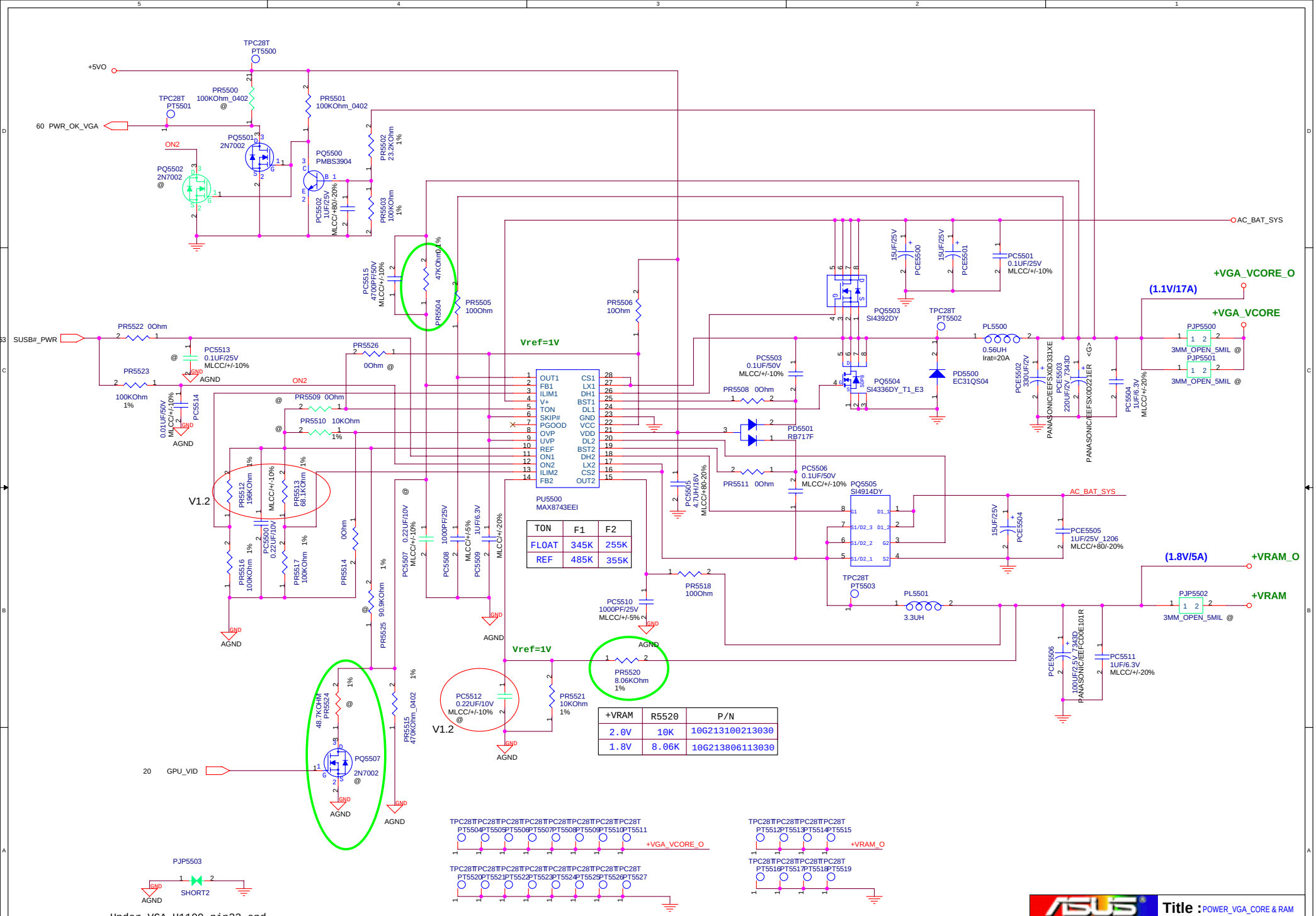




+2.5VS



ASUS	Title : POWER_I/O_+3VA & +2.5V	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 54 of 64	



TON	F1	F2
FLOAT	345K	255K
REF	485K	355K

+VRAM	R5520	P/N
2.0V	10K	10G213100213030
1.8V	8.06K	10G213806113030

Title : POWER_VGA_CORE & RAM

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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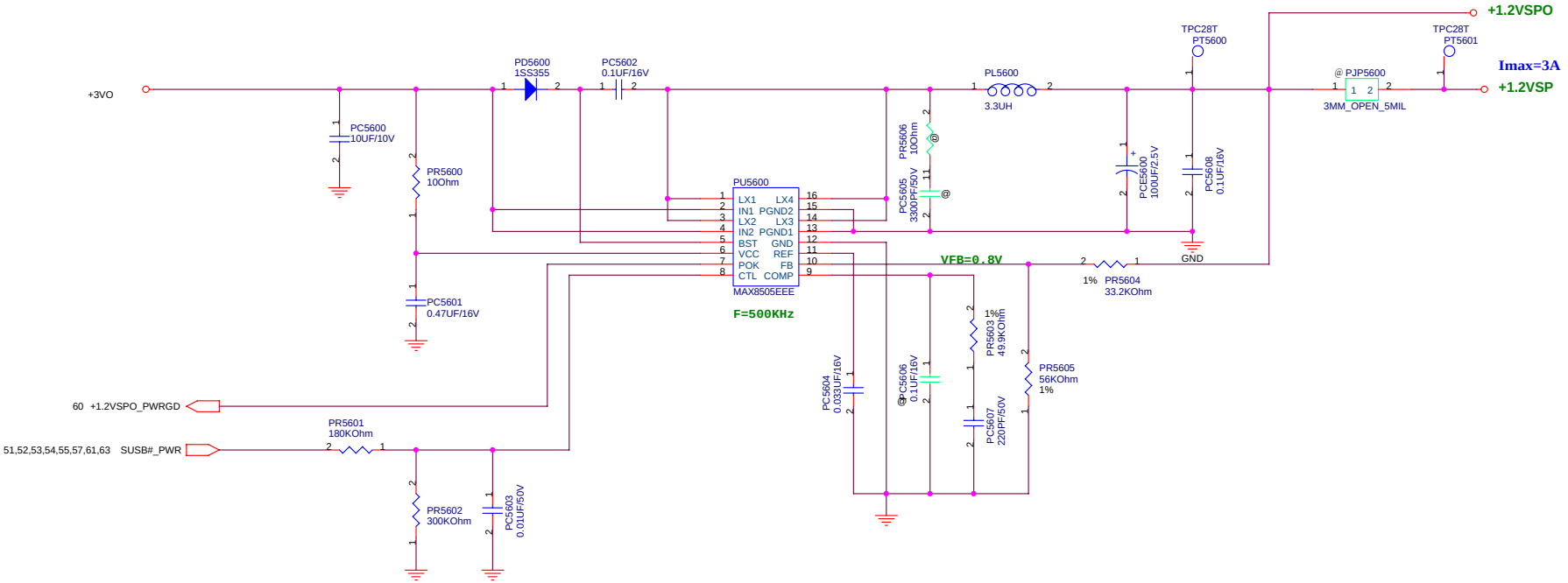
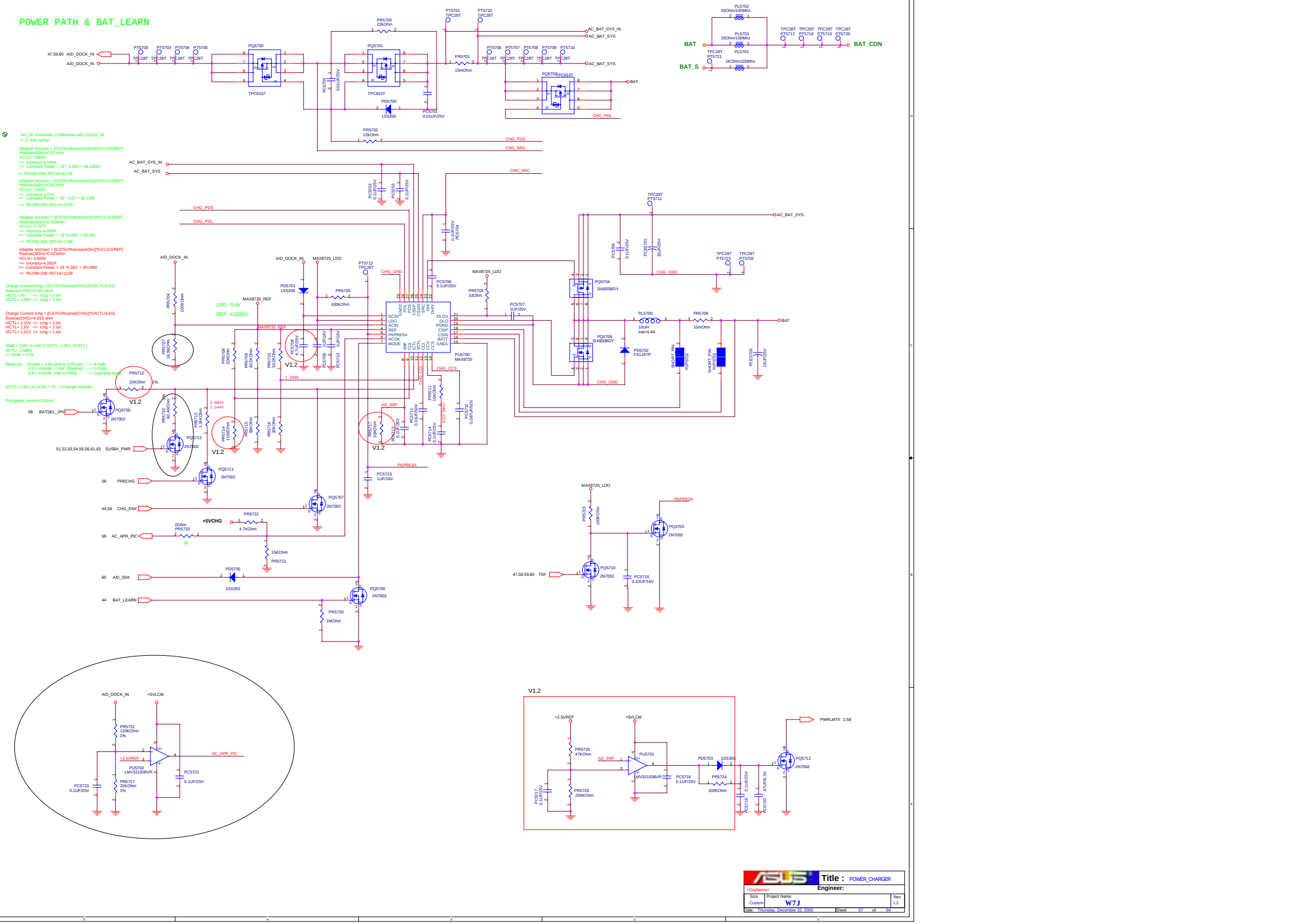
+1.2VSP



ASUS	Title : POWER_VGA_+1.2VSP	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 56 of 64	

POWER PATH & BAT_LEARN



Title : POWER_CHARGER
<OrgName>
Engineer:
Size: Custom
Project Name: W7J
Rev: 1.2
Date: Thursday, December 22, 2005
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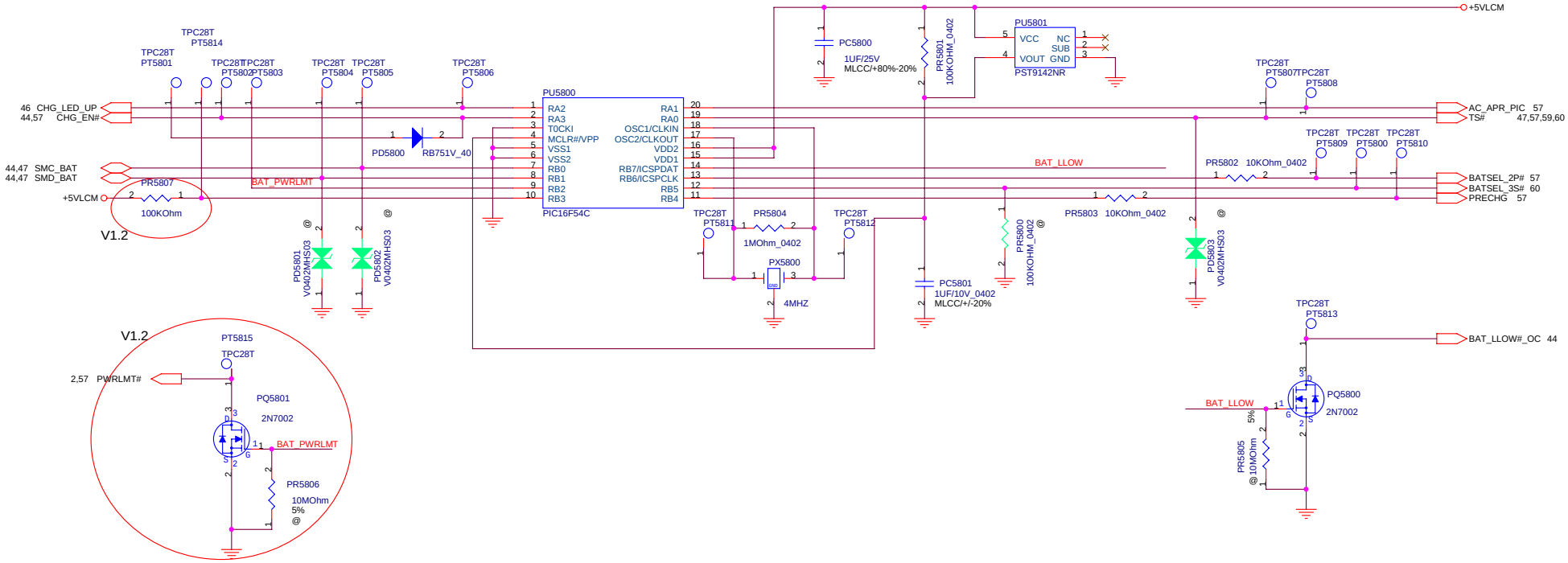
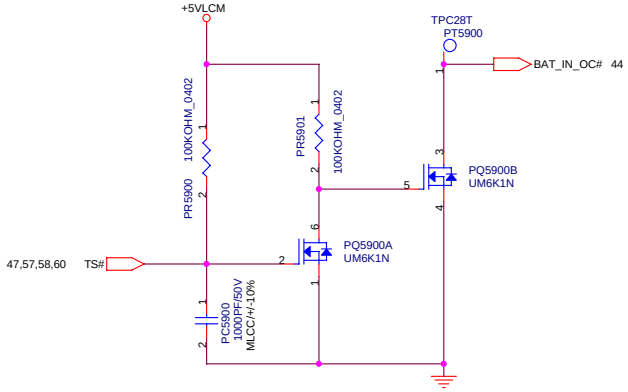
PIC16F54C

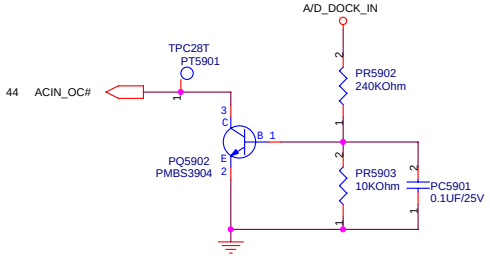


ASUS	Title : POWER_PIC	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 58 of 64	

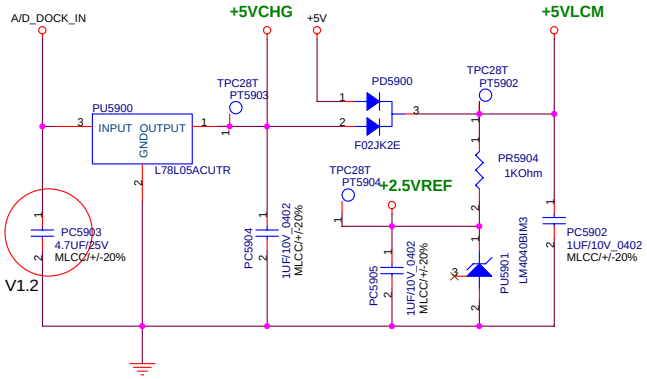
BATTERY IN DETECT



ADAPTER IN DETECT

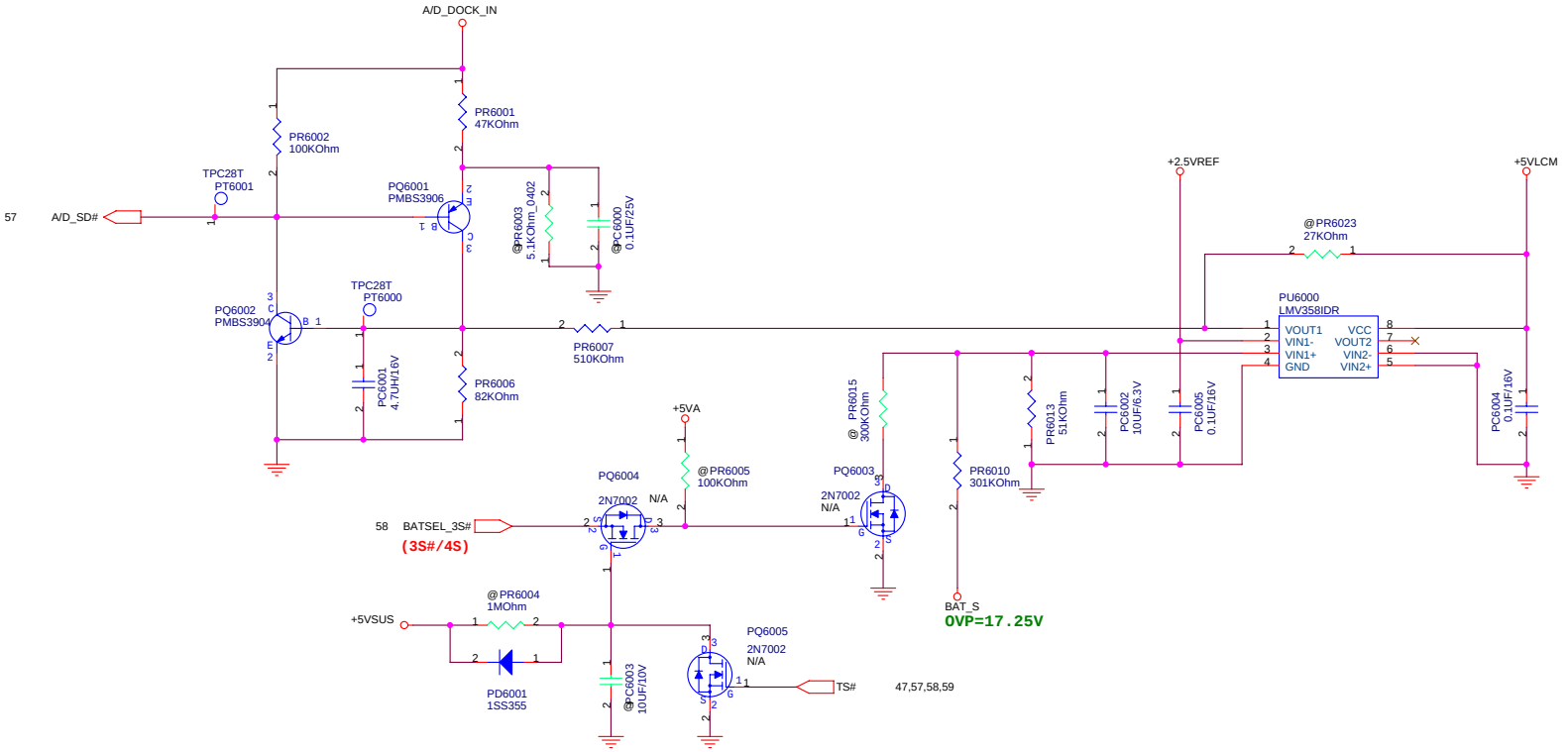


+5VLCM, +5VCHG & +2.5VREF

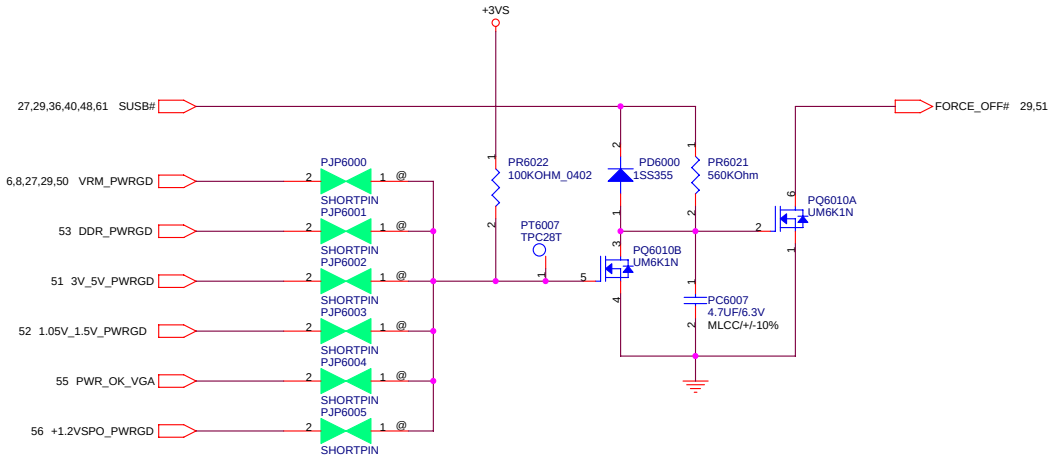


ASUS	Title : POWER_DETECT	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 59 of 64	

BATTERY A/D_SD# (OVP)



POWER GOOD DETECTER



TPC28T PT6003 1 VRM_PWRGD
TPC28T PT6004 1 DDR_PWRGD
TPC28T PT6005 1 3V_5V_PWRGD
TPC28T PT6006 1 1.05V_1.5V_PWRGD

ASUS

Title : POWER_PROTECT

<OrgName>

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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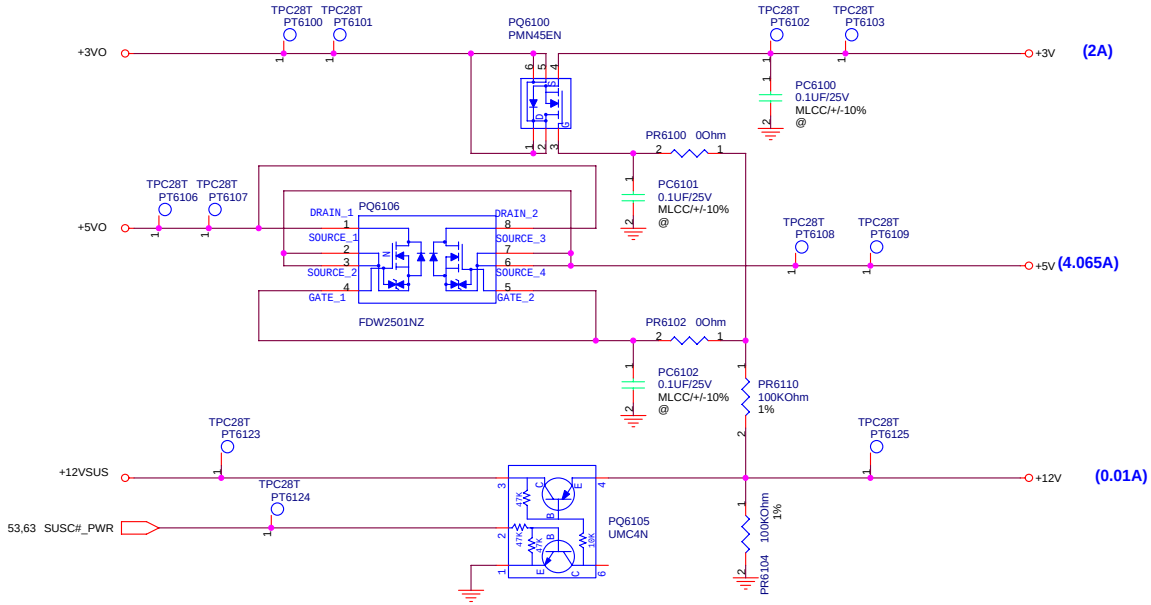
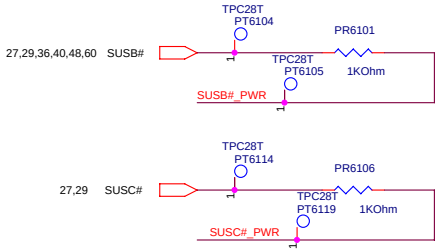
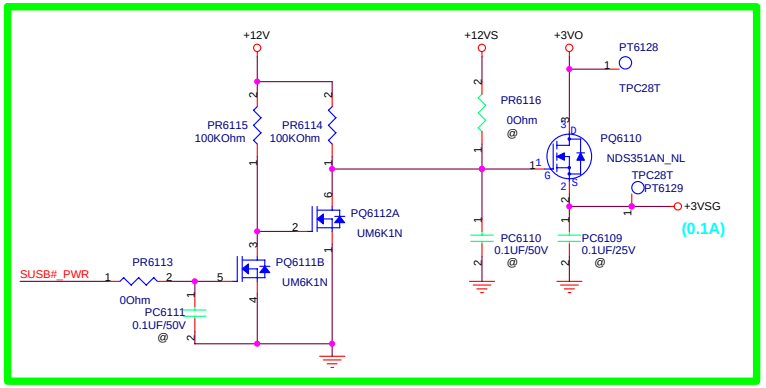
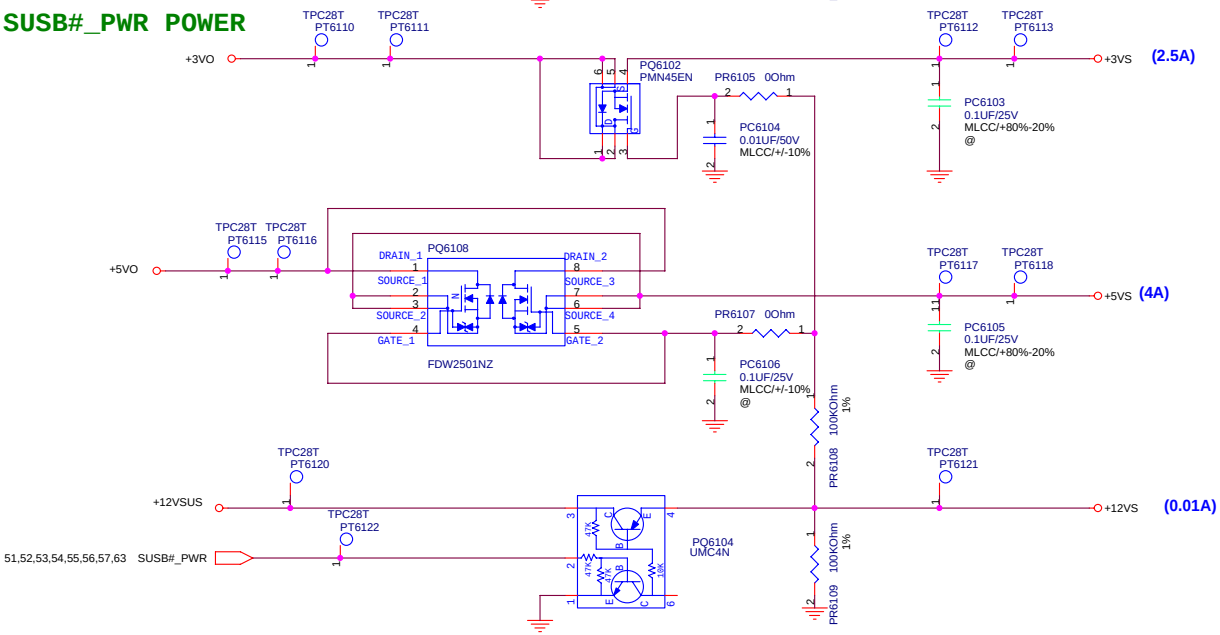
SUSC#_PWR POWER

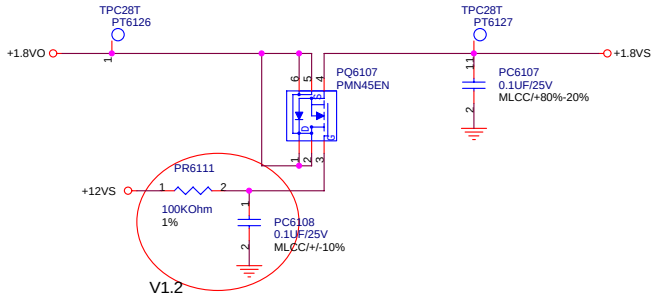






SUSB#_PWR POWER





ASUS	Title : POWER_LOAD SWITCH	
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
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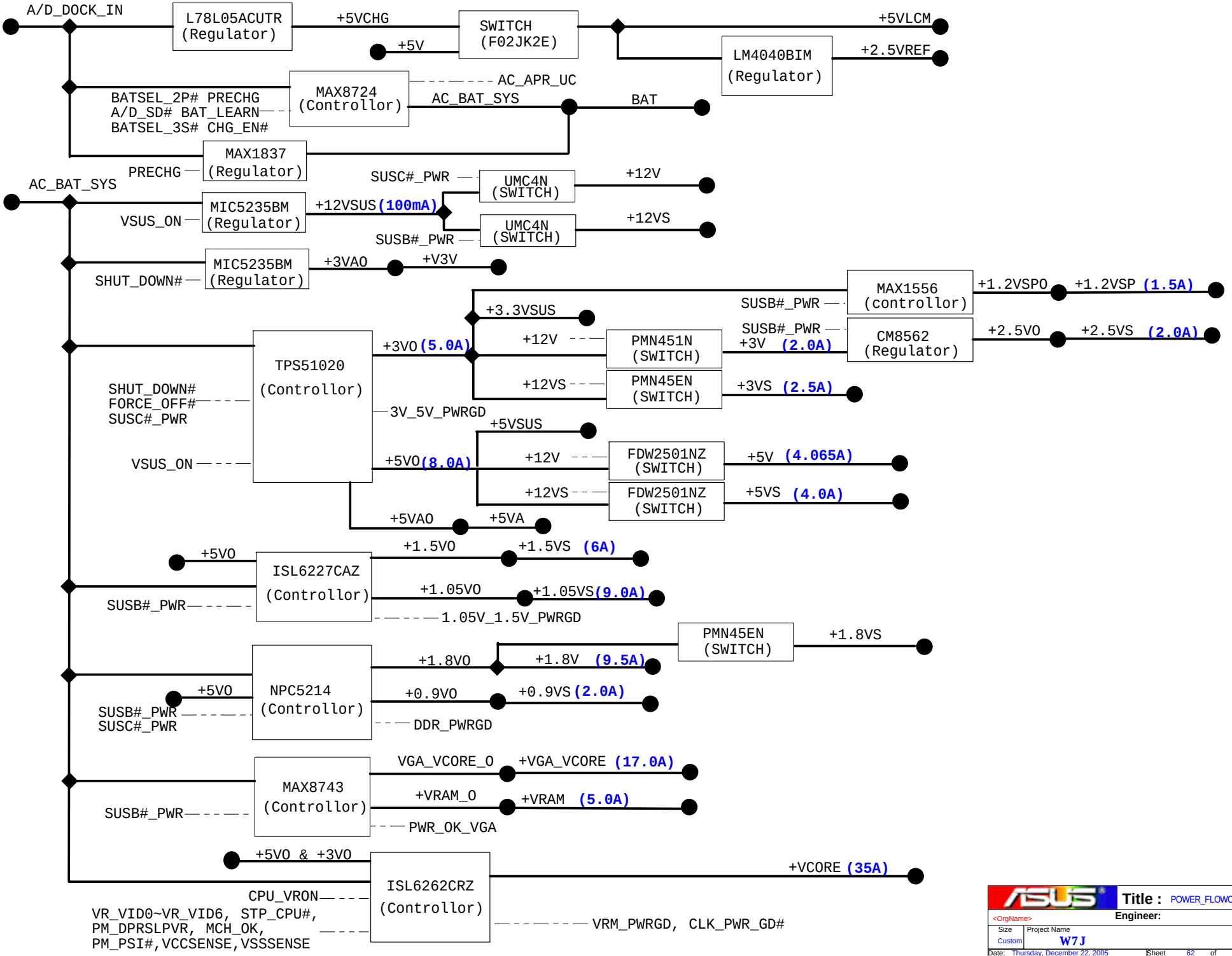

Title : POWER_FLOWCHART		
<OrgName>	Engineer:	
Size: Custom	Project Name: W7J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 62 of 64	

AC_BAT_SYS → AC_BAT_SYS 23,50,51,52,53,54,55,57

+3VA → +3VA 25,29,47,54

+5VA → +5VA 51,54,60

+5VO → +5VO 51,52,53,55,61

+3VO → +3VO 51,52,56,61

+3VSUS → +3VSUS 26,27,28,29,32,38,41,51

+5VSUS → +5VSUS 28,51,60

+3V → +3V 26,29,39,40,41,44,48,54,61

+3VS → +3VS 5,6,8,10,12,15,17,20,21,23,24,27,28,29,30,34,35,36,37,38,40,41,42,43,44,45,46,48,50,52,60,61

+12VSUS → +12VSUS 51,61

+12V → +12V 27,32,33,61

+12VS → +12VS 5,24,34,46,61

+5V → +5V 16,30,32,37,44,45,46,47,48,59,61

+5VS → +5VS 5,24,28,29,30,32,33,42,43,44,46,47,50,61

+2.5VO → +2.5VO 54

+2.5VS → +2.5VS 10,20,21,48,54

+1.8VO → +1.8VO 53,61

+1.8V → +1.8V 8,12,13,14,15,16,48,53

+1.8VS → +1.8VS 20,61

+VCCP → +VCCP 2,3,4,6,7,8,10,11,12,25,28,52

+0.9VS → +0.9VS 16,53

BAT → BAT 57

+5VCHG → +5VCHG 29,57,59

+5VLCM → +5VLCM 23,44,46,57,58,59,60

+2.5VREF → +2.5VREF 54,57,59,60

+VCORE → +VCORE 3,4,5,44,50

+VGA_VCORE → +VGA_VCORE 17,55

+VRAM → +VRAM 18,19,22,55

+1.2VSP → +1.2VSP 17,18,48,56

BAT_CON → BAT_CON 47,57

FOR POWER TEST

+3VA → PJP6300 (1 2 2) SGL_JUMP @ → CPU_VRON_PWR 50

+3VA → PJP6301 (1 2 2) SGL_JUMP @ → SUSB#_PWR → SUSB#_PWR 51,52,53,54,55,56,57,61

+3VA → PJP6302 (1 2 2) SGL_JUMP @ → SUSC#_PWR → SUSC#_PWR 53,61

+3VA → PJP6303 (1 2 2) SGL_JUMP @ → VSUS_ON_PWR → VSUS_ON_PWR 51

Title : POWER_SIGNAL		
<OrgName>	Engineer:	
Size: Custom	Project Name: W7 J	Rev: 1.2
Date: Thursday, December 22, 2005	Sheet 63 of 64	

Rev	Date	Description
R1.0	2005/10/15	1. Initial release.
R1.1	2005/11/29	1. Change Project name from W6J/H to W7J/F 2. Add NET: PWRLMT# to CPU pin: PROCHOT# (Page 2) 3. Add NET: DREFCLKSS,DREFCLKSS# to CLK GEN: pin17,pin18 (Page 6) 4. Add NET: DREFCLKSS,DREFCLKSS# to GMCH: C40,D41 (Page 8) 5. Pull high GMCH VCCA_LVDC to +2.5VS (Page 10) 6. Add Jumper at G72M pin: B4 (Page 20) 7. Change R6811 from 200Kohm to 100Kohm (Page 23) 8. Change U57,U58 from 74LVC1G32GV to NC7SZ08M5 (Page 24) 9. Change D2 from EC31QS04 to RB751V_40 (Page 24) 10. Add Double-pi filter in VGA port (Page 24) 11. Swap ICH PCIE lans (Page 26) 12. Change GPIO7 NET from WB_AP to MUTE_POP_ICHGPIO# (Page 27) 13. Add NET: PWR_LED_1HZ to ICH: GPIO13 (Page 27) 14. Add Q6197 in net: PCIE_WAKE# (Page 27) 15. Add Q6192 in net: PWR_SW#_Q (Page 29) 16. Change R719 from 100Kohm to 1Mohm (Page 29) 17. Change R306 from 1Mohm to 10Mohm (Page 29) 18. Change C388 from 0.33uF to 1uF (Page 29) 19. Change Pull-high LID_EC# from +3VSUS to +3V (Page 29) 20. Change Audio CODEC from ADI1986 to ALC660 (Page 30) 21. Change R6614 from 0ohm to 4.7Kohm (Page 32) 22. Change R6616 from 10Kohm to 51KOhm (Page 32) 23. Change R6613 from 0ohm to 4.7Kohm (Page 32) 24. Change R6615 from 10Kohm to 51KOhm (Page 32) 25. Add NET: MUTE_POP_ICHGPIO# to MUTE_POP# circuit (Page 32) 26. Add Q6193 in net: SUSCLK (Page 34) 27. Change SLB9635TT pin16 from PLT_RST# to BUF_PLT_RST# (Page 34) 28. Delete NET PME# (Page 36) 29. Change Pull-high MDIO04 from +3V to +3VS (Page 37) 30. Change Pull-high XD_PWR_EN from +3V to +3VS (Page 37) 31. Change PCIE lans from port 1 to port 2 (Page 38) 32. Add C6625,C6626 in phone connector (Page 39) 33. Change PCIE lans from port 3 to port 1 (Page 40) 34. Add NET: EXPD# to R5538 pin20 (Page 40) 35. Add NET: C_PRESENT# to R5538 pin9,pin10 (Page 40) 36. Change PCIE lans from port 2 to port 3 (Page 41) 37. Change Pull-high 802WLAN_ON# from +3V to +3VSUS (Page 41) 38. Change FWH packaging from PLCC to TSOP (Page 43) 39. Add NET: EXPD# to M38857 P53 (Page 44) 40. Add NET: WB_AP to M38857 P67 (Page 44) 41. Add NET: C_PRESENT# to M38857 P62 (Page 44) 42. Add NET: ACZ_RST#_AUD to M38857 P61 (Page 44) 43. Change U10,U6012 pin4 from SUSC# to SUSC (Page 45) 44. Add Q6196 in net: BTPWRCL# (Page 45) 45. Add R6922 between net: WIRELESS_LAN_ON/OFF# and WB_AP (Page 47) 46. Add Q6198 in +3VS discharge (Page 48) 47. Change Power LED ON circuit (Page 48)

Rev	Date	Description
R1.2	2005/12/20	1. Change R6491 from 23.2KOhm to 51KOhm (Page 5) 2. Add Q6200 at U42 :D2+,D2- (Page 5) 3. Add NET: DREFCLKSS,DREFCLKSS# at ICS954310 pin: pin17,18 (Page 6) 4. Add RN79 at DREFCLKSS,DREFCLKSS# (Page 6) 5. Add NET: DREFCLKSS,DREFCLKSS# at GMCH: C40,D41 (Page 8) 4. Add R6934,R6935 at DREFCLKSS,DREFCLKSS# (Page 8) 5. Change R1001 from 1Kohm to C6631:0.1uF (Page 16) 6. Modify LCD enable circuit by U6059 (Page 23) 7. Change L89,L90,L92 to Bead 120Ohm/100MHz (Page 24) 8. Change Q60,Q61 from SI1906DL to SI1902DL (Page 24) 9. Add C6632 in Y1 (Page 25) 10. Connect H_DPRSTP# to PU5000 (Page 25) 11. Change U69 from SN74LVC1G32G to 74LVC1G32GV (Page 26) 12. Disonnect STP_CPU# to PU5000 (Page 27) 13. Add GPIO9:W_OLED# (Page 27) 14. Change R523 from 10KOhm to 100KOhm (Page 29) 15. Change R303 from 10KOhm to C6630:1uF (Page 29) 16. Add R6936 in Net:PWR_SW#_Q (Page 29) 17. Add R6633,R6634,R6635,R6636 in CN20(Page 31) 18. Add R6938 in +3.3Vaux (Page 41) 19. Change CE41,CE5705,CE25 from 100uF to 150uF (Page 45) 20. Add R6937 in BTPWRCL# (Page 45) 21. Change Q6180,Q6181 by Q6202 (Page 46) 22. Add Q6201,LED10 in WIRELESS_OLED# (Page 46) 23. Change R6686 from 0Ohm to 470Ohm (Page 47) 24. Add R6940 in Power Board +5Vs (Page 47)

<Variant Name>

ASUSTek Computer INC. NB1

Title : History

Engineer:

Size	Project Name	Rev
Custom	W7J	1.2

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