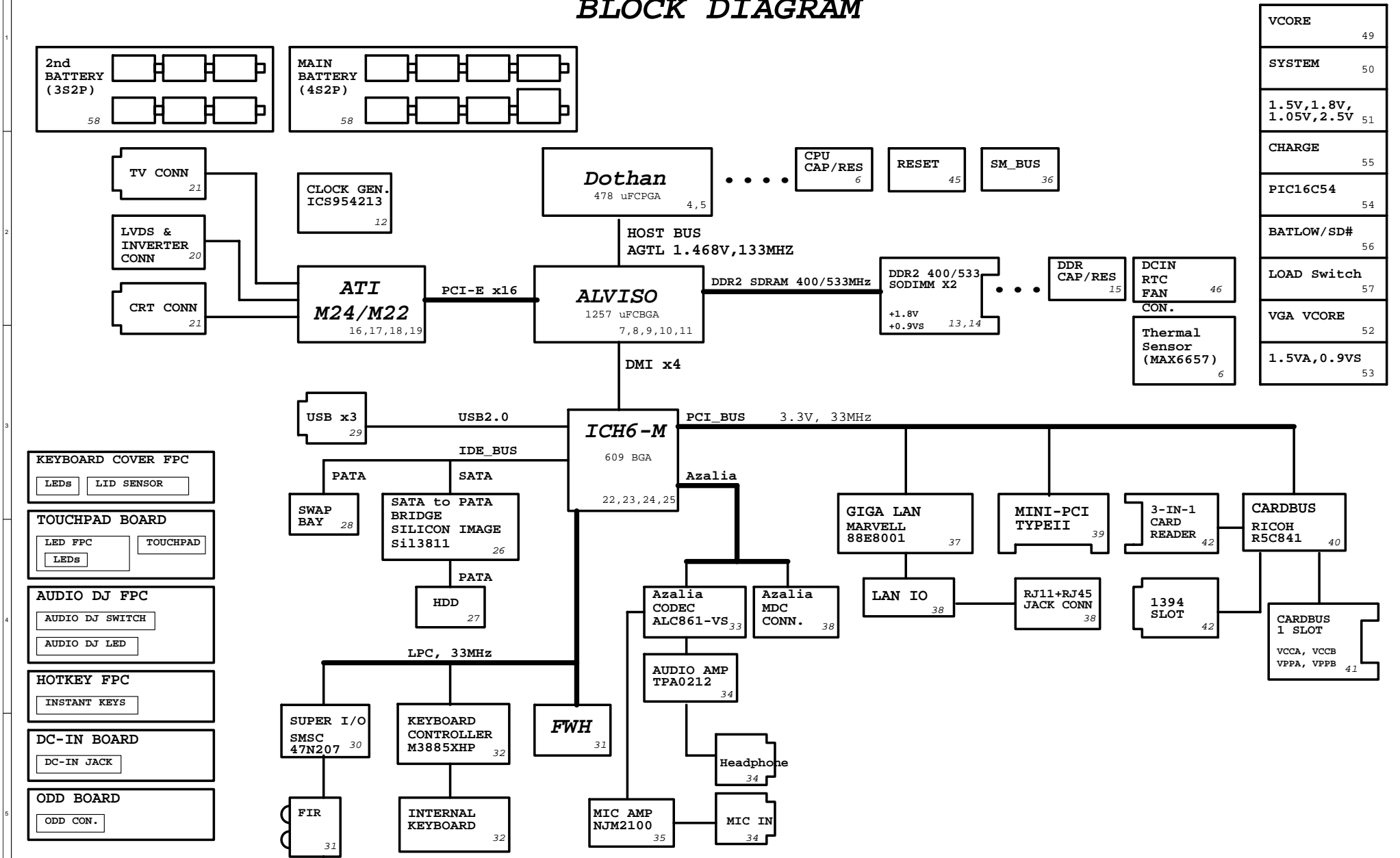


W3V/A SCHEMATIC V2.1

PAGE	Content	PAGE	Content
	SYSTEM PAGE REF.		POWER PAGE REF.
4	DOTHAN CPU-1	49	VCORE_MAX1987
5	DOTHAN CPU-2	50	SYSTEM
6	CPU CAP/THERMAL SENSOR/ITP	51	1.5V,1.8V,2.5V,1.05V
7	ALVISO: CPU	52	VGA VCORE
8	ALVISO: DDR2 & DMI & PEG	53	1.5VA & DDR2
9	ALVISO: DDR2	54	PIC16C54/BATCON/PWOK
10	ALVISO: POWER & Caps	55	CHARGER
11	ALVISO: GND & NCTF & Straps	56	BATLOW/SD#
12	CLOCK GEN (ICS954213)	57	LOAD SWITCH
13	DDR2 SODIMM(0) & Caps	58	BATCON
14	DDR2 SODIMM(1) & Caps	59	Power Flowchart
15	DDR2 TERMINATOR	60	HISTORY
16	ATI M24: MAIN	61	DC_IN CONN.
17	ATI M24: MEMORY/SS	62	ODD CONN.
18	ATI M24: PWR & GND	63	TP&LED CONN
19	ATI M24: Strapping		
20	LVDS/INVERTER		
21	CRT/TV/TPM CONN		
22	ICH6: SATA/LPC/IDE/ACZ (1)		
23	ICH6: PCI/DMI/USB/PCIE(2)		
24	ICH6M: PWR/GND/CAPS(3)		
25	ICH6: PULL UP & Straping		
26	SATA to PATA BRIDGE		
27	HDD CON		
28	SWAP BAY CON		
29	USB PORTS		
30	SUPER I/O (LPC47N207)		
31	FIR & FWH		
32	KBC 38857		
33	Azalia AUDIO (ALC861-VS)		
34	AUDIO AMP/JACKS		
35	MIC AMP		
36	SMBUS		
37	PCI GIGA LAN (88E8001)		
38	RJ11_RJ45/MDC/BT		
39	MINIPCI		
40	PCI CARDBUS (R5C841)		
41	PCI PCMCIA SOCKET A		
42	IEEE1394A/3in1 CONN		
43	LEDs & DEBUG PORT		
44	DJ/HOTKEY/TP LED		
45	PWR SW/RESET/KBC LED		
46	FAN & DC_IN		
47	POWER-ON SEQUENCE		
48	DISCHARGE/EMI/VCCA		

W3V/A:Dothan & Alviso-PM+M24-CSP/Alviso-GM BLOCK DIAGRAM



PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
Mini_PCI	AD18	3	B,D	
LAN --88E8001	AD16	0	C	
CardBus	AD17	1	B	
1394	AD17	1	A	
3 IN 1		1	C	

Azalia : PCI_INTB#
 USB 0,1 : PCI_INTA#
 USB 2,3 : PCI_INTD#
 USB 4,5 : PCI_INTC#

SMBUS ADDRESS :

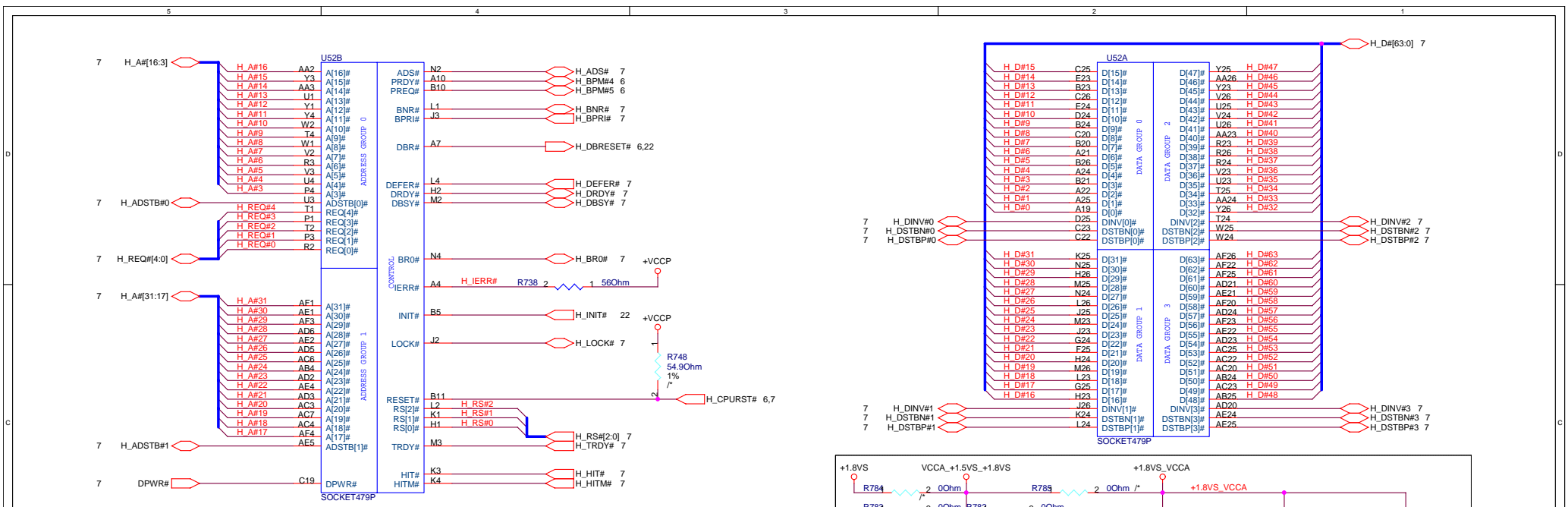
CLK = 1101001x (D2)
 DDR_SODIMMO = 1010010x (A4)
 DDR_SODIMM1 = 1010000x (A0)
 THERMAL = 1001100x (98)

ICH6M_GPIO	Used As	Signal Name
GPIO00	GPI	KBDDT0
GPIO01	GPI	KBDDT1
GPIO06	GPI	PM_BMBUSY#
GPIO07	GPI	FIR_SEL
GPIO08	GPI	EXTSMI#_3A
GPIO11	GPI	LID_ICH#_3A
GPIO12	GPI	KBDSKI_3
GPIO13	GPI	ATI_OVERTEMP#
GPIO14	GPI	GPI14
GPIO15	GPI	CHG_EN#_OC
GPIO16	GPO	GPO16
GPIO17	GPO	GPO17
GPIO21	GPO	BACK_OFF#
GPIO23	GPO	FWH_WP#
GPIO24	GPO	CB_SD#
GPIO25	BLINK	ICH6_1HZ
GPIO26	GPI	SATA_DET_#0
GPIO27	GPI	PCB_VID0
GPIO28	GPI	PCB_VID1
GPIO29	GPI	PCB_VID2
GPIO30	GPI	SATA_DET_#2
GPIO31	GPI	AGP_EXT
GPIO33	GPO	XIDE_EN#_3
GPIO34	GPO	OP_SD#
GPIO40	GPI	PID0
GPIO41	GPI	PID1

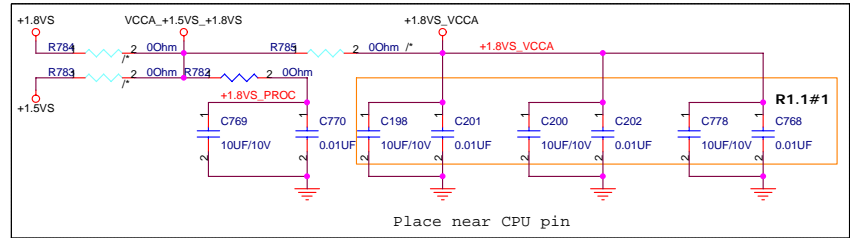
M38857_GPIO	Used As	Signal Name
P20	GPO	KBCRSM
P21	GPO	BAT_SEL
P22	GPO	BAT_LEARN
P23	GPO	MSK_INSTKEY#
P42	GPO	WATCHDOG
P43	GPI	SWDJ_EN#
P44	GPO	KBCPURST_3Q
P45	GPO	KBC_GA20
P46	GPO	KBSCI_3Q
P47	GPI	PM_CLKRUN#
P50	GPI	BAT_LLOW#_KBC
P51	GPO	DJ_LED_EN
P52	GPO	WIRELESS_LED#
P53	GPO	BAT_LOW#_KBC
P54	GPI	BAYDOCK_IN#
P55	GPI	BAT1_IN#_OC
P56	GPO	FAN_DA
P57	GPO	ADJ_BL
P60	GPI	BT_#
P61	GPI	INTERNET_#
P62	GPI	CPUFAN_SPD_A
P63	GPI	WIRELESS_#
P64	GPI	ACIN_OC
P65	GPI	MARATHON_#
P66	GPO	PANLOCK_#
P67	GPI	BAT2_IN#_OC
P76	GPIO	SMD_BAT_KBC
P77	GPO	SMC_BAT_KBC

M38857_GPIO	Used As	Signal Name
P27	GPO	--
P26	GPO	NUM_LED#
P25	GPO	CAP_LED#
P24	GPO	SET_PCIRSTNS#
P41	GPO	BT_LED#
P40	GPO	KBC_EXTSMI

47N207_GPIO	Used As	Signal Name
GP10	GPI	BAY_IN0
GP11	GPI	BAY_IN1
GP12	GPI	--
GP13	GPI	SW_RST#
GP14	GPIO	--
GP15	GPO	BAY_RST
GP16	GPO	DJKEY_EN
GP17	GPO	802_EN#
GP34	GPO	OVER_CLK1
GP35	GPO	OVER_CLK2
GP36	GPO	--

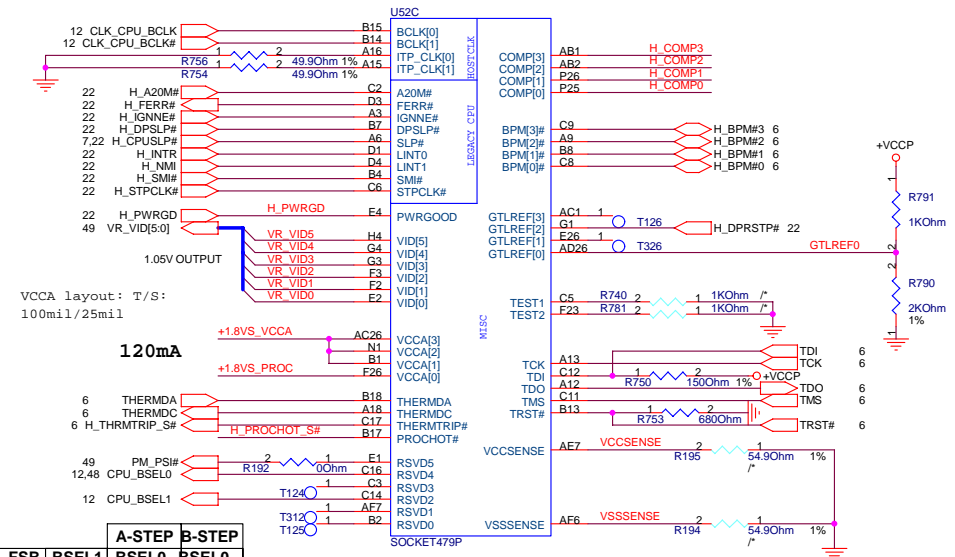
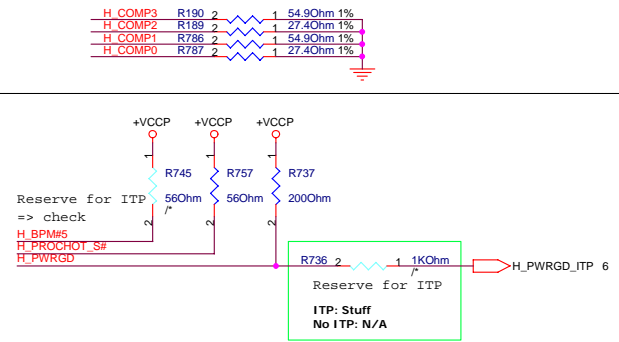


P/N = 12-046004791

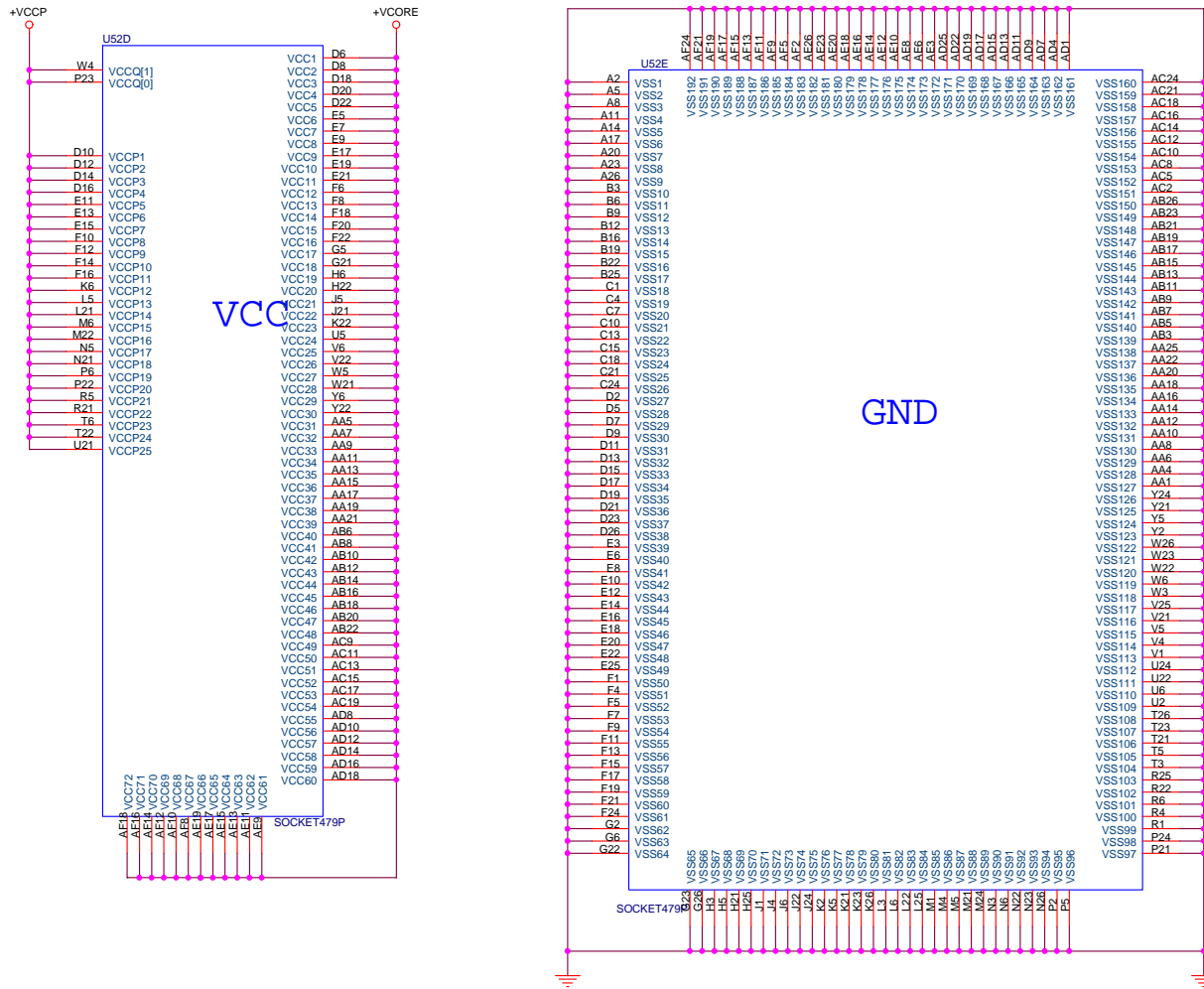


Layout note:
 COMP0 and COMP2 need to be Zo=27.4ohm traces.
 Best estimate is 18mil wide trace for outer layers and 14mil if on internal layer. See RDDP of Banias.
 Traces should be shorter than 0.5". Refer to latest CS layout

COMP1, COMP3 should be routed as Zo=55ohm traces shorter than 0.5"



	A-STEP	B-STEP
FSB	BSEL1	BSELO
400	0	N/A
533	0	N/A



Mobile Dothan VID Table

VID[5..0]	Voltage	VID[5..0]	Voltage
0 0 0 0 0	1.708V	1 0 0 0 0	1.196V
0 0 0 0 1	1.692V	1 0 0 0 1	1.180V
0 0 0 1 0	1.676V	1 0 0 1 0	1.164V
0 0 0 1 1	1.660V	1 0 0 1 1	1.148V
0 0 1 0 0	1.644V	1 0 0 1 0	1.132V
0 0 1 0 1	1.628V	1 0 0 1 1	1.116V
0 0 1 1 0	1.612V	1 0 0 1 1	1.100V
0 0 1 1 1	1.596V	1 0 0 1 1	1.084V
0 1 0 0 0	1.580V	1 0 1 0 0	1.068V
0 1 0 0 1	1.564V	1 0 1 0 1	1.052V
0 1 0 1 0	1.548V	1 0 1 0 1	1.036V
0 1 0 1 1	1.532V	1 0 1 0 1	1.020V
0 1 1 0 0	1.516V	1 0 1 1 0	1.004V
0 1 1 0 1	1.500V	1 0 1 1 0	0.988V
0 1 1 1 0	1.484V	1 0 1 1 0	0.972V
0 1 1 1 1	1.468V	1 0 1 1 1	0.956V
1 0 0 0 0	1.452V	1 1 0 0 0	0.940V
1 0 0 0 1	1.436V	1 1 0 0 1	0.924V
1 0 0 1 0	1.420V	1 1 0 1 0	0.908V
1 0 0 1 1	1.404V	1 1 0 1 1	0.892V
1 0 1 0 0	1.388V	1 1 0 1 0	0.876V
1 0 1 0 1	1.372V	1 1 0 1 0	0.860V
1 0 1 1 0	1.356V	1 1 0 1 1	0.844V
1 0 1 1 1	1.340V	1 1 0 1 1	0.828V
1 1 0 0 0	1.324V	1 1 1 0 0	0.812V
1 1 0 0 1	1.308V	1 1 1 0 1	0.796V
1 1 0 1 0	1.292V	1 1 1 0 1	0.780V
1 1 0 1 1	1.276V	1 1 1 0 1	0.764V
1 1 1 0 0	1.260V	1 1 1 1 0	0.748V
1 1 1 0 1	1.244V	1 1 1 1 0	0.732V
1 1 1 1 0	1.228V	1 1 1 1 1	0.716V
1 1 1 1 1	1.212V	1 1 1 1 1	0.700V



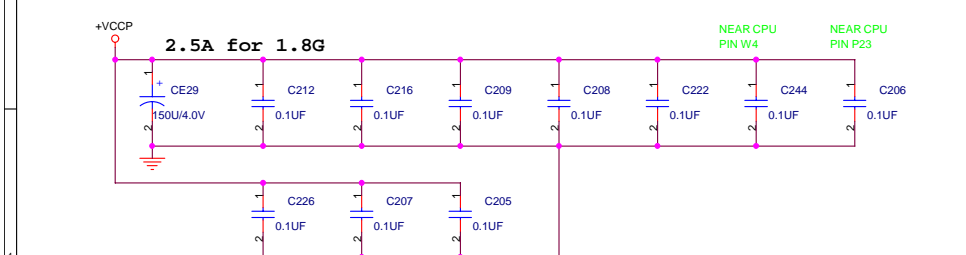
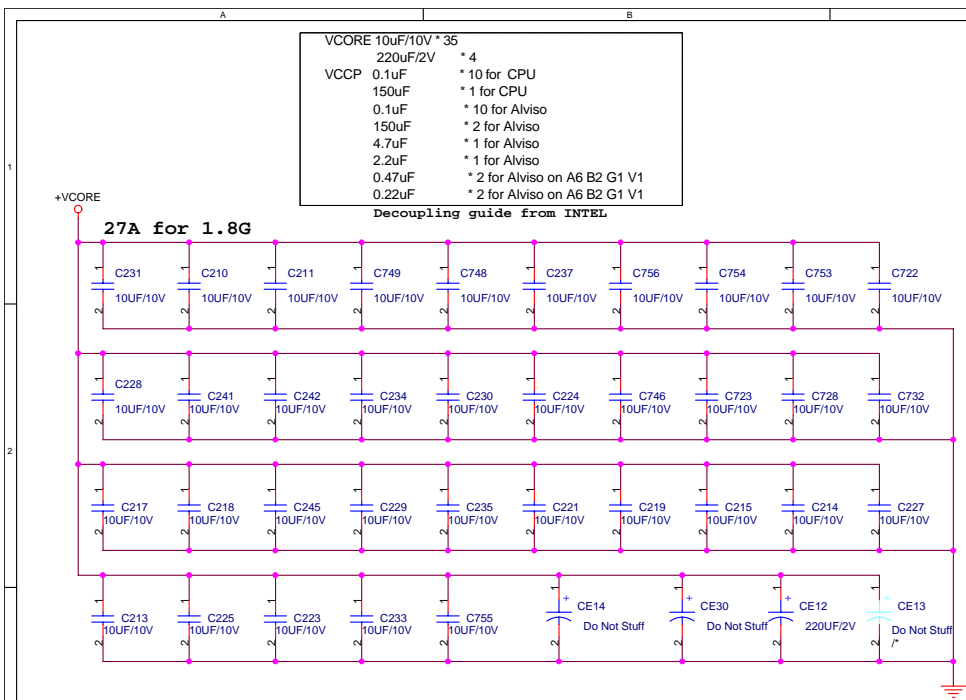
PROJECT: W3V

REVISION: 2.1
 DATE: Monday, January 17, 2005
 SHEET: 5 OF 63

DESCRIPTION: DOTHAN CPU (2)

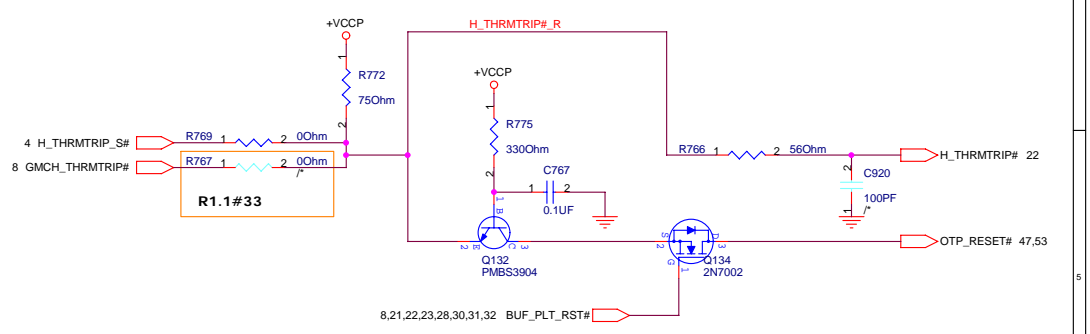
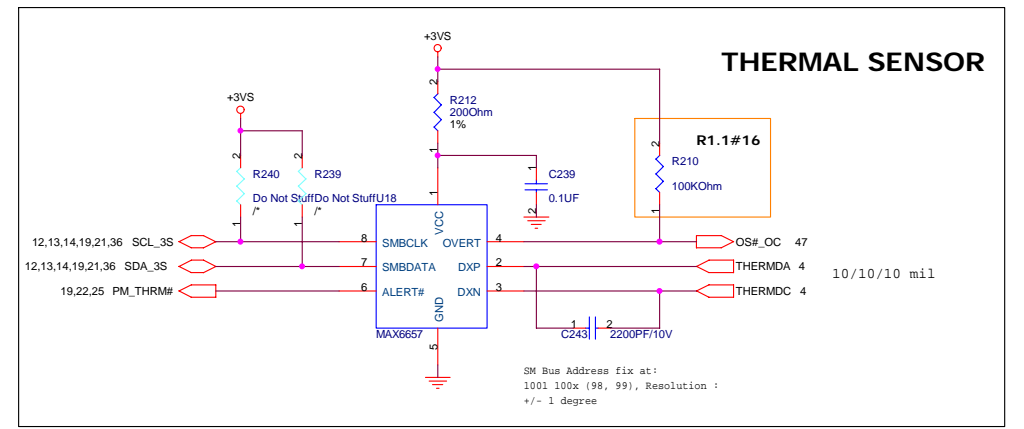
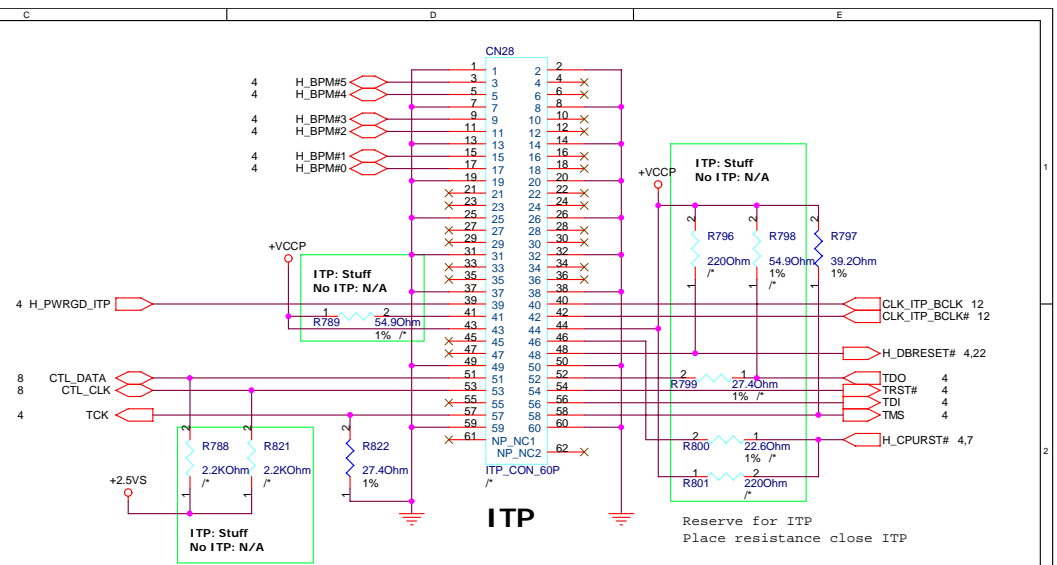
SCHEMATIC FILE NAME: <OrgName>
 RELEASE DATE:

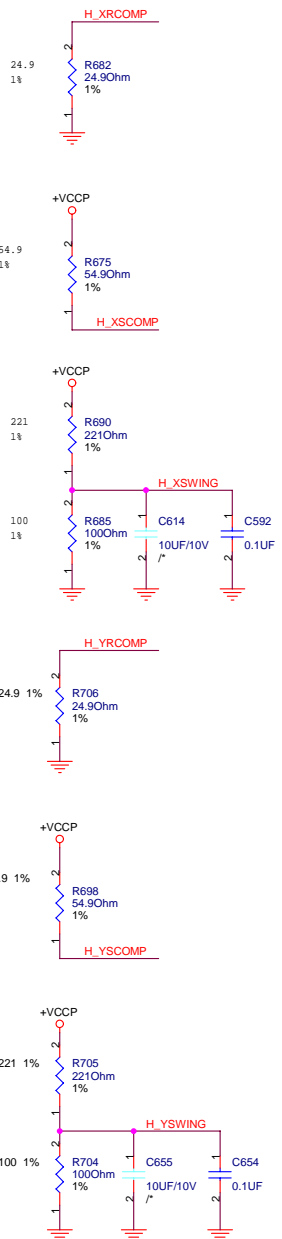
DESIGN ENGINEER: M.Y.



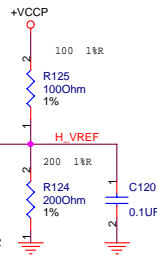
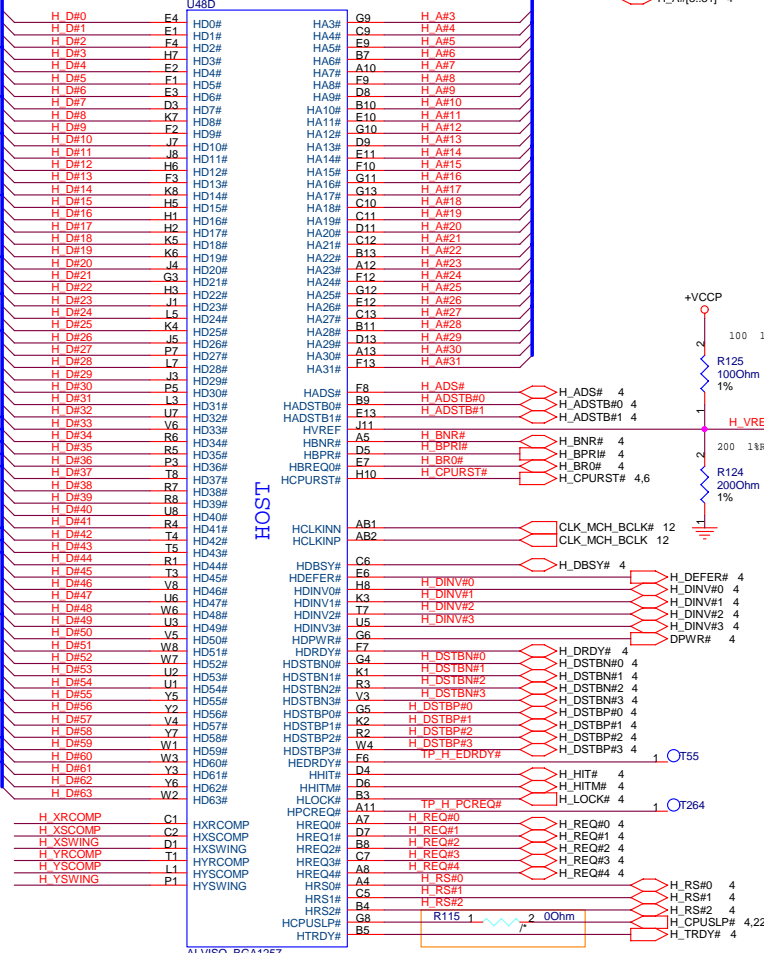
DOTHAN VID TABLE

CPU FREQ.	HFM VOLTAGE	1.6G	1.4G	1.2G	1G	LFM 0.6G	C3/C4
1.8G	1.308V	1.292V	1.260V	1.228V	1.196V	0.844V	0.748V
1.7G							



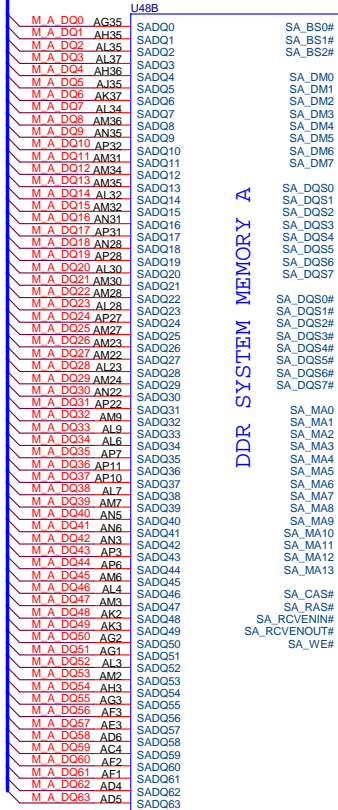


4 H_D#[0..63]

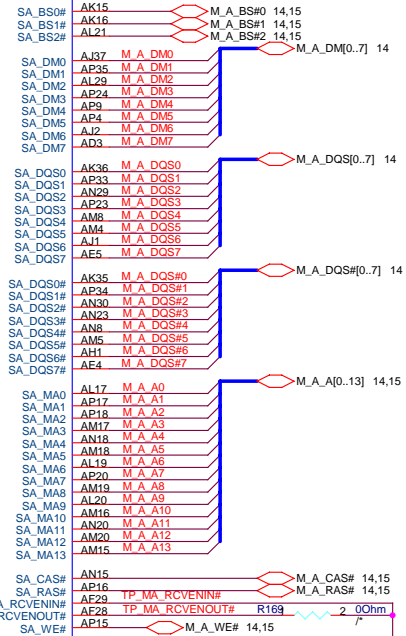


14 M_A_DQ[0..63]

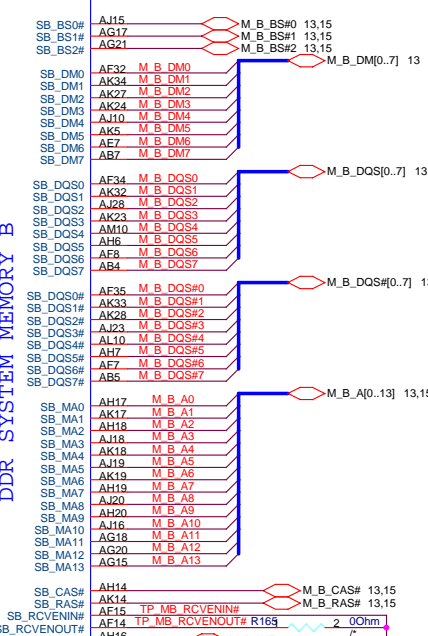
13 M_B_DQ[0..63]



DDR SYSTEM MEMORY A



DDR SYSTEM MEMORY B

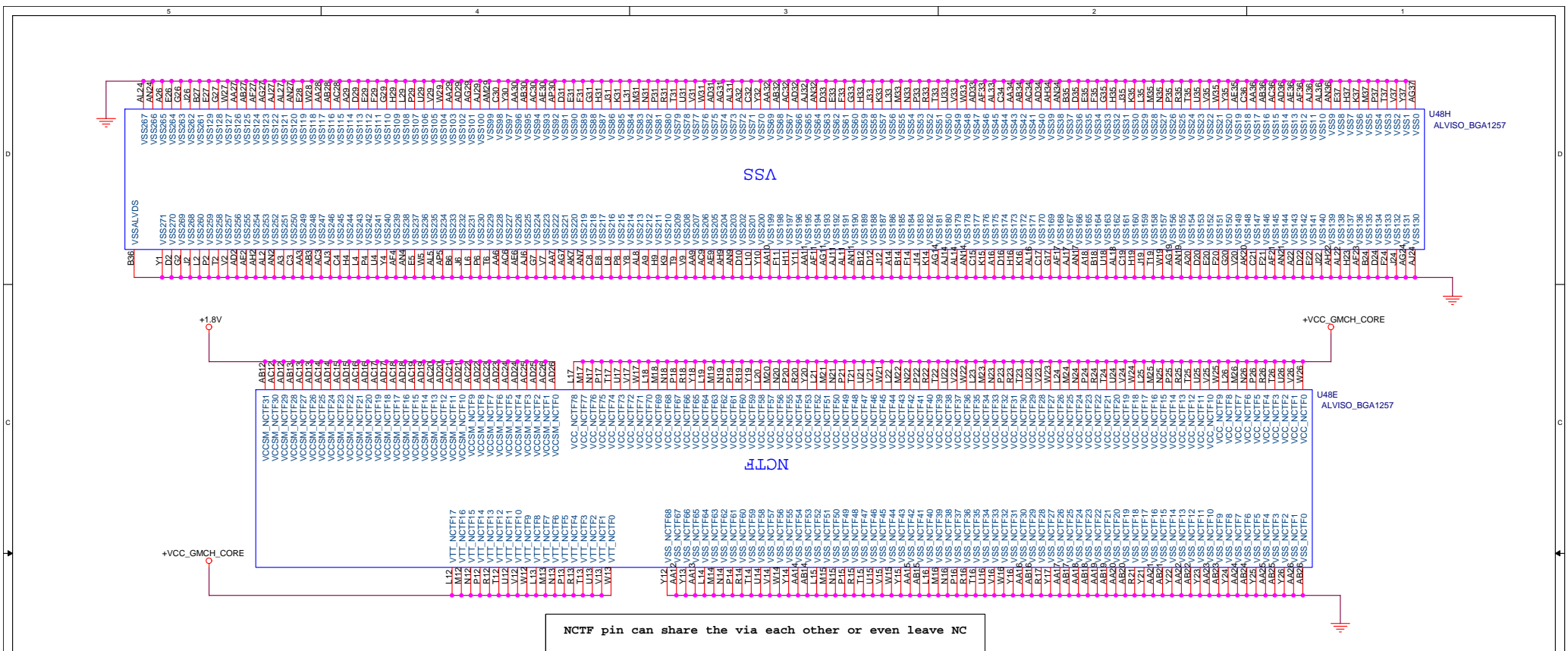


REVISION	DATE: Monday, January 17, 2005	DESCRIPTION:
2.1	SHEET 9 OF 63	MCH: DDR2

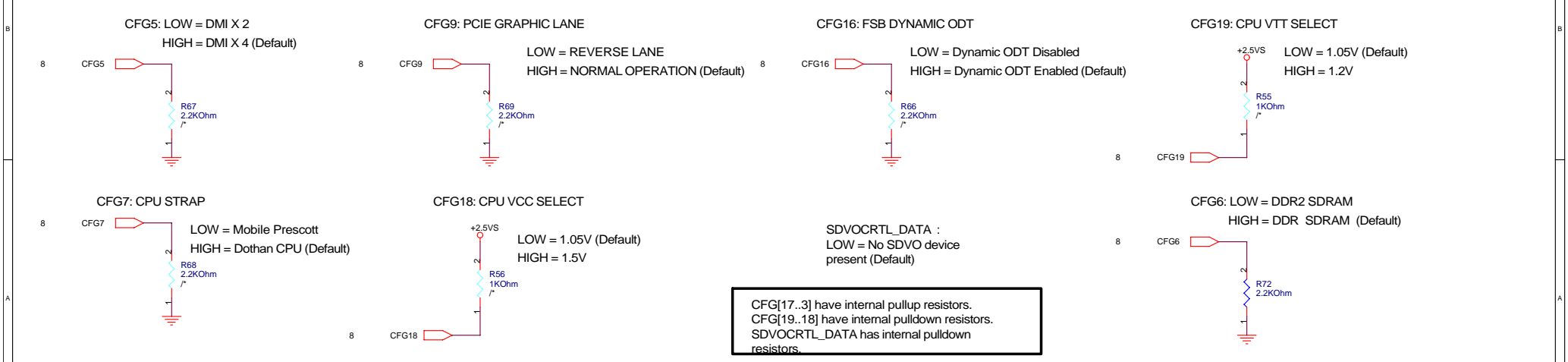
SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
RELEASE DATE :		M.Y.

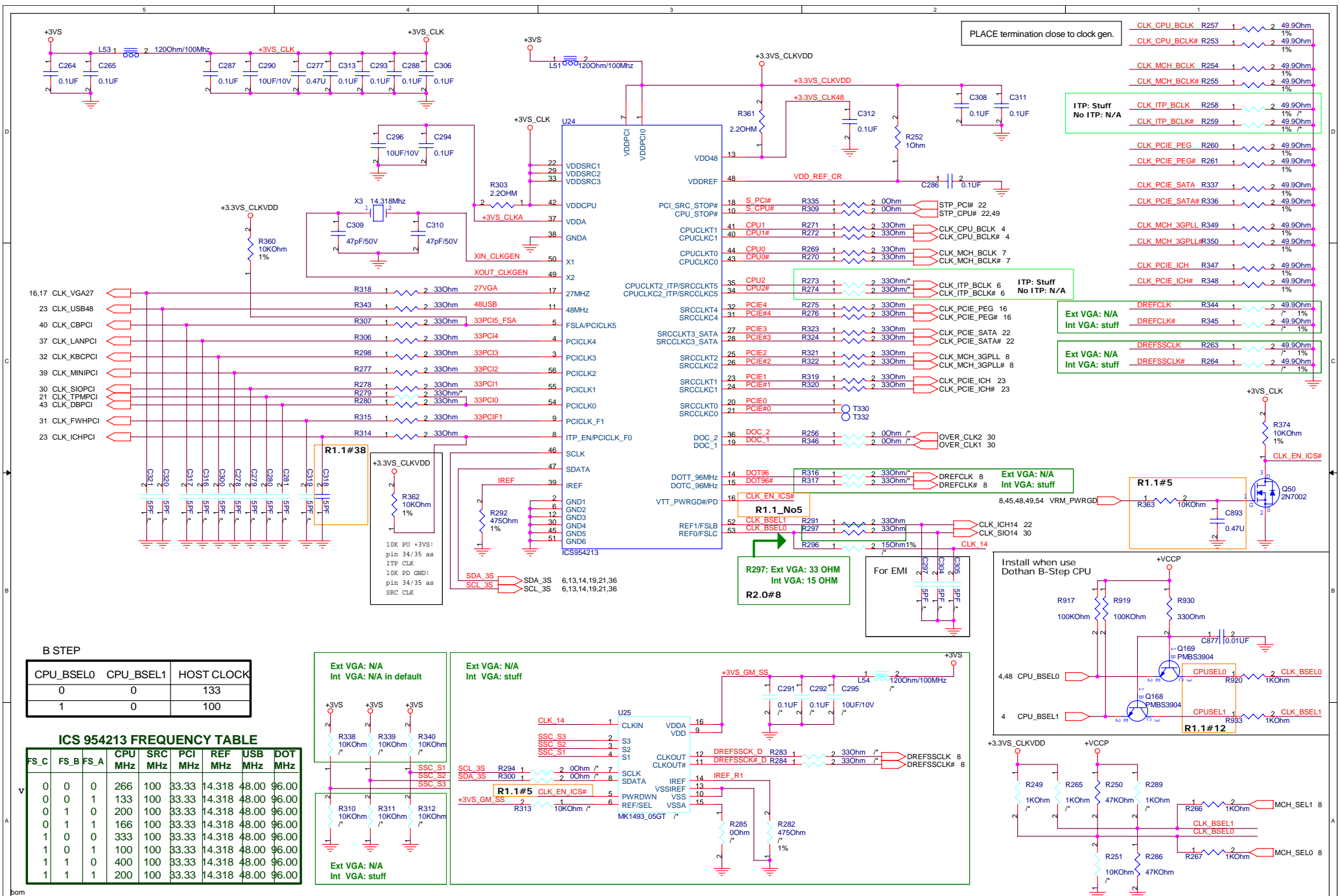


PROJECT: W3V



NCTF pin can share the via each other or even leave NC





PLACE termination close to clock gen.

ITP: Stuff
No ITP: N/A

Ext VGA: N/A
Int VGA: stuff

Ext VGA: N/A
Int VGA: stuff

Ext VGA: N/A
Int VGA: stuff

R297: Ext VGA: 33 OHM
Int VGA: 15 OHM

Install when use
Dothan B-Step CPU

B STEP

CPU_BSEL0	CPU_BSEL1	HOST CLOCK
0	0	133
1	0	100

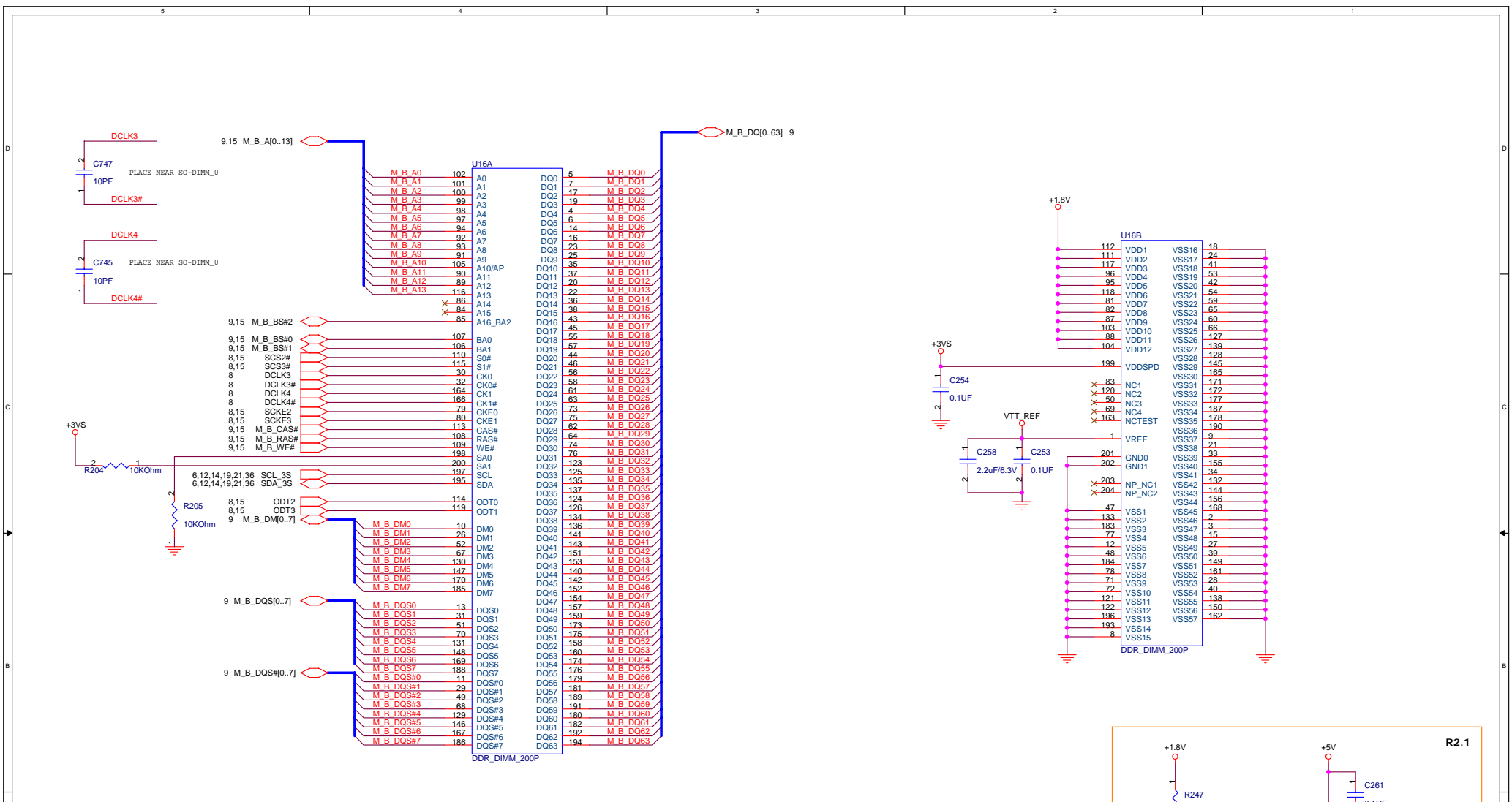
ICS 954213 FREQUENCY TABLE

FS_C	FS_B	FS_A	CPU MHz	SRC MHz	PCI MHz	REF MHz	USB MHz	DOT MHz
0	0	0	266	100	33.33	14.318	48.00	96.00
0	0	1	133	100	33.33	14.318	48.00	96.00
0	1	0	200	100	33.33	14.318	48.00	96.00
0	1	1	166	100	33.33	14.318	48.00	96.00
1	0	0	333	100	33.33	14.318	48.00	96.00
1	0	1	100	100	33.33	14.318	48.00	96.00
1	1	0	400	100	33.33	14.318	48.00	96.00
1	1	1	200	100	33.33	14.318	48.00	96.00

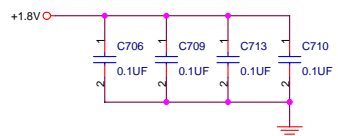
Ext VGA: N/A
Int VGA: N/A in default

Ext VGA: N/A
Int VGA: stuff

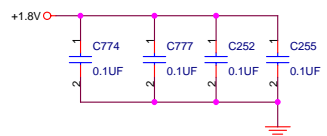
Ext VGA: N/A
Int VGA: stuff



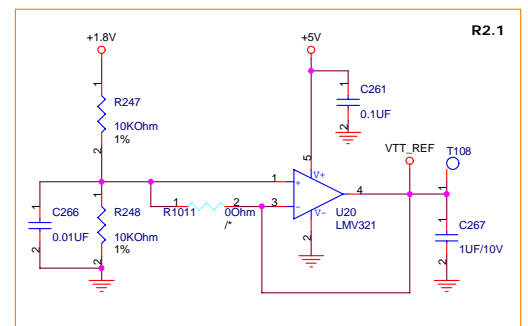
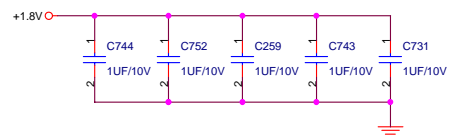
Layout Note: Place these High-Freq decoupling Caps near the GMCH

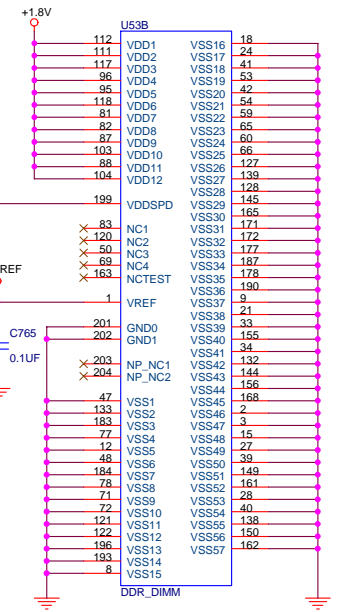
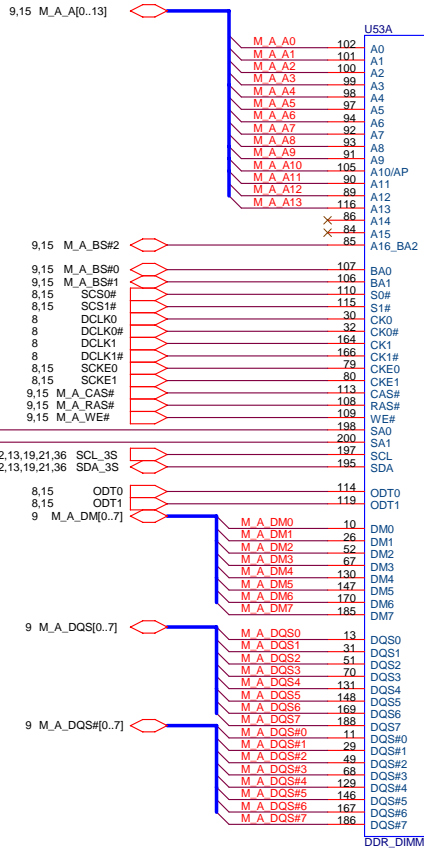
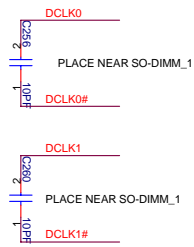


Layout Note: Place these Caps near SO DIMM 0

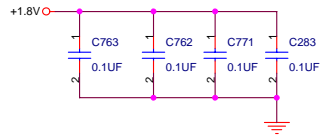


Layout Note: Place these Caps near SO DIMM 0

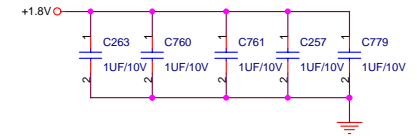


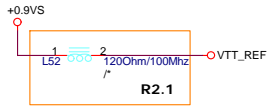


Layout Note: Place these Caps near SO DIMM 1

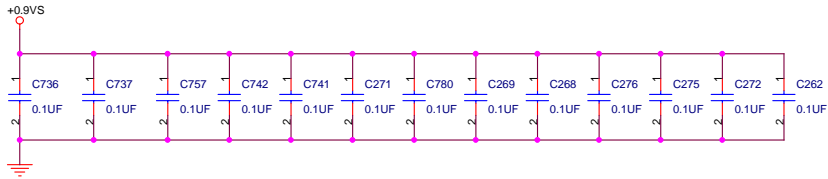


Layout Note: Place these Caps near SO DIMM 1

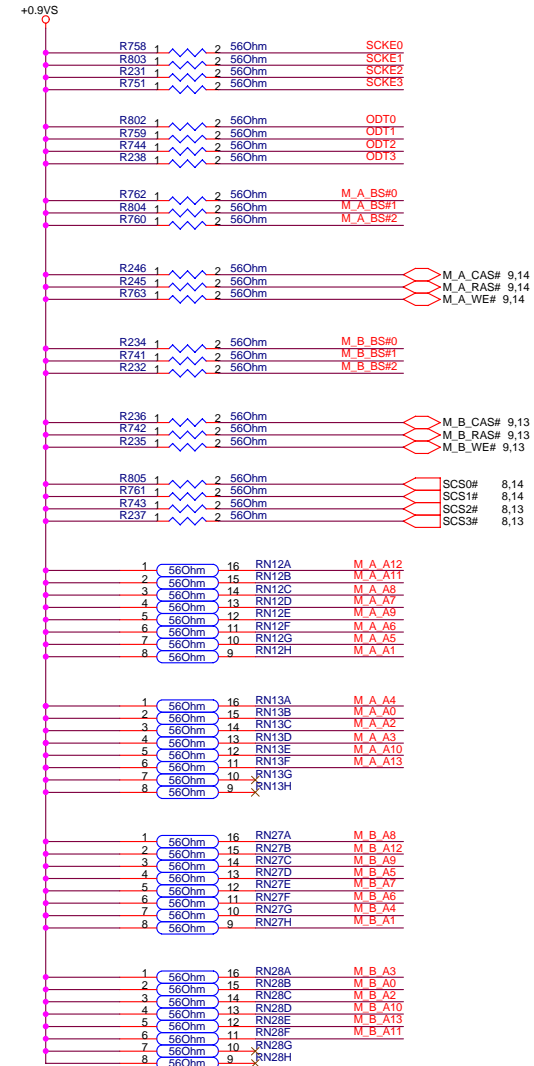
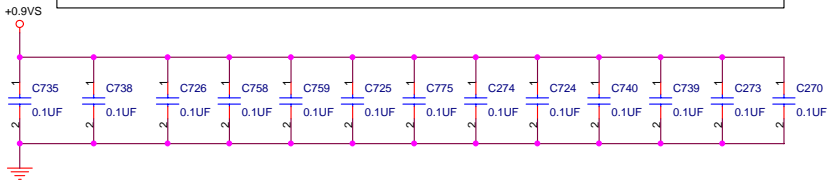




- M_A_A#[0..13] 9,14
- M_A_BS#[0..2] 9,14
- M_B_A#[0..13] 9,13
- M_B_BS#[0..2] 9,13
- SCKE[0..3] 8,13,14
- ODT[0..3] 8,13,14



Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



PROJECT: W3V

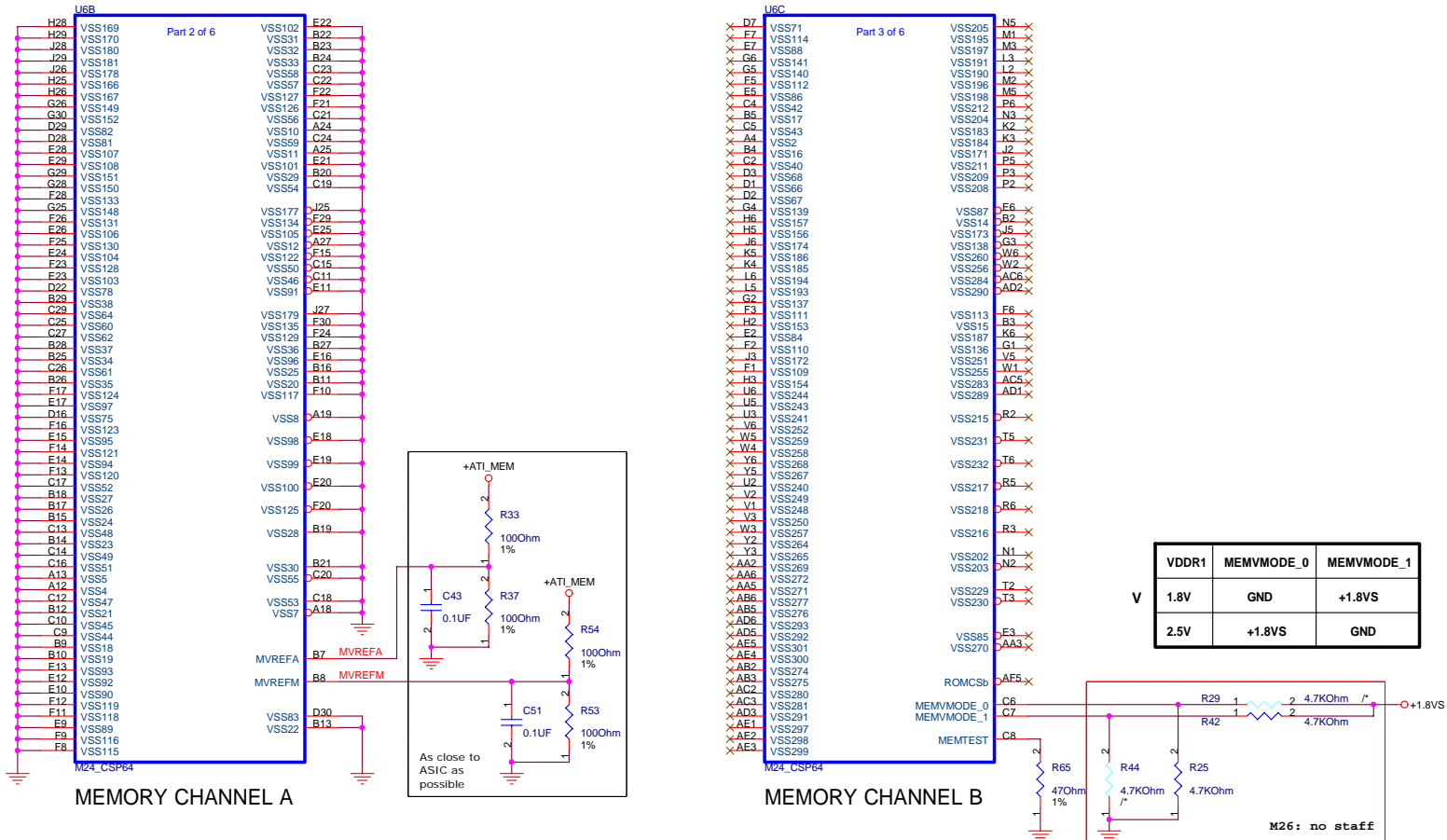
REVISION
2.1

DATE: Monday, January 17, 2005
SHEET 15 OF 63

DESCRIPTION: DDR2 Res

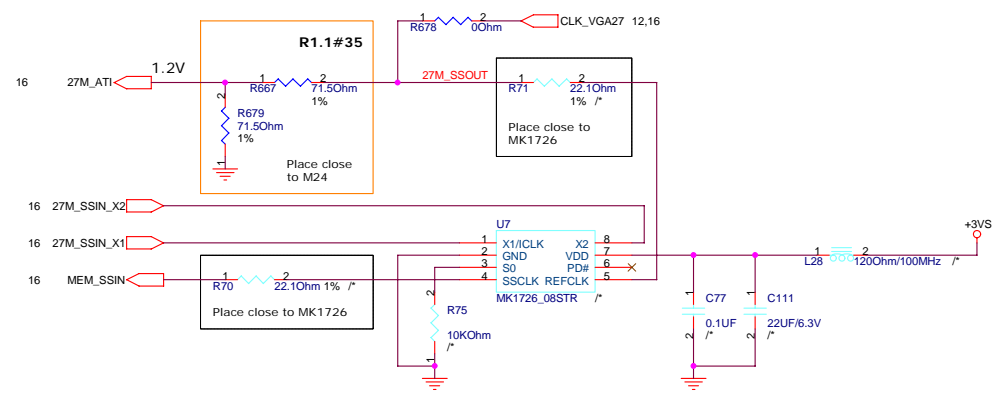
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RELEASE DATE:

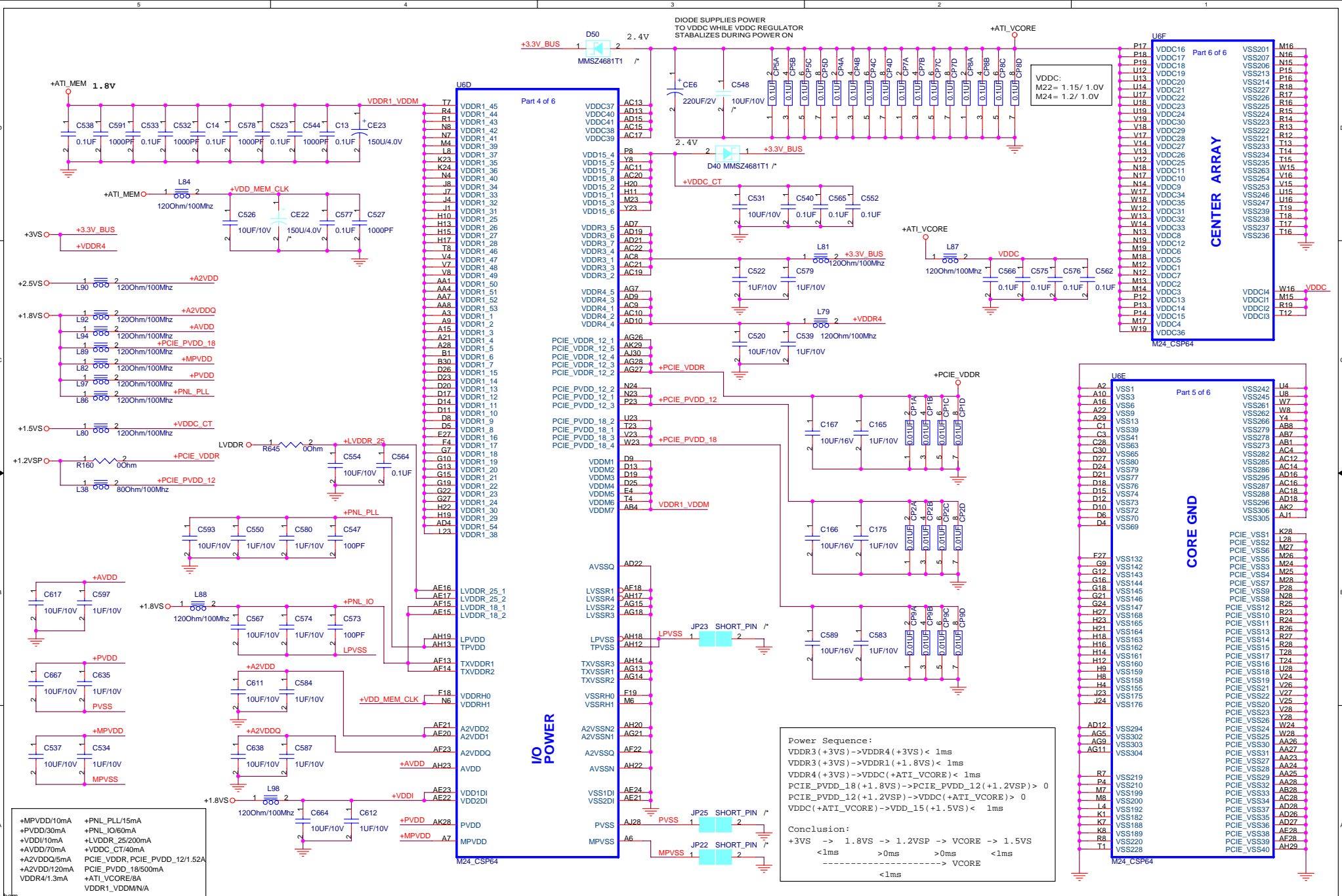
DESIGN ENGINEER: M.Y.



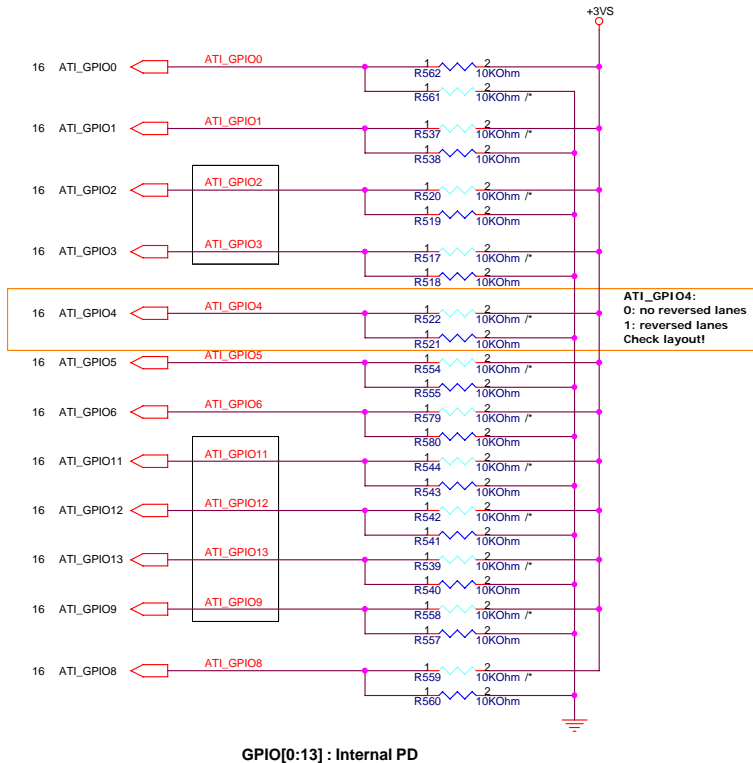
Memory Clock SS (Reserved)

S0 (Spread Percentage Select):
 GND: -1.8%
 VDD: -2.5% (default PU)
 NC : -0.6%



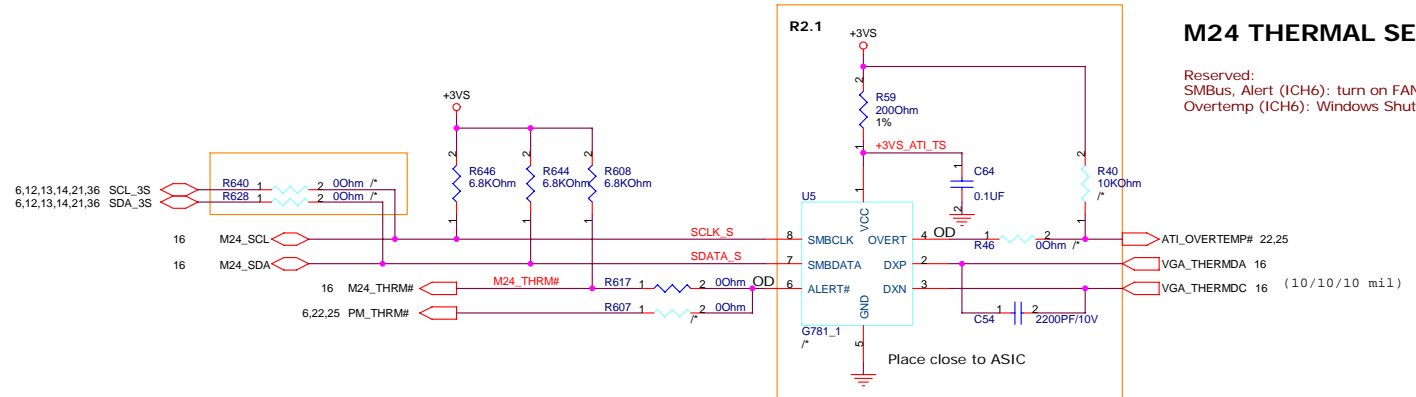


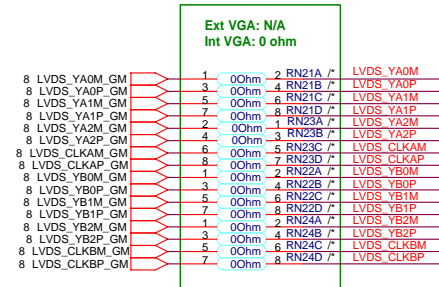
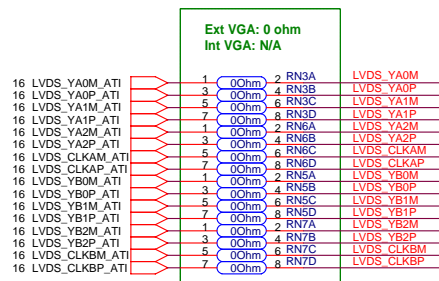
OPTION STRAPS



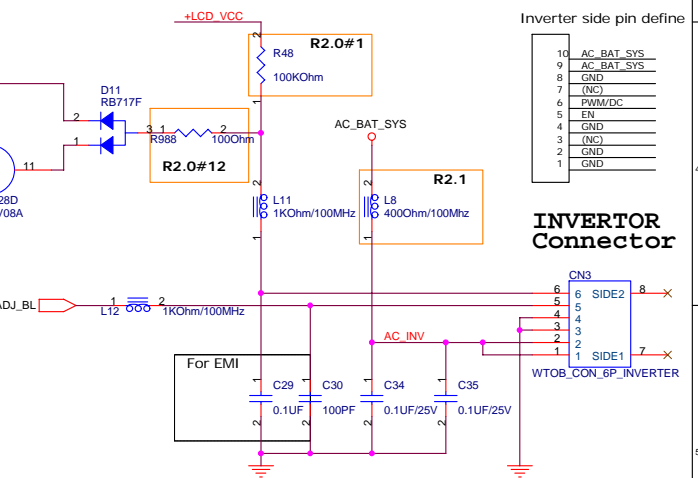
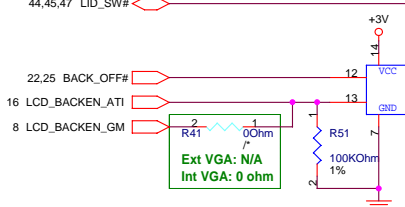
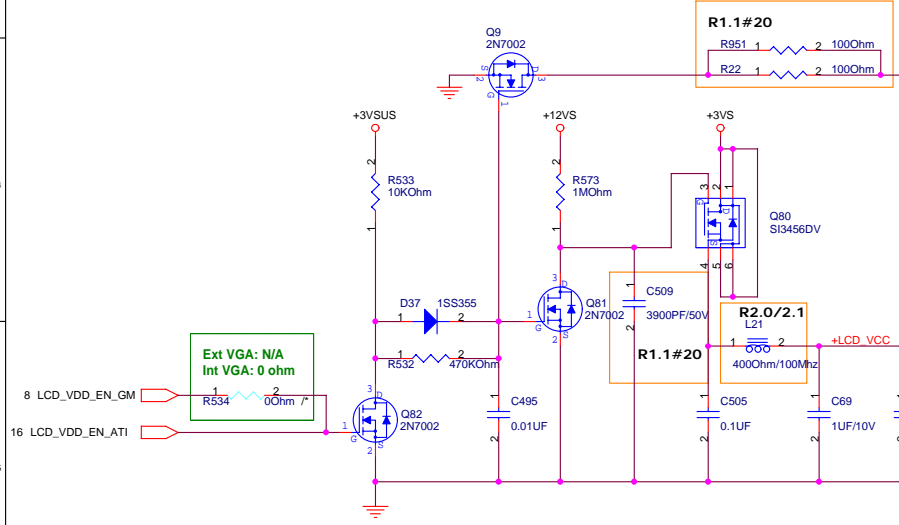
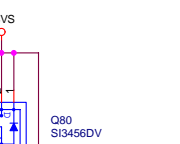
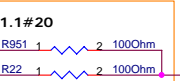
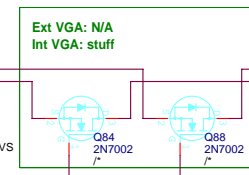
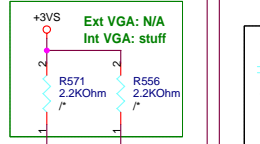
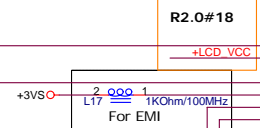
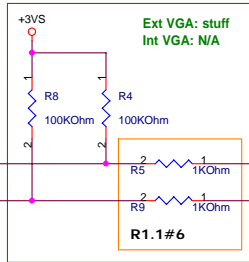
STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
B_PRX_IDLE_MODE (for A21) B_PTX_PDNB_MODE	PCIE_TEST	(For A21) PHY Receiver Idle Detector 0: Normal idle detector / 1: Alternate idle detector ATI internal use only. Other logic must not affect this signal during RESET	0
B_PTX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing for mobile mode 1: full Tx output swing (recommended) Must have an external 10K pullup to 3.3V	0
B_PTX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disable for mobile mode 1: Tx de_emphasis enable	0
PCIE_MODE(1:0)	GPIO(3:2)	00: PCI Express 1.0A mode 01: Kyrene-compatible mode 10: PCI Express 1.0 mode 11: PCI Express 1.0A mode and short-circuit internal loopback mode (Rx connected directly to Tx of PHY)	00
B_PTX_IEXT (For M24 A21/M22 A11)	GPIO4	0: normal mode 1: extra current in Tx output stage	0
REVERSE LANES (For M24A23/M22 A13)		0: non-reversed lanes layout 1: reversed lanes layout	0
FORCE_COMPLIANCE	GPIO5	Force chip to go to compliance state quickly for test purposes	0
B_PPLL_BW (For M24 A21/M22 A11)	GPIO6	0: Full PLL Bandwidth 1: Reduced PLL Bandwidth (ATI internal use only. Other logic must not affect this during RESET.)	0
CM_RANGE (For M24A23/M22 A13)		0: normal common-mode range 1: extended common-mode range	0
DEBUG_ACCESS	GPIO8	Controls whether ROM bytes 77-76 are used as SUBSYS_VEN_ID strap or DEBUG_PORT_MUX_SELECT strap.	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDis. If ROM attached identifies ROM type 00x - No ROM, CHG_ID=0 01x - No ROM, CHG_ID=1 1000 - Parallel ROM, chip IDis from ROM 1001 - 1M Serial AT25F1024 ROM (Atmel) 1010 - 1M Serial AT45DB011 ROM (Atmel) 1011 - 1M Serial M25P10 ROM (ST) 1100 - 512K Serial M25P05 ROM (ST) 1101 - 1M Serial SST45LF010 (SST), W45B512 (Winbond), 512K W45B012 (Winbond) 1110 - 1M Serial SST25VF010 (SST), 512K SST25VF512 (SST) 1111 - 1M Serial NX25F011B (NextFlash)	0000 (internal PD)
VIP_DEVICE	DVPPDATA_20	0: Slave VIP host port device present 1: No slave VIP host port device	(internal PD)
PKGTYP(4:0)	DVPPDATA(15:11)	ATI internal use only Identifies package/memory combinations	

M26: GPIO11 is memory aperture size (0=128M, 1=256M)

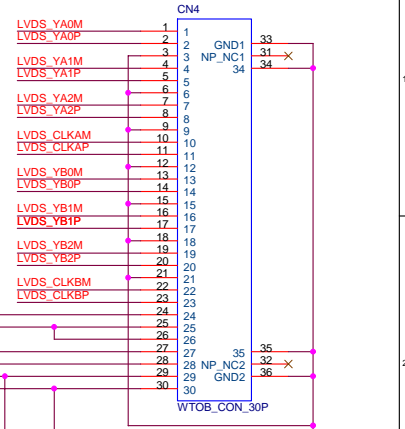




LCD CABLE ID	PID1	PID0
14" WXGA (AU/SS/CMO/CPT)	0	0



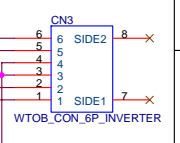
LVDS Connector

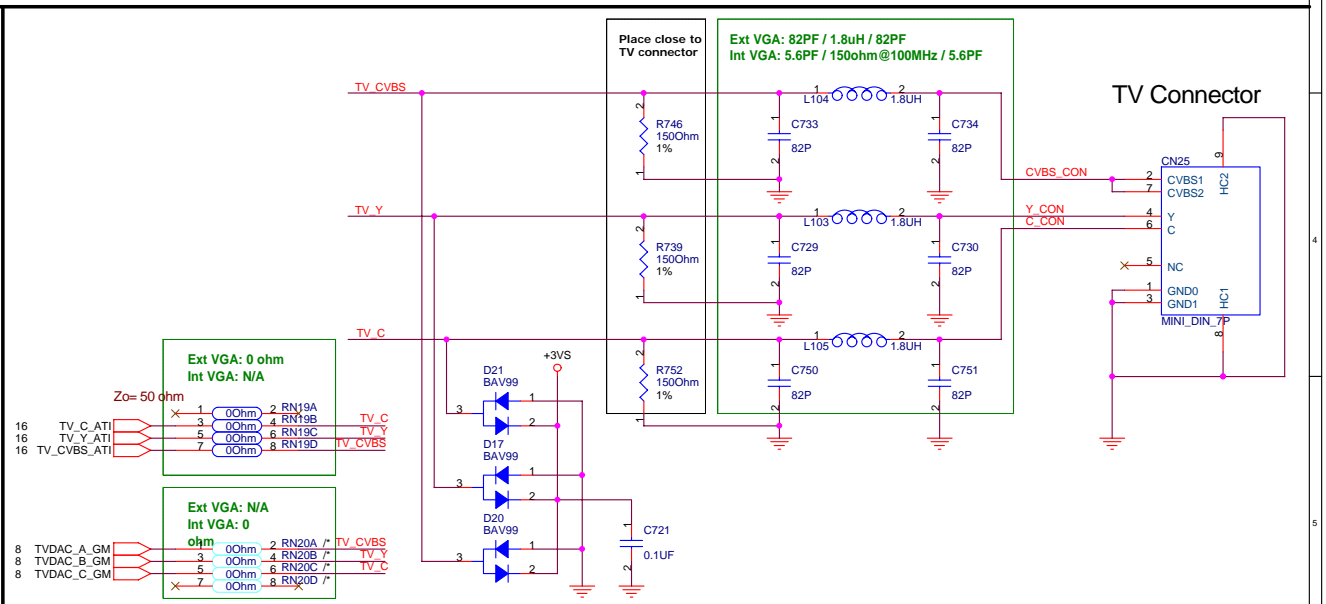
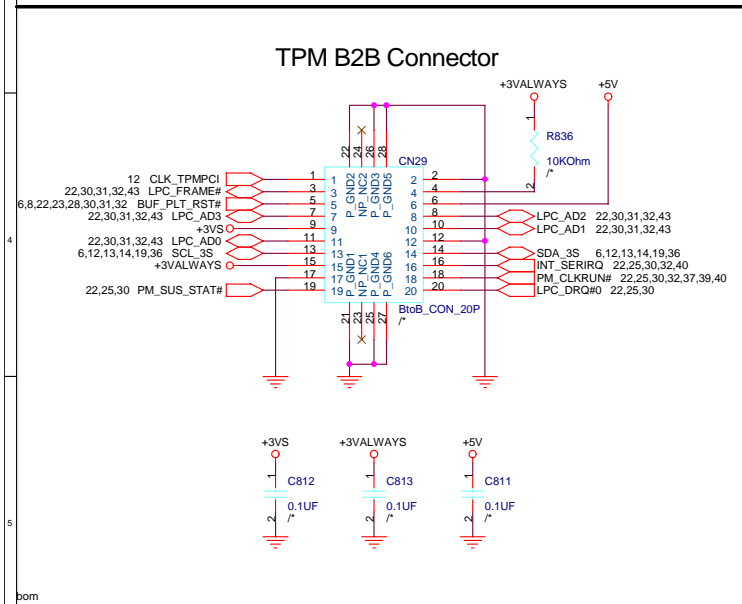
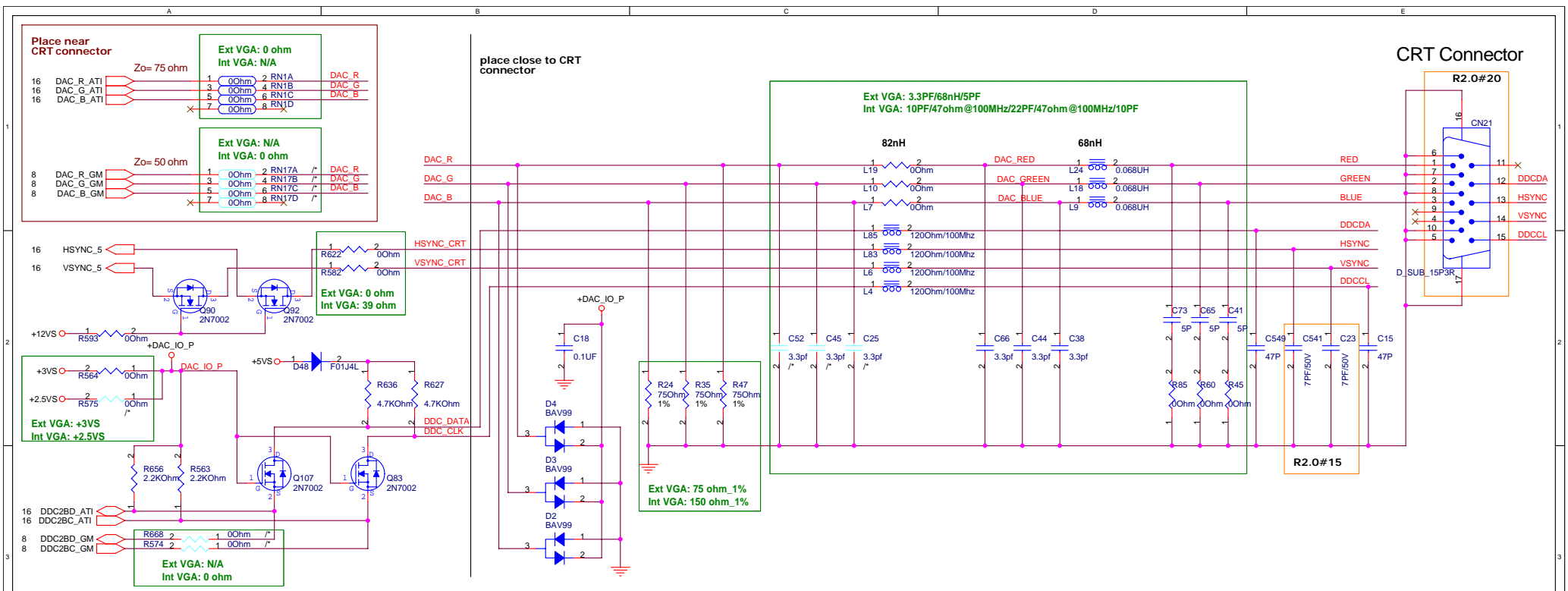


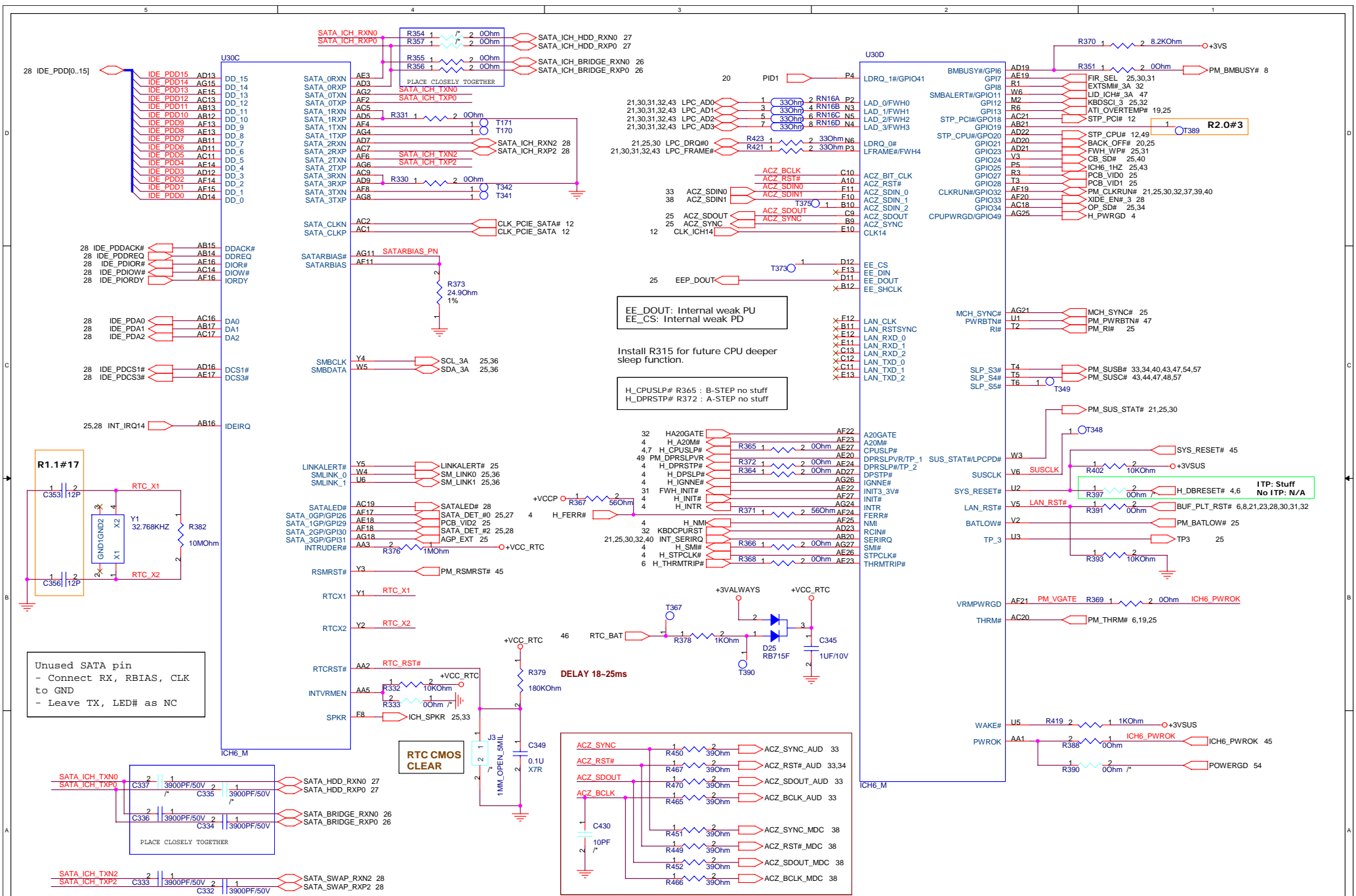
Inverter side pin define

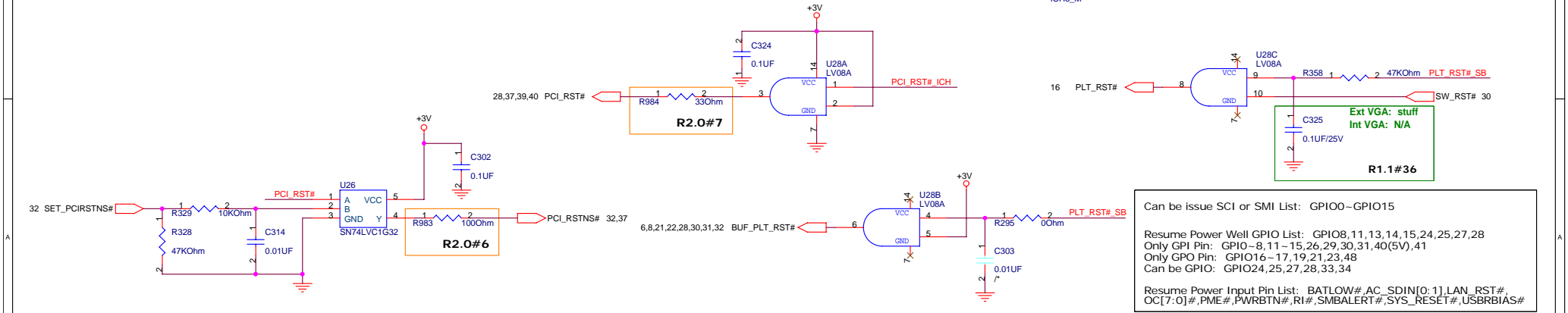
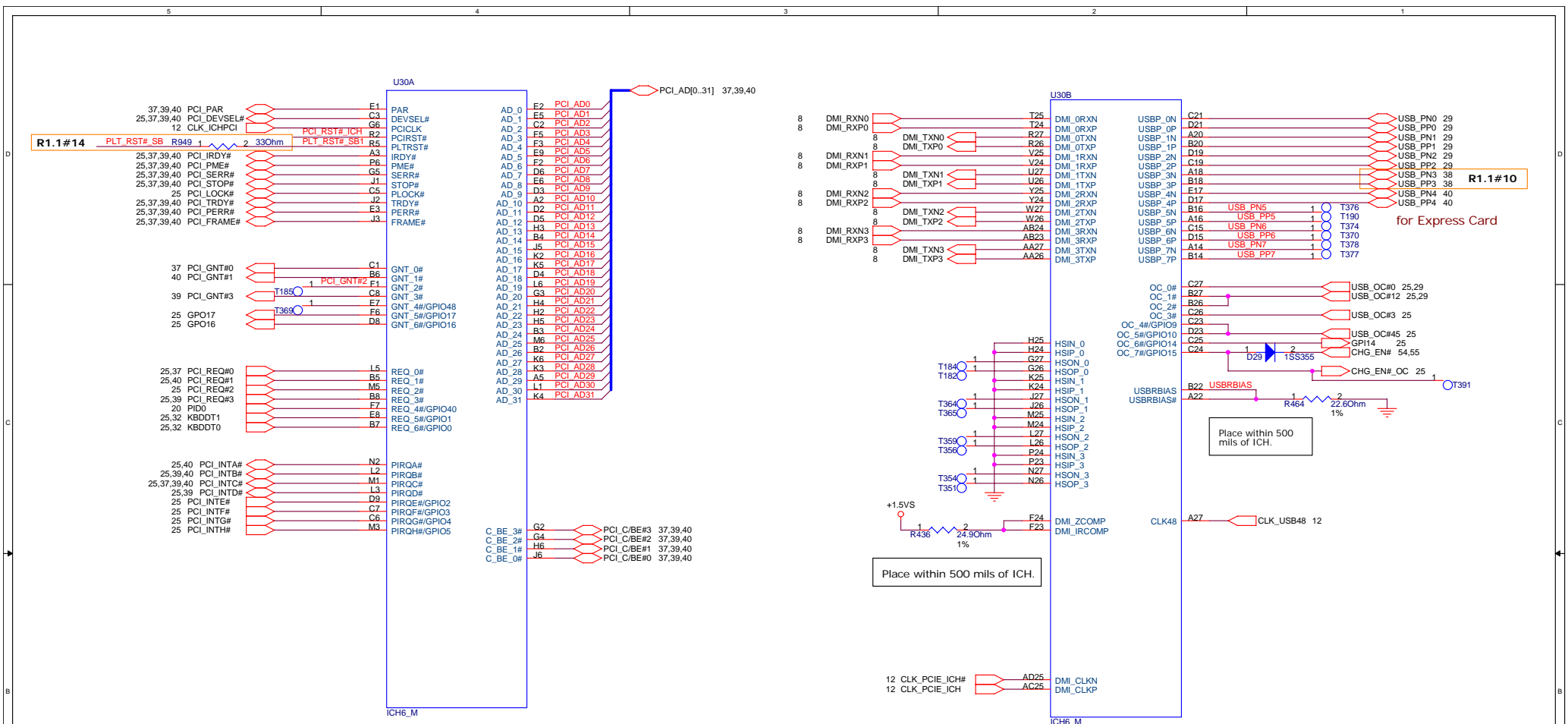
10	AC_BAT_SYS
9	AC_BAT_SYS
8	GND
7	(NC)
6	PWM/DC
5	EN
4	GND
3	(NC)
2	GND
1	GND

INVERTOR Connector

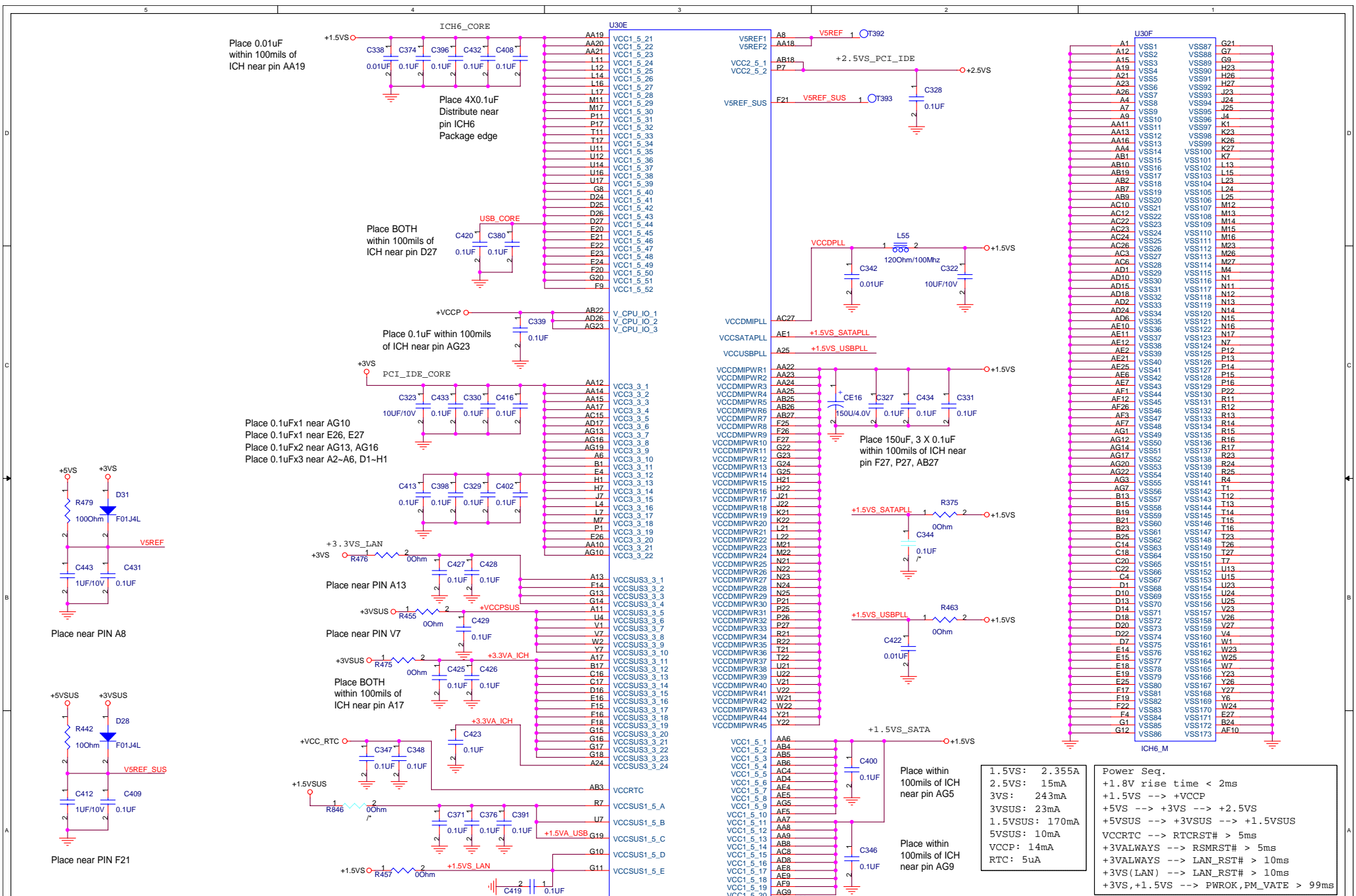




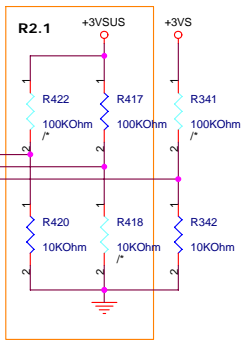
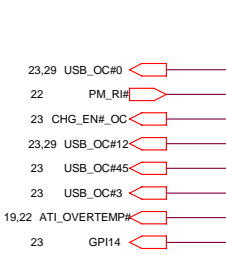
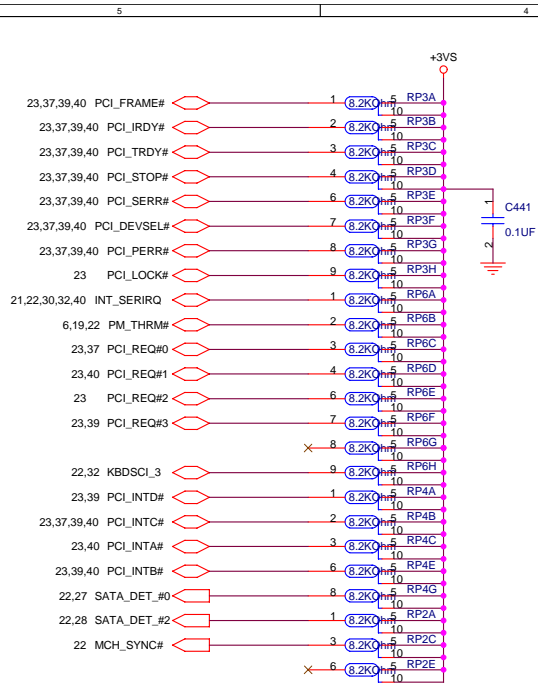




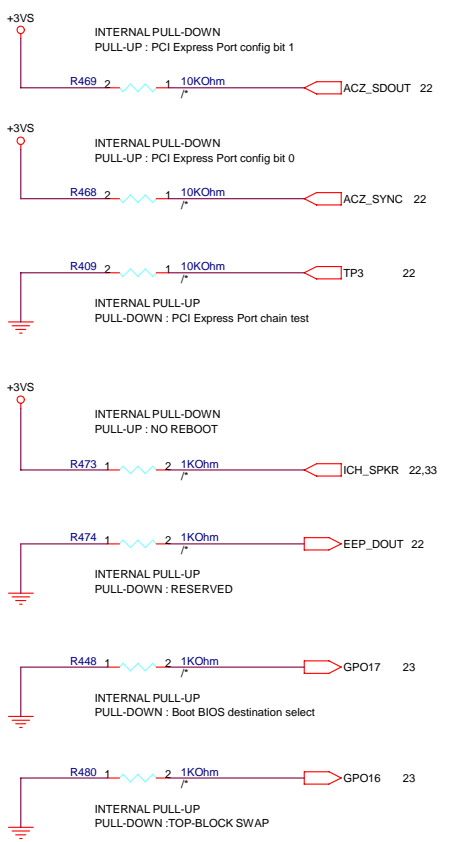
Can be issue SCI or SMI List: GPIO0-GPIO15
 Resume Power Well GPIO List: GPIO8,11,13,14,15,24,25,27,28
 Only GPI Pin: GPIO-8,11-15,26,29,30,31,40(5V),41
 Only GPO Pin: GPIO16-17,19,21,23,48
 Can be GPIO: GPIO24,25,27,28,33,34
 Resume Power Input Pin List: BATLOW#,AC_SDINIO:1,LAN_RST#,OC[7:0]#,PME#,PWRBTN#,RI#,SMBALERT#,SYS_RESET#,USBRBIAS#



1.5VS: 2.355A	Power Seq.
2.5VS: 15mA	+1.8V rise time < 2ms
3VS: 243mA	+1.5VS --> +VCCP
3VSUS: 23mA	+5VS --> +3VS --> +2.5VS
1.5VSUS: 170mA	+5VSUS --> +3VSUS --> +1.5VSUS
5VSUS: 10mA	VCCRTC --> RTCRST# > 5ms
VCCP: 14mA	+3VALWAYS --> RSMRST# > 5ms
RTC: 5uA	+3VALWAYS --> LAN_RST# > 10ms
	+3VS(LAN) --> LAN_RST# > 10ms
	+3VS, +1.5VS --> PWR0K, PM_VATE > 99ms

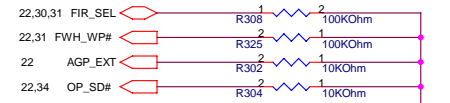
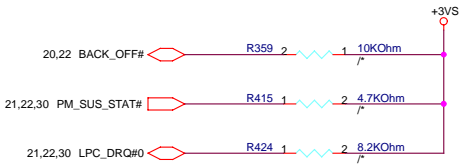
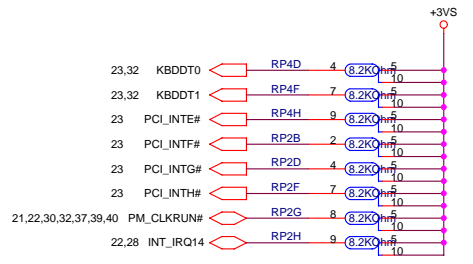
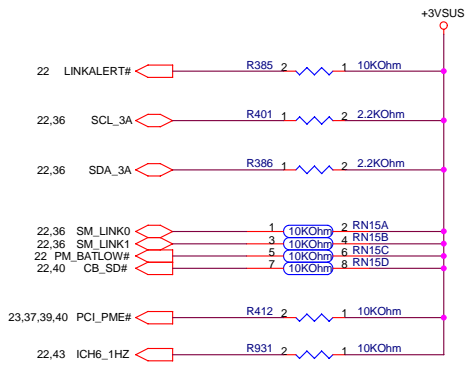


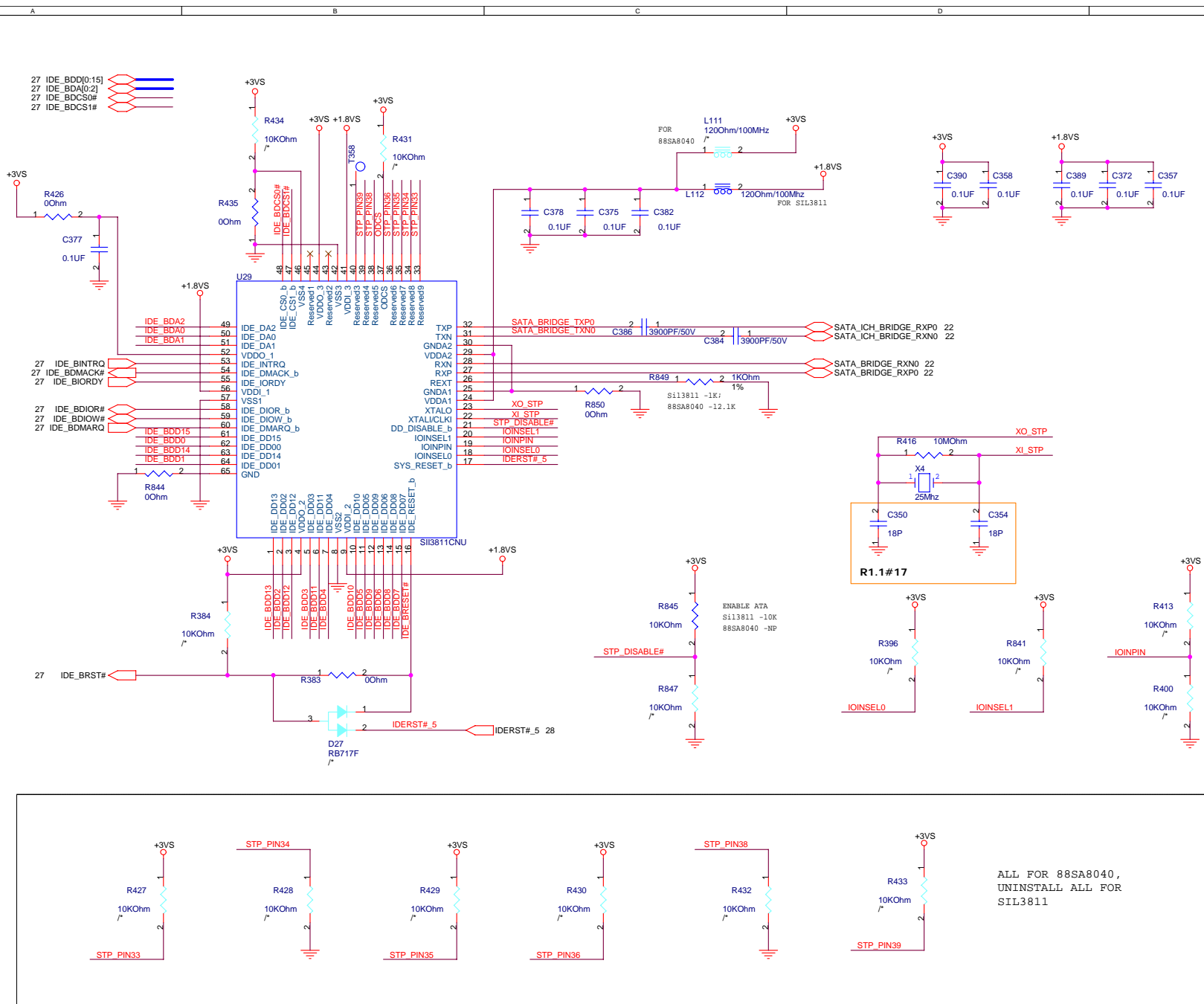
	PCB_VID2	PCB_VID1	PCB_VID0
MB R1.0	0	0	0
MB R1.1	0	0	0
MB R2.0	0	0	1
MB R2.1	0	1	0

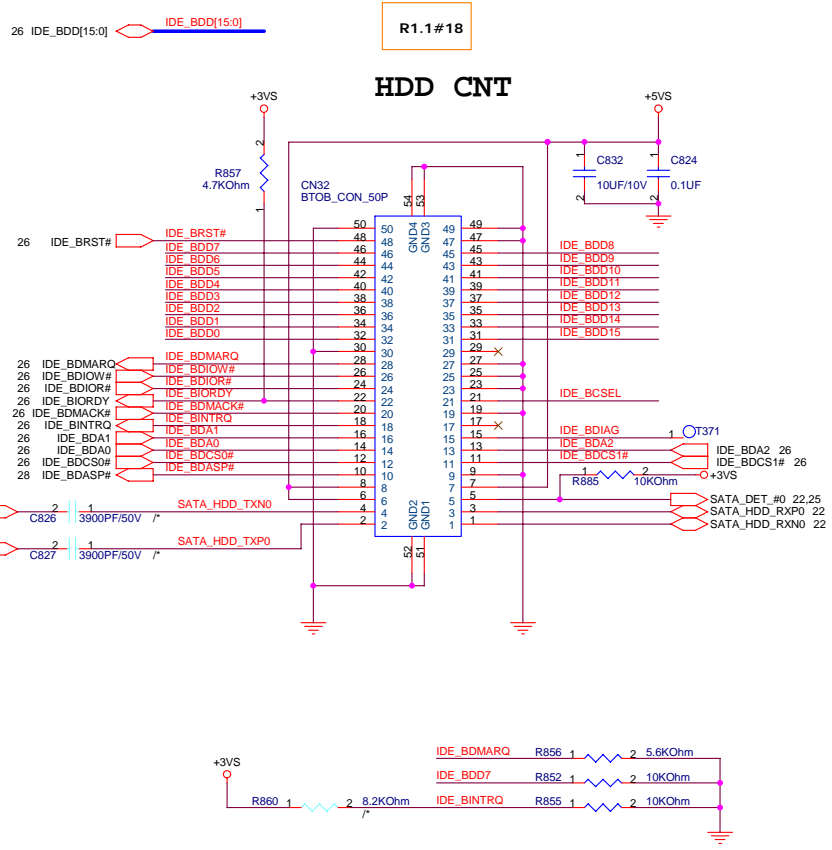


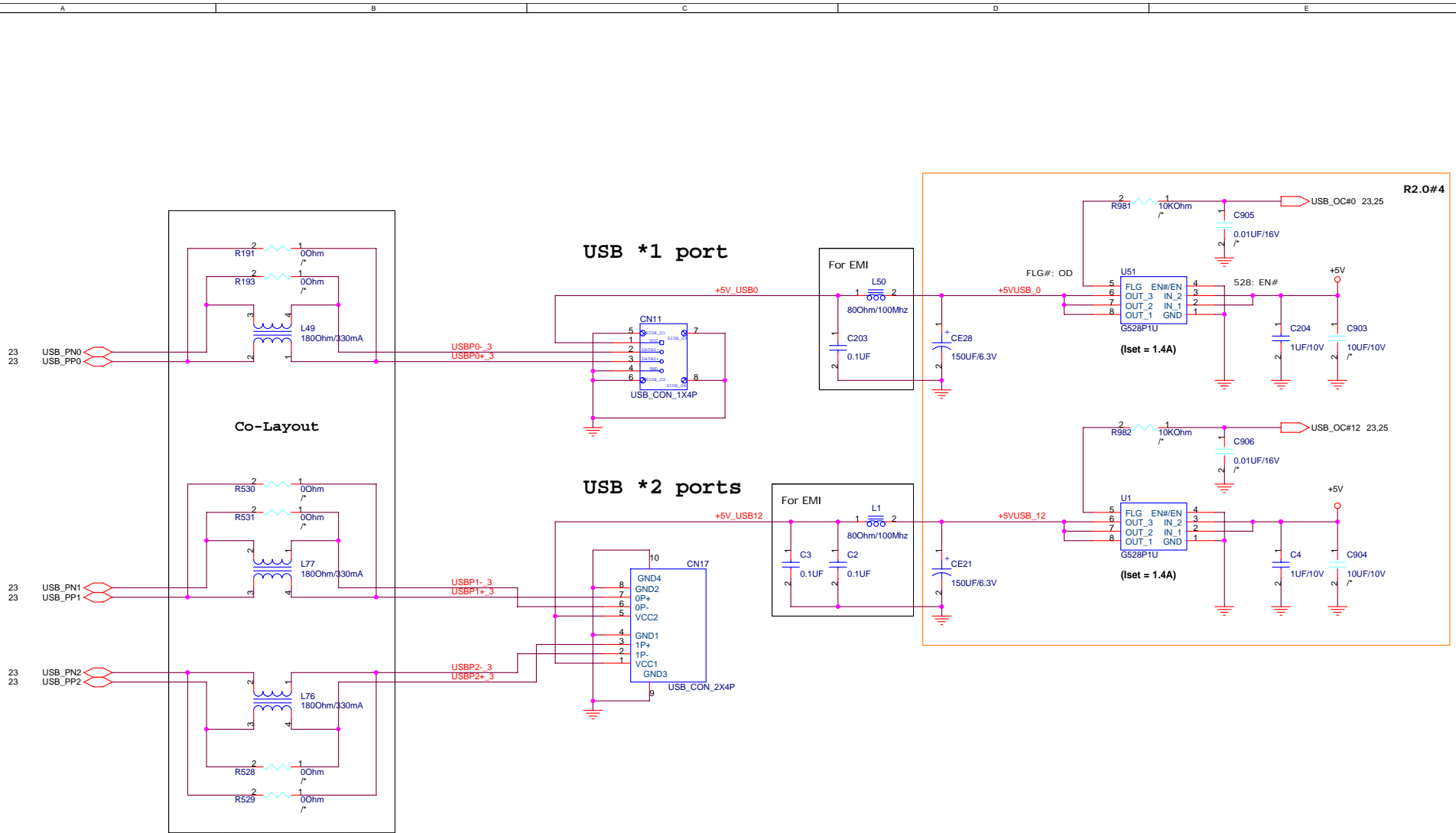
INTERNAL PULL-DOWN SIGNALS :
 AC_BITCLK, AC_RST#, AC_SDIN[2:0], AC_SDOUT, AC_SYNC, DPSPVP, LAN_CLK, PDD[7], PDDREQ, SPKR, USB[7:0][P.N]

INTERNAL PULL-UP SIGNALS :
 EE_DIN, EE_DOUT, EE_CS, GPIO[17:16], LAD[3:0]#, LDRQ[0:1], LAN_RXD[2:0], PME#, PWRTN#, TP3, SATALED#, GNT[4:0]







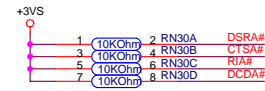
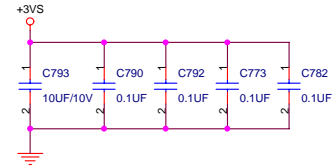


R2.0#4

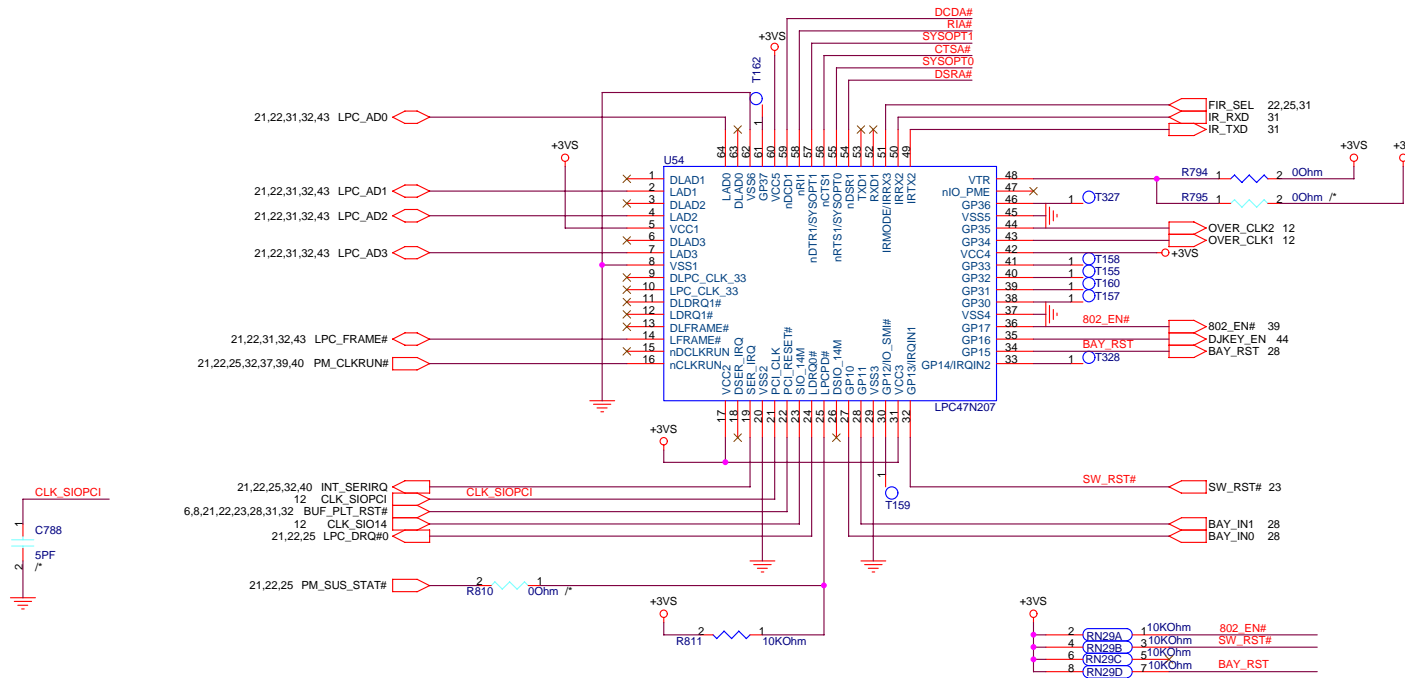
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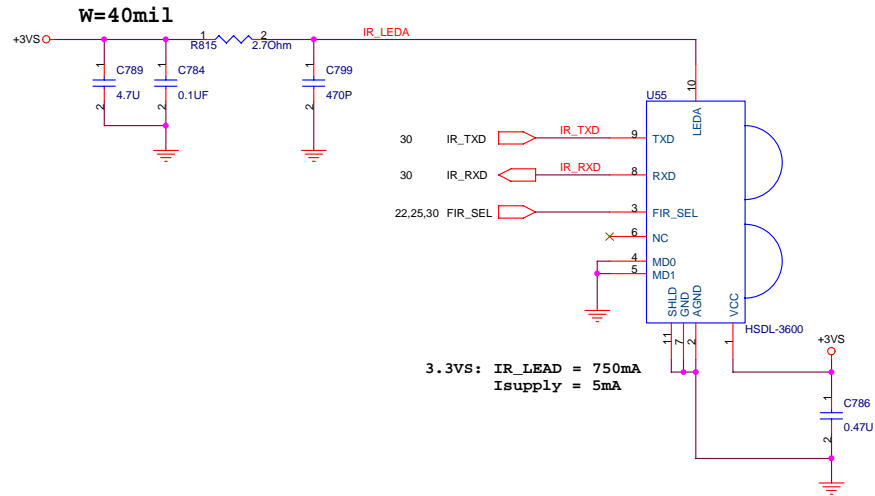
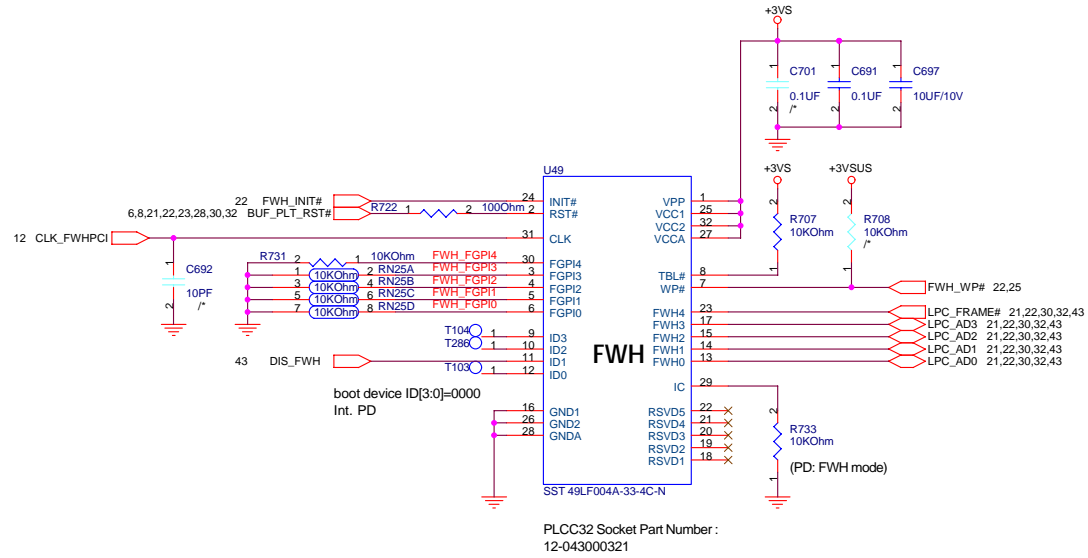
SYSOPT0=0, SYSOPT1=0 --> 0x002e
SYSOPT0=1, SYSOPT1=0 --> 0x004e
SYSOPT0=0, SYSOPT1=1 --> 0x162e
SYSOPT0=1, SYSOPT1=1 --> 0x164e

```



Super I/O





PROJECT: W3V

REVISION
2.1

DATE: Monday, January 17, 2005
SHEET 31 OF 63

DESCRIPTION:
FIR & FWH

SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :

DESIGN ENGINEER :
Alice Shih

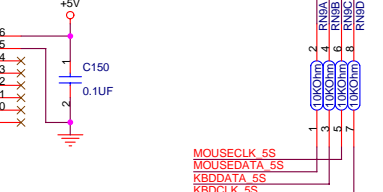
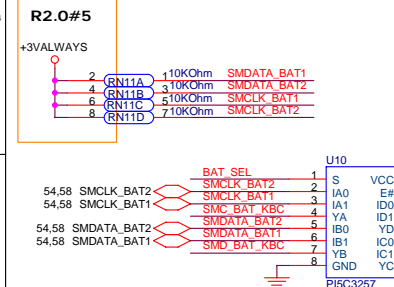
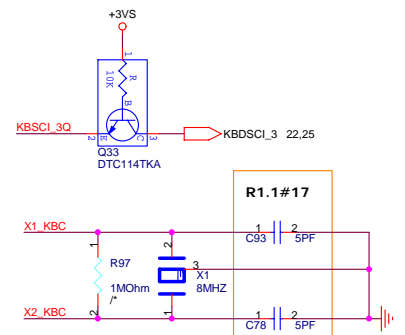
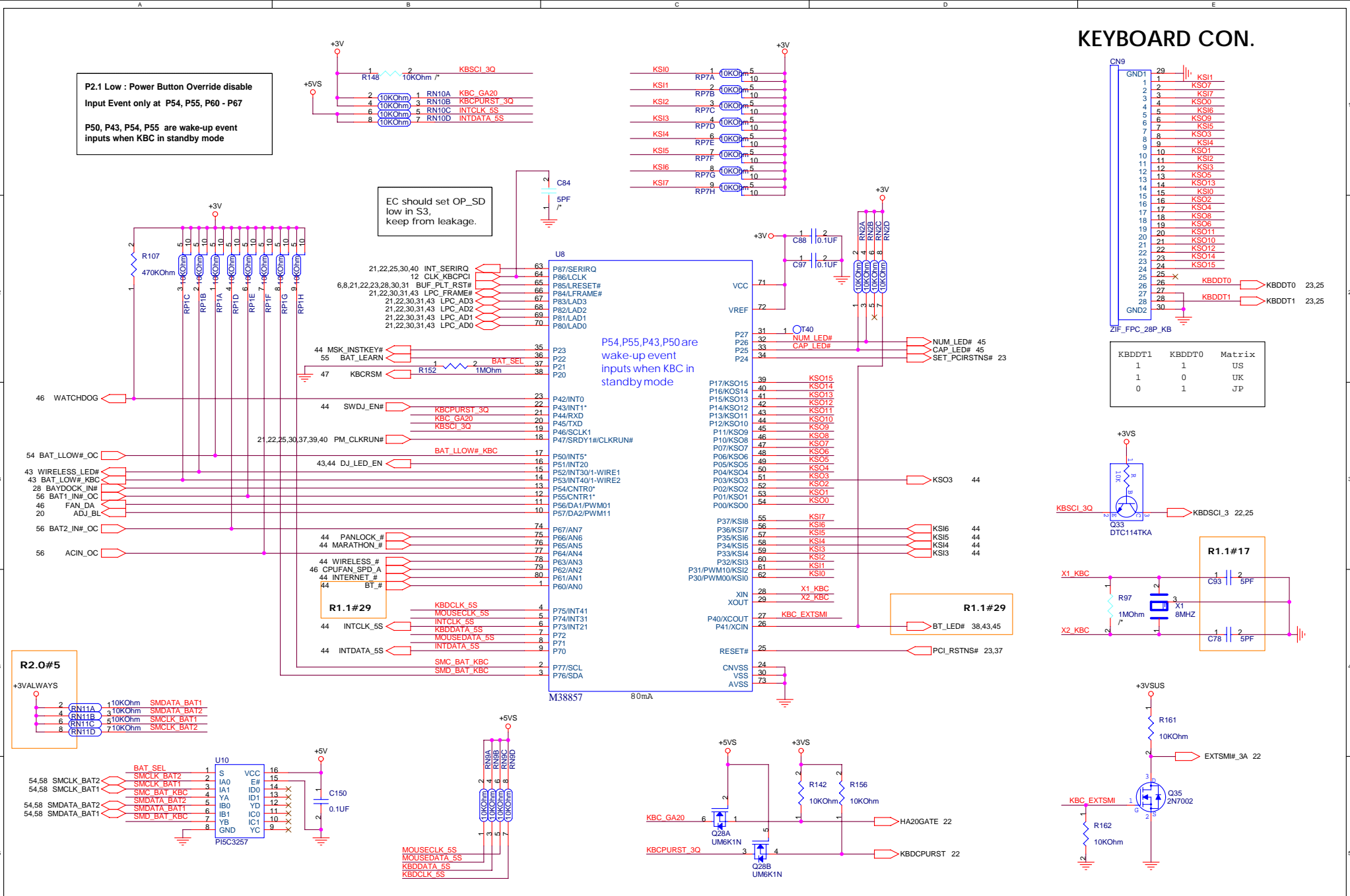
KEYBOARD CON.

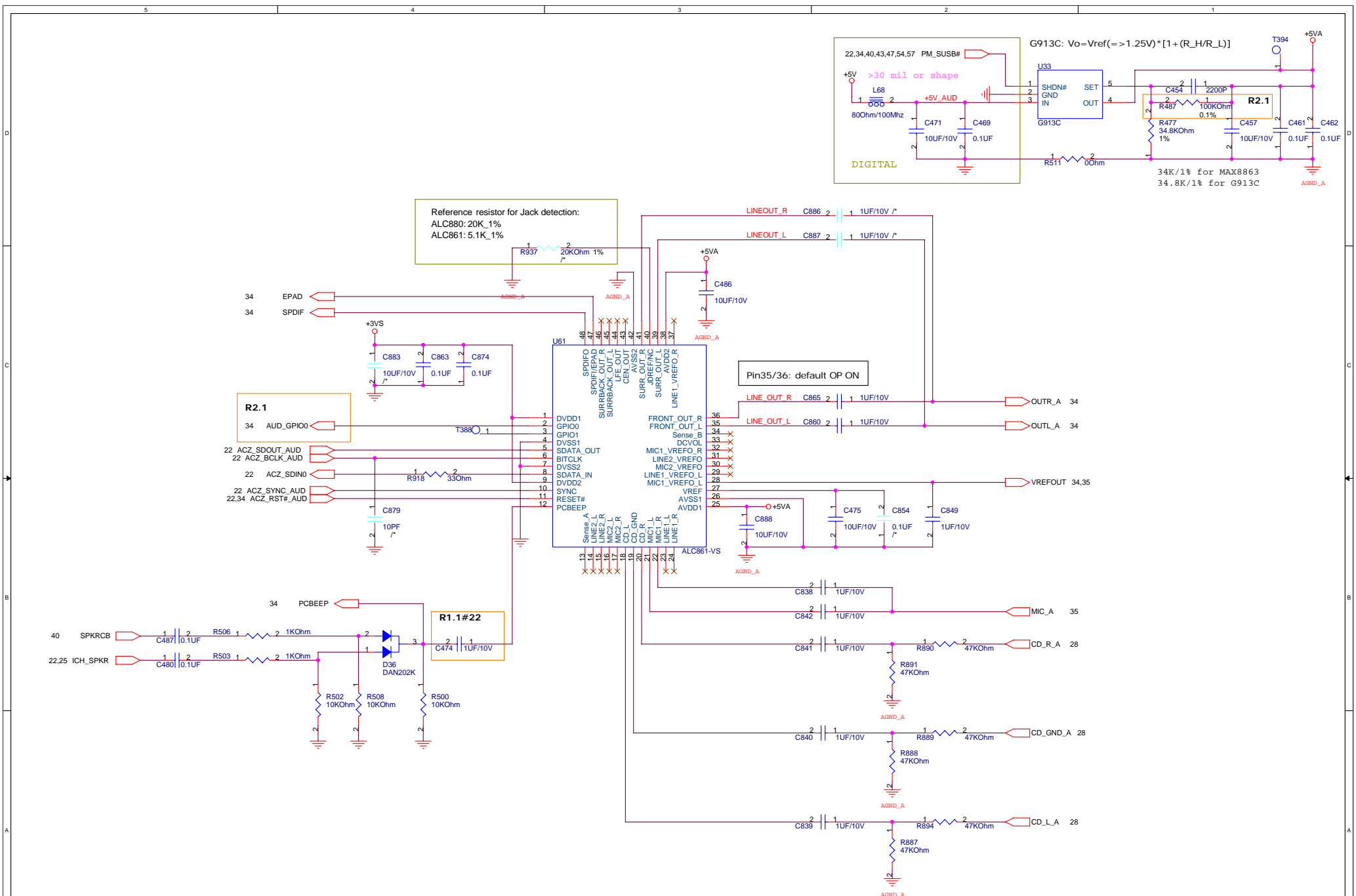
P2.1 Low : Power Button Override disable
Input Event only at P54, P55, P60 - P67
P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode

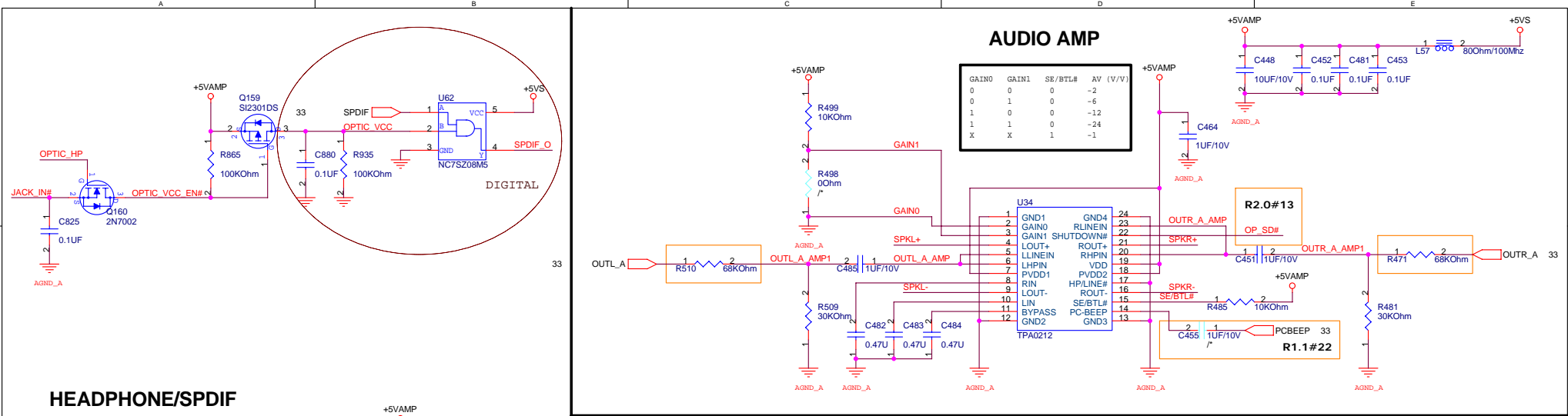
EC should set OP_SD low in S3, keep from leakage.

P54, P55, P43, P50 are wake-up event inputs when KBC in standby mode

KBDDT1	KBDDT0	Matrix
1	1	US
1	0	UK
0	1	JP

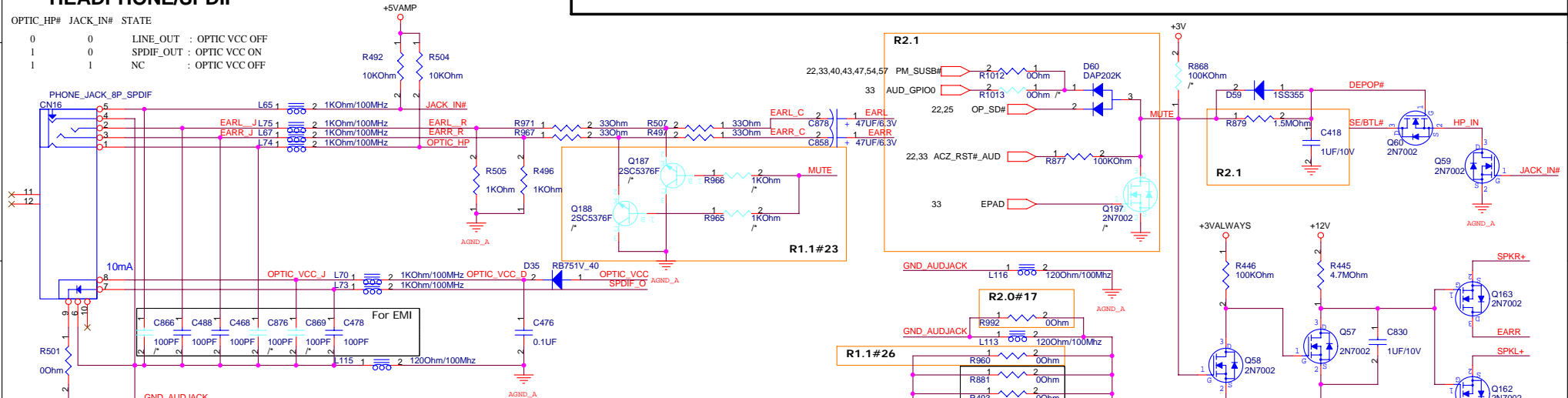




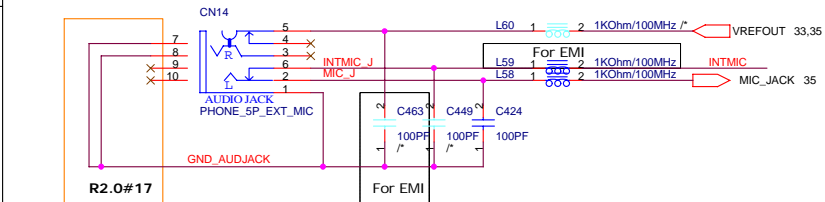


HEADPHONE/SPDIF

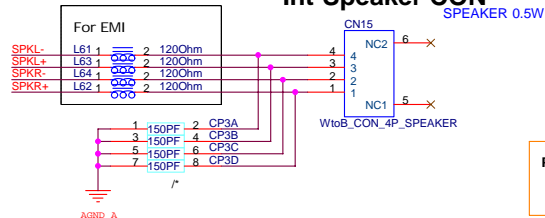
OPTIC_HP#	JACK_IN#	STATE
0	0	LINE_OUT : OPTIC VCC OFF
1	0	SPDIF_OUT : OPTIC VCC ON
1	1	NC : OPTIC VCC OFF



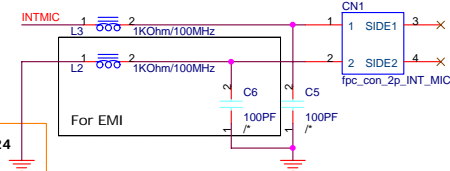
Ext MIC CON

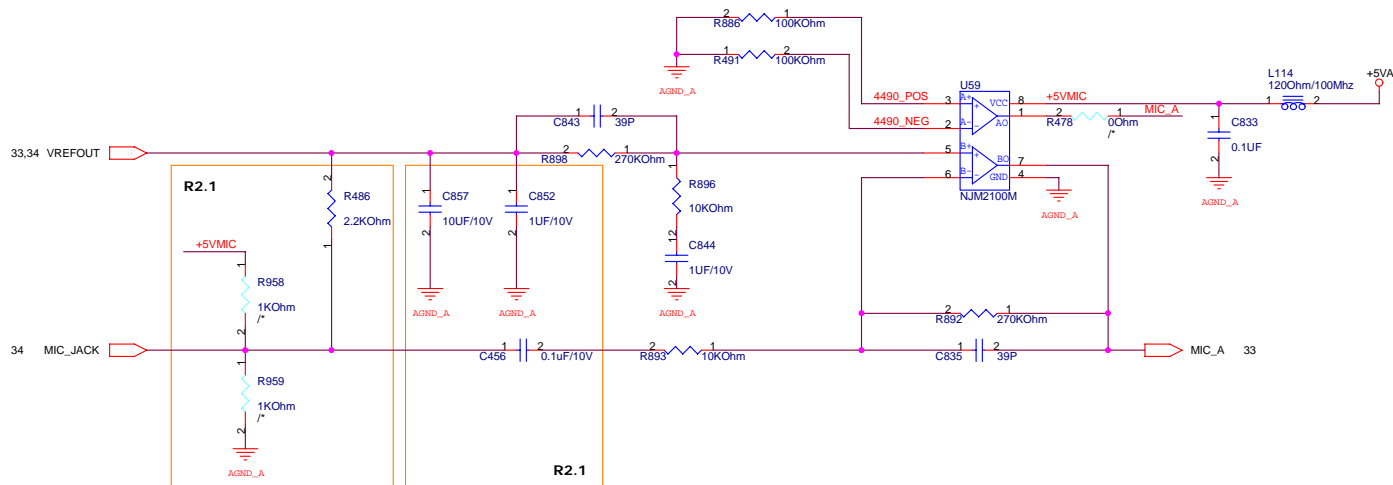
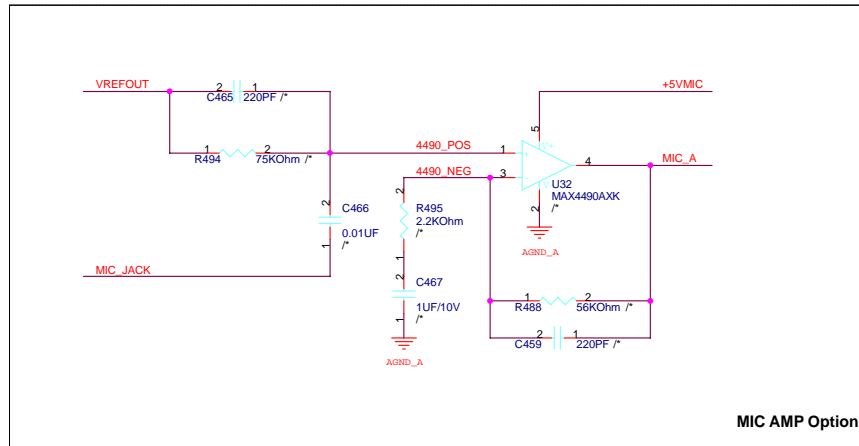


Int Speaker CON



Int MIC CON





PROJECT: W3V

REVISION
2.1

DATE: Monday, January 17, 2005
SHEET 35 OF 63

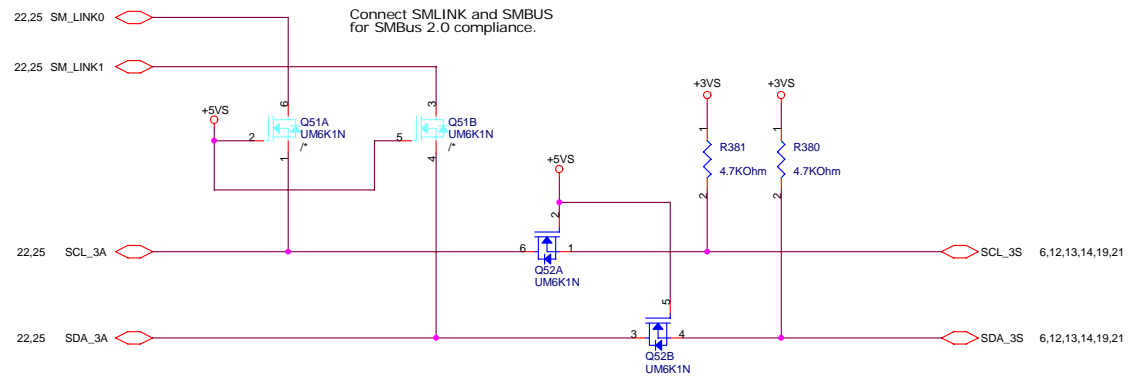
DESCRIPTION: MIC AMP

SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :

DESIGN ENGINEER : Alice Shih

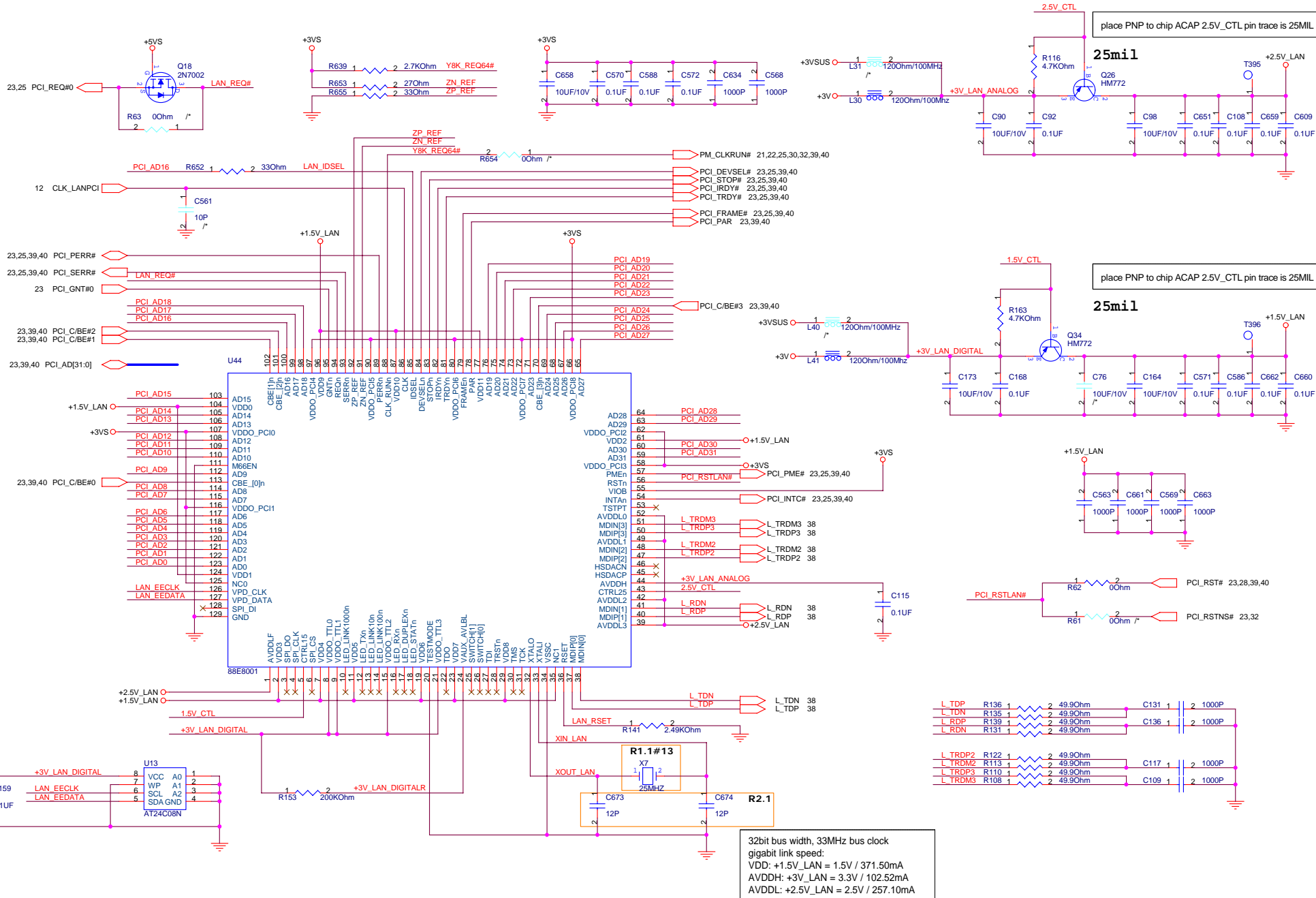
ICH6-M

ICH6-M



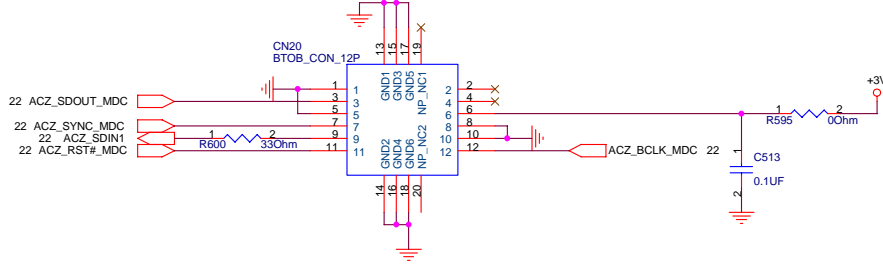
System Thermal Sensor
ATI Thermal Sensor
Clock Generator
DDR2 SO-DIMM
TPM

- +3VALWAYS ○ ○ +3VALWAYS 21,22,32,34,43,44,45,47,48,50,51,57
- +3VSUS ○ ○ +3VSUS 20,22,24,25,31,32,37,45,47,53,57
- +5VALWAYS ○ ○ +5VALWAYS 48,51,53
- +5VSUS ○ ○ +5VSUS 24,57
- +1.5VSUS ○ ○ +1.5VSUS 24,53
- +3V ○ ○ +3V 20,23,30,32,34,37,38,39,40,41,42,43,44,47,48,53,57
- +5V ○ ○ +5V 13,21,29,32,33,41,43,44,45,48,52,56,57
- +12V ○ ○ +12V 34,42,57
- +3VS ○ ○ +3VS 6,10,12,13,14,16,17,18,19,20,21,22,24,25,26,27,28,30,31,32,33,37,38,39,40,43,45,47,48,49,52,53,54,57
- +5VS ○ ○ +5VS 21,24,27,28,32,34,37,39,43,45,46,48,57
- +12VS ○ ○ +12VS 20,21,28,44,57
- +VCORE ○ ○ +VCORE 5,6,49
- +VCCP ○ ○ +VCCP 4,5,6,7,10,12,22,24,48,53
- +1.2VSP ○ ○ +1.2VSP 18,52
- +2.5VS ○ ○ +2.5VS 6,8,10,11,18,20,21,24,48,51,52
- +1.8VS ○ ○ +1.8VS 4,16,17,18,26,48,52,53,57
- +0.9VS ○ ○ +0.9VS 15,53
- +1.5VS ○ ○ +1.5VS 4,8,10,18,23,24,48,51
- +VCC_RTC ○ ○ +VCC_RTC 22,24
- +1.8V ○ ○ +1.8V 8,10,11,13,14,40,51,53
- +VCC_GMCH_CORE ○ ○ +VCC_GMCH_CORE 8,10,11,53
- +VCCCB ○ ○ +VCCCB 40,41
- +VPPCB ○ ○ +VPPCB 41
- VTT_REF ○ ○ VTT_REF 8,13,14,15
- A/D_DOCK_IN ○ ○ A/D_DOCK_IN 46,55,56
- +ATI_VCORE ○ ○ +ATI_VCORE 18,52

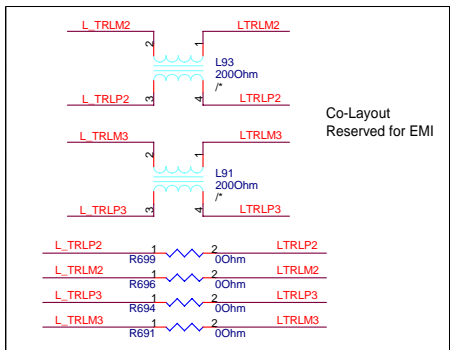
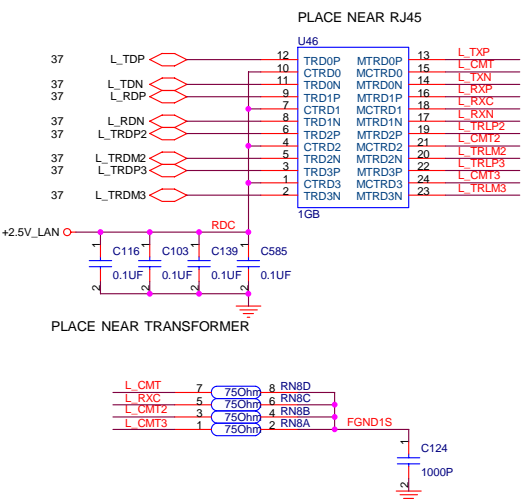
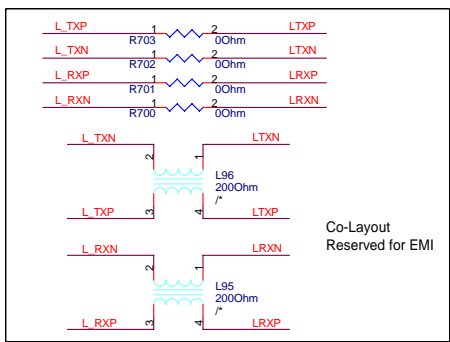
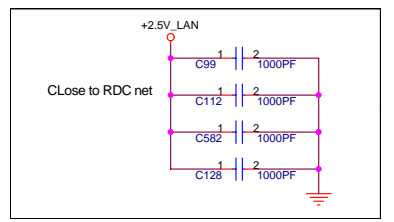
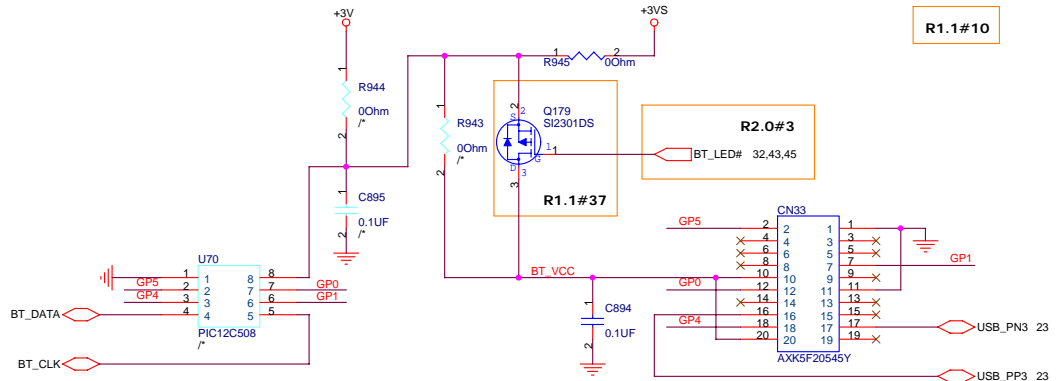


Azalia MDC MODEM

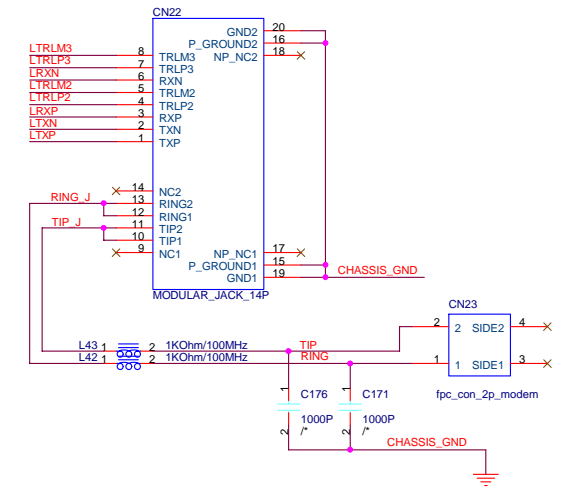
[ACZ_SDOUT/SYNC/BITCLK/RST#]:
 ICH6: 39 ohm to Audio / 39 ohm to MDC
 [ACZ_SDIN]:
 Audio 33 ohm to ICH6 / MDC 33 ohm to ICH6

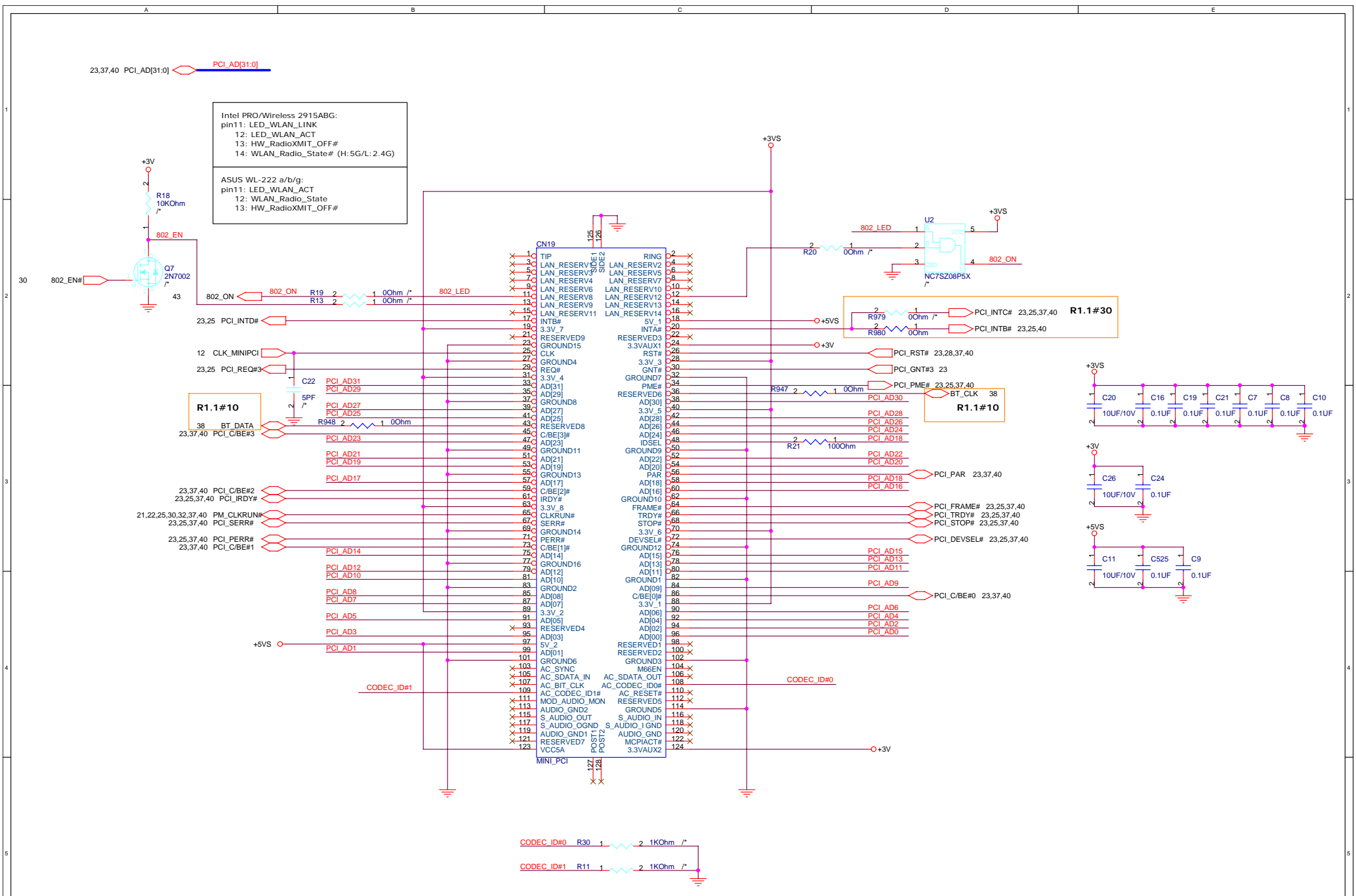


BT



RJ11+RJ45





Intel PRO/Wireless 2915ABG:
pin11: LED_WLAN_LINK
12: LED_WLAN_ACT
13: HW_RadioXMIT_OFF#
14: WLAN_Radio_State# (H:5G/L:2.4G)

ASUS WL-222 a/b/g:
pin11: LED_WLAN_ACT
12: WLAN_Radio_State
13: HW_RadioXMIT_OFF#

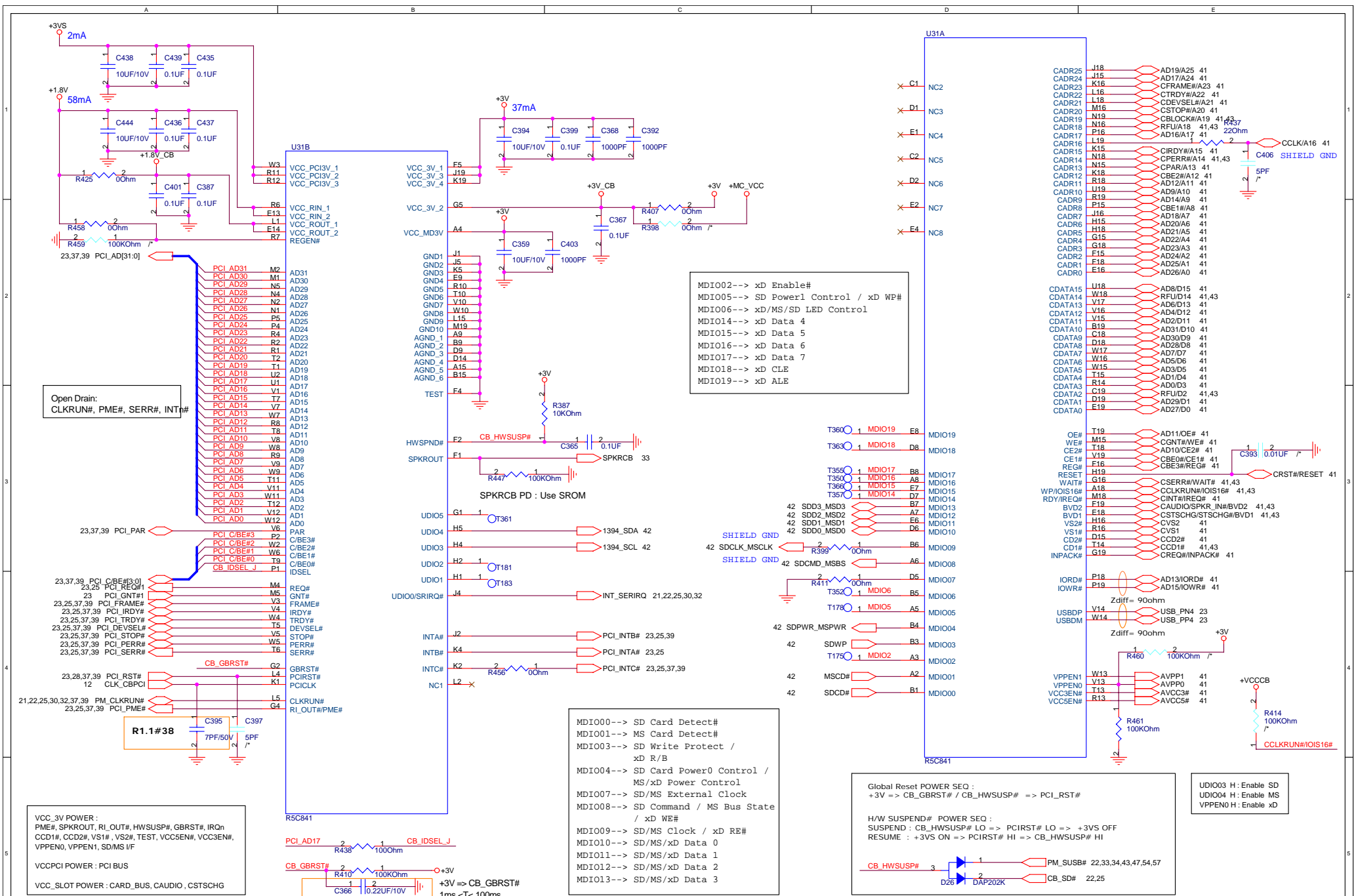
R1.1#10

R1.1#10

R1.1#30

CODEC_ID#0 R30 1 2 1KOhm /

CODEC_ID#1 R11 1 2 1KOhm /



Open Drain:
CLKRUN#, PME#, SERR#, INT#

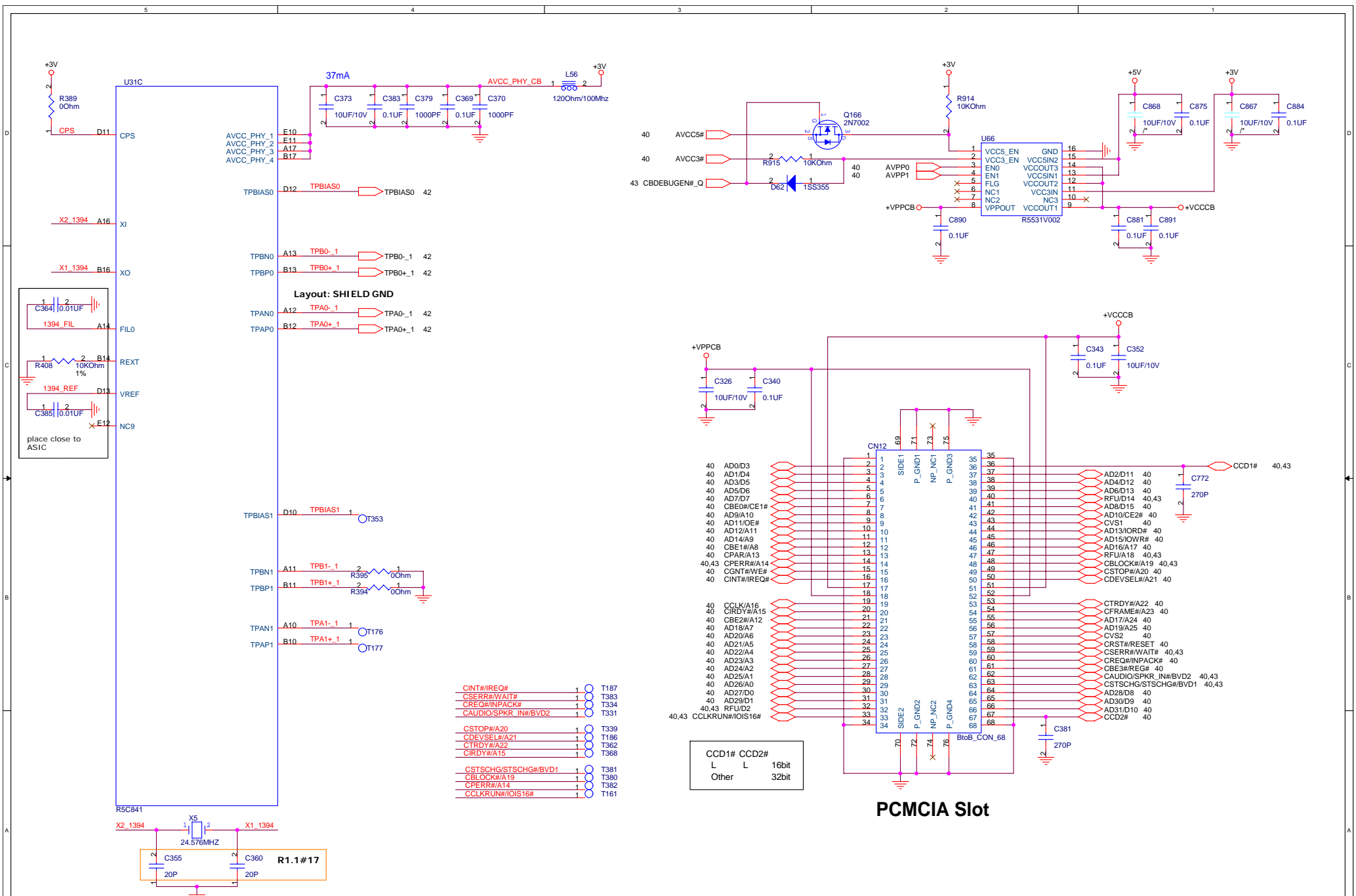
MDIO02--> xD Enable#
MDIO05--> SD Power1 Control / xD WP#
MDIO06--> xD/MS/SD LED Control
MDIO14--> xD Data 4
MDIO15--> xD Data 5
MDIO16--> xD Data 6
MDIO17--> xD Data 7
MDIO18--> xD CLE
MDIO19--> xD ALE

MDIO00--> SD Card Detect#
MDIO01--> MS Card Detect#
MDIO03--> SD Write Protect /
xD R/B
MDIO04--> SD Card Power0 Control /
MS/xD Power Control
MDIO07--> SD/MS External Clock
MDIO08--> SD Command / MS Bus State
/ xD WE#
MDIO09--> SD/MS Clock / xD RE#
MDIO10--> SD/MS/xD Data 0
MDIO11--> SD/MS/xD Data 1
MDIO12--> SD/MS/xD Data 2
MDIO13--> SD/MS/xD Data 3

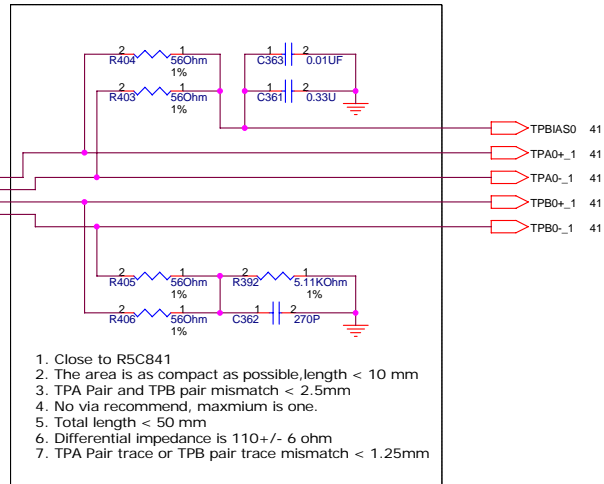
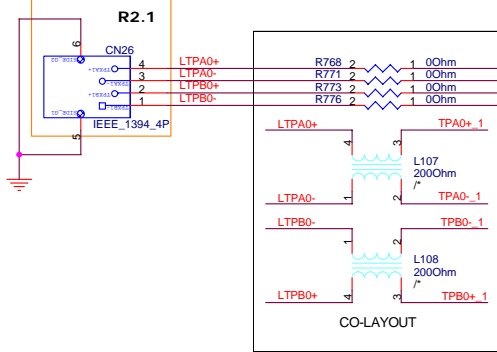
Global Reset POWER SEQ :
+3V => CB_GBRST# / CB_HWSUSP# => PCI_RST#

H/W SUSPEND# POWER SEQ :
SUSPEND : CB_HWSUSP# LO => PCIRST# LO => +3VS OFF
RESUME : +3VS ON => PCIRST# HI => CB_HWSUSP# HI

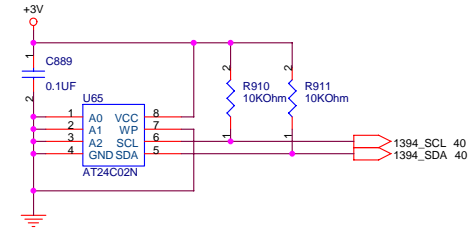
UDIO03 H : Enable SD
UDIO04 H : Enable MS
VPPEN0 H : Enable xD



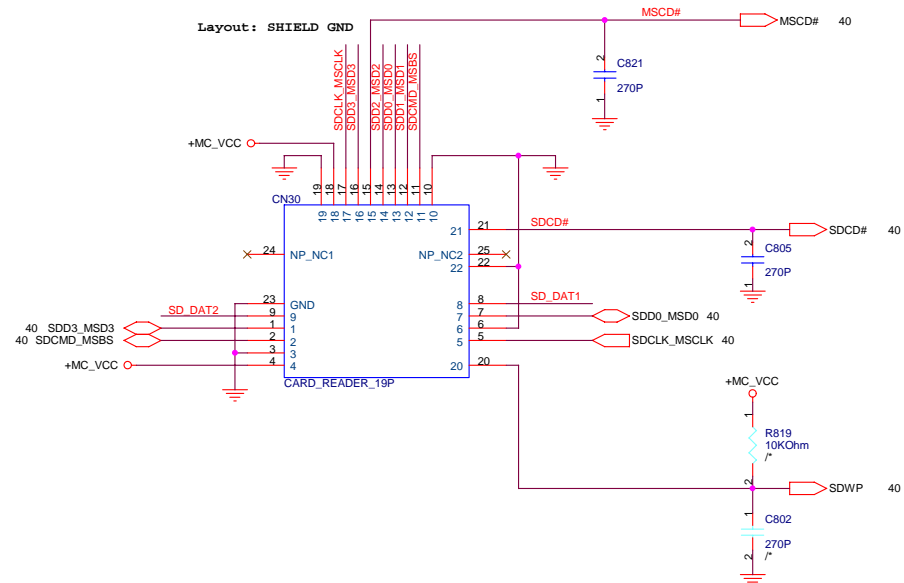
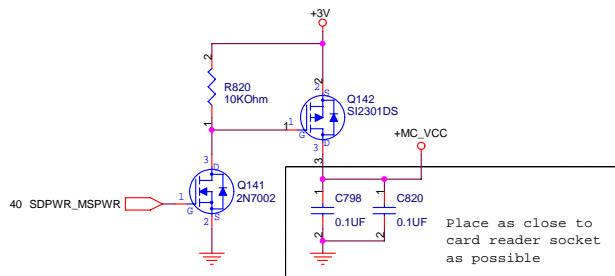
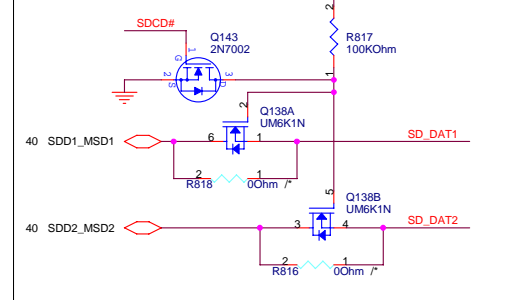
1394A CON

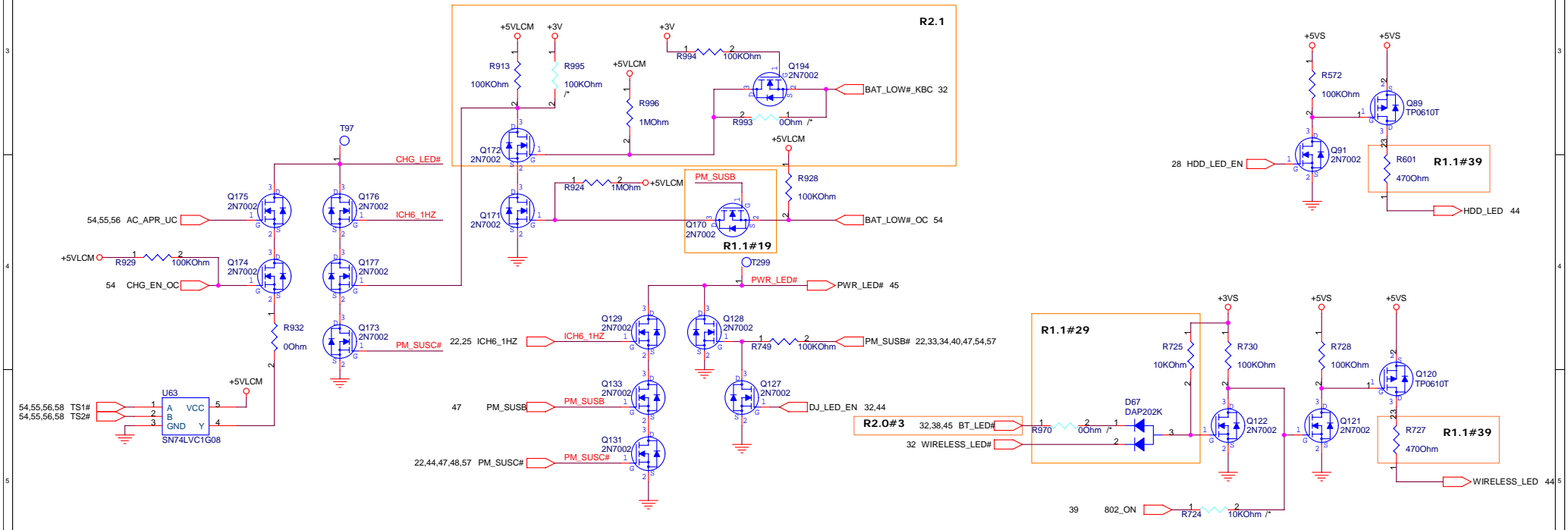
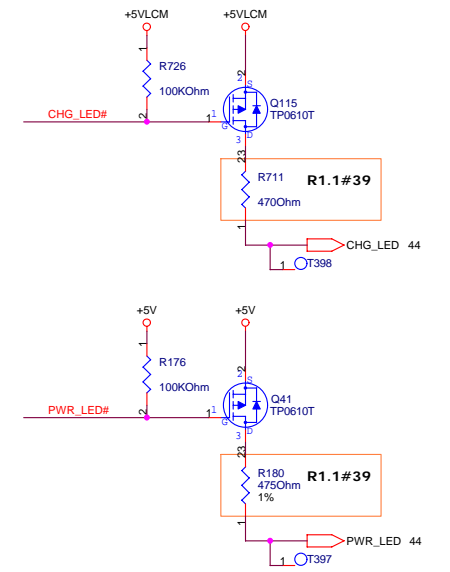
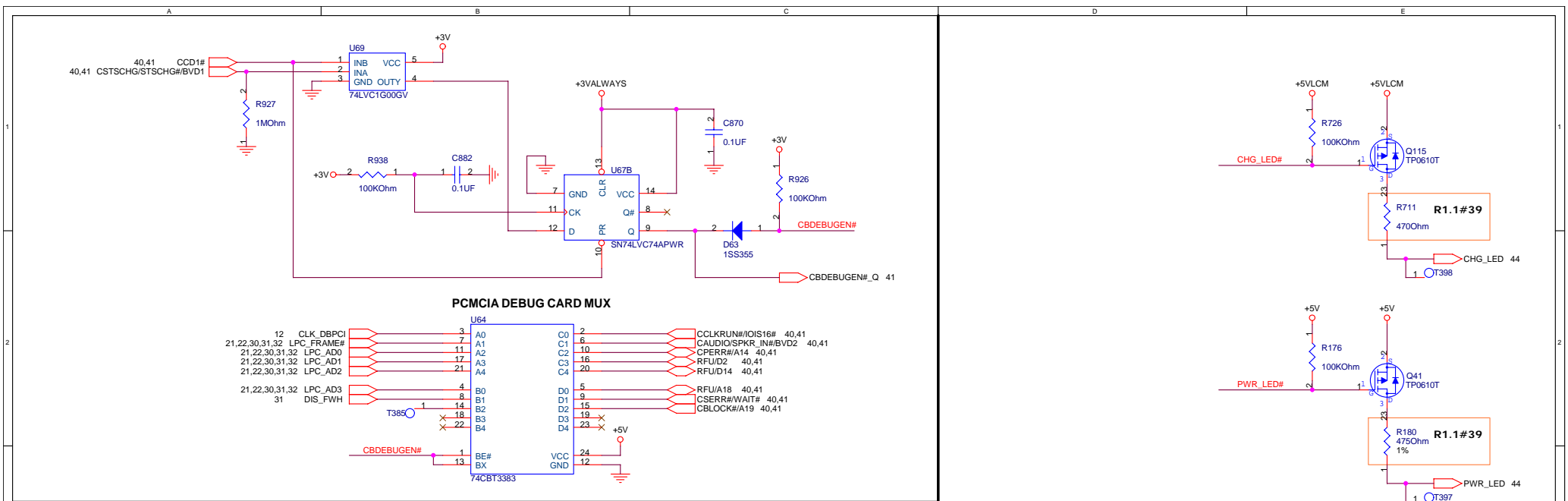


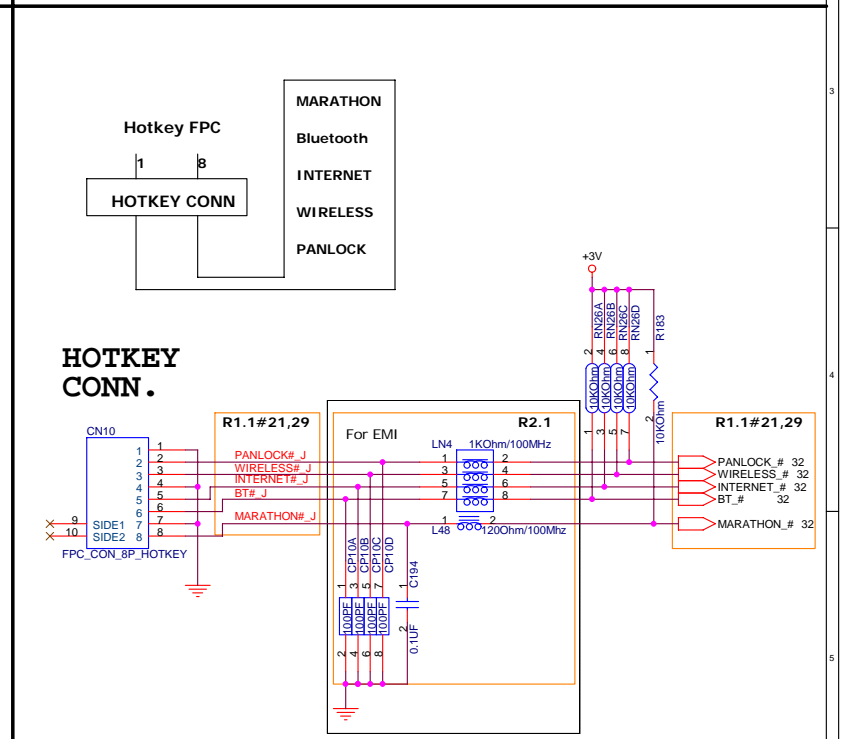
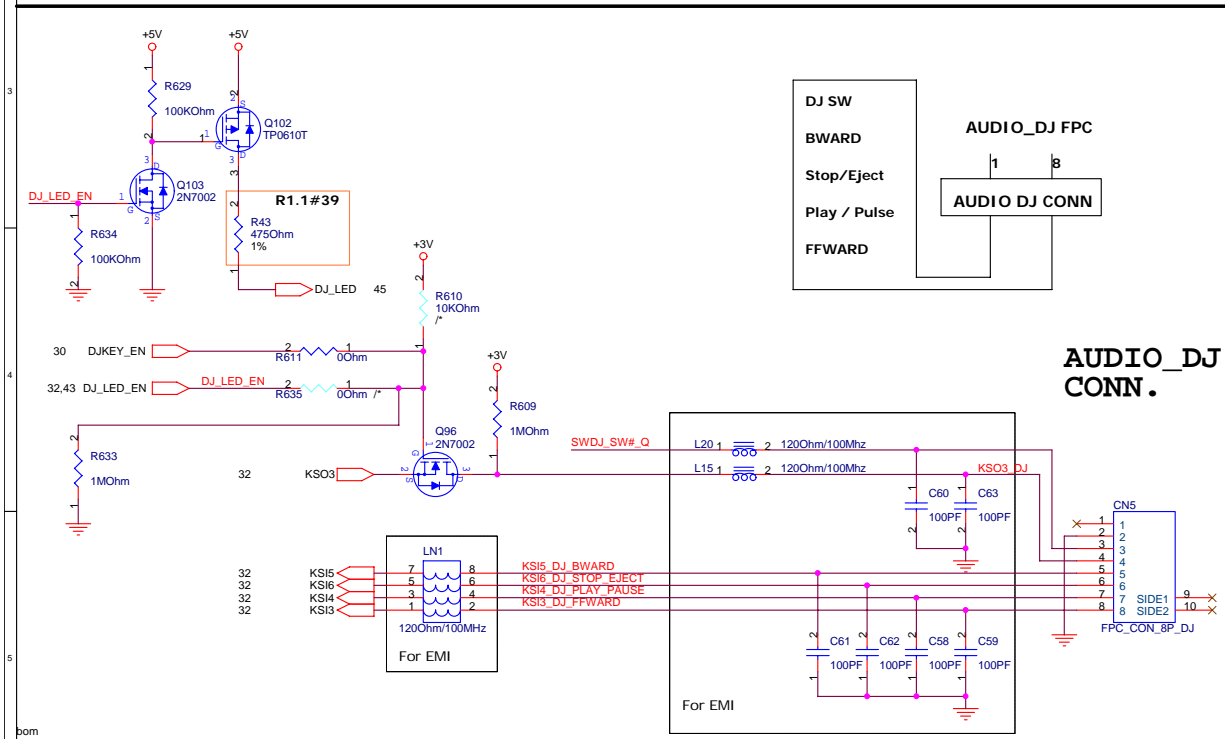
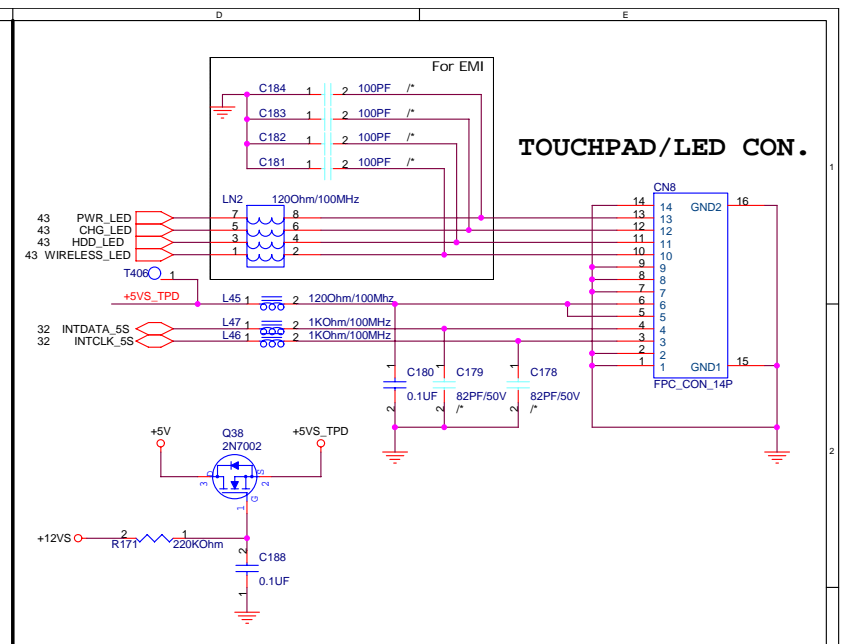
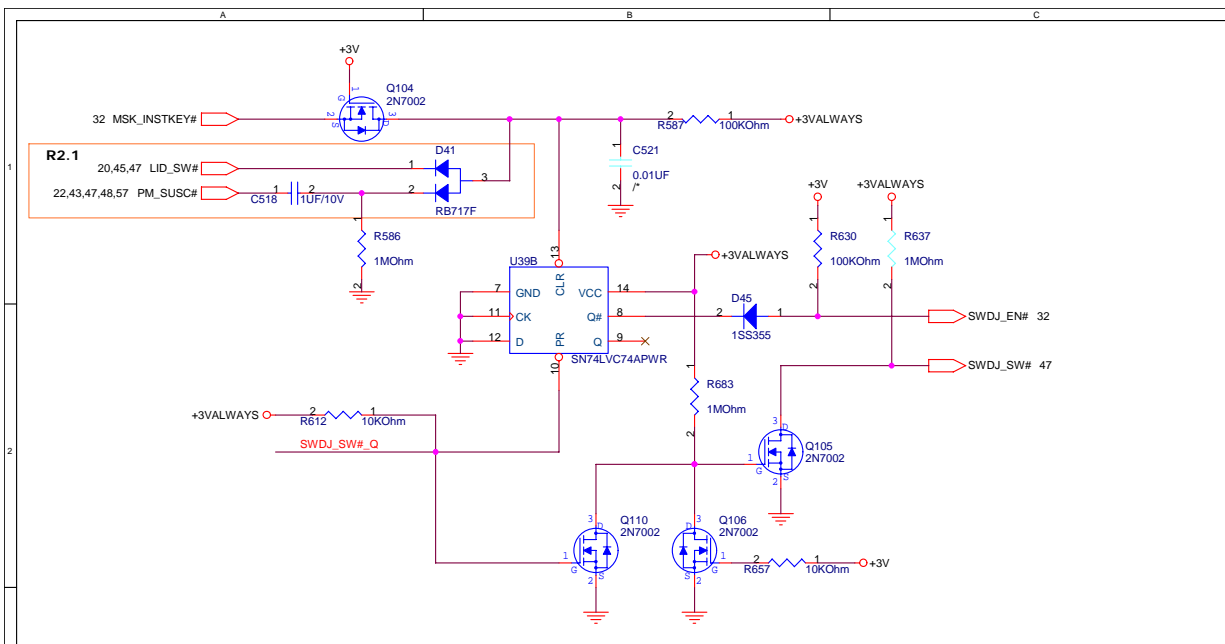
1. Close to R5C841
2. The area is as compact as possible, length < 10 mm
3. TPA Pair and TPB pair mismatch < 2.5mm
4. No via recommend, maximum is one.
5. Total length < 50 mm
6. Differential impedance is 110+/- 6 ohm
7. TPA Pair trace or TPB pair trace mismatch < 1.25mm



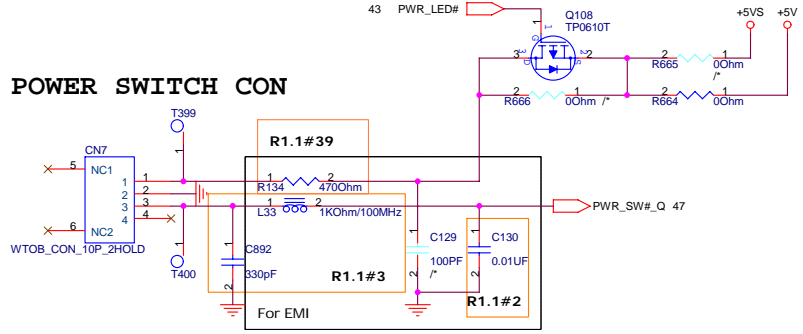
To solve MS-Duo short with SD card



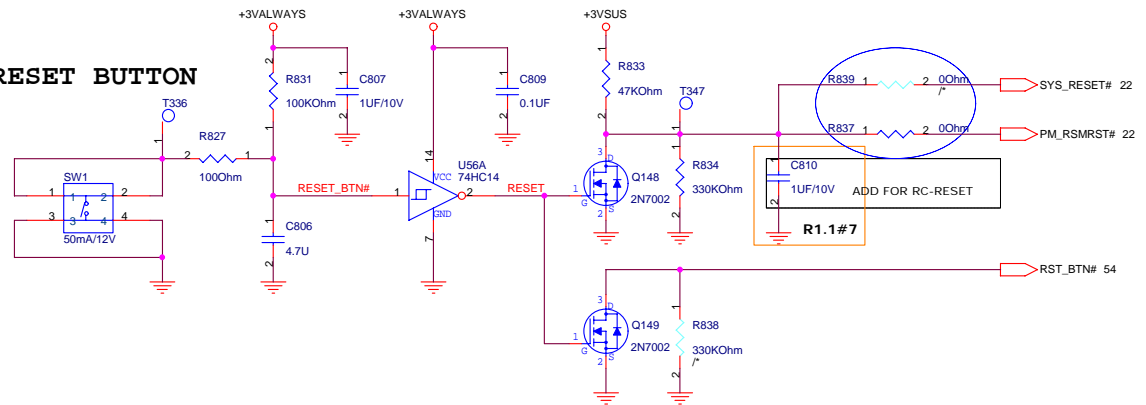




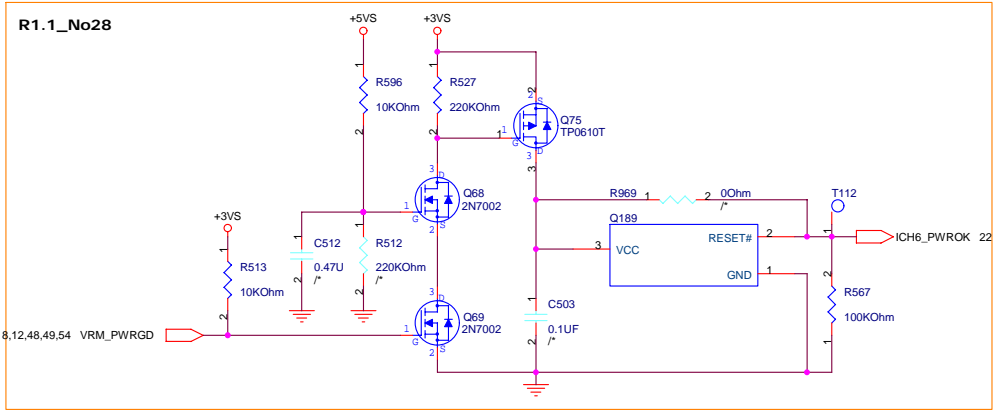
POWER SWITCH CON



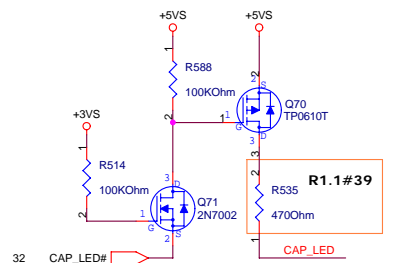
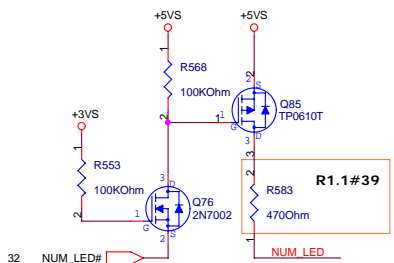
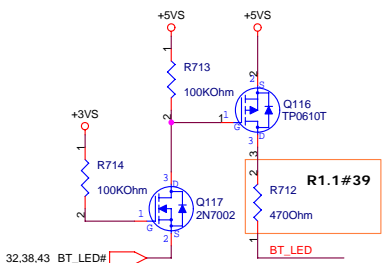
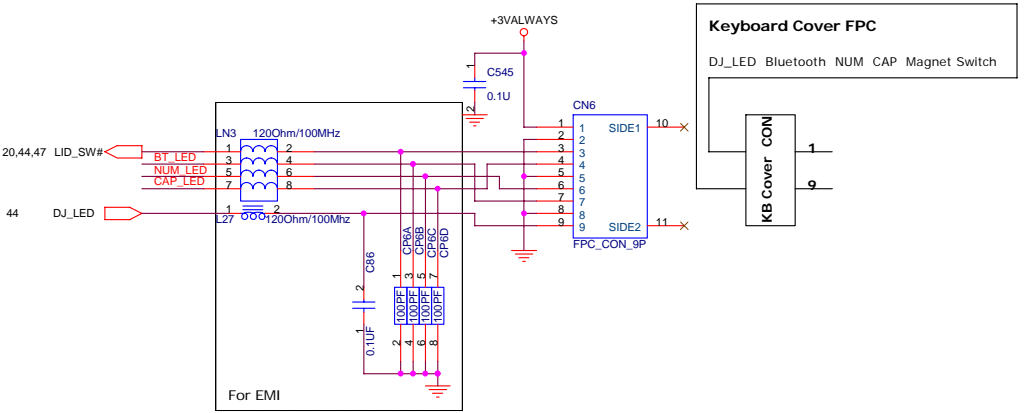
RESET BUTTON

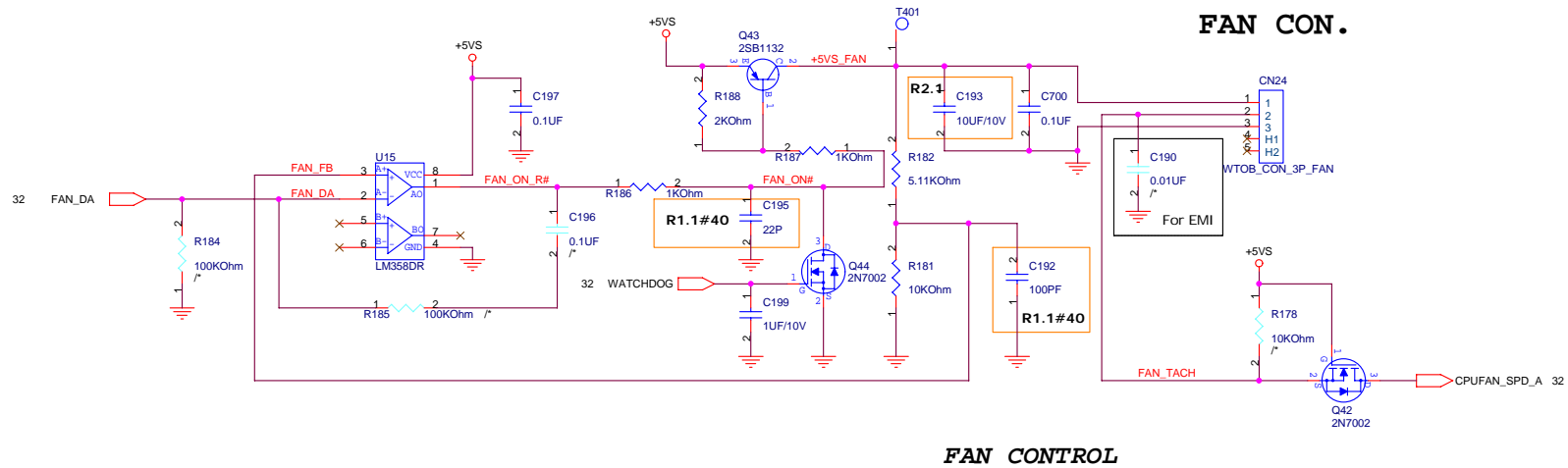


R1.1_No28

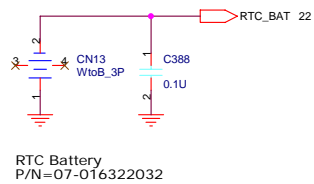


KB COVER CON

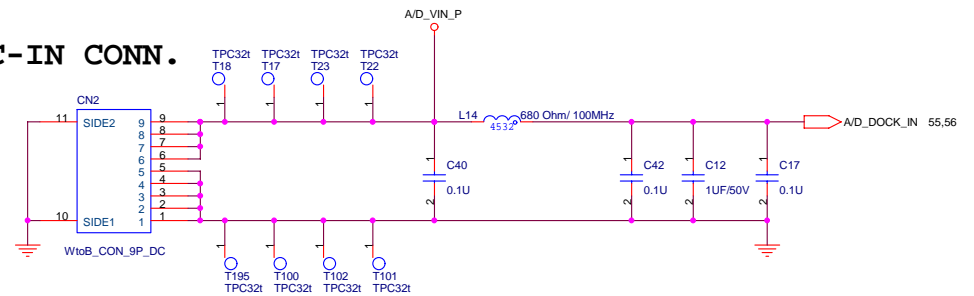




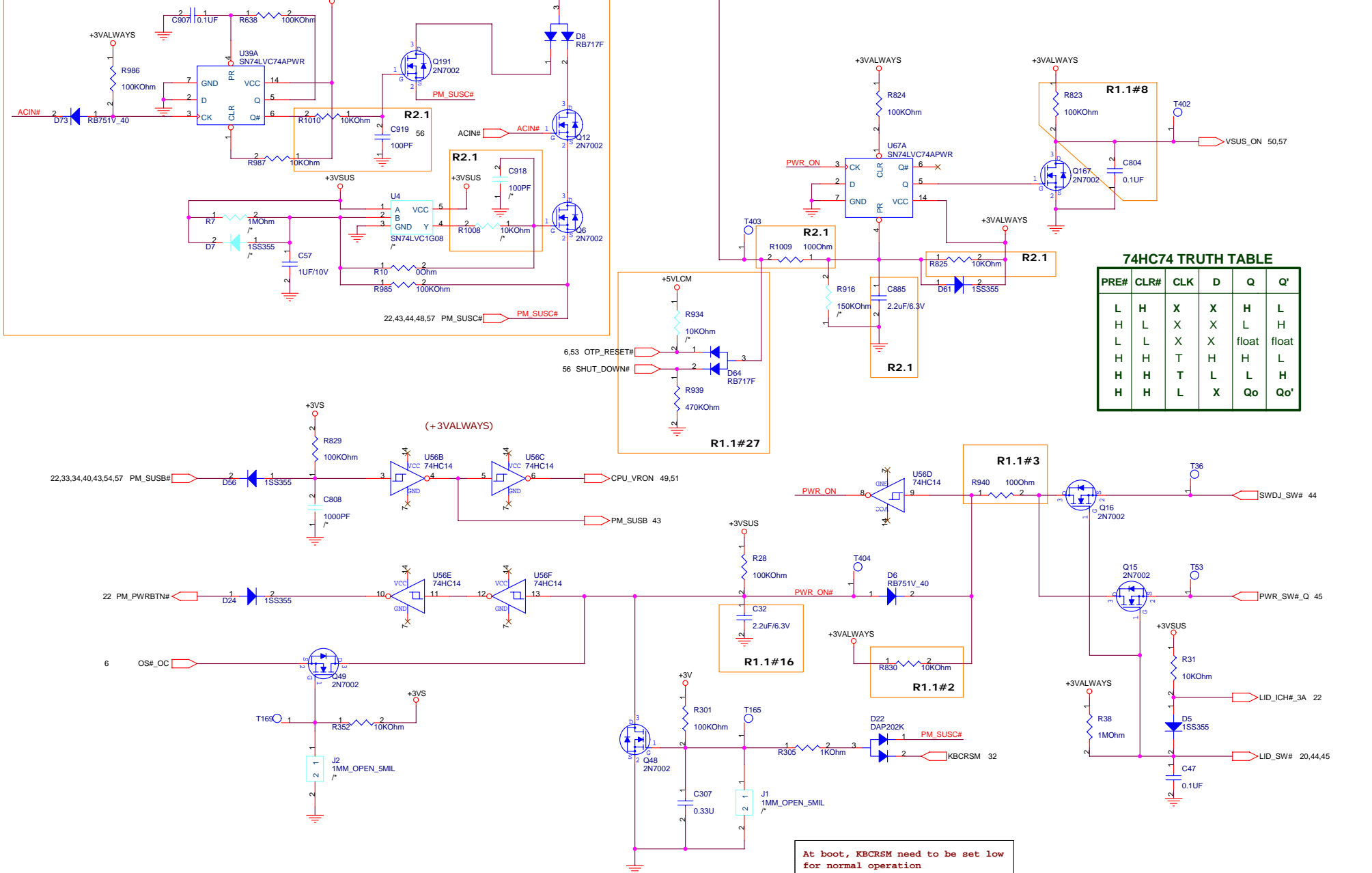
RTC BAT CON.



DC-IN CONN.



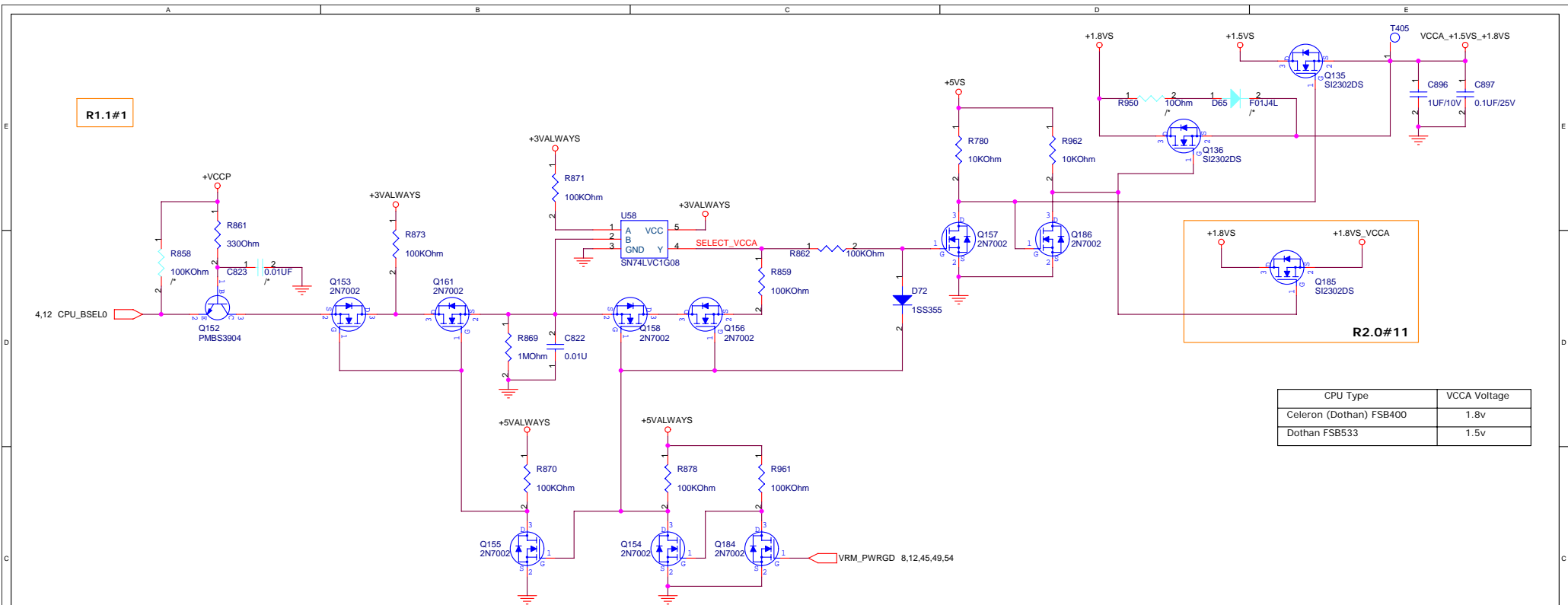
R2.0#10



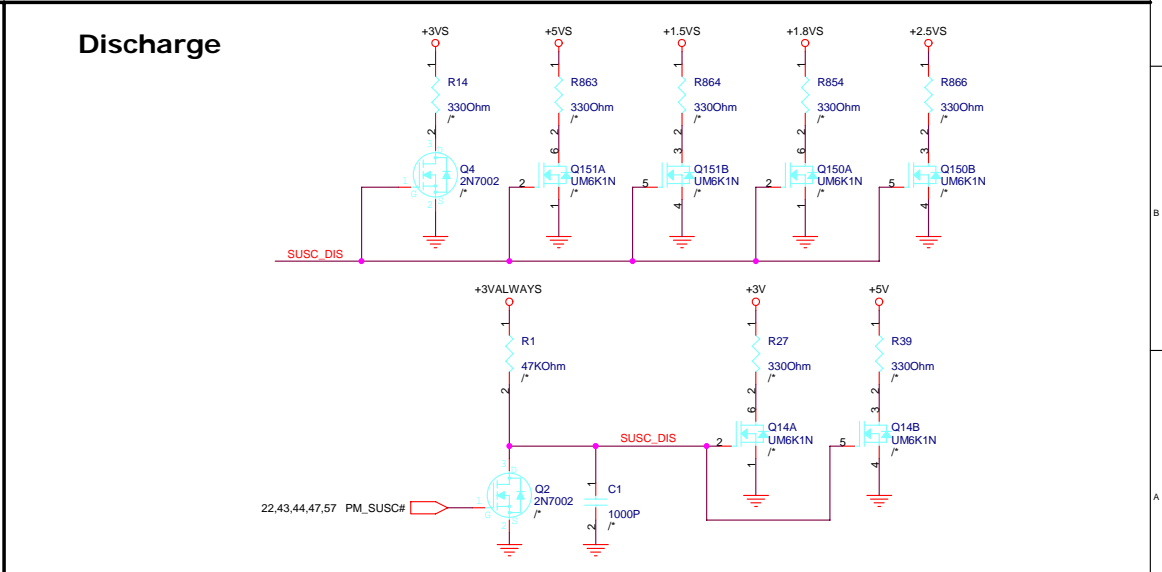
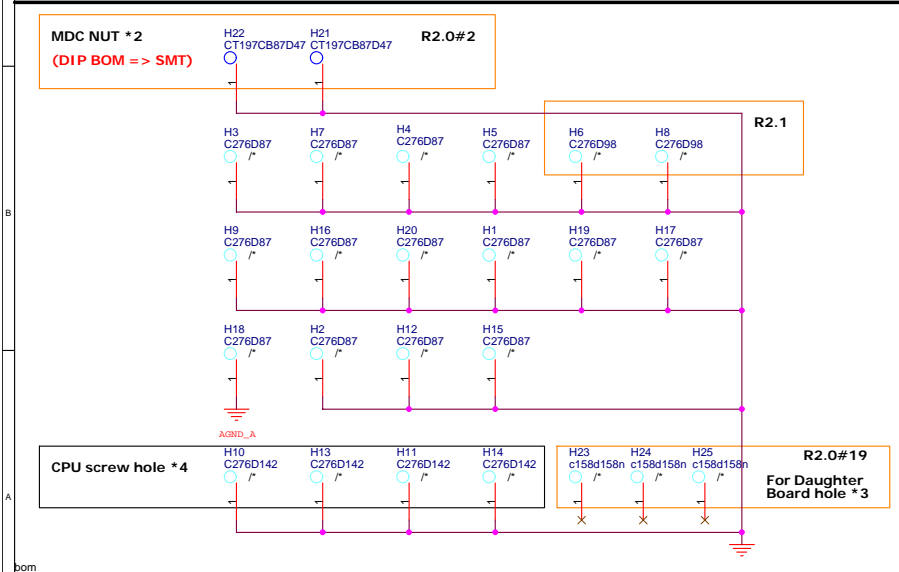
74HC74 TRUTH TABLE

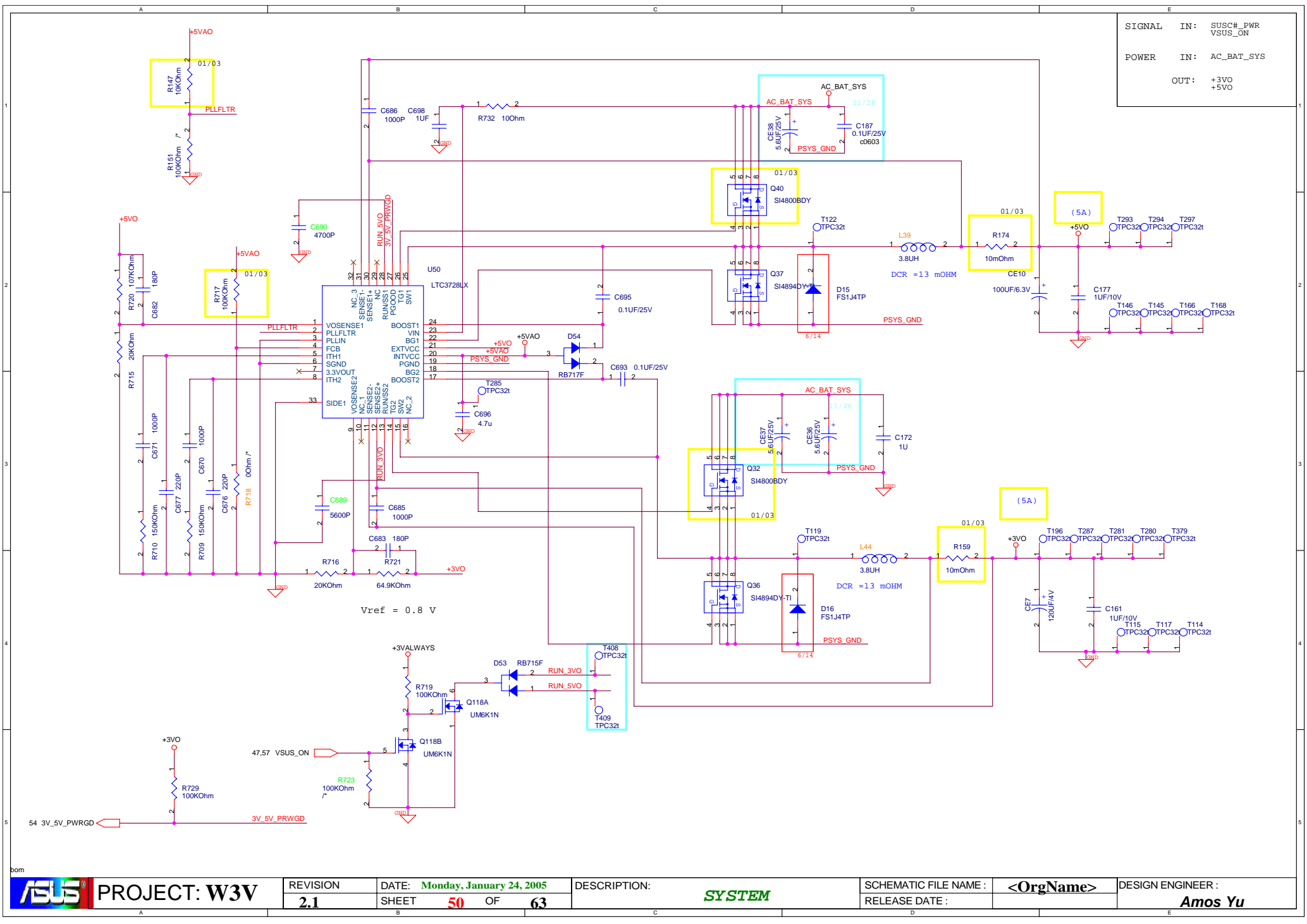
PRE#	CLR#	CLK	D	Q	Q'
L	H	X	X	H	L
L	L	X	X	L	H
L	L	X	X	float	float
H	H	T	H	H	L
H	H	T	L	L	H
H	H	L	X	Qo	Qo'

At boot, KBCRSM need to be set low for normal operation

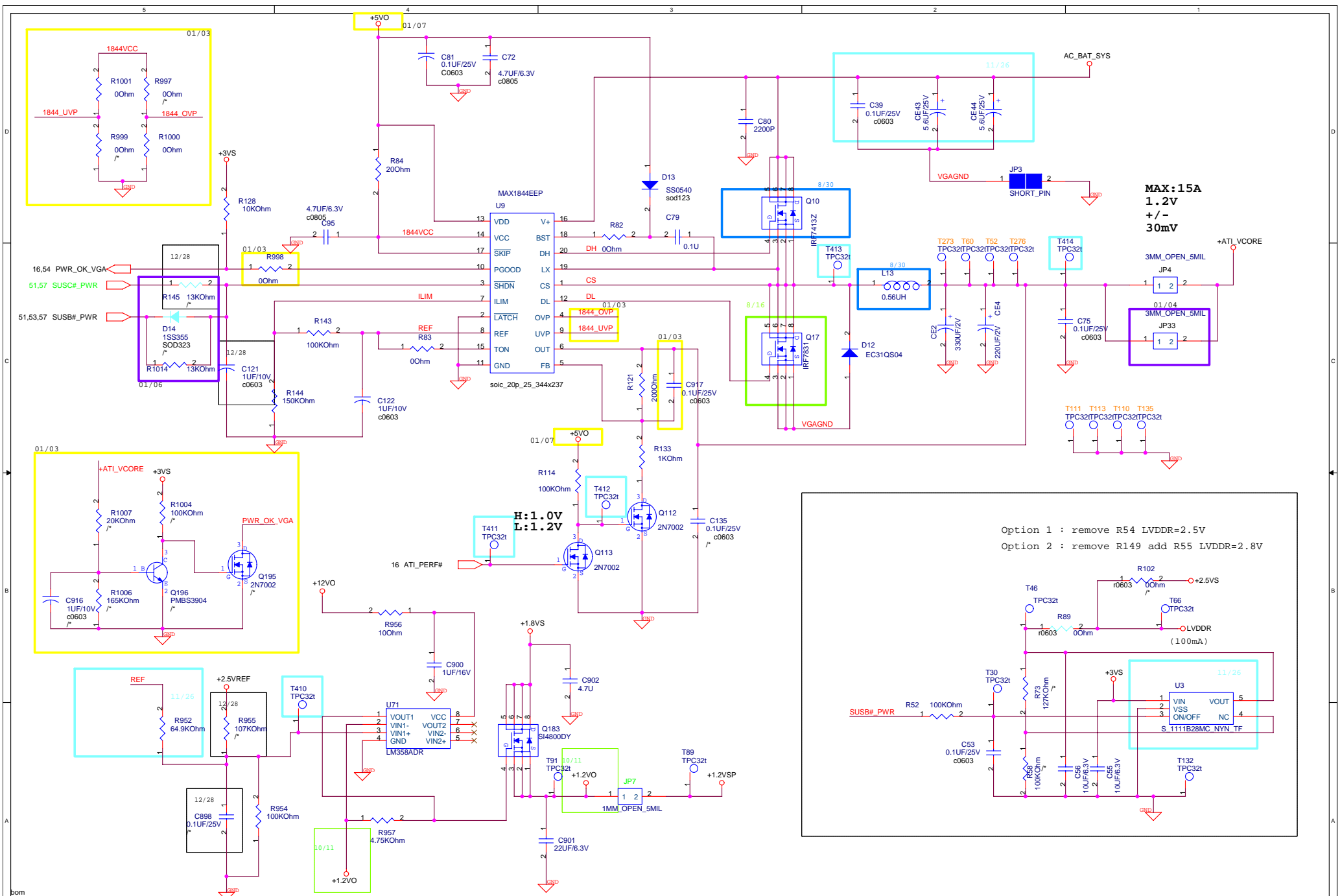


CPU Type	VCCA Voltage
Celeron (Dothan) FSB400	1.8v
Dothan FSB533	1.5v





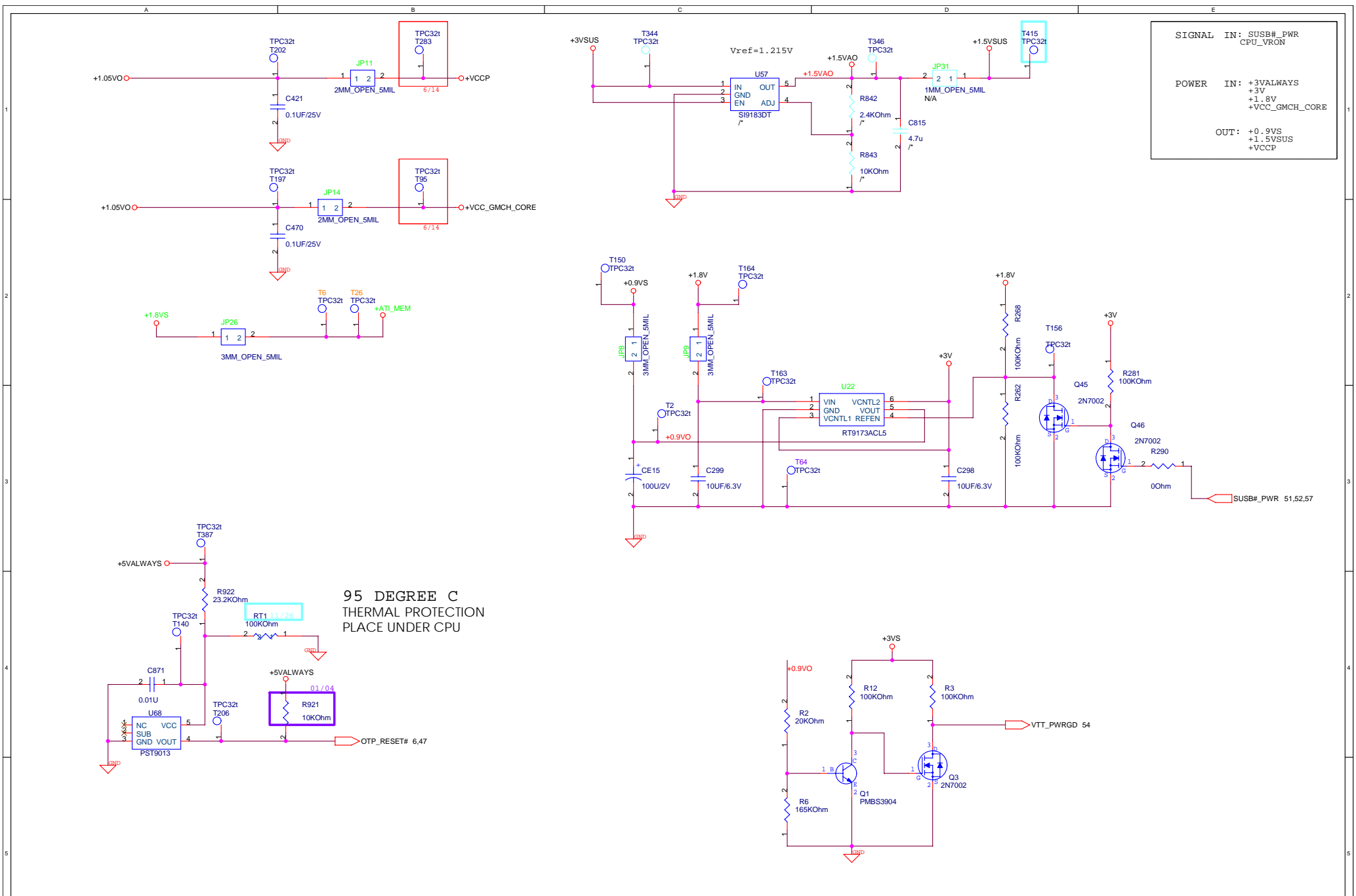
SIGNAL	IN:	SUSC#_PWR
		VSUS_ON
POWER	IN:	AC_BAT_SYS
	OUT:	+3V0
		+5V0



MAX: 1.5A
1.2V
+/- 30mV

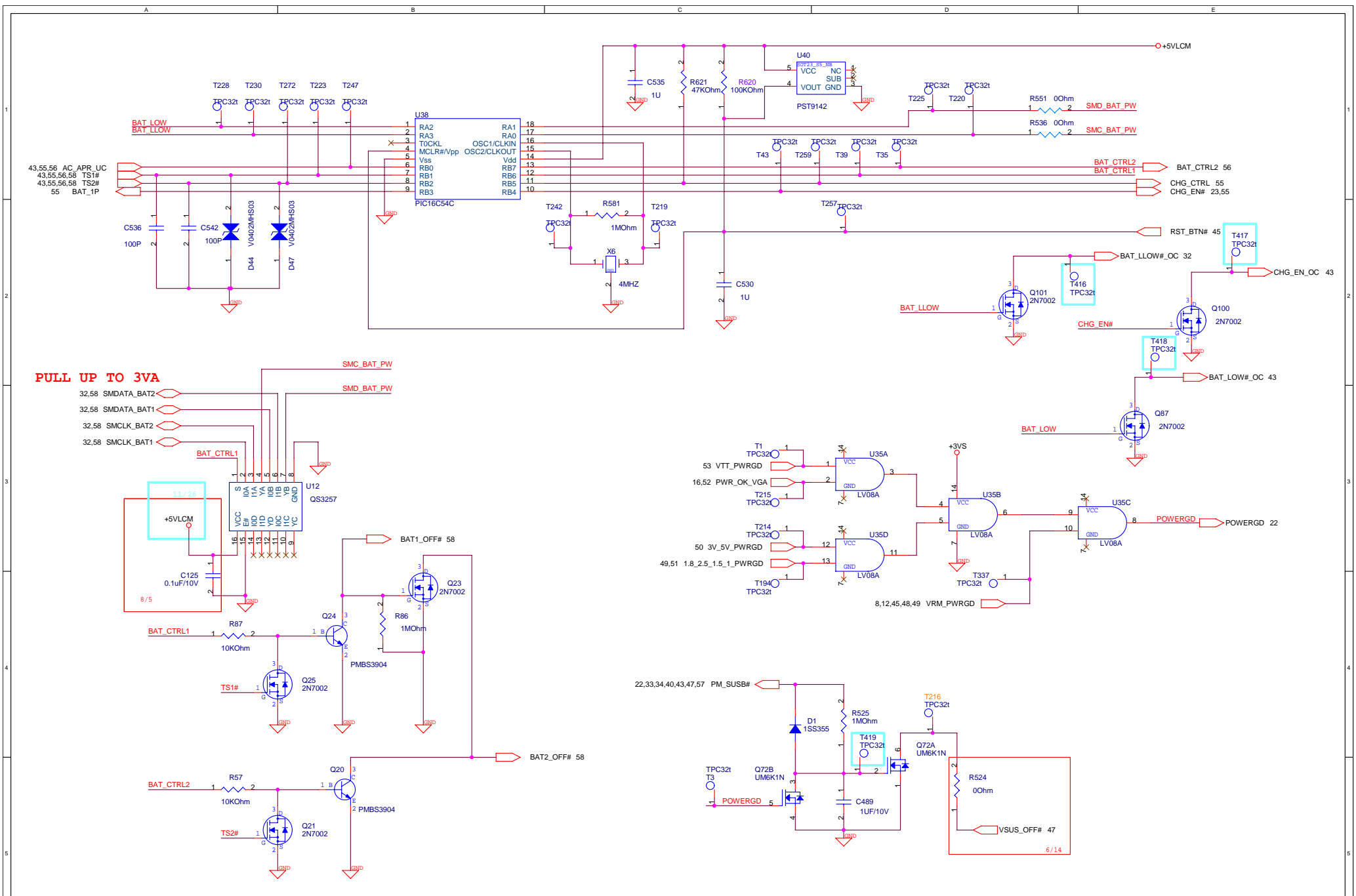
H: 1.0V
L: 1.2V

Option 1 : remove R54 LVDDR=2.5V
Option 2 : remove R149 add R55 LVDDR=2.8V

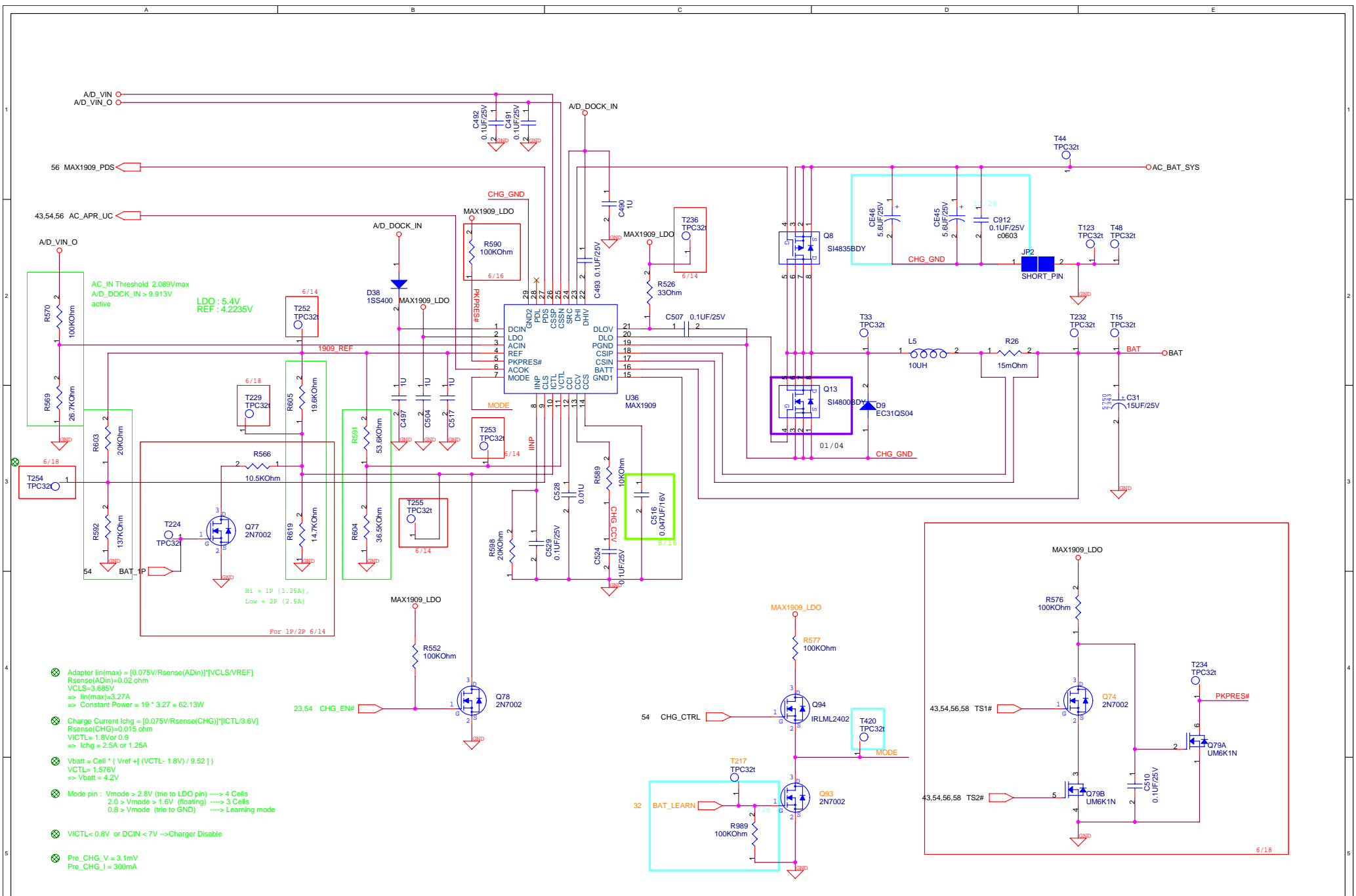


SIGNAL	IN: SUSB#_PWR CPU_VRON
POWER	IN: +3VALWAYS +3V +1.8V +VCC_GMCH_CORE
OUTPUT	OUT: +0.9VS +1.5VSUS +VCCP

95 DEGREE C
THERMAL PROTECTION
PLACE UNDER CPU



PULL UP TO 3VA



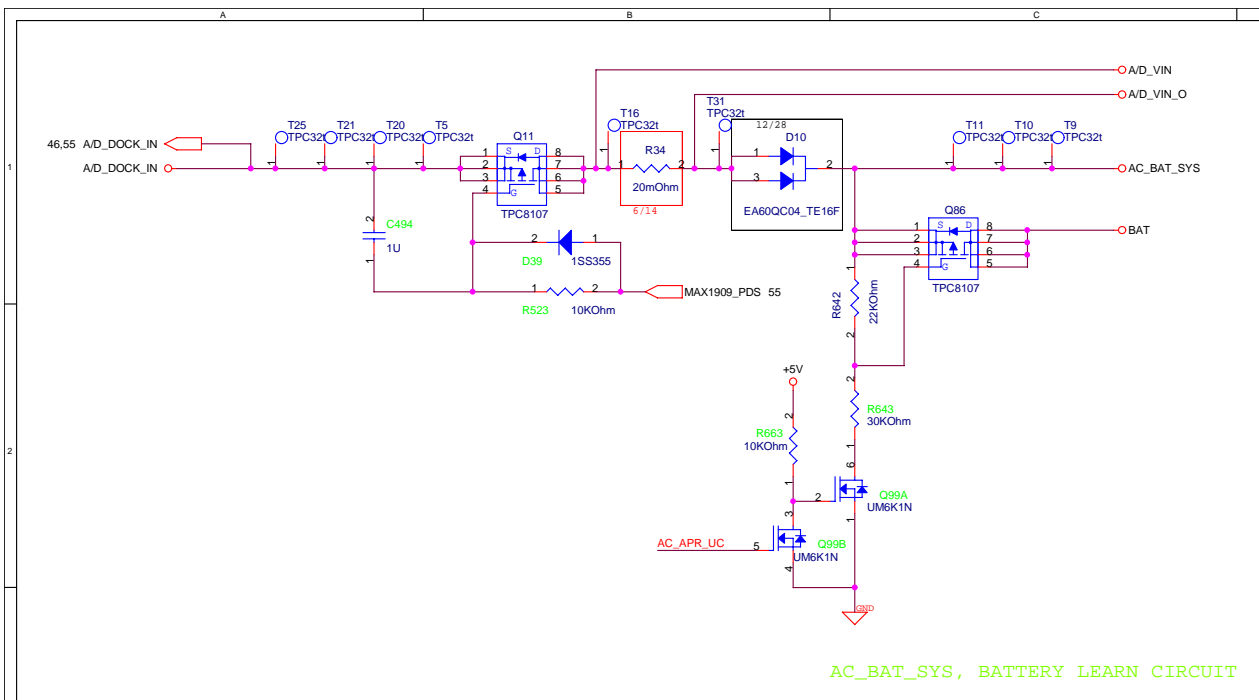
AC_IN_Threshold 2.089Vmax
 A/D_DOCK_IN > 9.913V
 active

LDO : 5.4V
 REF : 4.2235V

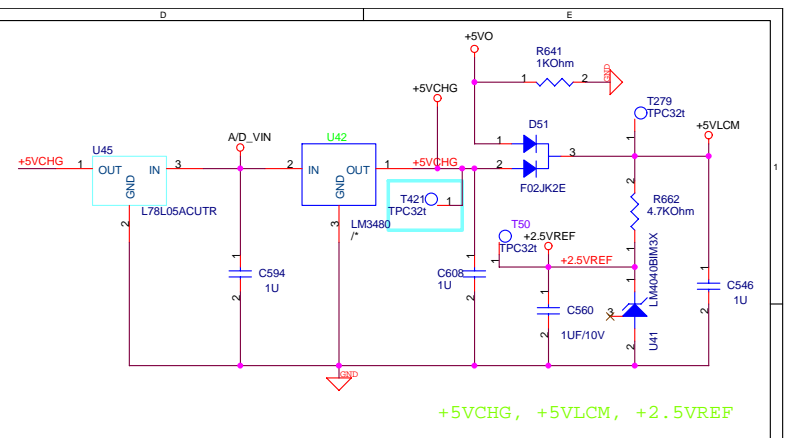
Hi = 1P (1.25A),
 Low = 2P (2.5A)

Pot 1P/2P 6/14

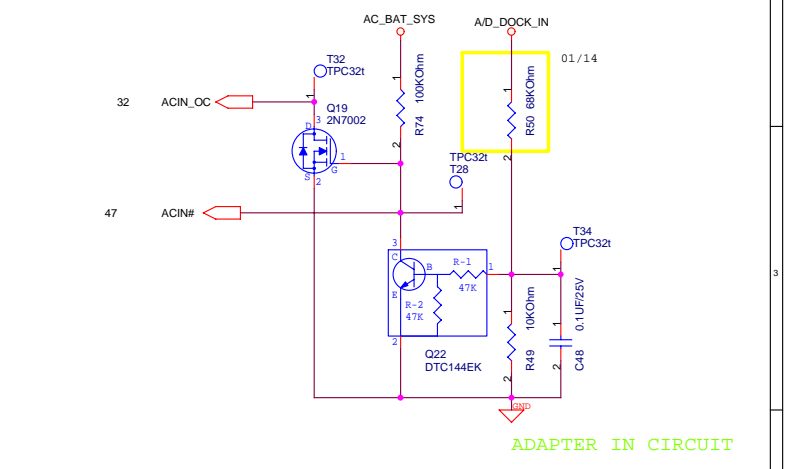
- ⊗ Adapter lin(max) = [0.075V/Rsense(ADIN)]*[VCLS/VREF]
 Rsense(ADIN)=0.02 ohm
 VCLS=3.685V
 => lin(max)=3.27A
 => Constant Power = 19 * 3.27 = 62.13W
- ⊗ Charge Current Ichg = [0.075V/Rsense(CHG)]*[ICTL/3.6V]
 Rsense(CHG)=0.015 ohm
 VICTL= 1.8V or 0.9
 => Ichg = 2.5A or 1.25A
- ⊗ Vbatt = Cell * [Vref + [(VCTL - 1.8V) / 9.52]]
 VCTL= 1.576V
 => Vbatt = 4.2V
- ⊗ Mode pin : Vmode > 2.8V (tie to LDO pin) ----> 4 Cells
 2.0 > Vmode > 1.6V (floating) ----> 3 Cells
 0.8 > Vmode (tie to GND) ----> Learning mode
- ⊗ VICTL < 0.8V or DCIN < 7V --> Charger Disable
- ⊗ Pre_CHG_V = 3.1mV
 Pre_CHG_I = 300mA



AC_BAT_SYS, BATTERY LEARN CIRCUIT

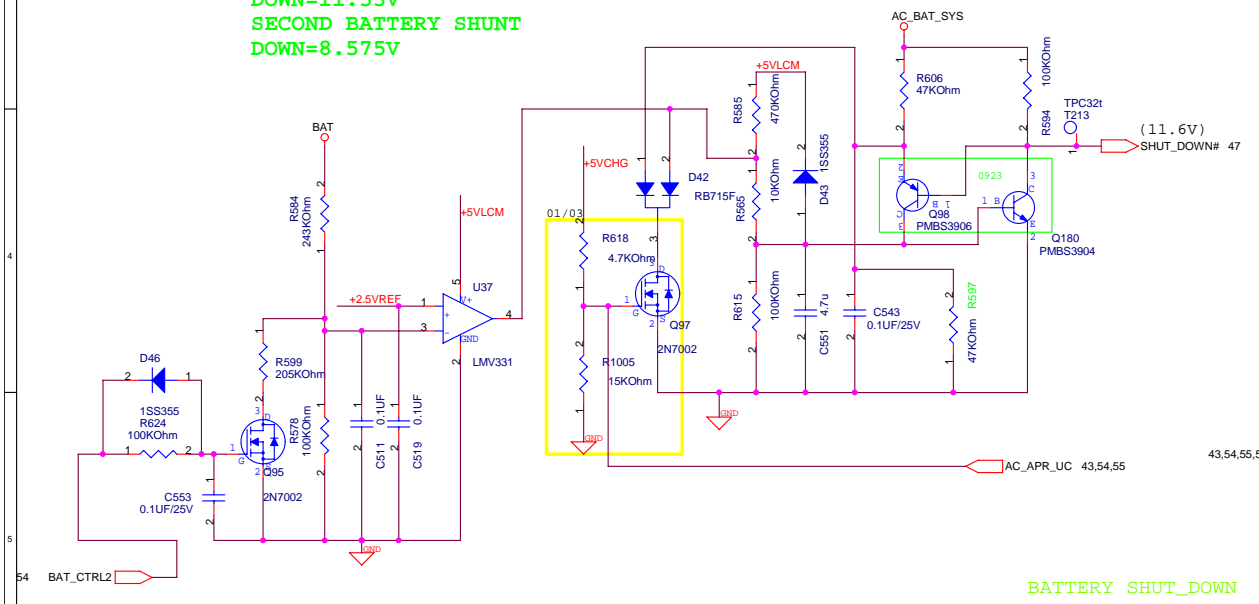


+5VCHG, +5VLCM, +2.5VREF

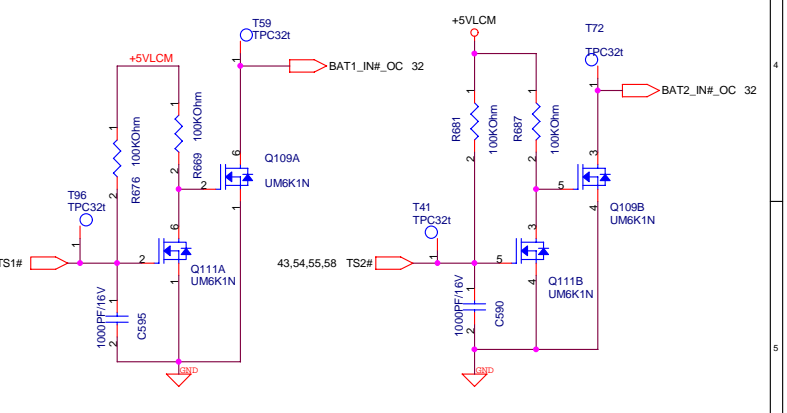


ADAPTER IN CIRCUIT

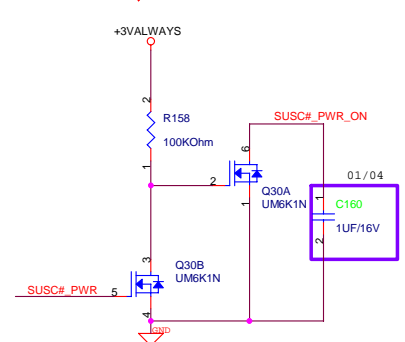
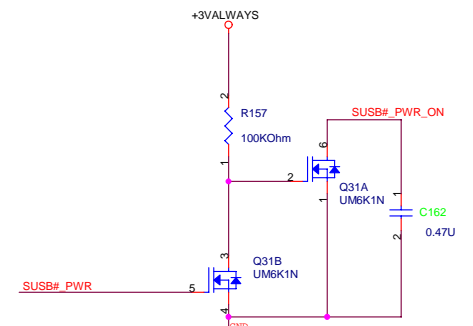
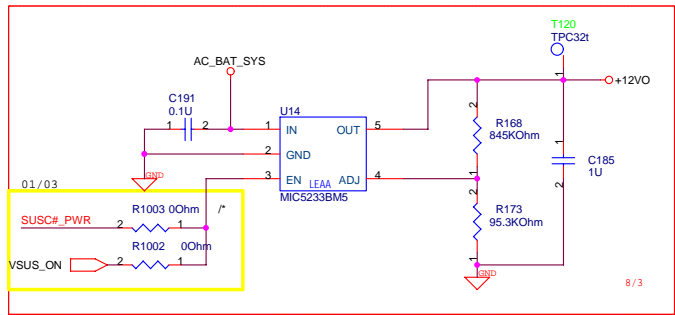
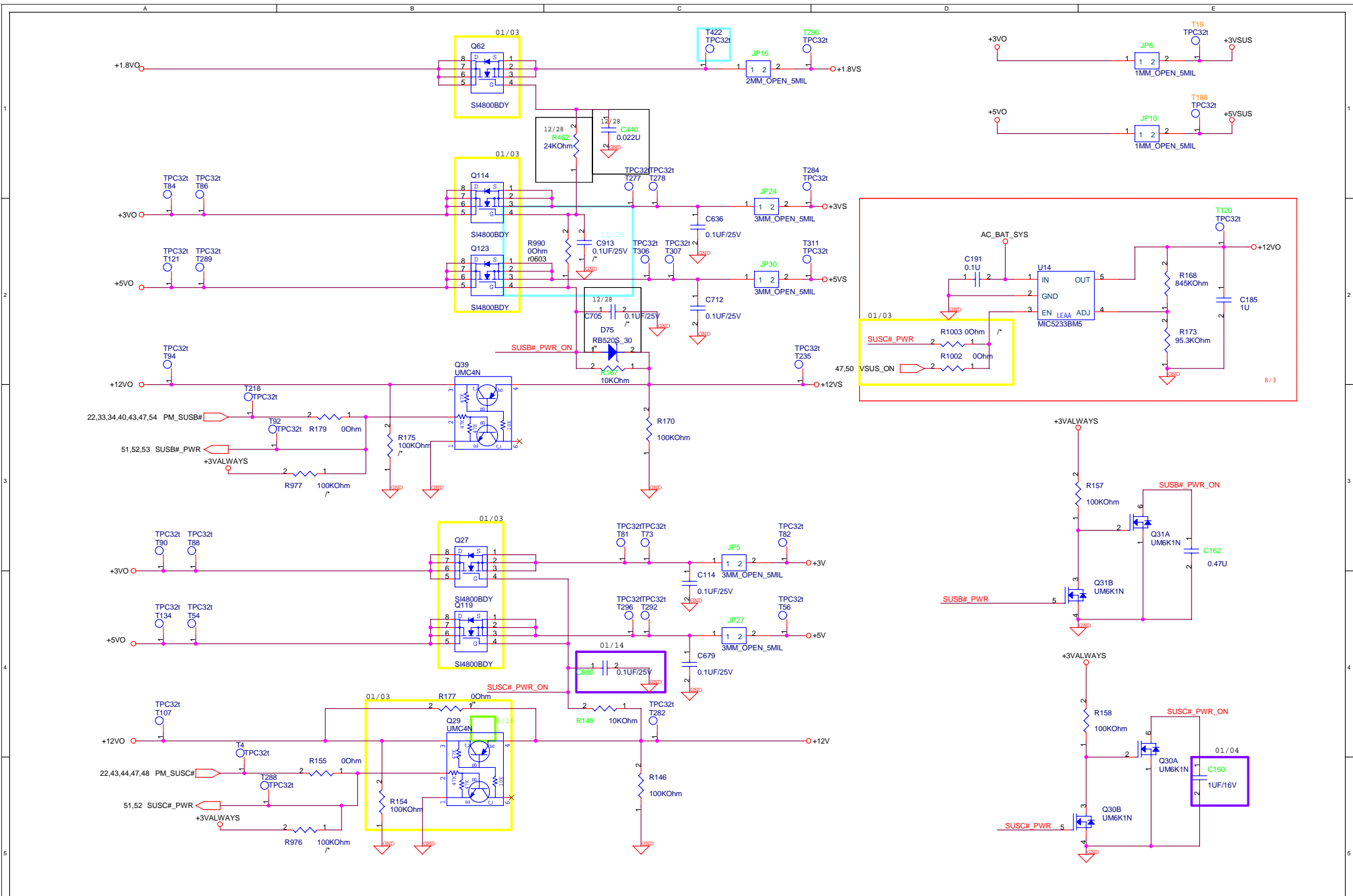
MAIN BATTERY SHUNT
DOWN=11.53V
SECOND BATTERY SHUNT
DOWN=8.575V

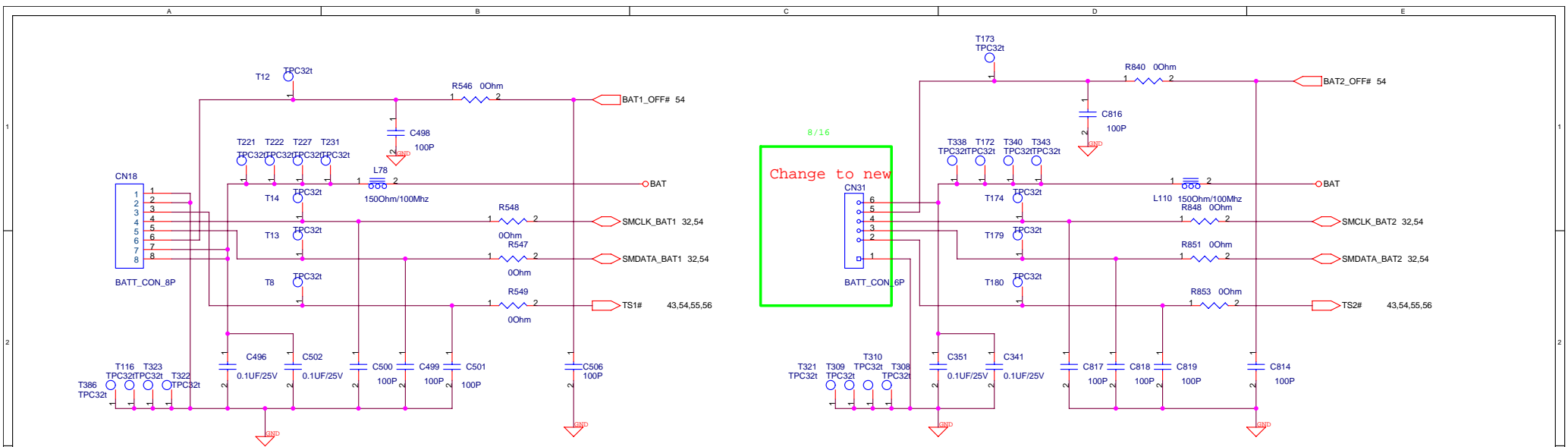


BATTERY SHUT_DOWN

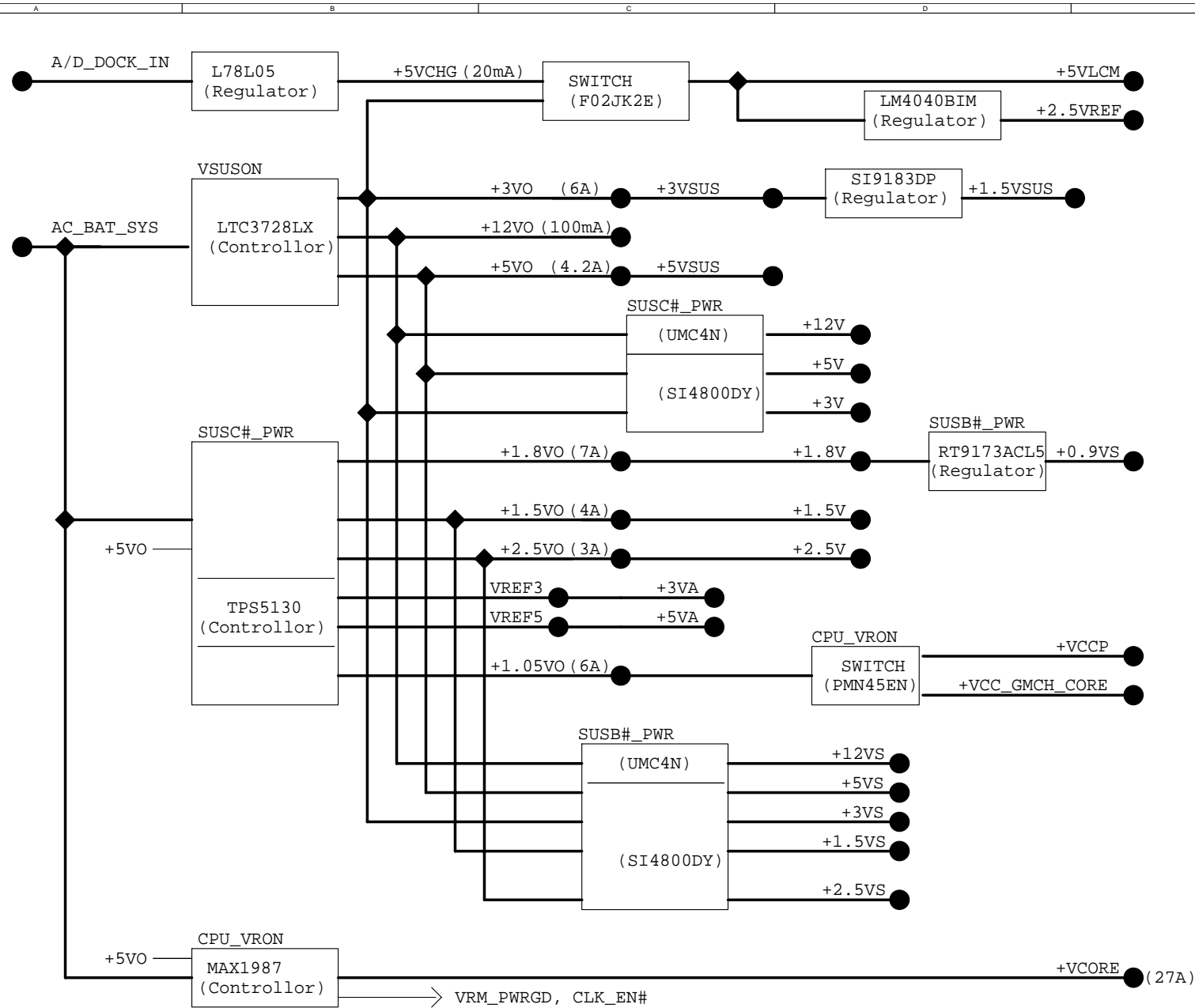


BATTERY IN CIRCUIT





	PROJECT: W3V		REVISION	DATE: Monday, January 24, 2005	DESCRIPTION:	SCHMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
			2.1	SHEET 58 OF 63	PIC16C54/BATCON/PWOK	RELEASE DATE :		Amos Yu



VR_VID0 - VR_VID5, STP_CPU#, PM_DPRSLPVR, PM_PSI#

bom

ASUS Title : POWER FLOWCHART
 ASUSTeK COMPUTER INC Engineer:

Size	Project Name	Rev
Custom	W3V	2.1
Date: Wednesday, January 26, 2005		Sheet 59 of 63

Revision History

R1.1

SYSTEM

1. (p48) Modify CPU +VCCA
2. (p45,47) Fix auto power on when AC in in AC mode
3. (p45,57) Solve U56 easily damaged
4. (p8) Add R941 for BIOS internal VGA strapping
5. (p8) U48, D30 change from ICH6_PWROK to VRM_PWRGD (p12) R363 change to 10K, C893=0.47uF
6. (p20) Fix PID1 can't strapped low
7. (p45) Modify power sequence of +3VSUS -> PM_RSMRST#
8. (p47) Fix that +3VSUS/+5VSUS may be turned on for a while when the power comes in at the first time
9. (p16) Fix TV out can't work
10. Add Bluetooth support
11. (p24) DEL reserved V5REF_SUS circuit
12. (p12) ADD net "CPUSELO/1" for layout
13. (p37) Change X7 part
14. (p23) Add R949 to reduce overshoot
15. (p34) Solve pop noise in Windows boot
16. (p47) Power button debounce
17. Tune X'tal freq. (p22) C353/C356 (p26) C350/C354 (p32) C78/C93 (p41) C355/C360
18. (p27) Change CN32 part
19. (p43) Change R924 to +5VLCM to solve +5V leakage in power off.
20. (p20) Tune LCD_VCC timing
21. (p44) Modify CN10 pin define for ID change
22. (p23,34) Add ALC861VS PC-Beep support
23. (p33) ADD T388, U61.3 ADD "AUD_GPI00" (p34) DEL R482, ADD U72
24. (p34,35) DEL net "MIC_AGND_A"
25. (p39) ADD voltage divider for Mic VREF
26. (p34) for EMI request
27. (p47) VSUS_OFF#
28. (p45) Modify power on sequence
29. (p43,p32) Reserved for bluetooth LED
30. (p39) Reserved PCI_INTC# for MINI-PCI.
31. (p29) Solve USB power surge warning when USB HDD plug-in
32. (p28) Support CSEL+ ODD
33. (p6) GMCH_THRMTRIP# no function in high temperature
34. (p10) unstuff for W3V
35. (p17) Adjust ATI 27MHz Vhigh
36. (p23) Aviod logic output unstable
37. (p4) Fix BT_VCC unstable
38. (p40) Tune clock timing
39. (p43) Tune LED current for LED spec
40. (p46) Adjust for +5VS_FAN stable
41. (p47) Fix can't power on in battttery mode

POWER

- 1 (p49) Add R942, MCH_OK connect to 1.8_2.5_1.5_1_PWRGD, C248, R233 unstuff

R2.0

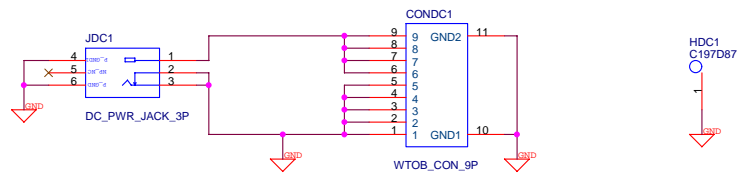
SYSTEM

1. (p20) Adjust BACK_EN Vhigh
2. (p48) Change MDC nut
3. (p22,38,43) DEL BT_ON#, control BT_VCC by BT_LED#
4. (p29) Adjust for USB-IF spec
5. (p32) Solve SMBus loss pull-high power in power-off.
6. (p23) Reduce PCI_RSTNS# overshoot
7. (p23) Reduce 2V step on PCI_RST#
8. (p12) Tune W3V clock
9. (p25) Update PCB_VID
10. (p47) Solve system can't power on in battery mode
11. (p48) Modify +1.8VS_VCCA gate ckt
12. (p20) Avoid U28 damage
13. (p34) Remove reserved Windows de-pop Ckt
14. (p16) Tune W3A HSYNC/VSYNC timing
15. (p21) Tune W3V HSYNC/VSYNC timing
16. (p28) Modify for swap bay detection.
17. (p34) For EMI
18. (p20) For EMI
19. (p48) For PD4
20. (p21) For ME
21. (p33) DEL net "AUD_GPI00"

bom

	PROJECT: W3V			REVISION	DATE: Wednesday, January 26, 2005	DESCRIPTION:	SCHEMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
	2.1	SHEET	60	OF	63	History	RELEASE DATE :		Alice Shih

DC IN



PROJECT: W3V

REVISION
2.1

DATE: Wednesday, January 26, 2005
SHEET 61 OF 63

DESCRIPTION:
DC_IN CONNECTOR

SCHEMATIC FILE NAME : <OrgName>
RELEASE DATE :

DESIGN ENGINEER :
Renyu Wang

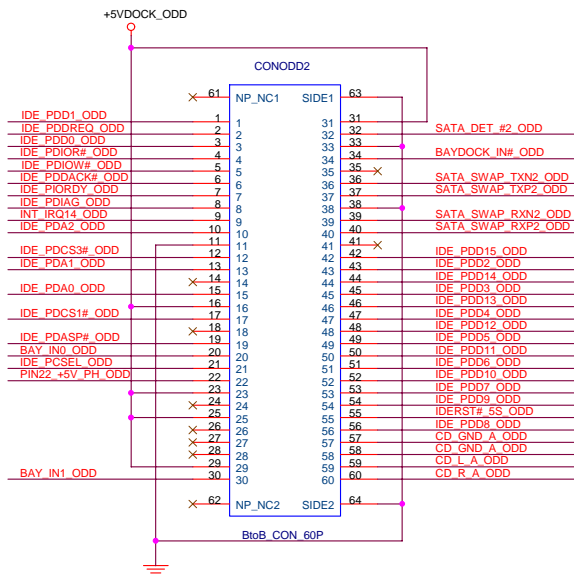
W3V ODD Board

Block Diagram

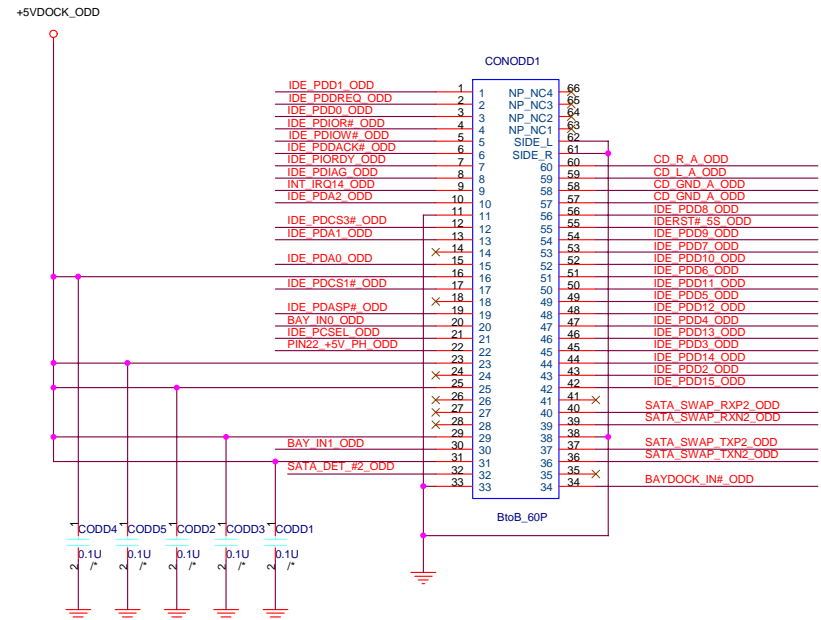
ODD Board Connector

ODD CONN.

ODD BOARD CONN.

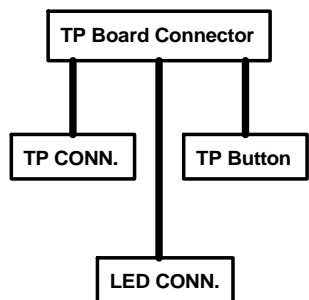


ODD CONN.

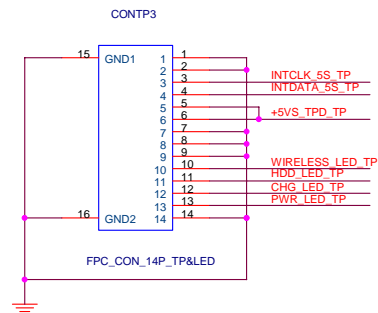


W3V TP & LED Board

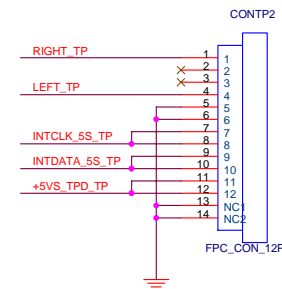
Block Diagram



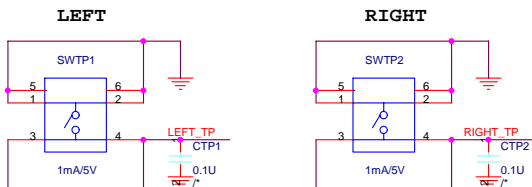
TOUCHPAD & LED BOARD CONN.



TP CONN.



TOUCHPAD BUTTON



LED CONN.

