

MODEL NAME : *QCL00_QCL20*

PCB NO : *LA-8241P*

BOM P/N : *4619GP31L21 Inspiron DIS*
4619GQ31L21 Inspiron UMA
4619GP31L01 Vostro DIS
4619GQ31L01 Vostro UMA

Dell / Compal Confidential

Schematic Document

Inspron A5 & Vostro 3560 (Intel Chief River) Ivy Bridge (rPGA) + Panther Point (mainstream)

Discrete AMD Thames-XT

46@ : for 46 level

@ : Nopop Component

CONN@ : Connector Component

KB930@ : ENE KB930 Implemented

KB9012@ : ENE KB9012 Implemented

EXP@ : Express Card Implemented

FFS@ : Only for Free Fall Sensor

VOS@ : Only for Vostro

INS@ : Only for Inspiron

UMA@ : Only for UMA

GCLK@ : Green CLK implemented

AMP@ : External Amplifier implemented

KBBL@ : Keyboard Back Light implemented

2012-02-01

Rev: 1.0

X76@ : VRAM Group

CH@ : Chelsea M2

SE@ : Seymour M2

TH@ : Thames-XT

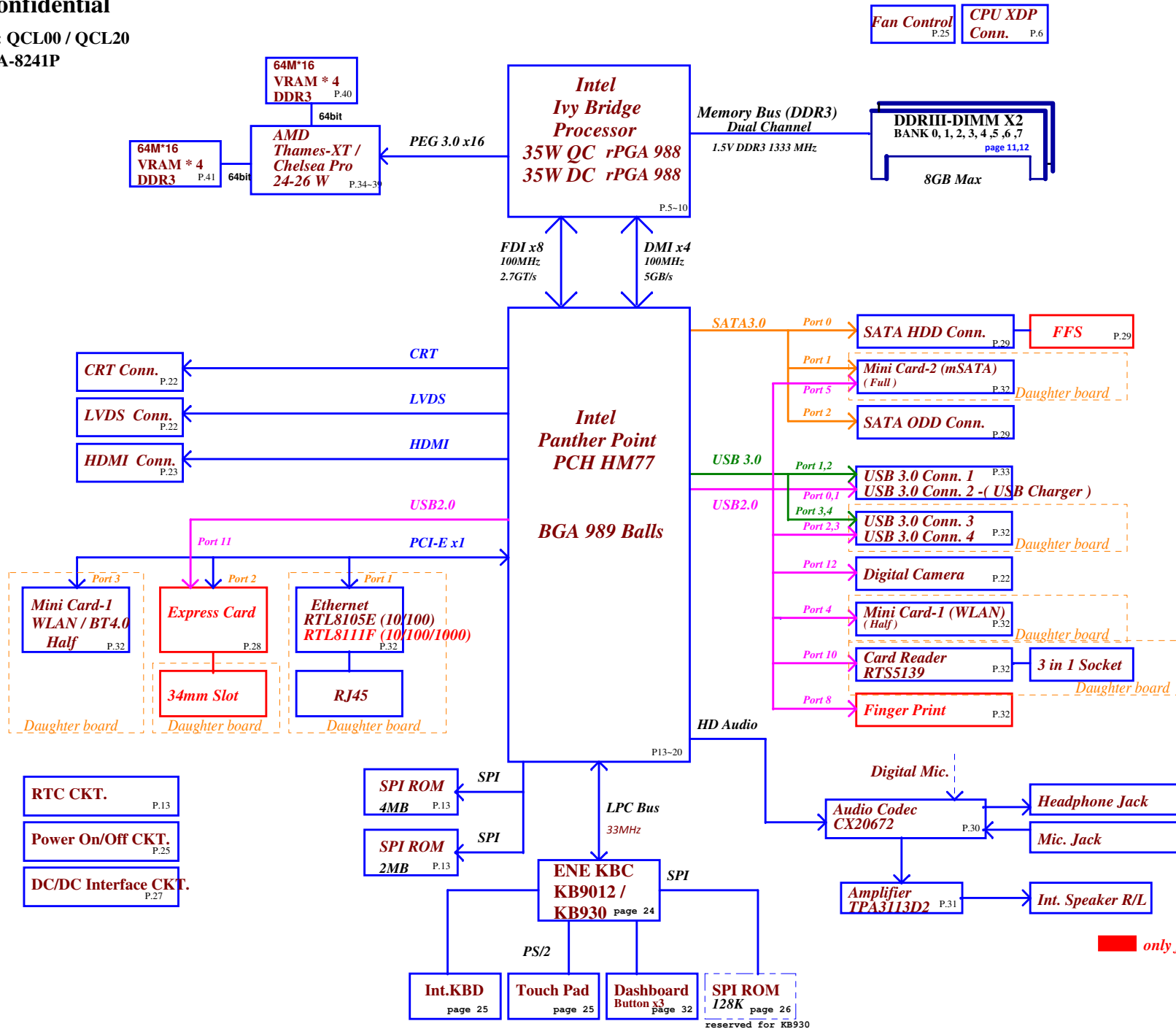
DIS@ : Only for Discrete

MB Type	BOM P/N	Config

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Project Code : QCL00 / QCL20

File Name : LA-8241P



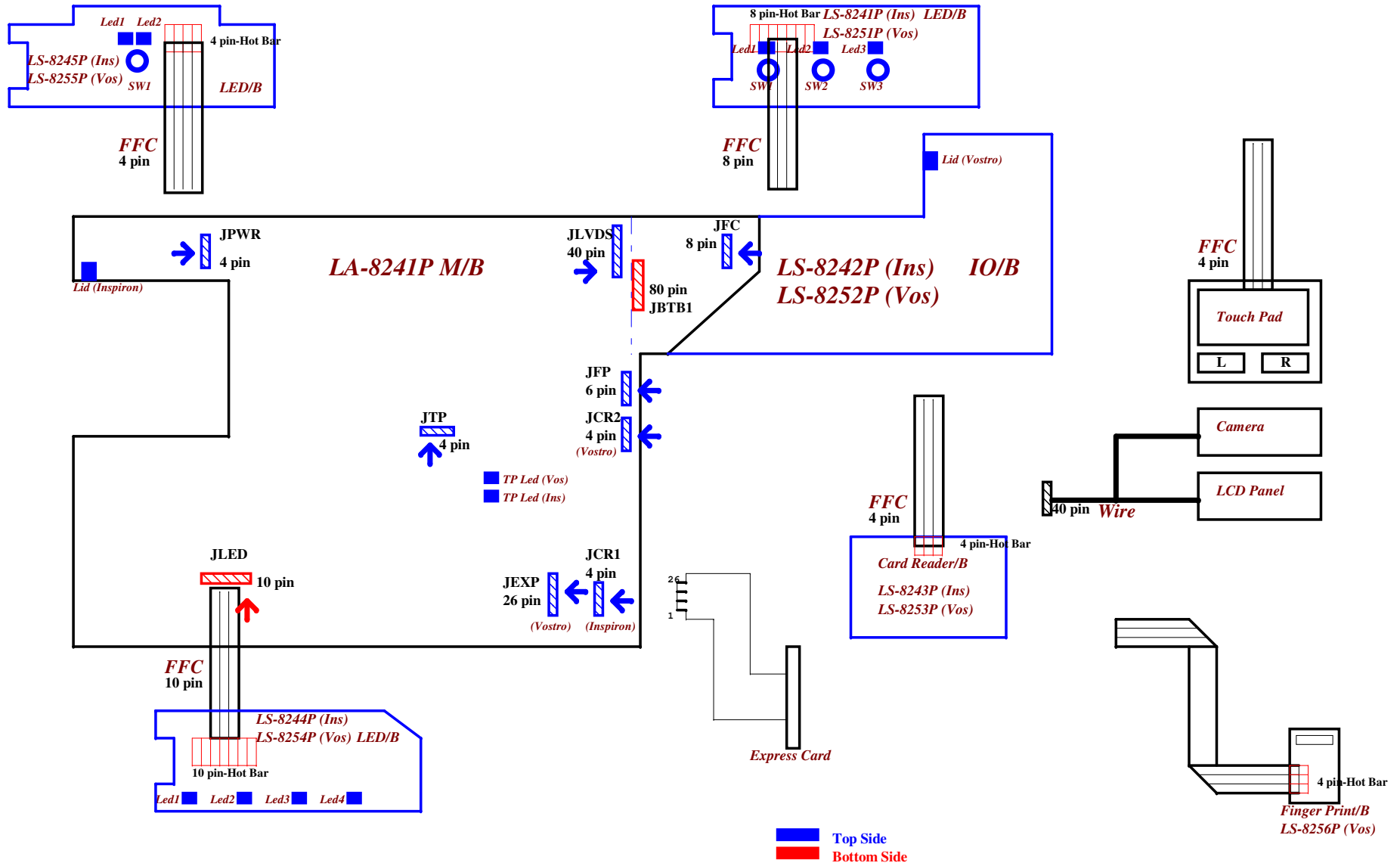
only for Vostro 3560

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Size	Document Number	Rev		
	LA-8241P	1.0		
Date:	Wednesday, February 01, 2012	Sheet	2	of 56

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				Rev
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Date: Wednesday, February 01, 2012				Sheet 3 of 56

Board ID Table for AD channel

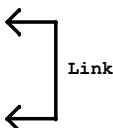
Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	V _{AD_BID min}	V _{AD_BID typ}	V _{AD_BID max}	EC_AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision		
0	0.1		
1		0.1	
2	0.2		
3		0.2	
4	0.3		0.2
5		0.3	0.3
6	1.0		1.0
7		1.0	

SMBUS Control Table

	SOURCE	MINI1	MINI2	BATT	SODIMM	Express Card	Thermal Sensor	FFS	VGA Thermal Sensor	VGA	XDP	Charger
EC_SMB_CK1 EC_SMB_DA1	KB9012			V								V
EC_SMB_CK2 EC_SMB_DA2	KB9012								V	V		
PCH_SML0CLK PCH_SML0DATA	PCH											
PCH_SML1CLK PCH_SML1DATA	PCH											
MEM_SMBCLK MEM_SMBDATA	PCH	V	V		V	V		V			V	



PCH	USB PORT#	DESTINATION
	0	USB conn.1
	1	USB conn.2 - Power Share
	2	USB conn.3
	3	USB conn.4
	4	MINI CARD-1 (WLAN)
	5	NC
	6	NC
	7	NC
	8	Finger Print
	9	NC
	10	Card Reader
	11	Express Card
	12	Camera
13	NC	

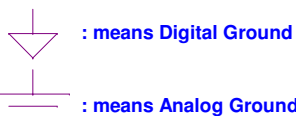
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

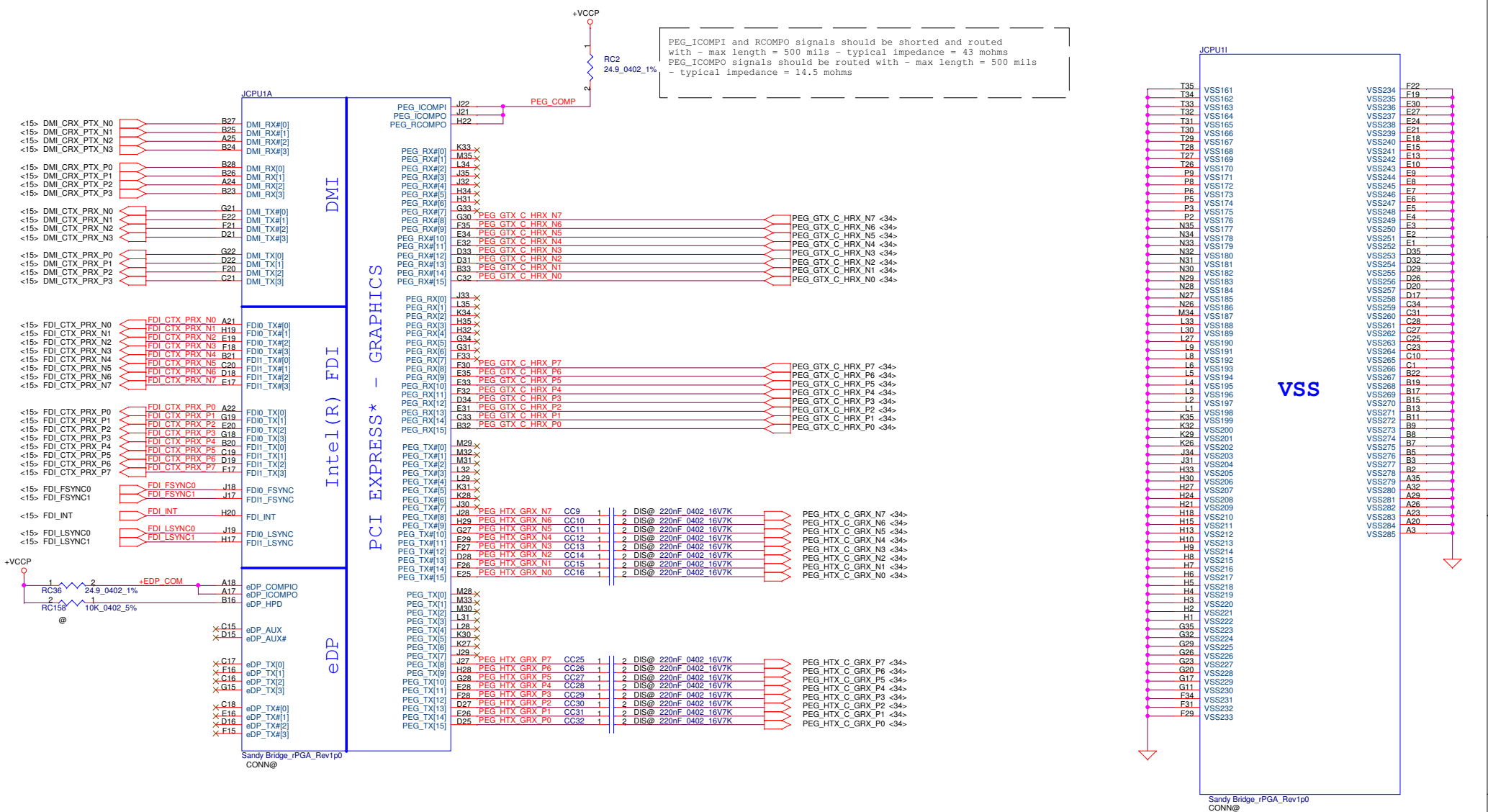
SATA	DESTINATION
SATA0	HDD
SATA1	SSD
SATA2	ODD
SATA3	None
SATA4	None
SATA5	None

PCI EXPRESS	DESTINATION
Lane 1	10/100/1G LAN
Lane 2	MINI CARD-1 (WLAN)
Lane 3	Express Card
Lane 4	None
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

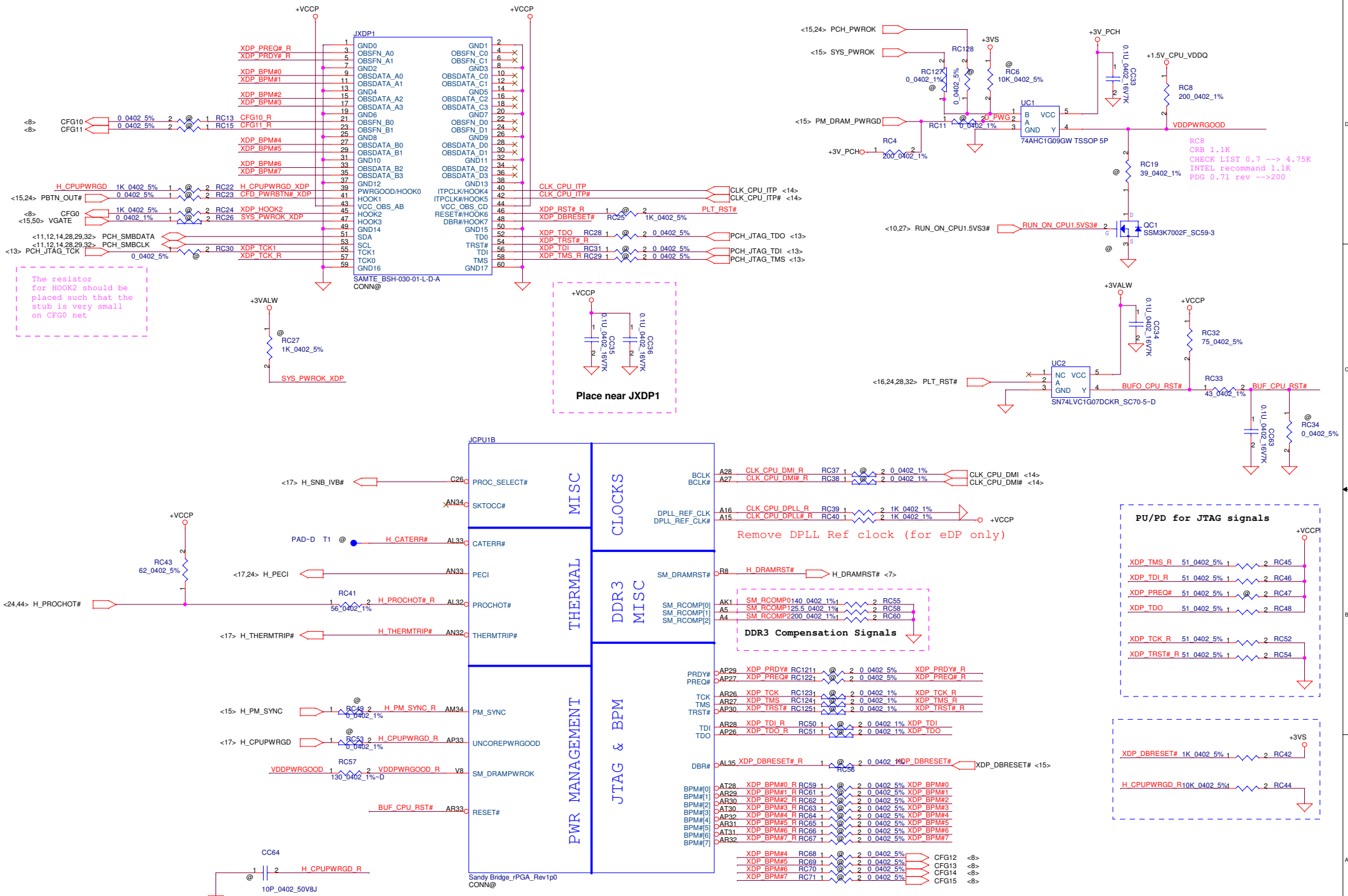
CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	10/100/1G LAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD-1 WLAN	CLKOUTFLEX1	None
	CLKOUT_PCIE2	Express Card	CLKOUTFLEX2	None
	CLKOUT_PCIE3	None	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
CLKOUT_PCIE7	None			
CLKOUT_PEG_B	None			

Symbol Note :



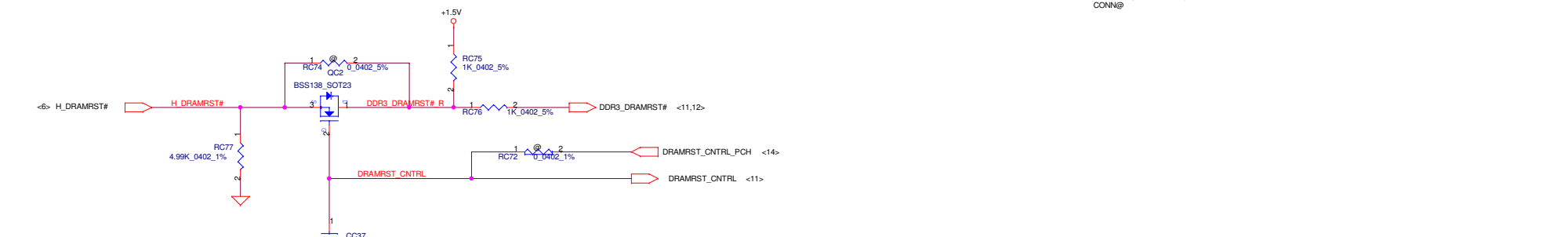
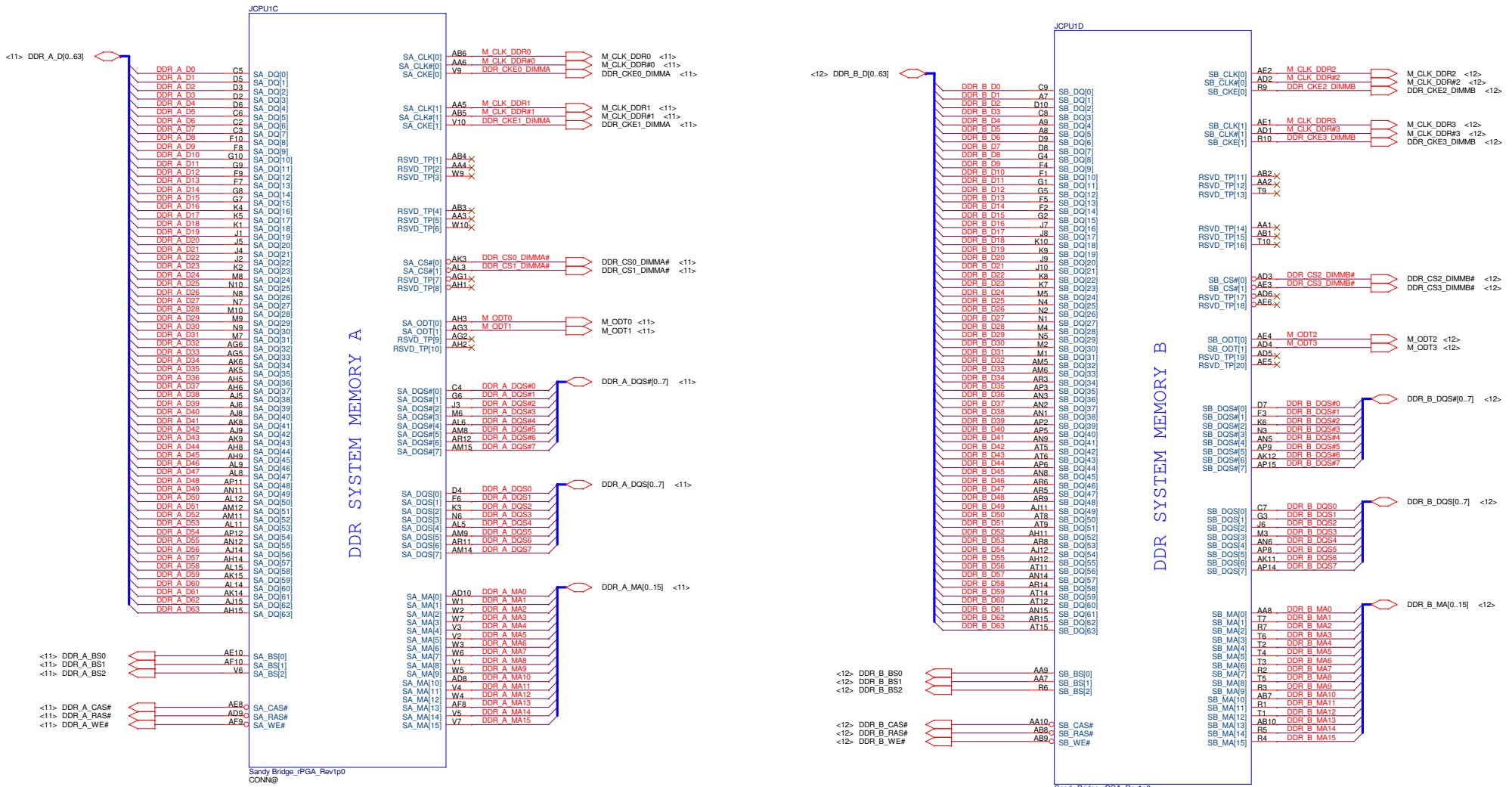


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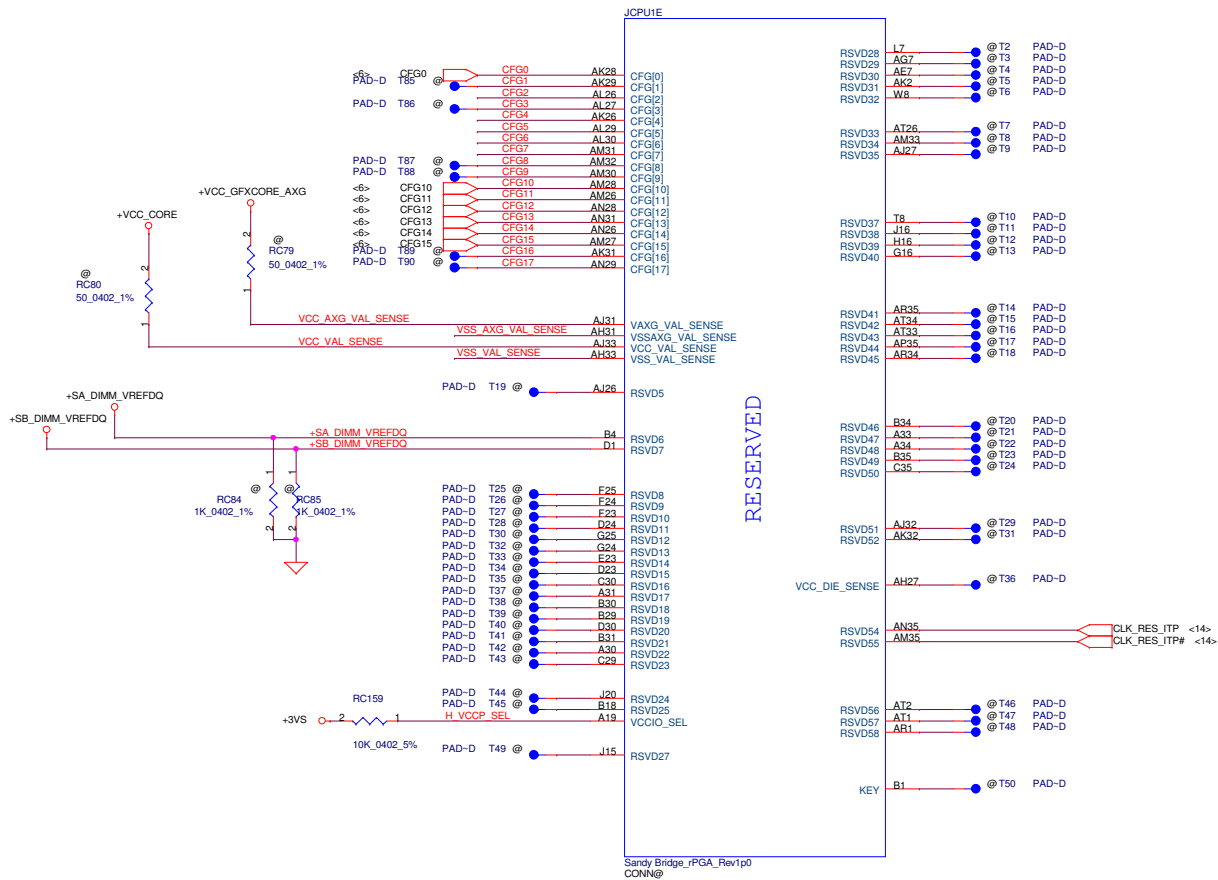
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				PROCESSOR(2/6) PM,XDP,CLK
				Document Number
				LA-8241P
				Rev
				1.0
				Date: Wednesday, February 01, 2012
				Sheet 6 of 56

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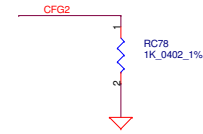


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				PROCESSOR(3/6) DDRIII
				Document Number
				LA-8241P
				Rev 1.0
				Date: Wednesday, February 01, 2012
				Sheet 7 of 56

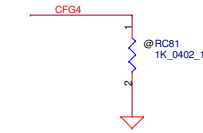
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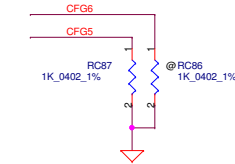
CFG Straps for Processor



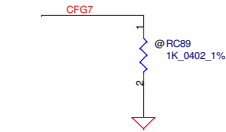
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1: (Default) Normal Operation; Lane # definition matches socket pin map definition *0: Lane Reversed



Display Port Presence Strap	
CFG4	*1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

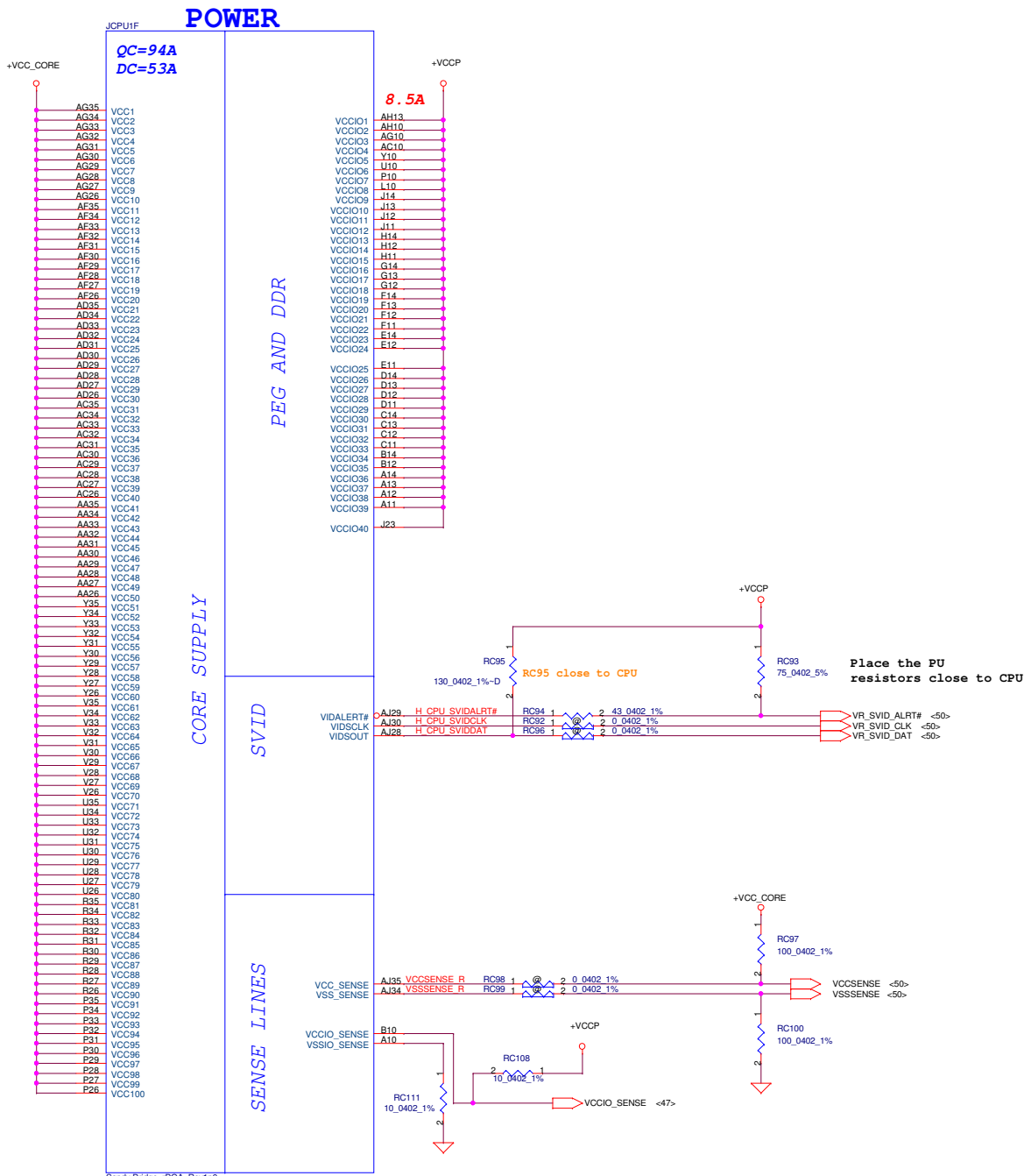


PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled *10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



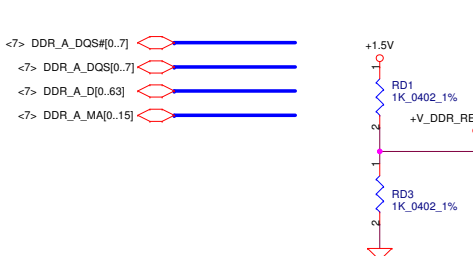
PEG DEFER TRAINING	
CFG7	*1: (Default) PEG Train immediately following xRESETB de assertion 0: PEG Wait for BIOS for training

INTEL 12/28 recommend
to add RC120, RC121, RC122, RC123
Please place as close as JCPU1



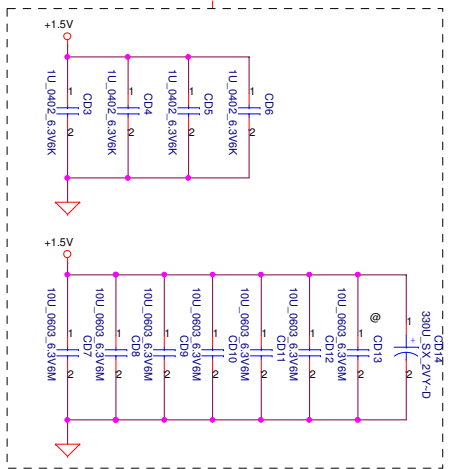
Sandy Bridge_rPGA_Rev1p0
CONN@

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				Rev 1.0

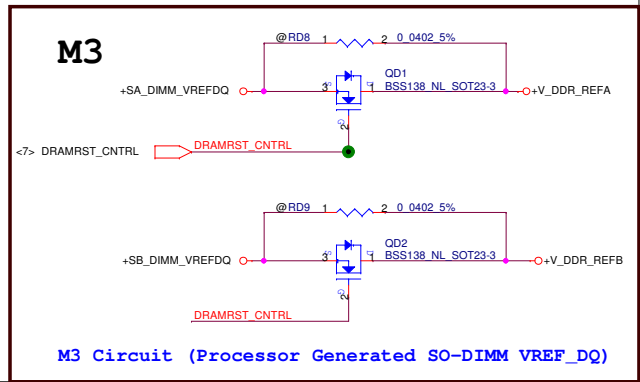
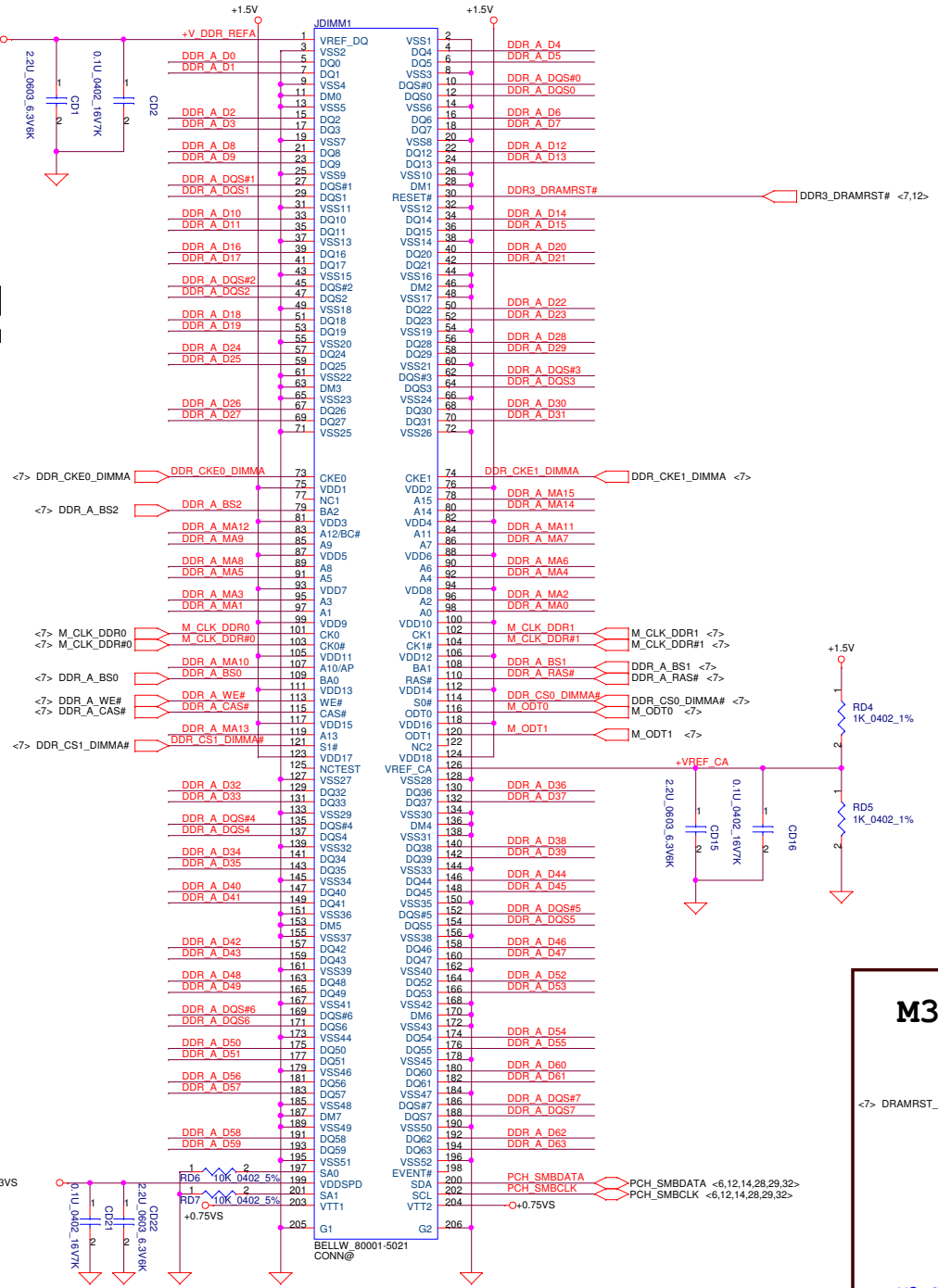
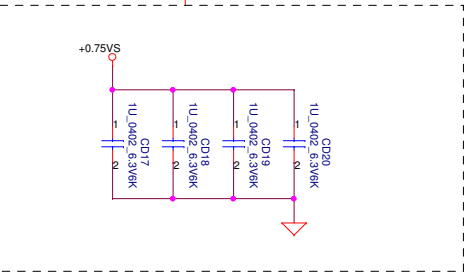


Layout Note:
Place near JDIMM1

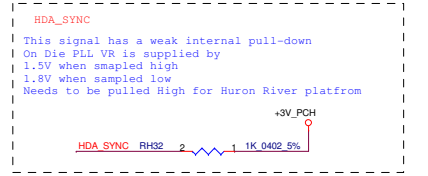
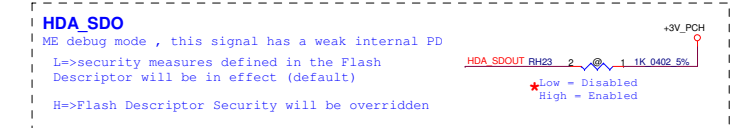
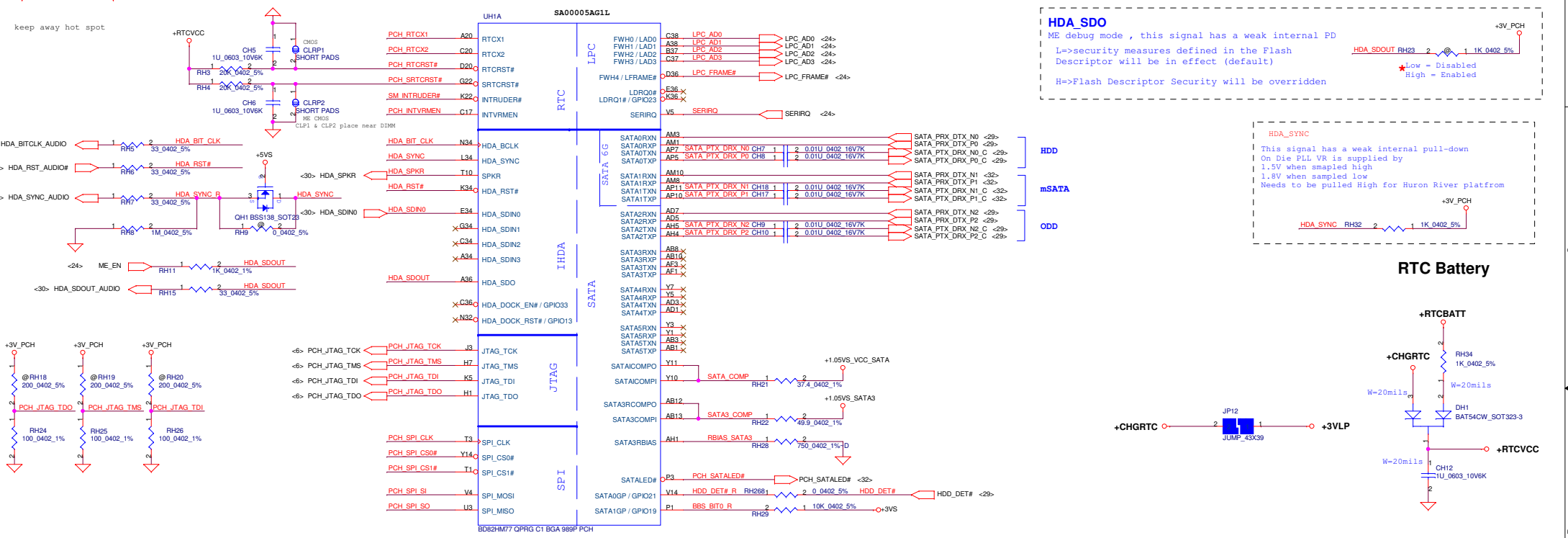
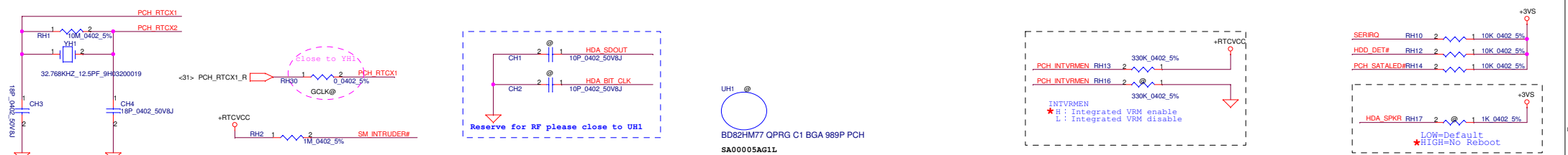
All VREF traces should have 10 mil trace width



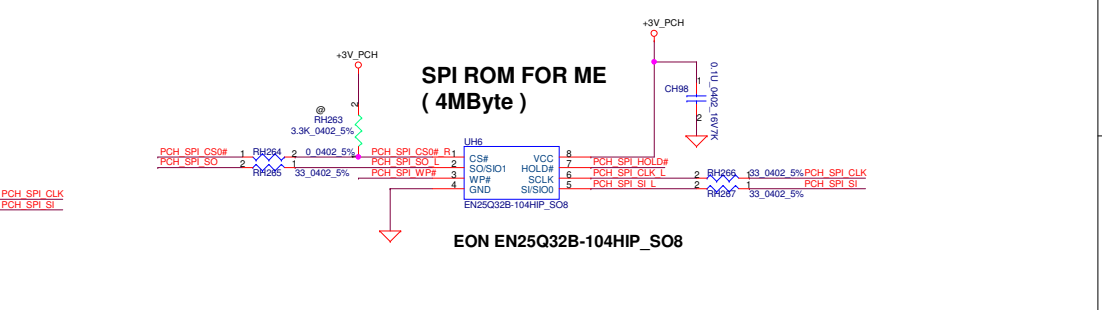
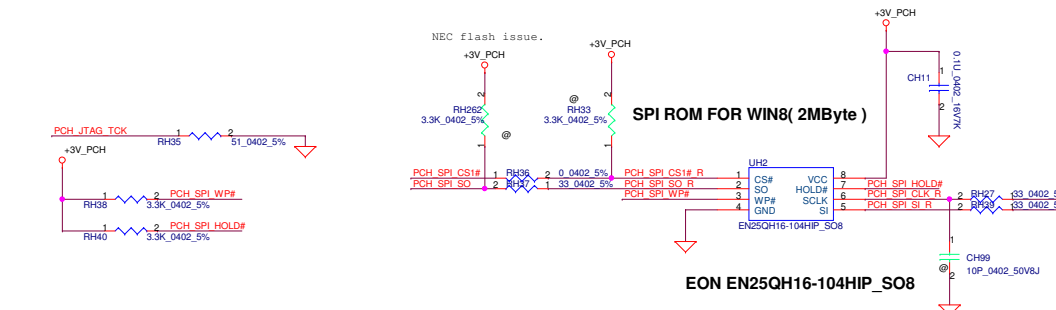
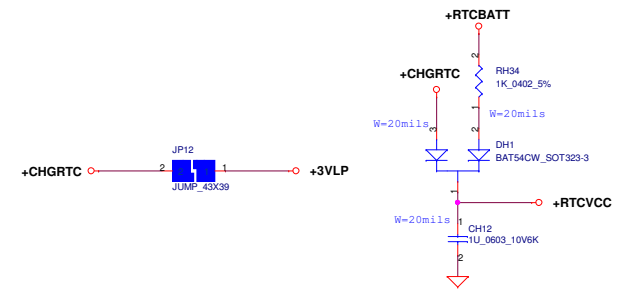
Layout Note:
Place near JDIMM1.203,204



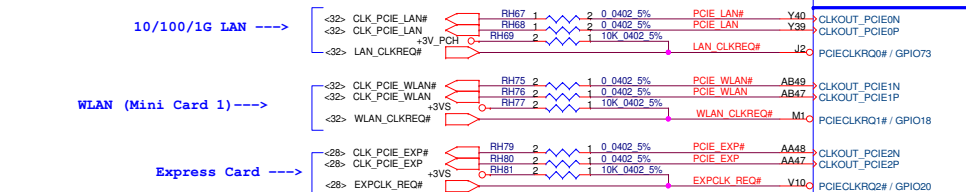
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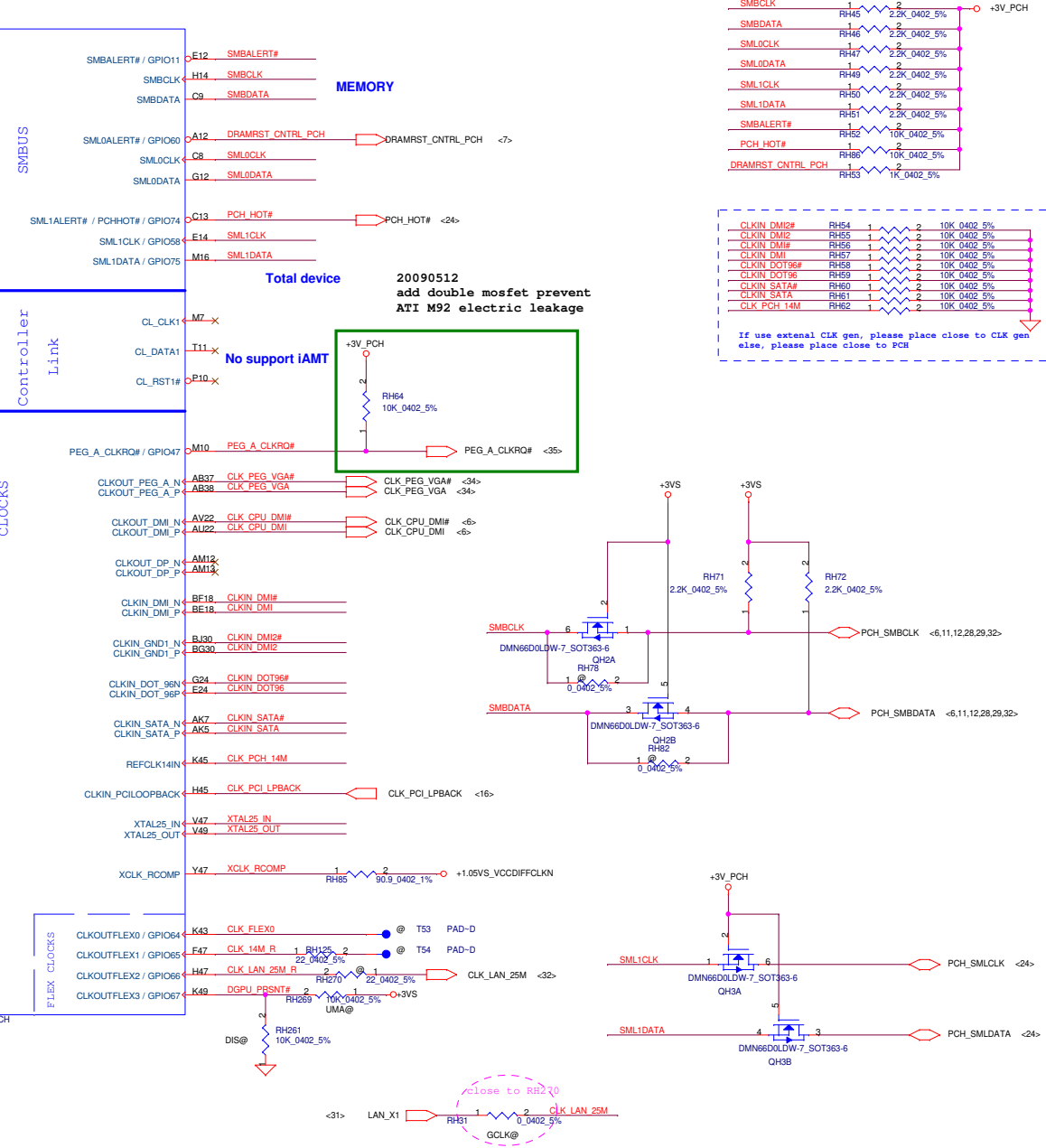
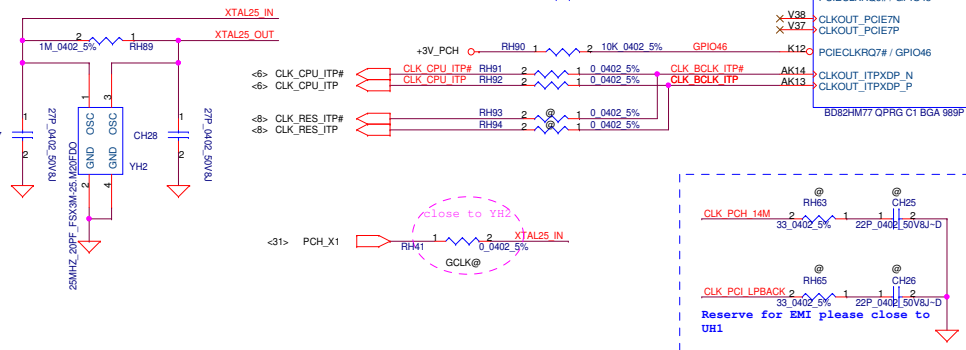
RTC Battery



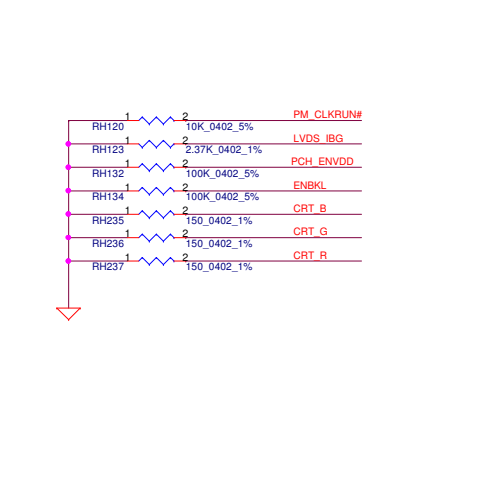
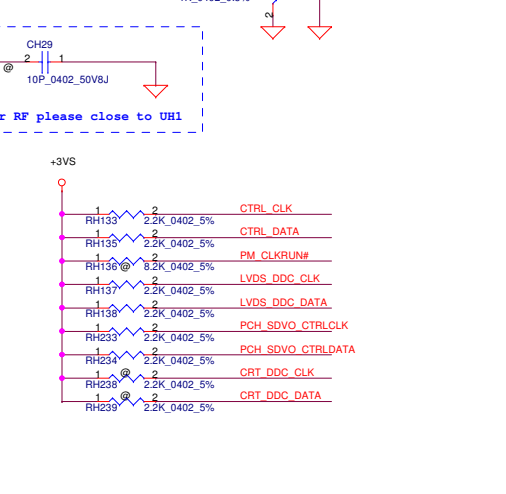
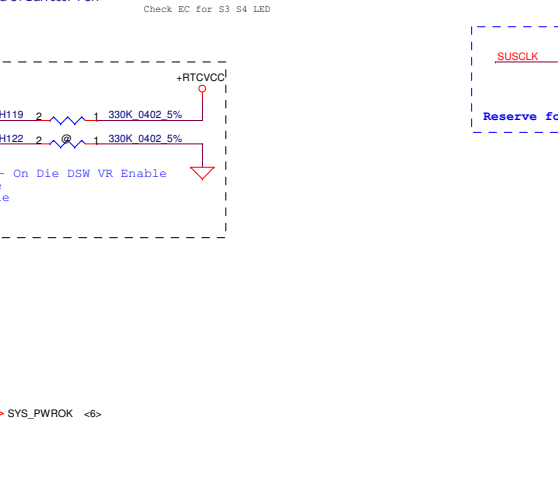
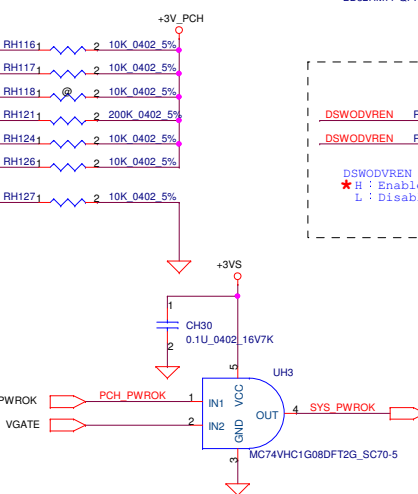
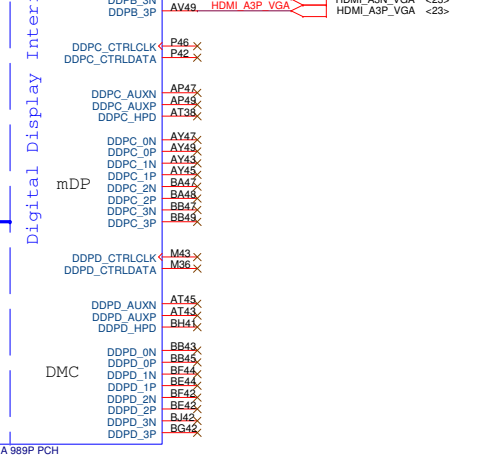
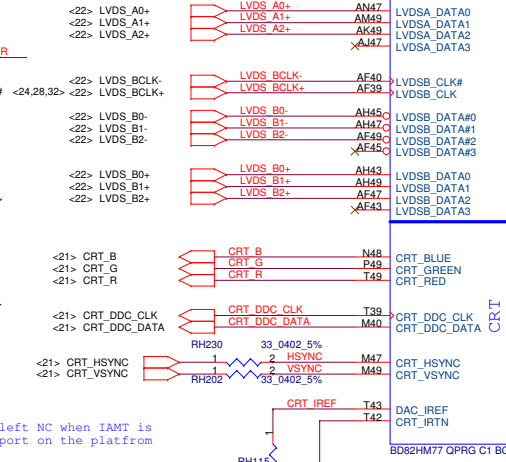
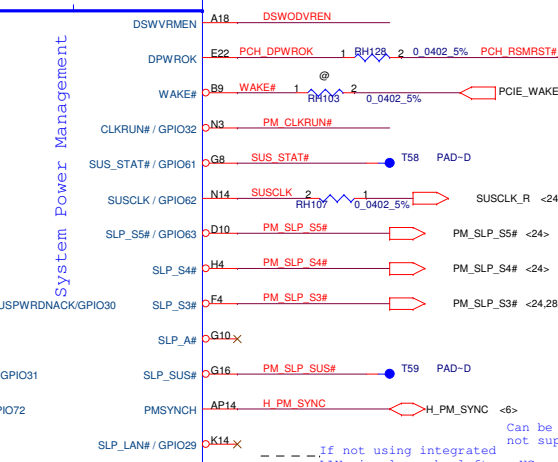
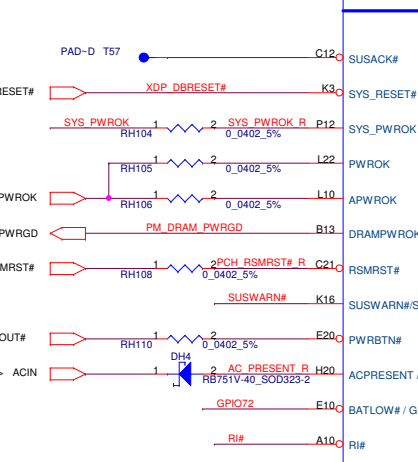
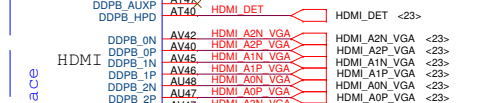
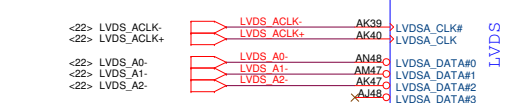
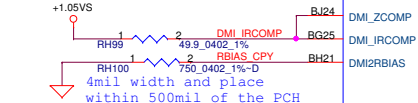
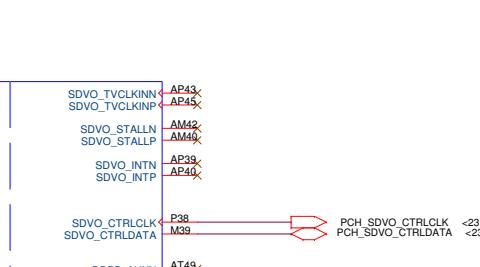
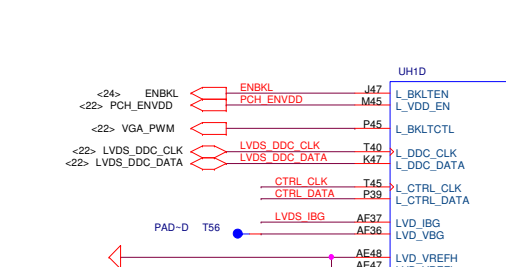
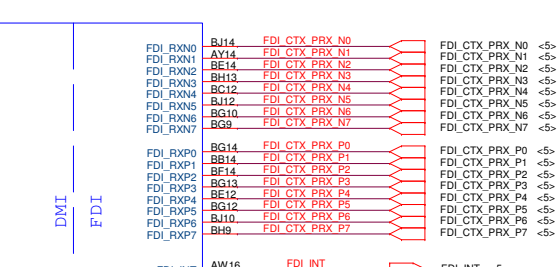
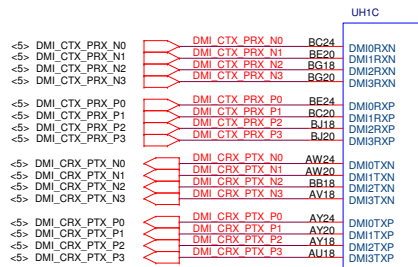
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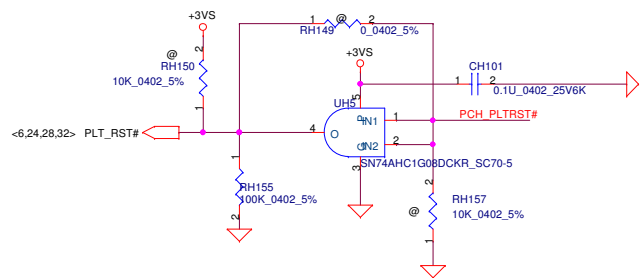
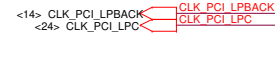
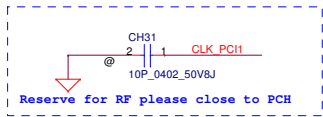
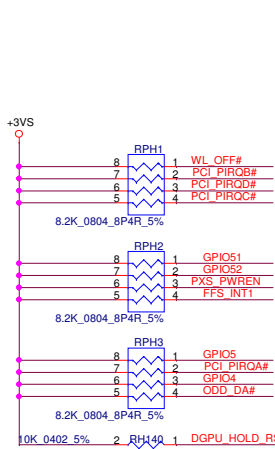
*PCIE REQ power rail:
suspend: 0 3 4 5 6 7
core: 1 2



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	LA-8241P	Wednesday, February 01, 2012	14 of 56	1.0



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				LA-8241P	Rev 1.0
				Date	Wednesday, February 01, 2012
				Sheet	15 of 56



- UH1E
- RSVD
- TP1 BG26
- TP2 BA26
- TP3 BH25
- TP4 BJ16
- TP5 BG16
- TP6 AH38
- TP7 AH37
- TP8 AK43
- TP9 AK45
- TP10 C18
- TP11 N30
- TP12 H3
- TP13 AH12
- TP14 AM5
- TP15 Y13
- TP16 K24
- TP17 L24
- TP18 AB46
- TP19 AB45
- TP20
- TP21 B21
- TP22 M20
- TP23 AY18
- TP24 BG46
- TP25 BE28
- TP26 BC30
- TP27 BE32
- TP28 BJ32
- TP29 BC28
- TP30 BE30
- TP31 BF32
- TP32 BG32
- TP33 AV28
- TP34 BB26
- TP35 AU28
- TP36 AY30
- TP37 AV26
- TP38 AV28
- TP39 AV28
- TP40 AW30

- PCI
- PIROA# K40C
- PIROB# K38C
- PIROC# H38C
- PIROD# G38C
- REQ1# / GPIO50
- REQ2# / GPIO52
- REQ3# / GPIO54
- GNT1# / GPIO51
- GNT2# / GPIO53
- GNT3# / GPIO55
- PIROE# / GPIO2
- PIROF# / GPIO3
- PIROG# / GPIO4
- PIROH# / GPIO5

- USB
- USBP0N C24
- USBP0P A24
- USBP1N B25
- USBP1P A26
- USBP2N C26
- USBP2P K26
- USBP3N H28
- USBP3P E28
- USBP4N D28
- USBP4P A28
- USBP5P C29
- USBP5P B29
- USBP6N N28
- USBP6P M28
- USBP7N L30
- USBP7P K30
- USBP8N E30
- USBP8P C30
- USBP9N A30
- USBP9P L32
- USBP10N K32
- USBP10P G32
- USBP11N E32
- USBP11P C32
- USBP12N A32
- USBP12P X32
- USBP13N
- USBP13P
- USB20_N0 <-32>
- USB20_P0 <-32>
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- USB20_N10 <-32>
- USB20_P10 <-32>
- USB20_N11 <-28>
- USB20_P11 <-28>
- USB20_N12 <-22>
- USB20_P12 <-22>

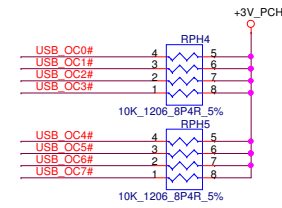
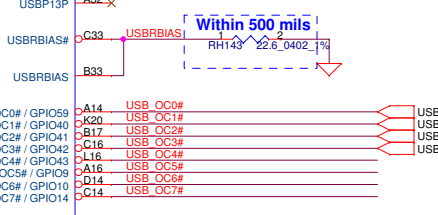
BD82HM77 QPRG C1 BGA 989P PCH

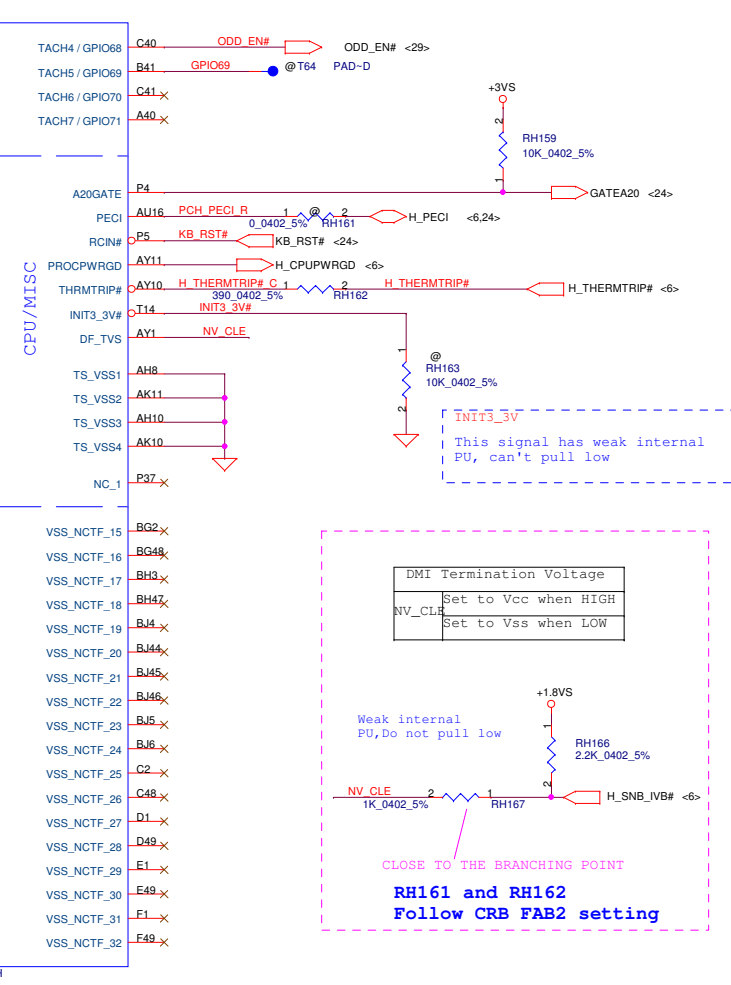
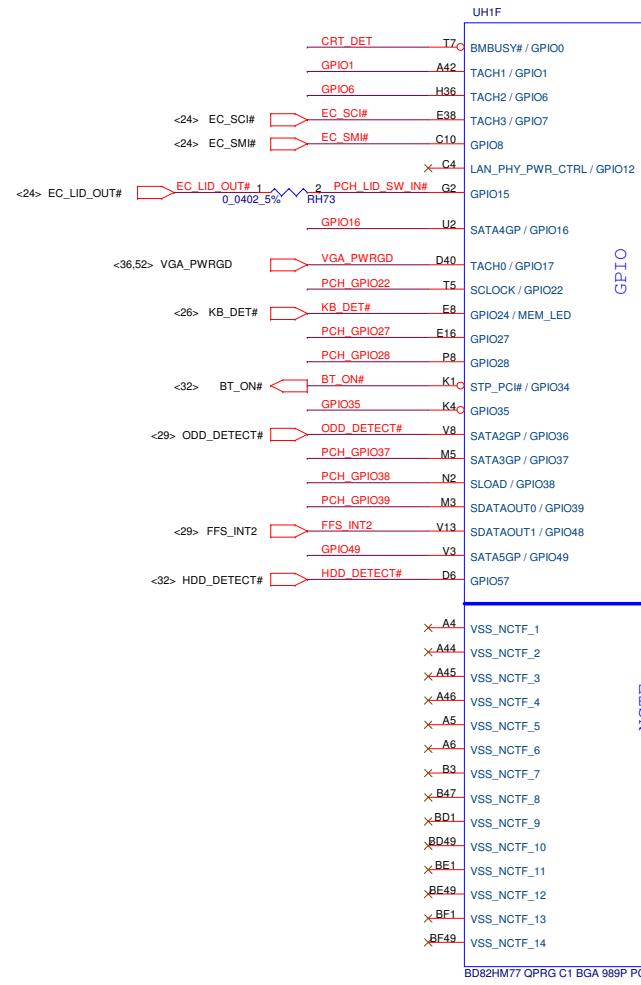
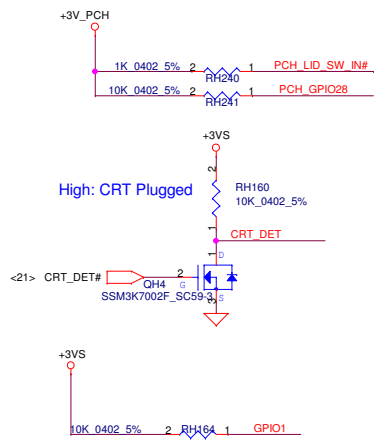
- RSVD1 CAV7
- RSVD2 CAV7
- RSVD3 CAU3
- RSVD4 CBG4
- RSVD5 AT10
- RSVD6 BCB
- RSVD7 AU2
- RSVD8 AT4
- RSVD9 AT13
- RSVD10 AT11
- RSVD11 AY3
- RSVD12 AT5
- RSVD13 AV3
- RSVD14 AV1
- RSVD15 BB1
- RSVD16 BA3
- RSVD17 BB5
- RSVD18 BB3
- RSVD19 BB7
- RSVD20 BE8
- RSVD21 BD4
- RSVD22 BFG
- RSVD23 AV5
- RSVD24 AV10
- RSVD25 AT8
- RSVD26 AV5
- RSVD27 BA2
- RSVD28 AT12
- RSVD29 BF3

Intel Anti-Theft Technology	
NV_ALE	High=Enabled
	Low=Disable (floating) *

- USB Conn 1
- USB Conn 2 (with PWR Share)
- USB Conn 3
- USB Conn 4
- Mini Card-1 (WLAN)
- Mini Card-2 (mSATA)

- Finger Print
- Card Reader
- Express Card
- Camera





GPIO28
On-Die PLL Voltage Regulator
This signal has a weak internal pull up
* H : On-Die voltage regulator enable
L : On-Die PLL Voltage Regulator disable

PCH_GPIO37
FDI TERMINATION VOLTAGE OVERRIDE
* LOW - Tx, Rx terminated to same voltage (DC Coupling Mode)

DMI Termination Voltage

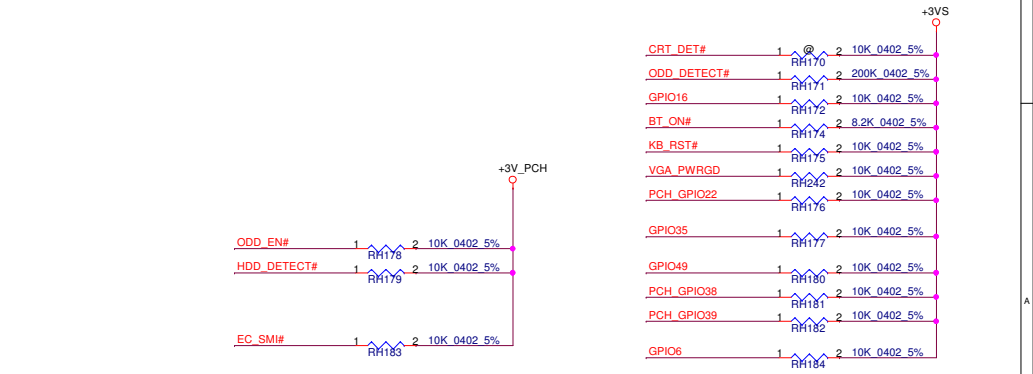
NV_CLE#	Set to Vcc when HIGH
	Set to Vss when LOW

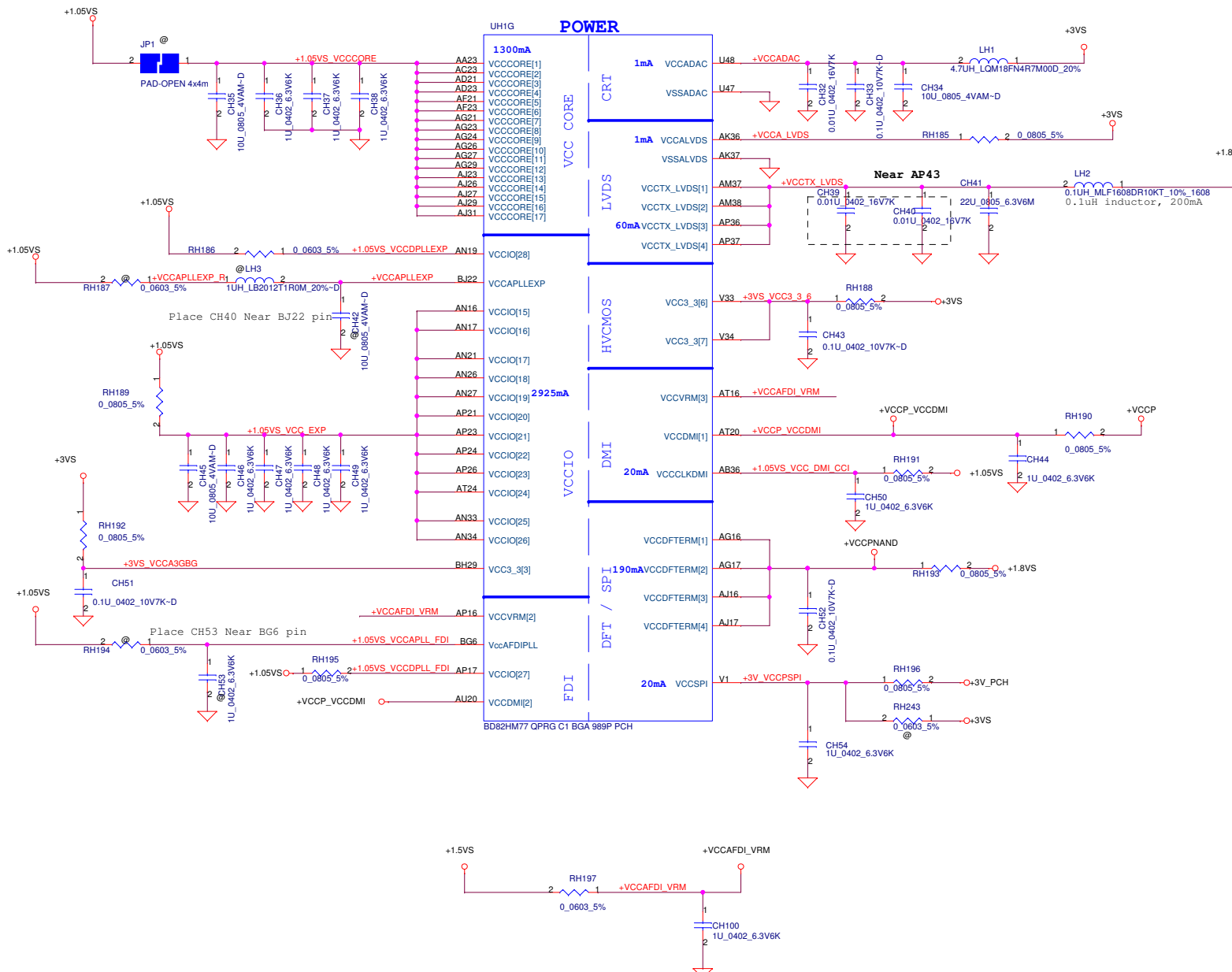
Weak internal PU, Do not pull low

CLOSE TO THE BRANCHING POINT
RH161 and RH162
Follow CRB FAB2 setting

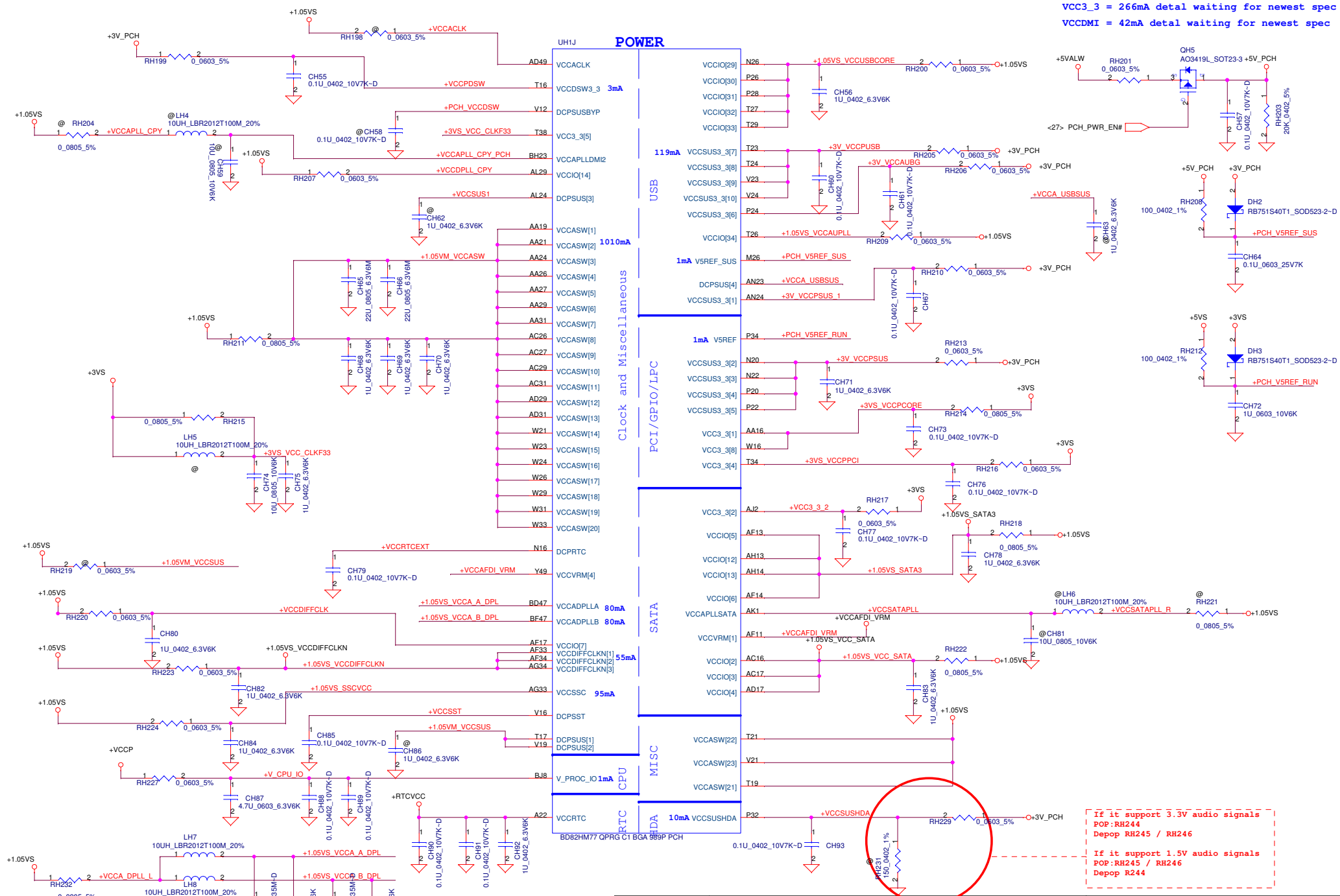
PCH_GPIO28 needs to be connected to XDP_FN8
PCH_GPIO35 needs to be connected to XDP_FN9
PCH_GPIO15 needs to be connected to XDP_FN16

Please refer to Huron River Debug Board DG 0.5





PCH Power Rail Table		
Voltage Rail	Voltage	SO Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_Sus	5	0.001
Vcc3_3	3.3	0.266
VccADAC	3.3	0.001
VccADPLL	1.05	0.08
VccADPLL	1.05	0.08
VccCore	1.05	1.3
VccDMI	1.05	0.042
VccIO	1.05	2.925
VccASW	1.05	1.01
VccSPI	3.3	0.02
VccDSW	3.3	0.003
VccpNAND	1.8	0.19
VccRTC	3.3	6 uA
VccSus3_3	3.3	0.119
VccSusHDA	3.3 / 1.5	0.01
VccVRM	1.8 / 1.5	0.16
VccCLKDMI	1.05	0.02
VccSSC	1.05	0.095
VccDIFFCLKN	1.05	0.055
VccALVDS	3.3	0.001
VccTX_LVDS	1.8	0.06

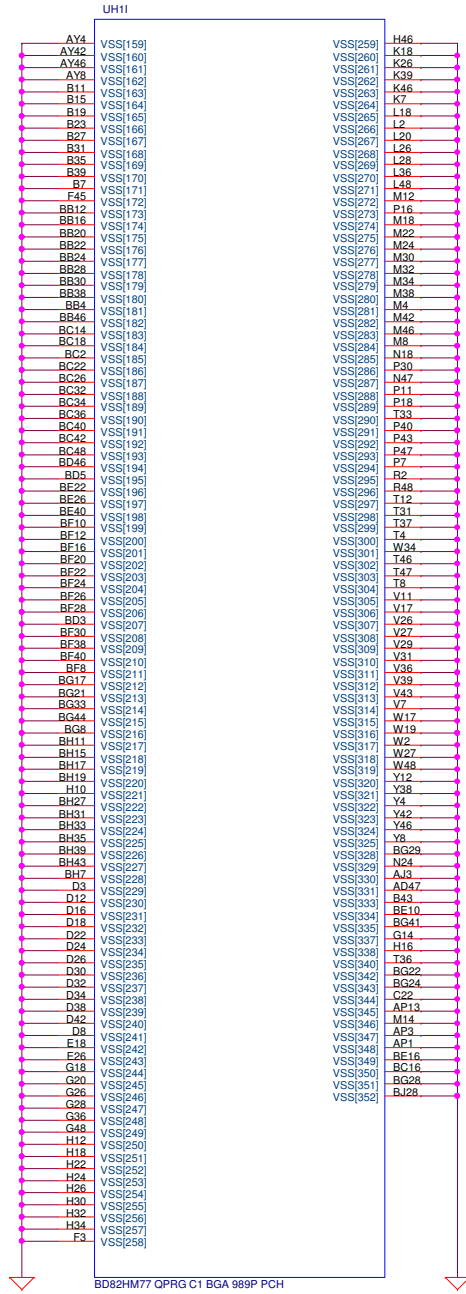
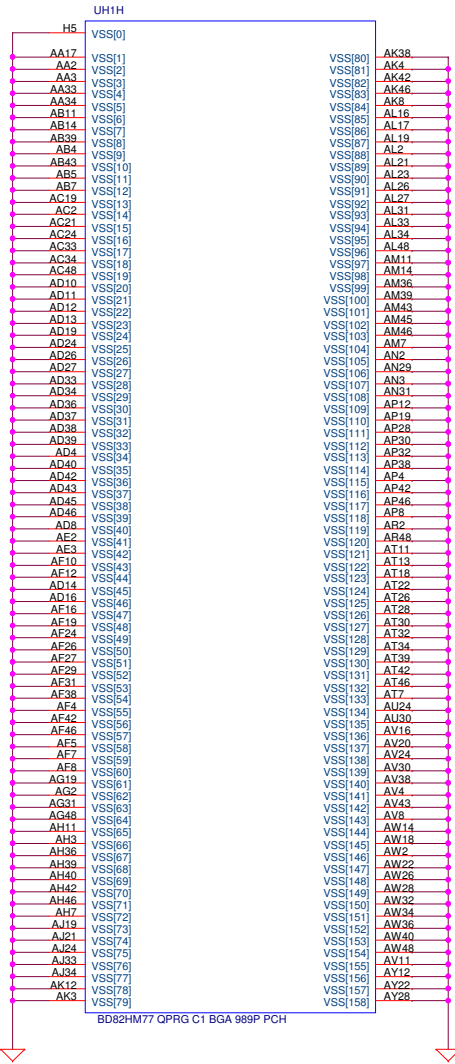


VCC3_3 = 266mA detail waiting for newest spec
 VCCDMI = 42mA detail waiting for newest spec

If it support 3.3V audio signals
 POP: RH244
 Depop RH245 / RH246

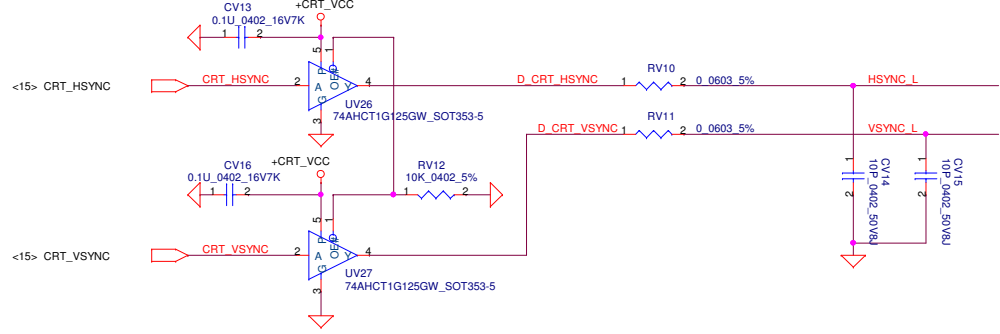
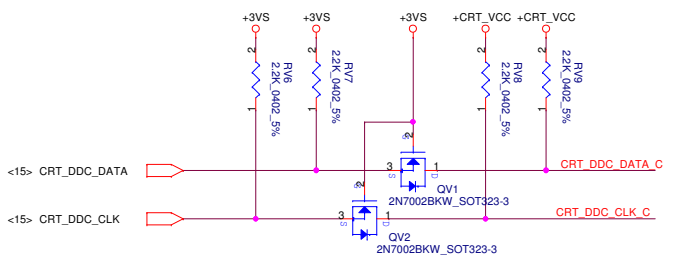
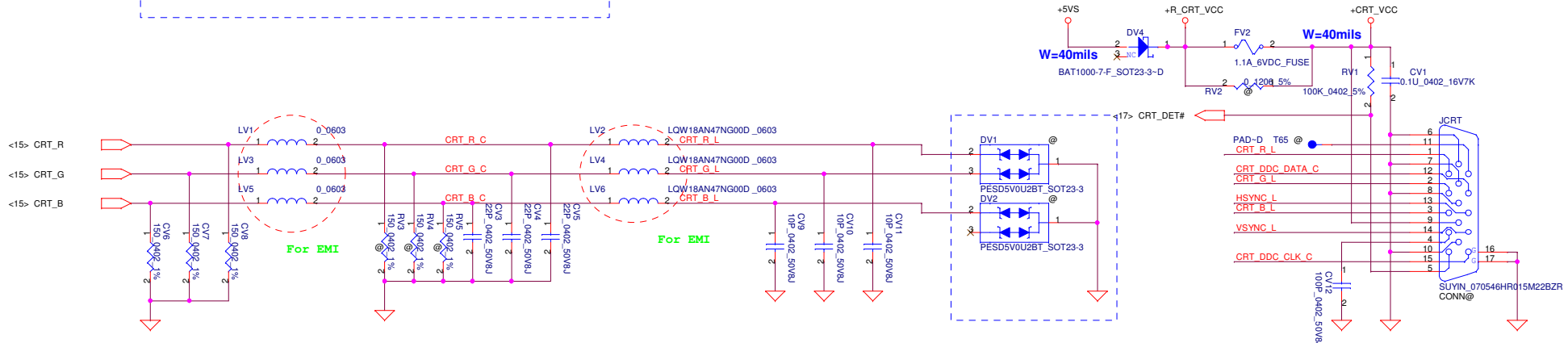
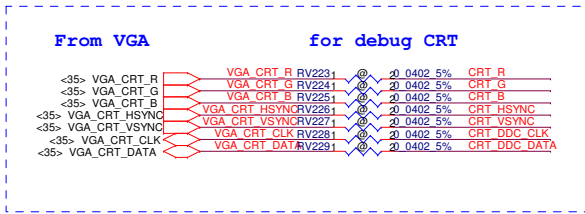
If it support 1.5V audio signals
 POP: RH245 / RH246
 Depop R244

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			LA-8241P		1.0
			Date:	Wednesday, February 01, 2012	Sheet 19 of 56



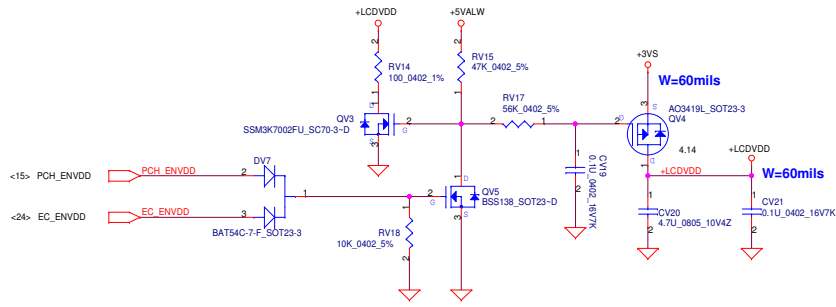
Security Classification	Compal Secret Data		Title	
Issued Date	2012/01/17	Deciphered Date	2013/01/16	PCH (8/8) VSS
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Date: Wednesday, February 01, 2012				Rev 1.0
Sheet 20 of 56				

CRT

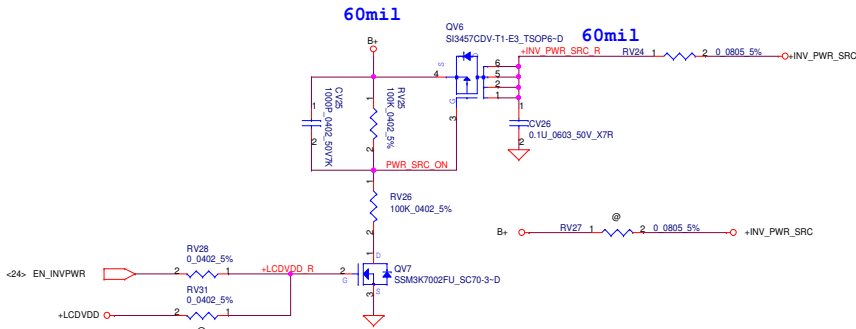


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Date: Wednesday, February 01, 2012				Sheet 21 of 56

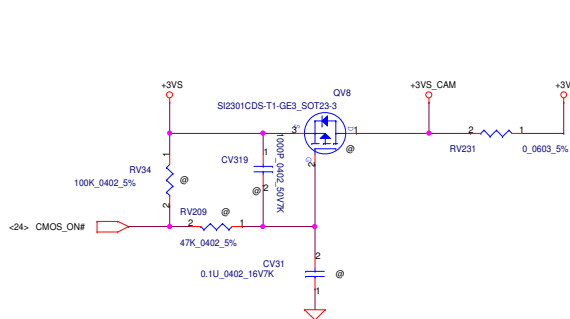
LCD PWR CTRL



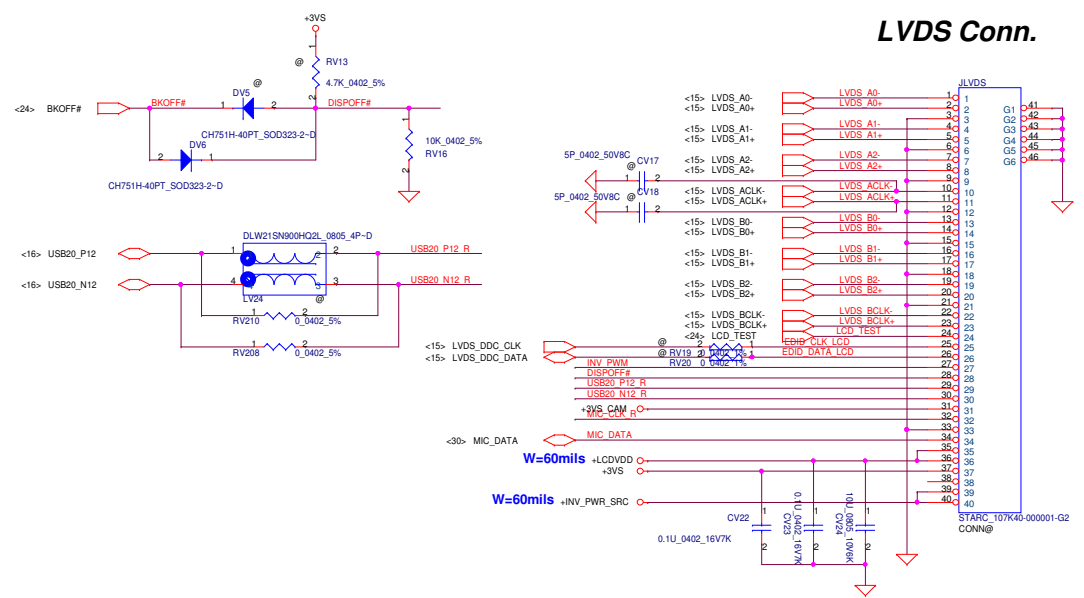
LCD backlight PWR CTRL



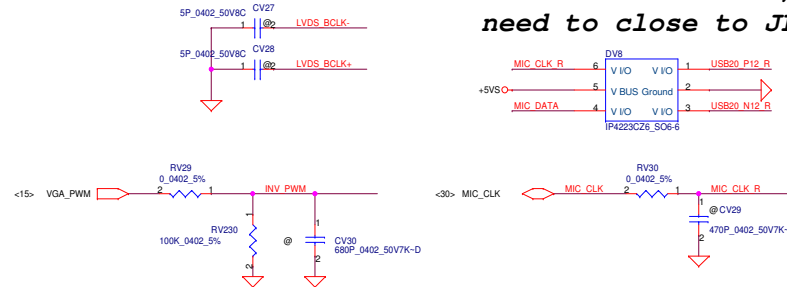
Wedcam PWR CTRL



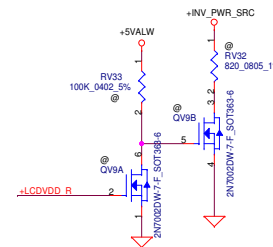
LVDS Conn.



*** Reserved for EMI/ESD/RF
need to close to JLVDs**

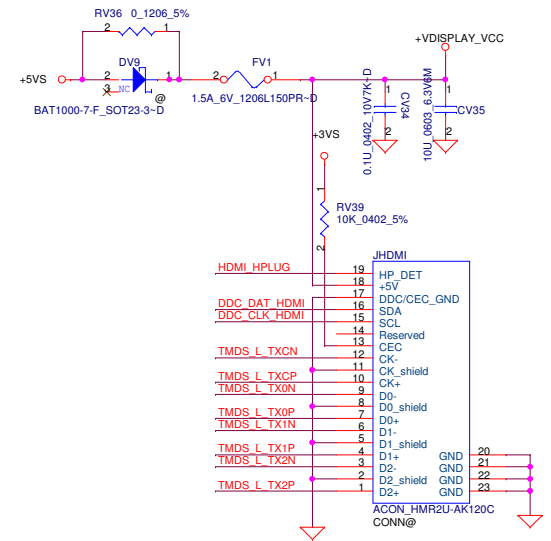
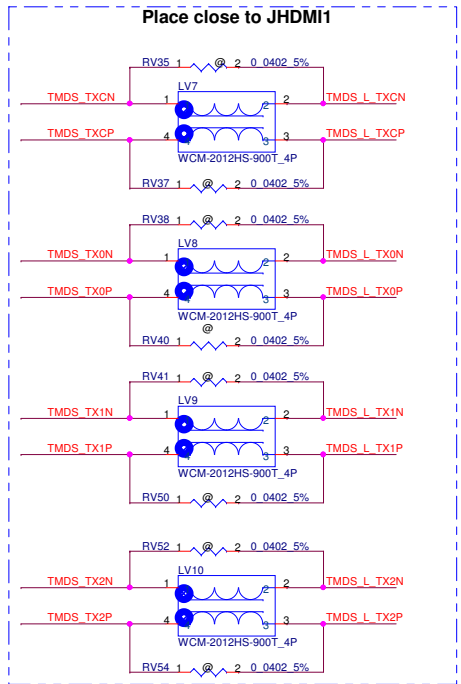
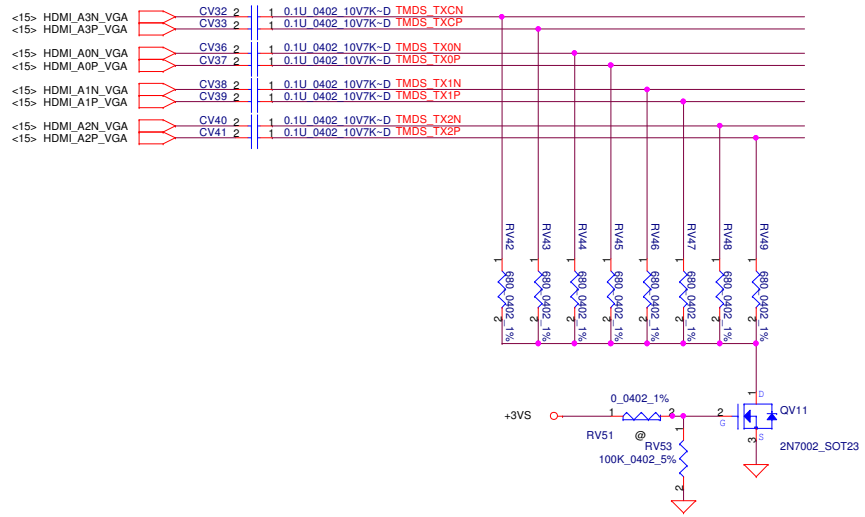


*** Reserved for LCD
sequence tuning**

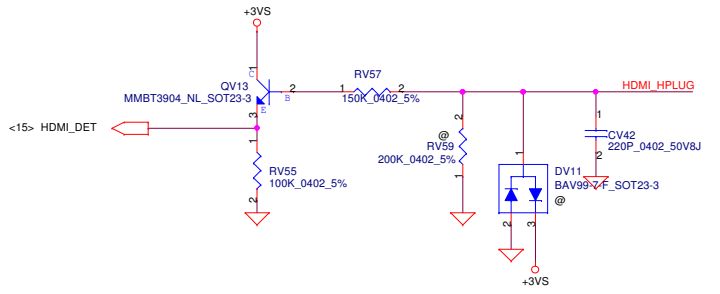
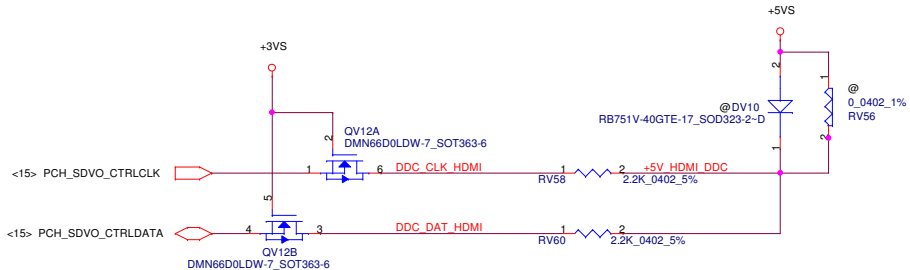
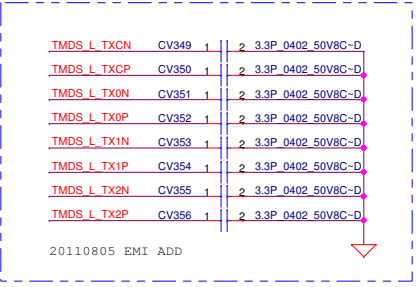
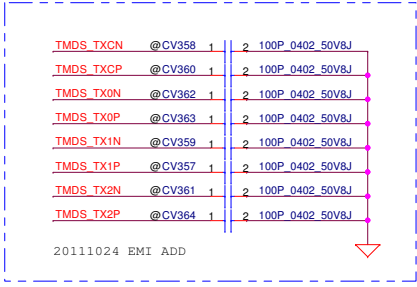


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Date: Wednesday, February 01, 2012				Rev 1.0
Sheet 22 of 56				

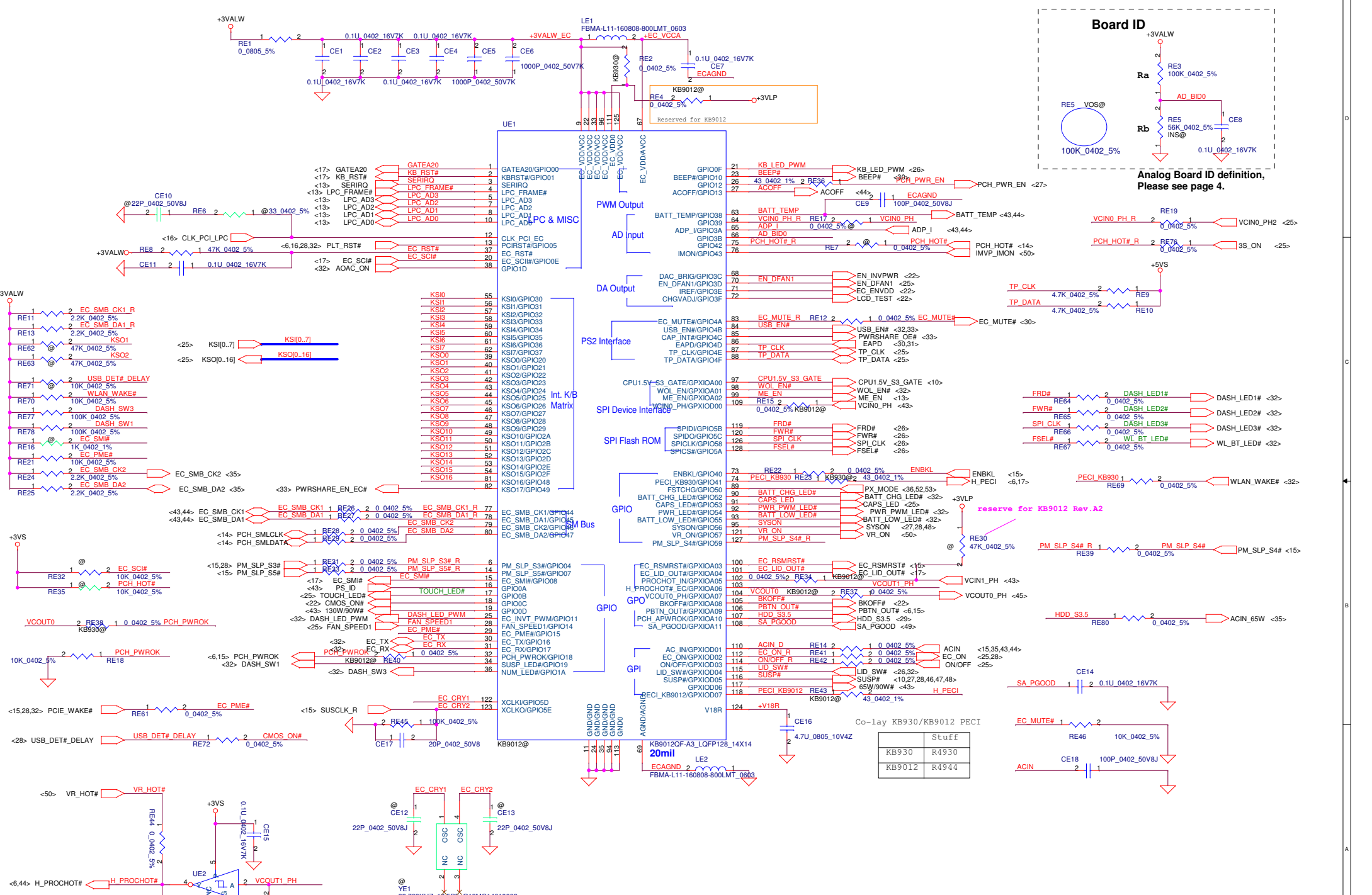
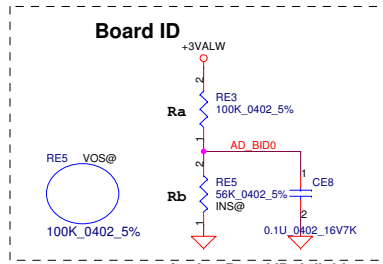
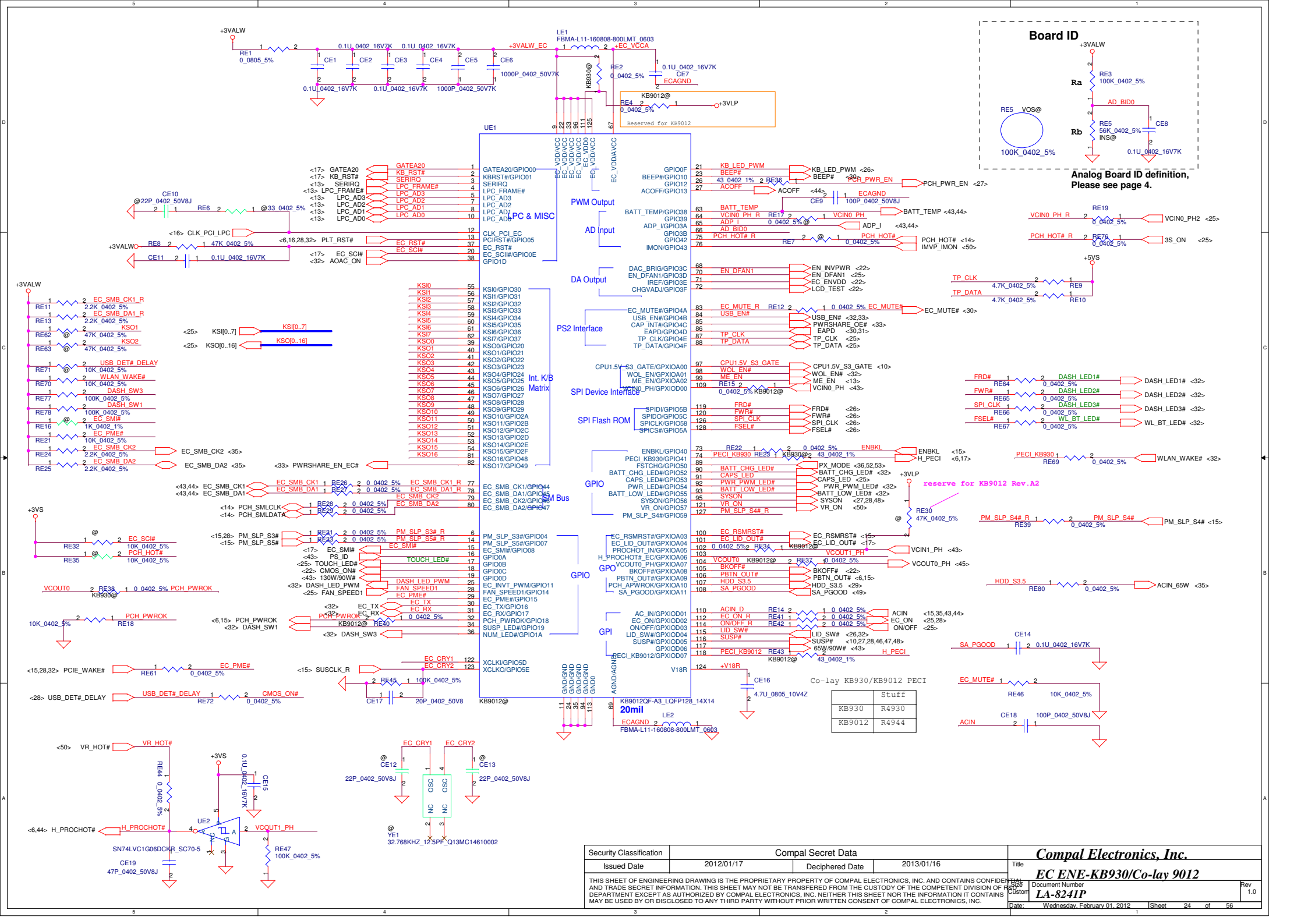
W=40mils



Part Number	Description
RO000002HM	ROYALTY HDMI W/LOGO
HDMI W/Logo:RO000002HM	



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Compal Electronics, Inc. HDMI				Rev 1.0 LA-824IP



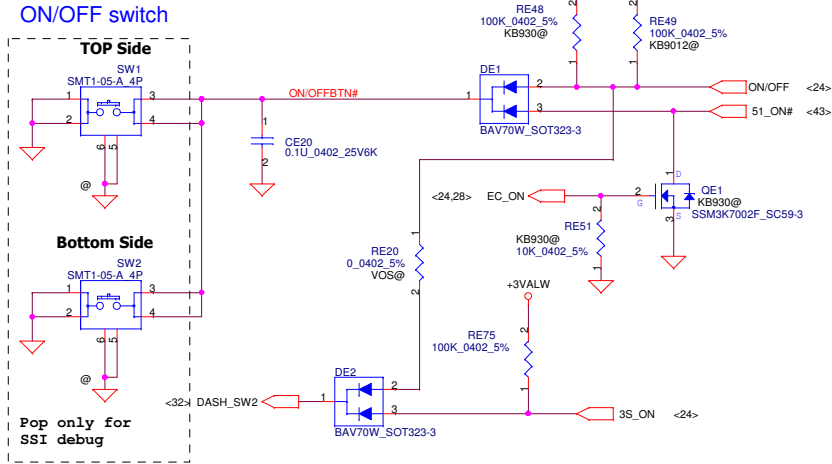
Security Classification	2012/01/17	Compal Secret Data	Deciphered Date	2013/01/16
Issued Date	2012/01/17			

Board ID	Value
KB9012QF-A3_LQFF128_14X14	20mil
ECAGND	2
KB9012	R4930
KB9012	R4944

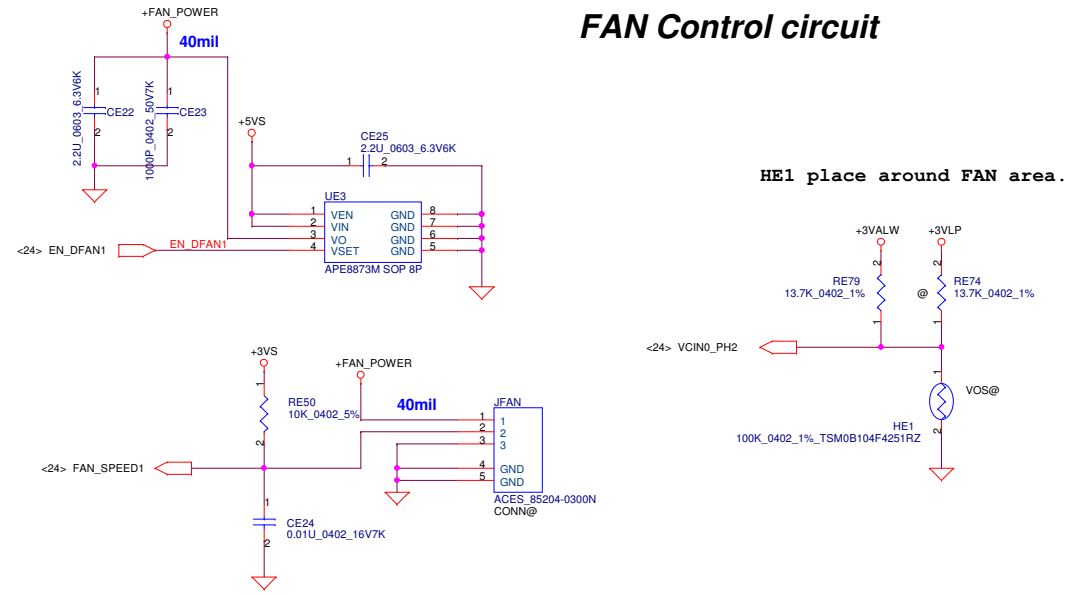
Item	Quantity	Part Number	Value
EC MUTE#	1	RE46	10K_0402_5%
ACIN	2	CE18	100P_0402_50V8J

Compal Electronics, Inc.
EC ENE-KB930/Co-lay 9012
 Document Number: LA-8241P
 Date: Wednesday, February 01, 2012 | Sheet 24 of 56

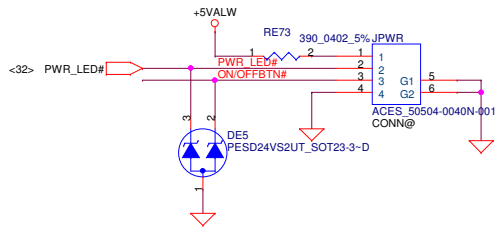
Power ON Circuit



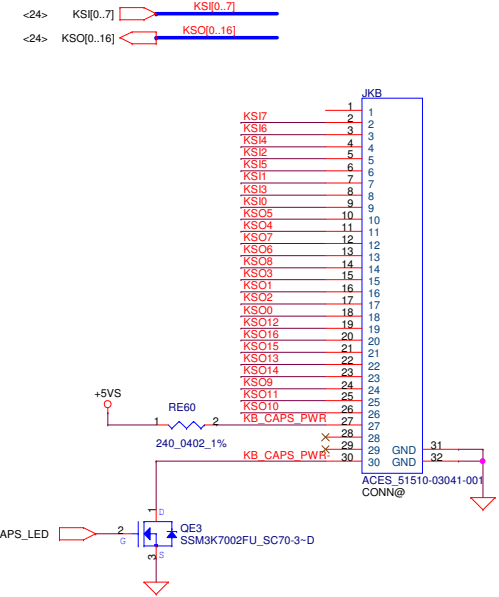
FAN Control circuit



To POWER/B

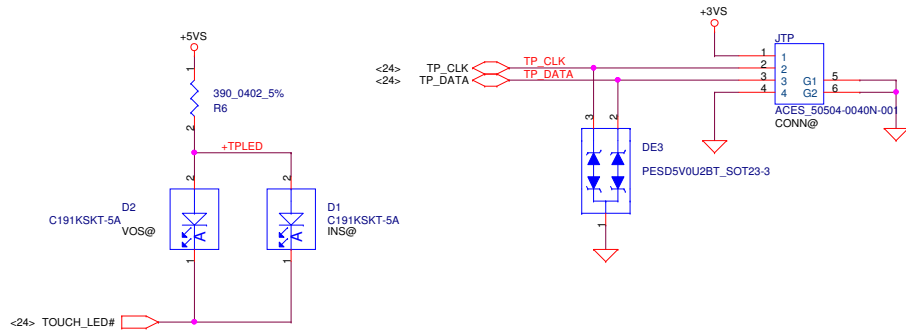


INT_KBD Conn.



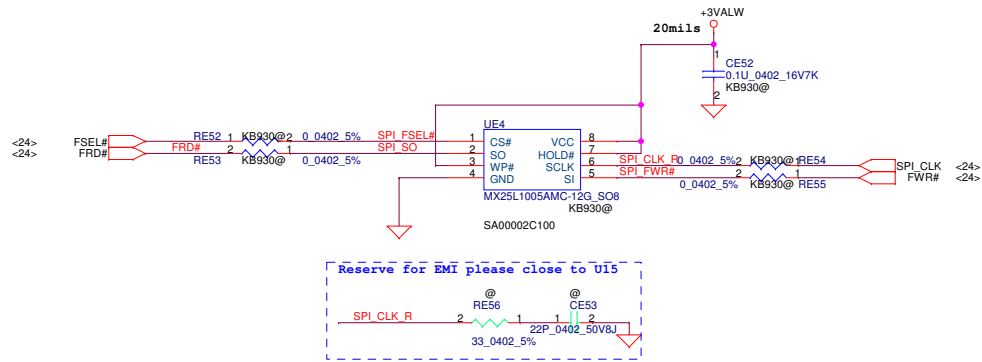
Touch Pad LED

Touch pad

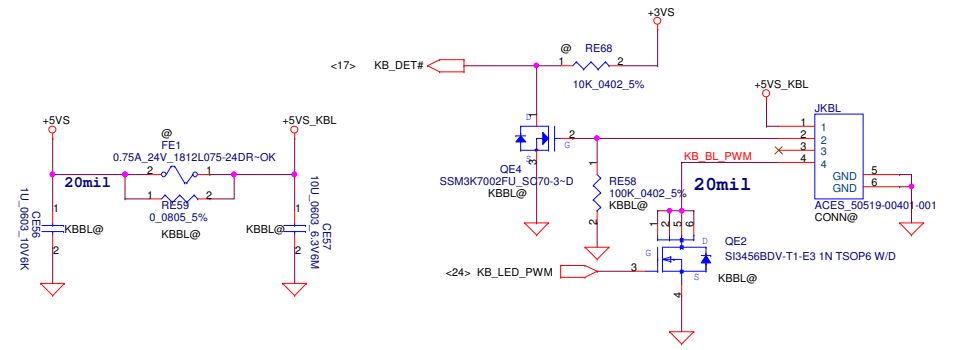


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Date:	Wednesday, February 01, 2012	Sheet	25	of	56

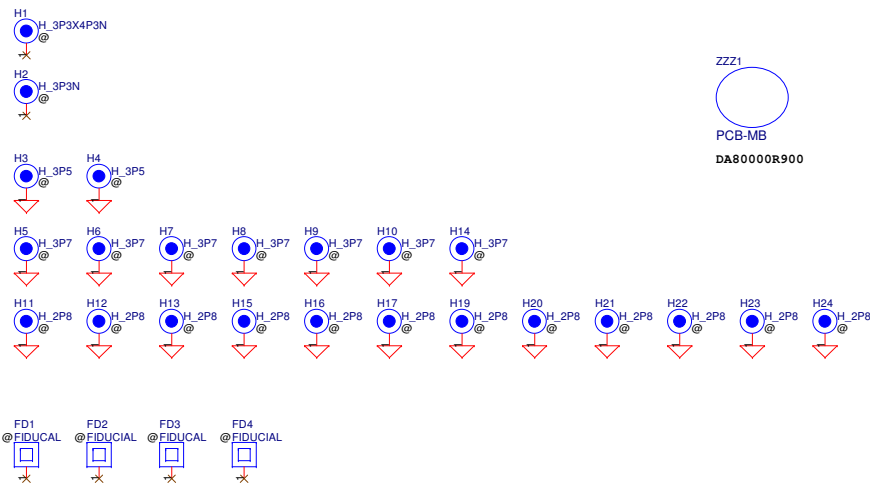
SPI ROM 128KB



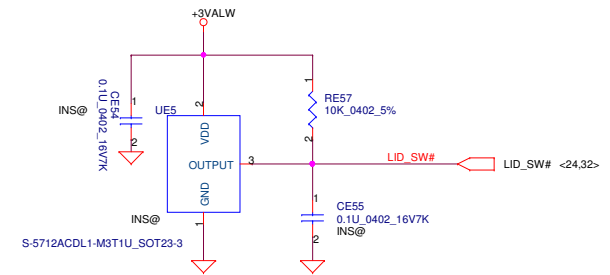
Keyboard back light



Screw Hole

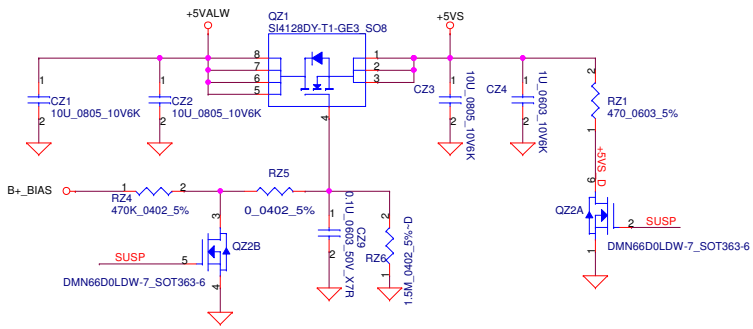


Lid Switch

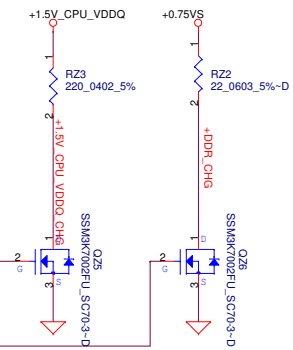
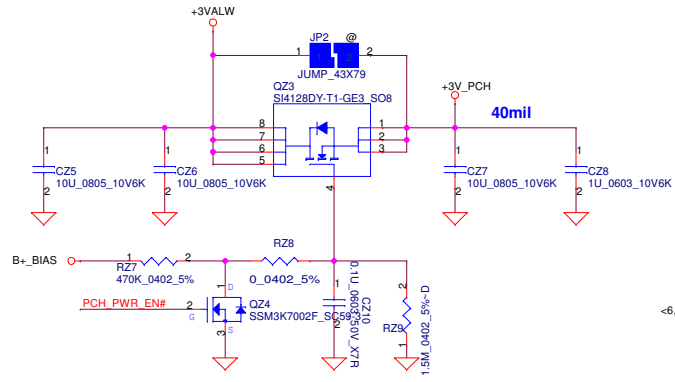


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				Rev 1.0

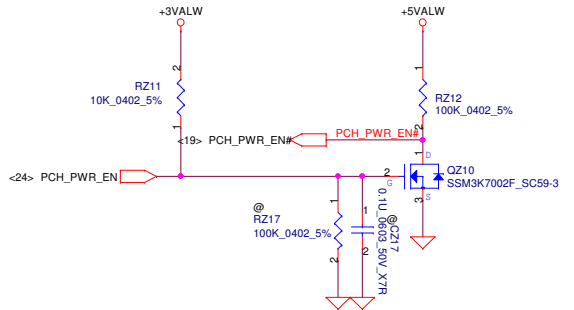
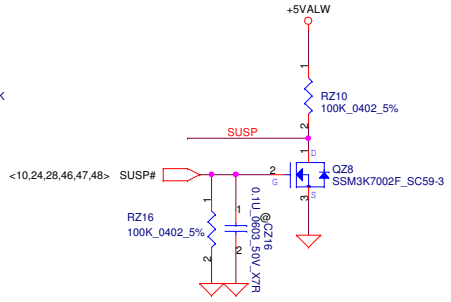
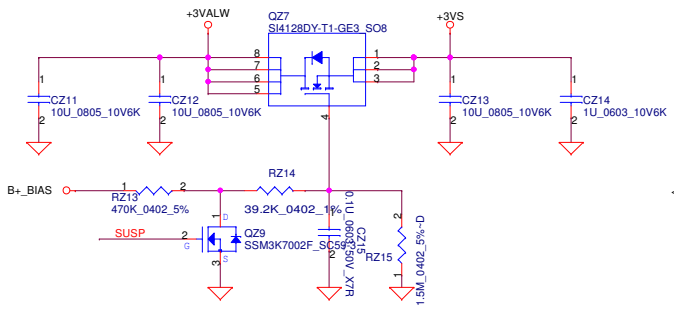
+5VALW to +5VS



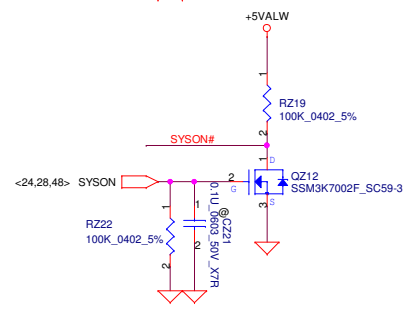
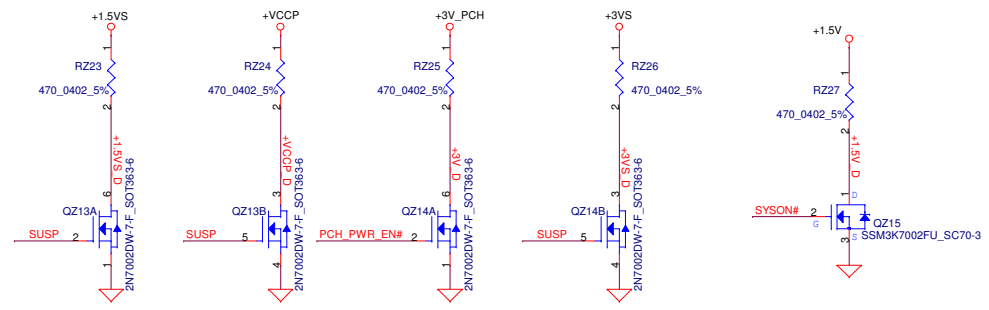
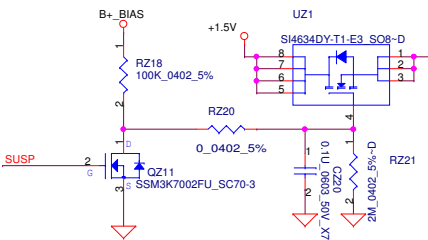
+3VALW to +3V_PCH



+3VALW to +3VS



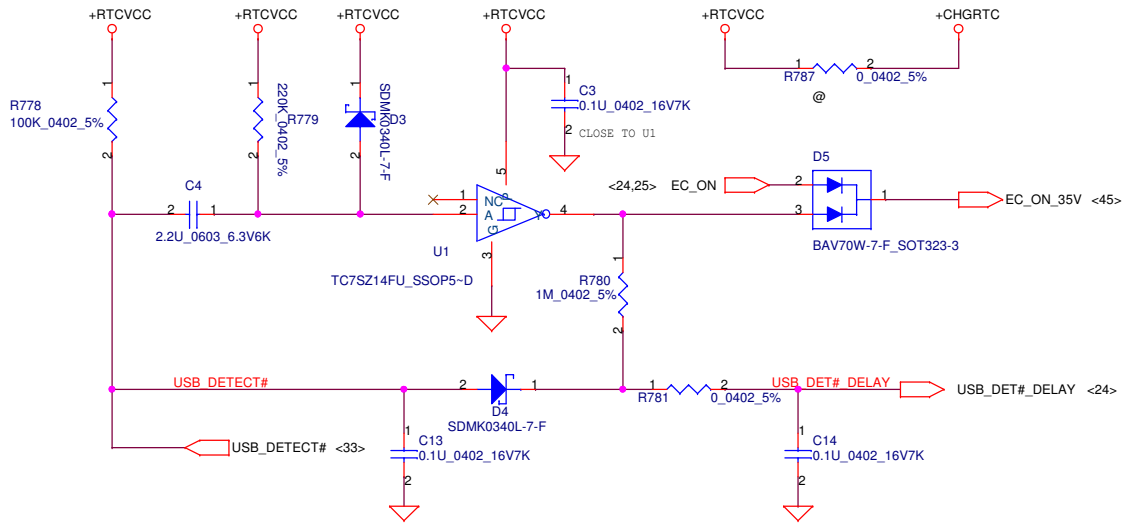
+1.5V To +1.5VS



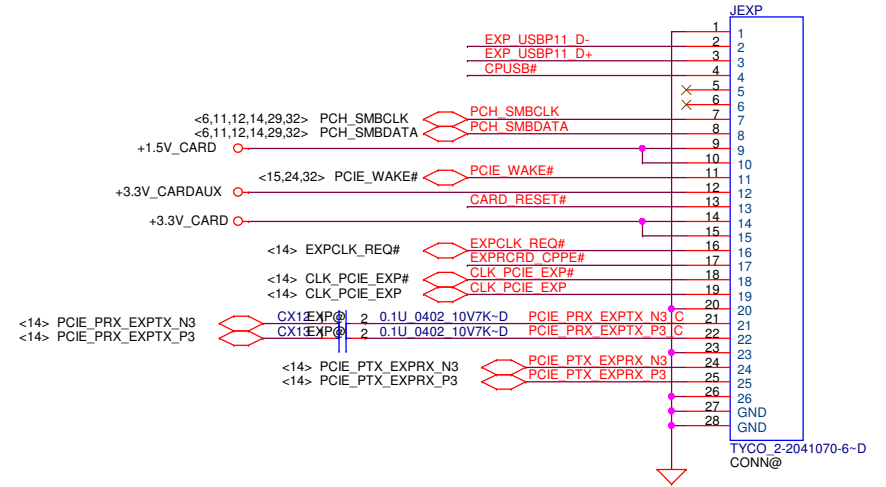
Security Classification	Compal Secret Data	
Issued Date	2012/01/17	Deciphered Date
		2013/01/16
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Compal Electronics, Inc.	
Title	DC/DC Interface
Document Number	LA-8241P
Date: Wednesday, February 01, 2012	Sheet 27 of 56

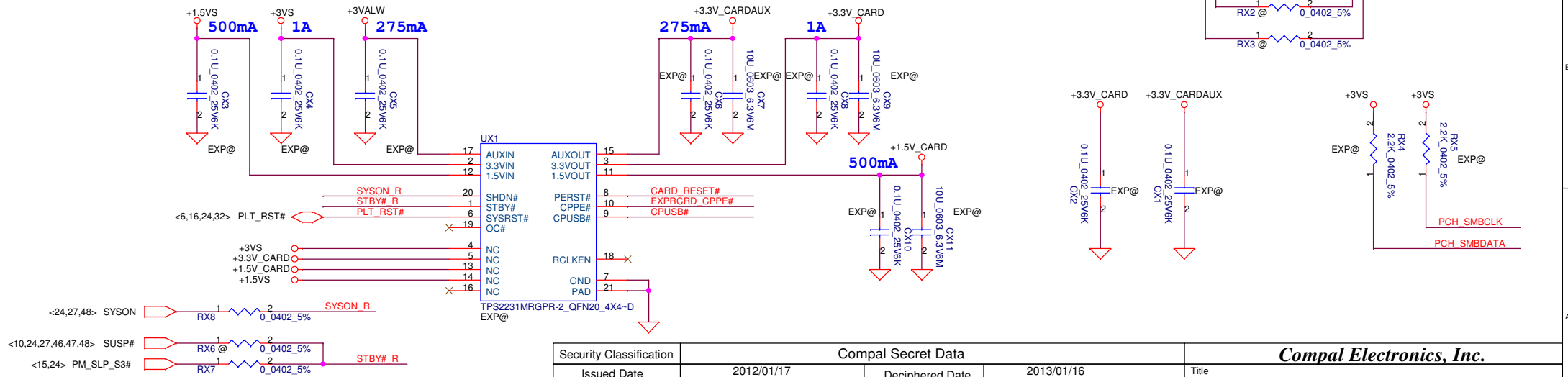
USB Detected for PWR Share



Express Card

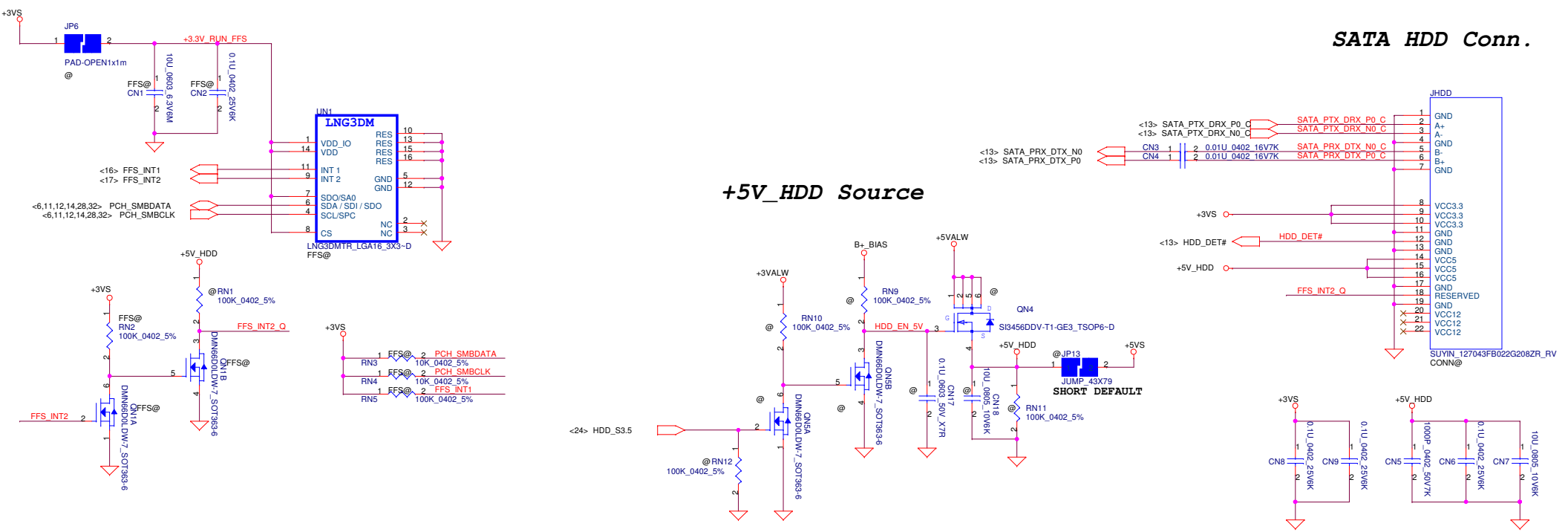


Express Card PWR S/W

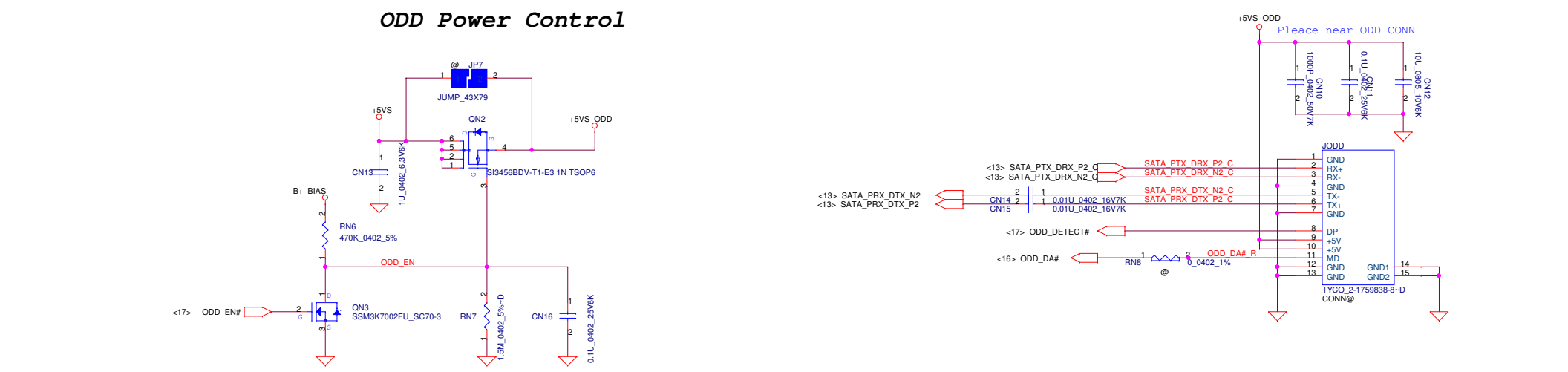


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Date	Wednesday, February 01, 2012	Sheet	28 of 56	Rev
				1.0

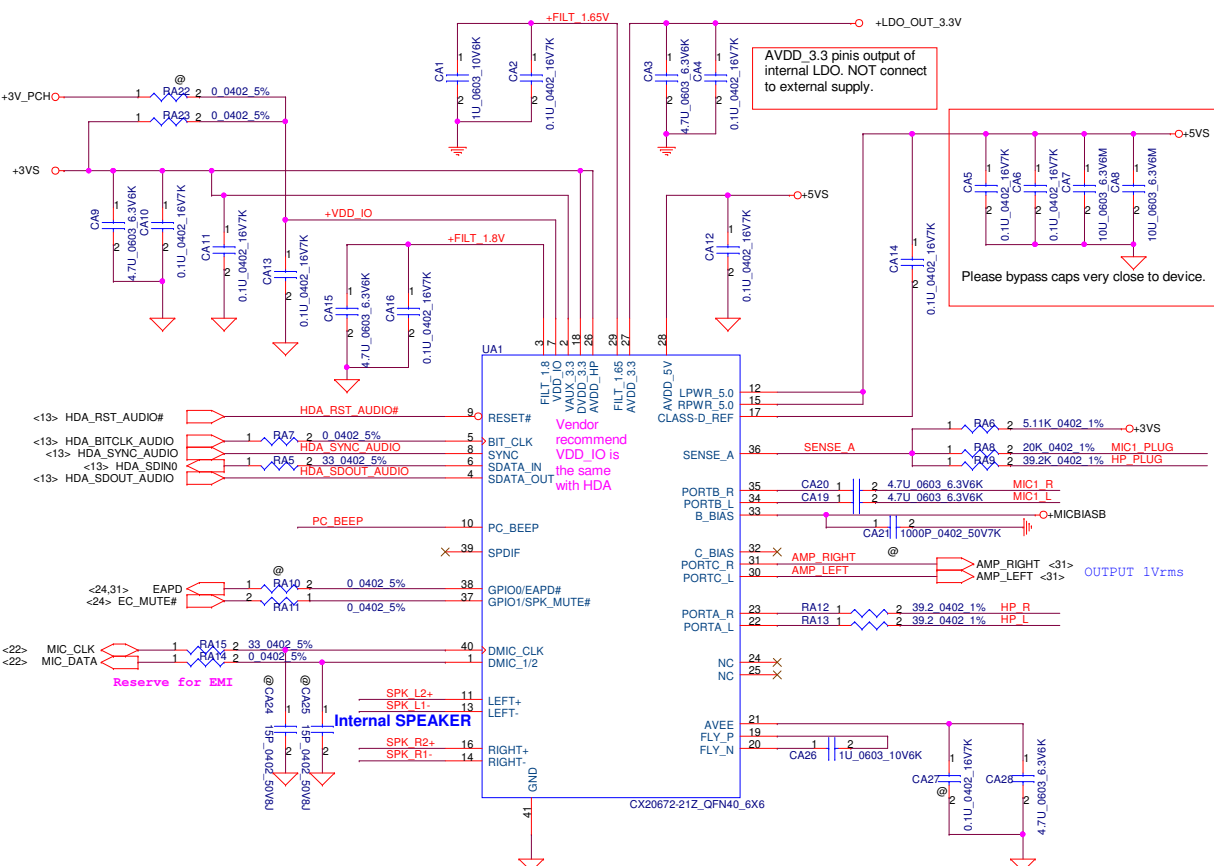
SATA HDD Conn.



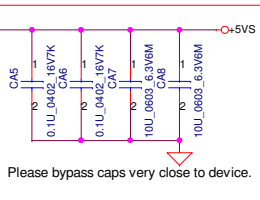
SATA ODD Conn.



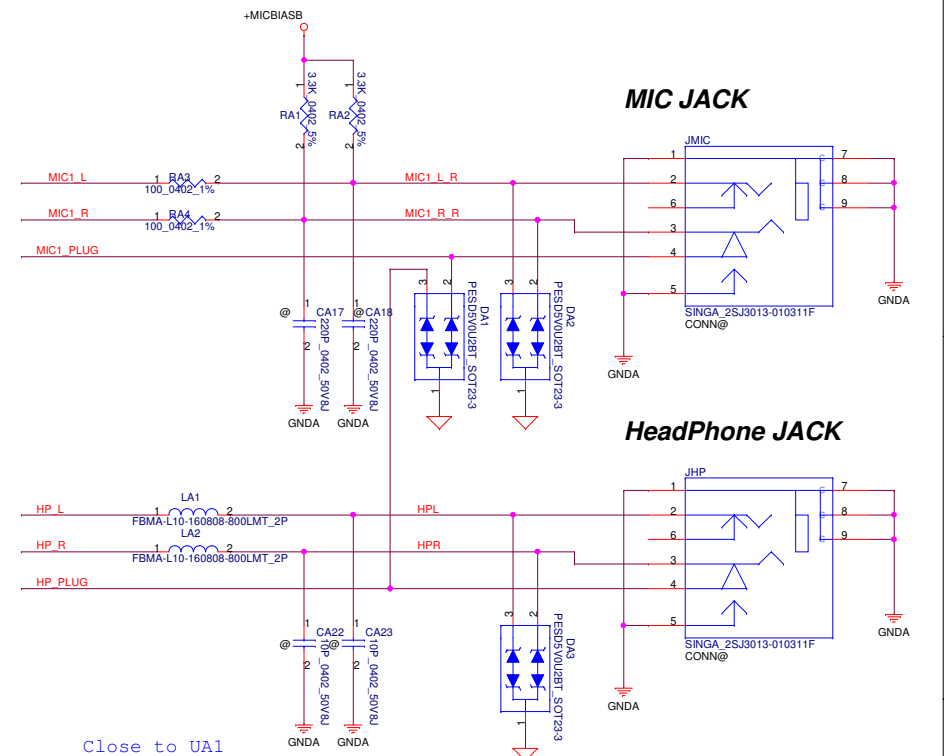
Security Classification	Compal Secret Data		Title	
Issued Date	2012/01/17	Deciphered Date	2013/01/16	HDD/ODD/FAN
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Date: Wednesday, February 01, 2012				Rev 1.0
Sheet 29			of 56	



AVDD_3.3 pins output of internal LDO. NOT connect to external supply.

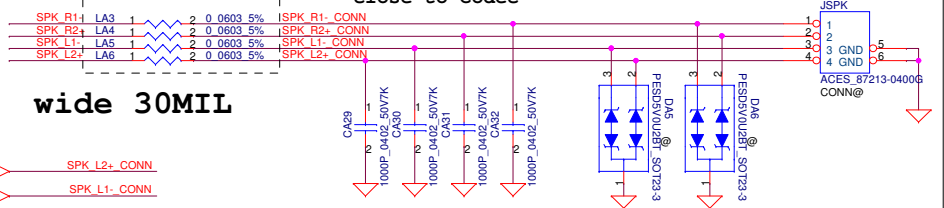


Please bypass caps very close to device.



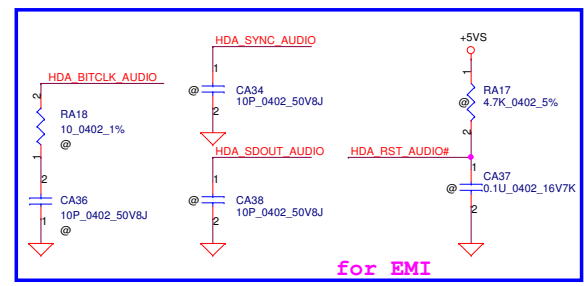
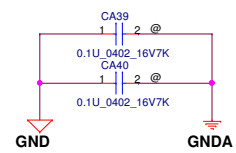
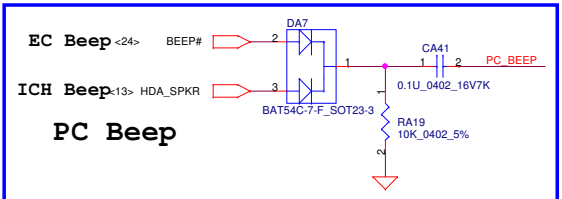
Close to UA1 Pin1,13,14,16

close to Codec



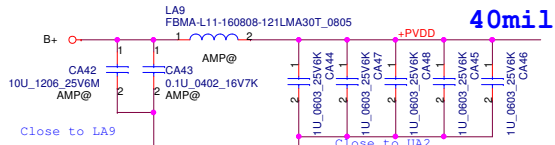
wide 30MIL

- <31> SPK_L2+_CONN SPK L2+_CONN
- <31> SPK_L1-_CONN SPK L1-_CONN
- <31> SPK_R2+_CONN SPK R2+_CONN
- <31> SPK_R1-_CONN SPK R1-_CONN

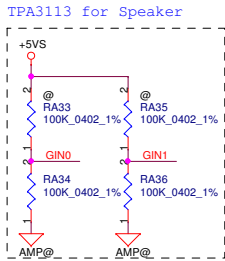


for EMI

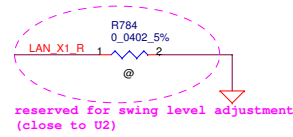
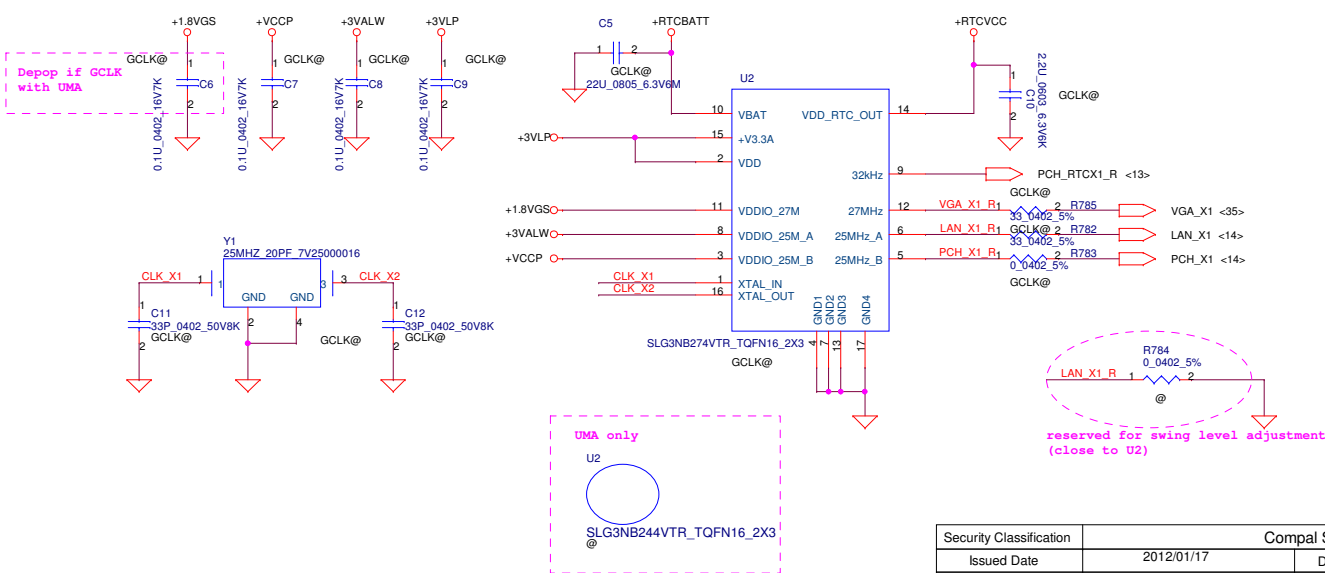
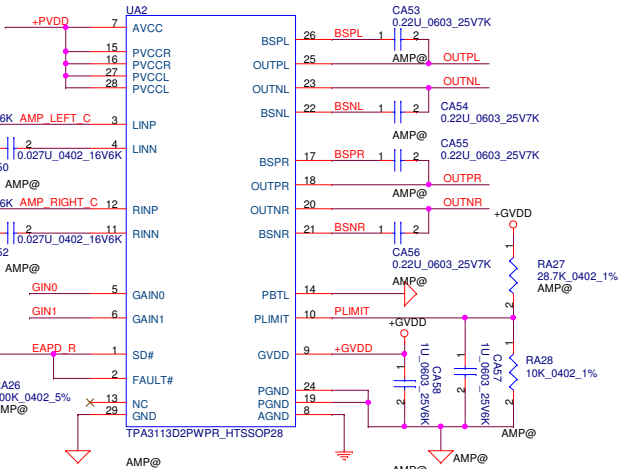
Security Classification		Compal Secret Data		Title	
Issued Date		Deciphered Date		Compal Electronics, Inc.	
2012/01/17		2013/01/16		PROCESSOR(I/6) DMI,FDI,PEG	
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		LA-8241P		1.0	
Date: Wednesday, February 01, 2012		Sheet 30 of 56			

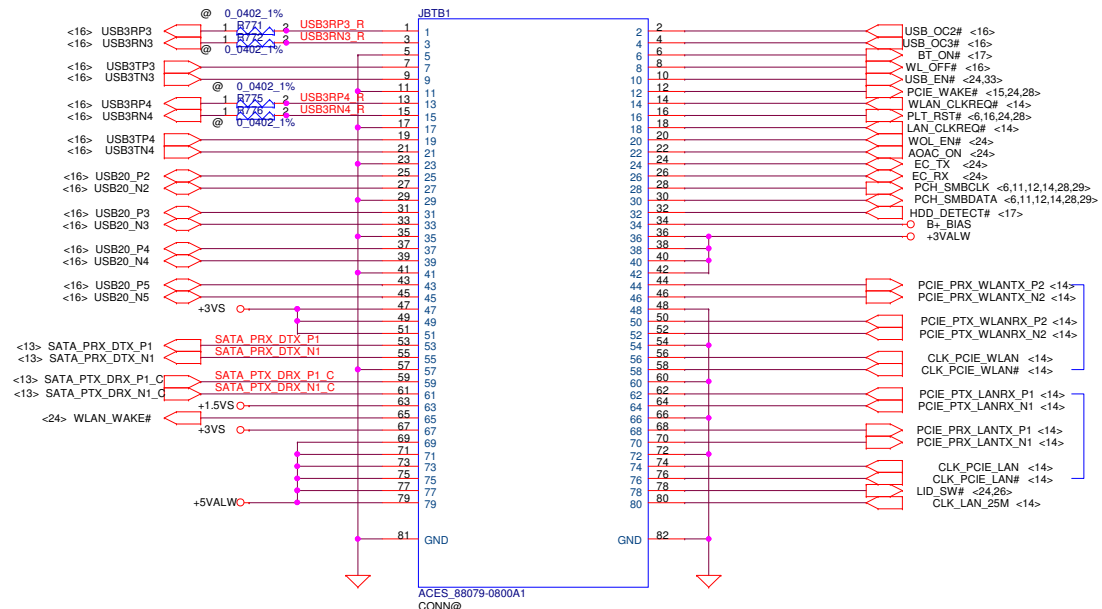


Need final turn R/C
10/24

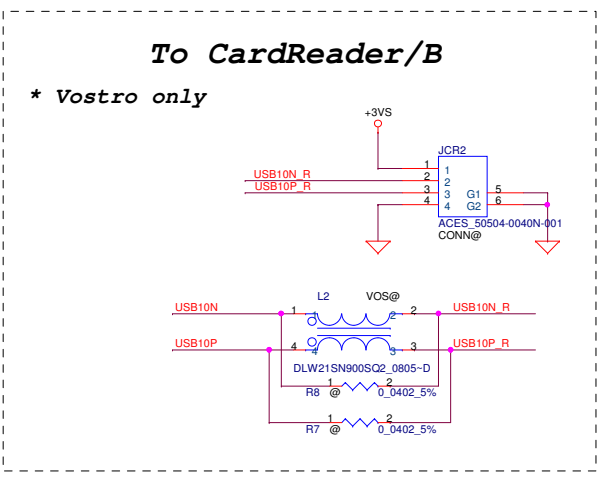
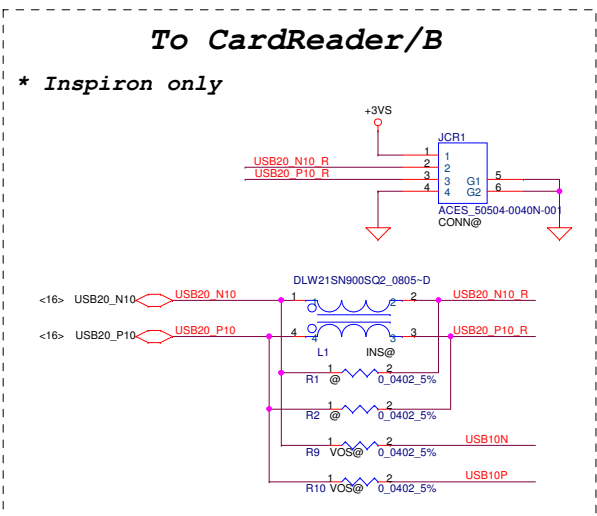


GAIN1	GAIN0	AV (inv)	INPUT IMPEDANCE
0	0	20dB	60Kohm
0	1	26dB	30Kohm
1	0	32dB	15Kohm
1	1	36dB	9Kohm

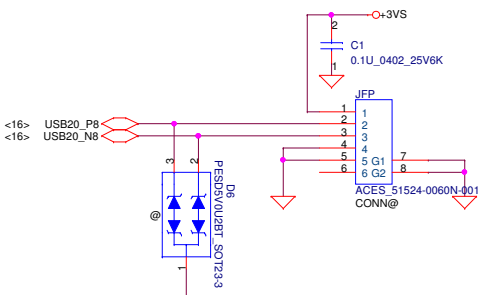




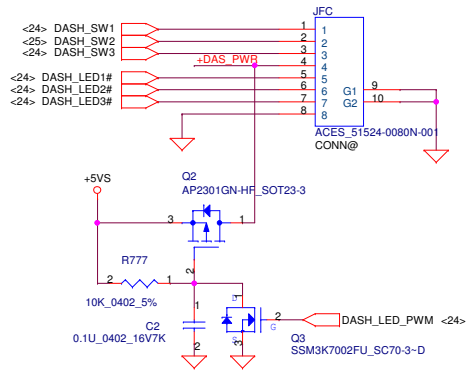
←---WLAN (Mini Card 1)
←---10/100/1G LAN



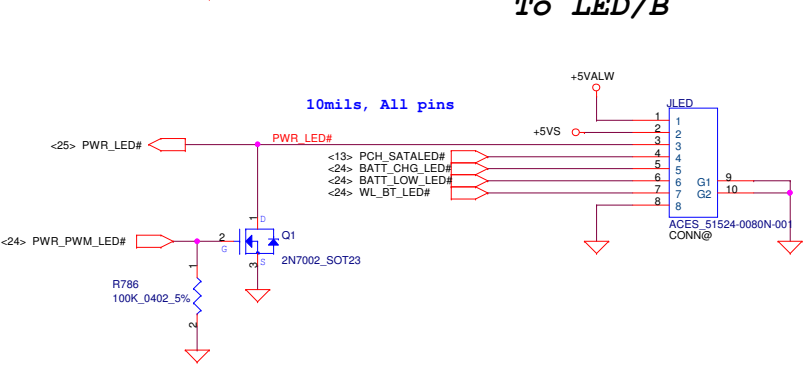
To Finger Print



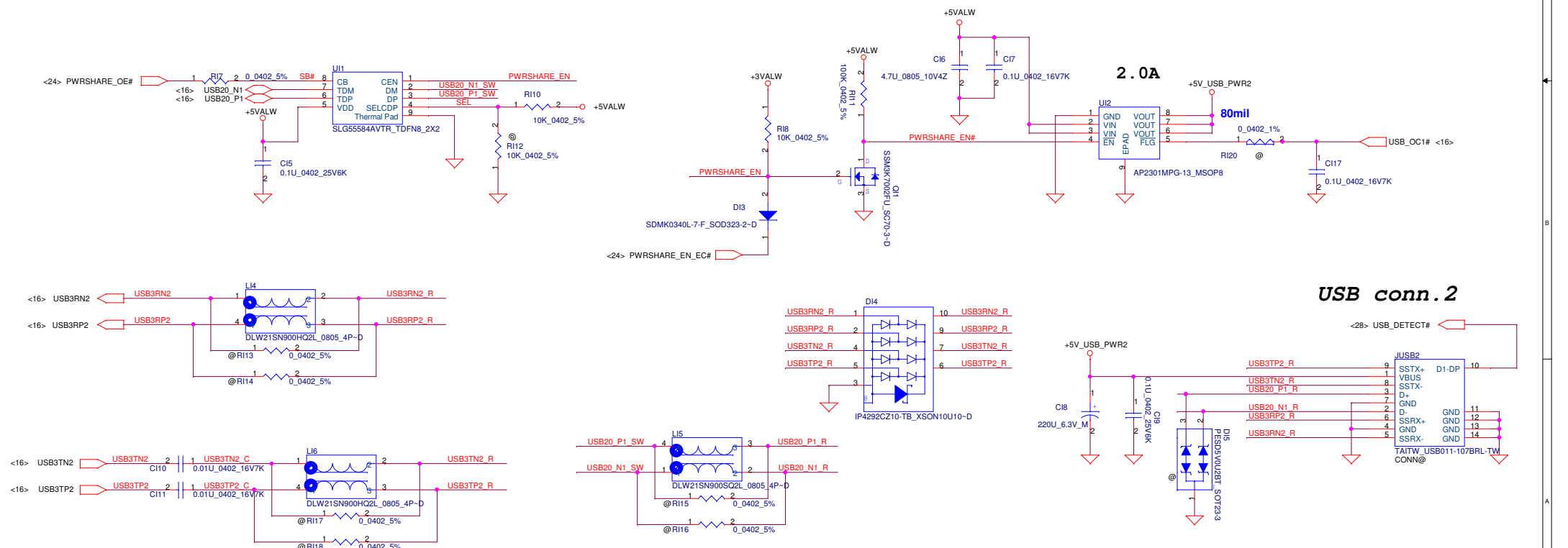
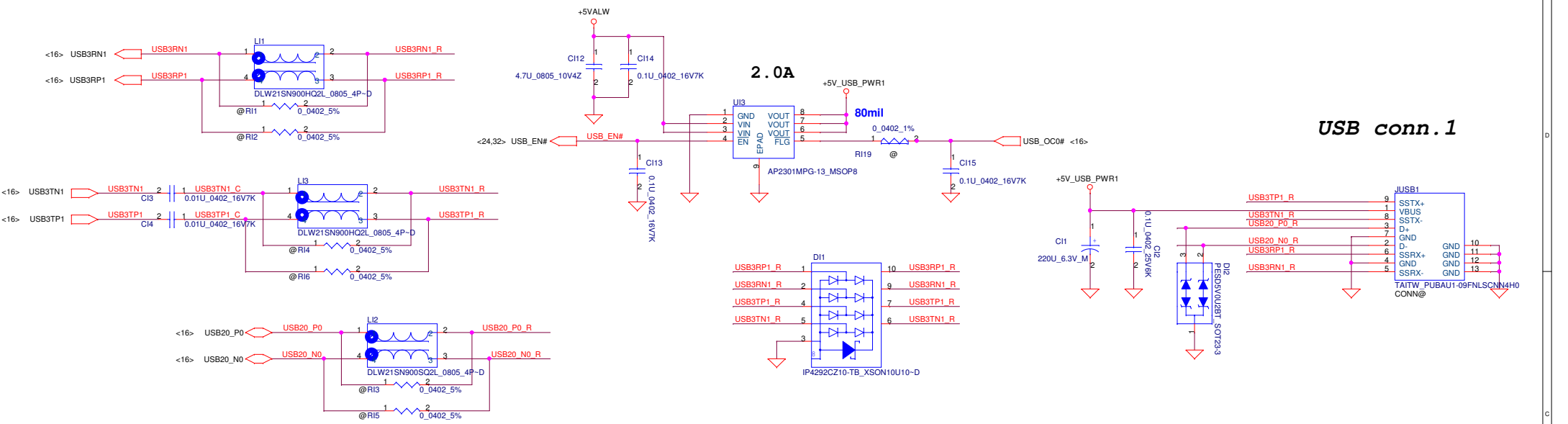
TO Function/B



To LED/B

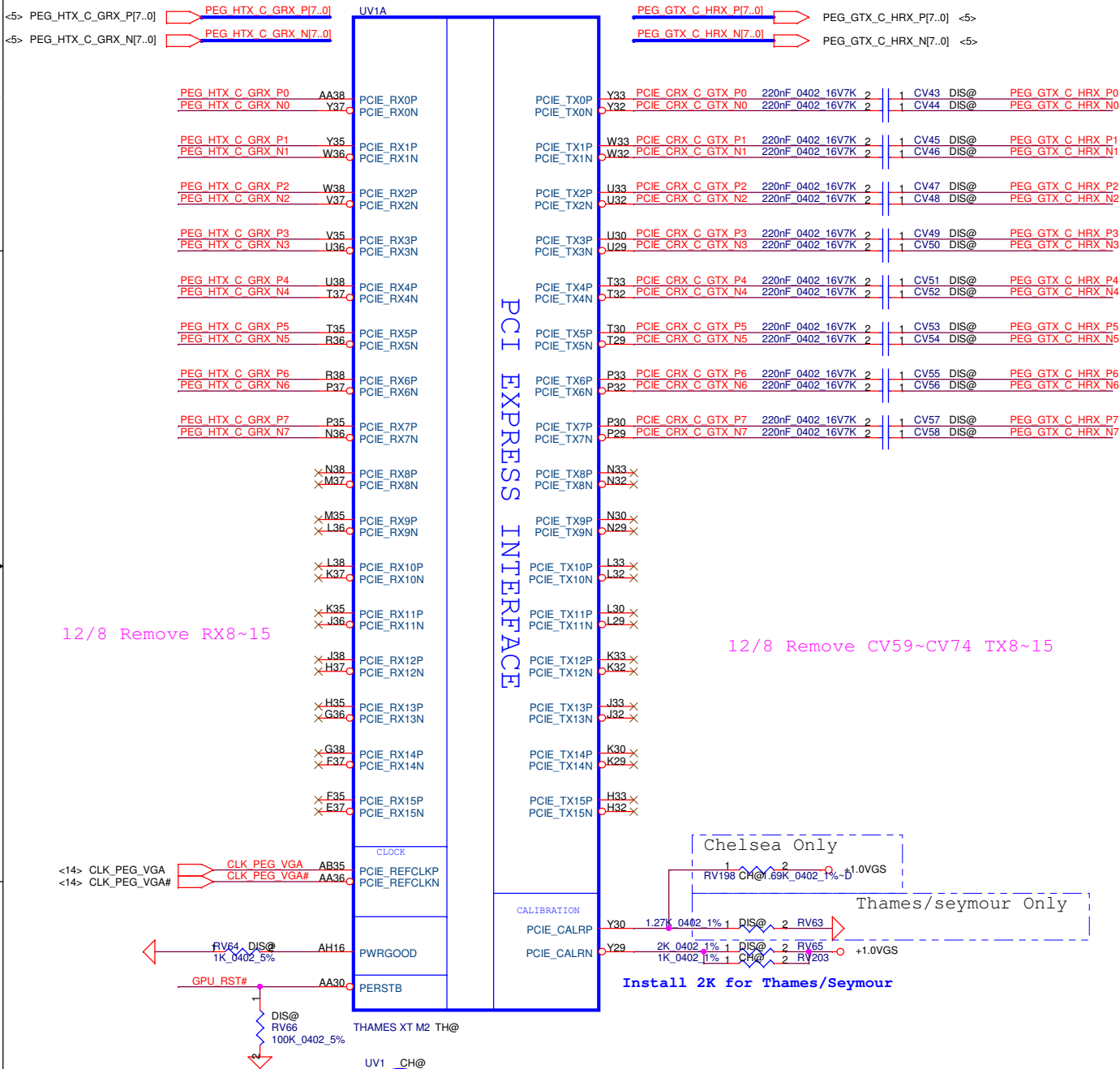


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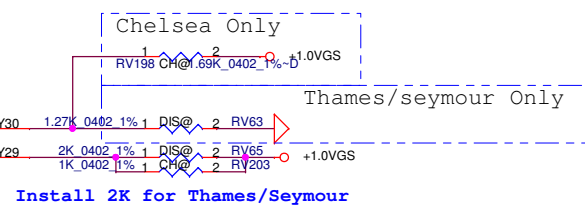
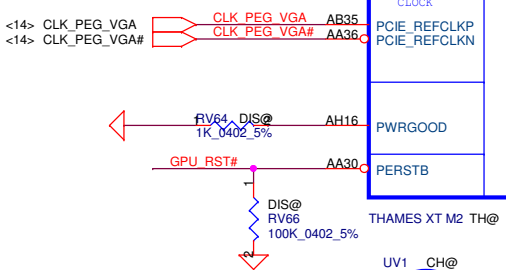
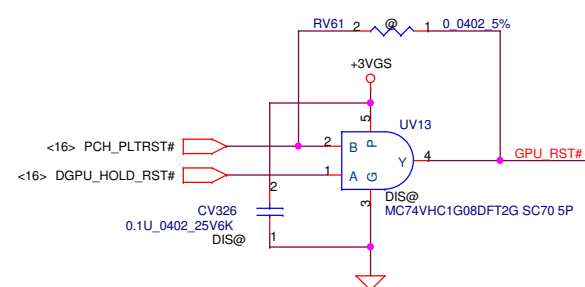
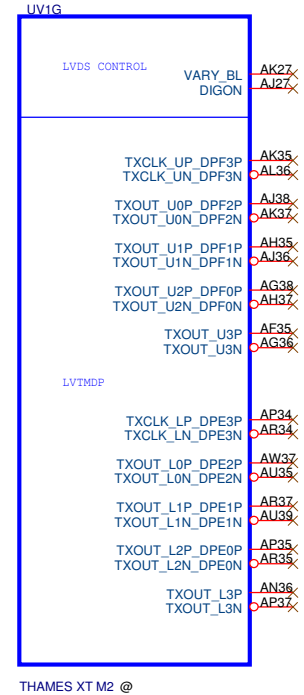


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Title PROCESSOR(I/6) DMI,FDI,PEG Document Number LA-8241P			Rev 1.0
Date: Wednesday, February 01, 2012			Sheet 33 of 56

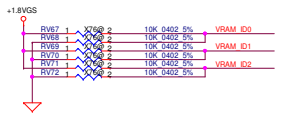
GFX PCIe LANE REVERSAL



LVDS Interface

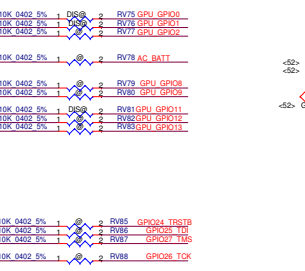


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				Document Number	LA-8241P
				Date:	Wednesday, February 01, 2012
				Sheet	34 of 56



Vendor	VRAM_ID0	VRAM_ID1	VRAM_ID2	
64MX16 (1G)	RV67	RV70	RV72	PT
64MX16 (1G)	RV68	RV69	RV72	PT
128M16 (2G)	RV67	RV70	RV71	
128M16 (2G)	RV68	RV69	RV71	
64MX16 (1G)	RV67	RV69	RV71	PT

STRAPS



0.60 V level, Please VREFQ Divider ans cap close to ASIC

20mil

20mil

20mil

20mil

XTALIN Voltage Swing: 1.8 V

1.8V@20mA TSVD

10mil

10mil

10mil

10mil

10mil

10mil

10mil

10mil

10mil

10mil

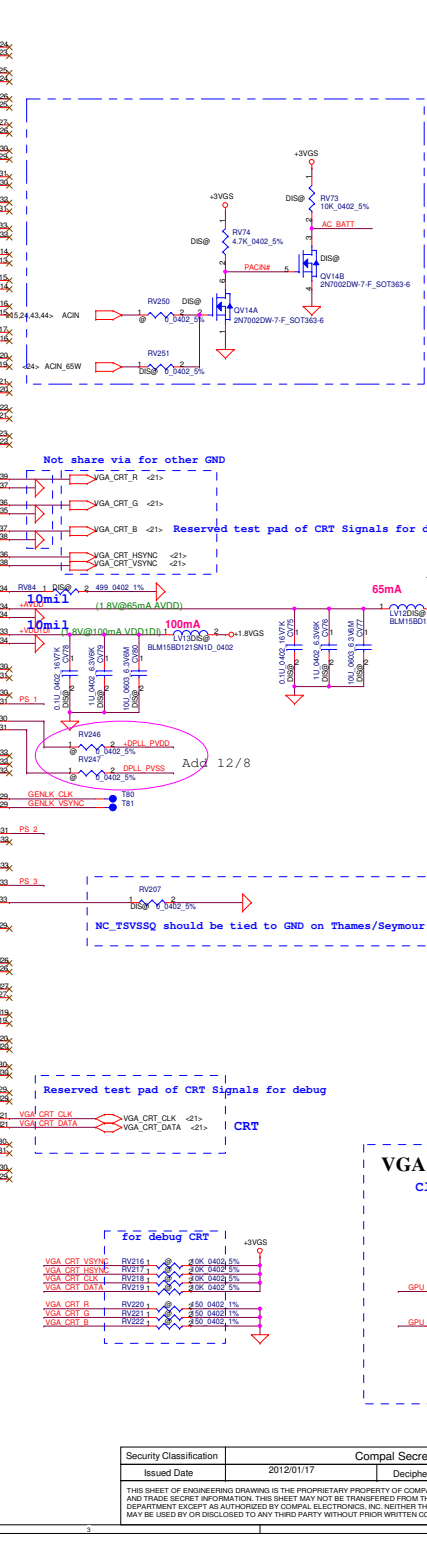
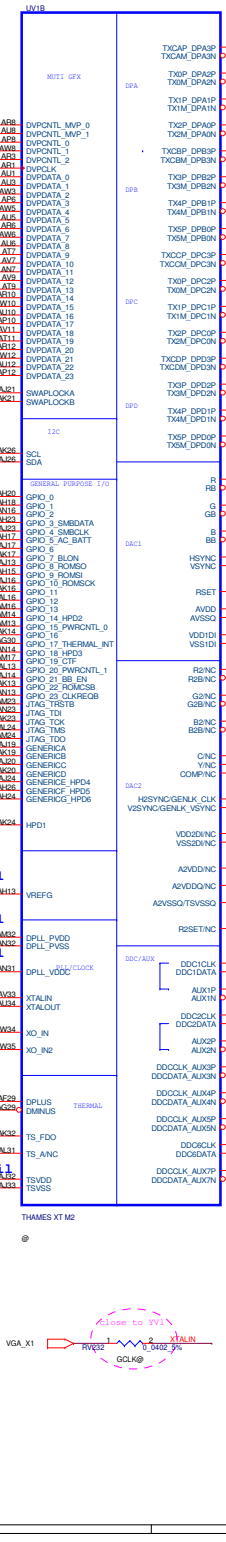
10mil

10mil

10mil

10mil

10mil

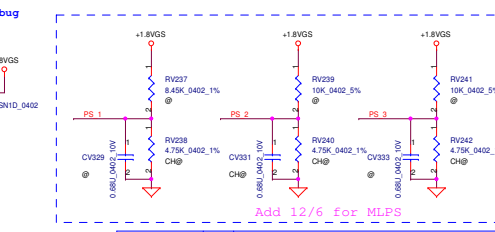


CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

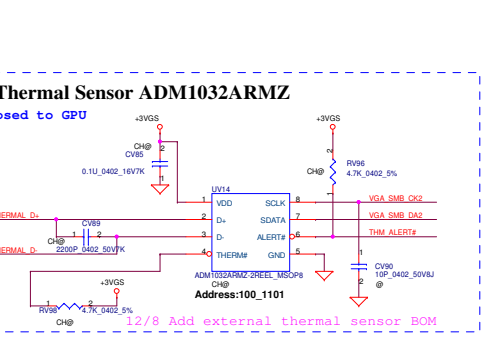
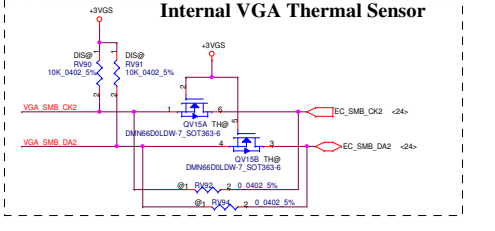
STRAPS	PN	DESCRIPTION OF DEFAULT SETTINGS	RECOMMENDED SETTINGS	RECOMMENDED SETTINGS
TX_PWR5_ENB	GPIO0	PCIe FULL TX OUTPUT SWING	0: 50% swing 1: Full swing	X
TX_DEEMPH_EN	GPIO1	PCIe TRANSMITTER DE-EMPHASIS	0: enable 1: enable	X
RSVD	GPIO2	Advertises PCIe speed when compliance test	0: 527/a 1: 507/a	0
RSVD	GPIO8	RESERVED		0
BF_VGA_DS	GPIO9	VGA ENABLED		0
RSVD	GPIO21	RESERVED		0
BIOS_ROM_EN	GPIO22, ROMCSB	ENABLE EXTERNAL BIOS ROM	0: enable 1: enable	X
ROMIDCFG(20)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT		XXX
VP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS		0
RSVD	HSYNC			0
RSVD	GENERICC			0
AUD[1]	HSYNC	AUD[1] AUDIO	0: 0 No audio function 0: 1 Audio for DisplayPort and HDMI if dongle is detected 1: 0 Audio for DisplayPort only 1: 1 Audio for both DisplayPort and HDMI	11
AUD[0]	VSYSNC			

AMD RESERVED CONFIGURATION STRAPS
ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET

GPIO21	HSYNC	GENERICC	GPIO2	GPIO8
--------	-------	----------	-------	-------

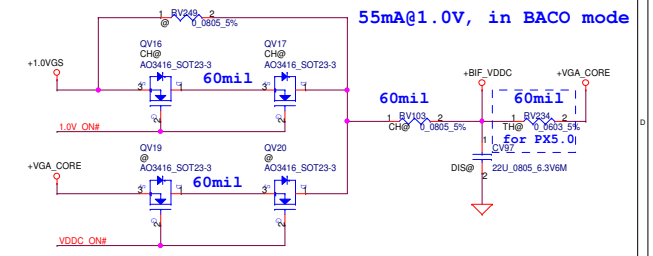
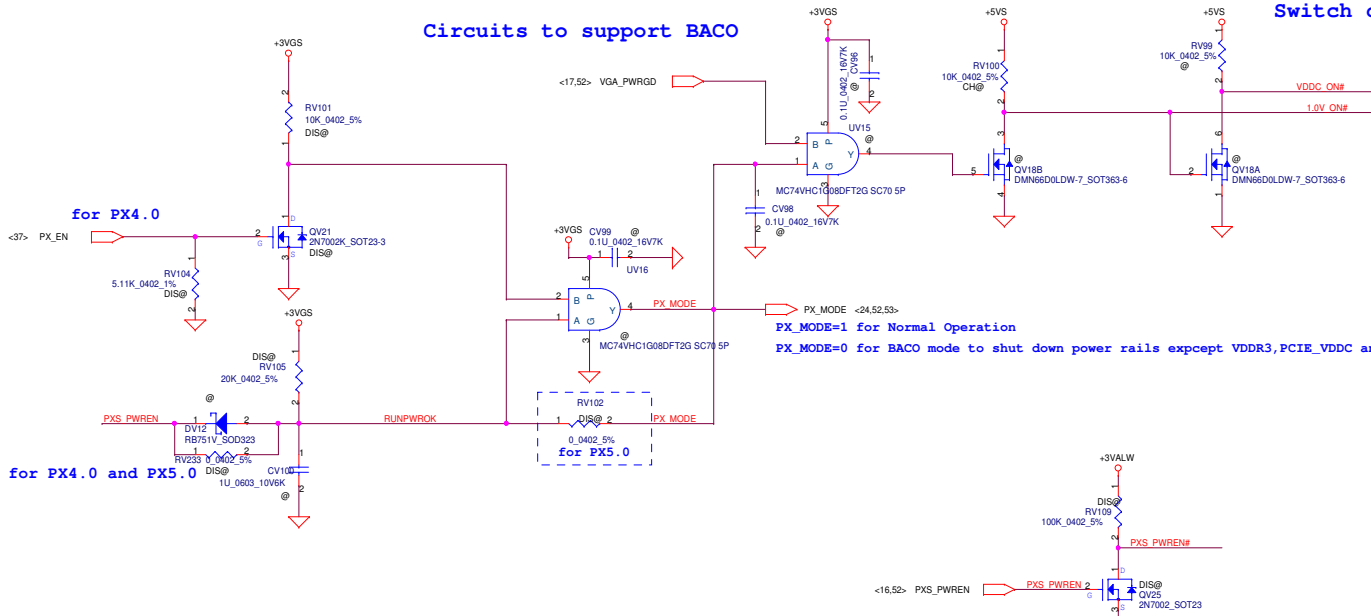


TX_PWR5_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing for mobile mode 1: Full Tx output swing (Default setting for Desktop)
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis disabled for mobile mode 1: Tx de-emphasis enabled (Default setting for desktop)



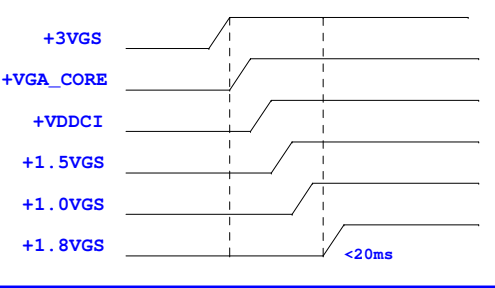
Switch circuits in BACO desings for Thames/Seymour only

Circuits to support BACO

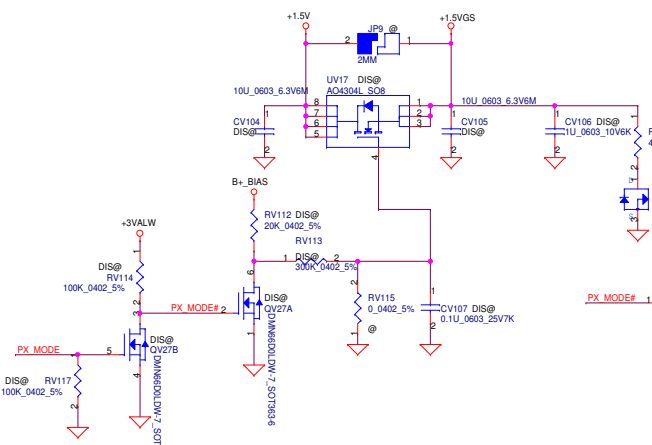


Note:
 PX4.0 +VGA_CORE, VDDCI, +1.5VGS ON
 PX4.0 +3VGS, +1.0VGS, +1.8VGS OFF
 PX5.0 +3VGS, +VGA_CORE, VDDCI, +1.5VGV, +1.0VGS, +1.8VGS OFF

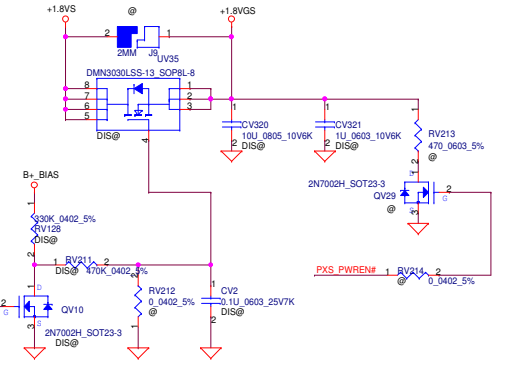
Power Sequence of Thames and Chelsea



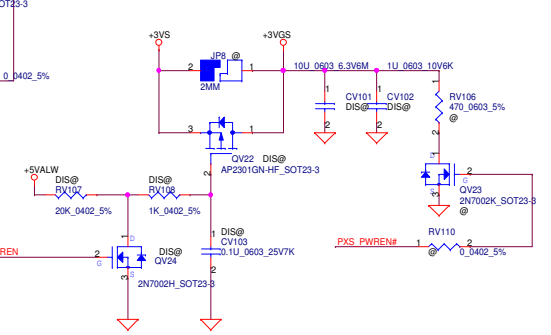
+1.5V TO +1.5VGS



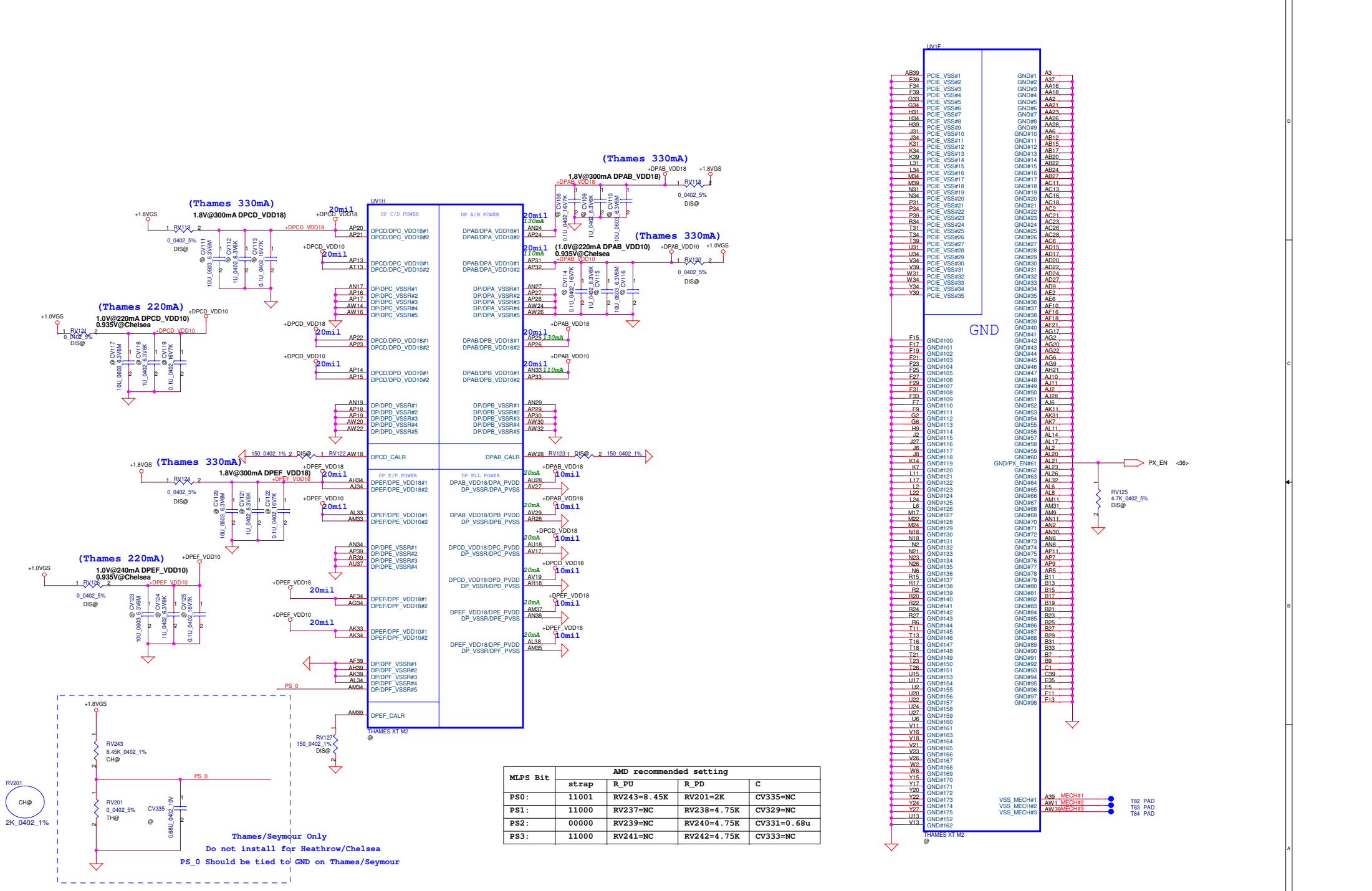
+1.8VS TO +1.8VGS



+3.3VS TO +3.3VGS

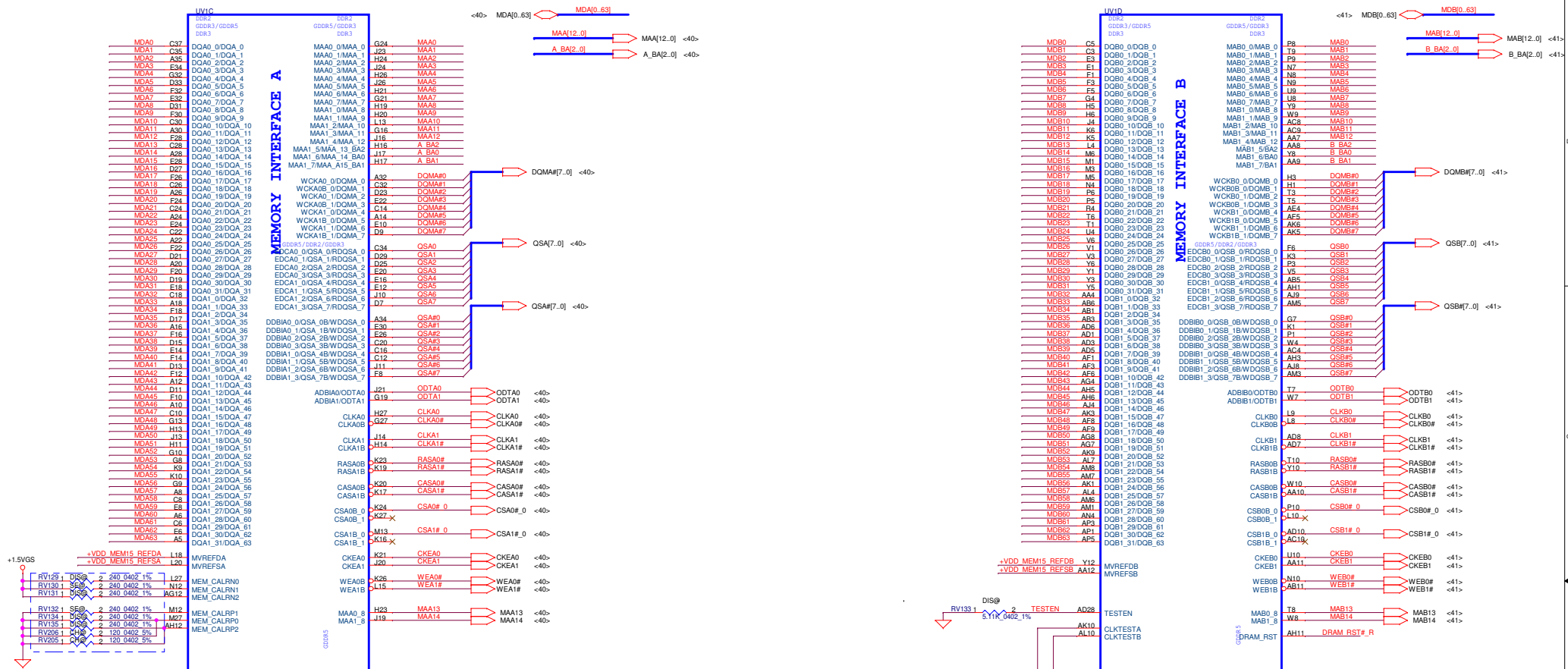


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Size	C	Document Number	LA-8241P	Rev
Date:	Wednesday, February 01, 2012	Sheet	36	of 56



MLPS Bit	AMD recommended setting			
	strap	R_PU	R_PD	C
PS0:	11001	RV243=8.45k	RV201=2K	CV335=NC
PS1:	11000	RV237=NC	RV238=4.75k	CV329=NC
PS2:	00000	RV239=NC	RV240=4.75k	CV331=0.68u
PS3:	11000	RV241=NC	RV242=4.75k	CV333=NC

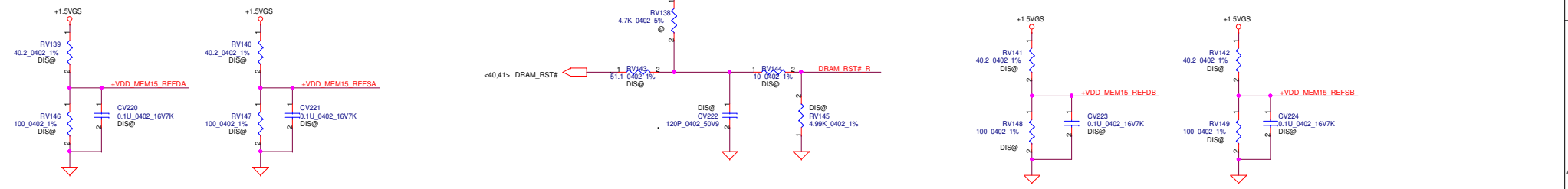
Thames/Seymour Only
Do not install for Heathrow/Chelsea
PS_0 Should be tied to GND on Thames/Seymour



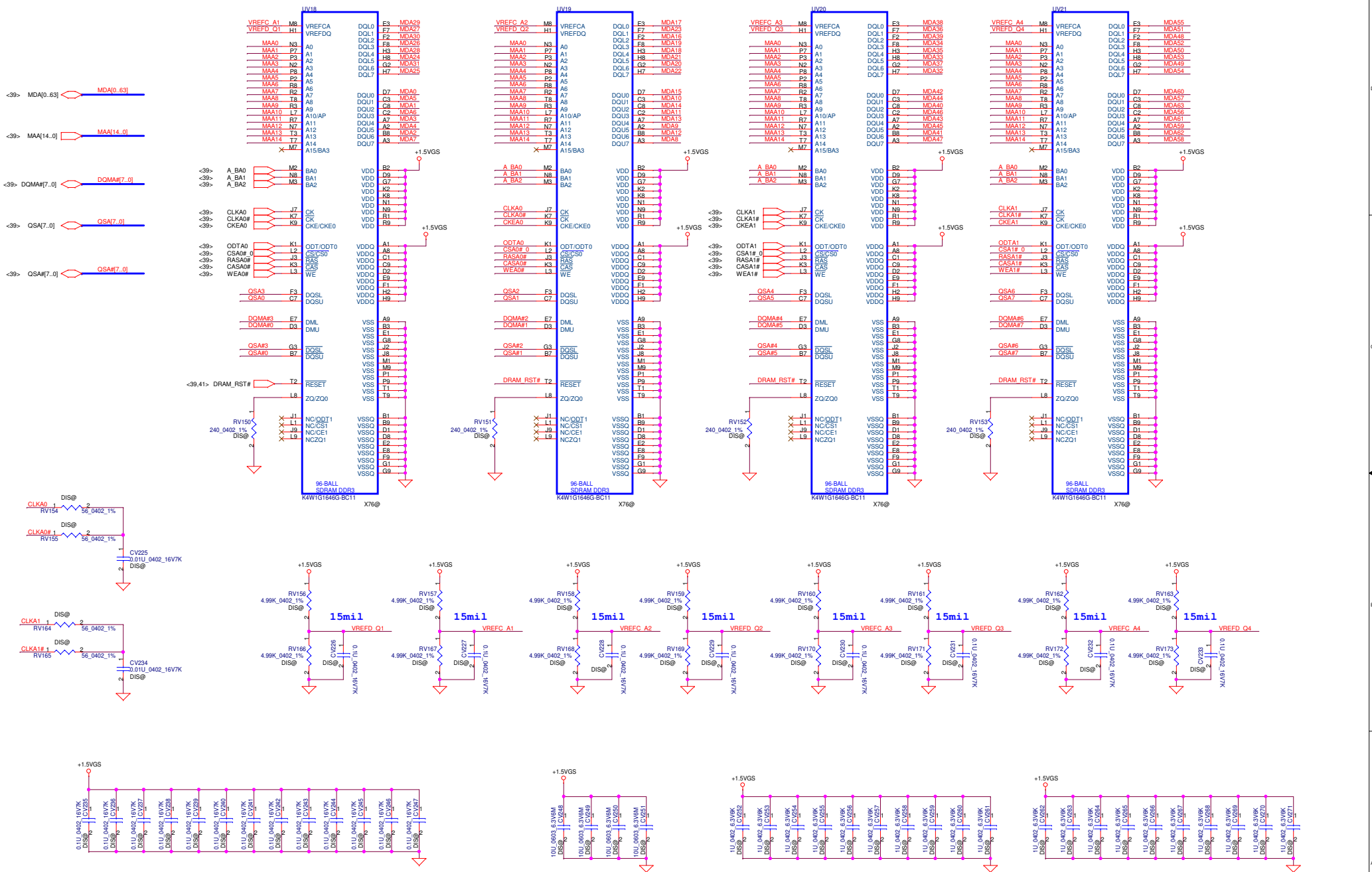
Co-lay Thames/Seymour/Chelsea

	Thames M2	Seymour M2	Chelsea M2
RV129	POP	POP	POP
RV130	POP	POP	POP
RV131	POP	POP	POP
RV132	POP	POP	POP
RV134	POP	POP	POP
RV135	POP	POP	POP
RV206	POP	POP	POP
RV205	POP	POP	POP

This basic topology should be used for DRAM_RST for DDR3/GDDR5. These Capacitor and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM Load and will have to be calculated for different Memory, DRAM Load and board to pass Reset Signal Spec. Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

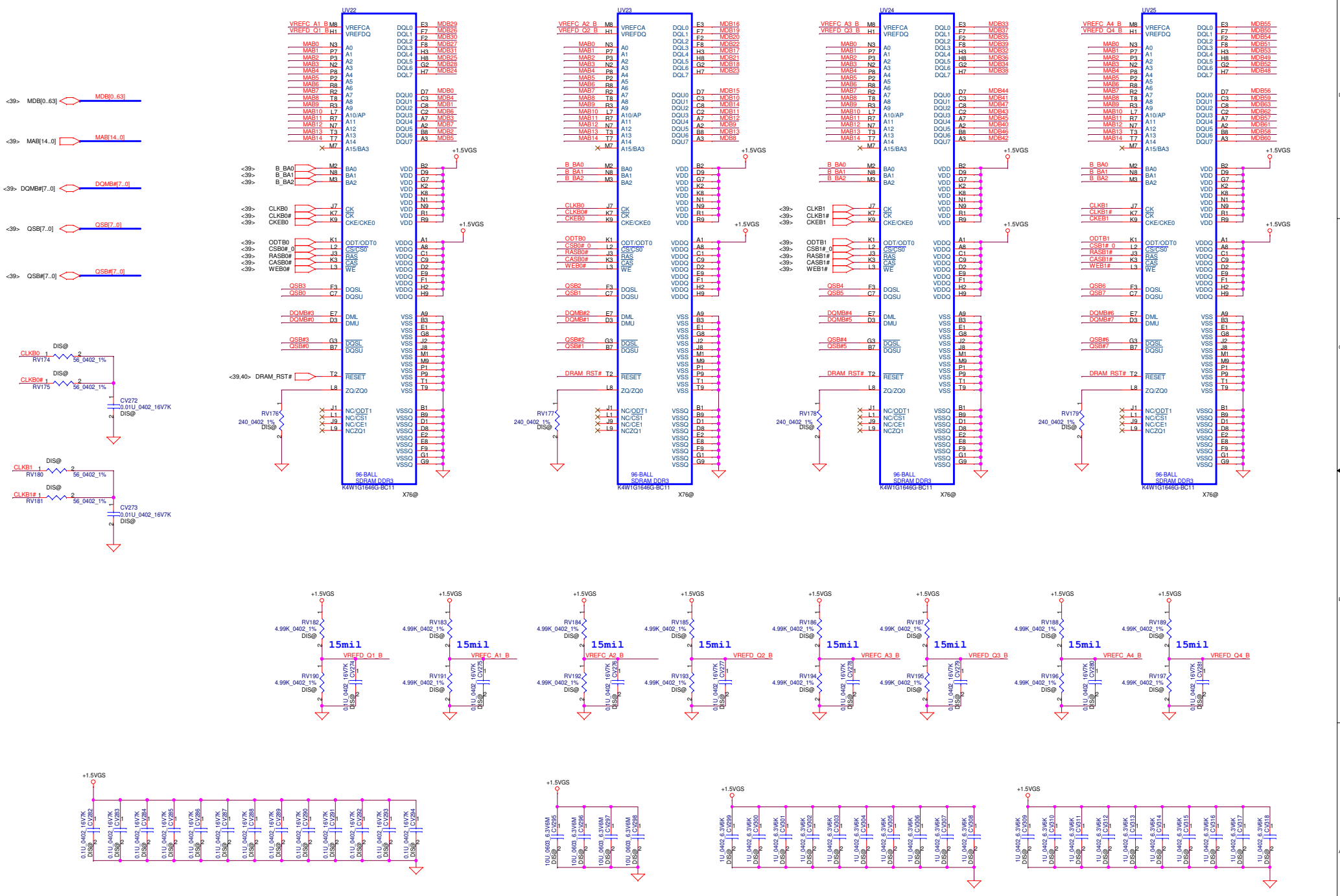


CHANNEL A: 256MB/512MB DDR3



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Size	Document Number	LA-8241P	Rev	1.0
Date:	Wednesday, February 01, 2012	Sheet	40	of 56

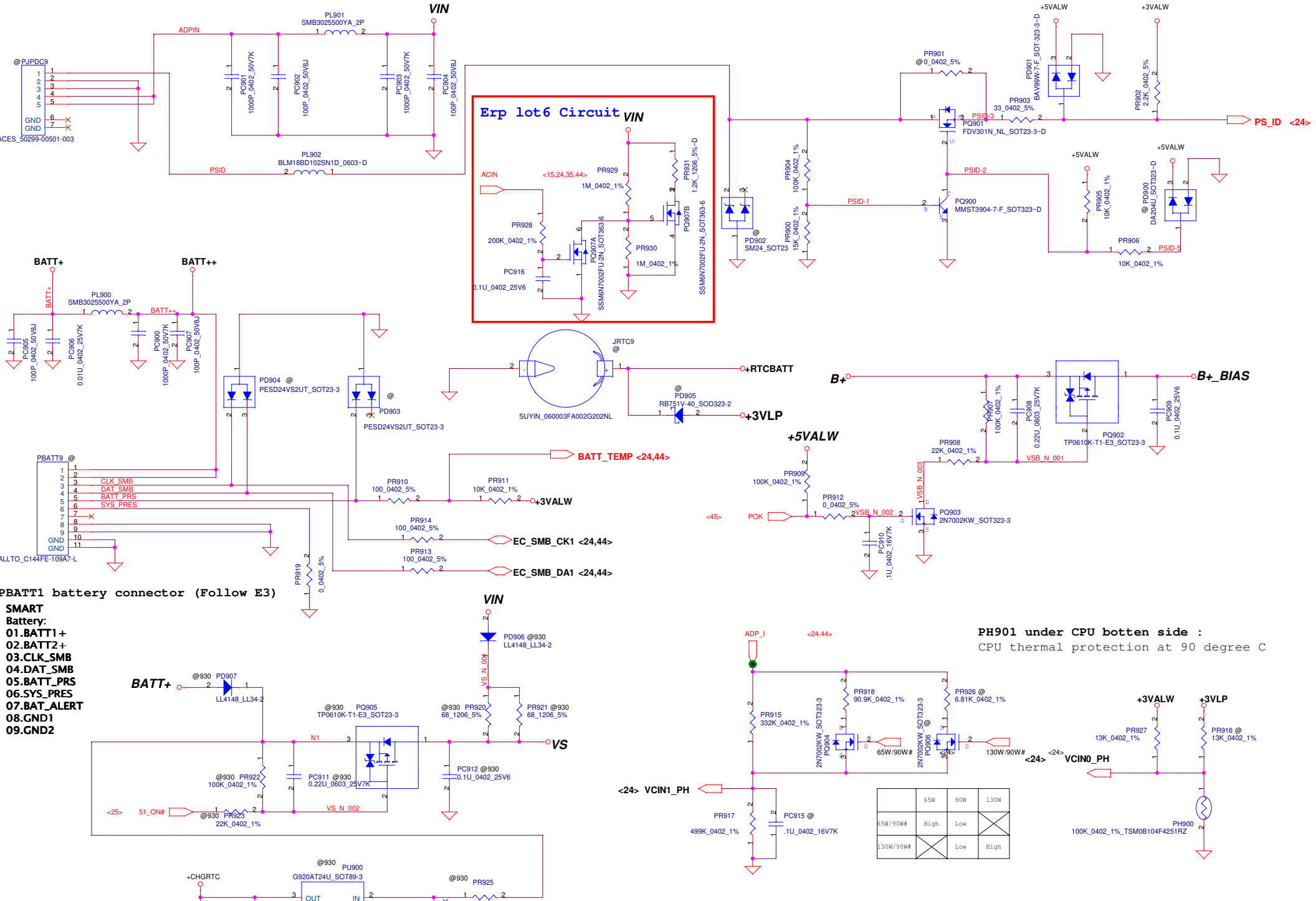
CHANNEL B: 256MB/512MB DDR3



Security Classification	Compal Secret Data			Compal Electronics, Inc.
Issued Date	2012/01/17	Deciphered Date	2013/01/16	ATI SeymourXT M2 VRAM B
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Size	Document Number	Date:	Wednesday, February 01, 2012	Sheet 41 of 56
C	LA-8241P	Rev	1.0	

Version Change List (P. I. R. List)

<i>Item</i>	<i>Page#</i>	<i>Title</i>	<i>Date</i>	<i>Request Owner</i>	<i>Issue Description</i>	<i>Solution Description</i>	<i>Rev.</i>
1	08,11,12	DIMM	11/07/28	COMPAL	The M3 traces are routed to the Sandy Bridge Processor reserved pins for DDR3 VREF	Intel CHRLST Rev1.5 required	0.1
2	18,19	FCH	11/07/28	COMPAL	VCCDMI, V_PROC_IO change to +VCCP from +1.05VS	Intel CHRLST Rev1.5 required	0.1
3	09,10	CPU	11/07/28	COMPAL	remove decoupling cap for +VCC_CORE, +VCCP, +VCC_GFXCORE_AKG, owner change to PWR	Intel CHRLST Rev1.5 required	0.1
4	10	CPU	11/07/28	COMPAL	VCCSA_SELECT[0:1] which should be connected to VID[1:0] of the System Agent (SA) VR controller.	Intel CHRLST Rev1.5 required	0.1
5							
6							
7							
8							
9							
10							
11							
12							
13							
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15							
16							
17							
18							

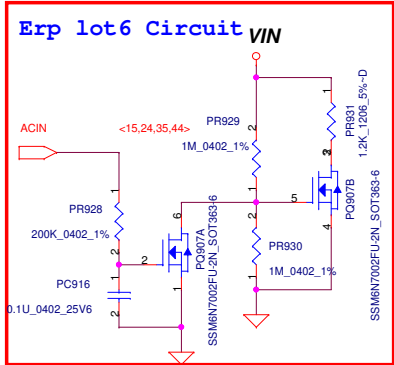


BATT+
BATT++

PBATT9 @
 1
 2
 3
 4
 5
 6
 7
 8
 9
 10
 11
 GND
 GND

SMART Battery:
01.BATT1+
02.BATT2+
03.CLK_SMB
04.DAT_SMB
05.BATT_PRS
06.SYS_PRES
07.BAT_ALERT
08.GND1
09.GND2

BATT+ @930 PD907
 LL4148_LL34-2
 @930 PQ905
 TP0610K-T1-E3_SOT23-3
 @930 PR920
 68_1206_5%
 @930 PR921
 68_1206_5%
 @930 PR922
 100K_0402_1%
 @930 PR923
 22K_0402_1%
 @930 PR925
 22K_0402_1%
 VS_N_002
 @930 PU900
 G920AT24U_SOT89-3
 @930 PR925
 200_0805_5%
 @930 PC913
 4.7U_0603_5.3V6K-D
 @930 PC914
 1U_0603_25V6K



PH901 under CPU bottom side :
 CPU thermal protection at 90 degree C

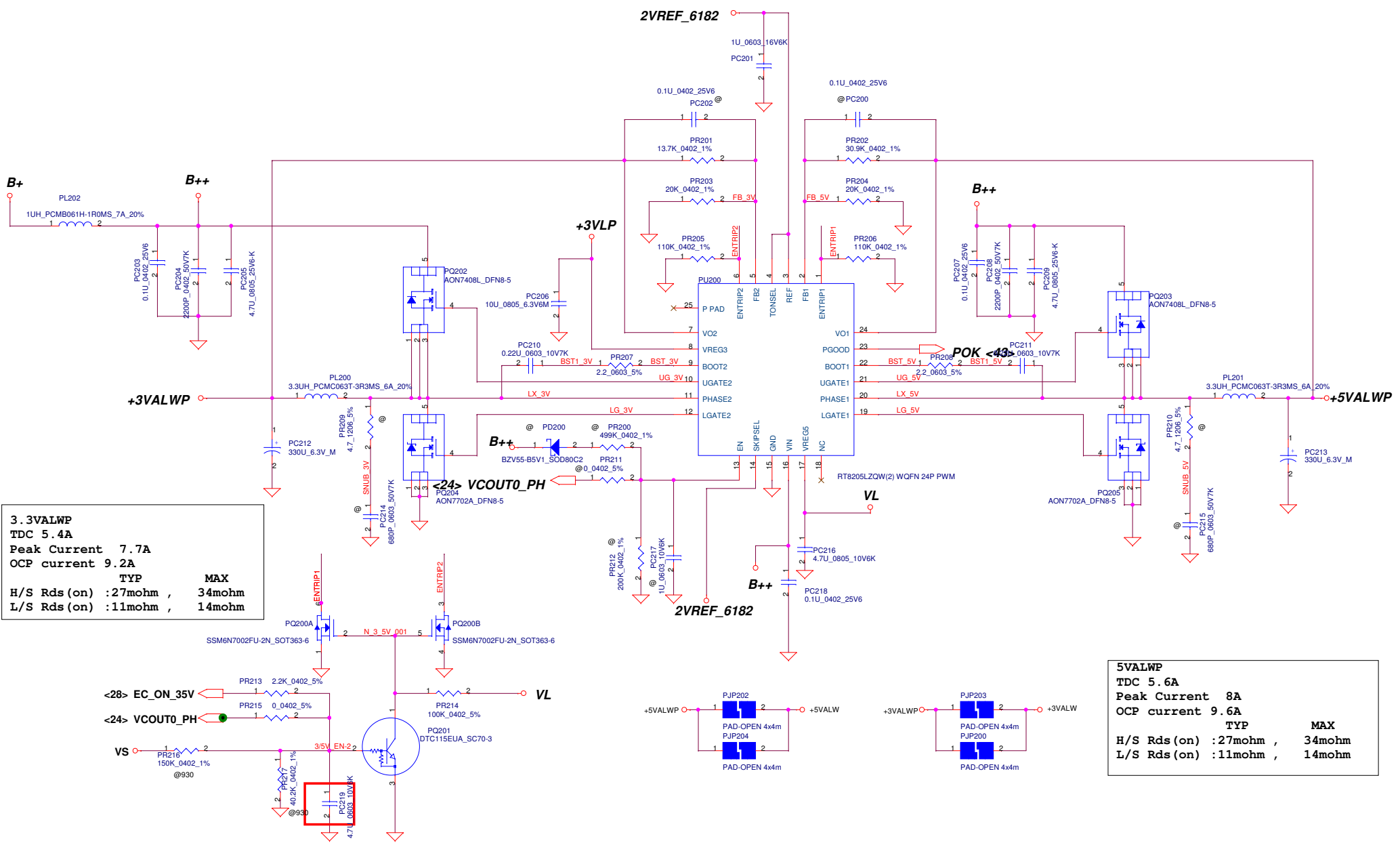
	65W	90W	130W
65W/90W#	High	Low	X
130W/90W#	X	Low	High

3.3VALWP
 TDC 5.4A
 Peak Current 7.7A
 OCP current 9.2A

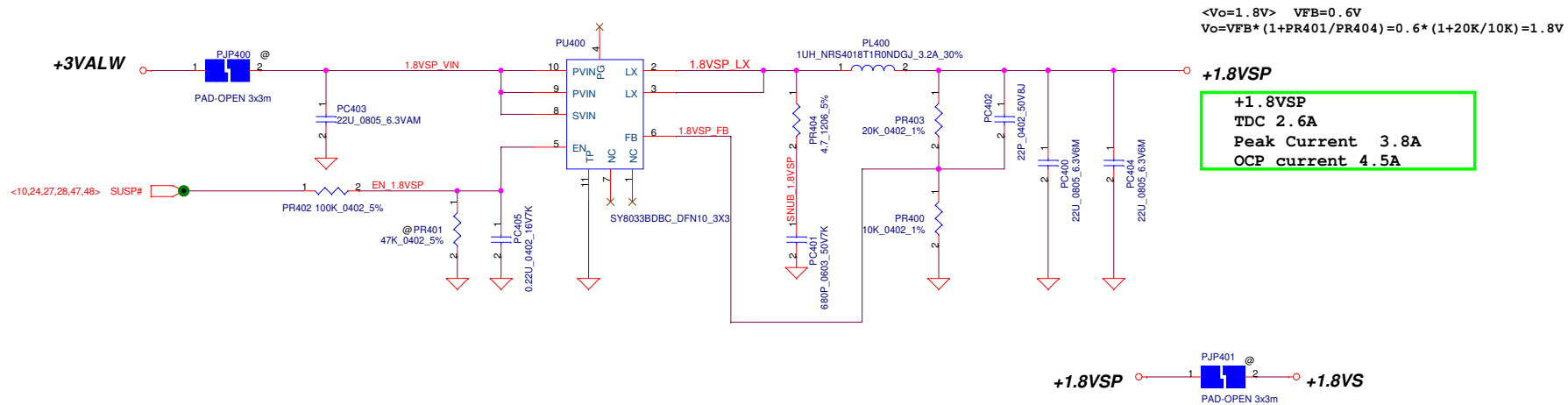
TYP	MAX
H/S Rds (on) : 27mohm ,	34mohm
L/S Rds (on) : 11mohm ,	14mohm

5VALWP
 TDC 5.6A
 Peak Current 8A
 OCP current 9.6A

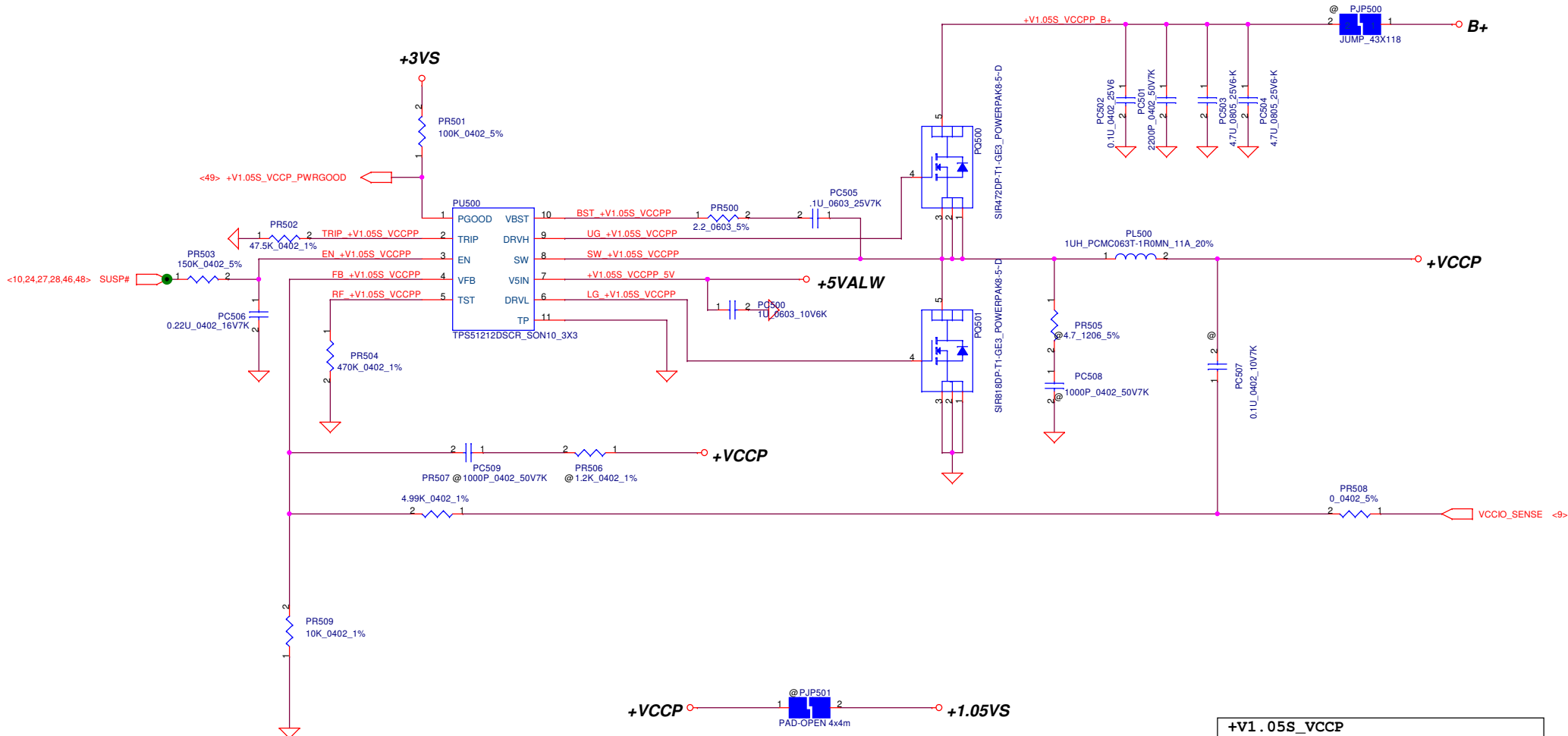
TYP	MAX
H/S Rds (on) : 27mohm ,	34mohm
L/S Rds (on) : 11mohm ,	14mohm



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				Rev 1.0

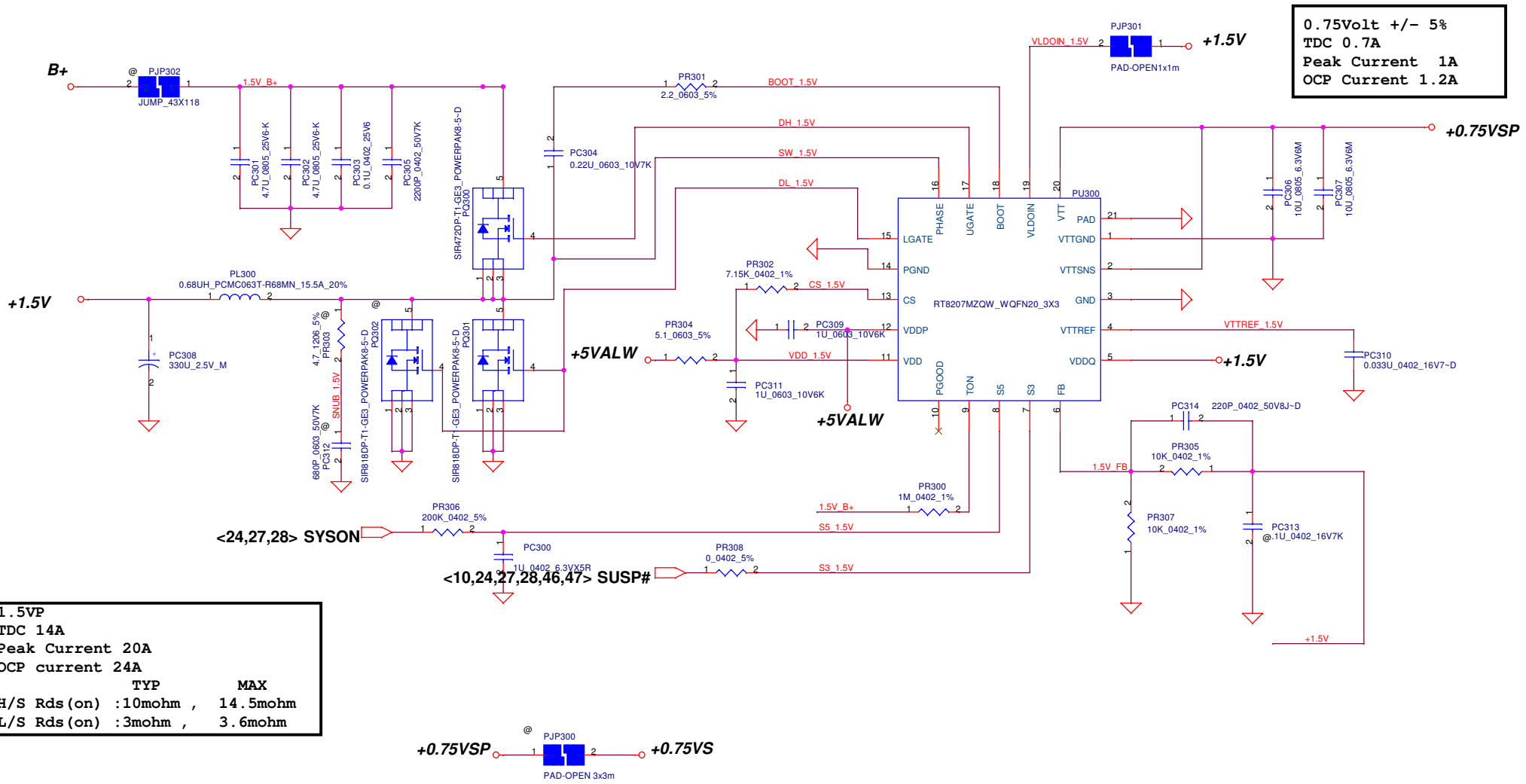


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				Date:	Wednesday, February 01, 2012
				Sheet	46 of 56
				Rev	1.0



+V1.05S_VCCPP	
TDC 11A	
Peak Current 16A	
OCP current 19A	
	TYP MAX
H/S Rds (on)	10mohm , 14.5mohm
L/S Rds (on)	: 3mohm , 3.6mohm

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				Document Number	
				LA-8241P	
				Date:	Wednesday, February 01, 2012
				Sheet	47 of 56
				Rev	1.0



0.75Volt +/- 5%
 TDC 0.7A
 Peak Current 1A
 OCP Current 1.2A

1.5VP
 TDC 14A
 Peak Current 20A
 OCP current 24A

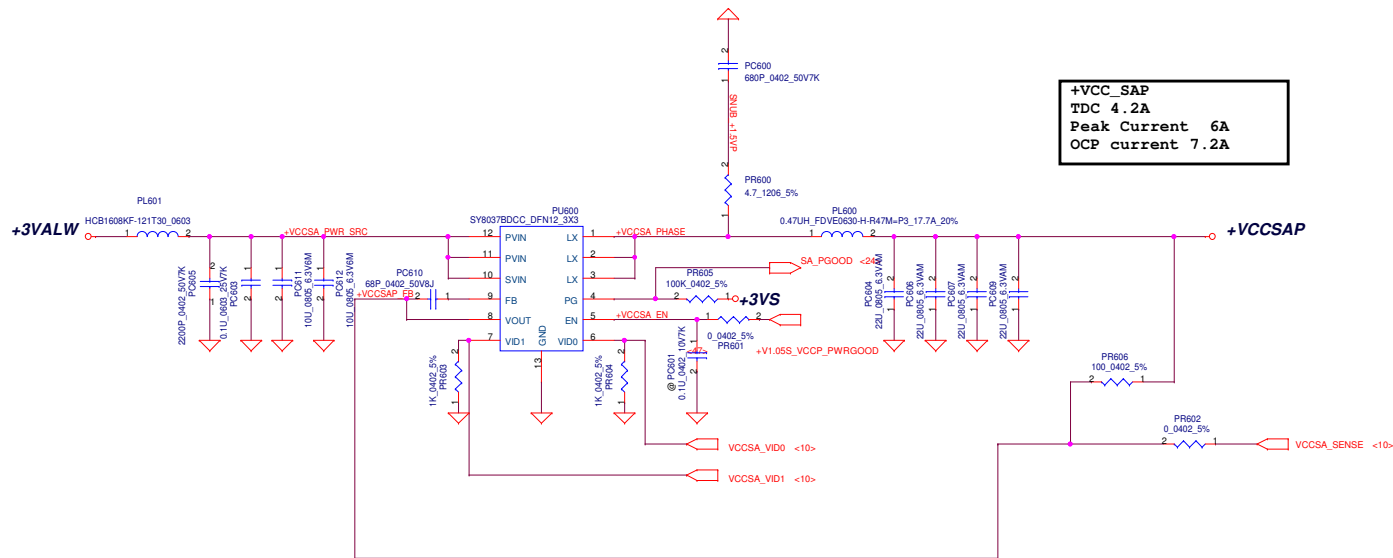
TYP MAX
 H/S Rds (on) : 10mohm , 14.5mohm
 L/S Rds (on) : 3mohm , 3.6mohm

+0.75VSP +0.75VS

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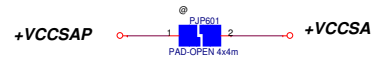
VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.8V
1	0	0.725V
1	1	0.675V

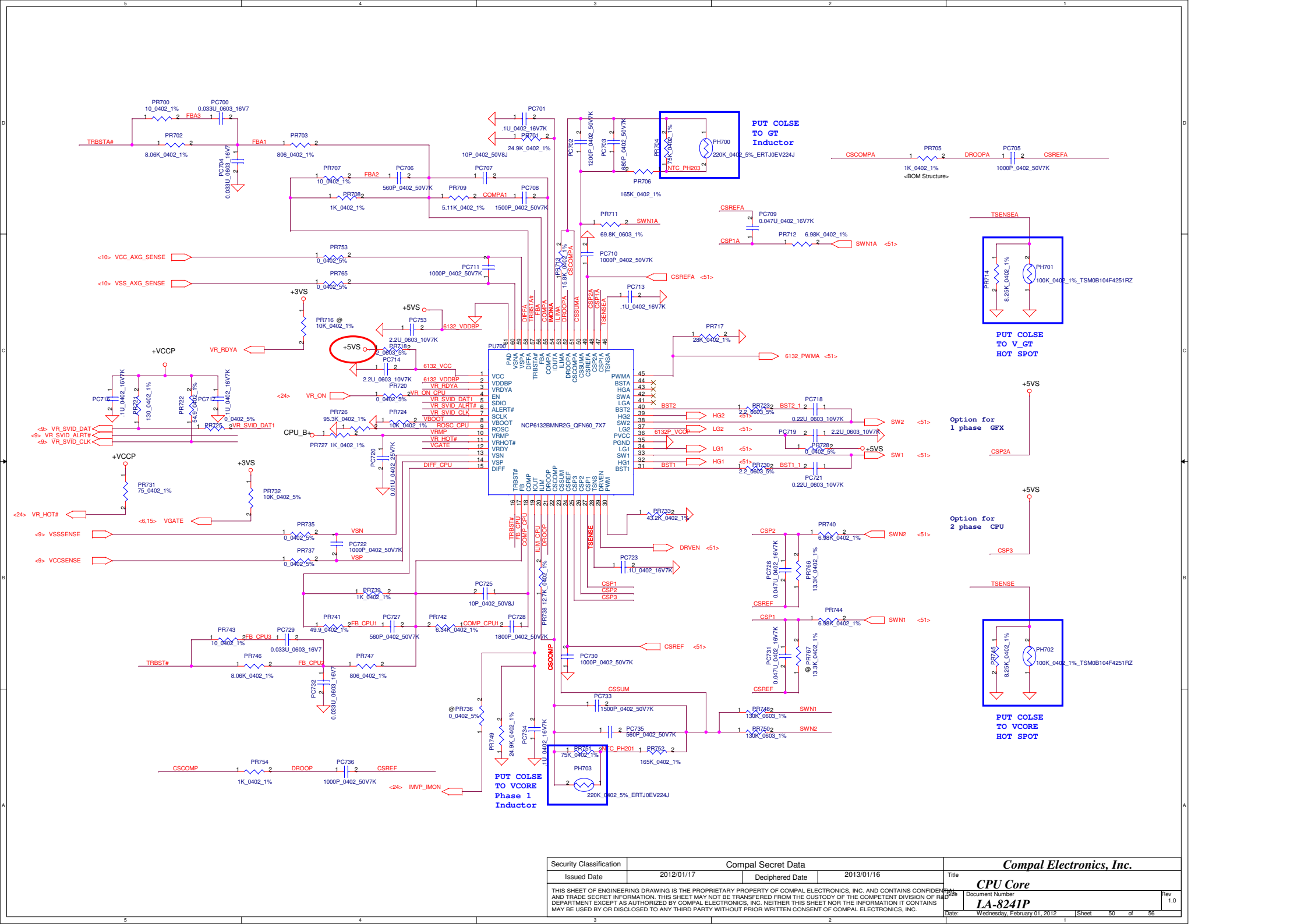
output voltage adjustable network



+VCC_SAP
TDC 4.2A
Peak Current 6A
OCP current 7.2A

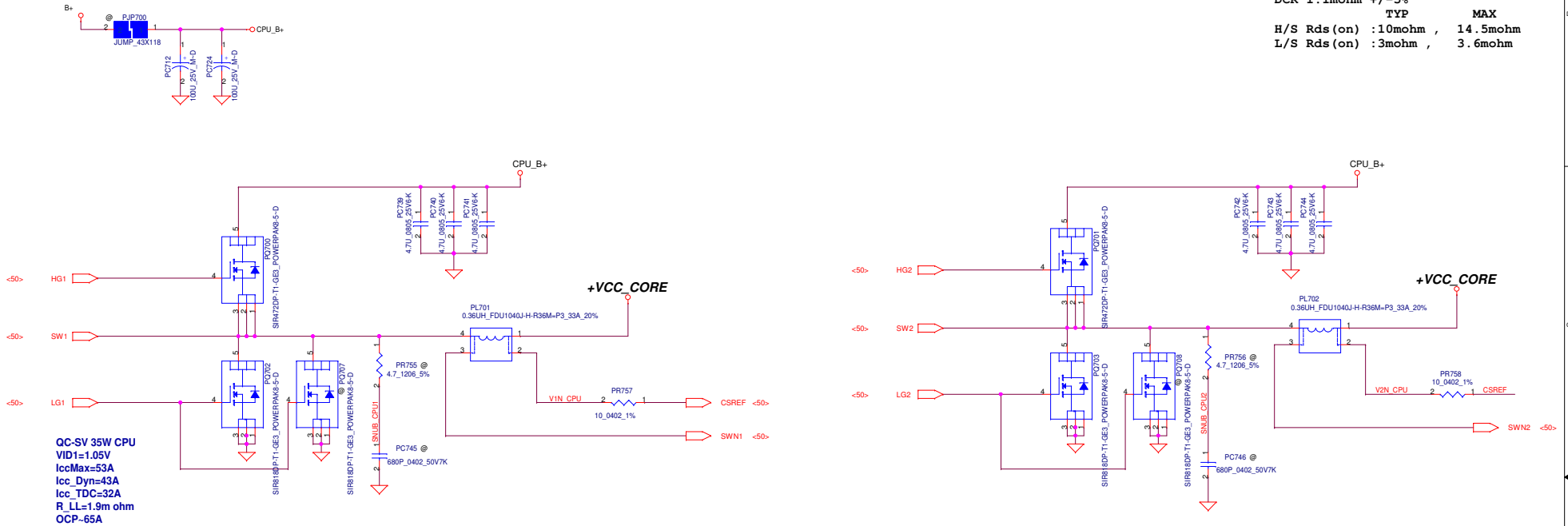
The 1k PD on the VCCSA VIDs are empty.
These should be stuffed to ensure that
VCCSA VID is 00 prior to VCCIO stability.



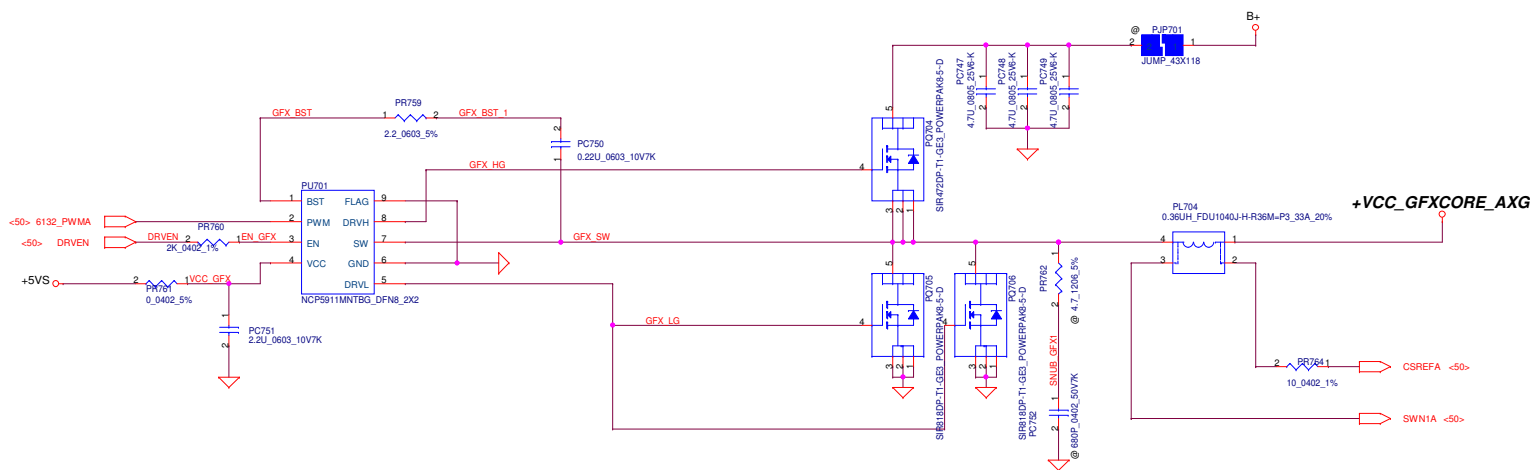


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Date:	Wednesday, February 01, 2012	Sheet	50	of 56

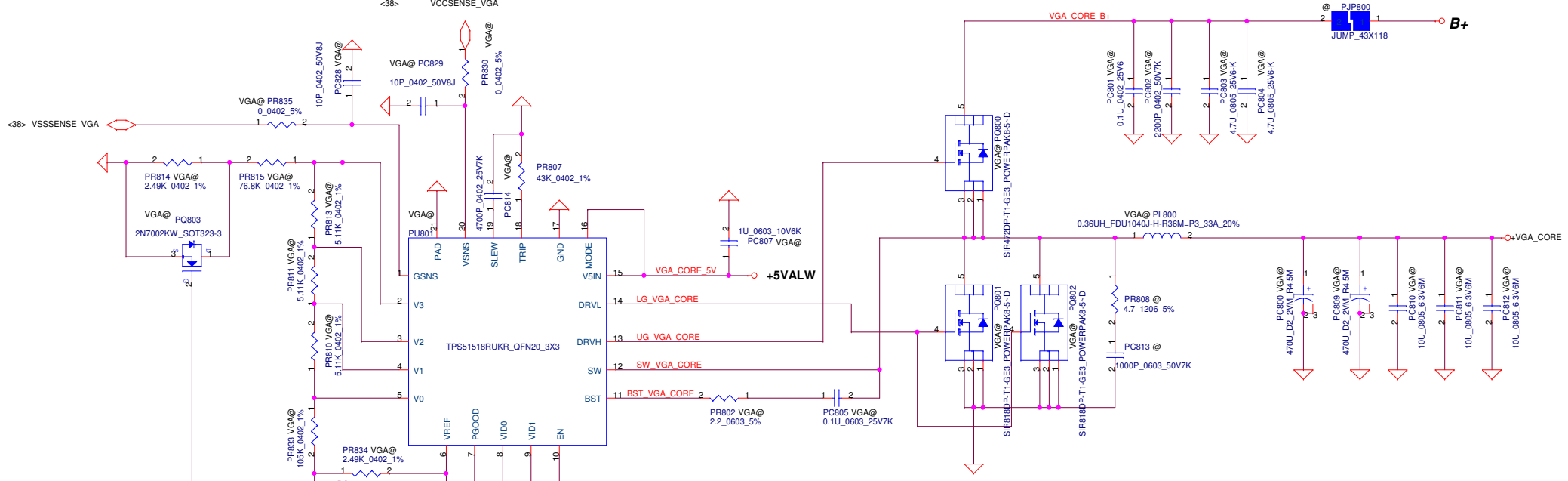
VCC_core
TDC 32A
Peak Current 53A
OCF current 65
Load line -1.9mV/A
FSW=300kHz
DCR 1.1mohm +/-5%
TYP **MAX**
H/S Rds (on) :10mohm , 14.5mohm
L/S Rds (on) :3mohm , 3.6mohm



+VCC_GFXCORE_AXG
TDC 21.5A
Peak Current 33A
OCF current 40A
Load line -3.9mV/A
FSW=300kHz
DCR 1.1mohm +/-5%
TYP **MAX**
H/S Rds (on) :10mohm , 14.5mohm
L/S Rds (on) :3mohm , 3.6mohm



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Compal Electronics, Inc. PWR-VCC_SAP			Title PWR-VCC_SAP	
Size LA-8241P			Document Number LA-8241P	
Date: Wednesday, February 01, 2012			Rev 1.0	
Sheet 51 of 56				



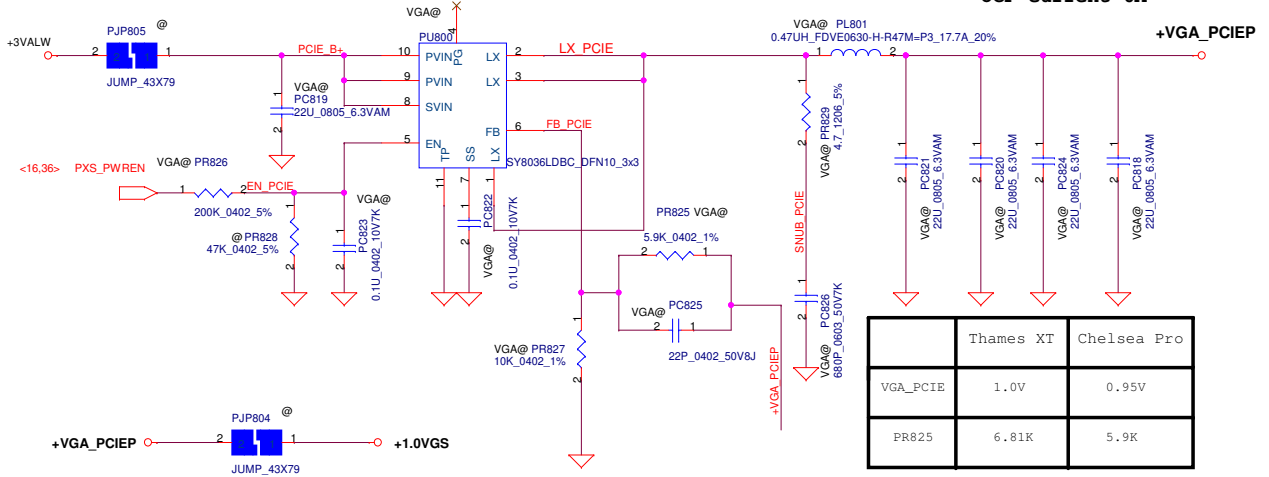
+VGA_CORE
TDC 22A
Peak Current 30A
OCV current 36A
FSW=350kHz
DCR 1.1mohm +/-5%

TYP **MAX**
H/S Rds (on) : 10mohm , 14.5mohm
L/S Rds (on) : 3mohm , 3.6mohm

+VGA_PCIE
TDC 3.6A
Peak Current 5.2A
OCV current 6A

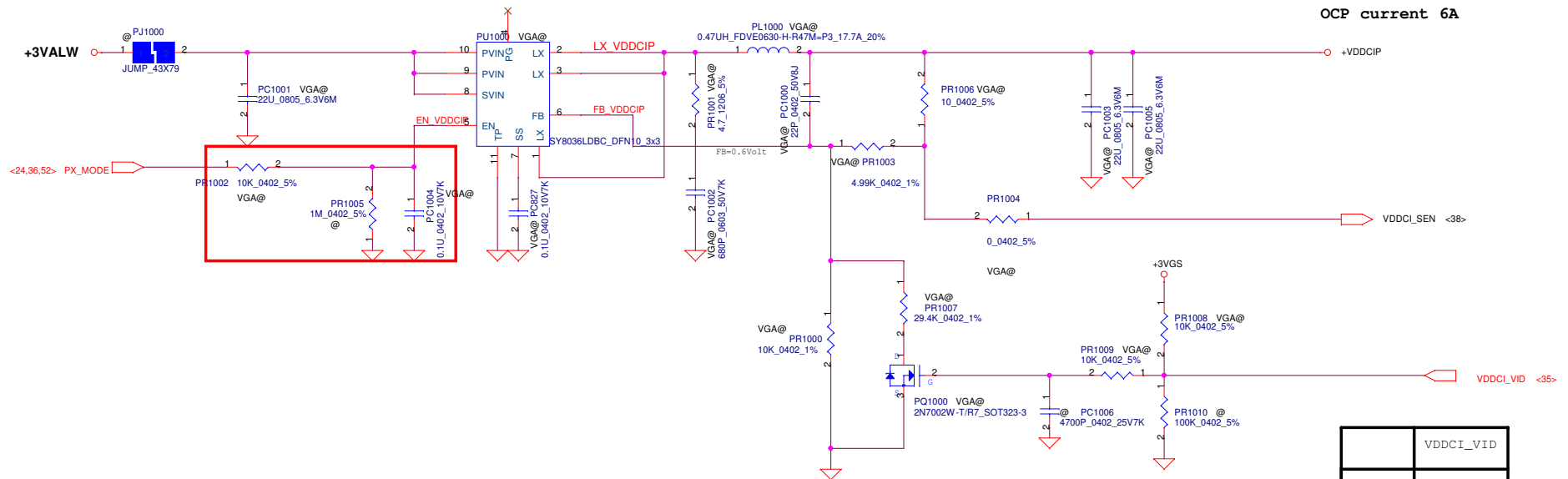
Chelsea Pro

GPU_VID1	GPU_VID0	GPU_VID2	Core Voltage Level
0	0	0	0.95V
0	0	1	0.925V
0	1	0	0.9V
0	1	1	0.875V
1	0	0	0.85V
1	0	1	0.825V
1	1	0	0.8V
1	1	1	0.775V

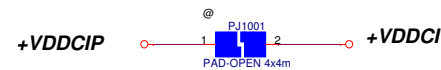


	Thames XT	Chelsea Pro
VGA_PCIE	1.0V	0.95V
PR825	6.81K	5.9K

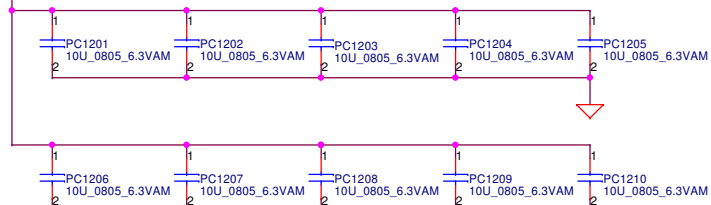
+VDDCI
TDC 2.8A
Peak Current 4A
OCp current 6A



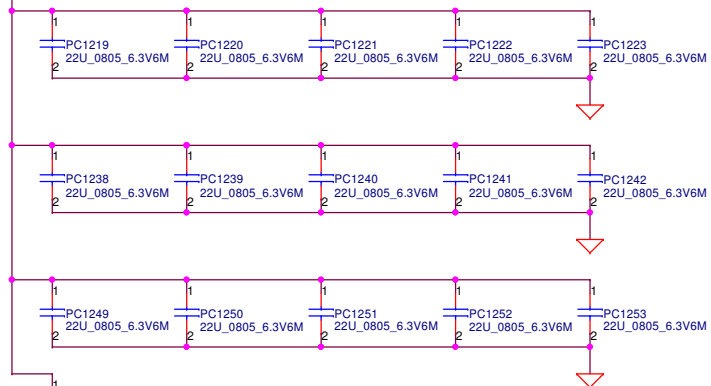
	VDDCI_VID
High	1V
Low	0.9V



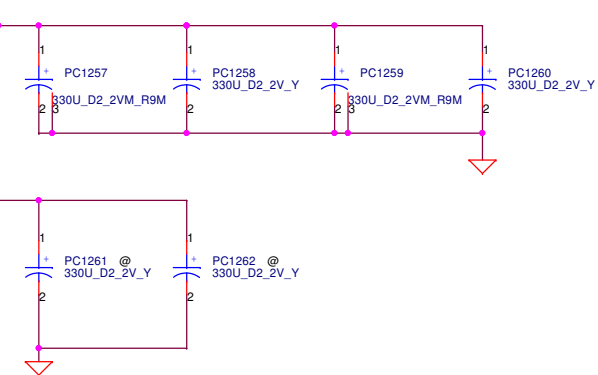
+VCC_CORE



+VCC_CORE

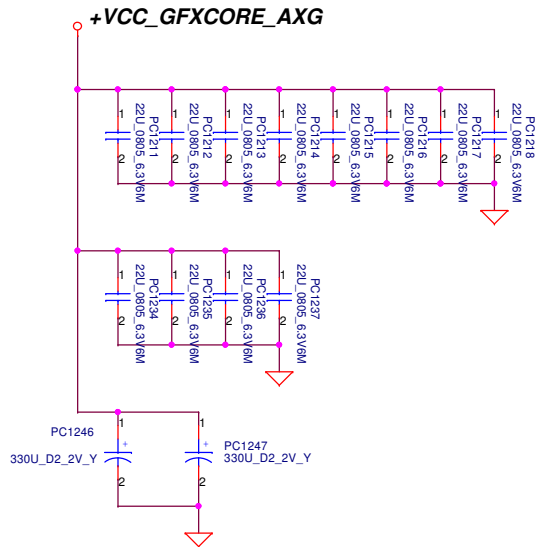


+VCC_CORE



+VCC_CORE

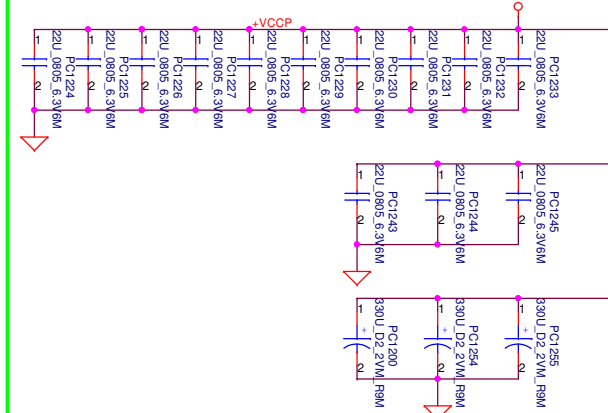
+VCC_GFXCORE_AXG



Below is 458544_CRV_PDDG_0.5 Table 5-8.

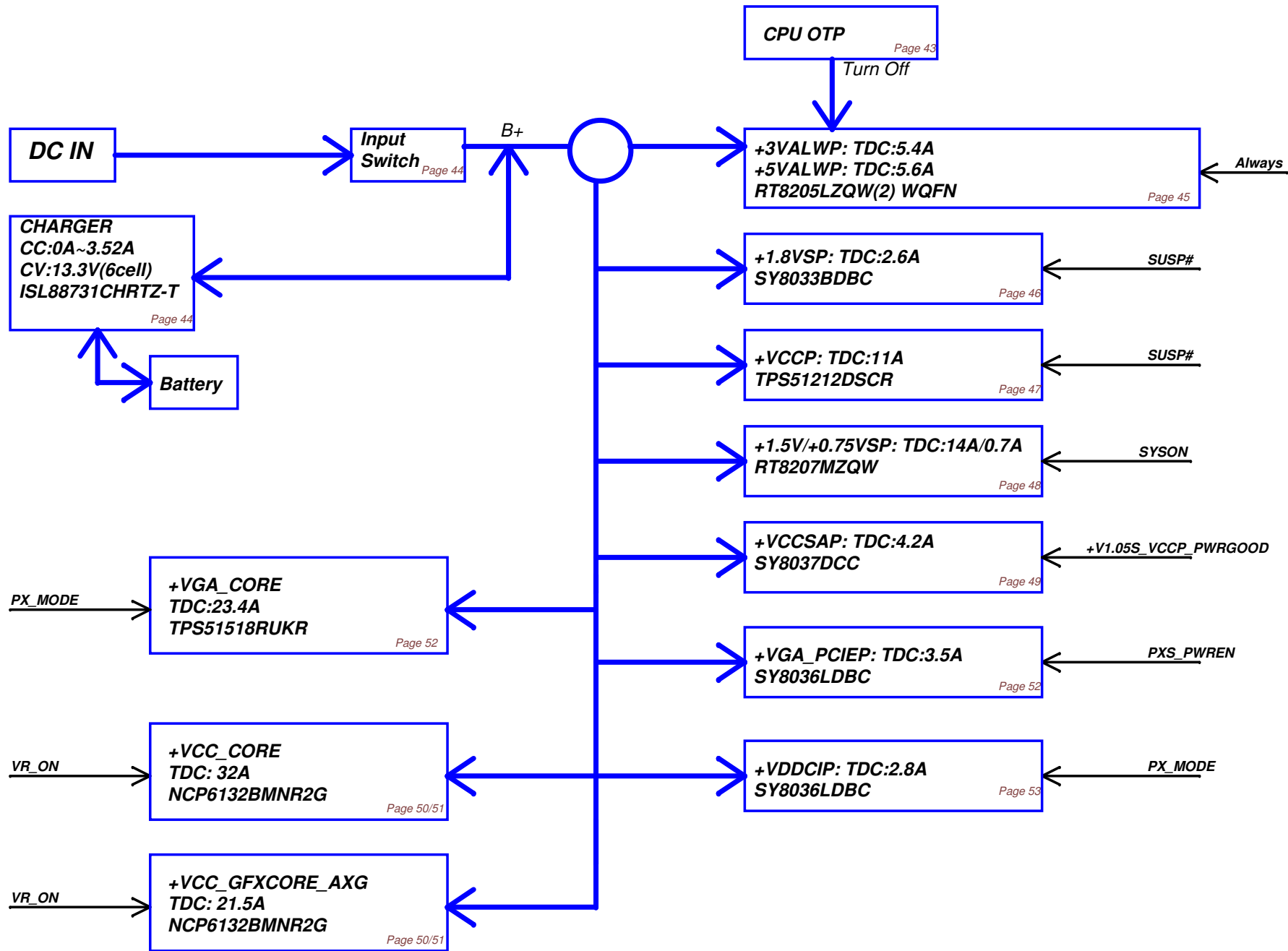
Socket Bottom	5 x 22 μ F (0805) 5 x (0805) no-stuff sites
Socket Top	7 x 22 μ F (0805) 2 x (0805) no-stuff sites

+VCCP



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Size	Document Number	Date		Sheet	Rev
	LA-8241P	Wednesday, February 01, 2012		54 of 56	1.0

Power block



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				LA-8241P	0.2
Date: Wednesday, February 01, 2012				Sheet	55 of 56

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