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61	VGA POWER(GMCH)		
62	SYSPWR(+1_5VRUN/+1_05VRUN)		
63	HDD PWR (+12VRUN)		
64	Others power plan		
65	OVP protection		
66	DB CONNS		
67	CRT		
68	HOLE/BOSS PAD		

BOM OPTION

COMPONENT	WINBOND	ENE
C72,RP9	NC	STUFF
R110	4.7K	47K

COMPONENT	Samsung	Qimonda
R26	Stuff	NC
R39	NC	Stuff

PCB P/N: __-_____-__SA
__-_____-__SA
__-_____-__SA

Project Code & Schematics Subject: M630/M640 Main Board

	M630GM	M630PM	M640GM	M640PM
CR_	V		V	
NV_		V		V
NC_	V	V	V	V
Exclude "M640_"	V	V		
(Default)			V	

P. Leader	Check by	Design by

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Title: ***Index Page***

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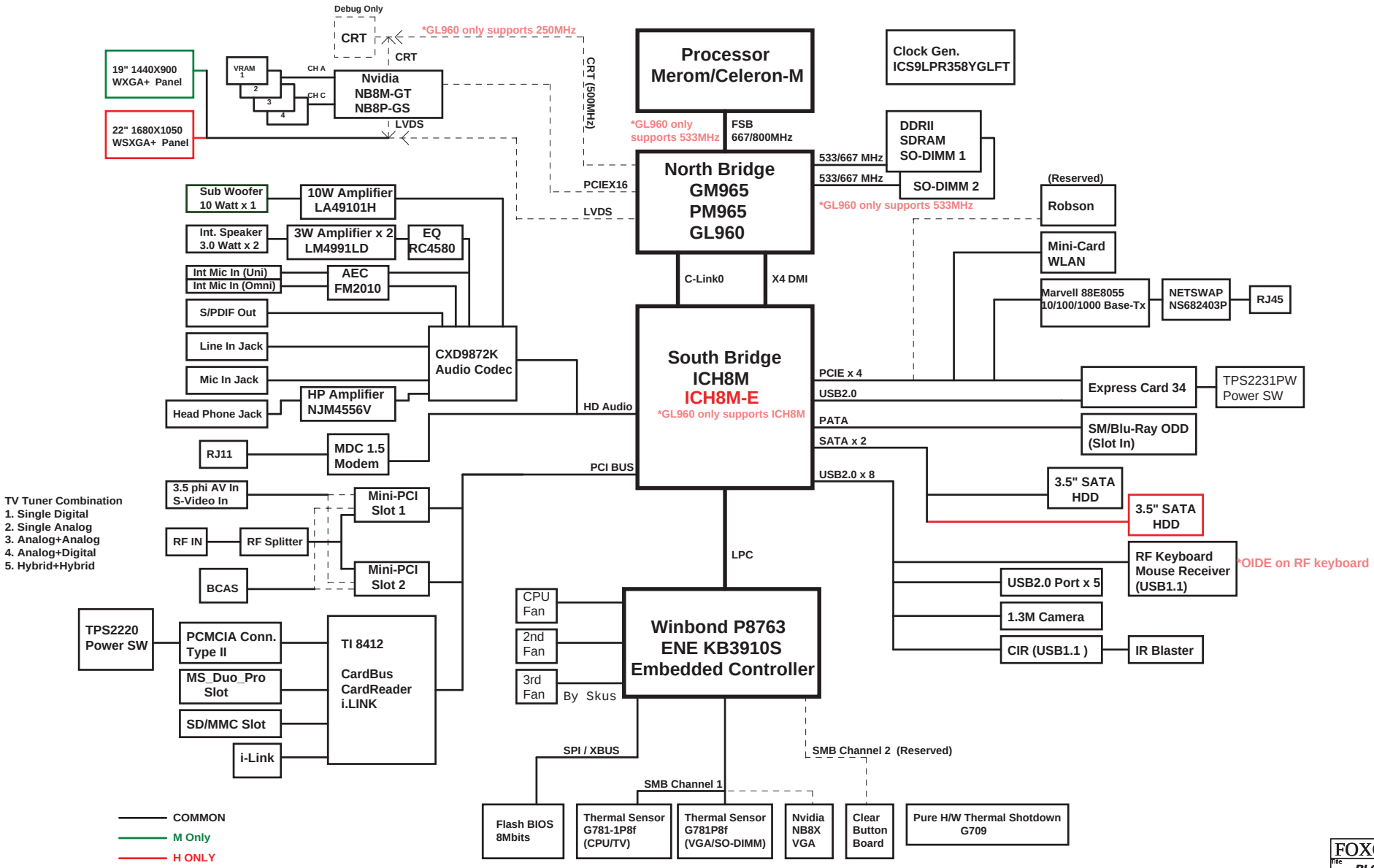
M630/640 Block Diagram (19"/22" Wide Screen)



SYSTEM DC/DC MAX8734A P.57

INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC

SYSTEM DC/DC SC339 P.61

INPUTS	OUTPUTS
+1_8V_S3_SUS	+1_5VRUN

SC486 P.58

INPUTS	OUTPUTS
DCBATOUT	+1_8V_S3_SUS +0_9V_S3_SUS

CPU DC/DC ISL6262A P.59

INPUTS	OUTPUTS
DCBATOUT	VHCORE

CPU DC/DC MAX8546 P.62

INPUTS	OUTPUTS
DCBATOUT	+12VRUN

SYSTEM DC/DC GMT923/GMT966 P.63

INPUTS	OUTPUTS
+1_8V_S3_SUS	+1_25VRUN

SYSTEM DC/DC OZ811 GMT966(PEX_VDD) P.60

INPUTS	OUTPUTS
DCBATOUT	+1_05VRUN
DCBATOUT	NV_VDD
+1_8V_S3_SUS	PEX_VDD

Nvidia Gfx VDDC

INPUTS	OUTPUTS
+VGFX_CORE	+1_05VRUN (or NV_VDD)

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Title: BLOCK DIAGRAM

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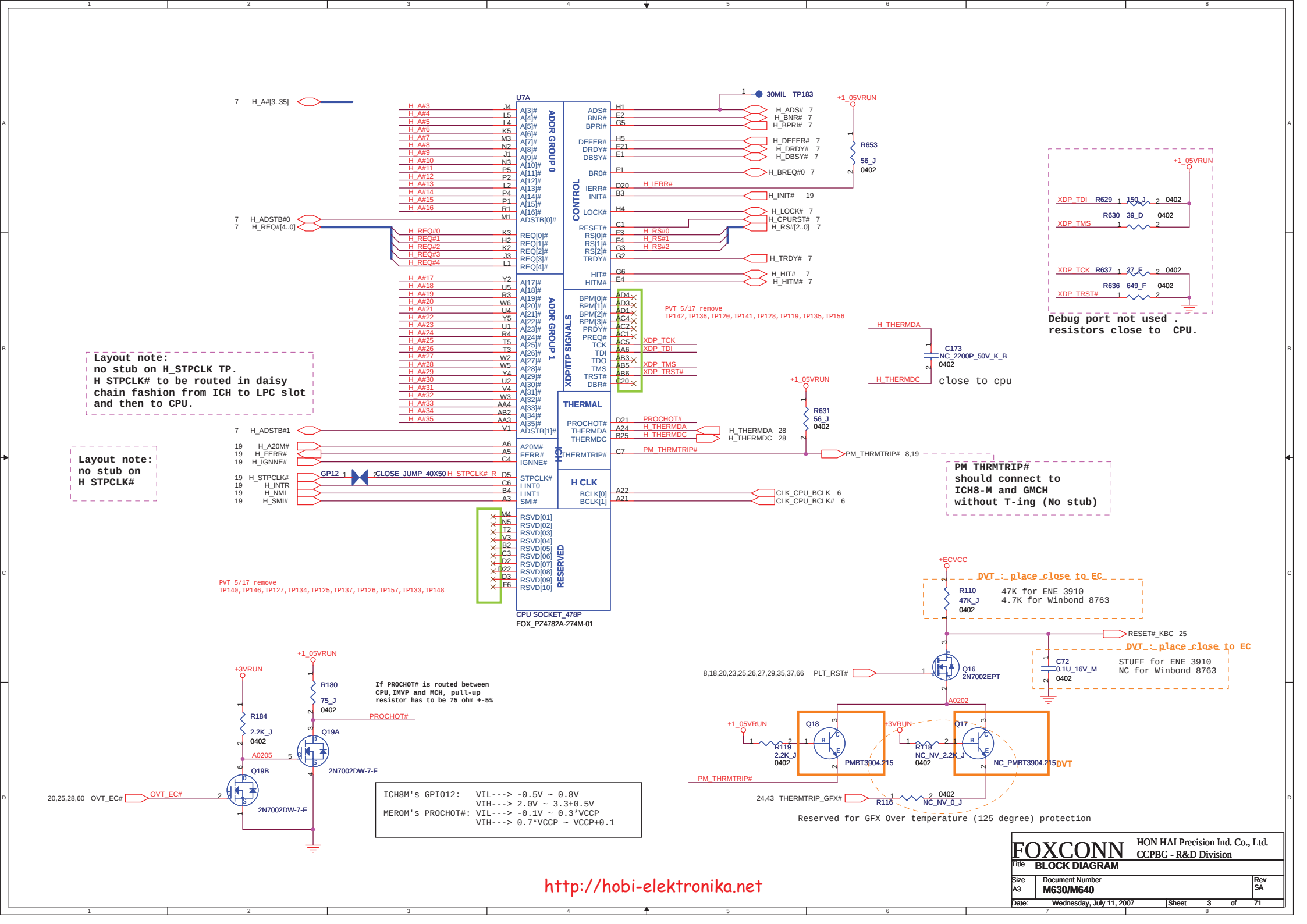

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Title	BLOCK DIAGRAM		
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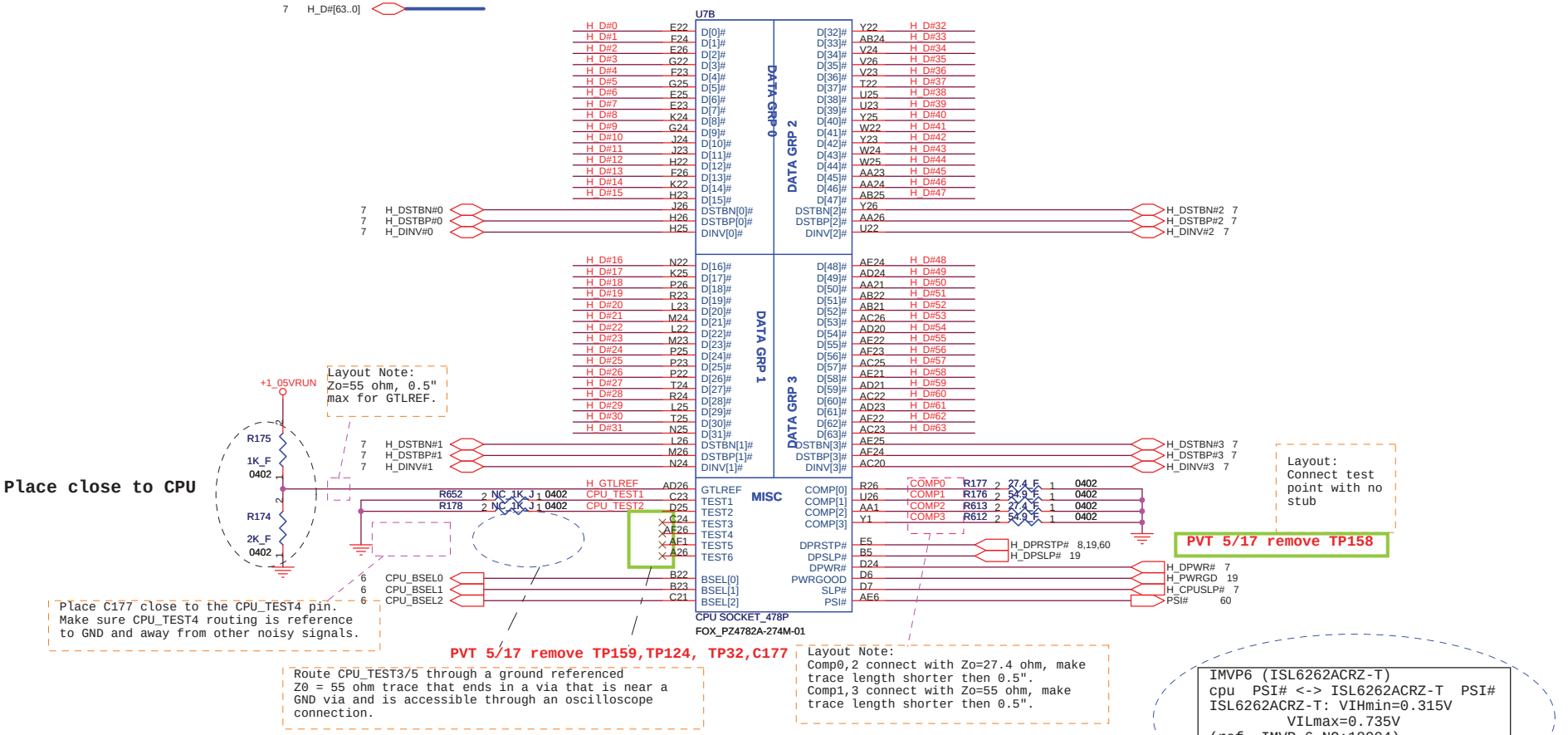

FSB Frequency Table:

BSEL[2:0]	Freq.(MHz)
L L L	266MHz
L L H	133MHz
L H H	166MHz
L H L	200MHz
H H L	400MHz
H H H	Reserve
H L H	100MHz
H L L	333MHz

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Title: Merom (HOST BUS) 2/3

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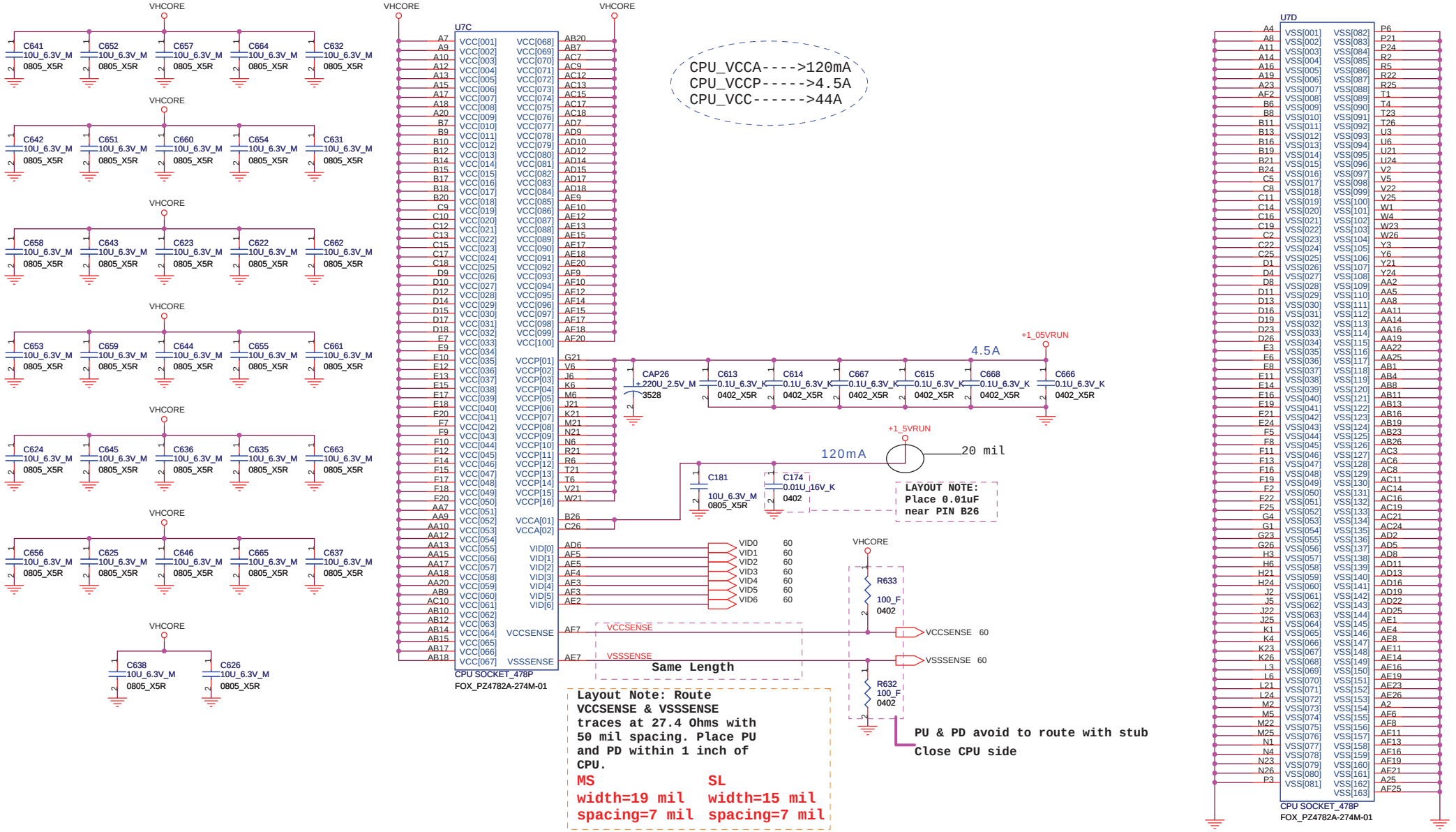

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Title: *Merom (POWER/GROUND) 3/3*

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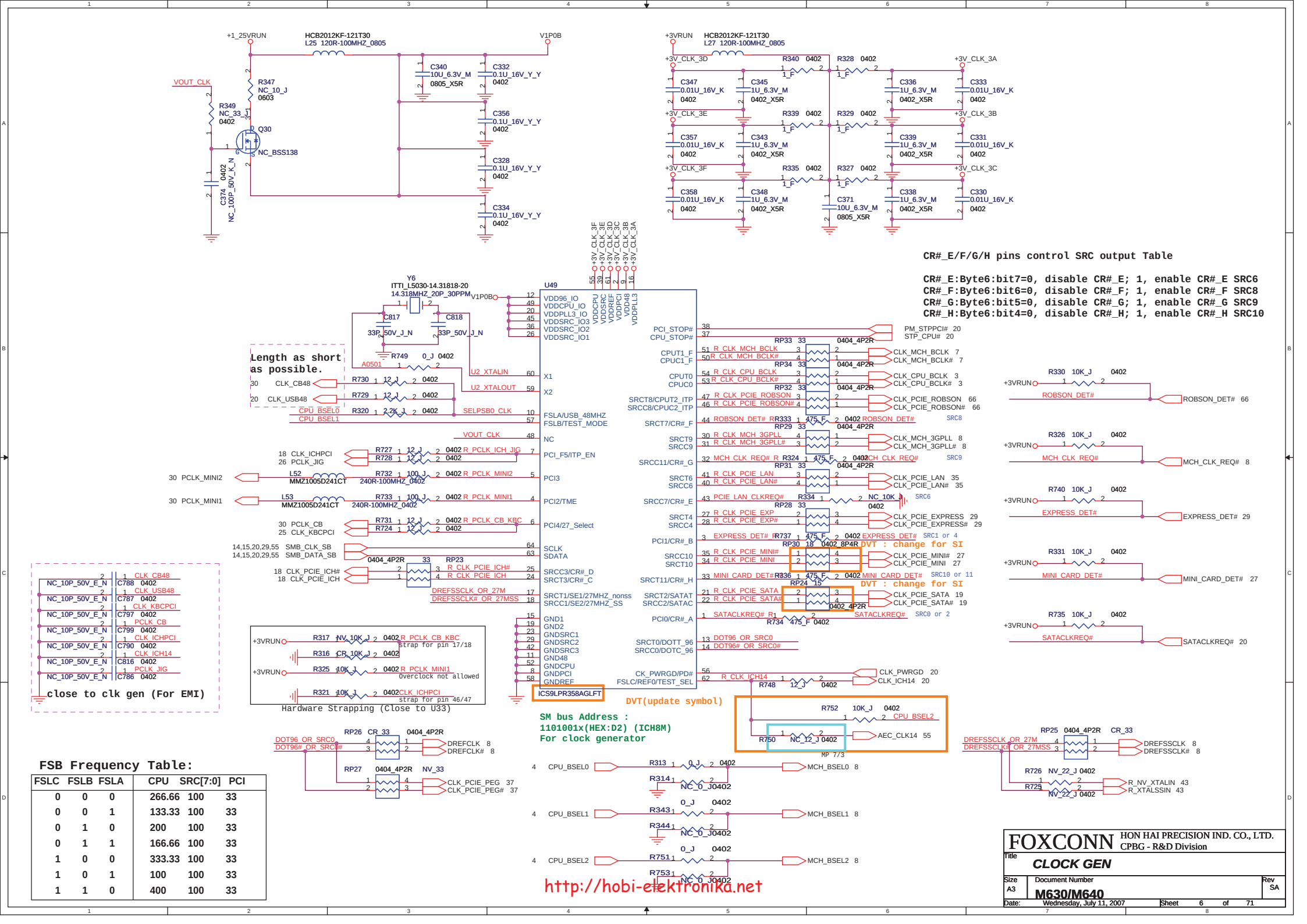
+1_25VRUN
HCB2012KF-121T30
L25 120R-100MHZ_0805
V1P0B
VOUT_CLK
R347 NC_10_J 0603
R349 NC_33_J 0402
Q30 NC_BSS138
C374 0402 NC_100P_50V_K_N
C340 10U_6.3V_M 0805_X5R
C332 0.1U_16V_Y_Y 0402
C356 0.1U_16V_Y_Y 0402
C328 0.1U_16V_Y_Y 0402
C334 0.1U_16V_Y_Y 0402
+3VRUN
HCB2012KF-121T30
L27 120R-100MHZ_0805
+3V_CLK_3D
+3V_CLK_3E
+3V_CLK_3F
+3V_CLK_3A
+3V_CLK_3B
+3V_CLK_3C
R340 0402 1_F
R339 0402 1_F
R335 0402 1_F
R328 0402 1_F
R329 0402 1_F
R327 0402 1_F
C347 0.01U_16V_K 0402
C357 0.01U_16V_K 0402
C358 0.01U_16V_K 0402
C345 1U_6.3V_M 0402_X5R
C343 1U_6.3V_M 0402_X5R
C348 1U_6.3V_M 0402_X5R
C371 10U_6.3V_M 0805_X5R
C336 1U_6.3V_M 0402_X5R
C339 1U_6.3V_M 0402_X5R
C338 1U_6.3V_M 0402_X5R
C333 0.01U_16V_K 0402
C331 0.01U_16V_K 0402
C330 0.01U_16V_K 0402
+3V_CLK_3F
+3V_CLK_3E
+3V_CLK_3D
+3V_CLK_3C
+3V_CLK_3B
+3V_CLK_3A
Y6
ITTI_L5030-14.31818-20
14.318MHZ_20P_30PPM
C817 33P_50V_J_N
C818 33P_50V_J_N
Length as short as possible.
R749 0_J 0402
A0501
U2_XTALIN
U2_XTALOUT
CPU_BSEL0
CPU_BSEL1
U49
VDD96_IO
VDDCPU_IO
VDDPLL3_IO
VDDSRC_IO3
VDDSRC_IO2
VDDSRC_IO1
VDDCPU
VDDSRC
VDDREF
VDD48
VDDPLL3
X1
X2
FSLA/USB_48MHZ
FSLB/TEST_MODE
NC
PCI_F5/ITP_EN
PCI3
PCI2/TME
PCI4/27_Select
SCLK
SDATA
SRCC3/CR#_D
SRCT3/CR#_C
SRCT1/SE1/27MHZ_nonss
SRCC1/SE2/27MHZ_SS
GND1
GND2
GNDSRC1
GNDSRC2
GNDSRC3
GND48
GNDCPU
GNDPCI
GNDREF
ICS9LPR358AGLFT
PCI_STOP#
CPU_STOP#
CPUT1_F
CPUC1_F
CPUT0
CPUC0
SRCT8/CPUT2_ITP
SRCC8/CPUC2_ITP
SRCT7/CR#_F
SRCT9
SRCC9
SRCC11/CR#_G
SRCT6
SRCC6
SRCC7/CR#_E
SRCT4
SRCC4
PCI1/CR#_B
SRCC10
SRCT10
SRCT11/CR#_H
SRCT2/SATAT
SRCC2/SATAC
PCI0/CR#_A
SRCT0/DOTT_96
SRCC0/DOTC_96
CK_PWRGD/PD#
FSLC/REF0/TEST_SEL
PM_STPPCI# 20
STP_CPU# 20
RP33 33 0404_4P2R
RP34 33 0404_4P2R
RP32 33 0404_4P2R
RP29 33 0404_4P2R
RP31 33 0404_4P2R
RP28 33 0402
RP30 18 0402_8P4R
RP24 15 0402_4P2R
R_CLK_MCH_BCLK
R_CLK_CPU_BCLK
R_CLK_PCIE_ROBSON
R_CLK_MCH_3GPLL
R_CLK_PCIE_LAN
R_CLK_PCIE_EXP
R_CLK_PCIE_MINI
R_CLK_PCIE_SATA
CLK_MCH_BCLK 7
CLK_MCH_BCLK# 7
CLK_CPU_BCLK 3
CLK_CPU_BCLK# 3
CLK_PCIE_ROBSON 66
CLK_PCIE_ROBSON# 66
CLK_MCH_3GPLL 8
CLK_MCH_3GPLL# 8
CLK_PCIE_LAN 35
CLK_PCIE_LAN# 35
CLK_PCIE_EXPRESS 29
CLK_PCIE_EXPRESS# 29
CLK_PCIE_MINI 27
CLK_PCIE_MINI# 27
CLK_PCIE_SATA 19
CLK_PCIE_SATA# 19
ROBSON_DET# 66
MCH_CLK_REQ# 8
EXPRESS_DET# 29
MINI_CARD_DET# 27
SATACLKREQ# 20
DVT : change for SI
DVT : change for SI
SRC8
SRC9
SRC6
SRC1 or 4
SRC10 or 11
SRC0 or 2
DOT96_OR_SRC0
DOT96#_OR_SRC0#
CLK_PWRGD 20
CLK_ICH14 20
R748 12_J 0402
R752 10K_J 0402
CPU_BSEL2
R750 NC_12_J 0402
AEC_CLK14 55
MP 7/3
DVT(update symbol)
SM bus Address :
1101001x(HEX:D2) (ICH8M)
For clock generator
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
R313 0_J 0402
R314 NC_0_J0402
R343 0_J 0402
R344 NC_0_J0402
R751 0_J 0402
R753 NC_0_J0402
MCH_BSEL0 8
MCH_BSEL1 8
MCH_BSEL2 8
R330 10K_J 0402
R326 10K_J 0402
R740 10K_J 0402
R331 10K_J 0402
R735 10K_J 0402
R333 475_F 0402
R324 475_F 0402
R737 475_F 0402
R336 475_F 0402
R734 475_F 0402
NC_10K_J 0402
R727 12_J 0402
R728 12_J 0402
R729 12_J 0402
R730 12_J 0402
R320 2.2K_J 0402
R731 12_J 0402
R724 12_J 0402
R732 100_J 0402
R733 100_J 0402
L52 MMZ1005D241CT 240R-100MHZ_0402
L53 MMZ1005D241CT 240R-100MHZ_0402
R_PCLK_ICH_JIG
R_PCLK_MINI2
R_PCLK_MINI1
R_PCLK_CB_KBC
R_CLK_PCIE_ICH
DREFSSCLK_OR_27M
DREFSSCLK#_OR_27MSS
SELPSB0_CLK
VOUT_CLK
CLK_CB48
CLK_USB48
CLK_KBCPCI
PCLK_CB
CLK_ICHPCI
CLK_ICH14
PCLK_JIG
NC_10P_50V_E_N
C788 0402
C787 0402
C797 0402
C799 0402
C790 0402
C816 0402
C786 0402
close to clk gen (For EMI)
Hardware Strapping (Close to U33)
R317 NV_10K_J 0402 R_PCLK_CB_KBC strap for pin 17/18
R316 CR_10K_J 0402
R325 10K_J 0402 R_PCLK_MINI1 Overclock not allowed
R321 10K_J 0402 CLK_ICHPCI strap for pin 46/47
RP26 CR_33 0404_4P2R
RP27 0404_4P2R NV_33
DREFCLK 8
DREFCLK# 8
CLK_PCIE_PEG 37
CLK_PCIE_PEG# 37
RP25 0404_4P2R CR_33
DREFSSCLK 8
DREFSSCLK# 8
R726 NV_22_J 0402
R725 NV_22_J 0402
R_NV_XTALIN 43
R_XTALSSIN 43
CR#_E/F/G/H pins control SRC output Table
CR#_E:Byte6:bit7=0, disable CR#_E; 1, enable CR#_E SRC6
CR#_F:Byte6:bit6=0, disable CR#_F; 1, enable CR#_F SRC8
CR#_G:Byte6:bit5=0, disable CR#_G; 1, enable CR#_G SRC9
CR#_H:Byte6:bit4=0, disable CR#_H; 1, enable CR#_H SRC10
FSB Frequency Table:
FSLC FSLB FSLA CPU SRC[7:0] PCI
0 0 0 266.66 100 33
0 0 1 133.33 100 33
0 1 0 200 100 33
0 1 1 166.66 100 33
1 0 0 333.33 100 33
1 0 1 100 100 33
1 1 0 400 100 33
http://hobi-elektronika.net
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Title
CLOCK GEN
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Document Number
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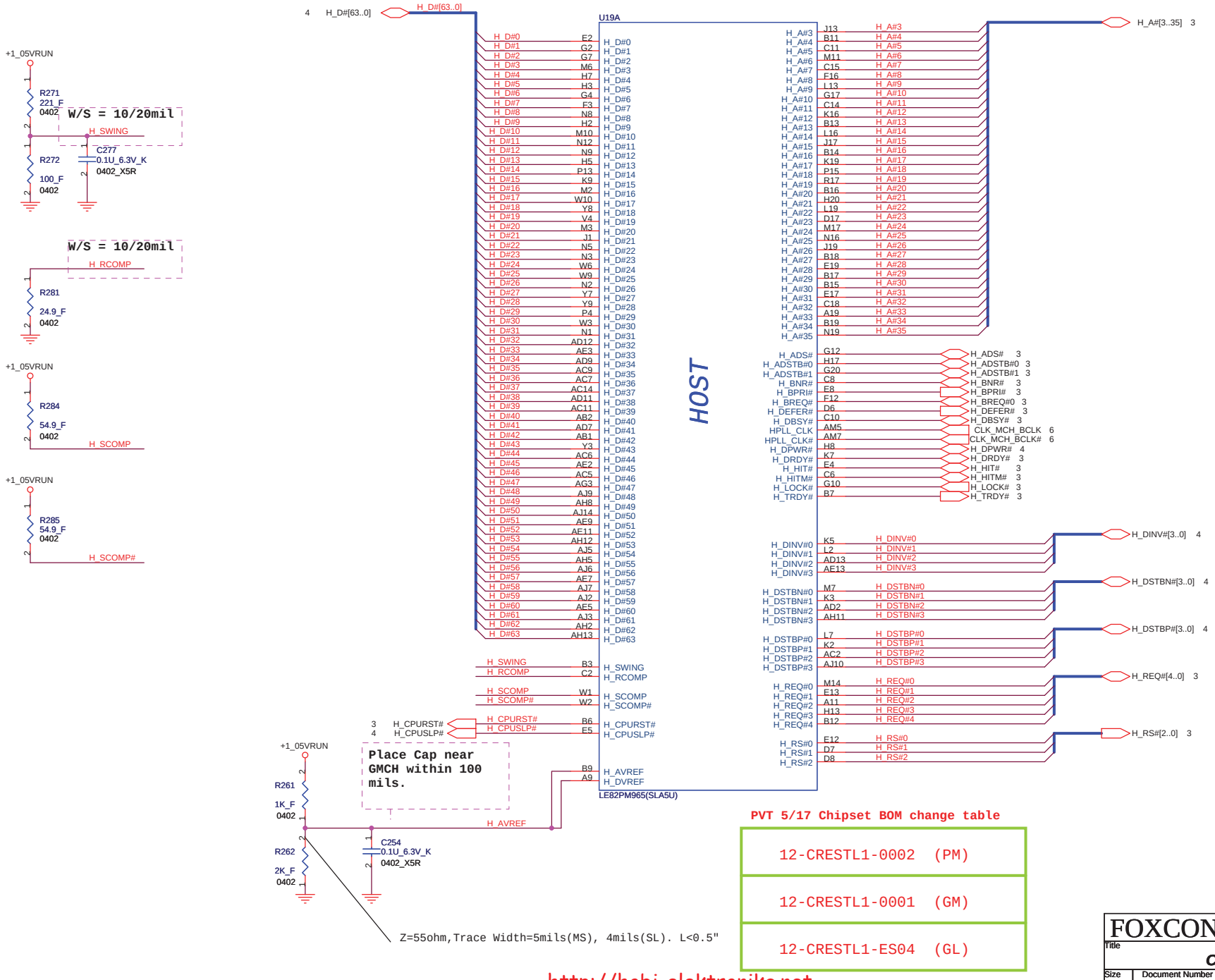

PVT 5/17 Chipset BOM change table

12-CRESTL1-0002 (PM)
12-CRESTL1-0001 (GM)
12-CRESTL1-ES04 (GL)

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Title: *Crestline (HOST) 1/of 7*

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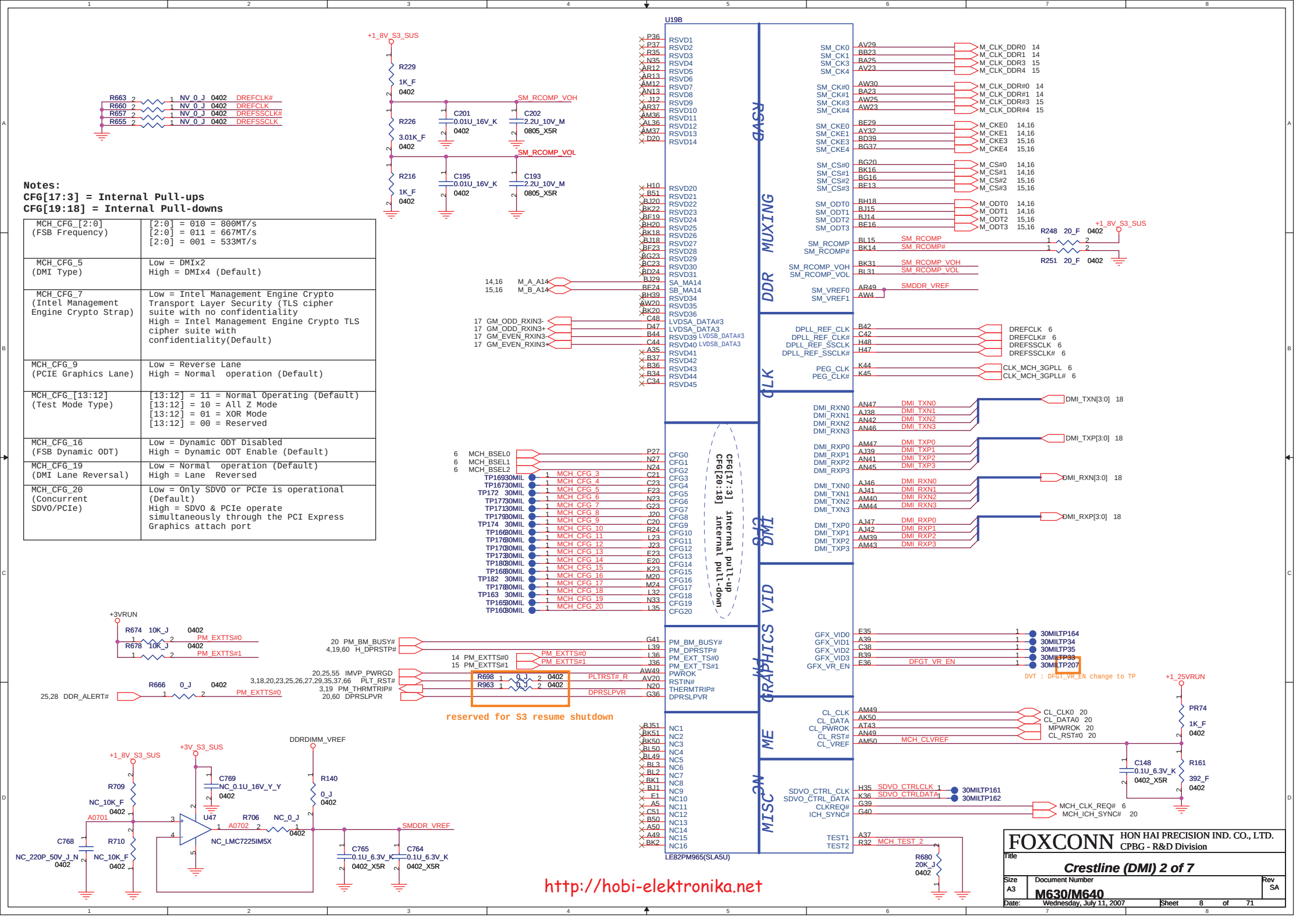
U19B
R663 NV_0_J 0402 DREFCLK#
R660 NV_0_J 0402 DREFCLK
R657 NV_0_J 0402 DREFSSCLK#
R655 NV_0_J 0402 DREFSSCLK
+1_8V_S3_SUS
R229 1K_F 0402
R226 3.01K_F 0402
R216 1K_F 0402
SM_RCOMP_VOH
SM_RCOMP_VOL
C201 0.01U_16V_K 0402
C202 2.2U_10V_M 0805_X5R
C195 0.01U_16V_K 0402
C193 2.2U_10V_M 0805_X5R
Notes:
CFG[17:3] = Internal Pull-ups
CFG[19:18] = Internal Pull-downs
MCH_CFG_[2:0] (FSB Frequency) | [2:0] = 010 = 800MT/s [2:0] = 011 = 667MT/s [2:0] = 001 = 533MT/s
MCH_CFG_5 (DMI Type) | Low = DMIx2 High = DMIx4 (Default)
MCH_CFG_7 (Intel Management Engine Crypto Strap) | Low = Intel Management Engine Crypto Transport Layer Security (TLS cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality(Default)
MCH_CFG_9 (PCIE Graphics Lane) | Low = Reverse Lane High = Normal operation (Default)
MCH_CFG_[13:12] (Test Mode Type) | [13:12] = 11 = Normal Operating (Default) [13:12] = 10 = All Z Mode [13:12] = 01 = XOR Mode [13:12] = 00 = Reserved
MCH_CFG_16 (FSB Dynamic ODT) | Low = Dynamic ODT Disabled High = Dynamic ODT Enable (Default)
MCH_CFG_19 (DMI Lane Reversal) | Low = Normal operation (Default) High = Lane Reversed
MCH_CFG_20 (Concurrent SDVO/PCIe) | Low = Only SDVO or PCIe is operational (Default) High = SDVO & PCIe operate simultaneously through the PCI Express Graphics attach port
CFG[17:3] internal pull-up
CFG[20:18] internal pull-down
reserved for S3 resume shutdown
LE82PM965(SLA5U)
http://hobi-elektronika.net
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Crestline (DMI) 2 of 7
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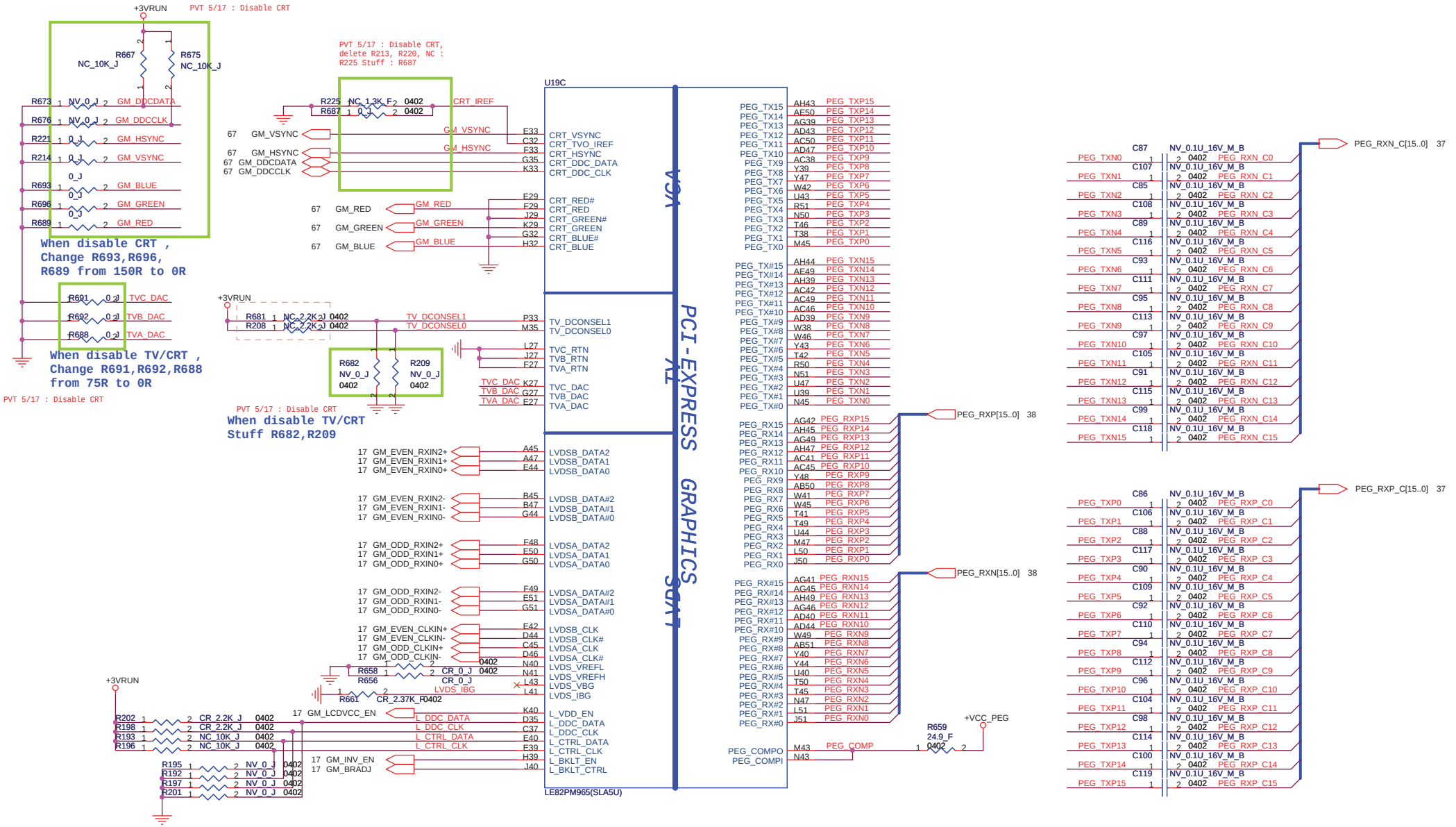

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Title: Crestline (Gfx) 3 of 7

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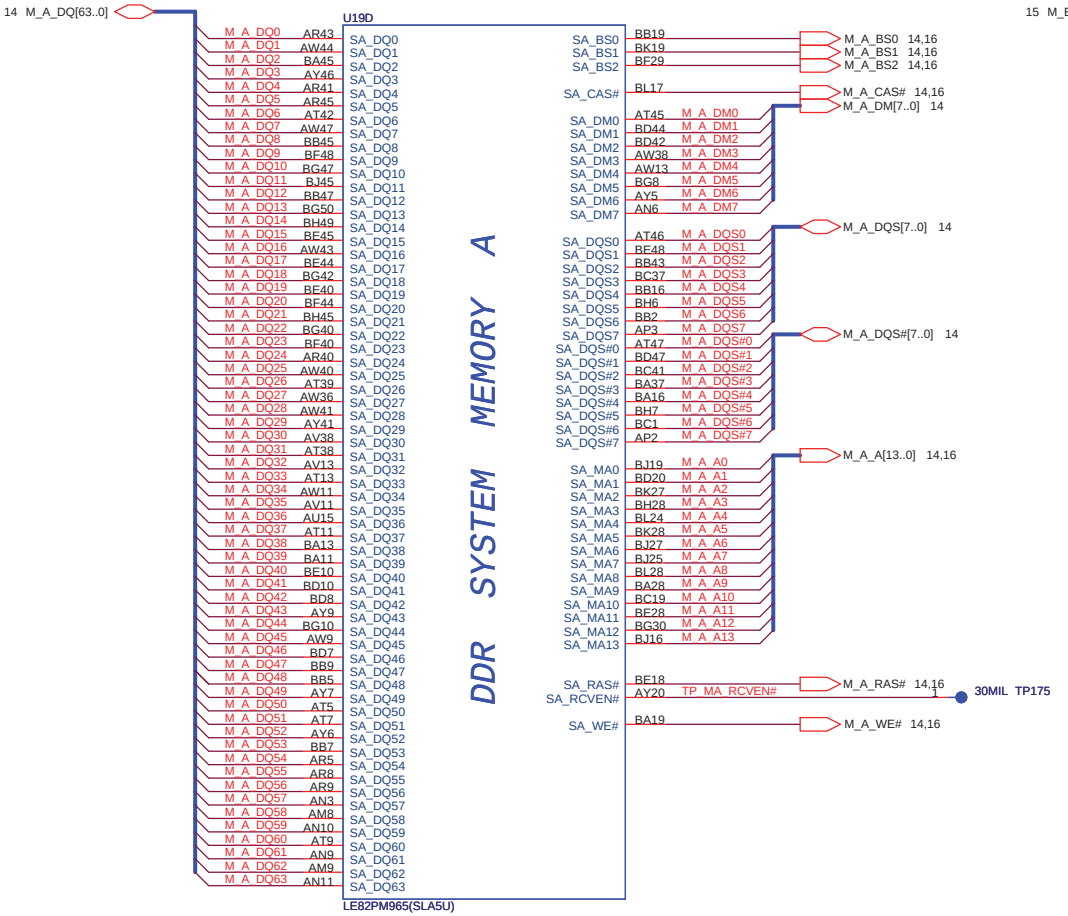

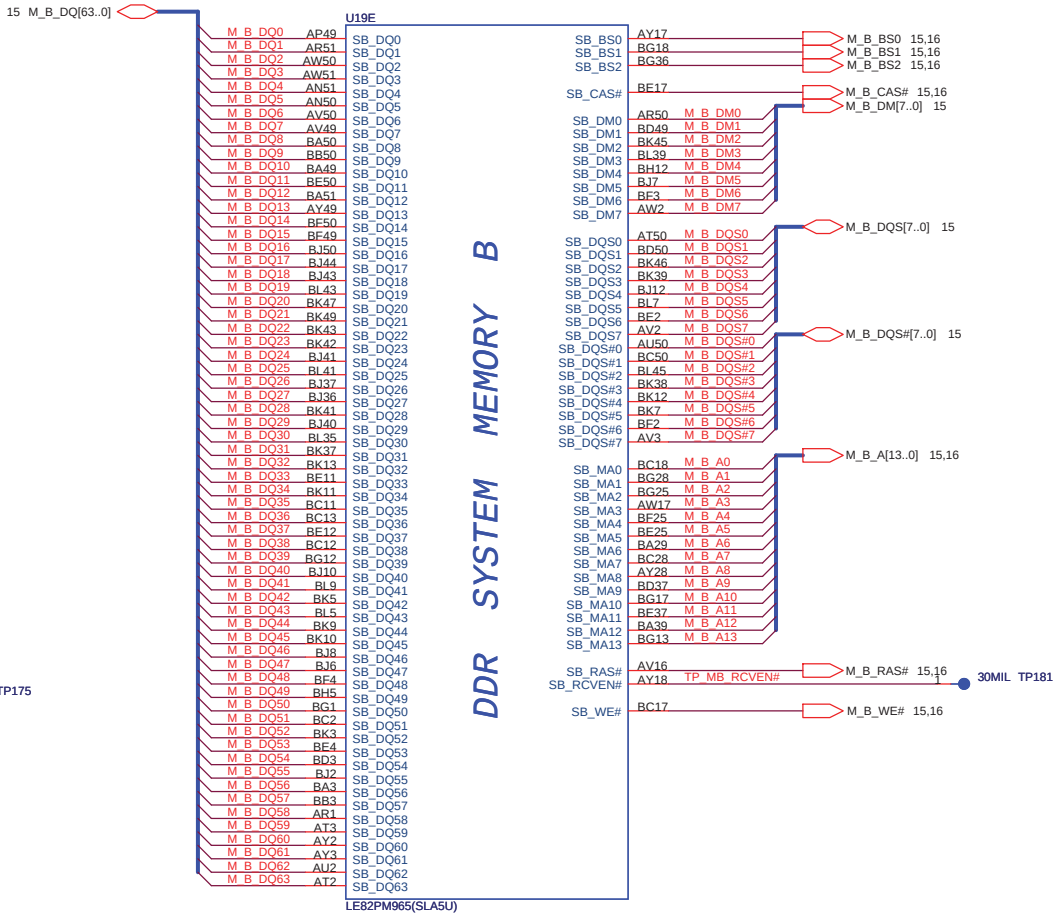

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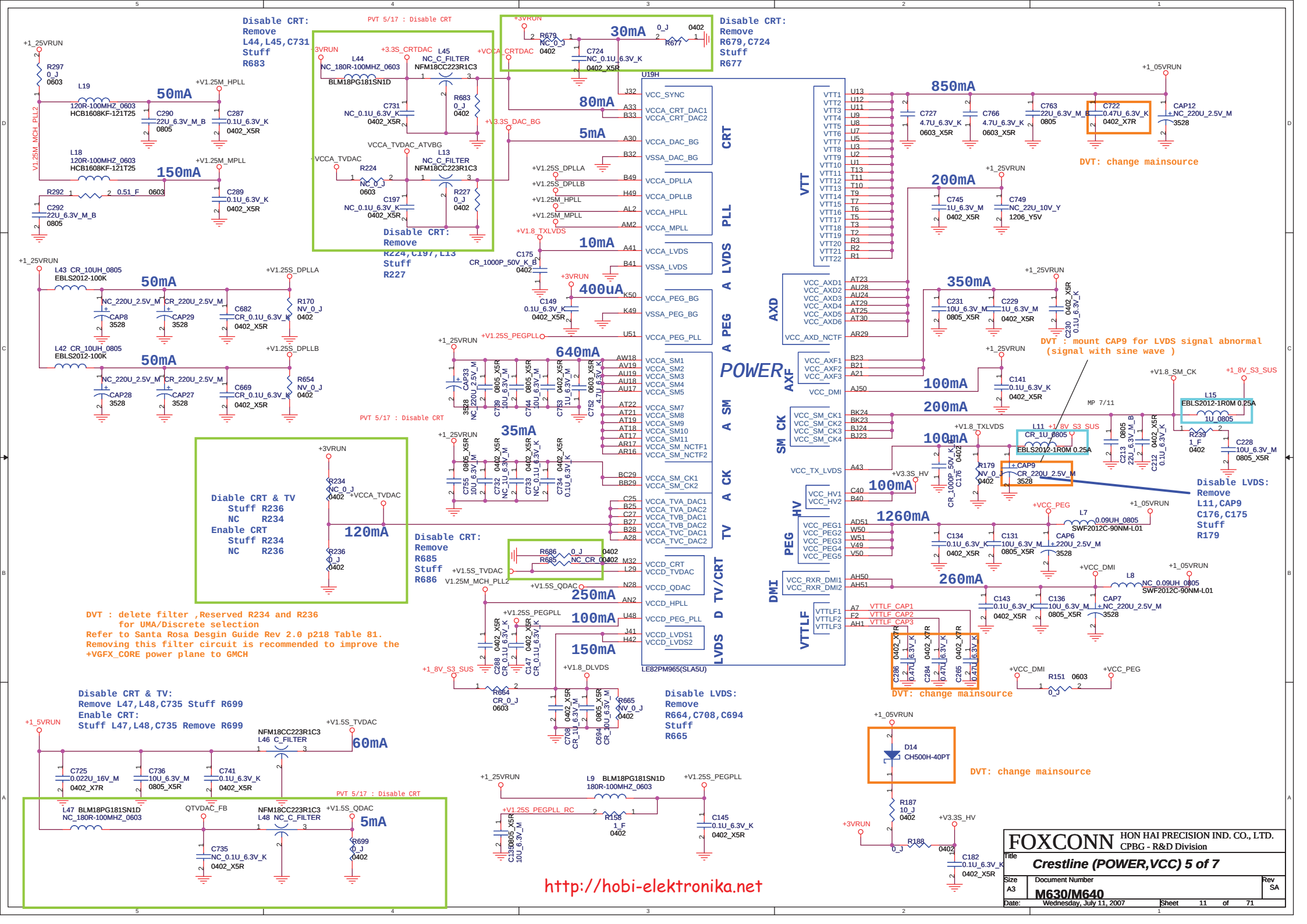
Disable CRT:
Remove
L44,L45,C731
Stuff
R683
PVT 5/17 : Disable CRT
Disable CRT:
Remove
R679,C724
Stuff
R677
Disable CRT:
Remove
R224,C197,L13
Stuff
R227
Disable CRT & TV
Stuff R236
NC R234
Enable CRT
Stuff R234
NC R236
Disable CRT:
Remove
R685
Stuff
R686
DVT : delete filter ,Reserved R234 and R236
for UMA/Discrete selection
Refer to Santa Rosa Desgin Guide Rev 2.0 p218 Table 81.
Removing this filter circuit is recommended to improve the
+VGFX_CORE power plane to GMCH
Disable CRT & TV:
Remove L47,L48,C735 Stuff R699
Enable CRT:
Stuff L47,L48,C735 Remove R699
PVT 5/17 : Disable CRT
Disable LVDS:
Remove
R664,C708,C694
Stuff
R665
DVT : change mainsource
DVT : mount CAP9 for LVDS signal abnormal
(signal with sine wave)
Disable LVDS:
Remove
L11,CAP9
C176,C175
Stuff
R179
DVT: change mainsource
DVT: change mainsource
POWER
U19H
LE82PM965(SLA5U)
CRT
PLL
LVDS
PEG
SM CK
TV
HV
DMI
VTTLF
AXD
AXF
VTT
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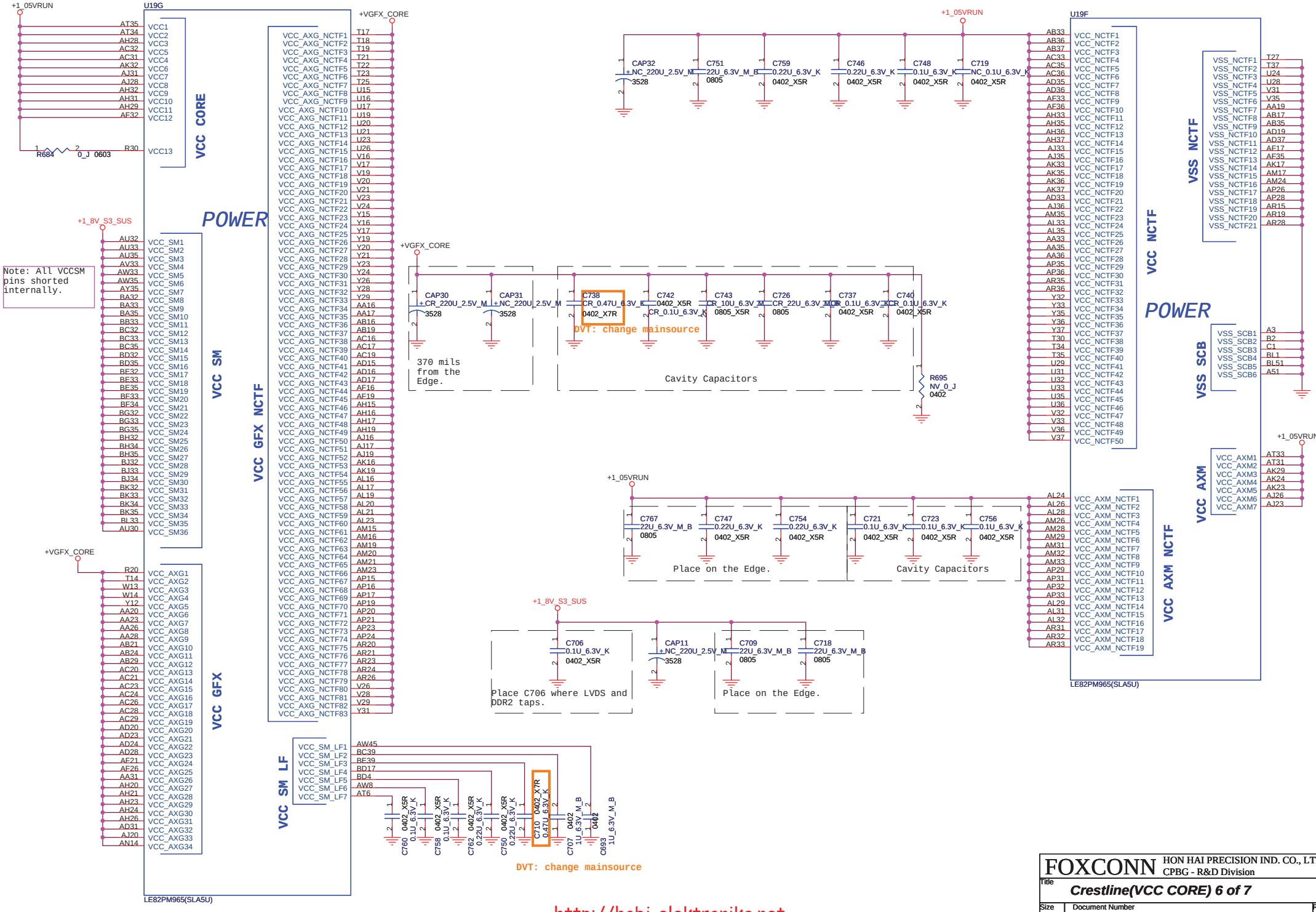
U19G
U19F
POWER
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
VCC NCTF
VSS NCTF
VSS SCB
VCC AXM
VCC AXM NCTF
+1_05VRUN
+1_8V_S3_SUS
+VGFX_CORE
Note: All VCCSM pins shorted internally.
370 mils from the Edge.
Cavity Capacitors
DVT: change mainsource
Place on the Edge.
Place C706 where LVDS and DDR2 taps.
LE82PM965(SLA5U)
http://hobi-elektronika.net
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Crestline(VCC CORE) 6 of 7
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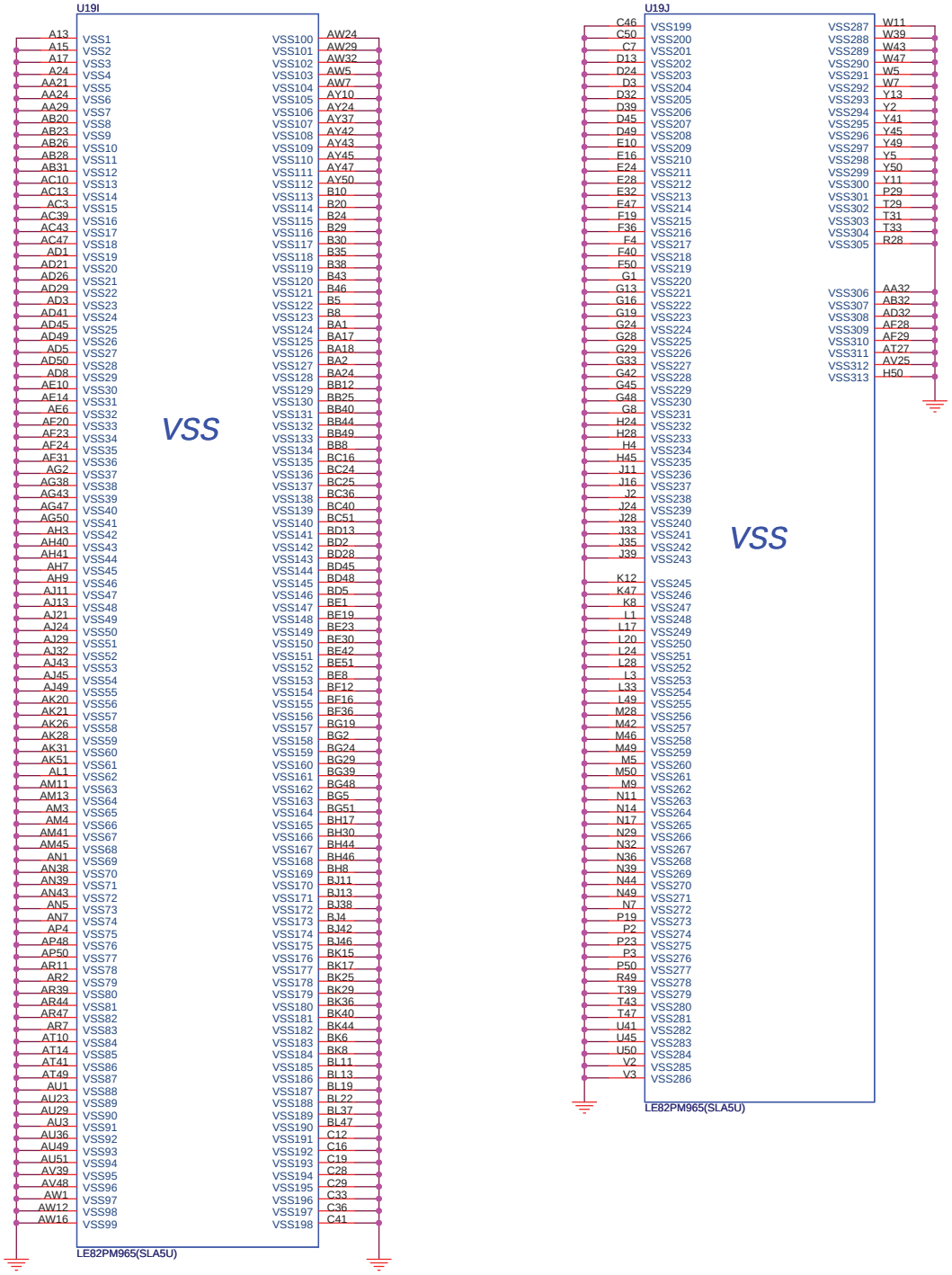

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Title: *Crestline (VSS) 7 of 7*

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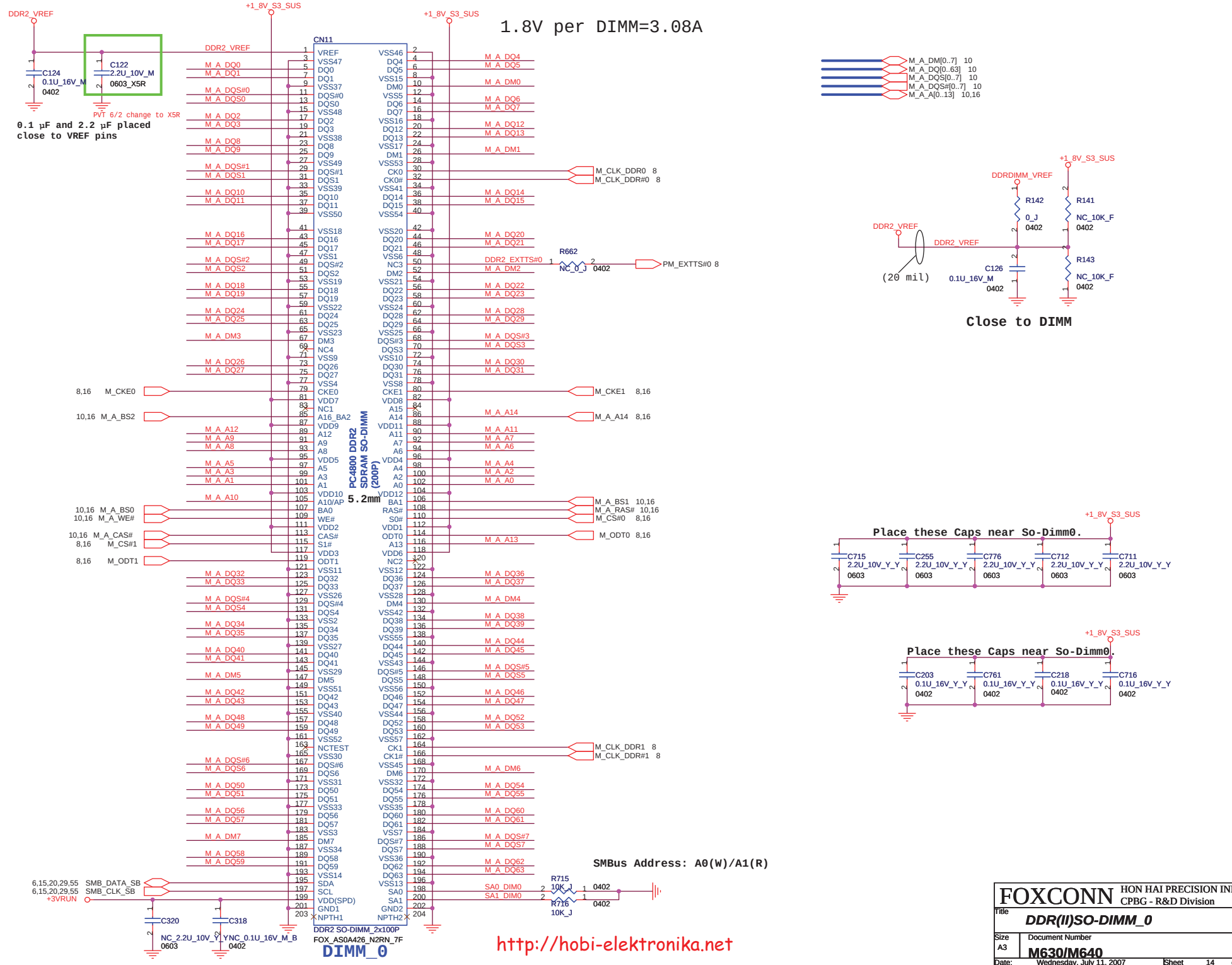
1.8V per DIMM=3.08A
CN11
DDR2_VREF
+1_8V_S3_SUS
C124 0.1U_16V_M 0402
C122 2.2U_10V_M 0603_X5R
PVT 6/2 change to X5R
0.1 µF and 2.2 µF placed close to VREF pins
M_A_DM[0..7] 10
M_A_DQ[0..63] 10
M_A_DQS[0..7] 10
M_A_DQS#[0..7] 10
M_A_A[0..13] 10,16
M_CLK_DDR0 8
M_CLK_DDR#0 8
M_CLK_DDR1 8
M_CLK_DDR#1 8
M_CKE0 8,16
M_CKE1 8,16
M_A_BS2 10,16
M_A_A14 8,16
M_A_BS0 10,16
M_A_WE# 10,16
M_A_CAS# 10,16
M_CS#0 8,16
M_CS#1 8,16
M_ODT0 8,16
M_ODT1 8,16
M_A_BS1 10,16
M_A_RAS# 10,16
DDR2_EXTTS#0
R662 NC_0_J 0402
PM_EXTTS#0 8
PC4800 DDR2 SDRAM SO-DIMM (200P)
5.2mm
DDR2 SO-DIMM_2x100P
FOX_AS0A426_N2RN_7F
DIMM_0
SMBus Address: A0(W)/A1(R)
SMB_DATA_SB 6,15,20,29,55
SMB_CLK_SB 6,15,20,29,55
+3VRUN
R715 10K_J 0402
R716 10K_J 0402
SA0_DIM0
SA1_DIM0
C320 NC_2.2U_10V_M 0603
C318 0.1U_16V_M_B 0402
DDRDIMM_VREF
R142 0_J 0402
R141 NC_10K_F 0402
R143 NC_10K_F 0402
C126 0.1U_16V_M 0402
(20 mil)
Close to DIMM
Place these Caps near So-Dimm0.
C715 2.2U_10V_Y_Y 0603
C255 2.2U_10V_Y_Y 0603
C776 2.2U_10V_Y_Y 0603
C712 2.2U_10V_Y_Y 0603
C711 2.2U_10V_Y_Y 0603
Place these Caps near So-Dimm0.
C203 0.1U_16V_Y_Y 0402
C761 0.1U_16V_Y_Y 0402
C218 0.1U_16V_Y_Y 0402
C716 0.1U_16V_Y_Y 0402
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Title
DDR(II)SO-DIMM_0
Size A3
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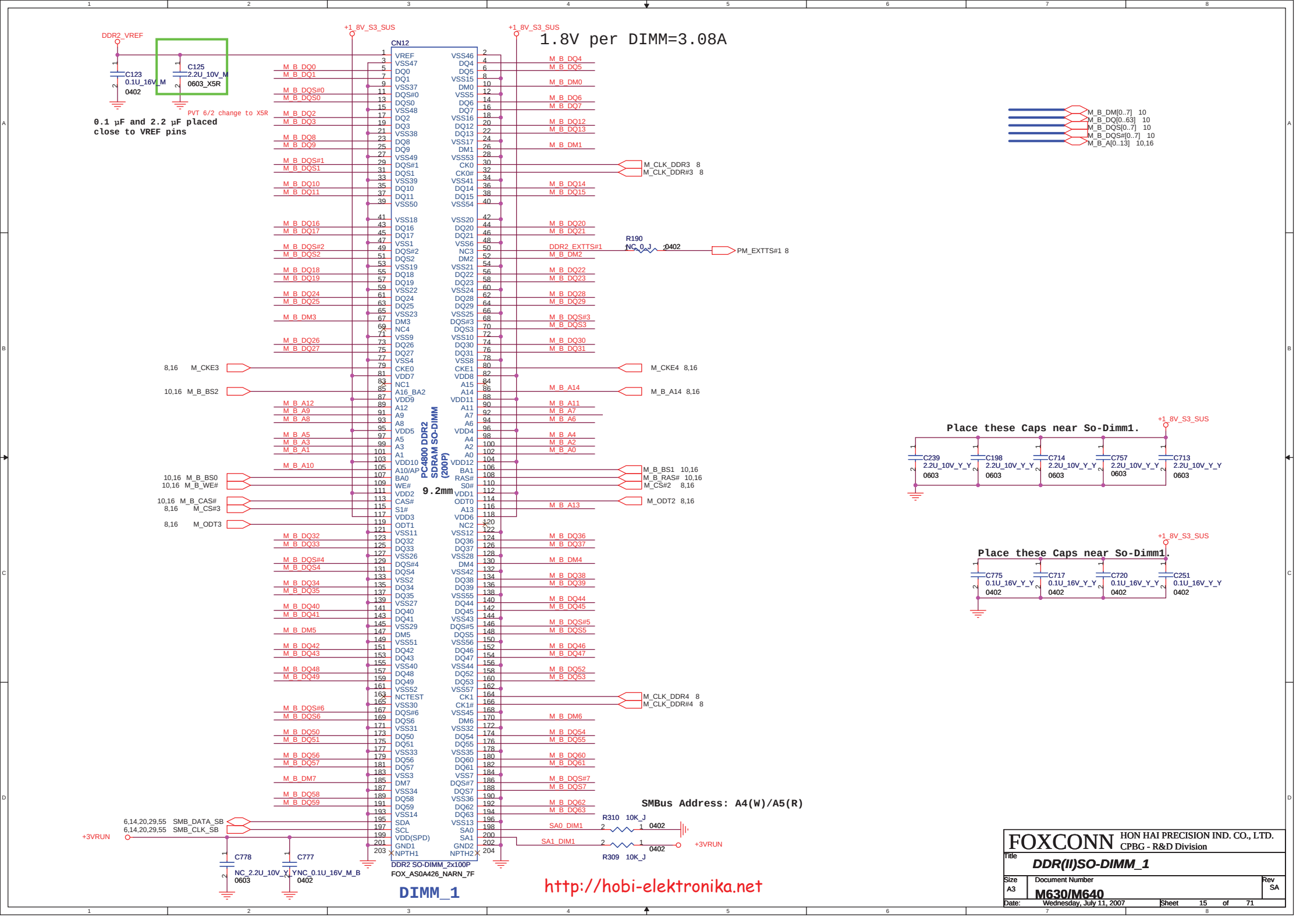
1.8V per DIMM=3.08A
DDR2_VREF
+1_8V_S3_SUS
C123 0.1U_16V_M 0402
C125 2.2U_10V_M 0603_X5R
PVT 6/2 change to X5R
0.1 µF and 2.2 µF placed close to VREF pins
CN12
DDR2 SO-DIMM_2x100P
FOX_AS0A426_NARN_7F
PC4800 DDR2 SDRAM SO-DIMM (200P)
9.2mm
DIMM_1
R190 NC_0_J 0402
PM_EXTTS#1 8
M_B_DM[0..7] 10
M_B_DQ[0..63] 10
M_B_DQS[0..7] 10
M_B_DQS#[0..7] 10
M_B_A[0..13] 10,16
M_CLK_DDR3 8
M_CLK_DDR#3 8
M_CLK_DDR4 8
M_CLK_DDR#4 8
M_CKE3 8,16
M_CKE4 8,16
M_B_BS2 10,16
M_B_BS1 10,16
M_B_BS0 10,16
M_B_WE# 10,16
M_B_RAS# 10,16
M_CS#2 8,16
M_B_CAS# 10,16
M_CS#3 8,16
M_ODT2 8,16
M_ODT3 8,16
Place these Caps near So-Dimm1.
C239 2.2U_10V_Y_Y 0603
C198 2.2U_10V_Y_Y 0603
C714 2.2U_10V_Y_Y 0603
C757 2.2U_10V_Y_Y 0603
C713 2.2U_10V_Y_Y 0603
Place these Caps near So-Dimm1.
C775 0.1U_16V_Y_Y 0402
C717 0.1U_16V_Y_Y 0402
C720 0.1U_16V_Y_Y 0402
C251 0.1U_16V_Y_Y 0402
SMBus Address: A4(W)/A5(R)
6,14,20,29,55 SMB_DATA_SB
6,14,20,29,55 SMB_CLK_SB
+3VRUN
R310 10K_J 0402
R309 10K_J 0402
SA0_DIM1
SA1_DIM1
C778 NC_2.2U_10V_Y 0603
C777 0.1U_16V_M_B 0402
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Title
DDR(II)SO-DIMM_1
Size A3
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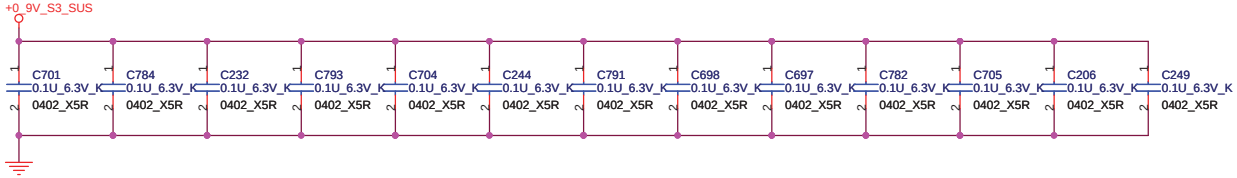
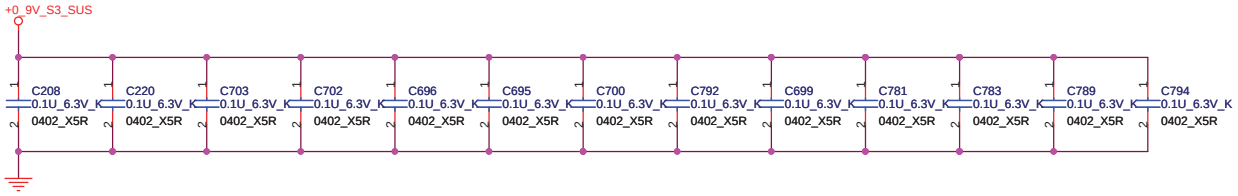
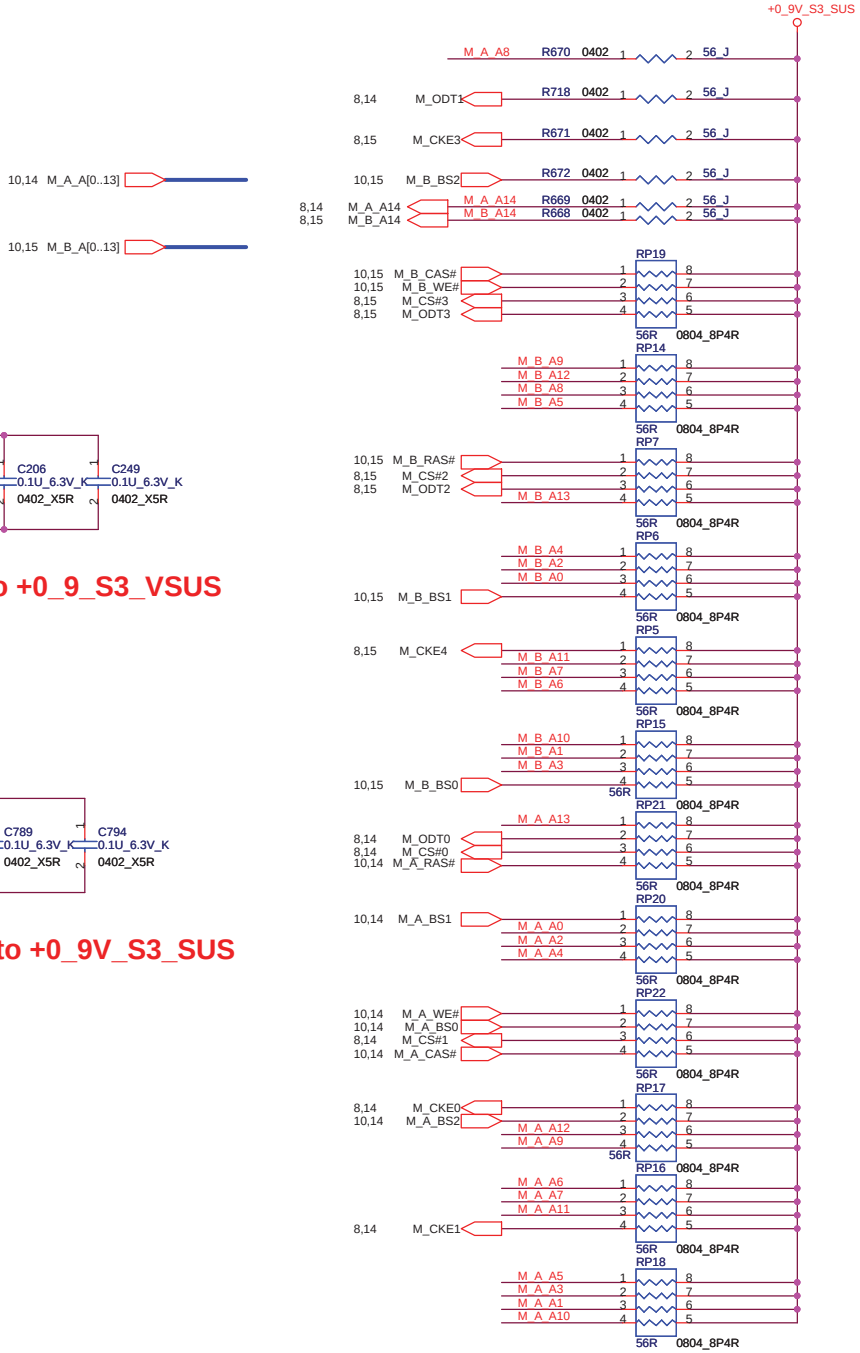


Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9_S3_VSUS



Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9V_S3_SUS



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Title: ***DDR(II)Termination***

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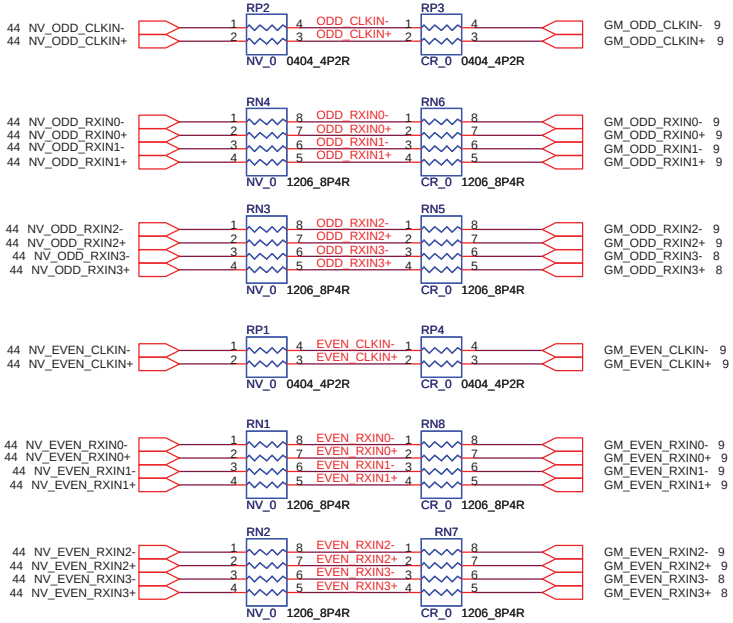
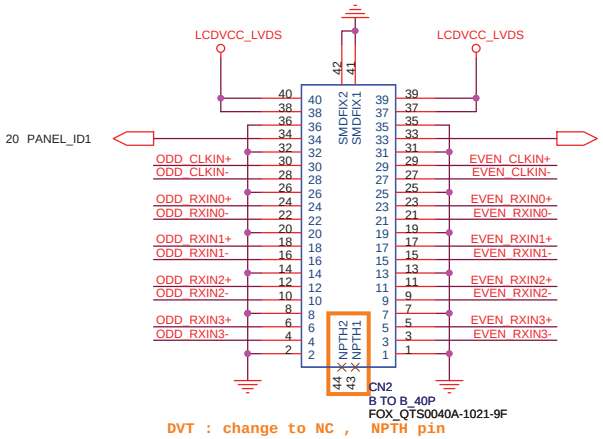
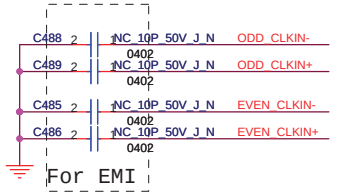
LVDS





DVT : change to NC , NPTH pin

LVDS CONNECTOR

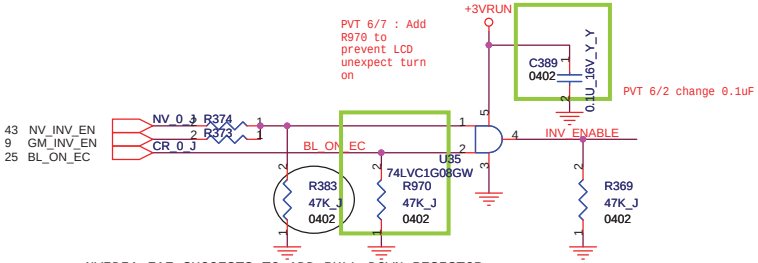


M630, 19"

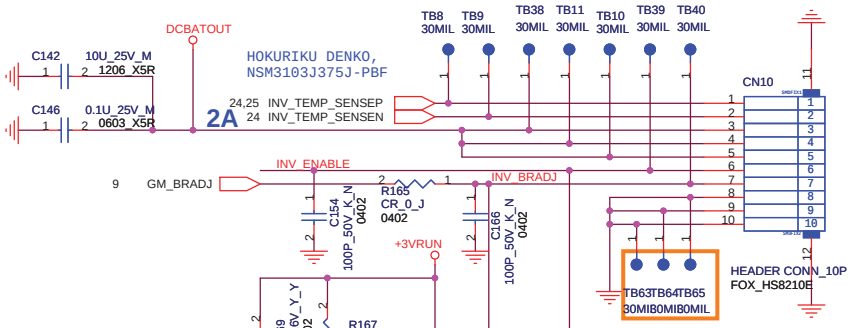
	Type 1	Type 2	Type 3	Type 4
00	AUO M190PW01 V.1			V
01			V	
10		V		
11				

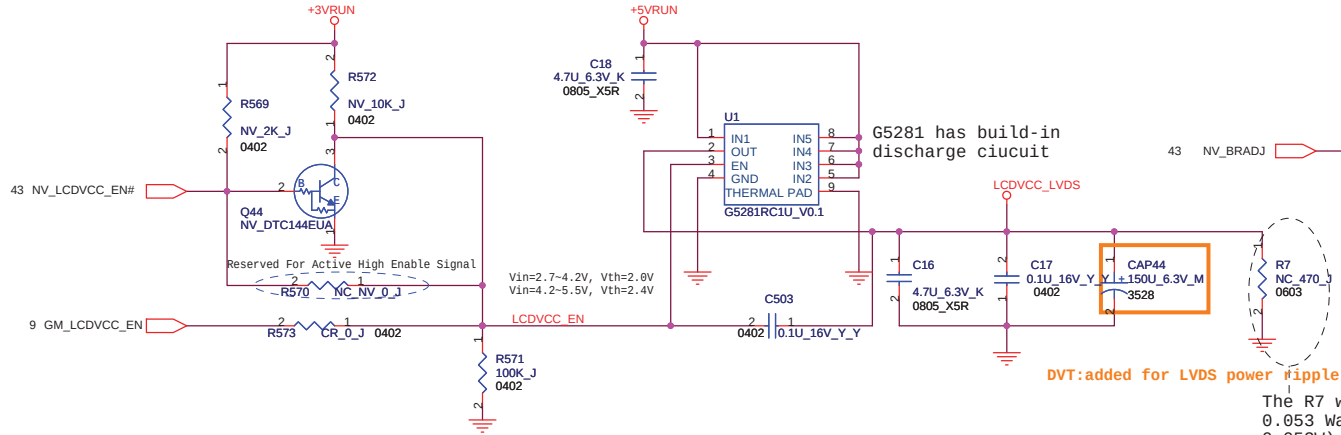
M640, 22"

	Type 1	Type 2	Type 3	Type 4
00	AUO M220EW01 V.2			V
01			V	
10		V		
11				



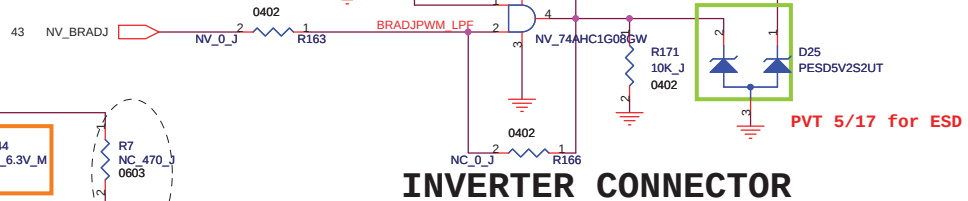
NVIDIA FAE SUGGESTS TO ADD PULL DOWN RESISTOR





DVT:added for LVDS power ripple (too large,spec is 200mv)

The R7 will consume about 0.053 Watt (5x5/470 = 0.053W). We changed resistor to 0603 size (1/10 Watt)



PVT 5/17 for ESD

INVERTER CONNECTOR

LCD POWER

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Title	LVDS	
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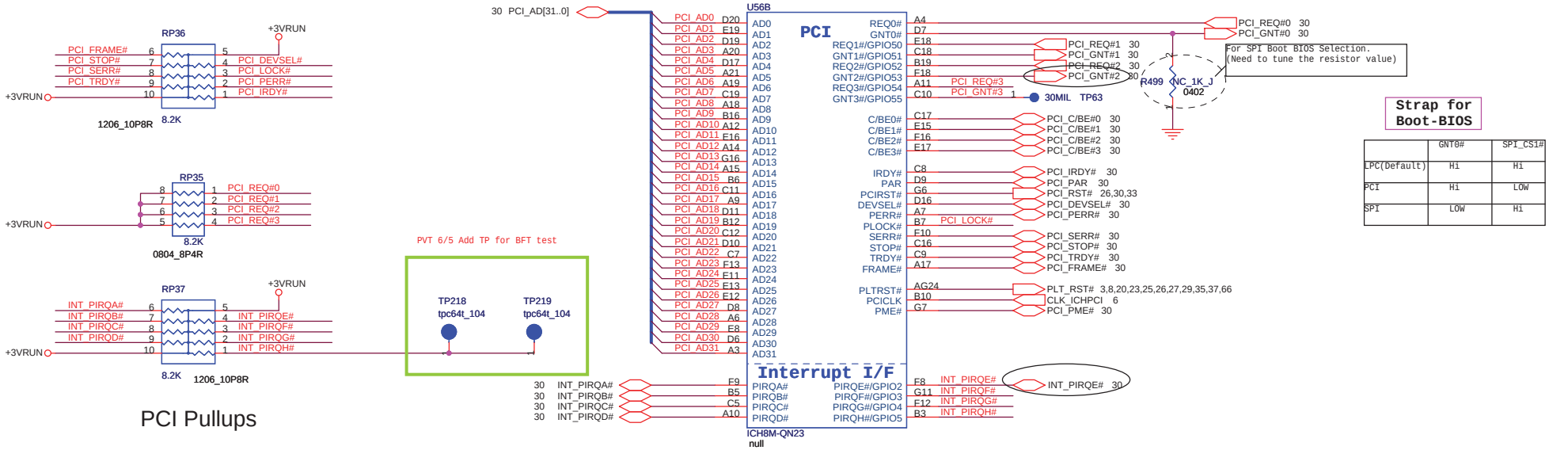

USB PORT	Function
PORT-0	REAR-1
PORT-1	REAR-2
PORT-2	REAR-3
PORT-3	SIDE-1
PORT-4	SIDE-2
PORT-5	EXPRESS CARD
PORT-6	CAMERA
PORT-7	CIR
PORT-8	RF KBD
PORT-9	NC

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Title: ICH8-M(PCI/DMI/USB/PCIE) 1/5

Size: A3 | Document Number: M630/M640 | Rev: SA

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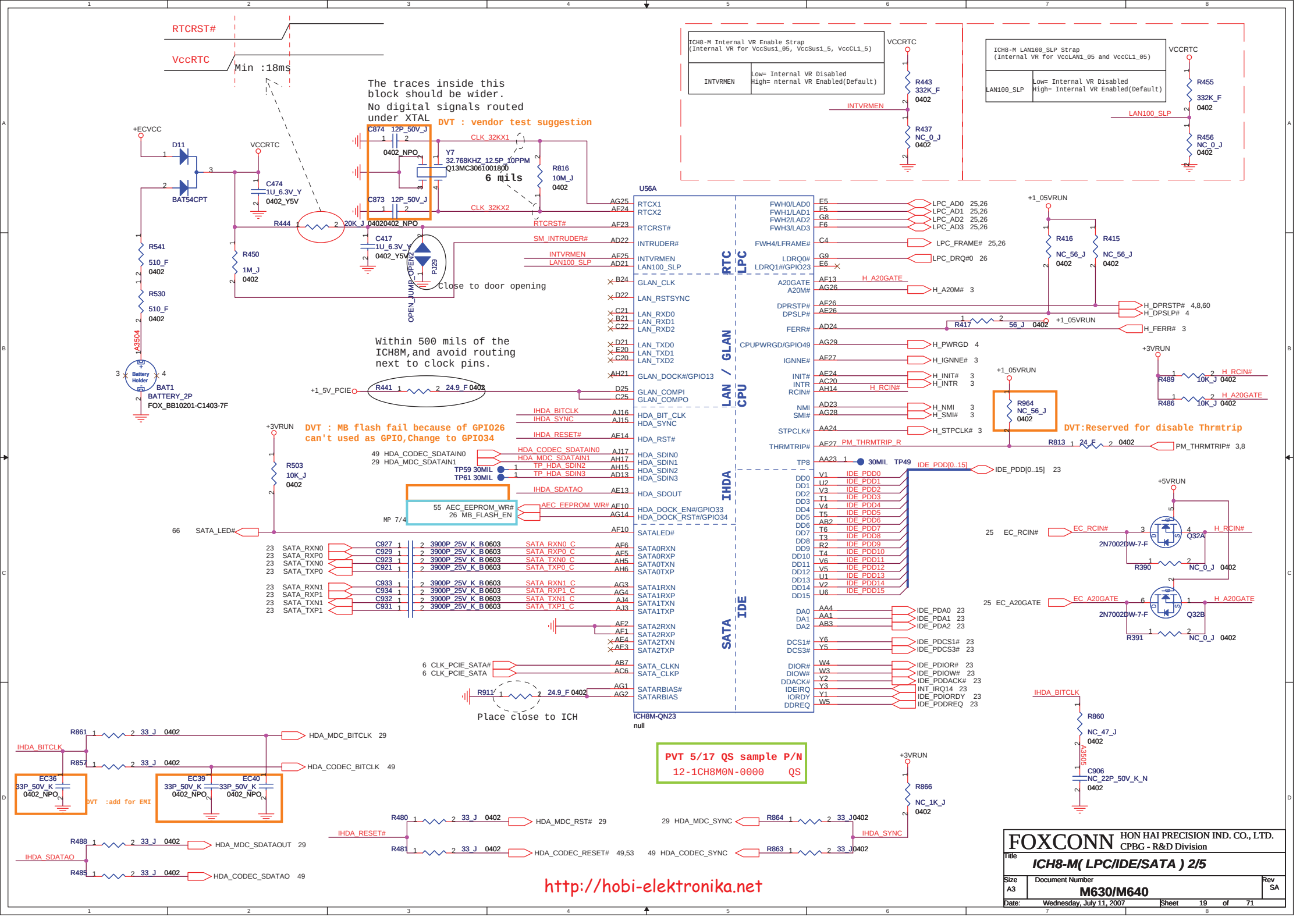
RTCRST#
VccRTC
Min :18ms
The traces inside this block should be wider.
No digital signals routed under XTAL
DVT : vendor test suggestion
6 mils
Close to door opening
Within 500 mils of the ICH8M,and avoid routing next to clock pins.
DVT : MB flash fail because of GPIO26 can't used as GPIO,Change to GPIO34
DVT :Reserved for disable Thrmtrip
Place close to ICH
ICH8-M Internal VR Enable Strap (Internal VR for VccSus1_05, VccSus1_5, VccCL1_5)
INTVRMEN
Low= Internal VR Disabled
High= nternal VR Enabled(Default)
ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1_05)
LAN100_SLP
Low= Internal VR Disabled
High= Internal VR Enabled(Default)
U56A
RTC
LPC
LAN / GLAN
CPU
IHDA
SATA
IDE
ICH8M-QN23
null
PVT 5/17 QS sample P/N
12-1CH8M0N-0000 QS
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Title
ICH8-M(LPC/IDE/SATA) 2/5
Size A3
Document Number
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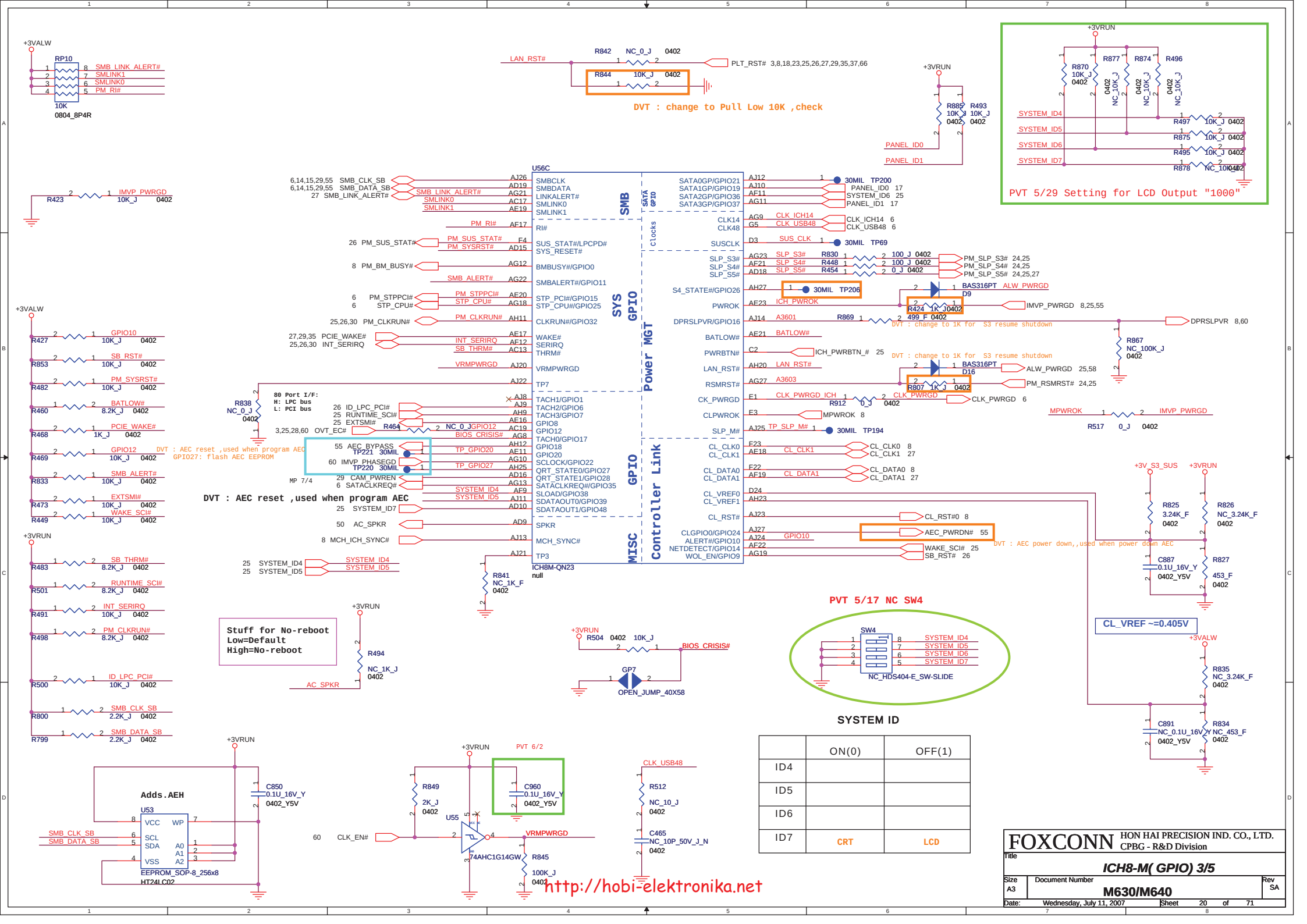
RP10
SMB_LINK_ALERT#
SMLINK1
SMLINK0
PM_RI#
10K
0804_8P4R
R423 IMVP_PWRGD 10K_J 0402
LAN_RST#
R842 NC_0_J 0402
R844 10K_J 0402
PLT_RST# 3,8,18,23,25,26,27,29,35,37,66
DVT : change to Pull Low 10K ,check
+3VRUN
R885 10K_J 0402
R493 10K_J 0402
PANEL_ID0
PANEL_ID1
R870 10K_J 0402
R877
R874
R496
SYSTEM_ID4
SYSTEM_ID5
SYSTEM_ID6
SYSTEM_ID7
R497 10K_J 0402
R875 10K_J 0402
R495 10K_J 0402
R878 NC_10K_J 0402
PVT 5/29 Setting for LCD Output "1000"
U56C
ICH8M-QN23
null
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
Controller Link
MISC
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SUS_STAT#/LPCPD#
SYS_RESET#
BMBUSY#/GPIO0
SMBALERT#/GPIO11
STP_PCI#/GPIO15
STP_CPU#/GPIO25
CLKRUN#/GPIO32
WAKE#
SERIRQ
THRM#
VRMPWRGD
TP7
TACH1/GPIO1
TACH2/GPIO6
TACH3/GPIO7
GPIO8
GPIO12
TACH0/GPIO17
GPIO18
GPIO20
SCLOCK/GPIO22
QRT_STATE0/GPIO27
QRT_STATE1/GPIO28
SATACLKREQ#/GPIO35
SLOAD/GPIO38
SDATAOUT0/GPIO39
SDATAOUT1/GPIO48
SPKR
MCH_SYNC#
TP3
SATA0GP/GPIO21
SATA1GP/GPIO19
SATA2GP/GPIO36
SATA3GP/GPIO37
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
S4_STATE#/GPIO26
PWROK
DPRSLPVR/GPIO16
BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
CK_PWRGD
CLPWROK
SLP_M#
CL_CLK0
CL_CLK1
CL_DATA0
CL_DATA1
CL_VREF0
CL_VREF1
CL_RST#
CLGPIO0/GPIO24
ALERT#/GPIO10
NETDETECT/GPIO14
WOL_EN/GPIO9
6,14,15,29,55 SMB_CLK_SB
6,14,15,29,55 SMB_DATA_SB
27 SMB_LINK_ALERT#
26 PM_SUS_STAT#
8 PM_BM_BUSY#
6 PM_STPPCI#
6 STP_CPU#
25,26,30 PM_CLKRUN#
27,29,35 PCIE_WAKE#
25,26,30 INT_SERIRQ
26 ID_LPC_PCI#
25 RUNTIME_SCI#
25 EXTSMI#
3,25,28,60 OVT_EC#
55 AEC_BYPASS
60 IMVP_PHASEGD
29 CAM_PWREN
6 SATACLKREQ#
25 SYSTEM_ID7
50 AC_SPKR
8 MCH_ICH_SYNC#
25 SYSTEM_ID4
25 SYSTEM_ID5
80 Port I/F:
H: LPC bus
L: PCI bus
R838 NC_0_J 0402
R464 NC_0_J
GPIO12
BIOS_CRISIS#
TP_GPIO20
TP_GPIO27
SYSTEM_ID4
SYSTEM_ID5
TP221 30MIL
TP220 30MIL
MP 7/4
DVT : AEC reset ,used when program AEC
GPIO27: flash AEC EEPROM
R841 NC_1K_F 0402
AJ12 AJ10 AF11 AG11
30MIL TP200
PANEL_ID0 17
SYSTEM_ID6 25
PANEL_ID1 17
AG9 G5
CLK_ICH14
CLK_USB48
CLK_ICH14 6
CLK_USB48 6
D3 SUS_CLK
30MIL TP69
AG23 AF21 AD18
SLP_S3# R830 100_J 0402
SLP_S4# R448 100_J 0402
SLP_S5# R454 0_J 0402
PM_SLP_S3# 24,25
PM_SLP_S4# 24,25
PM_SLP_S5# 24,25,27
AH27
30MIL TP206
BAS316PT ALW_PWRGD
D9
AE23 ICH_PWROK
R424 1K_J 0402
IMVP_PWRGD 8,25,55
AJ14 A3601
R869 499_F 0402
DVT : change to 1K for S3 resume shutdown
DPRSLPVR 8,60
R867 NC_100K_J 0402
AE21 BATLOW#
C2 ICH_PWRBTN_# 25
DVT : change to 1K for S3 resume shutdown
AH20 LAN_RST#
BAS316PT D16
ALW_PWRGD 25,58
AG27 A3603
R807 1K_J 0402
PM_RSMRST# 24,25
E1 CLK_PWRGD_ICH
R912 0_J 0402
CLK_PWRGD
CLK_PWRGD 6
E3 MPWROK 8
MPWROK
R517 0_J 0402
IMVP_PWRGD
AJ25 TP_SLP_M#
30MIL TP194
F23 AE18
CL_CLK0 8
CL_CLK1 27
F22 AF19
CL_DATA0 8
CL_DATA1 27
D24 AH23
AJ23
CL_RST#0 8
AJ27 AJ24 AF22 AG19
GPIO10
AEC_PWRDN# 55
WAKE_SCI# 25
SB_RST# 26
DVT : AEC power down,,used when power down AEC
+3V_S3_SUS
R825 3.24K_F 0402
R826 NC_3.24K_F 0402
C887 0.1U_16V_Y 0402_Y5V
R827 453_F 0402
CL_VREF ~=0.405V
R835 NC_3.24K_F 0402
C891 NC_0.1U_16V_Y 0402_Y5V
R834 NC_453_F 0402
+3VALW
R427 GPIO10 10K_J 0402
R853 SB_RST# 10K_J 0402
R482 PM_SYSRST# 10K_J 0402
R460 BATLOW# 8.2K_J 0402
R468 PCIE_WAKE# 1K_J 0402
R469 GPIO12 10K_J 0402
R833 SMB_ALERT# 10K_J 0402
R473 EXTSMI# 10K_J 0402
R449 WAKE_SCI# 10K_J 0402
+3VRUN
R483 SB_THRM# 8.2K_J 0402
R501 RUNTIME_SCI# 8.2K_J 0402
R491 INT_SERIRQ 10K_J 0402
R498 PM_CLKRUN# 8.2K_J 0402
R500 ID_LPC_PCI# 10K_J 0402
R800 SMB_CLK_SB 2.2K_J 0402
R799 SMB_DATA_SB 2.2K_J 0402
Stuff for No-reboot
Low=Default
High=No-reboot
R494 NC_1K_J 0402
AC_SPKR
R504 0402 10K_J
BIOS_CRISIS#
GP7
OPEN_JUMP_40X58
PVT 5/17 NC SW4
SW4
NC_HDS404-E_SW-SLIDE
SYSTEM ID
ID4
ID5
ID6
ID7
ON(0)
OFF(1)
CRT
LCD
Adds.AEH
U53
EEPROM_SOP-8_256x8
HT24LC02
C850 0.1U_16V_Y 0402_Y5V
SMB_CLK_SB
SMB_DATA_SB
PVT 6/2
R849 2K_J 0402
C960 0.1U_16V_Y 0402_Y5V
U55
74AHC1G14GW
60 CLK_EN#
VRMPWRGD
R845 100K_J 0402
CLK_USB48
R512 NC_10_J 0402
C465 NC_10P_50V_J_N 0402
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FOXCONN
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CPBG - R&D Division
Title
ICH8-M(GPIO) 3/5
Size A3
Document Number
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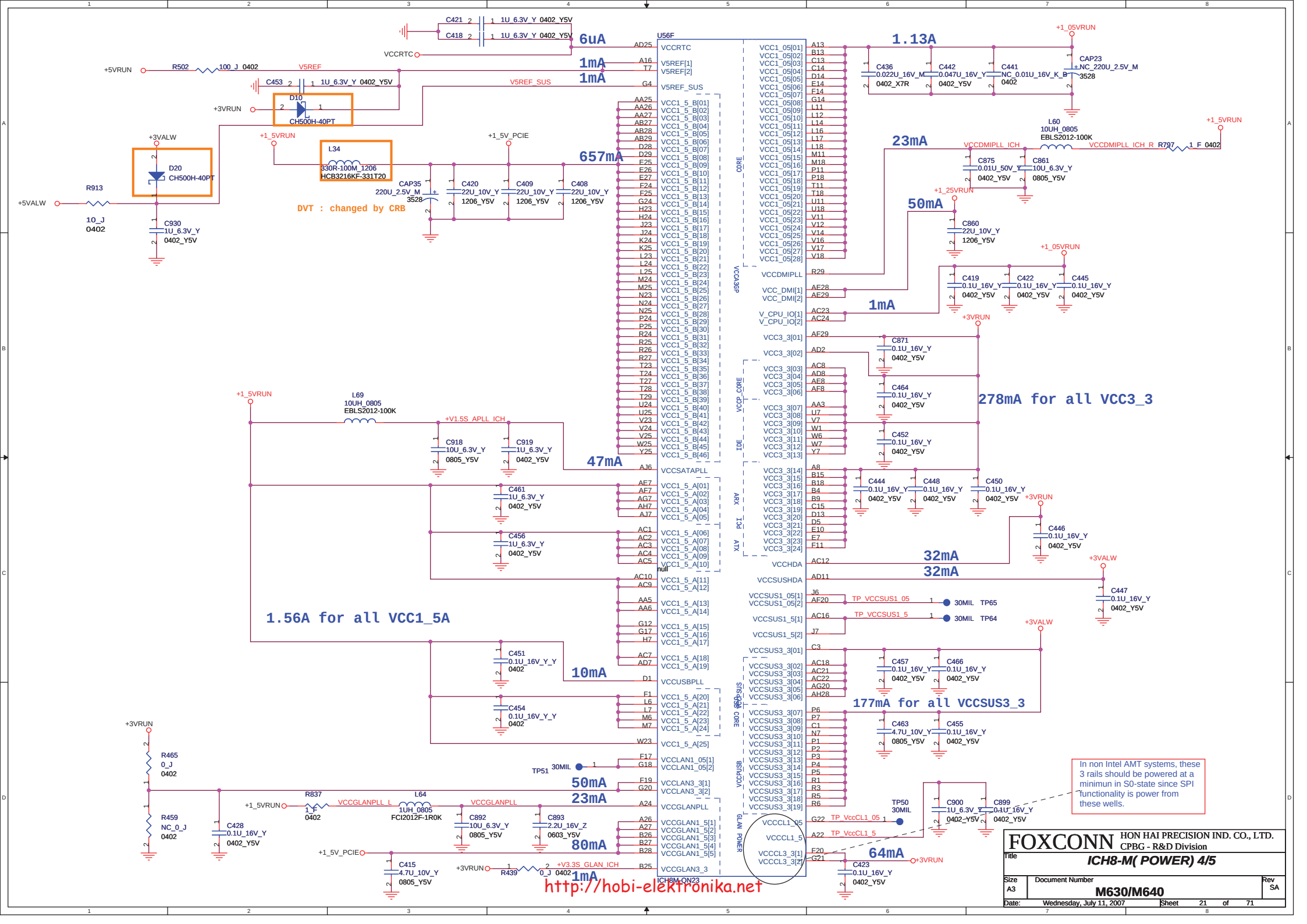
6uA
1mA
1mA
657mA
47mA
10mA
50mA
23mA
80mA
1mA
1.13A
23mA
50mA
1mA
278mA for all VCC3_3
32mA
32mA
1.56A for all VCC1_5A
177mA for all VCCSUS3_3
64mA
DVT : changed by CRB
In non Intel AMT systems, these 3 rails should be powered at a minimun in S0-state since SPI functionality is power from these wells.
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ICH8-M(POWER) 4/5
M630/M640
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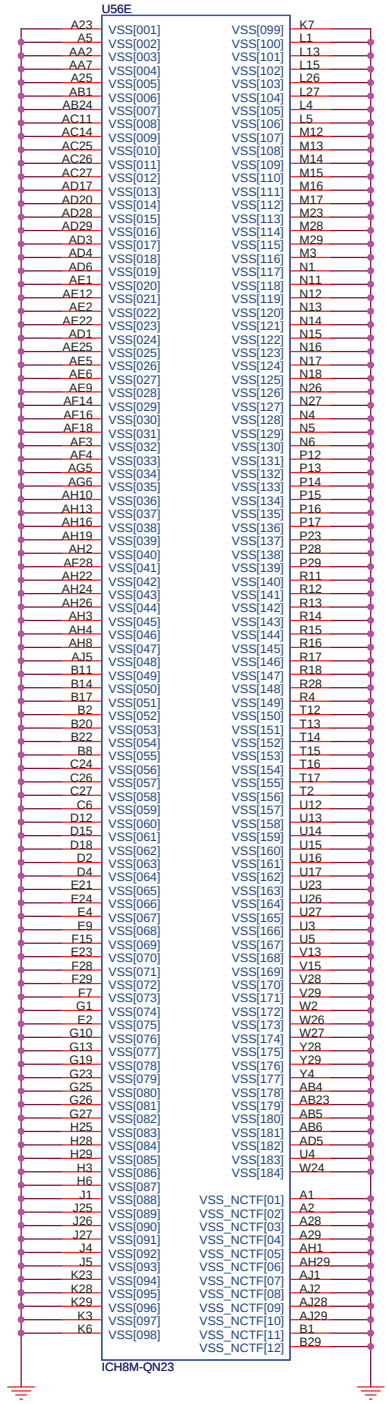

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Title: ICH8-M(GND) 5/5

Size: A3 | Document Number: M630/M640 | Rev: SA

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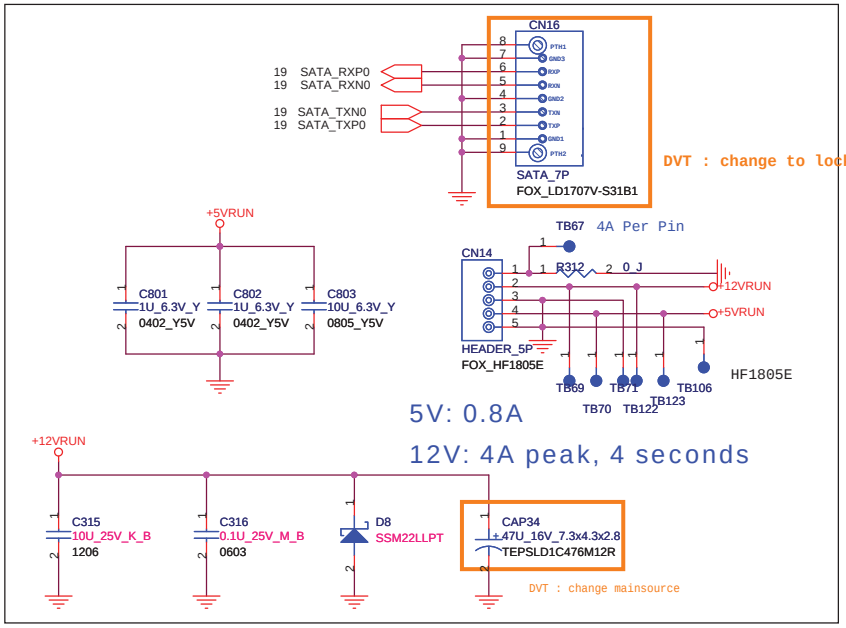
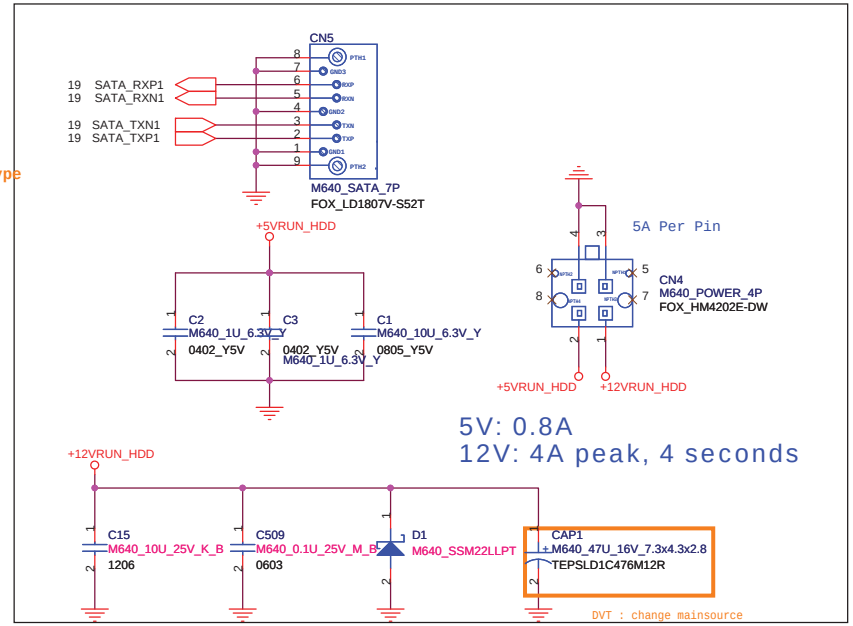
SATA HDD CONN

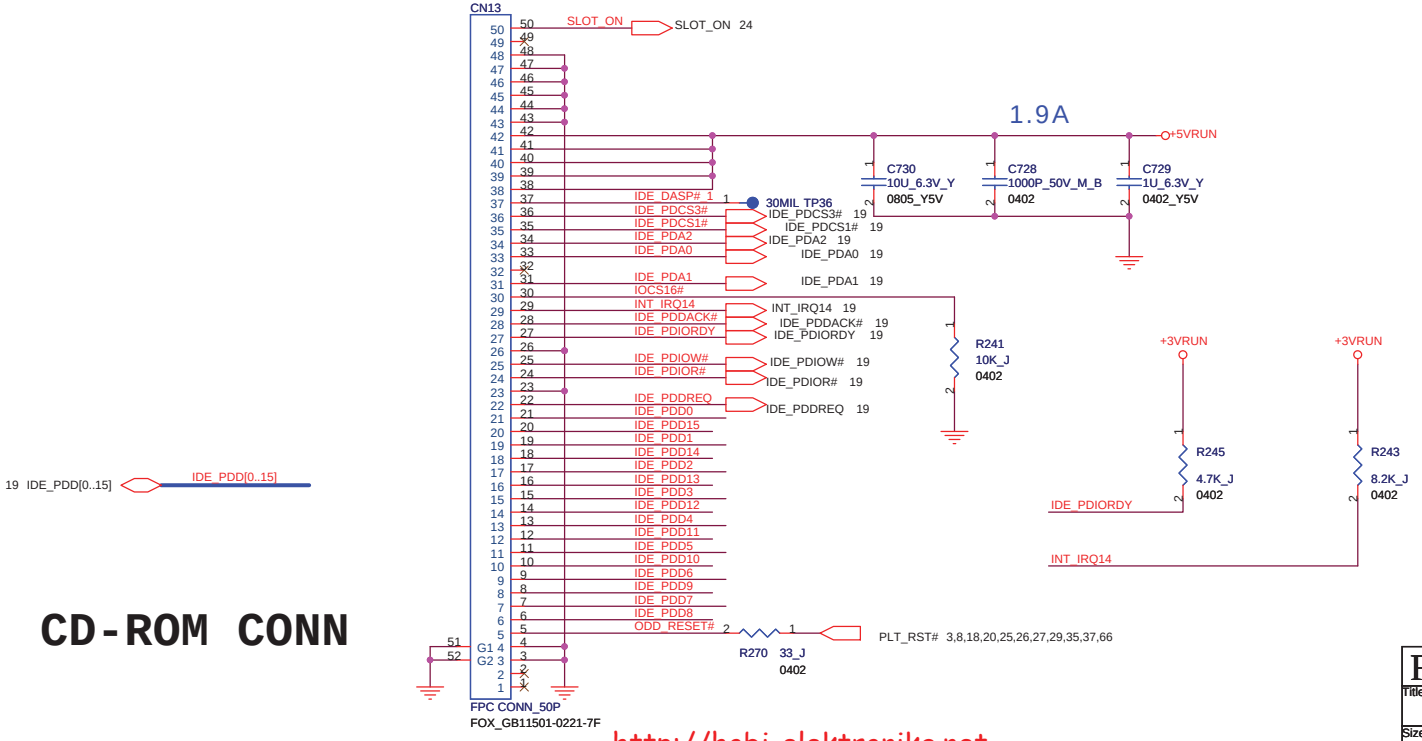


HDD1



HDD2

CD-ROM CONN

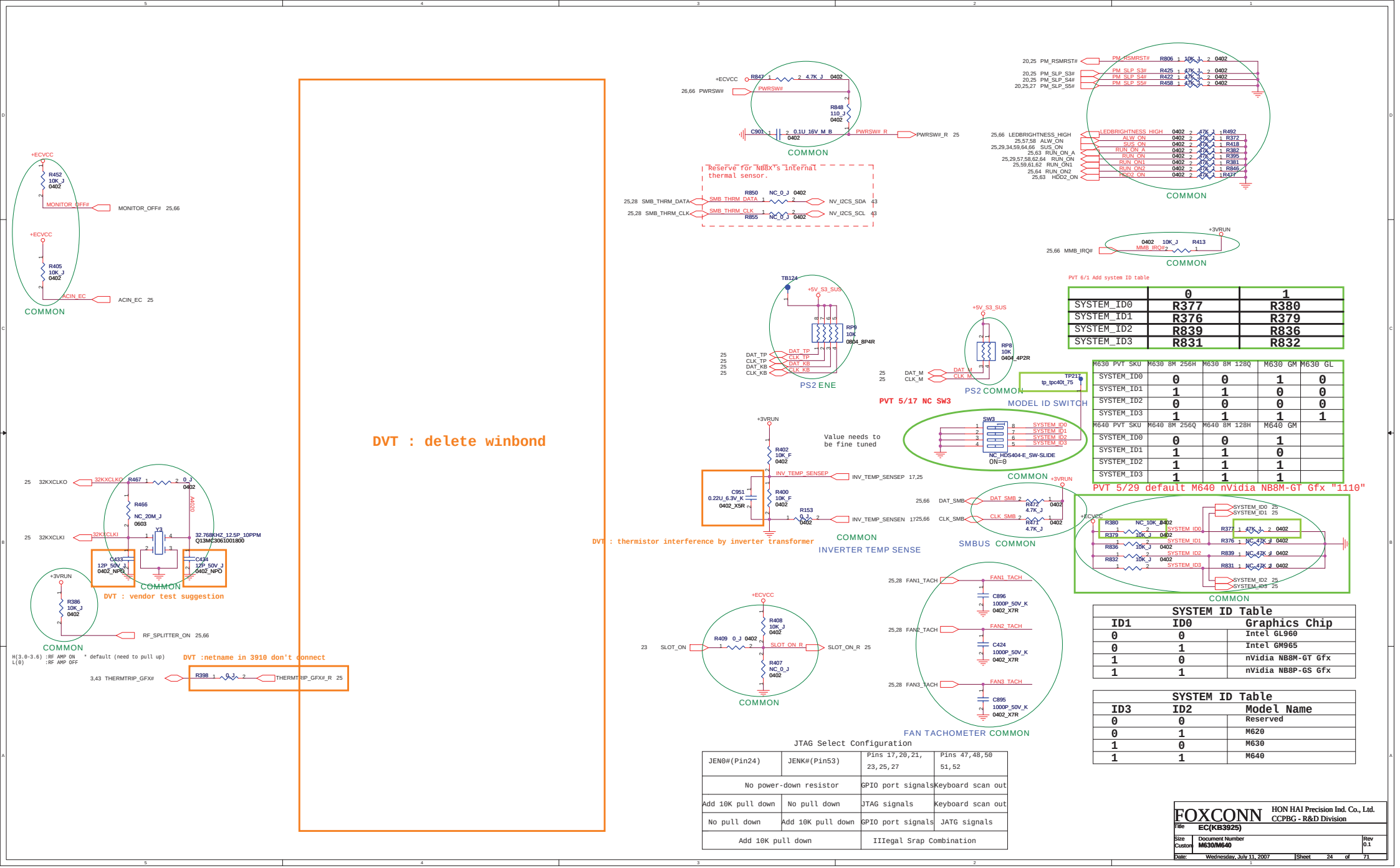


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: SATA HDD/CD-ROM

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 23 of 71



PVT 6/1 Add system ID table

	0	1
SYSTEM_ID0	R377	R380
SYSTEM_ID1	R376	R379
SYSTEM_ID2	R839	R836
SYSTEM_ID3	R831	R832

M630 PVT SKU	M630 8M 256H	M630 8M 128Q	M630 GM	M630 GL
SYSTEM_ID0	0	0	1	0
SYSTEM_ID1	1	1	0	0
SYSTEM_ID2	0	0	0	0
SYSTEM_ID3	1	1	1	1
M640 PVT SKU	M640 8M 256Q	M640 8M 128H	M640 GM	
SYSTEM_ID0	0	0	1	
SYSTEM_ID1	1	1	0	
SYSTEM_ID2	1	1	1	
SYSTEM_ID3	1	1	1	

PVT 5/29 default M640 nVidia NB8M-GT Gfx "1110"

SYSTEM ID Table		
ID1	ID0	Graphics Chip
0	0	Intel GL960
0	1	Intel GM965
1	0	nVidia NB8M-GT Gfx
1	1	nVidia NB8P-GS Gfx

SYSTEM ID Table		
ID3	ID2	Model Name
0	0	Reserved
0	1	M620
1	0	M630
1	1	M640

JTAG Select Configuration

JEN0#(Pin24)	JENK#(Pin53)	Pins 17,20,21, 23,25,27	Pins 47,48,50 51,52
No power-down resistor		GPIO port signals	Keyboard scan out
Add 10K pull down	No pull down	JTAG signals	Keyboard scan out
No pull down	Add 10K pull down	GPIO port signals	JATG signals
Add 10K pull down		IIIegal Srap Combination	

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Title	EC(KB3925)	
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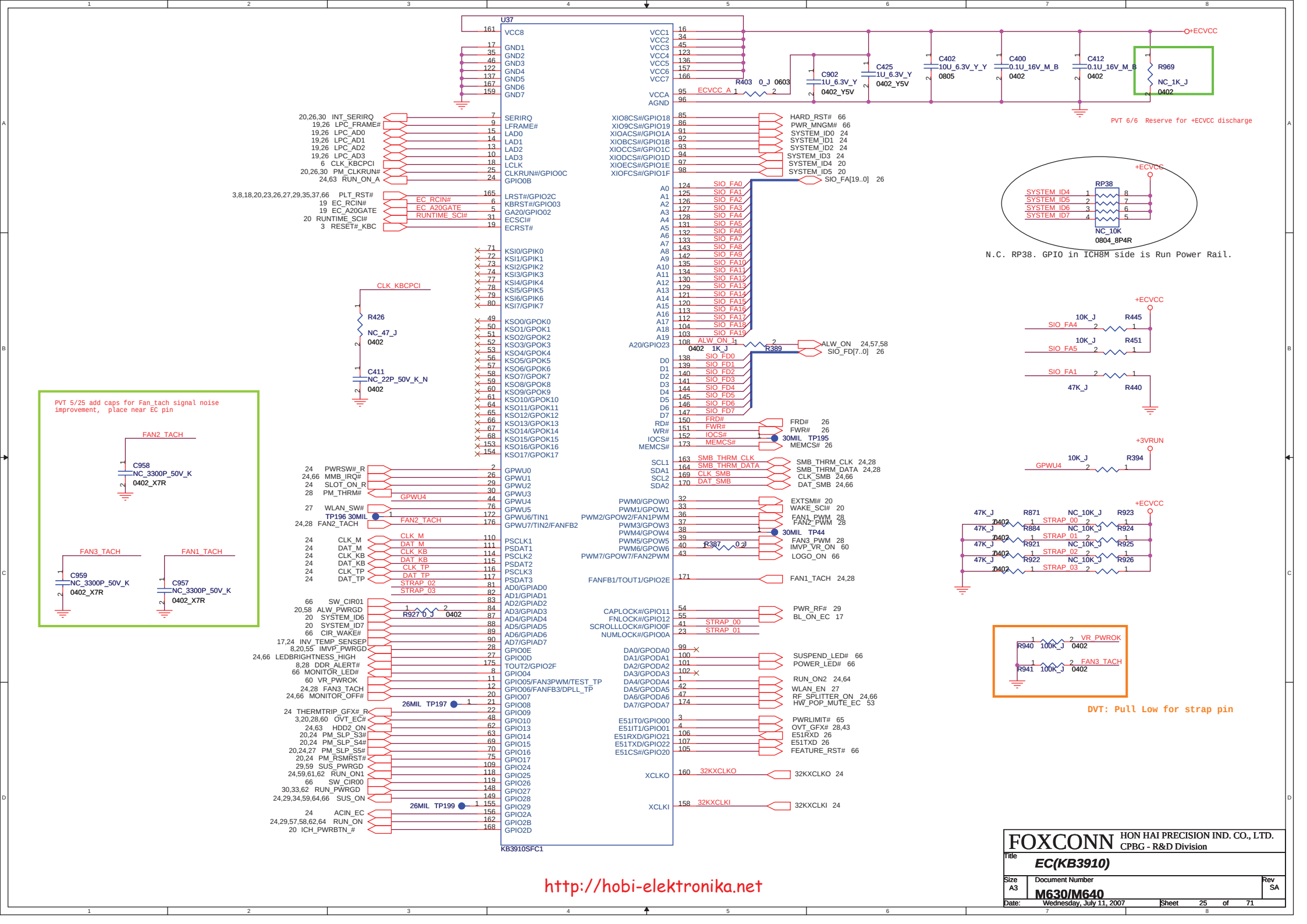
U37
KB3910SFC1
+ECVCC
PVT 6/6 Reserve for +ECVCC discharge
N.C. RP38. GPIO in ICH8M side is Run Power Rail.
PVT 5/25 add caps for Fan_tach signal noise improvement, place near EC pin
DVT: Pull Low for strap pin
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HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
EC(KB3910)
M630/M640
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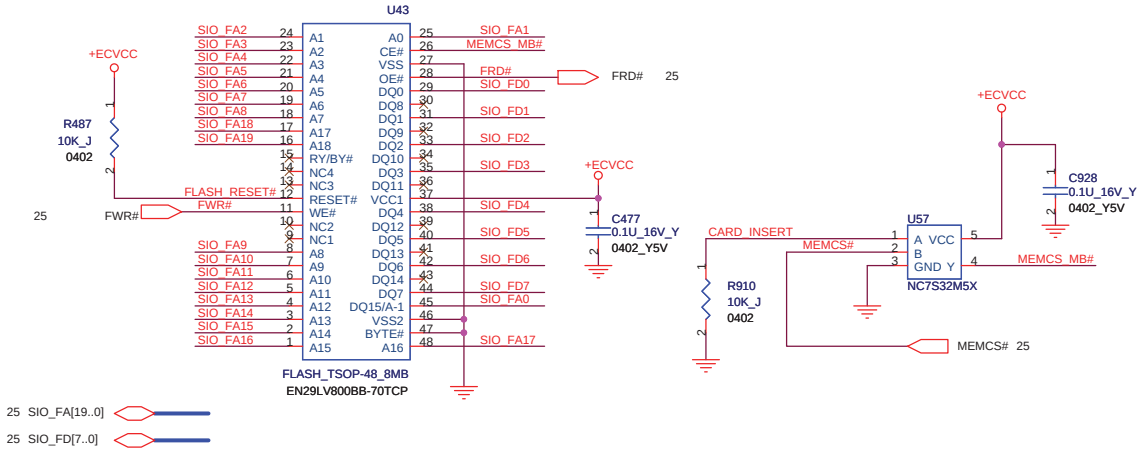
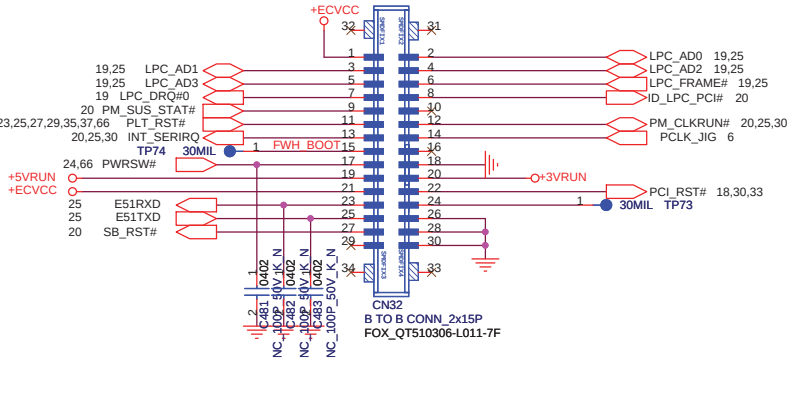


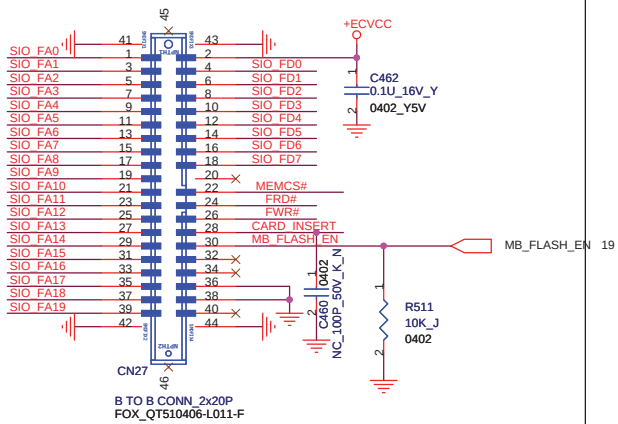
XBUS BIOS ROM

DVT : delete winbond

WINBOND



JIG-120 DEBUG PORT



EXTERNAL XBUS ROM INTERFACE

DVT : delete winbond

JTAG INTERFACE

WINBOND

EXTERNAL SPI ROM INTERFACE

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Title: *Flash ROM/X-Bus CONN*

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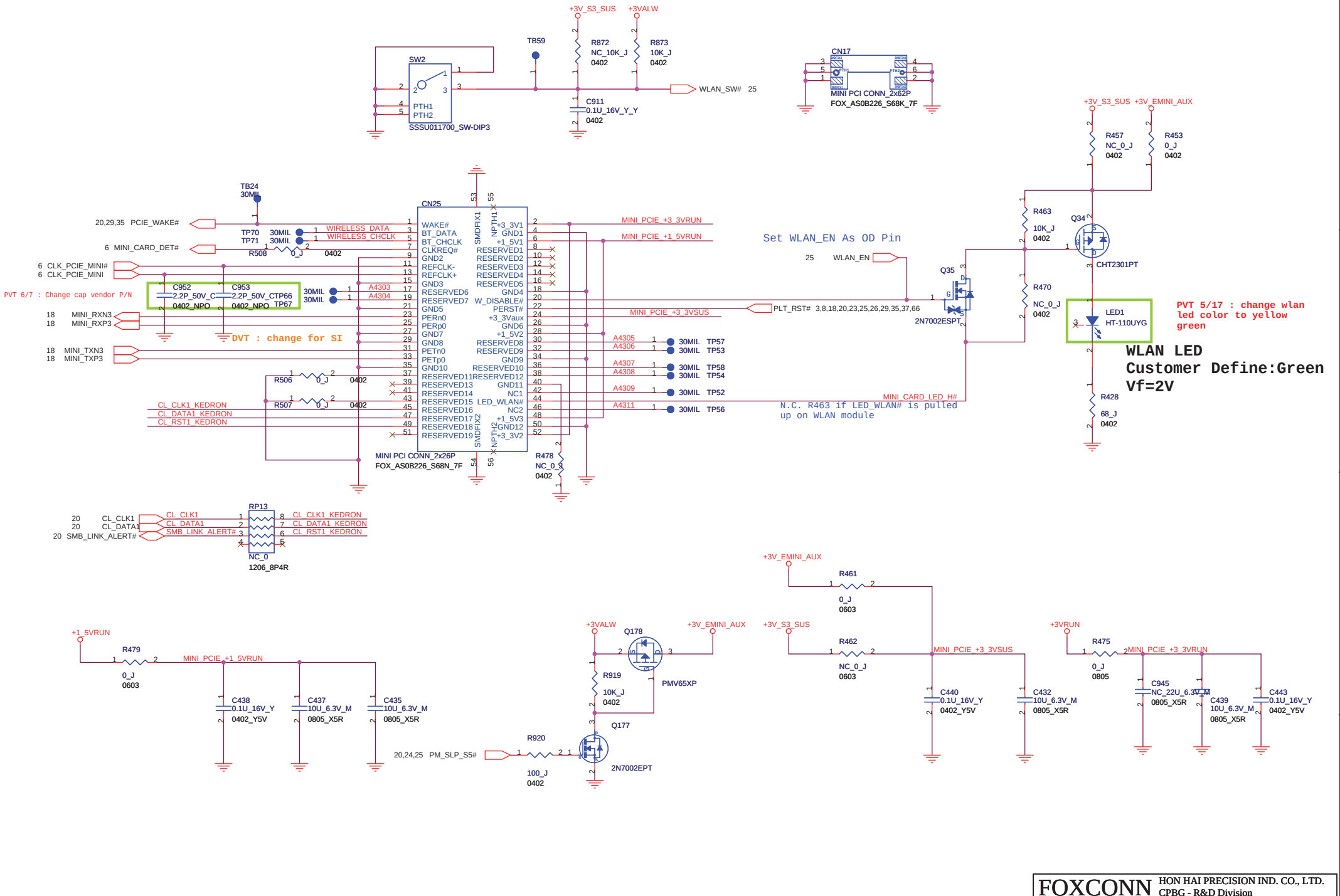

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Title: *Mini_Card*

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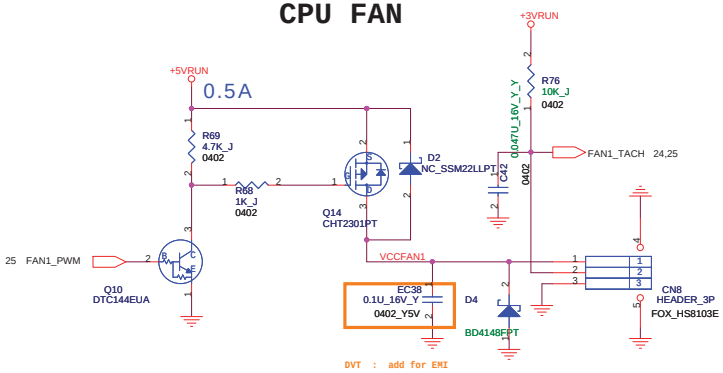
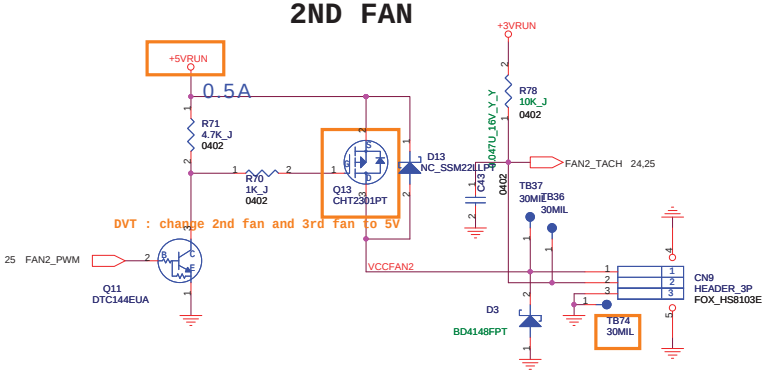
CPU FAN

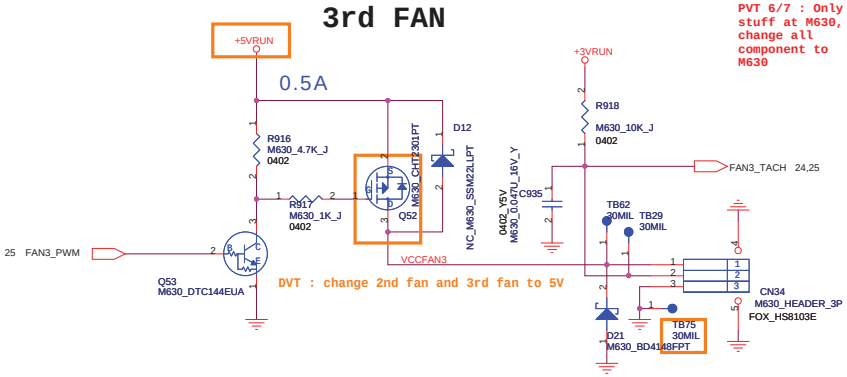


2ND FAN

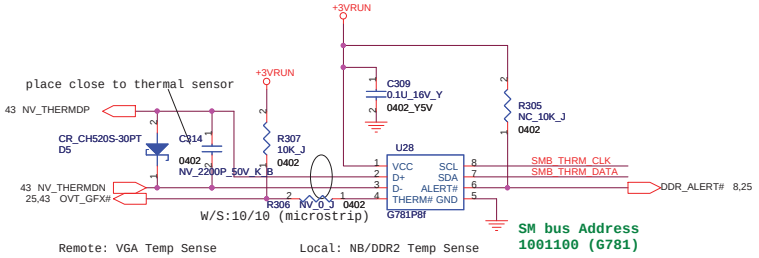


3rd FAN

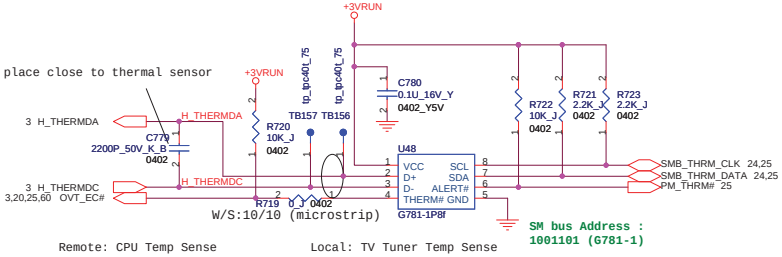
PVT 6/7 : Only stuff at M630, change all component to M630



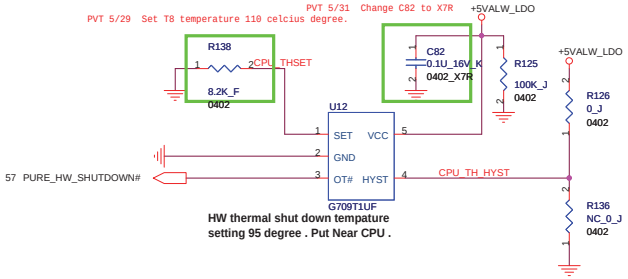
VGA SENSOR



CPU SENSOR



HW THERMAL PROTECTION



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	FAN/HW THERMAL PROTECT	
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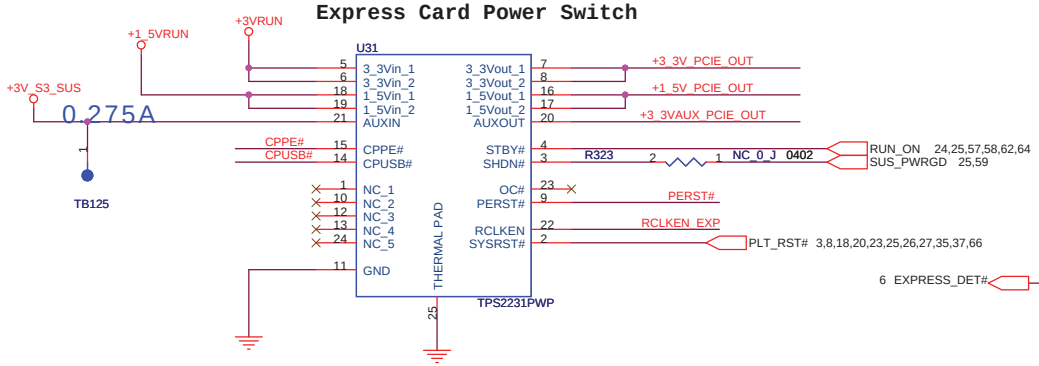
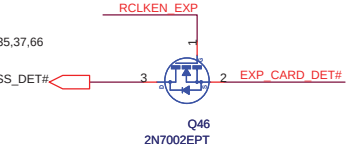
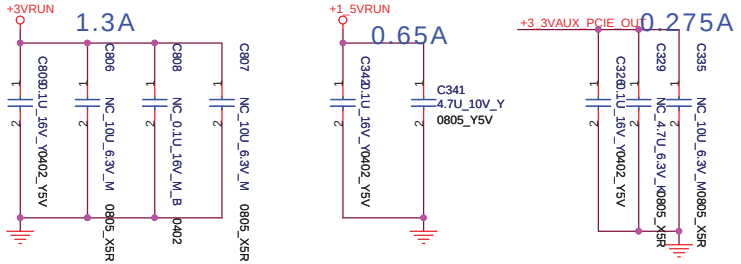
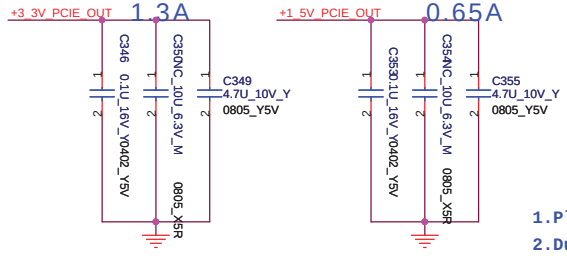
Express Card Power Switch



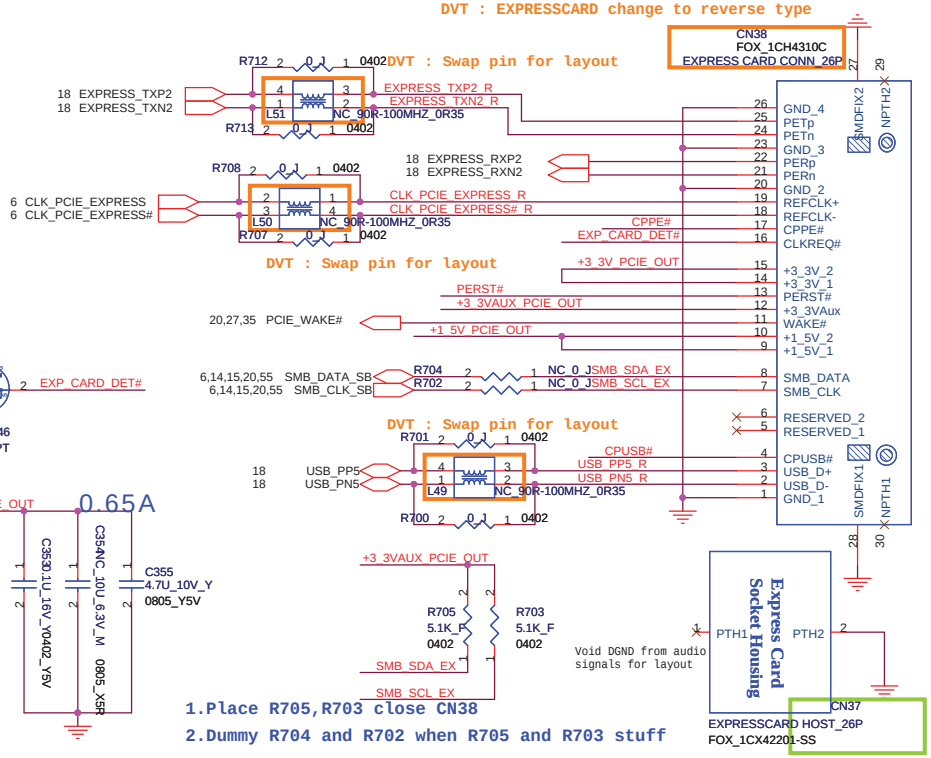






DVT : EXPRESSCARD change to reverse type

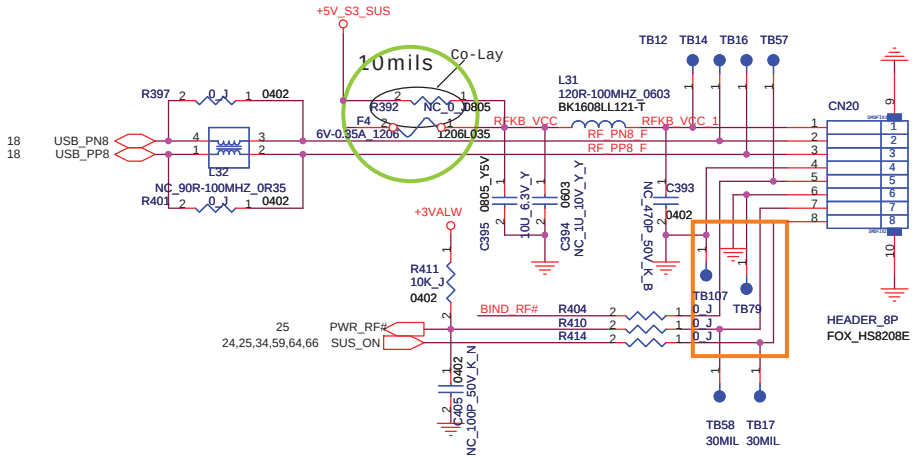
DVT : Swap pin for layout



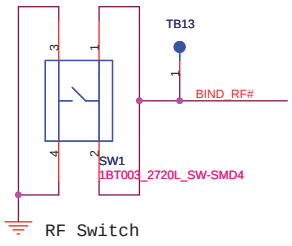
1.Place R705,R703 close CN38

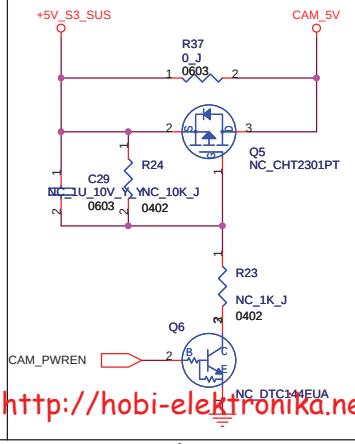
2.Dummy R704 and R702 when R705 and R703 stuff

PVT 6/18 : Change to 1CX42201-SS

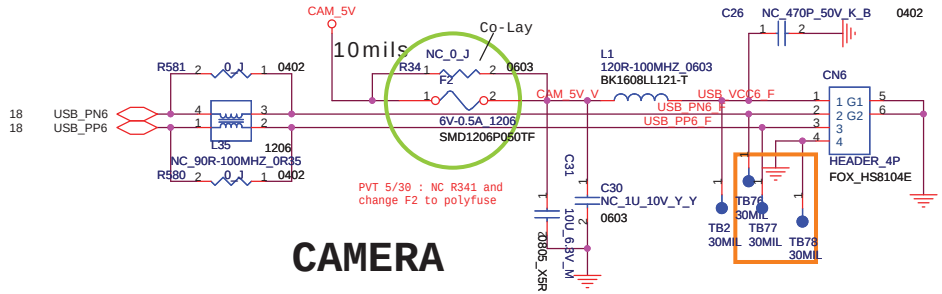


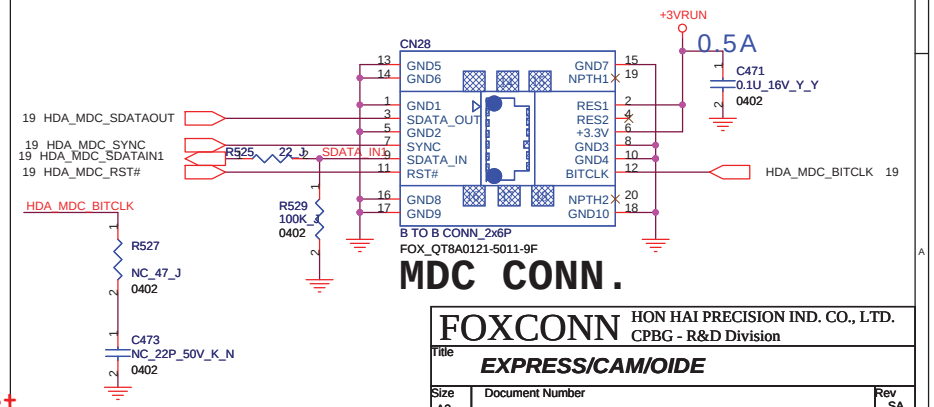
RF KEYBOARD





CAMERA





MDC CONN.

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: EXPRESS/CAM/OIDE

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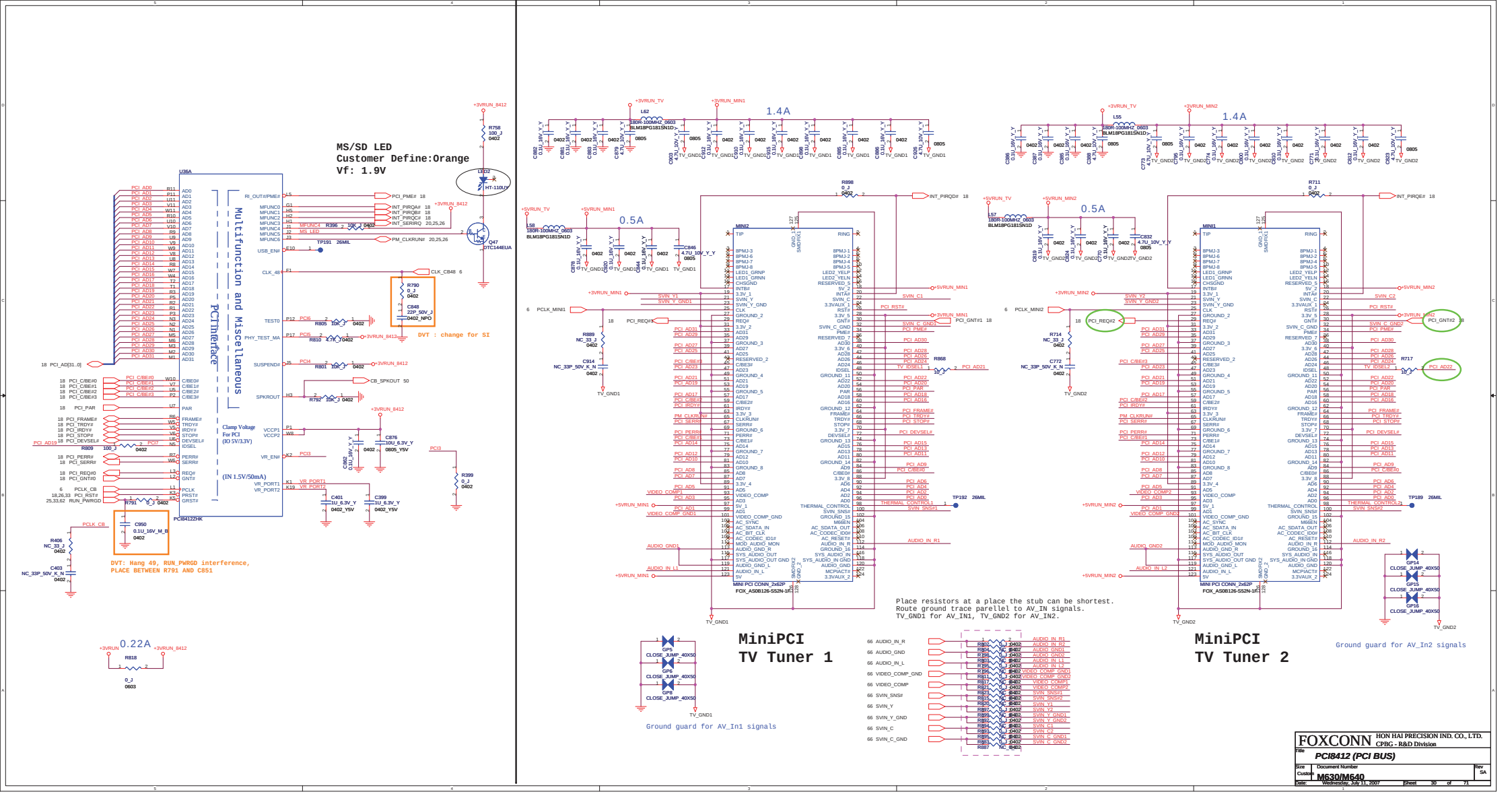

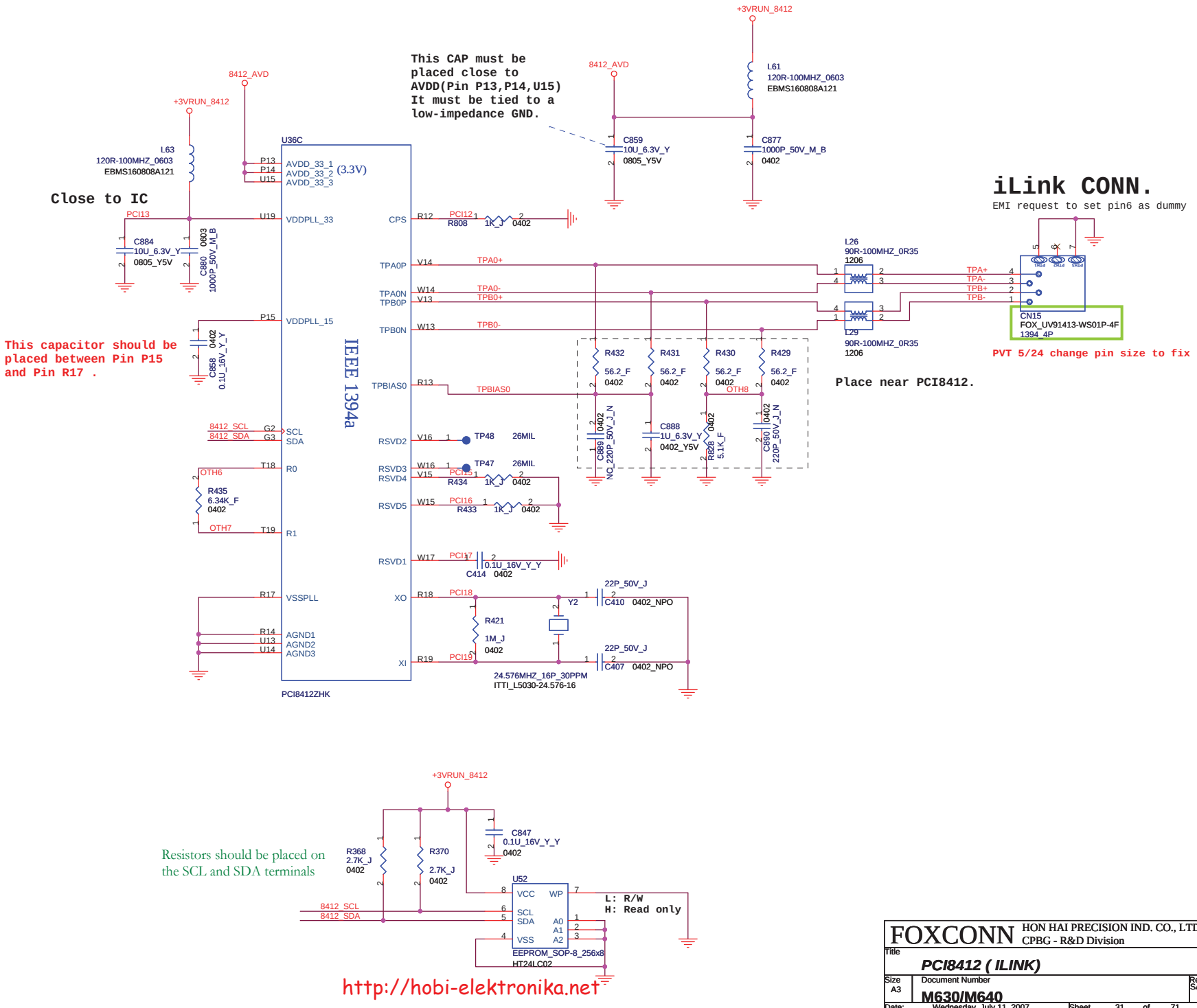
This CAP must be placed close to AVDD(Pin P13,P14,U15) It must be tied to a low-impedance GND.
Close to IC
This capacitor should be placed between Pin P15 and Pin R17 .
Place near PCI8412.
iLink CONN.
EMI request to set pin6 as dummy
PVT 5/24 change pin size to fix
IEEE 1394a
PCI8412ZHK
24.576MHZ_16P_30PPM
ITTI_L5030-24.576-16
EEPROM_SOP-8_256x8
HT24LC02
L: R/W
H: Read only
Resistors should be placed on the SCL and SDA terminals
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FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
PCI8412 (ILINK)
M630/M640
Wednesday, July 11, 2007
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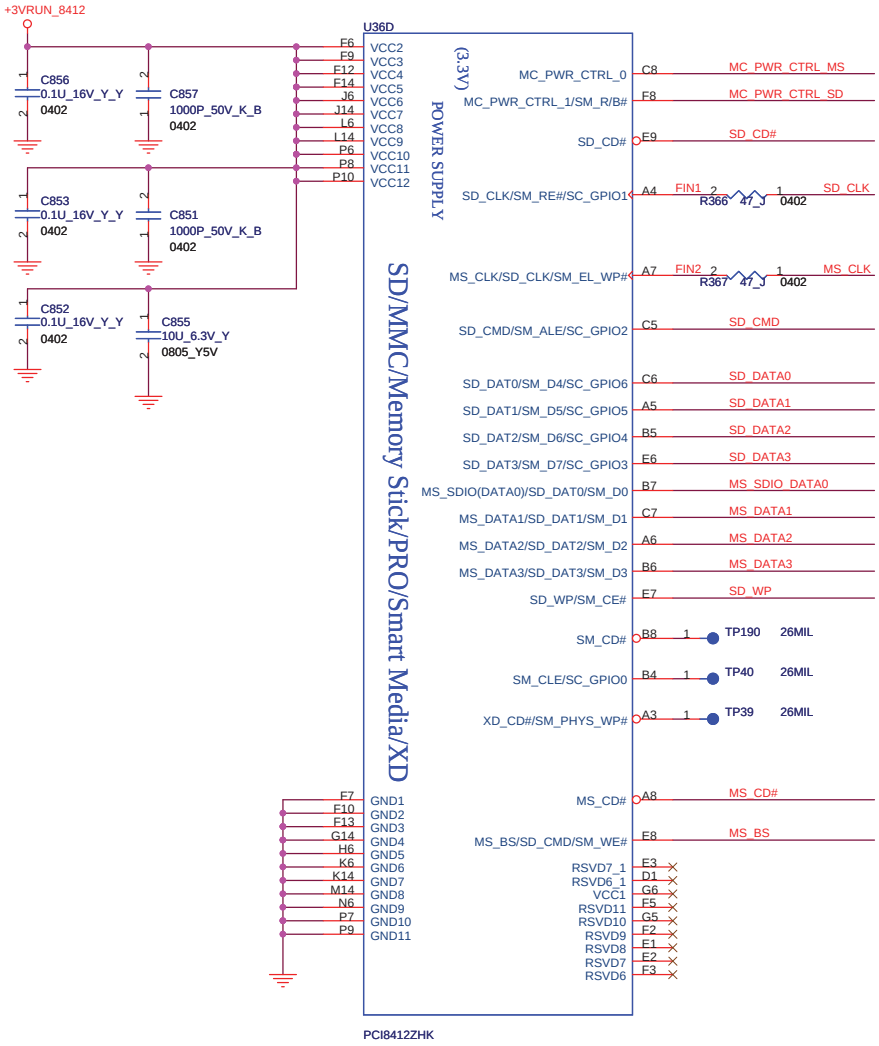
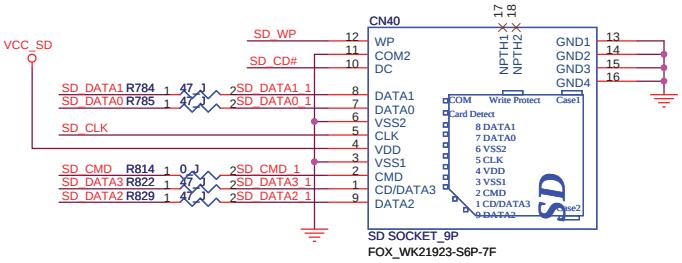
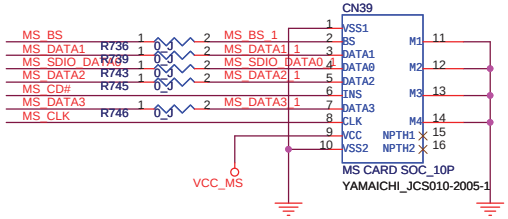
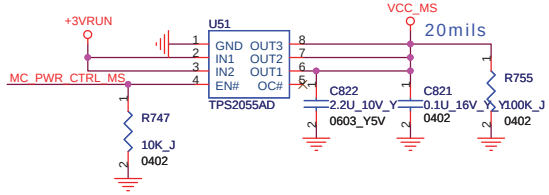


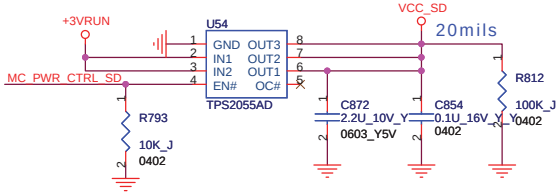
SD

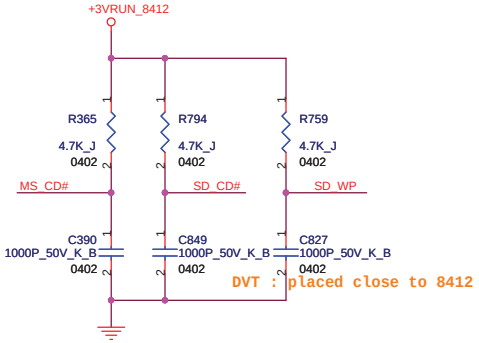


MS Pro/Duo









FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	PCI8412 (MS/SD)/MDC	
Size A3	Document Number M630/M640	Rev SA
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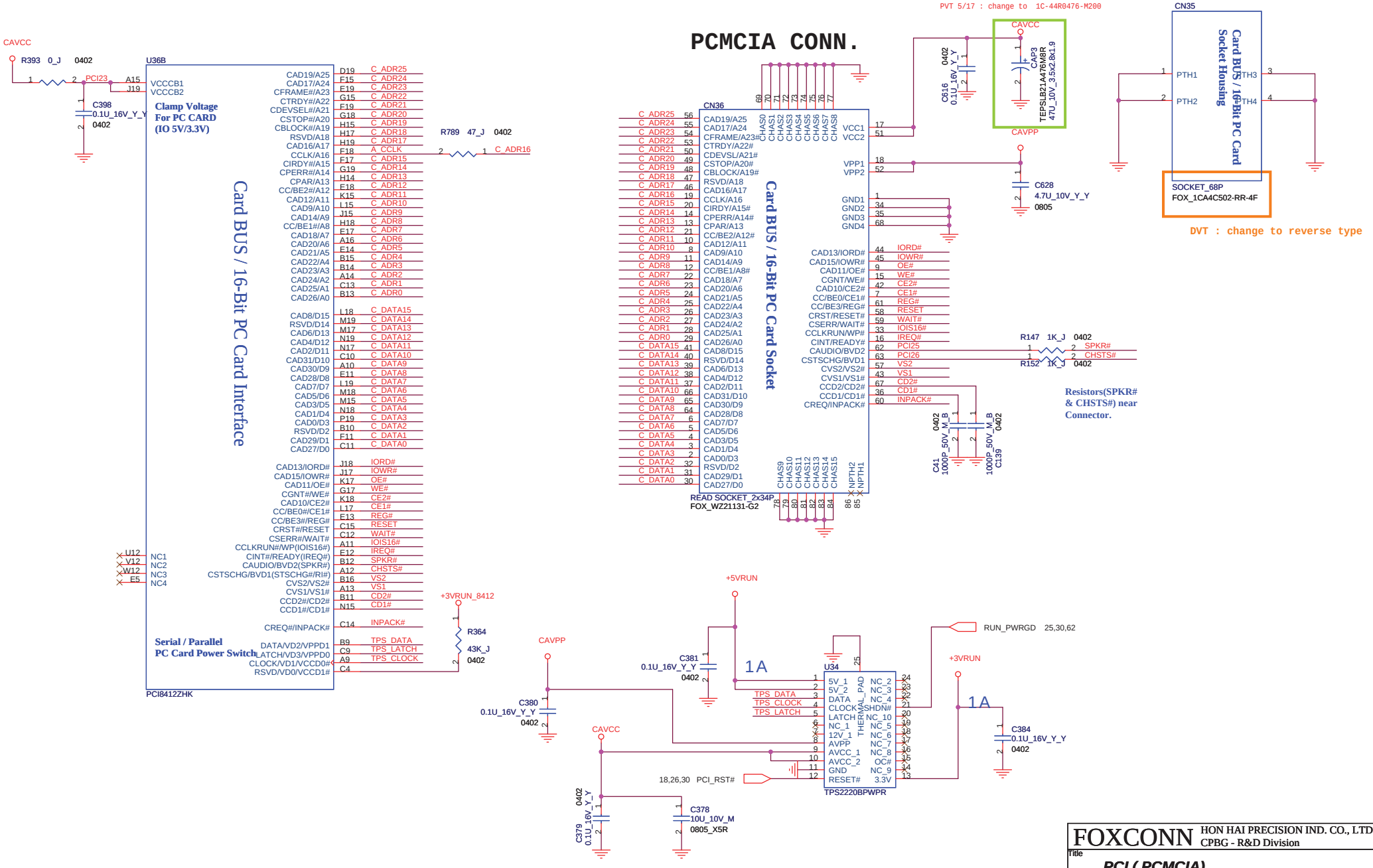
PCMCIA CONN.



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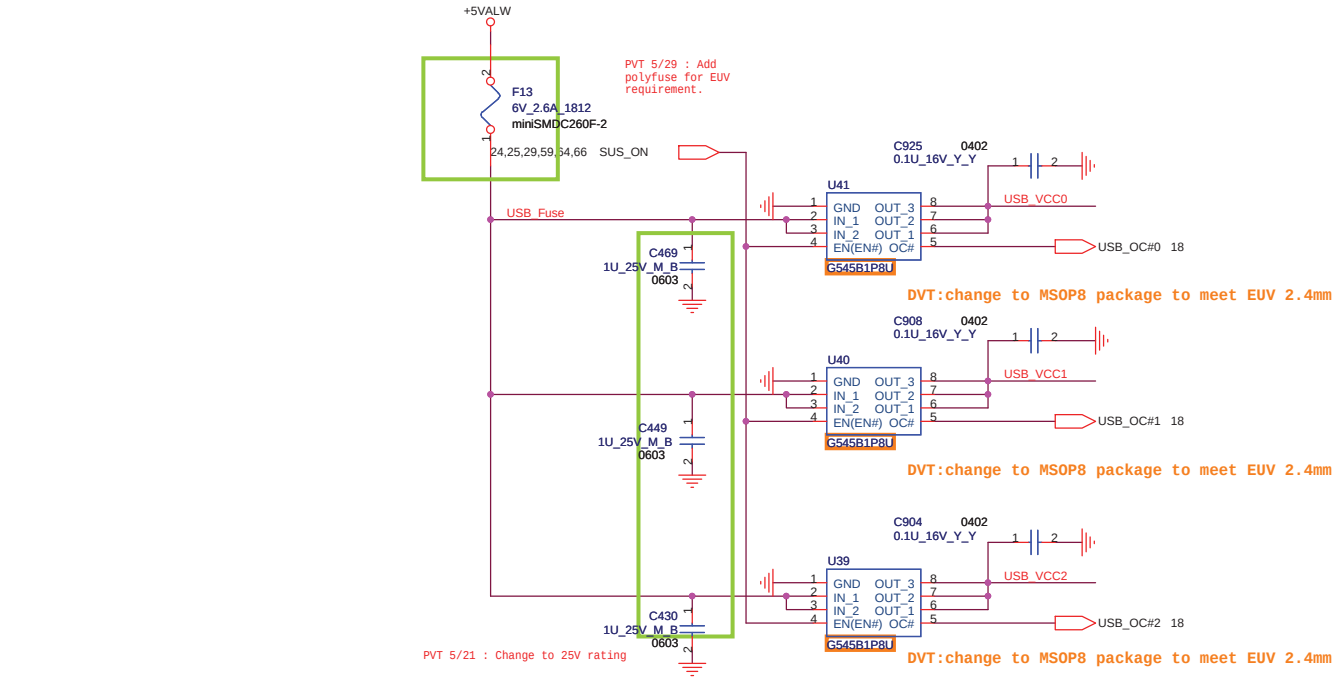
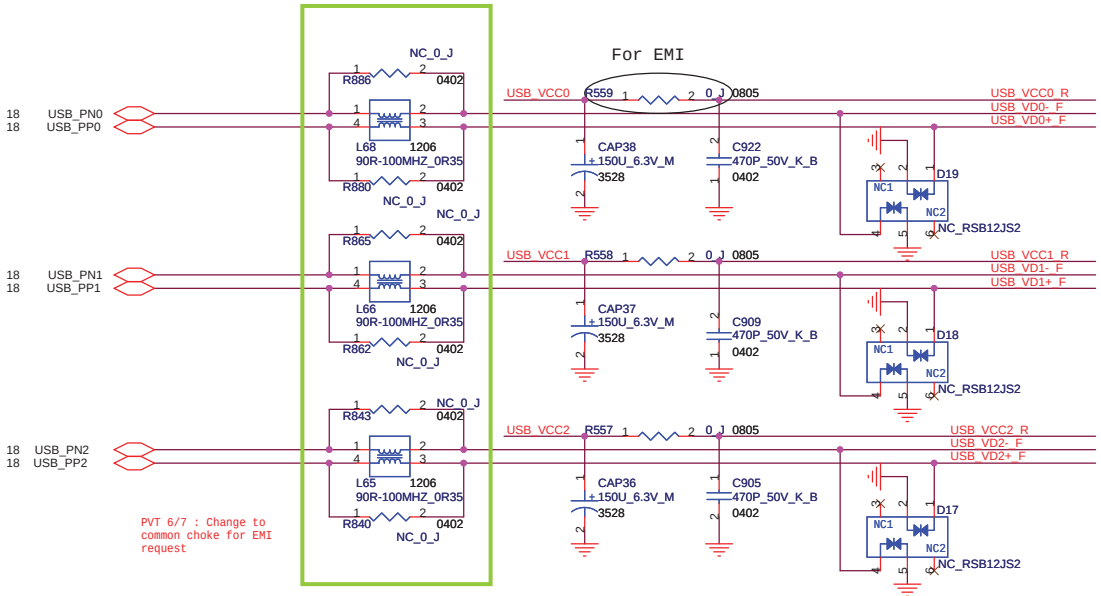
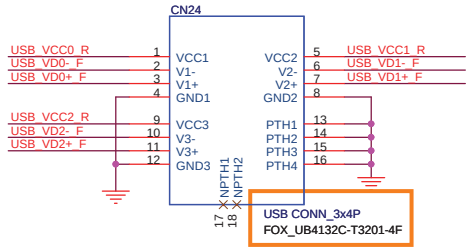
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	PCI (PCMCIA)	
Size A3	Document Number	Rev SA
Date: Wednesday, July 11, 2007	Sheet 33 of 71	





REAR USB CONN X 3



DVT change to black color

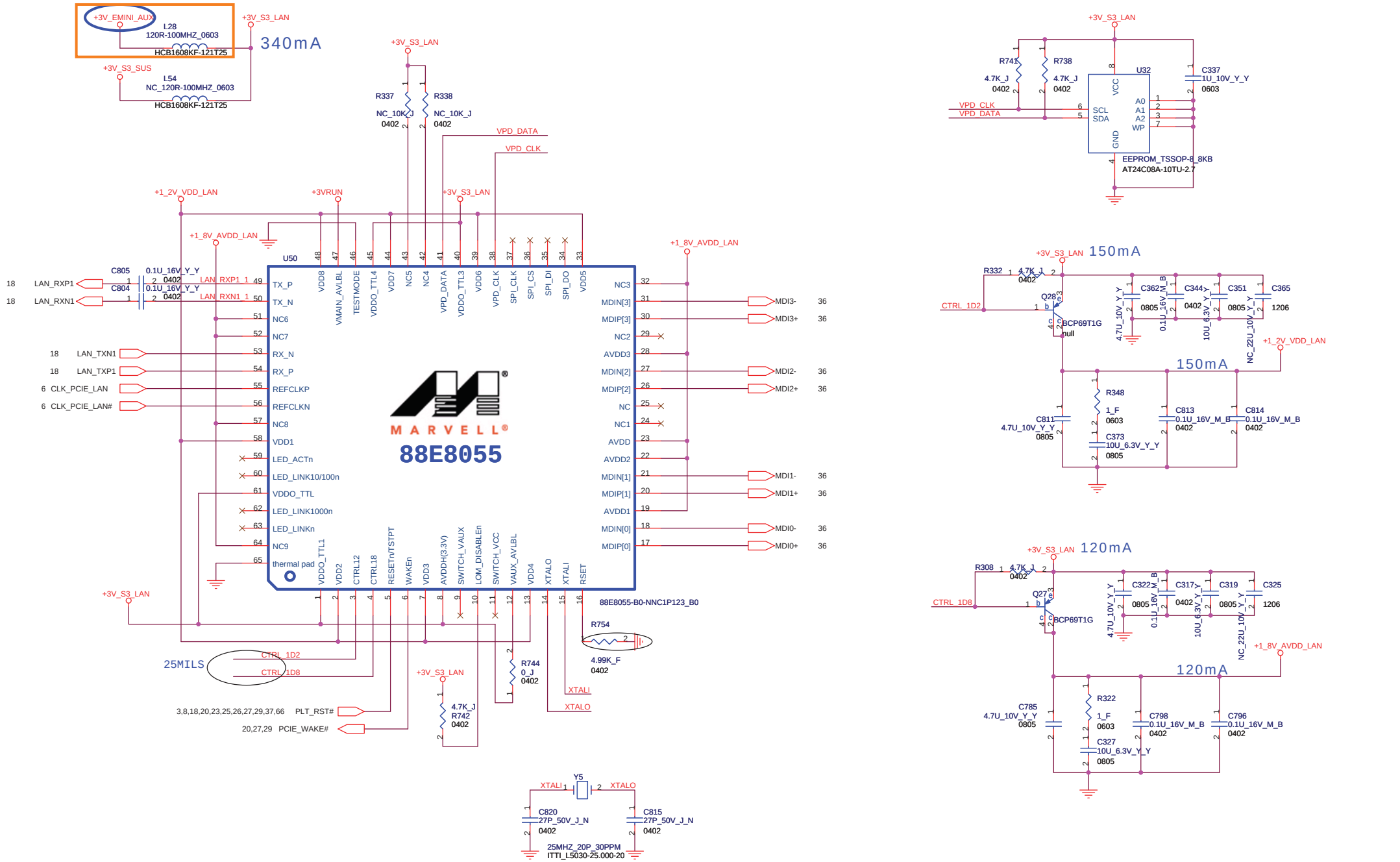
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: USB2.0 PORT

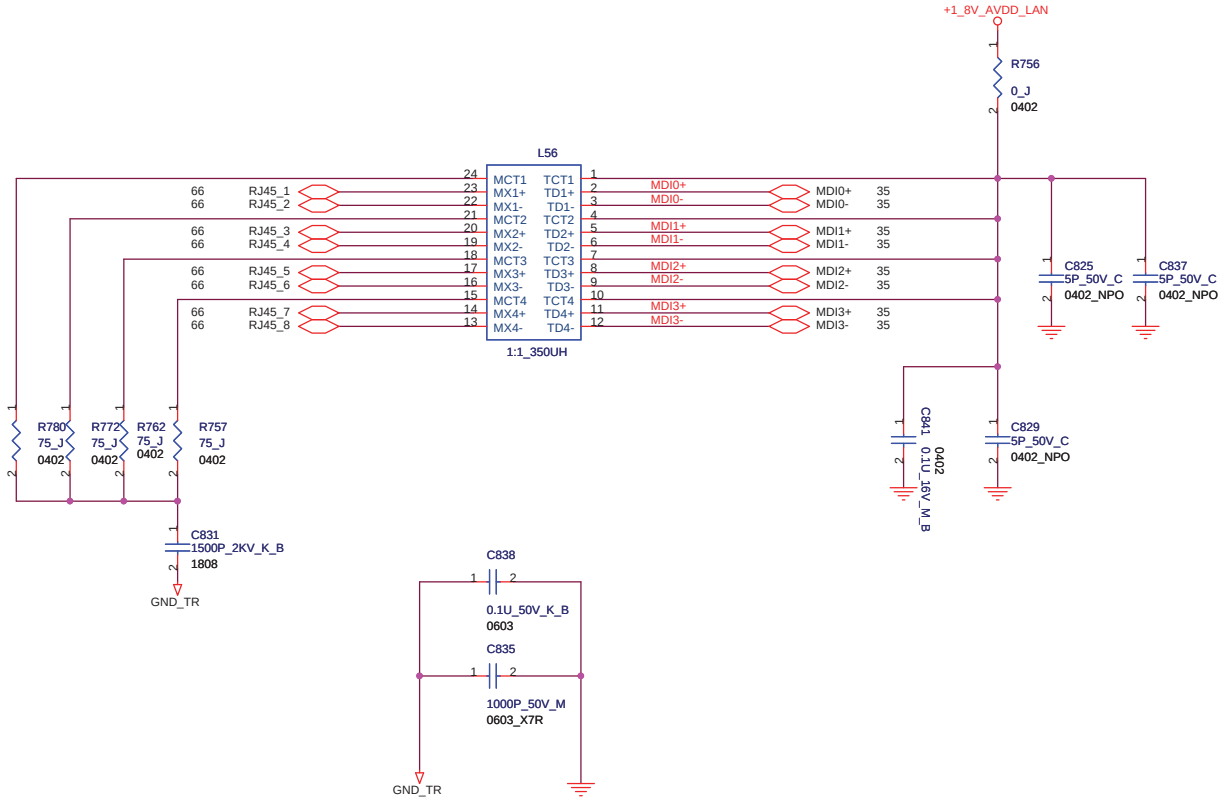
Size: A3 | Document Number: M630/M640 | Rev: SA

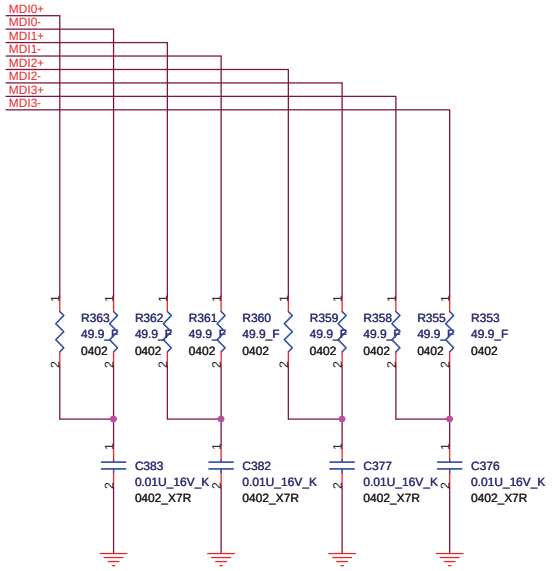
Date: Wednesday, July 11, 2007 | Sheet 34 of 71

To support S4 wake up **DVT : support S4 wake up , power change to +3V_EMINI_AUX**



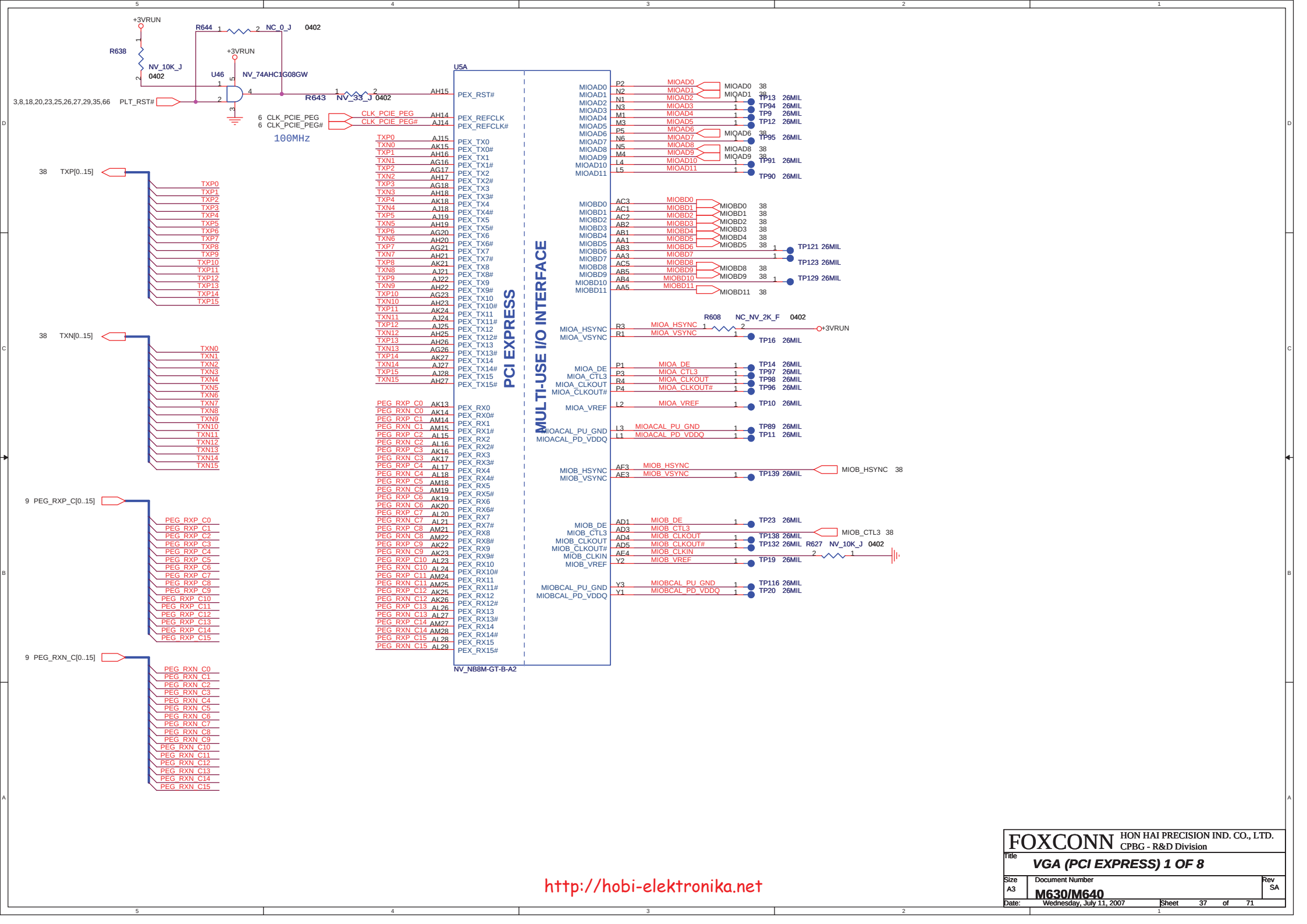
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LAN Controller	
Size A3	Document Number M630/M640	Rev SA
Date: Wednesday, July 11, 2007	Sheet 35 of 71	





FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	LAN Transformer	
Size A3	Document Number M630/M640	Rev SA
Date: Wednesday, July 11, 2007	Sheet 36 of 71	



FOXCONN HON HAI PRECISION IND. CO., LTD.
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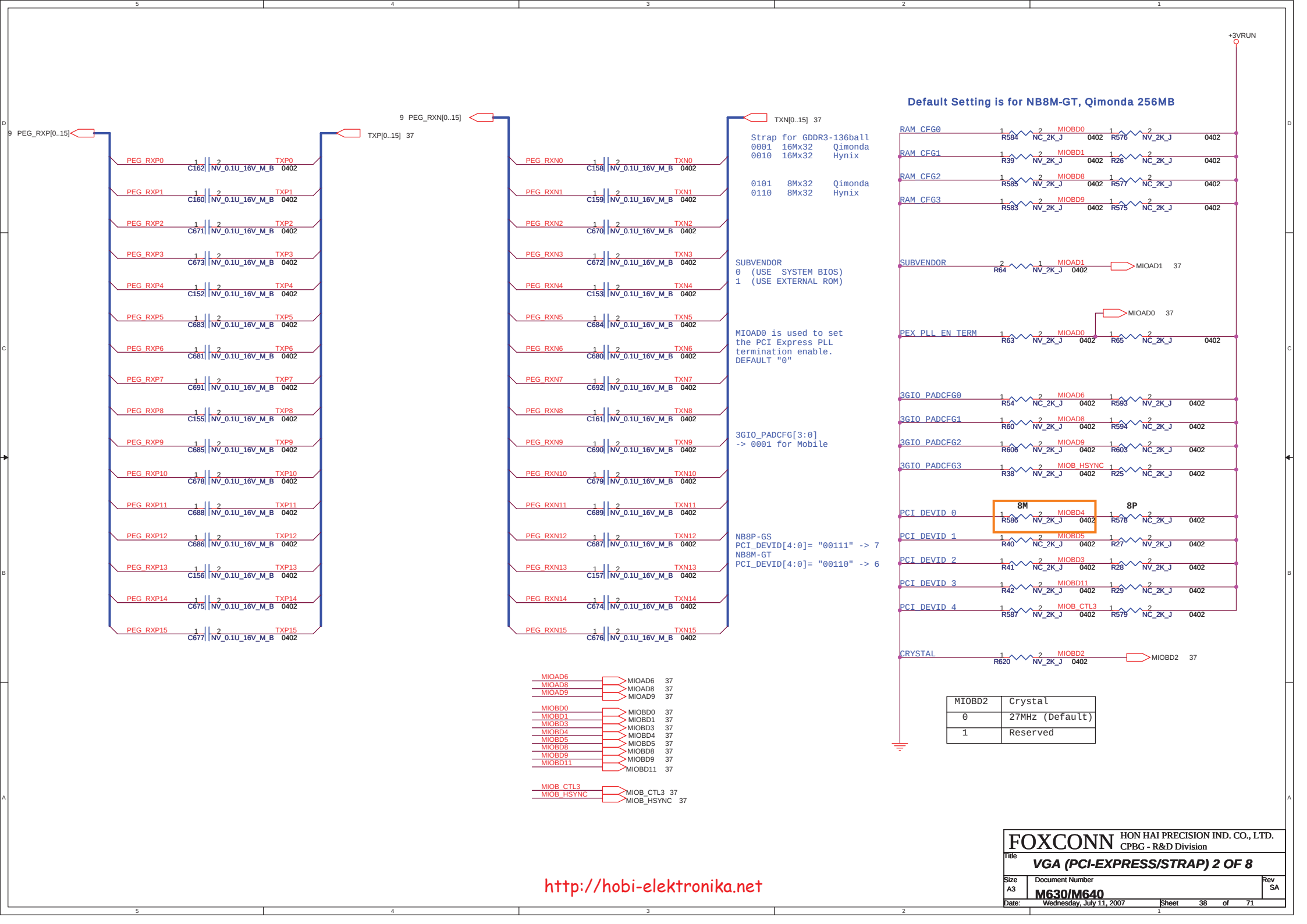
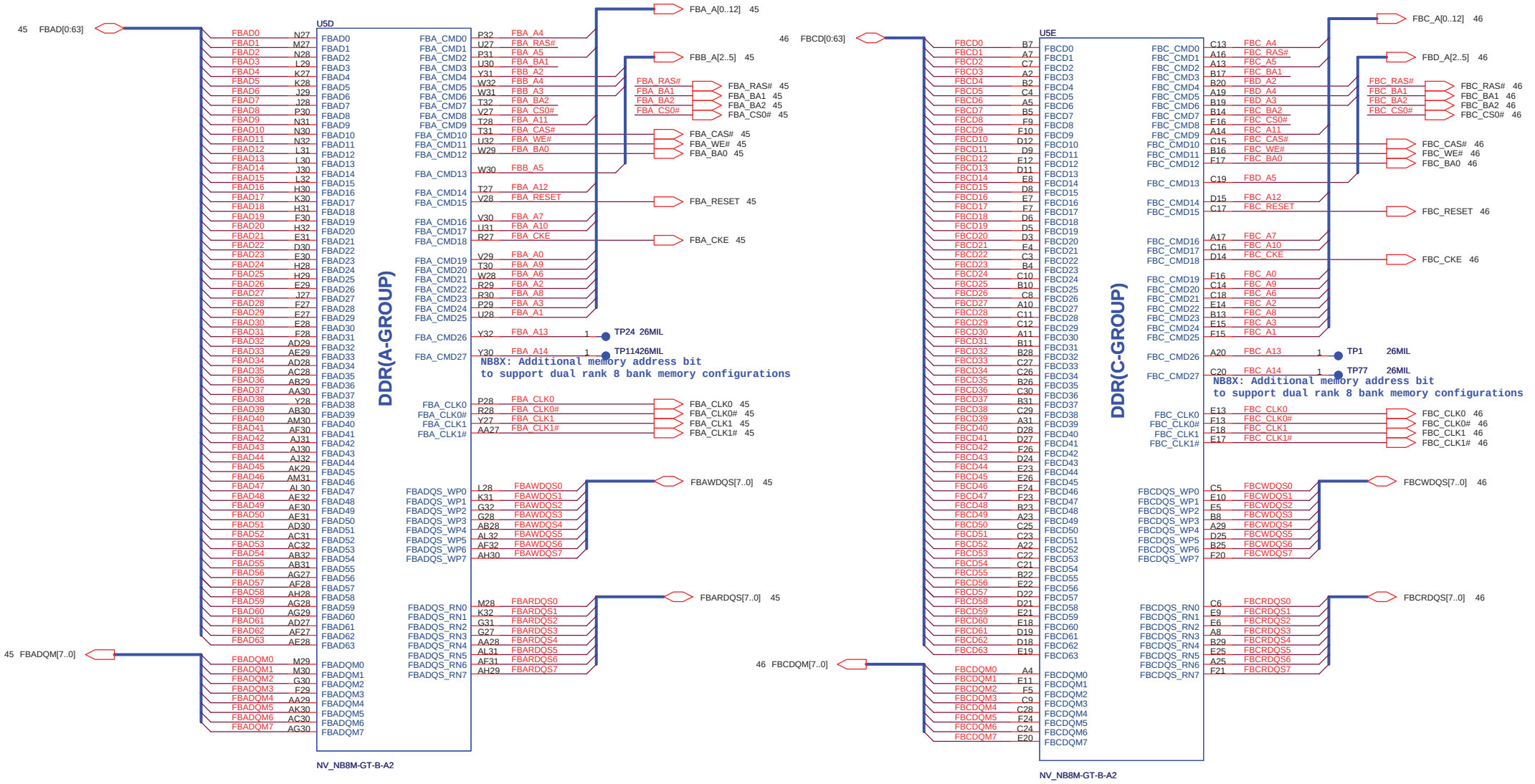
Title: VGA (PCI EXPRESS) 1 OF 8

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 37 of 71



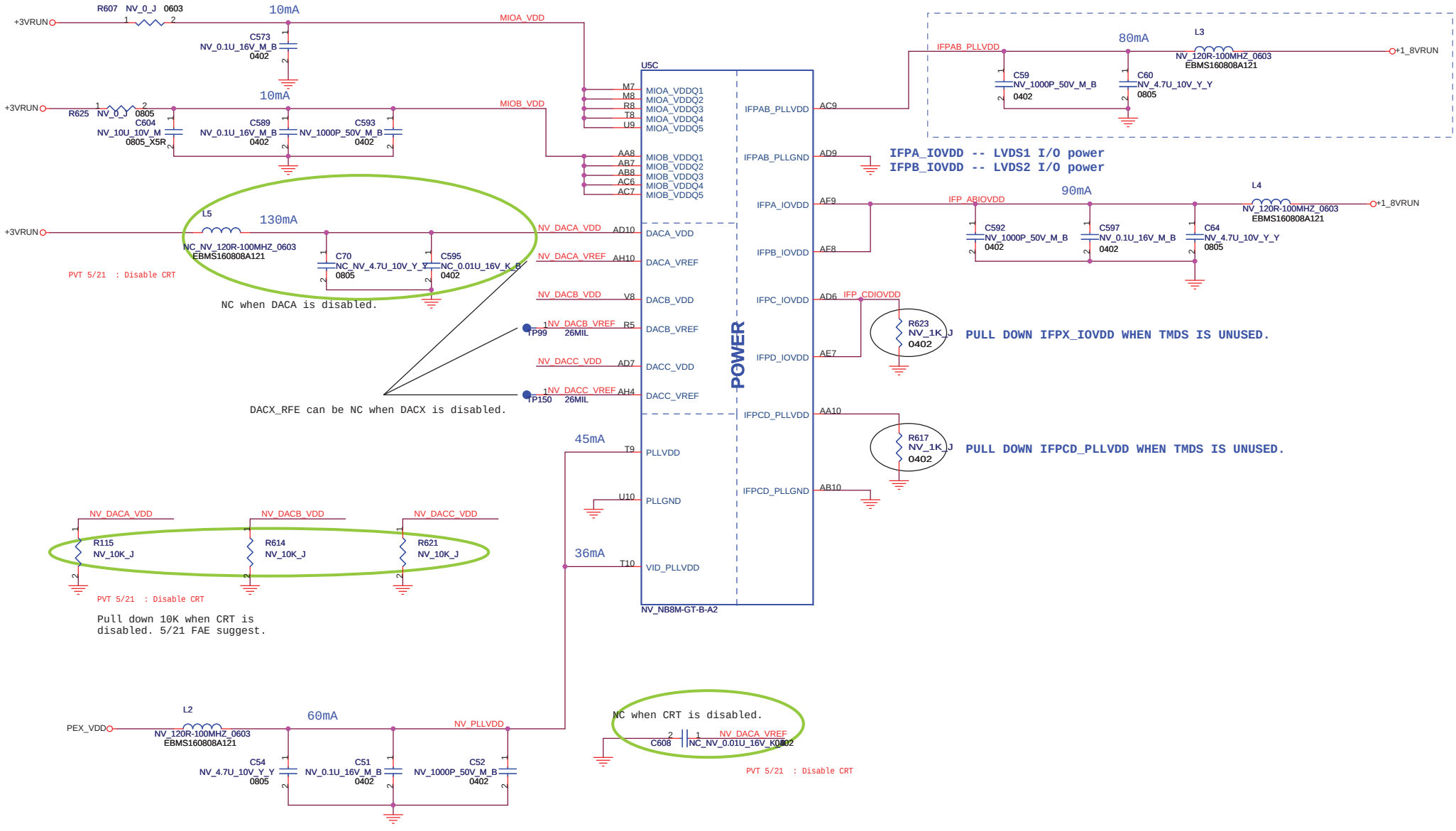


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

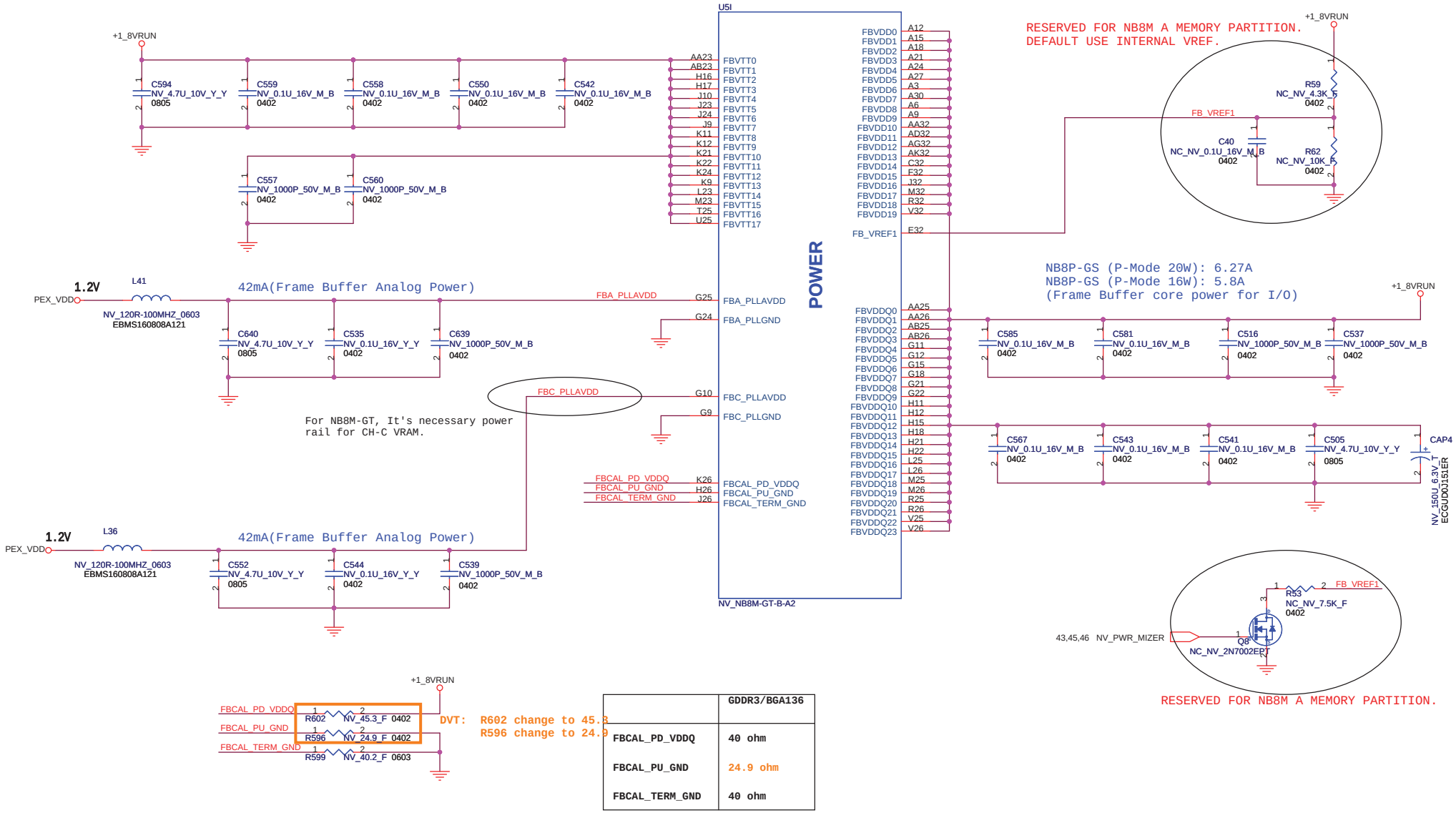
Title: VGA (GDDR) 3 OF 8

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 39 of 71



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VGA (POWER) 4 OF 8
Size A3	Document Number M630/M640
Rev SA	
Date: Wednesday, July 11, 2007	Sheet 40 of 71



	GDDR3/BGA136
FBCAL_PD_VDDQ	40 ohm
FBCAL_PU_GND	24.9 ohm
FBCAL_TERM_GND	40 ohm

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Title: VGA (POWER) 5 OF 8

Size: A3 | Document Number: M630/M640 | Rev: SA

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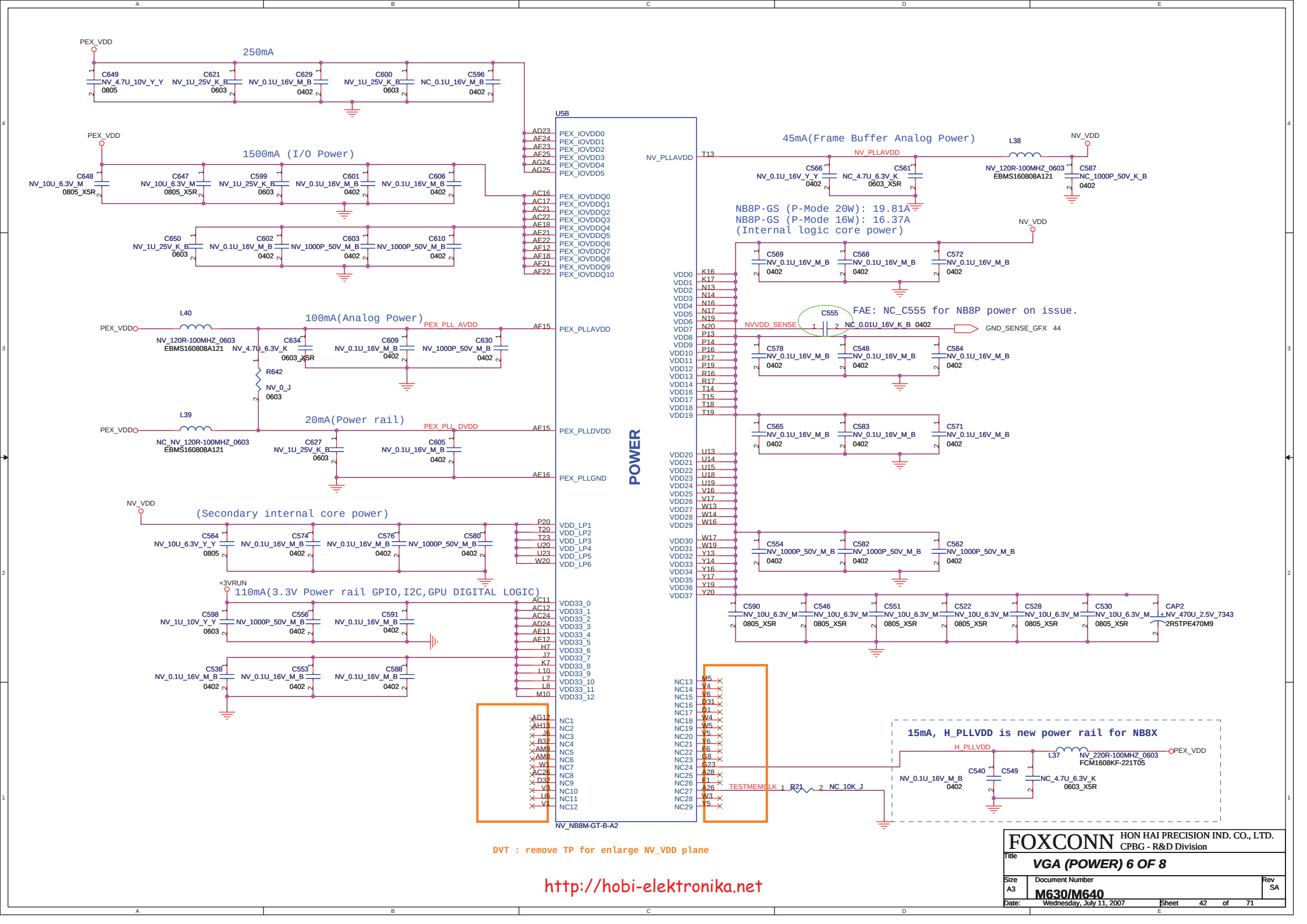

FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: VGA (POWER) 6 OF 8

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NB8X: Slave I2C/SMBUS
compatible interface. (Addr: 0x9e)

2006/8/30 Update

GPIO TABLE			
	I/O	Inter pull low	
GPIO0	I	Yes	HDMI Hot Plug Detect 0(HPD0)
GPIO1	I	Yes	DVI Hot Plug Detect 1(HPD1)
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM) **Active High**
GPIO3	O	No	Panel Power(LCD0_VDD) **Active Low**
GPIO4	O	Yes	LCDBacklight enable(LCD0_BL_EN) **Active High**
GPIO5	O	Yes	GPU Voltage selection (GPU_VID0)
GPIO6	O	Yes	GPU Voltage selection (GPU_VID1)
GPIO7	O	Yes	GPU/Memory Voltage selection(GPU_VID2/MEM_VID)
GPIO8	I/OD	No	Over Temperature Shutdown **Active Low**
GPIO9	I/OD	No	THERMAL ALERT I/O, FAN PWM Control **Active Low**
GPIO10	I/O	No	Memory Vref switch(MEM_VREF)
GPIO11	O	No	Rset switch control. H:SVIDEO(69.8) L:HDTV(88.7)
GPIO12	I	No	AC power detect input (AC_DET)
GPIO13	O	No	Power supply control (PWR_CTRL0)
GPIO14	O	No	Power supply control (PWR_CTRL1)

Could be NC if HDCP is not used.

Boundary scans in conjunction with testmode pin.

DVT : remove TP for enlarge NV_VDD plane

DVT : remove TP for enlarge NV_VDD plane

DVT : remove TP for enlarge NV_VDD plane

DVT : GPIO5 connect to VGA power

DVT : value change to NV_

NB8X: XTALIN use 3.3V level

OVERTEMP LATCHING CIRCUIT

SPREAD SPECTRUM SETTING FOR MK

S0	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.8
M	DOWN	-0.6
1	DOWN	-2.5

0 = connect to GND
M= unconnected
1 = connect directly to VDD

SPREAD SPECTRUM SETTING FOR P1819B

SRS PIN3	SPREAD DIRECTION	Spread Percentage(%)
0	DOWN	-1.25
1	DOWN	-1.75

nVidia support Down -1.25%

This chip can use MK1726 or P1819B

R616 place near GPU
R79 place near spectrum chip

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Title: VGA (MULTIUSE) 7 OF 8

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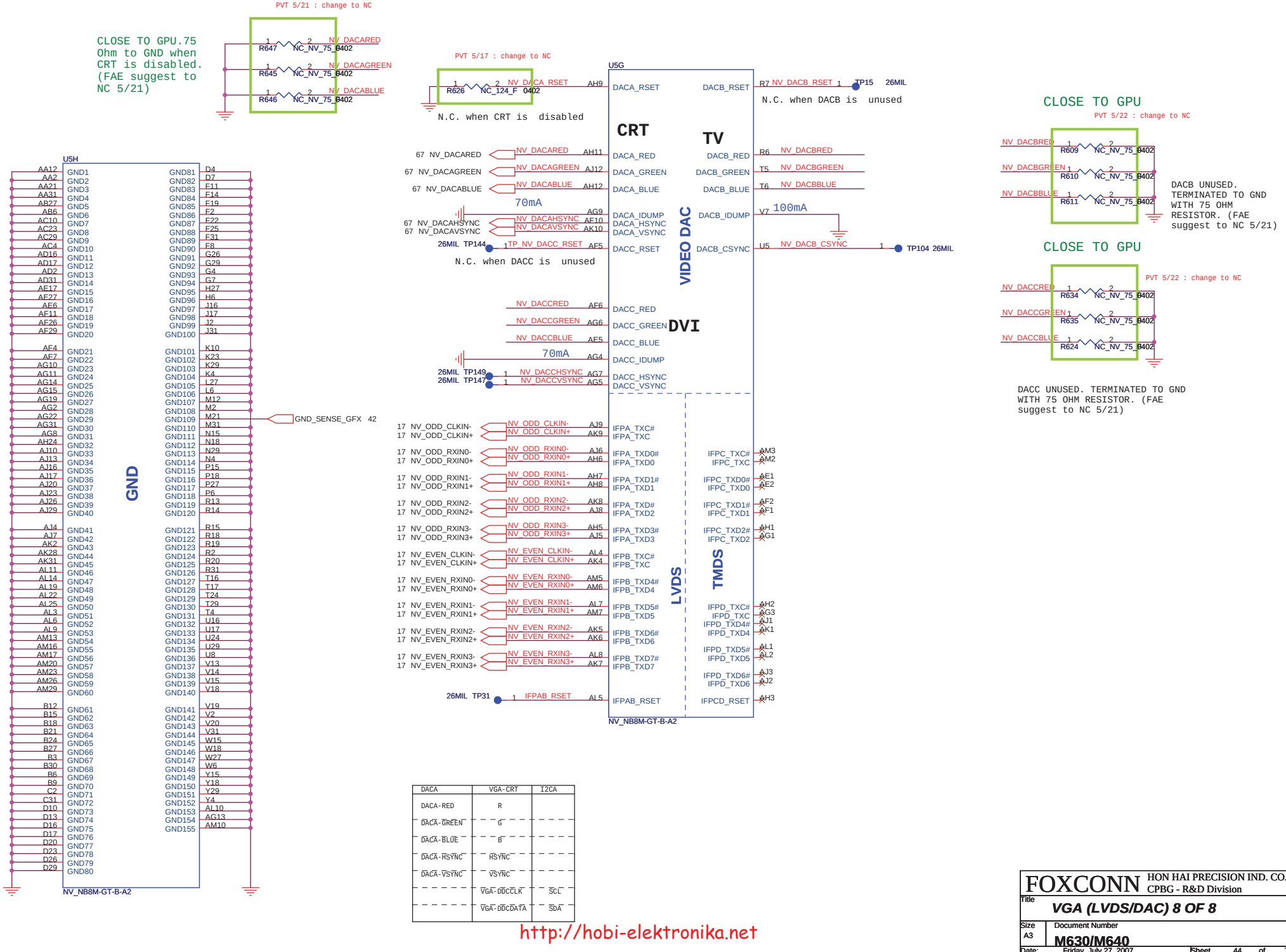
CLOSE TO GPU.75 Ohm to GND when CRT is disabled. (FAE suggest to NC 5/21)
PVT 5/21 : change to NC
R647 NC_NV_75_0402 NV_DACARED
R645 NC_NV_75_0402 NV_DACAGREEN
R646 NC_NV_75_0402 NV_DACABLUE
PVT 5/17 : change to NC
R626 NC_124_F 0402 NV_DACA_RSET
N.C. when CRT is disabled
U5H
GND
NV_NB8M-GT-B-A2
GND_SENSE_GFX 42
U5G
CRT
TV
VIDEO DAC
DACA_RSET
DACB_RSET
R7 NV_DACB_RSET TP15 26MIL
N.C. when DACB is unused
67 NV_DACARED NV_DACARED AH11
67 NV_DACAGREEN NV_DACAGREEN AJ12
67 NV_DACABLUE NV_DACABLUE AH12
DACA_RED
DACA_GREEN
DACA_BLUE
DACB_RED
DACB_GREEN
DACB_BLUE
R6 NV_DACBRED
T5 NV_DACBGREEN
T6 NV_DACBBLUE
70mA
100mA
DACA_IDUMP
DACB_IDUMP
V7
67 NV_DACAHSYNC NV_DACAHSYNC AE10
67 NV_DACAVSYNC NV_DACAVSYNC AK10
DACA_HSYNC
DACA_VSYNC
26MIL TP144 TP_NV_DACC_RSET AF5
DACC_RSET
DACB_CSYNC
U5 NV_DACB_CSYNC TP104 26MIL
N.C. when DACC is unused
DVI
NV_DACCRED AF6
NV_DACCGREEN AG6
NV_DACCBLUE AF5
DACC_RED
DACC_GREEN
DACC_BLUE
70mA AG4
DACC_IDUMP
26MIL TP149 NV_DACCHSYNC AG7
26MIL TP147 NV_DACCVSYNC AG5
DACC_HSYNC
DACC_VSYNC
LVDS
TMDS
17 NV_ODD_CLKIN- NV_ODD_CLKIN- AJ9
17 NV_ODD_CLKIN+ NV_ODD_CLKIN+ AK9
IFPA_TXC#
IFPA_TXC
17 NV_ODD_RXIN0- NV_ODD_RXIN0- AJ6
17 NV_ODD_RXIN0+ NV_ODD_RXIN0+ AH6
IFPA_TXD0#
IFPA_TXD0
IFPC_TXC# AM3
IFPC_TXC AM2
17 NV_ODD_RXIN1- NV_ODD_RXIN1- AH7
17 NV_ODD_RXIN1+ NV_ODD_RXIN1+ AH8
IFPA_TXD1#
IFPA_TXD1
IFPC_TXD0# AE1
IFPC_TXD0 AE2
17 NV_ODD_RXIN2- NV_ODD_RXIN2- AK8
17 NV_ODD_RXIN2+ NV_ODD_RXIN2+ AJ8
IFPA_TXD#
IFPA_TXD2
IFPC_TXD1# AF2
IFPC_TXD1 AF1
17 NV_ODD_RXIN3- NV_ODD_RXIN3- AH5
17 NV_ODD_RXIN3+ NV_ODD_RXIN3+ AJ5
IFPA_TXD3#
IFPA_TXD3
IFPC_TXD2# AH1
IFPC_TXD2 AG1
17 NV_EVEN_CLKIN- NV_EVEN_CLKIN- AL4
17 NV_EVEN_CLKIN+ NV_EVEN_CLKIN+ AK4
IFPB_TXC#
IFPB_TXC
17 NV_EVEN_RXIN0- NV_EVEN_RXIN0- AM5
17 NV_EVEN_RXIN0+ NV_EVEN_RXIN0+ AM6
IFPB_TXD4#
IFPB_TXD4
17 NV_EVEN_RXIN1- NV_EVEN_RXIN1- AL7
17 NV_EVEN_RXIN1+ NV_EVEN_RXIN1+ AM7
IFPB_TXD5#
IFPB_TXD5
IFPD_TXC# AH2
IFPD_TXC AG3
IFPD_TXD4# AJ1
IFPD_TXD4 AK1
17 NV_EVEN_RXIN2- NV_EVEN_RXIN2- AK5
17 NV_EVEN_RXIN2+ NV_EVEN_RXIN2+ AK6
IFPB_TXD6#
IFPB_TXD6
IFPD_TXD5# AL1
IFPD_TXD5 AL2
17 NV_EVEN_RXIN3- NV_EVEN_RXIN3- AL8
17 NV_EVEN_RXIN3+ NV_EVEN_RXIN3+ AK7
IFPB_TXD7#
IFPB_TXD7
IFPD_TXD6# AJ3
IFPD_TXD6 AJ2
26MIL TP31 IFPAB_RSET AL5
IFPAB_RSET
IFPCD_RSET AH3
NV_NB8M-GT-B-A2
CLOSE TO GPU
PVT 5/22 : change to NC
R609 NC_NV_75_0402 NV_DACBRED
R610 NC_NV_75_0402 NV_DACBGREEN
R611 NC_NV_75_0402 NV_DACBBLUE
DACB UNUSED. TERMINATED TO GND WITH 75 OHM RESISTOR. (FAE suggest to NC 5/21)
CLOSE TO GPU
PVT 5/22 : change to NC
R634 NC_NV_75_0402 NV_DACCRED
R635 NC_NV_75_0402 NV_DACCGREEN
R624 NC_NV_75_0402 NV_DACCBLUE
DACC UNUSED. TERMINATED TO GND WITH 75 OHM RESISTOR. (FAE suggest to NC 5/21)
DACA VGA-CRT I2CA
DACA-RED R
DACA-GREEN G
DACA-BLUE B
DACA-HSYNC HSYNC
DACA-VSYNC VSYNC
VGA-DDCCLK SCL
VGA-DDCDATA SDA
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CPBG - R&D Division
Title VGA (LVDS/DAC) 8 OF 8
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Document Number M630/M640
Rev SA
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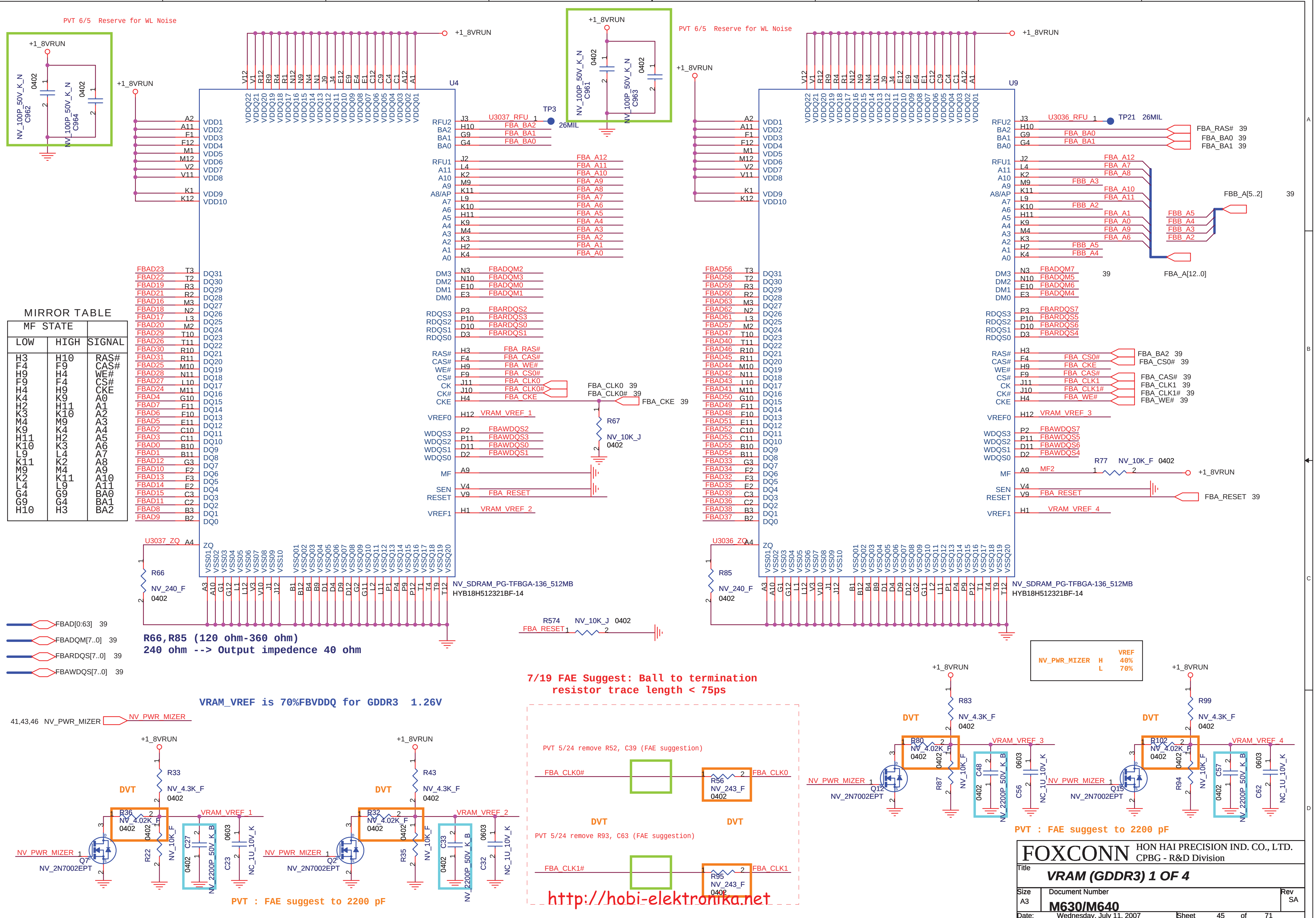

PVT 6/5 Reserve for WL Noise
+1_8VRUN
NV_100P_50V_K_N
C962
C964
C961
C963
U4
U9
TP3
TP21
26MIL
U3037_RFU
U3036_RFU
NV_SDRAM_PG-TFBGA-136_512MB
HYB18H512321BF-14
R66
R85
NV_240_F
0402
R67
NV_10K_J
R574
FBA_RESET
R77
NV_10K_F
FBAD[0:63] 39
FBADQM[7..0] 39
FBARDQS[7..0] 39
FBAWDQS[7..0] 39
FBA_A[12..0]
FBB_A[5..2] 39
FBA_RAS# 39
FBA_BA0 39
FBA_BA1 39
FBA_BA2 39
FBA_CS0# 39
FBA_CAS# 39
FBA_CLK1 39
FBA_CLK1# 39
FBA_WE# 39
FBA_CLK0 39
FBA_CLK0# 39
FBA_CKE 39
FBA_RESET 39
41,43,46 NV_PWR_MIZER
NV_PWR_MIZER
VRAM_VREF_1
VRAM_VREF_2
VRAM_VREF_3
VRAM_VREF_4
R33
R43
R83
R99
NV_4.3K_F
R36
R32
R80
R102
NV_4.02K_F
R22
R35
R87
R94
C27
C33
C48
C57
NV_2200P_50V_K_B
C23
C32
C56
C62
NC_1U_10V_K
0603
Q7
Q2
Q12
Q15
NV_2N7002EPT
DVT
PVT : FAE suggest to 2200 pF
PVT 5/24 remove R52, C39 (FAE suggestion)
PVT 5/24 remove R93, C63 (FAE suggestion)
FBA_CLK0#
FBA_CLK0
FBA_CLK1#
FBA_CLK1
R56
R95
NV_243_F

MIRROR TABLE

MF STATE		
LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F9	F4	CS#
H4	H9	CKE
K4	K9	A0
H2	H11	A1
K3	K10	A2
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
G9	G4	BA1
H10	H3	BA2

R66,R85 (120 ohm-360 ohm)
240 ohm --> Output impedence 40 ohm

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

7/19 FAE Suggest: Ball to termination resistor trace length < 75ps

	VREF
NV_PWR_MIZER H	40%
L	70%

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PVT 6/5 Reserve for WL Noise

PVT 6/5 Reserve for WL Noise

MIRROR TABLE

MF STATE		
LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F9	F4	CS#
H4	H9	CKE
K4	K9	A0
H2	H11	A1
K3	K10	A2
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
G9	G4	BA1
H10	H3	BA2

R6,R15(120 ohm-360 ohm)
240 ohm --> Output impedence 40 ohm

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

7/19 FAE Suggest: Ball to termination resistor trace length < 75ps

PVT 5/24 remove R17, C24 (FAE suggestion)

PVT 5/24 remove R561, C487 (FAE suggestion)

PVT : FAE suggest to 2200 pF

PVT : FAE suggest to 2200 pF

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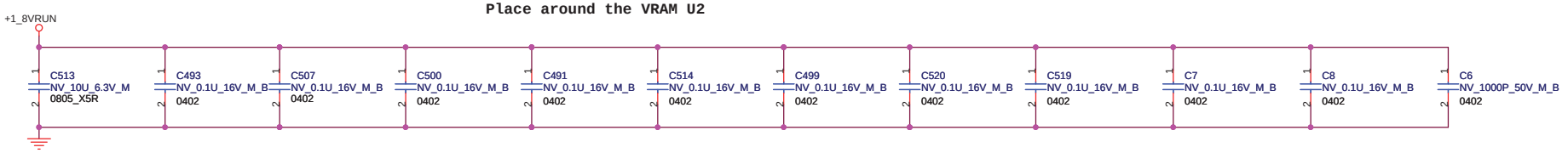
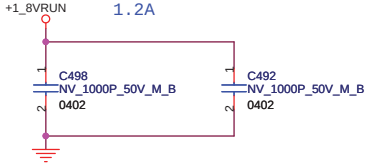
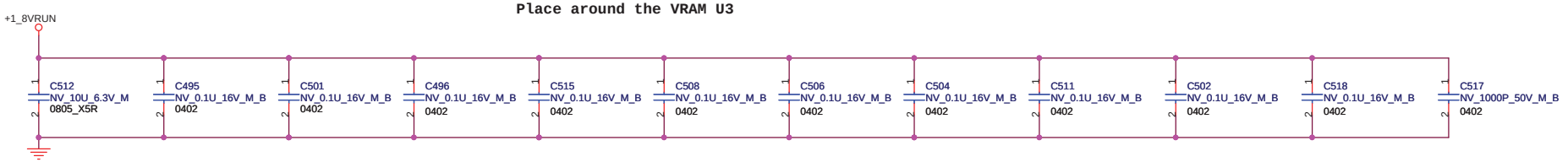
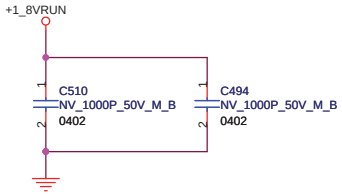
Place around the VRAM U2





Place around the VRAM U3





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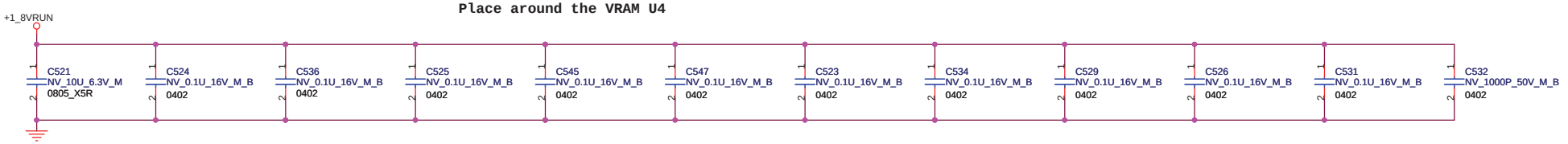
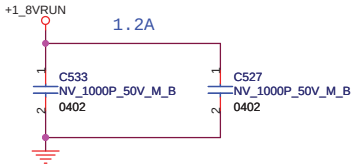
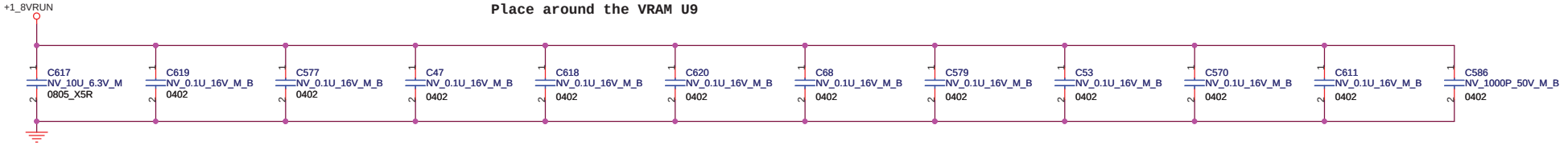
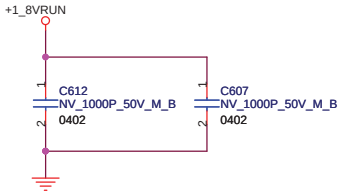
Place around the VRAM U4





Place around the VRAM U9





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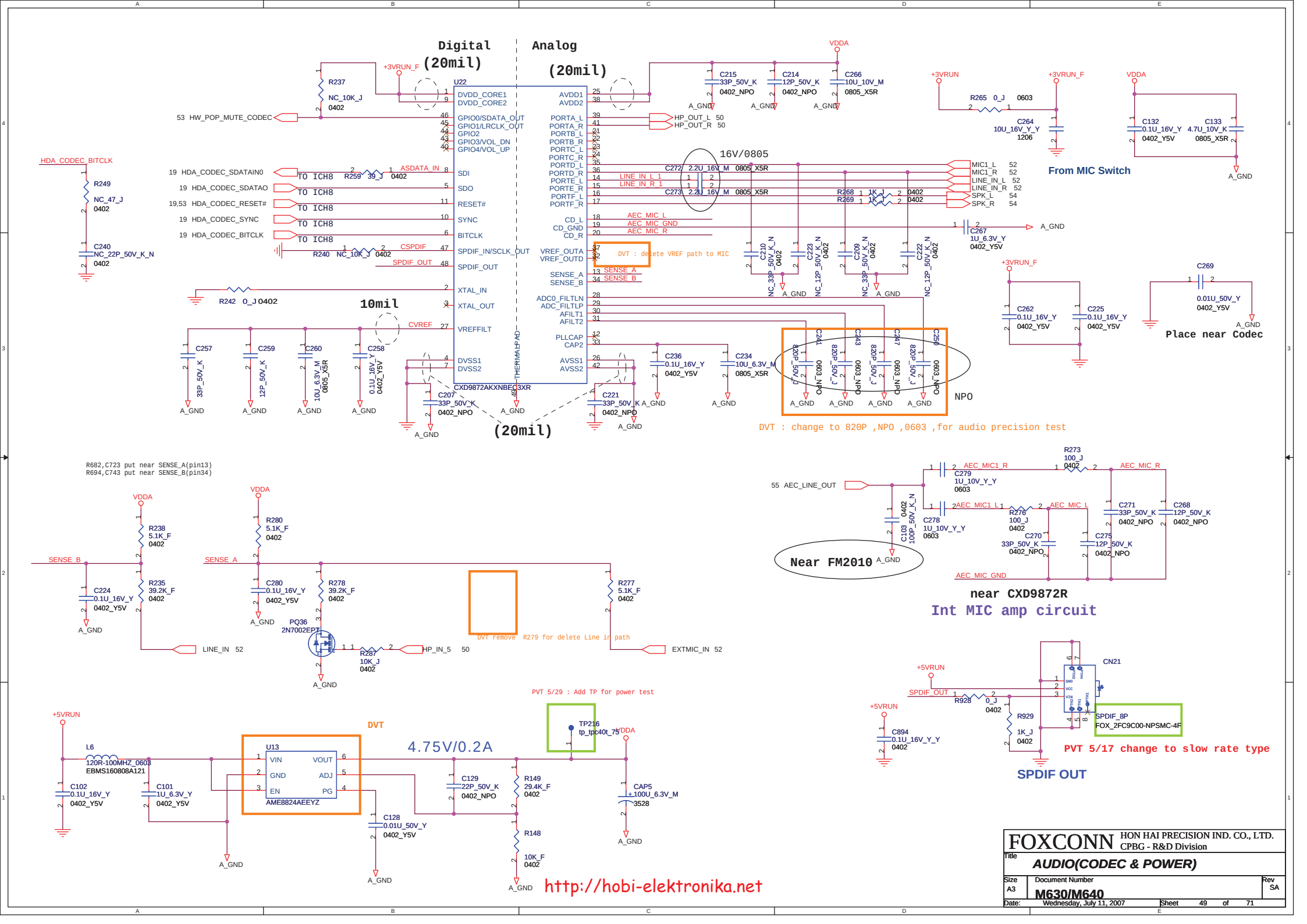
Digital
(20mil)
Analog
(20mil)
U22
CXD9872AKXNBEC3XR
DVDD_CORE1
DVDD_CORE2
GPIO0/SDATA_OUT
GPIO1/LRCLK_OUT
GPIO2
GPIO3/VOL_DN
GPIO4/VOL_UP
SDI
SDO
RESET#
SYNC
BITCLK
SPDIF_IN/SCLK_OUT
SPDIF_OUT
XTAL_IN
XTAL_OUT
VREFFILT
DVSS1
DVSS2
AVDD1
AVDD2
PORTA_L
PORTA_R
PORTB_L
PORTB_R
PORTC_L
PORTC_R
PORTD_L
PORTD_R
PORTE_L
PORTE_R
PORTF_L
PORTF_R
CD_L
CD_GND
CD_R
VREF_OUTA
VREF_OUTD
SENSE_A
SENSE_B
ADC0_FILTLN
ADC_FILTLP
AFILT1
AFILT2
PLLCAP
CAP2
AVSS1
AVSS2
THERMAL PAD
+3VRUN_F
VDDA
A_GND
HP_OUT_L
HP_OUT_R
MIC1_L
MIC1_R
LINE_IN_L
LINE_IN_R
SPK_L
SPK_R
AEC_MIC_L
AEC_MIC_GND
AEC_MIC_R
CVREF
HDA_CODEC_BITCLK
HDA_CODEC_SDATAIN0
HDA_CODEC_SDATAO
HDA_CODEC_RESET#
HDA_CODEC_SYNC
HDA_CODEC_BITCLK
HW_POP_MUTE_CODEC
TO ICH8
ASDATA_IN
CSPDIF
SPDIF_OUT
16V/0805
DVT : delete VREF path to MIC
10mil
(20mil)
From MIC Switch
Place near Codec
NPO
DVT : change to 820P ,NPO ,0603 ,for audio precision test
R682,C723 put near SENSE_A(pin13)
R694,C743 put near SENSE_B(pin34)
SENSE_A
SENSE_B
LINE_IN 52
HP_IN_5 50
EXTMIC_IN 52
DVT remove R279 for delete Line in path
PQ36
2N7002EPT
Near FM2010
near CXD9872R
Int MIC amp circuit
55 AEC_LINE_OUT
AEC_MIC1_R
AEC_MIC1_L
AEC_MIC_R
AEC_MIC_L
AEC_MIC_GND
PVT 5/29 : Add TP for power test
DVT
4.75V/0.2A
U13
AME8824AEEYZ
VIN
VOUT
GND
ADJ
EN
PG
TP216
tp_tpc40t_75
SPDIF OUT
CN21
SPDIF_8P
FOX_2FC9C00-NPSMC-4F
PVT 5/17 change to slow rate type
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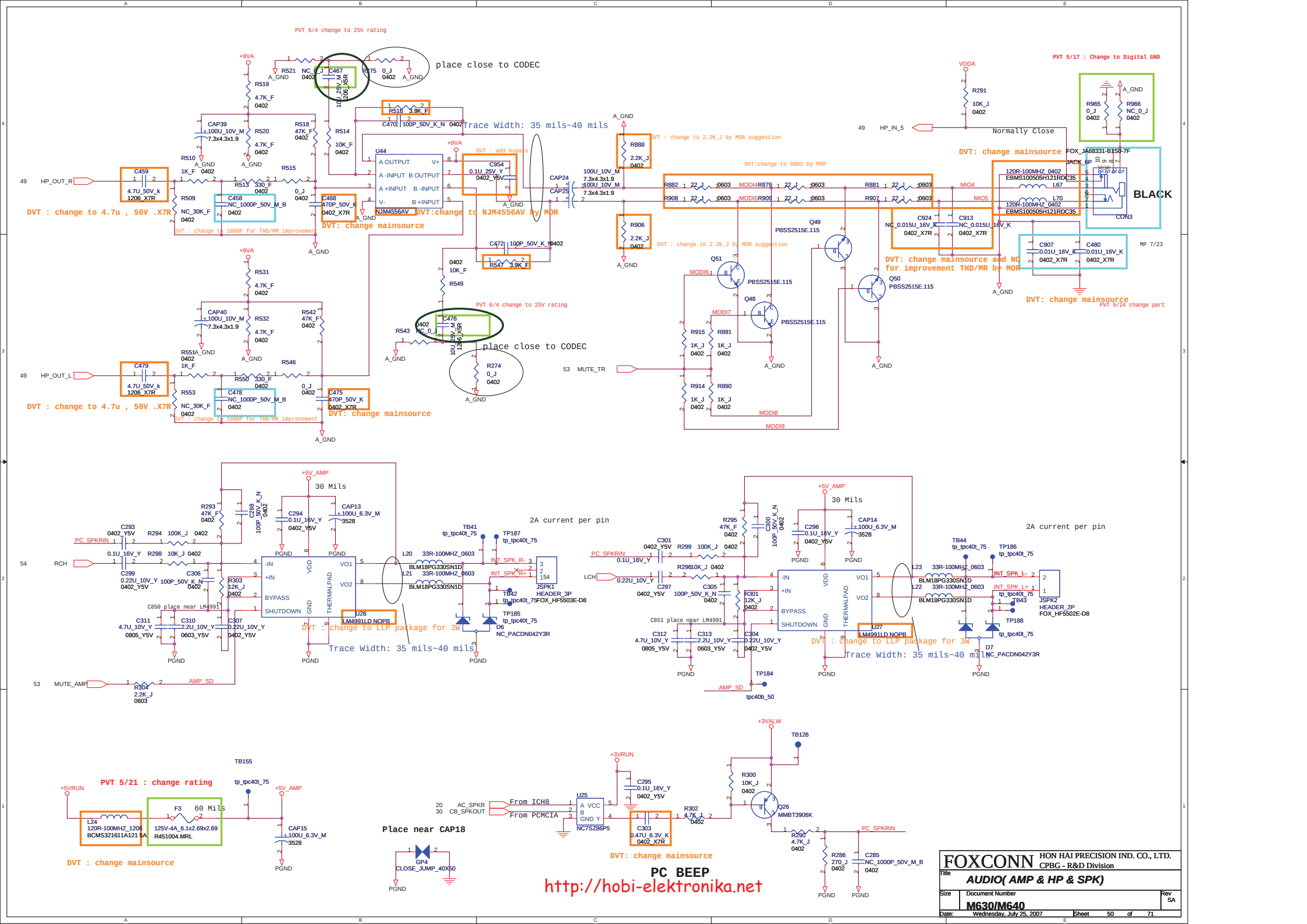
PVT 6/4 change to 25V rating
place close to CODEC
Trace Width: 35 mils~40 mils
DVT : change to 2.2K_J by MOR suggestion
DVT:change to 0603 by MOR
DVT : add bypass
DVT:change to NJM4556AV by MOR
DVT : change to 4.7u , 50V .X7R
DVT : change to 1800P for THD/MR improvement
DVT: change mainsource
DVT : change to 2.2K_J by MOR suggestion
PVT 6/4 change to 25V rating
place close to CODEC
PVT 5/17 : Change to Digital GND
Normally Close
DVT: change mainsource
DVT: change mainsource and NC for improvement THD/MR by MOR
PVT 5/24 change part
30 Mils
2A current per pin
DVT : change to LLP package for 3W
Trace Width: 35 mils~40 mils
PVT 5/21 : change rating
Place near CAP18
PC BEEP
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BLACK
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HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
AUDIO(AMP & HP & SPK)
M630/M640
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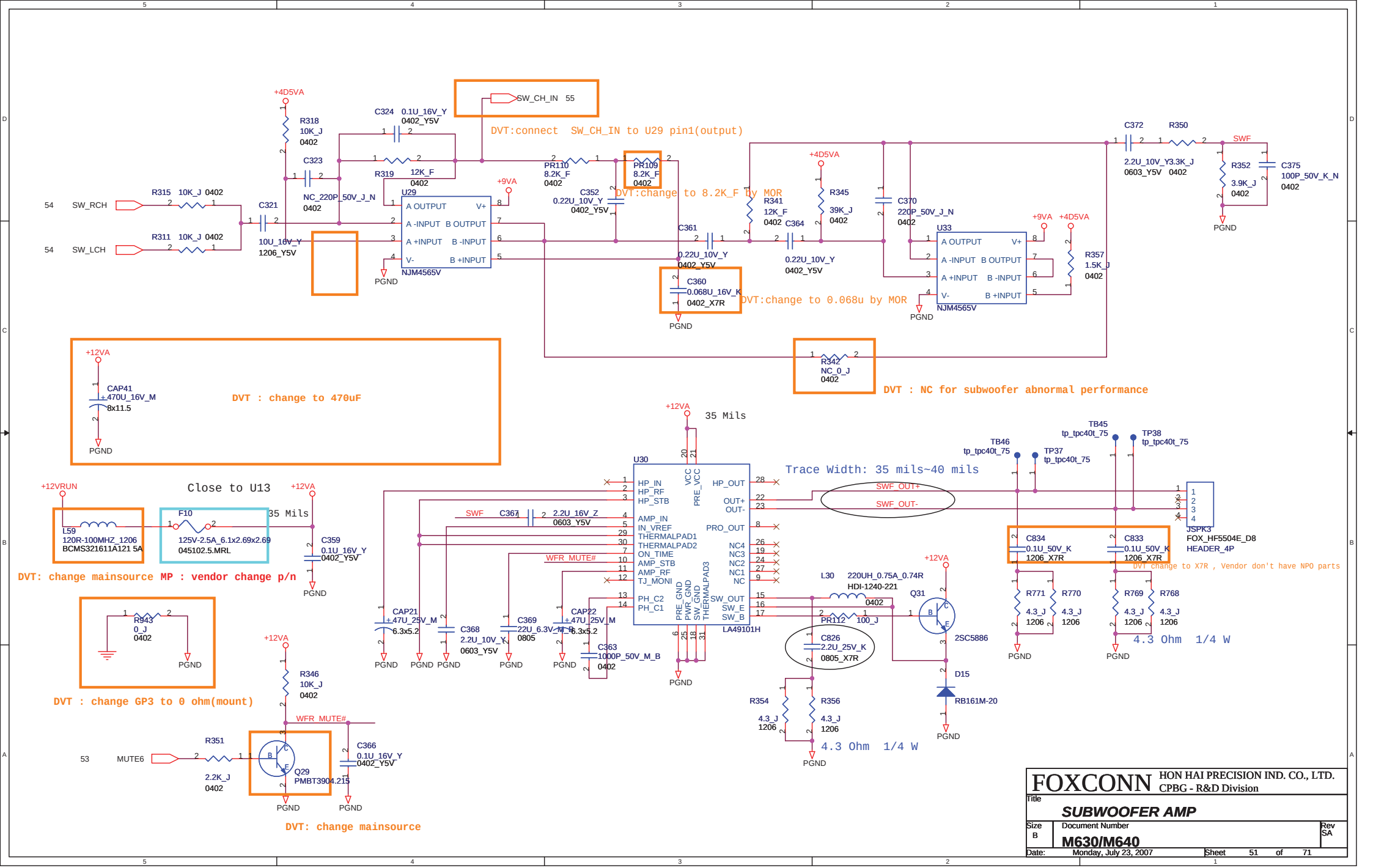
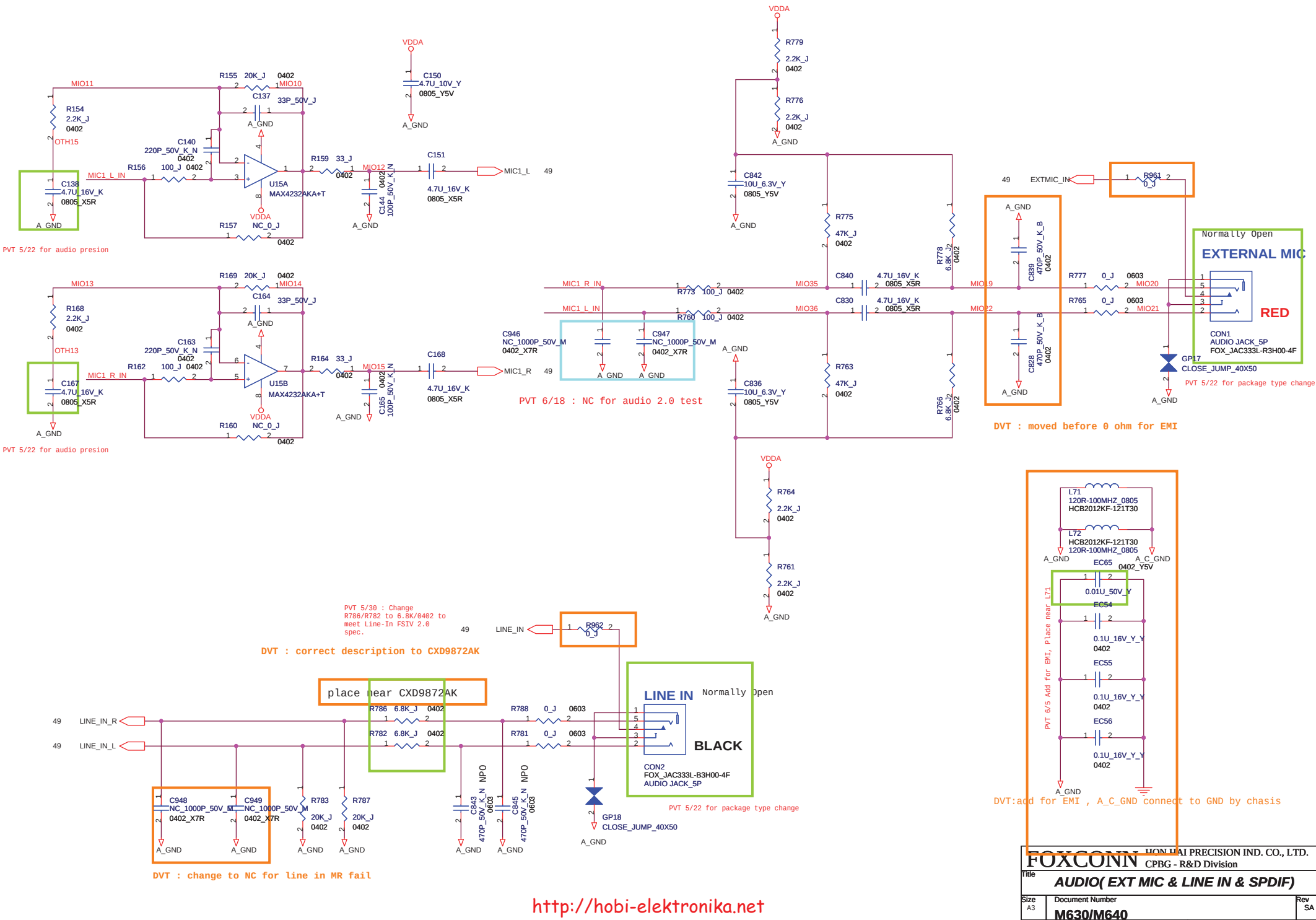
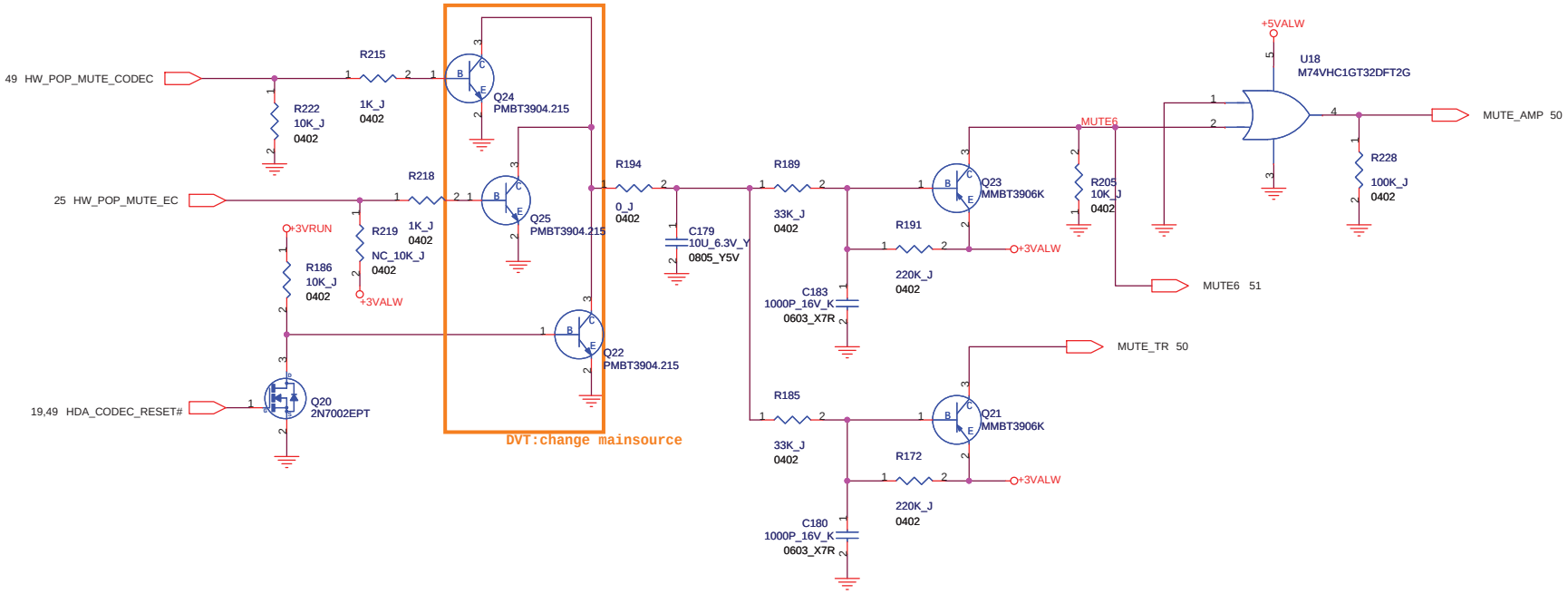
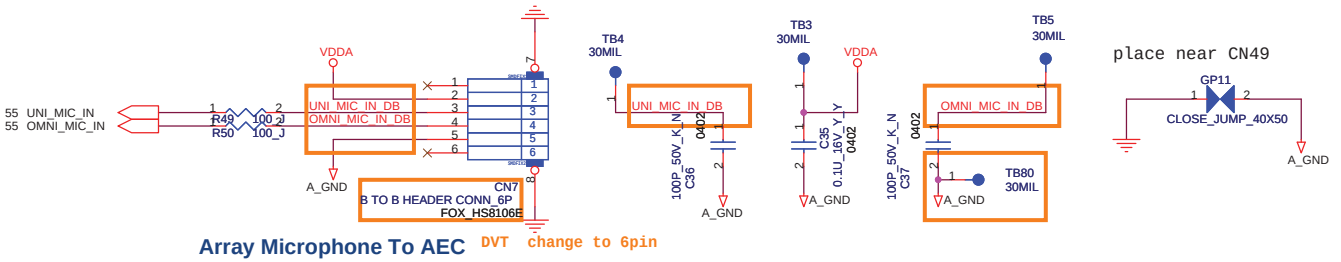



MIO11
R155 20K_J 0402
MIO10
C137 33P_50V_J
R154 2.2K_J 0402
OTH15
C140 220P_50V_K_N 0402
R156 100_J 0402
MIC1_L_IN
C138 4.7U_16V_K 0805_X5R
U15A MAX4232AKA+T
R157 NC_0_J 0402
R159 33_J 0402
MIO12
C144 100P_50V_K_N 0402
C150 4.7U_10V_Y 0805_Y5V
C151 4.7U_16V_K 0805_X5R
MIC1_L 49
A_GND
VDDA
PVT 5/22 for audio presion
MIO13
R169 20K_J 0402
MIO14
C164 33P_50V_J
R168 2.2K_J 0402
OTH13
C163 220P_50V_K_N 0402
R162 100_J 0402
MIC1_R_IN
C167 4.7U_16V_K 0805_X5R
U15B MAX4232AKA+T
R160 NC_0_J 0402
R164 33_J 0402
MIO15
C165 100P_50V_K_N 0402
C168 4.7U_16V_K 0805_X5R
MIC1_R 49
PVT 5/22 for audio presion
R779 2.2K_J 0402
R776 2.2K_J 0402
C842 10U_6.3V_Y 0805_Y5V
R775 47K_J 0402
R778 6.8K_J 0402
MIC1_R_IN
MIC1_L_IN
R773 100_J 0402
R760 100_J 0402
C946 NC_1000P_50V_M 0402_X7R
C947 NC_1000P_50V_M 0402_X7R
MIO35
MIO36
C840 4.7U_16V_K 0805_X5R
C830 4.7U_16V_K 0805_X5R
R763 47K_J 0402
C836 10U_6.3V_Y 0805_Y5V
R766 6.8K_J 0402
MIO19
MIO22
PVT 6/18 : NC for audio 2.0 test
49 EXTMIC_IN
R961 0_J
C839 470P_50V_K_B 0402
C828 470P_50V_K_B 0402
R777 0_J 0603
R765 0_J 0603
MIO20
MIO21
Normally Open
EXTERNAL MIC
RED
CON1
AUDIO JACK_5P
FOX_JAC333L-R3H00-4F
GP17
CLOSE_JUMP_40X50
PVT 5/22 for package type change
DVT : moved before 0 ohm for EMI
R764 2.2K_J 0402
R761 2.2K_J 0402
PVT 5/30 : Change R786/R782 to 6.8K/0402 to meet Line-In FSIV 2.0 spec.
49 LINE_IN
R962 0_J
DVT : correct description to CXD9872AK
place near CXD9872AK
49 LINE_IN_R
49 LINE_IN_L
R786 6.8K_J 0402
R782 6.8K_J 0402
R788 0_J 0603
R781 0_J 0603
LINE IN
Normally Open
BLACK
CON2
FOX_JAC333L-B3H00-4F
AUDIO JACK_5P
C948 NC_1000P_50V_M 0402_X7R
C949 NC_1000P_50V_M 0402_X7R
R783 20K_J 0402
R787 20K_J 0402
C843 470P_50V_K_N 0603
C845 470P_50V_K_N 0603
GP18
CLOSE_JUMP_40X50
PVT 5/22 for package type change
DVT : change to NC for line in MR fail
L71 120R-100MHZ_0805 HCB2012KF-121T30
L72 HCB2012KF-121T30 120R-100MHZ_0805
A_C_GND
EC65 0402_Y5V
0.01U_50V_Y
EC54
0.1U_16V_Y_Y 0402
EC55
EC56
PVT 6/5 Add for EMI, Place near L71
DVT:add for EMI , A_C_GND connect to GND by chasis
http://hobi-elektronika.net
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
AUDIO(EXT MIC & LINE IN & SPDIF)
Size A3
Document Number
M630/M640
Rev SA
Date: Wednesday, July 11, 2007
Sheet 52 of 71

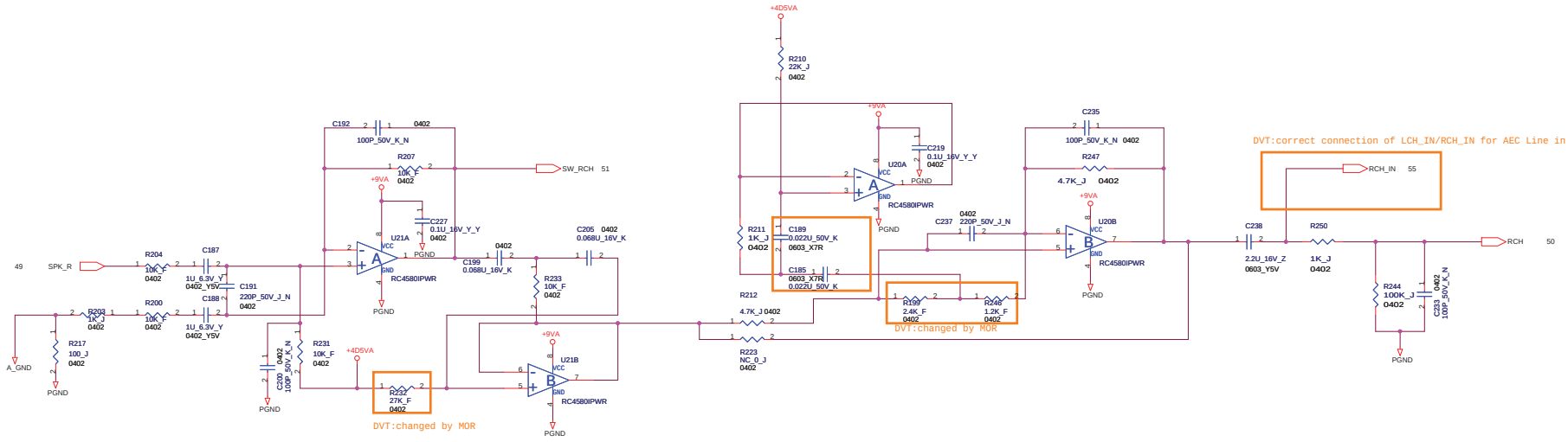


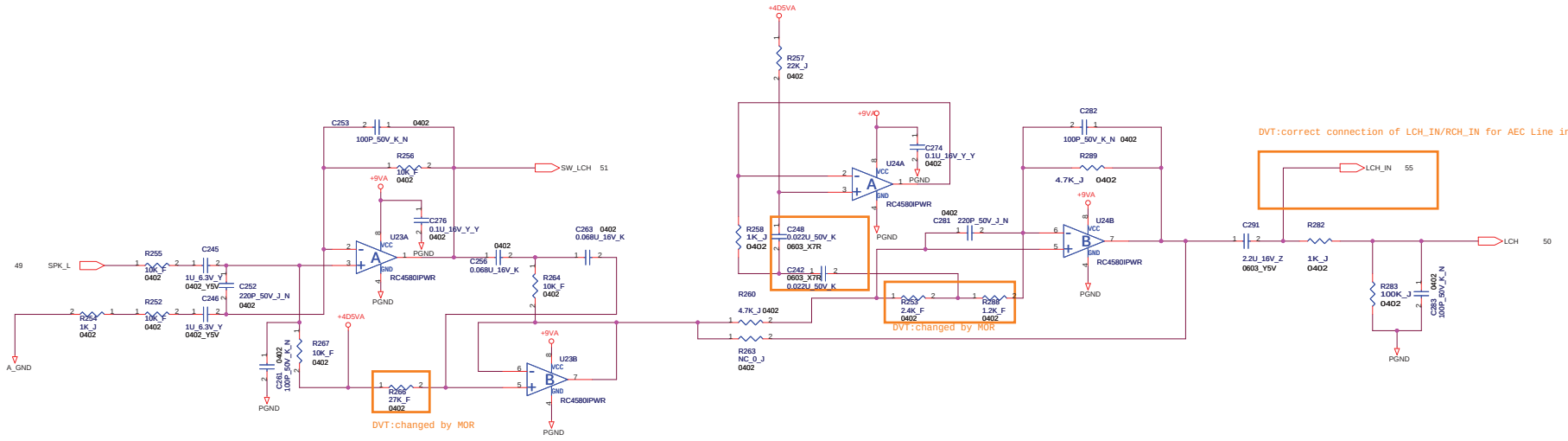


Array Microphone To AEC DVT change to 6pin

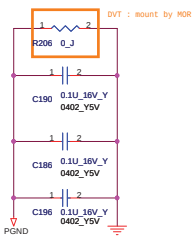
http://hobi-elektronika.net

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: AUDIO (MUTE & INT MIC)		
Size: A3	Document Number: M630/M640	Rev: SA
Date: Wednesday, July 11, 2007	Sheet 53 of 71	



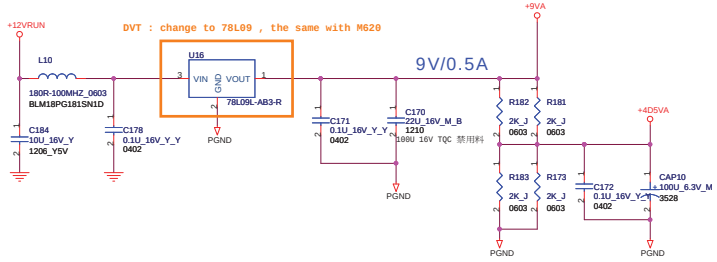


Reserved for EMI

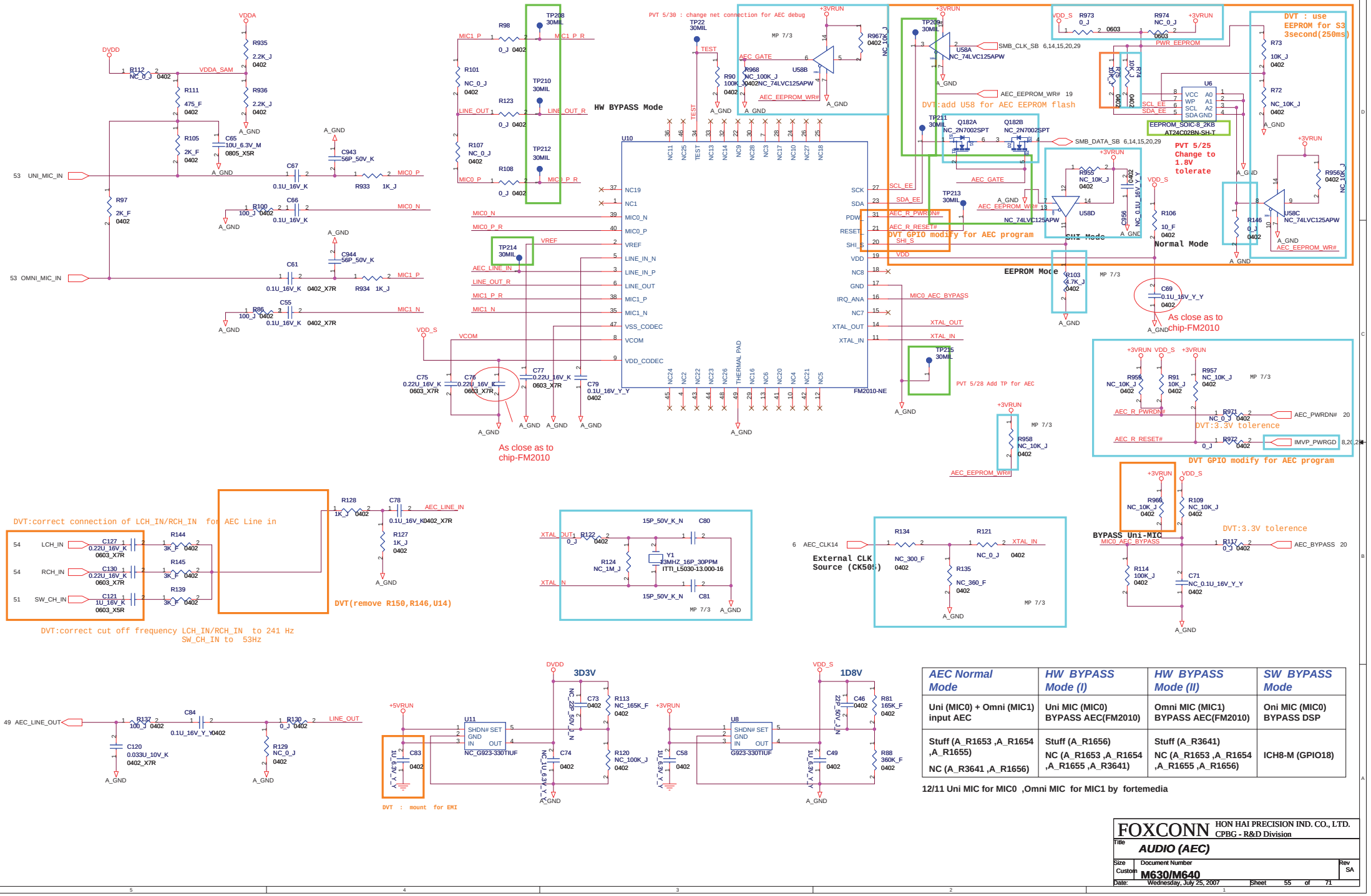


For MIC-IN quality improvement

Do not place near each other & far apart within PGND area.

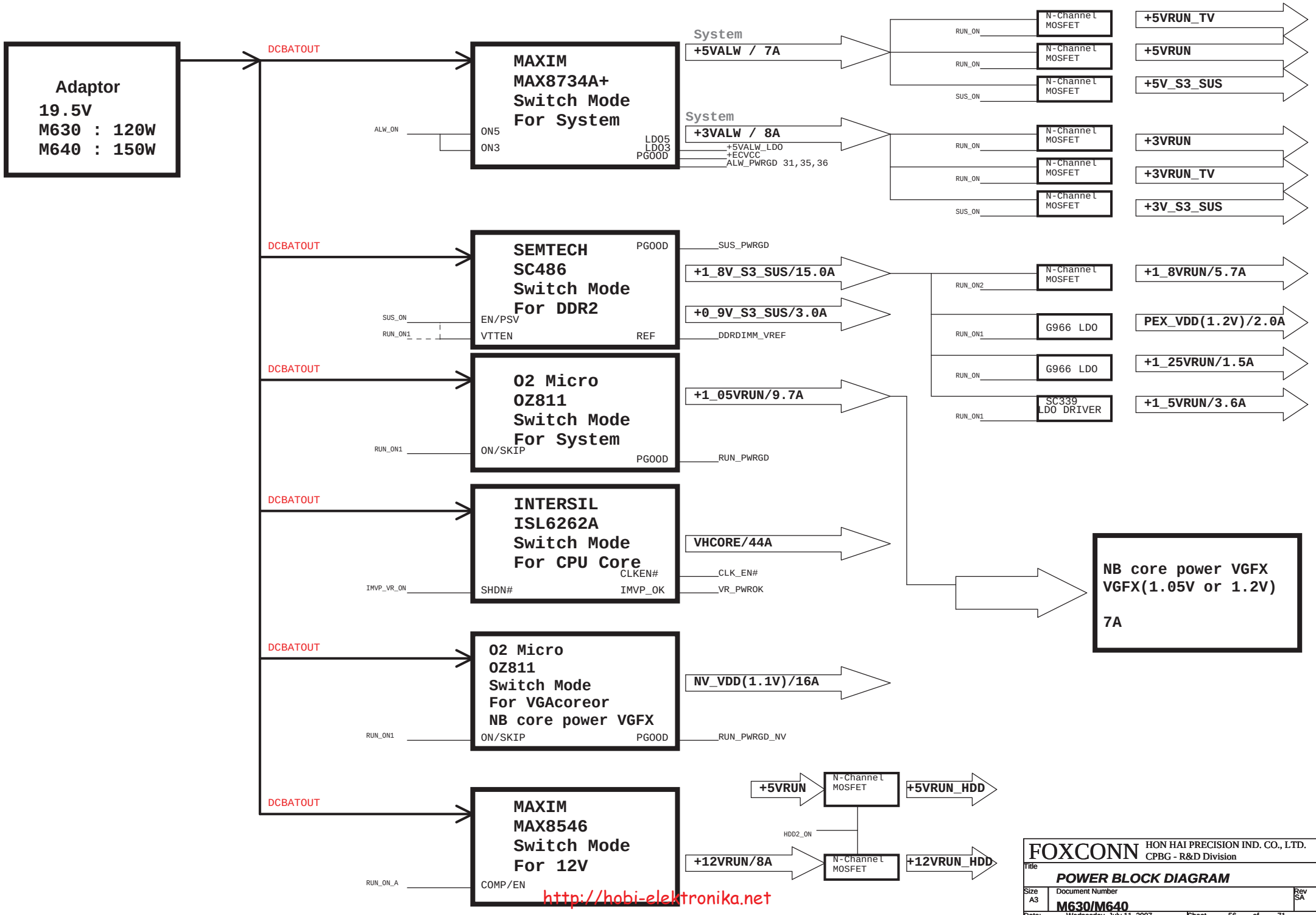


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	AUDIO(EQ)	
Size A2	Document Number M630/M640	Rev SA
Date: Wednesday, July 11, 2007	Sheet 54 of 71	



AEC Normal Mode	HW BYPASS Mode (I)	HW BYPASS Mode (II)	SW BYPASS Mode
Uni (MIC0) + Omni (MIC1) input AEC	Uni MIC (MIC0) BYPASS AEC(FM2010)	Omni MIC (MIC1) BYPASS AEC(FM2010)	Oni MIC (MIC0) BYPASS DSP
Stuff (A_R1653 ,A_R1654 ,A_R1655) NC (A_R3641 ,A_R1656)	Stuff (A_R1656) NC (A_R1653 ,A_R1654 ,A_R1655 ,A_R3641)	Stuff (A_R3641) NC (A_R1653 ,A_R1654 ,A_R1655 ,A_R1656)	ICH8-M (GPIO18)

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	AUDIO (AEC)		
Size: Custom	Document Number: M630/M640		Rev: SA
Date: Wednesday, July 25, 2007	Sheet 55 of 71		

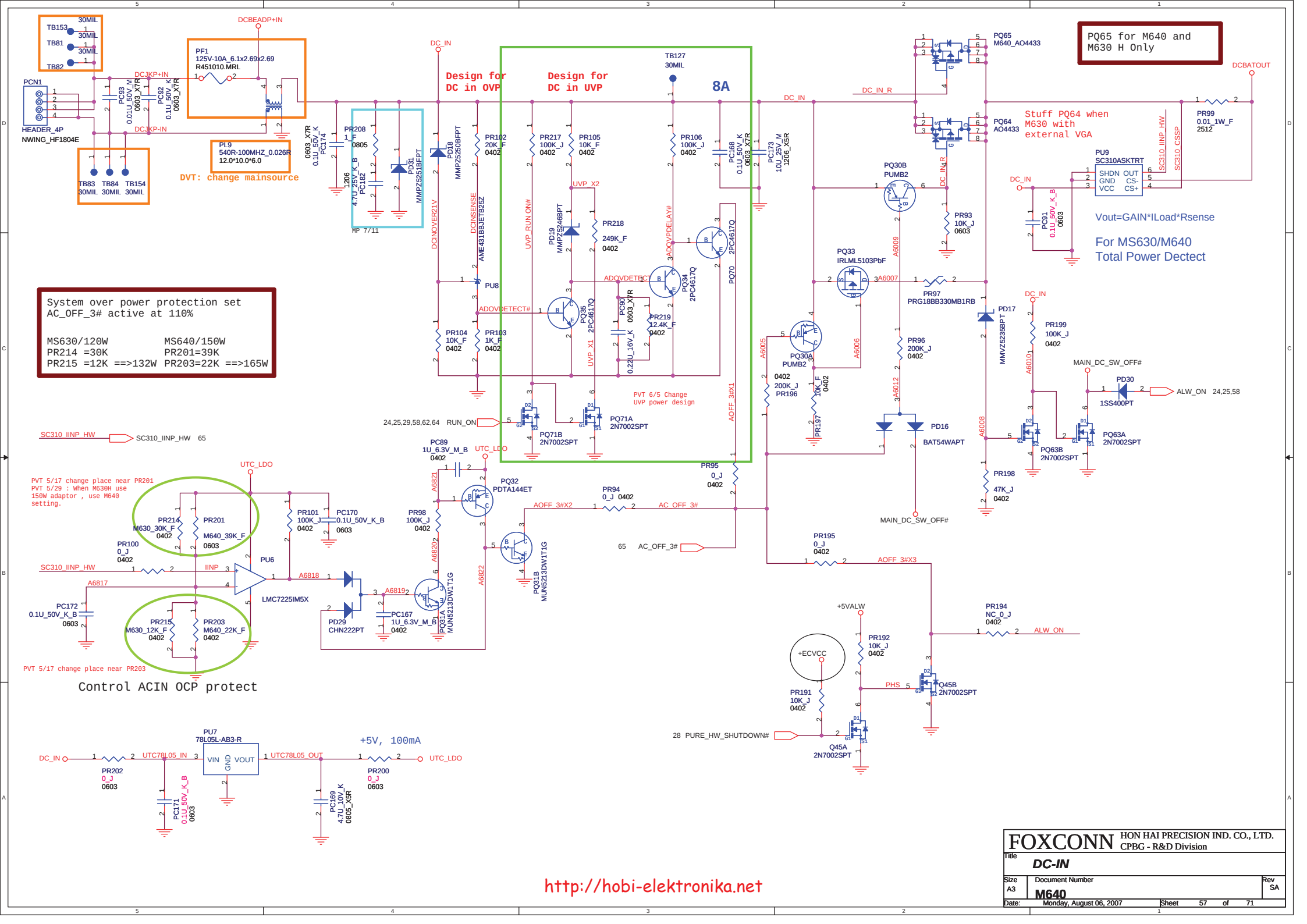


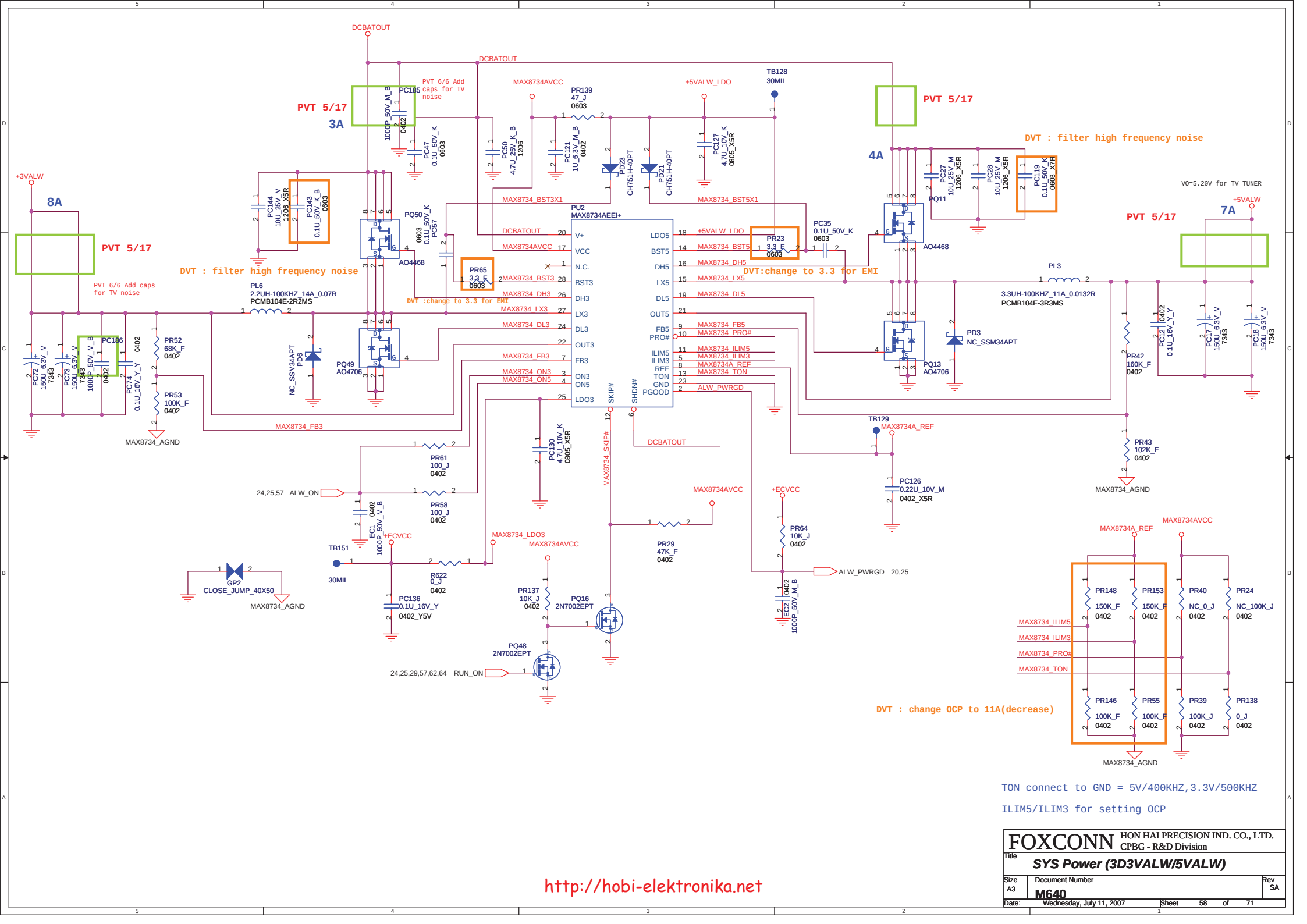
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

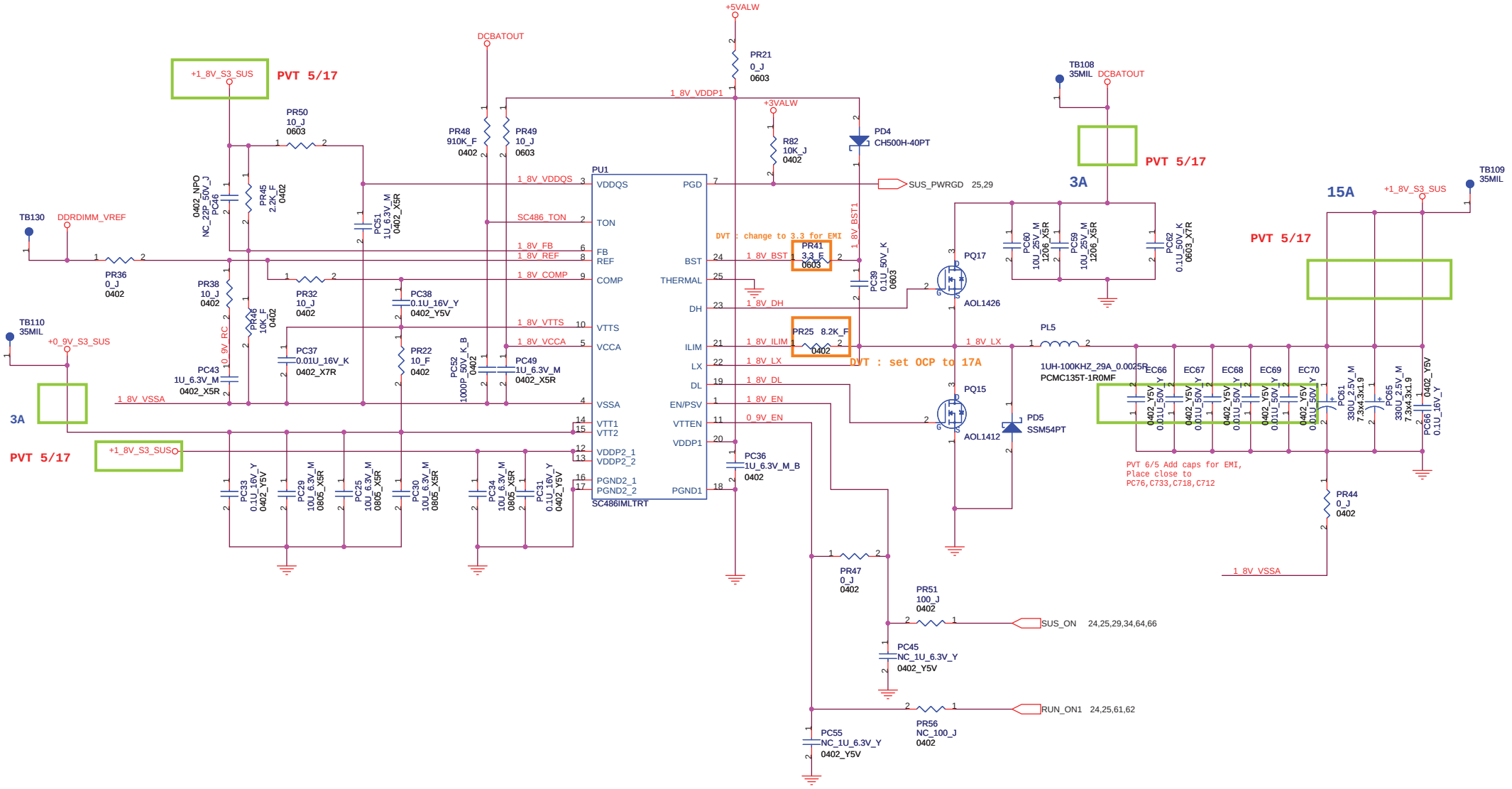
Title: POWER BLOCK DIAGRAM

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 56 of 71

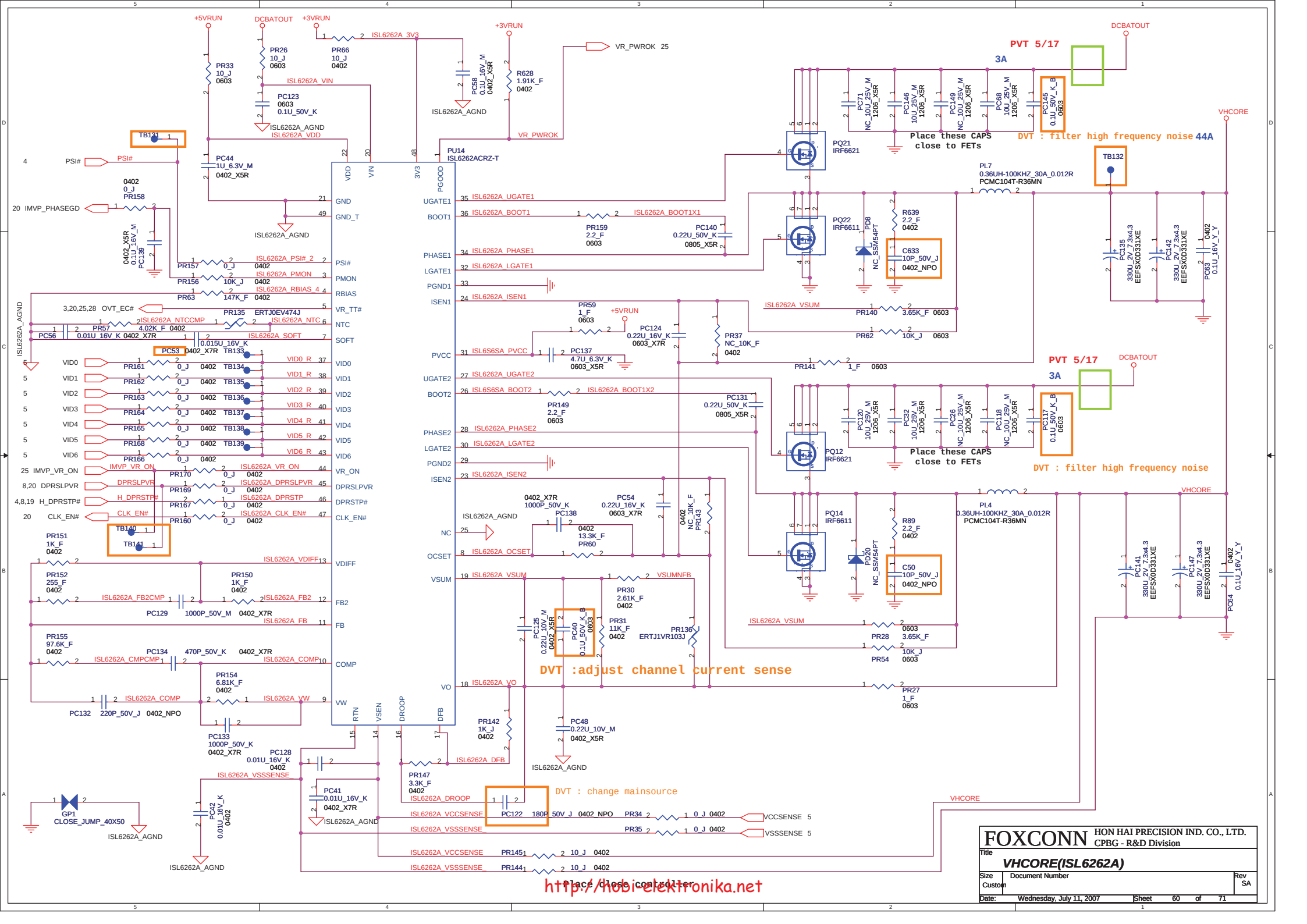

PQ65 for M640 and M630 H Only
Design for DC in OVP
Design for DC in UVP
8A
Stuff PQ64 when M630 with external VGA
Vout=GAIN*ILoad*Rsense
For MS630/M640 Total Power Dectect
System over power protection set
AC_OFF_3# active at 110%
MS630/120W MS640/150W
PR214 =30K PR201=39K
PR215 =12K ==>132W PR203=22K ==>165W
DVT: change mainsource
PVT 6/5 Change UVP power design
PVT 5/17 change place near PR201
PVT 5/29 : When M630H use 150W adaptor , use M640 setting.
PVT 5/17 change place near PR203
Control ACIN OCP protect
+5V, 100mA
http://hobi-elektronika.net
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
DC-IN
M640
Monday, August 06, 2007
Sheet 57 of 71


DCBATOUT
PVT 5/17
3A
PVT 6/6 Add caps for TV noise
MAX8734AVCC
+5VALW_LDO
TB128
30MIL
PR139
47_J
0603
PC185
1000P_50V_M_B
0402
PC47
0.1U_50V_K
0603
PC50
4.7U_25V_K_B
1206
PC121
1U_6.3V_M_B
0402
PD23
CH751H-40PT
PD21
CH751H-40PT
PC127
4.7U_10V_K
0805_X5R
PVT 5/17
4A
DVT : filter high frequency noise
PC27
10U_25V_M
1206_X5R
PC28
10U_25V_M
1206_X5R
PC119
0.1U_50V_K
0603_X7R
PQ11
AO4468
VO=5.20V for TV TUNER
+5VALW
7A
PVT 5/17
+3VALW
8A
PVT 5/17
PC144
10U_25V_M
1206_X5R
PC143
0.1U_50V_K_B
0603
PQ50
0.1U_50V_K
0603
PC57
AO4468
DVT : filter high frequency noise
PR65
3.3_F
0603
DVT :change to 3.3 for EMI
PU2
MAX8734AEEI+
V+
VCC
N.C.
BST3
DH3
LX3
DL3
OUT3
FB3
ON3
ON5
LDO3
LDO5
BST5
DH5
LX5
DL5
OUT5
FB5
PRO#
ILIM5
ILIM3
REF
TON
GND
PGOOD
SKIP#
SHDN#
+5VALW_LDO
MAX8734_BST5
MAX8734_DH5
MAX8734_LX5
MAX8734_DL5
MAX8734_FB5
MAX8734_PRO#
MAX8734_ILIM5
MAX8734_ILIM3
MAX8734A_REF
MAX8734_TON
ALW_PWRGD
PR23
3.3_F
0603
PC35
0.1U_50V_K
0603
DVT:change to 3.3 for EMI
PL3
3.3UH-100KHZ_11A_0.0132R
PCMB104E-3R3MS
PL6
2.2UH-100KHZ_14A_0.07R
PCMB104E-2R2MS
PC186
PR52
68K_F
0402
PR53
100K_F
0402
MAX8734_AGND
NC_SSM34APT
PD6
PQ49
AO4706
PD3
NC_SSM34APT
PQ13
AO4706
PR42
160K_F
0402
PC12
0.1U_16V_Y
PC17
150U_6.3V_M
7343
PC18
150U_6.3V_M
7343
PC72
150U_6.3V_M
7343
PC73
150U_6.3V_M
7343
PC74
0.1U_16V_Y
MAX8734_FB3
TB129
MAX8734A_REF
PR43
102K_F
0402
PC126
0.22U_10V_M
0402_X5R
PC130
4.7U_10V_K
0805_X5R
MAX8734_SKIP#
DCBATOUT
24,25,57 ALW_ON
PR61
100_J
0402
PR58
100_J
0402
EC1
1000P_50V_M_B
0402
+ECVCC
MAX8734_LDO3
MAX8734AVCC
TB151
30MIL
R622
0_J
0402
PC136
0.1U_16V
0402_Y5V
PR29
47K_F
0402
PR64
10K_J
0402
ALW_PWRGD 20,25
EC2
1000P_50V_M_B
0402
PR137
10K_J
0402
PQ16
2N7002EPT
PQ48
2N7002EPT
24,25,29,57,62,64 RUN_ON
GP2
CLOSE_JUMP_40X50
MAX8734_AGND
PR148
150K_F
0402
PR153
150K_F
0402
PR40
NC_0_J
0402
PR24
NC_100K_J
0402
MAX8734_ILIM5
MAX8734_ILIM3
MAX8734_PRO#
MAX8734_TON
PR146
100K_F
0402
PR55
100K_F
0402
PR39
100K_J
0402
PR138
0_J
0402
DVT : change OCP to 11A(decrease)
TON connect to GND = 5V/400KHZ,3.3V/500KHZ
ILIM5/ILIM3 for setting OCP
http://hobi-elektronika.net
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
SYS Power (3D3VALW/5VALW)
Size A3
Document Number
M640
Rev SA
Date: Wednesday, July 11, 2007
Sheet 58 of 71



http://hobi-elektronika.net

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	DDR2Power(+1_8V_S3_SUS/+0_9VRUN)	
Size A3	Document Number M640	Rev SA
Date: Wednesday, July 11, 2007	Sheet 59 of 71	


PU14
ISL6262ACRZ-T
PVT 5/17
3A
DVT : filter high frequency noise
Place these CAPS close to FETs
DVT :adjust channel current sense
DVT : change mainsource
Place close controller
http://hobi-elektronika.net
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
VHCORE(ISL6262A)
Wednesday, July 11, 2007
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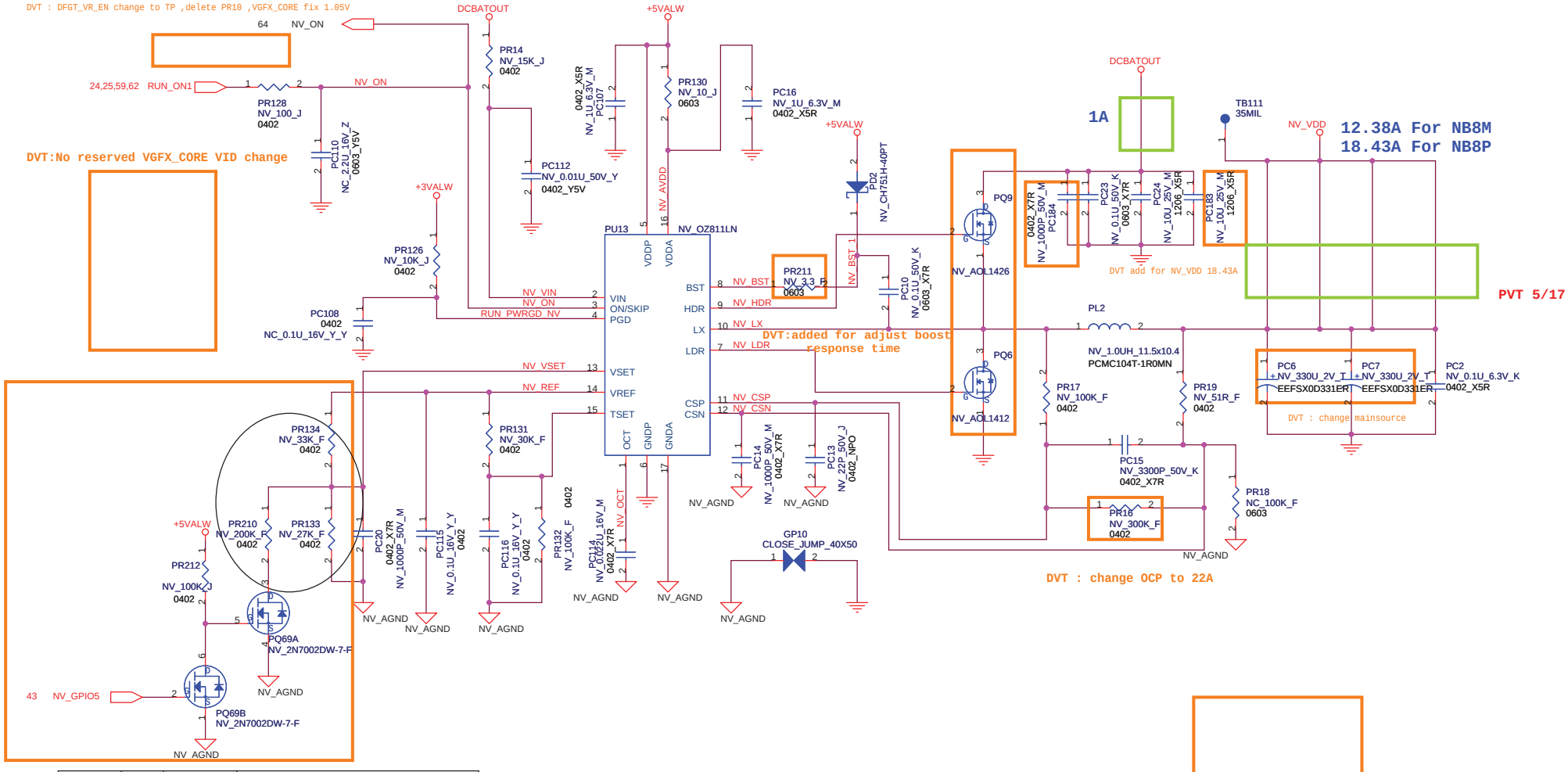
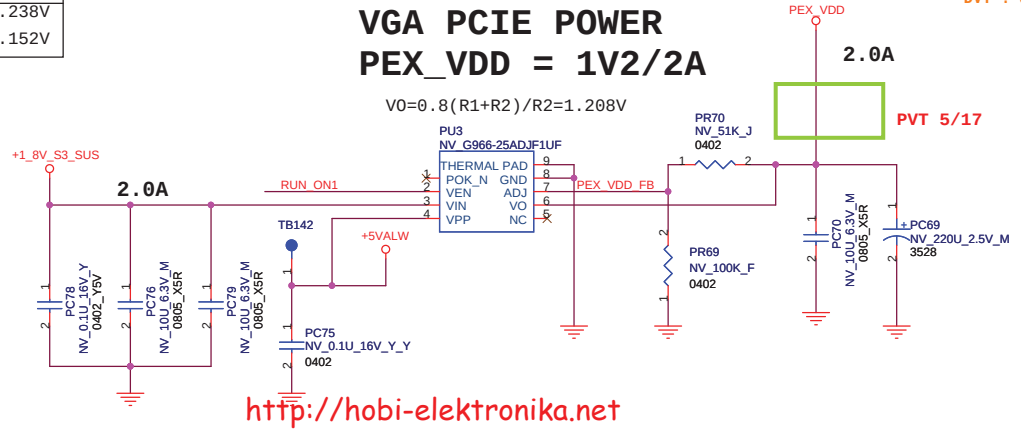


	I/O	Inter pull low	GPIO TABLE
GPIO5	O	Yes	GPU Voltage H: NVDD=1.238V GPU Voltage L: NVDD=1.152V

VGA PCIE POWER
PEX_VDD = 1V2/2A

VO=0.8(R1+R2)/R2=1.208V

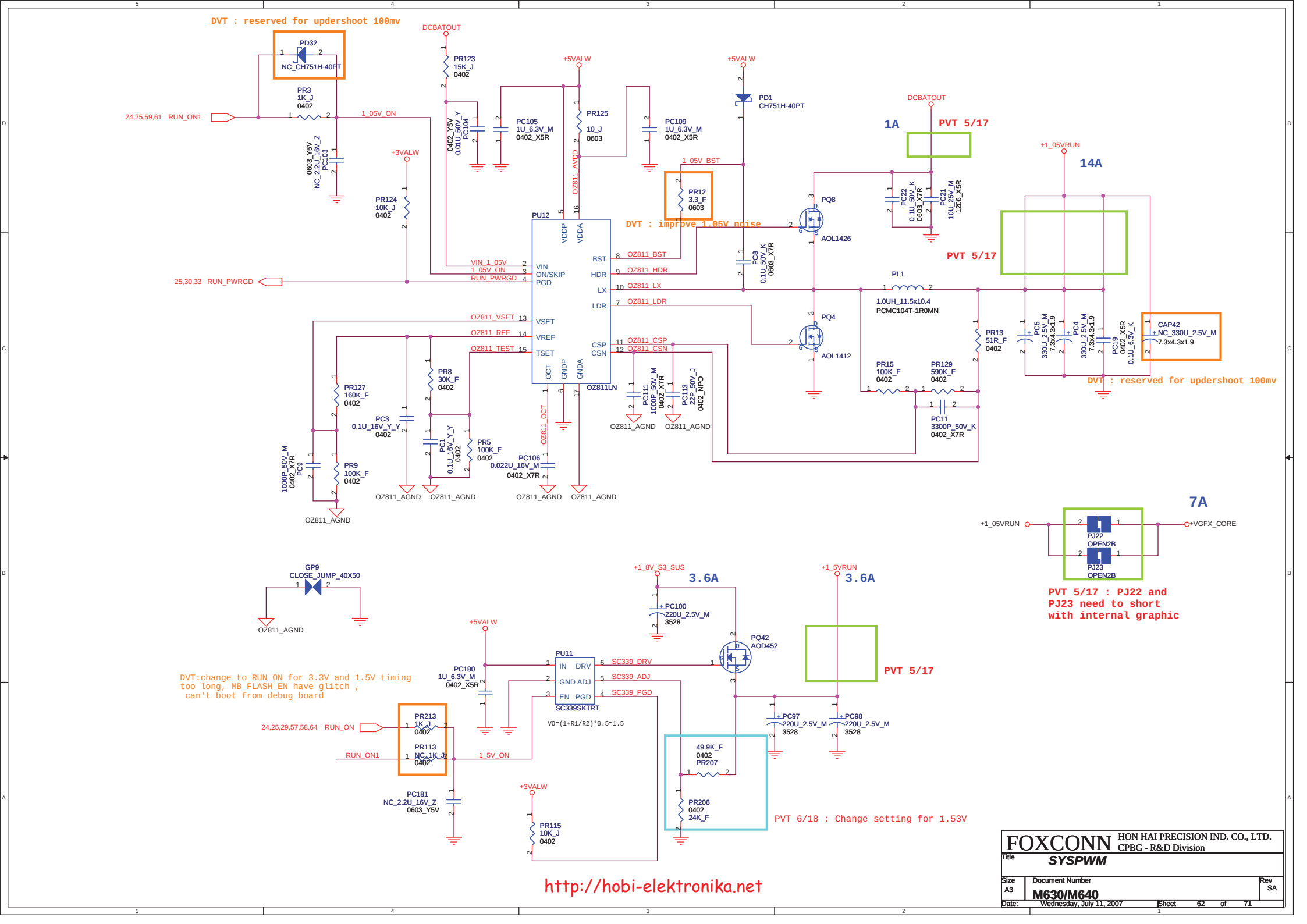


FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA POWER(GMCH)

Size: A3 | Document Number: M630/M640 | Rev: SA

Date: Wednesday, July 11, 2007 | Sheet 61 of 71


DVT : reserved for updershoot 100mv
PD32
NC_CH751H-40PT
DCBATOUT
PR123
15K_J
0402
PR3
1K_J
0402
24,25,59,61 RUN_ON1
1_05V_ON
+5VALW
PC105
1U_6.3V_M
0402_X5R
PC109
1U_6.3V_M
0402_X5R
PR125
10_J
0603
PD1
CH751H-40PT
1_05V_BST
PR12
3.3_F
0603
PQ8
AOL1426
PC22
0.1U_50V_K
0603_X7R
PC21
10U_25V_M
1206_X5R
1A
PVT 5/17
+1_05VRUN
14A
PVT 5/17
+3VALW
PR124
10K_J
0402
PU12
DVT : improve 1.05V noise
VDDP
VDDA
OZ811_AVDD
VIN_1_05V
1_05V_ON
RUN_PWRGD
25,30,33 RUN_PWRGD
VIN
ON/SKIP
PGD
BST
HDR
LX
LDR
OZ811_BST
OZ811_HDR
OZ811_LX
OZ811_LDR
PC8
0.1U_50V_K
0603_X7R
PL1
1.0UH_11.5x10.4
PCMC104T-1R0MN
PQ4
AOL1412
OZ811_VSET
OZ811_REF
OZ811_TEST
VSET
VREF
TSET
CSP
CSN
OZ811_CSP
OZ811_CSN
OCT
GNDP
GNDA
OZ811LN
PR127
160K_F
0402
PR8
30K_F
0402
PC3
0.1U_16V_Y_Y
0402
PC1
0.1U_16V_Y_Y
0402
PR5
100K_F
0402
PR9
100K_F
0402
PC9
1000P_50V_M
0402_X7R
PC106
0.022U_16V_M
0402_X7R
PC111
1000P_50V_M
0402_X7R
PC113
22P_50V_J
0402_NPO
PR15
100K_F
0402
PR129
590K_F
0402
PR13
51R_F
0402
PC11
3300P_50V_K
0402_X7R
PC5
330U_2.5V_M
7.3x4.3x1.9
PC4
330U_2.5V_M
7.3x4.3x1.9
PC19
0402_X5R
0.1U_6.3V_K
CAP42
NC_330U_2.5V_M
7.3x4.3x1.9
DVT : reserved for updershoot 100mv
OZ811_AGND
7A
+1_05VRUN
PJ22
OPEN2B
PJ23
OPEN2B
+VGFX_CORE
PVT 5/17 : PJ22 and
PJ23 need to short
with internal graphic
GP9
CLOSE_JUMP_40X50
+1_8V_S3_SUS
3.6A
+1_5VRUN
3.6A
PC100
220U_2.5V_M
3528
PQ42
AOD452
PVT 5/17
PU11
IN DRV
GND ADJ
EN PGD
SC339_DRV
SC339_ADJ
SC339_PGD
SC339SKTRT
V0=(1+R1/R2)*0.5=1.5
PC180
1U_6.3V_M
0402_X5R
DVT:change to RUN_ON for 3.3V and 1.5V timing
too long, MB_FLASH_EN have glitch ,
can't boot from debug board
24,25,29,57,58,64 RUN_ON
RUN_ON1
PR213
1K_J
0402
PR113
NC_1K_J2
0402
1_5V_ON
PC97
220U_2.5V_M
3528
PC98
220U_2.5V_M
3528
49.9K_F
0402
PR207
PR206
0402
24K_F
PVT 6/18 : Change setting for 1.53V
PC181
NC_2.2U_16V_Z
0603_Y5V
PR115
10K_J
0402
http://hobi-elektronika.net
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
SYSPWM
Size
A3
Document Number
M630/M640
Rev
SA
Date:
Wednesday, July 11, 2007
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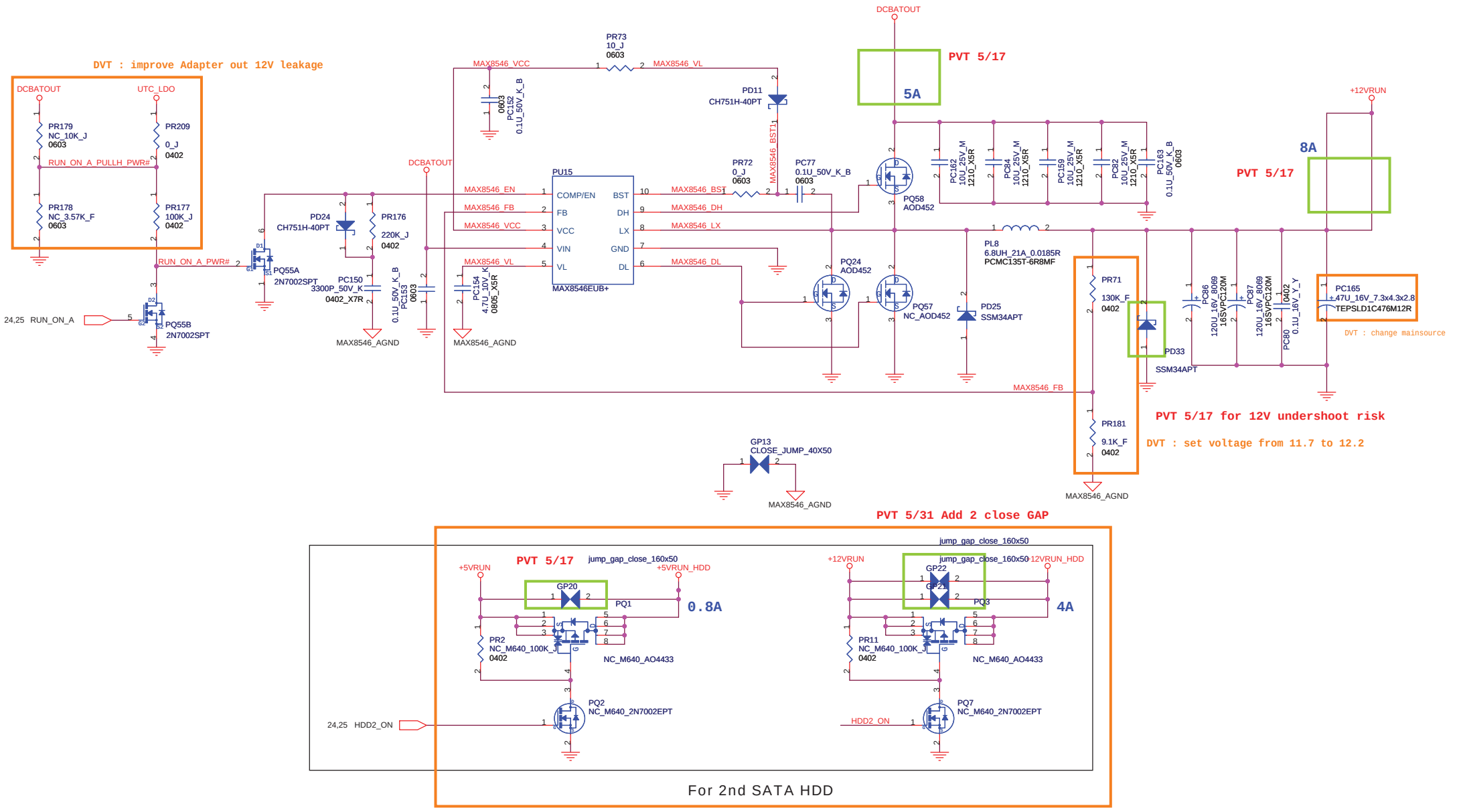
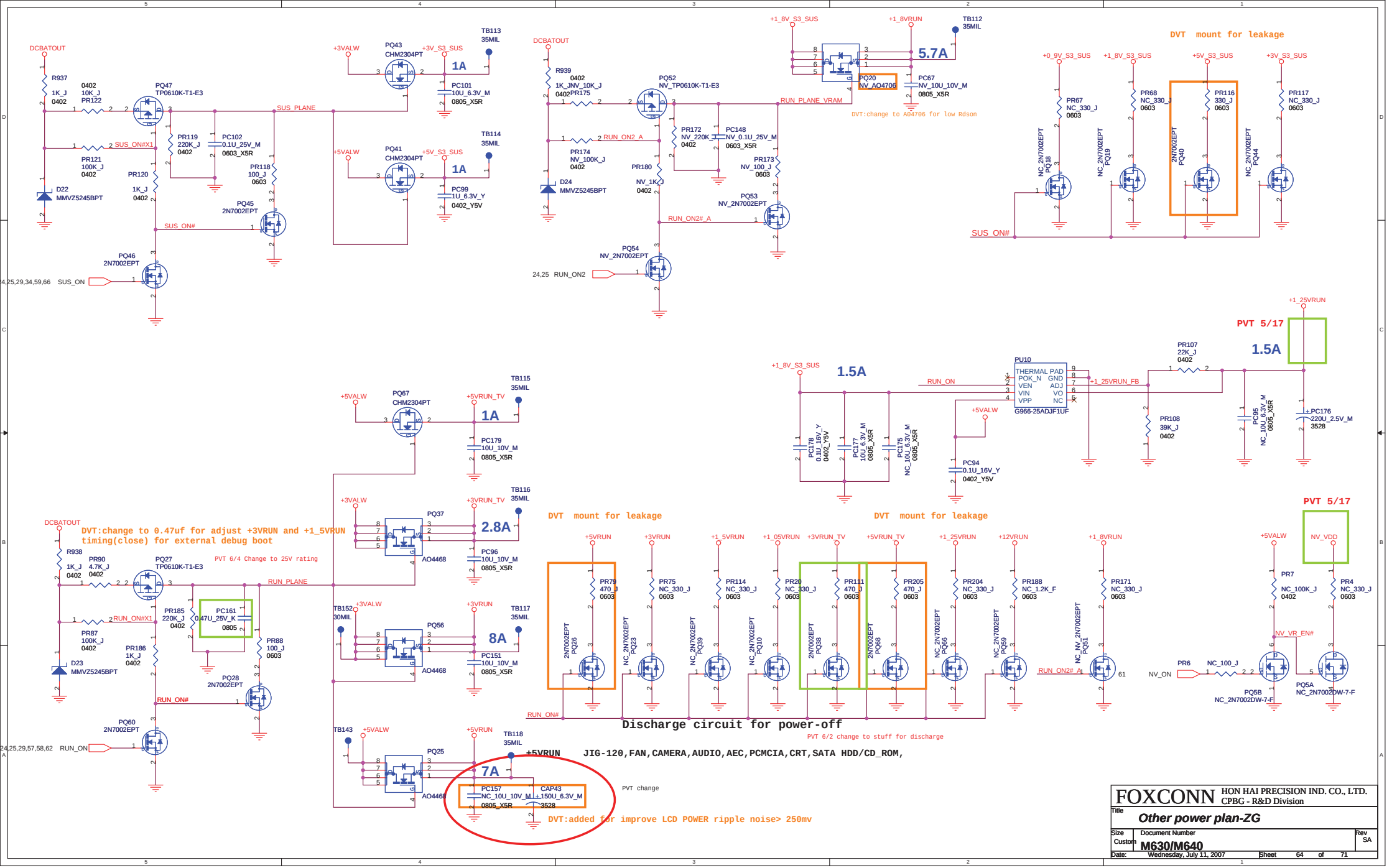
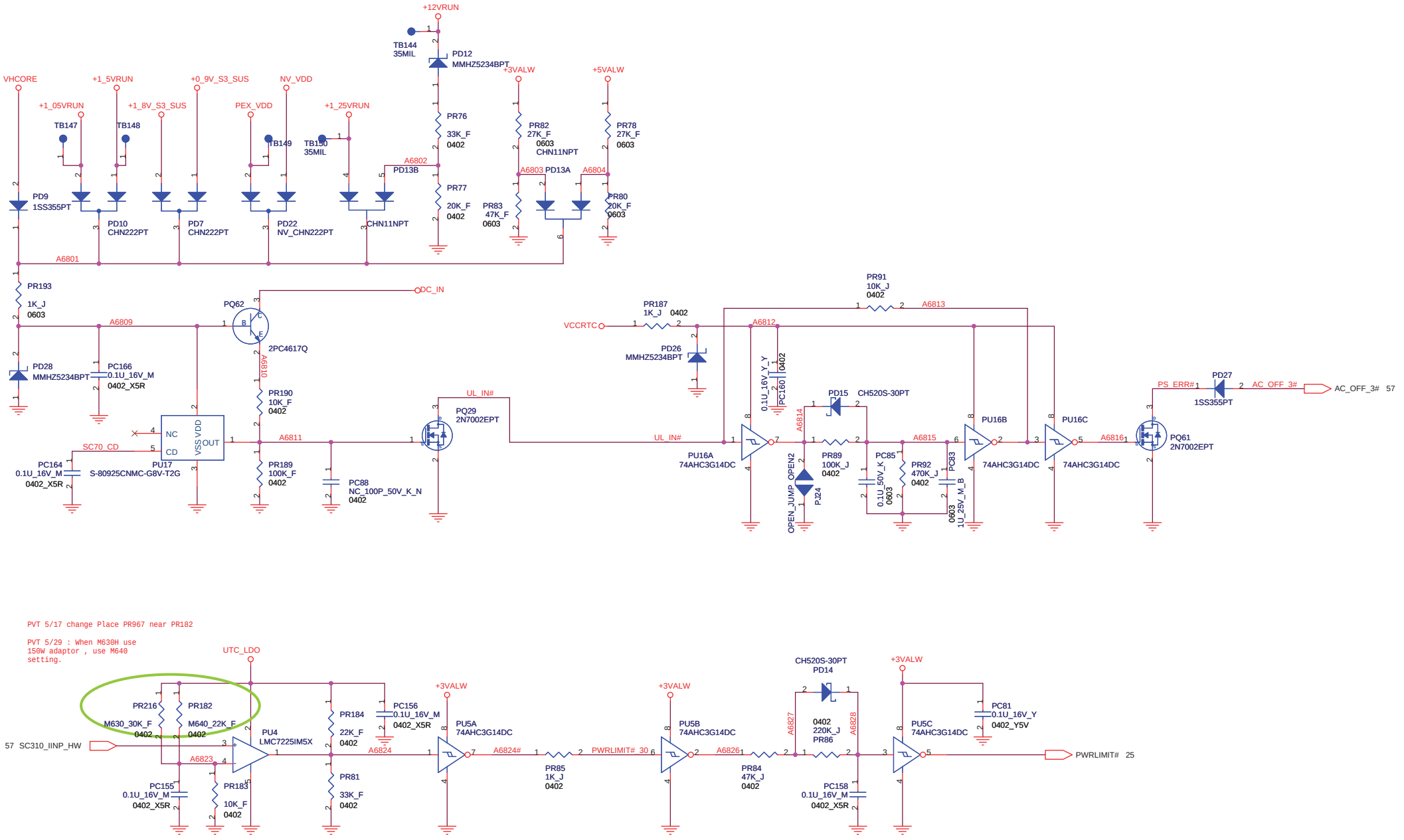


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	+12VRUN POWER(MAX8546)
Size A3	Document Number M630/M640
Rev	SB
Date:	Wednesday, July 11, 2007
Sheet	63 of 71



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title	Other power plan-ZG	
Size: Custom	Document Number: M630/M640	Rev: SA
Date: Wednesday, July 11, 2007	Sheet 64 of 71	



PWLIMIT
System power saving mode set
PWLIMIT active at 95%

MS630	120W	MS640
PR216	=30K	PR182=22K
PR183	=10K ==>114W	PR183=10K ==>140W

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FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	OVP protection-ZG	
Size A3	Document Number M630/M640	Rev SA
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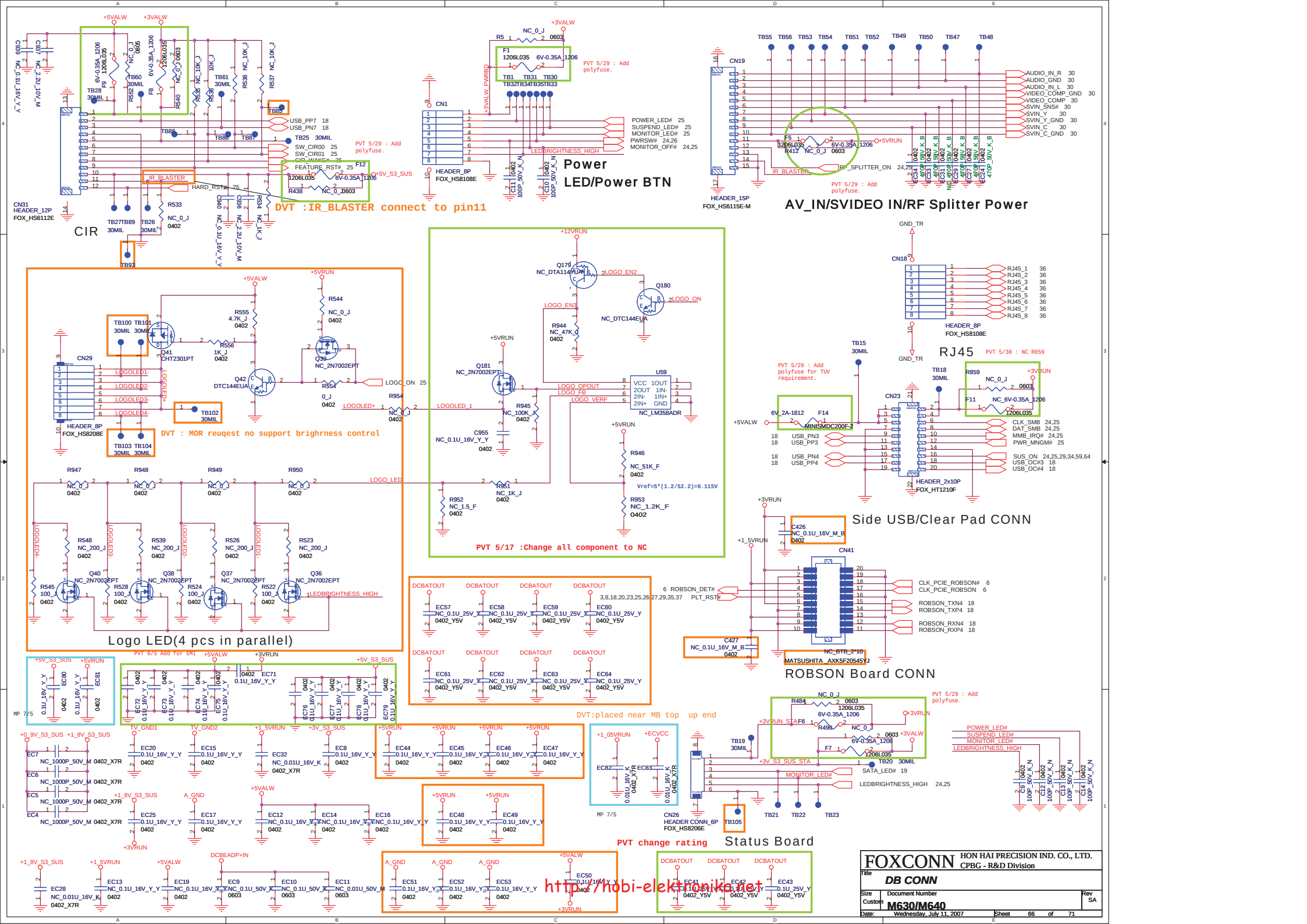

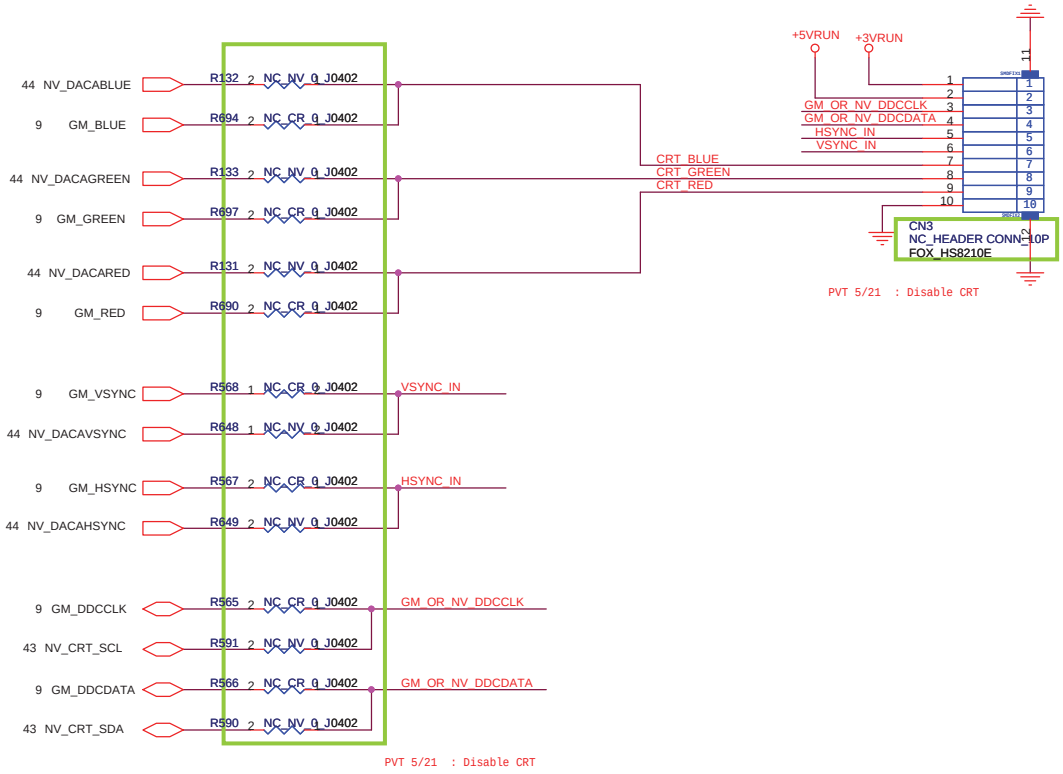

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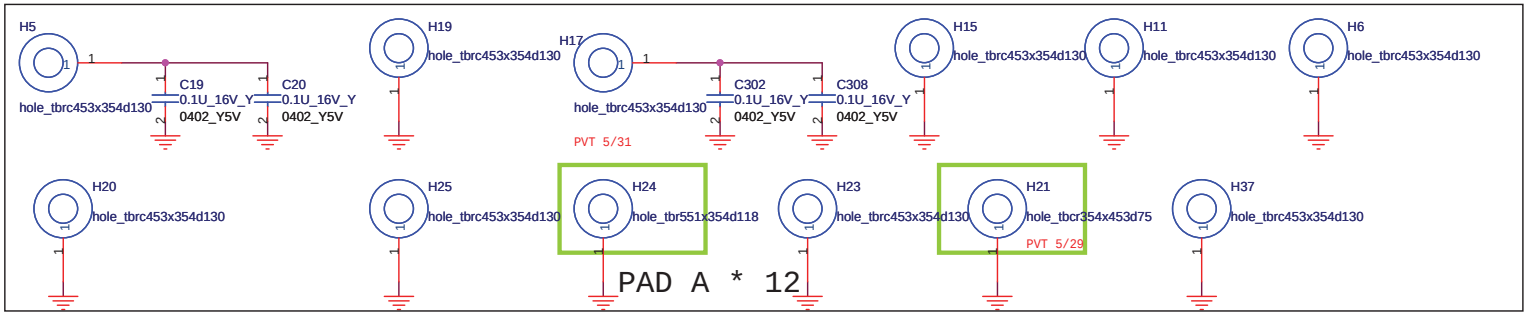
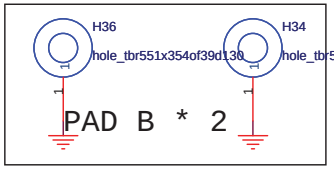
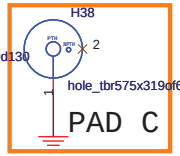
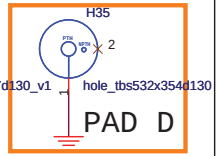
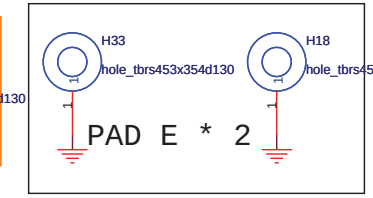
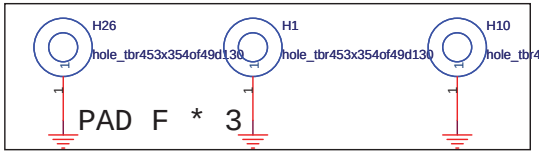


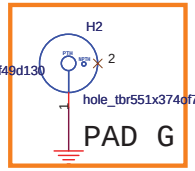


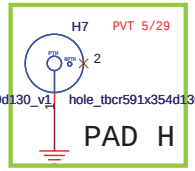


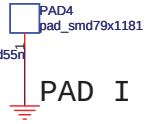


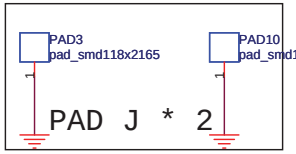




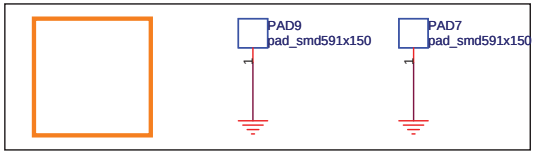


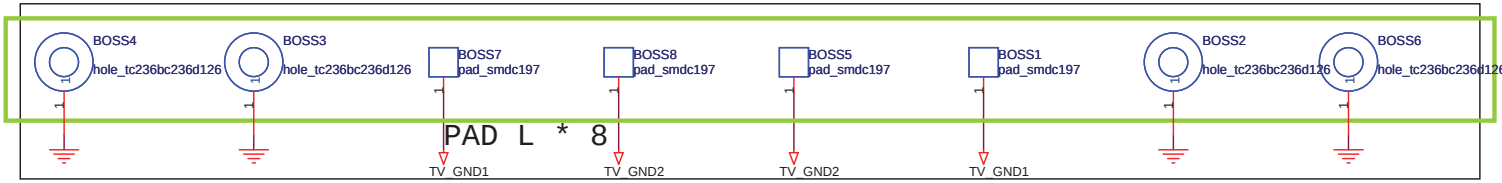


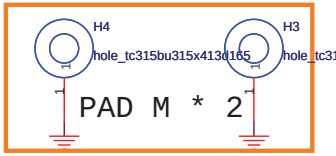


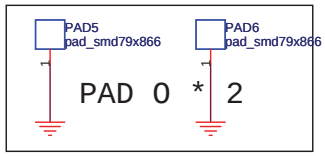


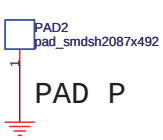
PVT 5/23 : change reference to BOSS

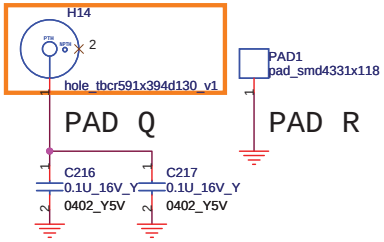


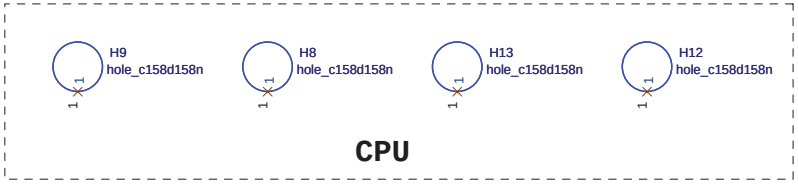












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12/15
Change VRAM from " K4J55323QG-BC20" to "K4J52324QE-BC14 "

12/16
Add R3720
Update Library of CN30,CN31,CN26

12/18
Update screw hole/pad
Add R3721 NC_0 ohm
Change P/N of JSPK3 to HF5504 for current rating
Add R3722~3724 for EMI
NC RP1 (Default use Winbond EC)
Change U22/U23/U26 to G545 for safety certification
Add C3680~3685 for EMI
Remove R2007 resistor.
N.C. R2017
Delete R1994, L83, L84, L85, C1634, C1640, C1647.
Update symbol & footprint of CN41(SPDIF)
Update Ex-GFX Configuration on P.38

12/19
Back-annotation 08:24AM
Change R522,R523,R524,R526,R528,R539,R545,R548 to 200 ohm
Add Q178,R919,Q177,R920 for WoWLAN on S4 support.
Delete Q33, R438 for not supporting half brightness control of WLAN LED
Change R428 value to 68 ohm for brightness adjustment
N.C. R872, STUFF R873
N.C. R457, STUFF R453
N.C. R462, STUFF R461

12/20
Re-assign GPIO pin of EC
N.C. R535
Delete L33,R371,R436
Add R438,R928,R929,R930,R931
N.C. C325,C365
Add C936~940

12/21
1.@p23CAP1,CAP34 change to 47uF16V 1C-44T0476-M300
2.@p51CAP16,CAP17,CAP18,CAP19,CAP20 change to 47uF16V 1C-44T0476-M300
3.@p63PC165 change to 47uF16V 1C-44T0476-M300
4.@p59PQ17 change to AOL1426 17-A0L1426-0000
5.@p59PQ15 change to AOL1412 17-A0L1412-0000
6.@p62PQ8 change to AOL1426 17-A0L1426-0000
7.@p59PQ4 change to AOL1412 17-A0L1412-0000
8.@p57PQ64,PQ65 change to AO4433
9.@P63PQ1,PQ3 change to AO4433
10.@p58PQ11,PQ50 change to AO4468 17-A0L4468-0000
11.@p61PQ9change to AO4468 17-A0L4468-0000
12.@p64PQ20,PQ25,PQ37,PQ56 change to AO4468 17-A0L4468-0000

12/21
Delete R492,R876
Delete net "VDDA_M". Add R935,R936
Change PURE_HW_SHUTDOWN# pull high power from +5VALW to +ECVCC(PR191)
Add PR208,PC182,PD31
Add R492 for LEDBRIGHTNESS_HIGH pull down
Change Q178 to PMV65XP for lower Rds(on) and voltage ripple

12/22
N.C. R815,EC31
Add Net "USB_VCC0_R", "USB_VCC1_R","USB_VCC2_R" for USB connector
Change CAP16~20 value to 68uF
Change PJ33 to larger pad open jump
Add PJ35 for higher current requirement for NB8P

12/23
Change H16 net to TV_GND2, H30 to TV_GND1
Add R937,R938,R939,D22,D23,D24 to prevent 2N7002 from damage if DC_IN is over 20V
N.C. KB3910SFC1 to create BOM for factory (Winbond will be used in EVT by default)

12/25
P.41,P.42,P56,P.61 Change description of current (Ampere) requriement for NV_VDD & FBVDDQ
Connect H21, H37 to GND
Delet EC23,EC8,EC22,EC30,EC26,EC21
Add C946~949 for vista requirement
Change VGA Straping resistors to set NB8M-GT, Qimonda 256MB as default
Add net THERMTRIP_GFX#_R to KB3910S

12/26
N.C. R521,R543
Mount R274,R275

12/27
N.C. All Winbond EC parts
N.C. RP38
Update SYSTEM_ID Table

12/28
N.C. C749
Add prefix NV_ FOR R572
Delete prefix NV_ for C503
Change value to from 39 to 33ohm(R861/R857/R488/R485/R480/R481/R864/R863)
Change R467 value from 33K to 0 Ohm
Change C433/C434 value from 6.8pf to 10pf
N.C. R466,R305

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070206
P06 update U49 symbol data to ICS9LPR358AGLFT
P55 remove R150,R146,U14 short R128 pin1 and R145 pin2 for AEC function fail

0301
NV design change
change R596 from 30 to 24.9ohm
change R502 from 40.2 to 45.3 ohm
change R52,R93,R17,R561 from 240 to 0 ohm
       R56,R95,R19,R560 from 240 to 243 ohm
change R1,R10,R18,R32,R36,R80,R102,R563 from 7.5k to 4.02k ohm

0302
 P53 modify netname for netname consistance for UNI_MIC_IN and OMNI_MIC_IN
 P25 add R940,R941 for KBC strap pin pull low
 P30 add C950 for RUN_PWRGD interferenced ,hang 49
 P24 mount R398 for THERMTRIP_GFX#_R disconnection
Crystal vendor suggestion
 (1)P19 change C874,C873 to 12P
 (2)P24 change C433,C434 to 12P
AEC EEPROM mounted for S3
 P55 mount R72,U6,R75,
     NC R92,R96,R104
AEC programming GPI change
 P20 GPIO24 connect to AEC_PWRDN# for power down AEC
     GPIO20 connect to AEC_RESEt# for programming AEC
Brightness control not support for Logo LED
 P66 (1)NC Q36,R523,Q37,R526,Q38,R539,Q40,R548
     (2)change R545,R58,R524,R522 from 200 to 100 ohm
Mount parts for leakage
 P64 mount PR116,PQ40,PR205,PQ68,PR79,PQ26
MB_FLASH function fail :change MB_FLASH_EN from SB GPIO 26 to GPIO34,GPIO26 can't used as GPIO
 P20 connect GPIo6 to TP206 , connect GPIo34 to MB_FLASH_EN ,add R942
change 2nd and 3rd fan from 12V to 5V , change Q52,Q13 to CHT2301 for 5V source

P51 NC R342 for subwoofer abnormal performance
P24 add C951 for thermistor interference by inverter transformer
P50 change F3 to 1M-F1252A5-F000 for the same with M620
P51 change F10 to 1M-F1252A5-F000 for the same with M620

0305
P20 change R844 to 10K, LAN_RST# change to pull low 10K

0306
POWER
P58 change PR148,PR153 to 150K_F,PR146,PR55 to 100K_F
    to change ocp setting to 11A
P61 (1)change PR16 to 1M_F to change OCP to 15A
    (2)delete PJ10,PJ9 ,VGFX_CORE from NV_OUT
P63 change PR71 to 130K_F,PR181 to 9.1K_F , change 12V from 11.7 to 12.2v
P59 change PR25 to 8.2K_F to set OCP to 17A
P60 mount PC145,PC117 to filter high frequency noise
P58 mount PC119,PC143 to filter high frequency noise
P62 change PR12 to 3.3_F to improve 1.05V noise
P63 change PR177 to 100K_J,add PR209,NC PR179,PR178 for improve
    adapter out 12V leakage

P33 modify CN36 symbol for PCMCIA reverse type,
P35 change ln power to +3V_EMINI_AUX to support S4 wake up

0307
P50 change U26,U27 to LLP package for support 3W
P61 change PQ9 to AOL1426 ,PQ6 to AOL1412 for support 15A NV_VDD
P34 change U41,U40,U39 to MSOP8 to meet EUV 2.4mm

0309
correct EVT BOM mian source to Substitute List
(1)P50,P60 change PC53,C913,C924 to 1C-2B20153-K000
(2)change C468,C475,C480,C907 to 1C-2B20471-K000
(3)P11,P12,P50 change C265,C284,C286,C722,C710,C738,C303 to 1C-2B20474-K000
(4)P50,P51 change L24 ,L59 to 1L-BBCMS32-1600
(5)P57 ,change PL9 to 1L-FBHWP12-1000
(6)P49 ,change C241,C243,C247,C250 to 820P NPO 0603
(7)P60 ,change PC122 to 1C-2N20181-J600
P25 delete Winbond solution

0313
P60 change PC40 to 0.1u to adjust channel current sense by vendor suggestion
P54 change U16 to 78L09L , the same with M620
P61 add PR210,PQ69,change PR133 to 28K_F for VGA power mizer(1.2V and 1.15V switch)
P43 connect NV_GPIO5 to VGA power for power mizer(1.2V and 1.15V switch)
P43 change R930,R931,C938 value to NV_*
P06 connect R752 pin 1 to R750 pin1 to follow CPU_BSEL0
P27 change LED1 to HT-110NG for changing wlan led to side
P51 change CAP16~20 to 47UF for 6BUF shortage(evt used 47uf)
P50 change L67,L70 to EBMS100505H121RDC35 for changing mainsource(EVT use this part)

0314
P53 change CN7 to HS8106,防呆
P67 NC CN3(CRT CONN) for ME interfere with thermal module
P34 change CN24 to FOX_UB4132C-T3201-4F,black color
P31 change CN15 to FOX_UV91413-WS01P-4F,black color
P11 delete L12,C194,C211,L17,L16,C204,L14,C226,R230
    Reserved R234 to +3VRUN and R236 to GND for UMA/Discrete selection,
    Refer to Santa Rosa design Guide Rev 2.0 Table 81.

0319
Modify for Clock SI
P30 mount R790,0 ohm and C848,22P for PCI_CB48 SI fail]
P06,P27 change RP30 to 18 ohm ,add C 2.2p for CLK_PCIE_MINI# SI fail
P06 change RP24 to 15ohm for CLK_PCIE_SATA# SI fail

P29 swap L51,L50,L49 for layout

0322
MOR
P49 remove R279 for delete Line in path
P50 change C458,C478 to 1000P ,X7R for THD/MR improvement
P50 add C for U44 bypass
P50 change C924 and C913 to NC for THD/MR improvement
P50 change the connection of CON3 pin7 and pin8 to DGND
P50 change GP3 to 0ohm resistor (mounted)
P52 delete R774 and R767 completely for delete MIC VREF path from CODEC
P49 U22 pin32 change to NC for delete MIC VREF path from CODEC

P45 change C27,C33,C48,C57 to 0.01uf by nvidia FAE suggestion
P46 change C28,C947,C5,C21 to 0.01uf by nvidia FAE suggestion

EMI
P59 change PR41 to 3.3ohm for EMI
P58 change PR23,PR65 to 3.3 ohm for EMI
P19 add EC36,EC39,EC40 33P bypass for BITCLK

P55 mount C83 for EMI

0326
(1)add AEC_EEPROM_WR# for programming AEC EEPROM
(2)connect DFGT_VR_EN to TP and delete PR10 , VGFX_CORE 1.05V fix

0327
(3)reserved Linear voltage control circuit for logo led suddenly off (U59,Q180,Q179,Q18
(4)1.5V enable pin change to RUN_ON for no boot from ext debug board issue
**   add CAP41(470uF) for subwoofer +12V power**

0328
(1)change C127 and C130 to 0.22uF, C121 to 1uF.
(2)change the connection of C127 to C291, C130 to C238, C121 to C324.
(3)change PR109 to 18K
(4)change R232/R266 to 33K
(5)change R199/R253 to 1.8K

0329
(1)change R424,R807 to 1K_J for follow M610(MOR request)
(2)remove NVIDIA NC pin TP to enlarge NV_VDD power plan
(3)add R962,R961,L71,L72,EC54,EC55,EC56 for EMI

0331
Reserved CAP42 and PD32 for 1.05V undershoot 100mV
Reserved R963 for S3 resume shutdown

0402
(1)change PC161 to 0.47uf ,50V for adjust +3VRUN and +1_5VRUN
timing(close) for external debug boot
(2)reserved R964 for disable Thrmtrip

0403
add CAP44 for LVDS power ripple (too large,spec is 200mv)

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070602
Page 55 U6 change to 13-AT24C02-8001, add TP for AEC test usage.
Page 58 Remove PJ20,PJ21,PJ32,PJ31,PJ8,PJ11 .
Page 59 Remove PJ14,PJ15,PJ17,PJ18,PJ19 .
Page 60 Remove PJ16,PJ13.
Page 61 Remove PJ33,PJ12,PJ2,PJ6,PJ30,PJ35.
Page 62 Remove PJ7,PJ3,PJ4,PJ5,PJ28.
Page 63 Remove PJ26,PJ27,PJ25, Change PR1 and PJ1 to close gap GP20, GP21,GP22
         Add PD33 at +12VRUN output.
Page 64 Remove PJ34.
Page 33 CAP3 change to 1C-44R0476-M200.
Page 27 LED1 change to HT-110UYG.
Page 24 NC SW3 and change to resistor for System ID control
Page 50 change R966 to stuff and R965 to NC.
Page 9   Change to NC : R675, R667, R225 Change to Stuff : R221, R214, R693,
         R696, R689, R691, R692, R688, R687 for disable CRT function.
Page 11 Change from stuff to NC :L44,L45,C731,R224,C197,L13,R679,R234,R685,L47,C735,L48,
         Change from NC to stuff : R683,R227,R677,R236,R686,R699 for disable CRT function.
Page 66 Change from stuff to NC :Q179,Q180,U59,R946,R953,R951,R952,C955,R945,Q181,R944
         to remove 2nd logo LED solution.
Page 57 Add PR214 to 30K ohm, PR215 to 12K ohm, Change PR203 to 22K ohm, PR201 to 39K ohm.
         To set the different setting for M630 and M640.
Page 65 Add PR216 30K ohm, change PR182 22K ohm, change PR183 10k ohm.
         To set the different setting for M630 and M640.
Page 49 Change CN21 to 2N-0006000-FET0.
Page 17 Add ESD diode D25 for INV_ENABLE and INV_BRADJ signal for U17, U35 damaged issue.
Page 3   Remove TP :TP140,TP146,TP127,TP134,TP125,TP137,TP126,TP157,TP133,TP148,TP142,TP136
         ,TP120,TP141,TP128,TP119,TP135,TP156
         to Remove test point for interference with CPU bracket.
Page 20 NC SW4 and use resistor for system ID control
Page 4   Remove TP159,TP124, TP158,TP32 for not interference with CPU bracket.
Page 40 NC :L5,C70,C595,C608, Change to pull down 10K ohm : R115,R614,R621 diable CRT function.
Page 67 NC : R132,R694,R133,R697,R131,R690,R568,R648,R567,R649,R565,R591,R566,R590,CN3
         Disable CRT function.
Page 50 Change F3 to 4A capability.
Page 34 Change C469,C449,C430 to 1C-2B30105-M000 : 25V rating component
Page 44 Change to NC : R647,R645,R646,R626,R609,R610,R611,R634,R635,R624 Disable CRT
Page 52 Change C138,C167 to 4.7u_16V_0805(1C-2B70475-K300) for audio precision test result.
Page 52,50 change CON1, CON2 , CON3 vendor part number.
Page 68 Change nut pad reference to BOSS for factory requirement.
Page 46,45 Remove R52, C39, R17, C24, R561, C487, R93, C63 change Vram clock termination.
Page 25 Reserve caps C957,C958,C959 for Fan_tach signal noise improvement.
Page 57 Add PD34 for different setting for M640.
Page 55 Change net connection for AEC debugging.
Page 28 Change R138 to 8.2K and C82 to X7R for T8 setting to 110 celcius degree.
Page 66, 34 Add F13 and F14 for TUV spec.
Page 52 Change R786 and R782 to 6.8K Change resistor value to meet FSIV 2.0.
Page 66 Change to polyfuse 1M-F006A35-F000 0.35A rating from using 0 ohm at DVT.
        (F1,F4,F5,F6,F7) F2 use 0.5A rating.
0604
Page 14,15 Change C125, C122 to X5R rating for high temperature near Dimm module.
Page 20 Add C960 0.1uF at IC power pin.
Page 17 change C389 from 1uF to 0.1uF.
Page 64 Stuff PR111 and PQ38 for +3VRUN_TV discharge slow.
0607
Page 57 Implement new UVP protect circuit to prevent insert different adaptor risk.
Page 59 Add EC66,EC67,EC68,EC69,EC70 to +1_8V_S3_SUS to GND for EMI solution.
Page 66, 52 Add EC72,EC73,EC74,EC75 +5VALW to GND ,EC71 +5VALW to +5VALW , EC76, EC77, EC78
         , EC79 +5V_S3_SUS to GND for EMI solution. Page 52 EC65 A_GND to GND, Place near L71.

Page 45,46 Reserver 8 caps for Vram power and place 2 pcs for each Vram.
Page 58 Add PC186, PC185 at +3VALW input and output for noise improvement.
Page 25 Add R969 for +ECVCC discharge path reservation.
Page 57 Add PR219 for the discharge of UVP protect circuit, and change PR105 to 10K,
         PR218 change to 249K for tolerance control.
Page 34 Change from 0 ohm to common choke for EMI request on all USB port.
Page 28 Change Fan3 circuit for stuff at M630 only.

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