

Winery13 CALPELLA DIS N11M-GE1 Schematics

uFCPGA Mobile Arrandale

Intel IbeX Peak-M

2010-01-13

REV : A00

DY : Nopop Component
UMA : Pop when schematic is UMA
DIS : Pop when schematic is DIS

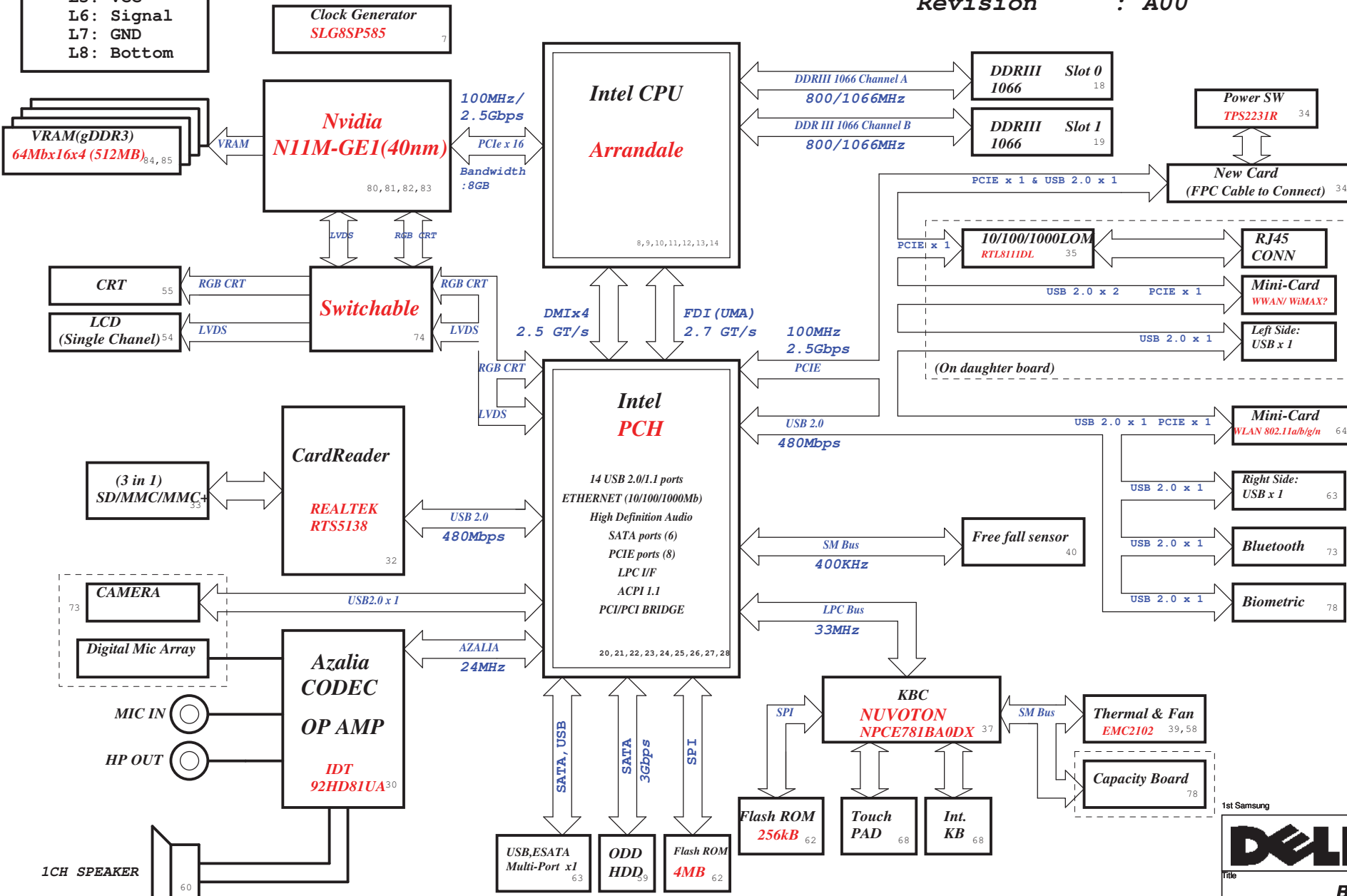
Winery CALPELLA Block Diagram

PCB LAYER

- L1: Top
- L2: GND
- L3: Signal
- L4: Signal
- L5: VCC
- L6: Signal
- L7: GND
- L8: Bottom

Project code : 91.4EX01.001
 Part Number : 48.4EX01.001
 PCB P/N : 09288
 Revision : A00

CPU DC/DC ISL62883 47,48	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_CORE
SYSTEM DC/DC RT8205B 46	
INPUTS	OUTPUTS
+PWR_SRC	+15V_ALW +3.3V_RTC_LDO +5V_ALW +3.3V_ALW
SYSTEM DC/DC TPS51116 50	
INPUTS	OUTPUTS
+PWR_SRC	+1.5V_SUS +0.75V_DDR_VTT +V_DDR_REF
SYSTEM DC/DC ADP3211 53	
INPUTS	OUTPUTS
+PWR_SRC	+CPU_GFXCORE
SYSTEM DC/DC TPS51218 86	
INPUTS	OUTPUTS
+PWR_SRC	+VCC_GFX_CORE
CHARGER BQ24745 45	
INPUTS	OUTPUTS
+DC_IN +PBATT	+PWR_SRC
SYSTEM DC/DC TPS51218 49	
INPUTS	OUTPUTS
+PWR_SRC	+1.05V_VTT
LDO APL5930 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN
LDO RT9025 51	
INPUTS	OUTPUTS
+3.3V_ALW	+1.8V_RUN_GPU



<http://laptop-motherboard-schematic.blogspot.com/>

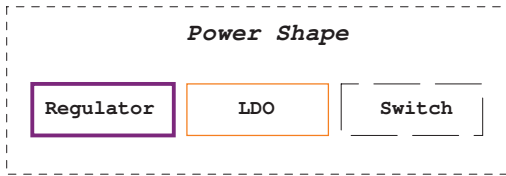
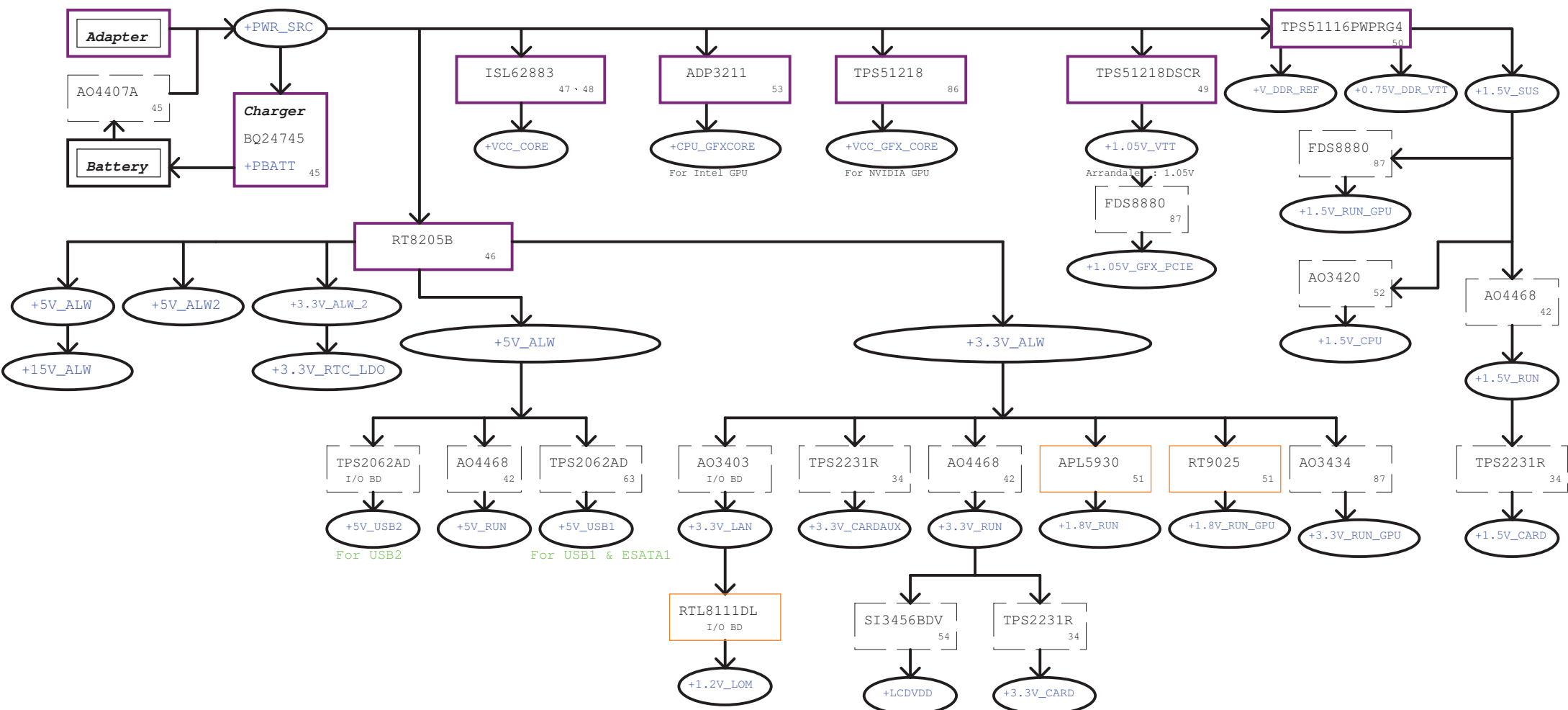
1st Samsung

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Block Diagram

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 2 of 88



1st Samsung

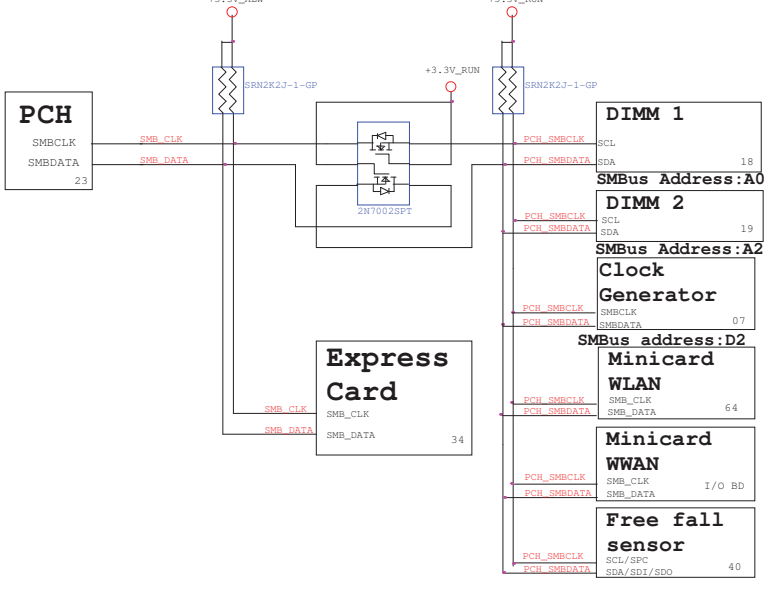
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

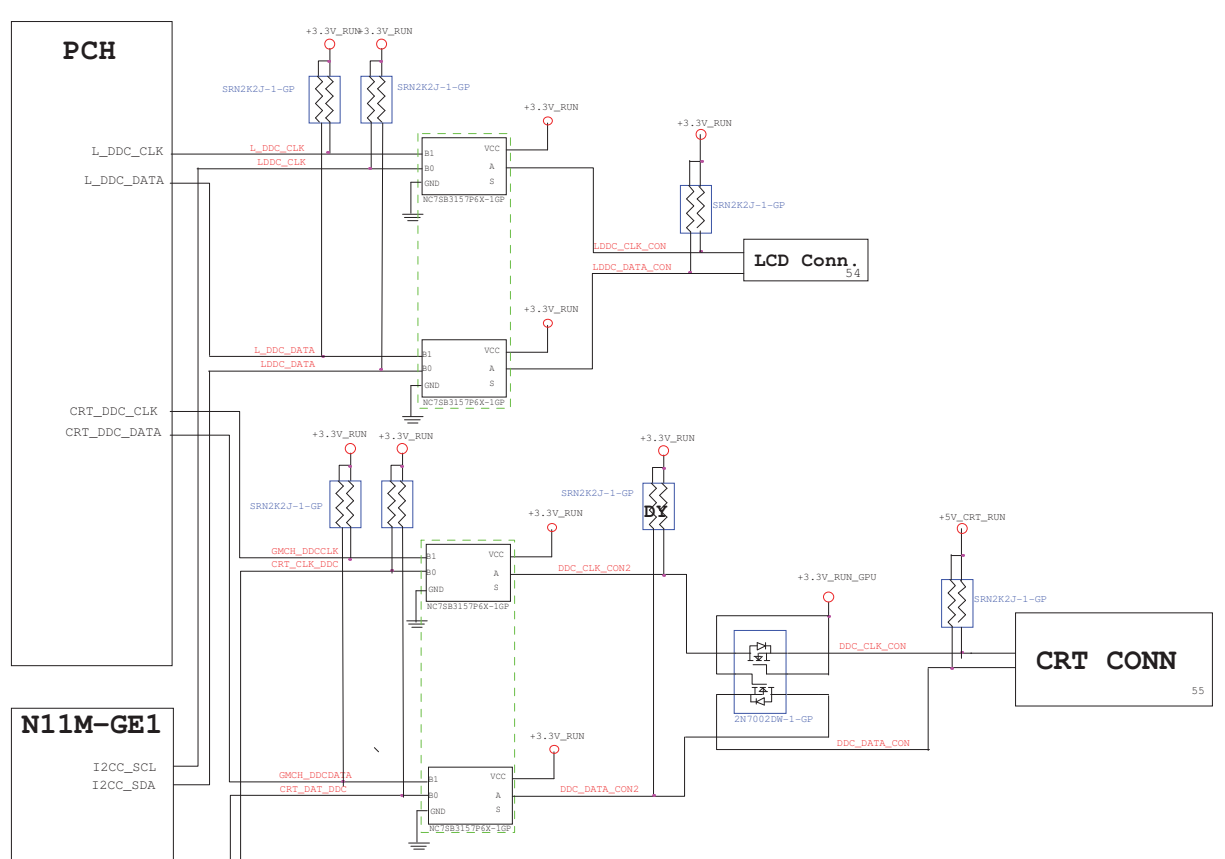
Size: Custom Document Number: **Winery13 MB DIS** Rev: **A00**

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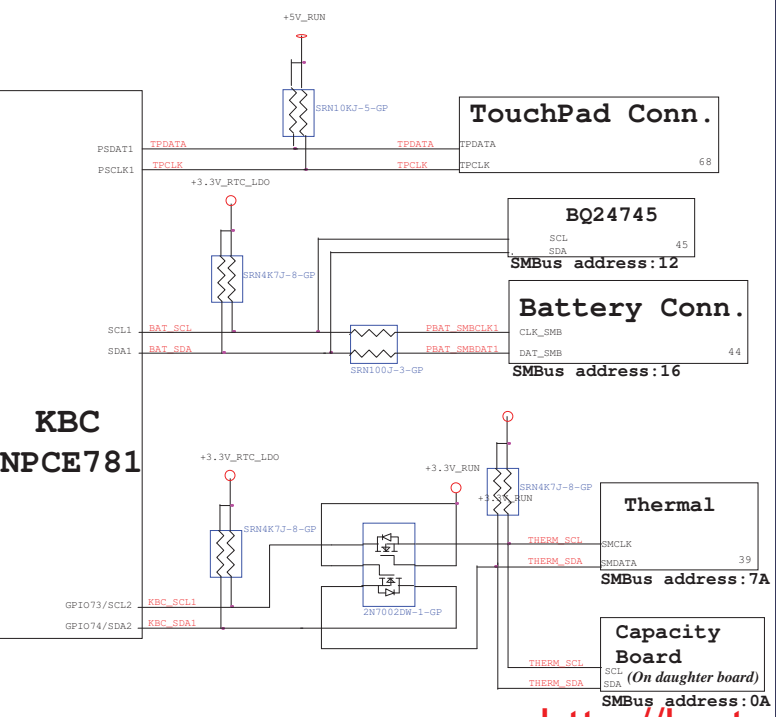
PCH SMBus Block Diagram



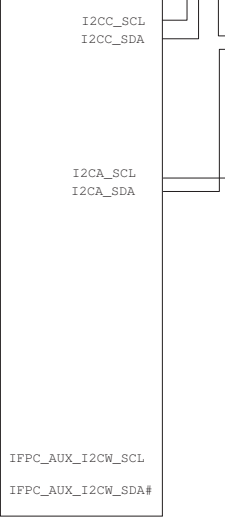
Switchable Graphic SMBus Block Diagram



KBC SMBus Block Diagram



N11M-GE1



<http://laptop-motherboard-schematic.blogspot.com/>

1st Samsung

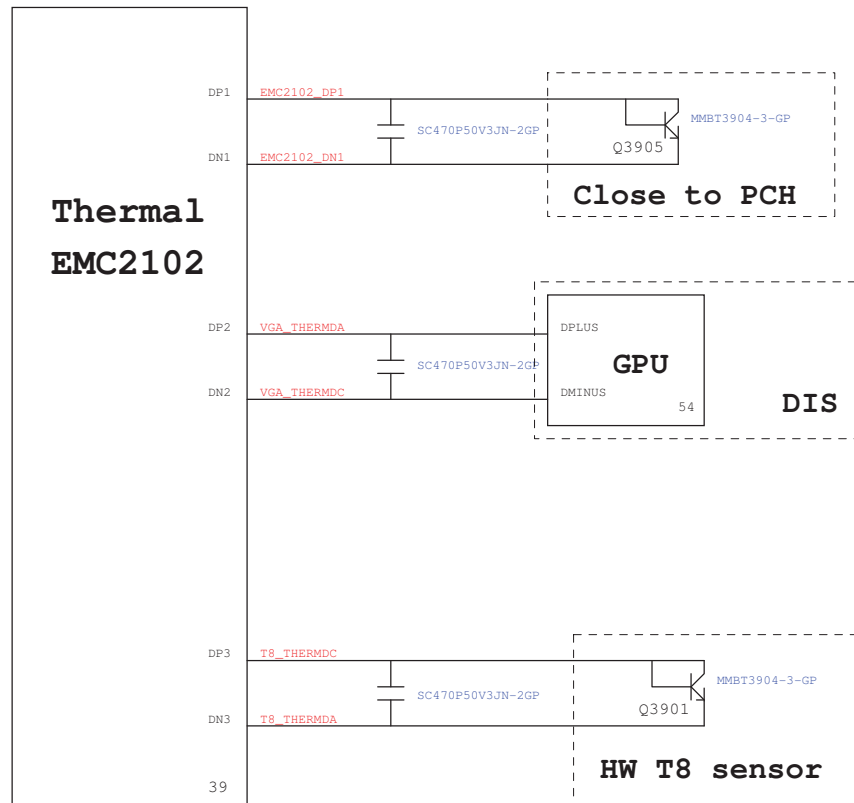
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

#/0
SMBUS Block Diagram

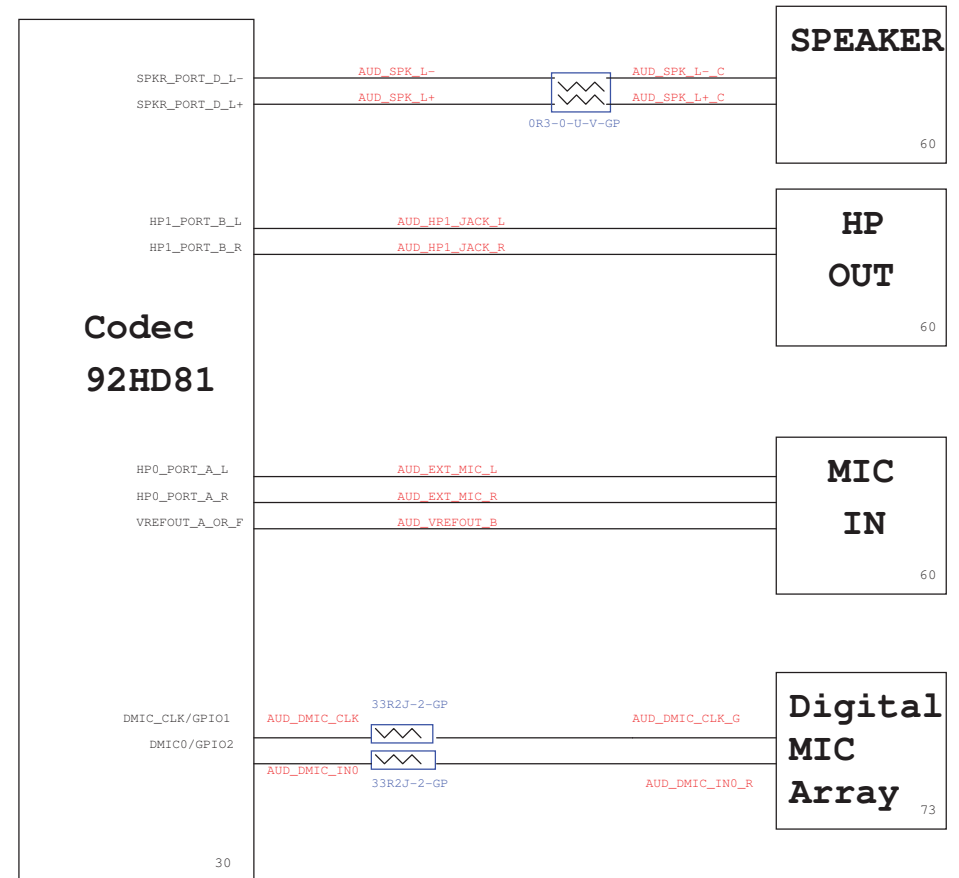
Size C Document Number **Winery13 MB DIS** Rev **A00**

Date: Wednesday, January 13, 2010 Sheet 4 of 88

Thermal Block Diagram



Audio Block Diagram



PCH Strapping Calpella Schematic Checklist Rev1.6

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor. Intel suggest 1K resistor (Fonseca)
INIT3_3V#	Internal pull-up. Leave as "No Connect"
GNT3#/GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode Note: Connect to ground with 4.7-kΩ weak pull-down resistor. CRB uses a 1 kΩ; do not stuff resistor.
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled Note: CRB uses a 330-kΩ resistor.
GNT0#, GNT1#	Default (SPI): Leave both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor. Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating.
GNT2#/GPIO53	Default - Internal pull-up. Low (0) = Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
SPI_MOSI	Enable Intel Anti-Theft Technology: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Intel Anti-Theft Technology: Left floating, no pull-down required.
NV_ALE	Enable Intel Anti-Theft Technology: Connect to +NVRAM_Vccq with 8.2-kΩ weak pull-up resistor. [CRB has it pulled up with 1-kΩ no-stuff resistor] Disable Intel Anti-Theft Technology: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HDA_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kΩ pull-down for FD Override. There is an internal pull-up of 20 kΩ for HDA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low (0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High (1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality Note: This is an unmuxed signal. This signal has a weak internal pull-down of 20 KΩ which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kΩ pull-up on this signal to +3.3VA rail.
GPIO8	Weak internal pull-up. Do not pull low. Sampled at rising edge of RSMRST#.
GPIO27	Default = Do not connect (floating). Internal pull-up. High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping Calpella Schematic Checklist Rev1.6

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1

PCIE Routing

LANE1	Card reader
LANE2	MiniCard WLAN
LANE3	LAN
LANE4	MiniCard WWAN
LANE5	New Card

USB Table

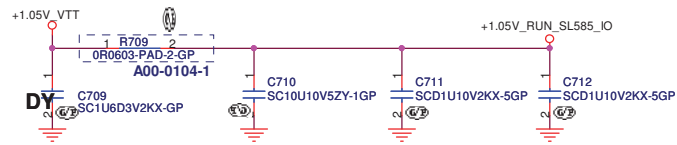
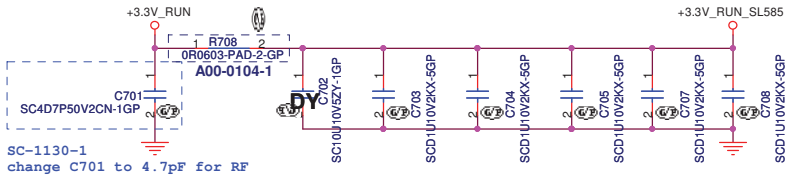
USB	
Pair	Device
0	USB1
1	USB for ESATA
2	USB2
3	RESERVE
4	WLAN
5	WWAN
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BLUETOOTH
9	Card Reader
10	Biometric
11	CAMERA
12	New Card
13	RESERVED

1st Samsung



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Date: Wednesday, January 13, 2010	Sheet 6 of	88

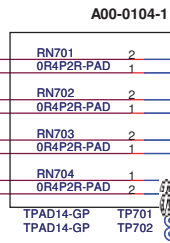
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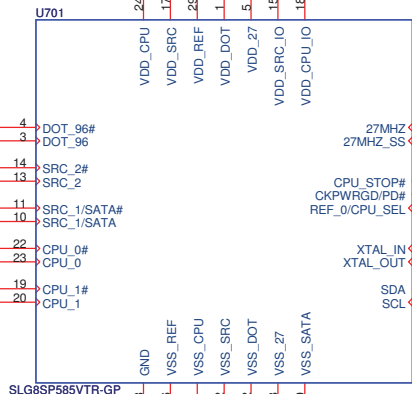
+3.3V_RUN_SL585

+1.05V_RUN_SL585_IO

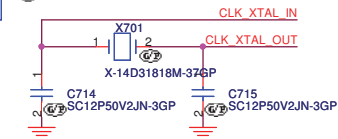
- [23] DREFCLK#
- [23] DREFCLK
- [23] CLKIN_DMI#
- [23] CLKIN_DMI
- [23] CLK_PCIE_SATA#
- [23] CLK_PCIE_SATA
- [23] CLK_CPU_BCLK#
- [23] CLK_CPU_BCLK



1st Silego 71.08585.003
2nd ICS 71.93197.003

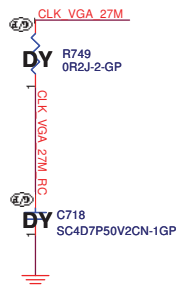
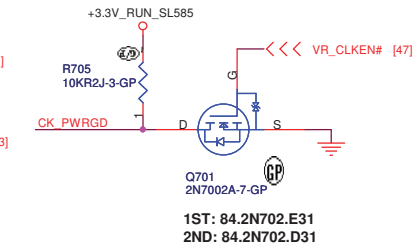


VGA 27M	R706	R710
SS	DY	Mount
NON-SS	Mount	DY



1st: HARMONY 82.30005.901
2nd: ITTI 82.30005.C51
3rd: TXC 82.30005.B81

FSC	0	1
SPEED	133MHz (Default)	100MHz



1st Samsung

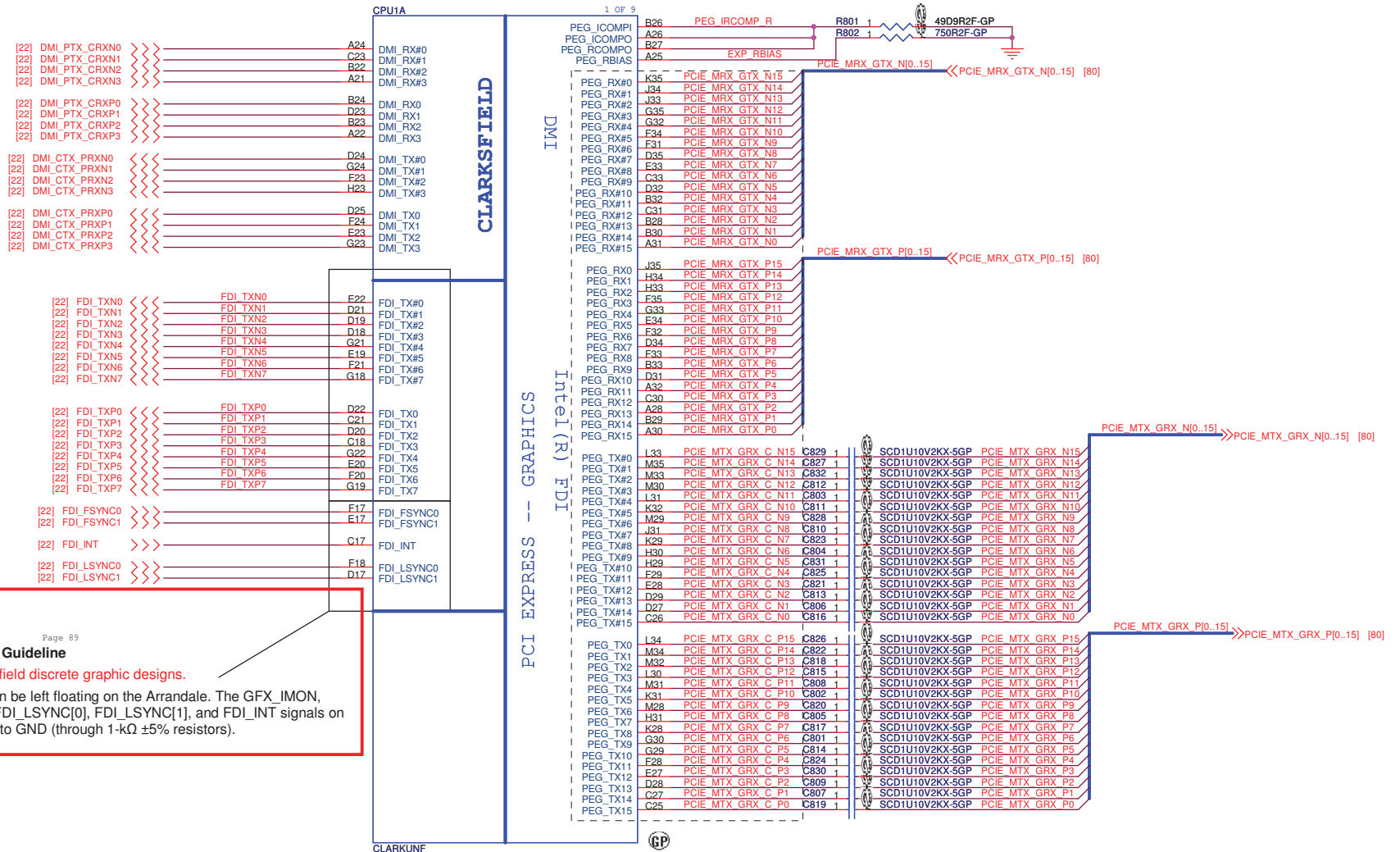
DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Clock Generator SLG8SP585**

Size	Document Number	Rev
		A00

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SSID = CPU



Calpella Platform Design Guide
Revision 1.6

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2.4 Arrandale Graphics Disable Guideline

It applies to Arrandale and Clarksfield discrete graphic designs.

FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The GFX_IMON, FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

<http://laptop-motherboard-schematic.blogspot.com/>

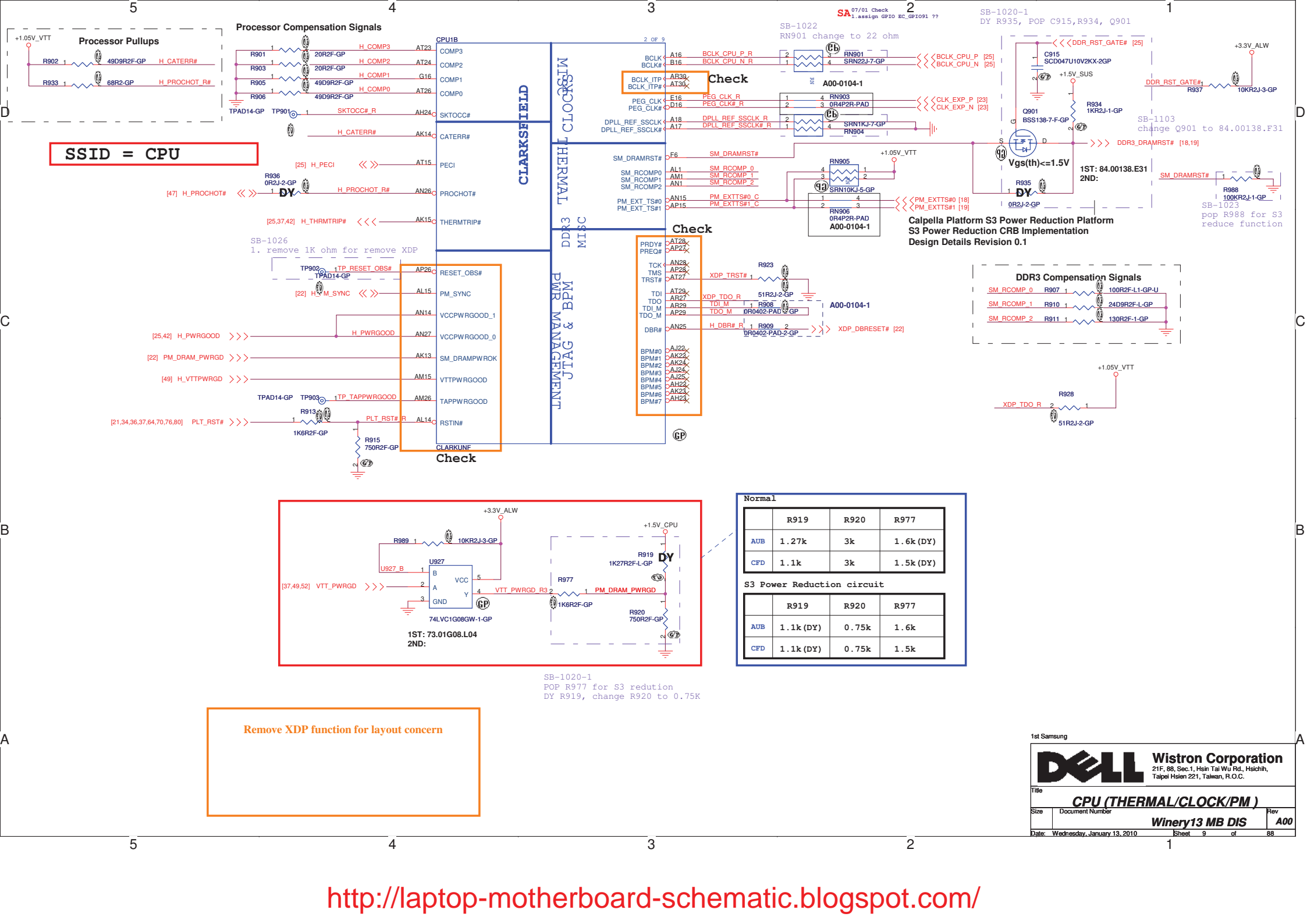
1st Samsung

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (PCIe/DMI/FDI)**

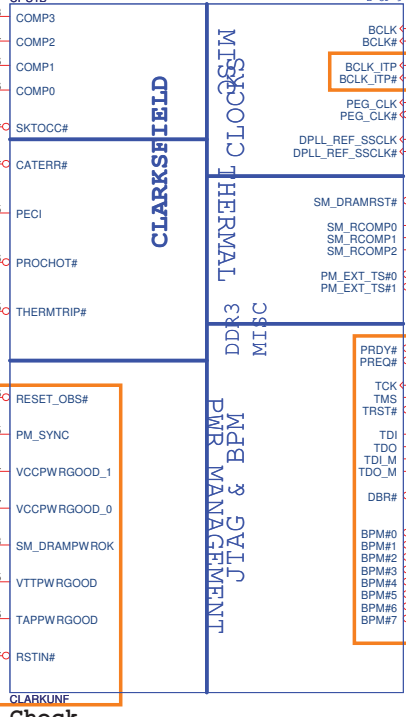
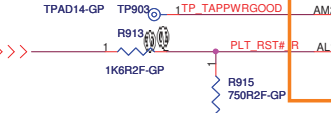
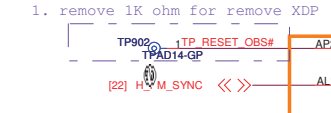
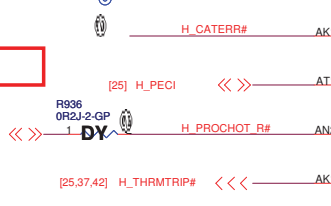
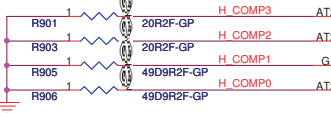
Size: Document Number: **Winery13 MB DIS** Rev: **A00**

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SSID = CPU

Processor Compensation Signals



Check

Check

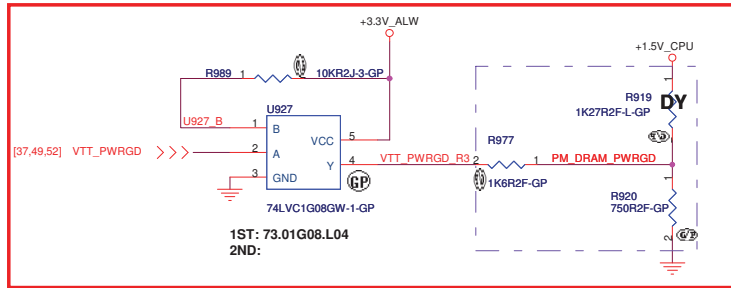
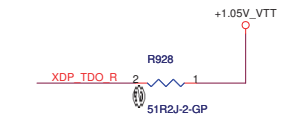
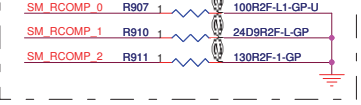
Check

SA 07/01 Check
1. assign GPIO EC_GP1091 ??

SB-1020-1
DY R935, POP C915, R934, Q901

**Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details Revision 0.1**

DDR3 Compensation Signals



	R919	R920	R977
Normal			
AUB	1.27k	3k	1.6k (DY)
CPD	1.1k	3k	1.5k (DY)
S3 Power Reduction circuit			
AUB	1.1k (DY)	0.75k	1.6k
CPD	1.1k (DY)	0.75k	1.5k

SB-1020-1
POP R977 for S3 reduction
DY R919, change R920 to 0.75k

Remove XDP function for layout concern

1st Samsung

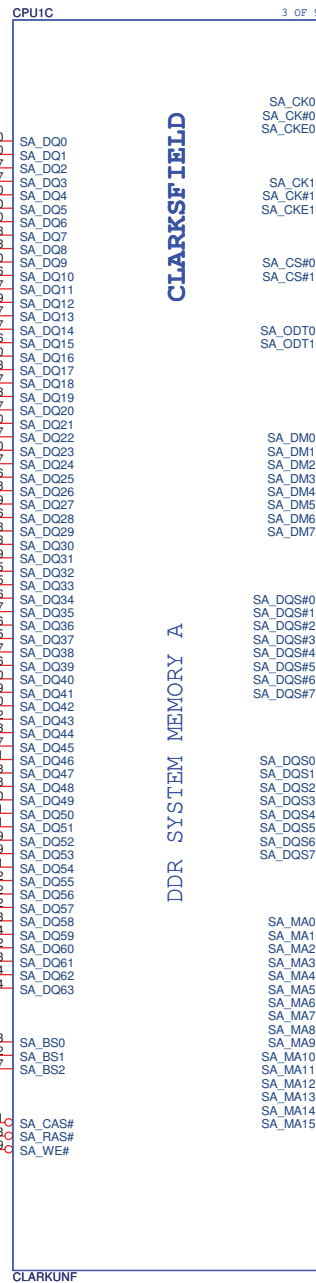
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (THERMAL/CLOCK/PM)**

Size: Document Number: **Winery13 MB DIS** Rev: **A00**

Date: Wednesday, January 13, 2010 Sheet 9 of 88

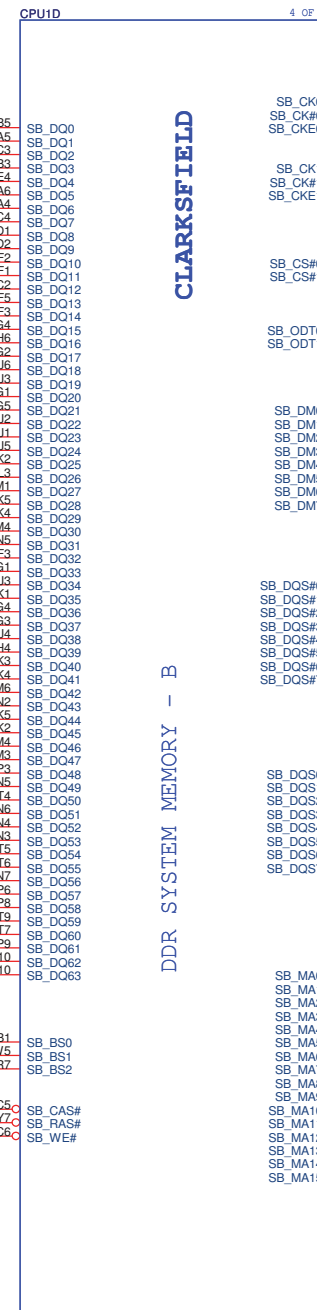
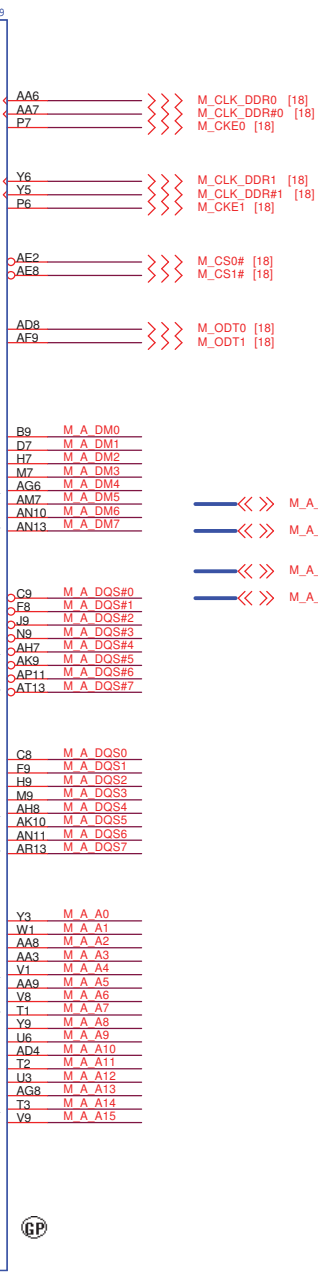
SSID = CPU



CLARKSFIELD

DDR SYSTEM MEMORY A

CLARKUNF



CLARKSFIELD

DDR SYSTEM MEMORY - B

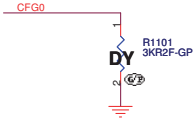
CLARKUNF

1st Samsung

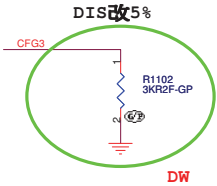
DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title			CPU (DDR)		
Size	Document Number	Rev	A00		
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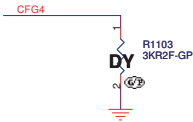
SSID = CPU



PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled



CFG3 - PCI-Express Static Lane Reversal	
CFG3	1:Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...



CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

**Calpella Platform Design Guide
Revision 1.6**

4.8.3.1 LVDS Switching

Switchable GFX, just like integrated GFX only, to enable LVDS it is required that the OEM set the LDVS (L_DDC_DATA) strap to present (pulled up) and the eDP strap (CFG[4]) to disabled (not pulled down).

4.8.3.2 eDP Switching

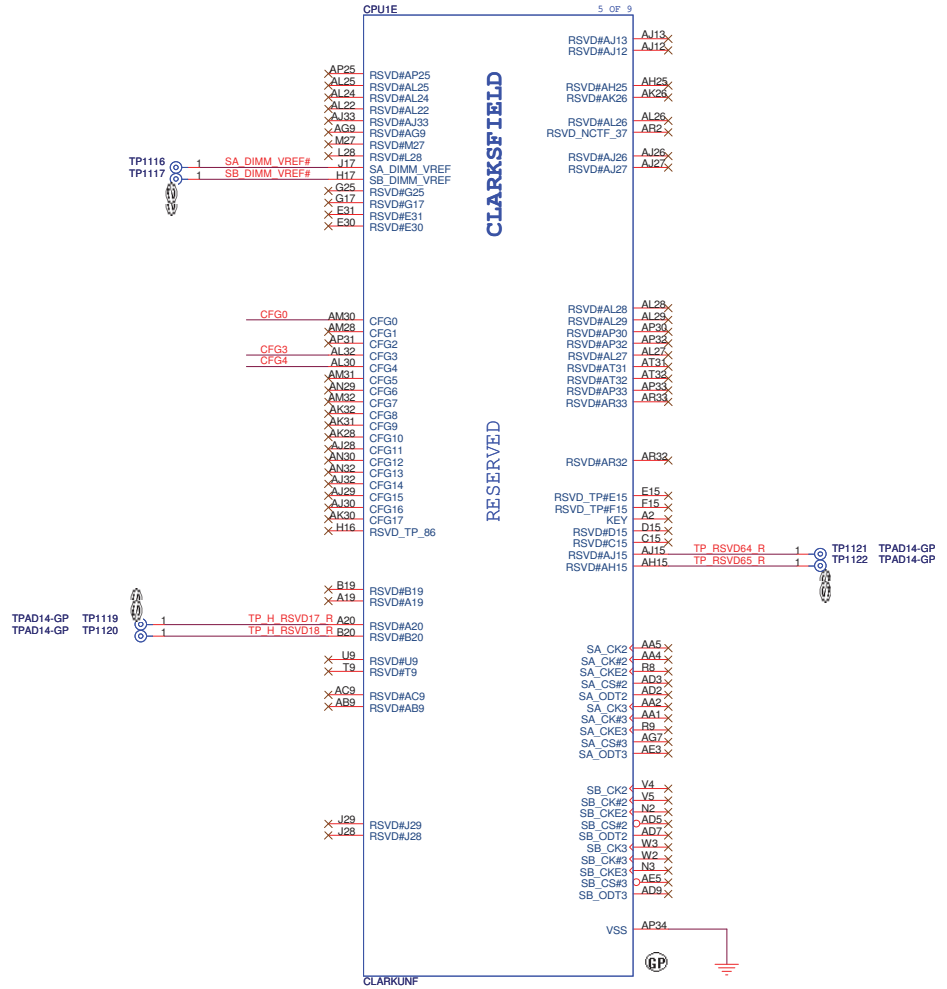
eDP for Switchable GFX can only be driven out of Port D of PCH. To configure Port D for embedded DP it is required to set the DDPD_CTRLDATA strap high to 3.3V Core rail through 2.2 kΩ ±5% resistor, LVDS (L_DDC_DATA) strap as no connect and the eDP strap CFG[4] as no connect.

Page 482, 486

DW
07/02 Added
1.Added display Switchable strap commentariat

DW30 Only support Arrandale, CFG7 no need pull down

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.



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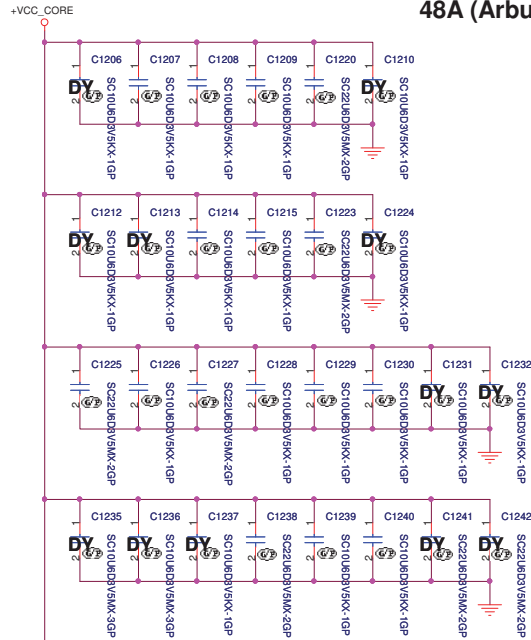
Title: **CPU (RESERVED)**

Size: Document Number: **Winery13 MB DIS** Rev: **A00**

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SSID = CPU

PROCESSOR CORE POWER
48A (Arburdale)



SC-1207-1
pop C1243 and change size to 0603 for EMI

- +VCC_CORE
- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AF35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AF26 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- U35 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- R27 VCC
- R26 VCC
- P35 VCC
- P34 VCC
- P33 VCC
- P32 VCC
- P31 VCC
- P30 VCC
- P29 VCC
- P28 VCC
- P27 VCC
- P26 VCC

CLARKSFIELD

1.1V RAIL POWER

CPU CORE SUPPLY

POWER

CPU VIDS

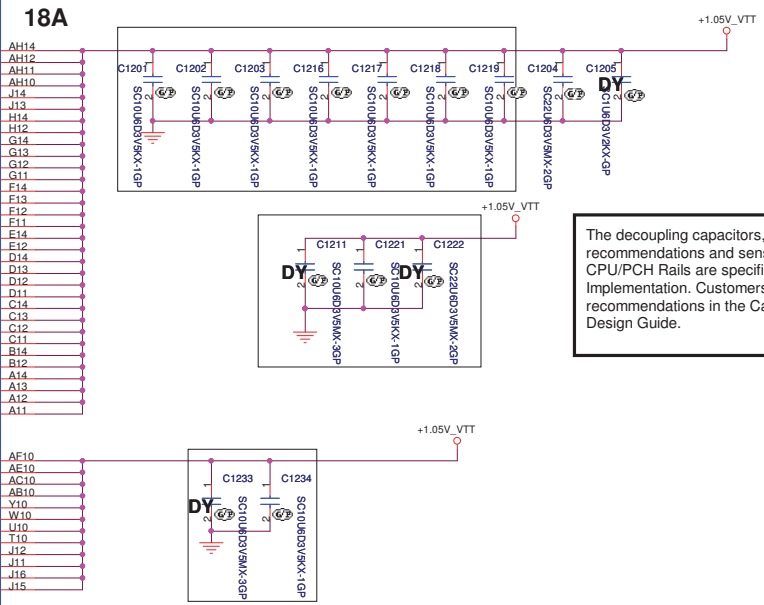
SENSE LINES

- VTT0 AH14
- VTT0 AH12
- VTT0 AH11
- VTT0 AH10
- VTT0 J14
- VTT0 H14
- VTT0 H13
- VTT0 H12
- VTT0 G14
- VTT0 G13
- VTT0 G12
- VTT0 G11
- VTT0 F14
- VTT0 F13
- VTT0 F12
- VTT0 E12
- VTT0 D14
- VTT0 D13
- VTT0 D12
- VTT0 D11
- VTT0 C14
- VTT0 C13
- VTT0 C12
- VTT0 C11
- VTT0 B14
- VTT0 B12
- VTT0 A14
- VTT0 A13
- VTT0 A12
- VTT0 A11

- PSH# AN33 >>> PSH# [47]
- VID AK35 CPU_VID0 >>> CPU_VID[6.0] [47]
- VID AK33 CPU_VID1
- VID AK34 CPU_VID2
- VID AL35 CPU_VID3
- VID AL33 CPU_VID4
- VID AM33 CPU_VID5
- VID AM35 CPU_VID6
- PROC_DPRSLPVR AM34 >>> PM_DPRSLPVR [47]

- VTT_SELECT G15 TP_H_VTTVID1 1 TP1203 TPAD14-GP

- ISENSE AN35 <<< IMVP_IMON [47]
- VCC_SENSE AJ34 VCC_SENSE >>> VCC_SENSE [47]
- VSS_SENSE AJ35 VSS_SENSE >>> VSS_SENSE [47]
- VTT_SENSE B15 TP_VSS_SENSE_VTT <<< VTT_SENSE [49]
- VSS_SENSE_VTT A15 TP_VSS_SENSE_VTT TP1202 TPAD14-GP



The decoupling capacitors, filter recommendations and sense resistors on the CPU/PCH Rails are specific to the CRB Implementation. Customers need to follow the recommendations in the Calpella Platform Design Guide.

Please note that the VTT Rail Values are
Arrandale VTT=1.05V;
Clarkfield VTT=1.1V
H_VTTVID1 = Low, 1.1V
H_VTTVID1 = High, 1.05V

SA
07/01 Check
1. DPRSLPVR ??

1st Samsung

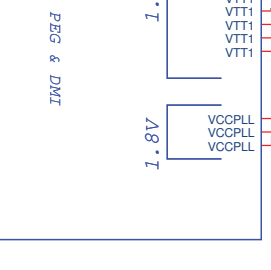
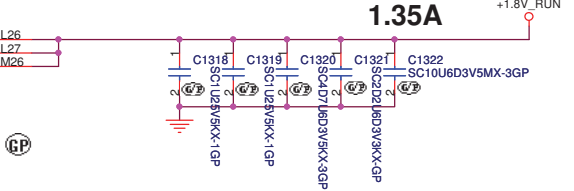
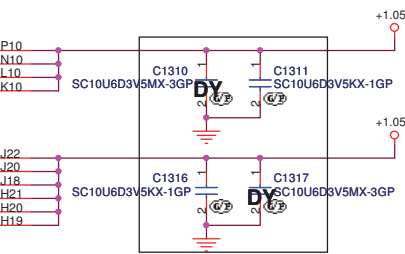
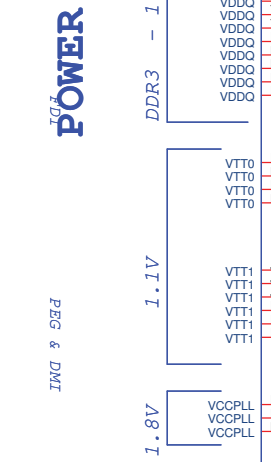
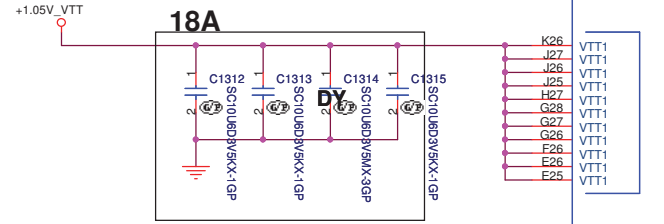
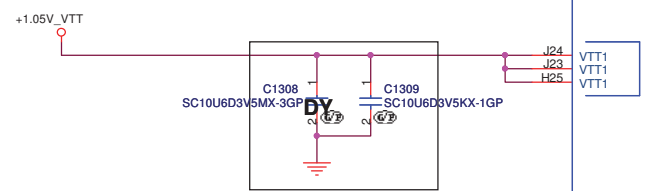
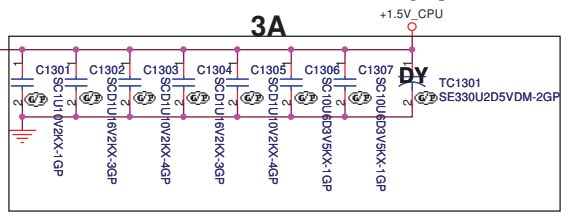
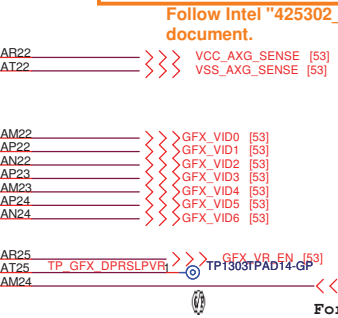
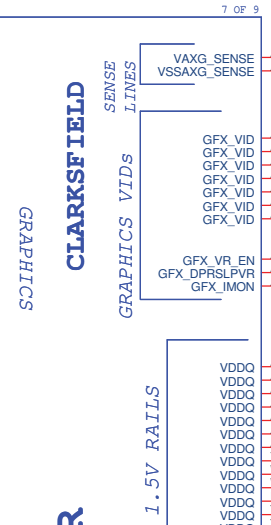
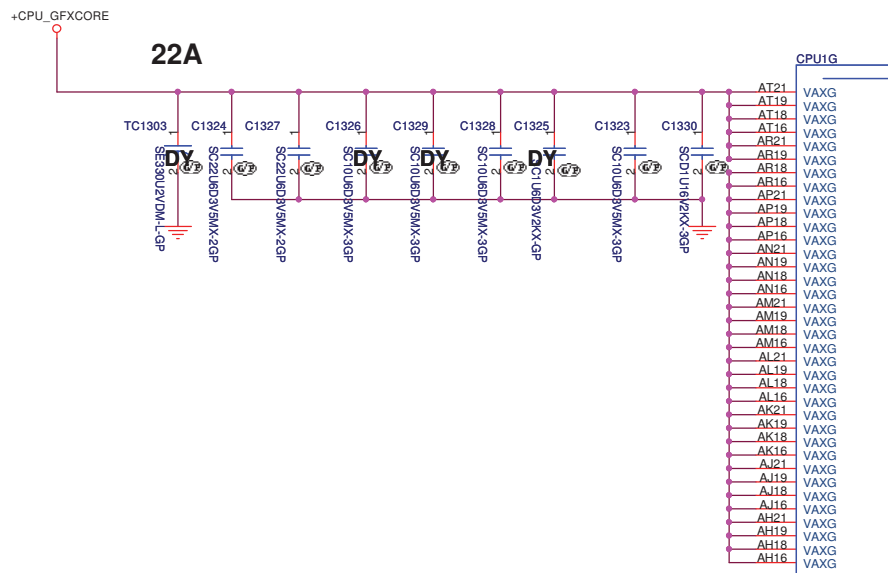


Table with 4 columns: Title, Size, Document Number, Rev. Title: CPU (VCC_CORE), Size: Winery13 MB DIS, Rev: A00

SSID = CPU



Follow Intel "425302_Calpella_S3PowerReduction_WhitePaper_Rev0.9.pdf" document.



1st Samsung

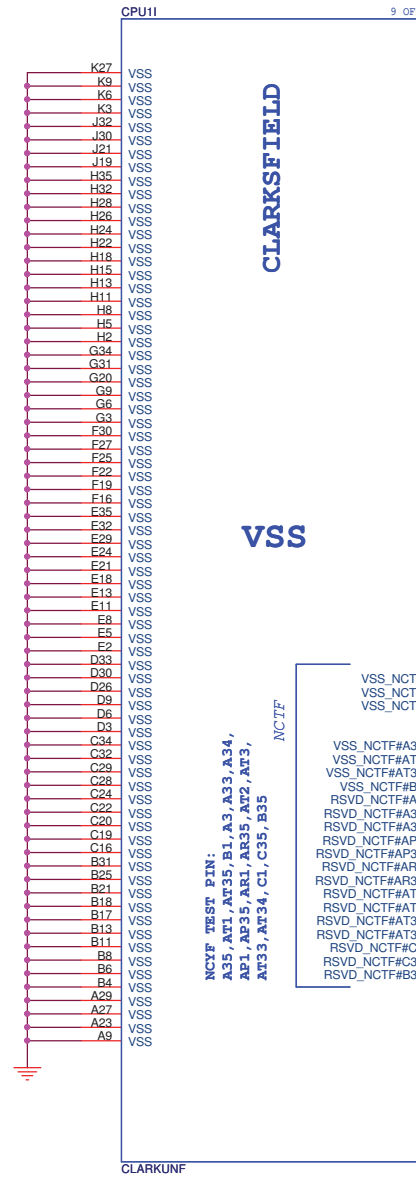
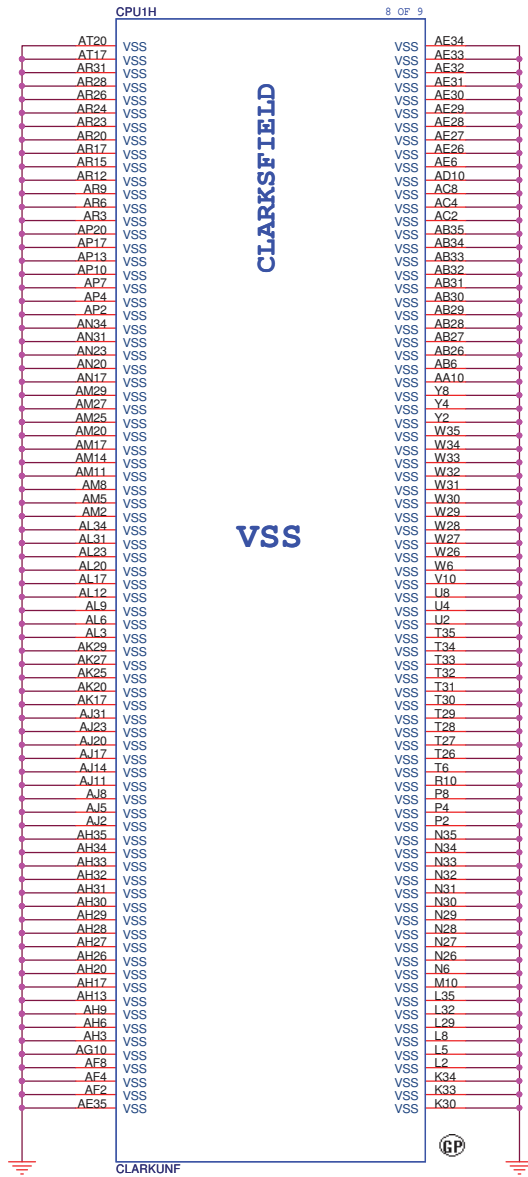
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (VCC_GFXCORE)**

Size: Document Number: **Winery13 MB DIS** Rev: **A00**

Date: Wednesday, January 13, 2010 Sheet 13 of 88

SSID = CPU



1st Samsung



Title		CPU (VSS)	
Size	Document Number	Rev	A00
Date:	Wednesday, January 13, 2010	Sheet	14 of 88

(Blanking)

1st Samsung

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A3	Document Number	Winery13 MB DIS	Rev A00
Date: Wednesday, January 13, 2010	Sheet 15	of	88

(Blanking)


1st Samsung

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A3	Document Number	Winery13 MB DIS	Rev A00
Date: Wednesday, January 13, 2010	Sheet 16	of 88	

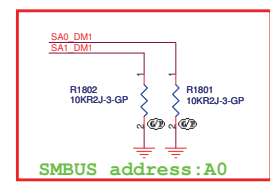
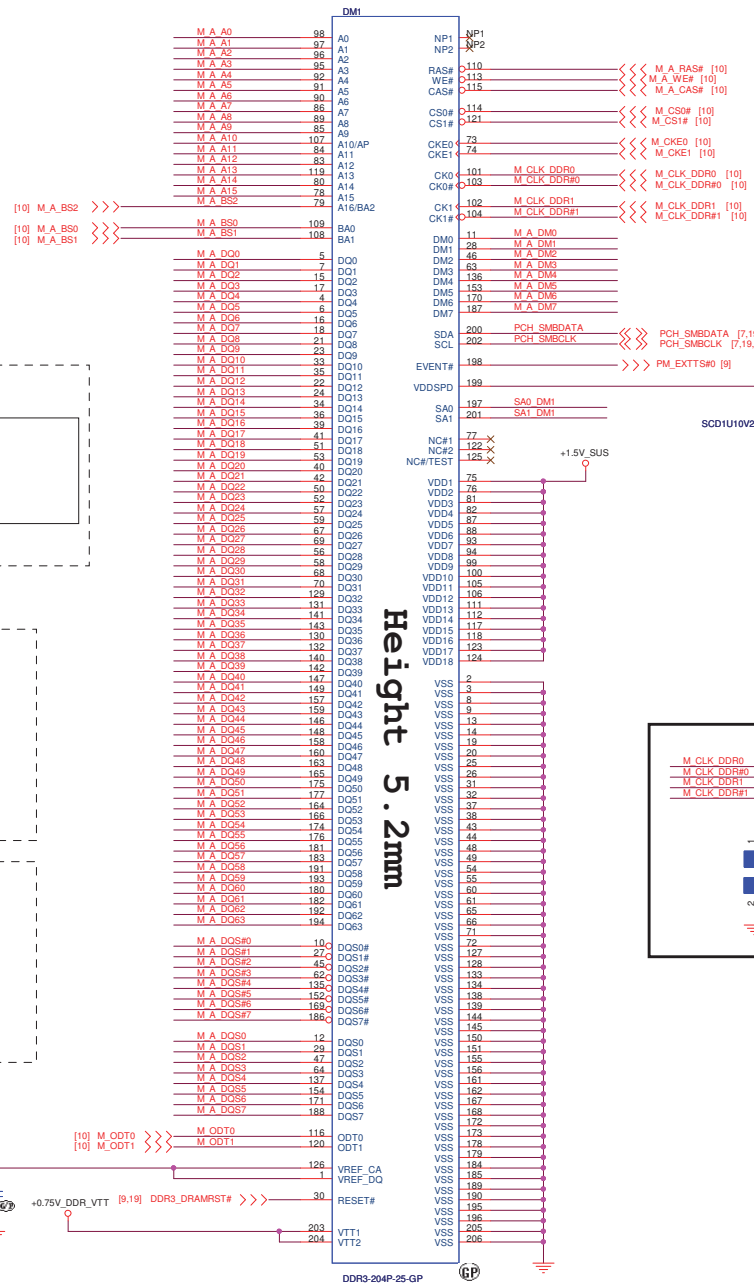
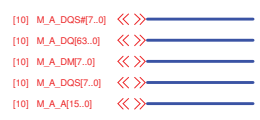
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<http://laptop-motherboard-schematic.blogspot.com/>

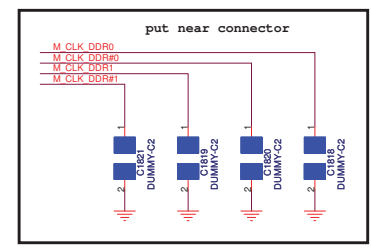
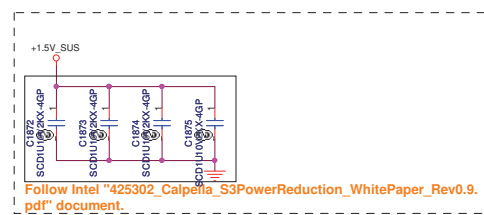
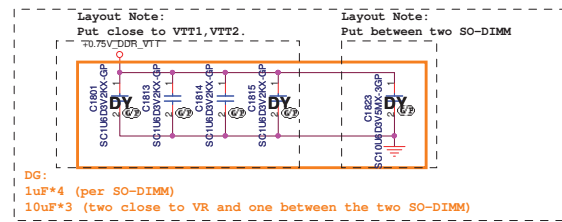
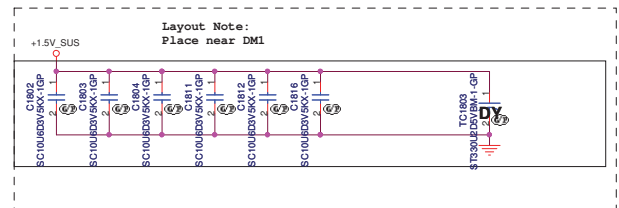
1st Samsung

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserve)					
Size	Document Number				Rev
Custom	Winery13 MB DIS				A00
Date: Wednesday, January 13, 2010					
Sheet 17 of 88					

SSID = MEMORY



DW
 07/02 Reserve
 1. Added SA0_DM1 pull-up resistor
 07/07
 2. Reserve pull-bi, lo resistor



Height 5.2mm

1st Samsung

Wistron Corporation
 21F, 88, Sec.1, Heintai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

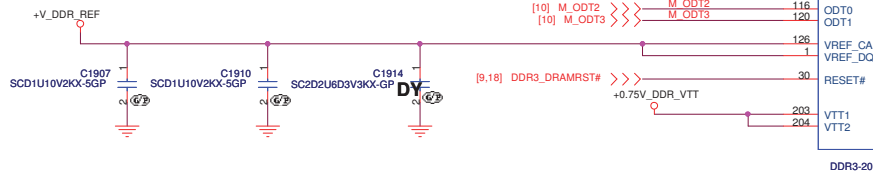
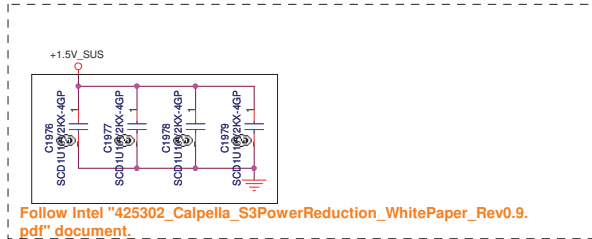
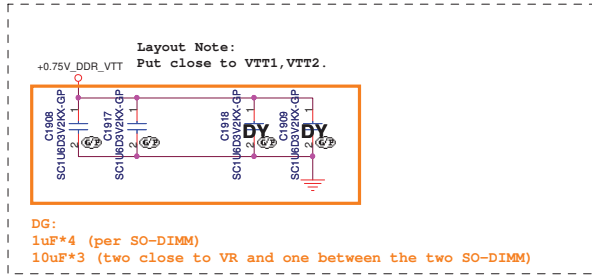
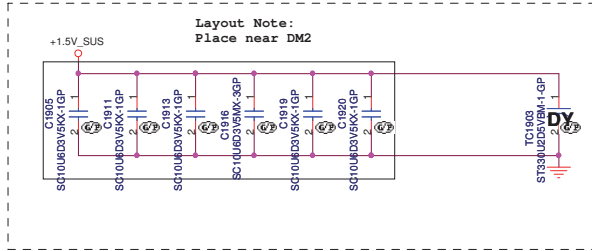
Title: **DDRIII-SODIMM SLOT1**

Revision: **A00**

Date: Wednesday, January 13, 2010 Sheet 18 of 88

SSID = MEMORY

- [10] M_B_DQS# [7..0] <<>
- [10] M_B_DQ# [63..0] <<>
- [10] M_B_DM [7..0] <<>
- [10] M_B_DQS# [7..0] <<>
- [10] M_B_A [15..0] <<>

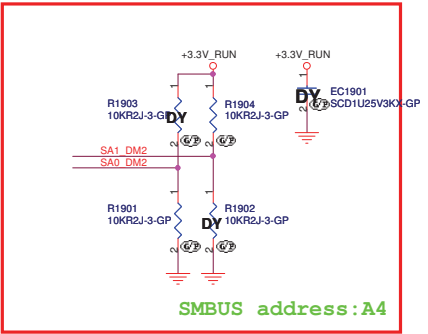


- [10] M_B_BS2 >>>
- [10] M_B_BS0 >>>
- [10] M_B_BS1 >>>

M_B A0	98	A0
M_B A1	97	A1
M_B A2	96	A2
M_B A3	95	A3
M_B A4	94	A4
M_B A5	93	A5
M_B A6	92	A6
M_B A7	91	A7
M_B A8	90	A8
M_B A9	89	A9
M_B A10	88	A10/AP
M_B A11	87	A11
M_B A12	86	A12
M_B A13	85	A13
M_B A14	84	A14
M_B A15	83	A15
M_B BS2	79	A16/BA2
M_B BS0	109	BA0
M_B BS1	108	BA1
M_B DQ0	5	DQ0
M_B DQ1	7	DQ1
M_B DQ2	15	DQ2
M_B DQ3	17	DQ3
M_B DQ4	4	DQ4
M_B DQ5	6	DQ5
M_B DQ6	16	DQ6
M_B DQ7	18	DQ7
M_B DQ8	21	DQ8
M_B DQ9	23	DQ9
M_B DQ10	33	DQ10
M_B DQ11	35	DQ11
M_B DQ12	22	DQ12
M_B DQ13	24	DQ13
M_B DQ14	34	DQ14
M_B DQ15	36	DQ15
M_B DQ16	38	DQ16
M_B DQ17	41	DQ17
M_B DQ18	51	DQ18
M_B DQ19	53	DQ19
M_B DQ20	40	DQ20
M_B DQ21	42	DQ21
M_B DQ22	50	DQ22
M_B DQ23	52	DQ23
M_B DQ24	57	DQ24
M_B DQ25	59	DQ25
M_B DQ26	67	DQ26
M_B DQ27	69	DQ27
M_B DQ28	56	DQ28
M_B DQ29	58	DQ29
M_B DQ30	68	DQ30
M_B DQ31	70	DQ31
M_B DQ32	129	DQ32
M_B DQ33	131	DQ33
M_B DQ34	141	DQ34
M_B DQ35	143	DQ35
M_B DQ36	130	DQ36
M_B DQ37	132	DQ37
M_B DQ38	140	DQ38
M_B DQ39	142	DQ39
M_B DQ40	147	DQ40
M_B DQ41	149	DQ41
M_B DQ42	157	DQ42
M_B DQ43	159	DQ43
M_B DQ44	146	DQ44
M_B DQ45	148	DQ45
M_B DQ46	158	DQ46
M_B DQ47	160	DQ47
M_B DQ48	163	DQ48
M_B DQ49	165	DQ49
M_B DQ50	175	DQ50
M_B DQ51	177	DQ51
M_B DQ52	164	DQ52
M_B DQ53	166	DQ53
M_B DQ54	174	DQ54
M_B DQ55	176	DQ55
M_B DQ56	181	DQ56
M_B DQ57	183	DQ57
M_B DQ58	191	DQ58
M_B DQ59	193	DQ59
M_B DQ60	180	DQ60
M_B DQ61	182	DQ61
M_B DQ62	192	DQ62
M_B DQ63	194	DQ63
M_B DQS#0	10	DQS#0
M_B DQS#1	27	DQS#1
M_B DQS#2	45	DQS#2
M_B DQS#3	63	DQS#3
M_B DQS#4	81	DQS#4
M_B DQS#5	99	DQS#5
M_B DQS#6	117	DQS#6
M_B DQS#7	135	DQS#7
M_B DQS#0	12	DQS#0
M_B DQS#1	29	DQS#1
M_B DQS#2	47	DQS#2
M_B DQS#3	64	DQS#3
M_B DQS#4	82	DQS#4
M_B DQS#5	100	DQS#5
M_B DQS#6	118	DQS#6
M_B DQS#7	136	DQS#7
M_B DQS#0	12	DQS#0
M_B DQS#1	29	DQS#1
M_B DQS#2	47	DQS#2
M_B DQS#3	64	DQS#3
M_B DQS#4	82	DQS#4
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M_B DQS#6	118	DQS#6
M_B DQS#7	136	DQS#7

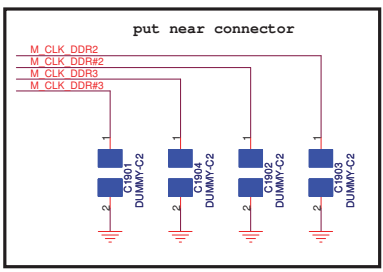
Change CONN
2009/06/01

NP1	NP1
NP2	NP2
RAS#	M_B_RAS# [10]
WE#	M_B_WE# [10]
CAS#	M_B_CAS# [10]
CS0#	M_CS2# [10]
CS1#	M_CS3# [10]
CKE0	M_CKE2 [10]
CKE1	M_CKE3 [10]
CK0	M_CLK_DDR2
CK0#	M_CLK_DDR#2 [10]
CK1	M_CLK_DDR3
CK1#	M_CLK_DDR#3 [10]
DM0	M_B_DM0
DM1	M_B_DM1
DM2	M_B_DM2
DM3	M_B_DM3
DM4	M_B_DM4
DM5	M_B_DM5
DM6	M_B_DM6
DM7	M_B_DM7
SDA	PCH_SMBDATA <<<>>> PCH_SMBDATA [7,18,23,40,64,76]
SCL	PCH_SMBCLK <<<>>> PCH_SMBCLK [7,18,23,40,64,76]
EVENT#	PM_EXTS#1 [9]
VDDSPD	
SA0	SA0_DM2
SA1	SA1_DM2
NC#1	77 X
NC#2	122 X
NC#TEST	125 X
VDD1	75
VDD2	76
VDD3	81
VDD4	82
VDD5	87
VDD6	88
VDD7	84
VDD8	99
VDD9	100
VDD10	105
VDD11	106
VDD12	111
VDD13	112
VDD14	117
VDD15	118
VDD16	123
VDD17	124
VSS	2
VSS	3
VSS	8
VSS	9
VSS	13
VSS	14
VSS	19
VSS	20
VSS	25
VSS	26
VSS	31
VSS	32
VSS	37
VSS	38
VSS	43
VSS	44
VSS	48
VSS	49
VSS	54
VSS	55
VSS	60
VSS	61
VSS	65
VSS	66
VSS	71
VSS	72
VSS	127
VSS	128
VSS	133
VSS	134
VSS	138
VSS	139
VSS	144
VSS	145
VSS	150
VSS	151
VSS	155
VSS	156
VSS	161
VSS	162
VSS	167
VSS	168
VSS	172
VSS	173
VSS	178
VSS	179
VSS	184
VSS	185
VSS	189
VSS	190
VSS	195
VSS	196
VSS	205
VSS	206



Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
If SA0_DIM0 = 0, SA1_DIM0 = 1
SO-DIMMA SPD Address is 0xA4

Height 9.2mm



1st Samsung

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **DDRIII-SODIMM SLOT2**

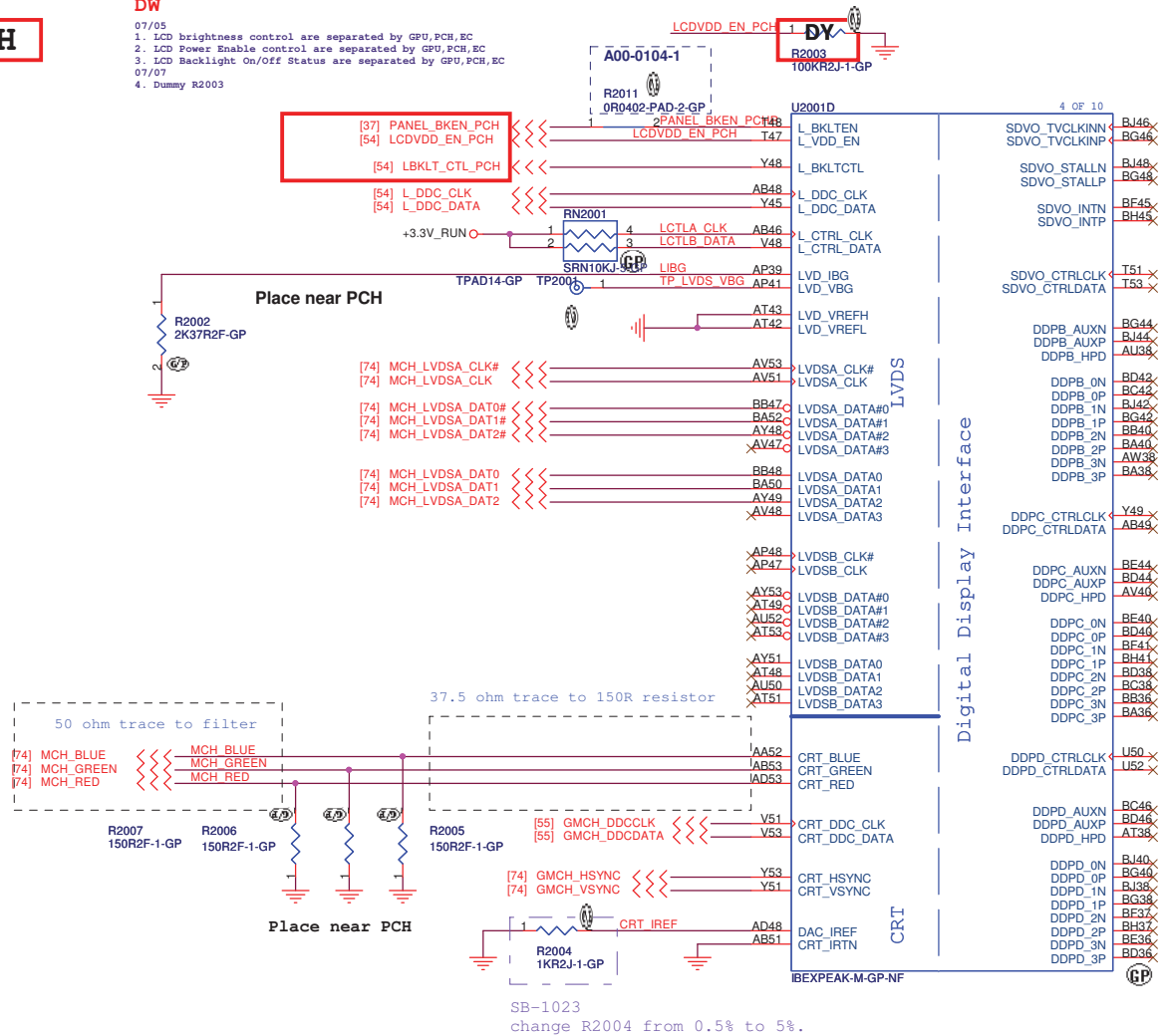
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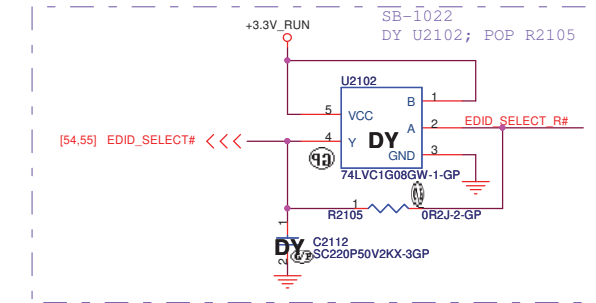
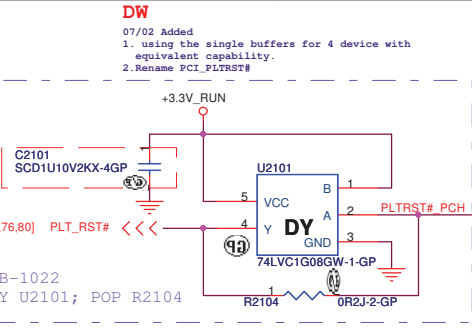
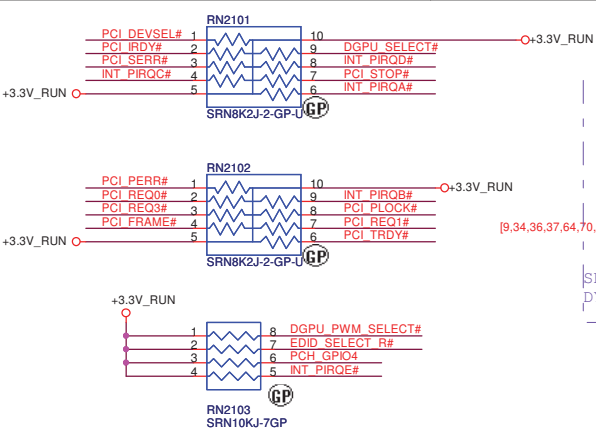
Date: Wednesday, January 13, 2010 Sheet 19 of 88

SSID = PCH

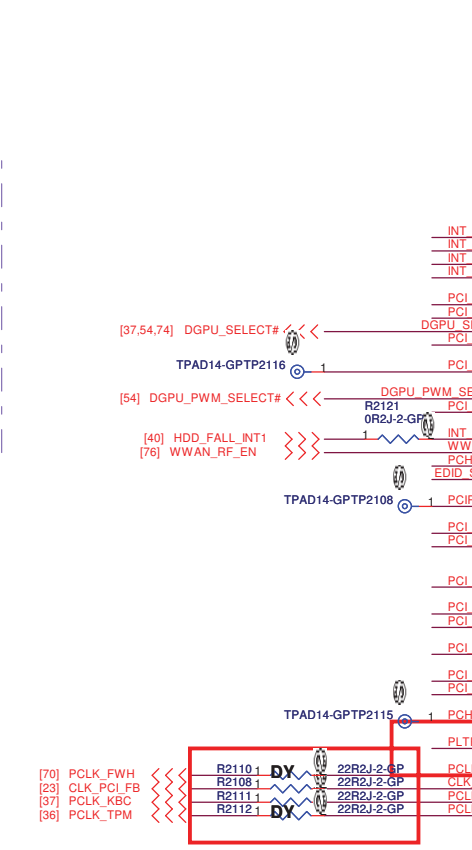
DW

- 07/05
- 1. LCD brightness control are separated by GPU,PCH,EC
- 2. LCD Power Enable control are separated by GPU,PCH,EC
- 3. LCD Backlight On/Off Status are separated by GPU,PCH,EC
- 07/07
- 4. Dummy R2003

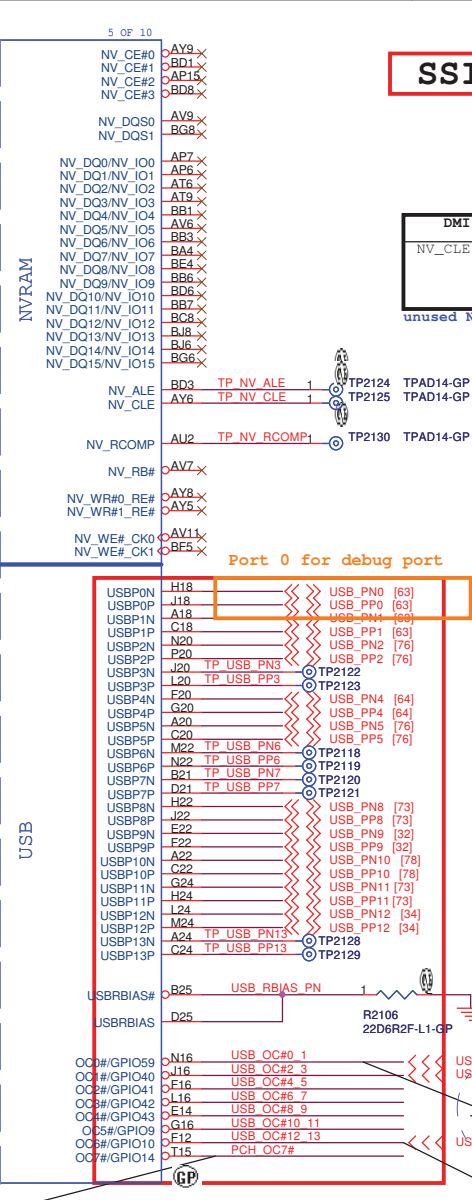
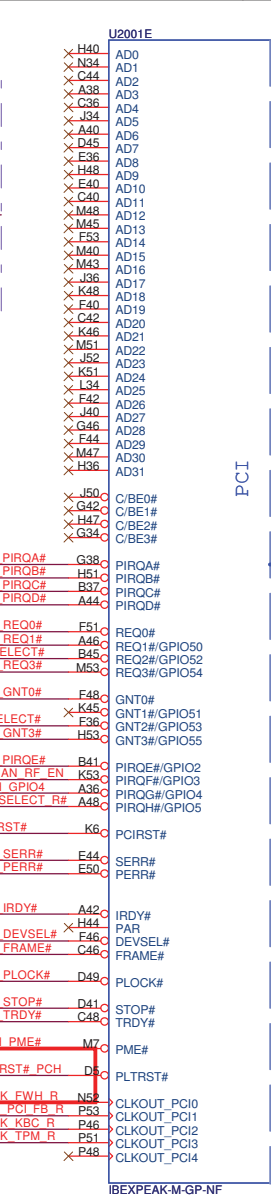
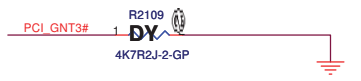




BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	PCI
1	1	SPI (Default)



A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default



SSID = PCH

DMI Termination Voltage	
NV_CLE	Set to Vss when low. Set to Vcc when high. Low = Default

unused NV_SLE strap

Port 0 for debug port

USB	
Pair	Device
0	USB1
1	USB for ESATA
2	USB2
3	RESERVE
4	WLAN
5	WWAN
6	RESERVED (Not available for HM55)
7	RESERVED (Not available for HM55)
8	BLUETOOTH
9	Card Reader
10	Biometric
11	CAMERA
12	New Card
13	RESERVED

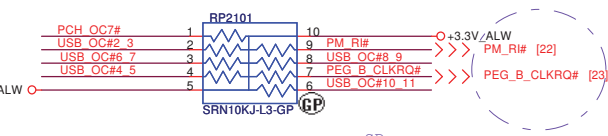
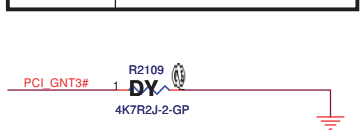
Pull up in page 22 for layout convenience
swap net for layout

Pull up in page 23 for layout convenience

Calpella Platform Design Guide
Revision 1.6

Table 111. Overcurrent Pin Example Configuration

These OC7# pins are not used for USB overcurrent protection and should be configured as GPIOs. The unused USB ports can be left as no connect.



1st Samsung

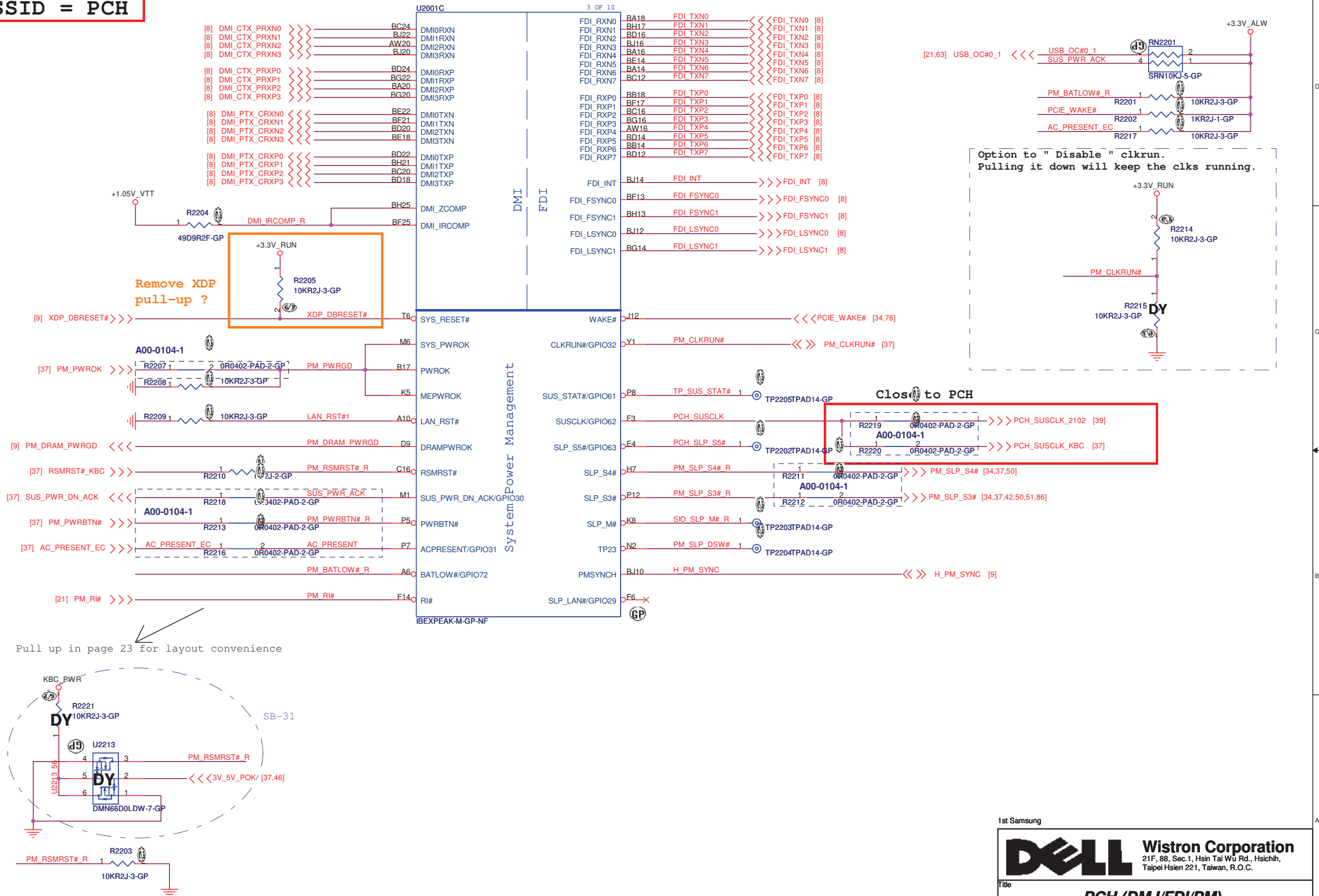
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (PCI/USB/NVRAM)**

Size: _____ Document Number: _____ Rev: **A00**

Date: Wednesday, January 13, 2010 Sheet 21 of 88

SSID = PCH



1st Samsung

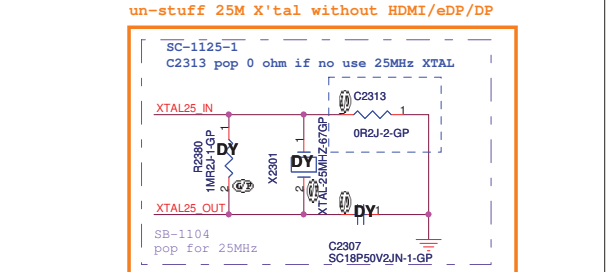
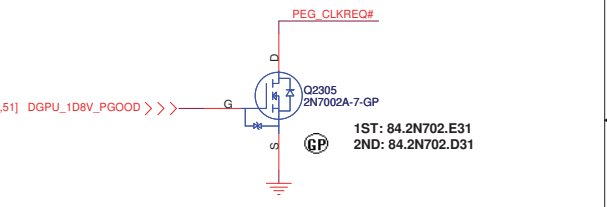
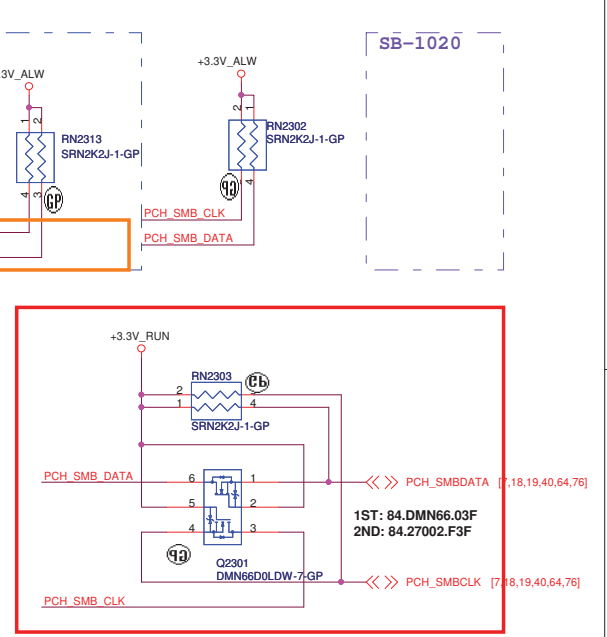
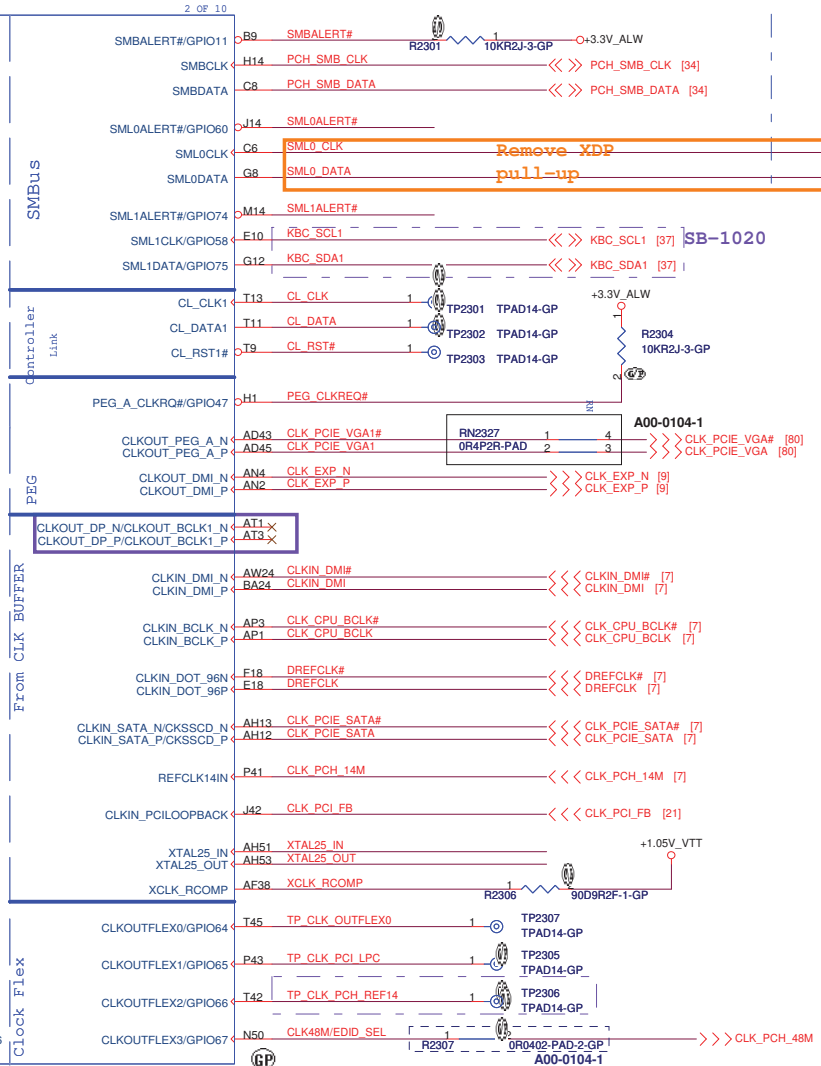
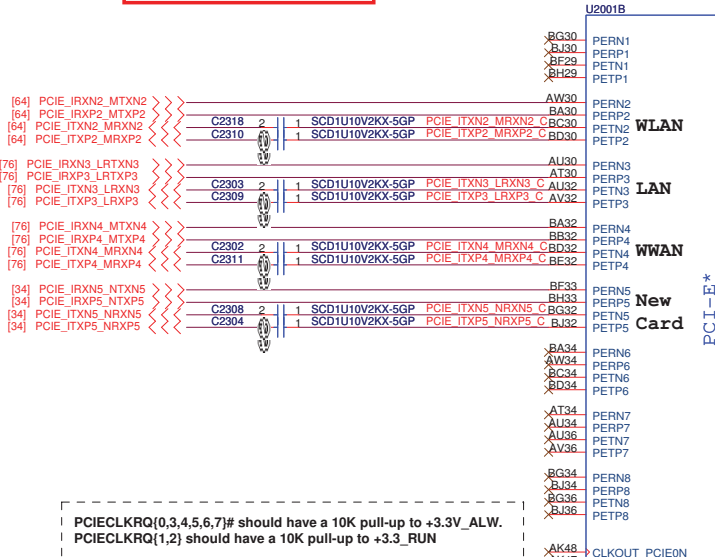
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (DM I/FDI/PM)**

Size: Document Number: **Winery13 MB DIS** Rev: **A00**

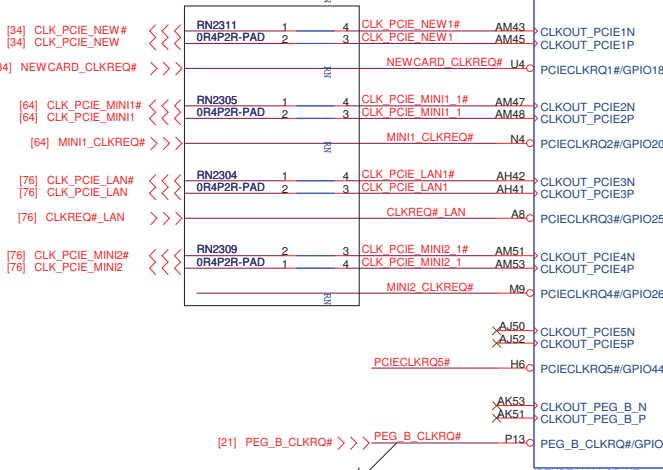
Date: Wednesday, January 13, 2010 Sheet 22 of 88

SSID = PCH

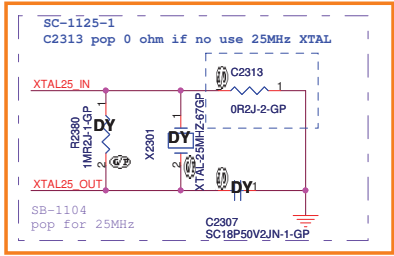
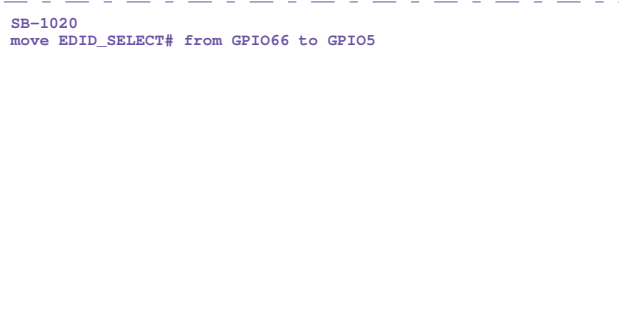
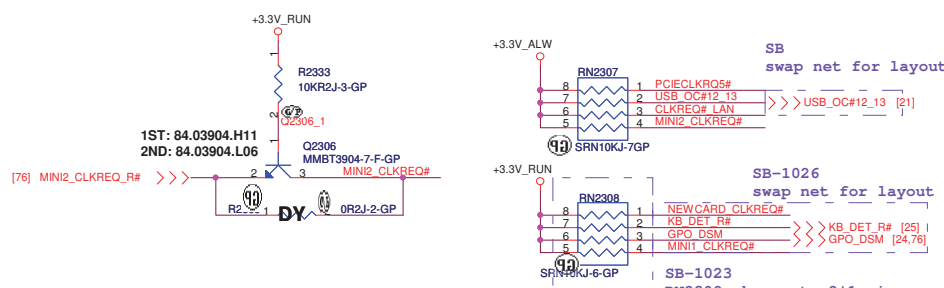


PCIECLKRQ(0,3,4,5,6,7)# should have a 10K pull-up to +3.3V_ALW.
PCIECLKRQ(1,2) should have a 10K pull-up to +3.3V_RUN

A00-0104-1



Pull up in page 21 for layout convenience



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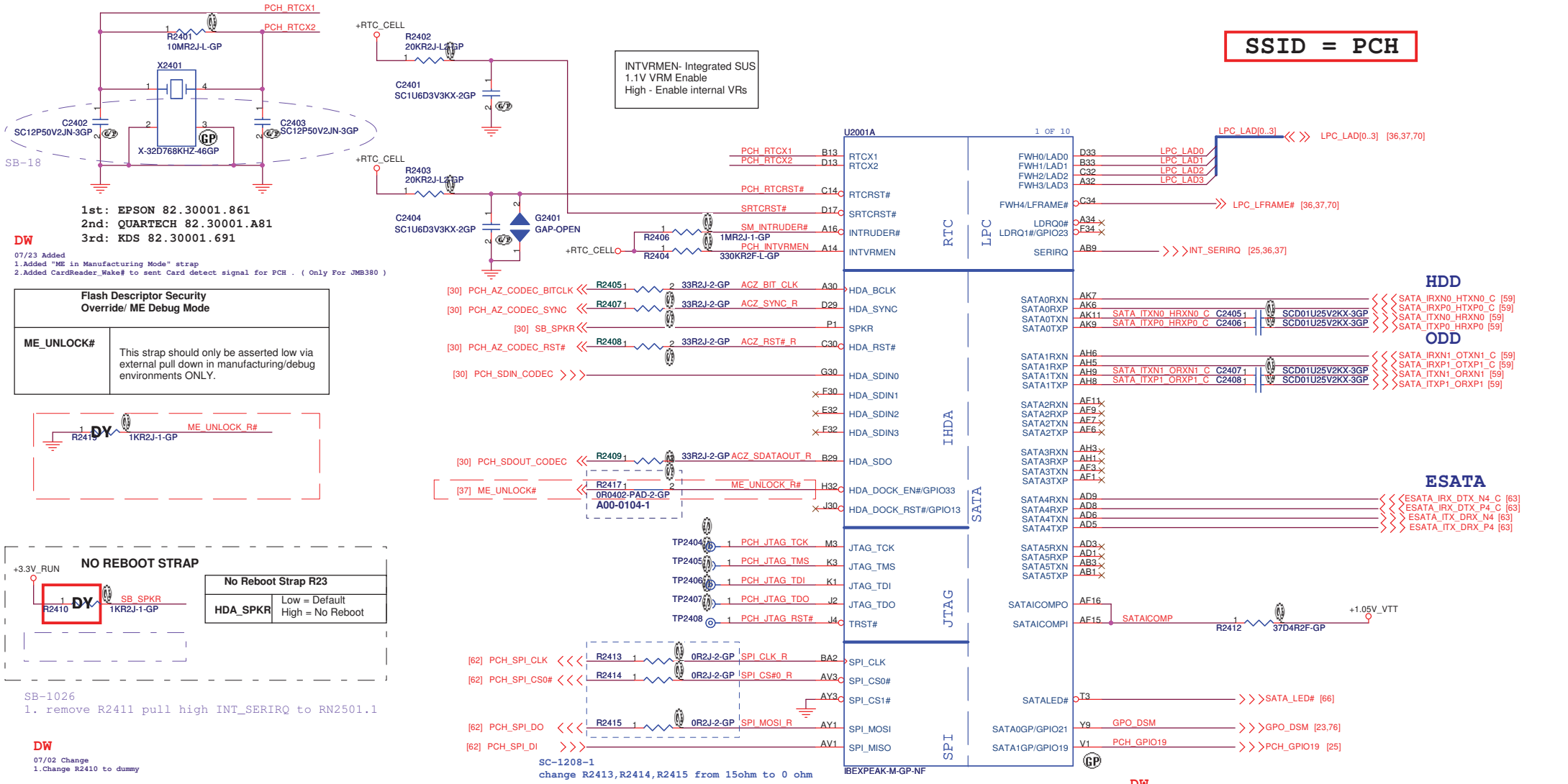
Title: **PCH (PCI-E/SMBUS/CLOCK/CL)**

Size: _____ Document Number _____ Rev _____

Winery13 MB DIS A00

Date: Wednesday, January 13, 2010 Sheet 23 of 88

SSID = PCH

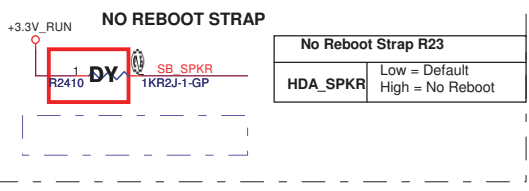
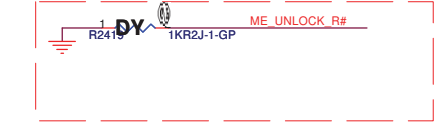


DW
07/23 Added
1. Added "ME in Manufacturing Mode" strap
2. Added CardReader_Wake# to sent Card detect signal for PCH . (Only For JMB380)

Flash Descriptor Security Override/ ME Debug Mode

ME_UNLOCK#

This strap should only be asserted low via external pull down in manufacturing/debug environments ONLY.



SB-1026
1. remove R2411 pull high INT_SERIRQ to RN2501.1

DW
07/02 Change
1. Change R2410 to dummy



DW
07/10 assign GPIO
1. assign GPIO GPIO_DSM, Felic_DETECT#

1st Samsung

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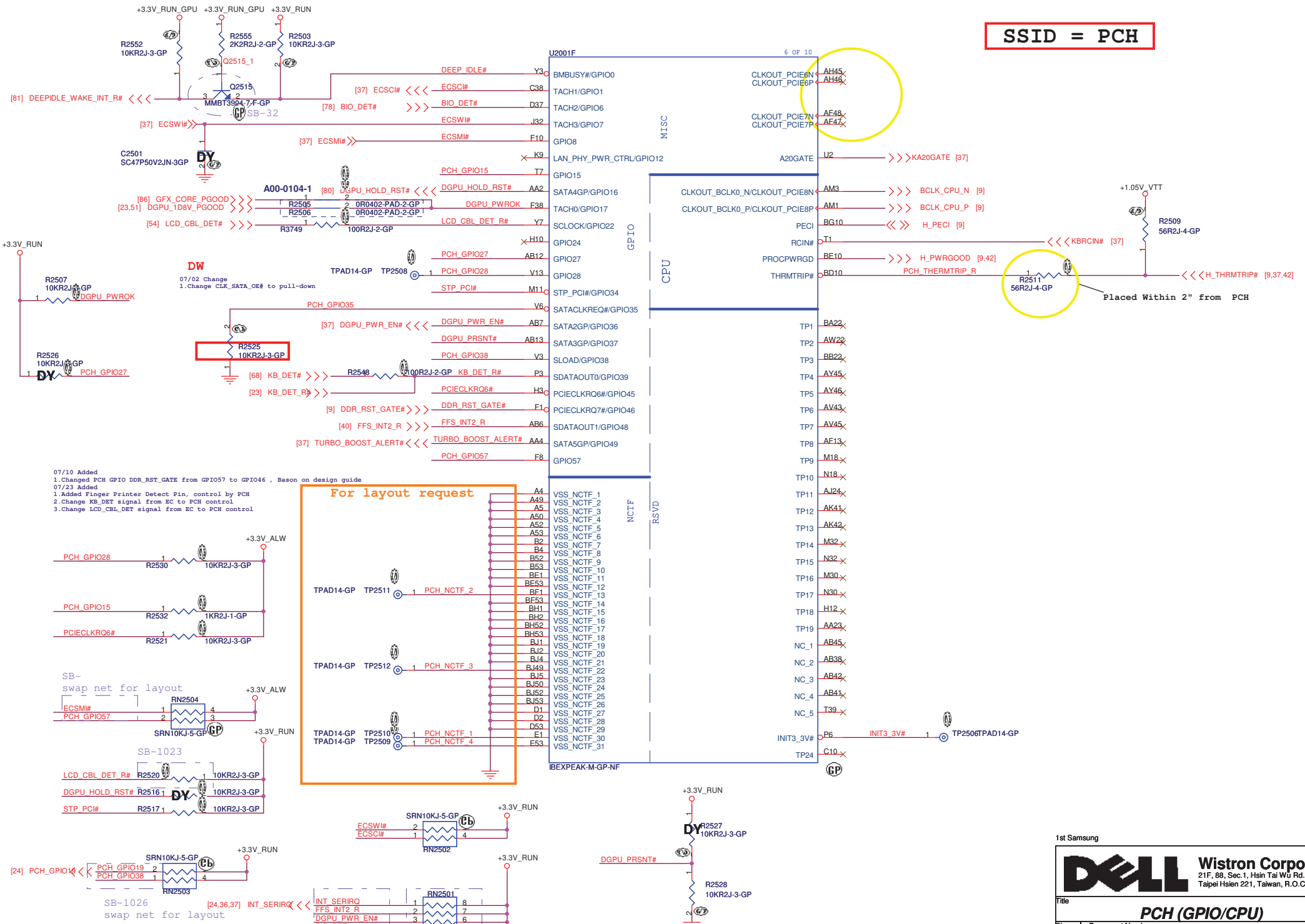
Title: **PCH (SPI/RTC/LPC/SATA/IHDA)**

Size: Document Number

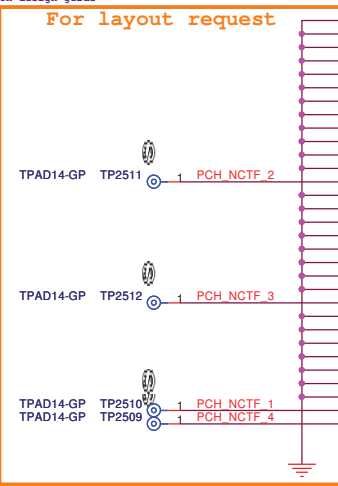
Rev: **A00**

Date: Wednesday, January 13, 2010 Sheet 24 of 88

SSID = PCH



07/10 Added
07/23 Added
1.Changed PCH GPIO DDR_RST_GATE from GPIO57 to GPIO46 , Based on design guide
1.Added Finger Printer Detect Pin, control by PCH
2.Change KB_DET signal from EC to PCH control
3.Change LCD_CBL_DET signal from EC to PCH control



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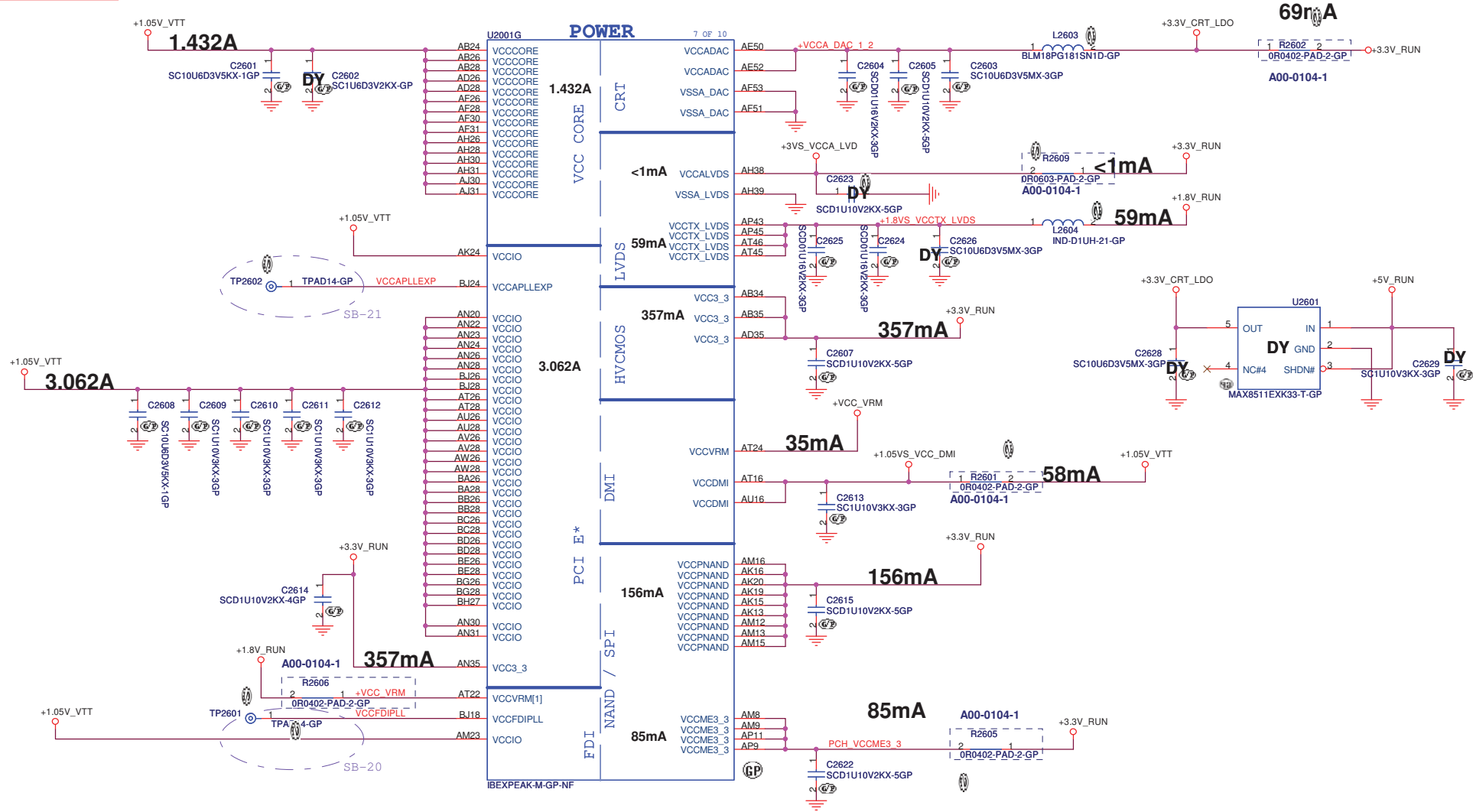
Title: **PCH (GPIO/CPU)**

Size	Document Number	Rev
		A00

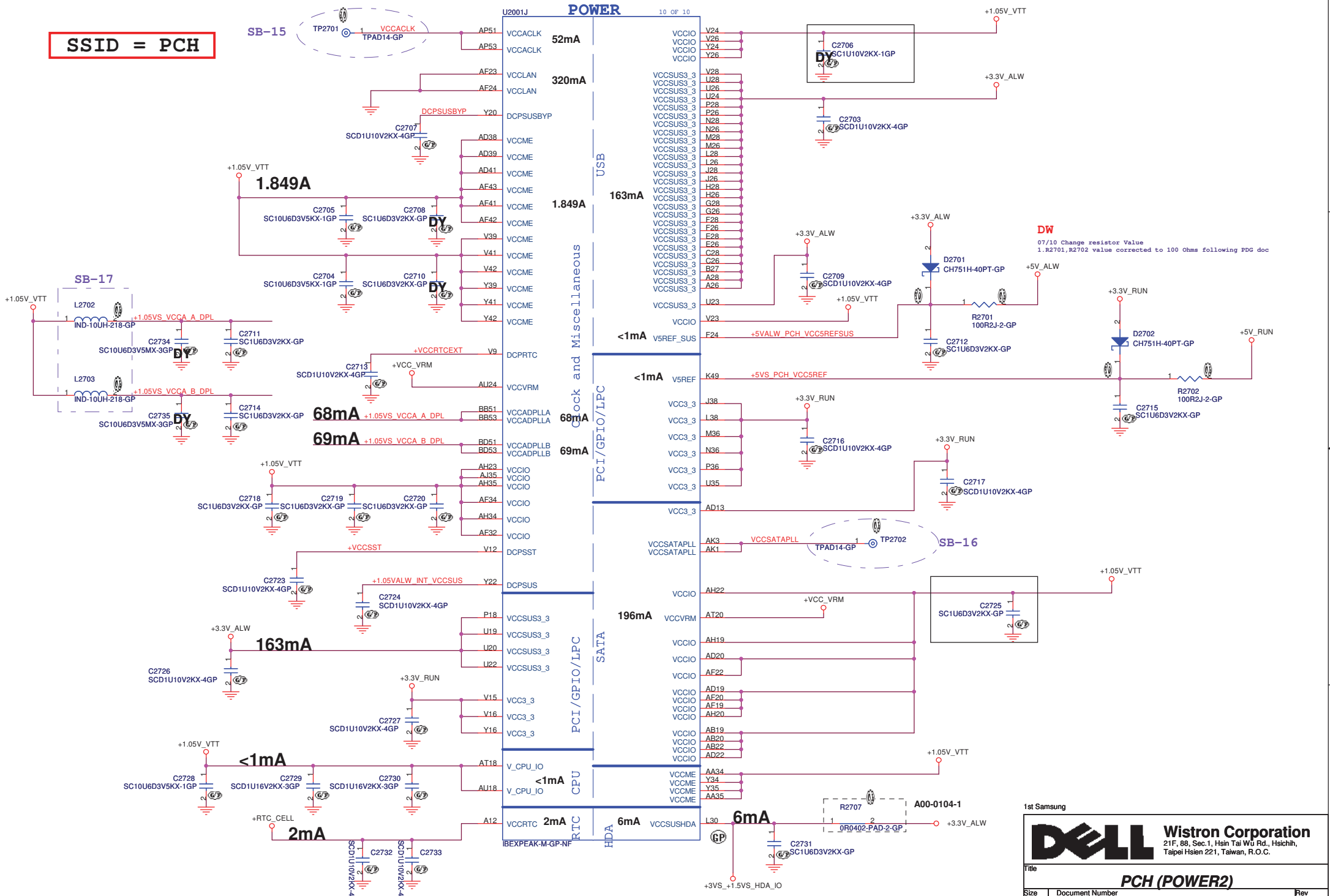
Date: Wednesday, January 13, 2010 Sheet 25 of 88

<http://laptop-motherboard-schematic.blogspot.com/>

SSID = PCH



SSID = PCH



<http://laptop-motherboard-schematic.blogspot.com/>

1st Samsung

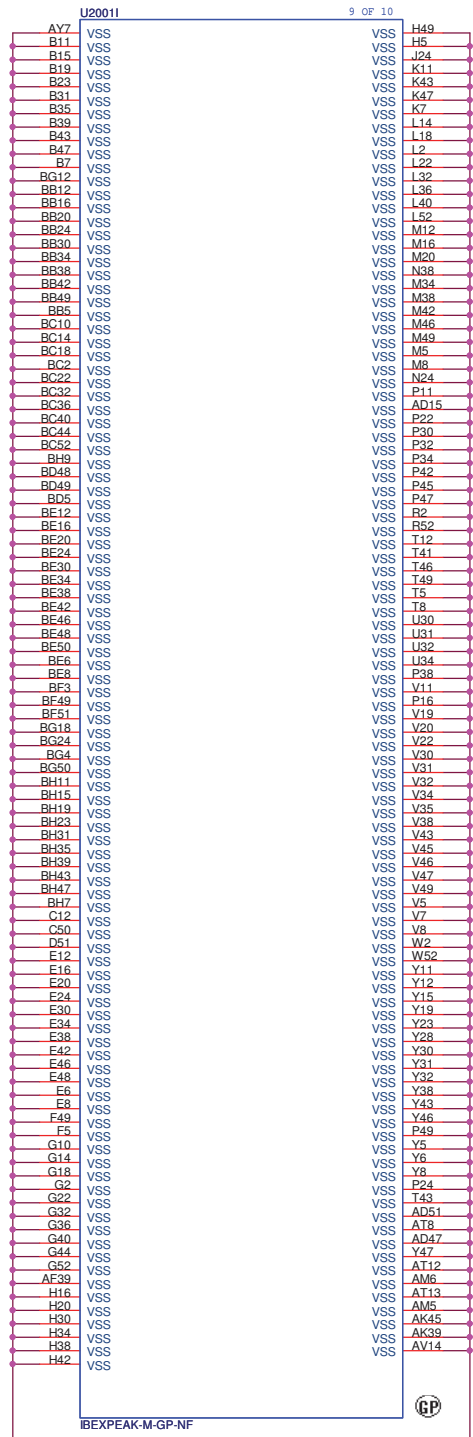
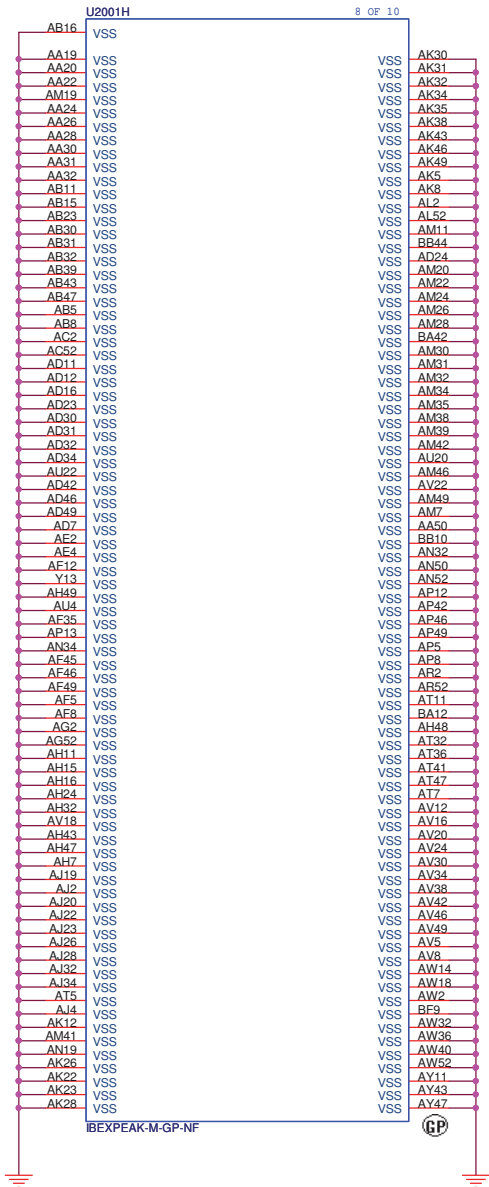
DELL Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **PCH (POWER2)**

Size	Document Number	Rev
		A00

Date: Wednesday, January 13, 2010 Sheet 27 of 88

SSID = PCH



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1st Samsung




Title			PCH (VSS)		
Size	Document Number	Rev			A00
Date:	Wednesday, January 13, 2010	Sheet	28	of	88

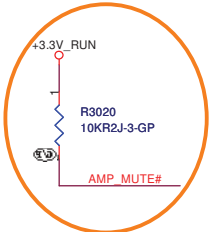
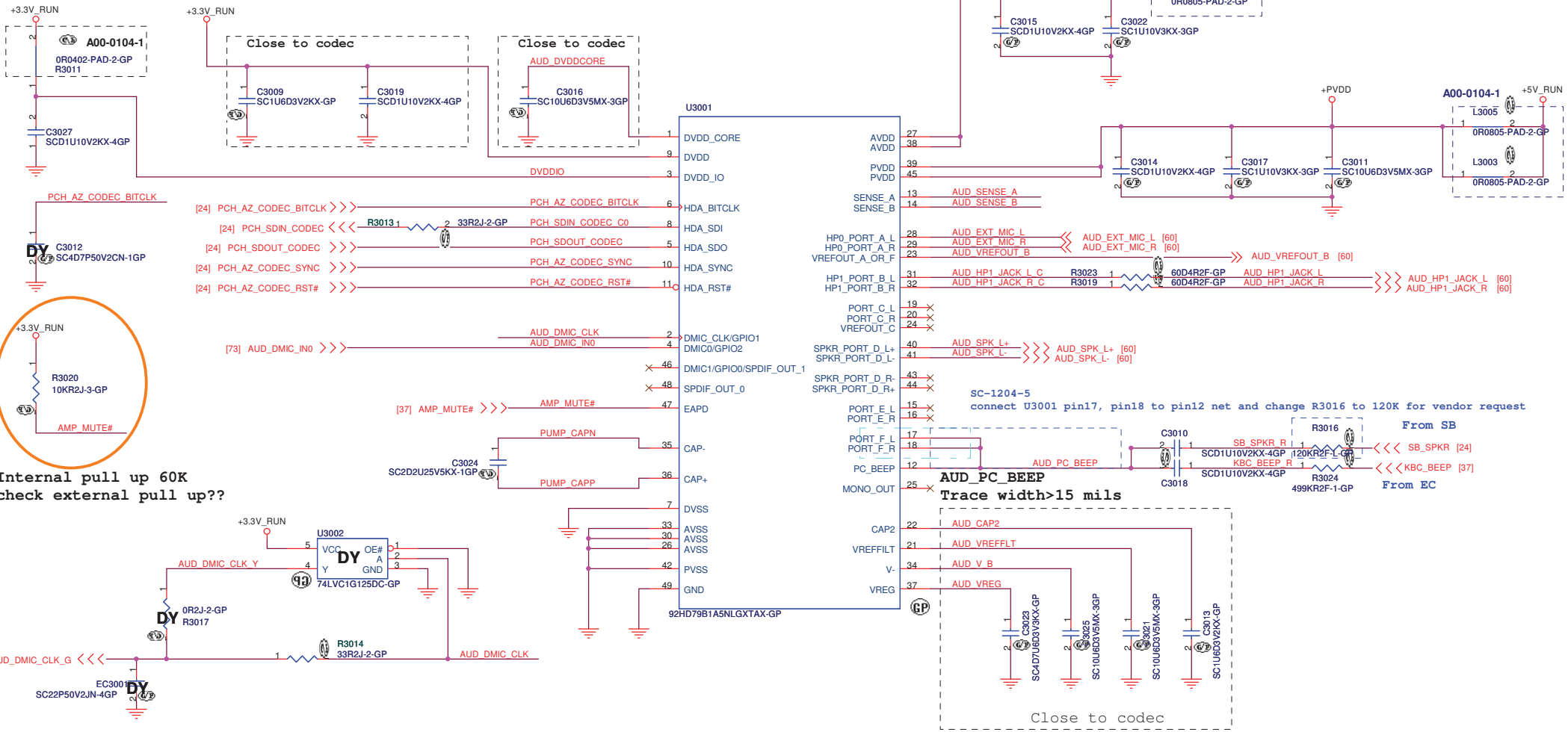
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<http://laptop-motherboard-schematic.blogspot.com/>

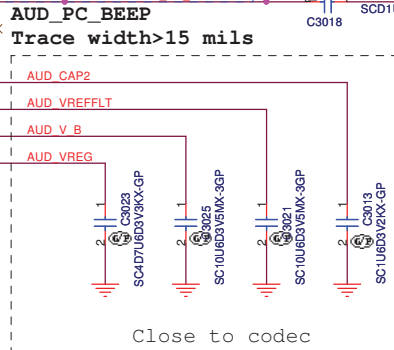
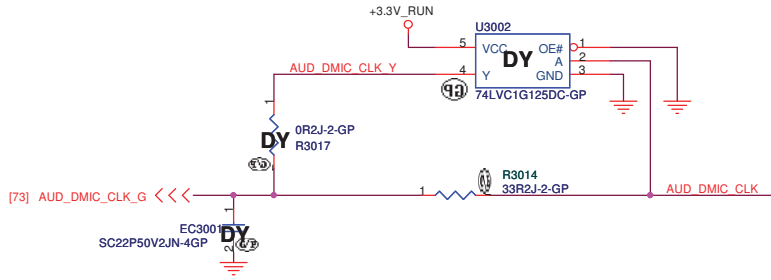
1st Samsung

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Title					
(Reserve)					
Size	Document Number				Rev
Custom	Winery13 MB DIS				A00
Date: Wednesday, January 13, 2010					
Sheet 29 of 88					

SSID = AUDIO

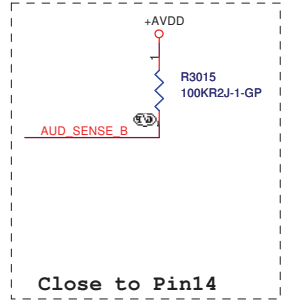
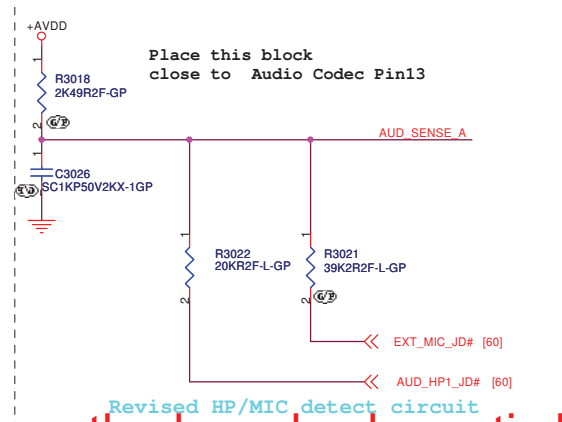
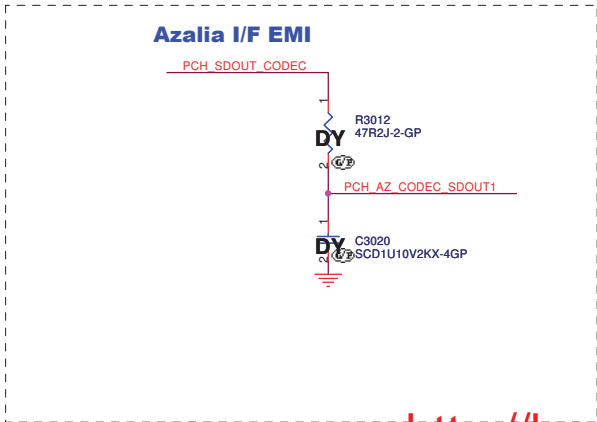


Internal pull up 60K
check external pull up??



sc-1204-5
connect U3001 pin17, pin18 to pin12 net and change R3016 to 120K for vendor request

AUD_PC_BEEP
Trace width > 15 mils



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Title: **AUDIO CODEC 92HD81**

Size A3	Document Number Winery13 MB DIS	Rev A00
Date: Wednesday, January 13, 2010	Sheet 30 of 88	

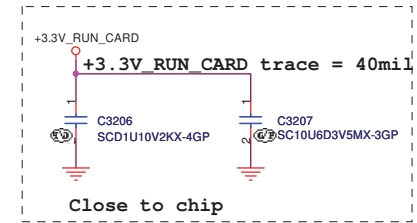
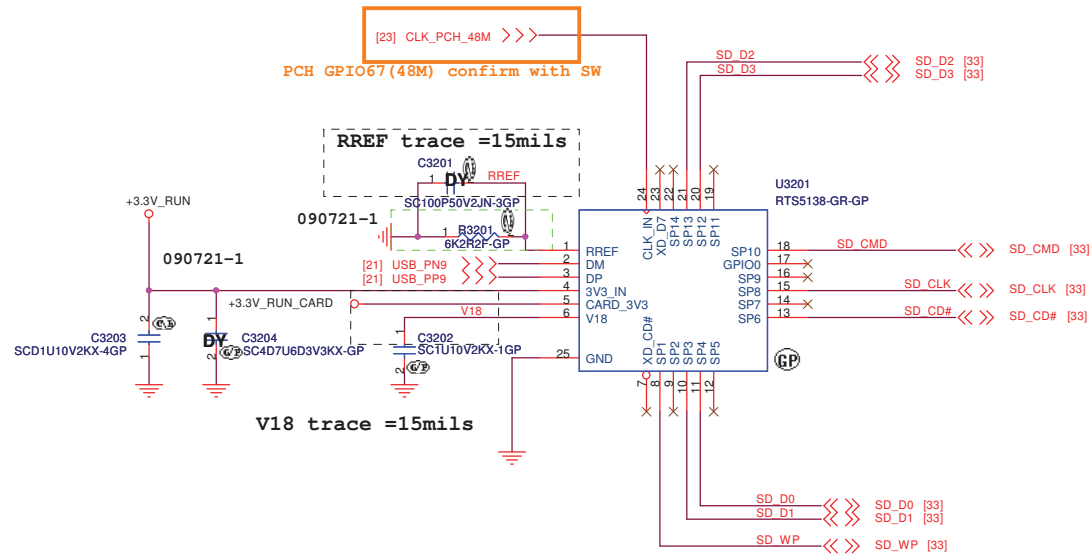
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Title					
(Reserve)					
Size	Document Number			Rev	
Custom	Winery13 MB DIS			A00	
Date: Wednesday, January 13, 2010			Sheet	31	of 88

SSID = SDIO



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1st Samsung

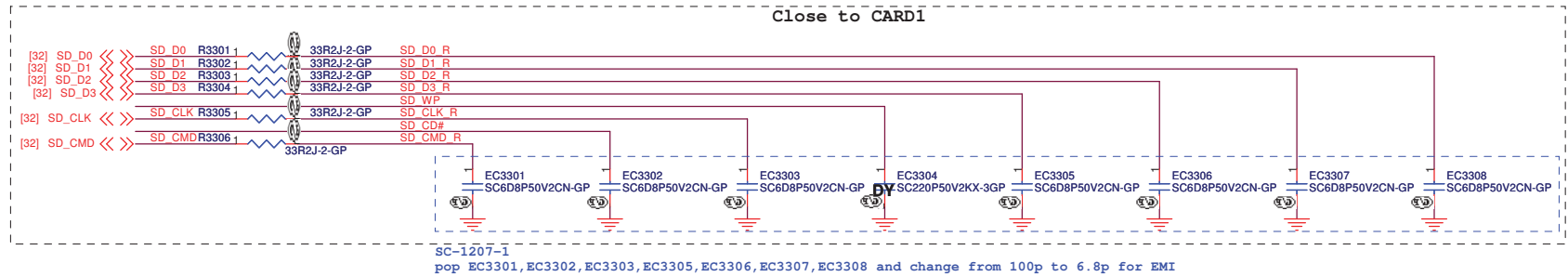
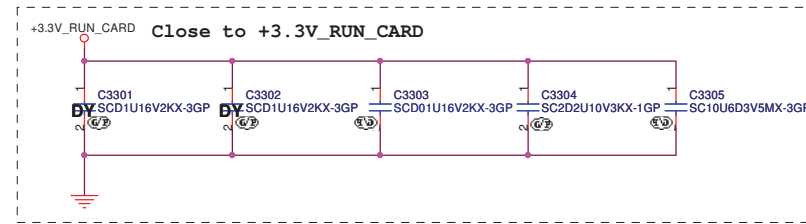
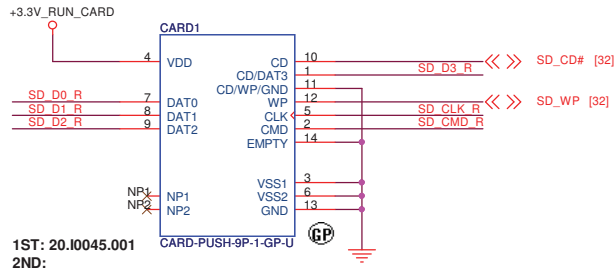
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title
CardReader/RTS5138

Size Custom	Document Number Winery13 MB DIS	Rev A00
Date: Wednesday, January 13, 2010	Sheet 32 of 88	

SSID = SDIO

SD/MMC/MMC+ Card Reader



SSID = 1394



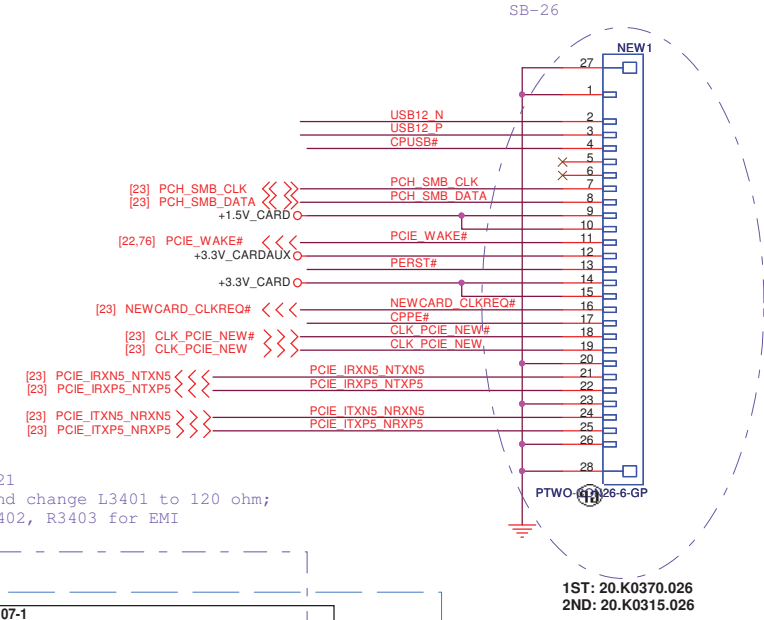
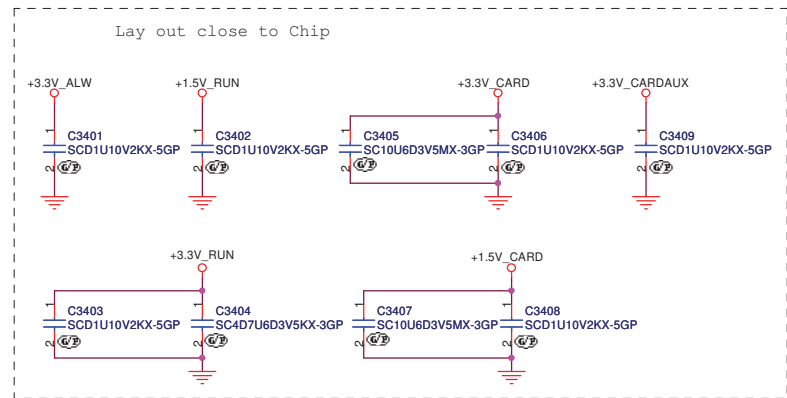
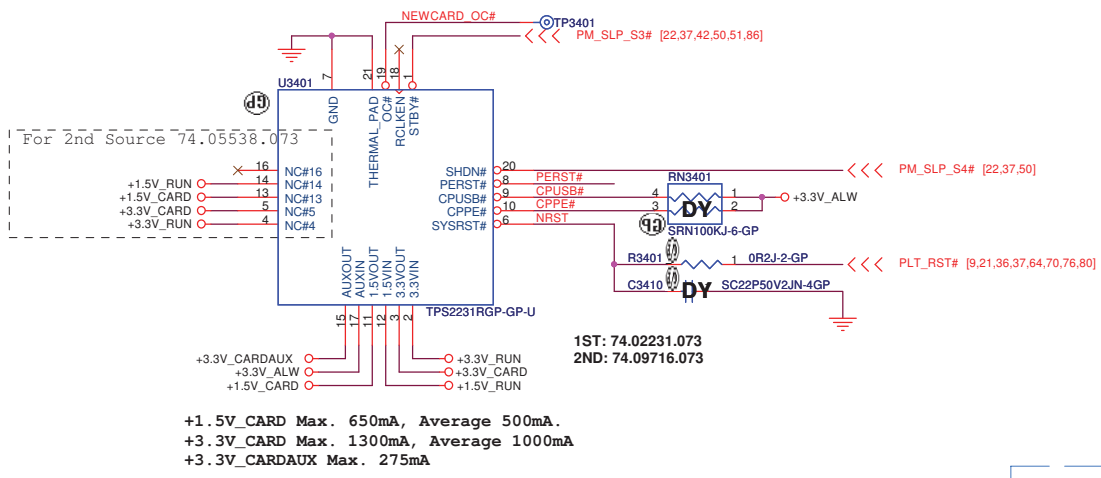
1st Samsung



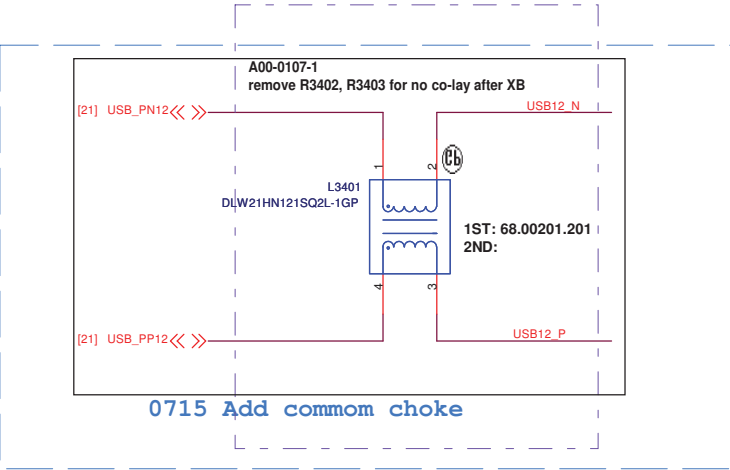
Title CARD READER CONN		
Size A3	Document Number Winery13 MB DIS	Rev A00
Date: Wednesday, January 13, 2010	Sheet 33	of 88

SSID = ExpressCard

+1.5V_CARD Max. 650mA, Average 500mA.
 +3.3V_CARD Max. 1300mA, Average 1000mA
 +3.3V_CARDAUX Max. 275mA



SB-1021
 pop and change L3401 to 120 ohm;
 DY R3402, R3403 for EMI



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 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ExpressCard**

Size: A3	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet: 34	of 88

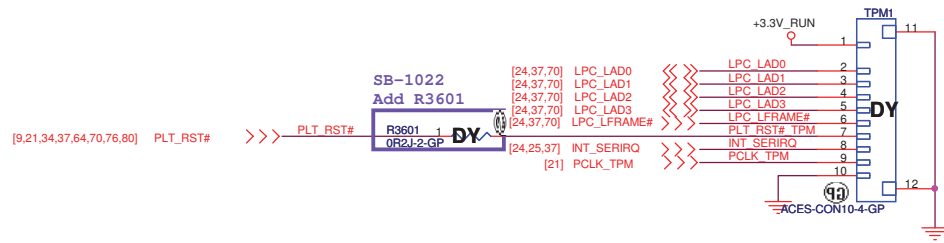
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1st Samsung

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Title		
(Reserve)		
Size	Document Number	Rev
A3	Winery13 MB DIS	A00
Date: Wednesday, January 13, 2010	Sheet 35 of	88

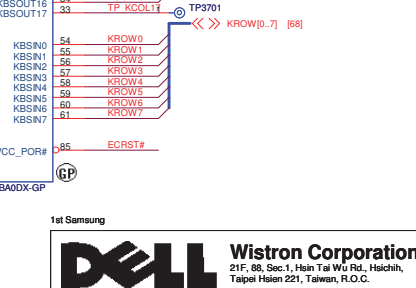
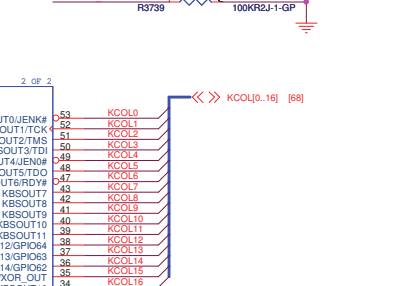
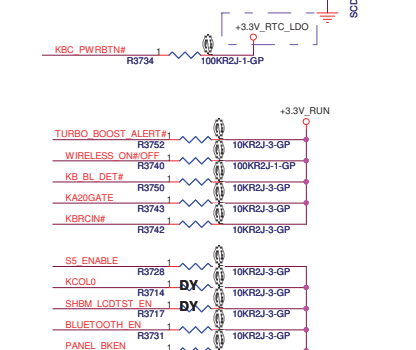
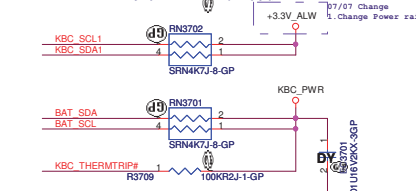
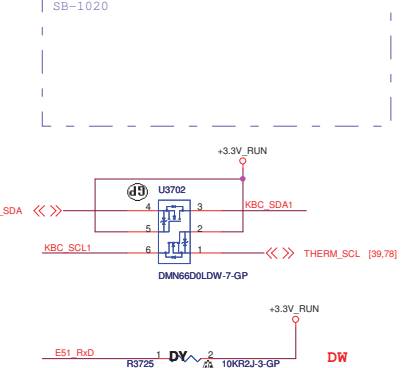
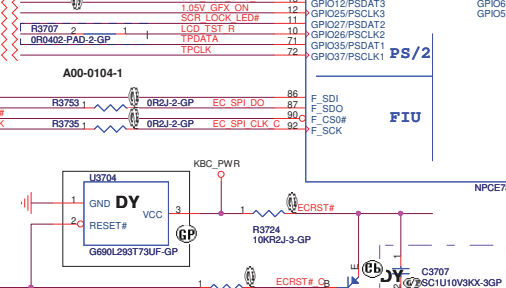
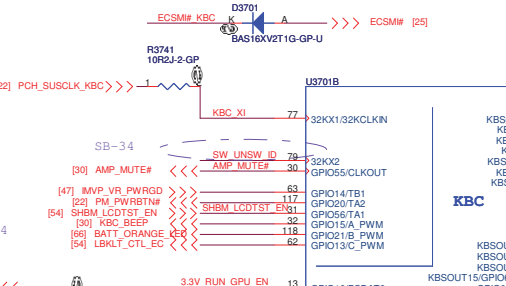
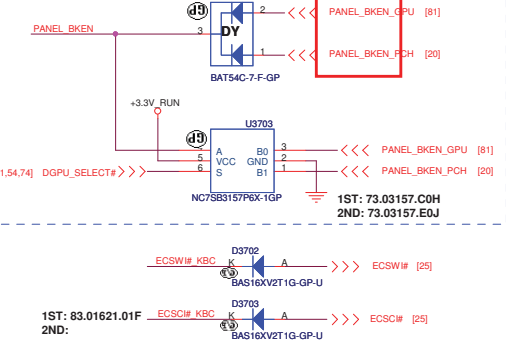
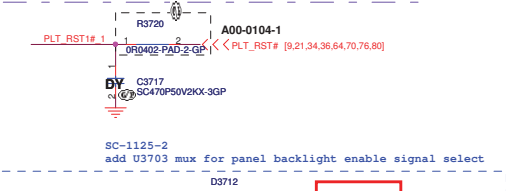
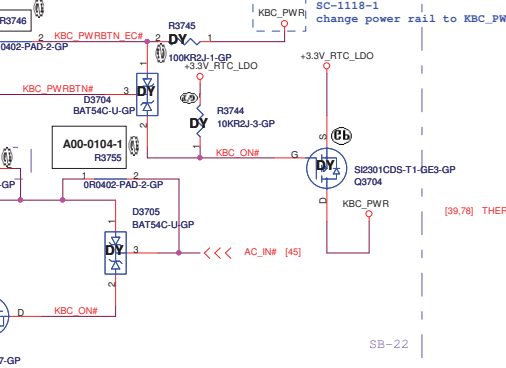
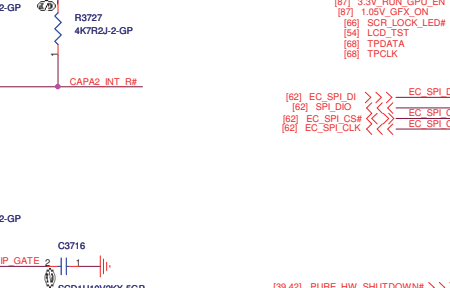
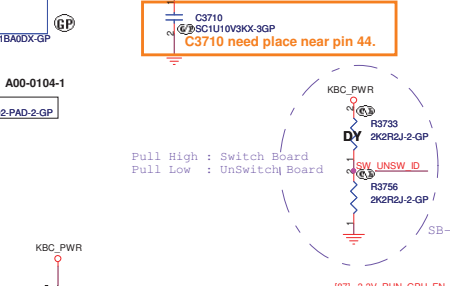
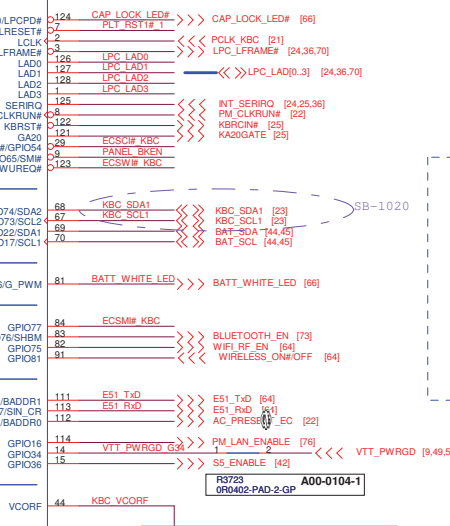
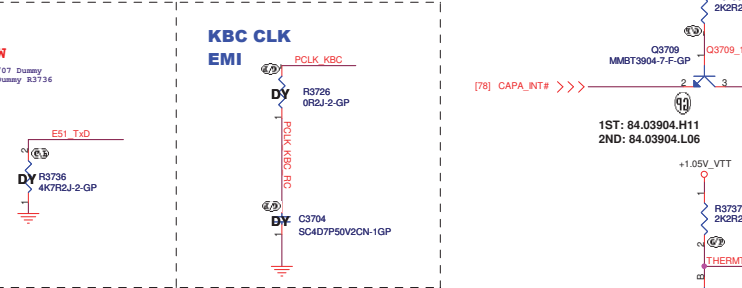
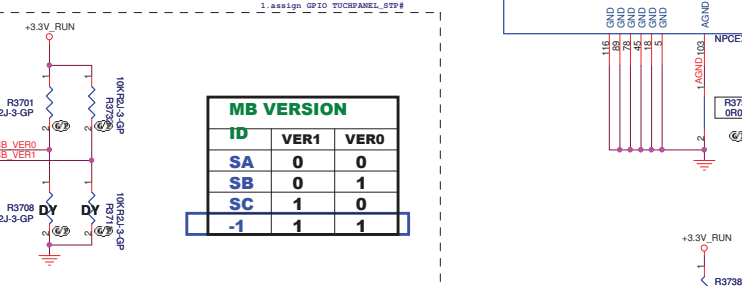
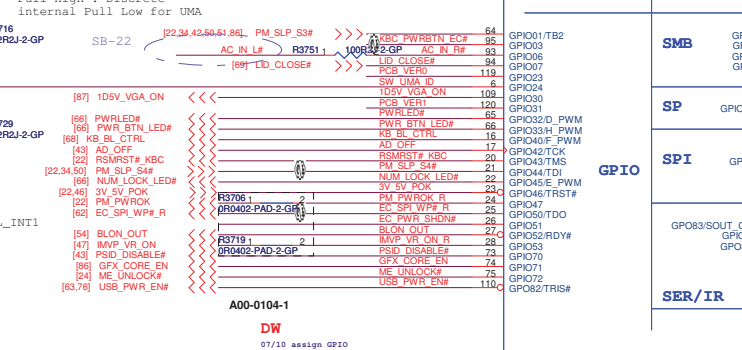
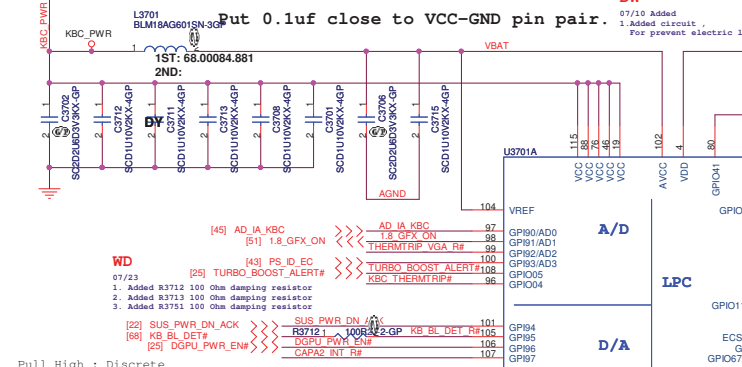
SSID = User.Interface

TPM board CONN



SC-1125-I
remove TPM AFTP

SSID = KBC




MB VERSION		
ID	VER1	VER0
SA	0	1
SB	0	1
SC	1	0
-1	1	1

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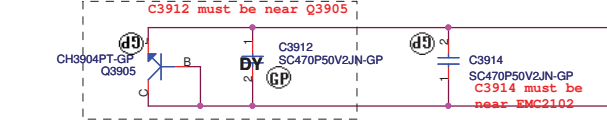
1st Samsung

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Title					
(Reserve)					
Size	Document Number				Rev
Custom	Winery13 MB DIS				A00
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SSID = Thermal

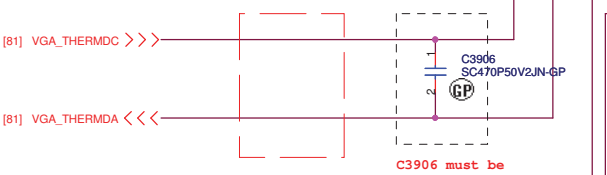
1. WWAN

1ST: 84.03904.P11
2ND: 84.03904.T11



Layout notice:
H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

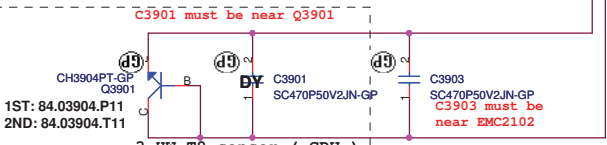
2. GPU Sensor



DW
07/23 Removed
1. Removed SYSTEM Sensor Critical

3. CPU Sensor

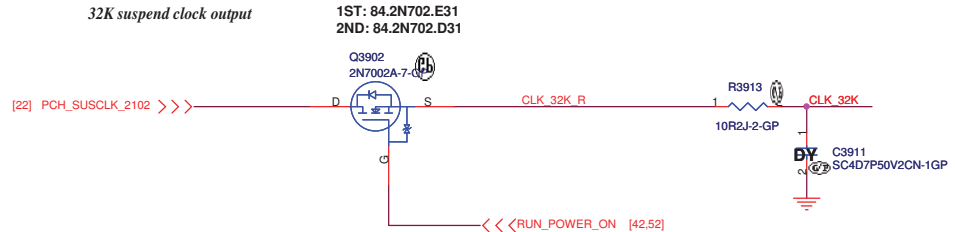
Layout notice :
Both VGA_THERMDA and THERMDC routing
10 mil trace width and 10 mil spacing.



3.HW T8 sensor (CPU)

Layout notice :
Both DN3 and DP3 routing 10 mil
trace width and 10 mil spacing.

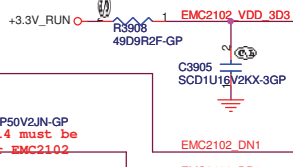
32K suspend clock output



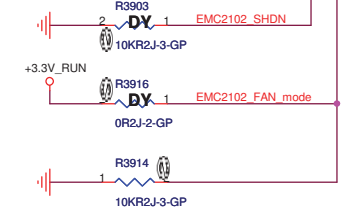
<http://laptop-motherboard-schematic.blogspot.com/>

DW

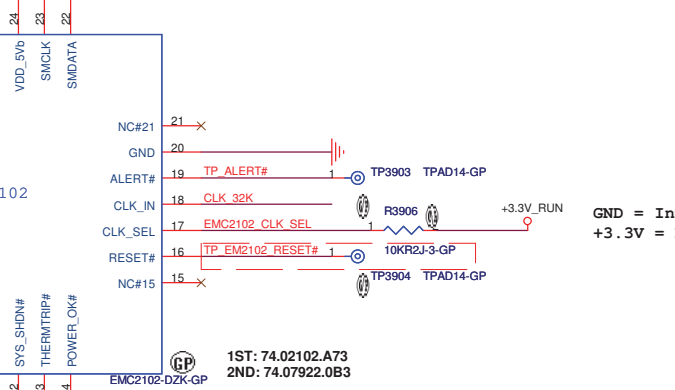
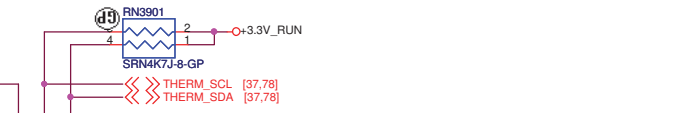
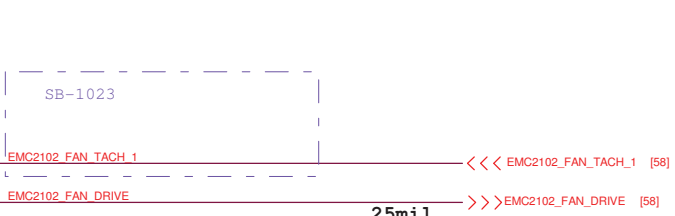
07/10 Del
1. Not reserve S5 power source rail for EMC2102 ??



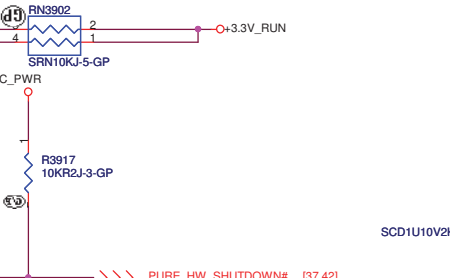
GND = Channel 1
OPEN = Channel 3
+3.3V = Disabled



GND = Fan is OFF
OPEN = Fan is at 60% full-scale
+3.3V = Fan is at 75% full-scale

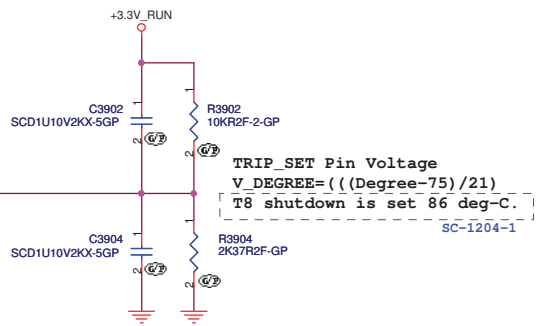


1ST: 74.02102.A73
2ND: 74.07922.0B3



1ST: 84.2N702.E31
2ND: 84.2N702.D31

GND = Internal Oscillator Selected
+3.3V = External 32.768kHz Clock Selected



TRIP_SET Pin Voltage
 $V_DEGREE = ((Degree-75)/21)$
T8 shutdown is set 86 deg-C.

DW

07/28 Removed
1. Removed U3902 AND gate.

1st Samsung

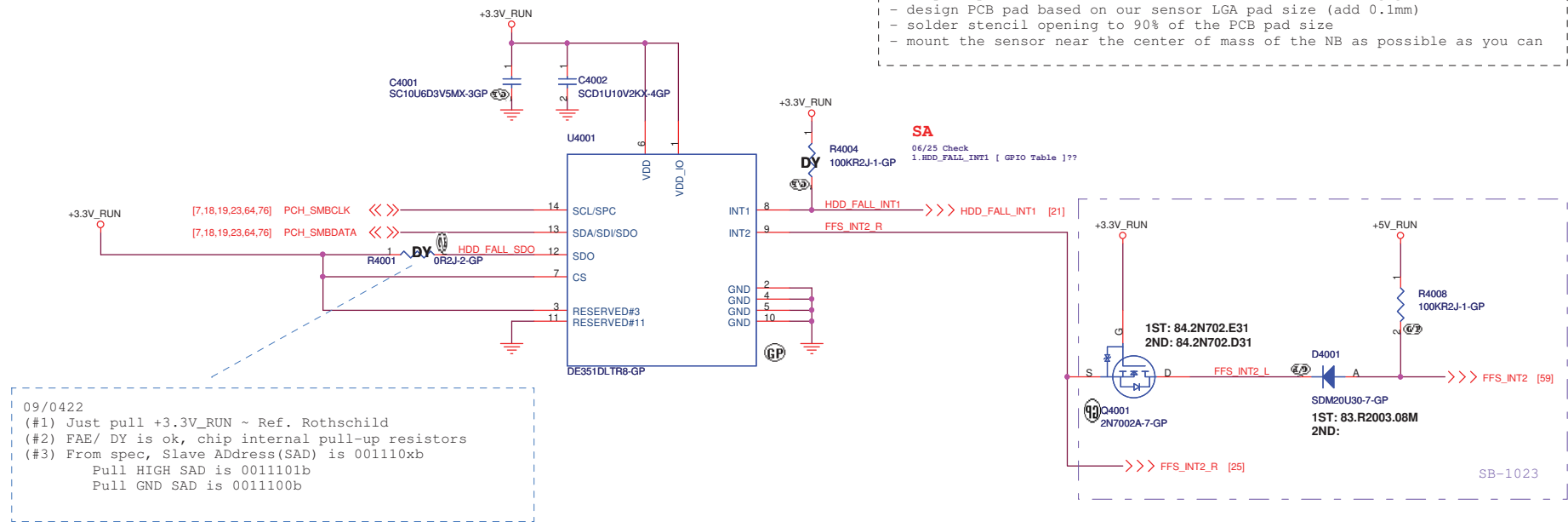


Title Thermal/Fan Controller EMC2102		
Size Custom	Document Number Winery13 MB DIS	Rev A00
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Free Fall Sensor

Note

- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



09/0422
 (#1) Just pull +3.3V_RUN ~ Ref. Rothschild
 (#2) FAE/ DY is ok, chip internal pull-up resistors
 (#3) From spec, Slave Address(SAD) is 001110xb
 Pull HIGH SAD is 0011101b
 Pull GND SAD is 0011100b

Note
 (1) Keep all signals are the same trace width. (included VDD, GND).
 (2) No VIA under IC bottom.

1st Samsung

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Title: **Free Fall Sensor**

Size: Custom	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010		Sheet 40 of 88

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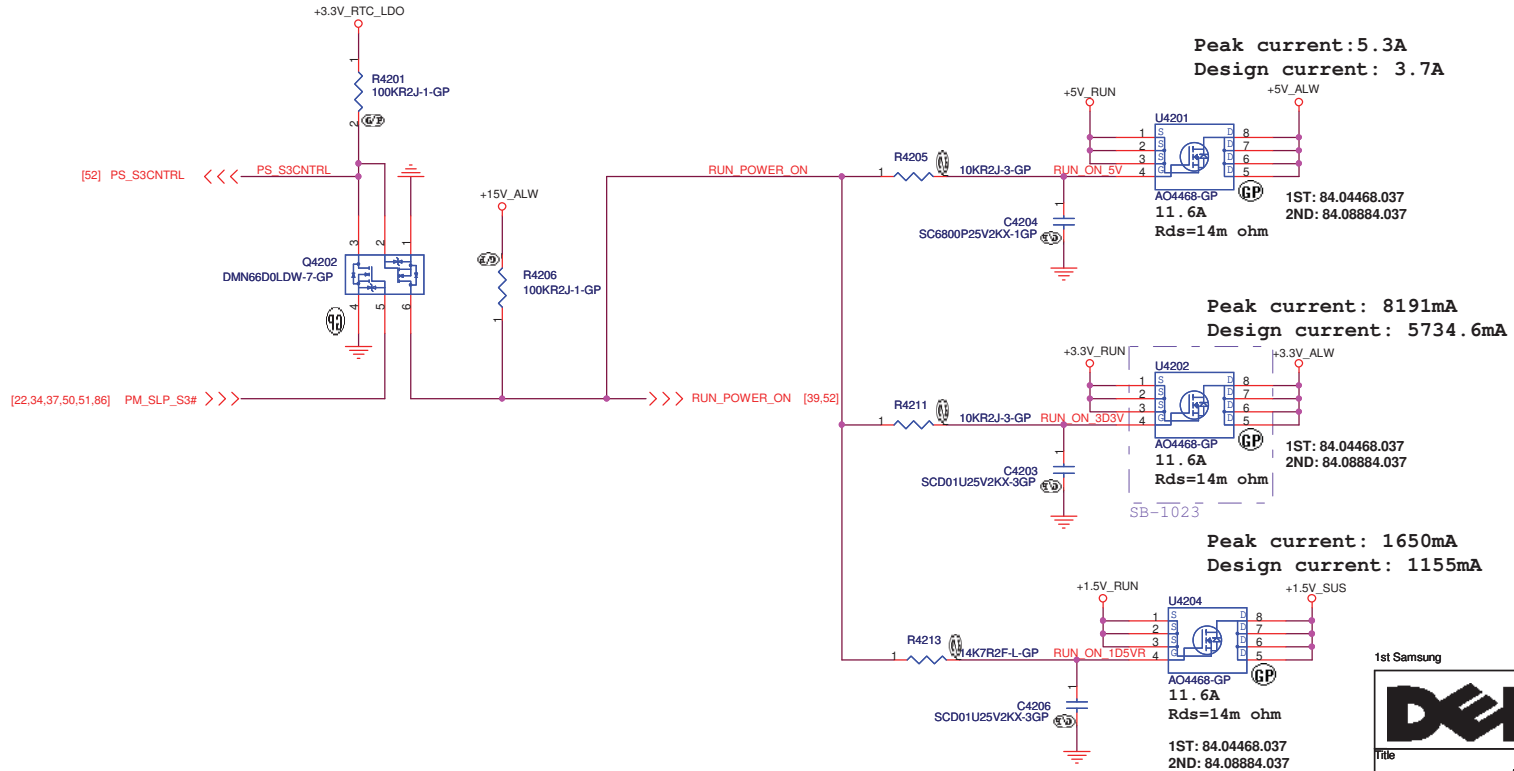
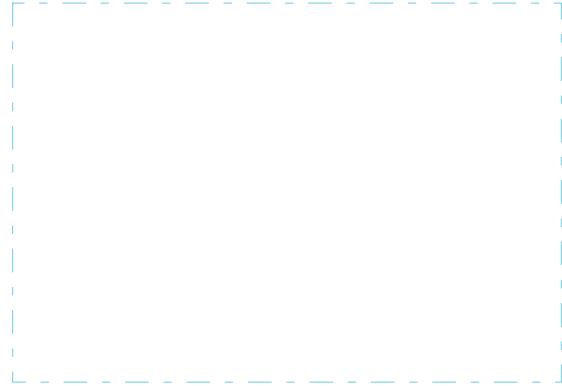
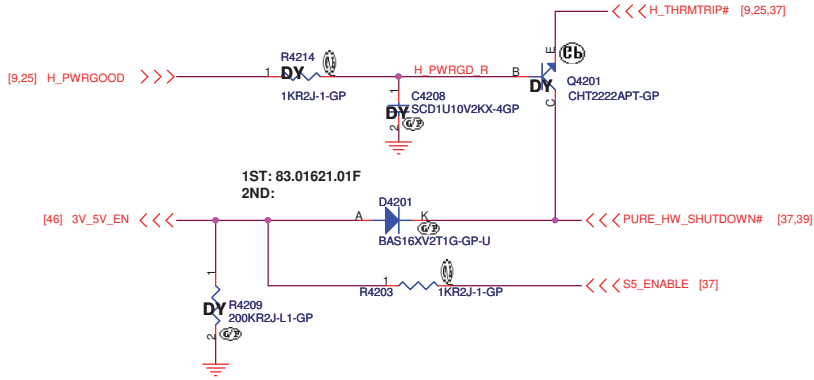
<http://laptop-motherboard-schematic.blogspot.com/>

1st Samsung

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Title			
(Reserve)			
Size	Document Number	Rev	
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SSID = Reset . Suspend

Remove +3.3V_DELAY power rail 2009/05/25



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1st Samsung

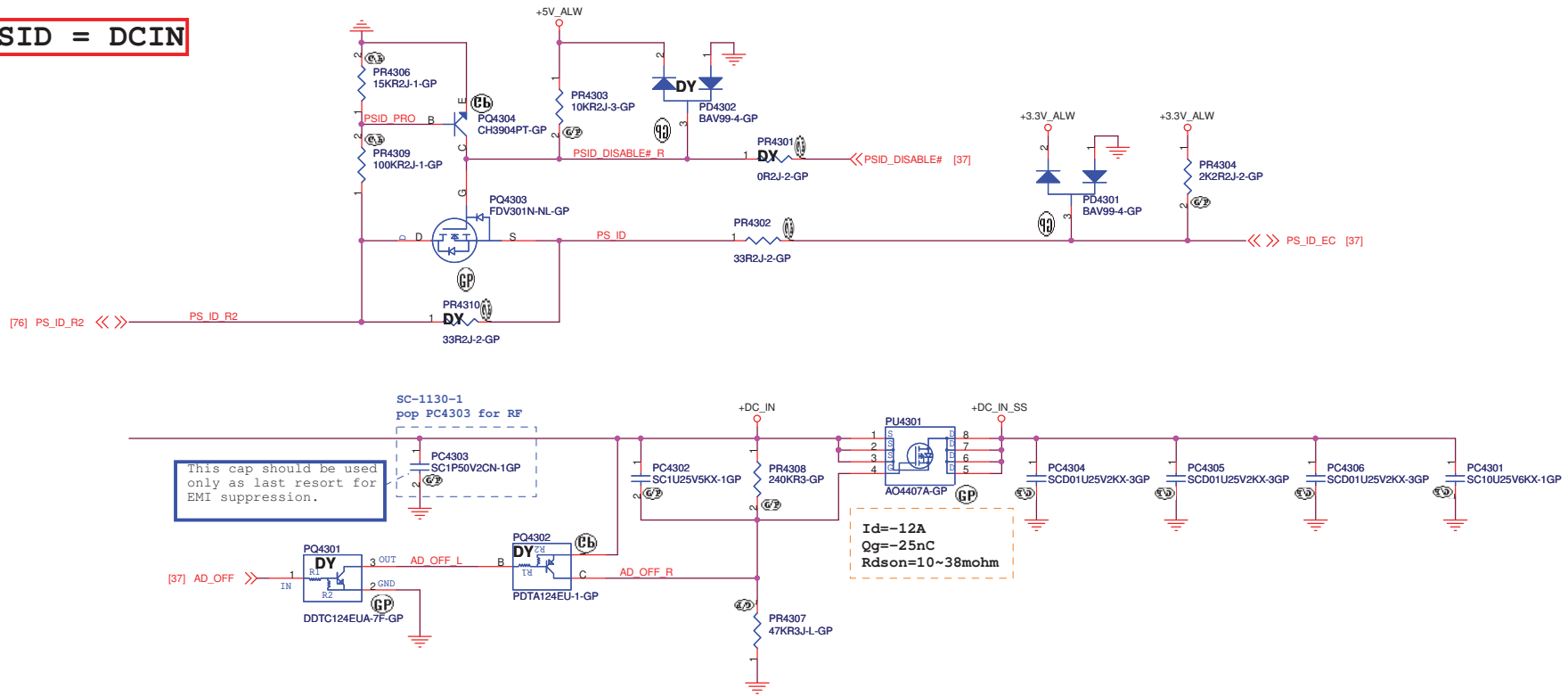
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Plane Enable**

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00


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SSID = DCIN



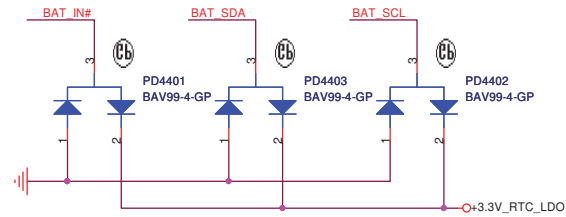
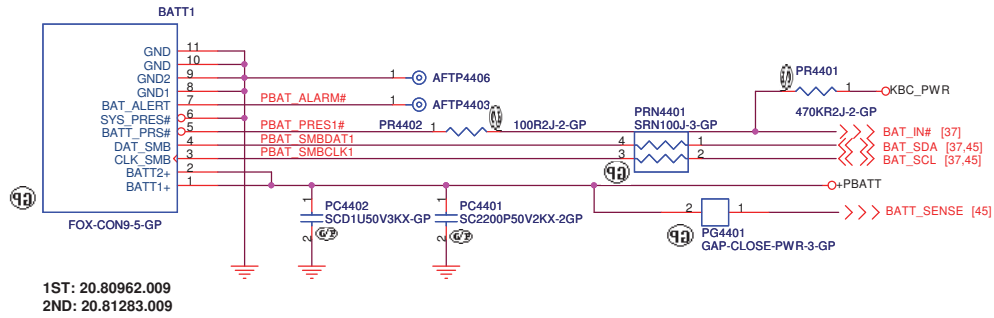
<http://laptop-motherboard-schematic.blogspot.com/>

1st Samsung

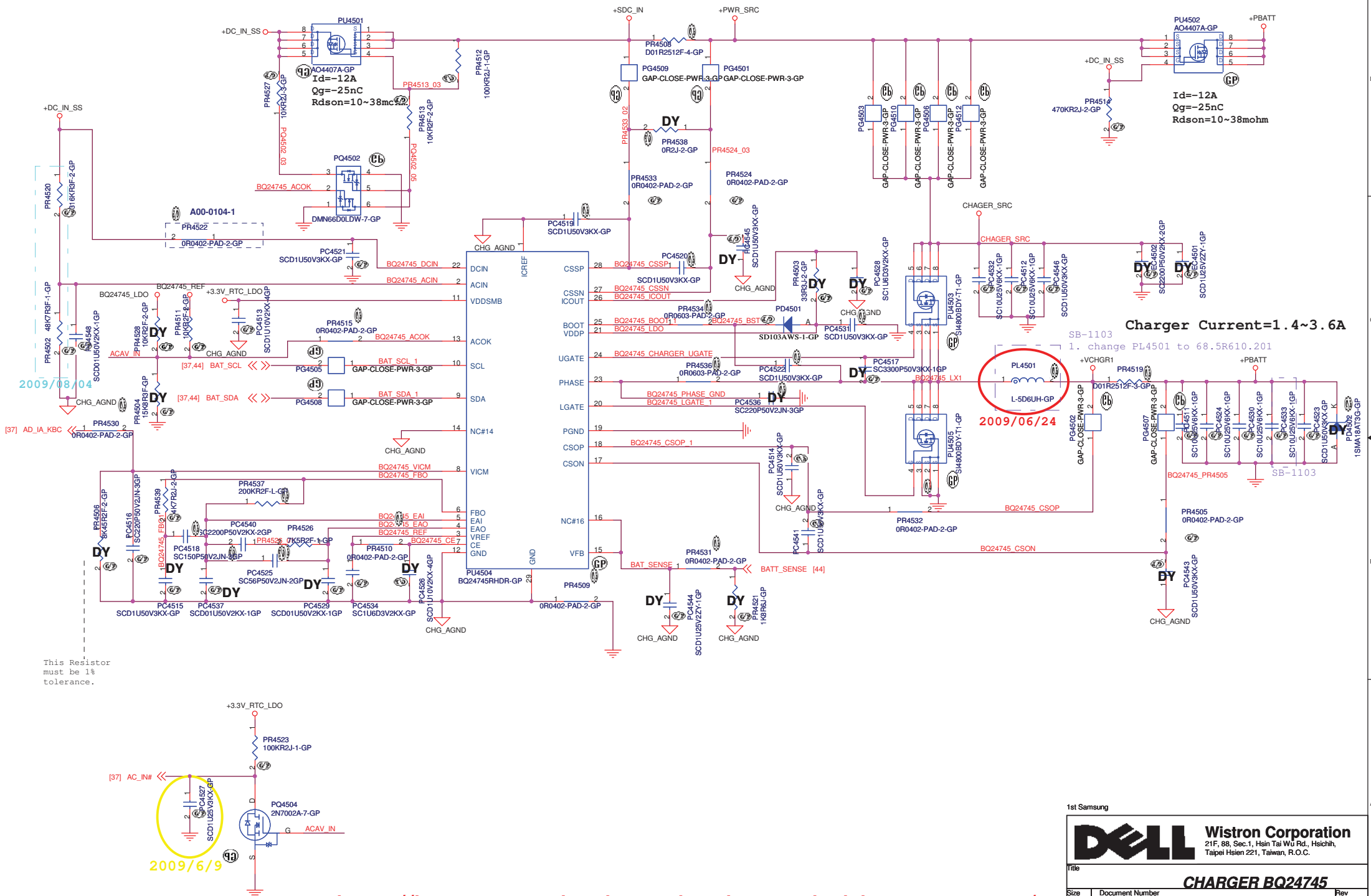
 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
DCIN		
Size	Document Number	Rev
Custom	Winery13 MB DIS	A00
Date:	Wednesday, January 13, 2010	Sheet 43 of 88

SSID = BATT

Batt Connector



SSID = Charger



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1st Samsung

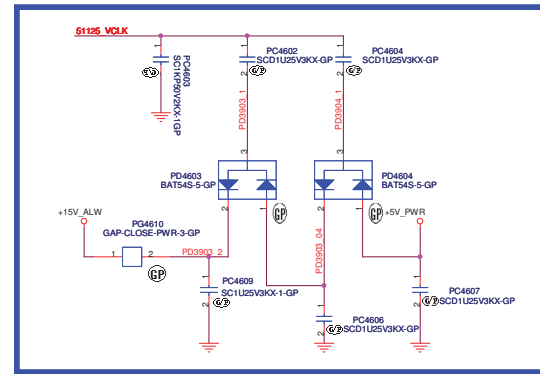
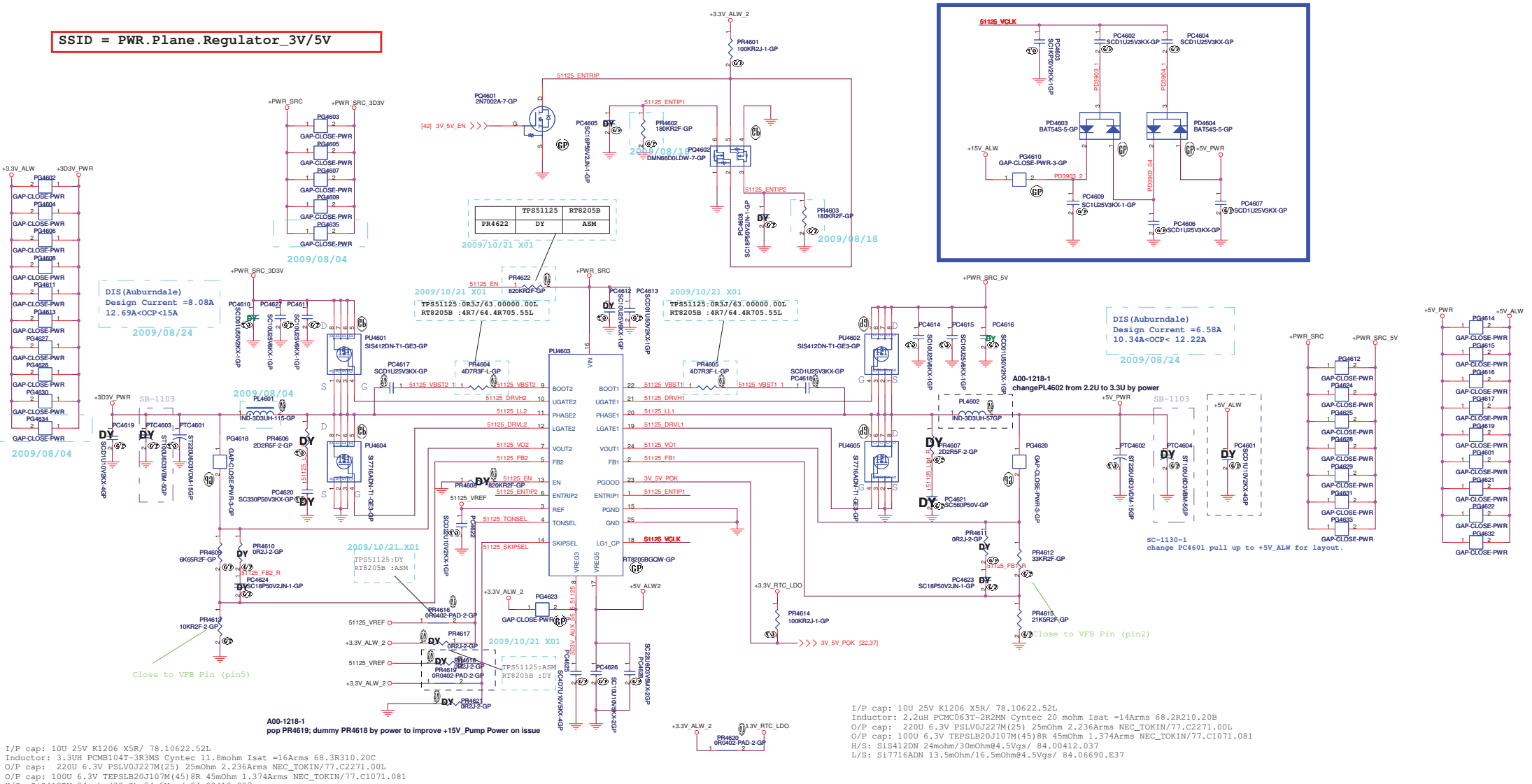
DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **CHARGER BQ24745**

Size	Document Number	Rev
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SSID = PWR.Plane.Regulator_3V/5V



DIS (Auburdale)
Design Current = 8.08A
12.69A <OCP < 15A
2009/08/24

DIS (Auburdale)
Design Current = 6.58A
10.34A <OCP < 12.22A
2009/08/24

I/P cap: 10u 25V K1206 X5R/ 78.10622.52L
Inductor: 3.3uH PCB104T-3R3MS Cyntec 11.8mohm Isat =16Arms 68.3R310.20C
O/P cap: 220u 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.c2271.00L
O/P cap: 100u 6.3V TEPSLB20J107M(45) 8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: S1S412DN 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: S17716ADN 13.5mOhm/16.5mOhm@4.5Vgs/ 84.06690.E37

I/P cap: 10u 25V K1206 X5R/ 78.10622.52L
Inductor: 2.2uH PCH063T-2R2MN Cyntec 20 mohm Isat =14Arms 68.2R210.20B
O/P cap: 220u 6.3V PSLV0J227M(25) 25mOhm 2.236Arms NEC_TOKIN/77.c2271.00L
O/P cap: 100u 6.3V TEPSLB20J107M(45) 8R 45mOhm 1.374Arms NEC_TOKIN/77.C1071.081
H/S: S1S412DN 24mohm/30mOhm@4.5Vgs/ 84.00412.037
L/S: S17716ADN 13.5mOhm/16.5mOhm@4.5Vgs/ 84.06690.E37

TONSEL	CH1	CH2	SKIPSEL	VREG3 or VREG5	VREF (2V)	GND
GND	200kHz	265kHz	Operating Mode	OOA Auto Skip	Auto Skip	PWM only
VREF	245kHz	305kHz				
VREG3	300kHz	375kHz				
VREG5	365kHz	460kHz				
ENO	Open	820kΩ to GND	GND			
Operating Mode	enable both LDOs, VCLK on and ready to turn on switcher channels	enable both LDOs, VCLK off and ready to turn on switcher channels	disable all circuit			

1st Samsung

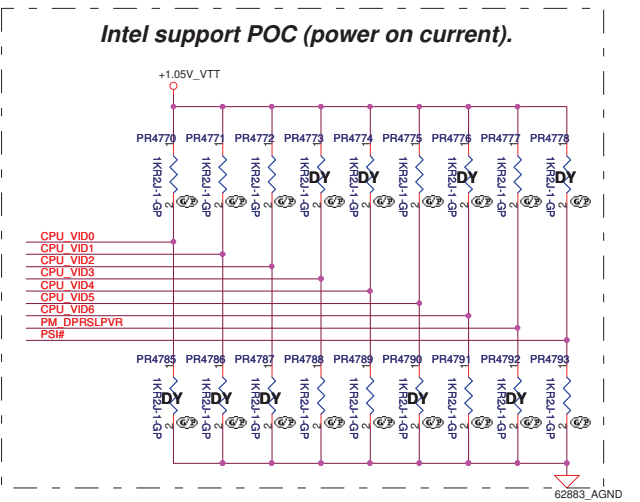
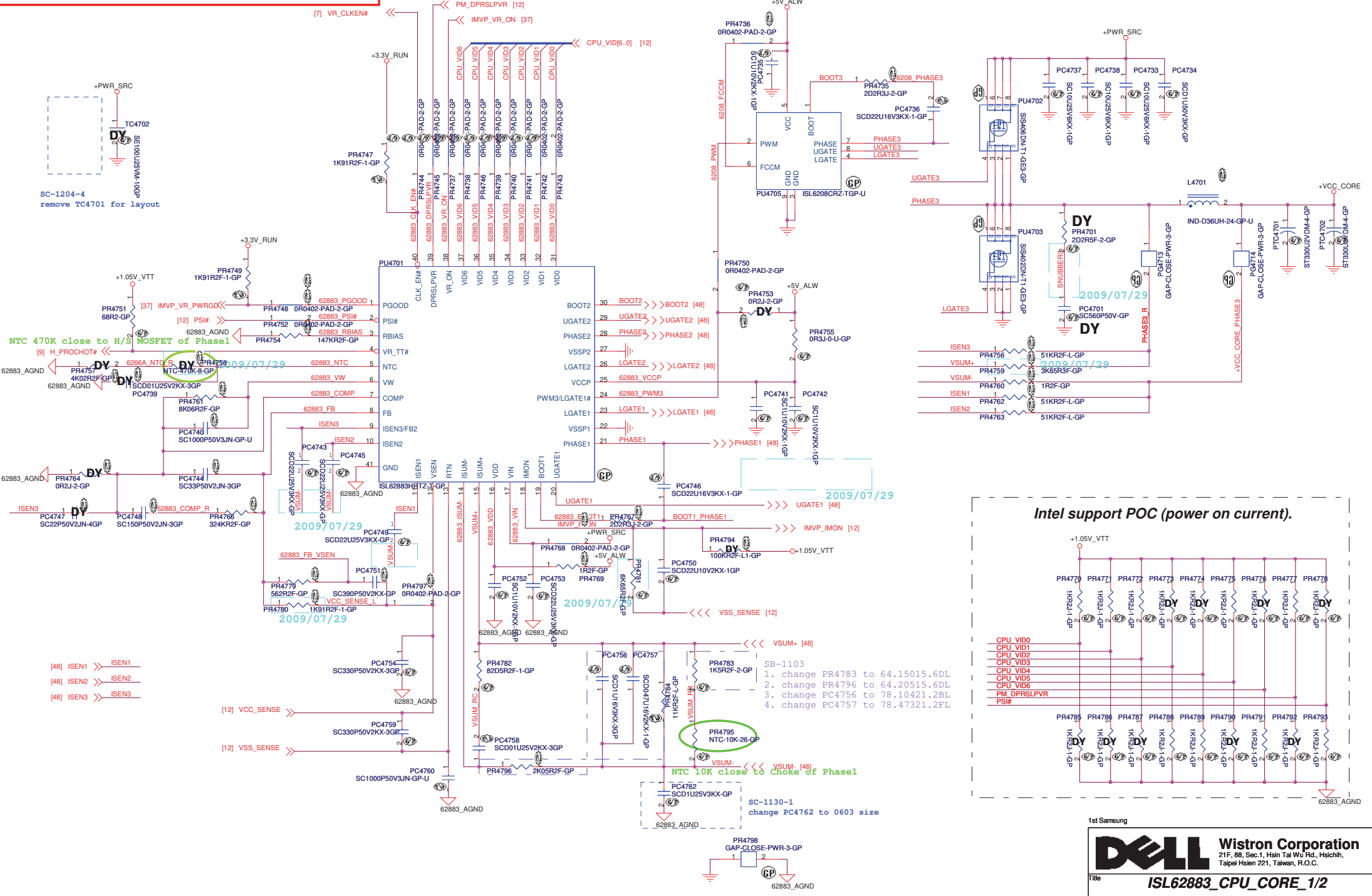
DELL Wistron Corporation
21F. 8R. Sec. 1. Hsin Tai Wu Rd. Hsinchu, Taipei Hsein 221, Taiwan, R.O.C.

File: **RT8205B_5V/3D3V**

Size: Custom Document Number: Winery13 MB DIS Rev: A00

Date: Wednesday, January 13, 2010 Sheet: 46 of 88

SSID = PWR.Plane.Regulator_CPU Core



1st Samsung

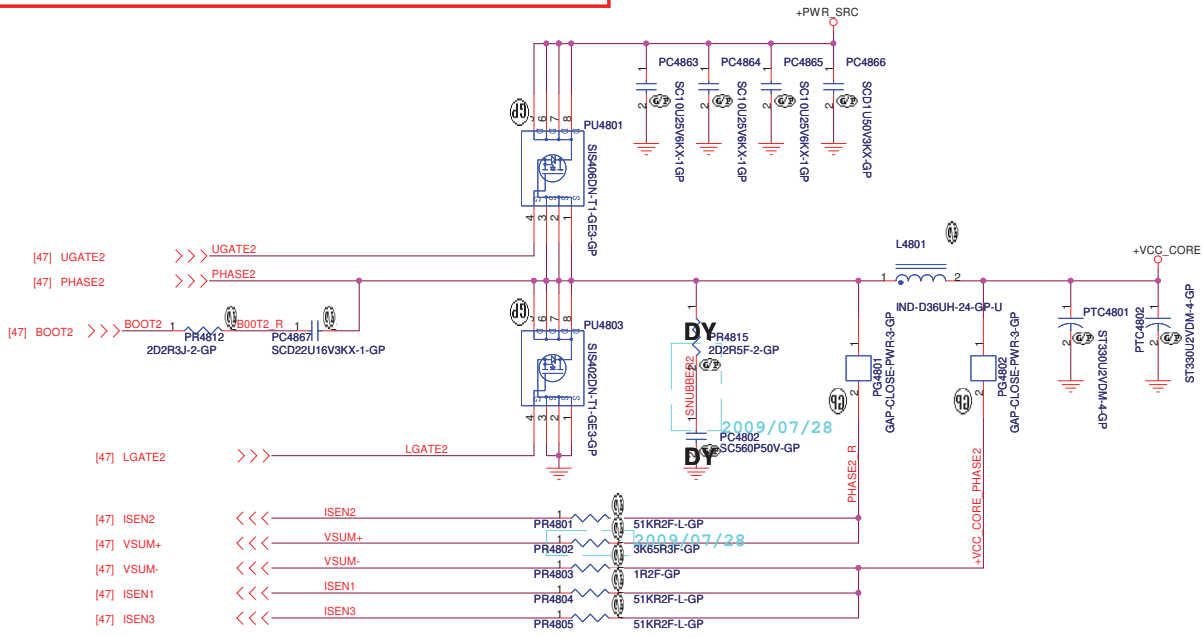
DELL **Wistron Corporation**
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ISL62883_CPU_CORE_1/2**

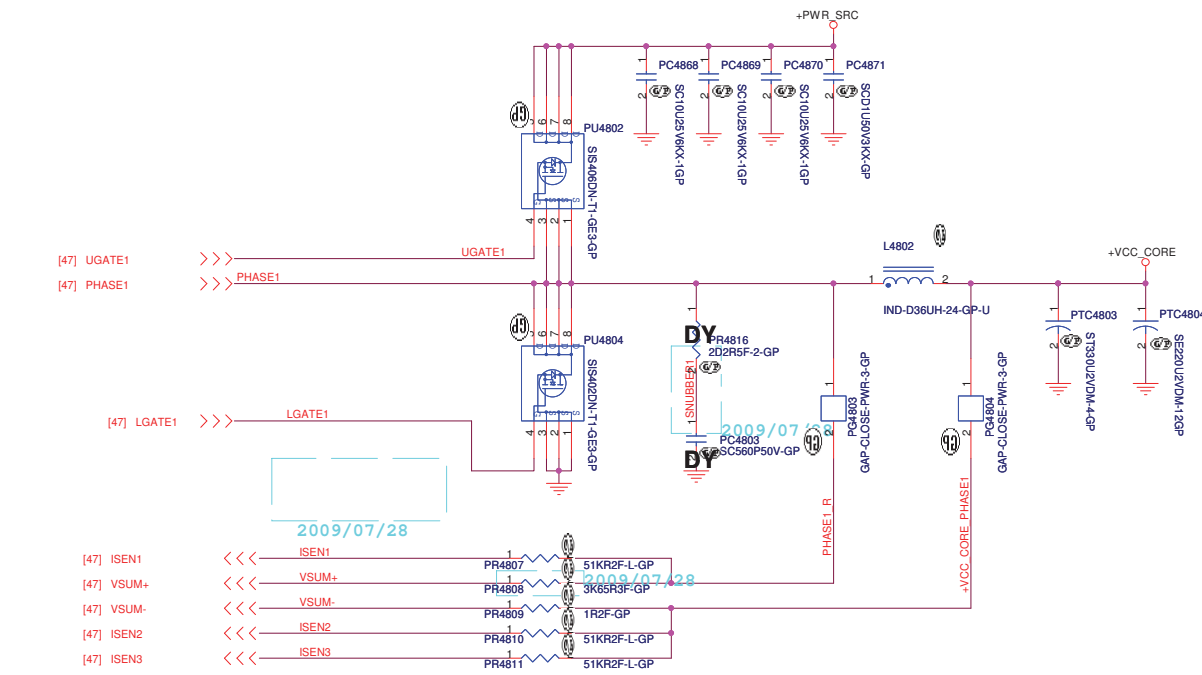
Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 47 of 88

SSID = PWR.Plane.Regulator_CPU Core



DIS (Auburndale)
 Design Current = 34A
 Peak Current=48A
 57.6A<OCP< 67.2A



I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 0.36UH ETQP4LR36WFC PANASONIC 1.1mohm/ 68.R3610.20A
 O/P cap: 330U 2V EEF5X0D221E7 6mOhm 3.0Arms Panasonic/79.33719.20L
 O/P cap: 220U 2V EEF5X0D331XE 7mOhm 3.4Arms Panasonic/79.22719.90L
 H/S: SiR474DP/ POWERPAK-8/ 10mOhm/12mOhm @4.5Vgs/ 84.00474.037
 L/S: S17170DP/ POWERPAK-8/ 3.6mOhm/4.3mohm@4.5Vgs/ 84.07170.037
 Freq=300KHz<PER PHASE

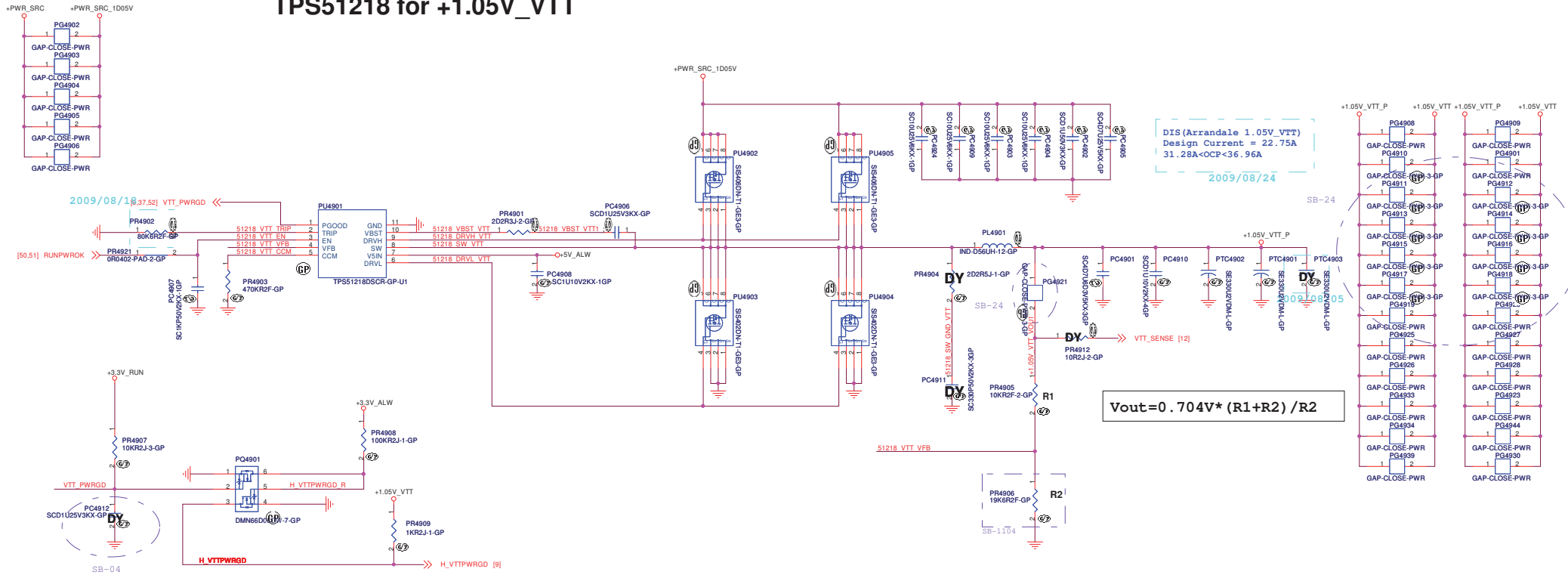
1st Samsung

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title **ISL62883_CPU_CORE_2/2**

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00
Date	January 13, 2010	Sheet 48 of 88

TPS51218 for +1.05V_VTT



DIS (Arrandale 1.05V_VTT)
Design Current = 22.75A
31.28A < OCP < 36.96A
2009/08/24

$$V_{out} = 0.704V * (R1 + R2) / R2$$

Frequency setting	
470K	-->290KHz
200K	-->340KHz
100K	-->380KHz
39K	-->430KHz

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
O/P cap: 330U 2.5V EEPX0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L01
H/S: S1S406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm 84.5Vgs/ 84.00406.037
L/S: S1S402DN/ POWERPAK-8/ 6.4mOhm/8mohm@4.5Vgs/ 84.00402.037

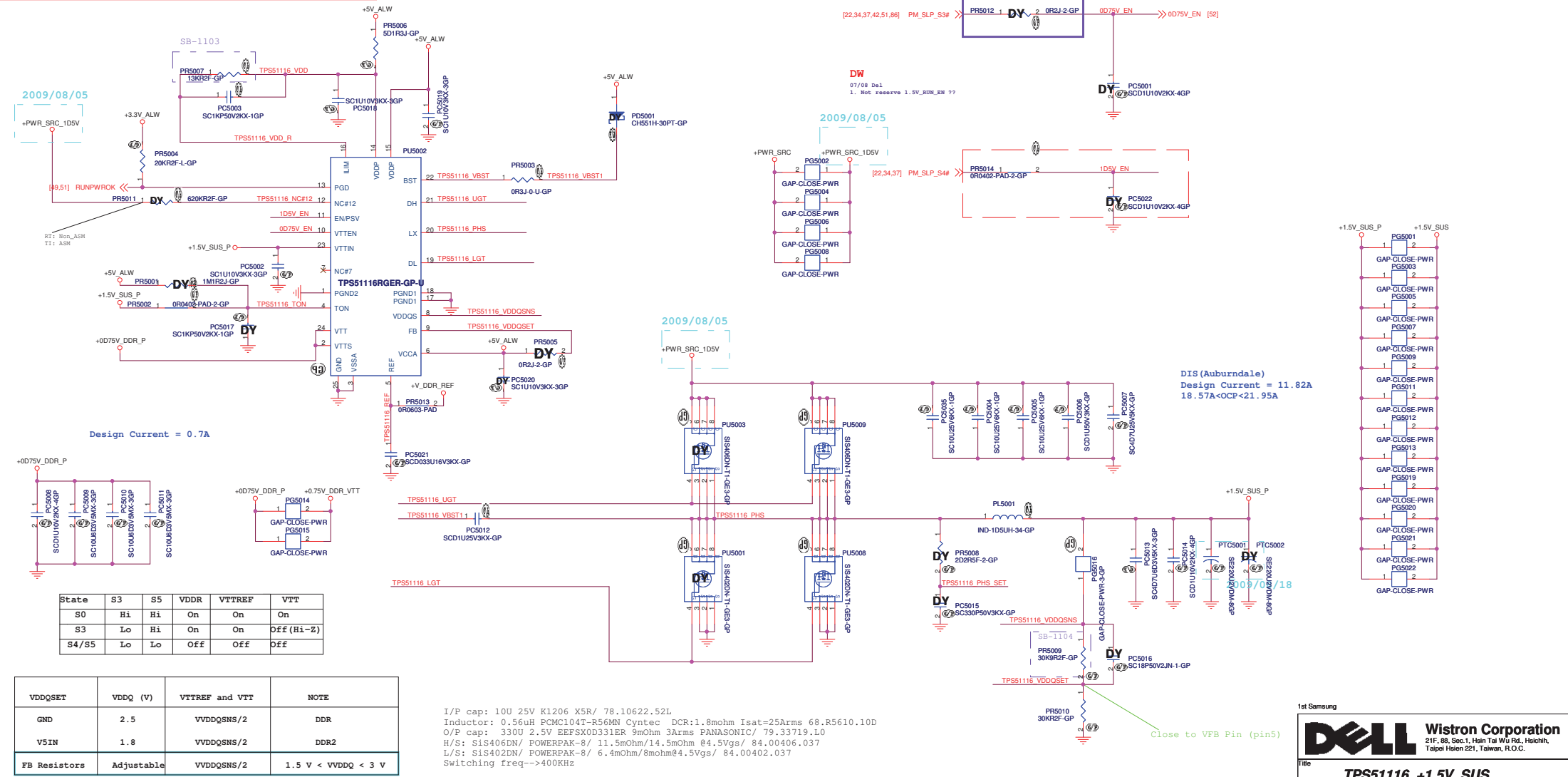
1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Heichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **TPS51218 +1.05V_VTT**

Size	Document Number	Rev
Custm	Winery13 MB DIS	A00
Date: Wednesday, January 13, 2010	Sheet 49 of 88	

SSID = PWR.Plane.Regulator_1D5V/0D75V



State	S3	S5	VDDR	VITREF	VIT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

VDDQSET	VDDQ (V)	VITREF and VIT	NOTE
GND	2.5	VVDDQSN/2	DDR
V5IN	1.8	VVDDQSN/2	DDR2
FB Resistors	Adjustable	VVDDQSN/2	1.5 V < VVDDQ < 3 V

I/P cap: 100 25V K1206 X5R/ 78.10622.52L
 Inductor: 0.56uH PCMC104T-R56MN Cyntec DCR:1.8mohm Isat=25Arms 68.R5610.10D
 O/P cap: 330U 2.5V EEF5X0D331ER 9mOhm 3Arms PANASONIC/ 79.33719.L0
 H/S: S1S406DN/ POWERPAK-8/ 11.5mOhm/14.5mOhm @4.5Vgs/ 84.00406.037
 L/S: S1S402DN/ POWERPAK-8/ 6.4mOhm/6mohm@4.5Vgs/ 84.00402.037
 Switching freq-->400KHz

Close to VFB Pin (pin5)

1st Samsung

Wistron Corporation
 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

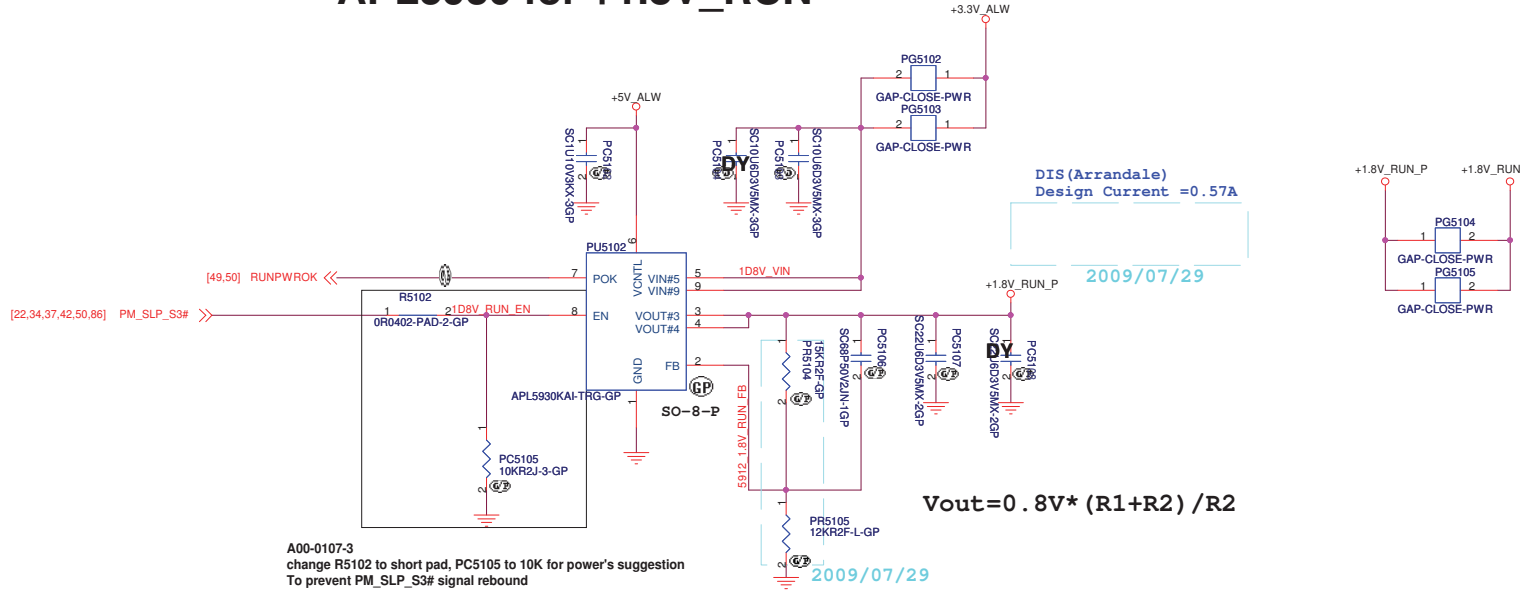
Title: **TPS51116 +1.5V SUS**

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00

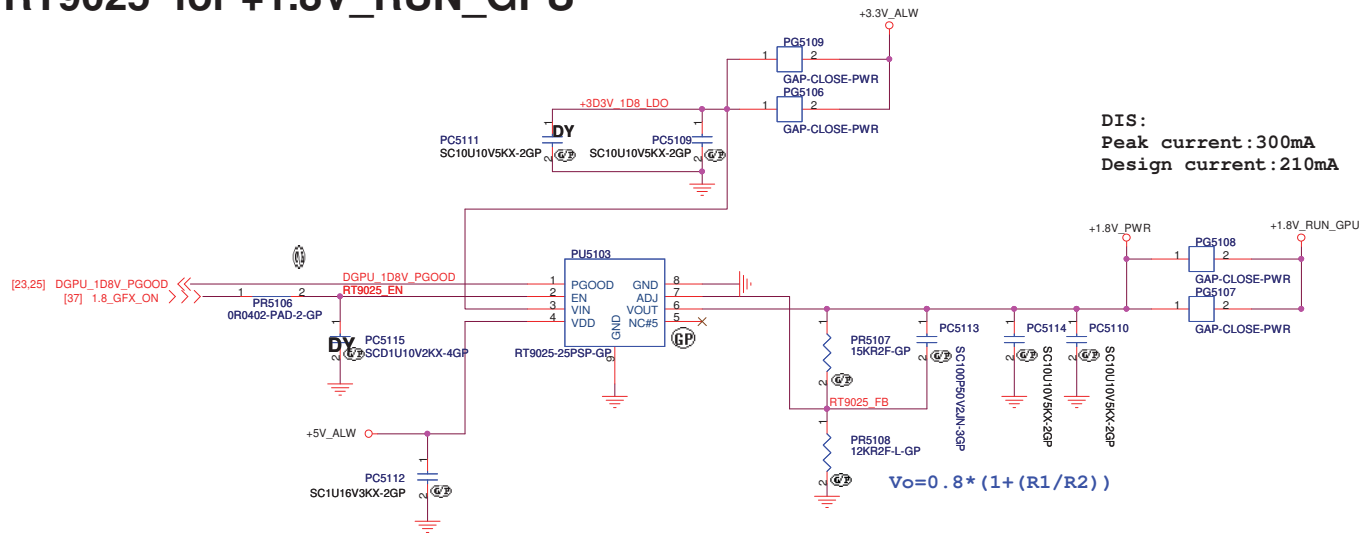
Date: Wednesday, January 13, 2010 ESheet 50 of 88

SSID = PWR.Plane.Regulator_1D8V

APL5930 for +1.8V_RUN



RT9025 for +1.8V_RUN_GPU



1st Samsung

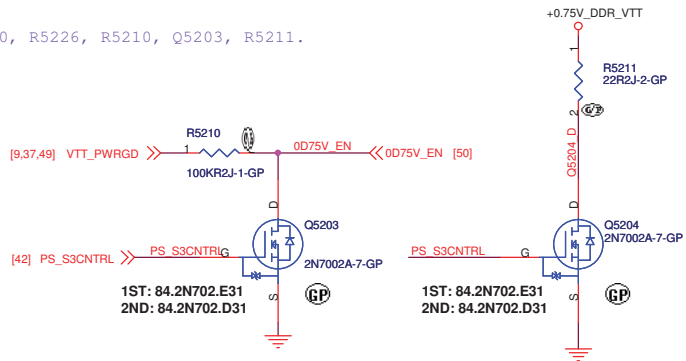
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
APL5930/RT9205

Size	Document Number	Rev
Custom	Winery13 MB DIS	A00
Date	Issue Date, January 13, 2010	Sheet 51 of 88

SSID = PWR.Plane.Switch_1D5V CPU

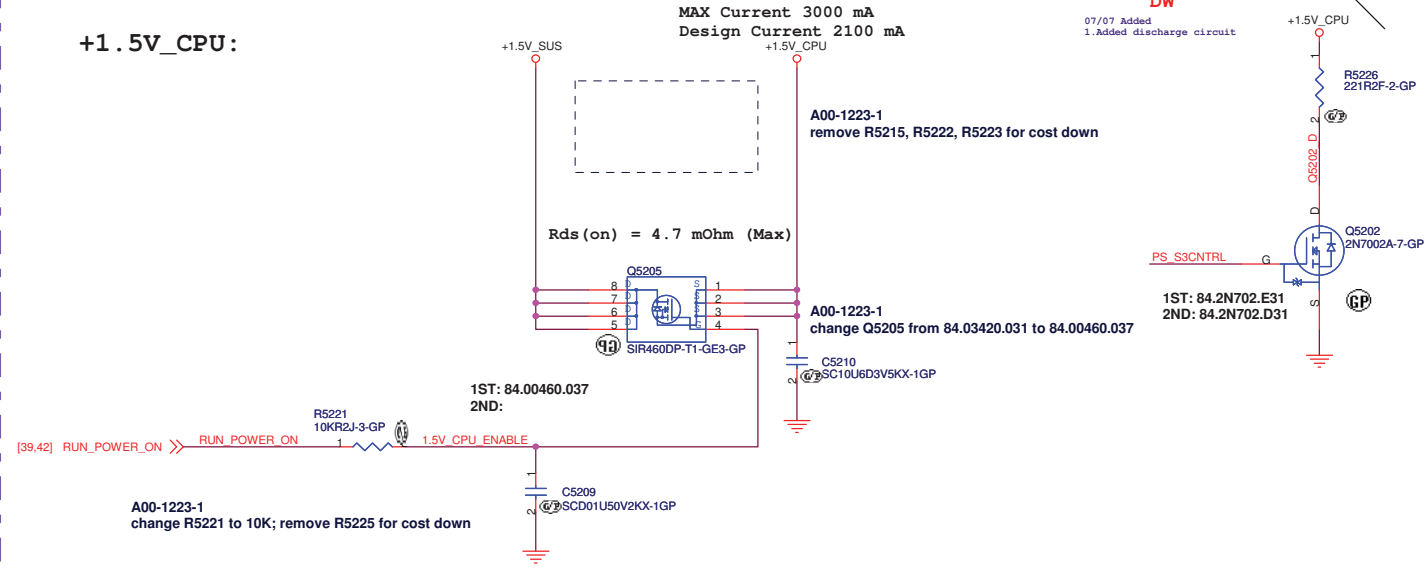
SB-1020-1
DY R5215, R5222, R5223; POP R5221, C5210, R5226, R5210, Q5203, R5211.



**Calpella Platform S3 Power Reduction Platform
S3 Power Reduction CRB Implementation
Design Details
Revision 0.1**

DW
07/07 Added
1. Added discharge circuit

+1.5V_CPU:



DW
07/20 corrected
1. Removed C5288
2. Removed Q5207, R5225, R5220 to save more part counts

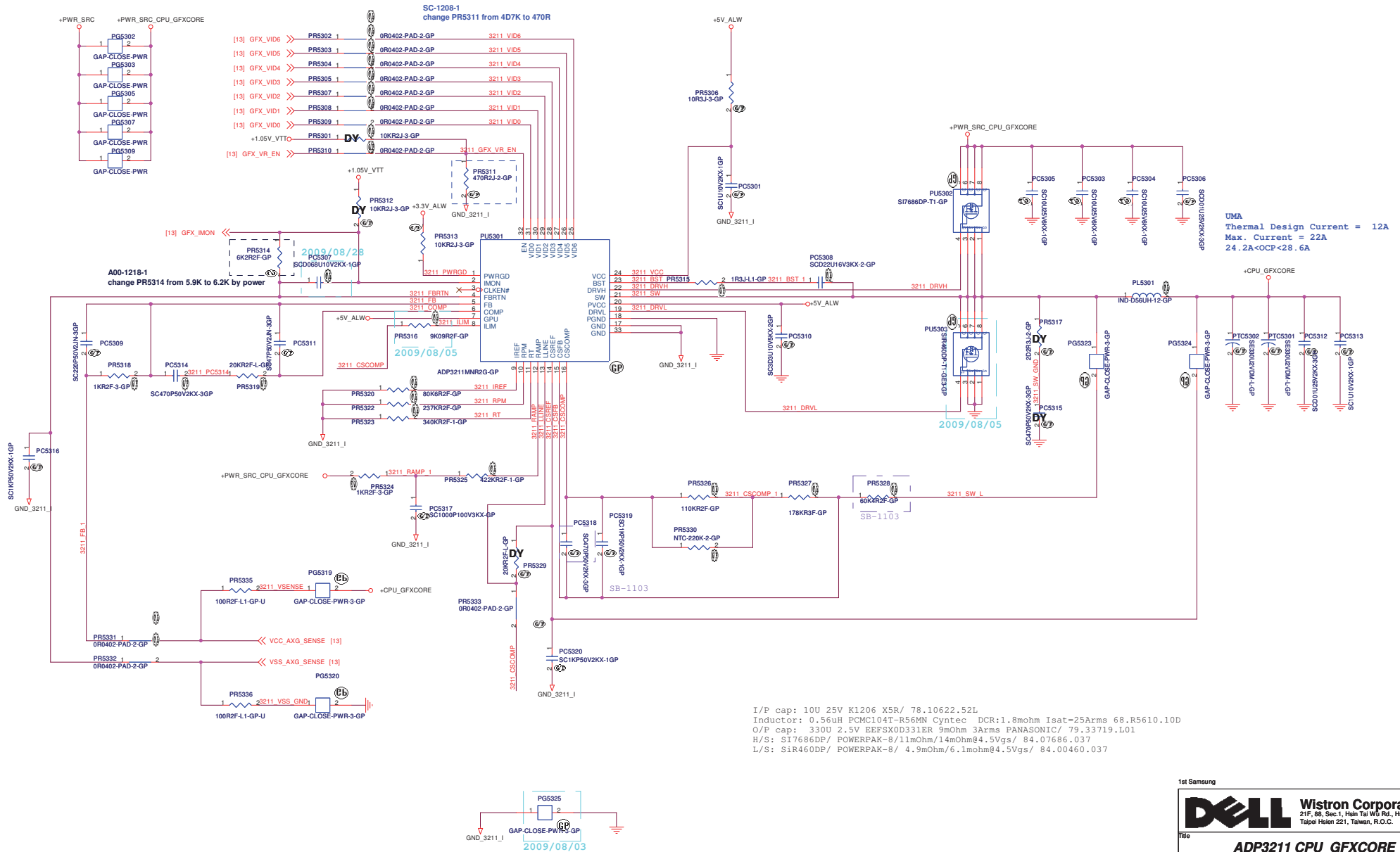
1st Samsung

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **DC to DC 1D5V**

Size Custom	Document Number Winery13 MB DIS	Rev A00
Date: Wednesday, January 13, 2010	Sheet 52	of 88

SSID = CPU.GFX.Regulator



1st Samsung

DELL Wistron Corporation
 21F, 89, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **ADP3211 CPU GFXCORE**

Size: Document Number
 Custom: **Winery13 MB DIS** Rev: **A00**

Date: Wednesday, January 13, 2010 Sheet: 33 of 88

SSID = VIDEO

Close PCH

Close GPU

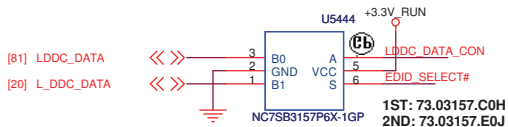
DW

07/07 Added
1. Added LVDS DDC CLK/DAT Pull Hi

[20] L_DDC_DATA
[20] L_DDC_CLK

[81] LDDC_DATA
[81] LDDC_CLK

UMA/DIS LVDS DDC CLK/DAT select circuit



H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)

[21.55] EDID_SELECT# >>> EDID_SELECT#

[81] LDDC_CLK <<<

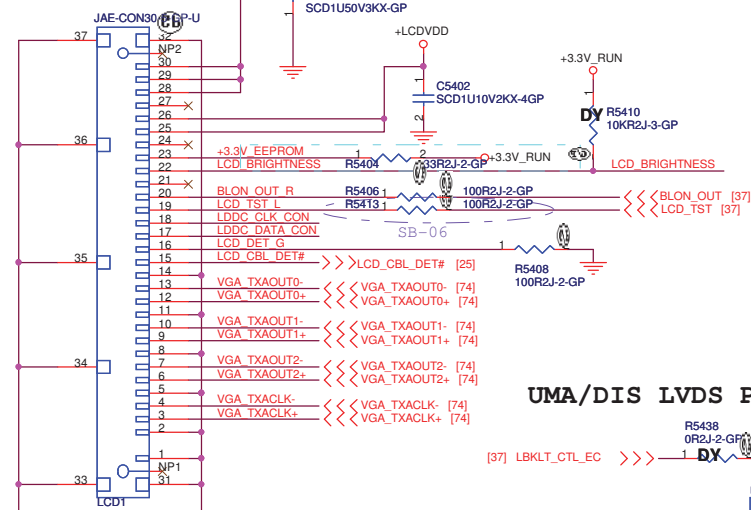
[20] L_DDC_CLK <<<

LDDC_DATA CON
LDDC_CLK CON

EV @ LVDS side

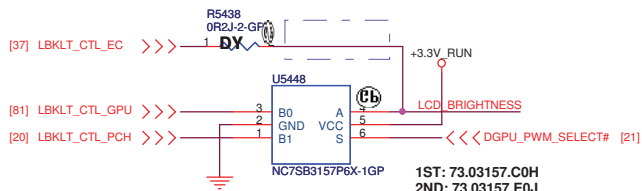
+PWR_SRC_LCD

LVDS CONNECTOR

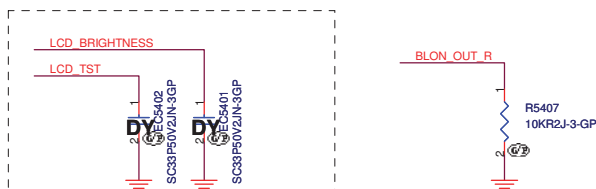


1ST: 20.F1555.030
2ND:

UMA/DIS LVDS PWM select circuit



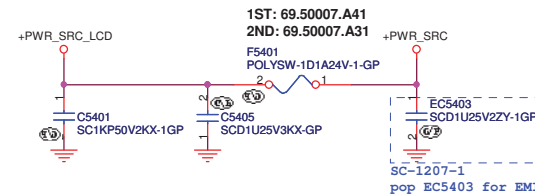
H=>B1 -iGPU PCH (UMA)
L=>B0 -dGPU GPU (DIS)



For EMI request

SSID = Inverter

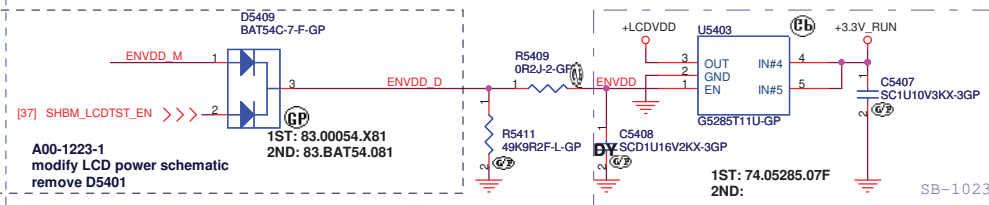
INVERTER POWER



SSID = VIDEO

LCD POWER

SC-1125-2
add mux U5446 to select LCDVDD enable signal

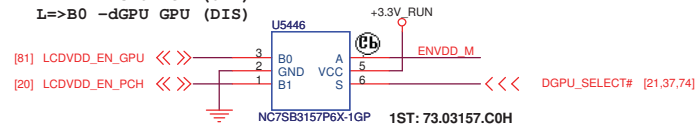


A00-1223-1
modify LCD power schematic
remove D5401

DGPU_SELECT# :

H=>B1 -iGPU PCH (UMA)

L=>B0 -dGPU GPU (DIS)

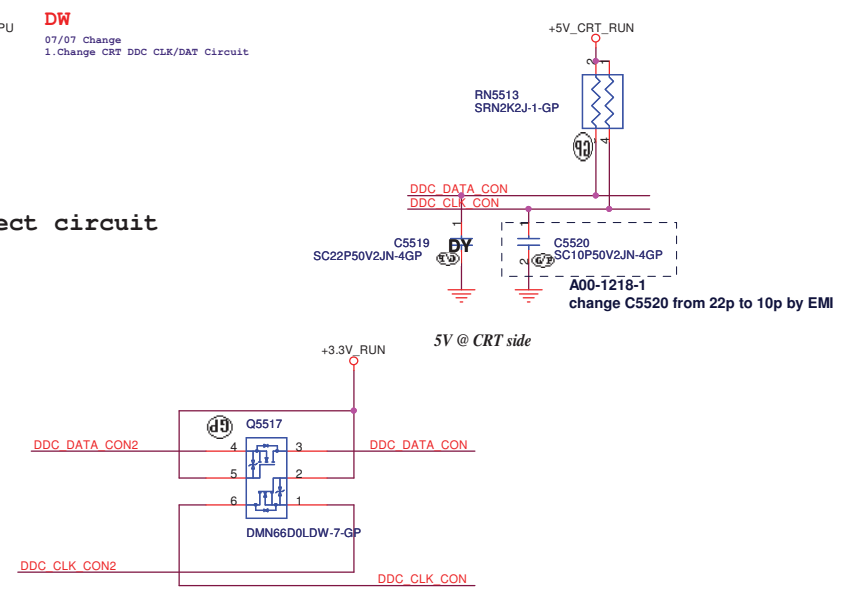
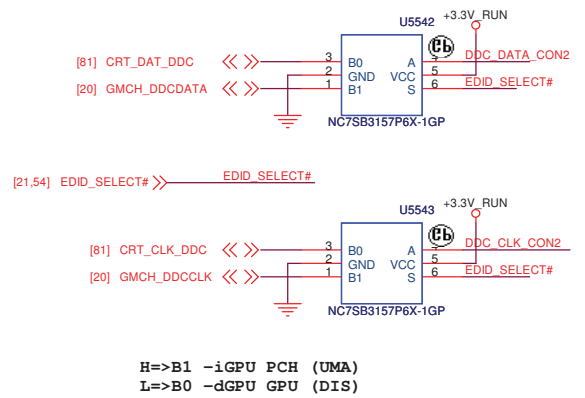
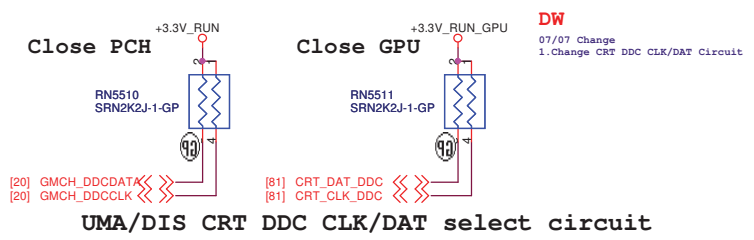
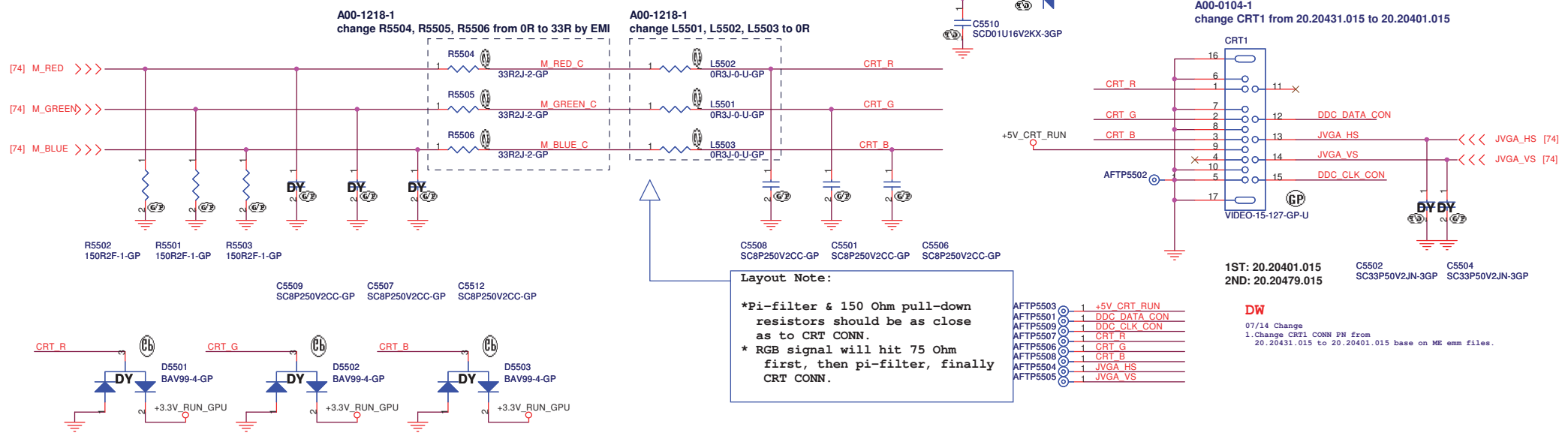


1st Samsung

DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD/Inverter Connector**
Size: Custom Document Number: **Winery13 MB DIS** Rev: **A00**
Date: Wednesday, January 13, 2010 Sheet 54 of 88

SSID = VIDEO



<Core Design>

Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **CRT Connector**


Size A3	Document Number	Rev
	Winery13 MB DIS	A00

Date: Wednesday, January 13, 2010 Sheet 55 of 88

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<http://laptop-motherboard-schematic.blogspot.com/>


1st Samsung

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserve)					
Size	Document Number				Rev
Custom	Winery13 MB DIS				A00
Date:	Wednesday, January 13, 2010		Sheet	56	of 88

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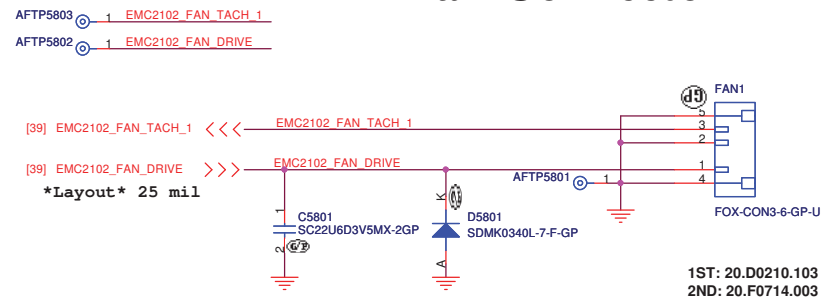
<http://laptop-motherboard-schematic.blogspot.com/>

1st Samsung

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsiehshih, Taipei Hsien 221, Taiwan, R.O.C.
Title			
HDMI Connector			
Size	Document Number	Rev.	
Custom	Winery13 MB DIS	A00	
Date: Wednesday, January 13, 2010			Sheet 57 of 88

SSID = Thermal

Fan Connector

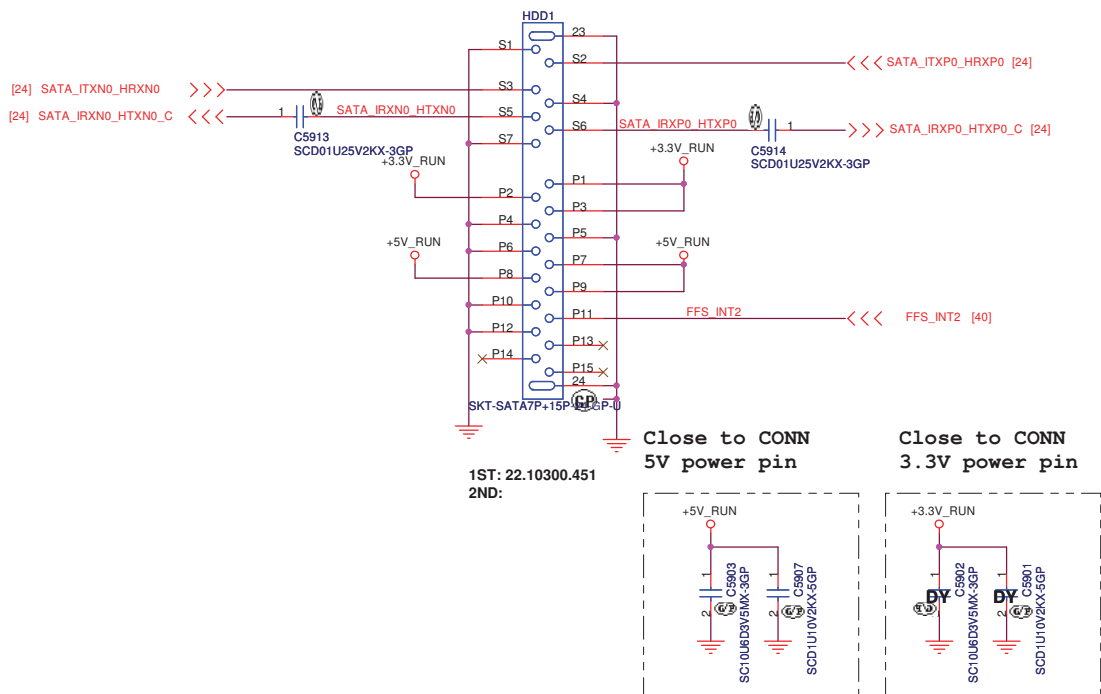


1st Samsung

		Wistron Corporation 21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
FAN		
Size A3	Document Number Winery13 MB DIS	Rev A00
Date: Wednesday, January 13, 2010	Sheet 58	of 88

SSID = SATA

SATA HDD Connector



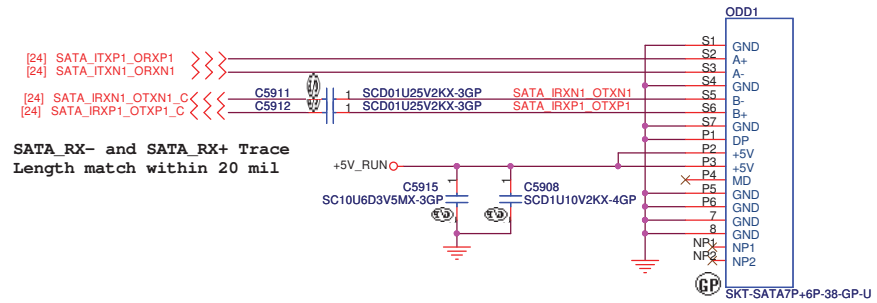
SATA HDD Interface comment

S1:GND
S2:RX+
S3:RX-
S4:GND
S5:TX-
S6:TX+
S7:GND

P1----- 3.3V
P2----- 3.3V
P3----- 3.3V
P4:GND
P5:GND / Dell Detected Pin
P6:GND
P7----- 5V
P8----- 5V
P9----- 5V
P10--- GND
P11:Dell: FFS_INT for supported HDD
P12:GND
P13----- 12V
P14----- 12V
P15----- 12V

SSID = SATA

ODD Connector



SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

1st Samsung

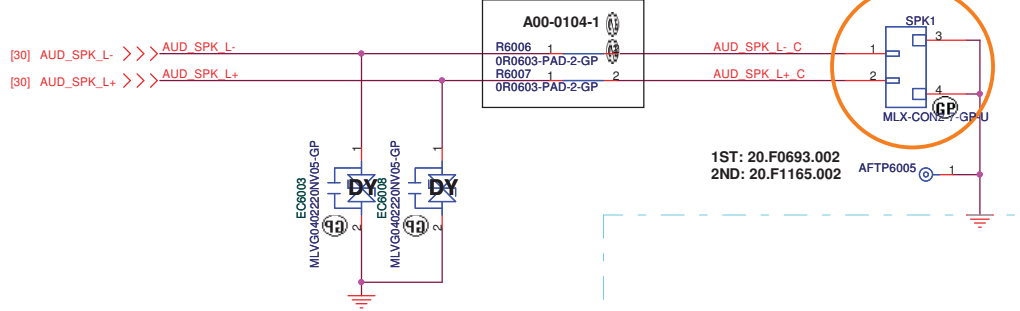
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
HDD/ODD Connector

Size A3	Document Number Winery13 MB DIS	Rev A00
Date: Wednesday, January 13, 2010	Sheet 59	of 88

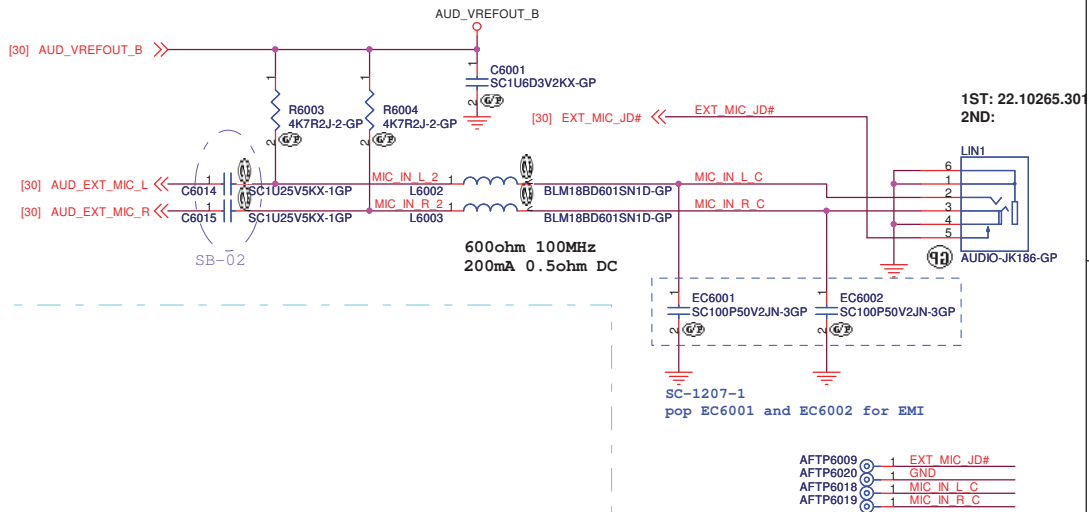
SSID = AUDIO

Speaker Connector



SSID = AUDIO

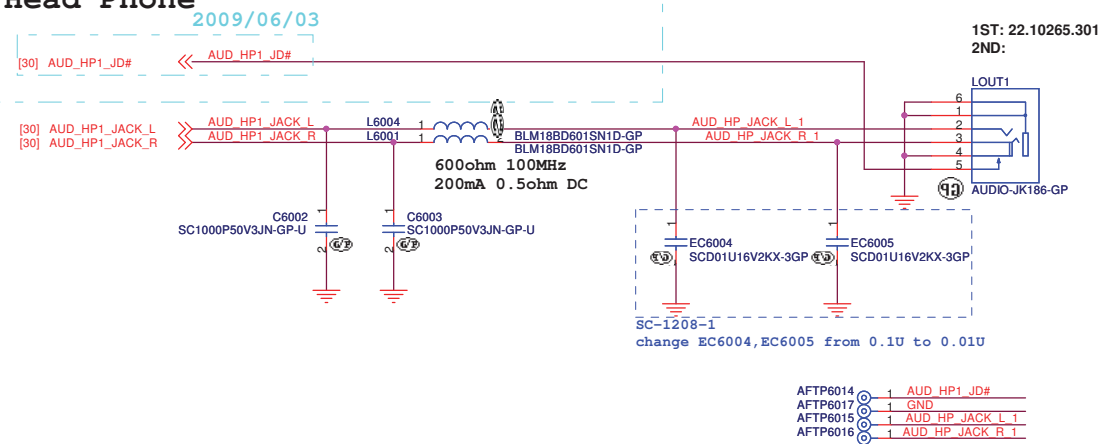
MIC IN



Delete Audio De-pop Circuit
2009/07/24

SSID = AUDIO

Head Phone



Added HP circuit 2009/05/26

1st Samsung




Title SPEAKER/MIC/AUDIO JACK		
Size A3	Document Number Winery13 MB DIS	Rev A00
Date: Wednesday, January 13, 2010	Sheet 60 of	88

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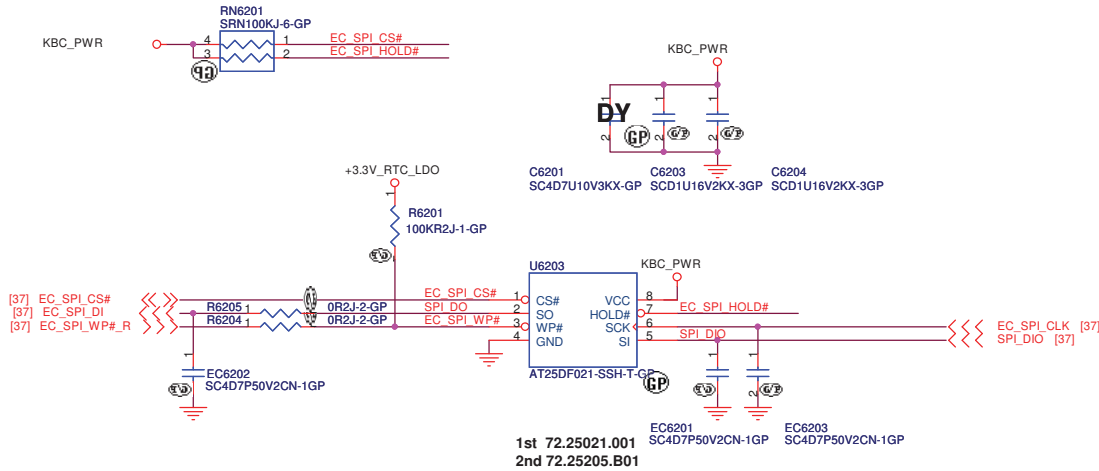
<http://laptop-motherboard-schematic.blogspot.com/>

1st Samsung

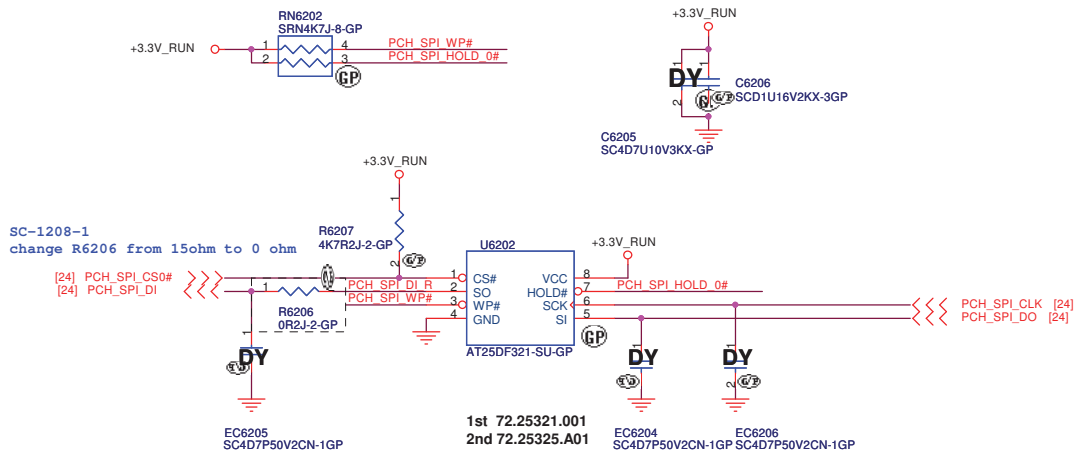
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
(Reserve)			
Size	Document Number	Rev	
Custom	Winery13 MB DIS	A00	
Date: Wednesday, January 13, 2010		Sheet 61	of 88

SSID = Flash.ROM

SPI FLASH ROM (2M bits) for KBC

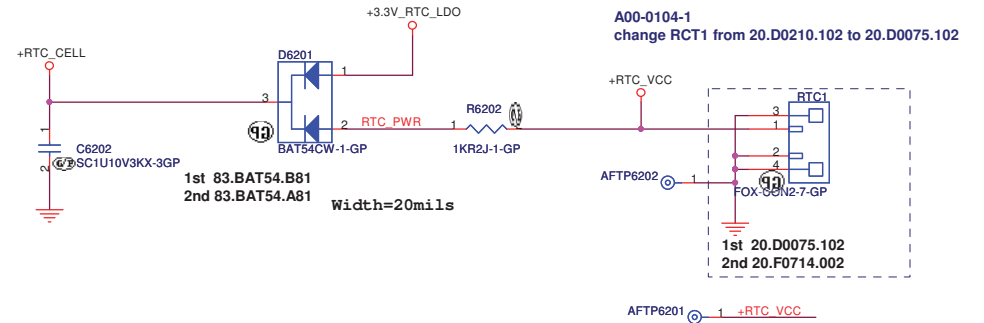


SPI FLASH ROM (32M bits) for PCH



SSID = RBATT

RTC Connector



1st Samsung

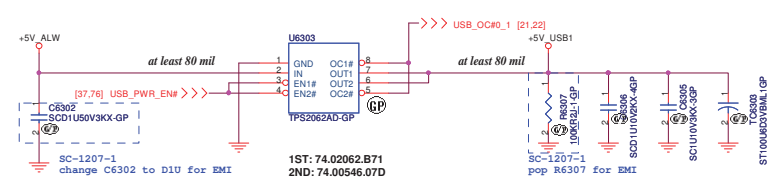
Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **EEPROM/RTC Connector**

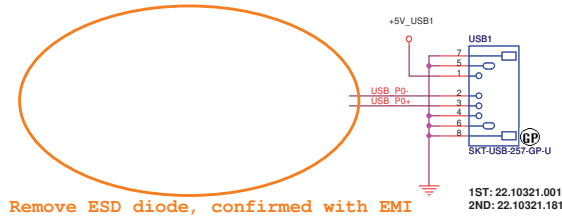
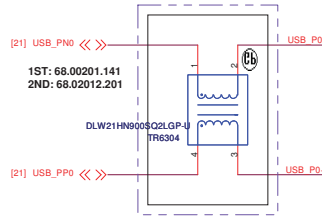
Size: A3	Document Number: Winery13 MB DIS	Rev: A00
Date: Wednesday, January 13, 2010	Sheet: 62	of: 88

SSID = USB

USB & ESATA Power SW



SB-1021
1. pop and change TR6304 to 90 ohm for EMI;
DY R6302, R6308

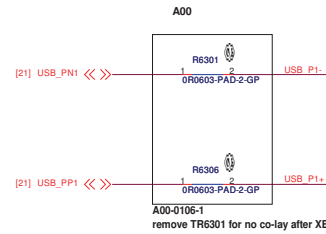


A00-0106-1
remove R6302, R6308 for no co-layer after XB

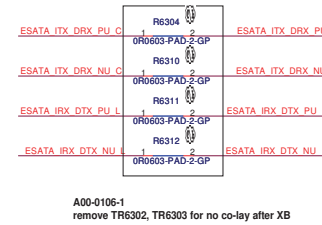
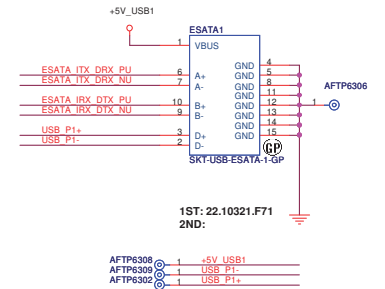
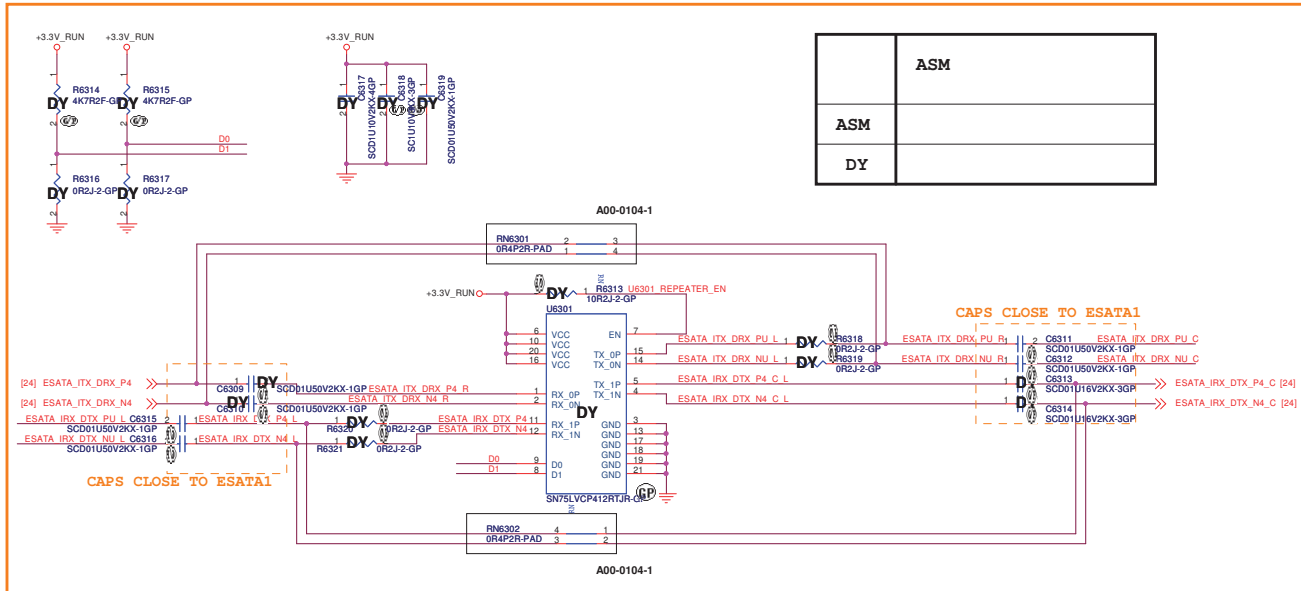
SSID = ESATA

ESATA Power

Share one power SW with USB port 1



	ASM
ASM	
DY	



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Tapei Hsien 221, Taiwan, R.O.C.

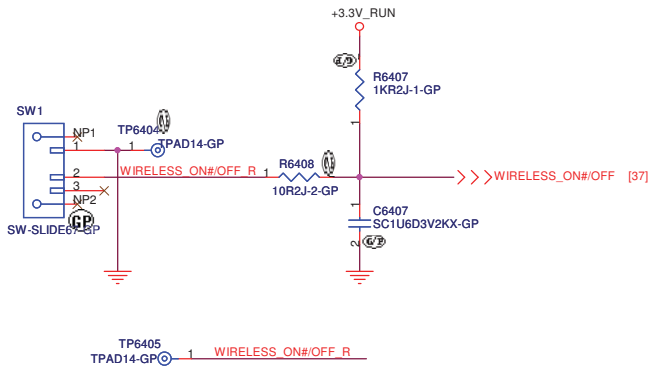
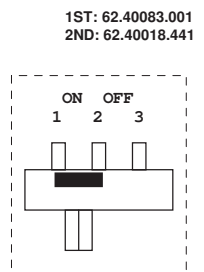
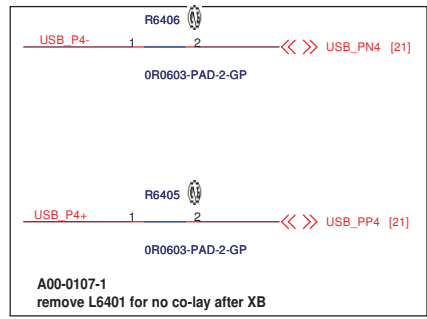
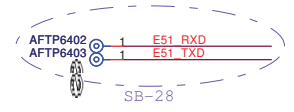
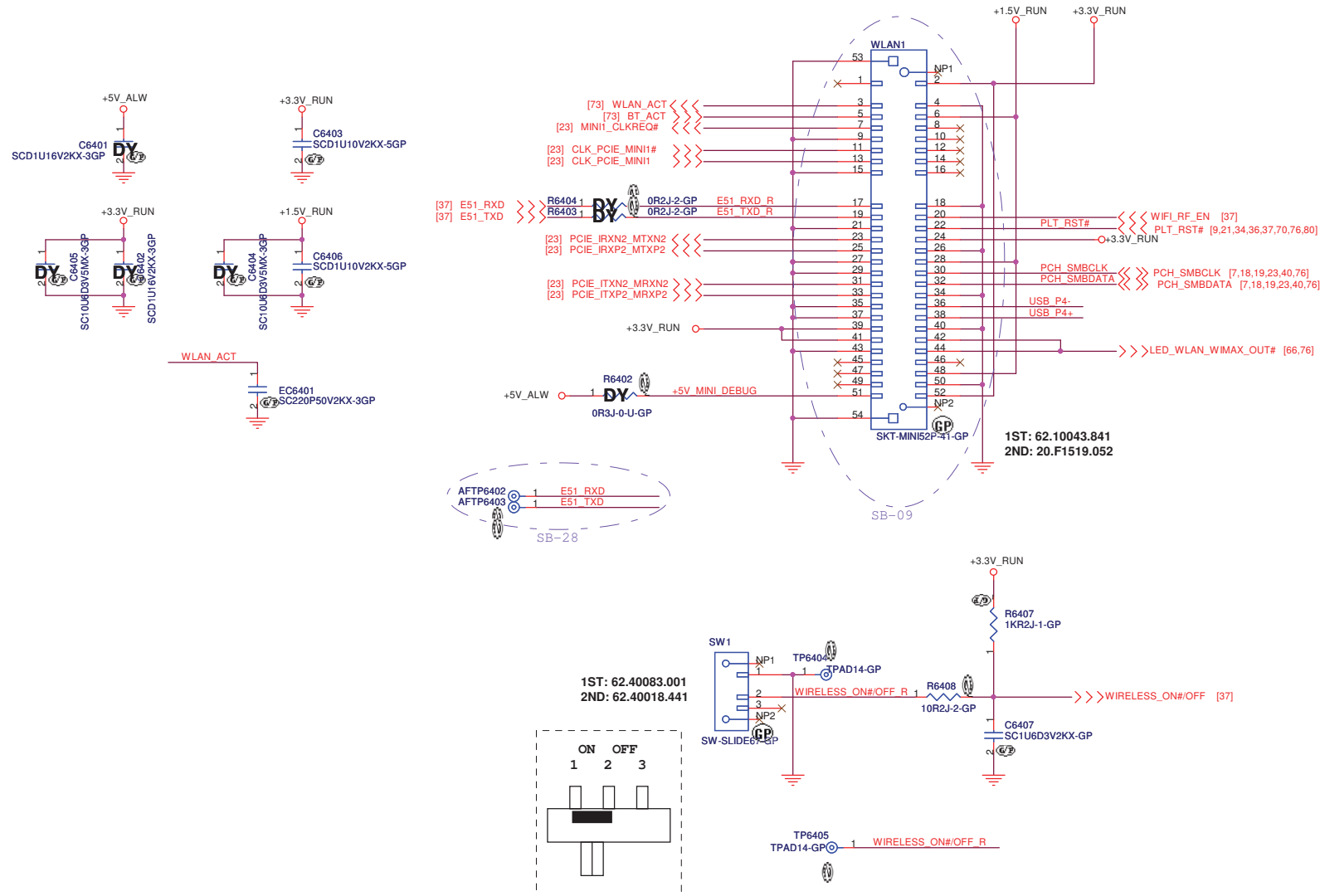
File: **USB/ESATA Port**

Size: Document Number
Customer: **Winery13 MB DIS**

Date: Wednesday, January 13, 2010 Sheet: 63 of 88

SSID = Wireless

Mini Card Connector(802.11a/b/g/n)



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DELL Wistron Corporation
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **MINICARD(WLAN)/ITP CONN**

Size A3	Document Number Winery13 MB DIS	Rev A00
Date: Wednesday, January 13, 2010	Sheet 64 of 88	

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1st Samsung

DELL **Wistron Corporation**
21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	
WWAN Connector	
Size	Document Number
A3	Winery13 MB DIS
Date: Wednesday, January 13, 2010	Sheet 65 of 88
Rev A00	

SSID = LED

For LED & Capacity board:

LED Type	Color	Power rail
BATTERY LED1	Amber (Multi-color)	ALW
SCRL LED	White	ALW
CAP LED	White	ALW
NUM LED	White	ALW
PWR BTN LED	White	ALW
SATA ACT LED1	White	RUN
BT ACT LED	White	RUN
WLAN/WWAN ACT LED	White	RUN

PWR BTN LED



SCRLK LED



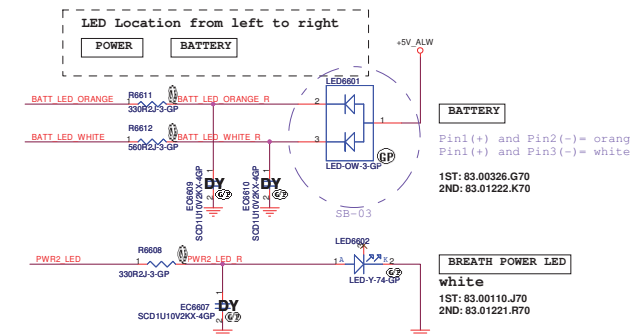
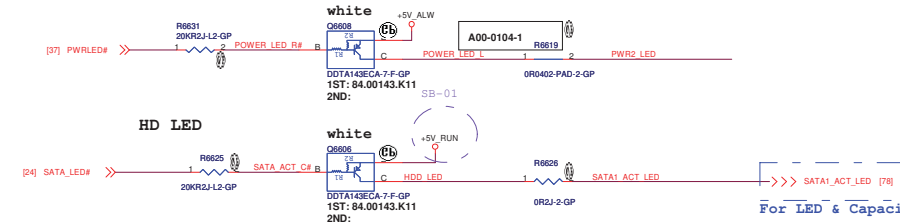
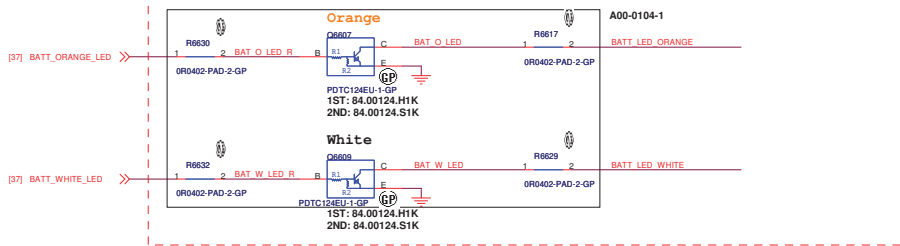
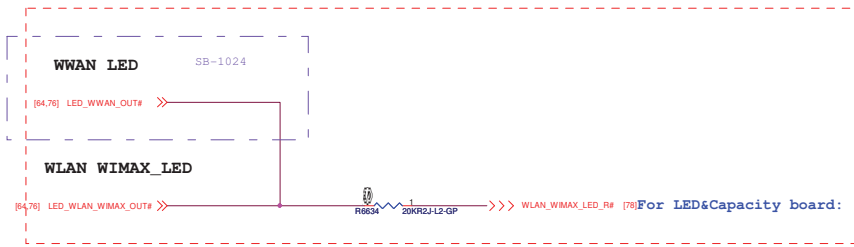
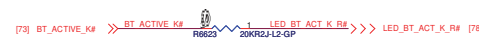
CAPS LED



NUM LED




Bluetooth LED



Remove HDD LED

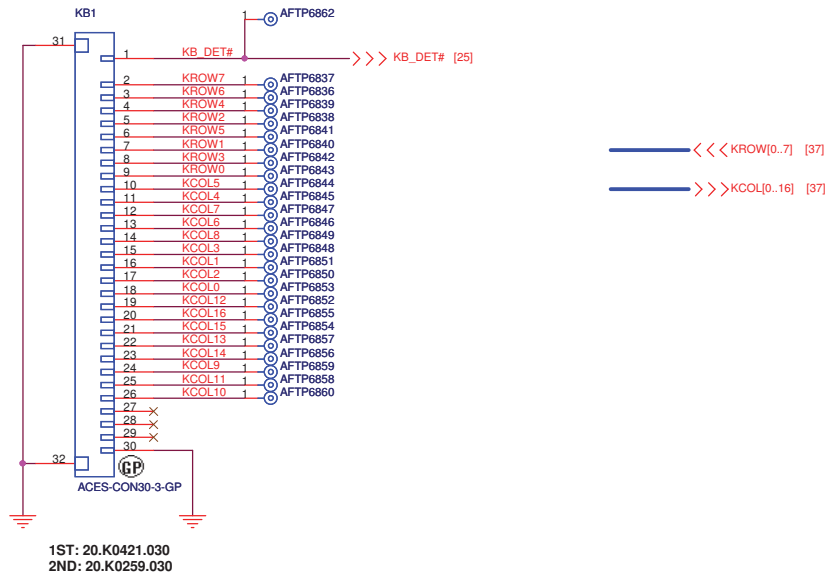
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1st Samsung

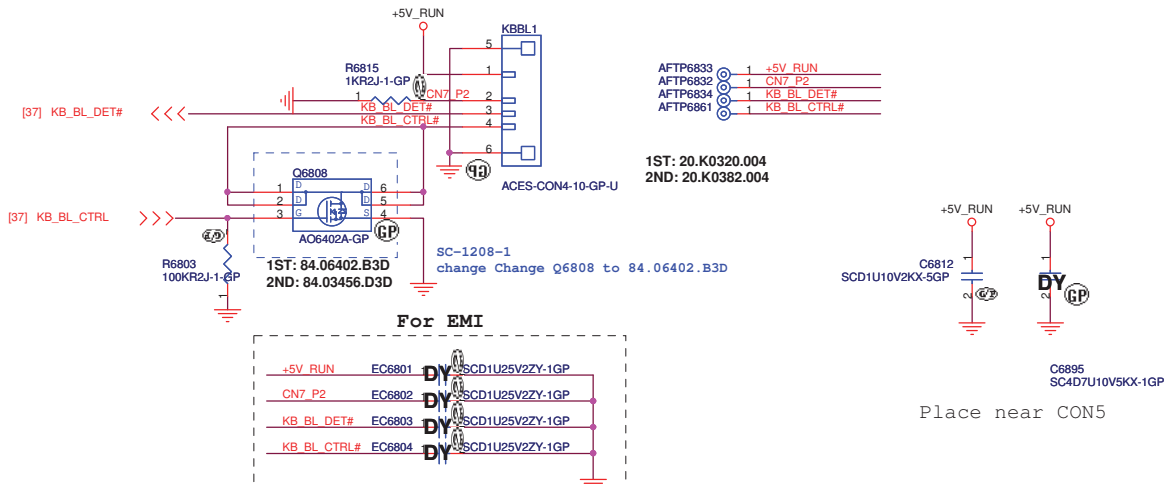
			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserve)					
Size	Document Number				Rev
Custom	Winery13 MB DIS				A00
Date:	Wednesday, January 13, 2010			Sheet	67 of 88

SSID = KBC

Internal Keyboard Connector

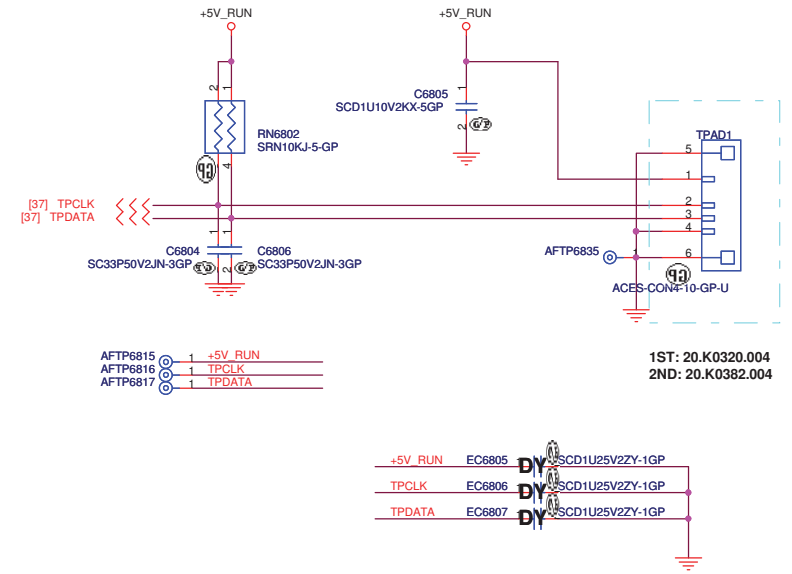


KB Backlight CONN



SSID = Touch.Pad

TouchPad Connector



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Title

Keyboard/Touch Pad

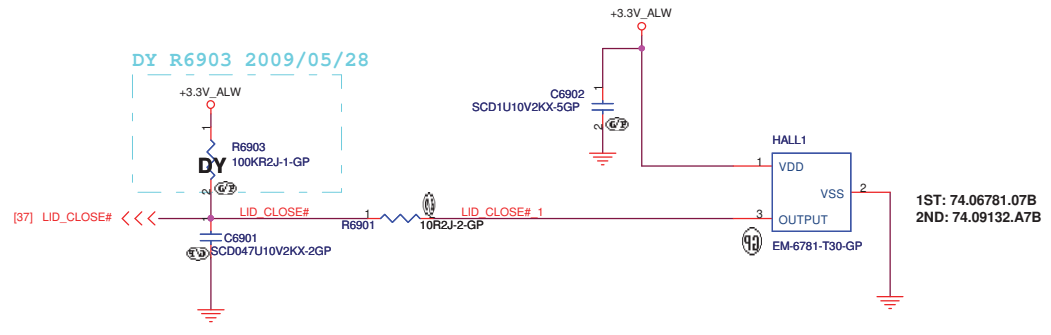
Size Document Number Rev

Custom **Winery13 MB DIS** A00


Date: Wednesday, January 13, 2010 Sheet 68 of 88

SSID = User.Interface

Hall Sensor Connector



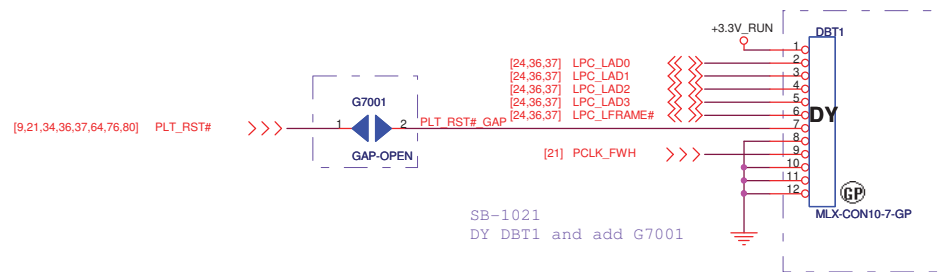
1st Samsung

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
Hall sensor					
Size	Document Number				Rev
Custom	Winery13 MB DIS				A00
Date:	Wednesday, January 13, 2010		Sheet	69	of 88

<http://laptop-motherboard-schematic.blogspot.com/>


SSID = DEBUG PORT

GOLDEN FINGER FOR DEBUG BOARD



<http://laptop-motherboard-schematic.blogspot.com/>


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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Debug port					
Size	Document Number			Rev	
Custom	Winery13 MB DIS			A00	
Date:	Wednesday, January 13, 2010	Sheet	70	of	88

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<http://laptop-motherboard-schematic.blogspot.com/>

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			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
(Reserve)					
Size	Document Number				Rev
Custom	Winery13 MB DIS				A00
Date: Wednesday, January 13, 2010			Sheet	71	of 88

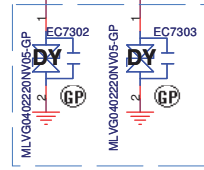
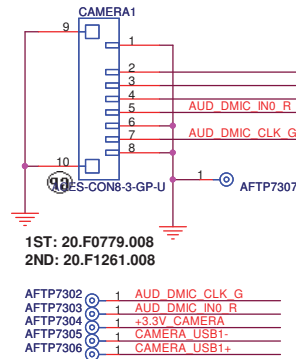
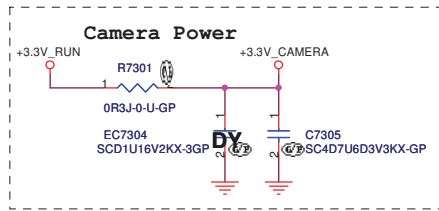
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1st Samsung

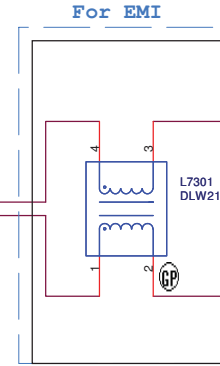
			Wistron Corporation 21F, 88, Sec.1, Hsin Tai WJ Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title			Braidwood
Size	Document Number	Rev	
Custom	Winery13 MB DIS	A00	
Date:	Wednesday, January 13, 2010	Sheet	72 of 88

SSID = User.Interface

Camera Connector



For ESD

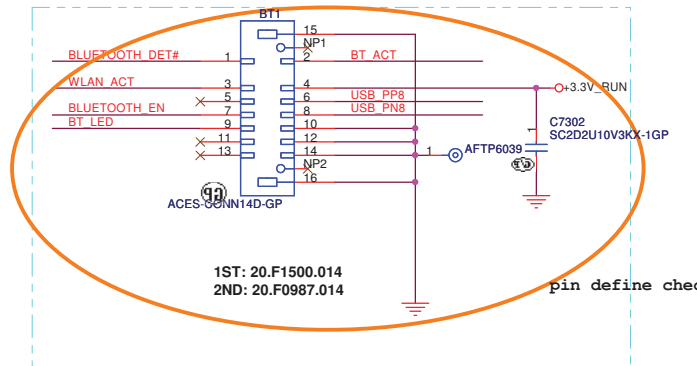
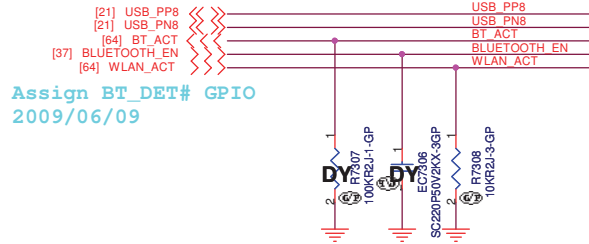


SC-1208-1
pop L7301 for EMI

A00-0107-1
remove R7302, R7303 for no co-lay after XB

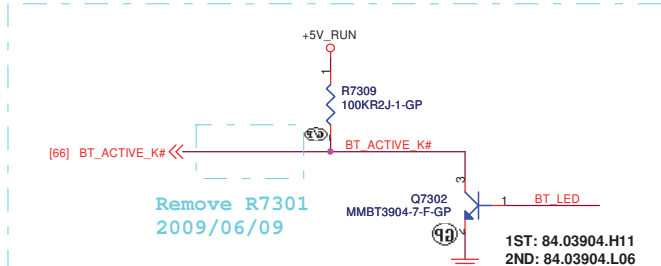
SSID = User.Interface

Bluetooth cable conn.

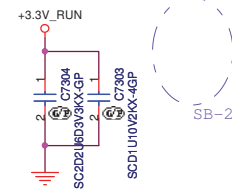


pin define check

BT LED control signal 2009/05/26



Close to BT1



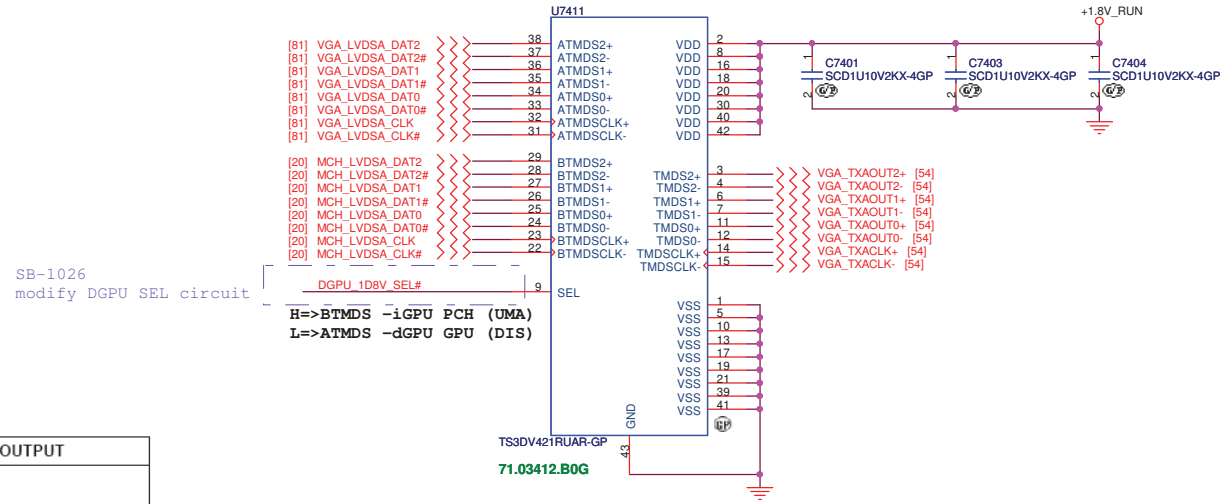
1st Samsung



Title		
Camera CONN		
Size	Document Number	Rev
A3	Winery13 MB DIS	A00
Date: Wednesday, January 13, 2010	Sheet 73 of 88	

SSID = VIDEO

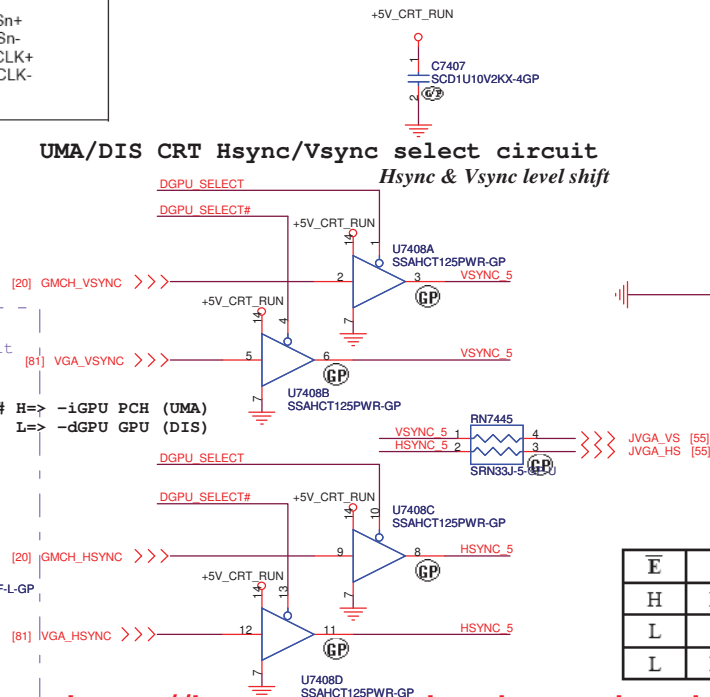
UMA/DIS LVDS signal select circuit



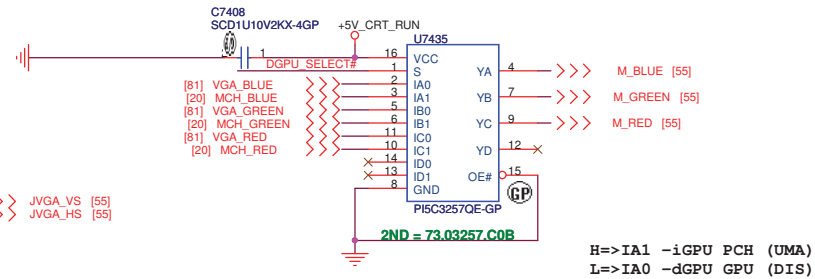
FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMSn+ TMDSn- = ATMSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMSn+ = High Impedance BTMSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMSn+ TMDSn- = BTMSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMSn+ = High Impedance ATMSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

UMA/DIS CRT Hsync/Vsync select circuit
Hsync & Vsync level shift



UMA/DIS CRT signal select circuit



\bar{E}	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

1st Samsung

DELL Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.


Title: **PX Swith-1**

Size: Custom Document Number: **Winery13 MB DIS** Rev: **A00**

Date: Wednesday, January 13, 2010 Sheet 74 of 88

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1st Samsung

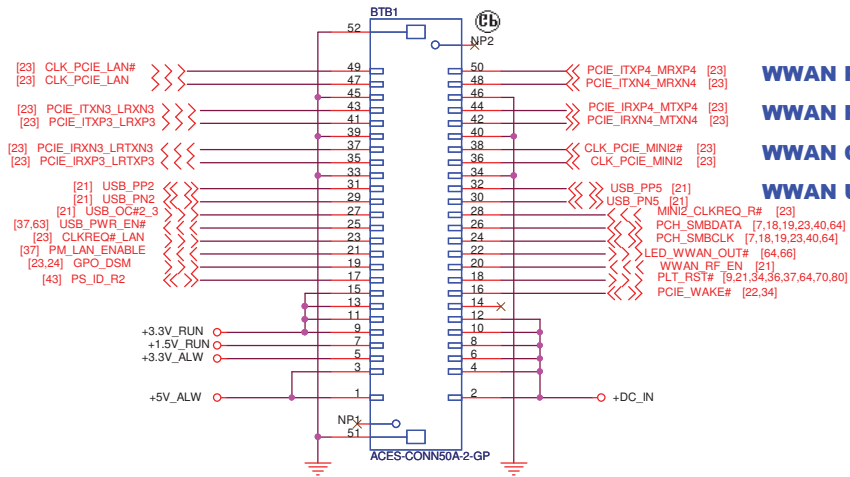
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title		
<i>(Reserve)</i>		
Size	Document Number	Rev
A3	Winery13 MB DIS	A00
Date: Wednesday, January 13, 2010		Sheet 75 of 88

DC_IN board CON

+DC_IN : 19.5V/85W
 +3.3V_RUN : 3300mA
 +5V_ALW : 1000mA
 +1.5V_RUN : 500mA
 +3.3V_ALW : 58mA

Please reoute 300 mil at least.

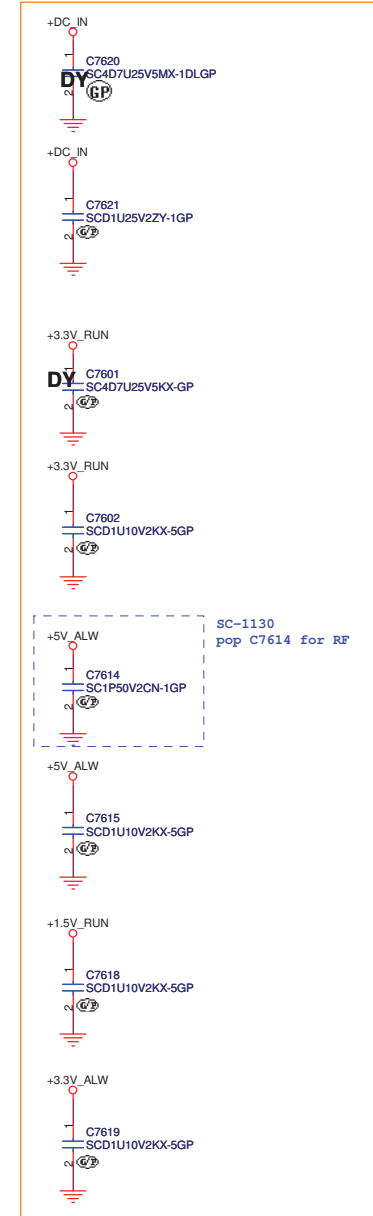
LAN CLK
 LAN PCIE
 LAN PCIE
 USB PORT2



Remove AFTP test point
 Confirmed with AFTE.

1ST: 20.F1631.050
 2ND:

Place near BTB1




<Core Design>

<http://laptop-motherboard-schematic.blogspot.com/>

Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title DC_IN Board BTB Connector		
Size	Document Number	Rev
Custom	Winery13 MB DIS	A00
Date:	Wednesday, January 13, 2010	Sheet 76 of 88

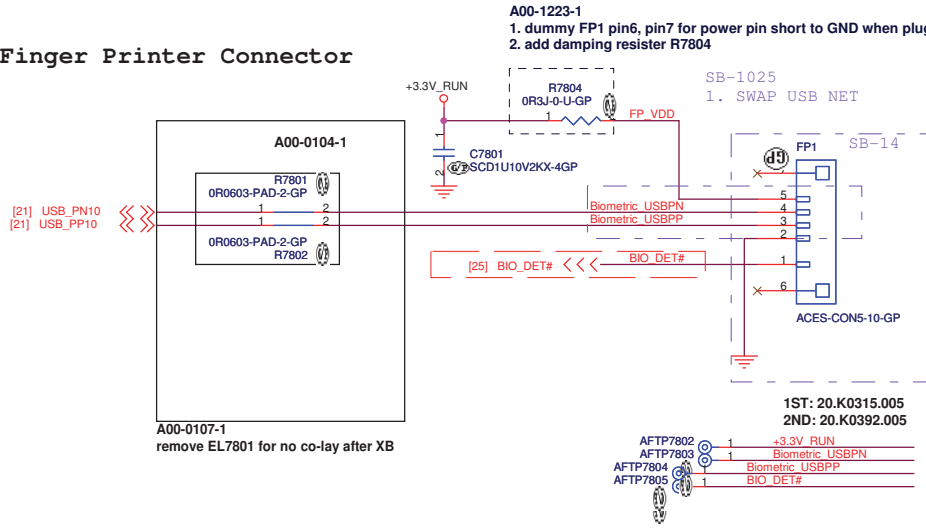
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1st Samsung

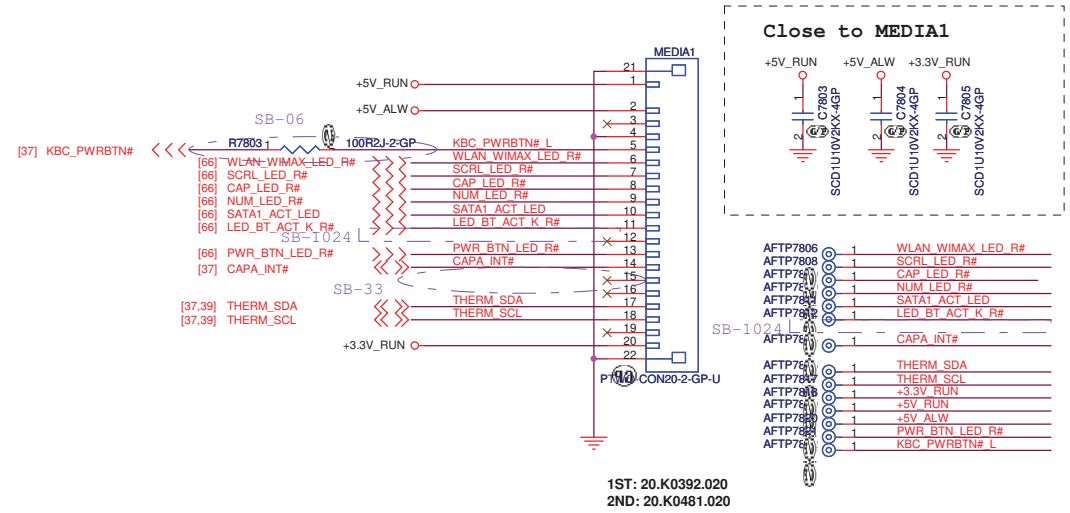
			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title			
Audio BD/IO BD CONN			
Size	Document Number	Rev	
Custom	Winery13 MB DIS	A00	
Date: Wednesday, January 13, 2010		Sheet 77	of 88

SSID = User.Interface

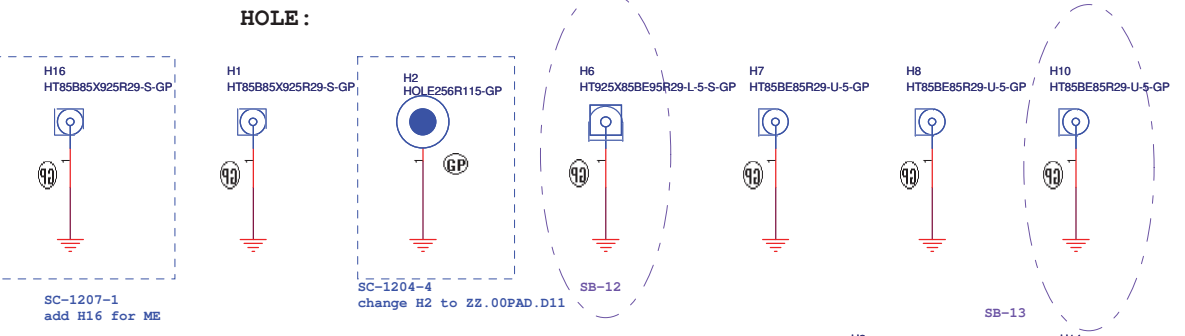
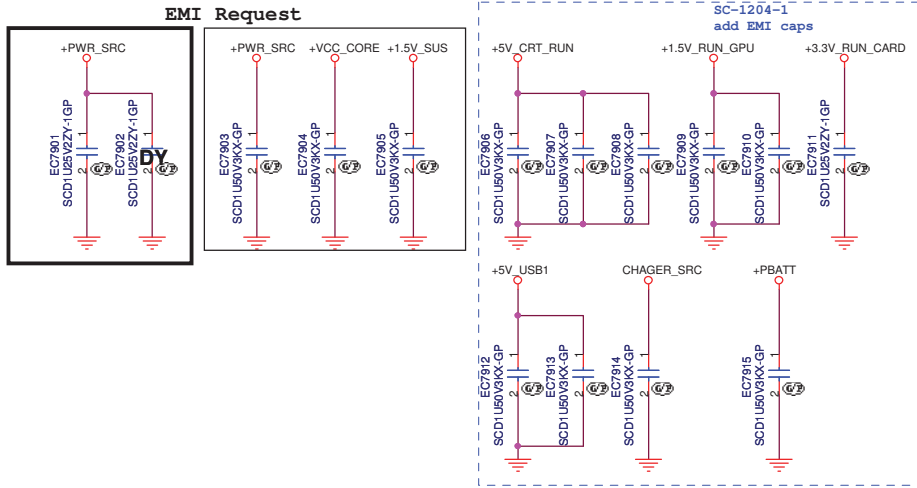
Finger Printer Connector



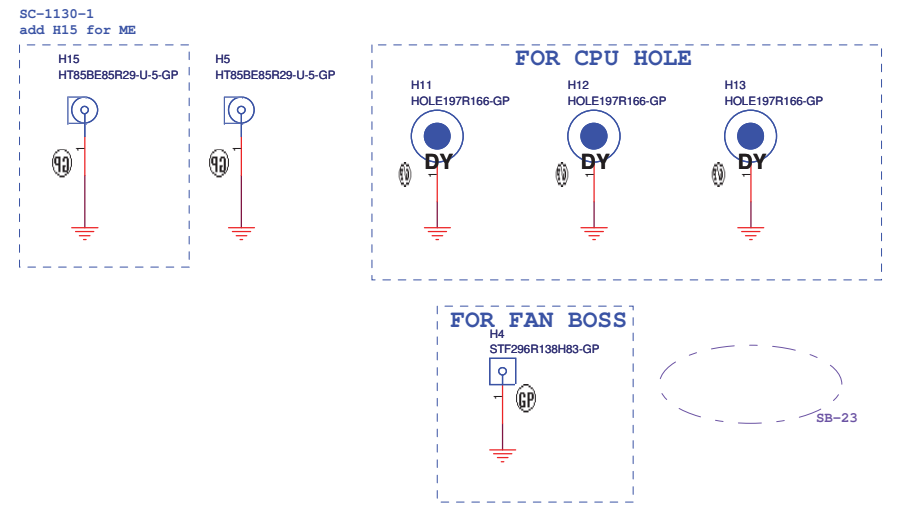
LED&Capacity board CONN



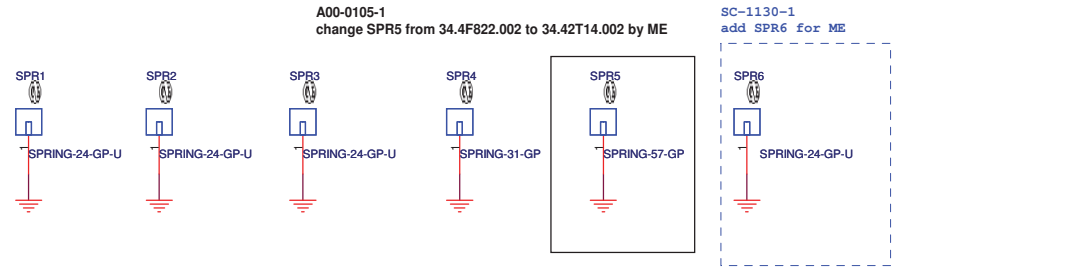
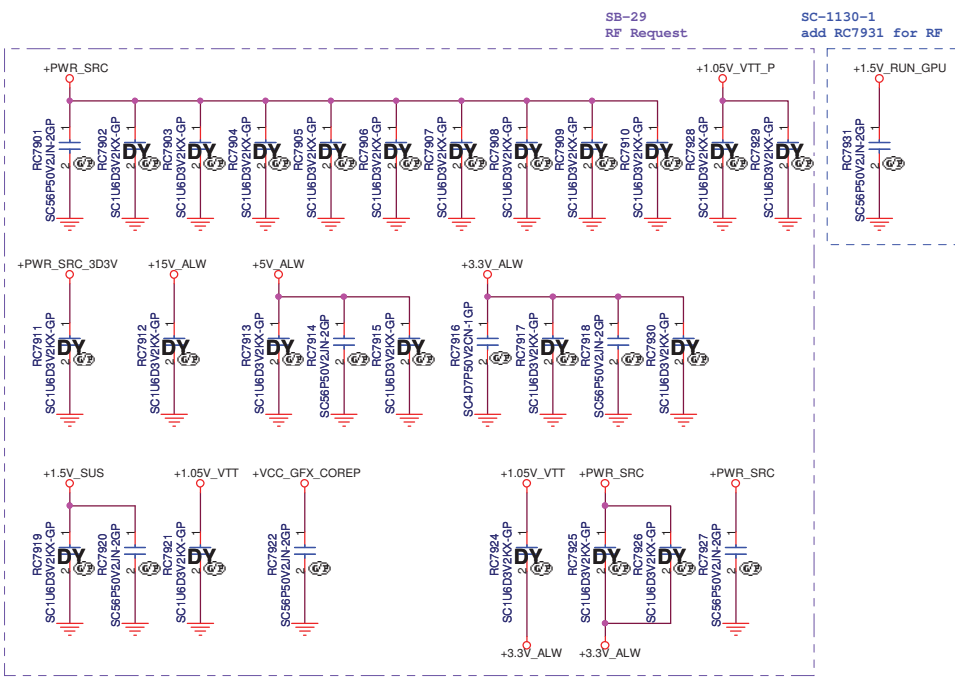
SSID = EMI



SSID = Mechanical



SSID = RF



<http://laptop-motherboard-schematic.blogspot.com/>

1st Samsung

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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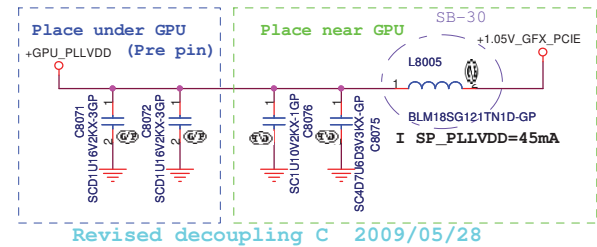
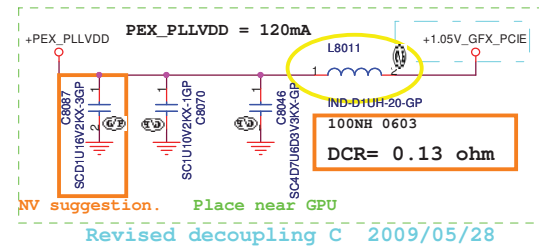
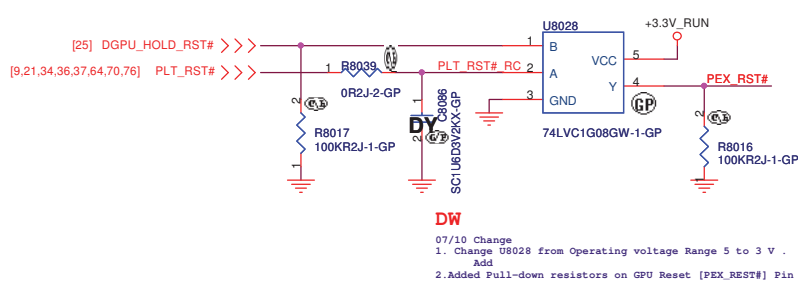
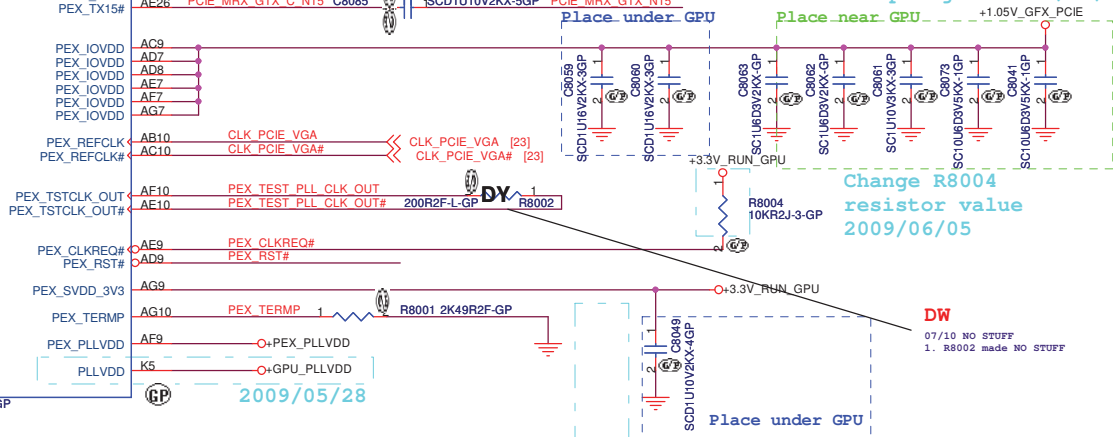
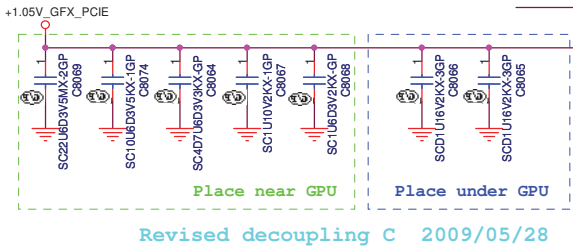
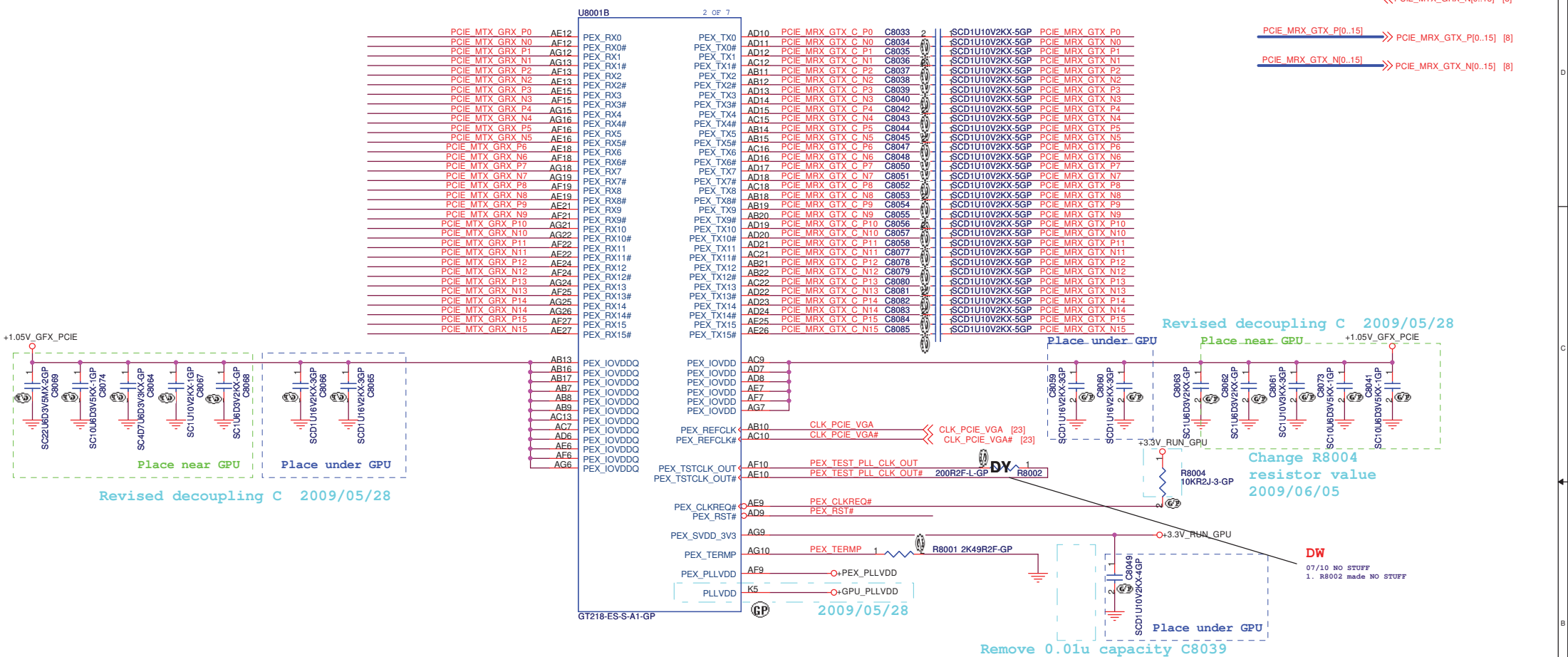
Title: **Miscellaneous Components**

Size: Custom	Document Number: Winery13 MB DIS	Rev: A00
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Date: Wednesday, January 13, 2010 Sheet 79 of 88

SSID = VIDEO

PCIE_MTX_GRX_P[0..15] << PCIE_MTX_GRX_P[0..15] [8]
 PCIE_MTX_GRX_N[0..15] << PCIE_MTX_GRX_N[0..15] [8]
 PCIE_MRX_GTX_P[0..15] >> PCIE_MRX_GTX_P[0..15] [8]
 PCIE_MRX_GTX_N[0..15] >> PCIE_MRX_GTX_N[0..15] [8]



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21F, 88, Sec. 1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

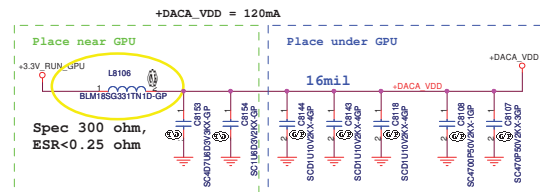
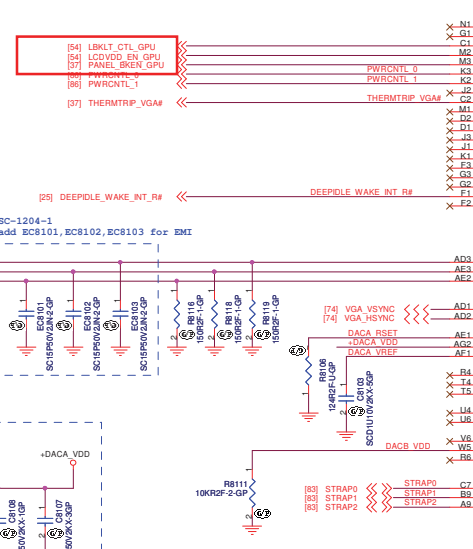
Title: **VGA-PCIE/LVDS(1/4)**

Size A3 Document Number: **Winery13 MB DIS** Rev: **A00**

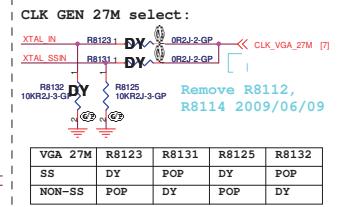
Date: Wednesday, January 13, 2010 Sheet 80 of 88

SSID = VIDEO

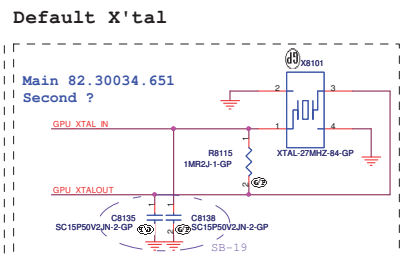
07/65
 1. LCD brightness control are separated by GPU, PCM, RC
 2. LCD Power Enable control are separated by GPU, PCM, RC
 3. LCD Backlight On/Off Status are separated by GPU, PCM, RC
 07/10 Not Reserve
 1. Shared LANE0_CTL_GPU, LCDVDD_EN_GPU, PANEL_BKEN_GPU Not Reserve R8134, R8135, R8136.



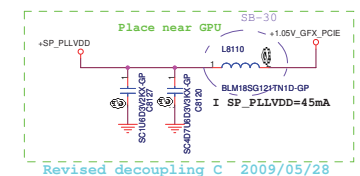
Revised decoupling C 2009/05/28



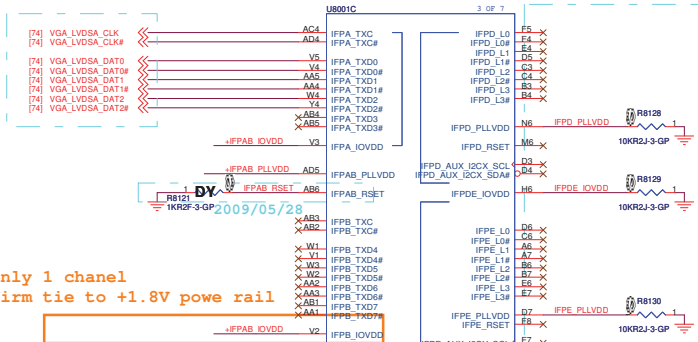
Added CLK GEN 27M select circuit 2009/06/15
 Added R8132 (DY) 2009/06/17



1st: HARMONY 82.30034.651
 2nd: ITTI 82.30034.801
 3rd: TXC 82.30034.681

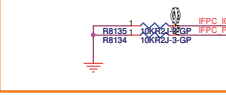


Revised decoupling C 2009/05/28

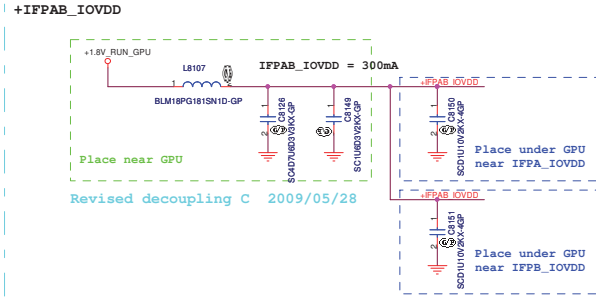


DW30 LVDS only 1 channel
 Vendor confirm tie to +1.8V power rail

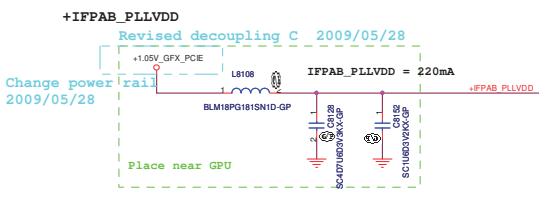
DW30 not support HDMI
 NV DG: pull-down 10K



Unused IFP Interfaces setting 2009/06/03

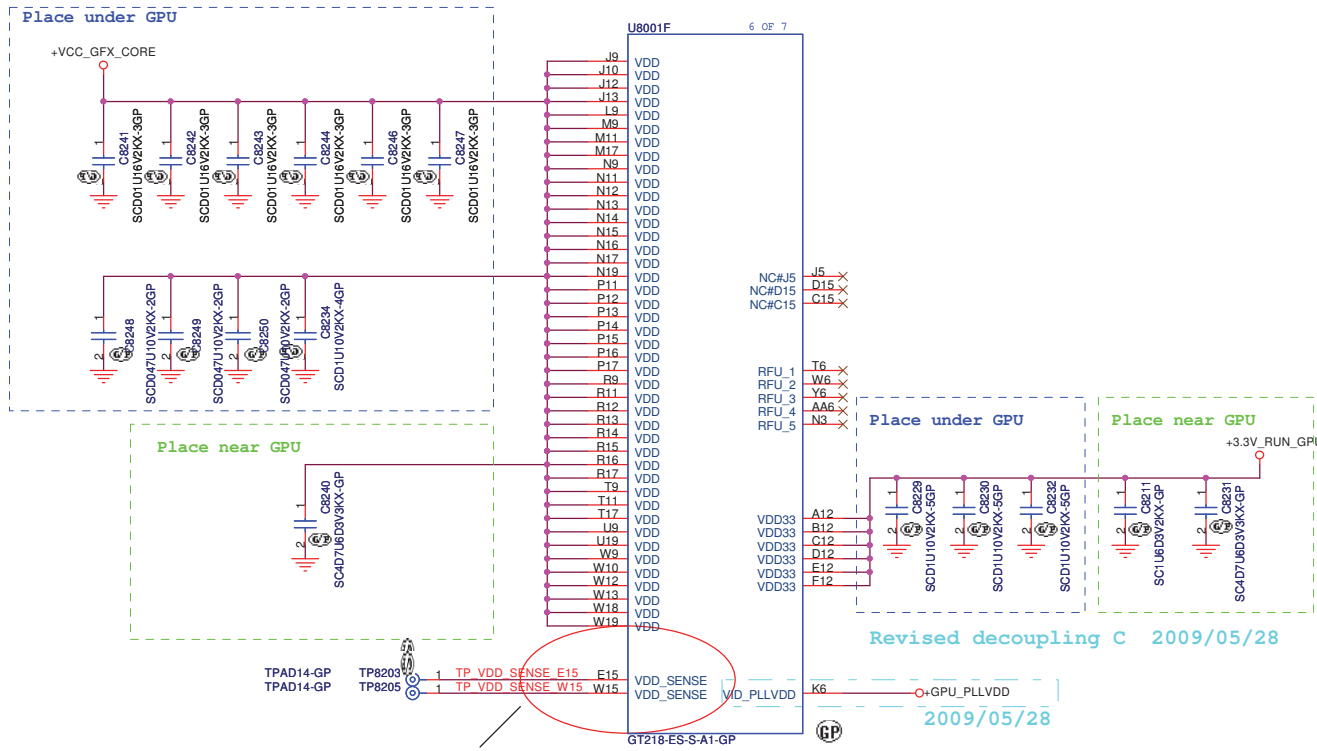


Revised decoupling C 2009/05/28



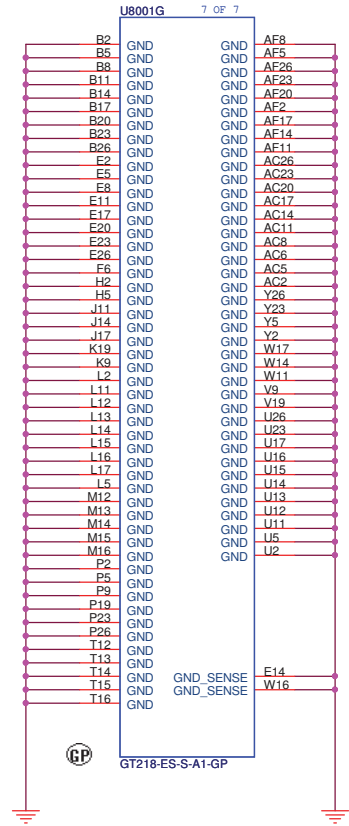
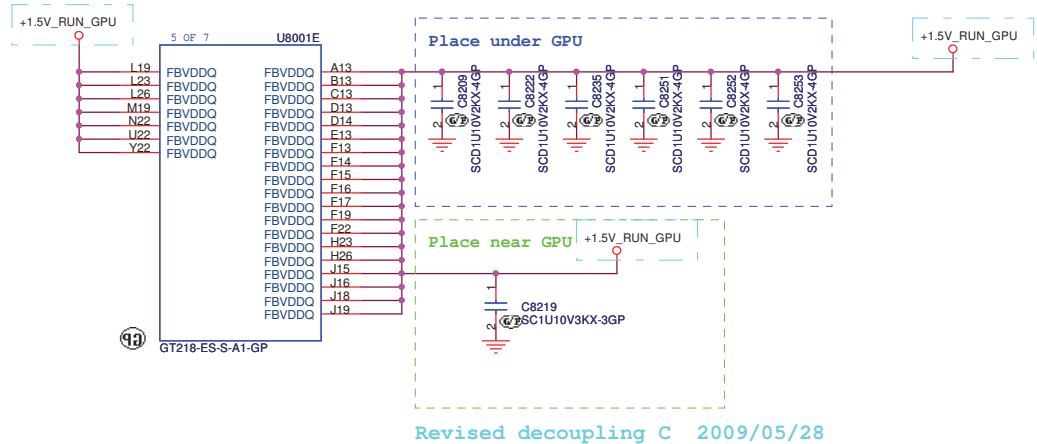
Change power rail 2009/05/28

Revised decoupling C 2009/05/28

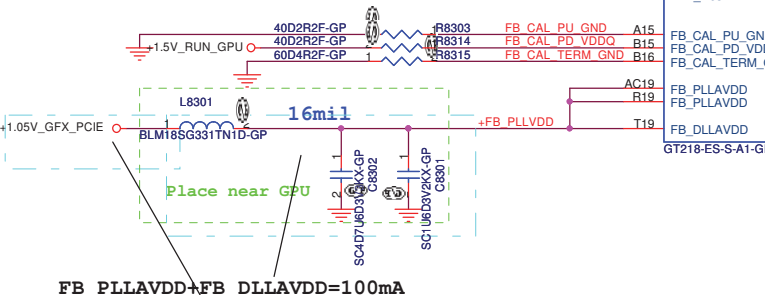


"Remote Voltage Sensing" not used, reserve Test-Point.

Change FBVDDQ power rail 2009/05/28



SSID = VIDEO

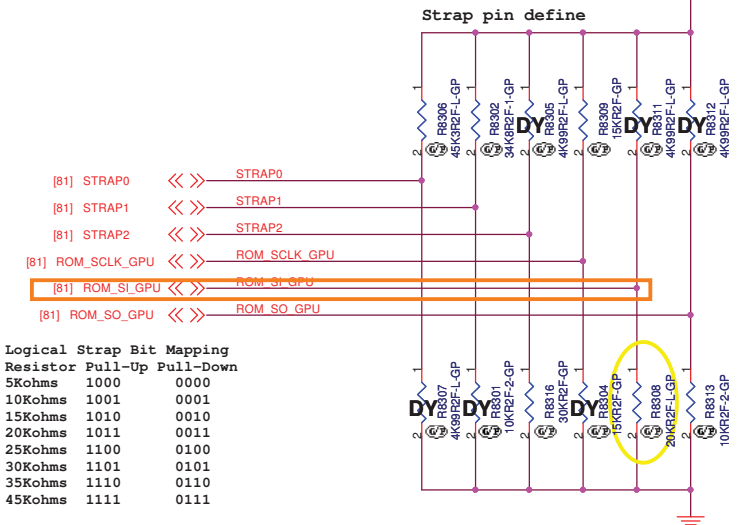


FB_PLLAVDD+FB_DLLAVDD=100mA

DW

07/10 Updated
1.*FB_PLLVDD power rail corrected to +1.05V_GFX_PCIE

Strap pin resistor need use 1% resistor (NV Design Guide)



Strap0	Strap1	Strap2
USER_BIT0 1	3GIO_PADCFG_LUT_ADRO 0	PCI_DEVID_0 1
USER_BIT1 1	3GIO_PADCFG_LUT_ADRI 1	PCI_DEVID_1 0
USER_BIT2 1	3GIO_PADCFG_LUT_ADRI 1	PCI_DEVID_2 1
USER_BIT3 1	3GIO_PADCFG_LUT_ADRI 1	PCI_DEVID_3 0
EDID is used	Reserved	N11M-GE1 GPU Device ID=0x0A75

ROM_SI_GPU	ROM_SO_GPU	ROM_SCLK_GPU	
RAM_CFG0	VGA_DEVICE 1	PEX_PLL_EN_TERM	0
RAM_CFG1	SMB_ALT_ADDR 0	SLOT_CLK_CONFIG	1
RAM_CFG2	FB_0_BAR_SIZE 0	SUB_VENDOR	0
RAM_CFG3	XCLK_417 0	PCI_DEVID_4	1

Default setting: SAMSUNG sDDR3 64Mx16BIT-->20K pull down (0x0011)
If use Hynix sDDR3 64Mx16BIT(0x0010), R8308 change to 15K.

RAM_CFG[3:0] Config FB_BUS Width Definitions

Config	FB_BUS Width	Definitions
0000		
0001		
0010	64MX16	DDR3 64Bit Hynix
0011	64MX16	DDR3 64Bit Samsung
0100		Default
0101		
0110		
0111		

SUB_VENDOR	XCLK_417	PEX_PLL_EN_TERM
0 No VBIOS ROM	0 277MHz (POR)	0 Disable (POR)
1 BIOS ROM present	1 Reserved	1 Enable

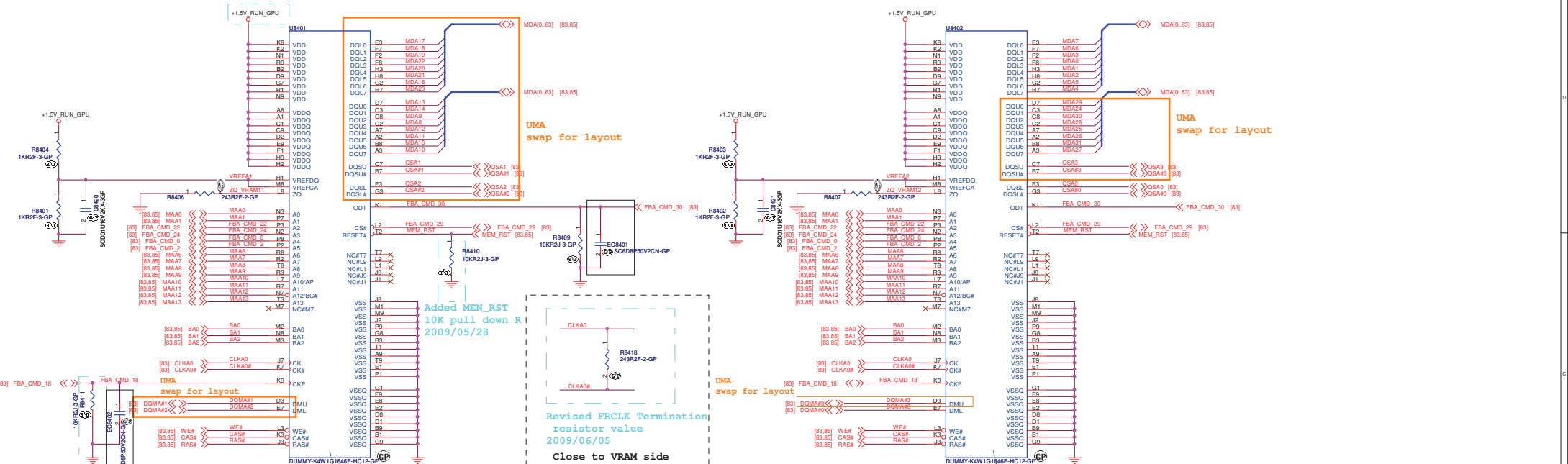
3GIO_PADCFG USER[3:0]
0000 Desktop 1111 Use EDID to detect panel settings
1110 Notebook (POR)

SLOT_CLOCK_CFG
0 GPU and MCH do not share a common reference clock
1 GPU and MCH share a common reference clock (POR)

1st Samsung

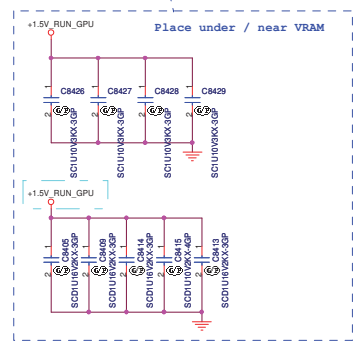
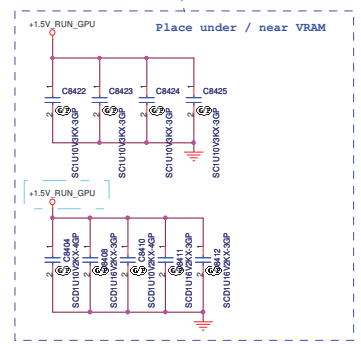


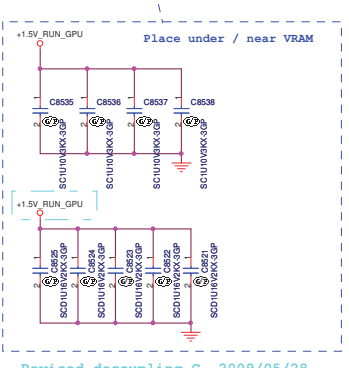
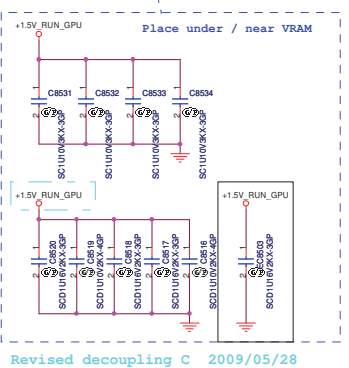
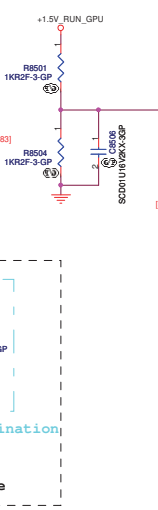
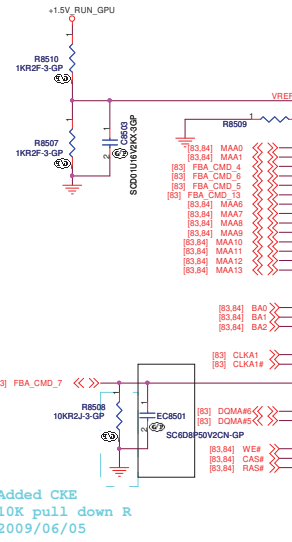
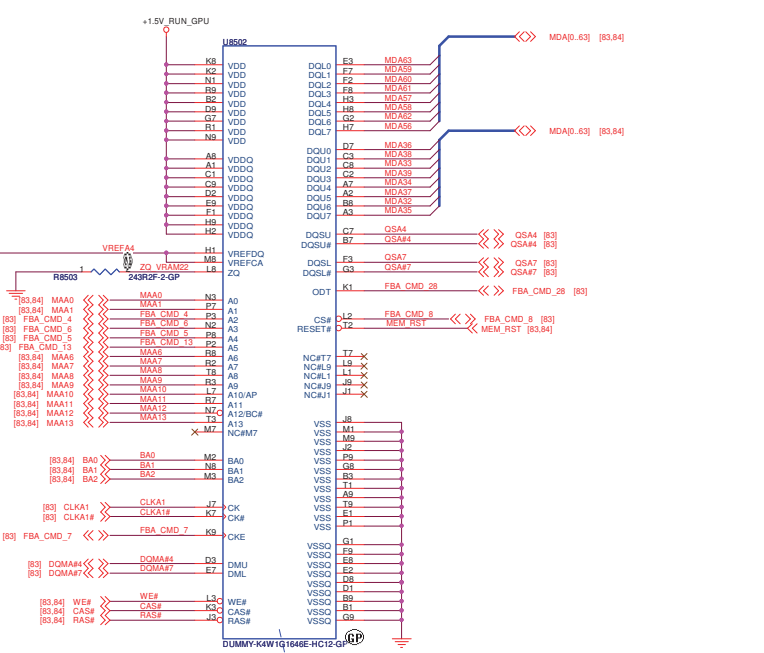
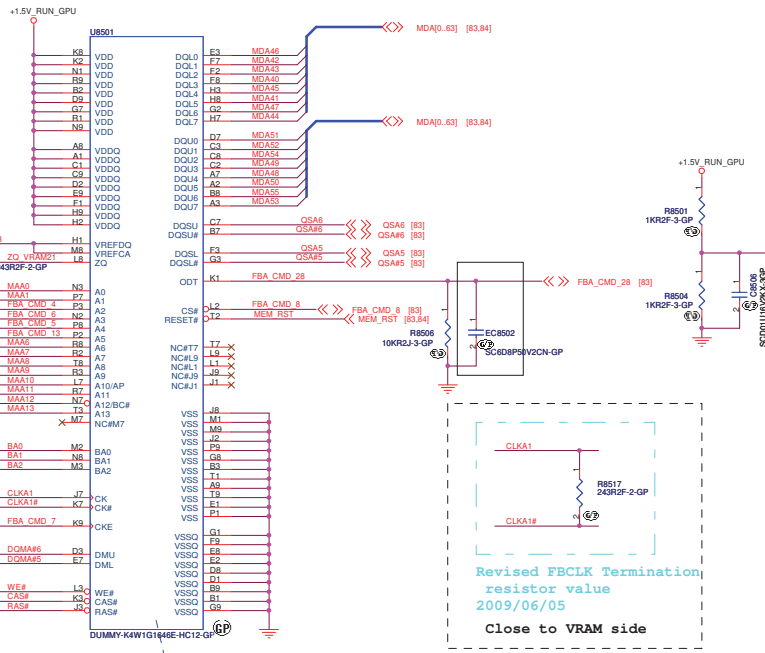
Title		VGA-MEMORY/STRAPS(4/4)	
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Added CKE 10K pull down R 2009/06/05

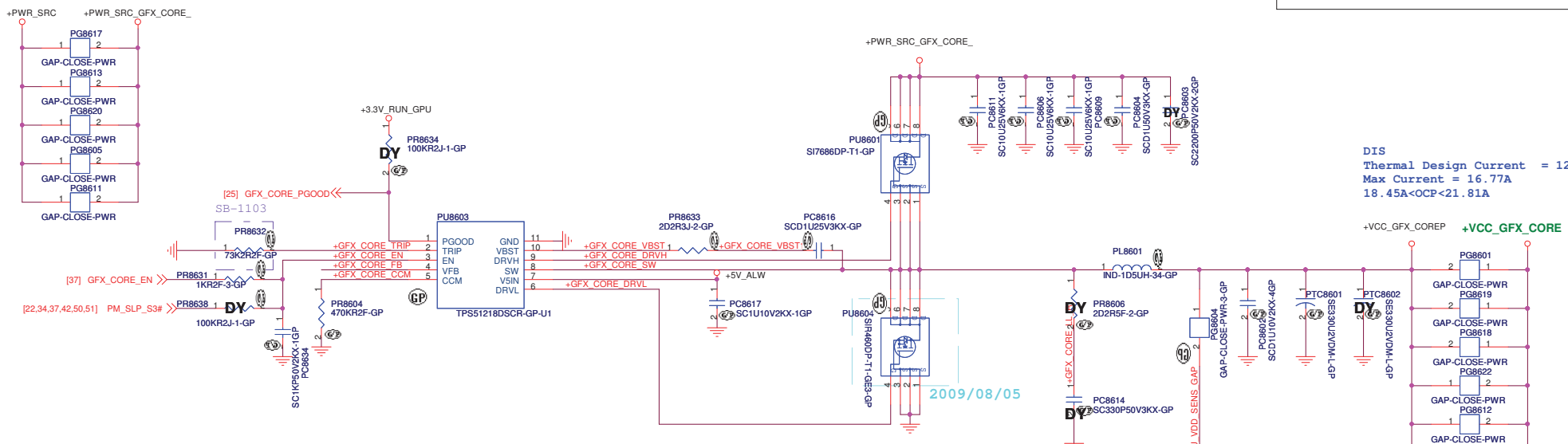
64X16 SAMSUNG K4W1G1646E-HC12 P/N:72.41164.H0U
 64X16 HYNIX H5TQ1G63BFR-12C P/N:72.51G63.C0U
 SC-1203-2
 change U8401, U8402 to Z5.00PAD.R01 for layout





SSID = PWR.Plane.Regulator_GFX

$$V_{out} = 0.704V * (R1 + R2) / R2$$



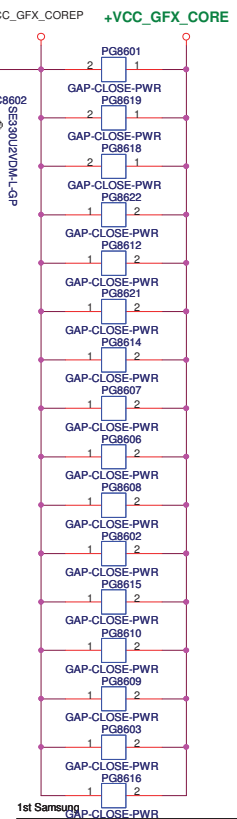
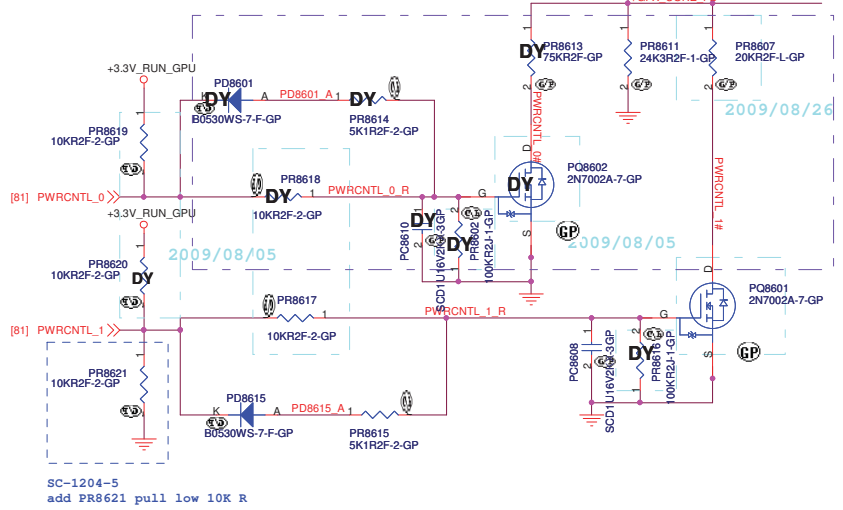
DIS
 Thermal Design Current = 12.9A
 Max Current = 16.77A
 18.45A < OCP < 21.81A

Frequency setting
 470K --> 290KHz
 200K --> 340KHz
 100K --> 380KHz
 39K --> 430KHz

SB-1023
 1. DY PD8601, PR8614, PR8618, PC8610, PG8602,
 PR8613; change PR8611 to 24.3K, PR8607 to 20K.
 for N11M A3 change P12 stay Voltage to 0.85V

PWRCNTL_0	PWRCNTL_1	+VCC_GFX_CORE
H	H	1.03V
H	L	0.85V

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
 Inductor: 1.5UH PCMC104T-1R5MN Cyntec DCR:4.2mohm Isat =33Arms 68.1R510.10J
 O/P cap: 330U 2V EEPFX0D331ER 9mOhm 3Arms Panasonic/ 79.33719.L01
 H/S: SI7686DP/ POWERPAK-8/ 11mOhm/ 14mOhm @ 4.5Vgs/ 84.07686.037
 L/S: SiR460DP/ POWERPAK-8/ 4.9mOhm/ 6.1mOhm @ 4.5Vgs/ 84.00460.037
 Switching freq --> 350KHz



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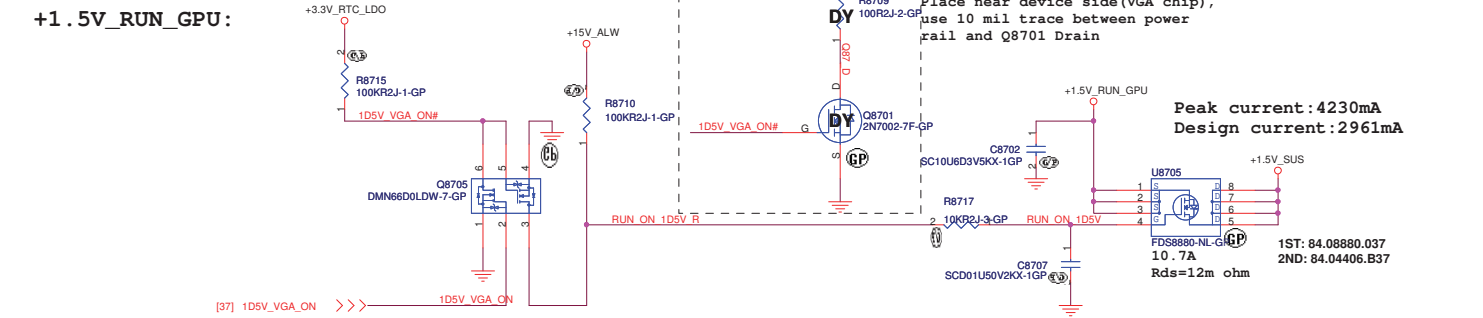
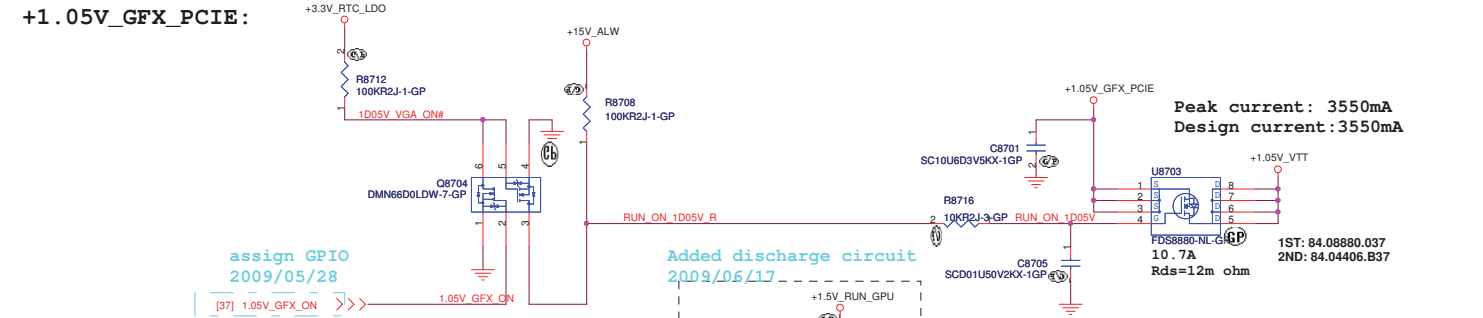
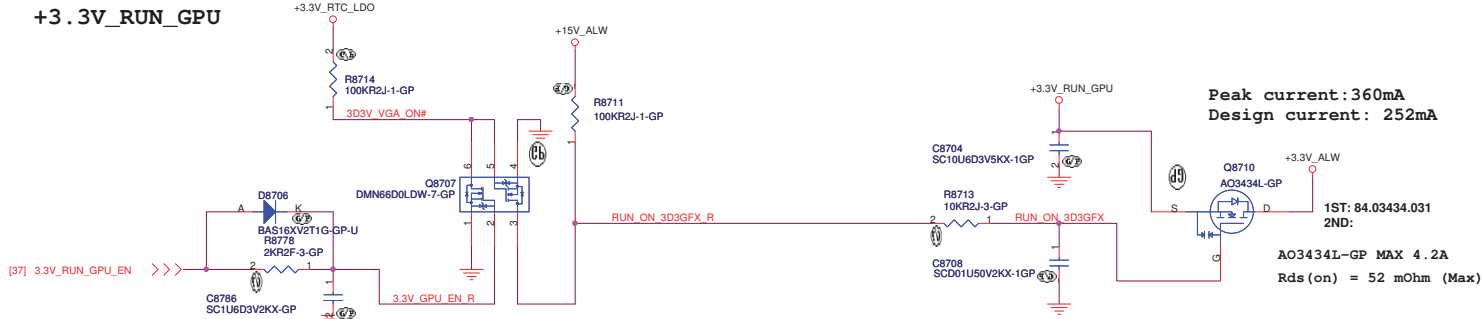
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Title: **TPS51218 +VCC GFX CORE**

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SSID = VIDEO



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Title: **LDO 1.8V**

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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
01	66	2009/10/08	EE	HDD LED light in S5.	Change HDD LED power rail from +5V_ALW to +5V_RUN.	SB
02	60	2009/10/08	EE	External MIC NG.	Add caps C6014 C6015.	SB
03	66	2009/10/08	EE	Correct battery LED color.	Swap LED6601 pin2 & pin3.	SB
04	49	2009/10/08	EE	Improve VTT_PWRGD ramp up signal.	Dummy C4912.	SB
05	51	2009/10/08	EE	Fine tune +1.8V_RUN power on sequence behind +3.3V_RUN.	Change PR5102 from 2.2K to 3K and PC5105 from 4700pF to 1uF.	SB
06	54, 78	2009/10/08	EE	For KBC ESD protect.	Add 100 ohm resistances R5413, R7803.	SB
07						
08	30	2009/10/08	EE		Change CODEC to 92HD79.	SB
09	64	2009/10/08	EE	By ME request	Change WLAN1 to 62.10043.841.	SB
10						
11	37	2009/10/09	EE	Change board ID.	Dummy R3708 and pop R3701.	SB
12	79	2009/10/12	ME	By ME request	Change H6 to ZZ.00PAD.F91	SB
13	79	2009/10/12	ME	By ME request	Change H10 to ZZ.00PAD.D41	SB
14	78	2009/10/12	ME	By ME request	Change FP1 to 20.K0315.005	SB
15	27	2009/10/12	EE	Follow Intel spec	Remove L2701, C2701, C2702; Add TP2701	SB
16	27	2009/10/12	EE	Follow Intel spec	Remove L2704, C2721, C2722; Add TP2702	SB
17	27	2009/10/12	EE	Cost down	Change L2702, L2703 to 68.10050.10Y	SB
18	24	2009/10/12	EE	XTAL Load Capacitance as Vendor suggestion	Change C2402, C2403 to 12pF	SB
19	81	2009/10/12	EE	XTAL Load Capacitance as Vendor suggestion	Change C8135, C8138 to 15pF	SB
20	26	2009/10/13	EE	Follow Intel spec	Remove L2602, C2616; Add TP2601	SB
21	26	2009/10/13	EE	Follow Intel spec	Remove L2601, C2606; Add TP2602	SB
22	37	2009/10/13	EE	Modify 10mW schematic		SB
23	79	2009/10/13	ME	By ME request	Remove H9 (BT BOSS)	SB
24	49	2009/10/13	EE	By PSE request	Change pg4910~pg4918 and pg4921 close gap to mask type	SB
25	73	2009/10/13	EE	Two AFTP for +3.3V_RUN	Remove AFTP6030	SB
26	34	2009/10/14	ME	By ME request	change NEW1 connector to 20.K0370.026	SB
27	79	2009/10/14	ME	By ME request	change SPR5 to 34.4F822.002	SB
28	64	2009/10/14	EE	By AFTE request	Add AFTP6402, AFTP6403	SB
29	79	2009/10/16	EE	By RF request	Add Cross Moat Caps	SB
30	80, 81	2009/10/16	EE	Voltage Drop over 3%	change bead value to 120 ohm DCR 0.55 ohm	SB
31	22	2009/10/16	EE	RTC data loss	Added 3v/5v S5 power good to control resume reset sequence prevent RTC data loss	SB
32	25	2009/10/16	EE		Swapped Q2515 C,E Pin	SB
33	78	2009/10/16	EE		remove CAPA_RST# from capacity board	SB
34	37	2009/10/16	EE	By SW request	Added Switch Board Detection circuit	SB

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Title: **Change List(1/3)**


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Item	Page#	Date	Request By	Issue description	Solution Description	Rev.
01	37	2009/11/18	EE	Correct R3745 power rail to KBC_PWR	Change R3745 power rail to KBC_PWR	SC
02	36	2009/11/25	EE	TPM connector needn't AFTE test point	Remove TPM1 AFTP	SC
03	23	2009/11/25	EE	No support HDMI and eDP so needn't pop 25MHz Xtal of PCH.	C2313 pop 0 ohm if no use 25MHz XTAL	SC
04	37	2009/11/25	EE	Toggle VGA mode will flicker white screen in hybrid mode.	Add U3703 mux for panel backlight enable signal select	SC
05	54	2009/11/25	EE	Toggle VGA mode will flicker white screen in hybrid mode.	Add mux U5446 to select LCDVDD enable signal	SC
06	7	2009/11/30	RF	For solve WiMAX noise	Change C701 to 4.7pF for RF	SC
07	43	2009/11/30	RF	For solve WiMAX noise	Pop PC4303 for RF	SC
08	46	2009/11/30	RF	For solve WiMAX noise	Change PC4601 pull up to +5V_ALW for layout.	SC
09	47	2009/11/30	EE	For combine material item	Change PC4762 to 0603 size	SC
10	79	2009/11/30	ME	For one hand hold issue, ODD have noise	Add H15 for ME	SC
11	79	2009/11/30	RF	For solve WWAN noise	Add RC7931 for RF	SC
12	79	2009/11/30	RF	For solve WiMAX noise	Add SPR6 for RF	SC
13	55	2009/12/04	EMI	By EMI requirement	Change L5501,L5502,L5503 for EMI	SC
14	79	2009/12/04	EMI	By EMI requirement	Add EMI caps	SC
15	81	2009/12/04	EMI	By EMI requirement	Add EC8101,EC8102,EC8103 for EMI	SC
16	47	2009/12/04	ME	For cosmetic issue when insert 8 cell battery	Remove TC4701 for layout	SC
17	79	2009/12/04	ME	For cosmetic issue when insert 8 cell battery	Change H2 to ZZ.00PAD.D11	SC
18	30	2009/12/04	EE	Base on Application Note: IDT 92H81/79 AUX Mode as input of Diagnostic sound.	Connect U3001 pin17, pin18 to pin12 net and change R3016 to 120K for vendor request	SC
19	86	2009/12/04	EE	Set PWRCNTL_1 for default low.	Add PR8621 pull low 10K ohm	SC
20	12	2009/12/07	EMI	By EMI requirement	Pop C1243 and change size to 0603 for EMI	SC
21	33	2009/12/07	EMI	By EMI requirement	Pop C3301, EC3302, EC3303, EC3305, EC3306, EC3307, EC3308 and change from 100p to 6.8p for EMI	SC
22	54	2009/12/07	EMI	By EMI requirement	Pop EC5403 for EMI	SC
23	60	2009/12/07	EMI	By EMI requirement	Pop EC6001 and EC6002 for EMI	SC
24	63	2009/12/07	EMI	By EMI requirement	Pop R6307 for EMI	SC
25	79	2009/12/07	ME	For cosmetic issue when insert 8 cell battery	Add H16 for ME	SC
26	24	2009/12/08	EE	Base on EA teset result, change to 0 ohm.	Change R2413,R2414,R2415 from 15ohm to 0 ohm	SC
27	53	2009/12/08	EE	Base on ARD Sightings Report_18 #3622146	Change PR5311 from 4.7K to 470 ohm	SC
28	60	2009/12/08	EE	Audio AP LO THD+N fail	Change EC6004,EC6005 from 0.1U to 0.01U	SC
29	62	2009/12/08	EE	Base on EA teset result, change to 0 ohm.	Change R6206 from 15ohm to 0 ohm	SC
30	68	2009/12/08	EE	Change PCB Footprint	Change Q6808 to 84.06402.B3D	SC
31	73	2009/12/08	EMI	By EMI requirement	Pop L7301 for EMI	SC

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Title: **Change List(2/3)**


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01	34	2010/01/07	EE	For no co-lay after XB	remove R3402, R3403	A00
02	37	2010/01/05	EE	Prevent SPI ROM data lost	Add reset IC U3704	A00
03	46	2009/12/18	EE	By POWER requirement	changePL4602 from 2.2U to 3.3U	A00
04	46	2009/12/18	EE	TO improve +15V_Pump Power on issue	pop PR4619; dummy PR4618	A00
05	51	2010/01/07	EE	To prevent PM_SLP_S3# signal rebound	change R5102 to short pad, PC5105 to 10K	A00
06	52	2009/12/23	EE	PREVNET MOS DEMAGE	Change C701 to 4.7pF for RF	A00
07	53	2009/12/18	EE	By POWER requirement	change PR5314 from 5.9K to 6.2K	A00
08	55	2009/12/18	EMI	By EMI requirement	change L5501, L5502, L5503 to 0R	A00
09	55	2009/12/18	EMI	By EMI requirement	change R5504, R5505, R5506 from 0R to 33R	A00
10	55	2009/12/18	EMI	By EMI requirement	change C5520 from 22p to 10p	A00
11	55	2010/01/04	ME	By ME requirement	change CRT1 from 20.20431.015 to 20.20401.015	A00
12	62	2010/01/04	ME	By ME requirement	change RCT1 from 20.D0210.102 to 20.D0075.102	A00
13	63	2010/01/06	EE	For no co-lay after XB	remove R6302, R6308, TR6301, TR6302, TR6303	A00
14	64	2010/01/07	EE	For no co-lay after XB	remove L6401	A00
15	73	2010/01/07	EE	For no co-lay after XB	remove R7302, R7303	A00
16	78	2009/12/23	EE	TO PREVENT power pin short to GND when plug in cable	dummy FP1 pin6, pin7	A00
17	78	2009/12/23	EE	add damping resister R7804	add R7804	A00
18	79	2010/01/05	ME	By ME requirement	change SPR5 from 34.4F822.002 to 34.42T14.002	A00

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Title: **Change List(3/3)**

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