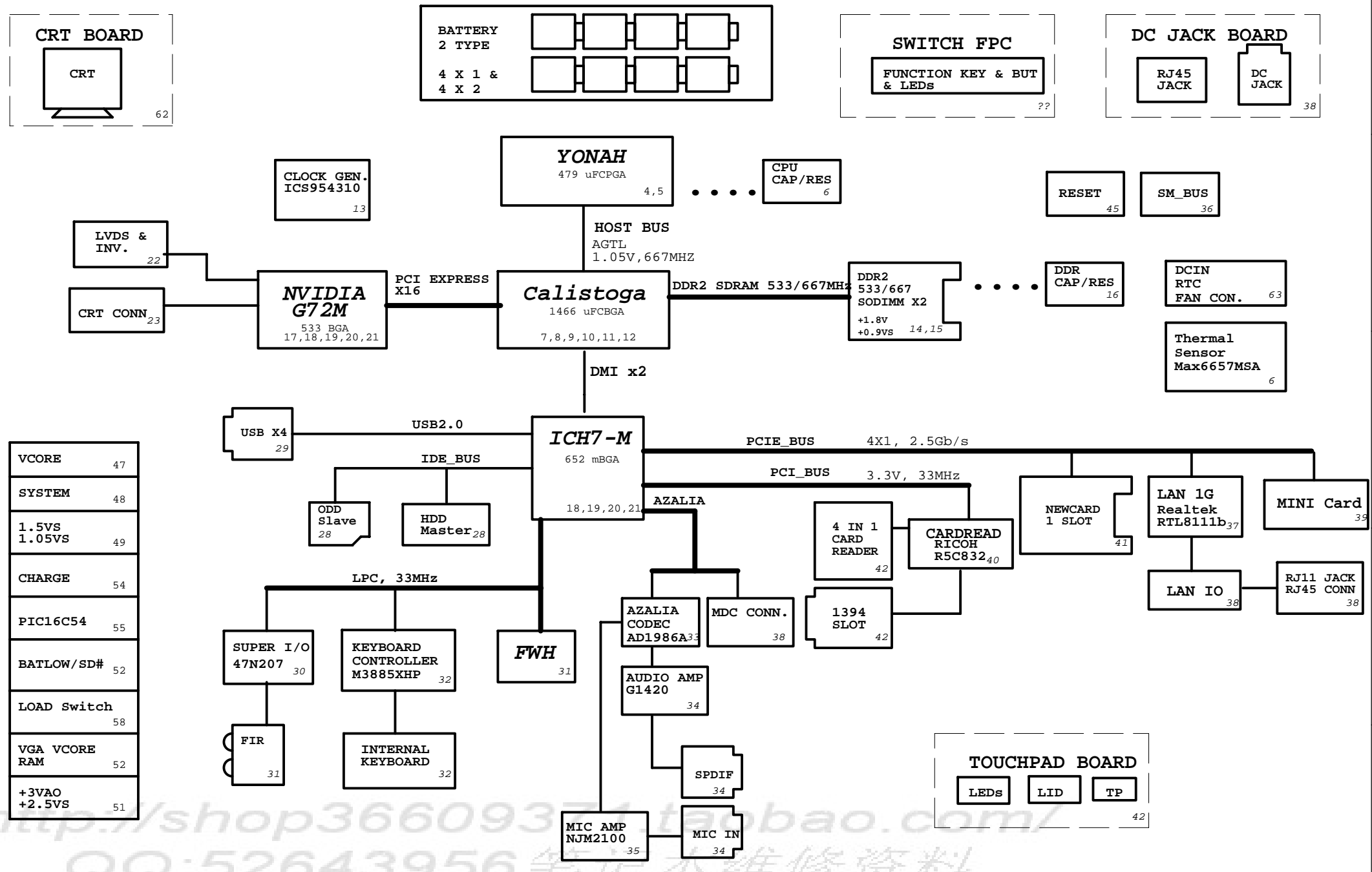


V6J SCHEMATIC V2.0

PAGE	Content	PAGE	Content
	SYSTEM PAGE REF.		POWER PAGE REF.
4	YONAH CPU-1	45	POWER ON SEQUENCE
5	YONAH CPU-2	46	DISCHARGE & HOLES & EMI
6	CPU CAP & THERMAL SENSOR	47	POWER_VCORE
7	Calistoga: CPU	48	POWER_SYSTEM
8	Calistoga: DDR2 & DMI & PCIE	49	POWER_I/O_1.5VS & 1.05VS
9	Calistoga: DDR2	50	POWER_I/O_DDR & VTT
10	Calistoga: POWER & Caps	51	POWER_I/O_+3VAO & +2.5VS
11	Calistoga: GND & NCTF	52	POWER_VGA_CORE & RAM
12	Calistoga: Straps	53	POWER_+1.2VSP
13	CLOCK: ICS954310	54	POWER_CHARGER
14	DDR2 SODIMM (0) & Caps	55	POWER_PIC
15	DDR2 SODIMM (1) & Caps	56	POWER_SELECTOR
16	DDR2 TERMINATOR	57	POWER_PROTECT
17	G72M: PCIE	58	POWER_LOAD SWITCH
18	G72M: FB	59	POWER_FLOWCHART
19	G72M: VRAM	60	POWER_SIGNAL
20	G72M: RGB/LCD/ROM/GPIO		
21	G72M: MIOB/CRSTAL/TMDS		
22	LVDS & INVERTER CONNECTOR		
23	CRT & LID SW & TPM CONNECTOR		
24	ICH7: IDE & LPC & RTC & AC97		
25	ICH7: PCI & INT & USB & DMI		
26	ICH7: SMB & PWR & CLK & GPIO		
27	ICH7: PWR & Caps		
28	HDD & ODD CONNECTOR		
29	USB CONNECTOR		
30	SIO: LPC47N207		
31	FIR & FWH		
32	KBC: M38857		
33	AUDIO AD1986A		
34	AUDIO AMP GMT01420 & JACK		
35	MIC AMP		
36	SMBUS & POWER CONNECTION		
37	GIGA LAN: REALTEK 8111B		
38	LAN TRANSFORMER & JACK & MDC		
39	MINI Card		
40	RICOH: R5C832		
41	NEWCARD		
42	4 IN 1 MEMORY CARD & 1394		
43	FAN CONTROLLER & DC IN		
44	INSTANT KEY & TP BRD & SW FPC		

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V6J: YONAH/Calistoga/G72M BLOCK DIAGRAM



VCORE	47
SYSTEM	48
1.5VS	49
1.05VS	49
CHARGE	54
PIC16C54	55
BATLOW/SD#	52
LOAD Switch	58
VGA VCORE	52
RAM	52
+3VAO	51
+2.5VS	51

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PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
Mini_PCI	AD18	3	B,D	
LAN --88E8001	AD16	0	B	
CardBus	AD17	1	B	
1394	AD17	1	A	
4 IN 1		1	C	

AZALIA : PCI_INTB#
 USB 0,1 : PCI_INTA#
 USB 2,3 : PCI_INTD#
 USB 4,5 : PCI_INTC#

CLK = 1101001x (D2)
 SMBUS ADDRESS : DDR_SODIMM0 = 1010010x (A4)
 DDR_SODIMM1 = 1010000x (A0)
 THERMAL = 1001100x (98)
 TPM = TBD

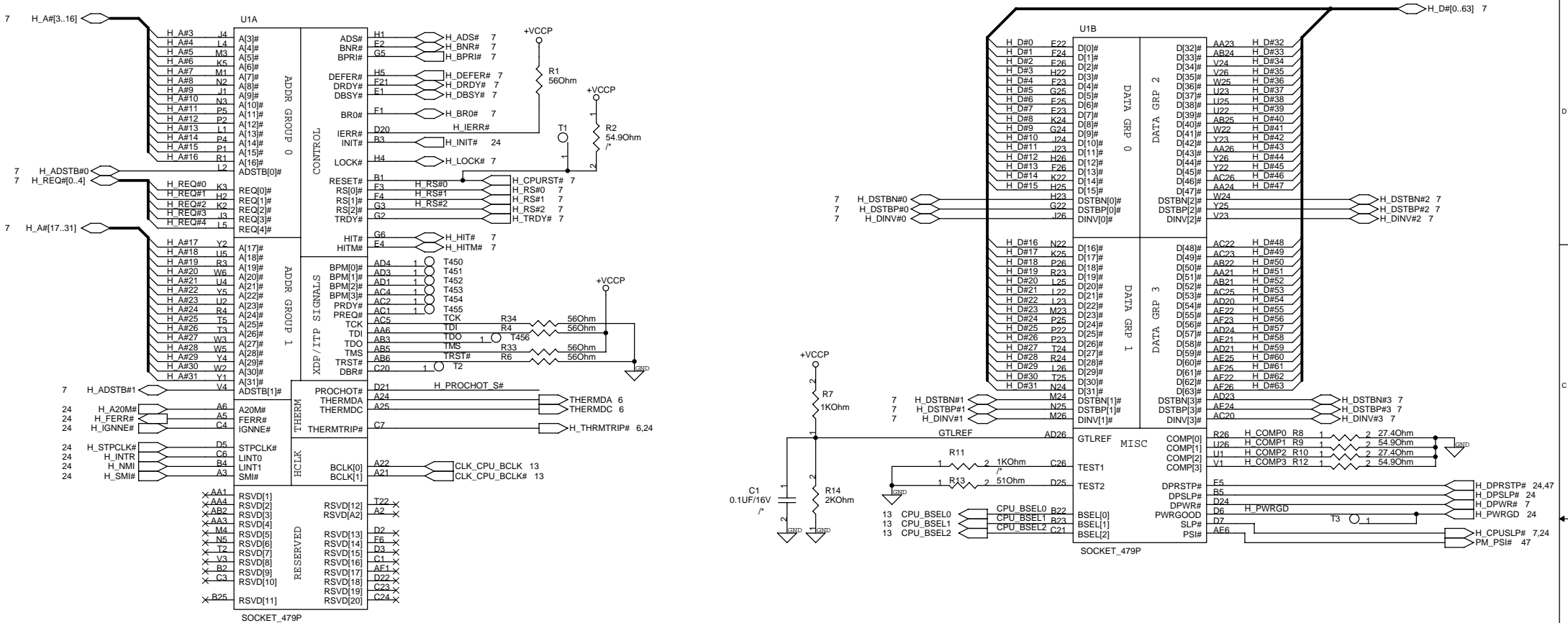
ICH7M_GPIO	Use As	Signal Name	Power
GPIO00	GPI	PM_BMBUSY#	+3VS
GPIO01	GPI	PCI_REQ#5	+3VS
GPIO02	GPI	G72M_THRM#(reserve)	+3VS
GPIO[3:5]	GPI	PCI_INT[E:H]	+3VS
GPIO06	GPO	BACK_OFF#	+3VS
GPIO07	GPI	WIRELESS_#	+3VS
GPIO08	GPI	EXTSMI#_3A	+3VSUS
GPIO09	GPI	ACIN_OC_ICH(reserve)	+3VSUS
GPIO10	GPI	CHG_FULLL_OC	+3VSUS
GPIO11	NATIVE	SMBALERT#	+3VSUS
GPIO12	GPI	KBCSCI_3	+3VSUS
GPIO13	GPI	BATIN_OC#_ICH(reserve)	+3VSUS
GPIO14	GPO	LID_ICH#_3A(reserve)	+3VSUS
GPIO15	GPI	802_LED#	+3VSUS
GPIO16	GPO	PM_DPRS_LPVR	+3VSUS
GPIO17	GPO	PCI_GNT#5	+3VSUS
GPIO18	GPO	STP_PCI#	+3VSUS
GPIO19	GPI	SATA_DET_#1	+3VSUS
GPIO20	GPO	STP_CPU#	+3VS
GPIO21	GPI	BATSEL_2P(reserve)	+3VS
GPIO22	NATIVE	PCI_REQ#4	+3VS
GPIO23	NATIVE	LDRQ1#	+3VS
GPIO24	GPO		+3VSUS
GPIO25	GPO		+3VSUS
GPIO26	GPO	OP_SD#	+3VSUS
GPIO27	GPO	WLAN_ON	+3VSUS
GPIO28	GPO	PWR_1HZ	+3VSUS
GPIO29	NATIVE	USB_OC#45	+3VSUS
GPIO30	NATIVE	USB_OC#67	+3VSUS
GPIO31	NATIVE	USB_OC#67	+3VSUS
GPIO32	GPO	PM_CLKRUN#	+3VSUS
GPIO33	GPO	BT_ON	+3VS
GPIO34	GPO	FWH_WP#	+3VS
GPIO35	GPO		+3VS
GPIO36	GPO	BT_LED#	+3VS
GPIO37	GPI	PCB_VID0	+3VS
GPIO38	GPI	PCB_VID1	+3VS
GPIO39	GPI	PCB_VID2	+3VS
GPIO[40:47]	N/A	N/A	N/A
GPIO48	NATIVE	FWH_TBL#	+3VS
GPIO49	NATIVE	H_PWRGD	+3VS

M38857_GPIO	Use As	Signal Name
P20	GPO	KBCRSM
P21	GPI	
P22	GPO	BAT_LEARN
P23	GPO	CPPE_EN
P24	GPO	SET_PCIRSTNS#
P25	GPO	CAP_LED#
P26	GPO	NUM_LED#
P27	GPO	SCROLL_LED#
P40	GPO	KBC_EXTSMI
P41	GPO	PANLOCK_LED#
P42	GPO	WATCHDOG
P43	GPO	CHG_FULLL_KBC(reserve)
P44	GPO	KBDCPURST_3Q
P45	GPO	KBC_GA20
P46	GPO	KBSCI_3Q
P47	GPI	PM_CLKRUN#
P50	GPI	BAT_LOW#_KBC
P51	GPO	
P52	GPI	KBDDT0
P53	GPI	KBDDT1
P54	GPI	LID_ICH#_3A
P55	GPI	BAT_IN#_OC
P56	GPO	FAN_DA
P57	GPO	ADJ_BL
P60	GPI	BLUETOOTH_#
P61	GPI	INTERNET#
P62	GPI	CPPE#
P63	GPI	
P64	GPI	ACIN_OC
P65	GPI	MARATHON_#
P66	GPI	PANLOCK_#
P67	GPI	
P76	GPI/O	SMD_BAT
P77	GPI/O	SMC_BAT

G72M_GPIO	Use As	Signal Name
GPIO00	GPI	
GPIO01	GPI	
GPIO02	GPO	
GPIO03	GPO	LCD_VDD_EN#
GPIO04	GPO	LCD_BACKEN
GPIO05	GPO	
GPIO06	GPO	
GPIO07	GPO	
GPIO08	GPI	GPIO8/ALERT#
GPIO09	GPO	
GPIO10	GPIO	G72M_GPIO12
GPIO11	GPO	
GPIO12	GPO	

47N207_GPIO	Use As	Signal Name
GP10	GPIO	
GP11	GPIO	
GP12	GPO	
GP13	GPO	
GP14	GPO	FIR_SEL
GP15	GPIO	PWR_THRO#
GP16	GPIO	ODD_DIS#
GP17	GPIO	RST#_XCARD
GP30	GPIO	PID0
GP31	GPIO	
GP32	GPIO	G72M_THRO#
GP33	GPIO	CPUFAN_SPD_A
GP34	GPIO	SW_RST#
GP35	GPIO	
GP36	GPIO	
GP37	GPIO	

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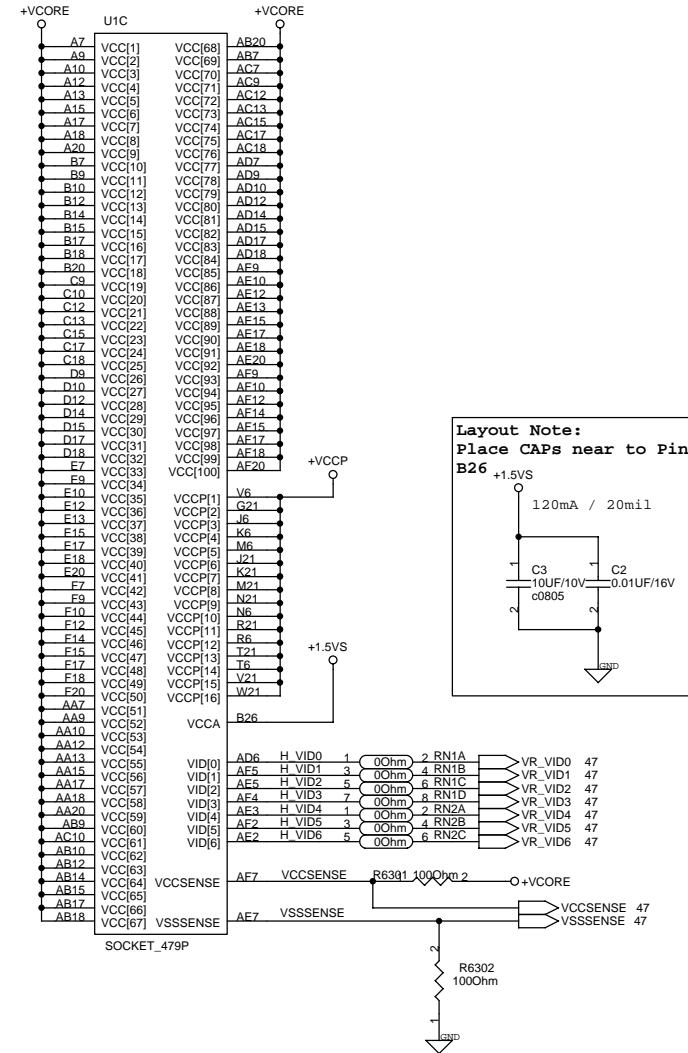
Layout Note : GTLREF
Trace Length<500 mil (55 Ohm)
T/B trace 5.5 , Space 25

BCLK	FSB	BSEL0	BSEL1	BSEL2
133	533	H	L	L
166	667	H	H	L

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YONAH FSB667			
	LFM	TYP	HFM
CPU State	C4	C3	C0
VCC	1.14V	1.2V	1.356V
ICC	0.9A	7.59A	27A

YONAH FSB667			
	MIN	TYP	MAX
VCCP	0.997V	1.05V	1.102V
ICCP			2.5A

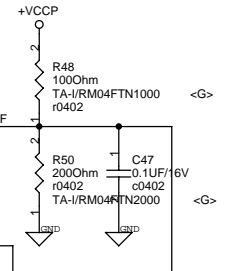
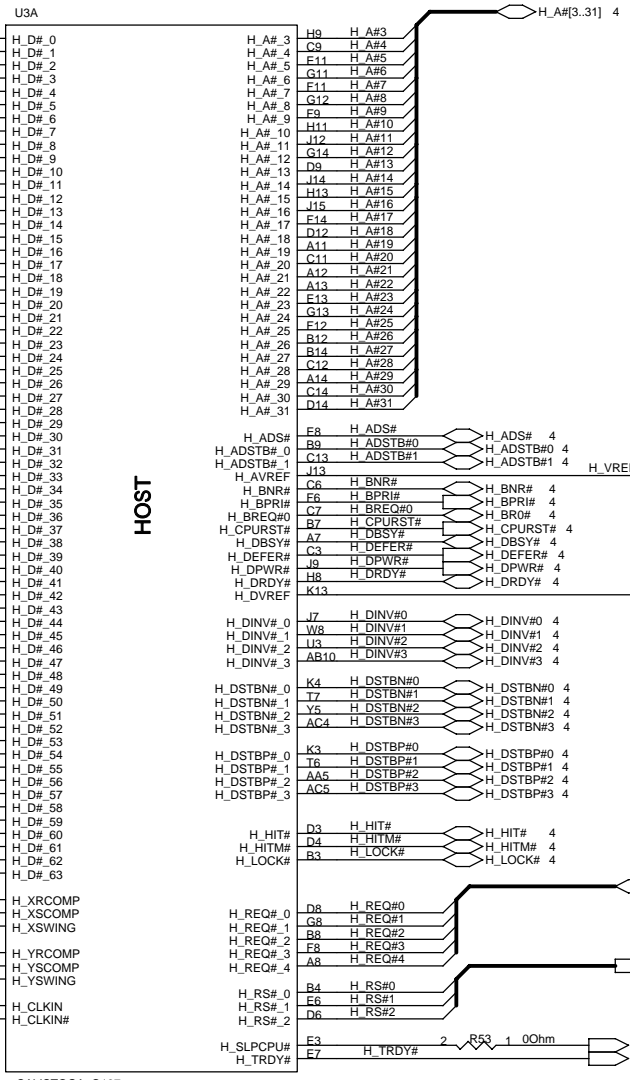
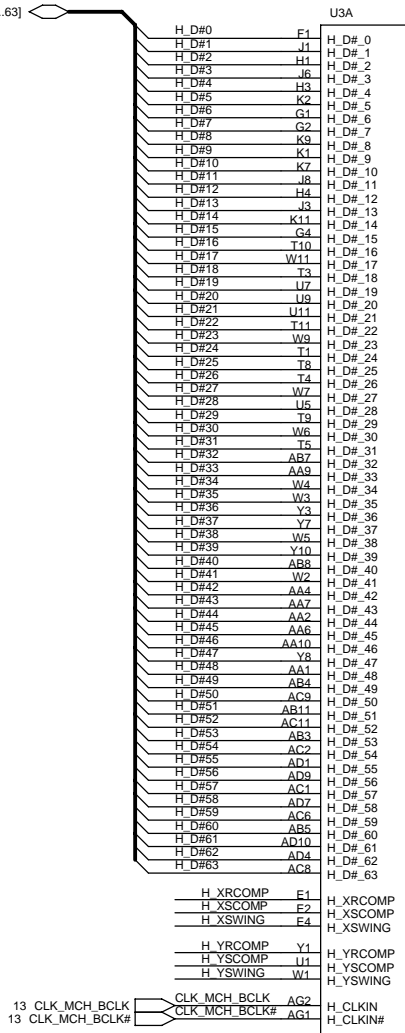
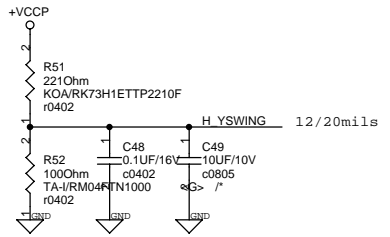
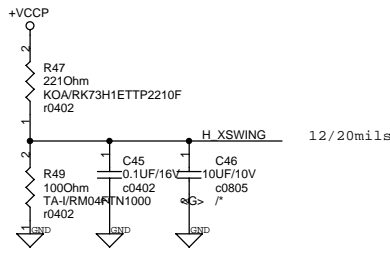
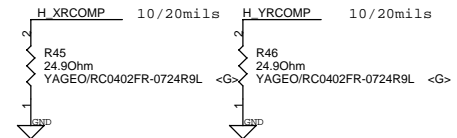
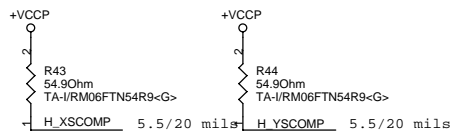


UID	
A4	VSS[1]
A8	VSS[2]
A11	VSS[3]
A14	VSS[4]
A16	VSS[5]
A19	VSS[6]
A23	VSS[7]
A26	VSS[8]
B6	VSS[9]
B8	VSS[10]
B11	VSS[11]
B13	VSS[12]
B16	VSS[13]
B21	VSS[14]
B24	VSS[15]
B27	VSS[16]
C5	VSS[17]
C8	VSS[18]
C11	VSS[19]
C14	VSS[20]
C16	VSS[21]
C19	VSS[22]
C2	VSS[23]
C22	VSS[24]
C25	VSS[25]
D1	VSS[26]
D4	VSS[27]
D8	VSS[28]
D11	VSS[29]
D13	VSS[30]
D16	VSS[31]
A19	VSS[32]
D23	VSS[33]
D26	VSS[34]
E3	VSS[35]
E6	VSS[36]
E8	VSS[37]
E11	VSS[38]
E14	VSS[39]
E16	VSS[40]
E19	VSS[41]
E21	VSS[42]
E24	VSS[43]
E5	VSS[44]
E8	VSS[45]
F11	VSS[46]
F13	VSS[47]
F16	VSS[48]
F19	VSS[49]
F22	VSS[50]
F25	VSS[51]
F28	VSS[52]
G4	VSS[53]
G1	VSS[54]
G23	VSS[55]
G26	VSS[56]
H3	VSS[57]
H6	VSS[58]
H21	VSS[59]
H24	VSS[60]
J2	VSS[61]
J5	VSS[62]
J22	VSS[63]
J25	VSS[64]
K1	VSS[65]
K4	VSS[66]
K23	VSS[67]
K26	VSS[68]
L3	VSS[69]
L6	VSS[70]
L21	VSS[71]
M2	VSS[72]
M4	VSS[73]
M5	VSS[74]
M22	VSS[75]
M25	VSS[76]
N1	VSS[77]
N4	VSS[78]
N23	VSS[79]
N26	VSS[80]
P3	VSS[81]
P6	VSS[82]
P21	VSS[83]
P24	VSS[84]
R2	VSS[85]
R5	VSS[86]
R22	VSS[87]
R25	VSS[88]
T1	VSS[89]
T4	VSS[90]
T23	VSS[91]
T26	VSS[92]
U3	VSS[93]
U6	VSS[94]
U21	VSS[95]
U24	VSS[96]
V2	VSS[97]
V5	VSS[98]
V22	VSS[99]
V25	VSS[100]
W4	VSS[101]
W23	VSS[102]
W26	VSS[103]
Y3	VSS[104]
Y6	VSS[105]
Y21	VSS[106]
Y24	VSS[107]
Y27	VSS[108]
Y28	VSS[109]
Y110	VSS[110]
Y111	VSS[111]
Y112	VSS[112]
Y113	VSS[113]
Y114	VSS[114]
Y115	VSS[115]
Y116	VSS[116]
Y117	VSS[117]
Y118	VSS[118]
Y119	VSS[119]
Y120	VSS[120]
Y121	VSS[121]
Y122	VSS[122]
Y123	VSS[123]
Y124	VSS[124]
Y125	VSS[125]
Y126	VSS[126]
Y127	VSS[127]
Y128	VSS[128]
Y129	VSS[129]
Y130	VSS[130]
Y131	VSS[131]
Y132	VSS[132]
Y133	VSS[133]
Y134	VSS[134]
Y135	VSS[135]
Y136	VSS[136]
Y137	VSS[137]
Y138	VSS[138]
Y139	VSS[139]
Y140	VSS[140]
Y141	VSS[141]
Y142	VSS[142]
Y143	VSS[143]
Y144	VSS[144]
Y145	VSS[145]
Y146	VSS[146]
Y147	VSS[147]
Y148	VSS[148]
Y149	VSS[149]
Y150	VSS[150]
Y151	VSS[151]
Y152	VSS[152]
Y153	VSS[153]
Y154	VSS[154]
Y155	VSS[155]
Y156	VSS[156]
Y157	VSS[157]
Y158	VSS[158]
Y159	VSS[159]
Y160	VSS[160]
Y161	VSS[161]
Y162	VSS[162]

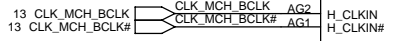
MOBILE YONAH VID TABLE

VID[6..0]	Voltage	VID[6..0]	Voltage	VID[6..0]	Voltage	VID[6..0]	Voltage
0000000	1.5000V	0100000	1.1000V	1000000	0.7000V	1100000	0.3000V
0000001	1.4875V	0100001	1.0875V	1000001	0.6875V	1100001	0.2875V
0000010	1.4750V	0100010	1.0750V	1000010	0.6750V	1100010	0.2750V
0000011	1.4625V	0100011	1.0625V	1000011	0.6625V	1100011	0.2650V
0000100	1.4500V	0100100	1.0500V	1000100	0.6500V	1100100	0.2500V
0000101	1.4375V	0100101	1.0375V	1000101	0.6375V	1100101	0.2375V
0000110	1.4250V	0100110	1.0250V	1000110	0.6250V	1100110	0.2250V
0000111	1.4125V	0100111	1.0125V	1000111	0.6125V	1100111	0.2125V
0001000	1.4000V	0101000	1.0000V	1001000	0.6000V	1101000	0.2000V
0001001	1.3875V	0101001	0.9875V	1001001	0.5875V	1101001	0.1875V
0001010	1.3750V	0101010	0.9750V	1001010	0.5750V	1101010	0.1750V
0001011	1.3625V	0101011	0.9625V	1001011	0.5625V	1101011	0.1625V
0001100	1.3500V	0101100	0.9500V	1001100	0.5500V	1101100	0.1500V
0001101	1.3375V	0101101	0.9375V	1001101	0.5375V	1101101	0.1375V
0001110	1.3250V	0101110	0.9250V	1001110	0.5250V	1101110	0.1250V
0001111	1.3125V	0101111	0.9125V	1001111	0.5125V	1101111	0.1125V
0010000	1.3000V	0110000	0.9000V	1010000	0.5000V	1110000	0.1000V
0010001	1.2875V	0110001	0.8875V	1010001	0.4875V	1110001	0.0875V
0010010	1.2750V	0110010	0.8750V	1010010	0.4750V	1110010	0.0750V
0010011	1.2625V	0110011	0.8625V	1010011	0.4625V	1110011	0.0625V
0010100	1.2500V	0110100	0.8500V	1010100	0.4500V	1110100	0.0500V
0010101	1.2375V	0110101	0.8375V	1010101	0.4375V	1110101	0.0375V
0010110	1.2250V	0110110	0.8250V	1010110	0.4250V	1110110	0.0250V
0010111	1.2125V	0110111	0.8125V	1010111	0.4125V	1110111	0.0125V
0011000	1.2000V	0111000	0.8000V	1011000	0.4000V	1111000	0.0000V
0011001	1.1875V	0111001	0.7875V	1011001	0.3875V	1111001	0.0000V
0011010	1.1750V	0111010	0.7750V	1011010	0.3750V	1111010	0.0000V
0011011	1.1625V	0111011	0.7625V	1011011	0.3625V	1111011	0.0000V
0011100	1.1500V	0111100	0.7500V	1011100	0.3500V	1111100	0.0000V
0011101	1.1375V	0111101	0.7375V	1011101	0.3375V	1111101	0.0000V
0011110	1.1250V	0111110	0.7250V	1011110	0.3250V	1111110	0.0000V
0011111	1.1125V	0111111	0.7125V	1011111	0.3125V	1111111	0.0000V

YONAH VID TABLE							
CPU FRQ.	HFM VOLTAGE	1.6G	1.4G	1.2G	1G	LFM 0.8G	C3/C4
2.13G/B1	1.372V					0.988V	0.726V
2.0G/B1	1.356V					0.988V	0.726V
1.87G/B1	1.356V					0.988V	0.726V
1.73G/B1	1.356V					0.988V	0.726V
1.6G/B1	1.356V					0.988V	0.726V
1.6G/A2	1.308V	1.292V	1.260V	1.228V	1.196V	0.844V	0.748V

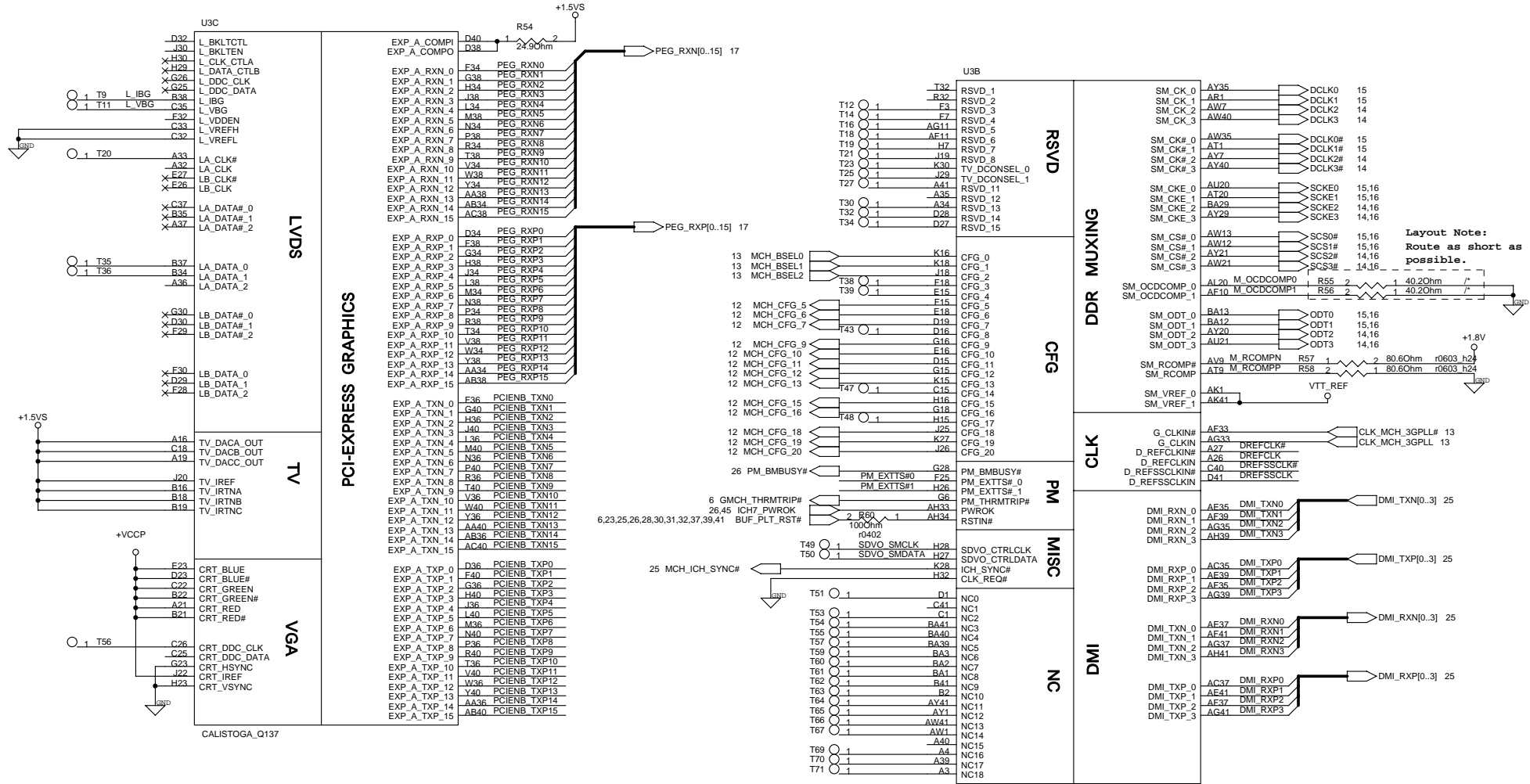


Layout Note : H_VREF
Trace Length<500 mil (55 Ohm)



CALISTOGA_Q137

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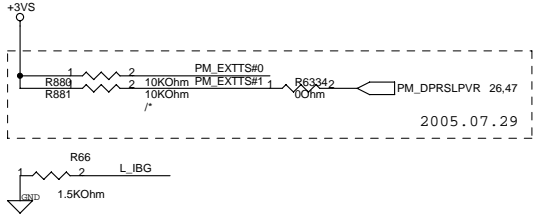


Layout Note:
Route as short as possible.

+1.8V

PCIEBN_TXN0	1	2	PEG_G_RXN0	PCIEBN_TXP0	1	2	PEG_G_RXP0
PCIEBN_TXN1	1	2	0.1uF/16V	PCIEBN_TXP1	1	2	0.1uF/16V
PCIEBN_TXN1	1	2	PEG_G_RXN1	PCIEBN_TXP1	1	2	PEG_G_RXP1
PCIEBN_TXN2	1	2	0.1uF/16V	PCIEBN_TXP2	1	2	0.1uF/16V
PCIEBN_TXN2	1	2	PEG_G_RXN2	PCIEBN_TXP2	1	2	PEG_G_RXP2
PCIEBN_TXN3	1	2	0.1uF/16V	PCIEBN_TXP3	1	2	0.1uF/16V
PCIEBN_TXN3	1	2	PEG_G_RXN3	PCIEBN_TXP3	1	2	PEG_G_RXP3
PCIEBN_TXN4	1	2	0.1uF/16V	PCIEBN_TXP4	1	2	0.1uF/16V
PCIEBN_TXN4	1	2	PEG_G_RXN4	PCIEBN_TXP4	1	2	PEG_G_RXP4
PCIEBN_TXN5	1	2	0.1uF/16V	PCIEBN_TXP5	1	2	0.1uF/16V
PCIEBN_TXN5	1	2	PEG_G_RXN5	PCIEBN_TXP5	1	2	PEG_G_RXP5
PCIEBN_TXN6	1	2	0.1uF/16V	PCIEBN_TXP6	1	2	0.1uF/16V
PCIEBN_TXN6	1	2	PEG_G_RXN6	PCIEBN_TXP6	1	2	PEG_G_RXP6
PCIEBN_TXN7	1	2	0.1uF/16V	PCIEBN_TXP7	1	2	0.1uF/16V
PCIEBN_TXN7	1	2	PEG_G_RXN7	PCIEBN_TXP7	1	2	PEG_G_RXP7
PCIEBN_TXN8	1	2	0.1uF/16V	PCIEBN_TXP8	1	2	0.1uF/16V
PCIEBN_TXN8	1	2	PEG_G_RXN8	PCIEBN_TXP8	1	2	PEG_G_RXP8
PCIEBN_TXN9	1	2	0.1uF/16V	PCIEBN_TXP9	1	2	0.1uF/16V
PCIEBN_TXN9	1	2	PEG_G_RXN9	PCIEBN_TXP9	1	2	PEG_G_RXP9
PCIEBN_TXN10	1	2	0.1uF/16V	PCIEBN_TXP10	1	2	0.1uF/16V
PCIEBN_TXN10	1	2	PEG_G_RXN10	PCIEBN_TXP10	1	2	PEG_G_RXP10
PCIEBN_TXN11	1	2	0.1uF/16V	PCIEBN_TXP11	1	2	0.1uF/16V
PCIEBN_TXN11	1	2	PEG_G_RXN11	PCIEBN_TXP11	1	2	PEG_G_RXP11
PCIEBN_TXN12	1	2	0.1uF/16V	PCIEBN_TXP12	1	2	0.1uF/16V
PCIEBN_TXN12	1	2	PEG_G_RXN12	PCIEBN_TXP12	1	2	PEG_G_RXP12
PCIEBN_TXN13	1	2	0.1uF/16V	PCIEBN_TXP13	1	2	0.1uF/16V
PCIEBN_TXN13	1	2	PEG_G_RXN13	PCIEBN_TXP13	1	2	PEG_G_RXP13
PCIEBN_TXN14	1	2	0.1uF/16V	PCIEBN_TXP14	1	2	0.1uF/16V
PCIEBN_TXN14	1	2	PEG_G_RXN14	PCIEBN_TXP14	1	2	PEG_G_RXP14
PCIEBN_TXN15	1	2	0.1uF/16V	PCIEBN_TXP15	1	2	0.1uF/16V
PCIEBN_TXN15	1	2	PEG_G_RXN15	PCIEBN_TXP15	1	2	PEG_G_RXP15
PCIEBN_TXN15	1	2	0.1uF/16V	PCIEBN_TXP15	1	2	0.1uF/16V

No stuff for internal graphic



2005.07.29

15 M_A_DQ[0..63]

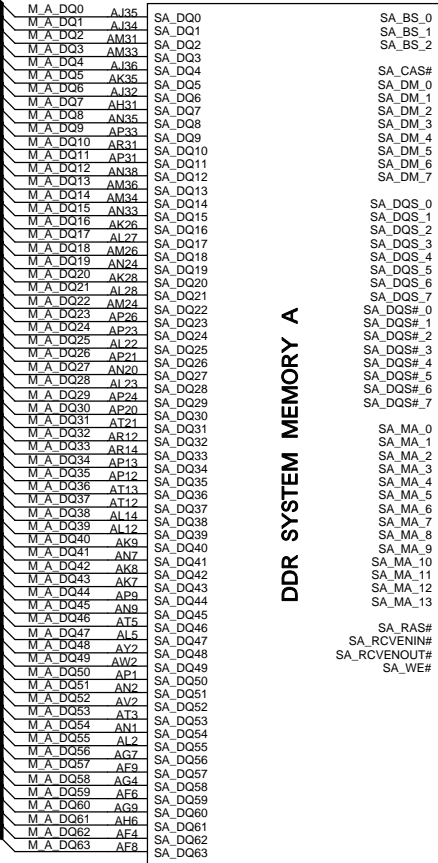
U3D

14 M_B_DQ[0..63]

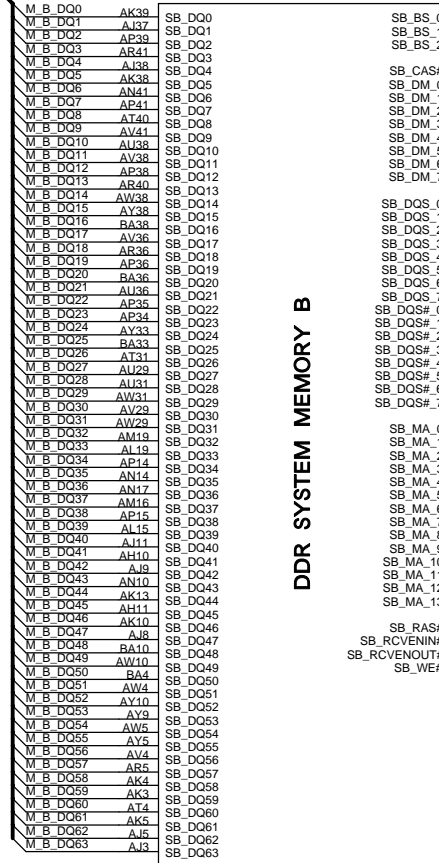
U3E

DDR SYSTEM MEMORY A

DDR SYSTEM MEMORY B



CALISTOGA_Q137



CALISTOGA_Q137

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PROJECT: V6J

REVISION: 2.0

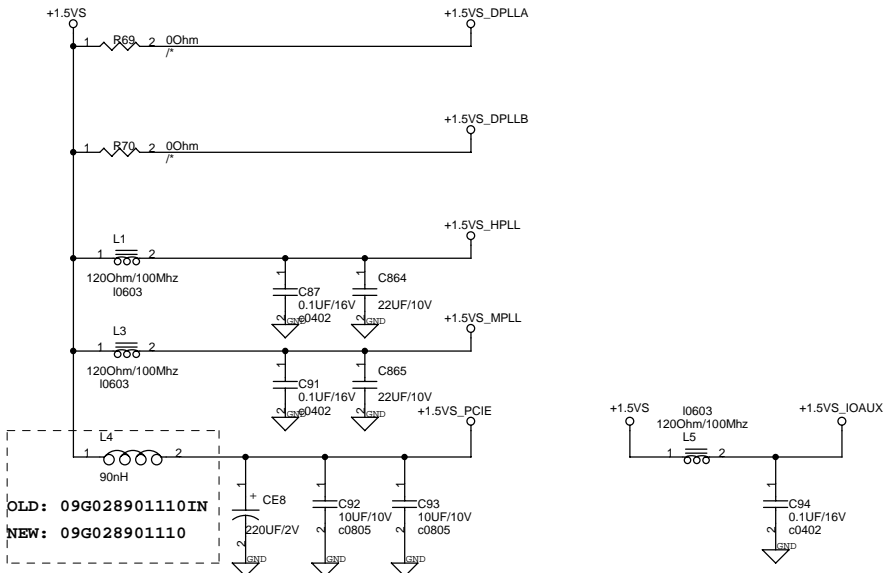
DATE: Friday, November 25, 2005
SHEET: 9 OF 63

DESCRIPTION: Calistoga DDR2 (3)

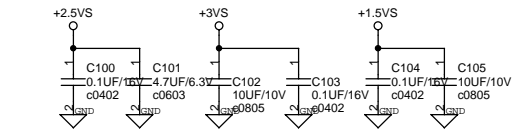
SCHEMATIC FILE NAME: <OrgName>
RELEASE DATE:

DESIGN ENGINEER: Feng Lin

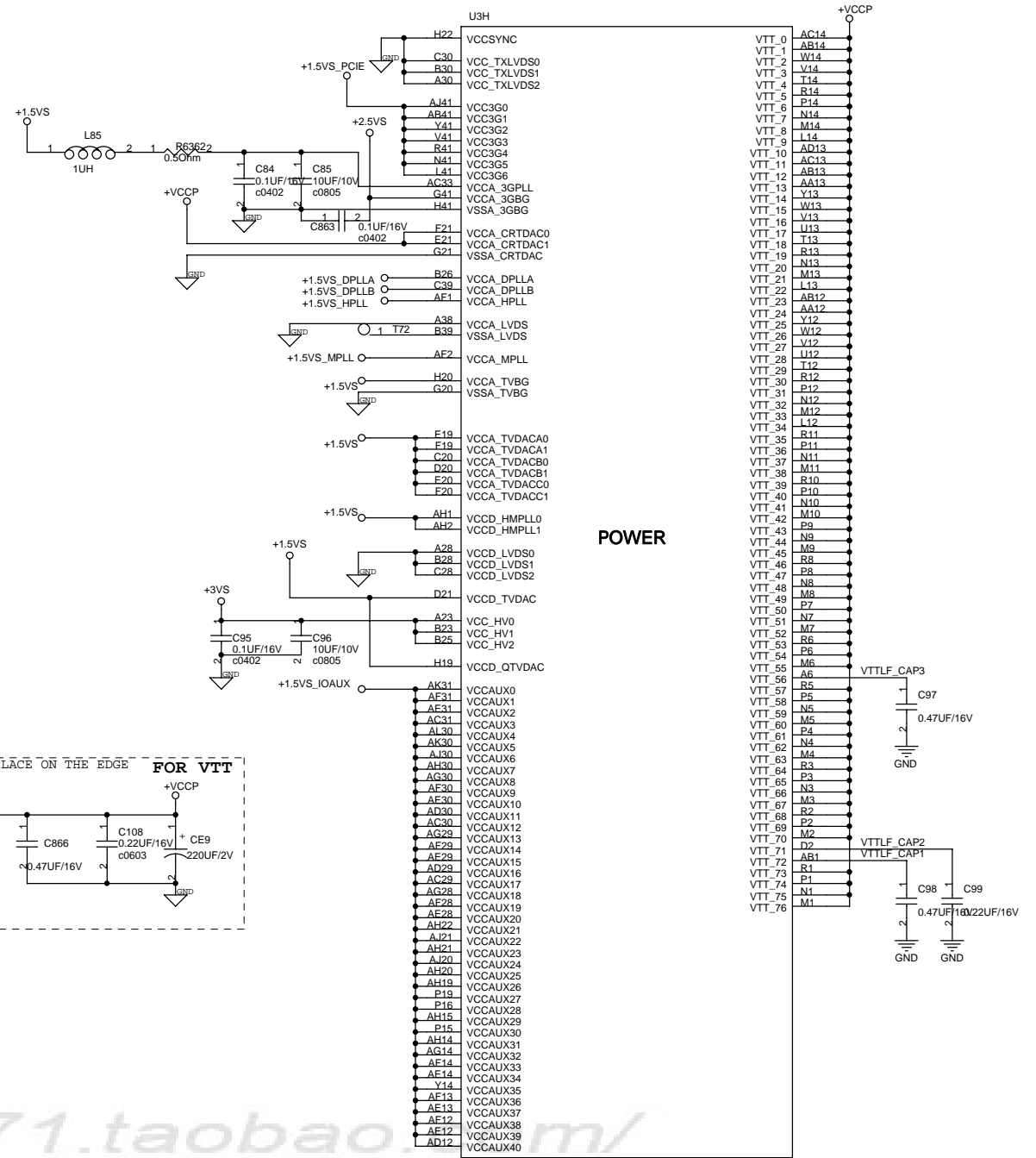
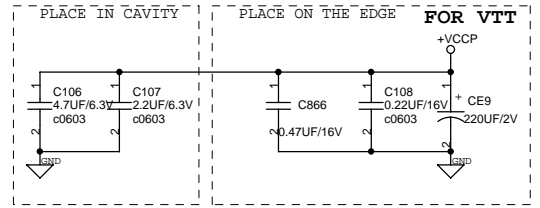
NOTE: 0.1uF caps in 1.5SxPLL need to be located as edge caps within 200 mils.



OLD: 09G028901110IN
NEW: 09G028901110



NOTE: 0.1uF CAPS USED IN +1.5VS, +3.3VS +2.5VS should be placed within 200 mils of edge.

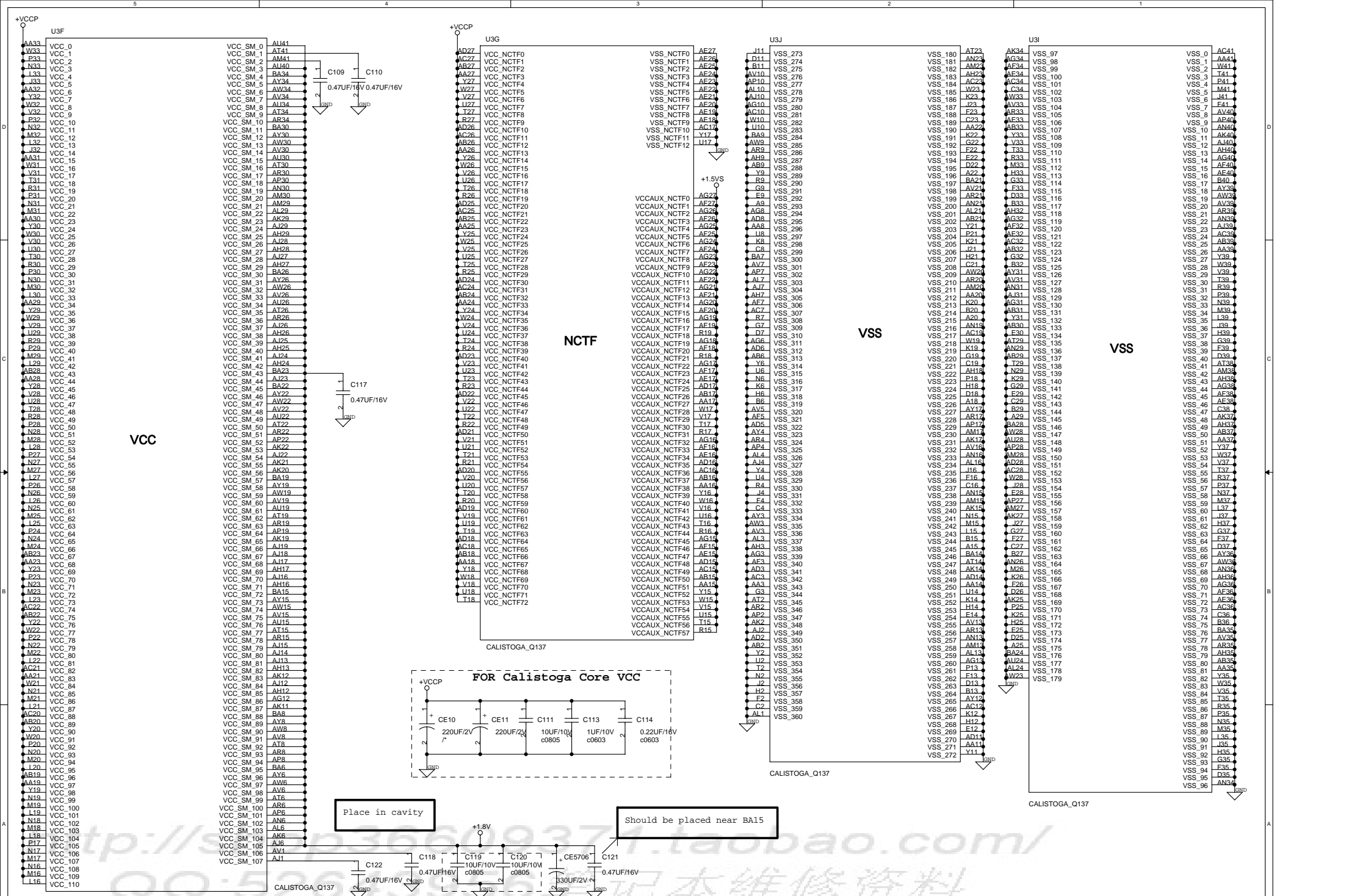


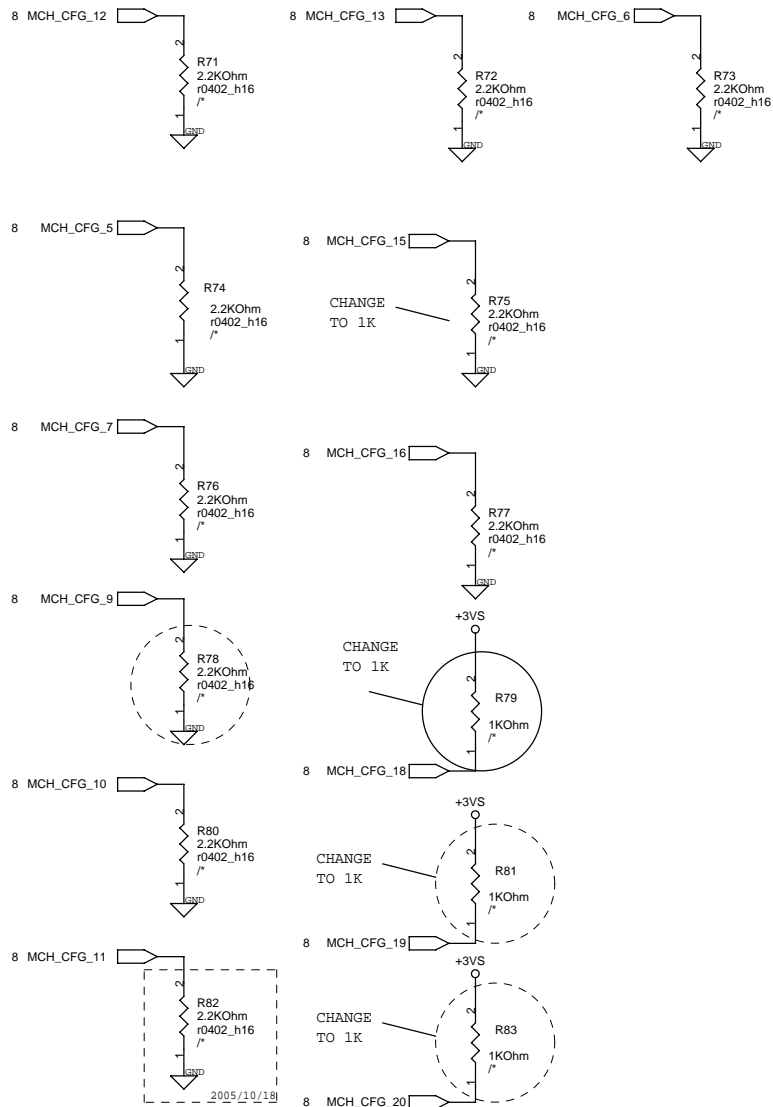
POWER

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CALISTOGA_Q137

	PROJECT: V6J	REVISION	DATE: Friday, November 25, 2005	DESCRIPTION:	SCHMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		2.0	SHEET 10 OF 63	MCH: Power	RELEASE DATE :		Feng Lin



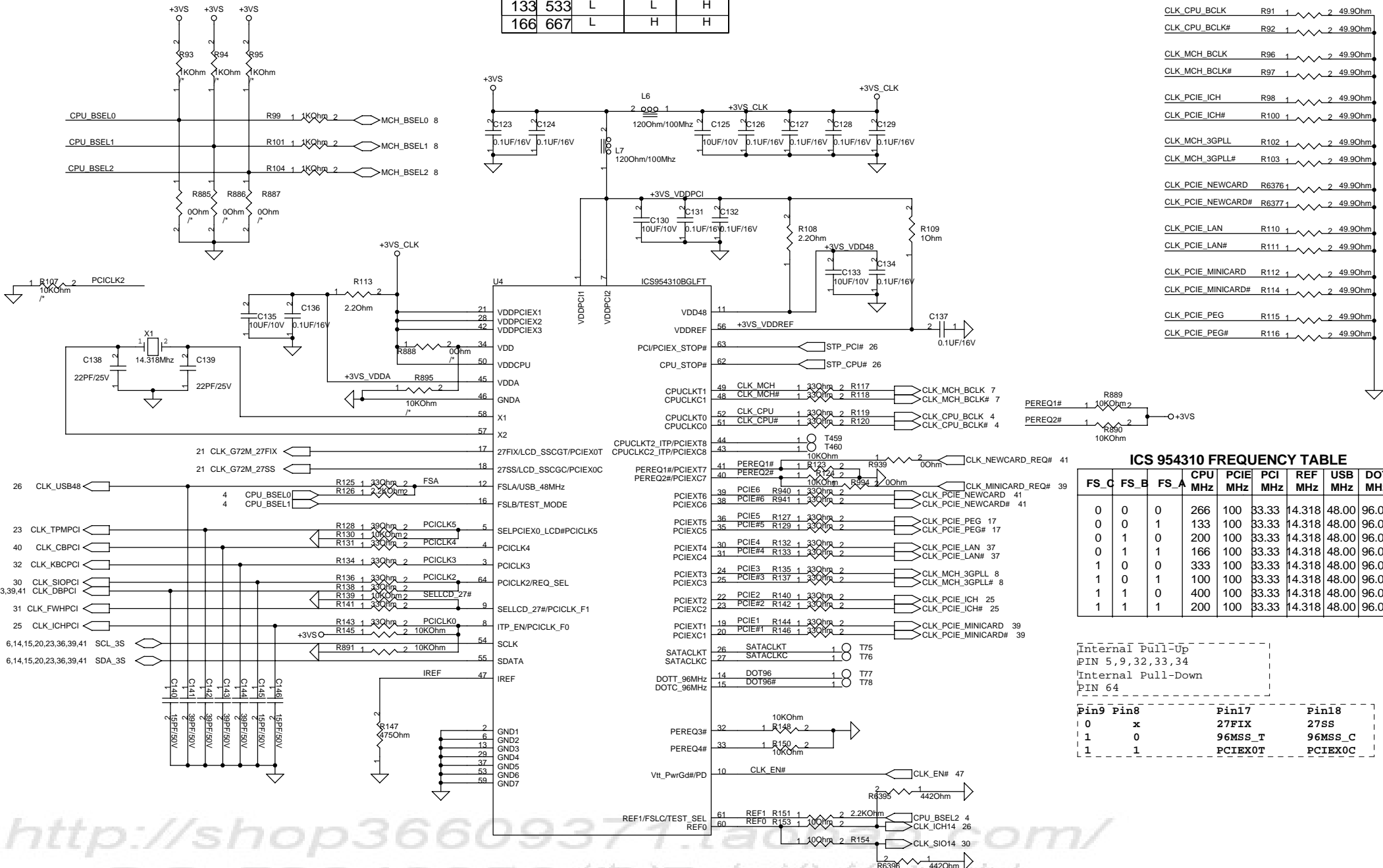


Signal Name	Configuration	Notes
CFG[2:0]	011= 667 FSB 001= 533 FSB	Selection the FSB frequency
CFG5	0= DMIX2 1= DMIX4	Selection between DMIX2 and DMIX4
CFG7	0= Reserved 1= Mobil Yonah	Control the target processor
CFG9	0= Lane Reversal EN 1= Normal Operation	
CFG[13:12]	01= XOR 10= Z 11= Normal Operation	
CFG16	0= Dynamic ODT DIS 1= Dynamic ODT EN	Control FSB Dynamic ODT
CFG18	0= 1.05V 1= 1.5V	Control GMCH Vcore level
CFG19	0= Normal Operation 1= DMI Lane Revesal EN	
SDVOCTRL_DATA	0= No SDVO device 1= SDVO device present	
Intel Demo Circuit		
CFG6	0= Moby Dick 1= Calistoga	
CFG9	0= Lane Reversal EN 1= Normal Operation	
CFG11	0= Reserved 1= 8x Enable	PSB 4x CLK Enable
CFG20	0= Only SDVO or PCIE x1 (Default) 1= SDVO and PCIE x1 are operating	
<p>CFG[2..0] need external pullup resistors. CFG[17..3] have internal pullup resistors. CFG[19..18] have internal pulldown resistors. SDVOCRTL_DATA has internal pulldown resistors.</p>		

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Bclk	FSB	FSLC	FSLB	FSLA
133	533	L	L	H
166	667	L	H	H

PLACE termination close to source IC



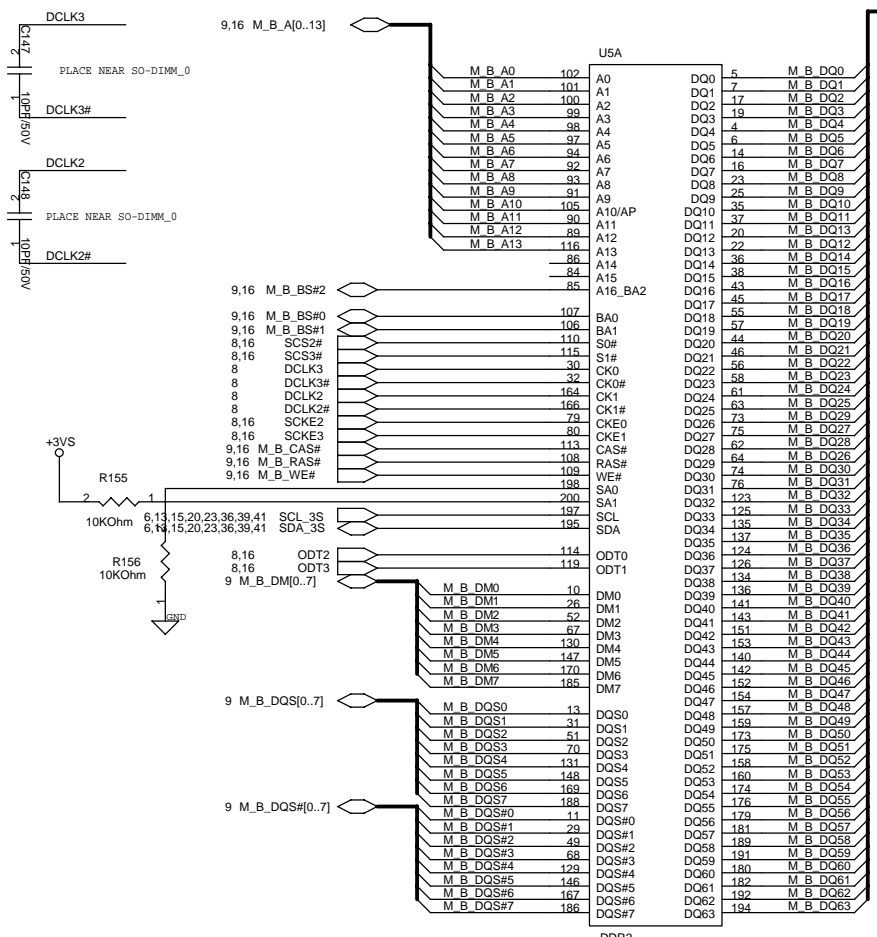
ICS 954310 FREQUENCY TABLE

FS_C	FS_B	FS_A	CPU MHz	PCI MHz	PCI MHz	REF MHz	USB MHz	DOT MHz
0	0	0	266	100	33.33	14.318	48.00	96.00
0	0	1	133	100	33.33	14.318	48.00	96.00
0	1	0	200	100	33.33	14.318	48.00	96.00
0	1	1	166	100	33.33	14.318	48.00	96.00
1	0	0	333	100	33.33	14.318	48.00	96.00
1	0	1	100	100	33.33	14.318	48.00	96.00
1	1	0	400	100	33.33	14.318	48.00	96.00
1	1	1	200	100	33.33	14.318	48.00	96.00

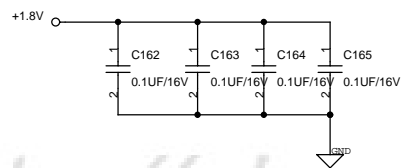
Internal Pull-Up
PIN 5, 9, 32, 33, 34
Internal Pull-Down
PIN 64

Pin9	Pin8	Pin17	Pin18
0	x	27FIX	27SS
1	0	96MSS_T	96MSS_C
1	1	PCIE_X0T	PCIE_X0C

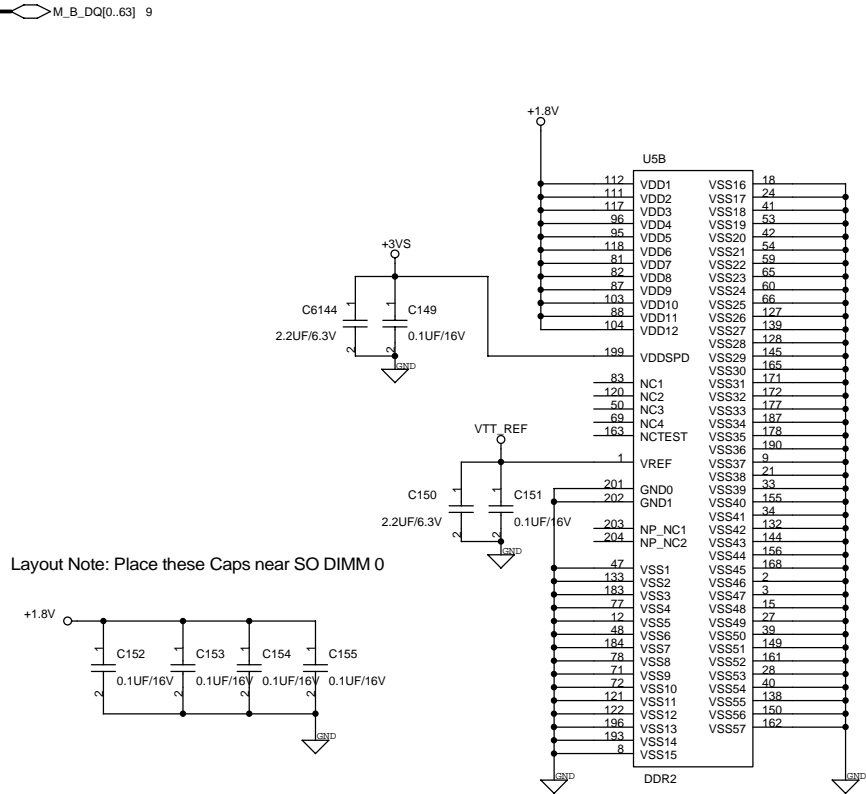
<http://shop36609371.taobao.com/>
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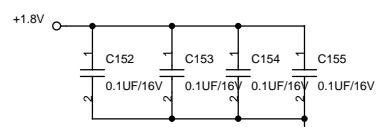
Layout Note: Place these High-Freq decoupling Caps near the GMCH



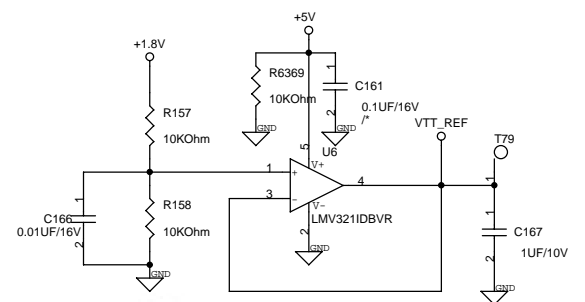
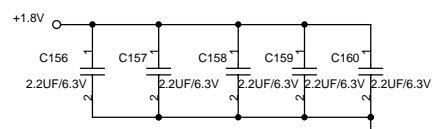
SO-DIMM Part is QUASAR
BOM is TYCO



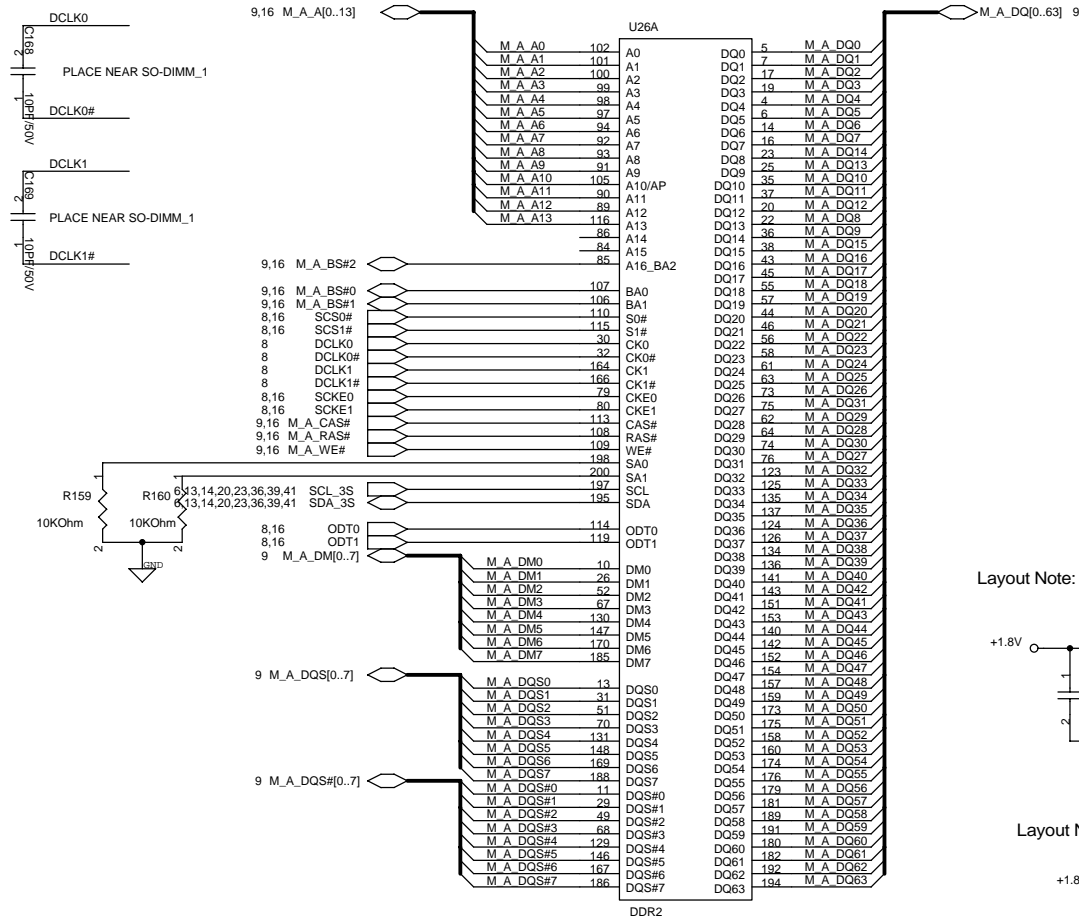
Layout Note: Place these Caps near SO DIMM 0



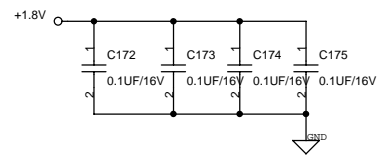
Layout Note: Place these Caps near SO DIMM 0



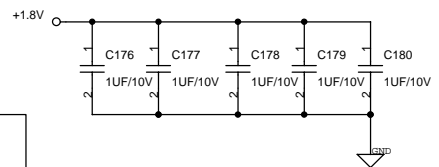
<http://shop36609371.taobao.com/>
QQ:52643956 笔记本维修资料



Layout Note: Place these Caps near SO DIMM 1



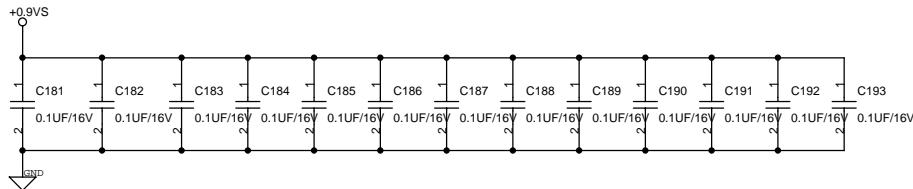
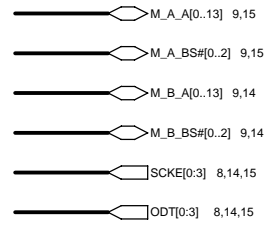
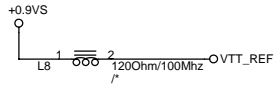
Layout Note: Place these Caps near SO DIMM 1



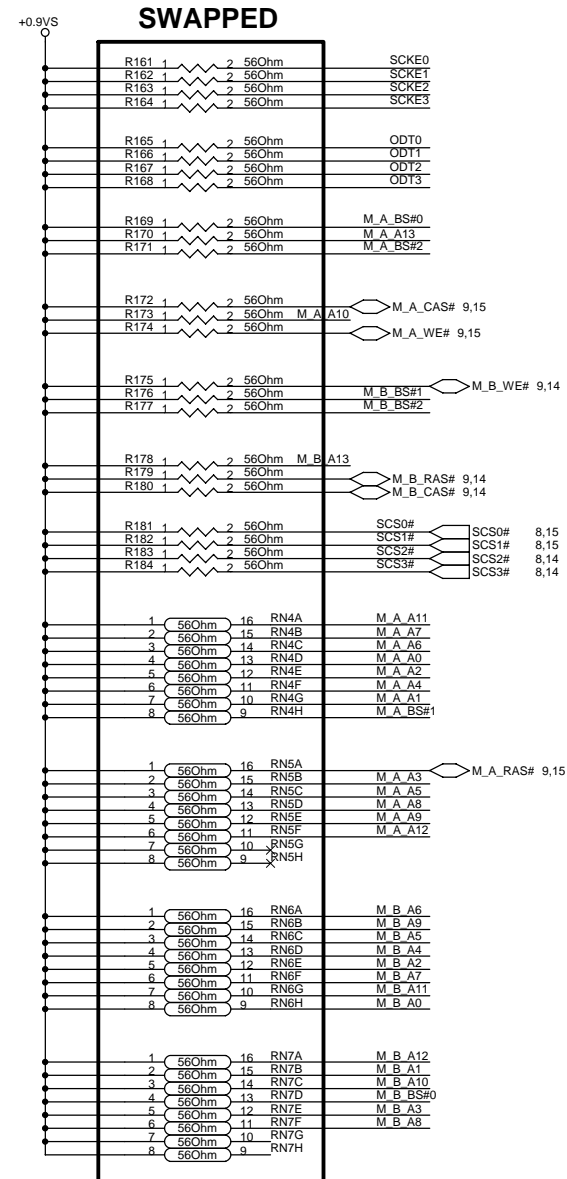
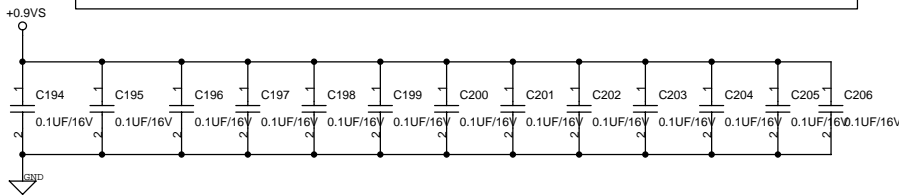
SO-DIMM Part is QUASAR
BOM is TYCO

SO-DIMM 1 is placed farther
from the GMCH than SO-DIMM 0

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Layout note: Place one cap close to every 2 pullup resistors terminated to +0.9VS



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PROJECT: V6J

REVISION
2.0

DATE: Friday, November 25, 2005
SHEET **16** OF **63**

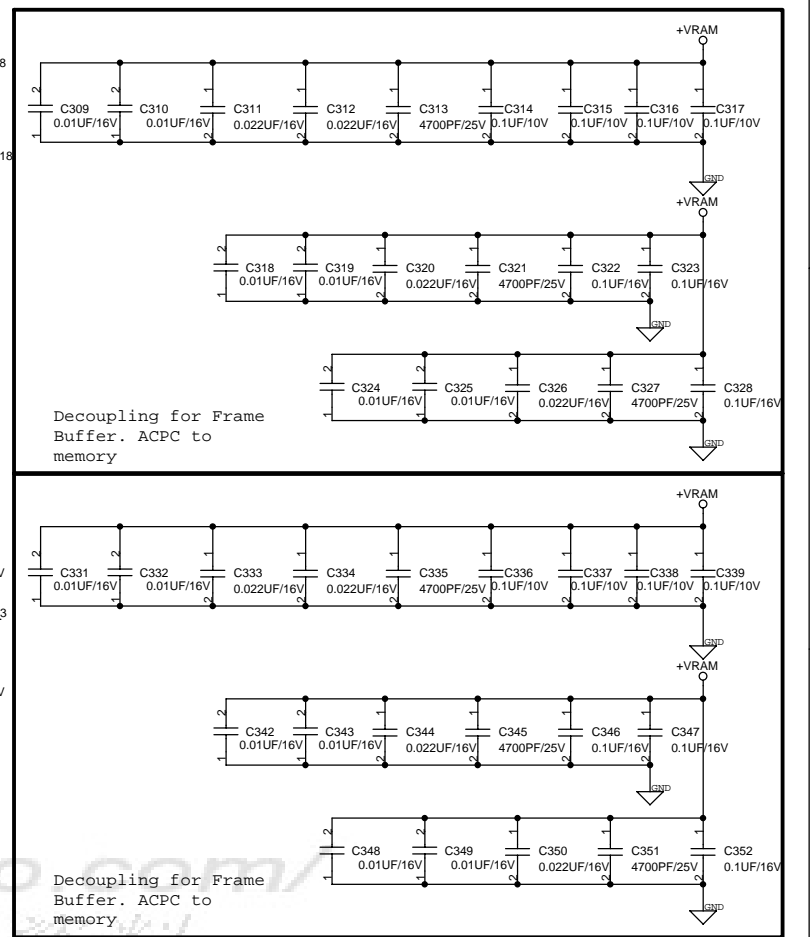
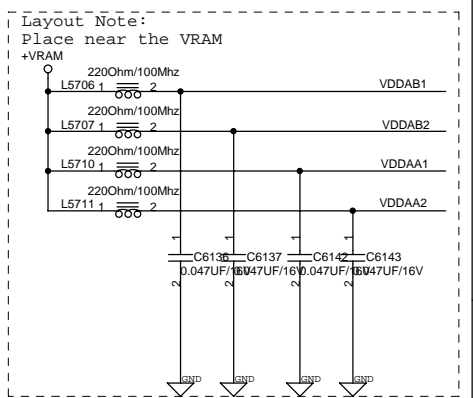
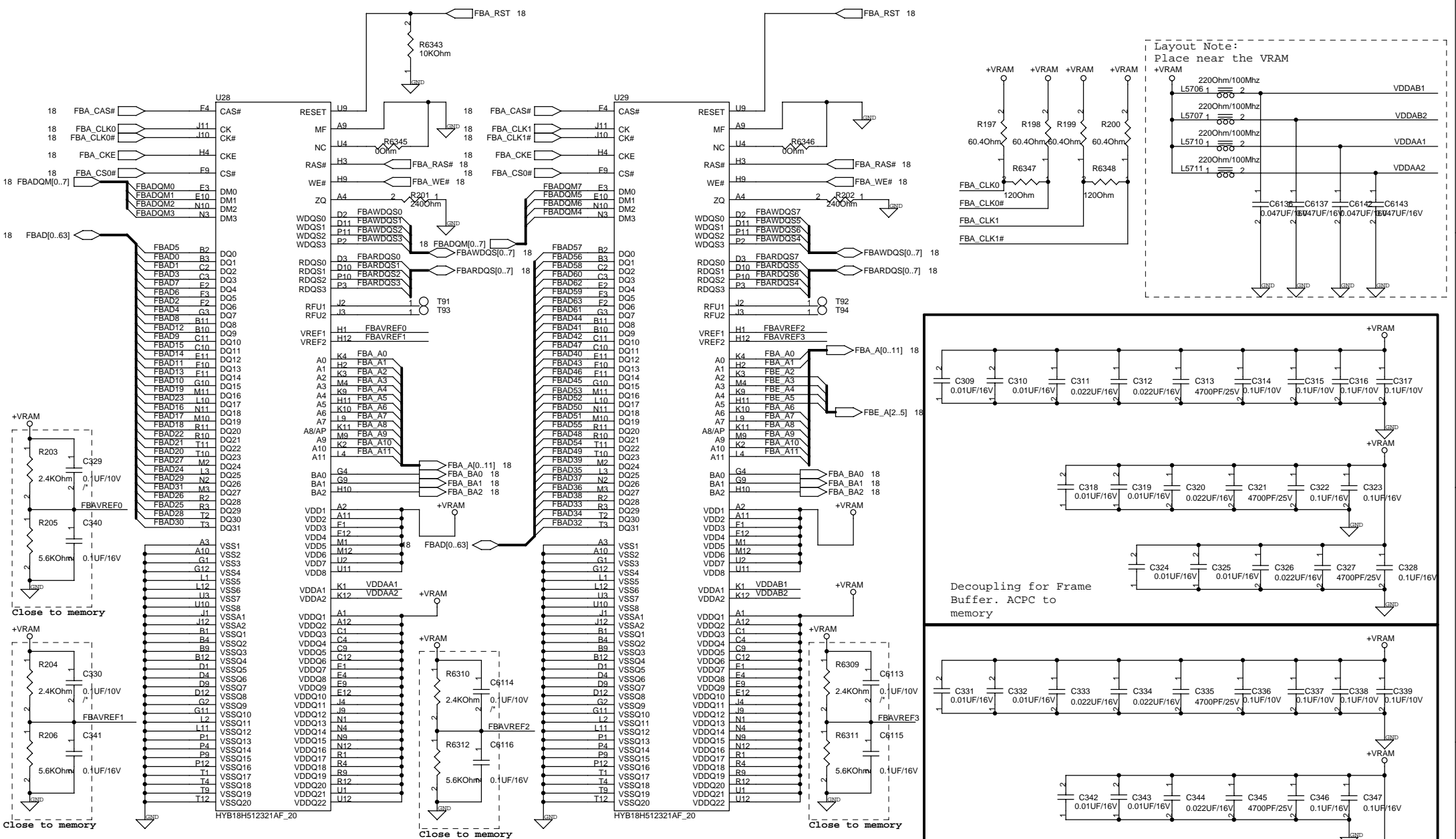
DESCRIPTION:

DDR2 Res

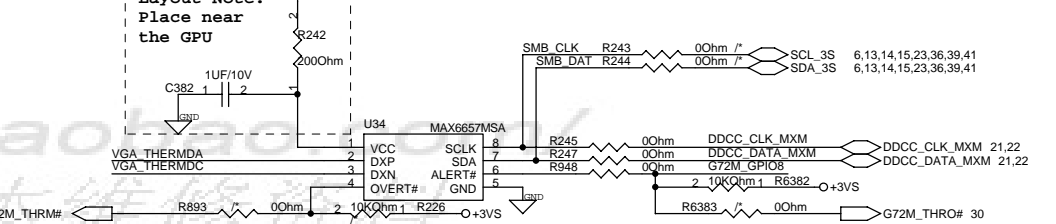
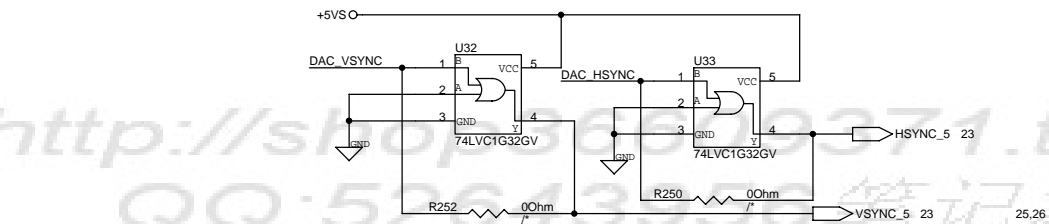
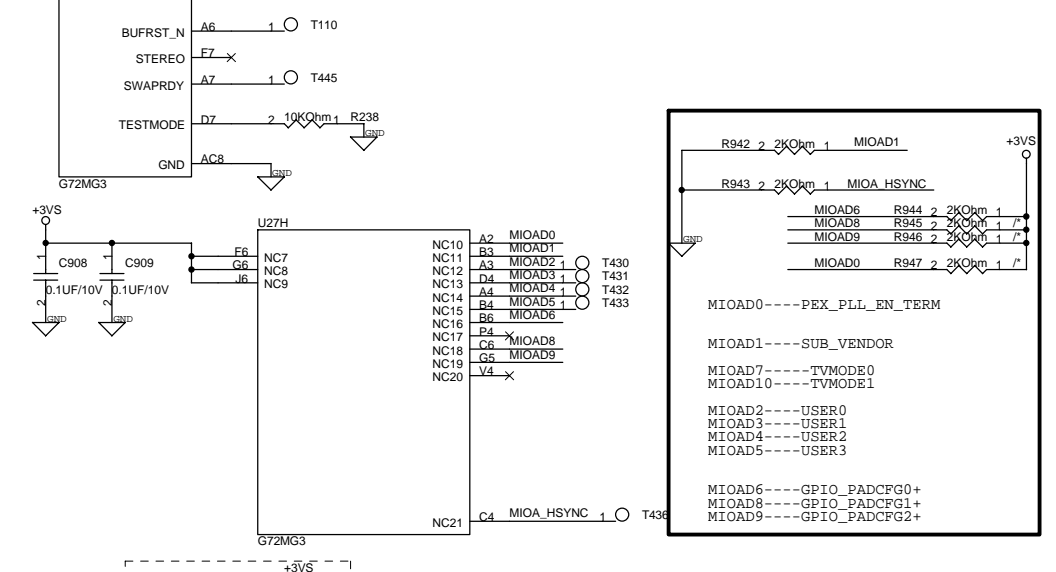
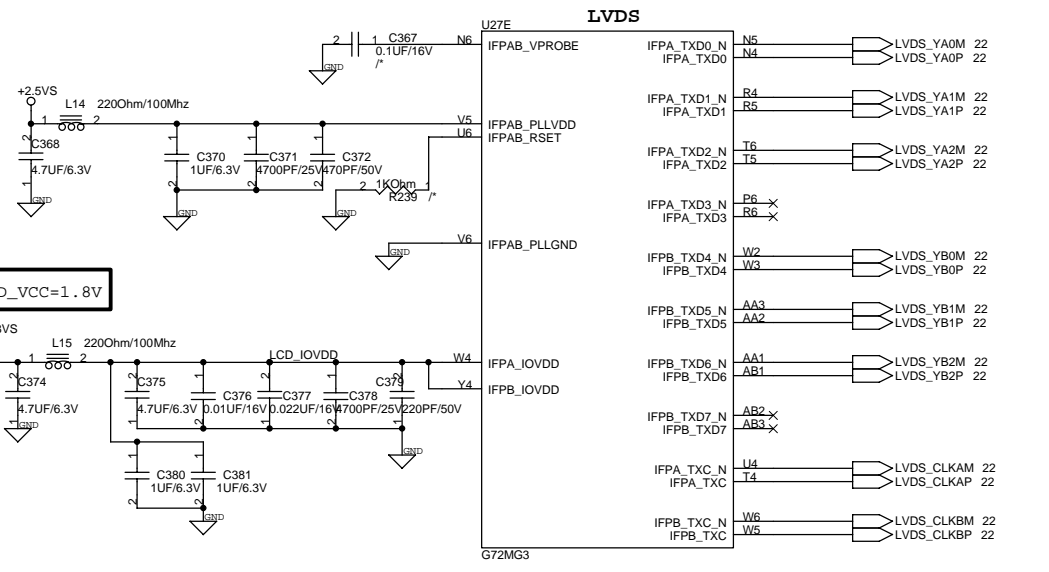
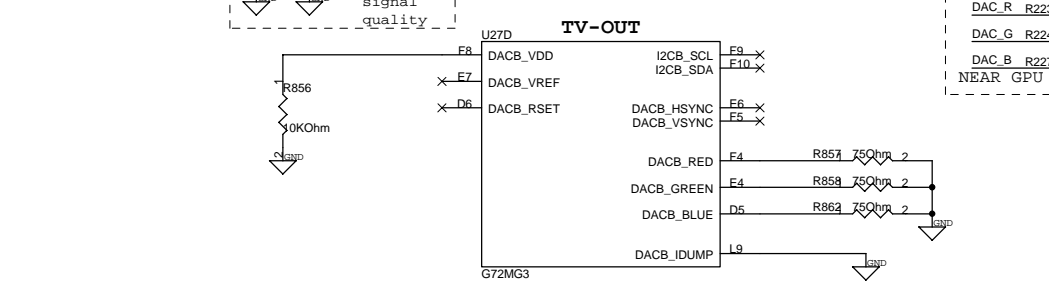
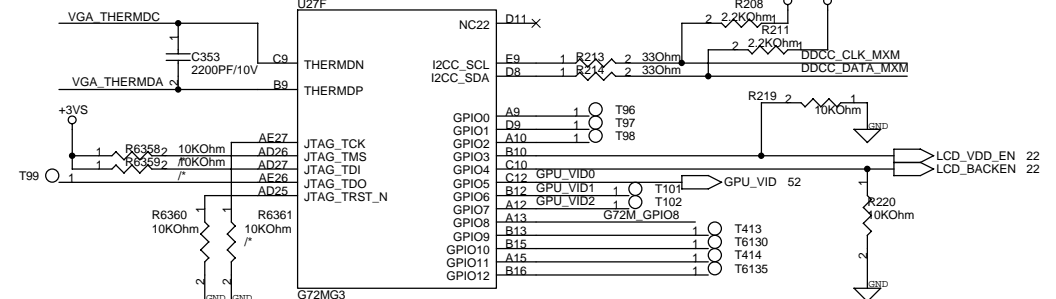
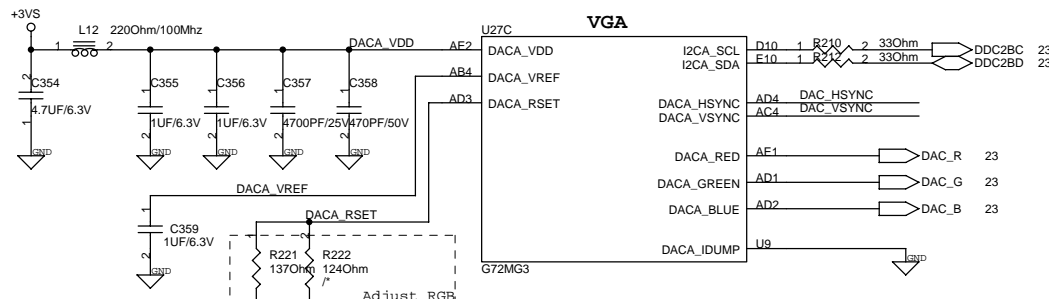
SCHEMATIC FILE NAME :
RELEASE DATE :

<OrgName>

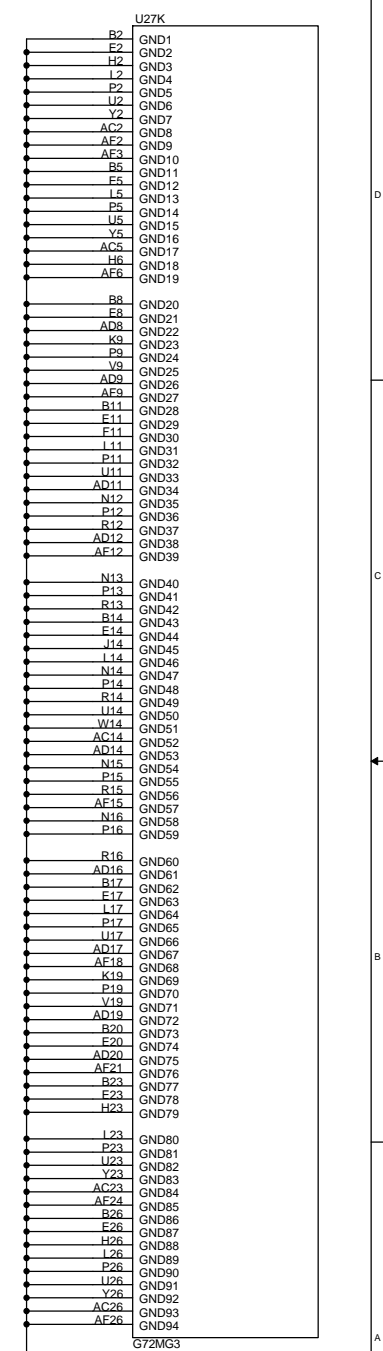
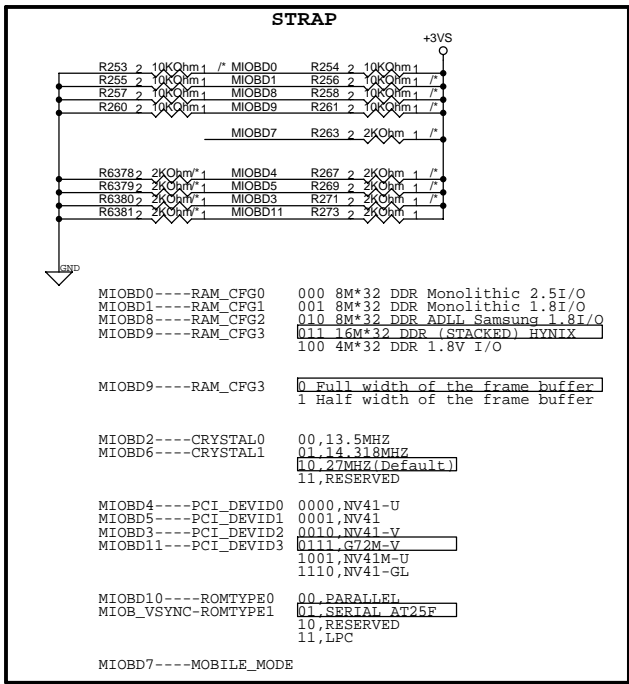
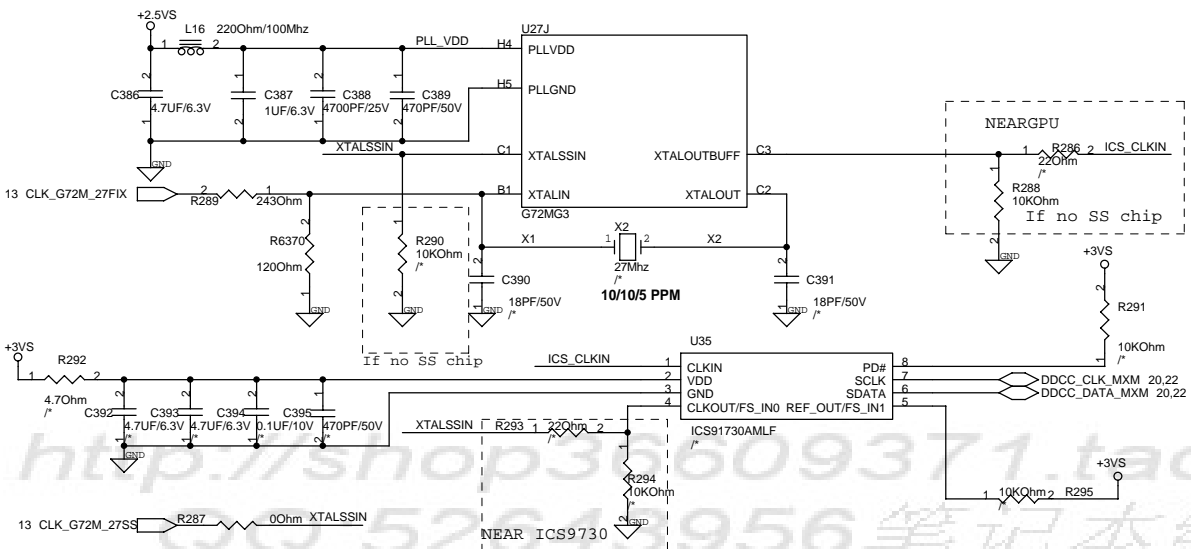
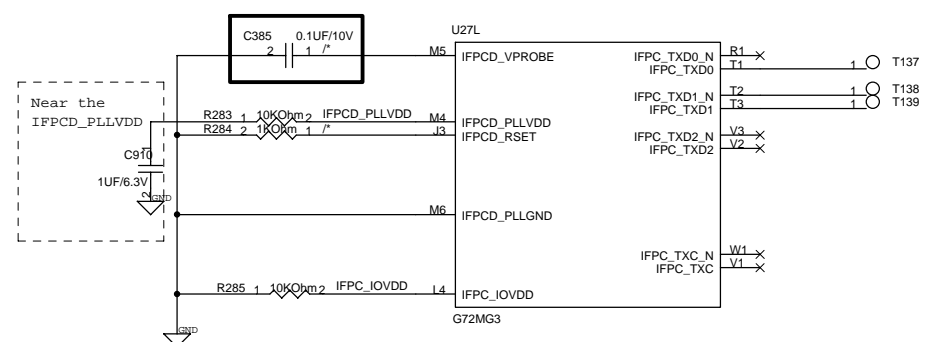
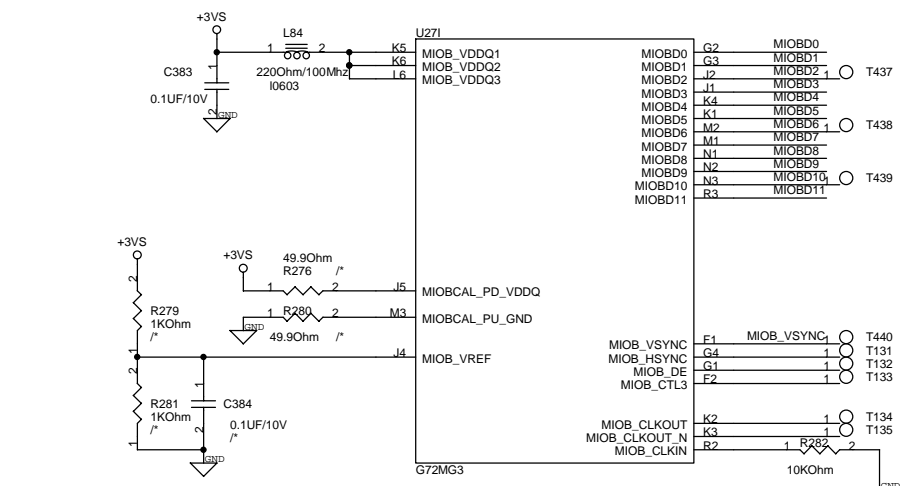
DESIGN ENGINEER :
Feng Lin

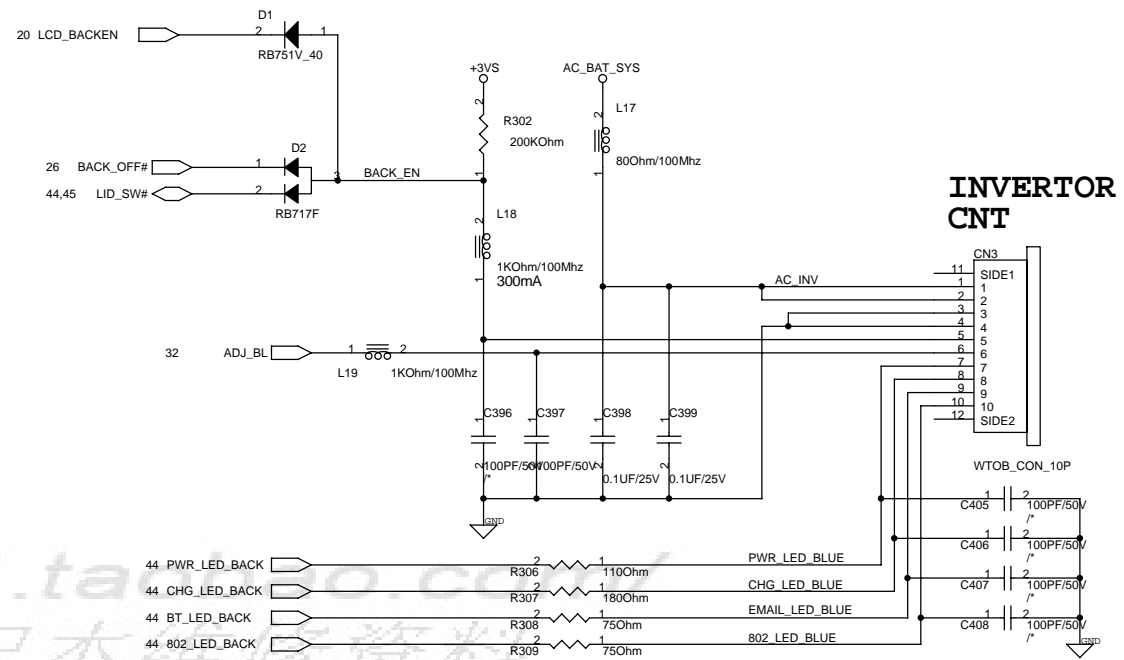
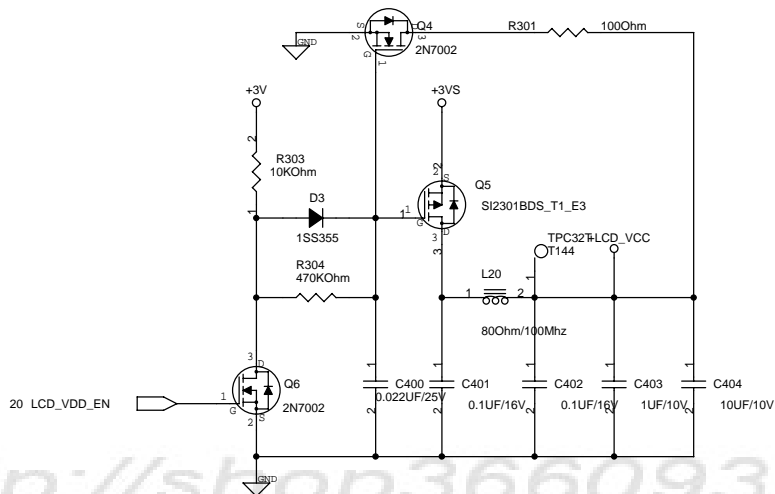
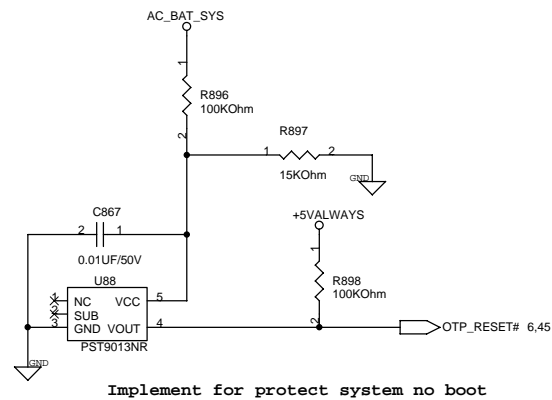
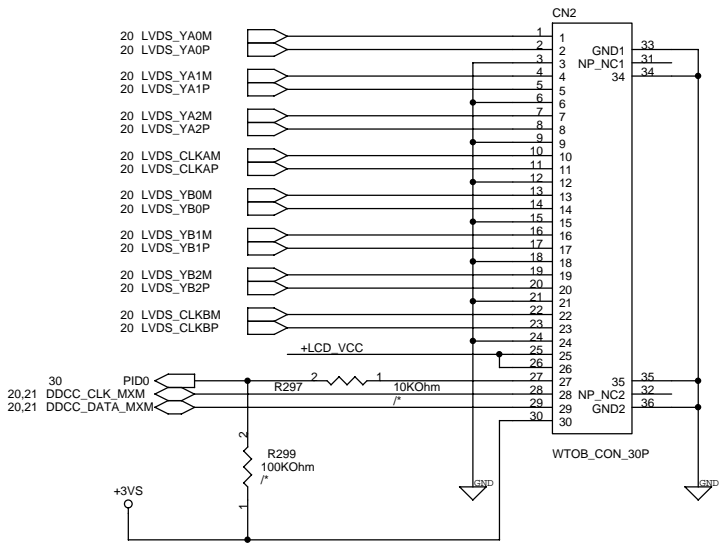


FBVDDQ=1.8V in Infineon SPEC

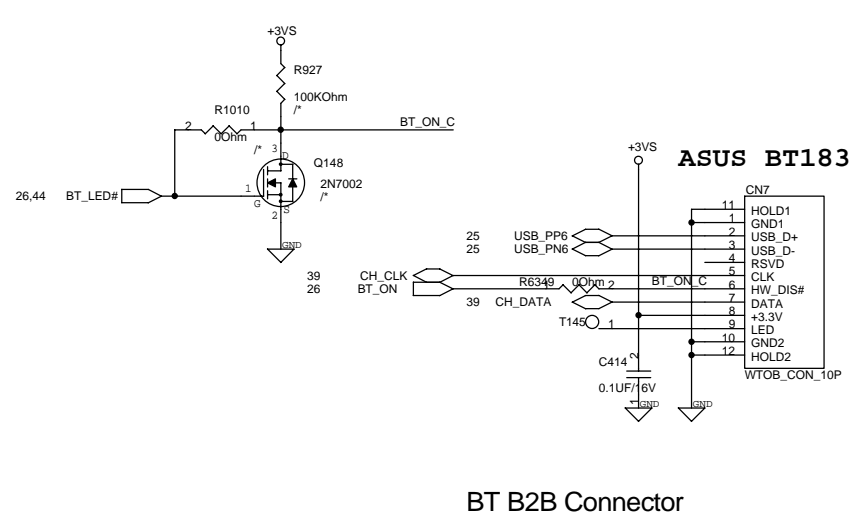
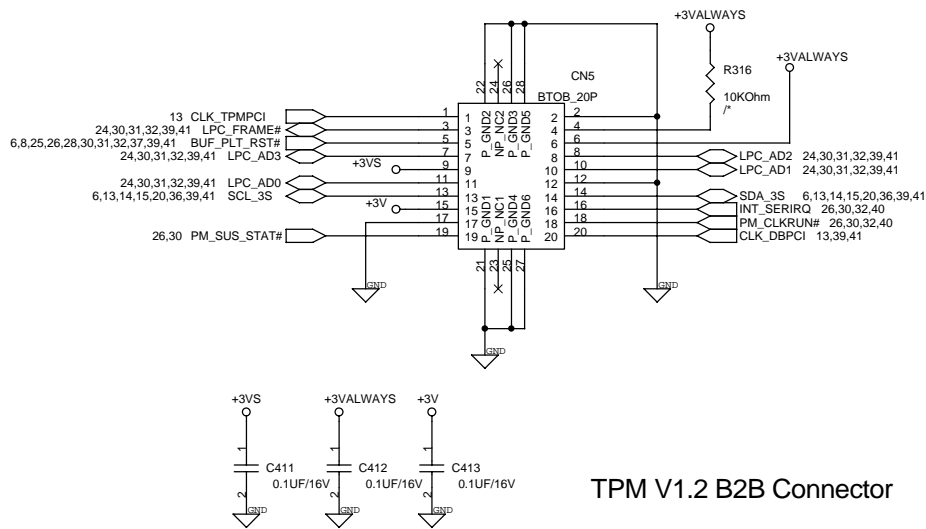
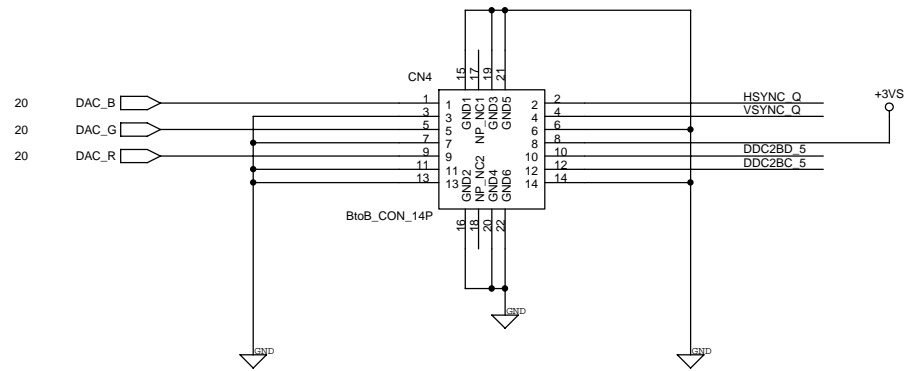
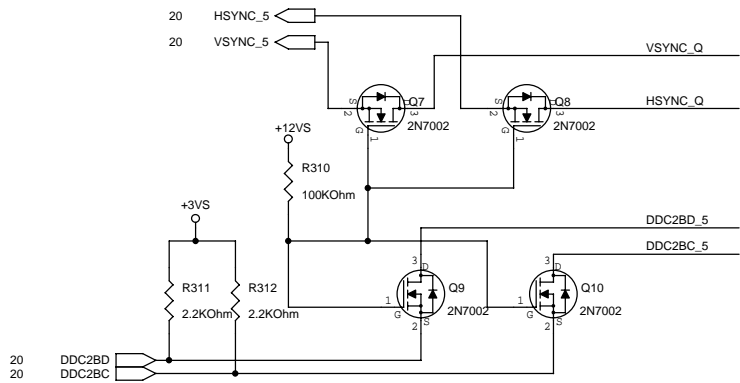


Layout Note:
Place near the GPU

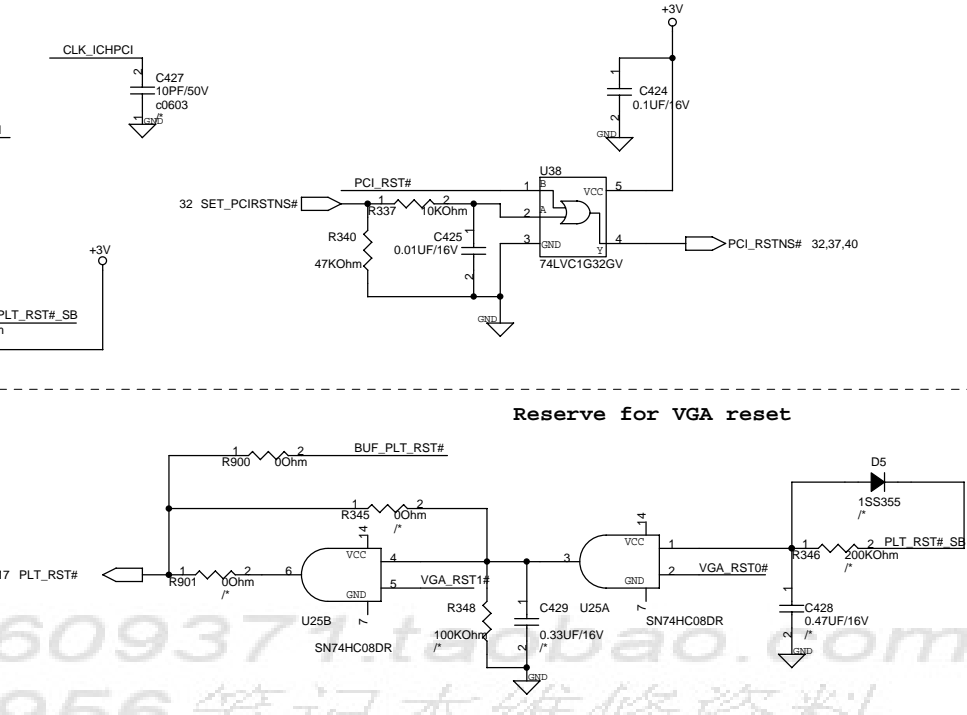
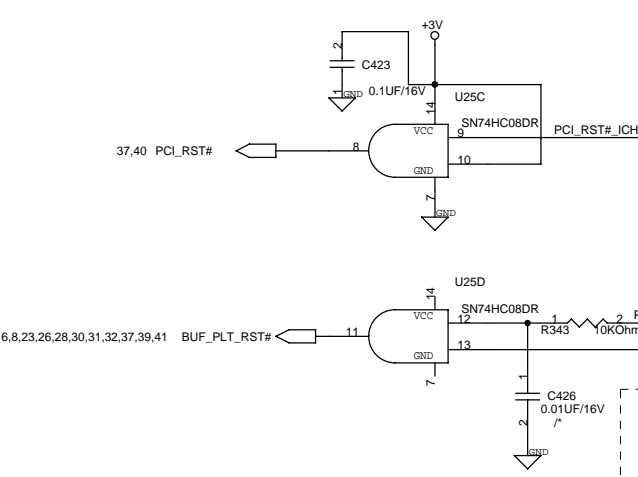
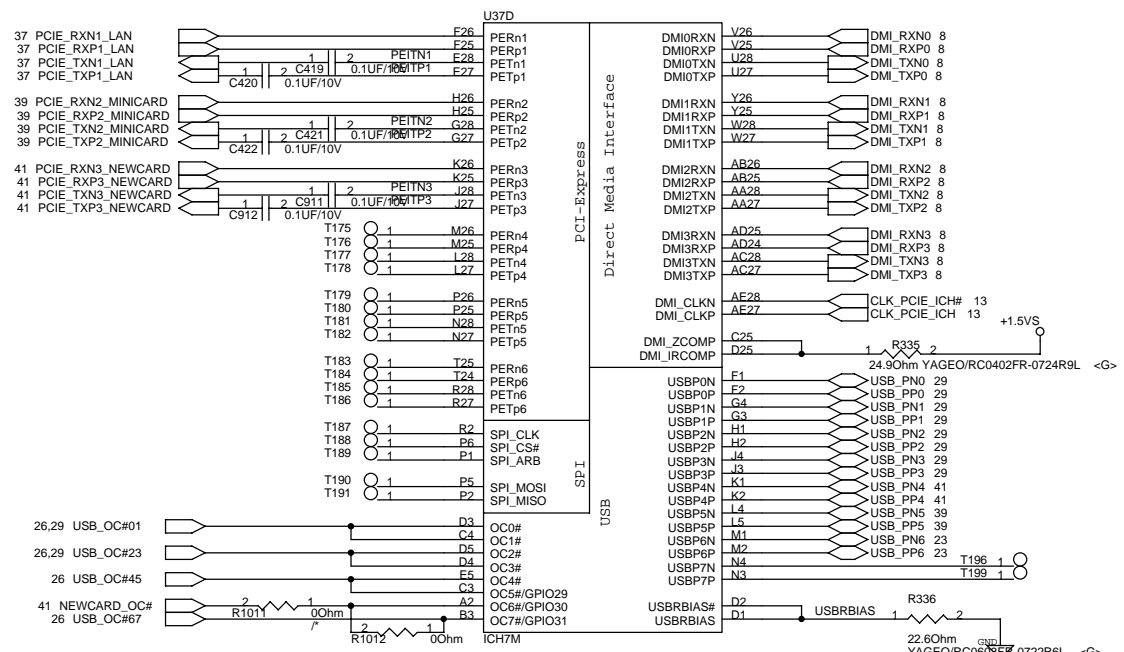
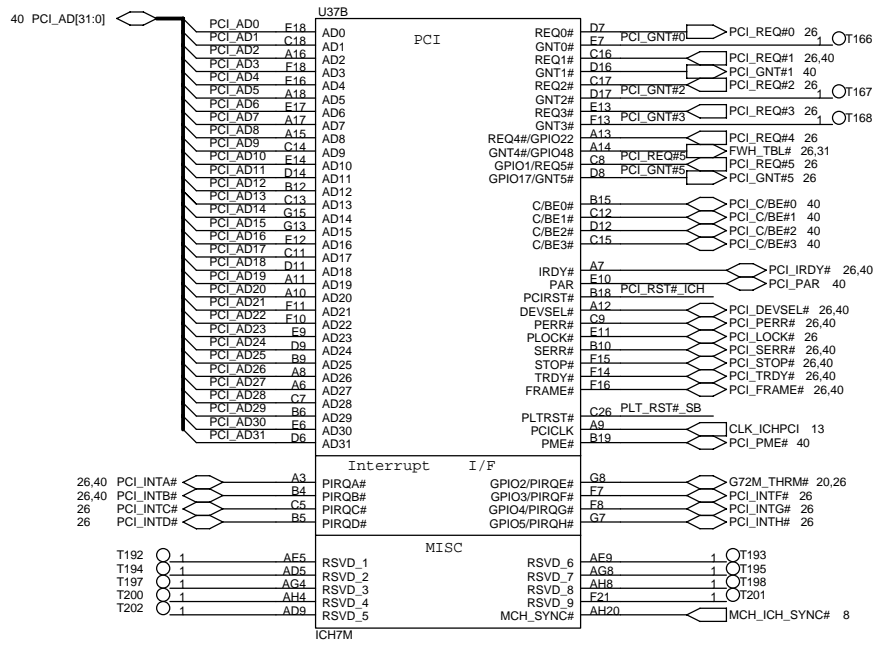


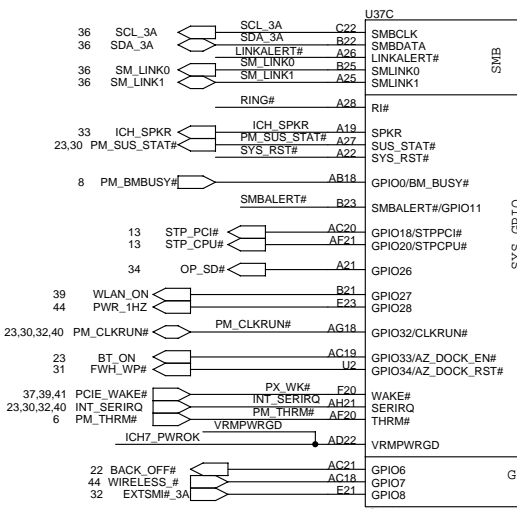


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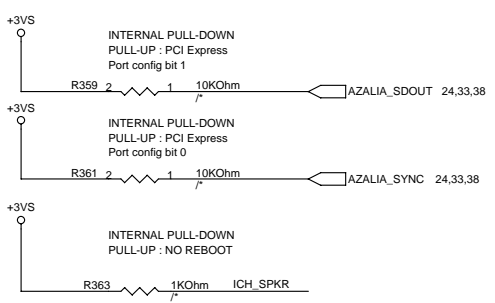
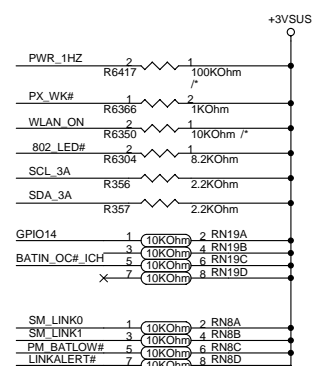
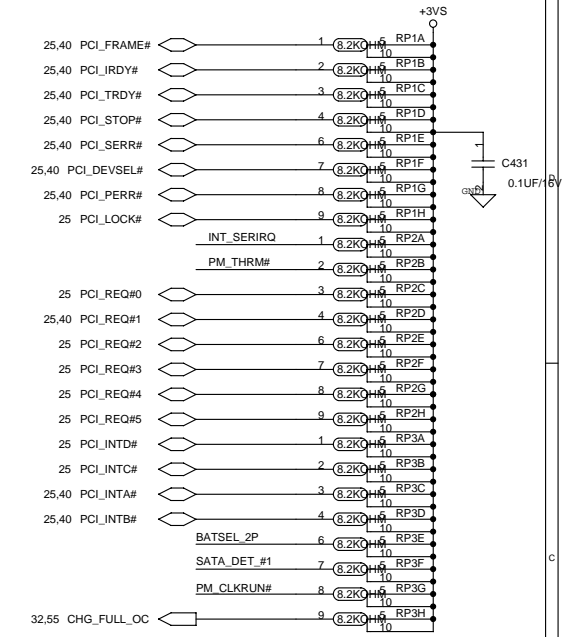


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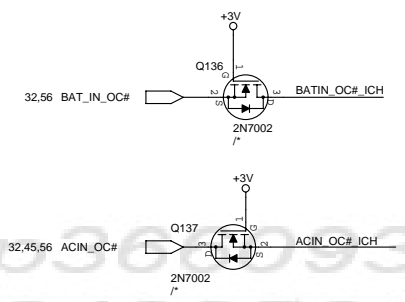
PWROK active no sooner than 100ms after Vcc3_3 and Vcc1_5



INTERNAL PULL-DOWN SIGNALS :
 AC_BITCLK, AC_RST#, AC_SDIN[2:0], AC_SDOUT, AC_SYNC, DPSP_LVPR, LAN_CLK, PDD[7], PDDREQ, SPKR, USB[7:0][P.N], SPL_ARB, SPL_CLK, GPIO[16]

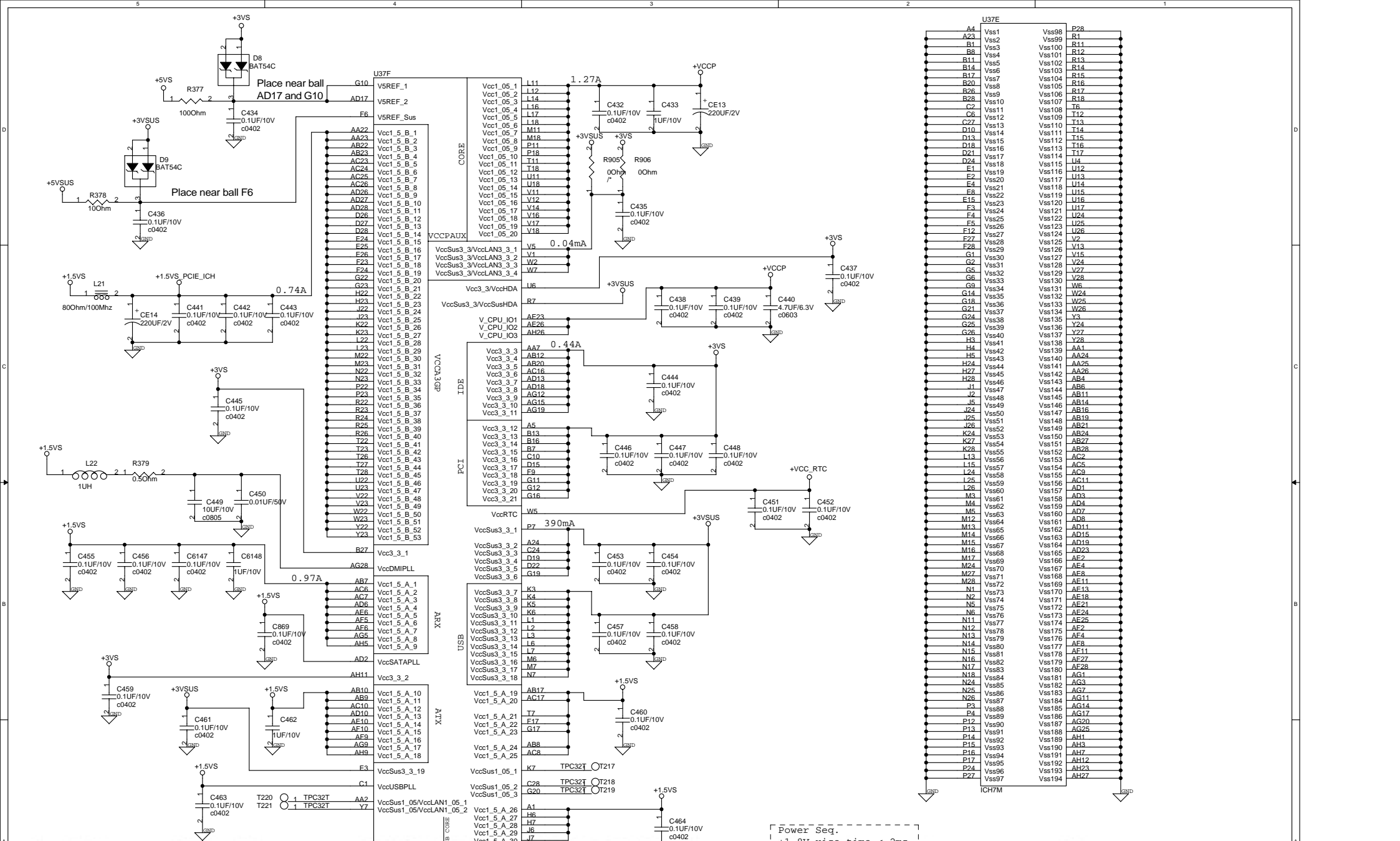
INTERNAL PULL-UP SIGNALS :
 EE_DIN, EE_DOUT, EE_CS, GPIO[17], LAD[3:0]#, LDRQ[0:1], LAN_RXD[2:0], PME#, PWRBTN#, TP3, SATALED#, GNT[5:0]

	GNT#5	GNT#4	(default)
LPC	11	1	
PCI	10	1	0
SPI	01	0	1

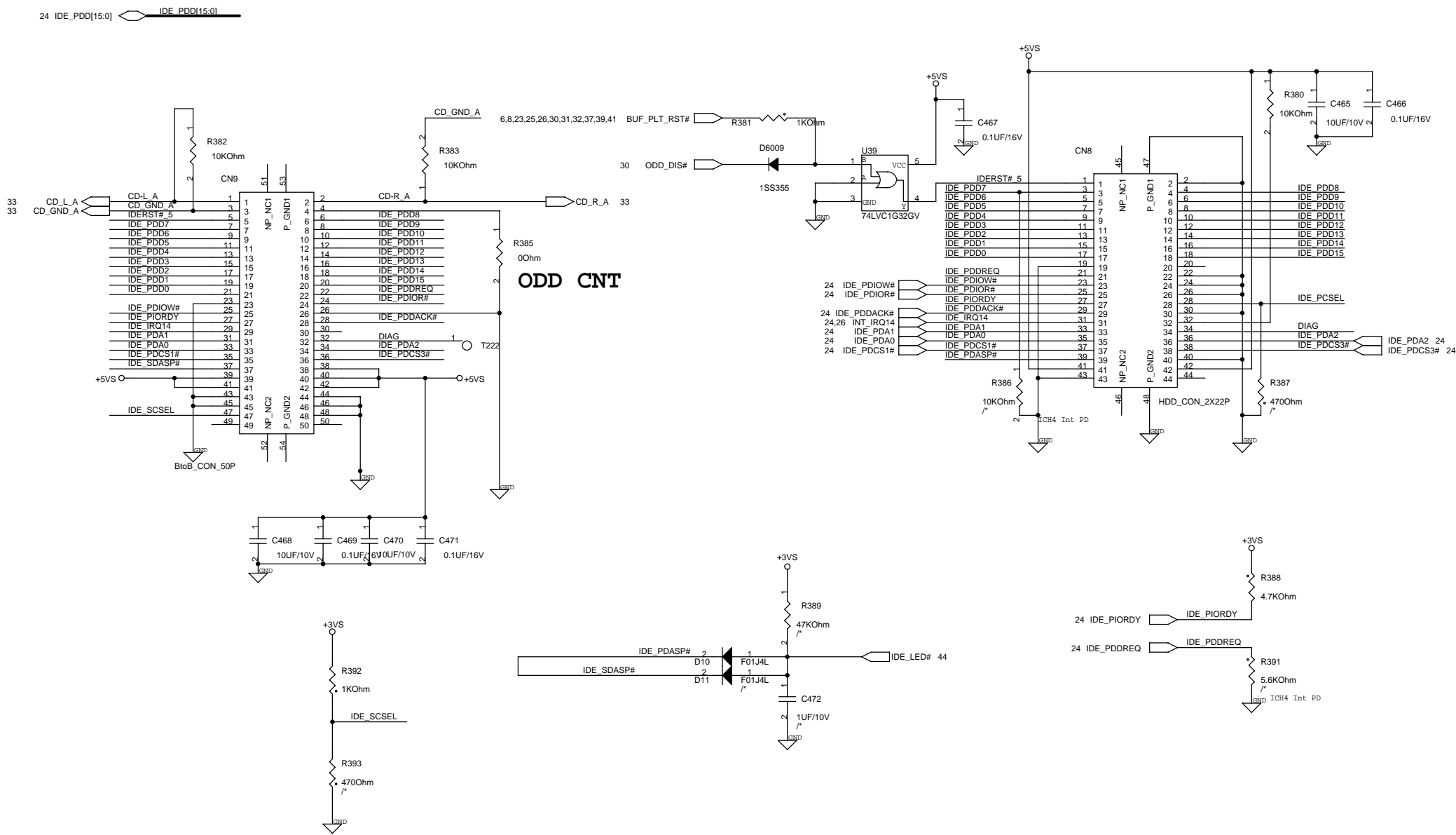


PCB_VID2	PCB_VID1	PCB_VID0
0 0 0	0 0 1	V1.0
0 0 1	0 1 0	V1.1
1 0 0	0 1 1	V2.0
X	X	X

<http://shop3609371.taobao.com/>
 QQ:52643956 笔记本维修资料

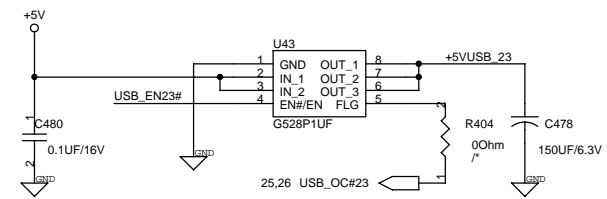
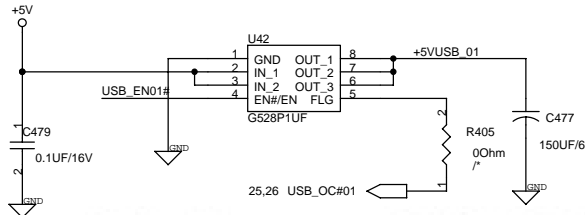
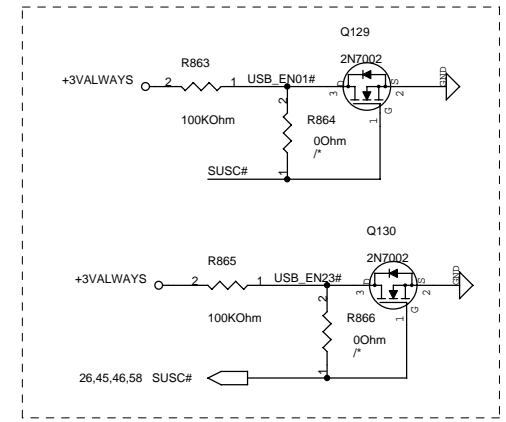
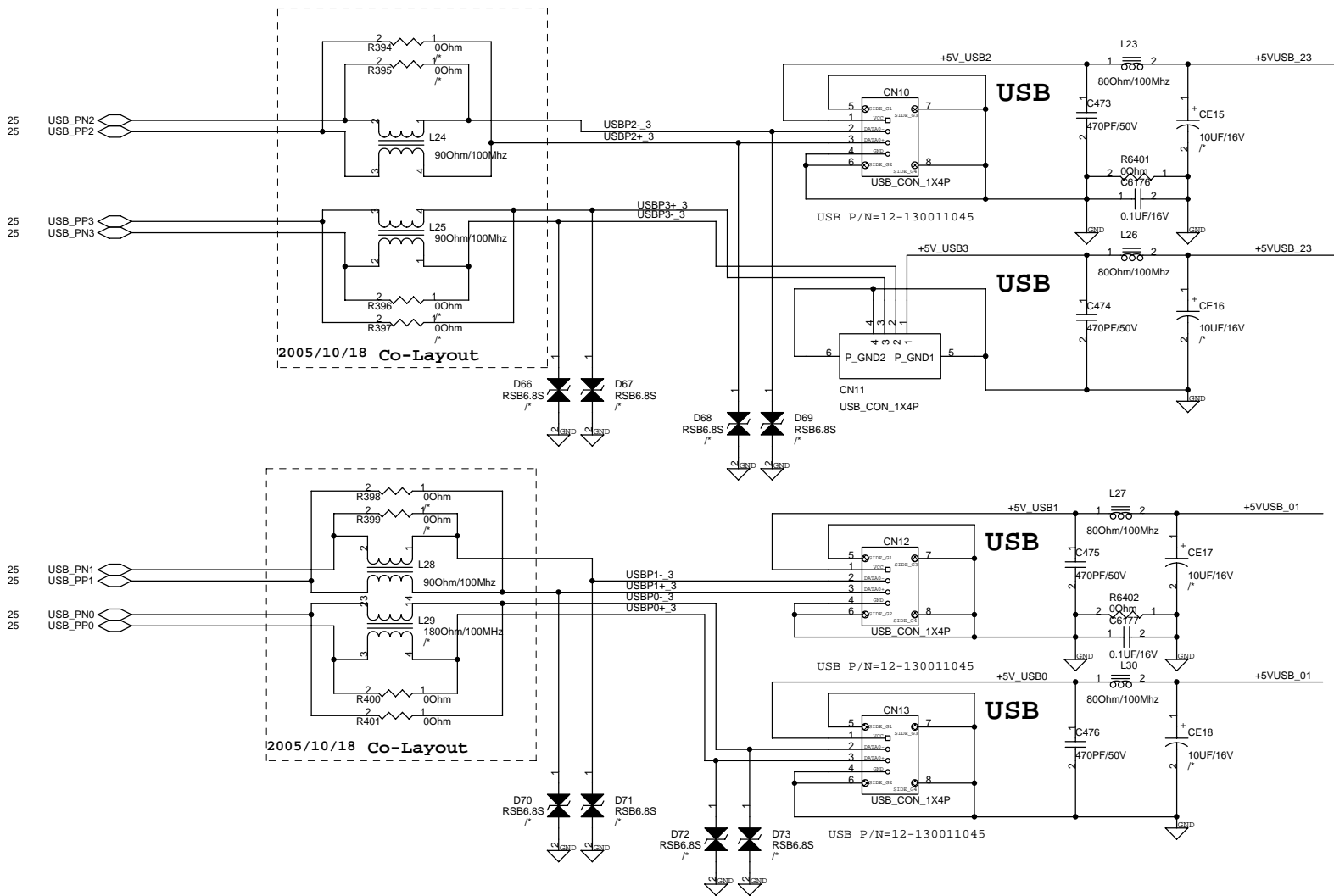


Power Seq.
+1.8V rise time < 2ms
+1.5VS --> +VCCP
+5VS --> +3VS
+5VSUS --> +3VSUS

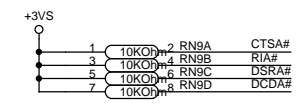
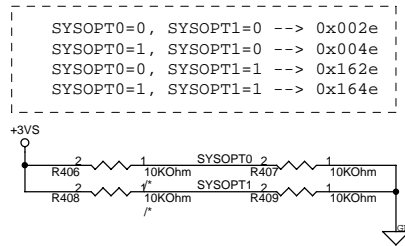
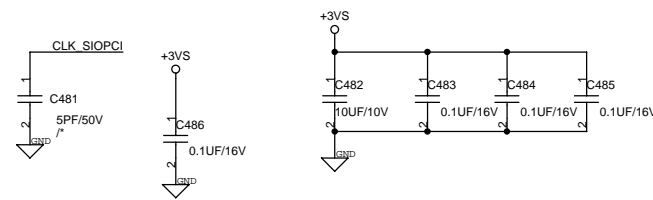


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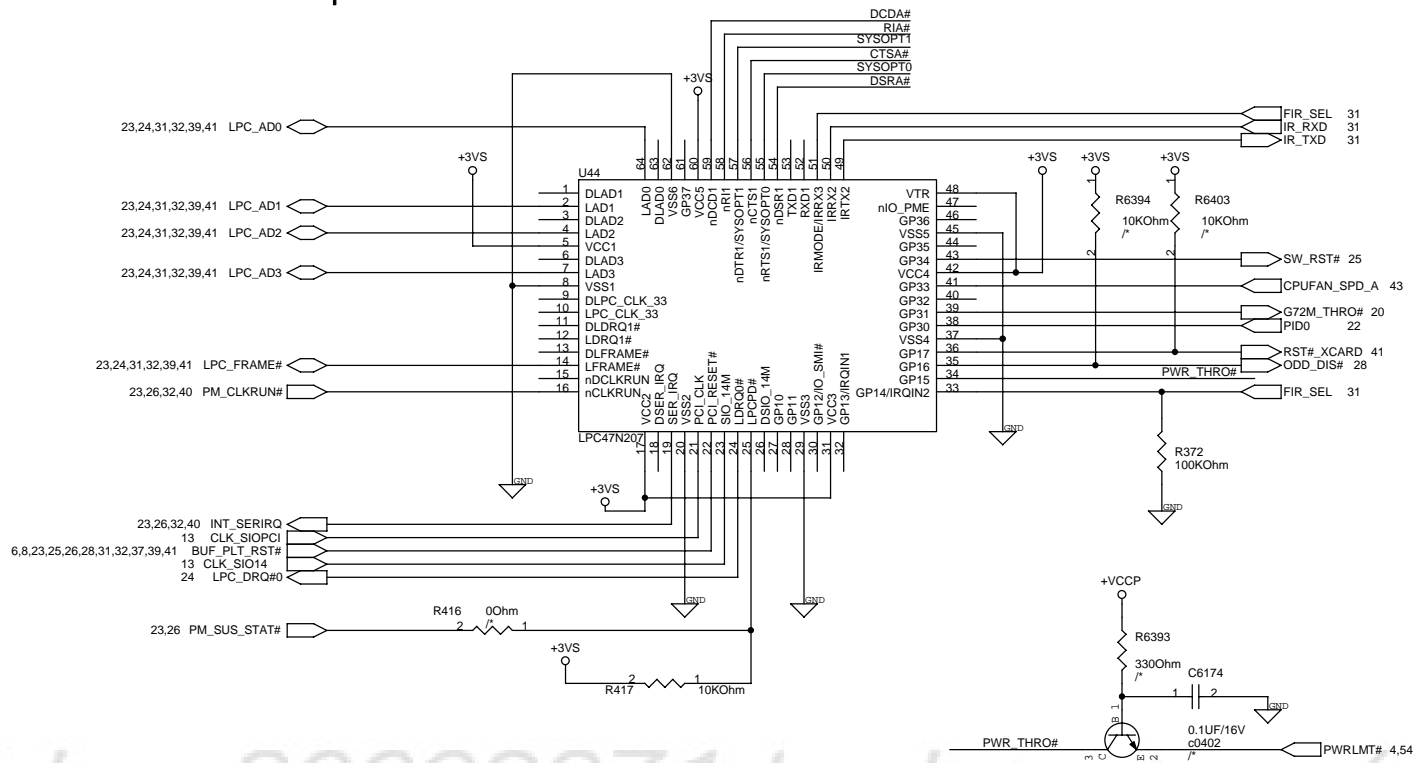
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	2.0	SHEET 28 OF 63	HDD & ODD CONN.	RELEASE DATE :		Julian Kuo



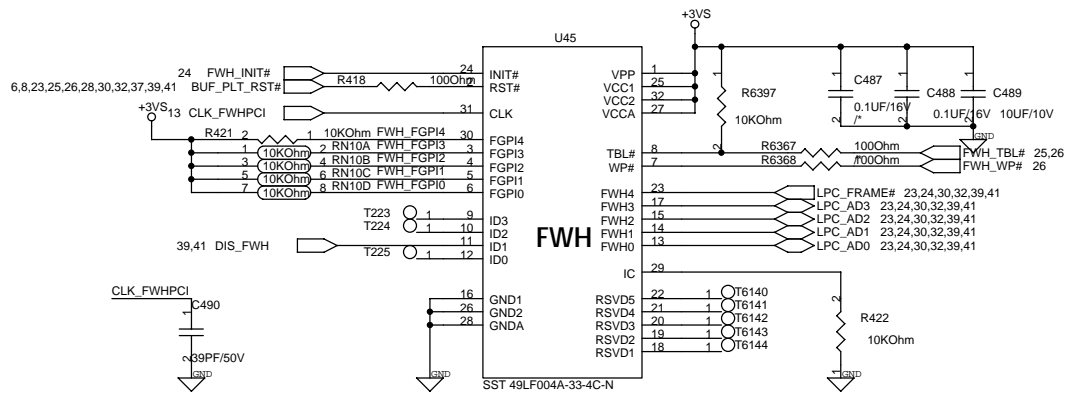
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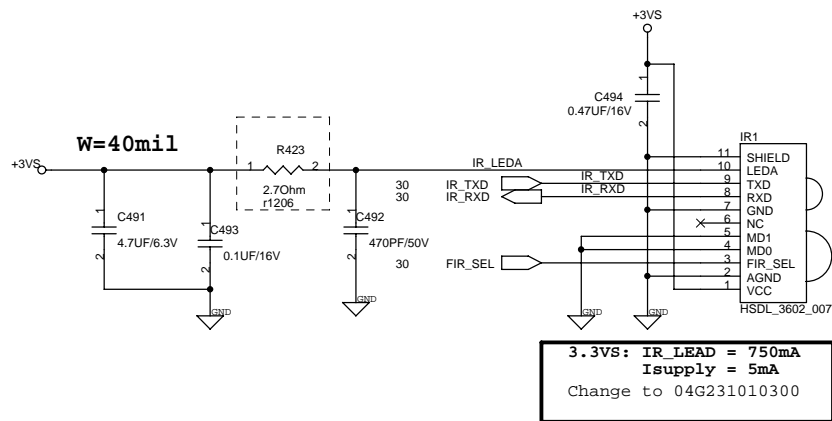
Super I/O



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PLCC32 Socket Part Number :
 12G04300032F,12-04300032I
 ,12-04300032J,12-04300032J

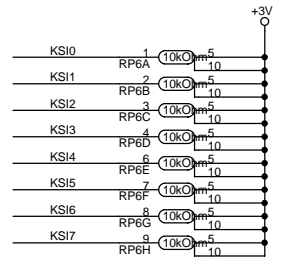


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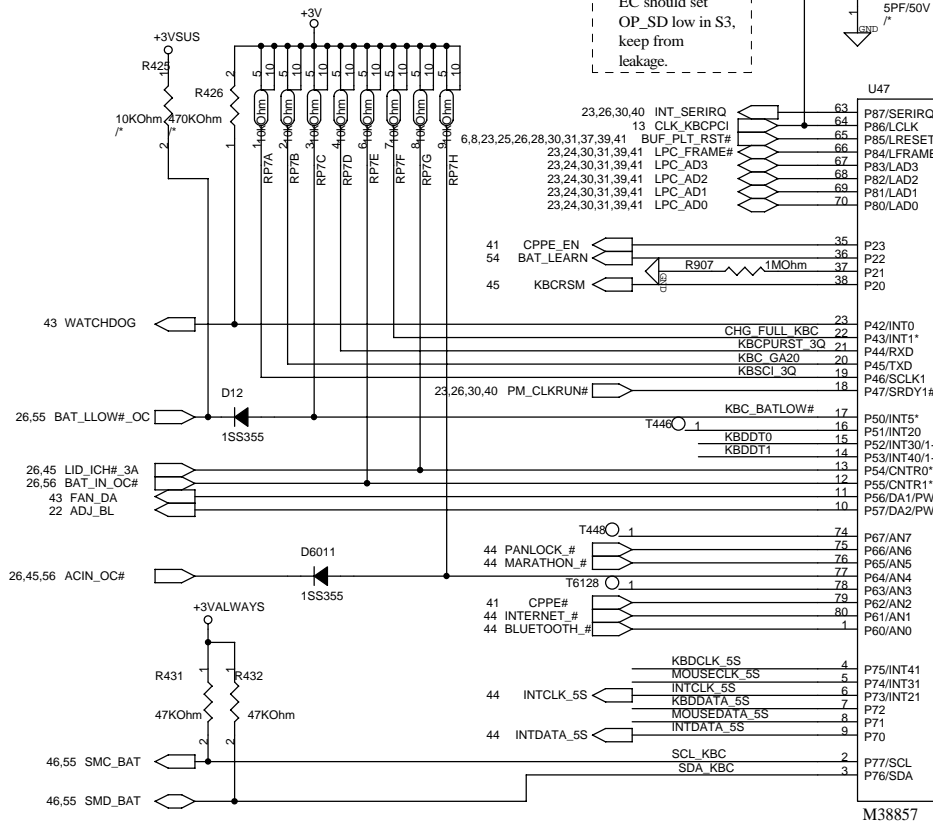
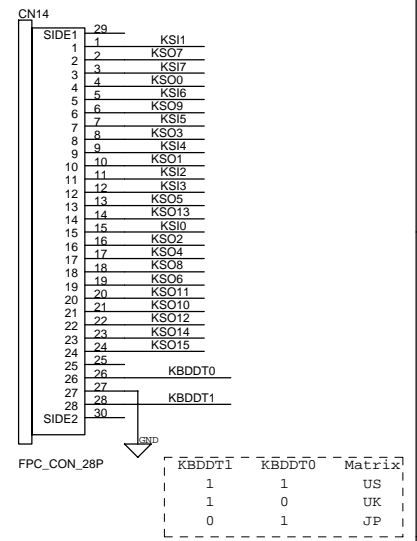
P2.1 Low : Power Button Override disable
Input Event only at P54, P55, P60 - P67

P50, P43, P54, P55 are wake-up event inputs when KBC in standby mode

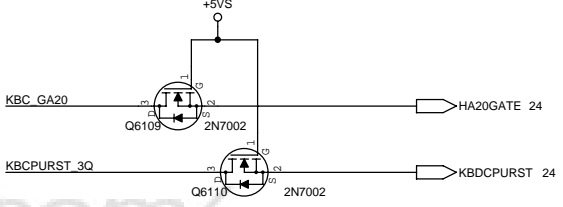
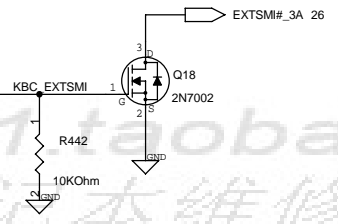
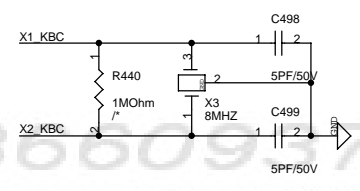
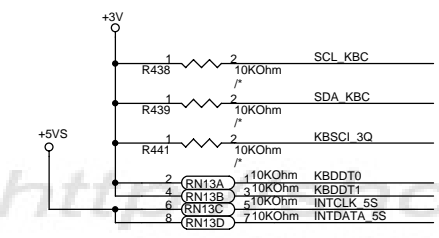
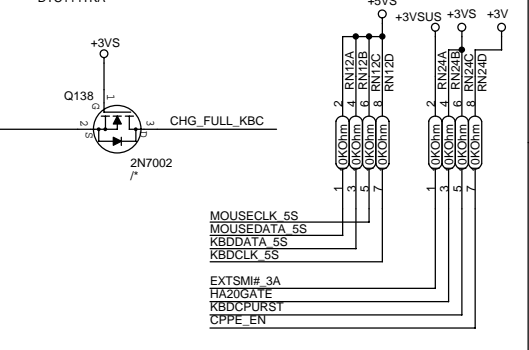
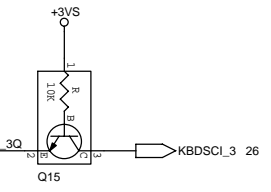
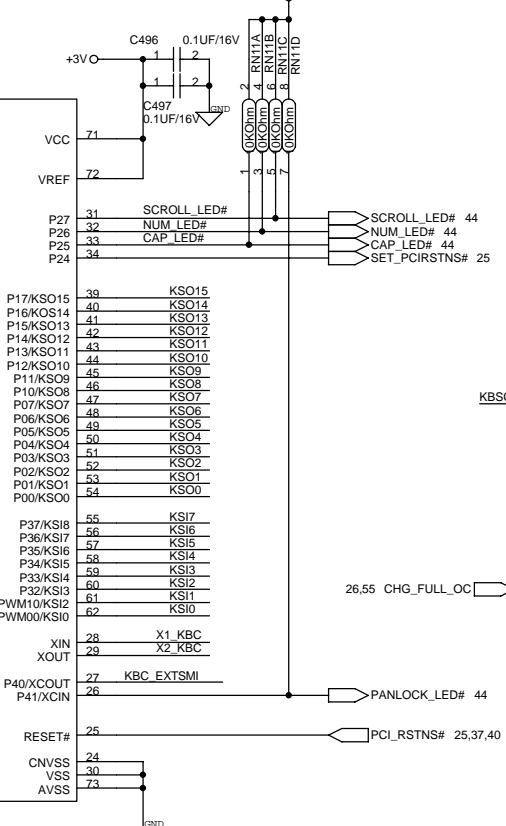
EC should set
 OP_SD low in S3,
 keep from
 leakage.



KEYBOARD CNT

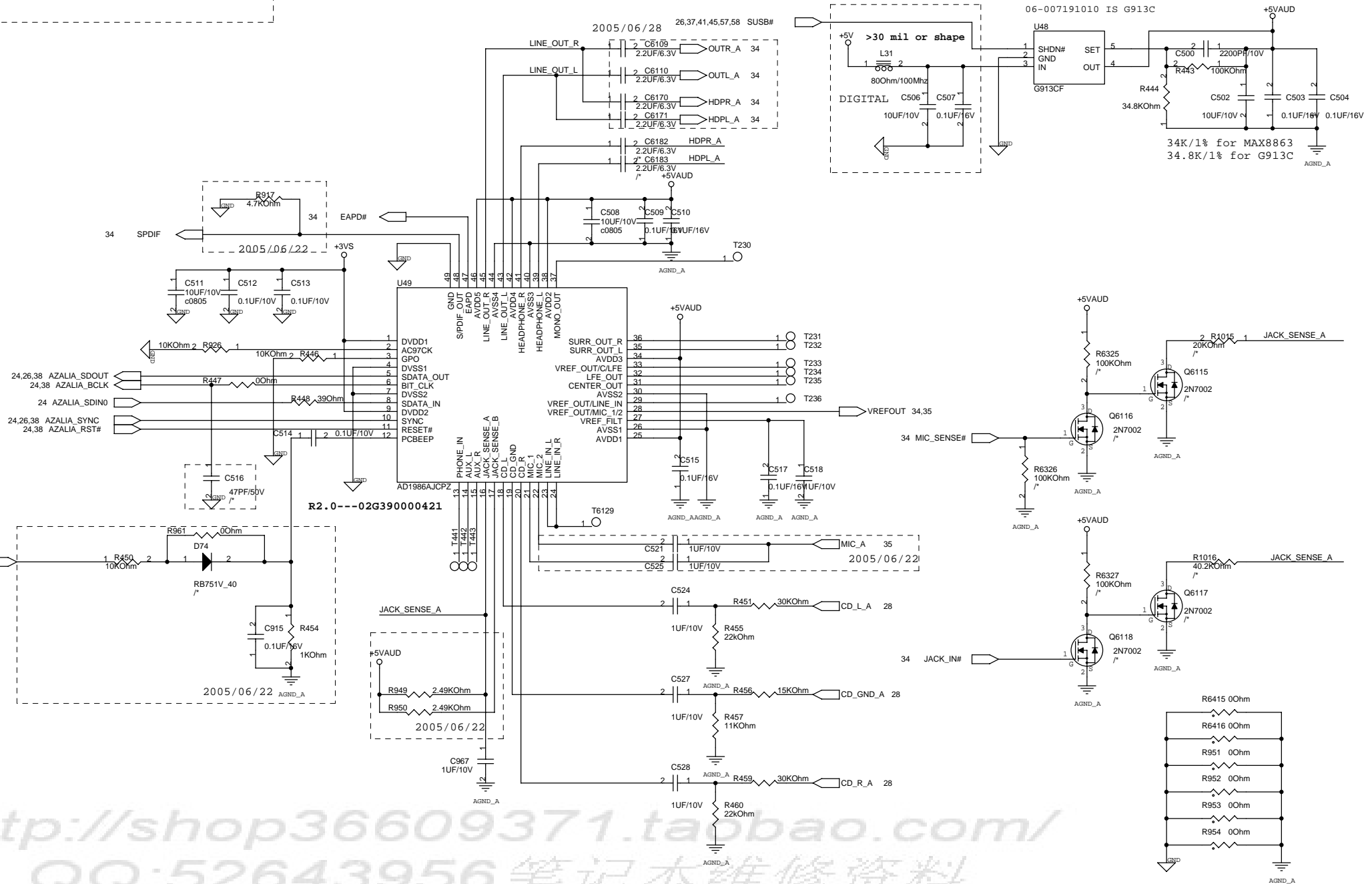


P54, P55, P43, P50 are
 wake-up event
 inputs when KBC in
 standby mode



Internal pull low: SDATA-IN
 Internal pull up: JD0, JD1, JD2, XTLSSEL

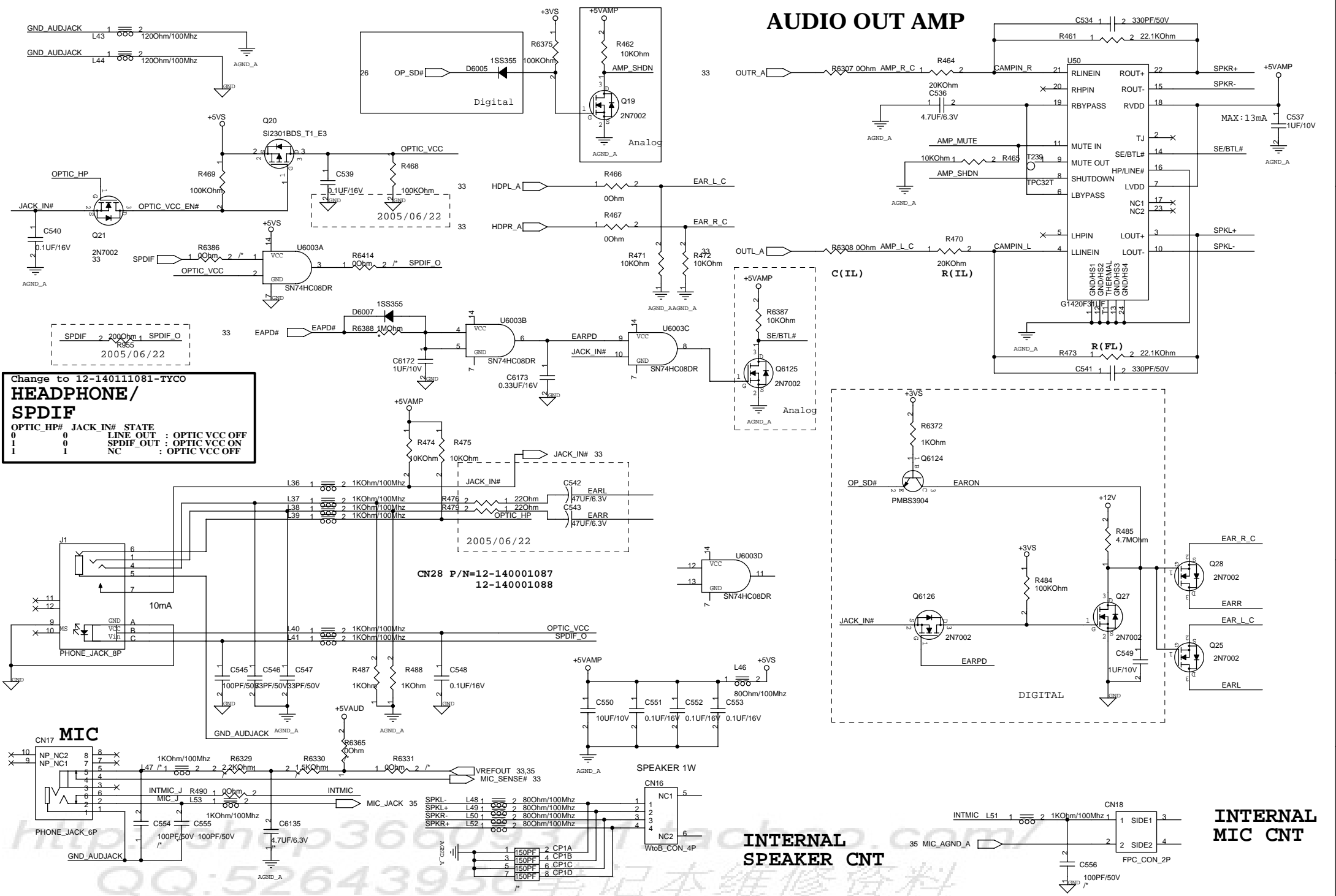
$$V_o = V_{ref} = (1.250) * (1 + R_{428}/R_{429}) - G_{913C}$$



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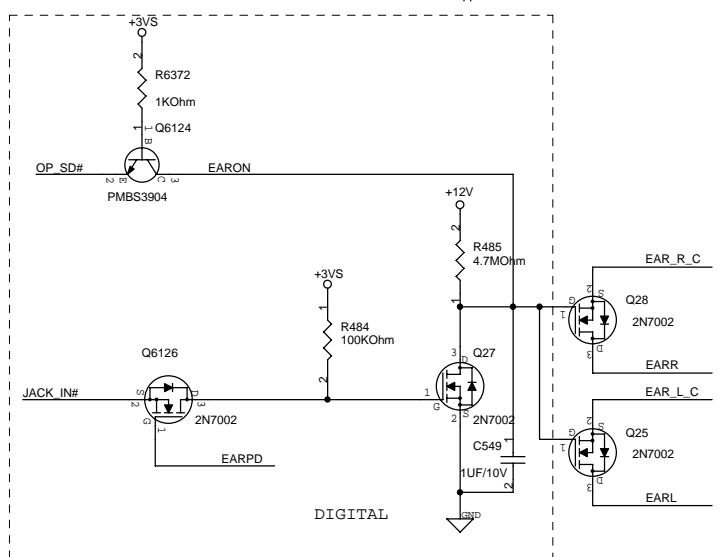
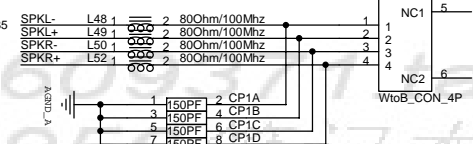
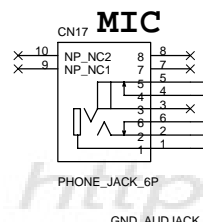
ASUS	PROJECT: V6J	REVISION	DATE: Friday, November 25, 2005	DESCRIPTION:	SCHMATIC FILE NAME :	<OrgName>	DESIGN ENGINEER :
		2.0	SHEET 33 OF 63	AUDIO AD1986	RELEASE DATE :		Feng Lin

AUDIO OUT AMP



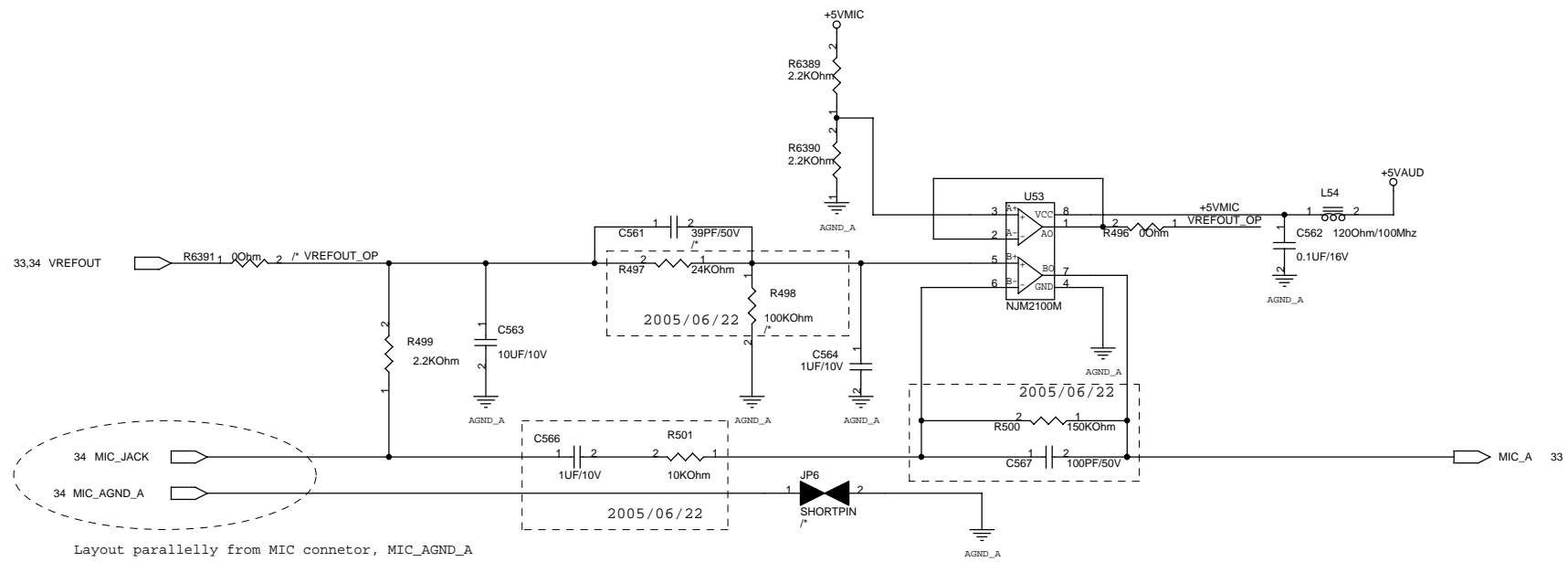
Change to 12-140111081-TYCO HEADPHONE/SPDIF

OPTIC_HP#	JACK_IN#	STATE
0	0	LINE_OUT : OPTIC VCC OFF
1	0	SPDIF_OUT : OPTIC VCC ON
1	1	NC



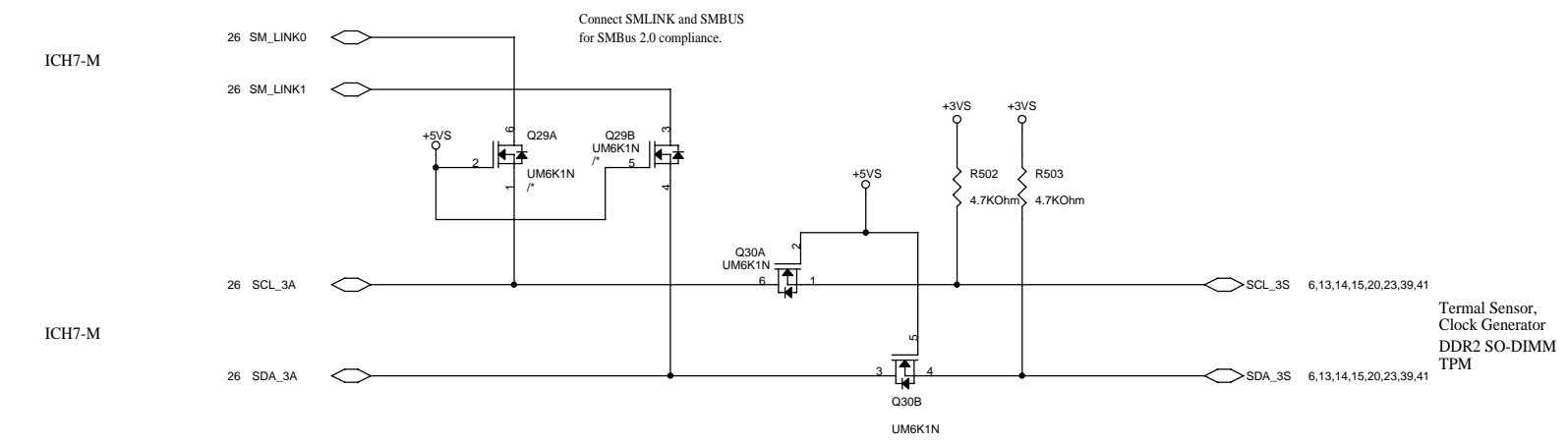
INTERNAL MIC CNT

INTERNAL SPEAKER CNT



Layout parallely from MIC connetor, MIC_AGND_A
short AGND_A by JP3 near U48

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Termal Sensor,
Clock Generator
DDR2 SO-DIMM
TPM

+3VALWAYS	O	+3VALWAYS	23,24,29,32,44,45,46,51,60
+3VSUS	O	+3VSUS	26,27,32,37,41,45,48
+5VALWAYS	O	+5VALWAYS	22,48,51,54
+5VSUS	O	+5VSUS	27,44,48
+3VO	O	+3V	22,23,25,26,32,37,38,39,41,42,44,45,46,51,58
+5VO	O	+5V	14,29,33,41,44,46,56,58
+12V	O	+12V	34,42,58
+3VS	O	+3VS	6,8,10,12,13,14,15,17,20,21,22,23,26,27,28,30,31,32,33,34,37,39,40,41,42,44,45,46,47,49,57,58
+5VS	O	+5VS	20,27,28,32,34,39,43,44,45,46,47,58
+12VS	O	+12VS	23,44,58
VTT_REF0	O	VTT_REF	8,14,15,16
+2.5VS	O	+2.5VS	10,20,21,46,51
+1.8VS	O	+1.8VS	20,46,58
+0.9VS	O	+0.9VS	16,50
+1.5VS	O	+1.5VS	5,8,10,11,25,27,39,41,46,49
+VCC_RTC	O	+VCC_RTC	24,27
+1.8V	O	+1.8V	8,11,14,15,46,50
+3VA	O	+3VALWAYS	23,24,29,32,44,45,46,51,60
+5VA	O	+5VALWAYS	22,48,51,54
+5VAUD	O	+5VAUD	33,34,35
VTT_REF0	O	VTT_REF	8,14,15,16
A/D_DOCK_IN	O	A/D_DOCK_IN	43,54,56,57
+3VSUS_PEO	O	+3VSUS_PE	41
+3VS_PEO	O	+3VS_PE	41
+1.5VS_PEO	O	+1.5VS_PE	41

NEWCARD

YONAH			
+VCCP	O	+VCCP	4,5,6,7,8,10,11,24,27,30,46,49
+VCORE	O	+VCORE	5,6,46,47
+1.5VS	O	+1.5VS	5,8,10,11,25,27,39,41,46,49

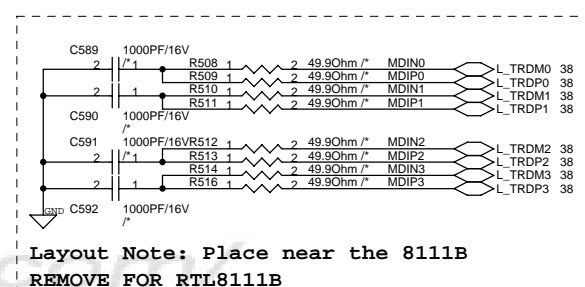
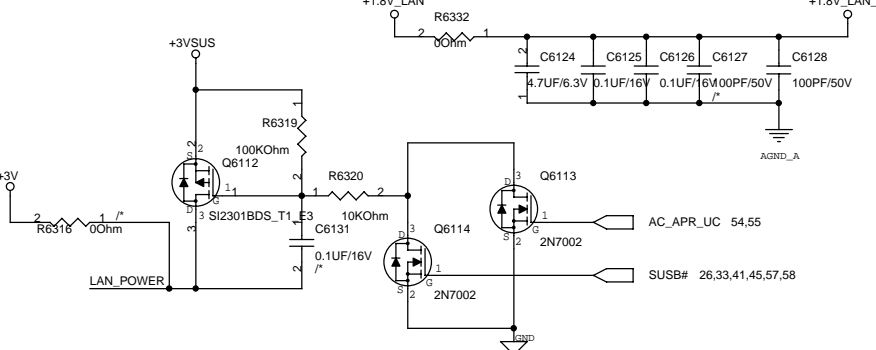
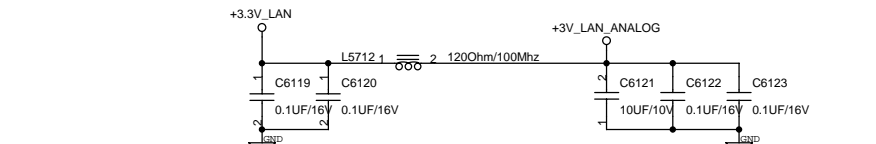
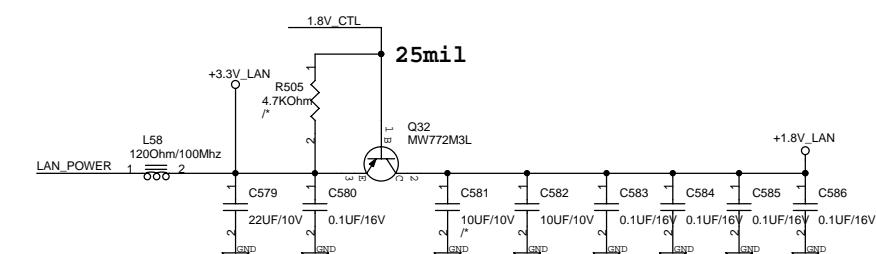
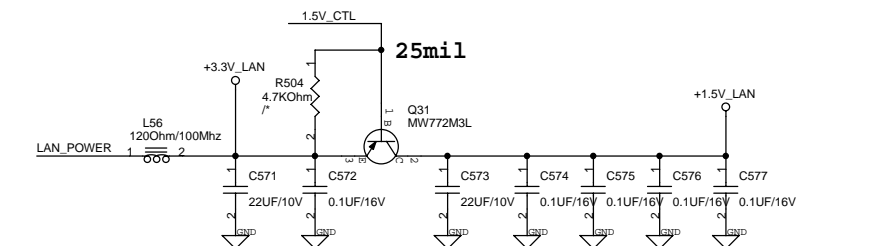
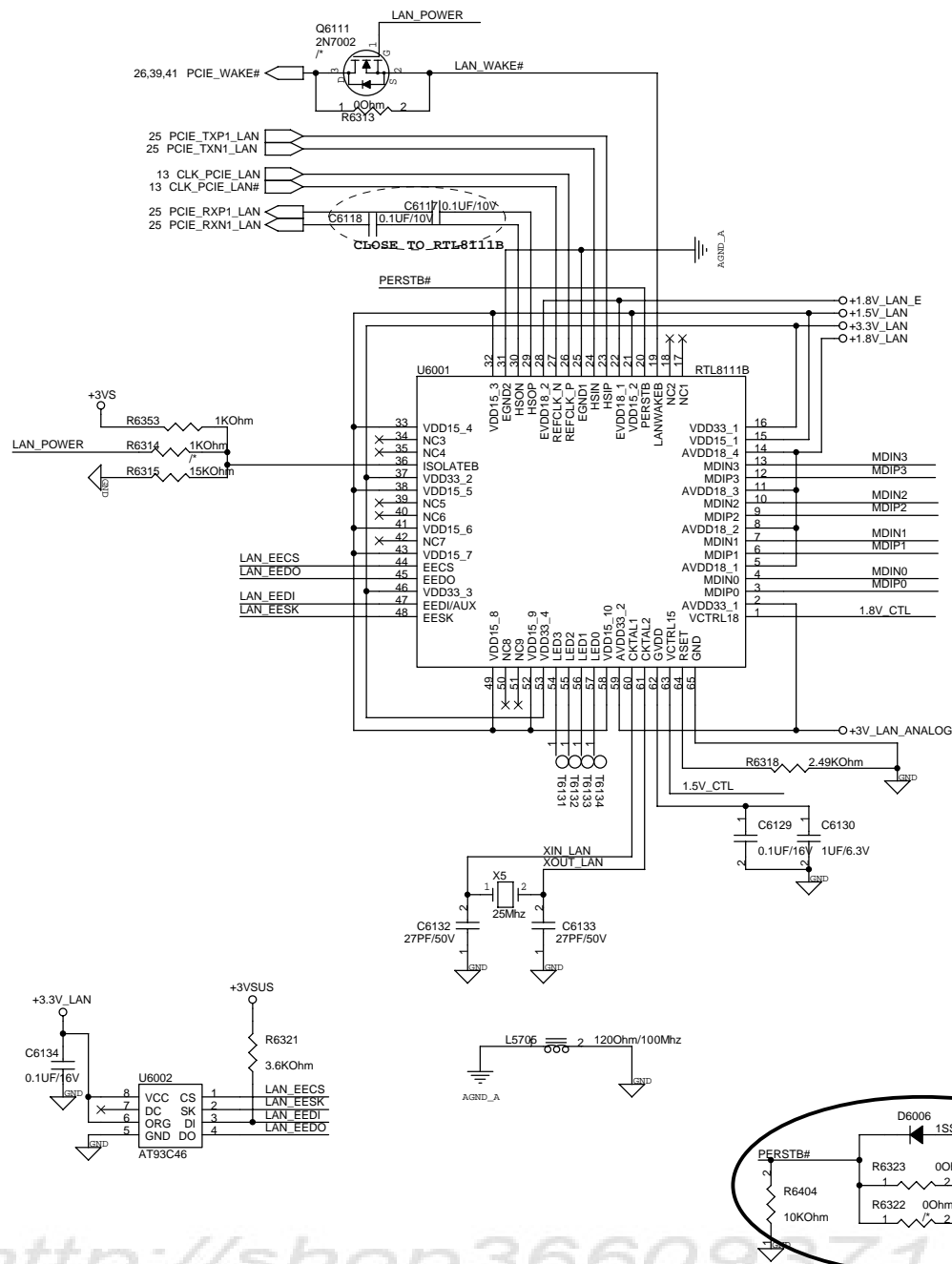
Calistoga			
+VCCP	O	+VCCP	4,5,6,7,8,10,11,24,27,30,46,49
+1.5VS	O	+1.5VS	5,8,10,11,25,27,39,41,46,49
+3VS	O	+3VS	6,8,10,12,13,14,15,17,20,21,22,23,26,27,28,30,31,32,33,34,37,39,40,41,42,44,45,46,47,49,57,58
+1.8VS	O	+1.8VS	20,46,58
VTT_REF0	O	VTT_REF	8,14,15,16
+2.5VS	O	+2.5VS	10,20,21,46,51
+1.8V	O	+1.8V	8,11,14,15,46,50

G72M G3-64			
+VGA_VCORE	O	+VGA_VCORE	17,46,52
+1.2VSP	O	+1.2VSP	17,18,46,53
+3VS	O	+3VS	6,8,10,12,13,14,15,17,20,21,22,23,26,27,28,30,31,32,33,34,37,39,40,41,42,44,45,46,47,49,57,58
+VRAM	O	+VRAM	18,19,46,52
+2.5VS	O	+2.5VS	10,20,21,46,51
+1.8VS	O	+1.8VS	20,46,58
+5VS	O	+5VS	20,27,28,32,34,39,43,44,45,46,47,58

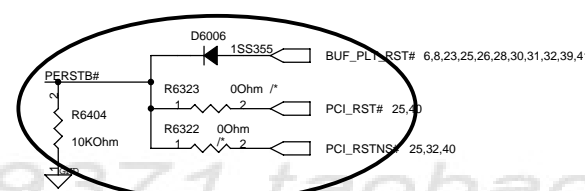
ICH7			
+VCC_RTC	O	+VCC_RTC	24,27
+VCCP	O	+VCCP	4,5,6,7,8,10,11,24,27,30,46,49
+3V	O	+3V	22,23,25,26,32,37,38,39,41,42,44,45,46,51,58
+1.5VS	O	+1.5VS	5,8,10,11,25,27,39,41,46,49
+3VSUS	O	+3VSUS	26,27,32,37,41,45,48
+5VSUS	O	+5VSUS	27,44,48

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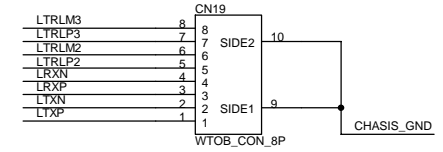
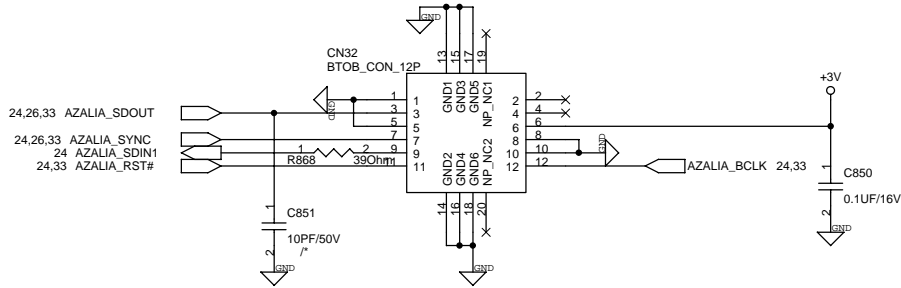


Layout Note: Place near the 8111B
REMOVE FOR RTL8111B

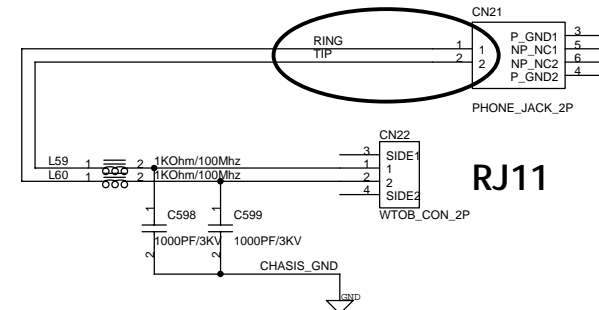


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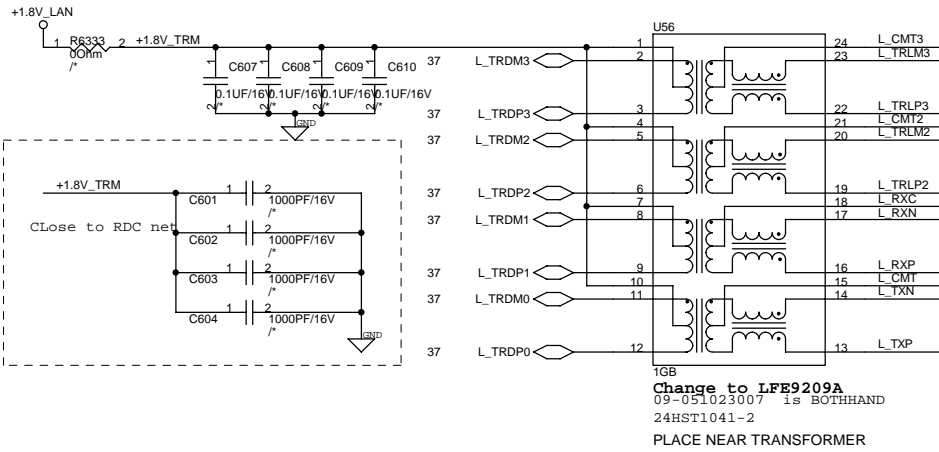
MDC CNT



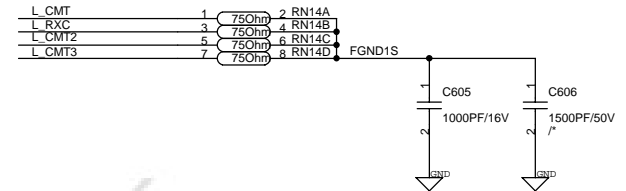
RJ45



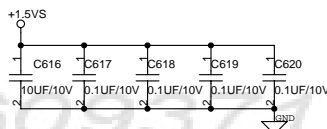
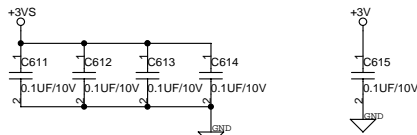
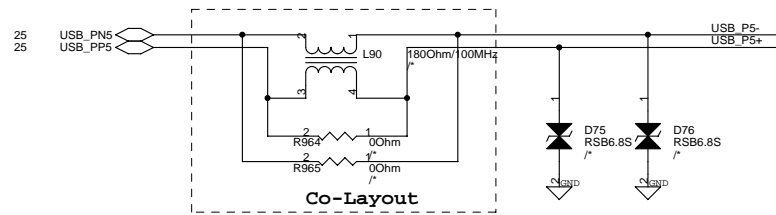
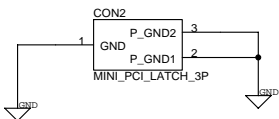
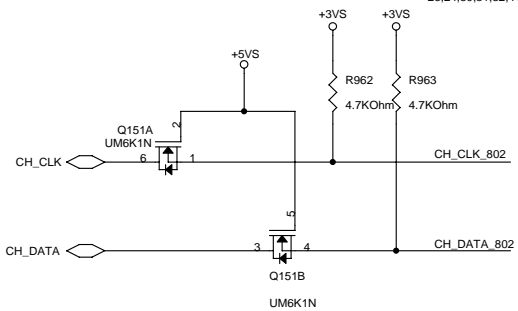
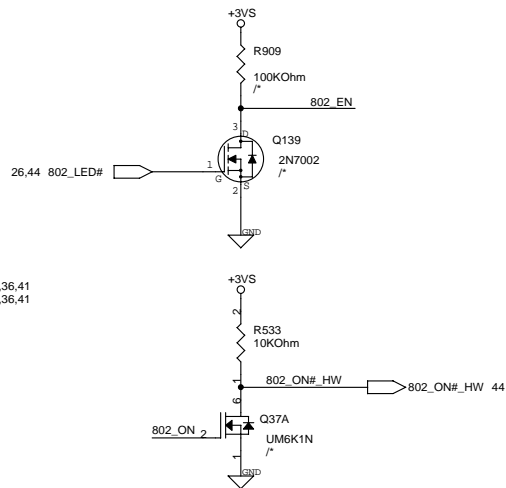
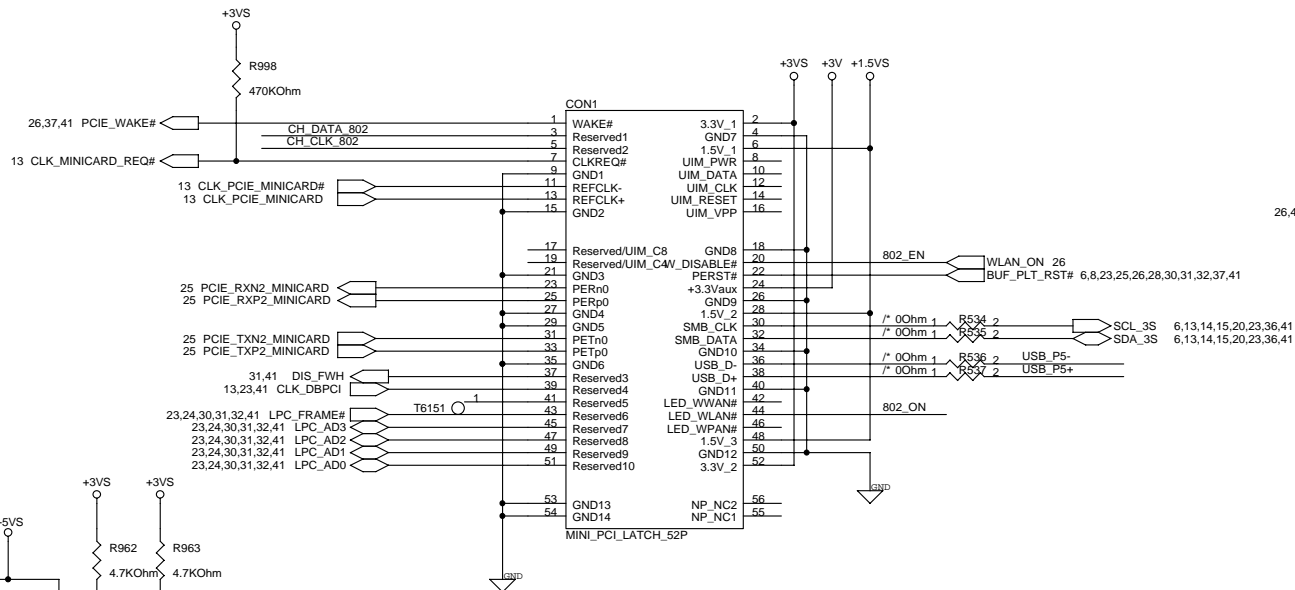
RJ11



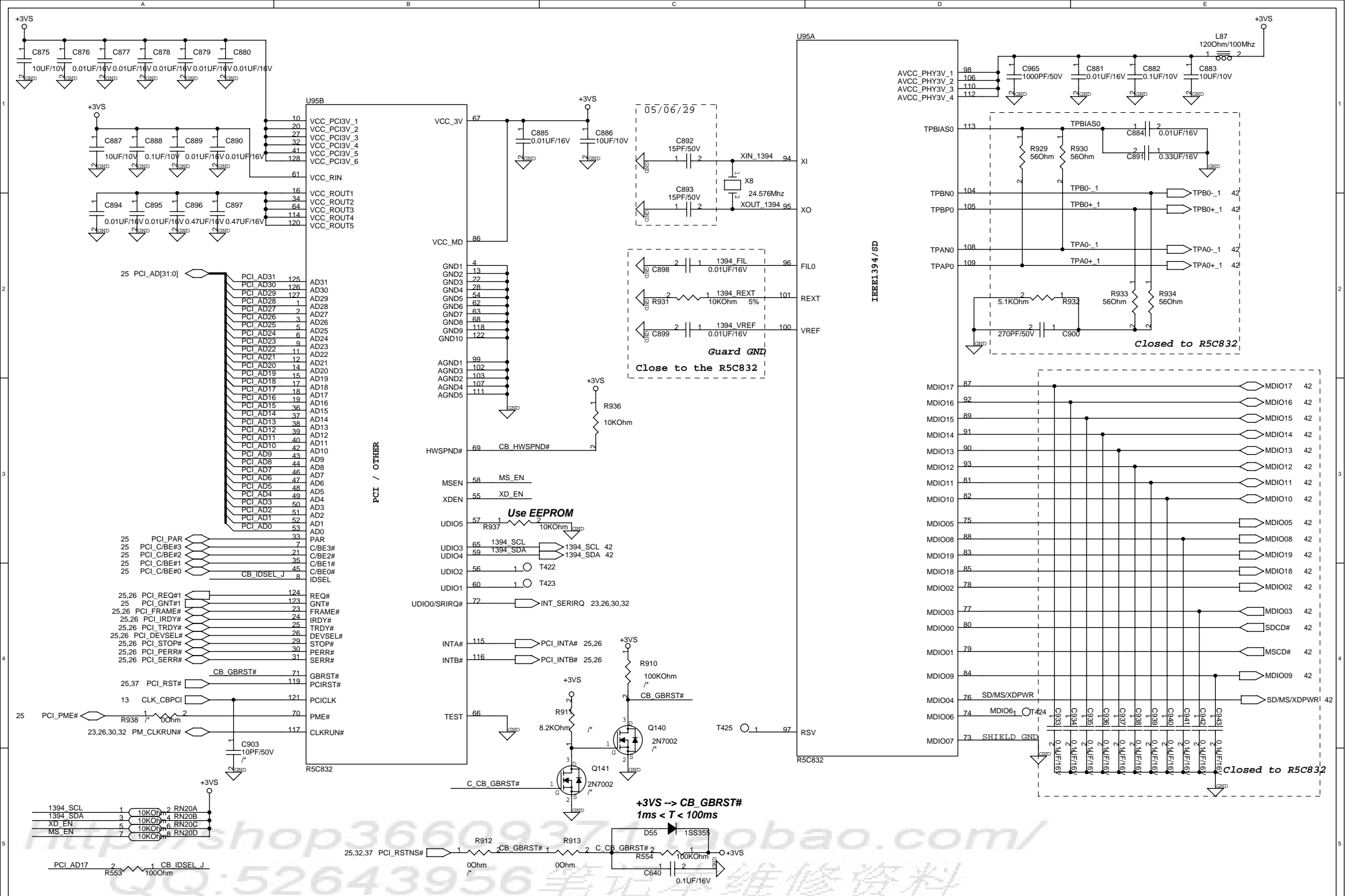
L_TRLP2	LTRLP2	L_TXP	LTXP
L_TRLM2	LTRLM2	L_TXN	LTXN
L_TRLP3	LTRLP3	L_RXP	LRXP
L_TRLM3	LTRLM3	L_RXN	LRXN



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PROJECT: V6J

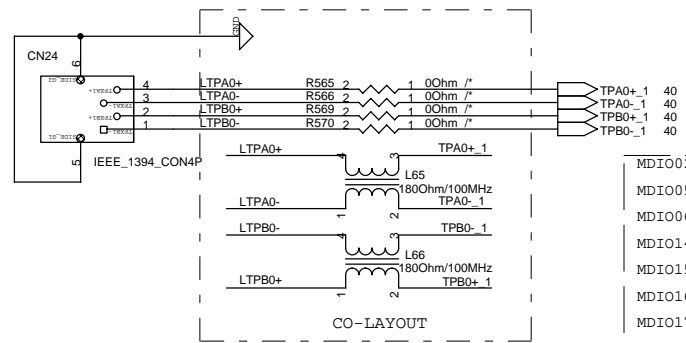
REVISION: 2.0 DATE: Friday, November 25, 2005 SHEET: 40 OF 63

DESCRIPTION: RICOH R5C832

SCHEMATIC FILE NAME: <OrgName> RELEASE DATE:

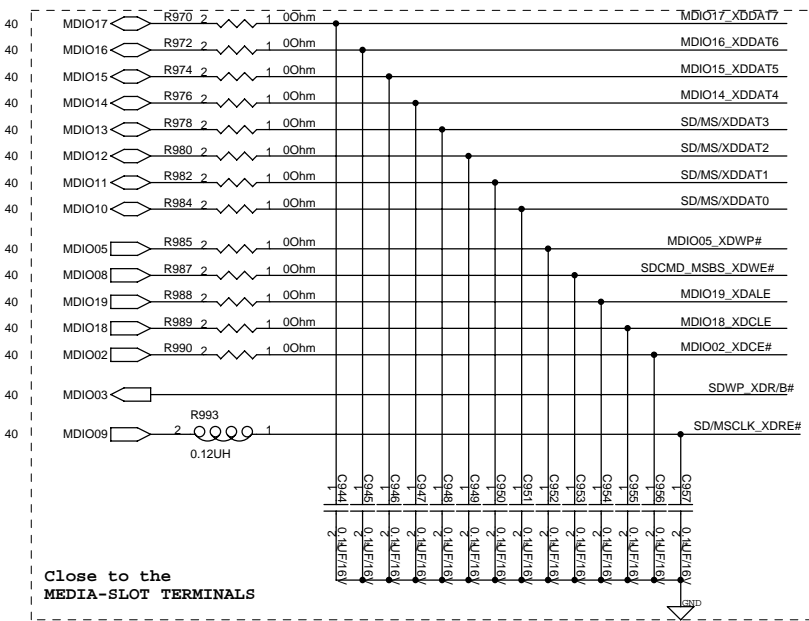
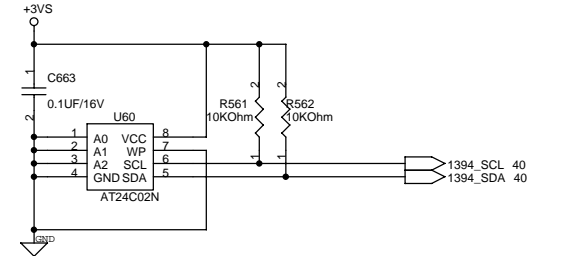
DESIGN ENGINEER: Feng Lin

1394A

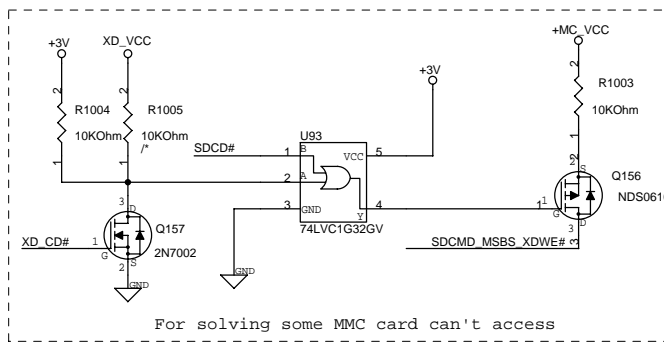


- MDIO02--> xDCE#
- MDIO05--> SD Power Control 1 / xDWP
- MDIO06--> xD/MS/SD LED Control
- MDIO14--> xD Data
- MDIO15--> xD Data
- MDIO16--> xD Data
- MDIO17--> xD Data
- MDIO18--> xD CL#
- MDIO19--> xD ALE

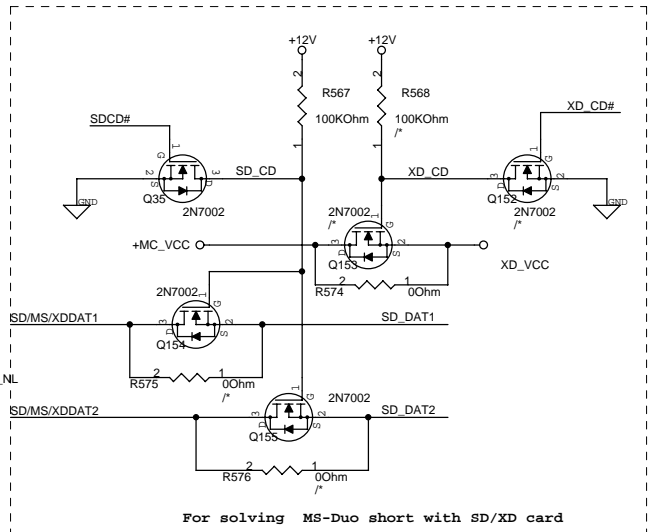
- MDIO01--> MS Card Detect
- MDIO03--> SD Write Protect
- MDIO04--> SD Card Power0 Control/MS Power Control
- MDIO07--> SD External Clock/MS External Clock
- MDIO08--> SD Command/MS Bus State
- MDIO09--> SD Clock/MS Clock
- MDIO10--> SD Data 0/MS Data 0
- MDIO11--> SD Data 1/MS Data 1
- MDIO12--> SD Data 2/MS Data 2
- MDIO13--> SD Data 3/MS Data 3



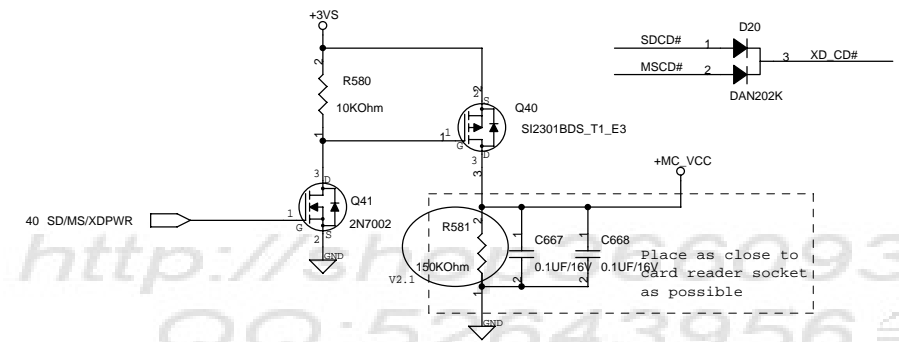
Close to the MEDIA-SLOT TERMINALS



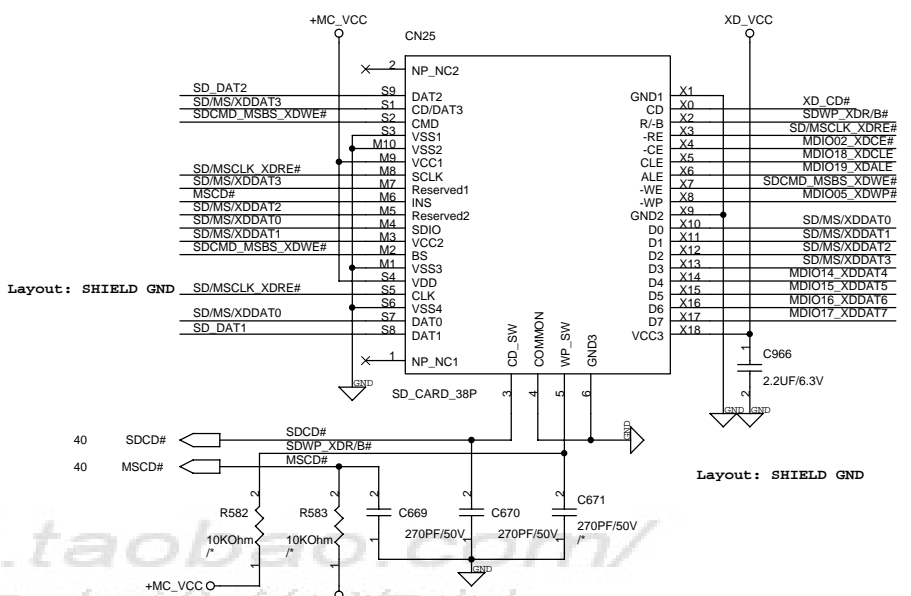
For solving some MMC card can't access



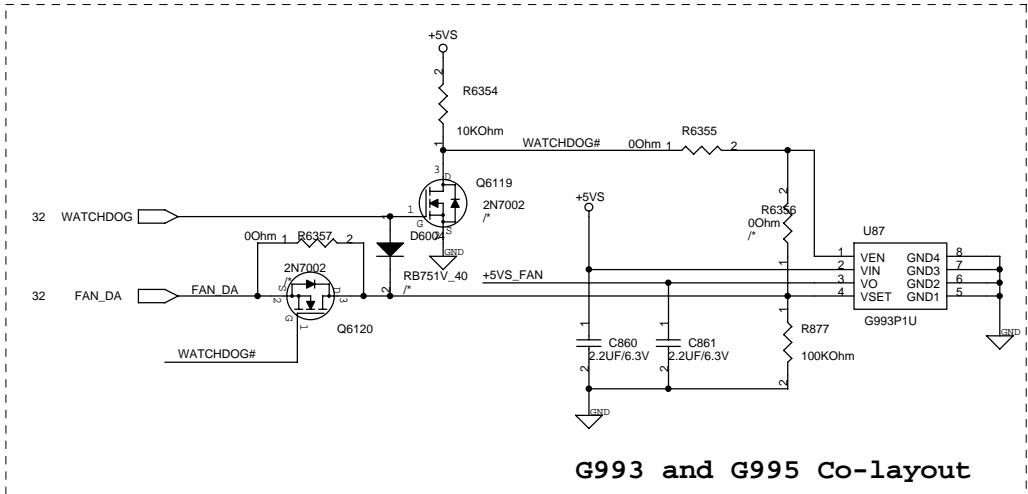
For solving MS-Duo short with SD/XD card



Place as close to card reader socket as possible

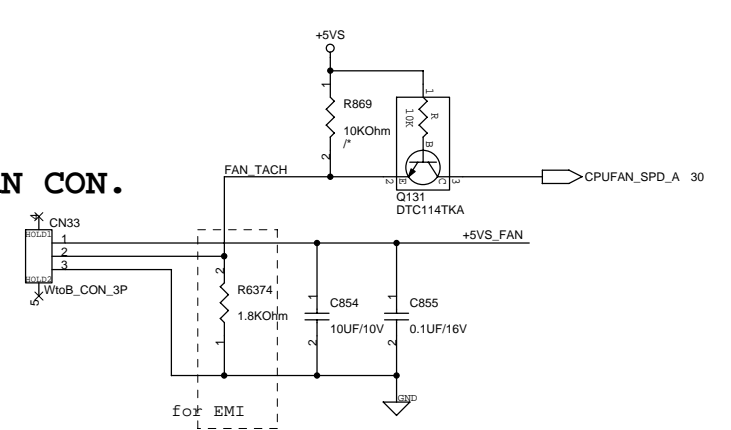


Layout: SHIELD GND

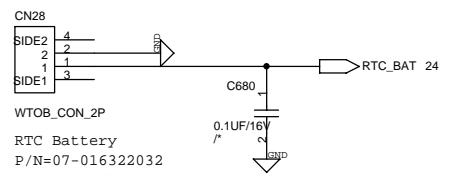


G993 and G995 Co-layout

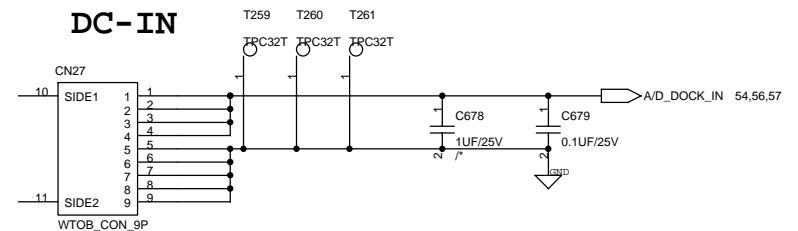
FAN CON.



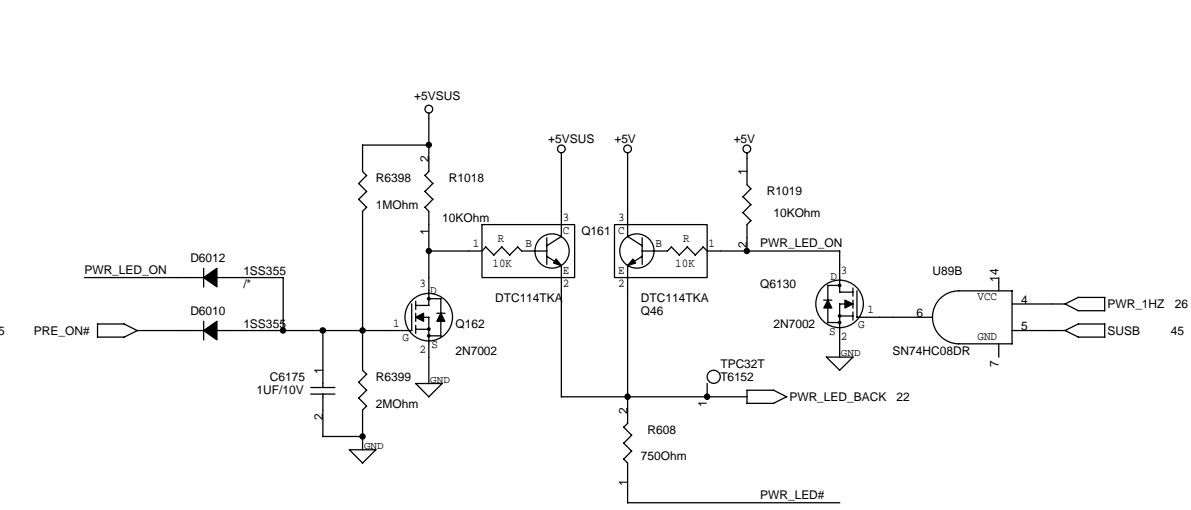
RTC BAT



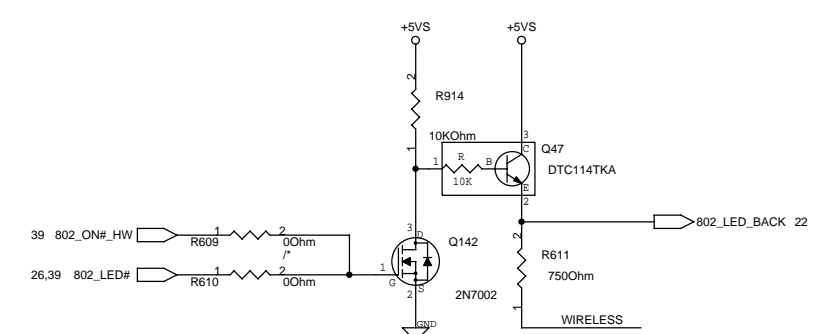
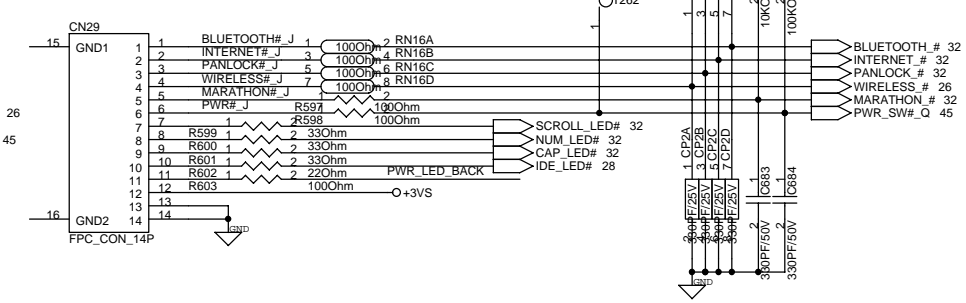
DC-IN



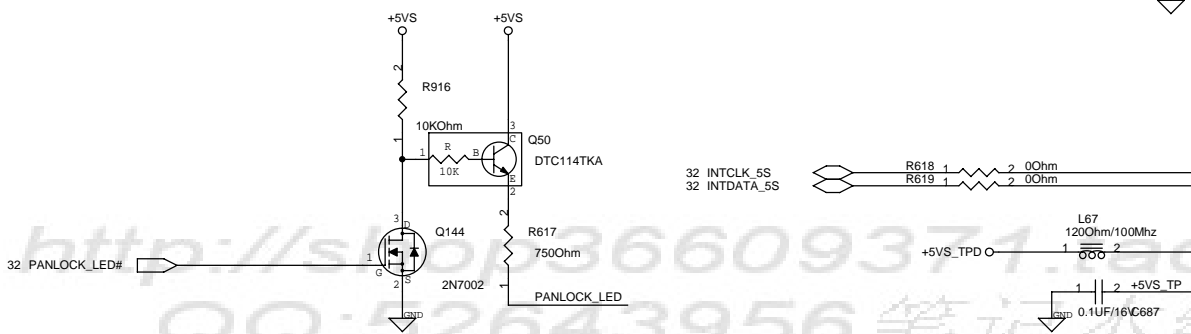
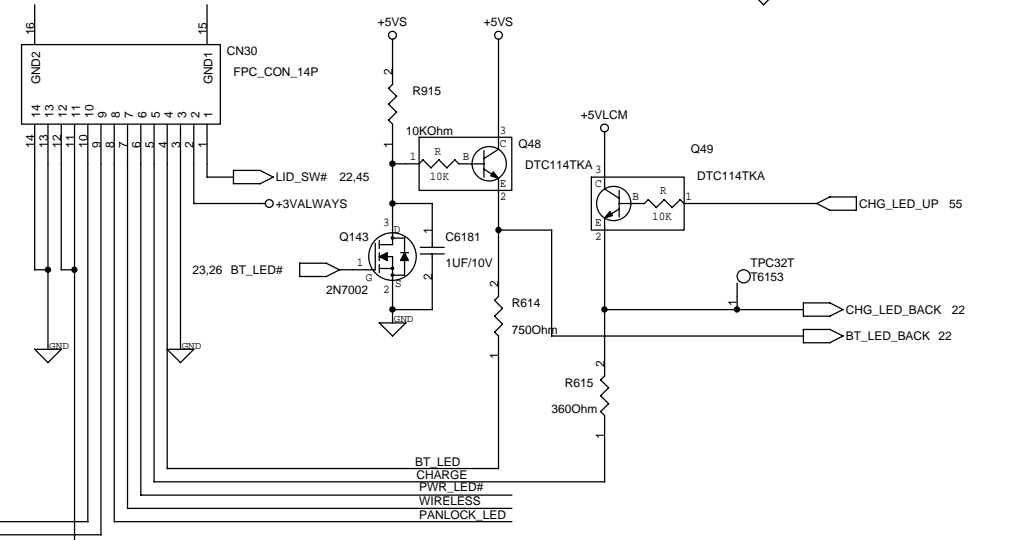
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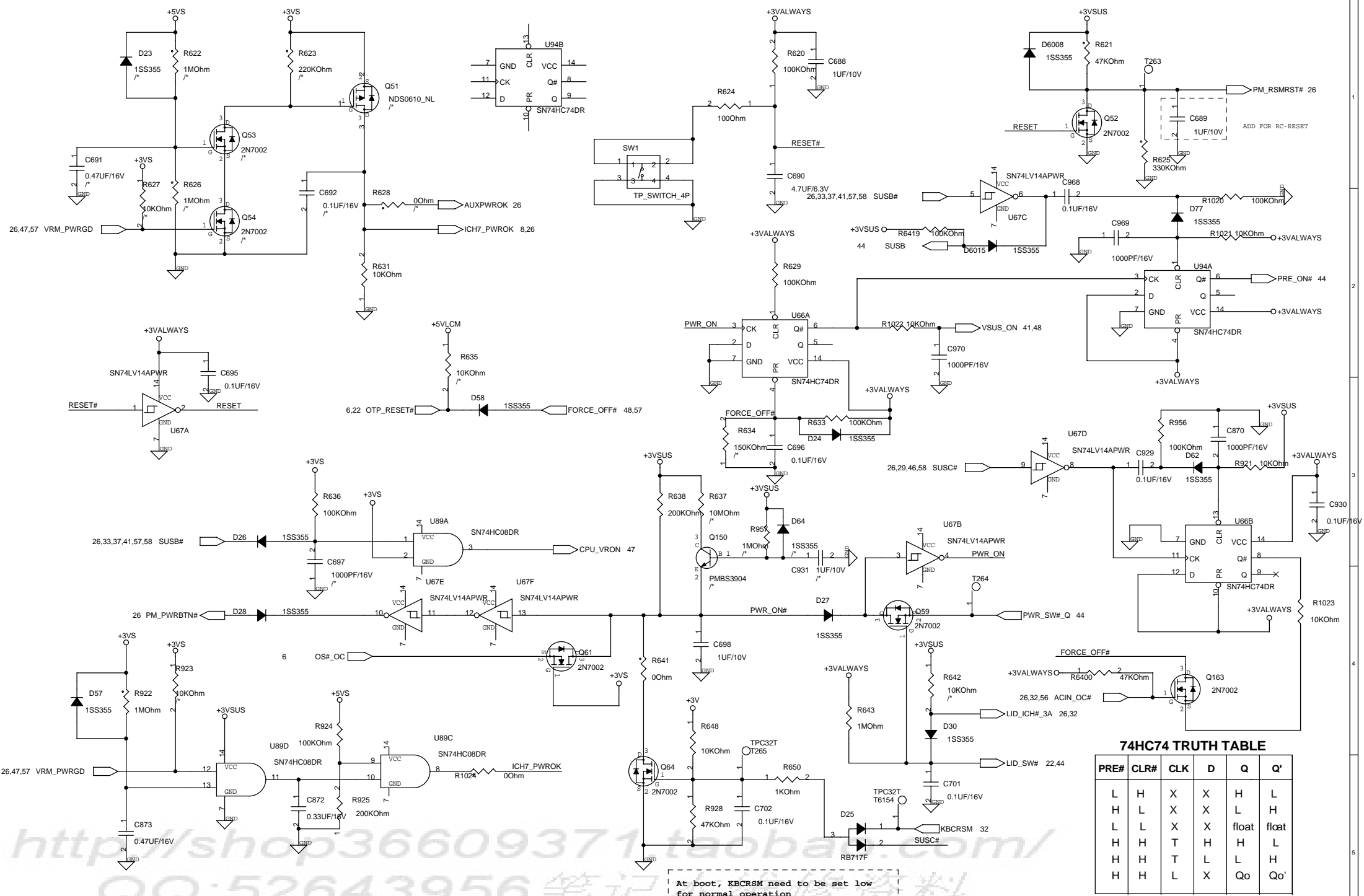
SWITCH FPC CONN



TOUCH PAD CNT



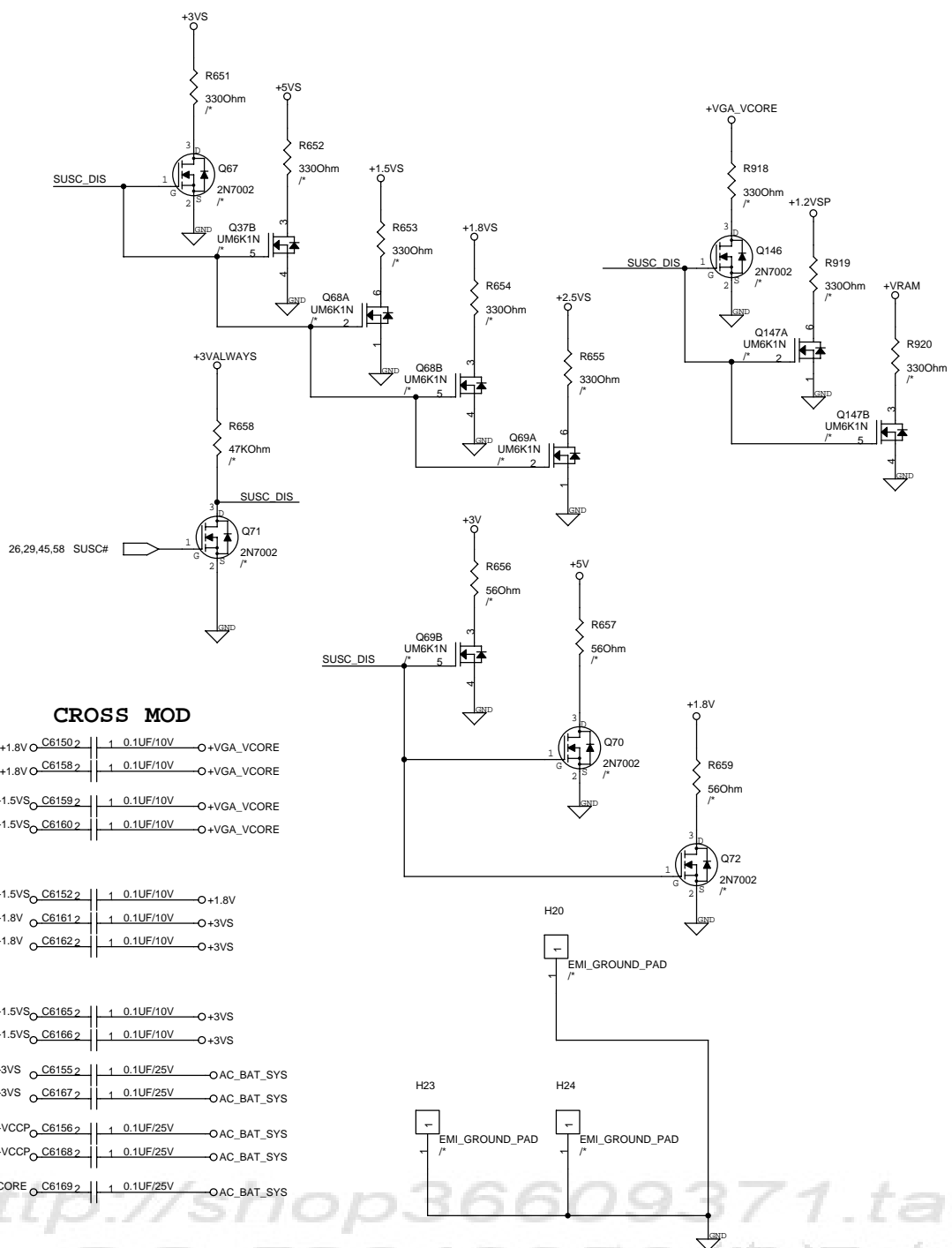
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74HC74 TRUTH TABLE

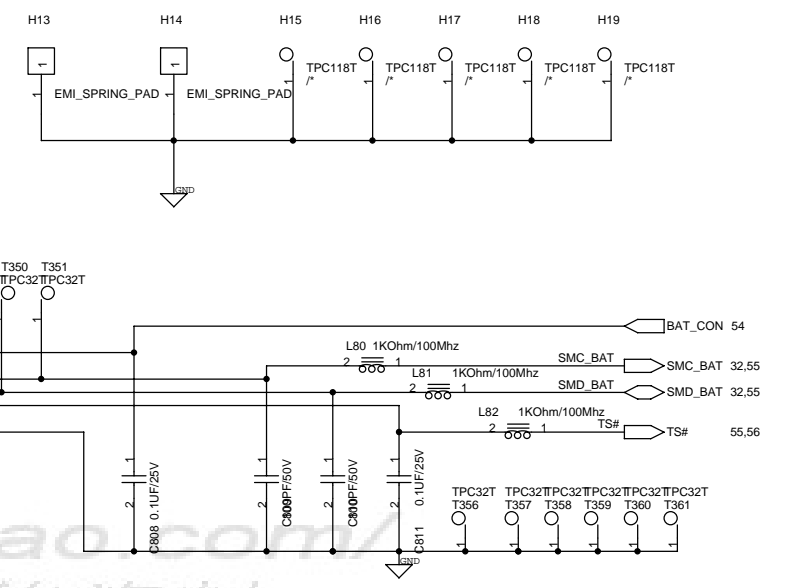
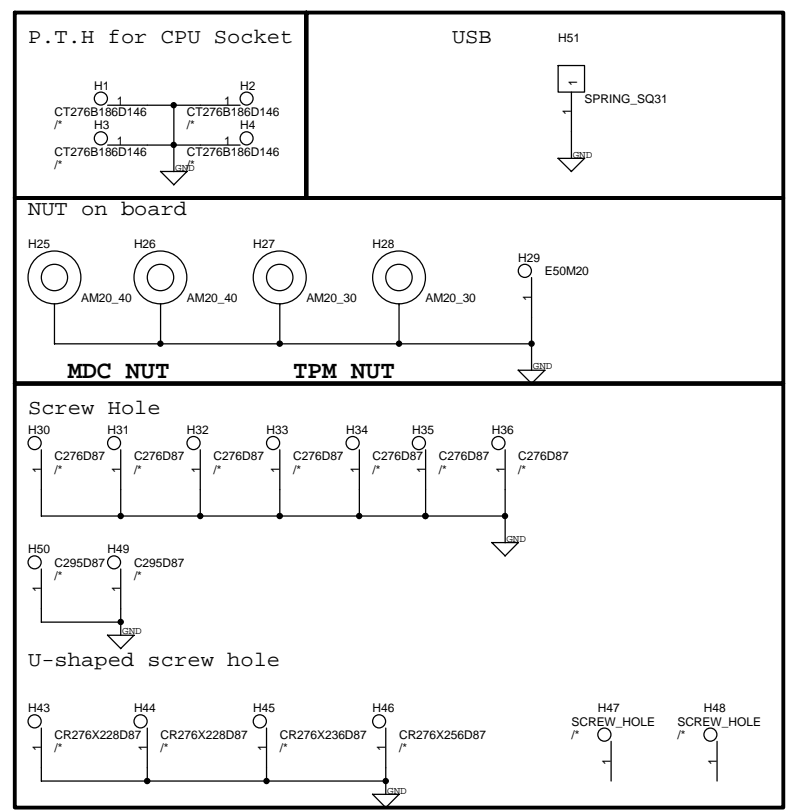
PRE#	CLR#	CLK	D	Q	Q'
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	float	float
H	H	T	H	H	L
H	H	T	L	L	H
H	H	L	X	Qo	Qo'

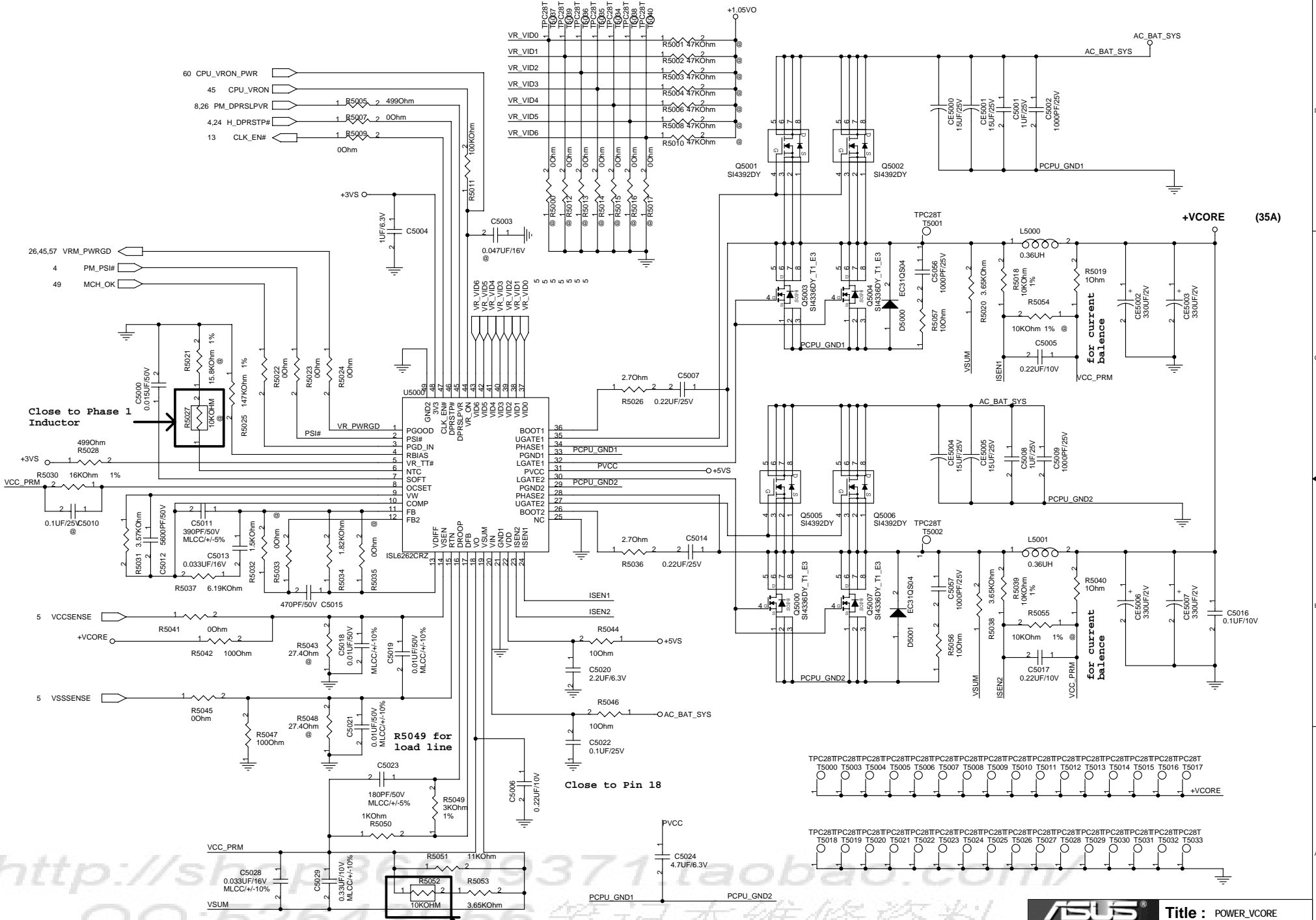
At boot, KBCRSM need to be set low for normal operation



CROSS MOD

+1.8V	C6150 2	1	0.1UF/10V	+VGA_VCORE
+1.8V	C6158 2	1	0.1UF/10V	+VGA_VCORE
+1.5VS	C6159 2	1	0.1UF/10V	+VGA_VCORE
+1.5VS	C6160 2	1	0.1UF/10V	+VGA_VCORE
+1.5VS	C6152 2	1	0.1UF/10V	+1.8V
+1.8V	C6161 2	1	0.1UF/10V	+3VS
+1.8V	C6162 2	1	0.1UF/10V	+3VS
+1.5VS	C6165 2	1	0.1UF/10V	+3VS
+1.5VS	C6166 2	1	0.1UF/10V	+3VS
+3VS	C6155 2	1	0.1UF/25V	AC_BAT_SYS
+3VS	C6167 2	1	0.1UF/25V	AC_BAT_SYS
+VCCP	C6156 2	1	0.1UF/25V	AC_BAT_SYS
+VCCP	C6168 2	1	0.1UF/25V	AC_BAT_SYS
+VCORE	C6169 2	1	0.1UF/25V	AC_BAT_SYS

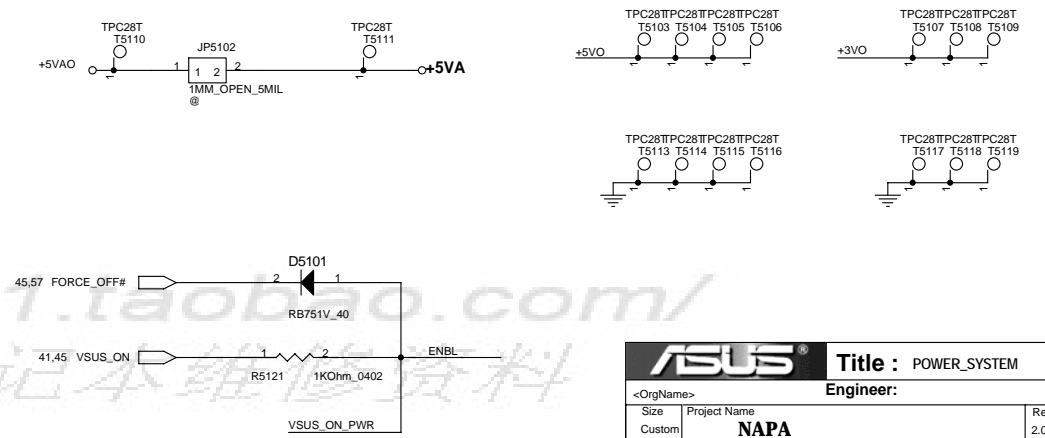
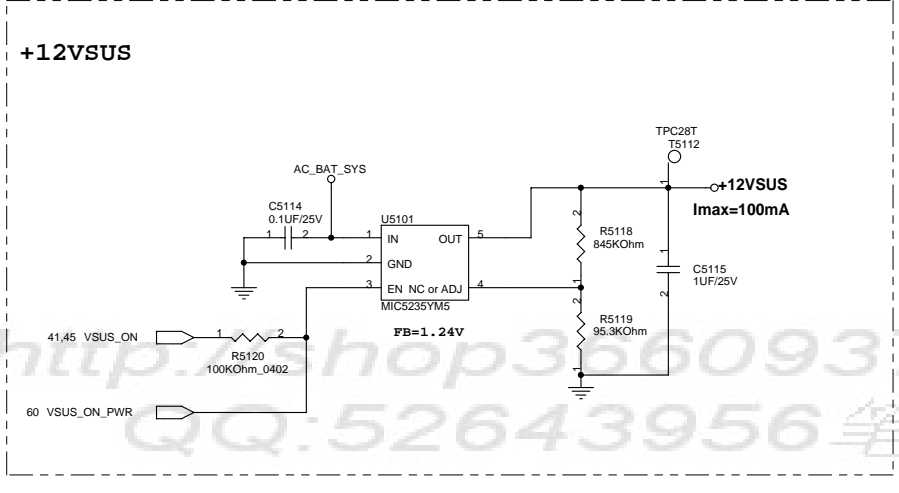
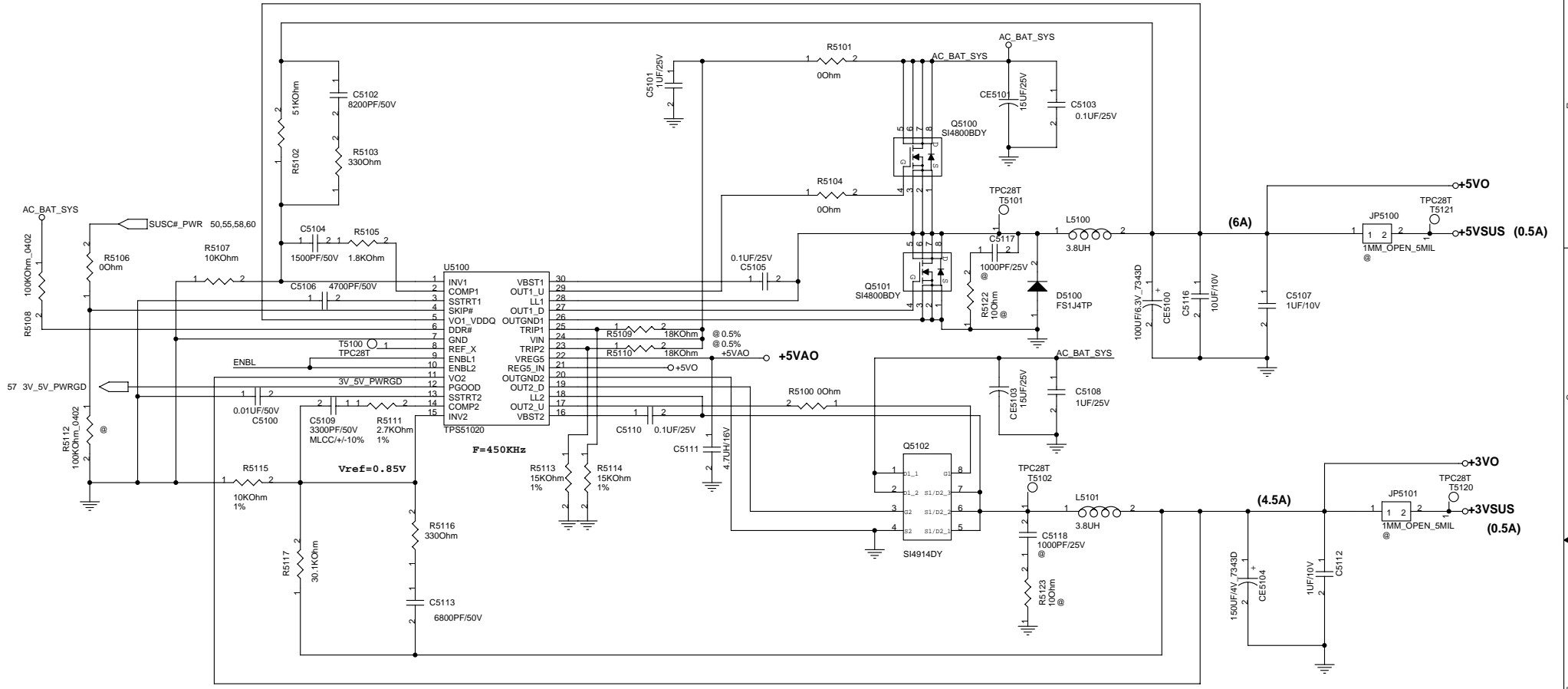


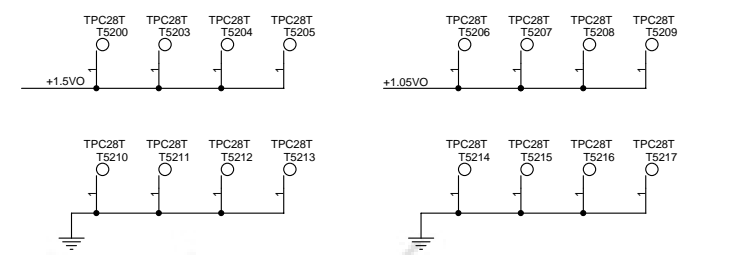
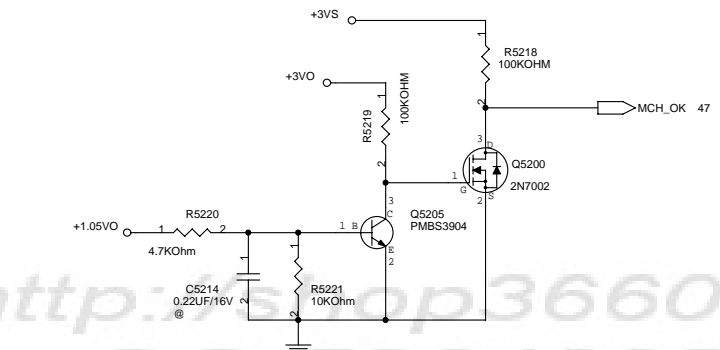
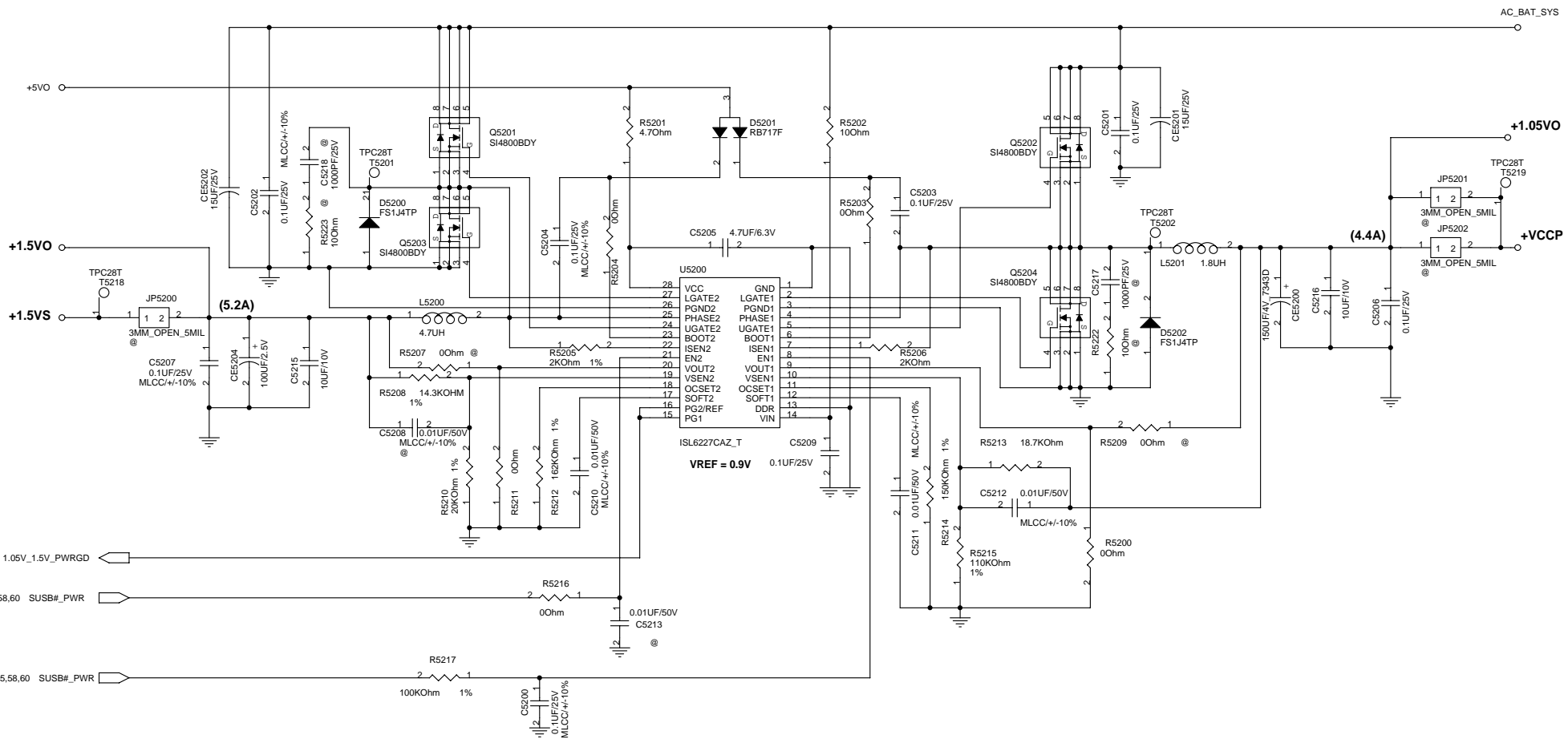


(35A)

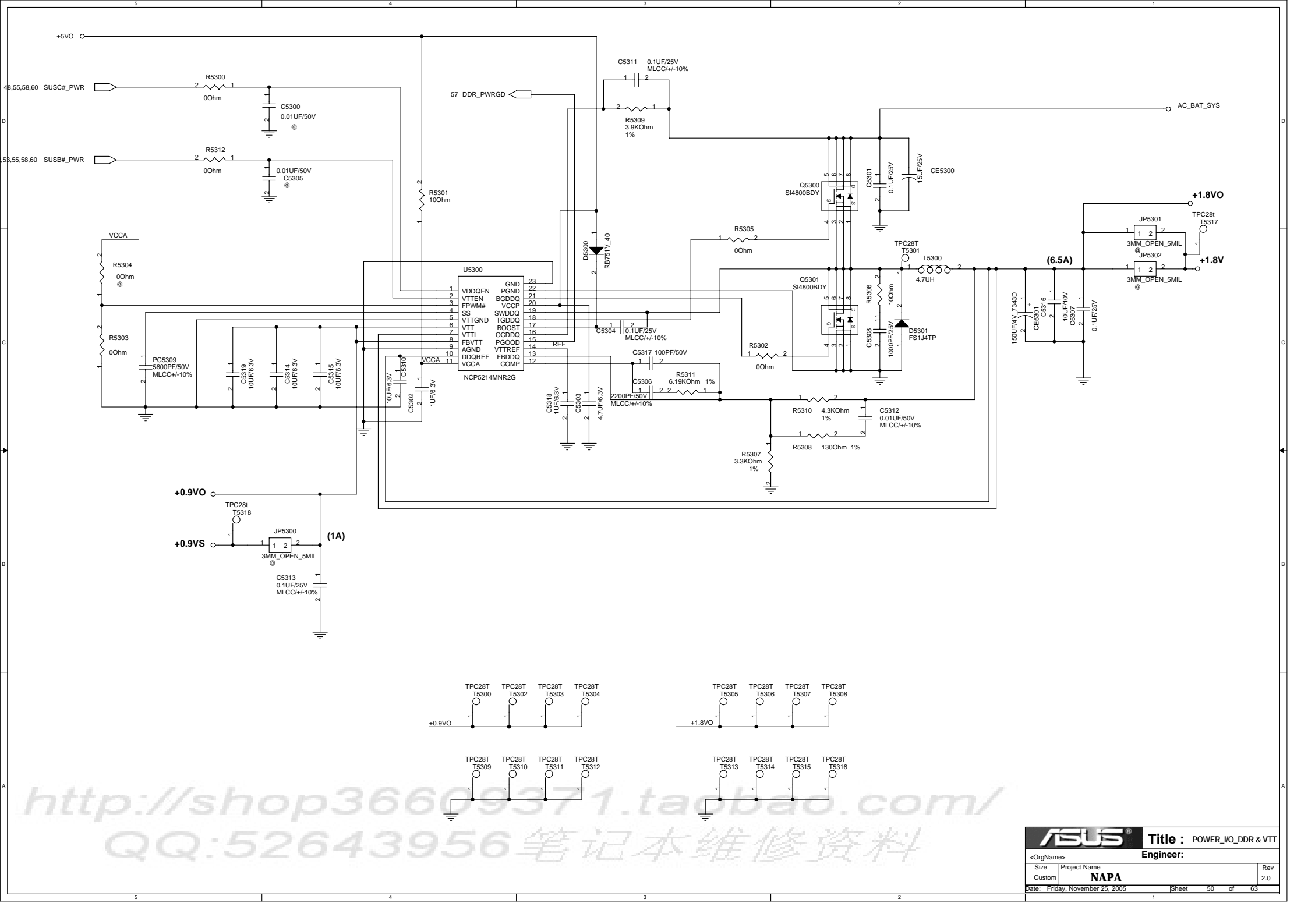
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 QQ:52643356 笔记本维修资料

ASUS		Title : POWER_VCORE	
Engineer:			
<OrgName>	Size	Project Name	Rev
	Custom	NAPA	2.0
Date: Friday, November 25, 2005		Sheet	47 of 63



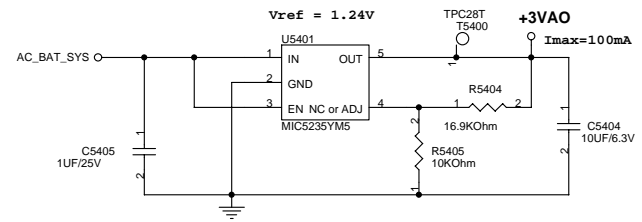
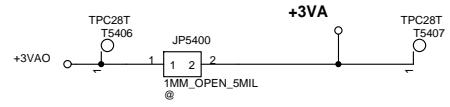


<http://www.taobao.com/>
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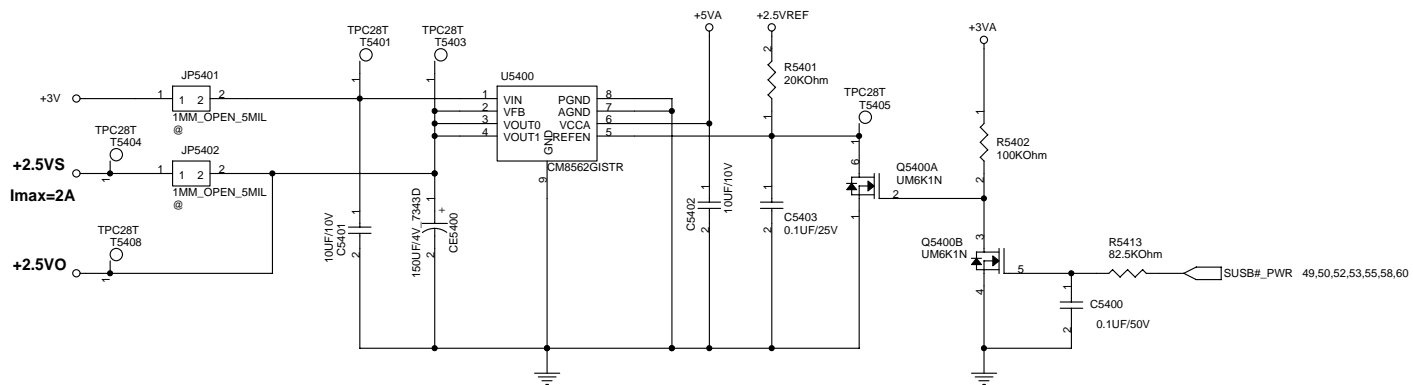


<http://shop36609371.taobao.com/>
 QQ:52643956 笔记本维修资料

+3VAO



+2.5VS

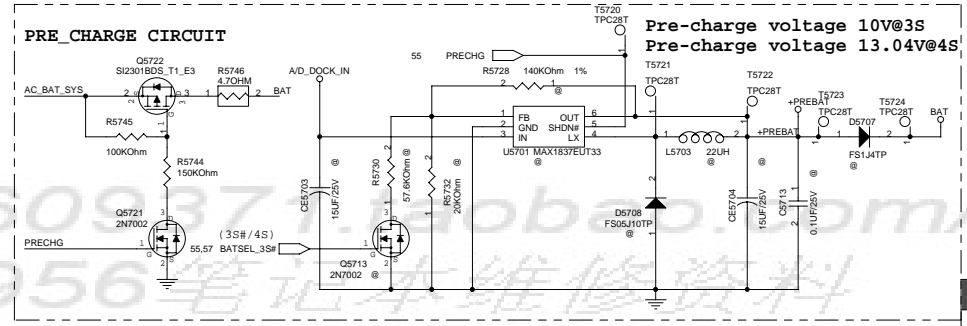
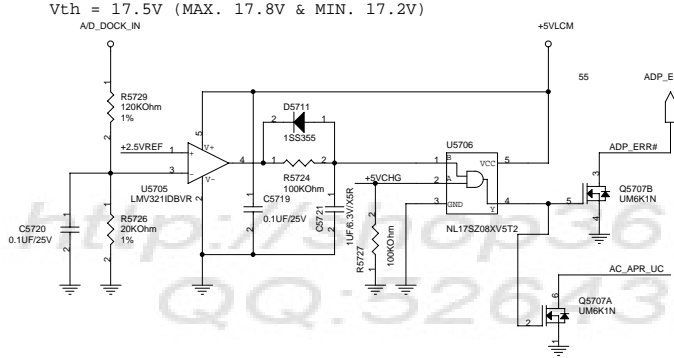
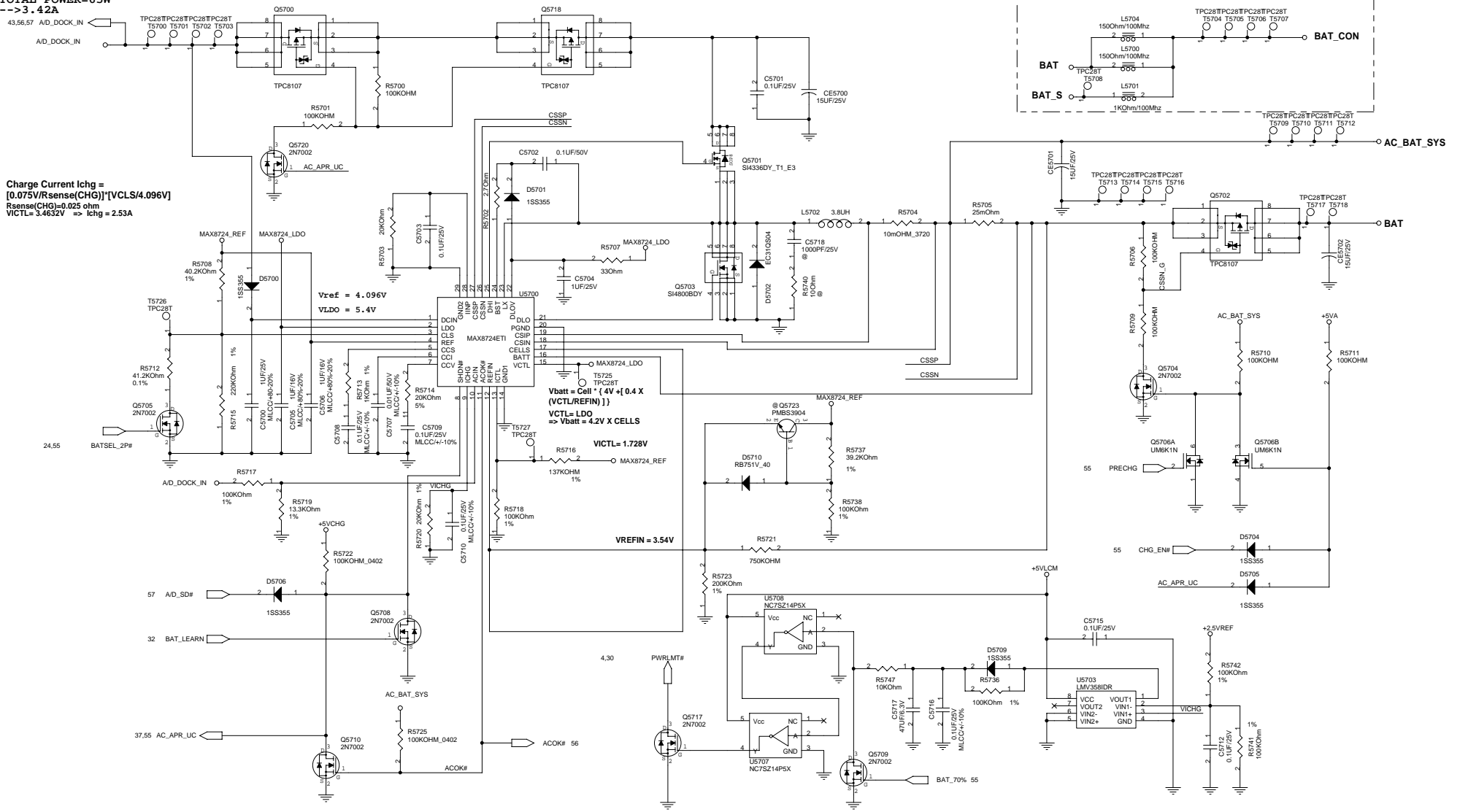


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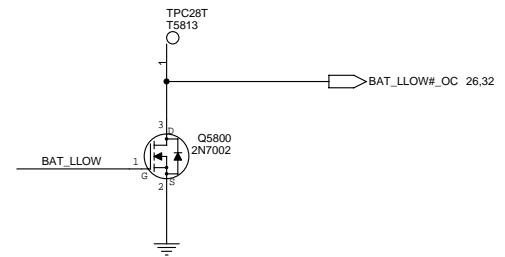
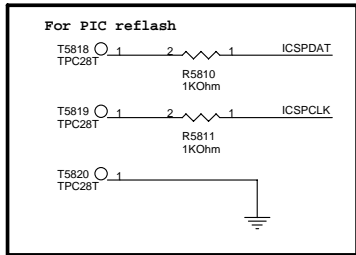
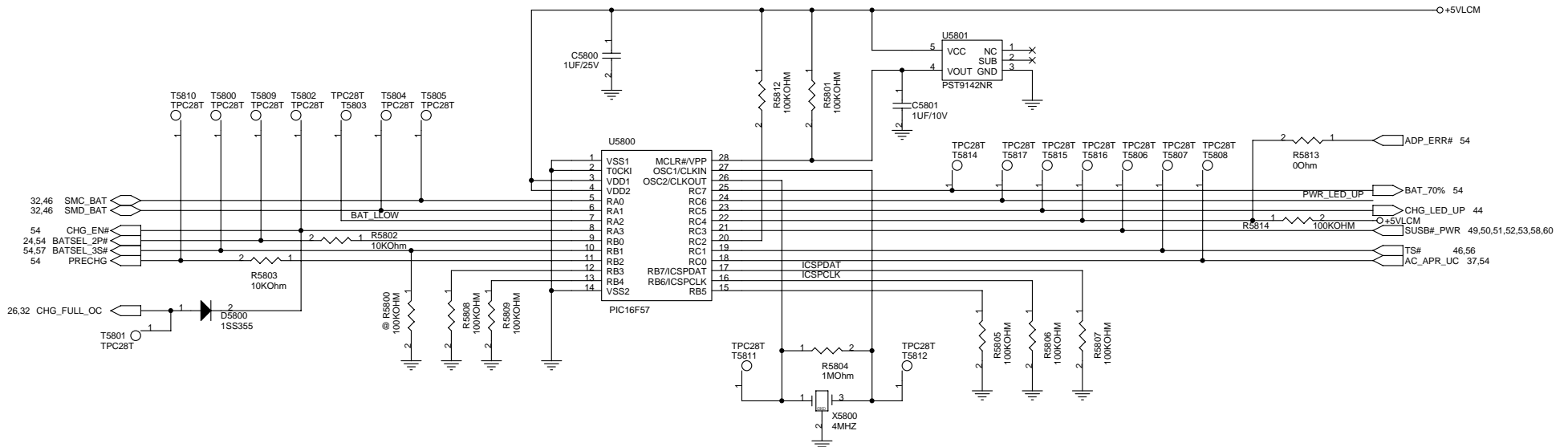
QQ:52643956 笔记本维修资料

TOTAL POWER=65W
 --> 3.42A

Charge Current Ichg =
 $[0.075V/Rsense(CHG)] \cdot [VCLS/4.096V]$
 $Rsense(CHG)=0.025\text{ ohm}$
 $VICTL=3.4632V \Rightarrow Ichg = 2.53A$

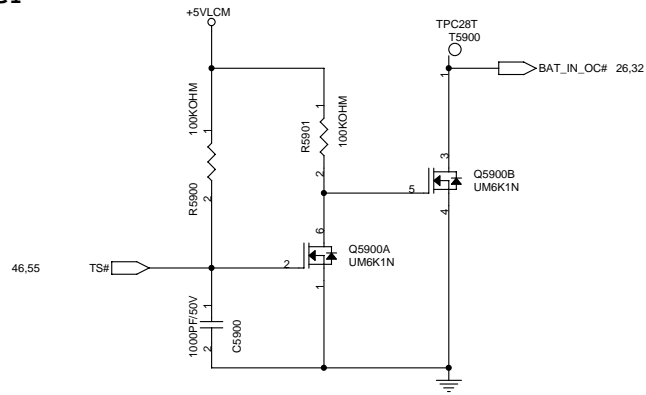


PIC16F57

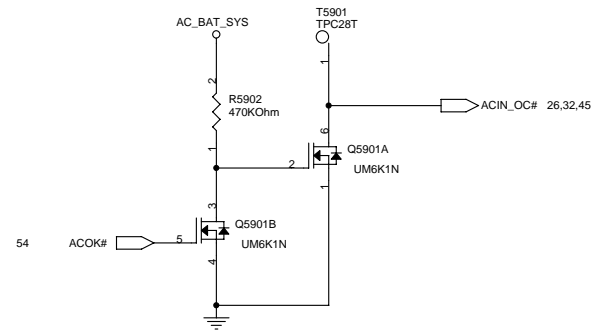


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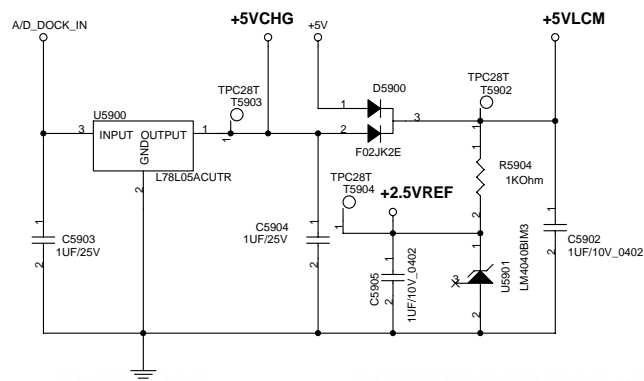
BATTERY IN DETECT



ADAPTER IN DETECT



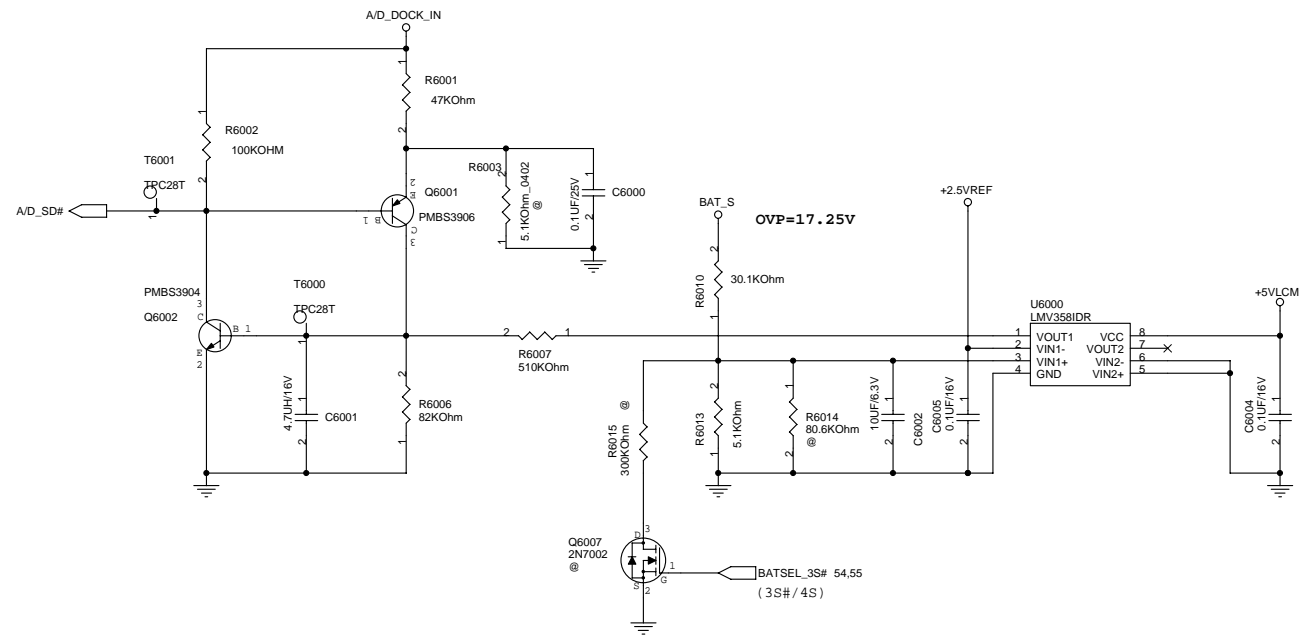
+5VLCM, +5VCHG & +2.5VREF



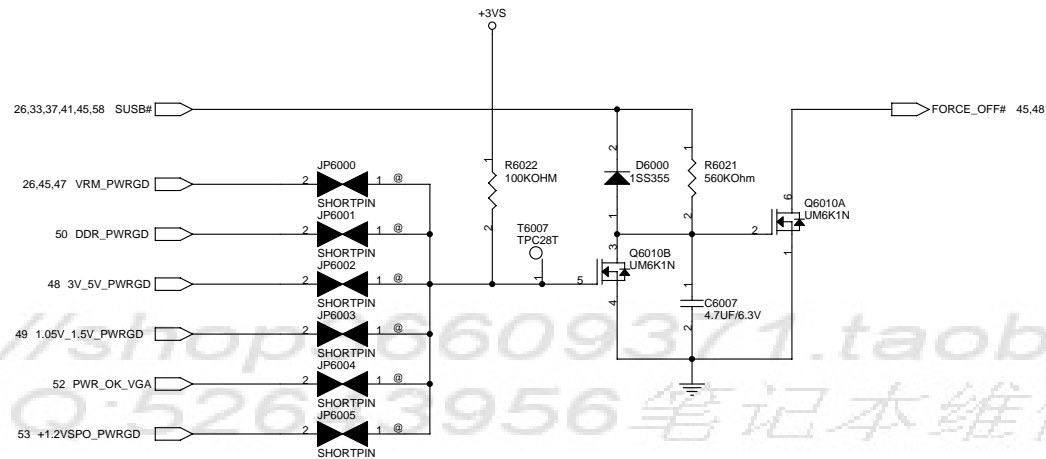
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ASUS		Title : POWER_DETECT	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	NAPA	2.0	
Date: Friday, November 25, 2005		Sheet	56 of 63

BATTERY A/D_SD# (OVP)



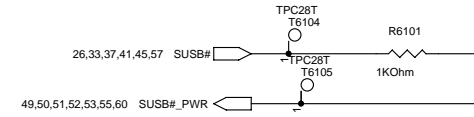
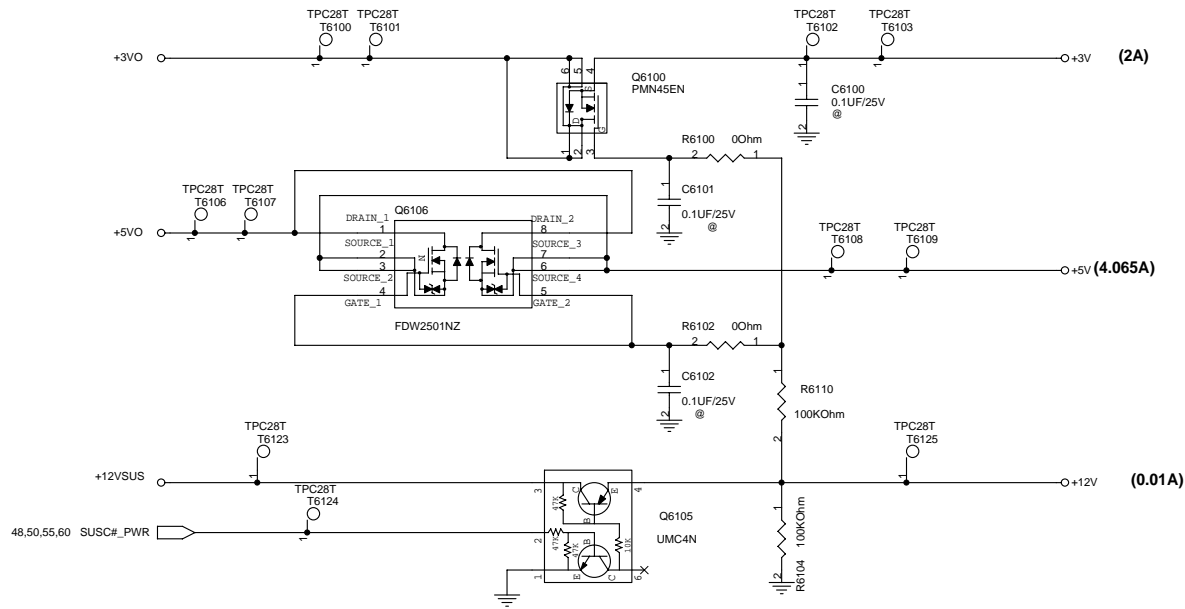
POWER GOOD DETECTOR



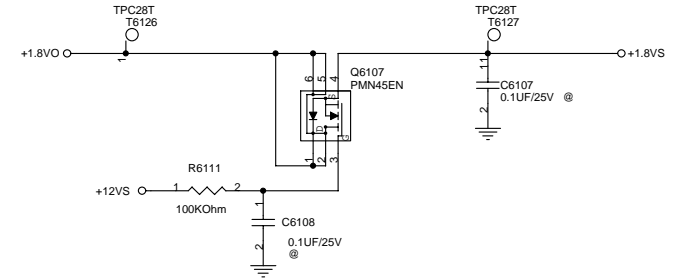
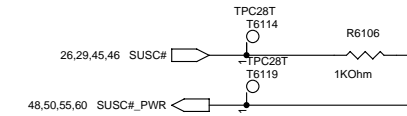
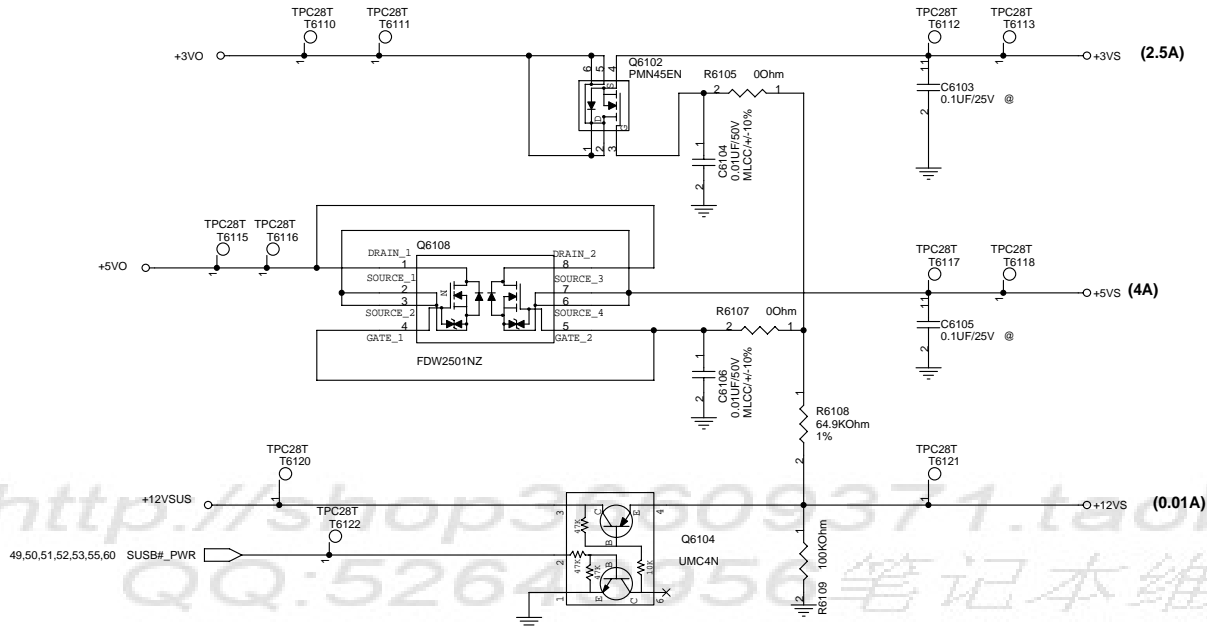
TPC28T	T6003	VRM_PWRGD
TPC28T	T6004	DDR_PWRGD
TPC28T	T6005	3V_5V_PWRGD
TPC28T	T6006	1.05V_1.5V_PWRGD

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 QQ: 5263956 笔记本维修资料

SUSC#_PWR POWER

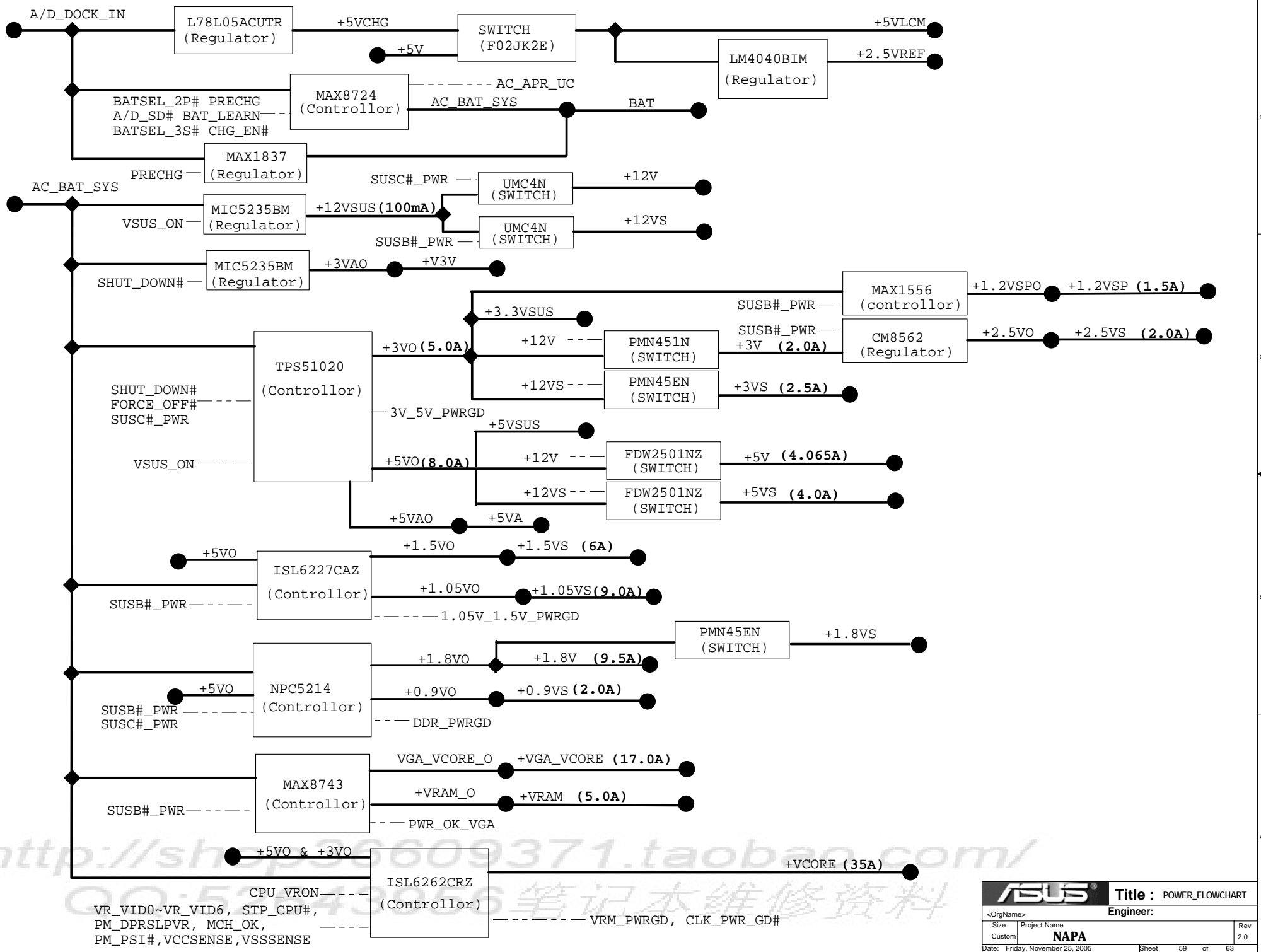


SUSB#_PWR POWER



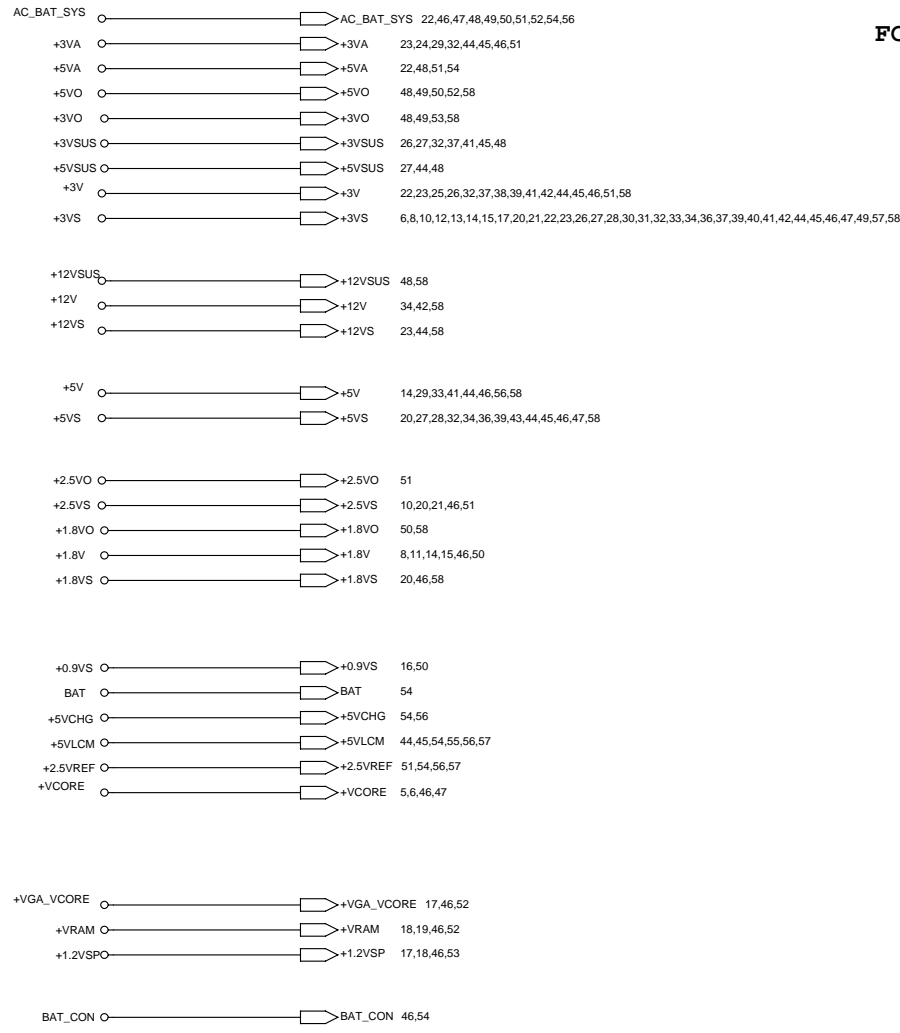
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ASUS		Title : POWER_LOAD SWITCH	
<OrgName>		Engineer:	
Size	Project Name	Rev	
Custom	NAPA	2.0	
Date: Friday, November 25, 2005		Sheet	58 of 63

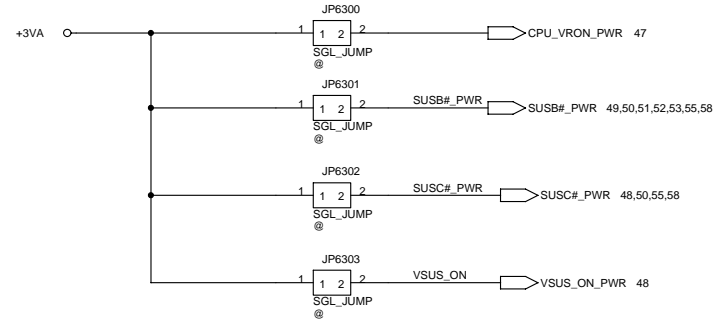


<http://shop3609371.taobao.com/>
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ASUS		Title : POWER_FLOWCHART	
Engineer:			
Size	Project Name	Rev	
Custom	NAPA	2.0	
Date: Friday, November 25, 2005		Sheet	59 of 63



FOR POWER TEST



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Revision History

V1.0 to V1.1

1. D58 change from DAP202 to lss355
2. Panel detection chagne from PID to EDID method.
3. Reserve panel dectection by PID method.
4. Tuning power sequence by power circuitry.
5. TP_MA_RCVEN* net can't connect with TP_MB_RCVEN*, so cut it.
6. CPU address A14 and A15 is swap for booting.
7. Populate R6347 = R6348 =120 Ohm by nVIDIA recommend.
8. Change VGA chip from G72M-V to G72M, so change device ID strapping.
9. CHG_FULLL_OC net has doubled pull-up to +3vs and +3vsus, so remove +3vsus pull-up for leakage.
10. CLK_EN# pull-up to +3vs will has leakage current from cpu vcore controller. so remove it.
11. Lan chip reset signal has leakage current output to system reset signal, so add D6006 to solve it.
12. +1.5VS power trace is too small from source to calistoga IC, so increase trace width.
13. Remove R639 because system has no shutdown signal from POWER.
14. R638 change to 200k and C698 change to 1uF for power on button feeling.
15. CFG18, 16, 15 has wrong connection, correct it.
16. C138=C139=22pF for tunning 14.318MHz crystal freauency.
17. RN15 pin 2 pull-up power change from +3V to +3VS for solving leakage current at S3 state.
18. Change audio circuitry for solving pop noise.
19. Change pci-express decoupling caps from 0.1uF/Y5V to 0.1uF/X5R.
20. Microphone pull-up power source change to OP AMP generate.
21. R287=0 Ohm and R290 remove for G72M need +3VS level input about 27MHz spread spectrum input pin.
22. MAX6649 be used on G72M has wrong connection, so correct it.
23. Populate R574=0 Ohm for XD card work fine.
24. Remove R6360, R6361, R6358, R6359 for JTAG pin pull-up/down on G72M.
25. Populate C563, C566 for improve microphone quality.
26. Add D6008 for PM_RSMRST# discharge quickly.
27. Tunning C141-C146, R128, C490 value base on EVT report about clk signal quality issue.
28. Add ODD disable function support.

V1.1 to V2.0

1. Calistoga CRT disable guide change, so IREF pin connect to power directly.
2. Add circuitry for newcard disable support.
3. R381 change to 1K Ohm for ODD disable support.
4. Reserve newcard type debug card support circuitry.
5. Add mini card type debug card support circuitry.
6. MAX6649 be used on G72M change to MAX6657.
7. Add TPM connector debug card support.
8. The reset signal of lan chip pull-down 10K Ohm.
9. RTCRST# delay time control add diode for quick discharge.
10. Populate R6351, C? for solving led will flash once when system power on.
11. Add usb spring and beas on agnd and dgnd for EMI request.
12. Disable audio jack sense feature.
13. Add Q6130 for 1HZ Flash

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PROJECT: V6J

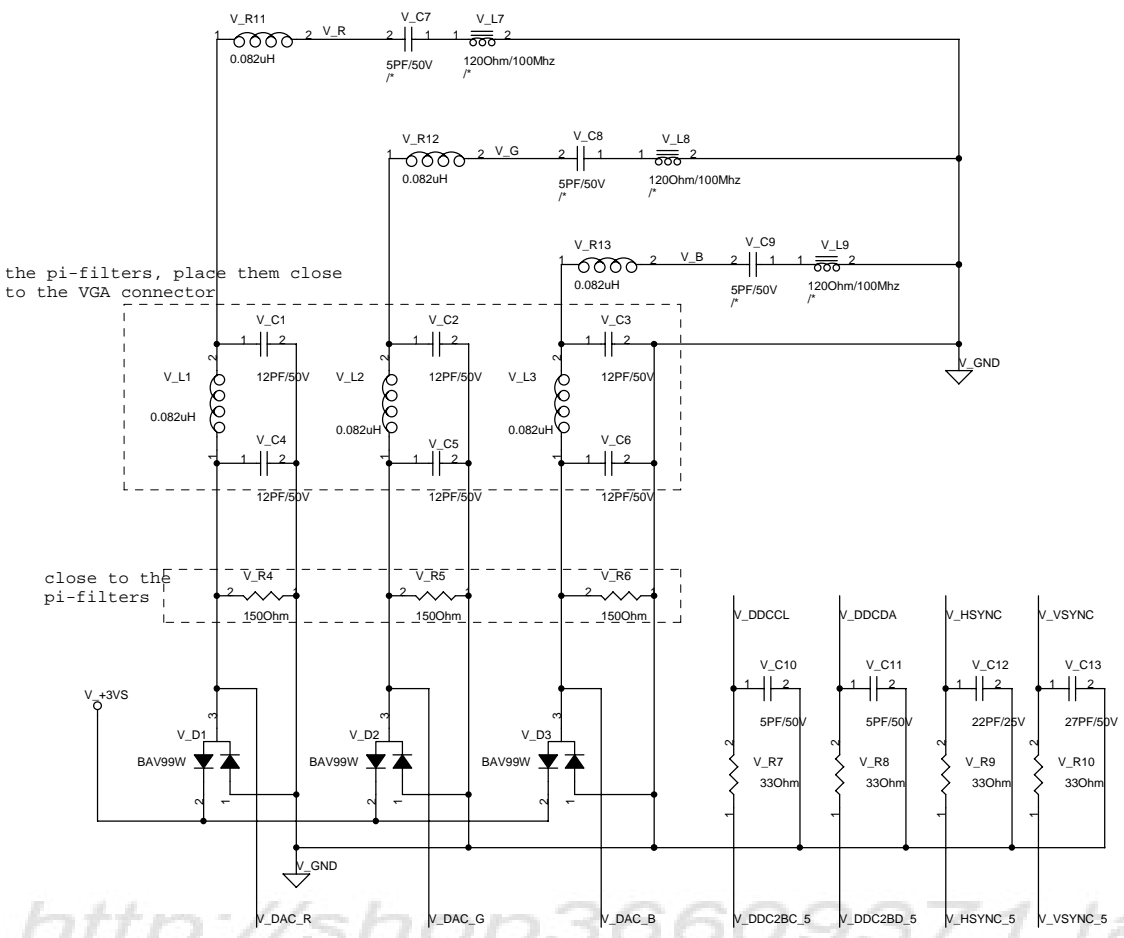
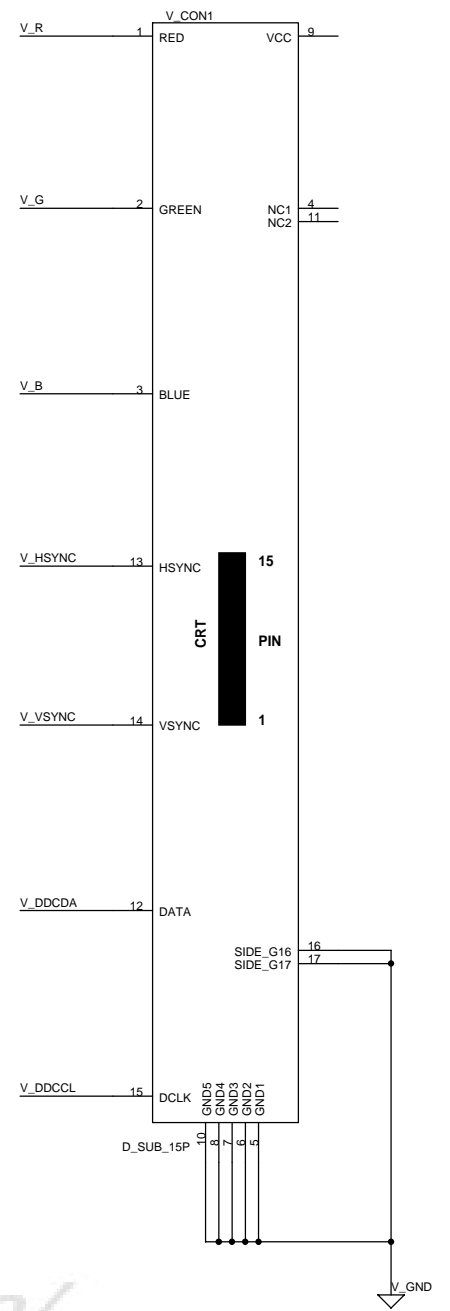
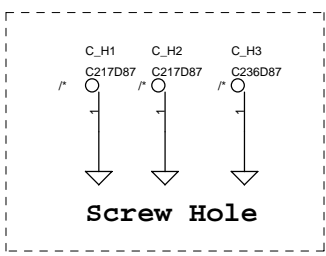
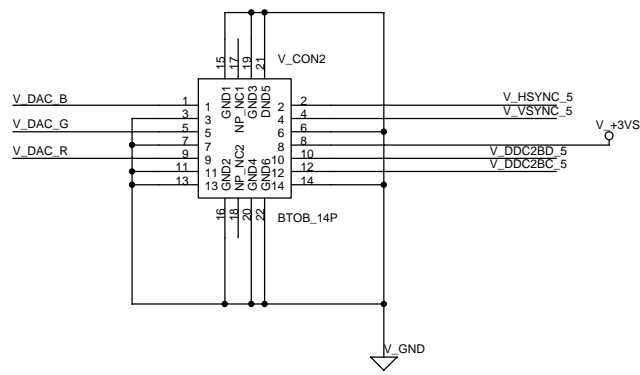
REVISION
2.0

DATE: **Friday, November 25, 2005**
SHEET **61** OF **63**

DESCRIPTION:
Content

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RELEASE DATE :

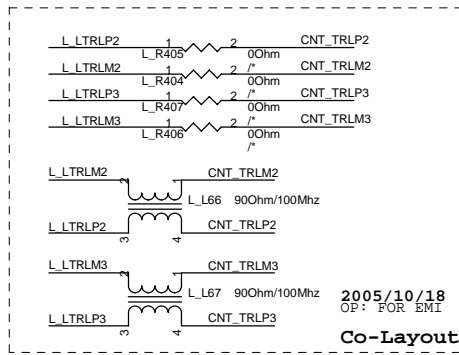
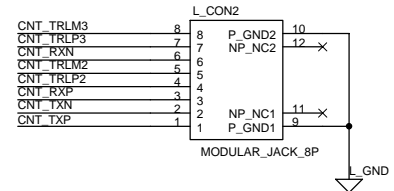
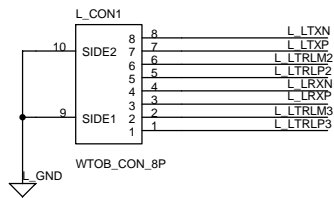
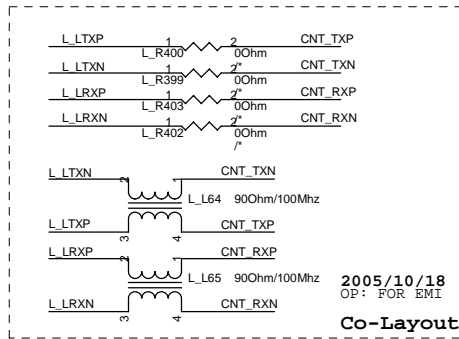
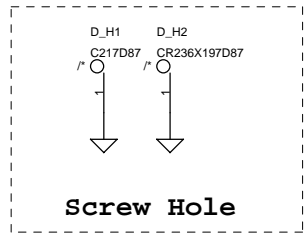
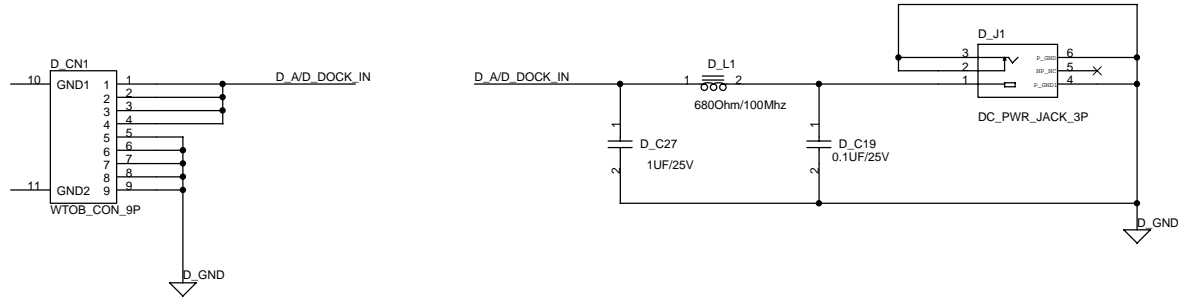
DESIGN ENGINEER :
Feng Lin



the pi-filters, place them close to the VGA connector

close to the pi-filters

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