

Compal Confidential

Model Name : V5WE2/T2 (EA/EG)

File Name : LA-9532P

Compal Confidential

EA50 UMA M/B Schematics Document

Intel Shark Bay ULT (Hasswell + Lynx PointLP)

2013-04-18

REV:1.0

Part Number	Description
DAZ0VR00200 V5WE2_PCB	PCB V5WE2 LA-9532P LS-9531P/9532P/9533P

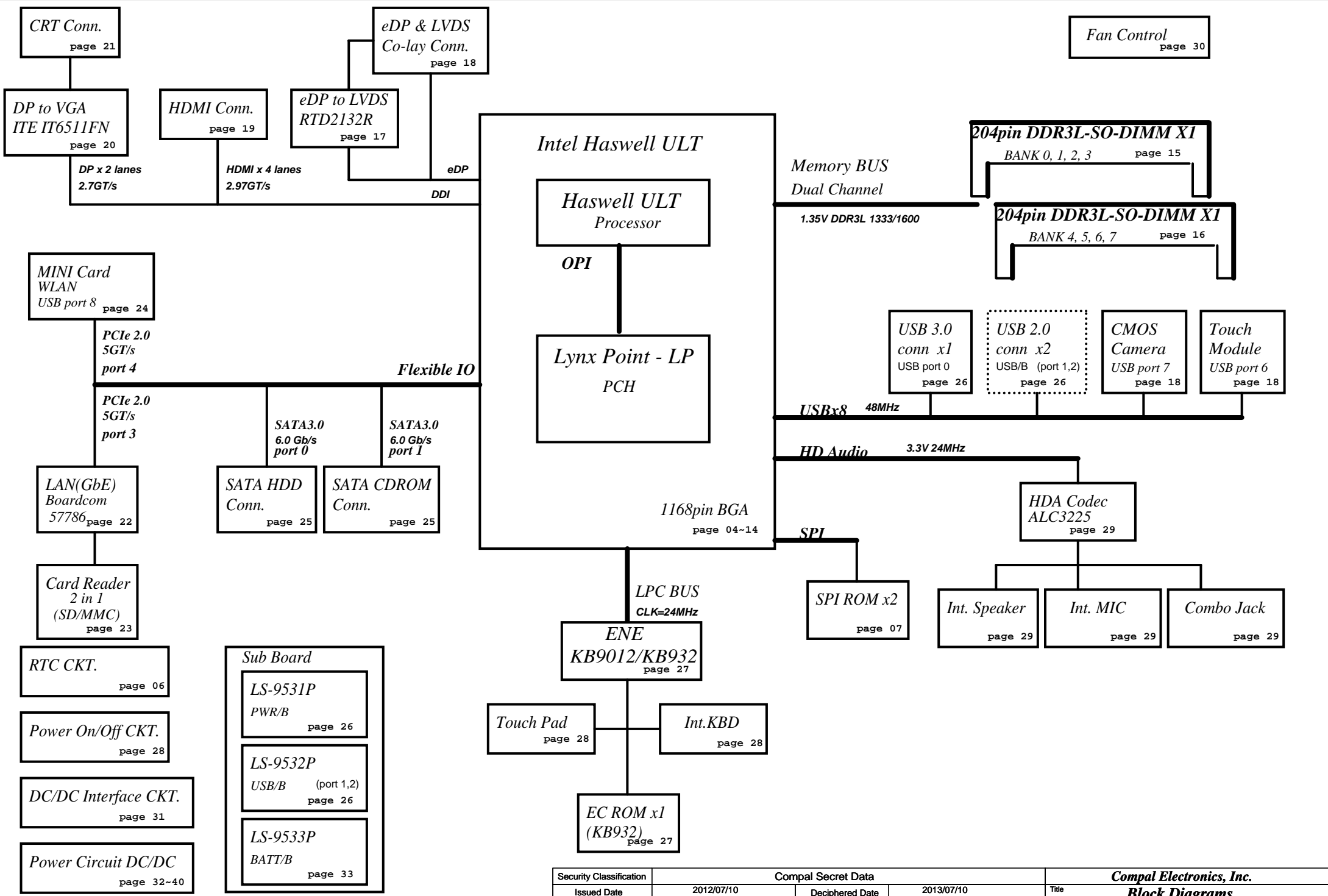
ZZZ1



HDMI ROYALTY
ROYALTY HDMI W/LOGO+HDCP
RQ0000003HM
45@

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
BATT+	Battery power supply (12.6V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+0.675VS	+0.675VSP to +0.675VS switched power rail for DDR terminator	ON	OFF	OFF
+1.35V	+1.35VP to +1.35V power rail for DDRIII.L	ON	ON	OFF
+1.5VS	+1.5V to +1.5VS switched power rail	ON	OFF	OFF
+1.8VS	+3VS to 1.8V switched power rail to CPU	ON	OFF	OFF
+3VALW	+3VALW always on power rail	ON	ON	ON*
+3VLP	B+ to +3VLP power rail for suspend power	ON	ON	ON
+3VS	+3VALW to +3VS power rail	ON	OFF	OFF
+5VALW	+5VALWP to +5VALW power rail	ON	ON	ON*
+5VS	+5VALW to +5VS switched power rail	ON	OFF	OFF
+VSB	+VSBP to +VSB always on power rail for sequence control	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON
+1.05VS_VTT	+1.05VSP to +1.05VS_VTT switched power rail for cpu	ON	OFF	OFF

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

EC SM Bus1 address

EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011X b	On Board Thermal Sensor	1001_101xb

PCH SM Bus address

Device	Address
ChannelA DIMM0 A0	1010 000X JDIMM1(SPD)

BOM config

PCB P/N	DA60000XR00 : PCB 0VR LA-9532P REV0 M/B
EVT BOM config	9012@ ; AMIC@ ; CHR@ ; BL@ ; EMC@ ; AOAC@
DVT BOM config	9012@ ; BL@ ; EMC@ ; EDP@ (L01~L04) 9012@ ; BL@ ; EMC@ ; TL@ (L05)
PVT BOM config	9012@ ; EMC@ ; EDP@ ; 1ROM@ ; IOAC@
PreMP BOM config	9012@ ; EMC@ ; EDP@ ; 1ROM@ ; IOAC@

11/1 Del XDP@

43 level BOM table

43 Level	Description
4319LWBOL01	SMT MB A9532 V5WE2 UMA I7 QDA7 HDMI
4319LWBOL02	SMT MB A9532 V5WE2 UMA I5 QDJB HDMI
4319LWBOL03	SMT MB A9532 V5WE2 UMA I5 QDJ7 HDMI
4319LWBOL04	SMT MB A9532 V5WE2 UMA I5 QDJ9 HDMI
4319LWBOL05	SMT MB A9532 V5WE2 UMA I5 QDJB LVDS HDMI
4319LWBOL06	SMT MB A9532 V5WE2 UMA WO/CPU HDMI
4319LWBOL07	SMT MB A9532 V5WE2 UMA I5 QEA4 HDMI
4319LWBOL08	SMT MB A9532 V5WE2 UMA I5-4200 HDMI
4319LWBOL09	SMT MB A9532 V5WE2 UMA I3-4010 HDMI
4319LWBOL10	SMT MB A9532 V5WE2 UMA I5-4250 HDMI
4319LWBOL21	SMT MB A9532 V5WC2 UMA I5-4200 HDMI
4319LWBOL22	SMT MB A9532 V5WC2 UMA I3-4010 HDMI

STATE / SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rc/Re	100K +/- 5%			
Board ID	Rb / Rd / Rf	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	1.0
5	
6	
7	

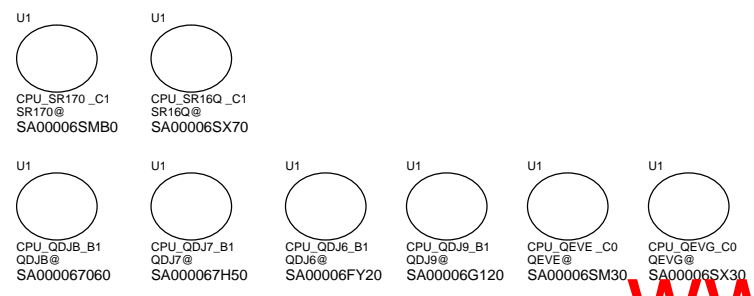
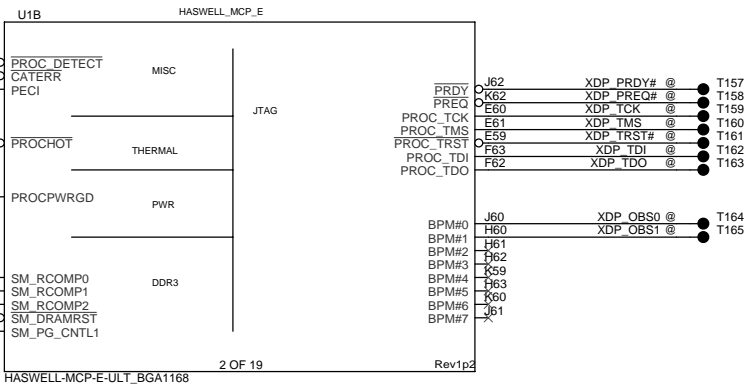
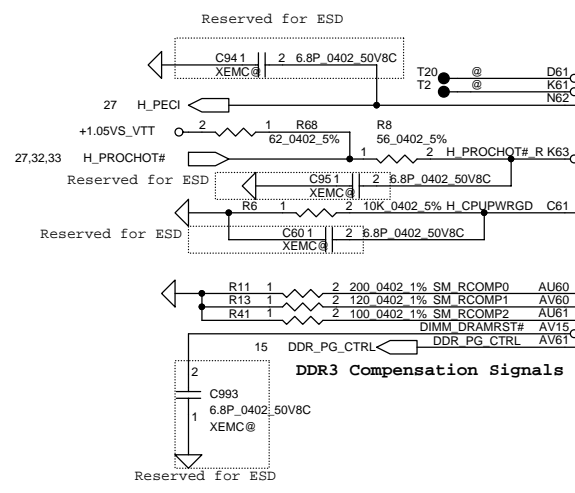
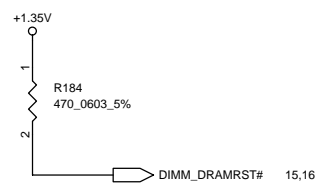
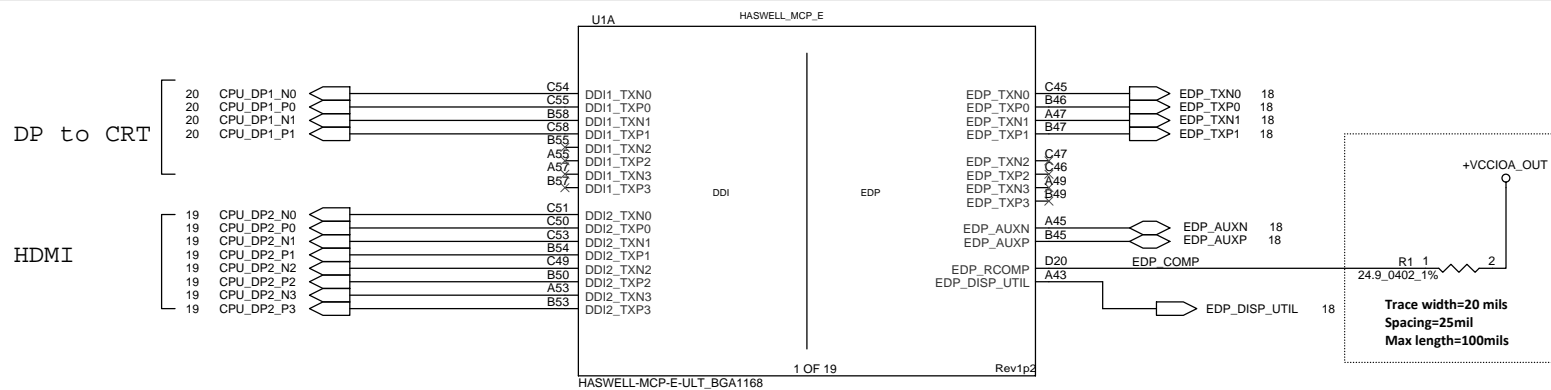
BTO Option Table

BTO Item	BOM Structure
EC 9012	9012@
EC 940	940@
Unpop	@
TPM Circuit	TPM@
eDP mode	EDP@
eDP to LVDS	TL@
Connector	CONN@
G-Sensor	GSEN@
XDP (Debug Port)	XDP@
KB Backlight	BL@
Debug Only	DEG@
MEC requirement	EMC@
MEC requirement unpop	XEMC@
GPU_Select	VGA@
reserve 3,5V MOS	35V@
BIOS 8M Solution	1ROM@
BIOS 4+2M Solution	2ROM@
IOAC Function	IOAC@
Touch screen Function	TS@

USB Port Table

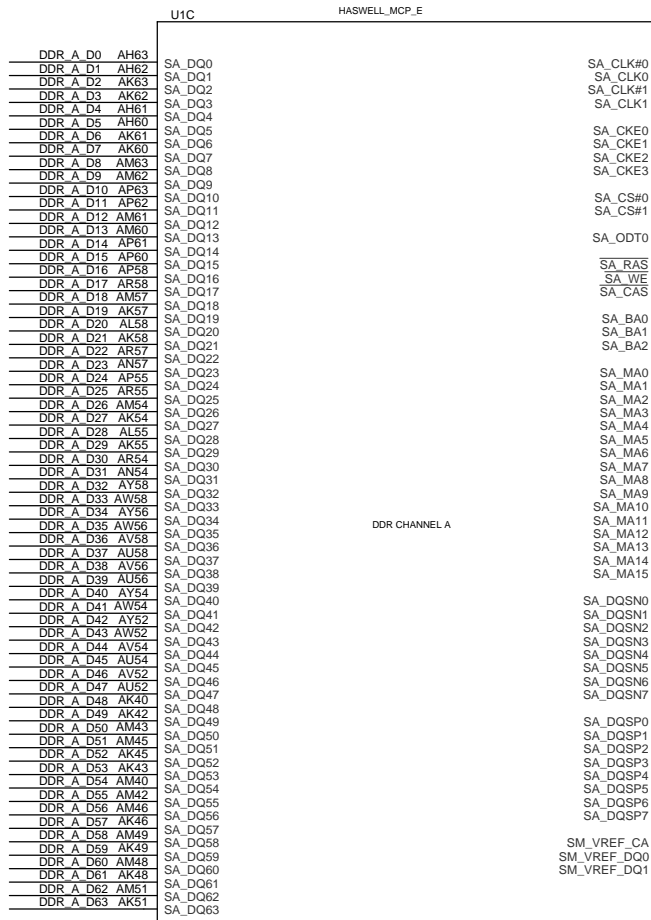
USB 3.0	Port		
XHCI	1	USB Port(Left 3.0)	
	2		
	3		
	4		
USB 2.0	USB 1.1	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port(Left 3.0)
		1	USB Port(Right 2.0)
	UHCI1	2	USB Port(Right 2.0)
		3	
		4	Mini Card(WLAN)
	UHCI2	5	
		6	Touch Screen
UHCI3	7	Camera	

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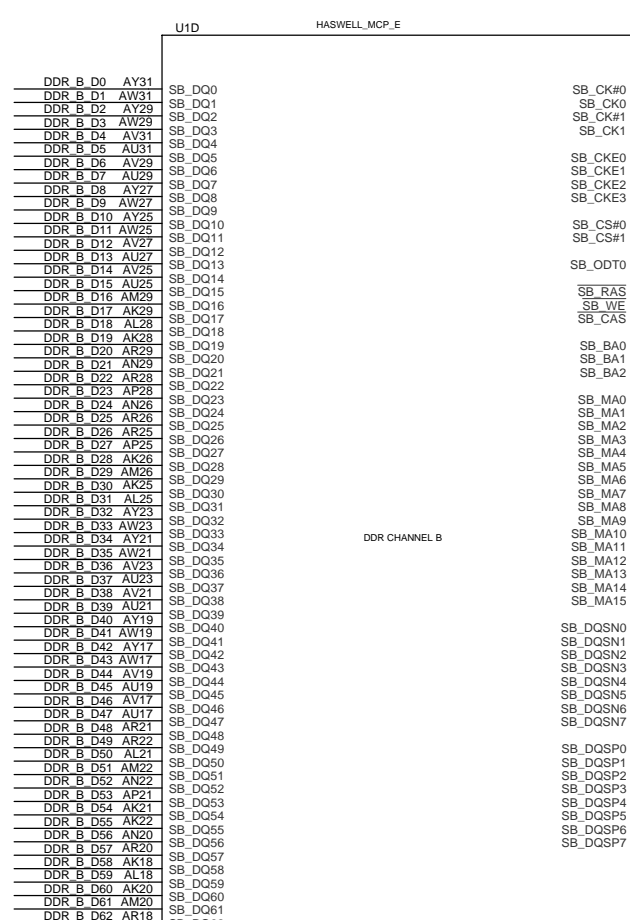
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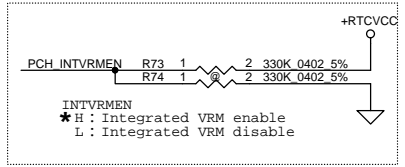
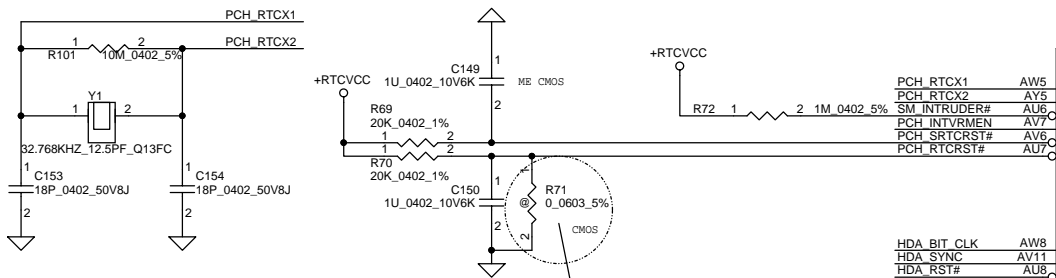
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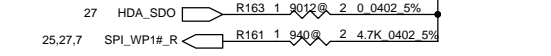
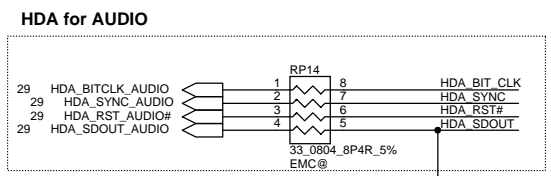
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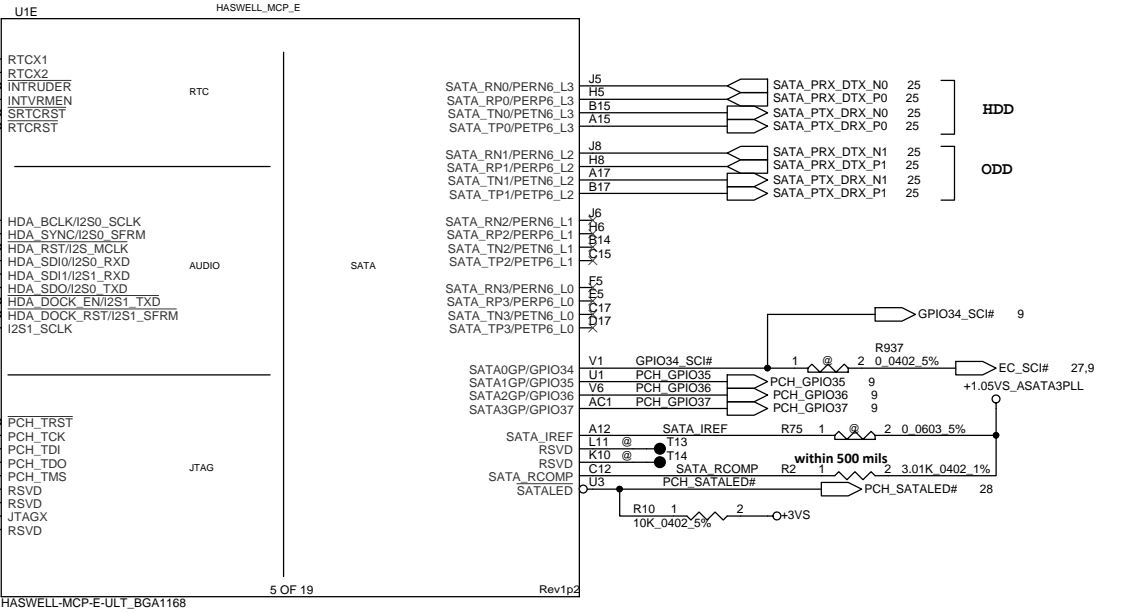
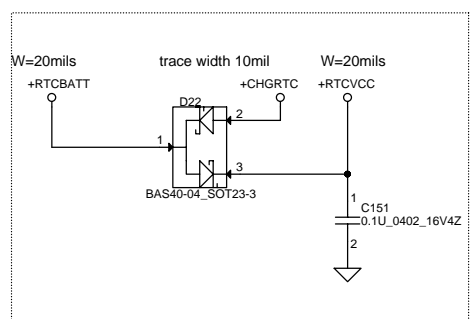
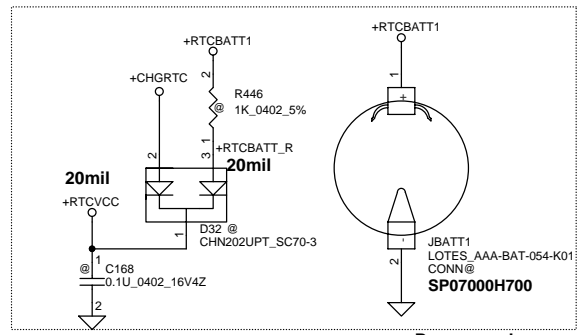
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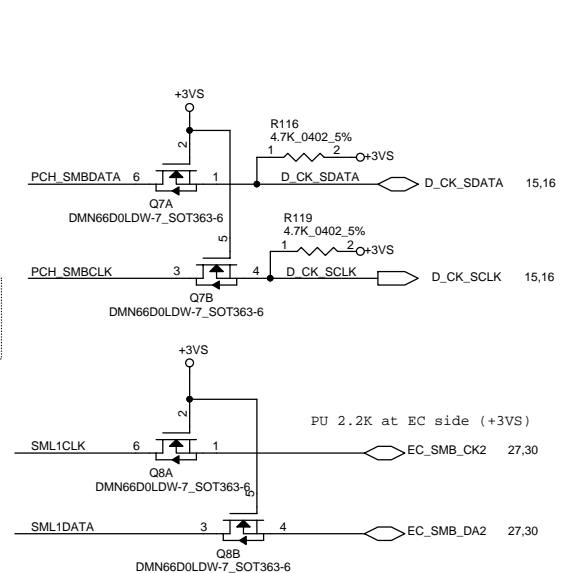
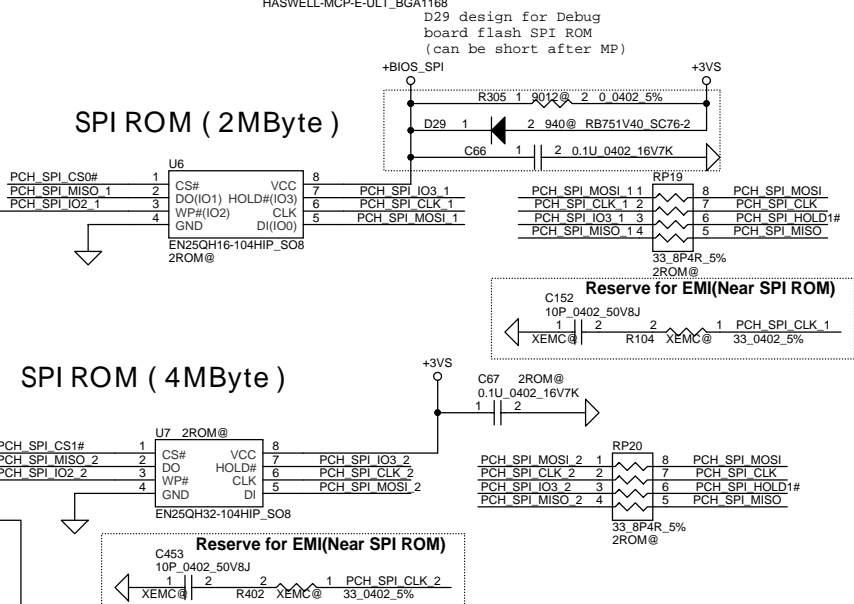
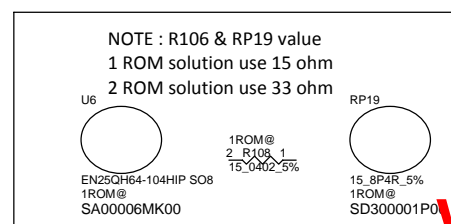
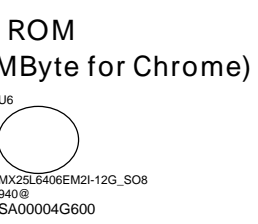
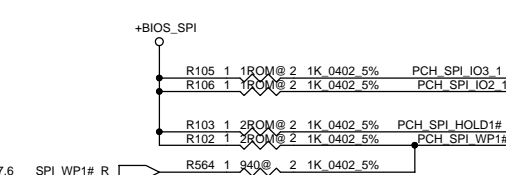
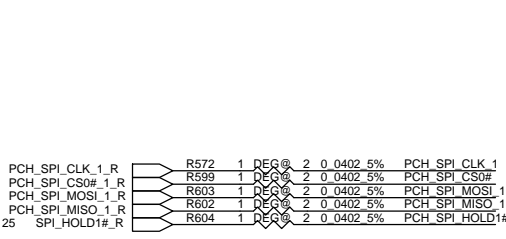
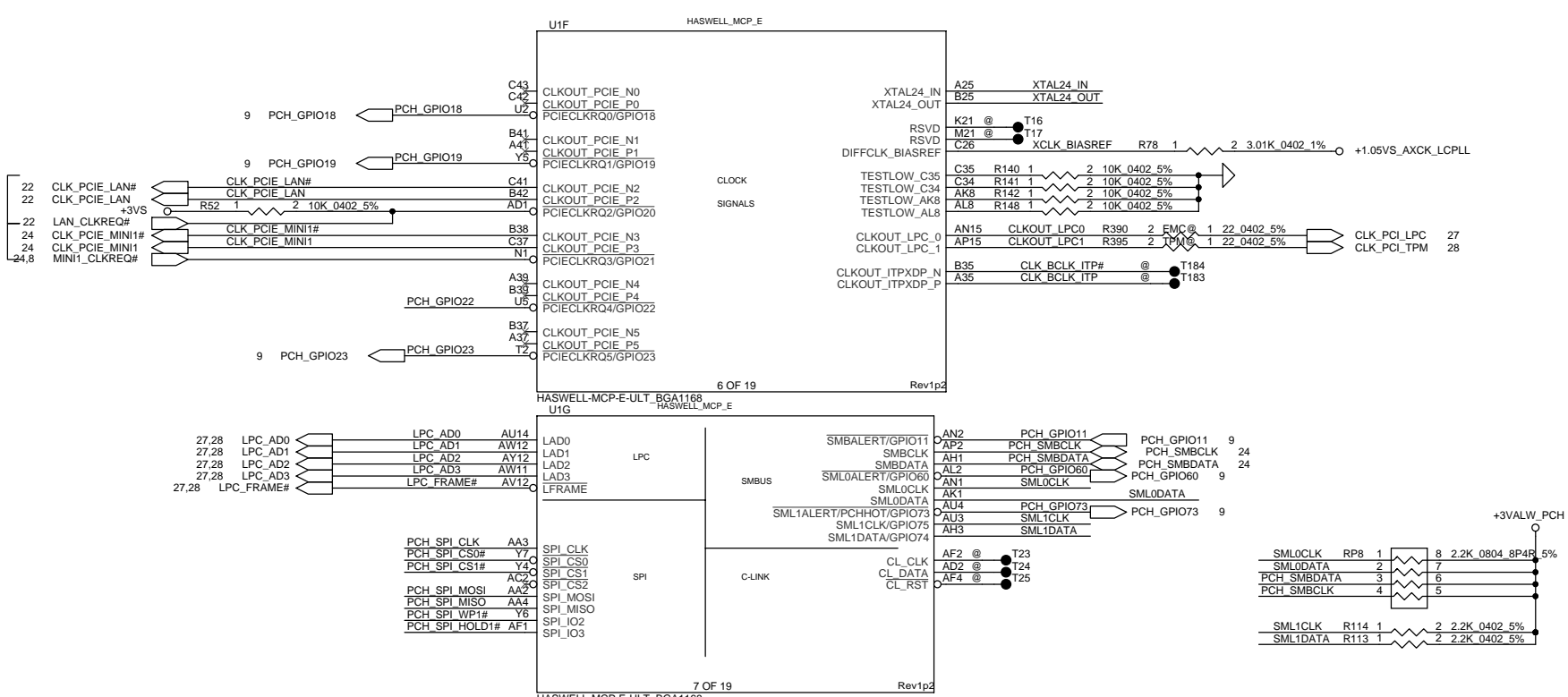
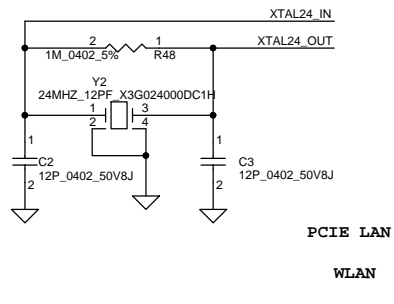
RTCRST close RAM door



ME Debug



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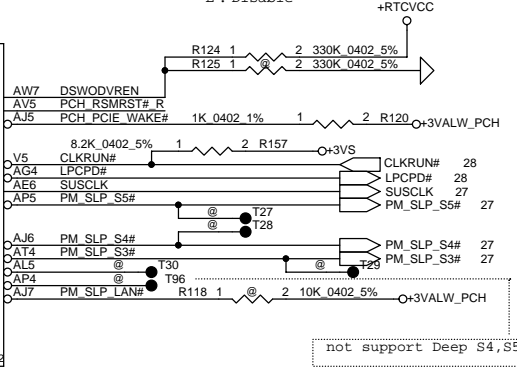
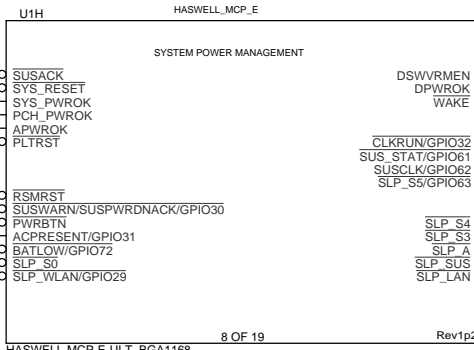
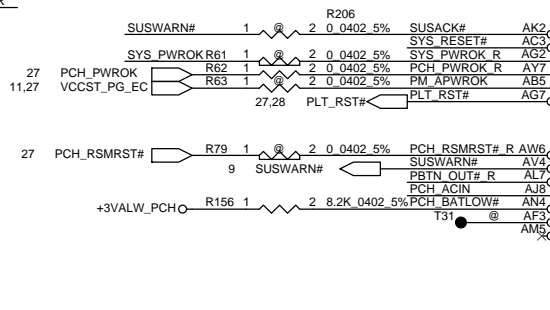
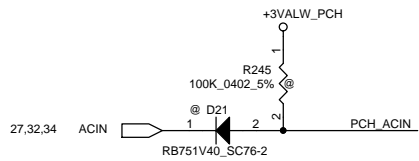
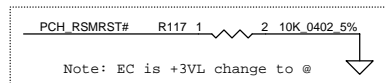
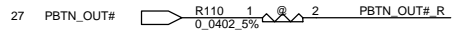
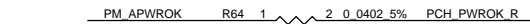
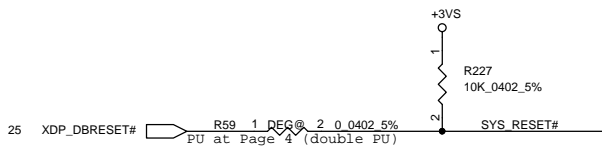
NOTE : R106 & RP19 value
 1 ROM solution use 15 ohm
 2 ROM solution use 33 ohm

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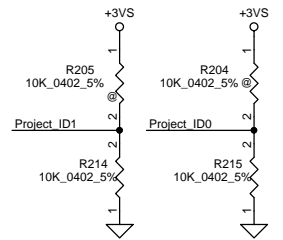
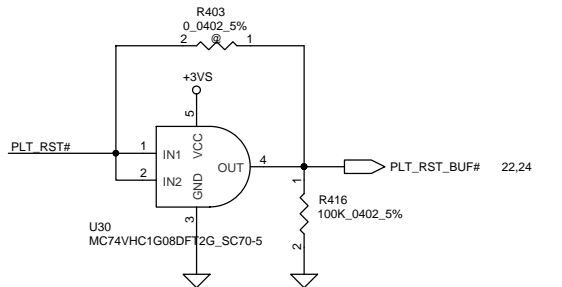
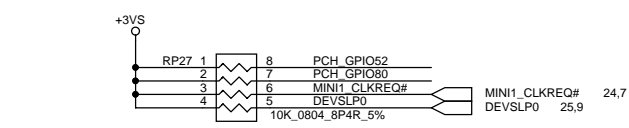
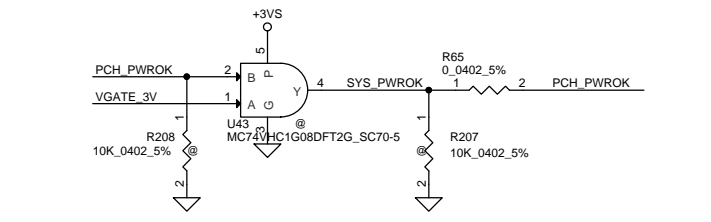
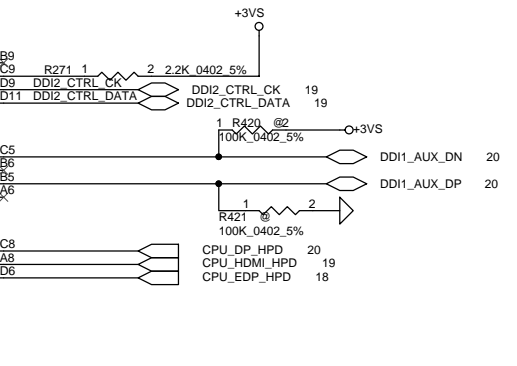
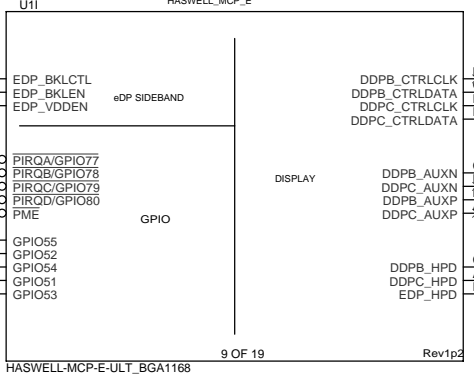
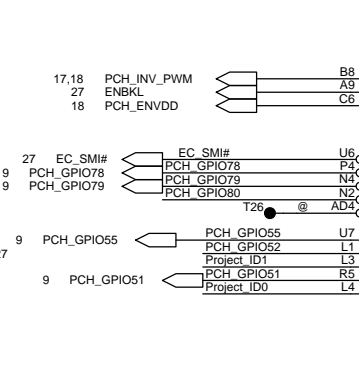
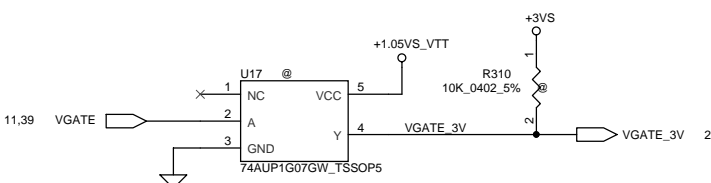
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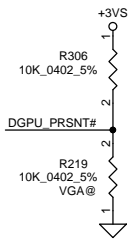
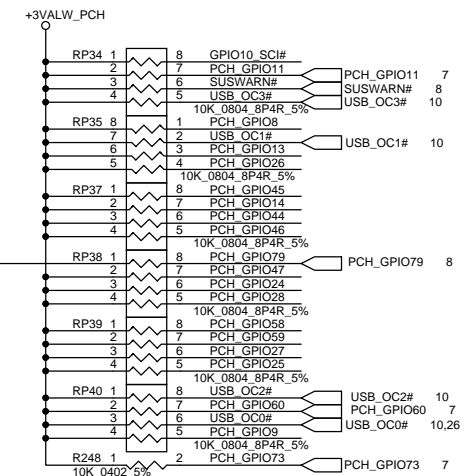
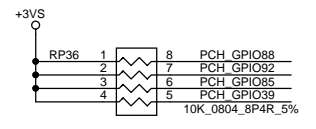
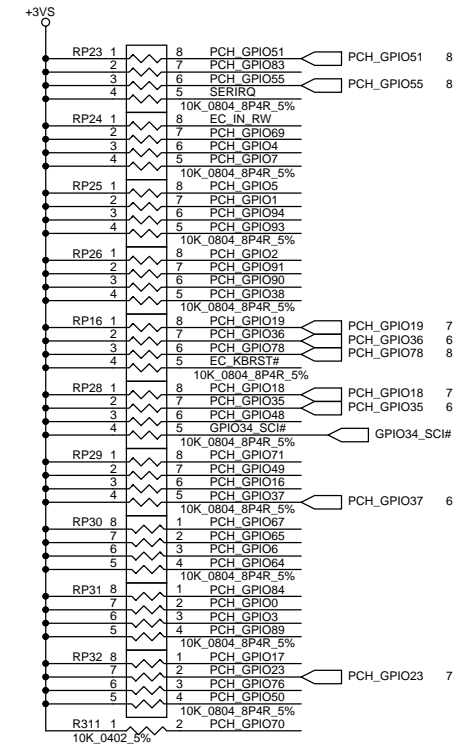
DDPB_CTRLDATA: Port B Detected
 DDPC_CTRLDATA: Port C Detected

* 1: Port B or C is detected
 0: Port B or C is not detected
 (Have internal PD)

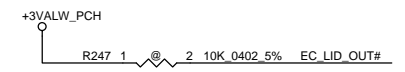
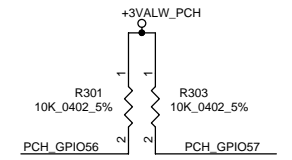
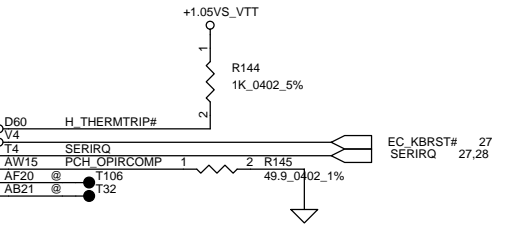
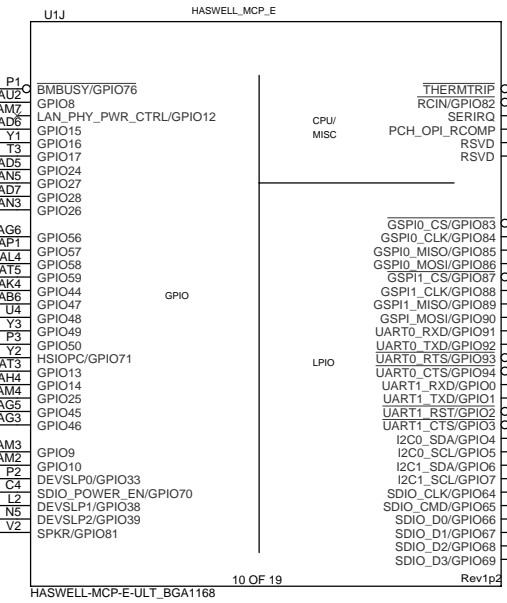


Project ID	Project_ID1 GPIO54	Project_ID0 GPIO53
*V5WE2/T2	0	0
Reserved	0	1
Reserved	1	0
Reserved	1	1

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	GPIO87 DGPU_PRSN#
DIS,Optimus	0
UMA	1



GPIO15 : TLS Confidentiality
 1: Intel ME TLS with confidentiality
 * 0: Intel ME TLS with no confidentiality
 (Have internal PD)

SDIO_D0 / GPIO66 : Top-Block Swap Override
 * 1: ENABLED (Have internal PU)
 0: DISABLED

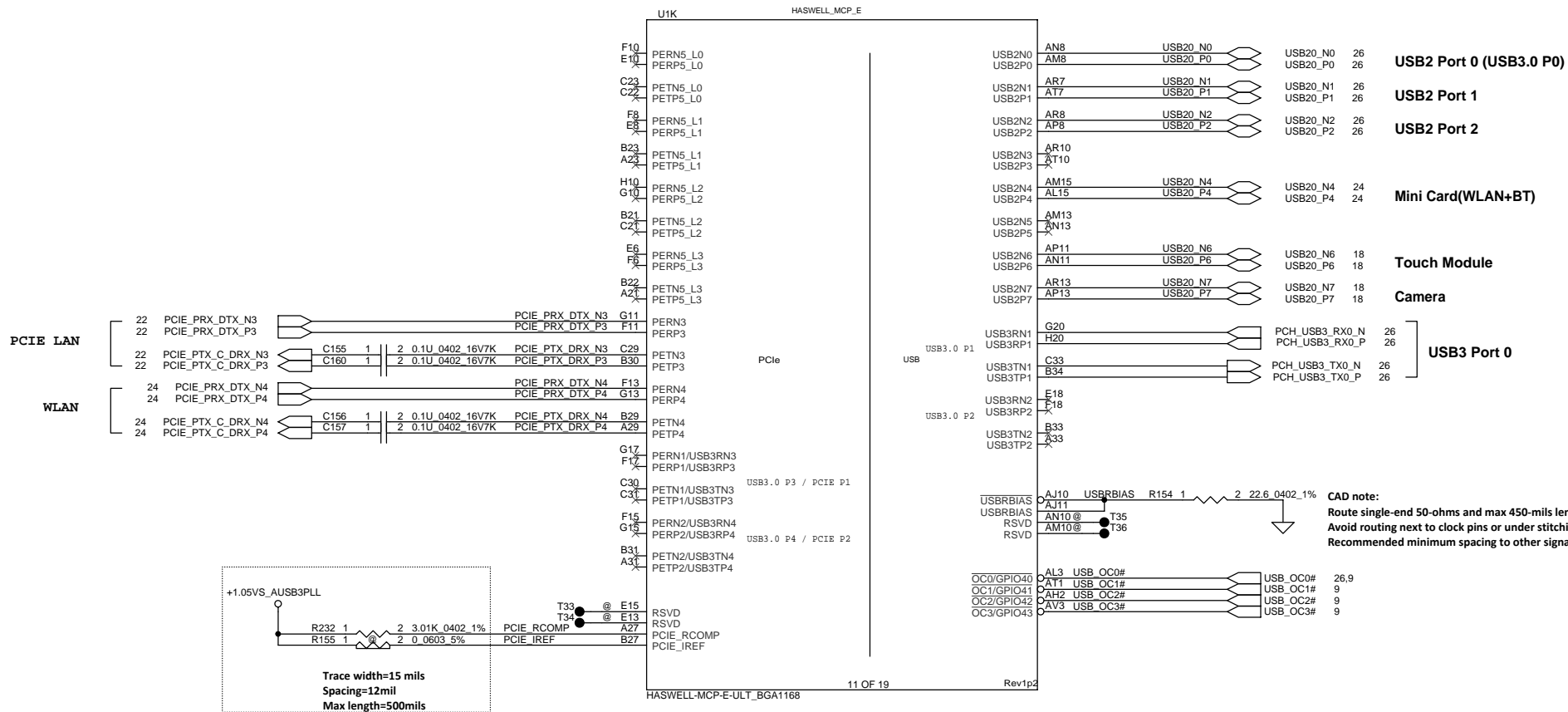
GSPI0_MOSI / GPIO86 : Boot BIOS Strap
 1: ENABLED
 * 0: SPI ROM (Have internal PL)

SPKR / GPIO81 : NO REBOOT
 1: ENABLED
 * 0: DISABLED (Have internal PD)

Security Classification		Compal Secret Data		Title	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Compal Electronics, Inc. HSW MCP(6/11) GPIO,LPIO	

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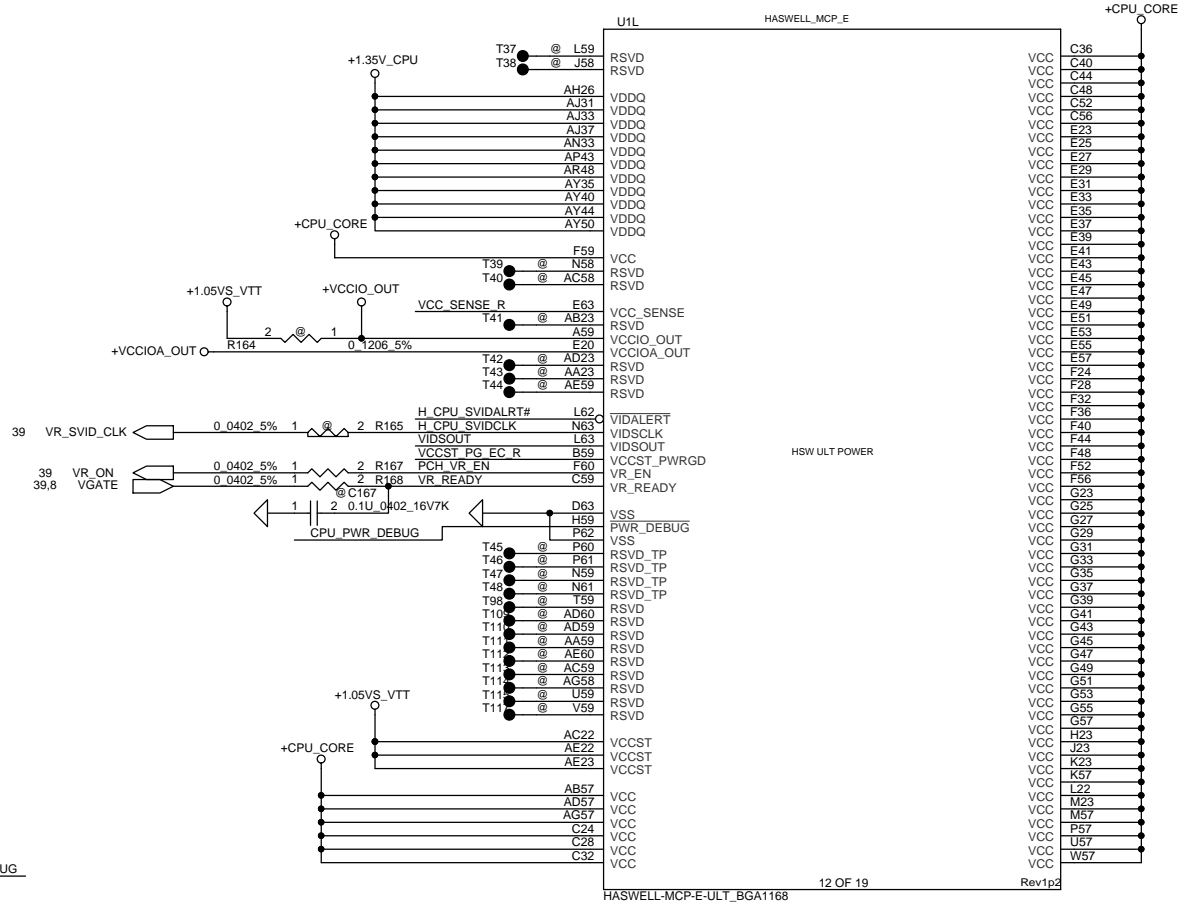
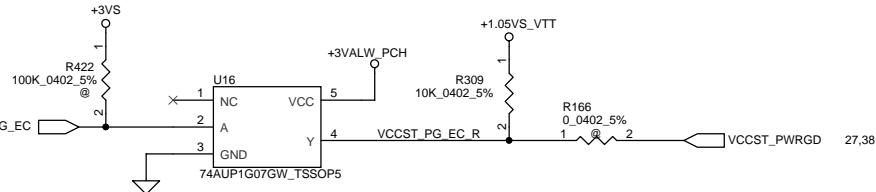
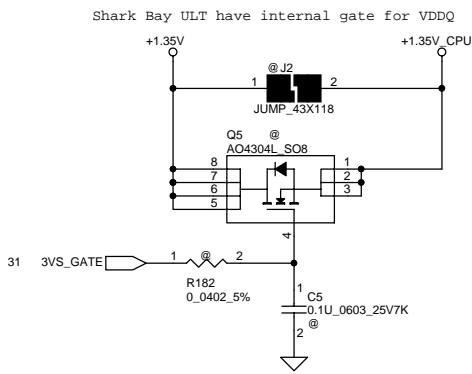
Document Number: **V5WE2 M/B LA-9532P Schematic**
 Date: Monday, April 08, 2013 Sheet 9 of 42



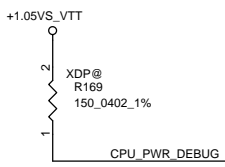
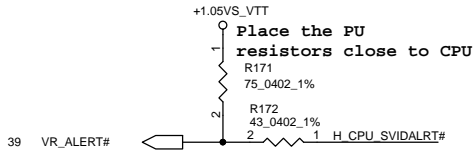
CAD note:
Route single-end 50-ohms and max 450-mils length.
Avoid routing next to clock pins or under stitching capacitors.
Recommended minimum spacing to other signal traces is 15 mils

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Document Number	V5WE2 M/B LA-9532P Schematic		Rev	0.2	
Date:	Monday, April 08, 2013		Sheet	10 of 42	

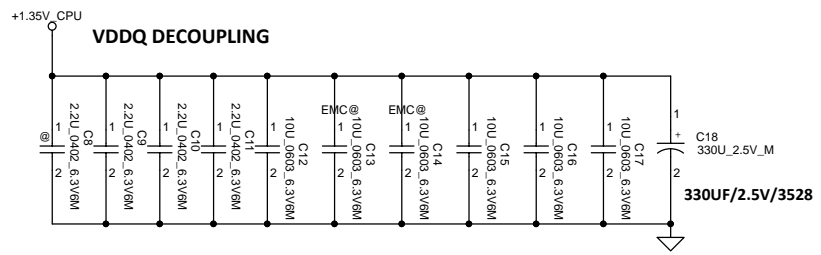
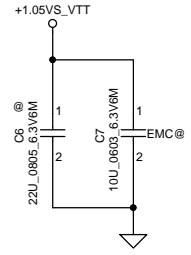
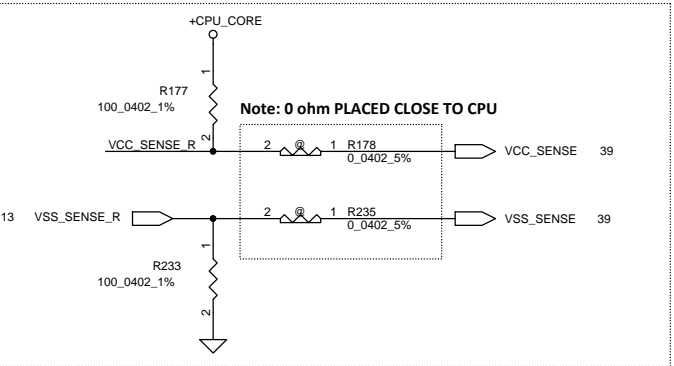
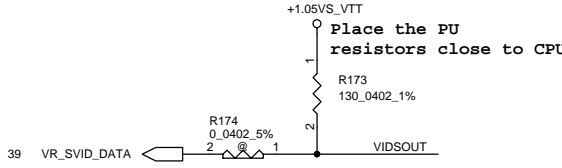
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SVID ALERT

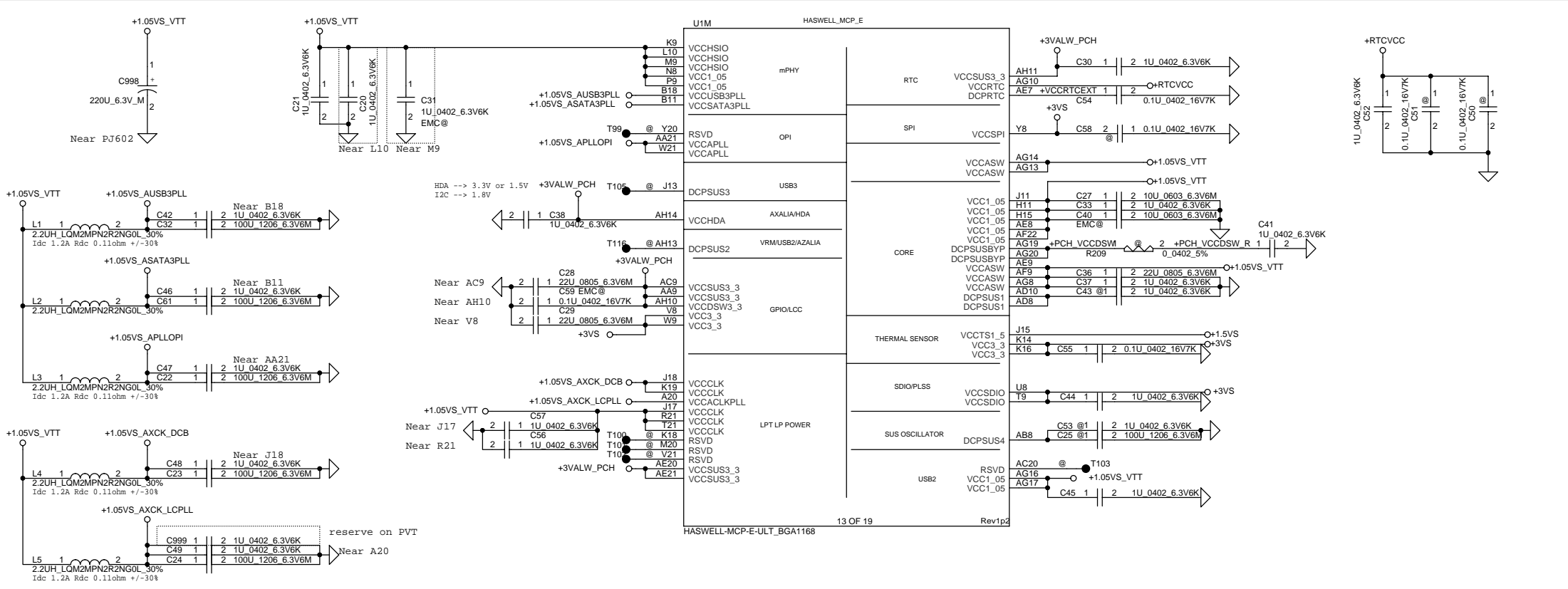


SVID DATA



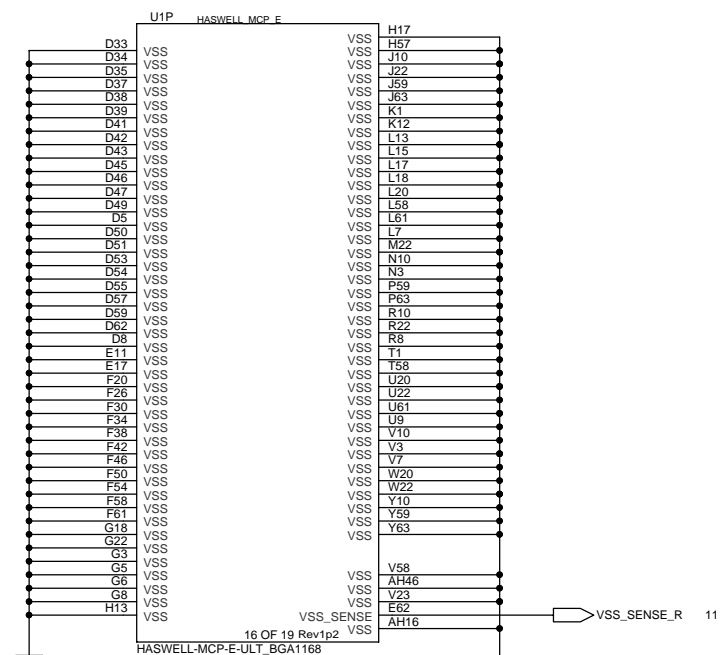
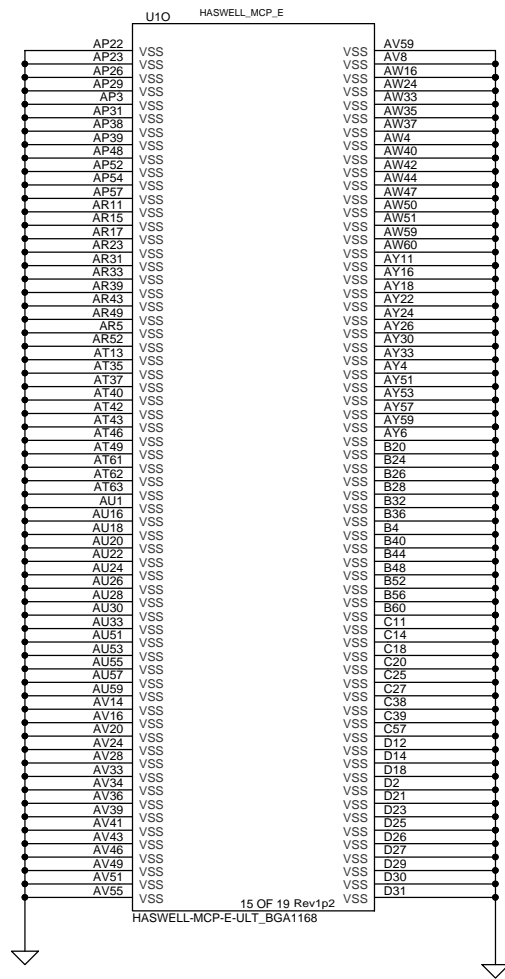
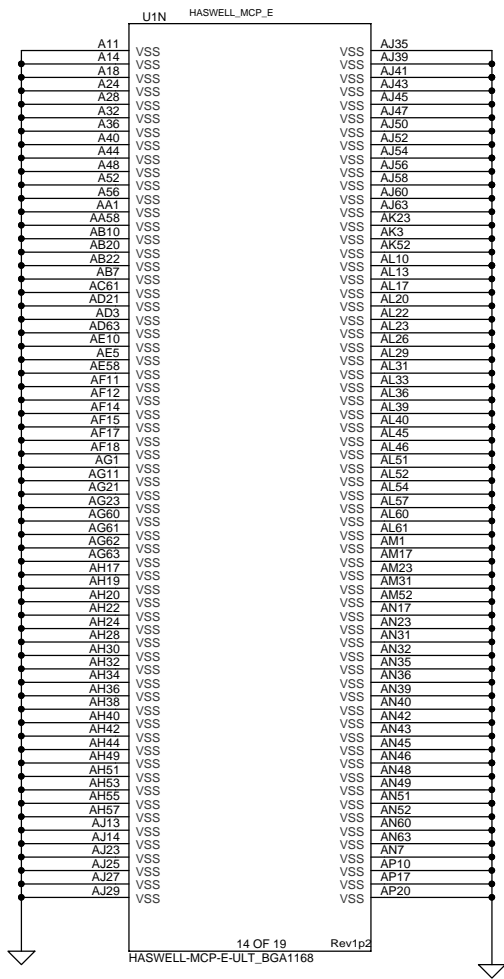
+1.35V : 470UF/2V/7343 *2
 10UF/6.3V/0603 * 6
 2.2UF/6.3V/0402 * 4

Security Classification		Compal Secret Data		Title	
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Document Number	V5WE2 M/B LA-9532P Schematic		Rev	0.2	
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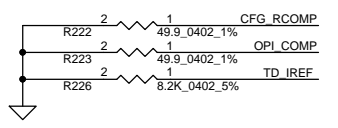
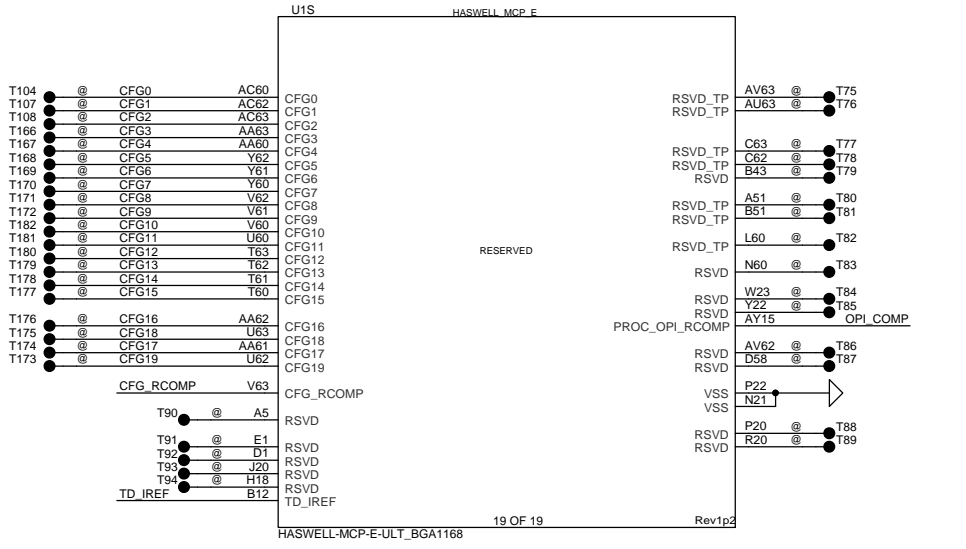
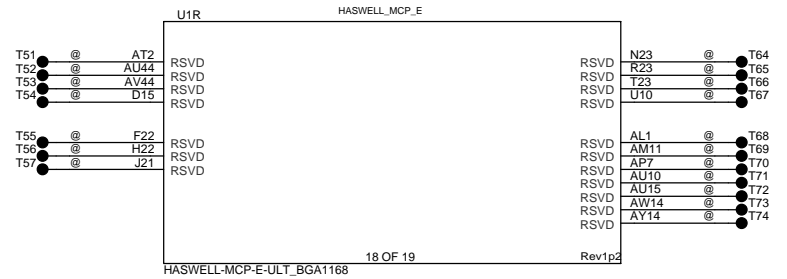
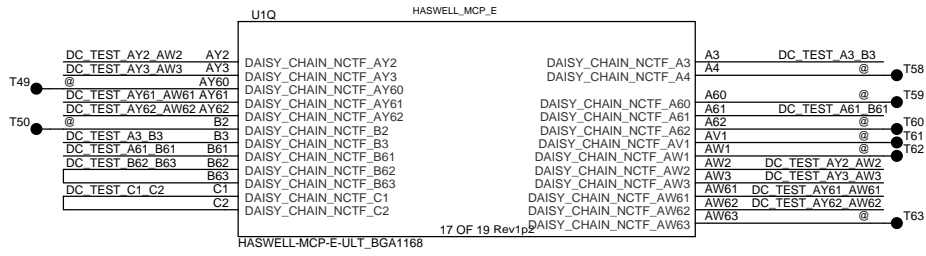
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Issued Date		Deciphered Date		Title	
2012/07/10		2013/07/10		HSW MCP(9/11) Power	
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Size	Document Number	Rev			
Custom	V5WE2 M/B LA-9532P Schematic	0.2			
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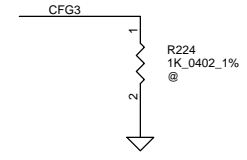


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	
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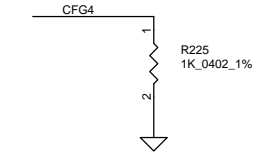
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CFG Straps for Processor

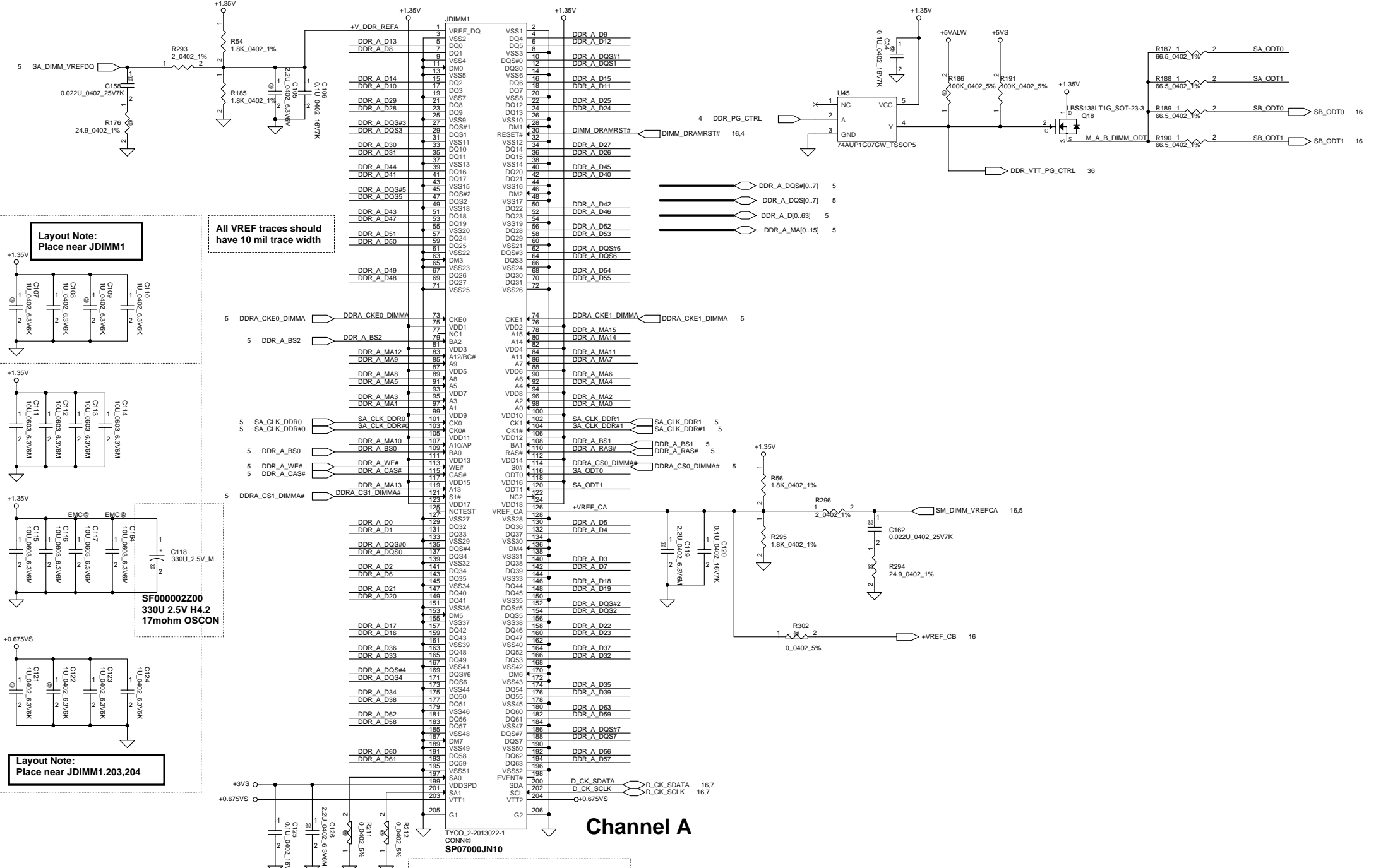


Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port





Layout Note:
Place near JDIMM1

All VREF traces should have 10 mil trace width

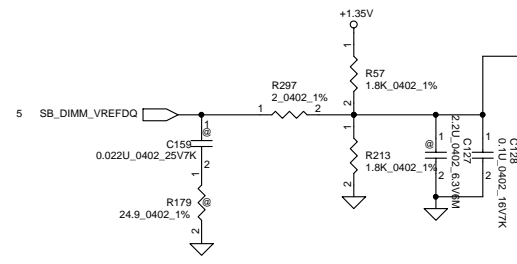
SF00002Z00
330U 2.5V H4.2
17mohm OSCON

Layout Note:
Place near JDIMM1.203,204

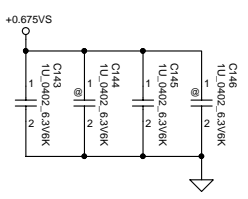
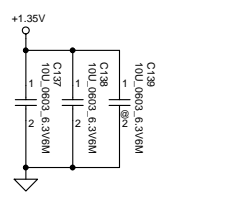
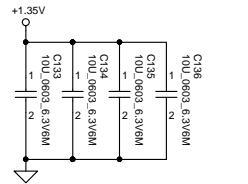
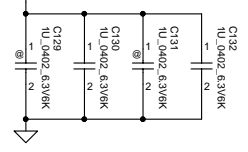
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DIMM_1 STD H:4mm

Channel A

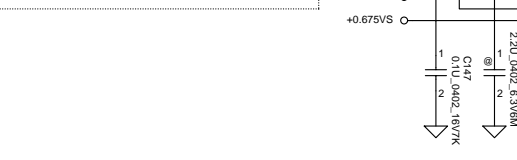
Security Classification		Compal Secret Data		Title	
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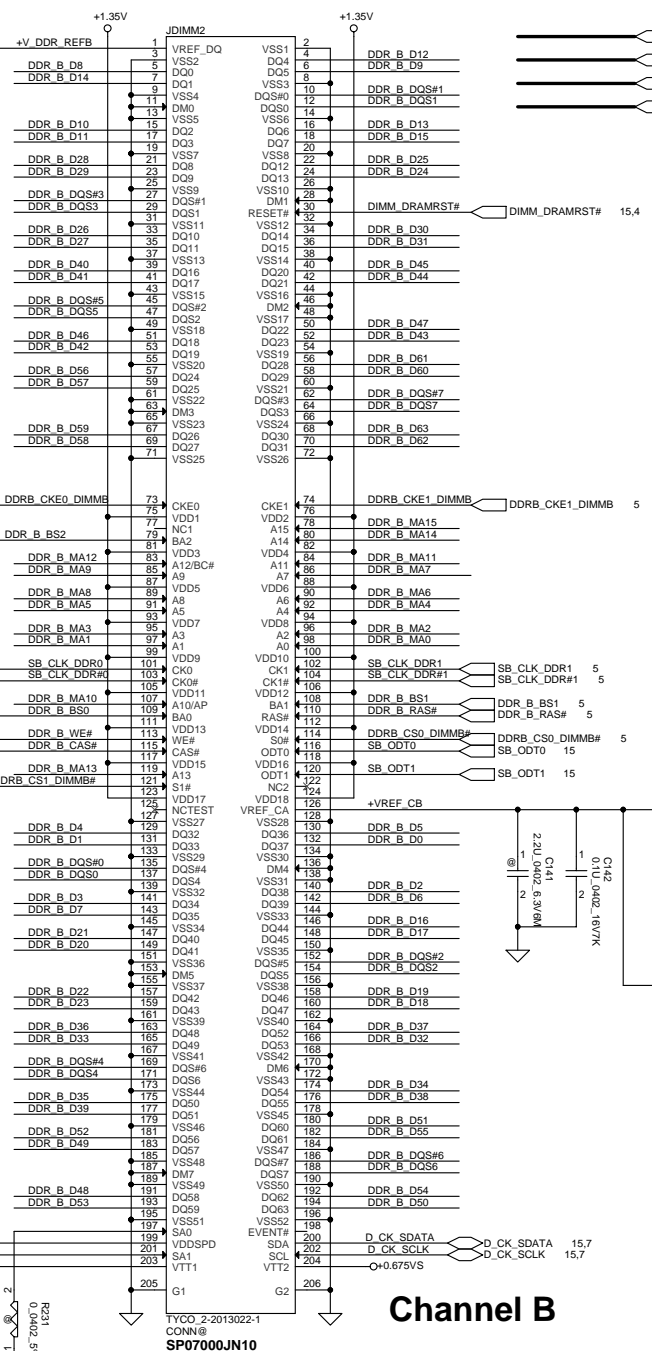
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204

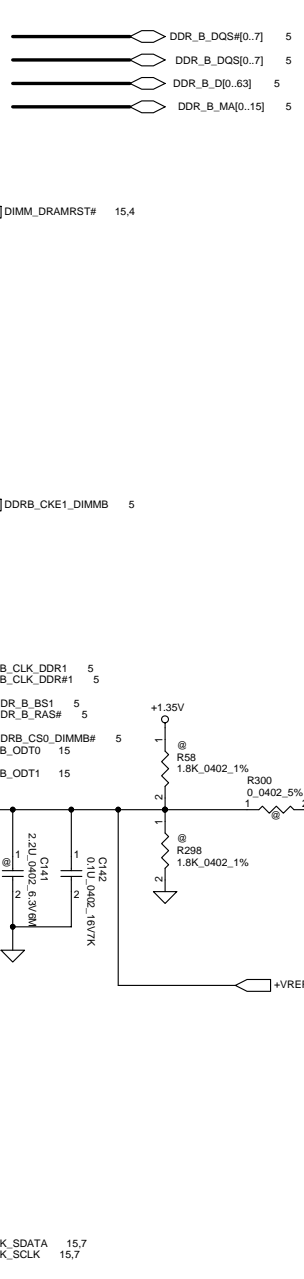


All VREF traces should have 10 mil trace width

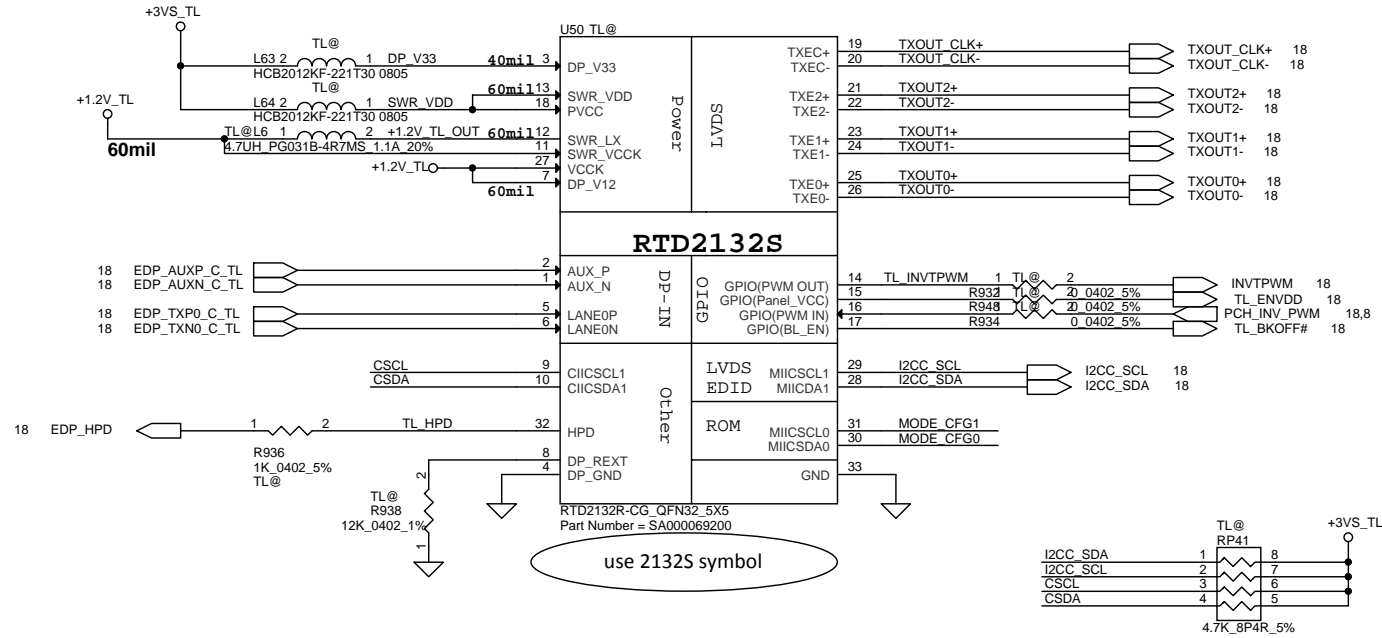
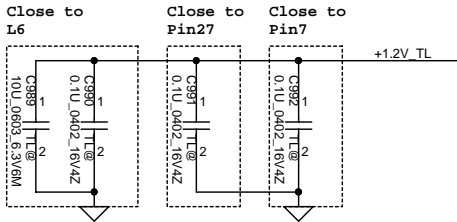
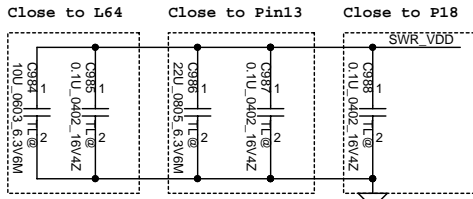
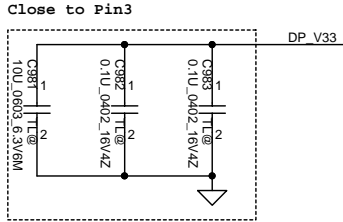
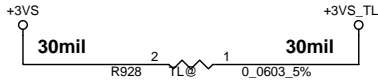


Channel B

<Address: SA1:SA0=10>
DIMM_2 STD H:4mm



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Document Number	VSW E2 M/B LA-9531P Schematic			Rev	0.2
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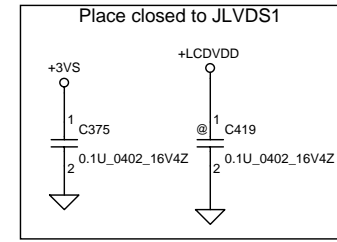
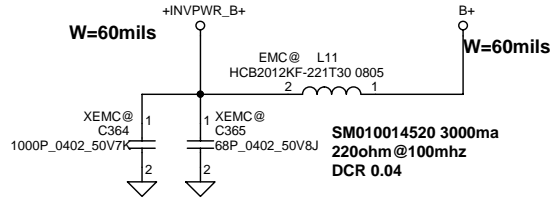
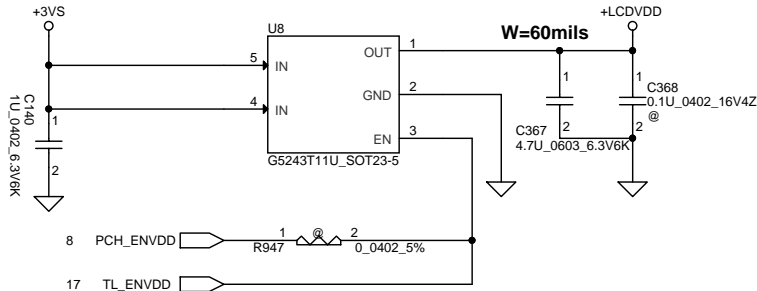


	MODE_CFG0(PIN30)	
	0	1
MODE_CFG1(PIN31)	0	EP MODE
	1	ROM ONLY MODE

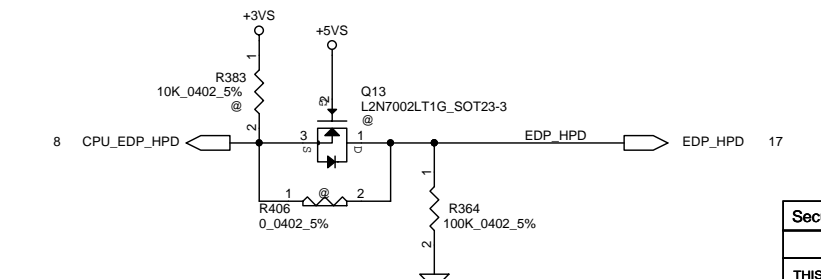
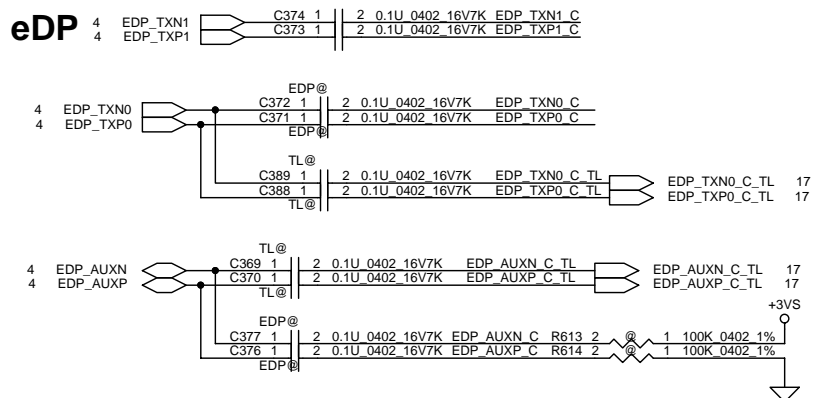
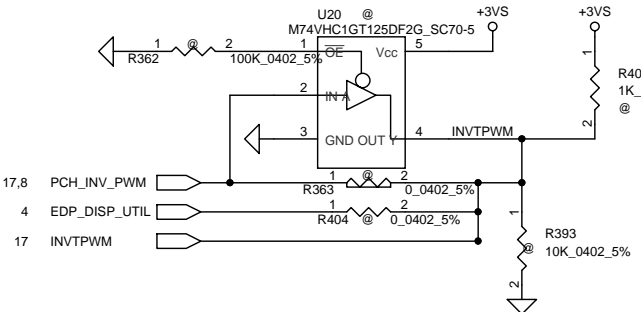
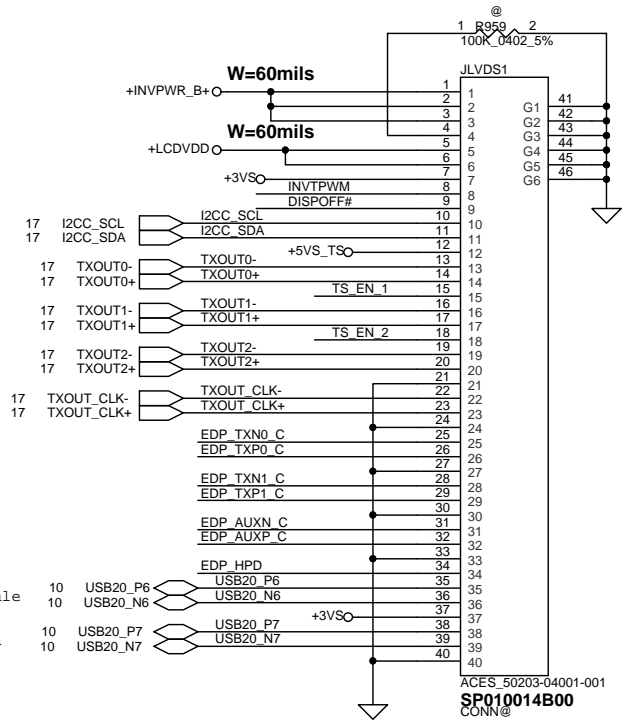
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Title	LVDS Translator - RTD2132R	
Document Number	V5WE2 M/B LA-9532P Schematic	
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LCD POWER CIRCUIT



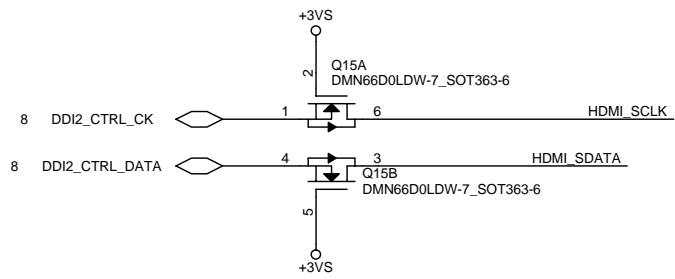
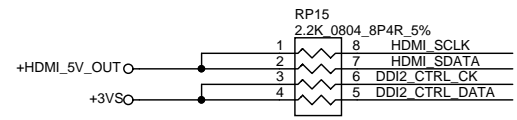
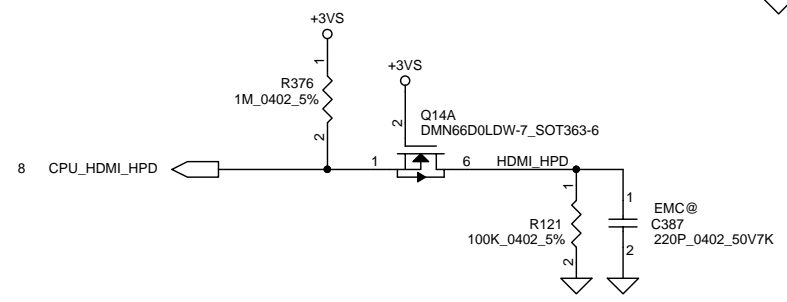
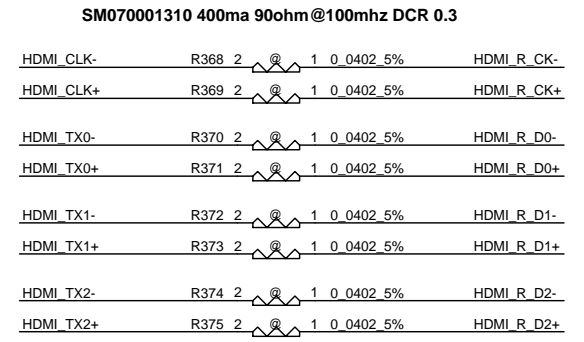
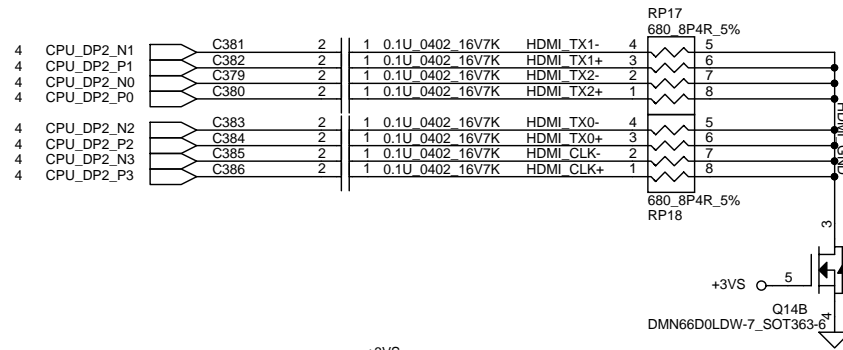
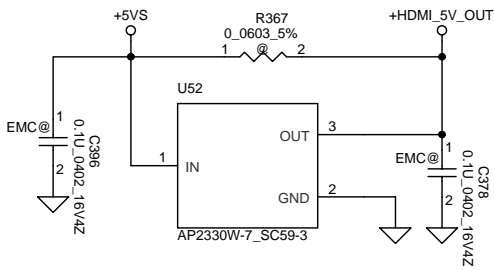
LCD/ LED PANEL Conn.



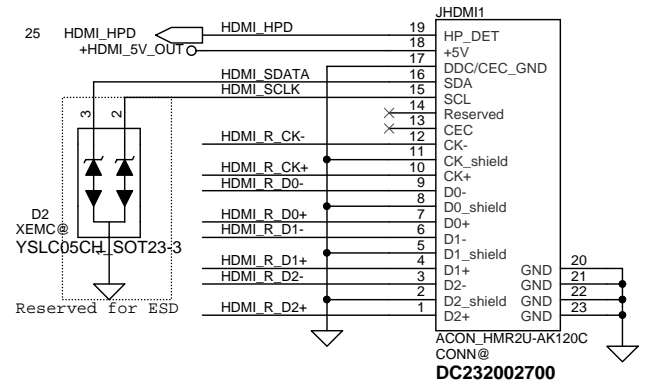
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	eDP Connector
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Document Number	V5WE2 M/B LA-9532P Schematic			Rev	0.2
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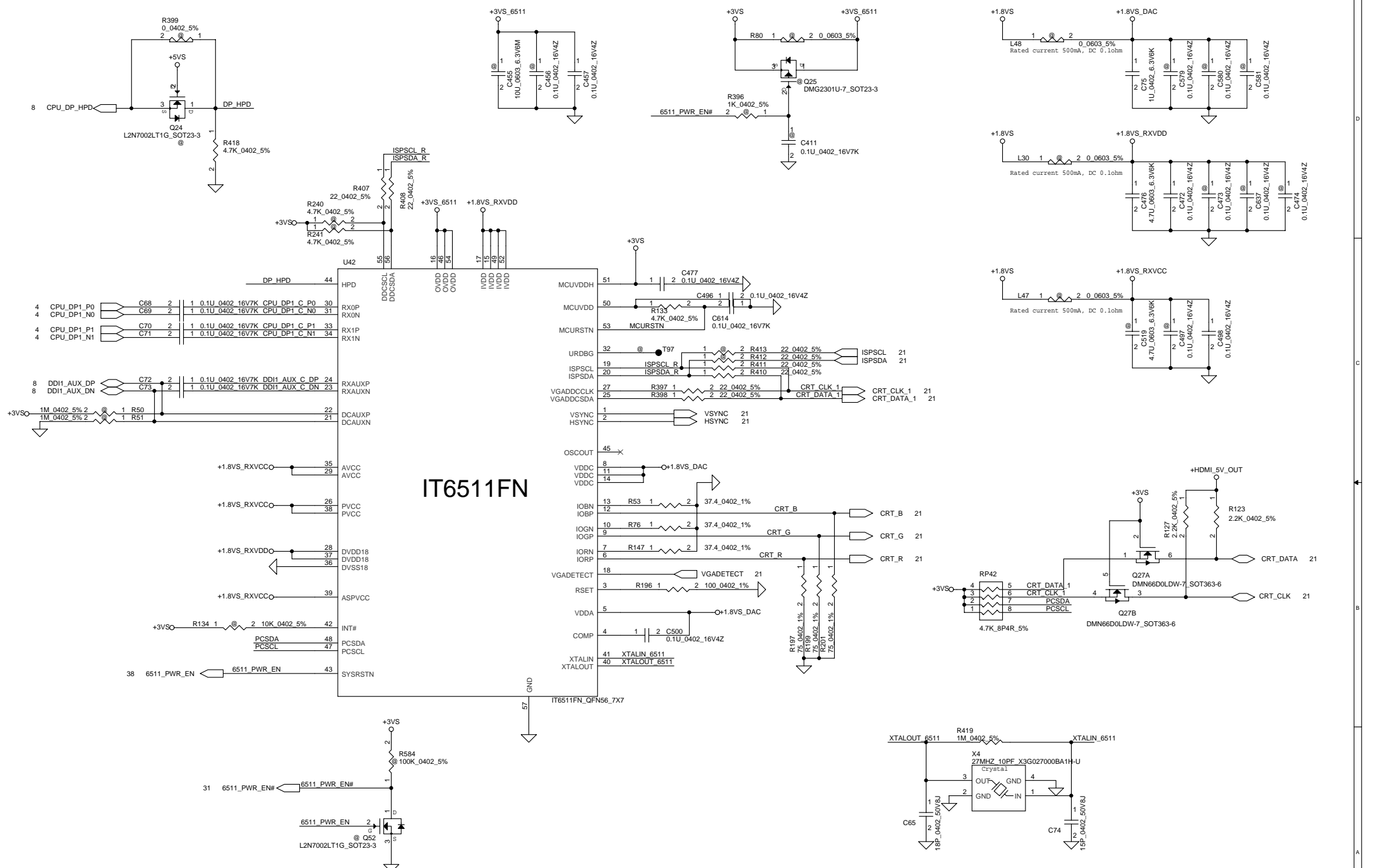
W=40mils



HDMI connector

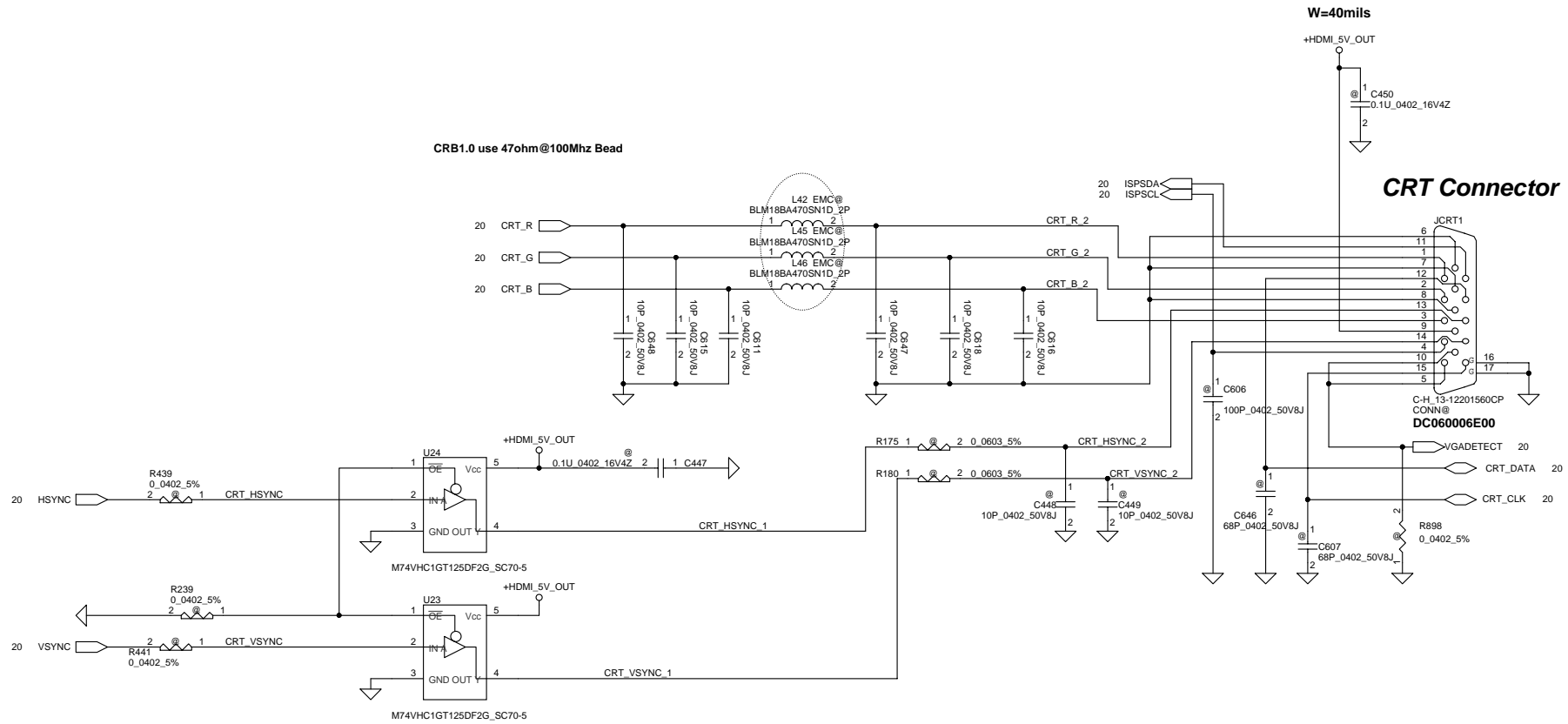


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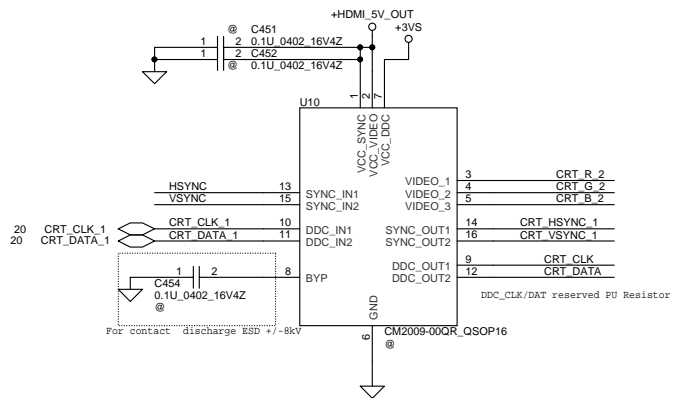


CRB1.0 use 47ohm@100Mhz Bead

W=40mils

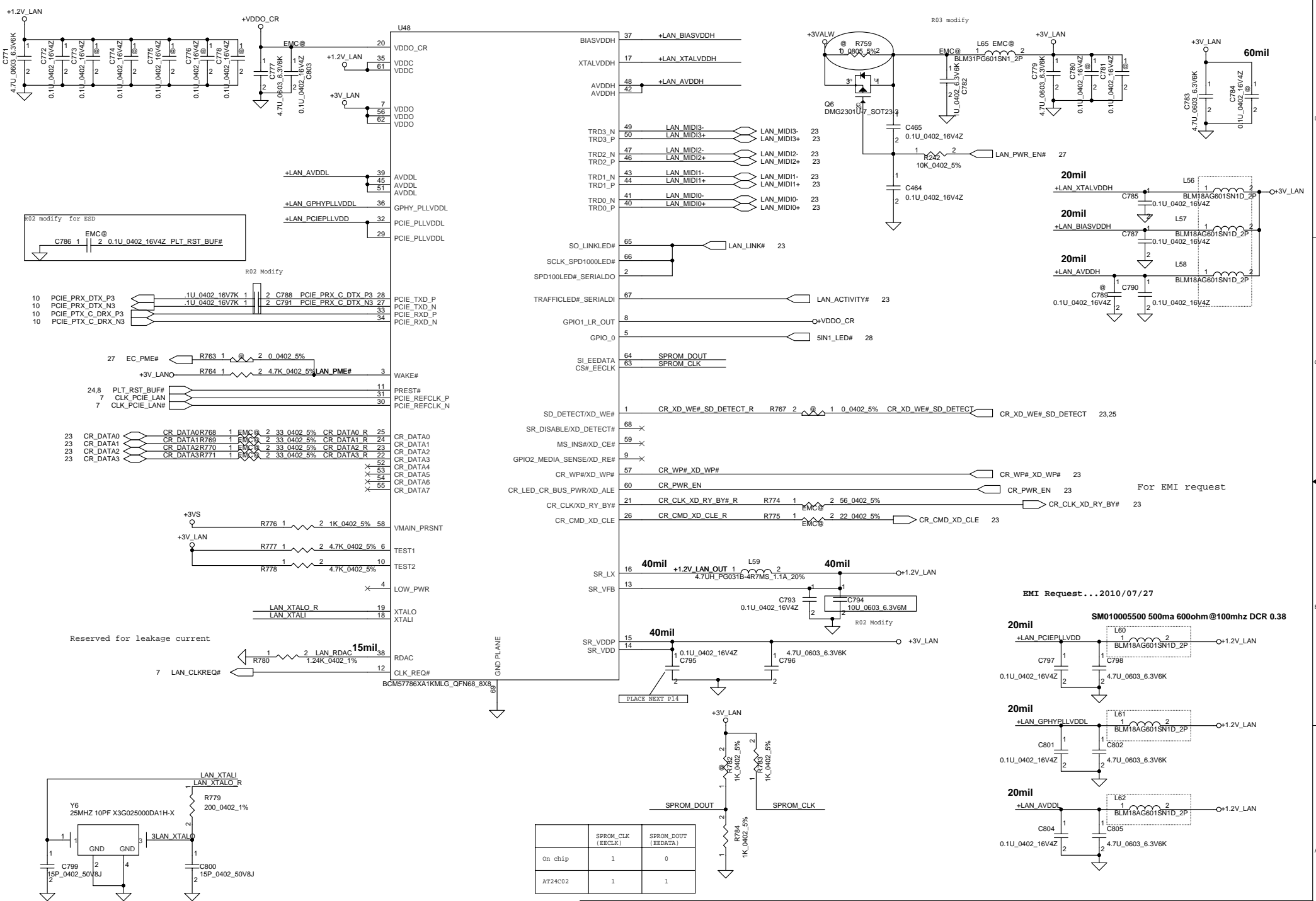
CRT Connector

C-H 13-12201560CP
CONN@
DC060006E00



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				Customer	0.2
				Date: Monday, April 08, 2013	
				Sheet 21 of 42	

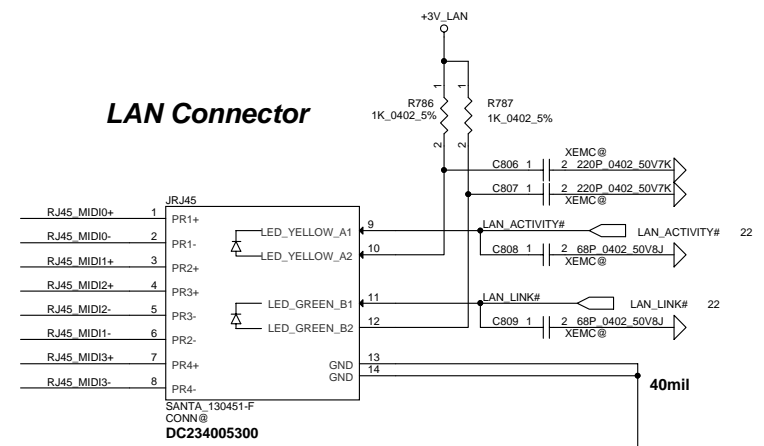
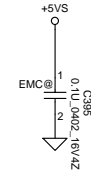
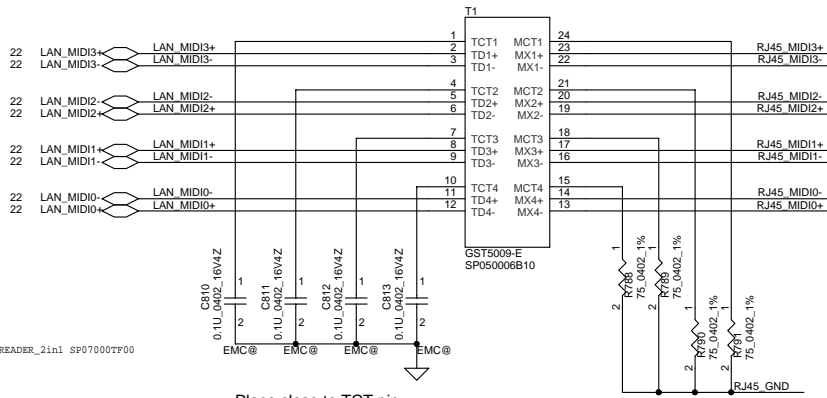
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	SPROM_CLK (EECLK)	SPROM_DOUT (EEDATA)
On chip	1	0
AT24C02	1	1

Security Classification		Compal Secret Data		Title	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Broadcom BCM57785	
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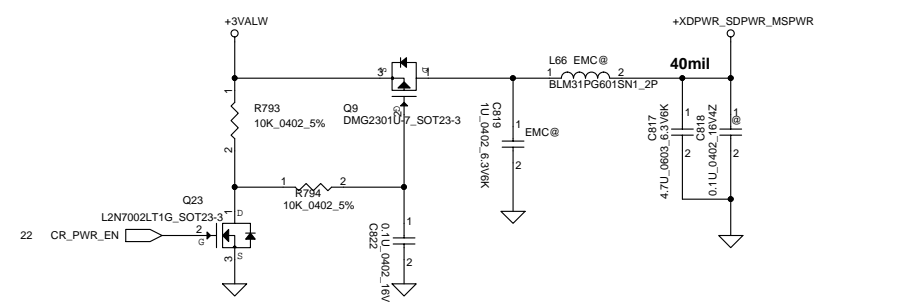
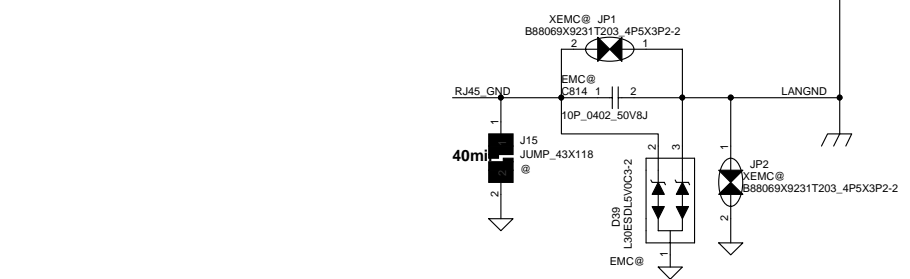
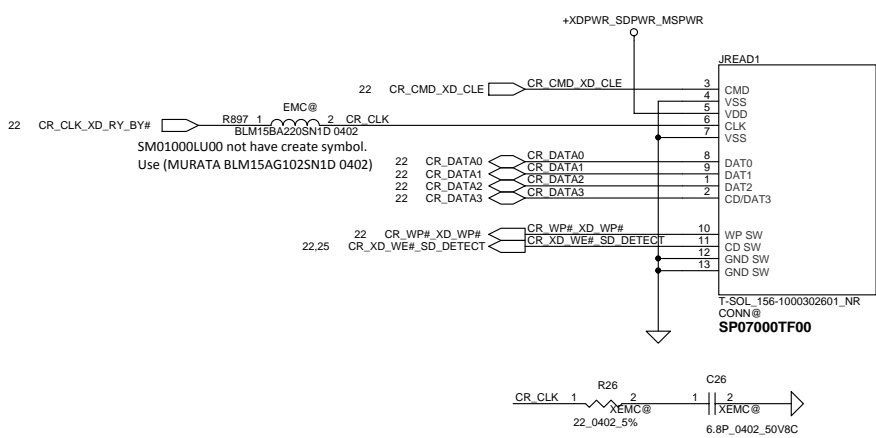


CARD READER_2in1 SP07000TF00

Place close to TCT pin

BOTHHAND: S X'FORM_GST5009-E LF LAN, SP050006B10
TIMAG:S X'FORM_IH-160 LAN , SP050006F00

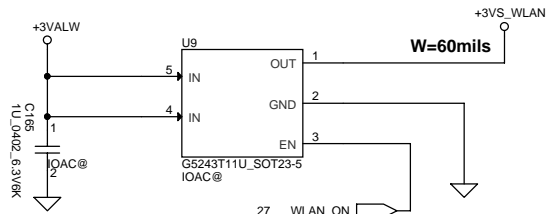
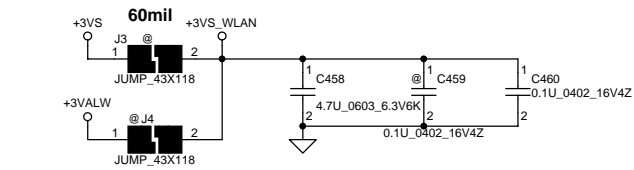
Card Reader Connector



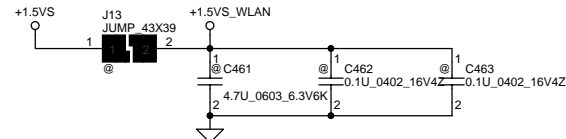
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	
				LAN Magnetic & RJ45	
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				V5WE2 M/B LA-9532P Schematic	0.2
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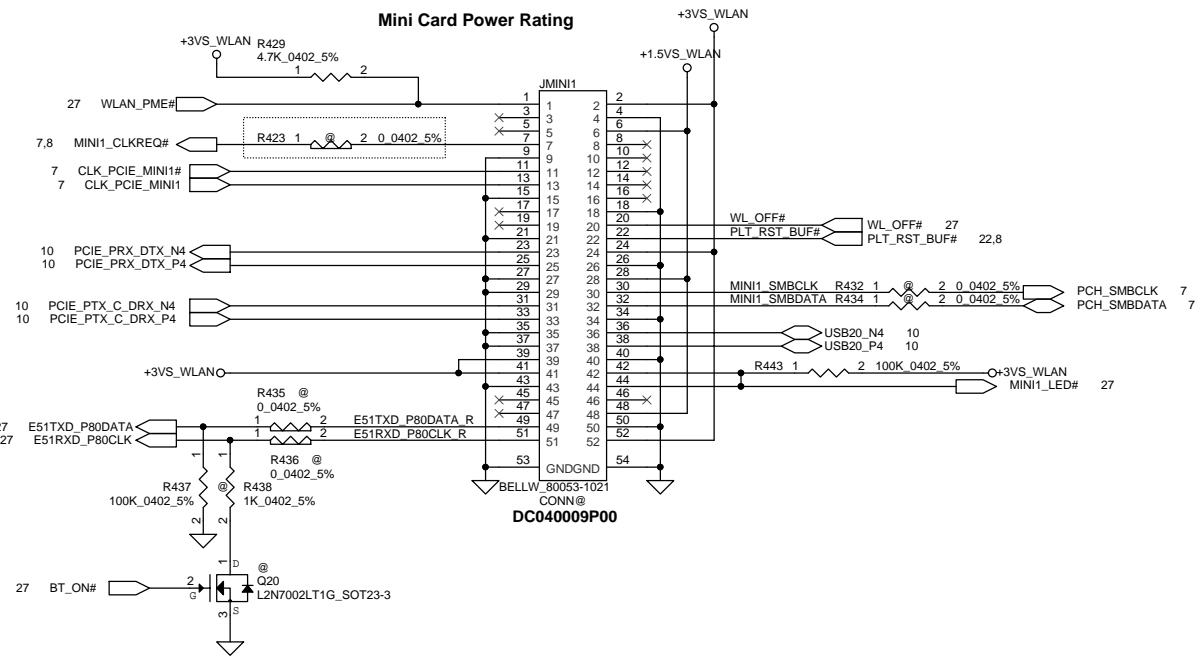
For Wireless LAN



For DVT2 verify IOAC function



Mini Card Power Rating

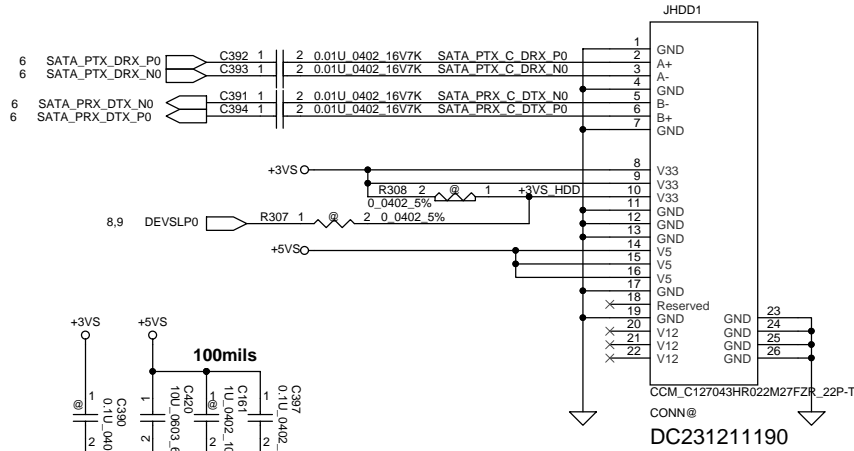


DC040009P00

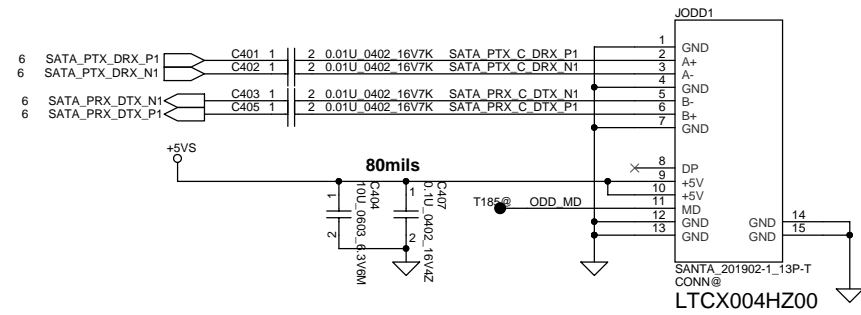
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	MINI CARD (WLAN)
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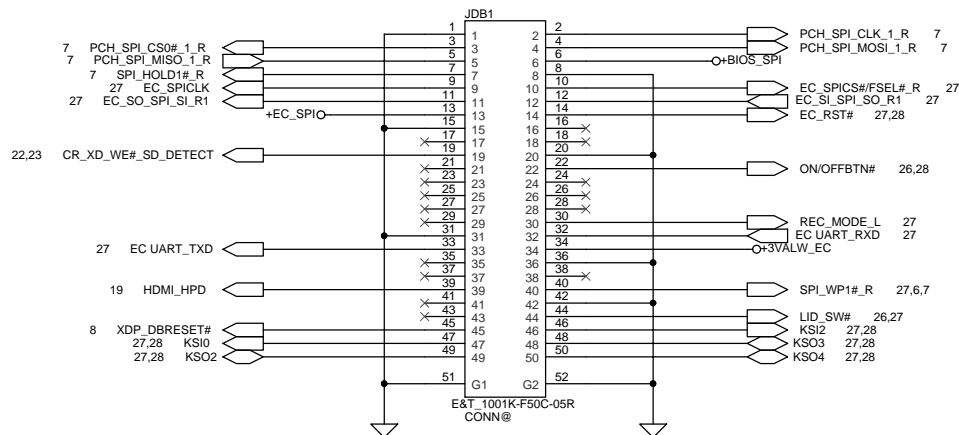
SATA HDD1 Conn.



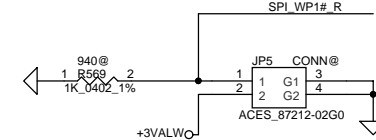
SATA ODD Conn.



Debug Board



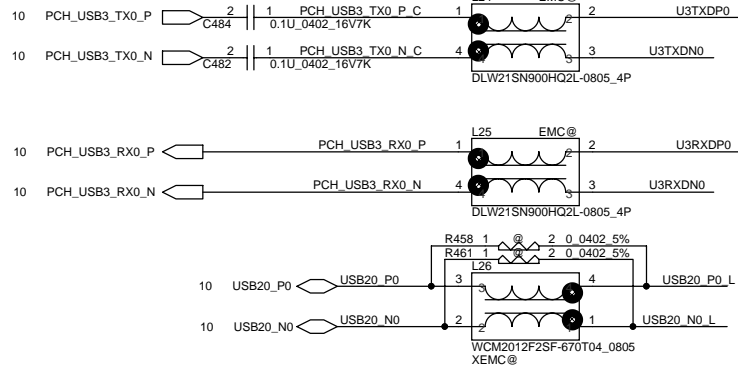
Kill SW



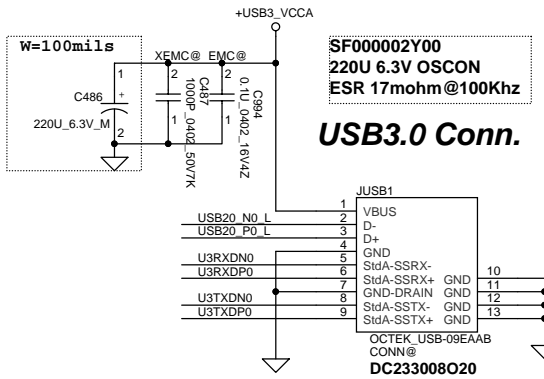
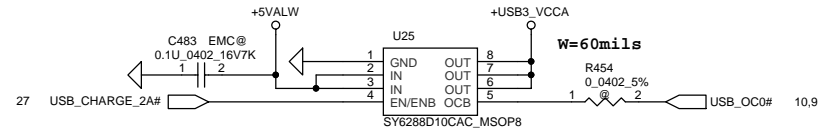
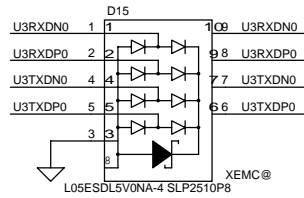
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	Title	HDD/ODD/USB3.0 Conn
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Document Number	V5WE2 M/B LA-9532P Schematic			Rev	0.2
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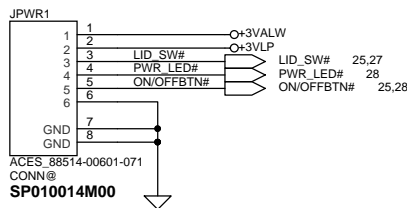
SM070000S80 WCM2012F2SF-670T04 67ohm



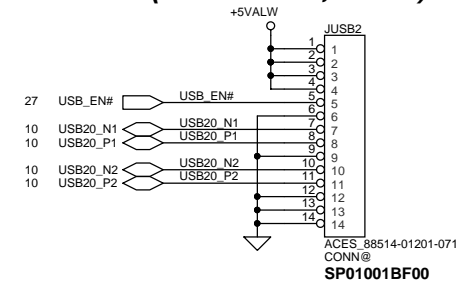
For ESD request



PWR / B

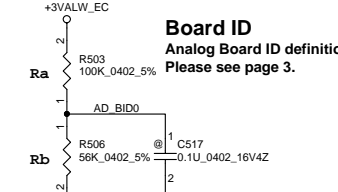
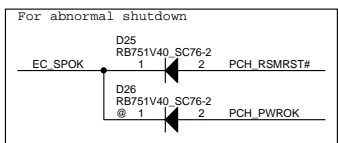
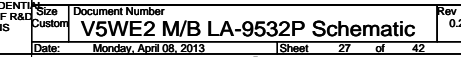
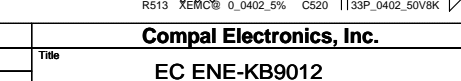
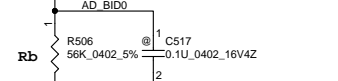
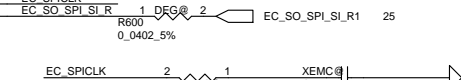
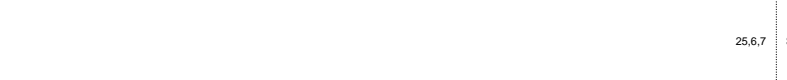
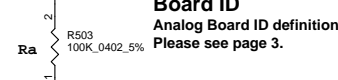
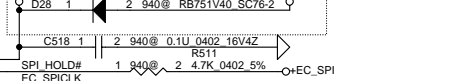
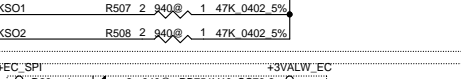
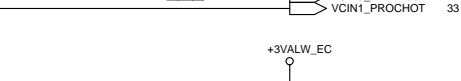
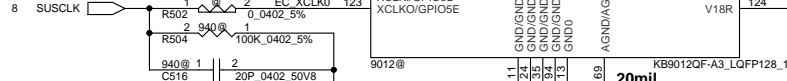
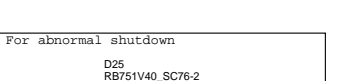
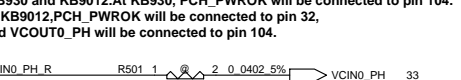
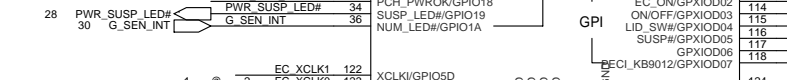
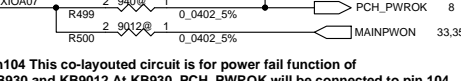
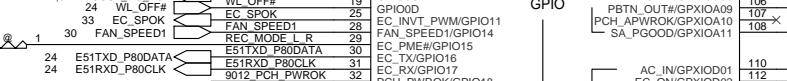
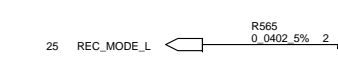
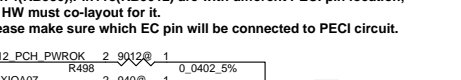
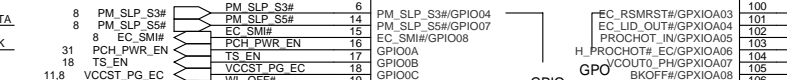
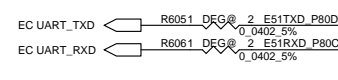
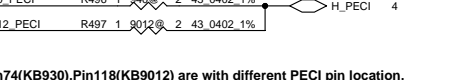
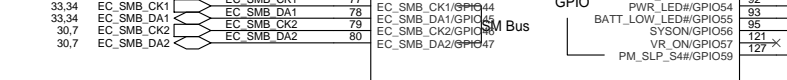
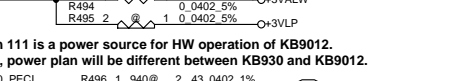
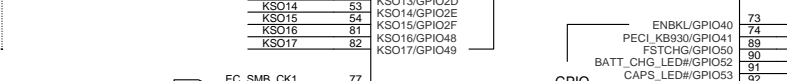
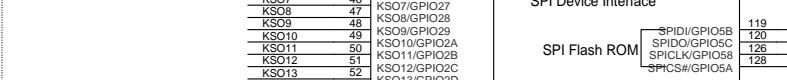
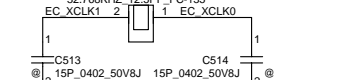
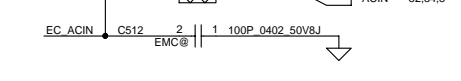
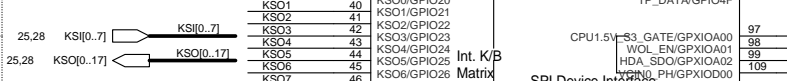
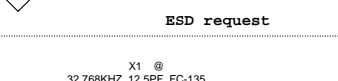
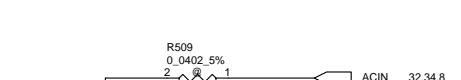
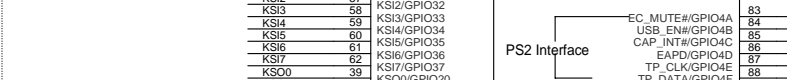
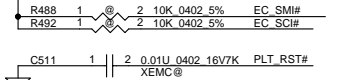
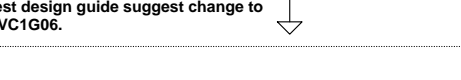
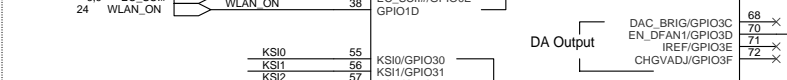
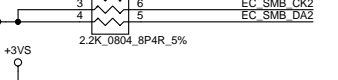
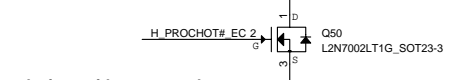
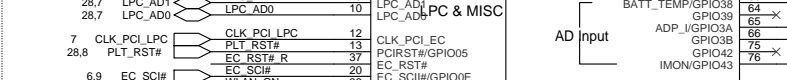
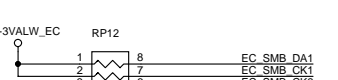
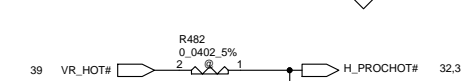
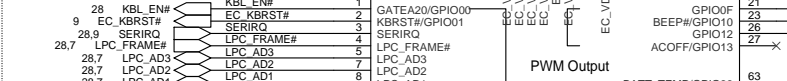
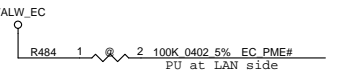
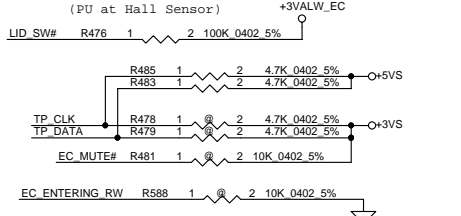
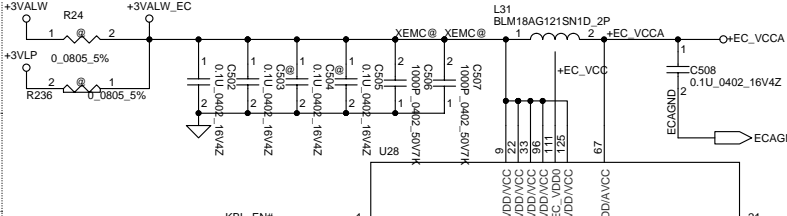
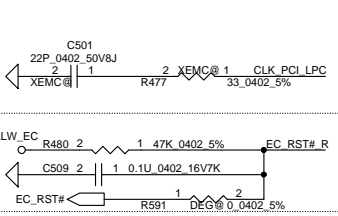


USB/B (USB Port 1, Port2)



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Size	Document Number	Rev	0.2		
Custom	V5WE2 M/B LA-9532P Schematic	Date:	Monday, April 08, 2013	Sheet	26 of 42

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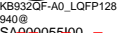
For abnormal shutdown
D25 RB751V40 SC76-2 PCH RSMRST#
D26 RB751V40 SC76-2 PCH PWROK

Board ID
Analog Board ID definition,
Please see page 3.

Follow KB930 checking List

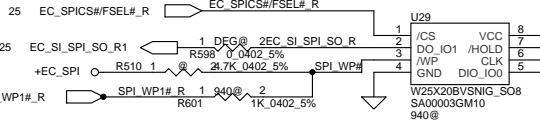


9012@



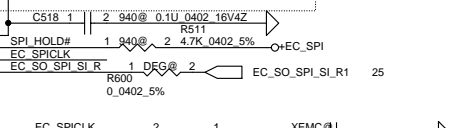
20mil

KB932&9012 Co-Layout Item
KB932 use 256KB ROM
KB9012 Embedded 128KB ROM



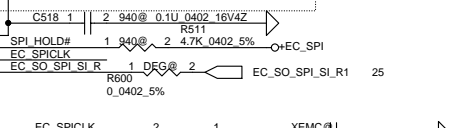
25 EC_SPICKL#_R EC_SPICKL#_R
25 EC_SI_SPI_SO_R1 DFG@ 2EC SI SPI_SO_R
+EC_SPI R510 1 2.7K 0.402 5% SPI W/P#
SUSP# 31,34,36,37,38 VCCST_PWRGD
118 9012 PECE

KB930&9012 Co-Layout Item
Pin 111 is a power source for HW operation of KB9012. So, power plan will be different between KB930 and KB9012.



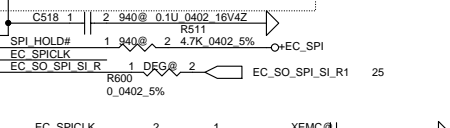
9012 PCH PWROK 2 9012@ 1 0.402 5%
GPXIOA07 2 940@ 1 0.402 5%
R499 2 940@ 1 0.402 5%
R500 2 9012@ 1 0.402 5%
MAINPWON 33,35
VCIN0_PH_R R501 1 2 0.402 5%
VCIN1_PROCHOT 33

Pin74(KB930), Pin118(KB9012) are with different PECE pin location, so HW must co-layout for it. Please make sure which EC pin will be connected to PECE circuit.



9012 PCH PWROK 2 9012@ 1 0.402 5%
GPXIOA07 2 940@ 1 0.402 5%
R499 2 940@ 1 0.402 5%
R500 2 9012@ 1 0.402 5%
MAINPWON 33,35
VCIN0_PH_R R501 1 2 0.402 5%
VCIN1_PROCHOT 33

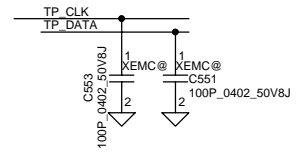
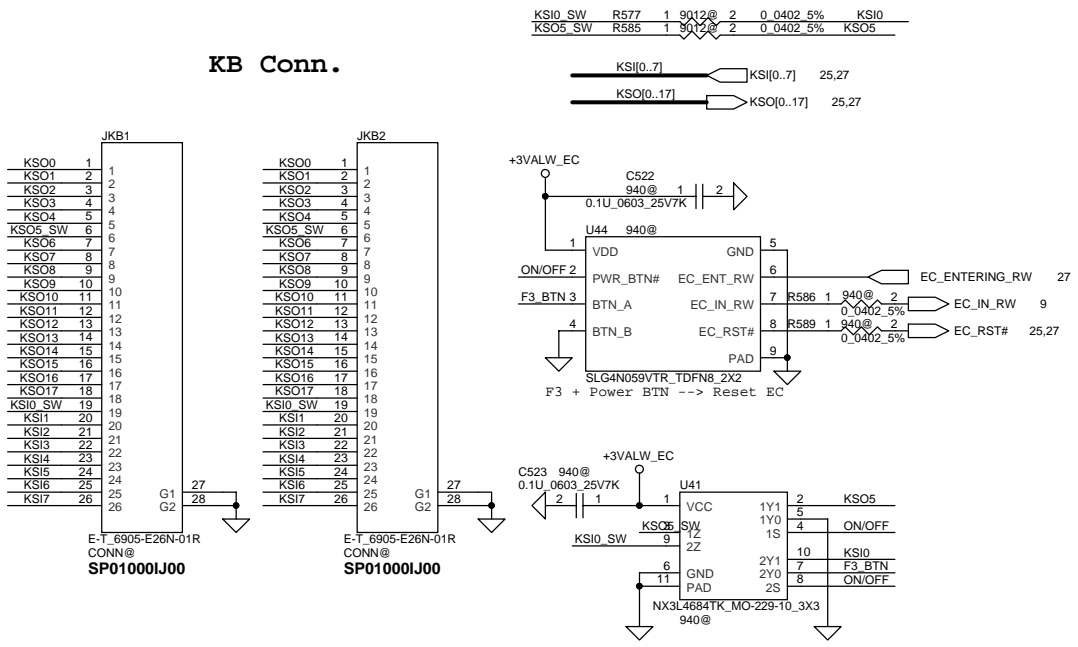
Pin114 is a power source for HW operation of KB930 and KB9012. At KB930, PCH_PWROK will be connected to pin 104. At KB9012, PCH_PWROK will be connected to pin 32, and VCOUT0_PH will be connected to pin 104.



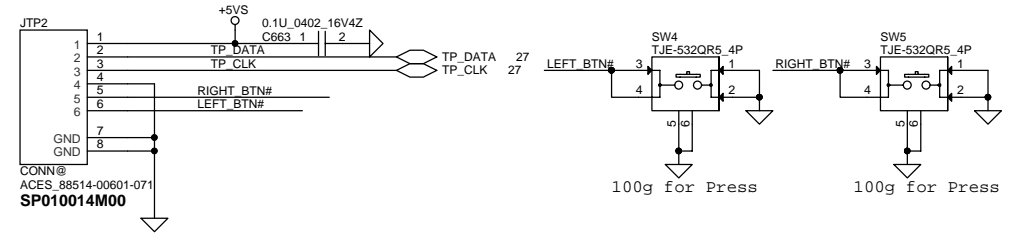
9012 PCH PWROK 2 9012@ 1 0.402 5%
GPXIOA07 2 940@ 1 0.402 5%
R499 2 940@ 1 0.402 5%
R500 2 9012@ 1 0.402 5%
MAINPWON 33,35
VCIN0_PH_R R501 1 2 0.402 5%
VCIN1_PROCHOT 33

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2012/07/10	Deciphered Date	2013/07/10	EC ENE-KB9012	
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Size	Document Number	Title		Rev	
Custom	V5WE2 M/B LA-9532P Schematic	EC ENE-KB9012		0.2	
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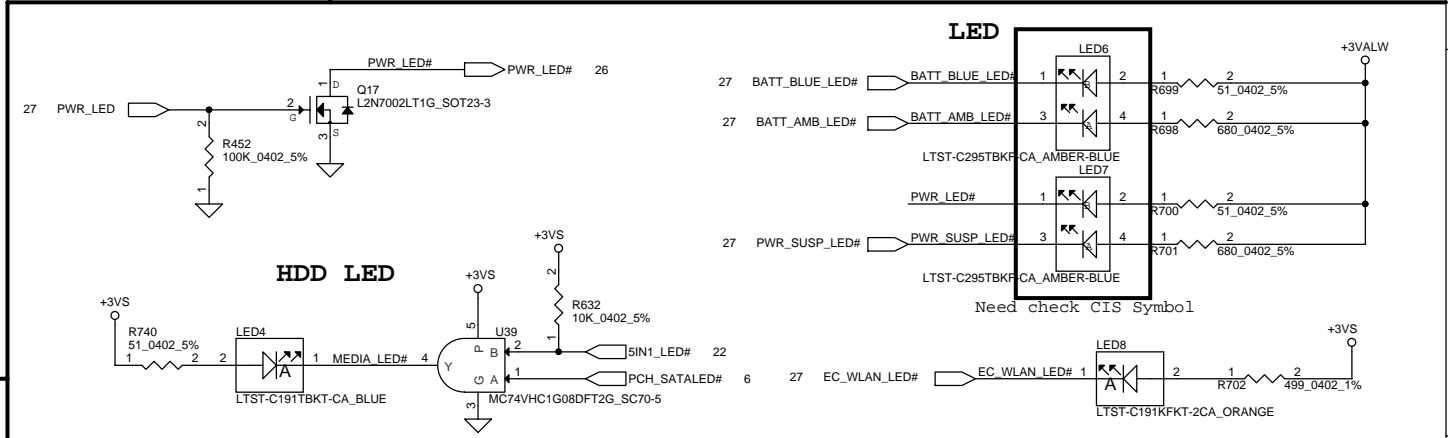
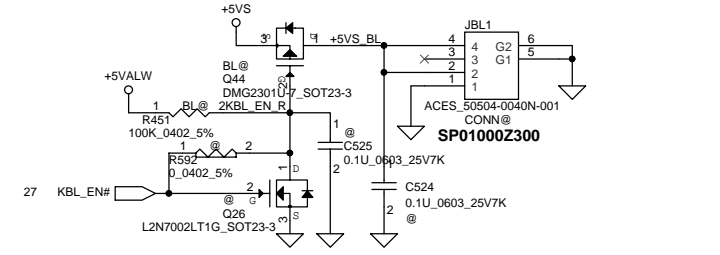
KB Conn.



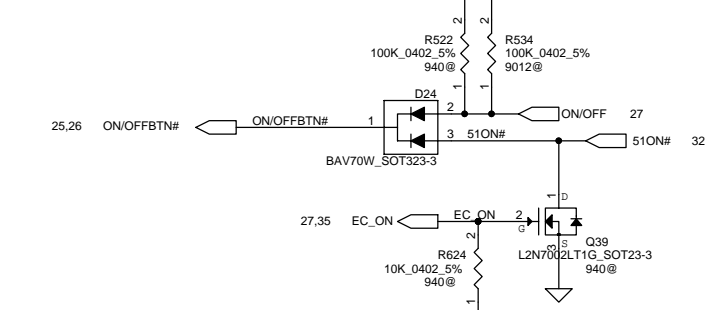
To TP/B Conn.



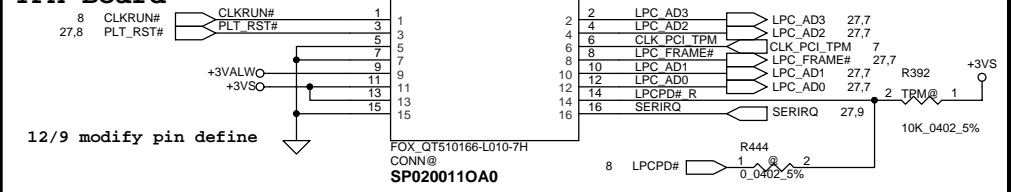
KB BackLight Conn.



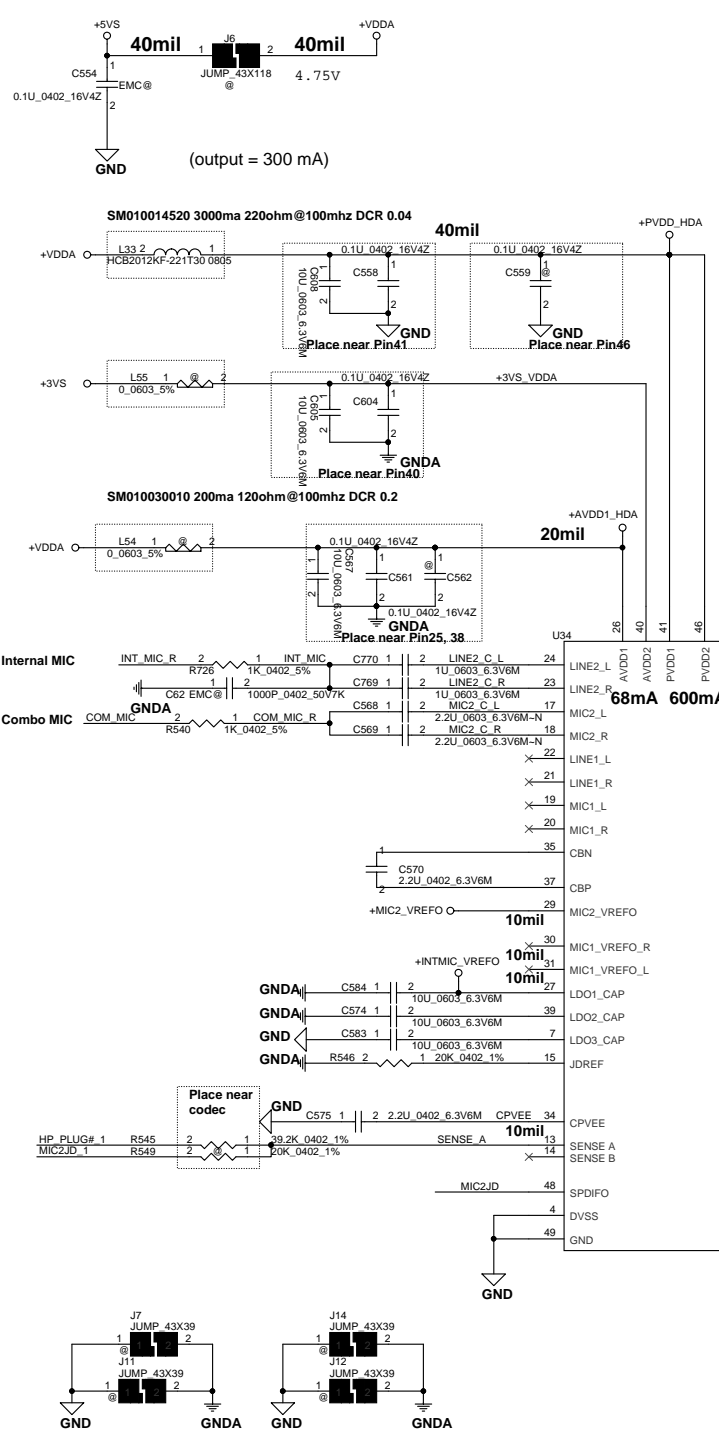
ON/OFF BTN



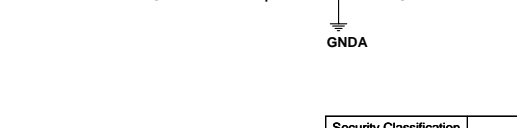
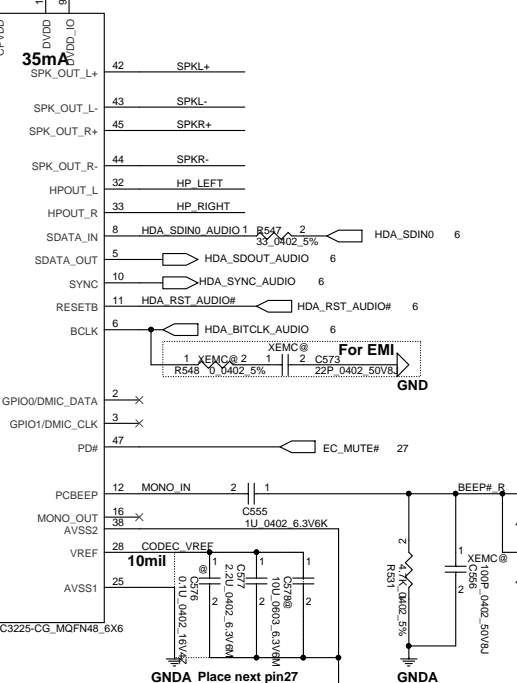
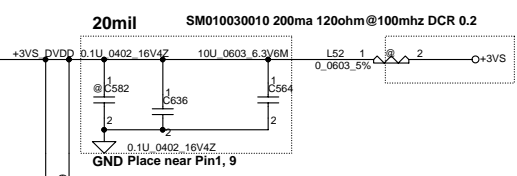
TPM Board



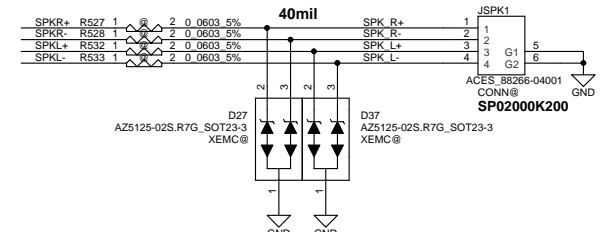
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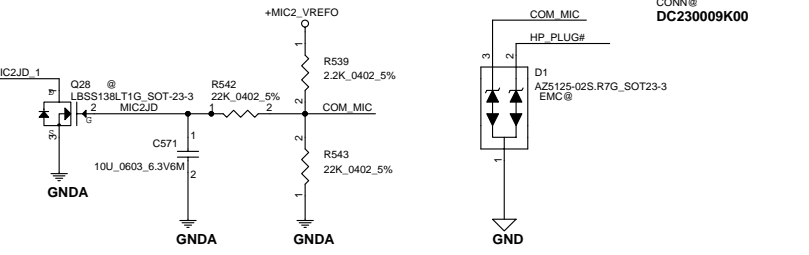
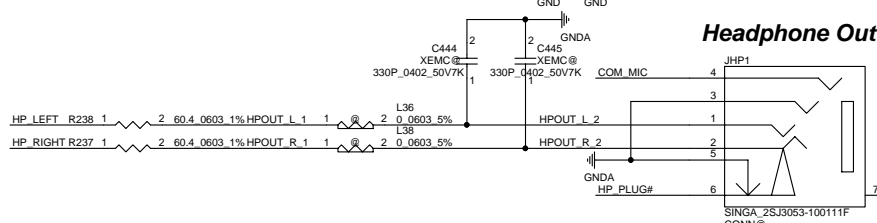
HD Audio Codec



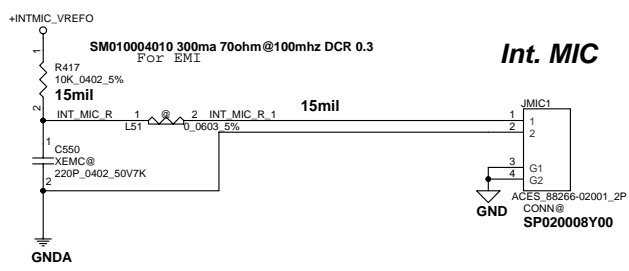
Int. Speaker Conn.



Headphone Out



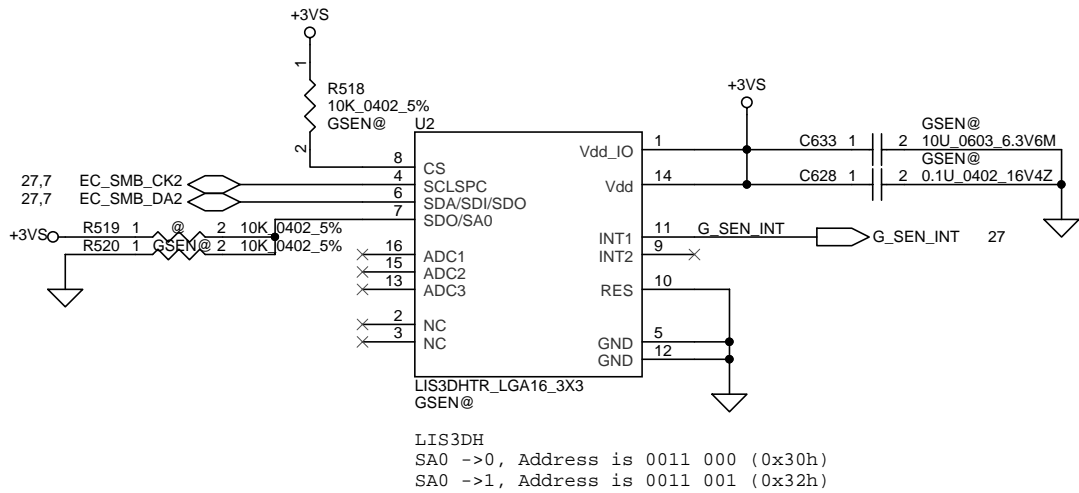
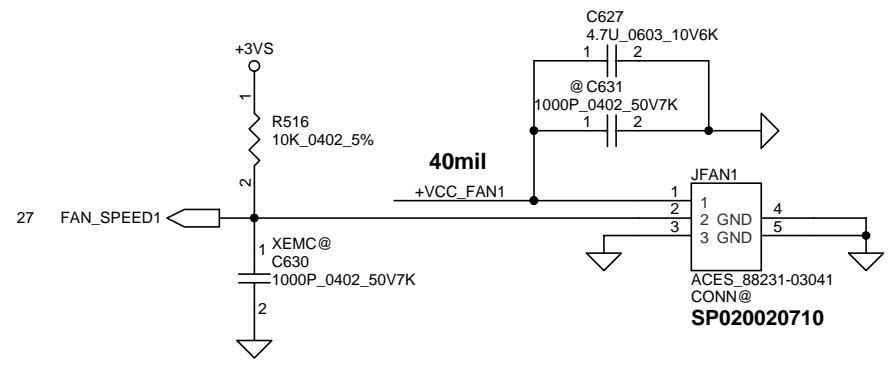
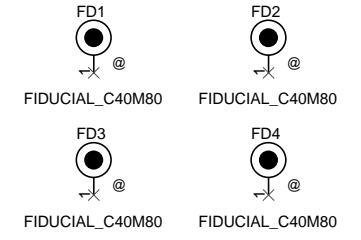
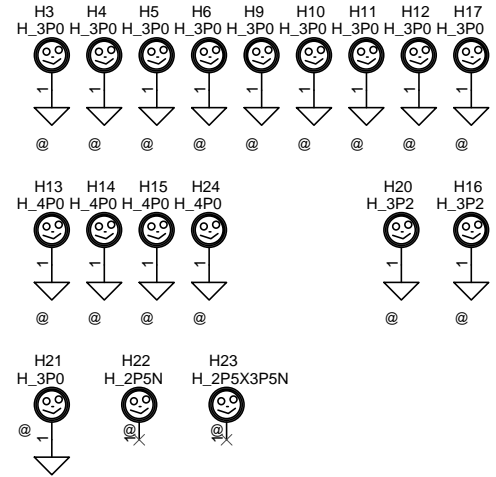
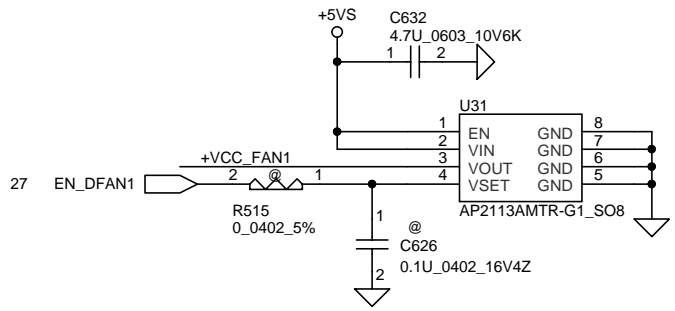
Int. MIC



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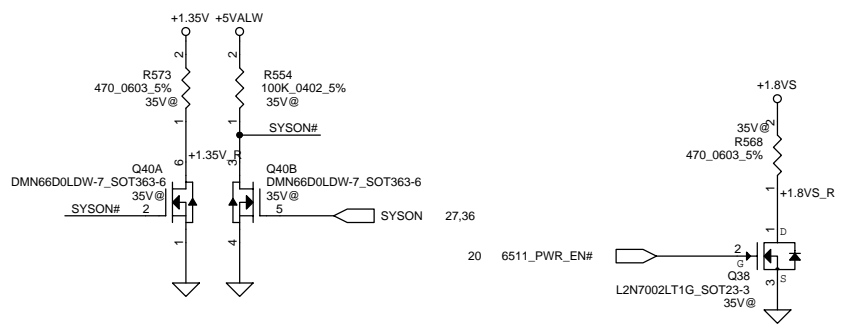
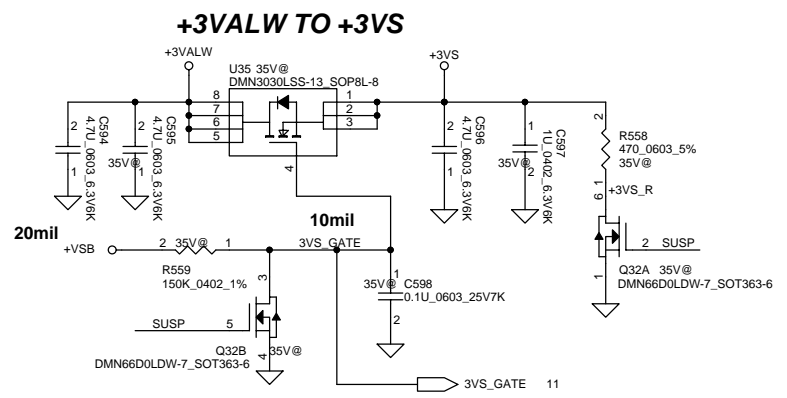
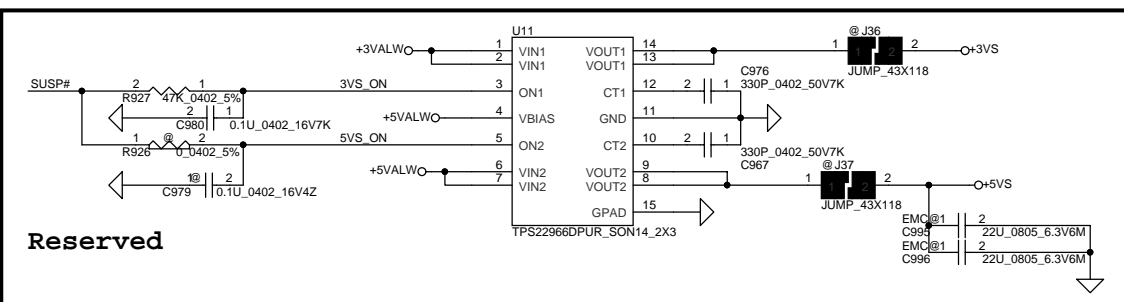
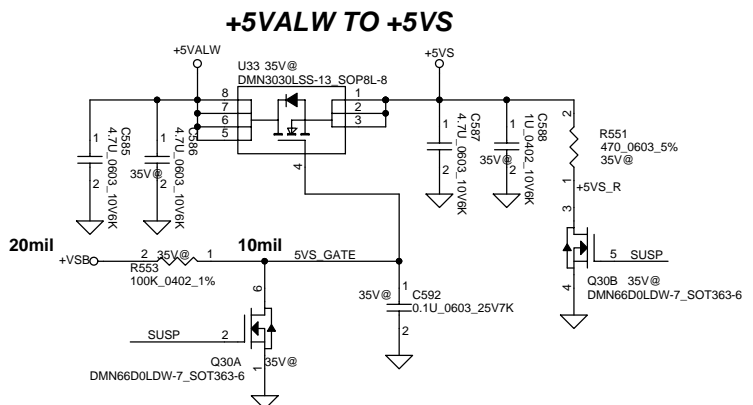
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FAN1 Conn

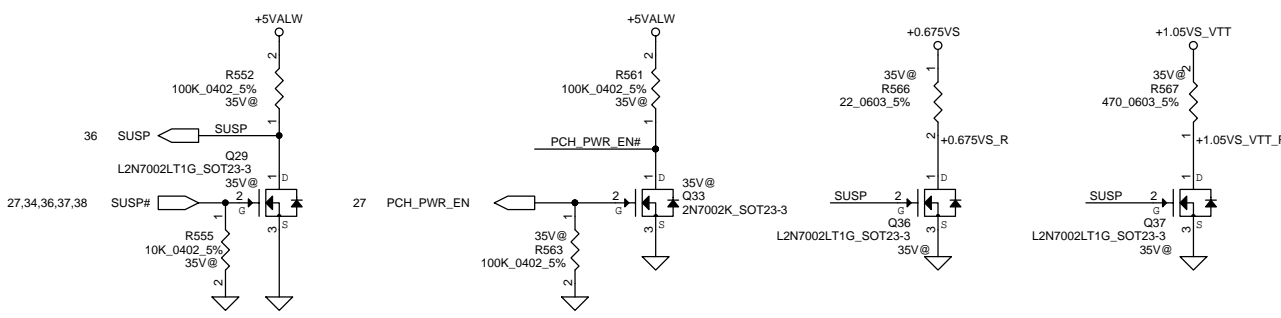
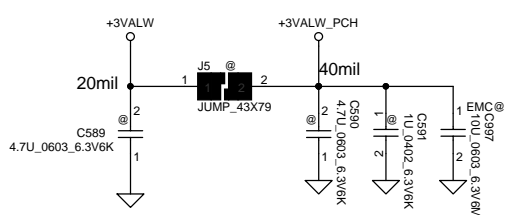


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Normal Platform (Not support M-STATE and Deep Sleep)

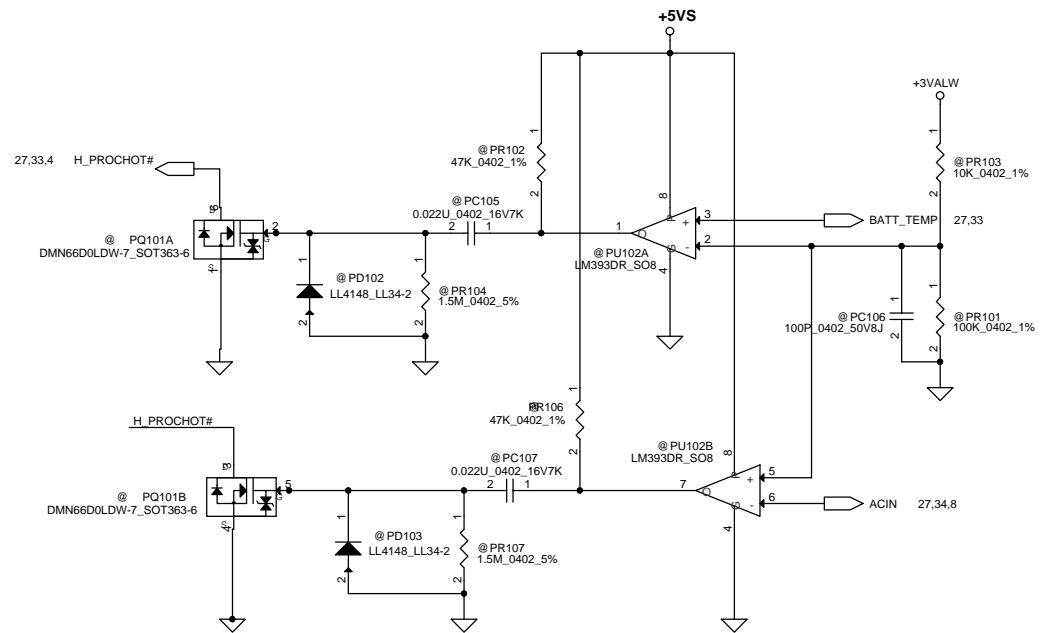
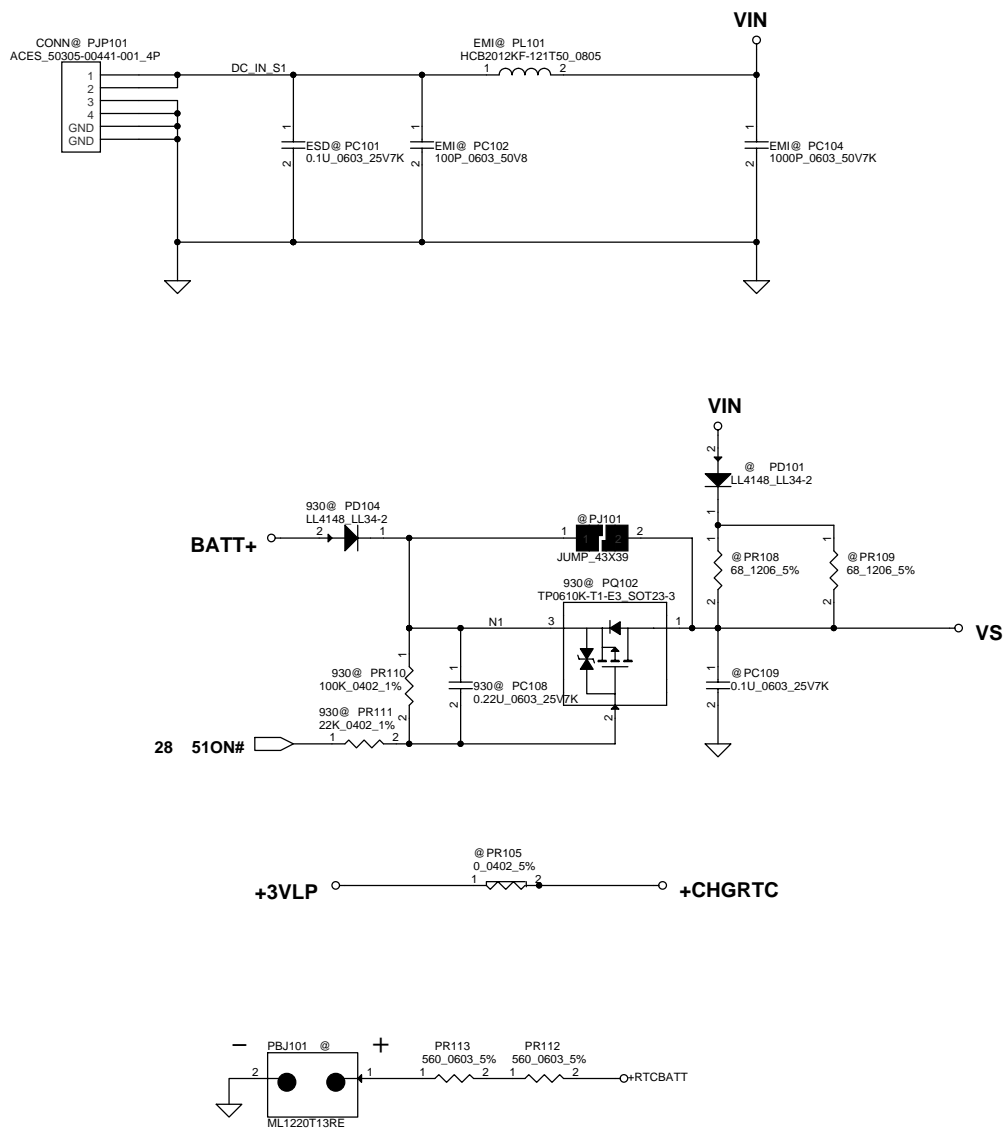


+3VALW TO +3VALW(PCH AUX Power)
Short J5 for PCH VCCSUS3.3



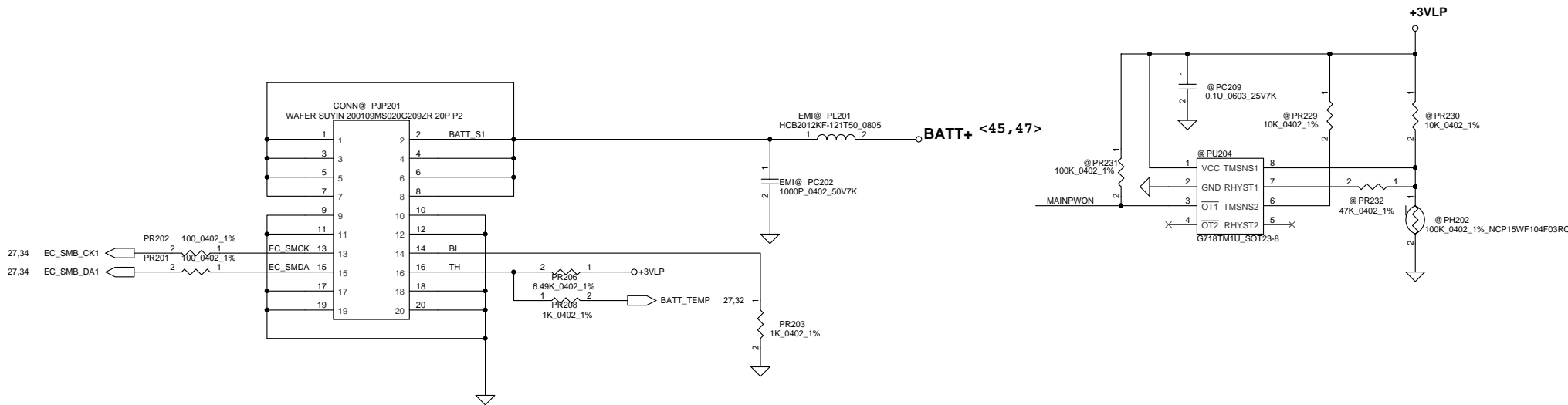
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DCIN			Document Number	0.2
V5WE2 M/B LA-9532P Schematic			Date	Monday, April 08, 2013
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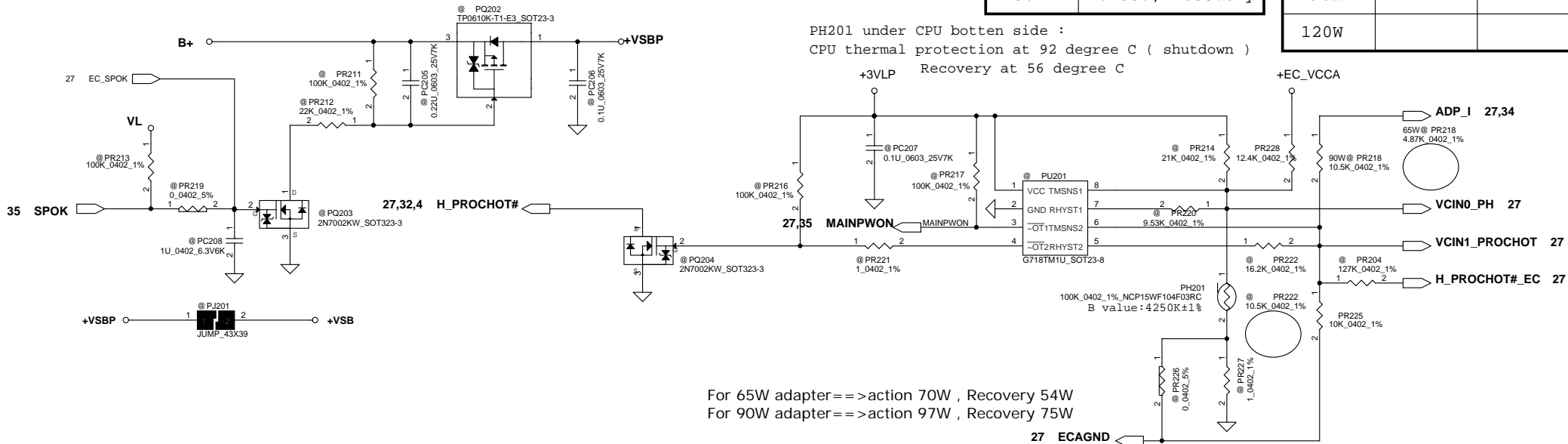
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For KB9012 OTP		
92	1.2V, Active	
56	2.255V, Recovery	

For KB9012 sense 20mΩ	Active	Recovery
65W	84W, 1.2V	56W, 0.793V
90W	117W, 1.2V	77W, 0.791V
120W		

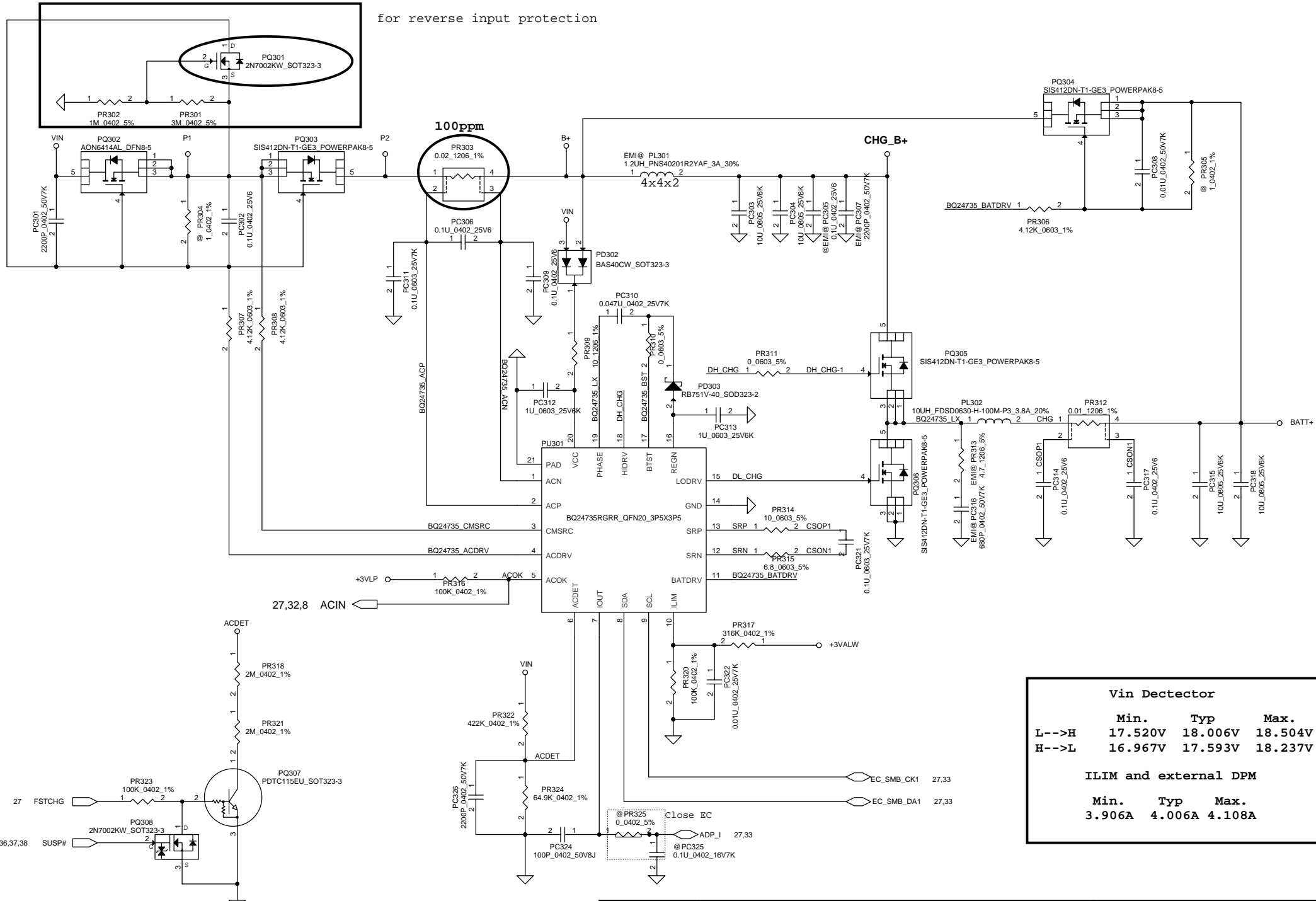
PH201 under CPU bottom side :
CPU thermal protection at 92 degree C (shutdown)
Recovery at 56 degree C



For 65W adapter ==> action 70W , Recovery 54W
For 90W adapter ==> action 97W , Recovery 75W

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				BATTERY CONN / OTP	
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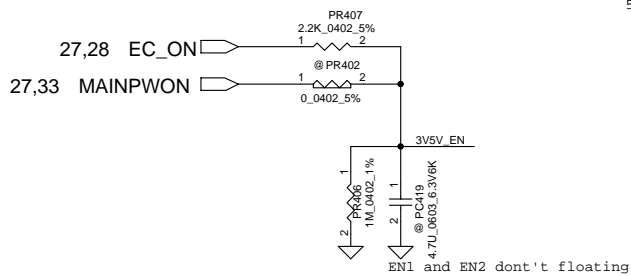
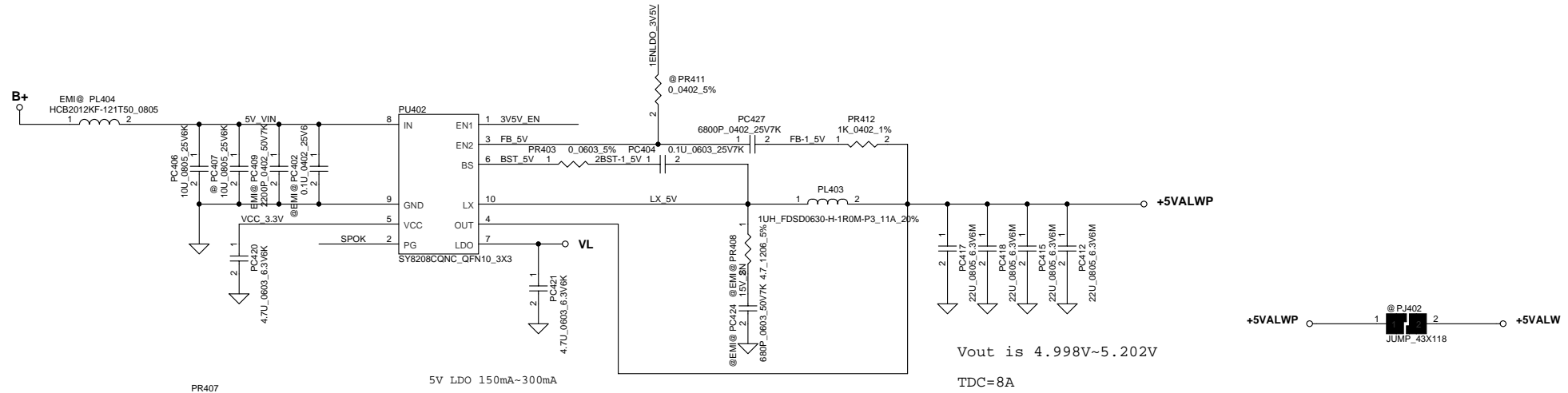
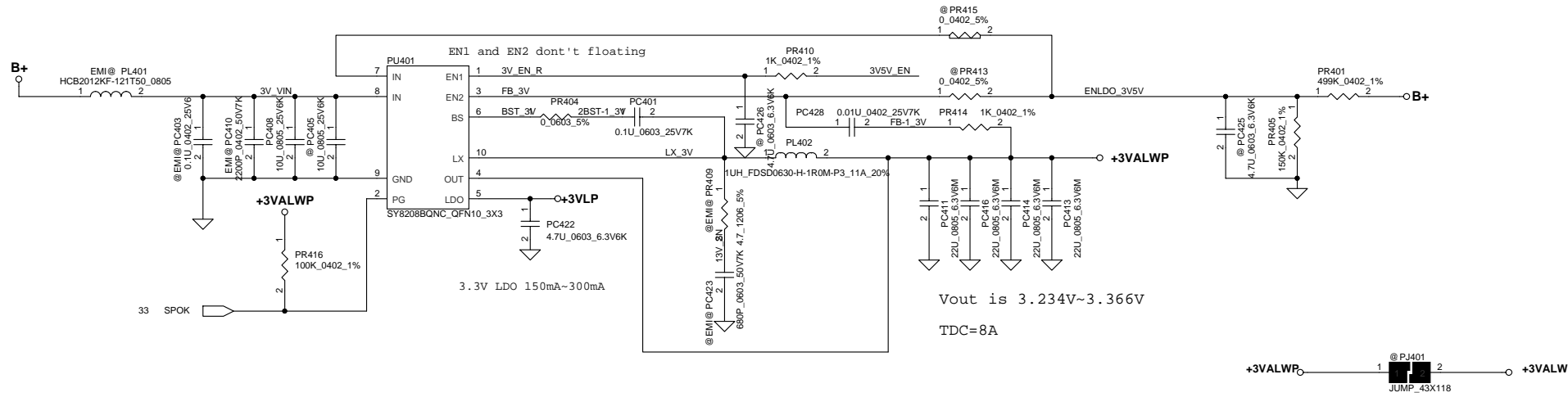
for reverse input protection



Vin Detector			
	Min.	Typ	Max.
L-->H	17.520V	18.006V	18.504V
H-->L	16.967V	17.593V	18.237V
ILIM and external DPM			
	Min.	Typ	Max.
	3.906A	4.006A	4.108A

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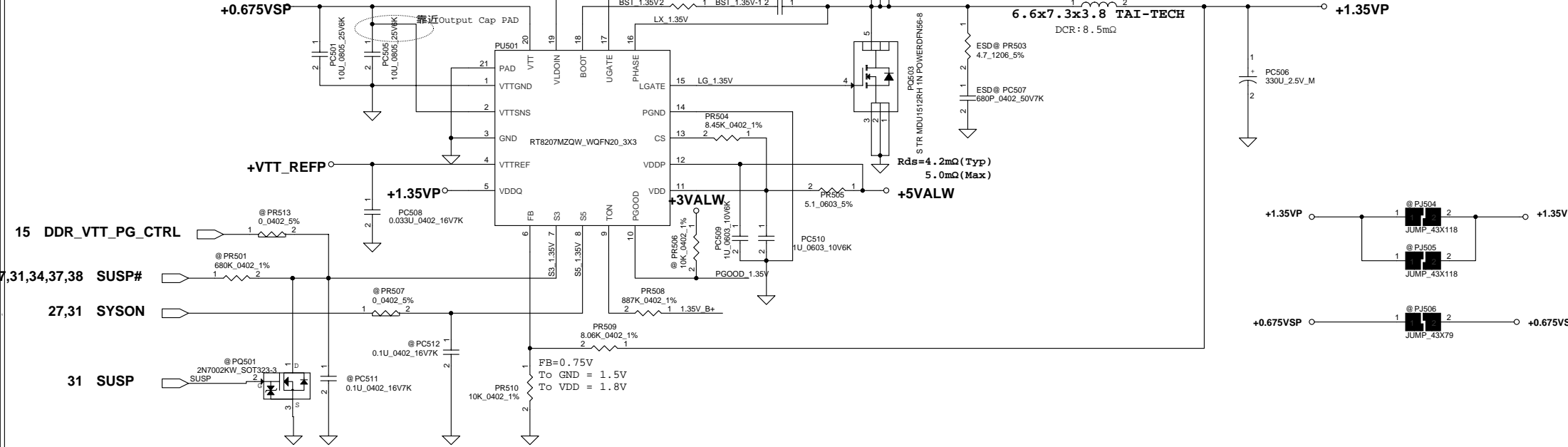
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+1.35VP
 $I_{peak} = \max\{0.7 * I_{budget}, 1st + 2nd \text{ max loading}\}$
 $I_{peak} = \max\{12.34 * 0.7, 4.2 + 8.14\}$
 $I_{peak} = 12.34A ; 1.2I_{peak} = 14.808A ; I_{max} = 8.638A$
 $1/2\Delta I = 0.7353A (F=300K \text{ Hz})$
 $PR504 = (1.2I_{peak} - 1/2\Delta I) * R_{ds(on)}(max) * 1.2 / 9uA = 8.45Kohm$
 choose $PR504 = 8.45Kohm$ (for safety $> 1.2I_{peak}$)
 $R_{ds(on)} = 5.0m \text{ ohm}(max) ; R_{ds(on)} = 4.2m \text{ ohm}(typical)$
 $I_{limit_min} = (8.366K * 9uA) / (5.0m * 1.2) = 15.058A$
 $I_{limit_max} = (8.535K * 11uA) / (4.2m * 1.2) = 22.352A$
 $I_{ocp} = I_{limit} + 1/2\Delta I = 15.79A \sim 23.09A$
 $I_{ocp}(min) > 1.2I_{peak}$

2011/9/19

OVP=110% 115% 120%



15 DDR_VTT_PG_CTRL

7,31,34,37,38 SUSP#

27,31 SYSON

31 SUSP

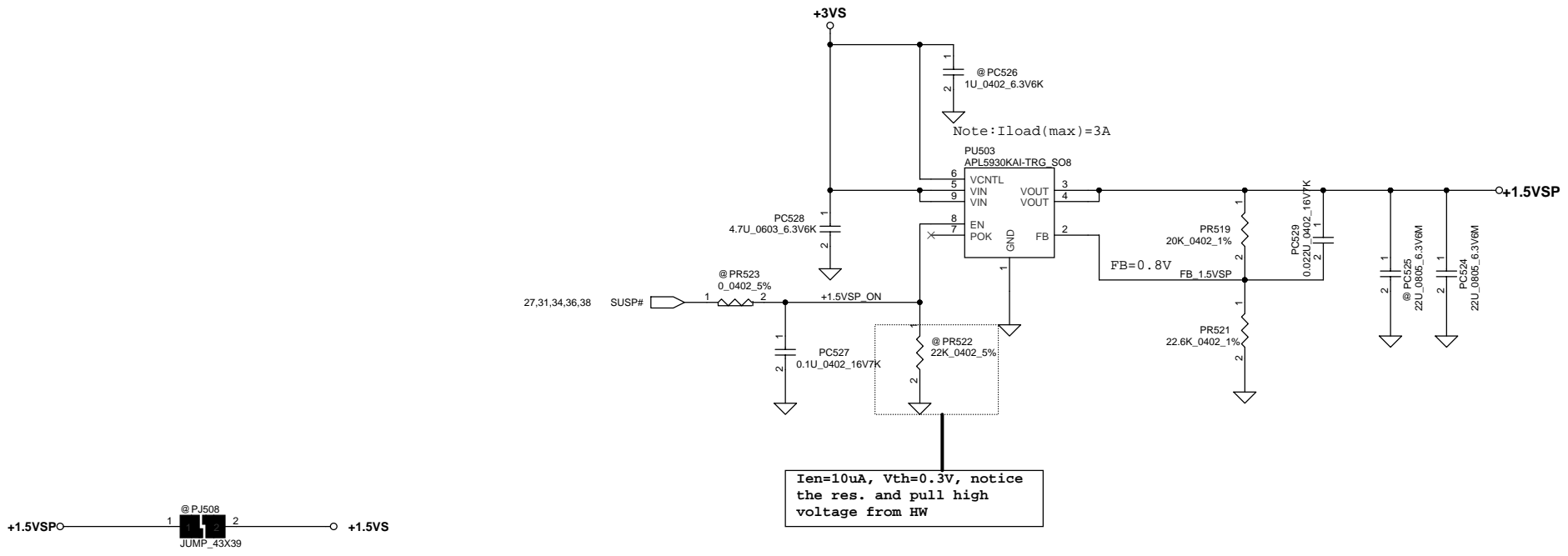
STATE	S3	S5	1.35VP	VTT_REFP	0.675VSP
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off (Discharge)	Off (Discharge)	Off (Discharge)

Note: S3 - sleep ; S5 - power off

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Issued Date	2012/07/10	Deciphered Date	2013/07/10	1.35VP/0.675VSP	
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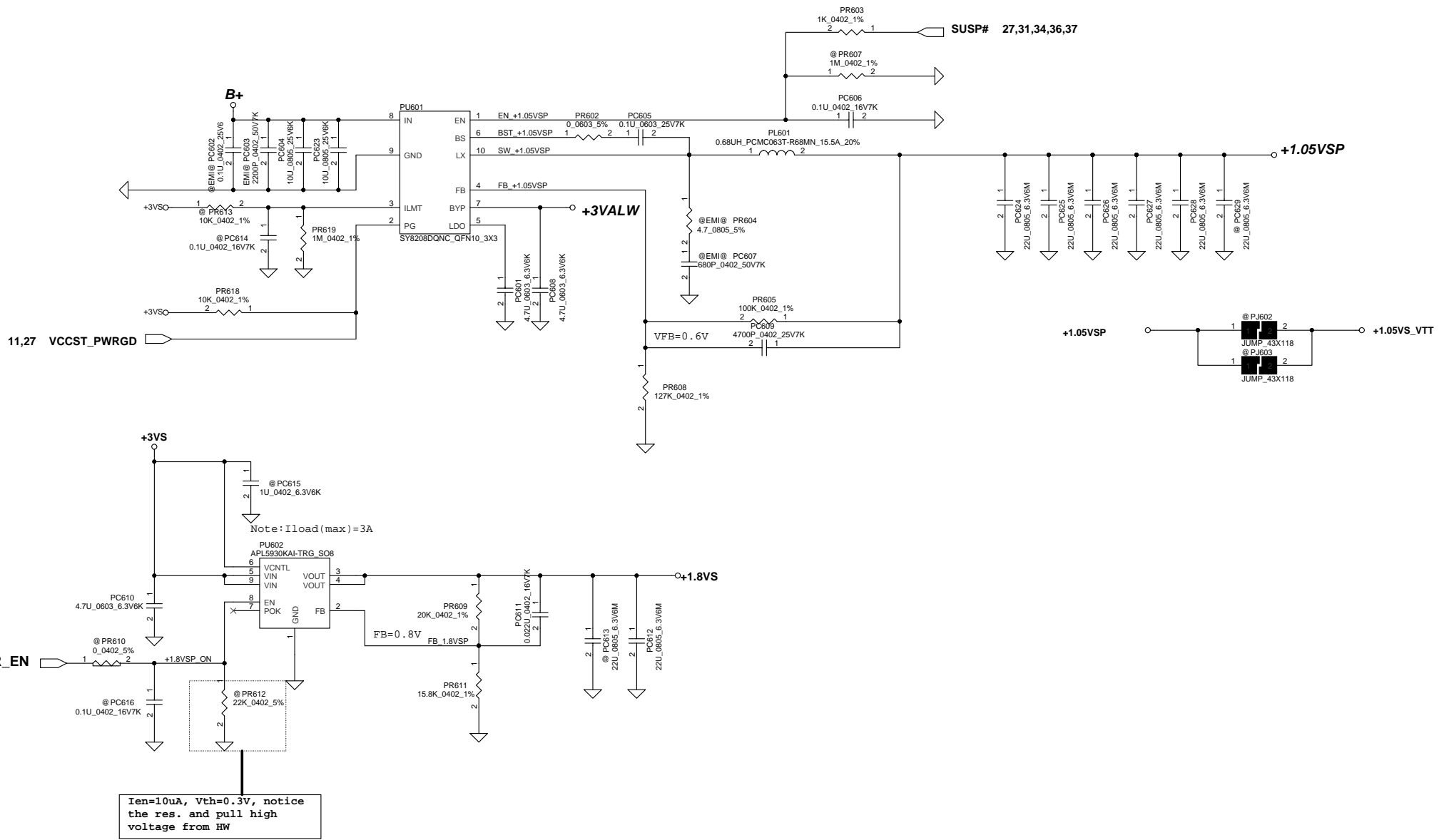
Note: Use VCCSA_SEL to switch High & Low Level of VTT...



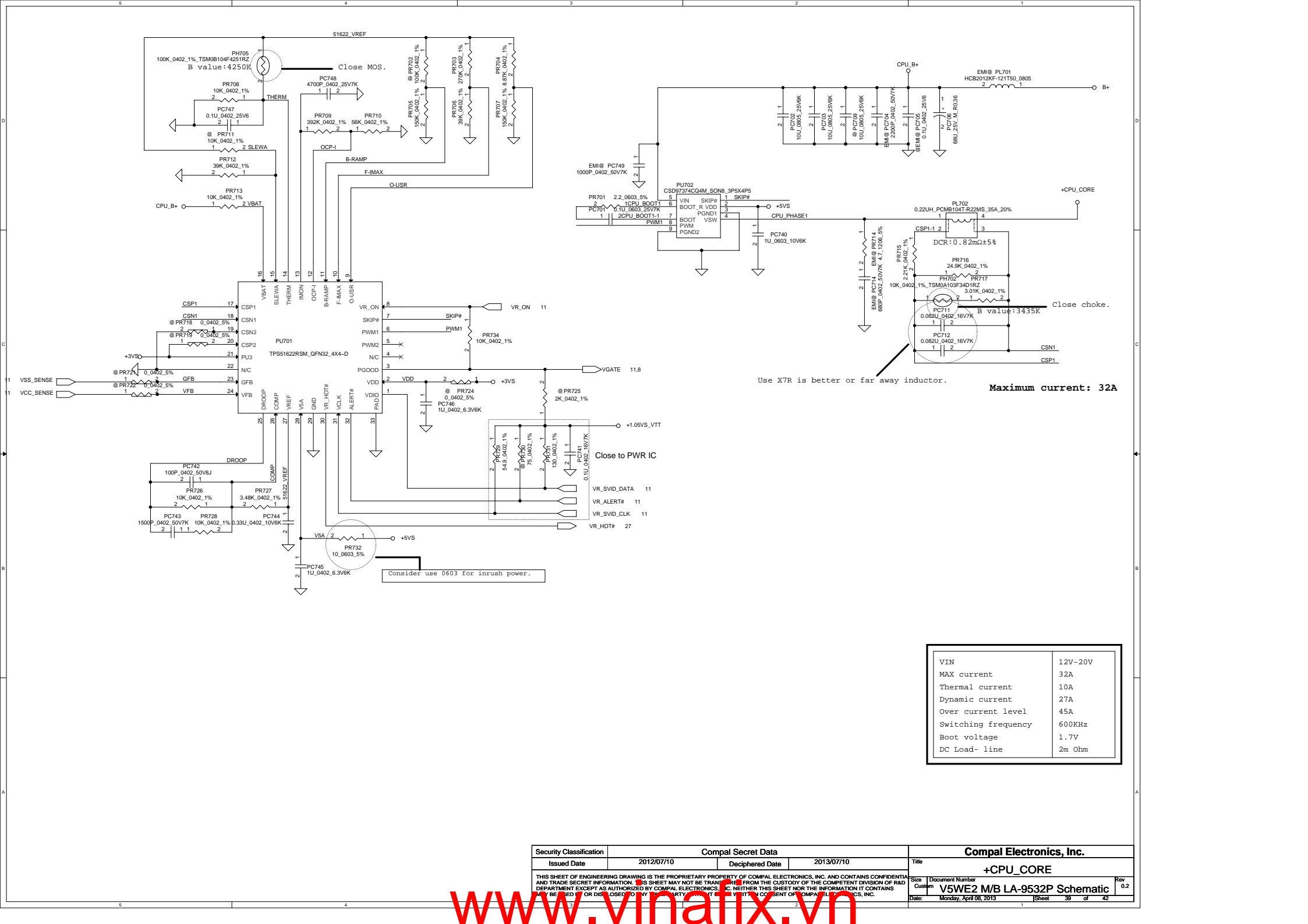
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+1.05VSP Ipeak=5.36A ; I_{max}=3.752A ; 1.2I_{peak}=6.432
 Delta I=0.0000A => 1/2 Delta I = 0.0000A, F = 800K Hz (typ)



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Use X7R is better or far away inductor.

Maximum current: 32A

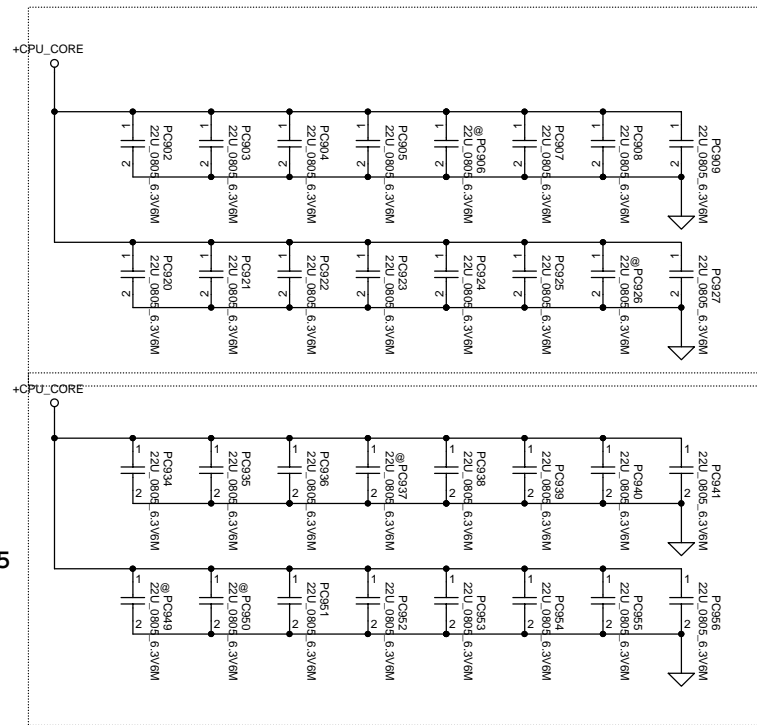
Consider use 0603 for inrush power.

VIN	12V-20V
MAX current	32A
Thermal current	10A
Dynamic current	27A
Over current level	45A
Switching frequency	600KHz
Boot voltage	1.7V
DC Load-line	2m Ohm

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				+CPU_CORE	
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PWR Rule
 CPU DCLL=1.5m ohm dedign 330uF/9m *0, 22uF *30



22u * 27, @*5

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Module Design	Module Design change 3/5V solution		3/5V		11/13	DVT
2		Change RTC type to non-charge		31	Un-pop PR112, PR113	11/13	DVT
3	TPS51622 update to ES2.1	Compensation modify		39	Change PR701 to 2.2, PR703 to 270K, PR727 to 3.48K Un-pop PC742	11/16	DVT
4	EMI request	Cut-in EMI solution		EMI	Add PR313, PC316, PR714, PC714, PC749	11/20	DVT
5	EMI request	EMI confirm remove		EMI	Delete PL102, PC103, PC101, PL202, PC201 and PL703	11/26	DVT
6	Costdown			35	Change PL402, PL403 from 5x5x3 to 7x7x3	12/13	DVT2
7		SY8208B/C update		35	Add PR411, PR413	12/22	DVT2
8	+1.05V ripple close upper and mean too low	Adjust output voltage and add Cff		36	Add PC609 into 4700P Change PR608 from 133K to 127K	12/22	DVT2
9		Improve CPU transient character		40	Unpop PC926	01/09	DVT2
10		Tune sequence		35	Change PC428 from 4700p to 10n, PC427 from 0.047u to 6.8n	02/04	PVT
11		0 ohm reduce			Change PR507, PR513, PR523 to R-pad	02/22	PVT
12		Provide 3/5V PG signal to EC		35	Add PR416	02/22	PVT
13	ESD request			32	Add PC101 into 0.1uF	02/26	PVT
14	ESD request			36	Add PC521, PR503, PC507	02/26	PVT
12							
13							
14							
15							
16							
17							

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