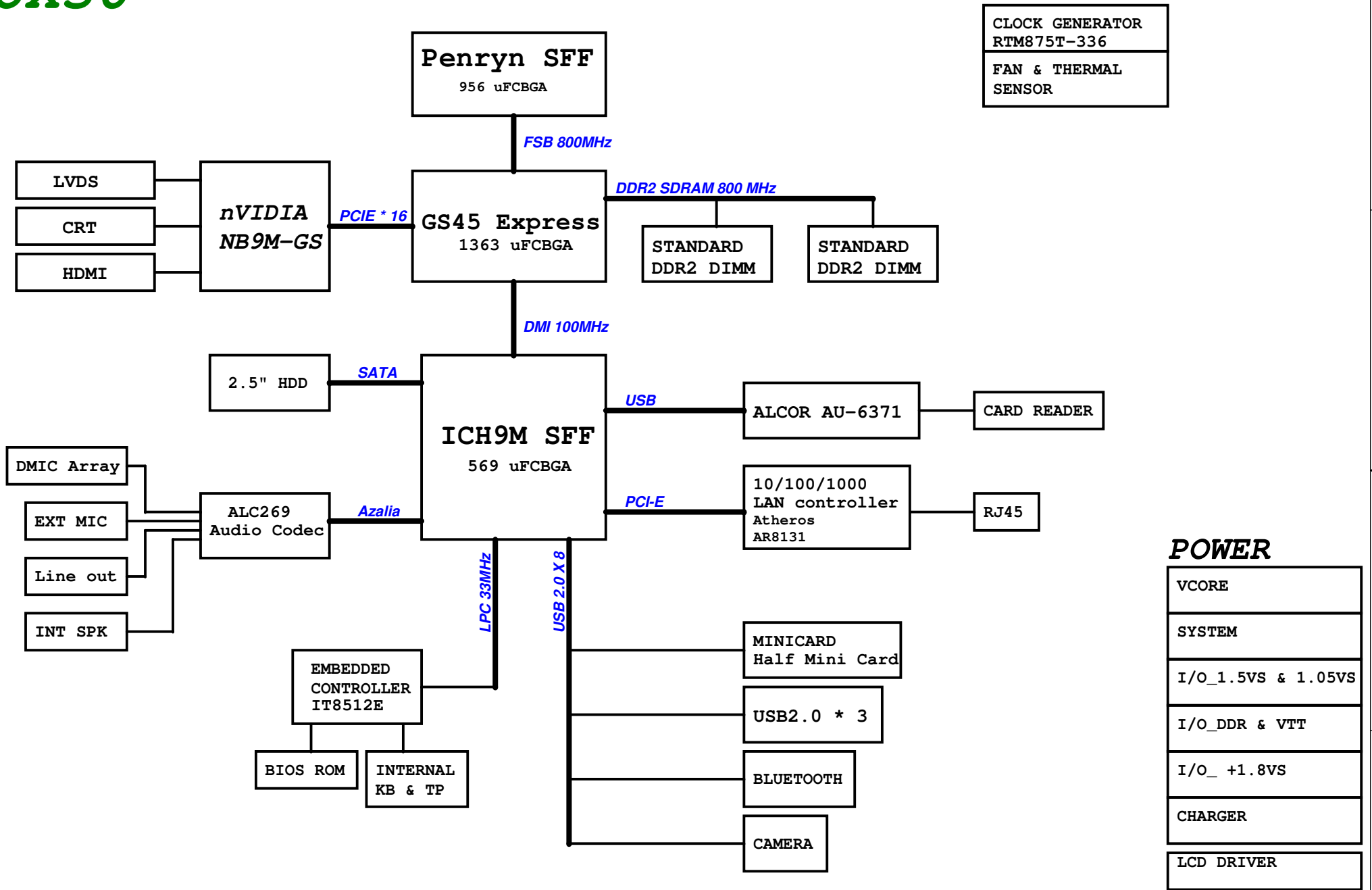


UX50

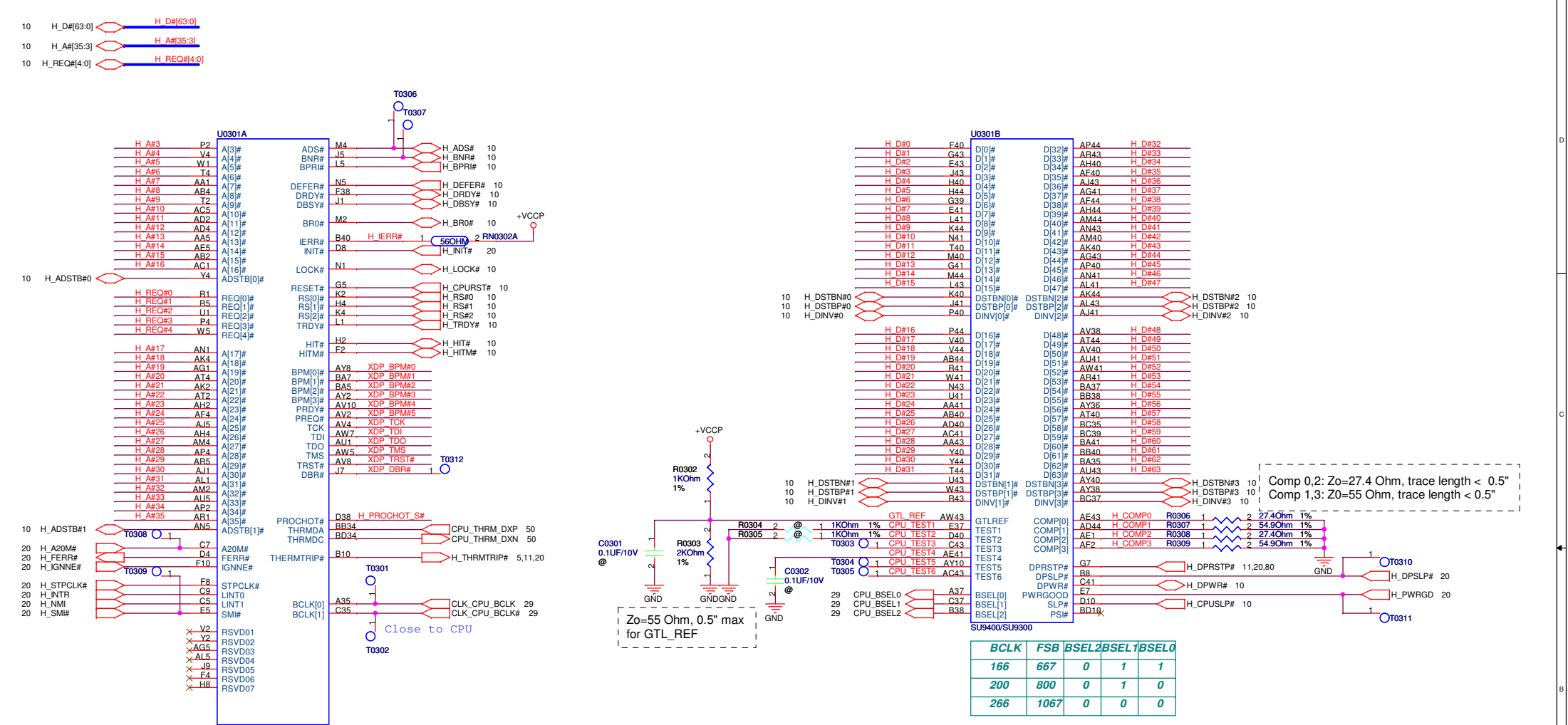


POWER

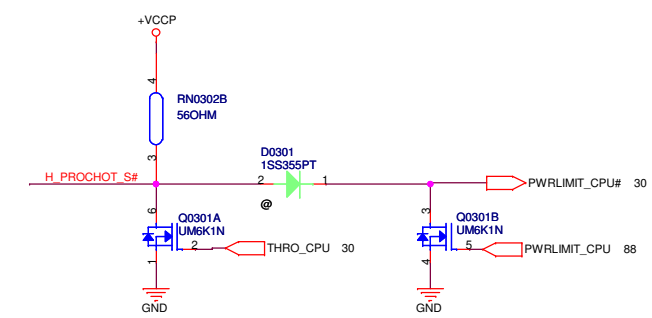
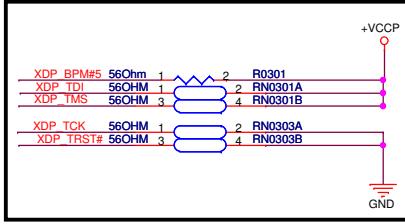
VCORE
SYSTEM
I/O_1.5VS & 1.05VS
I/O_DDR & VTT
I/O_ +1.8VS
CHARGER
LCD DRIVER

<Variant Name>

ASUS		Title : Block diagram
ASUSTeK COMPUTER INC		Engineer: Tony Su
Size Custom	Project Name UX50	Rev 1.0a
Date: Tuesday, March 31, 2009	Sheet 1 of 97	

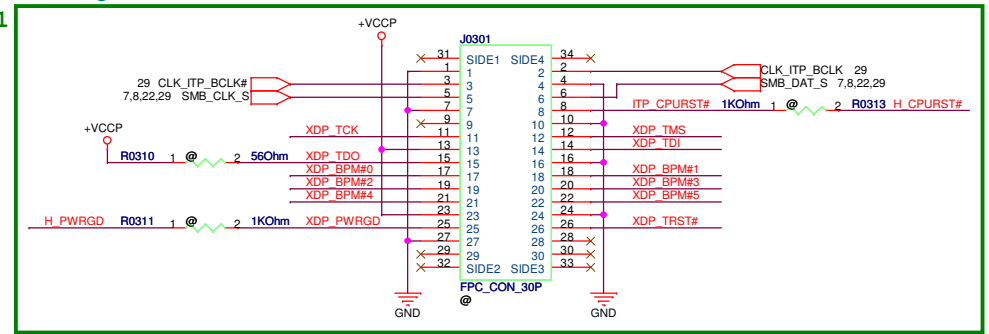


Default Strapping When Not Used



BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1067	0	0	0

ITP Debug Port
R1.1



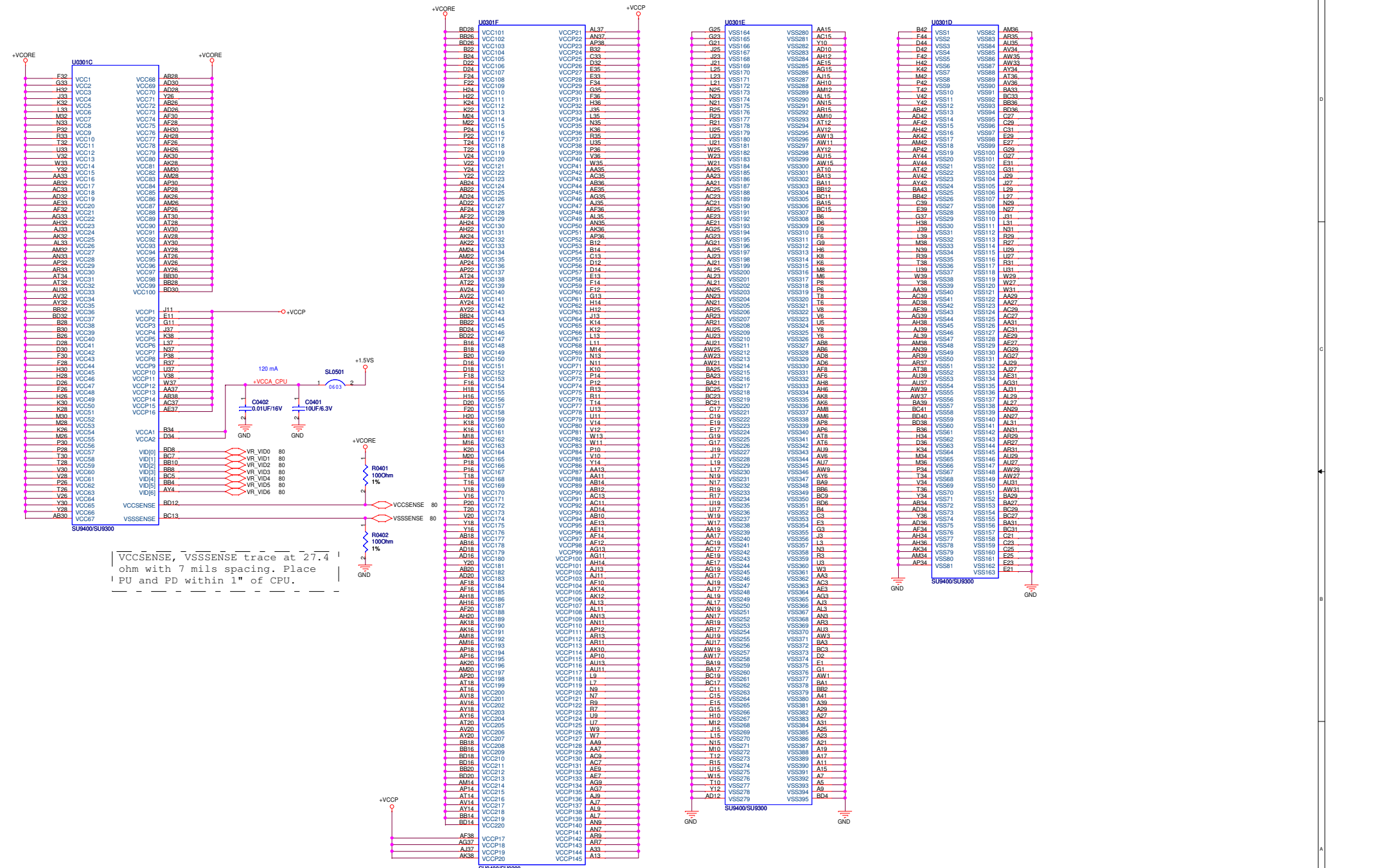
-Variant Name-

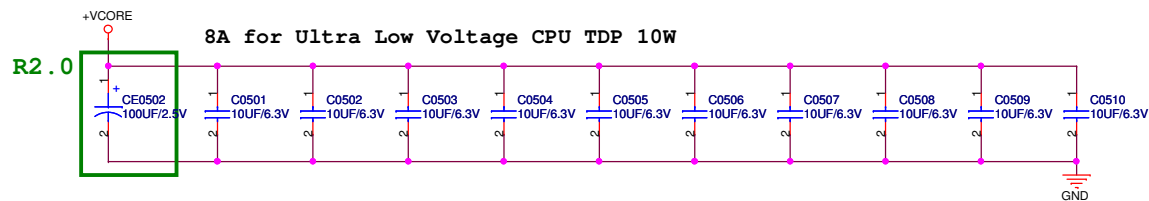
ASUS Title : CPU PENRYN ULV FSB

ASUSTek COMPUTER INC Engineer: Tony Su

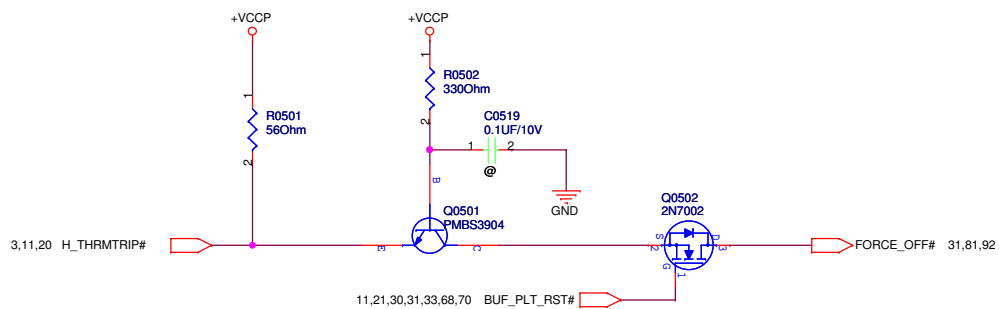
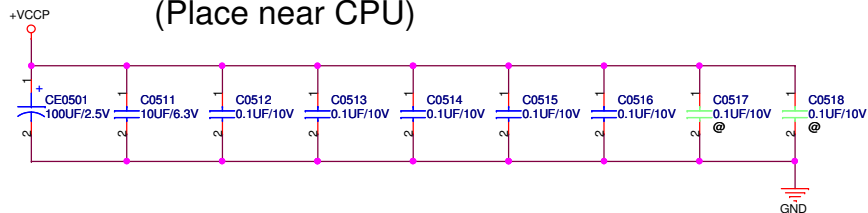
Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 3 of 97





**+VCCP Decoupling Capacitor
(Place near CPU)**



Decoupling guide from Intel

V CORE	10uF mount	*4pcs
	0.1uF mount	*5pcs
VCCP	1uF	*12pcs
	270uF	*1pcs
VCCA	0.01uF	*1 pcs
	10uF	*1 pcs

<Variant Name>

ASUS		Title :CPU CAPACITORS
ASUSTeK COMPUTER INC		Engineer: Tony Su
Size Custom	Project Name UX50	Rev 1.0a
Date: Tuesday, March 31, 2009	Sheet	5 of 97

5

4

3

2

1

D

D

C

C


B

B

A

A

<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: Tony Su
Size Custom	Project Name UX50	Rev 1.0a
Date: Tuesday, March 31, 2009		Sheet 6 of 97

5

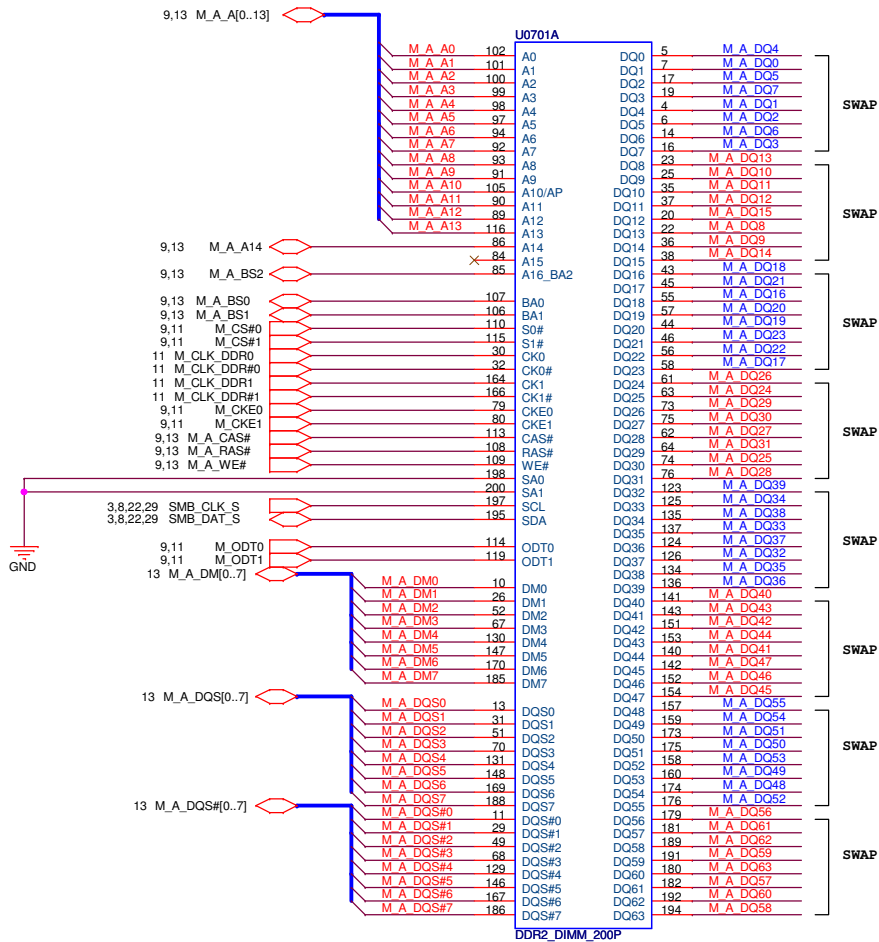
4

3

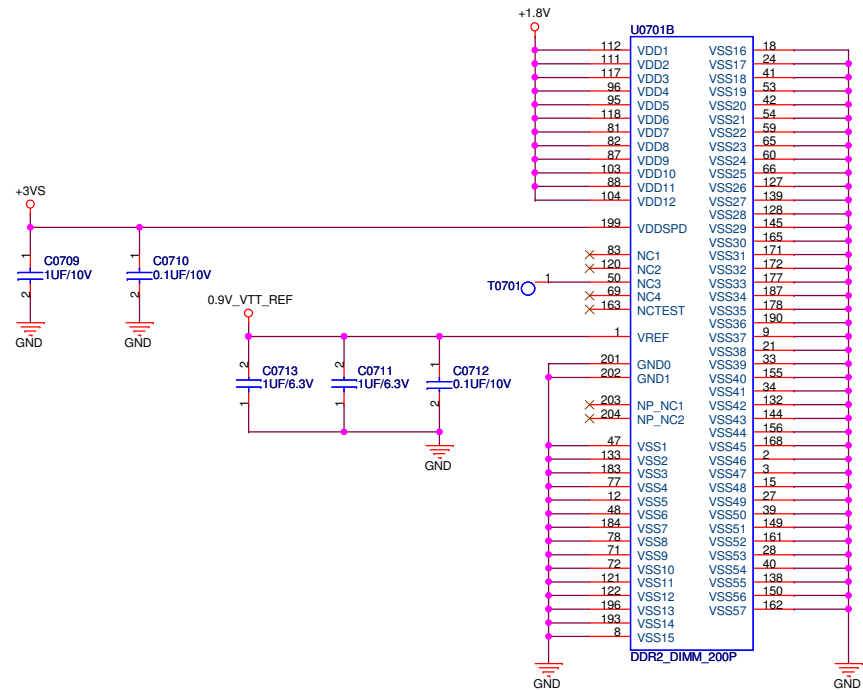
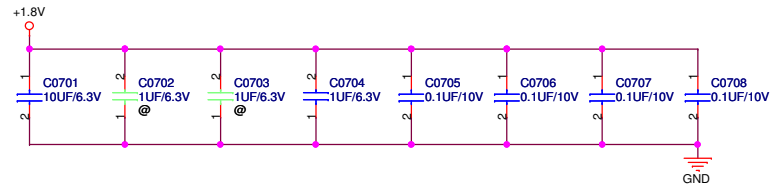
2

1

13 M_A_DQ[0..63] M A DQ[0..63]

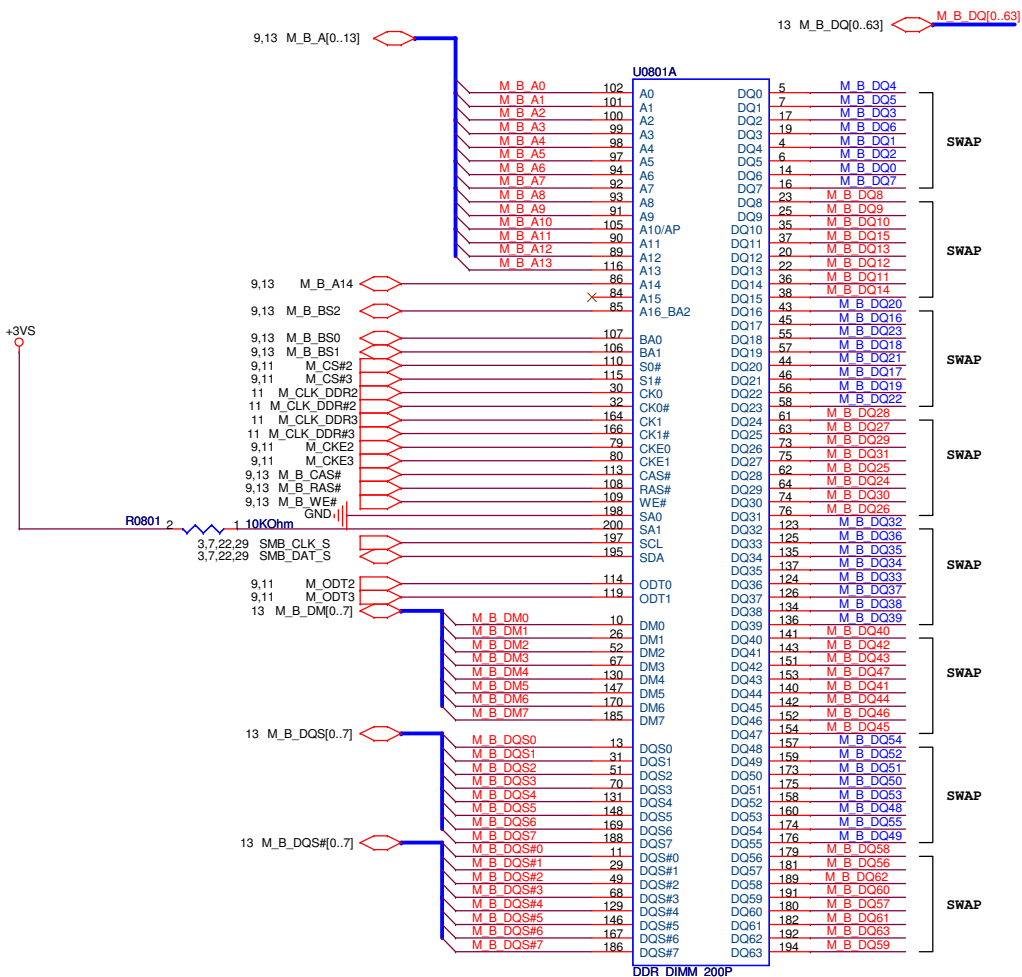


PN : 12G02512200Y (STD Type)

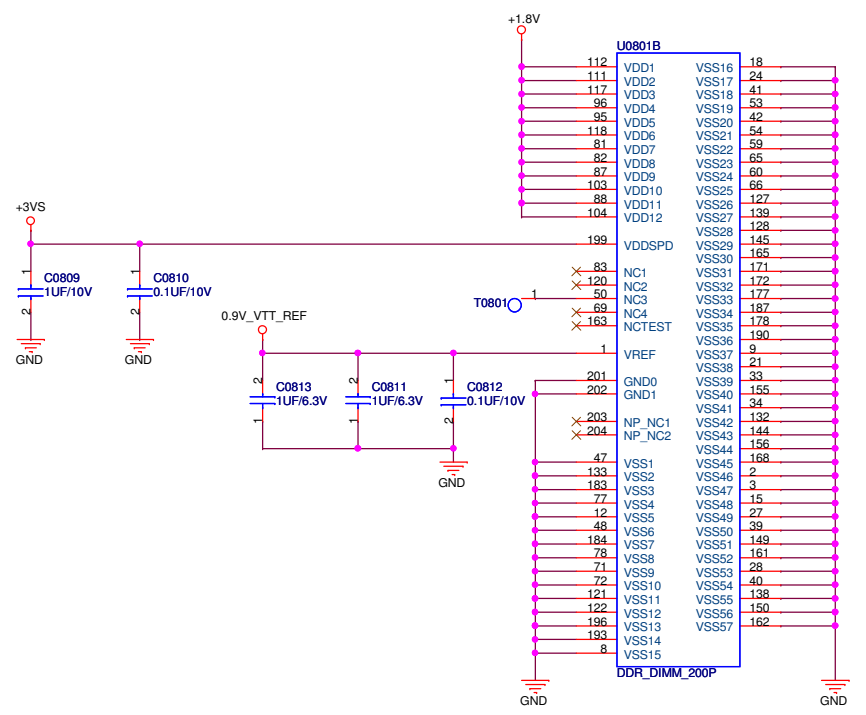
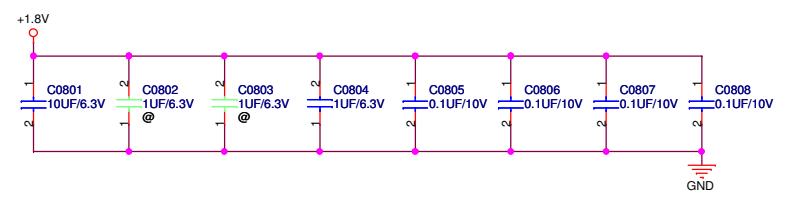


<Variant Name>

ASUS		R2-60 DIMM CHANNEL A	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size	Project Name	Rev	
Custom	UX50	1.0a	
Date: Tuesday, March 31, 2009	Sheet	7	of 97



PN: 12G02512200G (REV. Type)

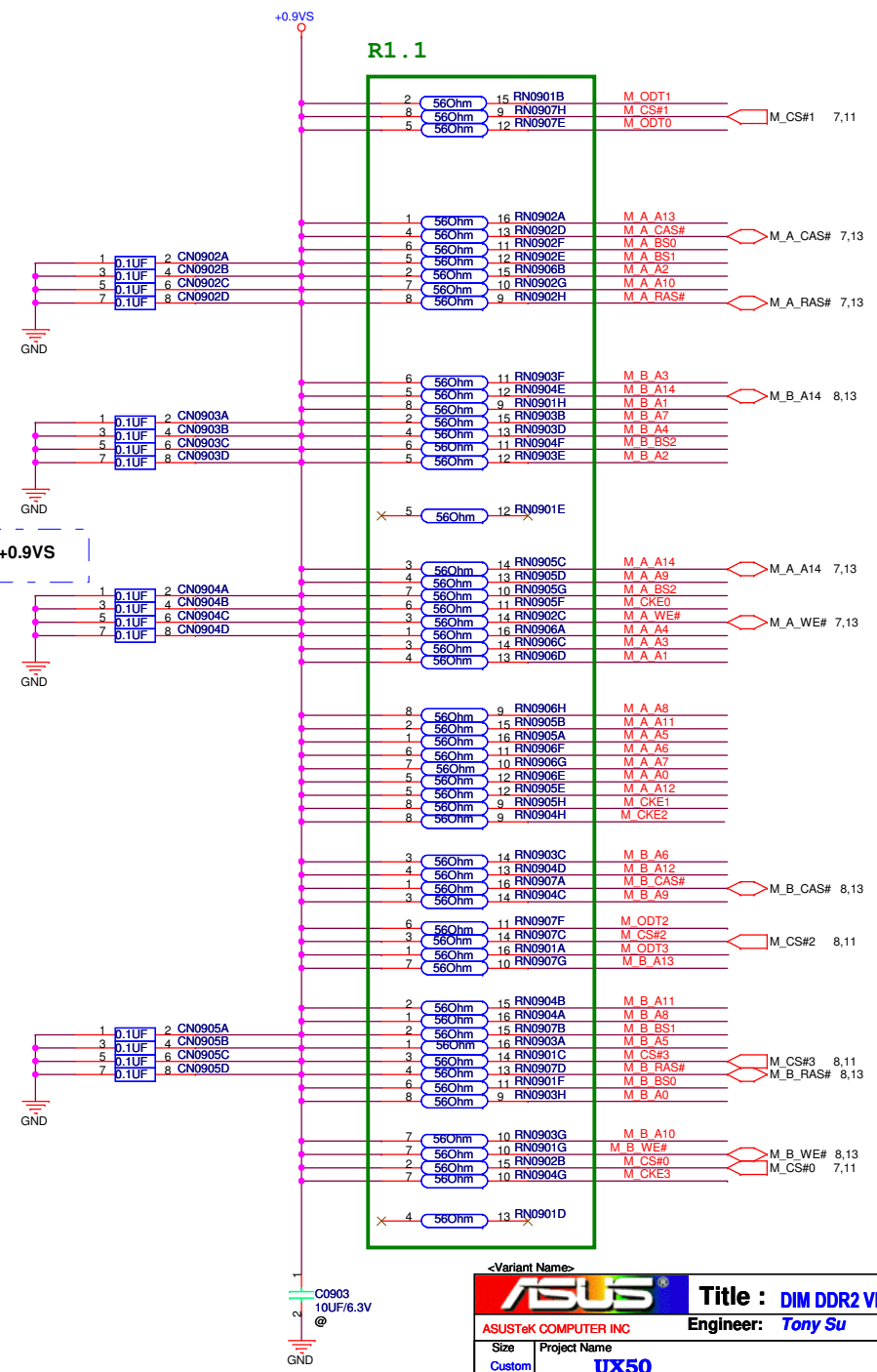


<Variant Name>

ASUS		Titles-DIMM CHANNEL B	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size Custom	Project Name UX50	Rev 1.0a	
Date: Tuesday, March 31, 2009	Sheet	8	of 97

- M_A_A[0..13] 7,13
- M_A_BS[0..2] 7,13
- M_B_A[0..13] 8,13
- M_B_BS[0..2] 8,13
- M_CKE[0..3] 7,8,11
- M_ODT[0..3] 7,8,11

Layout note: Place array cap close to each pullup resistors terminated to +0.9VS

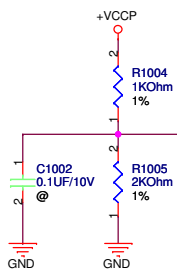
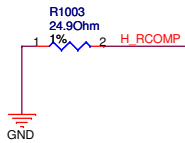
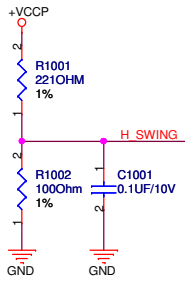


<Variant Name>

ASUS Title : DIM DDR2 VREF

ASUSTeK COMPUTER INC Engineer: Tony Su

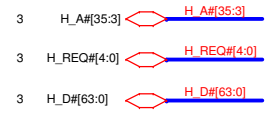
Size	Project Name	Rev
Custom	UX50	1.0a
Date: Tuesday, March 31, 2009	Sheet	9 of 97



U1001A		
H_D#0	J7	H_D#_0
H_D#1	H6	H_D#_1
H_D#2	L11	H_D#_2
H_D#3	J3	H_D#_3
H_D#4	H4	H_D#_4
H_D#5	G3	H_D#_5
H_D#6	K10	H_D#_6
H_D#7	K12	H_D#_7
H_D#8	L1	H_D#_8
H_D#9	M10	H_D#_9
H_D#10	M6	H_D#_10
H_D#11	N11	H_D#_11
H_D#12	L7	H_D#_12
H_D#13	K6	H_D#_13
H_D#14	M4	H_D#_14
H_D#15	K4	H_D#_15
H_D#16	P4	H_D#_16
H_D#17	W9	H_D#_17
H_D#18	V6	H_D#_18
H_D#19	V2	H_D#_19
H_D#20	P10	H_D#_20
H_D#21	W7	H_D#_21
H_D#22	N9	H_D#_22
H_D#23	P4	H_D#_23
H_D#24	U9	H_D#_24
H_D#25	V4	H_D#_25
H_D#26	U1	H_D#_26
H_D#27	W3	H_D#_27
H_D#28	V10	H_D#_28
H_D#29	U7	H_D#_29
H_D#30	W11	H_D#_30
H_D#31	U11	H_D#_31
H_D#32	AC11	H_D#_32
H_D#33	AC9	H_D#_33
H_D#34	Y4	H_D#_34
H_D#35	Y10	H_D#_35
H_D#36	AB6	H_D#_36
H_D#37	AB9	H_D#_37
H_D#38	AE10	H_D#_38
H_D#39	AA1	H_D#_39
H_D#40	AC3	H_D#_40
H_D#41	AC7	H_D#_41
H_D#42	AD12	H_D#_42
H_D#43	AB4	H_D#_43
H_D#44	Y6	H_D#_44
H_D#45	AD10	H_D#_45
H_D#46	AA11	H_D#_46
H_D#47	AB2	H_D#_47
H_D#48	AD4	H_D#_48
H_D#49	AE7	H_D#_49
H_D#50	AD2	H_D#_50
H_D#51	AE3	H_D#_51
H_D#52	AG9	H_D#_52
H_D#53	AG7	H_D#_53
H_D#54	AE11	H_D#_54
H_D#55	AK6	H_D#_55
H_D#56	AF6	H_D#_56
H_D#57	AJ9	H_D#_57
H_D#58	AH6	H_D#_58
H_D#59	AE12	H_D#_59
H_D#60	AH4	H_D#_60
H_D#61	AJ7	H_D#_61
H_D#62	AE9	H_D#_62
H_D#63	AE9	H_D#_63
H_SWING	B6	H_SWING
H_RCOMP	D4	H_RCOMP
H_CPURST#	J11	H_CPURST#
H_CPUSLP#	G9	H_CPUSLP#
H_VREF	L17	H_AVREF
	K18	H_DVREF
		897805

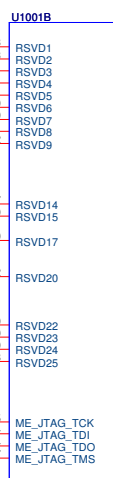
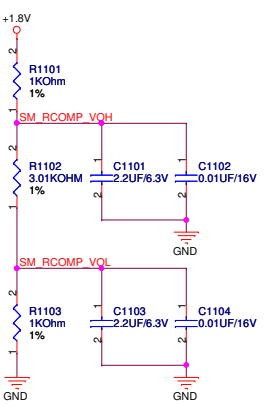
HOST

H_A#_3	L15	H_A#3
H_A#_4	B14	H_A#4
H_A#_5	C15	H_A#5
H_A#_6	D12	H_A#6
H_A#_7	F14	H_A#7
H_A#_8	G17	H_A#8
H_A#_9	B12	H_A#9
H_A#_10	J15	H_A#10
H_A#_11	D16	H_A#11
H_A#_12	C17	H_A#12
H_A#_13	D14	H_A#13
H_A#_14	K16	H_A#14
H_A#_15	F16	H_A#15
H_A#_16	B16	H_A#16
H_A#_17	C21	H_A#17
H_A#_18	D18	H_A#18
H_A#_19	J19	H_A#19
H_A#_20	B21	H_A#20
H_A#_21	D22	H_A#21
H_A#_22	G19	H_A#22
H_A#_23	J17	H_A#23
H_A#_24	L21	H_A#24
H_A#_25	L19	H_A#25
H_A#_26	C21	H_A#26
H_A#_27	D20	H_A#27
H_A#_28	K22	H_A#28
H_A#_29	F18	H_A#29
H_A#_30	K20	H_A#30
H_A#_31	F20	H_A#31
H_A#_32	F22	H_A#32
H_A#_33	B20	H_A#33
H_A#_34	A19	H_A#34
H_A#_35	A19	H_A#35
H_ADS#	F10	H_ADS# 3
H_ADSTB#_0	A15	H_ADSTB#0 3
H_ADSTB#_1	C19	H_ADSTB#1 3
H_BNR#	G9	H_BNR# 3
H_BPRI#	B8	H_BPRI# 3
H_BREQ#	E5	H_BREQ# 3
H_DEFER#	D6	H_DEFER# 3
H_DBSY#	AH10	H_DBSY# 3
HPLL_CLK	AH11	HPLL_CLK# 29
HPLL_CLK#	G11	HPLL_CLK# 29
H_DPWR#	H2	H_DPWR# 3
H_DRDY#	C7	H_DRDY# 3
H_HIT#	F8	H_HIT# 3
H_HITM#	A11	H_HITM# 3
H_LOCK#	D8	H_LOCK# 3
H_TRDY#	D8	H_TRDY# 3
H_DIN#_0	L9	H_DIN#0 3
H_DIN#_1	N7	H_DIN#1 3
H_DIN#_2	AA7	H_DIN#2 3
H_DIN#_3	AG3	H_DIN#3 3
H_DSTBN#_0	K2	H_DSTBN#0 3
H_DSTBN#_1	AA3	H_DSTBN#1 3
H_DSTBN#_2	AF4	H_DSTBN#2 3
H_DSTBN#_3	AF4	H_DSTBN#3 3
H_DSTBP#_0	L3	H_DSTBP#0 3
H_DSTBP#_1	M2	H_DSTBP#1 3
H_DSTBP#_2	Y2	H_DSTBP#2 3
H_DSTBP#_3	AF2	H_DSTBP#3 3
H_REQ#_0	J13	H_REQ#0
H_REQ#_1	L13	H_REQ#1
H_REQ#_2	C13	H_REQ#2
H_REQ#_3	G13	H_REQ#3
H_REQ#_4	G15	H_REQ#4
H_RS#_0	F4	H_RS#0 3
H_RS#_1	F2	H_RS#1 3
H_RS#_2	G7	H_RS#2 3

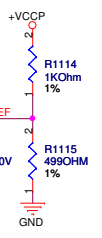
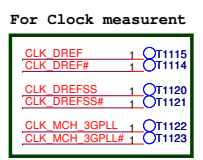
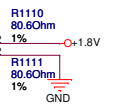
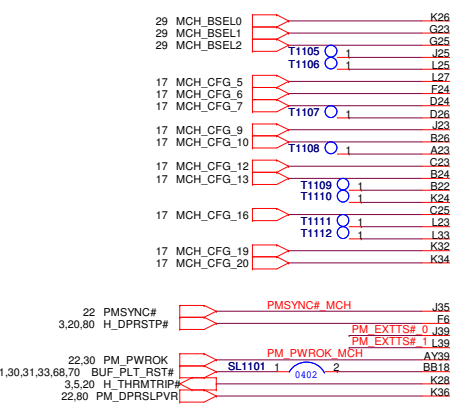
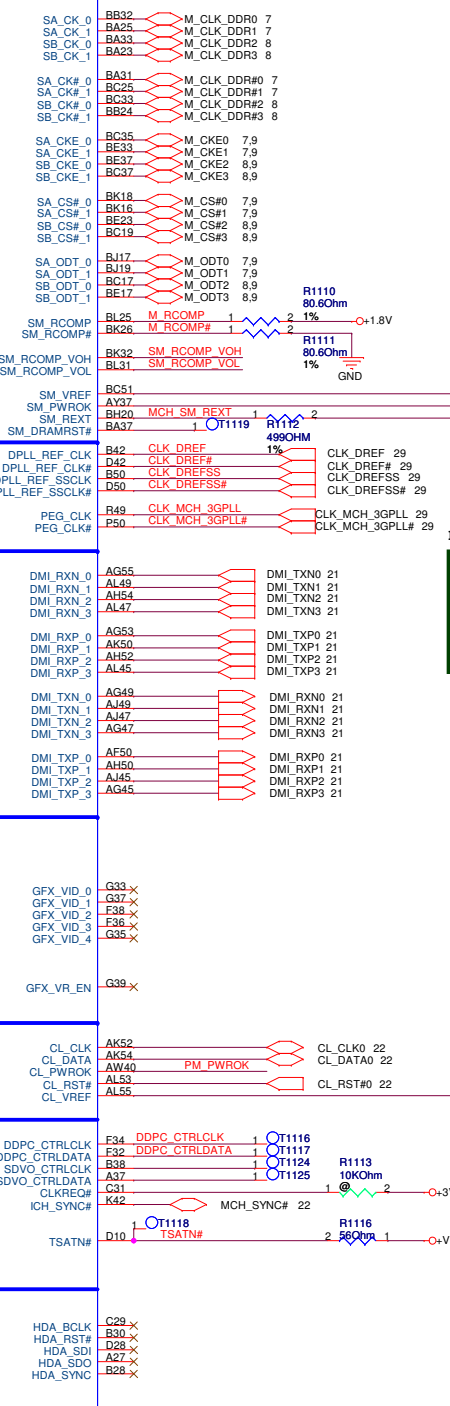


<Variant Name>

ASUS		Title :NB GS45 HOST	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size	Project Name	Rev	
Custom	UX50	1.0a	
Date: Tuesday, March 31, 2009	Sheet	10	of 97



RSVD
DDR CLK/ CONTROL/COMPENSATION
CLK
DMI
CFM
GRAPHICS VID
ME
ON
MISC
HDA



DG, Checklist: 500ohm
CRB: 511ohm

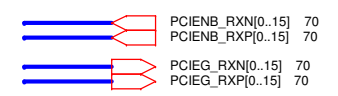
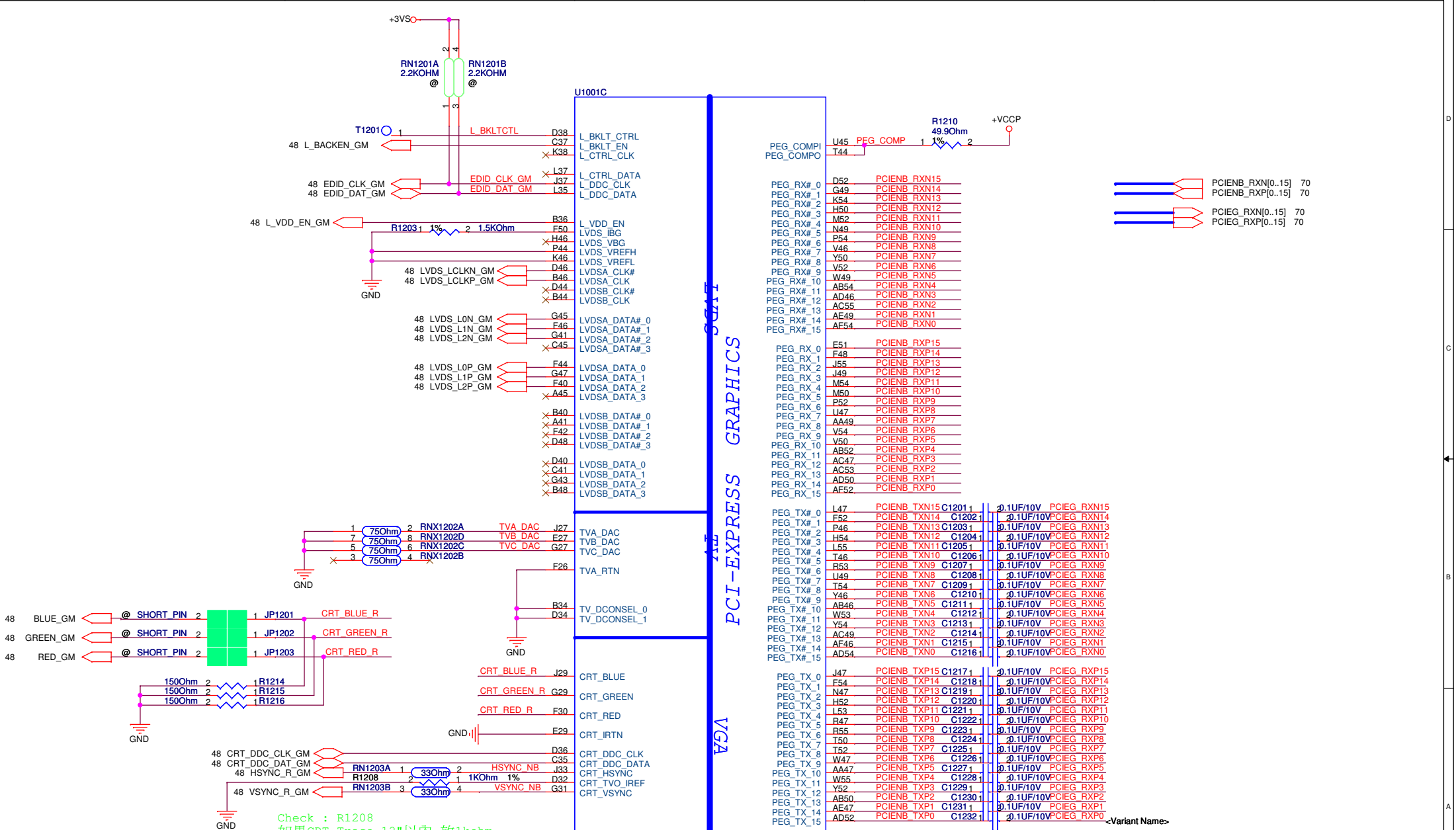
<Variant Name>

ASUS Title :NB GS45 DMI

ASUSTek COMPUTER INC Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 11 of 97



Check : R1208
 如果CRT Trace 12"以内,放1kohm
 如果CRT Trace 12~15.3",放976ohm

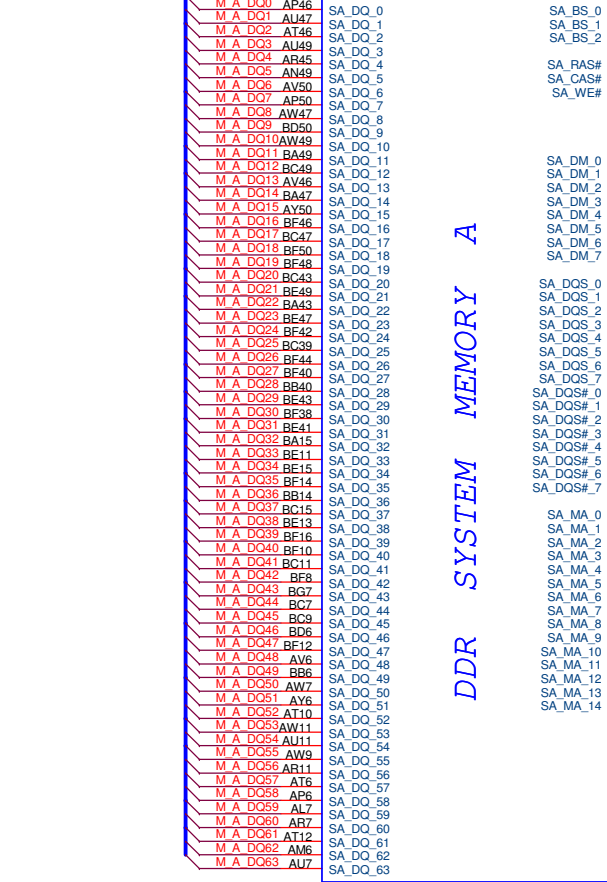
ASUS Title : NB GS45 DISPLAY

ASUSTeK COMPUTER INC Engineer: Tony Su

Size	Project Name	Rev
B	UX50	1.0a

Date: Friday, April 03, 2009 Sheet 12 of 97

7 M_A_DQ[0:63]

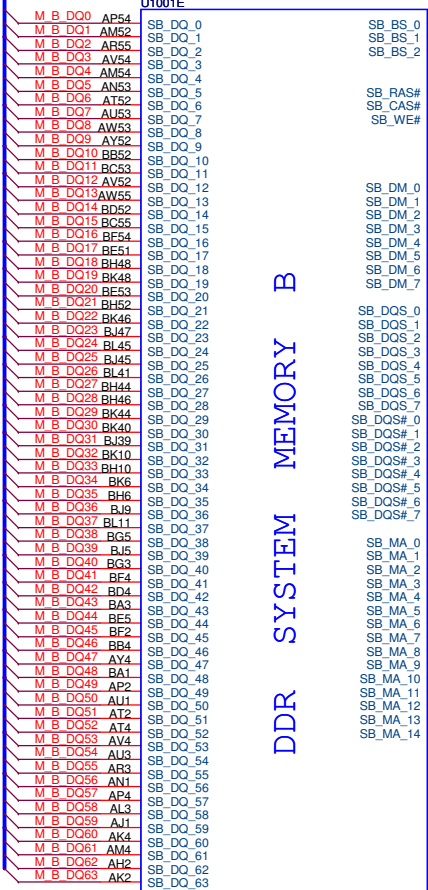


U1001D

DDR SYSTEM MEMORY A

897605

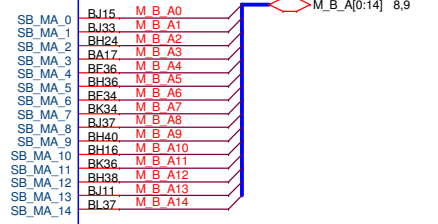
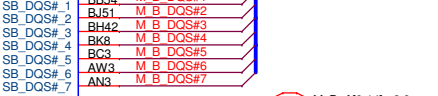
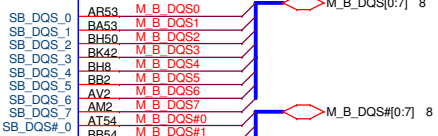
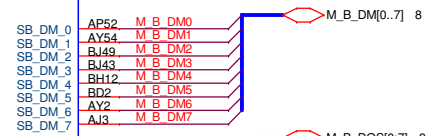
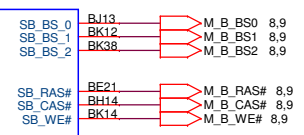
8 M_B_DQ[0:63]



U1001E

DDR SYSTEM MEMORY B

897605



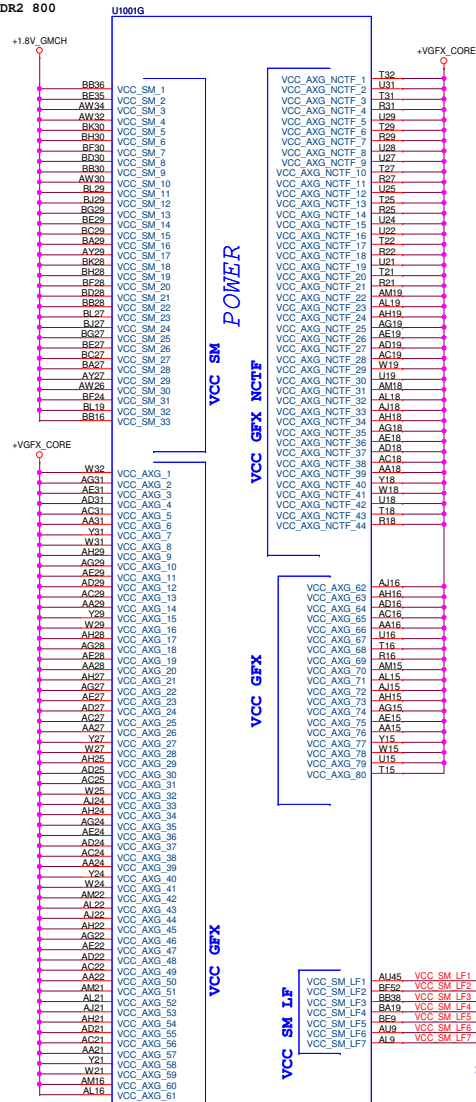
<Variant Name>



ASUSTeK COMPUTER INC Engineer: Tony Su

Size	Project Name	Rev
Custom	UX50	1.0a
Date: Tuesday, March 31, 2009	Sheet	13 of 97

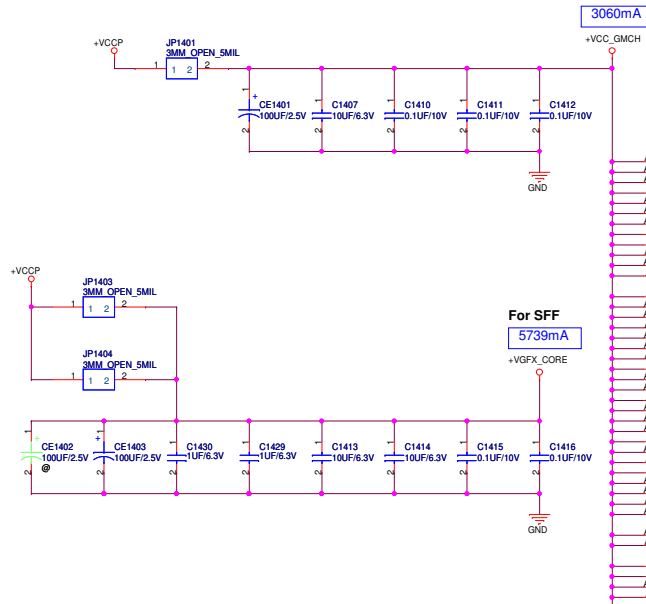
2.6A for DDR2 667
3A for DDR2 800



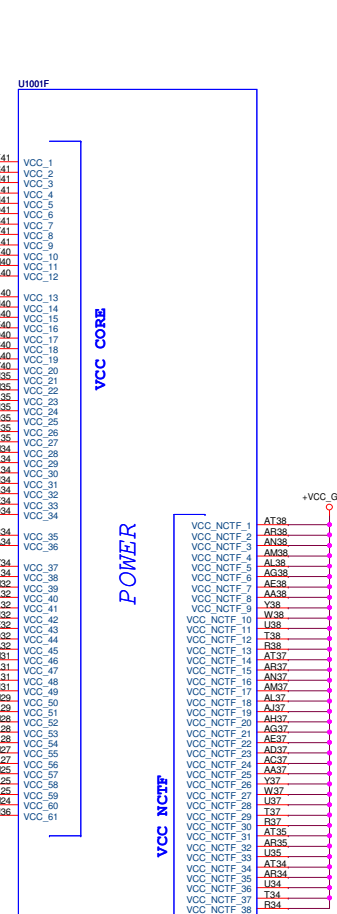
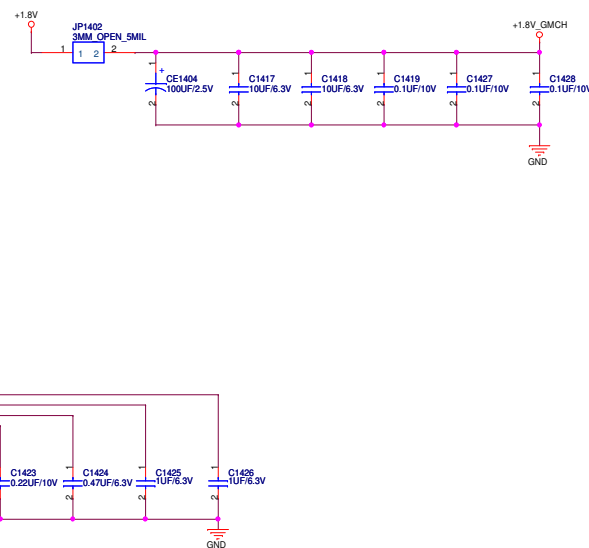
T1401 1 VCC_AXG_SENSE AG13 VCC_AXG_SENSE
T1402 1 VSS_AXG_SENSE AE13 VSS_AXG_SENSE

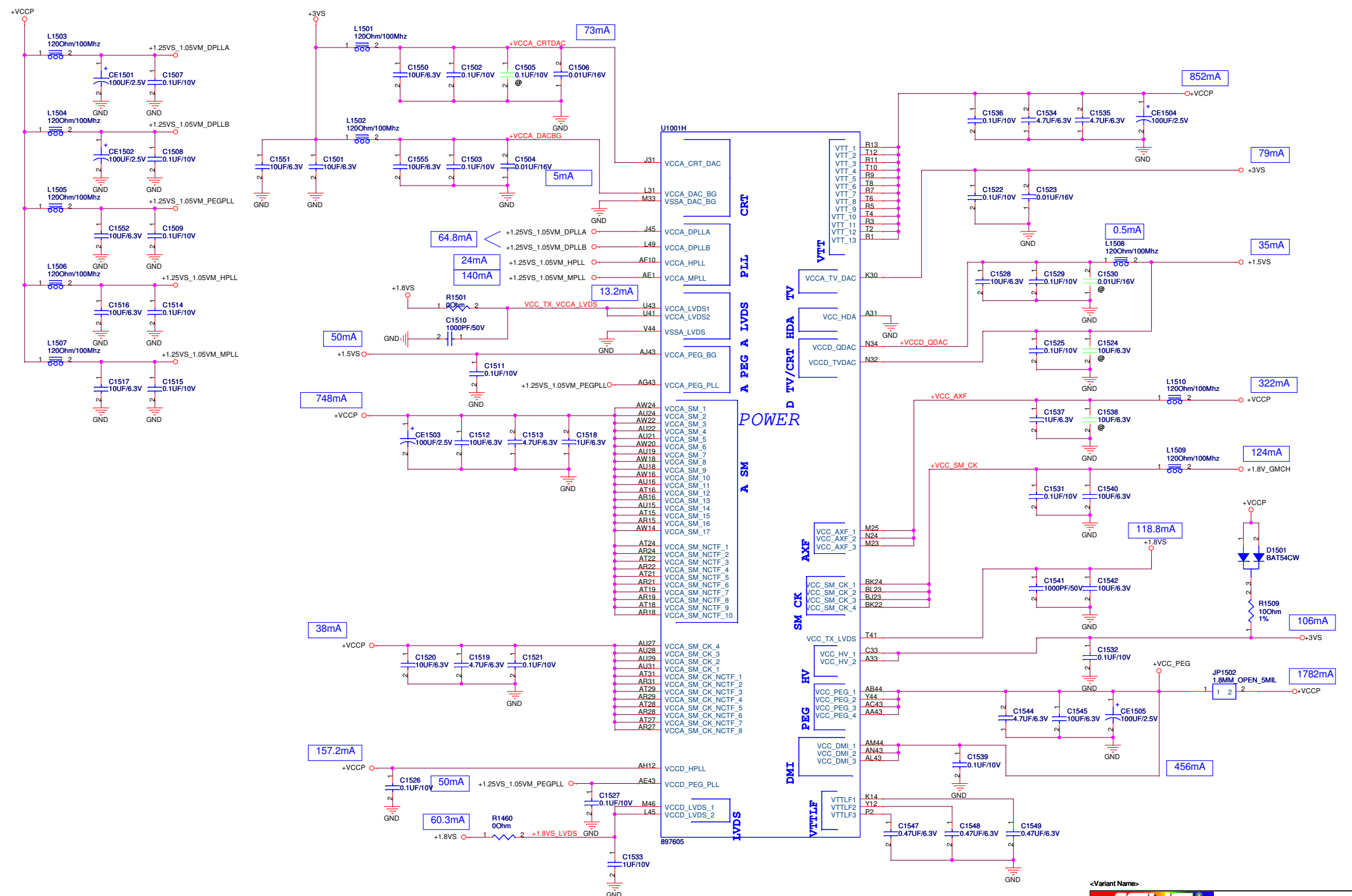
Route VCC_AXG_SENSE and VSS_AXG_SENSE differentially.

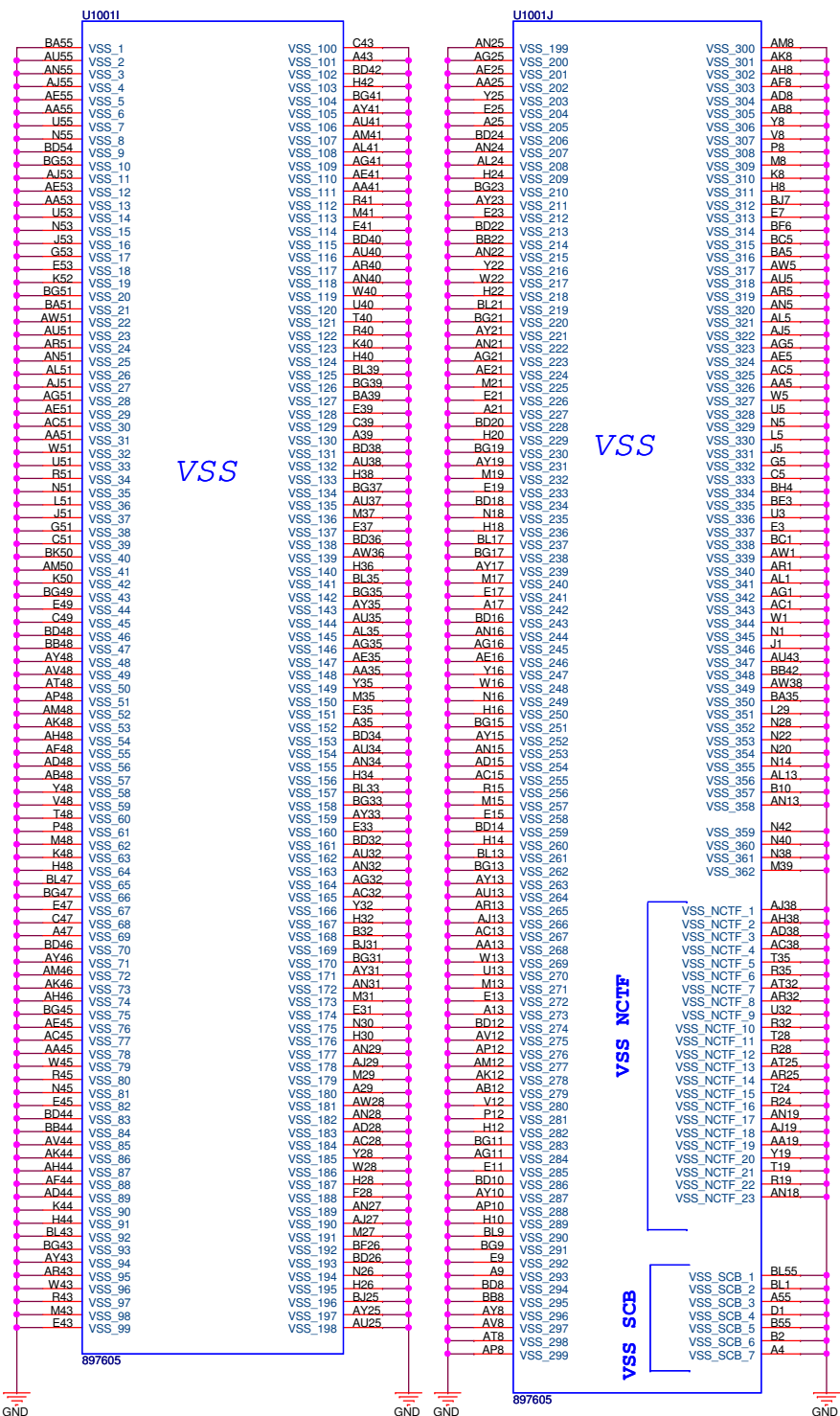
897605



2.6A for DDR2 667
3A for DDR2 800

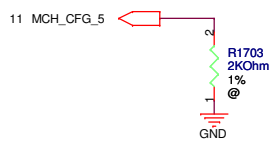




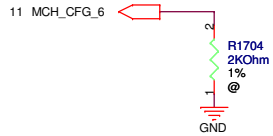


<Variant Name>

ASUS		Title :NB GS45 GND	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size Custom	Project Name UX50	Rev 1.0a	
Date: Tuesday, March 31, 2009	Sheet	16	of 97



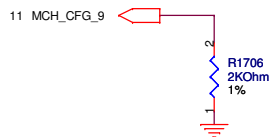
CFG5 : DMI STRAP
H = DMI X 4 (Default)
L = DMI X 2



CFG6 : ITPM Host Interface
(Relate to SPL_MOSI)
H = ITPM Disable (Default)
L = ITPM enable(Can disable by SW)



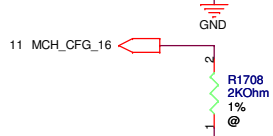
CFG7 : Intel ME Crypto Strap
H = With confidentiality (Default)
L = Without confidentiality



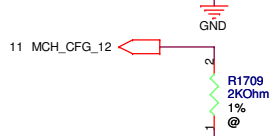
CFG9 : PCIE Graphic Lane Reverse
H = Normal (Default)
L = Lanes Reverse



CFG10 : PCIE Loopback
H = Disable (Default)
L = Enable



CFG16 : FSB Dynamic ODT
H =Enable (Default)
L = Disable

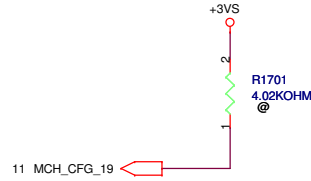


CFG12 : ALL-Z Mode
H =Disable (Default)
L = Enable

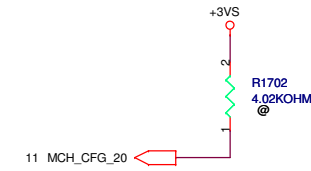


CFG13 : XOR Mode
H = Disable (Default)
L = Enable

CFG [13:12] : XOR/ALL-Z
 00 = Reserved
 01= XOR Mode Enabled
 10= All-Z Mode Enabled
11= Normal Operation (Default)



CFG19 : DMI Lane Reversal
H =DMI Lane Reversal
L = Normal (Default)



CFG20 : SDVO/PCIE CONCURRENT MODE
L = Only Digital display port or PCIE is Operational (Default)
H = Digital display port and PCIE are operating simultaneously via the PEG port

<Variant Name>

ASUS		Title :NB GS45 STRAPPING	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size	Project Name	Rev	
Custom	UX50	1.0a	
Date: Monday, April 06, 2009	Sheet	17	of 97

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<Variant Name>		
		Title :
<small>ASUSTeK COMPUTER INC</small>		Engineer: <i>Tony Su</i>
<small>Size</small> C	<small>Project Name</small> UX50	<small>Rev</small> 1.0a
<small>Date: Tuesday, March 31, 2009</small>		<small>Sheet 18 of 97</small>

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<Variant Name>



Title :

ASUSTeK COMPUTER INC

Engineer: *Tony Su*

Size	Project Name	Rev
A	UX50	1.0a

Date: Tuesday, March 31, 2009 Sheet 19 of 97

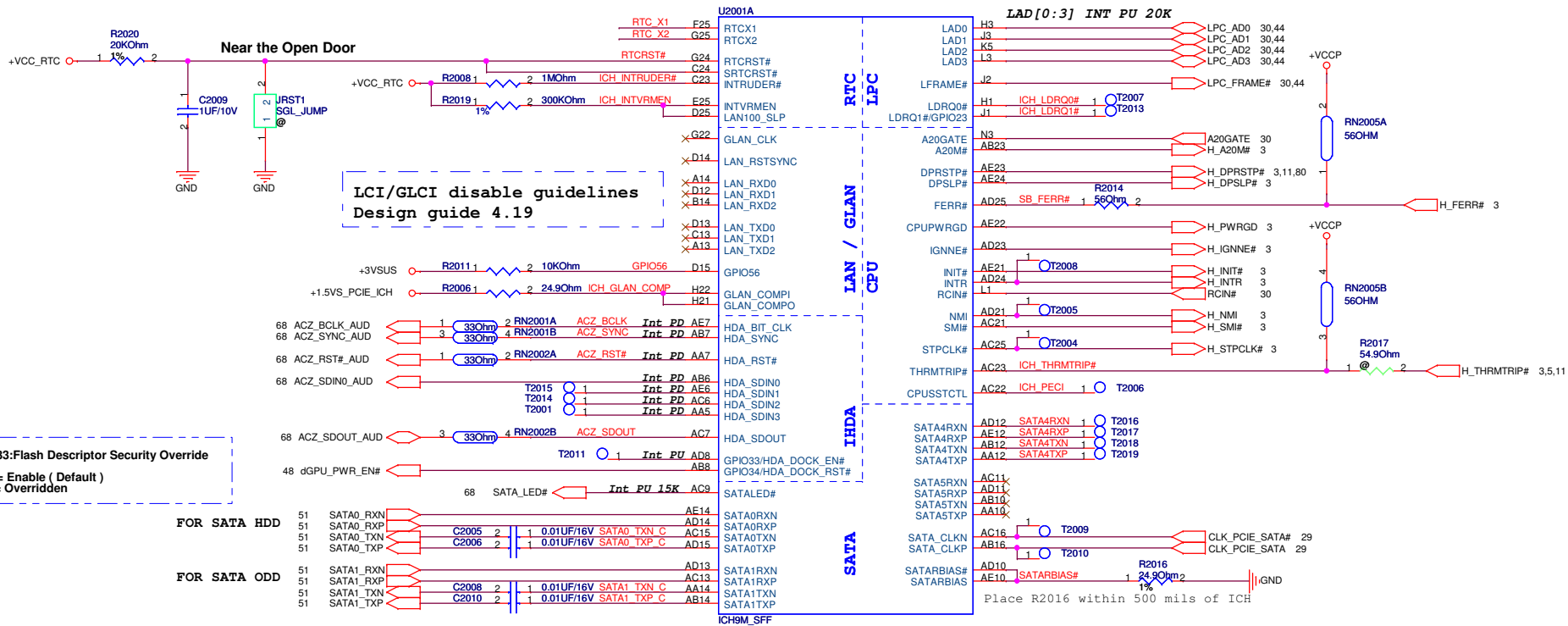
5

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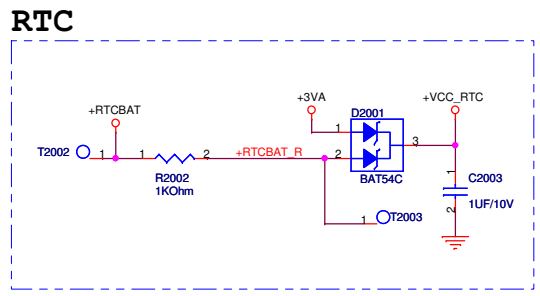
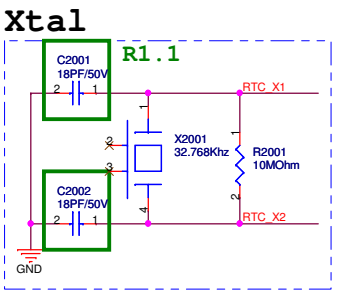
2

1

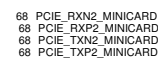
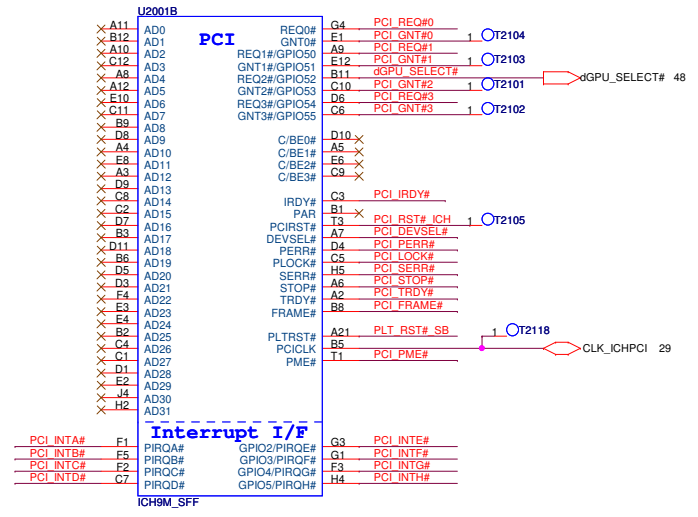


[ICH_TP3, ACZ_SDOUD] : XOR Chain Entrance Strap

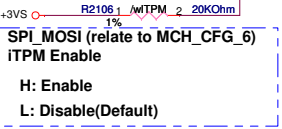
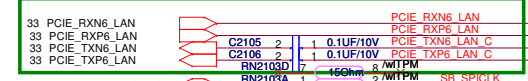
00 = Reserved
01 = Enter XOR Chain
10 = Normal Operation (Default)
11 = Set PCIe Port Config Bit 1



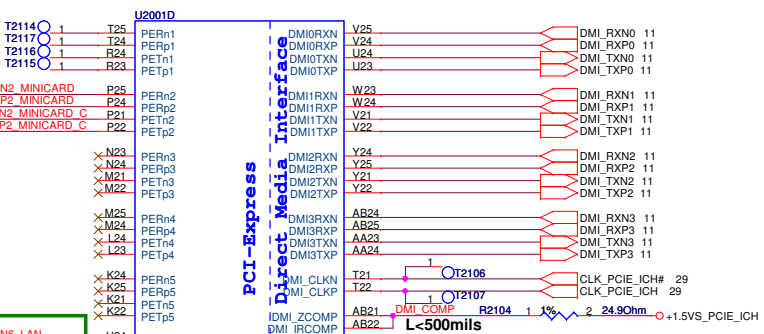
PCIE 1	
PCIE 2	WLAN
PCIE 3	Newcard
PCIE 4	GLAN



R1.1



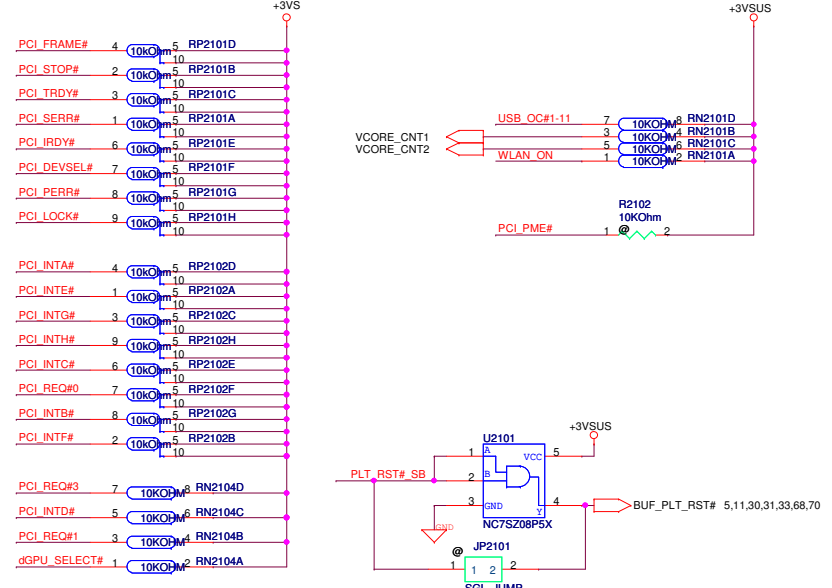
H: Enable
L: Disable(Default)



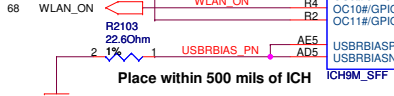
PCI-Express
Differential Mode Interface

USB

USB 0	USB Conn.(M/B)
USB 1	USB Conn.(M/B)
USB 2	Bluetooth
USB 3	
USB 4	CMOS Camera
USB 5	Card Reader
USB 6	WiMax
USB 7	
USB 8	
USB 9	
USB 10	USB Conn.(M/B)
USB 11	



SR Check可否Short過去?



ICH9M BIOS select

	GNT#0	SPICS#1
LPC	11	1
PCI	10	0
SPI	01	0

(default)

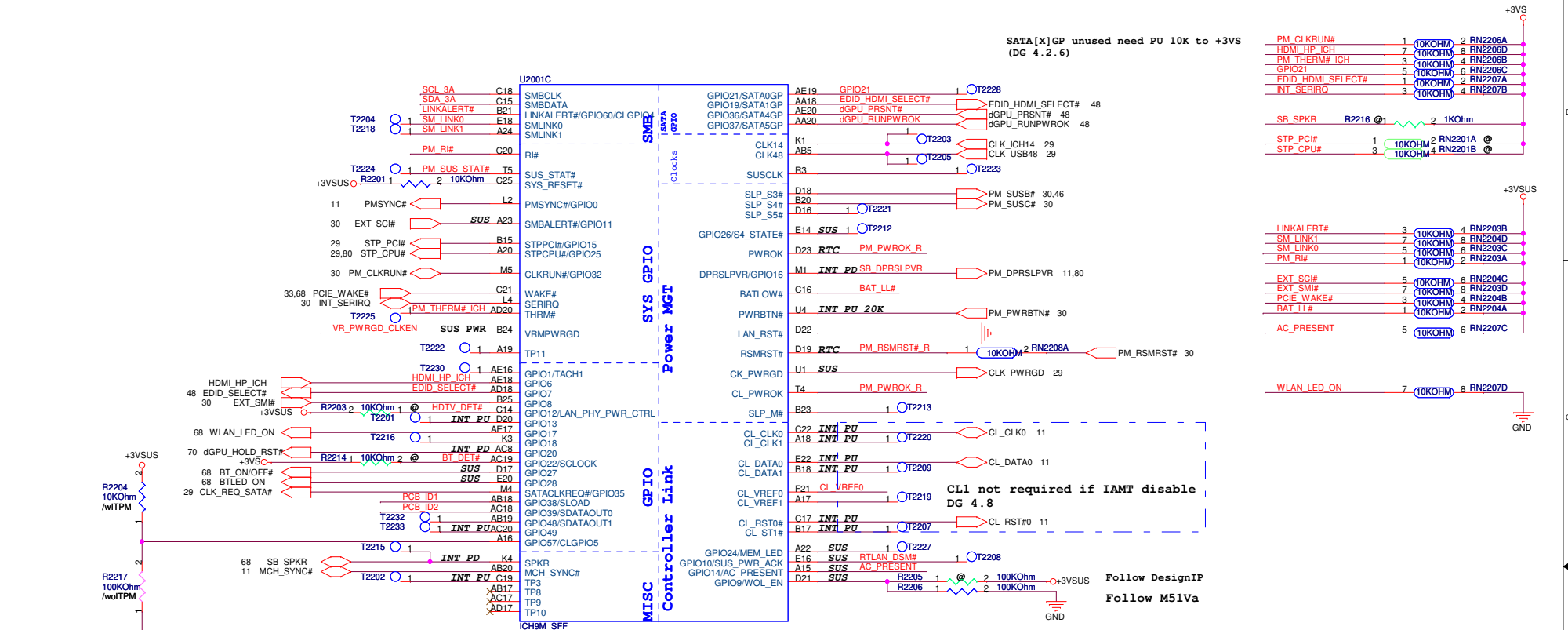
<Variant Name>

Title : SB ICH9M(2)

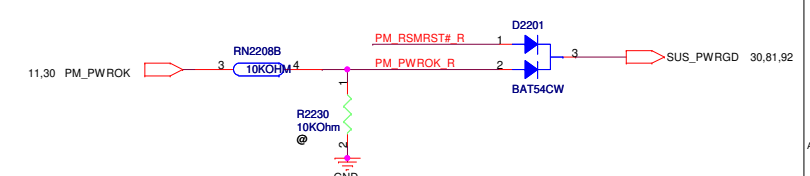
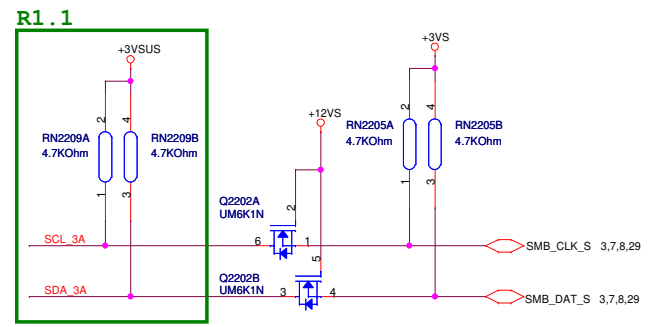
ASUSTek COMPUTER INC Engineer: **Tony Su**

Size Project Name
Custom **UX50**

Date: **Tuesday, March 31, 2009** Sheet 21 of 97



SPKR
No Reboot Strap
Low = Default
High = No Reboot



PCB ID	GPIO38	GPIO39
MBR1.0	0	0
MBR1.1	0	1
MBR2.0	1	0

CL_VREF0 routing rules
Width = 12 mils min
Spacing = 12 mils min
Break-out = 5 mils on 5 mils for 300 mils max

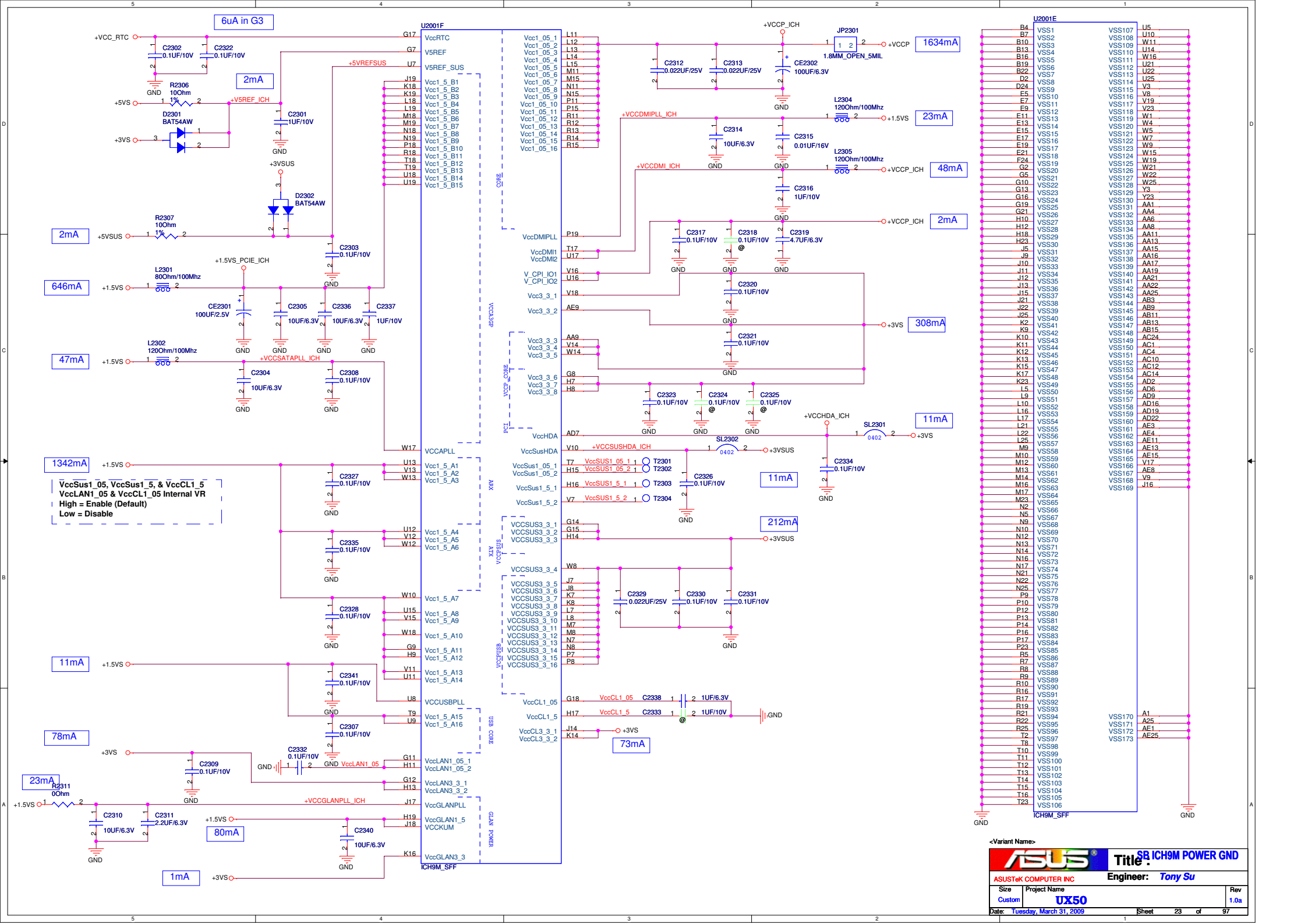
<Variant Name>

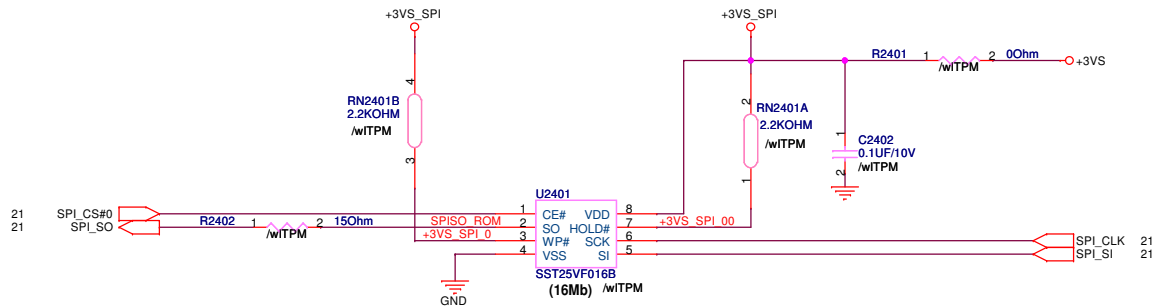
ASUS Title: **SB ICH9M GPIO PMGT**

ASUSTek COMPUTER INC Engineer: **Tony Su**

Size	Project Name	Rev
Custom	UX50	1.0a

Date: Monday, April 06, 2009 Sheet 22 of 97





FOR iTPM

<Variant Name>

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>
Size A	Project Name UX50	Rev 1.0a
Date: Tuesday, March 31, 2009		Sheet 25 of 97

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>
Size A	Project Name UX50	Rev 1.0a
Date: Tuesday, March 31, 2009		Sheet 26 of 97

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>
Size A	Project Name UX50	Rev 1.0a
Date: Tuesday, March 31, 2009		Sheet 27 of 97

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>
Size A	Project Name UX50	Rev 1.0a
Date: Tuesday, March 31, 2009		Sheet 28 of 97

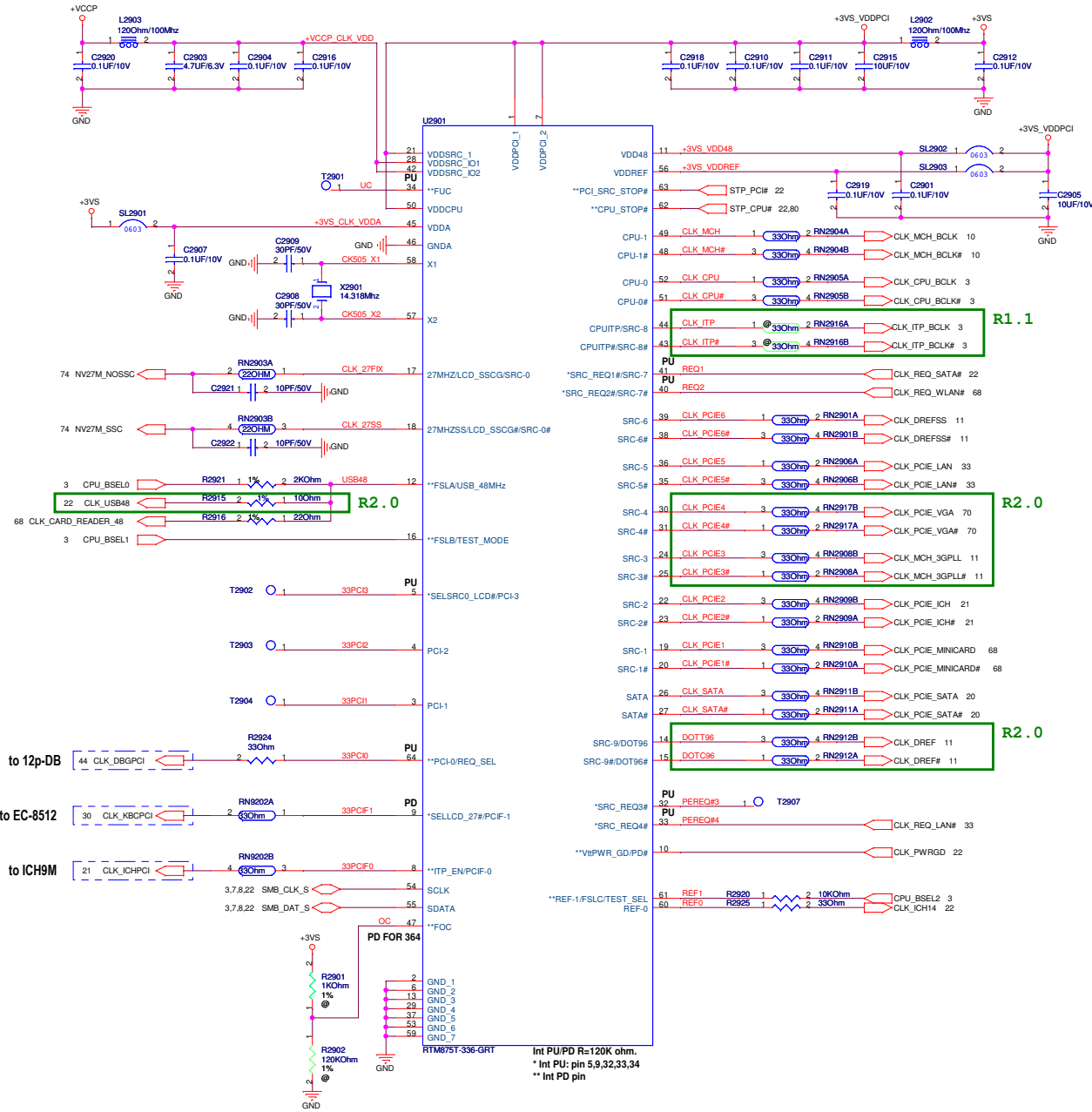
5

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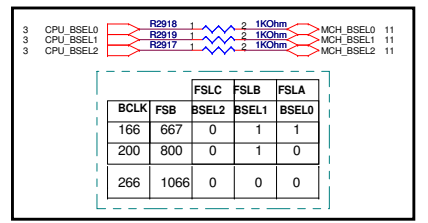
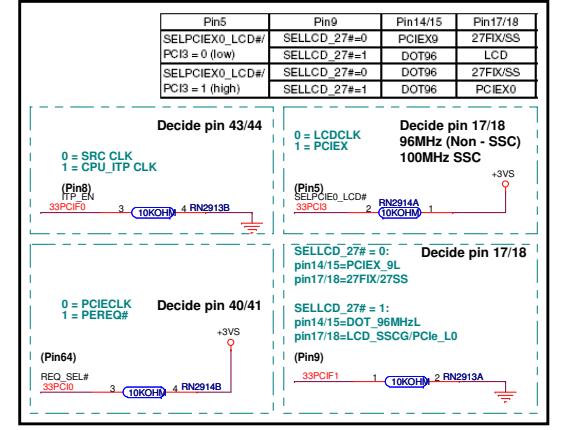
3

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Latched Input Select



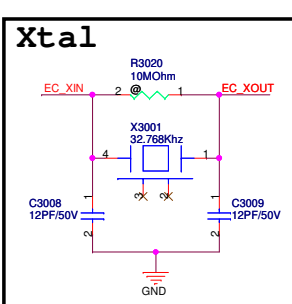
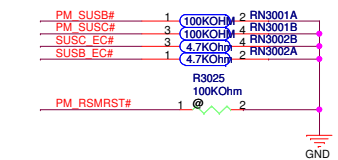
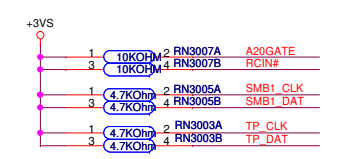
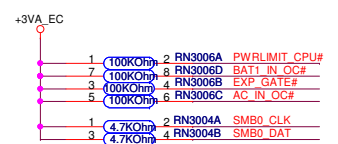
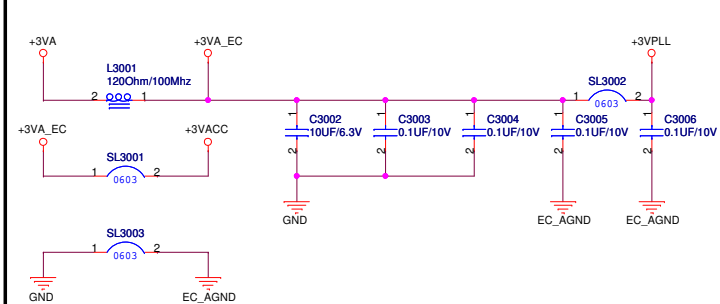
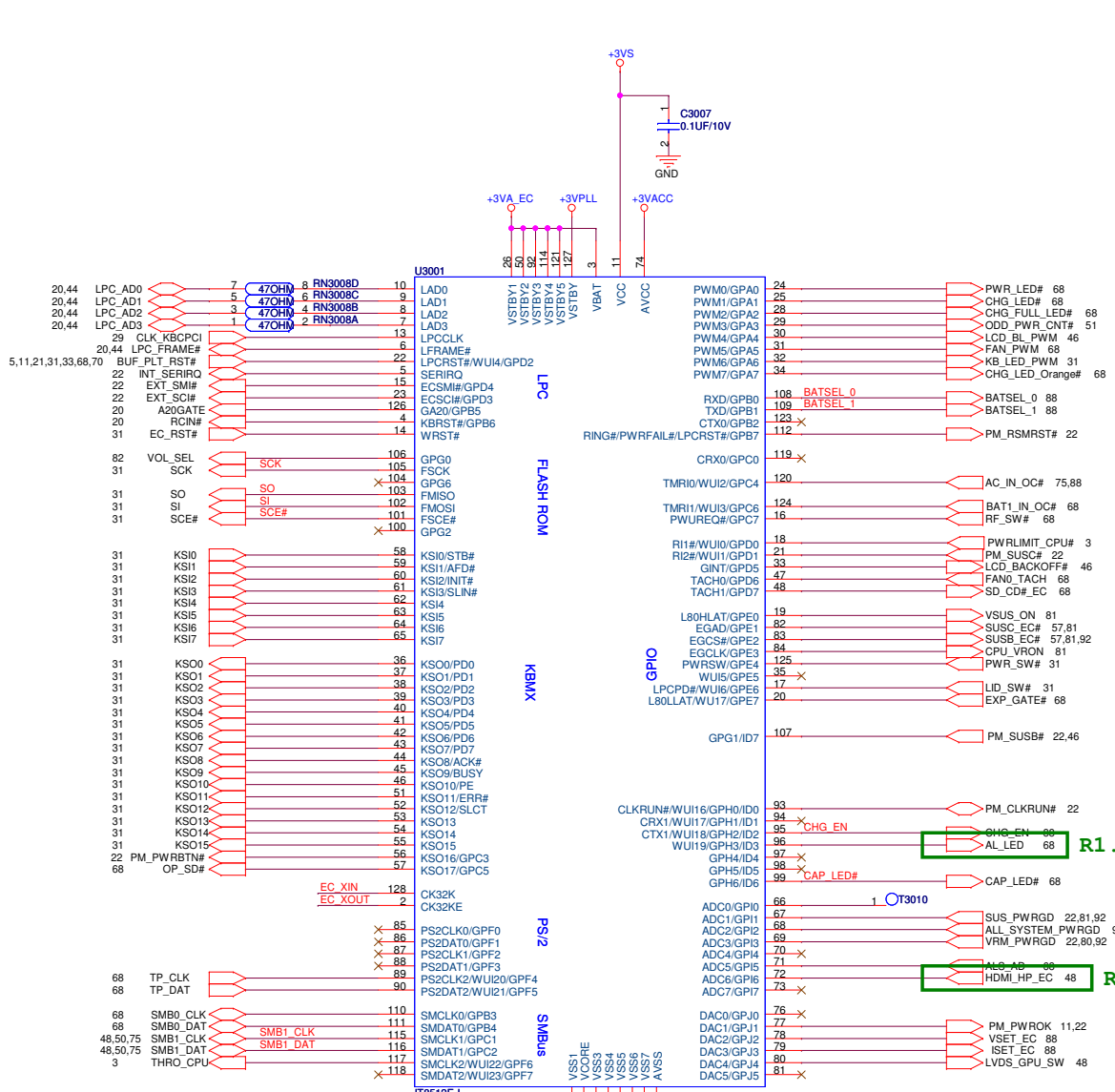
R2.0

R1.1

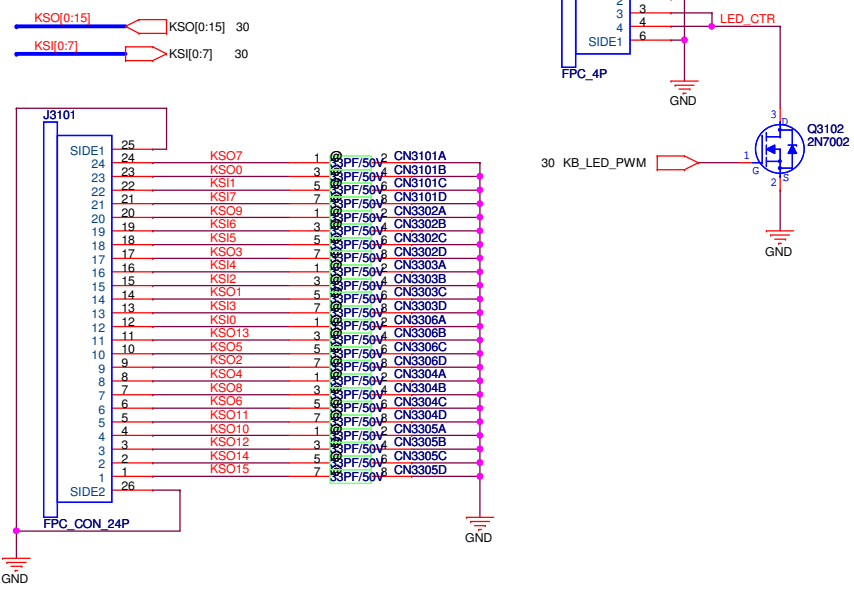
R2.0

R2.0

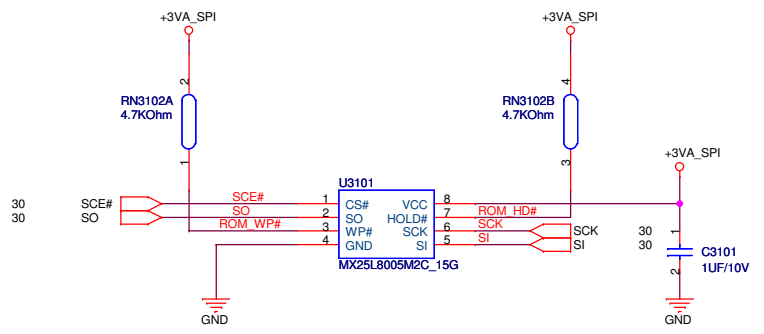
Int PU/PD R=120K ohm.
* Int PU: pin 5,9,32,33,34
** Int PD pin



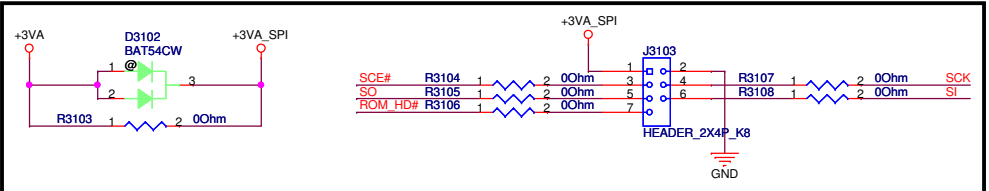
Internal Keyboard



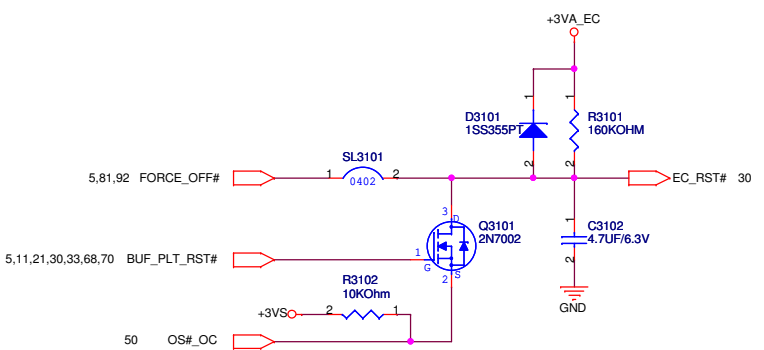
8Mb SPI ROM



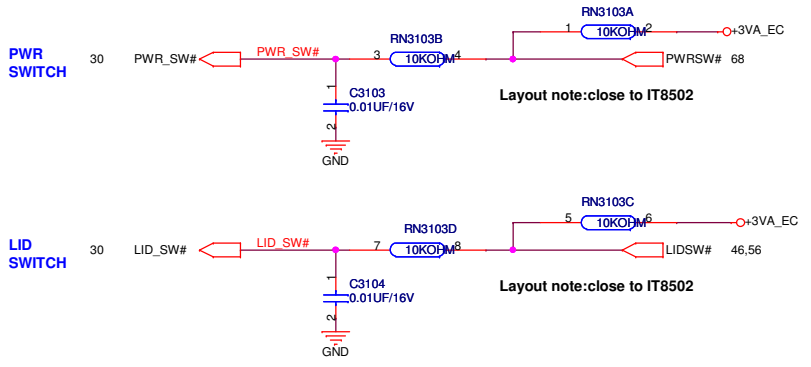
For SPI Flash Debug



EC RST



For Switch



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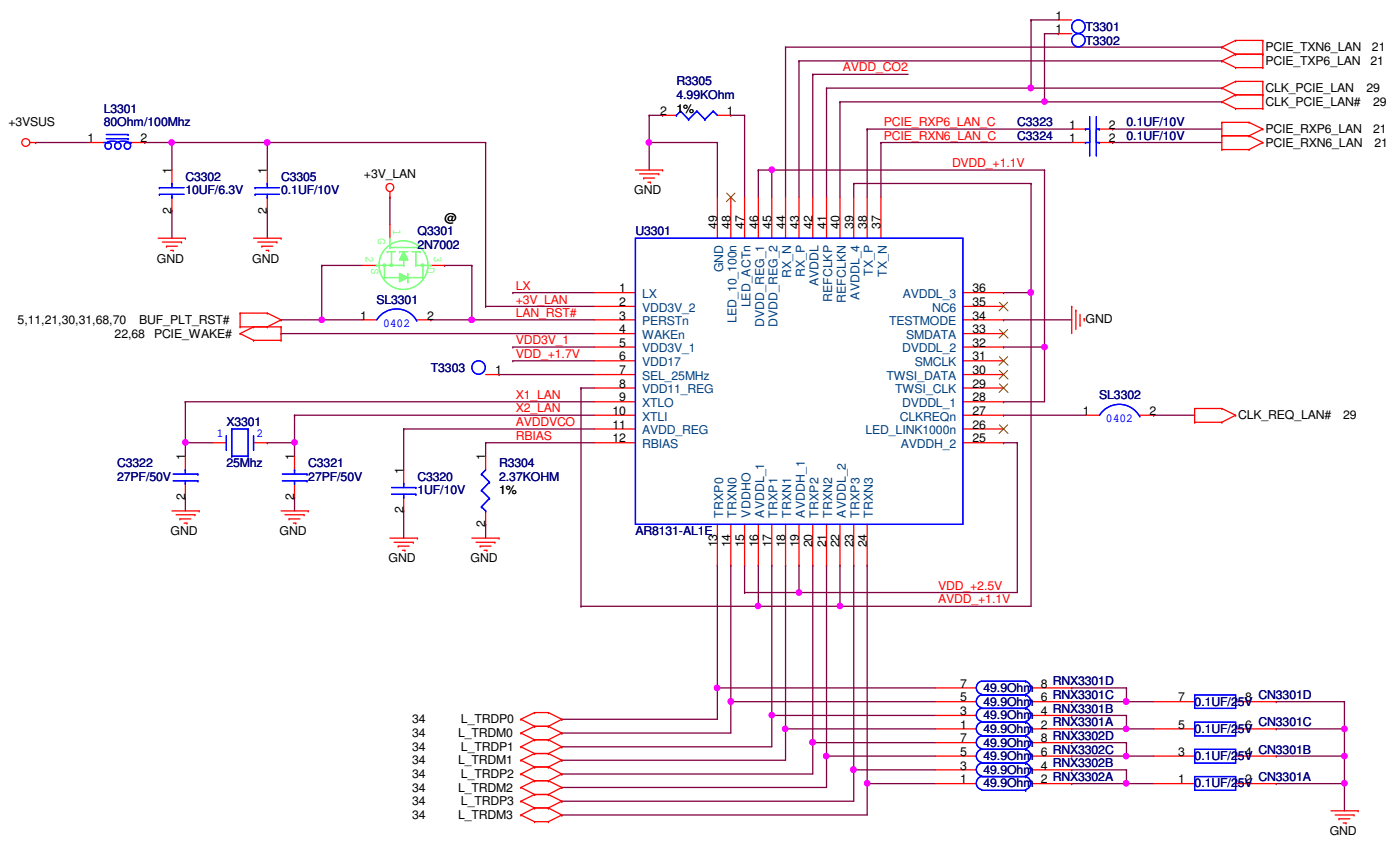
A

A

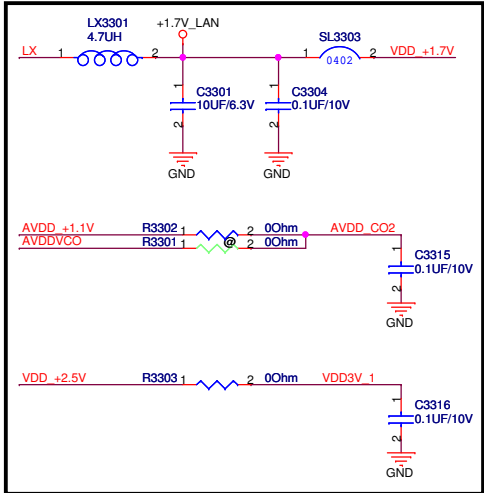
<Variant Name>

		Title: UVA LEVEL SHIFTERS	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	

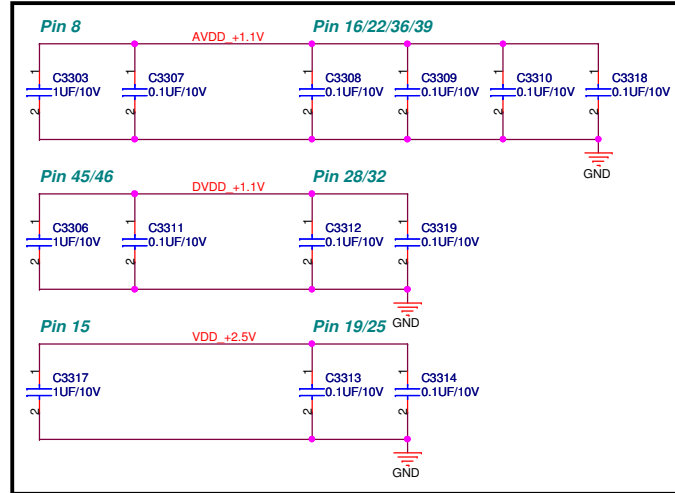
Size	Project Name	Rev
C	UX50	1.0a
Date: <u>Tuesday, March 31, 2009</u>		Sheet 32 of 97

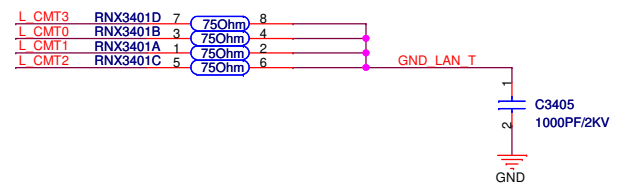
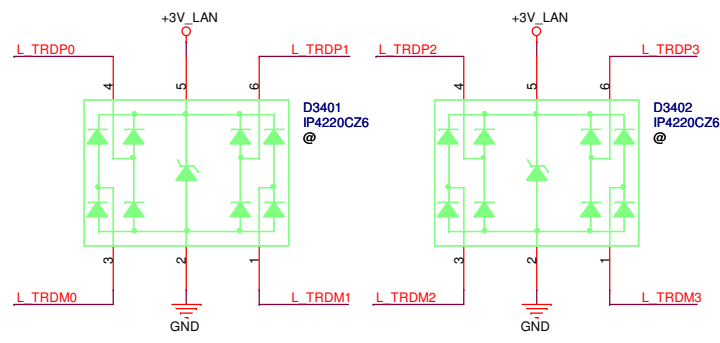


Power

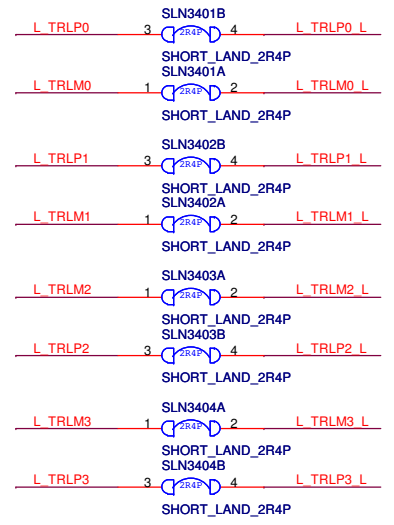
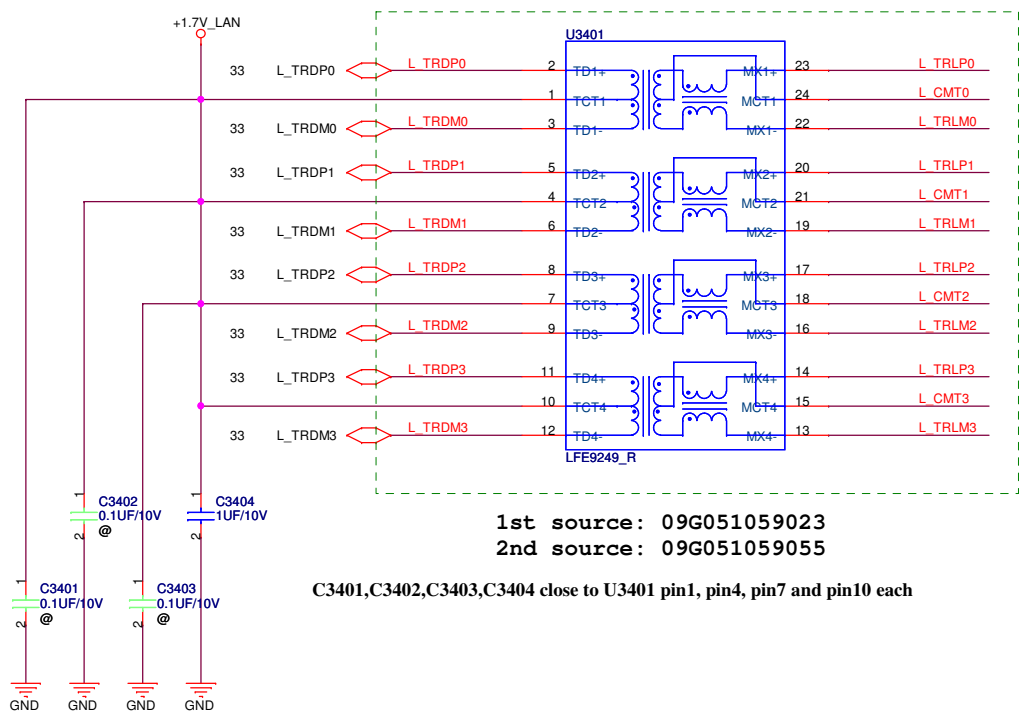
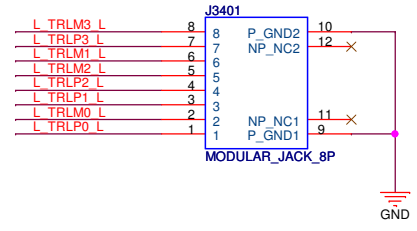


Cap.





For RJ-45



<Variant Name>

ASUS		Title :LAN RJ45 CONN	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name	Rev	
Custom	UX50	1.0	
Date: Tuesday, March 31, 2009		Sheet	34 of 97

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<Variant Name>

		Title : LAN RJ45 CONN
ASUSTeK COMPUTER INC		Engineer: Tony Su
Size A	Project Name UX50	Rev 1.0
Date: Tuesday, March 31, 2009		Sheet 35 of 97

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<Variant Name>

		Title :AUD ALC269	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size	Project Name	Rev	
Custom	UX50	1.0a	
Date: Tuesday, March 31, 2009		Sheet	36 of 97

5

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<Variant Name>



Title :

ASUSTeK COMPUTER INC Engineer: *Tony Su*

Size Custom	Project Name UX50	Rev 1.0a
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<Variant Name>

ASUS **AUD-HP&SPK&MIC&DMI-CONN**
Title :

ASUSTeK COMPUTER INC **Engineer: Tony Su**

Size	Project Name	Rev
Custom	U20A	1.0a

Date: Tuesday, March 31, 2009 Sheet 38 of 97

5

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>
Size	Project Name	Rev
A	UX50	1.0a
Date: Tuesday, March 31, 2009		Sheet 39 of 97

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>
Size A	Project Name UX50	Rev 1.0a
Date: Tuesday, March 31, 2009		Sheet 40 of 97

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<Variant Name>



Title :

ASUSTeK COMPUTER INC

Engineer: *Tony Su*

Size
A

Project Name
UX50

Rev
1.0a

Date: Tuesday, March 31, 2009

Sheet 41 of 97

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<Variant Name>

		Title: CARD READER AU6371	
ASUSTeK COMPUTER INC		Engineer: Tony Su	
Size	Project Name	Rev	
Custom	UX50	1.0a	
Date: Tuesday, March 31, 2009		Sheet	42 of 97

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<Variant Name>



Title : CB EXPRESS CARD CONN

ASUSTeK COMPUTER INC

Engineer: *Tony Su*

Size	Project Name	Rev
A	UX50	1.0a

Date: **Tuesday, March 31, 2009**

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5

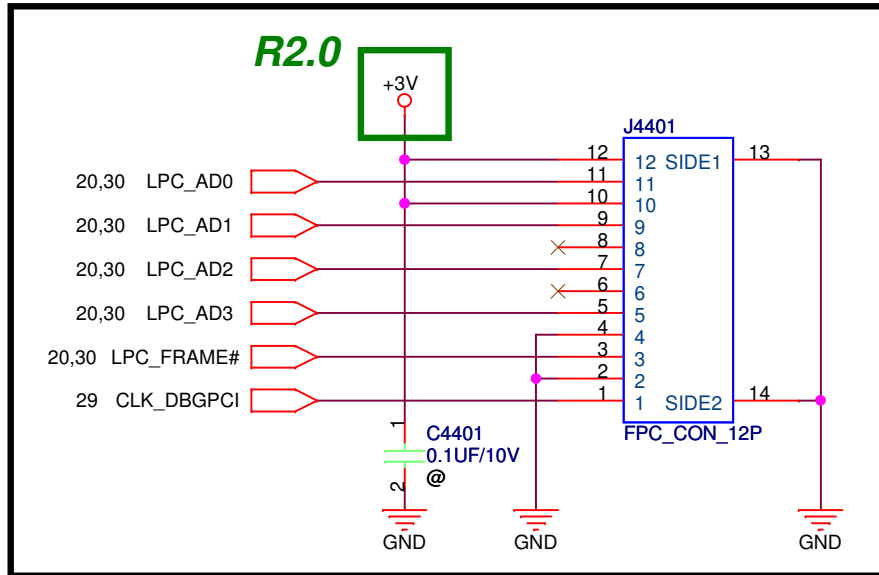
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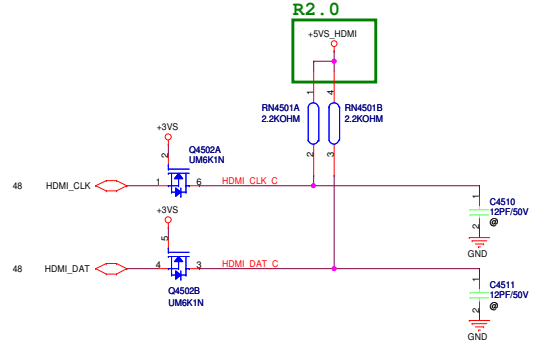
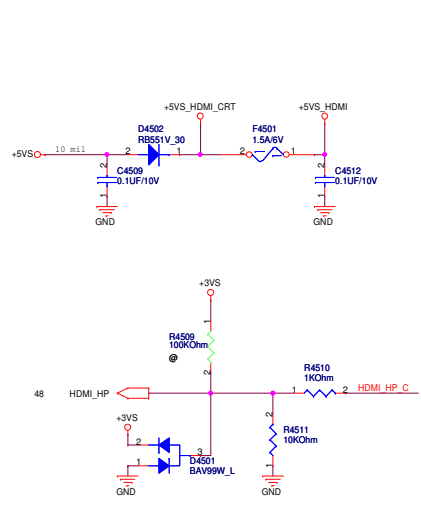
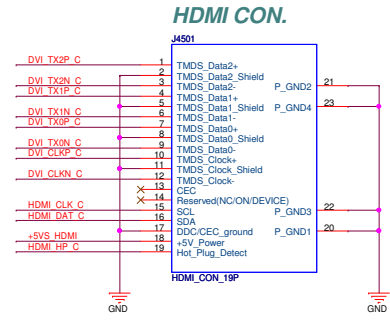
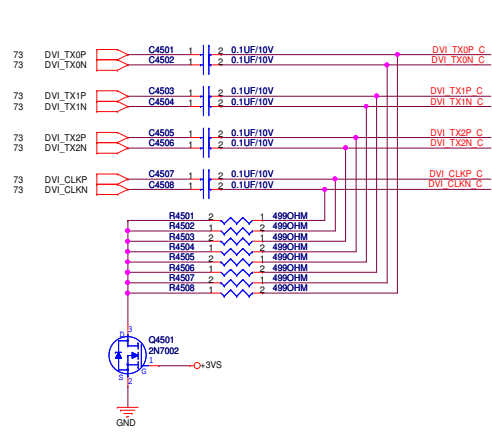
1

LPC DEBUG PORT

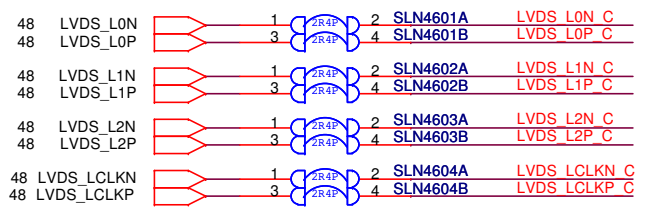
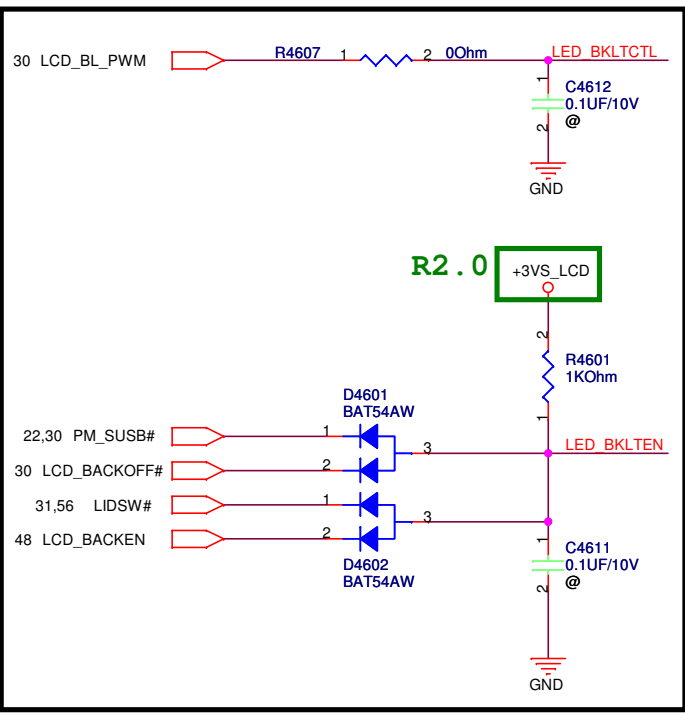
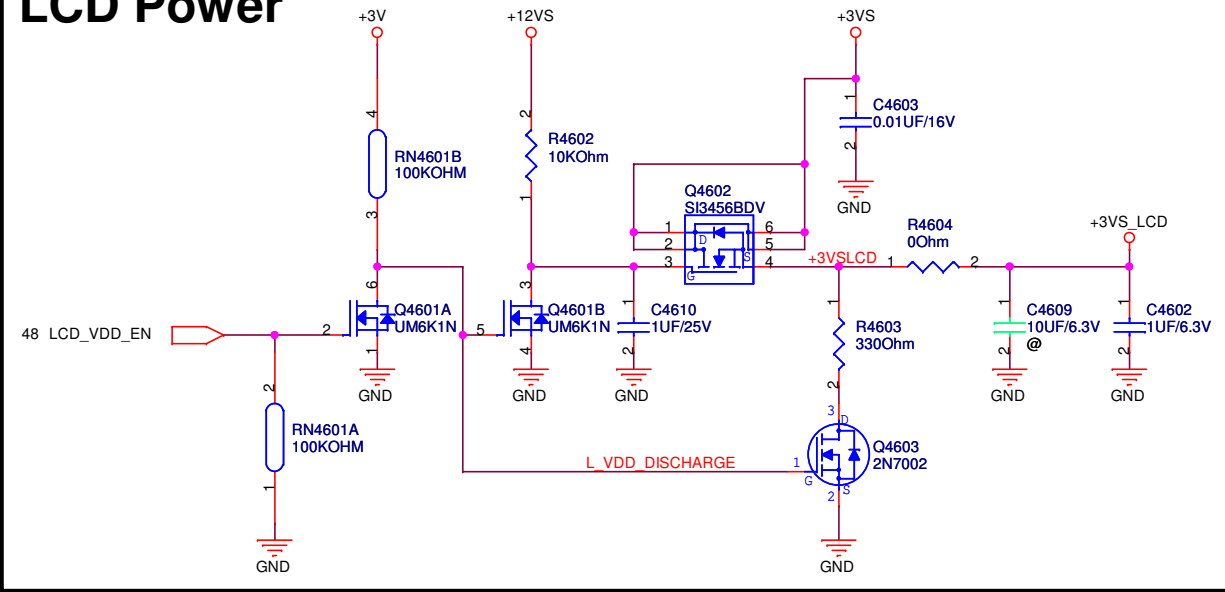


<Variant Name>

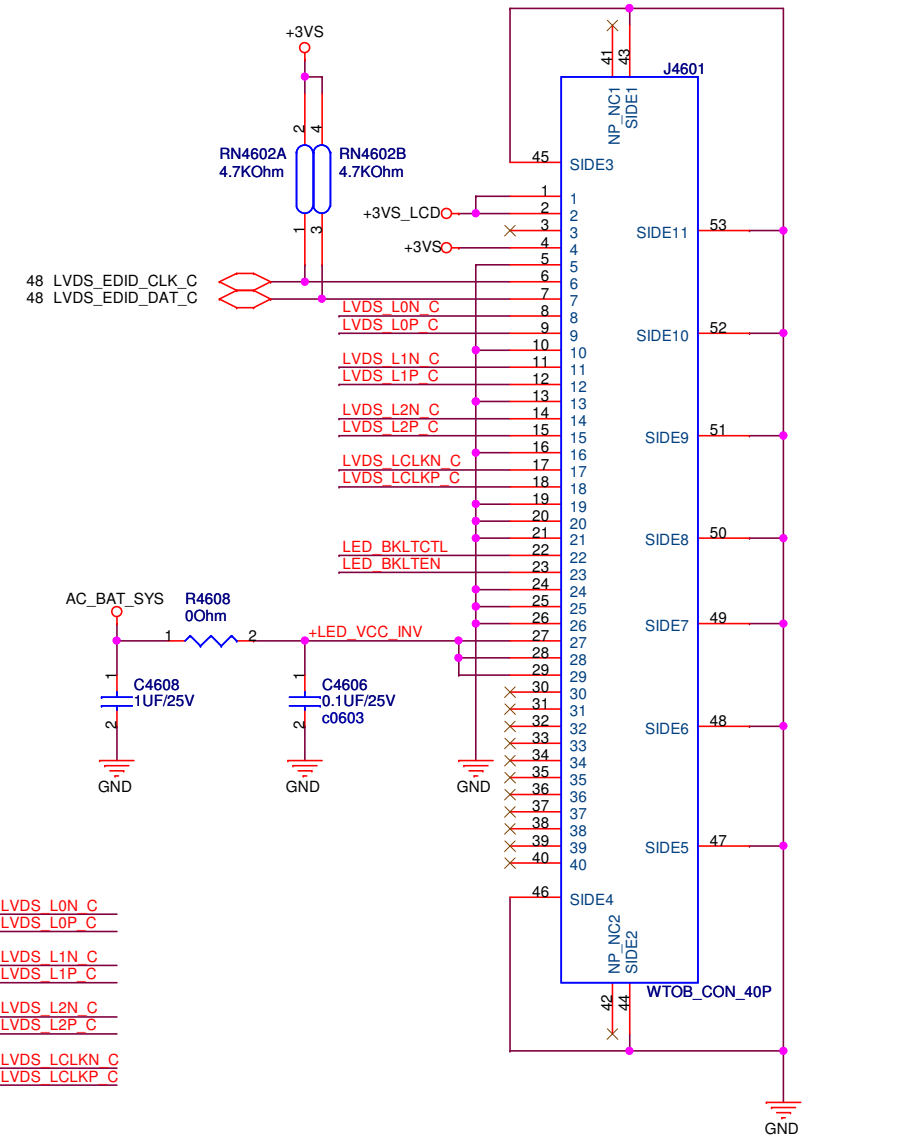
ASUS		Title :BUG DEBUG PORT
ASUSTeK COMPUTER INC		Engineer: Tony Su
Size A	Project Name UX50	Rev 1.0a
Date: Tuesday, March 31, 2009		Sheet 44 of 97



LCD Power



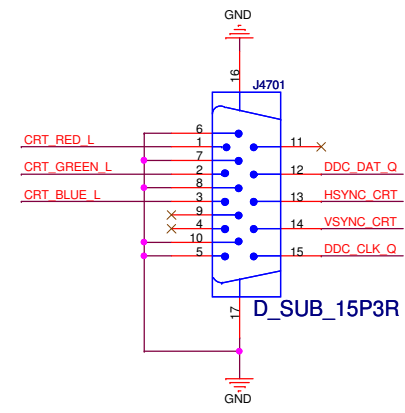
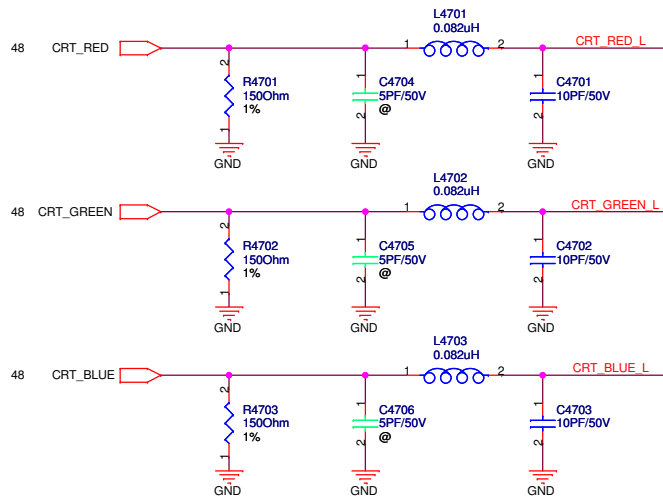
LVDS CONN



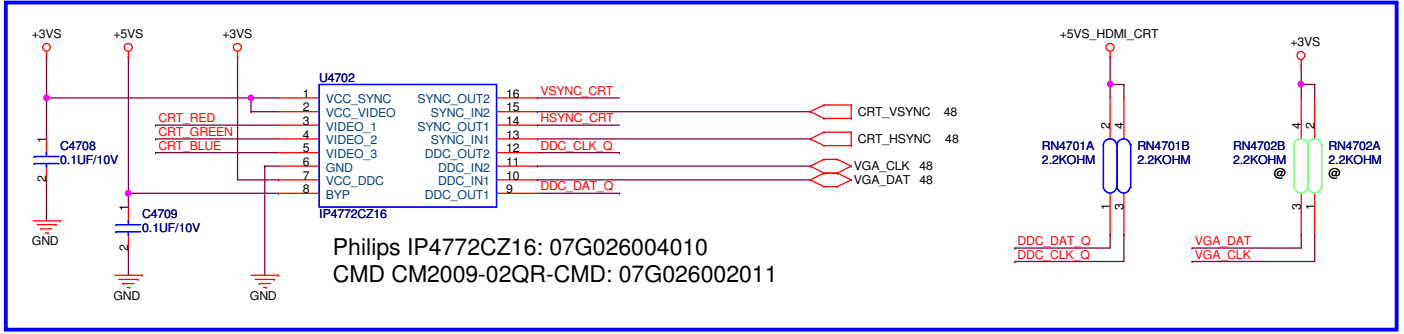
<Variant Name>

		Title :CRT LVDS CONN	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name	Rev	
Custom	UX50	1.0a	
Date: Tuesday, March 31, 2009		Sheet	46 of 97

CRT Connector



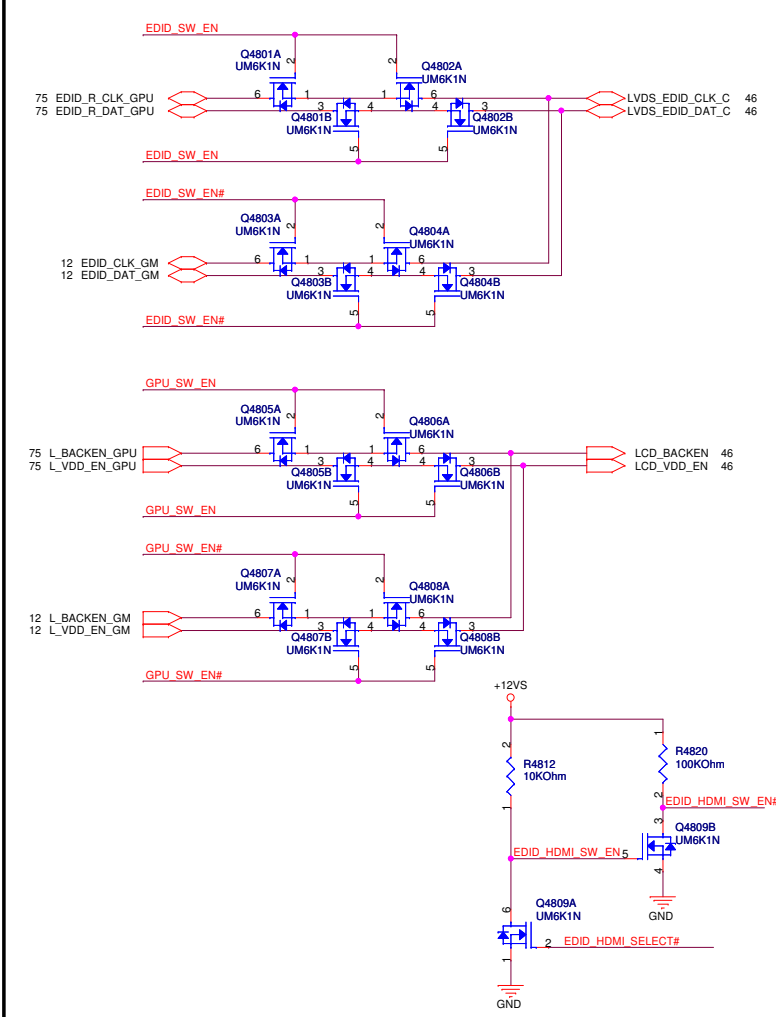
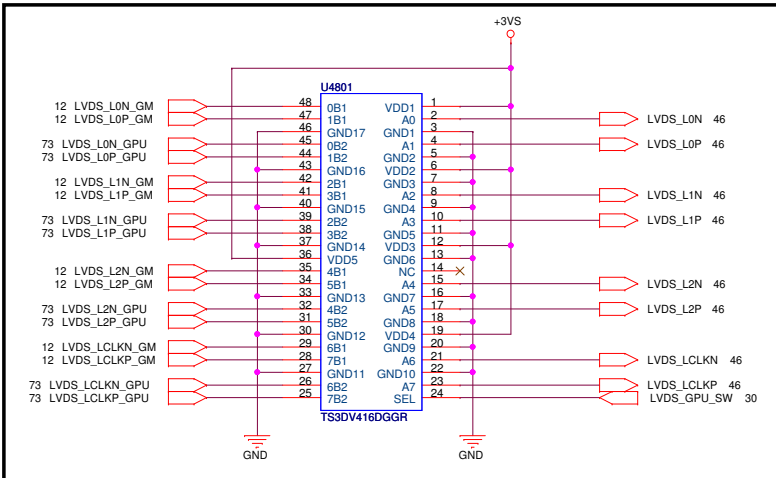
PLACE ESD IC near J4701



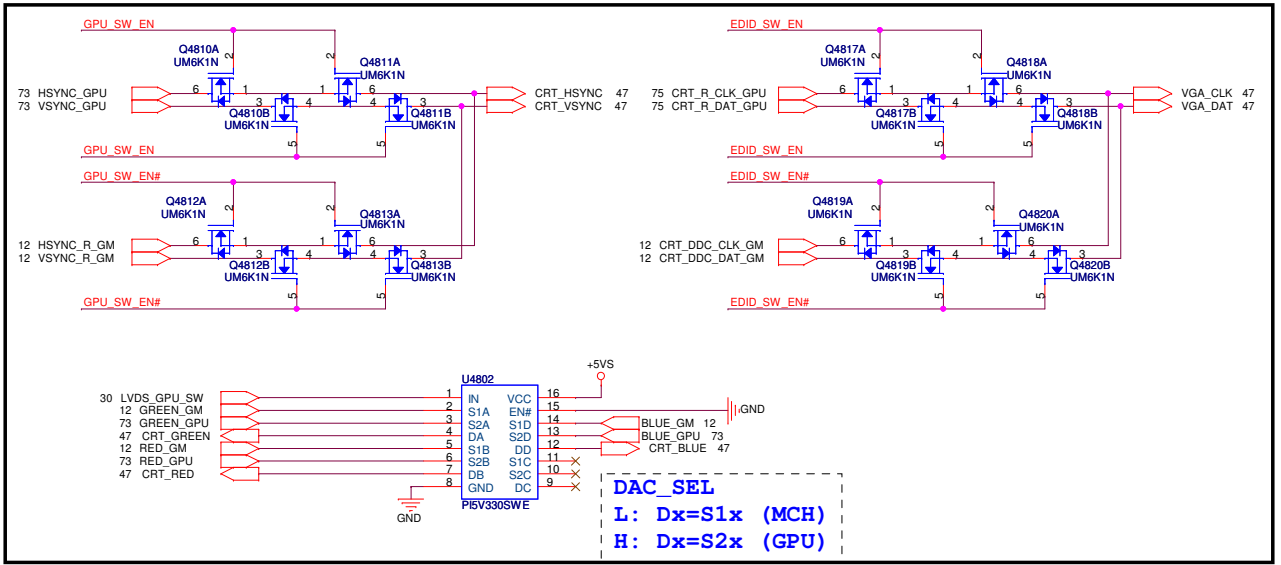
<Variant Name>

ASUS		Title : CRT D-SUB CONN
ASUSTeK COMPUTER INC		Engineer: Tony Su
Size Custom	Project Name UX50	Rev 1.0a
Date: Tuesday, March 31, 2009	Sheet 47 of 97	

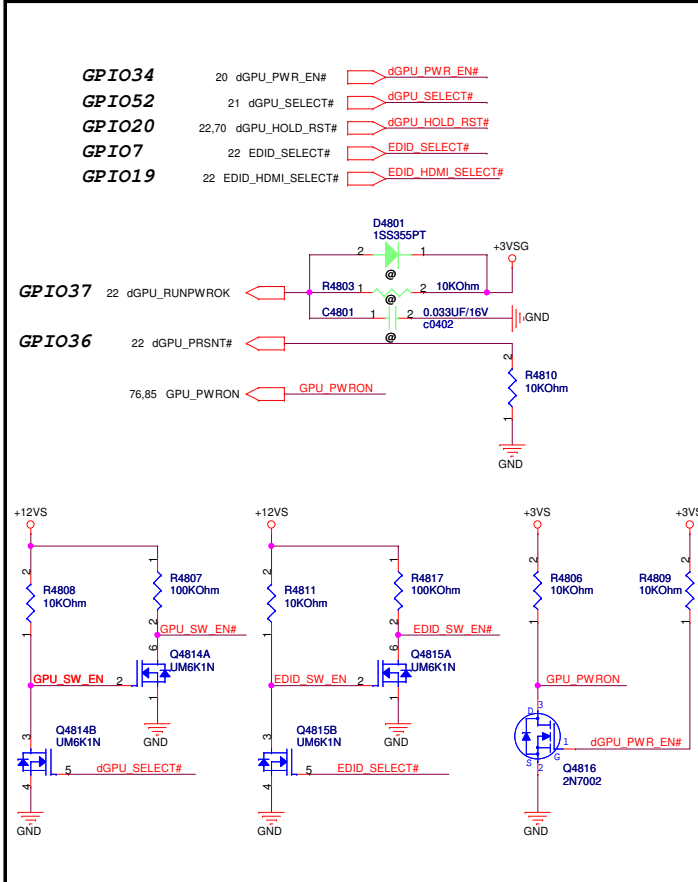
LVDS Switch



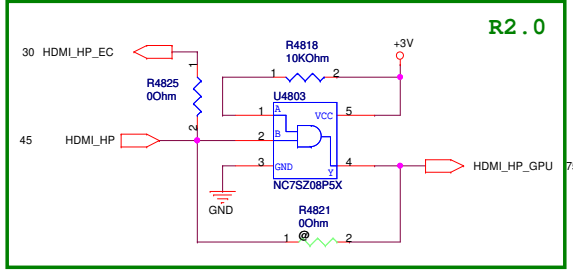
CRT Switch



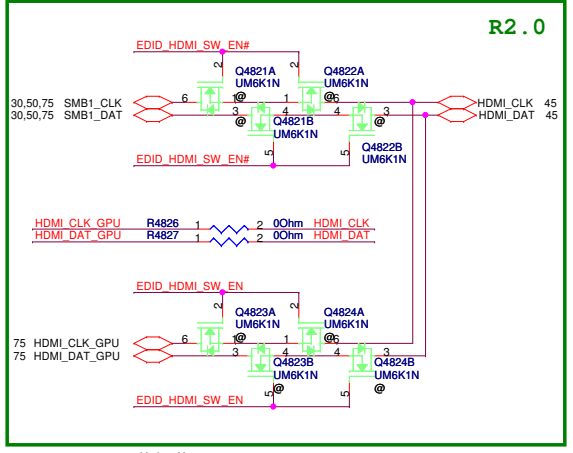
Control Signal from ICH9M



HDMI Hot-Plug Detect Switch



HDMI I2C Switch



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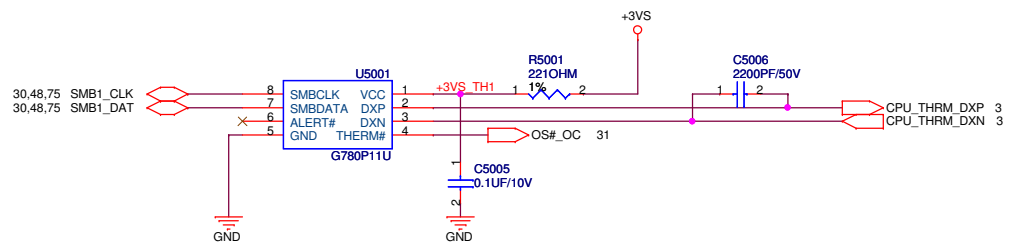
A

A

<Variant Name>

		Title : CRT D-SUB CONN	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name	Rev	
Custom	UX50	1.0a	
Date: <u>Tuesday, March 31, 2009</u>		Sheet	49 of 97

Thermal Seneor



1nd: 06G023096010 G780P11U SOP-8
 2nd: 06G023026012 MAX6657YMS+ SOP-8

Route CPU_THRM_DA , CPU_THRM_DC and MEM_THERM_DA , MEM_THERM_DC on the same layer

```

-----OTHER SIGNALS
10 mils
=====GND
10 mils
=====H_THERMDA(10 mils)
10 mils
=====H_THERMDC(10 mils)
10 mils
=====GND
10 mils
-----OTHER SIGNALS

Avoid FSB,Power
    
```

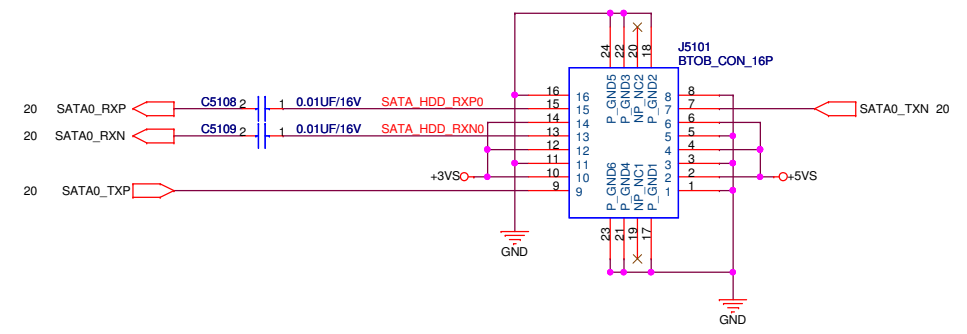
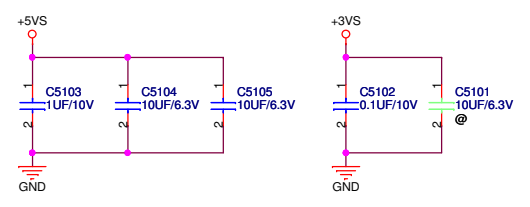
<Variant Name> **FAN THERMAL SENSOR FAN CONN**

ASUS Title :

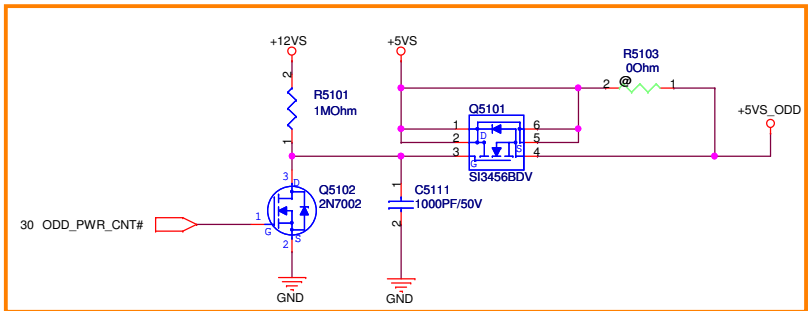
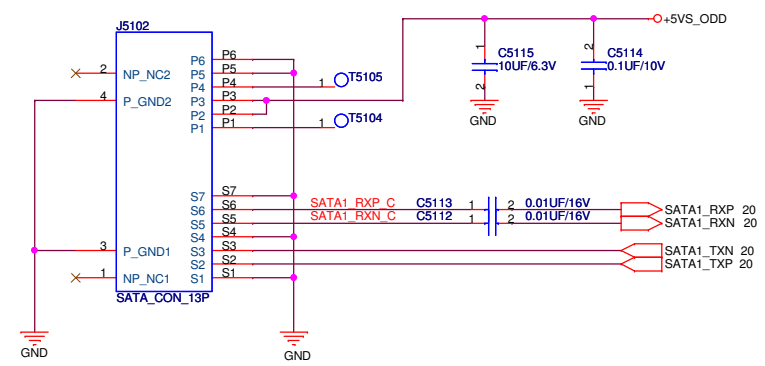
ASUSTeK COMPUTER INC Engineer: **Tony Su**

Size	Project Name	Rev
Custom	UX50	1.0a
Date: Tuesday, March 31, 2009	Sheet 50 of 97	

SATA HDD



SATA ODD




<Variant Name>

ASUS		Title: YDD SATA HDD CONN	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name	Rev	
Custom	UX50	1.0a	
Date: Tuesday, March 31, 2009	Sheet	51	of 97



<Variant Name>

		Title :USB 2.0 CONN*1
ASUSTek COMPUTER INC		Engineer: <i>Tony Su</i>
Size Custom	Project Name UX50	Rev 1.0a
Date: <u>Tuesday, March 31, 2009</u>		Sheet 52 of 97

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C

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A

		Title : PCI_Minicard	
ASUSTeK COMPUTER INC. NB1		Engineer: Tony Su	
Size	Project Name	Rev	
Custom	UX50	1.00	
Date: <u>Tuesday, March 31, 2009</u>		Sheet	53 of 97

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>
Size	Project Name	Rev
A	UX50	1.0a
Date: Tuesday, March 31, 2009		Sheet 54 of 97

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>
Size A	Project Name UX50	Rev 1.0a
Date: Tuesday, March 31, 2009		Sheet 55 of 97

5

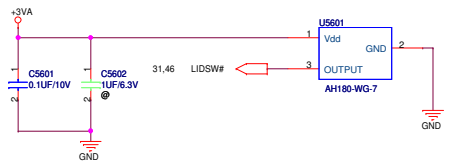
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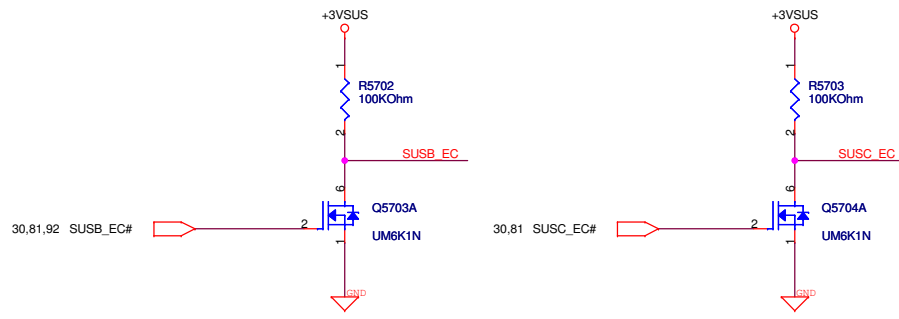
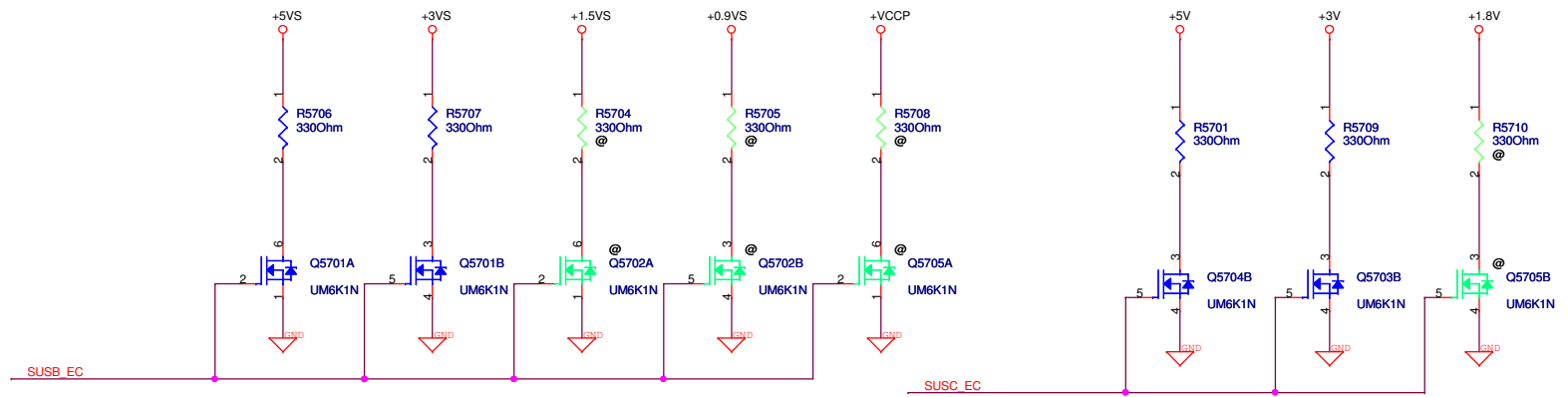
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LID SENSER



Hall Sensor Second Source
06G036012010 Cheap
06G036013010
06G036009011
06G051001012

Discharge Circuit



<Variant Name> **DSC-DISCHARGE CIRCUIT**

ASUS Title : **ASUSTeK COMPUTER INC** Engineer: **Tony Su**

Size	Project Name	Rev
Custom	UX50	1.0a
Date: Tuesday, March 31, 2009	Sheet 57 of 97	

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>
Size A	Project Name UX50	Rev 1.0a
Date: Tuesday, March 31, 2009		Sheet 58 of 97

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<Variant Name>



Title :

ASUSTeK COMPUTER INC

Engineer: *Tony Su*

Size	Project Name	Rev
A	UX50	1.0a

Date: Tuesday, March 31, 2009

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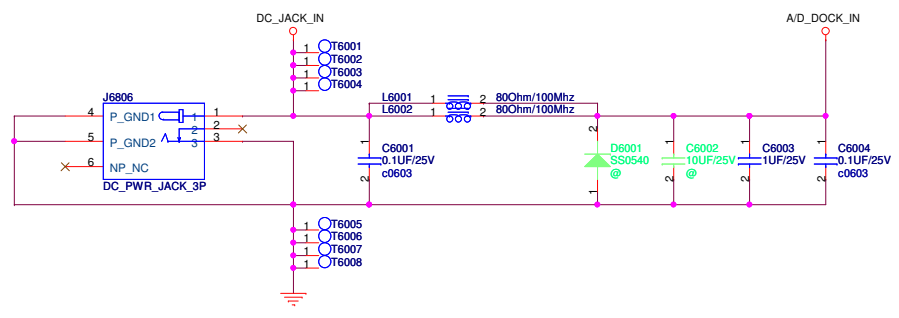
5

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<Variant Name>

		Title: BT BLUETOOTH CONN	
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>	
Size	Project Name		Rev
Custom	UX50		1.0a
Date: <u>Tuesday, March 31, 2009</u>		Sheet	61 of 97

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<Variant Name>

		Title :TPM
ASUSTeK COMPUTER INC		Engineer: Tony Su
Size A	Project Name UX50	Rev 1.0a
Date: Tuesday, March 31, 2009		Sheet 62 of 97

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>
Size	Project Name	Rev
A	UX50	1.0a
Date: Tuesday, March 31, 2009		Sheet 63 of 97

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<Variant Name>



Title :

ASUSTeK COMPUTER INC

Engineer: *Tony Su*

Size	Project Name	Rev
A	UX50	1.0a

Date: Tuesday, March 31, 2009

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5

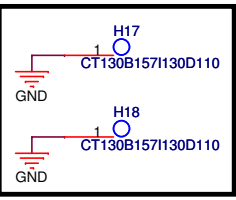
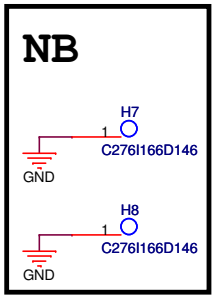
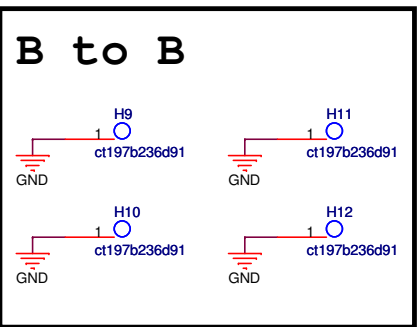
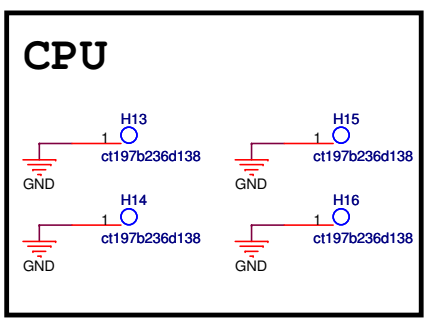
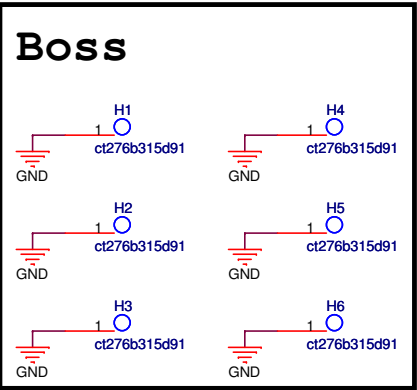
4

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Screw Hole & SMT Nut



<Variant Name>

		ME SCREW HOLE AMT NUT
ASUSTeK COMPUTER INC		Title :
Engineer: <i>Tony Su</i>		
Size	Project Name	Rev
Custom	UX50	1.0a
Date: <u>Tuesday, March 31, 2009</u>		Sheet 65 of 97

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<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>
Size	Project Name	Rev
A	UX50	1.0a
Date: Tuesday, March 31, 2009		Sheet 66 of 97

5

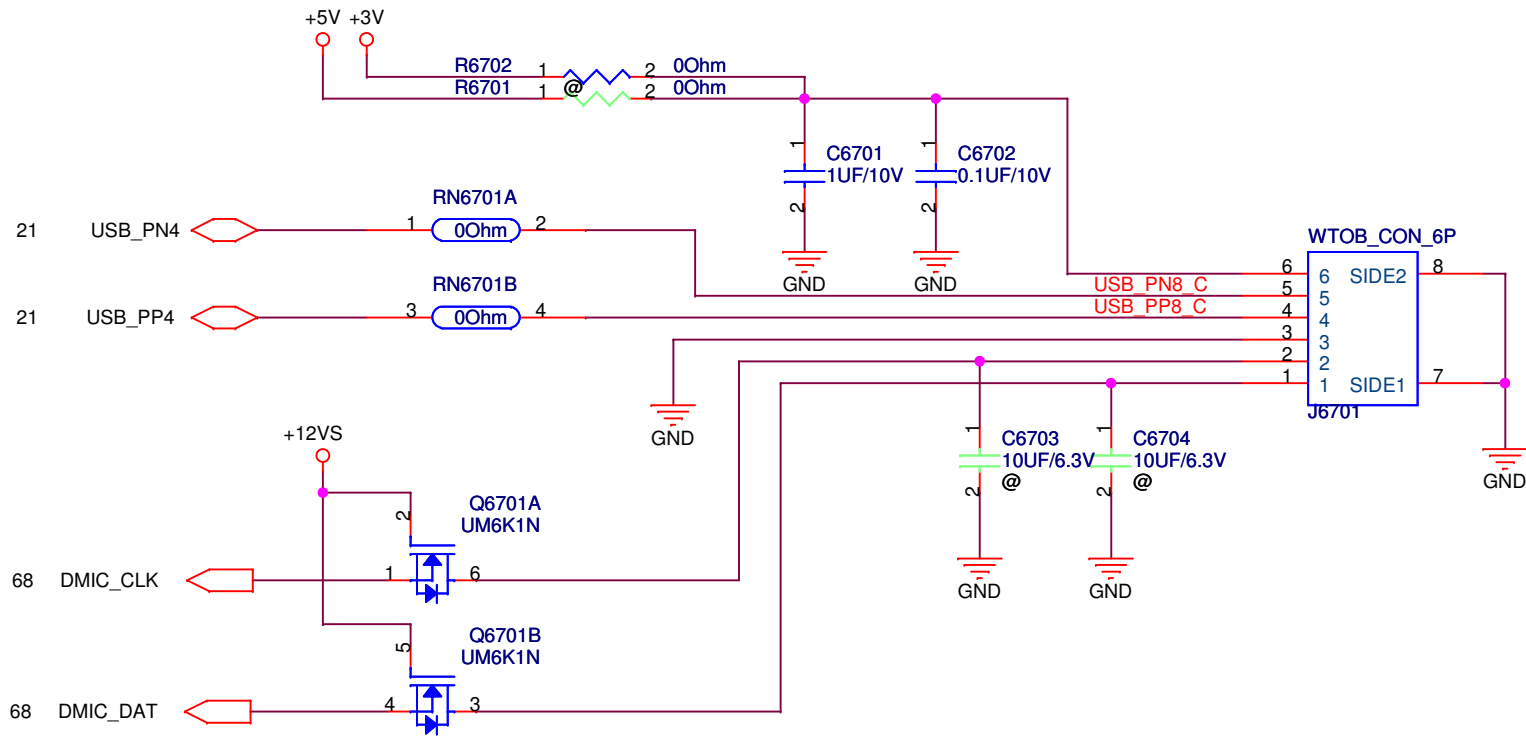
4

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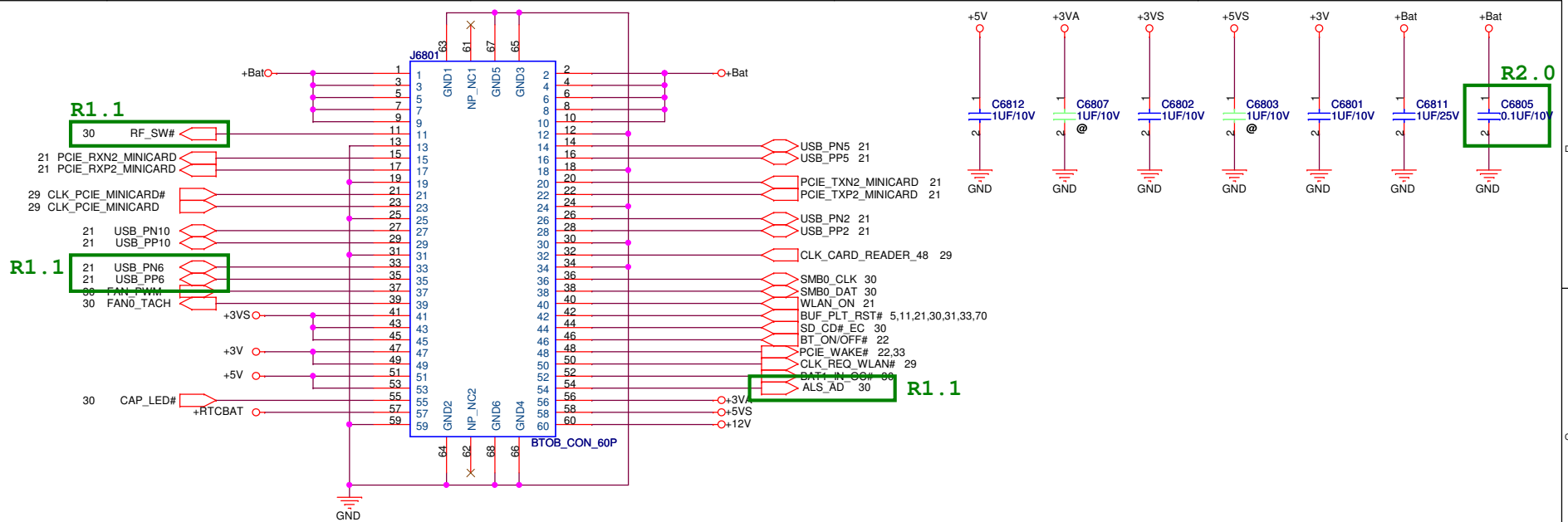
Camera Module



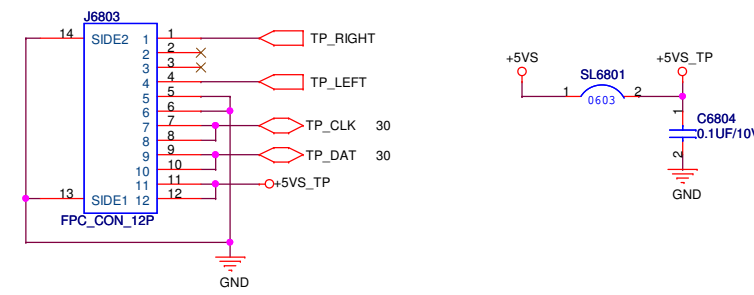
<Variant Name>

		Title : CMOS CAMERA
ASUSTeK COMPUTER INC		Engineer: Tony Su
Size A	Project Name UX50	Rev 1.0a
Date: Tuesday, March 31, 2009		Sheet 67 of 97

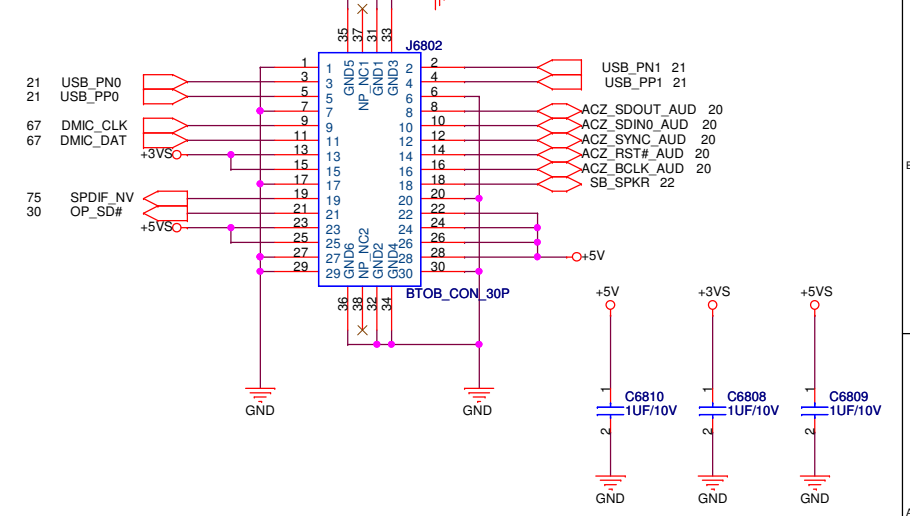
CR Board



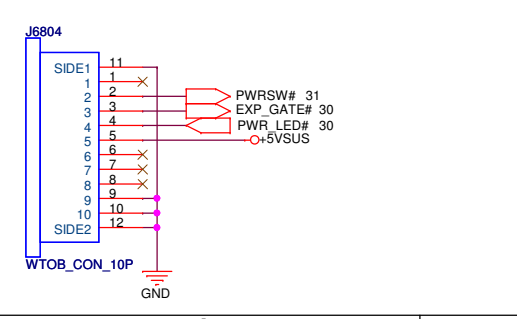
Touch Pad Board



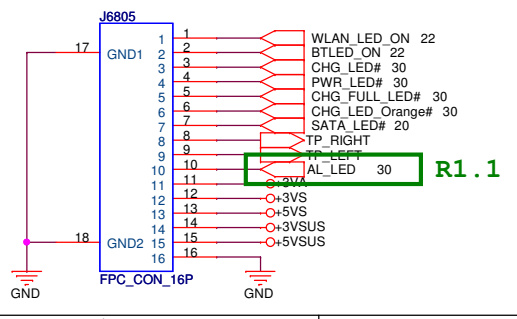
Audio Board



Switch Board



LED Board



<Variant Name>

Title : B TO B CONN

ASUSTeK COMPUTER INC **Engineer: Tony Su**

Size	Project Name	Rev
B	UX50	1.0a


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SYSTEM

+VCCP    +VCCP 3,4,5,10,11,12,14,15,20,23,29,57,76,82




+VCC_GMCH    +VCC_GMCH 14

+VGFX_CORE    +VGFX_CORE 14




+3VS    +3VS 7,8,11,12,15,17,21,22,23,24,29,30,31,45,46,47,48,50,51,57,68,80,91,92




+12VS    +12VS 22,46,48,51,67,91




+VCORE    +VCORE 4,5,80

+1.5VS    +1.5VS 4,15,20,23,57,84

AC_BAT_SYS    AC_BAT_SYS 46,80,81,82,83,85,86,88

+5V    +5V 31,57,67,68,91



+5VS    +5VS 23,45,47,48,51,57,68,80,84,91




+3VA    +3VA 20,30,31,56,68,81,88

+VCC_RTC    +VCC_RTC 20,23

+3V    +3V 44,46,48,57,67,68,70,91

+5VA    +5VA 81

+3VSUS    +3VSUS 20,21,22,23,30,33,57,68,76,81,85,91,92

+5VSUS    +5VSUS 23,68,80,81,82,83,85,86,88,91


+3VPLL    +3VPLL 30

+3VACC    +3VACC 30

+3VA_ECO    +3VA_EC 30,31

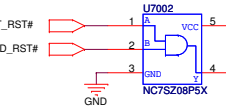
+12V    +12V 68,91

<Variant Name>

		Title :
ASUSTeK COMPUTER INC		Engineer: <i>Tony Su</i>
Size A	Project Name UX50	Rev 1.0a
Date: Tuesday, March 31, 2009		Sheet 69 of 97

PCIEG_RXP[0..15] 12
 PCIEG_RXN[0..15] 12
 PCIEB_RXP[0..15] 12
 PCIEB_RXN[0..15] 12

5,11,21,30,31,33,68 BUF_PLT_RST#
 22 dGPU_HOLD_RST#

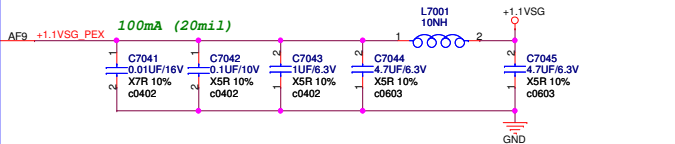
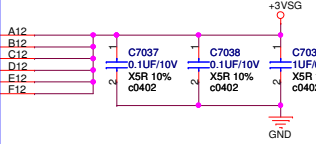
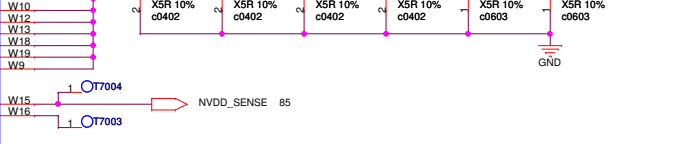
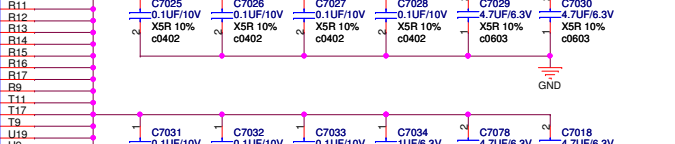
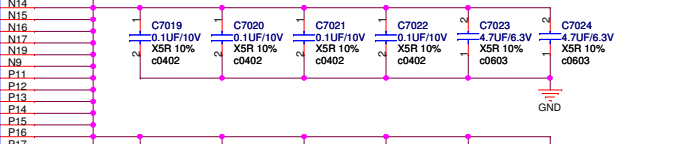
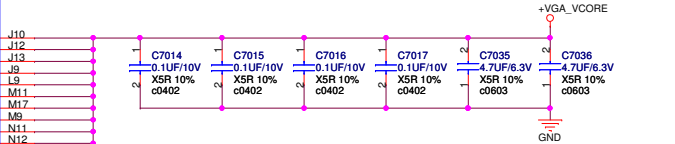
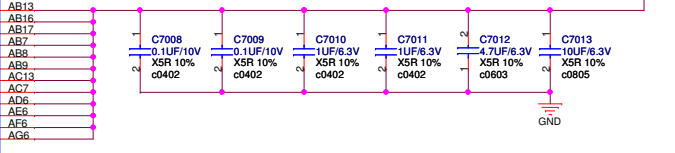
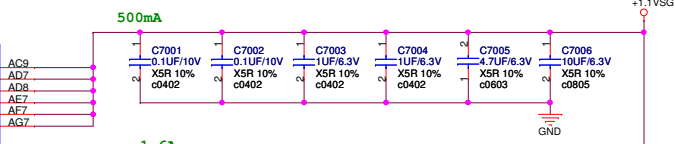
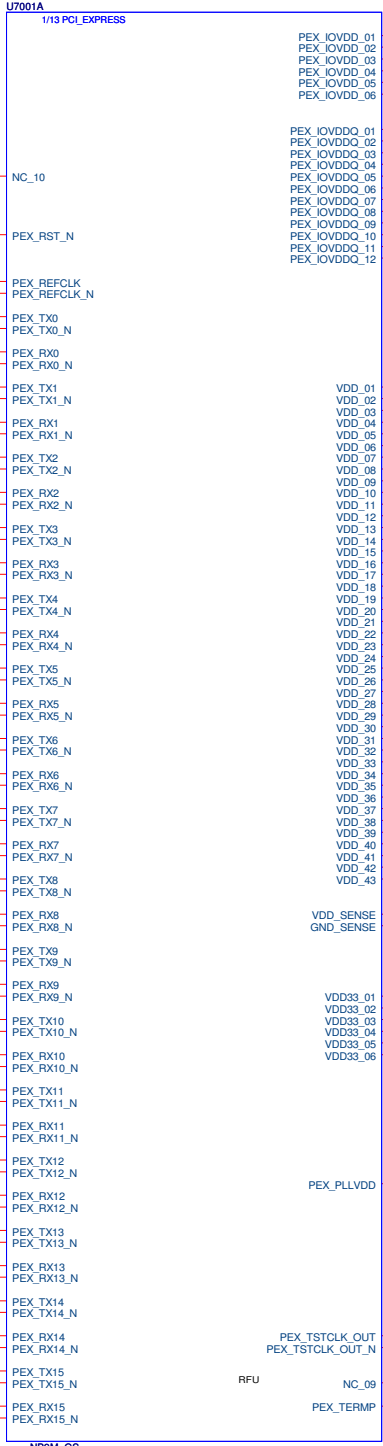


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PCIEB_RXP15	C7062	1	2	0.1UF/10V	PCIEG_TXP15
PCIEB_RXN14	C7047	1	2	0.1UF/10V	PCIEG_TXN14
PCIEB_RXP14	C7063	1	2	0.1UF/10V	PCIEG_TXP14
PCIEB_RXN13	C7048	1	2	0.1UF/10V	PCIEG_TXN13
PCIEB_RXP13	C7064	1	2	0.1UF/10V	PCIEG_TXP13
PCIEB_RXN12	C7049	1	2	0.1UF/10V	PCIEG_TXN12
PCIEB_RXP12	C7065	1	2	0.1UF/10V	PCIEG_TXP12
PCIEB_RXN11	C7050	1	2	0.1UF/10V	PCIEG_TXN11
PCIEB_RXP11	C7066	1	2	0.1UF/10V	PCIEG_TXP11
PCIEB_RXN10	C7051	1	2	0.1UF/10V	PCIEG_TXN10
PCIEB_RXP10	C7067	1	2	0.1UF/10V	PCIEG_TXP10
PCIEB_RXN9	C7052	1	2	0.1UF/10V	PCIEG_TXN9
PCIEB_RXP9	C7068	1	2	0.1UF/10V	PCIEG_TXP9
PCIEB_RXN8	C7053	1	2	0.1UF/10V	PCIEG_TXN8
PCIEB_RXP8	C7069	1	2	0.1UF/10V	PCIEG_TXP8
PCIEB_RXN7	C7054	1	2	0.1UF/10V	PCIEG_TXN7
PCIEB_RXP7	C7070	1	2	0.1UF/10V	PCIEG_TXP7
PCIEB_RXN6	C7055	1	2	0.1UF/10V	PCIEG_TXN6
PCIEB_RXP6	C7071	1	2	0.1UF/10V	PCIEG_TXP6
PCIEB_RXN5	C7056	1	2	0.1UF/10V	PCIEG_TXN5
PCIEB_RXP5	C7072	1	2	0.1UF/10V	PCIEG_TXP5
PCIEB_RXN4	C7057	1	2	0.1UF/10V	PCIEG_TXN4
PCIEB_RXP4	C7073	1	2	0.1UF/10V	PCIEG_TXP4
PCIEB_RXN3	C7058	1	2	0.1UF/10V	PCIEG_TXN3
PCIEB_RXP3	C7074	1	2	0.1UF/10V	PCIEG_TXP3
PCIEB_RXN2	C7059	1	2	0.1UF/10V	PCIEG_TXN2
PCIEB_RXP2	C7075	1	2	0.1UF/10V	PCIEG_TXP2
PCIEB_RXN1	C7060	1	2	0.1UF/10V	PCIEG_TXN1
PCIEB_RXP1	C7076	1	2	0.1UF/10V	PCIEG_TXP1
PCIEB_RXN0	C7061	1	2	0.1UF/10V	PCIEG_TXN0
PCIEB_RXP0	C7077	1	2	0.1UF/10V	PCIEG_TXP0

28 CLK_PCIE_VGA
 29 CLK_PCIE_VGA#



NB9M_RST#_AD9



ASUS Title :
 ASUSTeK COMPUTER INC. NBI Engineer: Tony Su
 Size Project Name
 Custom UX50
 Date: Tuesday, March 31, 2009 Sheet 70 of 97

72 FBAD[0..63]
72 FBADQM[0..7]
72 FBAWDS[0..7]
72 FBARDQS[0..7]

U7001B
2/13 FRAME_BUFFER

- FBAD0 D21 FBA_D0
- FBAD1 C22 FBA_D1
- FBAD2 A22 FBA_D2
- FBAD3 A22 FBA_D3
- FBAD4 C24 FBA_D4
- FBAD5 B25 FBA_D5
- FBAD6 A25 FBA_D6
- FBAD7 A26 FBA_D7
- FBAD8 D22 FBA_D8
- FBAD9 E22 FBA_D9
- FBAD10 E24 FBA_D10
- FBAD11 D24 FBA_D11
- FBAD12 D26 FBA_D12
- FBAD13 D27 FBA_D13
- FBAD14 C27 FBA_D14
- FBAD15 B27 FBA_D15
- FBAD16 D16 FBA_D16
- FBAD17 E16 FBA_D17
- FBAD18 D17 FBA_D18
- FBAD19 F18 FBA_D19
- FBAD20 D20 FBA_D20
- FBAD21 F20 FBA_D21
- FBAD22 E21 FBA_D22
- FBAD23 F21 FBA_D23
- FBAD24 C18 FBA_D24
- FBAD25 B18 FBA_D25
- FBAD26 C18 FBA_D26
- FBAD27 D18 FBA_D27
- FBAD28 C19 FBA_D28
- FBAD29 C21 FBA_D29
- FBAD30 B21 FBA_D30
- FBAD31 A21 FBA_D31
- FBAD32 C22 FBA_D32
- FBAD33 P24 FBA_D33
- FBAD34 R23 FBA_D34
- FBAD35 R24 FBA_D35
- FBAD36 T23 FBA_D36
- FBAD37 U24 FBA_D37
- FBAD38 V23 FBA_D38
- FBAD39 V24 FBA_D39
- FBAD40 N25 FBA_D40
- FBAD41 N26 FBA_D41
- FBAD42 R25 FBA_D42
- FBAD43 R26 FBA_D43
- FBAD44 T25 FBA_D44
- FBAD45 V26 FBA_D45
- FBAD46 V25 FBA_D46
- FBAD47 V27 FBA_D47
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- FBAD52 A22 FBA_D52
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- FBAD58 W27 FBA_D58
- FBAD59 A25 FBA_D59
- FBAD60 AB25 FBA_D60
- FBAD61 AB26 FBA_D61
- FBAD62 AD26 FBA_D62
- FBAD63 AD27 FBA_D63

- FBADQM0 D25 FBA_DQM0
- FBADQM1 C26 FBA_DQM1
- FBADQM2 D19 FBA_DQM2
- FBADQM3 B19 FBA_DQM3
- FBADQM4 T24 FBA_DQM4
- FBADQM5 T25 FBA_DQM5
- FBADQM6 AA23 FBA_DQM6
- FBADQM7 AB27 FBA_DQM7

- FBAWDS0 A24 FBA_DQS_WP0
- FBAWDS1 C25 FBA_DQS_WP1
- FBAWDS2 E19 FBA_DQS_WP2
- FBAWDS3 A19 FBA_DQS_WP3
- FBAWDS4 T22 FBA_DQS_WP4
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- FBAWDS7 AA26 FBA_DQS_WP7

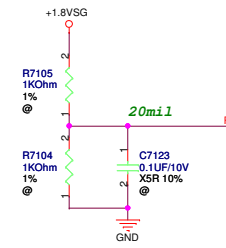
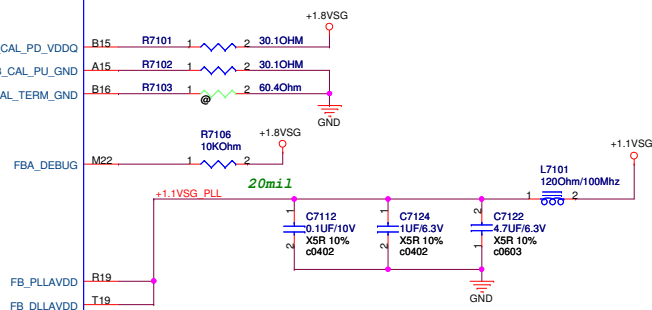
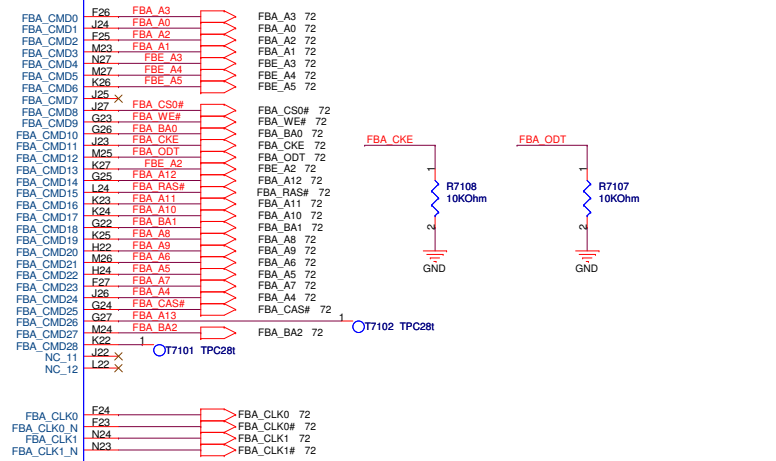
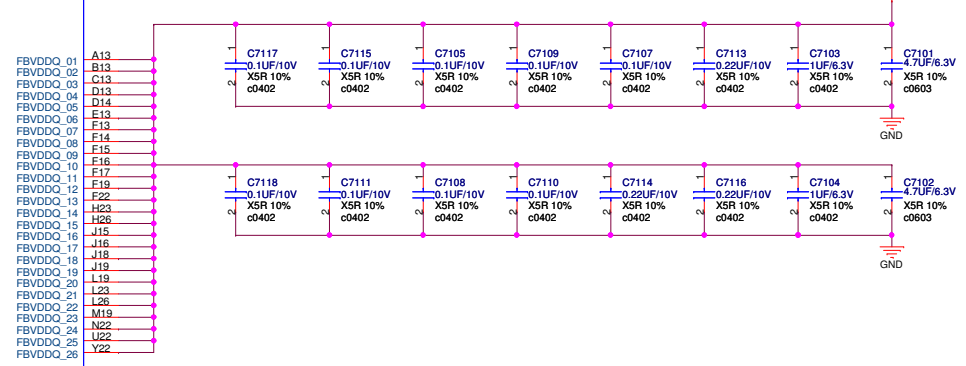
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- FBARDQS1 D25 FBA_DQS_RN1
- FBARDQS2 E18 FBA_DQS_RN2
- FBARDQS3 A18 FBA_DQS_RN3
- FBARDQS4 B22 FBA_DQS_RN4
- FBARDQS5 R27 FBA_DQS_RN5
- FBARDQS6 Y24 FBA_DQS_RN6
- FBARDQS7 AA27 FBA_DQS_RN7

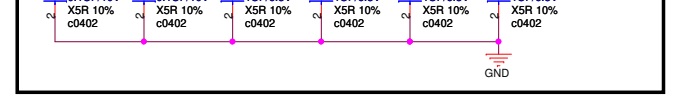
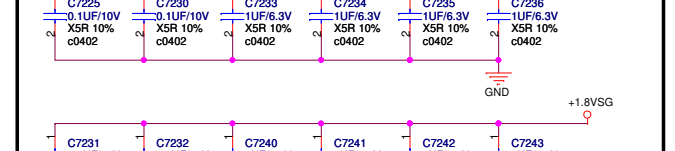
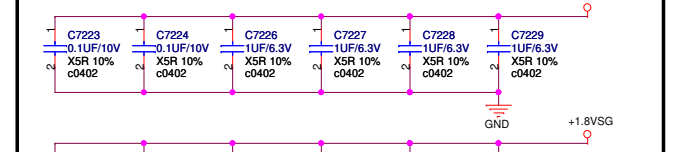
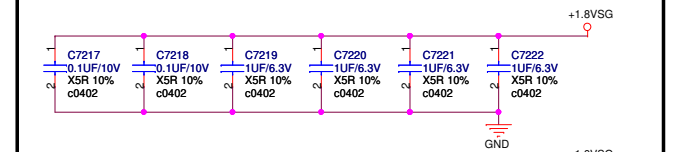
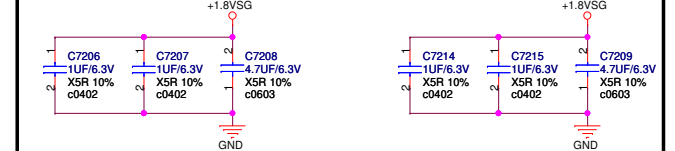
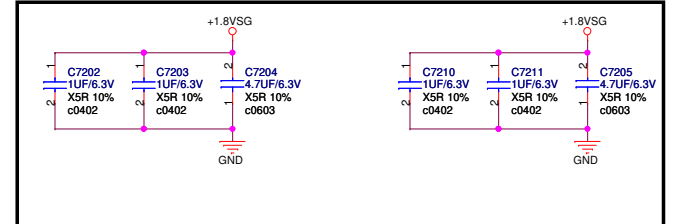
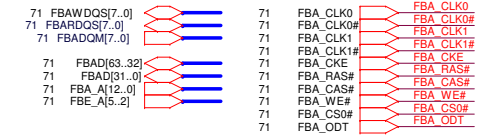
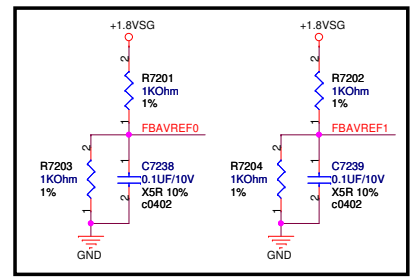
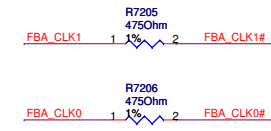
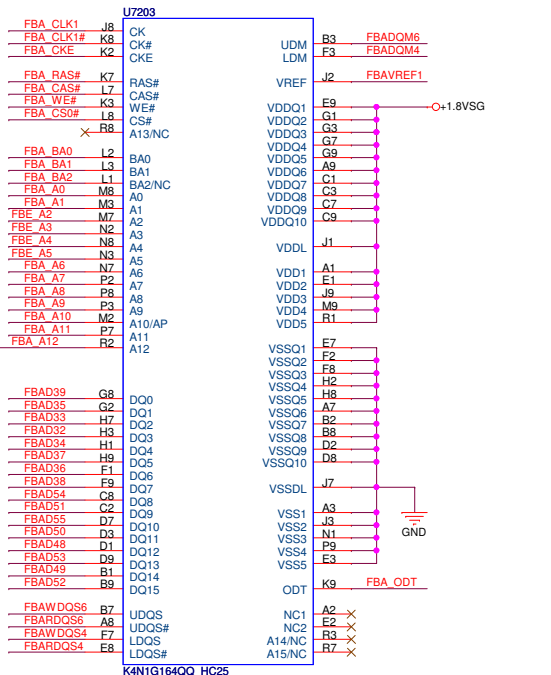
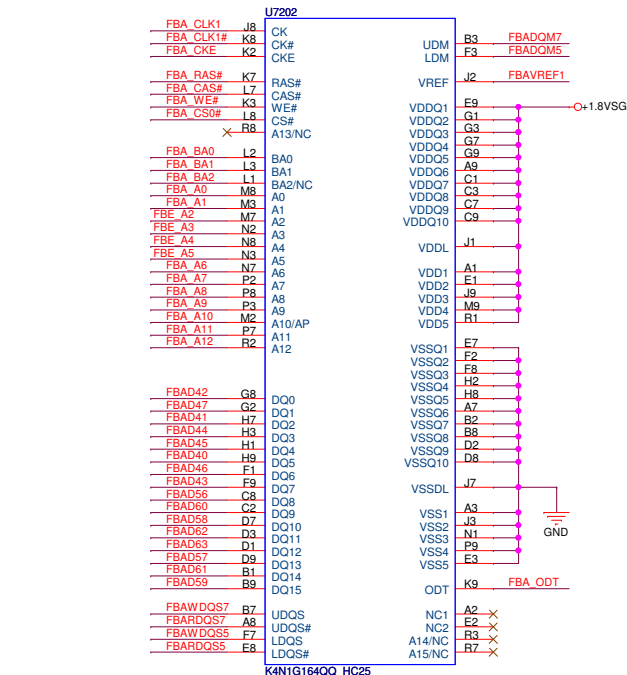
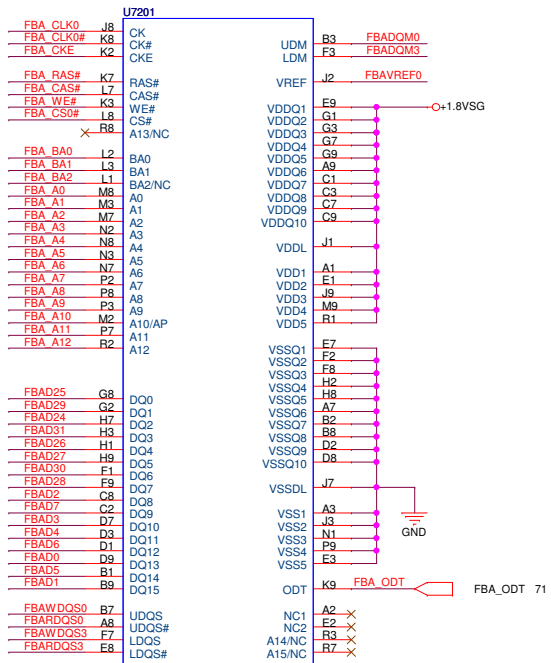
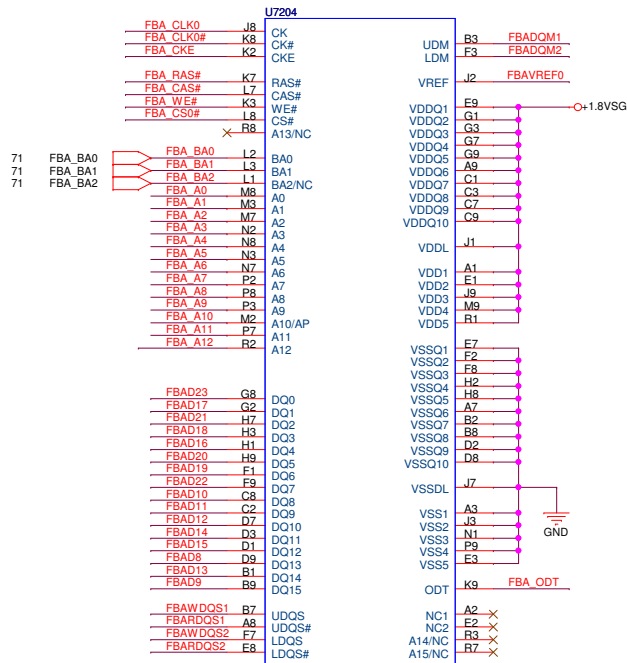
- FB_CAL_PD_VDDQ B15
- FB_CAL_PU_GND A15
- FB_CAL_TERM_GND B16

- FBA_DEBUG M22
- FB_PLLAVDD R19
- FB_DLLAVDD T19

- FB_VREF A16

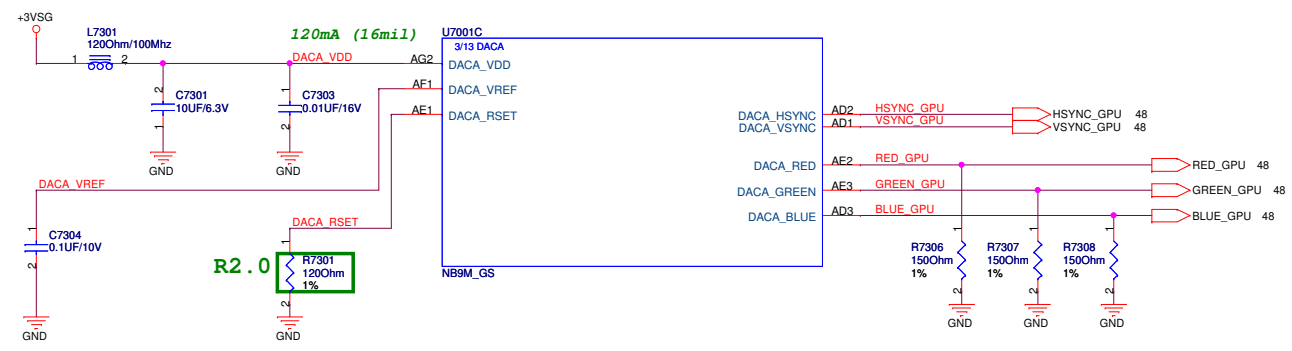
- NB9M_GS



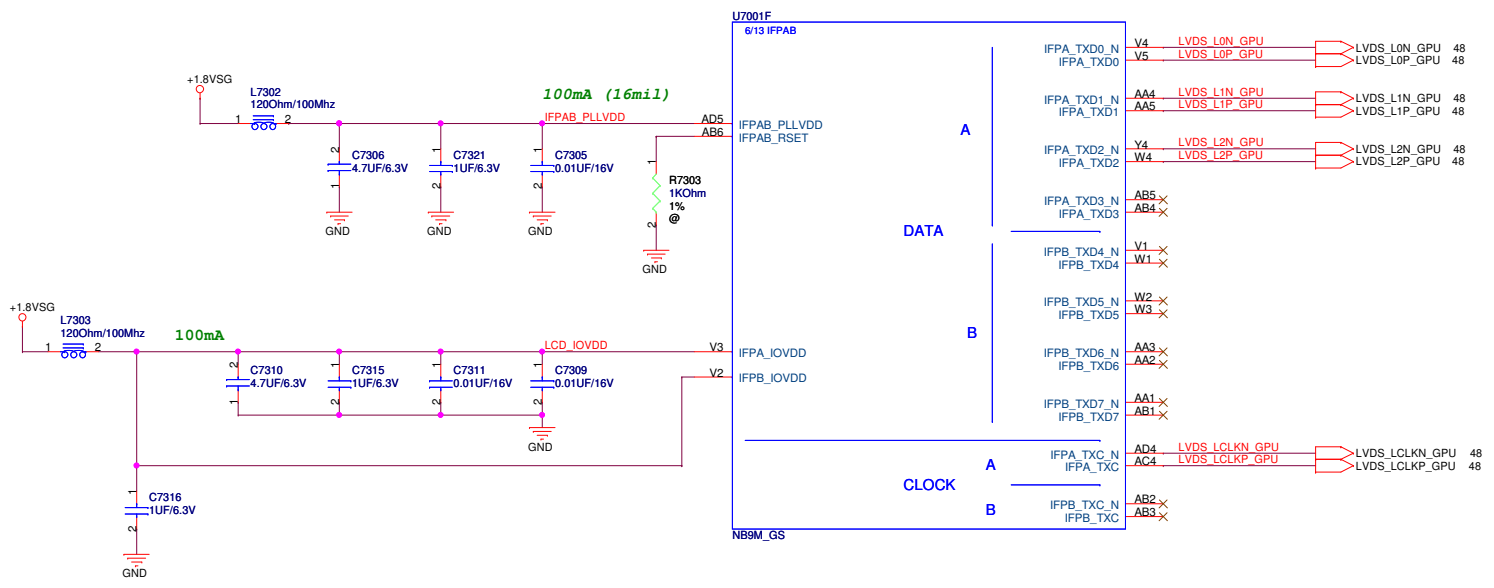


ASUS Title :
ASUSTek COMPUTER INC. NB1 Engineer: **Tony Su**
 Size Project Name
 Custom **UX50** Rev **2.2**
 Date: **Monday, April 06, 2009** Sheet **72** of **97**

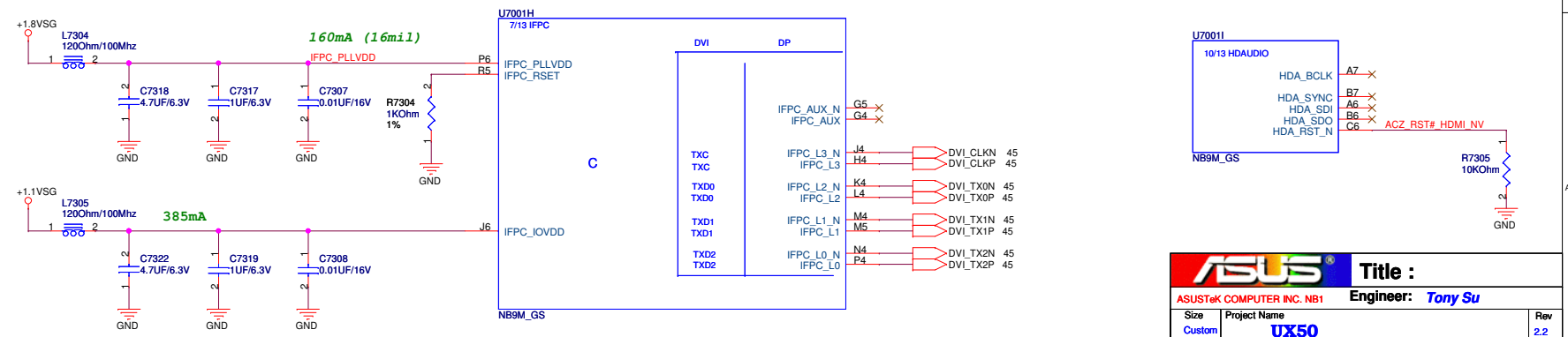
VGA



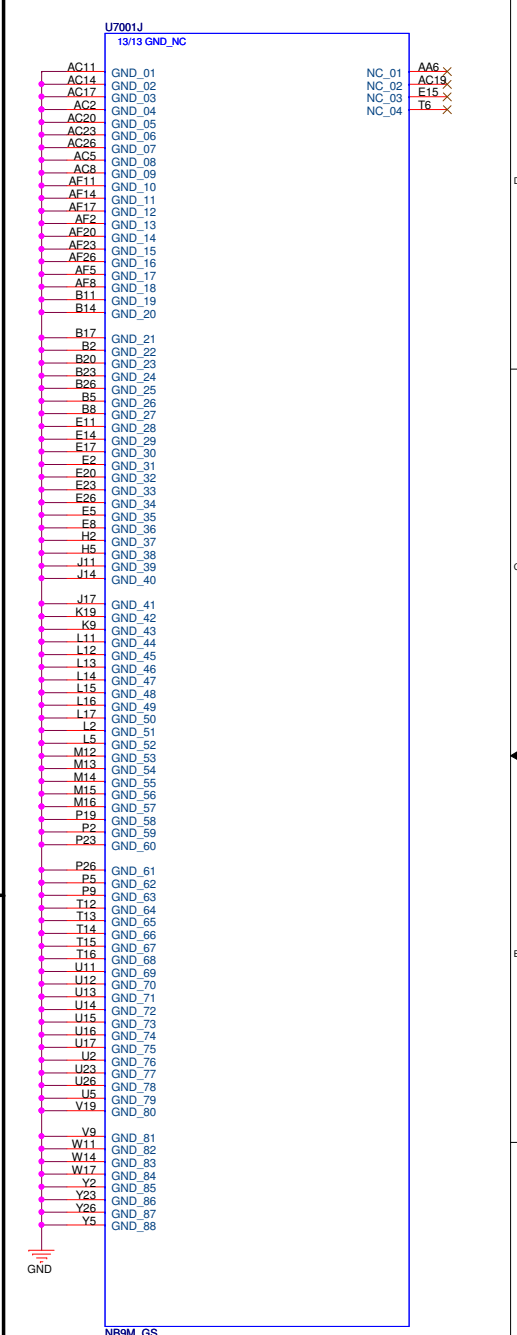
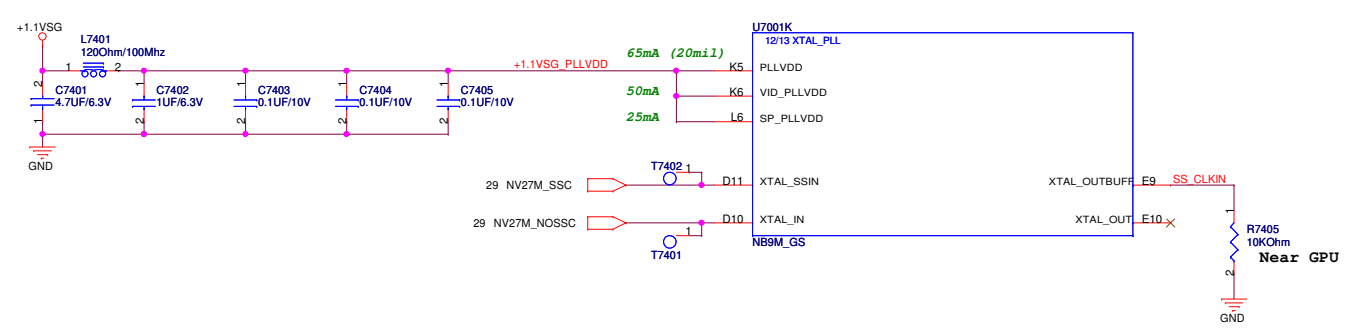
LVDS



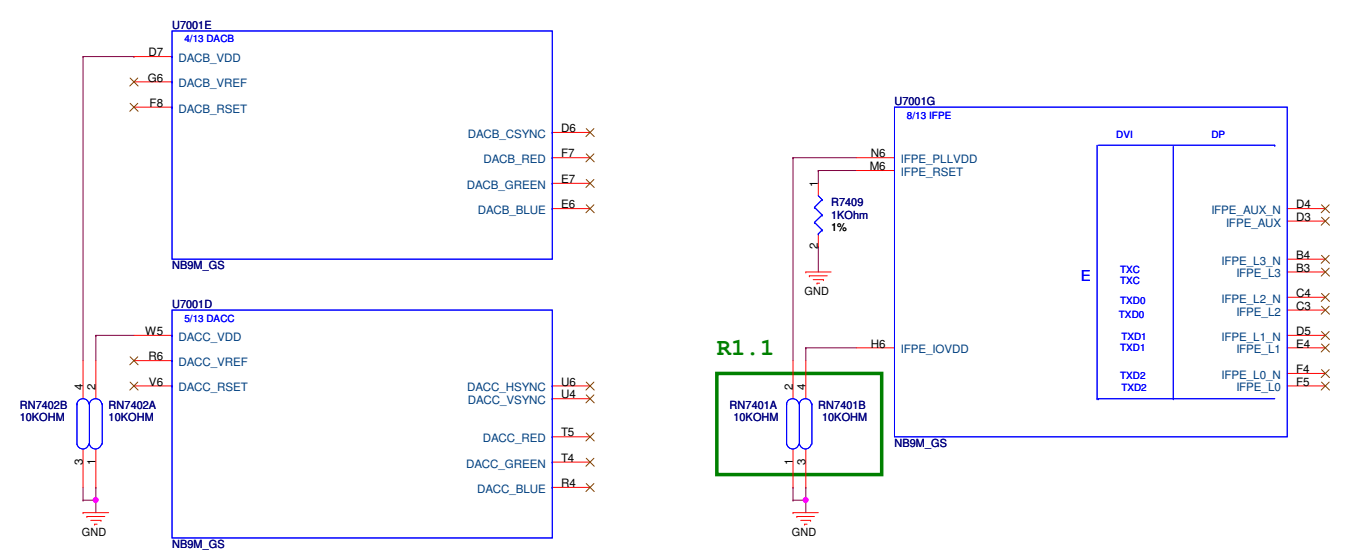
HDMI



Xtal

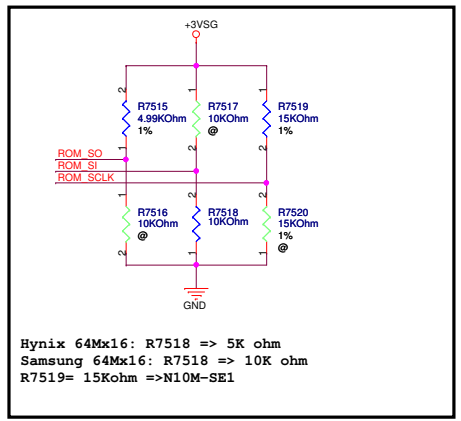
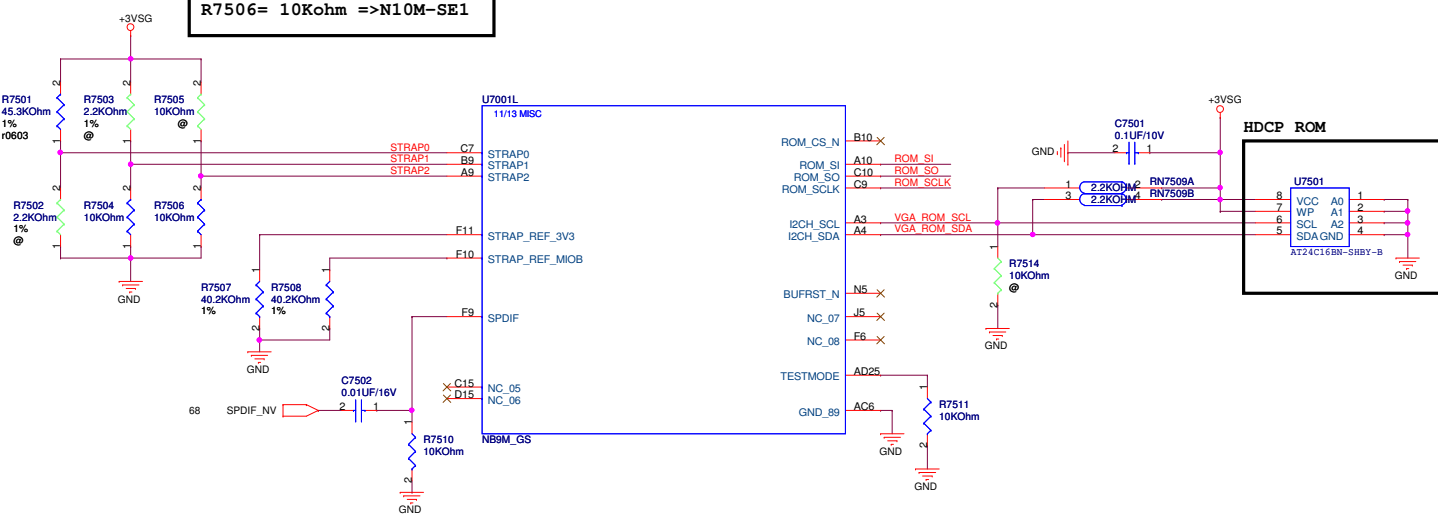


Other



ROM

R7506= 10Kohm =>N10M-SE1

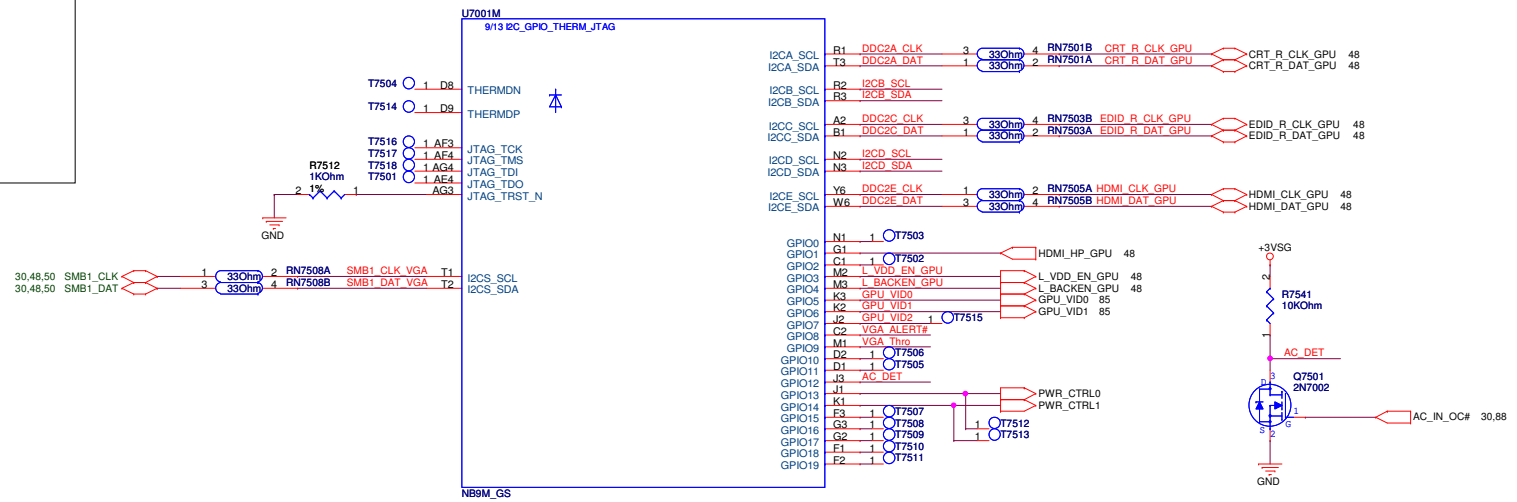
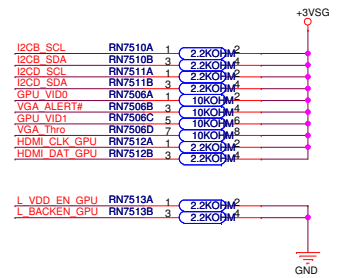


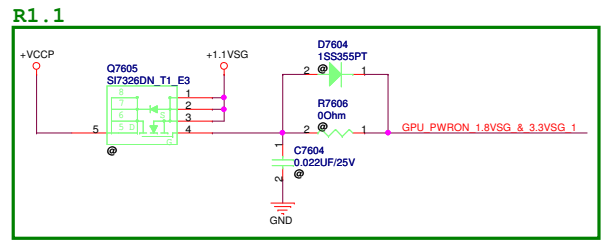
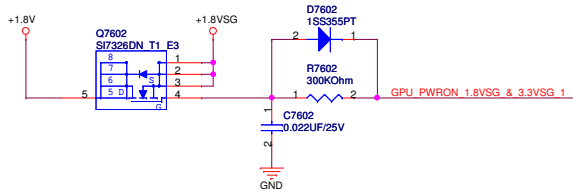
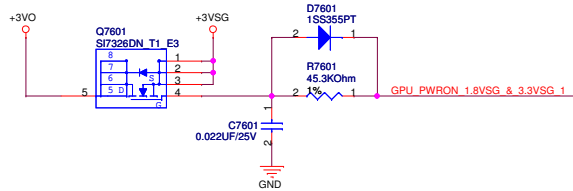
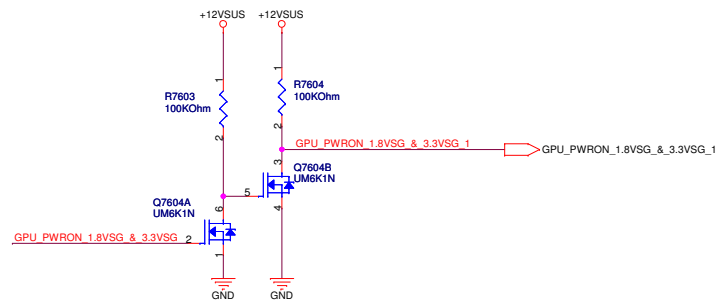
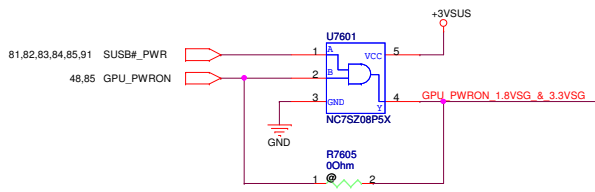
Hynix 64Mx16: R7518 => 5K ohm
 Samsung 64Mx16: R7518 => 10K ohm
 R7519= 15Kohm =>N10M-SE1

GPIO

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	N/A
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID 0
6	OUT	N/A	NVVDD VID 1
7	OUT	N/A	FBVDD VID 0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	PS CONTROL
14	OUT	N/A	PS CONTROL





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Title : Cantiga-POWER(5)

ASUSTeK COMPUTER INC. NB1

Engineer: Tony Su

Size	Project Name	Rev
A	UX50	2.2

Date: **Tuesday, March 31, 2009** Sheet **77** of **97**

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Title : Cantiga-POWER(5)

ASUSTeK COMPUTER INC. NB1

Engineer: Tony Su

Size	Project Name	Rev
A	UX50	2.2

Date: **Tuesday, March 31, 2009**

Sheet **78** of **97**

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Title :

ASUSTeK COMPUTER INC. NB1

Engineer: *Tony Su*

Size	Project Name	Rev
A	UX50	2.2

Date: Tuesday, March 31, 2009 Sheet 79 of 97

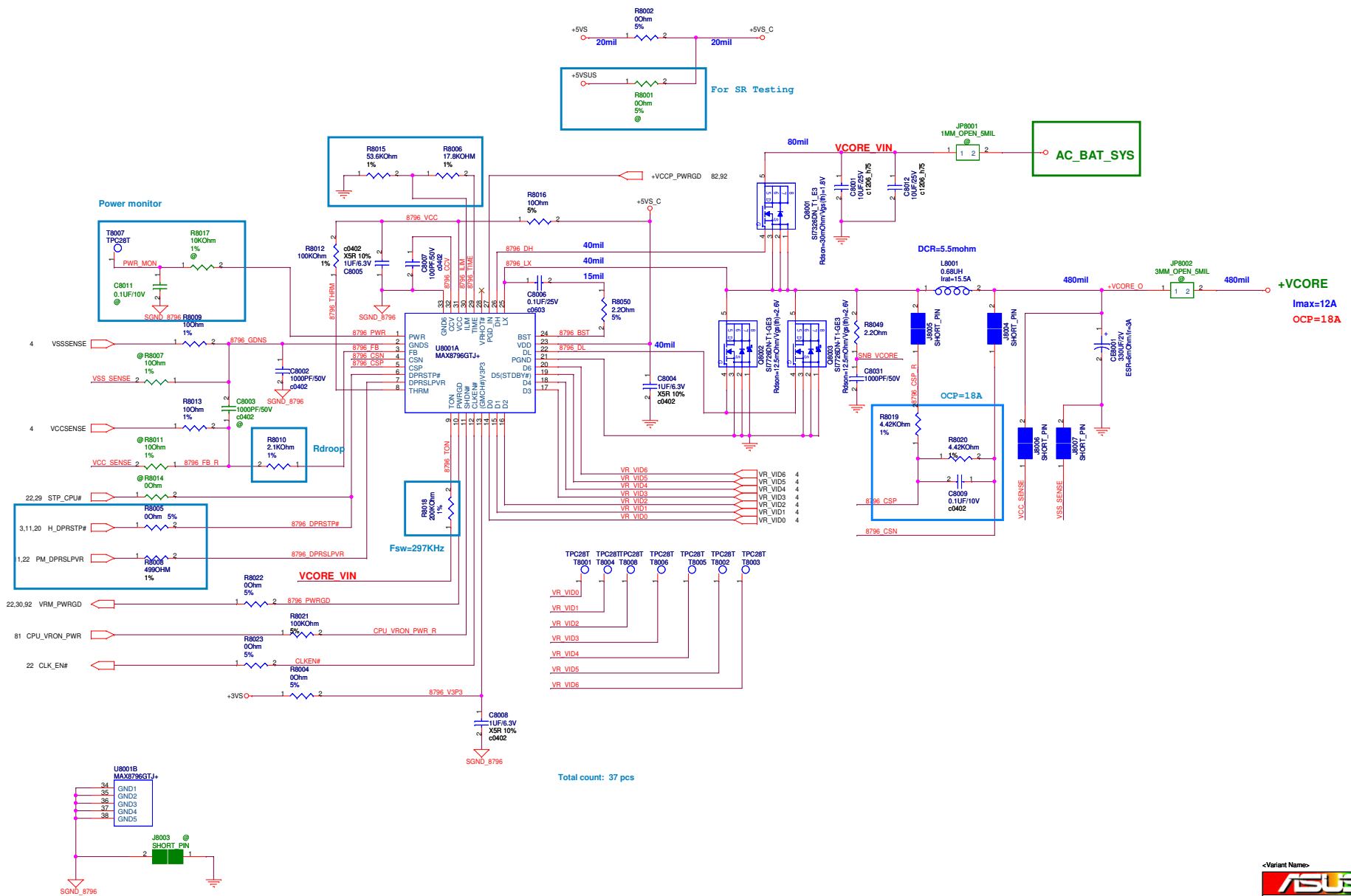
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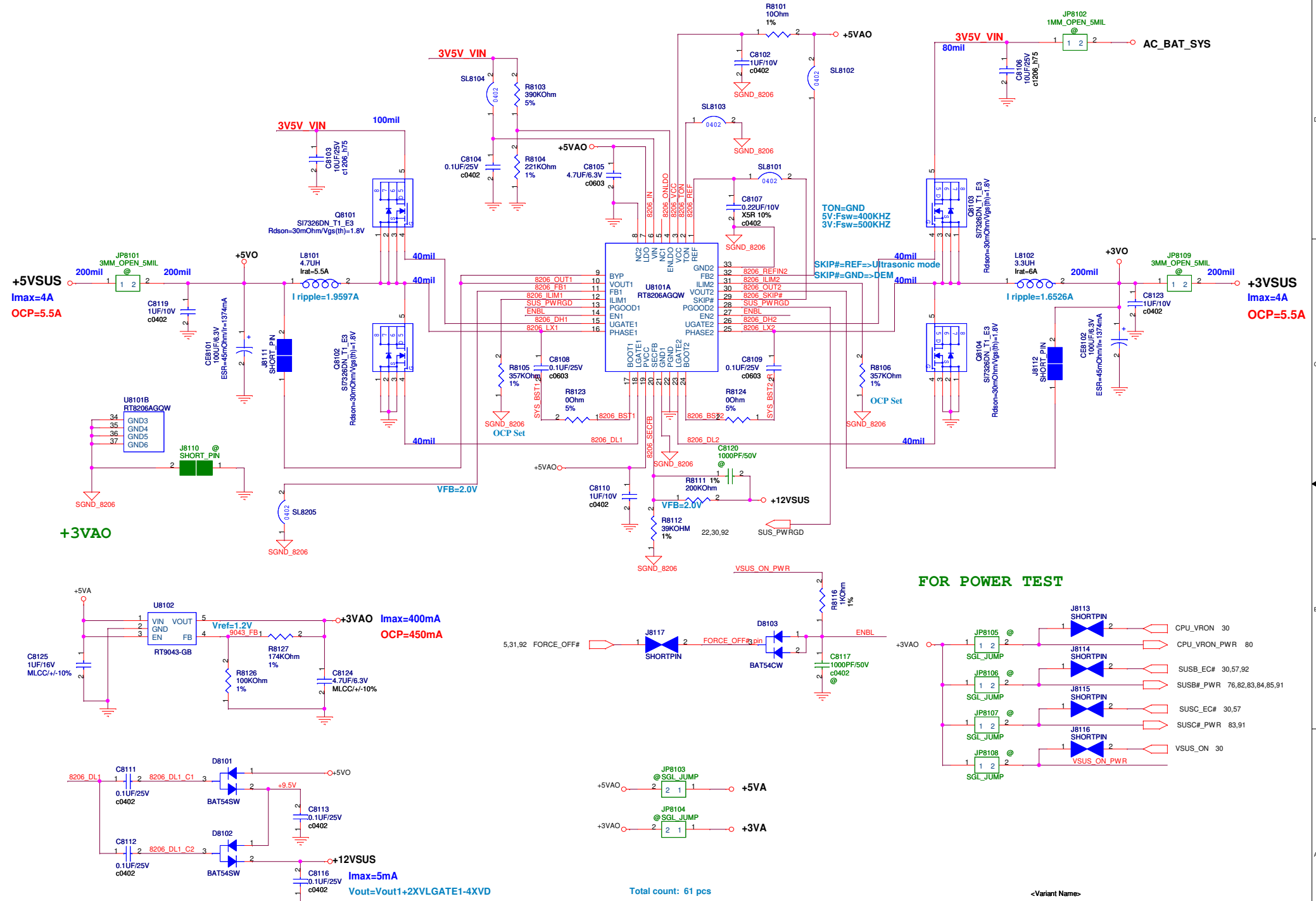
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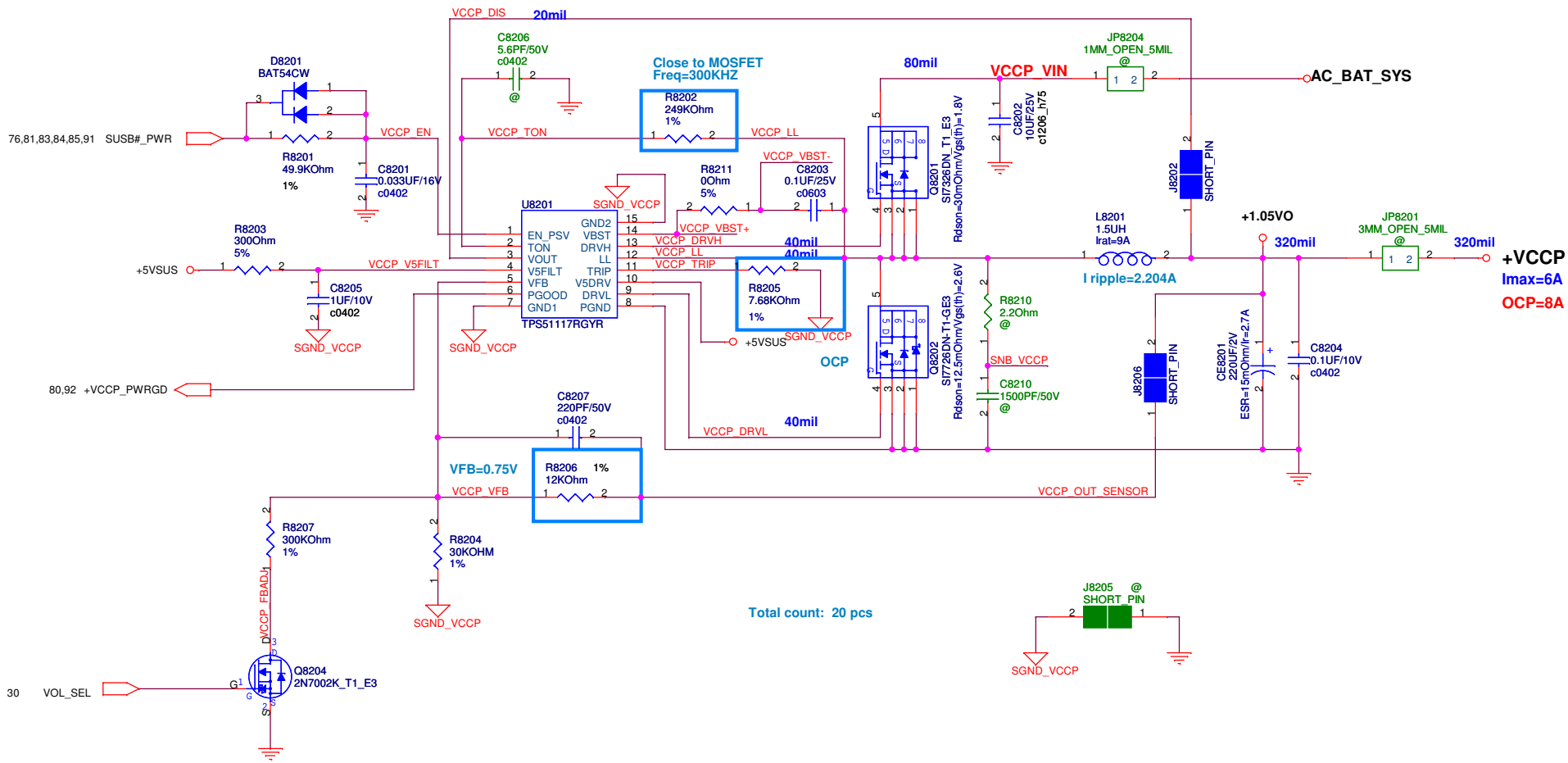


Total count: 37 pcs

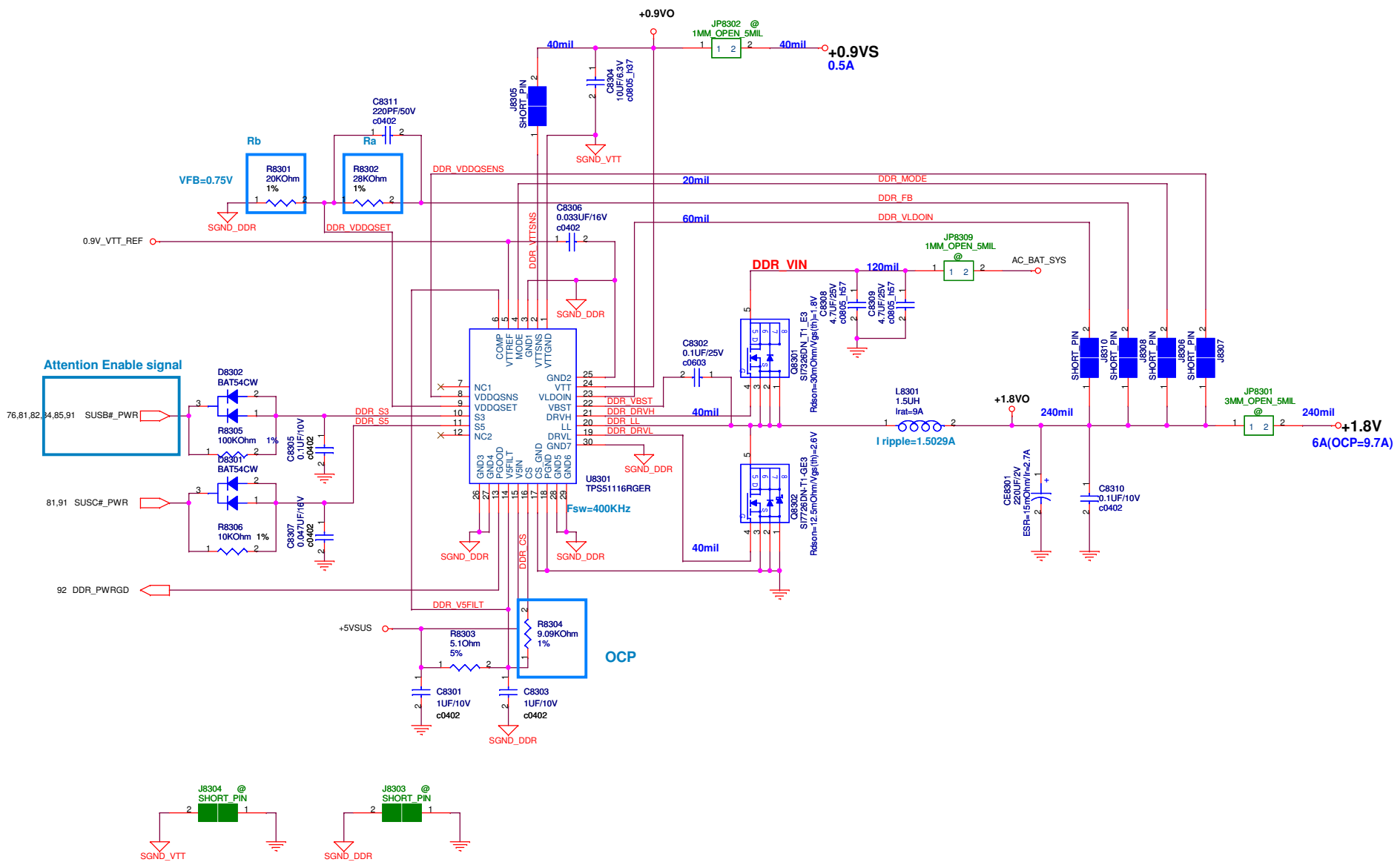
<Variant Names>

ASUS		Title : +Vcore	
ASUSTeK COMPUTER INC. NB1		Engineer: Morris/Eric	
Size	Project Name	Rev	
Custom	UX50	1.0	
Date: Tuesday, March 31, 2009		Sheet 80 of 97	





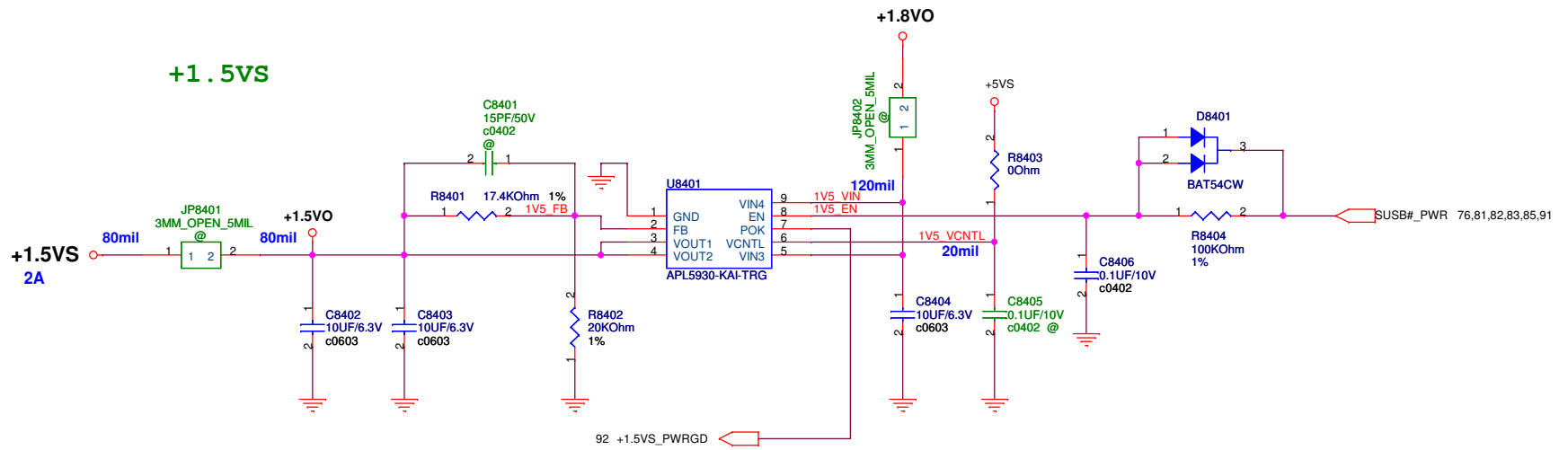
VOL_SEL:High VOLTAGE=1.080V
 VOL_SEL:Low VOLTAGE=1.050V



<Variant Name>

ASUS Title : POWER_I/O_DDR & VTT
 ASUSTek COMPUTER INC. NB Engineer: Morris/Eric

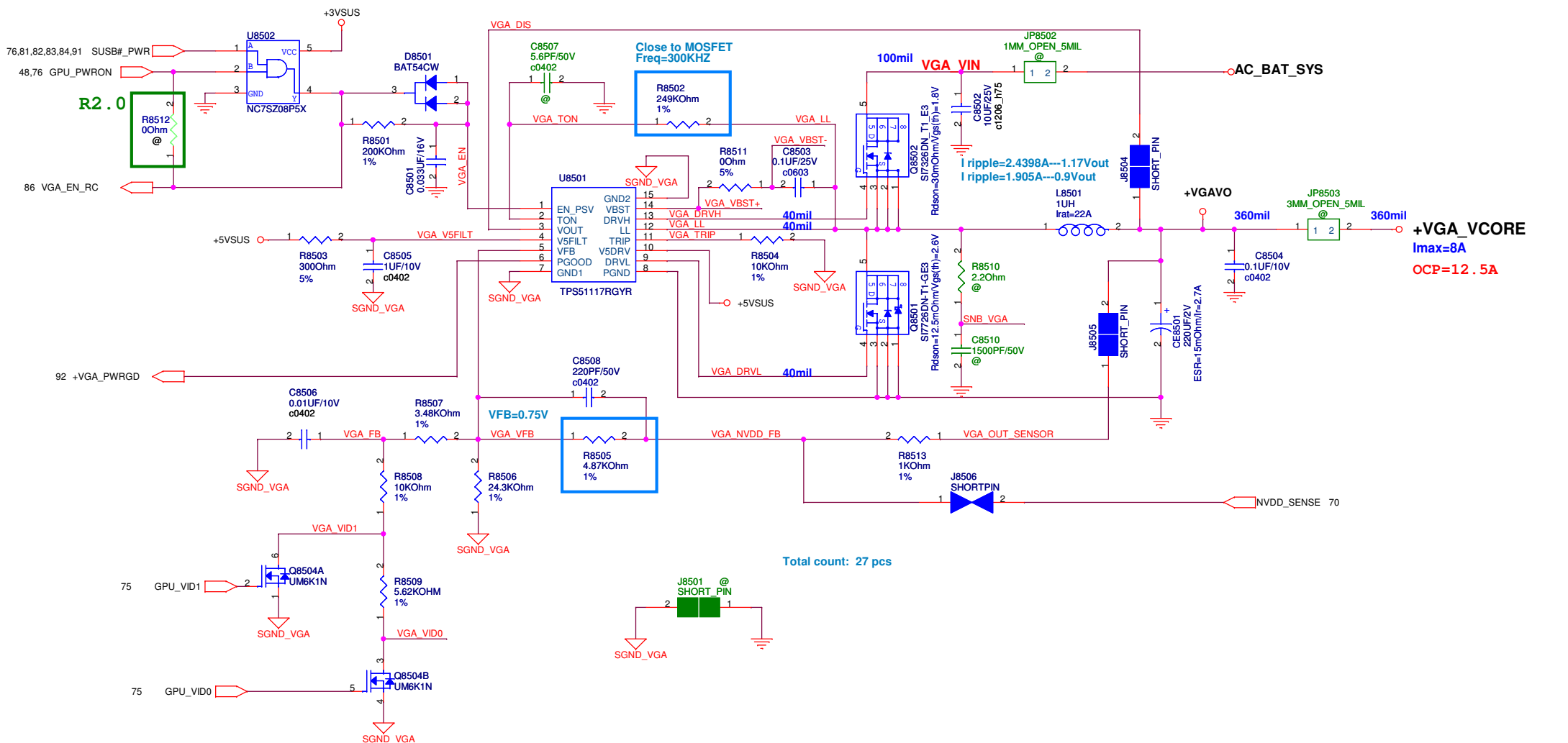
Size Custom	Project Name UX50	Rev 1.0
Date: Tuesday, March 31, 2009		Sheet 83 of 97



Total count: 12 pcs

LDO Second source APL5913-KAC-TRL

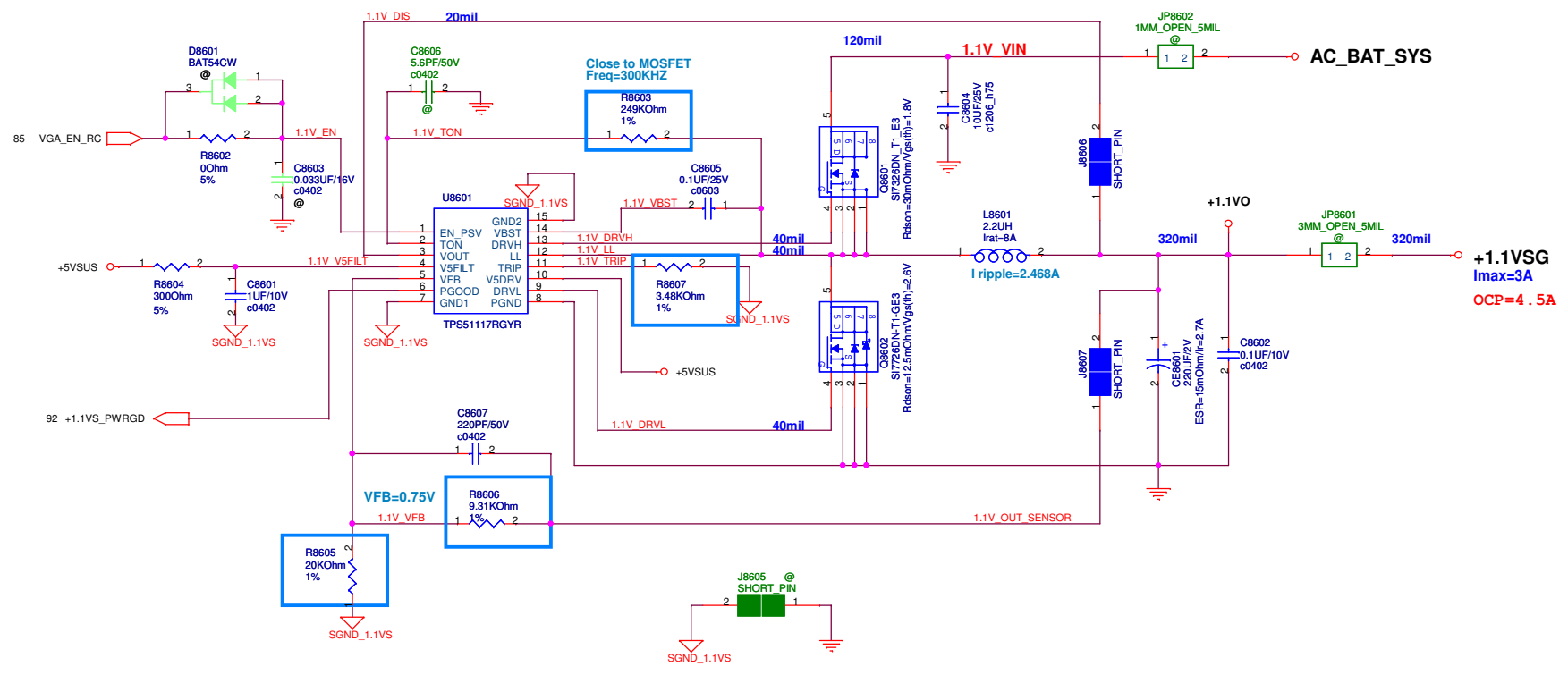
<Variant Name>		
ASUS		Title : POWER_IO_ +1.5VS
ASUSTeK COMPUTER INC. NB		Engineer: Morris/Eric
Size B	Project Name UX50	Rev 1.0
Date: Tuesday, March 31, 2009		Sheet 84 of 97



GPU_VID0	GPU_VID1	+VGA_VCORE
H	H	1.17V
H	L	1.09V
L	L	0.9V
L	H	1.17V

<Variant Name>

		Title :POWER_I/O_VGA
ASUSTeK COMPUTER INC. NB		Engineer: <i>Morris/Eric</i>
Size B	Project Name UX50	Rev 1.0
Date: <i>Tuesday, March 31, 2009</i>		Sheet <i>85</i> of <i>97</i>



<Variant Name>

		Title : POWER_IQ_1.1VS	
ASUSTeK COMPUTER INC. NB		Engineer: Morris/Eric	
Size	Project Name		Rev
Custom	UX50		1.0
Date: Tuesday, March 31, 2009	Sheet	86	of 97

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Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date:	Tuesday, March 31, 2009	Sheet 87 of 97

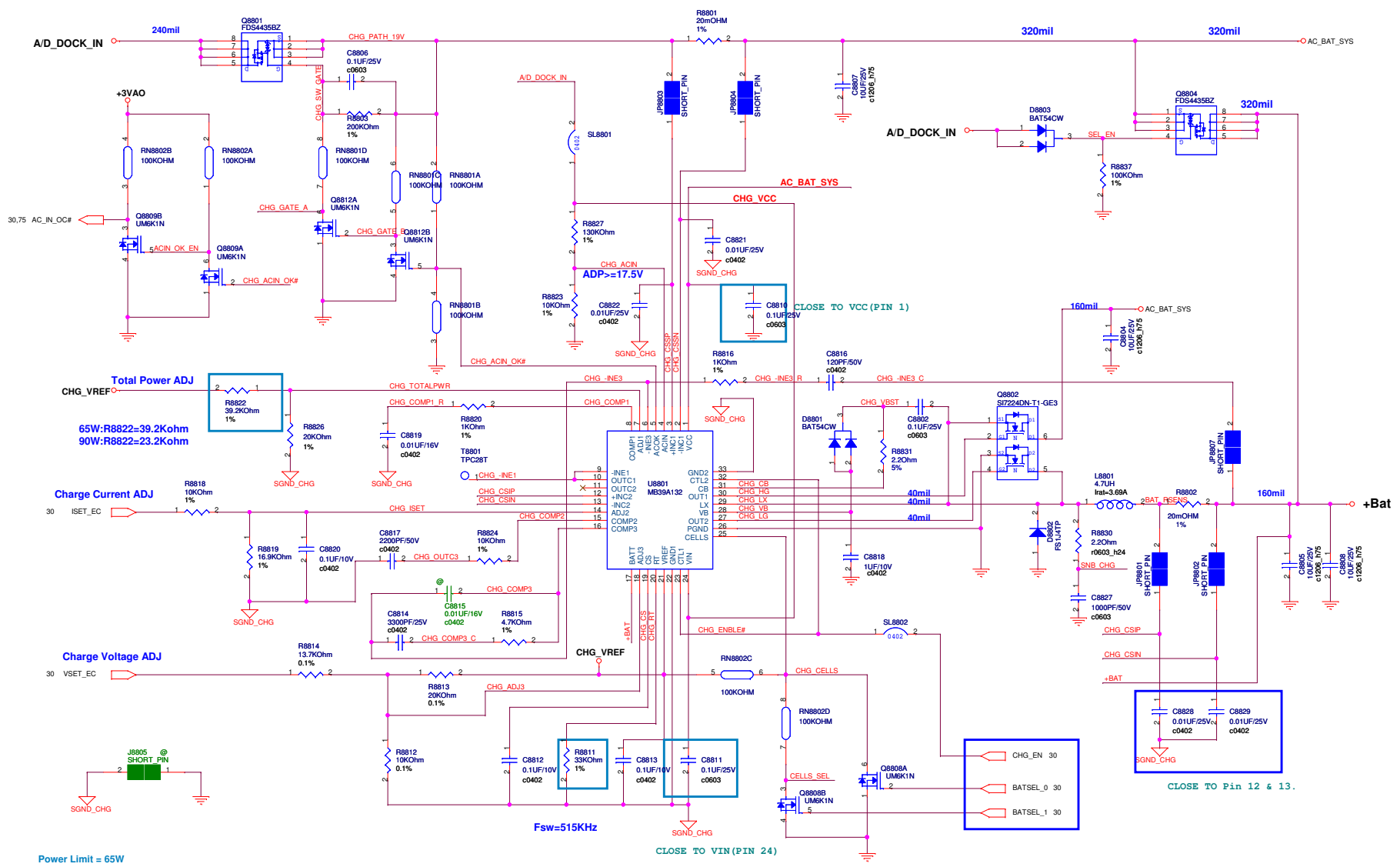
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Total Power ADJ
 CHG_VREF
 65W:R8822=39.2Kohm
 90W:R8822=23.2Kohm

Charge Current ADJ
 ISET_EC

Charge Voltage ADJ
 VSET_EC

Power Limit = 65W

TOTAL COUNT:56 PCS

Battery Cells

BATSEL_1	BATSEL_0	CELLS
H	H	2 CELLS
L	H	2 CELLS
H	L	3 CELLS
L	L	4 CELLS

Charger IC and EC Code correlation sheet :
 Charger MAX8725 => EC CODE : 200
 Charger MAX17015 => EC CODE : 201
 Charger MB39A132 => EC CODE : 202

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Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date:	Tuesday, March 31, 2009	Sheet 89 of 97

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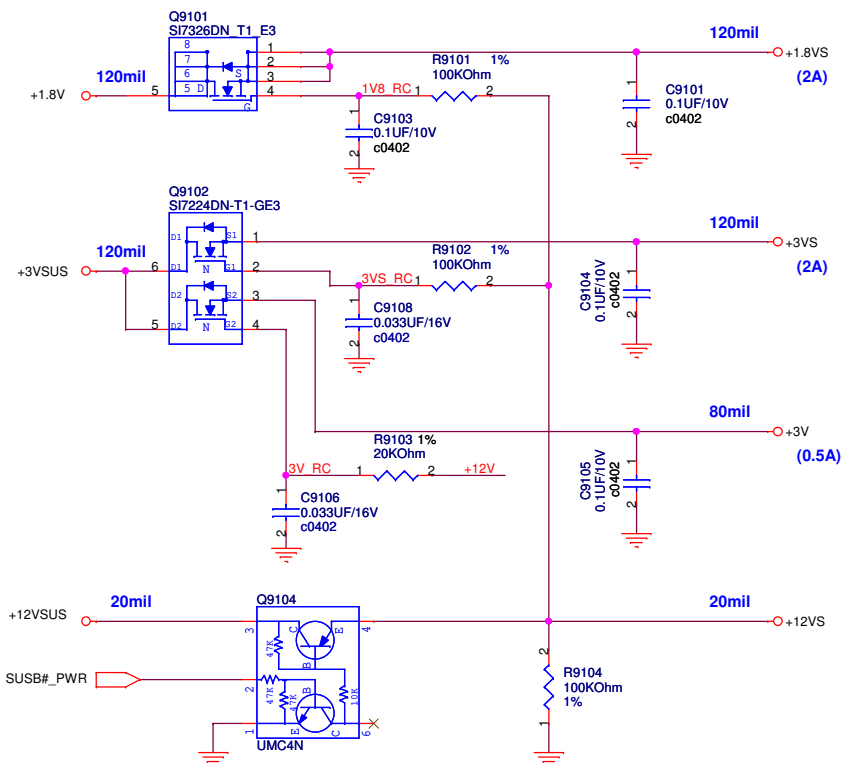
1

BATTERY IN DETECT

<Variant Name>

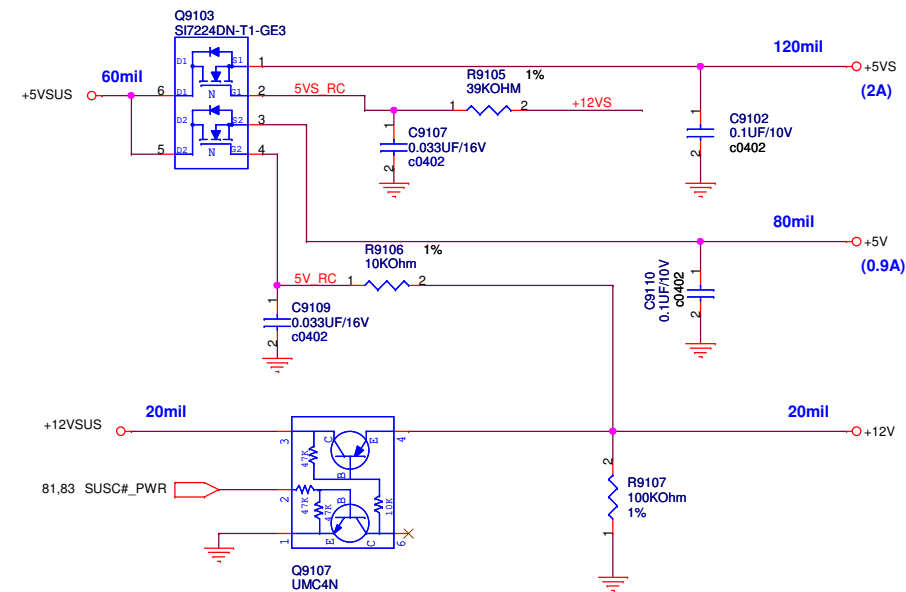
		Title : POWER_DETECT	
ASUSTeK COMPUTER INC. NB		Engineer: Morris/Eric	
Size	Project Name	Rev	
Custom	UX50	1.0	
Date: Tuesday, March 31, 2009		Sheet	90 of 97

SUSB#_PWR POWER



Total count: 20 pcs

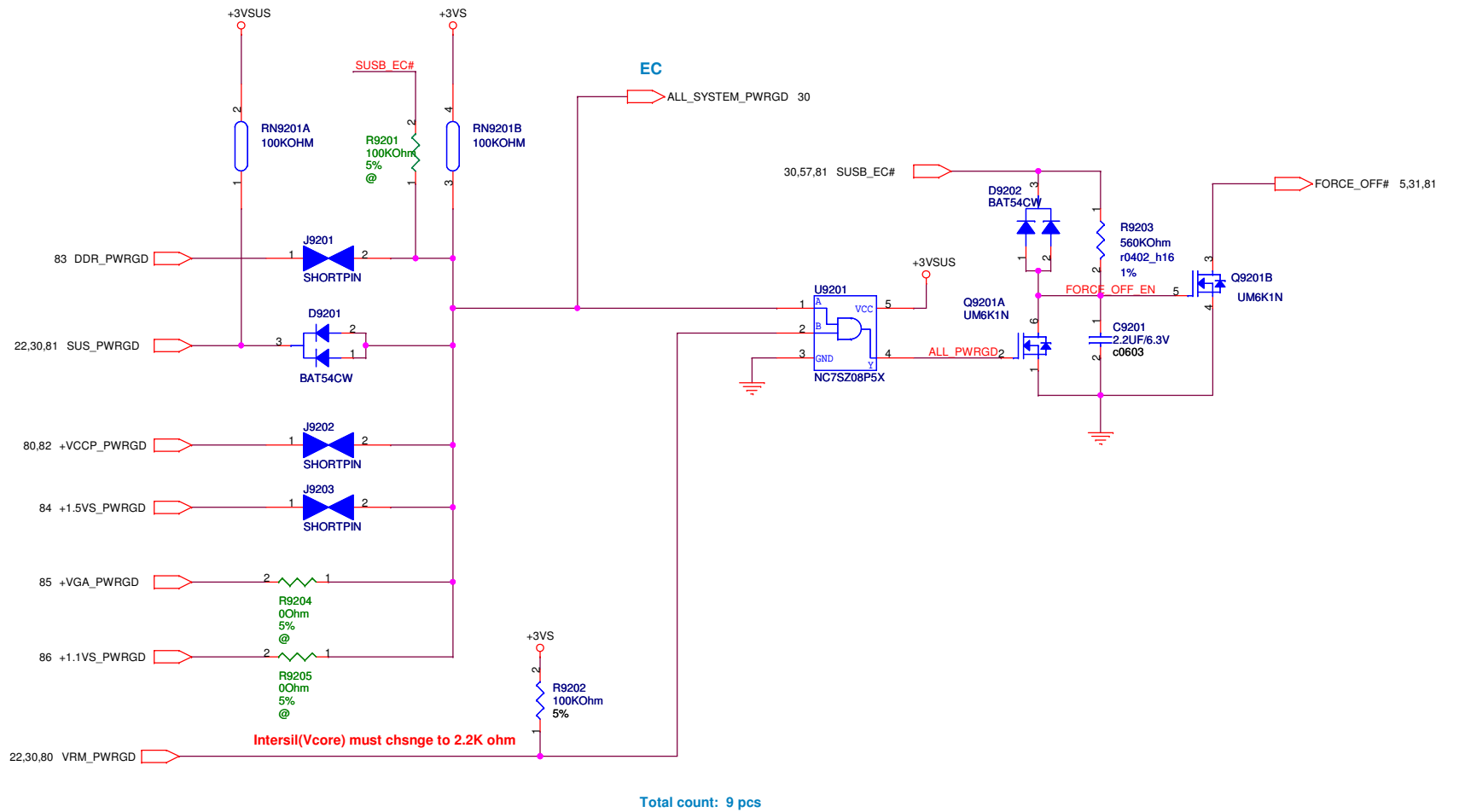
SUSC#_PWR POWER



<Variant Name>

ASUS		Title :POWER_LOAD SWITCH	
ASUSTeK COMPUTER INC. NB		Engineer: Morris/Eric	
Size B	Project Name UX50	Date Tuesday, March 31, 2009	Rev 1.0
		Sheet 91	of 97

POWER GOOD DETECTOR




<Variant Name>

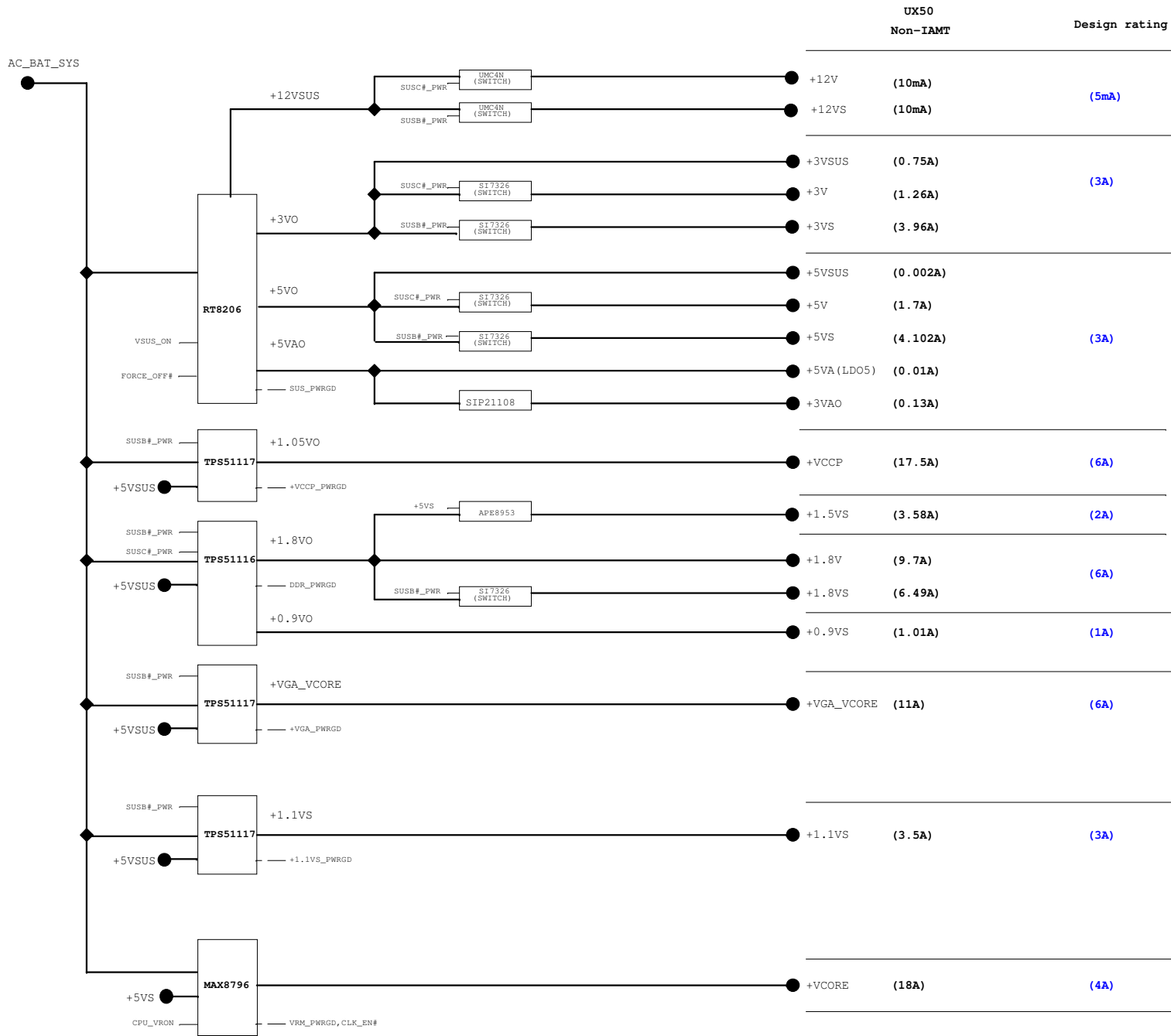
ASUS		Title :POWER_PROTECT	
ASUSTeK COMPUTER INC. NB		Engineer: Morris/Eric	
Size	Project Name	Rev	
B	UX50	1.0	
Date: Tuesday, March 31, 2009		Sheet 92 of 97	

AC_BAT_SYS	○	→	AC_BAT_SYS	46,80,81,82,83,85,86,88
+BAT	○	→	+BAT	68,88
+3VAO	○	→	+3VAO	81,88
+5VA	○	→	+5VA	81
+3VA	○	→	+3VA	20,30,31,56,68,81,88
+5VAO	○	→	+5VAO	81
+5VO	○	→	+5VO	81
+5VSUS	○	→	+5VSUS	23,68,80,81,82,83,85,86,88,91
+5V	○	→	+5V	31,57,67,68,91
+5VS	○	→	+5VS	23,45,47,48,51,57,68,80,84,91
+3VO	○	→	+3VO	76,81
+3VSUS	○	→	+3VSUS	20,21,22,23,30,33,57,68,76,81,85,91,92
+3V	○	→	+3V	44,46,48,57,67,68,70,91
+3VS	○	→	+3VS	7,8,11,12,15,17,21,22,23,24,29,30,31,45,46,47,48,50,51,57,68,80,91,92
+12VSUS	○	→	+12VSUS	76,81,91
+12V	○	→	+12V	68,91
+12VS	○	→	+12VS	22,46,48,51,67,91
+1.8VO	○	→	+1.8VO	83,84
+1.8V	○	→	+1.8V	7,8,11,14,57,76,83,91
+1.8VS	○	→	+1.8VS	15,91
+0.9VS	○	→	+0.9VS	9,57,83
+0.9VO	○	→	+0.9VO	83
+1.05VO	○	→	+1.05VO	82
+VCCP	○	→	+VCCP	3,4,5,10,11,12,14,15,20,23,29,57,76,82
+1.5VO	○	→	+1.5VO	84
+1.5VS	○	→	+1.5VS	4,15,20,23,57,84
+VCORE	○	→	+VCORE	4,5,80
+VCCP	○	→	+VCCP	3,4,5,10,11,12,14,15,20,23,29,57,76,82
+1.05VO	○	→	+1.05VO	82
+1.1VSG	○	→	+1.1VSG	70,71,73,74,76,86
+VGA_VCORE	○	→	+VGA_VCORE	70,85
A/D_DOCK_IN	○	→	A/D_DOCK_IN	60,88

Total sum count: 236 pcs

<Variant Name>

		Title : POWER_SIGNAL	
ASUS COMPUTER INC. NB		Engineer: <i>Morris/Eric</i>	
Size	Project Name	Rev	
Custom	UX50	1.0	
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VR_VID0-VR_VID6, H_DPRSTP#,
MCH_OK, PM_DPRSLEPVR, PM_PSI#,
VCCSENSE, VSSSENSE, STP_CPO#,
PWR_MON

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		Title :POWER_CHARGER
ASUSTeK COMPUTER INC. NB3		Engineer: Eric_Ho
Size A	Project Name UX50	Rev 1.0
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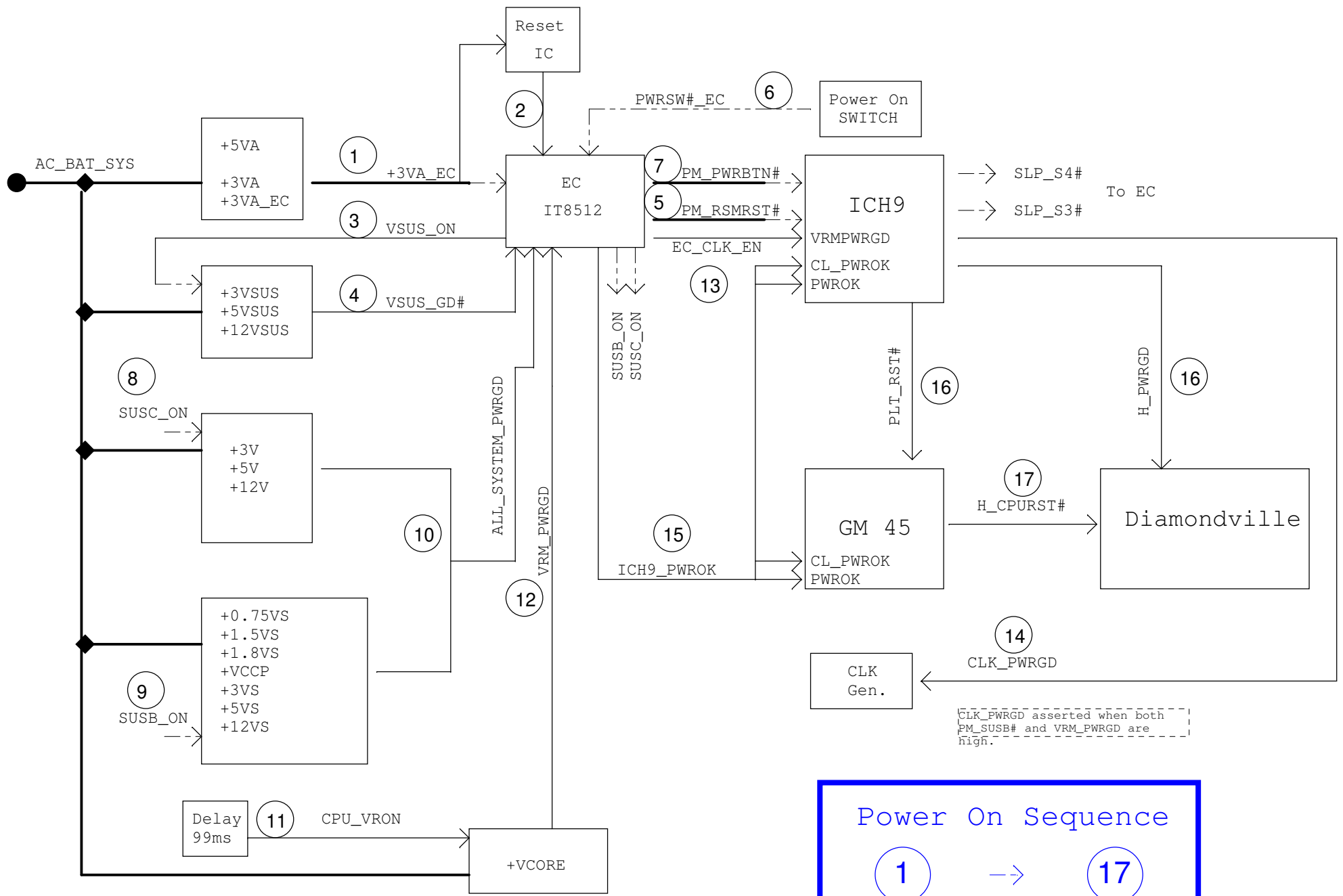
4

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Rev	Date	Description
1.00		First Release!
1.10	02/08/2009	1. Change net ALS_AD to J6801. (Page 68) 2. Change RTC circuit from small board to M/B. (Page 20) 3. Add net CLK_PCIE_VGA and CLK_PCIE_VGA#.(Page 29) 4. Add pull-up for SMBus.(Page 22) 5. Add ITP connector. (Page 03,29) 6. Add MOS for dGPU power. (Page 76)
	02/10/2009	7. Change LAN PCIE to port 6. (Page 21) 8. Add AL_LED# to control ambient light LED. (Page 30,68) 9. Change C7036 to 4.7UF. (Page 70)
	02/11/2009	10. Swapping DDR2 nets (Page 09,29,74) 11. Add USB port for WiMax (Page 68,21) 12. Remove test point for layout. (Page 30)
	02/16/2009	13. Change 8pF cap for 32.768KHz crystal. (Page 20,30)
	02/17/2009	14. Swap J6801 BAT pins (Page 68)
2.00	03/04/2009	1. Remove D4503 for HDA issue. (Page 45)
	03/09/2009	2. Add HDMI hot plug detect in iGPU mode. (Page 48)
	03/09/2009	3. Add C6805 for EMI. (Page 68)
	03/12/2009	4. Change HDMI hot plug detect pin to EC GPI6. (Page 30,48)
	03/12/2009	5. Add CE0502 for CPU SU9600 hang issue. (Page 5)
	03/12/2009	6. Pull up backligh enable pin tto +3VS_LCD from +3VS. (Page 46)
	03/16/2009	7. Swap RN2917. (Page 29)
	03/18/2009	8. Change R7301 to 120ohm. (Page 73)



Power On Sequence

1 → 17