



# U6V Schematic Index

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91	POWER_LOAD SWITCH
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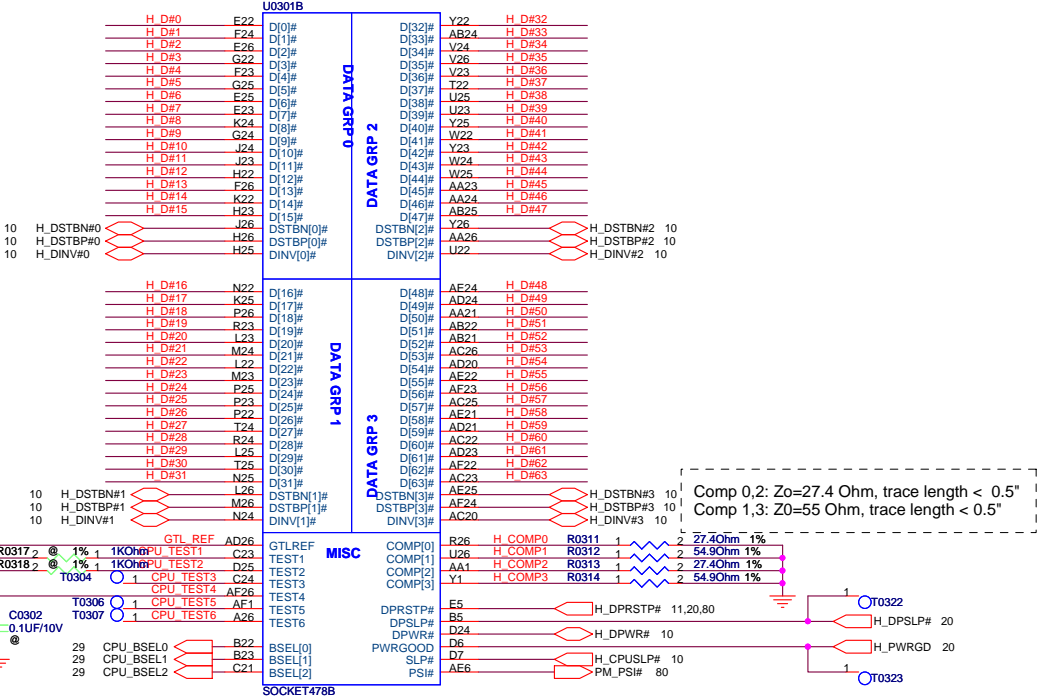
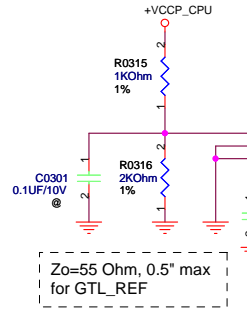
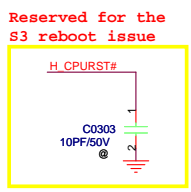
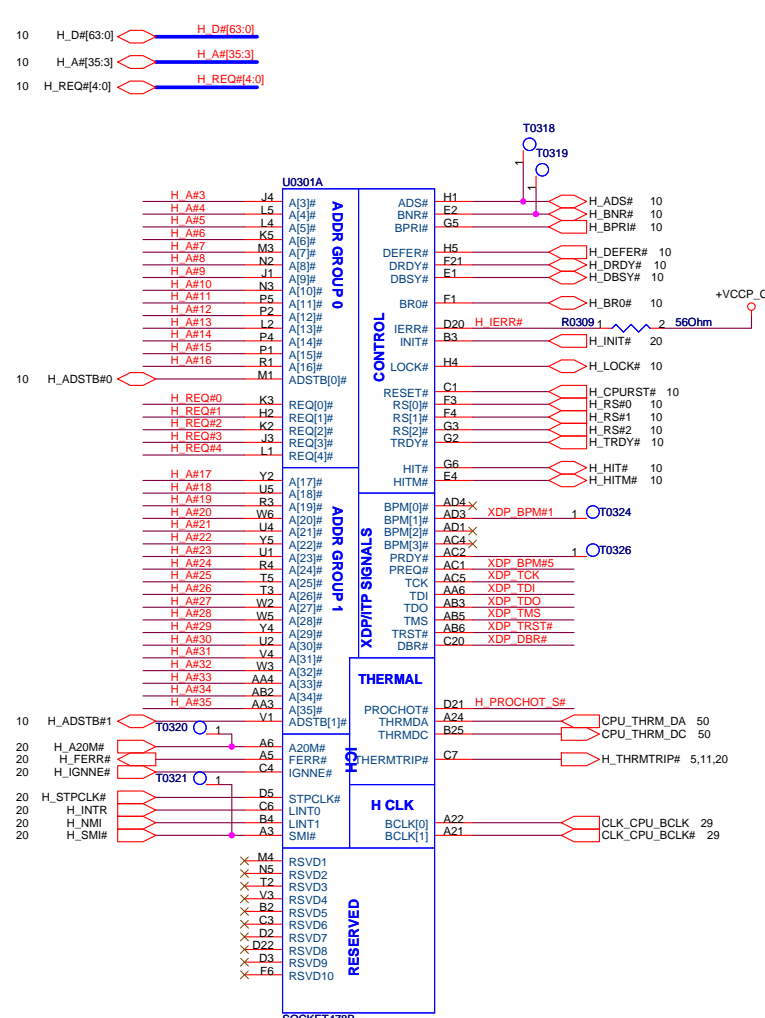
INT PU\*: PU or PD in special time

GPIO33 Internal Pull High, Go Low Flash -- I/O Descriptor Security will be overridden

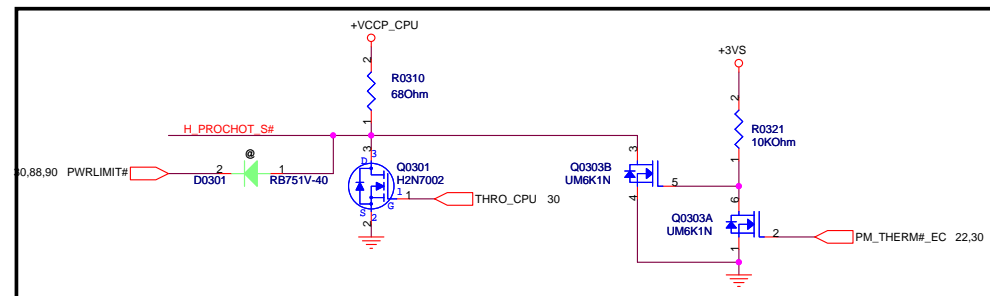
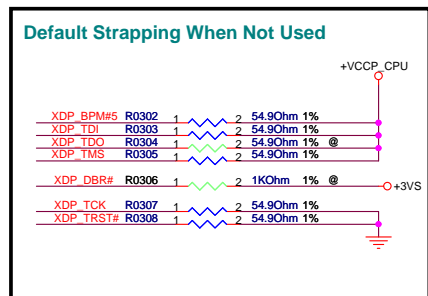
ICH9-M GPIO	Use As	Signal Name	Power
GPIO 00	GPI	PMSYNC#(programmed as GPO)	+3VS
GPIO 01	GPI	DOCKING_DET# EXT PU	+3VS
GPIO [2:5]	GPI	PCI_INT[E:H]#EXT PU	+5VS
GPIO 06	GPI	- EXT PU	+3VS
GPIO 07	GPI	- EXT PU	+3VS
GPIO 08	GPI	EXT_SMI# EXT PU	+3VSUS
GPIO 09	Native	WOL_EN	+3VSUS
GPIO 10	GPI	SUS_PWR_ACK EXT PU	+3VSUS
GPIO 11	Native	EXT_SCI#(Programmed as GPI)	+3VSUS
GPIO 12	GPO	-	+3VSUS
GPIO 13	GPI	CB_SD#(Programmed as GPO)	+3VSUS
GPIO 14	GPI	AC_PRESENT EXT PD	+3VSUS
GPIO 15	Native	STP_PCI#	+3VSUS
GPIO 16	Native	PM_DPRS_LPVR INT PD*	+3VS
GPIO 17	GPI	WLAN_LED(Programmed as GPO)	+3VS
GPIO 18	GPO	-	+3VS
GPIO 19	GPI	- EXT PU	+3VS
GPIO 20	GPO	- INT PD*	+3VS
GPIO 21	GPI	- EXT PU	+3VS
GPIO 22	GPI	BT_DET# EXT PU	+3VS
GPIO 23	Native	ICH_LDRQ1# INT PU	+3VS
GPIO 24	GPO	WLAN_ON	+3VSUS
GPIO 25	Native	STP_CPU#	+3VSUS
GPIO 26	Native	PM_S4_STATE#	+3VSUS
GPIO 27	GPO	BT_ON	+3VSUS
GPIO 28	GPO	BT_LED	+3VSUS
GPIO 29	Native	USB_OC#5	+3VSUS
GPIO 30	Native	USB_OC#6	+3VSUS
GPIO 31	Native	USB_OC#7	+3VSUS
GPIO 32	GPO	PM_CLKRUN#	+3VS
GPIO 33	GPO	- INT PU*	+3VS
GPIO 34	GPO	-	+3VS
GPIO 35	GPO	-	+3VS
GPIO 36	GPI	- EXT PU	+3VS
GPIO 37	GPI	PCB_ID0	+3VS
GPIO 38	GPI	PCB_ID1	+3VS
GPIO 39	GPI	PCB_ID2	+3VS
GPIO 40	Native	USB_OC01#	+3VSUS
GPIO 41	Native	USB_OC2#	+3VSUS
GPIO 42	Native	USB_OC3#	+3VSUS
GPIO 43	Native	USB_OC4#	+3VSUS
GPIO 44	Native	CLK_DEC#	+3VSUS
GPIO 45	Native	CLK_ACC	+3VSUS
GPIO 46	Native	NEWCARD_OC#	+3VSUS
GPIO 47	Native	UNDOCKING#	+3VSUS
GPIO 48	GPI	EMAIL_LED# EXT PU	+3VS
GPIO 49	GPO	GPU_RST# INT PU*	+3VS
GPIO 50	Native	PCI_REQ#1	+5VS
GPIO 51	Native	PCI_GNT#1 INT PU*	+3VS
GPIO 52	Native	PCI_REQ#2	+5VS
GPIO 53	Native	PCI_GNT#2 INT PU*	+3VS
GPIO 54	Native	PCI_REQ#3	+5VS
GPIO 55	Native	PCI_GNT#3 INT PU*	+3VS
GPIO 56	GPI	- EXT PU	+3VSUS
GPIO 57	GPI	- EXT PU	+3VSUS
GPIO 58	GPI	SPI_CS#1 INT PU*	+3VSUS
GPIO 59	Native	USB_OC0#	+3VSUS
GPIO 60	Native	LINKALERT#	+3VSUS

EC GPIO	Use As	Signal Name	Power
GPA0	GPO	PWR_LED_UP#	
GPA1	GPO	CHG_LED_UP#	
GPA2	GPO	BATSEL_3S#	
GPA3	-	-	
GPA4	GPO	LCD_BL_PWM	
GPA5	GPO	FAN0_PWM	
GPA6	GPO	BAT1_CNT1#	
GPA7	GPO	BAT2_CNT1#	
GPB0	GPO	CHG_EN#	
GPB1	GPO	PRECHG	
GPB2	GPI	DISTP#	
GPB3	ALT	SMB0_CLK	
GPB4	ALT	SMB0_DAT	
GPB5	OD	A20GATE	
GPB6	OD	RCIN#	
GPB7	GPO	PM_RSMRST#	
GPC0	GPI	MARATHON#	
GPC1	ALT	SMB1_CLK	
GPC2	ALT	SMB1_DAT	
GPC3	GPO	PM_PWRBTN#	
GPC4	ALT	AC_IN_OC#	
GPC5	GPO	OP_SD#	
GPC6	ALT	BAT1_IN_OC#	
GPC7	GPO	3G_ON#	
GPC0	GPI	PWRLIMIT#	
GPD1	ALT	PM_S4_STATE#	
GPD2	ALT	BUF_PLT_RST#	
GPD3	OD	EXT_SCI#	
GPD4	OD	EXT_SMI#	
GPD5	GPO	LCD_BACKOFF#	
GPD6	ALT	FAN0_TACH	
GPD7	GPI	COLOREN#	
GPE0	GPO	VSUS_ON	
GPE1	GPO	SUSC_EC#	
GPE2	GPO	SUSB_EC1#	
GPE3	GPO	CPU_VRON	
GPE4	ALT	PWR_SW#	
GPE5	ALT	BAT2_IN_OC#	
GPE6	GPI	LID_SW#	
GPE7	GPO	PM_THERM#	
GPF0	GPI	BLUETOOTH#	
GPF1	GPI	WIRELESS#	
GPF2	ALT	PS2_CLK_5S_PD	
GPF3	ALT	PS2_DATA_5S_PD	
GPF4	ALT	TP_CLK	
GPF5	ALT	TP_DAT	
GPF6	GPO	THRO_CPU	
GPF7	GPO	PS_SHDN#	
GGP0	GPI	INSTANT_ON#	
GPG1	ALT	PM_SUSB#	
GPG2	GPO	BAT1_CNT2#	
-	-	-	
-	-	-	

EC GPIO	Use As	Signal Name	Power
-	-	-	
GPG6	GPO	BAT2_CNT2#	
-	-	-	
GPH0	OD	PM_CLKRUN#	
GPH1	ALT	-	
GPH2	ALT	-	
GPH3	GPO	BAT_LEARN	
GPH4	GPO	-	
GPH5	GPO	NUM_LED	
GPH6	GPO	CAP_LED	
-	-	-	
GP10	GPI	-	
GP11	GPI	SUS_PWRGD	
GP12	GPI	ALL_SYSTEM_PWRGD	
GP13	GPI	VRM_PWRGD	
GP14	GPI	PWR_MON	
GP15	GPI	PD_DET#	
GP16	GPI	KB_ID0	
GP17	GPI	KB_ID1	
GPJ0	GPO	EC_CLK_EN	
GPJ1	GPO	PM_PWROK	
GPJ2	GPI	UNDOCK#_PD	
GPJ3	-	-	
GPJ4	GPO	BL_DA	
GPJ5	GPO	FAN_DA	
GPK0	GPI	PM_SLP_M#	
GPK1	GPI	SUSPWR_ACK	
GPK2	GPI	PM_SUSC#	
GPK3	GPI	+3VM_PG	
GPK4	GPI	+1.05VM_+3VMCLK_PG	
GPK5	GPI	LAN_WOL_EN	
GPL0	GPI	AC_APR_UC#	
GPL1	GPI	-	
GPL2	GPO	-	
GPL3	GPO	LAN_RST#	
GPL4	GPO	CL_PWROK	
GPL5	GPO	EC_WLAN_PWR	
GPL6	GPO	SLP_M_ON	
GPL7	GPO	S4_STATE_ON	
GPK6	GPO	AC_PRESENT	
GPK7	GPI	PS_CPPE#	
-	-	-	
-	-	-	

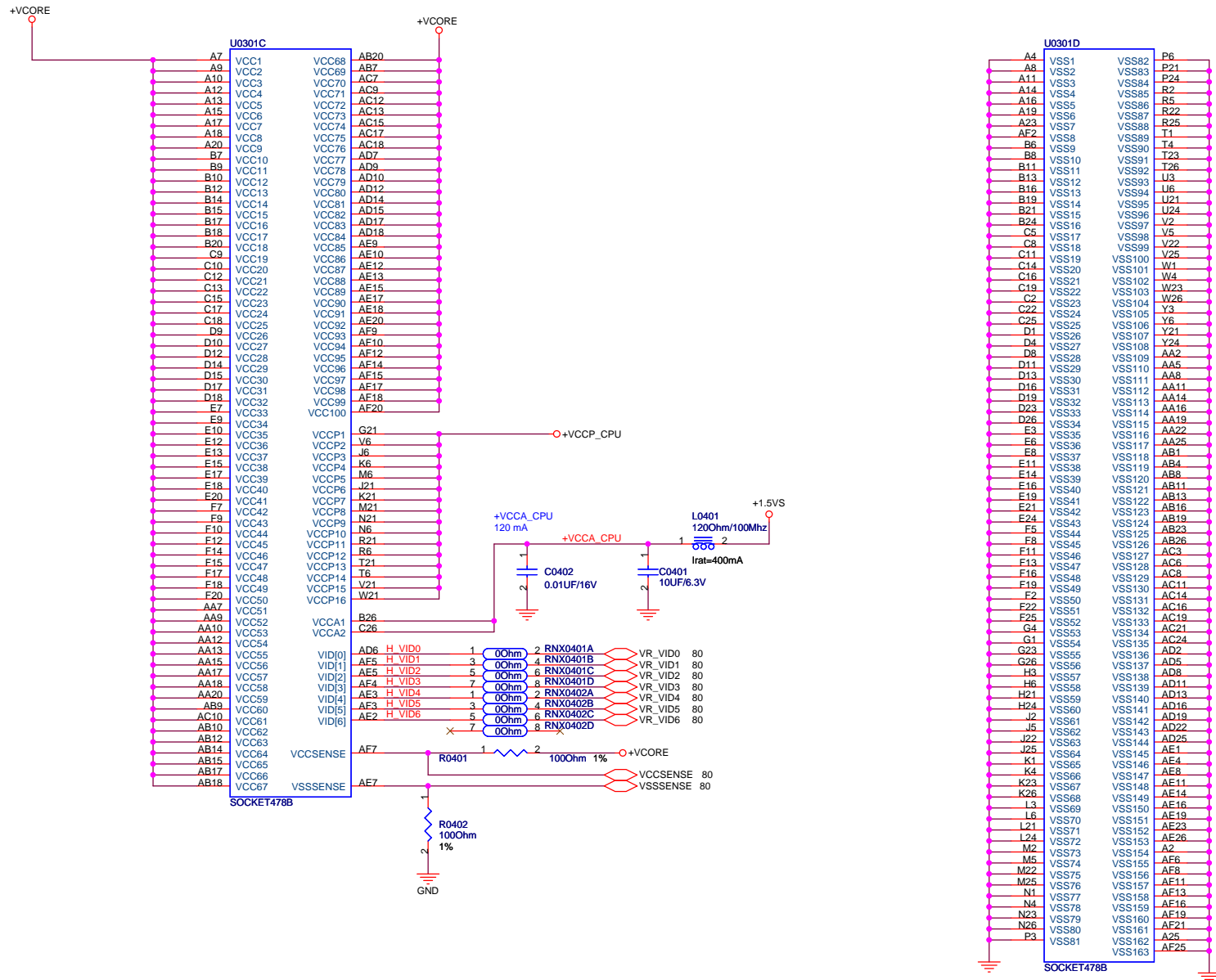


BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	L	H	H
200	800	L	H	L
266	1067	L	L	L

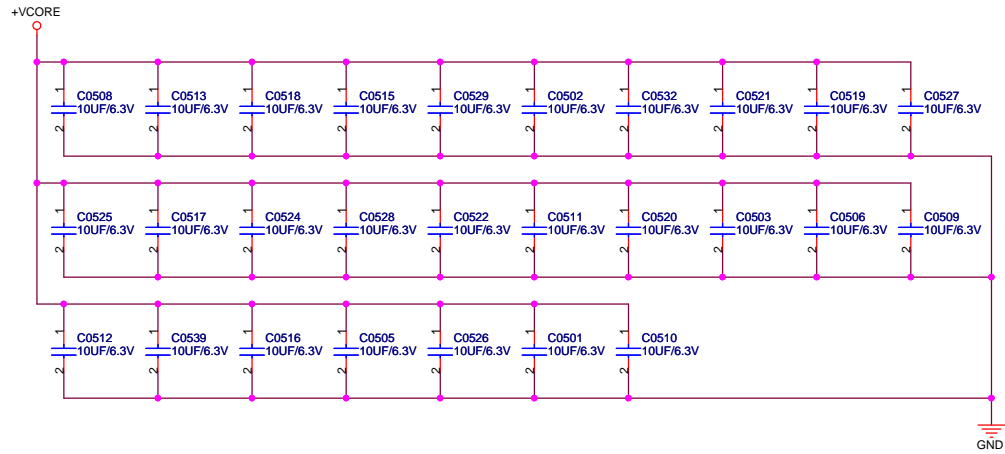


ASUS  
**Title : CLOCK GEN-IC59LPR363**  
 ASUSTeK COMPUTER INC. NB1 Engineer: <OrgAddr1>  
 Size Project Name  
 Custom U6V  
 Date: Tuesday, April 15, 2008 Sheet 3 of 102

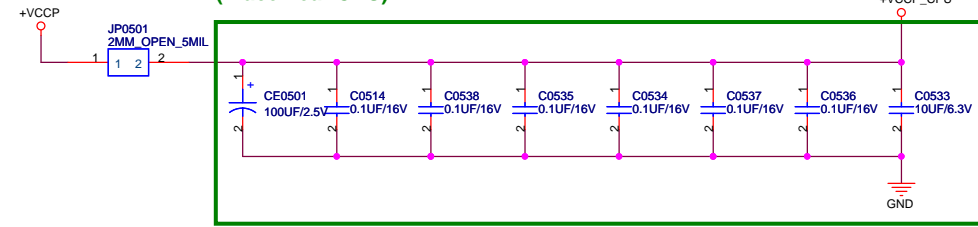
Place R0304 & R0306 for XDP function



### 38A for Penryn



### +VCCP Decoupling Capacitor (Place near CPU)



#### Decoupling guide from Intel

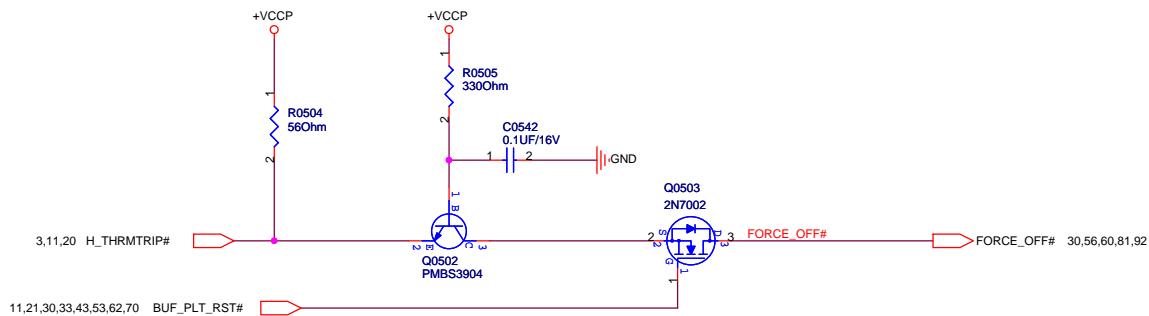
<b>CORE</b>	22uF/10V r 10uF	* 32pcs
	330uF/2V	* 6pcs
<b>VCCP</b>	0.1uF	* 6pcs
	150uF	* 1pcs ?
	10uF	* 1pcs ?

#### +VCCORE Mid-Frequency Capacitor

Intel: 22UF \*32  
 F3S: 10UF \*16  
 A7S: 10UF \*10 ....11/17  
 V1V: ?

#### +VCCP Decoupling Capacitor

Intel: 270UF \*1, 0.1UF \*6  
 F3S: 100UF \*1, 0.1UF \*4  
 V1V: ?



Thermal Trip signal (From CPU to ICH-9M and sequence)

5

4

3

2

1

D

D

C

C

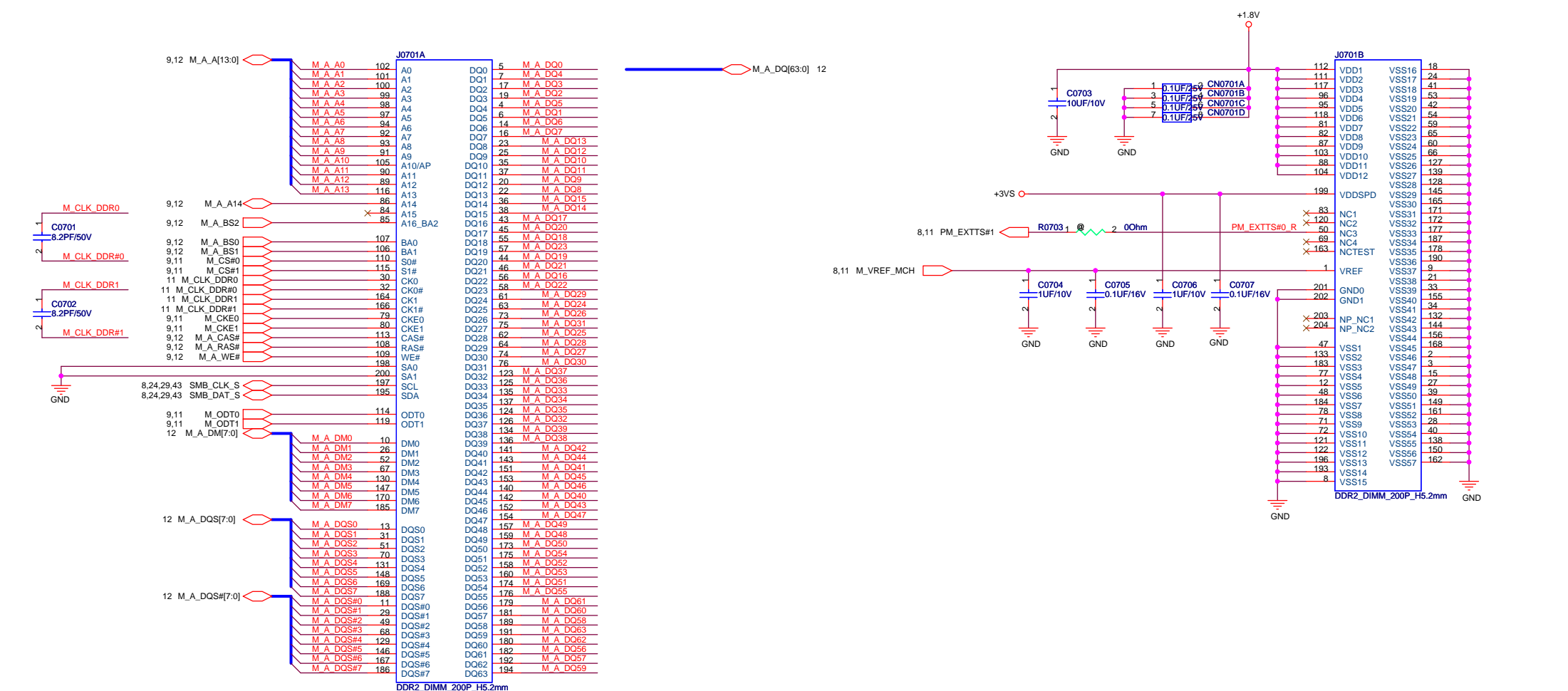
B

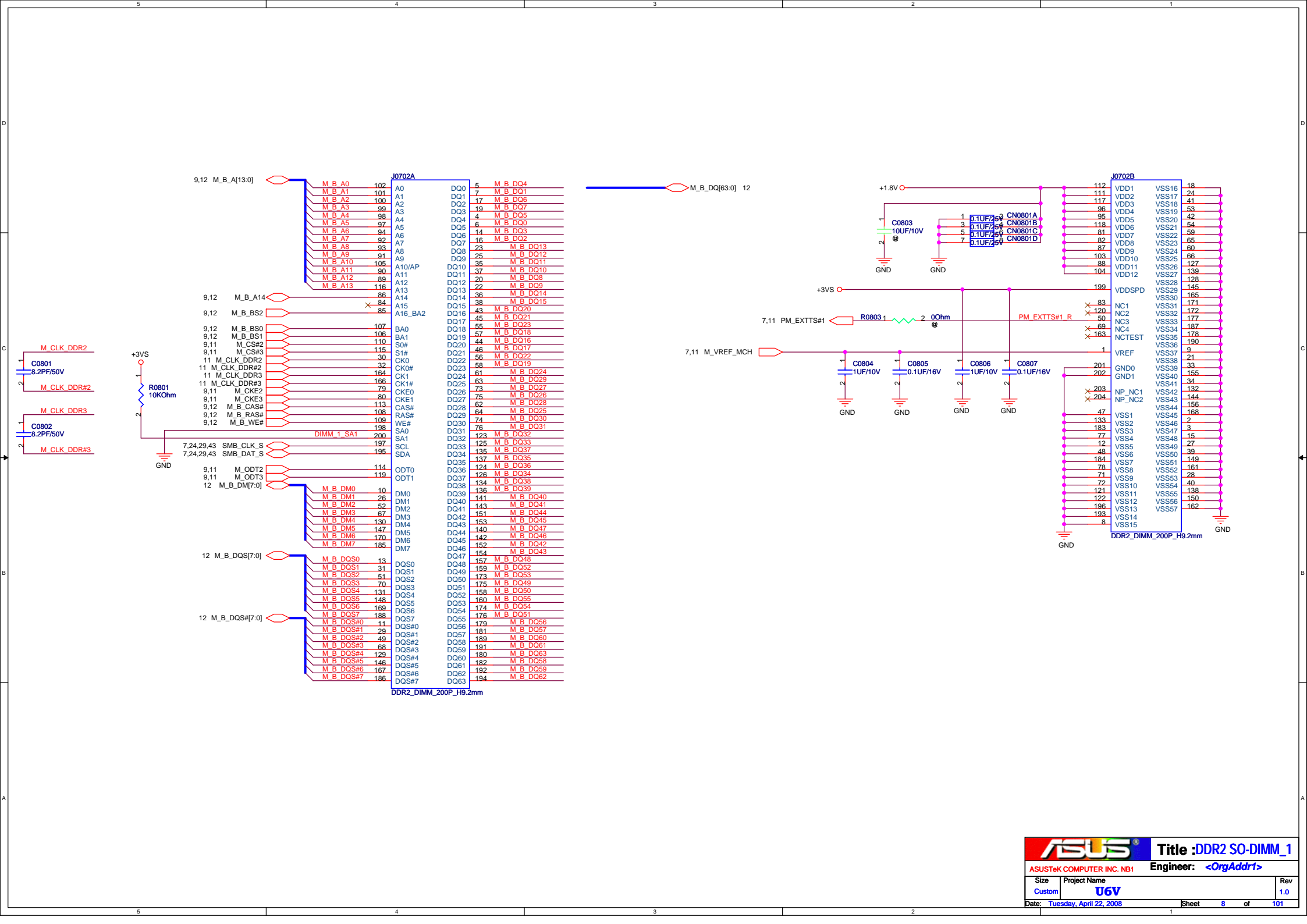
B

A

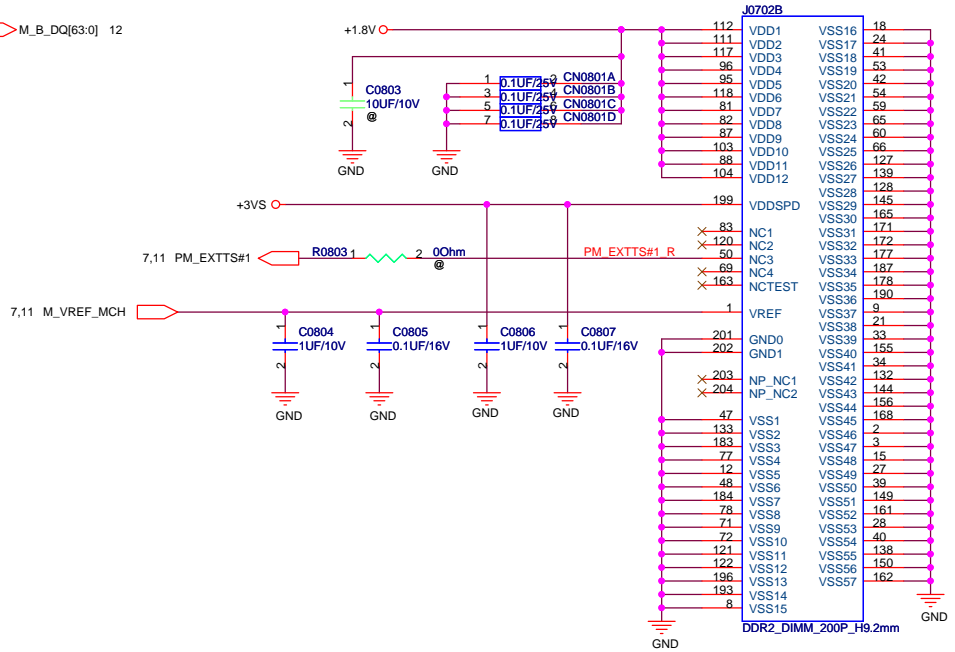
A

		<b>Title : CPU CAPS</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	<b>U6V</b>		2.0
Date: Tuesday, April 15, 2008		Sheet	6 of 102

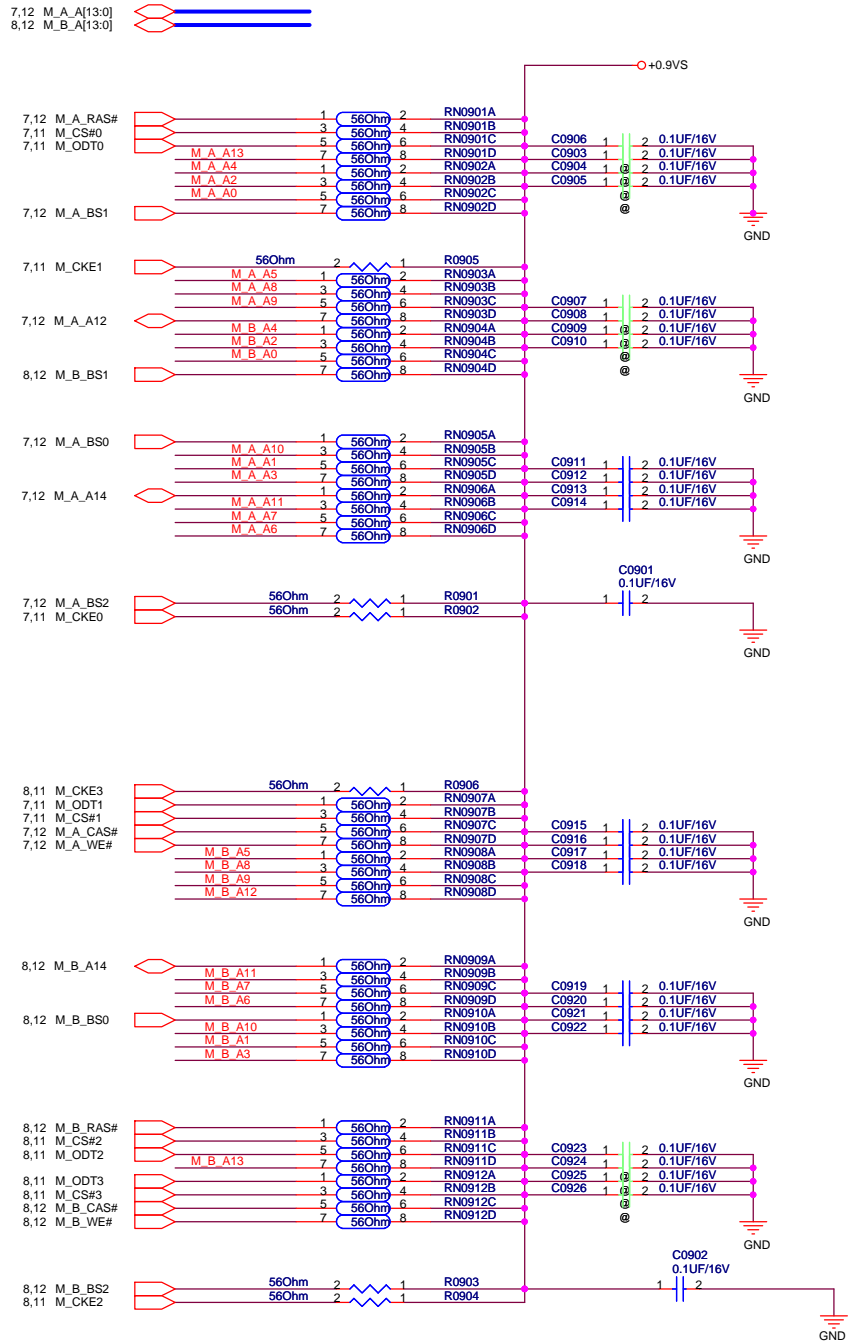


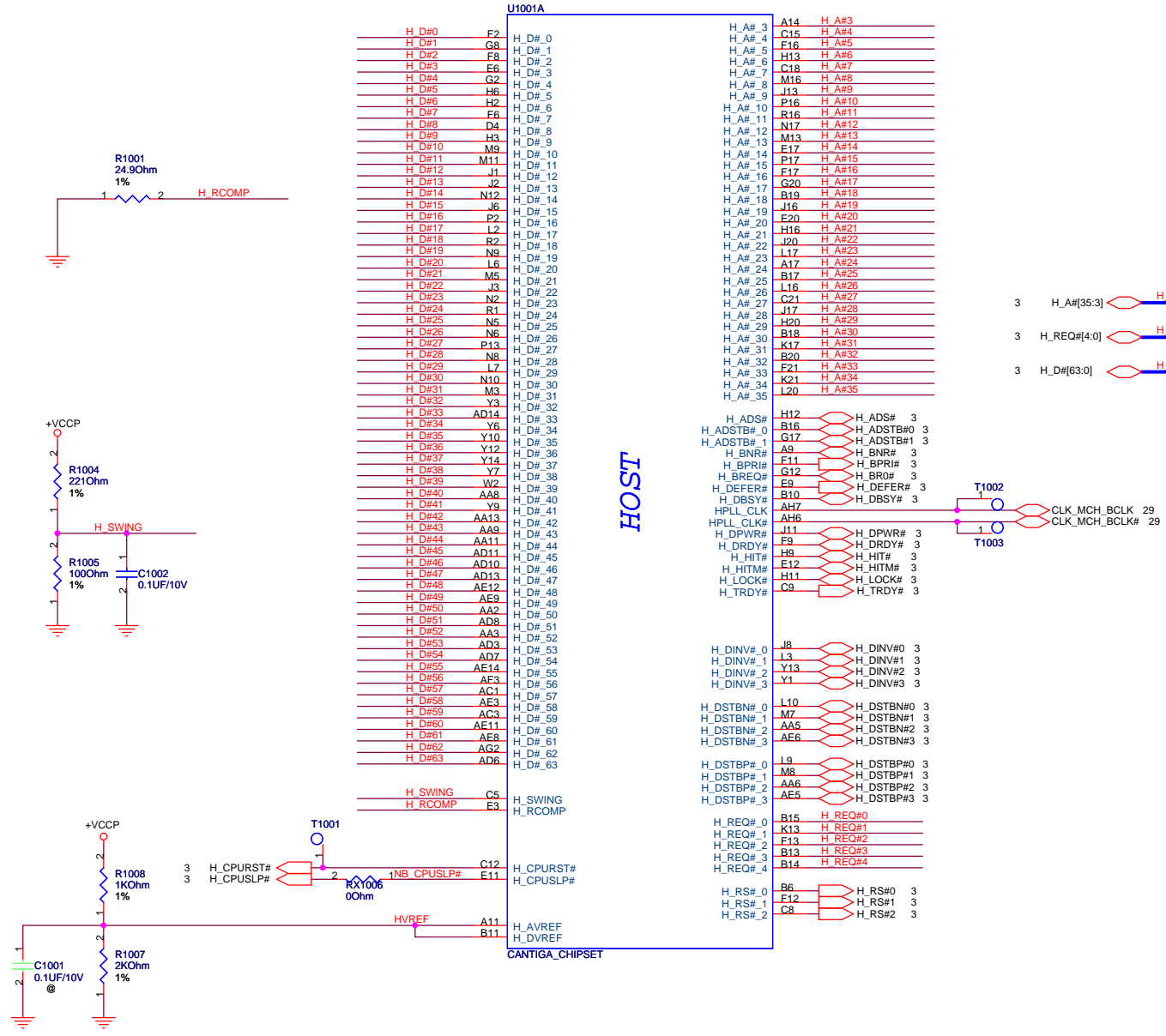


9,12 M_B_A[13:0]	M_B_A0	102	A0	DQ0	5	M_B_DQ4
	M_B_A1	101	A1	DQ1	7	M_B_DQ1
	M_B_A2	100	A2	DQ2	17	M_B_DQ6
	M_B_A3	99	A3	DQ3	19	M_B_DQ7
	M_B_A4	98	A4	DQ4	4	M_B_DQ5
	M_B_A5	97	A5	DQ5	6	M_B_DQ0
	M_B_A6	94	A6	DQ6	14	M_B_DQ3
	M_B_A7	92	A6	DQ6	16	M_B_DQ2
	M_B_A8	93	A7	DQ7	23	M_B_DQ13
	M_B_A9	91	A8	DQ8	25	M_B_DQ12
	M_B_A10	105	A9	DQ9	35	M_B_DQ11
	M_B_A11	90	A10/AP	DQ10	37	M_B_DQ10
	M_B_A12	89	A11	DQ11	20	M_B_DQ8
	M_B_A13	116	A12	DQ12	22	M_B_DQ9
		86	A13	DQ13	36	M_B_DQ14
9,12 M_B_A14		84	A14	DQ14	38	M_B_DQ15
9,12 M_B_BS2		85	A15	DQ15	43	M_B_DQ20
			A16_BA2	DQ16	45	M_B_DQ21
9,12 M_B_BS0		107	BA0	DQ17	55	M_B_DQ23
9,12 M_B_BS1		106	BA1	DQ18	57	M_B_DQ18
9,11 M_CS#2		115	SO#	DQ19	44	M_B_DQ16
9,11 M_CS#3		30	S1#	DQ20	46	M_B_DQ17
11 M_CLK_DDR2		32	CK0#	DQ21	56	M_B_DQ22
11 M_CLK_DDR3		164	CK1	DQ22	58	M_B_DQ19
11 M_CLK_DDR#3		166	CK1#	DQ23	61	M_B_DQ24
9,11 M_CKE2		80	CKE0	DQ24	63	M_B_DQ23
9,11 M_CKE3		113	CKE1	DQ25	73	M_B_DQ27
9,12 M_B_CAS#		108	CAS#	DQ26	75	M_B_DQ26
9,12 M_B_RAS#		109	RAS#	DQ27	62	M_B_DQ28
9,12 M_B_WE#		198	WE#	DQ28	64	M_B_DQ25
		197	SA0	DQ29	74	M_B_DQ30
		195	SA1	DQ30	76	M_B_DQ31
7,24,29,43 SMB_CLK_S		114	SA0	DQ31	123	M_B_DQ32
7,24,29,43 SMB_DAT_S		119	SA1	DQ32	125	M_B_DQ33
			SCL	DQ33	135	M_B_DQ37
			SDA	DQ34	137	M_B_DQ35
9,11 M_ODT2		114	ODT0	DQ35	124	M_B_DQ36
9,11 M_ODT3		119	ODT1	DQ36	126	M_B_DQ34
12 M_B_DM[7:0]	M_B_DM0	10	DM0	DQ37	134	M_B_DQ38
	M_B_DM1	26	DM1	DQ38	136	M_B_DQ39
	M_B_DM2	52	DM2	DQ39	141	M_B_DQ40
	M_B_DM3	67	DM3	DQ40	143	M_B_DQ41
	M_B_DM4	130	DM4	DQ41	151	M_B_DQ44
	M_B_DM5	147	DM5	DQ42	153	M_B_DQ45
	M_B_DM6	170	DM6	DQ43	140	M_B_DQ47
	M_B_DM7	185	DM7	DQ44	142	M_B_DQ46
12 M_B_DQS[7:0]	M_B_DQS0	13	DQ45	DQ45	152	M_B_DQ42
	M_B_DQS1	31	DQ46	DQ46	154	M_B_DQ43
	M_B_DQS2	51	DQ47	DQ47	157	M_B_DQ48
	M_B_DQS3	70	DQ48	DQ48	159	M_B_DQ52
	M_B_DQS4	131	DQ49	DQ49	173	M_B_DQ53
	M_B_DQS5	148	DQ50	DQ50	175	M_B_DQ49
	M_B_DQS6	169	DQ51	DQ51	158	M_B_DQ50
	M_B_DQS7	188	DQ52	DQ52	180	M_B_DQ55
12 M_B_DQS#[7:0]	M_B_DQS#0	11	DQ53	DQ53	174	M_B_DQ54
	M_B_DQS#1	29	DQ54	DQ54	176	M_B_DQ51
	M_B_DQS#2	49	DQ55	DQ55	179	M_B_DQ56
	M_B_DQS#3	68	DQ56	DQ56	181	M_B_DQ57
	M_B_DQS#4	129	DQ57	DQ57	189	M_B_DQ60
	M_B_DQS#5	146	DQ58	DQ58	191	M_B_DQ61
	M_B_DQS#6	167	DQ59	DQ59	180	M_B_DQ63
	M_B_DQS#7	186	DQ60	DQ60	182	M_B_DQ58
			DQ61	DQ61	192	M_B_DQ59
			DQ62	DQ62	194	M_B_DQ62
			DQ63	DQ63		

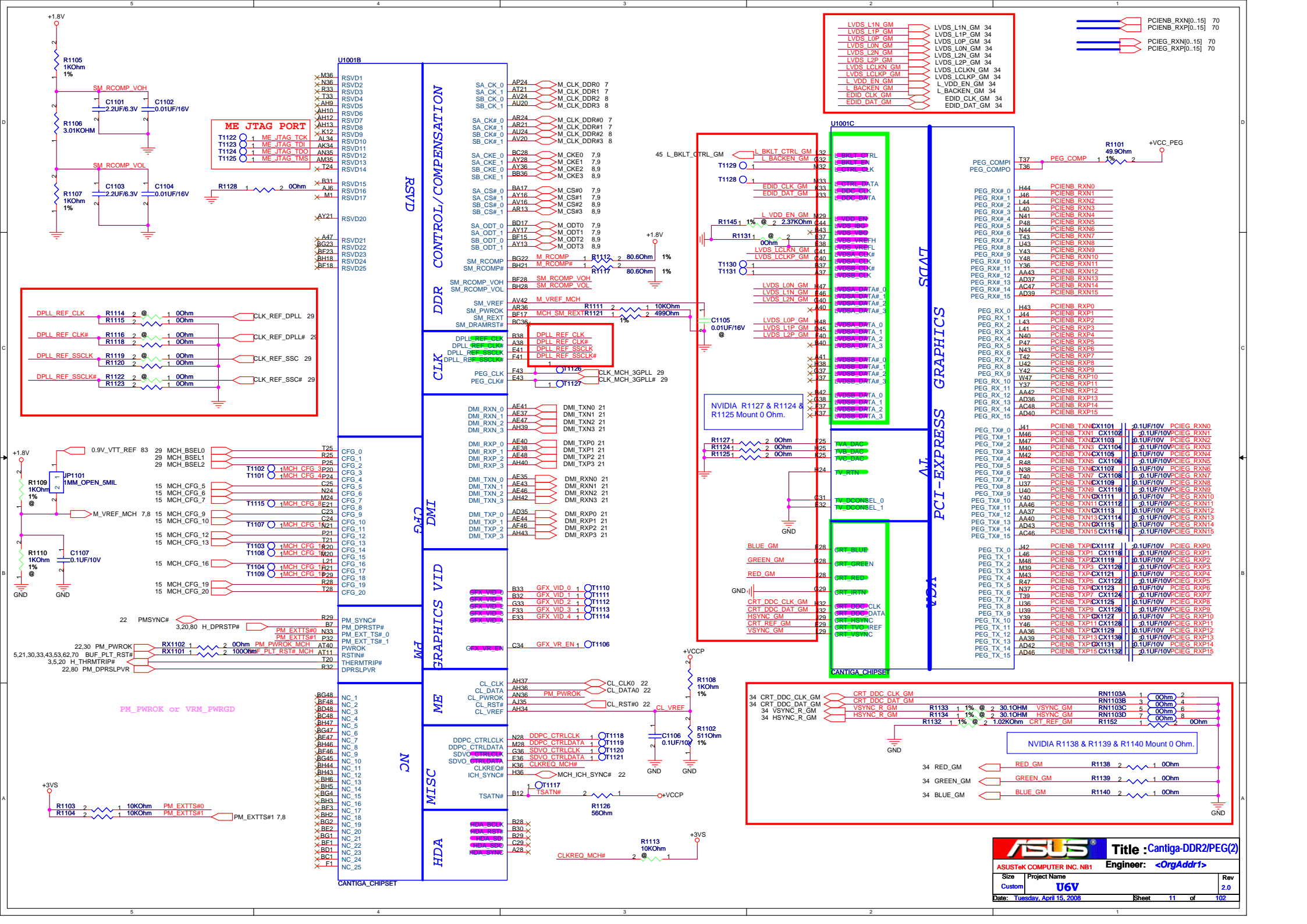








Cap 0.1uF within 100 mils from GMCH



**ME JTAG PORT**

T1122 1 ME JTAG TCK  
 T1123 1 ME JTAG TDI  
 T1124 1 ME JTAG TDO  
 T1125 1 ME JTAG TMS

DPLL REF\_CLK# R1114 2 @ 1 00hm  
 R1115 2 @ 1 00hm  
 DPLL REF\_CLK# R1116 2 @ 1 00hm  
 R1118 2 @ 1 00hm  
 DPLL REF\_SSCLK# R1119 2 @ 1 00hm  
 R1120 2 @ 1 00hm  
 DPLL REF\_SSCLK# R1122 2 @ 1 00hm  
 R1123 2 @ 1 00hm

MCH\_BSEL0 29 MCH\_BSEL1 29 MCH\_BSEL2 29  
 MCH\_CFG\_5 15 MCH\_CFG\_6 15 MCH\_CFG\_7 15  
 MCH\_CFG\_9 15 MCH\_CFG\_10 15  
 MCH\_CFG\_12 15 MCH\_CFG\_13 15  
 MCH\_CFG\_16 15 MCH\_CFG\_19 15 MCH\_CFG\_20 15

PM\_PWROK or VRM\_PWRGD  
 RX1102 1 2 00hm  
 RX1101 1 2 1000hm

PM\_EXTTSS#1 7.8  
 PM\_EXTTSS#0  
 PM\_EXTTSS#1

LVDS\_L1N\_GM LVDS\_L1N\_GM 34  
 LVDS\_L1P\_GM LVDS\_L1P\_GM 34  
 LVDS\_L0P\_GM LVDS\_L0P\_GM 34  
 LVDS\_L0N\_GM LVDS\_L0N\_GM 34  
 LVDS\_L2N\_GM LVDS\_L2N\_GM 34  
 LVDS\_L2P\_GM LVDS\_L2P\_GM 34  
 LVDS\_LCLKN\_GM LVDS\_LCLKN\_GM 34  
 LVDS\_LCLKP\_GM LVDS\_LCLKP\_GM 34  
 L\_VDD\_EN\_GM L\_VDD\_EN\_GM 34  
 L\_BACKEN\_GM L\_BACKEN\_GM 34  
 EDID\_CLK\_GM EDID\_CLK\_GM 34  
 EDID\_DAT\_GM EDID\_DAT\_GM 34

PCIENB\_RXN[0..15] 70  
 PCIENB\_RXP[0..15] 70  
 PCIEG\_RXN[0..15] 70  
 PCIEG\_RXP[0..15] 70

PCIENB\_RXN0 PCIENB\_RXN1  
 PCIENB\_RXN2 PCIENB\_RXN3  
 PCIENB\_RXN4 PCIENB\_RXN5  
 PCIENB\_RXN6 PCIENB\_RXN7  
 PCIENB\_RXN8 PCIENB\_RXN9  
 PCIENB\_RXN10 PCIENB\_RXN11  
 PCIENB\_RXN12 PCIENB\_RXN13  
 PCIENB\_RXN14 PCIENB\_RXN15

PCIENB\_RXP0 PCIENB\_RXP1  
 PCIENB\_RXP2 PCIENB\_RXP3  
 PCIENB\_RXP4 PCIENB\_RXP5  
 PCIENB\_RXP6 PCIENB\_RXP7  
 PCIENB\_RXP8 PCIENB\_RXP9  
 PCIENB\_RXP10 PCIENB\_RXP11  
 PCIENB\_RXP12 PCIENB\_RXP13  
 PCIENB\_RXP14 PCIENB\_RXP15

PCIENB\_TXN0 PCIENB\_TXN1  
 PCIENB\_TXN2 PCIENB\_TXN3  
 PCIENB\_TXN4 PCIENB\_TXN5  
 PCIENB\_TXN6 PCIENB\_TXN7  
 PCIENB\_TXN8 PCIENB\_TXN9  
 PCIENB\_TXN10 PCIENB\_TXN11  
 PCIENB\_TXN12 PCIENB\_TXN13  
 PCIENB\_TXN14 PCIENB\_TXN15

PCIENB\_TXP0 PCIENB\_TXP1  
 PCIENB\_TXP2 PCIENB\_TXP3  
 PCIENB\_TXP4 PCIENB\_TXP5  
 PCIENB\_TXP6 PCIENB\_TXP7  
 PCIENB\_TXP8 PCIENB\_TXP9  
 PCIENB\_TXP10 PCIENB\_TXP11  
 PCIENB\_TXP12 PCIENB\_TXP13  
 PCIENB\_TXP14 PCIENB\_TXP15

7 M\_A\_DQ[0:63]

M A DQ0	AJ38	SA_DQ_0
M A DQ1	AJ41	SA_DQ_1
M A DQ2	AN38	SA_DQ_2
M A DQ3	AJ38	SA_DQ_3
M A DQ4	AJ36	SA_DQ_4
M A DQ5	AJ40	SA_DQ_5
M A DQ6	AM44	SA_DQ_6
M A DQ7	AM42	SA_DQ_7
M A DQ8	AN43	SA_DQ_8
M A DQ9	AN44	SA_DQ_9
M A DQ10	AJ40	SA_DQ_10
M A DQ11	AT38	SA_DQ_11
M A DQ12	AN41	SA_DQ_12
M A DQ13	AN39	SA_DQ_13
M A DQ14	AU44	SA_DQ_14
M A DQ15	AU42	SA_DQ_15
M A DQ16	AV39	SA_DQ_16
M A DQ17	AY44	SA_DQ_17
M A DQ18	BA40	SA_DQ_18
M A DQ19	BD43	SA_DQ_19
M A DQ20	AV41	SA_DQ_20
M A DQ21	AY43	SA_DQ_21
M A DQ22	BA41	SA_DQ_22
M A DQ23	BA40	SA_DQ_23
M A DQ24	AY37	SA_DQ_24
M A DQ25	BD38	SA_DQ_25
M A DQ26	AV37	SA_DQ_26
M A DQ27	AT36	SA_DQ_27
M A DQ28	AY38	SA_DQ_28
M A DQ29	BA38	SA_DQ_29
M A DQ30	AV36	SA_DQ_30
M A DQ31	AW36	SA_DQ_31
M A DQ32	BD13	SA_DQ_32
M A DQ33	AU11	SA_DQ_33
M A DQ34	BC11	SA_DQ_34
M A DQ35	BA12	SA_DQ_35
M A DQ36	AU13	SA_DQ_36
M A DQ37	AV13	SA_DQ_37
M A DQ38	BD12	SA_DQ_38
M A DQ39	BC12	SA_DQ_39
M A DQ40	BB9	SA_DQ_40
M A DQ41	BA9	SA_DQ_41
M A DQ42	AU10	SA_DQ_42
M A DQ43	AV9	SA_DQ_43
M A DQ44	BA11	SA_DQ_44
M A DQ45	BD9	SA_DQ_45
M A DQ46	AY8	SA_DQ_46
M A DQ47	BA6	SA_DQ_47
M A DQ48	AV5	SA_DQ_48
M A DQ49	AV7	SA_DQ_49
M A DQ50	AT9	SA_DQ_50
M A DQ51	AN8	SA_DQ_51
M A DQ52	AU5	SA_DQ_52
M A DQ53	AU6	SA_DQ_53
M A DQ54	AT5	SA_DQ_54
M A DQ55	AN10	SA_DQ_55
M A DQ56	AM11	SA_DQ_56
M A DQ57	AM5	SA_DQ_57
M A DQ58	AJ9	SA_DQ_58
M A DQ59	AJ8	SA_DQ_59
M A DQ60	AN12	SA_DQ_60
M A DQ61	AM13	SA_DQ_61
M A DQ62	AJ11	SA_DQ_62
M A DQ63	AJ12	SA_DQ_63

CANTIGA\_CHIPSET

DDR SYSTEM MEMORY A

SA_BS_0	BD21	M_A_BS0	7,9
SA_BS_1	BG18	M_A_BS1	7,9
SA_BS_2	AT25	M_A_BS2	7,9
SA_RAS#	BB20	M_A_RAS#	7,9
SA_CAS#	BD20	M_A_CAS#	7,9
SA_WE#	AY20	M_A_WE#	7,9
SA_DM_0	AM37	M_A_DM0	7
SA_DM_1	AT41	M_A_DM1	7
SA_DM_2	AY41	M_A_DM2	7
SA_DM_3	AU39	M_A_DM3	7
SA_DM_4	BB12	M_A_DM4	7
SA_DM_5	AY6	M_A_DM5	7
SA_DM_6	AT7	M_A_DM6	7
SA_DM_7	AJ5	M_A_DM7	7
SA_DQS_0	AJ44	M_A_DQS0	7
SA_DQS_1	AT44	M_A_DQS1	7
SA_DQS_2	BA43	M_A_DQS2	7
SA_DQS_3	BC37	M_A_DQS3	7
SA_DQS_4	AW12	M_A_DQS4	7
SA_DQS_5	BC8	M_A_DQS5	7
SA_DQS_6	AU8	M_A_DQS6	7
SA_DQS_7	AM7	M_A_DQS7	7
SA_DQS#_0	AJ43	M_A_DQS#0	7
SA_DQS#_1	AT43	M_A_DQS#1	7
SA_DQS#_2	BA44	M_A_DQS#2	7
SA_DQS#_3	BD37	M_A_DQS#3	7
SA_DQS#_4	AY12	M_A_DQS#4	7
SA_DQS#_5	BD8	M_A_DQS#5	7
SA_DQS#_6	AU9	M_A_DQS#6	7
SA_DQS#_7	AM8	M_A_DQS#7	7
SA_MA_0	BA21	M_A_A0	7,9
SA_MA_1	BC24	M_A_A1	7,9
SA_MA_2	BG24	M_A_A2	7,9
SA_MA_3	BH24	M_A_A3	7,9
SA_MA_4	BG25	M_A_A4	7,9
SA_MA_5	BA24	M_A_A5	7,9
SA_MA_6	BD24	M_A_A6	7,9
SA_MA_7	BG27	M_A_A7	7,9
SA_MA_8	BF25	M_A_A8	7,9
SA_MA_9	AW24	M_A_A9	7,9
SA_MA_10	BC21	M_A_A10	7,9
SA_MA_11	BG26	M_A_A11	7,9
SA_MA_12	BH26	M_A_A12	7,9
SA_MA_13	BH17	M_A_A13	7,9
SA_MA_14	AY25	M_A_A14	7,9

8 M\_B\_DQ[0:63]

M B DQ0	AK47	SB_DQ_0
M B DQ1	AH46	SB_DQ_1
M B DQ2	AP47	SB_DQ_2
M B DQ3	AP46	SB_DQ_3
M B DQ4	AJ46	SB_DQ_4
M B DQ5	AJ48	SB_DQ_5
M B DQ6	AM48	SB_DQ_6
M B DQ7	AP48	SB_DQ_7
M B DQ8	AU47	SB_DQ_8
M B DQ9	AU46	SB_DQ_9
M B DQ10	BA48	SB_DQ_10
M B DQ11	AY48	SB_DQ_11
M B DQ12	AT47	SB_DQ_12
M B DQ13	AR47	SB_DQ_13
M B DQ14	BA47	SB_DQ_14
M B DQ15	BC47	SB_DQ_15
M B DQ16	BC46	SB_DQ_16
M B DQ17	BC44	SB_DQ_17
M B DQ18	BG43	SB_DQ_18
M B DQ19	BF43	SB_DQ_19
M B DQ20	BE45	SB_DQ_20
M B DQ21	BC41	SB_DQ_21
M B DQ22	BF40	SB_DQ_22
M B DQ23	BF41	SB_DQ_23
M B DQ24	BG38	SB_DQ_24
M B DQ25	BF38	SB_DQ_25
M B DQ26	BH35	SB_DQ_26
M B DQ27	BG35	SB_DQ_27
M B DQ28	BH40	SB_DQ_28
M B DQ29	BG39	SB_DQ_29
M B DQ30	BG34	SB_DQ_30
M B DQ31	BH34	SB_DQ_31
M B DQ32	BH14	SB_DQ_32
M B DQ33	BG12	SB_DQ_33
M B DQ34	BH11	SB_DQ_34
M B DQ35	BG8	SB_DQ_35
M B DQ36	BH12	SB_DQ_36
M B DQ37	BF11	SB_DQ_37
M B DQ38	BF8	SB_DQ_38
M B DQ39	BG7	SB_DQ_39
M B DQ40	BC5	SB_DQ_40
M B DQ41	BC6	SB_DQ_41
M B DQ42	AY3	SB_DQ_42
M B DQ43	AY1	SB_DQ_43
M B DQ44	BF6	SB_DQ_44
M B DQ45	BF5	SB_DQ_45
M B DQ46	BA1	SB_DQ_46
M B DQ47	BD3	SB_DQ_47
M B DQ48	AV2	SB_DQ_48
M B DQ49	AU3	SB_DQ_49
M B DQ50	AR3	SB_DQ_50
M B DQ51	AN2	SB_DQ_51
M B DQ52	AY2	SB_DQ_52
M B DQ53	AV1	SB_DQ_53
M B DQ54	AP3	SB_DQ_54
M B DQ55	AR1	SB_DQ_55
M B DQ56	AL1	SB_DQ_56
M B DQ57	AL2	SB_DQ_57
M B DQ58	AJ1	SB_DQ_58
M B DQ59	AH1	SB_DQ_59
M B DQ60	AM2	SB_DQ_60
M B DQ61	AM3	SB_DQ_61
M B DQ62	AH3	SB_DQ_62
M B DQ63	AJ3	SB_DQ_63

CANTIGA\_CHIPSET

DDR SYSTEM MEMORY B

SB_BS_0	BC16	M_B_BS0	8,9
SB_BS_1	BB17	M_B_BS1	8,9
SB_BS_2	BB33	M_B_BS2	8,9
SB_RAS#	AU17	M_B_RAS#	8,9
SB_CAS#	BG16	M_B_CAS#	8,9
SB_WE#	BF14	M_B_WE#	8,9
SB_DM_0	AM47	M_B_DM0	8
SB_DM_1	AY47	M_B_DM1	8
SB_DM_2	BD40	M_B_DM2	8
SB_DM_3	BF35	M_B_DM3	8
SB_DM_4	BC11	M_B_DM4	8
SB_DM_5	BA3	M_B_DM5	8
SB_DM_6	AP1	M_B_DM6	8
SB_DM_7	AK2	M_B_DM7	8
SB_DQS_0	AL47	M_B_DQS0	8
SB_DQS_1	AV48	M_B_DQS1	8
SB_DQS_2	BG41	M_B_DQS2	8
SB_DQS_3	BG37	M_B_DQS3	8
SB_DQS_4	BH9	M_B_DQS4	8
SB_DQS_5	BB2	M_B_DQS5	8
SB_DQS_6	AU1	M_B_DQS6	8
SB_DQS_7	AN6	M_B_DQS7	8
SB_DQS#_0	AL46	M_B_DQS#0	8
SB_DQS#_1	AV47	M_B_DQS#1	8
SB_DQS#_2	BH41	M_B_DQS#2	8
SB_DQS#_3	BH37	M_B_DQS#3	8
SB_DQS#_4	BG9	M_B_DQS#4	8
SB_DQS#_5	BC2	M_B_DQS#5	8
SB_DQS#_6	AT2	M_B_DQS#6	8
SB_DQS#_7	AN5	M_B_DQS#7	8
SB_MA_0	AV17	M_B_A0	8,9
SB_MA_1	BA25	M_B_A1	8,9
SB_MA_2	BC25	M_B_A2	8,9
SB_MA_3	AU25	M_B_A3	8,9
SB_MA_4	AW25	M_B_A4	8,9
SB_MA_5	BB28	M_B_A5	8,9
SB_MA_6	AU28	M_B_A6	8,9
SB_MA_7	AW28	M_B_A7	8,9
SB_MA_8	AT33	M_B_A8	8,9
SB_MA_9	BD33	M_B_A9	8,9
SB_MA_10	BB16	M_B_A10	8,9
SB_MA_11	AY33	M_B_A11	8,9
SB_MA_12	BH15	M_B_A12	8,9
SB_MA_13	AU33	M_B_A13	8,9
SB_MA_14			

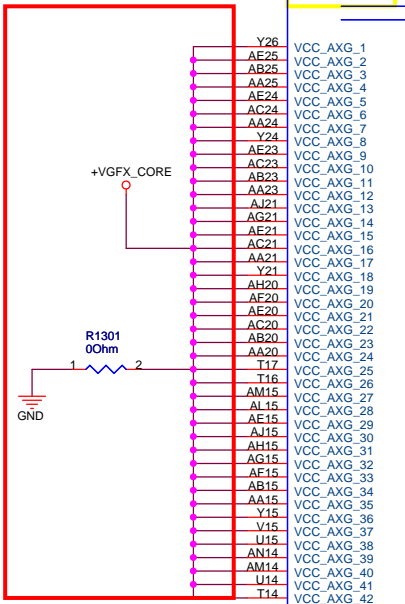
**ASUS** Title : Cantiga-DDR2 bus (3)  
 ASUSTek COMPUTER INC. NBI Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	U6V	2.0
Date: Tuesday, April 15, 2008	Sheet 12 of	102

+1.8V_GMCH	AP33	VCC_SM_1
	AN33	VCC_SM_2
	BH32	VCC_SM_3
	BG32	VCC_SM_4
	BF32	VCC_SM_5
	BD32	VCC_SM_6
	BC32	VCC_SM_7
	BB32	VCC_SM_8
	BA32	VCC_SM_9
	AY32	VCC_SM_10
	AW32	VCC_SM_11
	AV32	VCC_SM_12
	AU32	VCC_SM_13
	AT32	VCC_SM_14
	AR32	VCC_SM_15
	AP32	VCC_SM_16
	AN32	VCC_SM_17
	AH31	VCC_SM_18
	BF31	VCC_SM_19
	BG30	VCC_SM_20
	BH29	VCC_SM_21
	BG29	VCC_SM_22
	BF29	VCC_SM_23
	BD29	VCC_SM_24
	BC29	VCC_SM_25
	BB29	VCC_SM_26
	BA29	VCC_SM_27
	AY29	VCC_SM_28
	AW29	VCC_SM_29
	AV29	VCC_SM_30
	AU29	VCC_SM_31
	AT29	VCC_SM_32
	AR29	VCC_SM_33
	AP29	VCC_SM_34
		VCC_SM_35

FOR DDR3  
DDR2 MAY BE NC

T1303	1	BA36	VCC_SM_36/NC
T1304	1	BB24	VCC_SM_37/NC
T1305	1	BD16	VCC_SM_38/NC
T1306	1	BB21	VCC_SM_39/NC
T1307	1	AW16	VCC_SM_40/NC
T1308	1	AW13	VCC_SM_41/NC
T1309	1	AT13	VCC_SM_42/NC



VCC_SM_1	W28	VCC_AGX_NCTF_1
VCC_SM_2	V28	VCC_AGX_NCTF_2
VCC_SM_3	W26	VCC_AGX_NCTF_3
VCC_SM_4	V26	VCC_AGX_NCTF_4
VCC_SM_5	W25	VCC_AGX_NCTF_5
VCC_SM_6	W24	VCC_AGX_NCTF_6
VCC_SM_7	V24	VCC_AGX_NCTF_7
VCC_SM_8	W23	VCC_AGX_NCTF_8
VCC_SM_9	V23	VCC_AGX_NCTF_9
VCC_SM_10	W22	VCC_AGX_NCTF_10
VCC_SM_11	AM21	VCC_AGX_NCTF_11
VCC_SM_12	AK21	VCC_AGX_NCTF_12
VCC_SM_13	W21	VCC_AGX_NCTF_13
VCC_SM_14	V21	VCC_AGX_NCTF_14
VCC_SM_15	W20	VCC_AGX_NCTF_15
VCC_SM_16	AK20	VCC_AGX_NCTF_16
VCC_SM_17	U20	VCC_AGX_NCTF_17
VCC_SM_18	AM19	VCC_AGX_NCTF_18
VCC_SM_19	AL19	VCC_AGX_NCTF_19
VCC_SM_20	AK19	VCC_AGX_NCTF_20
VCC_SM_21	U19	VCC_AGX_NCTF_21
VCC_SM_22	AM18	VCC_AGX_NCTF_22
VCC_SM_23	AL18	VCC_AGX_NCTF_23
VCC_SM_24	AK18	VCC_AGX_NCTF_24
VCC_SM_25	U18	VCC_AGX_NCTF_25
VCC_SM_26	AM17	VCC_AGX_NCTF_26
VCC_SM_27	AL17	VCC_AGX_NCTF_27
VCC_SM_28	AK17	VCC_AGX_NCTF_28
VCC_SM_29	U17	VCC_AGX_NCTF_29
VCC_SM_30	AM16	VCC_AGX_NCTF_30
VCC_SM_31	AL16	VCC_AGX_NCTF_31
VCC_SM_32	AK16	VCC_AGX_NCTF_32
VCC_SM_33	U16	VCC_AGX_NCTF_33
VCC_SM_34	AM15	VCC_AGX_NCTF_34
VCC_SM_35	AL15	VCC_AGX_NCTF_35
VCC_SM_36/NC	AK15	VCC_AGX_NCTF_36
VCC_SM_37/NC	U15	VCC_AGX_NCTF_37
VCC_SM_38/NC	AM14	VCC_AGX_NCTF_38
VCC_SM_39/NC	AL14	VCC_AGX_NCTF_39
VCC_SM_40/NC	AK14	VCC_AGX_NCTF_40
VCC_SM_41/NC	U14	VCC_AGX_NCTF_41
VCC_SM_42/NC	AM13	VCC_AGX_NCTF_42

VCC_AGX_1	Y26	VCC_AGX_NCTF_43
VCC_AGX_2	AE25	VCC_AGX_NCTF_44
VCC_AGX_3	AB25	VCC_AGX_NCTF_45
VCC_AGX_4	AA25	VCC_AGX_NCTF_46
VCC_AGX_5	AE24	VCC_AGX_NCTF_47
VCC_AGX_6	AC24	VCC_AGX_NCTF_48
VCC_AGX_7	AA24	VCC_AGX_NCTF_49
VCC_AGX_8	Y24	VCC_AGX_NCTF_50
VCC_AGX_9	AE23	VCC_AGX_NCTF_51
VCC_AGX_10	AC23	VCC_AGX_NCTF_52
VCC_AGX_11	AA23	VCC_AGX_NCTF_53
VCC_AGX_12	AJ21	VCC_AGX_NCTF_54
VCC_AGX_13	AG21	VCC_AGX_NCTF_55
VCC_AGX_14	AE21	VCC_AGX_NCTF_56
VCC_AGX_15	AC21	VCC_AGX_NCTF_57
VCC_AGX_16	AA21	VCC_AGX_NCTF_58
VCC_AGX_17	Y21	VCC_AGX_NCTF_59
VCC_AGX_18	AH20	VCC_AGX_NCTF_60
VCC_AGX_19	AF20	
VCC_AGX_20	AE20	
VCC_AGX_21	AC20	
VCC_AGX_22	AB20	
VCC_AGX_23	AA20	
VCC_AGX_24	T17	
VCC_AGX_25	T16	
VCC_AGX_26	AM15	
VCC_AGX_27	AL15	
VCC_AGX_28	AE15	
VCC_AGX_29	AH15	
VCC_AGX_30	AH15	
VCC_AGX_31	AG15	
VCC_AGX_32	AF15	
VCC_AGX_33	AB15	
VCC_AGX_34	AA15	
VCC_AGX_35	AA15	
VCC_AGX_36	Y15	
VCC_AGX_37	U15	
VCC_AGX_38	AN14	
VCC_AGX_39	AM14	
VCC_AGX_40	U14	
VCC_AGX_41	U14	
VCC_AGX_42	T14	

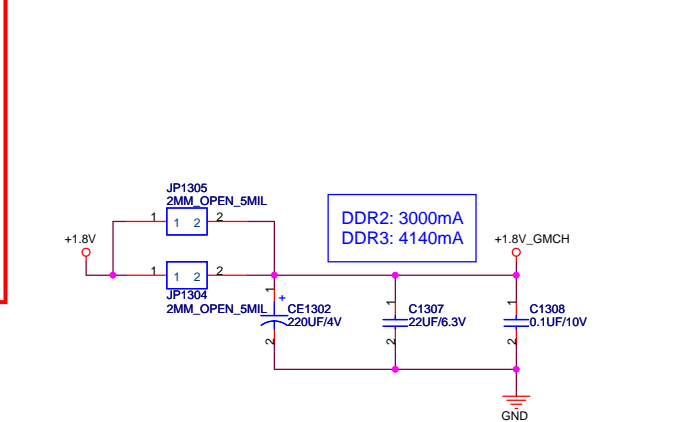
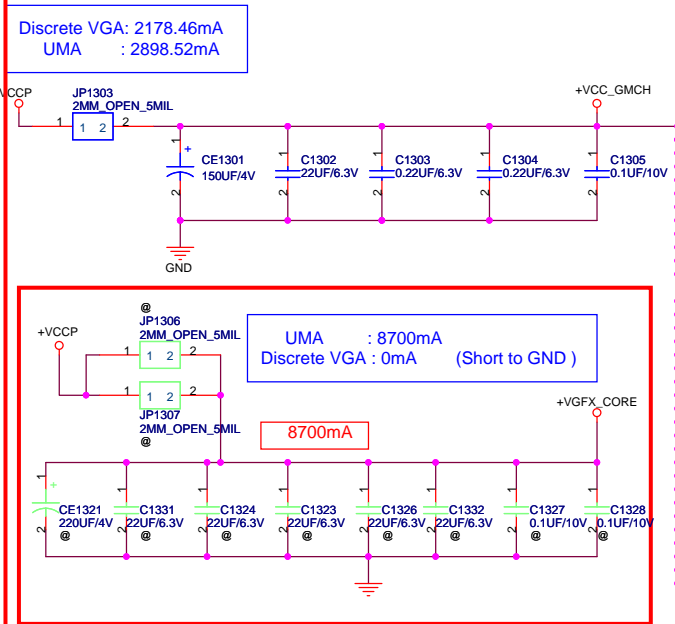
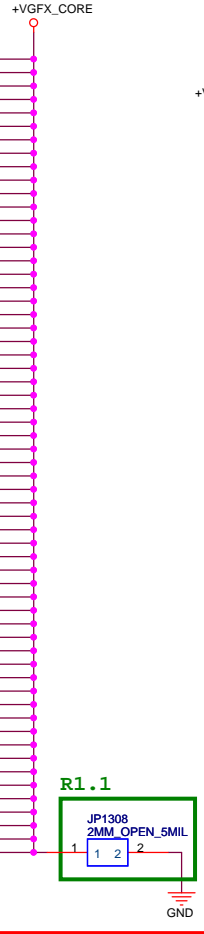
VCC SM POWER

VCC GFX NCTF

VCC GFX

VCC SM LF

VCC_SM_LF1	AV44	VCC_SM_LF1
VCC_SM_LF2	BA37	VCC_SM_LF2
VCC_SM_LF3	AM40	VCC_SM_LF3
VCC_SM_LF4	AV21	VCC_SM_LF4
VCC_SM_LF5	AY21	VCC_SM_LF5
VCC_SM_LF6	AM10	VCC_SM_LF6
VCC_SM_LF7	BB13	VCC_SM_LF7



VCC_1	AG34	VCC_NCTF_1
VCC_2	AC34	VCC_NCTF_2
VCC_3	AB34	VCC_NCTF_3
VCC_4	AA34	VCC_NCTF_4
VCC_5	Y34	VCC_NCTF_5
VCC_6	U34	VCC_NCTF_6
VCC_7	AM33	VCC_NCTF_7
VCC_8	AK33	VCC_NCTF_8
VCC_9	AJ33	VCC_NCTF_9
VCC_10	AG33	VCC_NCTF_10
VCC_11	AF33	VCC_NCTF_11
VCC_12		VCC_NCTF_12
VCC_13	AE33	VCC_NCTF_13
VCC_14	AC33	VCC_NCTF_14
VCC_15	AA33	VCC_NCTF_15
VCC_16	Y33	VCC_NCTF_16
VCC_17	W33	VCC_NCTF_17
VCC_18	V33	VCC_NCTF_18
VCC_19	U33	VCC_NCTF_19
VCC_20	AH28	VCC_NCTF_20
VCC_21	AF28	VCC_NCTF_21
VCC_22	AC28	VCC_NCTF_22
VCC_23	AA28	VCC_NCTF_23
VCC_24	AJ26	VCC_NCTF_24
VCC_25	AG26	VCC_NCTF_25
VCC_26	AE26	VCC_NCTF_26
VCC_27	AC26	VCC_NCTF_27
VCC_28	AH25	VCC_NCTF_28
VCC_29	AG25	VCC_NCTF_29
VCC_30	AF25	VCC_NCTF_30
VCC_31	AC24	VCC_NCTF_31
VCC_32	AJ23	VCC_NCTF_32
VCC_33	AH23	VCC_NCTF_33
VCC_34	AF23	VCC_NCTF_34
VCC_35	T32	VCC_NCTF_35

VCC CORE POWER

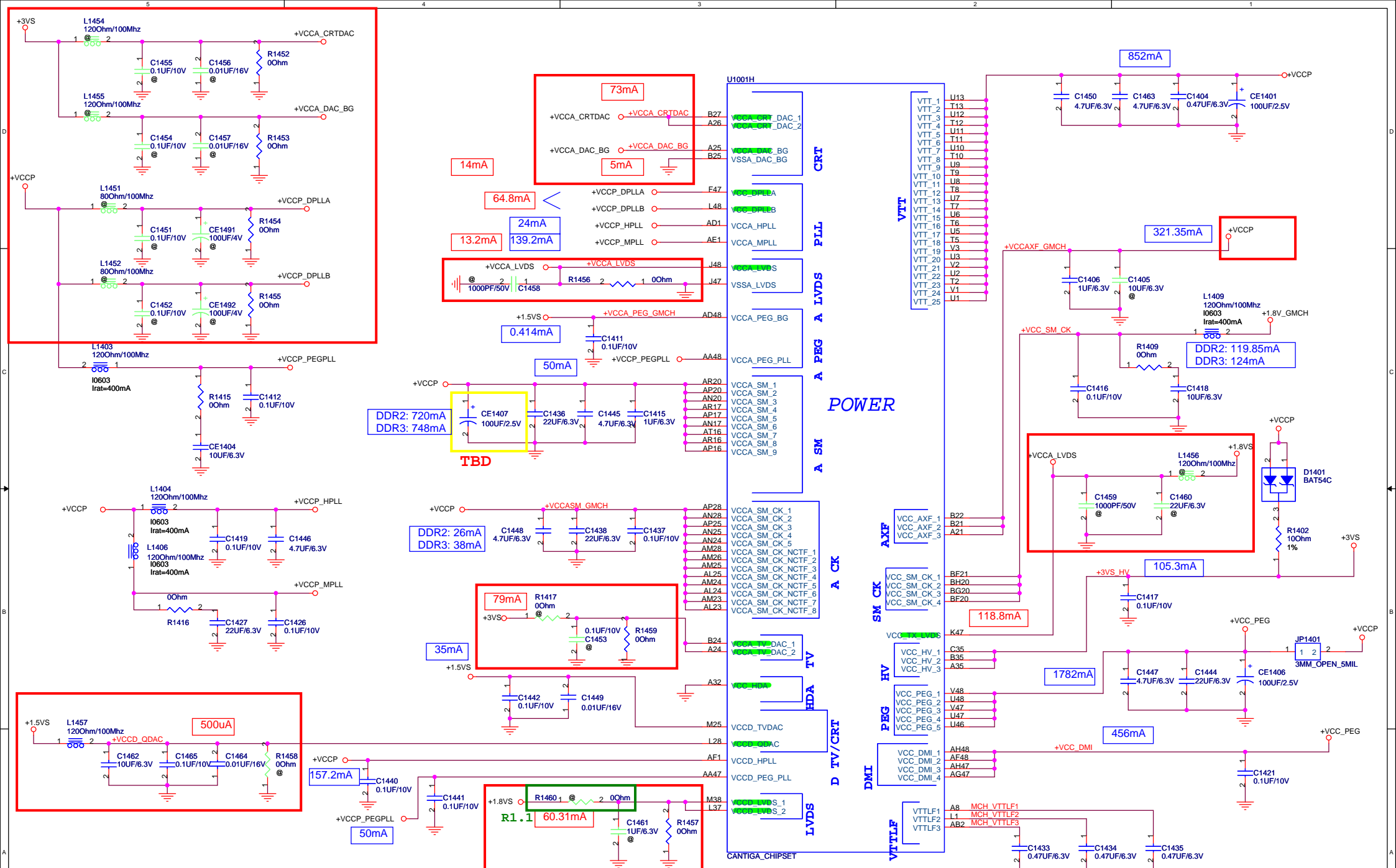
VCC NCTF

VCC_NCTF_1	AM32	VCC_NCTF_1
VCC_NCTF_2	AL32	VCC_NCTF_2
VCC_NCTF_3	AK32	VCC_NCTF_3
VCC_NCTF_4	AJ32	VCC_NCTF_4
VCC_NCTF_5	AG32	VCC_NCTF_5
VCC_NCTF_6	AE32	VCC_NCTF_6
VCC_NCTF_7	AC32	VCC_NCTF_7
VCC_NCTF_8	AA32	VCC_NCTF_8
VCC_NCTF_9	Y32	VCC_NCTF_9
VCC_NCTF_10	V32	VCC_NCTF_10
VCC_NCTF_11	U32	VCC_NCTF_11
VCC_NCTF_12	AM30	VCC_NCTF_12
VCC_NCTF_13	AL30	VCC_NCTF_13
VCC_NCTF_14	AK30	VCC_NCTF_14
VCC_NCTF_15	AJ30	VCC_NCTF_15
VCC_NCTF_16	AG30	VCC_NCTF_16
VCC_NCTF_17	AF30	VCC_NCTF_17
VCC_NCTF_18	AE30	VCC_NCTF_18
VCC_NCTF_19	AC30	VCC_NCTF_19
VCC_NCTF_20	AA30	VCC_NCTF_20
VCC_NCTF_21	Y30	VCC_NCTF_21
VCC_NCTF_22	V30	VCC_NCTF_22
VCC_NCTF_23	U30	VCC_NCTF_23
VCC_NCTF_24	AM29	VCC_NCTF_24
VCC_NCTF_25	AL29	VCC_NCTF_25
VCC_NCTF_26	AK29	VCC_NCTF_26
VCC_NCTF_27	AJ29	VCC_NCTF_27
VCC_NCTF_28	AG29	VCC_NCTF_28
VCC_NCTF_29	AF29	VCC_NCTF_29
VCC_NCTF_30	AE29	VCC_NCTF_30
VCC_NCTF_31	AC29	VCC_NCTF_31
VCC_NCTF_32	AA29	VCC_NCTF_32
VCC_NCTF_33	Y29	VCC_NCTF_33
VCC_NCTF_34	V29	VCC_NCTF_34
VCC_NCTF_35	U29	VCC_NCTF_35
VCC_NCTF_36	AM28	VCC_NCTF_36
VCC_NCTF_37	AL28	VCC_NCTF_37
VCC_NCTF_38	AK28	VCC_NCTF_38
VCC_NCTF_39	AJ28	VCC_NCTF_39
VCC_NCTF_40	AG28	VCC_NCTF_40
VCC_NCTF_41	AF28	VCC_NCTF_41
VCC_NCTF_42	AE28	VCC_NCTF_42
VCC_NCTF_43	AC28	VCC_NCTF_43
VCC_NCTF_44	AA28	VCC_NCTF_44

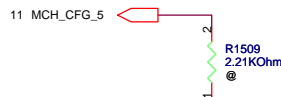
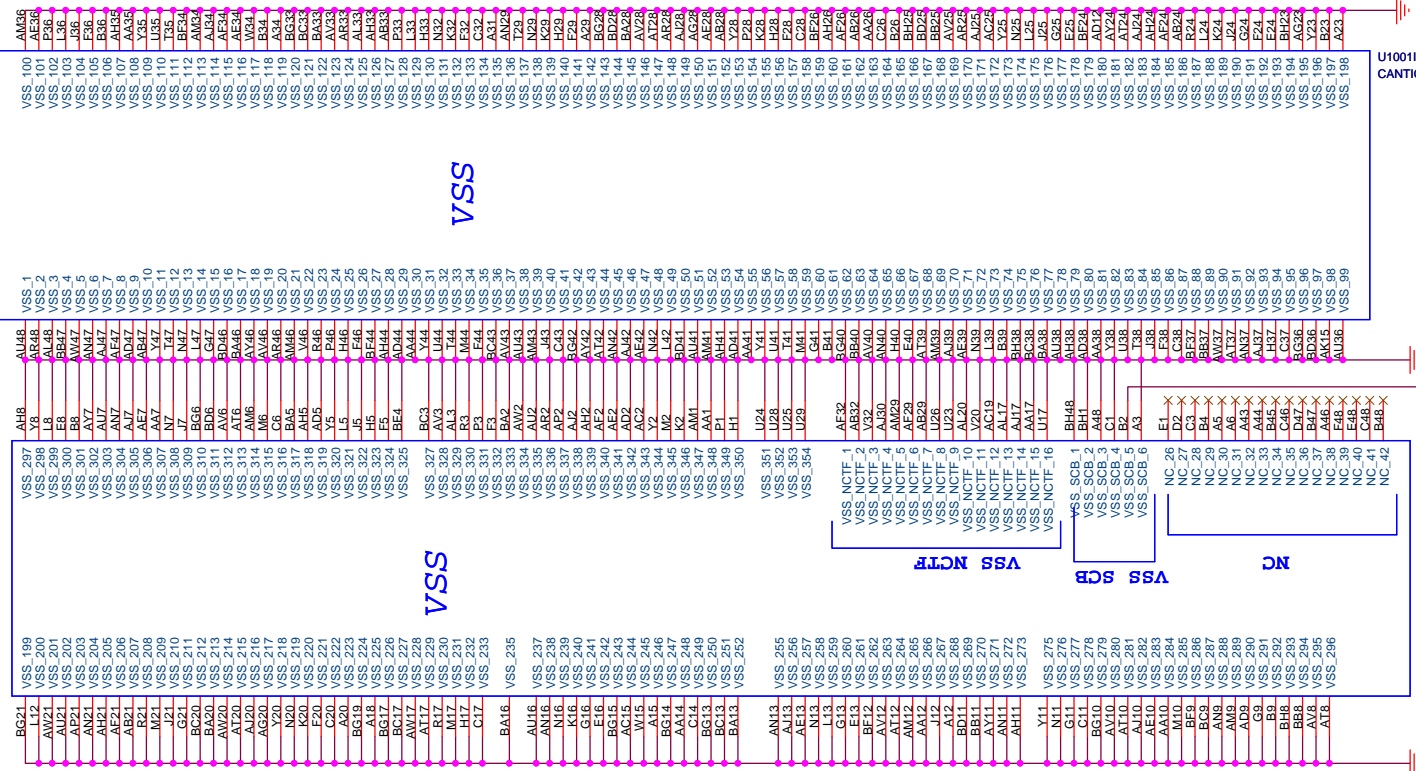
CANTIGA\_CHIPSET

T1301	1	VCC_AGX_SENSE	AJ14	VCC_AGX_SENSE
T1302	1	VSS_AGX_SENSE	AH14	VSS_AGX_SENSE

Route VCC\_AGX\_SENSE and VSS\_AGX\_SENSE differentially.



Power disable guidelines Refer to Design Guide Table 72  
 iAMT Power disable guidelines Refer to Design Guide 5.3.23.4  
 HDA Refer to 3.10.4



**CFG5 : DMI STRAP**  
**HIGH = DMI X 4 (Default)**  
**LOW = DMI X 2**



**CFG6 : Integrated TPM Host Interface**  
**HIGH = iTPM disable (Default)**  
**LOW = iTPM enable**



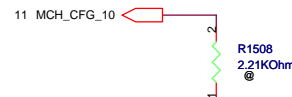
**CFG7 : Intel ME Crypto Strap Transport Layer Security cipher suite**  
**HIGH = With confidentiality (Default)**  
**LOW = Without confidentiality**



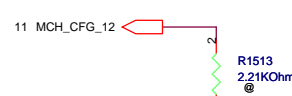
**CFG9 : PCIE GRAPHIC LANE**  
**HIGH = Normal Operation (Default)**  
**LOW = Reverse Lanes**



**CFG16 : FSB Dynamic ODT**  
**HIGH = Enable (Default)**  
**LOW = Disable**



**CFG10 : PCIe Loopback**  
**HIGH = Disable (Default)**  
**LOW = Enable**



**CFG [13:12] : XOR/ALL-Z**  
**00 = Reserved**  
**01= XOR Mode Enabled**  
**10= All-Z Mode Enabled**  
**11= Normal Operation (Default)**



**CFG19 : DMI Lane Reversal**  
**LOW = NORMAL (default)**  
**HIGH = Reverse Lanes**



**CFG20 : SDVO/PCIE CONCURRENT MODE**  
**LOW = ONLY SDVO or PCIE is Operational (Default)**  
**HIGH = SDVO and PCIE are operating simultaneously via the PEG port**

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Title :

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
A	U6V	2.0

Date: Tuesday, April 15, 2008

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Title :

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
A	U6V	2.0

Date: Tuesday, April 15, 2008

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Title :

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
A	U6V	2.0

Date: Tuesday, April 15, 2008

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Title :

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
A	U6V	2.0

Date: Tuesday, April 15, 2008

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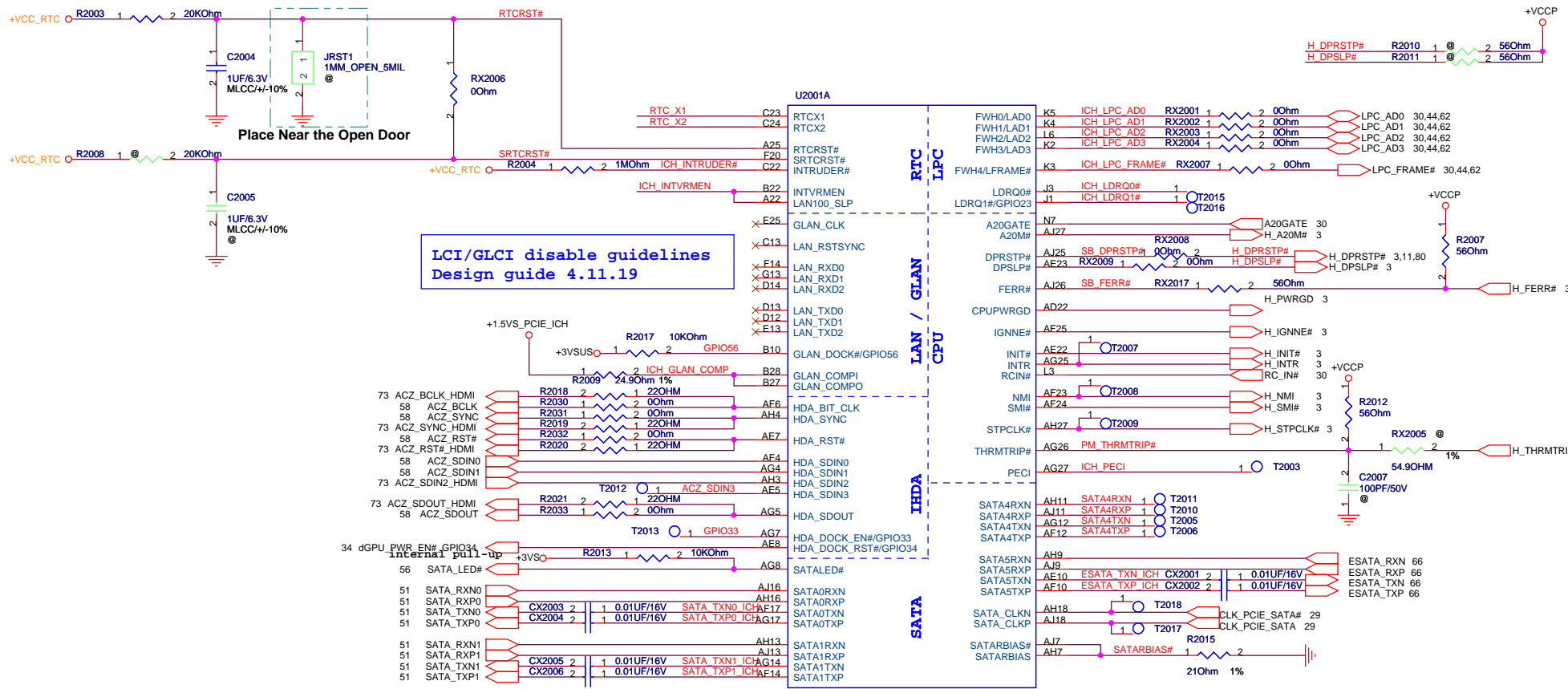
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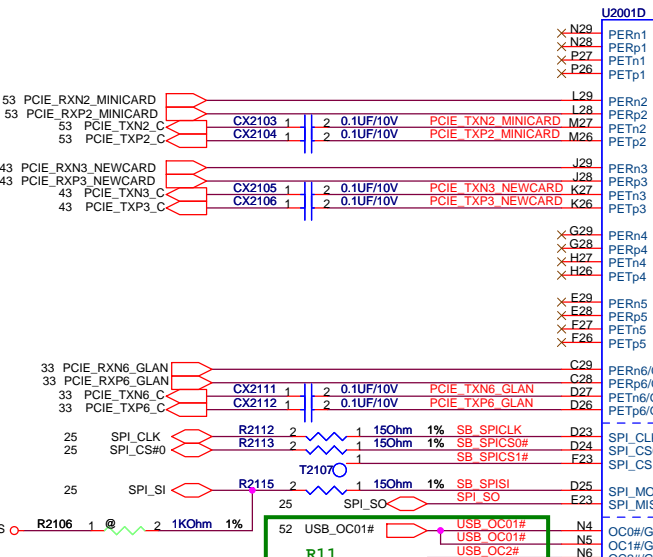
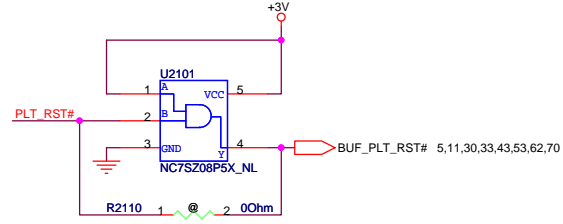
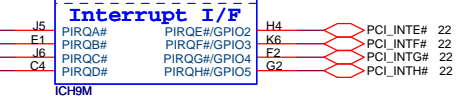
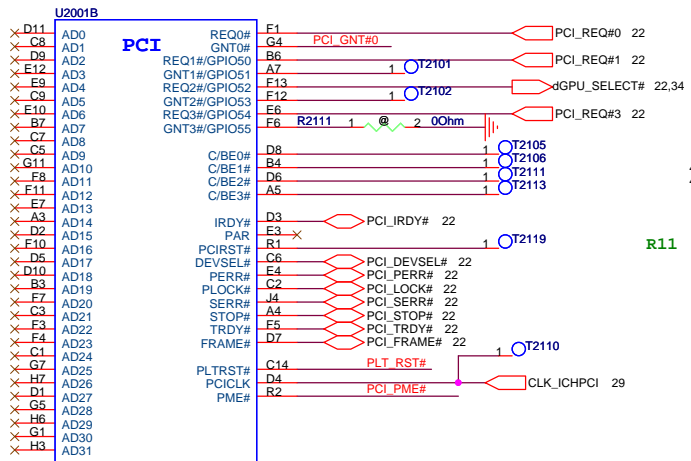
**LCI/GLCI disable guidelines**  
Design guide 4.11.19

**Flash Descriptor Security Override**  
High = Enable ( Default )  
Low = Overridden

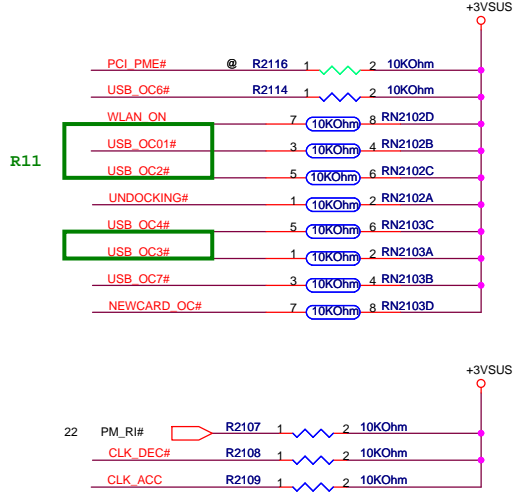
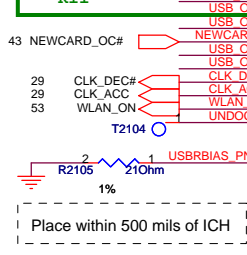
**VccSus1\_05, VccSus1\_5, & VccCL1\_5 Internal VR**  
High = Enable ( Default )  
Low = Disable

**XOR Chain Entrance Strap [ICH\_TP3, ACZ\_SDOUT] :**  
ICH\_TP3(T2207) default high  
00 = Reserved  
01 = Enter XOR Chain  
10 = Normal Operation (Default)  
11 = Set PCIe Port Config Bit 1

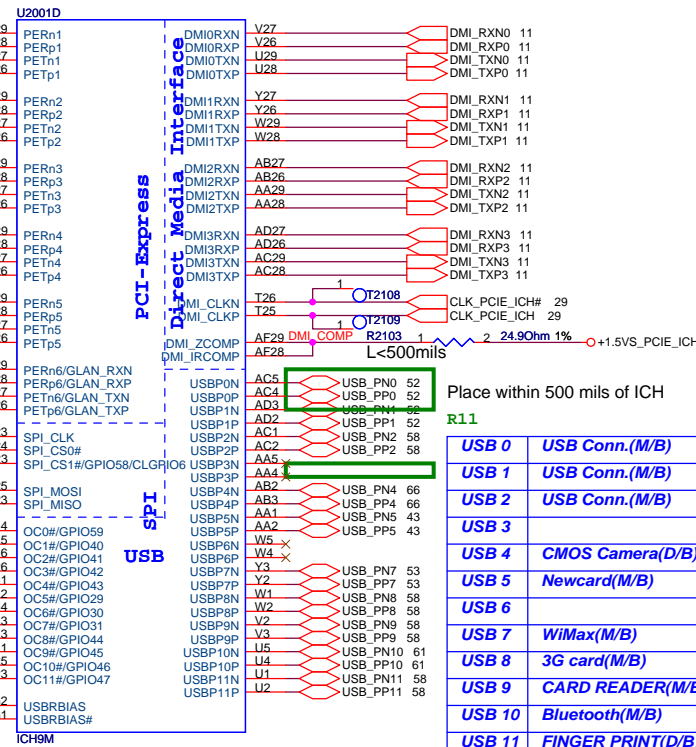
**ASUS** Title : **SB-ICH9M(1)**  
ASUSTek COMPUTER INC. NBI Engineer: <OrgAddr1>  
Size Project Name  
Custom **U6V**  
Date: Thursday, April 24, 2008 Sheet 20 of 102



**SPI\_MOSI ITPM Enable**  
 High = Enable  
 Low = Disable(Default)



When supporting CLK GEN Turbo PIN, UNI R2108, R2109



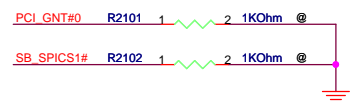
Place within 500 mils of ICH

USB 0	USB Conn.(M/B)
USB 1	USB Conn.(M/B)
USB 2	USB Conn.(M/B)
USB 3	
USB 4	CMOS Camera(D/B)
USB 5	Newcard(M/B)
USB 6	
USB 7	WiMax(M/B)
USB 8	3G card(M/B)
USB 9	CARD READER(M/B)
USB 10	Bluetooth(M/B)
USB 11	FINGER PRINT(D/B)

ICH9 Boot BIOS select

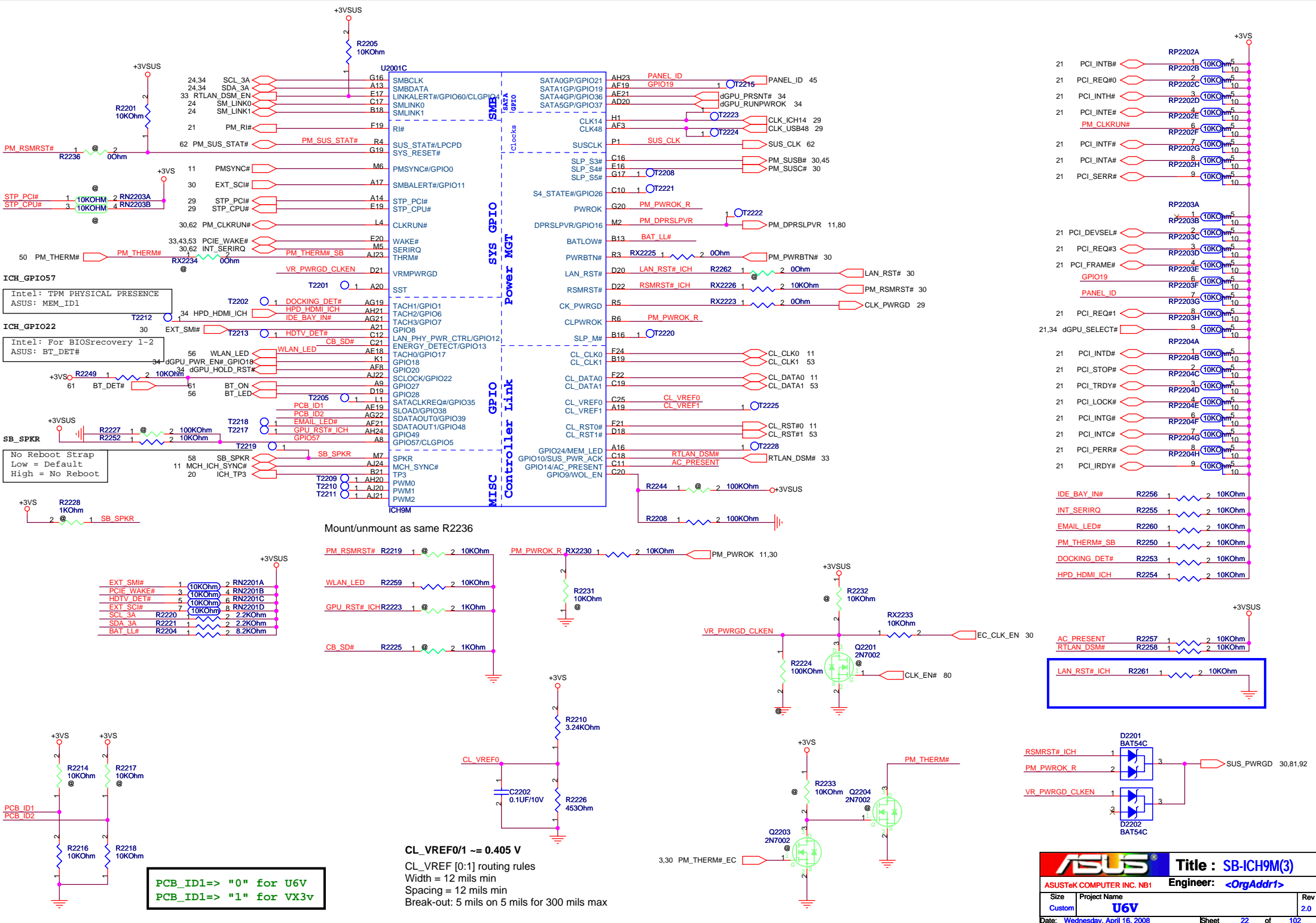
LPC	11	1	1
PCI	10	1	0
SPI	01	0	1

(default)



Refer to Montevina GPIO R1.1

PCIE 1	
PCIE 2	WLAN
PCIE 3	Newcard
PCIE 4	
PCIE 5	
PCIE 6	LAN

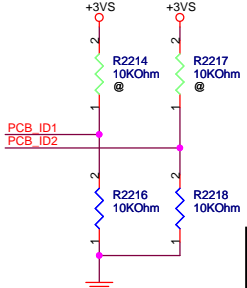


Intel: TPM PHYSICAL PRESENCE  
ASUS: MEM\_ID1

Intel: For BIOSrecovery 1-2  
ASUS: BT\_DET#

No Reboot Strap  
Low = Default  
High = No Reboot

- EXT\_SMI# 1 (10KOhm) 2 RN2201A
- PCIE\_WAKE# 3 (10KOhm) 4 RN2201B
- HDTV\_DET# 4 (10KOhm) 5 RN2201C
- EXT\_SCI# 5 (10KOhm) 8 RN2201D
- SCL\_3A R2220 2 2.2KOhm
- SDA\_3A R2221 1 2 2.2KOhm
- BAT\_LL# R2204 1 2 8.2KOhm

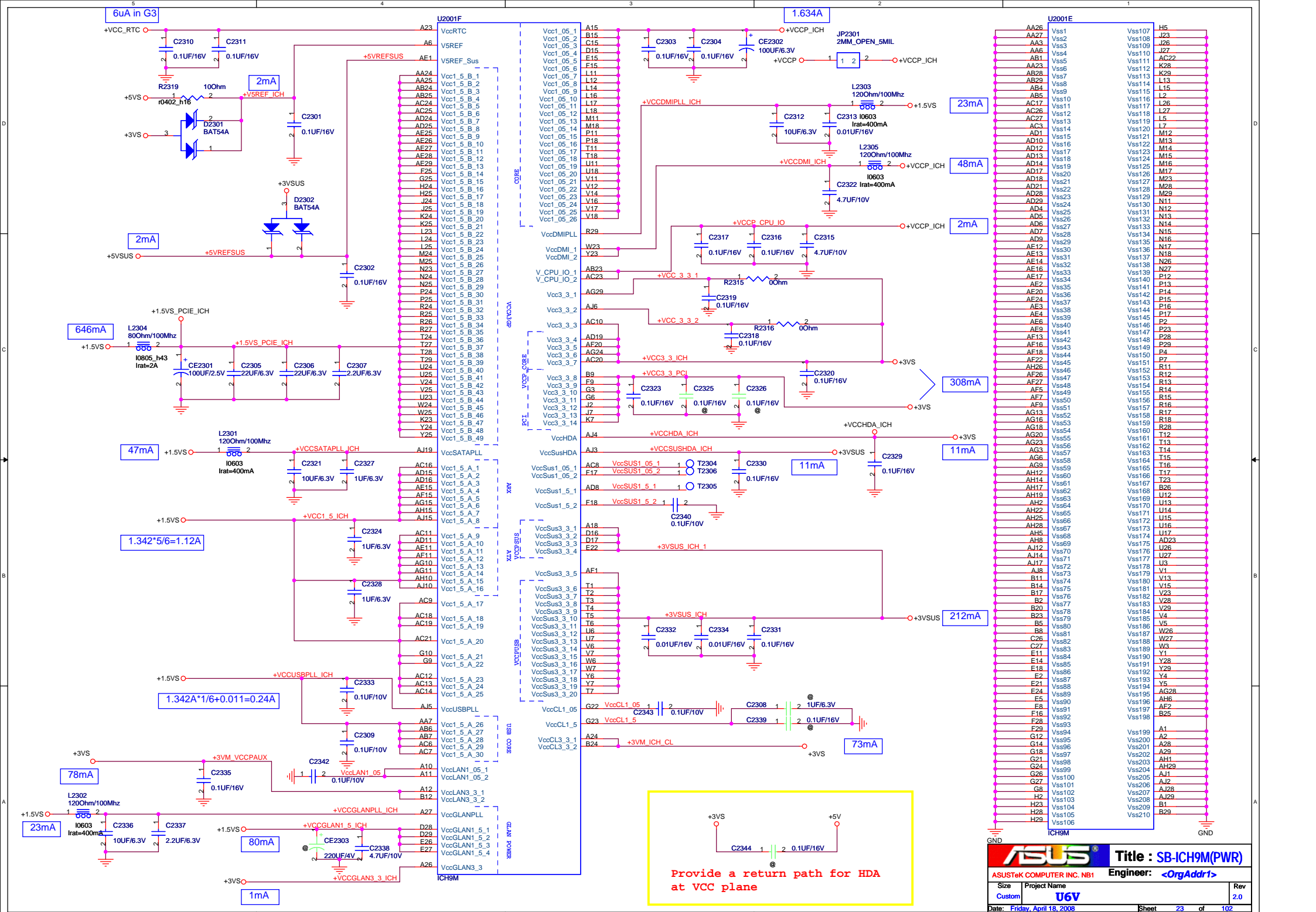


PCB\_ID1 => "0" for U6V  
PCB\_ID1 => "1" for VX3v

CL\_VREF0/1 ~ 0.405 V  
CL\_VREF [0:1] routing rules  
Width = 12 mils min  
Spacing = 12 mils min  
Break-out: 5 mils on 5 mils for 300 mils max

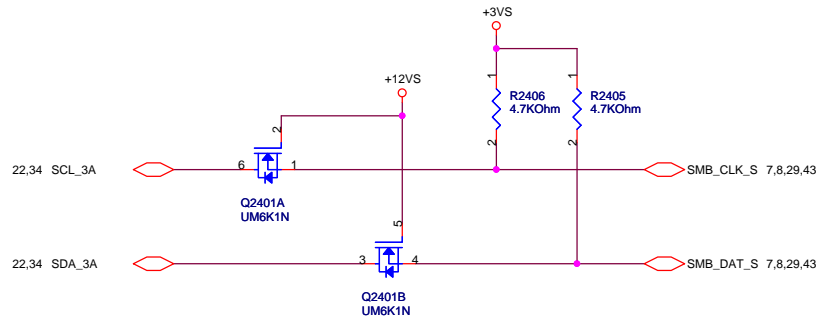
**ASUS** Title : SB-ICH9M(3)  
ASUSTek COMPUTER INC. NBI Engineer: <OrgAddr1>

Size	Project Name	Rev
Custom	<b>U6V</b>	2.0
Date: Wednesday, April 16, 2008	Sheet 22	of 102



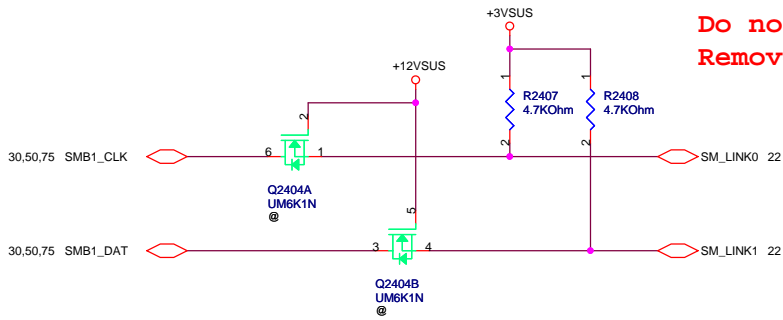
Provide a return path for HDA at VCC plane

# ICH9-M



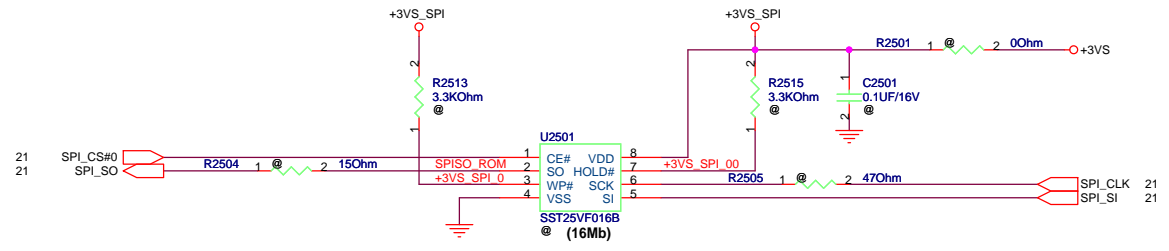
# EC-IT8752

**Do not support iAMT  
Remove ME-EC smbus**



Master	Slave
SCL_3A SDA_3A (ICH9M)	SMB_CLK_S → SO-DIMM0; SO-DIMM1; SMB_DAT_S → Debug; WLAN Card CLK Generator
SMB0_CLK SMB0_DAT (EC)	BATTERY
SMB1_CLK SMB1_DAT (EC)	Thermal Sensor





FOR iTPM  
8Mb 05G00120A010

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Title :

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
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Date: Tuesday, April 15, 2008

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Title :

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
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Date: Tuesday, April 15, 2008

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Title :

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size  
A

Project Name  
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Rev  
2.0

Date: Tuesday, April 15, 2008

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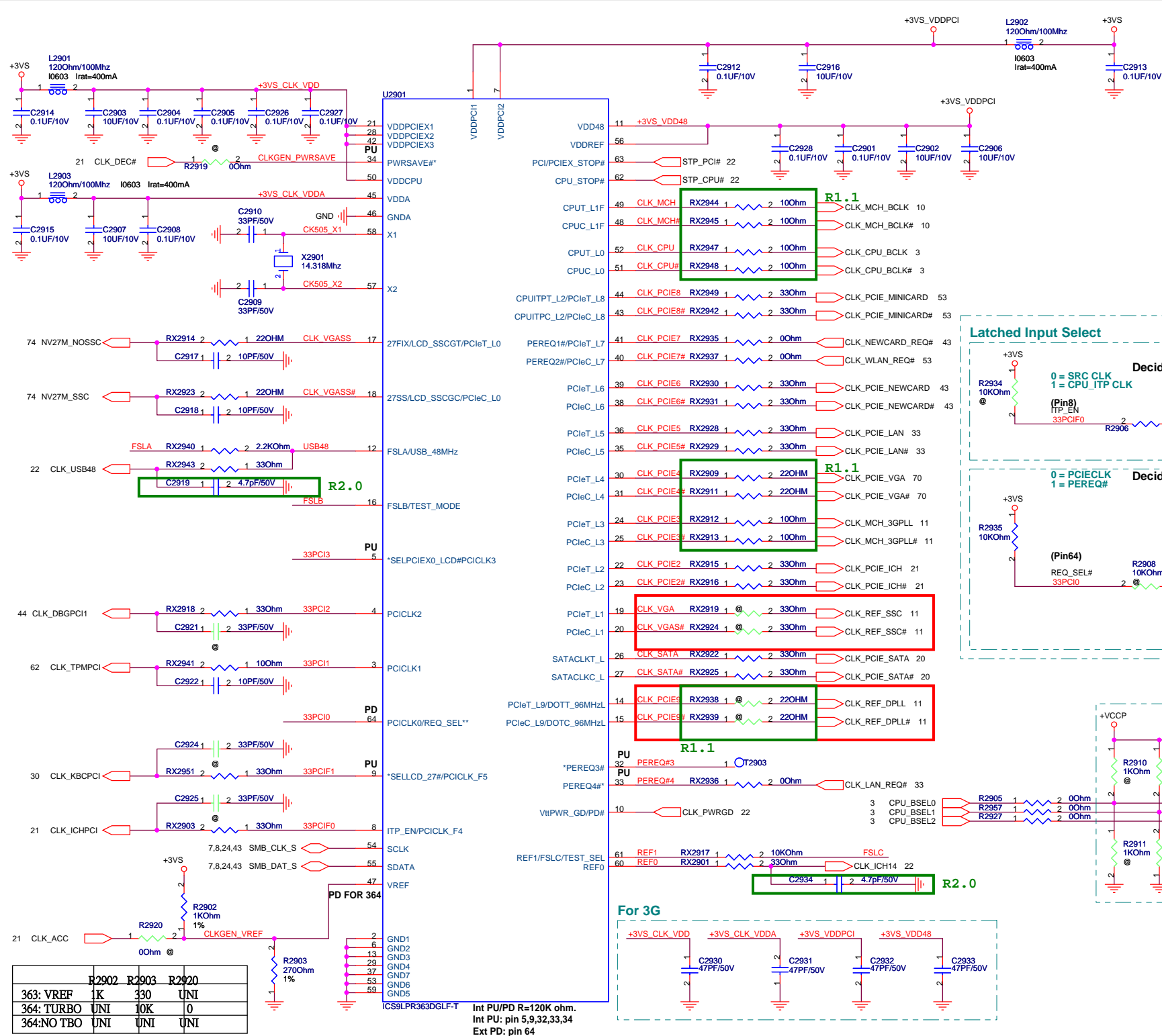
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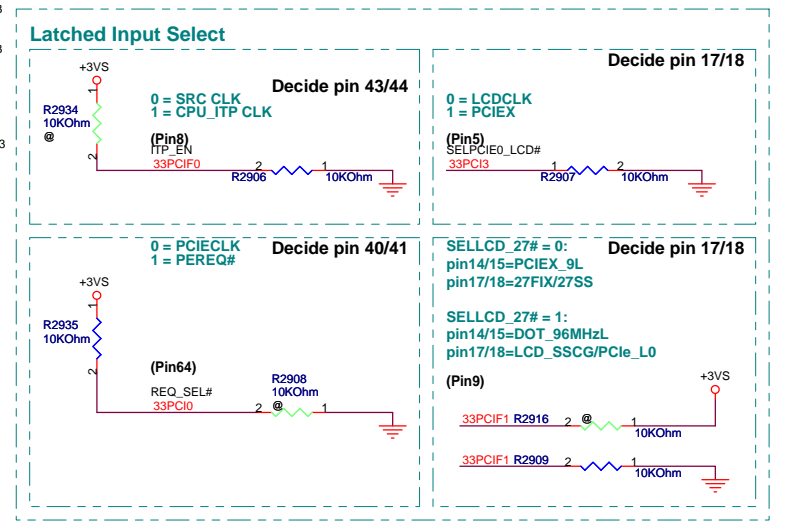
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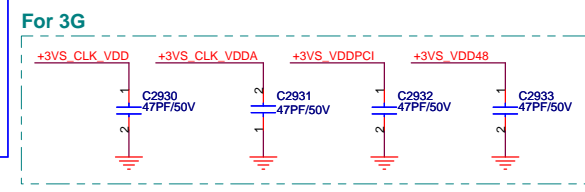
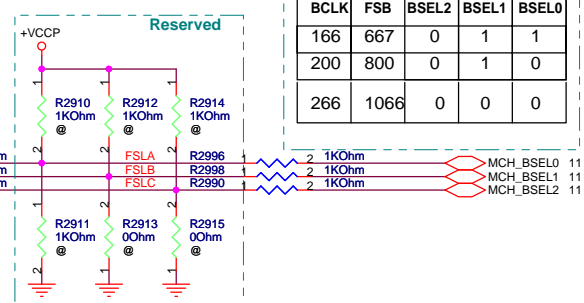


- PEREQ#1**  
0: Enable control SATACLK & PCIEX0 / 6 through I2C  
1: Disable SATACLK & PCIEX0 / 6 Controlled through I2C
- PEREQ#2**  
0: Enable control PCIE1 / 8 through I2C  
1: Disable PCIE1/8 Controlled through I2C
- PEREQ#3**  
0: Enable control PCIE4 / 2 through I2C  
1: Disable PCIE 4 / 2 Controlled through I2C
- PEREQ#4**  
0: Enable control PCIE7 / 5 / 3 through I2C  
1: Disable PCIE7 / 5 / 3 Controlled through I2C

Pin5	Pin9	Pin14/15	Pin17/18
SELPCIE0_LCD# FCI3 = 0 (low)	SELLCD_27# = 0 SELLCD_27# = 1	PCIE#9 DOT96	27FIWSS LCD
SELPCIE0_LCD# FCI3 = 1 (high)	SELLCD_27# = 0 SELLCD_27# = 1	PCIE#9 DOT96	PCIE#0 PCIE#0

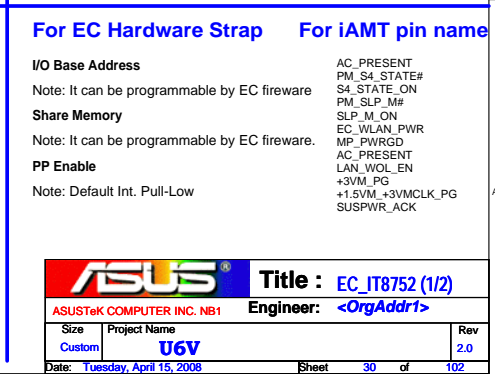
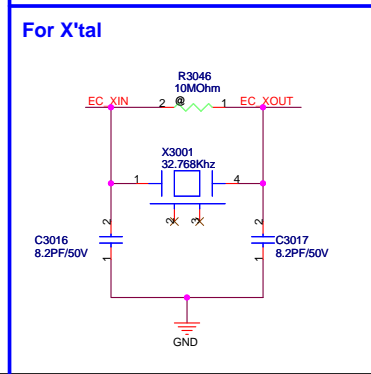
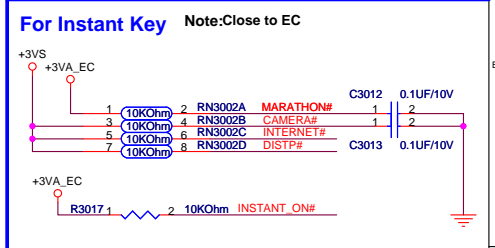
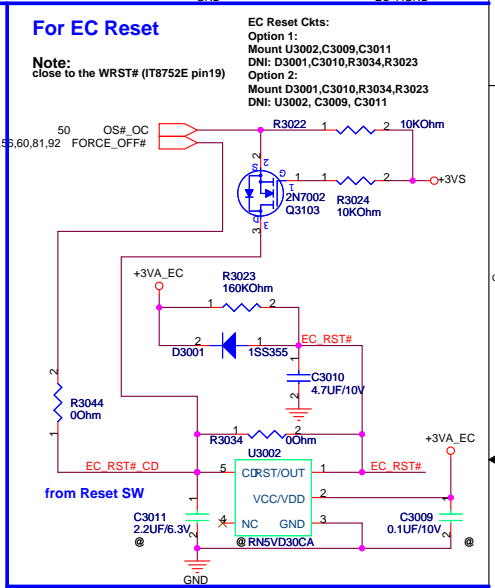
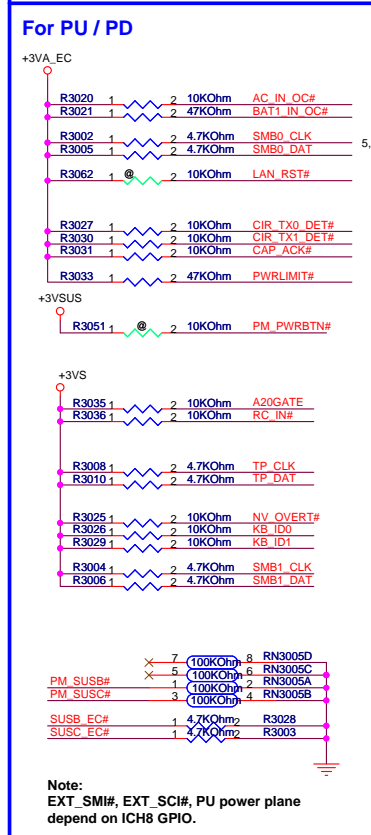
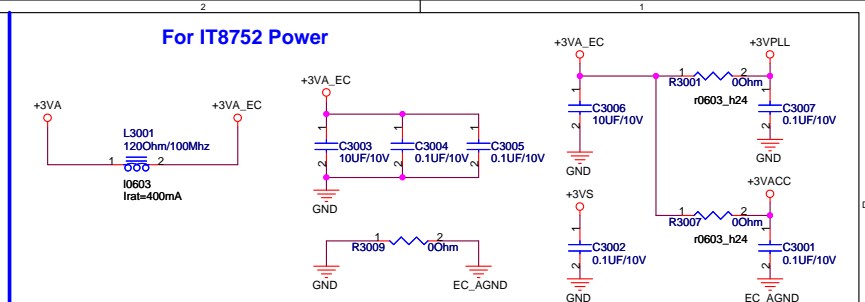
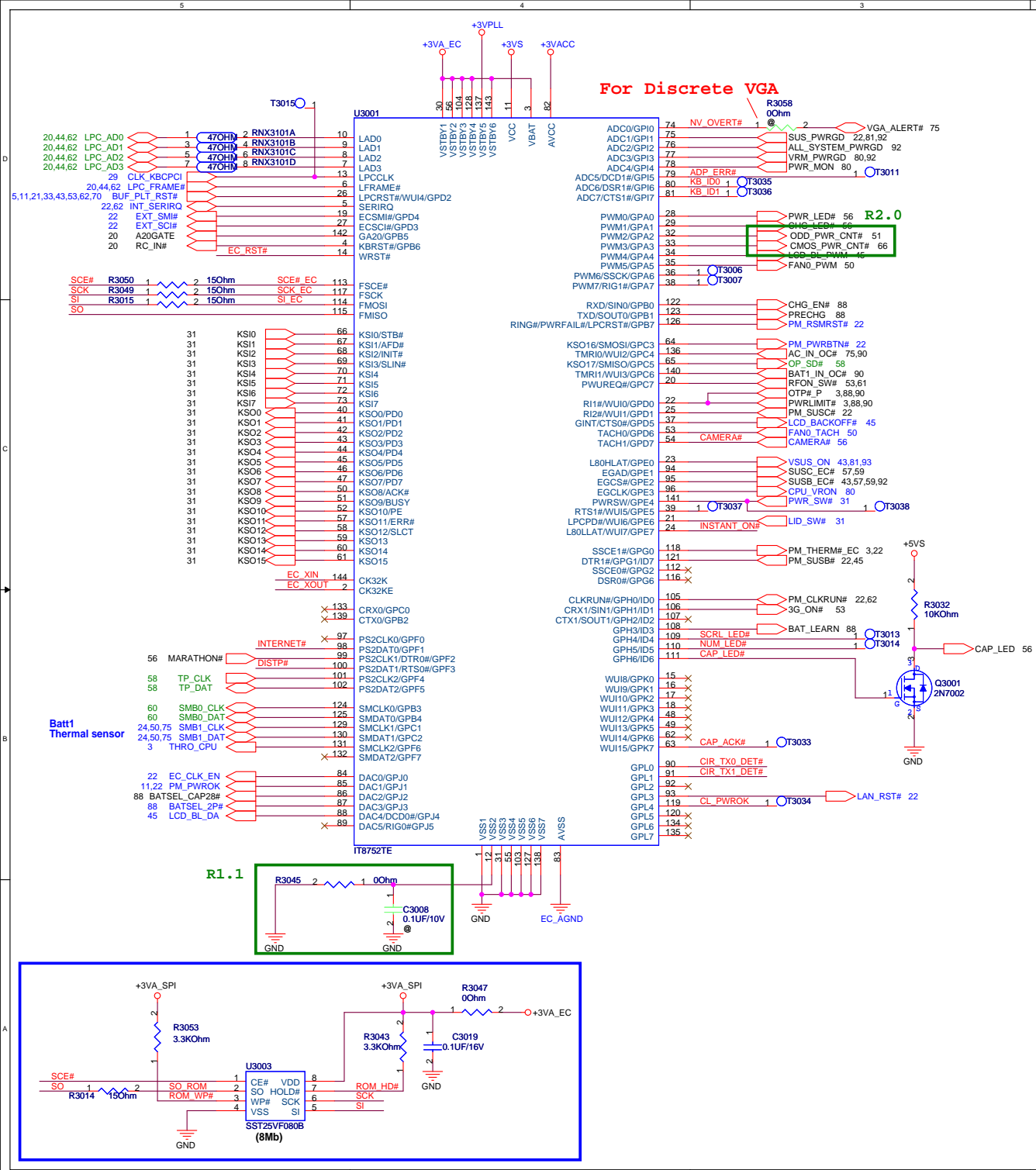


	FSLC	FSLB	FSLA	
BCLK	FSB	BSEL2	BSEL1	BSEL0
166	667	0	1	1
200	800	0	1	0
266	1066	0	0	0



	R2902	R2903	R2920
363: VREF	1K	330	UNI
364: TURBO	UNI	10K	0
364: NO TBO	UNI	UNI	UNI

Int PU/PD R=120K ohm.  
Int PU: pin 5,9,32,33,34  
Ext PD: pin 64



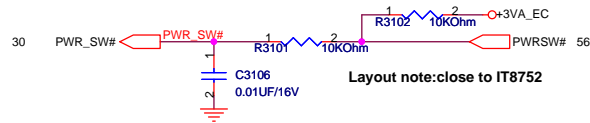
**For Battery**

**Note:** When plug in or out the battery, it may cause a spike to damage EC and gas gauge. It needs to add varistors to protect those pins.

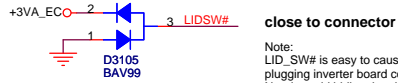
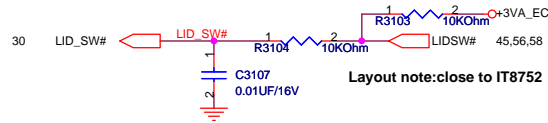
In Page 60

**For Switch**

**PWR SWITCH**

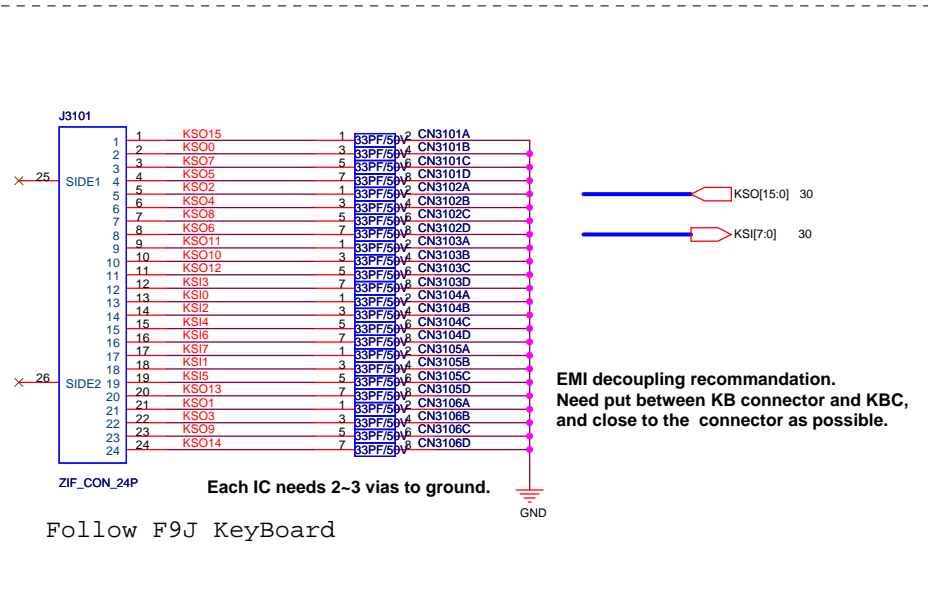


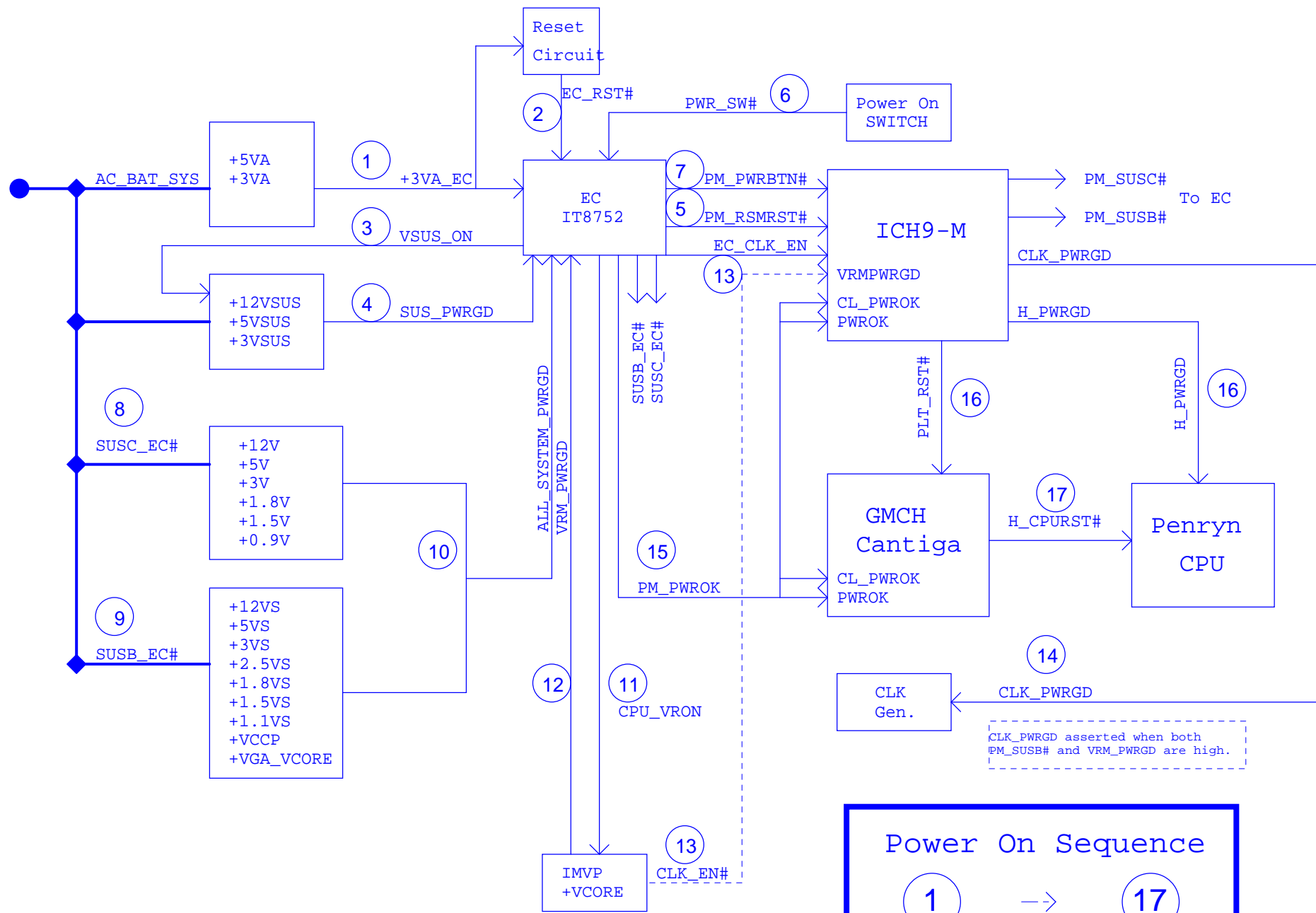
**LID SWITCH**



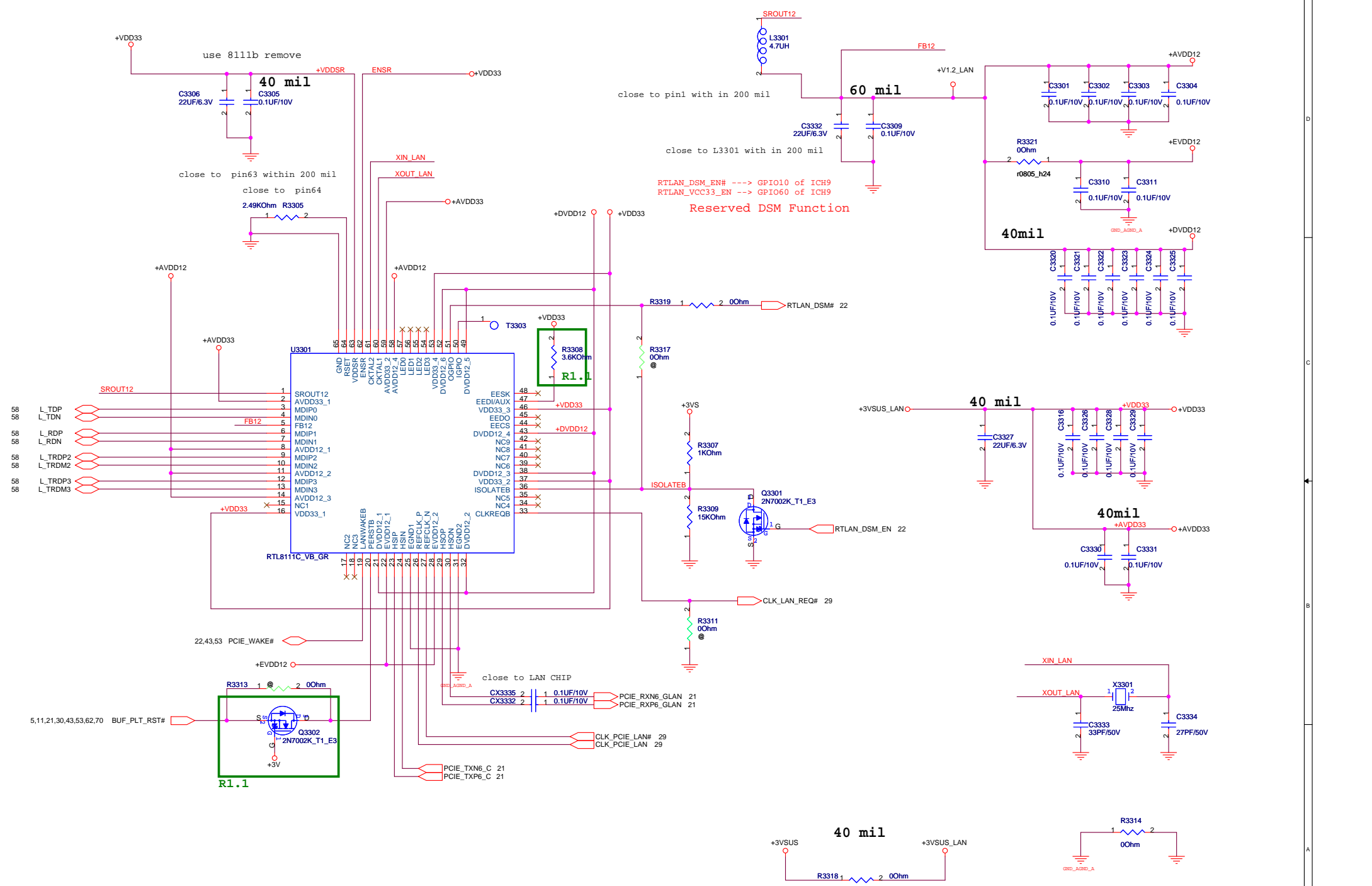
Note:  
LID\_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present. Need to add bidirectional diode to protect this pin.

**Keyboard Connector**

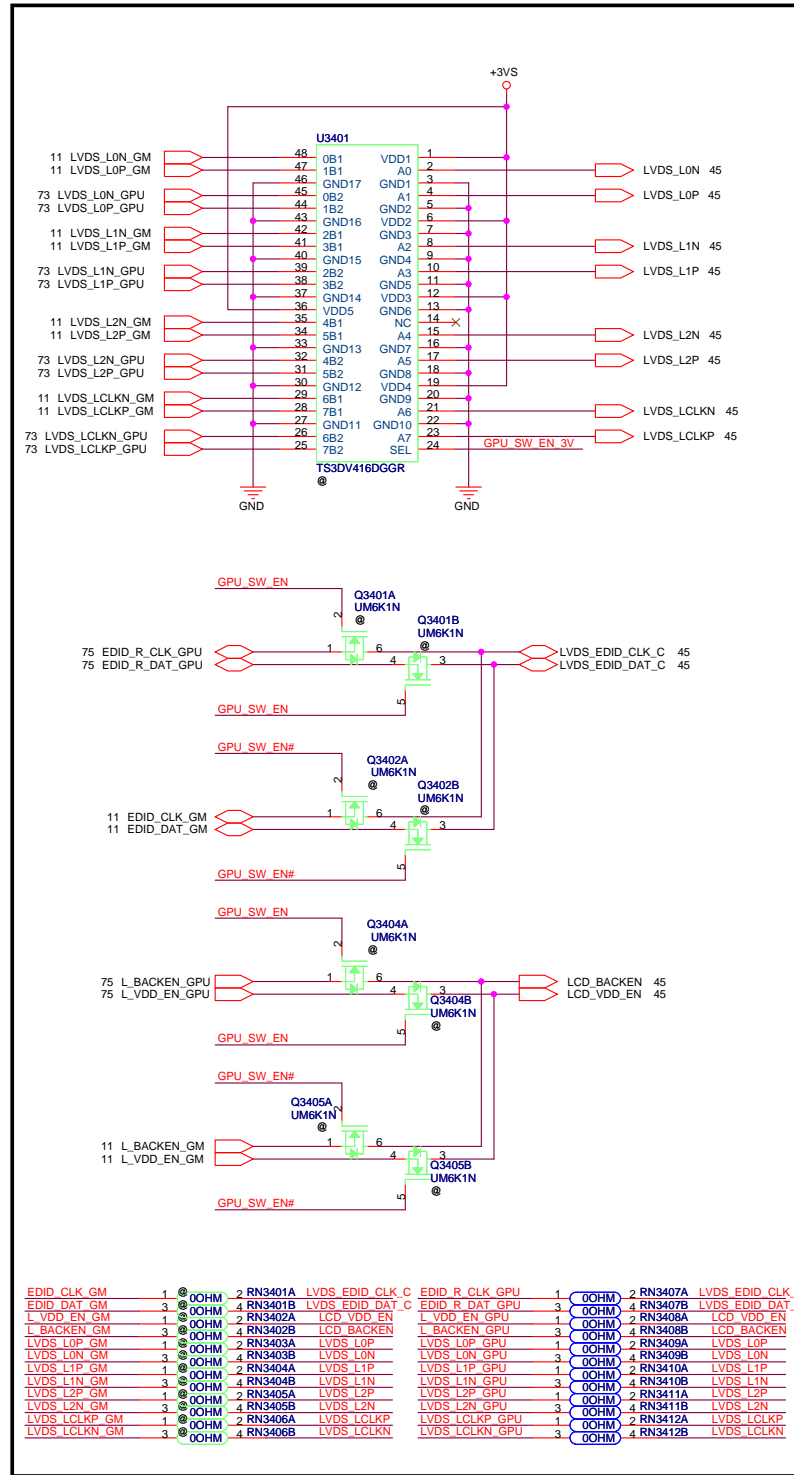




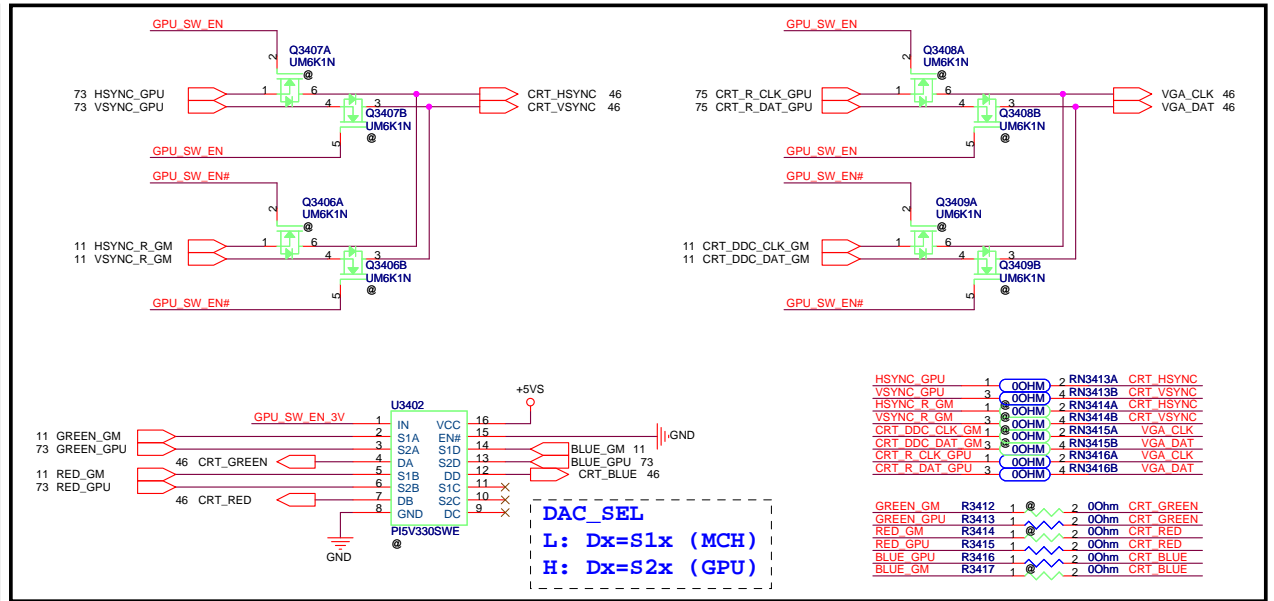




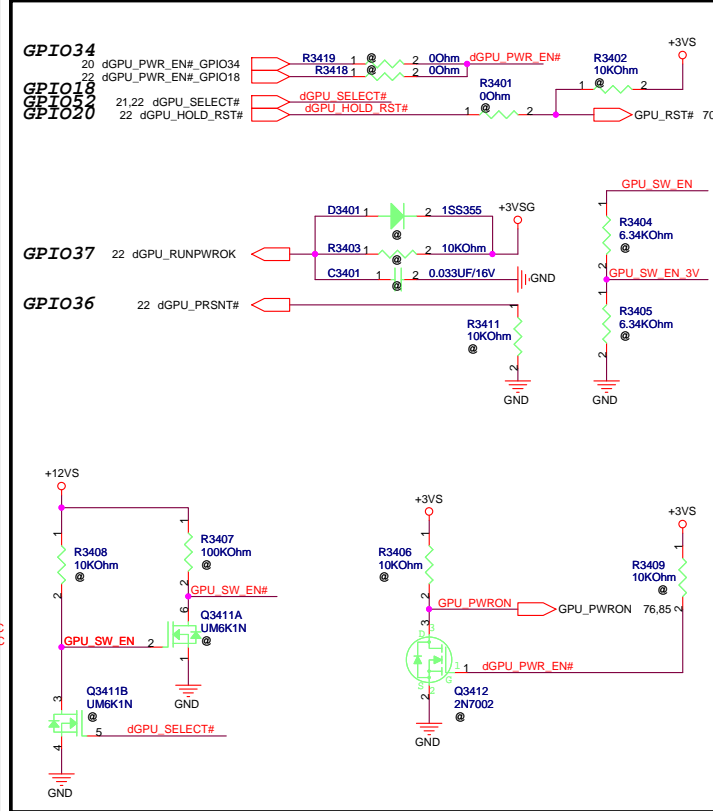
# LVDS Switch



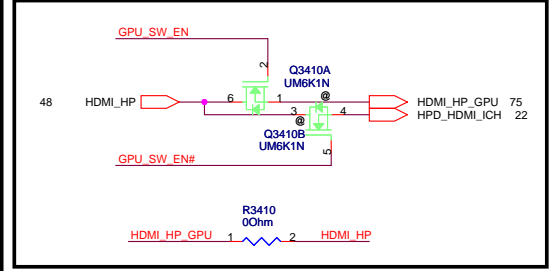
# CRT Switch



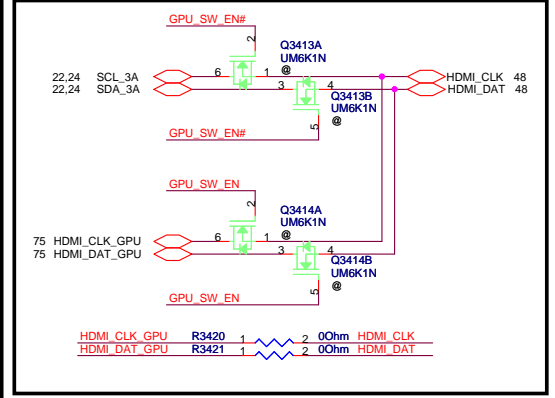
# Control Signal from ICH9M



# HDMI Hot-Plug Detect Switch



# HDMI I2C Switch



**ASUS** Title : Hybrid Switch  
 ASUSTeK COMPUTER INC. NB1 Engineer: <OrgAddr>  
 Size Project Name  
 Custom U6V  
 Date: Tuesday, April 22, 2008 Sheet 34 of 102  
 Rev 2.0

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		<b>Title :</b>	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> <OrgAddr1>	
Size	Project Name		Rev
Custom	<b>U6V</b>		2.0
Date: Tuesday, April 15, 2008		Sheet	35 of 102

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		<b>Title :</b>	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> <OrgAddr1>	
Size	Project Name		Rev
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		<b>Title :</b>	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> <OrgAddr1>	
Size	Project Name		Rev
Custom	<b>U6V</b>		2.0
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		<b>Title :</b>	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> <OrgAddr1>	
Size	Project Name		Rev
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**Title : DSP**

ASUSTeK COMPUTER INC. NB1

**Engineer: <OrgAddr1>**

Size	Project Name	Rev
A	<b>U6V</b>	2.0

Date: **Tuesday, April 15, 2008**

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		<b>Title :CARDBUS R5C833 (1)</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	<b>U6V</b>		2.0
Date: Tuesday, April 15, 2008		Sheet	40 of 102





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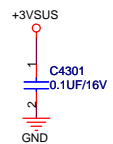
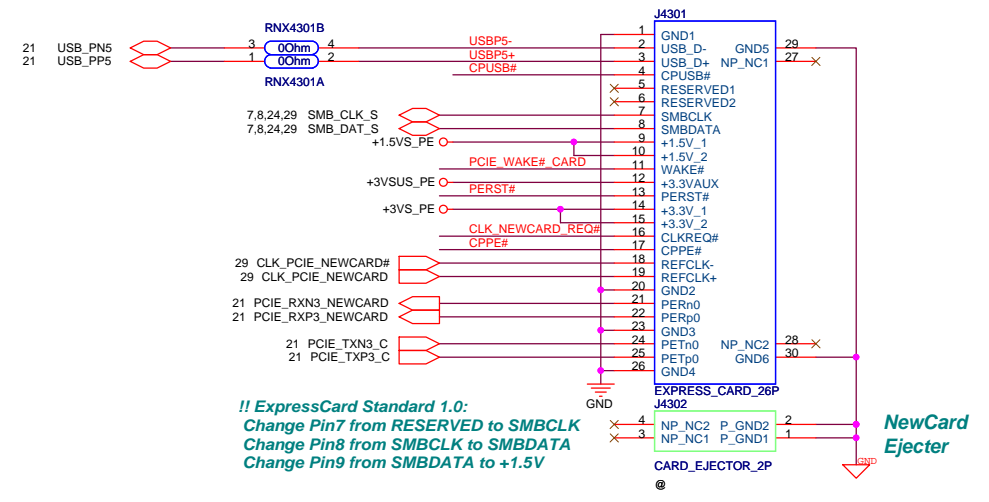
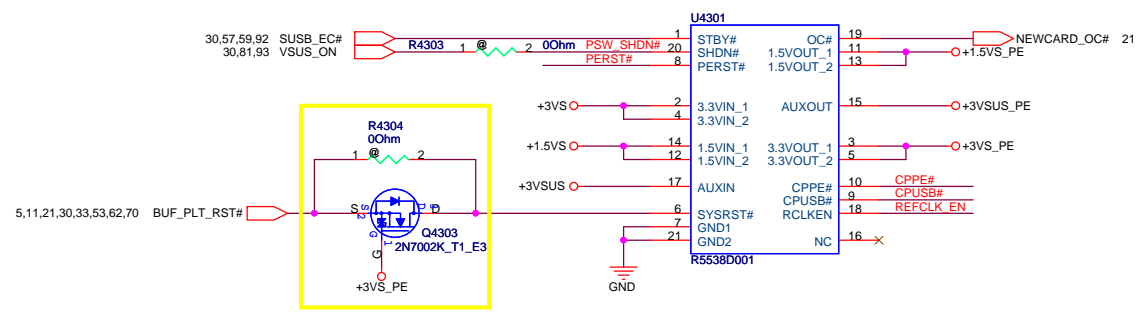
A

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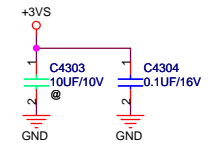
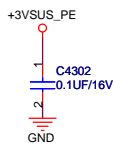
		<b>Title :</b> CARDBUS R5C833 (2)	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> <OrgAddr1>	
Size	Project Name		Rev
Custom	<b>U6V</b>		2.0
Date: Tuesday, April 15, 2008		Sheet	41 of 102



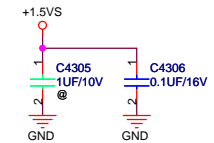
		<b>Title :</b> 1394&CardReader CON	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> <Engineer Name>	
Size	Project Name		Rev
Custom	<b>U6V</b>		2.0
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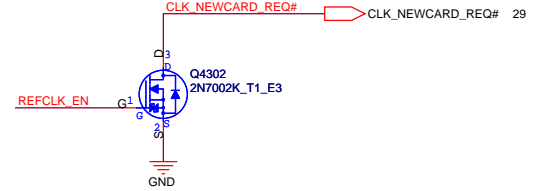
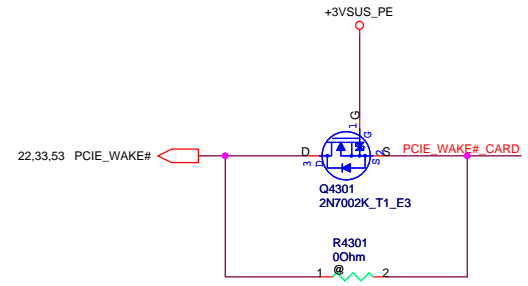
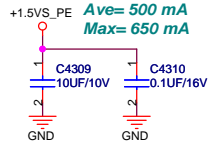
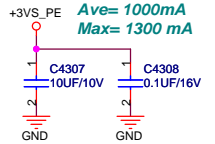
3.0V-3.6V  
Ave= 200mA  
Max= 275 mA



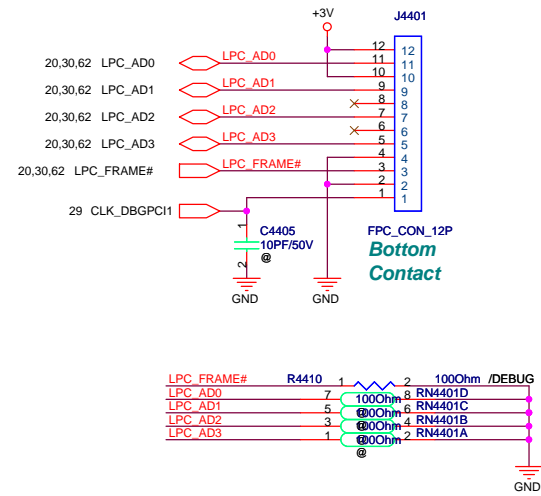
3.0V-3.6V  
Ave= 1000mA  
Max= 1300 mA



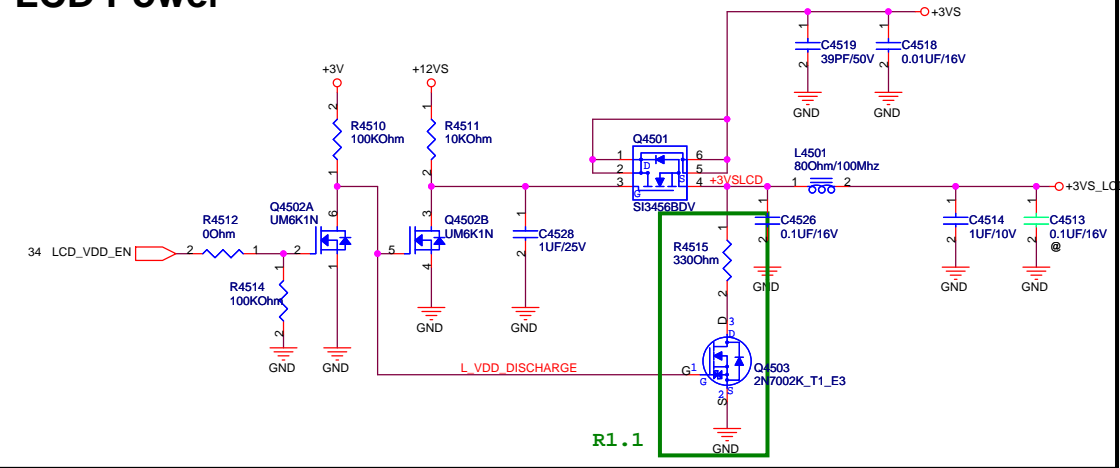
1.35V-1.65V  
Ave= 500 mA  
Max= 650 mA



# LPC DEBUG PORT

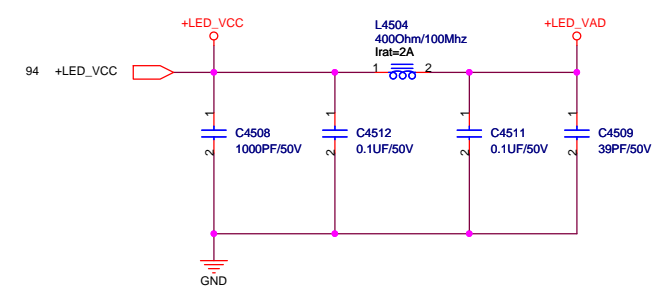
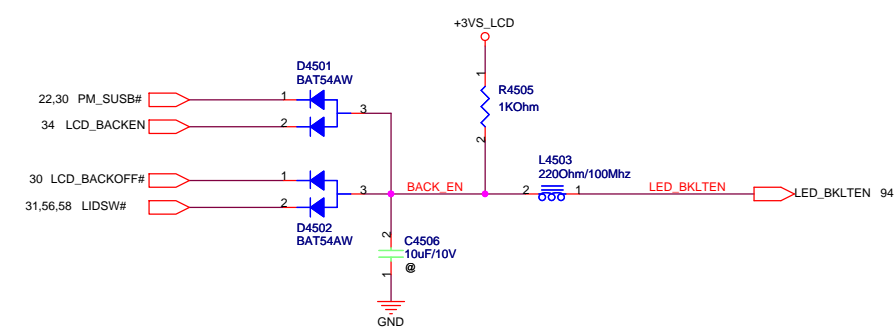
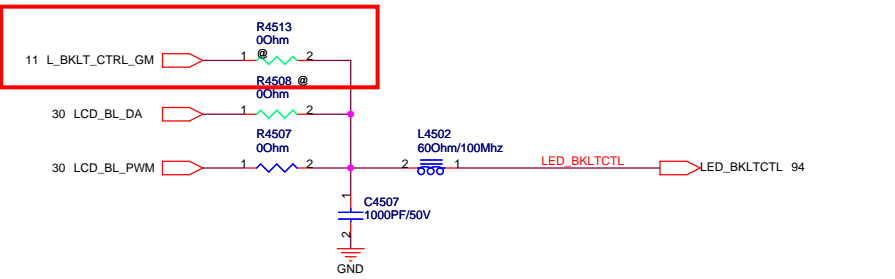
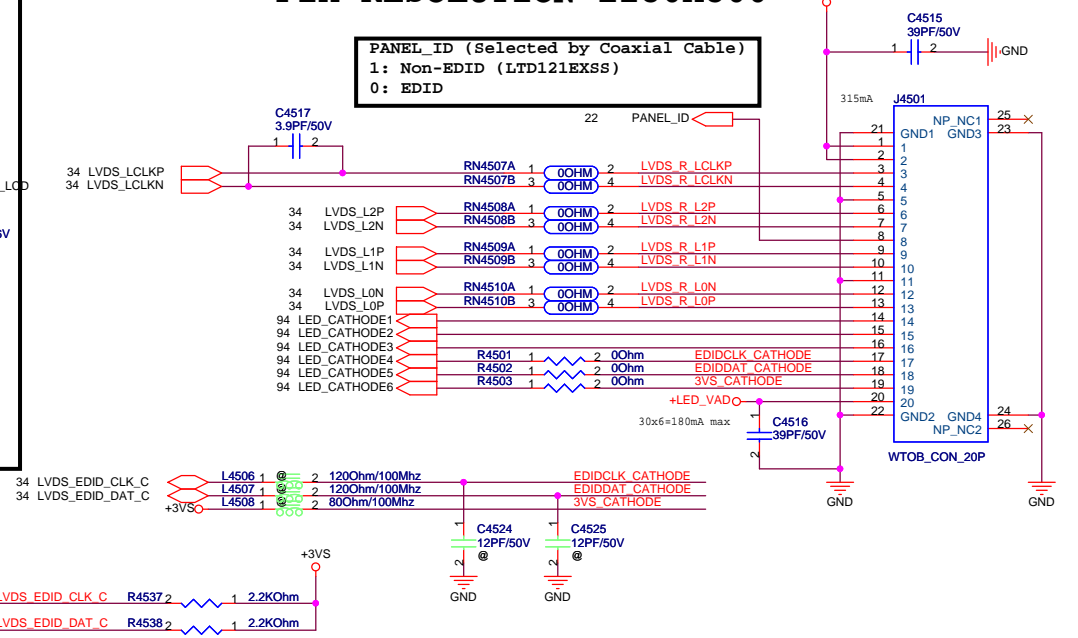


# LCD Power

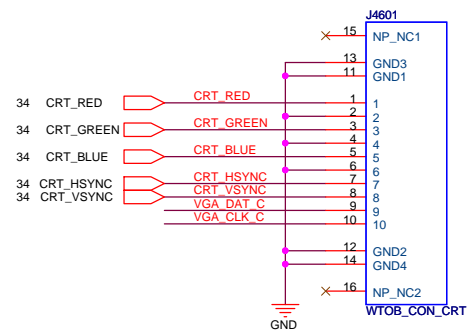


# FIX RESOLUTION 1280x800

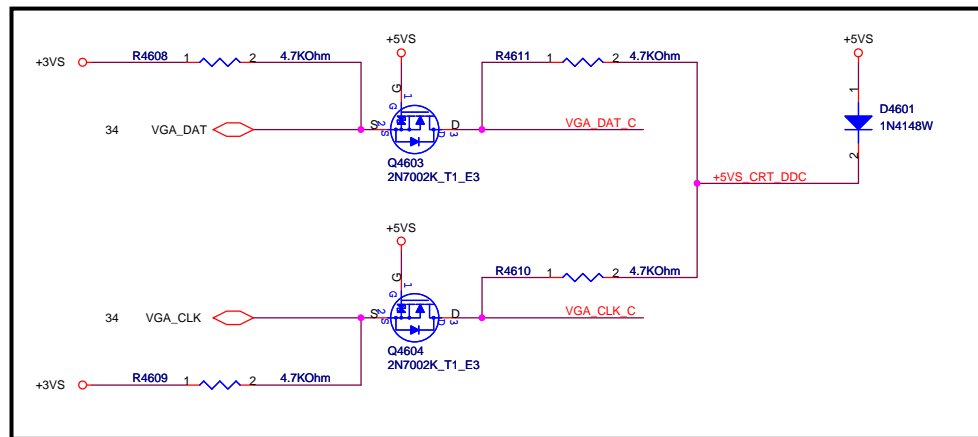
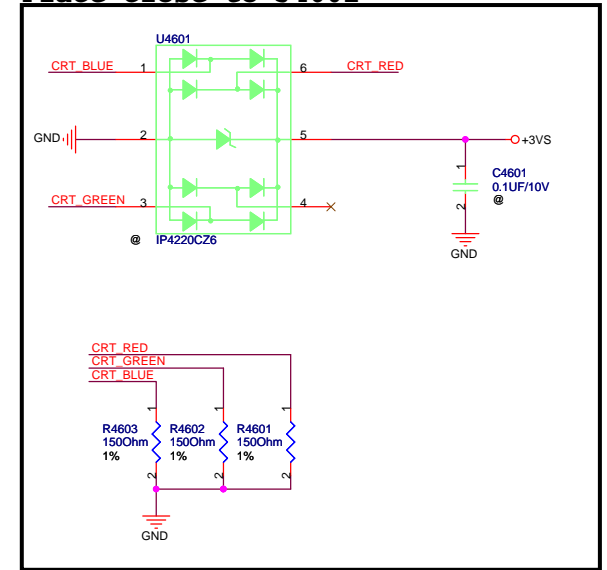
PANEL\_ID (Selected by Coaxial Cable)  
 1: Non-EDID (LTD121EXSS)  
 0: EDID



**7S6P LED PANEL**  
**+LED\_VCC=3.3Vx7=23.1V**  
**I=20mAx6=0.12A**



Place close to J4601



5

4

3

2

1

D

D

C

C

B

B

A

A



**Title :** Cantiga-POWER(5)

ASUSTeK COMPUTER INC. NB1

**Engineer:** <OrgAddr1>

Size	Project Name	Rev
A	U6V	2.0

Date: Tuesday, April 15, 2008

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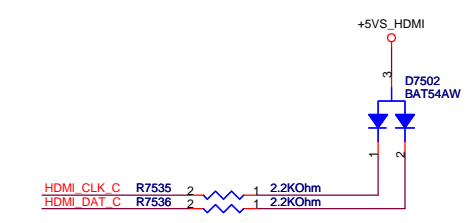
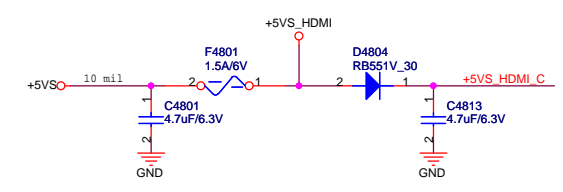
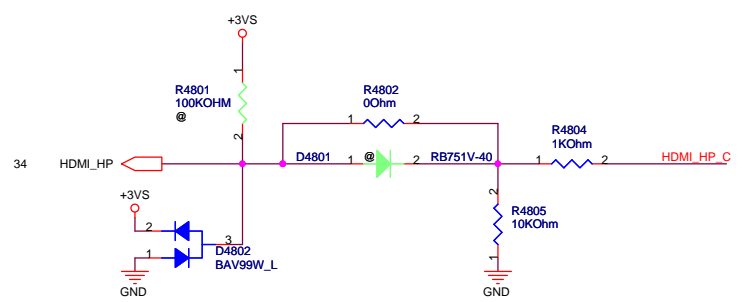
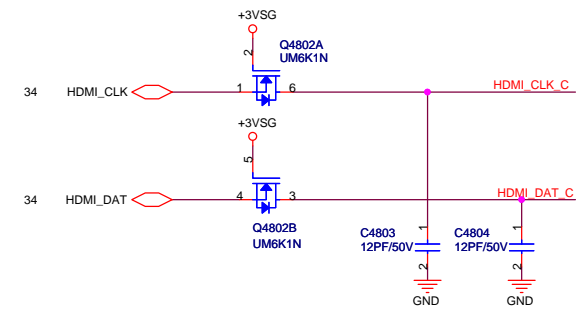
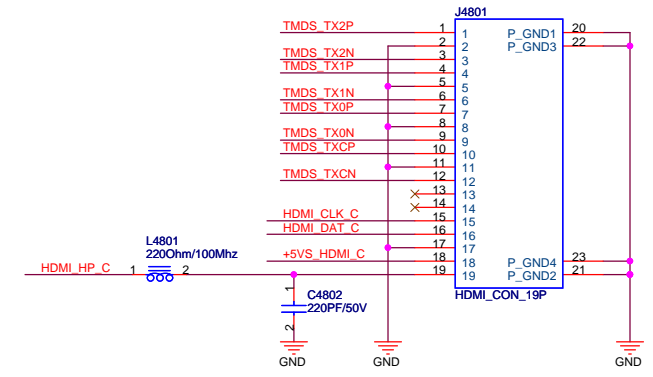
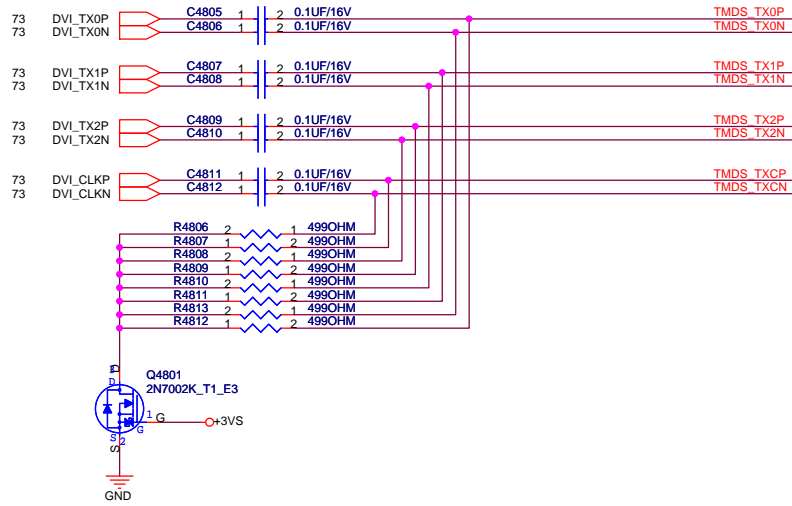
5

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**Title :** Cantiga-POWER(5)

ASUSTeK COMPUTER INC. NB1

**Engineer:** <OrgAddr1>

Size	Project Name	Rev
A	U6V	2.0

Date: Tuesday, April 15, 2008

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5

4

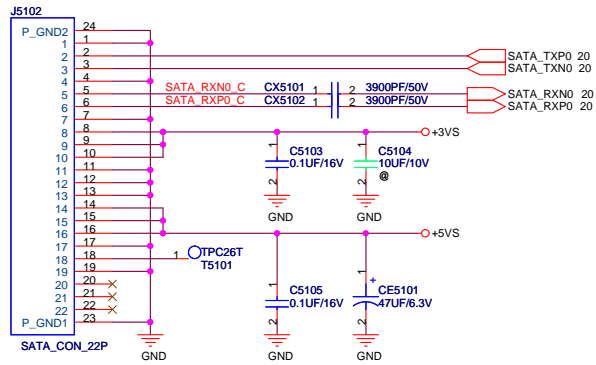
3

2

1

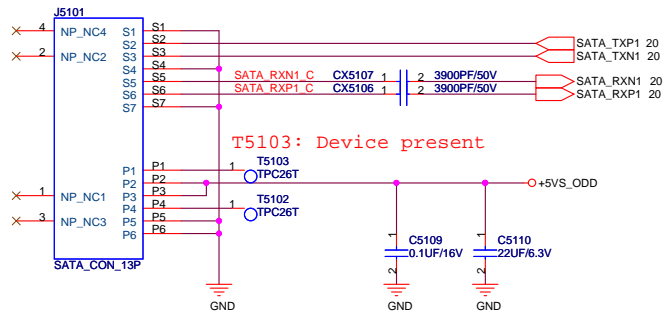


# SATA HDD

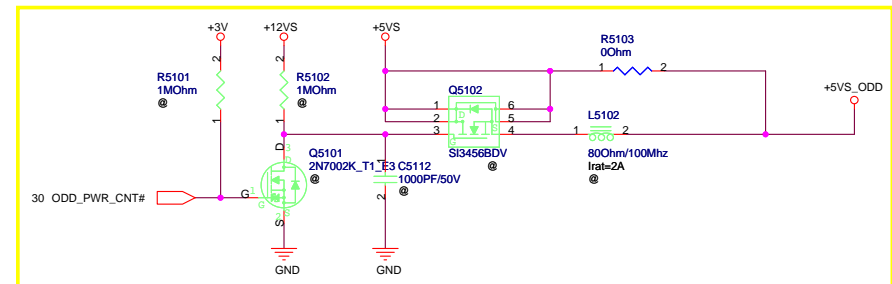


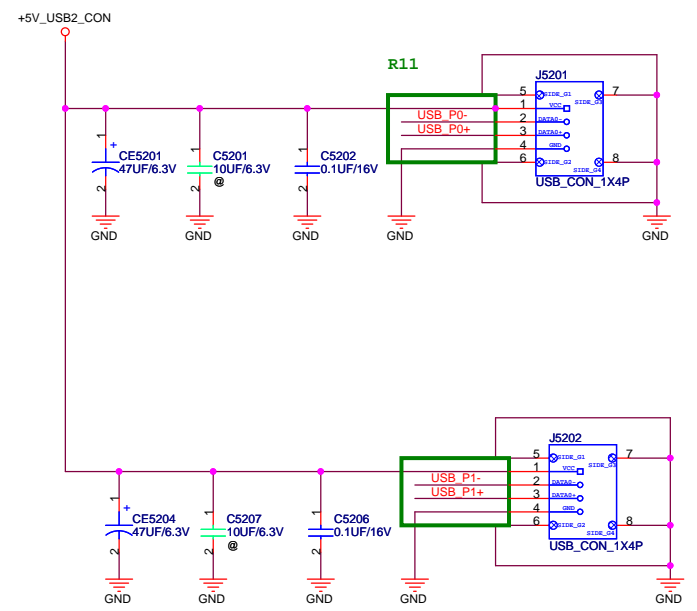
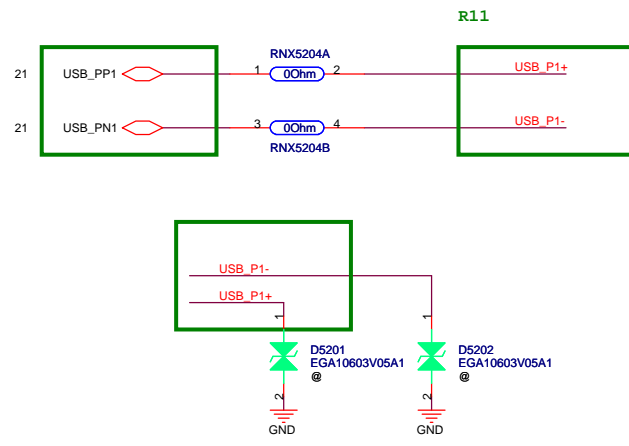
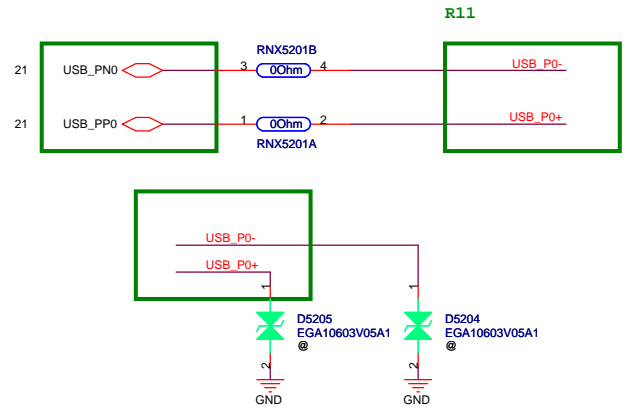
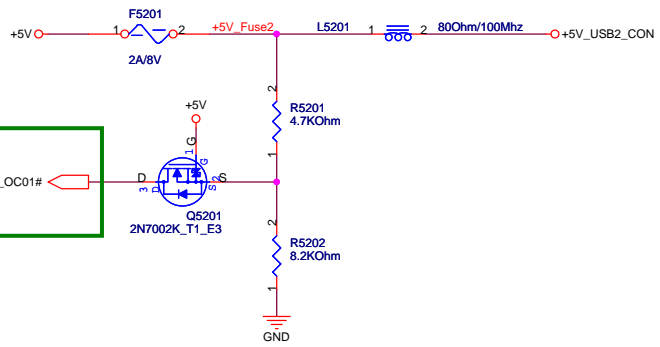
# ODD

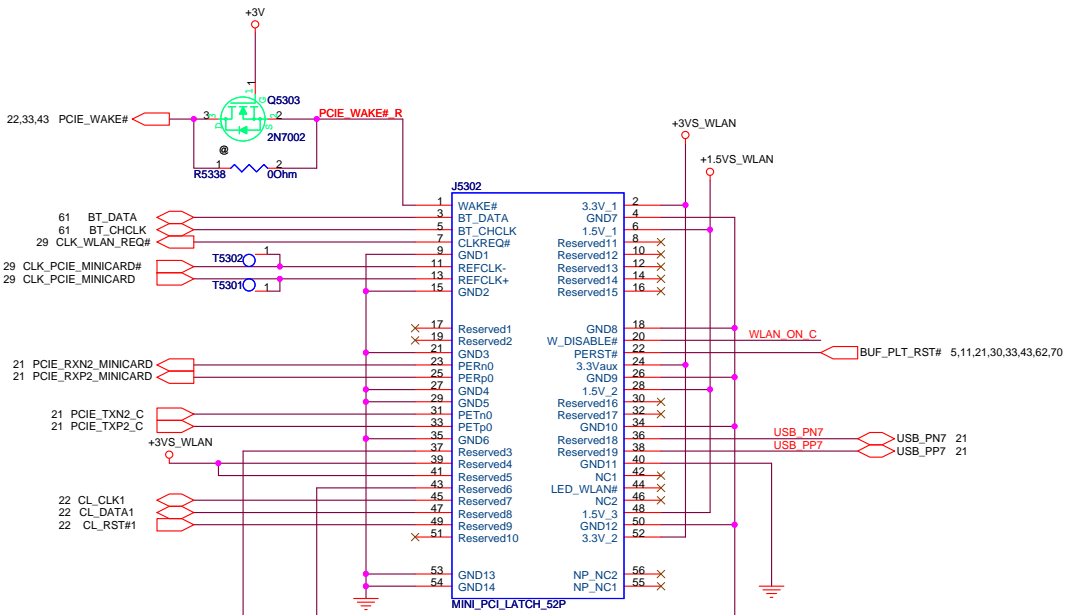
CHANGE NEW PART NUMBER



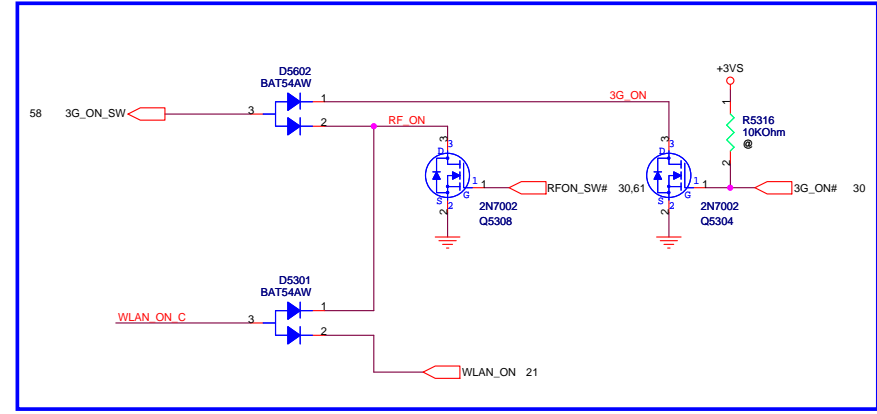
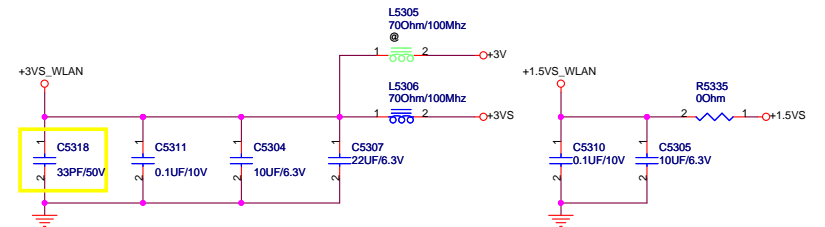
R2.0







Shirley Peak(Shiloh) /  
Echo Peak(Ebron)



	5	4	3	2	1
D					
C					
B					
A					



**Title : Port Docking**

ASUSTeK COMPUTER INC. NB1

**Engineer: <OrgAddr1>**

Size	Project Name	Rev
A	<b>U6V</b>	2.0

Date: **Tuesday, April 15, 2008** Sheet **54** of **102**

	5	4	3	2	1
D					
C					
B					
A					

A

B

C

D

E

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		<b>Title : Super I/O &amp; FIR</b>
ASUSTeK COMPUTER INC. NB1		<b>Engineer: &lt;OrgAddr1&gt;</b>
Size A	Project Name <b>U6V</b>	Rev 2.0
Date: <b>Tuesday, April 15, 2008</b>		Sheet <b>55</b> of <b>102</b>

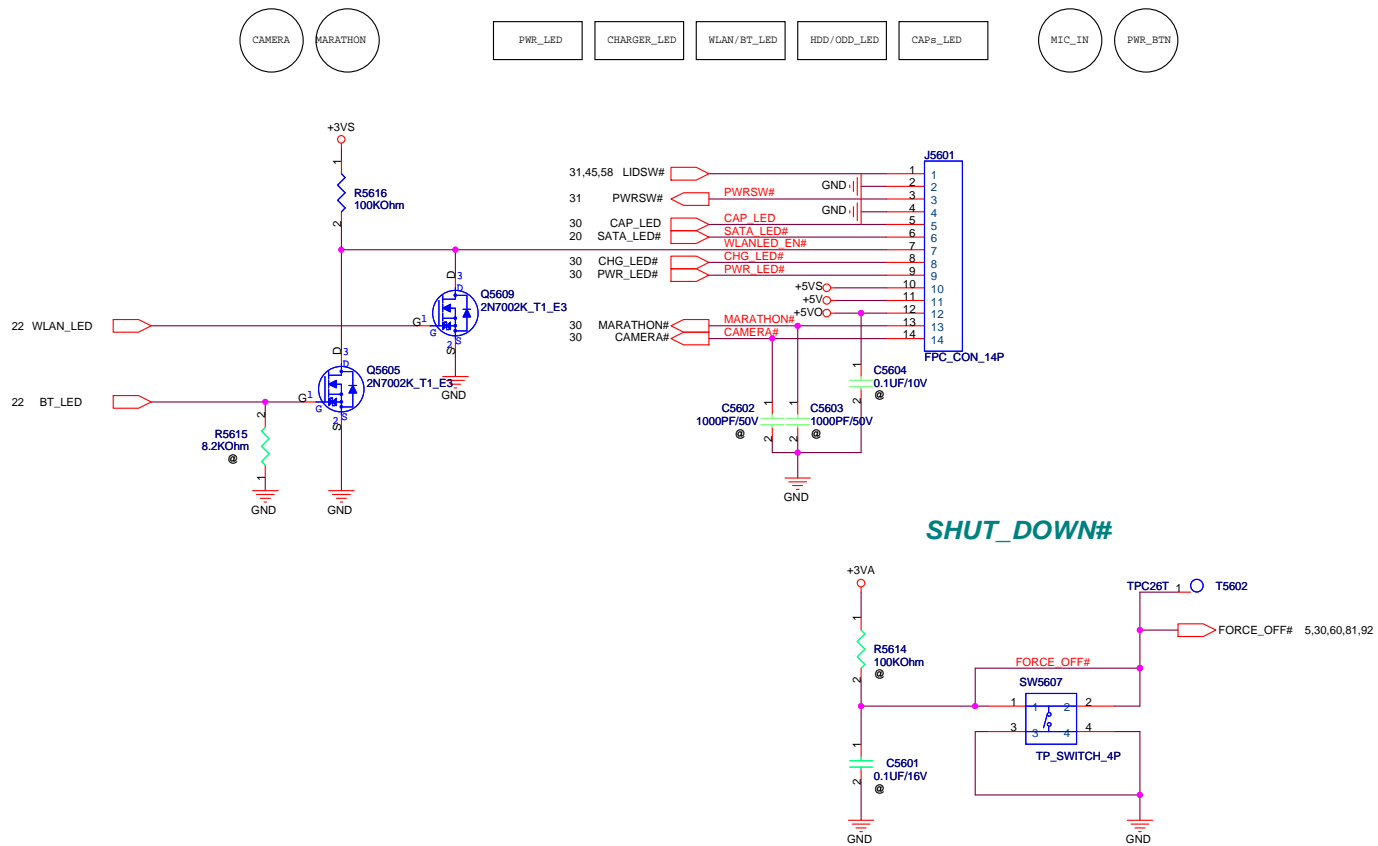
A

B

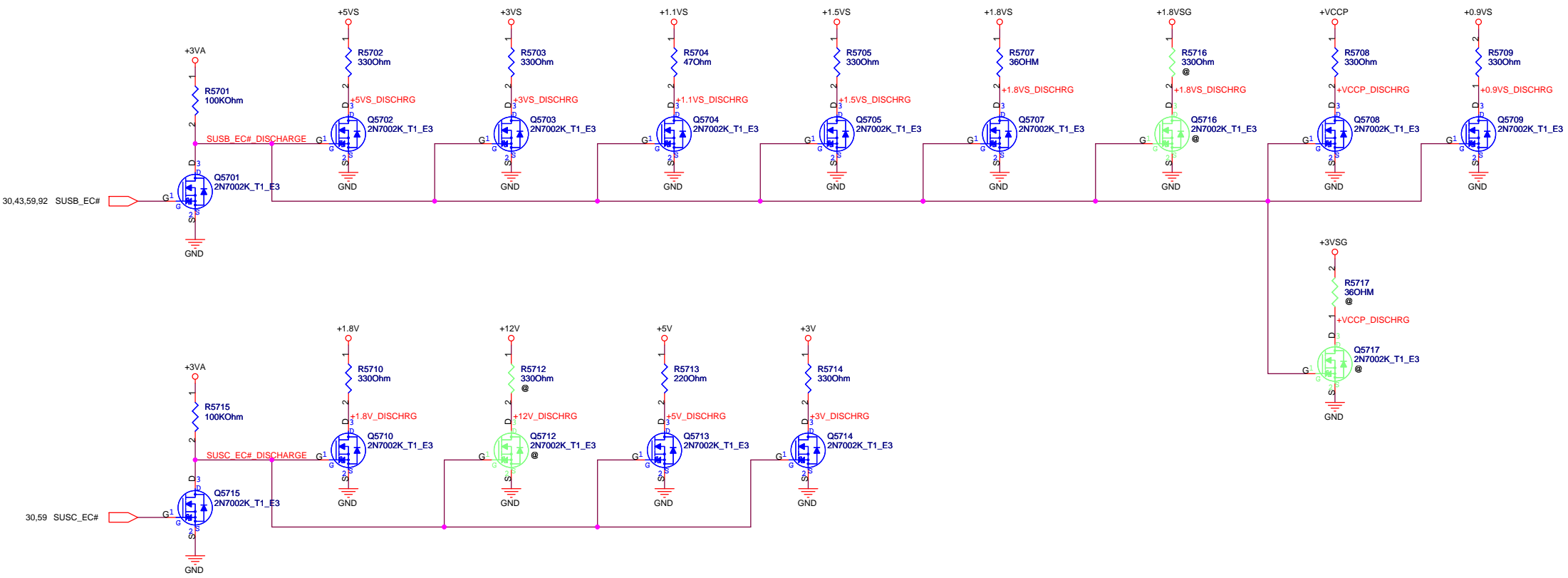
C

D

E

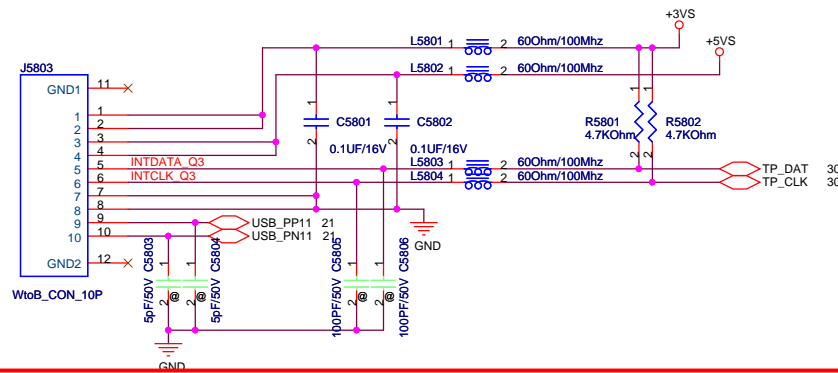




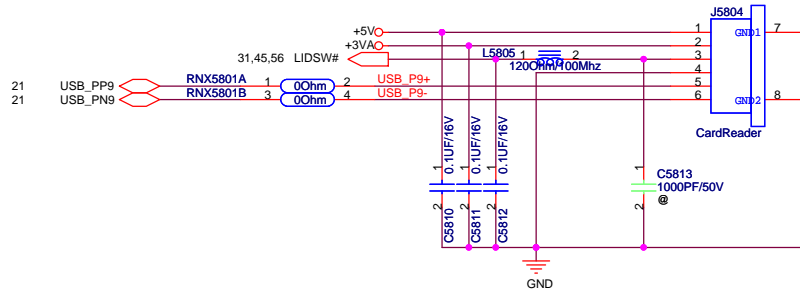


# SUBSYS CONN

## Touch Pad Connector & Finger Printer

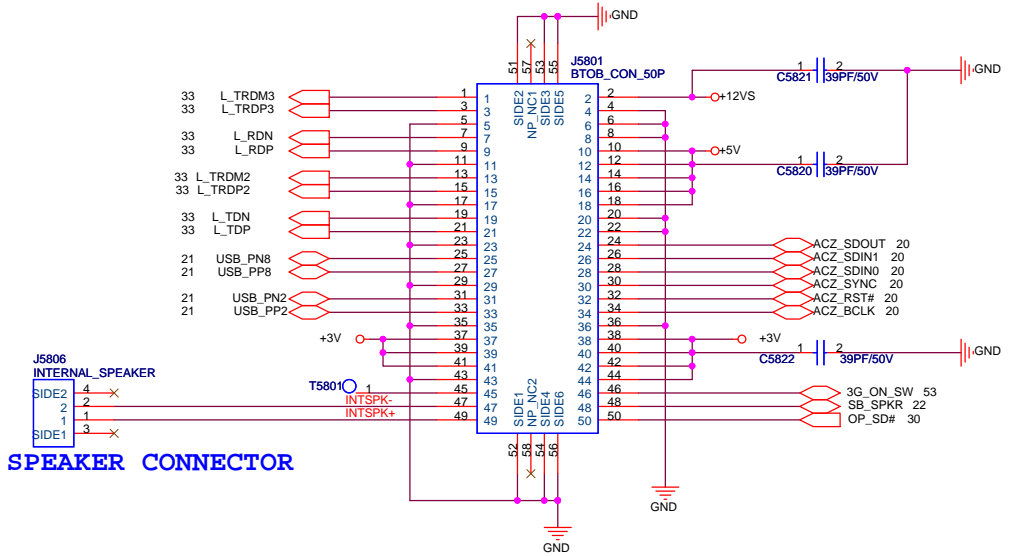


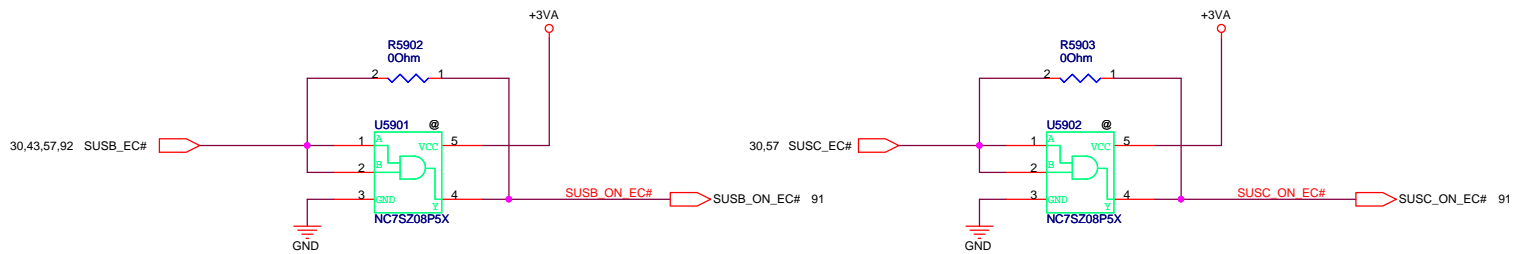
## Card Reader Connector & Lid Switch



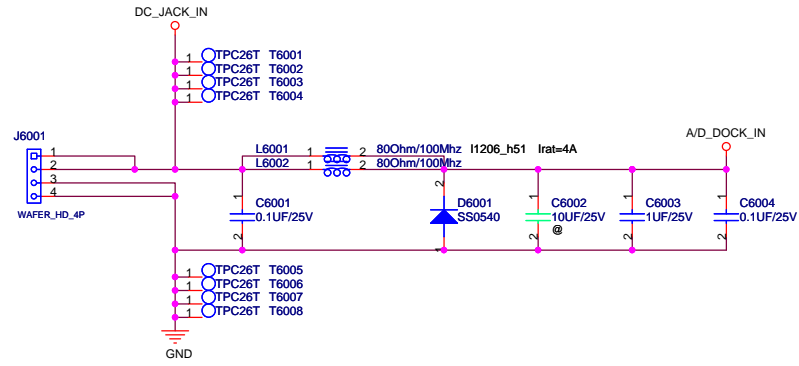
R20

## Audio Chip & 3G Card & GigaLAN & USB Connector

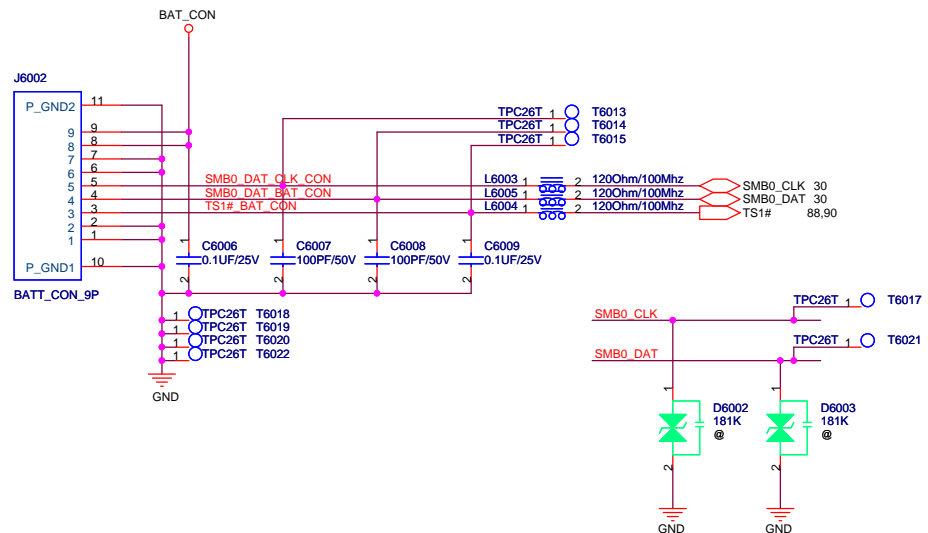




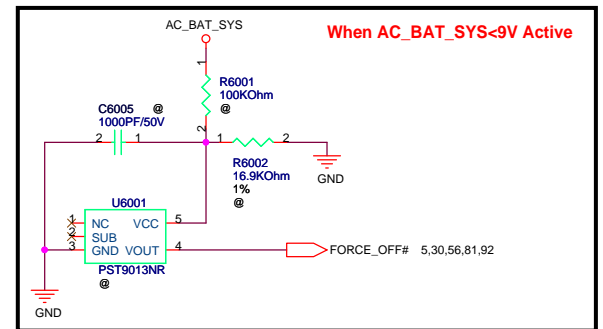
# DC IN



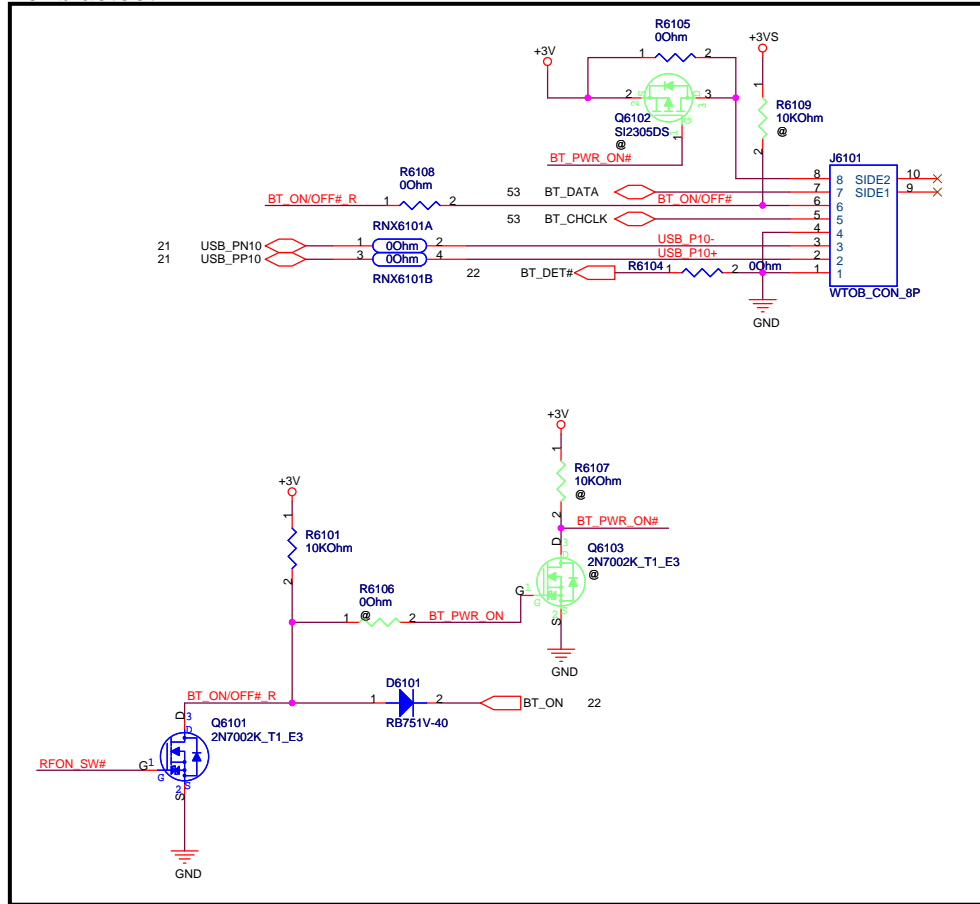
# BAT IN



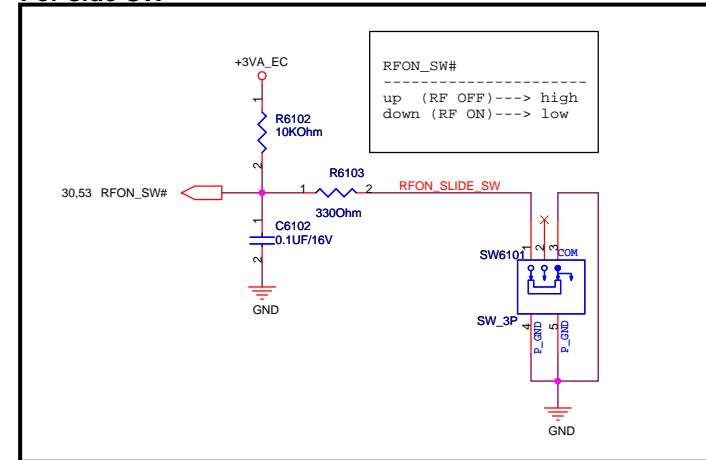
## Without Battery & Pull out Adapter



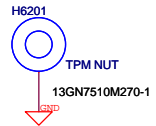
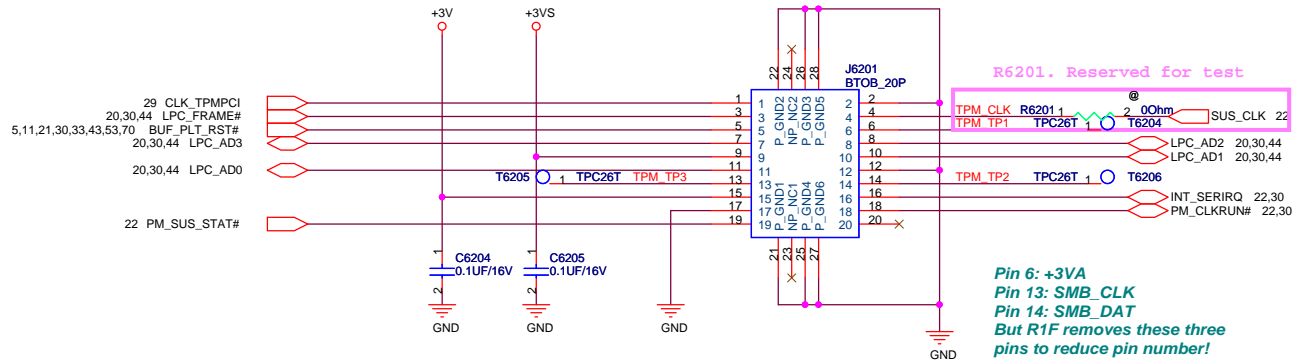
For bluetooth



For side SW



For TPM module



5

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3

2

1

D

D

C

C

B

B

A

A

		<b>Title :</b>	
ASUSTeK COMPUTER INC. NB1		<b>Engineer:</b> <OrgAddr1>	
Size	Project Name	Rev	
Custom	<b>U6V</b>	2.0	
Date: Tuesday, April 15, 2008		Sheet	63 of 102

	5	4	3	2	1
D					
C					
B					
A					



**Title :** TUN

ASUSTeK COMPUTER INC. NB1

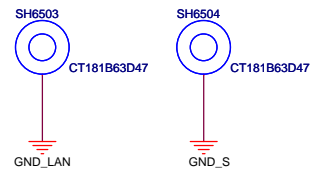
**Engineer:** <OrgAddr1>

Size	Project Name	Rev
A	U6V	2.0

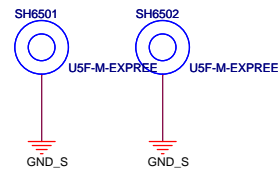
Date: Tuesday, April 15, 2008 Sheet 64 of 102



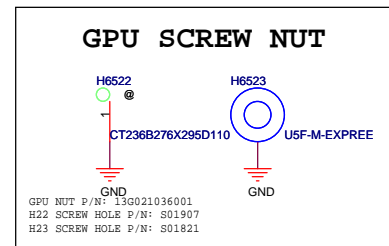
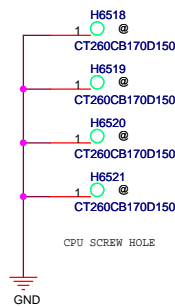
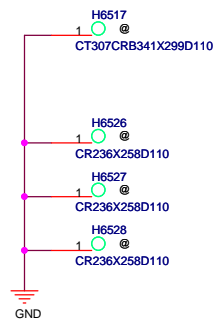
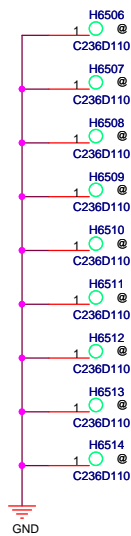
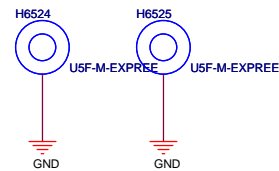
**FOR MDC (TOP)**



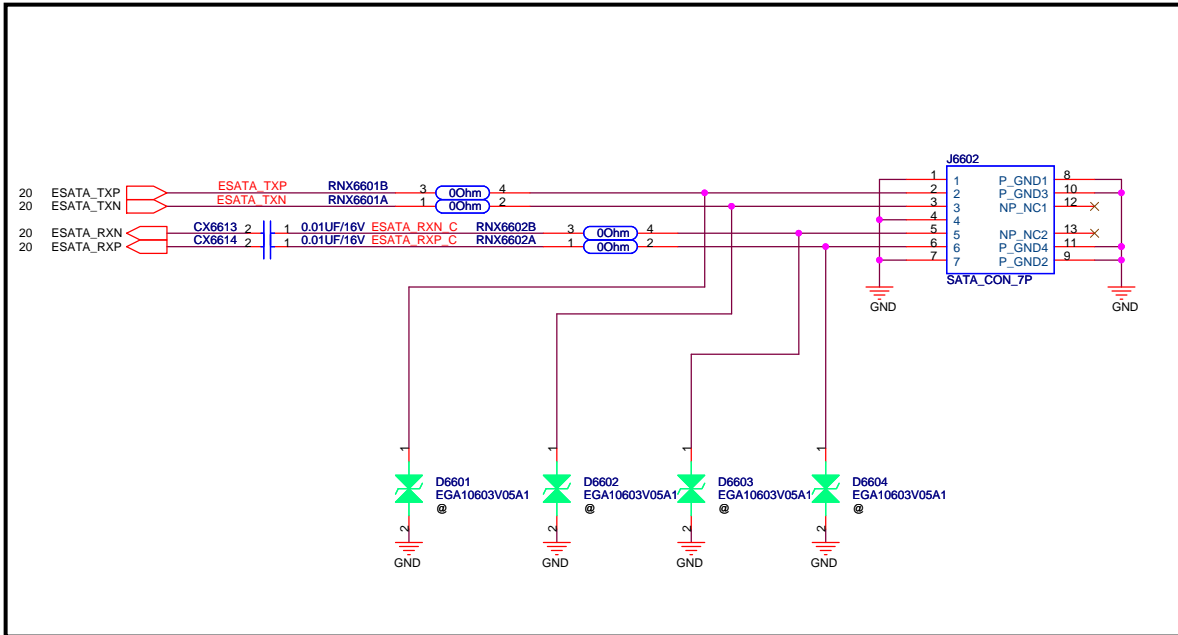
**FOR 3G (TOP)**



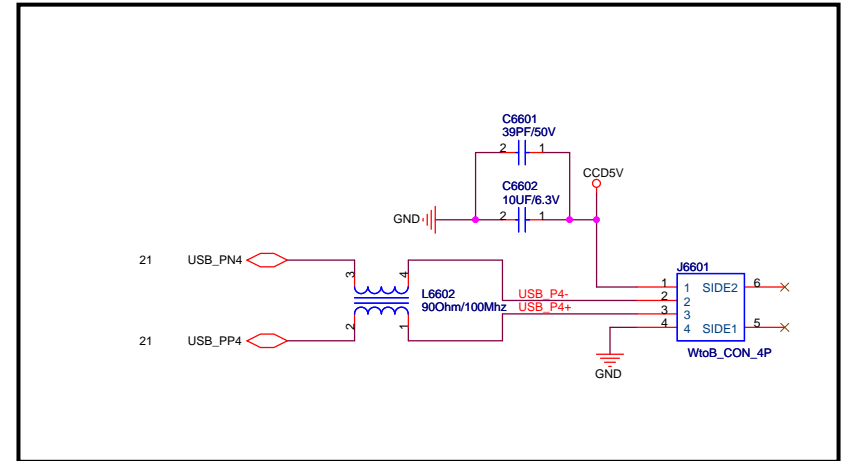
**FOR WLAN (TOP)**



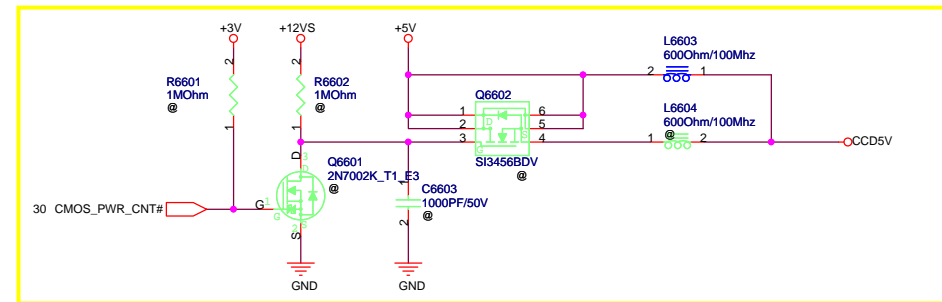
## E-SATA Connector



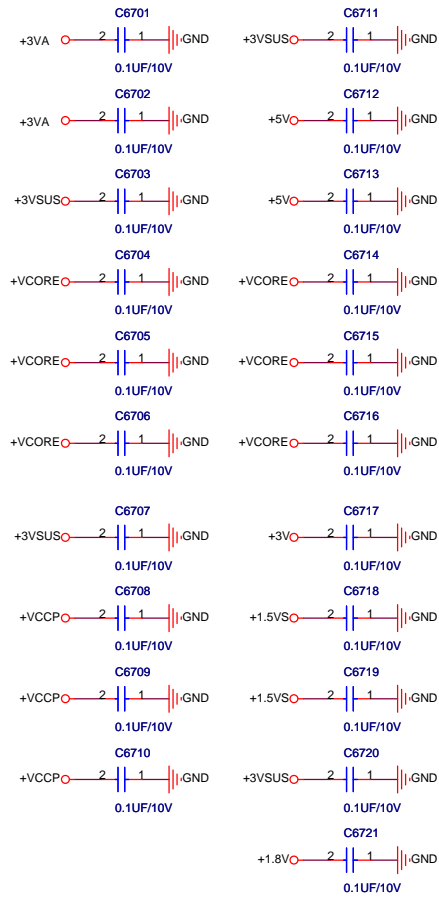
## CMOS Camera Connector



## R2.0



### CAPS for EMI request



### CAPS for VCC cross plane resistance continuity



5

4

3

2

1

D

D

C


C

B

B

A

A

		<b>Title : XDP</b>	
ASUSTeK COMPUTER INC. NB1		Engineer: <OrgAddr1>	
Size	Project Name		Rev
Custom	<b>U6V</b>		2.0
Date: Tuesday, April 15, 2008		Sheet	68 of 102

5

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3

2

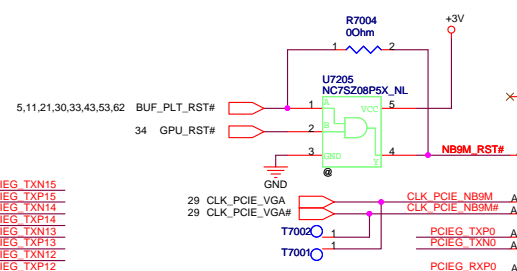
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# U6V Revision History

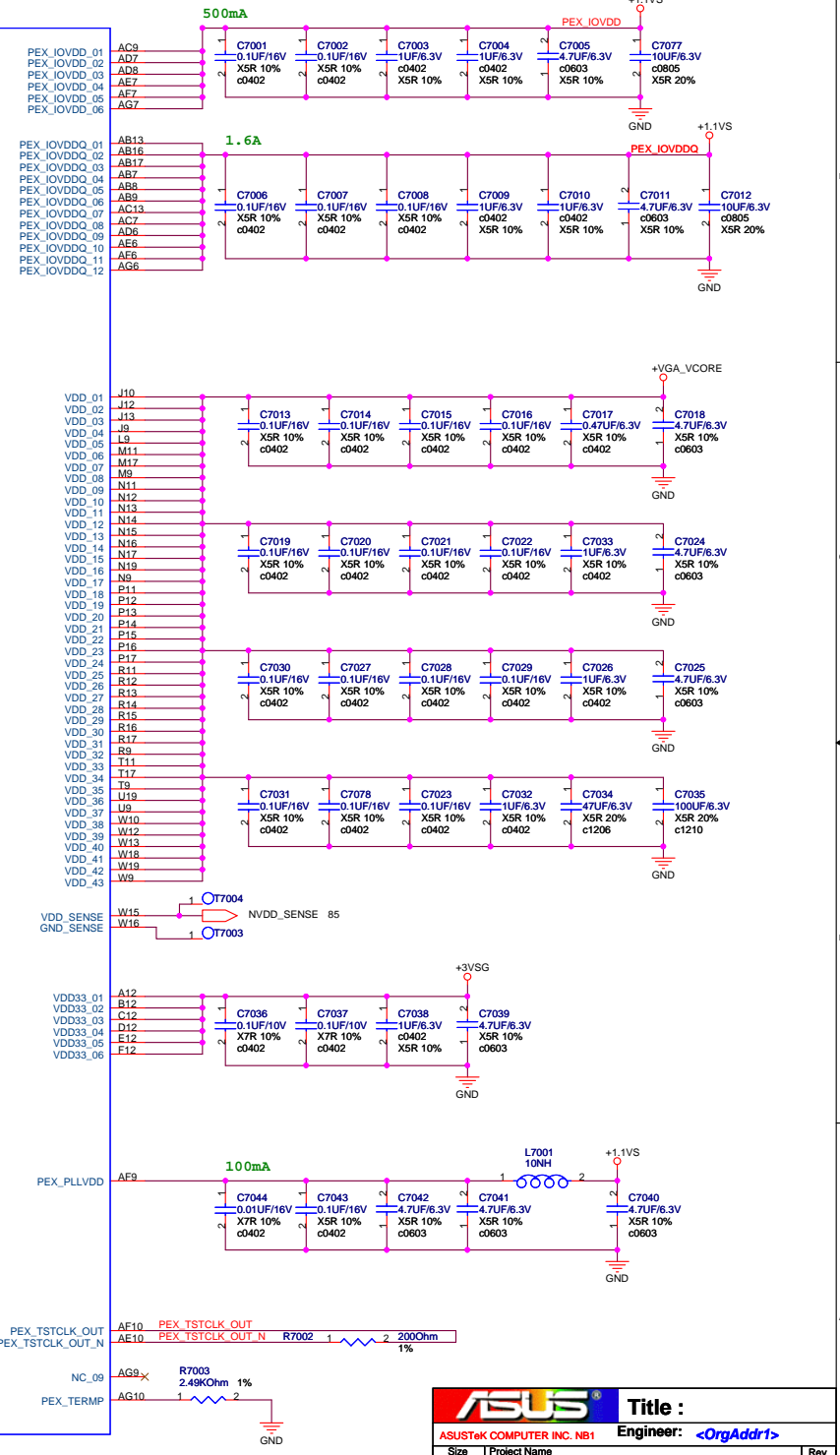
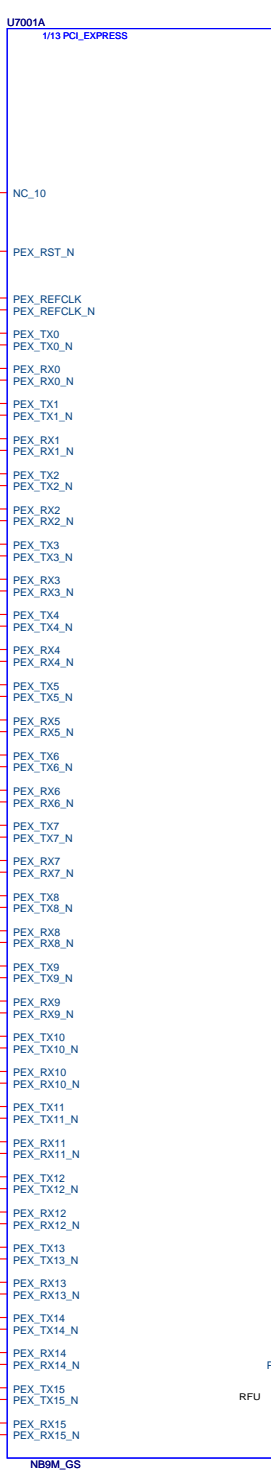
Rev	Date	Description
0.1		

Rev	Date	Description
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PCIEG\_RXP[0..15] 11  
 PCIEG\_RXN[0..15] 11  
 PCIEB\_RXP[0..15] 11  
 PCIEB\_RXN[0..15] 11



PCIEB_RXN15	C7048	1	2	0.1UF/10V	PCIEG_TXN15
PCIEB_RXP15	C7056	1	2	0.1UF/10V	PCIEG_TXP15
PCIEB_RXN14	C7065	1	2	0.1UF/10V	PCIEG_TXN14
PCIEB_RXP14	C7058	1	2	0.1UF/10V	PCIEG_TXP14
PCIEB_RXN13	C7045	1	2	0.1UF/10V	PCIEG_TXN13
PCIEB_RXP13	C7069	1	2	0.1UF/10V	PCIEG_TXP13
PCIEB_RXN12	C7060	1	2	0.1UF/10V	PCIEG_TXN12
PCIEB_RXP12	C7057	1	2	0.1UF/10V	PCIEG_TXP12
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PCIEB_RXN10	C7052	1	2	0.1UF/10V	PCIEG_TXN10
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PCIEB_RXN3	C7053	1	2	0.1UF/10V	PCIEG_TXN3
PCIEB_RXP3	C7050	1	2	0.1UF/10V	PCIEG_TXP3
PCIEB_RXN2	C7074	1	2	0.1UF/10V	PCIEG_TXN2
PCIEB_RXP2	C7051	1	2	0.1UF/10V	PCIEG_TXP2
PCIEB_RXN1	C7062	1	2	0.1UF/10V	PCIEG_TXN1
PCIEB_RXP1	C7054	1	2	0.1UF/10V	PCIEG_TXP1
PCIEB_RXN0	C7075	1	2	0.1UF/10V	PCIEG_TXN0
PCIEB_RXP0	C7077	1	2	0.1UF/10V	PCIEG_TXP0



**ASUS** Title :  
 ASUSTeK COMPUTER INC. NB1 Engineer: <OrgAddr1>  
 Size Project Name Rev  
 Custom U6V 2.0  
 Date: Tuesday, April 15, 2008 Sheet 70 of 102

72 FBAD[0..63]  
72 FBADQM[0..7]  
72 FBARDQS[0..7]  
72 FBARDQS[0..7]

**U7001B**

**2/13 FRAME\_BUFFER**

- FBAD0 D21
- FBAD1 C22
- FBAD2 B22
- FBAD3 A22
- FBAD4 C24
- FBAD5 B25
- FBAD6 B25
- FBAD7 A26
- FBAD8 D22
- FBAD9 E24
- FBAD10 E22
- FBAD11 D24
- FBAD12 D26
- FBAD13 E20
- FBAD14 C27
- FBAD15 B27
- FBAD16 D16
- FBAD17 E16
- FBAD18 D17
- FBAD19 F18
- FBAD20 D20
- FBAD21 E20
- FBAD22 E21
- FBAD23 F21
- FBAD24 C18
- FBAD25 B18
- FBAD26 C18
- FBAD27 D18
- FBAD28 C19
- FBAD29 C21
- FBAD30 B21
- FBAD31 A21
- FBAD32 C22
- FBAD33 P24
- FBAD34 R23
- FBAD35 R24
- FBAD36 T23
- FBAD37 U24
- FBAD38 V23
- FBAD39 V24
- FBAD40 N25
- FBAD41 N26
- FBAD42 R25
- FBAD43 B18
- FBAD44 T25
- FBAD45 V26
- FBAD46 V25
- FBAD47 V27
- FBAD48 W22
- FBAD49 W22
- FBAD50 W23
- FBAD51 W24
- FBAD52 A22
- FBAD53 AB23
- FBAD54 AB24
- FBAD55 AC24
- FBAD56 W25
- FBAD57 W26
- FBAD58 W27
- FBAD59 A25
- FBAD60 AB25
- FBAD61 AB26
- FBAD62 AD26
- FBAD63 AD27
- FBAD63

- FBADQM0 D23
- FBADQM1 C26
- FBADQM2 D19
- FBADQM3 B19
- FBADQM4 T24
- FBADQM5 T26
- FBADQM6 AA23
- FBADQM7 AB27

- FBARDQS0 A24
- FBARDQS1 C26
- FBARDQS2 E18
- FBARDQS3 A19
- FBARDQS4 T22
- FBARDQS5 T27
- FBARDQS6 AA24
- FBARDQS7 AA26

- FBARDQS0 B24
- FBARDQS1 D25
- FBARDQS2 E18
- FBARDQS3 A18
- FBARDQS4 R22
- FBARDQS5 R27
- FBARDQS6 Y24
- FBARDQS7 AA27

- FBA\_DQS\_WP0
- FBA\_DQS\_WP1
- FBA\_DQS\_WP2
- FBA\_DQS\_WP3
- FBA\_DQS\_WP4
- FBA\_DQS\_WP5
- FBA\_DQS\_WP6
- FBA\_DQS\_WP7

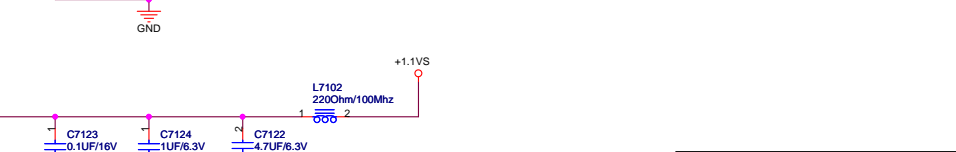
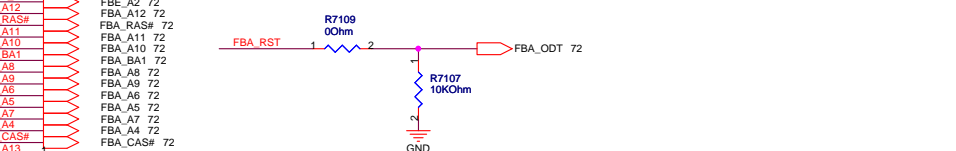
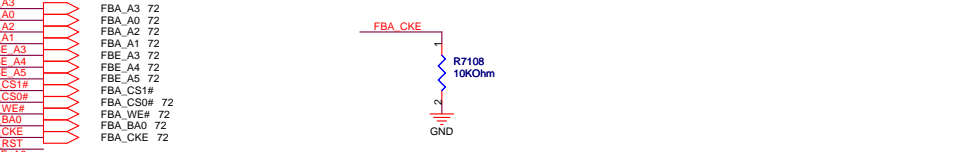
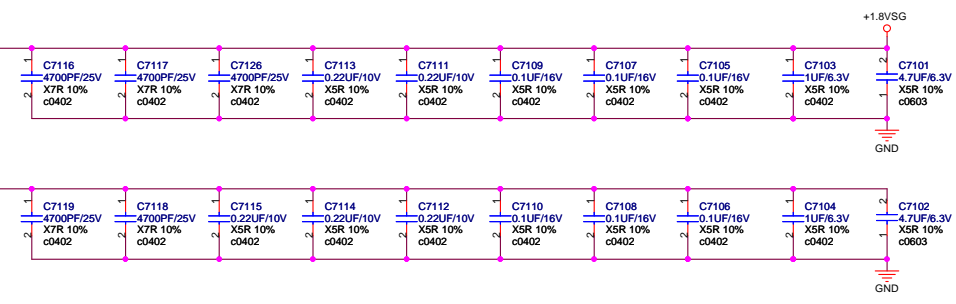
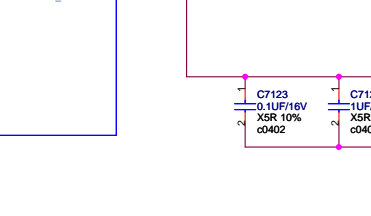
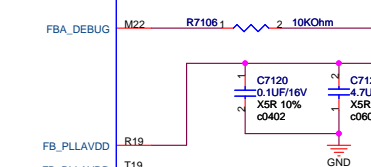
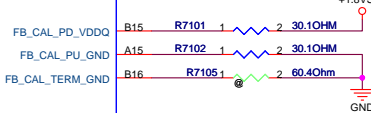
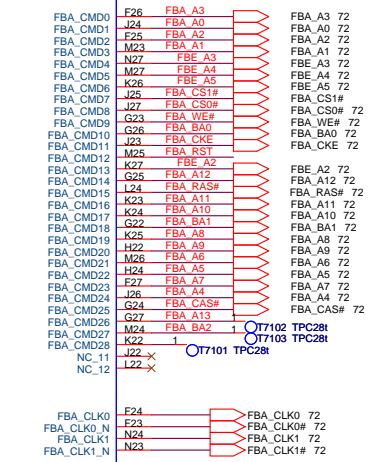
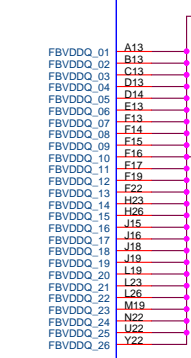
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- FBA\_DQS\_RN1
- FBA\_DQS\_RN2
- FBA\_DQS\_RN3
- FBA\_DQS\_RN4
- FBA\_DQS\_RN5
- FBA\_DQS\_RN6
- FBA\_DQS\_RN7

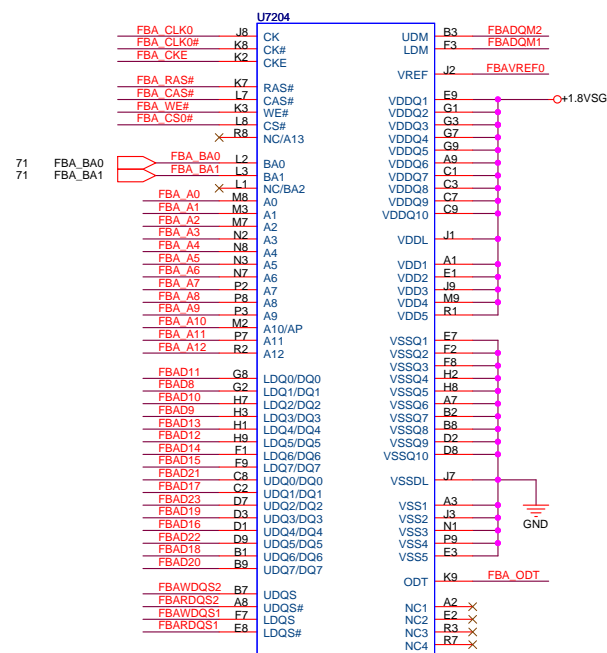
- FBVDDQ\_01
- FBVDDQ\_02
- FBVDDQ\_03
- FBVDDQ\_04
- FBVDDQ\_05
- FBVDDQ\_06
- FBVDDQ\_07
- FBVDDQ\_08
- FBVDDQ\_09
- FBVDDQ\_10
- FBVDDQ\_11
- FBVDDQ\_12
- FBVDDQ\_13
- FBVDDQ\_14
- FBVDDQ\_15
- FBVDDQ\_16
- FBVDDQ\_17
- FBVDDQ\_18
- FBVDDQ\_19
- FBVDDQ\_20
- FBVDDQ\_21
- FBVDDQ\_22
- FBVDDQ\_23
- FBVDDQ\_24
- FBVDDQ\_25
- FBVDDQ\_26

- FBA\_CMD0
- FBA\_CMD1
- FBA\_CMD2
- FBA\_CMD3
- FBA\_CMD4
- FBA\_CMD5
- FBA\_CMD6
- FBA\_CMD7
- FBA\_CMD8
- FBA\_CMD9
- FBA\_CMD10
- FBA\_CMD11
- FBA\_CMD12
- FBA\_CMD13
- FBA\_CMD14
- FBA\_CMD15
- FBA\_CMD16
- FBA\_CMD17
- FBA\_CMD18
- FBA\_CMD19
- FBA\_CMD20
- FBA\_CMD21
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- FBA\_CMD25
- FBA\_CMD26
- FBA\_CMD27
- FBA\_CMD28

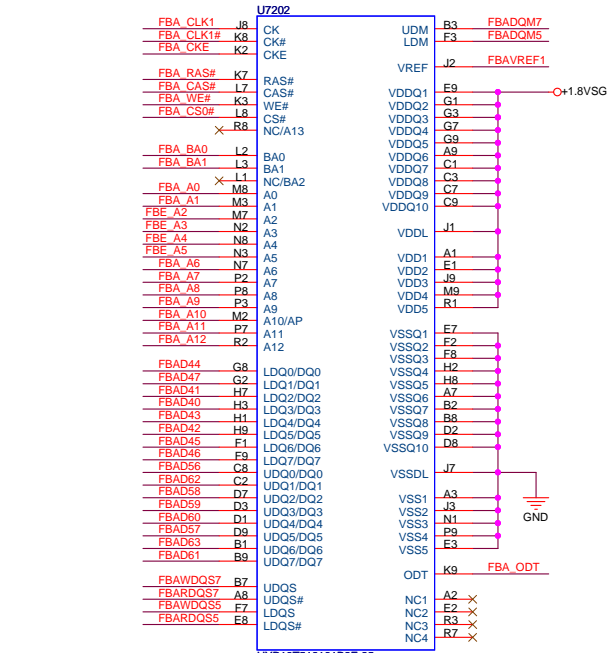
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- FBA\_CLK0\_N
- FBA\_CLK1
- FBA\_CLK1\_N

- FBA\_CKE
- FBA\_RST
- FBA\_ODT

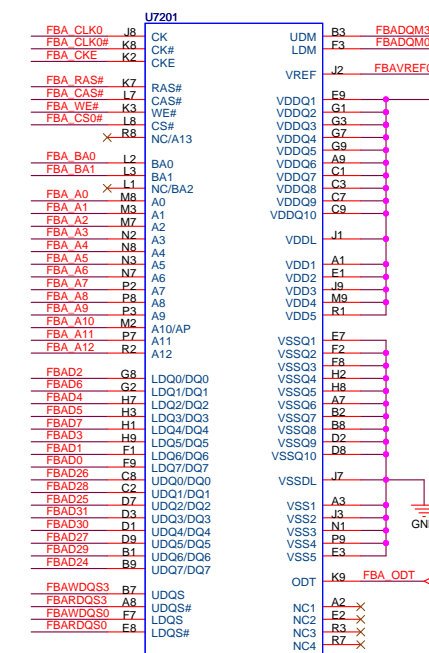




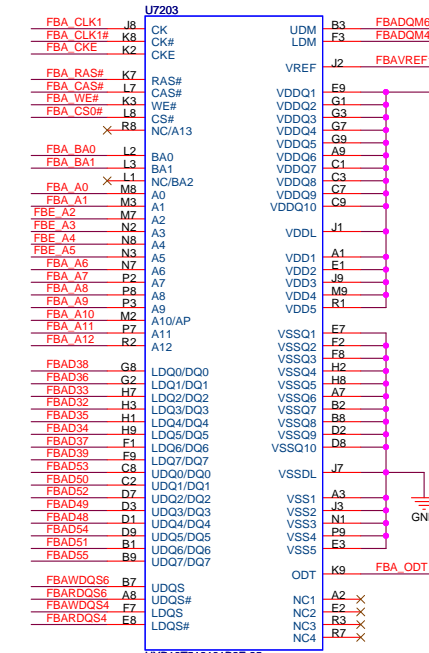
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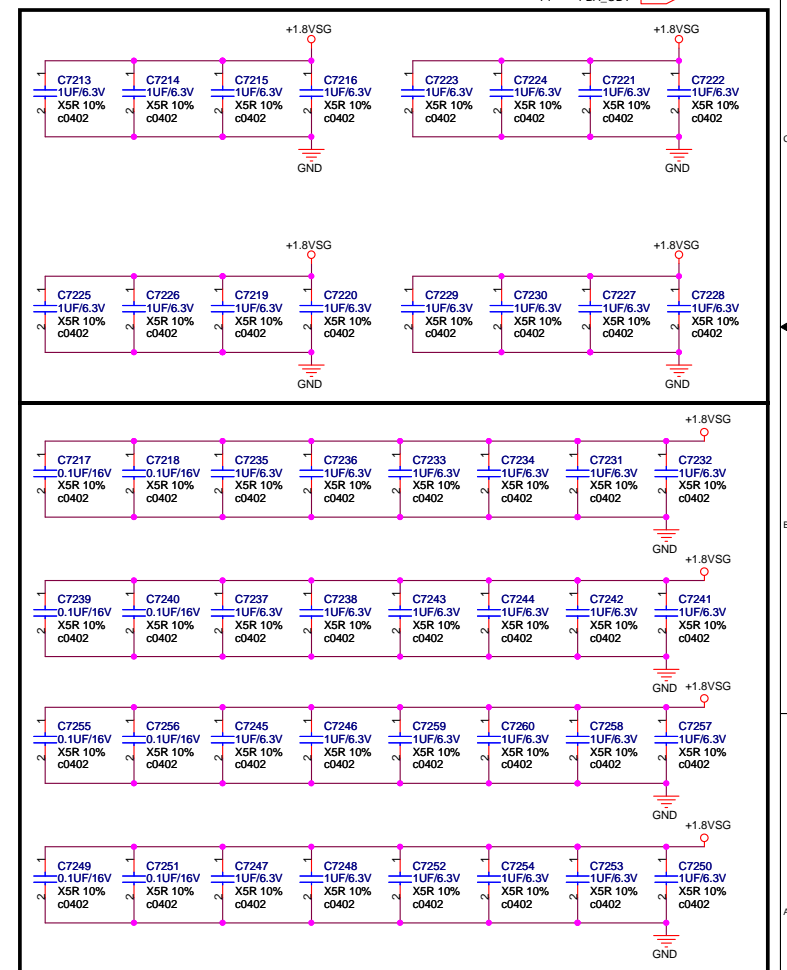
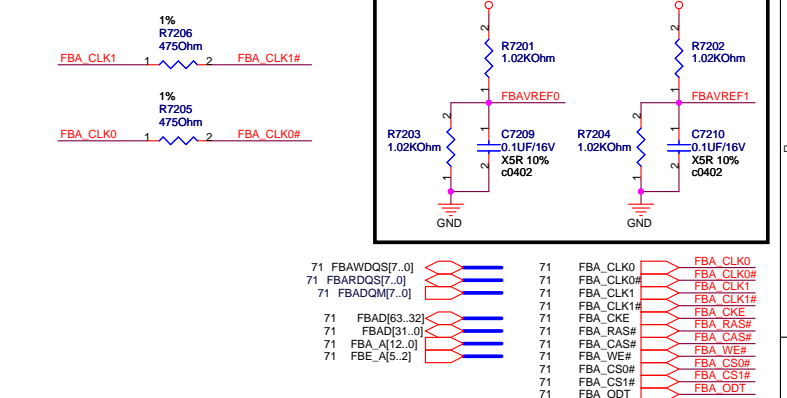
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HYB18T512161B2F-25

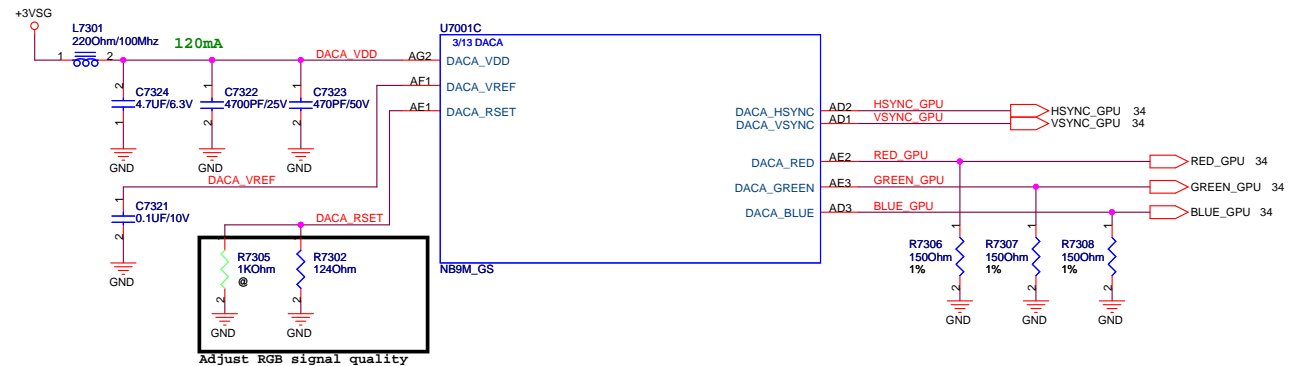


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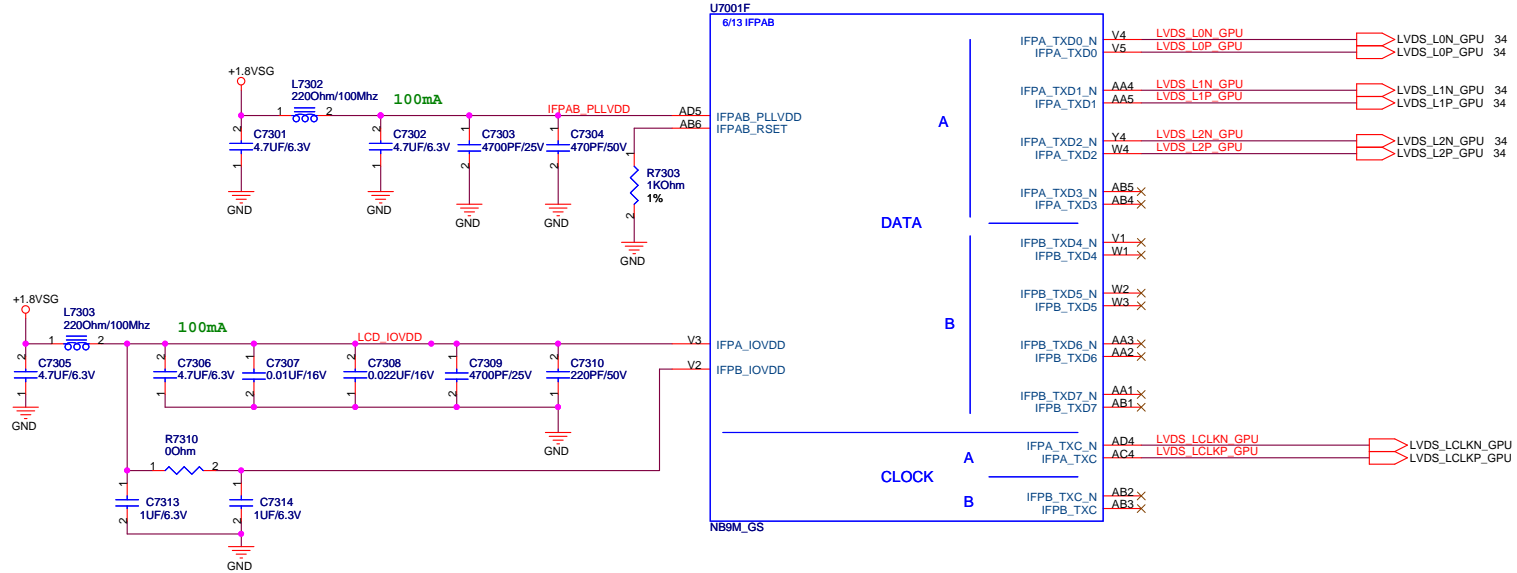




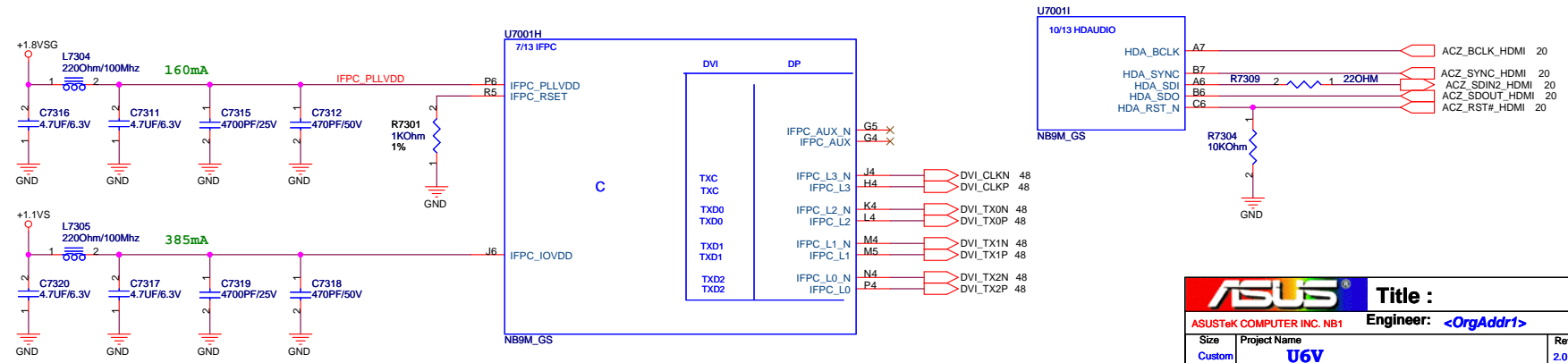
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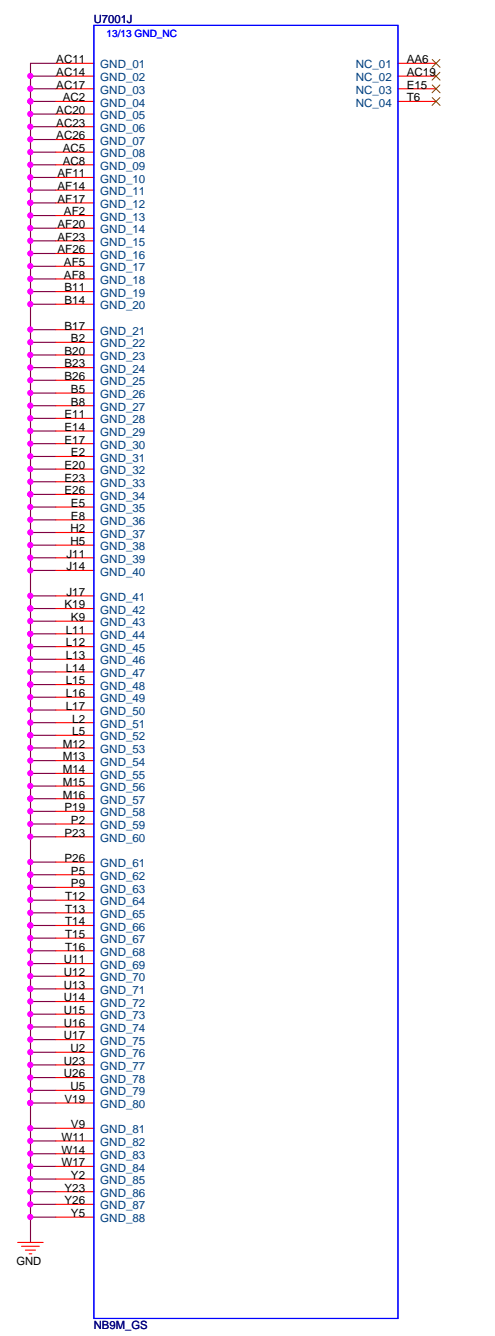
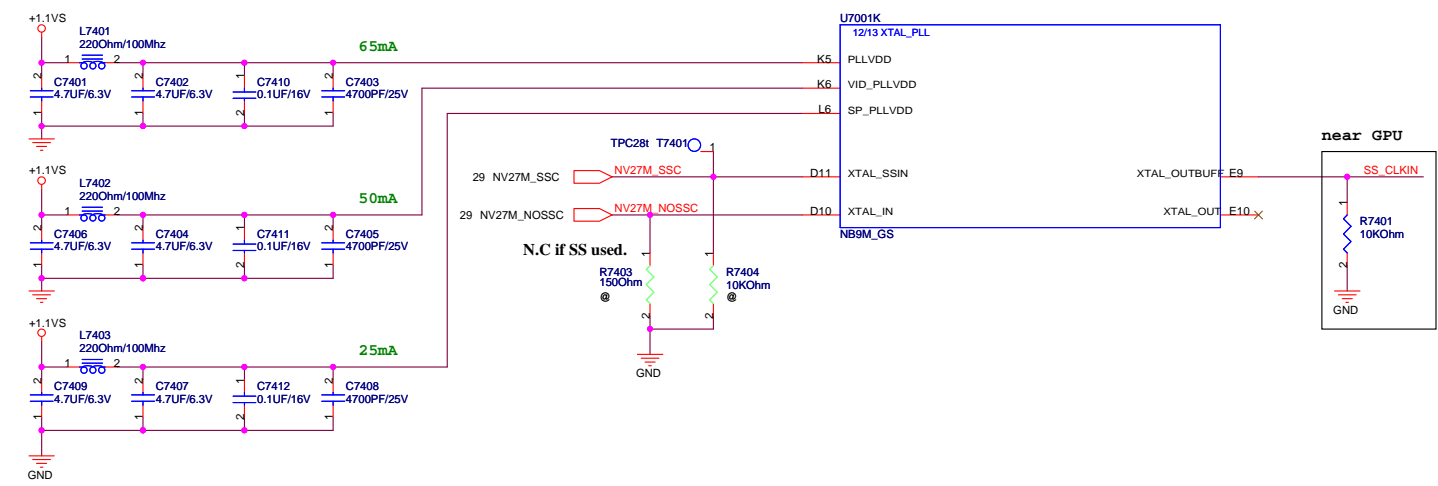
# LVDS



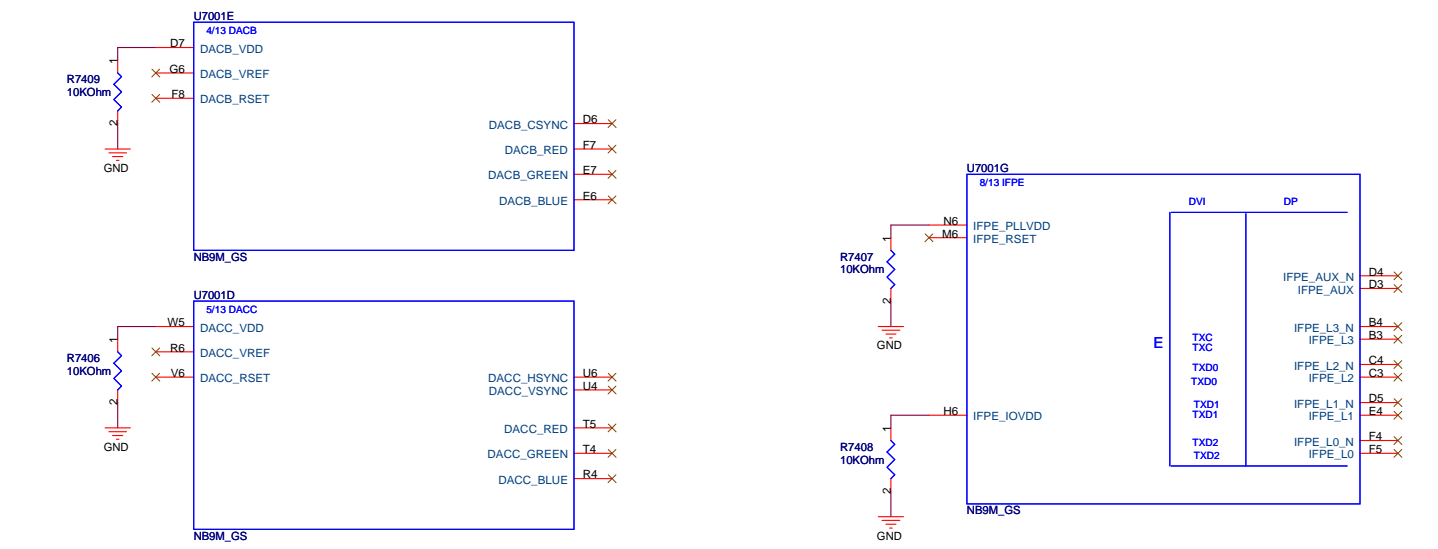
# HDMI



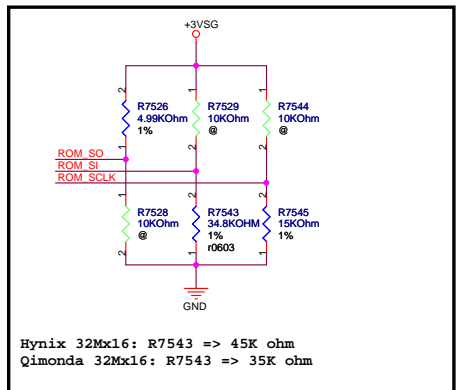
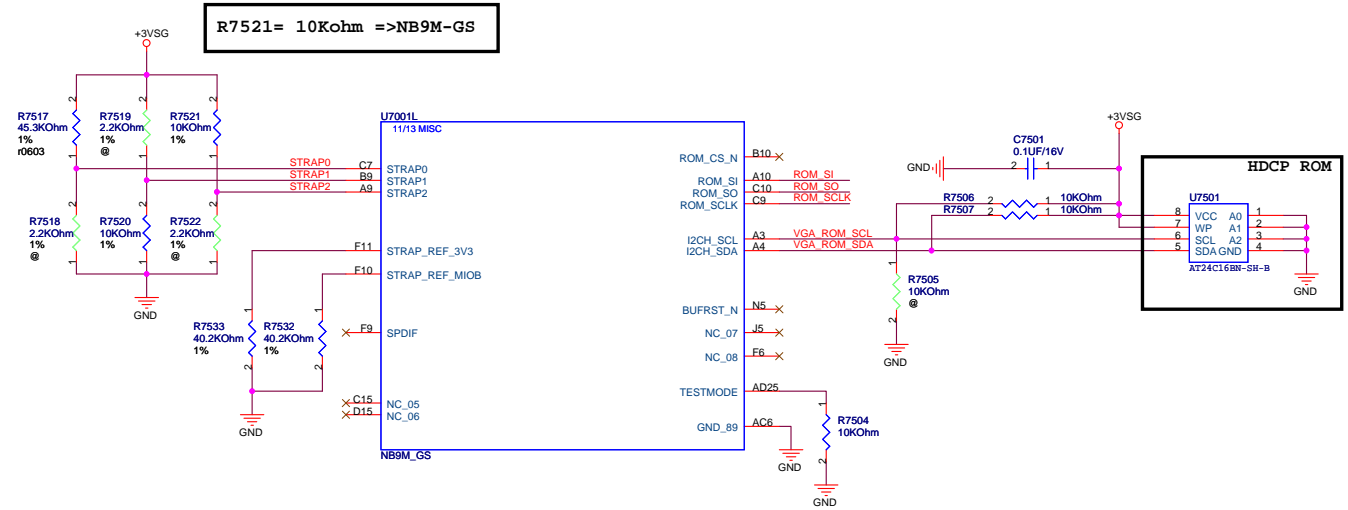
# Xtal



# Other

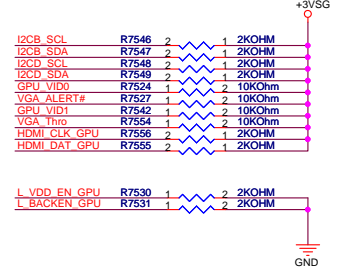
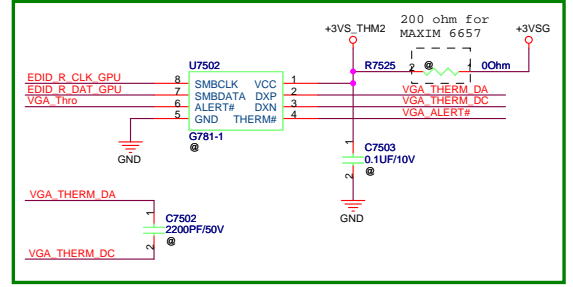


**ROM**



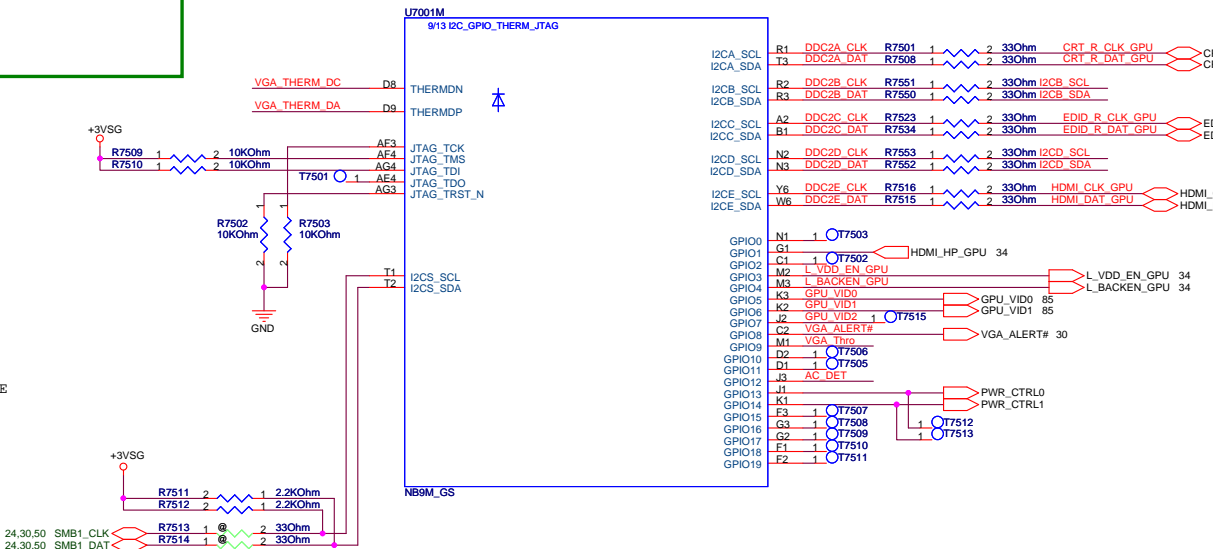
**GPIO**

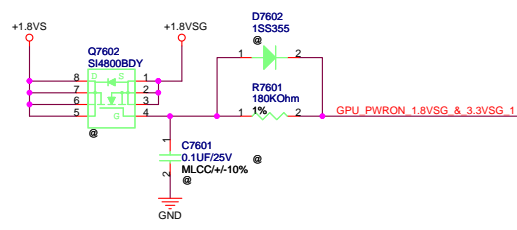
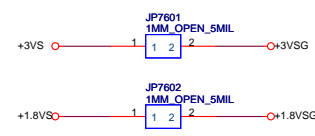
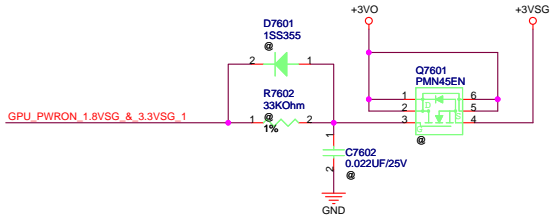
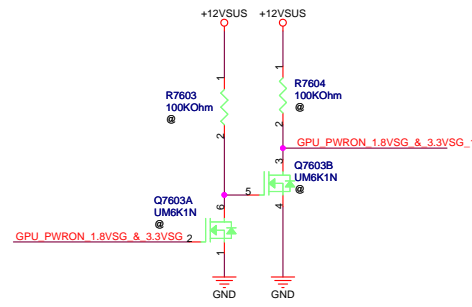
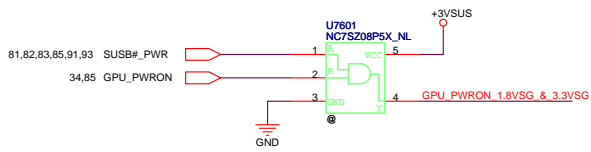
**External thermal sensor**



**GPIO ASSIGNMENTS**

GPIO	I/O	ACTIVE	USAGE
0	IN	N/A	N/A
1	IN	N/A	HDMI HOTPLUG
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVDD VID 0
6	OUT	N/A	NVDD VID 1
7	OUT	N/A	FBVDD VID 0
8	IN	LOW	THERMAL ALERT
9	OUT	LOW	FAN PWM
10	OUT	N/A	FBVREF SELECT
11	OUT	Low	SLI SYNCO
12	IN	N/A	AC DETECT
13	OUT	N/A	PS CONTROL
14	OUT	N/A	PS CONTROL





	5	4	3	2	1
D					
C					
B					
A					



**Title : Cantiga-POWER(5)**

ASUSTeK COMPUTER INC. NB1

**Engineer: <OrgAddr1>**

Size	Project Name	Rev
A	<b>U6V</b>	2.0

Date: **Tuesday, April 15, 2008** Sheet **77** of **102**

	5	4	3	2	1
D					
C					
B					
A					

5

4

3

2

1

D

D

C

C

B

B

A

A



**Title :** Cantiga-POWER(5)

ASUSTeK COMPUTER INC. NB1

**Engineer:** <OrgAddr1>

Size	Project Name	Rev
A	U6V	2.0

Date: Tuesday, April 15, 2008

Sheet 78 of 102

5

4

3

2

1

5

4

3

2

1

D

D

C

C

B

B

A

A



Title :

ASUSTeK COMPUTER INC. NB1

Engineer: <OrgAddr1>

Size	Project Name	Rev
A	U6V	2.0

Date: Tuesday, April 15, 2008

Sheet 79 of 102

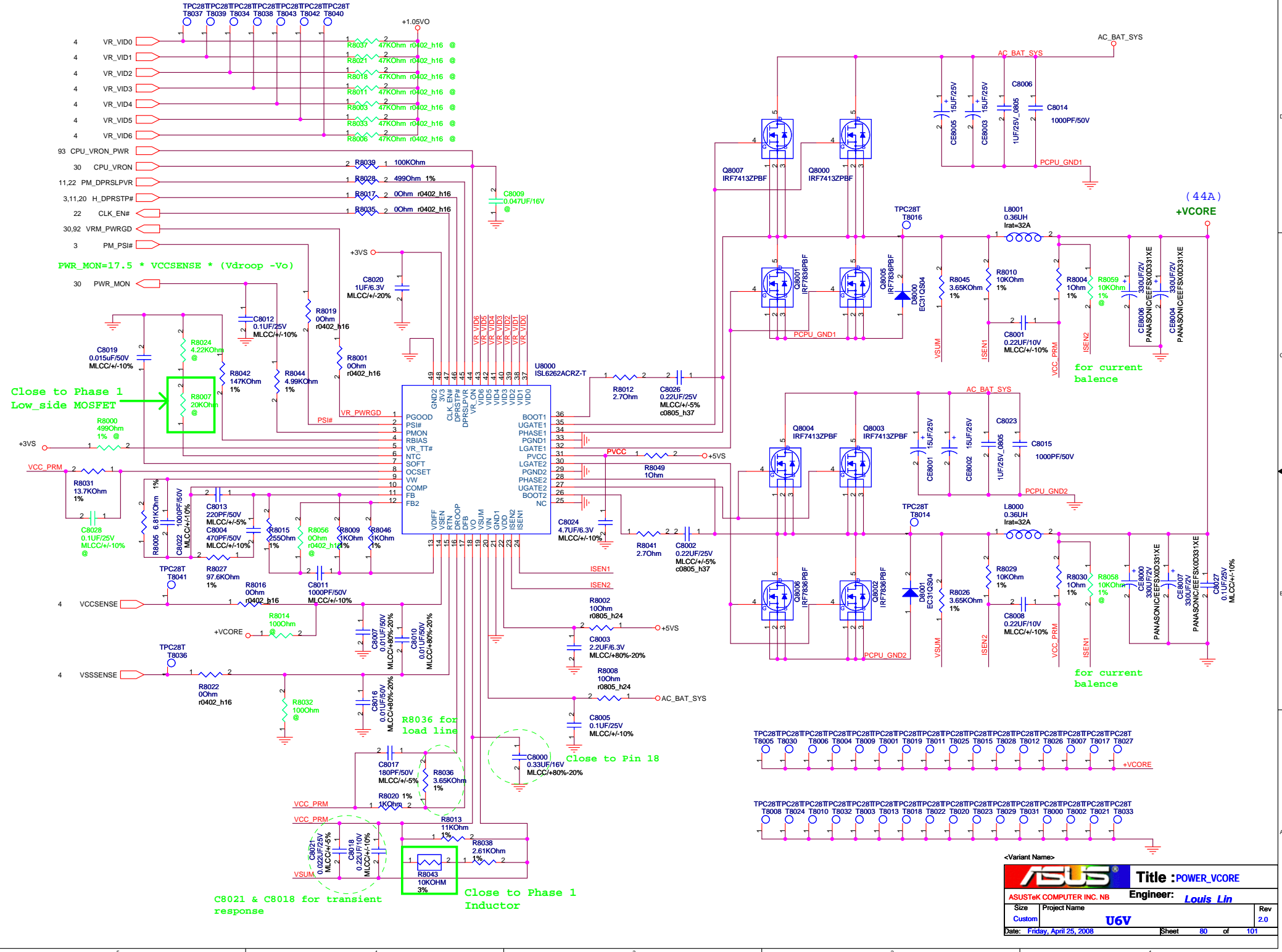
5

4

3

2

1



$PWR\_MON = 17.5 * VCCSENSE * (Vdroop - V_o)$

Close to Phase 1 Low\_side MOSFET

for current balance

for current balance

R8036 for load line

Close to Pin 18 Inductor

C8021 & C8018 for transient response

Close to Phase 1 Inductor

<Variant Name>

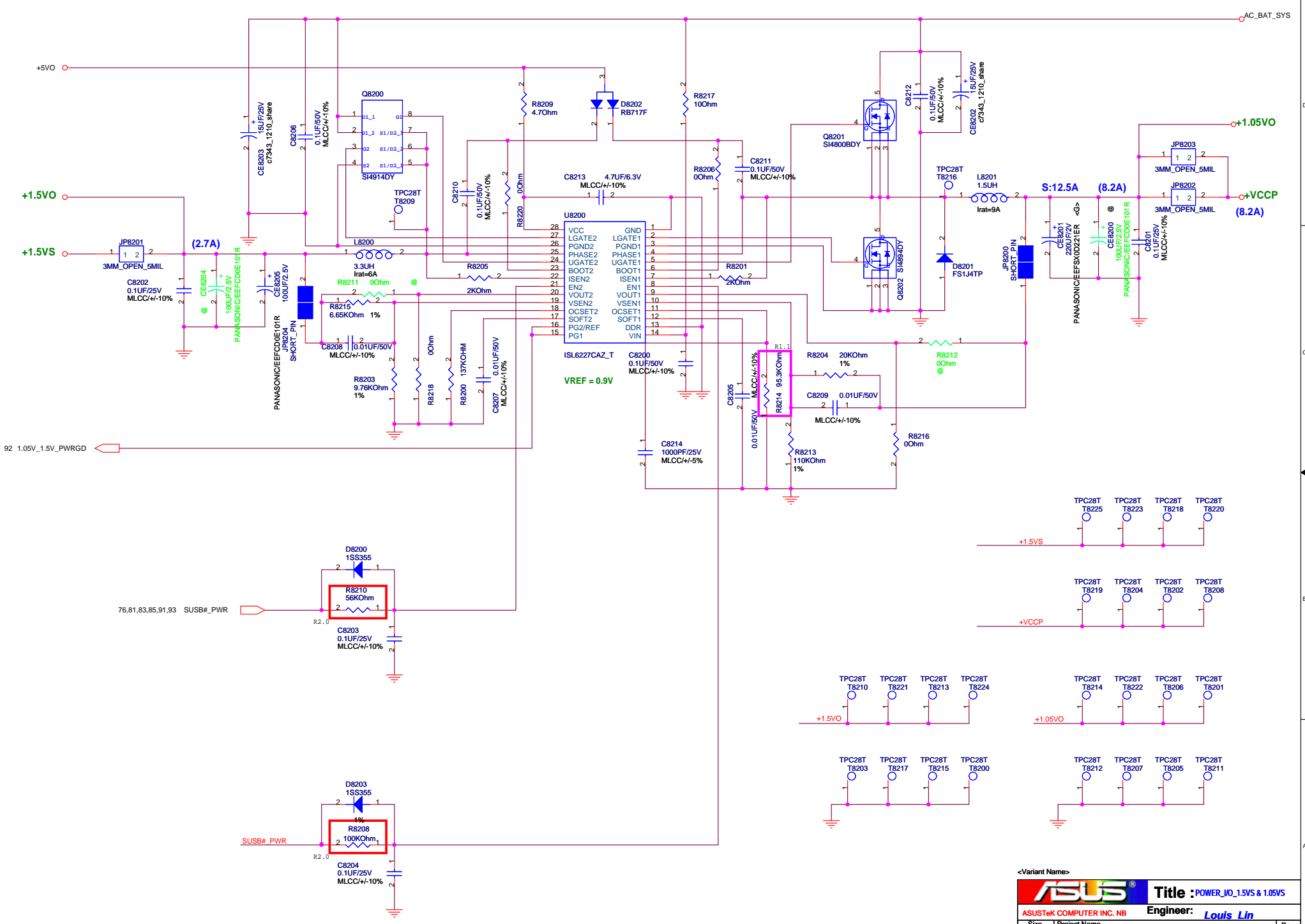
**Title : POWER\_VCORE**

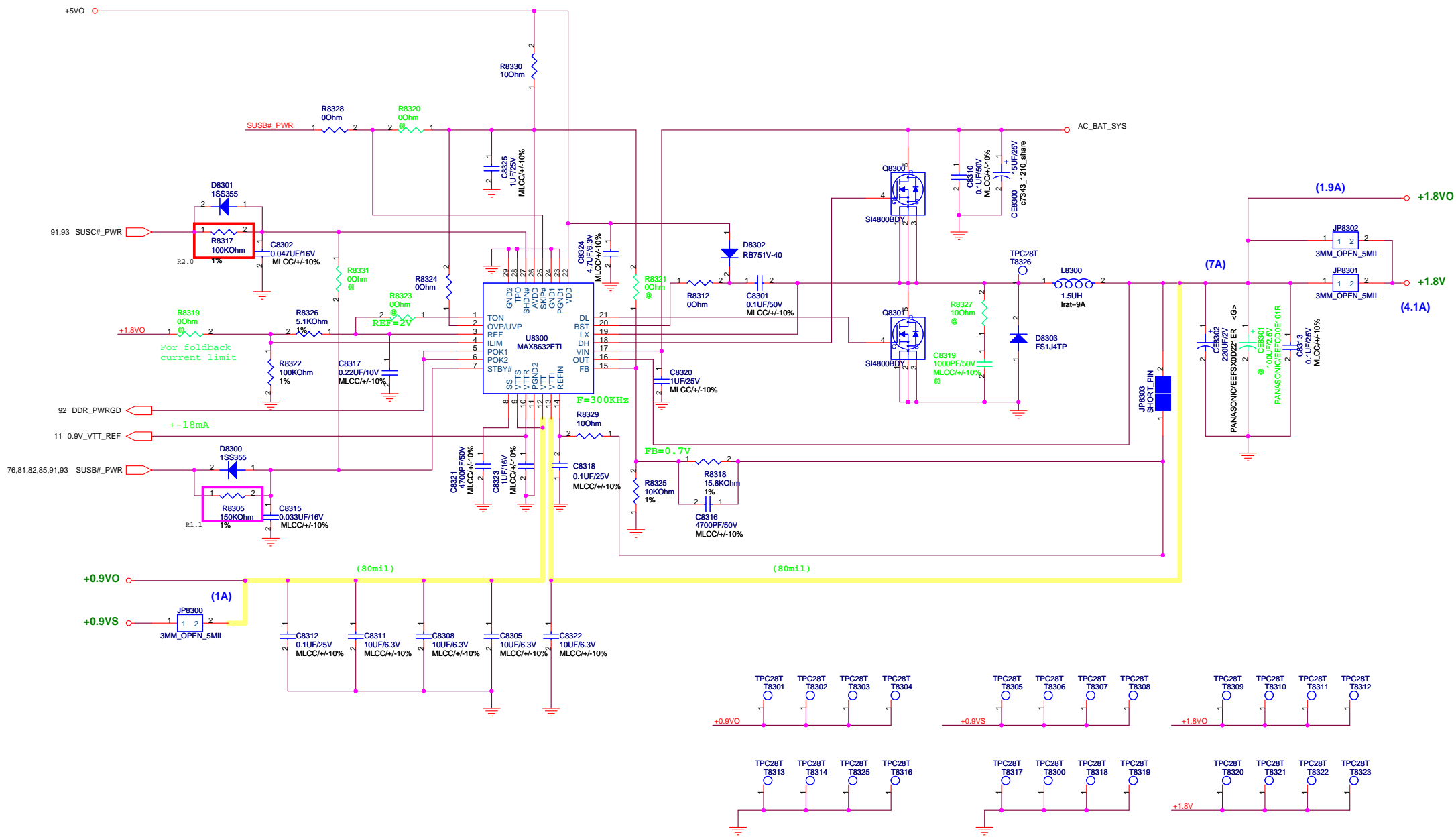
ASUSTeK COMPUTER INC. NB Engineer: **Louis Lin**

Size	Project Name	Rev
Custom	<b>U6V</b>	2.0
Date: Friday, April 25, 2008	Sheet	80 of 101









5

4

3

2

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D

D

C

C


B

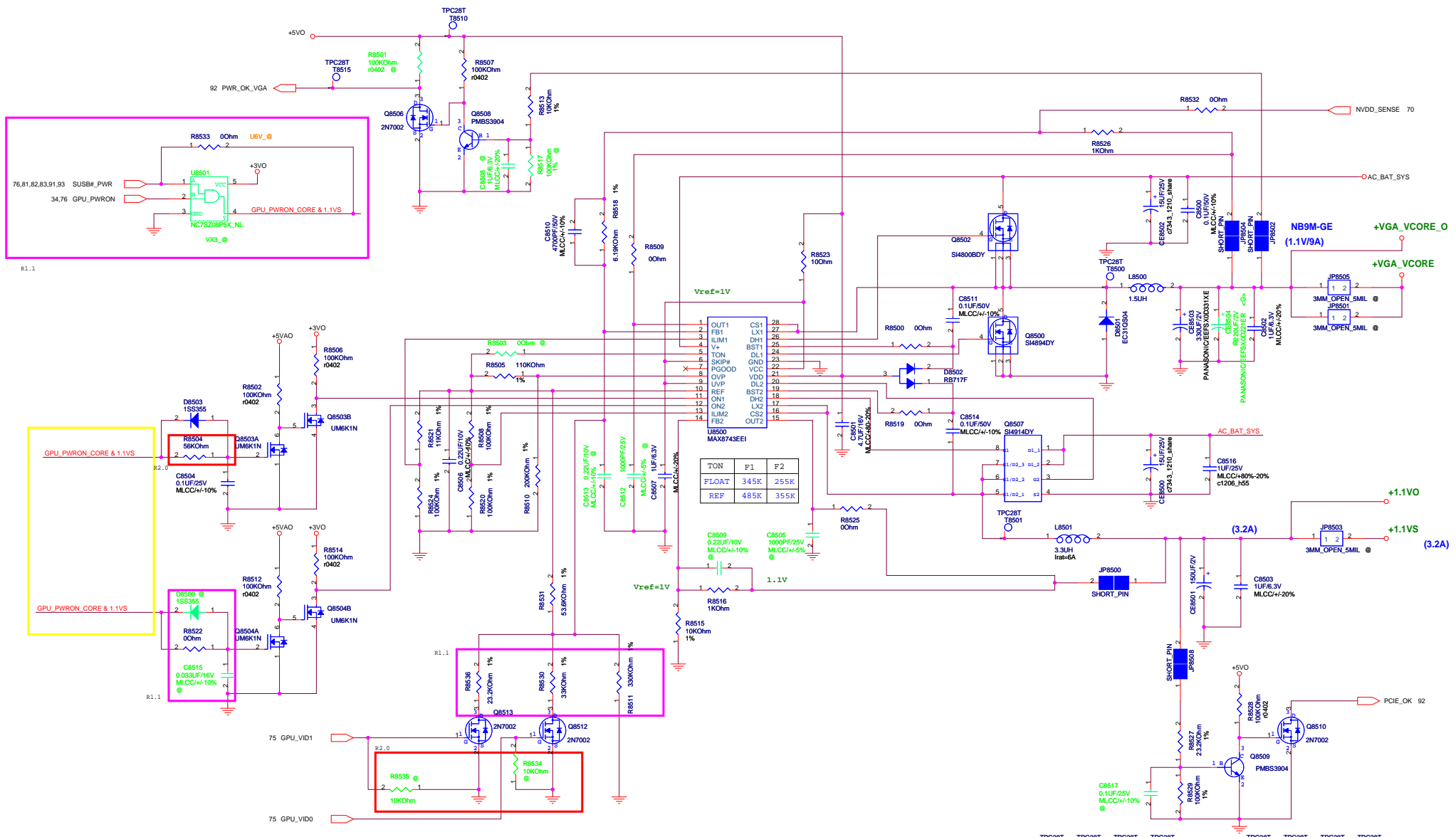
B

A

A

<Variant Name>

		<b>Title :</b> POWER_IO_+1.25VS&+2.5VS	
ASUSTeK COMPUTER INC. NB		<b>Engineer:</b> <i>Louis Lin</i>	
Size Custom	Project Name U6V	Rev 2.0	
Date: Friday, April 25, 2008		Sheet	84 of 101



**For NB9M-GS**

GPU_VID0	GPU_VID1	+VGA_VCORE_O
L	L	0.9V
H	L	1.09V
L	H	1.17V
H	H	X

R8511=330K(10G213330313010)  
 R8530=33K(10G213330213030)  
 R8536=23.2K(10G21332213030)

**For NB9M-GE**

GPU_VID0	+VGA_VCORE_O
L	0.9V
H	1.0V

Unmount Q8513, R8536, R8535  
 R8511=330K(10G213330313010)  
 R8530=61.9K(10G213619213030)

MAX8743EEI

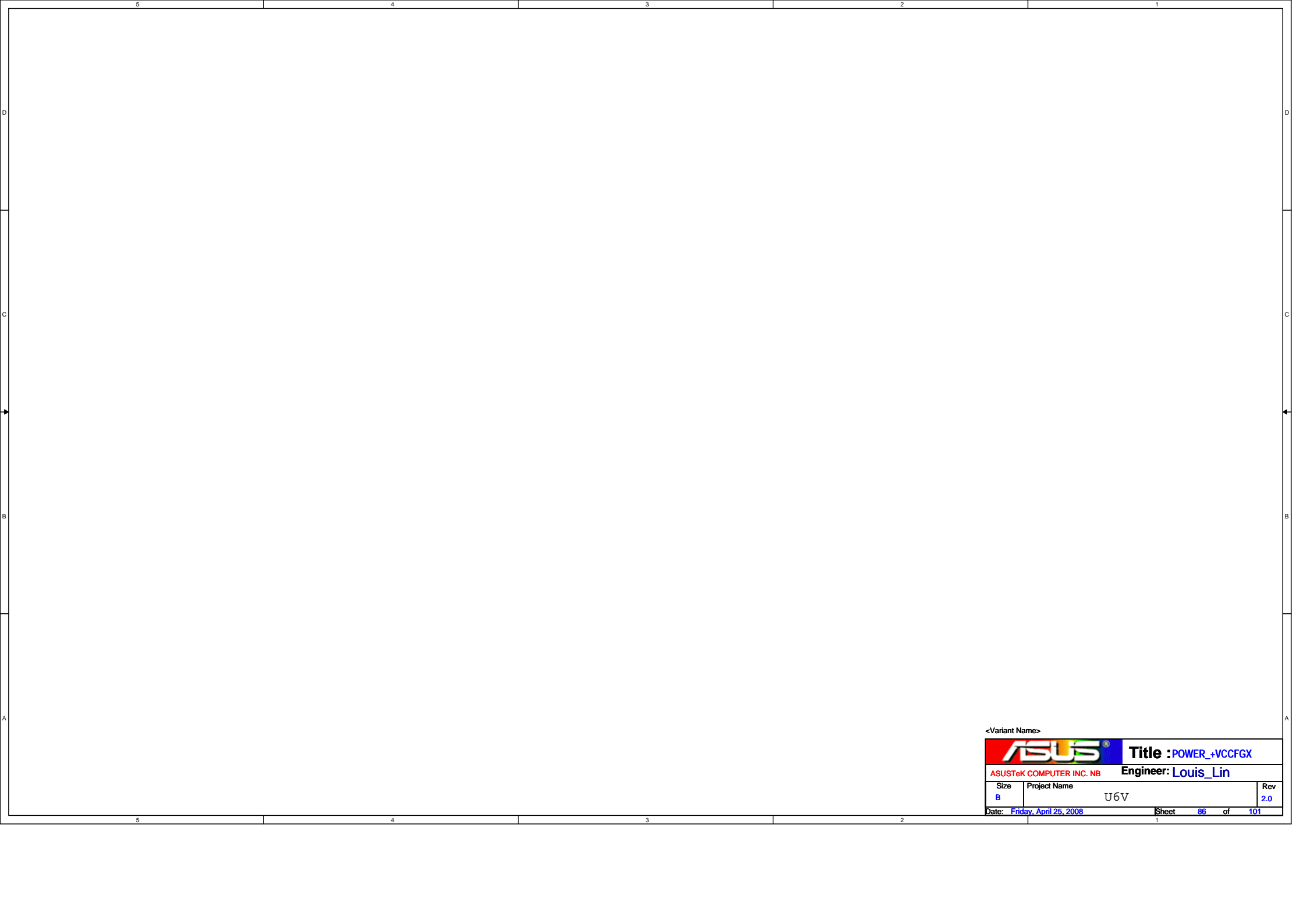
TON	F1	F2
Float	345K	255K
REF	485K	355K


<Variant Name>

**Title : POWER\_VGA\_CORE & 1.1VS**

ASUSTeK COMPUTER INC. NB Engineer: **Louis Lin**

Size	Project Name	Rev
Custom	U6V	2.0
Date: Friday, April 25, 2008	Sheet	85 of 101



<Variant Name>		
		<b>Title :</b> POWER+_VCCFGX
<b>ASUSTeK COMPUTER INC. NB</b>		<b>Engineer:</b> Louis_Lin
Size B	Project Name U6V	Rev 2.0
Date: <a href="#">Friday, April 25, 2008</a>		Sheet <a href="#">86</a> of <a href="#">101</a>

5

4

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D

D

C

C

B

B

A

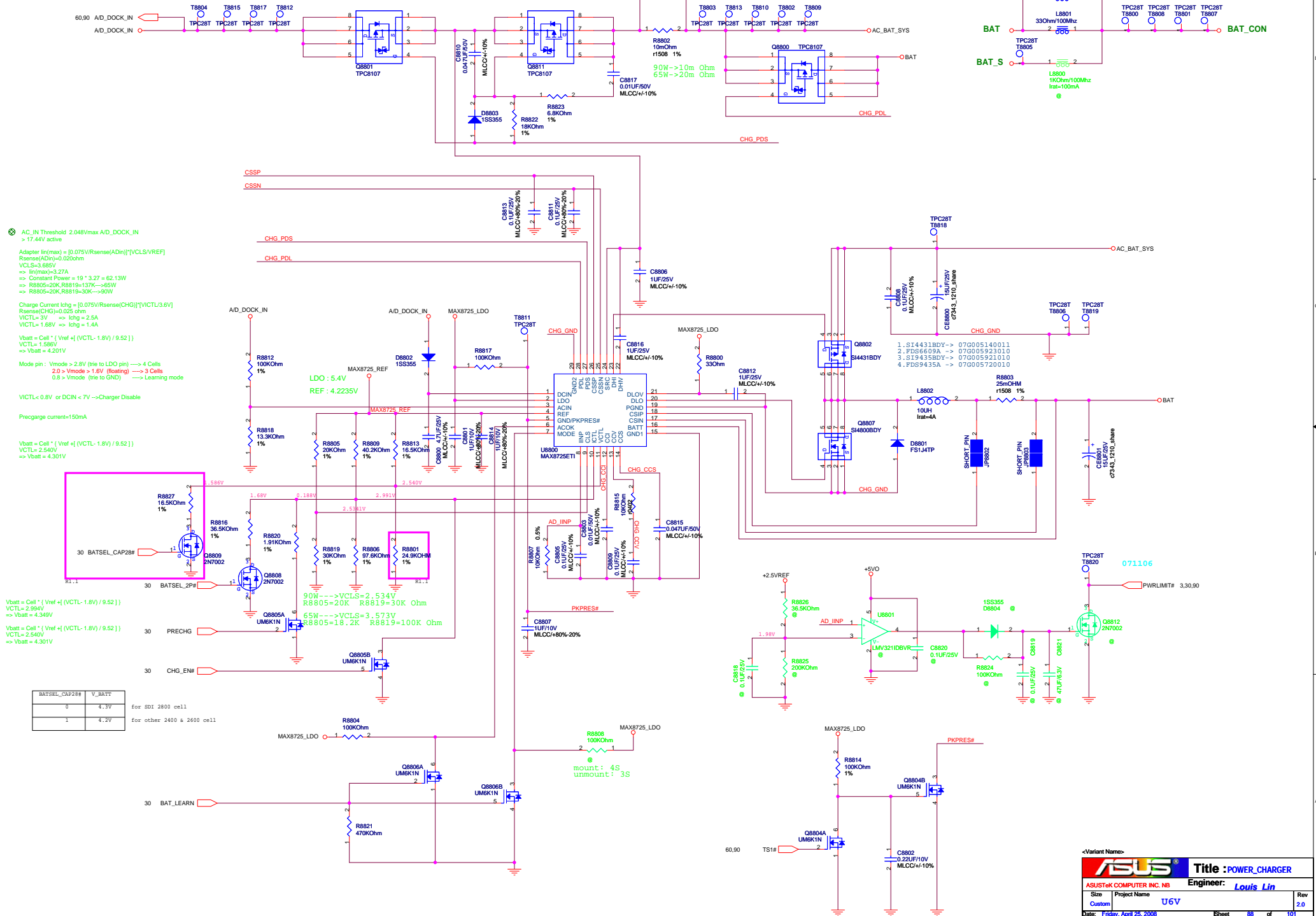
A

<Variant Name>

		<b>Title :</b> POWER_SHUTDOWN#
ASUSTeK COMPUTER INC. NB		<b>Engineer:</b> <i>Louis_Lin</i>

Size	Project Name	Rev
Custom	U6V	2.0
Date: <i>Friday, April 25, 2008</i>		Sheet 87 of 101

POWER PATH & BAT\_LEARN



**AC\_IN Threshold 2.048Vmax A/D\_DOCK\_IN > 17.44V active**  
 Adaptor In(max) = [0.075V/Rsense(ADin)]\*[VCLS/VREF]  
 Rsense(ADin)=0.020ohm  
 VCLS=3.685V  
 => In(max)=3.27A  
 => Constant Power = 19 \* 3.27 = 62.13W  
 => R8805=20K, R8819=137K-->65W  
 => R8805=20K, R8819=30K-->90W  
 Charge Current Ichg = [0.075V/Rsense(CHG)]\*[VICT/3.6V]  
 Rsense(CHG)=0.025 ohm  
 VICTL=3V => Ichg = 2.5A  
 VICTL= 1.68V => Ichg = 1.4A  
 Vbatt = Cell \* (Vref + (VCTL - 1.8V) / 9.52)  
 VCTL = 1.586V  
 => Vbatt = 4.201V  
 Mode pin : Vmode > 2.8V (tie to LDO pin) ----> 4 Cells  
 2.0 > Vmode > 1.6V (floating) ----> 3 Cells  
 0.8 > Vmode (tie to GND) ----> Learning mode  
 VICTL < 0.8V or DCIN < 7V --> Charger Disable  
 Precharge current=150mA

Vbatt = Cell \* (Vref + (VCTL - 1.8V) / 9.52)  
 VCTL = 2.994V  
 => Vbatt = 4.349V  
 Vbatt = Cell \* (Vref + (VCTL - 1.8V) / 9.52)  
 VCTL = 2.540V  
 => Vbatt = 4.301V

BATSEL_CAP2#	V_BATT
0	4.3V
1	4.2V

for SD1 2800 cell  
for other 2400 & 2600 cell

R8808 100KOhm  
 MAX8725\_LDO  
 mount: 4S  
 unmount: 3S

<Variant Name>

**ASUS** Title : POWER\_CHARGER

ASUSTek COMPUTER INC. NB Engineer: **Louis Lin**

Size: Custom Project Name: U6V Rev: 2.0

Date: Friday, April 25, 2008 Sheet: 88 of 101



5

4

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D

C

C

B

B

A

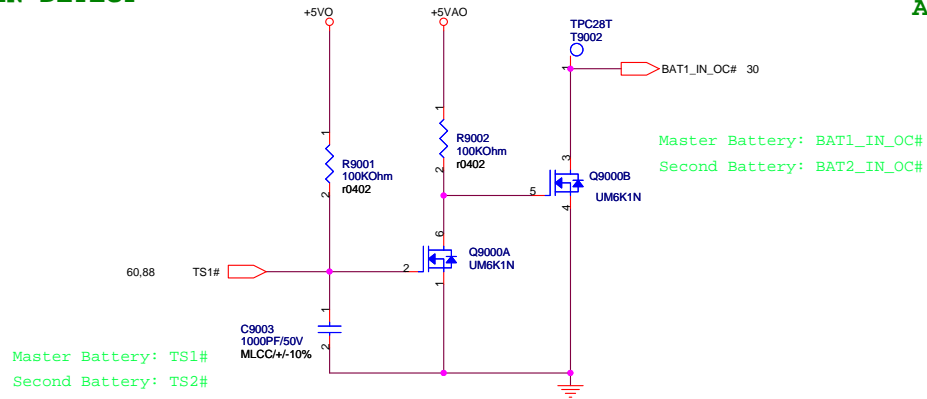
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<Variant Name>

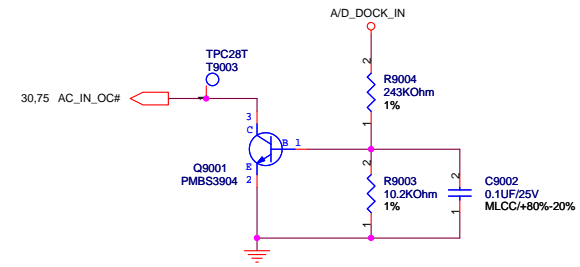
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ASUSTeK COMPUTER INC. NB		<b>Engineer:</b>

Size	Project Name	Rev
Custom		2.0
Date: Friday, April 25, 2008		Sheet 89 of 101

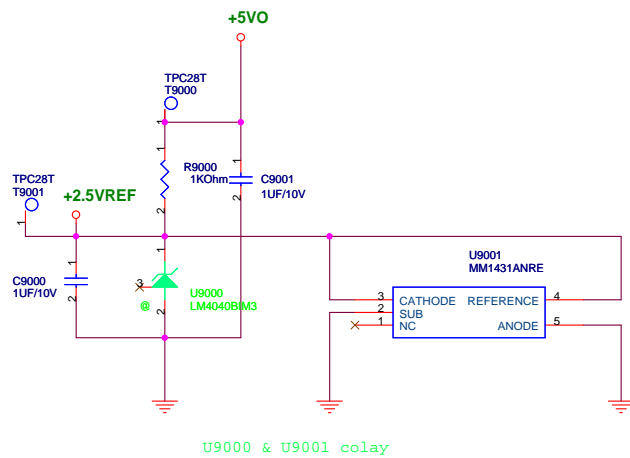
### BATTERY IN DETECT



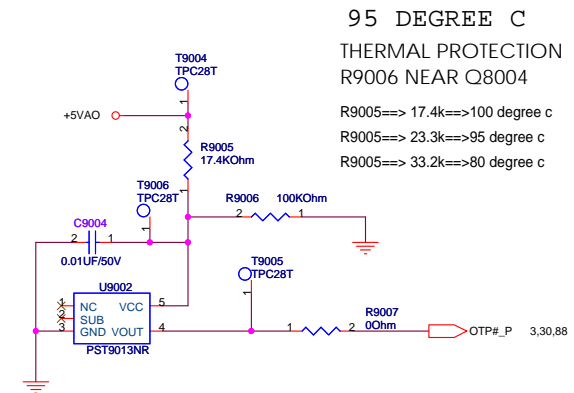
### ADAPTER IN DETECT



### +2.5VREF



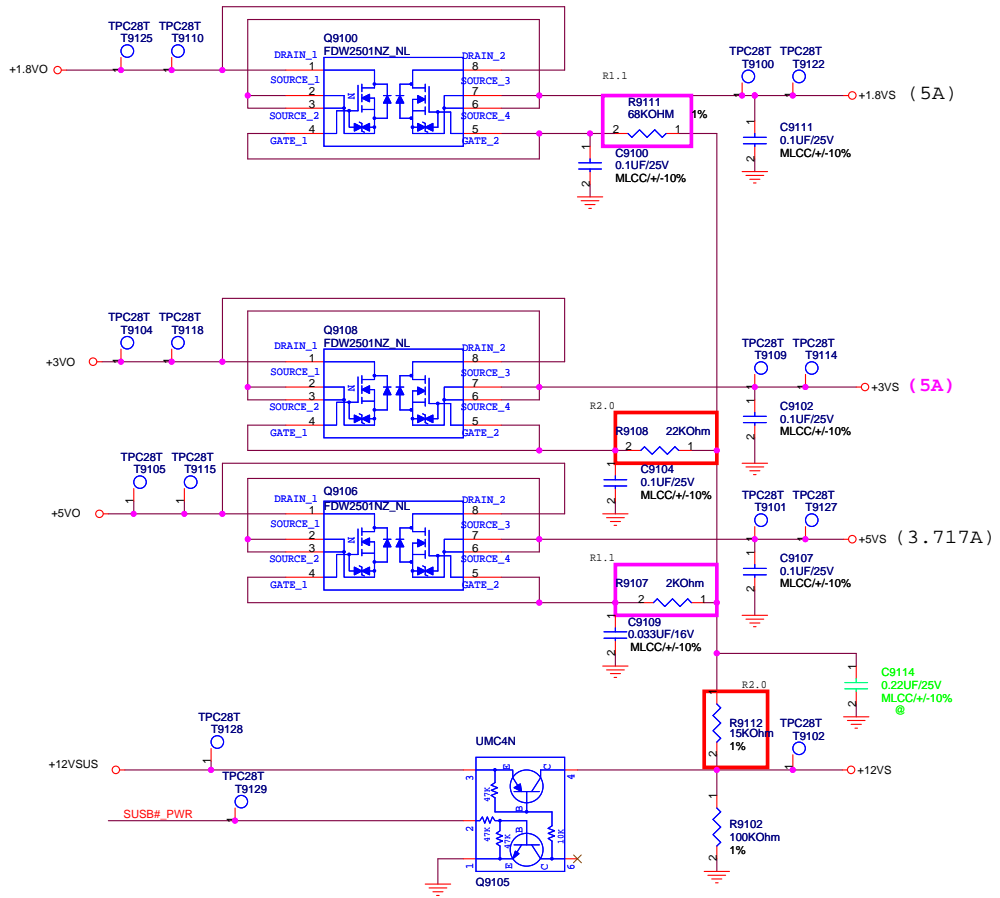
### THERMAL PROTECT



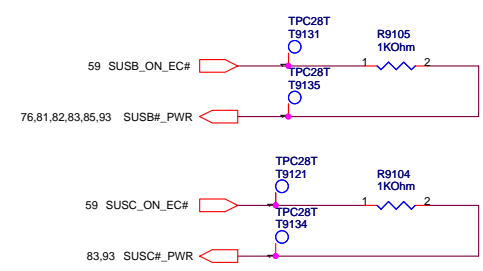
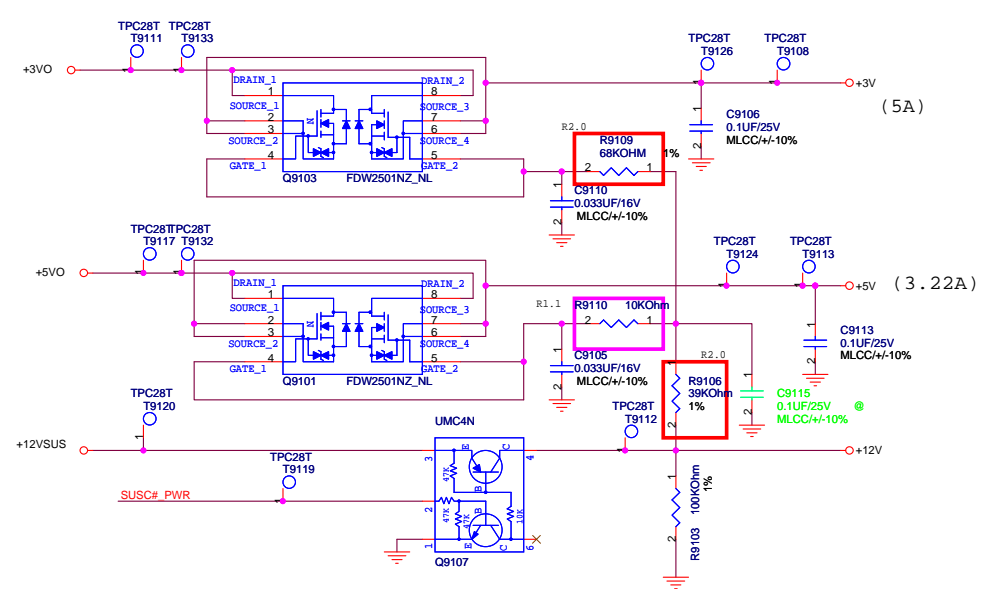
<Variant Name>

<b>ASUS</b>		<b>Title :POWER_DETECT</b>	
ASUSTeK COMPUTER INC. NB		Engineer: <b>Louis Lin</b>	
Size	Project Name	Rev	
Custom	U6V	2.0	
Date: Friday, April 25, 2008		Sheet	90 of 101

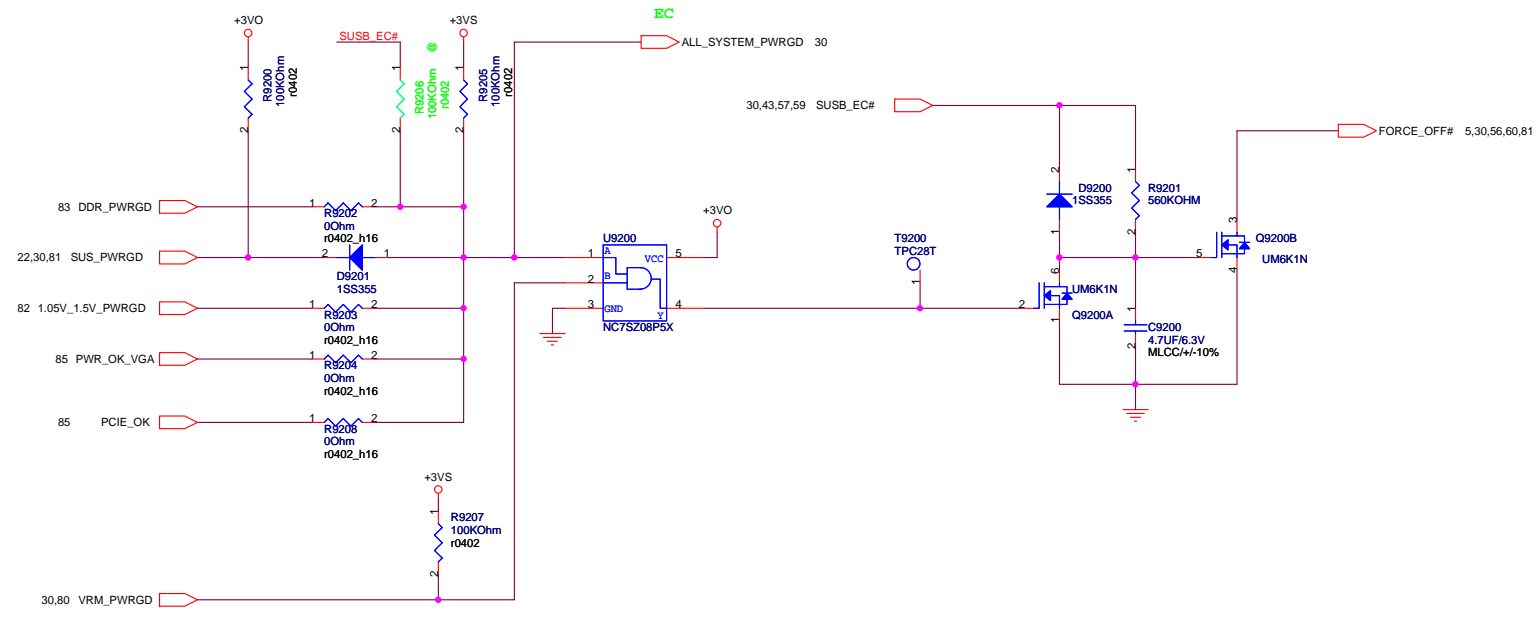
SUSB#\_PWR POWER

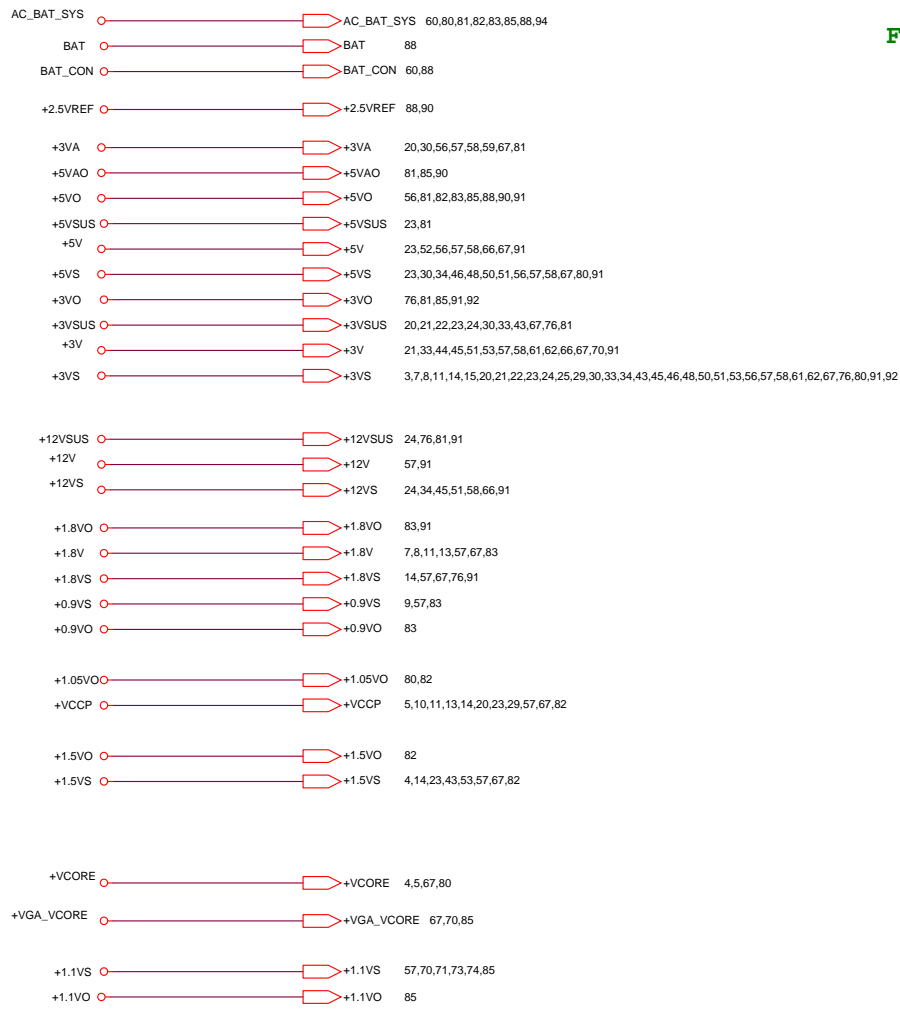


SUSC#\_PWR POWER

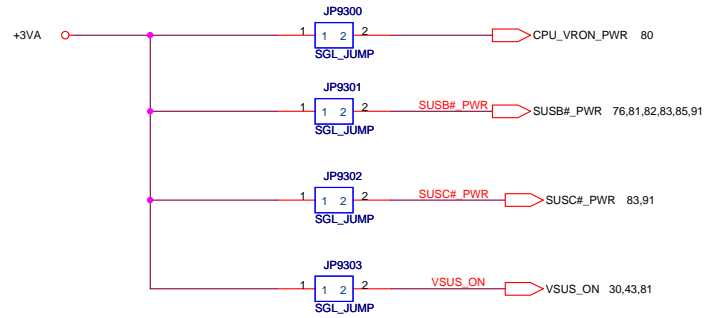


# POWER GOOD DETECTOR

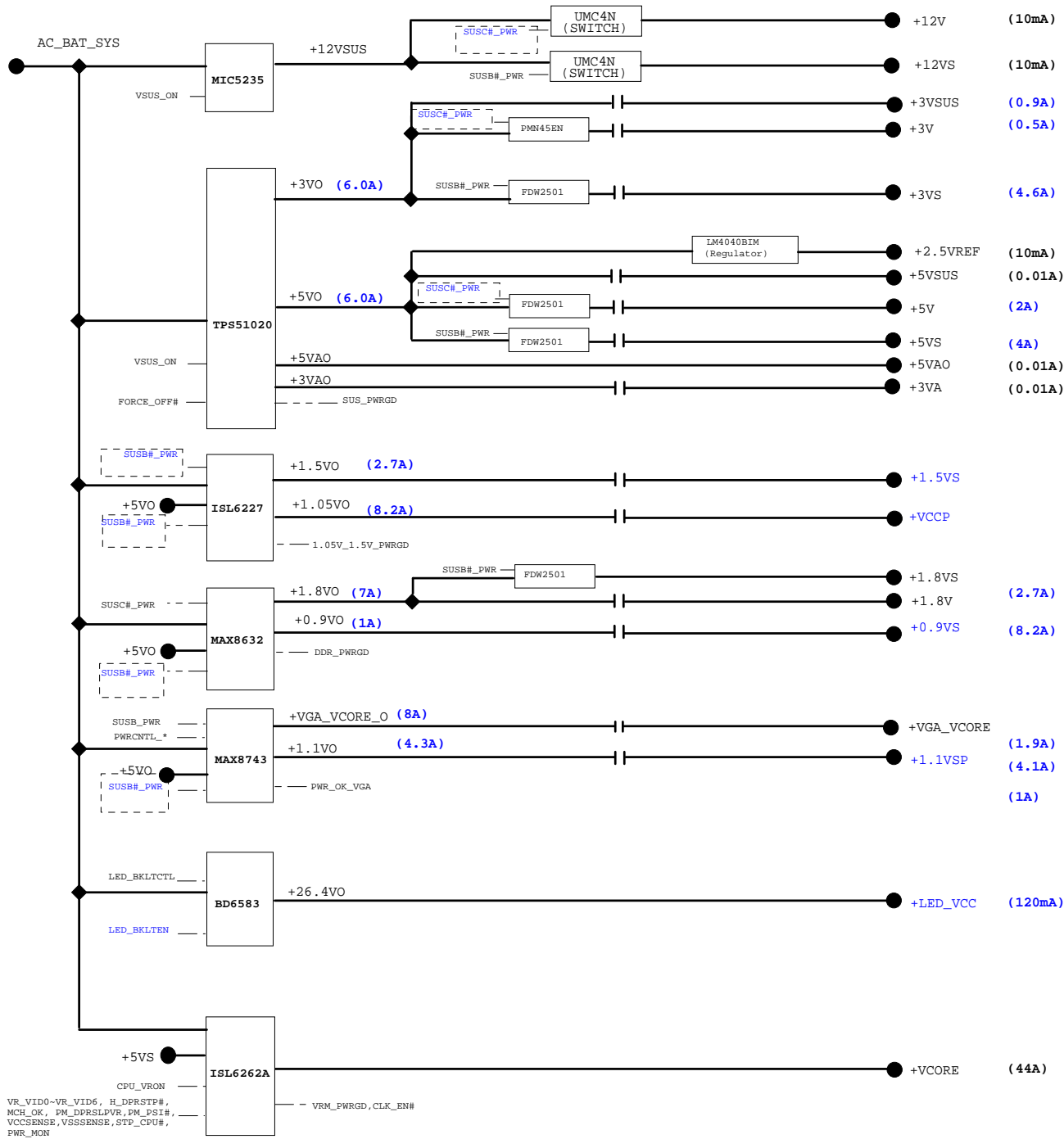




**FOR POWER TEST**







VR\_VID0-VR\_VID6, H\_DPRSTP#,  
MCH\_OK, PM\_DPRSLPVR, PM\_PSI#,  
VCCSENSE, VSSSENSE, STP\_CPU#,  
PWR\_MON





R2.0 DATE:04/11

- 1. Changing Q9400 from SI2318 to SI2308.
- 2. As below is EE suggestion.
  - a. R8504 from 33k change to 56k.
  - b. R8317 from 75k change to 100k.
  - c. R8208 from 56k change to 100k.
  - d. R8210 from 27k change to 56k.
  - e. R9106 from 27k change to 39k.
  - f. R9109 from 56k change to 68k.
  - g. R9108 from 18k change to 22k.
  - h. R9112 from 12k change to 15k.


R2.0 DATE:04/23

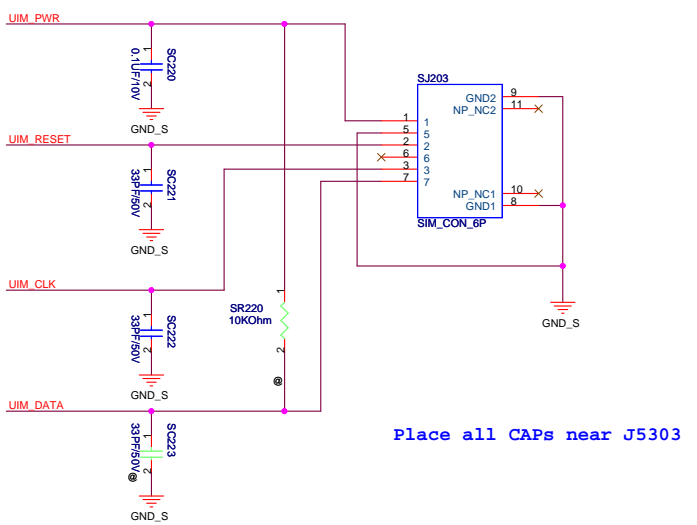
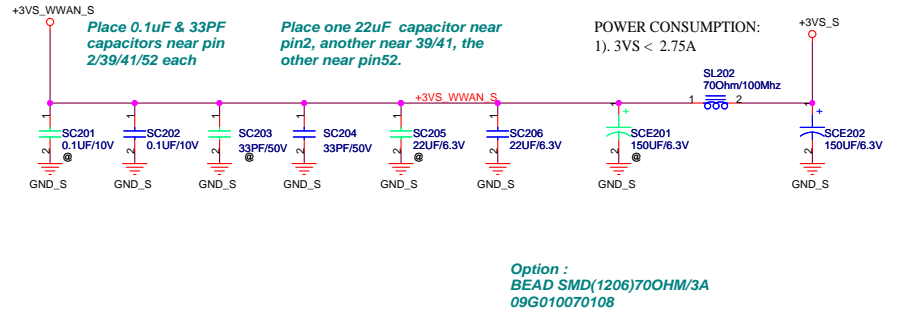
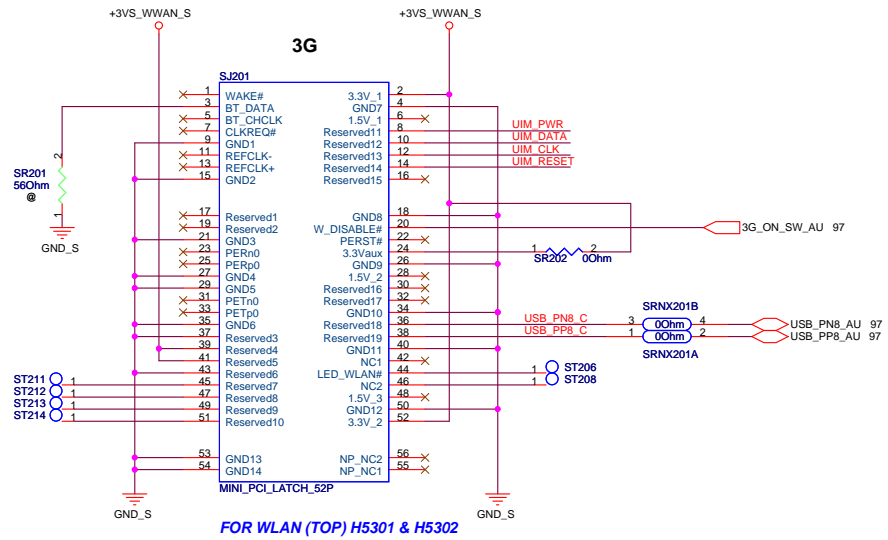
- 1. Changing R8504 Colay from 110k change to 82k, for VX3V series.

R2.0 DATE:04/25

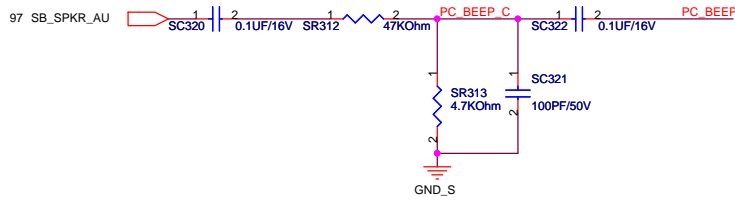
- 1. Unmount R8534 and R8535.

<Variant Name>

		<b>Title :</b> POWER_HISTORY
ASUSTeK COMPUTER INC. NB		<b>Engineer:</b> <i>Louis_Lin</i>
Size A	Project Name U6V	Rev 2.0
Date: Friday, April 25, 2008		Sheet 96 of 101

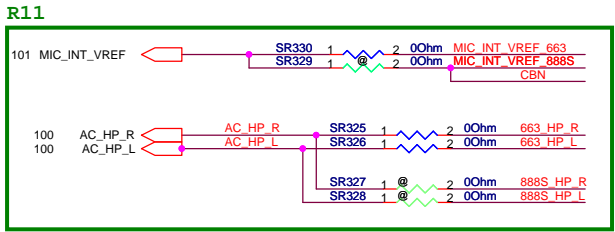
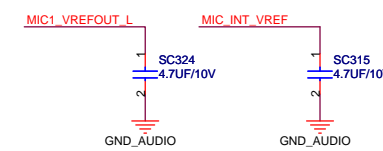
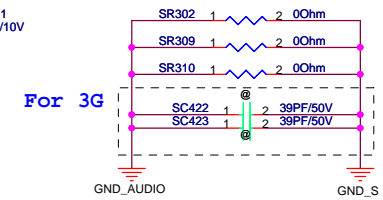
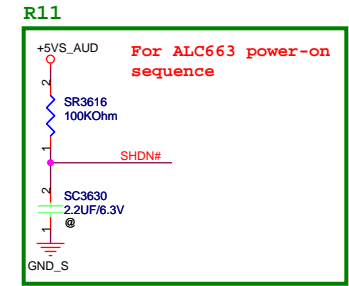
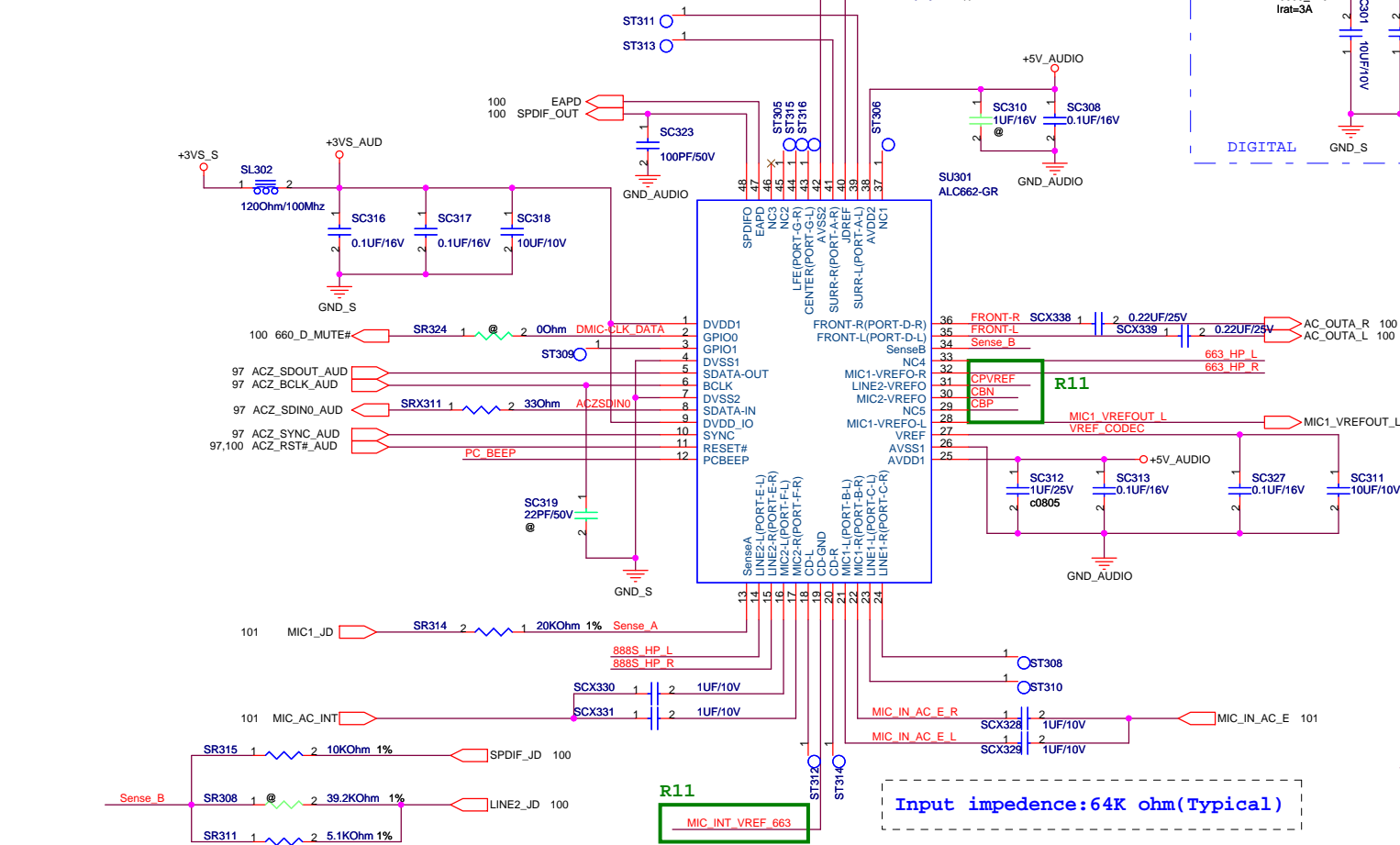
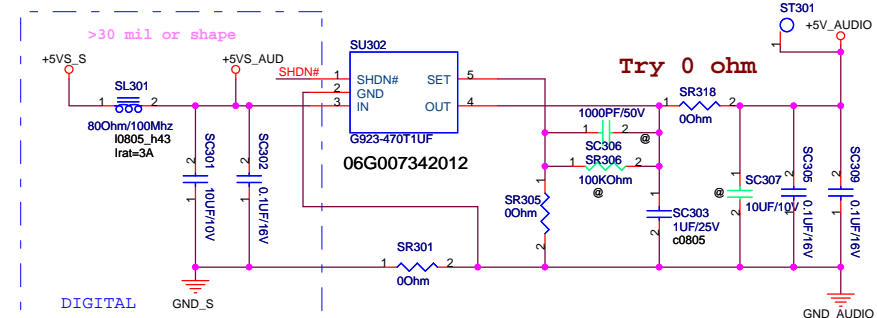


# PC BEEP



# Audio Power

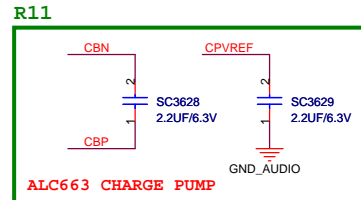
FOR ADJUST MODE:  
 $V_o = 1.25 * (1 + R_{3706} / R_{3705})$   
 $= 1.25 * (1 + 100K / 34.8K) = 4.84$



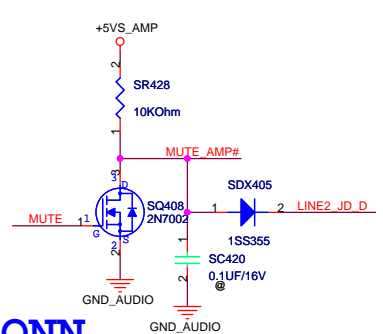
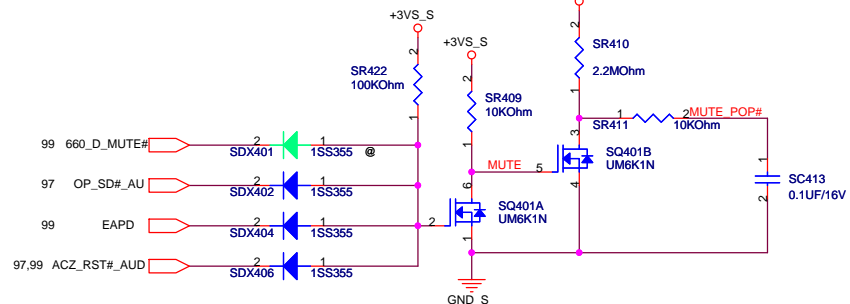
## Colay ALC663 & 888S

**ALC663**  
 Mount SR325, SR326 for Headphone  
 SR311 for jack sense  
 SC325 & SC326 for CHARGE PUMP  
 SR330 for Internal MIC

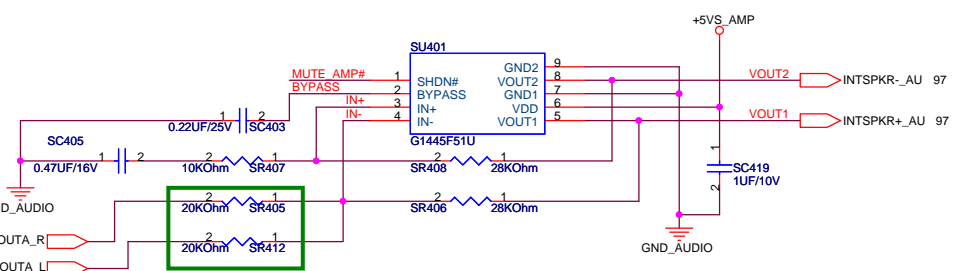
**ALC888S**  
 Mount SR327, SR328 for Headphone  
 SR308 for jack sense  
 SR329 for Internal MIC



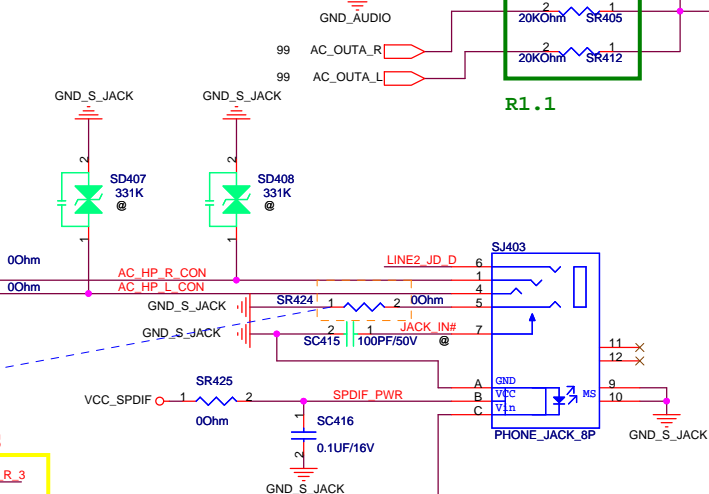
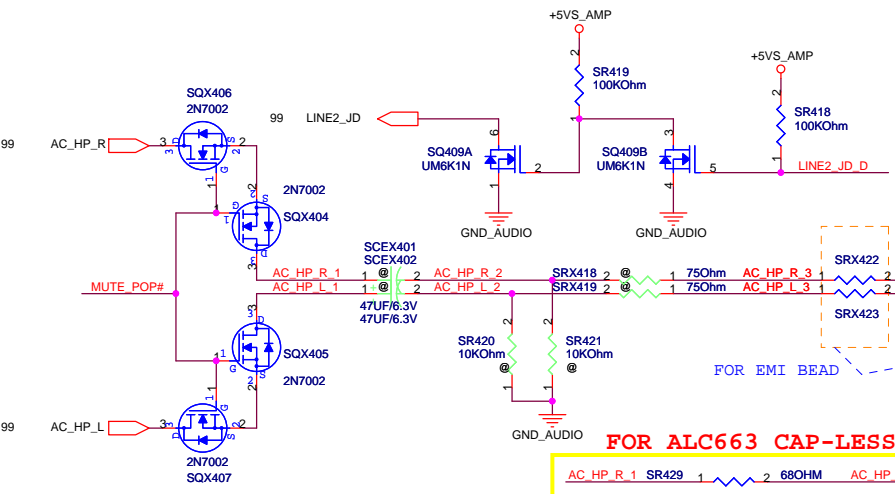
# MUTE CONTROL



2'nd source:  
TI/TPA6205A1DGNRG4, P/N: 06G045099110



# HP & SPDIF CONN



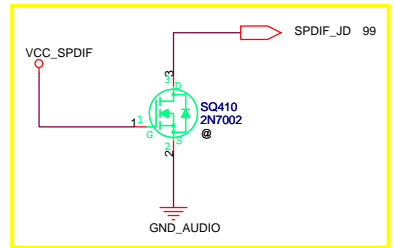
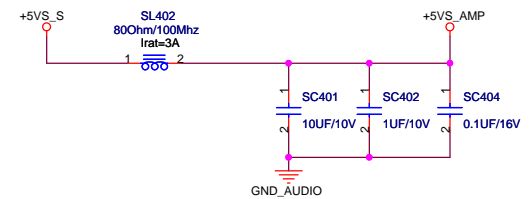
R1.1

FOR ALC663 CAP-LESS  
AC\_HP\_R\_1 SR429 1 680HM AC\_HP\_R\_3  
AC\_HP\_L\_1 SR430 1 680HM AC\_HP\_L\_3

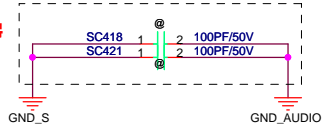
Colay ALC663 & 8885  
ALC663  
Mount SR429, SR430 for CAP less

ALC8885  
Mount SCEX401, SR420, SRX418  
SCEX402, SR421, SRX419

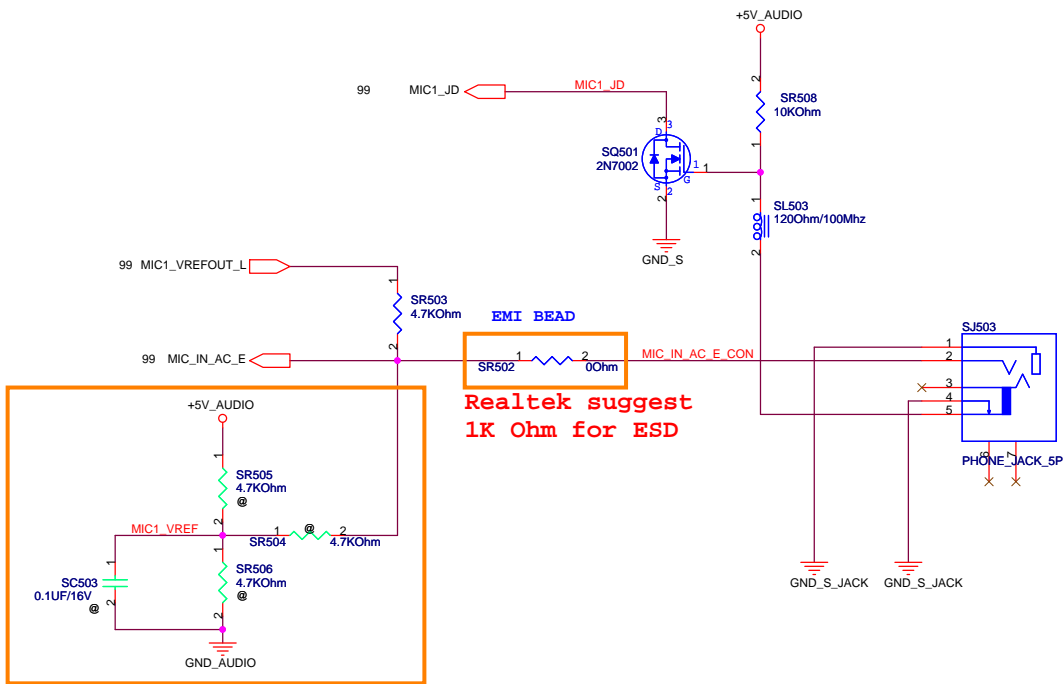
Removed the SPDIF power control signal. When HP jack sense enable, the driver must turn off the SPDIF.



For 3G



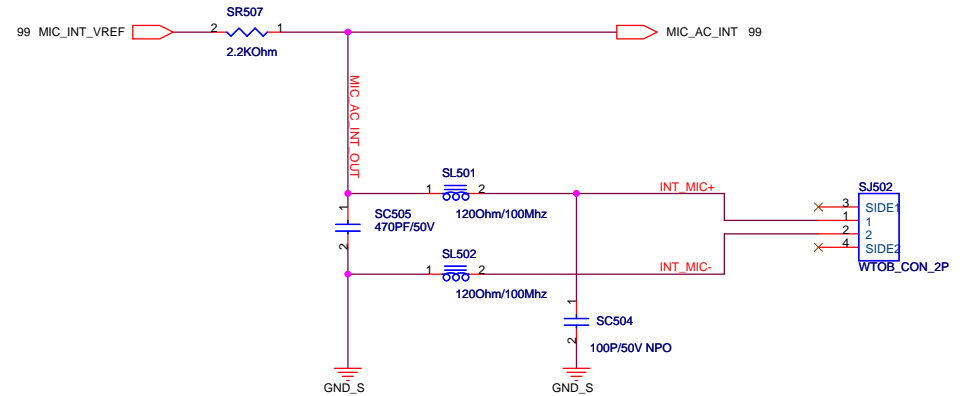
# EXTERNAL MICROPHONE



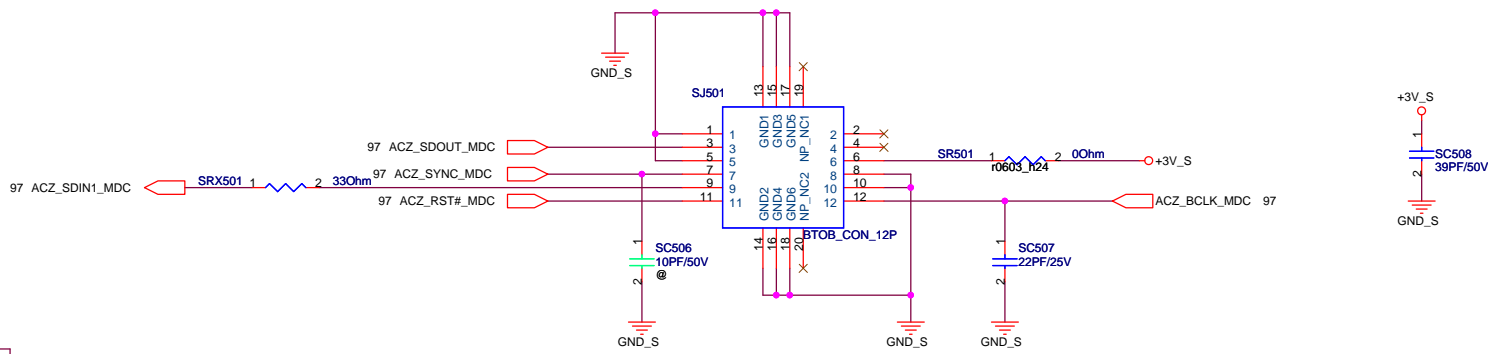
Realtek suggest  
1K Ohm for ESD

Reserved the external MIC  
bias(T filter).

# INTERNAL MICROPHONE



# MODEM



FOR MDC (TOP) H3501 & H3502

