

PROJECT U5A

Revision History

R1.0	SR	2005/05/17
R1.1	ER	2005/08/04
R2.0	PR	2005/10/07

SMB Signals

Host	Name	Devices	Address
Chipset	SMBCK, SMBDA	ICH6-M ADT7473(Thermal) ICS954213(Clock Genertor) DDR2 SO-DIMM	10h 2Eh D2h A0h

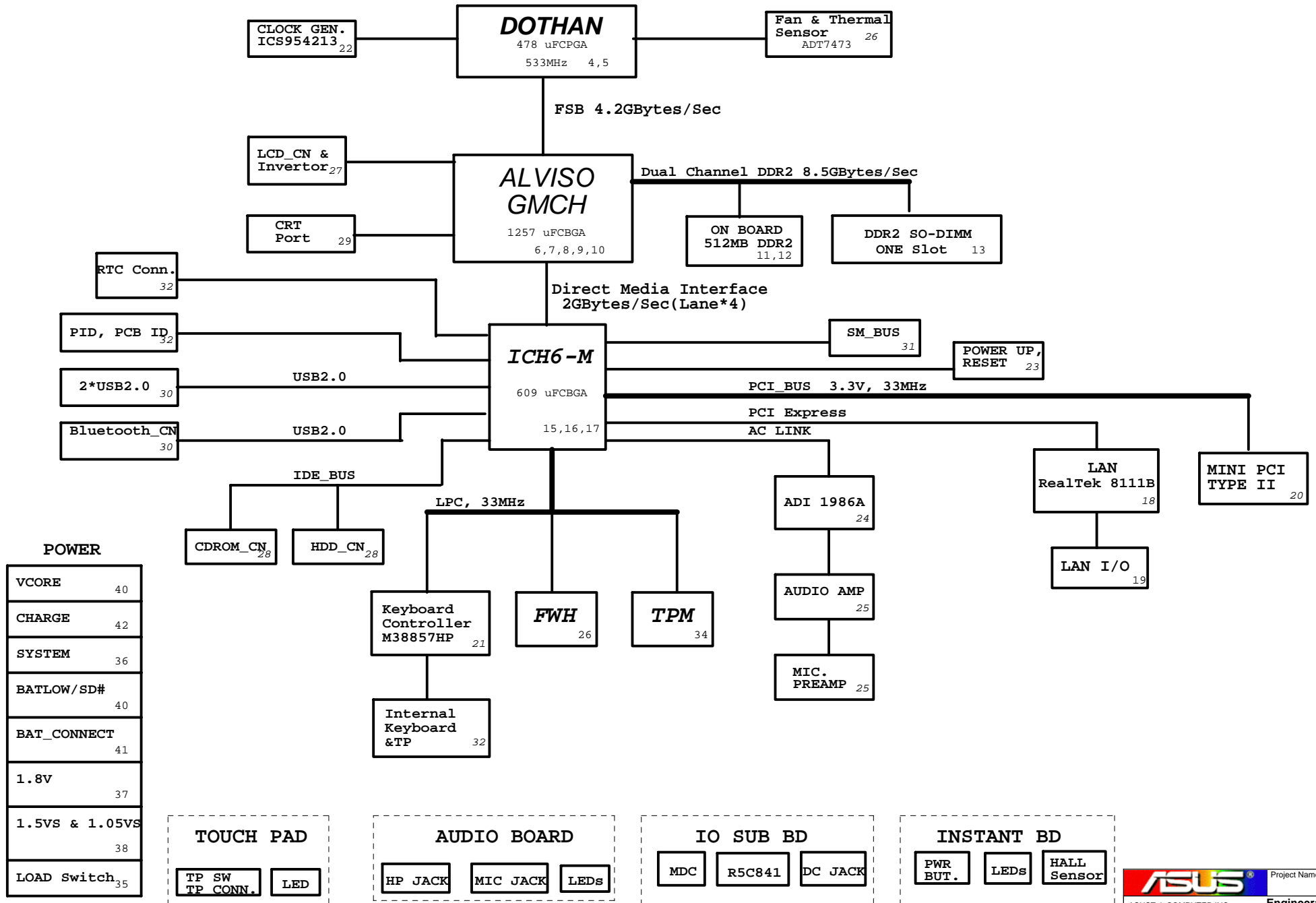
Power States

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#	++VALWAYS	++V	++VS	Clocks
Full ON	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3(Suspend to RAM)	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5/Sort OFF	LOW	LOW	LOW	ON	OFF	OFF	OFF

PCI Devices

Bus#	Device#	Function#	REQ/GNT#	IDSEL	APIC Interrupts	Device Function
Bus0	Device00	Function0				Intel 915GM Host Bridge / DRAM Controller
Bus0	Device01	Function0				Intel 915GM Virtual PCI to PCI
Bus0	Device02	Function0				Intel 915GM GMCH Integrated Graphics Device
Bus0	Device27	Function0				Azalia Controller
Bus0	Device28	Function0				PCI Express Port1
Bus0	Device28	Function1				PCI Express Port2
Bus0	Device28	Function2				PCI Express Port3
Bus0	Device28	Function3				PCI Express Port4
Bus0	Device29	Function0			A#	Intel UHCI USB Controller
Bus0	Device29	Function1			D#	Intel UHCI USB Controller
Bus0	Device29	Function2			C#	Intel UHCI USB Controller
Bus0	Device29	Function3			A#	Intel UHCI USB Controller
Bus0	Device29	Function7			H#	Intel EHCI USB Controller
Bus0	Device30	Function0				PCI to PCI Bridge
Bus0	Device30	Function2			B#	Intel Audio Controller
Bus0	Device30	Function3			B#	Intel Modem Controller
Bus0	Device31	Function0				Intel PCI-to-LPC Bridge
Bus0	Device31	Function1			C#	Intel IDB Controller
Bus0	Device31	Function2				SATA Controller
Bus1	Device03	Function0	2	AD19	F#	CardBus Bridge
Bus1	Device03	Function1	2	AD19	G#	IEEE 1394
Bus1	Device03	Function2	2	AD19	E#	SD Card Interface
Bus1	Device03	Function3	2	AD19	E#	Memory Stick Interface
Bus1	Device03	Function4	2	AD19	E#	xD Picture Card Interface
Bus1	Device04	Function0	1	AD20	E#	Ethernet Controller
Bus1	Device05	Function0	3	AD21	C#/D#	Mini PCI

DOTHAN/ALVISO-GM BLOCK DIAGRAM



POWER	
VCORE	40
CHARGE	42
SYSTEM	36
BATLOW/SD#	40
BAT_CONNECT	41
1.8V	37
1.5VS & 1.05VS	38
LOAD Switch	35

TOUCH PAD

TP SW

TP CONN.

LED

AUDIO BOARD

HP JACK

MIC JACK

LEDs

IO SUB BD

MDC

R5C841

DC JACK

INSTANT BD

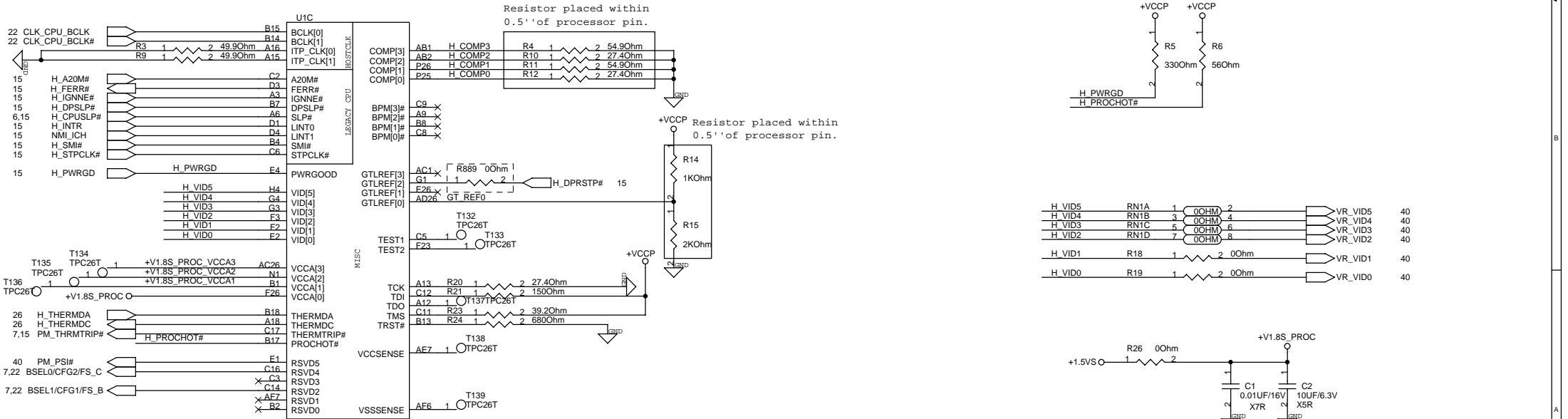
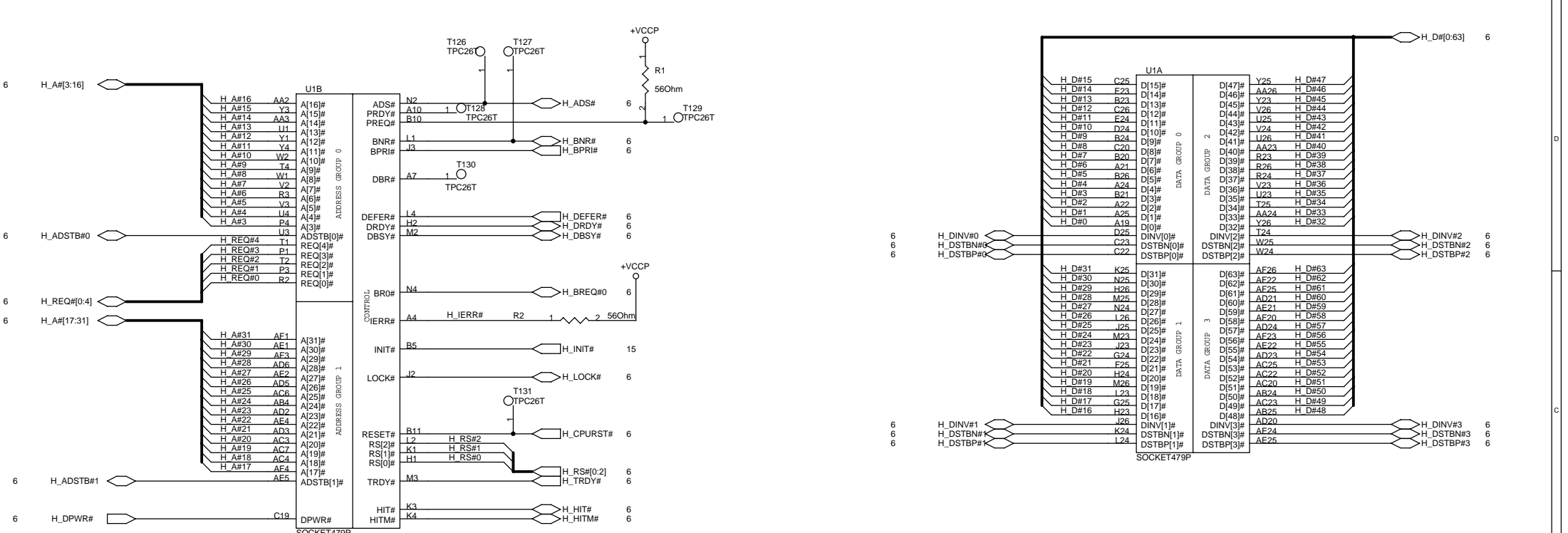
PWR BUT.

LEDs

HALL Sensor

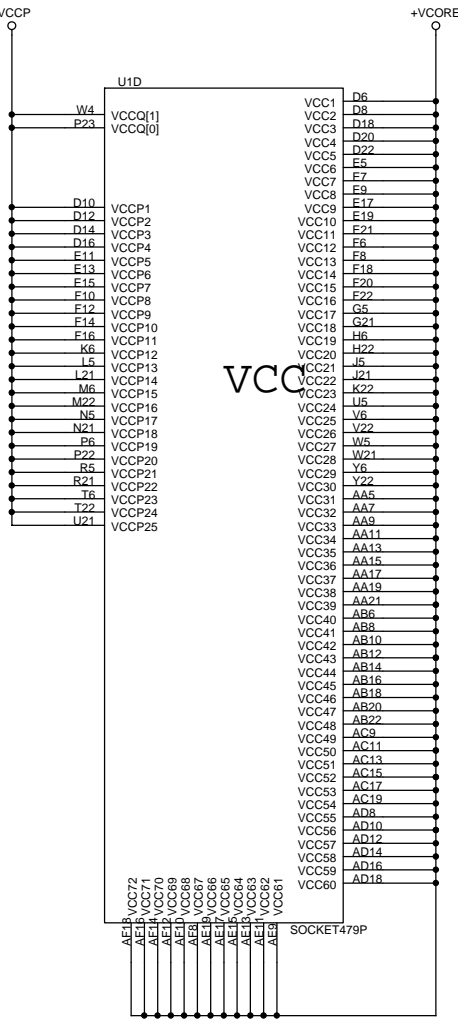
M38857MB_GPIO	Use As	Signal Name	Description
P20	GPO	ANKEY_RSM	Anykey wakeup
P21			
P22	GPO	BAT_LEARN	Switch AC power on or off
P23	GPO	802_ON#	Notify wireless LED status change
P27	GPO	SCROLLOCK#_3	
P42	GPO		
P43	GPI	LID_RSM#	Notify LID switch status
P44	GPO	KBDCPURST_3Q	
P45	GPO	A20GATE_3Q	
P46	GPO	KBDSMCI_3Q	Trigger EC's SCI event
P47	GPIO	CLKRUN#_3	
P50	GPI	BAT_LLOW#_OC	Battery low event
P51			
P52	GPO		
P53	GPO	BTPWRCL#	Control Bule Tooth on/off
P54	GPI	BAT_TYPE_3S1P#	Show battery type
P55	GPI	BAT_IN#_OC	Battery IN/OUT event
P56	GPO	CODEC_SHDN#	Switch CODEC power on/off
P57	GPO	TPD_LED_OFF#	Switch TPD LED on/off
P67	GPO	WIRELESS_LAN_ON#	Control wireless LAN module on/off
P66	GPI	BAT_SAVING#	
P65			
P64	GPI	ACIN_OC	AC IN / OUT event
P63	GPO		
P62	GPI	CHG_FULL_OC	End of charger status
P61			
P60			
P77	GPO	SMC_BAT	
P76	GPIO	SMD_BAT	
P26	GPI	KBNUM#_3	Notify NUM key status change
P25	GPI	KBCAP#_3	Notify CAP key status change
P24	GPO	PCIRST#_GATE	Block PCIRST# during S3 resume
P40			

ICH6_GPIO	Use As	Signal Name
GPI7	GPI	MEMORY_FREQ
GPI8	GPI	EXTSMI#
GPI11	GPI	LID_RSM#
GPI12	GPI	KB_SCI#
GPI13	GPI	
GPO18	GPO	STP_PCI#
GPO19	GPO	PWRLED_1HZ
GPO21		
GPO23	GPO	FWH_WP#
GPIO25	GPO	CB_SD#
GPIO27	GPI	PCB_ID0
GPIO28	GPI	PCB_ID1
GPI40	GPI	PANEL__ID0
GPI41	GPI	PANEL__ID1

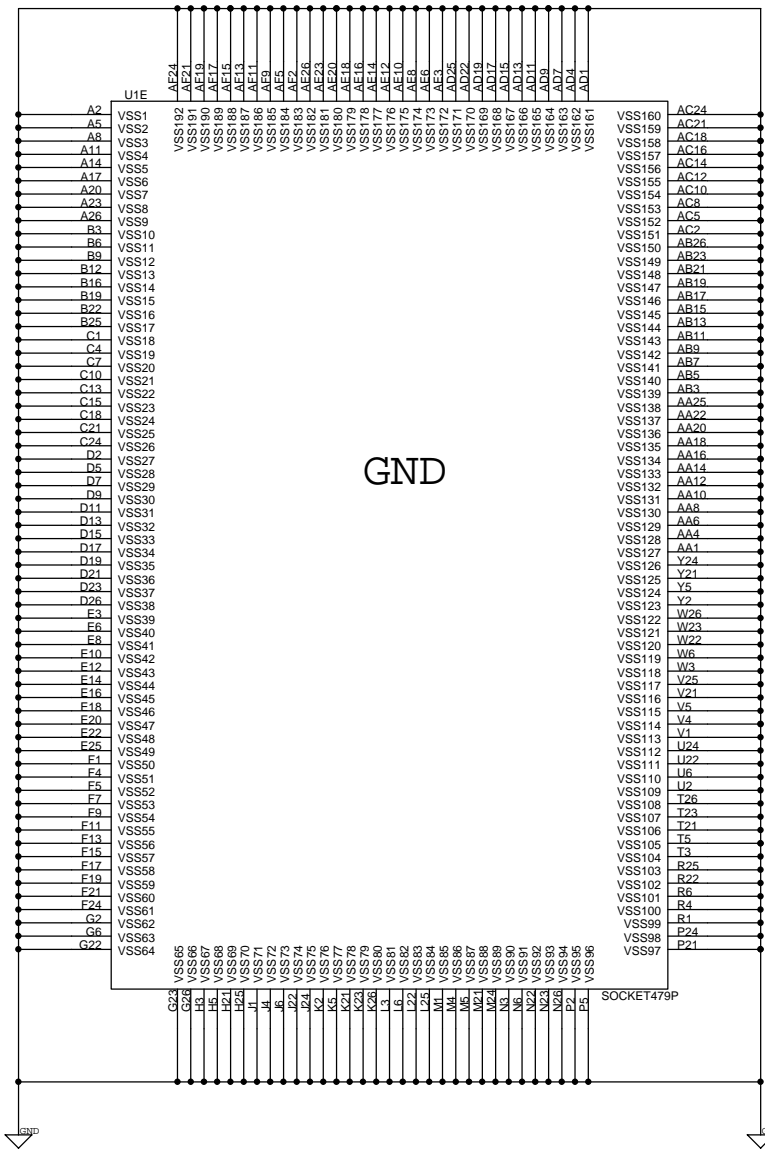


FSB	BSEL1	BSEL0
400	0	1
533	0	0

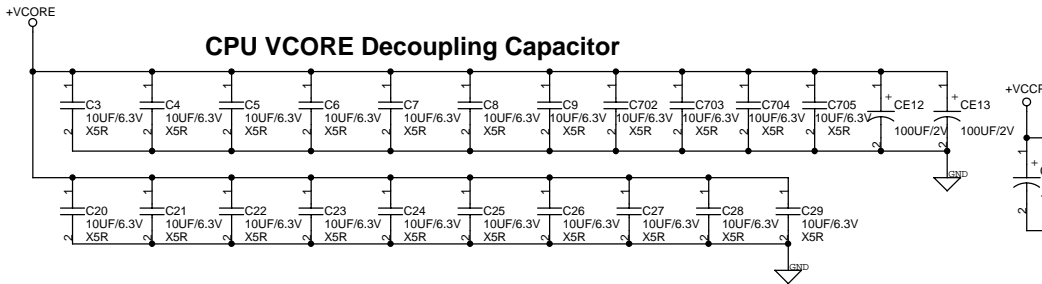
1.0V - 1.2V(+/- 5%)
SO-S1M: 2.5
A(CPU,MCH,ICH)



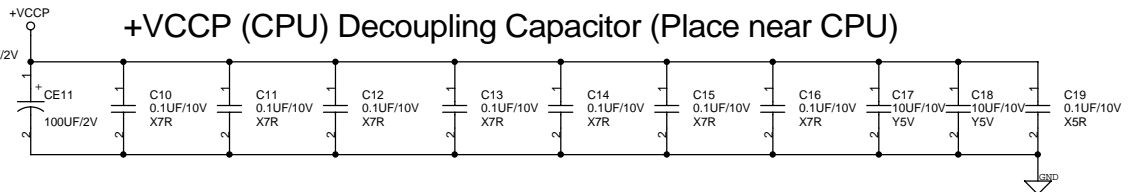
0.745V - 1.356V(+/- 1.5%)
C0: 27 A
C3: 7.59A
C4: 0.9A

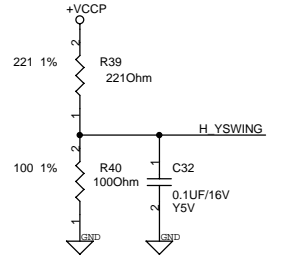
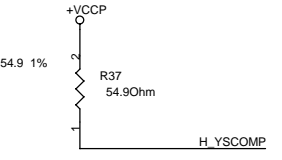
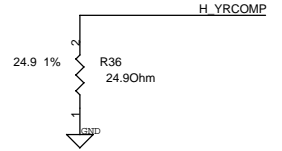
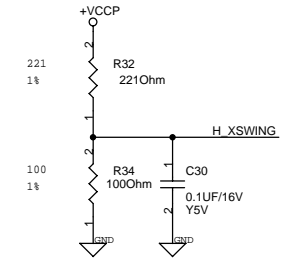
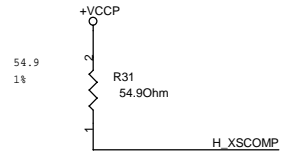
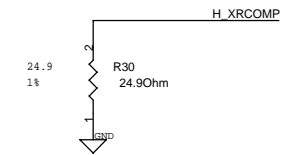


CPU VCORE Decoupling Capacitor



+VCCP (CPU) Decoupling Capacitor (Place near CPU)





4 H_D# [0..63]

H_D#0	F4	HD0#
H_D#1	F1	HD1#
H_D#2	F4	HD2#
H_D#3	H7	HD3#
H_D#4	E2	HD4#
H_D#5	F1	HD5#
H_D#6	F3	HD6#
H_D#7	D3	HD7#
H_D#8	K7	HD8#
H_D#9	F2	HD9#
H_D#10	J7	HD10#
H_D#11	J8	HD11#
H_D#12	H6	HD12#
H_D#13	F3	HD13#
H_D#14	K8	HD14#
H_D#15	H5	HD15#
H_D#16	H1	HD16#
H_D#17	H2	HD17#
H_D#18	K5	HD18#
H_D#19	K6	HD19#
H_D#20	J4	HD20#
H_D#21	G3	HD21#
H_D#22	H3	HD22#
H_D#23	J1	HD23#
H_D#24	L5	HD24#
H_D#25	K4	HD25#
H_D#26	J5	HD26#
H_D#27	P7	HD27#
H_D#28	L7	HD28#
H_D#29	J3	HD29#
H_D#30	P5	HD30#
H_D#31	L3	HD31#
H_D#32	U7	HD32#
H_D#33	V6	HD33#
H_D#34	R6	HD34#
H_D#35	R5	HD35#
H_D#36	P3	HD36#
H_D#37	T8	HD37#
H_D#38	R7	HD38#
H_D#39	R8	HD39#
H_D#40	U8	HD40#
H_D#41	R4	HD41#
H_D#42	T4	HD42#
H_D#43	T5	HD43#
H_D#44	R1	HD44#
H_D#45	T3	HD45#
H_D#46	V8	HD46#
H_D#47	U6	HD47#
H_D#48	W6	HD48#
H_D#49	U3	HD49#
H_D#50	V5	HD50#
H_D#51	W8	HD51#
H_D#52	W7	HD52#
H_D#53	U2	HD53#
H_D#54	U1	HD54#
H_D#55	Y5	HD55#
H_D#56	Y6	HD56#
H_D#57	V4	HD57#
H_D#58	Y7	HD58#
H_D#59	W1	HD59#
H_D#60	W3	HD60#
H_D#61	Y3	HD61#
H_D#62	Y6	HD62#
H_D#63	W2	HD63#

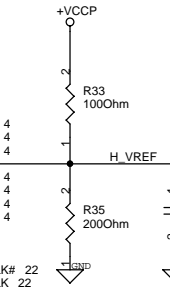
H_XRCOMP	C1	HXRCOMP
H_XSCOMP	C2	HXSCOMP
H_XSWING	D1	HXSWING
H_YRCOMP	T1	HYRCOMP
H_YSCOMP	L1	HYSCOMP
H_YSWING	P1	HYSWING

U2D

HA3#	G9	H_A#3
HA4#	C9	H_A#4
HA5#	F9	H_A#5
HA6#	B7	H_A#6
HA7#	A10	H_A#7
HA8#	F9	H_A#8
HA9#	D8	H_A#9
HA10#	B10	H_A#10
HA11#	E10	H_A#11
HA12#	G10	H_A#12
HA13#	D9	H_A#13
HA14#	F11	H_A#14
HA15#	F10	H_A#15
HA16#	G11	H_A#16
HA17#	G13	H_A#17
HA18#	C10	H_A#18
HA19#	C11	H_A#19
HA20#	D11	H_A#20
HA21#	C12	H_A#21
HA22#	B13	H_A#22
HA23#	A12	H_A#23
HA24#	F12	H_A#24
HA25#	G12	H_A#25
HA26#	E12	H_A#26
HA27#	C13	H_A#27
HA28#	B11	H_A#28
HA29#	D13	H_A#29
HA30#	A13	H_A#30
HA31#	F13	H_A#31

HOST

HADS#	F8	H_ADS#	4
HADSTB0#	B9	H_ADSTB#0	4
HADSTB1#	E13	H_ADSTB#1	4
HADSTB1#	H11	H_ADSTB#1	4
HVREF	A5	H_BNR#	4
HBNR#	D5	H_BPR#	4
HBREQ0#	E7	H_BREQ#0	4
HCPURST#	H10	H_CPURST#	4
HCLKINN	AB1	CLK_MCH_BCLK# 22	22
HCLKINP	AB2	CLK_MCH_BCLK# 22	22
HDBSY#	C6	H_DBSY#	4
HDEFER#	F6	H_DEFER#	4
HDINV0#	HR	H_DINV#0	4
HDINV1#	K3	H_DINV#1	4
HDINV2#	T7	H_DINV#2	4
HDINV3#	U5	H_DINV#3	4
HDPWR#	G6	H_DPWR#	4
HDRDY#	E7	H_DRDY#	4
HDSTBN0#	G4	H_DSTBN#0	4
HDSTBN1#	K1	H_DSTBN#1	4
HDSTBN2#	R3	H_DSTBN#2	4
HDSTBN3#	V3	H_DSTBN#3	4
HDSTBP0#	G5	H_DSTBP#0	4
HDSTBP1#	K2	H_DSTBP#1	4
HDSTBP2#	R2	H_DSTBP#2	4
HDSTBP3#	W4	H_DSTBP#3	4
HEDRDY#	F6	TP_H_EDRDY#	4
HHIT#	D4	H_HIT#	4
HHITM#	D6	H_HITM#	4
HLOCK#	B3	H_LOCK#	4
HPCREQ#	A11	TP_H_PCREQ#	4
HREQ0#	A7	H_REQ#0	4
HREQ1#	D7	H_REQ#1	4
HREQ2#	B8	H_REQ#2	4
HREQ3#	C7	H_REQ#3	4
HREQ4#	A8	H_REQ#4	4
HRS0#	A4	H_RS#0	4
HRS1#	C5	H_RS#1	4
HRS2#	B4	H_RS#2	4
HCPUSLP#	GR R38	1 0 VTY 2	4,15
HTRDY#	B5	H_TRDY#	4

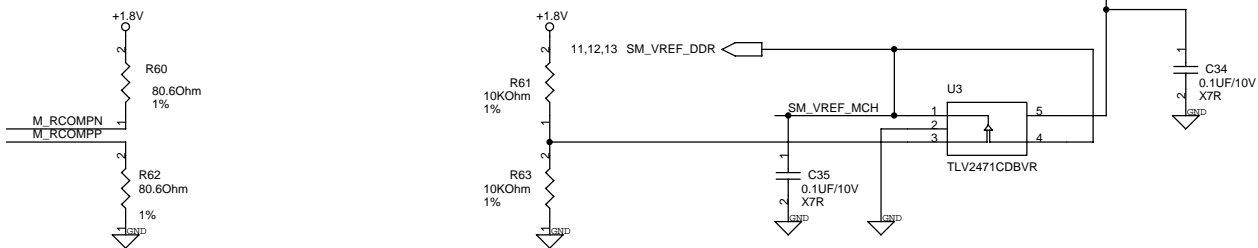
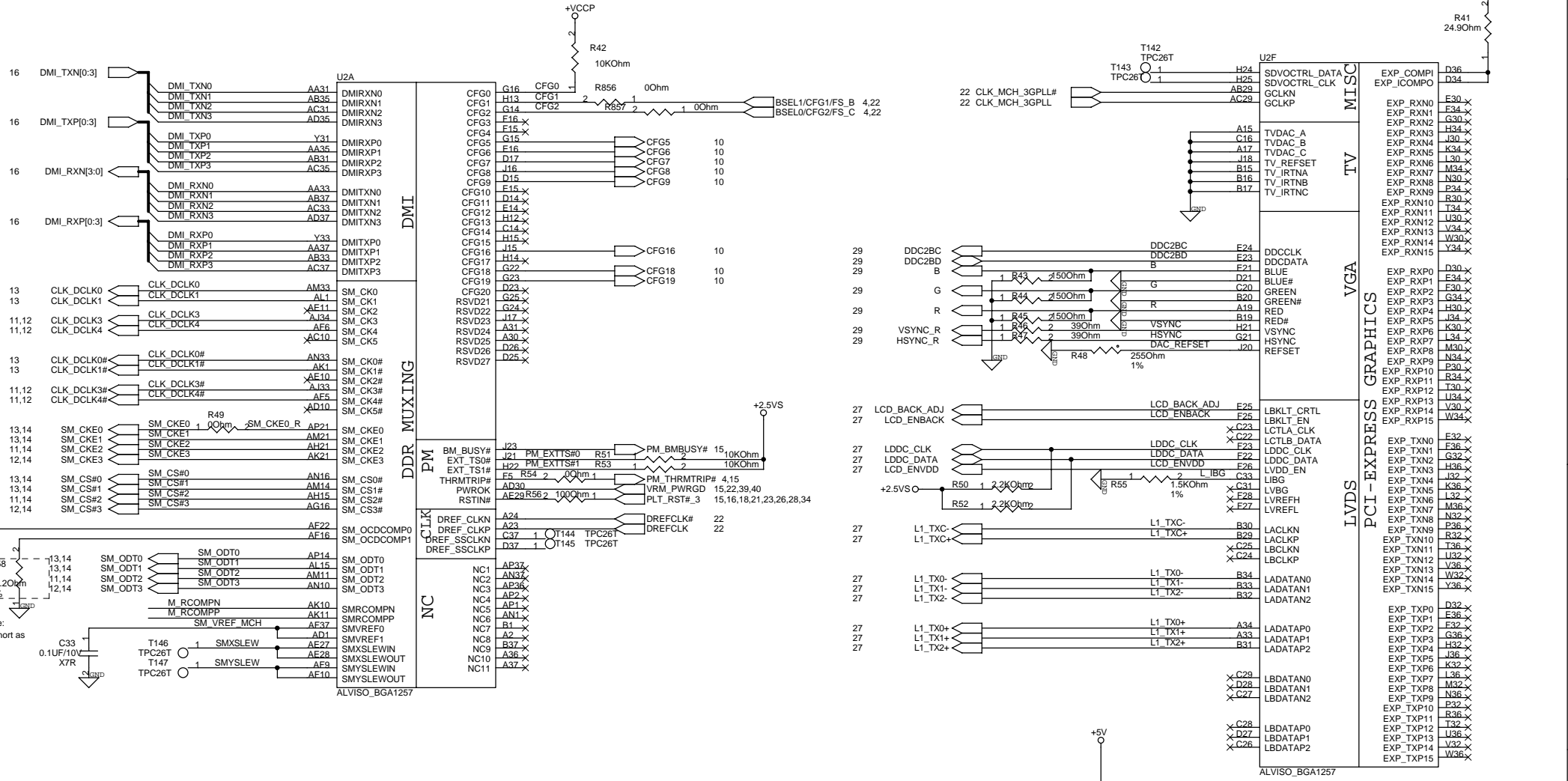


Cap should be placed 100 mils or less from GMCH pin.

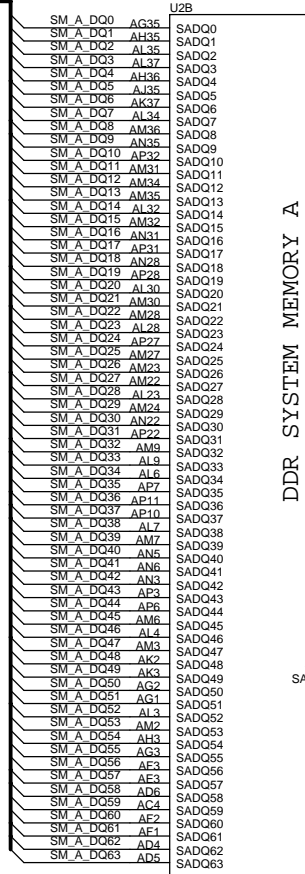
CFG[2:0]

001 = 533 MT/S (533MHz) FSB

101 = 400 MT/S (400MHz) FSB

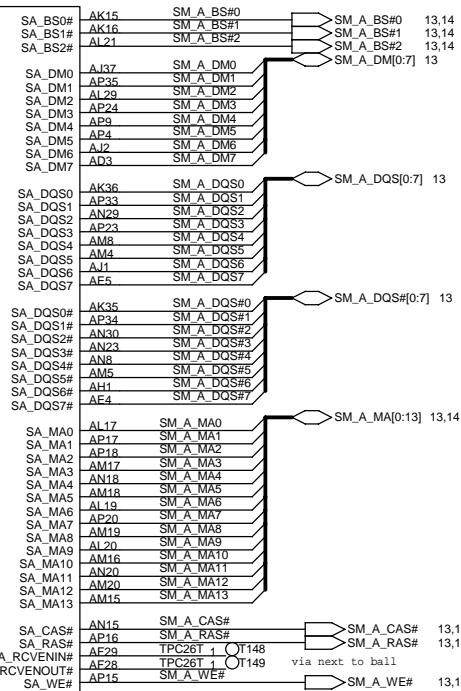


13 SM_A_DQ[0:63]

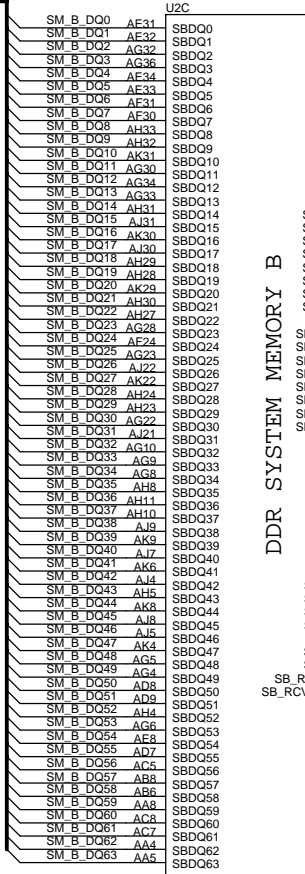


ALVISO_BGA1257

DDR SYSTEM MEMORY A

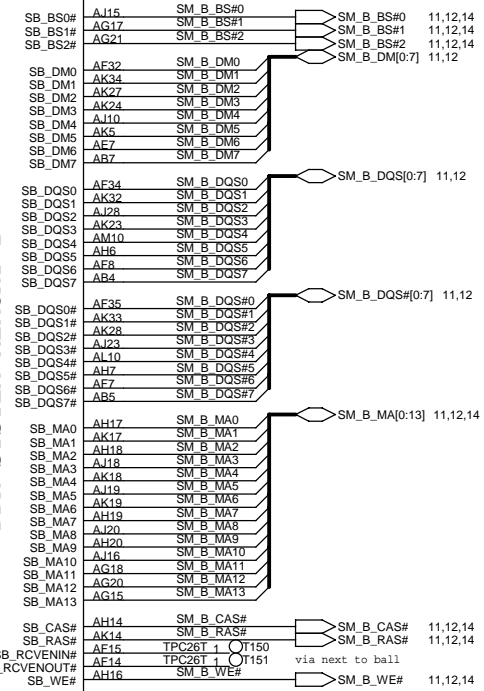


11,12 SM_B_DQ[0:63]

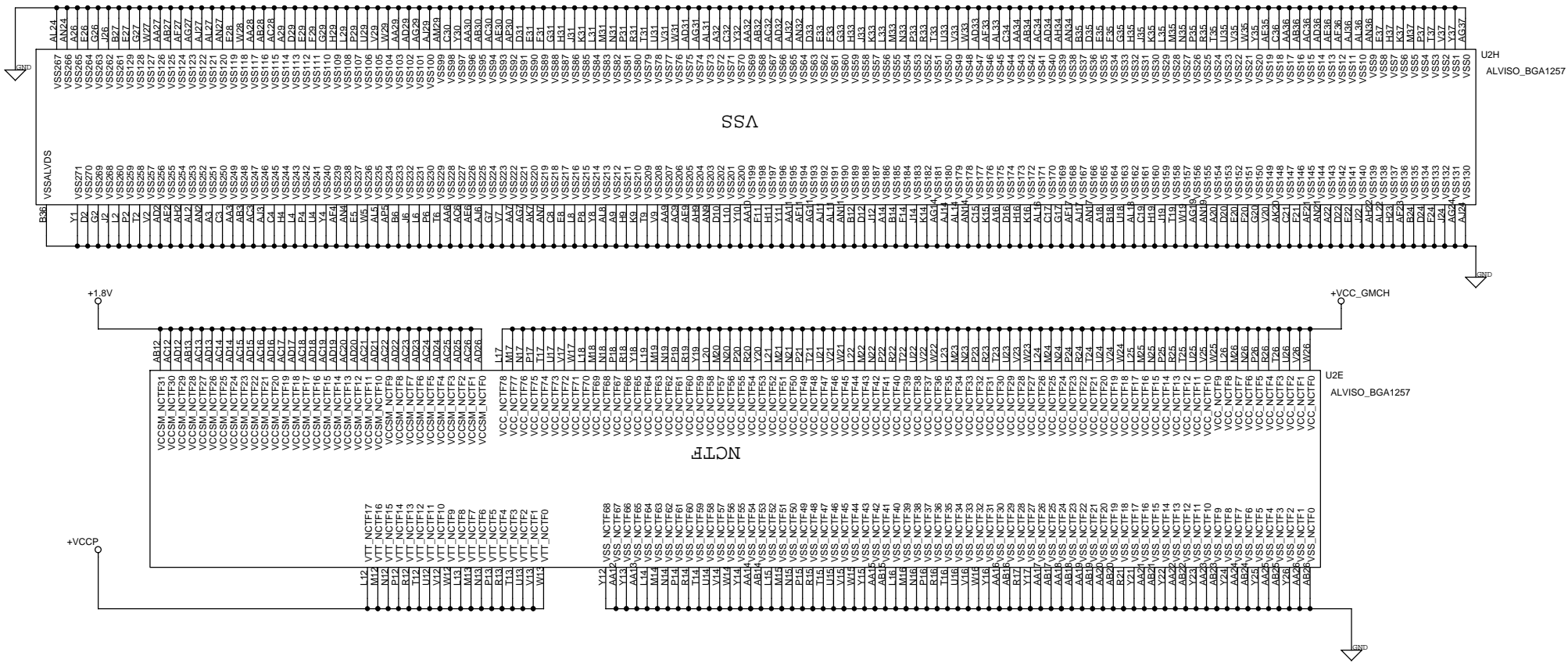


ALVISO_BGA1257

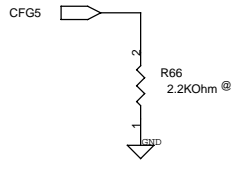
DDR SYSTEM MEMORY B



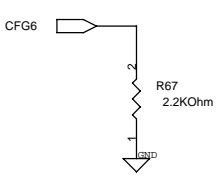
		Project Name	USA
ASUSTek COMPUTER INC		Engineer:	HF Lin
Size	Custom	Title :	ALVISO (3) -- DDR2 INTERFACE
Date:	Tuesday, September 27, 2005	Sheet	8 of 46
Rev	2.0		



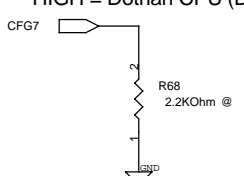
CFG5 : LOW = DMI X 2
HIGH = DMI X 4 (Default)



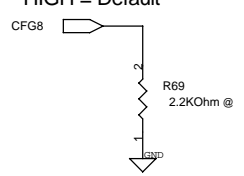
CFG6 : LOW = DDR2 SDRAM
HIGH = DDR SDRAM (Default)



CFG7 : CPU STRAP
LOW = Mobile Prescott
HIGH = Dothan CPU (Default)



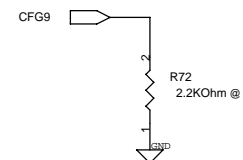
CFG8 : PCI-X POWER SAVING
LOW = PCI-X Power Saving
HIGH = Default



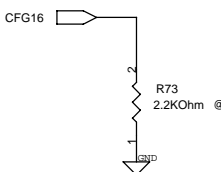
CFG[17..3] have internal pullup resistors.
CFG[19..18] have internal pulldown resistors.

SDVOCTRL_DATA LOW = No SDVO device present (Default)

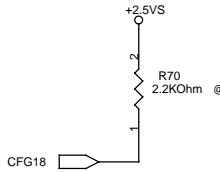
CFG9 : PCIE GRAPHIC LANE
LOW = REVERSE LANE
HIGH = NORMAL OPERATION (Default)



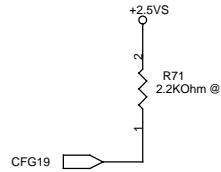
CFG16 : FSB DYNAMIC ODT
LOW = Dynamic ODT Disabled
HIGH = Dynamic ODT Enabled (Default)

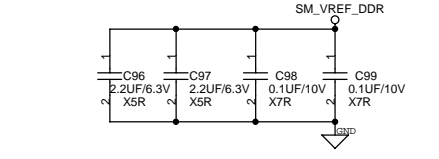
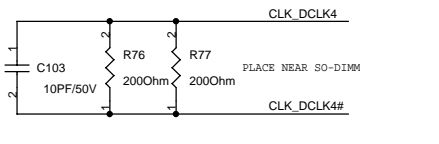
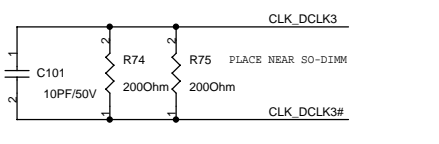
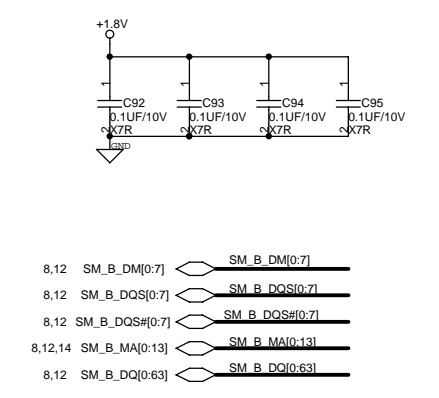
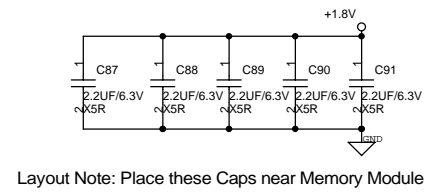
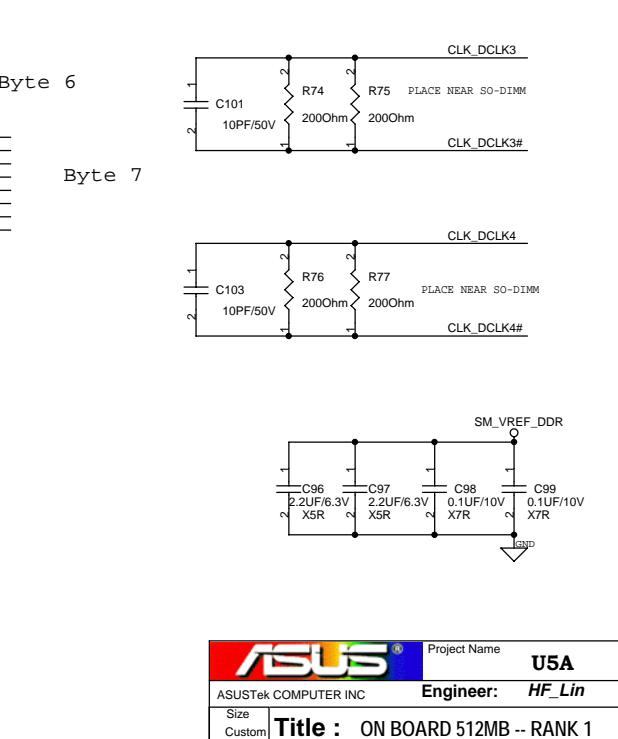
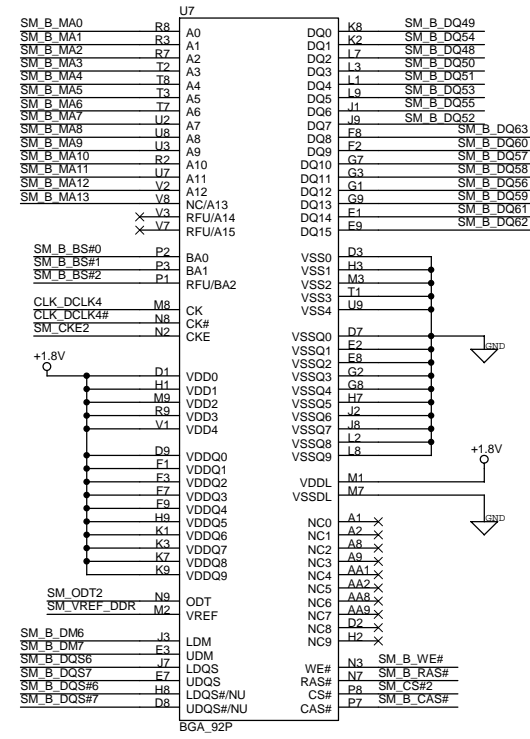
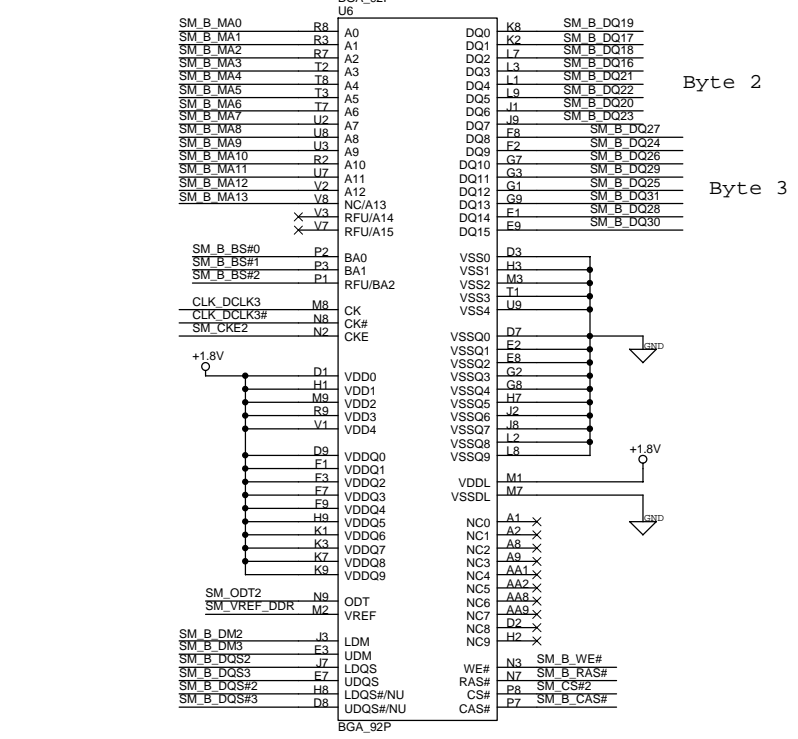
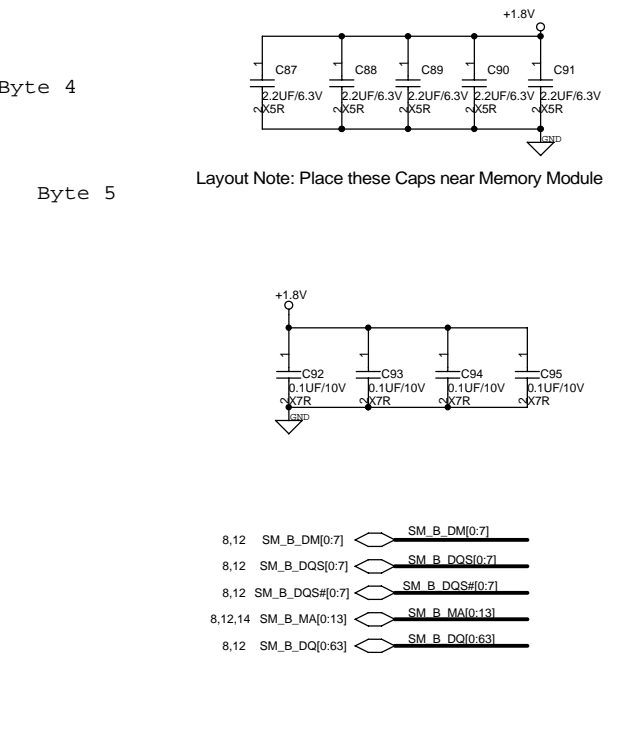
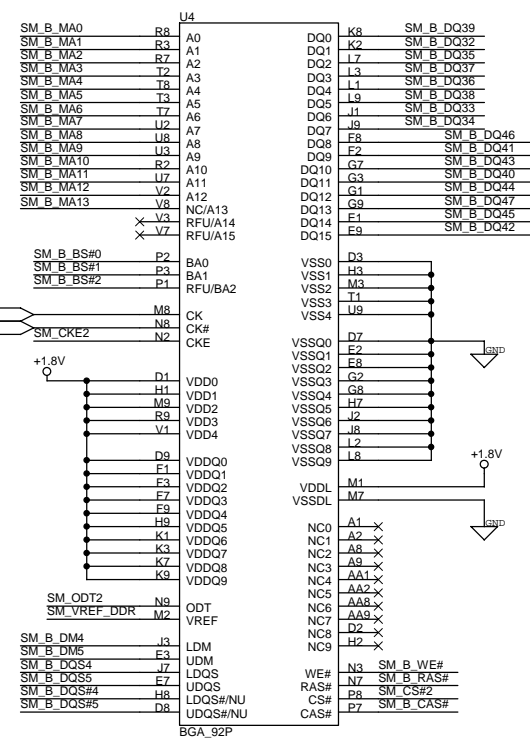
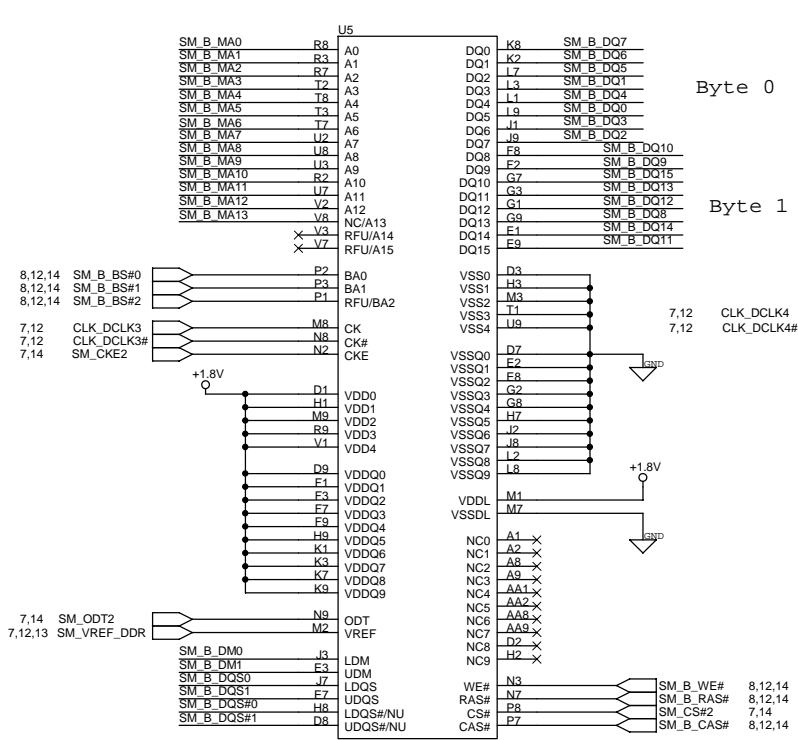


CFG18 : VCC SELECT
LOW = 1.05V (Default)
HIGH = 1.5V

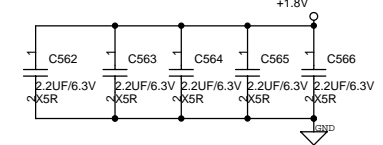
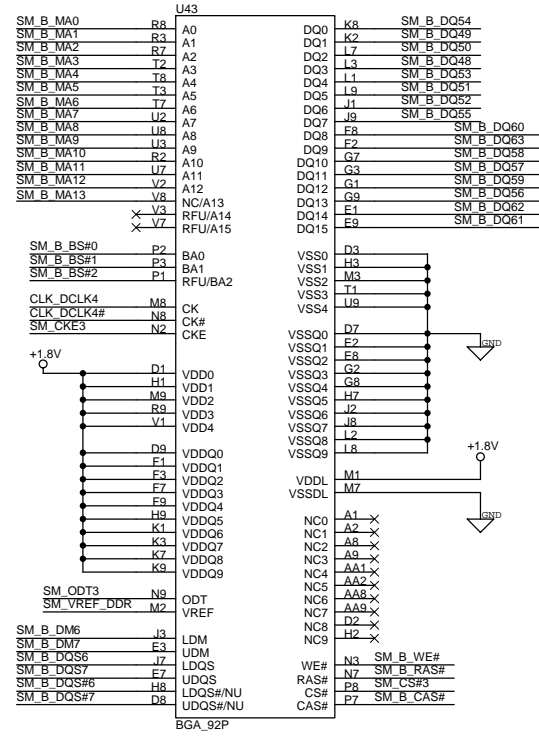
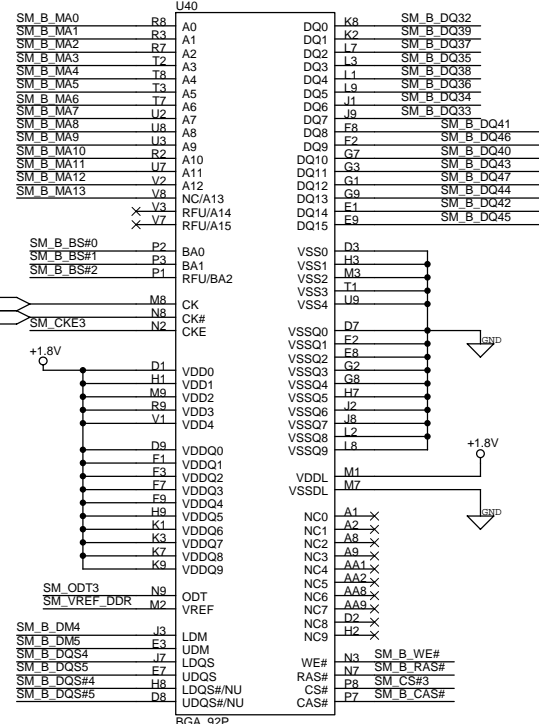
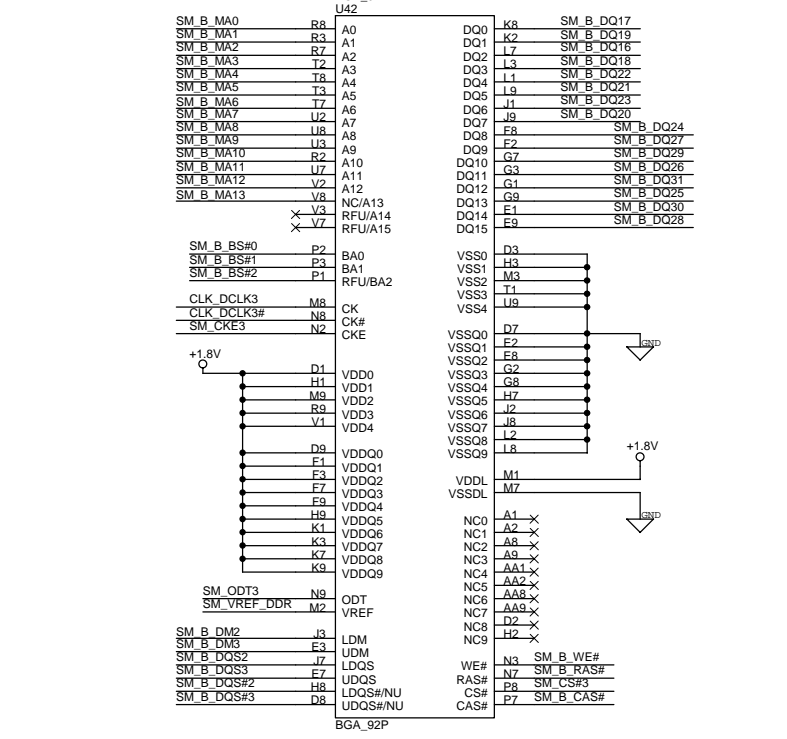
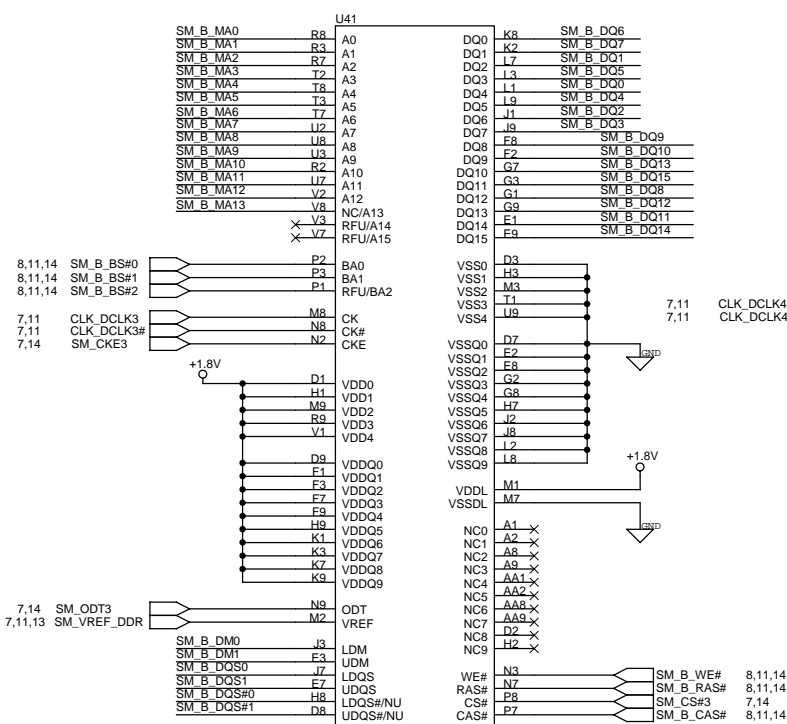


CFG19 : VTT SELECT
LOW = 1.05V (Default)
HIGH = 1.2V

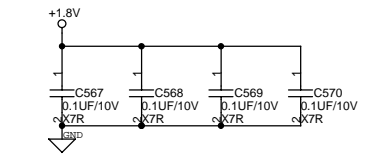




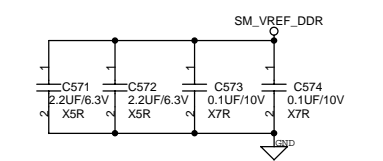
ASUS Project Name **USA**
ASUSTek COMPUTER INC Engineer: **HF Lin**
Size Custom **Title: ON BOARD 512MB -- RANK 1** Rev 2.0
Date: Tuesday, September 27, 2005 Sheet 11 of 46



Layout Note: Place these Caps near Memory Module



- 8,11 SM_B_DM[0:7] \rightarrow SM_B_DM[0:7]
- 8,11 SM_B_DQS[0:7] \rightarrow SM_B_DQS[0:7]
- 8,11 SM_B_DQS#[0:7] \rightarrow SM_B_DQS#[0:7]
- 8,11,14 SM_B_MA[0:13] \rightarrow SM_B_MA[0:13]
- 8,11 SM_B_DQ[0:63] \rightarrow SM_B_DQ[0:63]

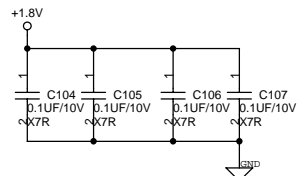
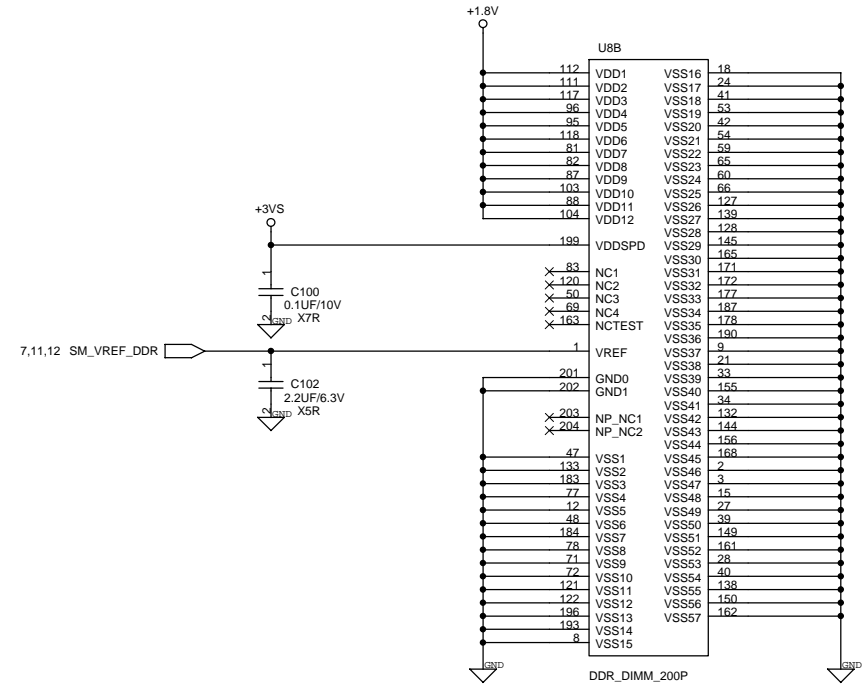


ASUS Project Name		USA
ASUSTek COMPUTER INC Engineer: HF_Lin		
Size Custom Title : ON BOARD 512MB -- RANK 2		Rev 2.0
Date: Tuesday, September 27, 2005		Sheet 12 of 46

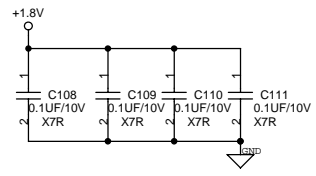
SM_A_MA[0:13] SM_A_MA[0:13] 8,14
 SM_A_DQ[0:63] SM_A_DQ[0:63] 8
 SM_A_DM[0:7] SM_A_DM[0:7] 8
 SM_A_DQS[0:7] SM_A_DQS[0:7] 8
 SM_A_DQS#[0:7] SM_A_DQS#[0:7] 8

U8A			
SM_A_MA0	102	A0	DQ0
SM_A_MA1	101	A1	DQ1
SM_A_MA2	100	A2	DQ2
SM_A_MA3	99	A3	DQ3
SM_A_MA4	98	A4	DQ4
SM_A_MA5	97	A5	DQ5
SM_A_MA6	94	A6	DQ6
SM_A_MA7	92	A7	DQ7
SM_A_MA8	93	A8	DQ8
SM_A_MA9	91	A9	DQ9
SM_A_MA10	105	A10/AP	DQ10
SM_A_MA11	90	A11	DQ11
SM_A_MA12	89	A12	DQ12
SM_A_MA13	116	A13	DQ13
	86	A14	DQ14
	84	A15	DQ15
	85	A16_BA2	DQ16
		BA0	DQ17
		BA1	DQ18
		BA2	DQ19
		BA3	DQ20
		BA4	DQ21
		BA5	DQ22
		BA6	DQ23
		BA7	DQ24
		BA8	DQ25
		BA9	DQ26
		BA10	DQ27
		BA11	DQ28
		BA12	DQ29
		BA13	DQ30
		BA14	DQ31
		BA15	DQ32
		BA16	DQ33
		BA17	DQ34
		BA18	DQ35
		BA19	DQ36
		BA20	DQ37
		BA21	DQ38
		BA22	DQ39
		BA23	DQ40
		BA24	DQ41
		BA25	DQ42
		BA26	DQ43
		BA27	DQ44
		BA28	DQ45
		BA29	DQ46
		BA30	DQ47
		BA31	DQ48
		BA32	DQ49
		BA33	DQ50
		BA34	DQ51
		BA35	DQ52
		BA36	DQ53
		BA37	DQ54
		BA38	DQ55
		BA39	DQ56
		BA40	DQ57
		BA41	DQ58
		BA42	DQ59
		BA43	DQ60
		BA44	DQ61
		BA45	DQ62
		BA46	DQ63

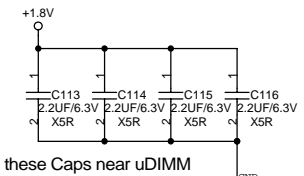
Byte 0
 Byte 1
 Byte 2
 Byte 3
 Byte 5
 Byte 4
 Byte 6
 Byte 7



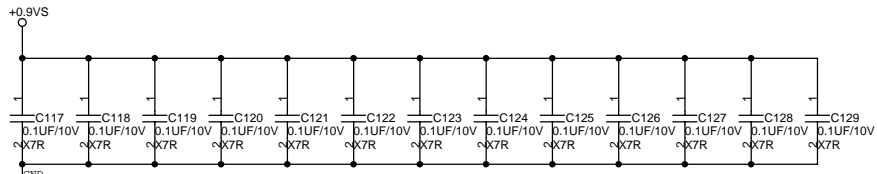
Layout Note: Place these Caps near uDIMM



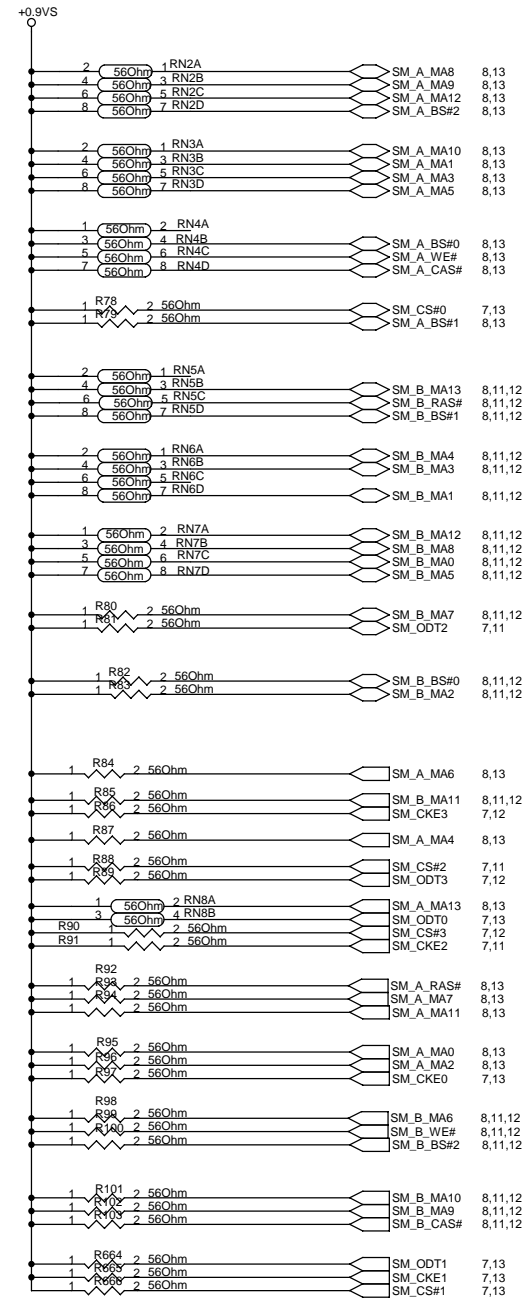
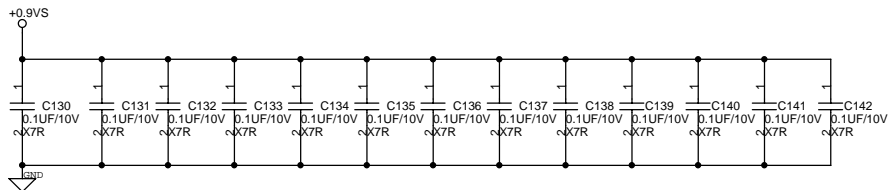
Layout Note: Place these High-Freq decoupling Caps near the GMCH



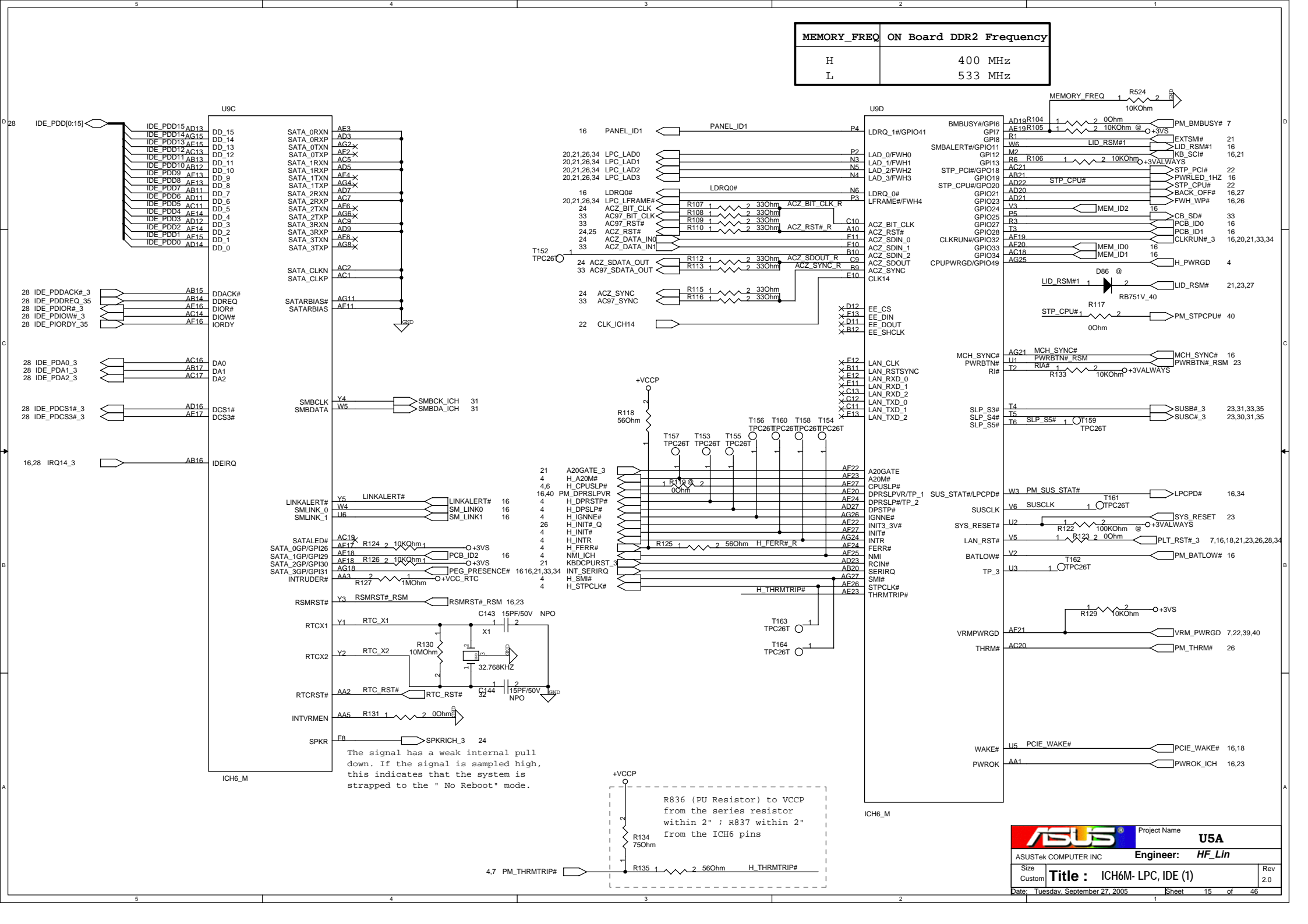
Layout Note: Place these Caps near uDIMM



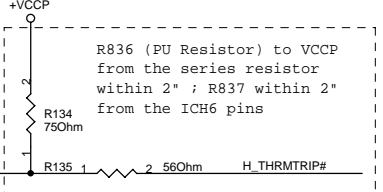
Layout Note: Place one cap close to every 2 pullup resistors terminated to +0.9VS

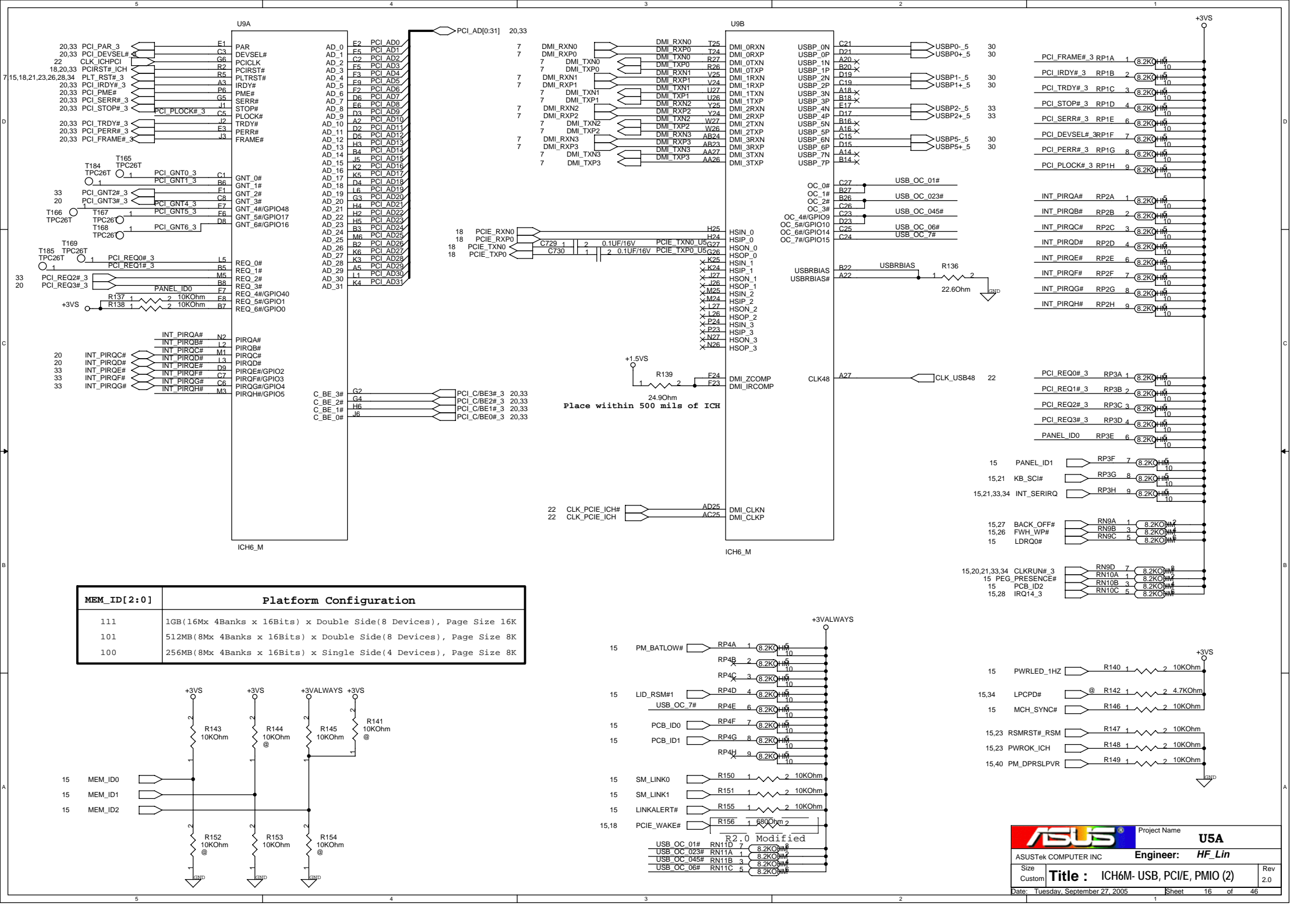


MEMORY_FREQ	ON Board DDR2 Frequency
H	400 MHz
L	533 MHz

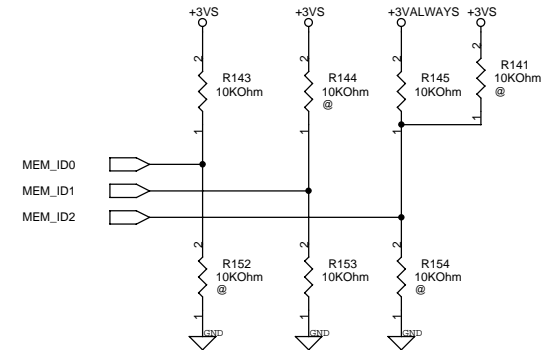


The signal has a weak internal pull down. If the signal is sampled high, this indicates that the system is strapped to the " No Reboot" mode.



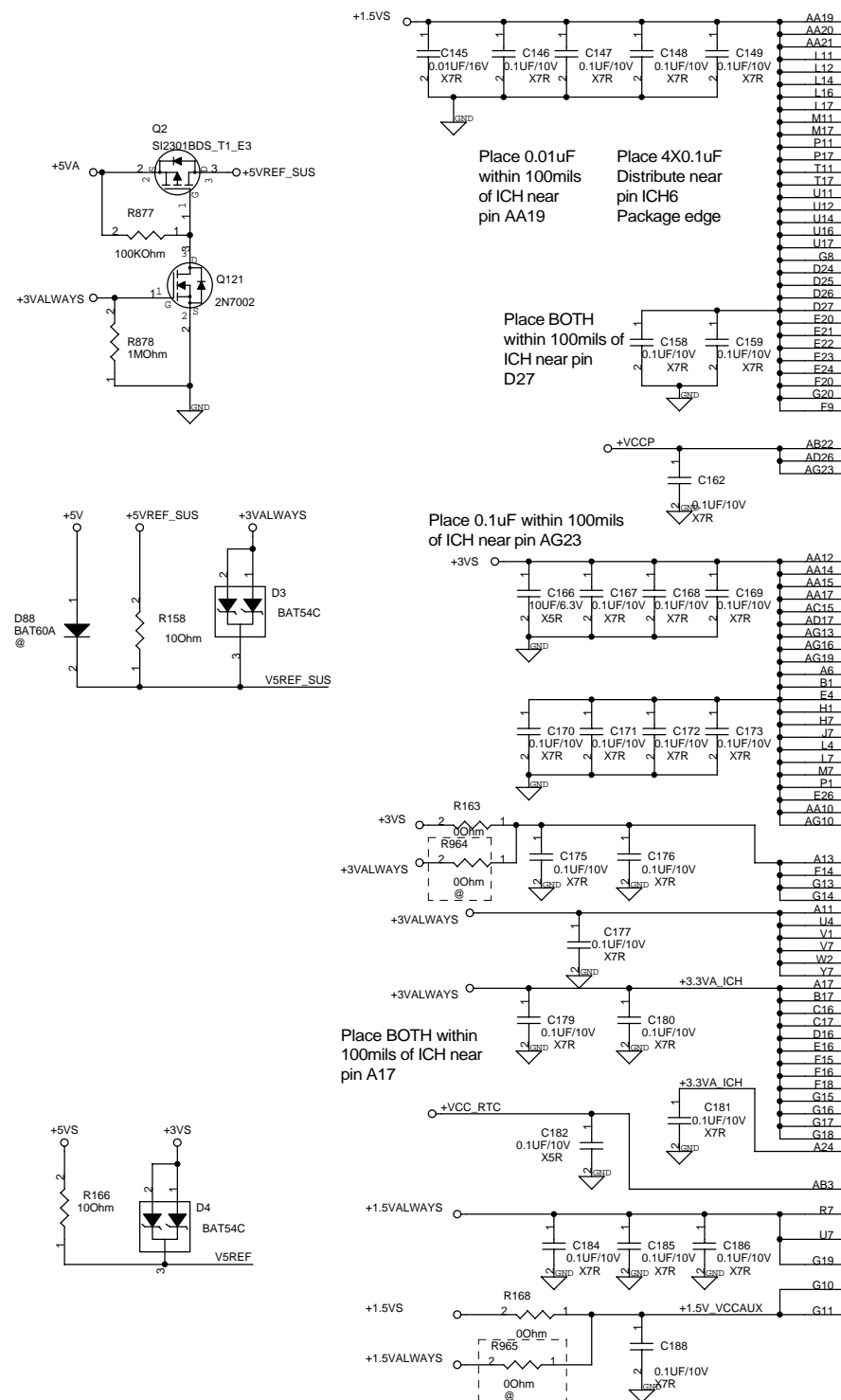


MEM_ID[2:0]	Platform Configuration
111	1GB(16Mx 4Banks x 16Bits) x Double Side(8 Devices), Page Size 16K
101	512MB(8Mx 4Banks x 16Bits) x Double Side(8 Devices), Page Size 8K
100	256MB(8Mx 4Banks x 16Bits) x Single Side(4 Devices), Page Size 8K

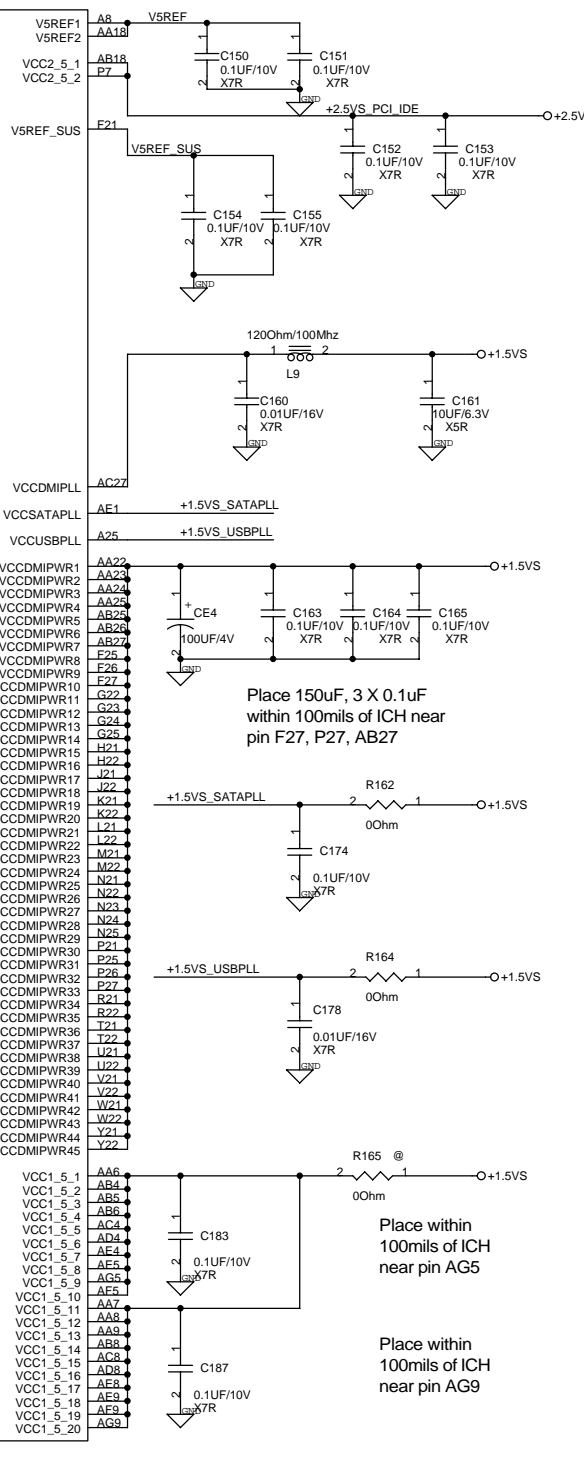


Place within 500 mils of ICH

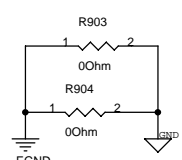
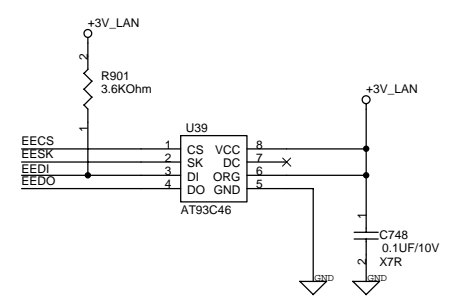
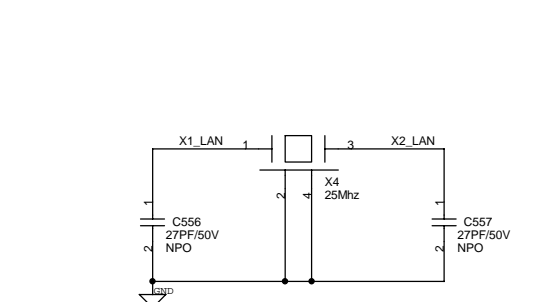
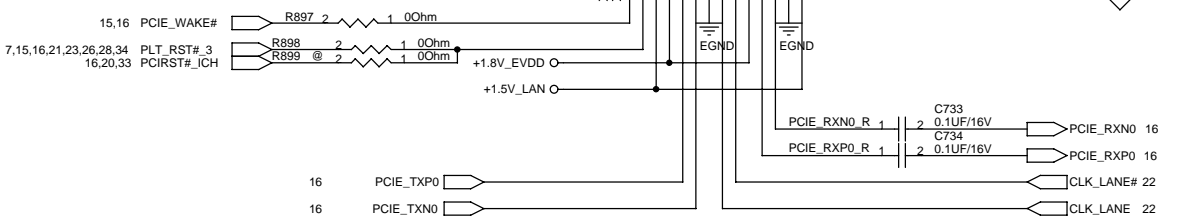
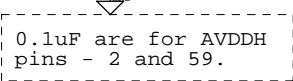
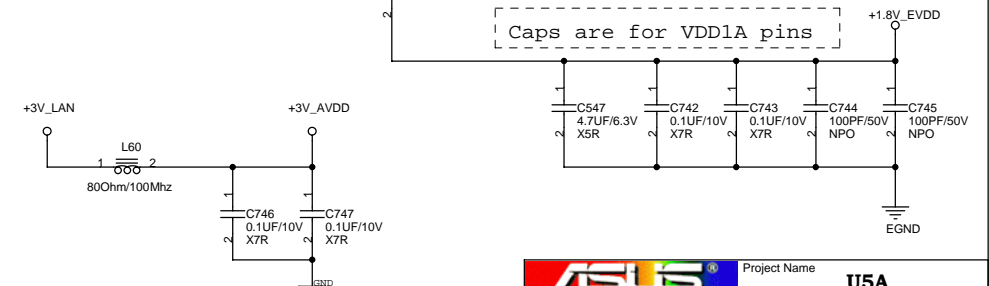
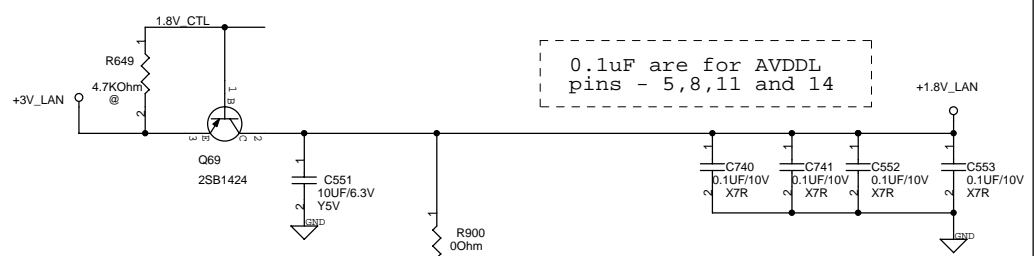
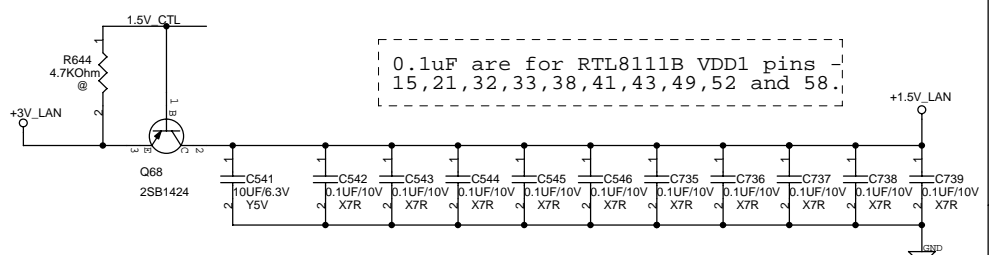
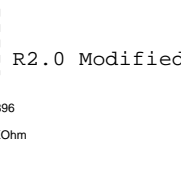
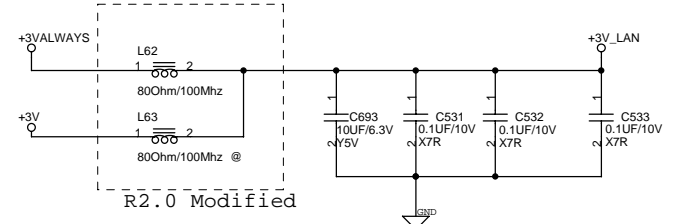
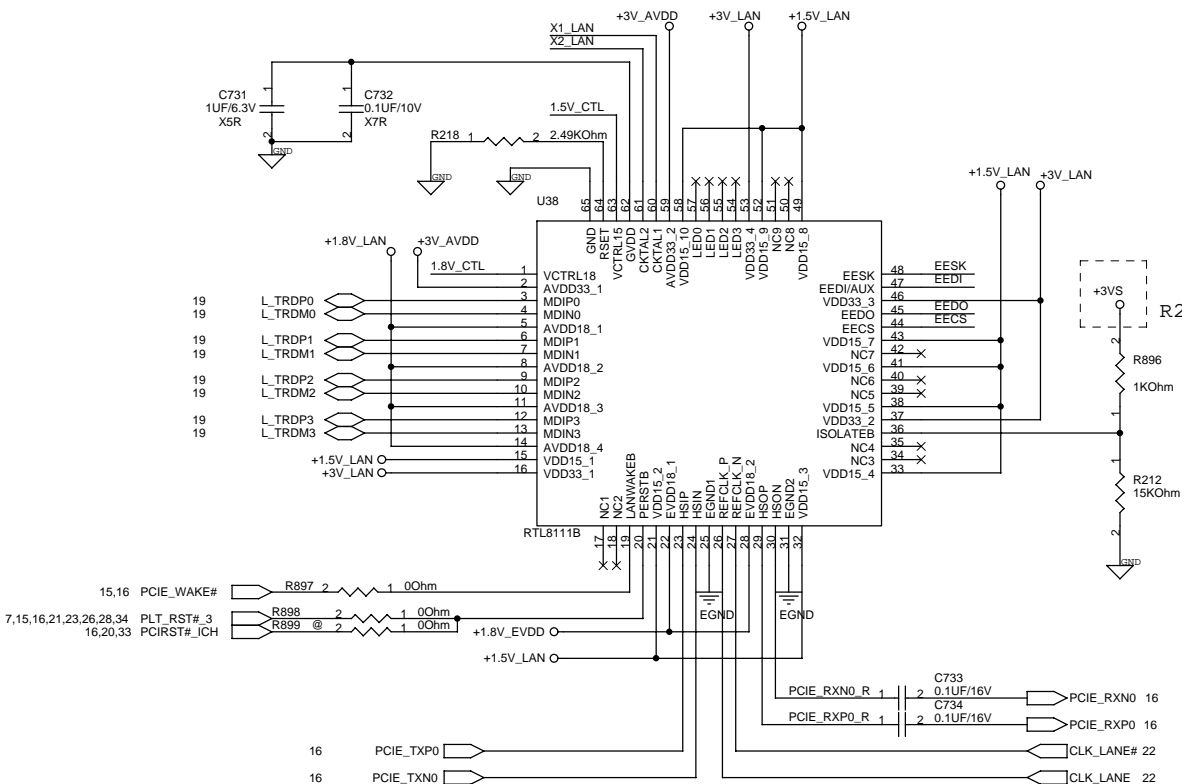
ASUS Project Name		USA
ASUSTek COMPUTER INC		Engineer: HF Lin
Size Custom		Title : ICH6M- USB, PCI/E, PMIO (2)
Date: Tuesday, September 27, 2005		Sheet 16 of 46

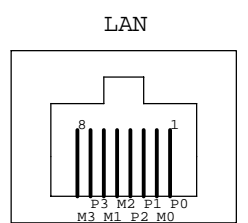
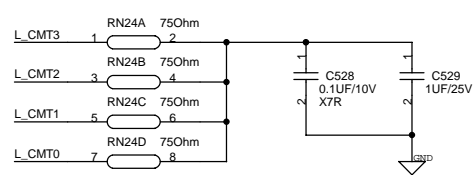
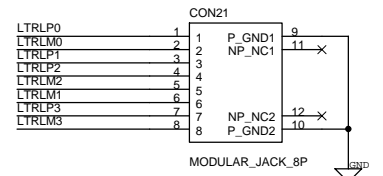
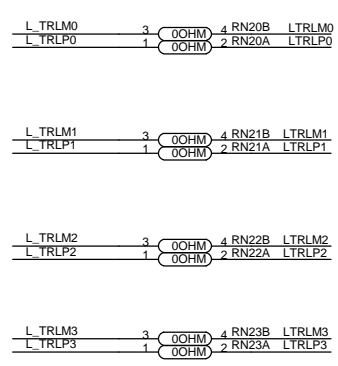
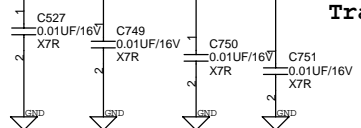
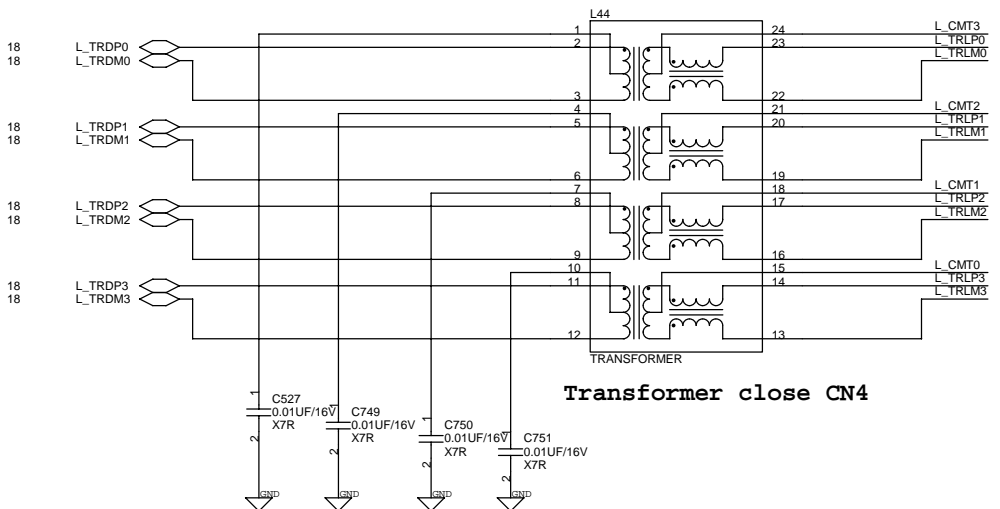


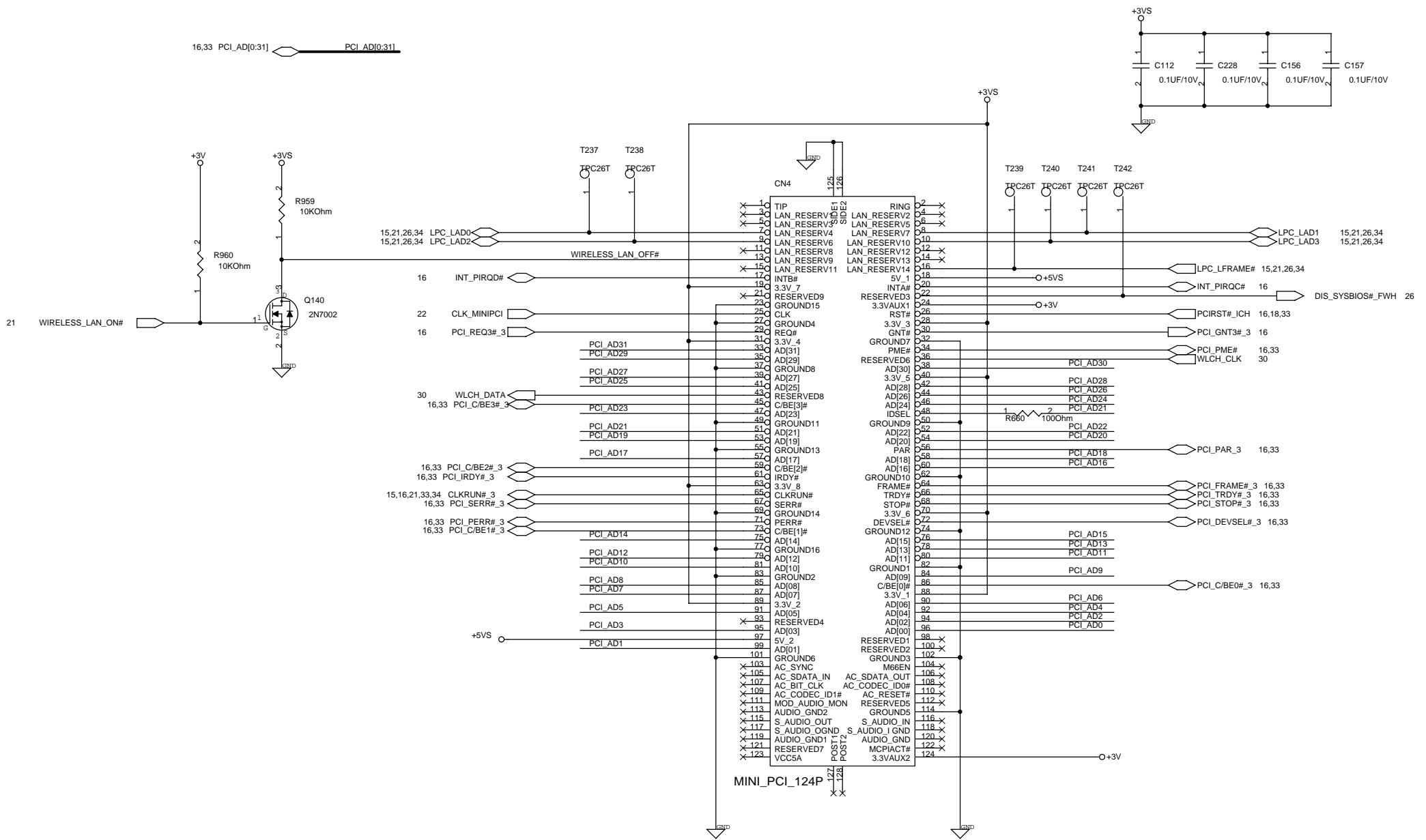
AA19	VCC1_5_21
AA20	VCC1_5_22
I11	VCC1_5_23
I12	VCC1_5_24
I14	VCC1_5_25
I16	VCC1_5_26
I17	VCC1_5_27
M11	VCC1_5_28
M17	VCC1_5_29
P11	VCC1_5_30
P17	VCC1_5_31
T17	VCC1_5_32
U11	VCC1_5_33
U12	VCC1_5_34
U14	VCC1_5_35
U16	VCC1_5_36
U17	VCC1_5_37
GA	VCC1_5_38
GA	VCC1_5_39
D24	VCC1_5_40
D25	VCC1_5_41
D26	VCC1_5_42
D27	VCC1_5_43
F20	VCC1_5_44
F21	VCC1_5_45
F22	VCC1_5_46
F23	VCC1_5_47
F24	VCC1_5_48
F20	VCC1_5_49
G20	VCC1_5_50
F9	VCC1_5_51
	VCC1_5_52
AA12	VCC3_3_1
AA14	VCC3_3_2
AA15	VCC3_3_3
AA17	VCC3_3_4
AC15	VCC3_3_5
AD17	VCC3_3_6
AG13	VCC3_3_7
AG16	VCC3_3_8
AG19	VCC3_3_9
A6	VCC3_3_10
B1	VCC3_3_11
E4	VCC3_3_12
H7	VCC3_3_13
J7	VCC3_3_14
L4	VCC3_3_15
L7	VCC3_3_16
MZ	VCC3_3_17
P1	VCC3_3_18
F26	VCC3_3_19
AA10	VCC3_3_20
AG10	VCC3_3_21
	VCC3_3_22
A13	VCCSUS3_3_1
G13	VCCSUS3_3_2
G14	VCCSUS3_3_3
A11	VCCSUS3_3_4
U4	VCCSUS3_3_5
V1	VCCSUS3_3_6
V7	VCCSUS3_3_7
W2	VCCSUS3_3_8
Y7	VCCSUS3_3_9
A17	VCCSUS3_3_10
B17	VCCSUS3_3_11
C16	VCCSUS3_3_12
C17	VCCSUS3_3_13
D16	VCCSUS3_3_14
F18	VCCSUS3_3_15
F15	VCCSUS3_3_16
F16	VCCSUS3_3_17
F18	VCCSUS3_3_18
G15	VCCSUS3_3_19
G16	VCCSUS3_3_20
G17	VCCSUS3_3_21
G18	VCCSUS3_3_22
G18	VCCSUS3_3_23
A24	VCCSUS3_3_24
AB3	VCCRTC
U7	VCCSUS1_5_A
G19	VCCSUS1_5_B
G10	VCCSUS1_5_C
G11	VCCSUS1_5_D
	VCCSUS1_5_E
AA6	VCC1_5_1
AB4	VCC1_5_2
AB5	VCC1_5_3
AB6	VCC1_5_4
AC4	VCC1_5_5
AD4	VCC1_5_6
AE4	VCC1_5_7
AE5	VCC1_5_8
AG5	VCC1_5_9
AE5	VCC1_5_10
AA7	VCC1_5_11
AA8	VCC1_5_12
AA9	VCC1_5_13
AB8	VCC1_5_14
AC8	VCC1_5_15
AD8	VCC1_5_16
AE8	VCC1_5_17
AE9	VCC1_5_18
AG9	VCC1_5_19
	VCC1_5_20

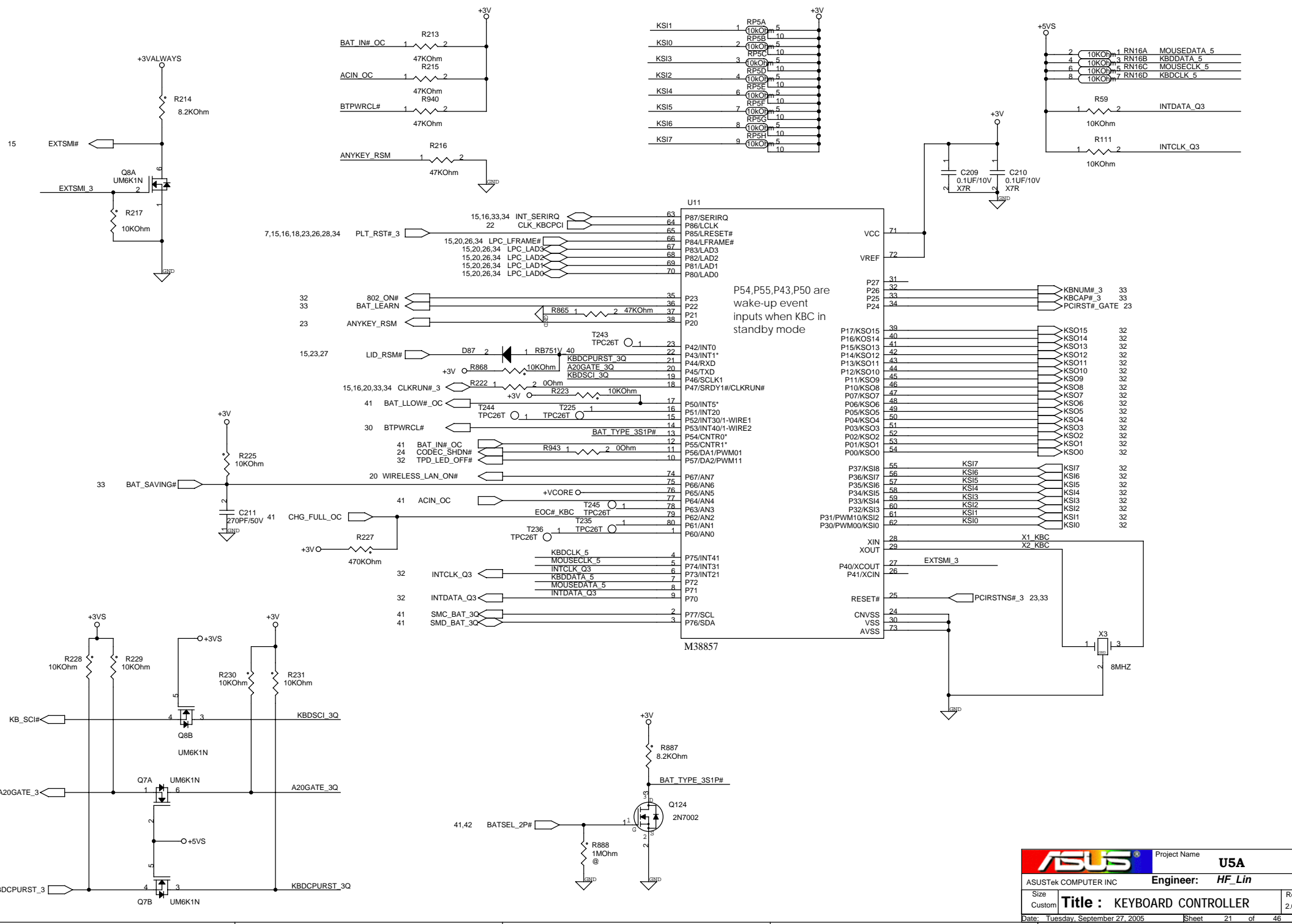


A1	VSS1	VSS87	G21
A12	VSS2	VSS88	G7
A15	VSS3	VSS89	G9
A19	VSS4	VSS90	H23
A21	VSS5	VSS91	H26
A23	VSS6	VSS92	H27
A26	VSS7	VSS93	J23
A4	VSS8	VSS94	J24
A7	VSS9	VSS95	J25
A9	VSS10	VSS96	J4
AA11	VSS11	VSS97	K1
AA13	VSS12	VSS98	K23
AA16	VSS13	VSS99	K26
AA17	VSS14	VSS100	K27
AB1	VSS15	VSS101	K7
AB10	VSS16	VSS102	L13
AB19	VSS17	VSS103	L15
AB7	VSS18	VSS104	L23
AB7	VSS19	VSS105	L24
AB9	VSS20	VSS106	L26
AC10	VSS21	VSS107	M12
AC12	VSS22	VSS108	M13
AC22	VSS23	VSS109	M14
AC23	VSS24	VSS110	M15
AC24	VSS25	VSS111	M16
AC28	VSS26	VSS112	M2
AC3	VSS27	VSS113	M26
AC6	VSS28	VSS114	M27
AD1	VSS29	VSS115	M4
AD10	VSS30	VSS116	N1
AD15	VSS31	VSS117	N11
AD18	VSS32	VSS118	N12
AD2	VSS33	VSS119	N13
AD24	VSS34	VSS120	N14
AD6	VSS35	VSS121	N15
AE10	VSS36	VSS122	N16
AE11	VSS37	VSS123	N17
AE12	VSS38	VSS124	N18
AE2	VSS39	VSS125	P12
AE21	VSS40	VSS126	P13
AE25	VSS41	VSS127	P14
AE6	VSS42	VSS128	P15
AE7	VSS43	VSS129	P16
AE7	VSS44	VSS130	R11
AF2	VSS45	VSS131	R12
AF26	VSS46	VSS132	R13
AF3	VSS47	VSS133	R13
AF7	VSS48	VSS134	R14
AG1	VSS49	VSS135	R15
AG12	VSS50	VSS136	R17
AG14	VSS51	VSS137	R22
AG17	VSS52	VSS138	R23
AG20	VSS53	VSS139	R24
AG22	VSS54	VSS140	R4
AG3	VSS55	VSS141	R4
AG7	VSS56	VSS142	T12
B13	VSS57	VSS143	T13
B15	VSS58	VSS144	T14
B19	VSS59	VSS145	T14
B21	VSS60	VSS146	T15
B23	VSS61	VSS147	T16
B25	VSS62	VSS148	T23
C14	VSS63	VSS149	T26
C18	VSS64	VSS150	T27
C20	VSS65	VSS151	T7
C22	VSS66	VSS152	U13
C4	VSS67	VSS153	U15
D1	VSS68	VSS154	U24
D10	VSS69	VSS155	U25
D13	VSS70	VSS156	U26
D14	VSS71	VSS157	V23
D18	VSS72	VSS158	V26
D20	VSS73	VSS159	V27
D22	VSS74	VSS160	V4
D7	VSS75	VSS161	W1
E14	VSS76	VSS162	W23
E15	VSS77	VSS163	W25
E18	VSS78	VSS164	W26
E19	VSS79	VSS165	W7
E20	VSS80	VSS166	Y23
E17	VSS81	VSS167	Y27
F19	VSS82	VSS168	Y6
F22	VSS83	VSS169	Y24
W21	VSS84	VSS170	W24
W22	VSS85	VSS171	W27
Y21	VSS86	VSS172	B24
Y22	VSS87	VSS173	AE10

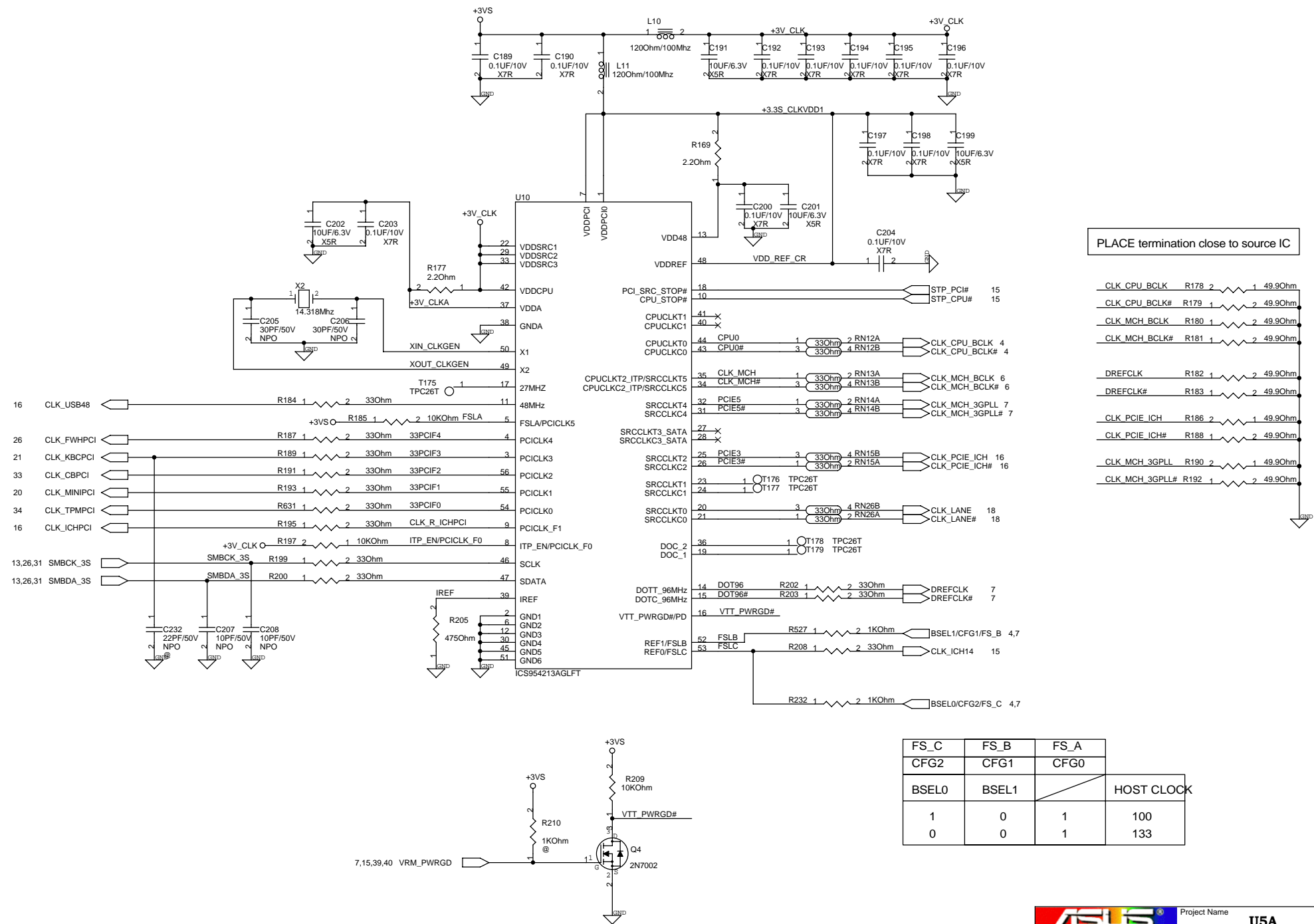








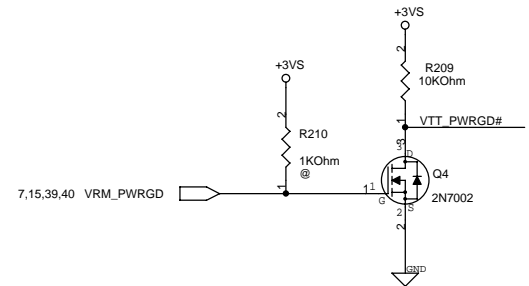
P54, P55, P43, P50 are wake-up event inputs when KBC in standby mode

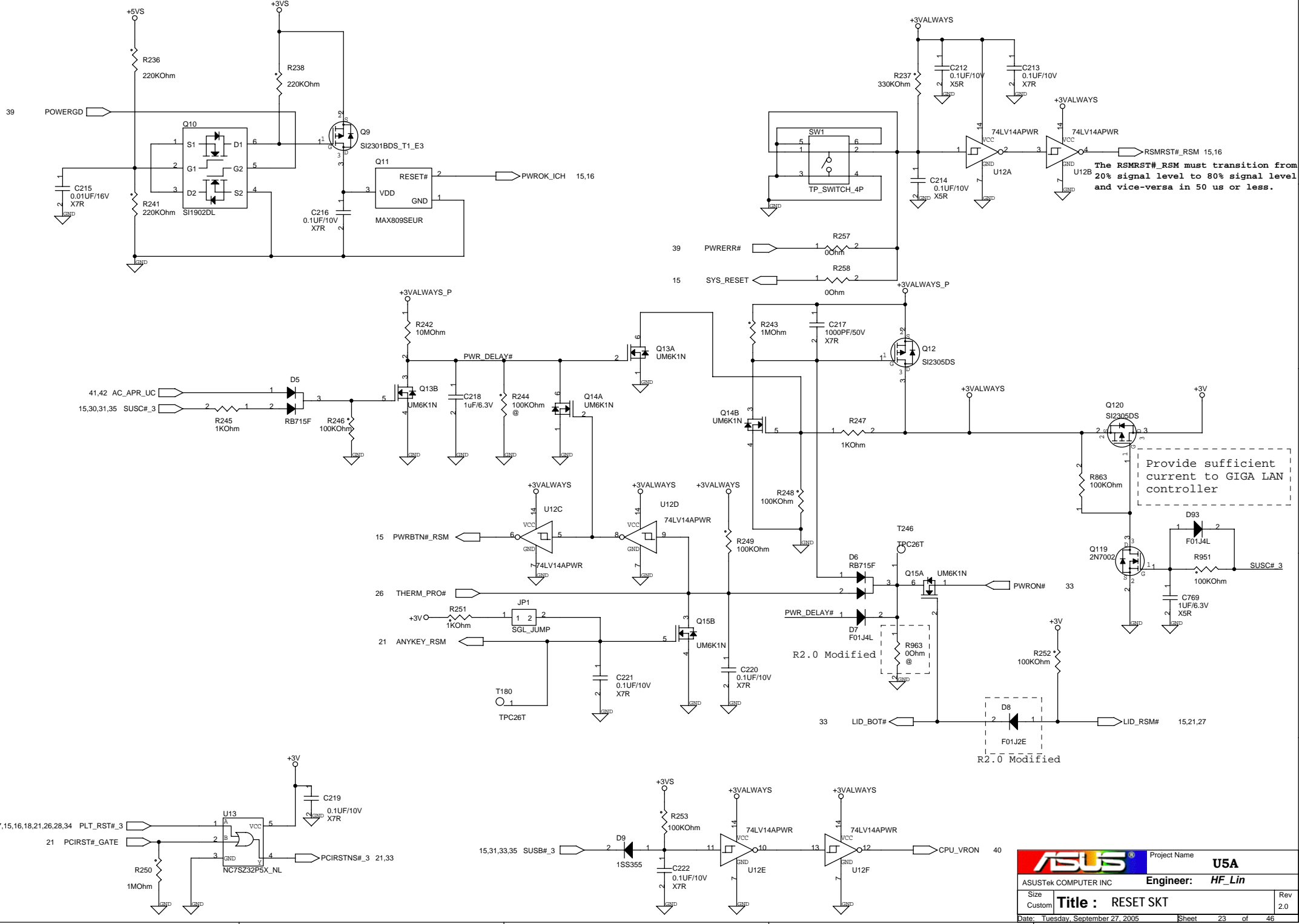


PLACE termination close to source IC

- CLK CPU_BCLK R178 2 1 49.90hm
- CLK CPU_BCLK# R179 1 2 49.90hm
- CLK MCH_BCLK R180 1 2 49.90hm
- CLK MCH_BCLK# R181 1 2 49.90hm
- DREFCLK R182 1 2 49.90hm
- DREFCLK# R183 1 2 49.90hm
- CLK PCIE_ICH R186 2 1 49.90hm
- CLK PCIE_ICH# R188 1 2 49.90hm
- CLK MCH_3GPLL R190 2 1 49.90hm
- CLK MCH_3GPLL# R192 1 2 49.90hm

FS_C	FS_B	FS_A	
CFG2	CFG1	CFG0	
BSEL0	BSEL1		HOST CLOCK
1	0	1	100
0	0	1	133



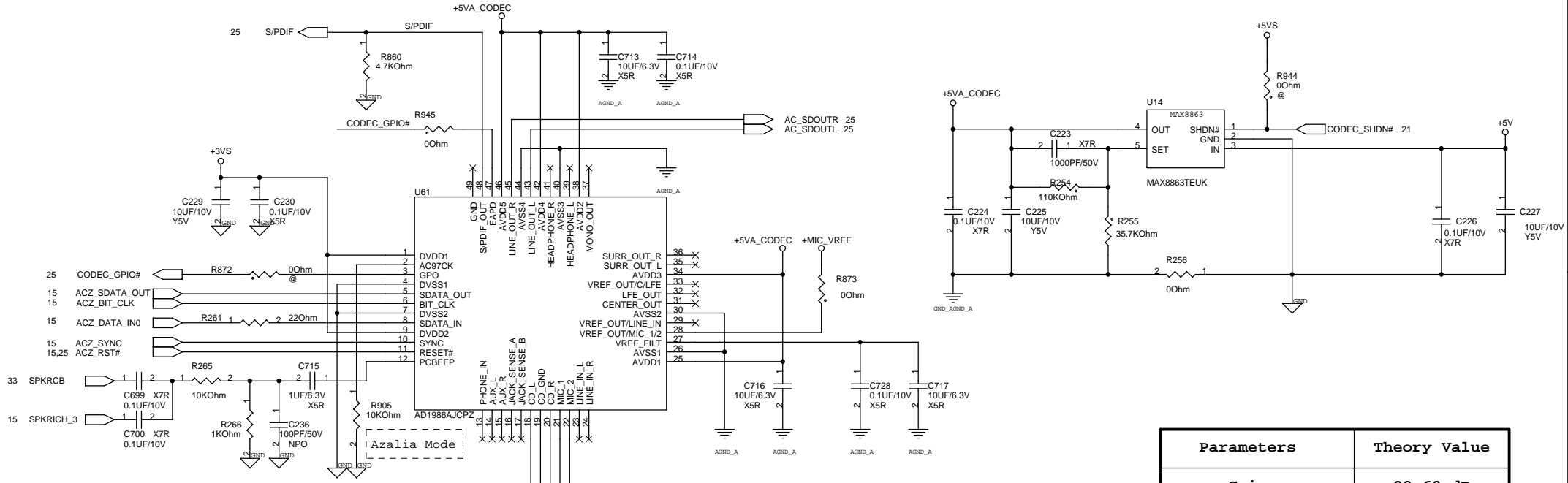


The RSMRST#_RSM must transition from 20% signal level to 80% signal level and vice-versa in 50 us or less.

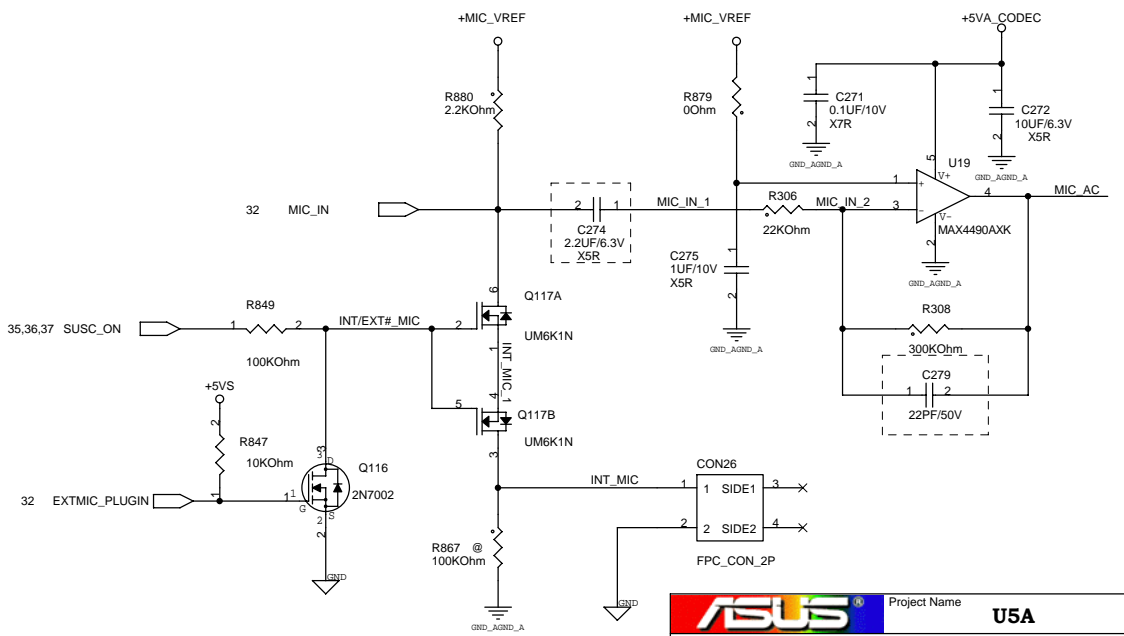
Provide sufficient current to GIGA LAN controller

R2.0 Modified

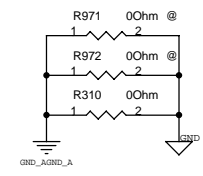
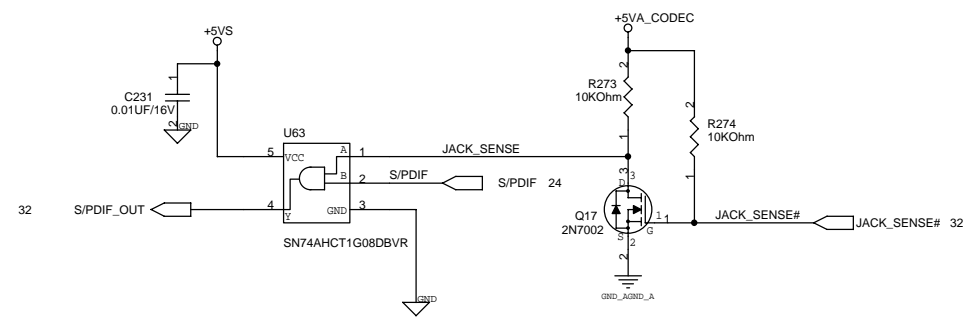
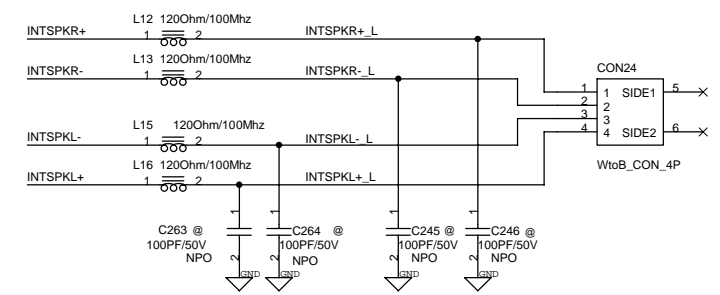
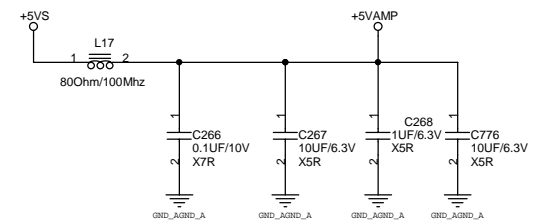
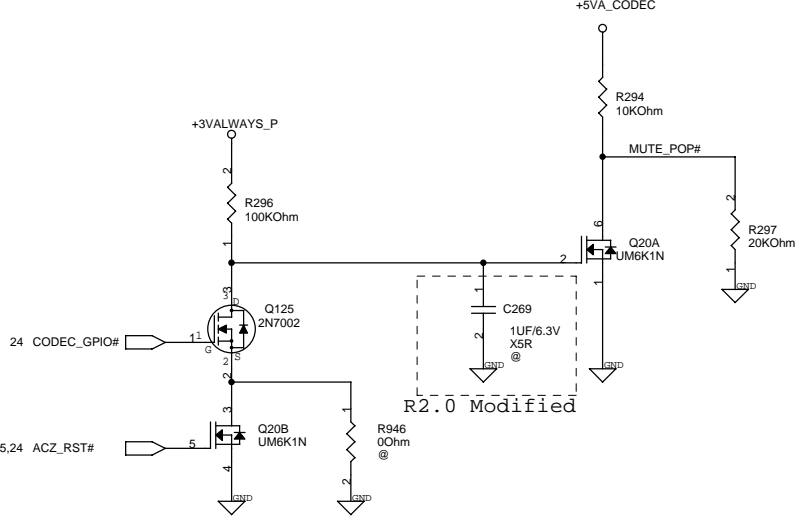
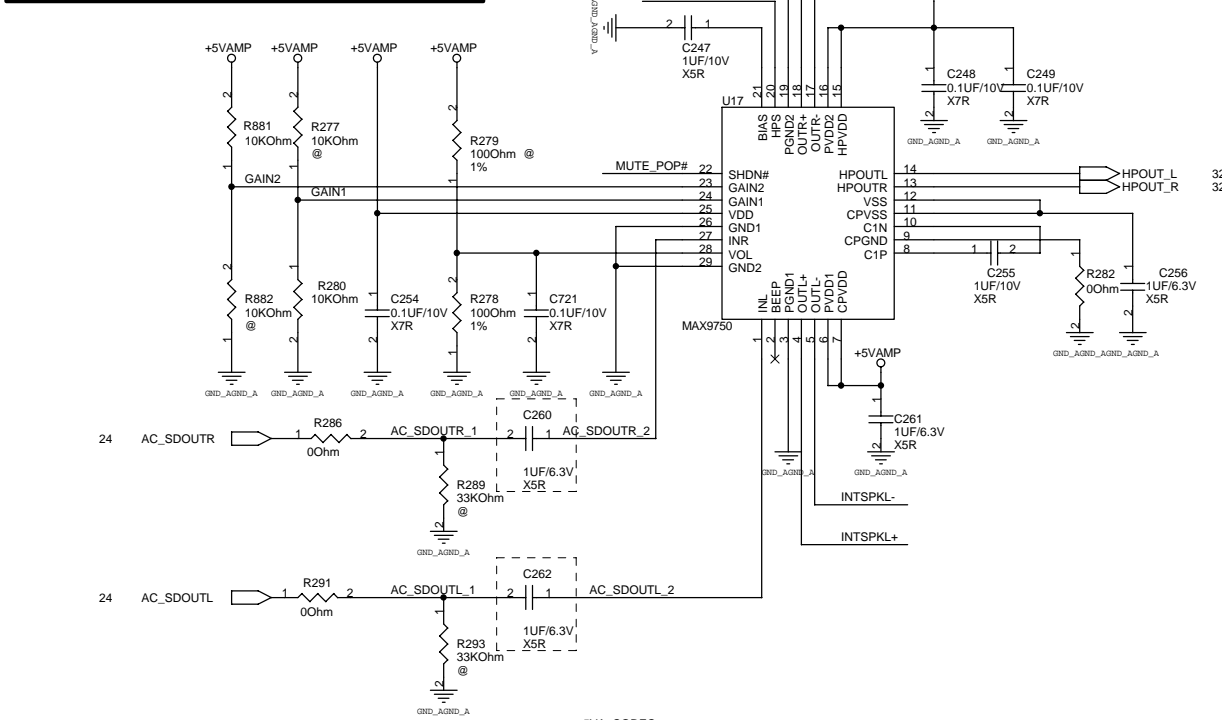
R2.0 Modified

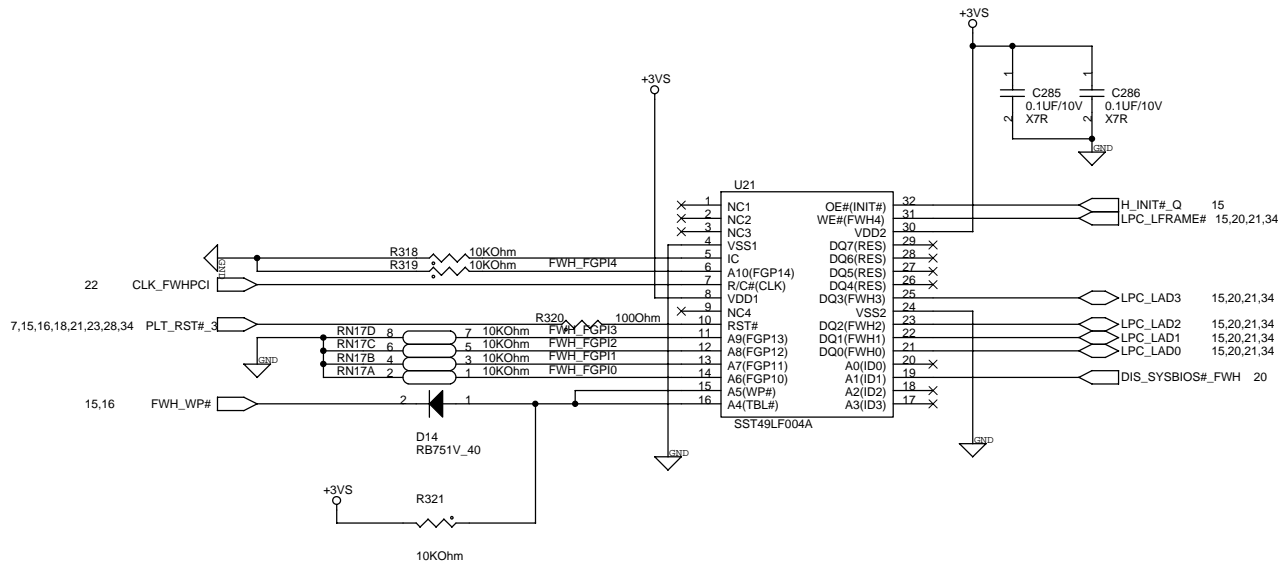
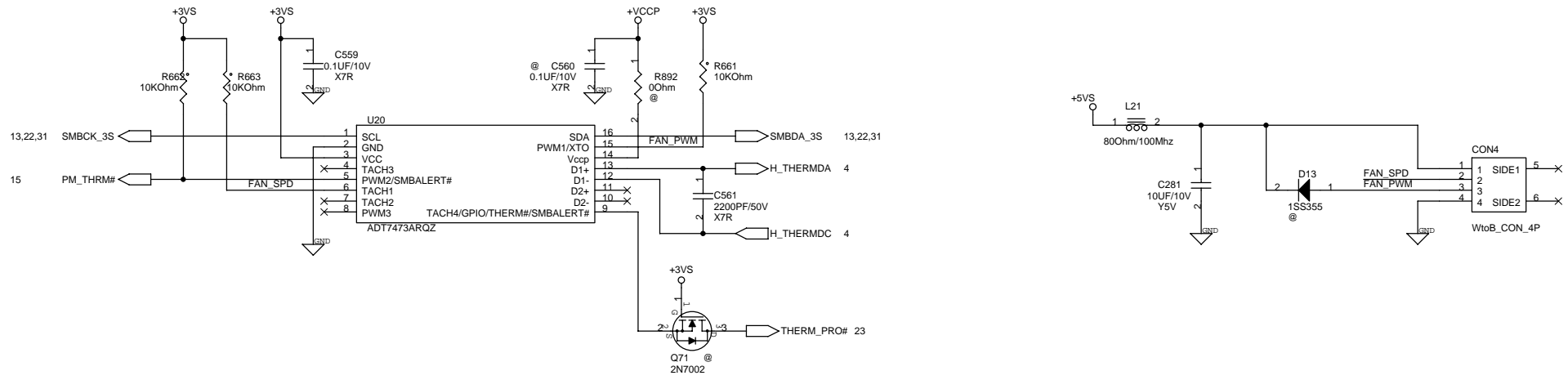


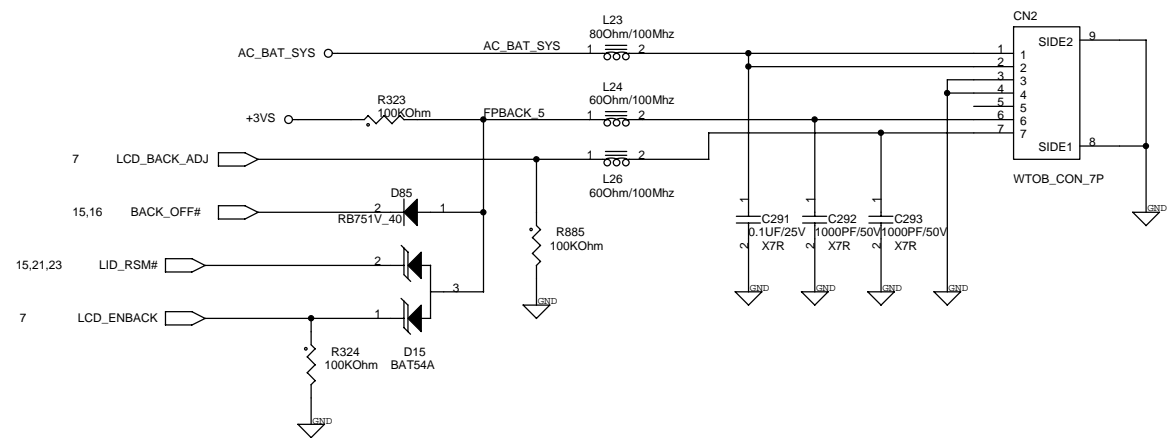
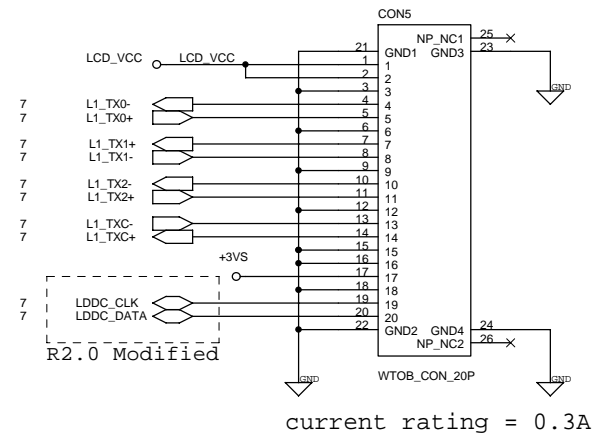
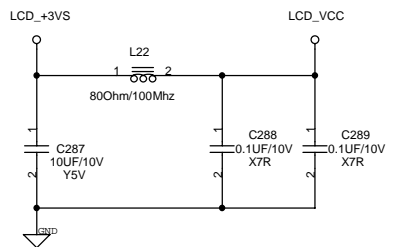
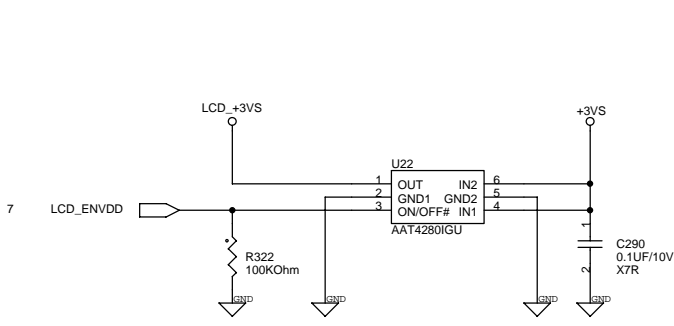
Parameters	Theory Value
Gain	22.69 dB
High Frequency Cutt-off	5.3 KHz
Low Frequency Cutt-off	7 Hz

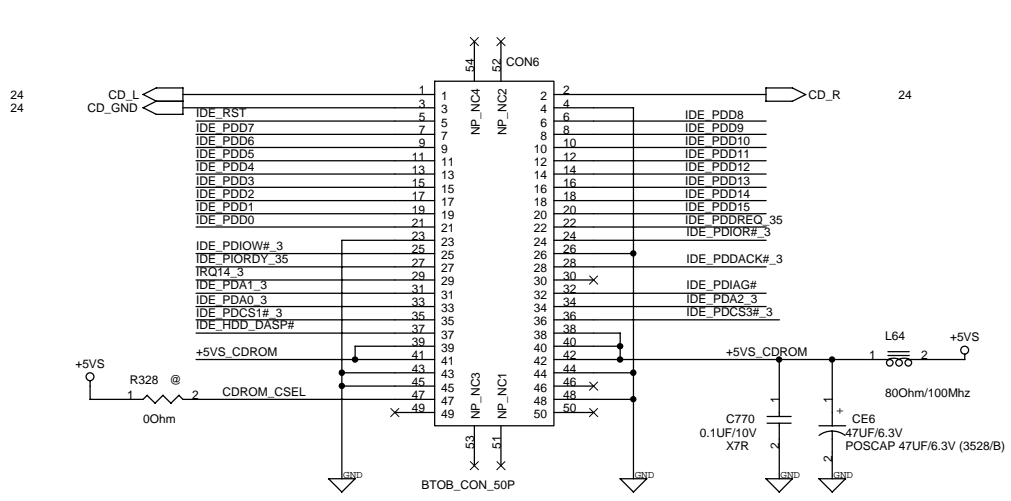


GAIN 2	GAIN 1	VOL	Speaker Gain	HP Gain
0	0	0 V	6 dB	0 dB
0	1	0 V	7.5 dB	0 dB
1	0	0 V	9 dB	3 dB
1	1	0 V	10.5 dB	3 dB



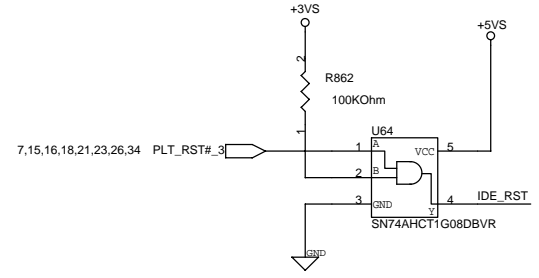
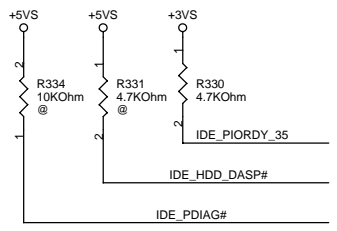
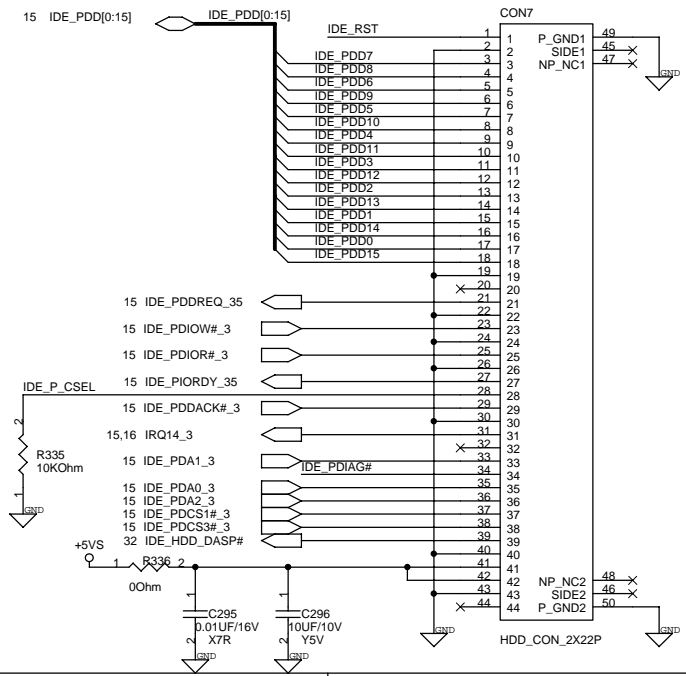
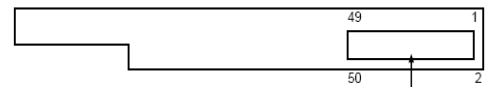




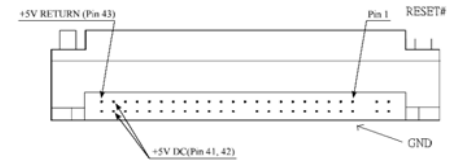


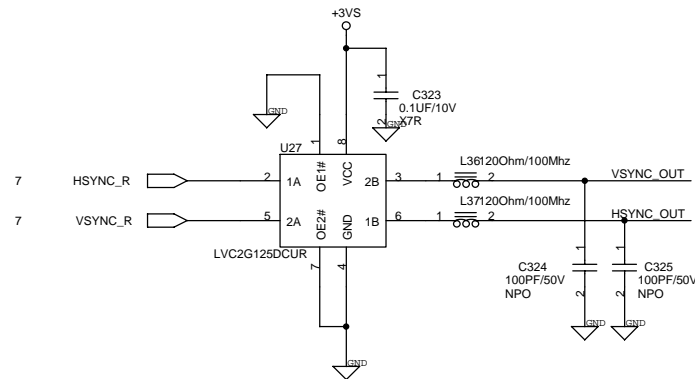
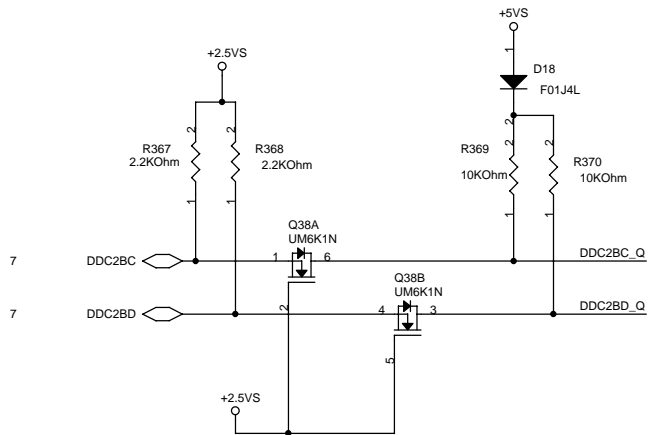
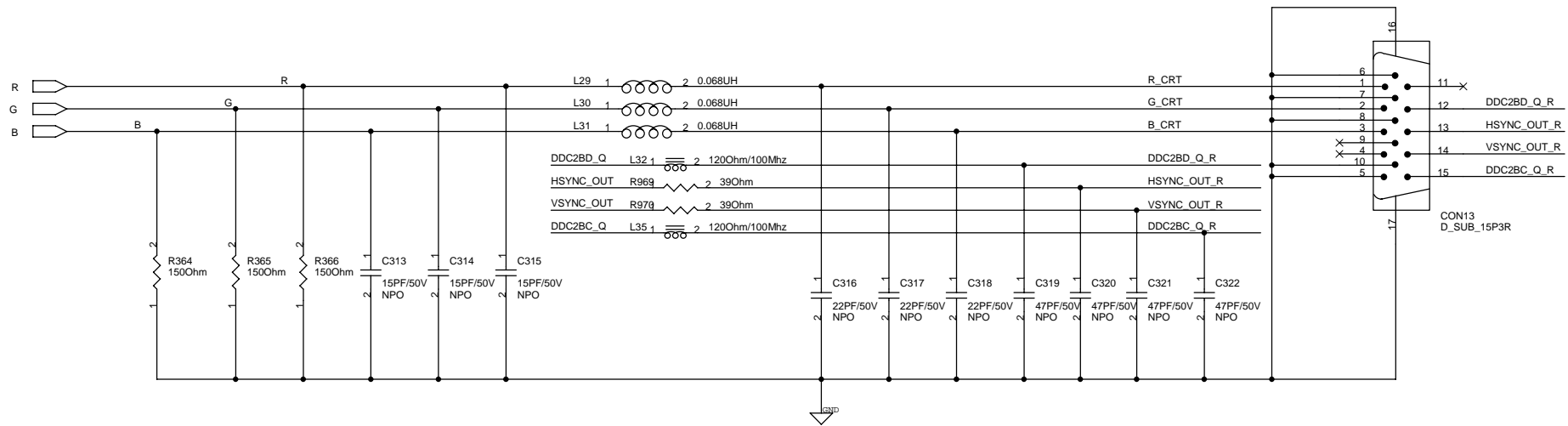
DVD/CDRW ROM
 CSEL: H level = Slave
 L level = Master

1AUDIO-L	2AUDIO-R
3AUDIO-G	4GND
5-RESET	6DD8
7DD7	8DD9
9DD6	10DD10
11DD5	12DD11
13DD4	14DD12
15DD3	16DD13
17DD2	18DD14
19DD1	20DD15
21DD0	22DMARQ
23GND	24-DIOR
25-DIOW	26GND
27IORDY	28-DMACK
29INTRQ	30-IOCS16
31DA1	32-PDIAG
33DA0	34DA2
35-CS0	36-CS1
37-DASP	38+5V
39+5V	40+5V
41+5V	42+5V
43GND	44GND
45GND	46Vender
47CSEL	48GND
49Vender	50Vender

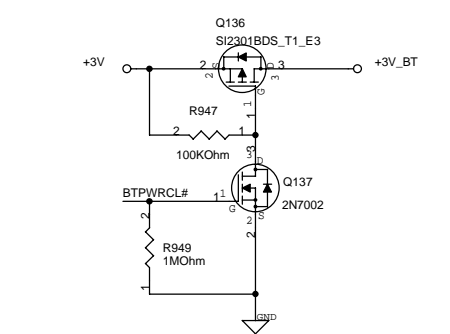
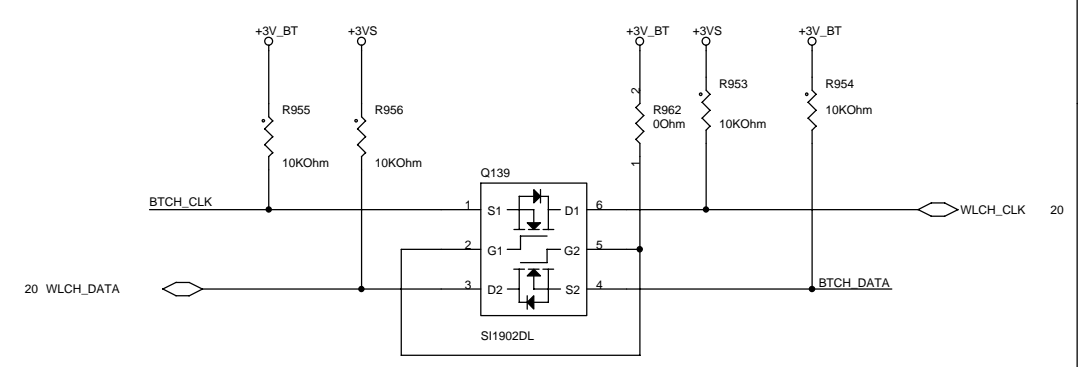
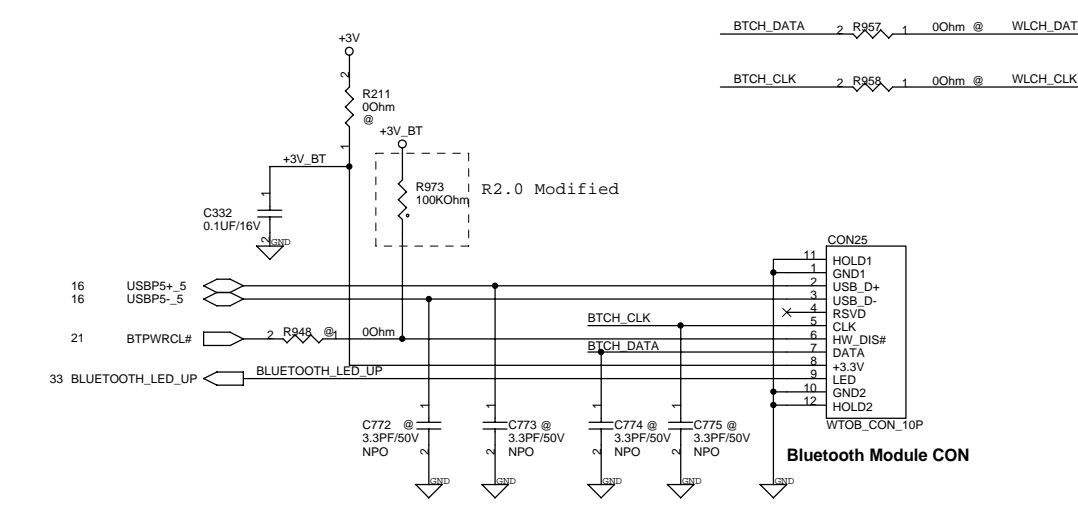
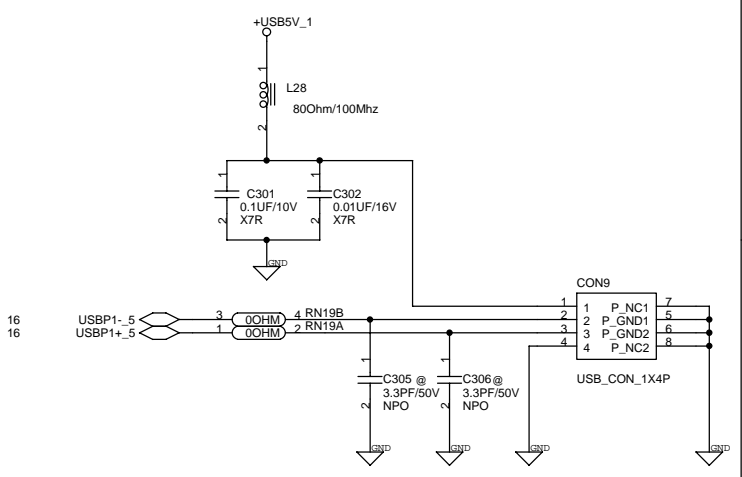
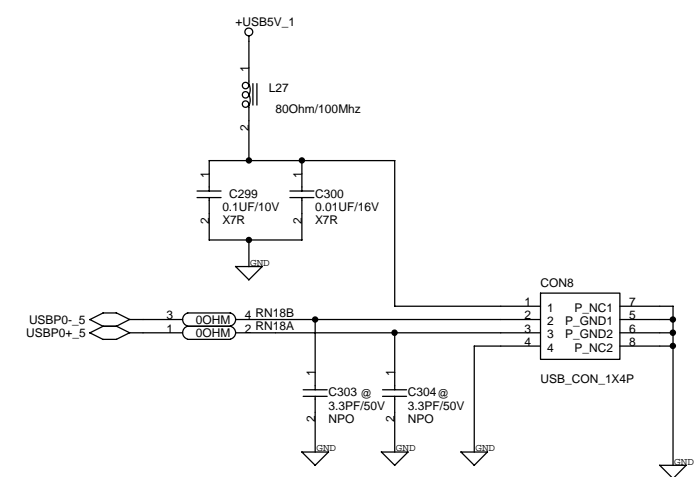
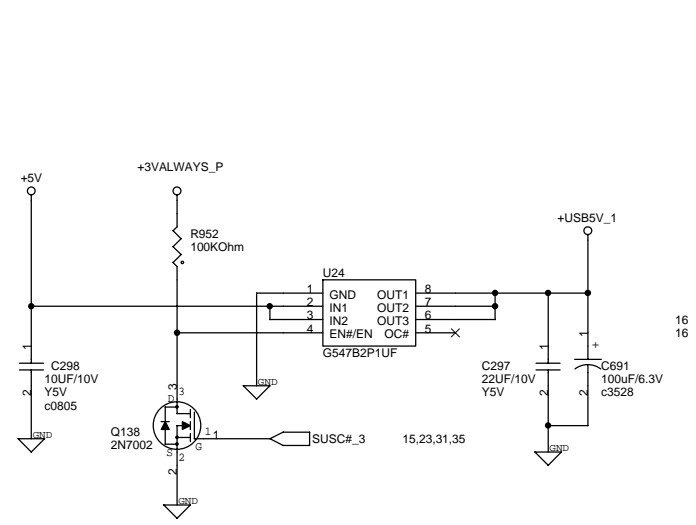


1 RESET-	2 GND
3 DATA7	4 DATA8
5 DATA6	6 DATA9
7 DATA5	8 DATA10
9 DATA4	10 DATA11
11 DATA3	12 DATA12
13 DATA2	14 DATA13
15 DATA1	16 DATA14
17 DATA0	18 DATA15
19 GND	20 (KEY)
21 DMARQ	22 GND
23 DIOW-	24 GND
25 DIOR-	26 GND
27 IORDY	28 CSEL
29 DMACK	30 GND
31 INTRQ	32
33 DA1	34 PDIAG
35 DA0	36 DA2
37 CS0	38 CS1
39 DASP	40 GND
41 +5VDC	42 +5VDC
43 GND	44 Reserved

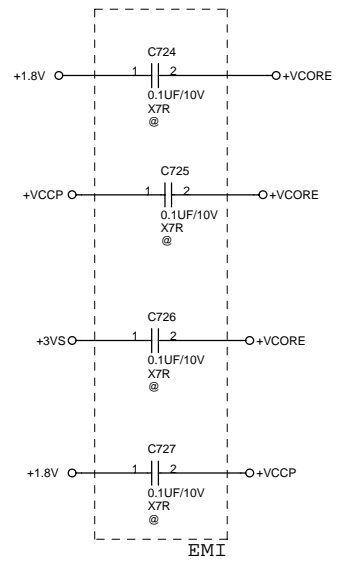
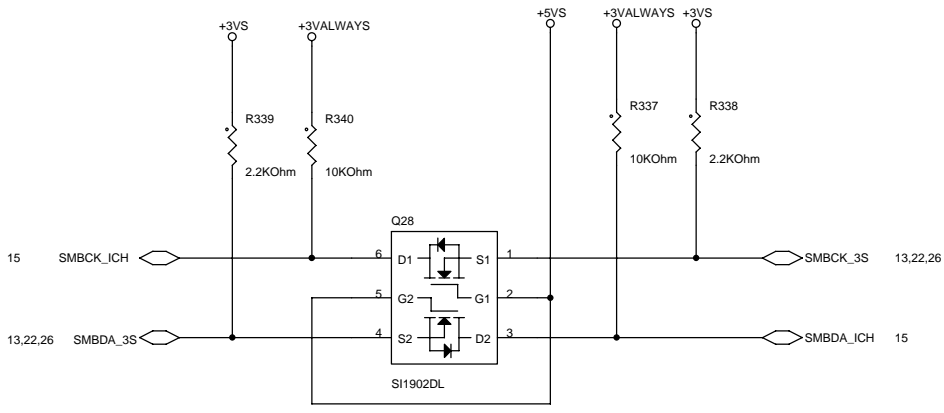




Unidirectional buffers (high impedance buffers) are required on both HSYNC and VSYNC to prevent potential electrical overstress and illegal operation of the GMCH, since some display monitors may attempt to drive HSYNC and VSYNC signals back to GMCH.

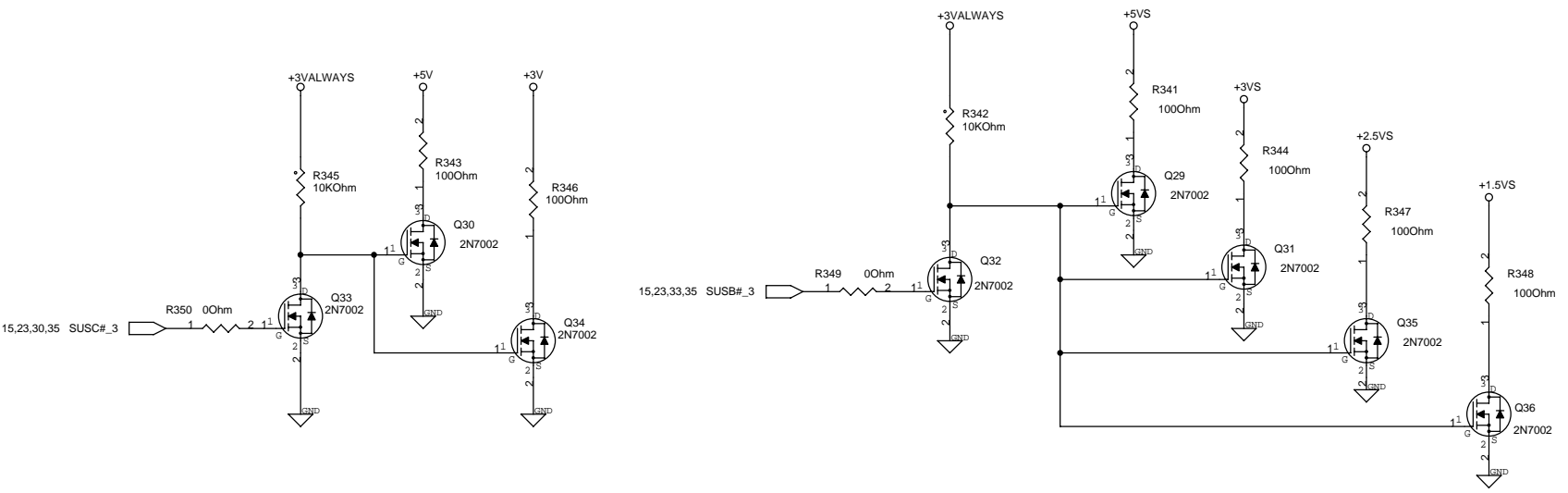


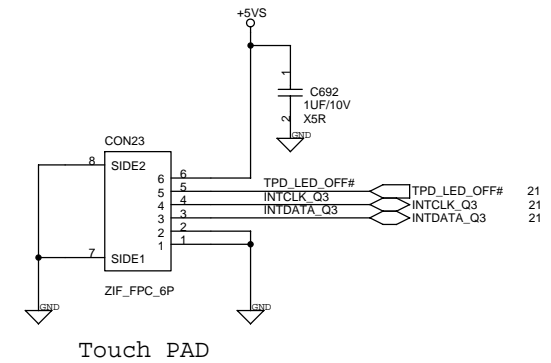
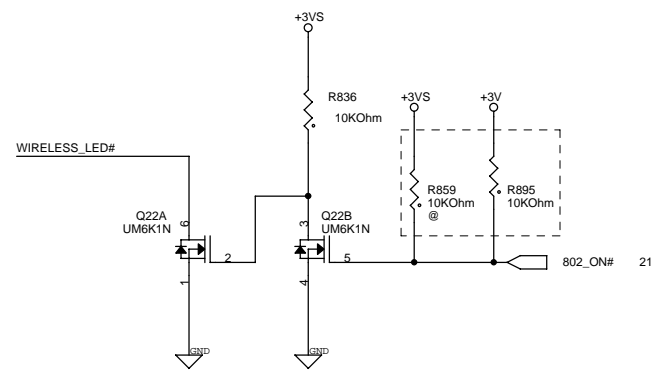
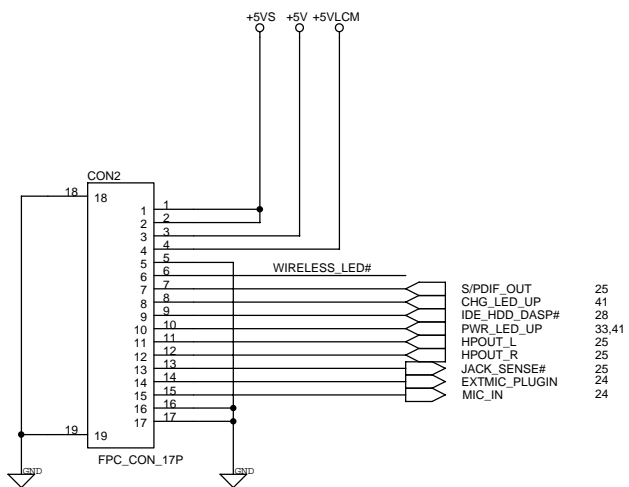
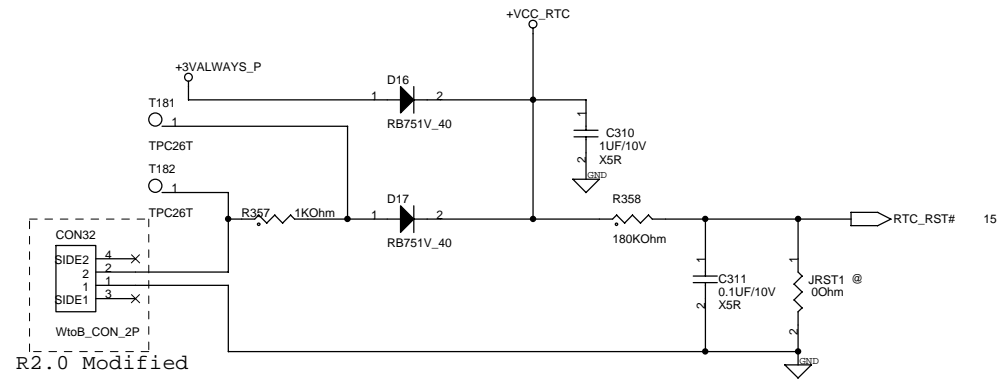
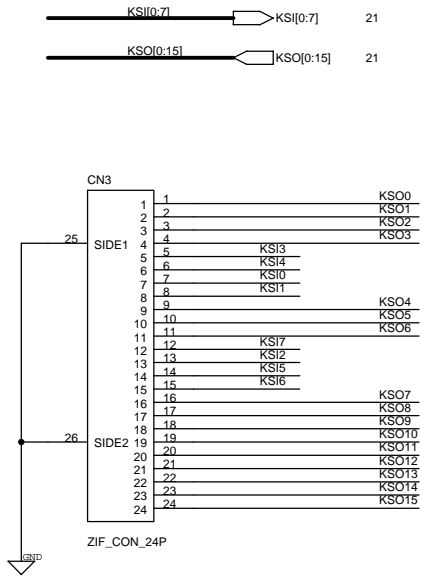
Pin Number	Name	Description
4	RSVD(PIO5)	Reserved for BT_Active output to 802.11g for co-existence. This is optional if you need activity signaling scheme
5	BT_Priority/CH_Clk (PIO4)	BT Priority AND Channel Clock for WCS
6	HW_DIS#(Optional)	Disable BT Device when low
7	CH_Data(PIO6)	Channel Data for WCS(Standard), or WLAN_Active input from 802.11b for Activity Signaling which is optional



AC_BAT_SYS	AC_BAT_SYS	27,35,36,37,38,40,42
A/D_VIN	A/D_VIN	33,42
+5V	+5V	7,17,24,30,32,33,35,41
+5VS	+5VS	17,20,21,23,24,25,26,28,29,32,35
+3VALWAYS	+3VALWAYS	15,16,17,18,21,23,35
+3VALWAYS_P	+3VALWAYS_P	23,25,30,32,33,35
+3V	+3V	18,20,21,23,30,32,33,35,37,41
+3VS	+3VS	9,13,15,16,17,18,20,21,22,23,24,26,27,28,29,30,32,34,35,37,38,39,40
+2.5VS	+2.5VS	7,9,10,17,29,39
+1.8V	+1.8V	7,9,10,11,12,13,37
+1.5VS	+1.5VS	4,7,9,16,17,38
+1.5VALWAYS	+1.5VALWAYS	17,35
+0.9VS	+0.9VS	14,37
+VCC_GMCH	+VCC_GMCH	4,5,6,7,9,10,15,17,26,38
+VCCP	+VCCP	4,5,6,7,9,10,15,17,26,38
+VCCO	+VCCO	5,21,40
+VCC_RTC	+VCC_RTC	15,17,32
+5VA_CODEC	+5VA_CODEC	24,25
+5VA	+5VA	17,36,39
+2.5VREF	+2.5VREF	39,41,42

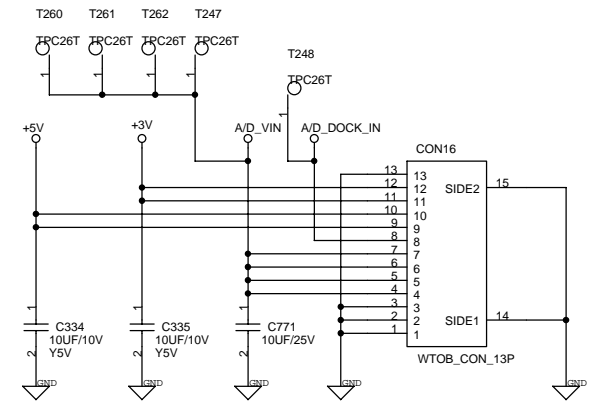
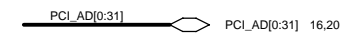
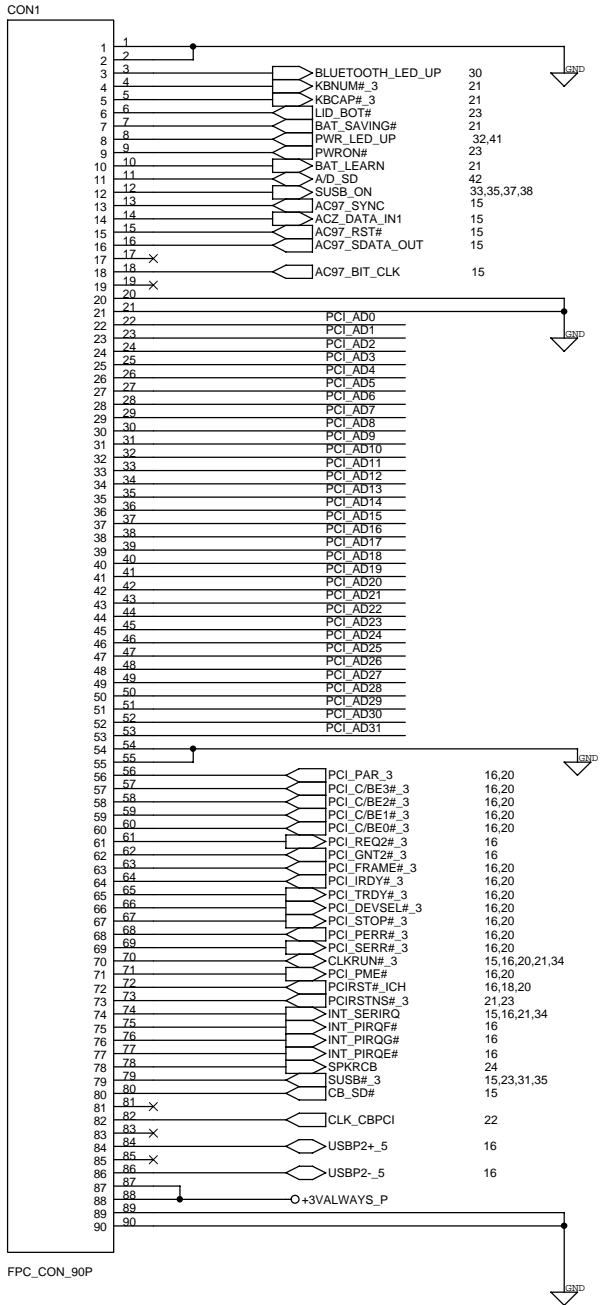
Discharge circuit for power fast down

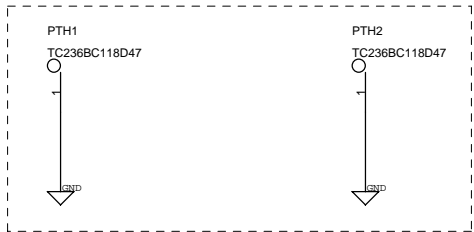
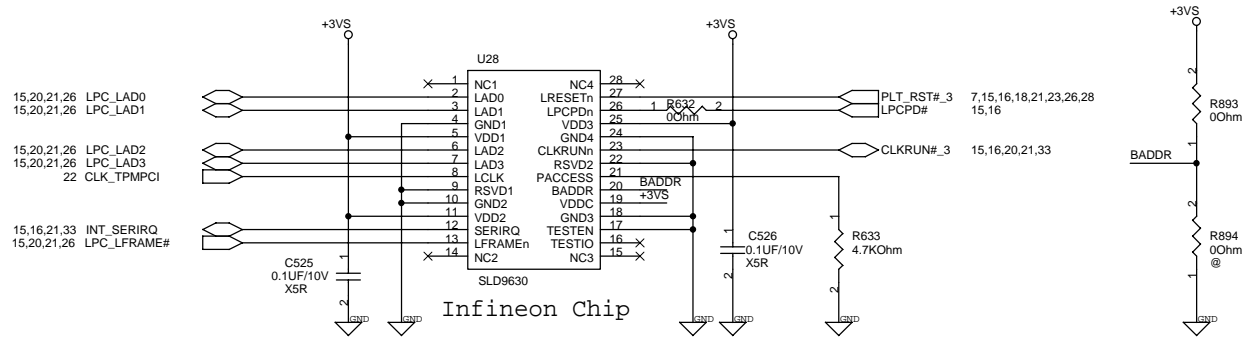




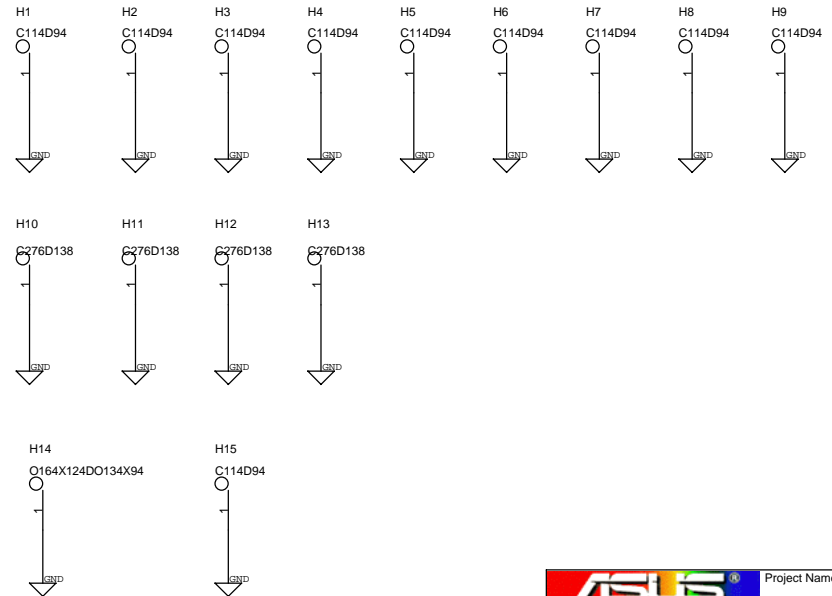
Audio Board

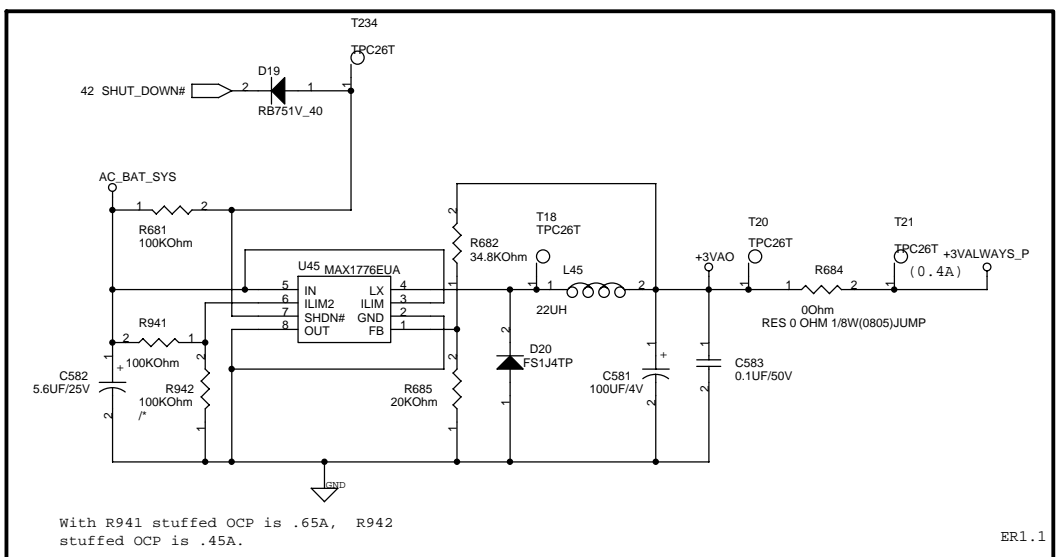
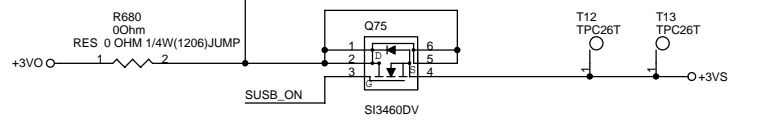
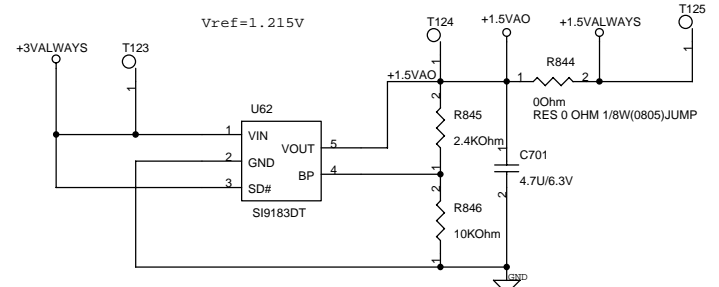
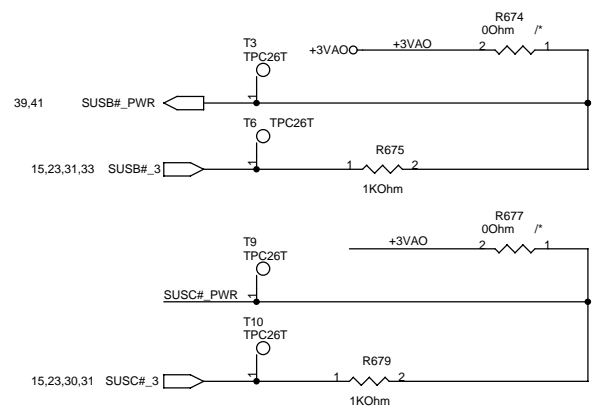
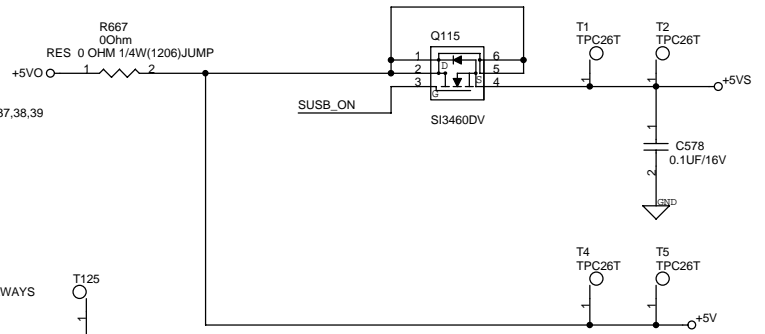
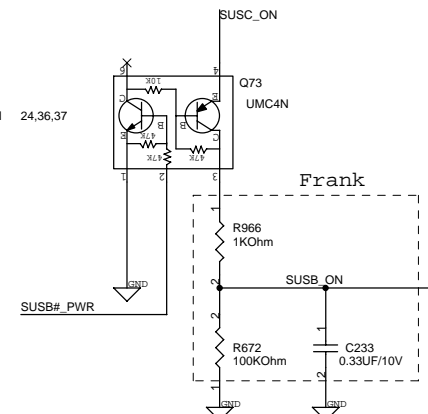
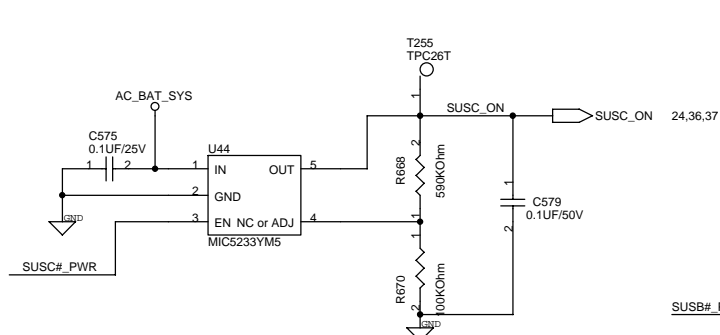
Touch PAD

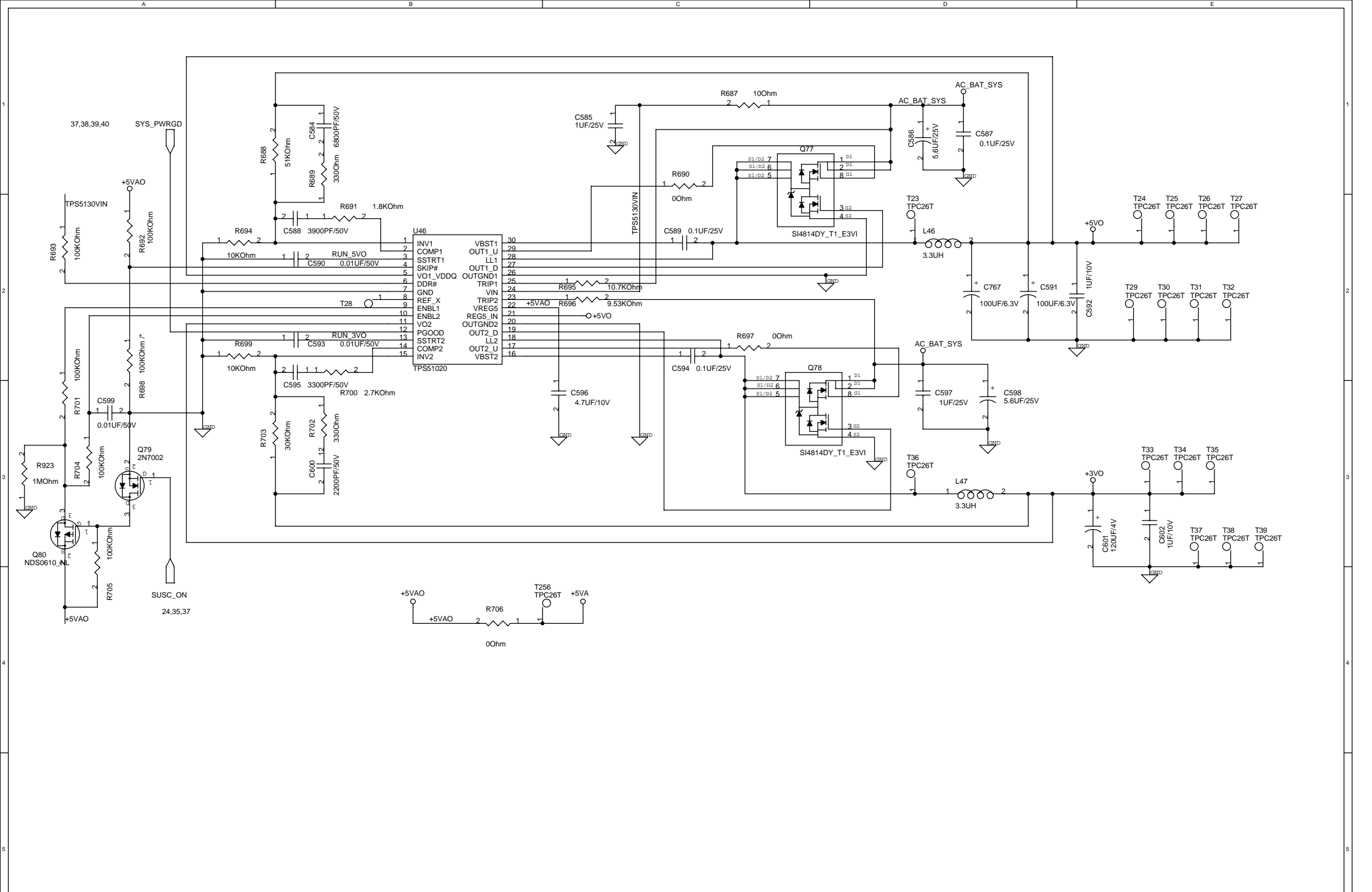


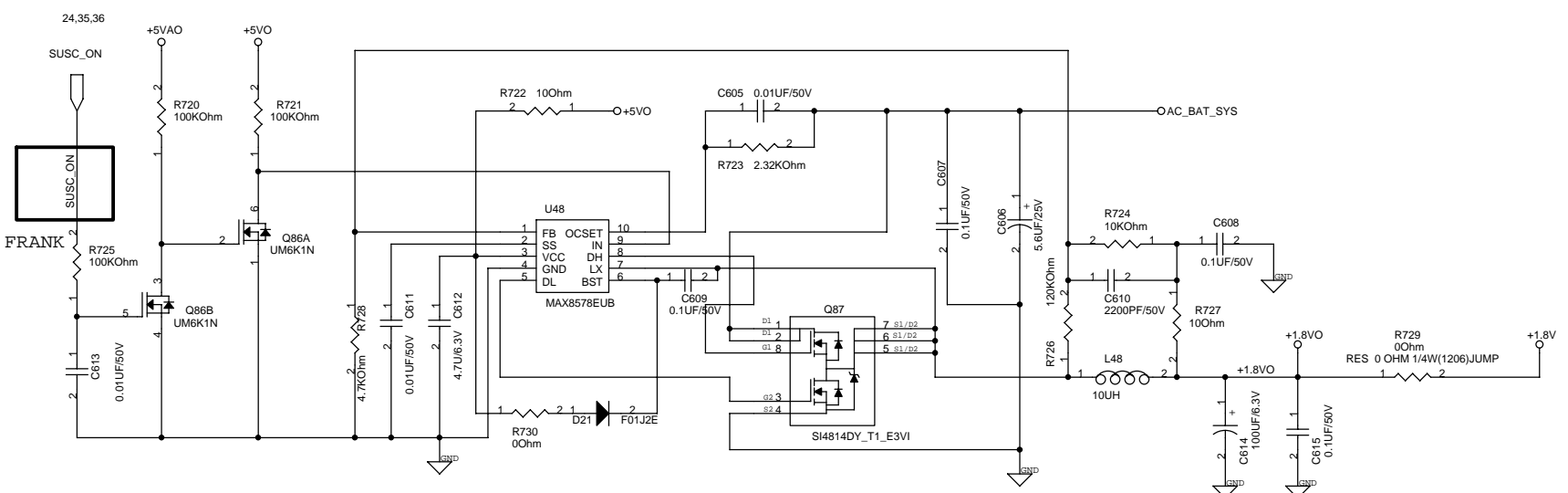
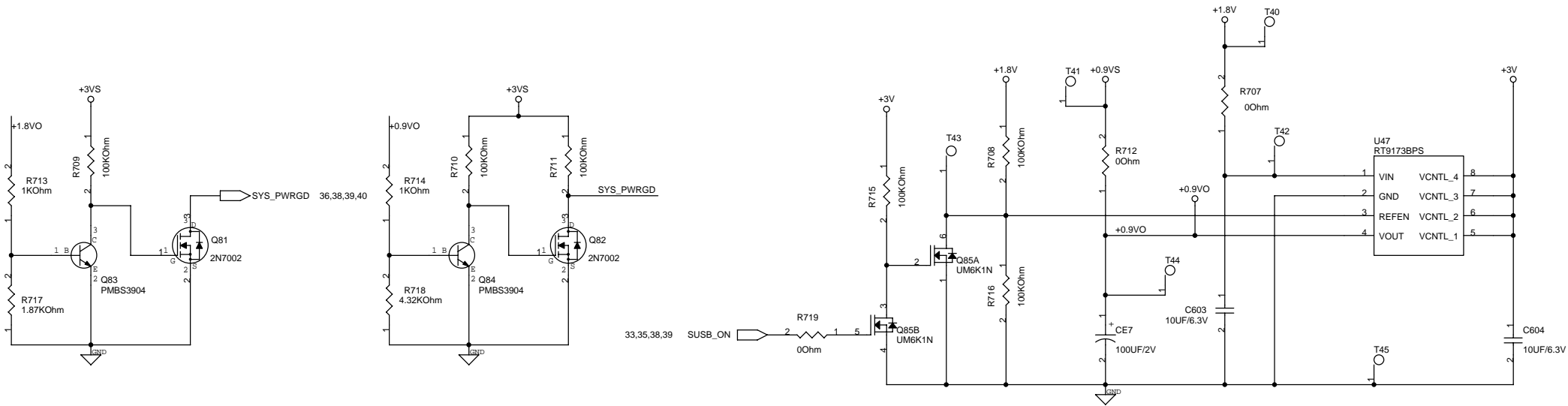


For ICH6 Thermal
13GN8K10T010



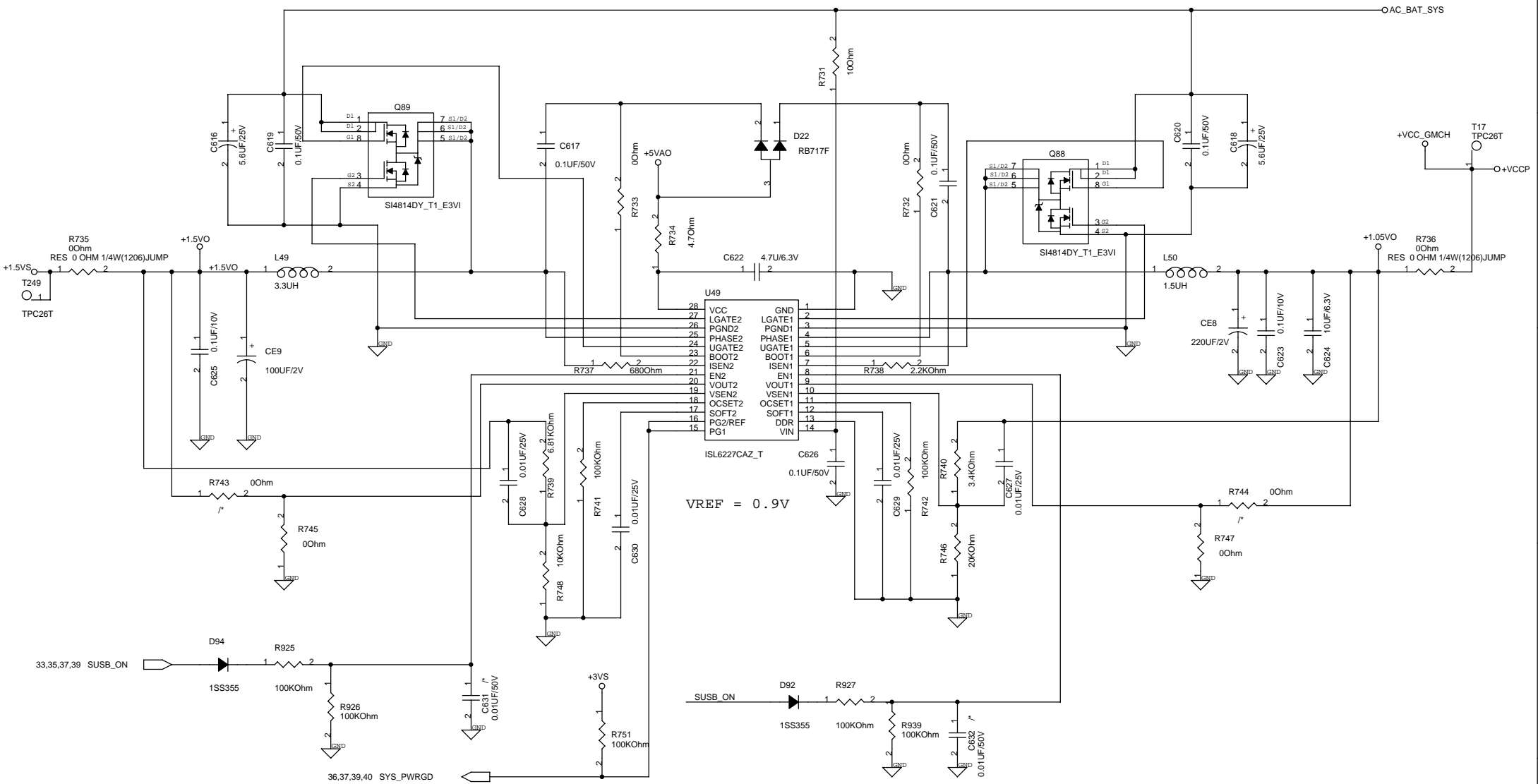


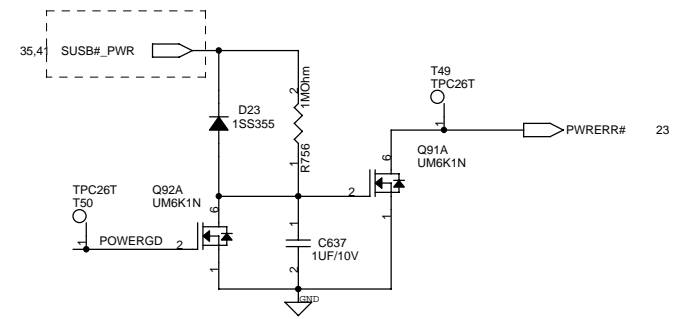
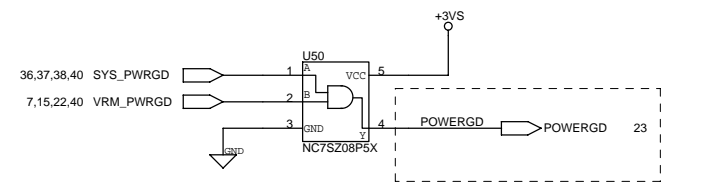
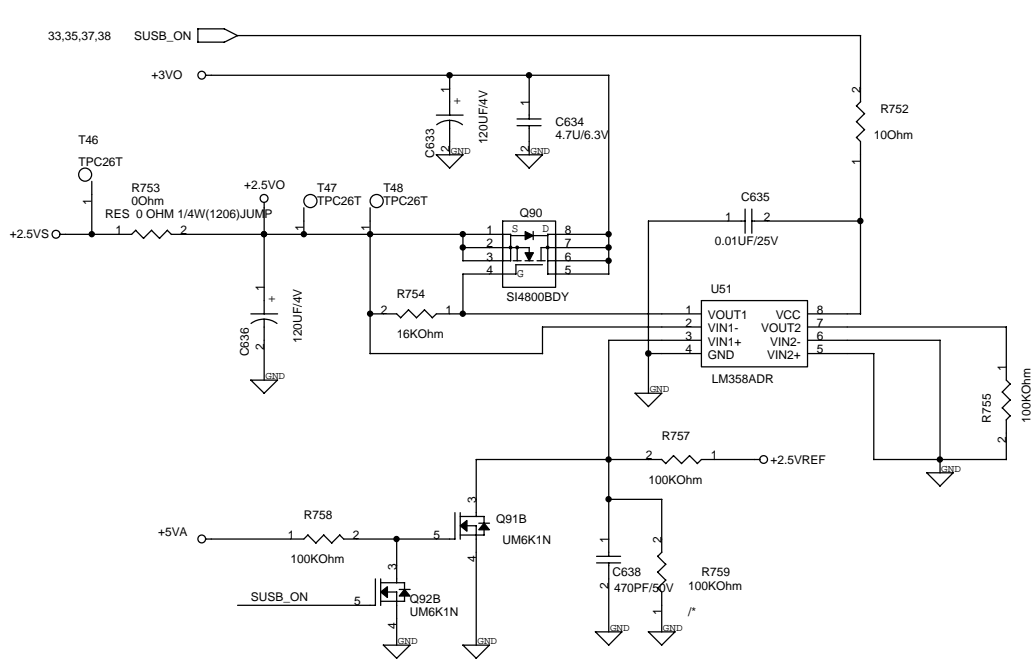




Need to change R728 to 4.53K ohm 1% 0603.

<Variant Name>





<Variant Name>



PROJECT: U5A

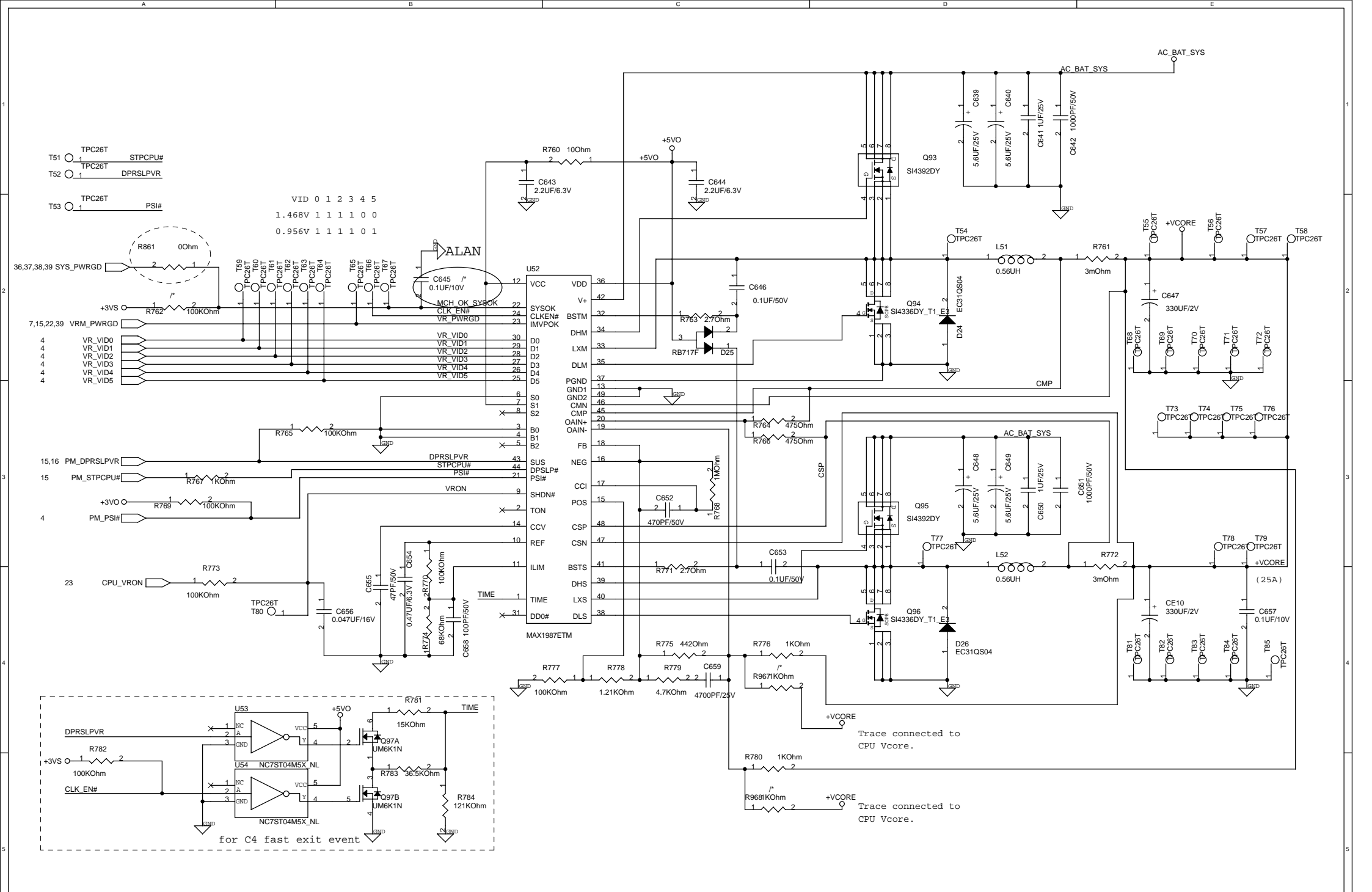
REVISION
2.0

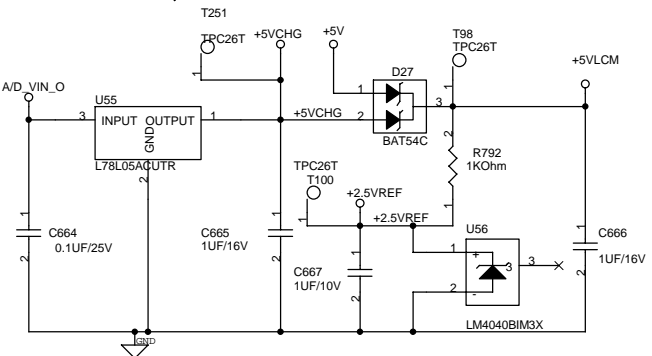
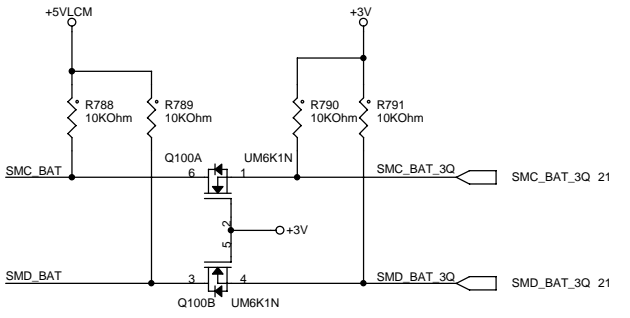
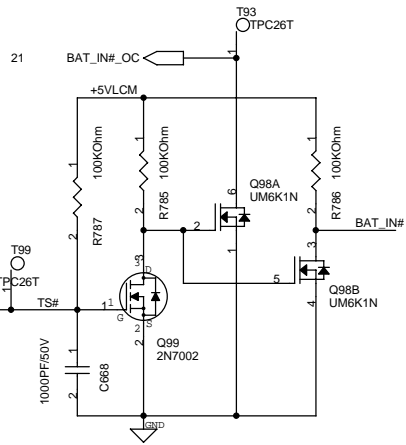
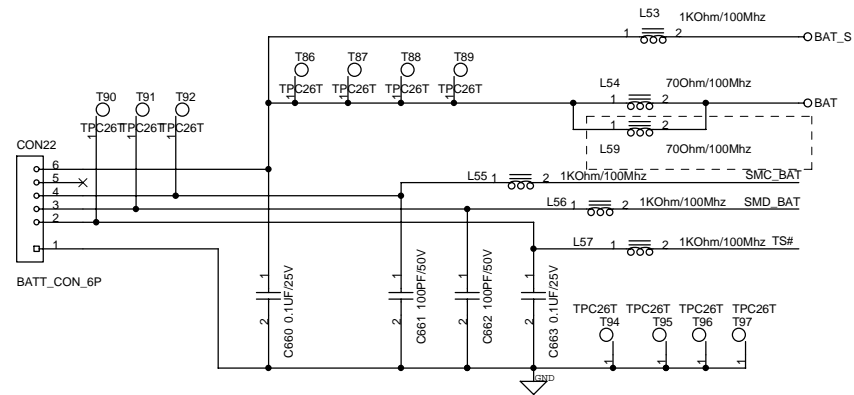
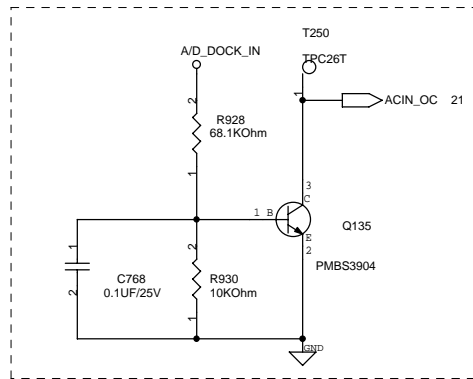
DATE: Tuesday, September 27, 2005
SHEET 39 OF 46

DESCRIPTION: 2.5VS_PWRGD

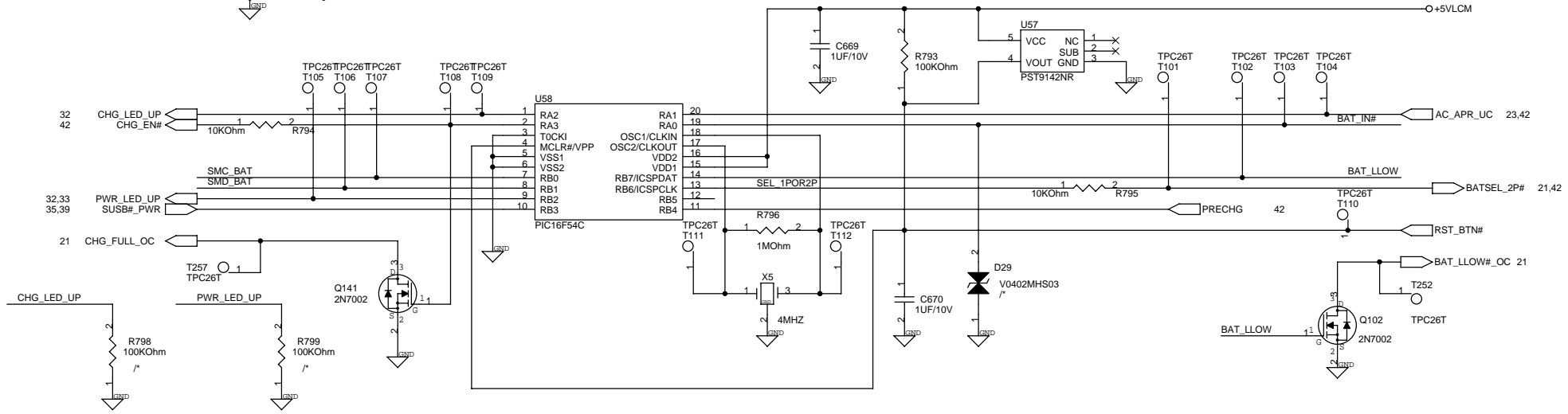
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RELEASE DATE :

DESIGN ENGINEER :



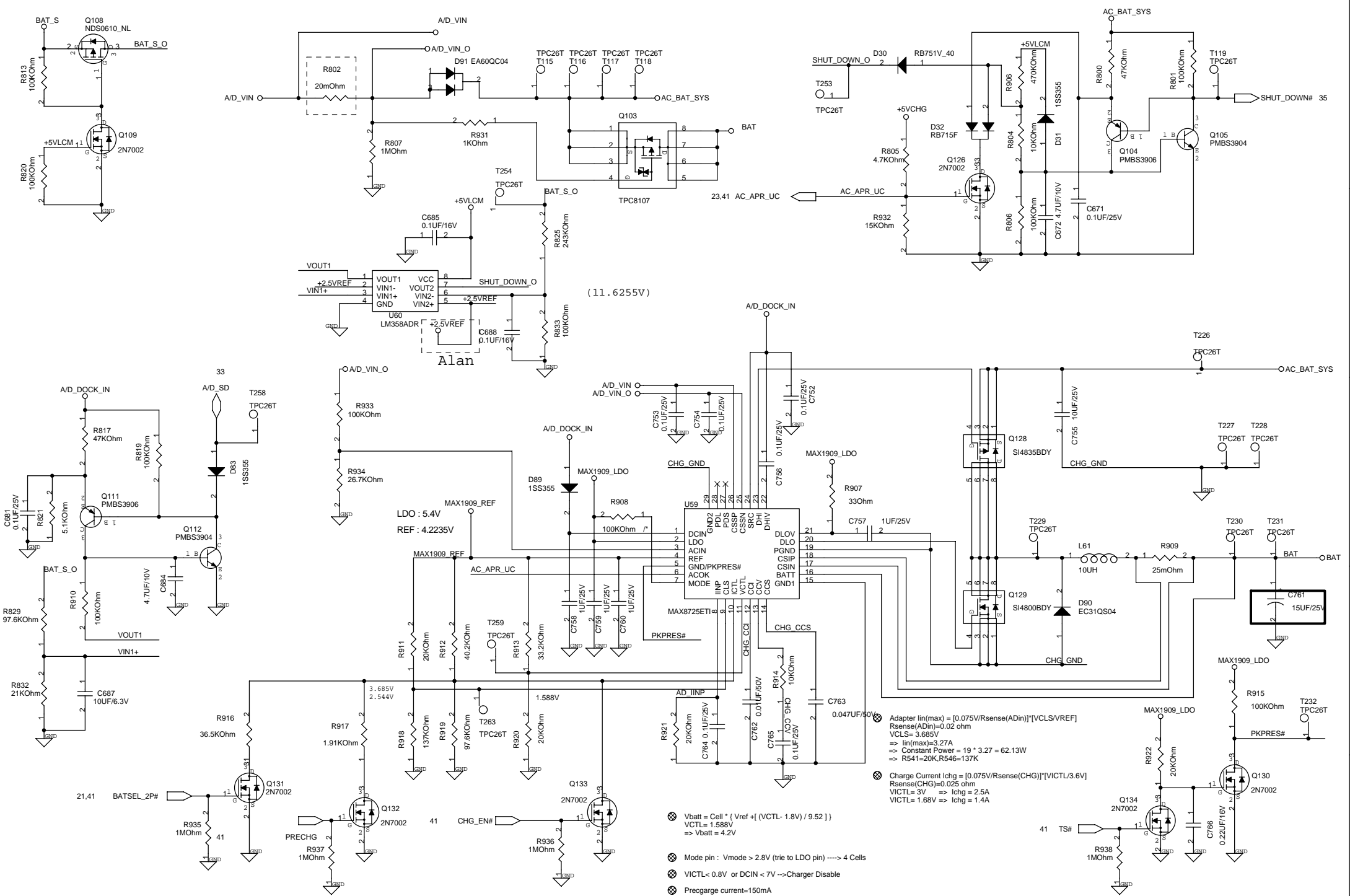


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<Variant Name>

ASUS	PROJECT: U5A		REVISION	DATE: Tuesday, September 27, 2005	DESCRIPTION:	SCHMATIC FILE NAME :	DESIGN ENGINEER :
			2.0	SHEET 41 OF 46	DCIN_BATCON_BATIN_+5VLCM_PIC	RELEASE DATE :	



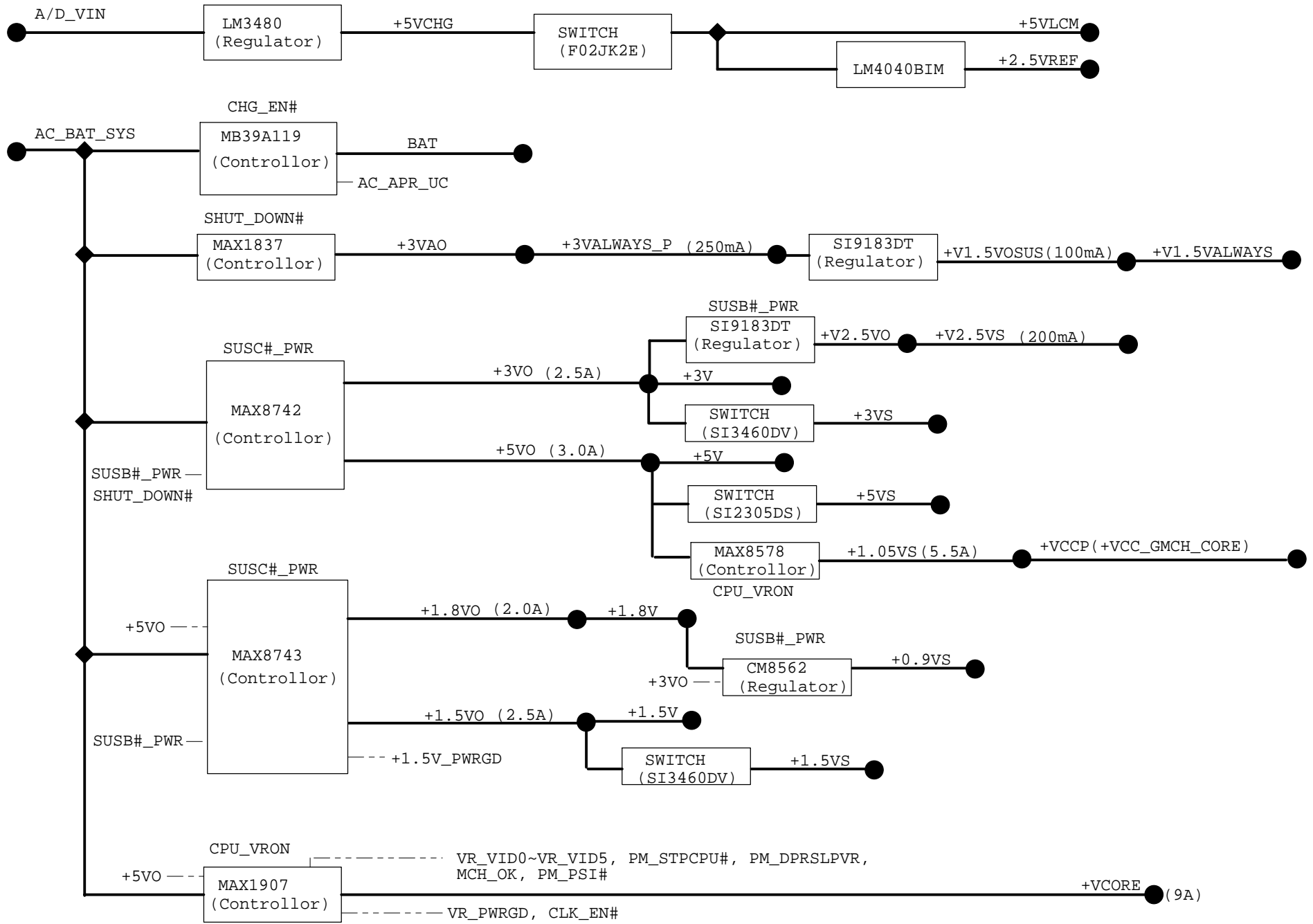
(11.6255V)

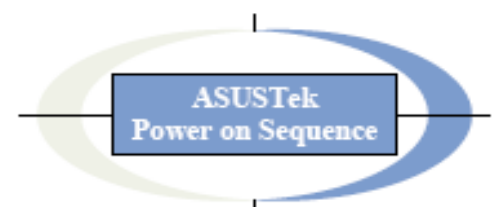
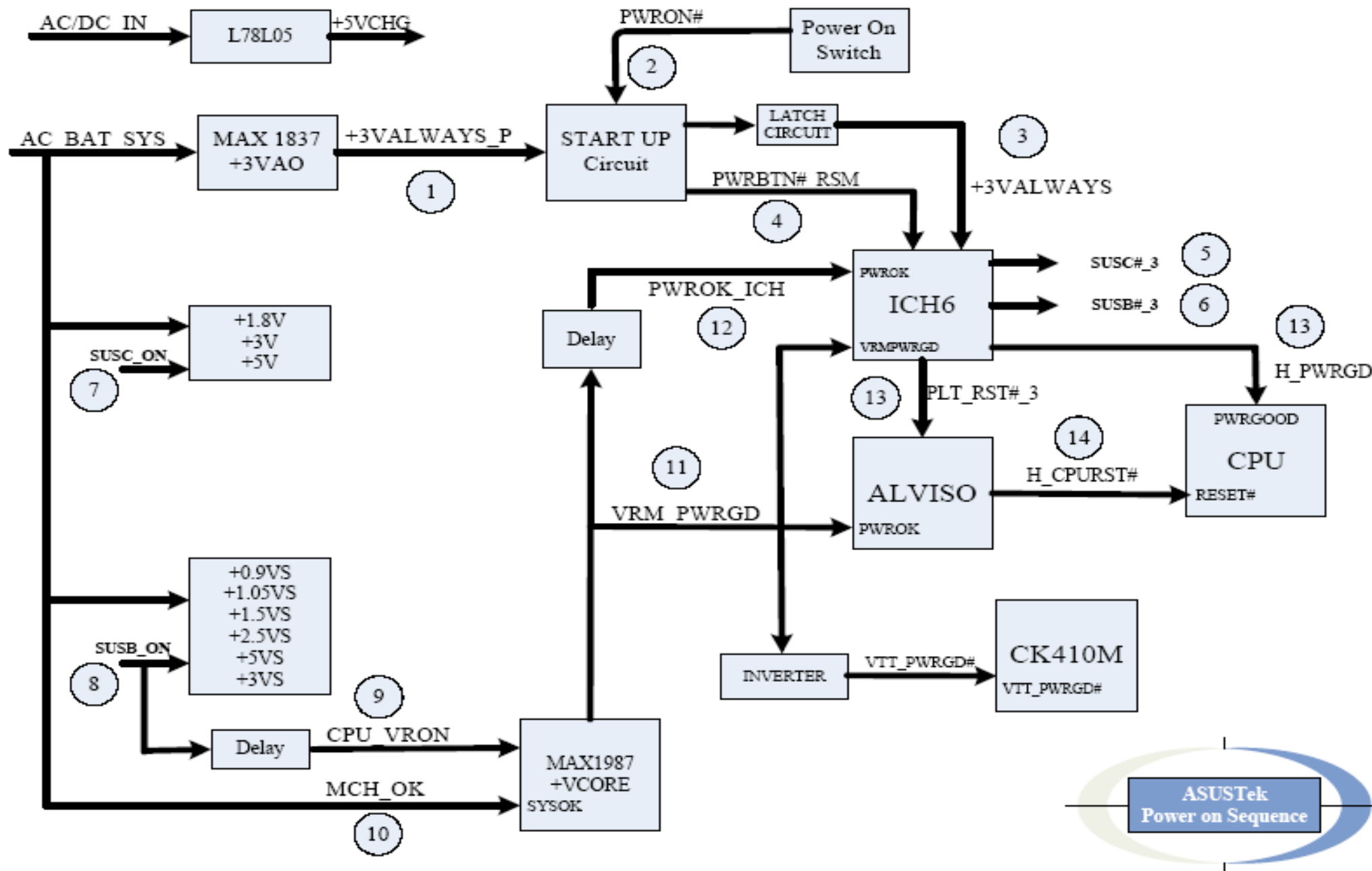
Alan

$\text{Adapter lin(max)} = [0.075V / \text{Rsense(ADin)}] * [\text{VCLS} / \text{VREF}]$
 $\text{Rsense(ADin)} = 0.02 \text{ ohm}$
 $\text{VCLS} = 3.685V$
 $\Rightarrow \text{lin(max)} = 3.27A$
 $\Rightarrow \text{Constant Power} = 19 * 3.27 = 62.13W$
 $\Rightarrow R541 = 20K, R546 = 137K$

$\otimes \text{ Charge Current } \text{Ichg} = [0.075V / \text{Rsense(CHG)}] * [\text{VICTL} / 3.6V]$
 $\text{Rsense(CHG)} = 0.025 \text{ ohm}$
 $\text{VICTL} = 3V \Rightarrow \text{Ichg} = 2.5A$
 $\text{VICTL} = 1.68V \Rightarrow \text{Ichg} = 1.4A$

- $\otimes \text{ Vbatt} = \text{Cell} * (\text{Vref} + [(\text{VCTL} - 1.8V) / 9.52])$
 $\text{VCTL} = 1.588V$
 $\Rightarrow \text{Vbatt} = 4.2V$
- $\otimes \text{ Mode pin : } \text{Vmode} > 2.8V \text{ (try to LDO pin)} \rightarrow 4 \text{ Cells}$
- $\otimes \text{ VICTL} < 0.8V \text{ or DCIN} < 7V \rightarrow \text{Charger Disable}$
- $\otimes \text{ Preccharge current} = 150mA$





Revision History

Rev1.1_EE

1. Replace LAN controller Marvell 8001 with RealTek 8111B because of large power consumption of 8001 when system power on-----Page 18.
2. Change audio codec vender from RealTek ALC861VS to ADI1986A for cost issue. -----Page 24.
3. Add a cap (22pF) to CLK_KBCPCI for EMI issue -----Page 22.
4. The net BTPWRCL# need be pulled up to +3V through a resistor due to port 53 is open drain ----- Page 21.
5. Replace internal mic near codec to solve the white noise problem ----- Page 24.
6. Remove C620 to avoid damage HDD motor. -----Page .
7. Add a EC pin (port 57)to control the TPD LED on / off (synchronous to Fn+F9) -----Page 21 .
8. Delete the Pin 5 of CON2 (LID_BOT#) and connect to ground. -----Page 32.
9. Replace net AC/DC_In with A/D_DOCK_IN due to D91 is removed to main board from I/O board -----Page 33.
- 10.Connect pin 88 of CON1 to +3VALWAYS_P and swap PWR_LED_UP from pin 88 to pin 8 -----Page 33.
- 11.Add a GPIO pin (CODEC_SHDN#) to switch +5VA_CODEC power on or off -----Page 24.
- 12.Add a circuit to control power of blue tooth -----Page 30.
- 13.Remove HDD protection IC circuit-----Page 34.
- 14.Add a control circuit to dominate USB power for avoiding that self power leakage current flow into +5V when system is powered off. -----Page 30.
- 15.Add a MOS to control wirless on or off -----Page 20.
- 16.Change vender of DDR2 SODIMM connector from QUASAR to TYCO for cost issue. -----Page 13.

Rev 2.0_EE

1. Swap pin of RTC battery to match battery module define. -----Page 32.
2. R896 need be pulled up to +3VS to solve problem S3 (S4) wake on LAN failed issue. -----Page 18.
3. Change R156 value from 1K ohm (2.2 volt) to 680 ohm (3.3 volt) for correcting PCIE_WAKE# level. -----Page 18.
4. Remove C269 to solve pop noise when entry S3 state-----Page 25.
5. Remove LAN power control circuit -----Page 18.
6. Remove ODD device power control circuit -----Page 28.
7. Redefine pin define of CON5 to support EDI and color enhanced function-----Page 27.
8. Change D8 compoment from F01J4L to F01J2E to provide corrcet level (0.42 volt --> 0.24 volt)of back_off# after LID_RSM# activated-----Page 23.
9. Change C579 value to sovlve that power button LED and power LED will flash once after power off system-----Page 35.
- 10.Add a 100k ohm to CON25.6 to provide correct level-----Page 30.
- 11.Reserve caps on each pin of CON26 for ESD issue-----Page 30.

Revision History

Rev1.1_Power

1. Page 40: Changed net name from "MCH_OK" to "SYS_PWRGD"
2. Page 36: Added R923(1M) ohm resistor for discharging voltage to Q80.3; R695 changed to 7.47K(increase OCP); R696 changed to 9.53K(increase OCP).
3. Page 36: +5V output current upgraded from 2.5A to 4.5A changed L46 to 3.3uH and added C767 (100uF/6.3V). Changed L46 to 3.3uH.
4. Page 37: Changed C610 to 3300pF (increase frequency to reduce ripple current); R726 changed to 120K, R728 changed to 4.7K, R723 changed to 4.7K.
5. Page 38: Changed L50 to 3.3uH (to meet transient spec). R742 to 100K ohm (OCP). R741 to 100K ohm (OCP).
6. Page 40: R775 to 442 ohm, R764 and R766 to 475 ohm to lower the droop voltage. C647 and CE10 to 330uF to meet transient spec. R774 to 63.4K (OCP 30A).
7. Page 42: Changed charger IC (U59) from MB39A119 to MAX8725.
8. Page 38: Added components (D924, R925, R926, D92, R927, R939) to make sure the enable pins (U49.21, U49.8) does not exceed 5V.
9. Page 42: Added D91, this diode is removed from the I/O BD.
10. Page 41: Changed net name on U55.3 to "A/D_VIN_0".
11. Page 35: Updated 3VAO circuit to 600mA.
12. Page 37: The enable signal to +1.8V changed to "SUSC_ON".
13. Page 42: Q103 source is connected to AC_BAT-SYS.
14. Page 42: C761 foot print changed to C7343d-h122.

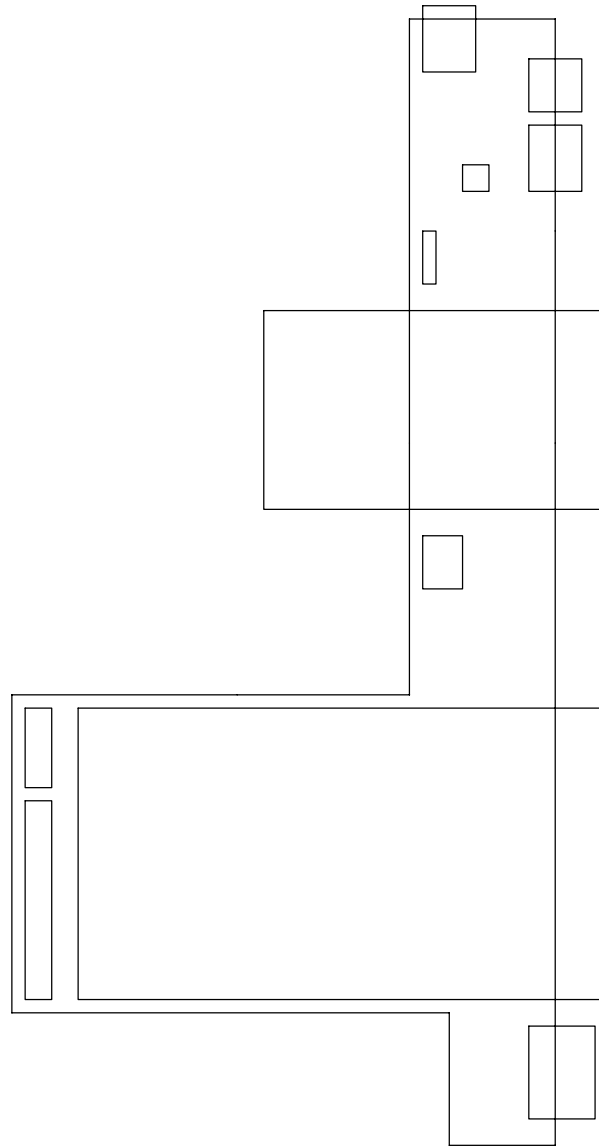
Rev1.2_Power

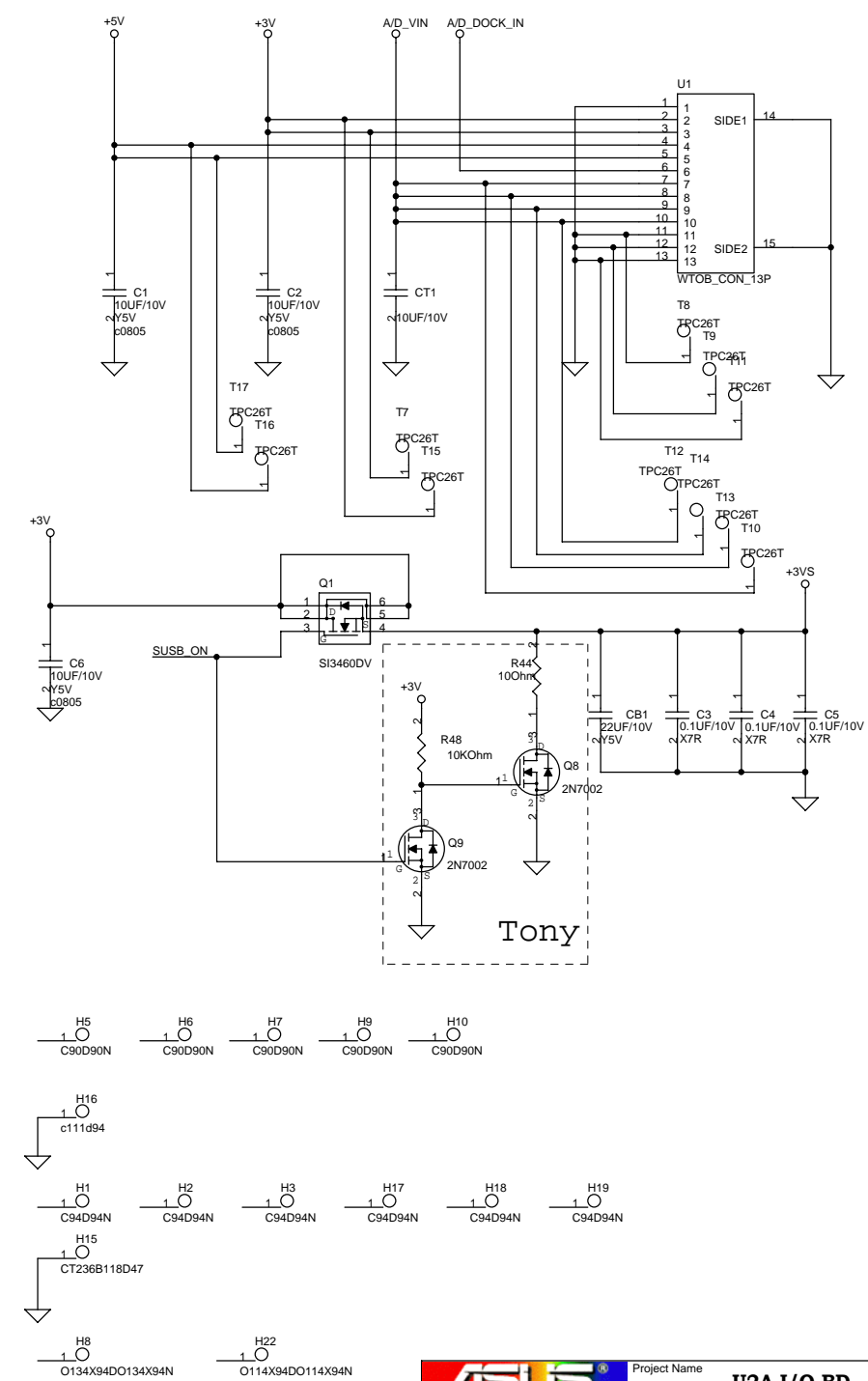
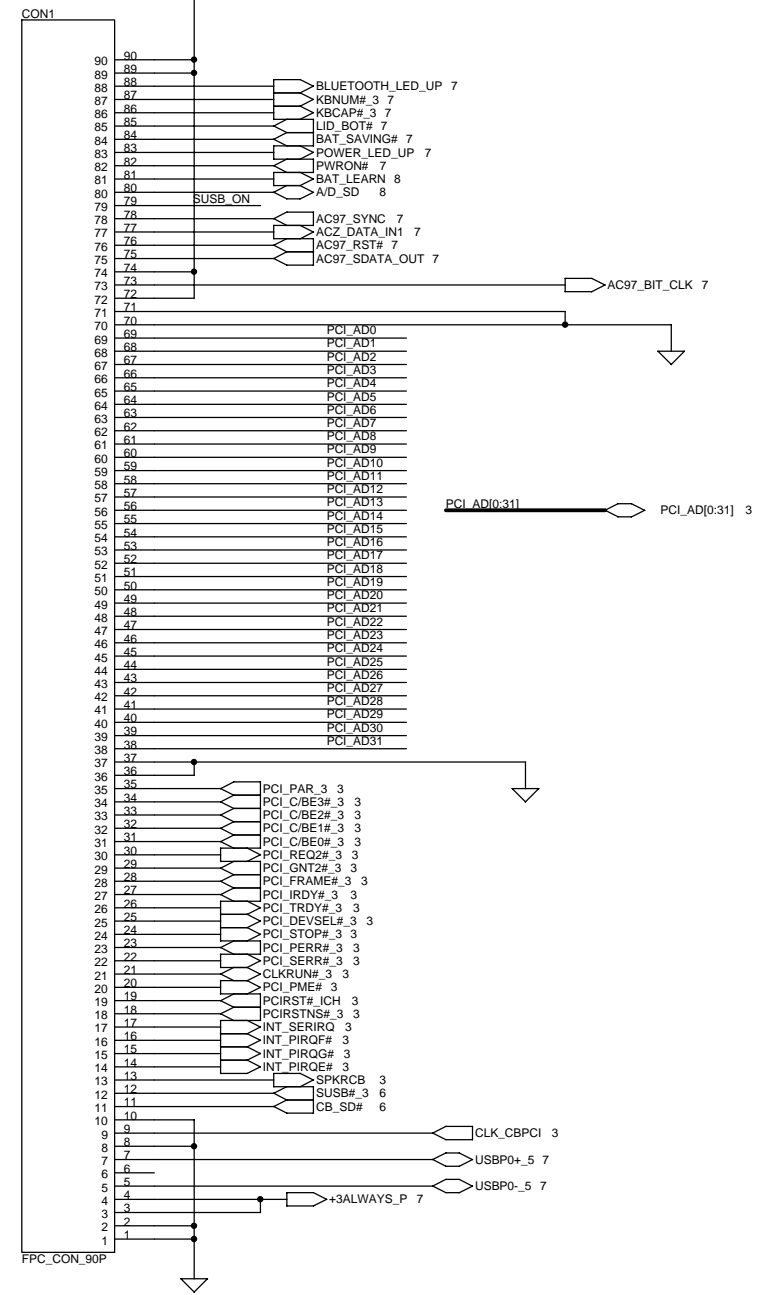
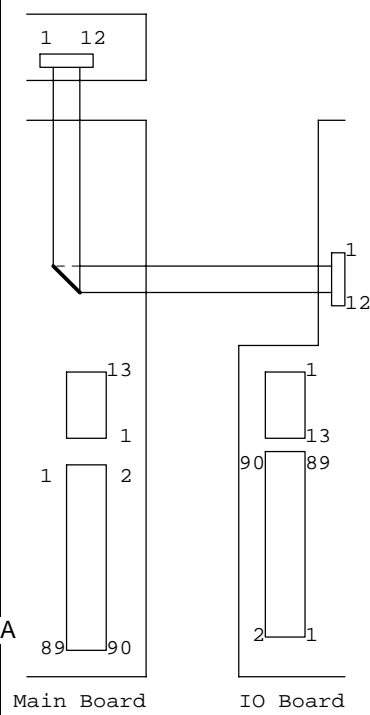
1. Page 42: After SMT, changed R908 to /*, this is 3 battery charge voltage setting. Replaced R802 with 20m Ohm resistor to improve total power.
2. Page 36: Changed C585 footprint to C0805.
3. Page 35: After SMT, changed R942 to /*, R941 is stuffed with 100KOhm. This is to increase OCP for +3VALWAYS from .45A to .65A. Changed C579 from 1uF to 0.1uF to speed up SUSC_ON time.
4. Page 37: Changed R723 to 2.32K OCP2.5A. Changed C610 to 2200pF, increase frequency from 190KHz to 240KHz. Changed R728 to 4.53K, Vout 1.811V.
5. Page 38: Changed L50 to 1.5uH/10A, changed L49 to 3.3uH/3.5A to improve transient response.
6. Page 40: Changed C641, C651 to 1000pF/50V X7R 10%.
7. Page 37: Changed D21 footprint to "sod323".
8. Page 40: 8/31/05 Added two more resistors for sensing the Vcore voltage more accurately.
9. Page 42: 9/5/05: changed Q103 to Fairchild part because Toshiba does not respond to GA.
10. Page 35: 9/5/05: changed Q73 to Rohm part because Toshiba does not respond to GA.
11. Page 41: 9/5/05: Changed L54 and L59 to 3A bead. U58.3 tied to Gnd.
12. Page 40: 9/8/05: Changed Q93 and Q95 to SI4932, changed Q94 and Q96 to SI4336.
13. Page 40: 9/9/05: Changed L51 and L52 to .56uH/15A 10 x 10 mm packaging to solve thermal issue.

PROJECT U5A IO & Audio Board

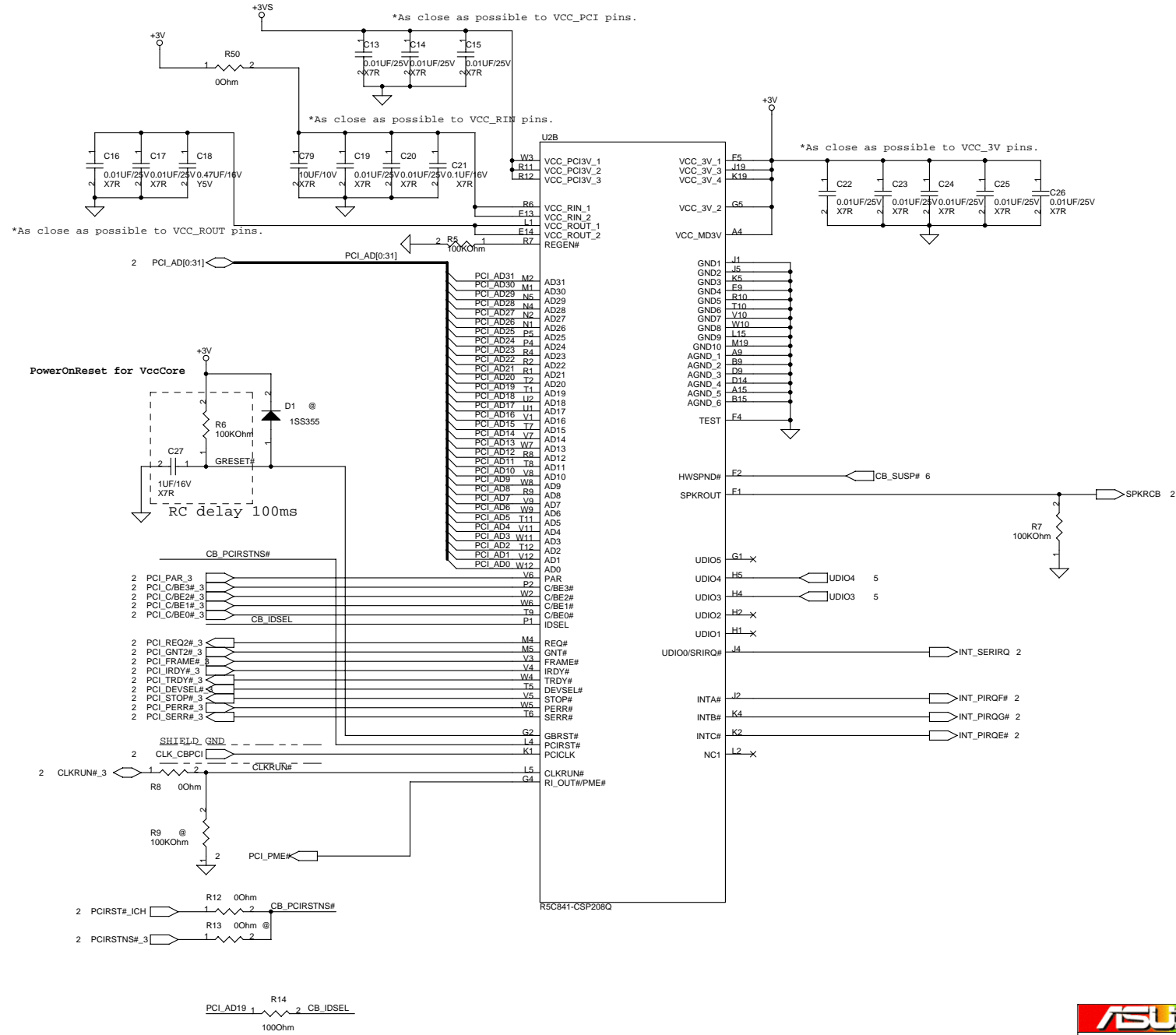
Revision History

R1.0	SR	2005/01/17
R1.1	SR	2005/06/2
R1.2	ER	2005/07/6
R2.0	PR	2005/09/21



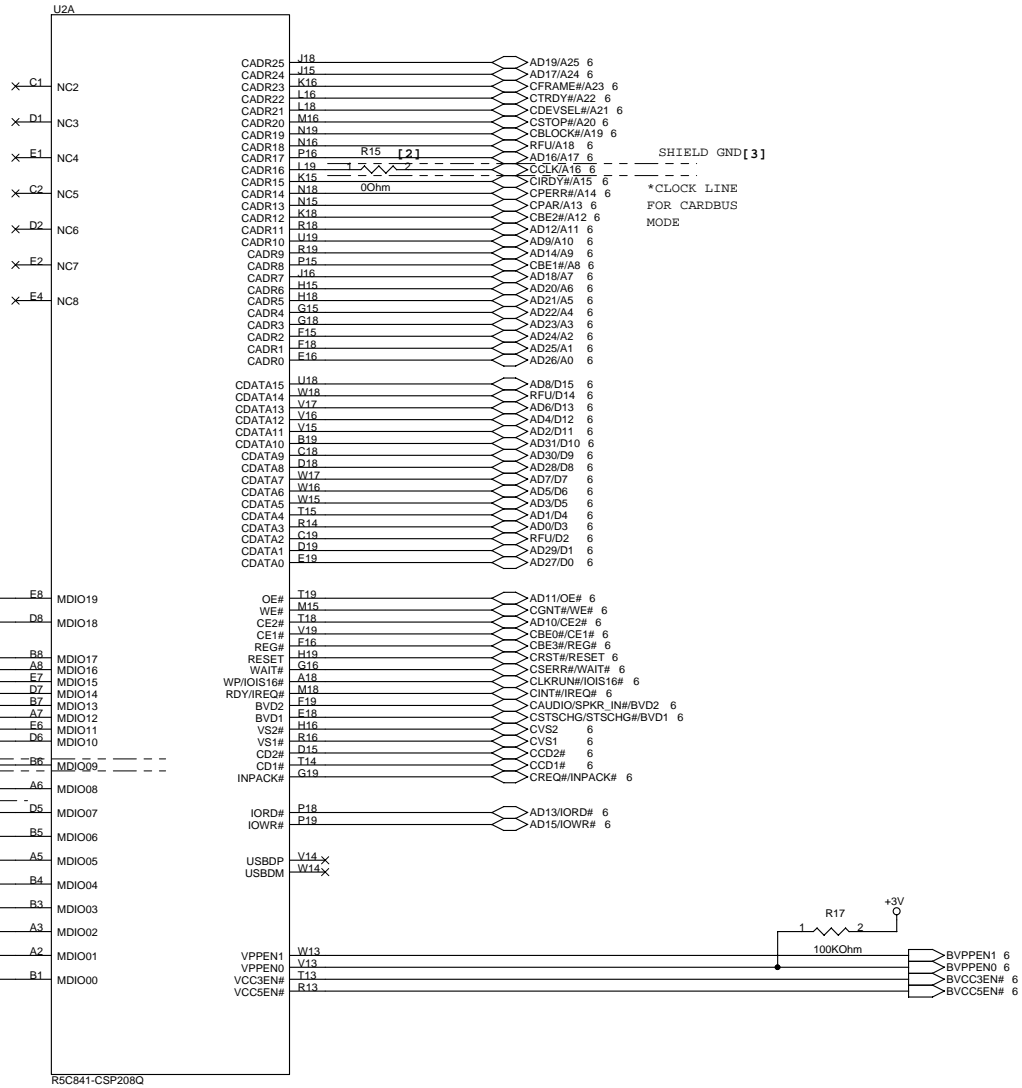
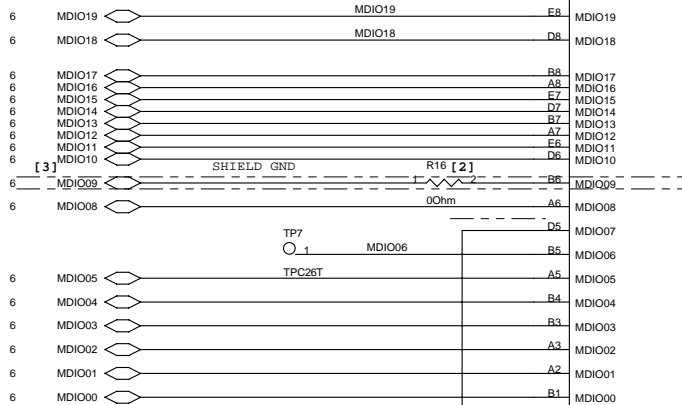


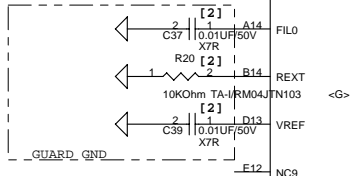
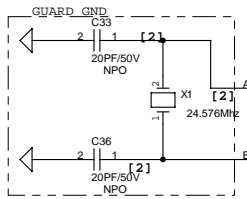
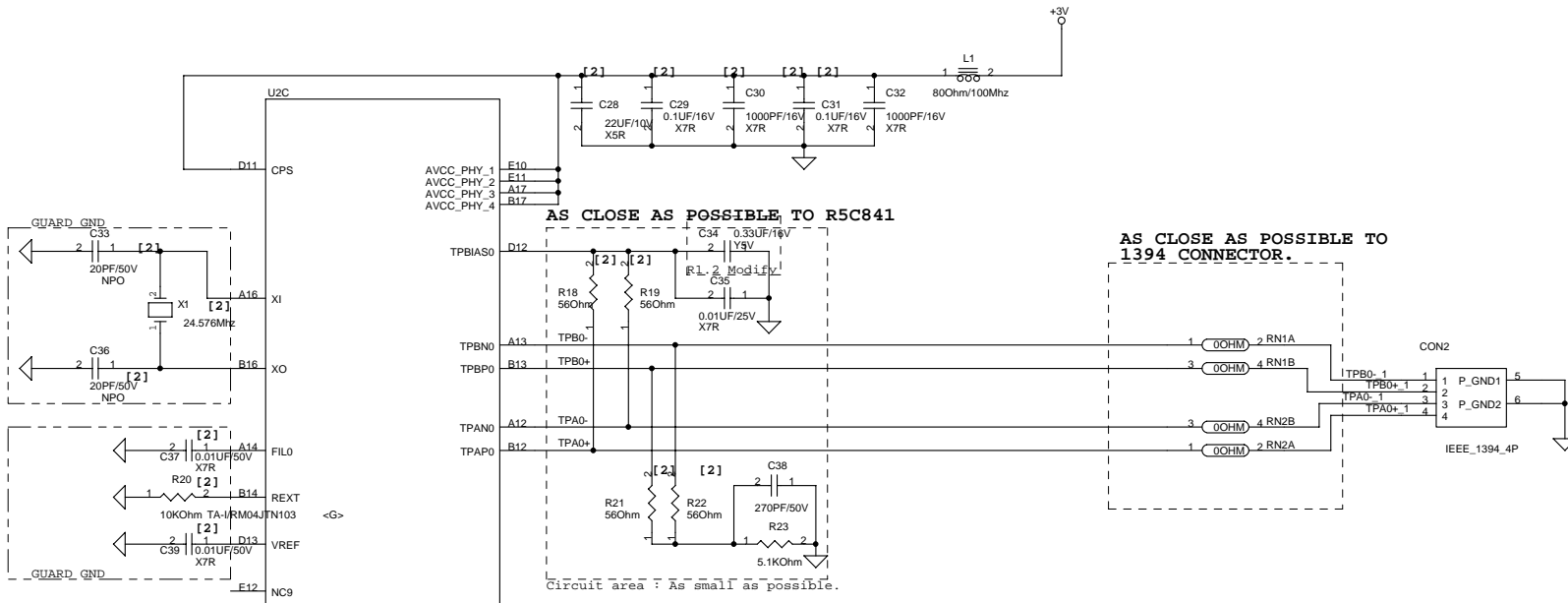
ASUS		Project Name	U2A I/O BD.
ASUSTek COMPUTER INC		Engineer:	Tony_Lin
Size	Custom	Title : Bridge MB and Sub Board	
Date: Thursday, September 22, 2005	Sheet	2	of 9



- [1] NOT INSTALLED
- [2] AS CLOSE AS POSSIBLE TO DEVICE TERMINALS.
- [3] CLK LINES : SHIELDED BY GND. (RECOMMENDED)

MDIO01--> MS Card Detect	MDIO02--> xDCE#
MDIO03--> SD Write Protect	MDIO05--> SD Power Control 1 / xDWP
MDIO04--> SD Card Power0 Control/ MS Power Control	MDIO06--> xD/MS/SD LED Control
MDIO07--> SD External Clock/ MS External Clock	MDIO14--> xD Data
MDIO08--> SD Command/MS Bus State	MDIO15--> xD Data
MDIO09--> SD Clock/MS Clock	MDIO16--> xD Data
MDIO10--> SD Data 0/MS Data 0	MDIO17--> xD Data
MDIO11--> SD Data 1/MS Data 1	MDIO18--> xD CLE
MDIO12--> SD Data 2/MS Data 2	MDIO19--> xD ALE
MDIO13--> SD Data 3/MS Data 3	



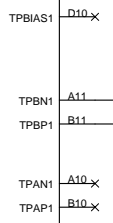
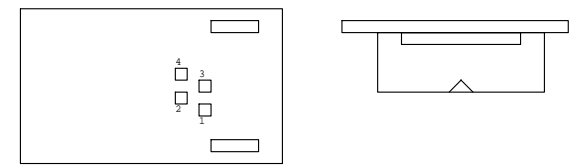


AS CLOSE AS POSSIBLE TO R5C841

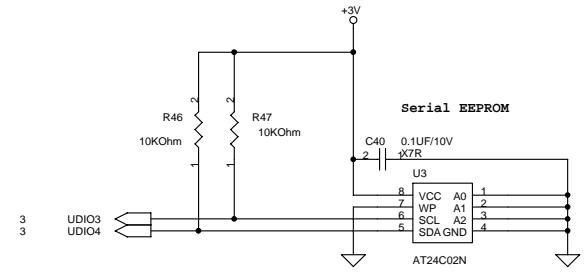
AS CLOSE AS POSSIBLE TO 1394 CONNECTOR.

*TPA/TPAH, TPB/TPB# pair trace : As close as possible.
 *TPA/TPAH, TPB/TPB# pair trace : Same length electrically.
 *TPBIAS traces from pin to the filter capacitors : Short and wide.
 *Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

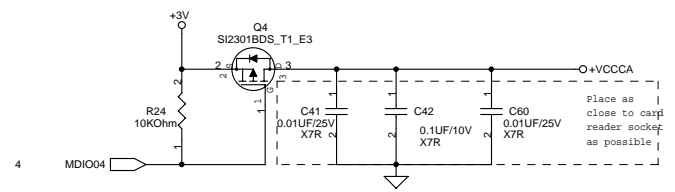
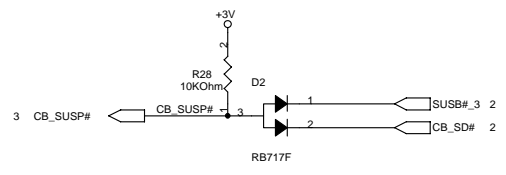
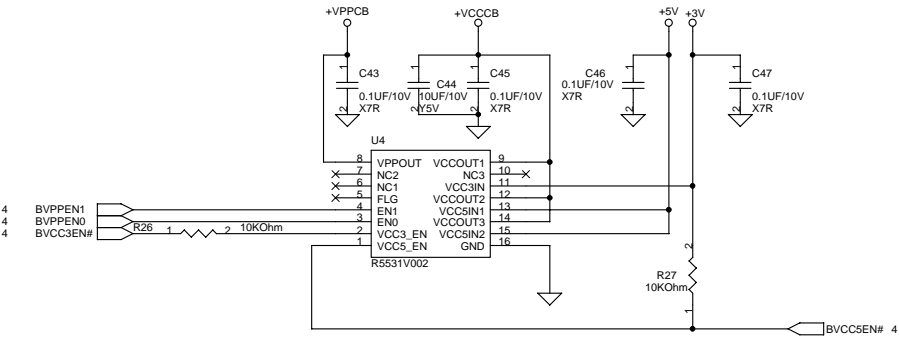
[1] NOT INSTALLED
 [2] AS CLOSE AS POSSIBLE TO DEVICE TERMINALS.



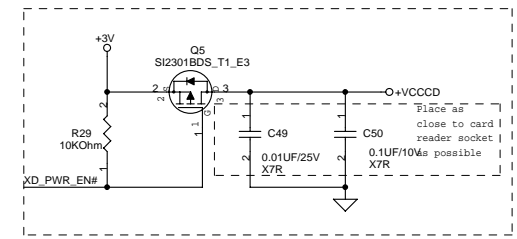
R5C841-CSP208Q



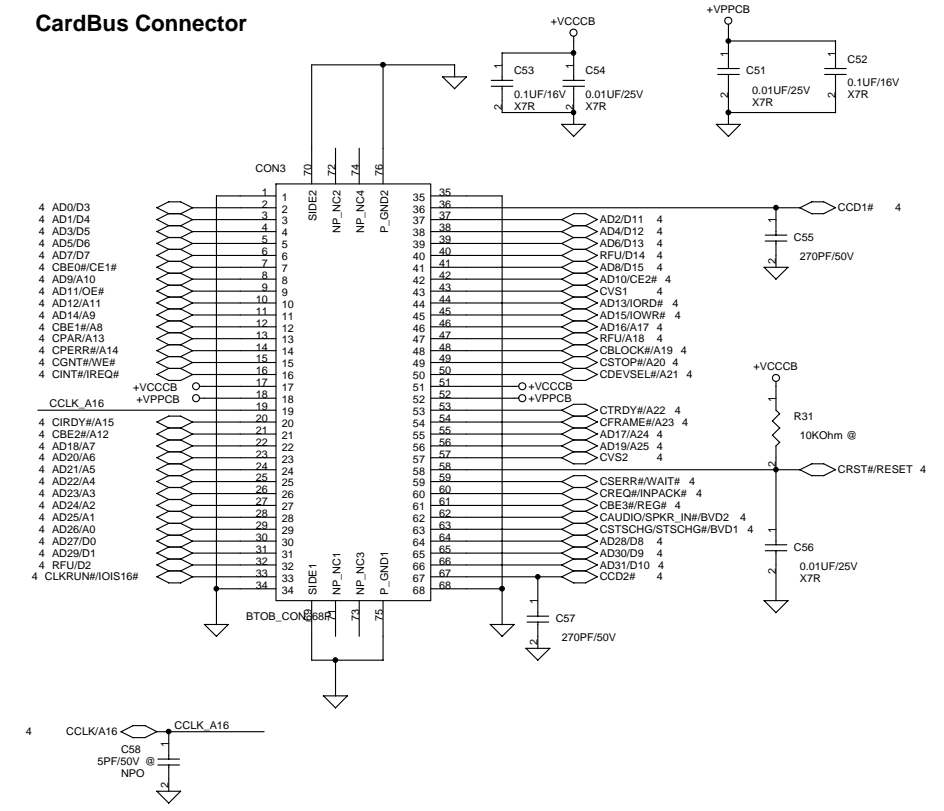
Power Switch



To correct the problem when MS Duo adaptor is in use.

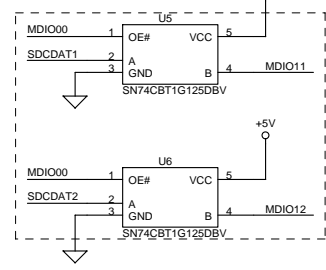


CardBus Connector

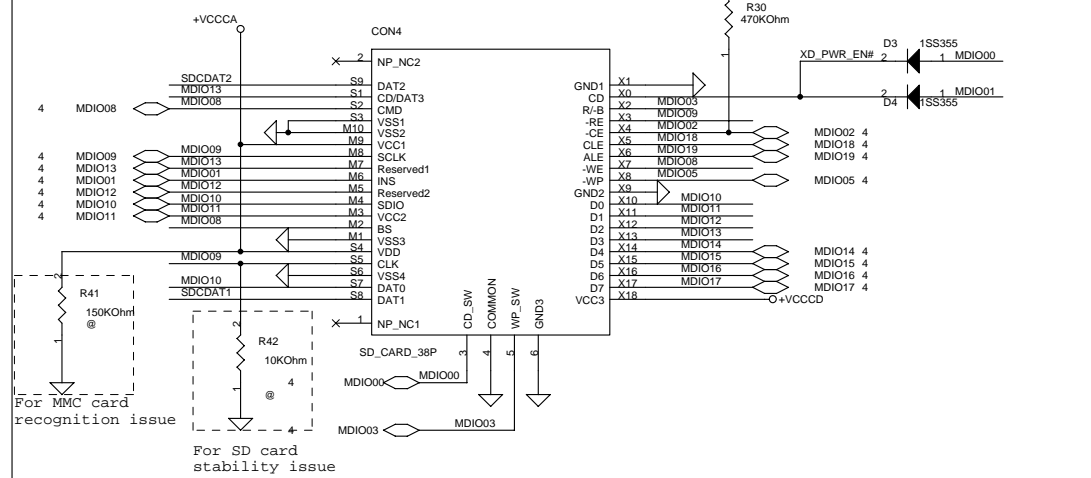


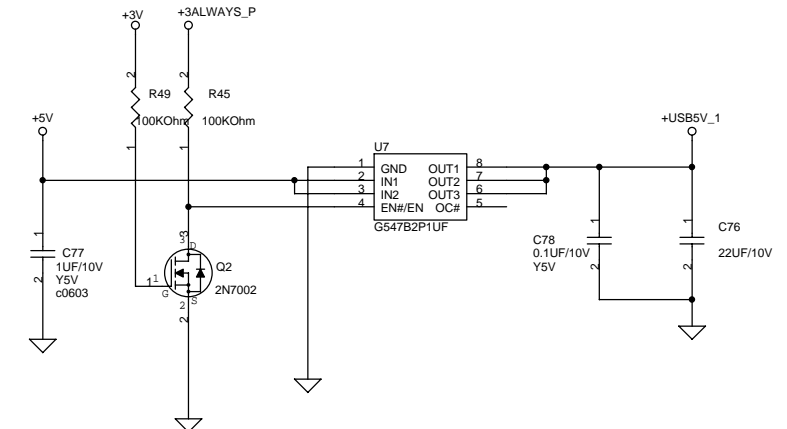
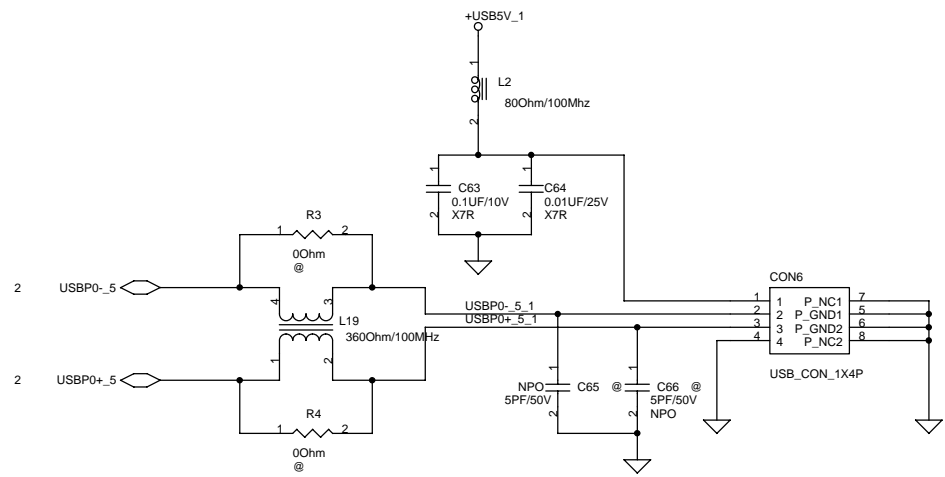
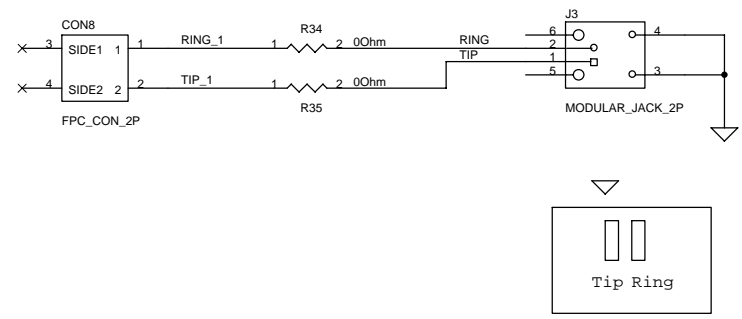
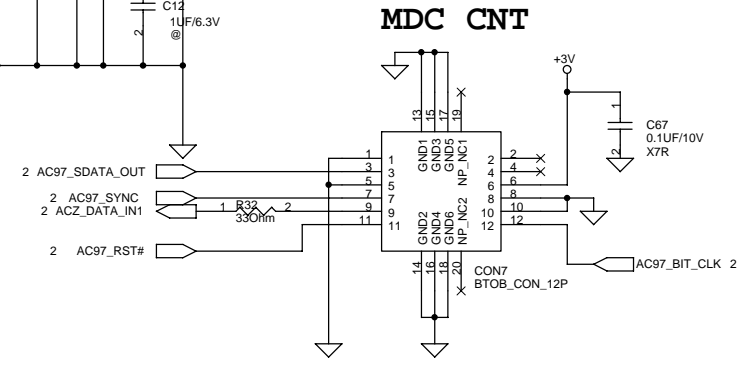
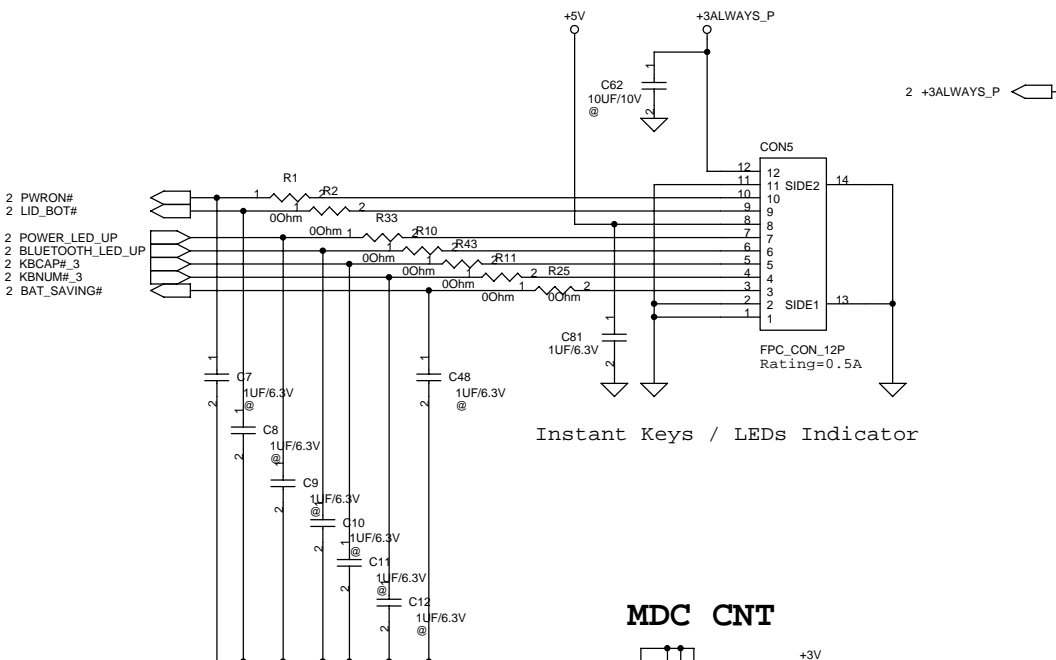
SD/MMC/MS/MS-PRO Card Reader Socket

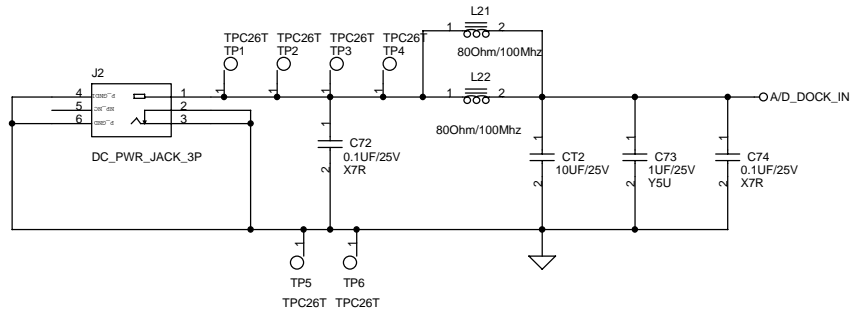
To correct the problem when MS Duo adaptor is in use.



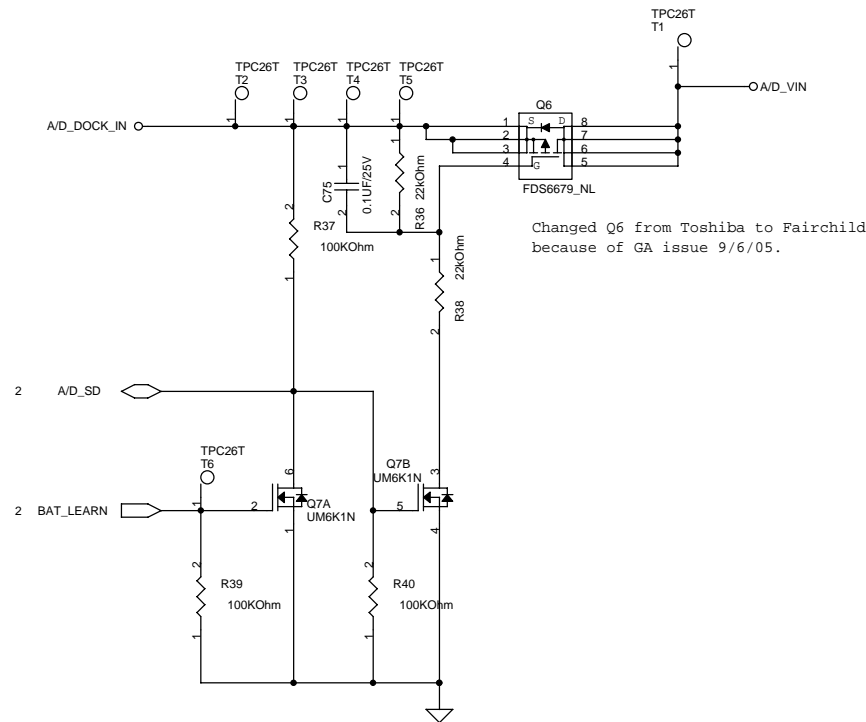
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MDIO01	-->	MS Card Detect
MDIO02	-->	XD Card Enable
MDIO03	-->	SD Write Protect / XD Card Ready/Busy#
MDIO04	-->	SD/MS/XD Card Power0 Control
MDIO05	-->	XD Card Write Protect
MDIO06	-->	SD/MS/XD LED
MDIO07	-->	SD/MS External Clock
MDIO08	-->	SD Command/MS Bus State /XD Card Write Enable
MDIO09	-->	SD/MS Clock /XD Card Read Enable
MDIO10	-->	SD/MS/XD Data 0
MDIO11	-->	SD/MS/XD Data 1
MDIO12	-->	SD/MS/XD Data 2
MDIO13	-->	SD/MS/XD Data 3
MDIO14	-->	XD Data 4
MDIO15	-->	XD Data 5
MDIO16	-->	XD Data 6
MDIO17	-->	XD Data 7
MDIO18	-->	XD Card Command Latch
MDIO19	-->	XD Card Address Latch



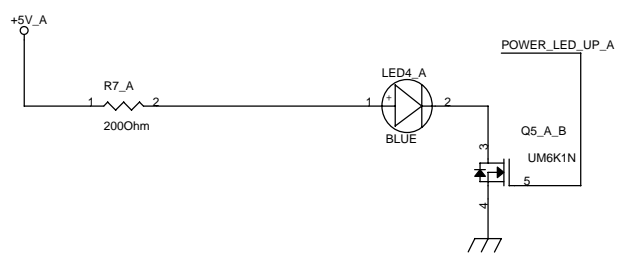
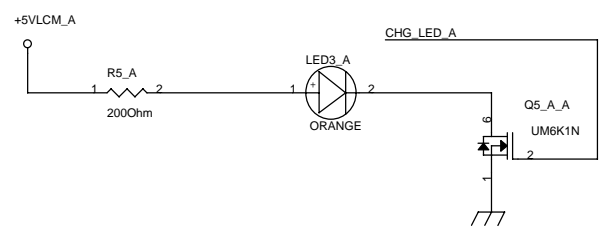
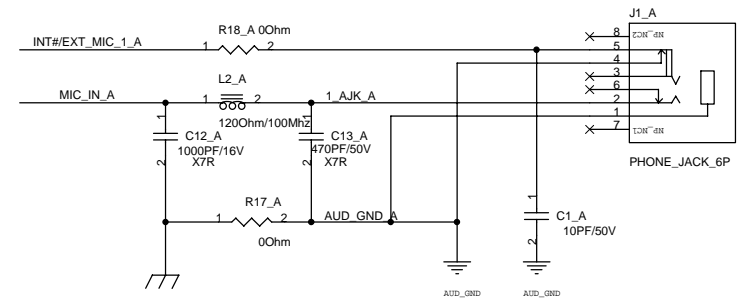
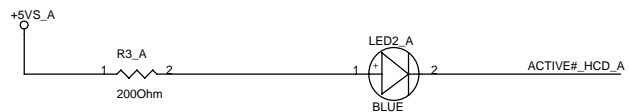
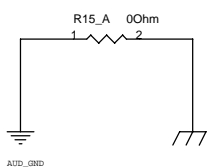
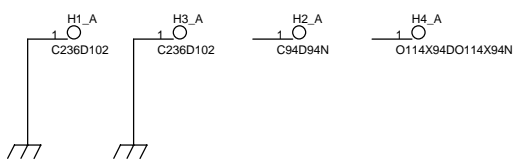
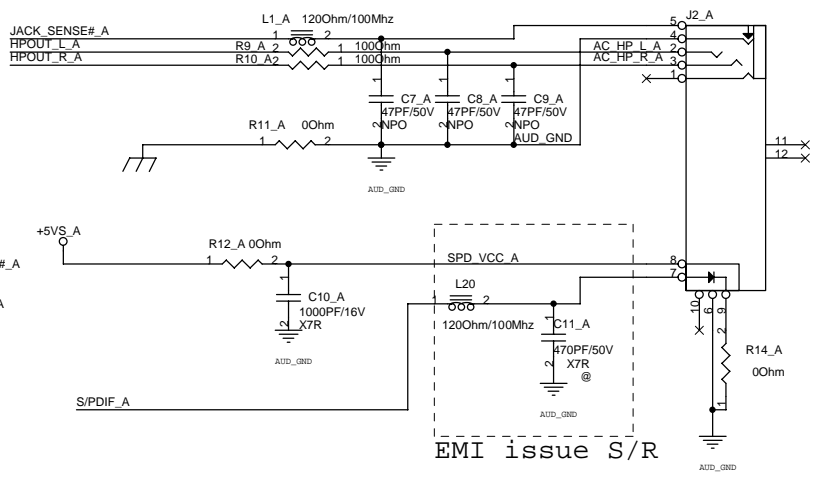
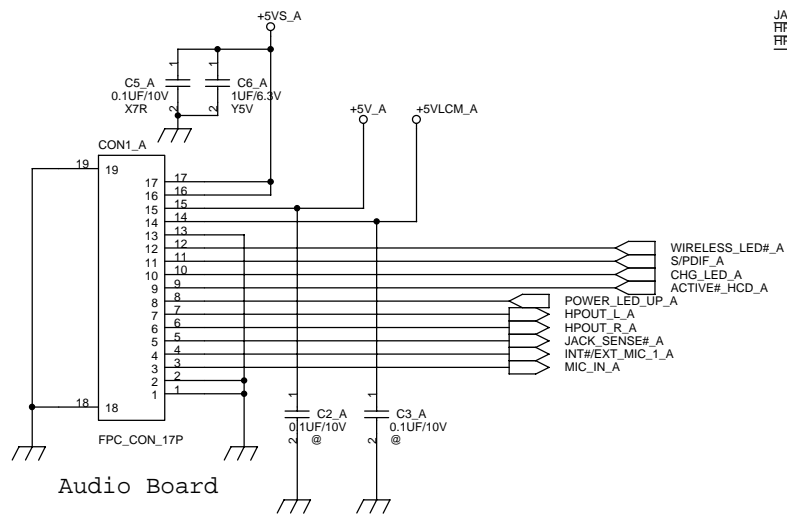
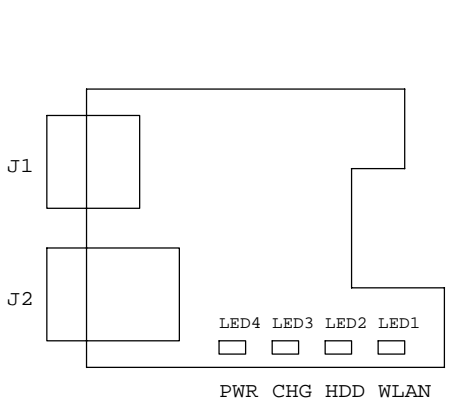




2 A/D_VIN ○ A/D_VIN
 2 A/D_DOCK_IN ○ A/D_DOCK_IN



Changed Q6 from Toshiba to Fairchild because of GA issue 9/6/05.



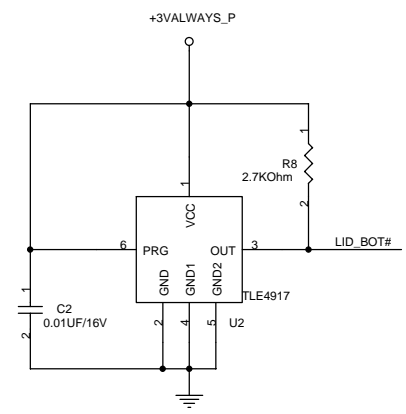
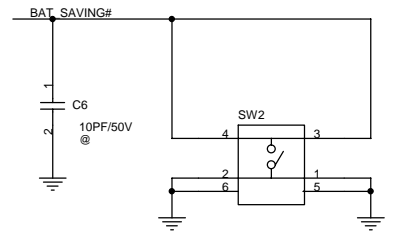
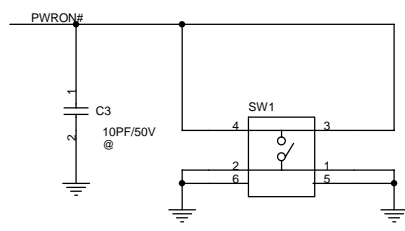
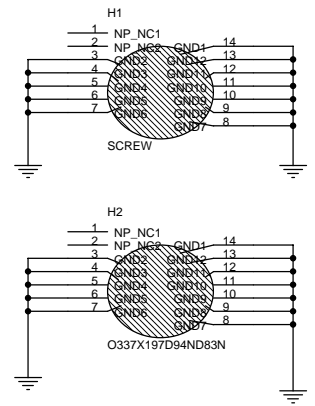
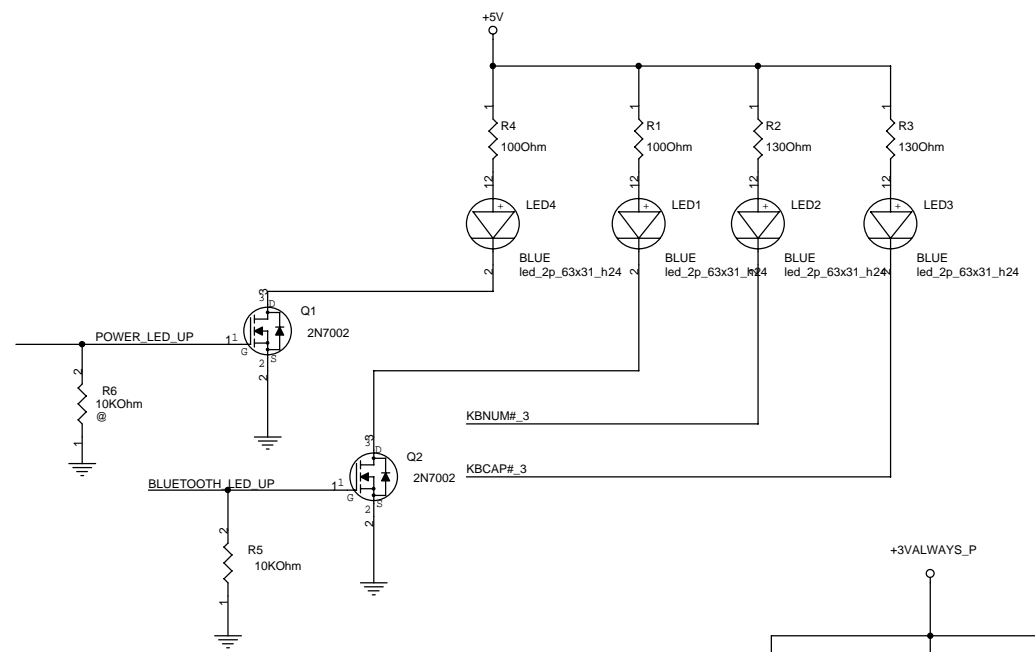
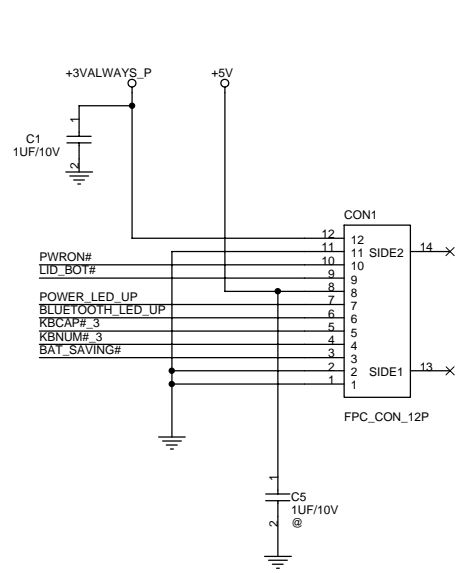
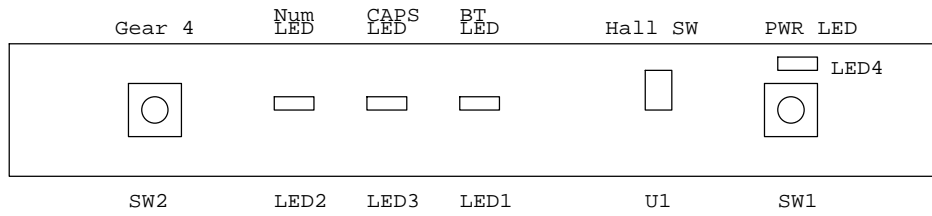
Revision History

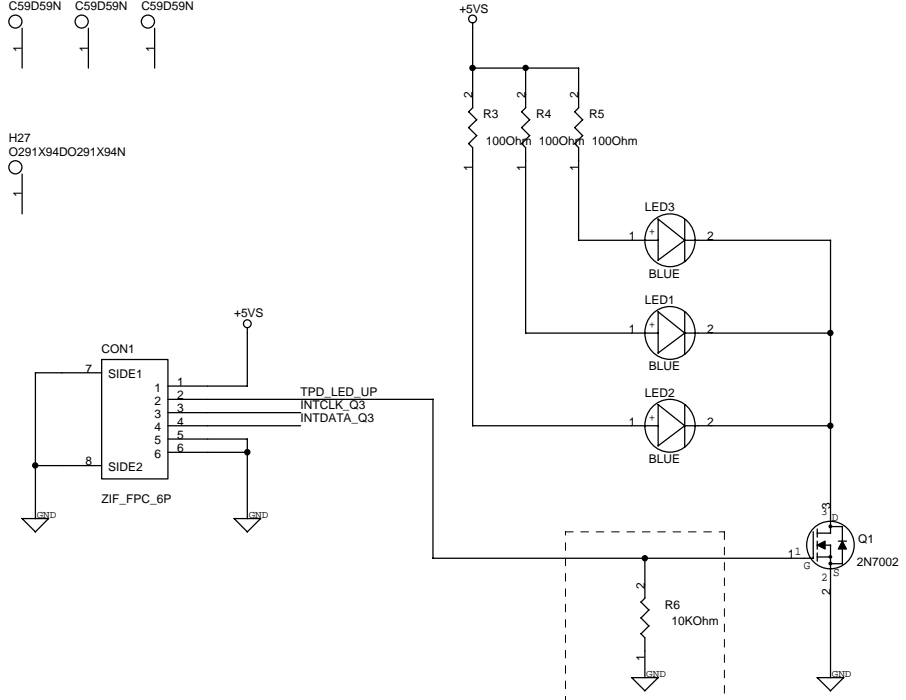
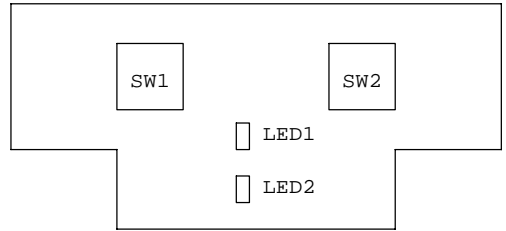
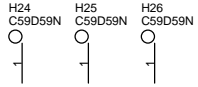
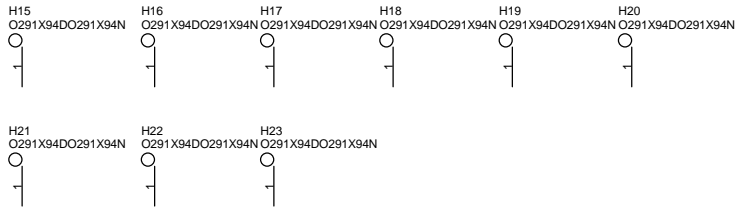
Rev1.2

1. Add on 3VS discharge circuit.
2. Add on EMI solution.
3. Replace X1, C33 and C36 for cost issue.
4. Add on USB Power isolation circuit for S4 state.

Rev2.0

1. U7.1 link to GND
2. Add on Pull low 10K for PowerOnLED and BT LED in Indicator Board.





R2.0 Modify

