Compal Confidential

NIMUA/UB

Schematics Document

Arrandale

with Intel IBEX PEAK-M core logic

REV:0.3

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

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Title: **Cover Sheet**

Size	Document Number	Rev
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File Name :

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14.1W_PCB_LA5941P

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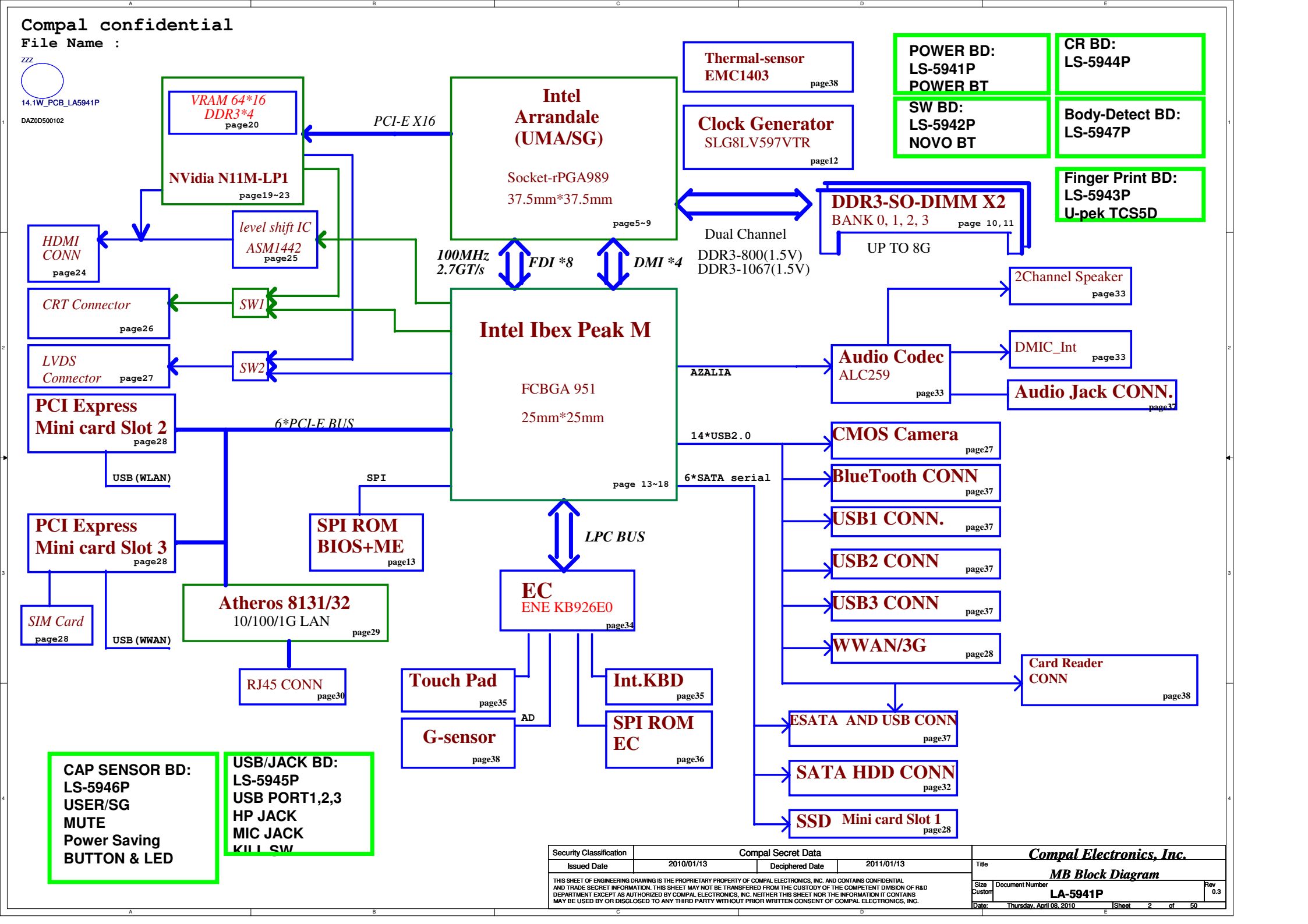

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Title: MB Block Diagram

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DDR3 Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +1.8VS +0.75VS +1.05VS For SG +3VS_DELAY +1.8VS_VGA +1.5VS_VGA
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

SMBUS Control Table

	SOURCE	RAM M2	BATT	KB926	SODIMM	CLK CHIP	WLAN WWAN	N11x Thermal Sensor	EMC1403	Cap sensor board	ALS	PCH
SMB_EC_CK1 SMB_EC_DA1	KB926 +3VALW	X	V +3VALW	X	X	X	X	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926 +3VALW	X	X	V +3VALW	X	X	X	V +3VS	V +3VS	X	V +3VS	V +3VALW
SMBCLK SMBDATA	PCH +3VALW	V +3VALW	X	X	V +3VS	V +3VS	X	X	X	X	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	X	X	V	X	X	X	X	X	X	X	X

PCH, I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0

EC, I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS	
PCH	96/98,R/W	1 0 0 1 0 1 1 X	1 0 0 1 1 0 0 X
EMC1403 Thermal sensor	9A	1 0 0 1 1 0 1 X	
N-vidia Thermal sensor	9E	1 0 0 1 1 1 1 X	
ALS	70/72,R/W	0 1 1 1 0 0 0 X	0 1 1 1 0 0 1 X

@ FUNCTION

	PVT	NON-USE
45@	(45 BOM)	
100@	10/100 LAN	
GIGA@	GIGA LAN	
UMA_HDMI@	FOR UMA HDMI components	
~~HDMI@~~	~~FOR HDMI components~~	
3G@	3G(WWAN) function	
X76@	(X76 BOM)	
~~ESATA@~~	~~ESATA function~~	
CMOS@	Camera function	
SSD@	SSD w/ miniPCIE socket	
~~10M@~~	~~FOR 10M CHIP~~	
~~11M@~~	~~FOR 11M CHIP~~	
UMA@	UMA only (Arranddale)	
~~DIS@~~	~~DIS only (Arranddale)~~	
~~VGA@~~	~~FOR NVIDIA PART~~	
HYBRID@	FOR SWITCHABLE	
HU@	SWITCHABLE or UMA only	
HD@	SWITCHABLE or DIS only	

SKU

Arrandale(dGPU) ~~DIS only~~	~~DIS@ / 100@ for EVT~~
Arrandale(iGPU) UMA only	~~UMA@ / 100@ for EVT~~
Arrandale(iGPU+dGPU) SWITCHABLE	HYBRID@

PCIE PORT LIST

PORT	DEVICE
1	~~NEW CARD~~
2	WLAN
3	LAN
4	3G
5	
6	
7	
8	

SATA PORT LIST

PORT	DEVICE
0	HDD
1	SSD
2,3	HM55 disabled
4	E-SATA
5	

USB PORT LIST

PORT	DEVICE
0	USB 1
1	USB/ESATA
2	CMOS
3	USB 2
4	
5	CARD READER
6	X HM55 disabled
7	X HM55 disabled
8	WIRELESS
9	USB 3
10	FigerPrinter
11	BT
12	
13	3G

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Title: MB Notes List

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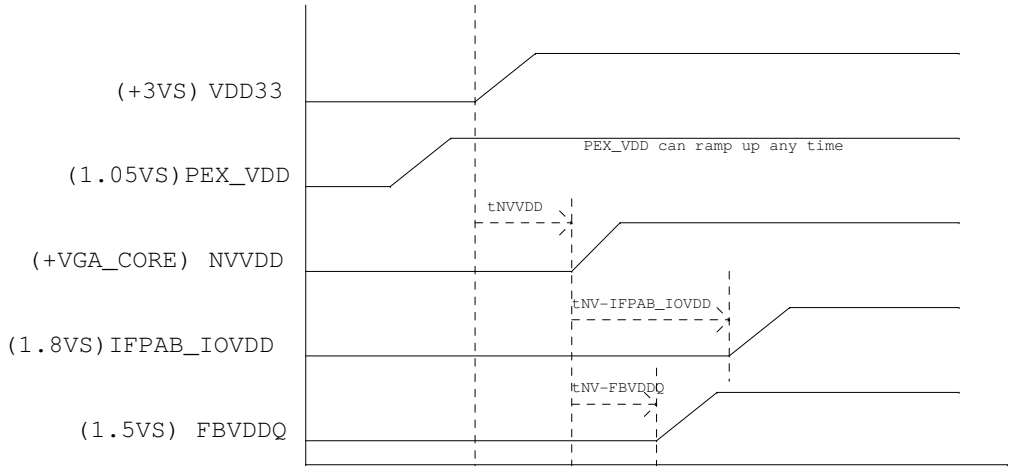
VGA and DDR3 Voltage Rails (N11M GPIO)

GPIO	I/O	ACTIVE	Function Description
GPIO0	N/A	N/A	
GPIO1	IN	-	HDMI_DETECT_VGA
GPIO2	OUT	H	NV_INVTPWM
GPIO3	OUT	H	VGA_ENVDD_R
GPIO4	OUT	H	VGA_ENABLT
GPIO5	OUT	-	GPU VID0
GPIO6	OUT	-	GPU VID1
GPIO7	OUT	-	
GPIO8	I/O	L	
GPIO9	OUT	L	
GPIO10	OUT		
GPIO11	I/O	L	
GPIO12	IN	-	
GPIO13	OUT	-	
GPIO14	OUT	-	
GPIO15	IN	-	
GPIO16	OUT	-	
GPIO17	IN	-	
GPIO18	IN	-	
GPIO19	IN	-	
GPIO20	IN	-	
GPIO21	IN	-	
GPIO22	IN	-	
GPIO23	I/O		

Power Sequence

The ramp time for any rail must be more than 40us



	Device ID
N11M-LP1 (40nm)	0x0A6E

GPIO5 GPIO6

GPU_VID0	GPU_VID1	VGA_CORE	P-State
0	0	0.8V	Deep P12
0	1	0.85V	P8
1	1	0.86V	P0

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Title: VGA Notes List

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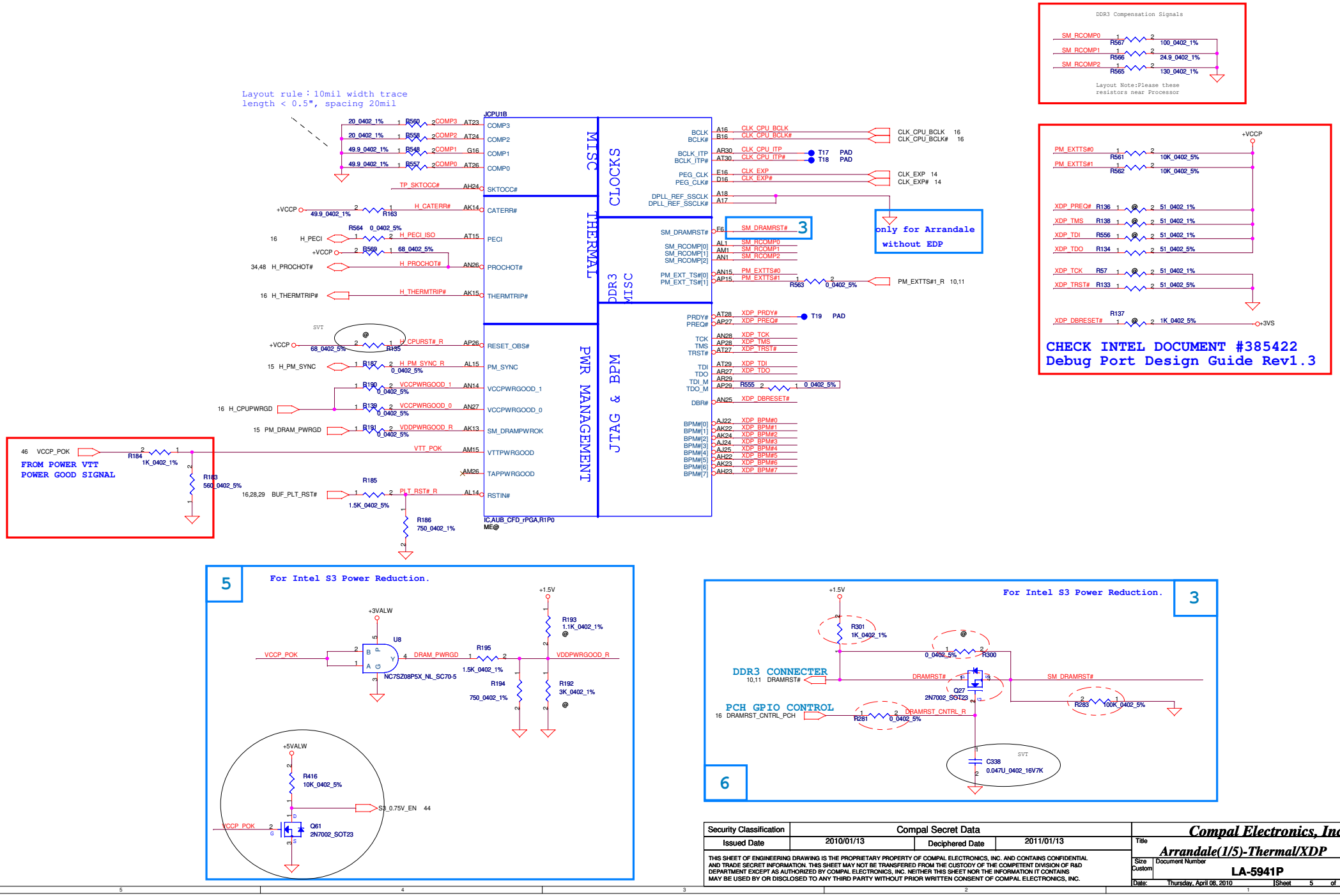

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Title: Arrandale(1/5)-Thermal/XDP

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Layout rule : trace length < 0.5"

JCPU1A

DMI

PCI EXPRESS -- GRAPHICS

Intel(R) FDI

IC,AUB_CFD_rPGA,R1P0
ME@

PCIE Lane Numbers Reversed

CFG3-PCI Express Static Lane Reversal

HYBRID@

FOR ES1 SAMPLE ONLY

JCPU1E

RESERVED

IC,AUB_CFD_rPGA,R1P0
ME@

CFG Straps for PROCESSOR

CFG0 — R58 3.01K_0402_1%

PCI-Express Configuration Select	
CFG0	1: Single PEG 0: Bifurcation enabled

Not applicable for Clarksfield Processor

CFG[1:0] 11=1*16 PEG
10=2*8 PEG

CFG3 — R61 3.01K_0402_1%

CFG3-PCI Express Static Lane Reversal	
CFG3	1: Normal Operation 0: Lane Numbers Reversed 15 -> 0, 14 ->1, ...

CFG4 — R60 3.01K_0402_1%

CFG4-Display Port Presence	
CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port

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Title: Arrandale(2/5)-DMI/PEG/FDI

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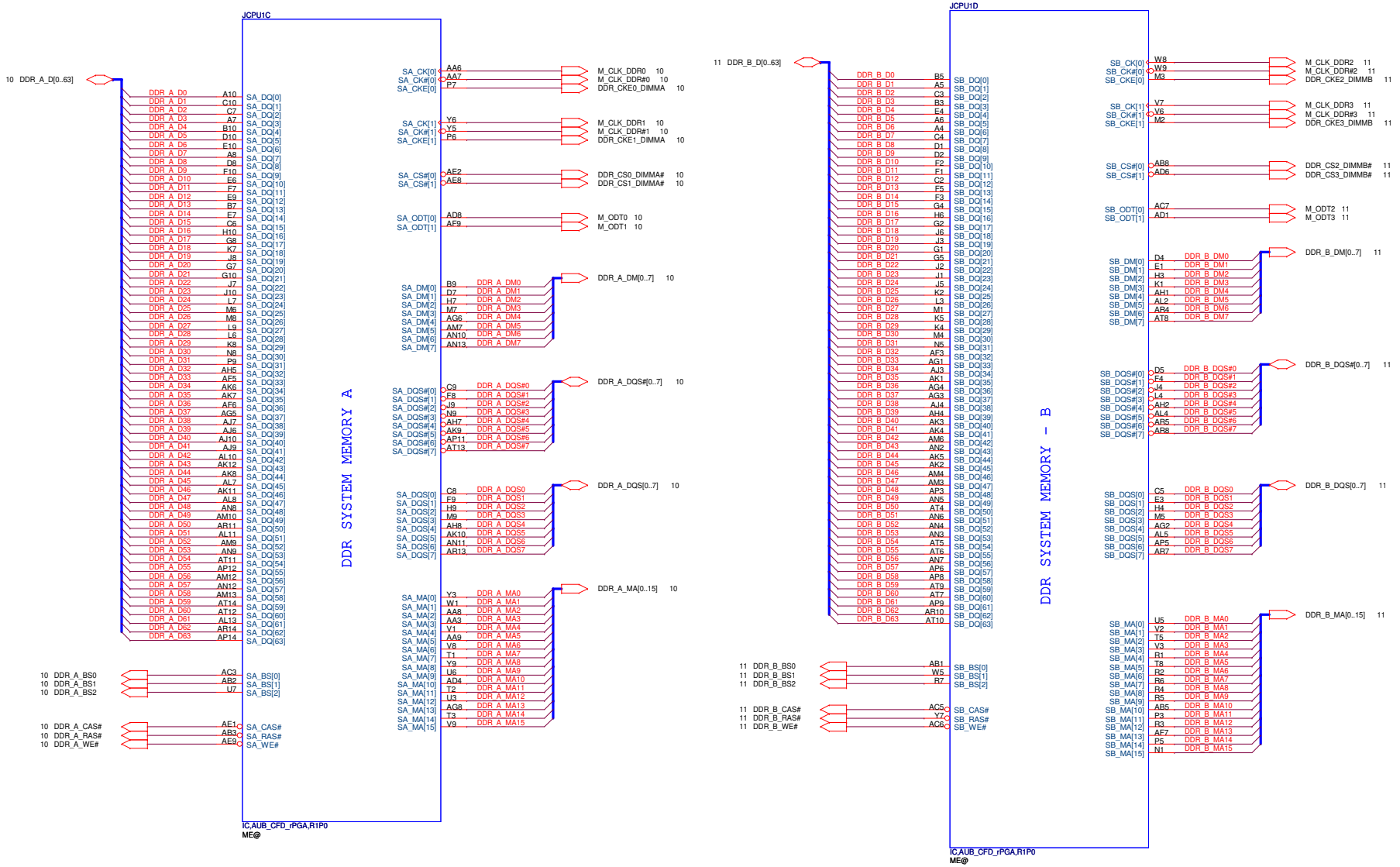

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Title: *Arrandale(3/5)-DDR III*

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AS NO CONNECT
BUT A SMALL AMOUNT OF POWER
(~15MW) MAYBE WASTED
DESIGN GUIDE REV1.1

Lenovo Request

For Intel S3 Power Reduction.

For Intel S3 Power Reduction.

H_VTTVID1 = Low, 1.1V FOR Clarksfiel
H_VTTVID1 = High, 1.05V FOR Auburndale

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Title: Arrandale(4/5)-PWR

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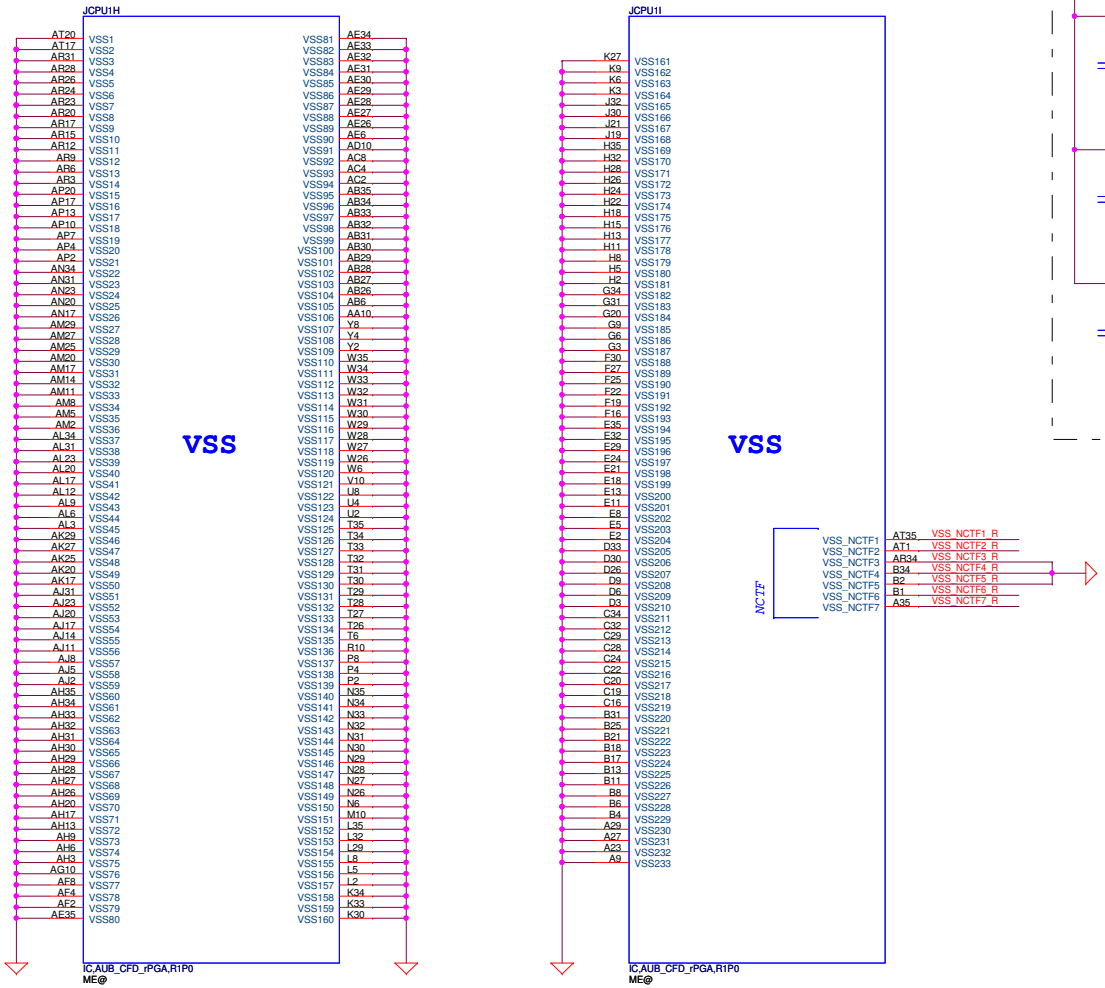

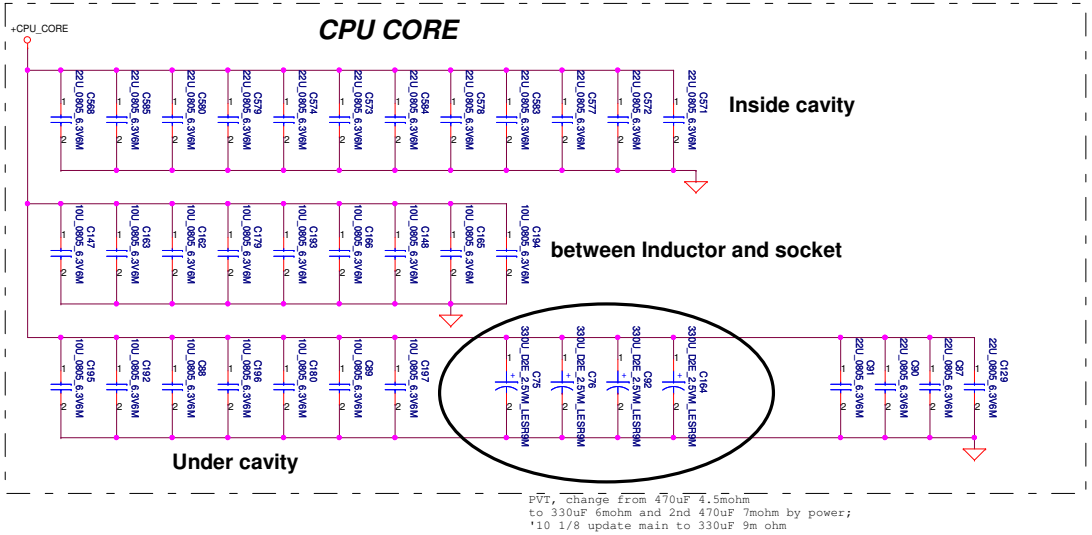

PVT, change from 470uF 4.5mohm
to 330uF 6mohm and 2nd 470uF 7mohm by power;
'10 1/8 update main to 330uF 9m ohm

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Title: *Arrandale(5/5)-GND/Bypass*

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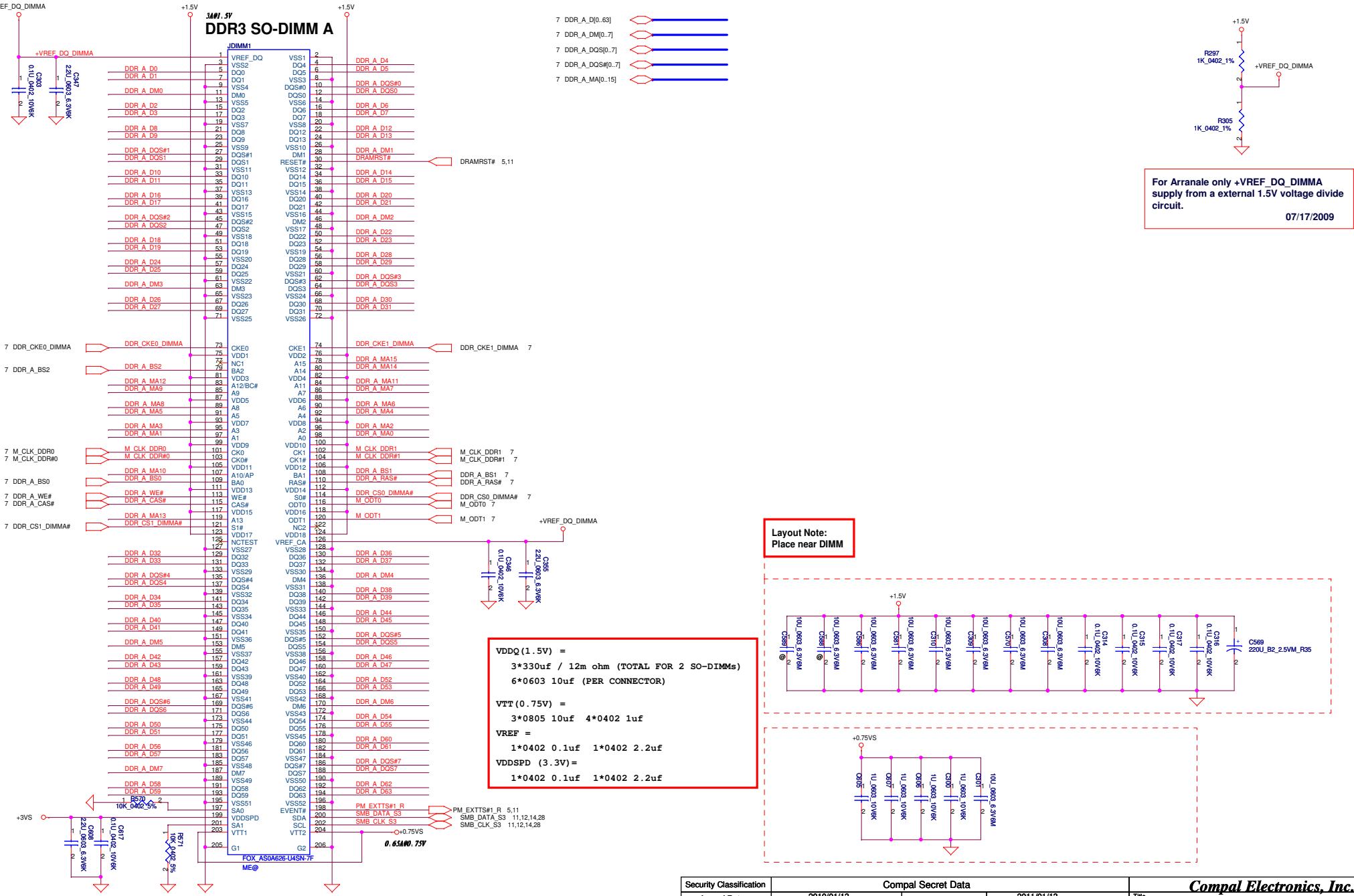
DDR3 SO-DIMM A



7 DDR_A_D[0..63]
7 DDR_A_DM[0..7]
7 DDR_A_DQS[0..7]
7 DDR_A_DQS#[0..7]
7 DDR_A_MA[0..15]

For Arranale only +VREF_DQ_DIMMA supply from a external 1.5V voltage divide circuit.

07/17/2009

Layout Note: Place near DIMM


```
VDDQ(1.5V) =
   3*330uf / 12m ohm (TOTAL FOR 2 SO-DIMMs)
   6*0603 10uf (PER CONNECTOR)

VTT(0.75V) =
   3*0805 10uf  4*0402 1uf
VREF =
   1*0402 0.1uf  1*0402 2.2uf
VDDSPD (3.3V)=
   1*0402 0.1uf  1*0402 2.2uf
```

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Title: **DDRIII-SODIMM SLOT1**

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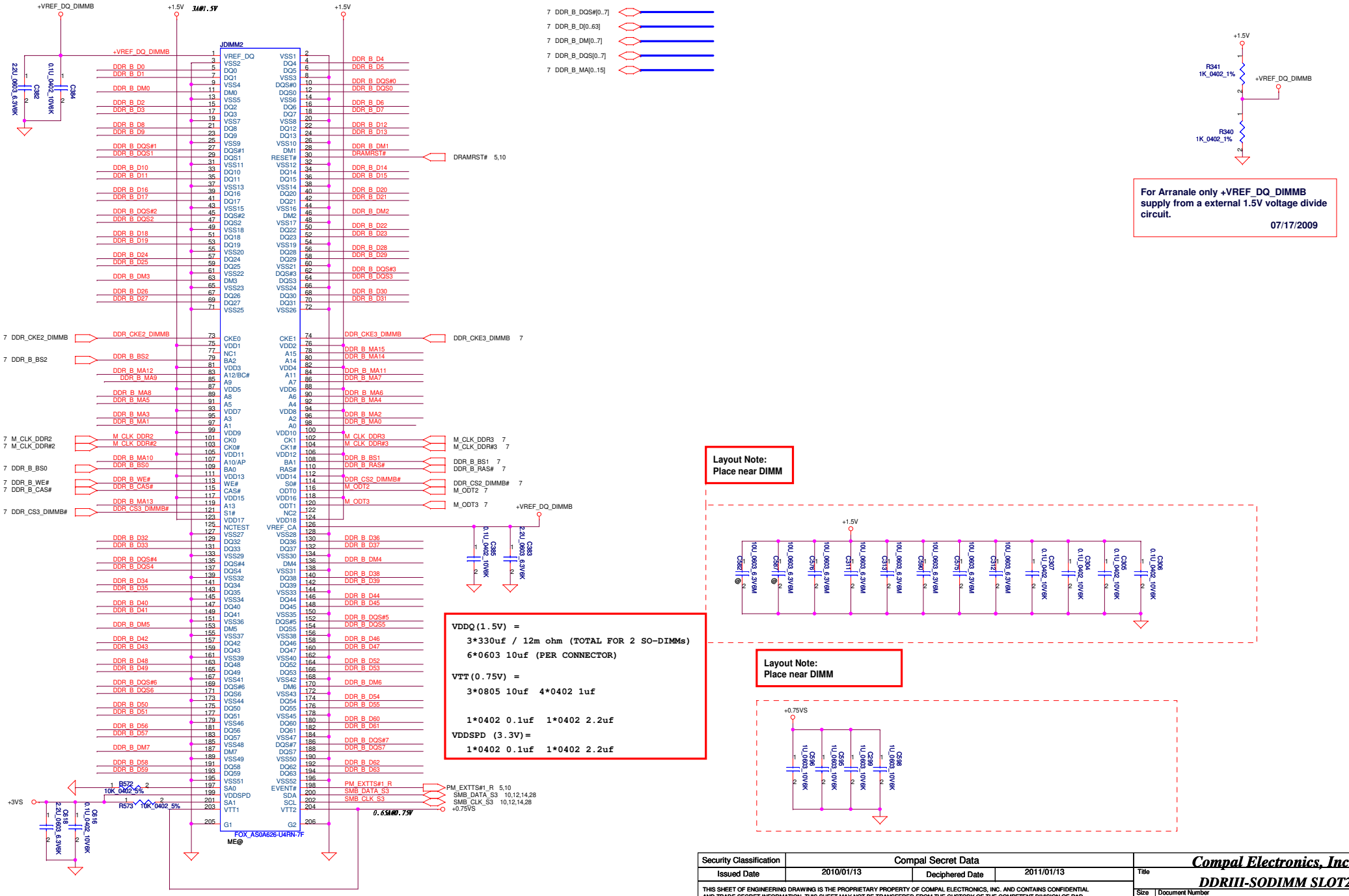

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Title: DDRIII-SODIMM SLOT2

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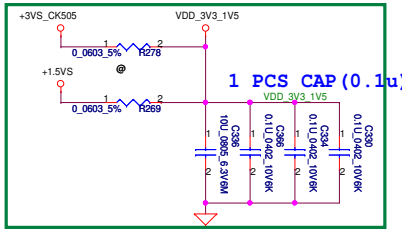
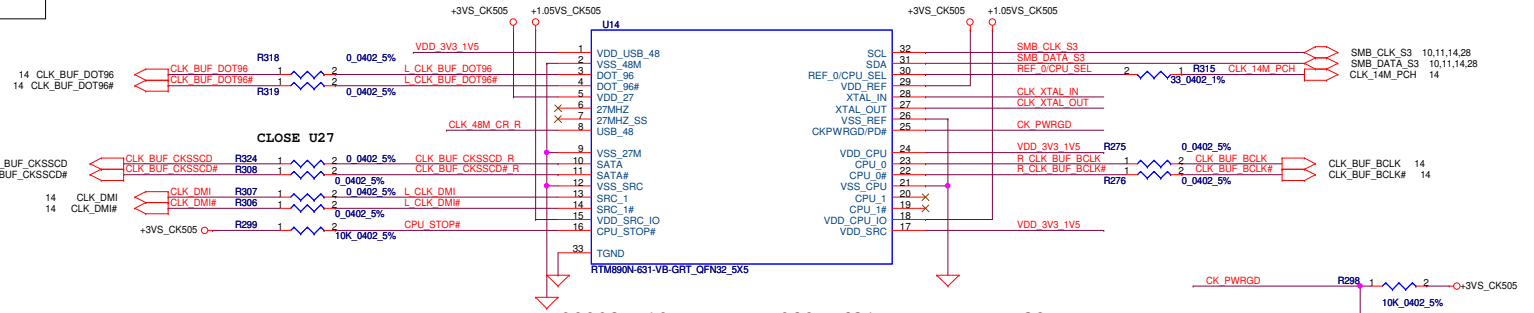
Reserve for Low Power CLK GEN.
RTM890N-632
SLG8LV597VTR



1 PCS CAP(0.1u) BY 1 INPUT PIN

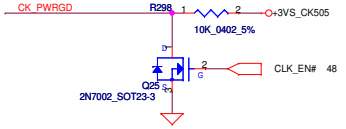
CLK GEN TO PCH
1. CLK_DMI
2. CLK_BUF_BCLK
3. CLK_BUF_CKSSCD
4. CLK_BUF_DOT96
5. CLK_14M_PCH

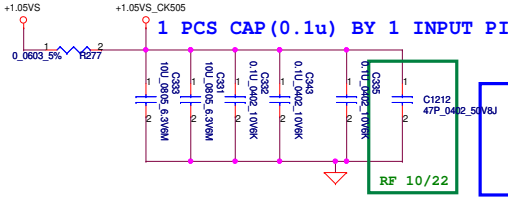
CLK GEN TO VGA
1. 27M_CLK
1. 27M_CLK_SS



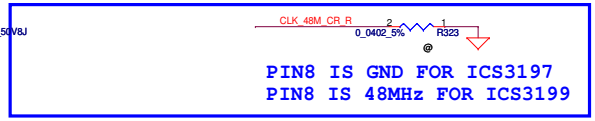
CLOSE U27

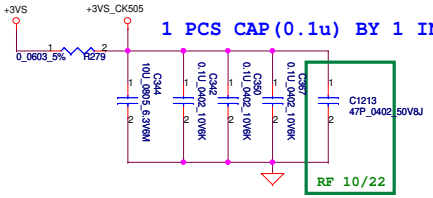
SA00003HQ10 S IC RTM890N-631-VB-GRT QFN 32P CLK GEN
(SA00003HR00)S IC ICS9LVS3199AKLFT MLF 32P CLK GEN
~~S IC SLG8SP587VTR QFN 32P CLK GEN (SA00002XY00)~~



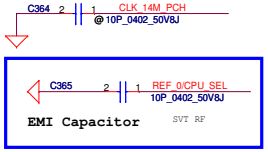


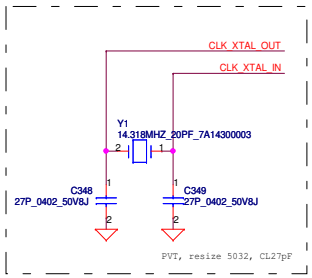
1 PCS CAP(0.1u) BY 1 INPUT PIN



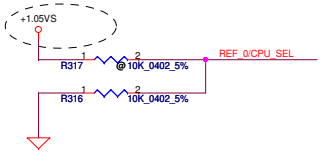


1 PCS CAP(0.1u) BY 1 INPUT PIN





PIN 30	CPU_0	CPU_1
0 (Default)	133MHz	133MHz
1	100MHz	100MHz



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Title: CLOCK GENERATOR

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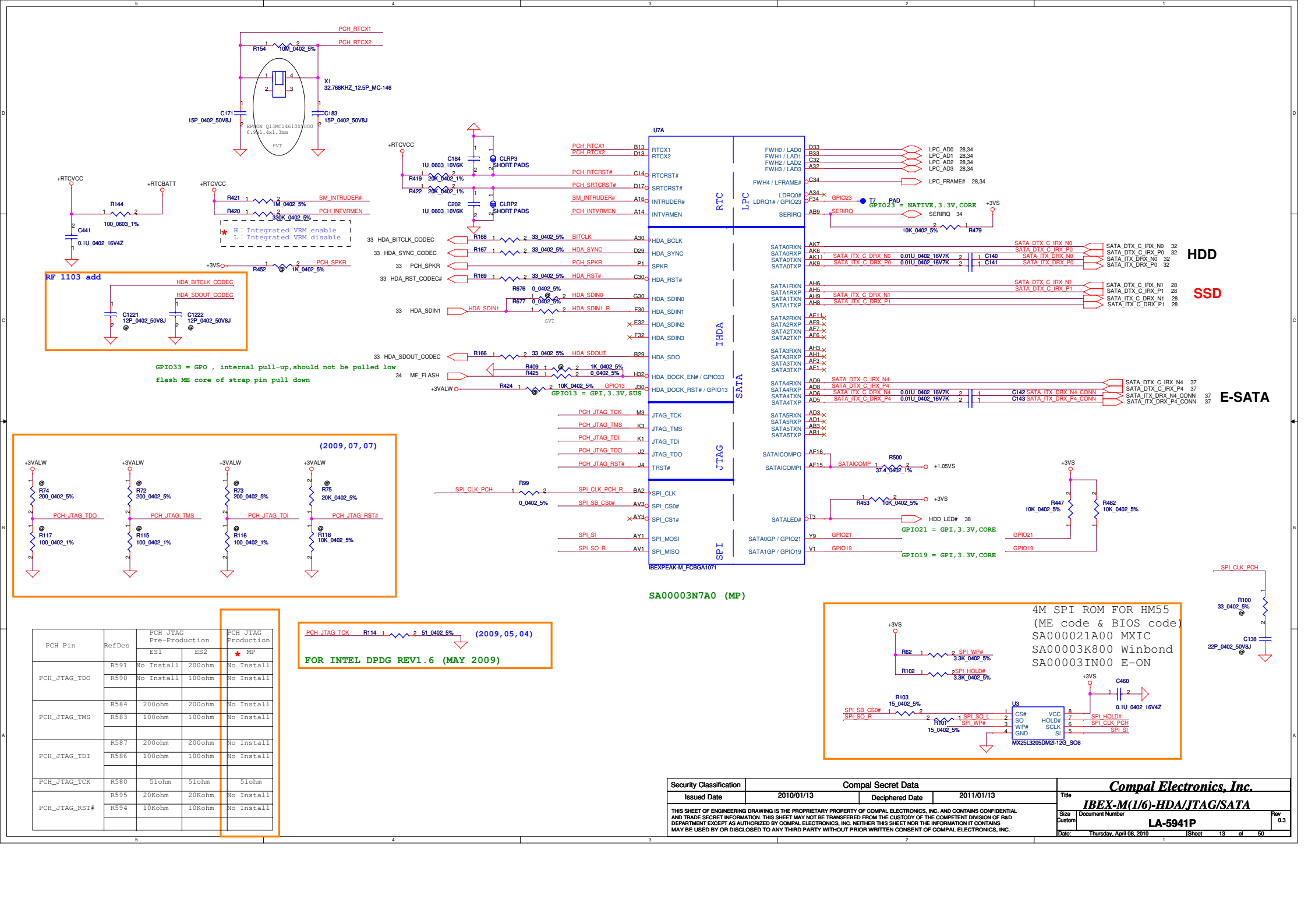

PCH Pin	RefDes	PCH JTAG Pre-Production ES1	PCH JTAG Pre-Production ES2	PCH JTAG Production * MP
PCH_JTAG_TDO	R591	No Install	200ohm	No Install
	R590	No Install	100ohm	No Install
PCH_JTAG_TMS	R584	200ohm	200ohm	No Install
	R583	100ohm	100ohm	No Install
PCH_JTAG_TDI	R587	200ohm	200ohm	No Install
	R586	100ohm	100ohm	No Install
PCH_JTAG_TCK	R580	51ohm	51ohm	51ohm
PCH_JTAG_RST#	R595	20Kohm	20Kohm	No Install
	R594	10Kohm	10Kohm	No Install

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Title: IBEX-M(1/6)-HDA/JTAG/SATA

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PCIE PORT LIST

PORT	DEVICE
1	~~NEW CARD~~
2	WLAN
3	LAN
4	3G
5	X
6	X
7	X
8	X

10/6 Remove Express card

10/6 Remove Express card CLK

U7B

IBEXPEAK-M_FCBGA1071

DDR3*2 AND CLK GEN

Nvidia Thermal sensor

EC_THERMAL

DTS , read from EC

EMI REQUEST 0303

For CR 48M CLK

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Title: IBEX-M(2/6)-PCI-E/SMBUS/CLK

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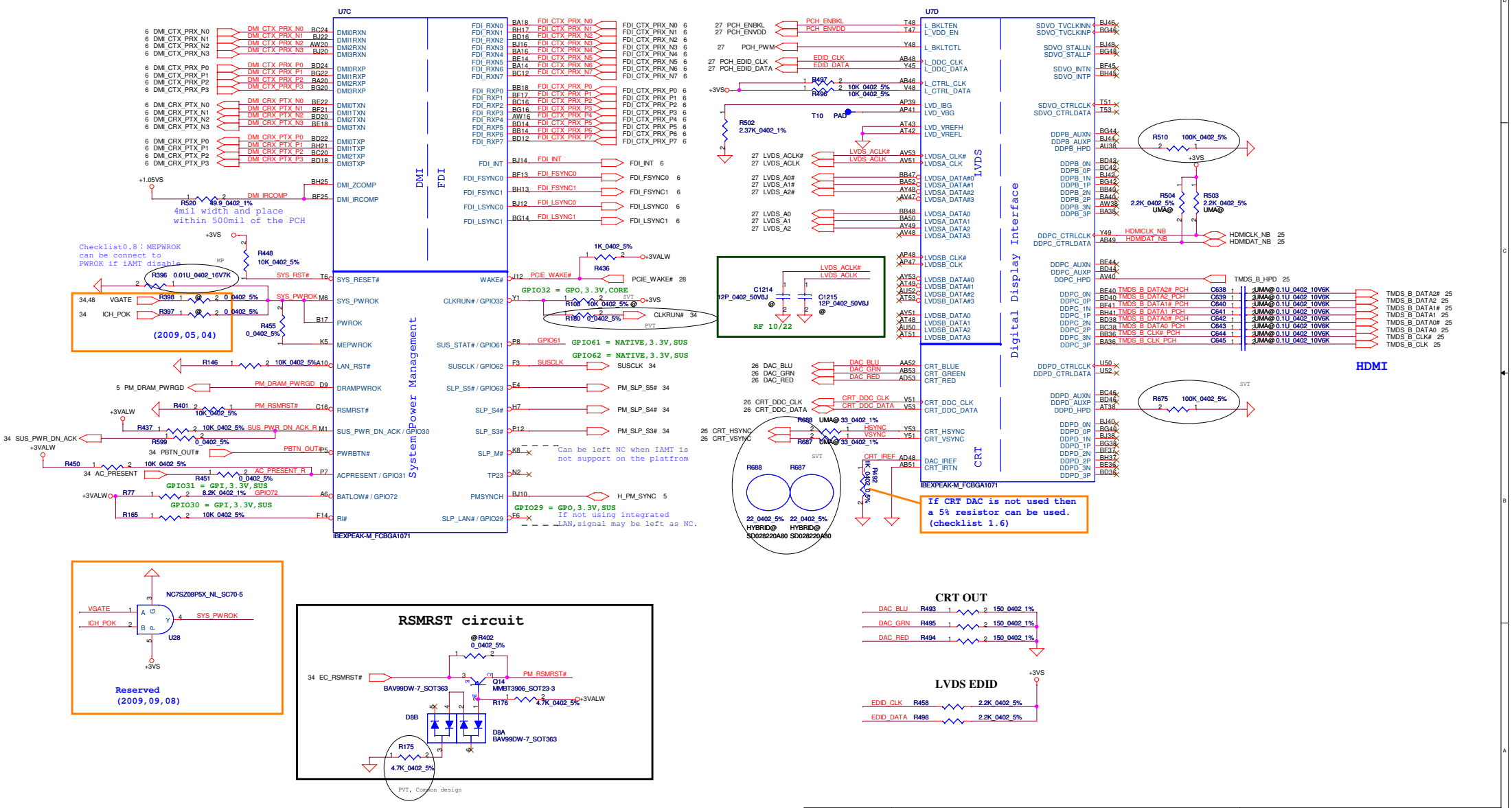

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Title	IBEX-M(3/6)-DMI/LVDS/DP/PM		
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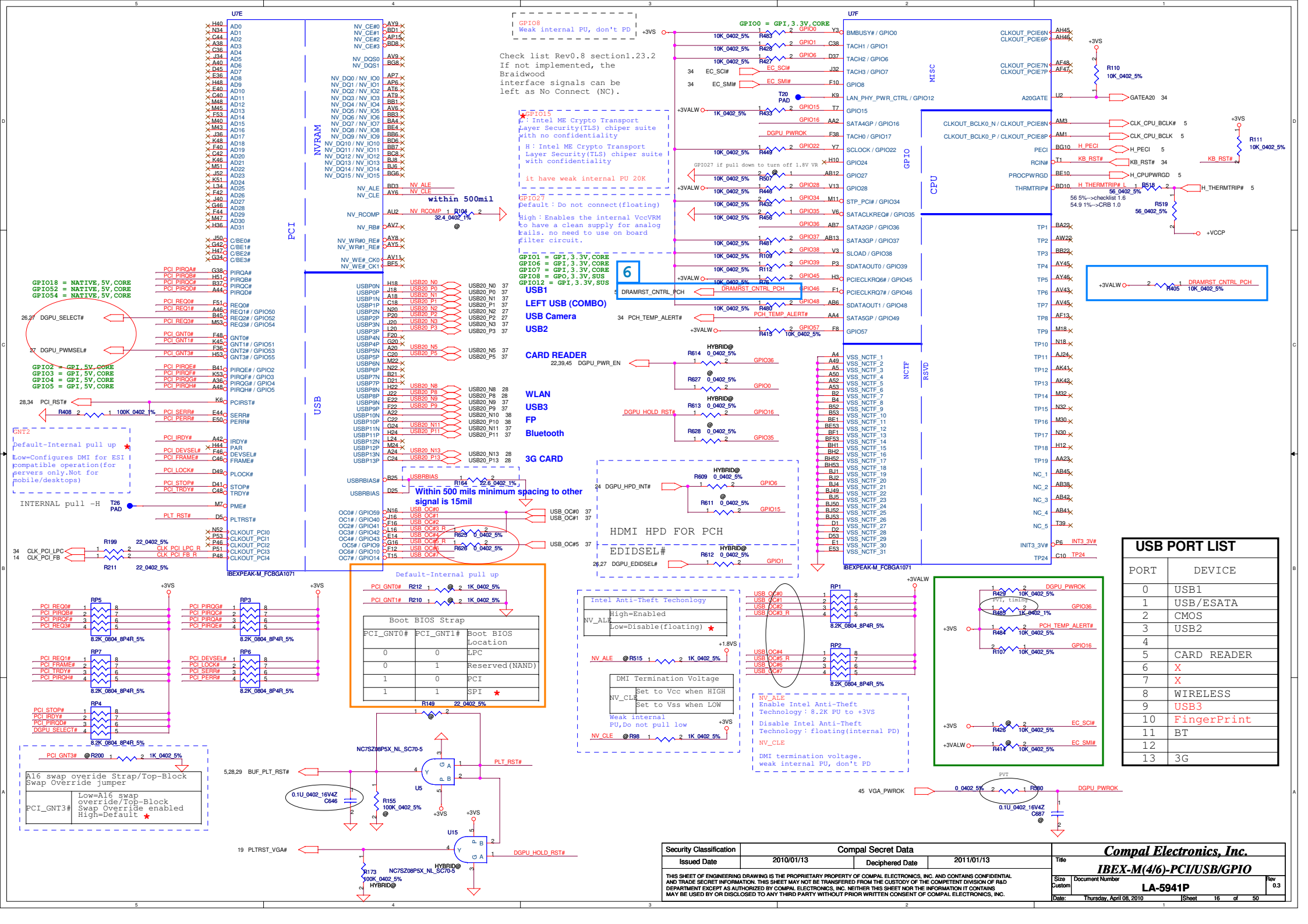

USB PORT LIST

PORT	DEVICE
0	USB1
1	USB/ESATA
2	CMOS
3	USB2
4	
5	CARD READER
6	X
7	X
8	WIRELESS
9	USB3
10	FingerPrint
11	BT
12	
13	3G

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Title: IBEX-M(4/6)-PCI/USB/GPIO

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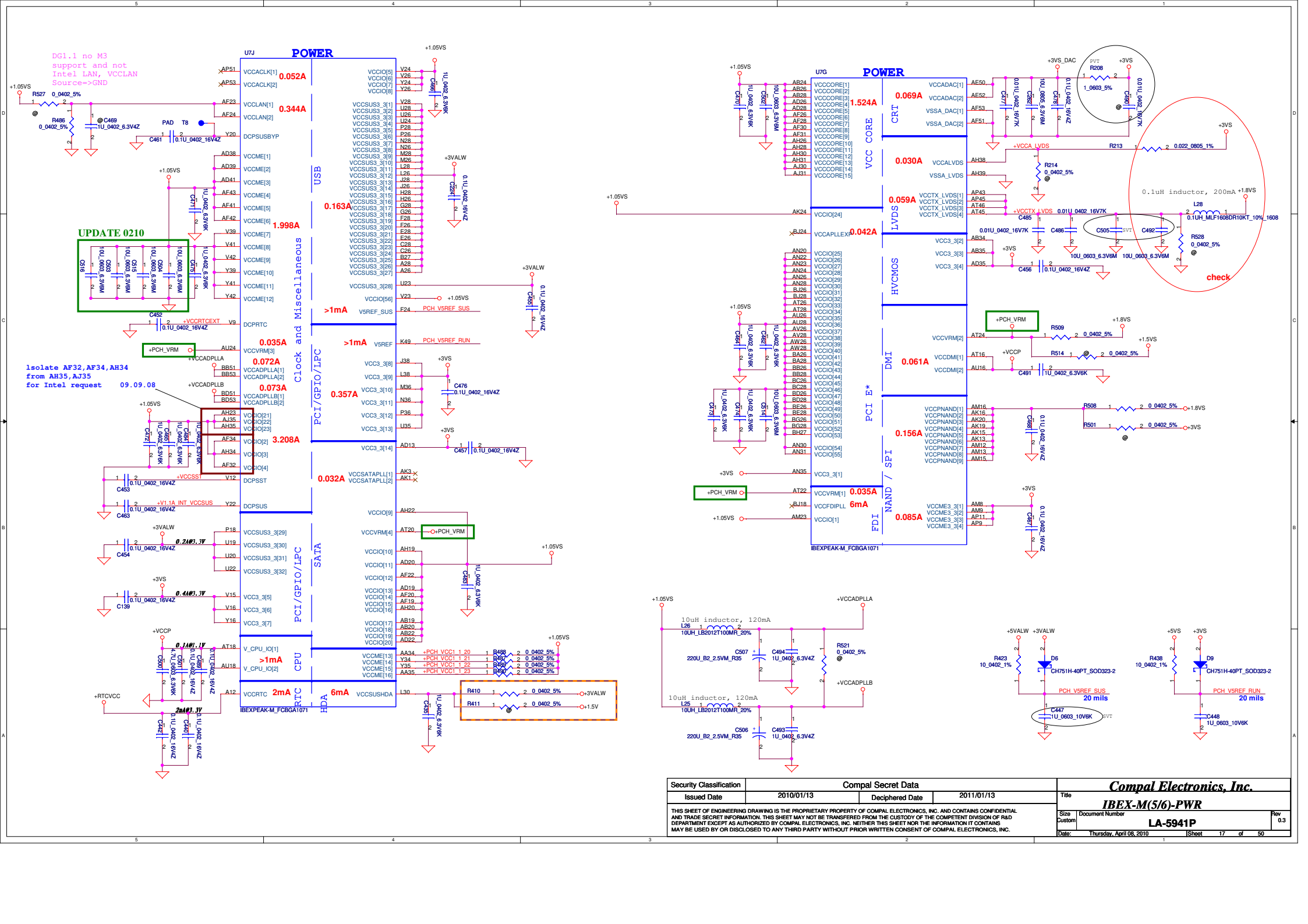
DG1.1 no M3 support and not Intel LAN, VCCLAN Source=>GND
POWER
U7J
UPDATE 0210
lsolate AF32,AF34,AH34 from AH35,AJ35 for Intel request 09.09.08
USB
Clock and Miscellaneous
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IBEXPEAK-M_FCBGA1071
POWER
U7G
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
IBEXPEAK-M_FCBGA1071
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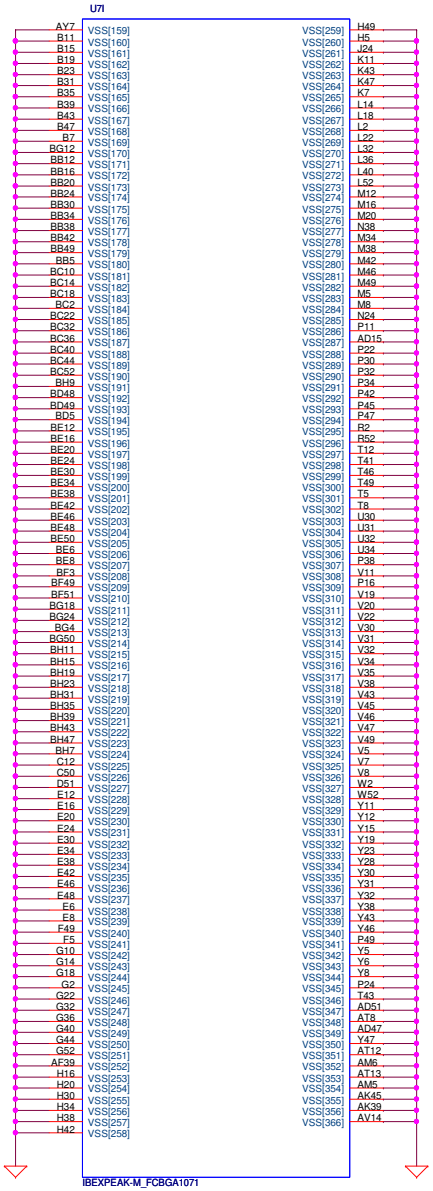

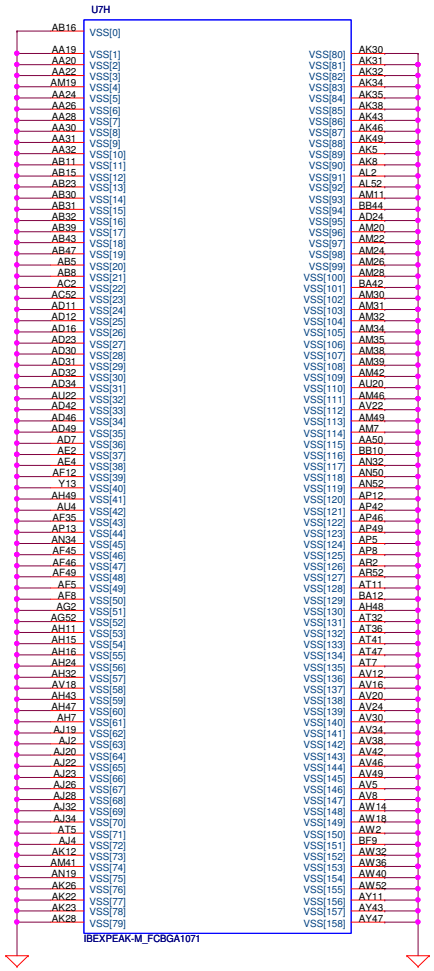

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Title: **IBEX-M(6/6)-GND**

Size	Document Number	Rev
Custom	LA-5941P	0.3

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	Device ID
N11M-GE1/LP1 (40nm)	0x0A7D

GPU_VID0	GPU_VID1	VGA_CORE	P-State
0	0	0.8V	Deep P12
0	1	0.85V	P8
1	1	0.9V	P0

GPIO5 GPIO6

CRT OUT

Removed external HDCP.
07/17/2009

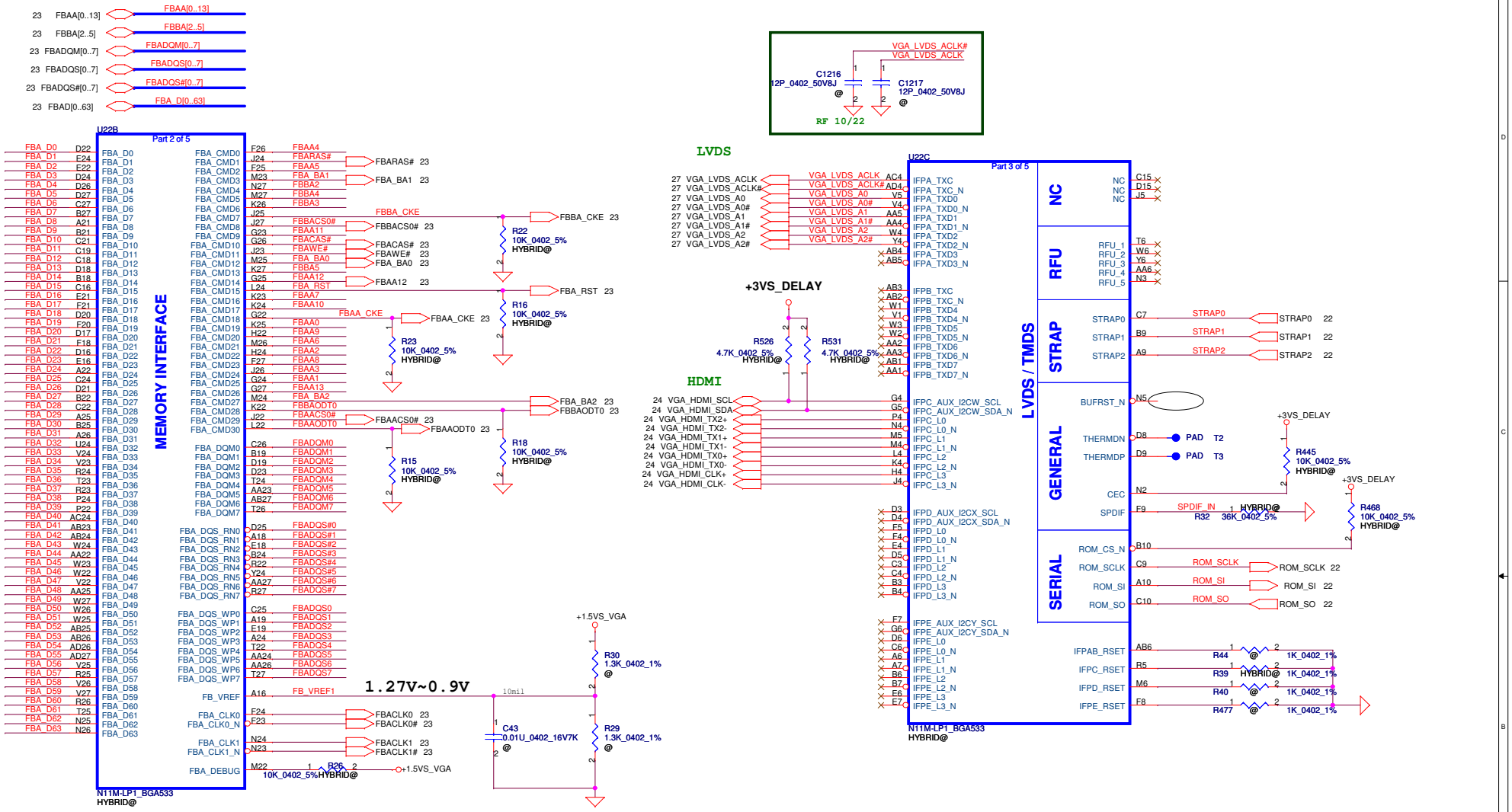
Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: N10M-GE1 PCIE,GPIO,CLK

Size	Document Number	Rev
B	LA-5941P	0.3

Date: Thursday, April 08, 2010 Sheet 19 of 50



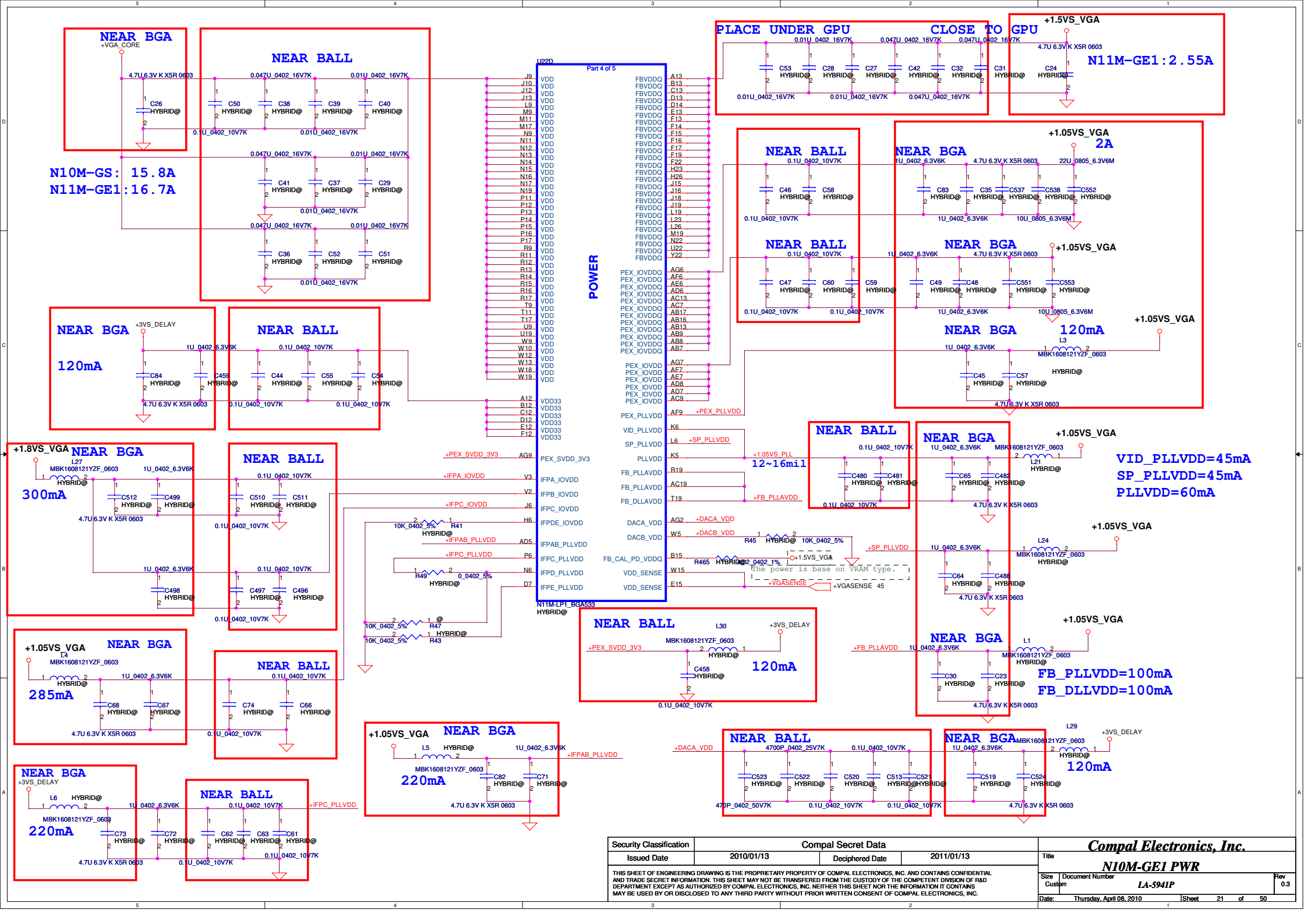
Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: N10M-GE1 LVDS,Memory Bus

Size	Document Number	Rev
B	LA-5941P	0.3

Date: Thursday, April 08, 2010 Sheet 20 of 50



Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

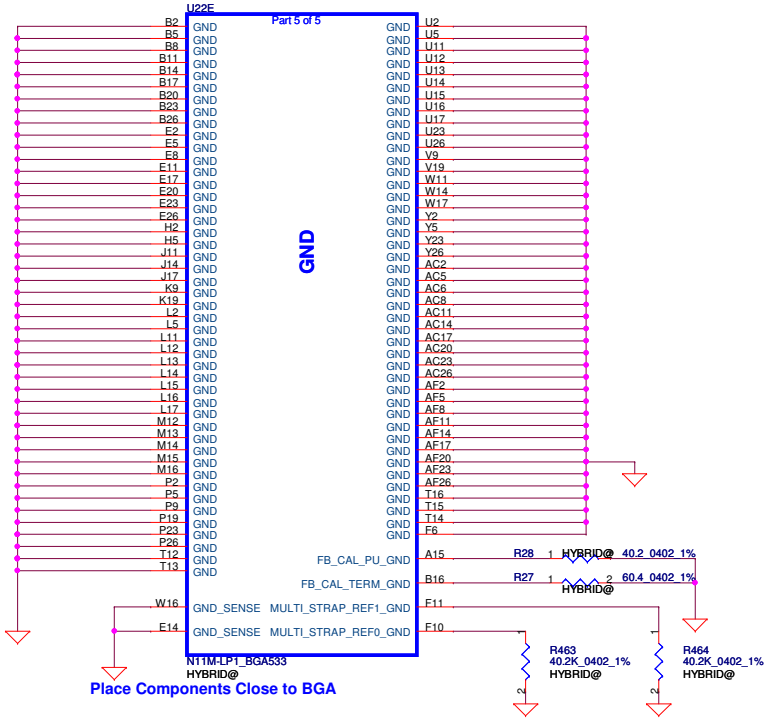
Compal Electronics, Inc.

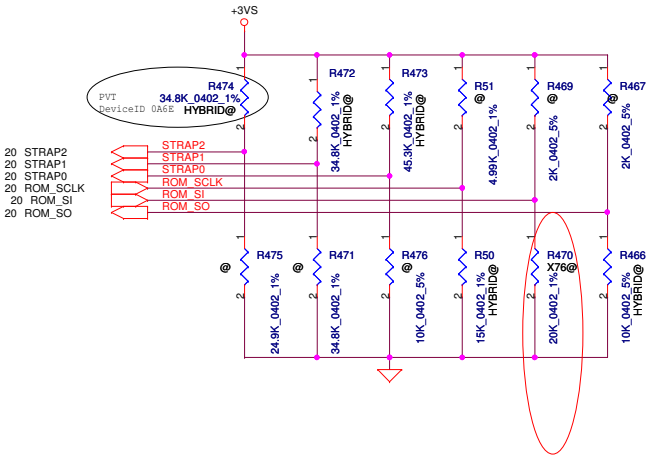
Title: **N10M-GE1 PWR**

Size	Document Number	Rev
Custom	LA-5941P	0.3

Date: Thursday, April 08, 2010 | Sheet 21 of 50

A total of 8 signals are required for GB1 strapping this includes
2 reference signals
6 physical strapping pins
4 logical strapping bits
A total of 24 logical strapping bits are available





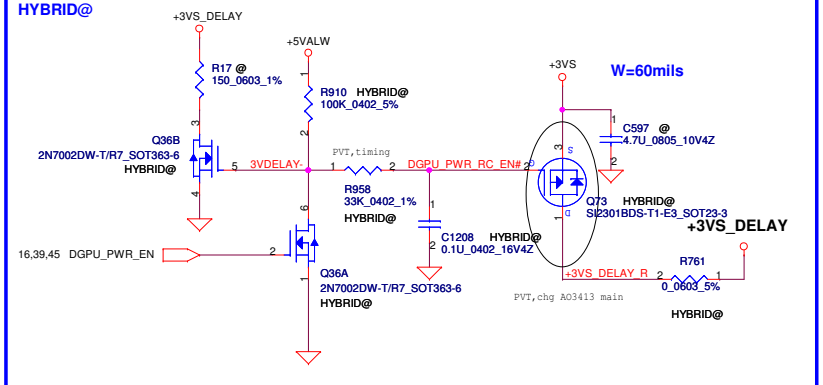
STRAP1 use for 3GIO_PADCFG to set 35K pull up.
(PUN-04335-001_V10 HW9 update)

GPU	FB Memory (DDR3)		ROM_SO	ROM_SCLK	ROM_SI	STRAP2	STRAP1	STRAP0
N11M-GE1 LP1 (0x0A7D) 40nm	Samsung 800MHz (defaul)	K4W1G1646E-HC12						
		64Mx16	PD 10K	PD 15K	PD 20K	PU 30K	PU 35K	PU 45K
	Hynix 800MHz	H5TQ1G63BFR-12C						
		64Mx16	PD 10K	PD 15K	PD 15K	PU 30K	PU 35K	PU 45K
					X76			

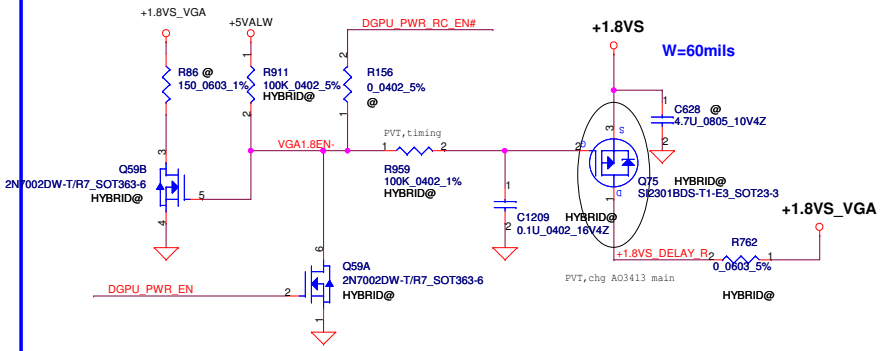
N11M-GE1 LP1	Memory/PKG	FBVDDQ	FB_CAL_PU_GND	FBCAL_PD_VDDQ	FBCAL_TERM_GND
	DDR3	+1.5VS	40.2 ohm	40.2 ohm	40.2/60.4 ohm

Must be used 1% resister for driver calibration DG-04642-001-V01(May 22, 2009)

HYBRID@



HYBRID@ 1021 add



Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

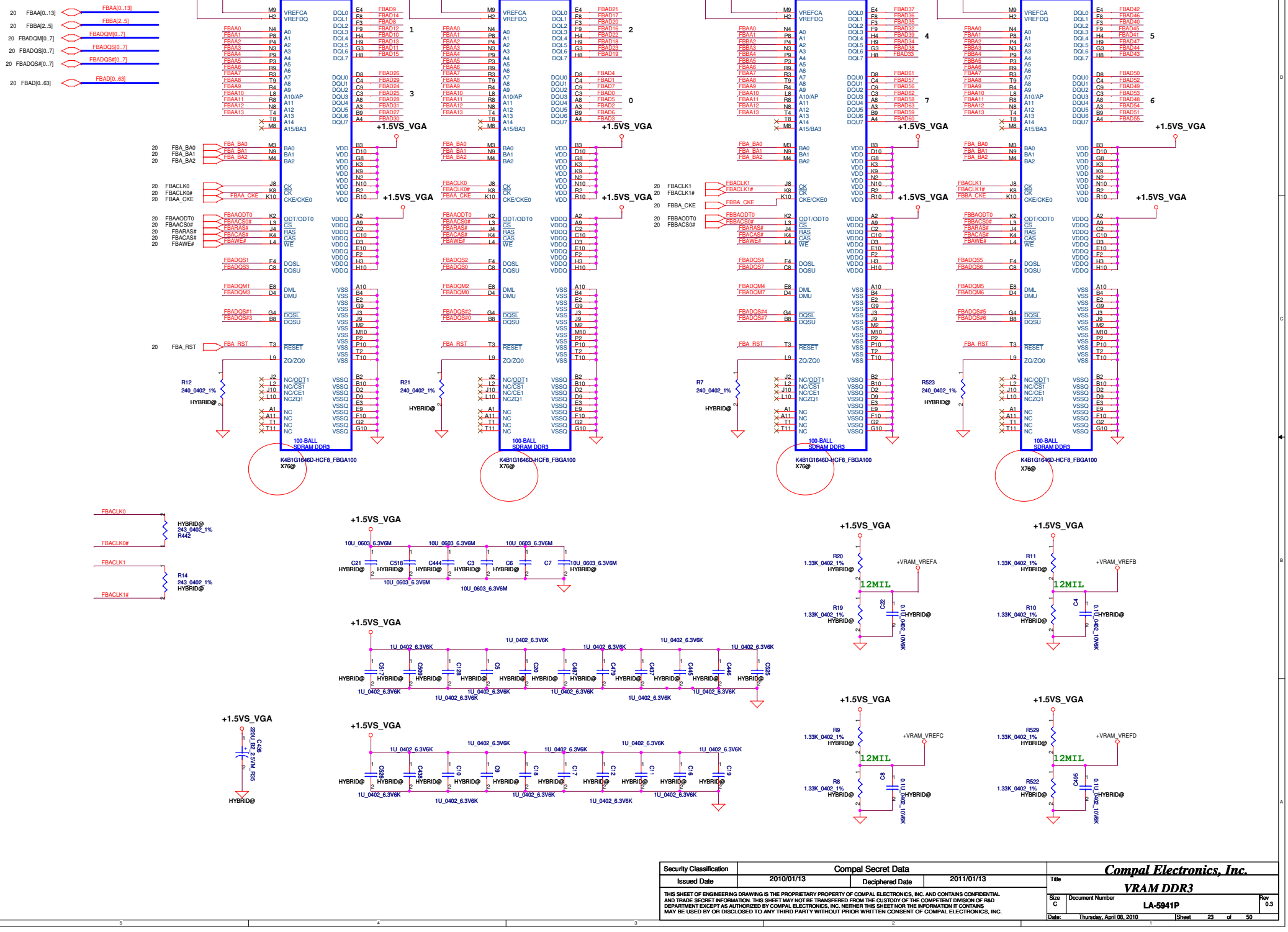
Compal Electronics, Inc.

Title: N10M-GE1 GND & STRAP

Size	Document Number	Rev
B	LA-5941P	0.3

Date: Thursday, April 08, 2010 Sheet 22 of 50

N10x 40nm DDR3 MAPPING
NVIDIA COCUMENT FOR DA-3978-001



Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: **VRAM DDR3**

Size	Document Number	Rev
C	LA-5941P	0.3

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From VGA

20 VGA_HDMI_CLK+	C284	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_CLK+_CK
20 VGA_HDMI_CLK-	C283	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_CLK-_CK
20 VGA_HDMI_TX0+	C282	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_TX0+_CK
20 VGA_HDMI_TX0-	C281	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_TX0-_CK
20 VGA_HDMI_TX1+	C601	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_TX1+_CK
20 VGA_HDMI_TX1-	C600	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_TX1-_CK
20 VGA_HDMI_TX2+	C614	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_TX2+_CK
20 VGA_HDMI_TX2-	C599	1	2	0.1U_0402_16V7K	HYBRID@	HDMI_TX2-_CK

Near L33,L34,L35,L36

From Level Shiftter

25 HDMI_CLK+_CK	HDMI_CLK+_CK
25 HDMI_CLK-_CK	HDMI_CLK-_CK
25 HDMI_TX0+_CK	HDMI_TX0+_CK
25 HDMI_TX0-_CK	HDMI_TX0-_CK
25 HDMI_TX1+_CK	HDMI_TX1+_CK
25 HDMI_TX1-_CK	HDMI_TX1-_CK
25 HDMI_TX2+_CK	HDMI_TX2+_CK
25 HDMI_TX2-_CK	HDMI_TX2-_CK

NEAR CONNECT

HDMI_CLK+_CONN	R585	HYBRID@	499_0402_1%	
HDMI_CLK-_CONN	R583	HYBRID@	499_0402_1%	
HDMI_TX0+_CONN	R589	HYBRID@	499_0402_1%	
HDMI_TX0-_CONN	R587	HYBRID@	499_0402_1%	
HDMI_TX1+_CONN	R593	HYBRID@	499_0402_1%	
HDMI_TX1-_CONN	R591	HYBRID@	499_0402_1%	
HDMI_TX2+_CONN	R597	HYBRID@	499_0402_1%	
HDMI_TX2-_CONN	R595	HYBRID@	499_0402_1%	

Q41 HYBRID@ 2N7002W-T/R7_SOT323-3 → +3VS

L33 @ WCM-2012-900T_4P
HDMI_CLK+_CK ↔ HDMI_CLK+_CONN
HDMI_CLK-_CK ↔ HDMI_CLK-_CONN

L34 @ WCM-2012-900T_4P
HDMI_TX0+_CK ↔ HDMI_TX0+_CONN
HDMI_TX0-_CK ↔ HDMI_TX0-_CONN

L35 @ WCM-2012-900T_4P
HDMI_TX1+_CK ↔ HDMI_TX1+_CONN
HDMI_TX1-_CK ↔ HDMI_TX1-_CONN

L36 @ WCM-2012-900T_4P
HDMI_TX2+_CK ↔ HDMI_TX2+_CONN
HDMI_TX2-_CK ↔ HDMI_TX2-_CONN

HDMI_CLK+_CK	R584	0_0402_5%	HDMI_CLK+_CONN	
HDMI_CLK-_CK	R582	0_0402_5%	HDMI_CLK-_CONN	
HDMI_TX0+_CK	R588	0_0402_5%	HDMI_TX0+_CONN	
HDMI_TX0-_CK	R586	0_0402_5%	HDMI_TX0-_CONN	
HDMI_TX1+_CK	R592	0_0402_5%	HDMI_TX1+_CONN	
HDMI_TX1-_CK	R590	0_0402_5%	HDMI_TX1-_CONN	
HDMI_TX2+_CK	R596	0_0402_5%	HDMI_TX2+_CONN	
HDMI_TX2-_CK	R594	0_0402_5%	HDMI_TX2-_CONN	

+3VS_DELAY
20 VGA_HDMI_SDA → Q84B HYBRID@ 2N7002DW-T/R7_SOT363-6 → HDMIDAT_R
20 VGA_HDMI_SCL → Q84A HYBRID@ 2N7002DW-T/R7_SOT363-6 → HDMICLK_R
C611 HYBRID@ 12P_0402_50V8J
C603 HYBRID@ 12P_0402_50V8J

+3VS
25 HP_DET# → R615 10K_0402_1% UMA@
16 DGPU_HPD_INT# → DGPU_HPD_INT# R618 0_0402_5% HYBRID@ → HP_DET#
Q53 2N7002W-T/R7_SOT323-3
C678 0.1U_0402_16V4Z
R616 100K_0402_5% → HP_DET
+3VS_DELAY → R617 10K_0402_1% HYBRID@
19 HDMI_DETECT_VGA → HDMI_DETECT_VGA
Q52 HYBRID@ 2N7002W-T/R7_SOT323-3

W=40mils
+5VS → D28 PMEG2010ET SOT23 → +5VS_HDMI_R
R581 0_0805_5% @
F2 1.1A_6V_SMD1812P110TF
R603 0_0805_5% @
+5VS_HDMI
C627 0.1U_0402_16V4Z
R249 2.2K_0402_5%
R257 2.2K_0402_5%

25 HP_DET
25 HDMIDAT_R
25 HDMICLK_R

JHDMI1 (PVT DIP type) FOX_QJ1119L-NVBT-7H ME@

19	HP_DET		
18	+5V		
17	DDC/CEC_GND		
16	SDA		
15	SCL		
14	Reserved		
13	CEC		
12	CK-	GND1	20
11	CK_shield	GND2	21
10	CK+		
9	D0-		
8	D0_shield		
7	D0+		
6	D1-		
5	D1_shield		
4	D1+		
3	D2-		
2	D2_shield		
1	D2+		

+5VS → HDMIDAT_R → @ D24 BAT54S-7-F_SOT23-3
+5VS → HDMICLK_R → @ D25 BAT54S-7-F_SOT23-3

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: HDMI CONN

Size	Document Number	Rev
Custom	LA-5941P	0.3

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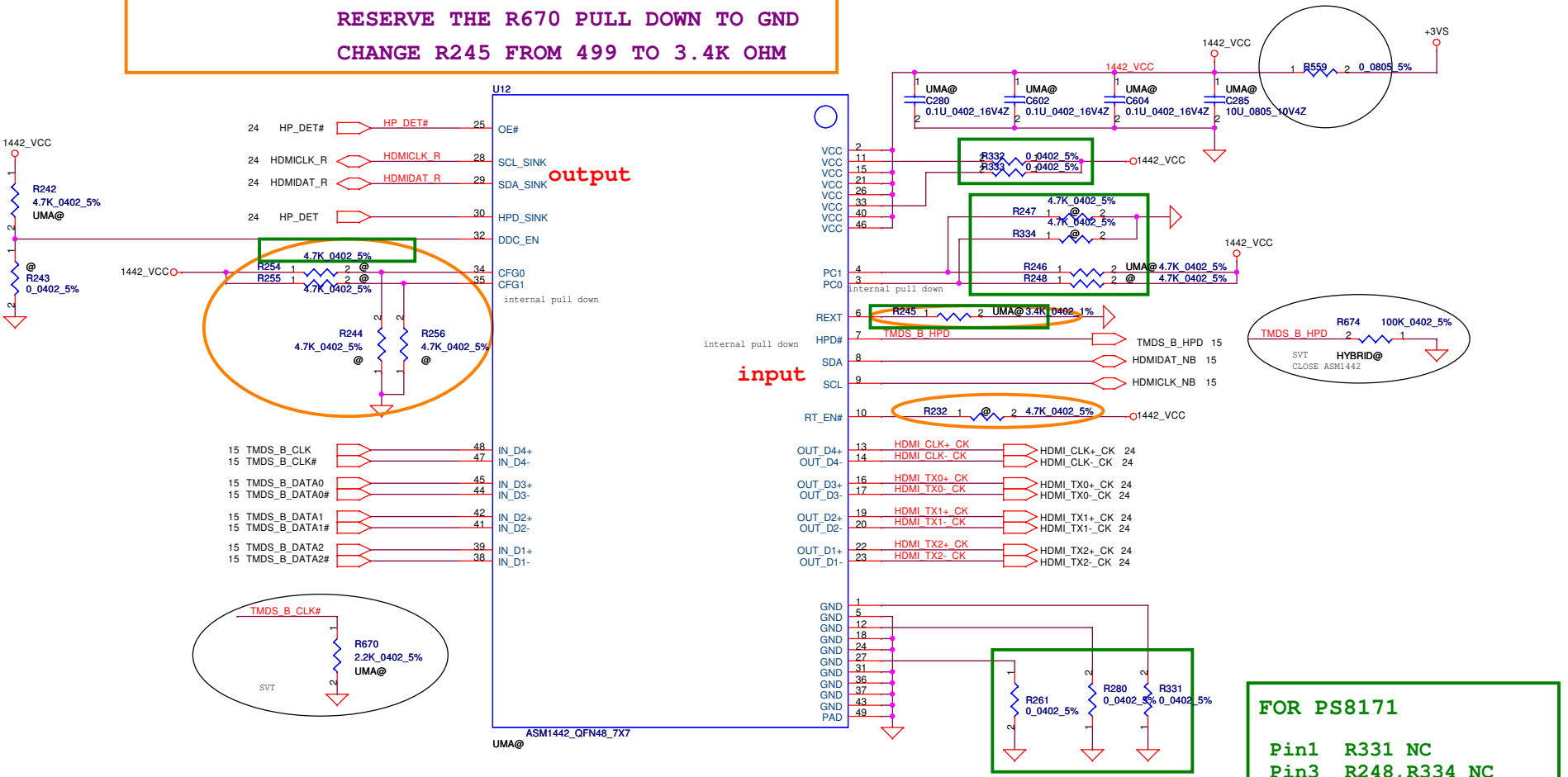
P/N:SA00003GT00 (ASM1442)

FOR asmedia R428 STUFF
RESERVE THE R668 PULL UP TO 3VS
RESERVE THE R670 PULL DOWN TO GND
CHANGE R245 FROM 499 TO 3.4K OHM



FOR PS8171

Pin1 R331 NC
Pin3 R248,R334 NC
Pin4 R246,R247 NC
Pin6 R245 499ohm
Pin11 R332 NC
Pin12 R280 NC
Pin27 R261 NC
Pin33 R333 NC
Pin34 R254 4.7K ohm

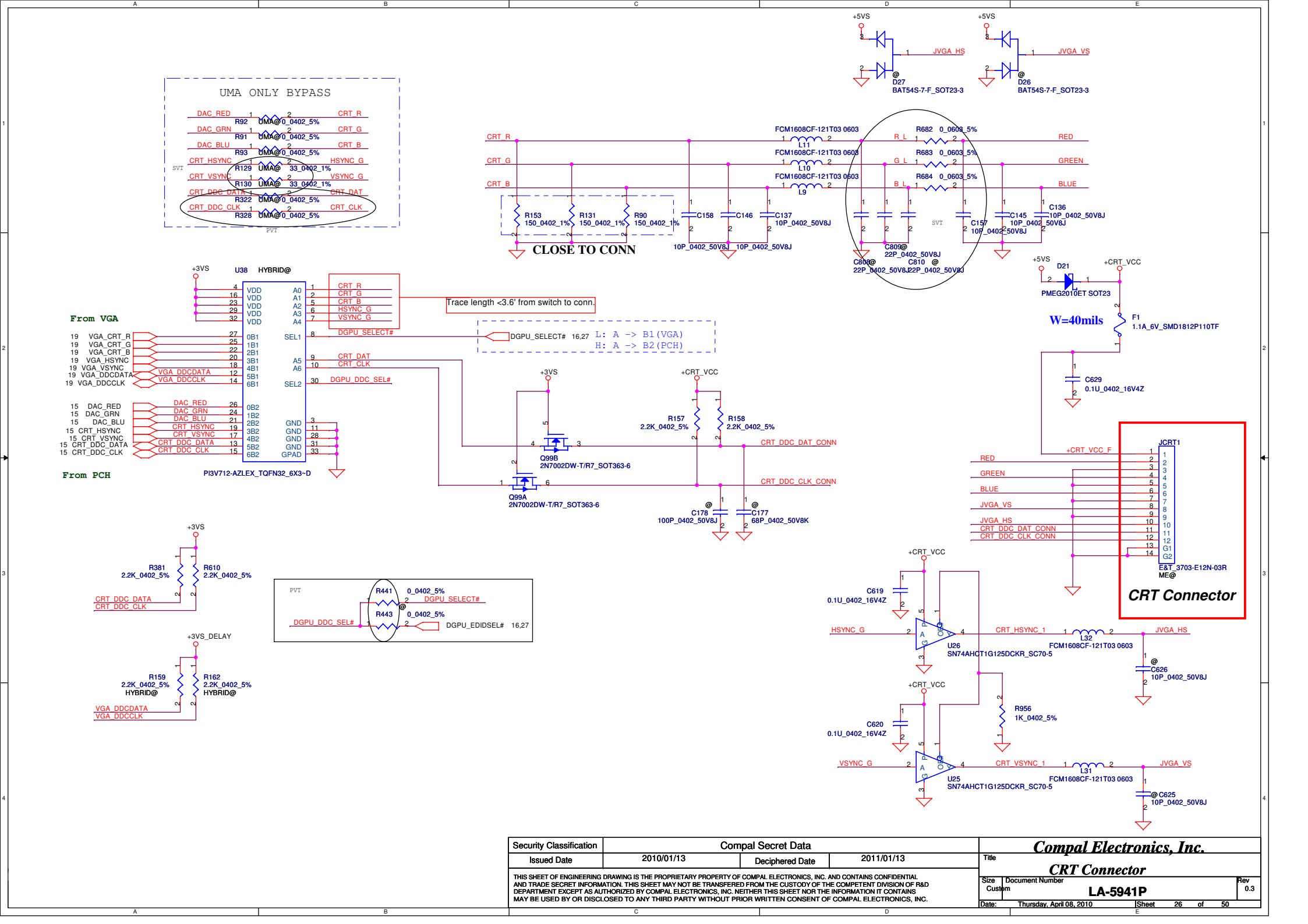
Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: Level Shiftter_ASM1442

Size: Custom | Document Number: LA-5941P | Rev: 0.3

Date: Thursday, April 08, 2010 | Sheet 25 of 50



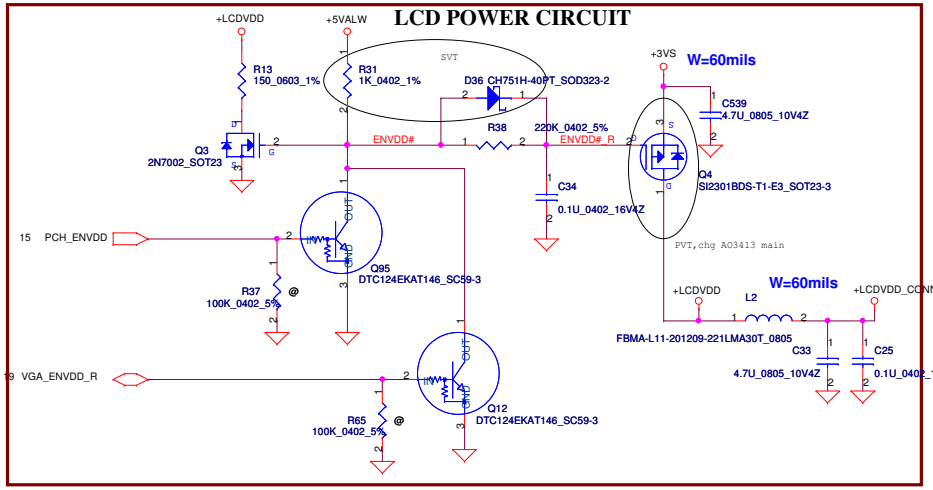
Compal Electronics, Inc.

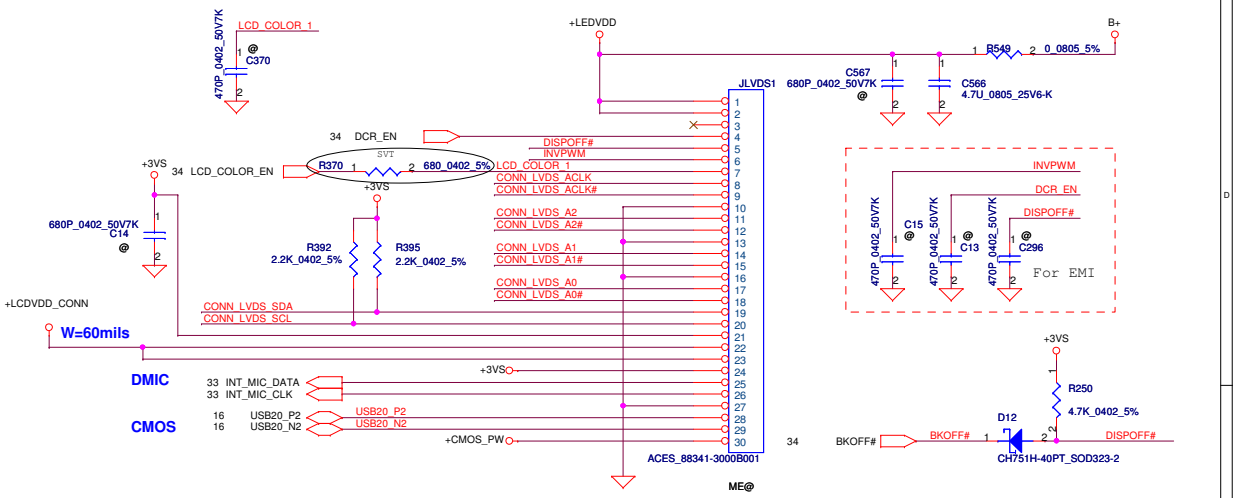
Title: CRT Connector

Size	Document Number	Rev
Custom	LA-5941P	0.3

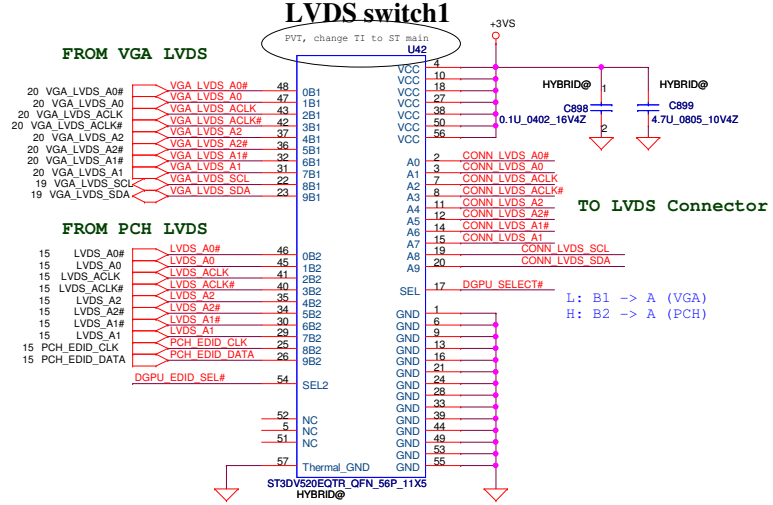
Date: Thursday, April 08, 2010 Sheet 26 of 50

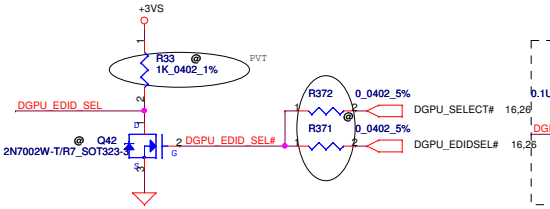
LCD POWER CIRCUIT

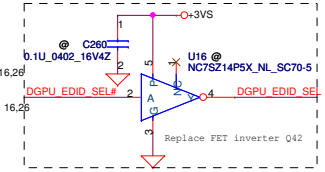




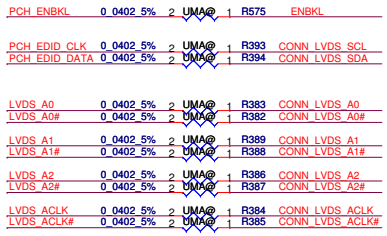
LVDS switch1





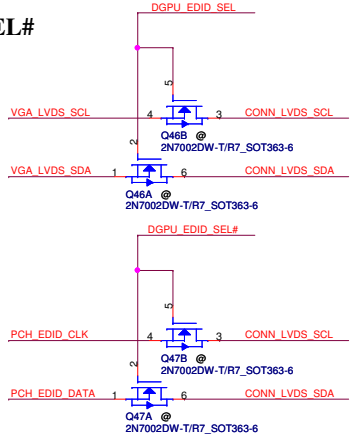


UMA SW BYPASS

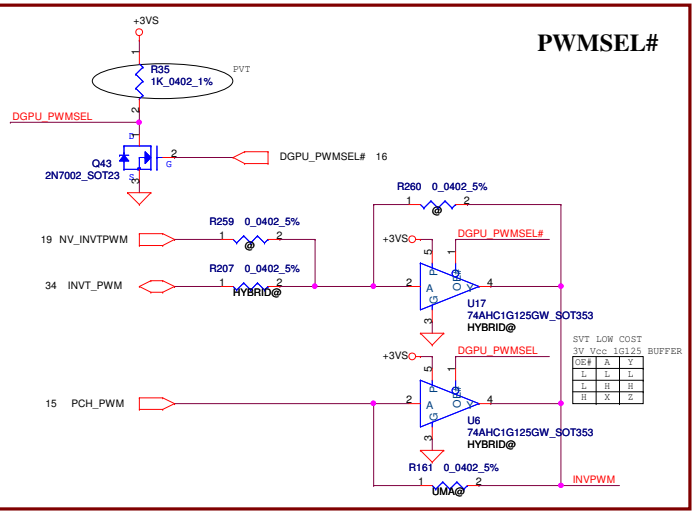


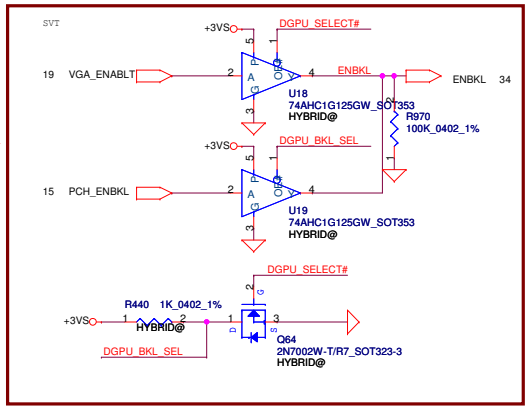
EDIDSEL#

L: VGA
H: PCH

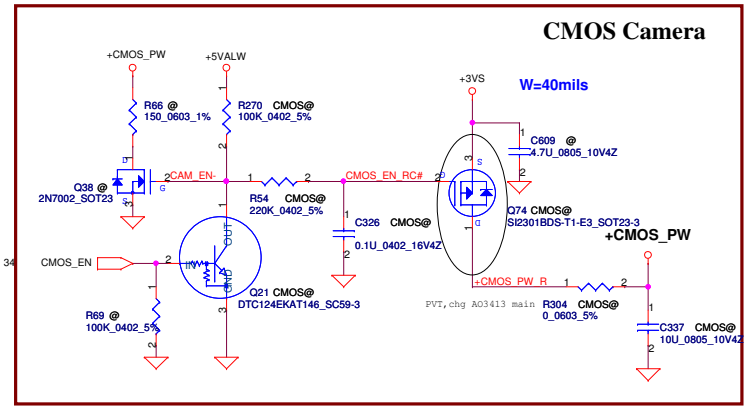


PWMSEL#





CMOS Camera



Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

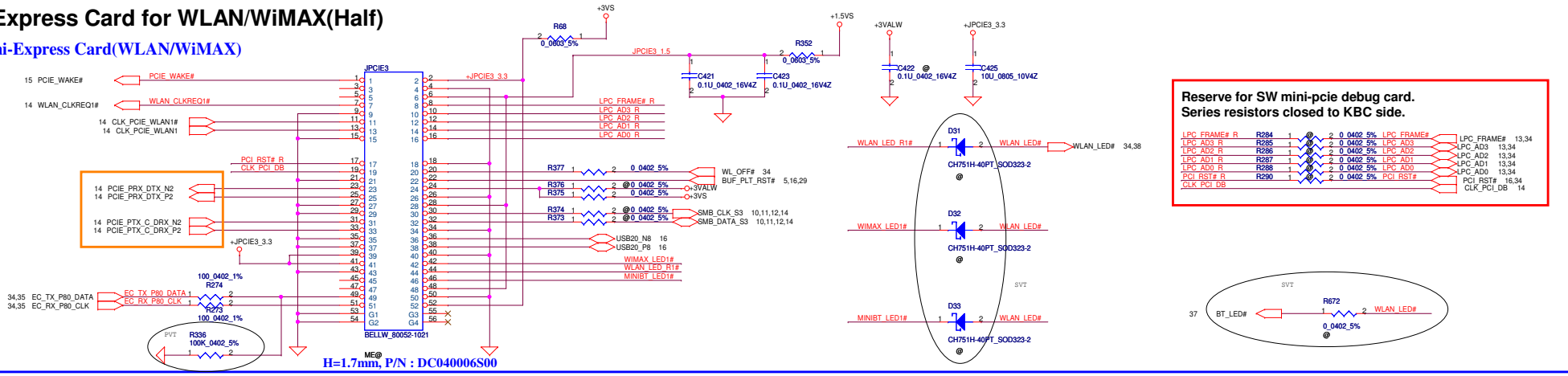
Title: **LVDS/CAMERA**

Size	Document Number	Rev
Custom	LA-5941P	0.3

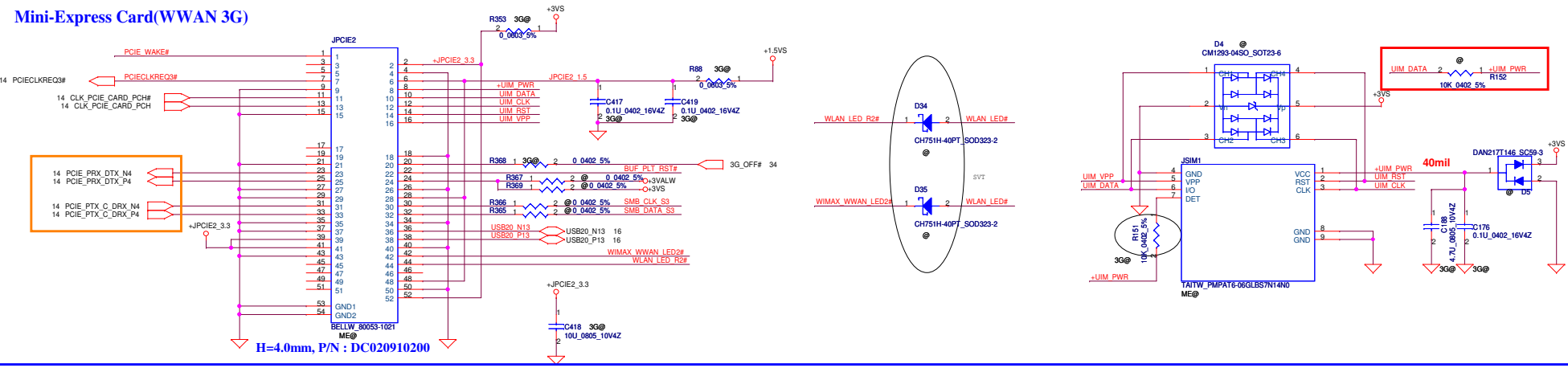
Date: Thursday, April 08, 2010 | Sheet 27 of 50

Mini-Express Card for WLAN/WiMAX(Half)

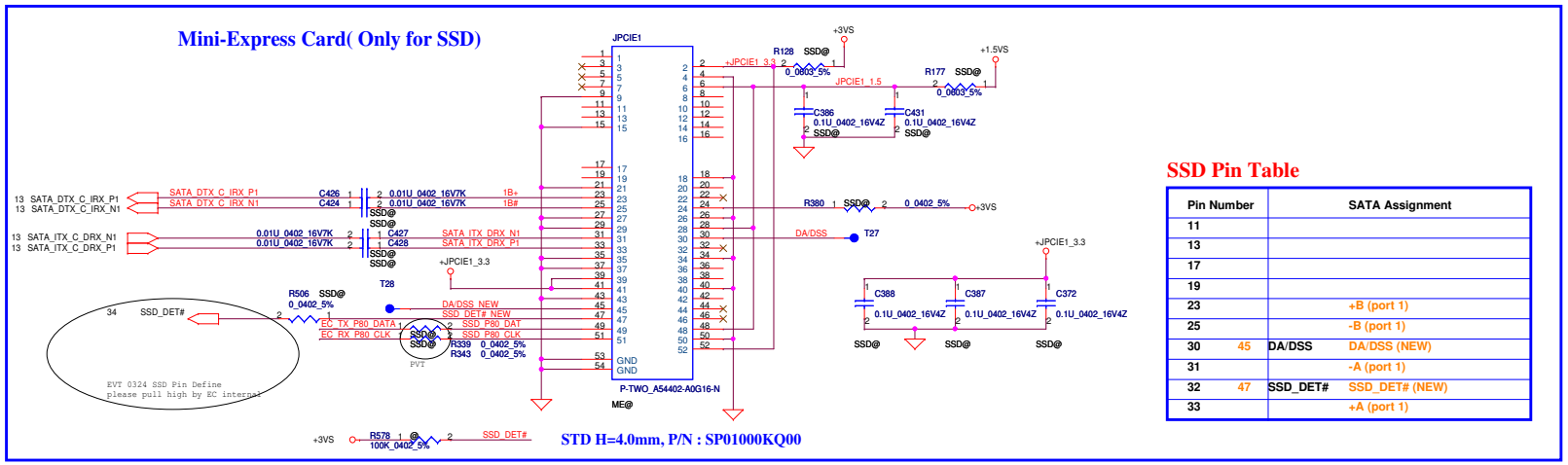
Mini-Express Card(WLAN/WiMAX)



Mini-Express Card(WWAN 3G)



Mini-Express Card(Only for SSD)

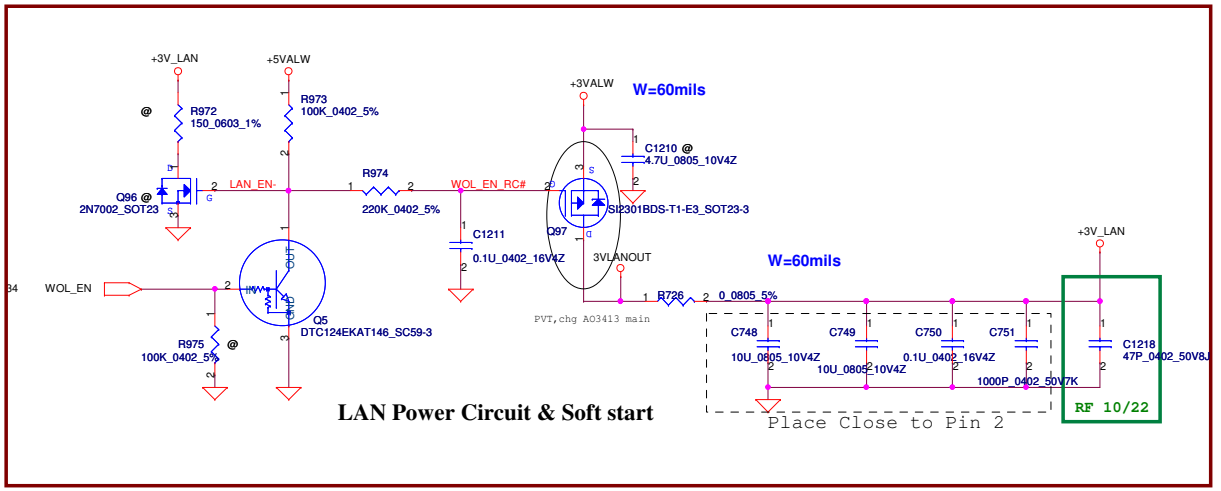


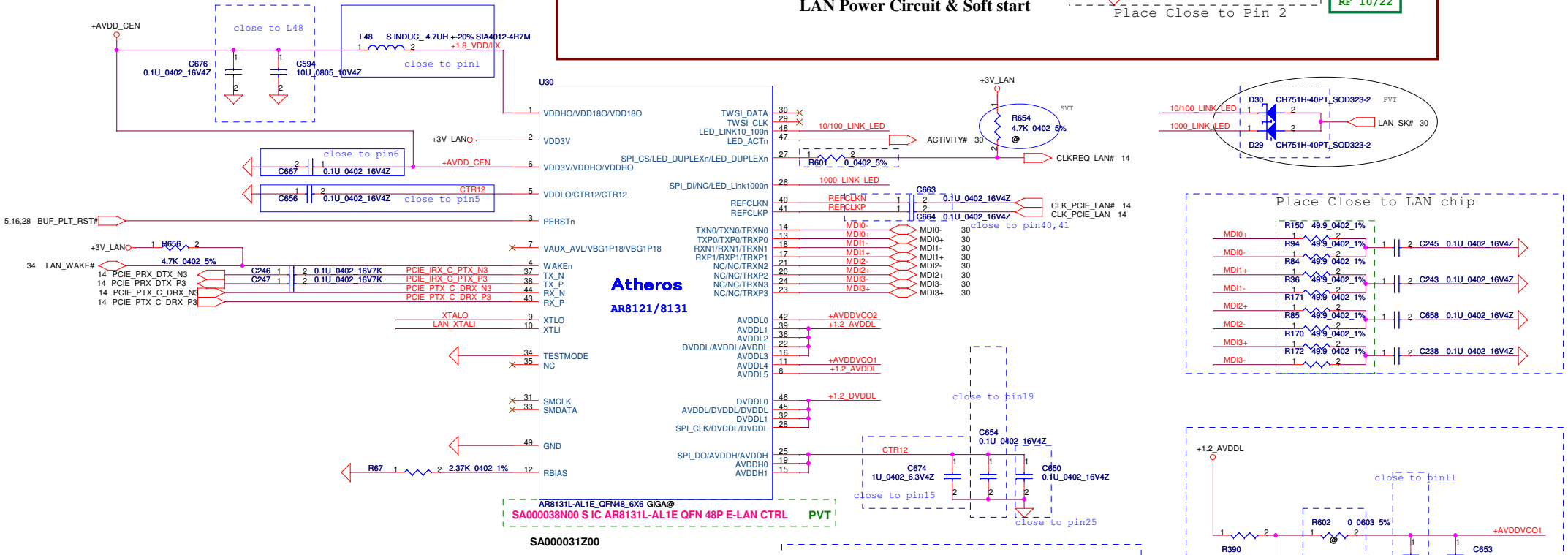
SSD Pin Table

Pin Number		SATA Assignment	
11			
13			
17			
19			
23			+B (port 1)
25			-B (port 1)
30	45	DA/DSS	DA/DSS (NEW)
31			-A (port 1)
32	47	SSD_DET#	SSD_DET# (NEW)
33			+A (port 1)

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.			
Title	Mini-Card/Nwe Card/SIM		
Size	Document Number	LA-5941P	Rev 0.3
Date: Thursday, April 08, 2010	Sheet 28 of 50		





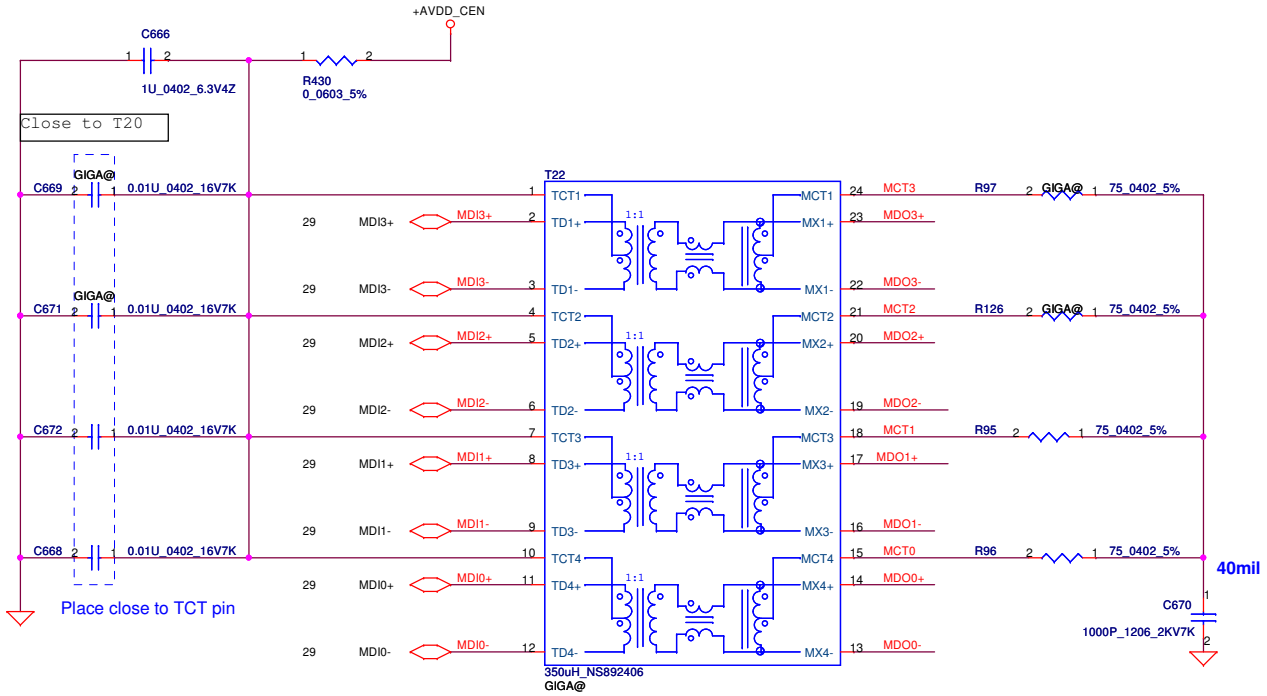
Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

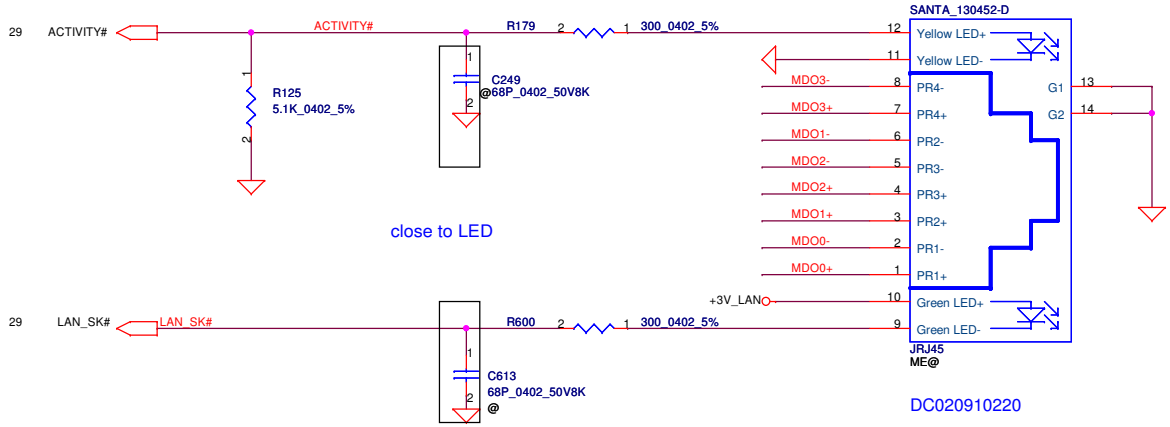
Title: AR8131/ AR8132

Size	Document Number	Rev
Custom		0.3

Date: Thursday, April 08, 2010 | Sheet 29 of 50



RJ45 Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

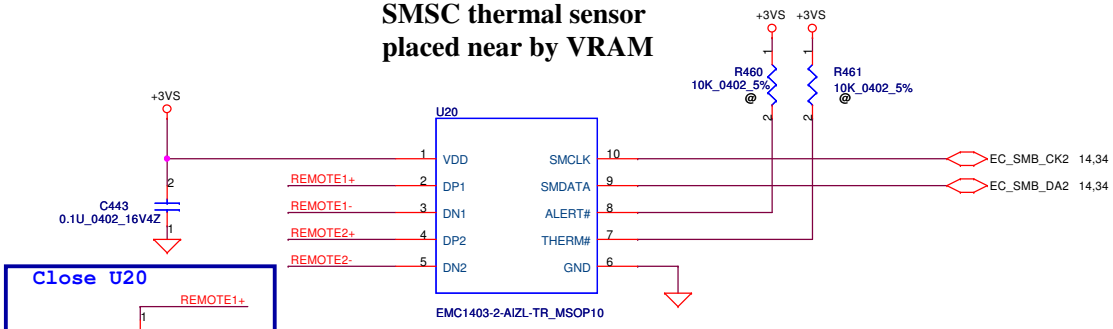
Compal Electronics, Inc.

Title: LAN Magnetic & RJ45

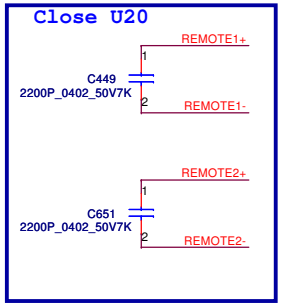
Size	Document Number	Rev
B	LA-5941P	0.3

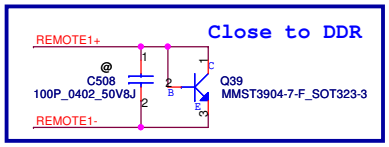
Date: Thursday, April 08, 2010 Sheet 30 of 50

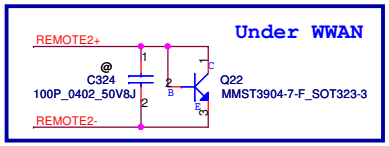
SMSC thermal sensor placed near by VRAM



Address 1001_101xb
P/N SA000029210

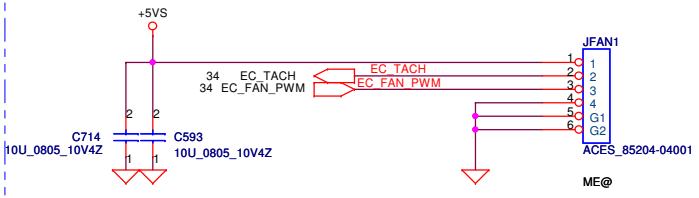






REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"

FAN1 Conn



SP02000CW00

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

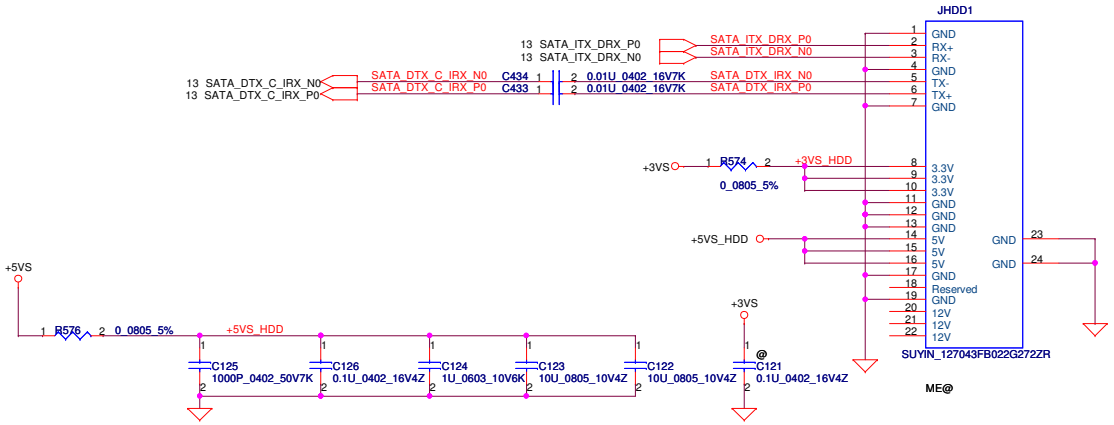
Compal Electronics, Inc.

Title: **EMC1403_Thermal sensor/FAN**

Size	Document Number	Rev
Custom	LA-5941P	0.3

Date: Thursday, April 08, 2010 Sheet 31 of 50

SATA HDD Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: HDD/ODD Connector

Size	Document Number	Rev
B	LA-5941P	0.3

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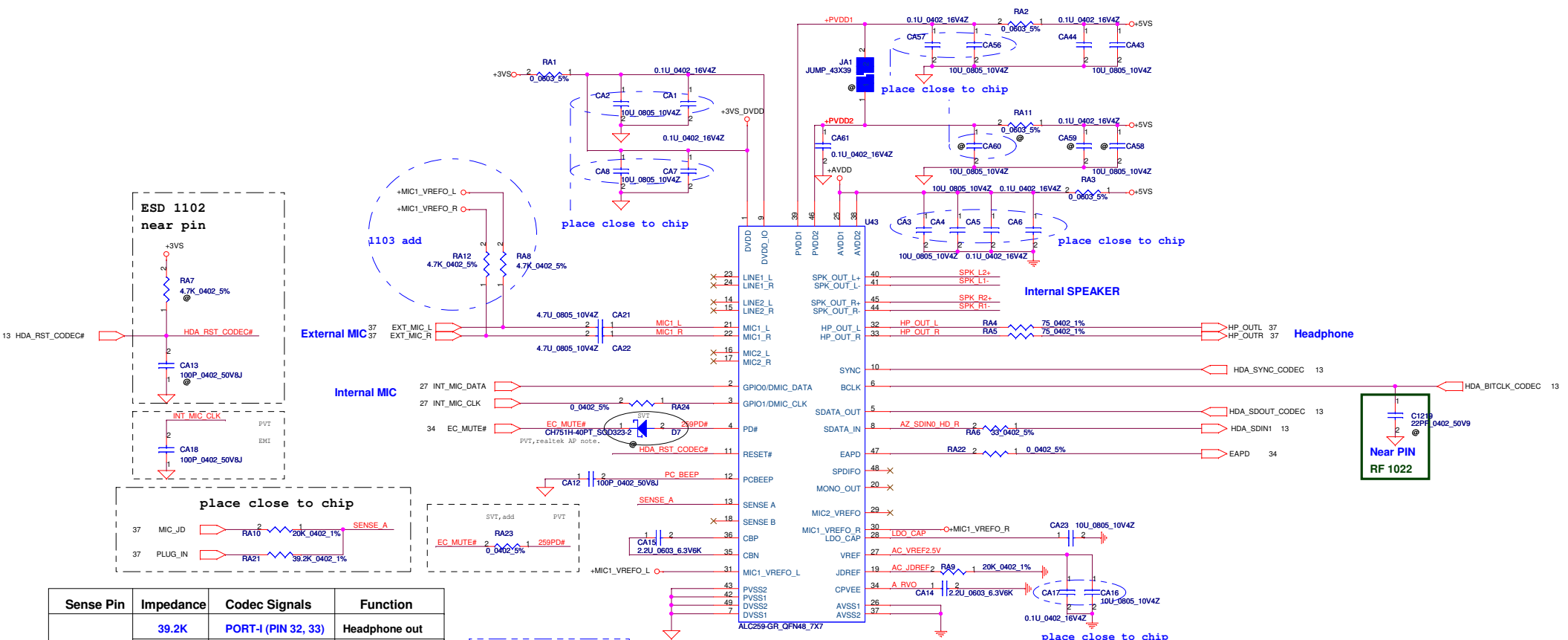
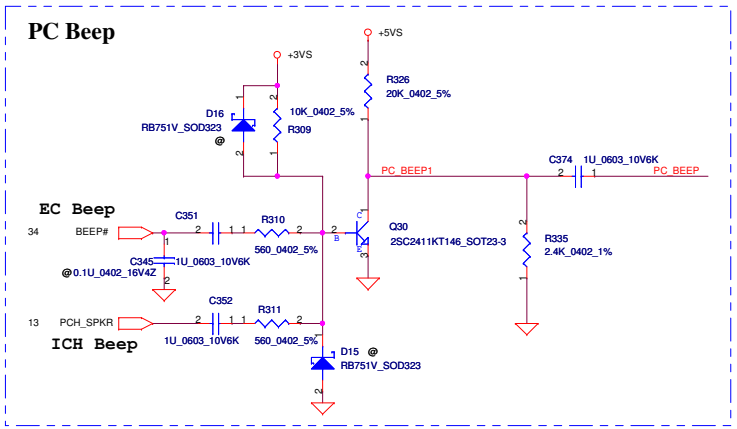
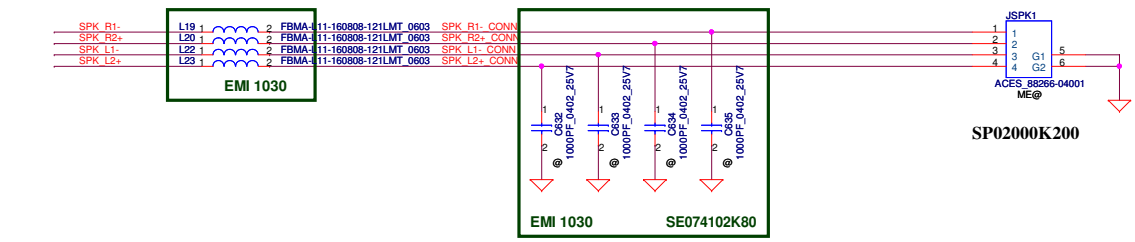


Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	





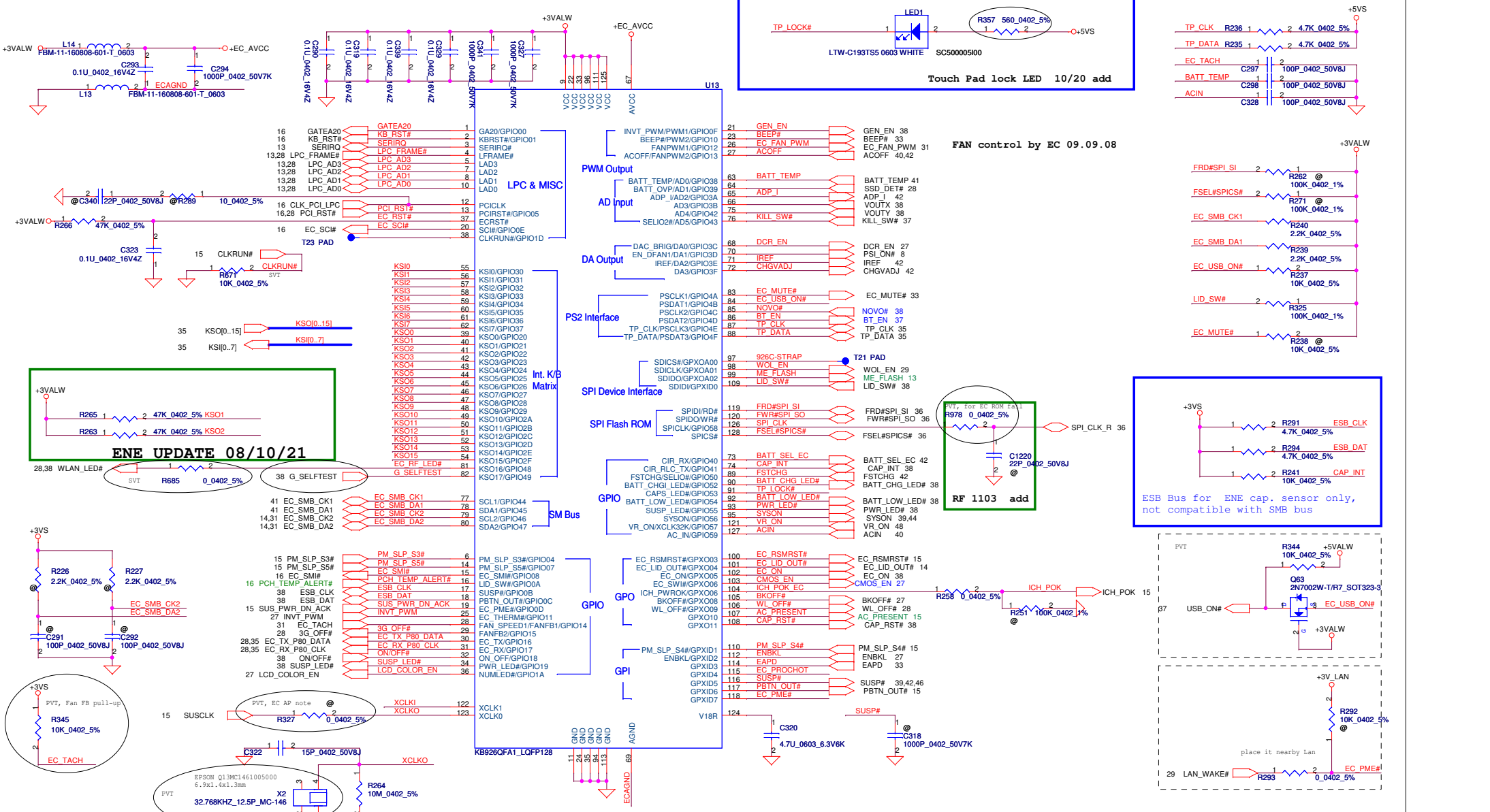
Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: **ALC259 Codec**

Size	Document Number	Rev
Custom	LA-5941P	0.3

Date: Thursday, April 08, 2010 | Sheet 33 of 50


U13
KB926QFA1_LQFP128
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Device Interface
SPI Flash ROM
GPIO
SM Bus
GPO
GPI
FAN control by EC 09.09.08
Touch Pad lock LED 10/20 add
ENE UPDATE 08/10/21
RF 1103 add
ESB Bus for ENE cap. sensor only, not compatible with SMB bus
ENE926E0 SA00001J5A0
PIN91 change to TP_LOCK#
PIN36 change to LCD_COLOR_EN
11/09 change EC pin
10/17 add
T23 PAD
T21 PAD
LED1
LTW-C193TS5 0603 WHITE
SC500005I00
X2
32.768KHZ_12.5P_MC-146
Q63
2N7002W-T/R7_SOT323-3
Q17
2N7002_SOT23
Compal Electronics, Inc.
BIOS & EC I/O Port
LA-5941P
Rev 0.3
Thursday, April 08, 2010
Sheet 34 of 50
Security Classification
Compal Secret Data
Issued Date 2010/01/13
Deciphered Date 2011/01/13
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INT_KBD Conn.

KSI[0..7] KSI[0..7] 34
KSO[0..15] KSO[0..15] 34

KSO2	C203	KSO1	C205	KSO7	C186	KSI2	C226
KSO15	C153	KSO7	C186	KSI2	C226	KSO5	C206
KSO6	C175	KSI2	C226	KSO5	C206	KSI3	C225
KSO8	C185	KSO5	C206	KSI3	C225	KSO14	C156
KSO13	C172	KSI3	C225	KSO14	C156	KSI7	C236
KSO12	C173	KSO14	C156	KSI7	C236	KSI6	C235
KSO11	C155	KSI7	C236	KSI6	C235	KSI5	C228
KSO10	C154	KSI6	C235	KSI5	C228	KSI4	C233
KSO3	C174	KSI5	C228	KSI4	C233	KSO9	C234
KSO4	C187	KSI4	C233	KSO9	C234	KSI1	C241
KSI0	C204	KSO9	C234	KSI1	C241		
KSO0	C227	KSI1	C241				

All: 1 — 2 @100P_0402_50V8J

KB Matrix 10/30

JKB1

KSI1	1	1	
KSI7	2	2	
KSI6	3	3	
KSO9	4	4	
KSI4	5	5	
KSI5	6	6	
KSO0	7	7	
KSI2	8	8	
KSI3	9	9	
KSO5	10	10	
KSO1	11	11	
KSI0	12	12	
KSO2	13	13	
KSO4	14	14	
KSO7	15	15	
KSO8	16	16	
KSO6	17	17	
KSO3	18	18	
KSO12	19	19	
KSO13	20	20	
KSO14	21	21	
KSO11	22	22	
KSO10	23	23	
KSO15	24	24	
		GND2	26
		GND1	25

E-T_6905-E24N-01R
ME@

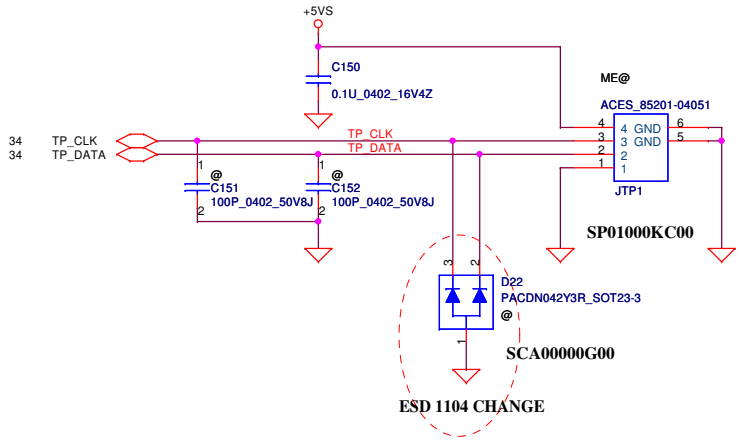
EC DEBUG PORT

JP11

	+3VALW	1	1
28,34	EC_TX_P80_DATA	EC_TX_P80_DATA 2	2
28,34	EC_RX_P80_CLK	EC_RX_P80_CLK 3	3
		4	4

ACES_85205-0400
ME@

To TP/B Conn.



Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

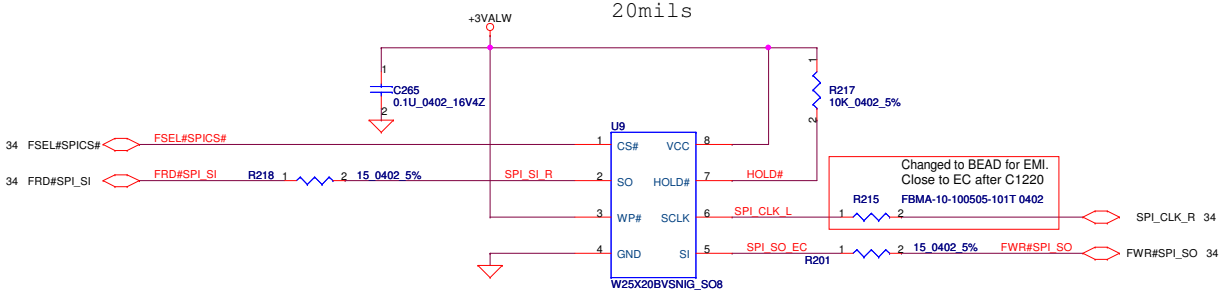
Title: KB /SW /LPC Debug Conn.

Size	Document Number	Rev
B	LA-5941P	0.3

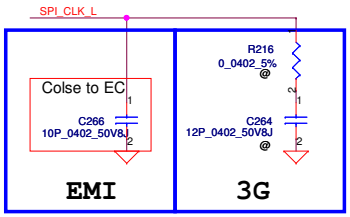
Date: Thursday, April 08, 2010 Sheet 35 of 50

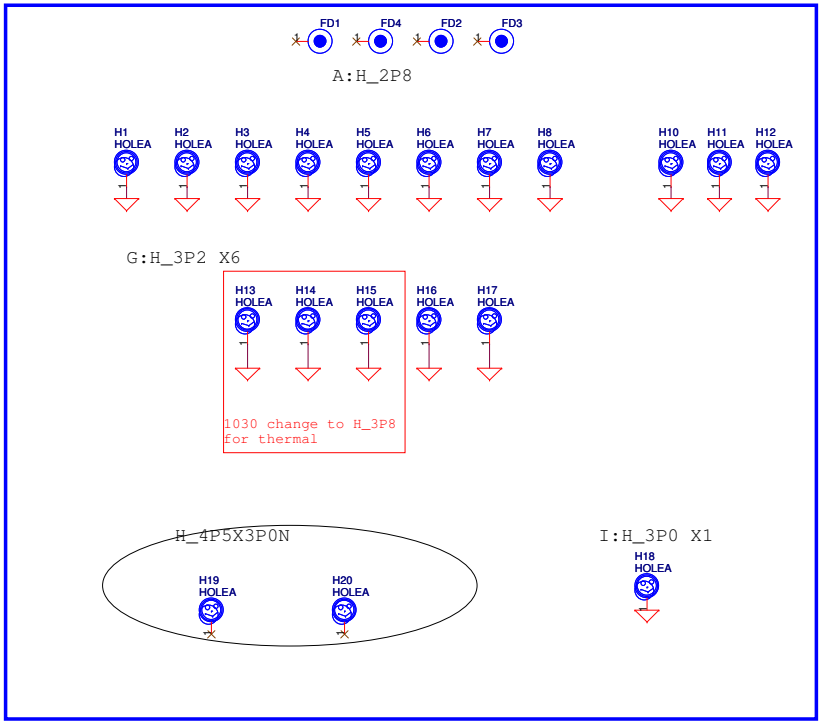
FOR EC 256KB SPI ROM
(150mil PACKAGE)

20mils



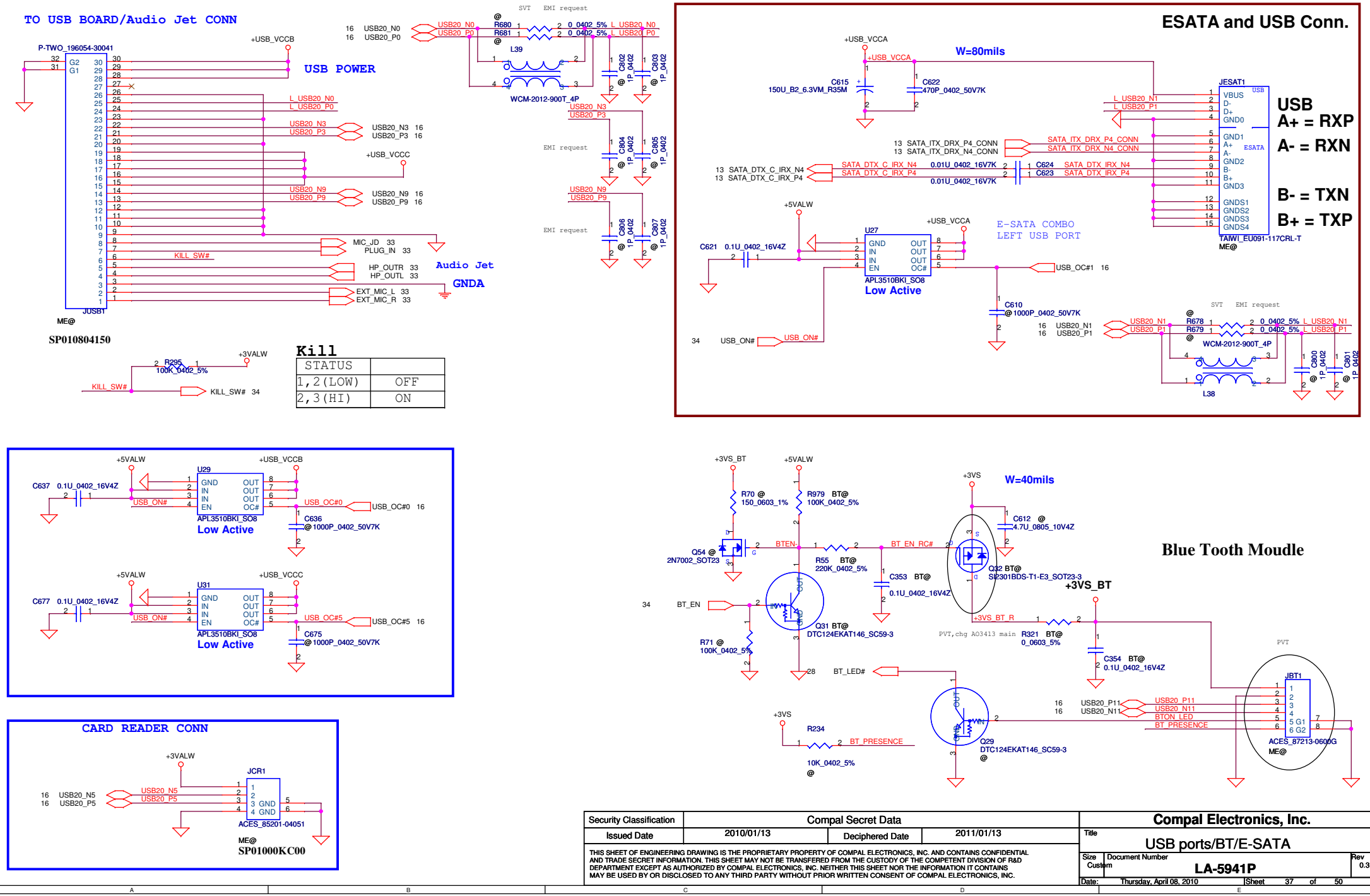
SA00003GM10





Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.			
Title	EC SPI ROM		
Size B	Document Number LA-5941P		Rev 0.3
Date: Thursday, April 08, 2010	Sheet 36 of 50		



Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: USB ports/BT/E-SATA

Size	Document Number	Rev
Custom	LA-5941P	0.3

Date: Thursday, April 08, 2010 Sheet 37 of 50

ON/OFF switch FOR DEBUG

Power Button

TOP Side

Bottom Side

SW1 SMT1-05_4P

D14 BAV70W_SOT323-3

R272 100K_0402_5%

R302 10K_0402_5%

Q28 2N7002_SOT23-3

ON/OFFBTN# ON/OFF# ON/OFF# 34 51_ON# 51_ON# 40 EC_ON EC_ON 34

+3VALW

Power Bottom Board Conn.4pin

JPW1 ACES_85201-04051

34 PWR_LED# ON/OFFBTN#

ME@

SP01000KC00

NOVOBottom/ALS Board Conn.6pin

JFB1 ACES_85201-06051

34 ALS_CLK 34 ALS_DATA 34 LID_SW# NOVO_BTN#

ME@

SP01000B000

D19 PJSOT24C 3P C/A SOT-23

D20 PJSOT24C 3P C/A SOT-23

R296 100K_0402_5% PVT

D13 BAV70W_SOT323-3

34 NOVO# NOVO# 51_ON# NOVO_BTN#

EMI REQUEST 1ST = SCA00000E00

2ST = SCA00000R00

Cap Sensor Board Conn. 8pin

ENE SB3534

+3VS +5VS R349 R351 0_0402_5%

+5VS_CAP +3VS_CAP

JCAP1 ACES_85201-0805N

13 HDD_LED# 34 CAP_RST# 34 CAP_INT R3 I2C_INT_R R2 R1 34 ESB_DAT 34 ESB_CLK

C1 33P_0402_50V8J C2 33P_0402_50V8J

PIN adjust

ME@

SP01000H200

FP Board Conn 4 pin

+3VS

JFP1 ACES_85201-04051

16 USB20_N10 16 USB20_P10 USB20_N10 USB20_P10

ME@

SP01000KC00

APS G-Sensor

+3VS_GEN +5VALW +3VS W=20mils

RG7 @ 150_0603_1% RG2 GEN@ 100K_0402_5%

QG2 @ 2N7002_SOT23 GENEN-

RG8 GEN@ 220K_0402_5% GEN_EN_RC#

CG9 @ 4.7U_0805_10V4Z

CG4 GEN@ 0.1U_0402_16V4Z

QG1 GEN@ SI2301BDS-T1-E3_SOT23-3

+3VS_GEN_R

34 GEN_EN

QG3 GEN@ DTC124EKAT146_SC59-3

PVT,chg AO3413 main

RG9 @ 100K_0402_5%

RG1 GEN@ 47_0402_5% +3VS_GEN_R

CG1 GEN@ 0.1U_0402_16V4Z

CG3 10U_0805_10V4Z GEN@

CG2 GEN@ 1U_0603_10V6K

RG3 @ 10K_0402_5%

RG6 GEN@ 100K_0402_5%

34 G_SELFTEST ST

UG1 GEN@

ST Xout Yout Vs Vs NC NC NC NC NC NC NC NC COM COM COM COM

S IC LIS244ALTR LGA 16P G-SENSOR

RG4 GEN@ 56K_0402_5%

RG5 GEN@ 56K_0402_5%

PVT

VOUTX VOUTY VOUTX 34 VOUTY 34

CG7 GEN@ 0.1U_0402_16V4Z

CG8 GEN@ 0.1U_0402_16V4Z

LED CONN 8 pin

Amber

Blue

+5VALW +3VALW +5VS

JLED ACES_85201-0805N

34 SUSP_LED# 34 BATT_LOW_LED# 34 BATT_CHG_LED# 28,34 WLAN_LED# WLAN_LED#

ME@

SP01000H200

+1.5VS_VGA +3VS +5VALW

C723 0.1U_0402_16V4Z

C724 0.1U_0402_16V4Z

C725 0.1U_0402_16V4Z

C729 0.1U_0402_16V4Z

+3VS +5VS +1.05VS +VGA_CORE +1.5VS_VGA

C720 0.1U_0402_16V4Z

C721 0.1U_0402_16V4Z

C722 0.1U_0402_16V4Z

C726 0.1U_0402_16V4Z

C727 0.1U_0402_16V4Z

C728 0.1U_0402_16V4Z

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: **Audio Jack & SW connector**

Size	Document Number	Rev
Custom	LA-5941P	0.3

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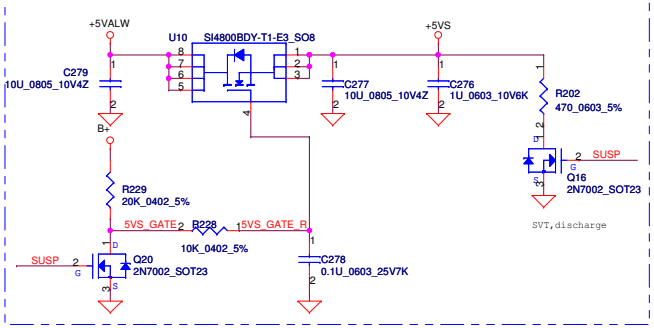
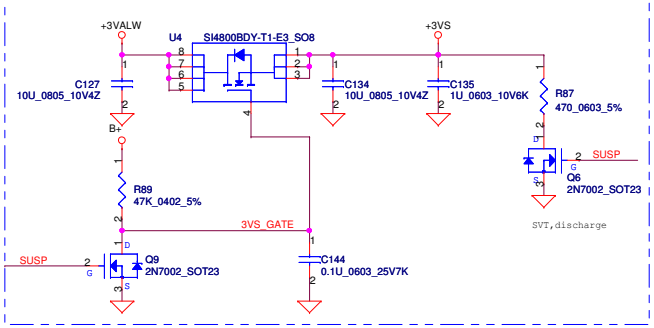
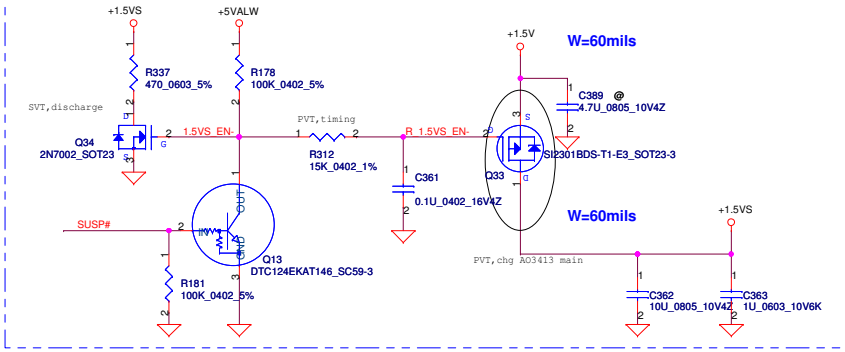
+5VALW TO +5VS

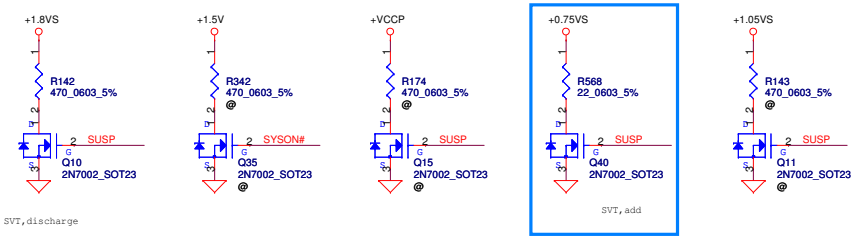


+3VALW TO +3VS

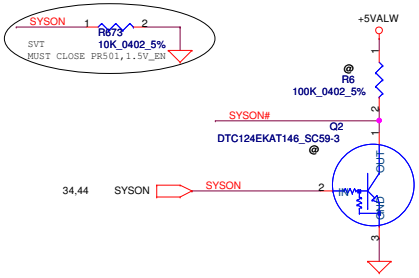


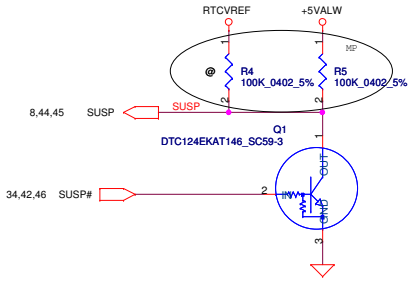
+1.5V to +1.5VS



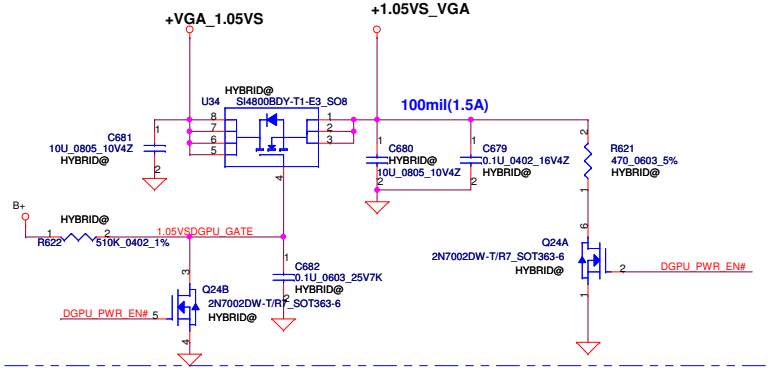


For Intel S3 Power Reduction.

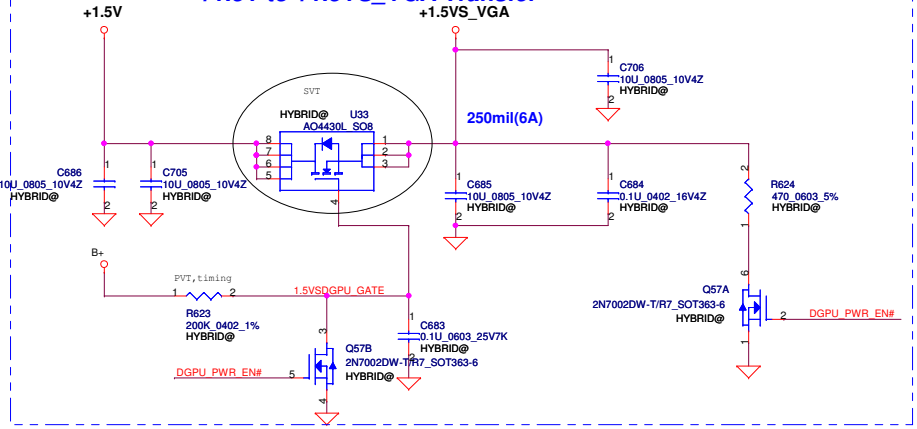


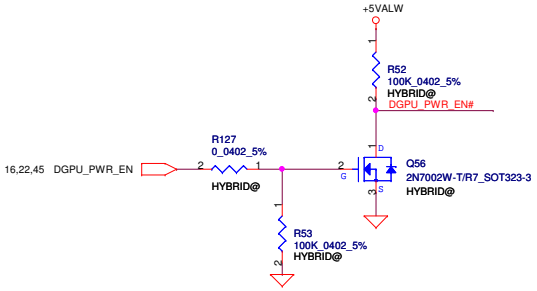


+1.05VS to +1.05VS_VGA Transfer



+1.5V to +1.5VS_VGA Transfer





Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: DC Interface

Size	Document Number	Rev
Custom	LA-5941P	0.3

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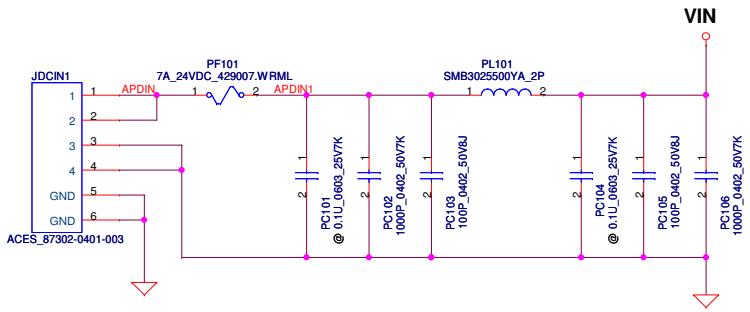
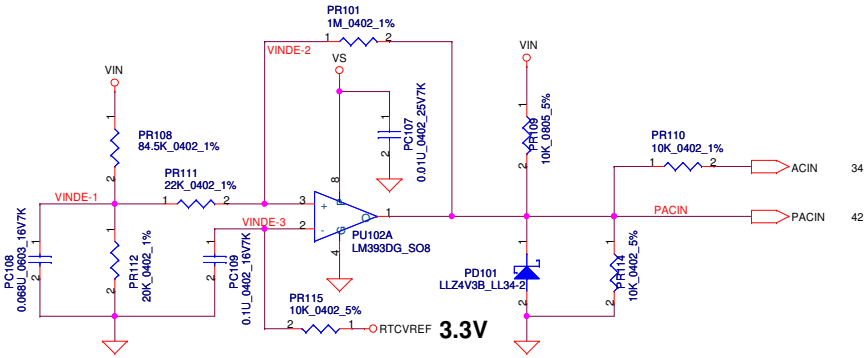
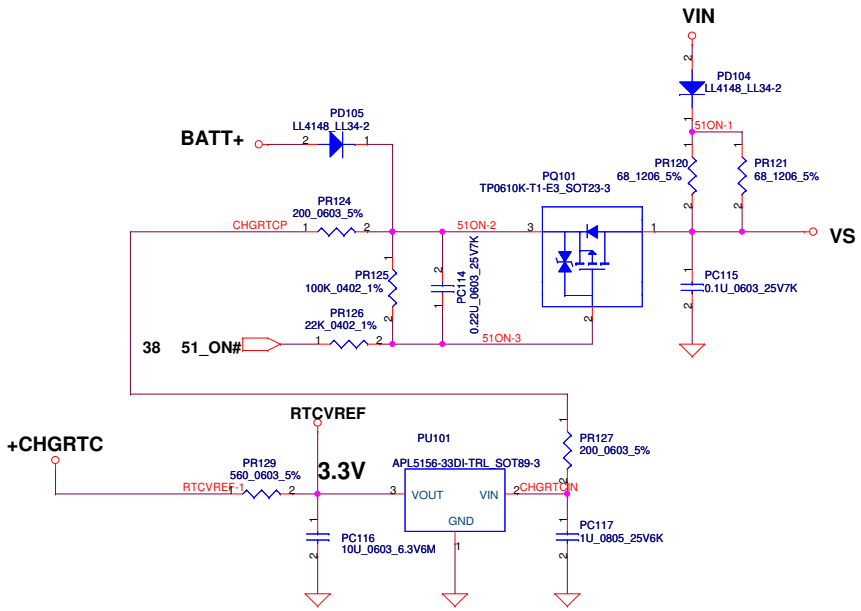


Vin Detector

	Min.	typ.	Max.
L-->H	17.430V	17.901V	18.384V
H-->L	16.976V	17.262V	17.728V





ACIN

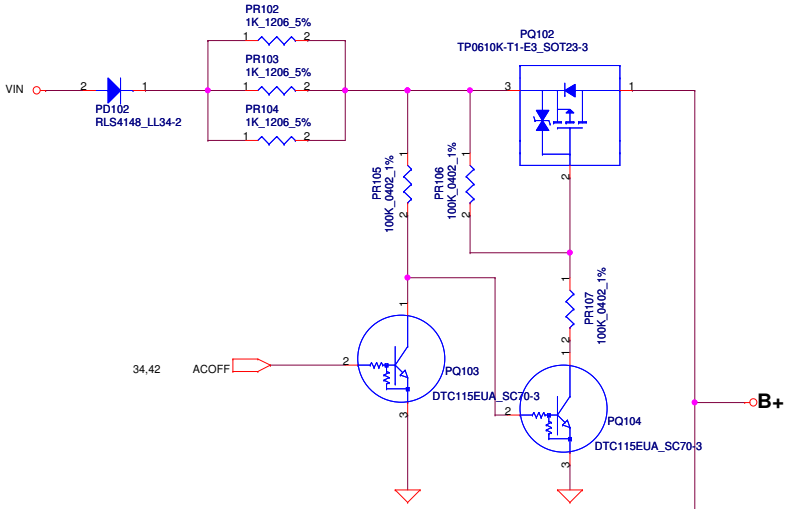
Precharge detector

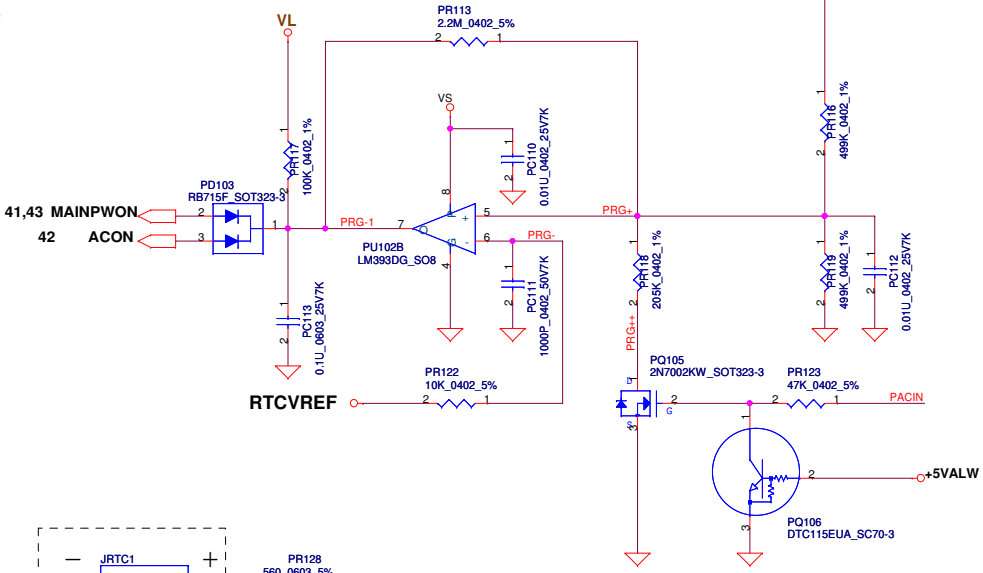
	Min.	typ.	Max.
L-->H	14.991V	15.381V	15.782V
H-->L	13.860V	14.247V	14.621V

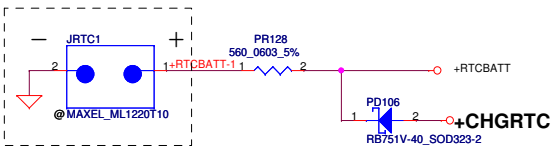
BATT ONLY

Precharge detector

	Min.	typ.	Max.
L-->H	7.196V	7.349V	7.505V
H-->L	6.138V	6.214V	6.056V







RTC Battery

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: DCIN & DETECTOR

Size	Document Number	Rev
Custom		0.3

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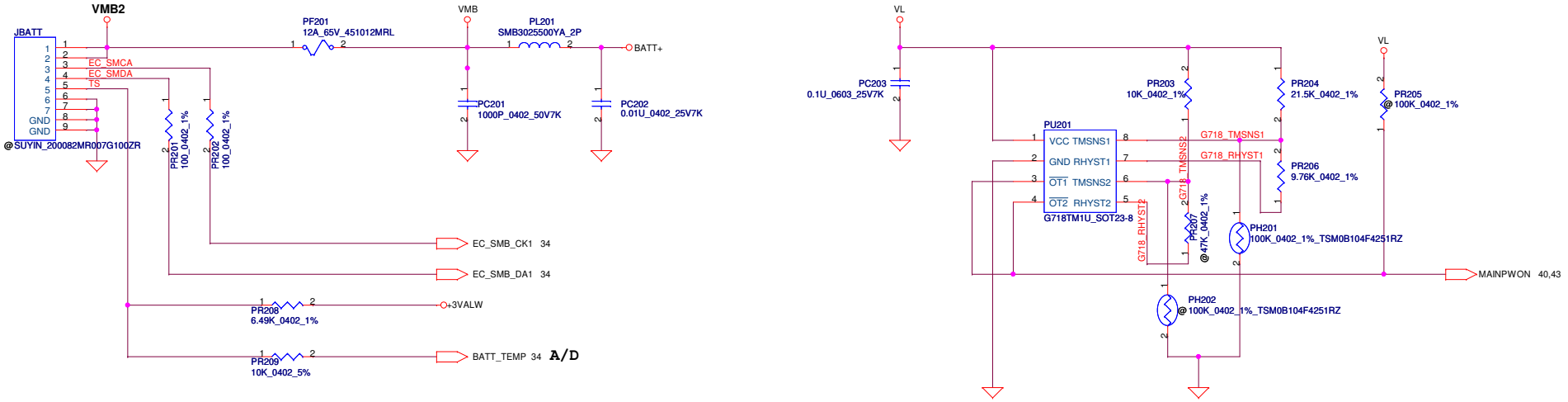
PH1 under CPU botten side :
CPU thermal protection at 92 degree C
Recovery at 56 degree C



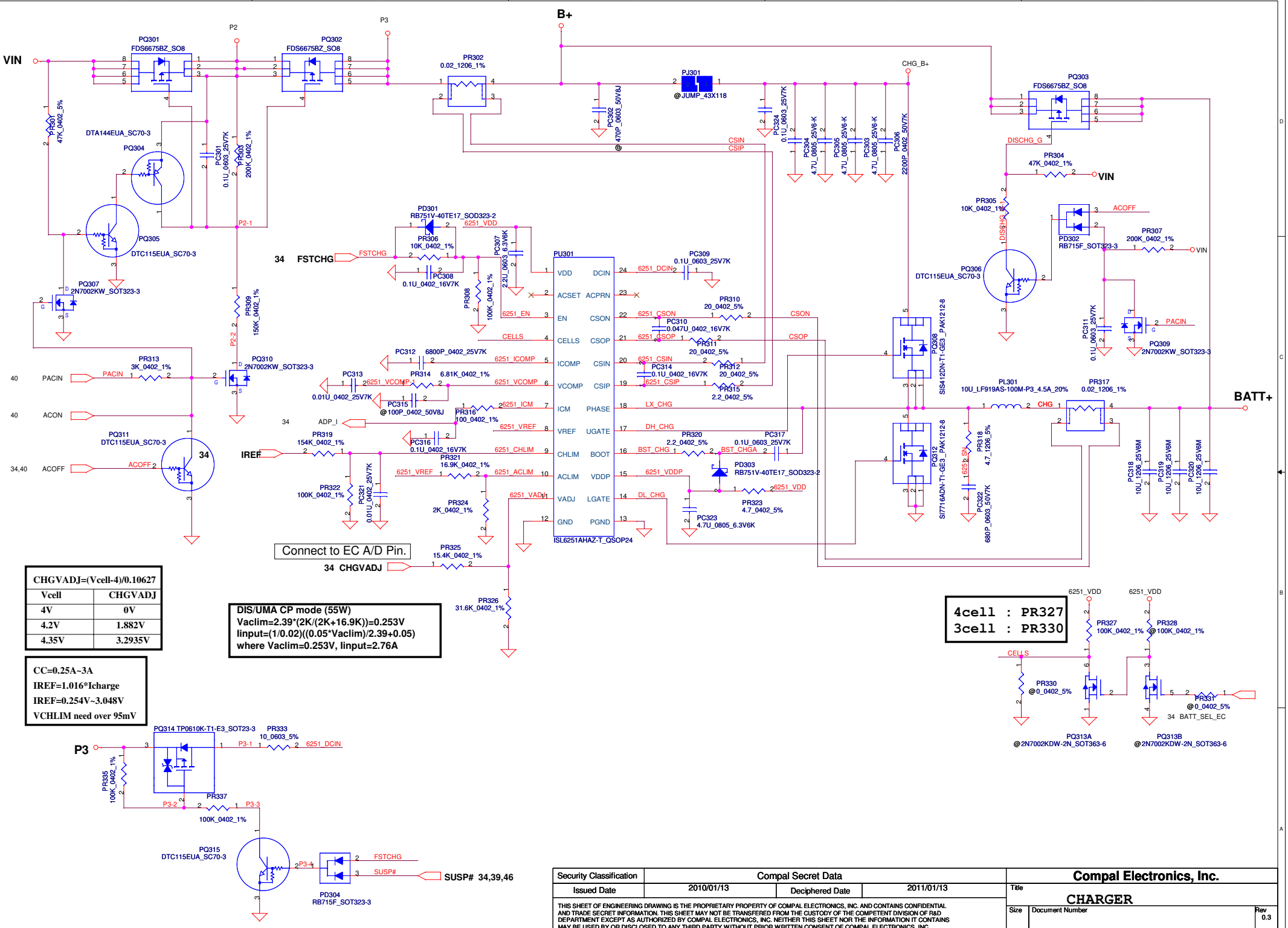
Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: BATTERY CONN / OTP

Size	Document Number	Rev
		0.3

Date: Thursday, April 08, 2010 | Sheet 41 of 50



CHGVADJ=(Vcell-4)/0.10627	
Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

CC=0.25A~3A
IREF=1.016*Icharge
IREF=0.254V~3.048V
VCHLIM need over 95mV

DIS/UMA CP mode (55W)
Vaclim=2.39*(2K/(2K+16.9K))=0.253V
Iinput=(1/0.02)((0.05*Vaclim)/2.39+0.05)
where Vaclim=0.253V, Iinput=2.76A

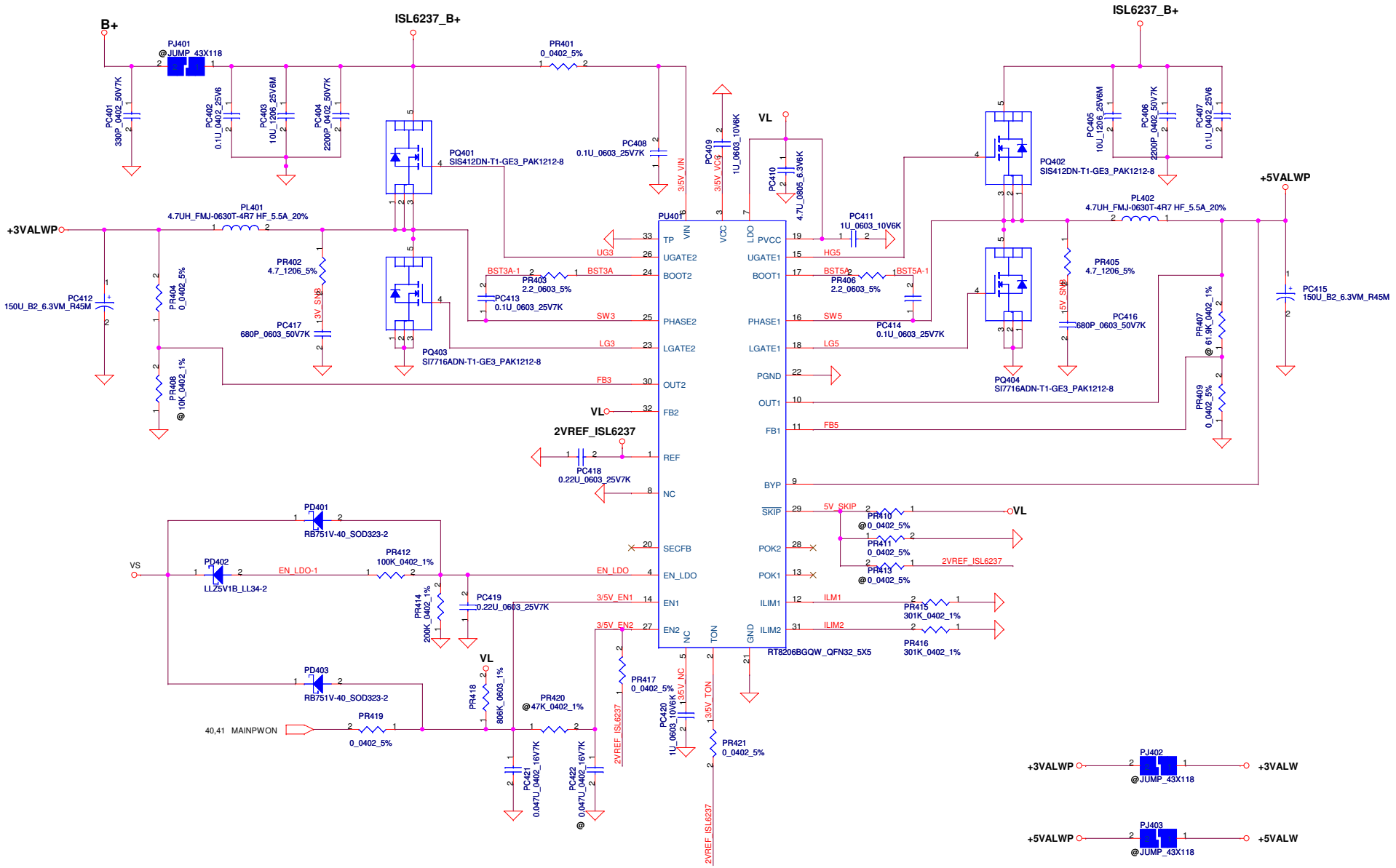
Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: CHARGER

Size	Document Number	Rev
		0.3

Date: Thursday, April 08, 2010 | Sheet 42 of 50



Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: 3VALW/5VALW

Size	Document Number	Rev
Custom		0.3

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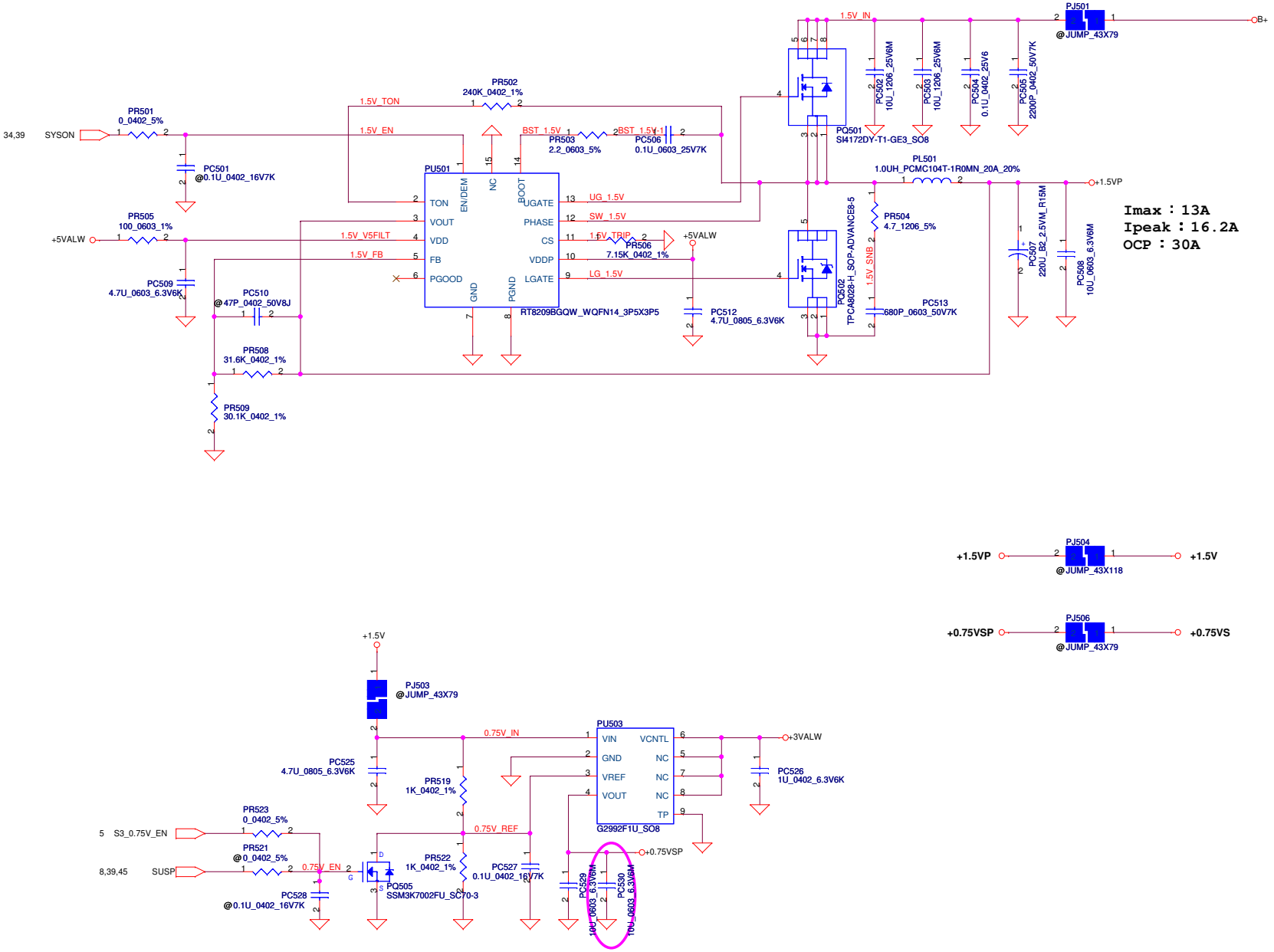


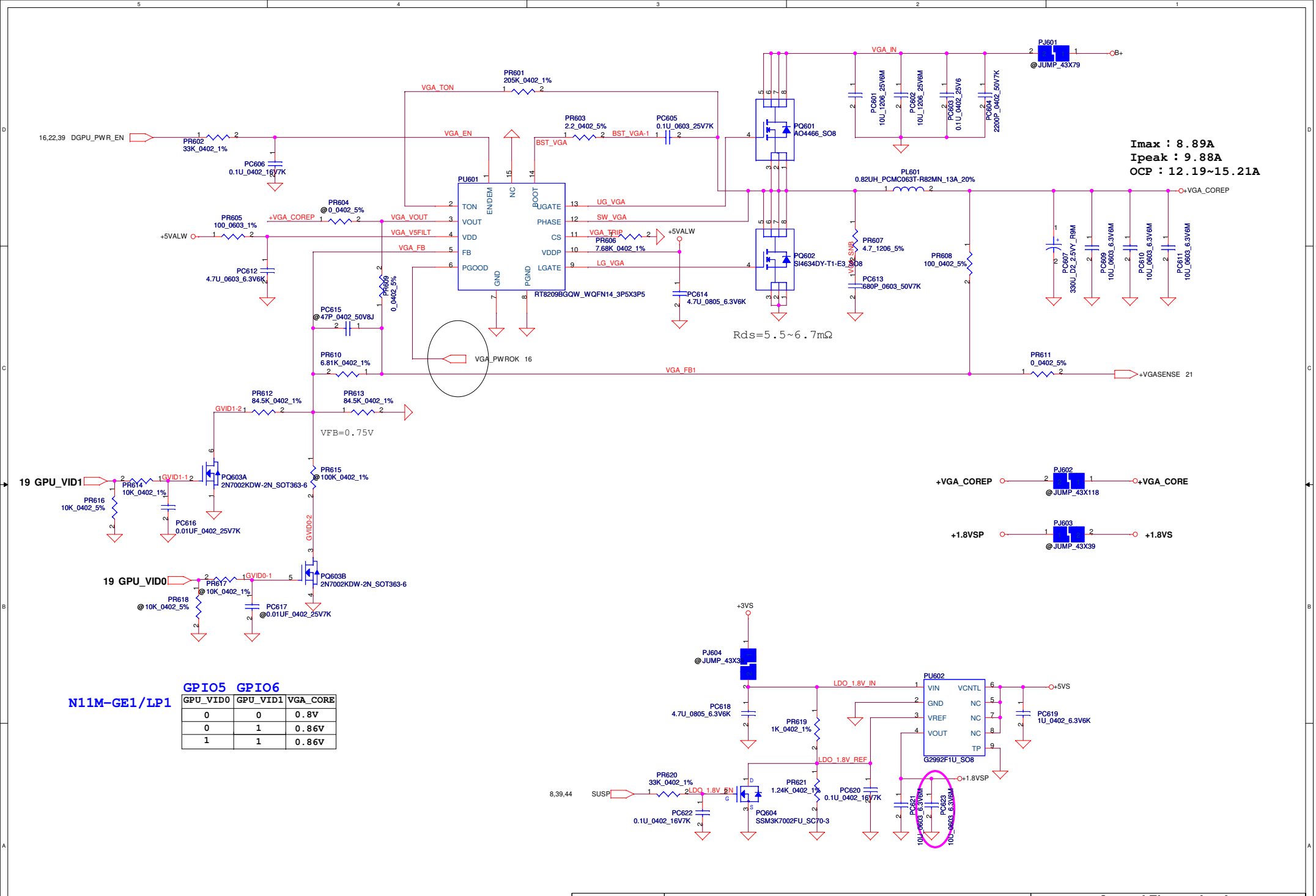
Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: 1.5V/0.75VS

Size	Document Number	Rev
		0.3

Date: Thursday, April 08, 2010 | Sheet 44 of 50



N11M-GE1/LP1

GPIO5 GPIO6

GPU_VID0	GPU_VID1	VGA_CORE
0	0	0.8V
0	1	0.86V
1	1	0.86V

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.

Title: VGA_CORE/1.8VS/1.1VS

Size	Document Number	Rev
		0.3

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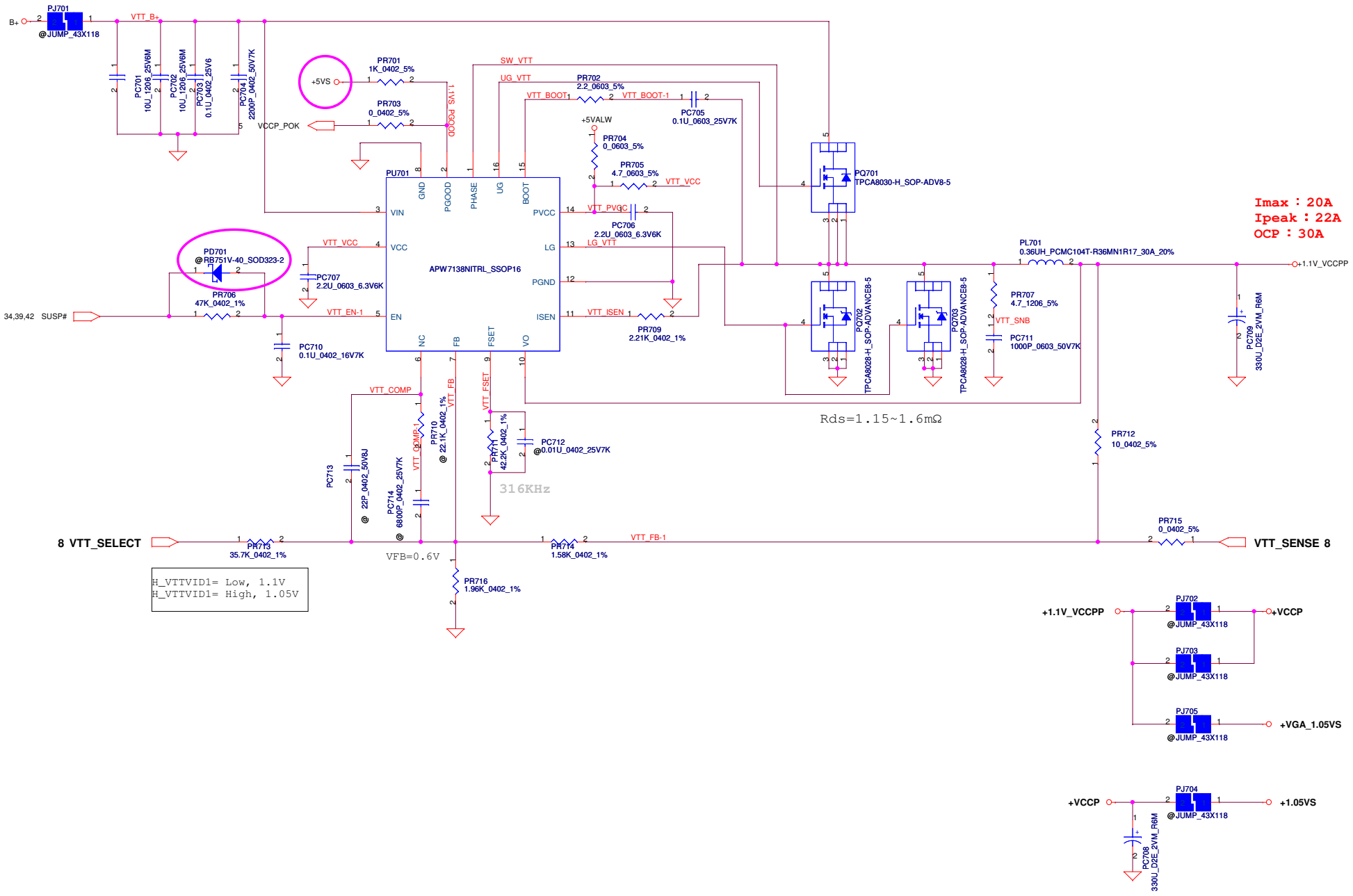

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

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Title: +1.1VS_VTT

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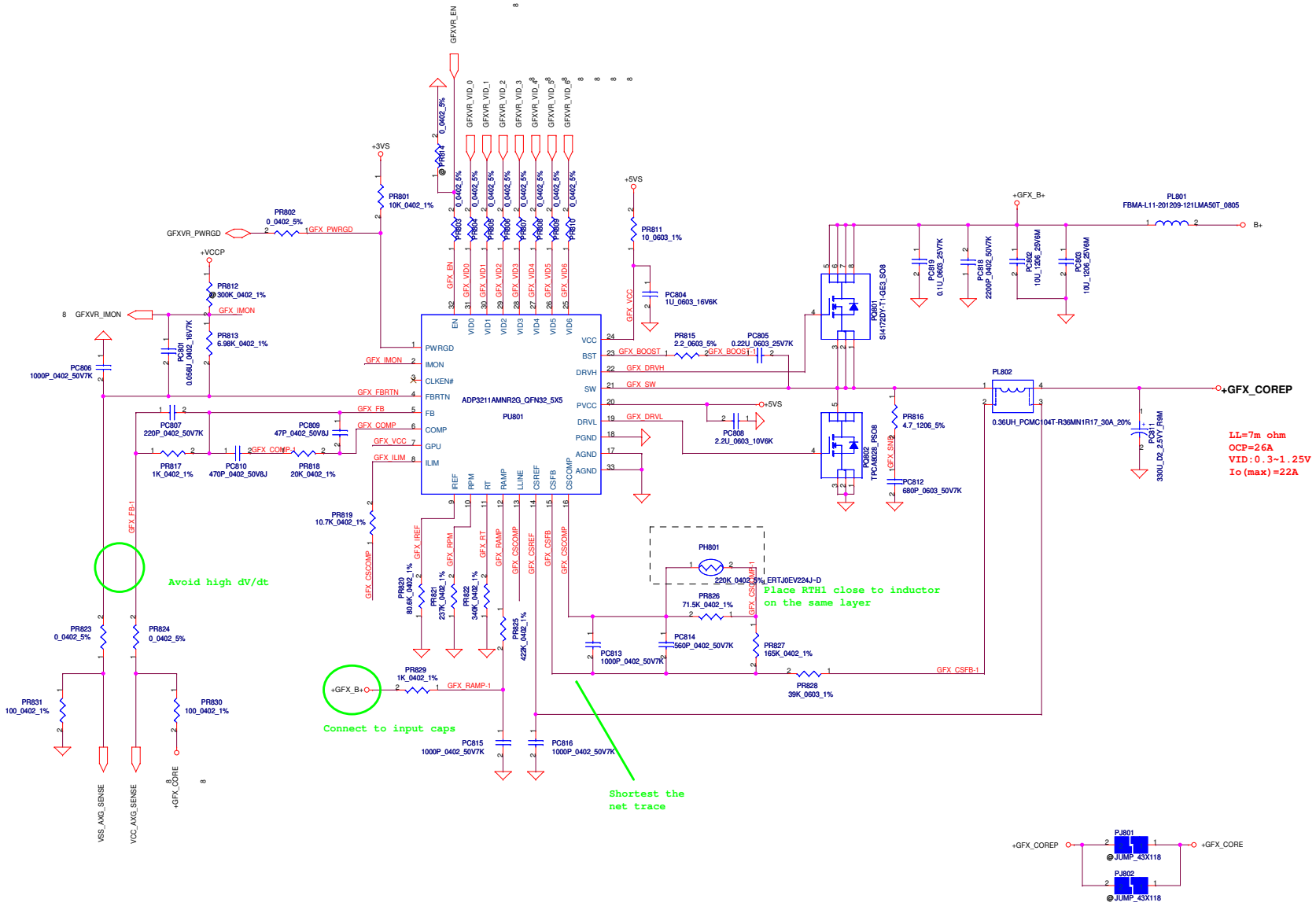

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

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Title: **GFX_CORE**

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	HFM_VID	HFM_Icc	LL	Icc_TDC	Icc_Dyn
Auburndale 45W	0.85	50	1.9m	37	35
Auburndale 35W	0.85	38	1.9m	29	27
Clarksfield SV	0.95	52	1.9m	38	39
Clarksfield XE	0.95	65	TBD	48	TBD

PH0	PH1	# of PH
0	0	1
0	1	2
1	1	3

ADP3212MNR2G_QFN48_7X7

Layout note: Boost Parts close

Close IC

Layout note: Boost Parts close

Avoid high dV/dt

Connect to input caps

Layout note: Close to PHASE 1 inductor on the same layer

Layout note: Close Phase 1 MOS

Shortest the net trace

0603 package at least

Layout note: Close CPU pin

DCR=1.1mΩ ±7%

DCR=1.1mΩ ±7%

LL=1.9m ohm
OCP=60A
VID:0.8~0.85V
Io(max)=48A

Auburndale SV: VID(0-5):001001
ULV: VID(0-5):001010

Security Classification	Compal Secret Data		
Issued Date	2010/01/13	Deciphered Date	2011/01/13

Compal Electronics, Inc.			
Title	CPU_CORE		
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Version change list (P.I.R. List)

for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1	Add S3_0.75V_EN for 0.75 enable singal	44	Add PR523 and reserve PR521	11/09	Before A
2	Modify VGA GPIO table for NVIDIA SPEC.	45	Reserve PR615, PR617, PR618 and PC617 PR612, PR613 change to 84.5K from 100K	11/09	Before A
3					
4					
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17				20081022	

Compal Electronics, Inc.

Title: PIR (PWR)

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NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
				VER. R0_1030
1		30	RJ45 CONNECTOR	
2		35	KB Matrix change	
3		31	EMC1403-1 change to EMC1403-2	
4		40,42	POWER modify PQ313,PU102	
5			change USB port	FP : port10
6				USB3 : port 9
7			change USB power	
		1102D MODIFY		
8		33	Add RA7,CA13	FOR ESD
9		35	Add D22	
10		38	JFIR CONN. CHANGE TO 12 PIN	
11		36	CHANGE NET NAME	
12		27	JLVDS1 CONN. PIN SWAP.	
13		13	DEL CLRP1	
14		1104DMODIFY		
15		16	Add U15,R173,R177,R178,R627,R628	
16		1105DMODIFY		
17		28	Add Q44,Q45,Q49,Q55,Q60,Q62,R336	
18		26	Add Q61,Q63	
19		29	R726 change to 0805	
20		25	Add R559	
21		15	Add R180	
22		14	Add T24 PAD,T25 PAD	
23		8	Add R282	
24		14	Add R327,R325,T21 PAD	
		1109DMODIFY		
25		14	Del R81,R83	
26		16	Add T26 PAD,C687	
27		27	Add R371,R372	
28		34	Del Q26,R303 T21PAD	
			Add R230,Q17	
29		26	Del Q61,Q63 Add Q99A,Q99B	
		5	Add Q61,R416	
			JFIR CONN change JLED CONN	
		34	add TP29,R320,R328,R230	

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	MP	15	Add R687,R688	Intel DG
2	MP	39	Add R5, Del R4	S5 power lost

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	PVT	24	HDMI connector change to DIP type	DFB request
2	PVT	28	R336 change to 100Kohm	BOM error
3	PVT	38	D13,D14 change to panjit	cost down
4	PVT	38	RG4,RG5 chagne 56k ohm	RC filter for G-sensor output, EC request.
5	PVT	37	JBT1 change to 6 pin	For 6 pin BT module
6	PVT	34	SUSCLK connect to clock out	EC issued change note.
7	PVT	34	R978 45 to 0 ohm	For ECROM can't flash
8	PVT	34	Add Q63 2N7002, R344 10K	USB Power pulse when AC in, bug
9	PVT	34	Add net CLKRUN# on pin38	reserve for power saving
10	PVT	34	32.768KHz change to 70x15x1.4	cost down
11	PVT	13	32.768KHz change to 70x15x1.4	cost down
12	PVT	33	INT_MIC_CLK add CA18 100pF cap.	EMI request
13	PVT	33	Audio pin4 add D7	Realtek change note for bug
14	PVT	28	Add Q45 2N7002	For Wimax LED no function, bug
15	PVT	27	change U42 to ST	cost down
16	PVT	27	Add Q64,Q37,R440	cost down, enable bkl circuit
17	PVT	26	Add R322,R328 0 ohm	For "non-PnP device" bug
18	PVT	22	Add R474 34.8K ohm	N-vidia N11M-LP1 device ID
19	PVT	19	L7,L8,L17,L18 change to 0 ohm	for EDID can't detect sometime, cost down
20	PVT	17	R208 change to 1 ohm	CRT garbege in uma mode
21	PVT	16	R580 add 0 ohm	for bug, uma switch to dis will hang up
22	PVT	15	R175 2.2k to 4.7k ohm	common design update
23	PVT	12	Y1 14.318MHz change to 5032 size	common design
24	PVT	09	C75,C76,C92,C164 change to 333uF 6m ohm	cost down
25	PVT	X	Q4,QG1,Q32,Q33,Q73,Q74,Q75,Q97 change to AO3413	cost down
26	PVT	34	Add R345 10Kohm	EC_TACH pull up

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	SVT	39	Add R568, Q40	+0.75VS discharge
2	SVT	39	Add R673 10K	+1.5V EN pin pull down
3	SVT	39	Change U33 to Low Rds-on type	VRAM voltage drop
4	SVT	37	Add EMI common chock on USB p1,p0;L38,L39	EMI
5	SVT	34	CLKRUN# pull down, R671 10K	common design
6	SVT	34	Reserve R685 for WLAN_LED by EC control	WLAN LED
7	SVT	33	ALC259 change to VB	Version change
8	SVT	29	del R654 leakage	leakage
9	SVT	28	WLAN LED control change to DTL AND gate	For some card design
10	SVT	27	Add U6,U17,U18,U19 for BKL and PWM control	signal select switch
11	SVT	27	Add R370 680ohm	support No color engine panel
12	SVT	27	Add D36	LCEVDD discharge
13	SVT	26	Reserve CRT double pi filter	Vidio Filter
14	SVT	25	Add R670 2.2K	HDMI common design
15	SVT	15,25	Add R675,R674 100K	Hybrid mode disable PCH HDMI
16	SVT	17	C505,C492 change size 0603	ME demend
17	SVT	17	C447 change to 1uF	common design
18	SVT	13	Add R677	HDA SDIN1
19	SVT	8	Change R268 to 47K	timing
20	SVT	8	Add R551 1K	PSI# pull down, strip pin
21	SVT	5	C338 change to 0.047uF	common design, S3 shutdown
22	SVT	5	R135 remove	warm boot issue
23	SVT	12	Add C365	10pF for RF
24	SVT	14	Add R413,C439 22ohm,10pF	For RF

Title
HW PIR

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A3	LA-5941P	0.3

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