



Part Number = DA8000FB20

Compal confidential

Schematics Document

Mobile Penryn ULV singal/dual
core with Intel
Cantiga_GS45/GS40 +ICH9-M SFF
core logic

ULV core logic board

2009-07-23

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				Sheet	1 of 30
				Rev	2.0

电脑维修网
<http://www.dnfix.cn/bbs>
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 技术支持: 252670528

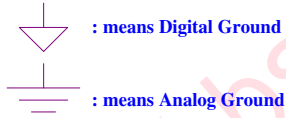
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Voltage Rails

(O MEANS ON X MEANS OFF)

power plane State	+B +3VL	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +0.75V +VCCP +CPU_CORE
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

Symbol Note :



@ : means just reserve , no build
 CONN@ : means ME part.
 45@ : means install after SMT.

SMBUS Control Table

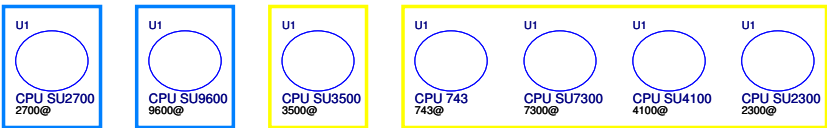
	SOURCE	INVERTER	BATT	SERIAL EEPROM	THERMAL SENSOR (CPU)	SODIMM	CLK CHIP	MINI CARD	LCD
SMB_EC_CK1 SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X
SMB_CK_CLK1 SMB_CK_DAT1	ICH9	X	X	X	X	V	V	V	X
LCD_CLK LCD_DAT	Cantiga	X	X	X	X	X	X	X	V

	Descreption		Descreption		Descreption
USB port 0	USB connector	PCI-e port 0		SATA port 0	SATA HDD
USB port 1	BT Module	PCI-e port 1	WLAN Conn.	SATA port 1	
USB port 2	cardreader	PCI-e port 2		SATA port 2	WWAN/SSD
USB port 3	USB connector	PCI-e port 3			
USB port 4	WLAN Conn.	PCI-e port 4			
USB port 5	WWAN/SSD	PCI-e port 5	LAN		
USB port 6	USB connector				
USB port 7	CMOS				
USB port 8	Fingerprint				

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	10100000
CLOCK GENERATOR (EXT.)	D2	11010010

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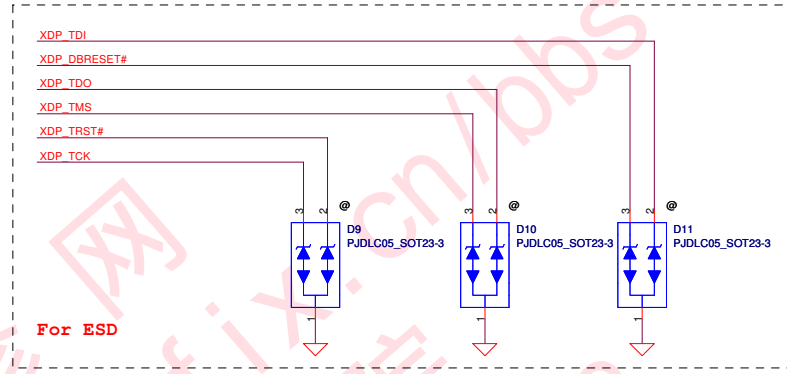
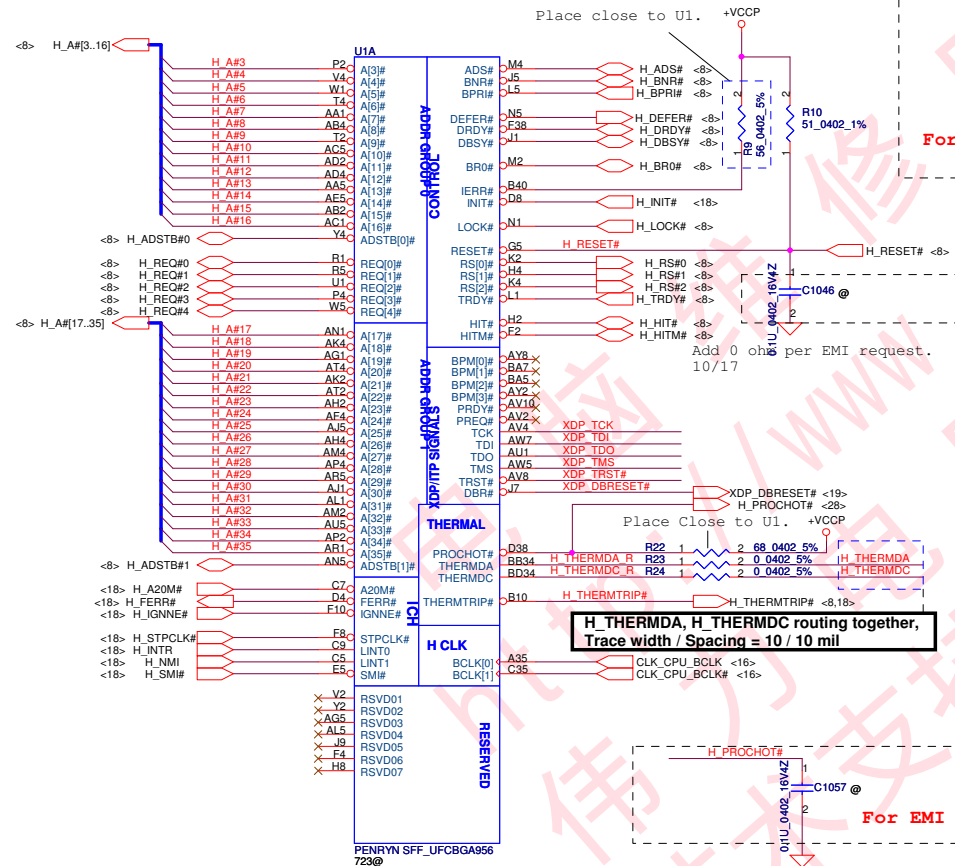
07/06 Add U1 SA00003BZ10 for 3500@

07/23 Add U1 SA00003IA50 for 7300@

Add U1 SA00003I950 for 4100@

Add U1 SA00003H060 for 2300@

Add U1 SA00003JO60 for 743@



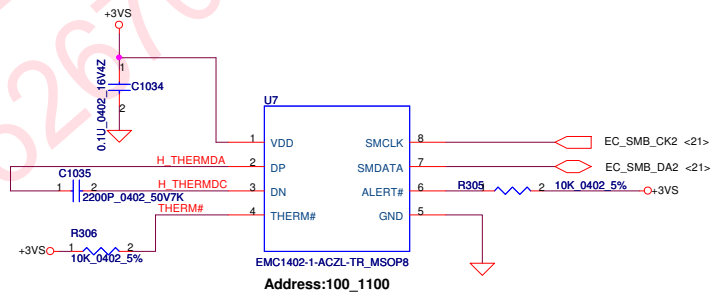
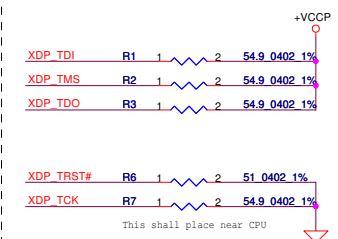
For ESD

For ESD

Add 0 ohm per EMI request.
10/17

H_THERMDA, H_THERMDC routing together,
Trace width / Spacing = 10 / 10 mil

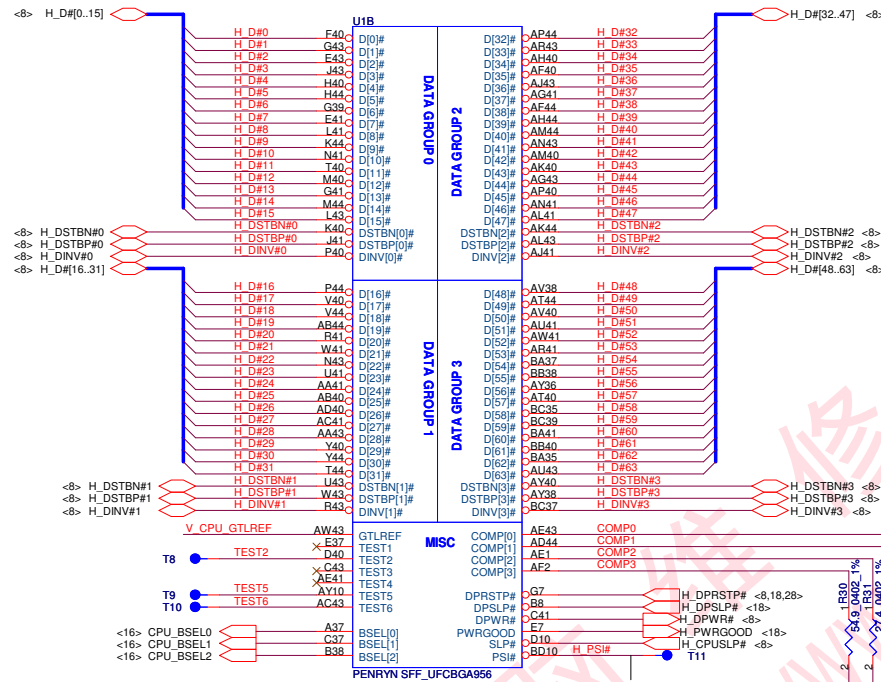
For EMI



Address:100_1100

07/06 Change U1 from SA000038J40 to SA000038J60

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Title	Penryn(1/3)-AGTL+/ITP-XDP			
Size	Document Number	LS-5581P		Rev
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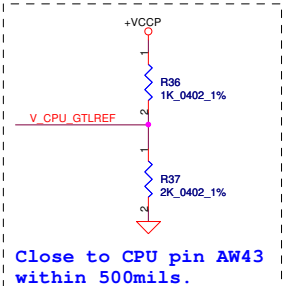


layout note: Route TEST3 & TEST5 traces on ground referenced layer to the TPs

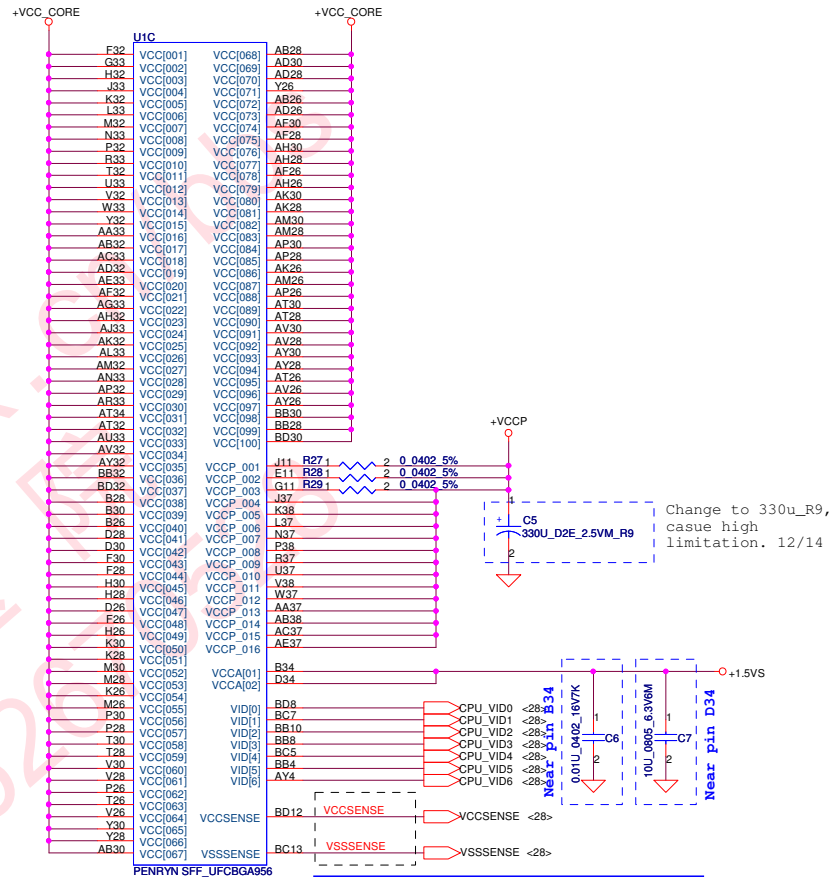
CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0
266	0	0	0

Cause CPU core power change to 1 phase, and not need support the pin, leave it as TP. 10/02

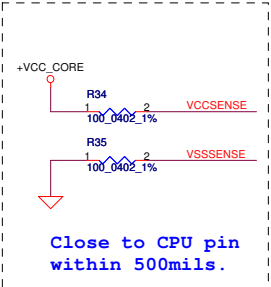
Resistor placed within 0.5" of CPU pin. Trace should be at least 25 mils away from any other toggling signal. COMP [0, 2] trace width is 18 mils. COMP [1, 3] trace width is 4 mils.



Close to CPU pin AW43 within 500mils.



Length match within 25 mils. The trace width/space/other is 20/7/25.

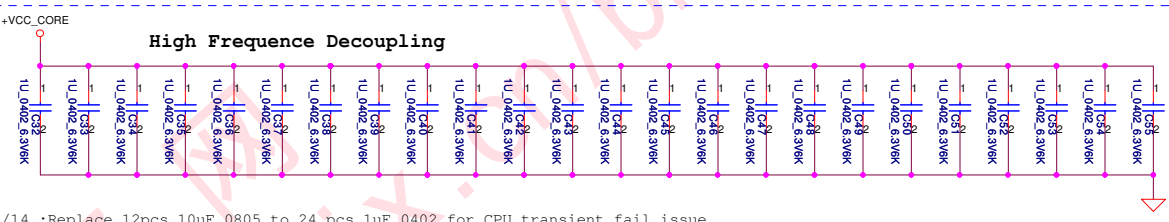
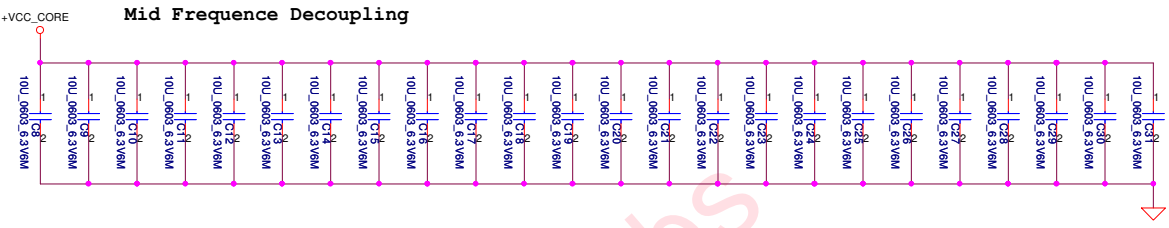


Close to CPU pin within 500mils.

UID		
B42	VSS001	VSS082
F44	VSS002	VSS083
D44	VSS003	VSS084
F42	VSS005	VSS086
H42	VSS006	VSS087
K42	VSS007	VSS088
M42	VSS008	VSS089
P42	VSS009	VSS090
T42	VSS010	VSS091
Y42	VSS011	VSS092
AB42	VSS012	VSS093
AD42	VSS014	VSS095
AF42	VSS015	VSS096
AH42	VSS016	VSS097
AK42	VSS017	VSS098
AM42	VSS018	VSS099
AV44	VSS019	VSS100
AW44	VSS020	VSS101
AX42	VSS022	VSS103
BA43	VSS024	VSS105
BB42	VSS026	VSS107
CB3	VSS027	VSS108
G37	VSS028	VSS109
H38	VSS030	VSS111
J39	VSS031	VSS112
L39	VSS032	VSS113
M38	VSS033	VSS114
N39	VSS034	VSS115
P39	VSS035	VSS116
T38	VSS036	VSS117
U39	VSS037	VSS118
W39	VSS038	VSS119
X38	VSS039	VSS120
AA39	VSS040	VSS121
AD38	VSS041	VSS122
AE39	VSS043	VSS124
AG38	VSS044	VSS125
AH38	VSS045	VSS126
AJ39	VSS047	VSS128
AM38	VSS048	VSS129
AN39	VSS049	VSS130
AR39	VSS050	VSS131
AT38	VSS051	VSS132
AU39	VSS052	VSS133
AW37	VSS053	VSS134
AX39	VSS054	VSS135
AW39	VSS055	VSS136
AW37	VSS056	VSS137
BA39	VSS057	VSS138
BC41	VSS058	VSS139
BD40	VSS059	VSS140
BD38	VSS060	VSS141
B36	VSS061	VSS142
H34	VSS062	VSS143
D36	VSS063	VSS144
K34	VSS064	VSS145
M34	VSS065	VSS146
M36	VSS066	VSS147
P34	VSS067	VSS148
T34	VSS068	VSS149
Y34	VSS069	VSS150
T36	VSS070	VSS151
V34	VSS071	VSS152
AB34	VSS072	VSS153
AD34	VSS073	VSS154
AD36	VSS074	VSS155
AF34	VSS075	VSS156
AH34	VSS076	VSS157
AH36	VSS077	VSS158
AK34	VSS078	VSS159
AM34	VSS079	VSS160
AP34	VSS080	VSS161
	VSS081	VSS162
		VSS163

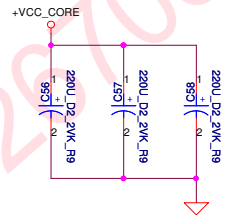
UIE		
G25	VSS 164	VSS 280
G21	VSS 165	VSS 281
J25	VSS 166	VSS 282
J23	VSS 167	VSS 283
J21	VSS 168	VSS 284
L23	VSS 169	VSS 285
L21	VSS 170	VSS 286
N25	VSS 171	VSS 287
N23	VSS 172	VSS 288
N21	VSS 173	VSS 289
R25	VSS 174	VSS 290
R23	VSS 175	VSS 291
R21	VSS 176	VSS 292
U25	VSS 177	VSS 293
U23	VSS 178	VSS 294
U21	VSS 179	VSS 295
W25	VSS 180	VSS 296
W23	VSS 181	VSS 297
W21	VSS 182	VSS 298
AA25	VSS 183	VSS 299
AA23	VSS 184	VSS 300
AA21	VSS 185	VSS 301
AC25	VSS 186	VSS 302
AC23	VSS 187	VSS 303
AC21	VSS 188	VSS 304
AD25	VSS 189	VSS 305
AD23	VSS 190	VSS 306
AD21	VSS 191	VSS 307
AE25	VSS 192	VSS 308
AE23	VSS 193	VSS 309
AE21	VSS 194	VSS 310
AG25	VSS 195	VSS 311
AG23	VSS 196	VSS 312
AG21	VSS 197	VSS 313
AJ25	VSS 198	VSS 314
AJ23	VSS 199	VSS 315
AJ21	VSS 200	VSS 316
AL25	VSS 201	VSS 317
AL23	VSS 202	VSS 318
AL21	VSS 203	VSS 319
AN25	VSS 204	VSS 320
AN23	VSS 205	VSS 321
AN21	VSS 206	VSS 322
AR25	VSS 207	VSS 323
AR23	VSS 208	VSS 324
AR21	VSS 209	VSS 325
AU25	VSS 210	VSS 326
AU23	VSS 211	VSS 327
AU21	VSS 212	VSS 328
AW25	VSS 213	VSS 329
AW23	VSS 214	VSS 330
AW21	VSS 215	VSS 331
BA25	VSS 216	VSS 332
BA23	VSS 217	VSS 333
BA21	VSS 218	VSS 334
BC25	VSS 219	VSS 335
BC23	VSS 220	VSS 336
BC21	VSS 221	VSS 337
C17	VSS 222	VSS 338
C19	VSS 223	VSS 339
E19	VSS 224	VSS 340
E17	VSS 225	VSS 341
G19	VSS 226	VSS 342
G17	VSS 227	VSS 343
J19	VSS 228	VSS 344
J17	VSS 229	VSS 345
L19	VSS 230	VSS 346
L17	VSS 231	VSS 347
N19	VSS 232	VSS 348
N17	VSS 233	VSS 349
R19	VSS 234	VSS 350
R17	VSS 235	VSS 351
U19	VSS 236	VSS 352
U17	VSS 237	VSS 353
W19	VSS 238	VSS 354
W17	VSS 239	VSS 355
AA19	VSS 240	VSS 356
AA17	VSS 241	VSS 357
AC19	VSS 242	VSS 358
AC17	VSS 243	VSS 359
AE19	VSS 244	VSS 360
AE17	VSS 245	VSS 361
AG19	VSS 246	VSS 362
AG17	VSS 247	VSS 363
AJ19	VSS 248	VSS 364
AJ17	VSS 249	VSS 365
AL19	VSS 250	VSS 366
AL17	VSS 251	VSS 367
AN19	VSS 252	VSS 368
AN17	VSS 253	VSS 369
AR19	VSS 254	VSS 370
AR17	VSS 255	VSS 371
AU19	VSS 256	VSS 372
AU17	VSS 257	VSS 373
AW19	VSS 258	VSS 374
AW17	VSS 259	VSS 375
BA19	VSS 260	VSS 376
BA17	VSS 261	VSS 377
BC19	VSS 262	VSS 378
BC17	VSS 263	VSS 379
C11	VSS 264	VSS 380
C15	VSS 265	VSS 381
E15	VSS 266	VSS 382
G15	VSS 267	VSS 383
H10	VSS 268	VSS 384
M12	VSS 269	VSS 385
M15	VSS 270	VSS 386
J15	VSS 271	VSS 387
N15	VSS 272	VSS 388
M10	VSS 273	VSS 389
T12	VSS 274	VSS 390
R15	VSS 275	VSS 391
U15	VSS 276	VSS 392
W15	VSS 277	VSS 393
T10	VSS 278	VSS 394
Y12	VSS 279	VSS 395
AD12		

PENRYN SFF_UFCBG956

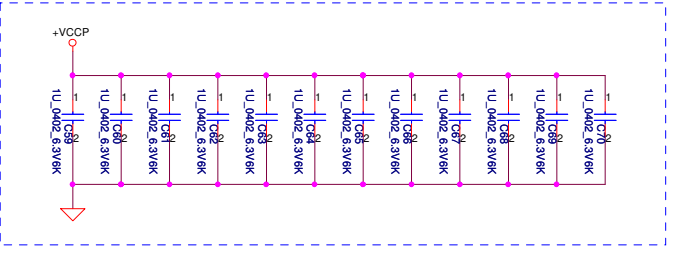


6/14 :Replace 12pcs 10uF_0805 to 24 pcs 1uF_0402 for CPU transient fail issue.

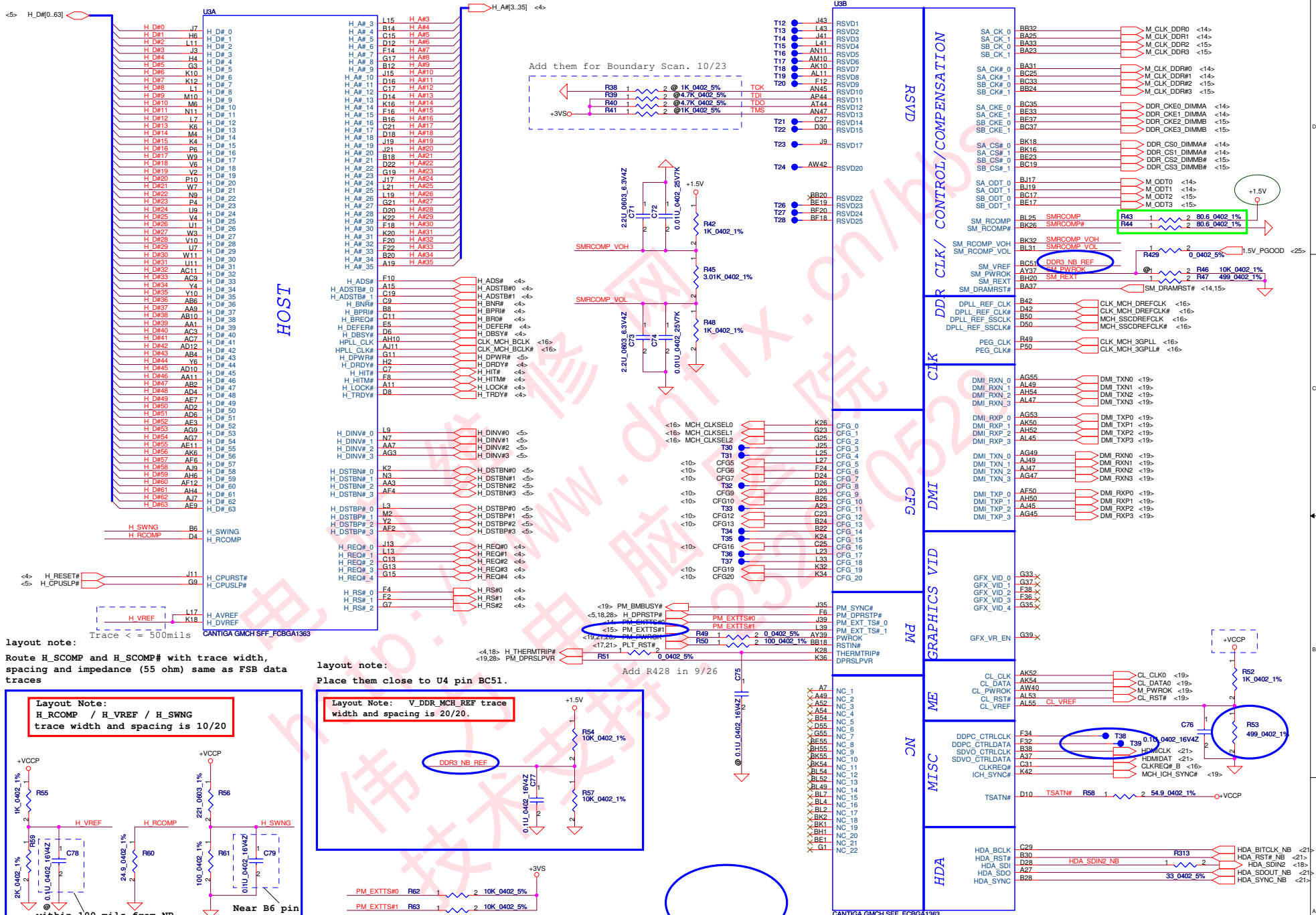
ESR <= 1.5m ohm
Near CPU CORE regulator



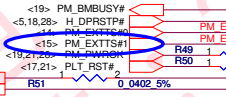
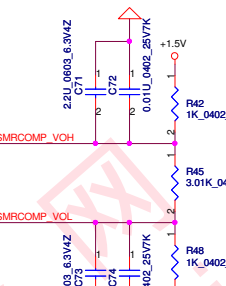
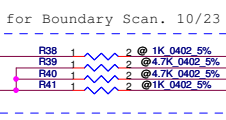
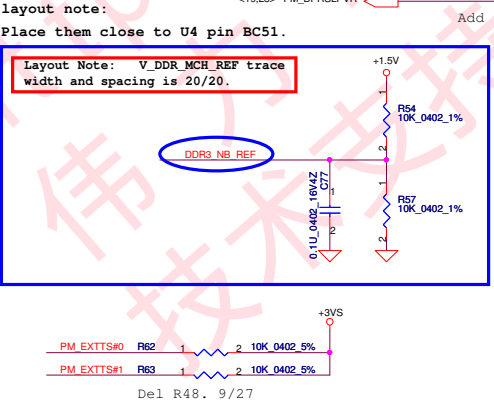
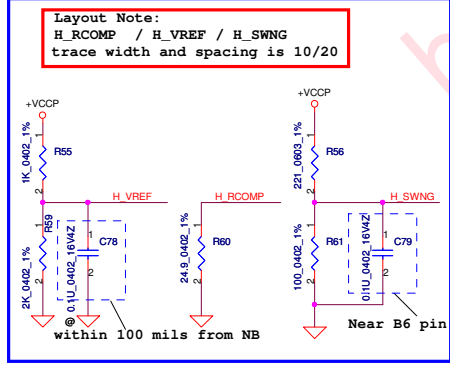
Del C37 to improve power plan. 6/14



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layout note: Trace <= 500mils
 Route H_SCOMP and H_SCOMP# with trace width, spacing and impedance (55 ohm) same as FSB data traces

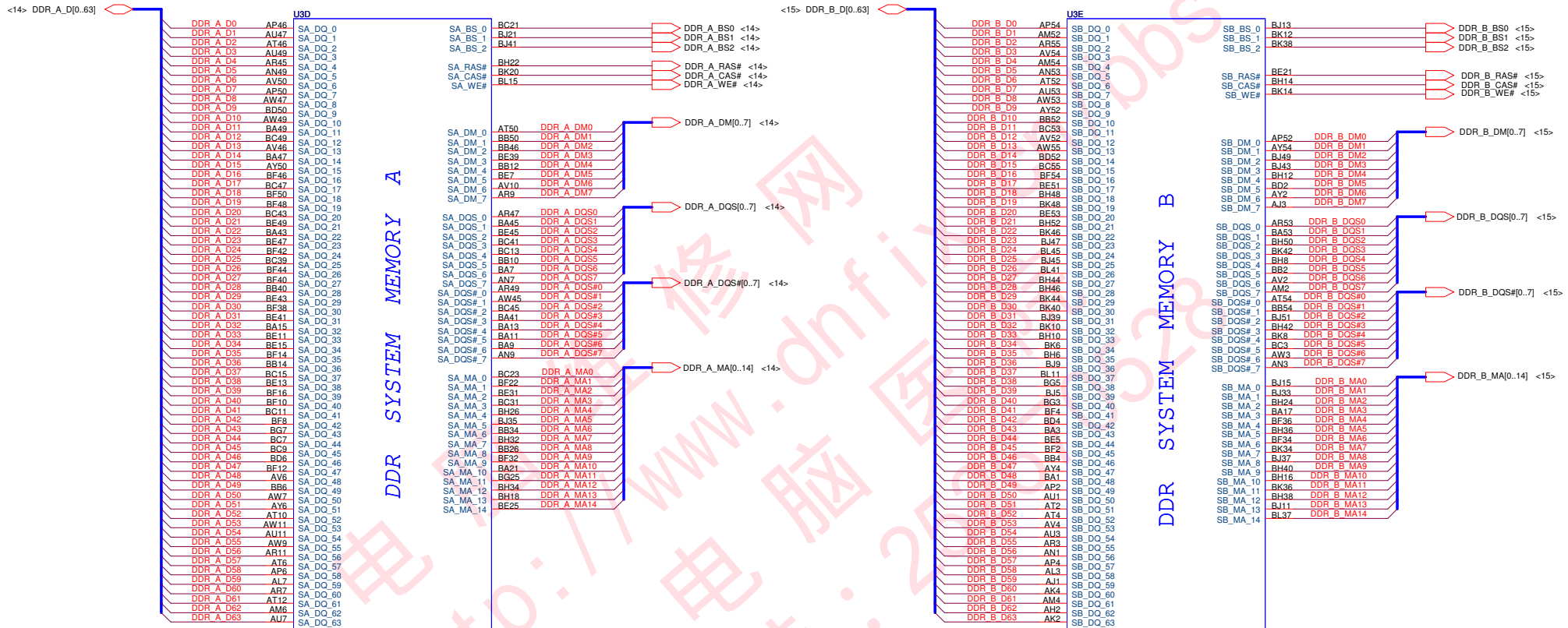


Add R428 in 9/26

Del R48. 9/27

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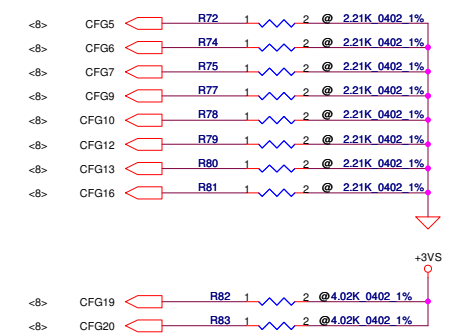
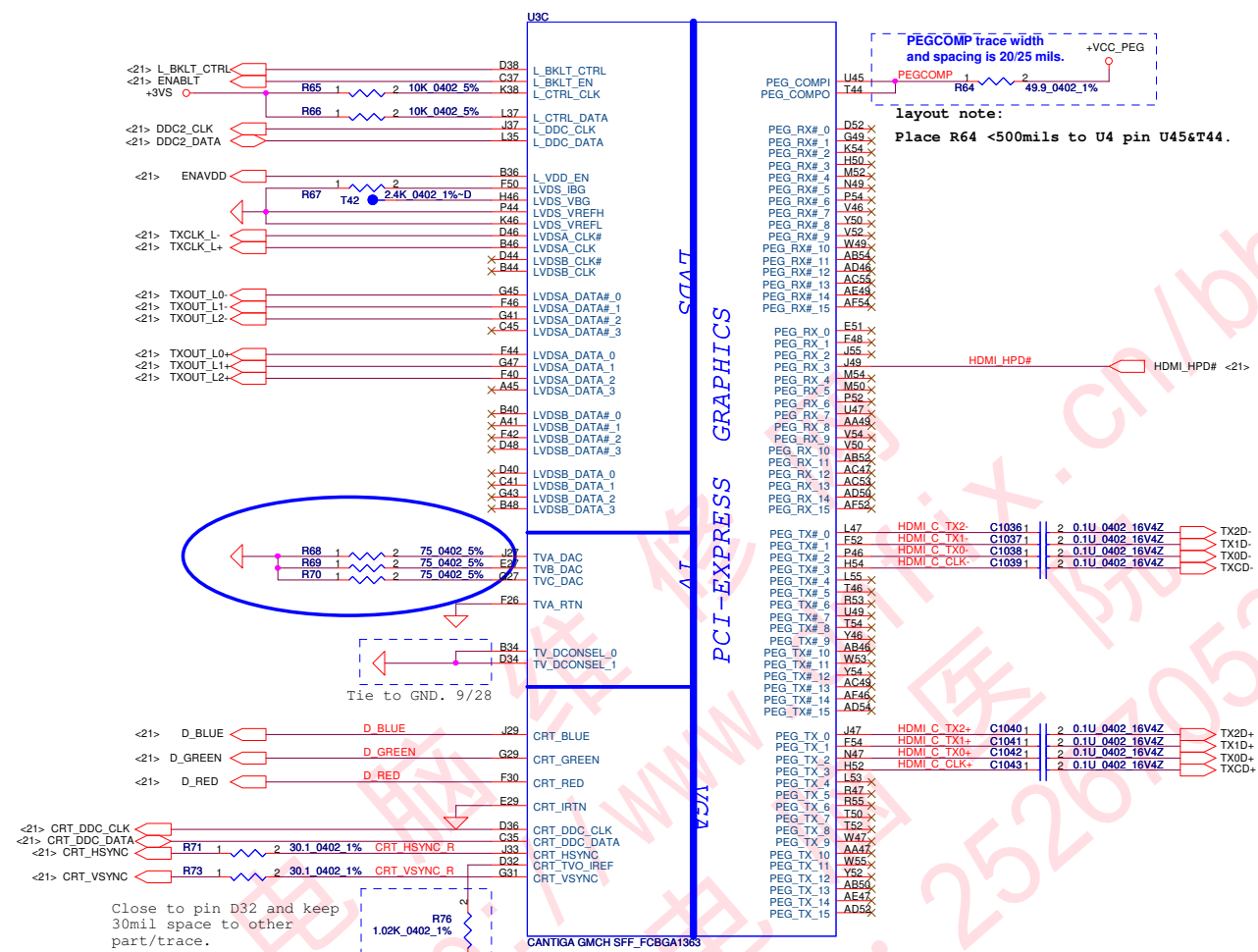
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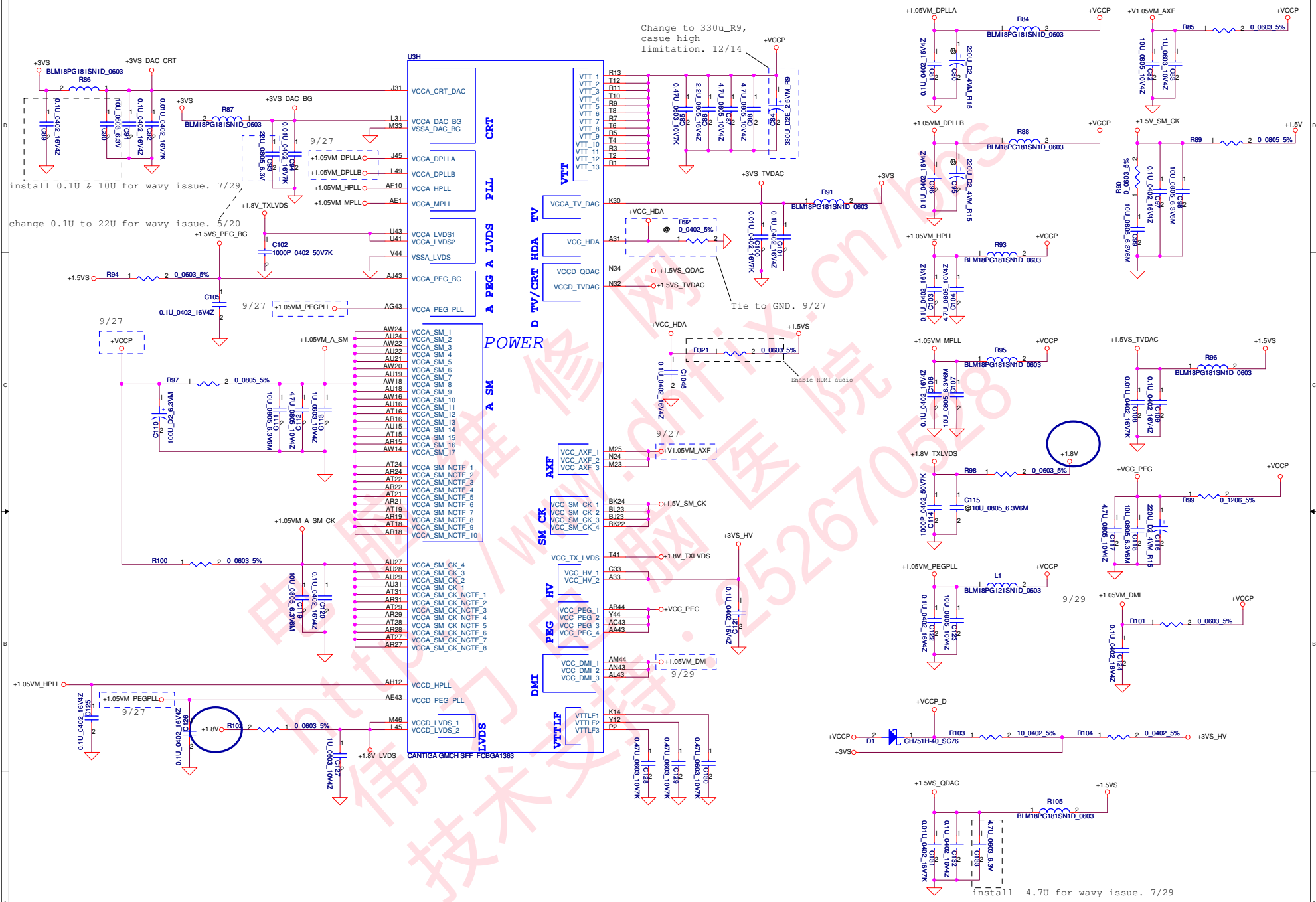
CANTIGA GMCH SFF_FCBGA1363

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Strap Pin Table

CFG[2:0] FSB Freq select	000 = FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz Others = Reserved
CFG[4:3]	Reserved
CFG5 (DMI select)	0 = DMI x 2 1 = DMI x 4 *
CFG6	0 = The iTPM Host Interface is enable 1 = The iTPM Host Interface is disable *
CFG7 (Intel Management Engine Crypto strap)	0 = (TLS)chiper suite with no confidentiality 1 = (TLS)chiper suite with confidentiality *
CFG8	Reserved
CFG9 (PCIe Graphics Lane Reversal)	0 = Reverse Lane, 15->0, 14->1 1 = Normal Operation, Lane Number in order *
CFG10 (PCIe Lookback enable)	0 = Enable 1 = Disable *
CFG11	Reserved
CFG[13:12] (XOR/ALLZ)	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation(Default) *
CFG[15:14]	Reserved
CFG16 (FSB Dynamic ODT)	0 = Disabled 1 = Enabled *
CFG[18:17]	Reserved
CFG19 (DMI Lane Reversal)	0 = Normal Operation * (Lane number in Order) 1 = Reverse Lane
CFG20 (PCIe/SDVO concurrent)	0 = Only PCIe or SDVO is operational. * 1 = PCIe/SDVO are operating simu.



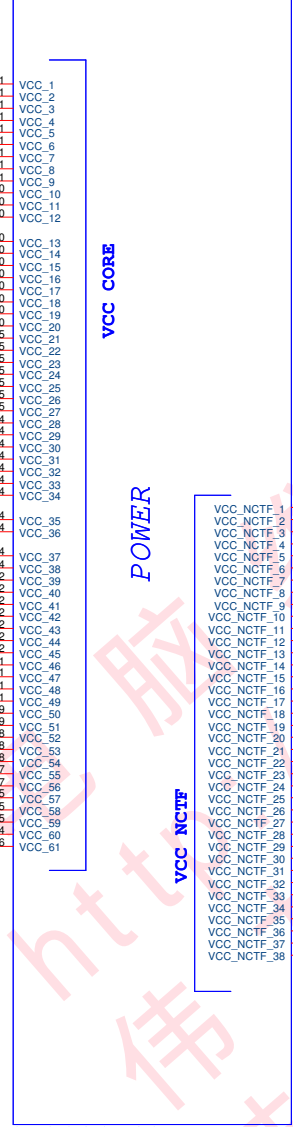
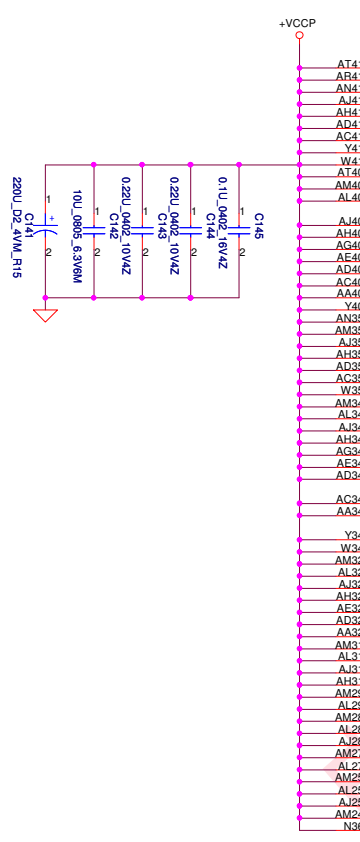


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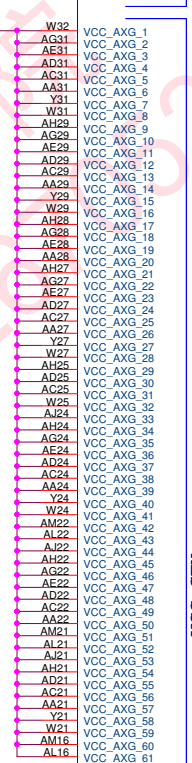
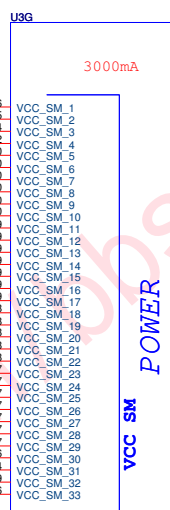
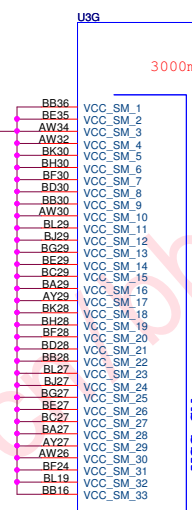
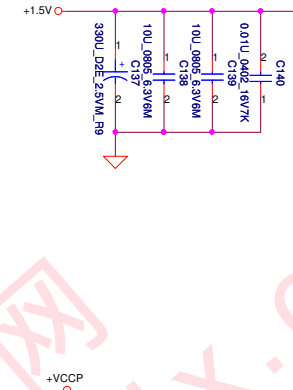
Compal Electronics, Inc.	
Canitiga(4)6-PWR	
Title	LS-551P
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Extenal Graphic: 1210.34mA
 integrated Graphic: 1930.4mA

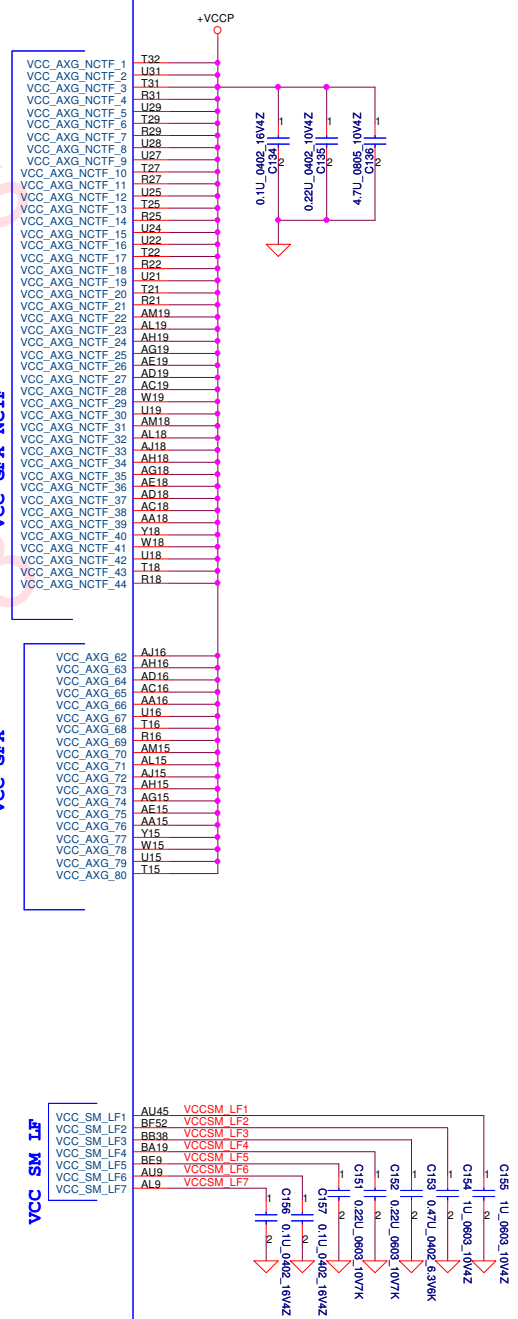
U3F



CANTIGA GMCH SFF_FCBGA1363



CANTIGA GMCH SFF_FCBGA1363



PAD T43 AG13 VCC_AGX_SENSE
 PAD T44 AE13 VSS_AGX_SENSE

Security Classification	Compal Secret Data		2009/02/20	
Issued Date	2006/02/20	Deciphered Date		
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Title Compal Electronics, Inc. Cantiga(5/6)-PWR/GND			Size	Rev
Customer LS-5581P			Document Number	2.0
Date	Tuesday, July 21, 2009	Sheet	12	of 30

U3I		
BA55	VSS_1	VSS_100
AJ55	VSS_2	A43
AN55	VSS_3	VSS_101
AJ55	VSS_4	VSS_102
AE55	VSS_5	VSS_103
AA55	VSS_6	VSS_104
US5	VSS_7	VSS_105
NS5	VSS_8	VSS_106
BD54	VSS_9	VSS_107
BG53	VSS_10	VSS_108
AJ53	VSS_11	VSS_109
AE53	VSS_12	VSS_110
AA53	VSS_13	VSS_111
US3	VSS_14	VSS_112
NS3	VSS_15	VSS_113
JS3	VSS_16	VSS_114
GS3	VSS_17	VSS_115
ES3	VSS_18	VSS_116
KS2	VSS_19	VSS_117
BG51	VSS_20	VSS_118
BA51	VSS_21	VSS_119
AW51	VSS_22	VSS_120
AJ51	VSS_23	VSS_121
AR51	VSS_24	VSS_122
AN51	VSS_25	VSS_123
AL51	VSS_26	VSS_124
AJ51	VSS_27	VSS_125
AG51	VSS_28	VSS_126
AE51	VSS_29	VSS_127
AC51	VSS_30	VSS_128
AA51	VSS_31	VSS_129
WS1	VSS_32	VSS_130
US1	VSS_33	VSS_131
RS1	VSS_34	VSS_132
NS1	VSS_35	VSS_133
LS1	VSS_36	VSS_134
JS1	VSS_37	VSS_135
GS1	VSS_38	VSS_136
CS1	VSS_39	VSS_137
BK50	VSS_40	VSS_138
AM50	VSS_41	VSS_139
K50	VSS_42	VSS_140
BG49	VSS_43	VSS_141
E49	VSS_44	VSS_142
C49	VSS_45	VSS_143
BD48	VSS_46	VSS_144
BB48	VSS_47	VSS_145
AY48	VSS_48	VSS_146
AV48	VSS_49	VSS_147
AT48	VSS_50	VSS_148
AP48	VSS_51	VSS_149
AM48	VSS_52	VSS_150
AK48	VSS_53	VSS_151
AH48	VSS_54	VSS_152
AF48	VSS_55	VSS_153
AD48	VSS_56	VSS_154
AB48	VSS_57	VSS_155
Y48	VSS_58	VSS_156
V48	VSS_59	VSS_157
P48	VSS_60	VSS_158
M48	VSS_61	VSS_159
K48	VSS_62	VSS_160
H48	VSS_63	VSS_161
BL47	VSS_64	VSS_162
BG47	VSS_65	VSS_163
E47	VSS_66	VSS_164
C47	VSS_67	VSS_165
A47	VSS_68	VSS_166
BD46	VSS_69	VSS_167
AY46	VSS_70	VSS_168
AM46	VSS_71	VSS_169
AK46	VSS_72	VSS_170
AH46	VSS_73	VSS_171
BG45	VSS_74	VSS_172
AA45	VSS_75	VSS_173
W45	VSS_76	VSS_174
R45	VSS_77	VSS_175
N45	VSS_78	VSS_176
E45	VSS_79	VSS_177
BD44	VSS_80	VSS_178
BB44	VSS_81	VSS_179
AV44	VSS_82	VSS_180
AK44	VSS_83	VSS_181
AH44	VSS_84	VSS_182
AF44	VSS_85	VSS_183
AD44	VSS_86	VSS_184
K44	VSS_87	VSS_185
H44	VSS_88	VSS_186
BL43	VSS_89	VSS_187
BG43	VSS_90	VSS_188
AY43	VSS_91	VSS_189
AR43	VSS_92	VSS_190
W43	VSS_93	VSS_191
R43	VSS_94	VSS_192
M43	VSS_95	VSS_193
E43	VSS_96	VSS_194
	VSS_97	VSS_195
	VSS_98	VSS_196
	VSS_99	VSS_197
		VSS_198

VSS

U3J		
AN25	VSS_199	VSS_300
AC25	VSS_200	VSS_301
AE25	VSS_201	VSS_302
AA25	VSS_202	VSS_303
Y25	VSS_203	VSS_304
E25	VSS_204	VSS_305
A25	VSS_205	VSS_306
BD24	VSS_206	VSS_307
AN24	VSS_207	VSS_308
AL24	VSS_208	VSS_309
H24	VSS_209	VSS_310
BG23	VSS_210	VSS_311
AY23	VSS_211	VSS_312
F23	VSS_212	VSS_313
BD22	VSS_213	VSS_314
BB22	VSS_214	VSS_315
AN22	VSS_215	VSS_316
Y22	VSS_216	VSS_317
W22	VSS_217	VSS_318
H22	VSS_218	VSS_319
BL21	VSS_219	VSS_320
BG21	VSS_220	VSS_321
AY21	VSS_221	VSS_322
AN21	VSS_222	VSS_323
AG21	VSS_223	VSS_324
AE21	VSS_224	VSS_325
M21	VSS_225	VSS_326
E21	VSS_226	VSS_327
A21	VSS_227	VSS_328
BD20	VSS_228	VSS_329
H20	VSS_229	VSS_330
BG19	VSS_230	VSS_331
AY19	VSS_231	VSS_332
M19	VSS_232	VSS_333
E19	VSS_233	VSS_334
BD18	VSS_234	VSS_335
N18	VSS_235	VSS_336
H18	VSS_236	VSS_337
BL17	VSS_237	VSS_338
BG17	VSS_238	VSS_339
AY17	VSS_239	VSS_340
E17	VSS_240	VSS_341
A17	VSS_241	VSS_342
BD16	VSS_242	VSS_343
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AG16	VSS_244	VSS_345
AE16	VSS_245	VSS_346
Y16	VSS_246	VSS_347
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AY15	VSS_251	VSS_352
M15	VSS_252	VSS_353
E15	VSS_253	VSS_354
A15	VSS_254	VSS_355
BD14	VSS_255	VSS_356
N14	VSS_256	VSS_357
H14	VSS_257	VSS_358
BL13	VSS_258	VSS_359
BG13	VSS_259	VSS_360
AY13	VSS_260	VSS_361
E13	VSS_261	VSS_362
A13	VSS_262	
BD12	VSS_263	
AN12	VSS_264	
AG12	VSS_265	
AE12	VSS_266	
Y12	VSS_267	
W12	VSS_268	
N12	VSS_269	
H12	VSS_270	
BG11	VSS_271	
AY11	VSS_272	
M11	VSS_273	
E11	VSS_274	
A11	VSS_275	
BD10	VSS_276	
N10	VSS_277	
H10	VSS_278	
BL9	VSS_279	
BG9	VSS_280	
AY9	VSS_281	
E9	VSS_282	
A9	VSS_283	
BD8	VSS_284	
N8	VSS_285	
H8	VSS_286	
BL7	VSS_287	
BG7	VSS_288	
AY7	VSS_289	
E7	VSS_290	
A7	VSS_291	
BD6	VSS_292	
N6	VSS_293	
H6	VSS_294	
BL5	VSS_295	
BG5	VSS_296	
AY5	VSS_297	
E5	VSS_298	
A5	VSS_299	

VSS

VSS NCTF

VSS SCB

VSS_NCTF_1	AJ38
VSS_NCTF_2	AH38
VSS_NCTF_3	AD38
VSS_NCTF_4	AC38
VSS_NCTF_5	T35
VSS_NCTF_6	R35
VSS_NCTF_7	AT32
VSS_NCTF_8	AR32
VSS_NCTF_9	U32
VSS_NCTF_10	E32
VSS_NCTF_11	T28
VSS_NCTF_12	B28
VSS_NCTF_13	AT25
VSS_NCTF_14	AR25
VSS_NCTF_15	T24
VSS_NCTF_16	R24
VSS_NCTF_17	AN19
VSS_NCTF_18	AJ19
VSS_NCTF_19	AA19
VSS_NCTF_20	Y19
VSS_NCTF_21	T19
VSS_NCTF_22	R19
VSS_NCTF_23	AN18

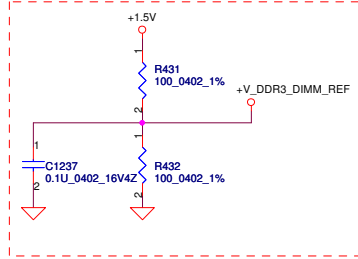
VSS_SCB_1	BL55
VSS_SCB_2	BL1
VSS_SCB_3	D1
VSS_SCB_4	B55
VSS_SCB_5	B2
VSS_SCB_6	A4
VSS_SCB_7	

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CANTIGA GMCH SFF_FCBGA1363

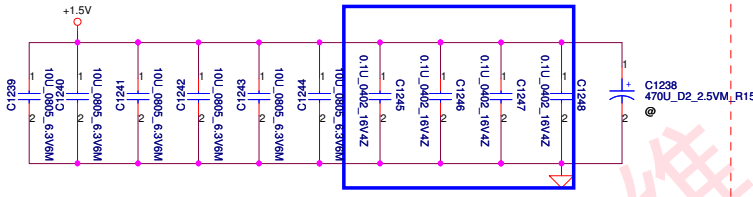
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Issued Date	2006/02/20	Deciphered Date	2009/02/20	Compal Electronics, Inc.
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- <-9> DDR_A_DQS#[0..7]
- <-9> DDR_A_D[0..63]
- <-9> DDR_A_DM[0..7]
- <-9> DDR_A_DQS0[0..7]
- <-9> DDR_A_MA[0..14]
- <-9> DDR_A_BS[0..2]

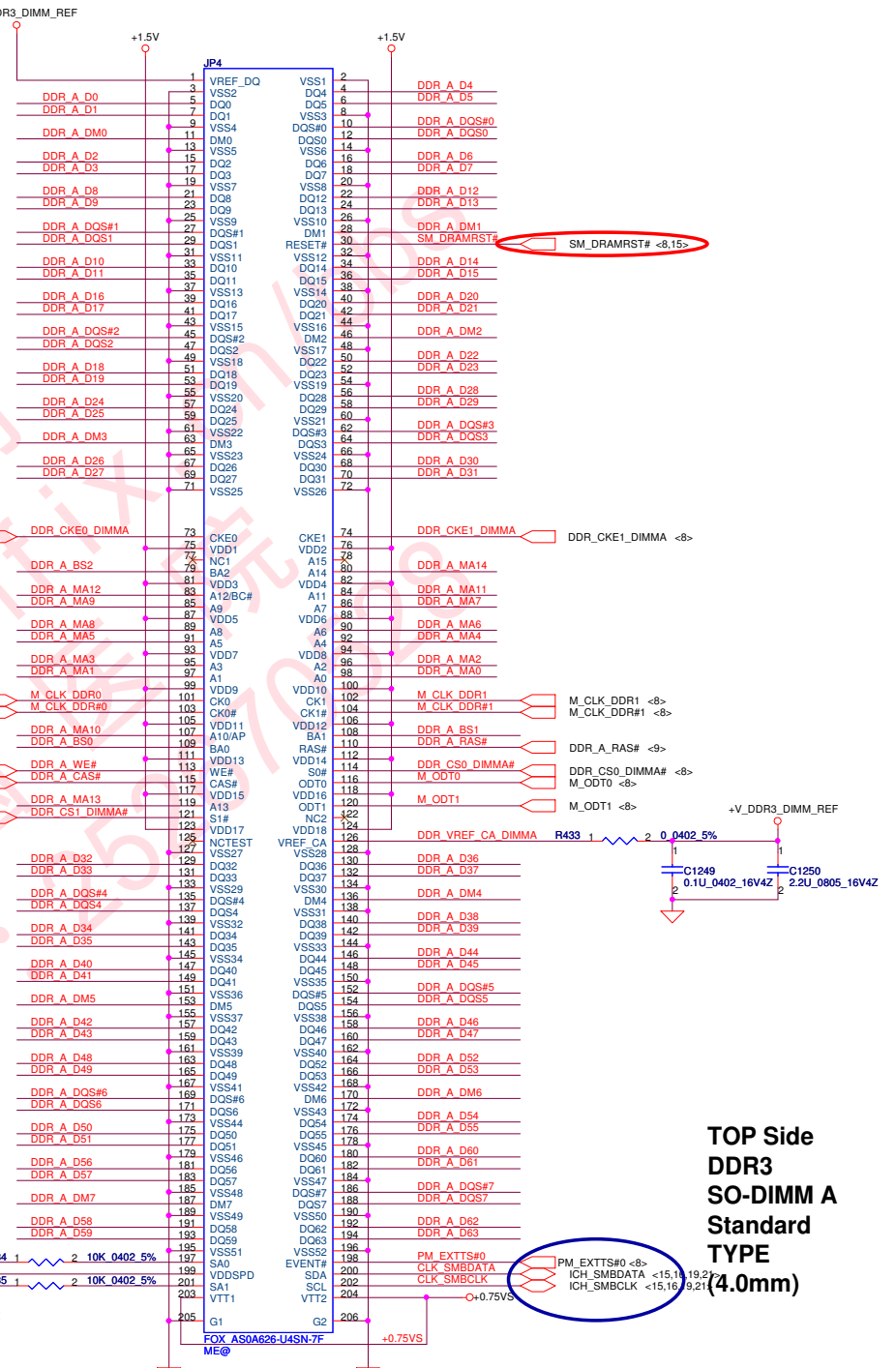
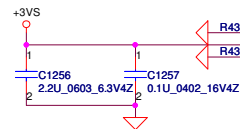
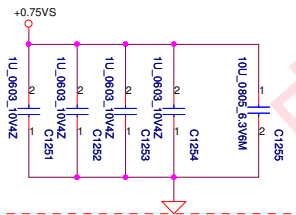


Layout Note:
Place near JP3

Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

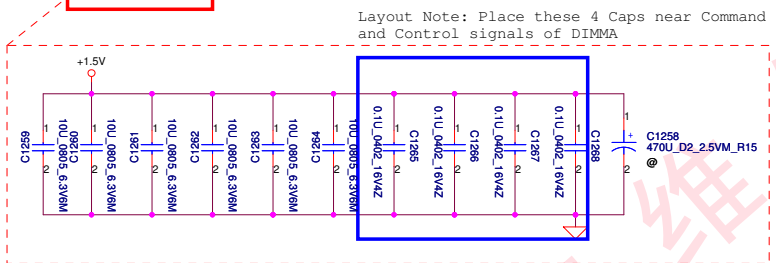


Layout Note:
Place near JP3.203 & JP3.204



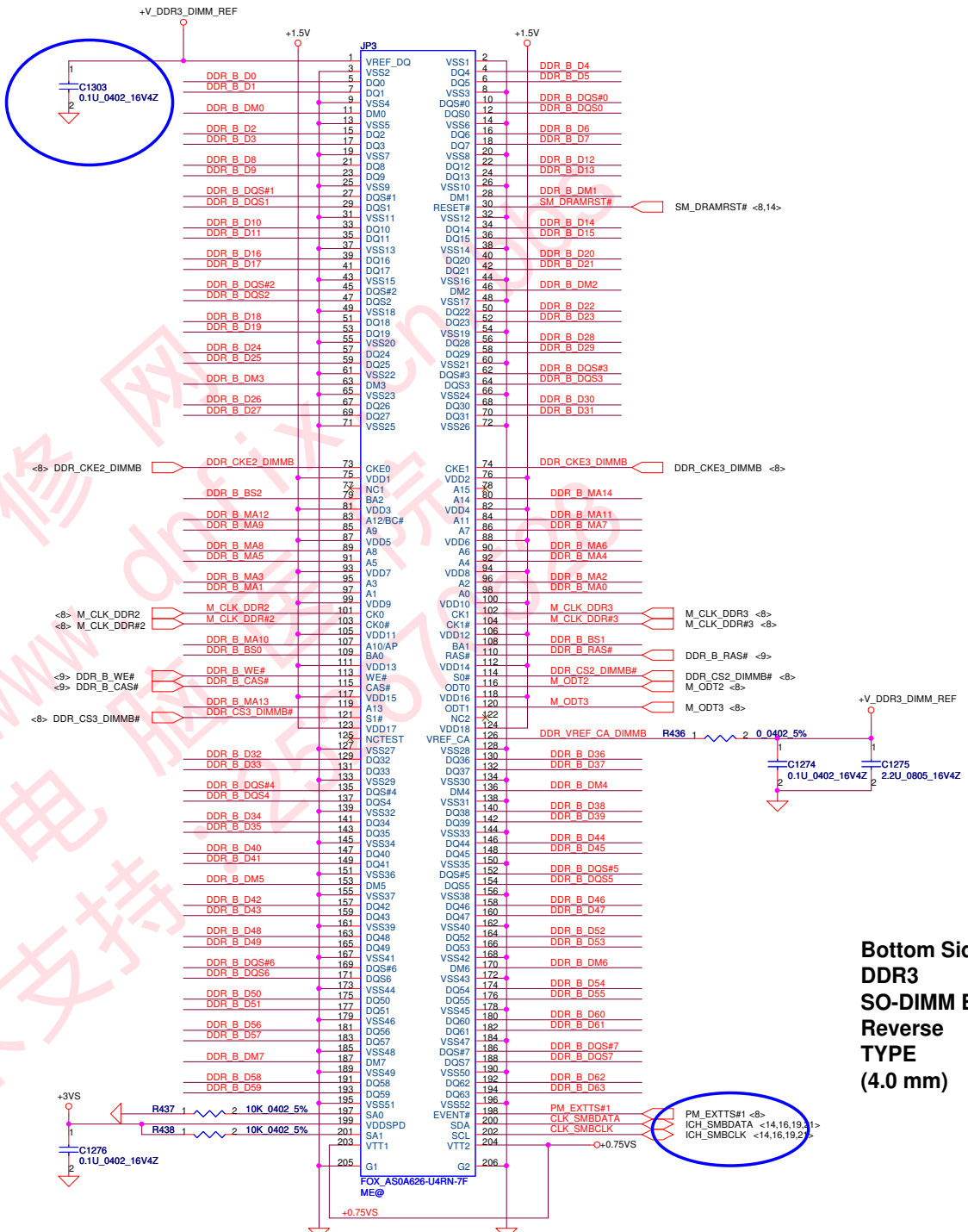
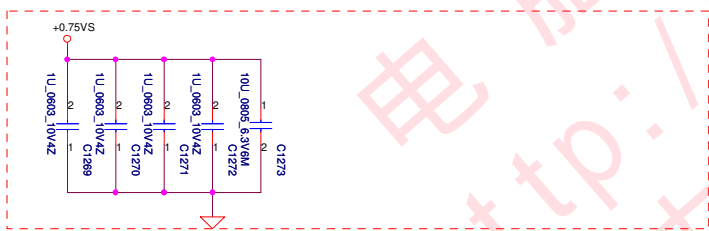
- <-> DDR_B_DQS[0..7]
- <-> DDR_B_D[0..63]
- <-> DDR_B_DM[0..7]
- <-> DDR_B_DQS#0..7]
- <-> DDR_B_MA[0..14]
- <-> DDR_B_BS[0..2]

Layout Note:
Place near JP4



Layout Note: Place these 4 Caps near Command and Control signals of DIMMA

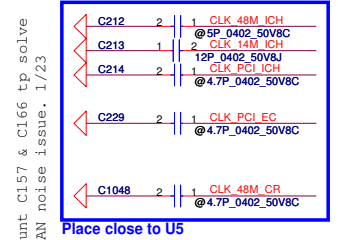
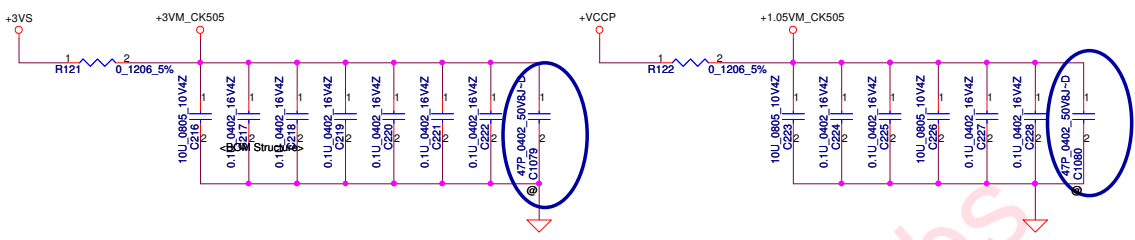
Layout Note:
Place near JP4.203 & JP4.204



**Bottom Side
DDR3
SO-DIMM B
Reverse
TYPE
(4.0 mm)**

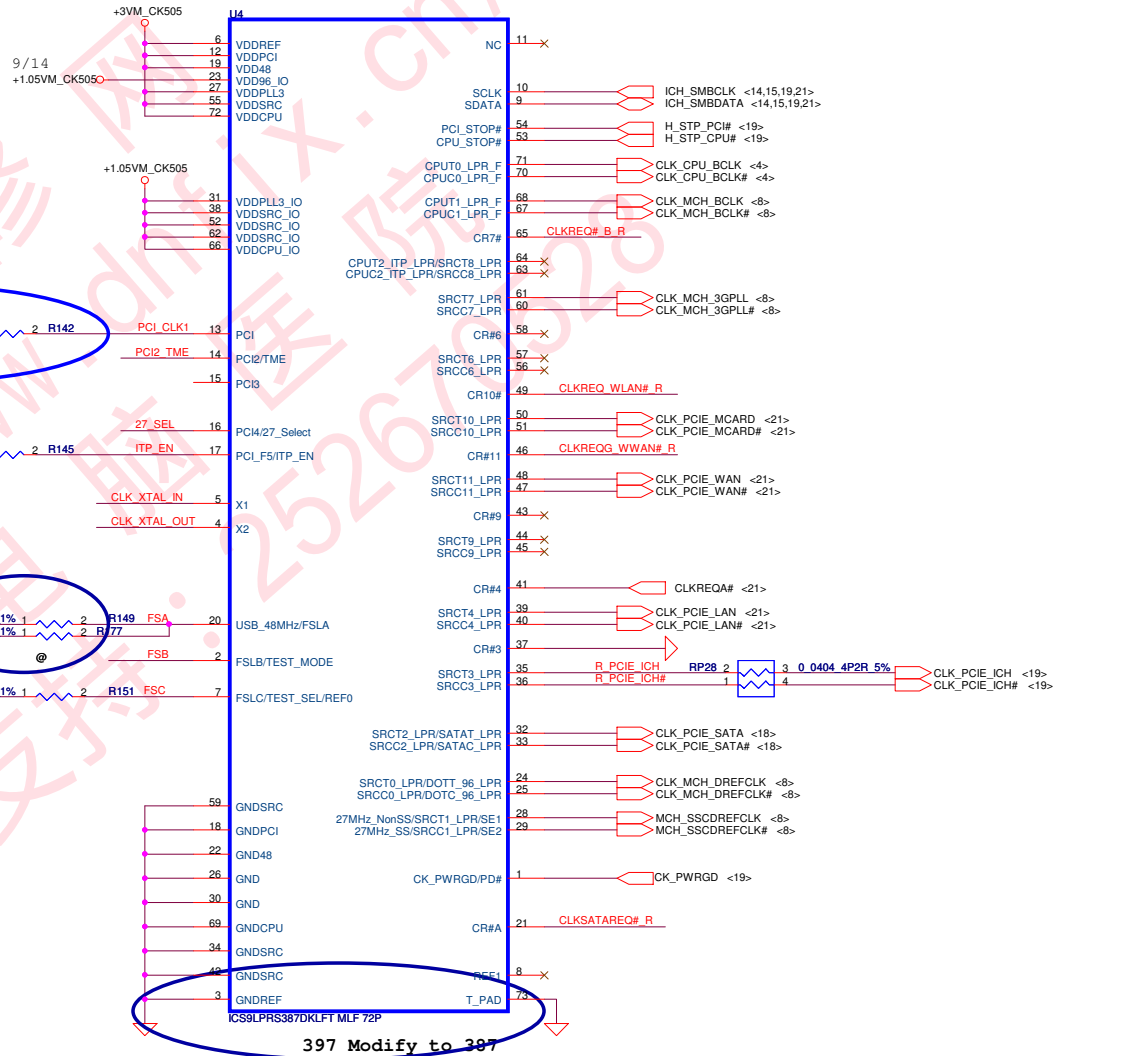
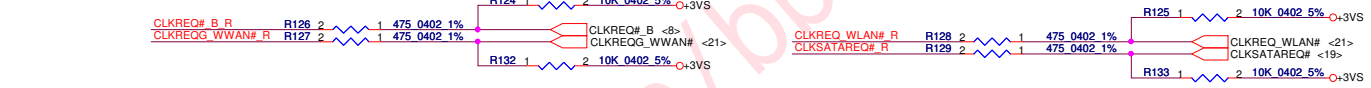
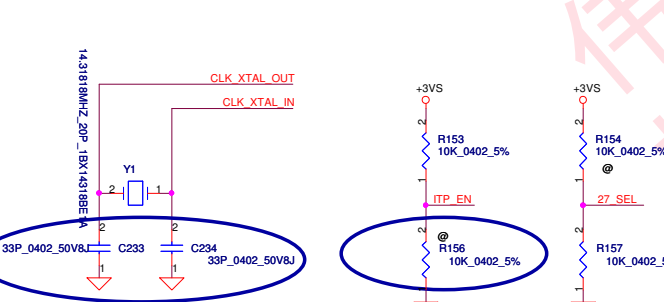
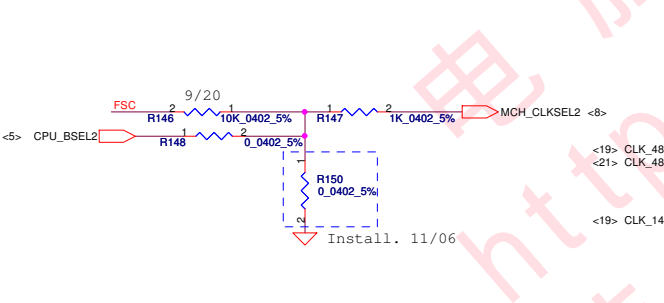
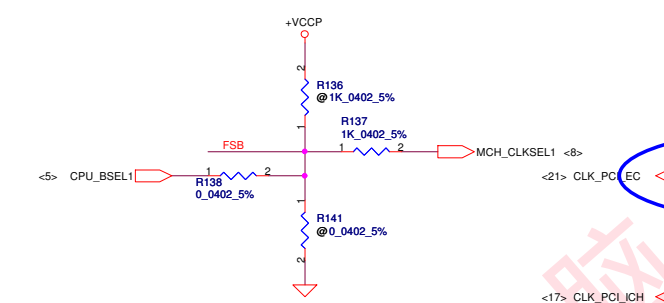
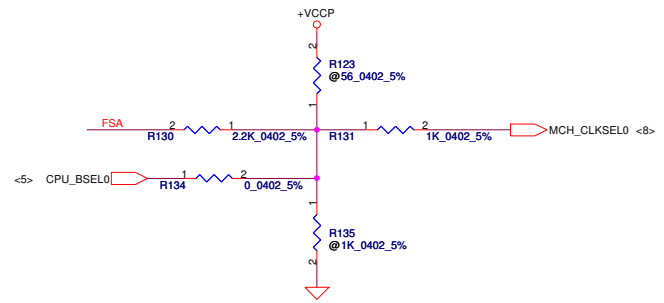
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Size	Document Number	Rev		Date	
	LS-5581P	2.0		Thursday, July 23, 2009	
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FSLC	FSLB	FSLA	CPU	FSB	SRC	PCI
CLKSEL2	CLKSEL1	CLKSEL0	MHz	MHz	MHz	MHz
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0	1	0	200	800	100	33.3
0	1	1	166	667	100	33.3

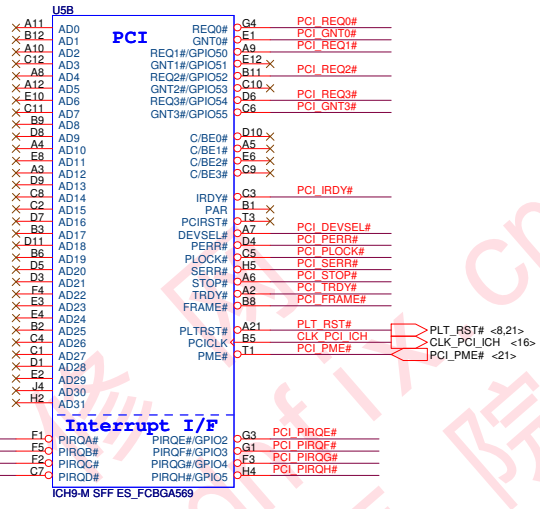
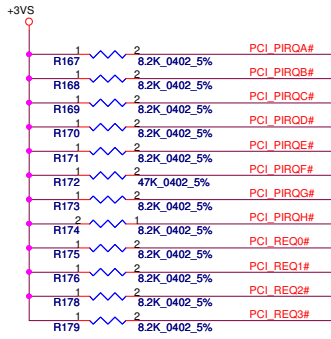
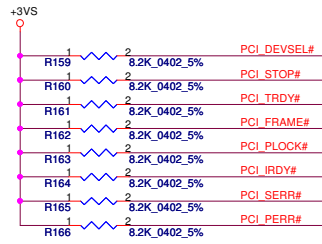


Mount C157 & C166 top solve
WLAN noise issue. 1/23

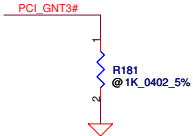
Place close to U5



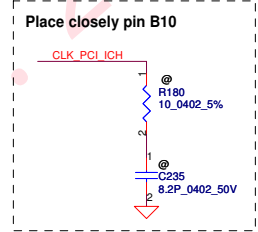
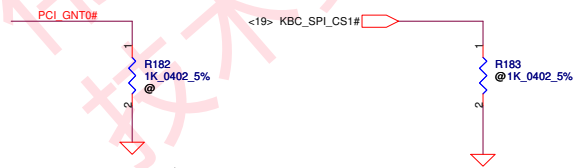
Security Classification	Compal Secret Data		Title	
Issued Date	2006/02/20	Deciphered Date	2009/02/20	Compal Electronics, Inc.
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Size	Document Number	Rev	Date	Sheet
	LS-5581P	2.0	Thursday, July 23, 2009	16 of 30



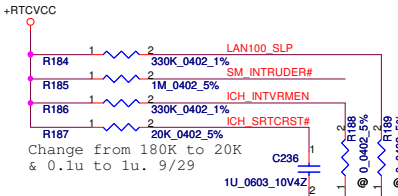
A16 swap override Strap
 Low= A16 swap override Enable
 High= Default*



Boot BIOS Strap		
PCI_GNT0#	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC *

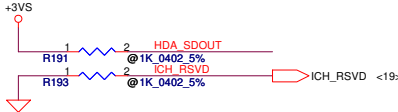


DEL J3. 9/29



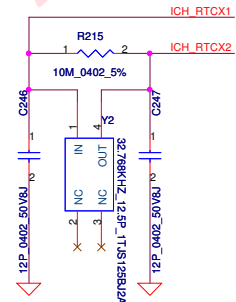
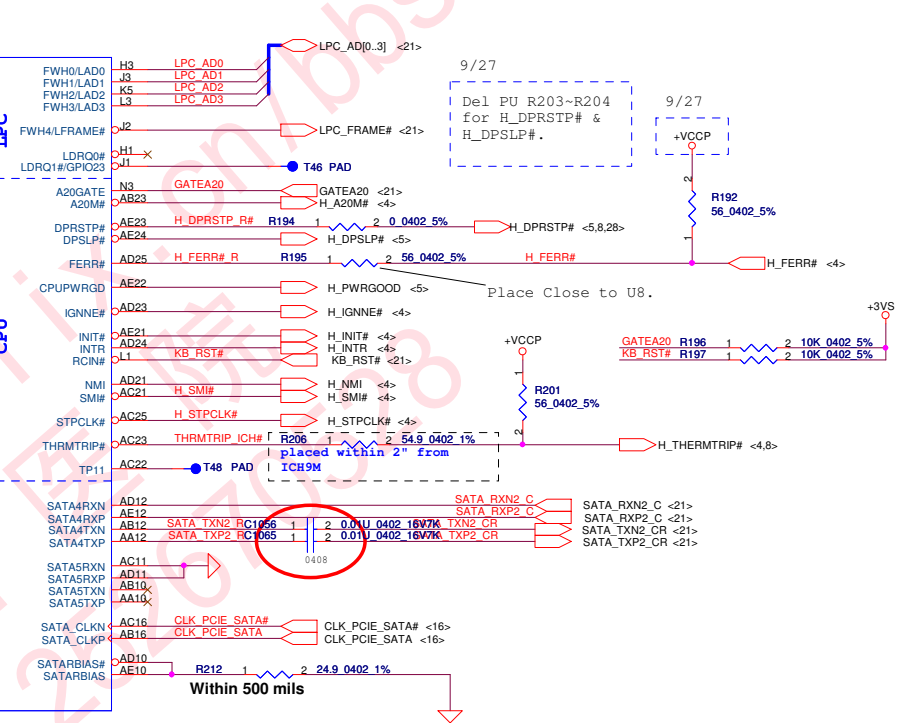
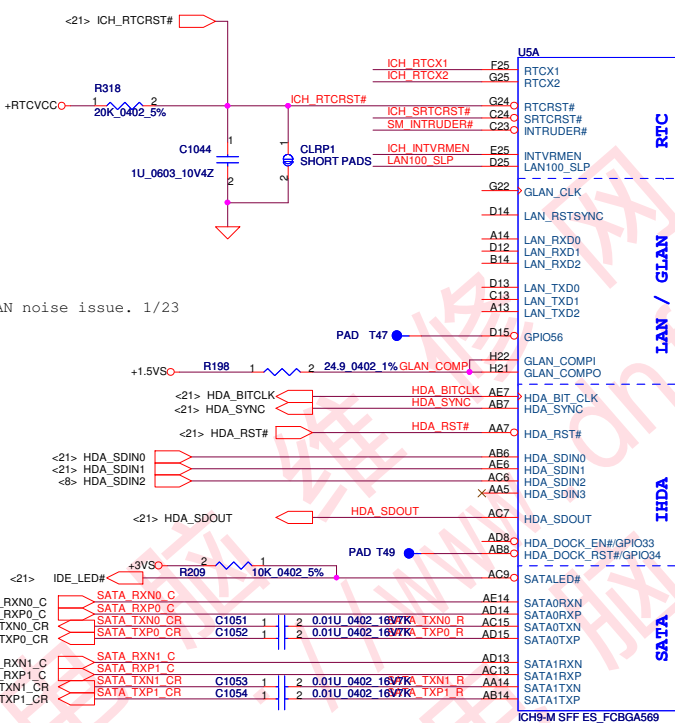
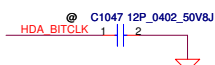
ICH_RSVD	HDA_SDOUT_CODECC	Description
0	0	RV
0	1	XOR
1	0	Normal (D)
1	1	PCIE Bit

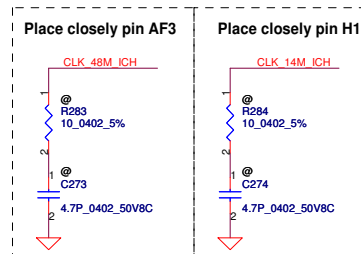
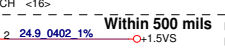
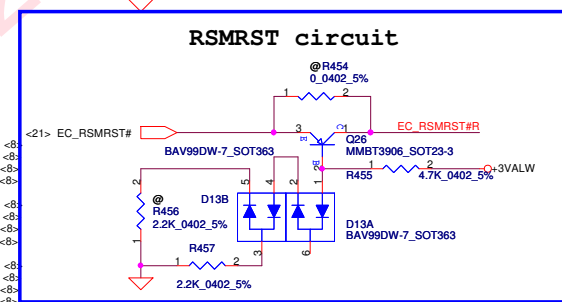
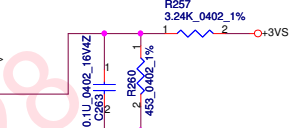
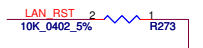
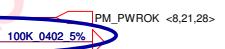
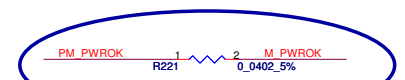
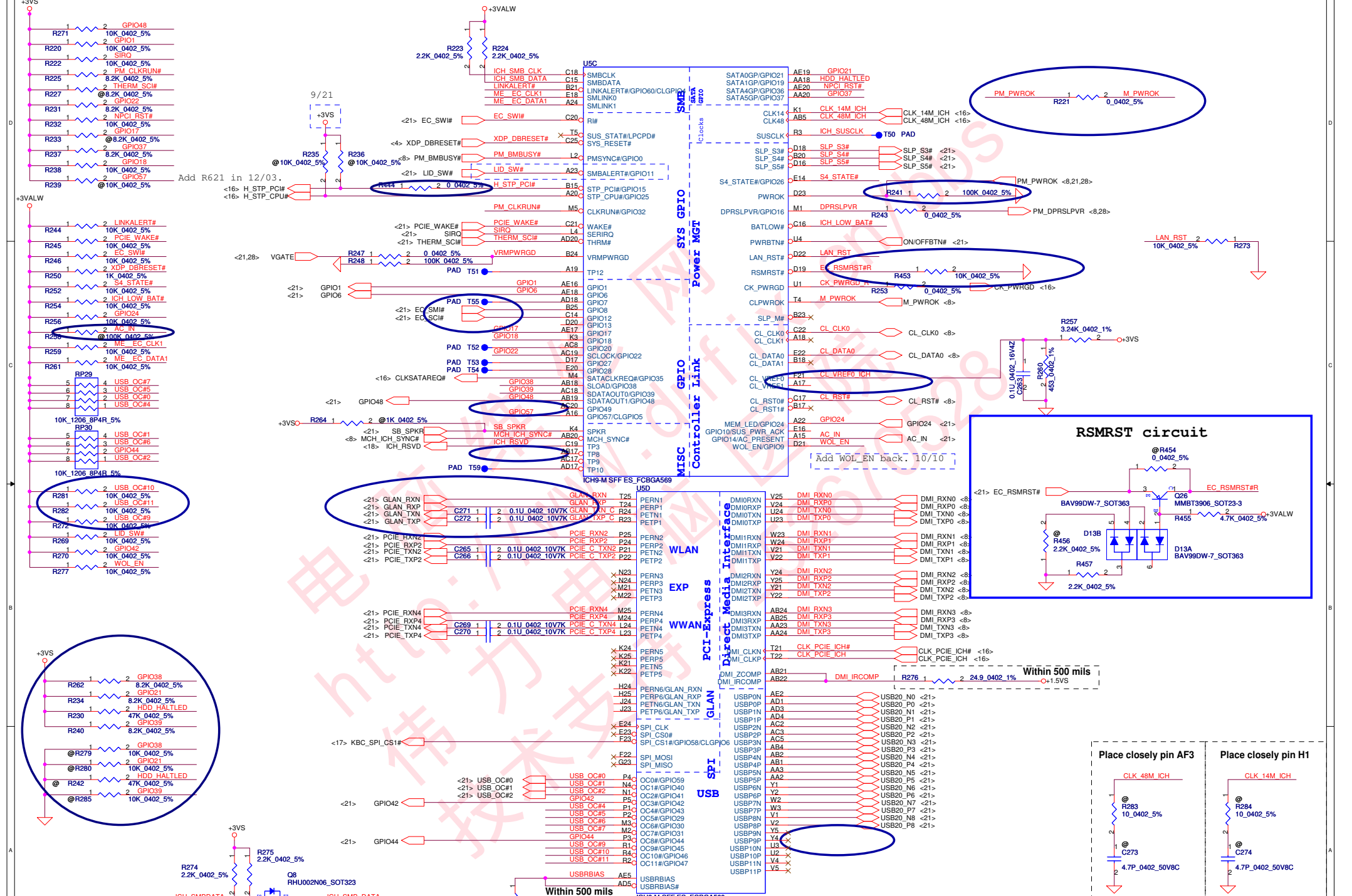
XOR CHAIN ENTRANCE STRAP:RSVD



Add C599 ~ C602 to solve WWAN noise issue. 1/23

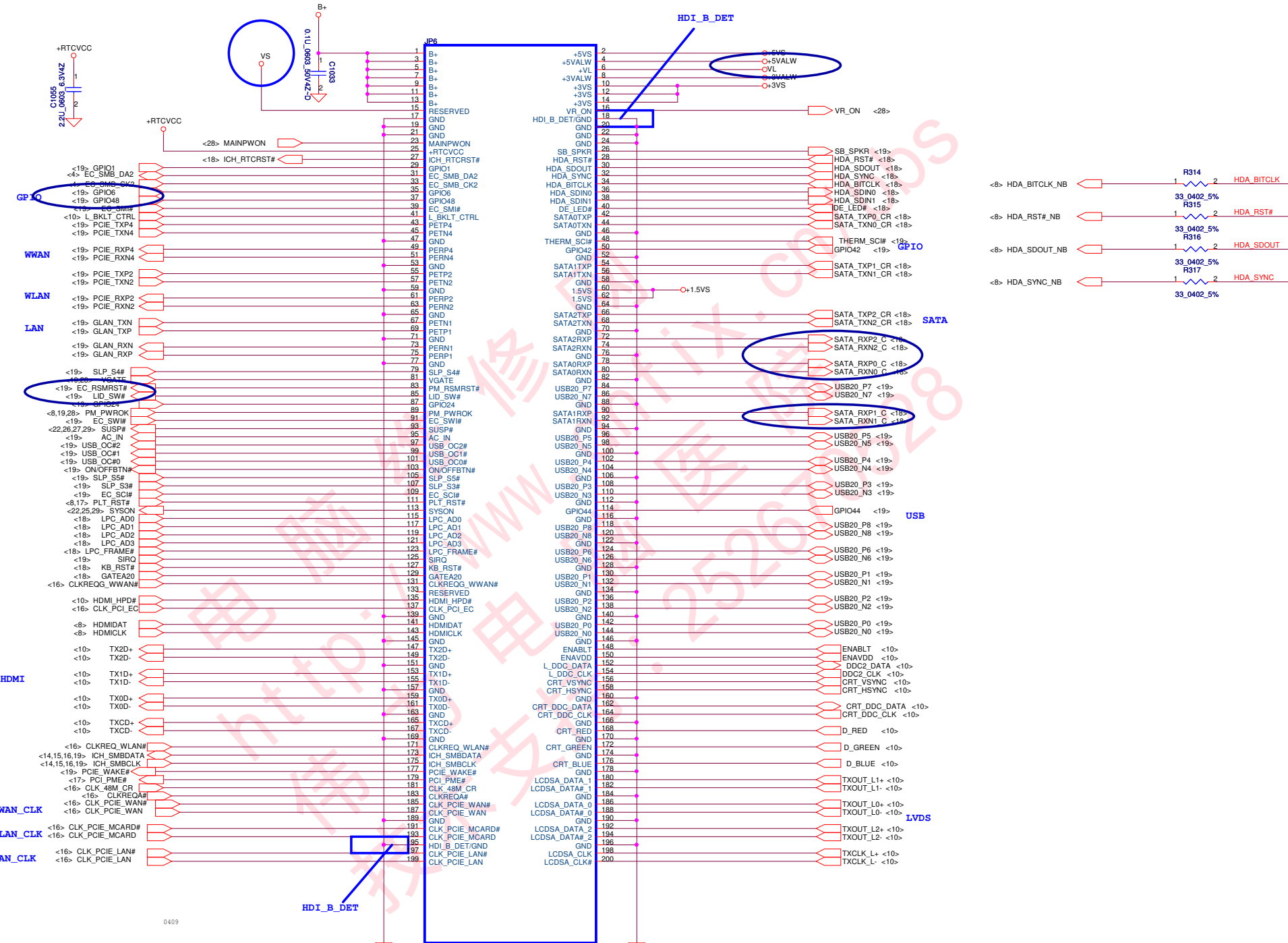
Remove R227 & C199



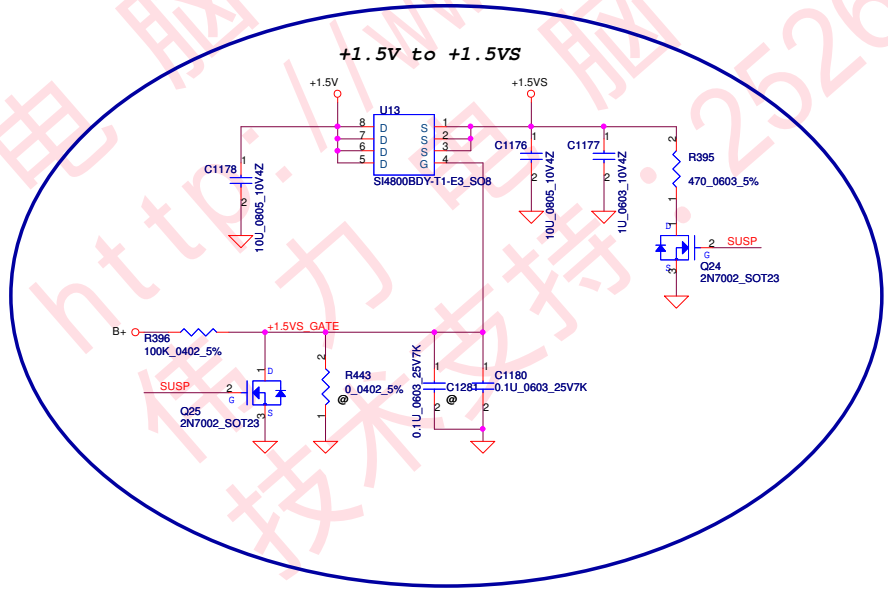
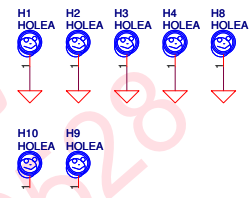
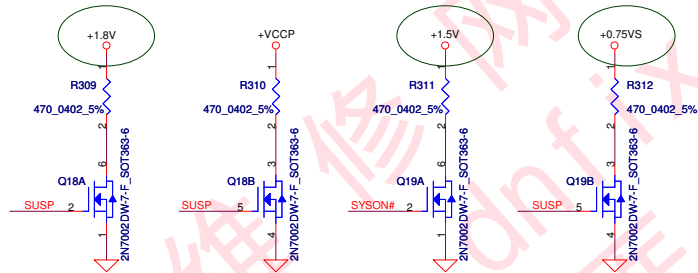
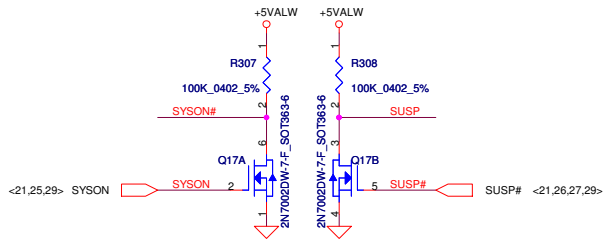
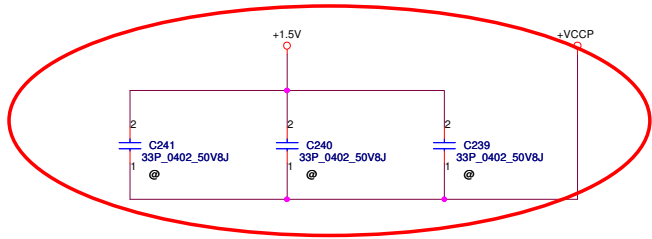


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Compal Electronics, Inc.		
ICH9(3/4) DMI,USB,GPIO,PCIE		
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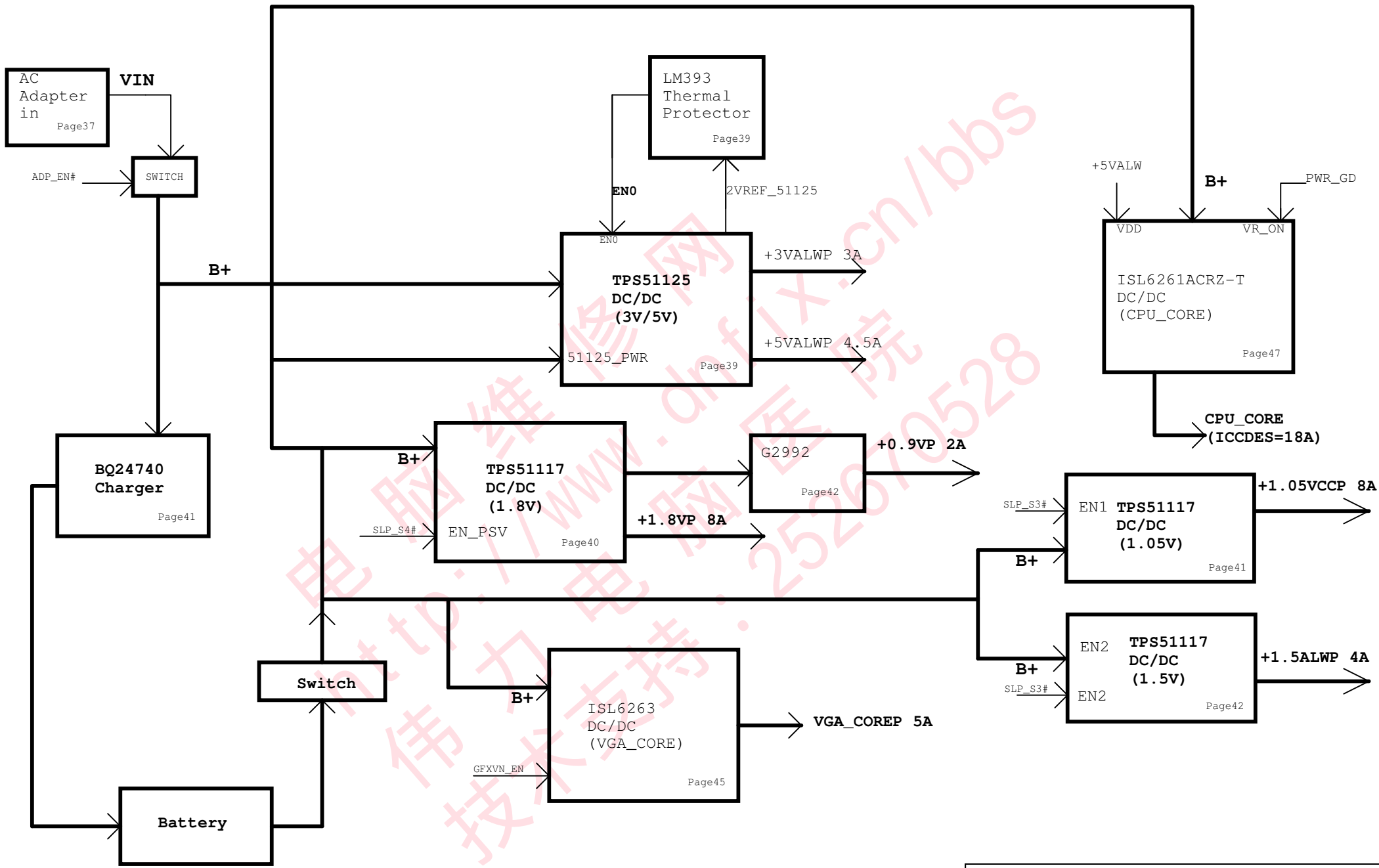
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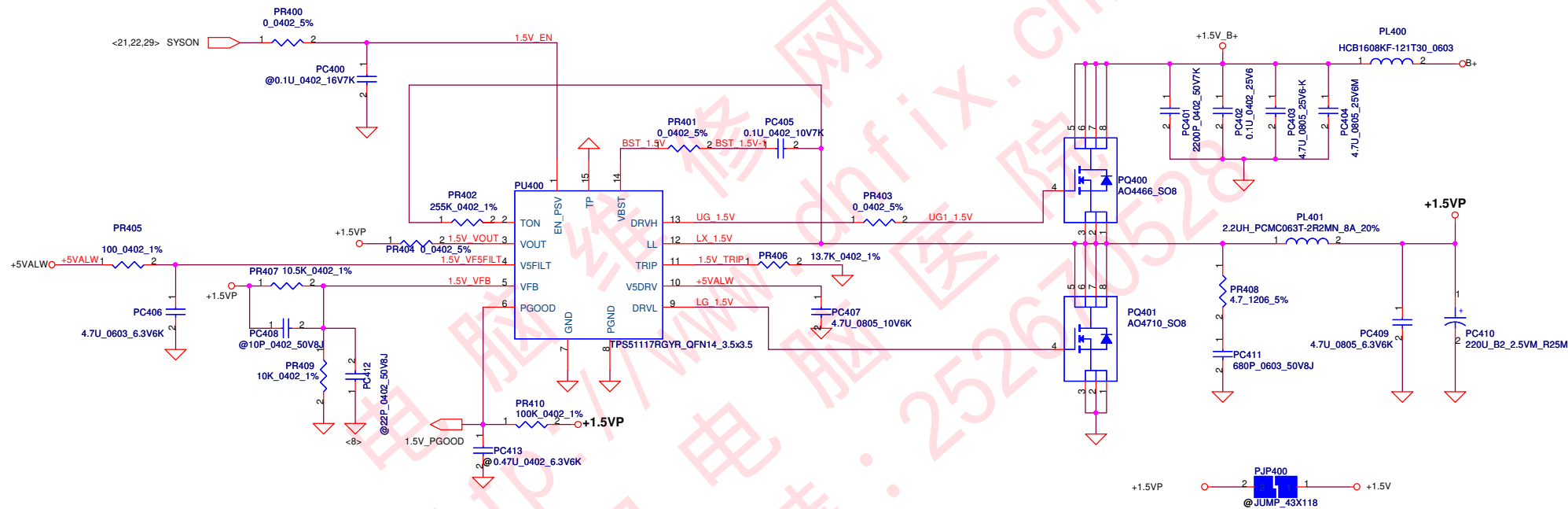
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Date	Description	Rev.
4/16	Release LS5581PR01 schematic.	01
5/8	<p>R53 change to 499 Ohm R68,R69,R70 implement 750hm Add C1303 for DDR3 request Change R149,R177 from 33 to 150hm Change C233,C234 from 33P to 22P R153 implement 10K_Ohm and R156 remove Add C1079,C1080 for EMI Delete R249,R255,R267,R268 for optionUSB and GPIO Delete C1066,C1067,C1068,C1069,C1070,C1071 for SATA AC cap Add VL voltage on JP6.6 for OCP use Modify SB VCCSUSHDA power level Modify SB GLAN fromPCIE4 to PCIE1 Delete R265,C264,C266 for CL_REF1 Delete R240 for H_STP_CPU# and Add R444 for H_STP_PCI# Change R221 connect from VGATE to PM_PWROK Change R240 from H_STP_CPU# to H_STP_PCI# Change EC_SCI# from GPIO7 to GPIO12 Delete T56,T57,T58,R263 for no use Add R281,R282 for USB OC# pull high Add R242,R285 for Project ID define Modify H5,H6,H7,H11,H12 footprint for ME recommend Delete R251 and Add Q26,D13,R453-R457 for RSMRST# function Delete USB9 pair on SB for not use Modify CLK_PCI_EC from U4.15 to U4.13 Modify power plane from +1.8VS to +1.8V for NB use Change Name from DDR3_DIMM_REF to DDR3_NB_REF for DDR3 recommend Change DDR_PM_EXITS# 1 from not use to JP3 Del R106 for Intel Recommend for HDMI setting</p>	

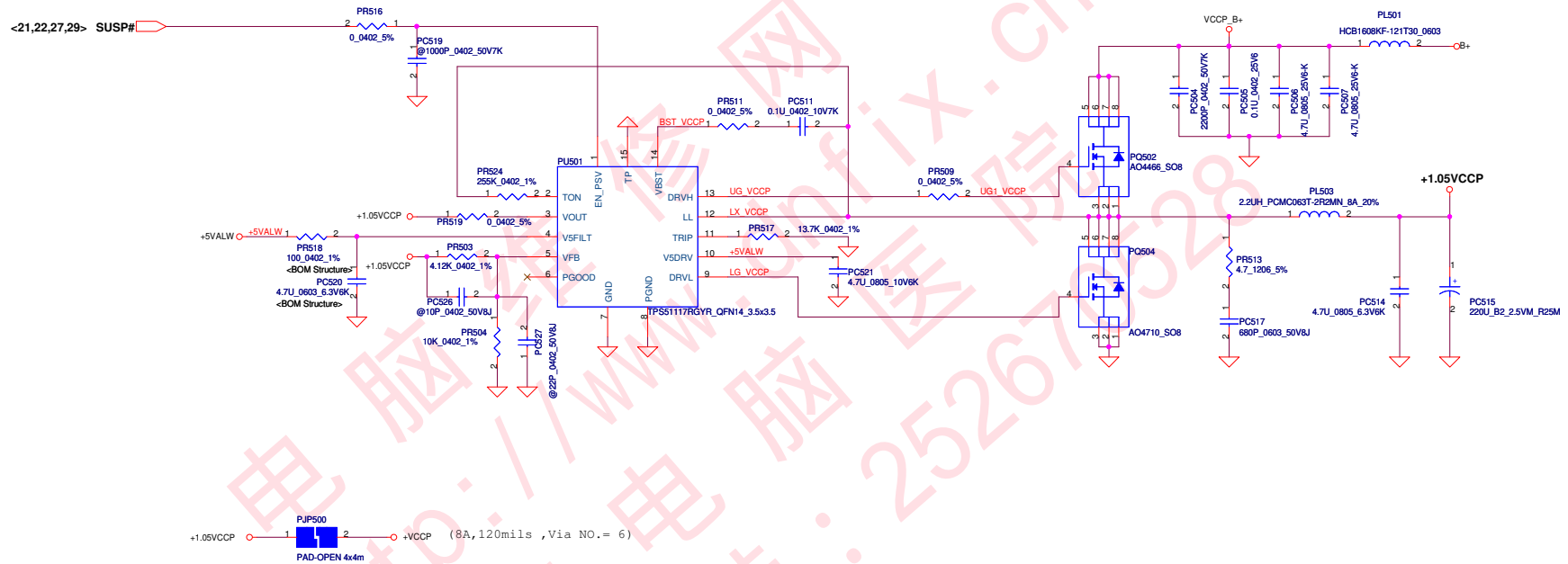
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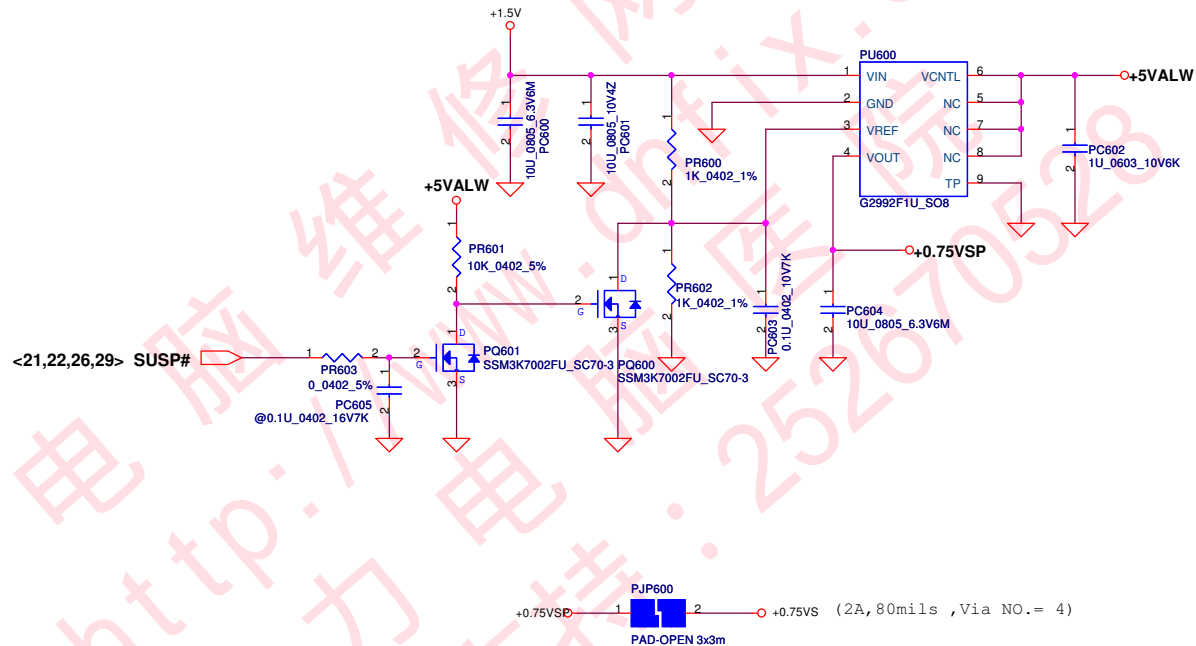
Title		
POWER BLOCK DIAGRAM		
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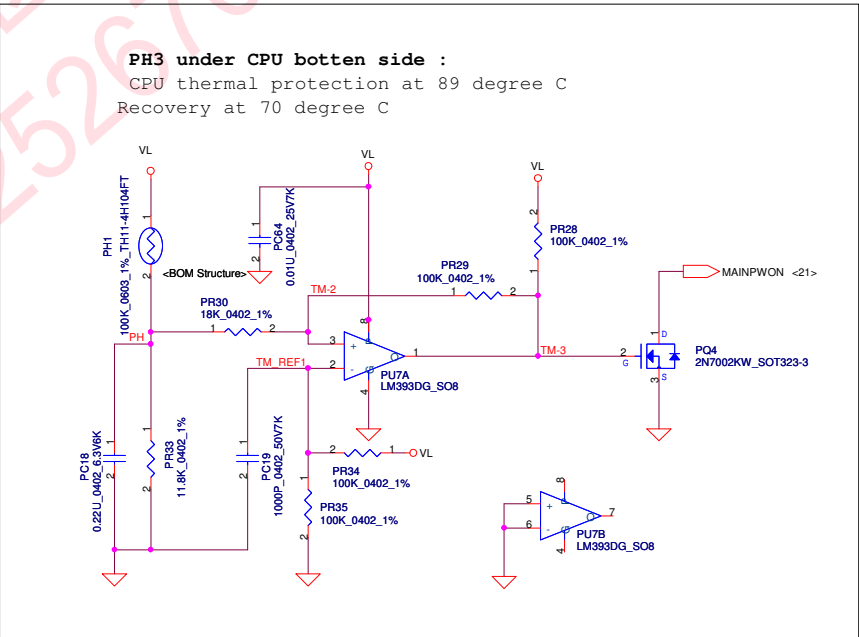
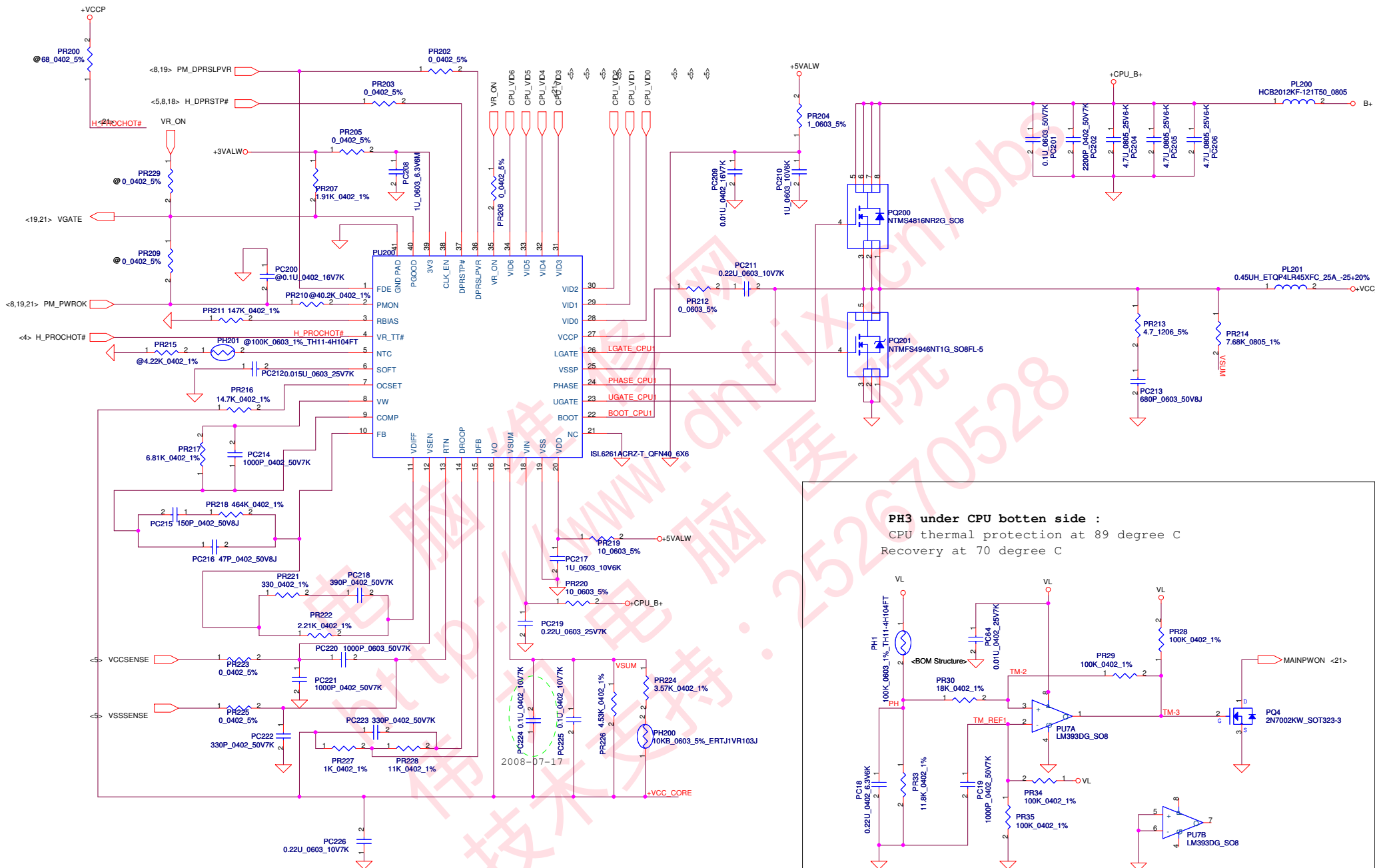
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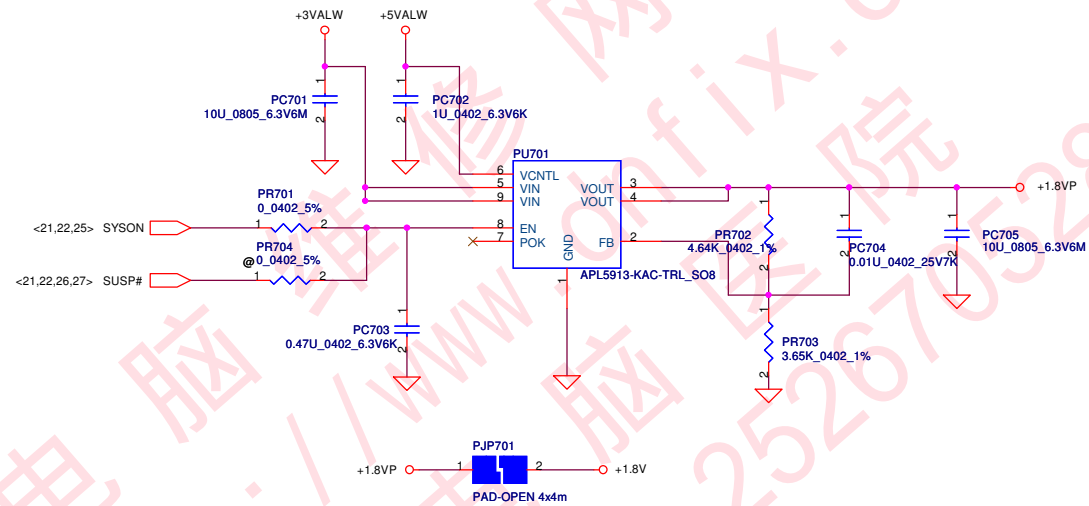
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Item	Reason for change	PG#	Modify List	Date	Phase
1	change OTP 89 degree protect 70 degree recover	B	change PR33=11.8k PR30=18k PR29=100k PR28=100K		
2	Change 1.8vp sequence to SYSON	B	Del PR704		
3	Change 1.5vp Voltage set for hw request	B	change PR407 to 10.5K		
4	For solve RT8209 issue	B	change PR405 PR518 to 100 PC406 PC520 to 4.7U		
5	modify PQ600 PQ601 PN follow C38 bom	C	modify 2N7002 from Rohm to toshiba		
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