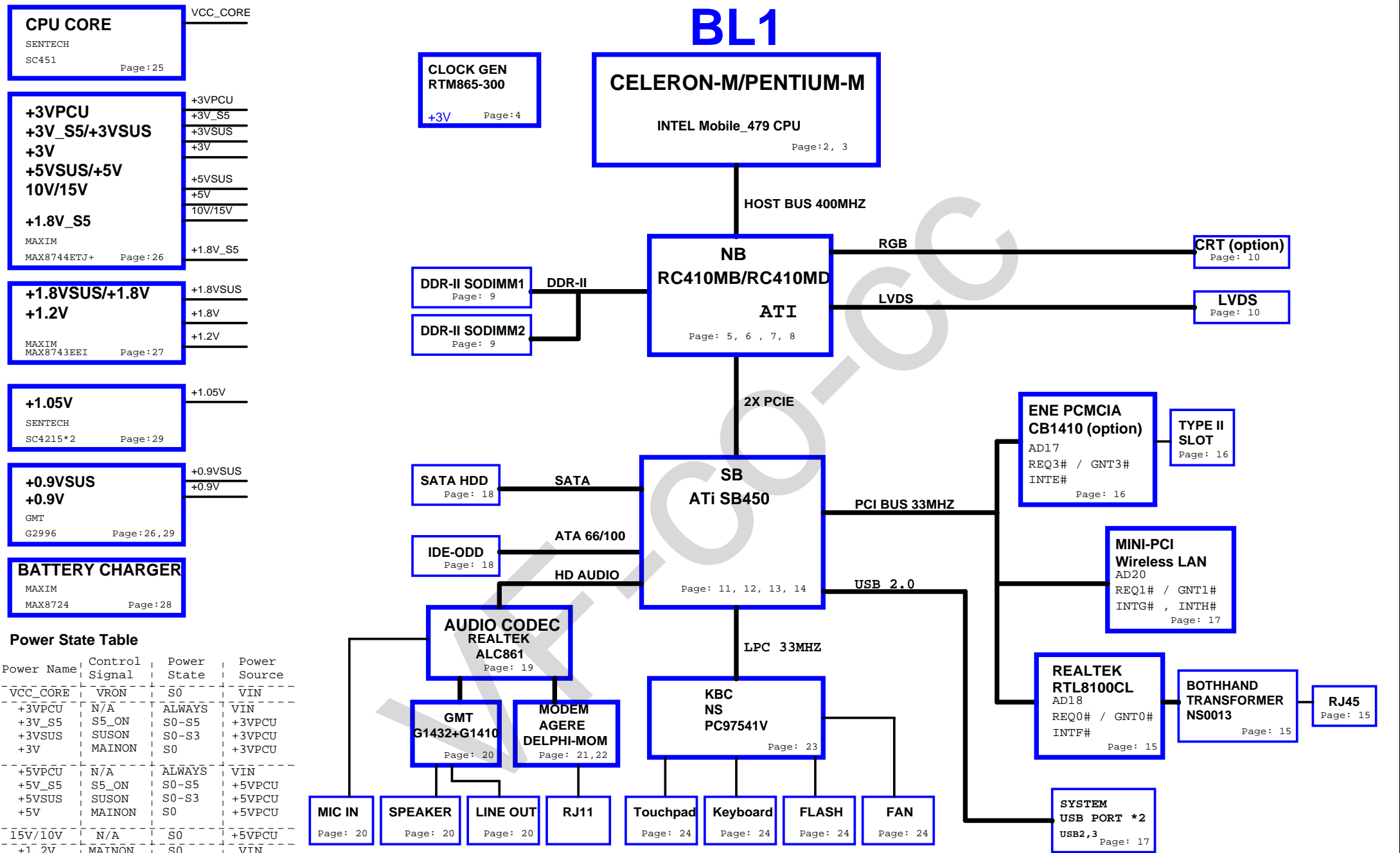
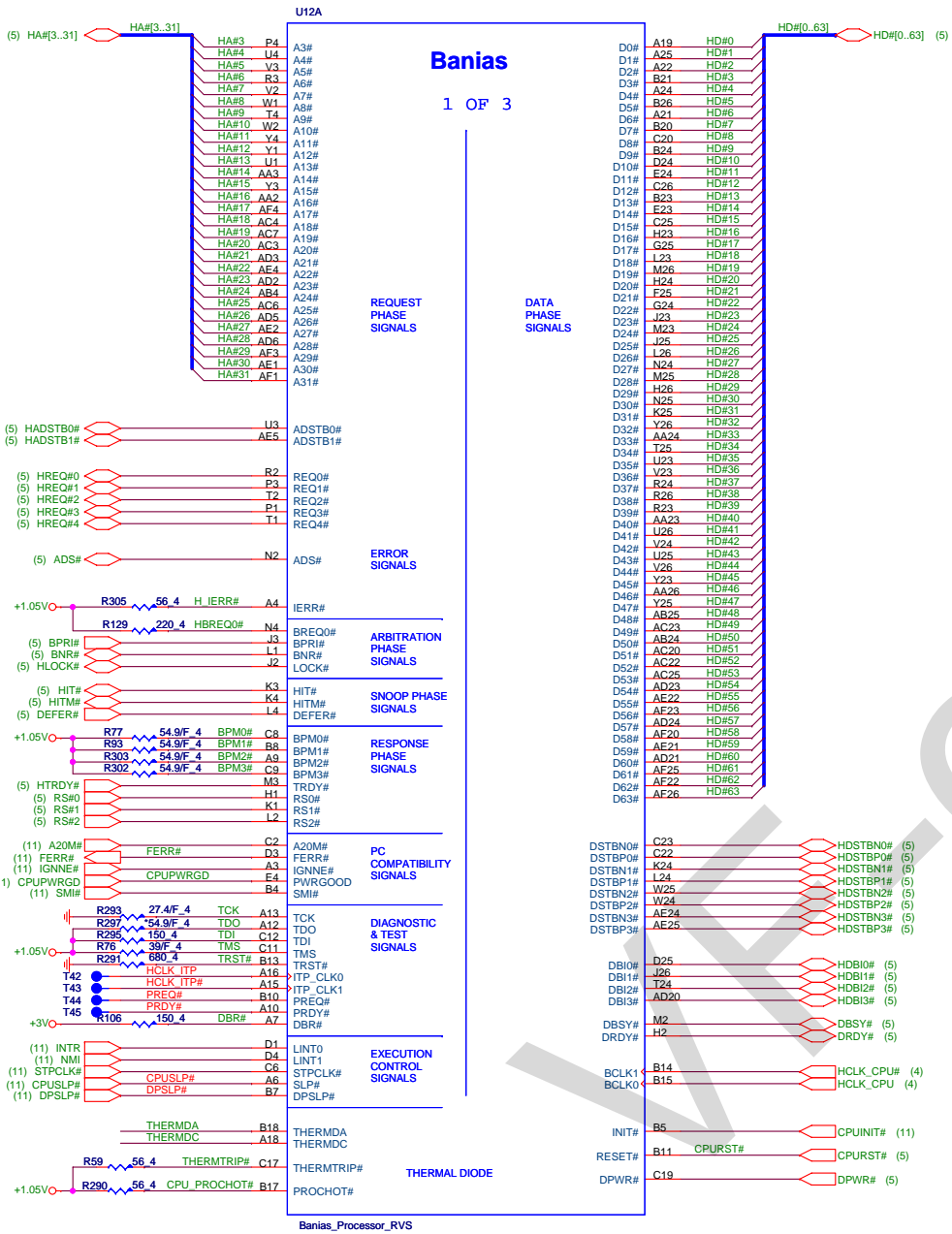


# BL1



**Power State Table**

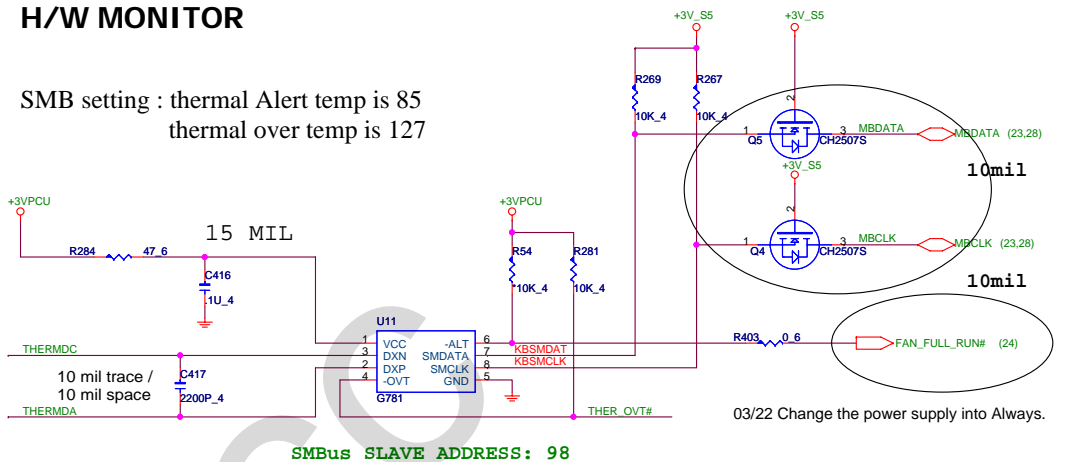
Power Name	Control Signal	Power State	Power Source
VCC_CORE	VRON	S0	VIN
+3VPCU	N/A	ALWAYS	VIN
+3V_S5	S5_ON	S0-S5	+3VPCU
+3VSUS	SUSON	S0-S3	+3VPCU
+3V	MAINON	S0	+3VPCU
+5VPCU	N/A	ALWAYS	VIN
+5V_S5	S5_ON	S0-S5	+5VPCU
+5VSUS	SUSON	S0-S3	+5VPCU
+5V	MAINON	S0	+5VPCU
15V/10V	N/A	S0	+5VPCU
+1.2V	MAINON	S0	VIN
+1.05V	MAINON	S0	+1.8VSUS
+0.9V	MAINON	S0	+1.8VSUS
+1.8V_S5	S5_ON	S0-S5	+3VPCU
+1.8VSUS	SUSON	S0-S3	VIN
+1.8V	MAINON	S0	+1.8VSUS



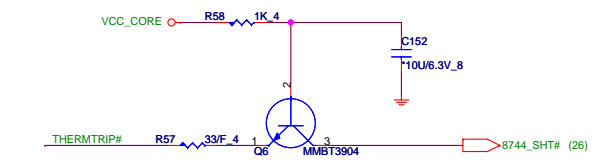
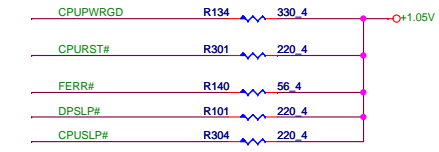
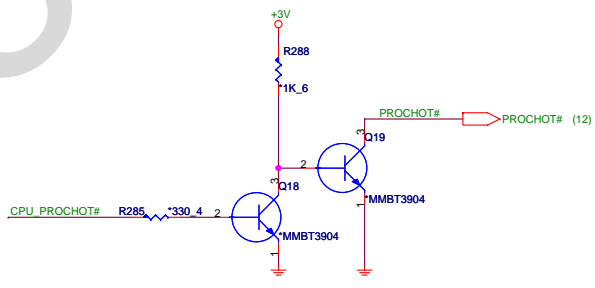
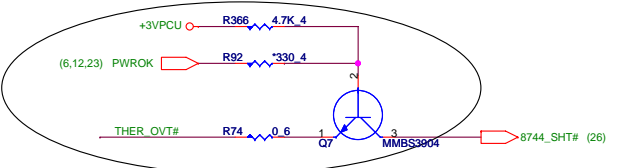
# CPU

## H/W MONITOR

SMB setting : thermal Alert temp is 85  
thermal over temp is 127

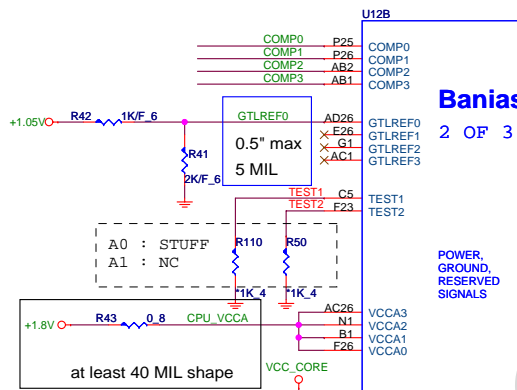
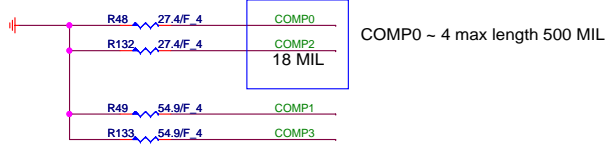


	-OVT	-ALT
CPU	127	
Ambient		85

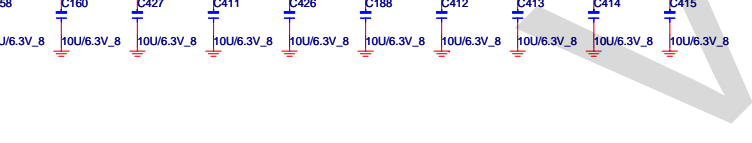
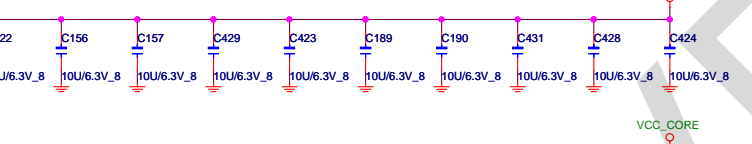
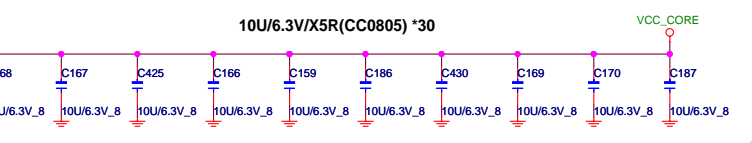
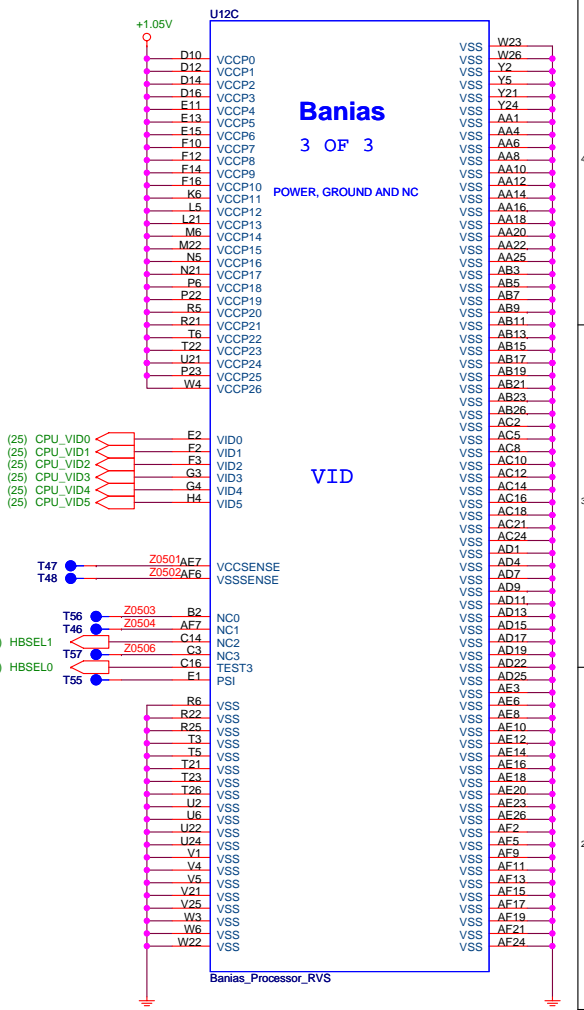


**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>CPU ( HOST BUS )-1</b>	2A
Date:	Monday, April 03, 2006	Sheet 2 of 30



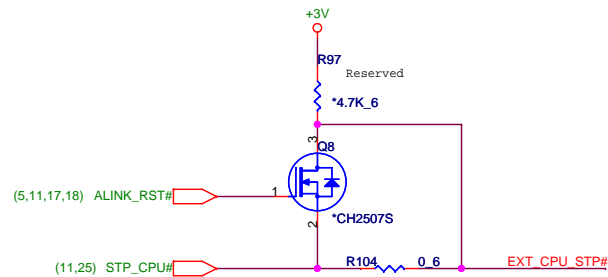
VSS	A2
VSS	A5
VSS	A8
VSS	A11
VSS	A14
VSS	A17
VSS	A20
VSS	A23
VSS	A26
VSS	B3
VSS	B6
VSS	B9
VSS	B12
VSS	B16
VSS	B19
VSS	B22
VSS	B25
VSS	M2
VSS	C1
VSS	C4
VSS	C7
VSS	C10
VSS	C13
VSS	C15
VSS	C18
VSS	C21
VSS	C24
VSS	D2
VSS	D7
VSS	D9
VSS	D11
VSS	D13
VSS	D17
VSS	D19
VSS	D21
VSS	D23
VSS	D26
VSS	E3
VSS	E6
VSS	E8
VSS	E10
VSS	E12
VSS	E14
VSS	E16
VSS	E18
VSS	E20
VSS	E22
VSS	E25
VSS	F1
VSS	F4
VSS	F7
VSS	F9
VSS	F11
VSS	F13
VSS	F15
VSS	F17
VSS	F19
VSS	F21
VSS	F24
VSS	G2
VSS	G6
VSS	G22
VSS	G23
VSS	G26
VSS	H3
VSS	H5
VSS	H21
VSS	H25
VSS	J1
VSS	J4
VSS	J6
VSS	J22
VSS	J24
VSS	K2
VSS	K5
VSS	K21
VSS	K23
VSS	K26
VSS	L3
VSS	L6
VSS	L22
VSS	L25
VSS	M1
VSS	M4
VSS	M5
VSS	M21
VSS	M24
VSS	N3
VSS	N6
VSS	N22
VSS	N23
VSS	N26
VSS	P2
VSS	P5
VSS	P21
VSS	P24
VSS	R1
VSS	R4



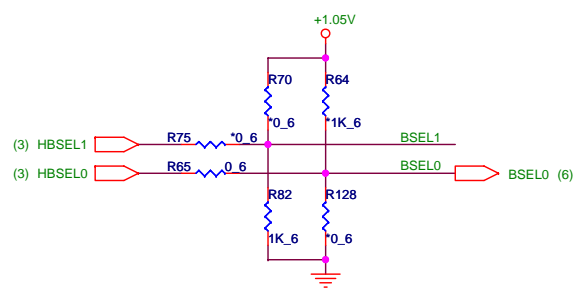
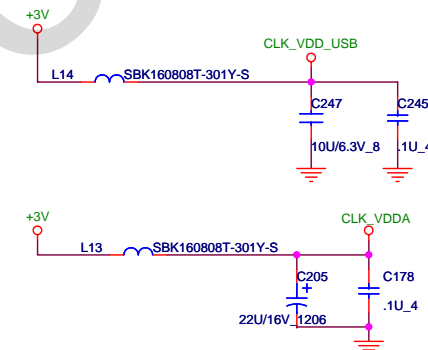
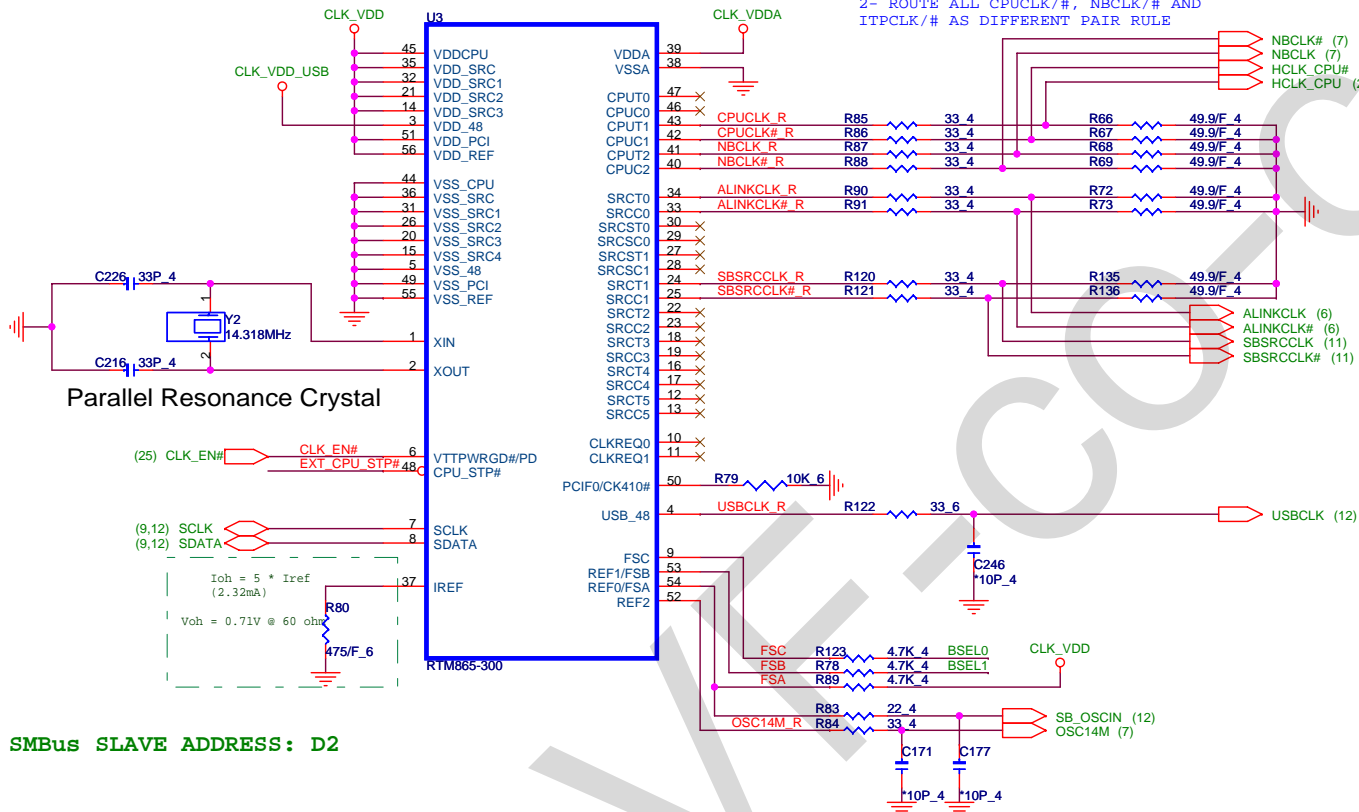
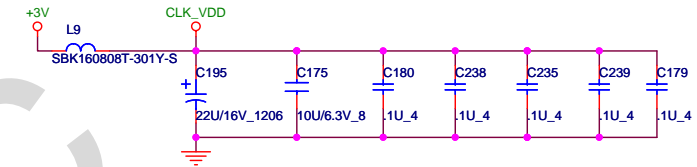
CPU

**PROJECT : BL1**  
**Quanta Computer Inc.**

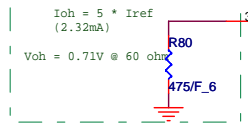
Size	Document Number	Rev
	<b>CPU (POWER)-2</b>	1A
Date:	Monday, April 03, 2006	Sheet 3 of 30



- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS CLK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBCLK/# AND ITPCCLK/# AS DIFFERENT PAIR RULE



**Parallel Resonance Crystal**



SMBus SLAVE ADDRESS: D2

**CK410 FREQUENCY SELECT TABLE(MHZ)**

FSC	FSB	FSA	CPU MHz
0	0	0	266.66
0	0	1	133.33
0	1	0	200.00
0	1	1	166.66
1	0	0	333.33
1	0	1	100.00
1	1	0	400.00
1	1	1	Rsvd

HBSEL1	HBSEL0	Frequency
0	0	133 MHz
0	1	100 MHz

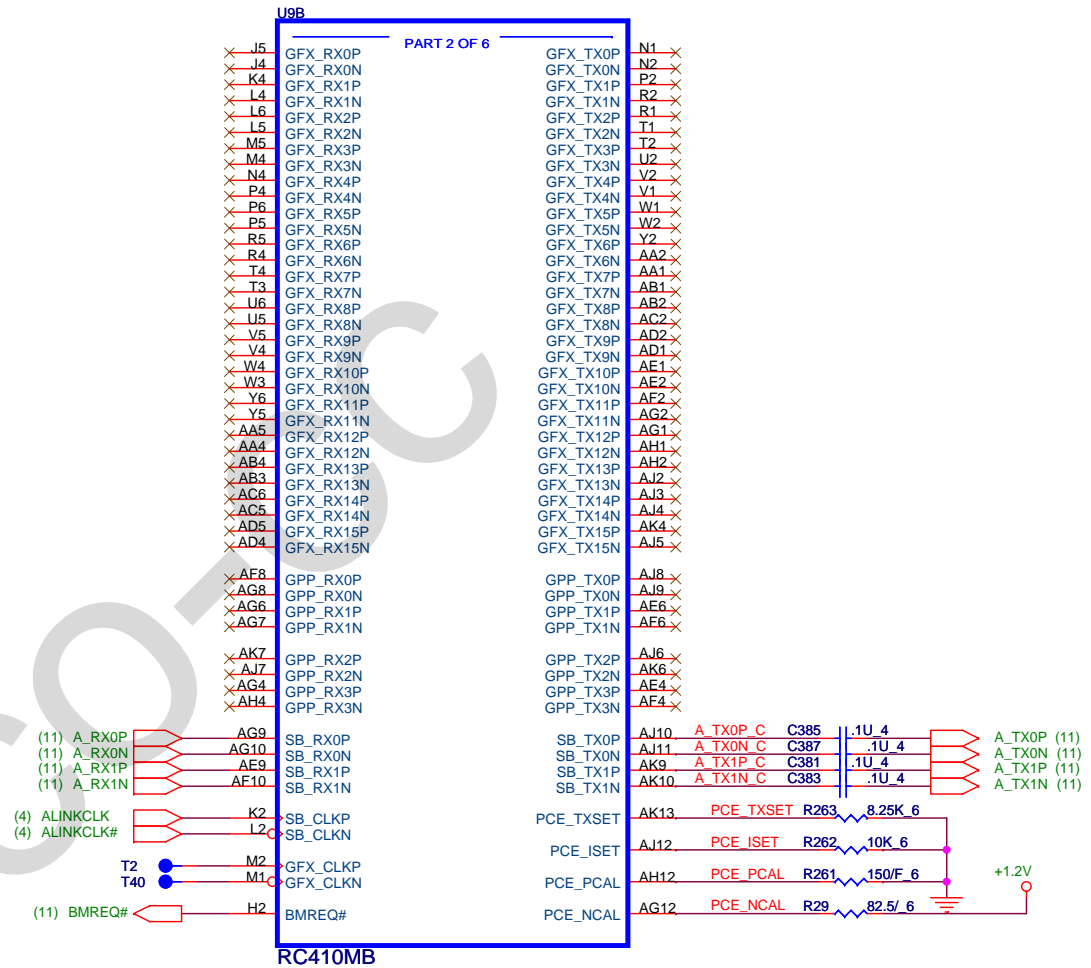
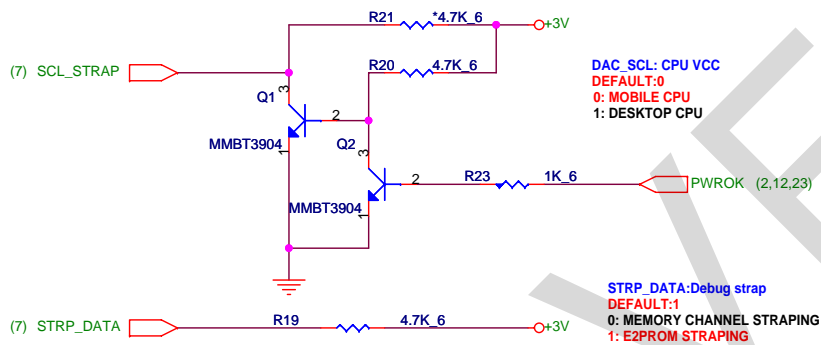
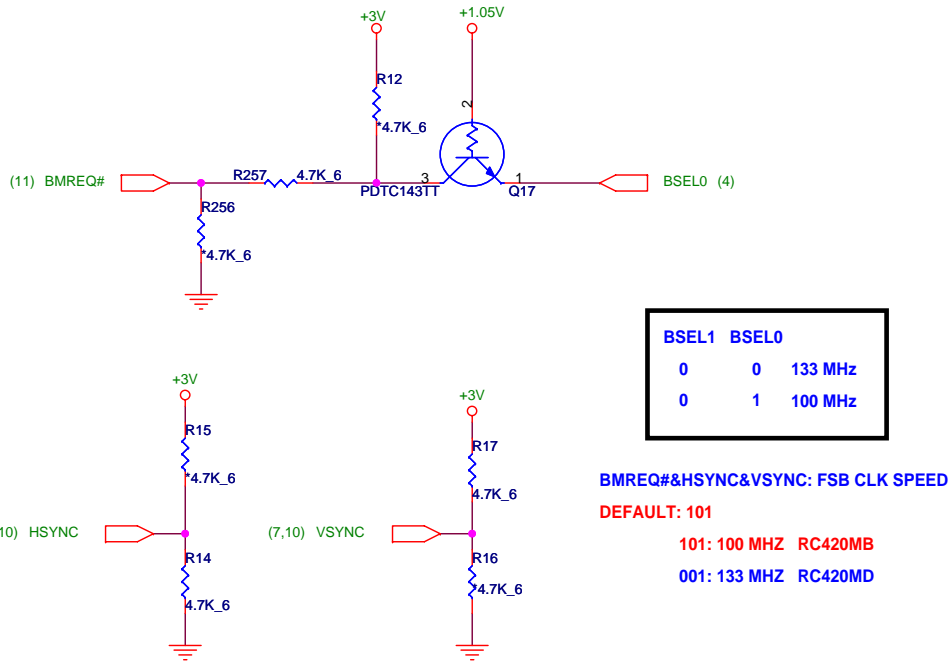
**CLK**

**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>EXTERNAL CLKGEN</b>	1A
Date:	Monday, May 08, 2006	Sheet 4 of 30

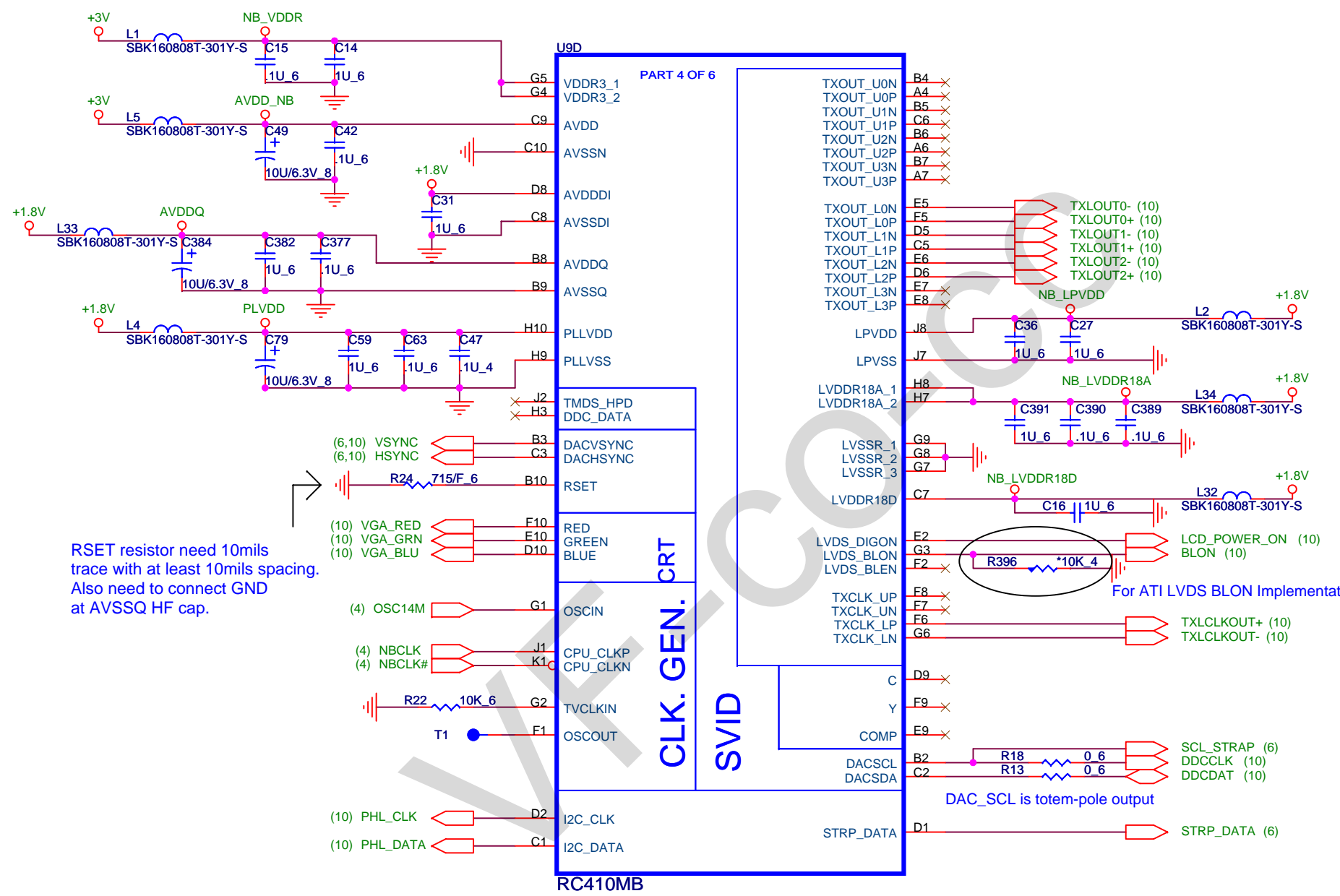


# NB strapping



**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>RC410MB-PCIE LINK I/F</b>	1A
Date:	Friday, April 28, 2006	Sheet 6 of 30



RSET resistor need 10mils trace with at least 10mils spacing. Also need to connect GND at AVSSQ HF cap.

For ATI LVDS BLON Implementation Details

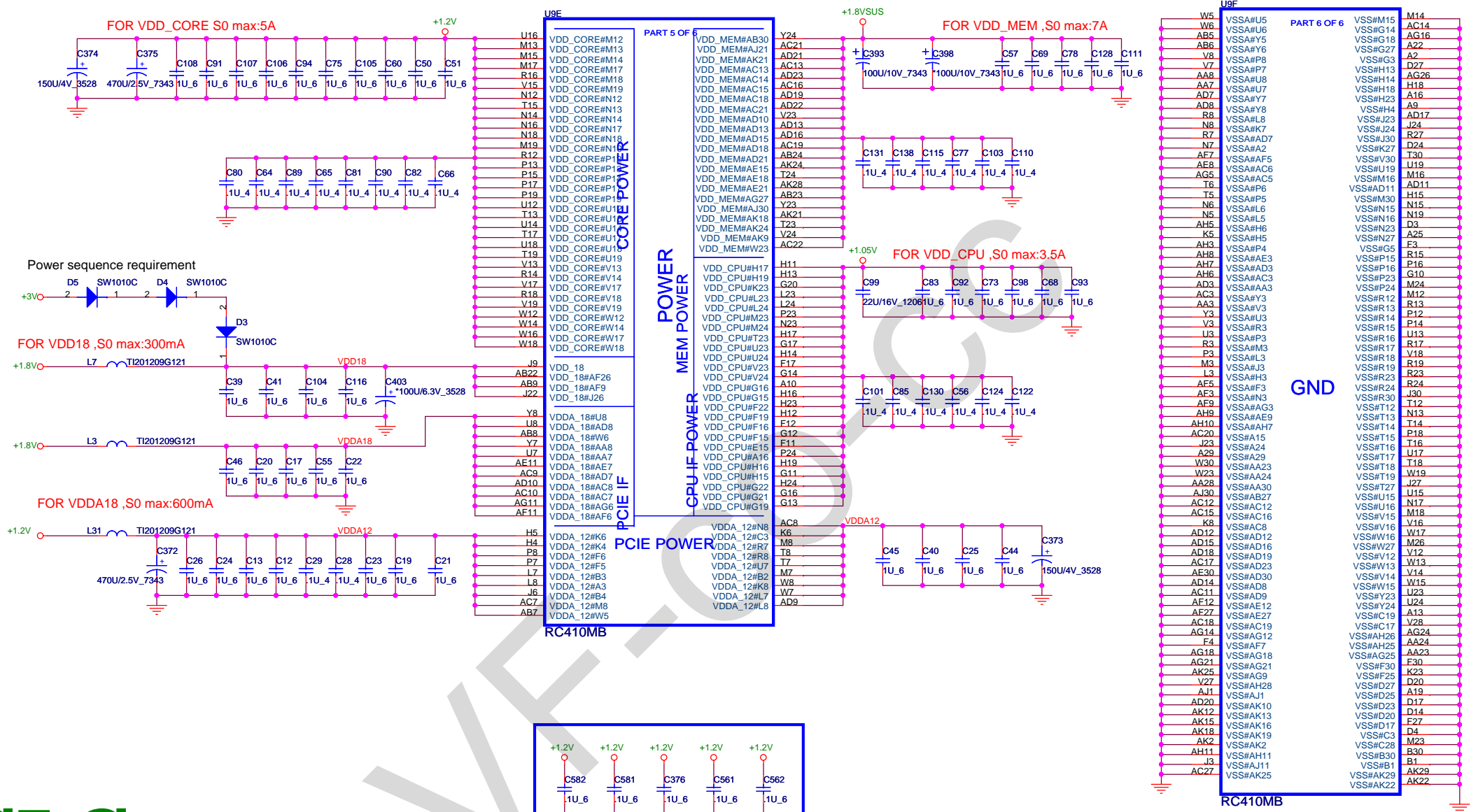
DAC\_SCL is totem-pole output

**PROJECT : BL1**

**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>RC410MB-VIDEO &amp; CLKGEN</b>	<b>2A</b>
Date:	Friday, May 05, 2006	Sheet 7 of 30

# CLG

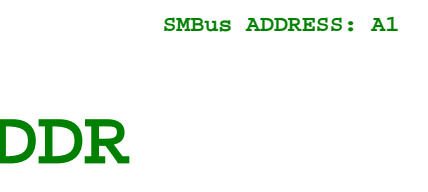
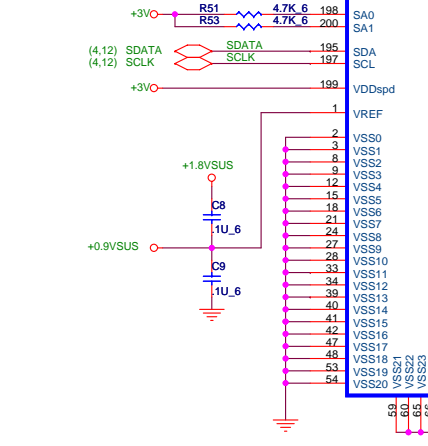
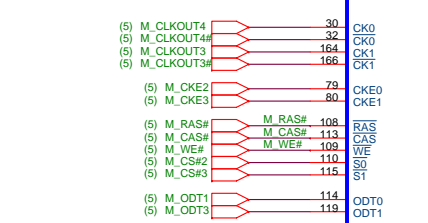
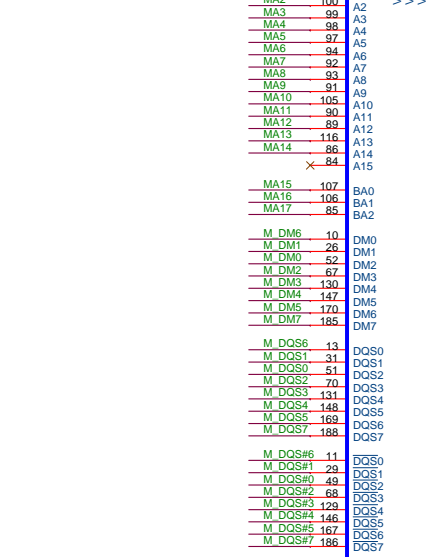
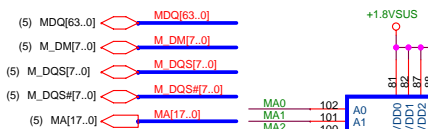


**PROJECT : BL1**

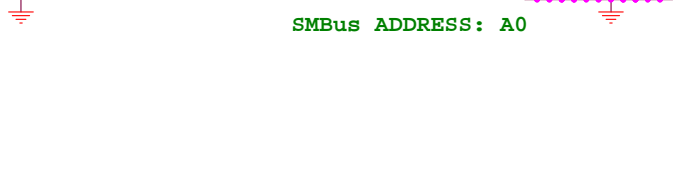
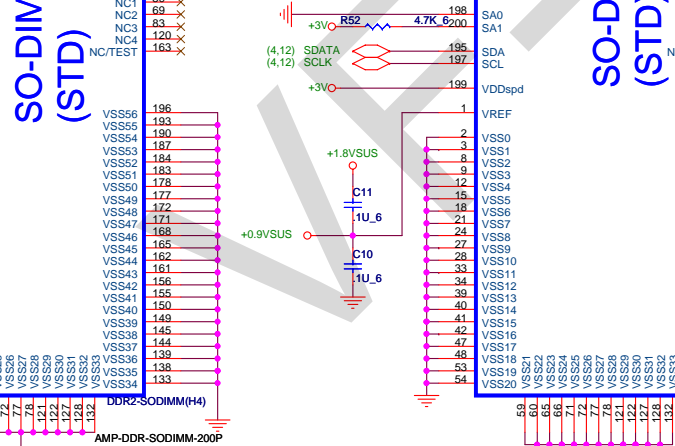
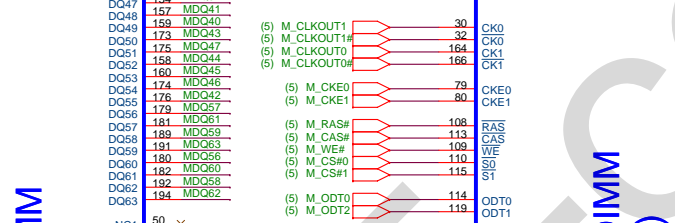
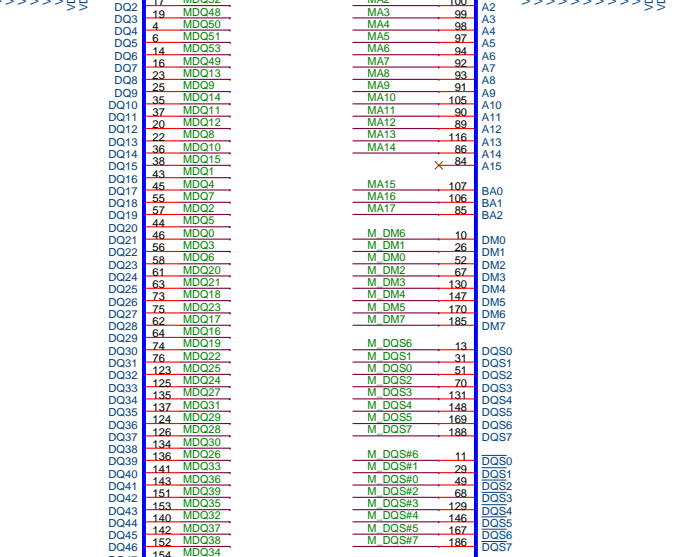
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>RC410MB-POWER</b>	1A
Date:	Thursday, April 06, 2006	Sheet 8 of 30

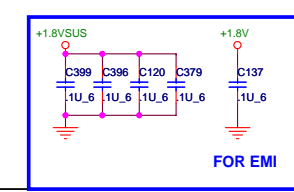
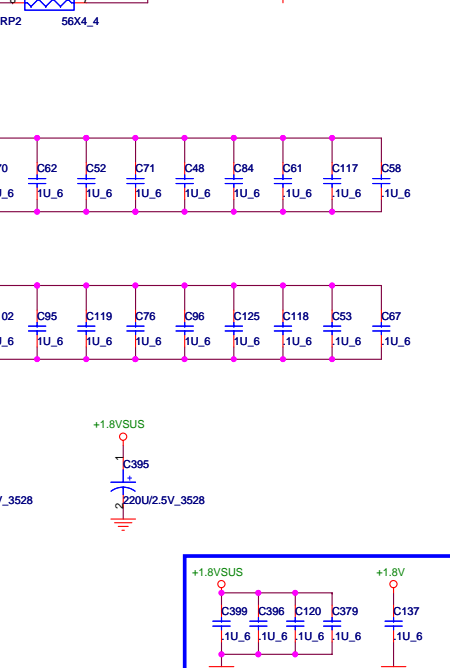
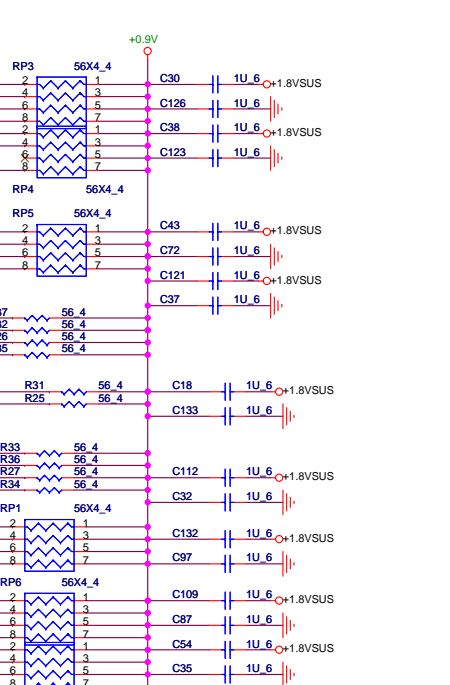
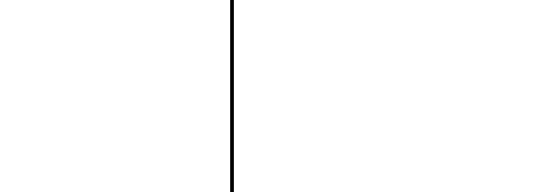
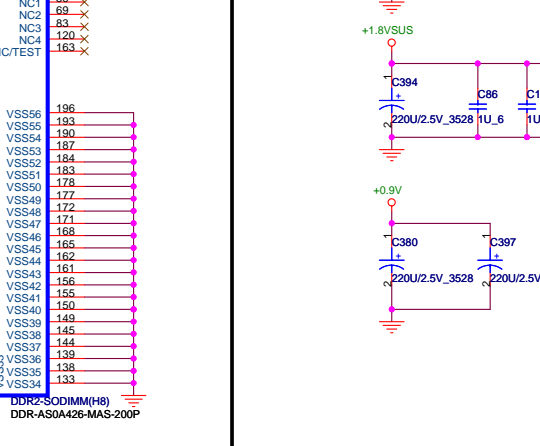
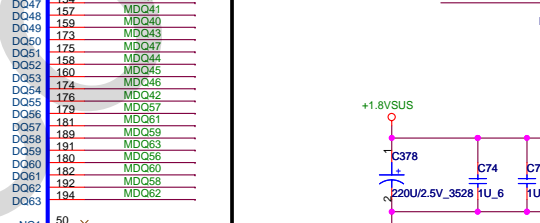
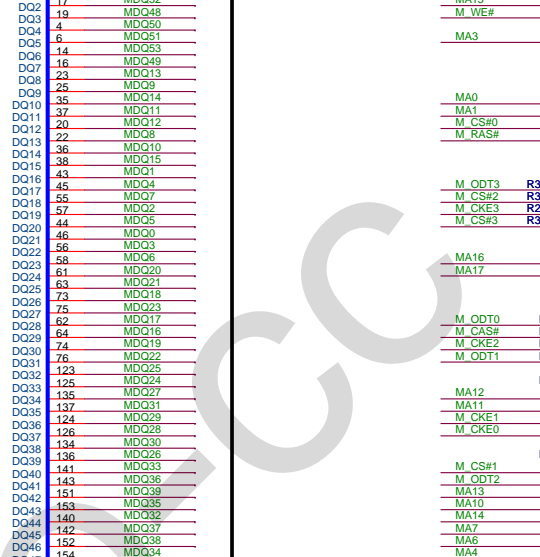




SO-DIMM (STD)



SO-DIMM (STD)

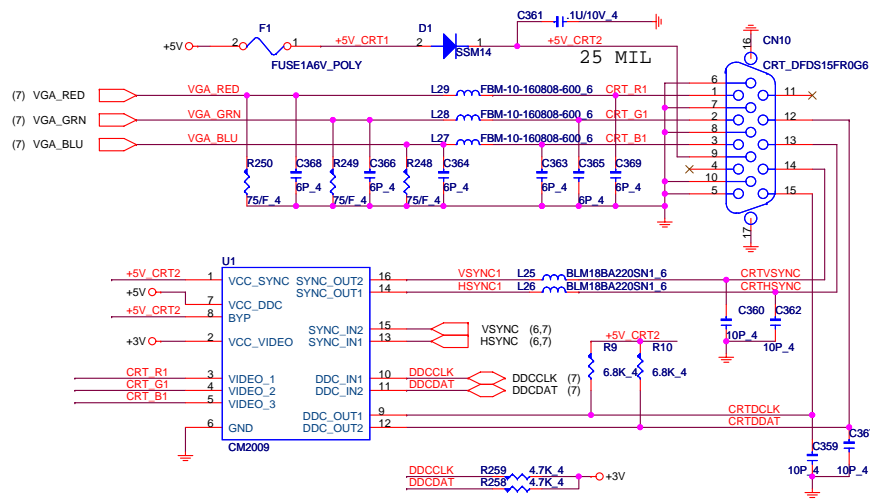


PROJECT : BL1  
 Quanta Computer Inc.

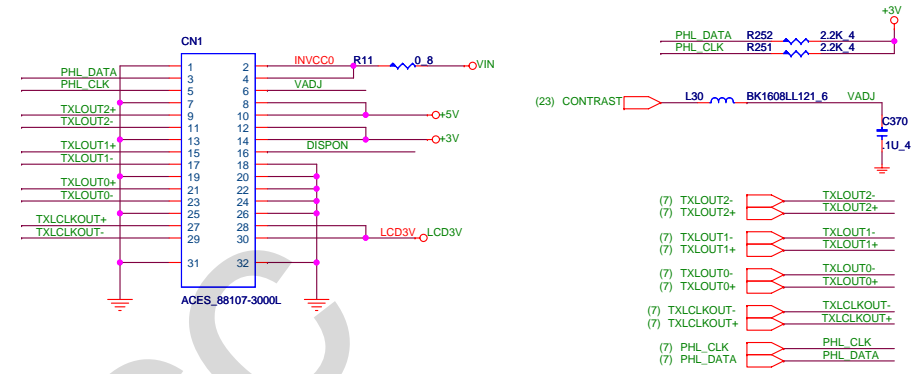
Size	Document Number	Rev
	DDR2 SO-DIMM	1A
Date:	Saturday, May 06, 2006	Sheet 9 of 30

DDR

# CRT PORT

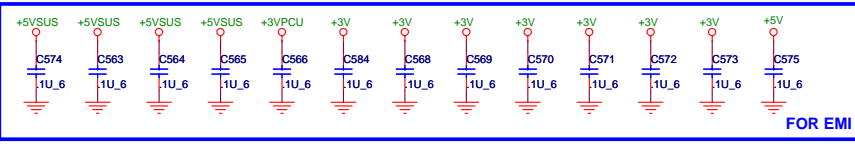
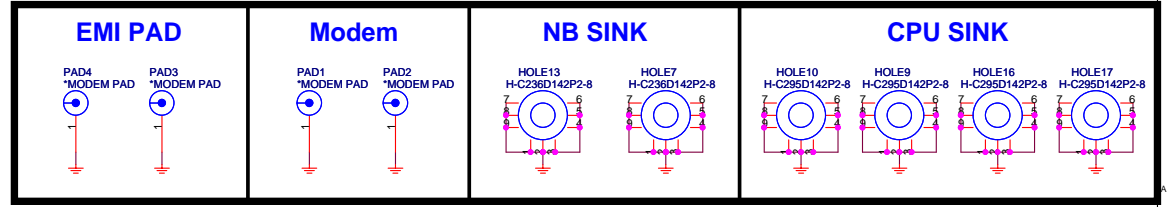
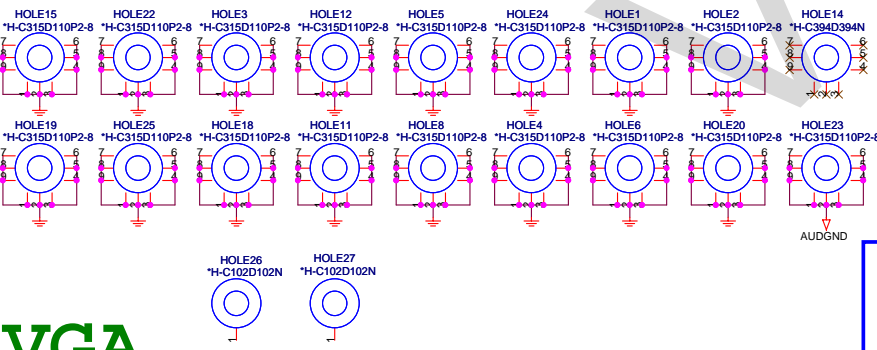
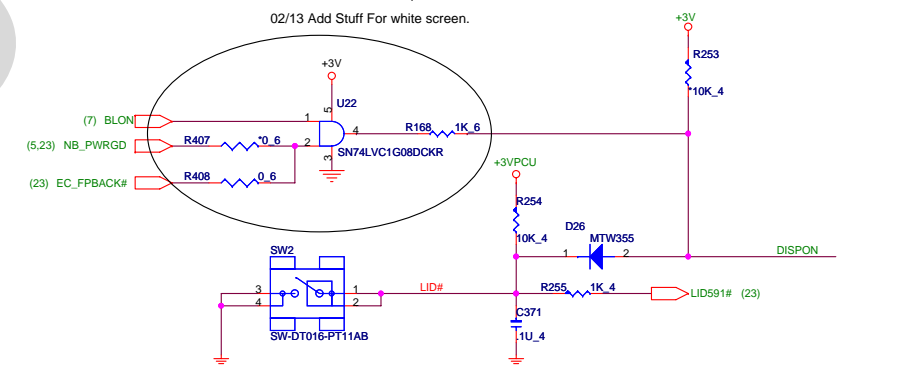


# LCD Connector



# Lid Switch

05/05 Add Resistor 1Kohm on Buffer output.  
 04/28 The Solve Boot up white line on LG LCD issue.  
 02/13 Add Stuff For white screen.



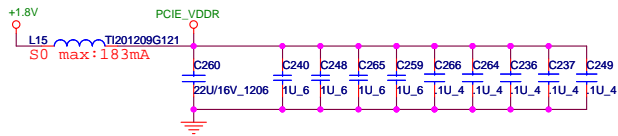
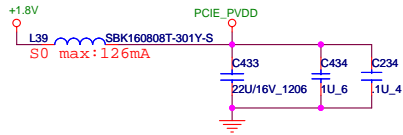
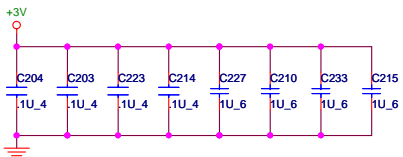
**PROJECT : BL1**  
**Quanta Computer Inc.**

Size: Document Number: **VGA Ports, LID, & HOLES** Rev: 3B  
 Date: Wednesday, May 10, 2006 Sheet: 10 of 30

**VGA**

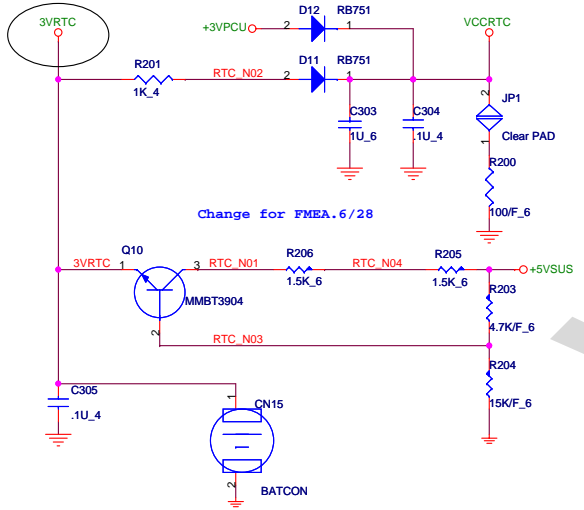
3/31 Add EMI Solution

FOR EMI

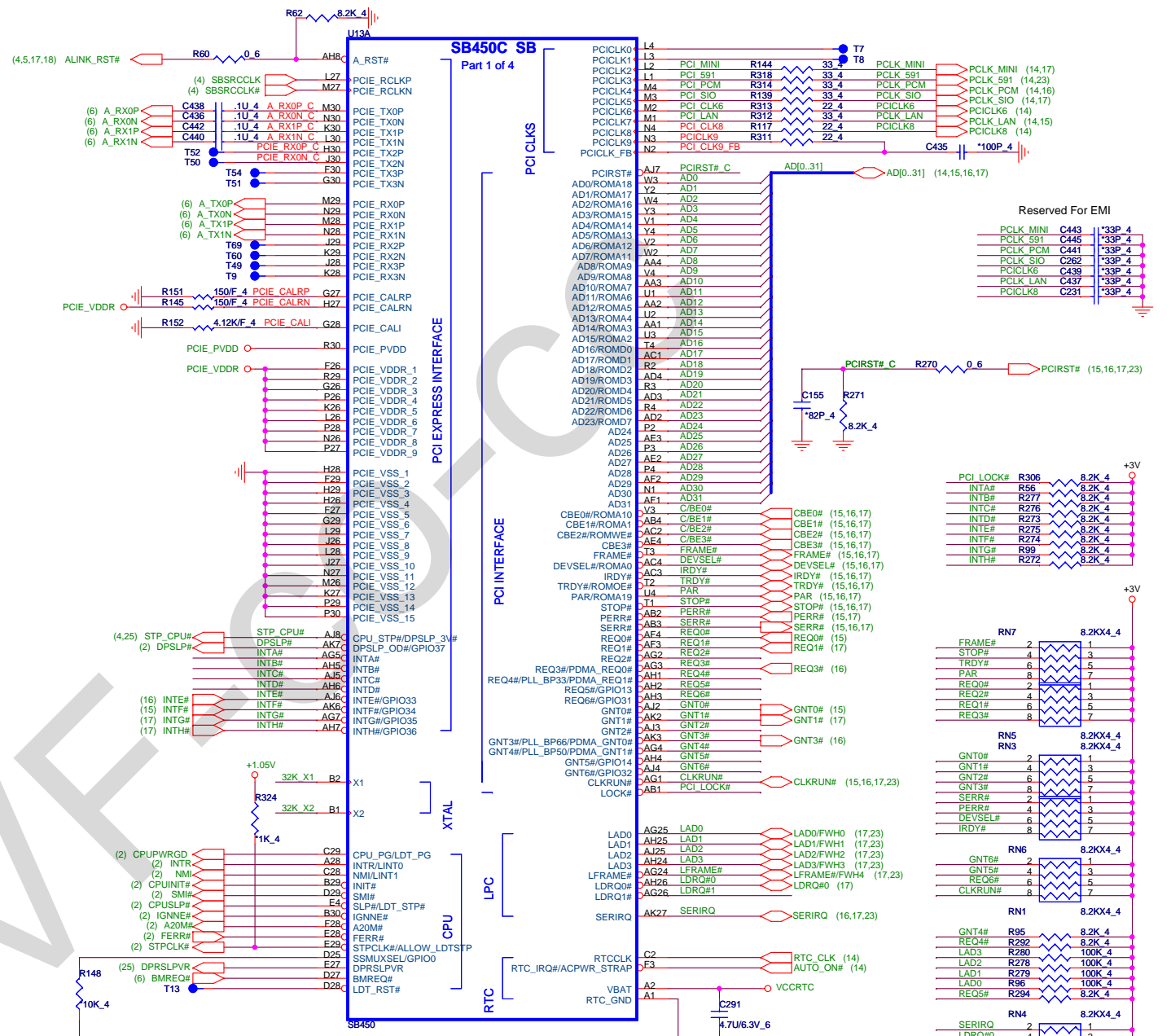


**RTC**

4/2 Battery should be connected directly - not through a UL resistor, and not through a diode.



**CLG**



Reserved For EMI

PCLK_MINI	C443	*33P_4
PCLK_S91	C445	*33P_4
PCLK_PCM	C441	*33P_4
PCLK_SIO	C262	*33P_4
PCICLK6	C439	*33P_4
PCLK_LAN	C437	*33P_4
PCICLK8	C231	*33P_4

PCI_LOCK#	R306	8.2K_4
INTA#	R56	8.2K_4
INTB#	R277	8.2K_4
INTC#	R276	8.2K_4
INTD#	R273	8.2K_4
INTE#	R275	8.2K_4
INTF#	R274	8.2K_4
INTG#	R99	8.2K_4
INTH#	R272	8.2K_4

FRAME#	RN7	8.2KX4_4
STOP#	2	1
TRDY#	6	5
PAR	8	7
REQ0#	2	1
REQ2#	4	3
REQ1#	6	5
REQ3#	8	7

GNT0#	RN5	8.2KX4_4
RN3	2	1
GNT1#	4	3
GNT2#	6	5
GNT3#	8	7
SERR#	2	1
PERR#	4	3
DEVSEL#	6	5
IRDY#	8	7

GNT6#	RN6	8.2KX4_4
GNT5#	4	3
REQ6#	6	5
CLKRUN#	8	7

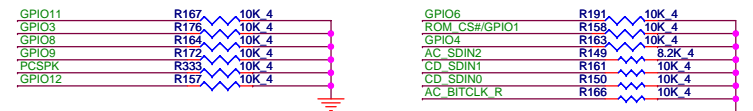
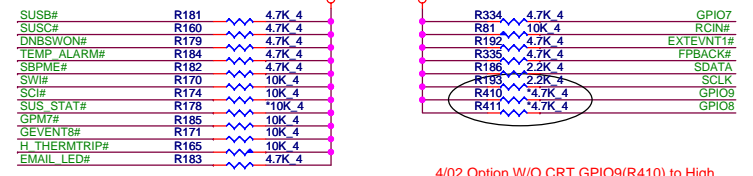
GNT4#	RN1	8.2KX4_4
REQ4#	2	1
LAD3	R280	100K_4
LAD2	R278	100K_4
LAD1	R279	100K_4
LAD0	R96	100K_4
REQ5#	R284	8.2K_4

GNT4#	RN4	8.2KX4_4
SERIRQ	2	1
LDRQ0#	4	3
LDRQ1#	6	5
CLKRUN#	8	7

**PROJECT : BL1**  
**Quanta Computer Inc.**

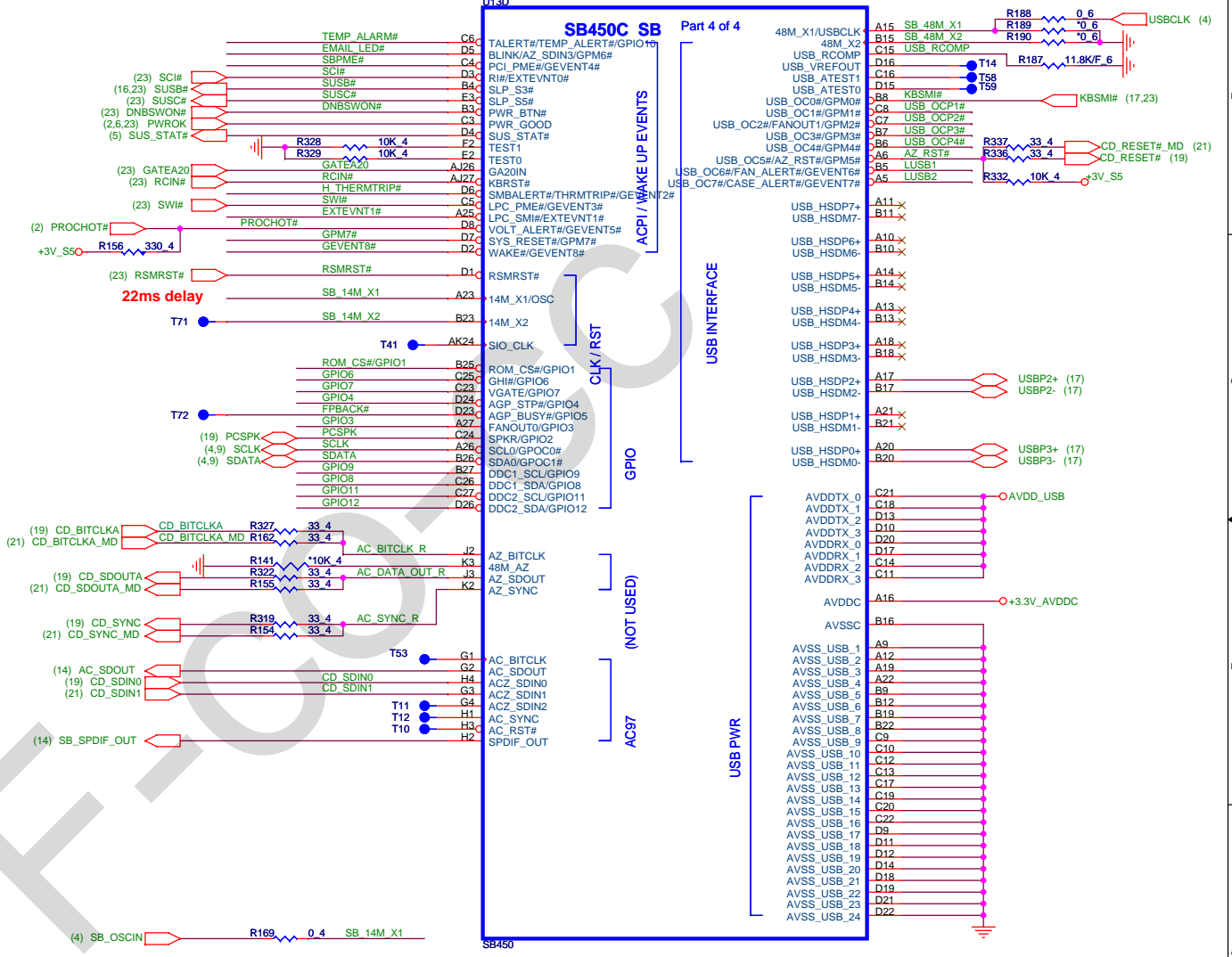
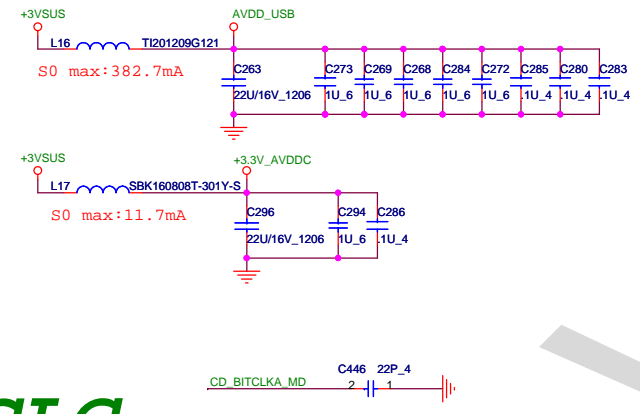
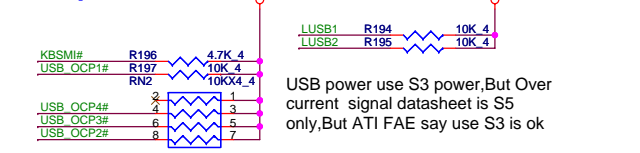
Size	Document Number	Rev
Customer	SB450C PCIE/PC/CPU/LPC/IF	1A
Date:	Friday, May 05, 2006	Sheet 11 of 30

**PU/PD**



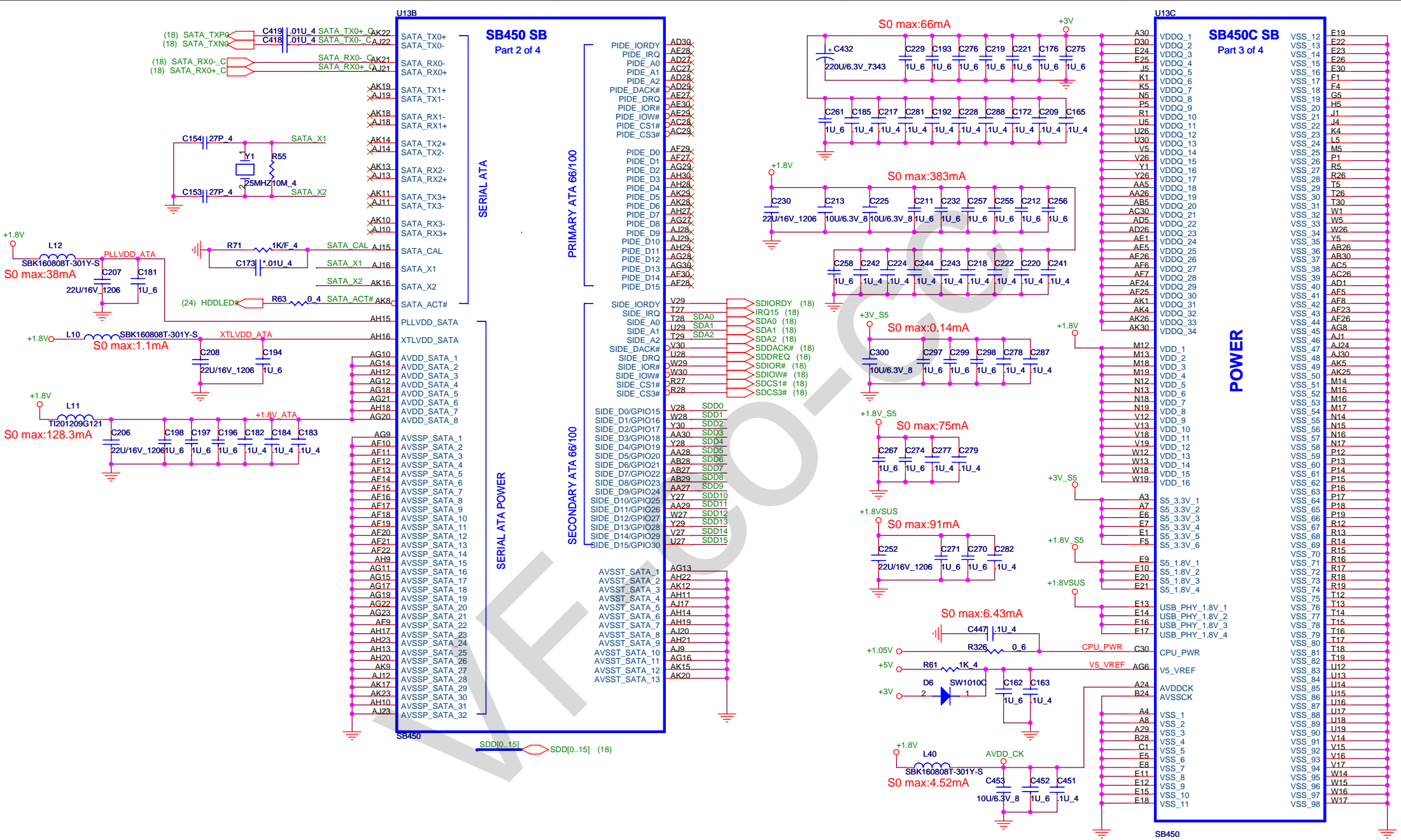
	GPIO9 PIN	GPIO8 PIN
CRT	LOW	
W/O CRT	HIGH	
Modem		LOW
W/O Modem		HIGH

**USB power**



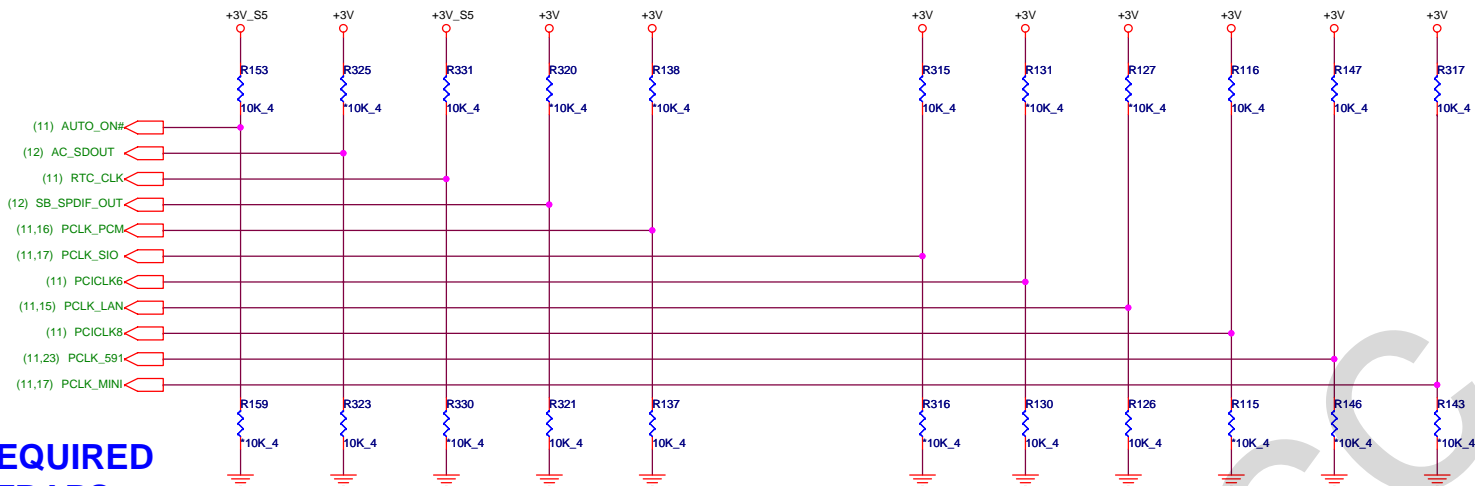
**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	SB450C ACP/GPIO/USB/AC97	3A
Date:	Monday, May 08, 2006	Sheet 12 of 30



**PROJECT : BL1**  
**Quanta Computer Inc.**

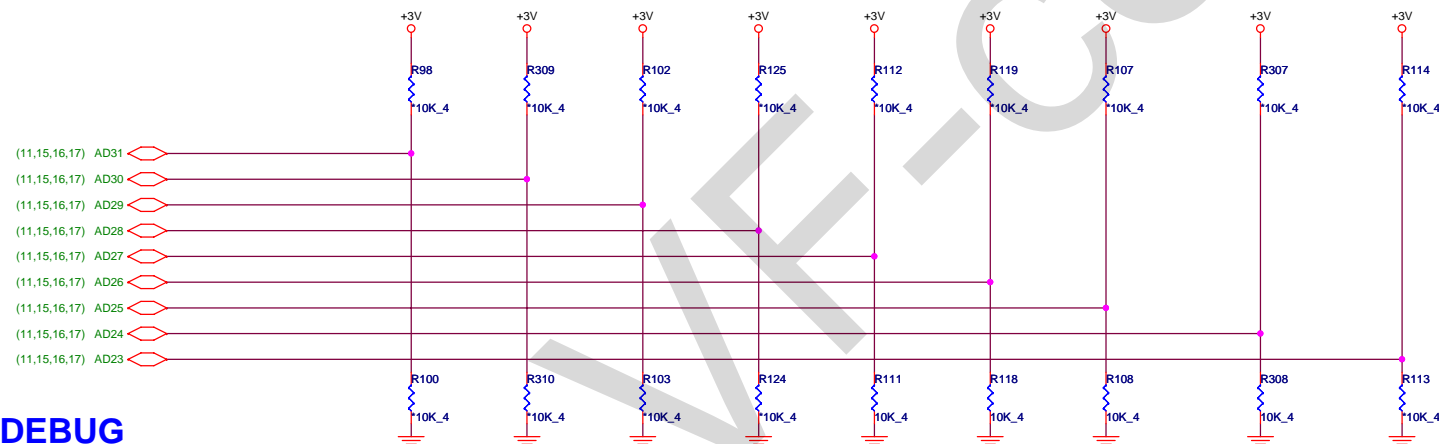
Size	Document Number	Rev
Custom	<b>SB450C HDD/POWER/DECOUPLING</b>	1A
Date:	Monday, May 08, 2006	Sheet 13 of 30



## REQUIRED STRAPS

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCLK_PCM	PCLK_SIO	PCI_CLK6	PCLK_LAN	PCI_CLK8	PCLK_591	PCLK_MINI*
<b>PULL HIGH</b>	MANUAL PWR ON <b>DEFAULT</b>	USE DEBUG STRAPS	INTERNAL RTC <b>DEFAULT</b>	SIO 24MHz	48MHz use Internal PLL	14MHz OSC MODE <b>DEFAULT</b>	CPU I/F = K8	H,H = PCI(X BUS) ROM L,L = LPC ROM I (LPC addresses are translated to the top of the 4G address space)		USB PHY PWRDOWN DISABLE <b>DEFAULT</b>	48MHz Crystal Pad <b>DEFAULT</b>
<b>PULL LOW</b>	AUTO PWR ON	IGNORE DEBUG STRAPS <b>DEFAULT</b>	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz <b>DEFAULT</b>	48MHz use External Clock <b>DEFAULT</b>	14MHz XTAL MODE	CPU I/F = P4 <b>DEFAULT</b>	L,H = LPC ROM II (addresses mapped to below 1M) L,L = FWH ROM		USB PHY PWRDOWN ENABLE	48MHz OSC/Clock Buffer

\*This strap is only required if the strap on PCICLK4 is configured for External Clock.



## DEBUG STRAPS

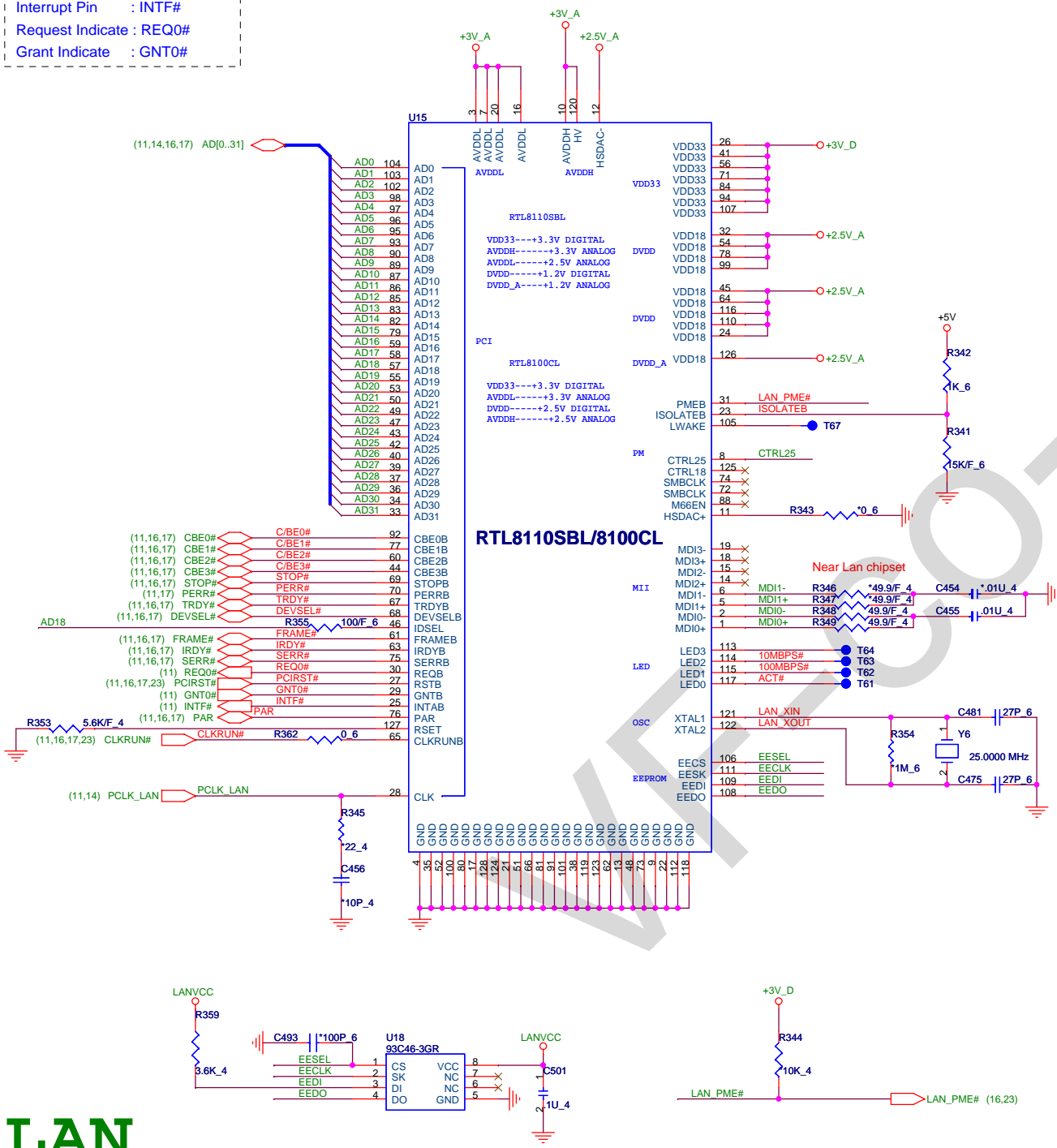
	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
<b>PULL HIGH</b>	USE LONG RESET <b>DEFAULT</b>	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
<b>PULL LOW</b>	USE SHORT RESET					USE PCI PLL <b>DEFAULT</b>	USE ACPI BCLK <b>DEFAULT</b>	USE IDE PLL <b>DEFAULT</b>	USE DEFAULT PCIE STRAPS <b>DEFAULT</b>	

**CLG**

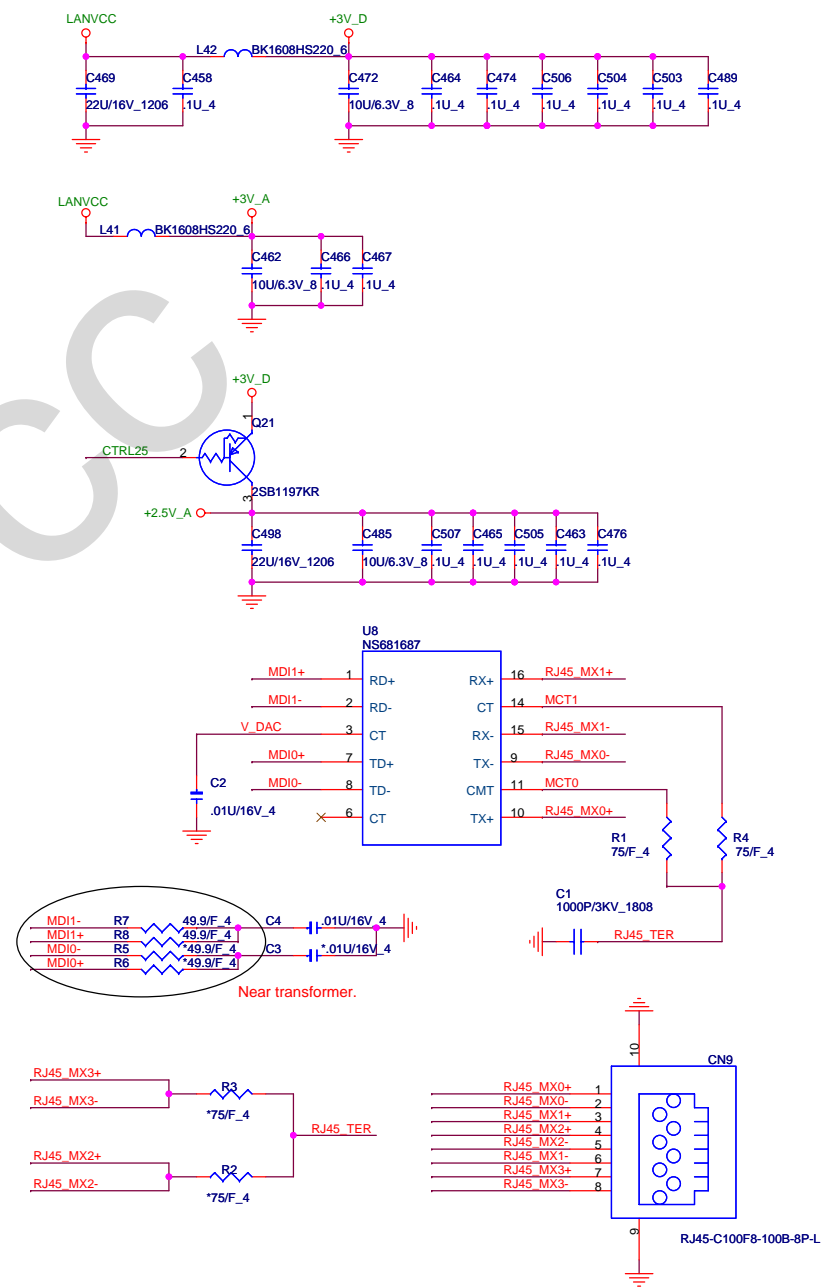
**PROJECT : BL1**  
**Quanta Computer Inc.**

Size Custom	Document Number	Rev 1A
<b>SB450C STRAPS</b>		
Date: Monday, April 03, 2006	Sheet 14 of 30	

ID Select : AD18  
 Interrupt Pin : INTF#  
 Request Indicate : REQ0#  
 Grant Indicate : GNT0#



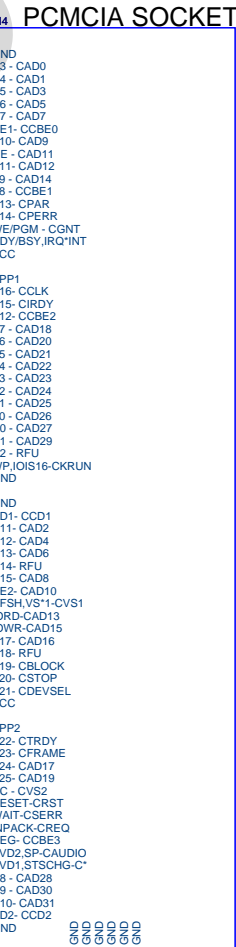
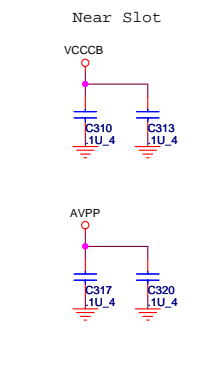
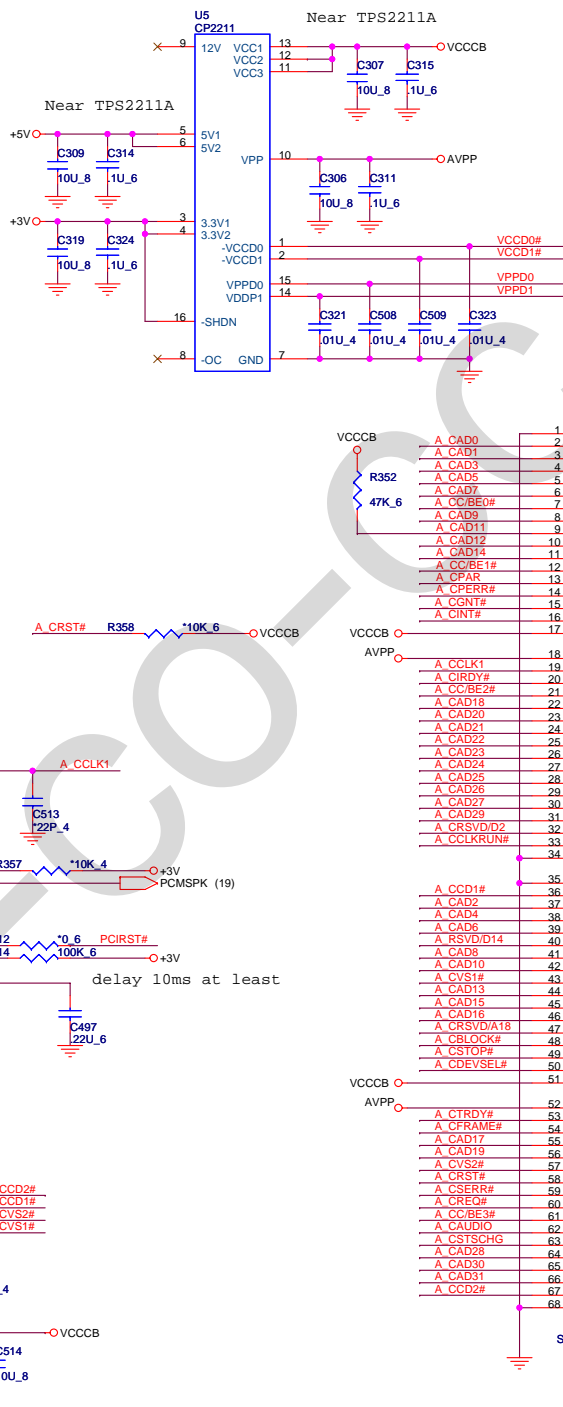
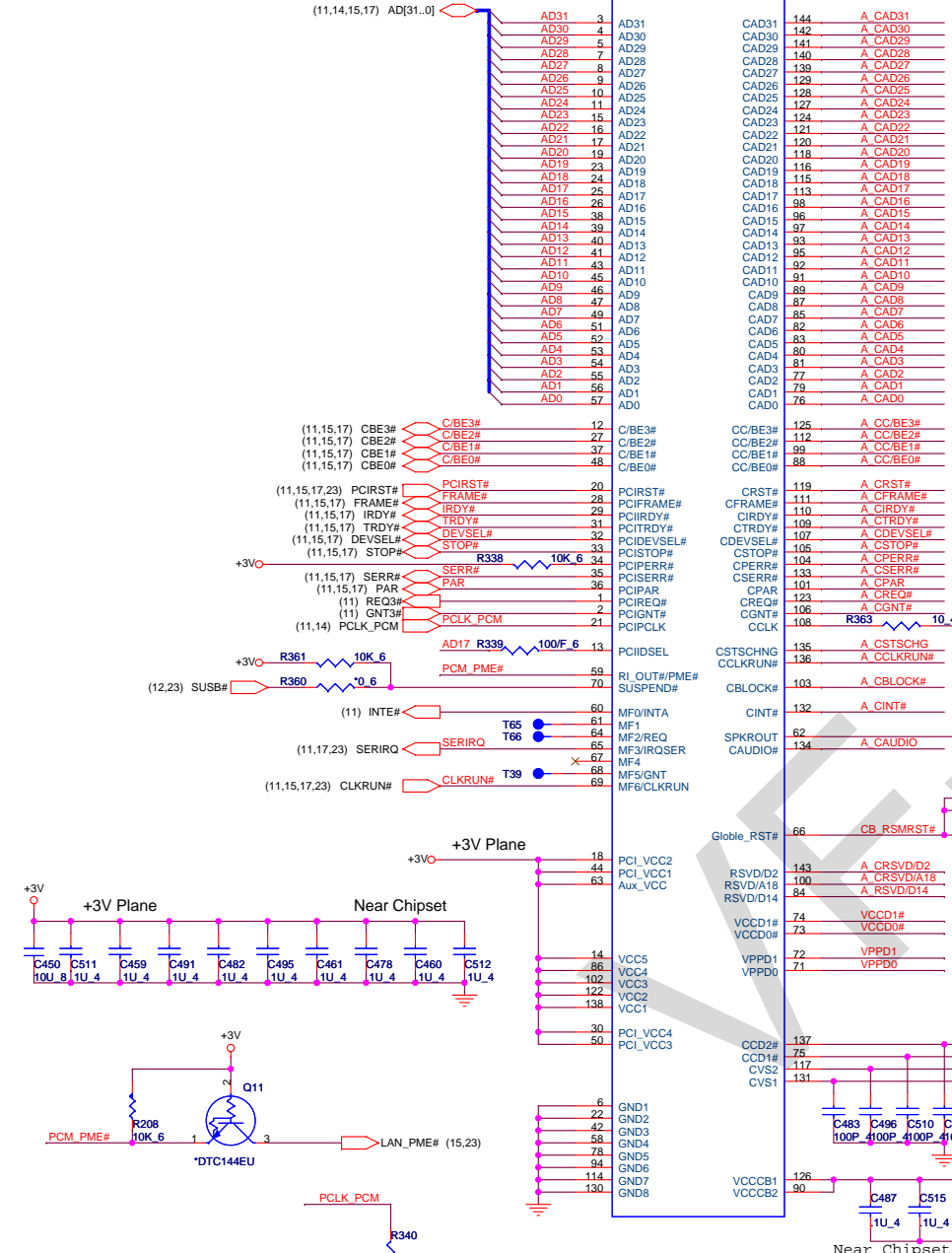
**LAN**



**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>LAN RTL8110SBL/8100CL</b>	1A
Date:	Saturday, May 06, 2006	Sheet 15 of 30

ID Select : AD17  
 Interrupt Pin : INTE#  
 Request Indicate : REQ3#  
 Grant Indicate : GNT3#



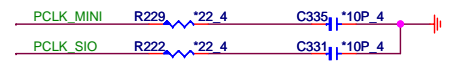
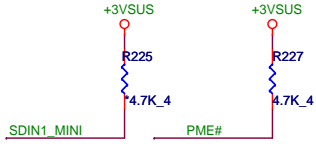
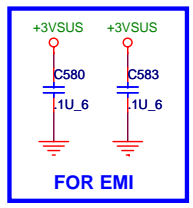
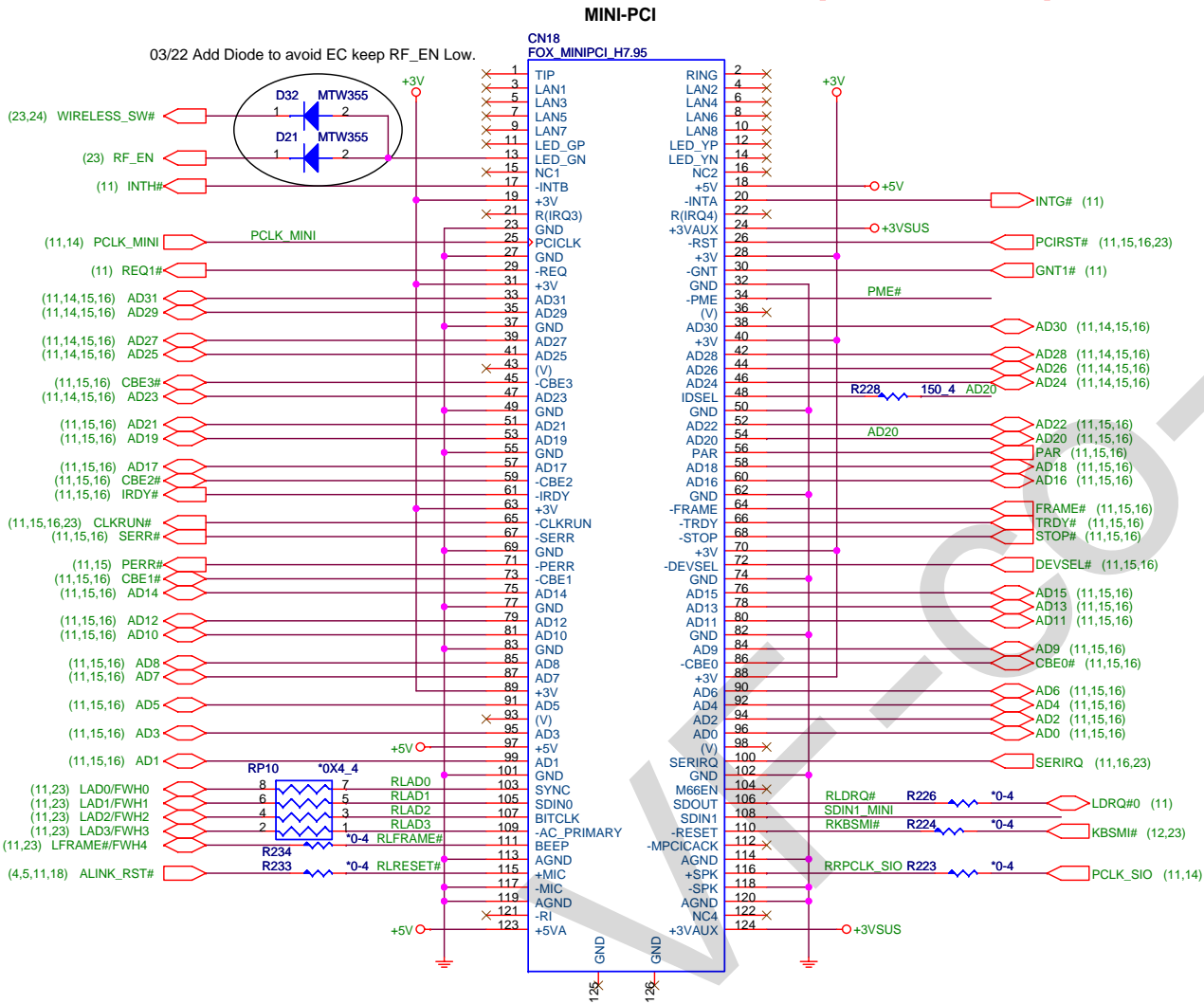
**PROJECT : BL1**  
**Quanta Computer Inc.**

Size Document Number  
**PCMCIA(CB1410)-OPTION**

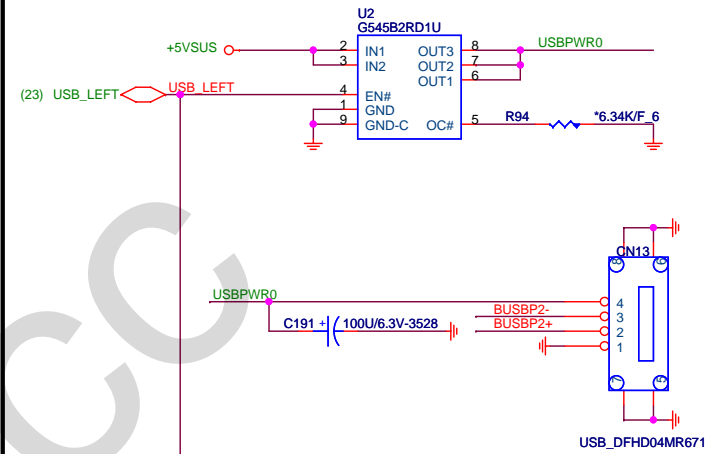
Date: Friday, April 28, 2006 Sheet 16 of 30 Rev 1A



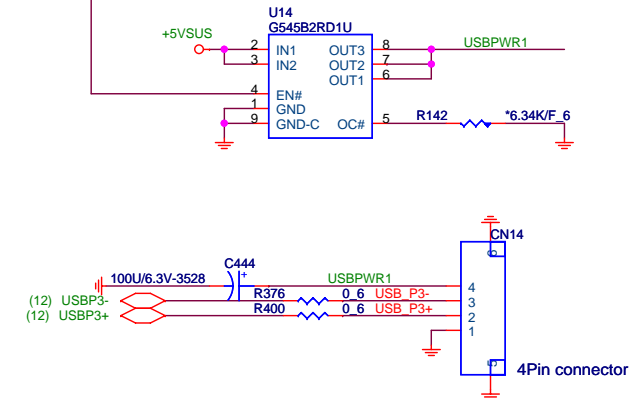
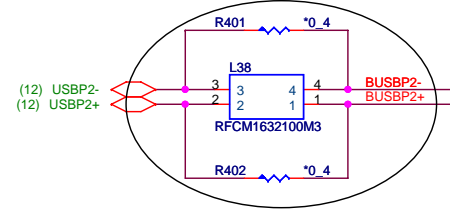
ID Select : AD20  
 Interrupt Pin : INTG# , INTH#  
 Request Indicate : REQ1#  
 Grant Indicate : GNT1#



# USB



02/24 Add 0ohm jumper

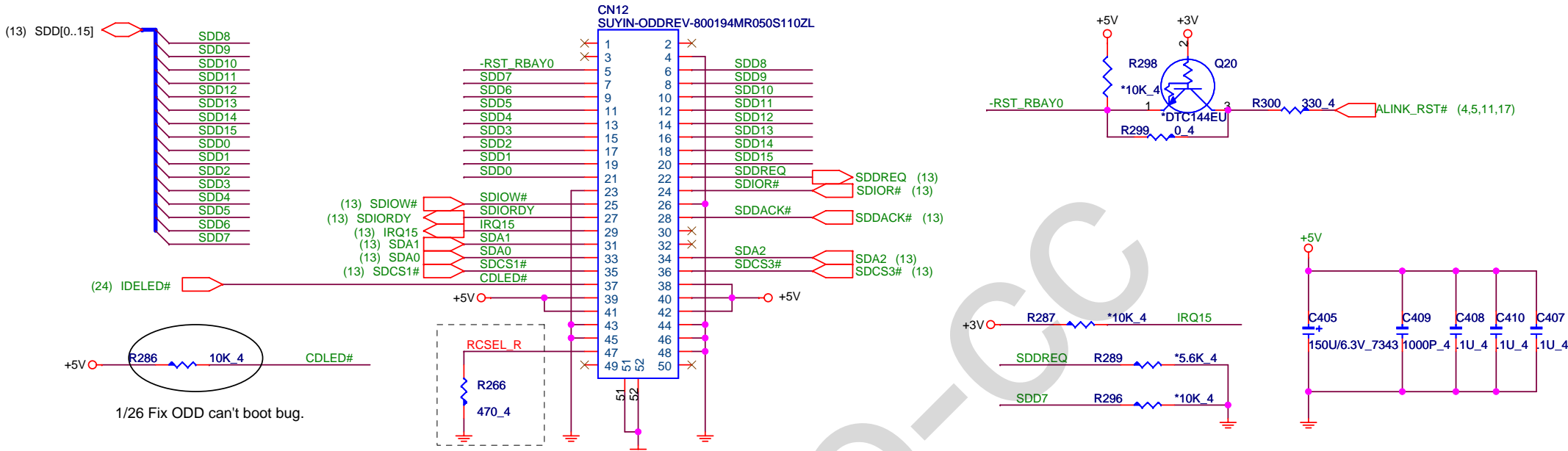


04/28 Del Reserved the Second USB Port.

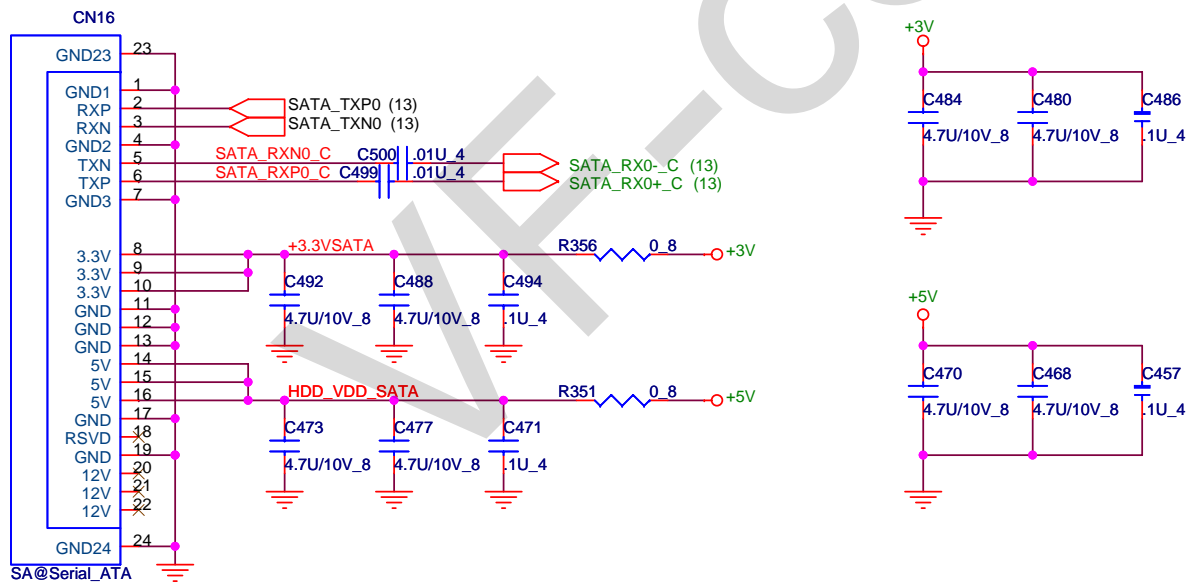


PROJECT : BL1  
 Quanta Computer Inc.

# ODD CONN



# SATA HDD CONN



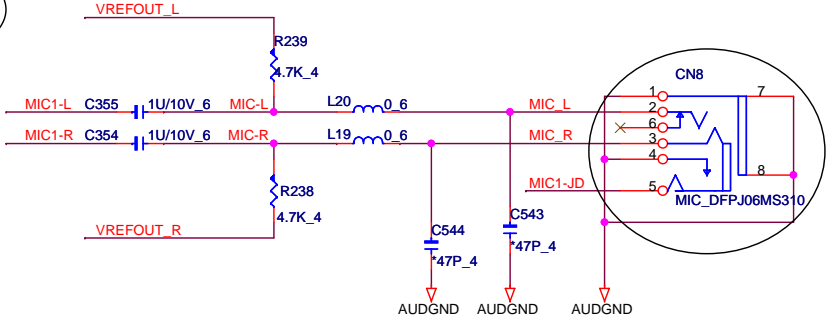
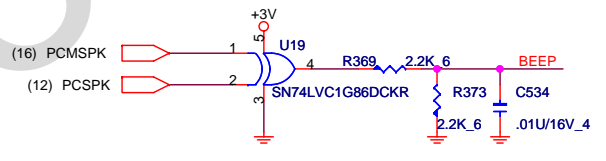
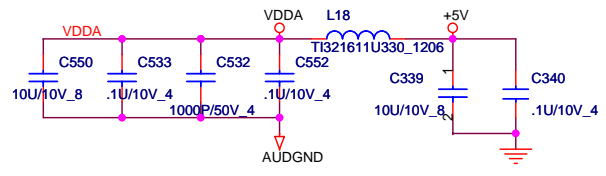
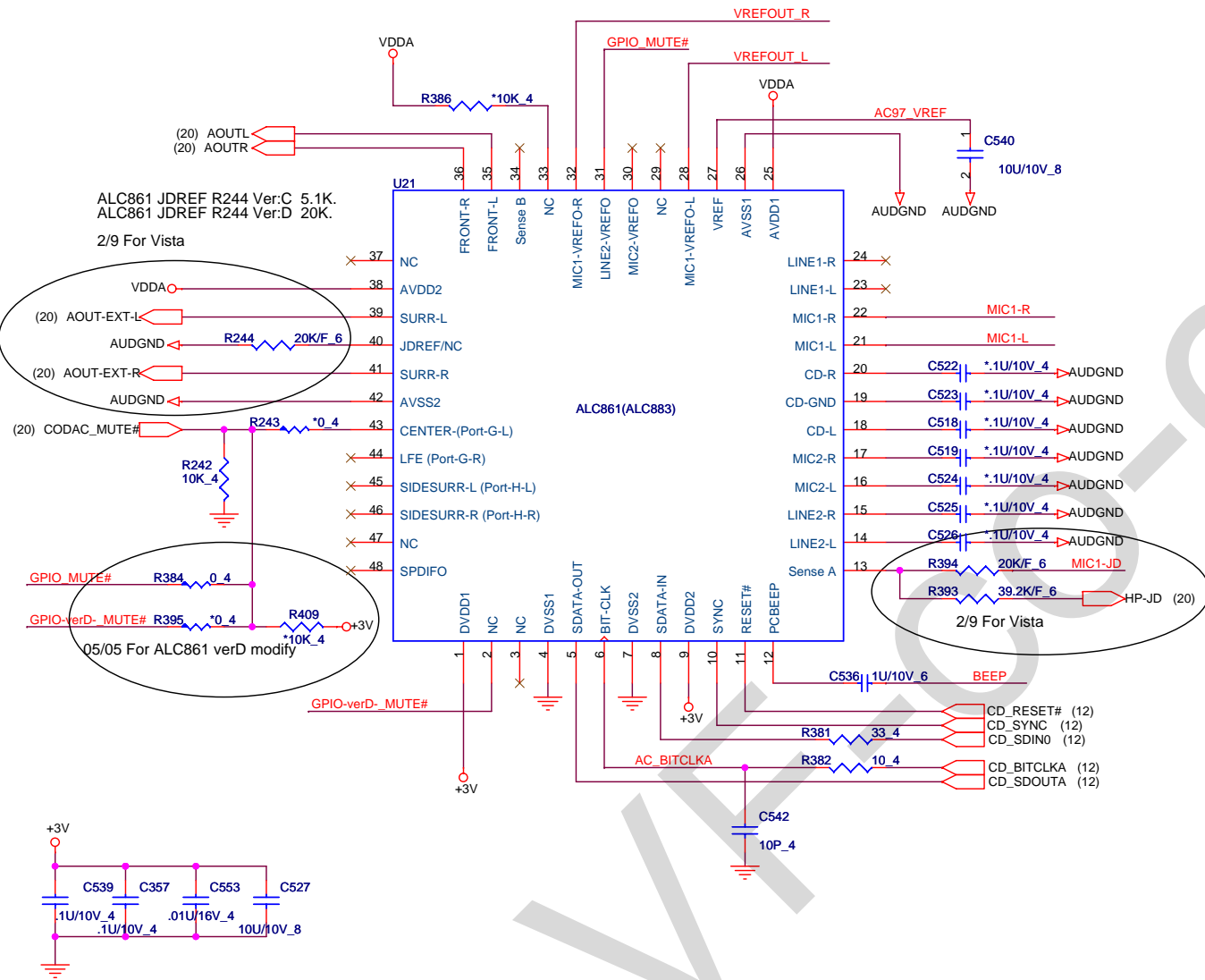
**IDE**




**PROJECT : BL1**  
**Quanta Computer Inc.**

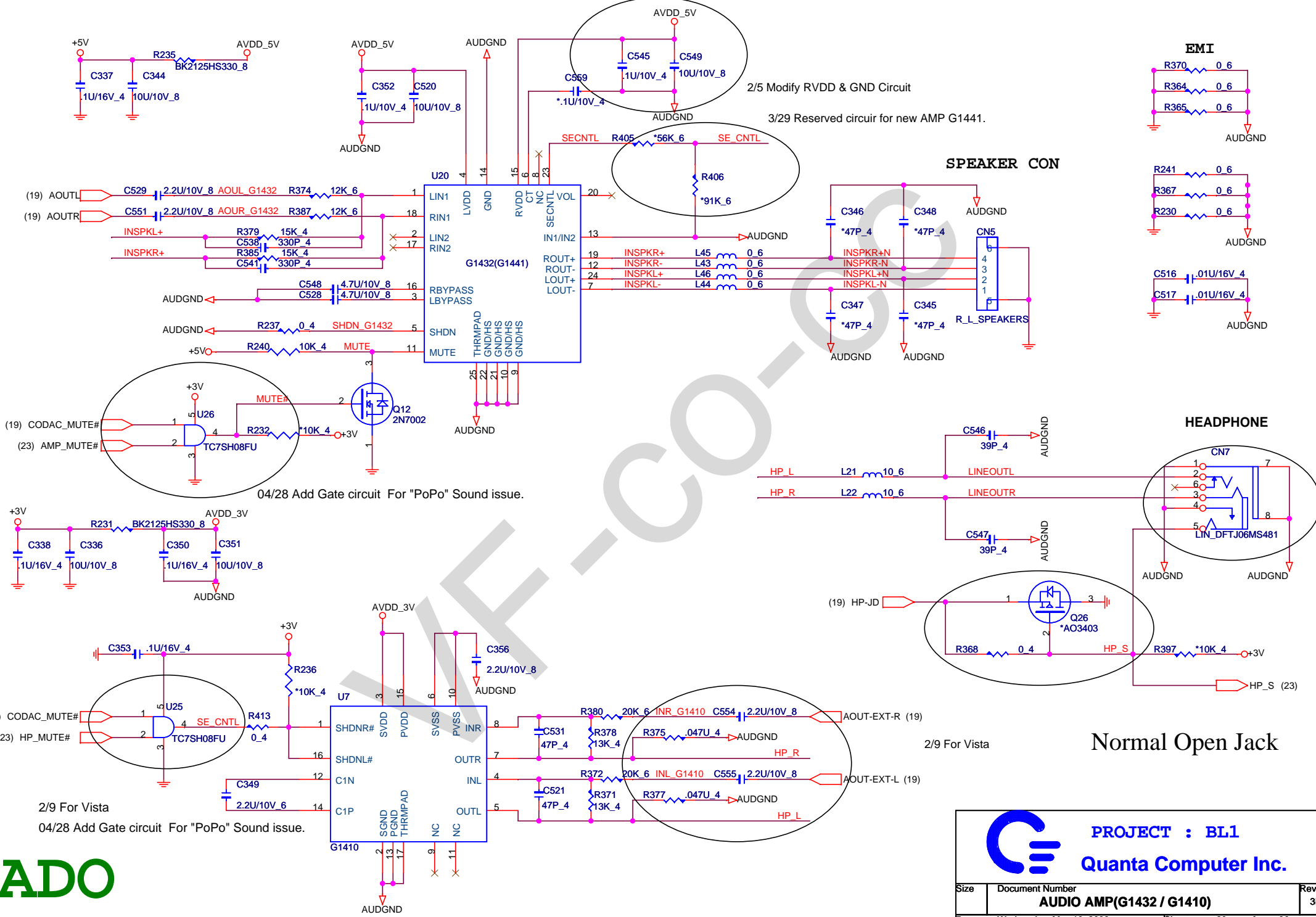
Size	Document Number	Rev
	<b>HDD &amp; CDROM</b>	2A
Date:	Monday, May 08, 2006	Sheet 18 of 30

**ADO**



Normal Open Jack

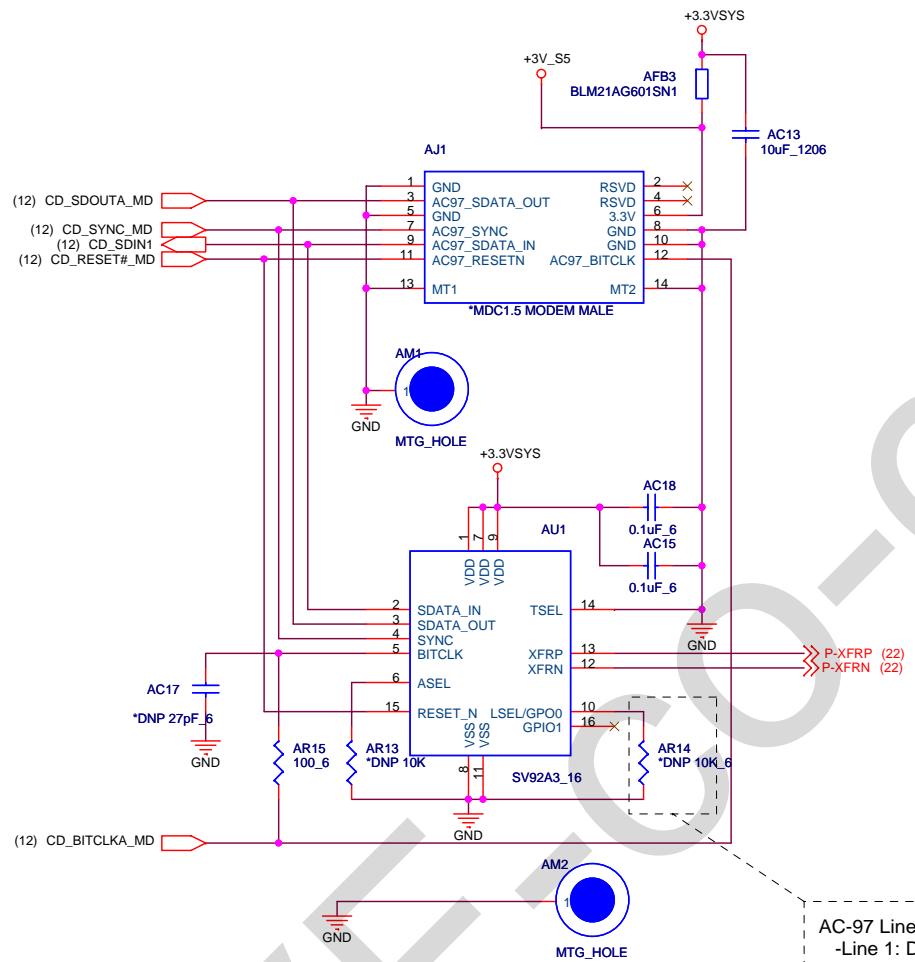
		PROJECT : BL1	
		Quanta Computer Inc.	
Size	Document Number	Rev 2A	
	<b>REALTEK ALC861</b>		
Date:	Friday, May 05, 2006	Sheet	19 of 30



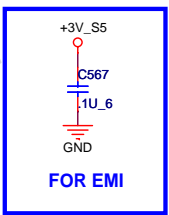
**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>AUDIO AMP(G1432 / G1410)</b>	<b>3B</b>
Date:	Wednesday, May 10, 2006	Sheet 20 of 30

**MDM**



AC-97 Line Select:  
 -Line 1: DNP R14  
 -Line 2:  
 POPULATE R14



**Agere Systems**  
 Holmdel NJ

Design Engineer: C. Russo

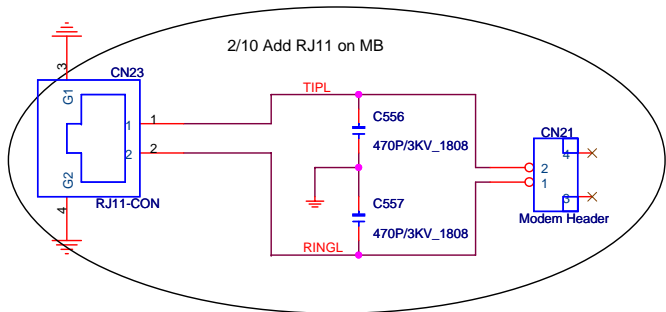
Title: **DELPHI SV92A3 MDC 1.5 Reference Design**

Size B Document Number **DIGITAL INTERFACE** Rev 1A

Date: Friday, April 28, 2006 Sheet 21 of 30

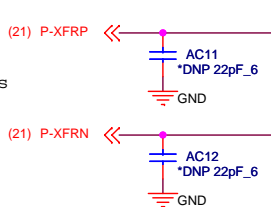
Agere Systems Proprietary  
 DRAFT COPY - FOR REVIEW ONLY  
 SUBJECT TO CHANGE





2/10 Add RJ11 on MB

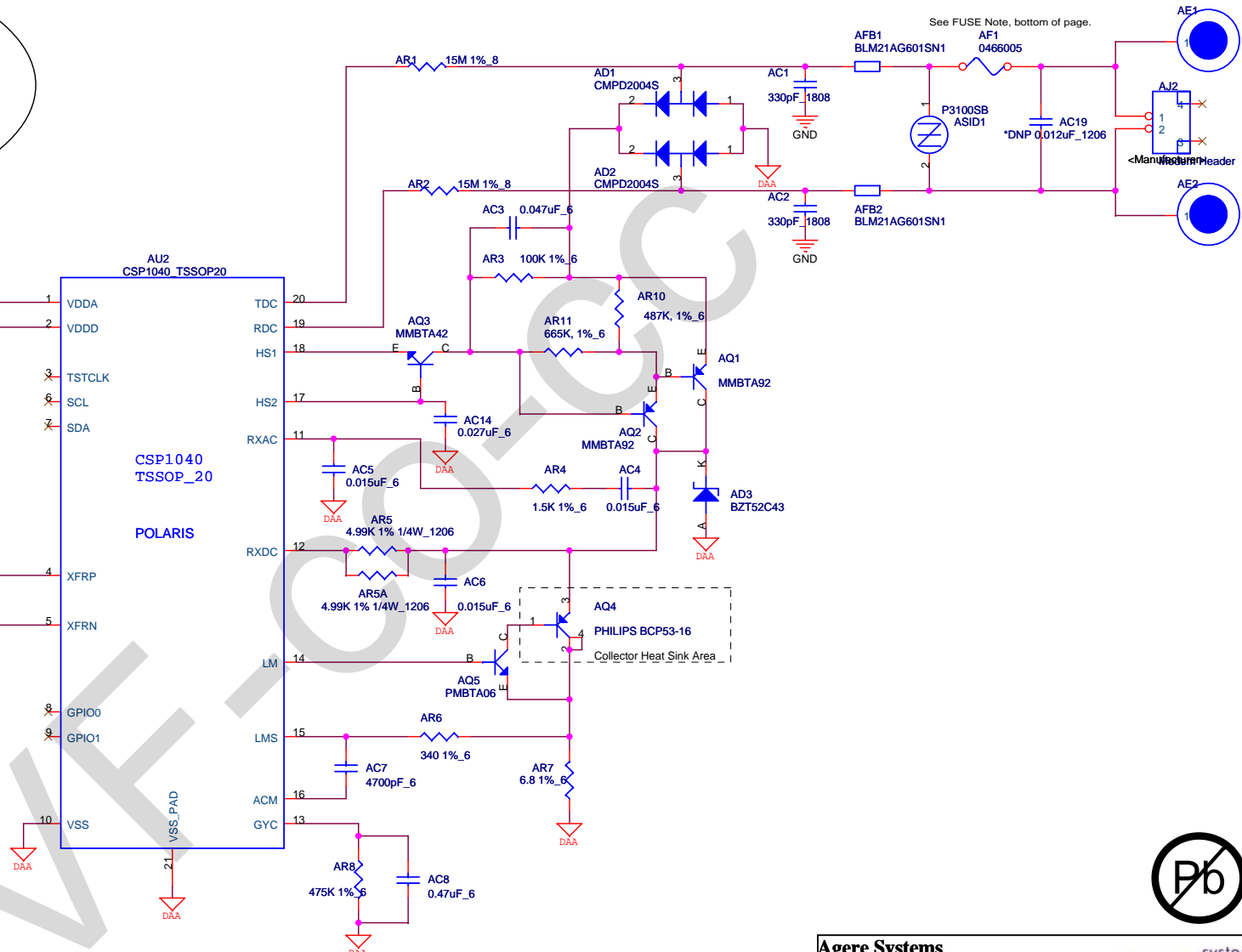
Locate C11, C12 as close to digital device as possible.



**MDM**

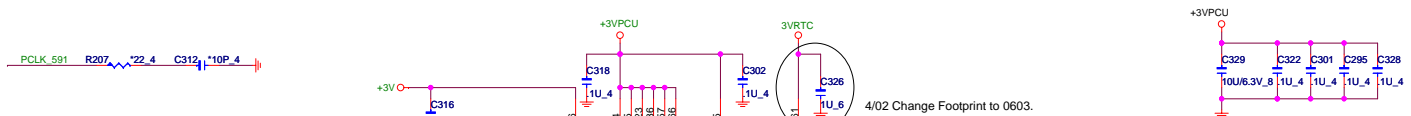
**FUSE Note:**  
The UL standard UL 1950 dictates the use of a fuse (needed to pass the M1, 600 V, 40A, 1.5 sec) to prevent component flaming during the overvoltage test. Unless one can insure that the modem is in a fire enclosure and provide 26 gauge line cord (acts as a fuse), a fusing element would be required.

Alternatively, if a TNV-1 flame resistant material is used, either as a wrap or cover over the DAA portion of the modem, this could satisfy both overvoltage protection and the separation requirement also contained in UL 1950. This latter requirement provides isolation such that unearthed parts of the DAA cannot be touched by a test finger or test probe.



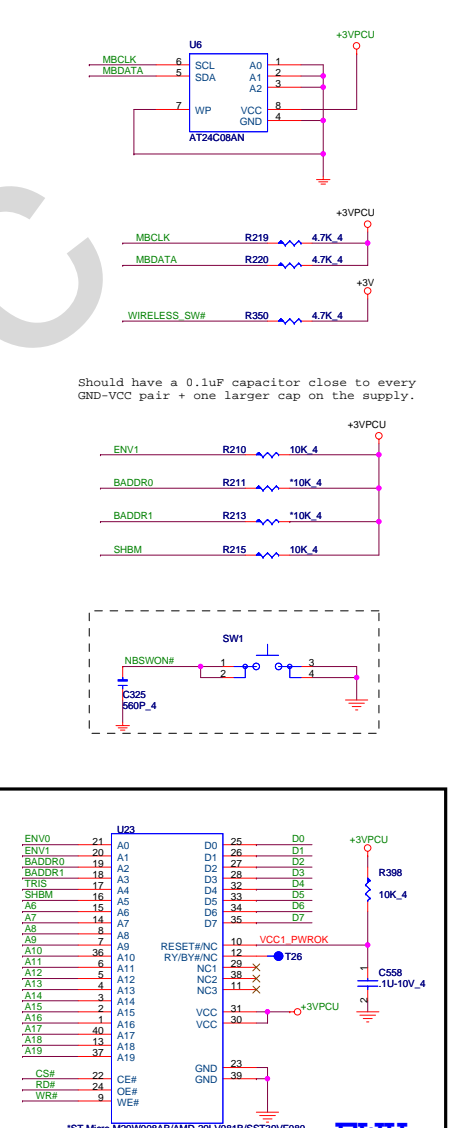
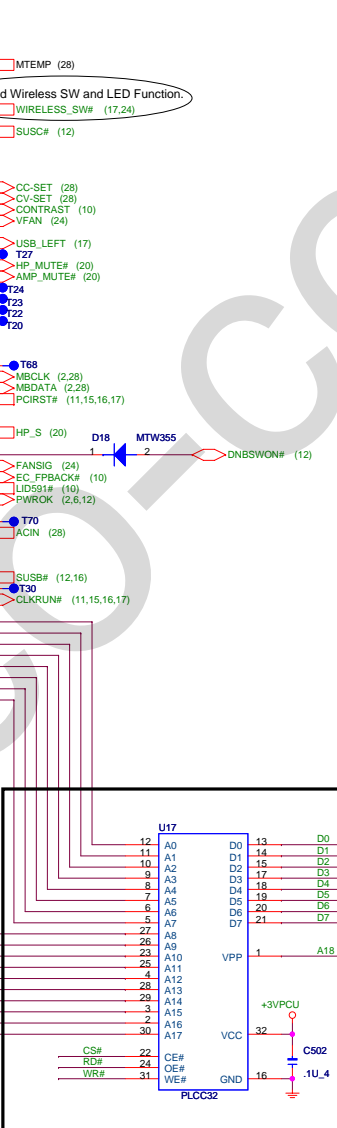
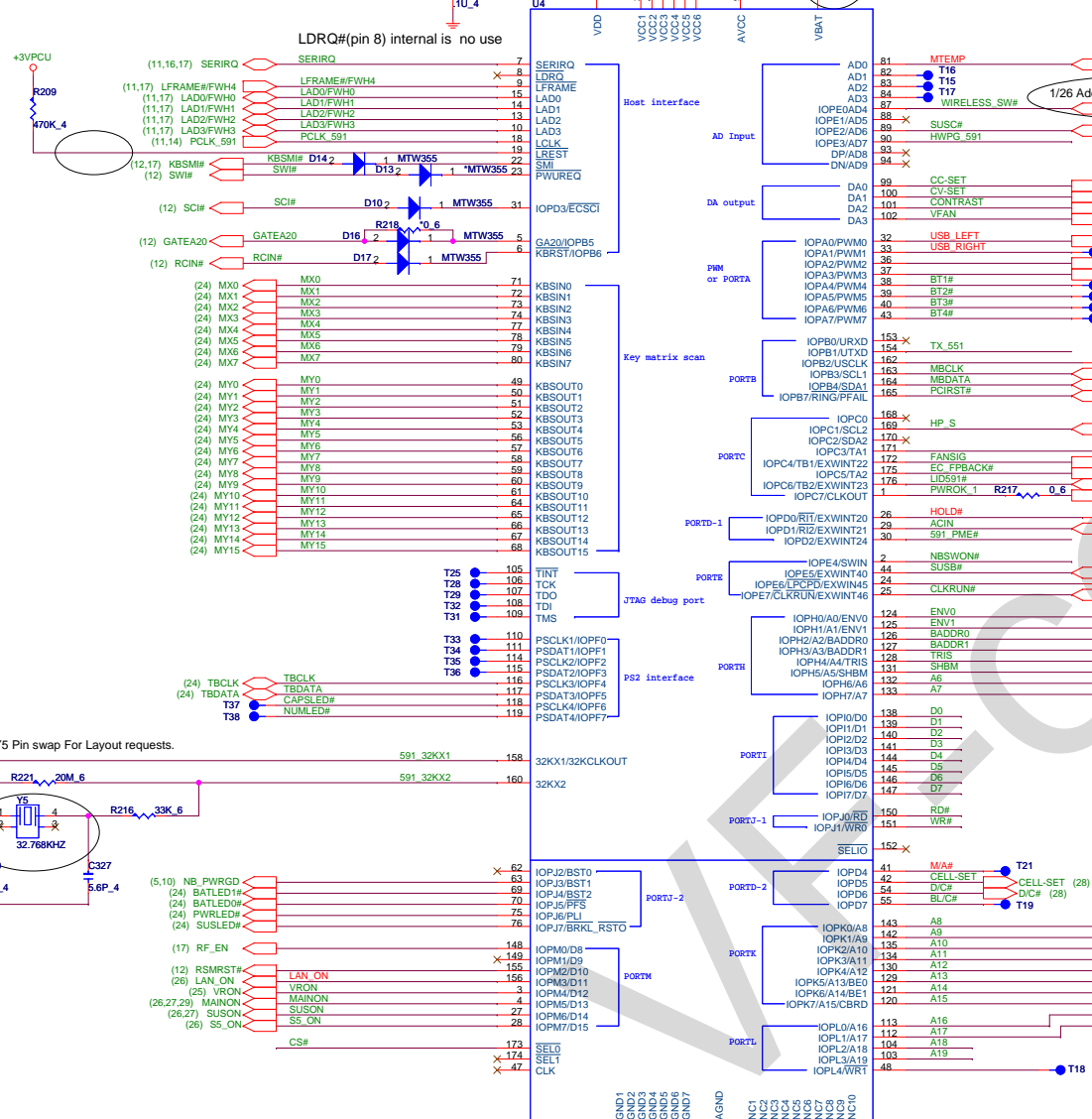
<b>Agere Systems</b> Holmdel NJ			
Design Engineer: R. Trevino			
Title <b>DELPHI SV92A3 MDC 1.5 Reference Design</b>			
Size B	Document Number <b>CSP1040 DAA</b>	Rev 2A	
Date:	Saturday, May 06, 2006	Sheet	22 of 30

Agere Systems Proprietary  
DRAFT COPY - FOR REVIEW ONLY  
SUBJECT TO CHANGE



SHBM=1: Enable shared memory with host BIOS

BADDR1-0	Index	Data
0 0	3F	3F
0 1	4E	4F
1 0	[HC]FPBAH, [HC]GPBAL, [HC]FPBAH, [HC]GPBAL+1	
1 1	Reserved	



PROJECT : BL1  
Quanta Computer Inc.

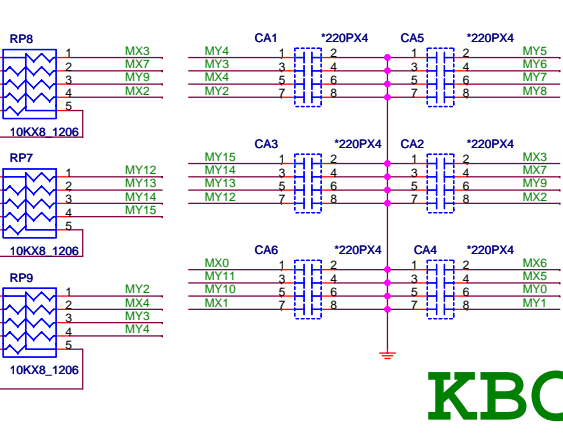
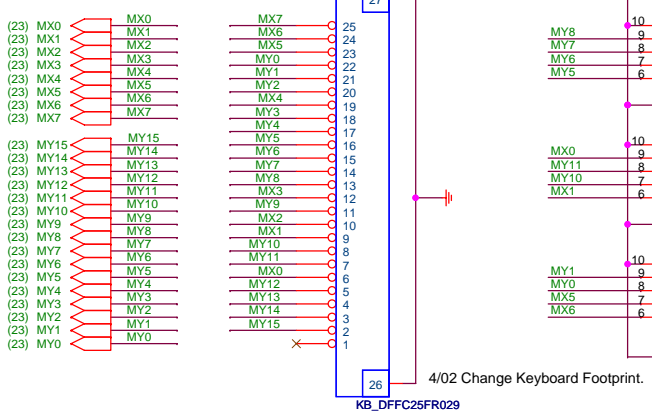


FOR 97551 ONLY

ADD 1M Flash ROM For Vista

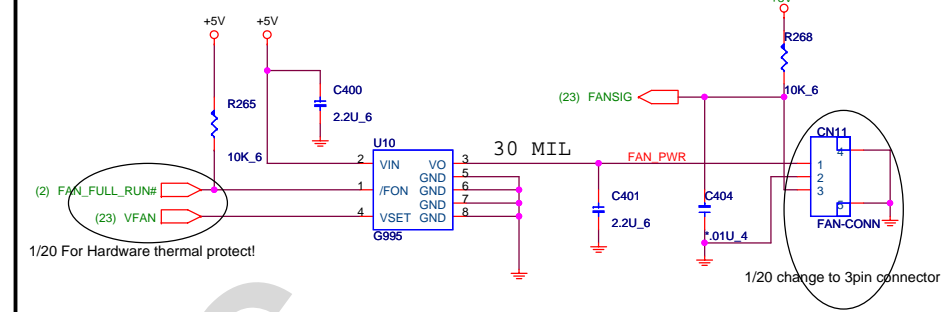
FWH

**INT K/B**



**KBC**

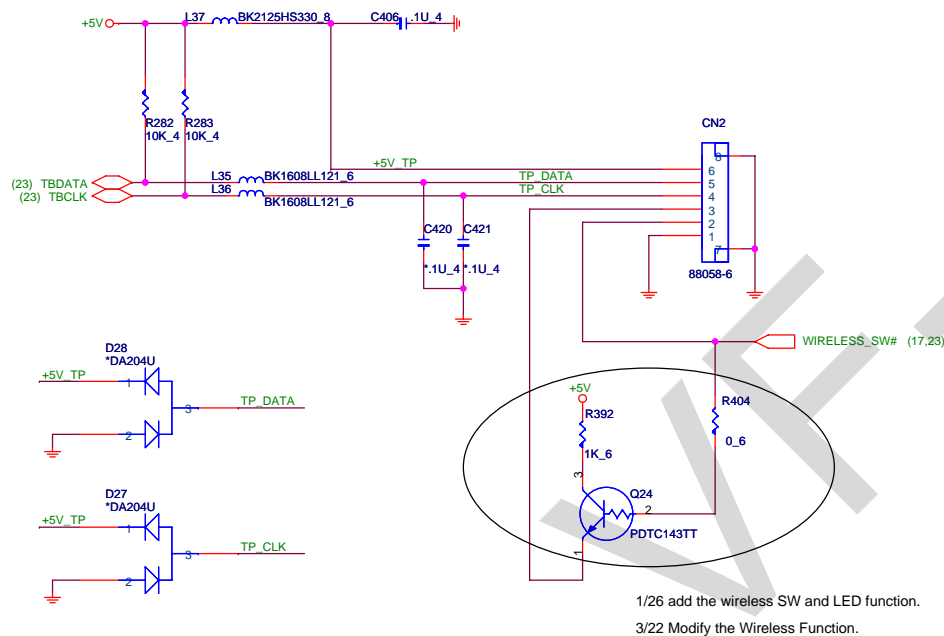
**FAN CONTROL**



**THM**

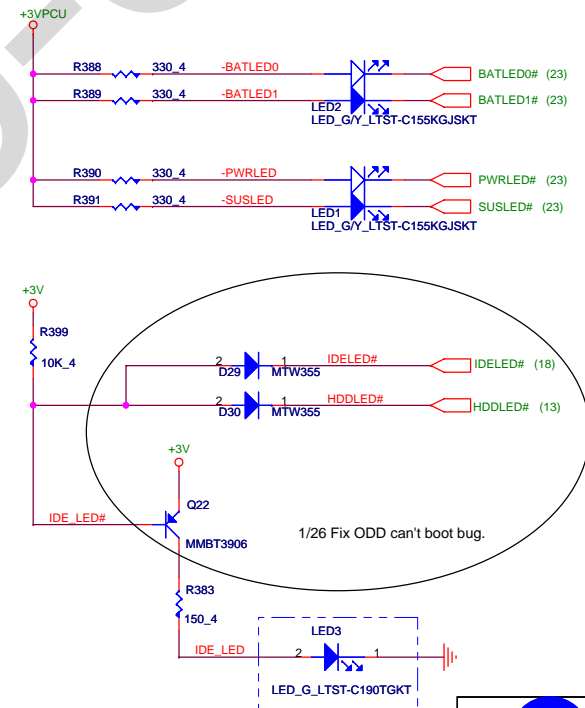
**TOUCH PAD**

20 MIL



**TPD**

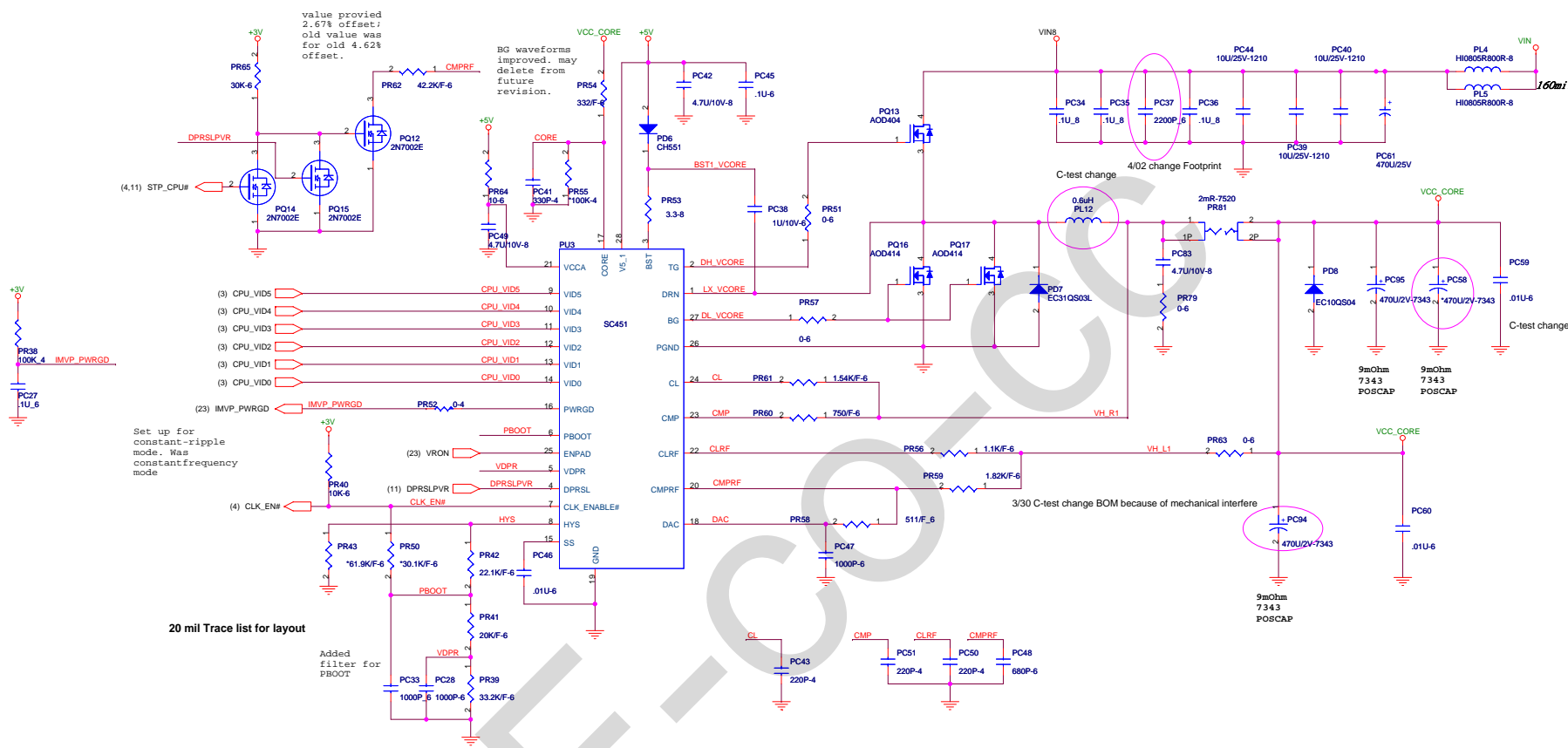
**ON BOARD LED**



**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>T/P,FAN,SWITCH,LED,K/B</b>	<b>3A</b>
Date:	Friday, May 05, 2006	Sheet 24 of 30





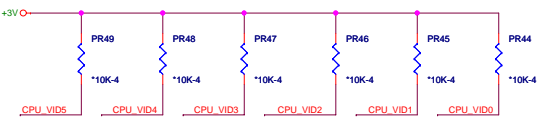
V I D							Vaore
VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	V	
0	1	0	1	1	1	1.340	
0	1	1	1	0	0	1.324	
0	1	1	0	1	0	1.292	
0	1	1	1	0	0	1.260	
0	1	1	1	1	0	1.244	
0	1	1	1	1	1	1.212	
1	0	0	0	0	1	1.180	
1	0	0	0	1	1	1.148	
1	0	0	1	1	0	1.100	
1	0	1	0	0	1	1.052	
1	0	1	0	1	1	1.020	
1	0	1	1	1	0	0.972	
1	1	0	0	0	0	0.940	

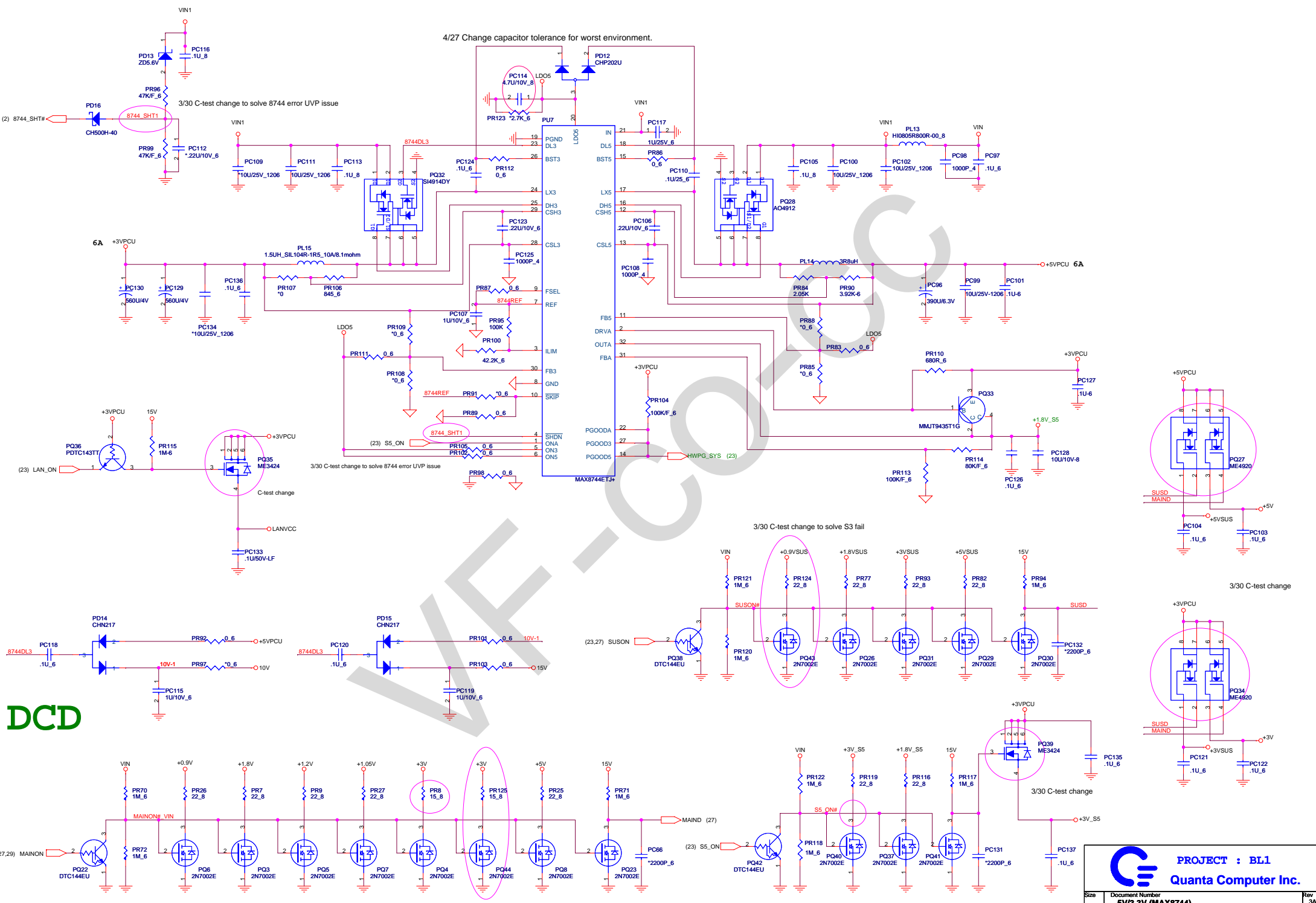
100 mil Trace list for layout

- DH\_VCORE
- LX\_VCORE
- DL\_VCORE
- DH\_VCORE2
- LX\_VCORE2
- DL\_VCORE2

30 mil Trace list for layout

- SC1476
- pin 4
- pin 5
- pin 7
- pin 25
- pin 30



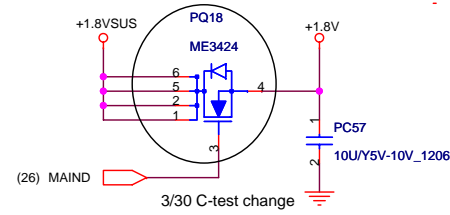
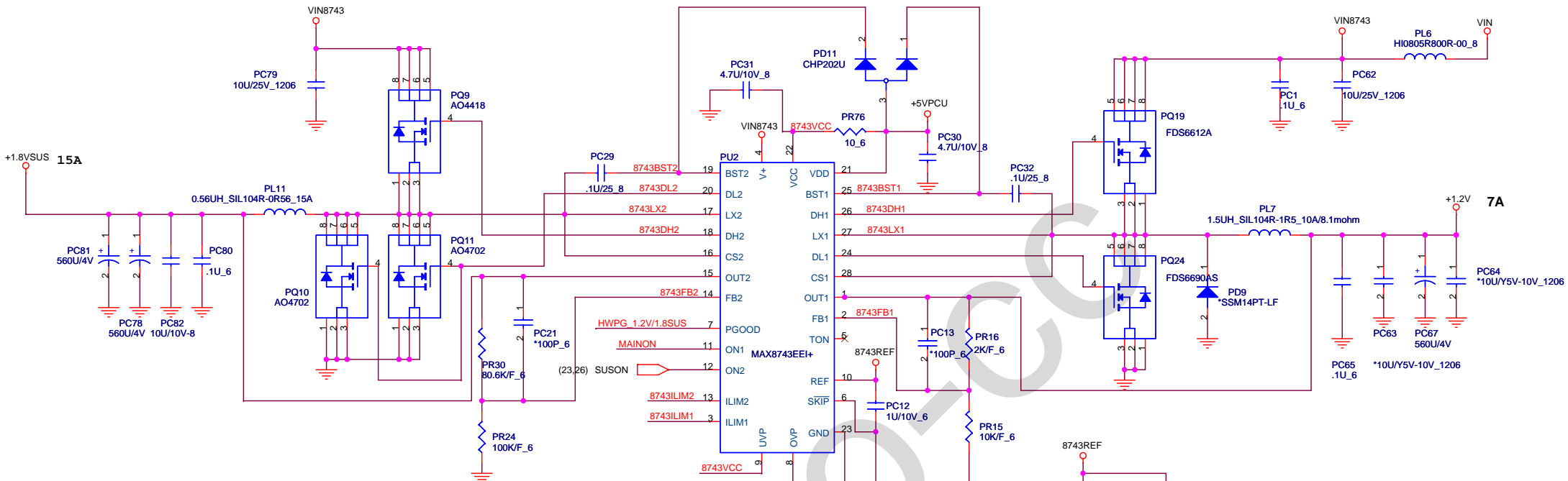


**DCD**

		<b>PROJECT : BL1</b> <b>Quanta Computer Inc.</b>	
		Size: Document Number <b>5V/3.3V (MAX8744)</b>	Rev: 3A
Date: Tuesday, May 09, 2006		Sheet 26 of 30	

3/30 C-test change to speed up +3V discharge time

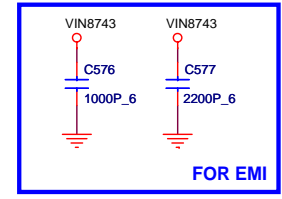
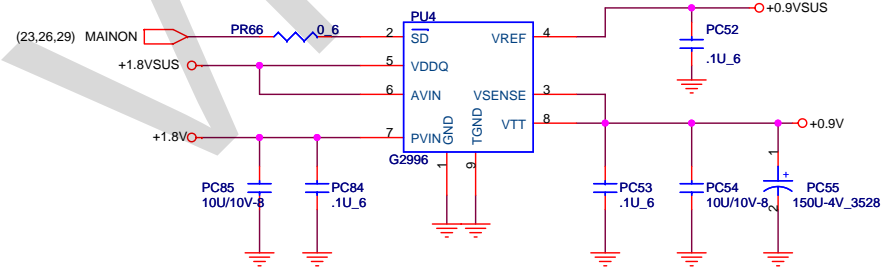
+1.8VSUS 15A



(23) HWPG\_1.2V/1.8SUS ← HWPG\_1.2V/1.8SUS

AO4704 Rds on = 13mOhm  
 ILOAD \* Rds on \* 10 = ILIM  
 ILIM2 = 1.235V Current limit 9.5A  
 ILIM1 = 0.91V Current limit 7A

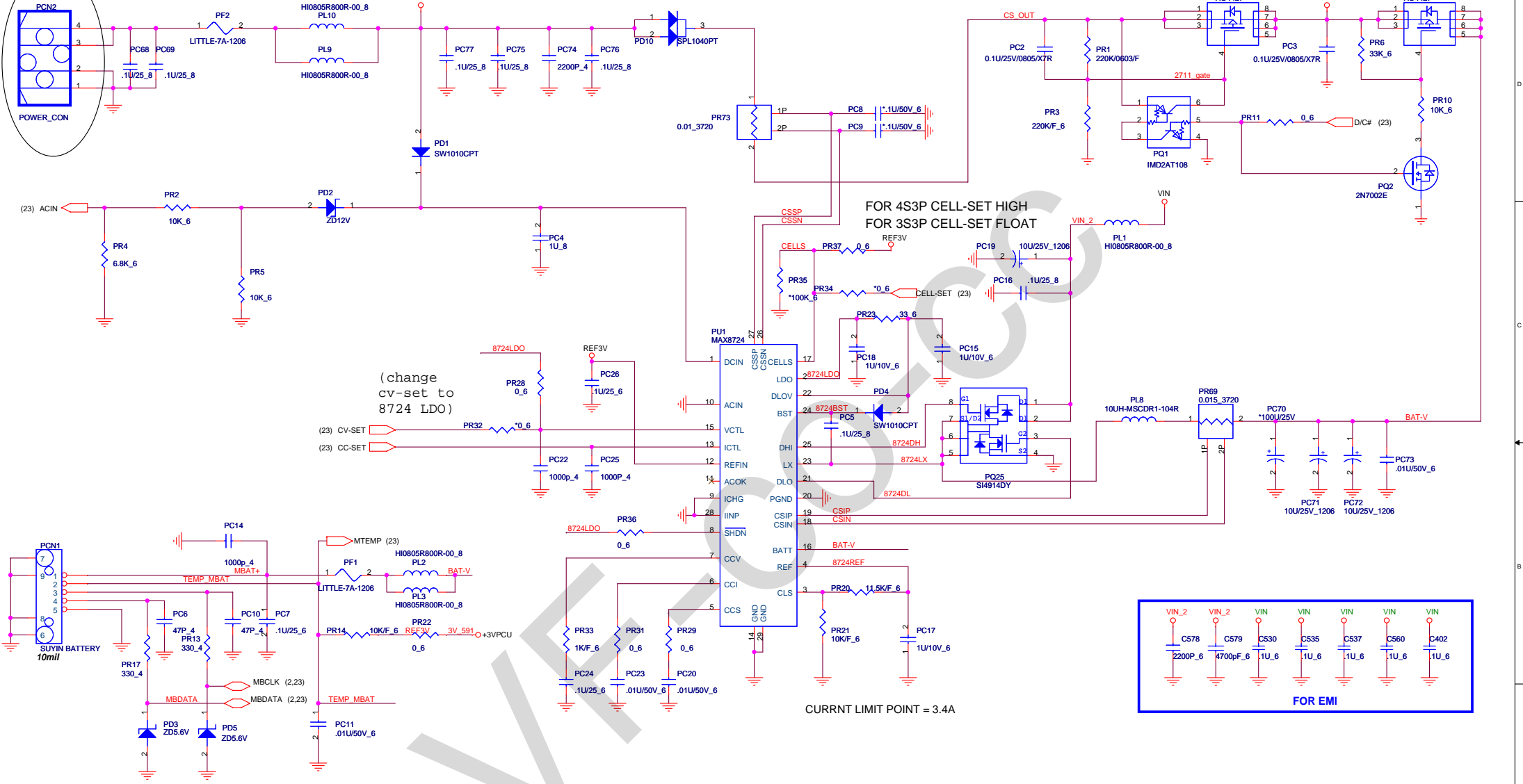
**DCD**



**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
	<b>+1.8/1.2V / VTT</b>	1A
Date:	Friday, April 28, 2006	Sheet 27 of 30

2/10 Modify Pin define

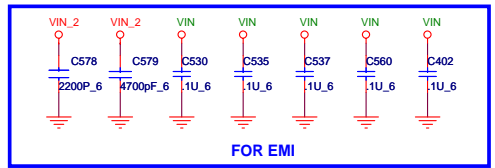


(change cv-set to 8724 LDO)

FOR 4S3P CELL-SET HIGH  
FOR 3S3P CELL-SET FLOAT

CURRNT LIMIT POINT = 3.4A

SMBus SLAVE ADDRESS: 16

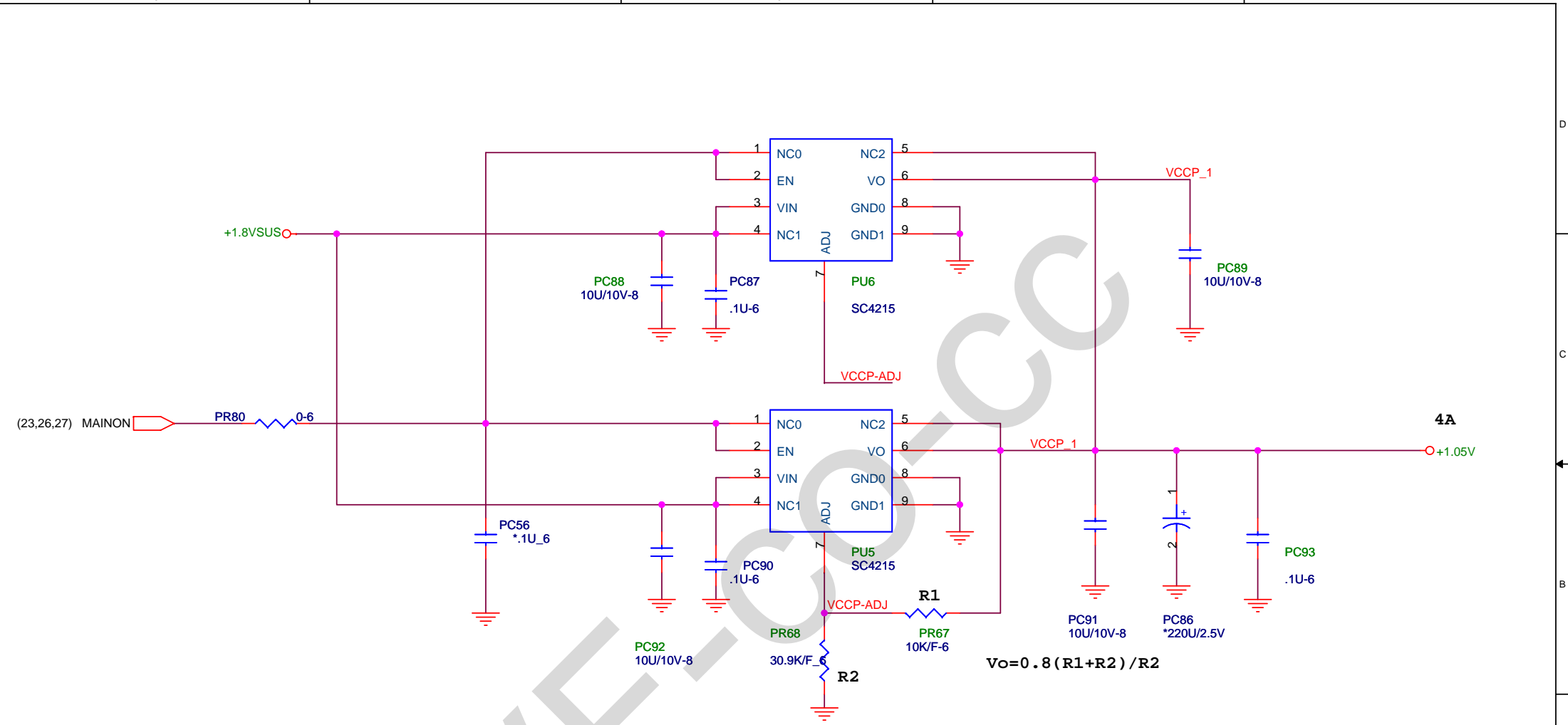


FOR EMI

# DCD


**PROJECT : BL1**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	<b>BATTERY CHARGER</b>	2A
Date:	Friday, April 28, 2006	Sheet 28 of 30



DCD

WVF

		PROJECT : BL1	
		Quanta Computer Inc.	
Size	Document Number	Rev	
	<b>+1.05V</b>	1A	
Date:	Friday, April 28, 2006	Sheet	29 of 30