

# COMPAL CONFIDENTIAL

MODEL NAME : *Sapporo XA*

COMPAL P/N : DFL10

PCB NO : LA-2051

Revision : 1.0

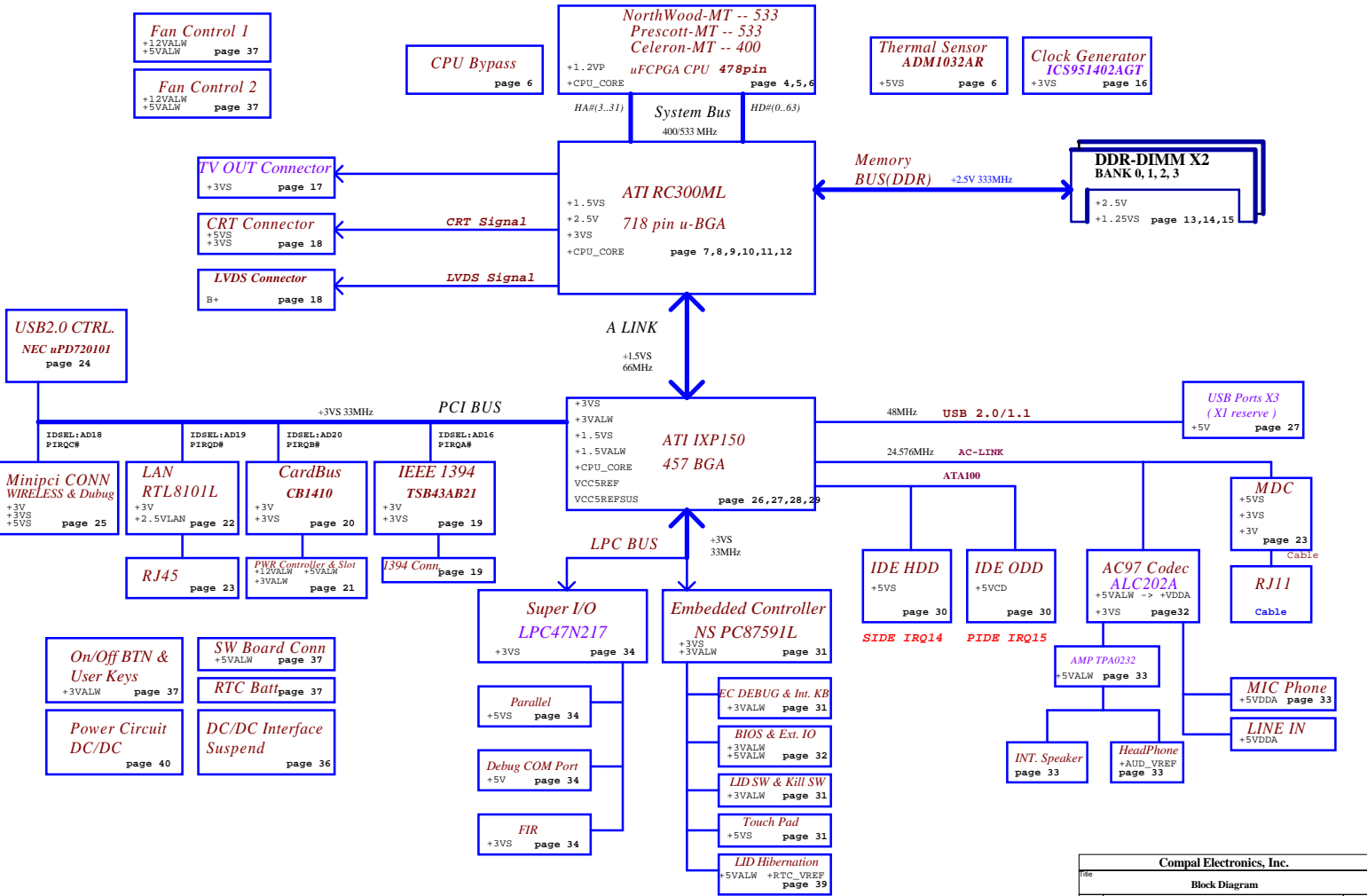
## Sapporo XA Schematics Document uFCBGA/uFCPGA NorthWood MT

2003 11 07 v1.0

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Model : DFL10 LA-2051



## Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	NA	NA	NA
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+1.2V	The voltage for Processor VID select	ON	OFF	OFF
+1.25VS	1.25V switched power rail for DDR Vtt	ON	OFF	OFF
+1.5VS	1.5V I/O power rail for ATI-RS300M/RC300M NB AGP.	ON	OFF	OFF
+1.8VS	1.8V switched power rail for ATI-RS300M/RC300M NB.	ON	OFF	OFF
+2.5VALW	2.5V always on power rail	ON	ON	ON*
+2.5V	2.5V system power rail for DDR	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V system power rail for SB,LAN,CardReader and HUB.	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V system power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

DEVICE	IDSEL #	REQ/GNT #	PIRQ
NB Internal VGA	N/A	N/A	A
AGP BUS	AGP_DEVSEL	N/A	A
SOUTHBRIDGE	AD31 (INT.)	N/A	N/A
USB	AD30 (INT.)	N/A	D
AC97	AD31 (INT.)	N/A	B
ATA 100	AD31 (INT.)	N/A	A
ETHERNET	AD24(INT.)	N/A	C
1394	AD16	0	A
LAN	AD19	1	D
CARD BUS	AD20	2	A
Wireless LAN(MINI PCI)AD18		3	C

← EXT USB AD23(EXT.) 4 A,C,D →

### EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16)	1010 000X b

### EC SM Bus2 address

Device	Address
ADM1032	1001 100X b

## I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 X
DDR SO-DIMM 1	A2	1 0 1 0 0 0 1 X
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 X

Power Managment table

Signal	+3VALW +5VALW +12VALW	+5V +3V +2.5V	+2.5VS +1.8VS +5VS +3VS +1.5VS +CPU_CORE +1.25VS
S0	ON	ON	ON
S1	ON	ON	ON
S3	ON	ON	OFF
S5 S4/AC	ON	OFF	OFF
S5 S4/AC don't exist	OFF	OFF	OFF

## SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
SKU ID	Rb	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

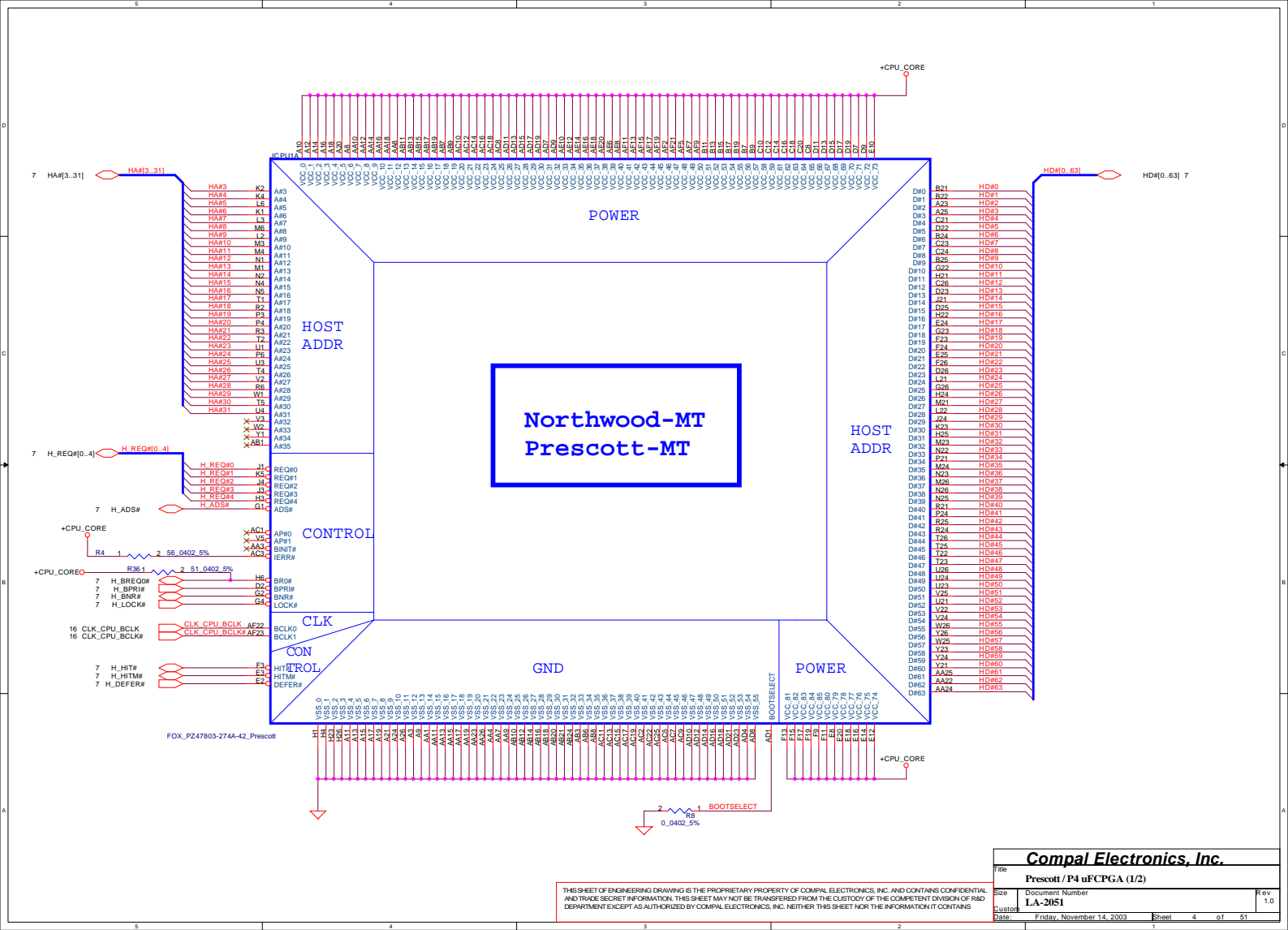
## BOARD ID

Version	BID1	BID0
0	0	0
1	0	1
2	1	0
3	1	1

SKU ID	CD PLAY FUNCTION	Short cut key
0		
1		
2		
3	YES	YES
4	YES	NO
5	NO	YES
6	NO	NO
7		

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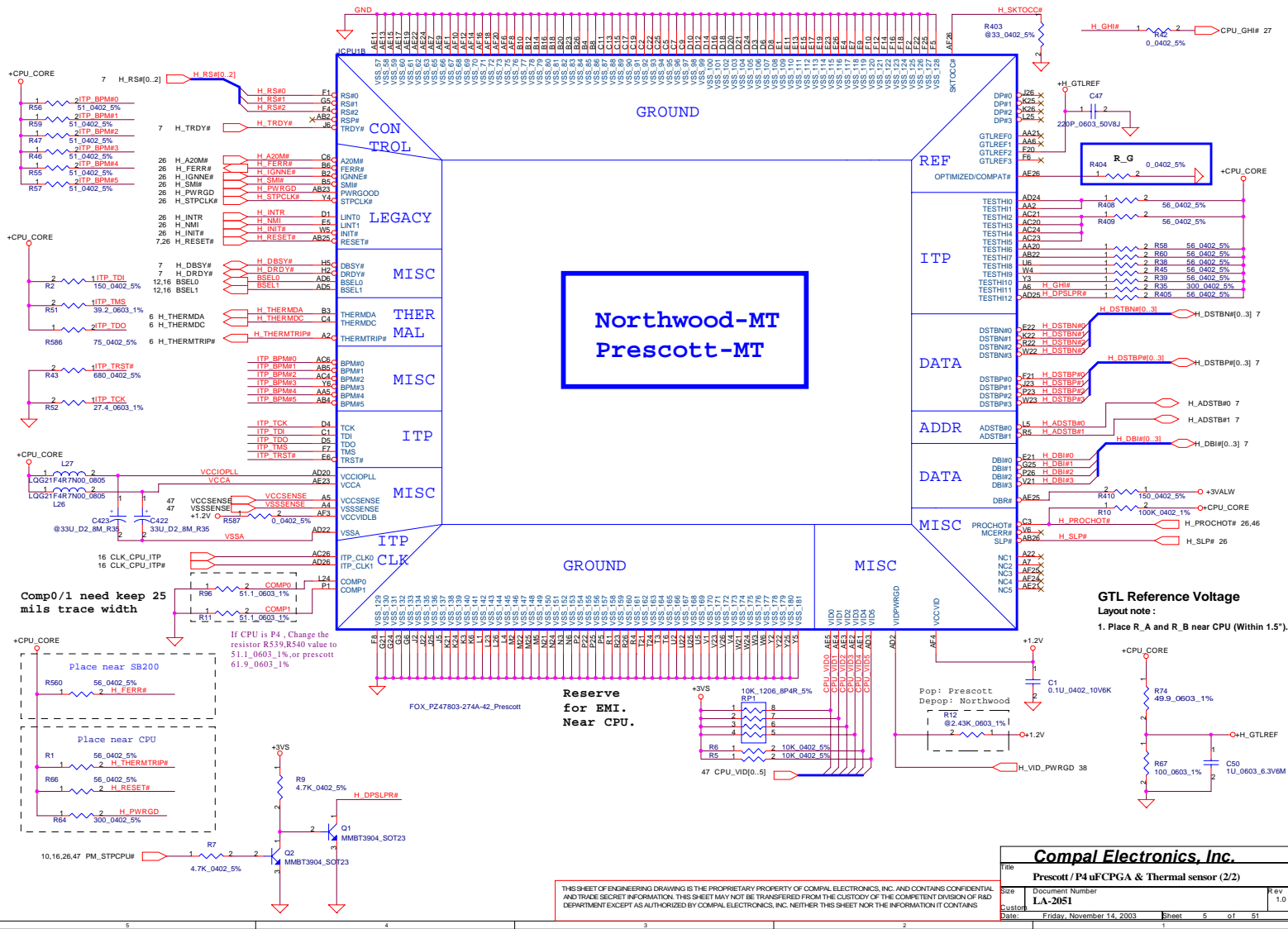
Compal Electronics, Inc.			
Title	Note & Revision		
Size	Document Number	Rev	
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<b>Compal Electronics, Inc.</b>			
Title	Prescott / P4 uFCPGA (1/2)		
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# Northwood-MT Prescott-MT



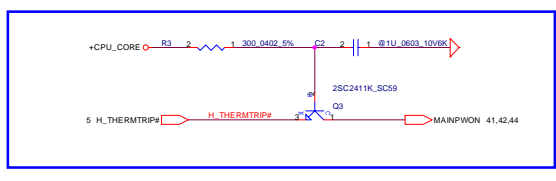
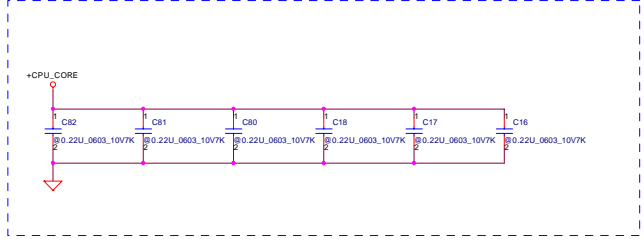
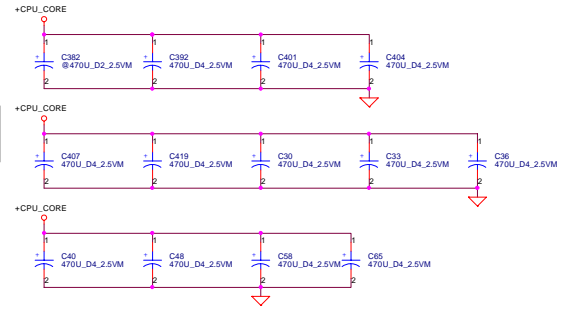
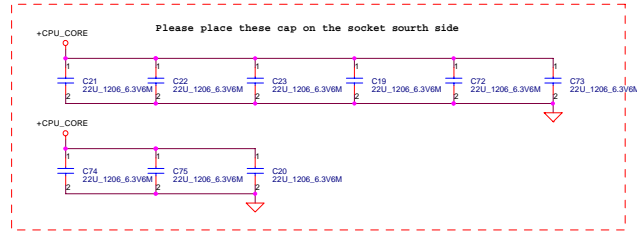
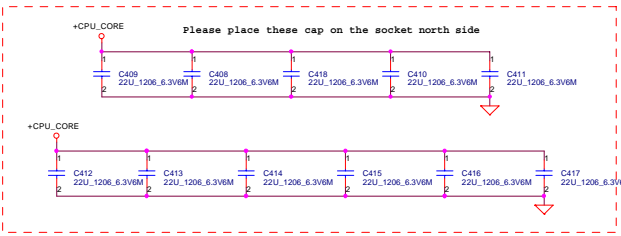
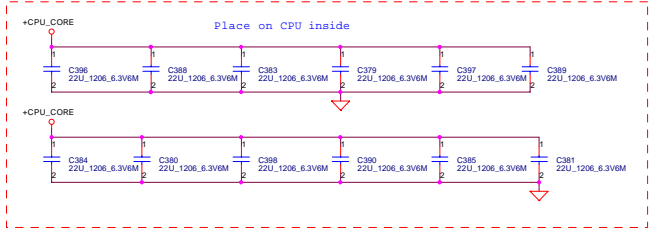
<b>Compal Electronics, Inc.</b>			
File: Prescott / P4 uFCPGA & Thermal sensor (2/2)			
Document Number		Rev	
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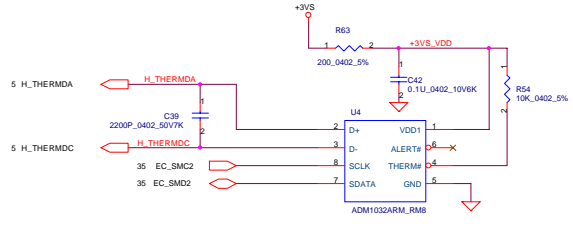
**Layout note :**  
Place close to CPU. Use 2-3 vias per PAD.  
Place 22uF caps x31 pcs, populated 14pcs.

**Layout note :**  
Place close to CPU power and ground pin as possible (<1inch)

**For Desktop's CPU:**  
470uF x 15 / 12mOhm H=1.8 each  
Total 0.923m ohm



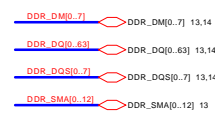
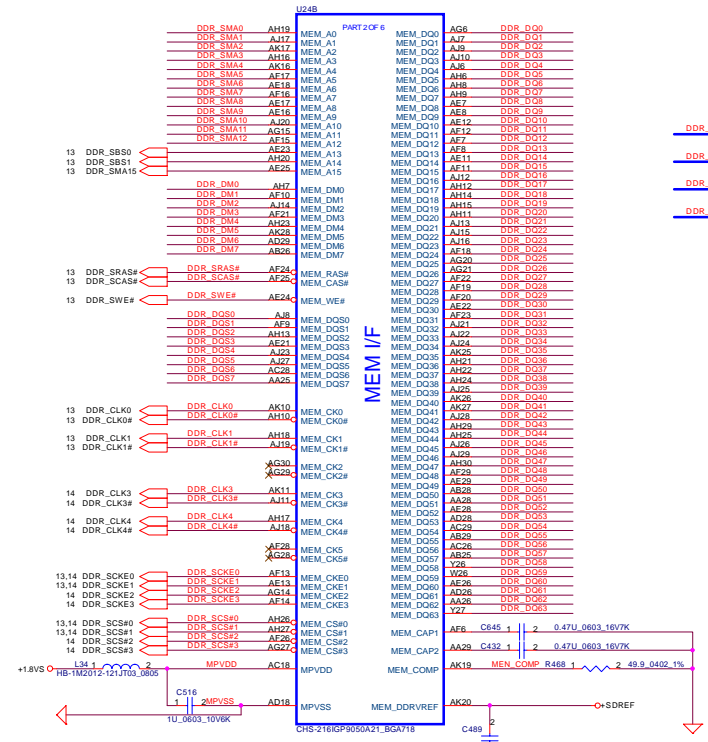
**CPU Temperature Sensor**



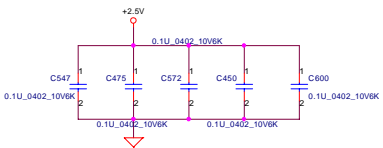
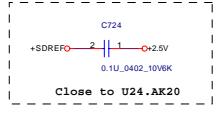
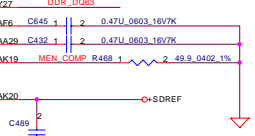
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Title	CPU Decoupling CAP.	
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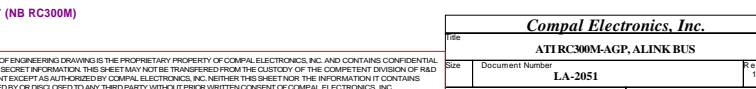
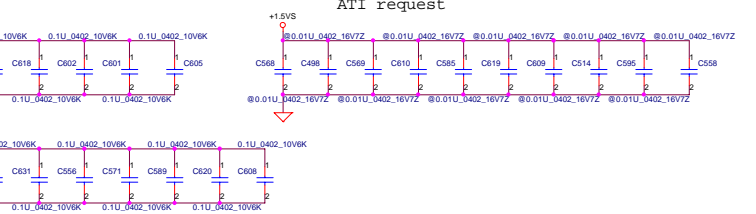
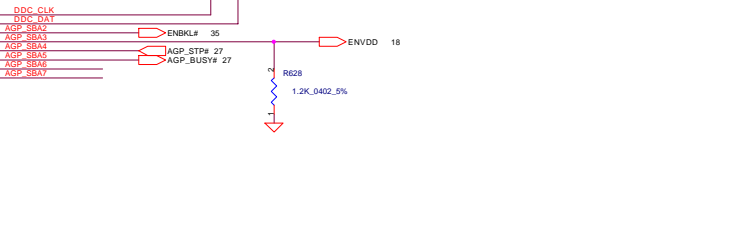
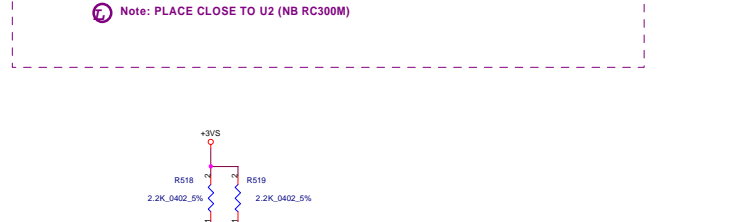
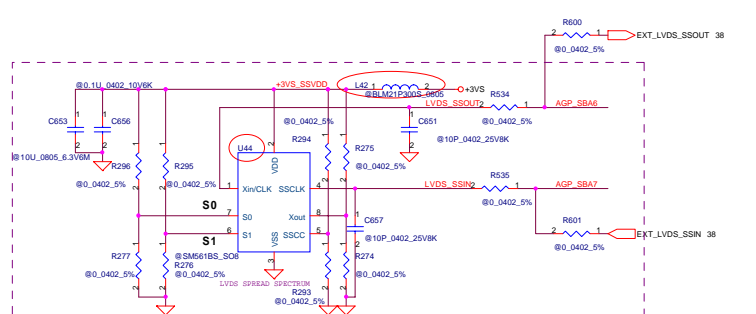
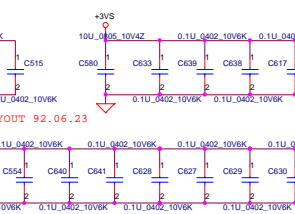
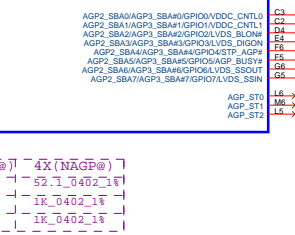
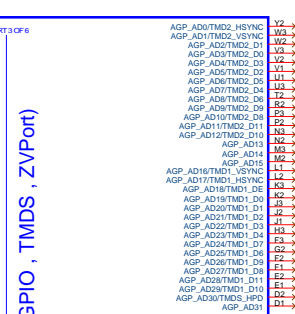
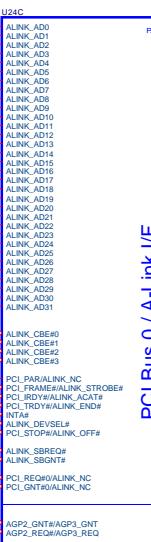
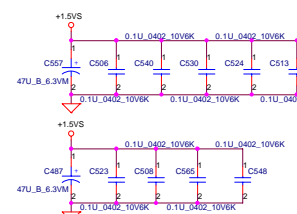
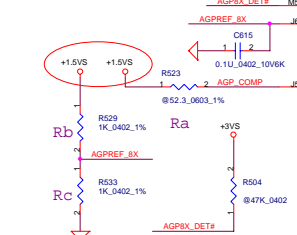
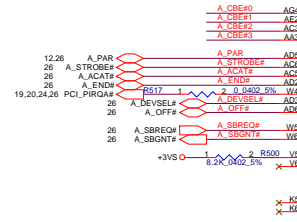
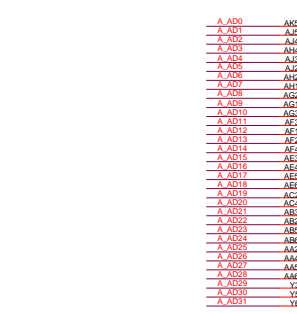
MEM / F



Compal Electronics, Inc.		
Title	ATRRC300M-DDR 1/F	
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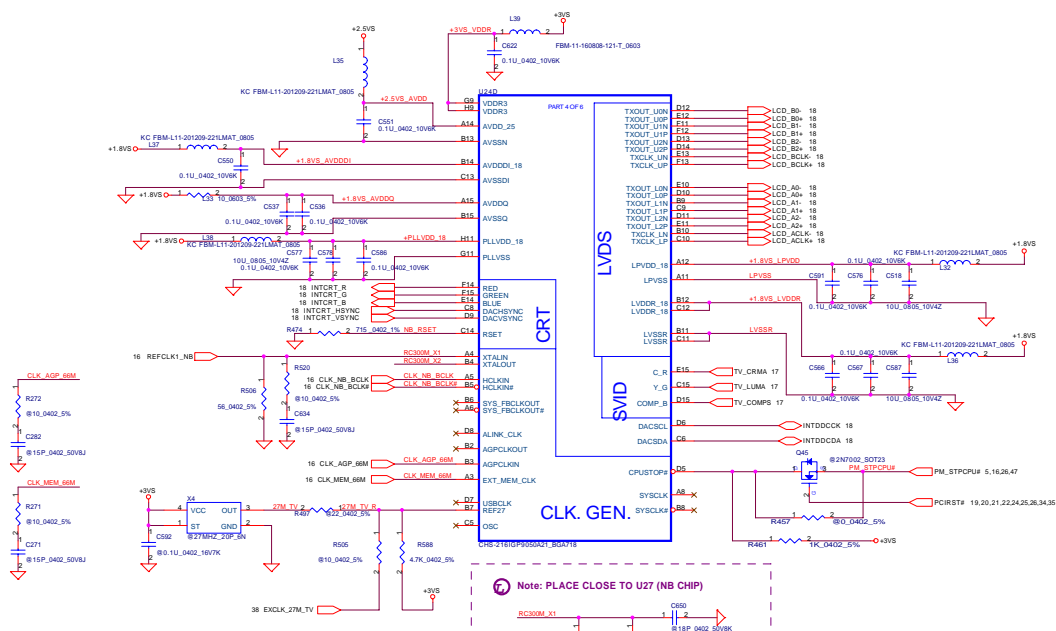
12.26 A\_AD0\_31  
12.26 A\_CBE#0\_31



Note: PLACE CLOSE TO U27 (NB RC300M)

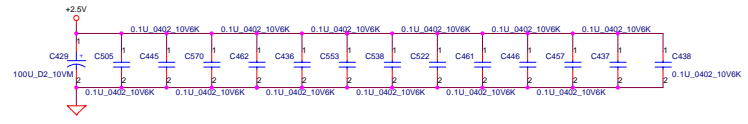
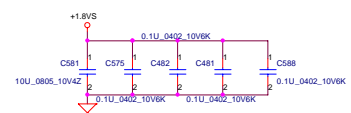
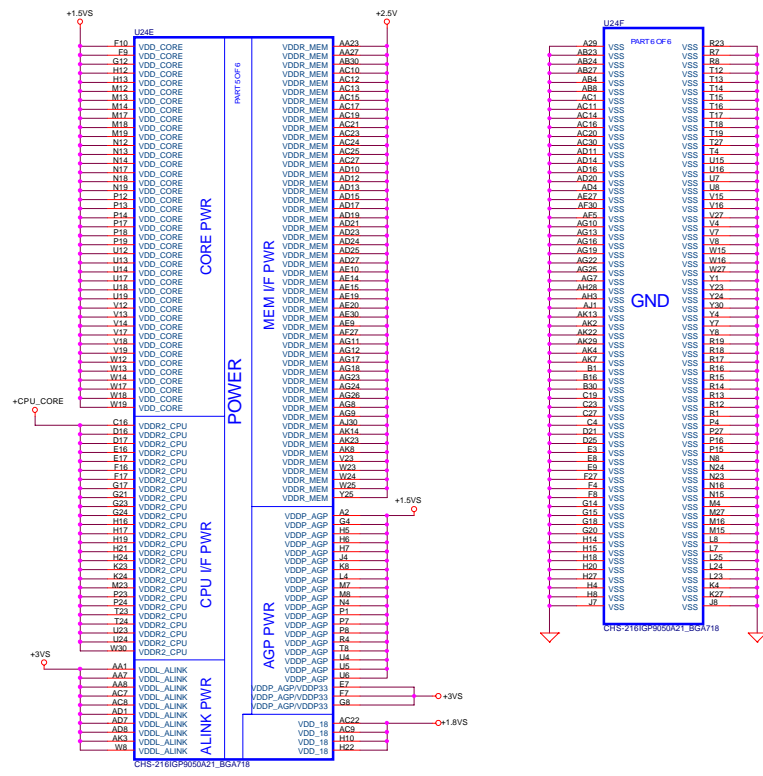
Compal Electronics, Inc.		
File:	AT1RC300M-AGP, ALINK BUS	
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File	<b>ATRC300M-VIDEO I/F</b>
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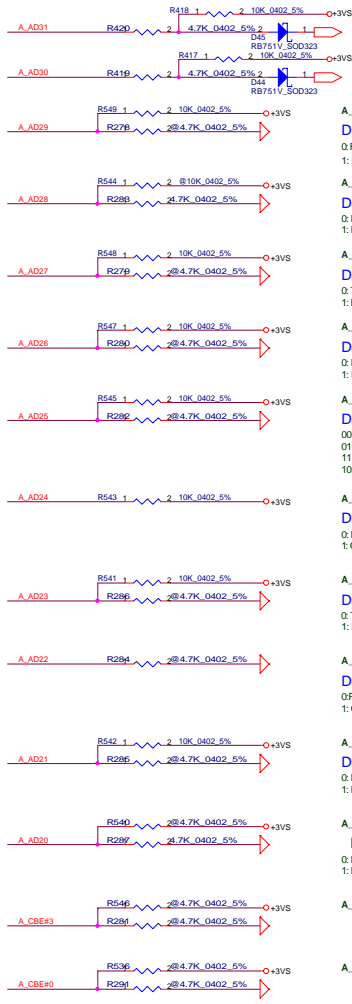
File: **ATIRC300M-POWER**

Size: Document Number **LA-2051** Rev: 1.0

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9.26 A\_ADJ0..31  
 9.26 A\_CBE#0..31



**A\_AD[31..30] : FSB CLK SPEED**  
**DEFAULT: 01**  
 00: 100 MHZ  
 01: 133 MHZ  
 10: 200MHZ  
 11:166 MHZ

**A\_AD29 : STRAP CONFIGURATION**  
**DEFAULT:1**  
 0:REDUCEDE SET  
 1:FULL SET(internal Pull high)

**A\_AD28 : SPREAD SPECTRUM ENABLE**  
**DEFAULT:0**  
 0: DISABLE  
 1: ENABLE

**A\_AD27: FrcShortReset#**  
**DEFAULT: 1**  
 0:TEST MODE  
 1:NORMAL MODE

**A\_AD26 : ENABLE IOQ**  
**DEFAULT: 1**  
 0:IOQ=1  
 1:IOQ=12

**A\_AD25/A\_AD17 : CPU VOLTAGE[1..0]**  
**DEFAULT: 10** AD25=1 DESTOP CPU  
 AD25=0 MOBILE CPU  
 AD17--DON'T CARE  
 00: 1.05V  
 01: 1.35V  
 11: 1.75V  
 10: 1.45V

**A\_AD24 : MOBILE CPU SELECT**  
**DEFAULT: 1**  
 0: BANIAS CPU  
 1: OTHER CPU

**A\_AD23 : CLOCK BYPASS DISABLE**  
**DEFAULT: 1**  
 0: TEST MODE  
 1: NORMAL(internal Pull high)

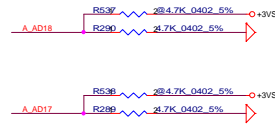
**A\_AD22 : OSC PAD OUTPUT PCICLK**  
**DEFAULT : 1**  
 0:PCICLK OUT  
 1: OSC CLK OUT

**A\_AD21 : AUTO\_CAL ENABLE**  
**DEFAULT : 1**  
 0: DISABLE  
 1: ENABLE

**A\_AD20 : INTERNAL CLK GEN ENABLE**  
**DEFAULT : 0**  
 0: DISABLE  
 1: ENABLE

**A\_CBE#3: NOT USED**

**A\_CBE#0 :NO USED**



**A\_AD18 : ENABLE PHASE CALIBRATION**  
**DEFAULT: 0**  
 0: DISABLE  
 1:ENABLE

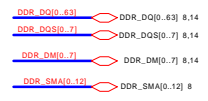
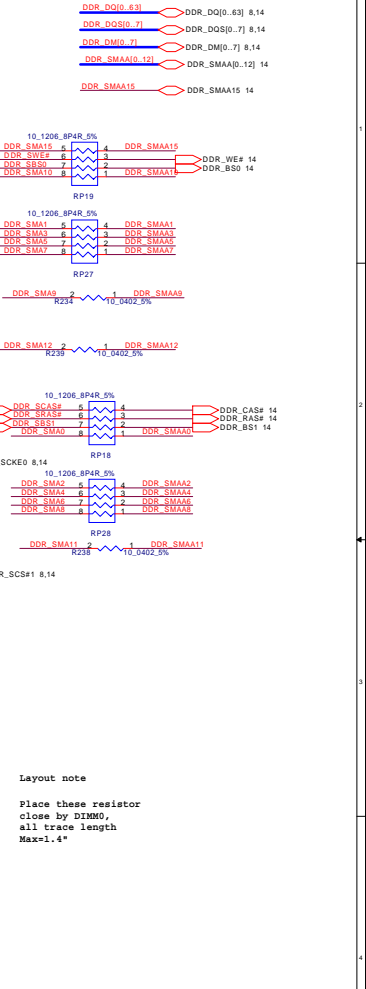
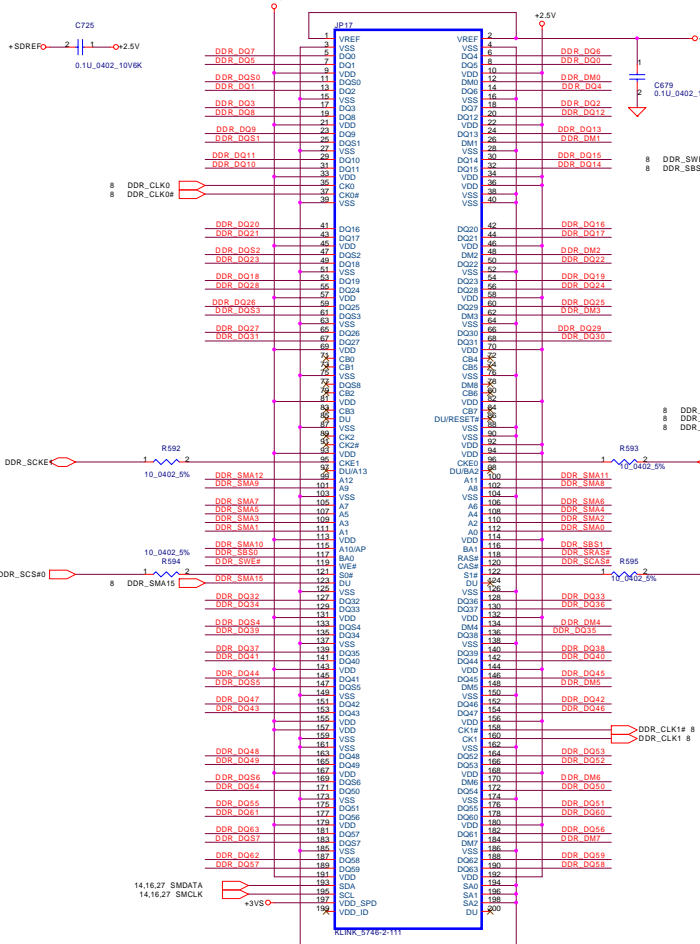
**A\_AD25/A\_AD17 : CPU VOLTAGE[1..0]**  
**DEFAULT: 0**  
 00: 1.05V  
 01: 1.35V  
 11: 1.75V  
 10: 1.45V



**PAR: EXTENDED DEBUG MODE**  
**DEFAULT : 1**  
 0: DEBUG MODE  
 1: NORMAL

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<b>Compal Electronics, Inc.</b>			
File:	AT1RC300M-SYSTEM STRAP		
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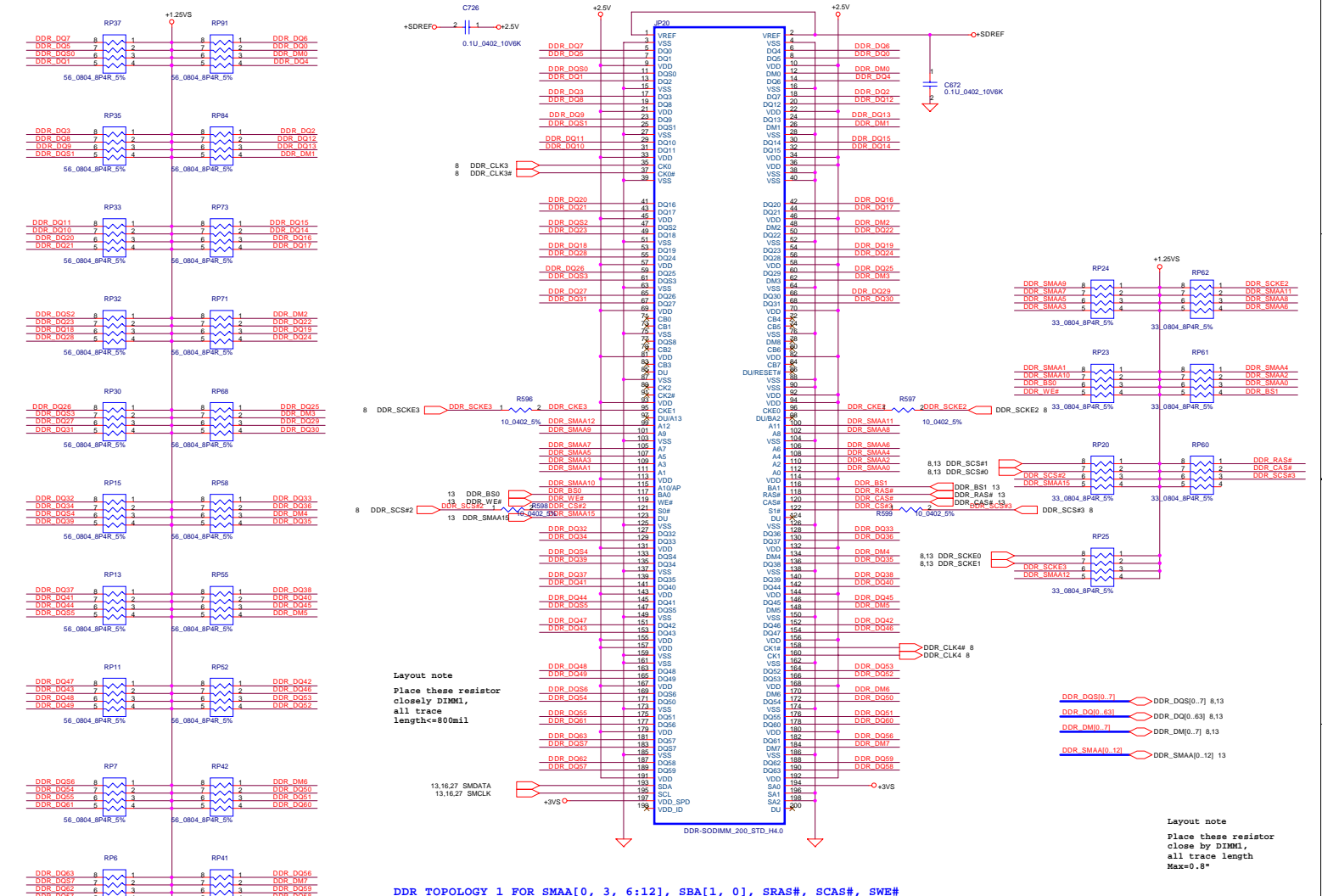
Layout note  
Place these resistors  
close to DIMM,  
all trace length<500 mil

**DDR TOPOLOGY 1 FOR SMAA[0, 3, 6:12], SBA[1, 0], SRAS#, SCAS#, SWE#**

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Layout note  
Place these resistor  
close by DIMM,  
all trace length  
Max=1.4"

Compal Electronics, Inc.		
File: DDR-SODIMM SLOT0		
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Layout note  
Place these resistor  
closely DIMM1,  
all trace  
length=800mil

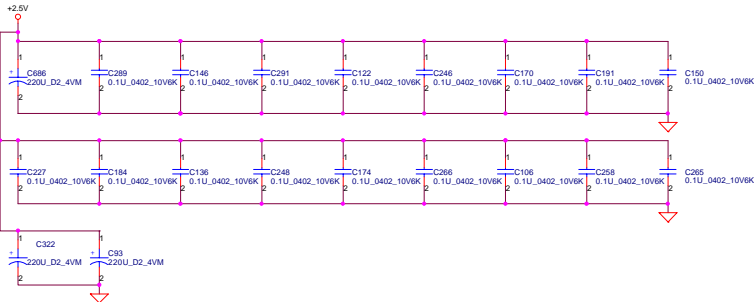
Layout note  
Place these resistor  
close by DIMM1,  
all trace length  
Max=0.6"

DDR TOPOLOGY 1 FOR SMAA[0, 3, 6:12], SBA[1, 0], SRAS#, SCAS#, SWE#

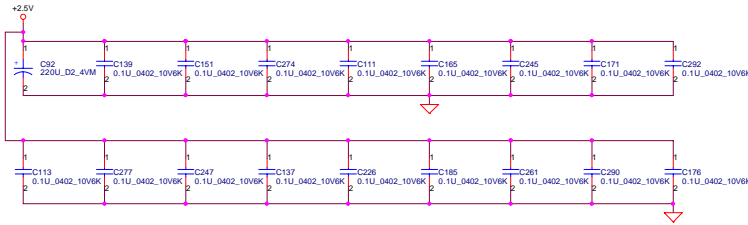
Compal Electronics, Inc.		
Doc Number	DDR-SODIMM SLOT1	
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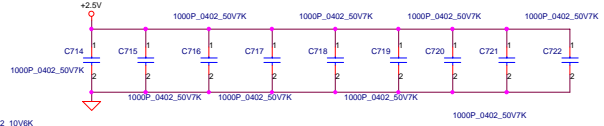
**Layout note :**  
Distribute as close as possible to DDR-SODIMM.



**Layout note :**  
Distribute as close as possible to DDR-SODIMM1.

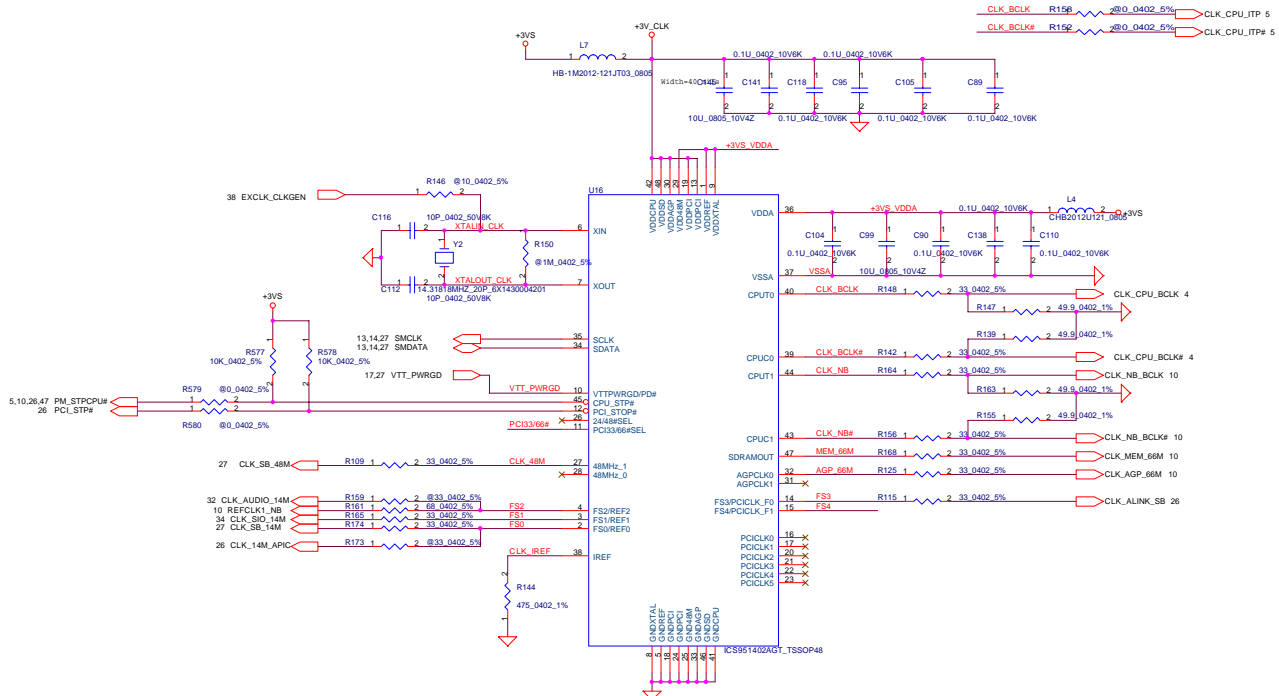


**Layout note :**  
for EMI solution



**Layout note :**  
Place one cap close to every 2 pull up resistors termination to +1.25VS





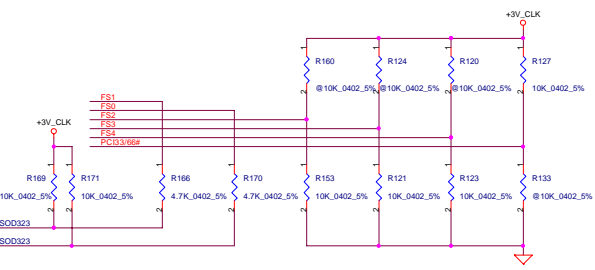
**CLOCK FREQUENCY SELECT TABLE**

FS4	FS3	FS2	FS1	FS0	CPU	MEM	With Spread Enabled...
0	0	0	1	0	200	200	Spread OFF OR Center spread +/-0.3%
0	0	0	0	1	133	133	
0	0	0	0	0	100	100	

Note: 0 = PULL LOW  
1 = PULL HIGH

**A-LINK FREQ**

PC13366# = HIGH	66MHz
PC13366# = LOW	33MHz



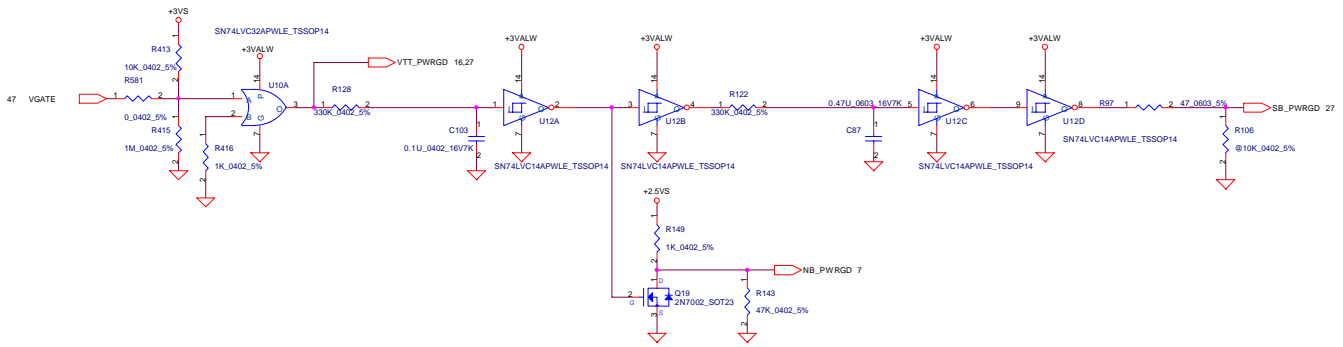
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**Compal Electronics, Inc.**

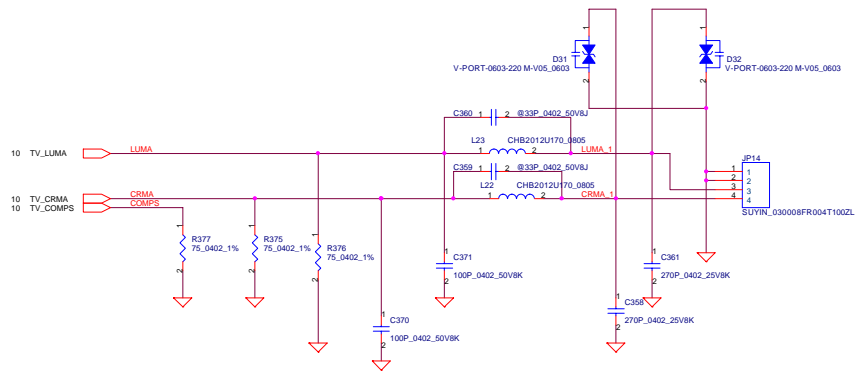
**Clock Generator**

File	LA-2051		Rev	1.0
Size	Document Number			
Date	Friday, November 14, 2003	Sheet	16	of 51



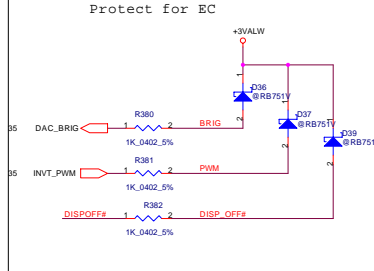
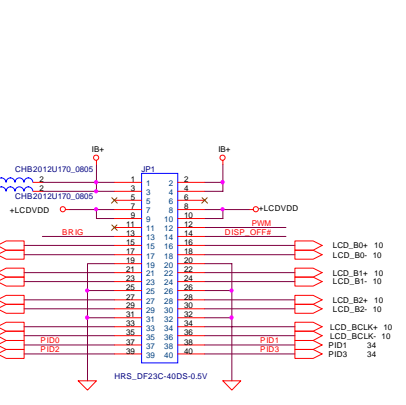
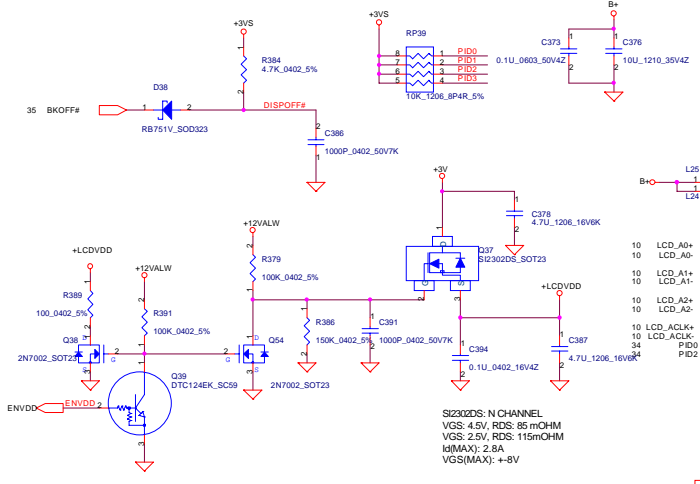
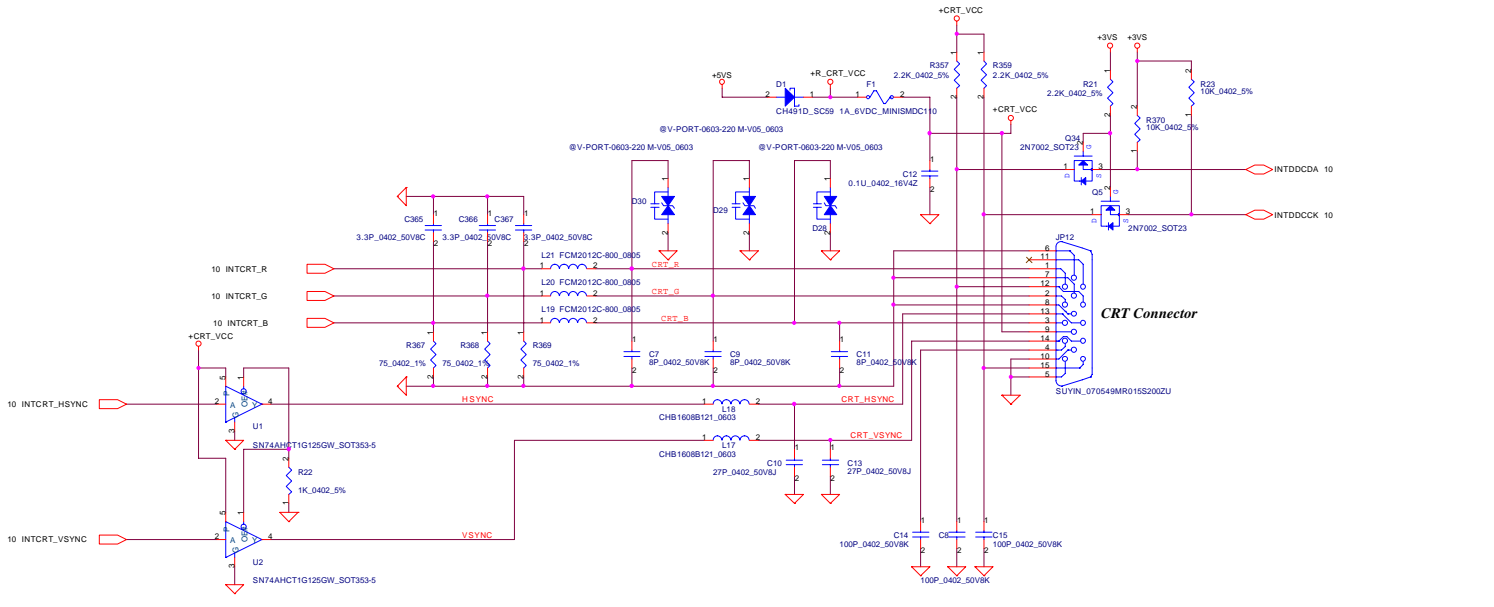


**TV-OUT CONN.**



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<b>Compal Electronics, Ltd.</b>		
File:	<b>CH-7011&amp; TV-CONN.</b>	
Size:	Document Number	Rev:
Customer:	<b>LA-2051</b>	1.0
Date:	Friday, November 14, 2003	Sheet 17 of 51

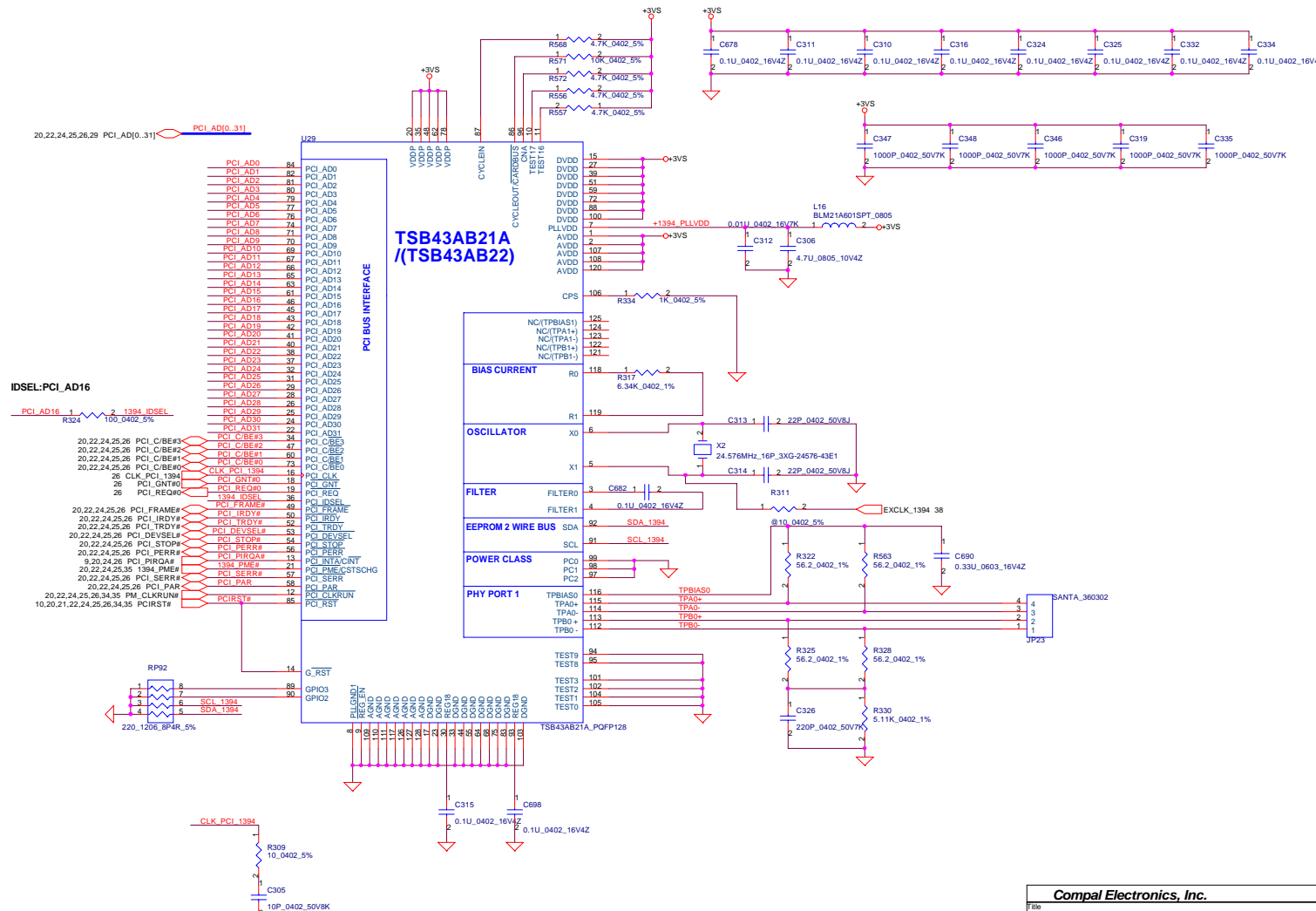


S2302DS: N CHANNEL  
 VGS: 4.5V, RDS: 85 m $\Omega$ HM  
 VGS: 2.5V, RDS: 115m $\Omega$ HM  
 I<sub>D</sub>(MAX): 2.8A  
 VGS(MAX): -8V

**Compal Electronics, Ltd.**

Title: <b>CRT &amp; LVDS CONN.</b>		Rev: 1.0
Size: L	Document Number: LA-2051	
Date: Friday, November 14, 2003	Sheet: 18	of 51

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ISSEL:PCI\_AD16

PCI\_AD16 1 2 1394 ISSEL  
R324 100\_0402\_5%

- 20,22,24,25,26 PCI\_AD0# 84
- 20,22,24,25,26 PCI\_AD1# 82
- 20,22,24,25,26 PCI\_AD2# 80
- 20,22,24,25,26 PCI\_AD3# 78
- 20,22,24,25,26 PCI\_AD4# 76
- 20,22,24,25,26 PCI\_AD5# 74
- 20,22,24,25,26 PCI\_AD6# 72
- 20,22,24,25,26 PCI\_AD7# 70
- 20,22,24,25,26 PCI\_AD8# 68
- 20,22,24,25,26 PCI\_AD9# 66
- 20,22,24,25,26 PCI\_AD10# 64
- 20,22,24,25,26 PCI\_AD11# 62
- 20,22,24,25,26 PCI\_AD12# 60
- 20,22,24,25,26 PCI\_AD13# 58
- 20,22,24,25,26 PCI\_AD14# 56
- 20,22,24,25,26 PCI\_AD15# 54
- 20,22,24,25,26 PCI\_AD16# 52
- 20,22,24,25,26 PCI\_AD17# 50
- 20,22,24,25,26 PCI\_AD18# 48
- 20,22,24,25,26 PCI\_AD19# 46
- 20,22,24,25,26 PCI\_AD20# 44
- 20,22,24,25,26 PCI\_AD21# 42
- 20,22,24,25,26 PCI\_AD22# 40
- 20,22,24,25,26 PCI\_AD23# 38
- 20,22,24,25,26 PCI\_AD24# 36
- 20,22,24,25,26 PCI\_AD25# 34
- 20,22,24,25,26 PCI\_AD26# 32
- 20,22,24,25,26 PCI\_AD27# 30
- 20,22,24,25,26 PCI\_AD28# 28
- 20,22,24,25,26 PCI\_AD29# 26
- 20,22,24,25,26 PCI\_AD30# 24
- 20,22,24,25,26 PCI\_AD31# 22
- 20,22,24,25,26 PCI\_C/BE#3# 34
- 20,22,24,25,26 PCI\_C/BE#2# 40
- 20,22,24,25,26 PCI\_C/BE#1# 46
- 20,22,24,25,26 PCI\_C/BE#0# 52
- 20,22,24,25,26 CLK\_PCI\_1394# 72
- 20,22,24,25,26 PCI\_GNT#0# 18
- 20,22,24,25,26 PCI\_REQ#0# 36
- 20,22,24,25,26 PCI\_FRAME# 48
- 20,22,24,25,26 PCI\_TRDY# 50
- 20,22,24,25,26 PCI\_DEVSEL# 54
- 20,22,24,25,26 PCI\_STOP# 56
- 20,22,24,25,26 PCI\_PERR# 58
- 20,22,24,25,26 PCI\_PIRDA# 60
- 20,22,24,25,26 1394\_PME# 62
- 20,22,24,25,26 PCI\_SERR# 64
- 20,22,24,25,26 PCI\_PAR# 66
- 20,22,24,25,26,34,35 PM\_CLKRUN# 12
- 10,20,21,22,24,25,26,34,35 PCIRST# 88

RP22 14

G\_RST 88

GPIO3 90

GPIO2 92

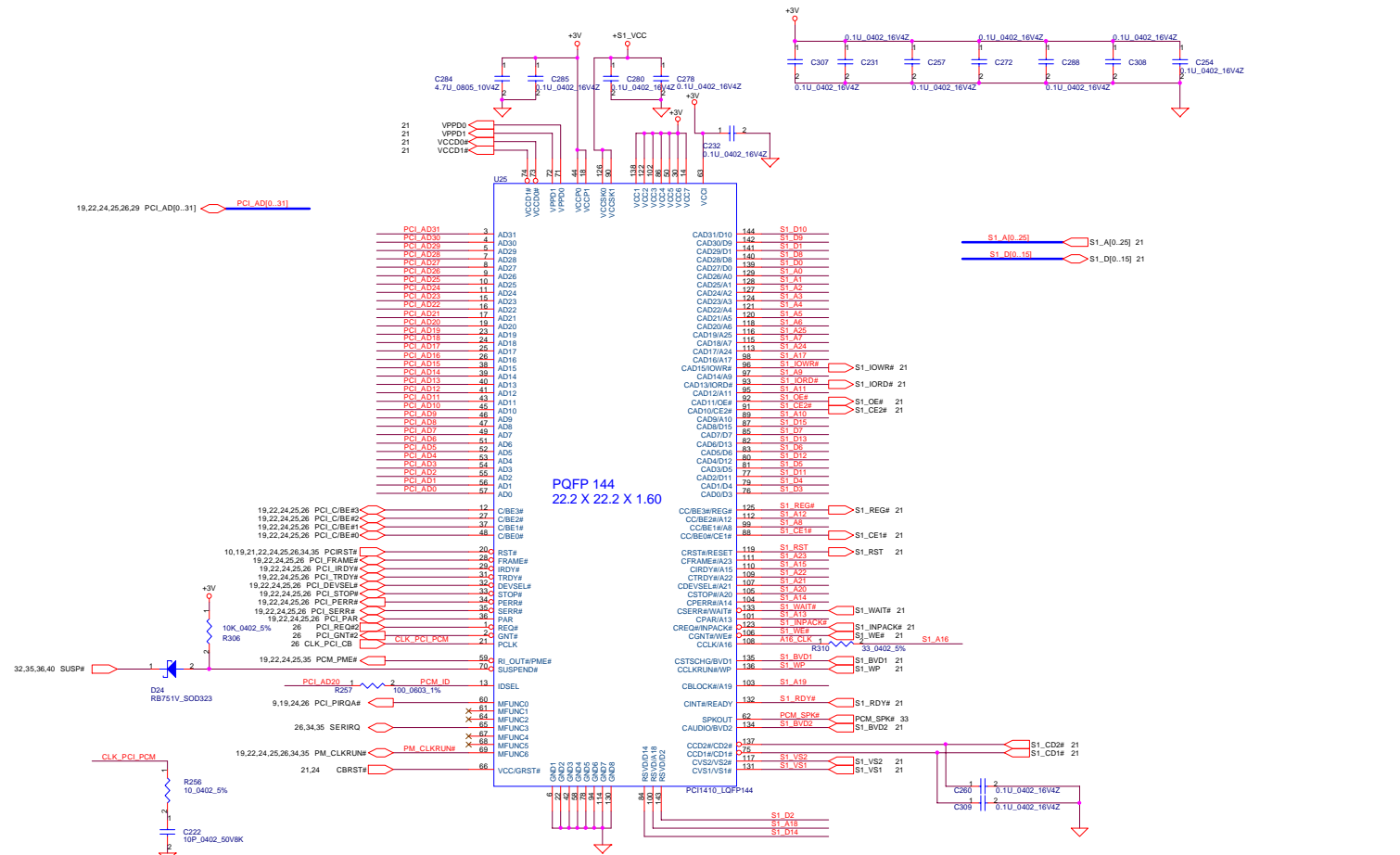
CLK\_PCI\_1394 10\_0402\_5%

C305 10P\_0402\_50V8K

<b>Compal Electronics, Inc.</b>			
File	T1 1394 Controller TSB43AB21A		
Size	Document Number	Rev	
Cus	LA-2051	1.0	
Date:	Friday, November 14, 2003	Sheet	19 of 51

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CARD BUS AD20 REQ#2/GNT#2 PCI\_PIRQA#

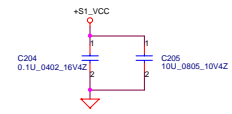
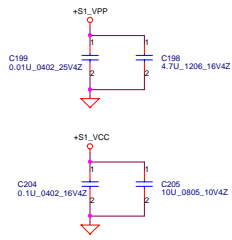
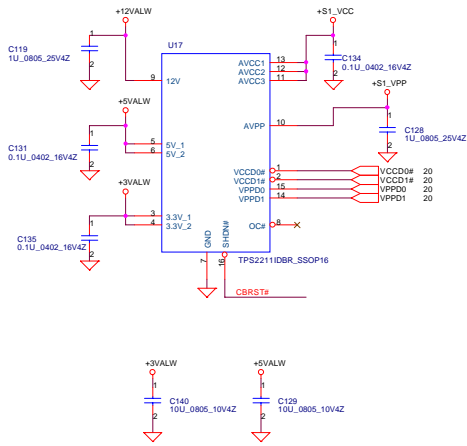


PQFP 144  
22.2 X 22.2 X 1.60

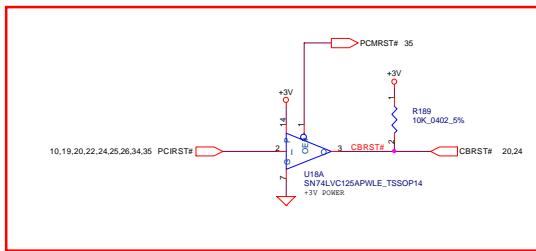
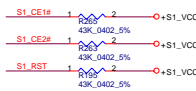
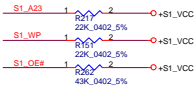
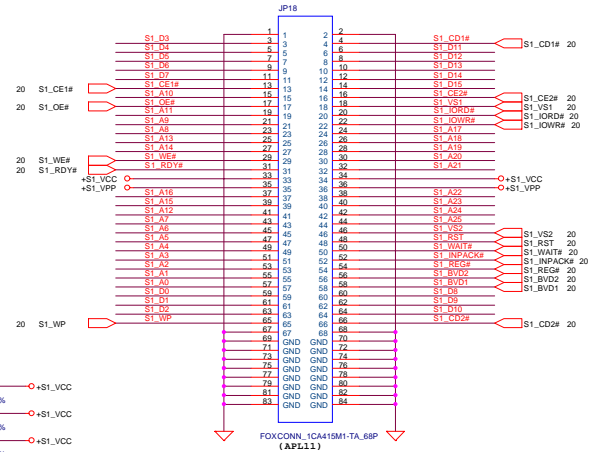
<b>Compal Electronics, Ltd.</b>			
File:	CardBus Controller-T1 PCI1410>		
Size:	Document Number	Rev: 1.0	
Customer:	L A-2051		
Date:	Friday, November 14, 2003	Sheet:	20 of 51

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PCMCIA Power Controller



CardBus Socket

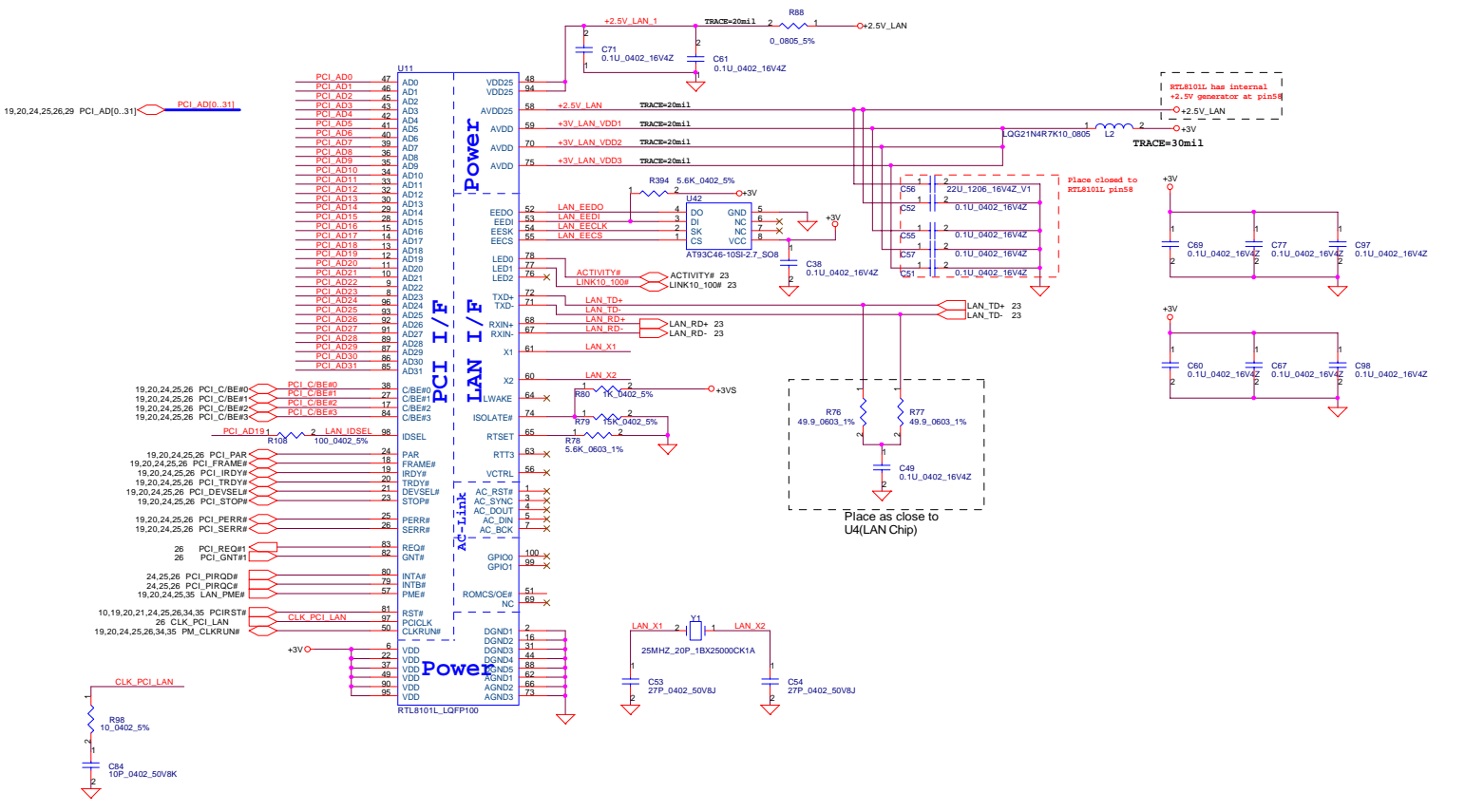


Compal Electronics, Ltd.

File		PCMCIA SOCKET	
Size	Document Number	Rev	
Cust#	LA-2051	1.0	
Date	Friday, November 14, 2003	Sheet	21 of 51

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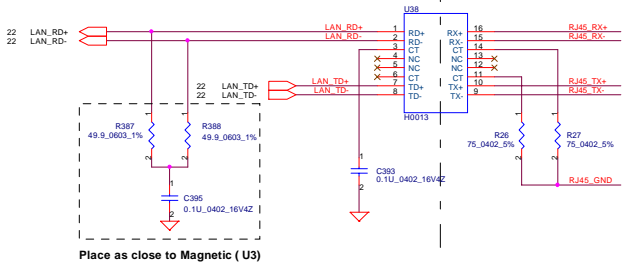
LAN AD19 REQ#1/GNT#1 PCI\_PIRQD#



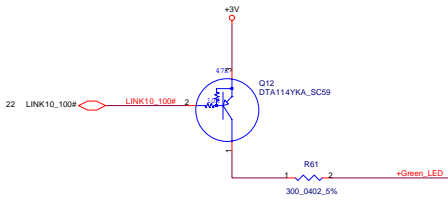
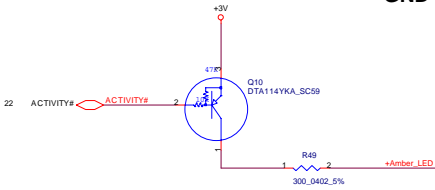
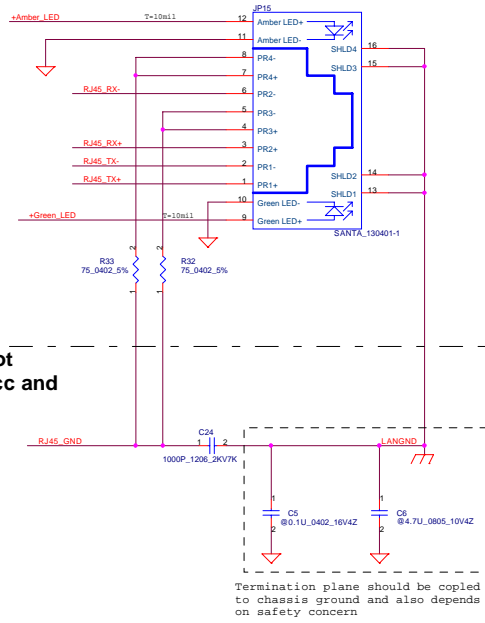
<b>Compal Electronics, Inc.</b>			
Title	LAN REALTEK RTL8101L		
Size	Document Number	Rev	
	LA-2051	1.0	
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# Keep Out 40mil

**Layout Note**  
R0013 pins close to conn.



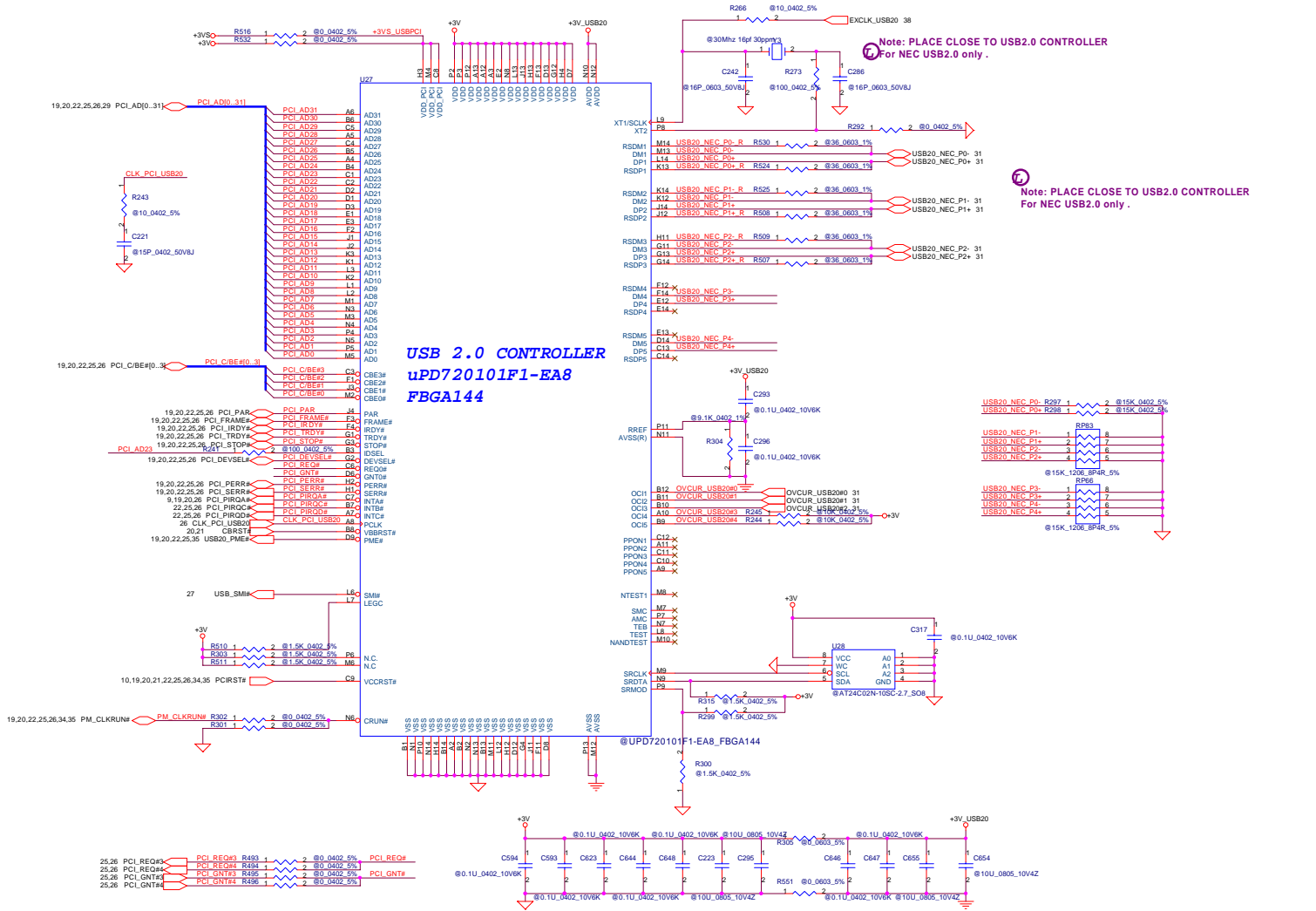
**LAYOUT NOTICE:** This area do not connect to power plan include Vcc and GND in any layer



**Compal Electronics, Ltd.**

File:	RJ11/RJ45 Connector	Rev:	1.0
Size:	Document Number	Date:	Friday, November 14, 2003
Customer:	L A-2051	Sheet:	23 of 51

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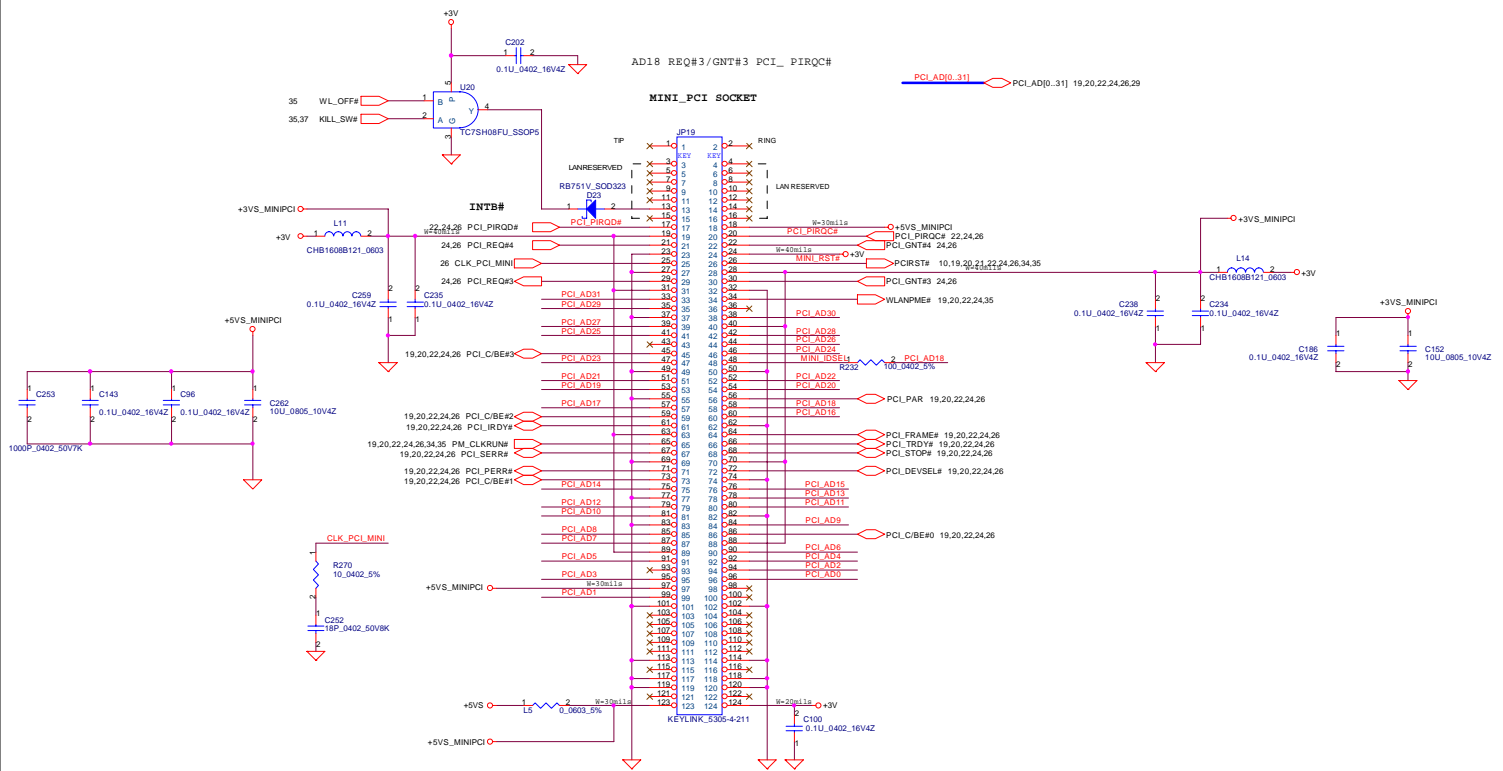


**Compal Electronics, Inc.**

Title: <b>NEC uPD720101 - USB2.0 Controller</b>		Rev: <b>1.0</b>
Size: <b>LA-2051</b>	Document Number: <b>LA-2051</b>	
Date: <b>Friday, November 14, 2003</b>	Sheet: <b>24</b>	of <b>51</b>

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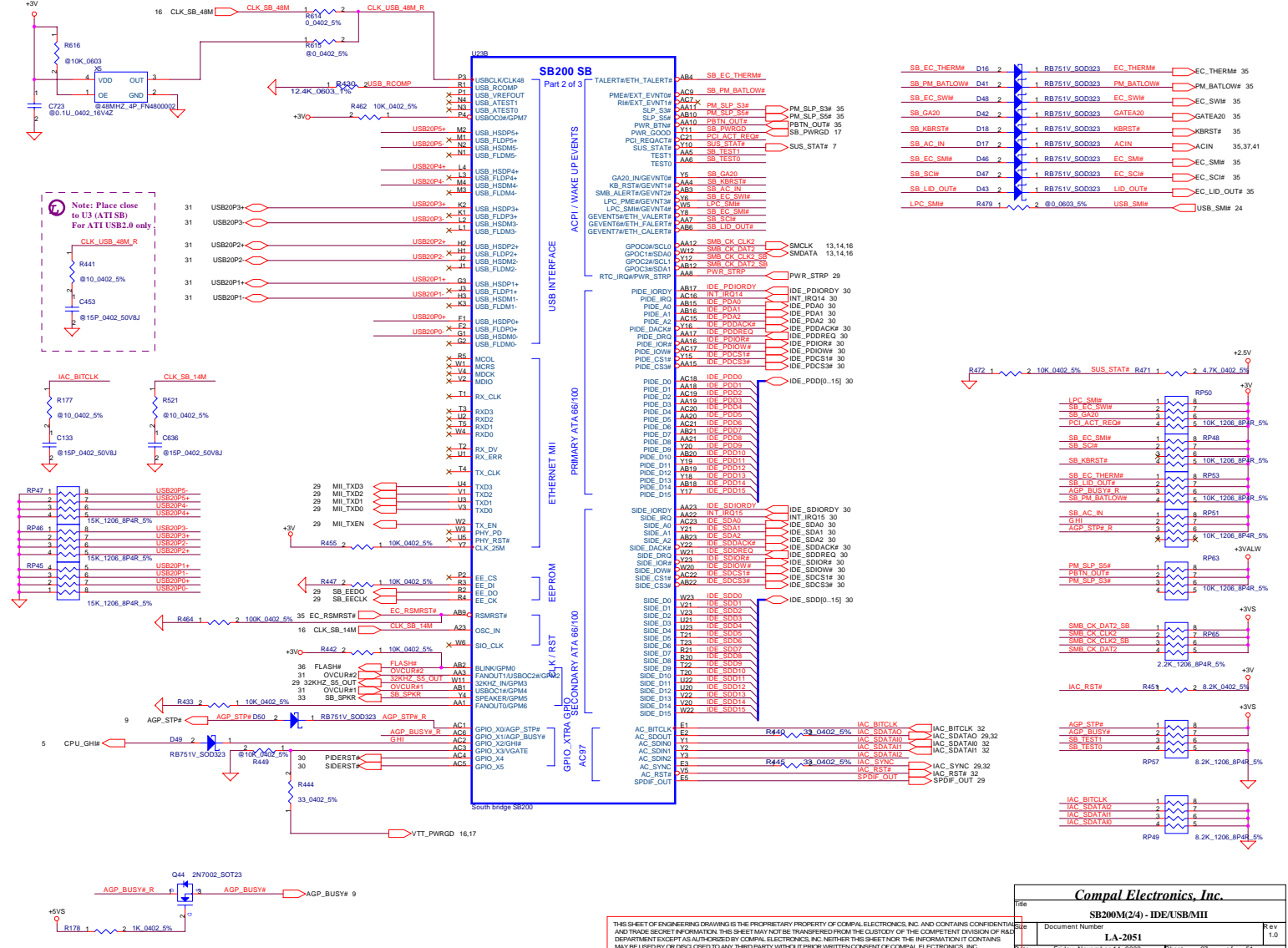




<b>Compal Electronics, Ltd.</b>		
File: <b>Mini PCI Slot</b>		
Size:	Document Number	Rev: 1.0
Customer:	<b>LA-2051</b>	
Date:	Friday, November 14, 2003	Sheet 25 of 51

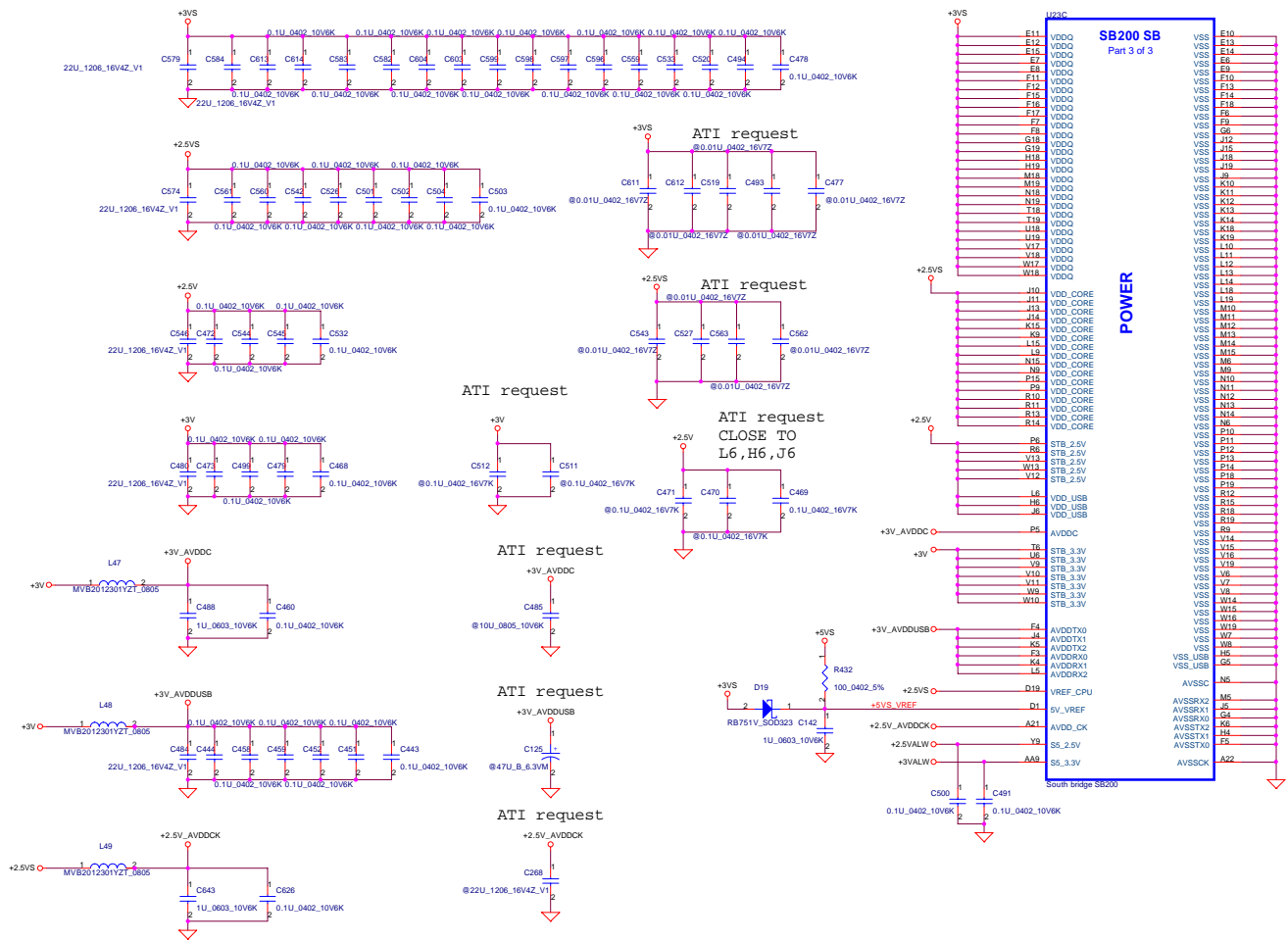
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Title		Document Number		Rev	
SB200M(2/4) - IDE/USBMI		LA-2051		1.0	
Date	Friday, November 14, 2003	Sheet	27	of	51

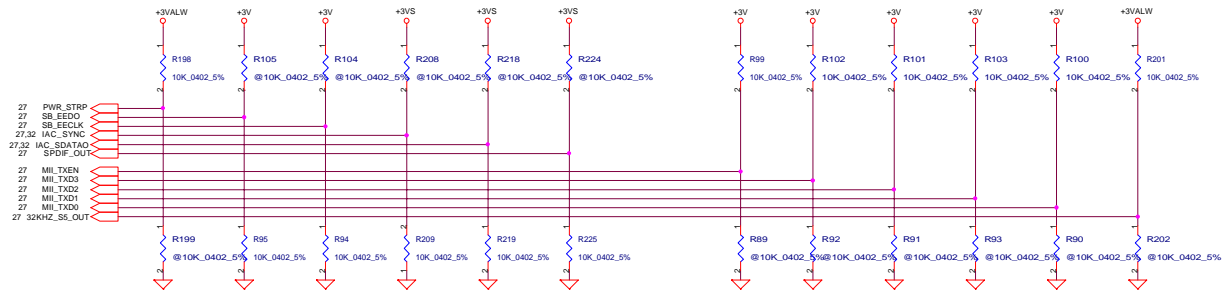


SB200 SB  
Part 3 of 3

POWER

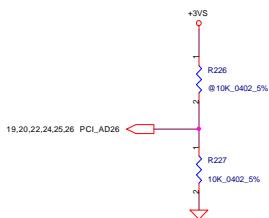
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<b>Compal Electronics, Inc.</b>		
File:	SB200M(3/4) - PWR	
Size:	Document Number	Rev.
	<b>LA-2051</b>	1.0
Date:	Friday, November 14, 2003	Sheet 28 of 81



**REQUIRED SYSTEM STRAPS**

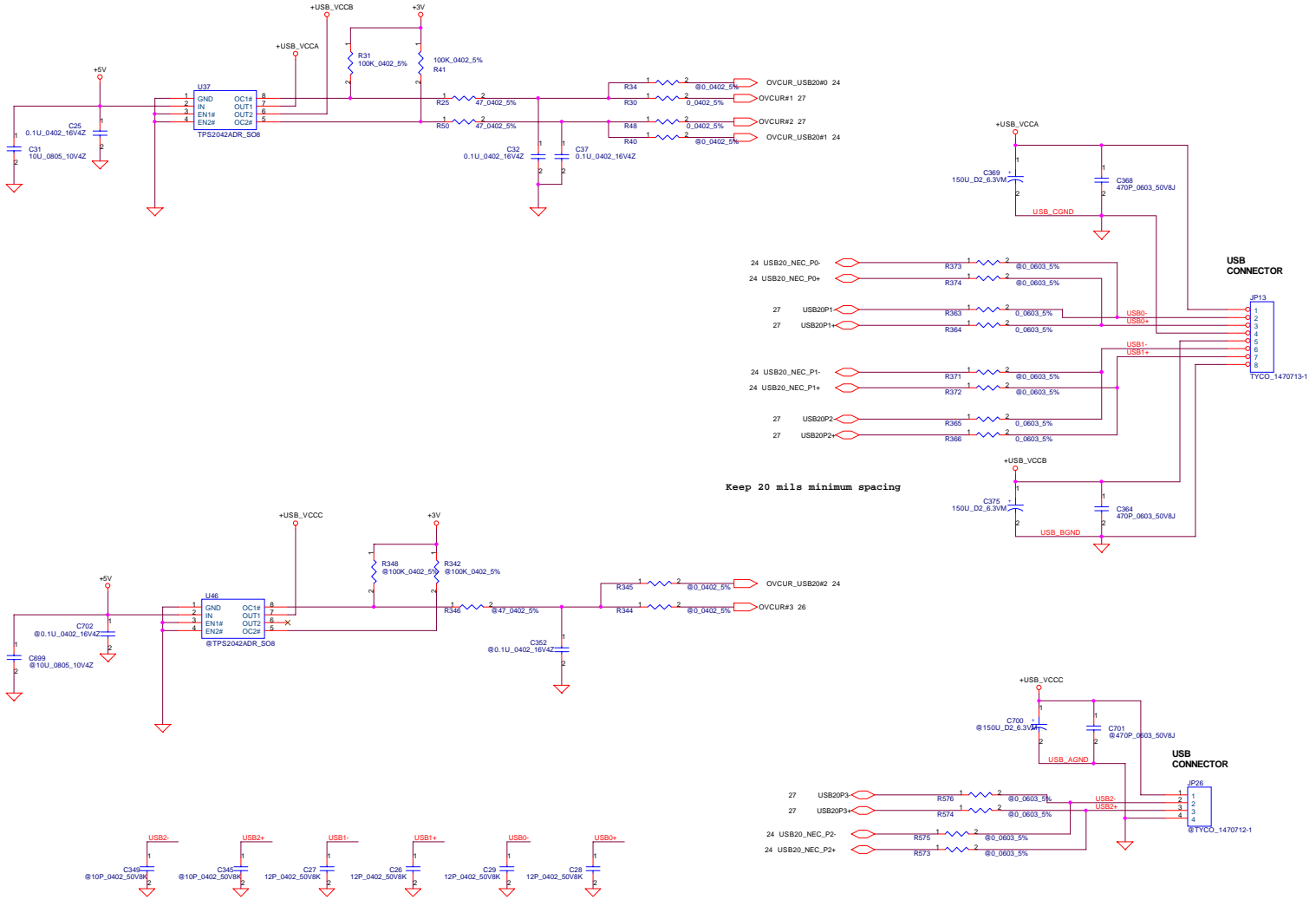
	PWR_STRP	IGN DEBUG EEDD	EECK	AC_SYNC	AC_SDOUT	SPDIF_OUT	SPEEDSTEP CPU_STRP#	FREQLTCH TX_EN	ETHERNET TXD[3:0]	32KHZ_S5
STRAP HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	ROM ON PCI BUS	INIT ACTIVE HIGH	33MHz NB BUS	SIO 24MHz	ENABLE SPEED STEP	DISABLE CPU FREQ SETTING DEFAULT	PROCESSOR FREQ MULTIPLIER	32KHZ OUTPUT FROM SB200 (INT RTC) DEFAULT
STRAP LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	ROM ON LPC BUS DEFAULT	INIT ACTIVE LOW (Pill) DEFAULT	HI SPEED A-LINK DEFAULT	SIO 48MHz DEFAULT	DISABLE SPEED STEP DEFAULT	ENABLE CPU FREQSETTING		32KHZ INPUT TO SB200 (EXT RTC)



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<b>Compal Electronics, Inc.</b>		
File	SB200M(4/4) - STRAPS	
Size	Document Number	Rev
	LA-2051	1.0
Date	Friday, November 14, 2003	Sheet 29 of 81

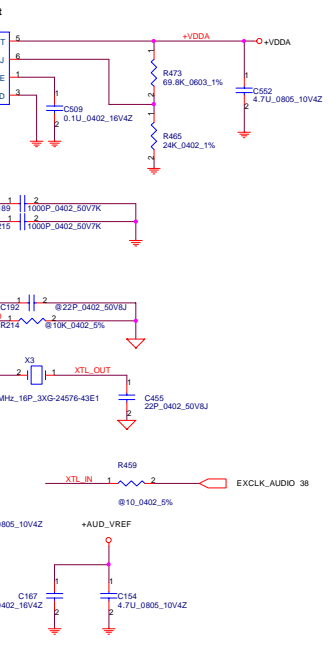
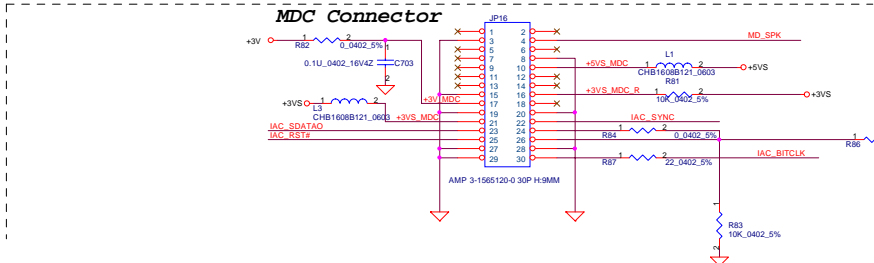
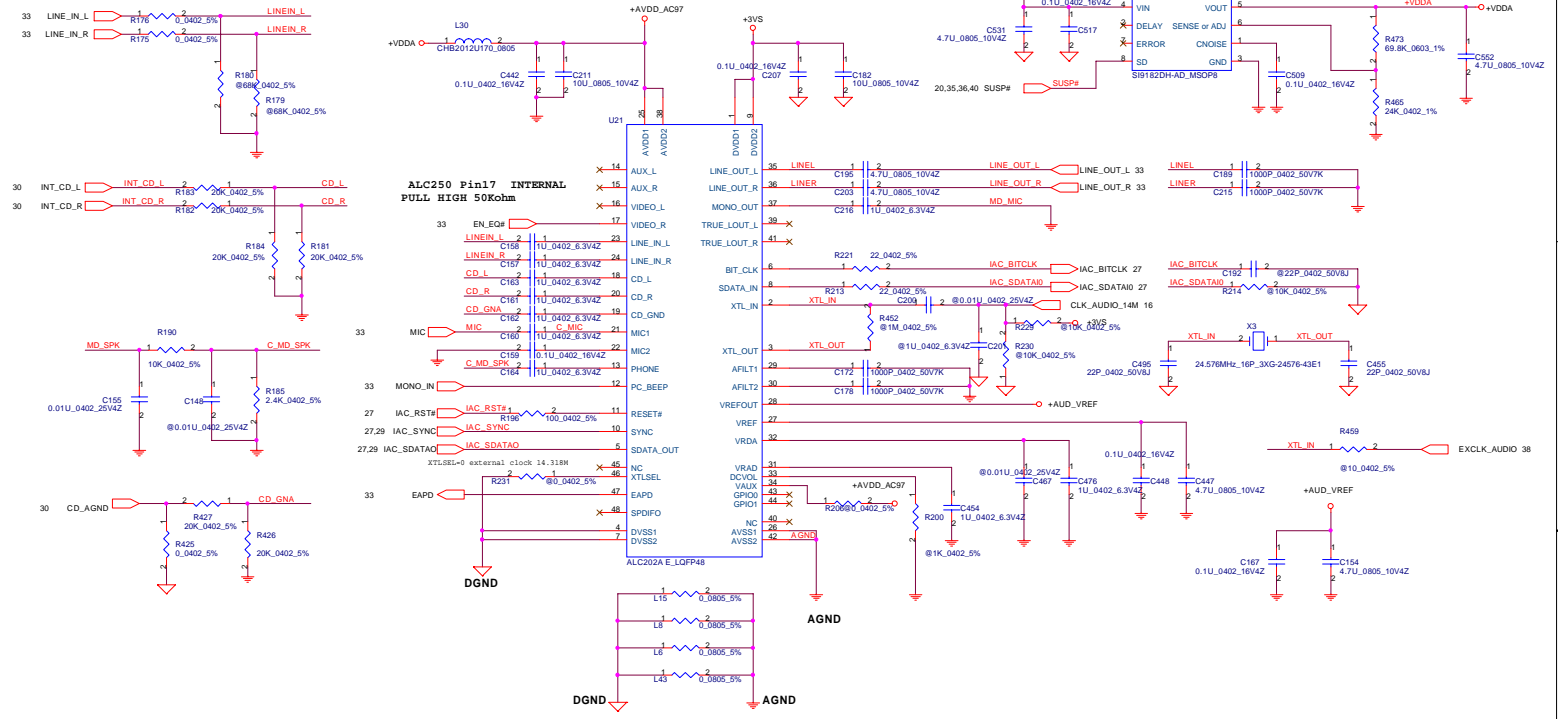




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<b>Compal Electronics, Ltd.</b>			
<b>USB &amp; Bluetooth</b>			
Size	Document Number	Rev	
Cust#	LA-2051	1.0	
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# AC97 Codec

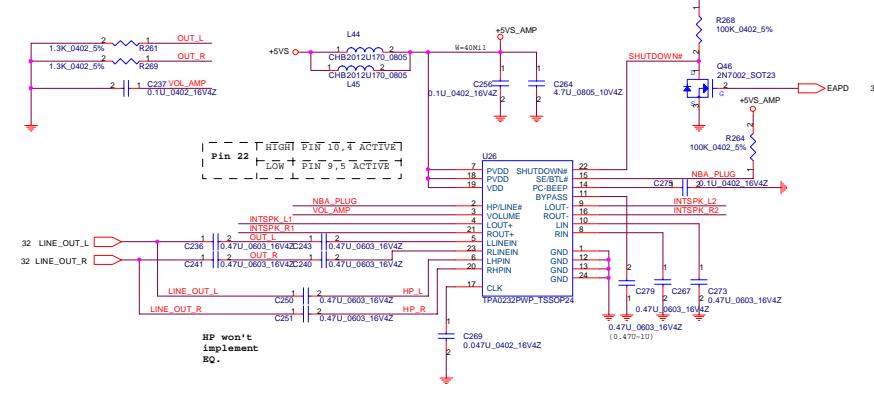


<b>Compal Electronics, Ltd.</b>		
File:	AC97 Codec ALC202	
Doc:	Document Number	R. rev
Customer:	L-A-2051	1.0
Date:	Friday, November 14, 2003	Sheet 32 of 51

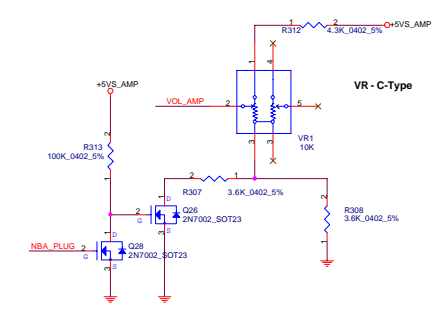
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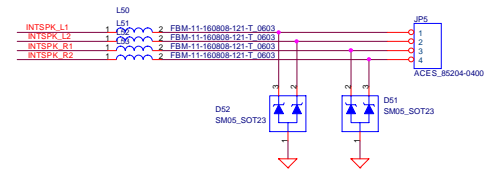
**Audio AMP**



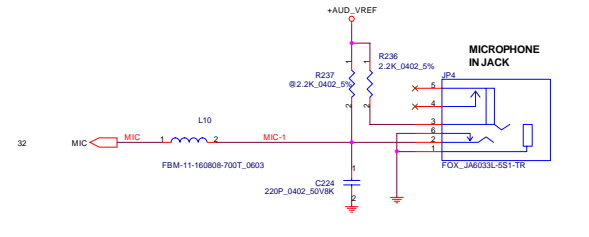
	W/O EQ	
R513	4.3K	
R307	3.6K	
R308	3.6K	
Bias (Gain)	SPK	056 V
		12 dB
		HP
		1.006V
		-2dB



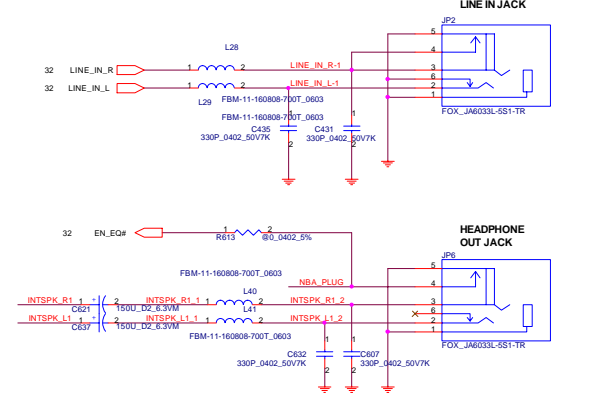
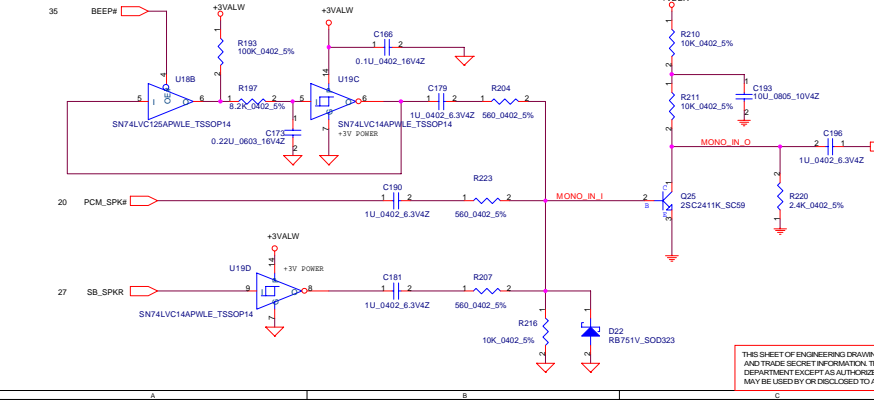
**Speaker Connector**



W/O EQ R385=R386= 1.3K Ohm  
 C537=C539= 0.47U  
 R = R385, R386  
 C = C537, C539  
 $f_o=1/(2*\pi*1.4*R*C)=260Hz$   
 $R=1.3K / C=0.47U$



**System Sound**



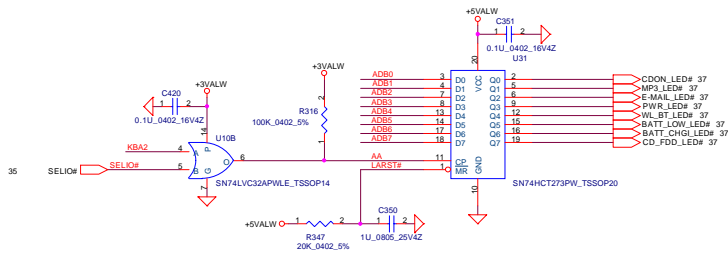
**Compal Electronics, Ltd.**

File: Audio AMP & JACK  
 Size: Document Number  
 Customer: LA-2051  
 Date: Friday, November 14, 2003 Sheet 33 of 51

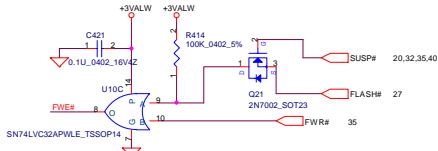
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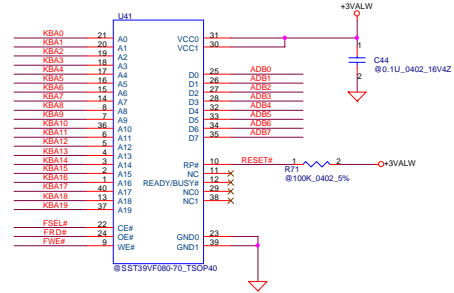
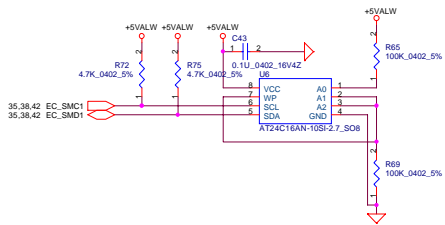
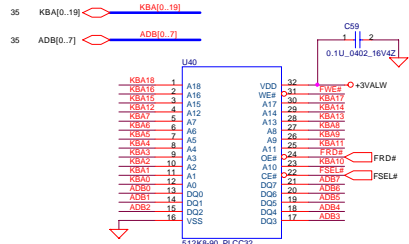




**System BIOS**



**SMBus EEPROM**

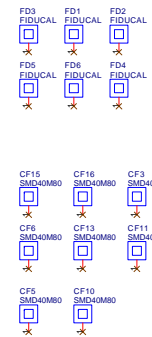
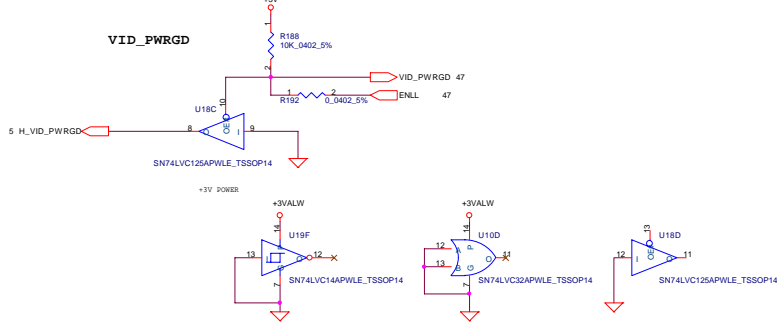


**Compal Electronics, Ltd.**

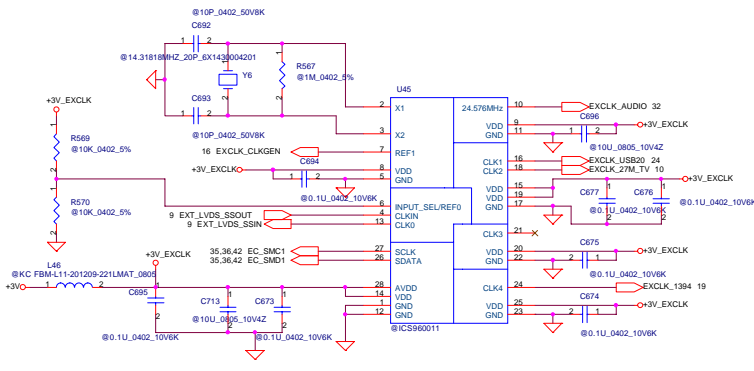
File		BIOS & Ext.I/O	
Size	Document Number	Rev	
LA-2051		1.0	
Date	Friday, November 14, 2003	Sheet	36 of 51

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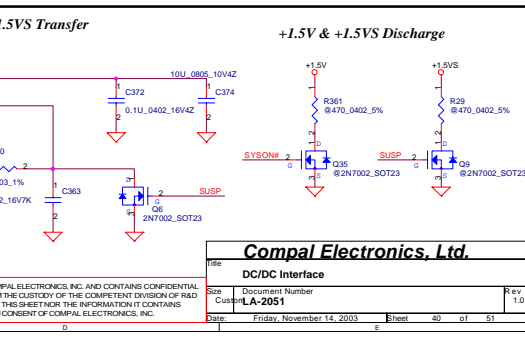
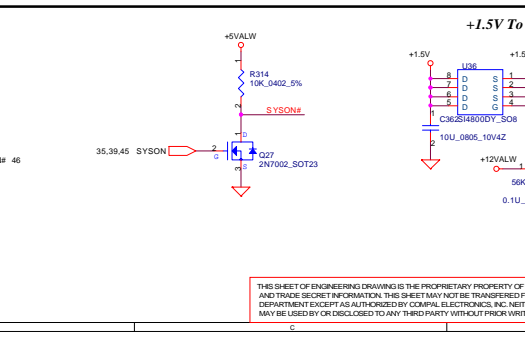
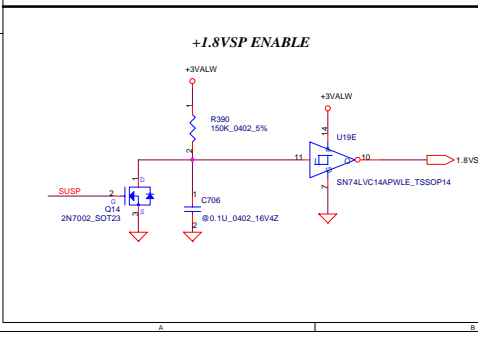
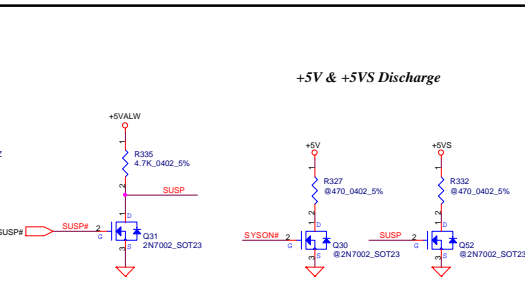
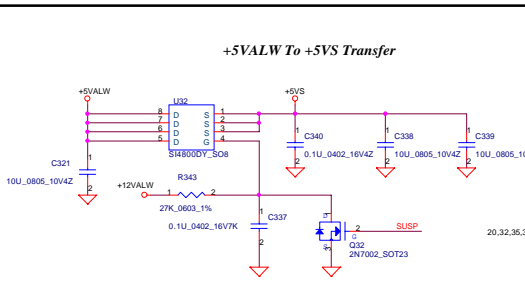
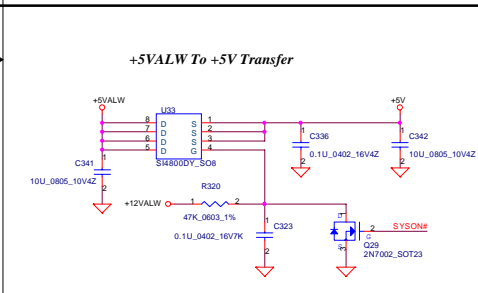
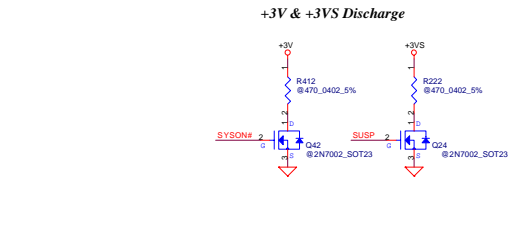
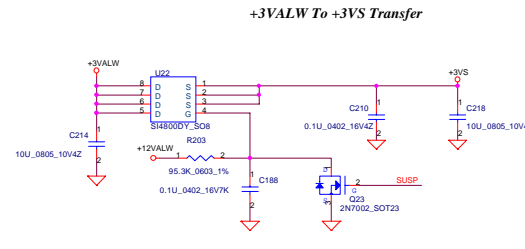
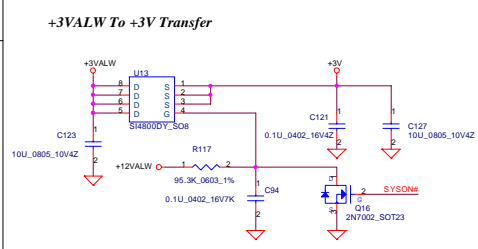
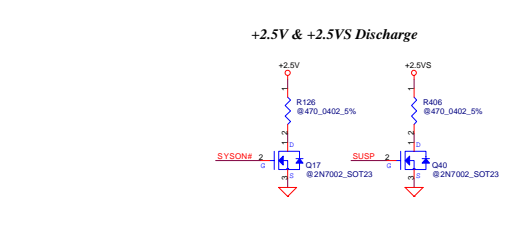
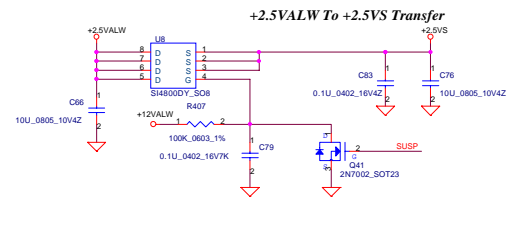
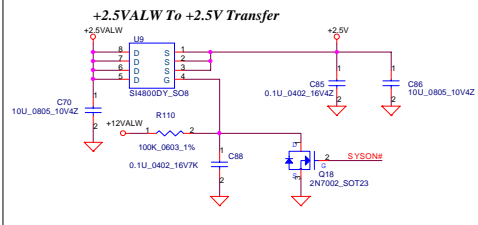
SS ENABLE  
HIGH: ?  
LOW: ?



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<b>Compal Electronics, Ltd.</b>		
File:	PowerGood	
Size:	Document Number	Rev:
Customer:	L.A-2051	1.0
Date:	Friday, November 14, 2003	Sheet 38 of 51



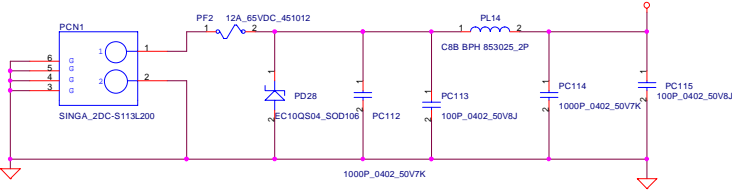


**Compal Electronics, Ltd.**

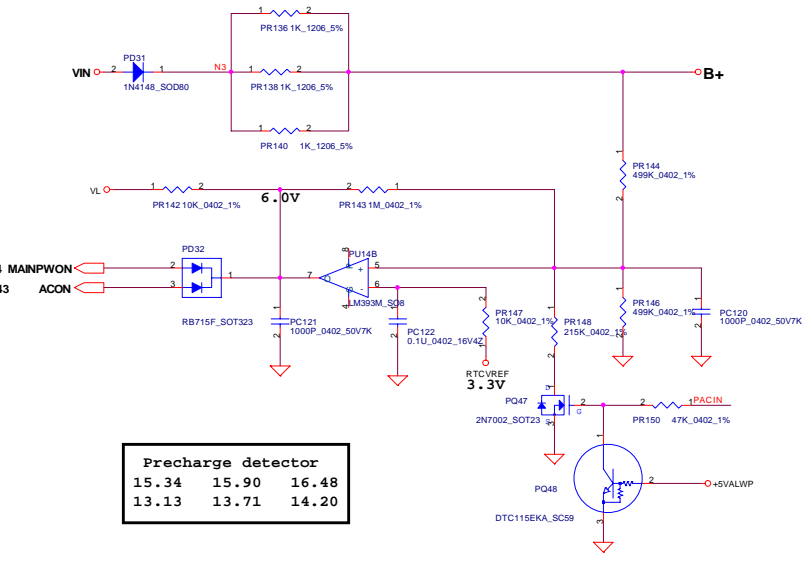
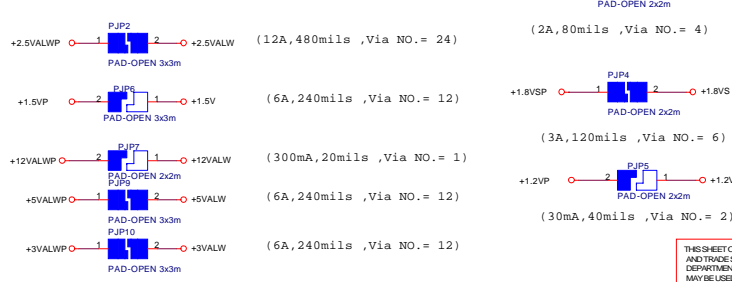
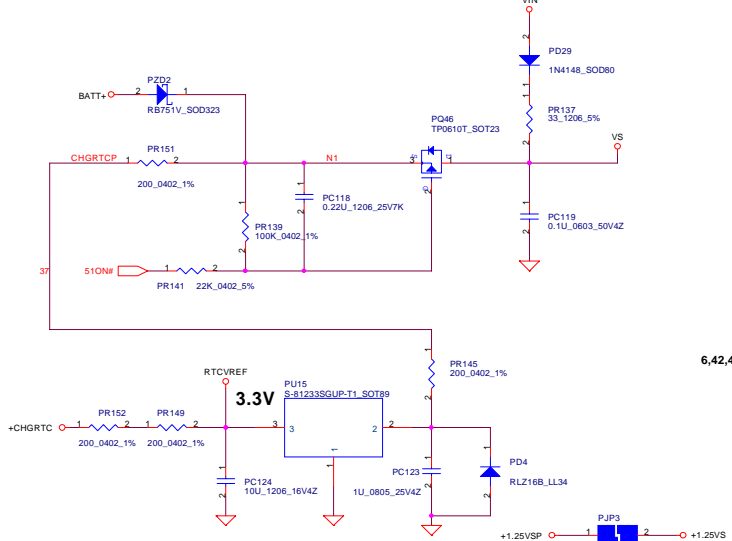
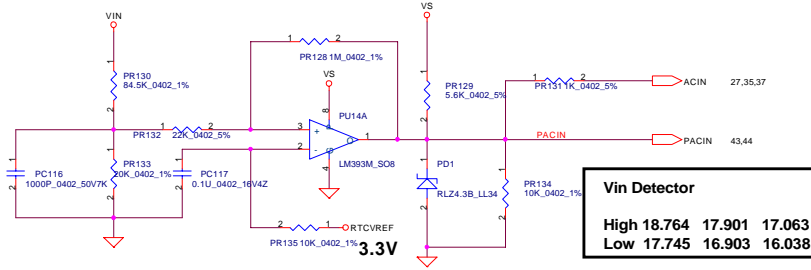
Title: <b>DC/DC Interface</b>		Rev: 1.0
Size: L	Document Number: <b>LA-2051</b>	
Date: Friday, November 14, 2003	Sheet: 40	of 51

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SINGA_2DC-S133L200	120W
SINGA_2DC-S726B201	90W

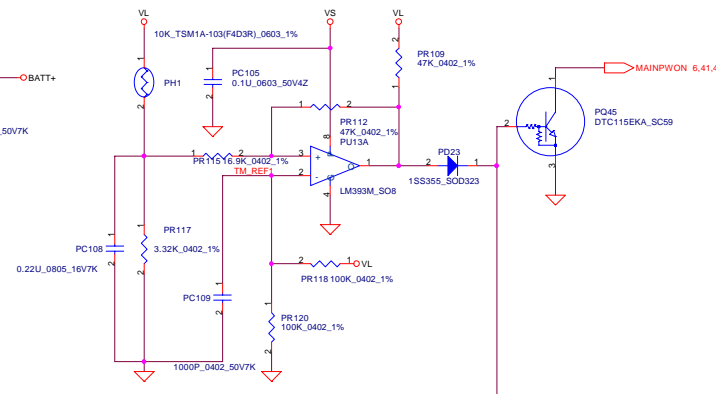
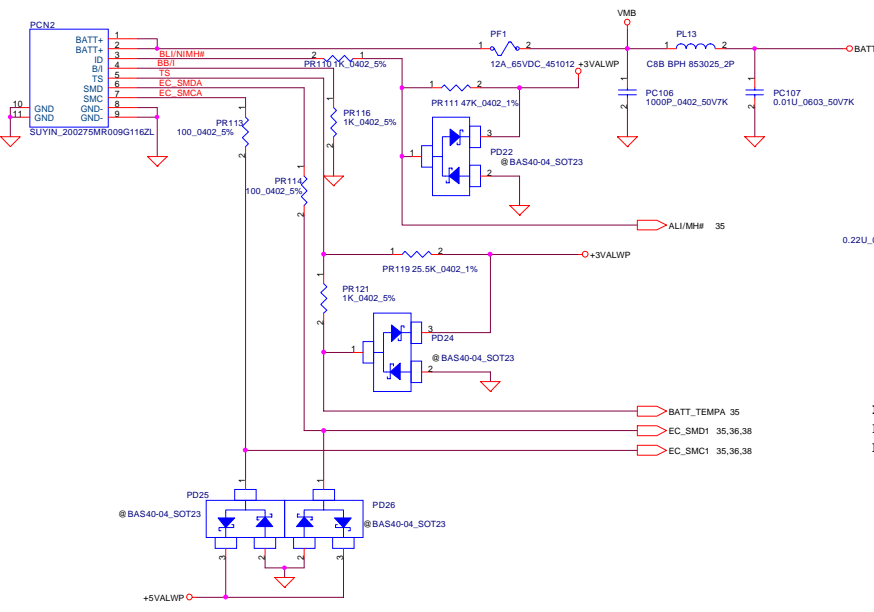


Precharge detector		
6.42,44	15.34	15.90
43	13.13	13.71
MAINPWON	16.48	14.20
ACON		

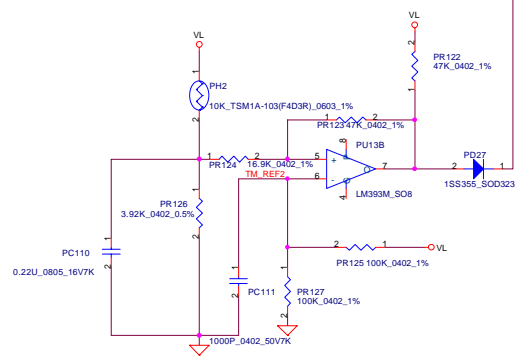
<b>Compal Electronics, Ltd.</b>		
Title	DCIN/DECTOR	
Size	Document Number	Rev
B		1.0
Date:	Friday, November 14, 2003	Sheet 41 of 51

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**PH1 under CPU bottom side :**  
 CPU thermal protection at 84 degree C  
 Recovery at 44(45) degree C



**PH2 near main Battery CONN :**  
 BAT. thermal protection at 78 degree C  
 Recovery at 39(40) degree C



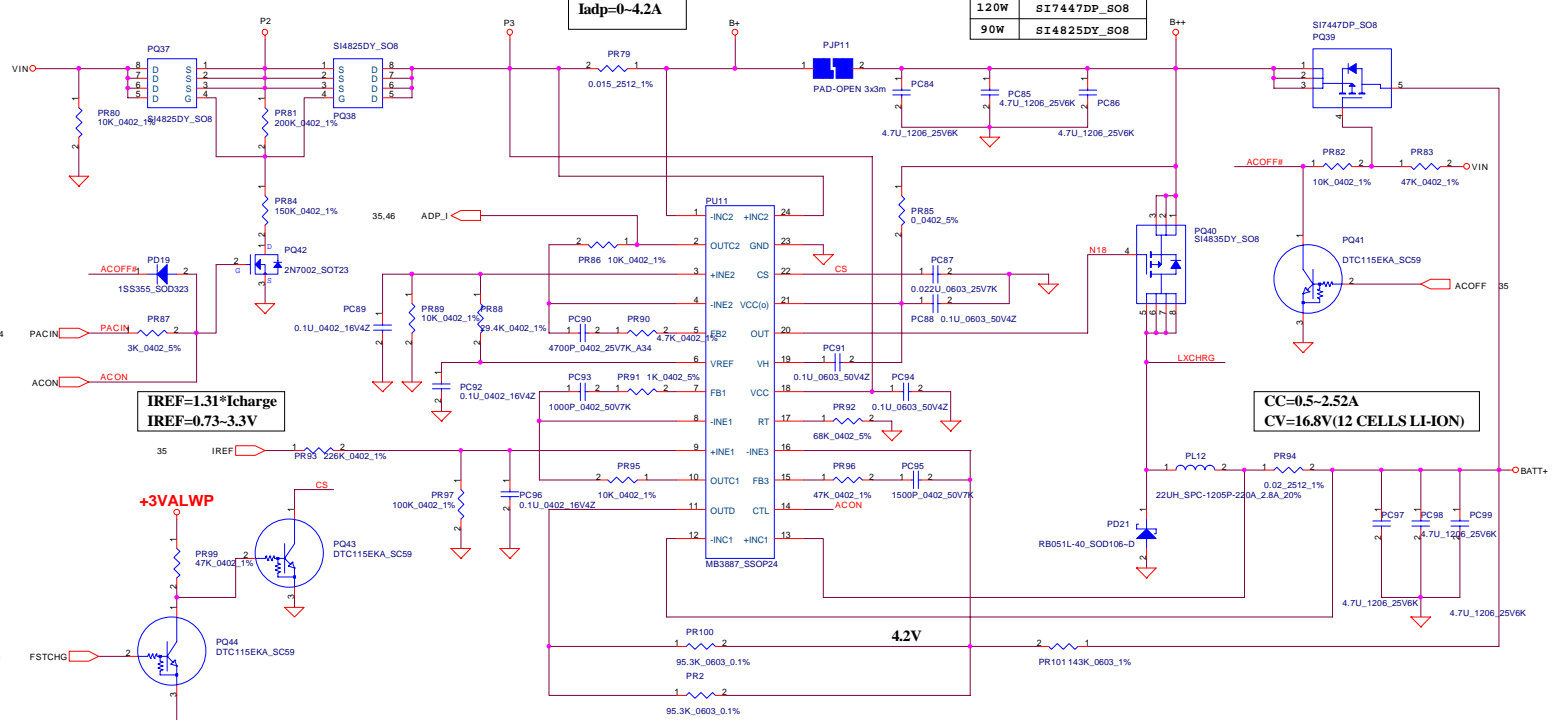
**Compal Electronics, Ltd.**

Title		BATTERY CONN/OTP
Size	Document Number	Rev
B		1.0
Date:	Friday, November 14, 2003	Sheet 42 of 51

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**Iadp=0-4.2A**

	<b>PQ39</b>
<b>120W</b>	<b>SI7447DP_S08</b>
<b>90W</b>	<b>SI4825DY_S08</b>



**IREF=1.31\*Icharge**  
**IREF=0.73-3.3V**

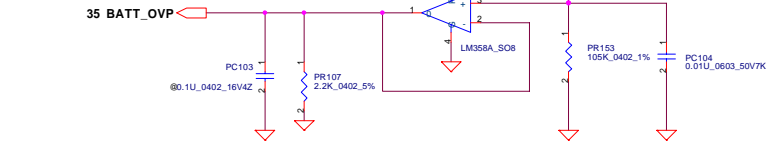
**+3VALWP**

**CC=0.5-2.5A**  
**CV=16.8V(12 CELLS LI-ION)**

**4.2V**

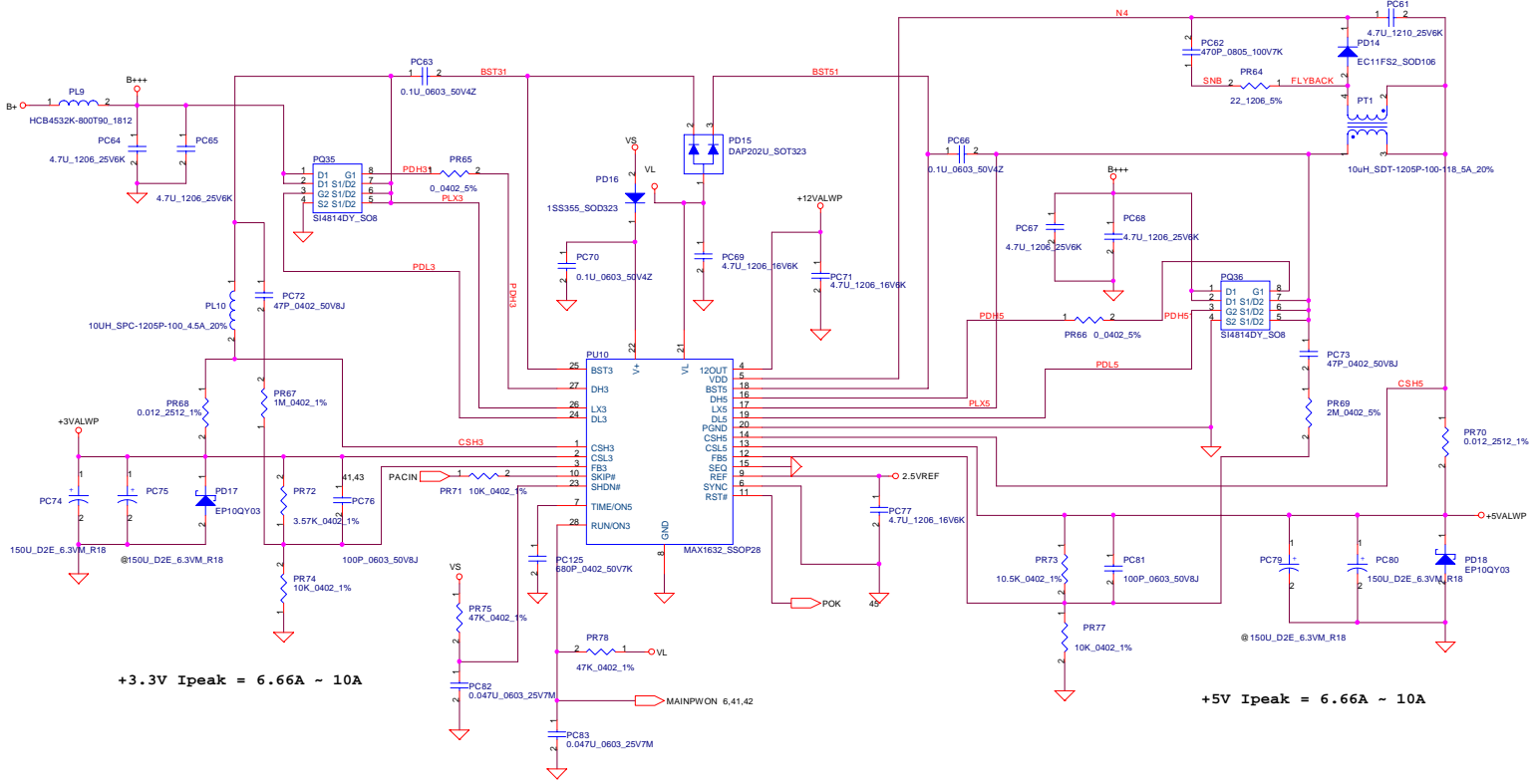
**OVP voltage : LI**  
4S3P : 18V--> BATT\_OVP= 2.0V  
3S4P/3S3P : 13.5V--> BATT\_OVP= 1.5V  
**(BATT\_OVP=0.1111 \*VMB)**

	<b>120W</b>	<b>90W</b>
<b>PR79</b>	<b>0.01_2512_1%</b>	<b>0.015_2512_1%</b>
<b>PR86</b>	<b>100K_0402_1%</b>	<b>10K_0402_1%</b>
<b>PR88</b>	<b>33.2K_0402_1%</b>	<b>29.4K_0402_1%</b>
<b>PR90</b>	<b>10K_0402_5%</b>	<b>4.7K_0402_5%</b>



<b>Compal Electronics, Ltd.</b>		
Title	<b>CHARGER</b>	
Size	Document Number	Rev
B	<b>LA-2051</b>	1.0
Date	Friday, November 14, 2003	Sheet 43 of 51

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**+3.3V Ipeak = 6.66A ~ 10A**

**+5V Ipeak = 6.66A ~ 10A**

<b>Compal Electronics, Ltd.</b>		
Title	5V3V12V	
Size	Document Number	Rev
B	LA-2051	1.0
Date:	Friday, November 14, 2003	Sheet 44 of 51

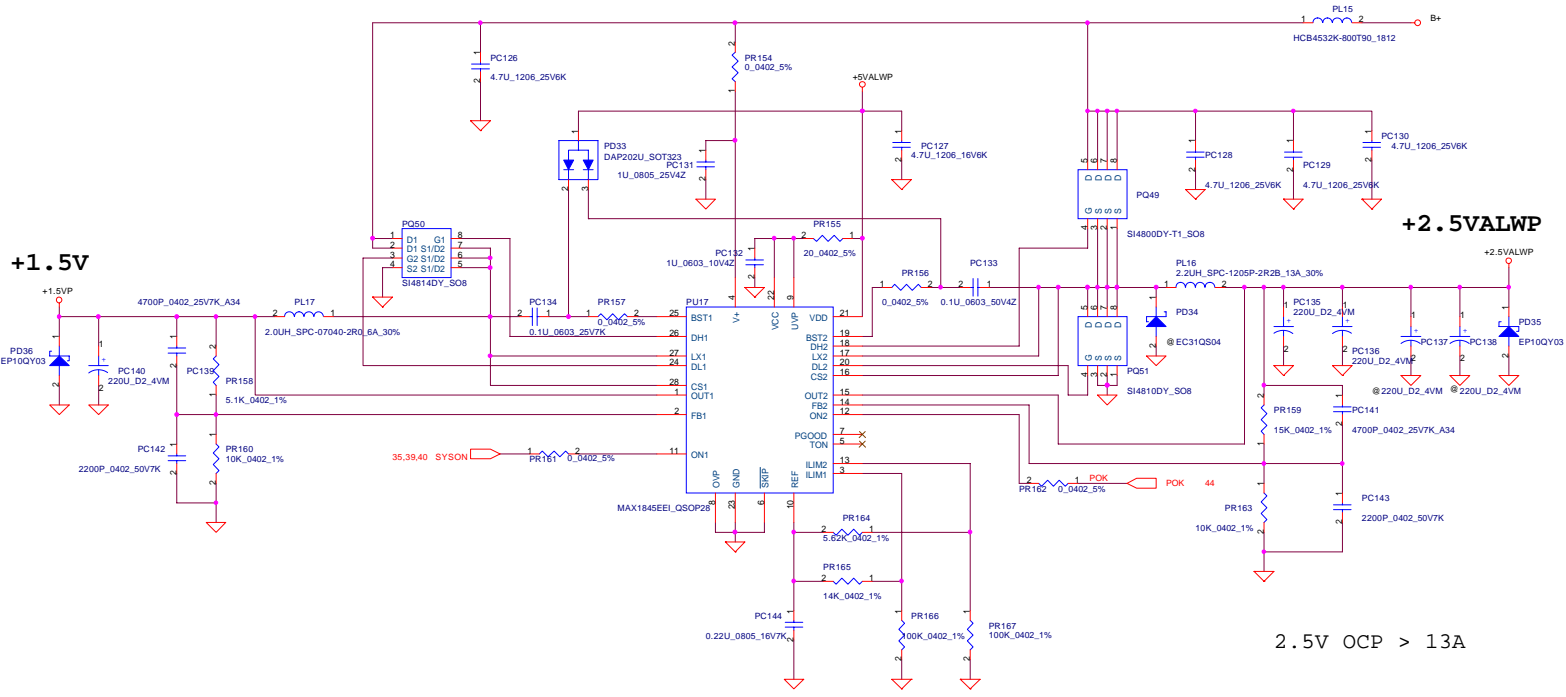
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+2.5VALWP/+1.5VP

+1.5V

+2.5VALWP

2.5V OCP > 13A

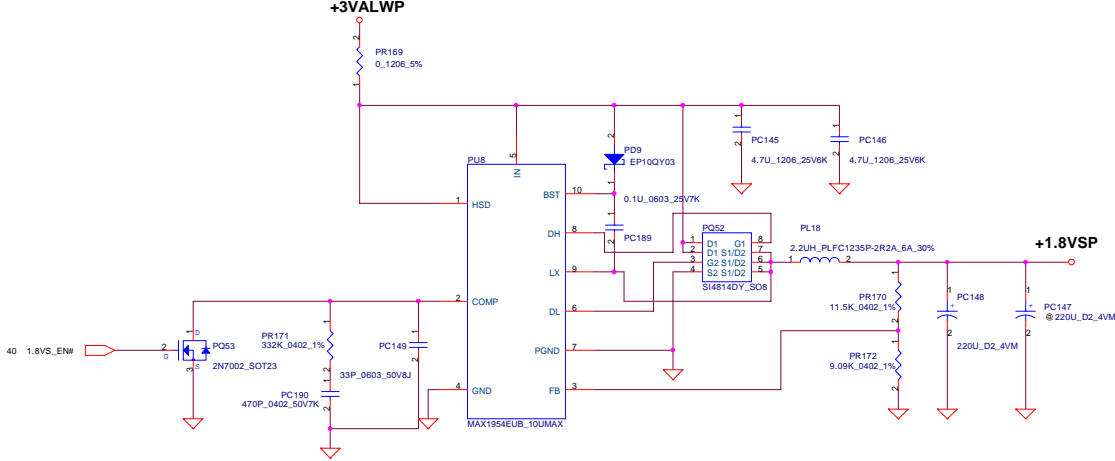


**Compal Electronics, Ltd.**

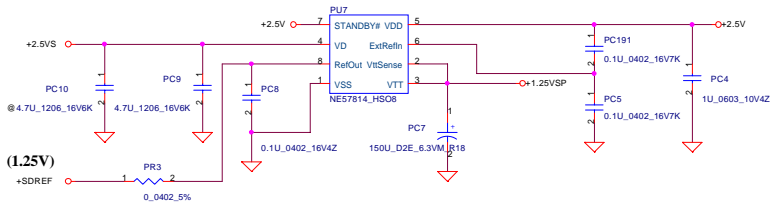
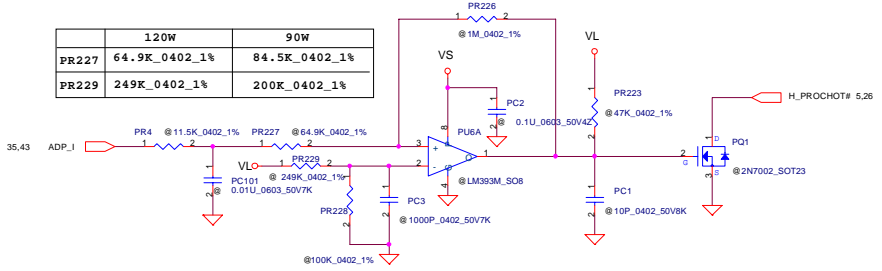
Title		<b>+2.5VALWP/1.5VP</b>	
Size	Document Number	Customer <b>LA-2051</b>	
Date	Friday, November 14, 2003	Sheet	45 of 51

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Rev 1.0



	120W	90W
PR227	64.9K_0402_1%	84.5K_0402_1%
PR229	249K_0402_1%	200K_0402_1%

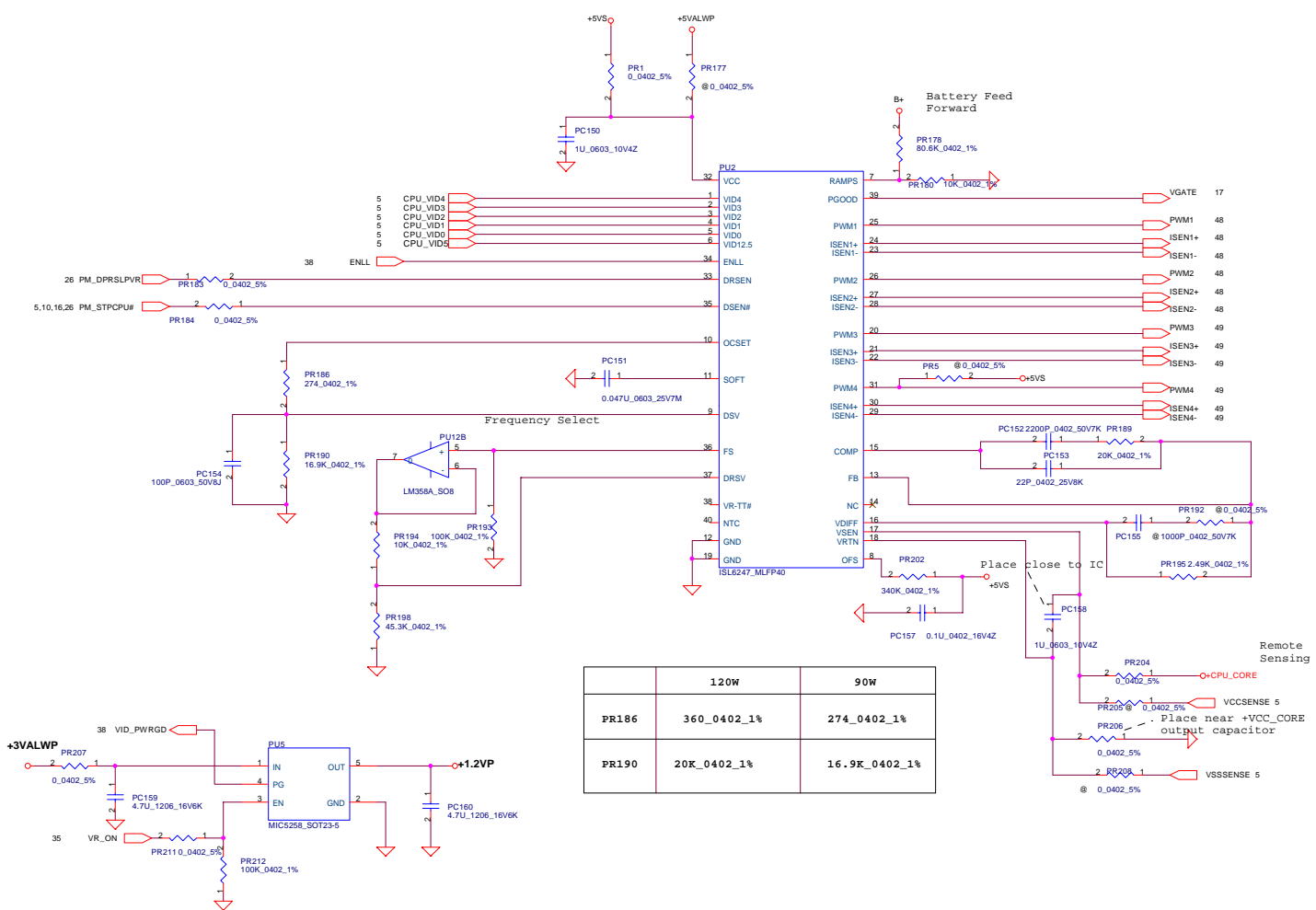


**Compal Electronics, Ltd.**

Title	+1.25VSP/+1.8VSP		
Size	Document Number		Rev
Cus	LA-2051		1.0
Date	Friday, November 14, 2003	Sheet	46 of 51

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	120W	90W
PR186	360_0402_1%	274_0402_1%
PR190	20K_0402_1%	16.9K_0402_1%

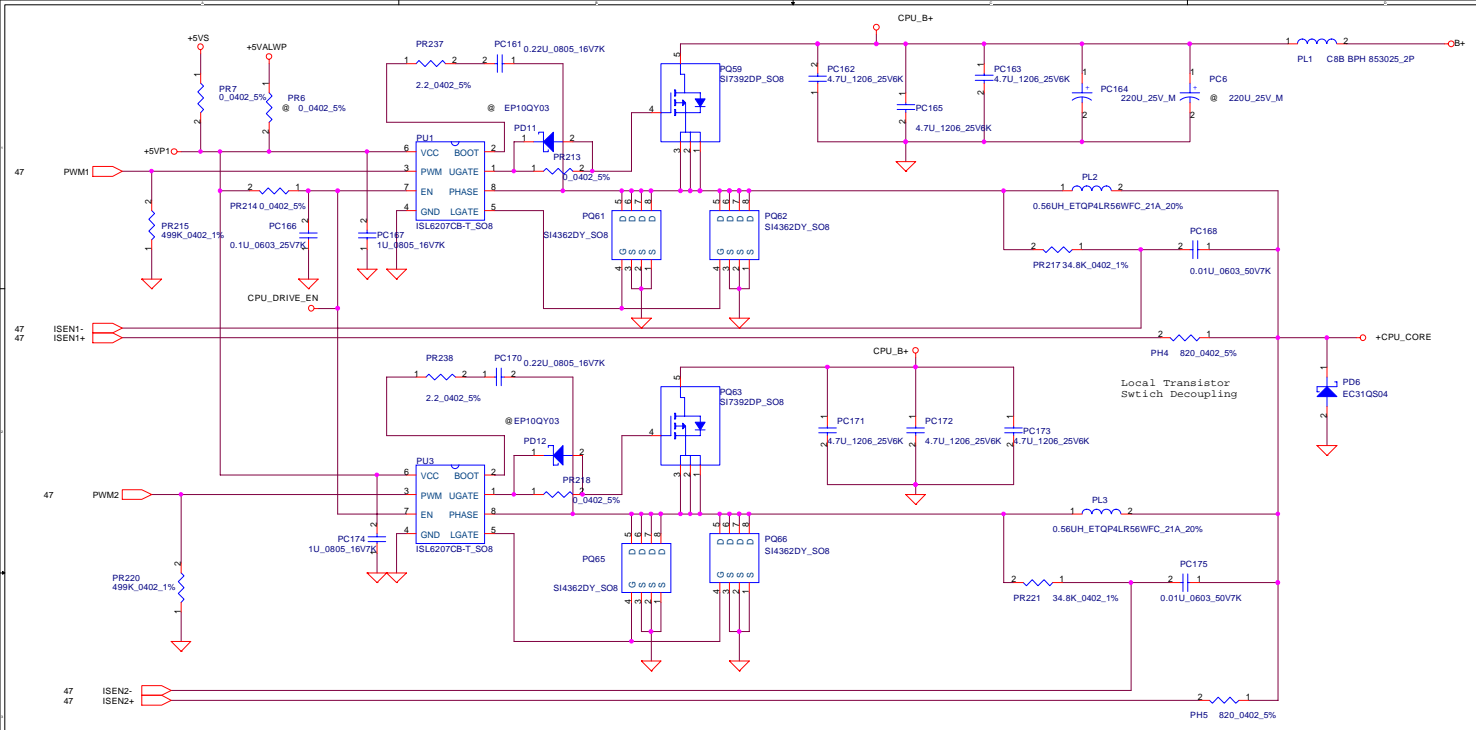
**Compal Electronics, Ltd.**

Title: **CPU CORE Controller**

Size: B      Document Number: **LA-2051**      Rev: 1.0

Date: Friday, November 14, 2003      Sheet: 47 of 51

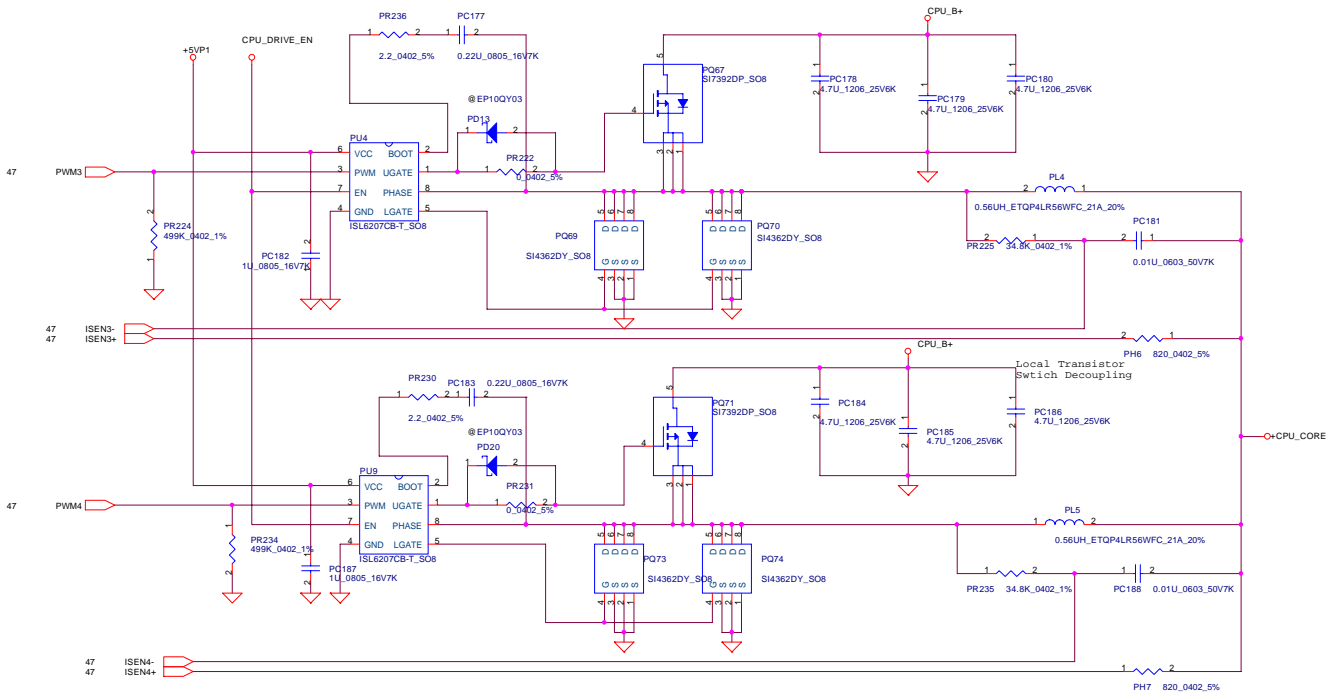
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<b>Compal Electronics, Ltd.</b>		
<b>Document Number</b>		
<b>LA-2051</b>		
Date	Friday, November 14, 2003	Sheet 48 of 51

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	3 PHASE	4 PHASE
UNPOP	FU9, PC187, PR234, PR230, PC183, PQ71 PQ73, PQ74, PR231, PR235, PL5, PC188, PH7	PR5
POP	PR5	FU9, PC187, PR234, PR230, PC183, PQ71 PQ73, PQ74, PR231, PR235, PL5, PC188, PH7

<b>Compal Electronics, Ltd.</b>			
Title	CPU_CORE Power stage		
Size	Document Number	Rev	
Cust	A-2051	1.0	
Date:	Friday, November 14, 2003	Sheet	49 of 51

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REV 0.1	Date	Page	Description	Location
09/12	P.13,P.14		Del DDR data damping	DEL RP40,RP43,RP44,RP54,RP59,RP64,RP67,RP70,RP74,RP82,RP5,RP8,RP10,RP12,RP16,RP26,RP29,RP31,RP34,RP36.
09/12	P.13,P.14		Add DDR address & control damping	ADD R592,R593,R594,R595,R596,R597,R598,R599
09/15	P.27		LPC_SMI# Pull high to +3V	LPC_SMI# connect to RP50 Pin 1
09/16	P.27		Del ATI USB feedback resistor	DEL R438,R439,R446,R448,R434,R435
09/16	P.31		Change USB form NEC to ATI	DEL R34,R40,R373,R374,R371,R372,R575,R573,R345 ADD R30,R48,R363,R364,R365,R366,R574,R576,R344
09/20	P.18		Change LVDS Conn to 40 pin	Change JP1
09/20	P.16		Disconnect CPU_STP# & PCI_STP#	DEL R579,R580 ADD R577,R578
09/20	P.24		Del external USB chip	DEL U27,R516,R241,R510,R303,R511,R302,R300,R315,R245,U28,R244,R304,R530,R524,R508,R509,R507,C242,C286,Y3,R273,R297,R298,RP83,RP66,C654,C655,C647,C646,R305,R551,R494,R496
09/22	P.33		Add bead between +5VS & +5V AMP	ADD L44,L45
09/22	P.32		Reserve LAN AC97-link to MDC	Reserve ADD R604,R605,R606,R607,R608,R609,R610,R612
10/15	P.27,35		Fix PME function	Del R421 and change EC591 EC_SWI#(pin70) connect to SB200 EXT_EVENT1 to SB200 GEVENT3#,Del LPC_PME#
10/15	P.10,16		Change NB CLK Voltage	Change R161=68,R506=56
10/16	P.27		Add USB 48M OSC	Add R614,R615,R616,C723,X5
10/16	P.8,13,14		Add 0.1uF between +SDREF & +2.5V	Add C724,C725,C726
10/16	P.28		Change R to L	Change R460,R475,R528 to L47,L48,L49
10/16	P.26		Solve CMOS reset when AC-IN	Change R589 from 1k to 0 ohm
10/17	P.35		Change PCIRST# to NB_RST# for ATI suggestion,change SIO and IDE & EC	Add R617,R618,R619,R620
10/17	P.10		Modify Q45	Mirror Q45
10/17	P.26		Modify R558	Reserve R558
10/17	P.26		Modify R558	Reserve R558
10/17	P.27,31		Change USB port form 0-2 to 1-3, because Port 0 have some problem	
10/17	P.28		Change R432 from 1k to 100 ohm for ATI suggestion	
10/20	P.33		change R312 from 3k to 4.3k to follow DBL10 gain	
10/20	P.33		Add L50,L51,L52,L53 for EMI request	
10/20	P.37		Add D57 for BSD	
10/20	P.25		change C252 form 10P to 18P for EMI	
10/23	P.34		Del R116 to fix FIR signal level drop	
10/23	P.31		Add C26,C27,C28,C29 for USB 2.0 EMI	
10/23	P.26		Change R242 from 33ohm to 39ohm for EMI	
11/07	P.26,35		Change X1,Y4 footprint	
11/07	P.35		Add R621,R623-R626 for board ID	
11/07	P.39		C35 change to X7R	
11/07	P.17		Delete R106 for SB_PWRGD timing	
11/07	P.34		Add R116 for FIR disconnect Issue	
11/07	P.15		C322,C686,C92,C93 change to 220uF/25mohm for RST issue	
11/07	P.38		Delete J1,J2 for EMI	
11/13	P.26		Add R627 for USB2.0 wakeup	
11/14	P.9		Add R628 for ENVDD goes high Issue	

<b>Compal Electronics, Ltd.</b>		
File: HW PIR		
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10/28 P.40 Delete PL11 for mechanic request  
10/28 P.41.43 Change PC7,PC74,PC80 from SGA20151300 to SGA20151320 for battery only not boot  
10/28 P.42.43 Change PC148,PC135,PC136,PC140 from SGA20221150to SGA20221130 for battery only not boot  
10/28 P.44 Change PC152 from SE074102K00 to SE074222K00 for prevent DBL10 system cannot resume from standby  
10/28 P.44.45 Add PR7,PR1 delete PR177 to prevent DBL10 system cannot resume from standby

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