

LA-1641 REV0.2 Schematic Document

Intel Mobile P4 uFCBGA/uFCPGA Northwood Celeron
with Montara GML / ICH4-M / Integrated VGA

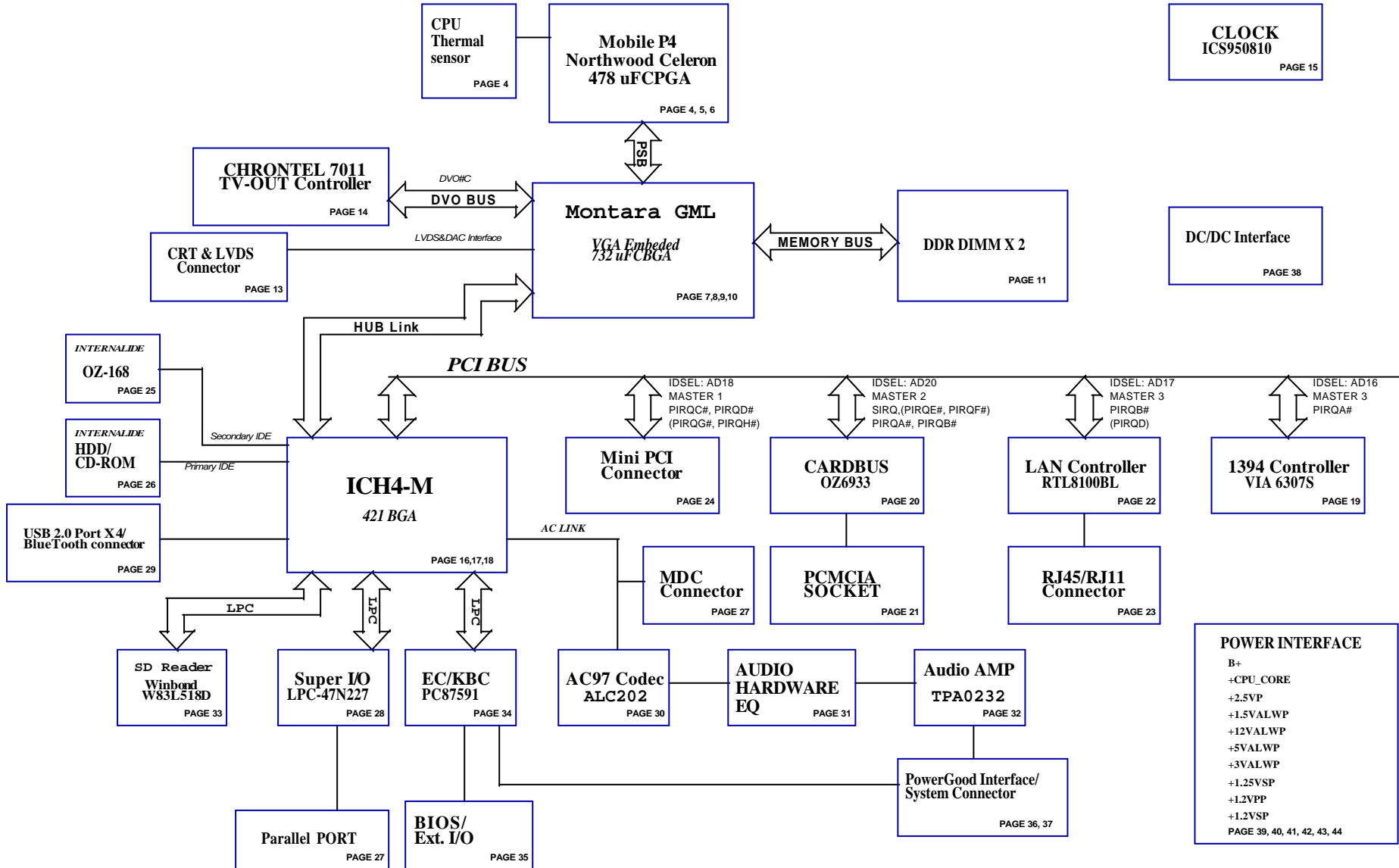
2002-11-20



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COMPAL CONFIDENTIAL

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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit	N/A	N/A	N/A
+CPU_VCC	Core voltage for CPU	ON	OFF	OFF
+1.2VP	1.2V switched power rail for CPU AGTLBus	ON	OFF	OFF
+1.2VS	1.2V switched power rail for Montara core	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VS	AGP 4X	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTC_VCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

External PCI Devices

Device	IDSEL#	REQ#/GN#	Interrupts
CardBus	AD20	2	PIRQA/PIRQB(PIRQE/PIRQF)
LAN	AD17	3	PIRQB(PIRQD)
Mini-PCI	AD18	1/1	PIRQC/PIRQD(PIRQG/PIRQH)
1394	AD16	0	PIRQA

EC SM Bus1 address

Device	Address
Smart Battery	0001 011X b
EEPROM(24C16/02)	1010 000X b
(24C04)	1011 000Xb

EC SM Bus2 address

Device	Address
ADM1032	1001 110X b
OZ168	0011 0100 b
Smart Battery	0001 011X b
Docking	0011 011X b
DOT Board	XXXX XXXXb

ICH4 SM Bus address

Device	Address
Clock Generator (ICS-950810)	1101 001X

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

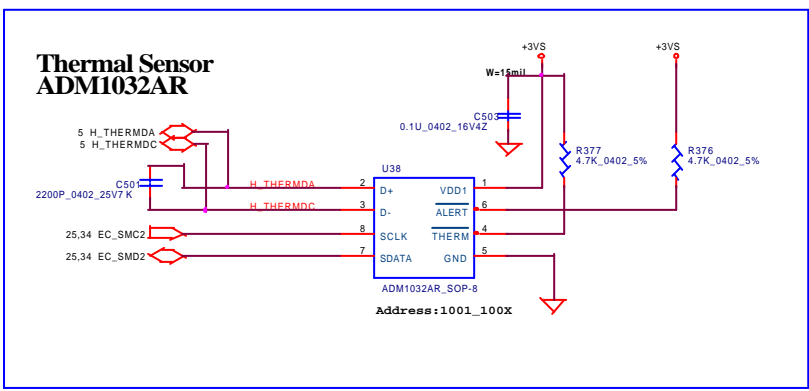
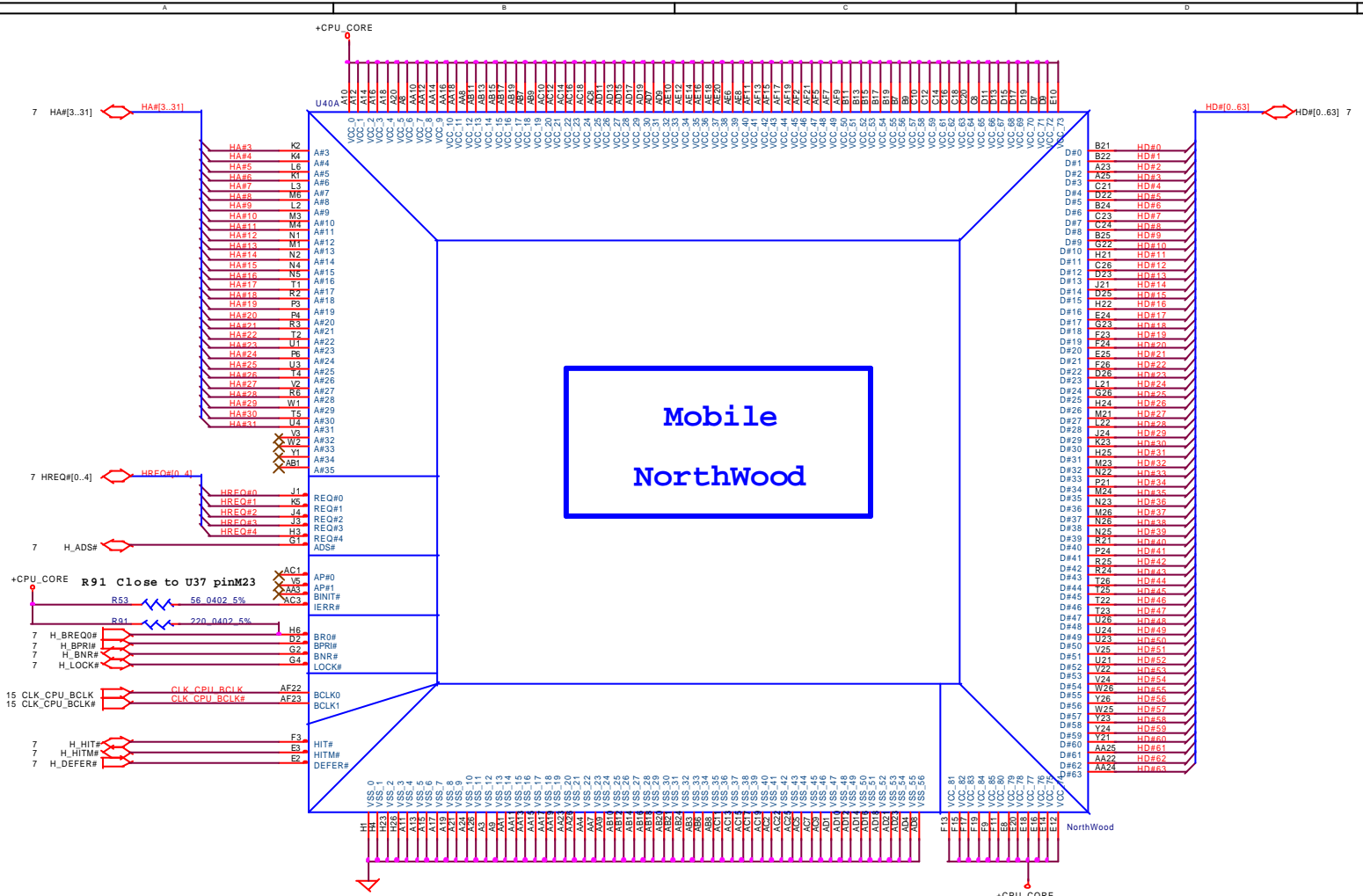
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	0.4
4	0.5
5	0.6
6	0.7
7	0.8

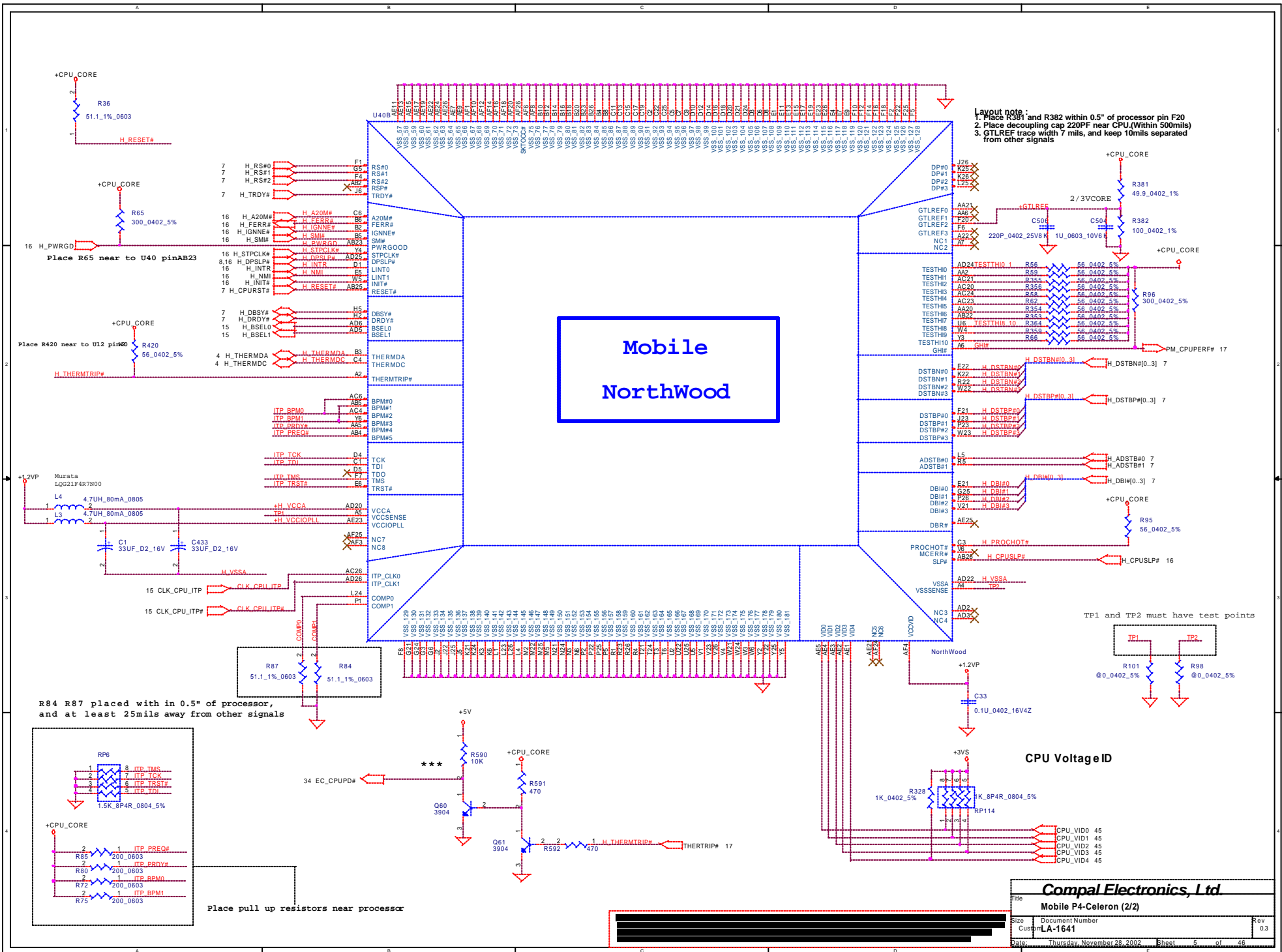
Sapporo Z to ZJ BOM modify list :

1. Remove R594
2. Add R112

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Note List			
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Mobile NorthWood





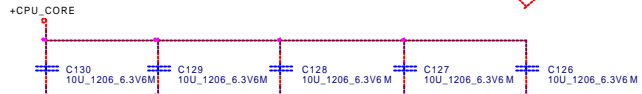
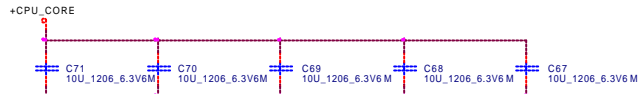
Layout note :

Place close to CPU, Use 2-3 vias per PAD.
 Place .22uF caps underneath balls on solder side.
 Place 10uF caps on the peripheral near balls.
 Use 2-3 vias per PAD.

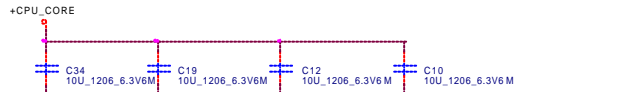
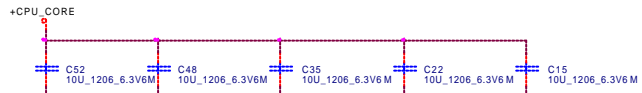
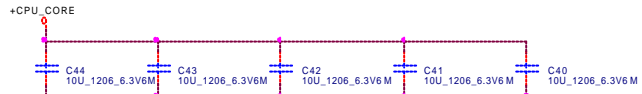
Layout note :

Place close to CPU power and ground pin as possible (<1inch)

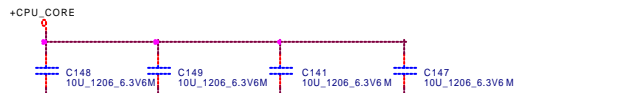
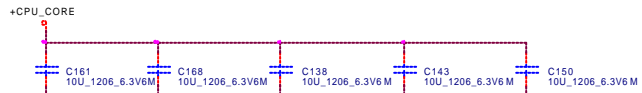
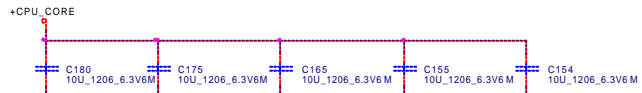
Please place these cap in the socket cavity area



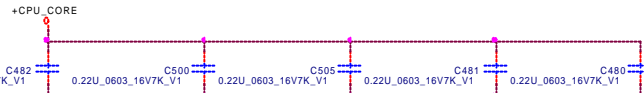
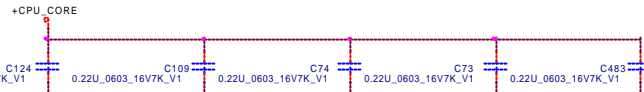
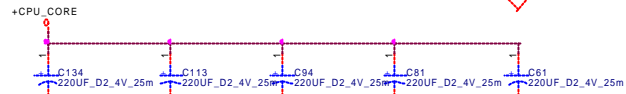
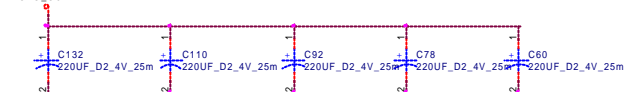
Please place these cap on the socket north side

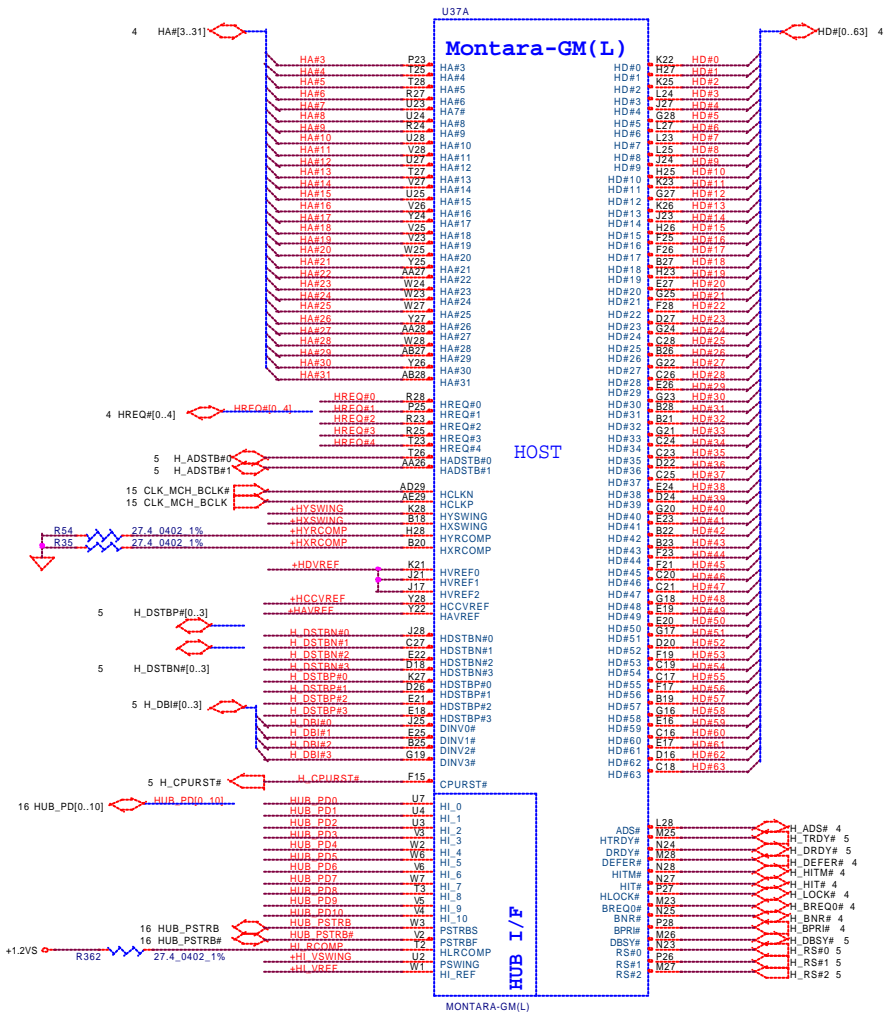


Please place these cap on the socket south side



Used ESR 25m ohm cap total ESR=2.5m ohm

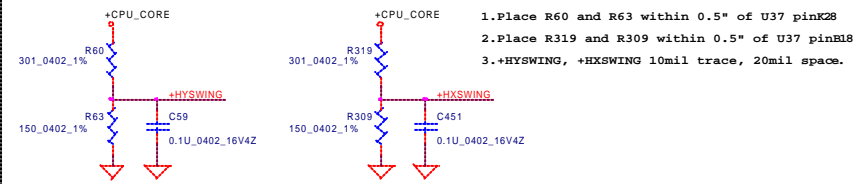




Layout Note:

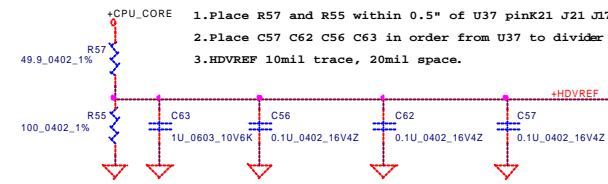
1. Place R35 and R54 within 0.5" of U37 pinH28 B20
2. Both HYRCOMP and HXRCOMP trace width are 18mil and 25mils away from other signals

HXSWING and HYSWING Ref. Voltage



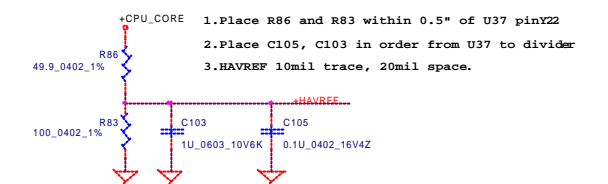
1. Place R60 and R63 within 0.5" of U37 pinK28
2. Place R319 and R309 within 0.5" of U37 pinB18
3. +HYSWING, +HXSWING 10mil trace, 20mil space.

Host data Ref. Voltage



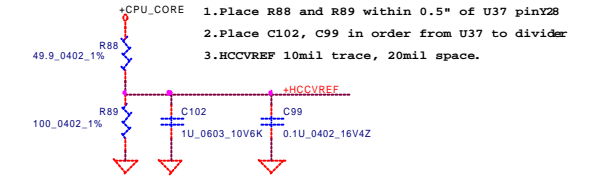
1. Place R57 and R55 within 0.5" of U37 pinK21 J21 J17
2. Place C57 C62 C56 C63 in order from U37 to divider
3. HDVREF 10mil trace, 20mil space.

Host address Ref. Voltage



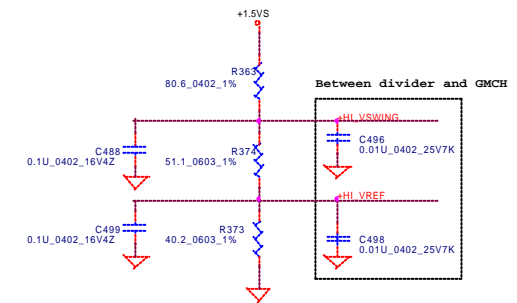
1. Place R86 and R83 within 0.5" of U37 pinY22
2. Place C105, C103 in order from U37 to divider
3. HAVREF 10mil trace, 20mil space.

Host common clock Ref. Voltage



1. Place R88 and R89 within 0.5" of U37 pinY28
2. Place C102, C99 in order from U37 to divider
3. HCCVREF 10mil trace, 20mil space.

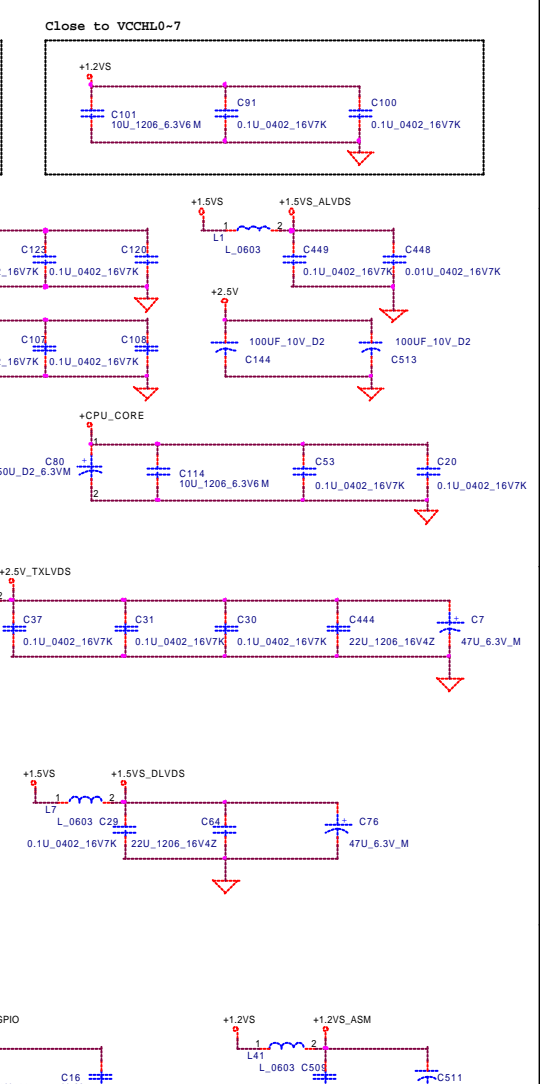
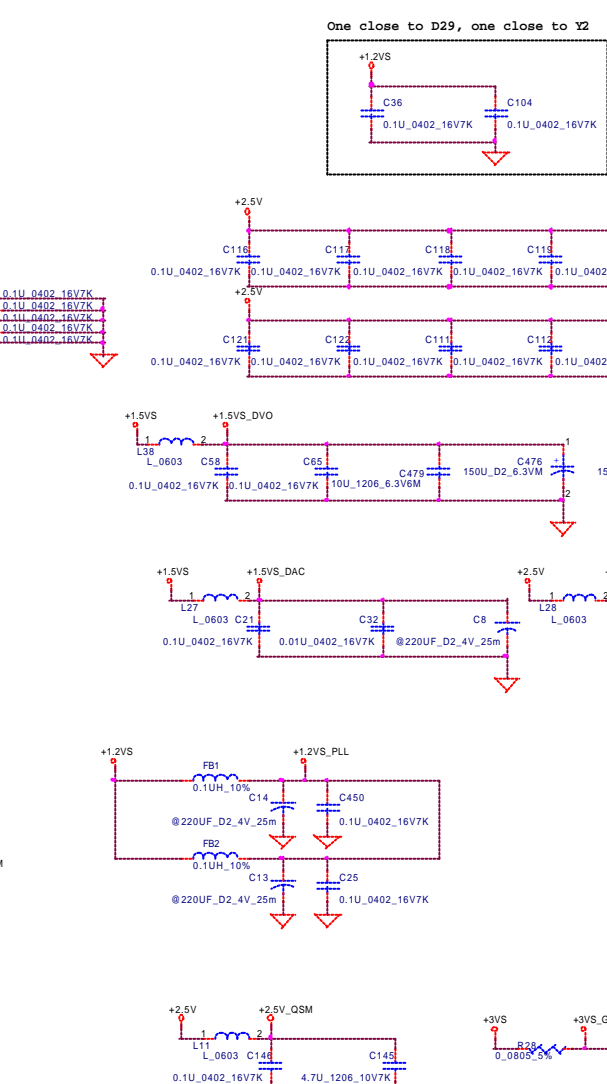
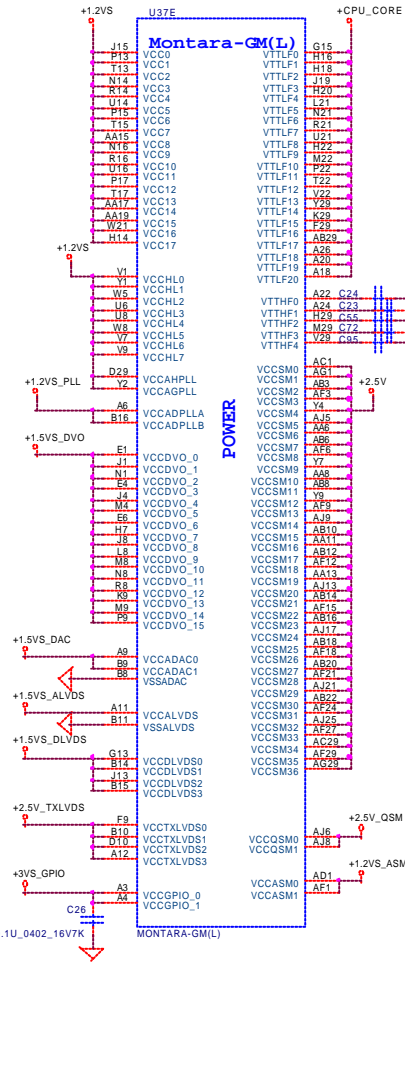
HUB I/F REF VOLTAGE



Place this schematic close to GMCH

Montara-GM(L)

U37D	C1	VSS0	VSS91	R17
	G1	VSS1	VSS92	U17
	L1	VSS2	VSS93	AB17
	AA1	VSS3	VSS94	F18
	AE1	VSS4	VSS95	J18
	R2	VSS5	VSS96	AA19
	AG3	VSS6	VSS97	AG18
	AJ3	VSS7	VSS98	A19
	G4	VSS8	VSS99	D19
	D4	VSS9	VSS100	H19
	K4	VSS10	VSS101	AB19
	V4	VSS11	VSS102	N4
	VSS12	VSS103	VSS104	AE19
	W4	VSS13	VSS105	J20
	AA4	VSS14	VSS106	AA20
	AC4	VSS15	VSS107	AC20
	AE4	VSS16	VSS108	A21
	B5	VSS17	VSS109	B21
	V5	VSS18	VSS110	H21
	Y5	VSS19	VSS111	H21
	Y6	VSS20	VSS112	H21
	AG5	VSS21	VSS113	T21
	C7	VSS22	VSS114	T21
	E7	VSS23	VSS115	Y21
	G7	VSS24	VSS116	AA21
	VSS25	VSS117	VSS118	AB21
	MT	VSS26	VSS119	B22
	R7	VSS27	VSS120	B22
	VSS28	VSS121	VSS122	F22
	AE7	VSS29	VSS123	F22
	AJ7	VSS30	VSS124	N22
	H8	VSS31	VSS125	U22
	K8	VSS32	VSS126	W22
	P8	VSS33	VSS127	AE22
	T8	VSS34	VSS128	AE22
	Y8	VSS35	VSS129	B23
	AC8	VSS36	VSS130	AA23
	E9	VSS37	VSS131	AA23
	L9	VSS38	VSS132	A123
	N9	VSS40	VSS133	F24
	R9	VSS41	VSS134	M4
	U9	VSS42	VSS135	K24
	W9	VSS43	VSS136	M24
	AB9	VSS44	VSS137	P24
	AG9	VSS45	VSS138	P24
	AG9	VSS46	VSS139	V24
	C10	VSS47	VSS140	AA24
	AA10	VSS48	VSS141	AC24
	AE10	VSS49	VSS142	A25
	D11	VSS50	VSS143	D25
	F11	VSS51	VSS144	R25
	H11	VSS52	VSS145	AE25
	AB11	VSS53	VSS146	G26
	VSS54	VSS147	VSS148	J26
	AJ11	VSS55	VSS149	N26
	H12	VSS56	VSS150	R26
	AG12	VSS58	VSS151	U26
	A13	VSS61	VSS152	U26
	D13	VSS62	VSS153	AB26
	F13	VSS63	VSS154	A27
	H13	VSS64	VSS155	F27
	R13	VSS65	VSS156	AC27
	U13	VSS66	VSS157	AG27
	AB13	VSS67	VSS158	A27
	AE13	VSS68	VSS159	AC28
	J14	VSS69	VSS160	AE28
	VSS70	VSS161	VSS162	C29
	AA14	VSS71	VSS163	G29
	AC14	VSS72	VSS164	J29
	D15	VSS73	VSS165	J29
	H15	VSS74	VSS166	N29
	N15	VSS75	VSS167	U29
	R15	VSS76	VSS168	W29
	U15	VSS77	VSS169	AA29
	AB15	VSS78	VSS170	A110
	AG15	VSS79	VSS171	A110
	F16	VSS80	VSS172	A110
	J16	VSS81	VSS173	A120
	P16	VSS82	VSS174	C22
	T16	VSS83	VSS176	D28
	AA16	VSS84	VSS177	E28
	AE16	VSS85	VSS178	L6
	VSS86	VSS179	VSS180	A126
	A17	VSS87	VSS181	
	H17	VSS88		
	N17	VSS89		
		VSS90		



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U37C

Montara-GM(L)

MEMORY

DDR_SMA0 AC18 SMA0
 DDR_SMA1 AD14 SMA1
 DDR_SMA2 AD17 SMA2
 DDR_SMA3 AD11 SMA3
 DDR_SMA4 AD11 SMA4
 DDR_SMA5 AD7 SMA5
 DDR_SMA6 AD7 SMA6
 DDR_SMA7 AD7 SMA7
 DDR_SMA8 AC5 SMA8
 DDR_SMA9 AC5 SMA9
 DDR_SMA10 AC19 SMA10
 DDR_SMA11 AD5 SMA11
 DDR_SMA12 AB5 SMA12

DDR_SDO0 AG2 SDO00
 DDR_SDO1 AH5 SDO01
 DDR_SDO2 AH8 SDO02
 DDR_SDO3 AE12 SDO03
 DDR_SDO4 AH17 SDO04
 DDR_SDO5 AE21 SDO05
 DDR_SDO6 AH24 SDO06
 DDR_SDO7 AH27 SDO07
 AH15 SDO08

DDR_SWE# AD25 SWE#
 DDR_SRA5# AC21 SRA5#
 DDR_SCA5# AC24 SCA5#

11 DDR_CLK0 DBRCLK0 AB2 SCMDCLK0
 11 DDR_CLK0# DDCCLK0# AA2 SCMDCLK0#
 11 DDR_CLK1# DDCCLK1# AC26 SCMDCLK1#
 11 DDR_CLK1# DDCCLK1# AB23 SCMDCLK1#
 11 DDR_CLK2# DDCCLK2# AC3 SCMDCLK2#
 11 DDR_CLK3# DDCCLK3# AC2 SCMDCLK3#
 11 DDR_CLK4# DDCCLK4# AB23 SCMDCLK4#
 11 DDR_CLK4# DDCCLK4# AB24 SCMDCLK4#
 11 DDR_CLK4# DDCCLK4# AB24 SCMDCLK5#

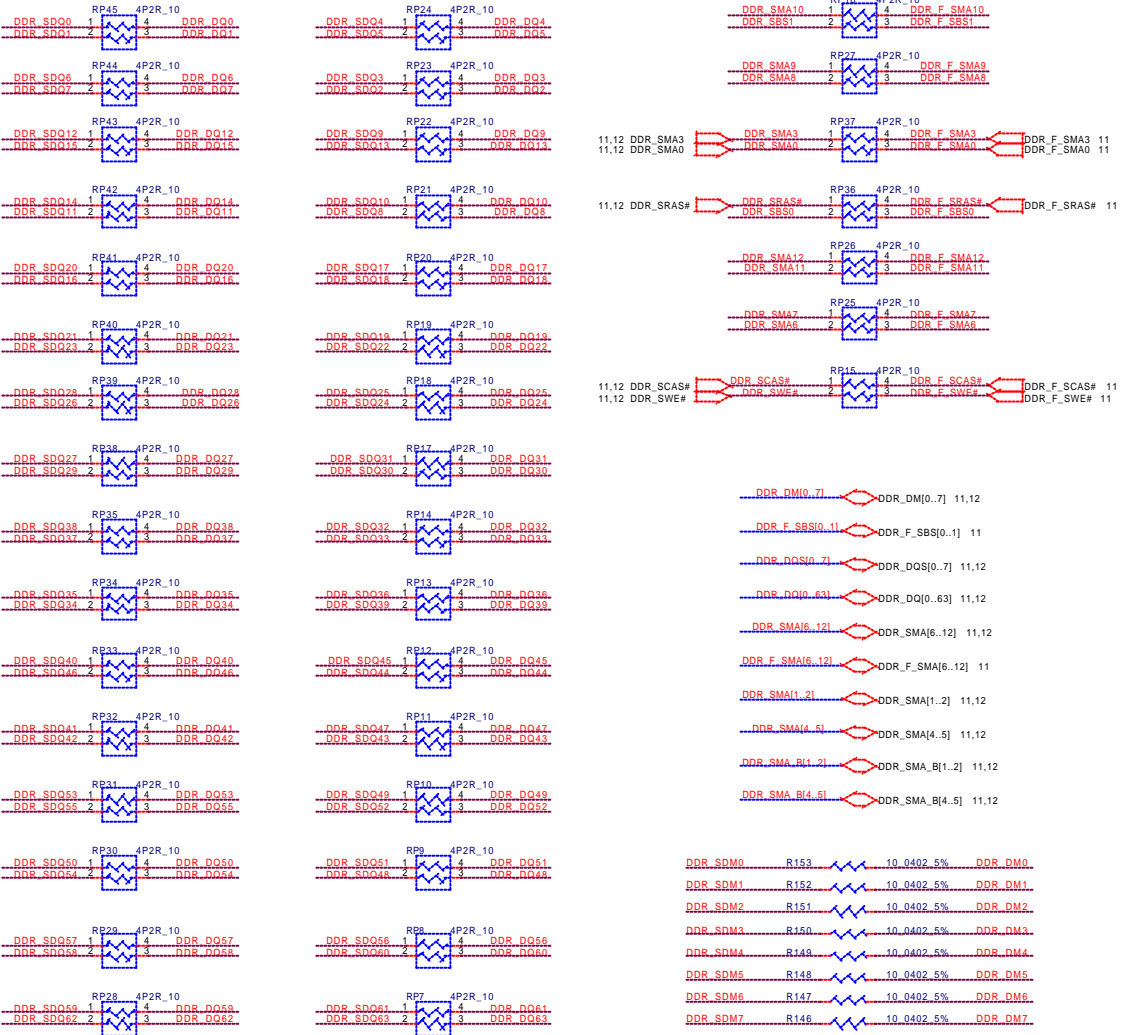
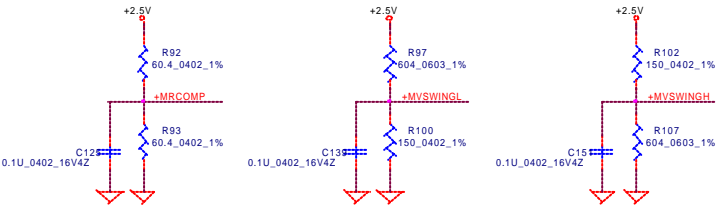
11,12 DDR_CKE0 AC7 SCKE0
 11,12 DDR_CKE1 AB7 SCKE1
 11,12 DDR_CKE2 AC9 SCKE2
 11,12 DDR_CKE3 AC10 SCKE3
 11,12 DDR_SC5#0 AD23 SC5#0
 11,12 DDR_SC5#1 AD26 SC5#1
 11,12 DDR_SC5#2 AC22 SC5#2
 11,12 DDR_SC5#3 AC25 SC5#3

11,12 DDR_SBS0 AD22 SBA0#
 11,12 DDR_SBS1 AB20 SBA1#

DDR_SDM0 AE5 SDM0
 DDR_SDM1 AE6 SDM1
 DDR_SDM2 AE8 SDM2
 DDR_SDM3 AH12 SDM3
 DDR_SDM4 AD19 SDM4
 DDR_SDM5 AD21 SDM5
 DDR_SDM6 AB24 SDM6
 DDR_SDM7 AH28 SDM7
 AH15 SDM8

Routed with Vias next to ball.
 ACVENOUT# AC15 SRCVENOUT#
 ACVENIN# AC16 SRCVENIN#
 +MRCOMP AB1 SMRCOMP
 +MVSINGL A122 SMVSWINGL
 +MVSINGH A119 SMVSWINGH

DDR REF & SWING VOLTAGE



DDR_SDO0	R171	10.0402.5%	DDR_DQ00
DDR_SDO1	R170	10.0402.5%	DDR_DQ01
DDR_SDO2	R169	10.0402.5%	DDR_DQ02
DDR_SDO3	R168	10.0402.5%	DDR_DQ03
DDR_SDO4	R167	10.0402.5%	DDR_DQ04
DDR_SDO5	R166	10.0402.5%	DDR_DQ05
DDR_SDO6	R165	10.0402.5%	DDR_DQ06
DDR_SDO7	R164	10.0402.5%	DDR_DQ07

11,12 DDR_SMA3# DDR_SMA3 1 4 DDR_F_SMA3 DDR_F_SMA3 11
11,12 DDR_SMA0# DDR_SMA0 2 3 DDR_F_SMA0 DDR_F_SMA0 11

11,12 DDR_SRA5# DDR_SRA5# 1 4 DDR_F_SRA5# DDR_F_SRA5# 11
11,12 DDR_SBS0# DDR_SBS0# 2 3 DDR_F_SBS0# DDR_F_SBS0# 11

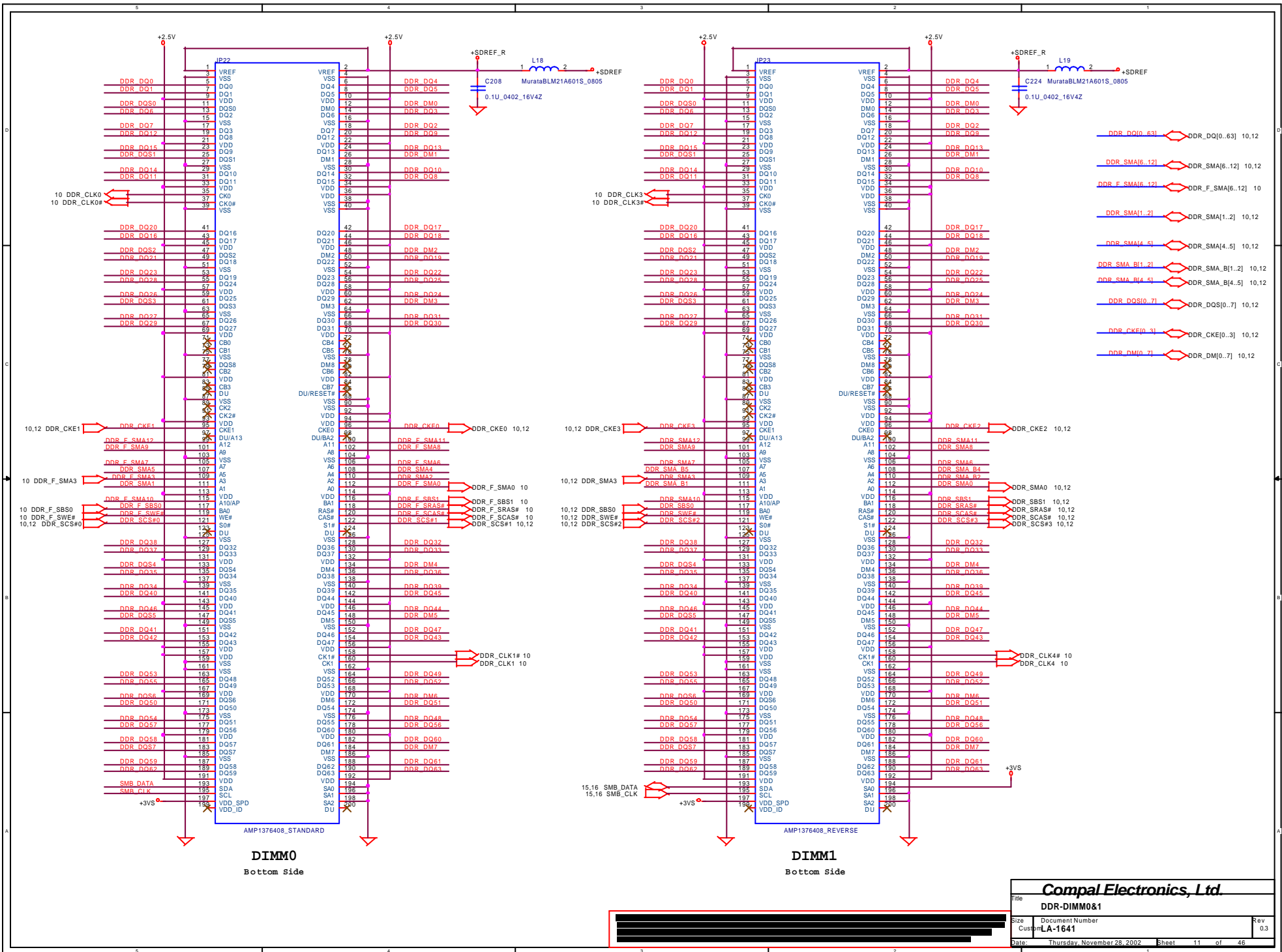
11,12 DDR_SCA5# DDR_SCA5# 1 4 DDR_F_SCA5# DDR_F_SCA5# 11
11,12 DDR_SWE# DDR_SWE# 2 3 DDR_F_SWE# DDR_F_SWE# 11

DDR_DM0[.7] DDR_DM[0..7] 11,12
DDR_F_SBS0[.1] DDR_F_SBS[0..1] 11
DDR_DQS0[.7] DDR_DQS[0..7] 11,12
DDR_DQ[0.63] DDR_DQ[0..63] 11,12
DDR_SMA[6..12] DDR_SMA[6..12] 11,12
DDR_F_SMA[6..12] DDR_F_SMA[6..12] 11
DDR_SMA[1..2] DDR_SMA[1..2] 11,12
DDR_SMA[4..5] DDR_SMA[4..5] 11,12
DDR_SMA_B[1..2] DDR_SMA_B[1..2] 11,12
DDR_SMA_B[4..5] DDR_SMA_B[4..5] 11,12

DDR_SDM0	R153	10.0402.5%	DDR_DM0
DDR_SDM1	R152	10.0402.5%	DDR_DM1
DDR_SDM2	R151	10.0402.5%	DDR_DM2
DDR_SDM3	R150	10.0402.5%	DDR_DM3
DDR_SDM4	R148	10.0402.5%	DDR_DM4
DDR_SDM5	R148	10.0402.5%	DDR_DM5
DDR_SDM6	R147	10.0402.5%	DDR_DM6
DDR_SDM7	R146	10.0402.5%	DDR_DM7

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 Montara-GML (DDR)

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DIMM0
Bottom Side

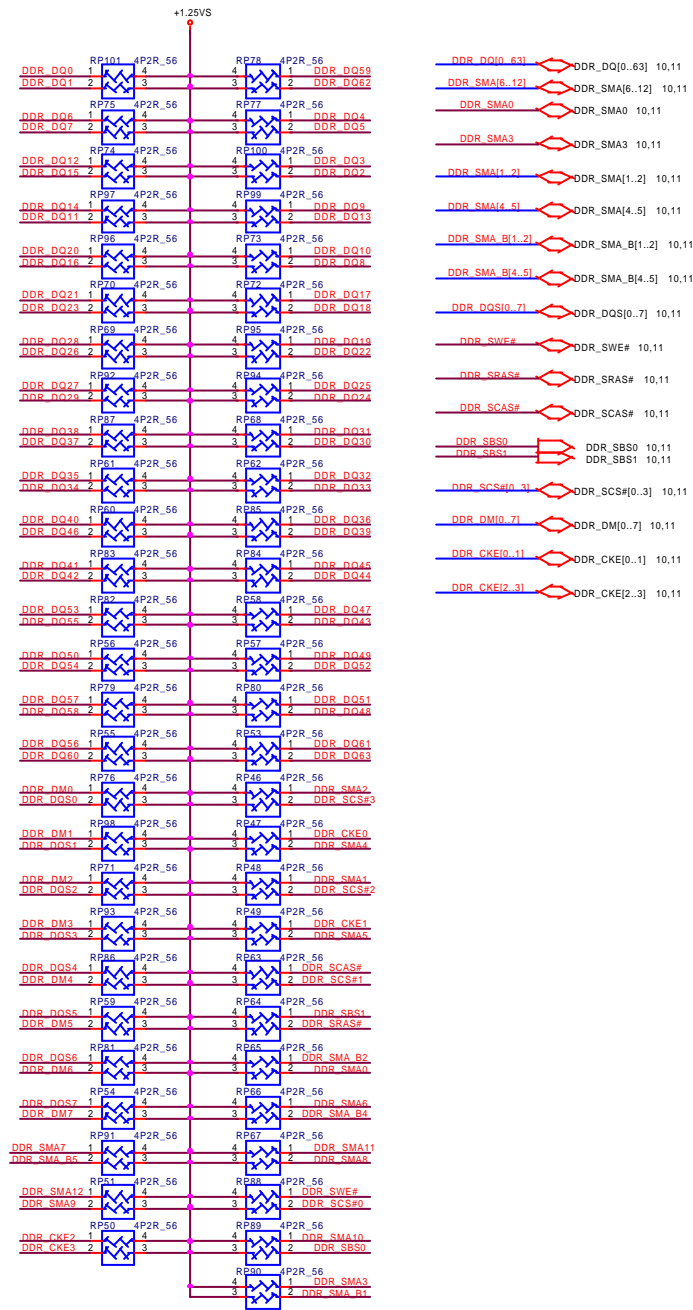
DIMM1
Bottom Side

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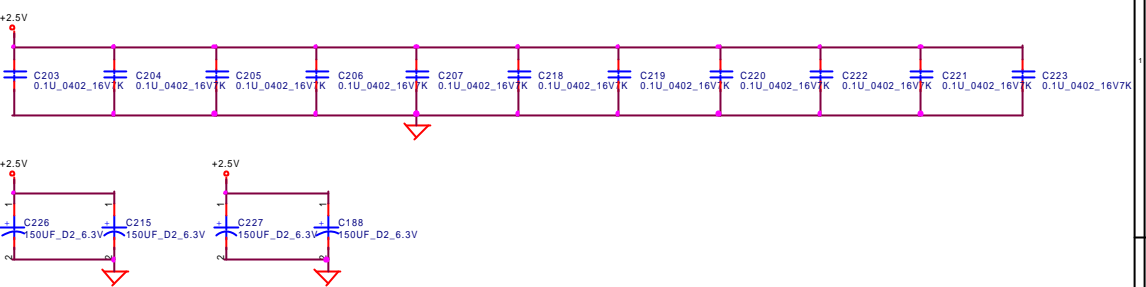
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Size: Document Number
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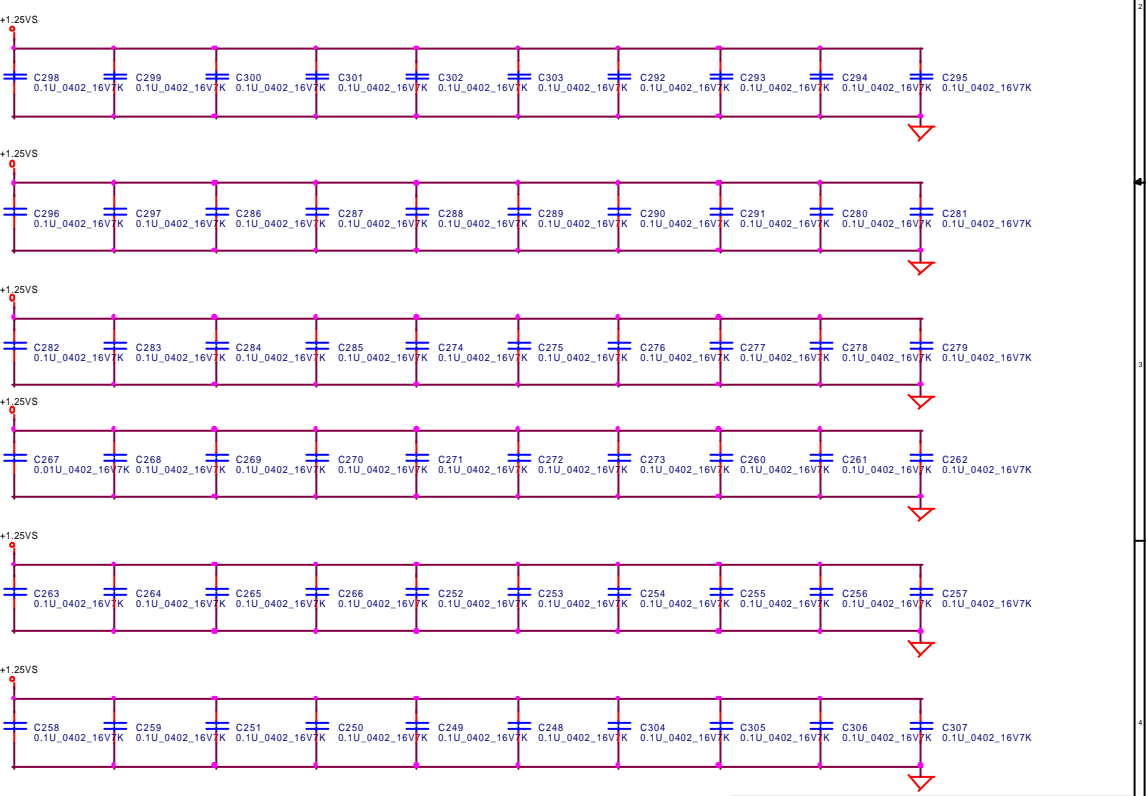
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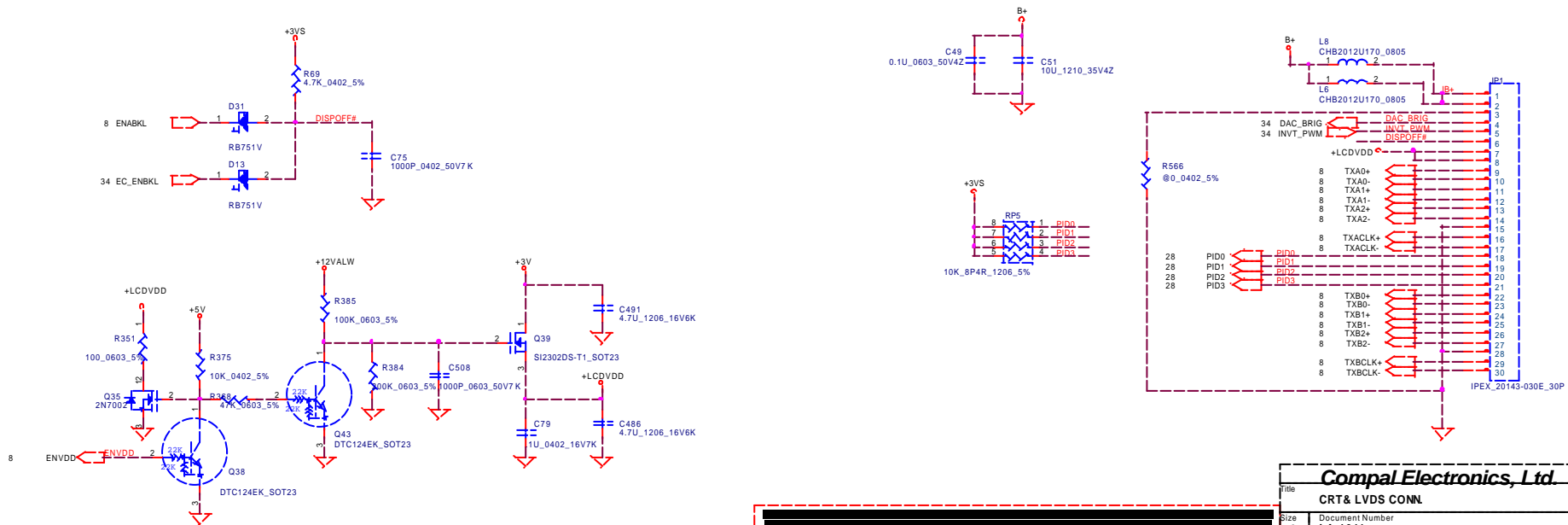
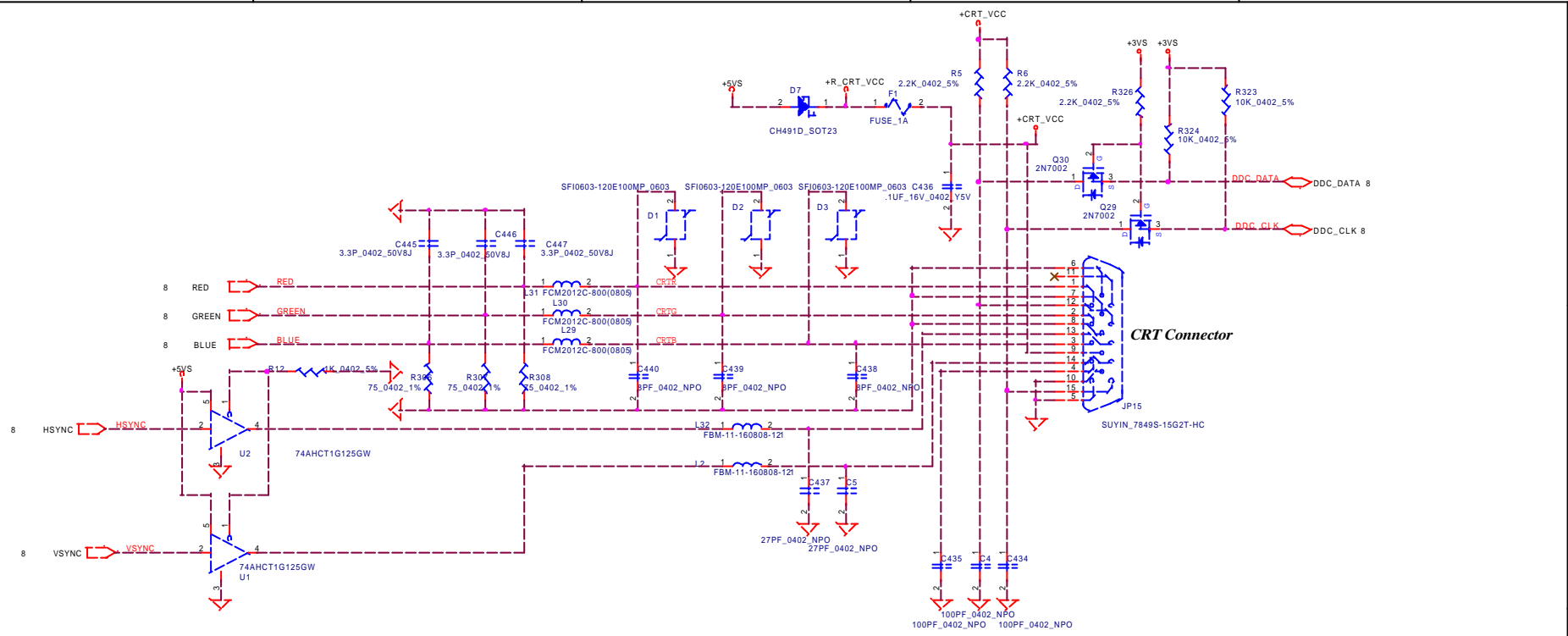


Layout note :
Distribute as close as possible to DDR-SODIMM.



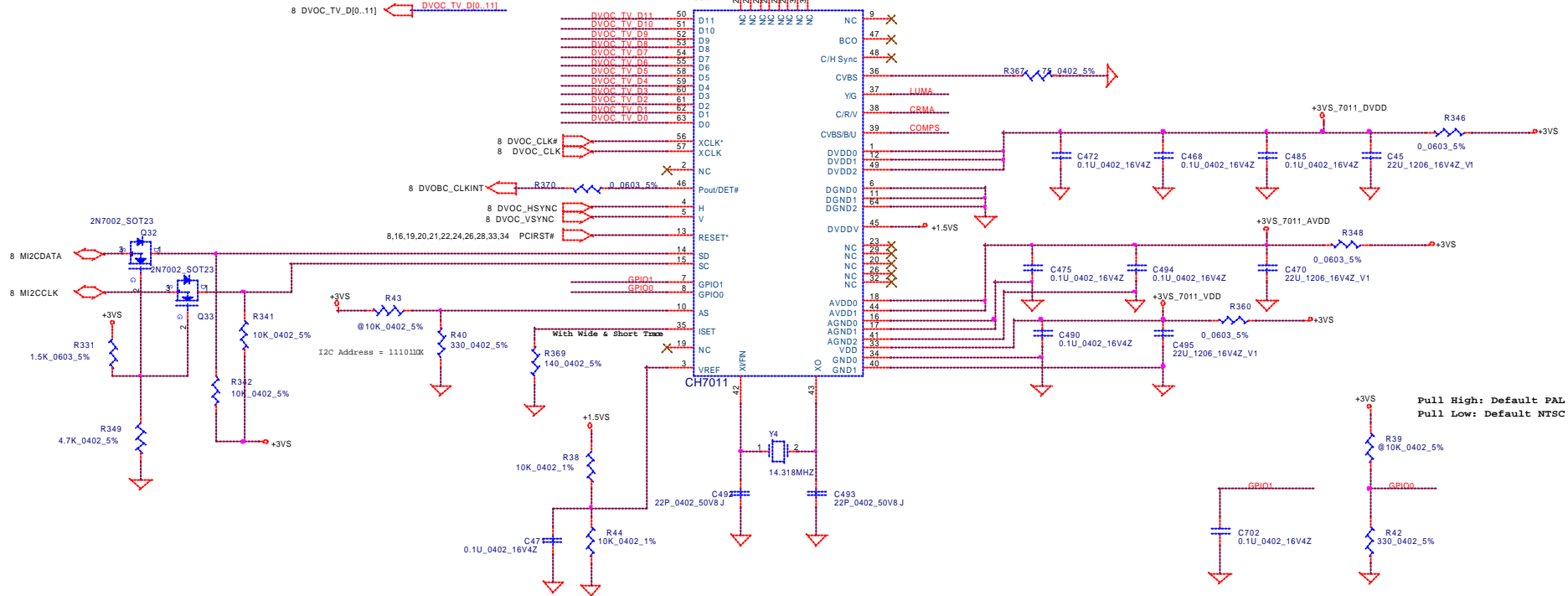
Layout note :
Place one cap close to every 2 pull up resistors termination to +1.25V



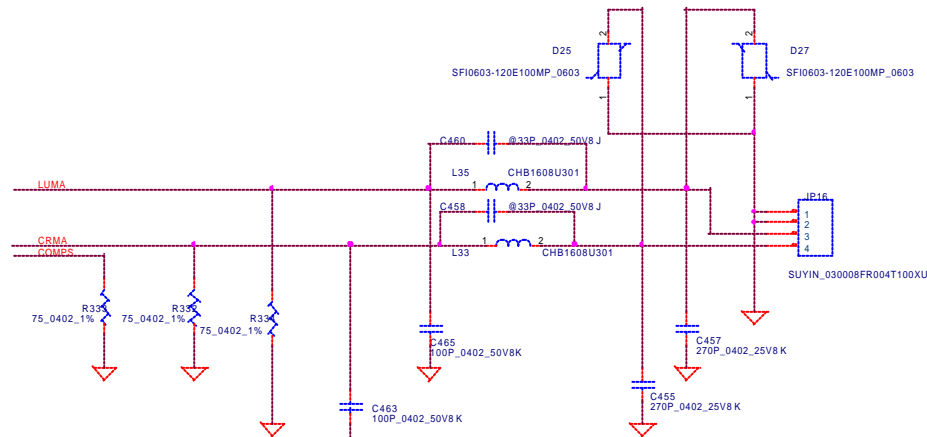


Compal Electronics, Ltd CRT & LVDS CONN.		
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CH-7011



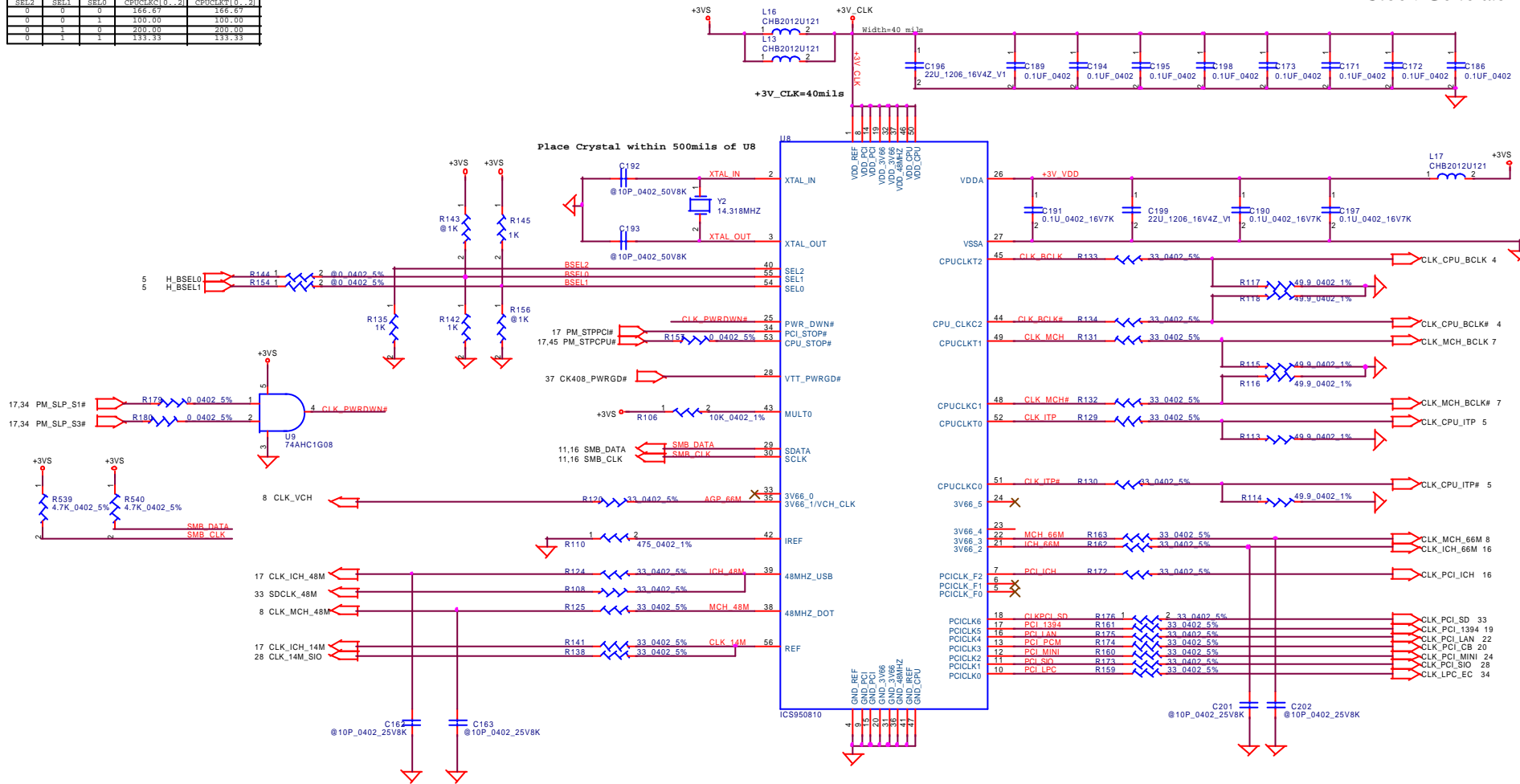
TV-OUT CONN.

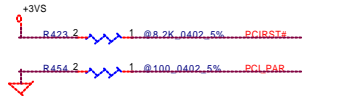
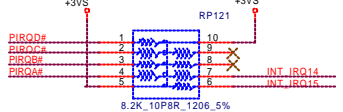
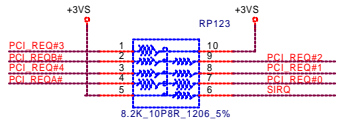
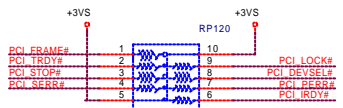


Compal Electronics, Ltd.			
CH-7011& TV-CONN			
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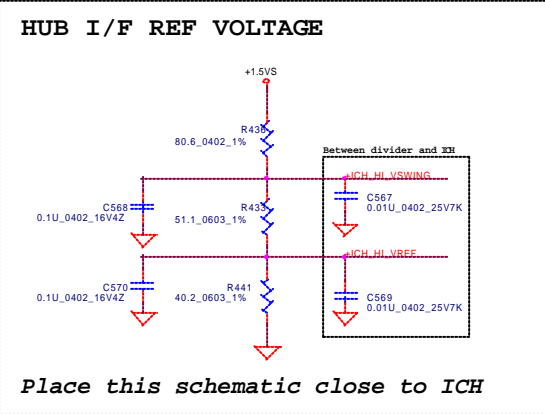
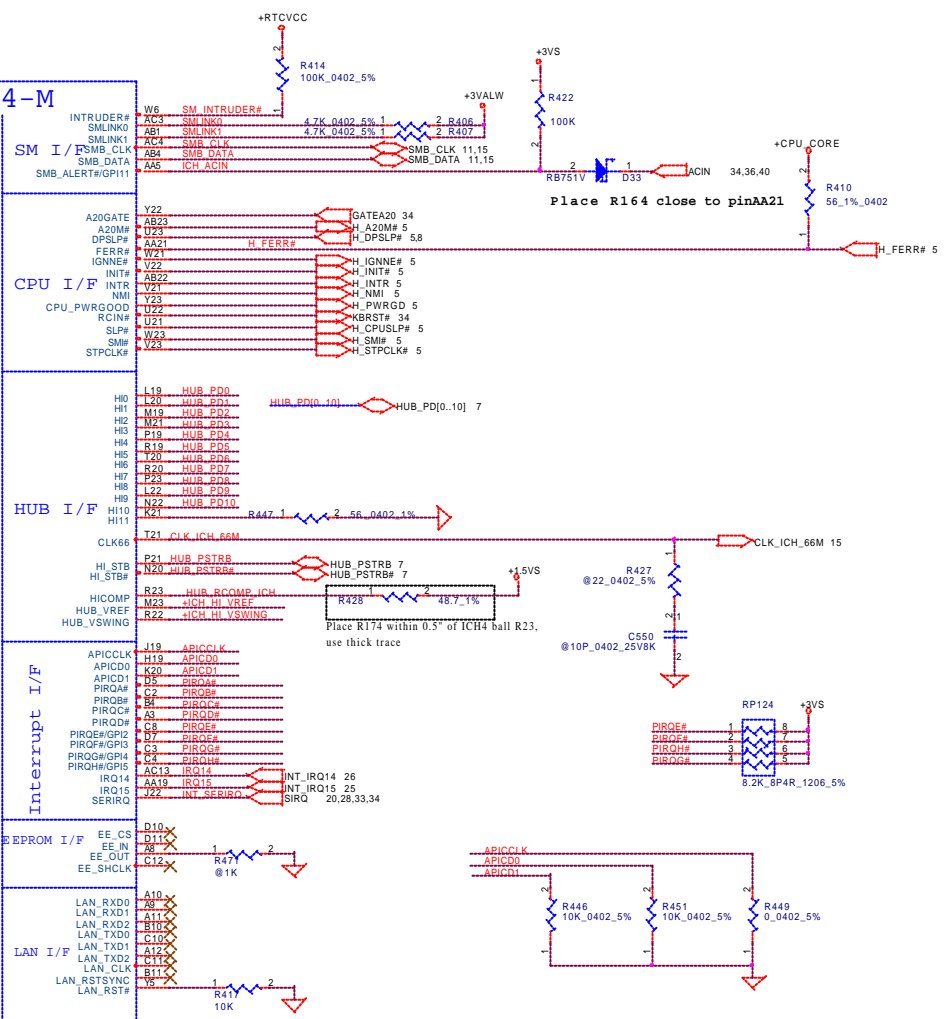
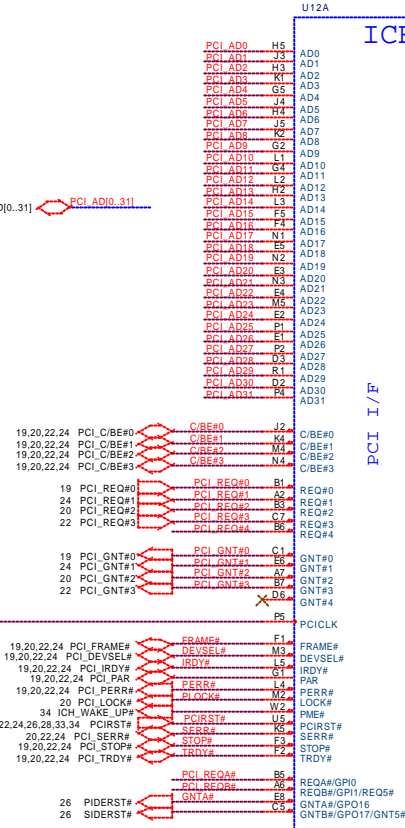
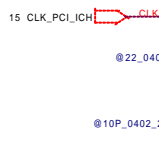
Clock Generator

SEL2	SEL1	SEL0	CPUCLK0 (0..2)	CPUCLK1 (0..2)
0	0	0	100.00	100.00
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

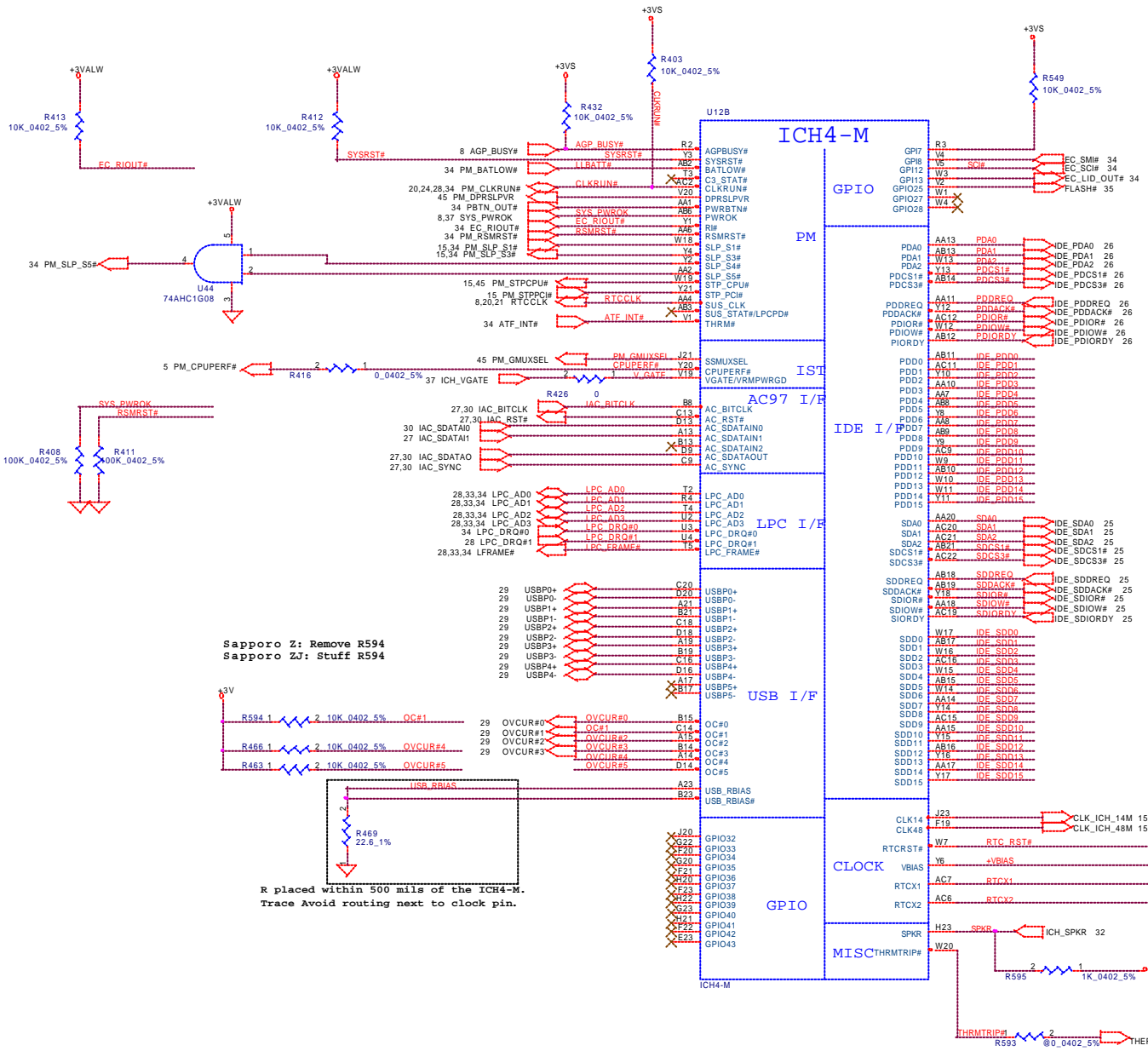




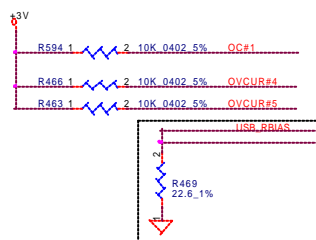
Note:
In ICH4, PCI_GNT[0..4] don't need external pullup



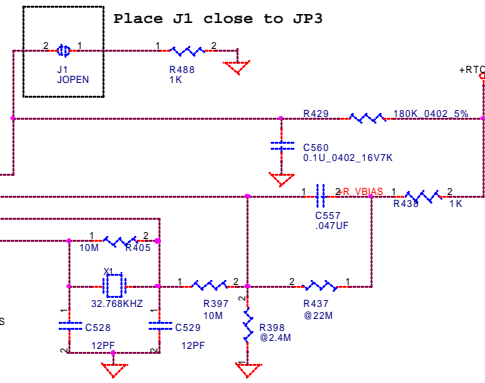
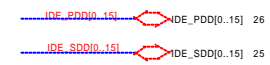
	Topology 1: Mount R458 RP122 R533 Unmount R474 RP125	Topology 2: Mount R458 R474 RP125 Unmount RP122 R533
1394	Trace: PIRQA#_1394 Use IRQA	Trace: PIRQA#_1394 Use IRQA
CardBus	Trace: PIRQA#/E# PIROB#/F#/D# Use IRQA IRQB	Trace: PIRQA#/E# PIROB#/F#/D# Use IRQE IRQF
LAN	Trace: PIRQ_LAN#/B#/D# Use IRQB	Trace: PIRQB#/F#/D# Use IRQD
MINIPCI	Trace: PIRQC#/G# PIROD#/H# Use IRQC IRQD	Trace: PIRQC#/G# PIROD#/H# Use IRQG IRQH

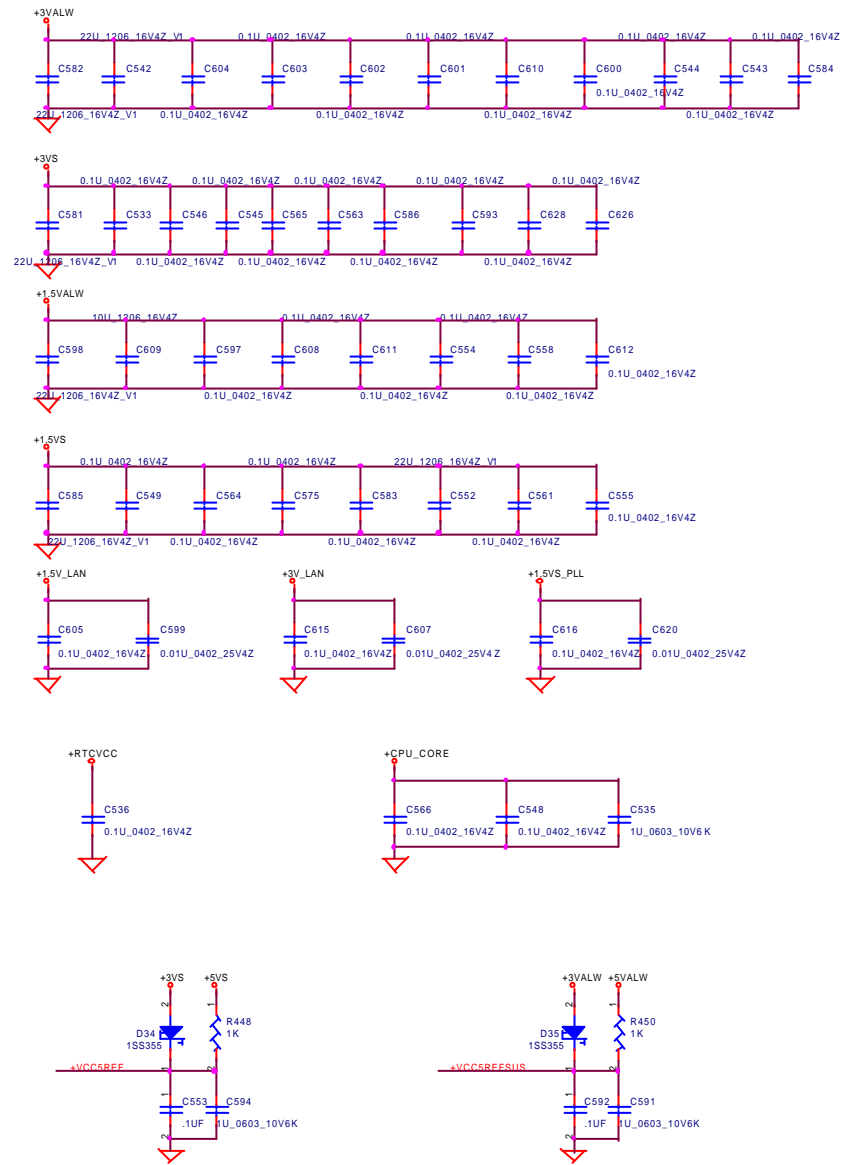
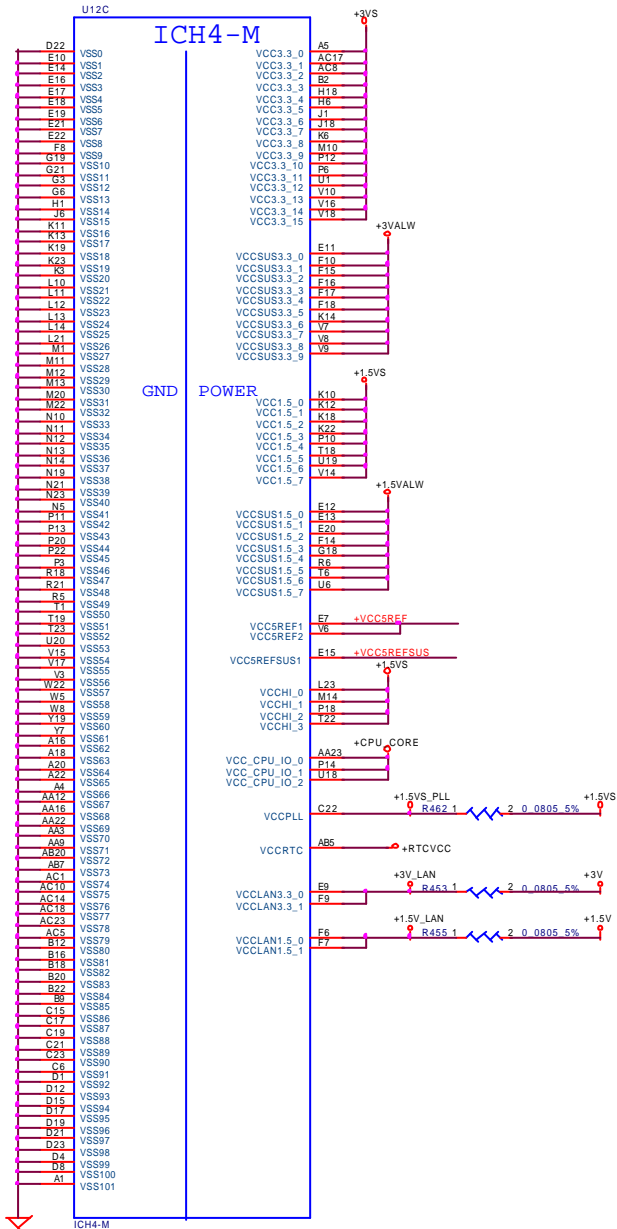


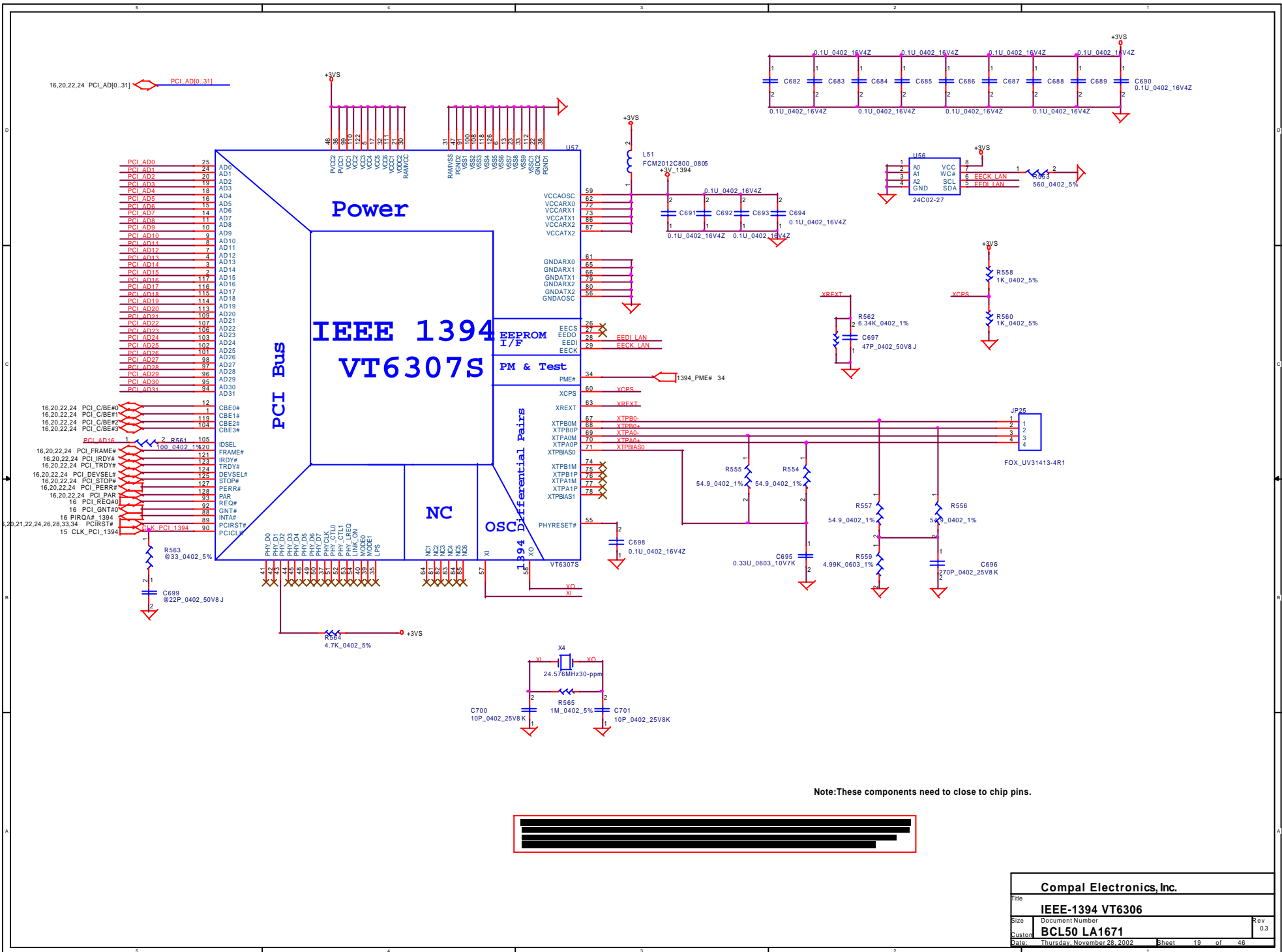
Sapporo Z: Remove R594
Sapporo ZJ: Stuff R594



R placed within 500 mils of the ICH4-M.
Trace Avoid routing next to clock pin.

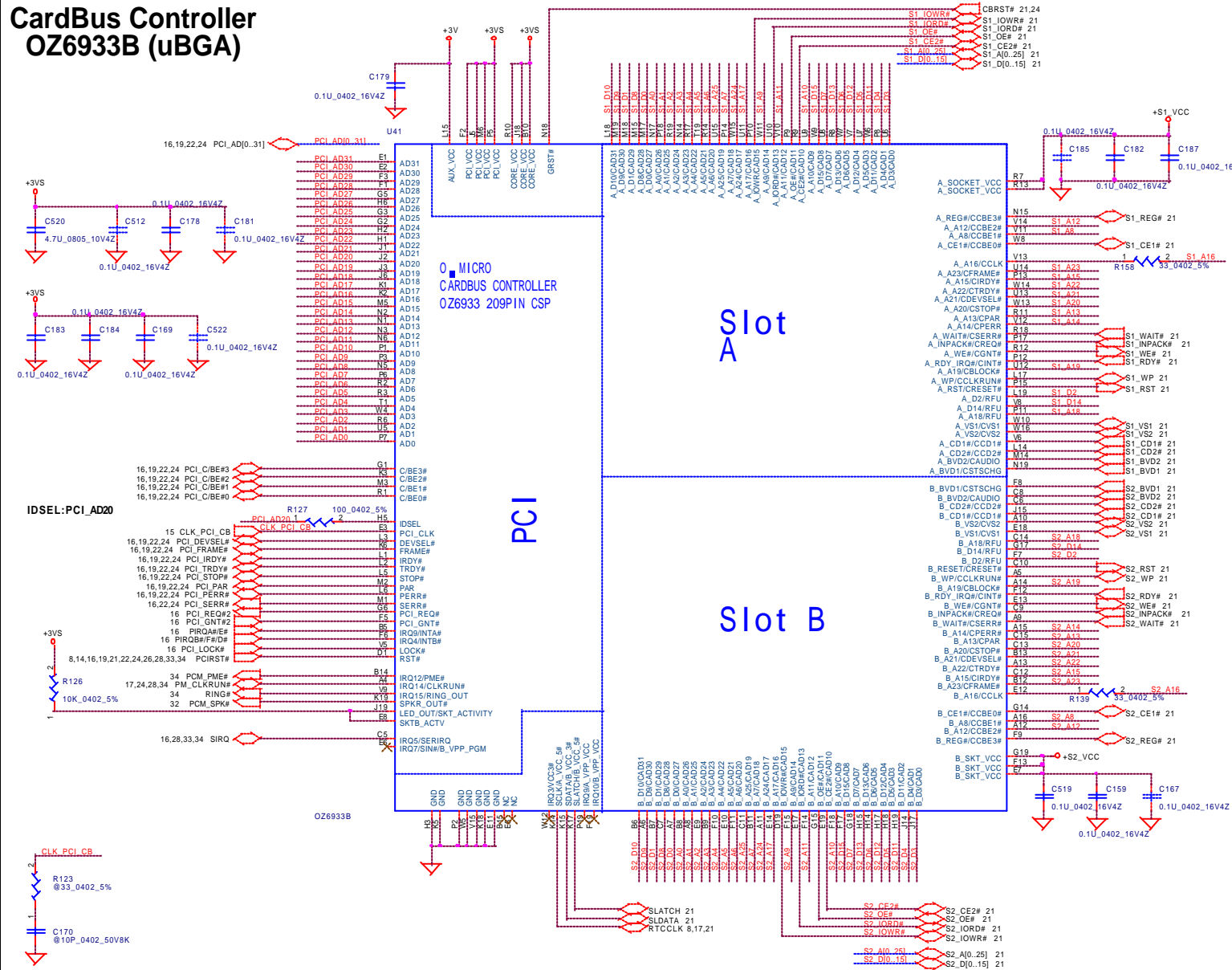






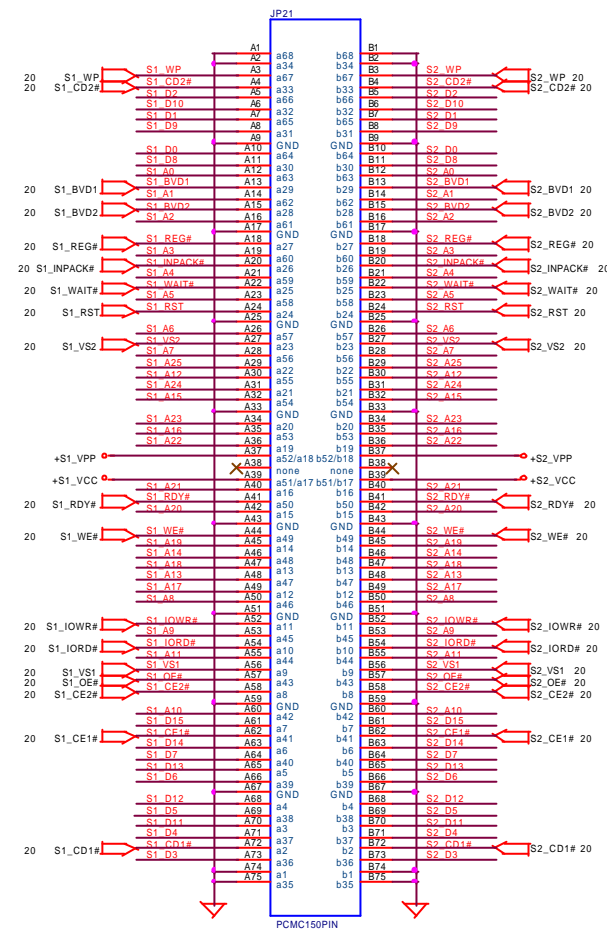
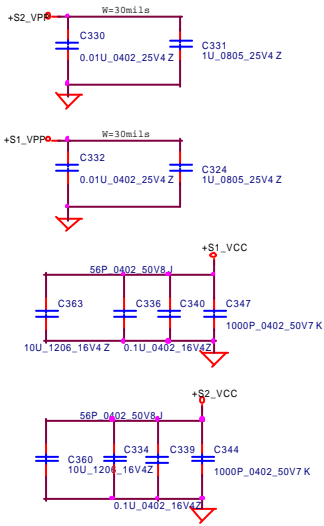
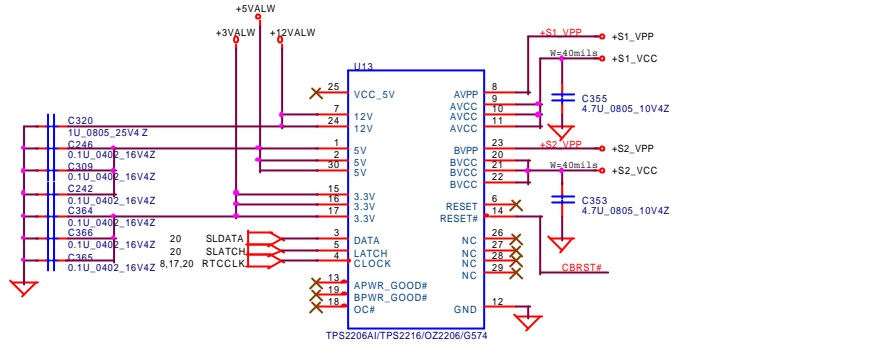
Compal Electronics, Inc.		
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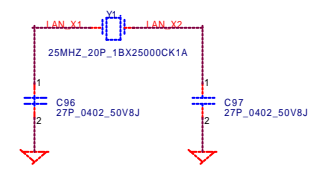
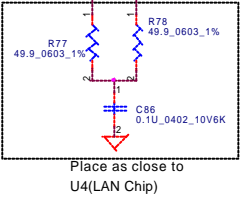
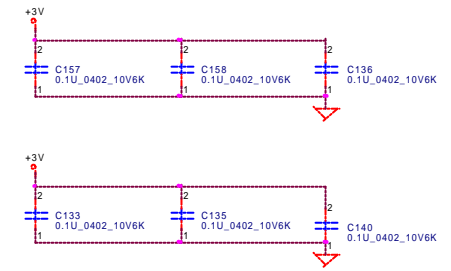
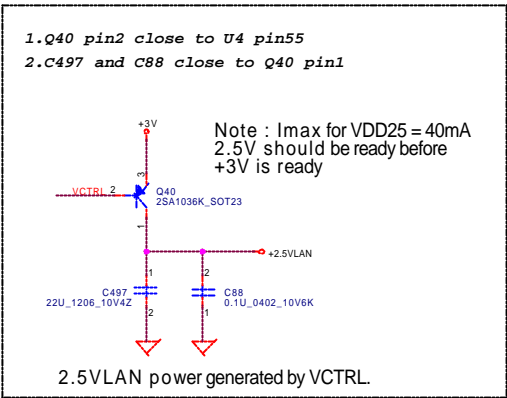
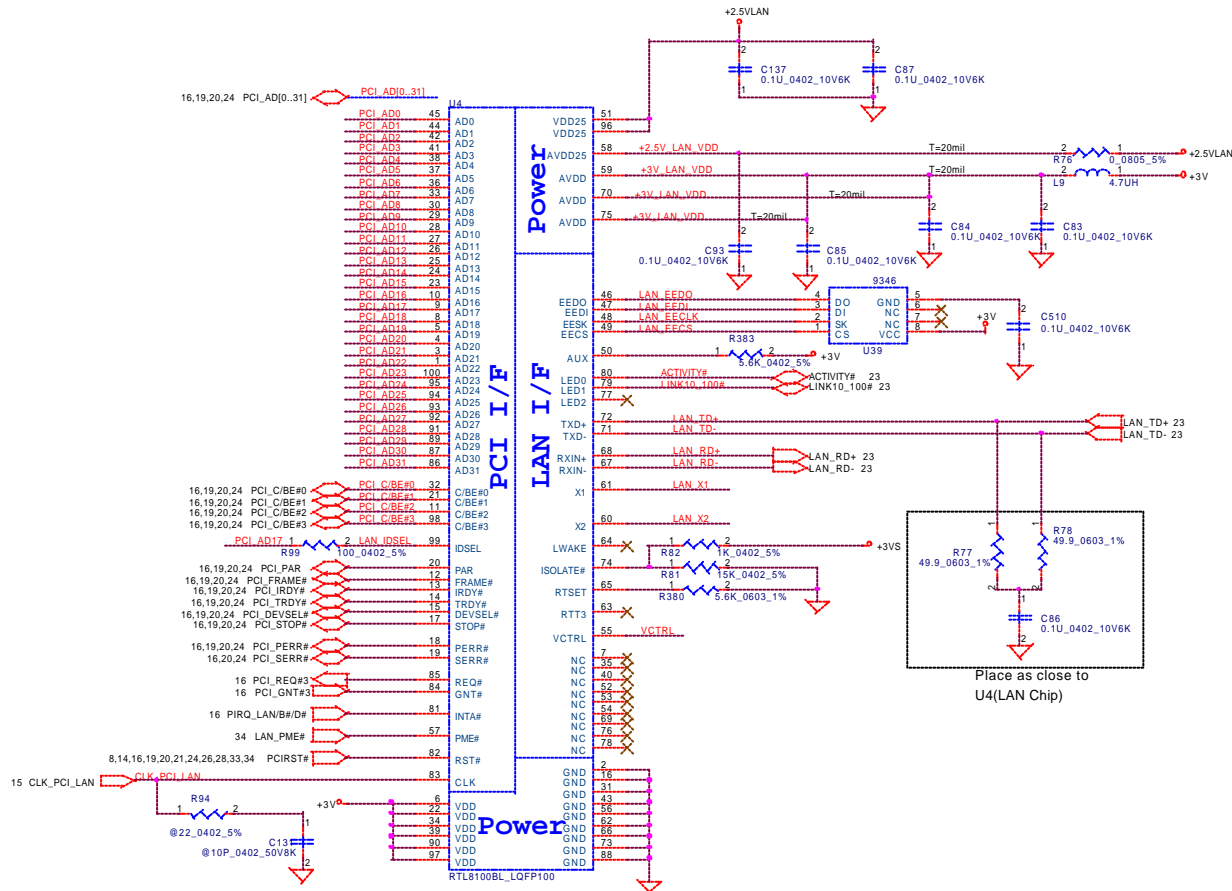
CardBus Controller OZ6933B (uBGA)



PCMCIA POWER CTRL.

CARDBUS SOCKET



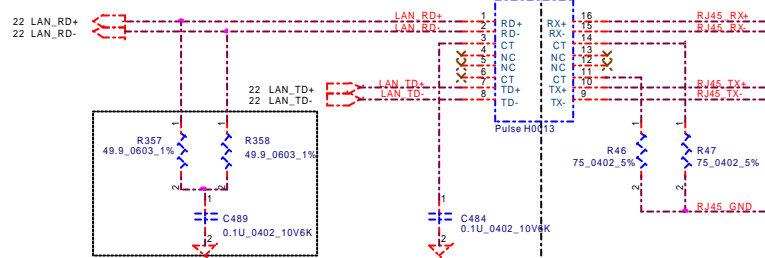


Compal Electronics, Ltd.			
LAN-Realtek RTL8100BL			
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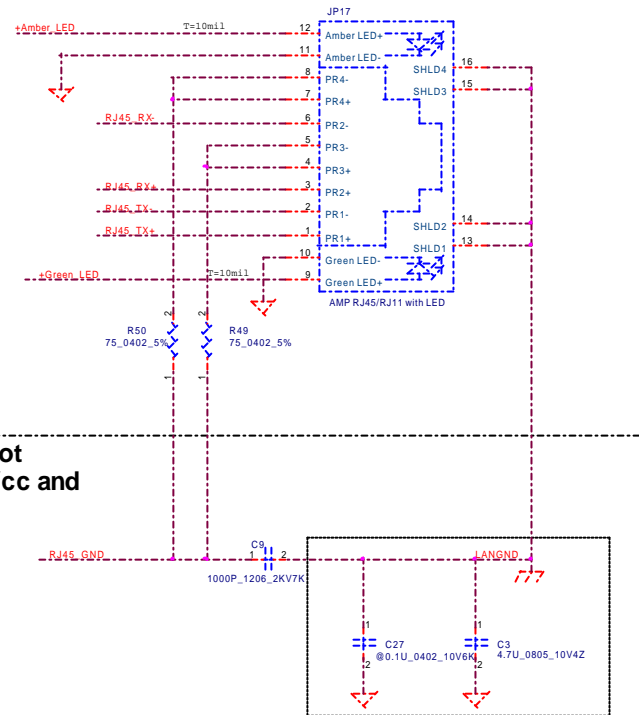
Keep Out 40mil

Layout Note
H0013 pls close to conn.

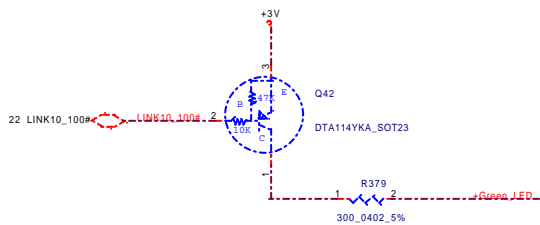
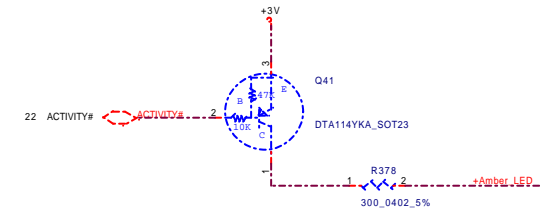


Place as close to Magnetic (U3)

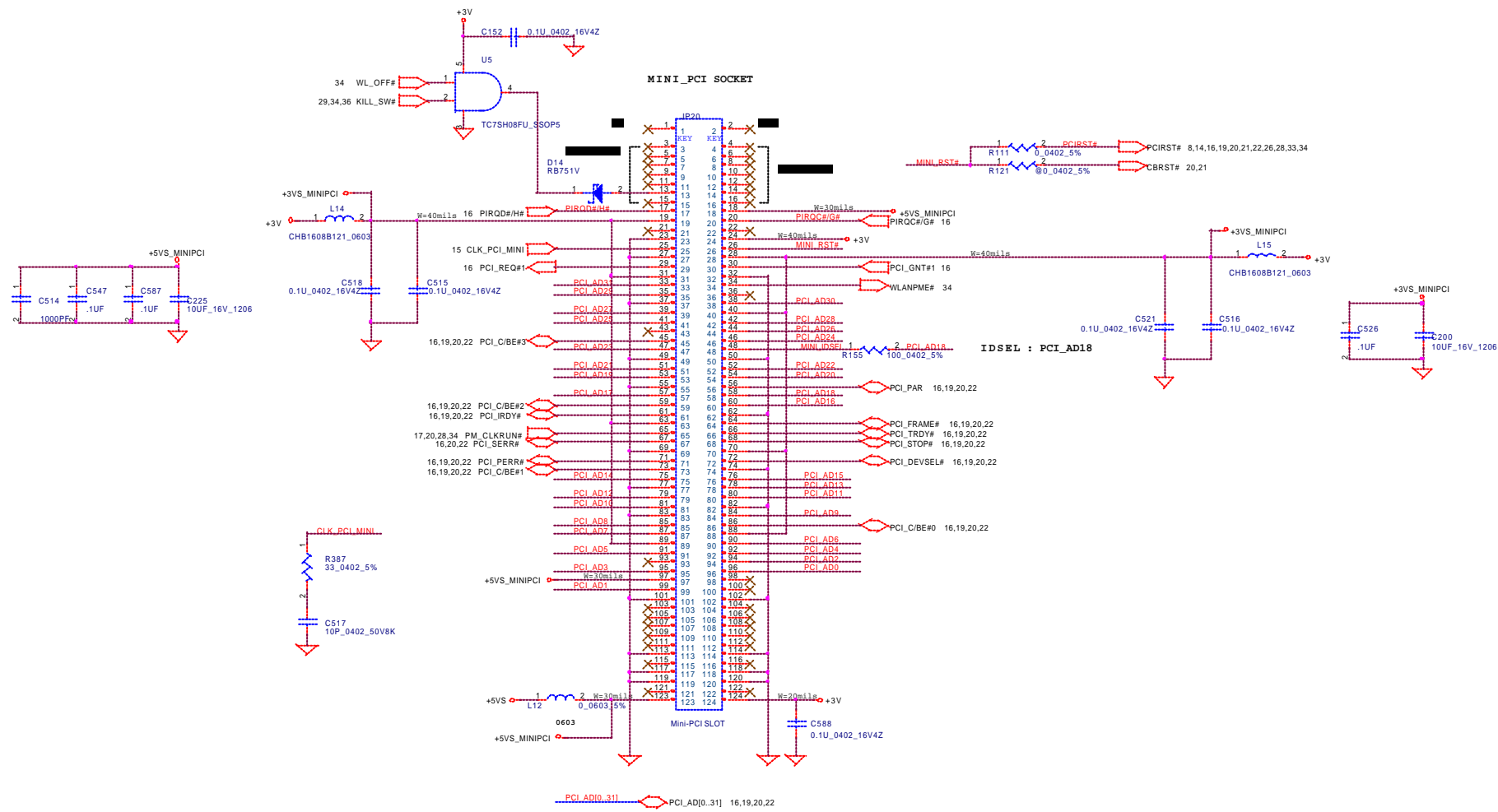
LAYOUT NOTICE: This area do not connect to power plan include Vcc and GND in any layer

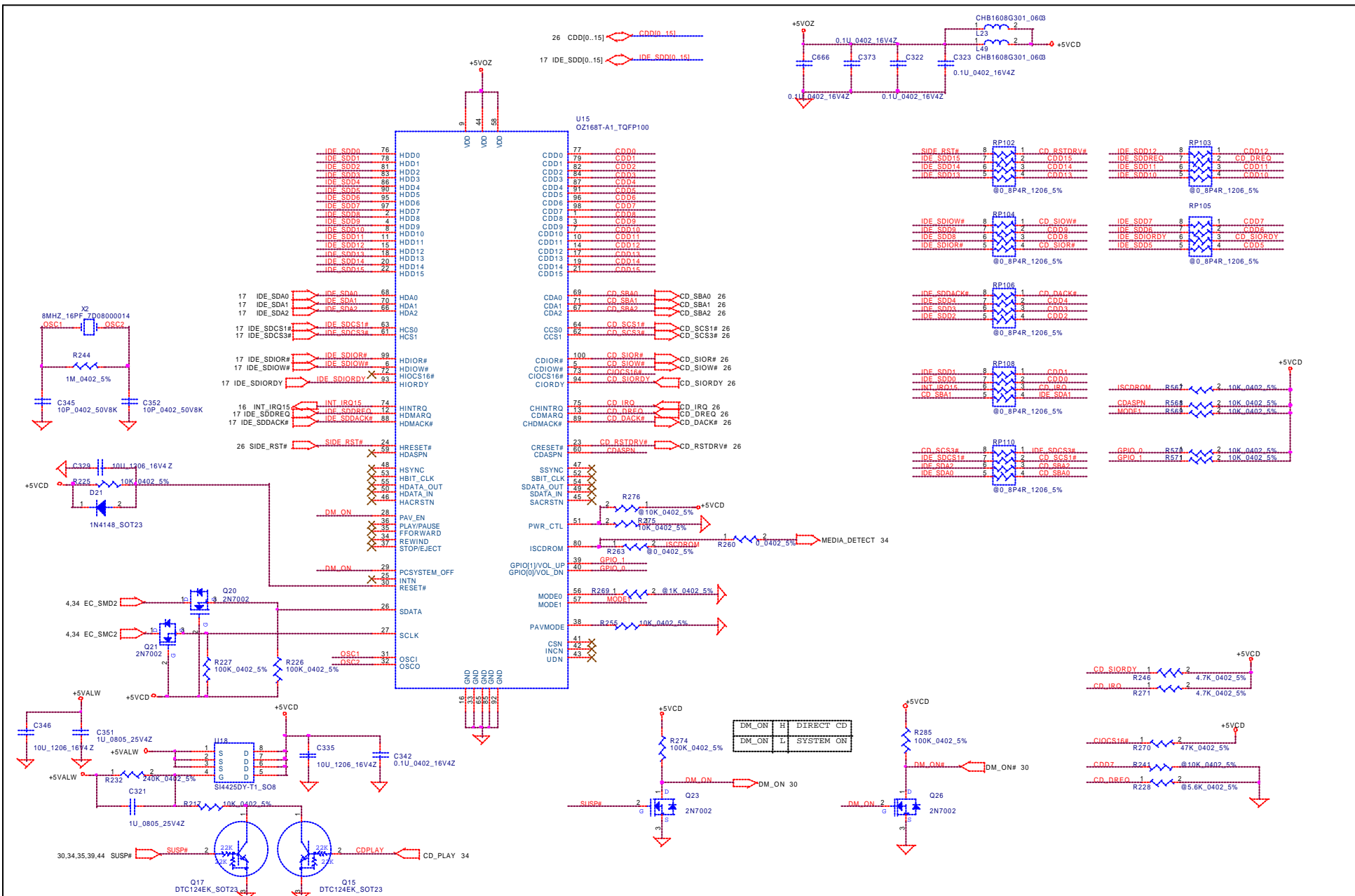


Termination plane should be copied to chassis ground and also depends on safety concern

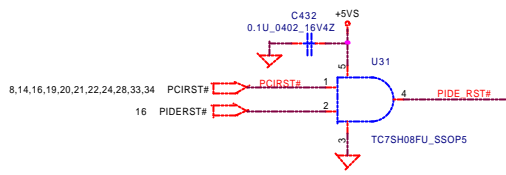
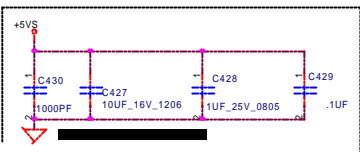
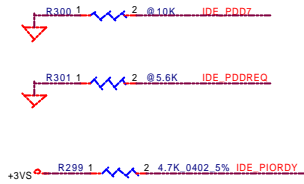
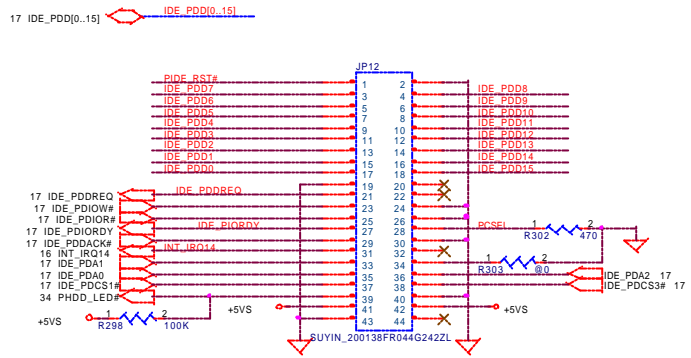


Compal Electronics, Ltd			
RJ11/RJ45 Connector			
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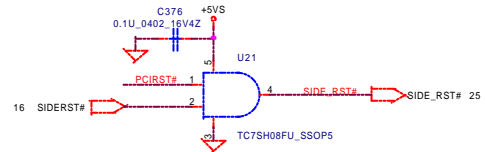
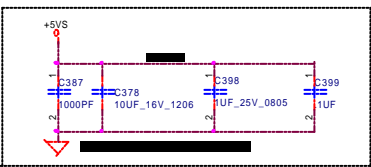
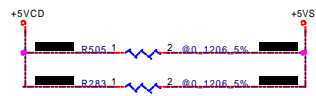
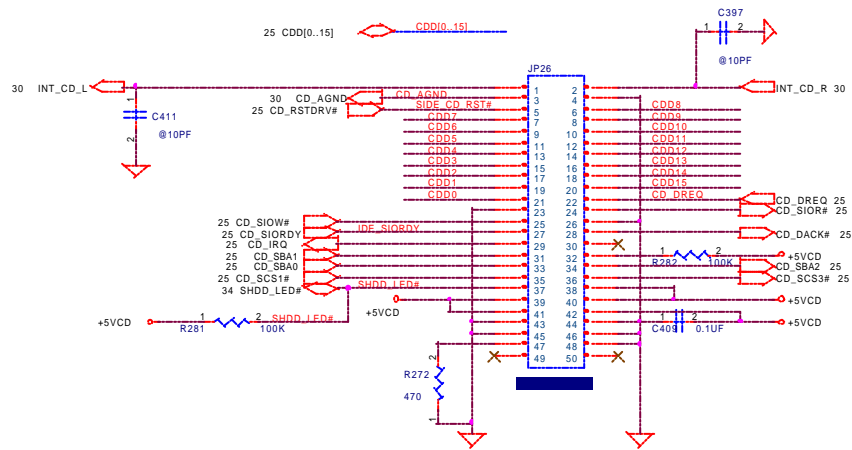




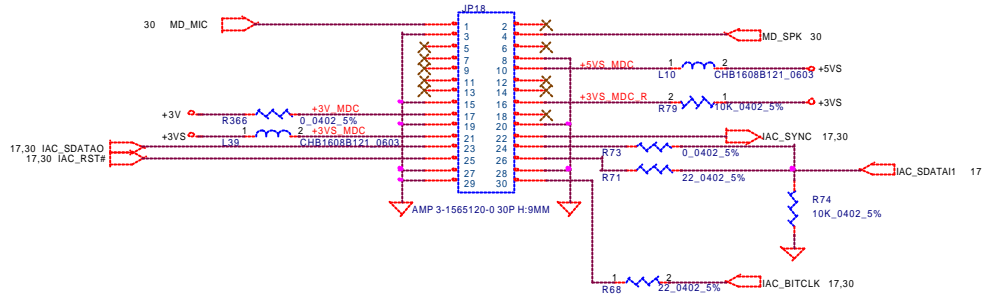
IDE Module CONN.



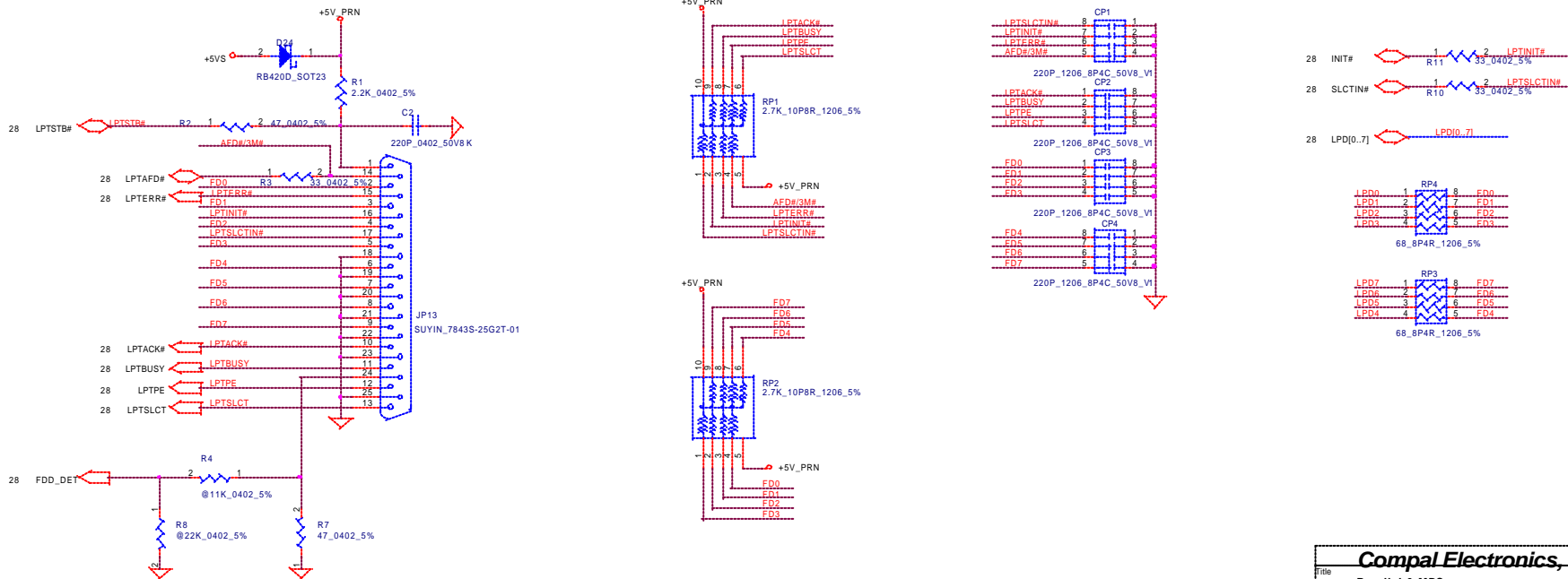
CD-ROM Module CONN.



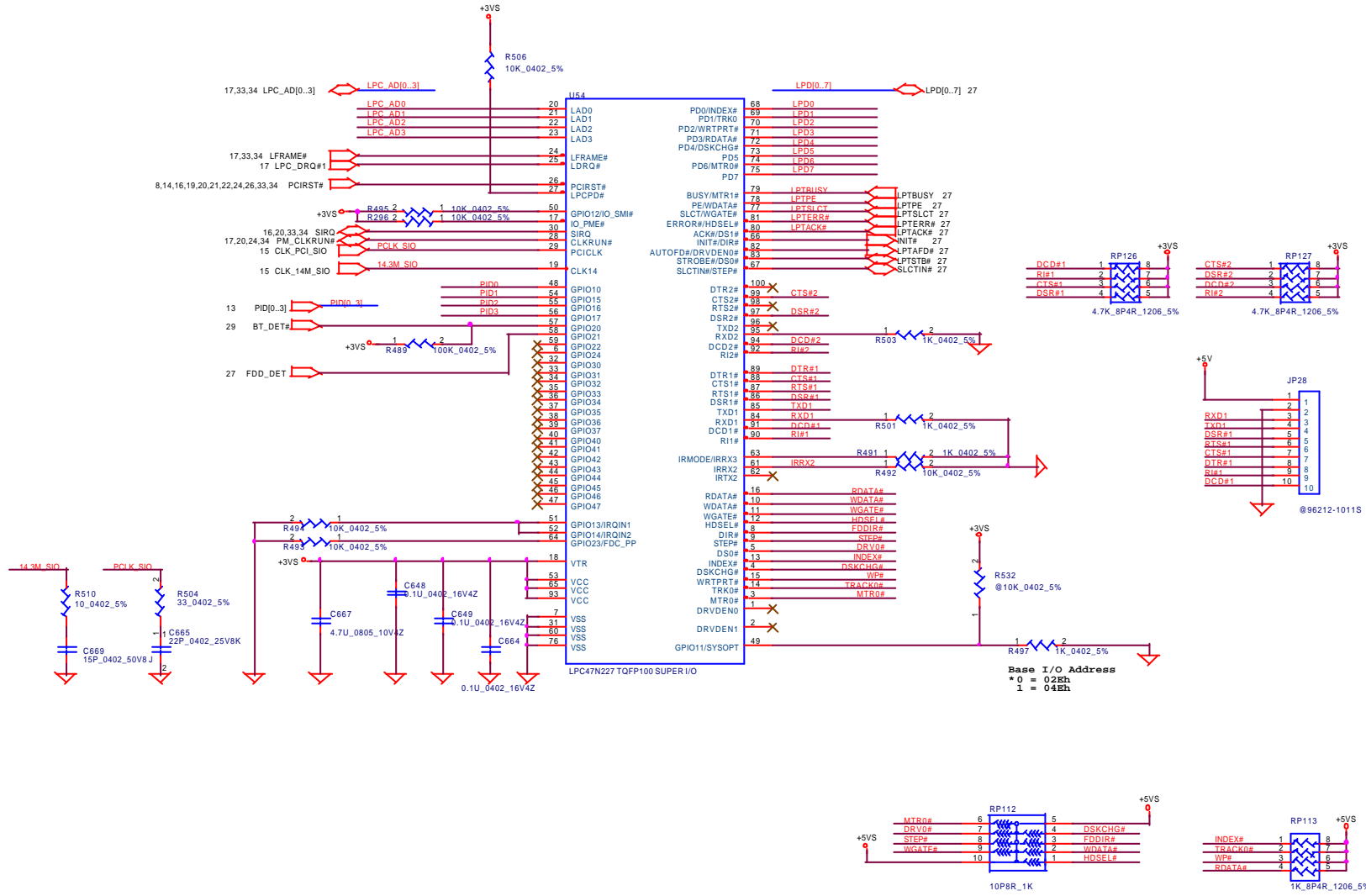
MDC Connector



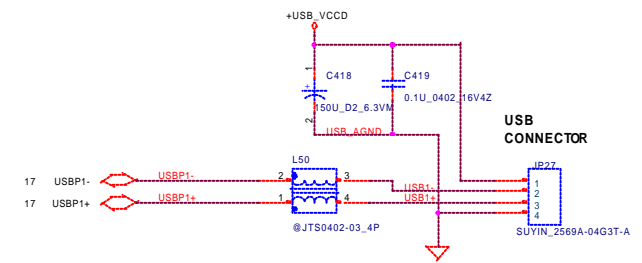
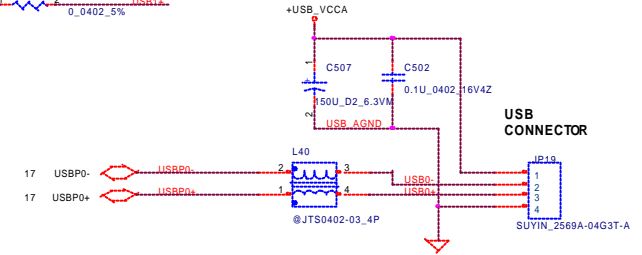
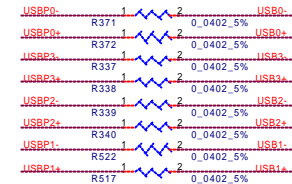
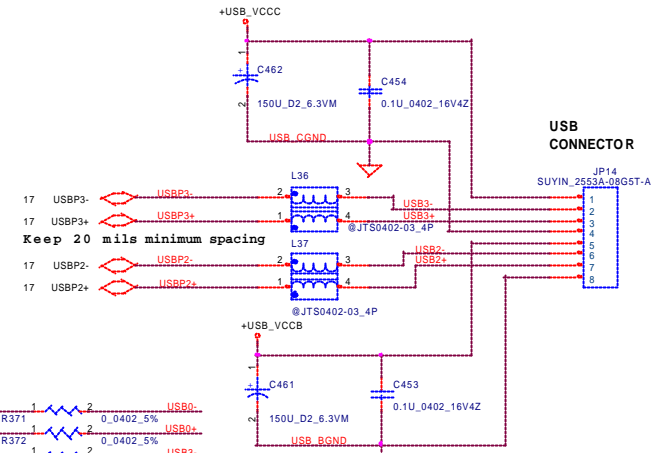
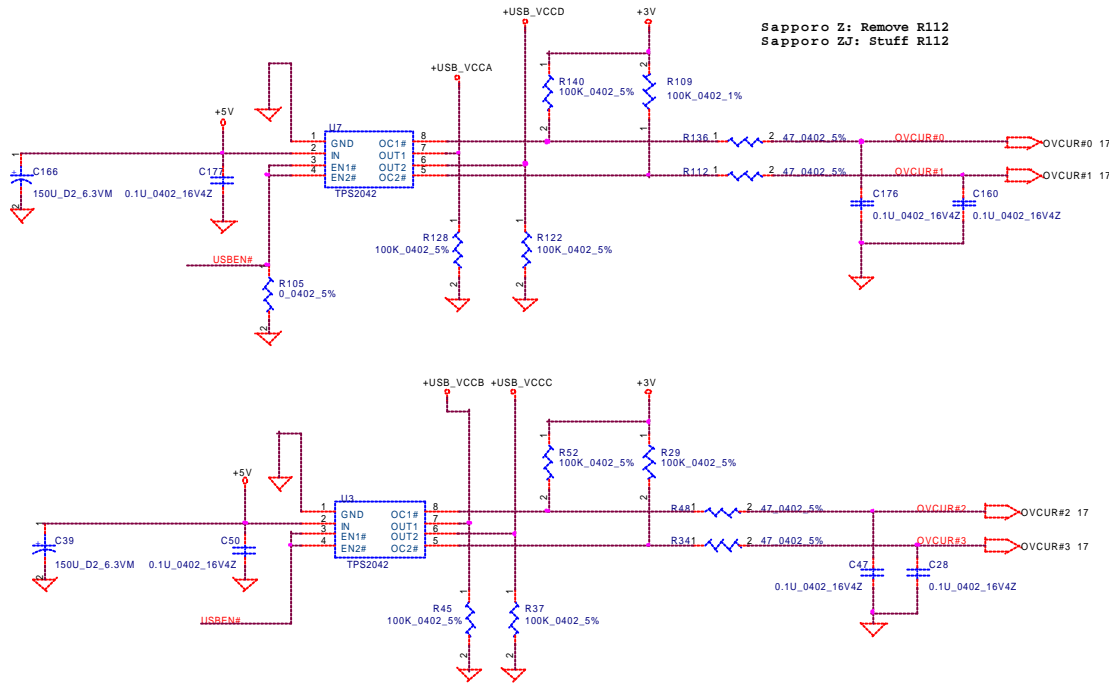
Parallel Port



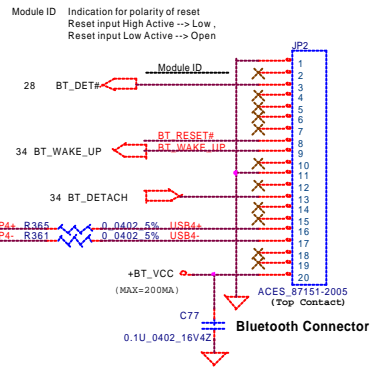
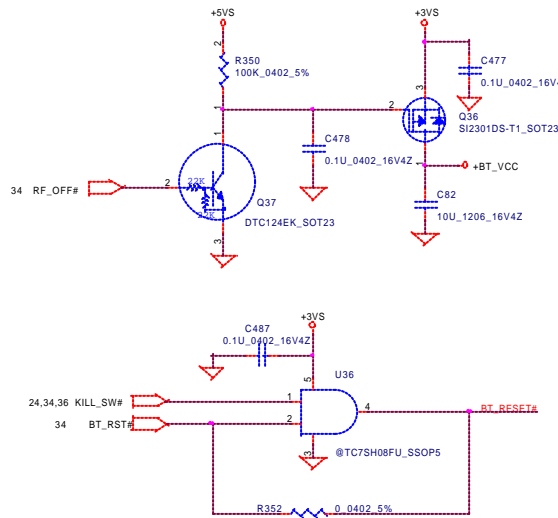
SUPER I/O SMCs FDC47N227



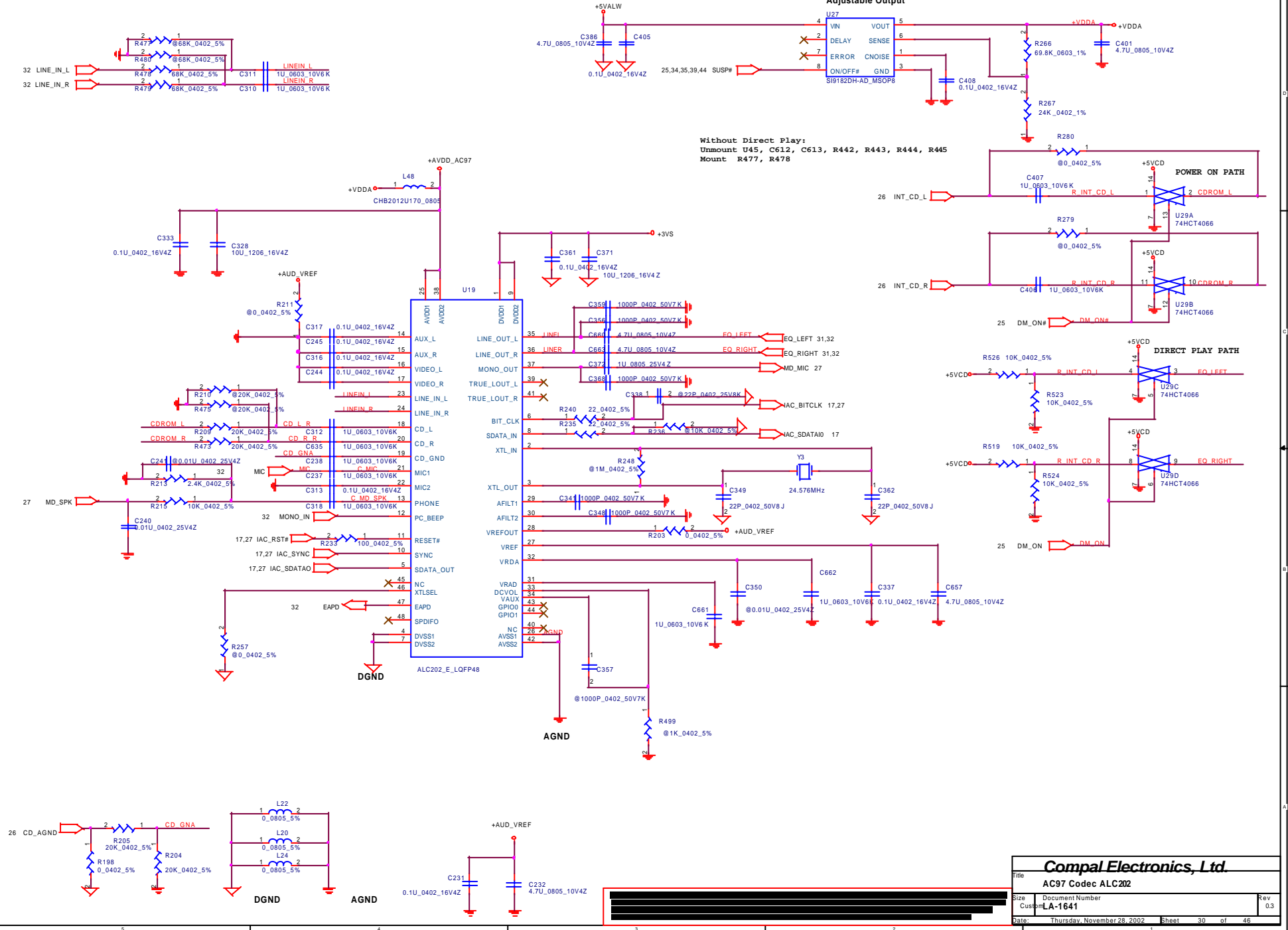
Sapporo Z: Remove R112
Sapporo ZJ: Stuff R112



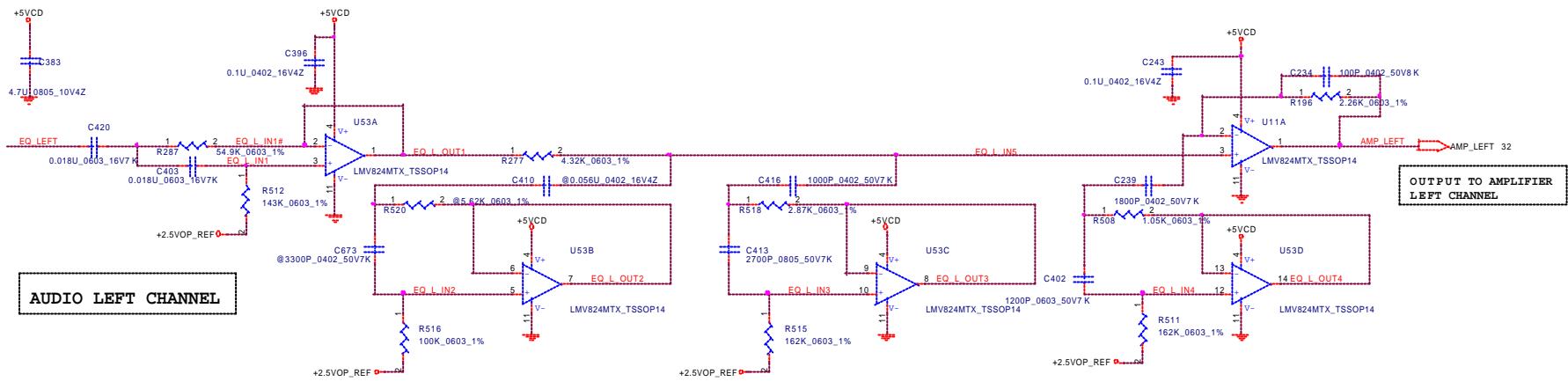
BlueTooth Interface



AC97 Codec



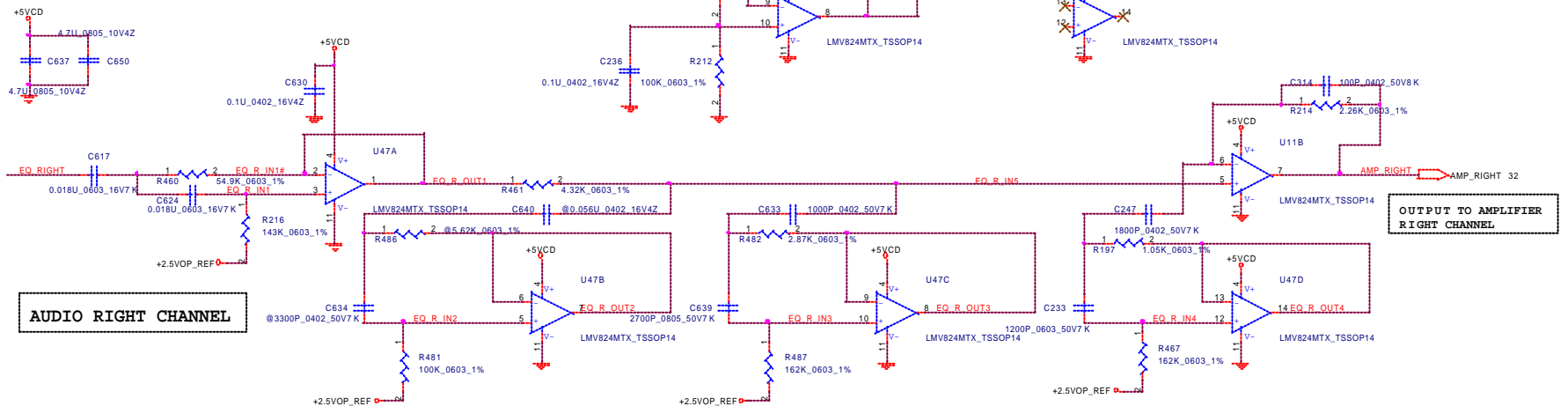
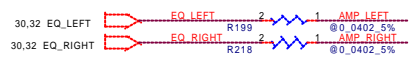
Compal Electronics, Ltd. File: AC97 Codec ALC202		
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AUDIO LEFT CHANNEL

OUTPUT TO AMPLIFIER LEFT CHANNEL

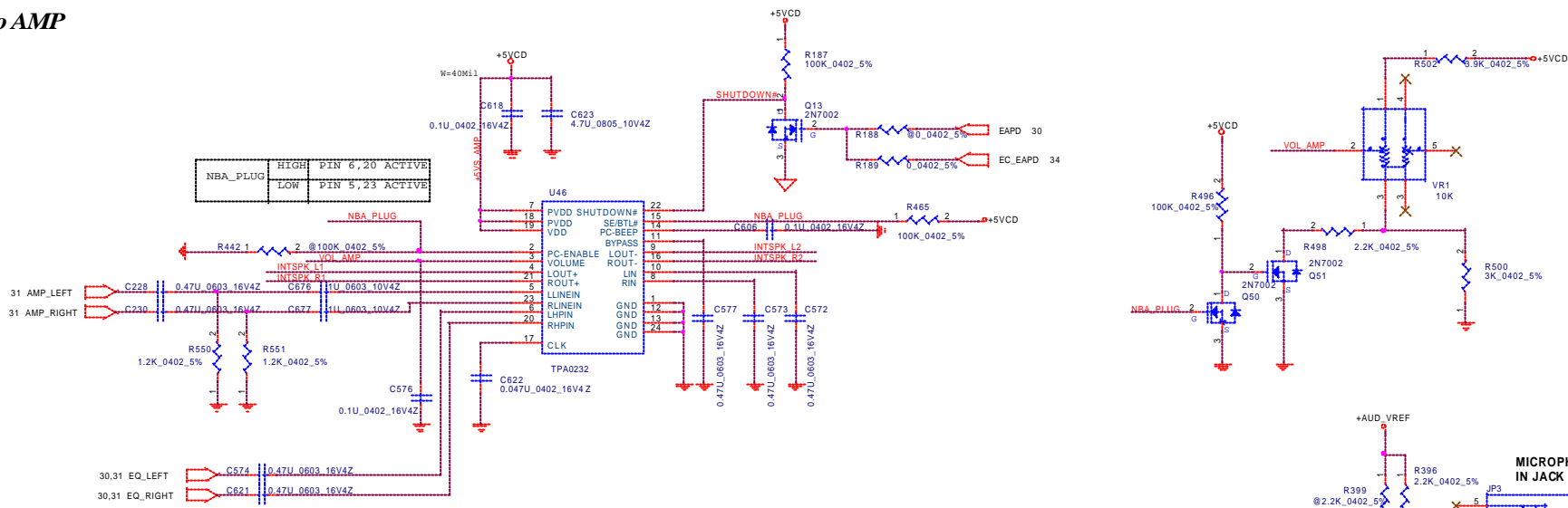
BY-PASS EQ CIRCUIT



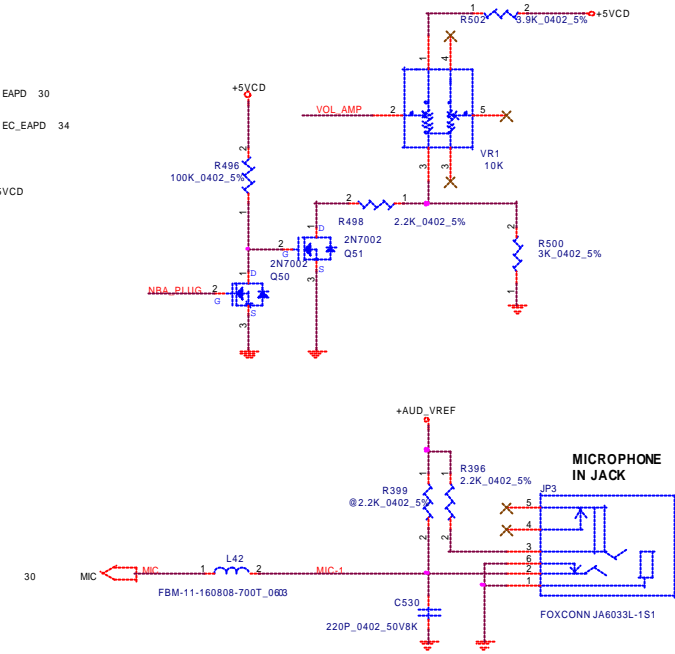
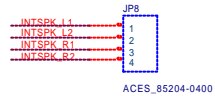
AUDIO RIGHT CHANNEL

OUTPUT TO AMPLIFIER RIGHT CHANNEL

Audio AMP



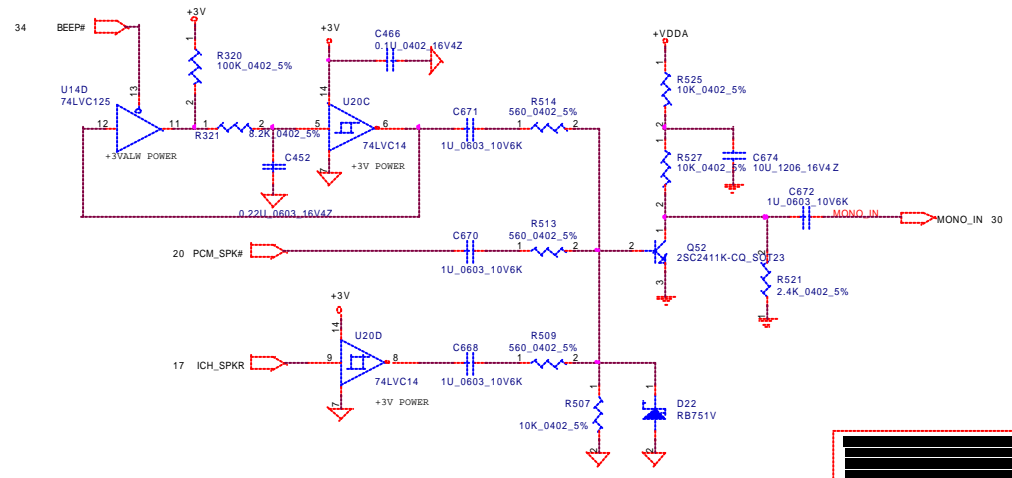
Speaker Connector



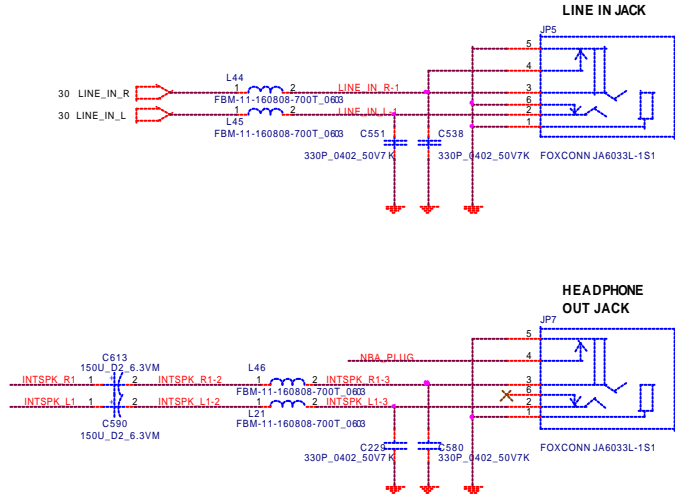
MICROPHONE IN JACK

LINE IN JACK

System Sound

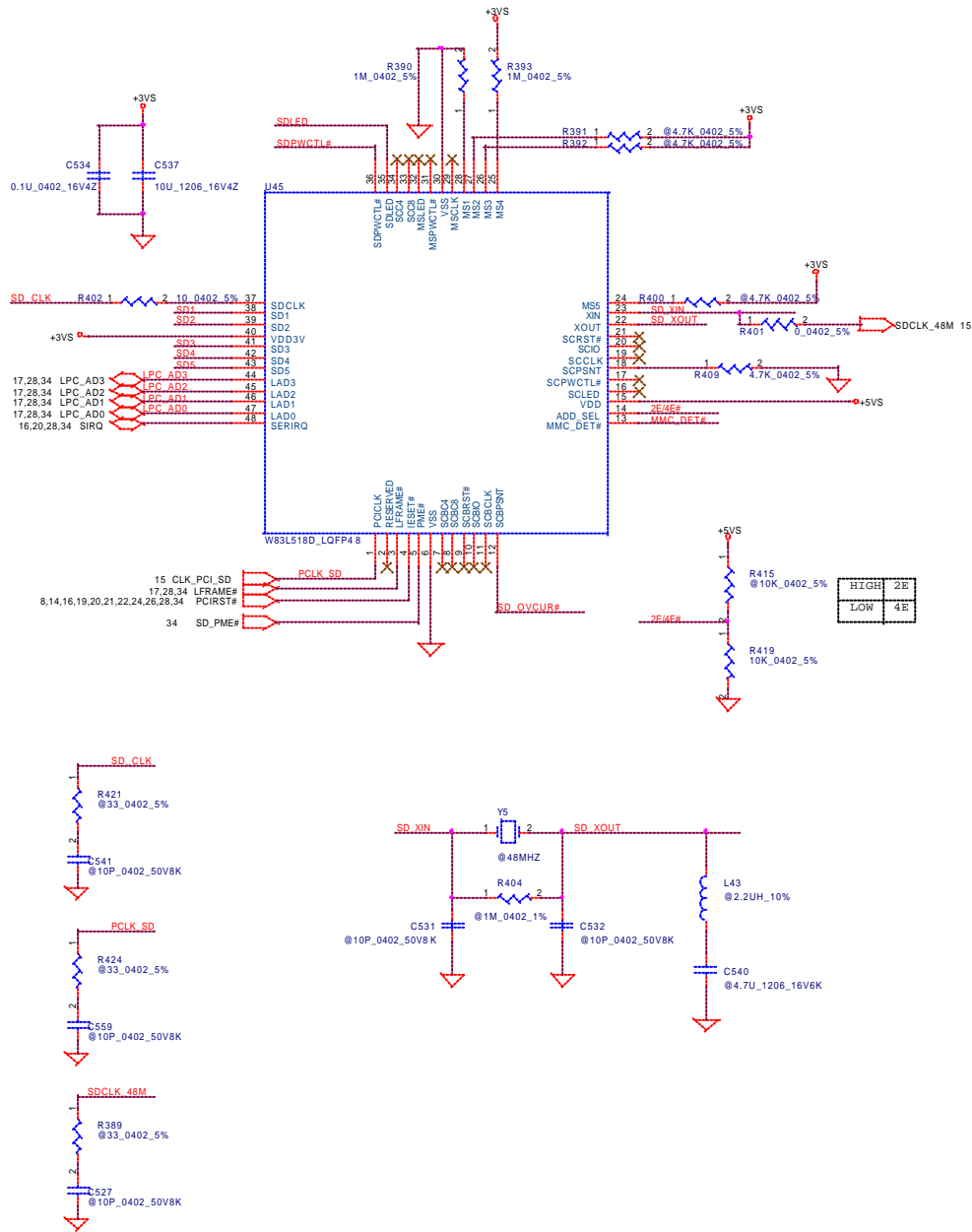


HEADPHONE OUT JACK

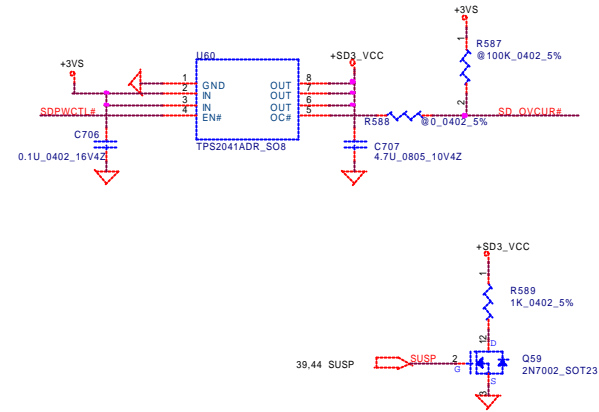


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Audio AMP & JACK			
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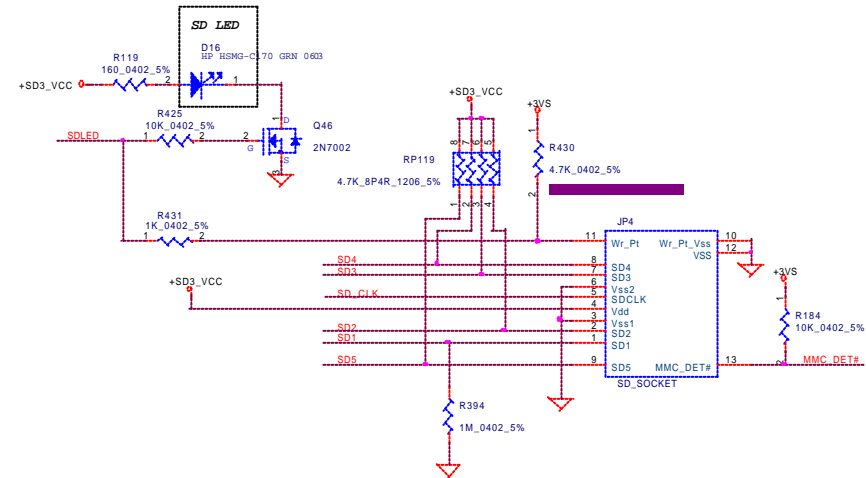
SD Card Reader

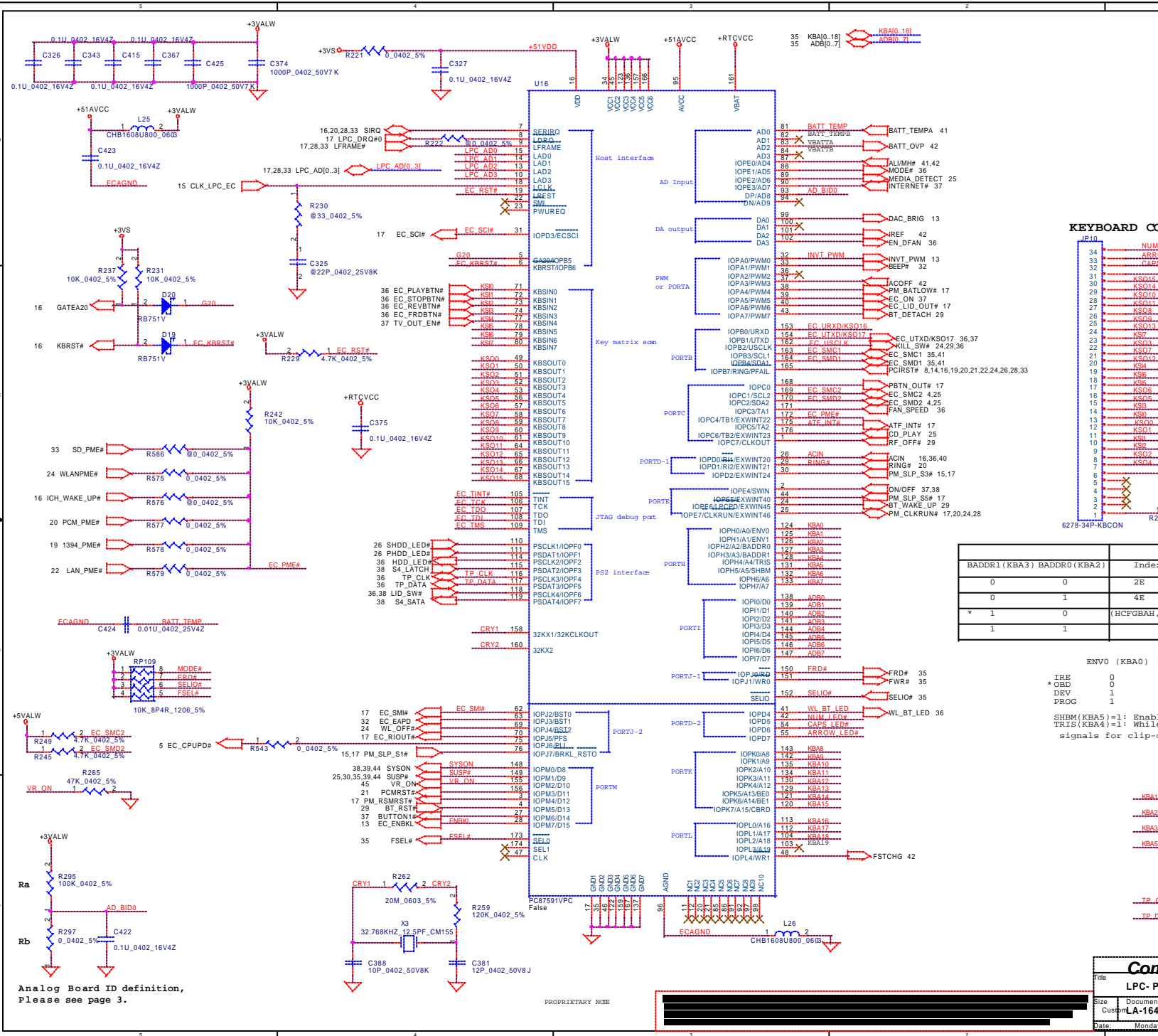


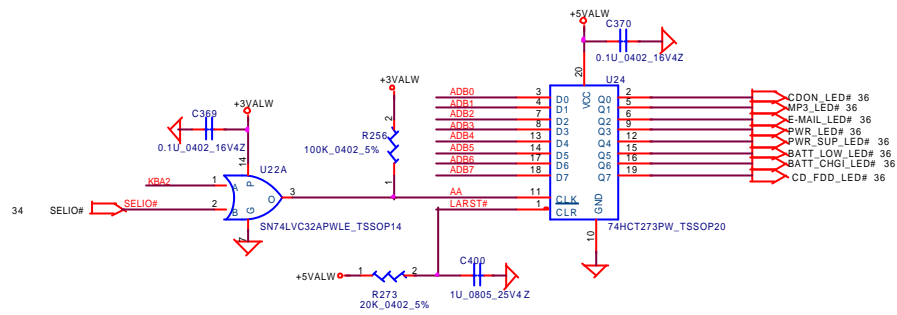
SD Power Switch



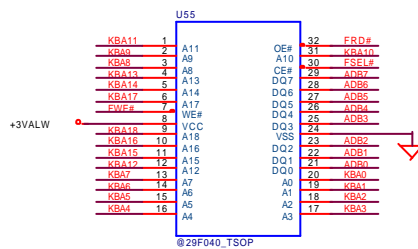
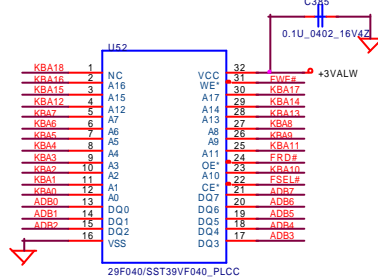
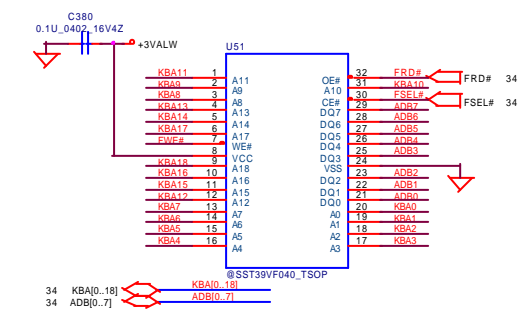
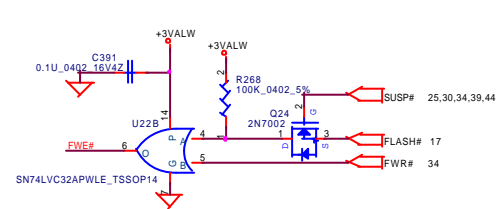
SD SOCKET



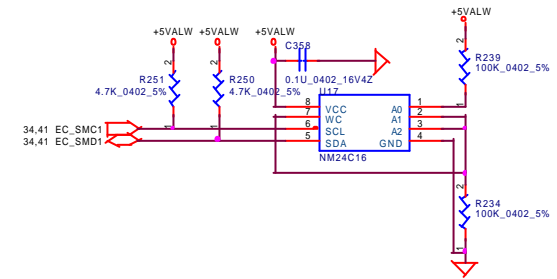




System BIOS

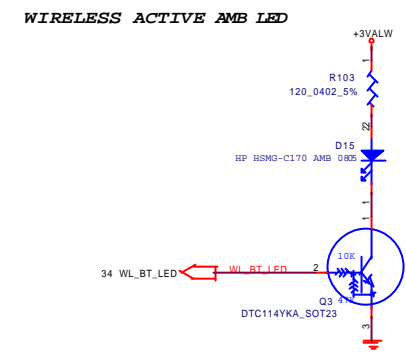
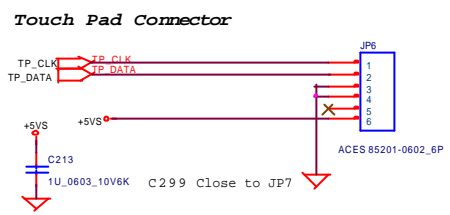
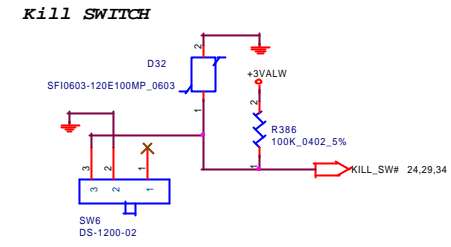
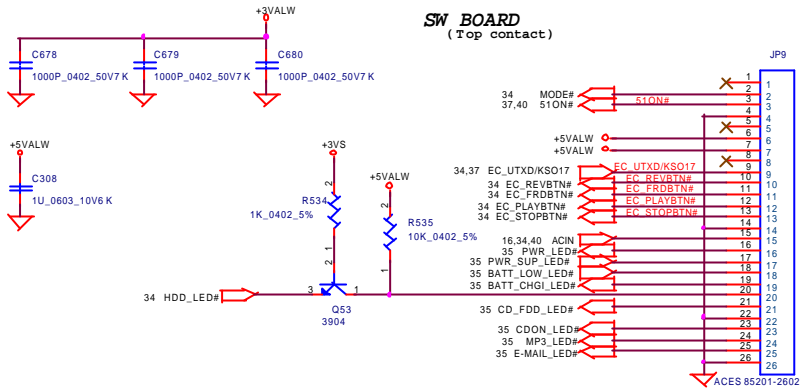


SMBus EEPROM

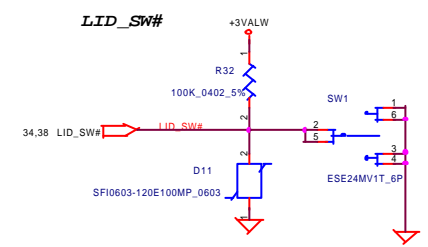
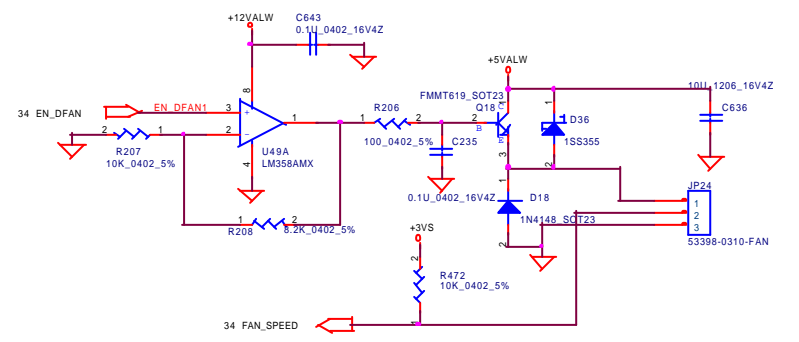


Compal Electronics, Ltd.

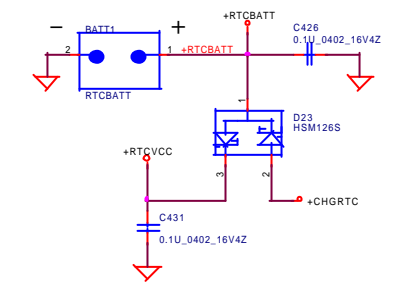
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FAN CONN

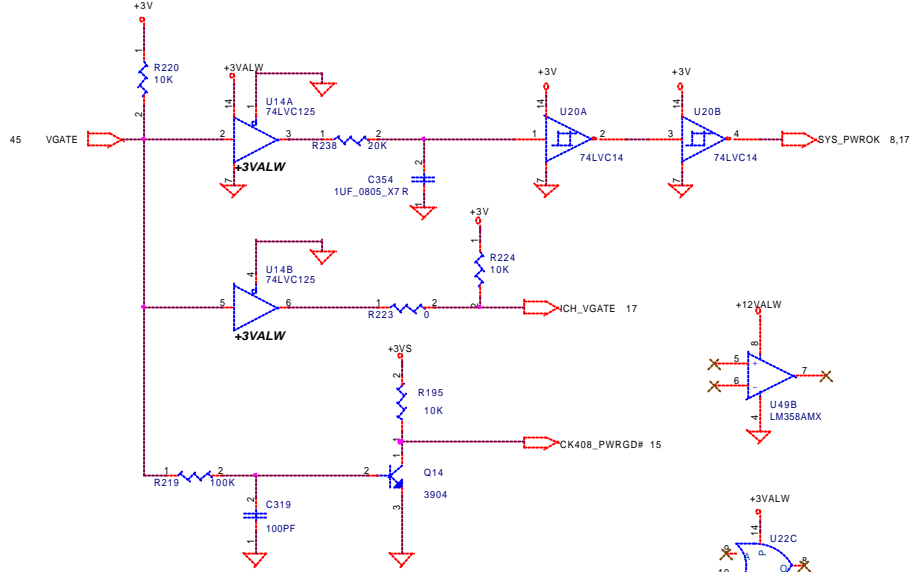


RTC BATT

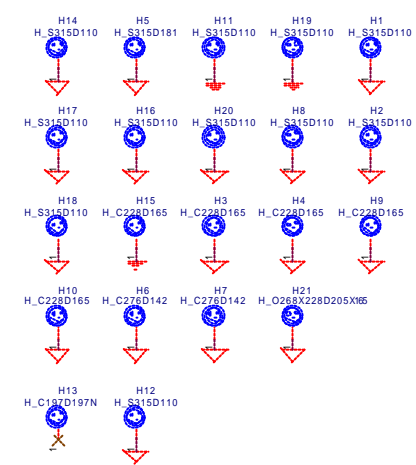
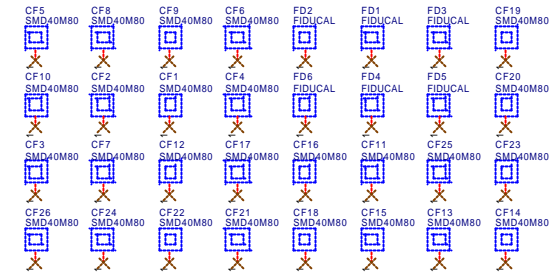
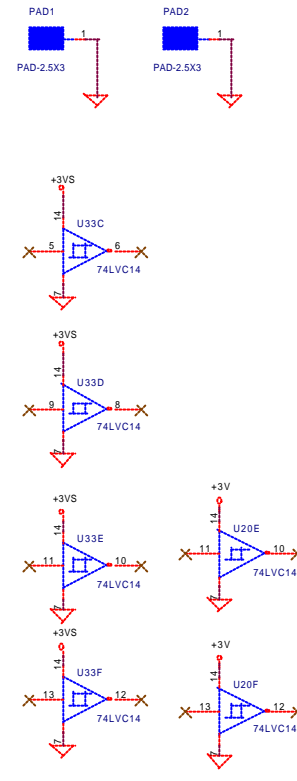


Compal Electronics, Ltd.			
System Connectors			
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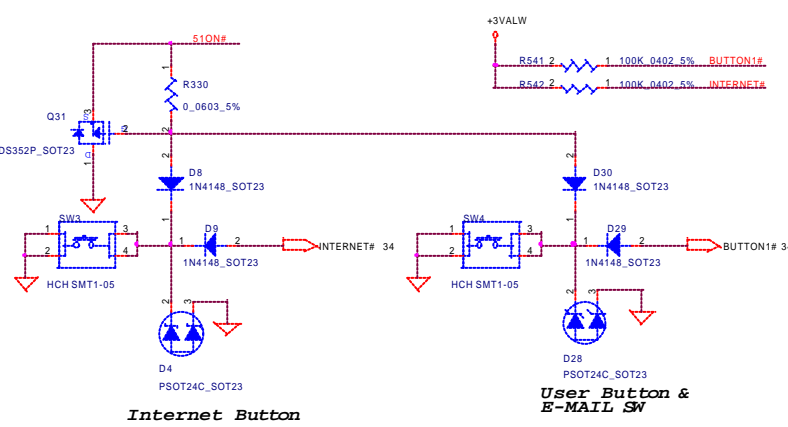
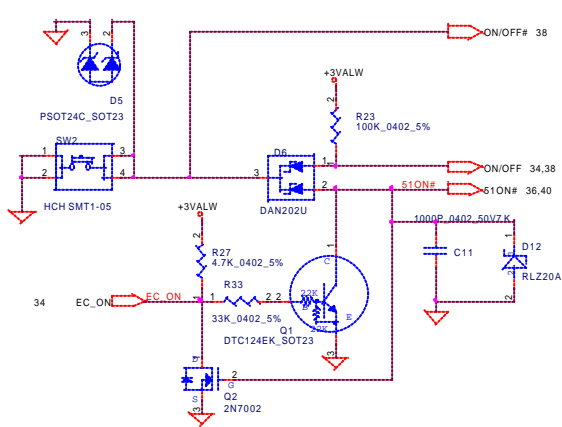
Power Good Circuit



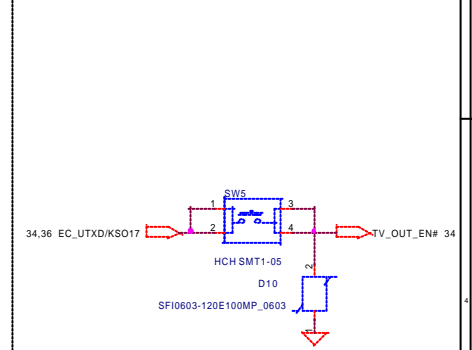
EMI Clip PAD for CPU



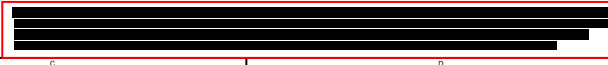
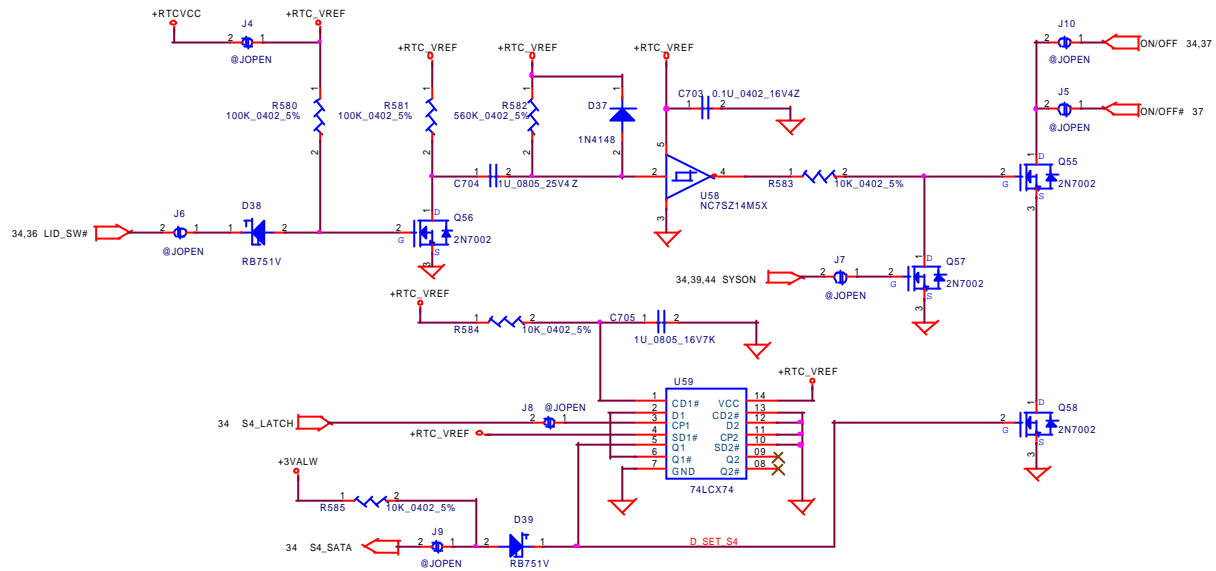
Power Button



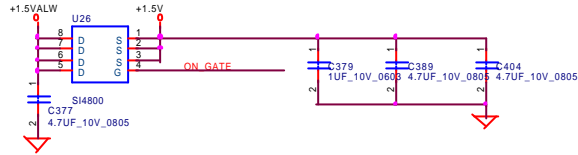
TV-OUT BUTTON



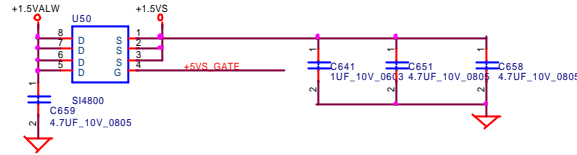
Compal Electronics, Ltd			
PowerGood			
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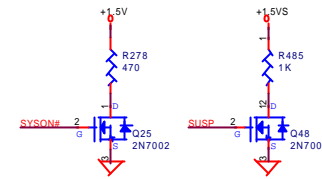
+1.5VALW To +1.5V Transfer



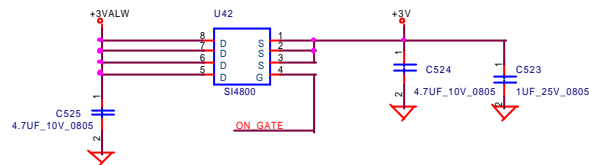
+1.5VALW To +1.5VVS Transfer



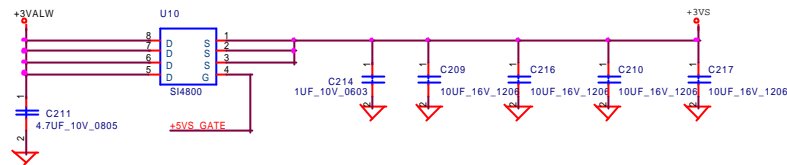
+1.5V & +1.5VVS Discharge



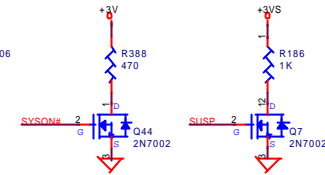
+3VALW To +3V Transfer



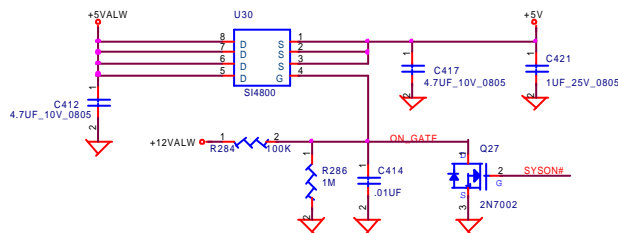
+3VALW To +3VVS Transfer



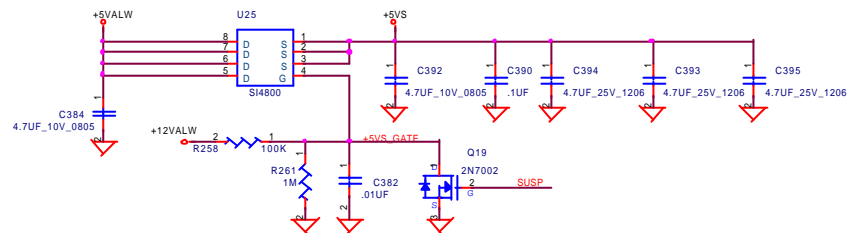
+3V & +3VVS Discharge



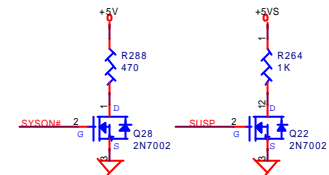
+5VALW To +5V Transfer



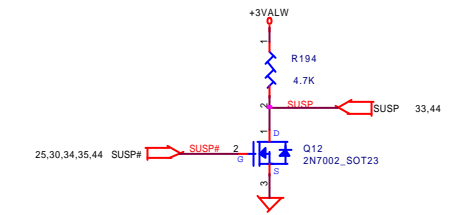
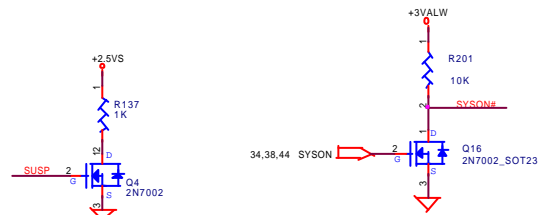
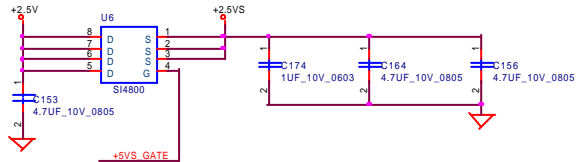
+5VALW To +5VVS Transfer

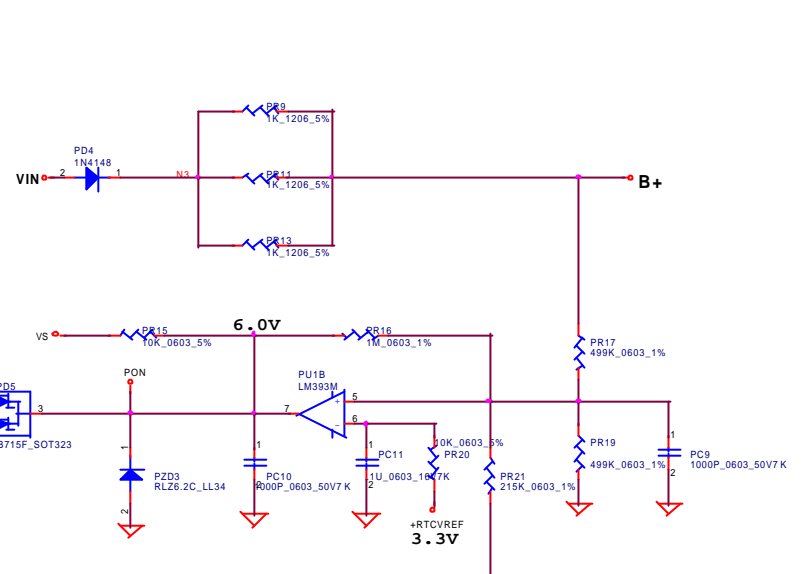
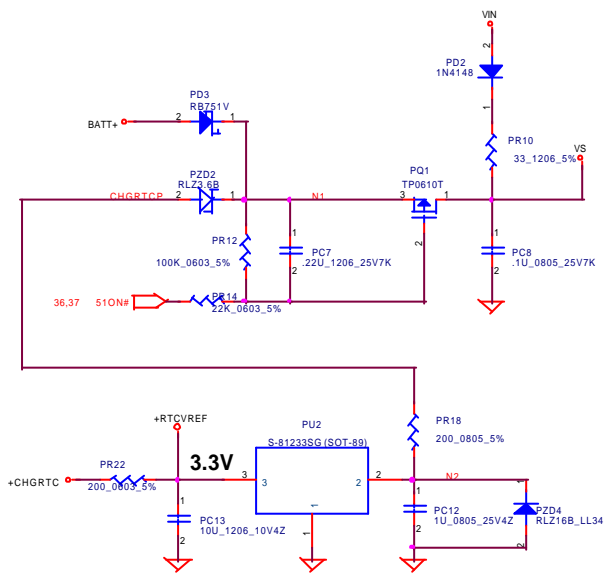
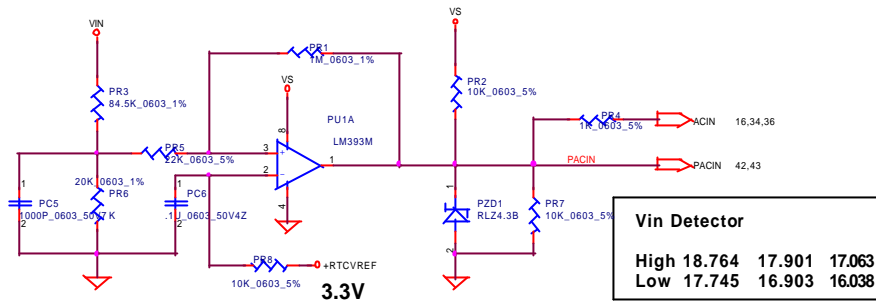
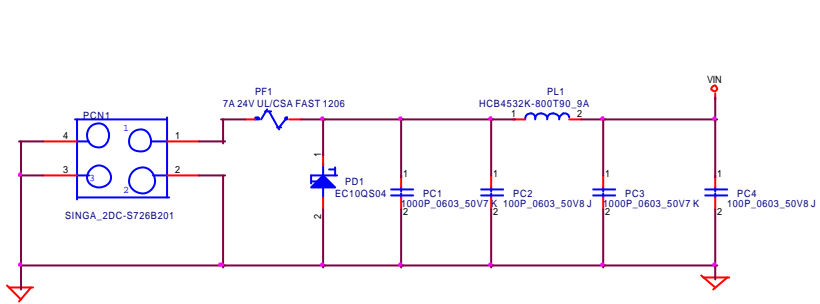


+5V & +5VVS Discharge

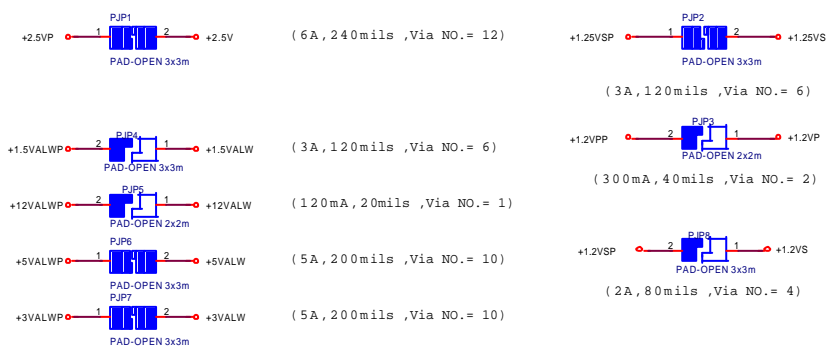


+2.5V To +2.5VVS Transfer





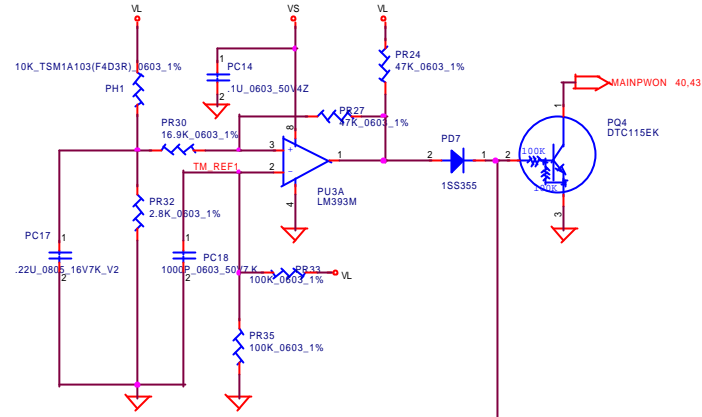
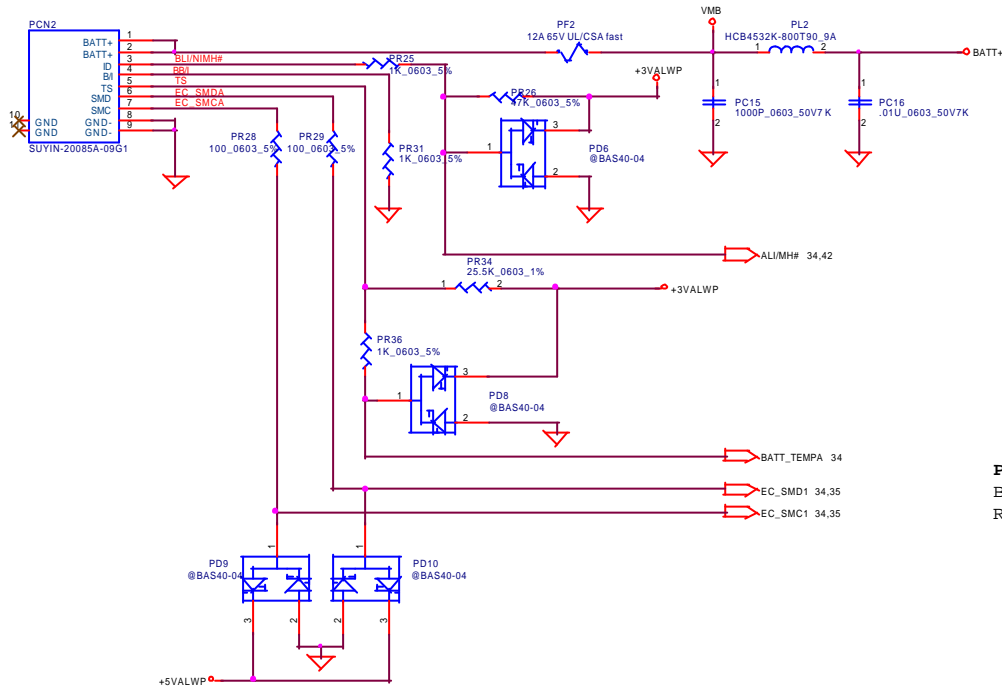
Precharge detector		
	15.34	15.90
	13.13	13.71



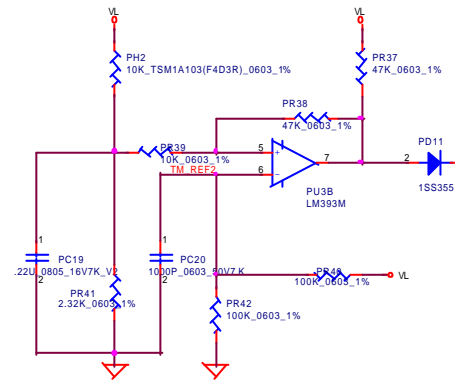
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DCIN & DETECTOR		
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PH1 under CPU bottom side :
 CPU thermal protection at 90(91) degree C
 Recovery at 50 degree C



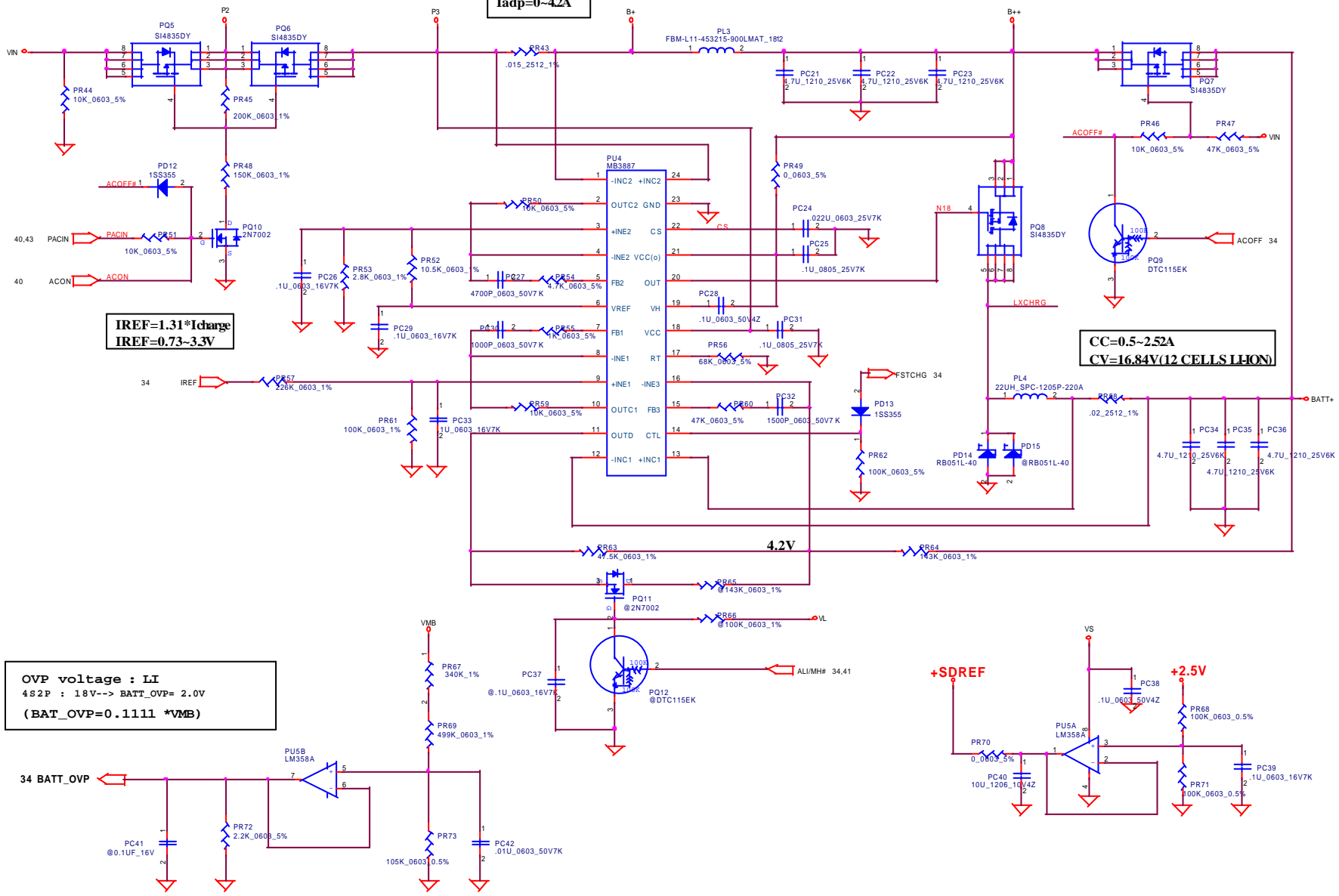
PH2 near main Battery CONN :
 BAT. thermal protection at 85 degree C
 Recovery at 60(61) degree C



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Compal Electronics, Inc.			
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Iadp=0-42A



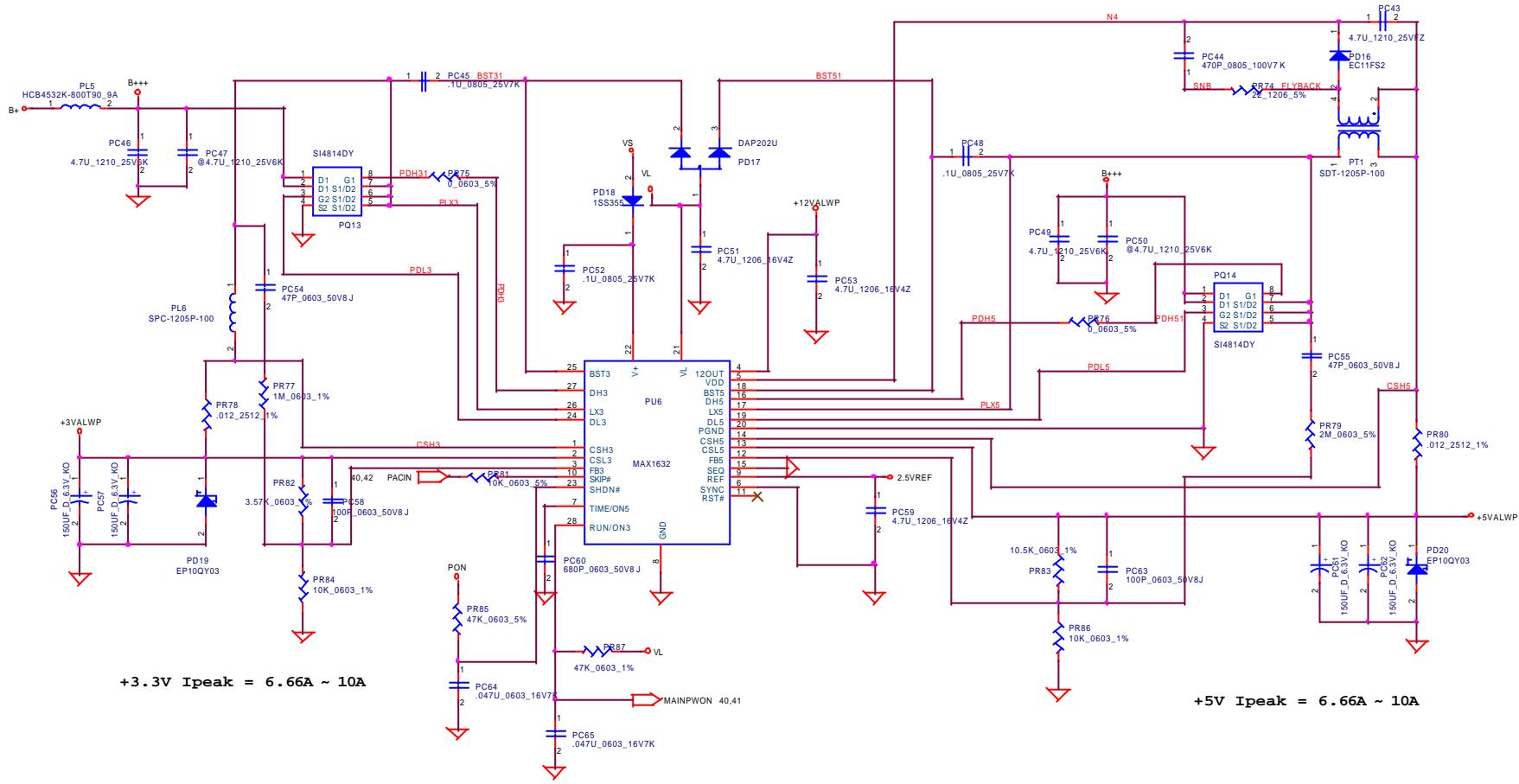
IREF=1.31*Icharge
IREF=0.73-3.3V

CC=0.5-2.52A
CV=16.84V(12 CELLS LIION)

OVP voltage : LI
4S2P : 18V--> BATT_OVP= 2.0V
(BATT_OVP=0.1111 *VMB)

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Compal Electronics, Inc.		
CHARGER		
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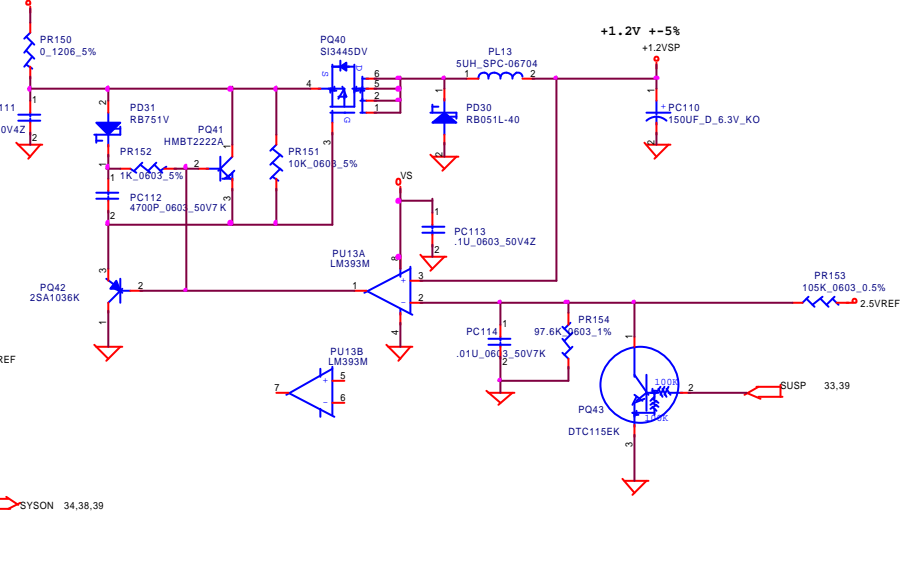
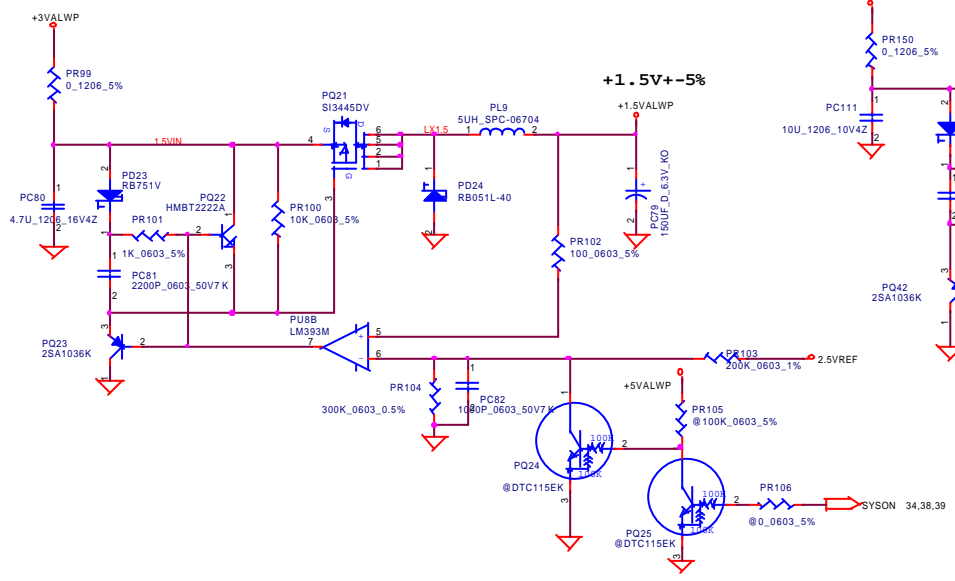
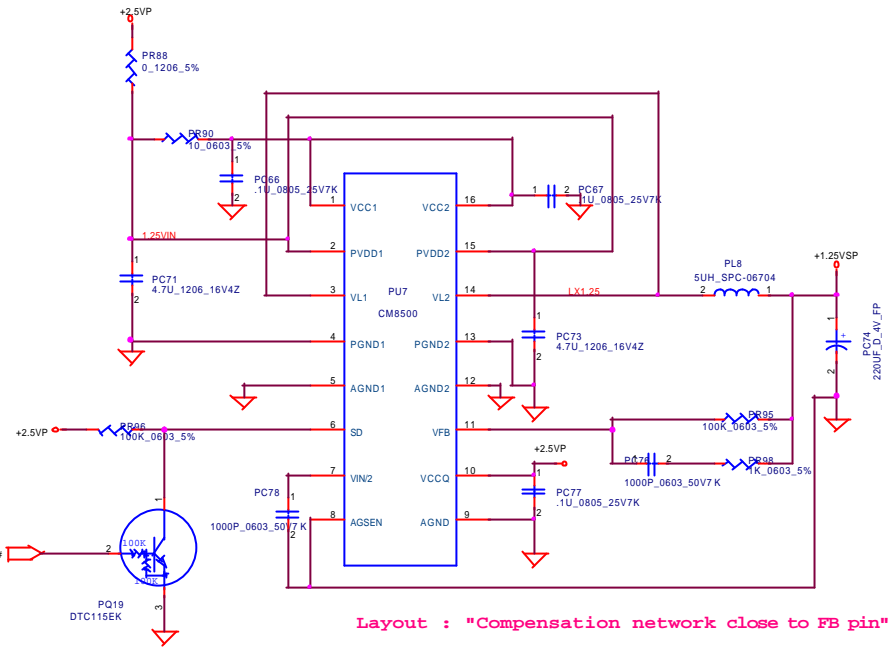
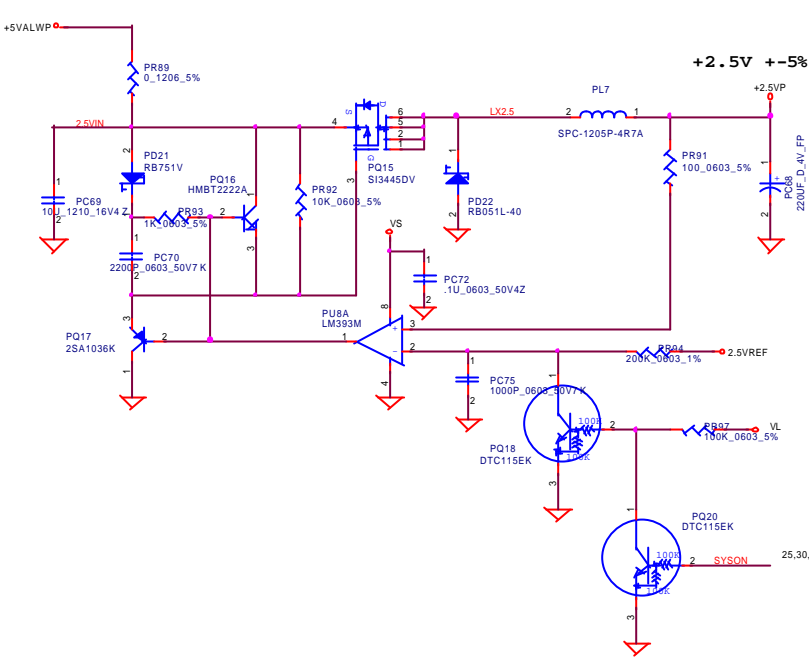


+3.3V Ipeak = 6.66A ~ 10A

+5V Ipeak = 6.66A ~ 10A

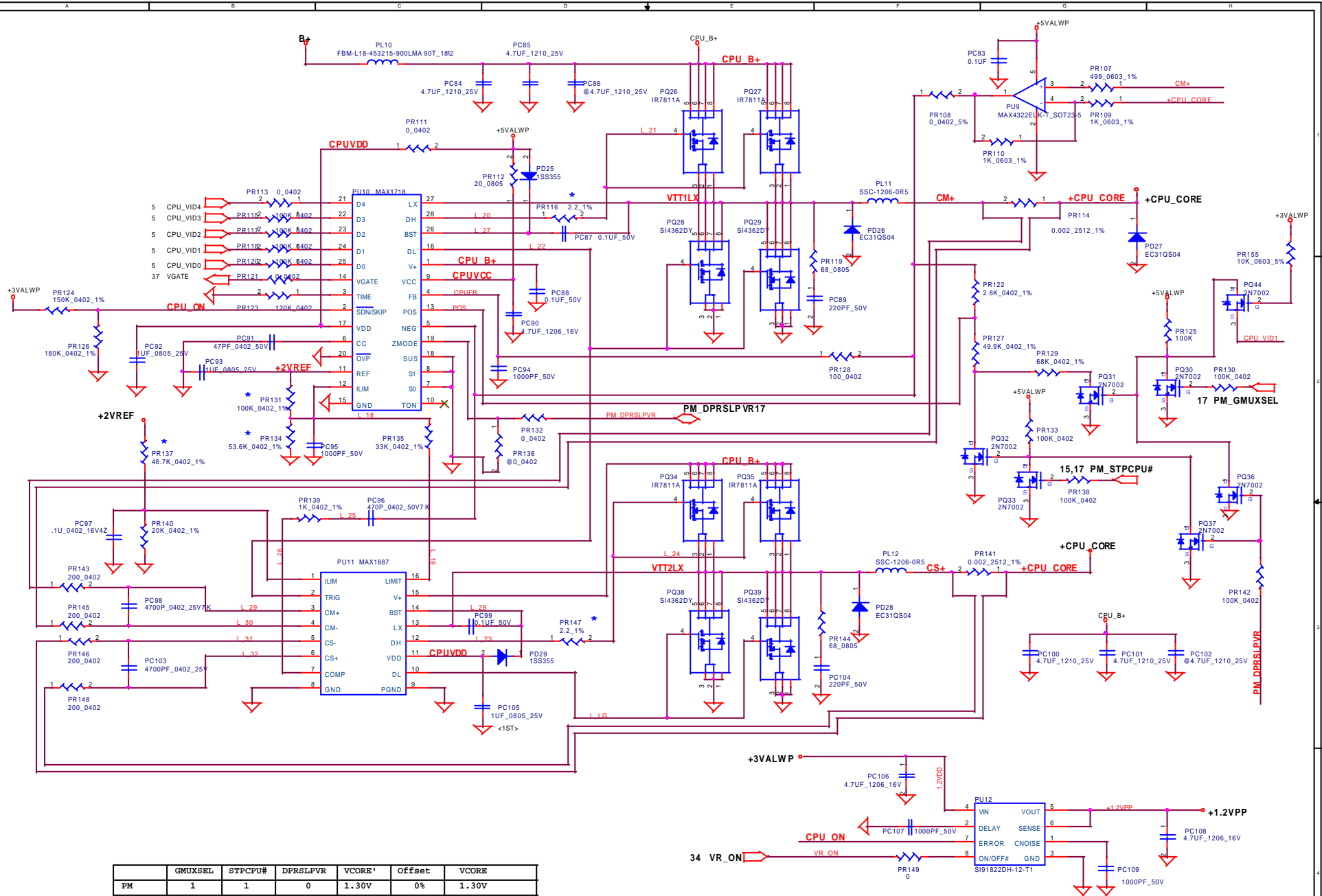
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Compal Electronics, Inc.			
File	5V/3.3V/12V		
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Compal Electronics, Inc.			
DDR / 2.5V / 1.25V/1.5V			
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	GMUXSEL	STPCPU#	DPRSLPVR	VCORE'	Offset	VCORE
PM	1	1	0	1.30V	0%	1.30V
PM D-S	1	0	0		4.62%	1.239V
BM	0	1	0	1.20V	2.0%	1.176V
BM D-S	0	0	0		4.62%	1.144V
Deeper	X	0	1	1.0V	0%	1.0V

Compal Electronics, Inc.

+CPU CORE

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REV 0.2

Date	Page	Description
09/27		Update Rev0.1 to Rev.0.2
10/16	8	Change U32(SSC) source from CLK_VCH to CLK_MCH_48M
	8	Change Q55 R537 R538 to U33A
	13	Add zero Ohm resistor between pin3 of JP1 and GND.
	15	Add R539 R540 2.2K pull high to +3VALW on net SMB_DATA and SMB_CLK
10/17	17	Add R549 on ICH4 GPI7 pull high to +3VS
	26	Add J3 between +5VS and +5VS_IDE
	17	Delete net USB_EN# and PAL/NTSC# on U12 pinW4 & pinW1
	29	Modify BlueTooth schematic
	32	Add Pass-High Filter (R550, R551, C676, C677) on net AMP_LEFT, AMP_RIGHT
	32	Change R465 power plan from +5VS to +5VCD
	34	Add Net Thertrip#, PM_SLP_S1#, BT_RST# on EC
35	Change U23 to U22B	
10/18	36	Change FAN Schematic from PWM to RPM
	37	Add R541 and R542 100K pull high to +3VALW on net Button1#, Internet#
10/22		Formal release Schematic Rev0.2
10/24	44	Add P4-M/P4-C auto detection schematic, PQ44, PR155
11/18	42	Change PC43 to 4.7U
11/18	40	Change PR32 to 2.8K, PR41 to 2.32K
11/20	34	Add R575, R576, R577, R578, R579 between device PME#s and EC_PME#



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