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# DAKAR10F/FG

2011.09.02

DATE	CHANGE NO.	REV
21-OCT-2002		

DRAWER		EE	DATE	POWER	DATE	<b>INVENTEC</b> <small>TITLE MODEL PROJECT, FUNCTION Everest Main Board</small>			
DESIGN									
CHECK									
RESPONSIBLE									
SIZE=		VER:		SIZE	CODE	DOC NUMBER	REV		
FILE NAME:		1310xxxx-0-0		C	CS		X01		
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**AMD**  
W/ POWER EXPRESS  
THAMES  
29X 29 MM

**IVY BRIDGE**  
DC 35W  
SOCKET-RPGA989  
37.5 X 37.5 X 5 mm

DDR3@1.5/0.75V  
(1333/1600 MHZ)  
204-PIN SODIMM0

DDR3@1.5/0.75V  
(1333/1600 MHZ)  
204-PIN SODIMM1

HDMI

CRT

LCM  
LVDS

RJ45

PCIE\_1:LAN  
ATHEROS\_AR8161/8162  
PCIE

PCIE\_2:WLAN  
PCIE

PCIE\_3:USB3.0  
PCIE

**PCH**  
PANTHER POINT  
25 X 25 X 2.3 mm

AUDIO CODEC  
REA\_ALC269Q\_VB6  
HDA

INTERNAL MIC IN  
EXT MIC IN  
HEADPHONE

USB\_0: USB CONN  
USB\_2: USB CONN  
USB\_8: CARD READER  
USB\_9: MINICARD WLAN  
USB\_10:WEBCAM

SLEEP & CHARGE

USB\_1: USB3.0 CONN

USB\_8: CARD READER  
REA\_RTS5129

SATA0:ESATA  
SATA1: HDD  
SATA6: ODD

ENE-P2809A  
THERMAL SENSOR

BATTERY CHARGER &  
DC/DC & IMVP 7

LI-ION BATTERY  
6-Cell

EC WINDBOND  
NPCE885LA0DX  
SPI

KEYBOARD

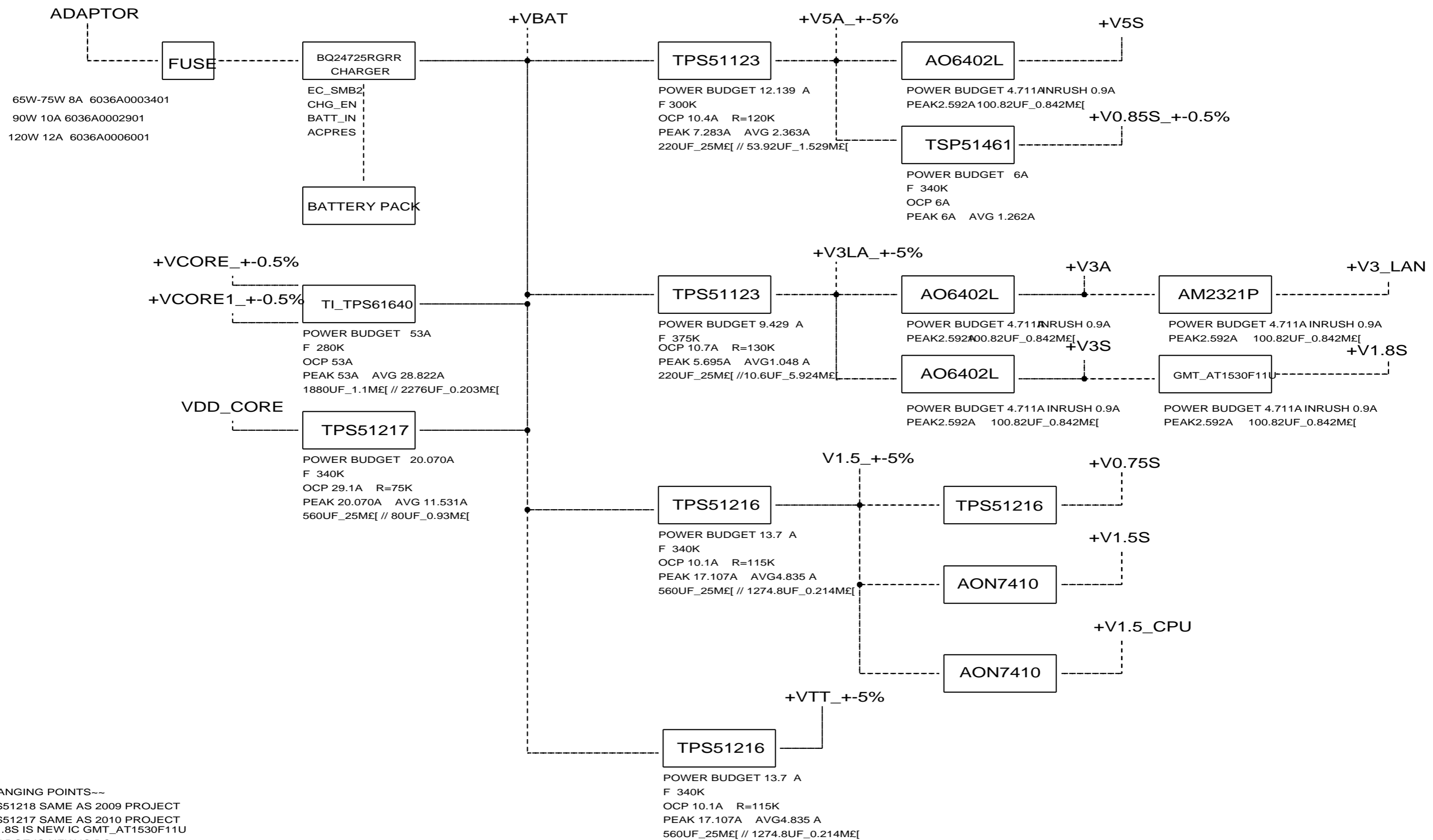
TOUCH PAD

SPI FLASH 8MB  
MXIC\_MX25L3206EM2I

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CHANGING POINTS--  
 TPS51218 SAME AS 2009 PROJECT  
 TPS51217 SAME AS 2010 PROJECT  
 +V1.8S IS NEW IC GMT\_AT1530F11U  
 CHARGE IS NEW IC BQ24725  
 VCC CORE IS NEW IC TPS51640  
 VTT IS NEW IC TPS51219  
 V0.85 IS NEW IC TPS 51641  
 V3\_V5 IS NEW IC TPS51123  
 POWER BUDGET --IC SPEC (MAX CURRENT)  
 PEAK CURRENT --RATIO OF INTERNAL PREDICTION  
 AVG CURRENT --TEST RESULT(MAX CURRENT)  
 INRUSH --L/S TURN NO

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FUSE6000  
 65W-75W 8A(6036A0003401)  
 90W 10A(6036A0002901)  
 120W 12A(6036A0006001)

D

C

B

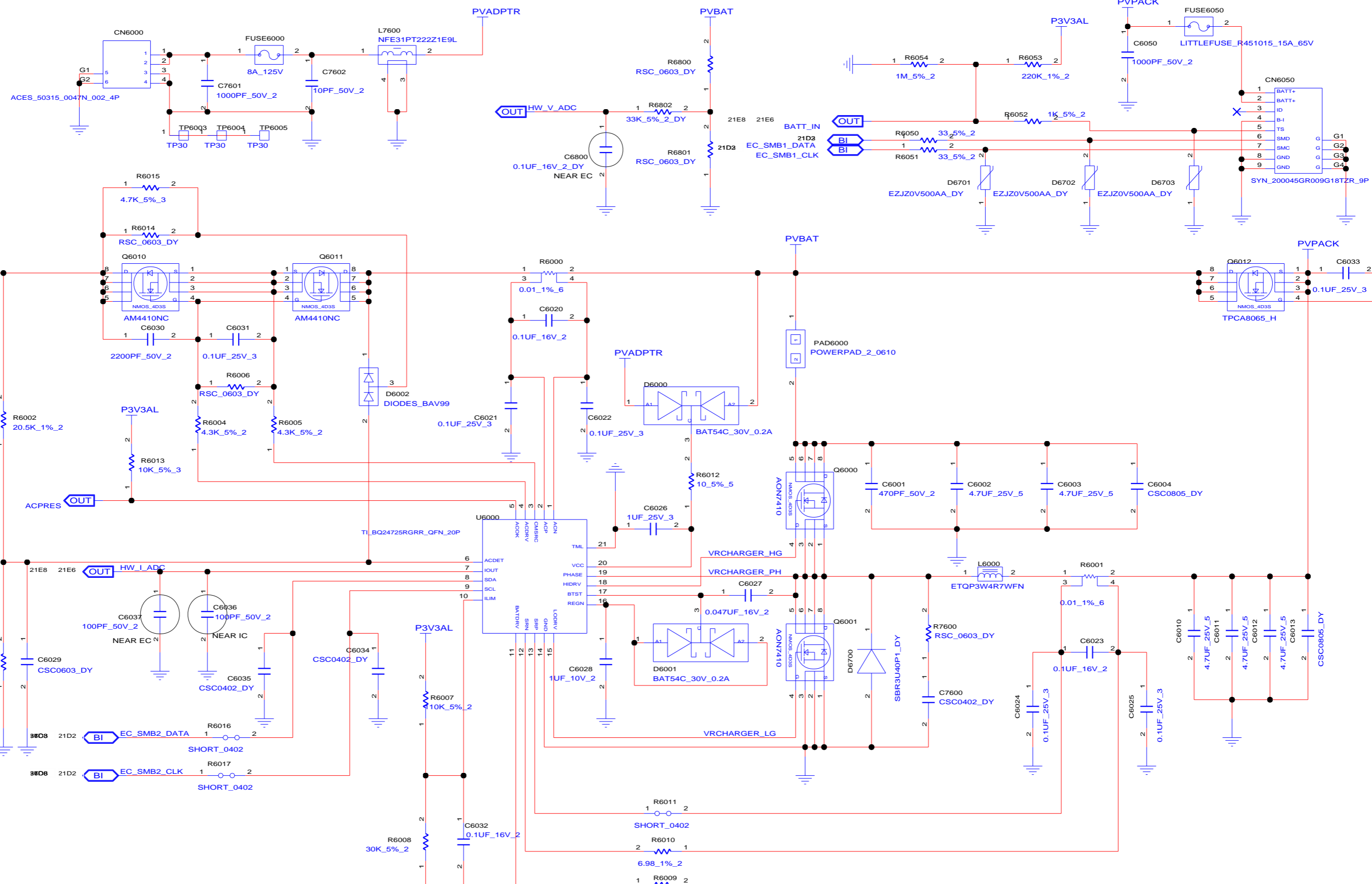
A

D

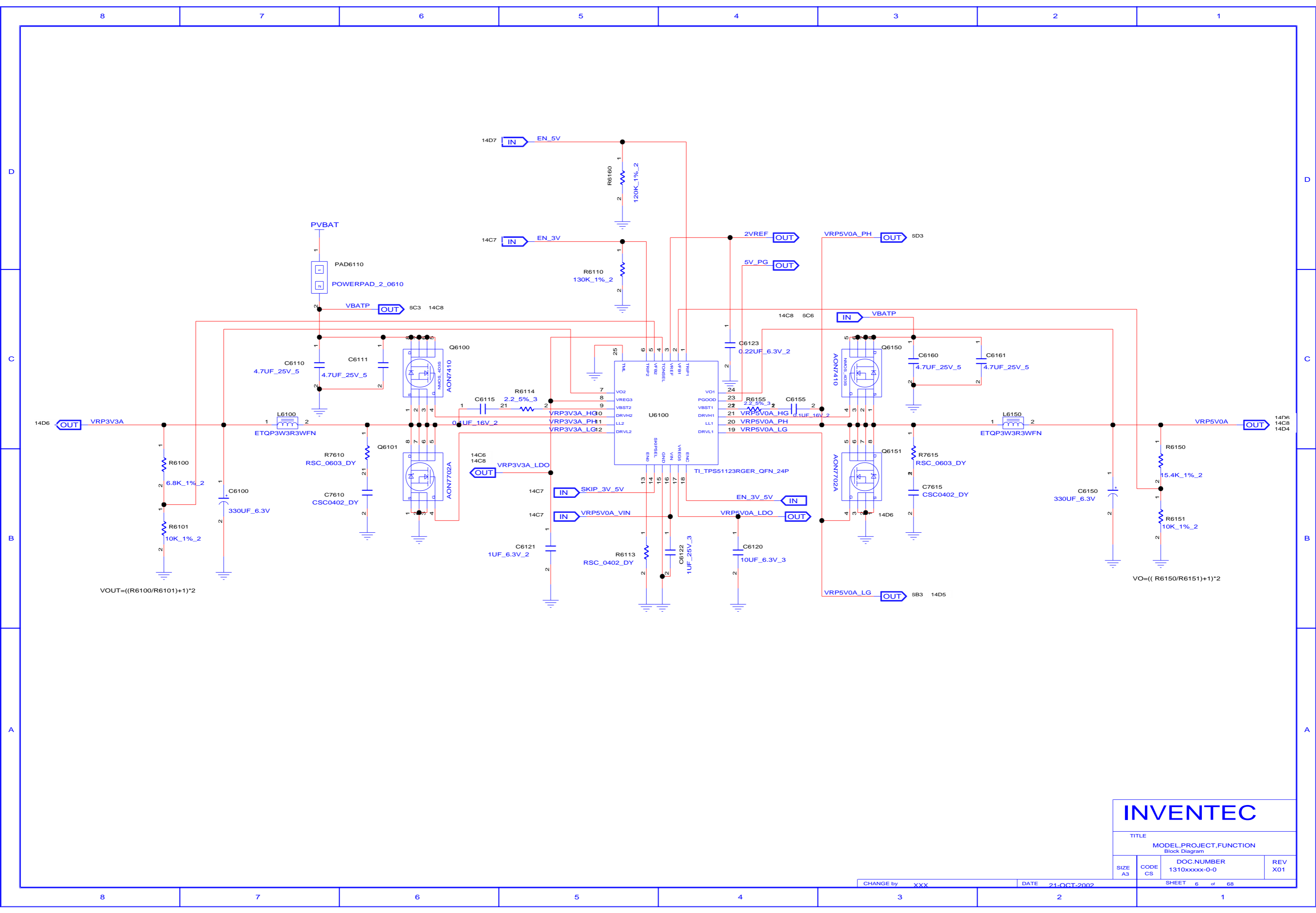
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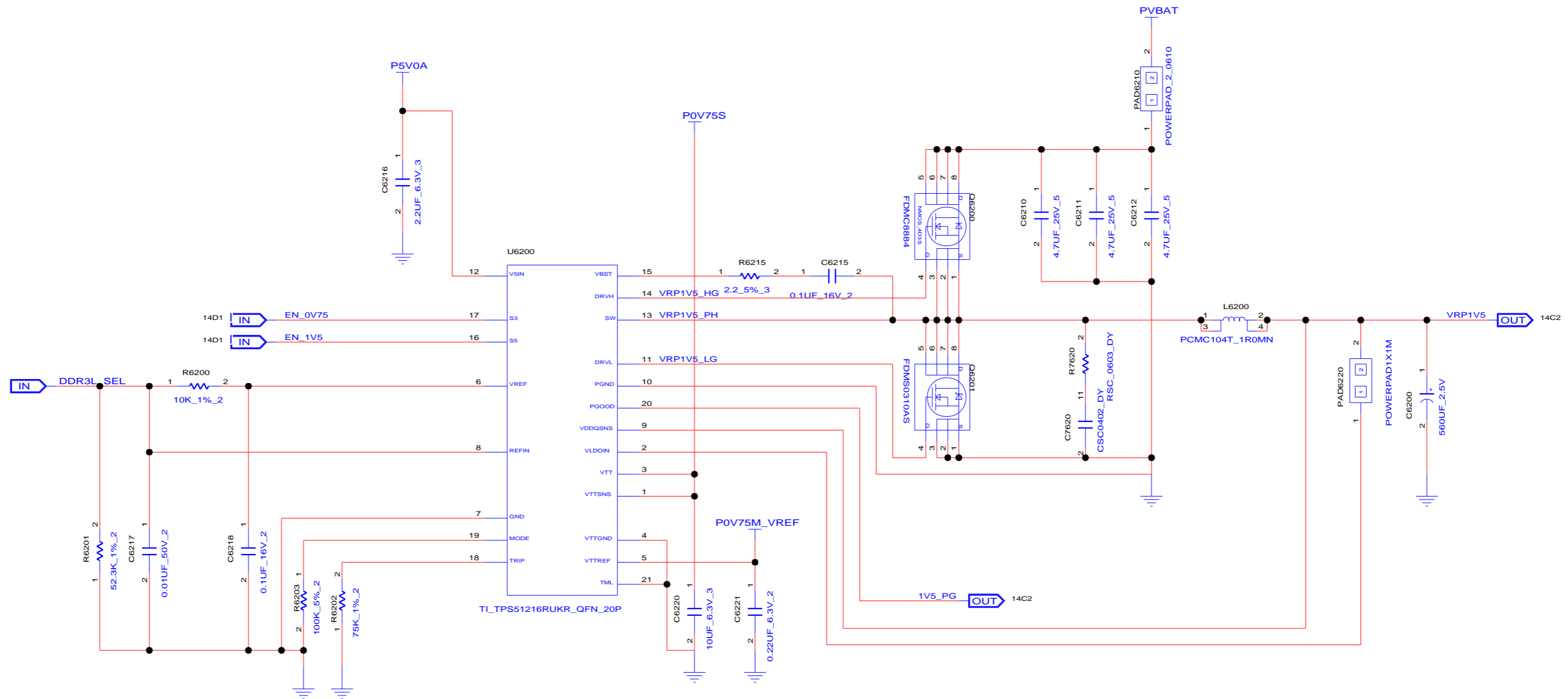
A



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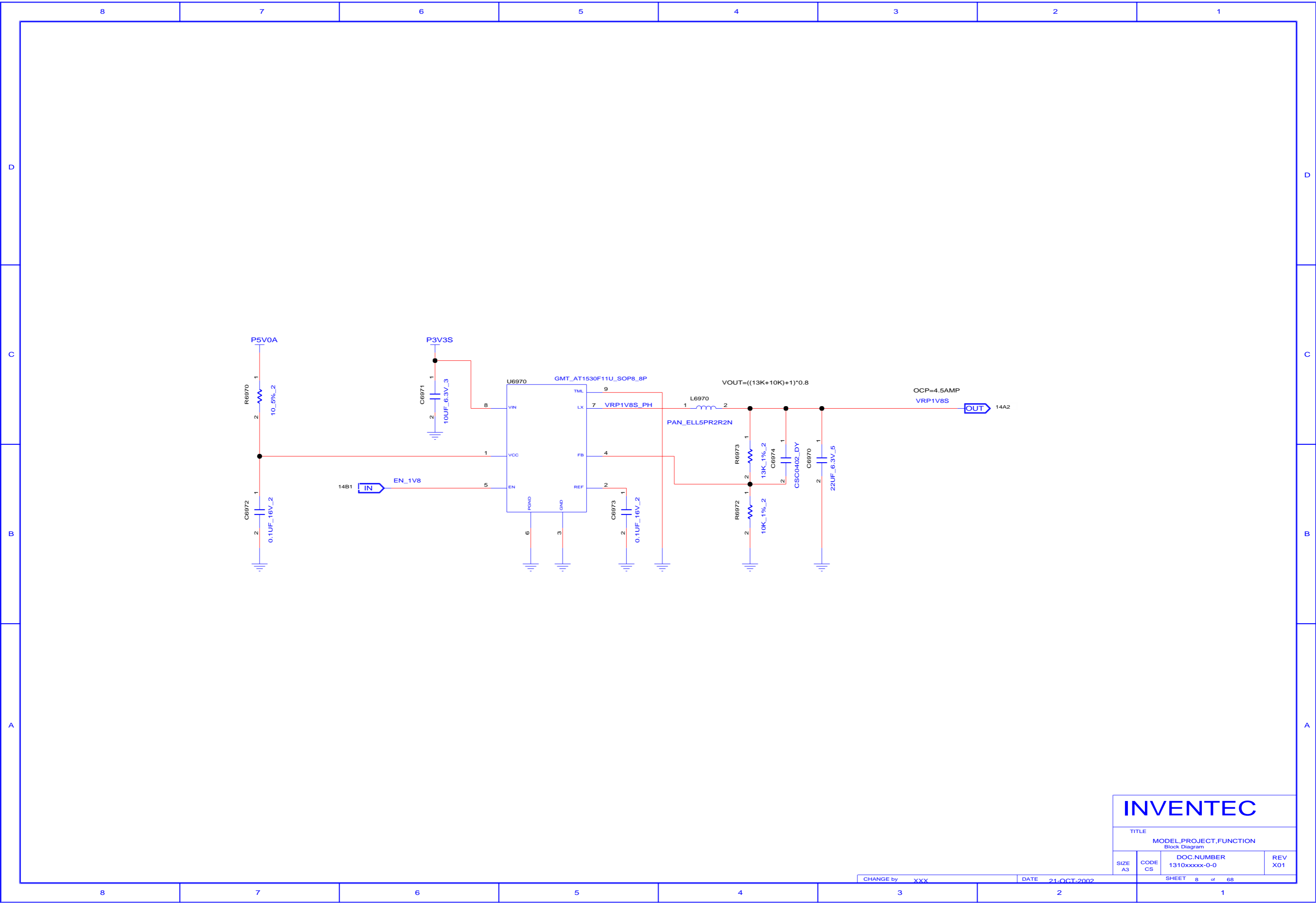


$$V_{OUT} = V_{REFIN} = 1.8 \cdot \frac{R_{6201}}{R_{6200} + R_{6201}}$$
 MODE=100KOHM:TRACKING DISCHARGE

STATE	S3	S5	VREF	VDDQ	VTTREF	VTT
S0	HI	HI	ON	ON	ON	ON
S3	LO	HI	ON	ON	ON	OFF(High-Z)
S4/S5	LO	LO	OFF	OFF(Discharge)	OFF(Discharge)	OFF(Discharge)

# INVENTEC

TITLE			
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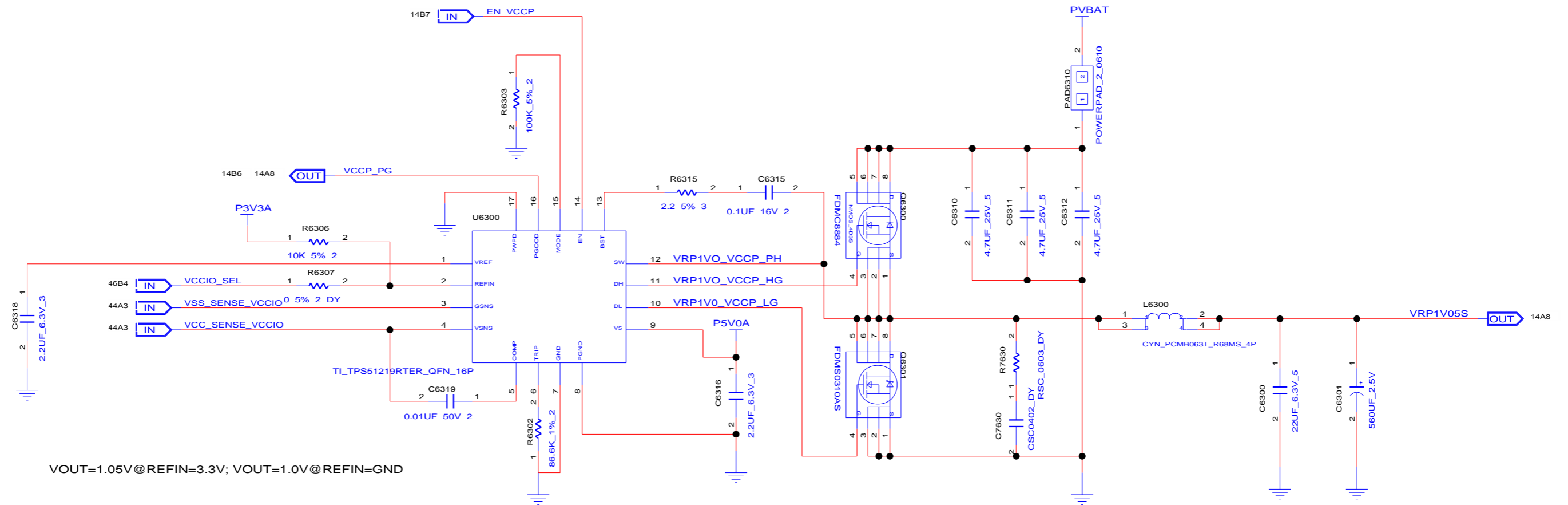
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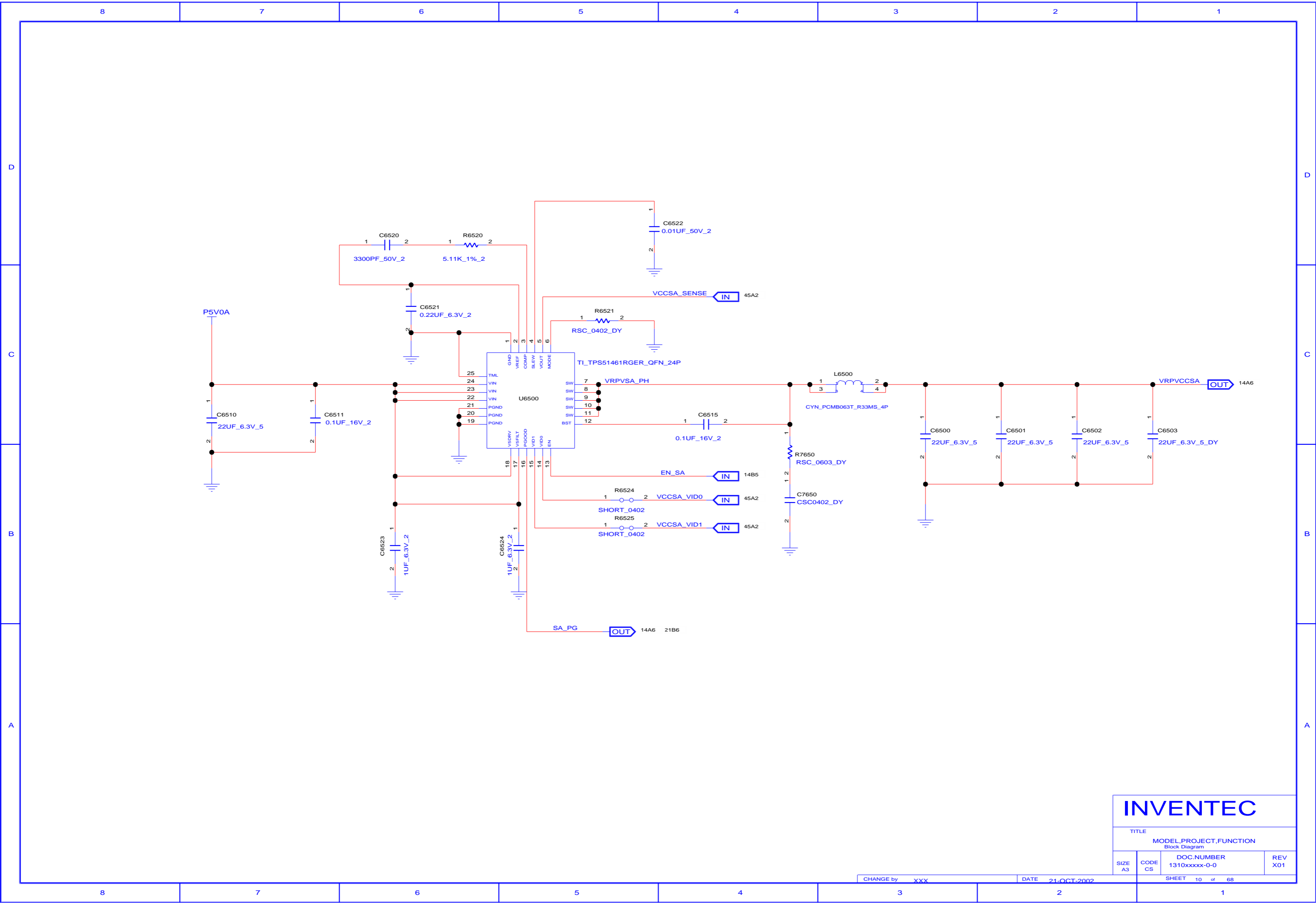
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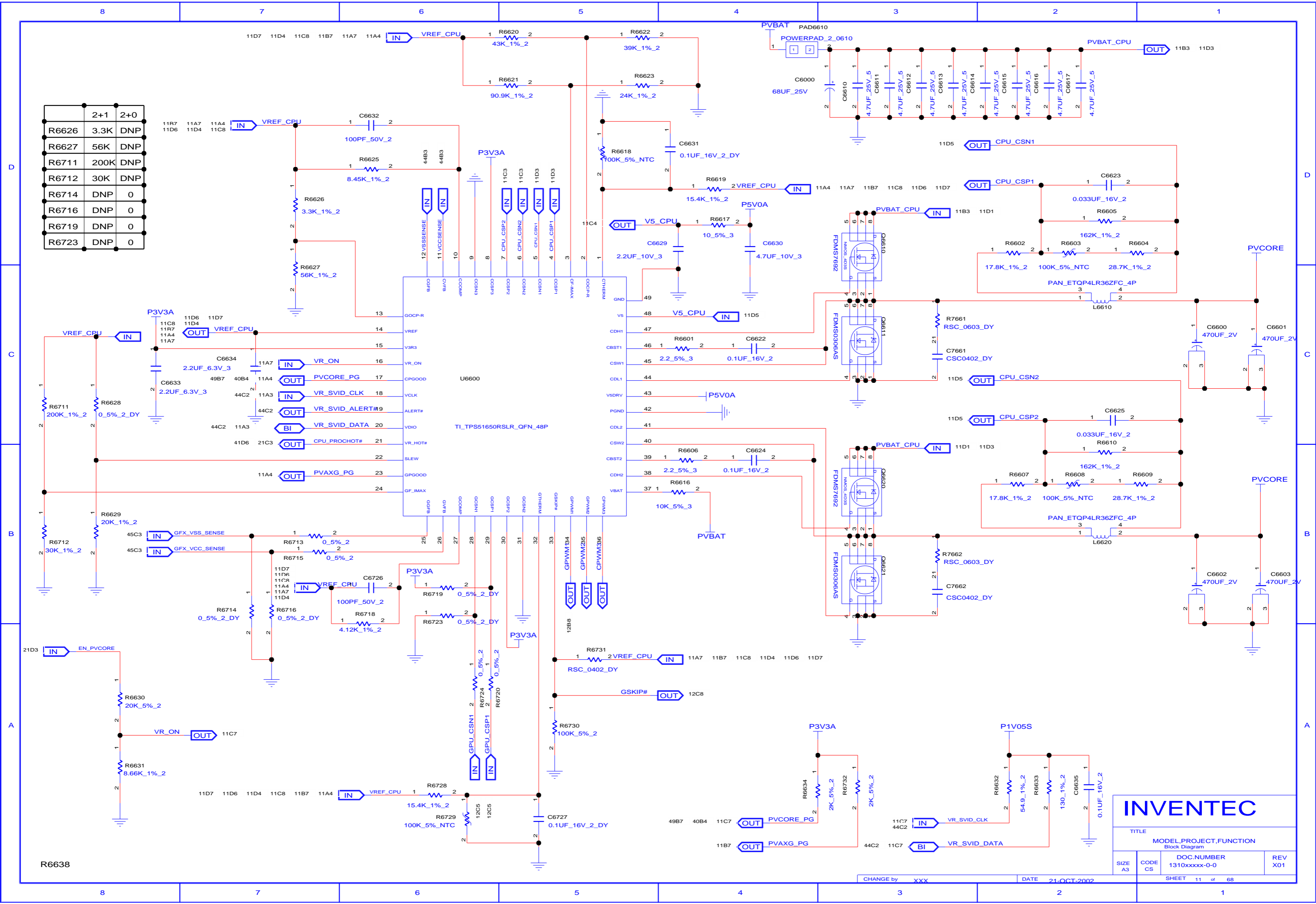
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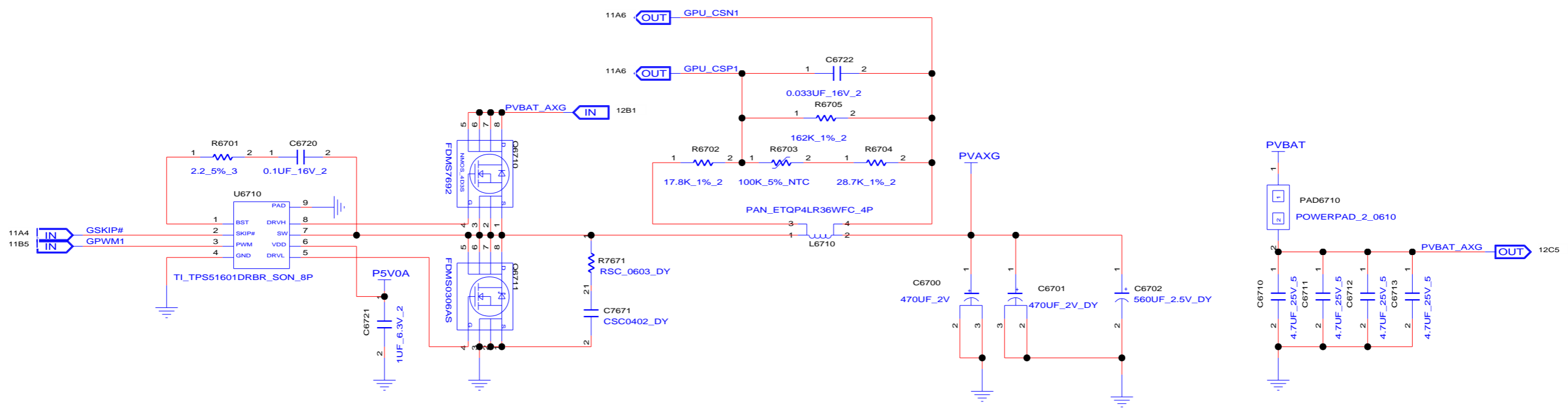
	2+1	2+0
R6626	3.3K	DNP
R6627	56K	DNP
R6711	200K	DNP
R6712	30K	DNP
R6714	DNP	0
R6716	DNP	0
R6719	DNP	0
R6723	DNP	0



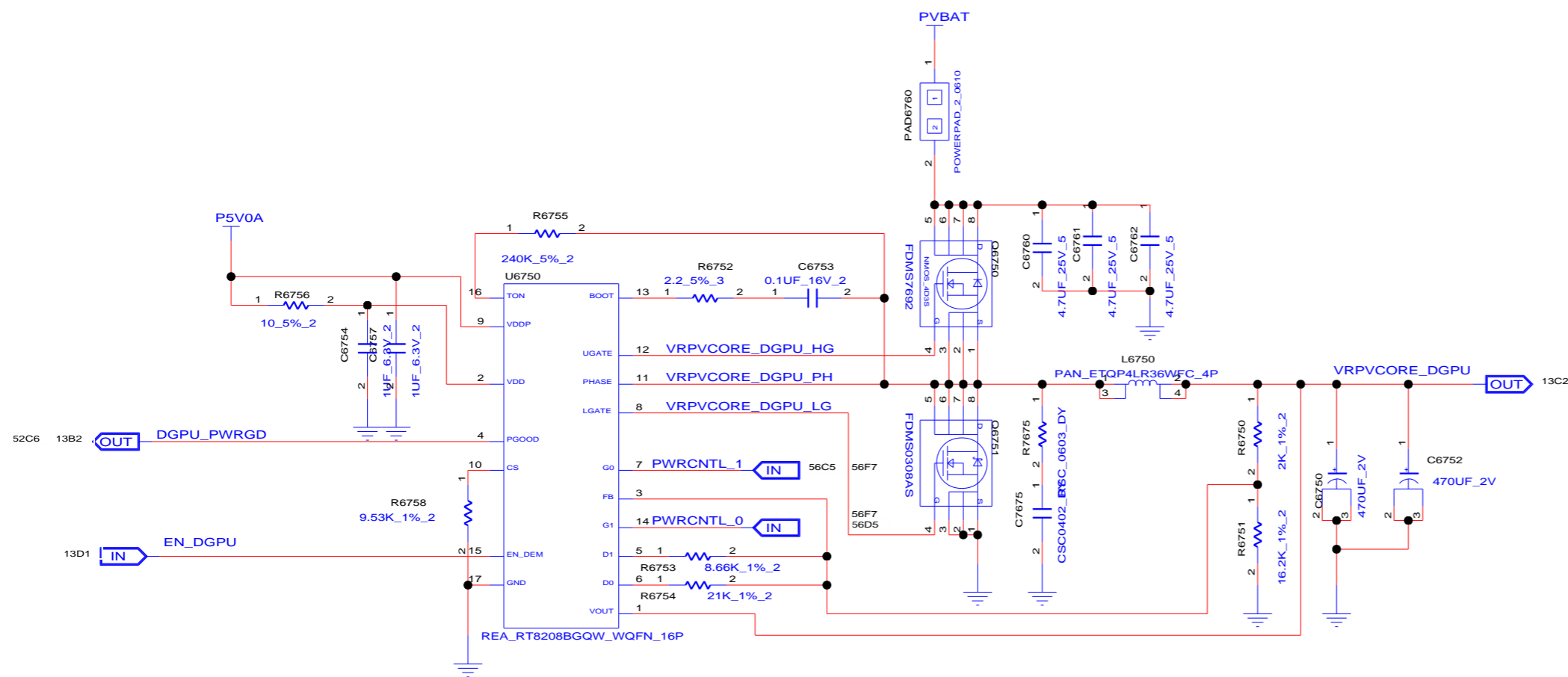
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R6638

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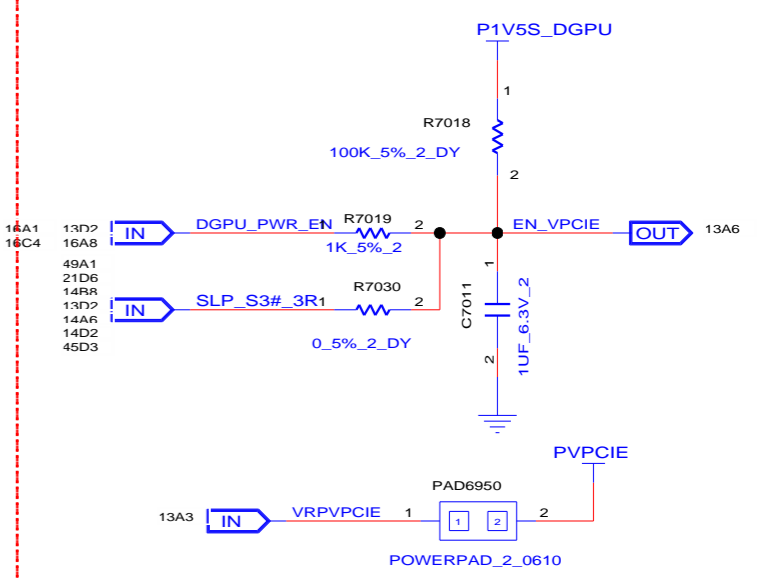
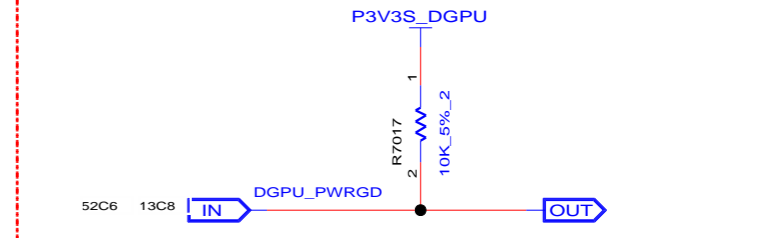
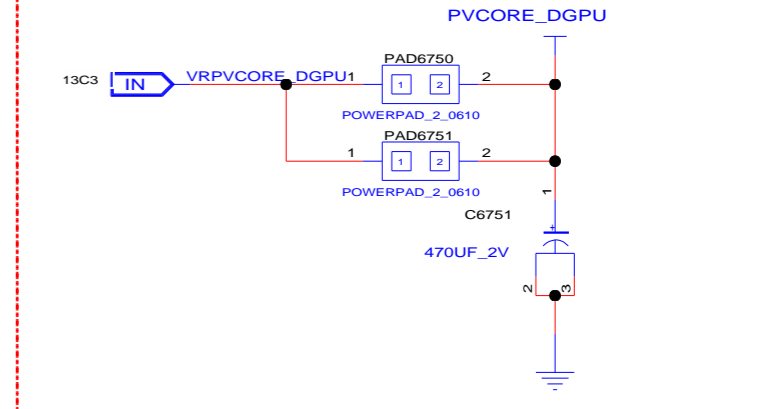
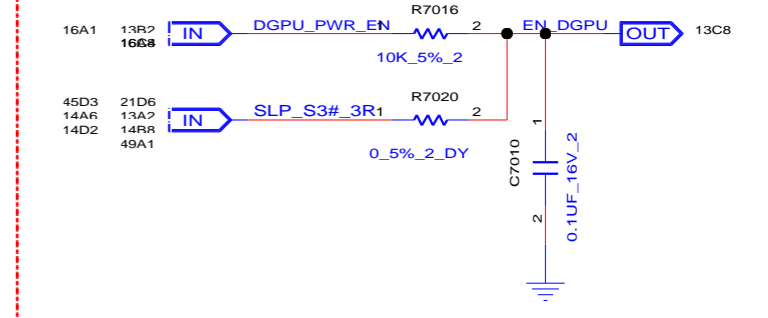
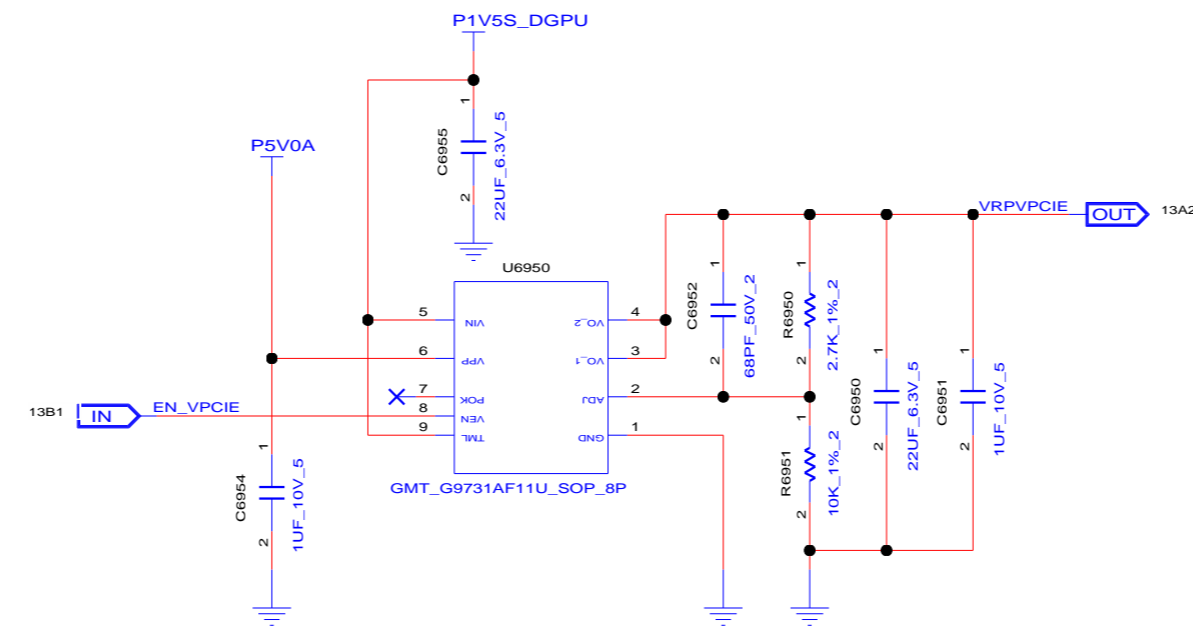


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P.S. R6750(R1) R6751(R2) R6753(R3) R6754(R4)

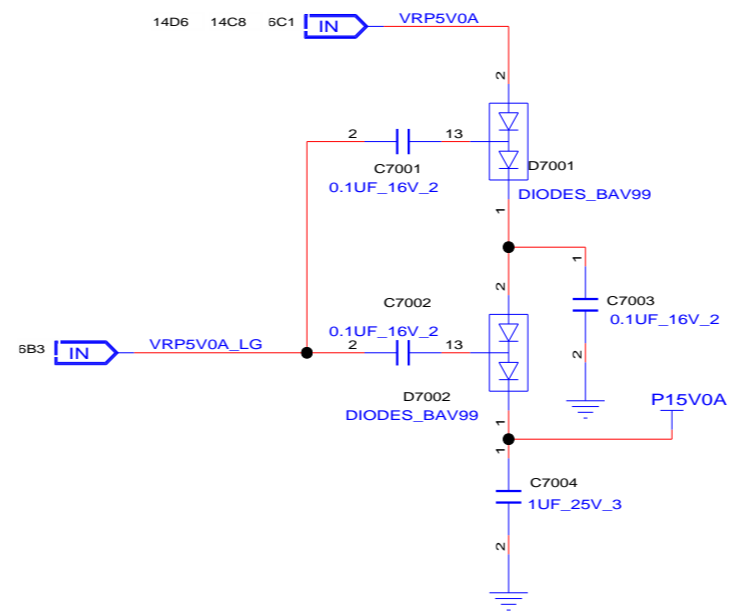
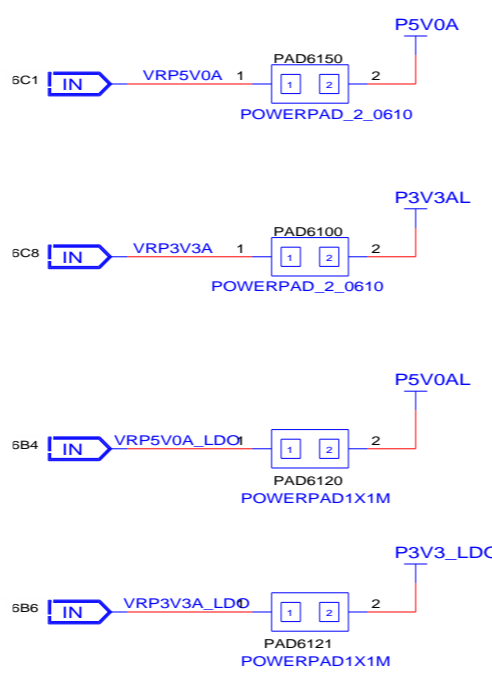
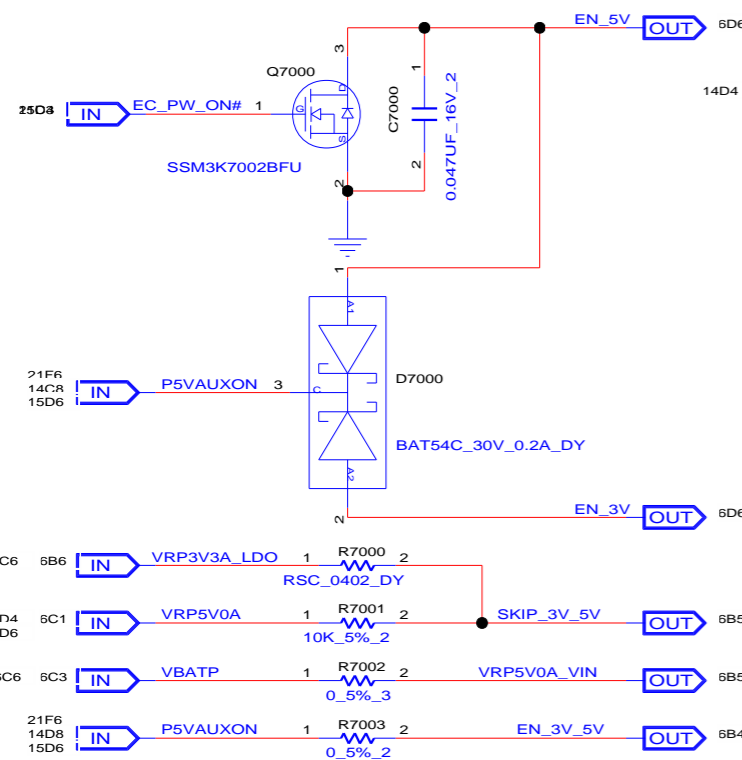
RT8208A	RT8208B	Output Voltage Equation		
G0	G1	G0	G1	
0	0	1	1	$V_{OUT} = \frac{R1+R2}{R2} \times 0.75$
1	0	0	1	$V_{OUT} = \frac{R1+(R2//R3)}{(R2//R3)} \times 0.75$
0	1	1	0	$V_{OUT} = \frac{R1+(R2//R4)}{(R2//R4)} \times 0.75$
1	1	0	0	$V_{OUT} = \frac{R1+(R2//R3//R4)}{(R2//R3//R4)} \times 0.75$



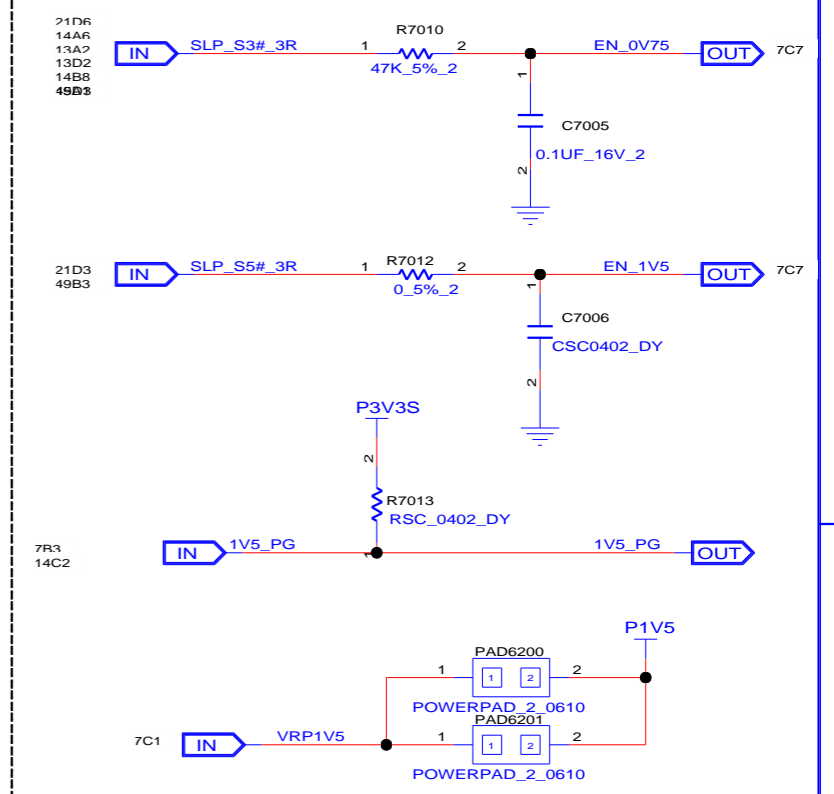
**INVENTEC**

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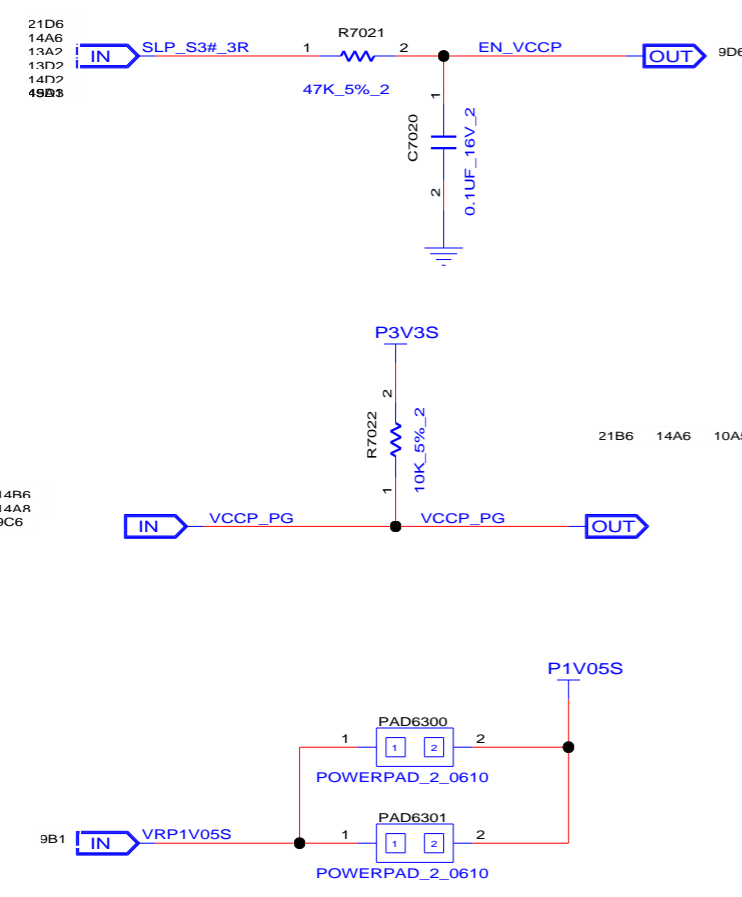
### 3V & 5V



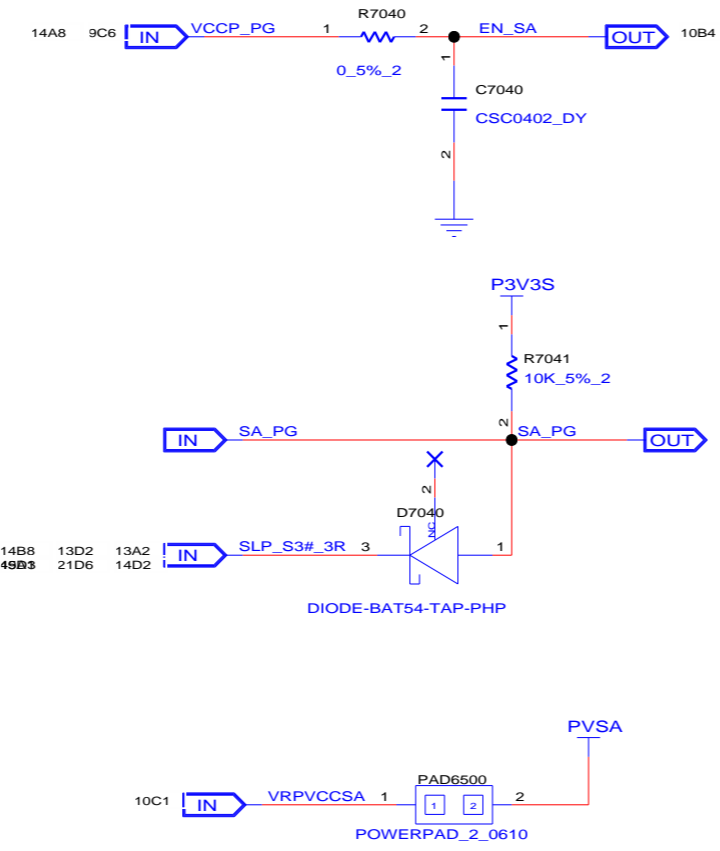
### DDR\_P1V5



### VCCIO



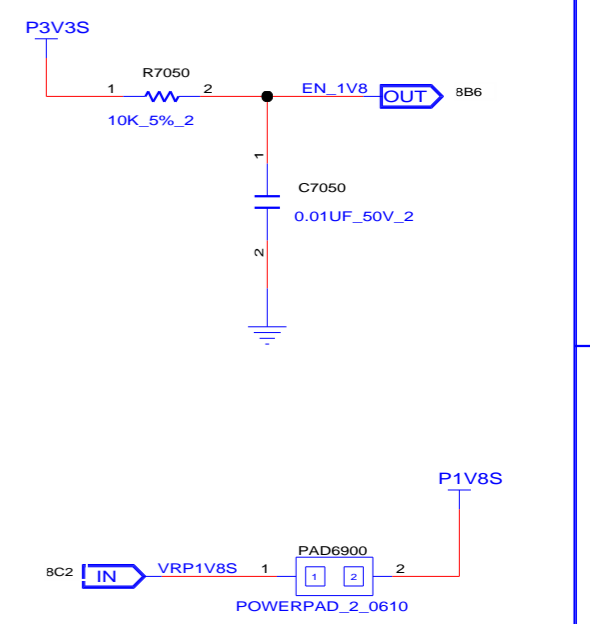
### VCCSA



### DGPU

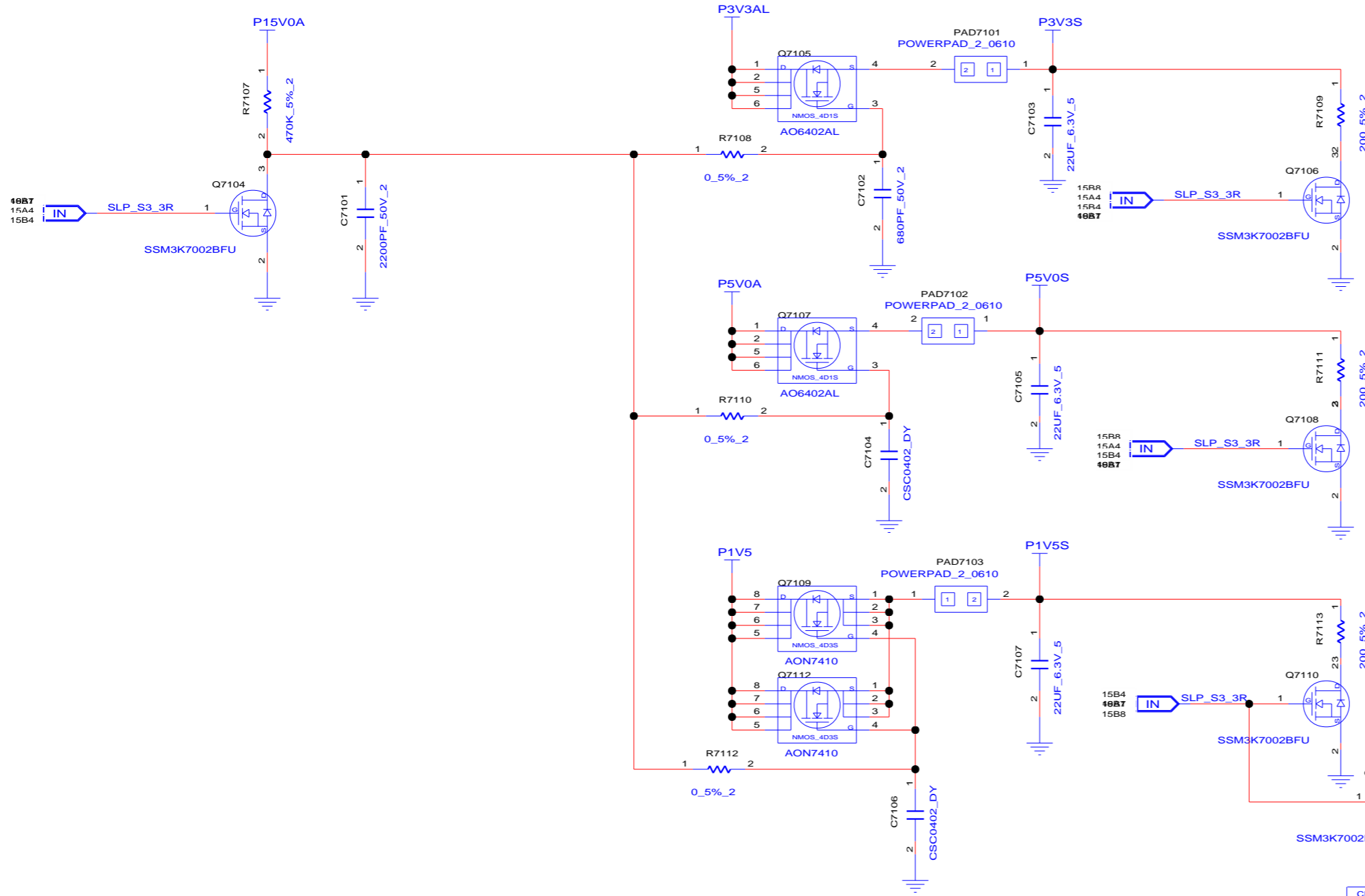
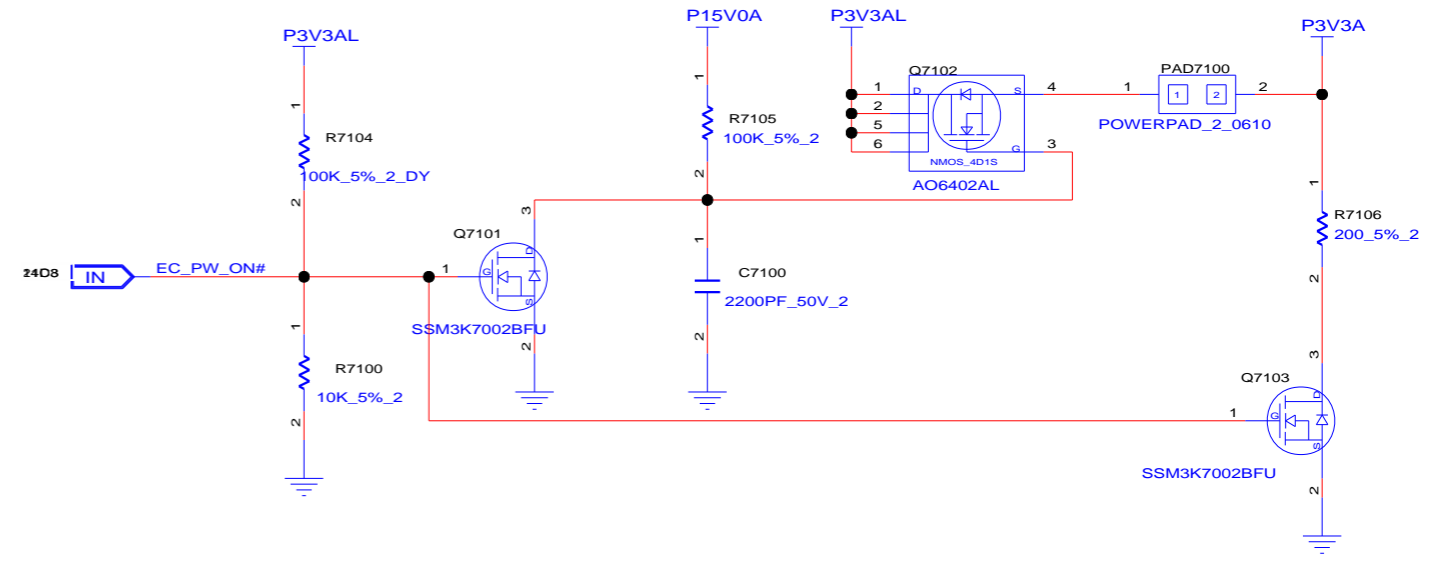
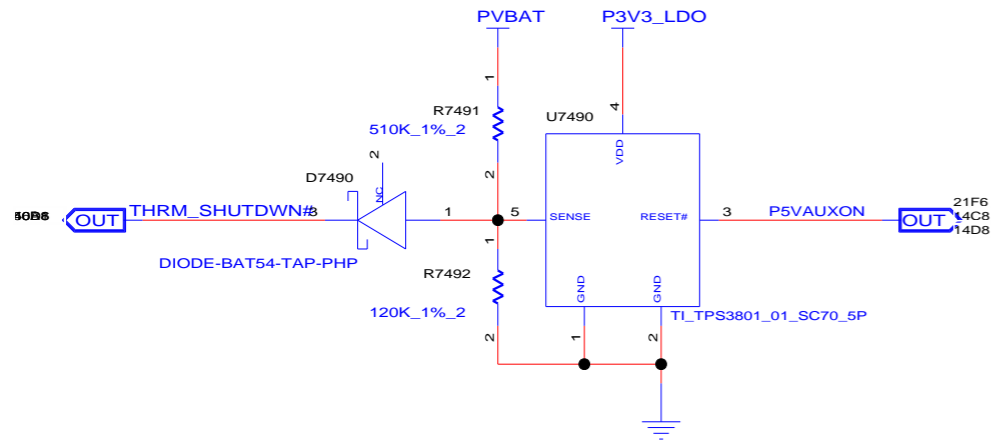


### P1V8S

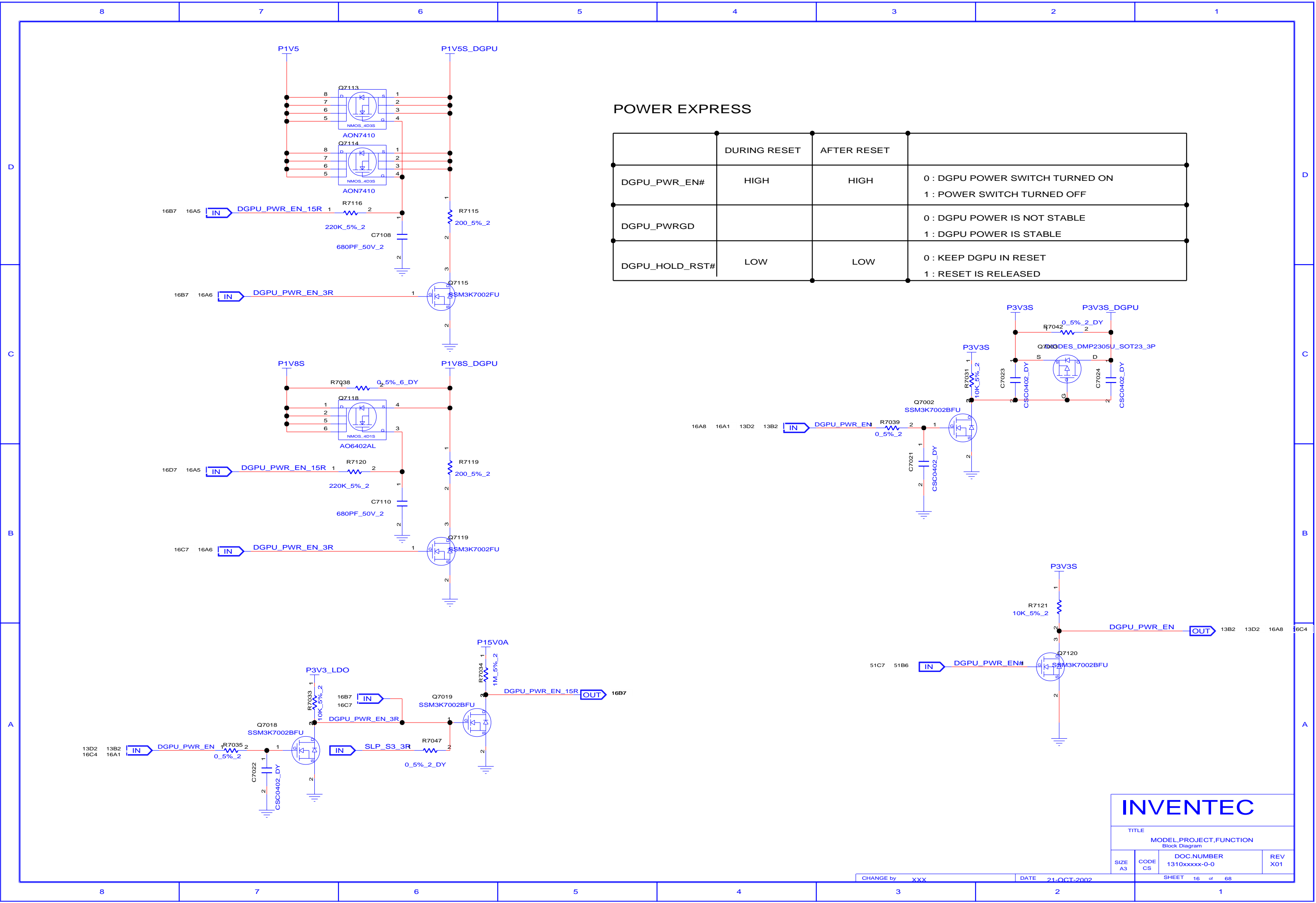


**INVENTEC**

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**POWER EXPRESS**

	DURING RESET	AFTER RESET	
DGPU_PWR_EN#	HIGH	HIGH	0 : DGPU POWER SWITCH TURNED ON 1 : POWER SWITCH TURNED OFF
DGPU_PWRGD			0 : DGPU POWER IS NOT STABLE 1 : DGPU POWER IS STABLE
DGPU_HOLD_RST#	LOW	LOW	0 : KEEP DGPU IN RESET 1 : RESET IS RELEASED

**INVENTEC**

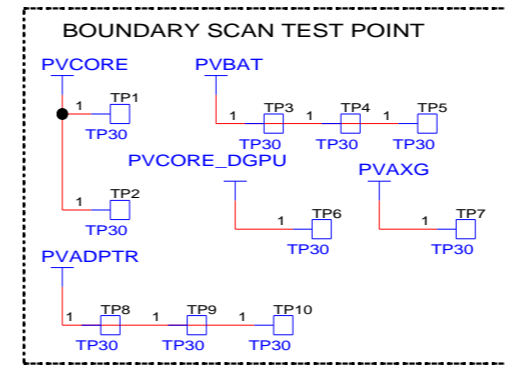
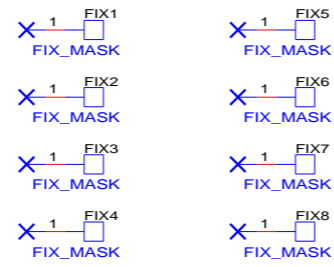
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REFERENCE 0~49(PCB SCREW)



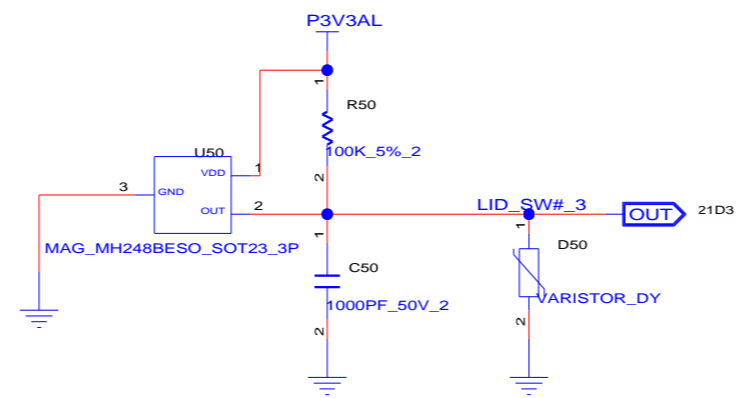
**INVENTEC**

TITLE  
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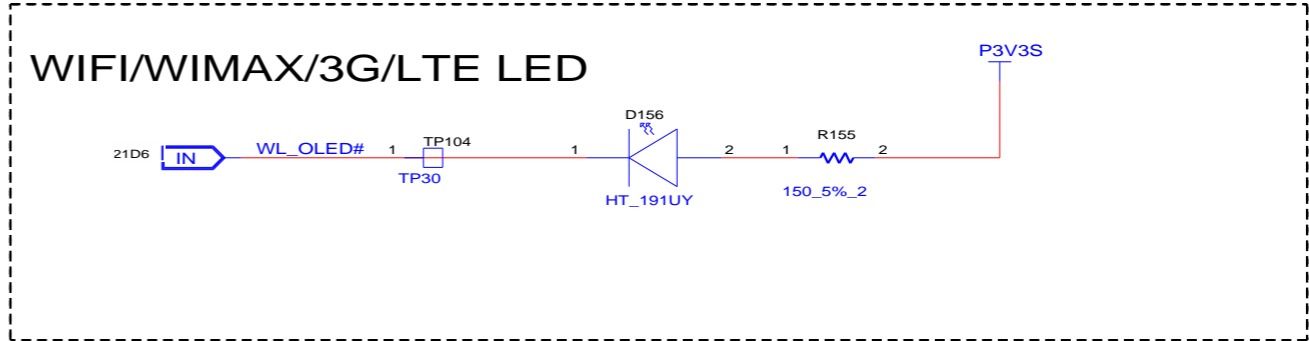
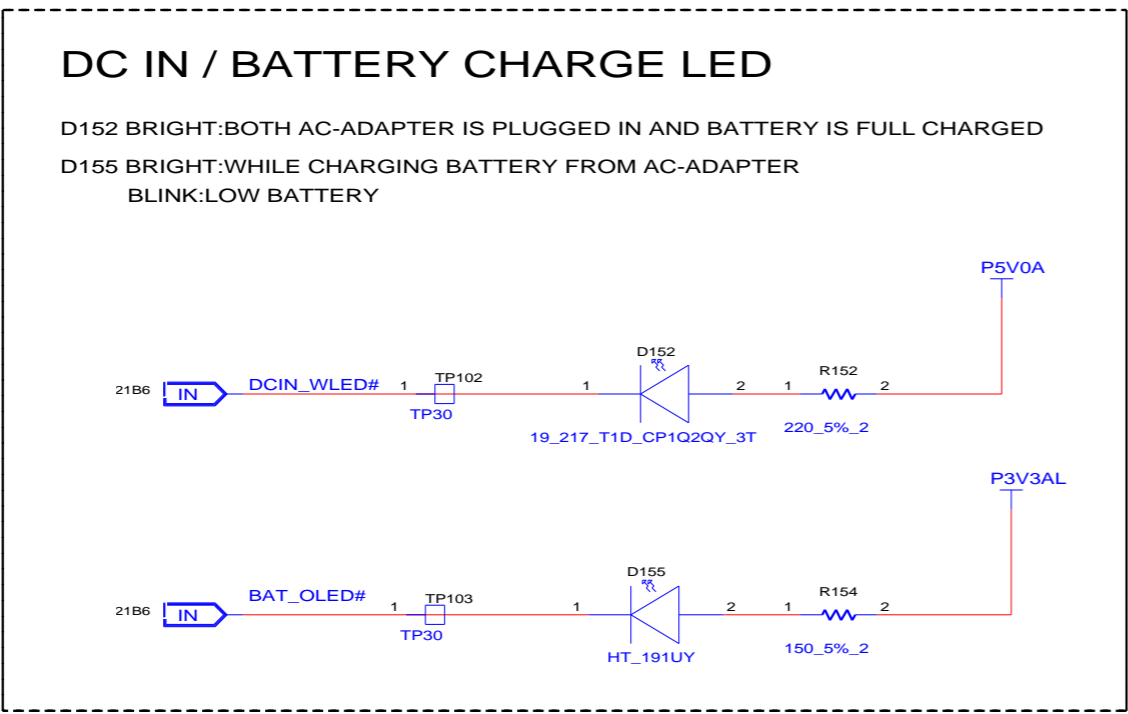
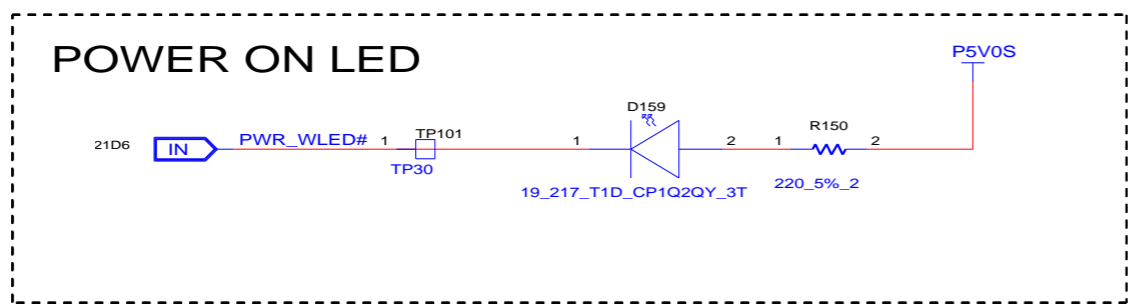
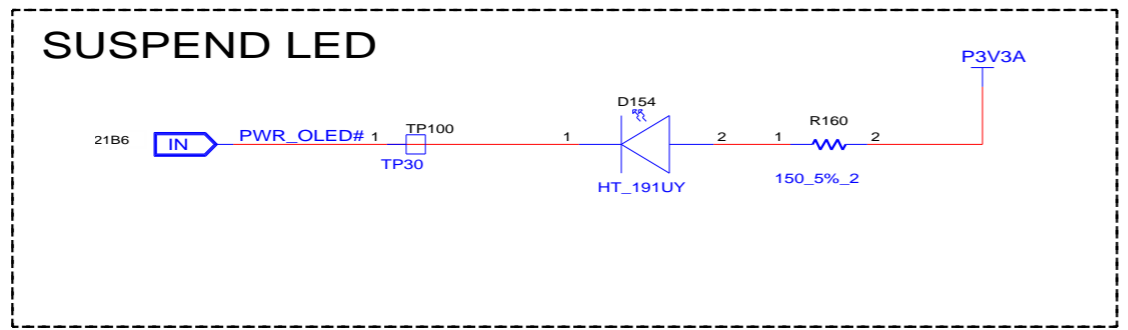
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REFERENCE 50-99(HALL SENSOR)



<b>INVENTEC</b>			
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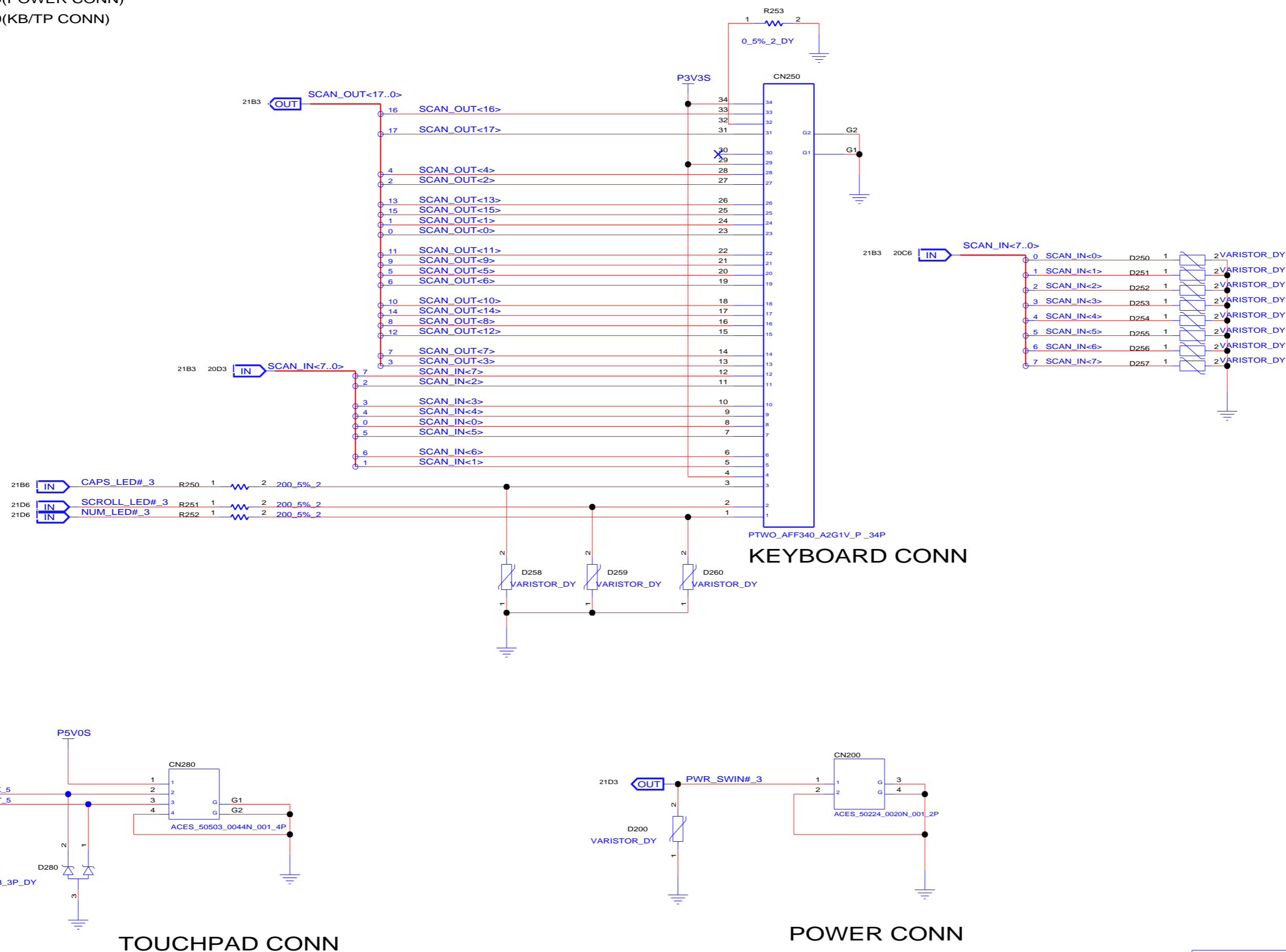
REFERENCE 100~199(LED)



<b>INVENTEC</b>			
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REFERENCE 200~249(POWER CONN)

REFERENCE 250~299(KB/TP CONN)



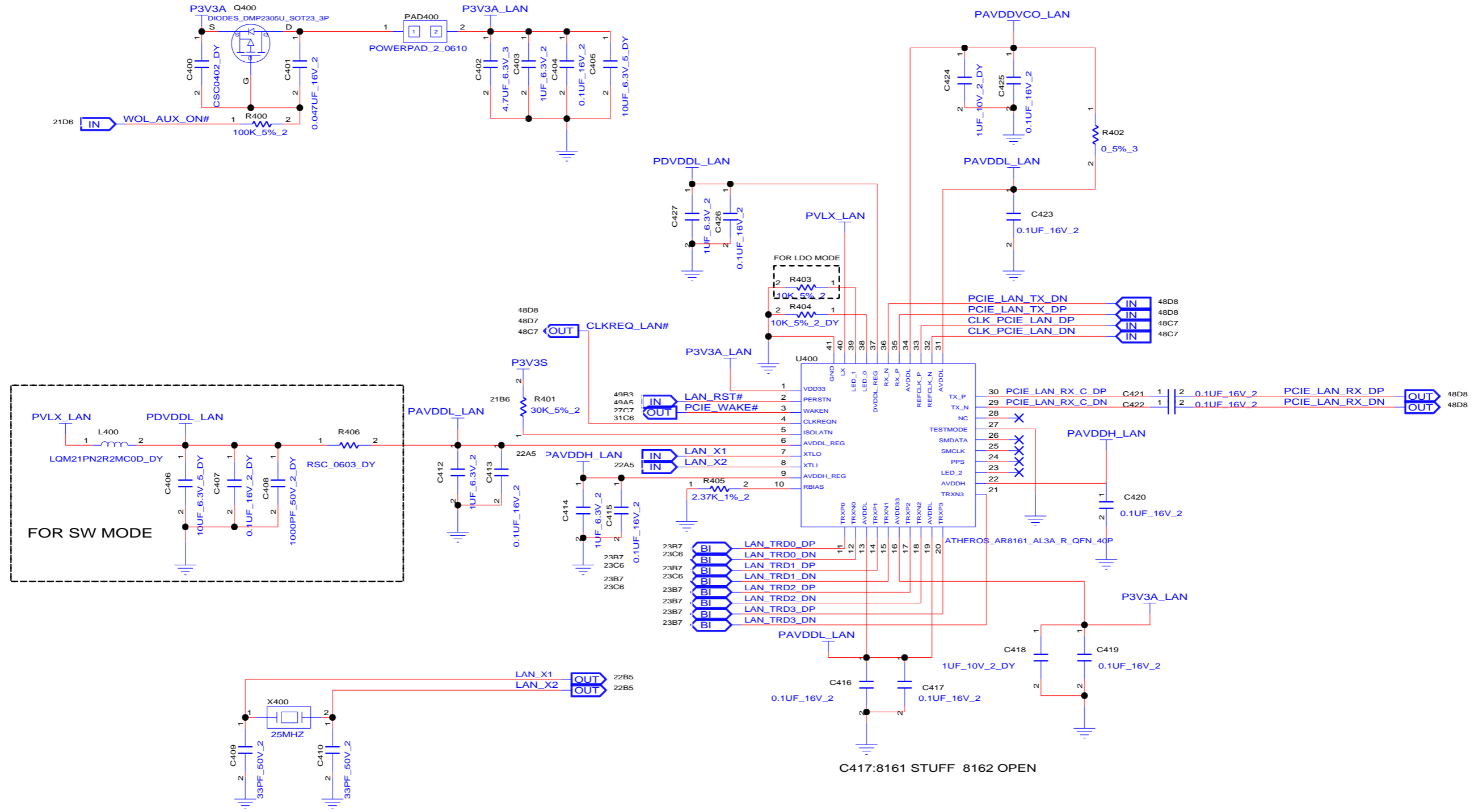
KEYBOARD CONN

TOUCHPAD CONN

POWER CONN

<b>INVENTEC</b>			
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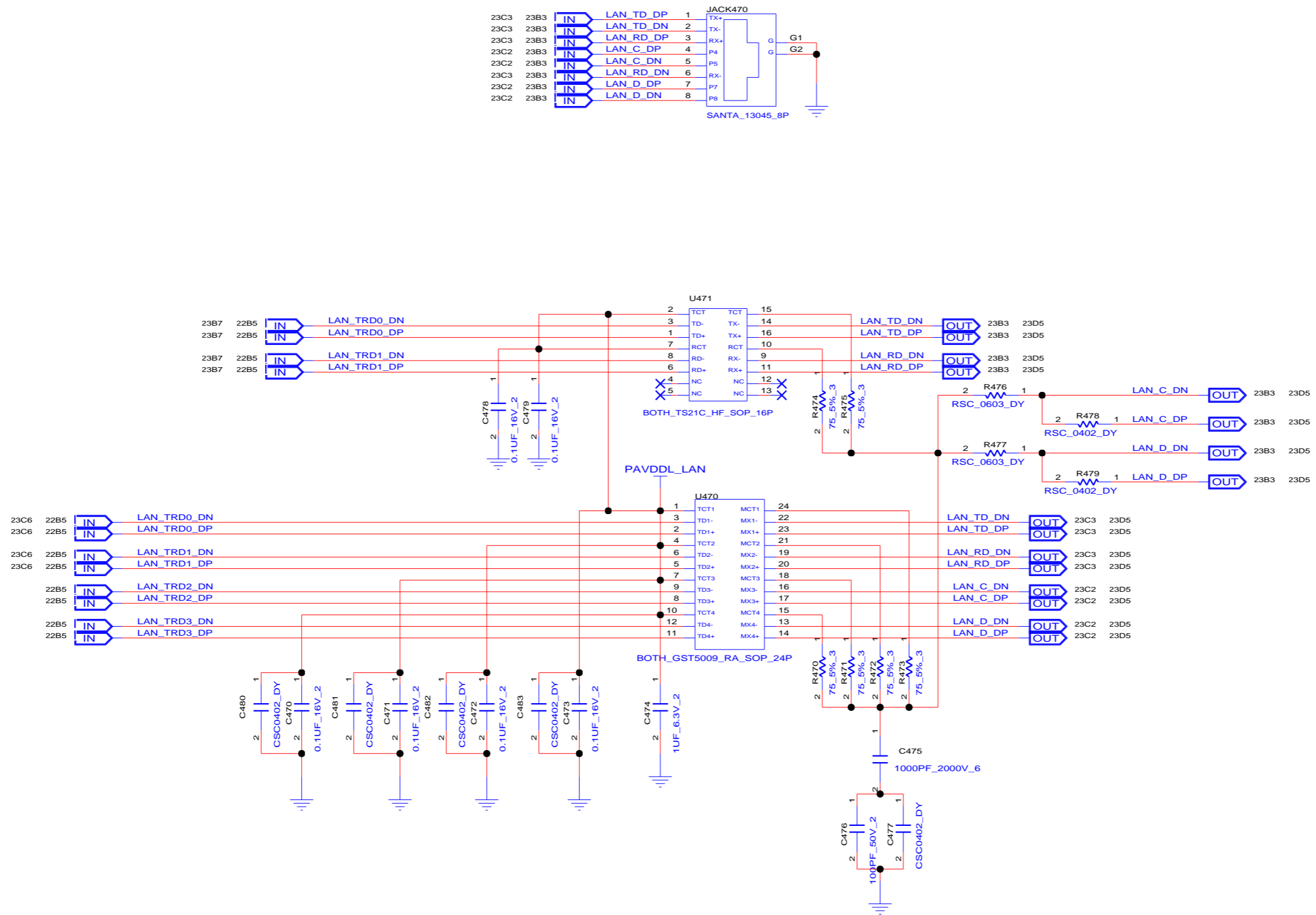




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REFERENCE 400~499(LAN)



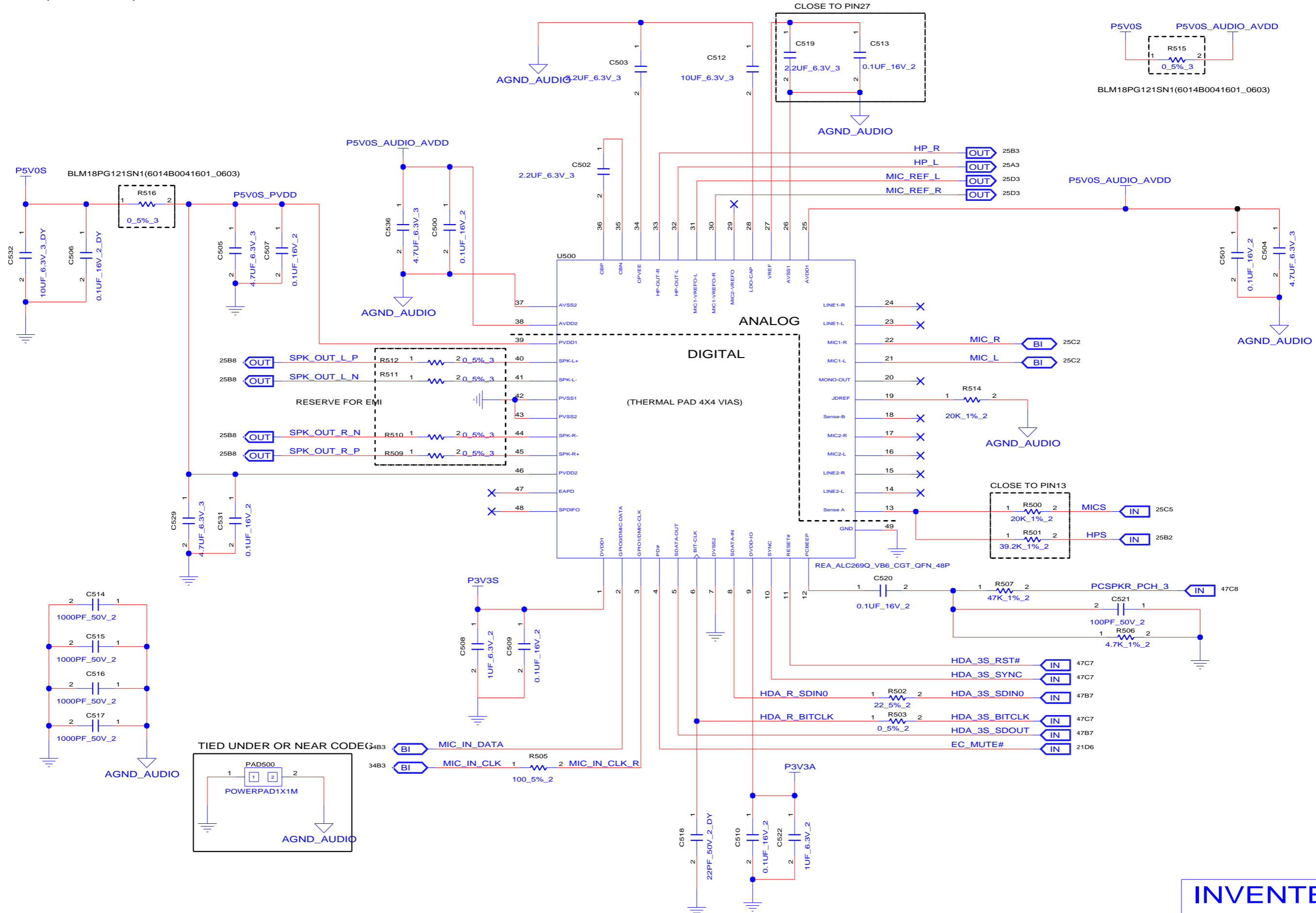
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REFERENCE 500~549(AUDIO CODEC)

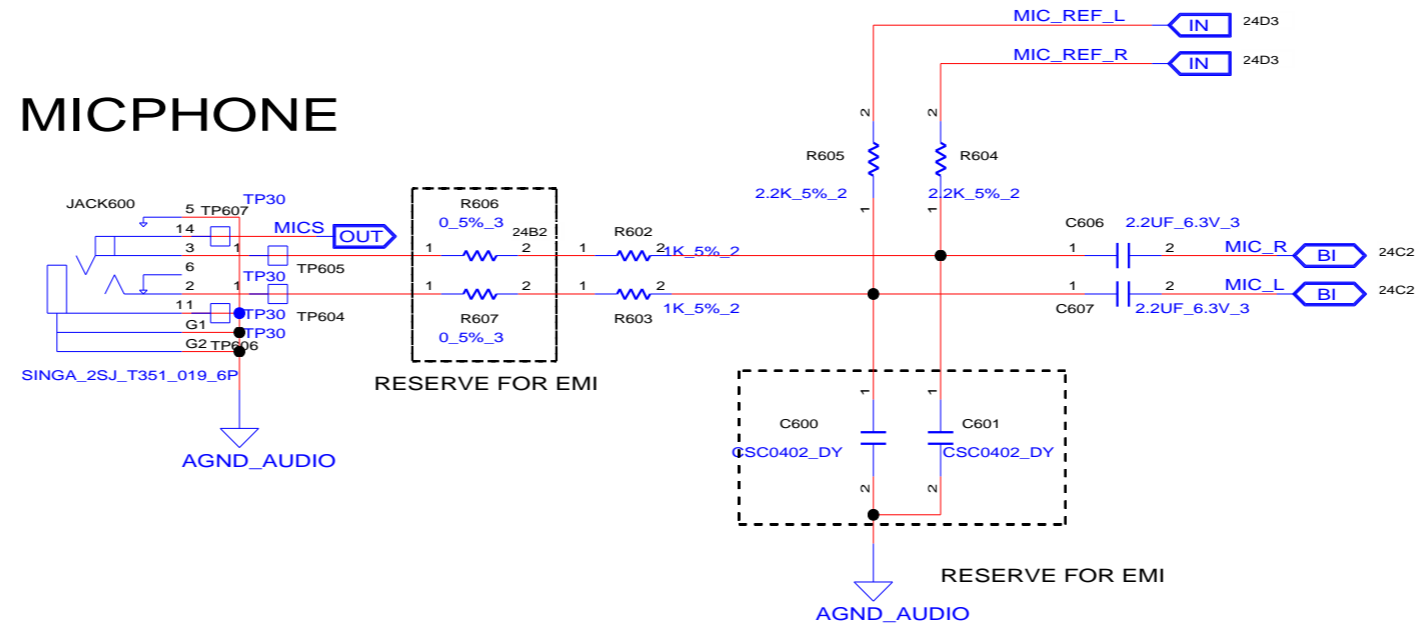


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TITLE			
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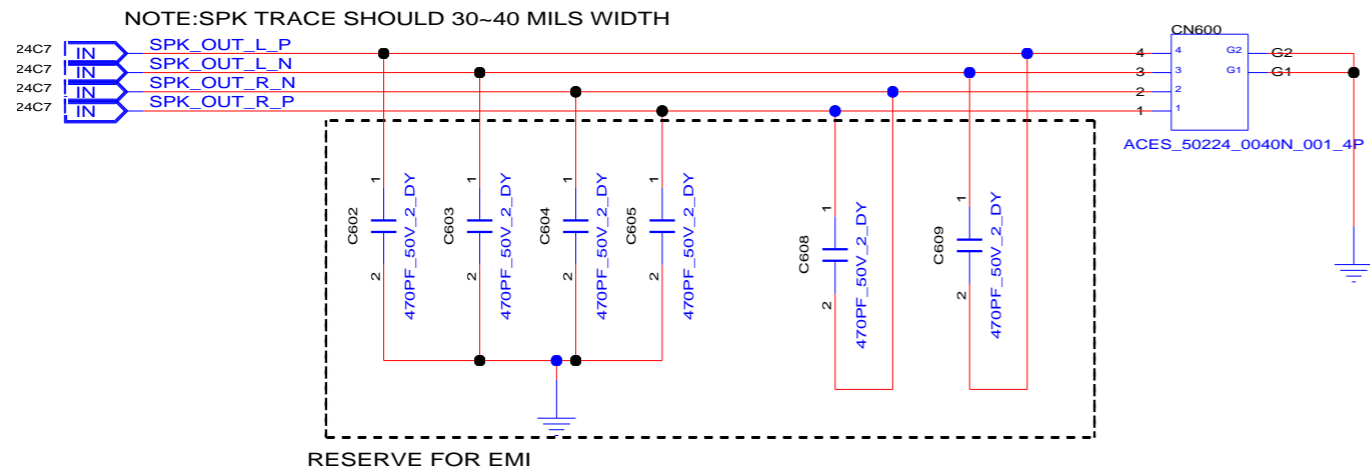


# AUDIO JACKS

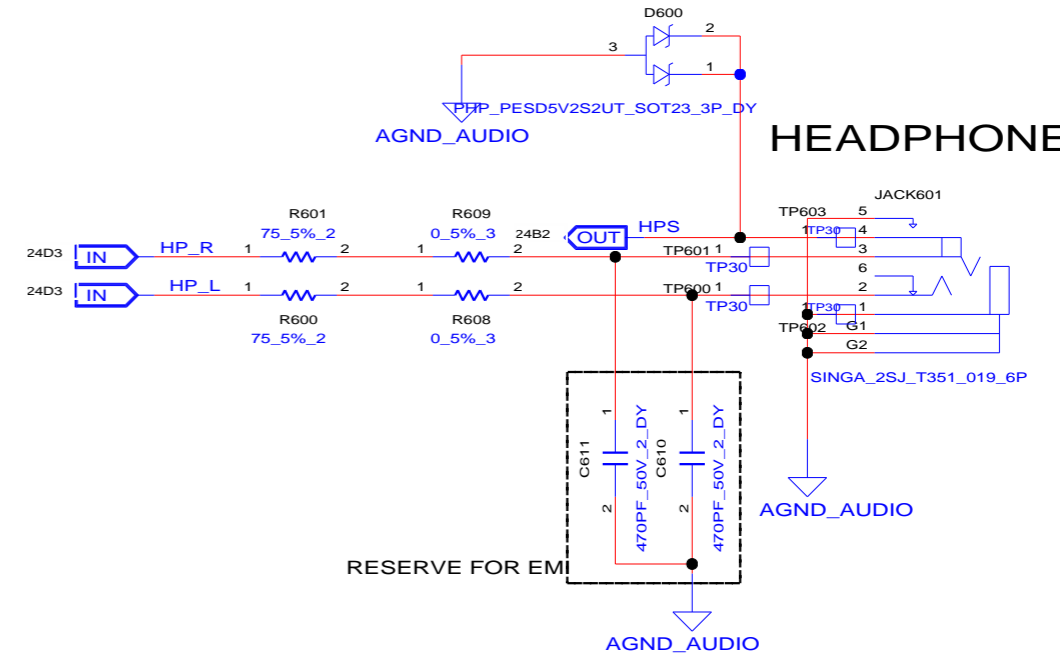
## MICPHONE



## INTERNAL SPEAKERS



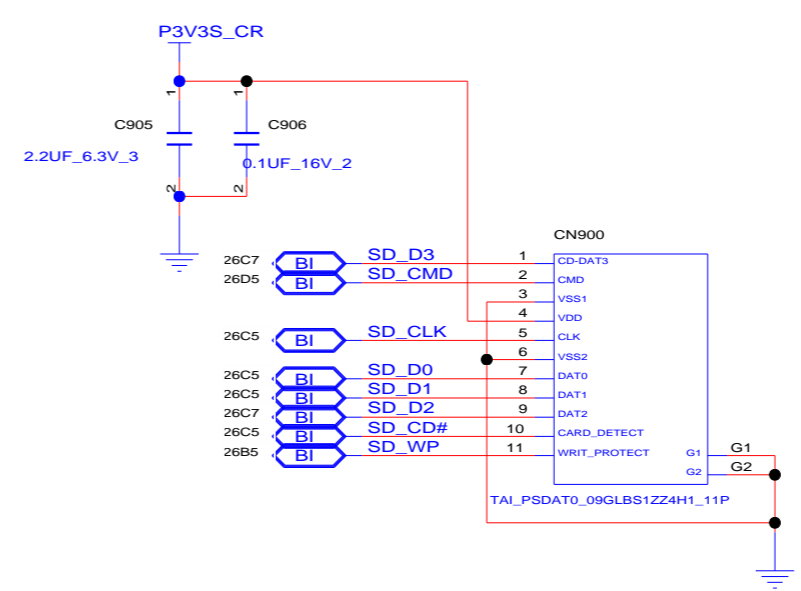
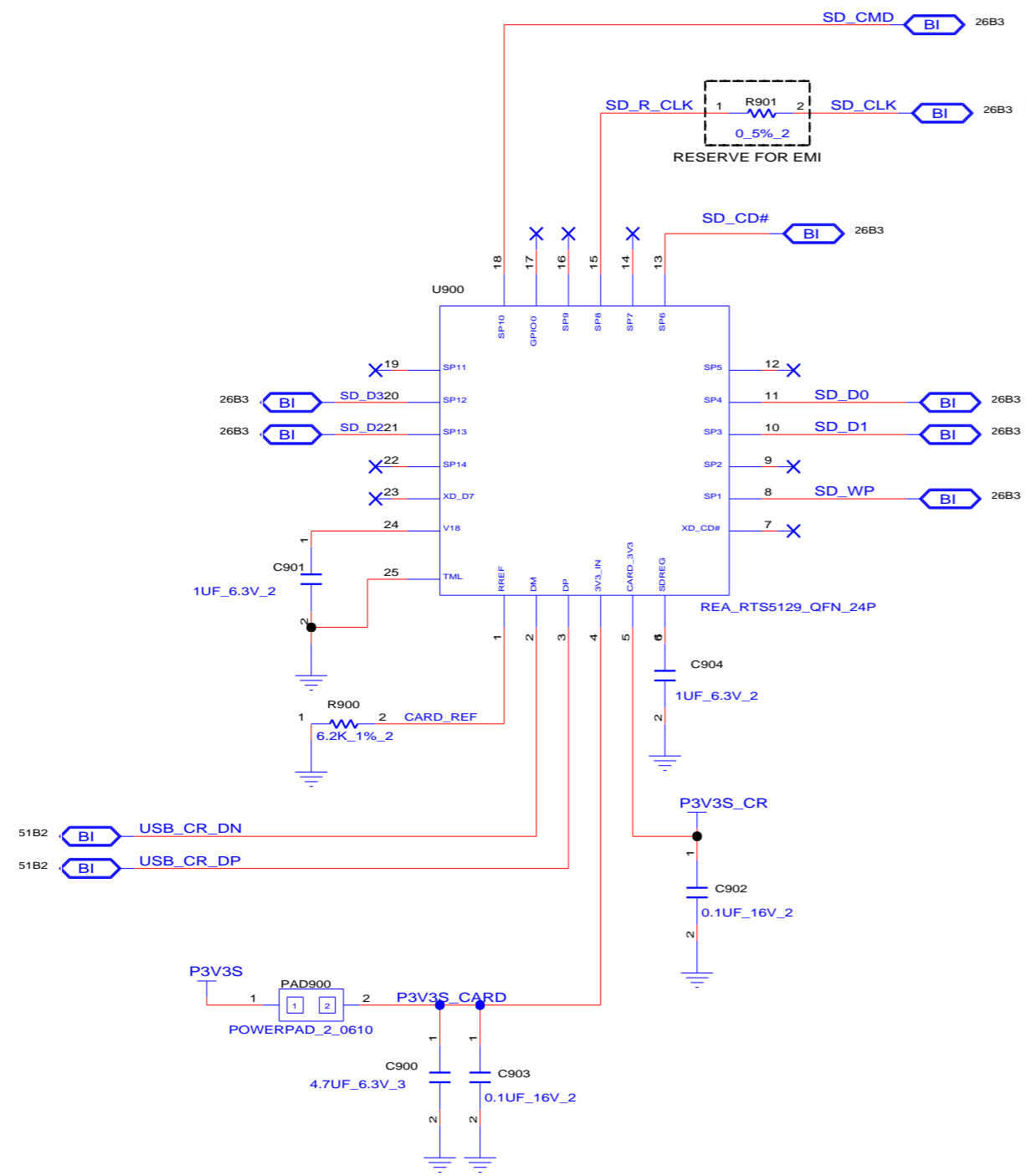
## HEADPHONE



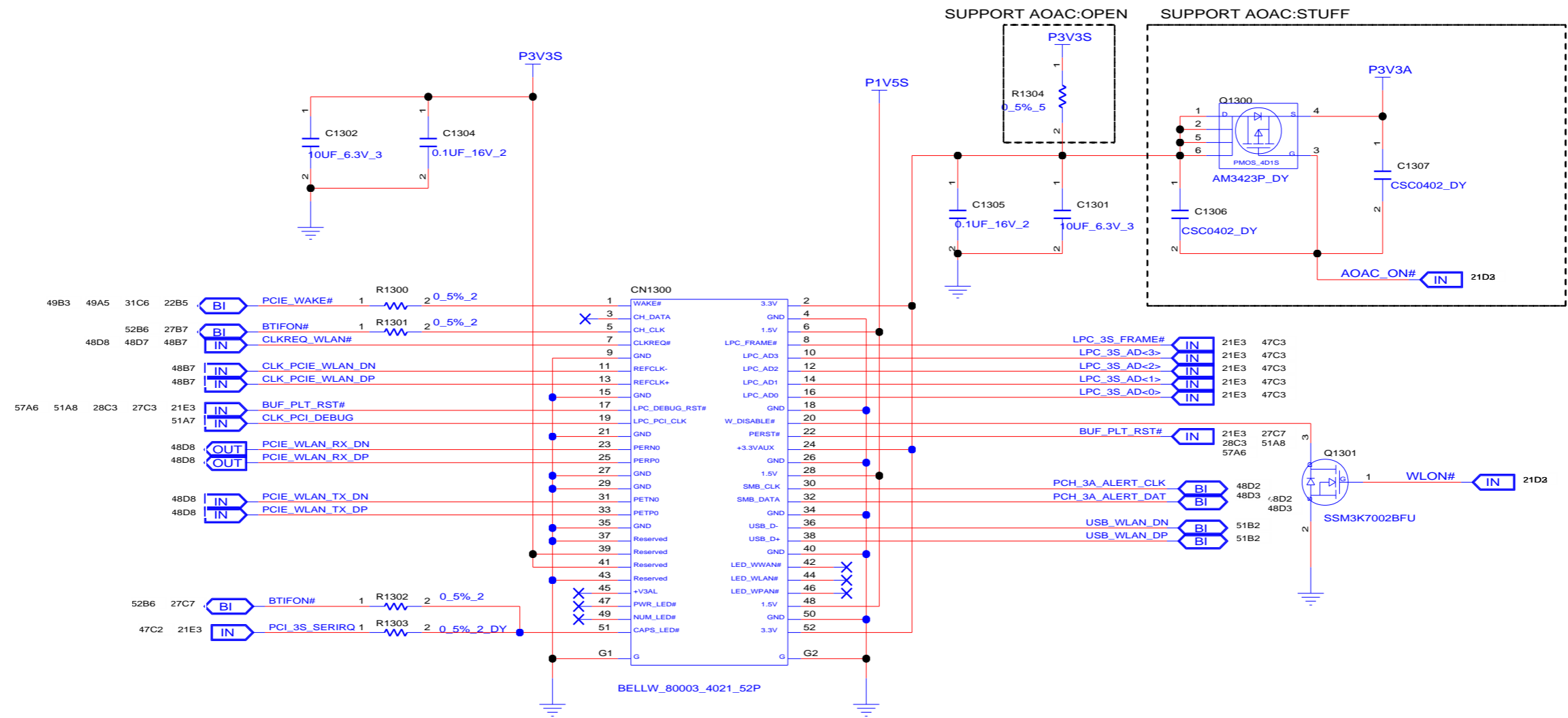
**INVENTEC**

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REFERNCE 900~999(CARDREADER)



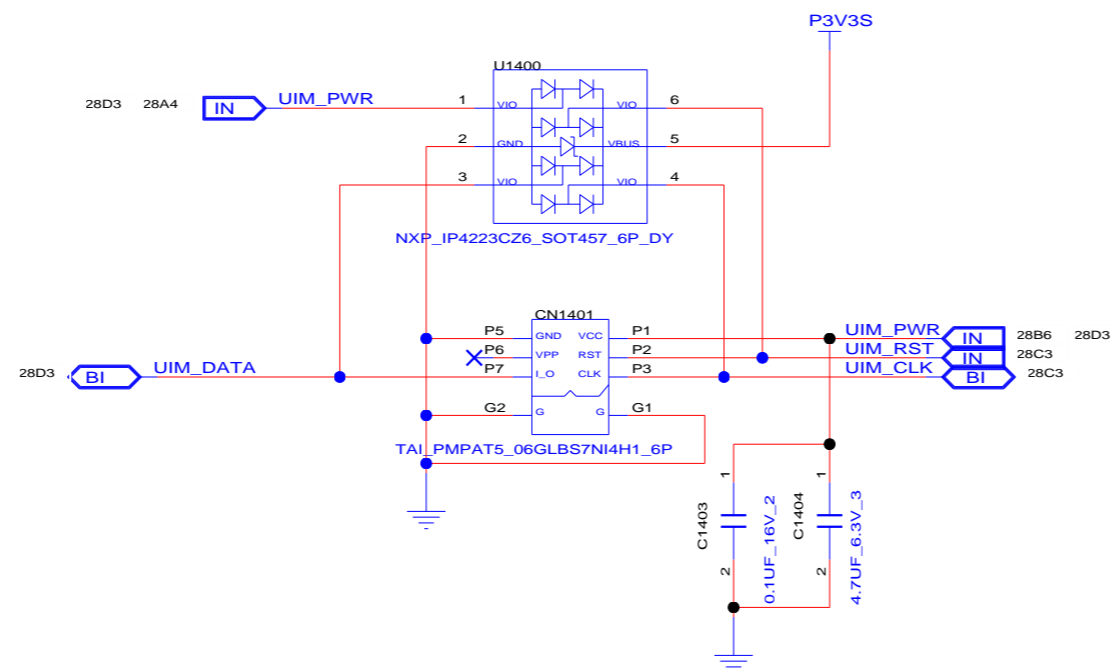
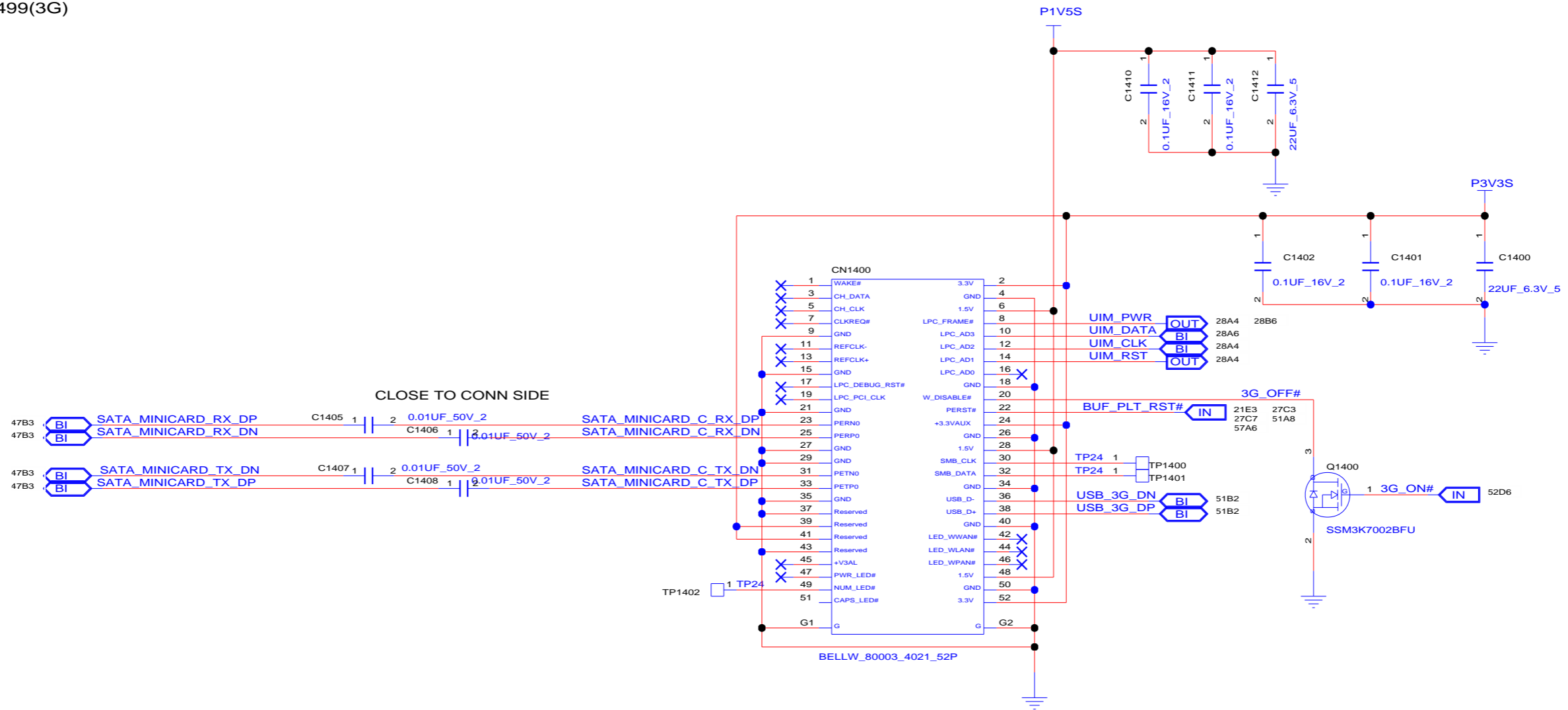
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# MINI CARD 1(WLAN)

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REFERENCE 1400-1499(3G)

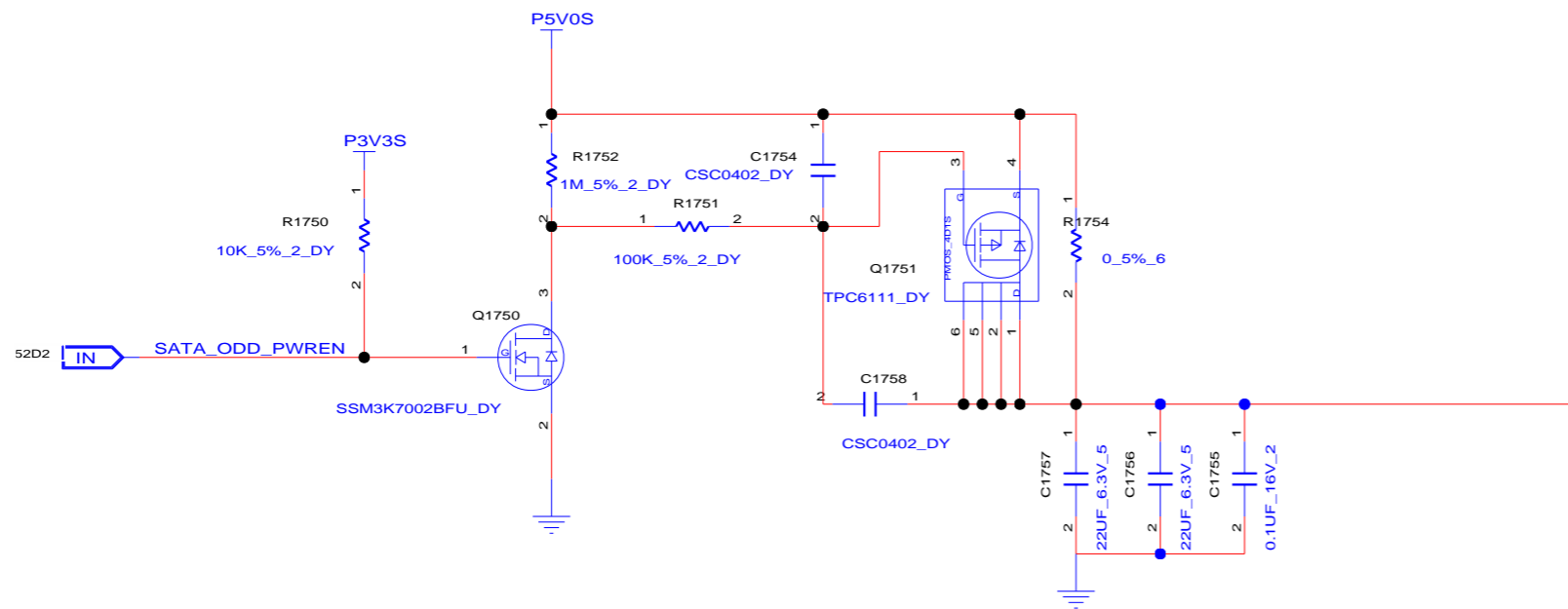
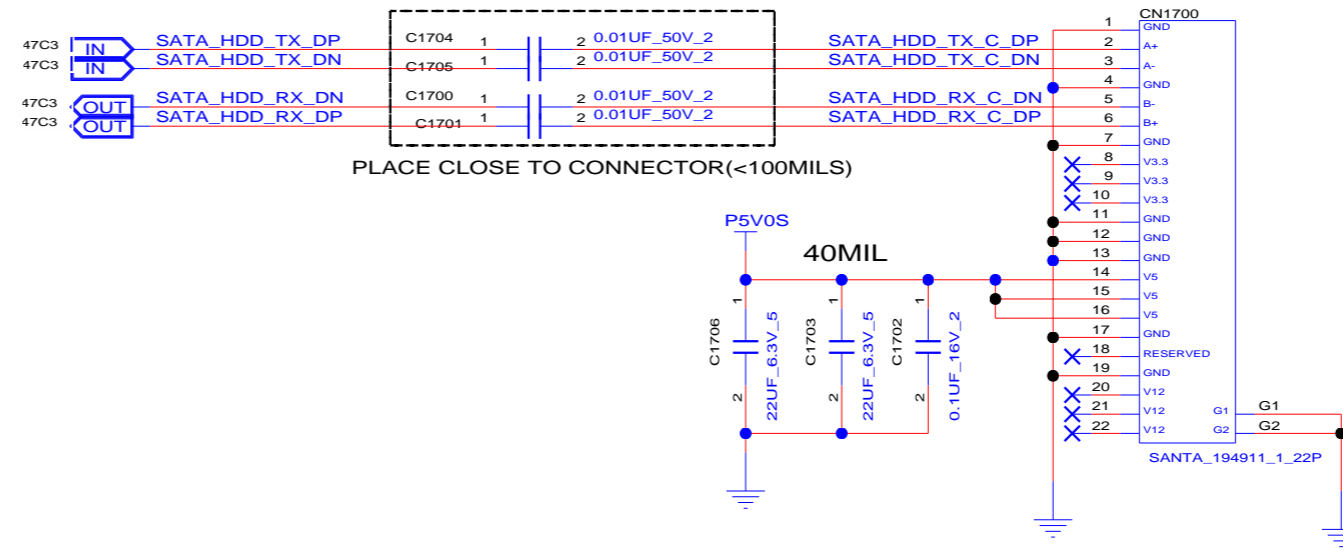


**INVENTEC**

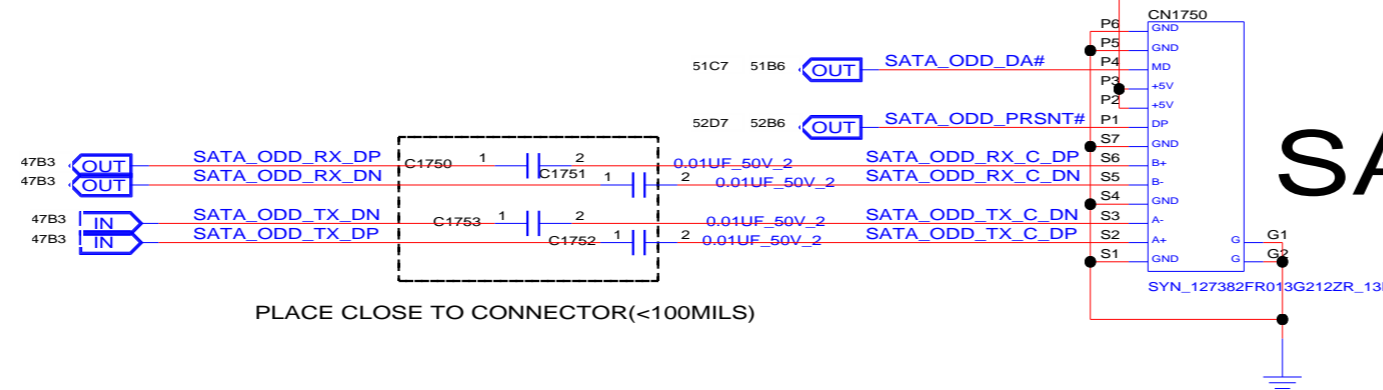
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SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

REFERENCE 1700~1749(HDD)  
 REFERENCE 1750~1799(ODD)

# SATA HDD



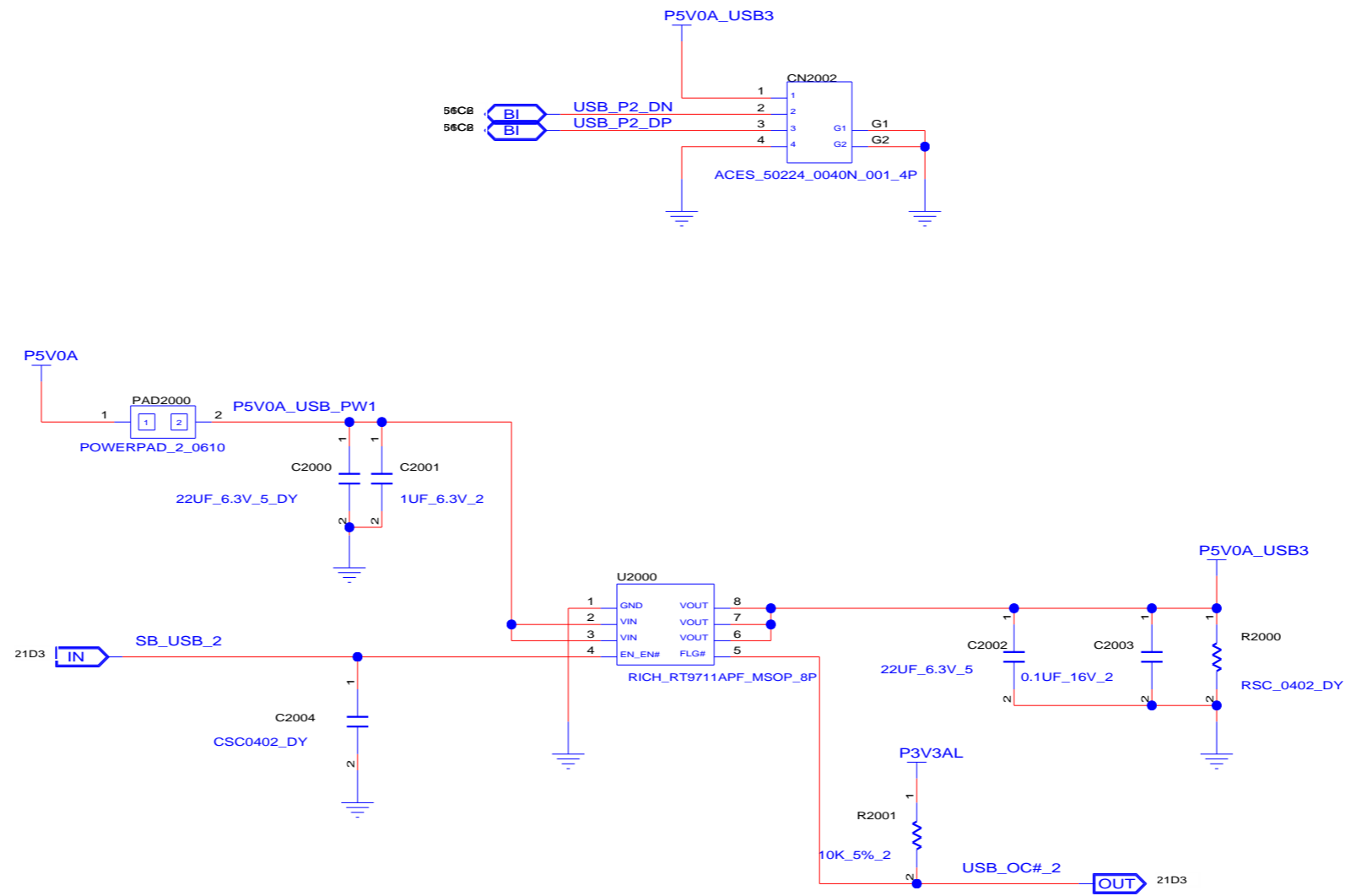
# SATA ODD



**INVENTEC**

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

REFERENCE 2000~2099(USB)



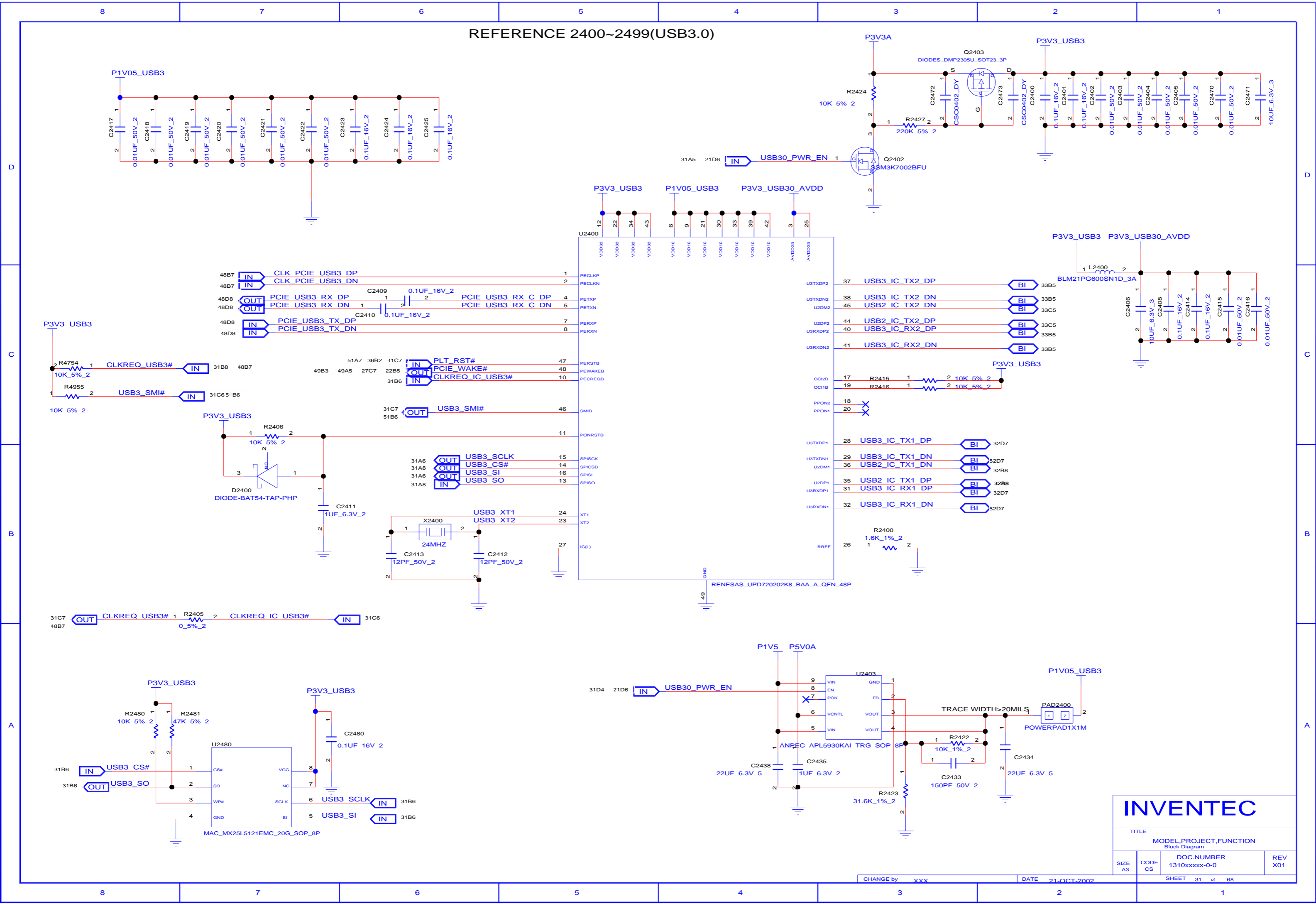
**INVENTEC**

TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

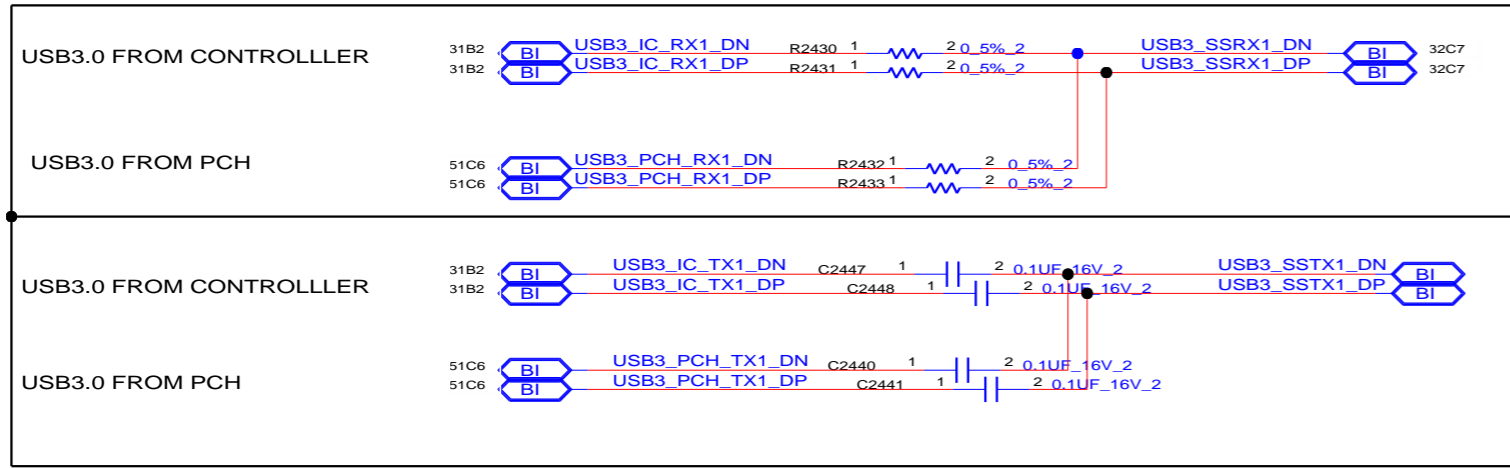
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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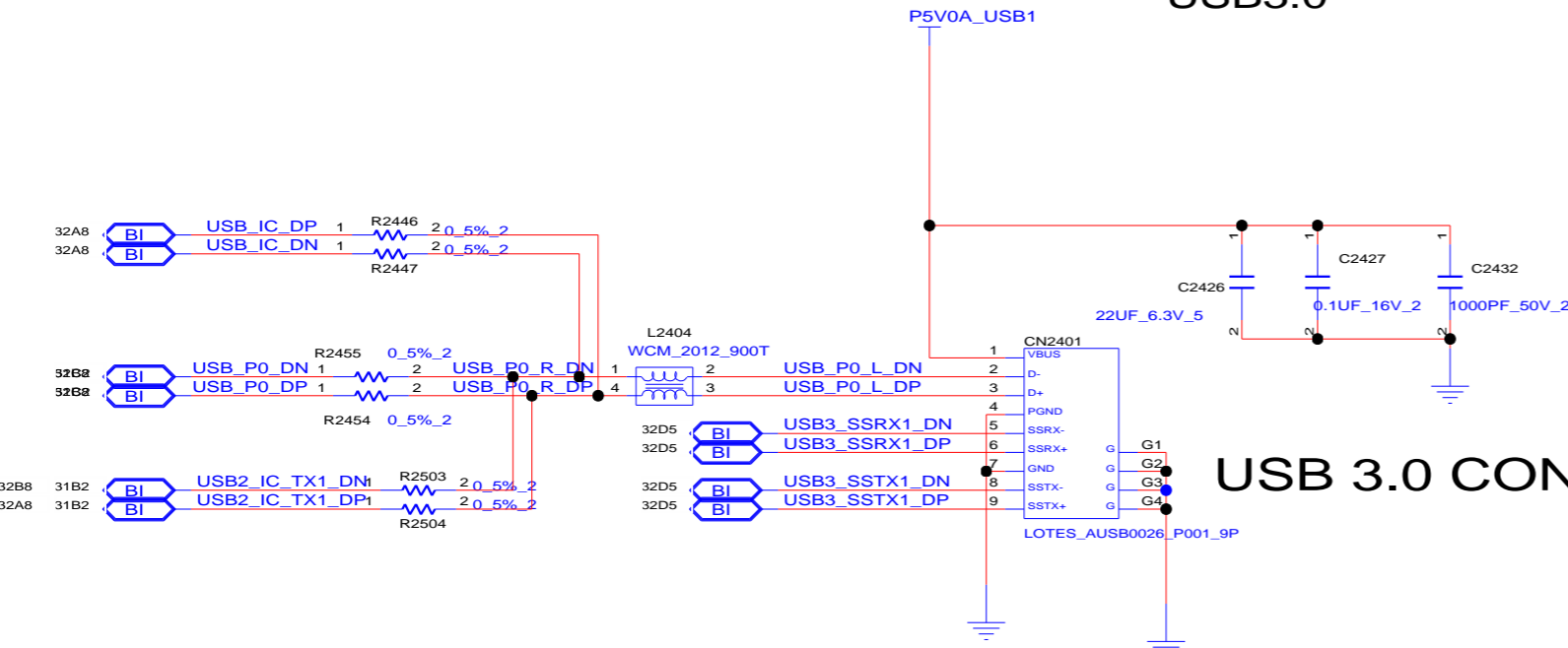
REFERENCE 2400~2499(USB3.0)



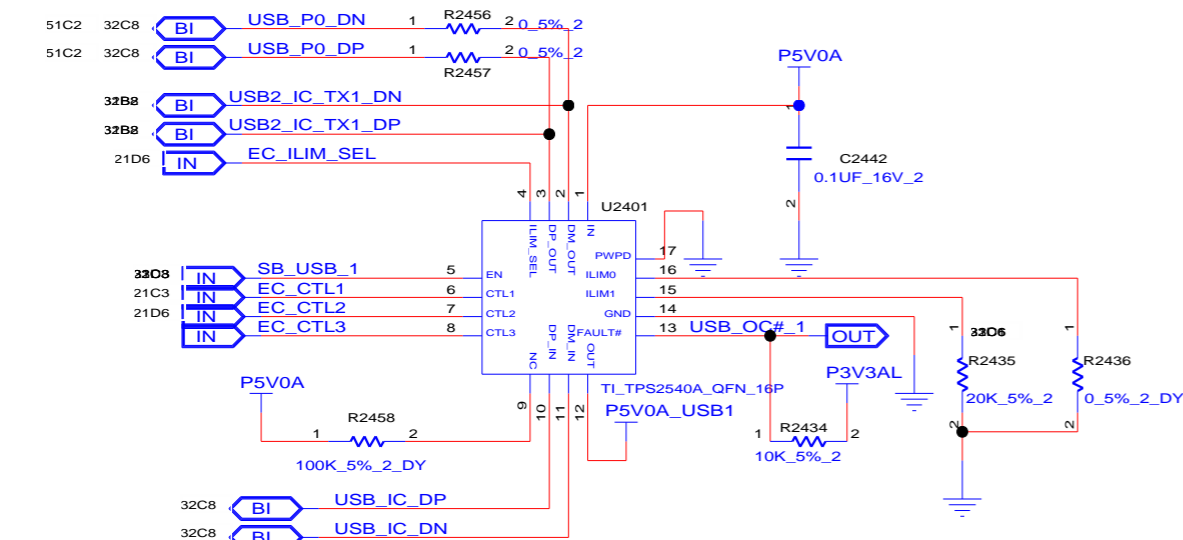
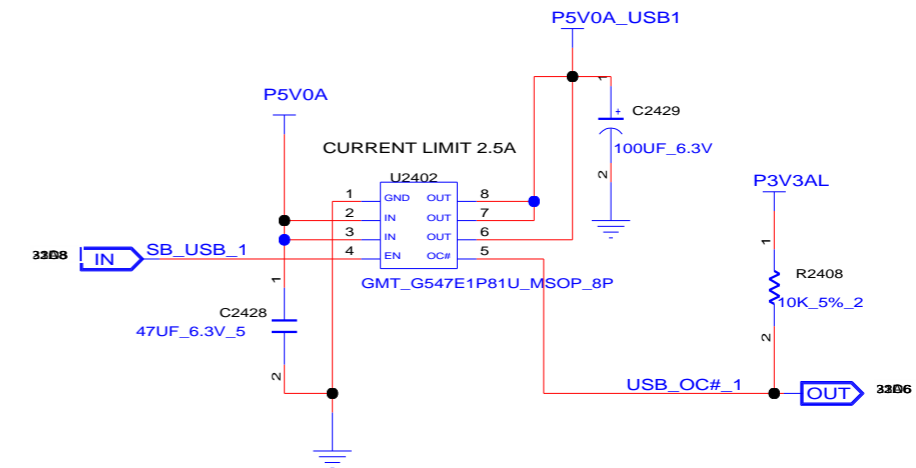
<b>INVENTEC</b>			
TITLE			
MODEL_PROJECT_FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by		DATE	SHEET
XXX		21-OCT-2002	31 of 68



USB3.0



USB 3.0 CONNECTOR



CTL1	CTL2	CTL3	Mode
0	0	X	Dedicated Charging Port, Auto-detect
0	1	X	Dedicated Charging Port, BC Specification 1.1 Only
1	0	X	Dedicated Charging Port, Apple Only
1	1	0	Standard Downstream Port, USB 2.0 Mode
1	1	1	Charging Downstream Port, BC Specification 1.1

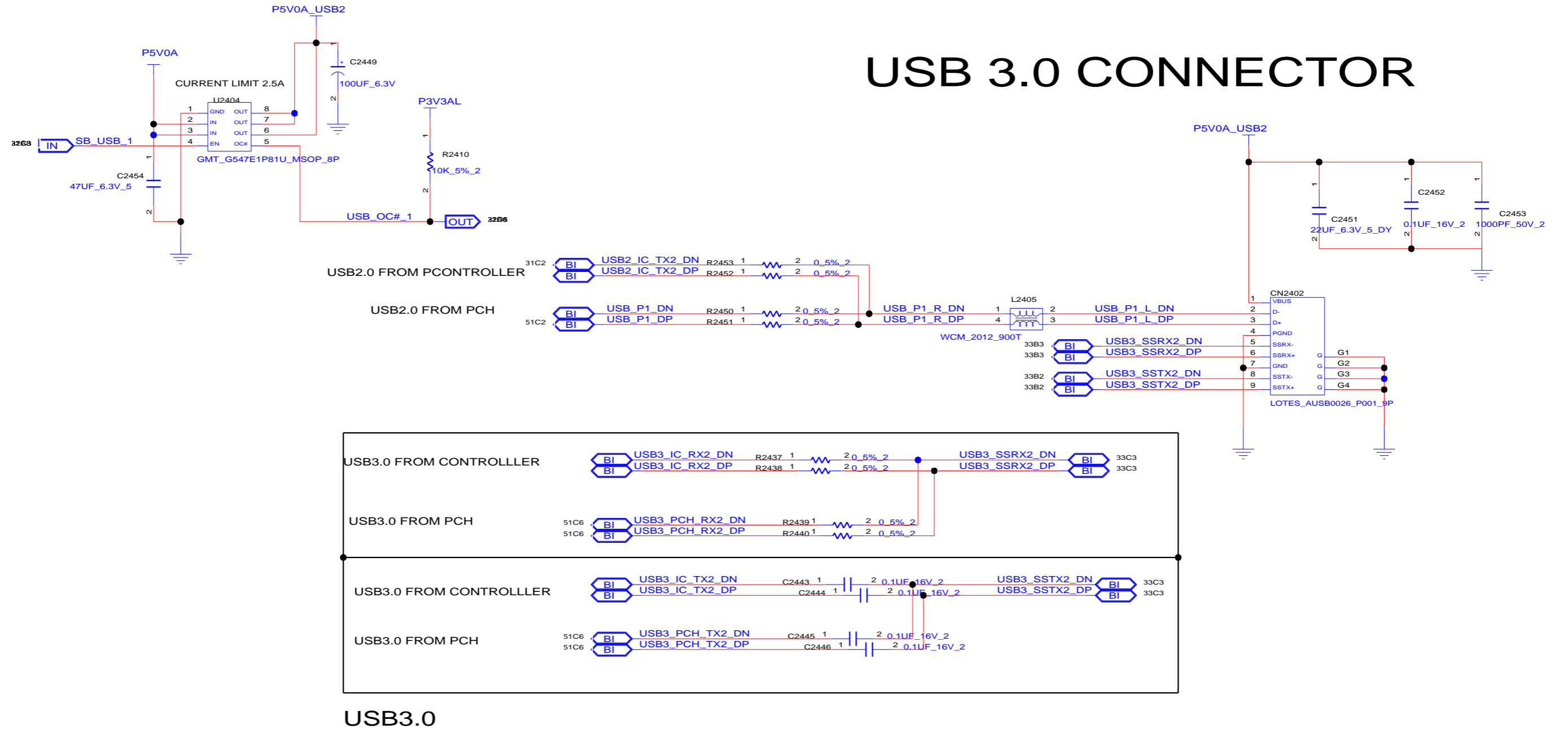
Table 3 – TPS2541 Control Truth Table

**INVENTEC**

TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01



# USB 3.0 CONNECTOR



**INVENTEC**

TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

REFERENCE 3000~3049(LCM)

D

C

B

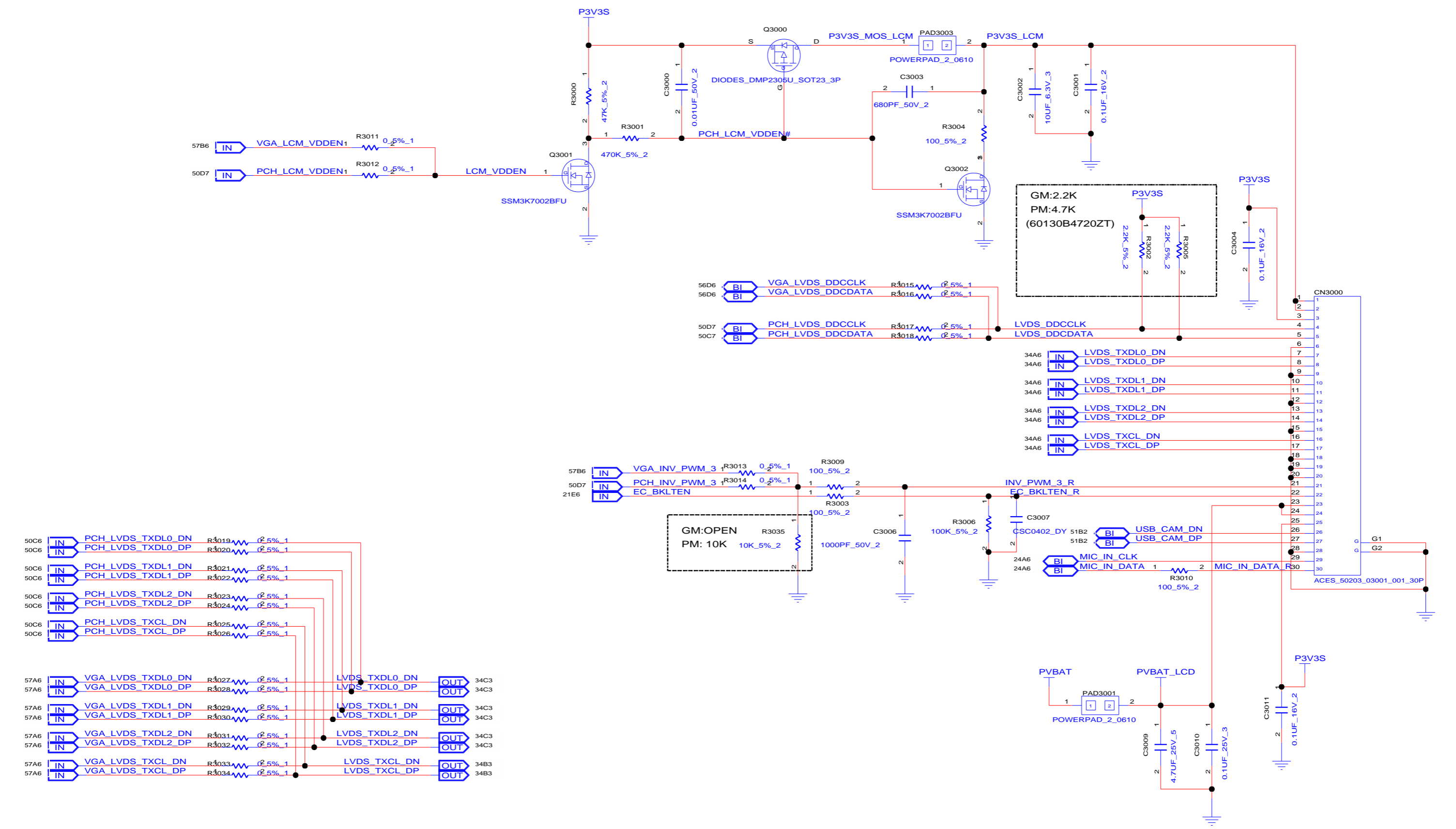
A

D

C

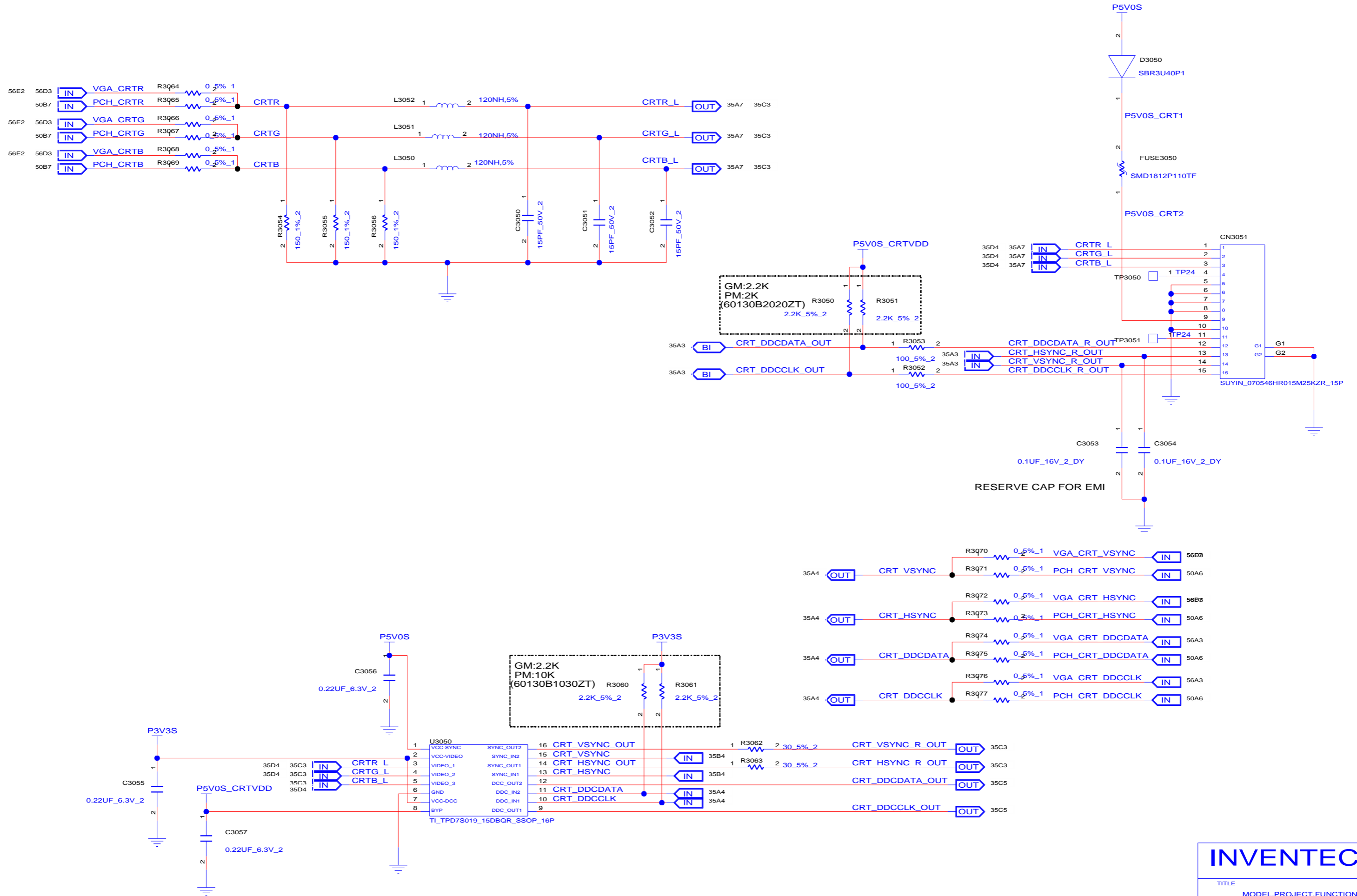
B

A



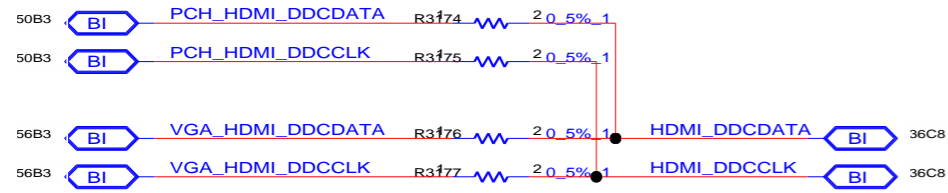
<b>INVENTEC</b>			
TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01

REFERENCE 3050~3099(CRT)

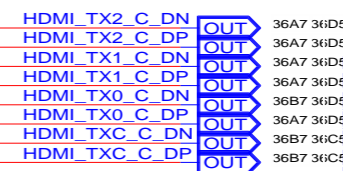
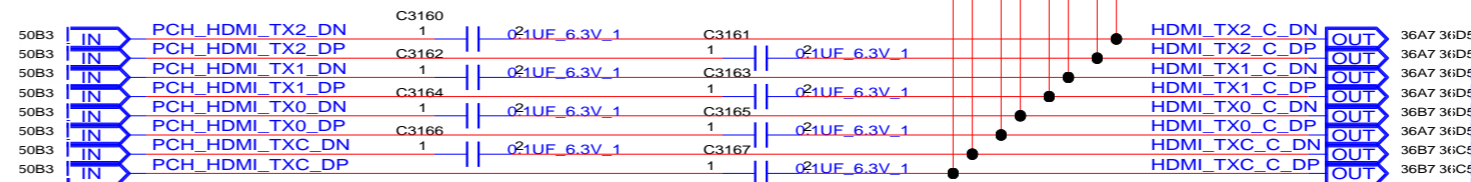
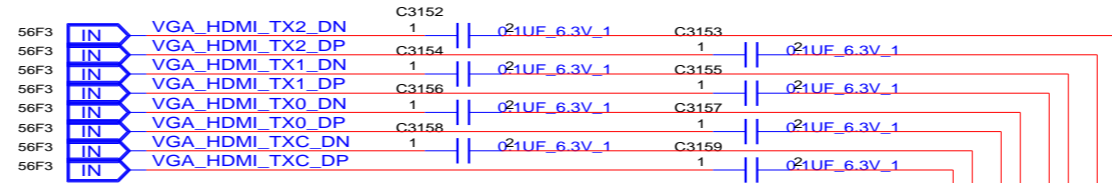
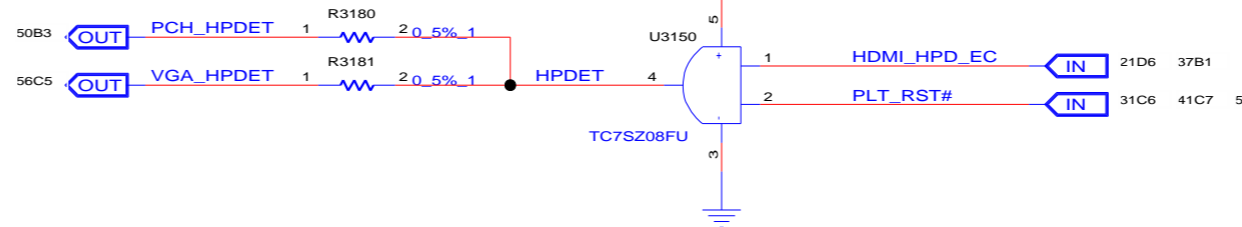
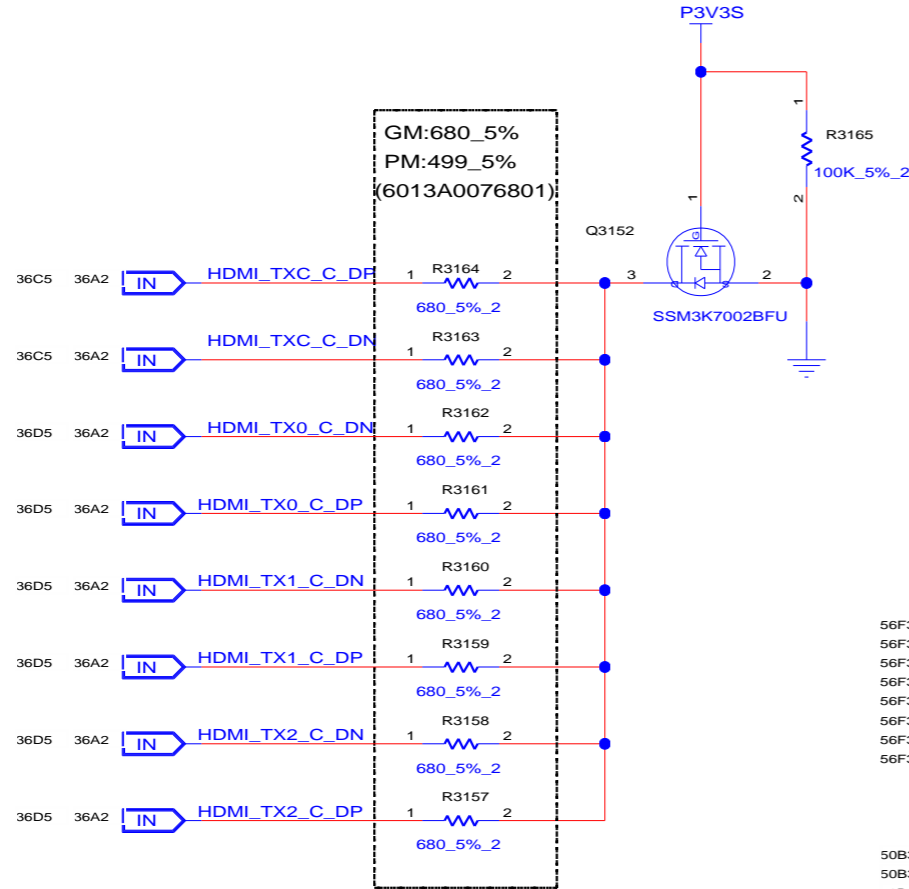
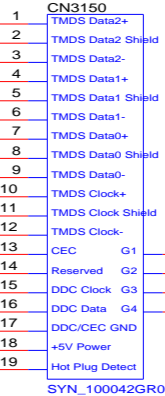
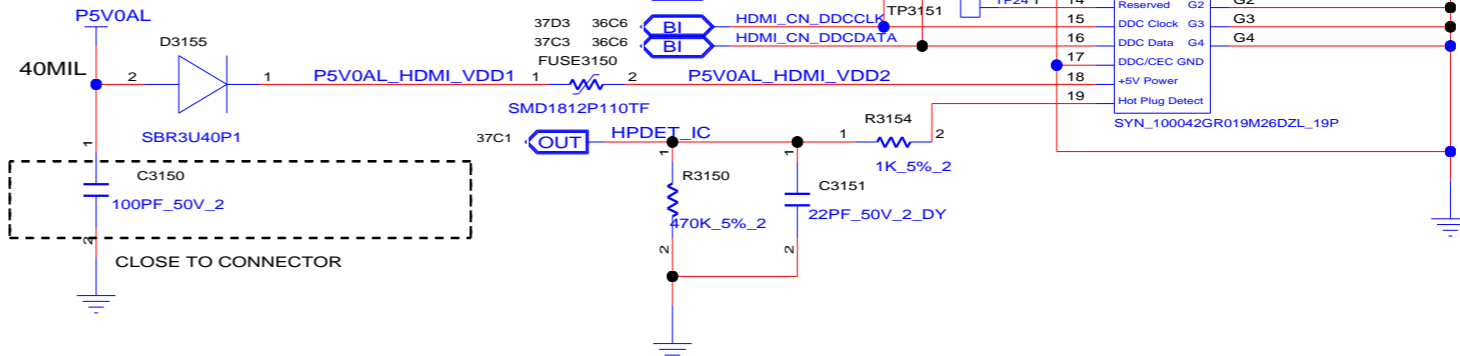
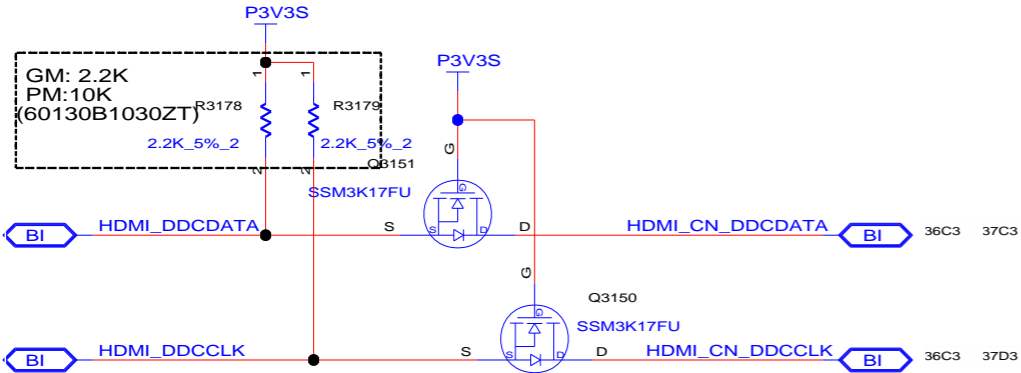
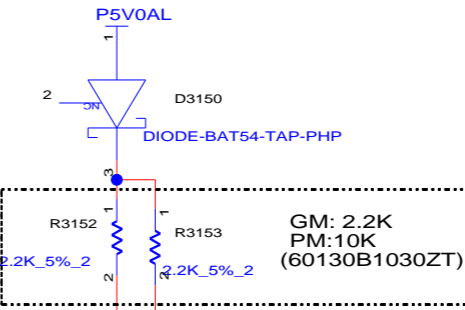
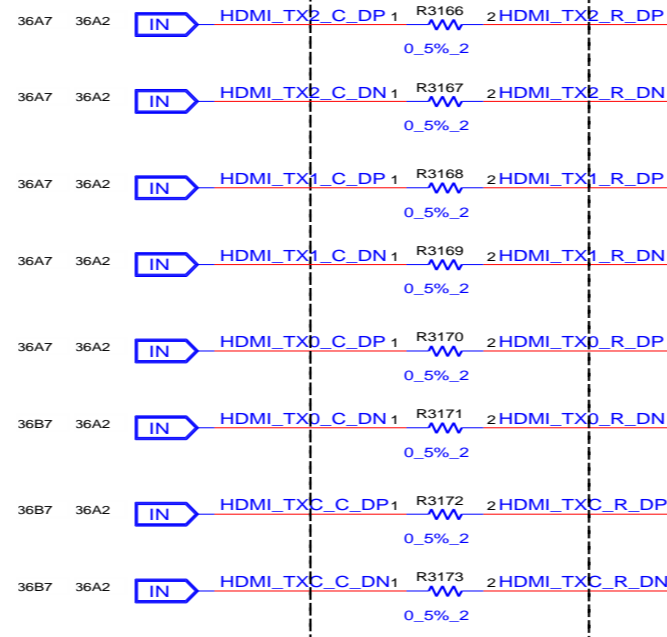


<b>INVENTEC</b>			
TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
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REFERENCE 3150~3199(HDMI)



PLACE CLOSE TO CONNECTOR

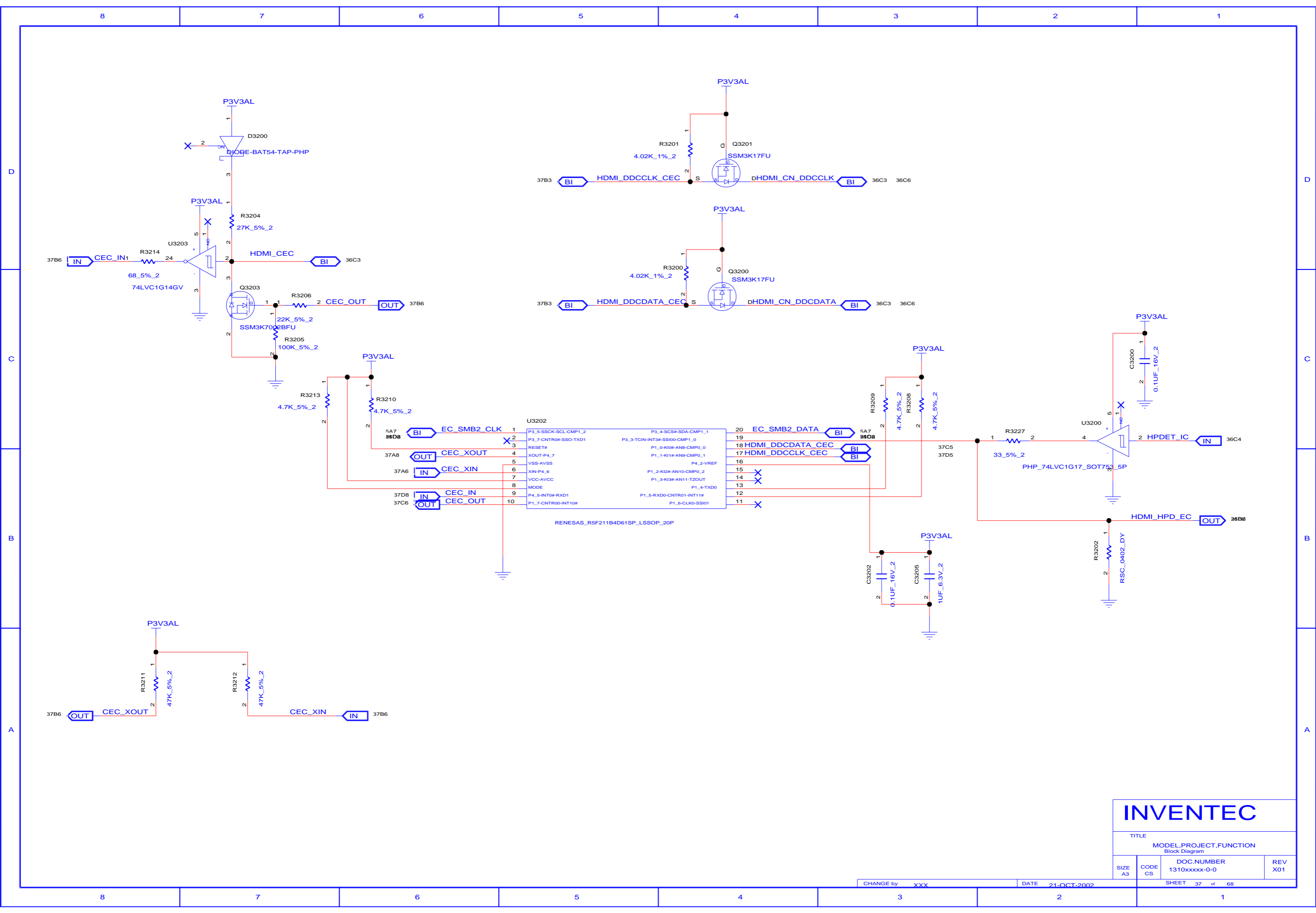


**INVENTEC**

TITLE MODEL\_PROJECT\_FUNCTION  
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
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CHANGE by XXX DATE 21-OCT-2002 SHEET 36 of 68



# INVENTEC

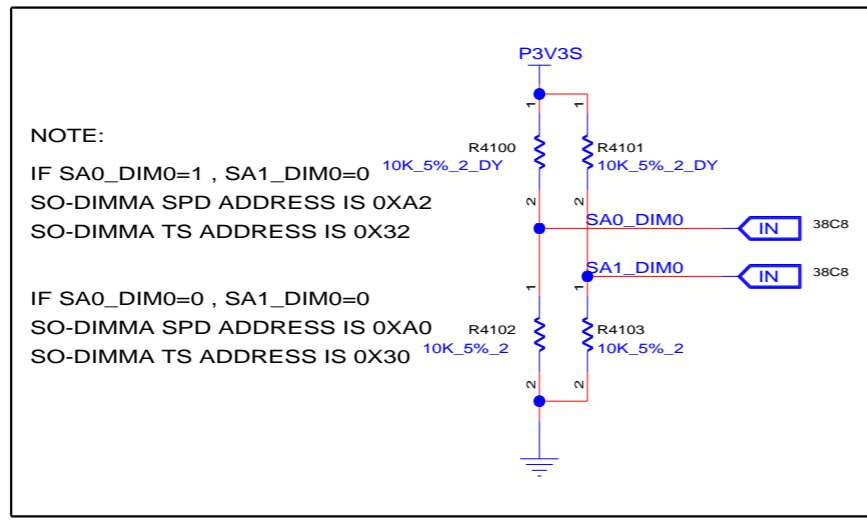
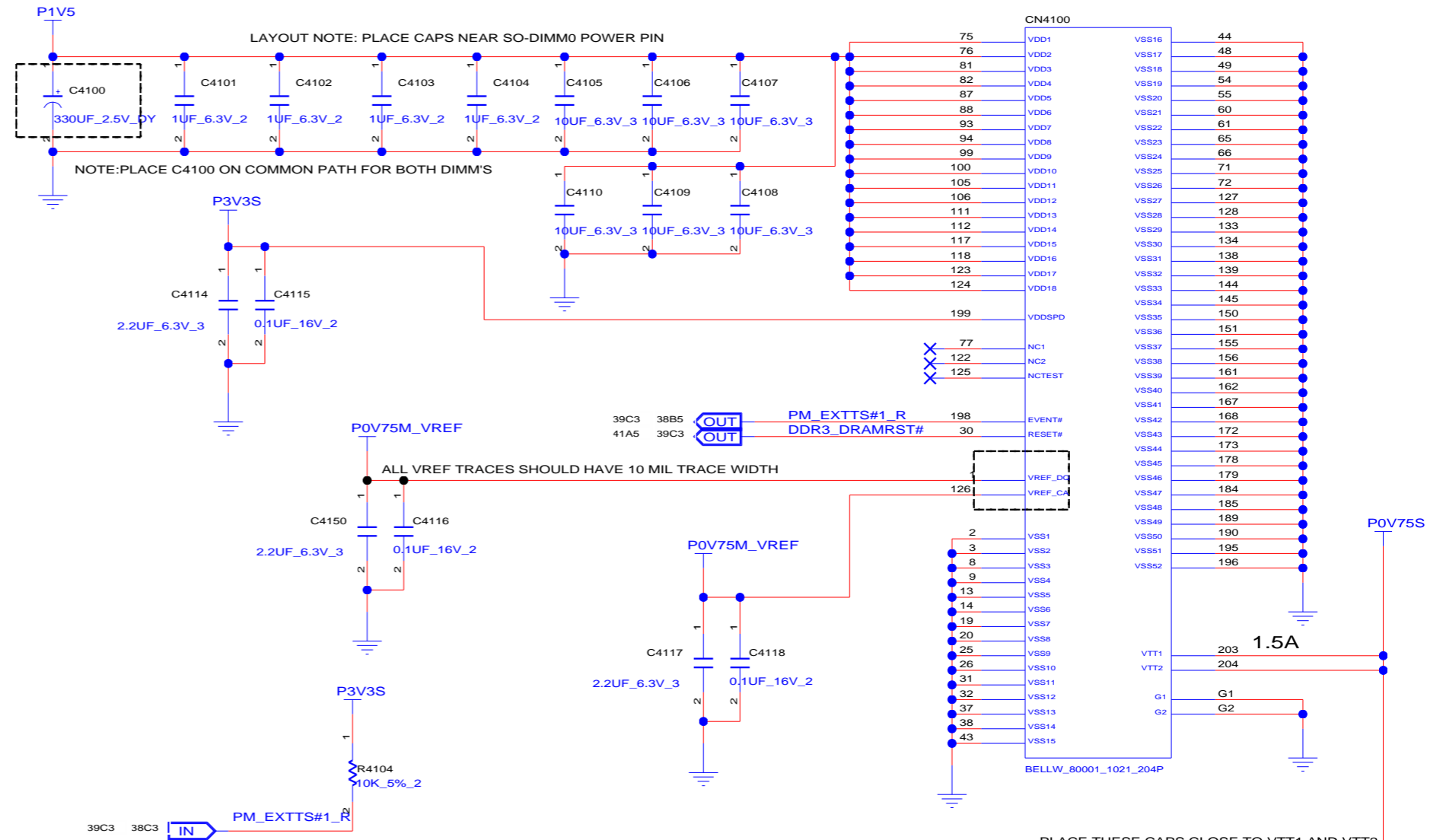
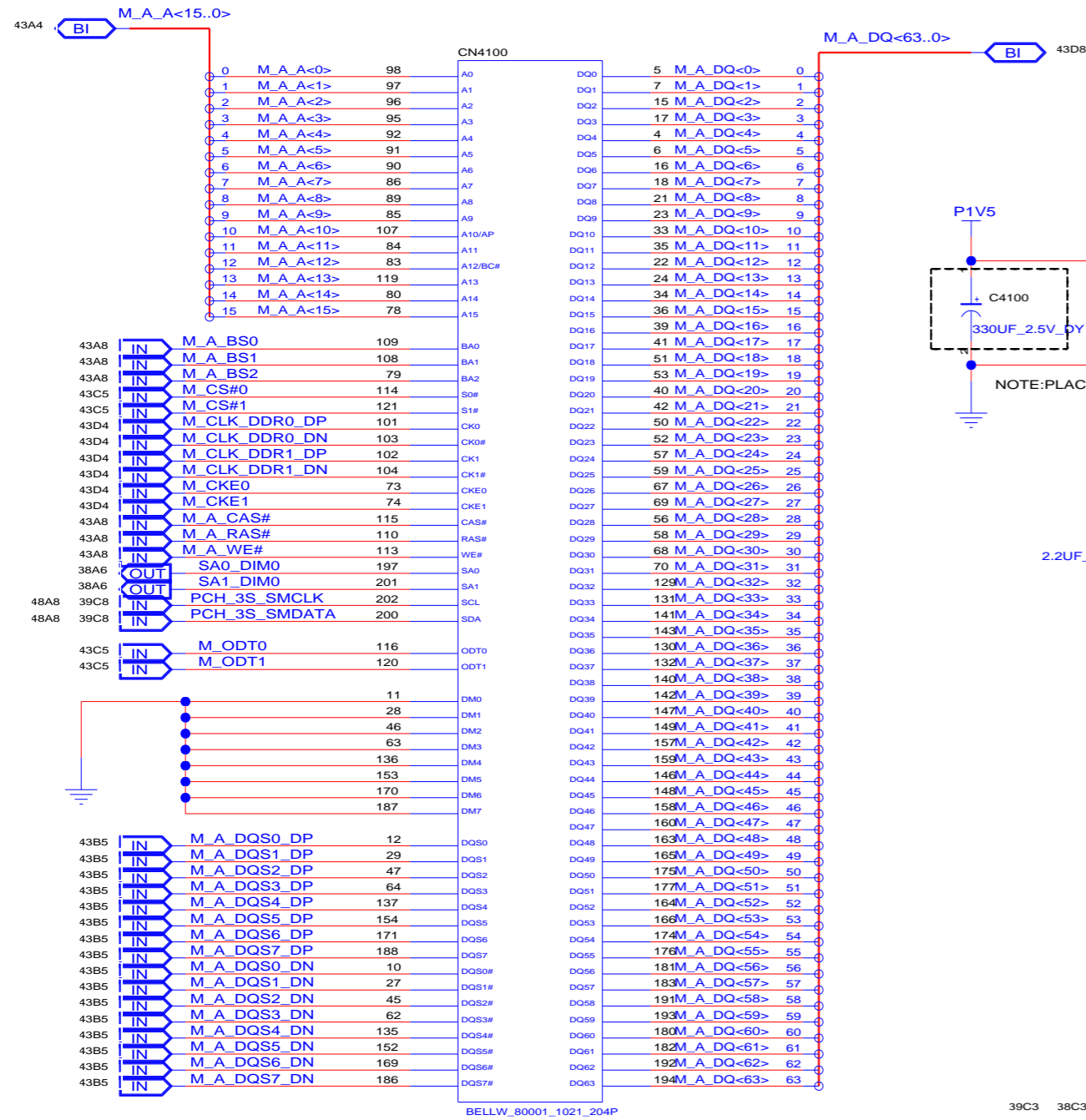
TITLE  
MODEL\_PROJECT\_FUNCTION  
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
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CHANGE by XXX DATE 21-OCT-2002 SHEET 37 of 68

# CHA

REFERENCE 4100-4299(DDR)

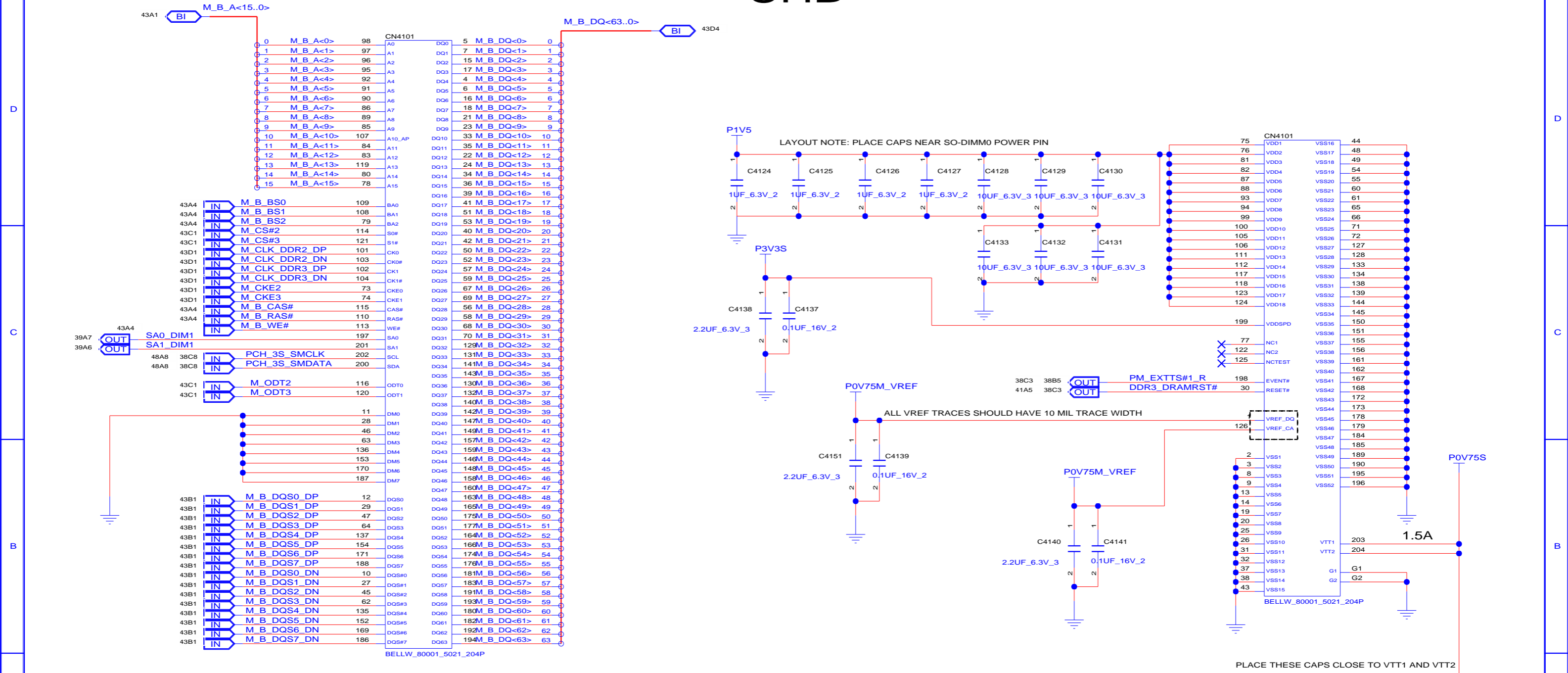


**INVENTEC**

TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 38 of 68

REFERENCE 4100~4299(DDR)

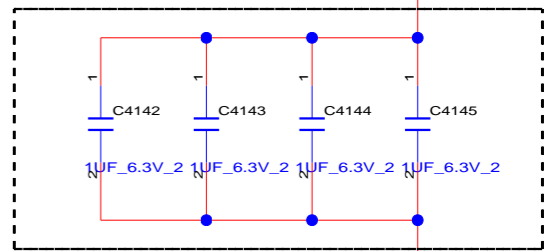
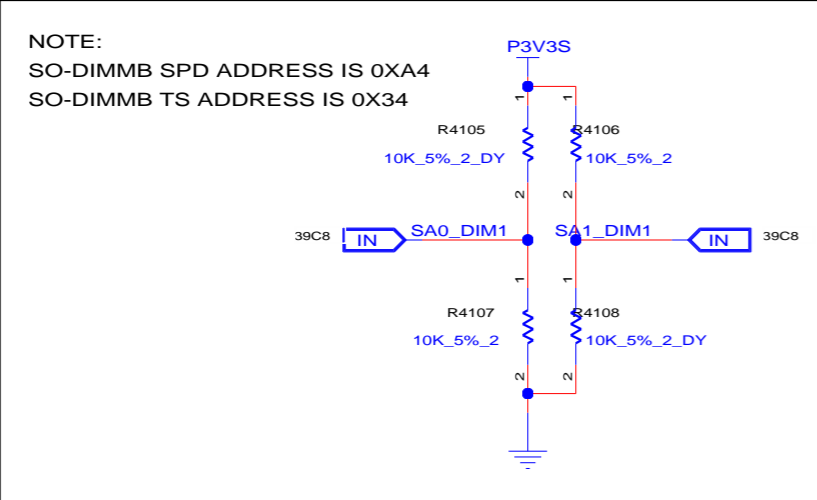
# CHB



LAYOUT NOTE: PLACE CAPS NEAR SO-DIMM0 POWER PIN

ALL VREF TRACES SHOULD HAVE 10 MIL TRACE WIDTH

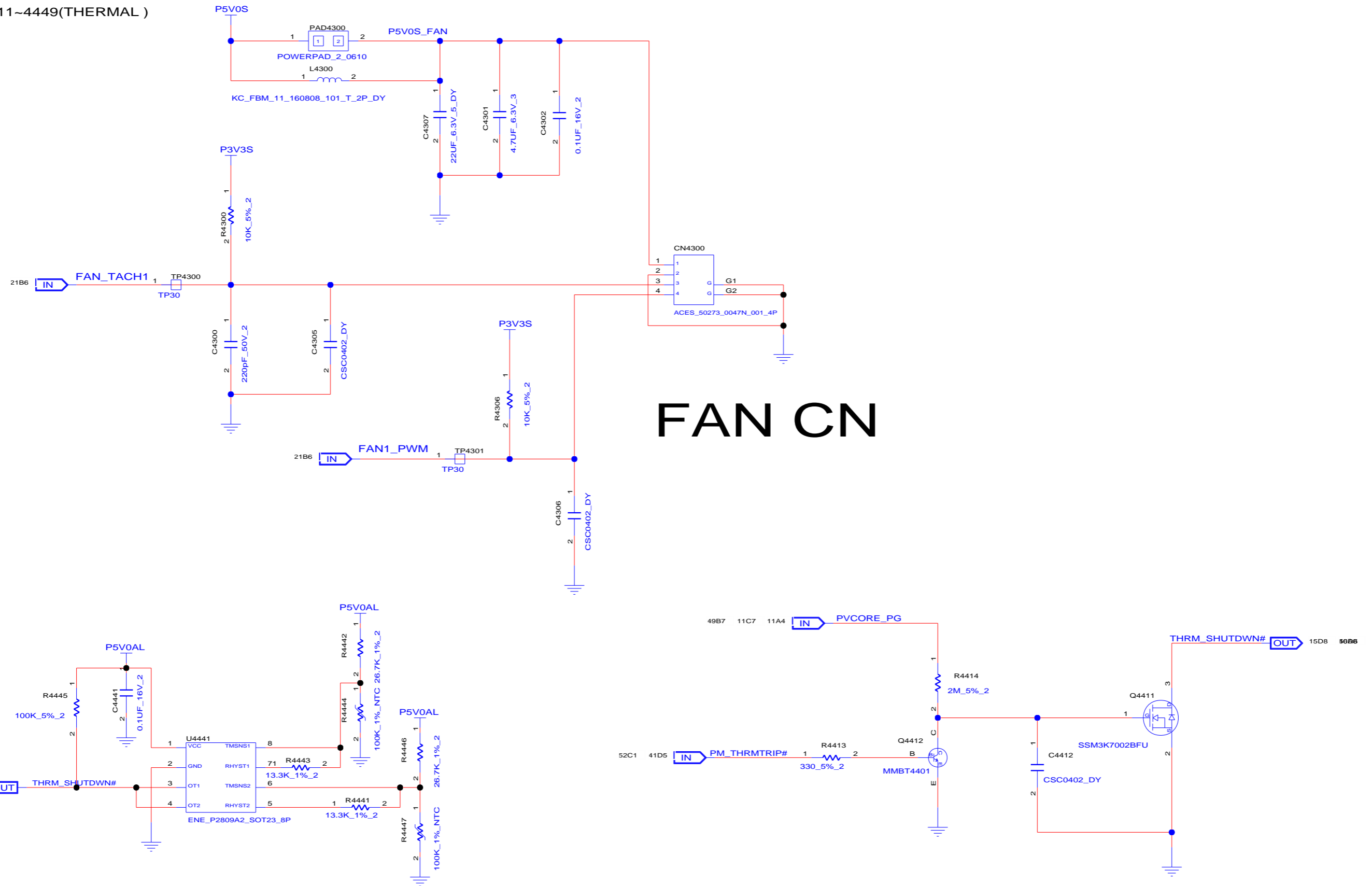
PLACE THESE CAPS CLOSE TO VTT1 AND VTT2



## INVENTEC

TITLE			
MODEL_PROJECT_FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01

REFERENCE 4300~4349(FAN)  
 REFERENCE 4411~4449(THERMAL)



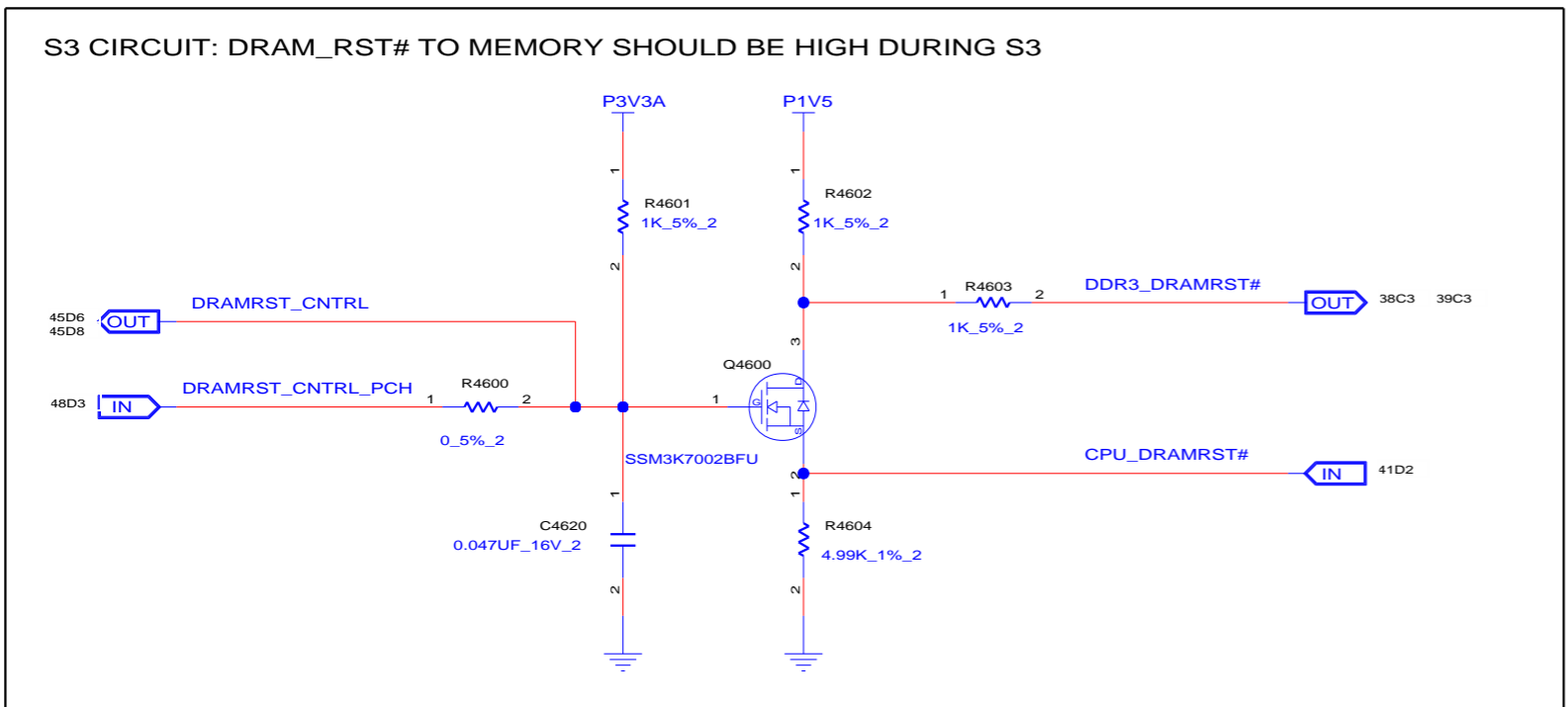
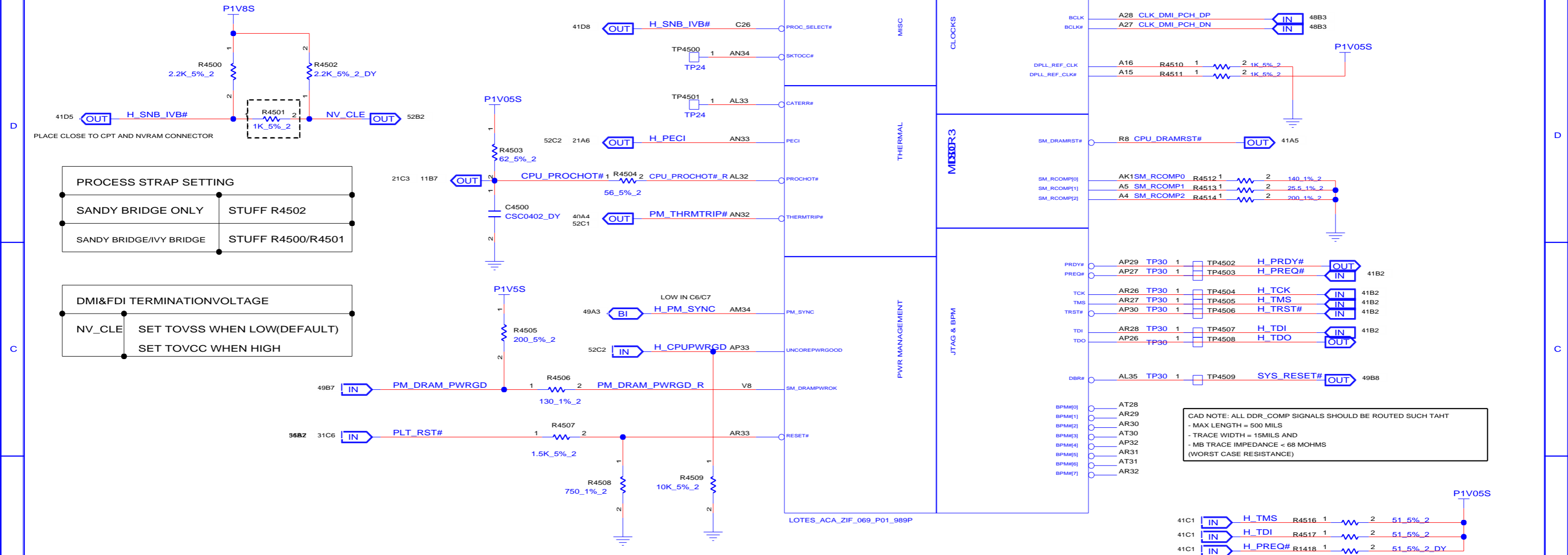
# FAN CN

**INVENTEC**

TITLE			
MODEL_PROJECT_FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01



REFERENCE 4500~4699(CPU)



<b>INVENTEC</b>			
TITLE			
MODEL_PROJECT_FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by		DATE	SHEET
XXX		21-OCT-2002	41 of 68

# REFERENCE 4500~4699(CPU)

D

C

B

A

D

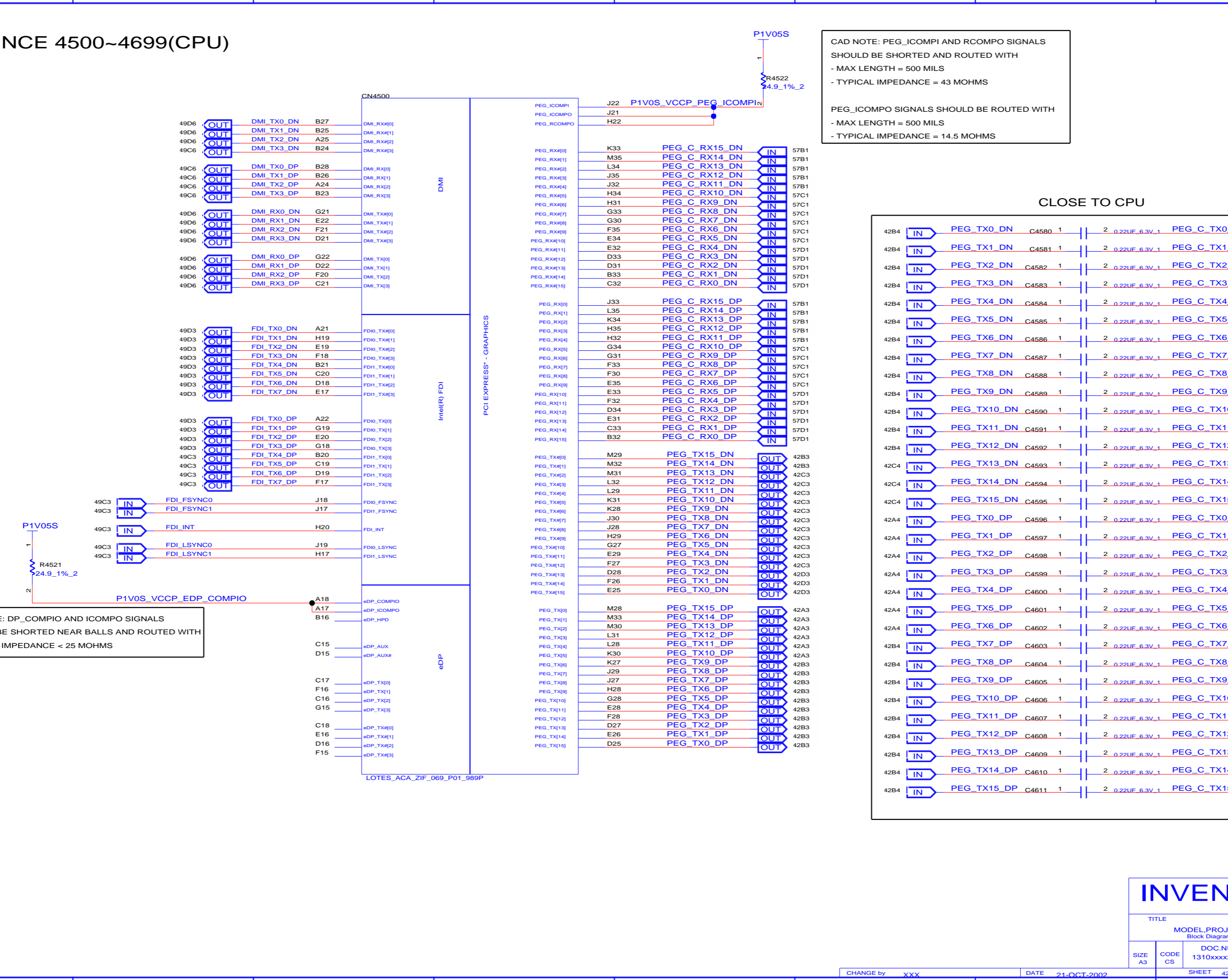
C

B

A

8 7 6 5 4 3 2 1

8 7 6 5 4 3 2 1

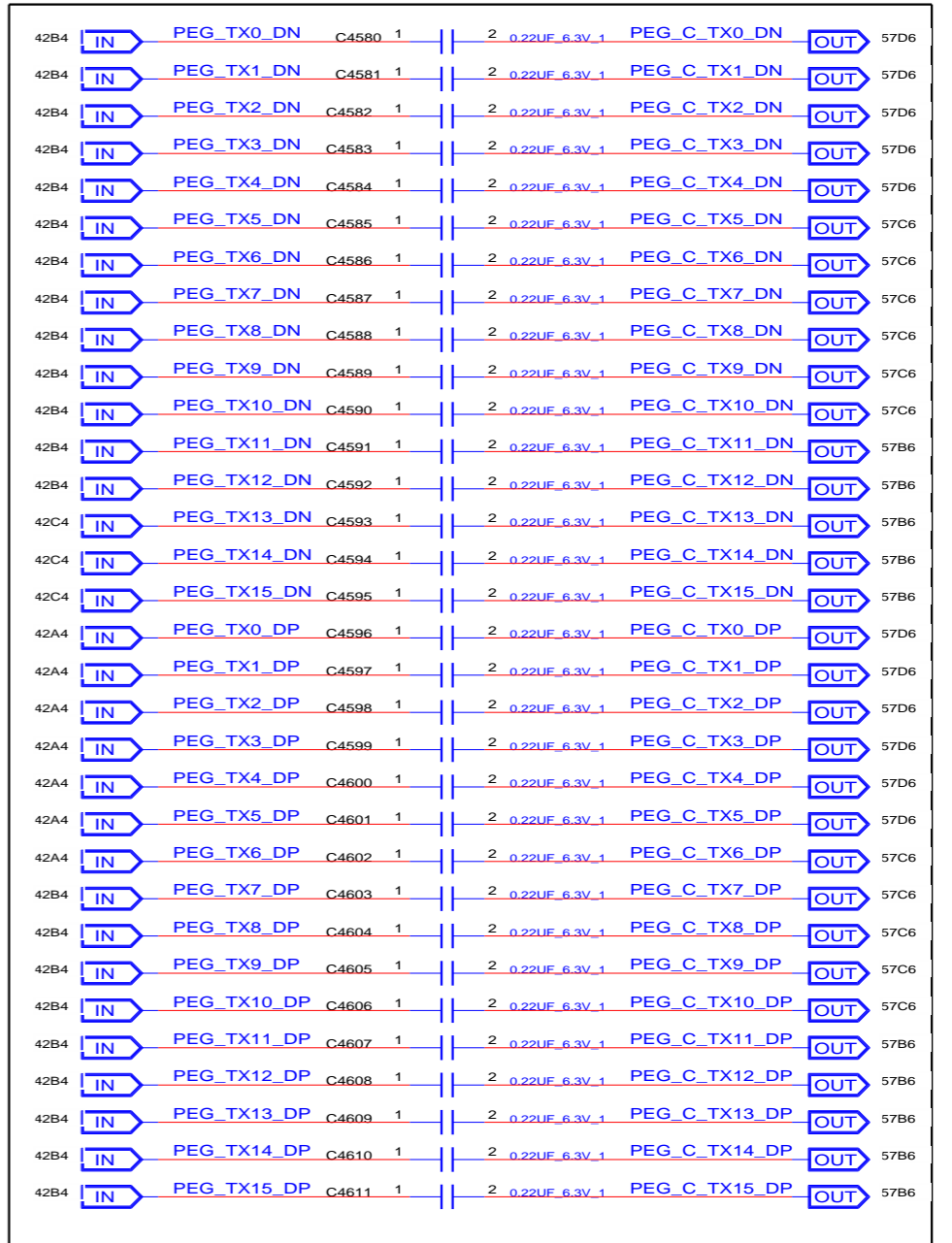


CAD NOTE: PEG\_ICOMPI AND RCOMPO SIGNALS SHOULD BE SHORTED AND ROUTED WITH  
 - MAX LENGTH = 500 MILS  
 - TYPICAL IMPEDANCE = 43 MOHMS

PEG\_ICOMPO SIGNALS SHOULD BE ROUTED WITH  
 - MAX LENGTH = 500 MILS  
 - TYPICAL IMPEDANCE = 14.5 MOHMS

CAD NOTE: DP\_COMPIO AND ICOMPO SIGNALS SHOULD BE SHORTED NEAR BALLS AND ROUTED WITH  
 - TYPICAL IMPEDANCE < 25 MOHMS

## CLOSE TO CPU



**INVENTEC**

TITLE  
 MODEL,PROJECT,FUNCTION  
 Block Diagram

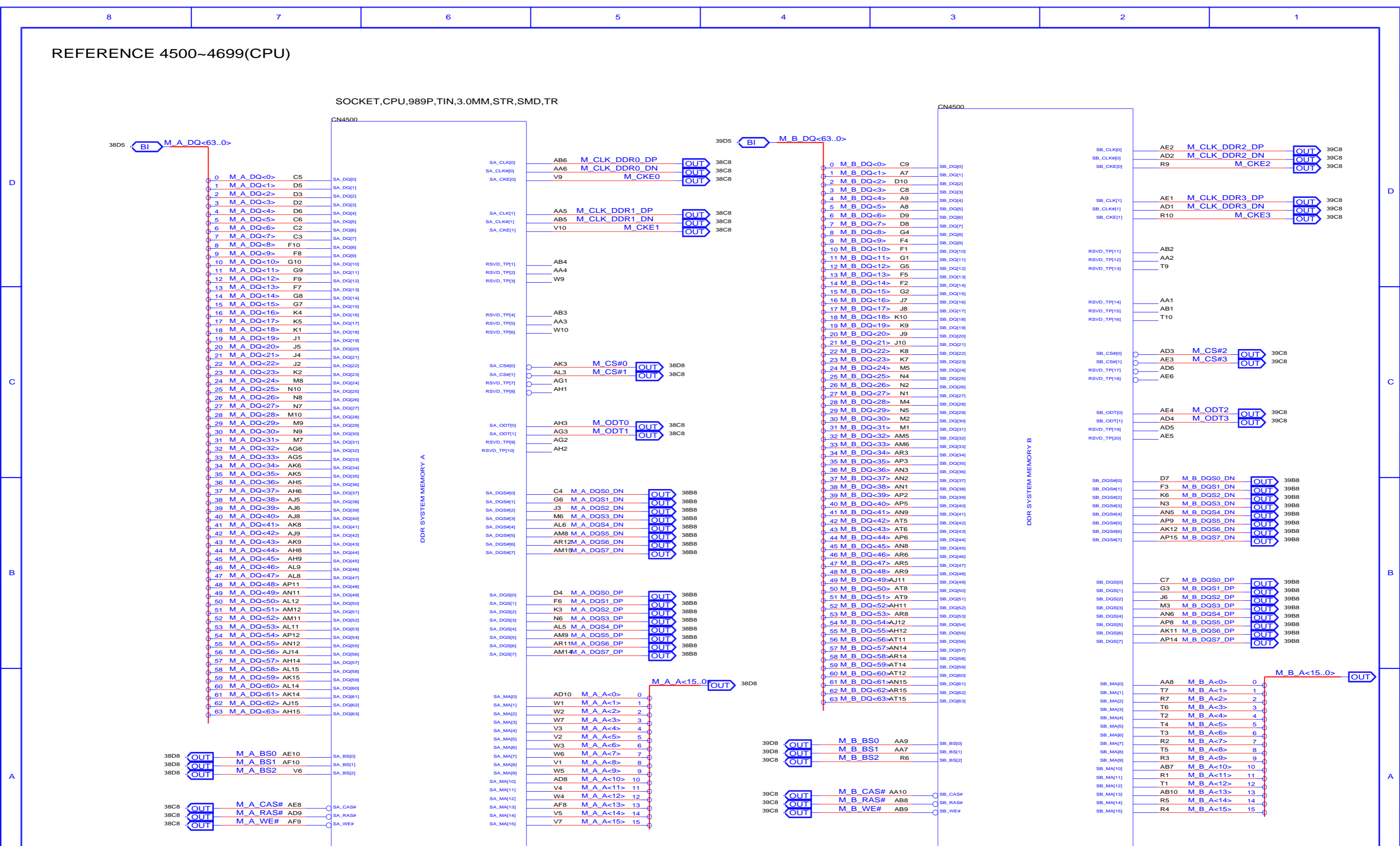
SIZE A3 CODE CS DOC.NUMBER 1310xxxx-0-0 REV X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 42 of 68

LOTES\_ACA\_ZIF\_069\_P01\_989P

REFERENCE 4500~4699(CPU)

SOCKET,CPU,989P,TIN,3.0MM,STR,SMD,TR

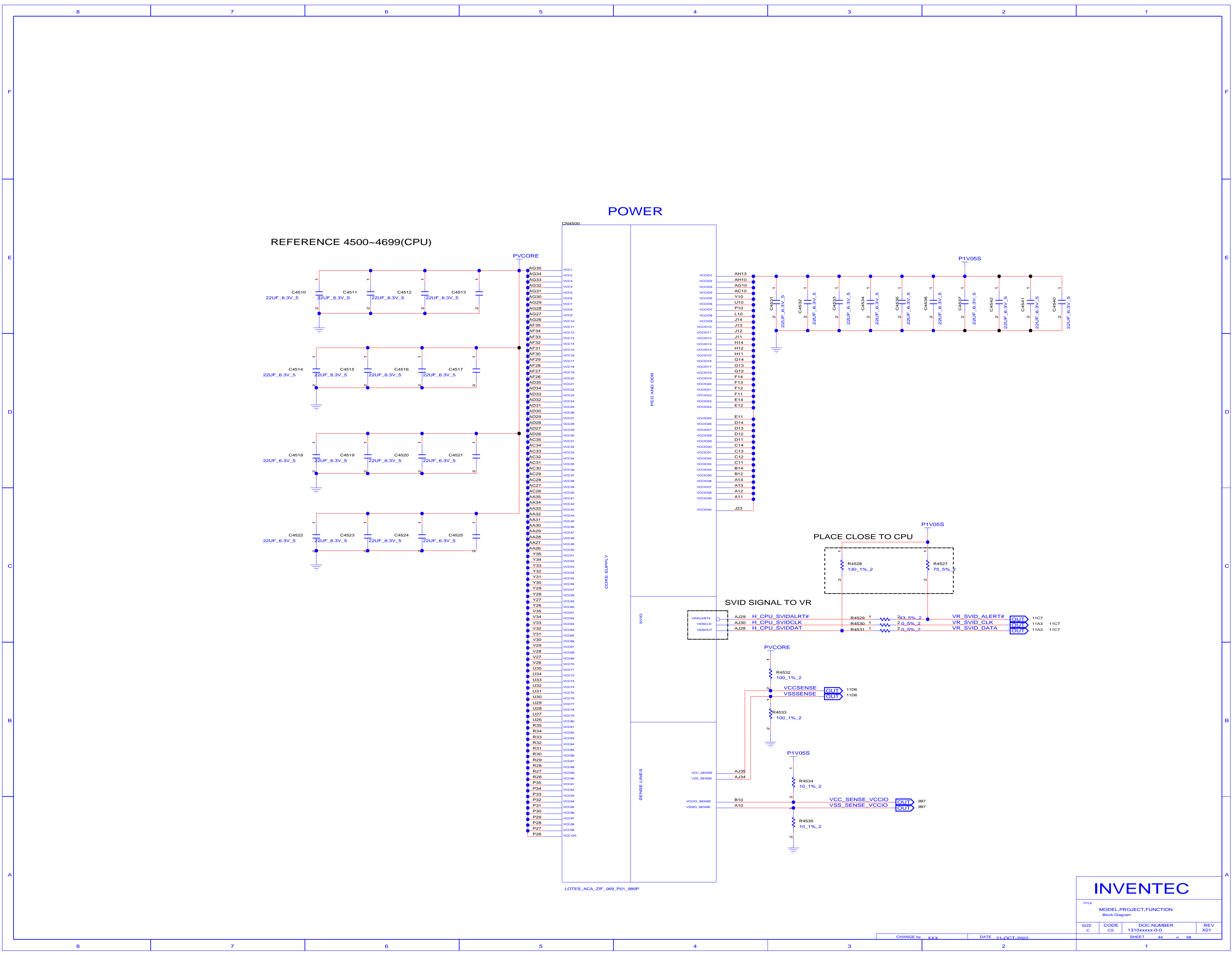


**INVENTEC**

TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
------------	------------	-----------------------------	------------

CHANGE by XXX DATE 21-OCT-2002 SHEET 43 of 68



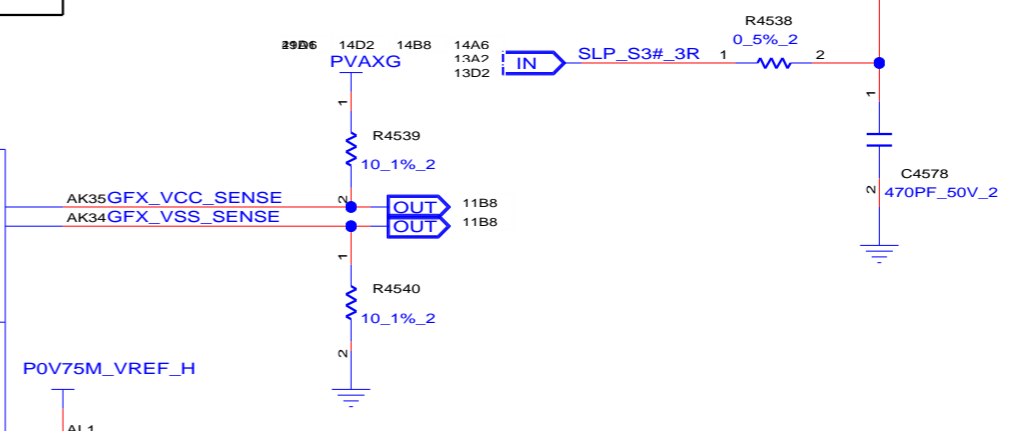
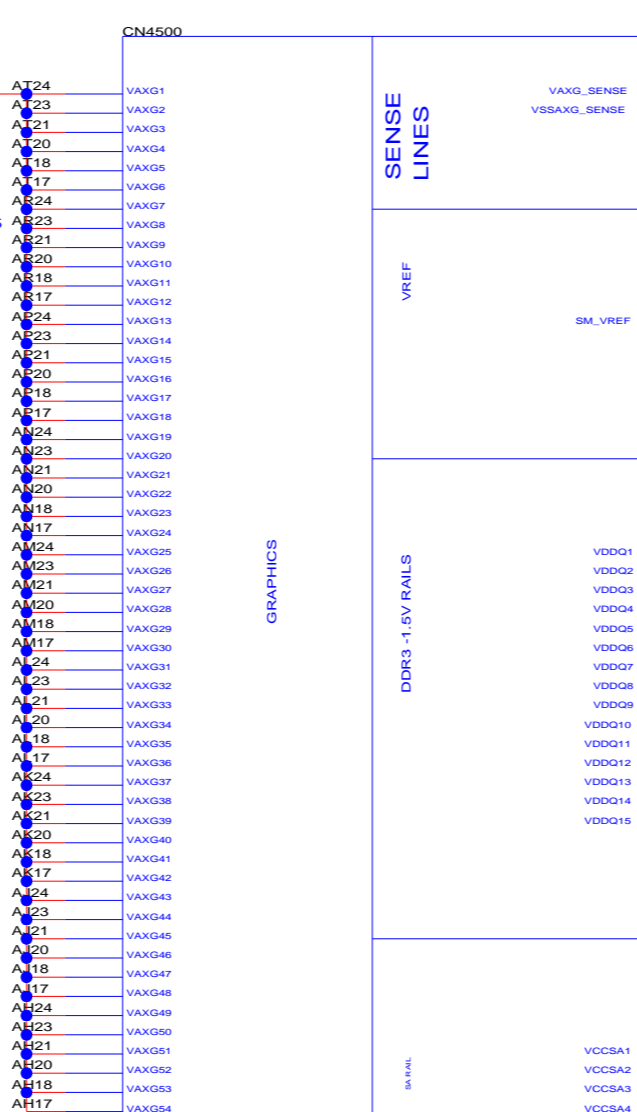
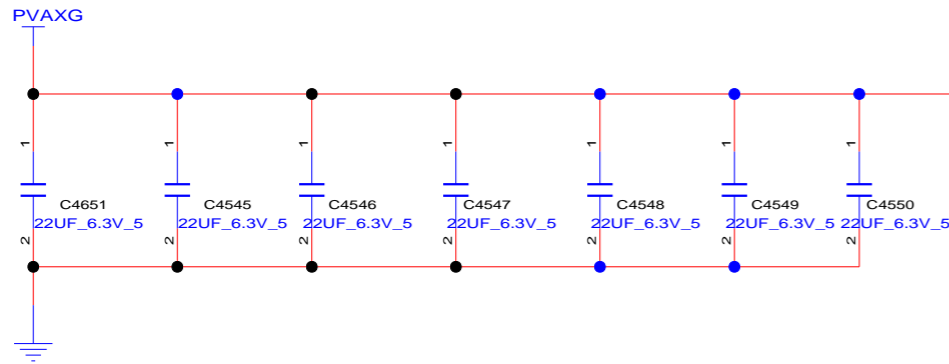
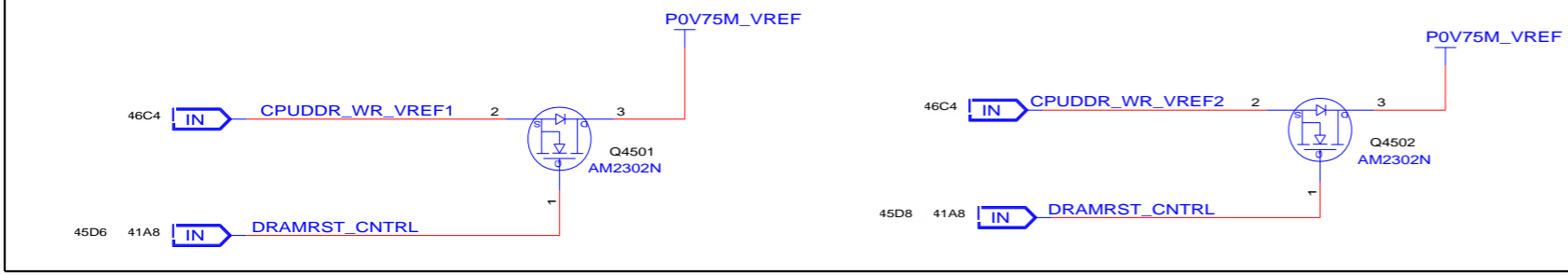
LOTES\_ACA\_ZIF\_069\_P01\_989P

<b>INVENTEC</b>			
TITLE MODEL_PROJECT,FUNCTION Block Diagram			
SIZE C	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV X01
CHANGE by xxx		DATE 21.OCT.2002	
SHEET 44		of 68	

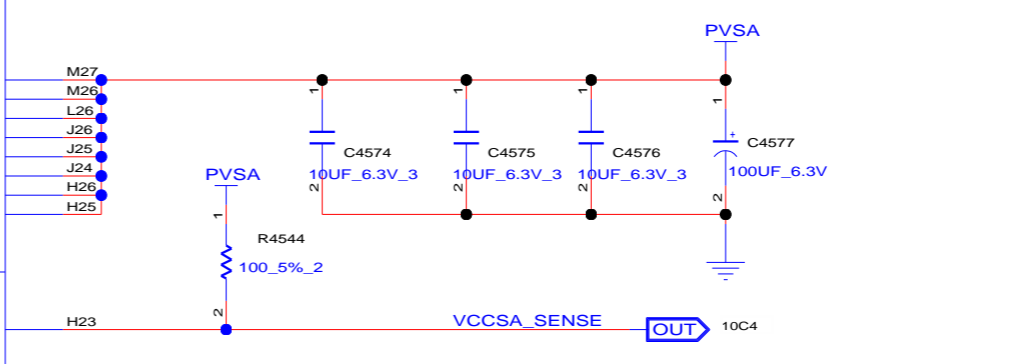
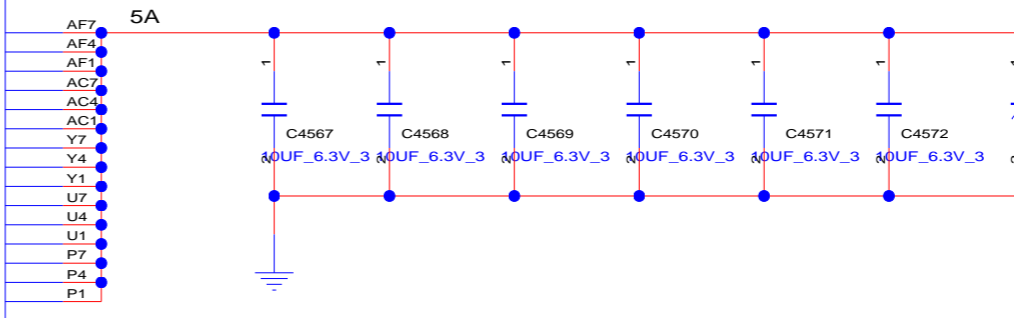
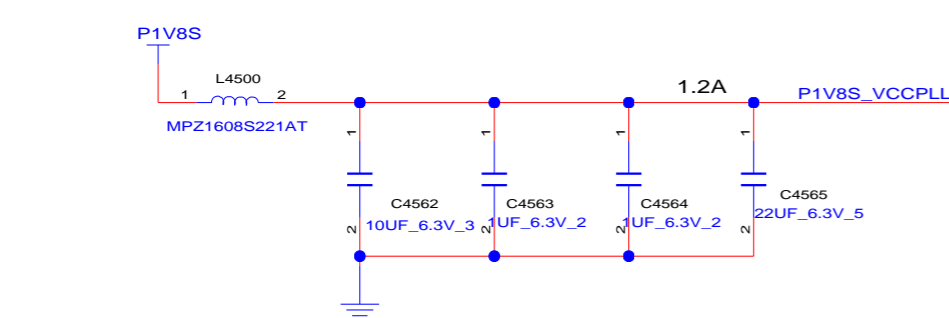
# POWER

PROCESSOR DRIVEN VREF PATH WAS STUFFED BY DEFAULT:

ROUTE WITH MIN. TRACE WIDTH OF 10 MILS



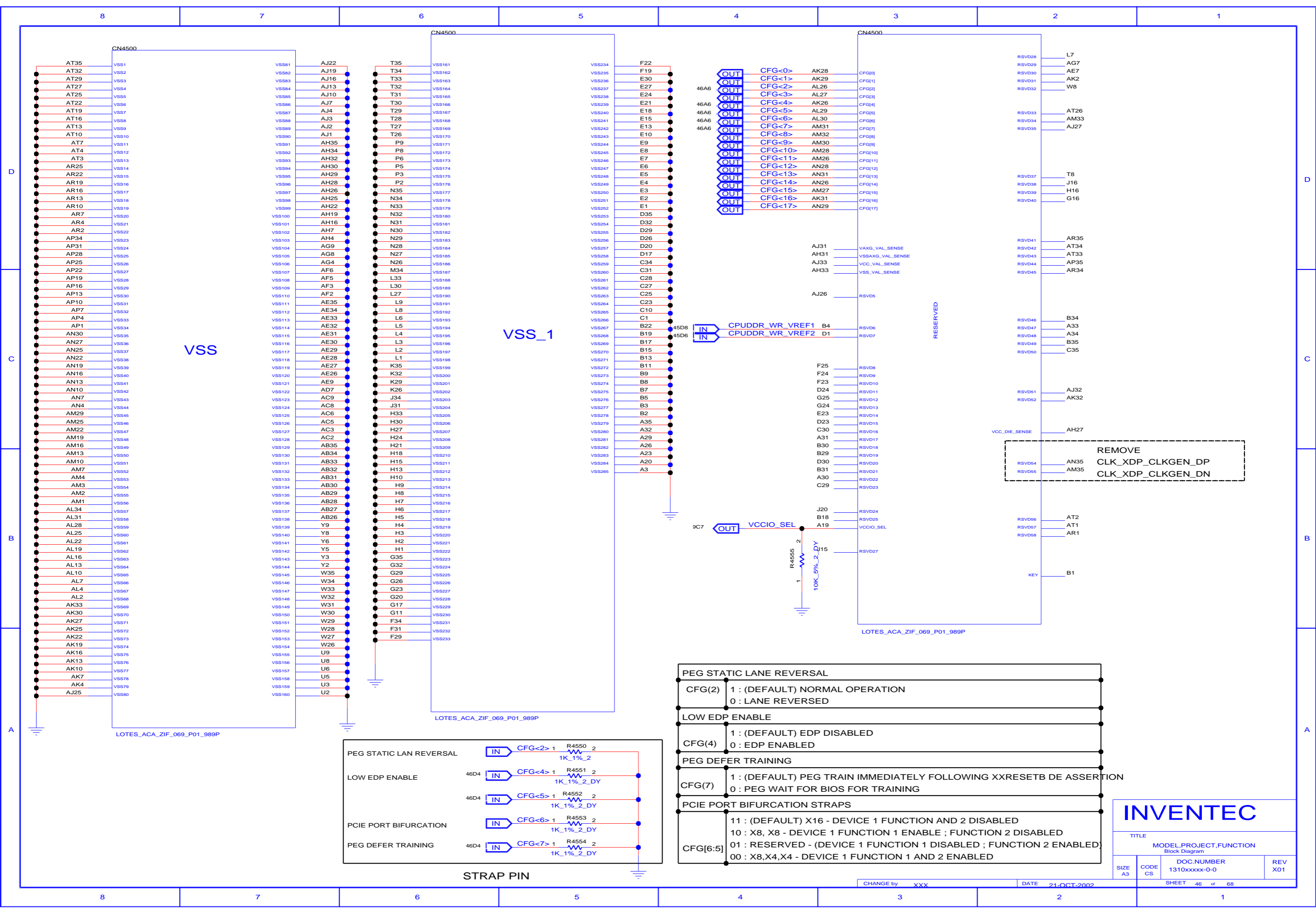
NOTE : DDR\_WR\_VREF SHOULD HAVE 20/20 MIL WHEREVER POSSIBLE



LOTES\_ACA\_ZIF\_069\_P01\_989P

<b>INVENTEC</b>			
TITLE			
MODEL_PROJECT_FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 45 of 68





D

C

B

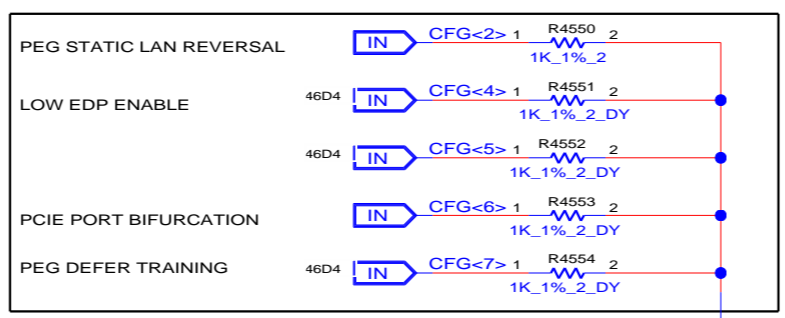
A

D

C

B

A



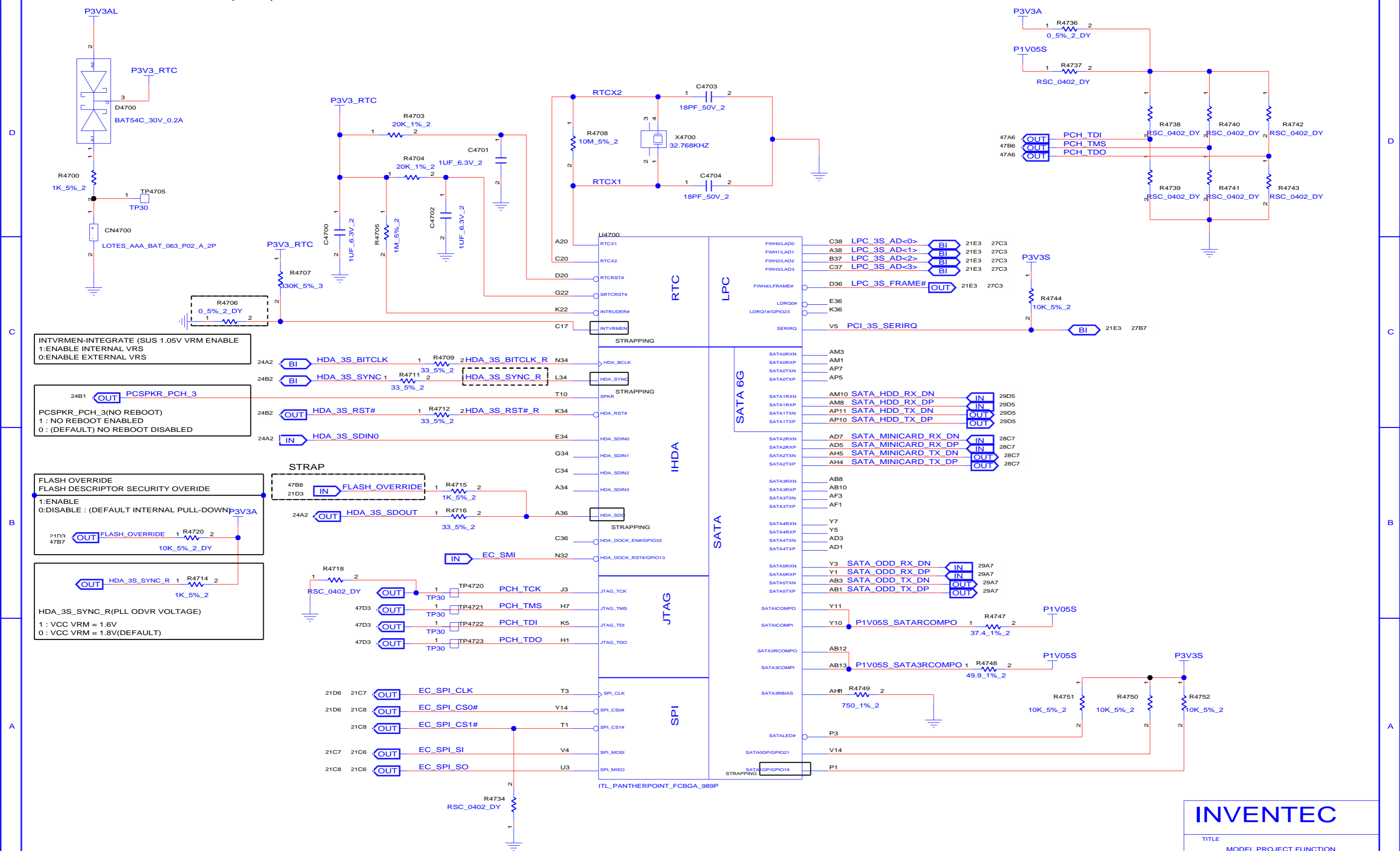
STRAP PIN

- PEG STATIC LANE REVERSAL
  - CFG(2) 1 : (DEFAULT) NORMAL OPERATION
  - 0 : LANE REVERSED
- LOW EDP ENABLE
  - CFG(4) 1 : (DEFAULT) EDP DISABLED
  - 0 : EDP ENABLED
- PEG DEFER TRAINING
  - CFG(7) 1 : (DEFAULT) PEG TRAIN IMMEDIATELY FOLLOWING XXRESETB DE ASSERTION
  - 0 : PEG WAIT FOR BIOS FOR TRAINING
- PCIE PORT BIFURCATION STRAPS
  - CFG[6:5] 11 : (DEFAULT) X16 - DEVICE 1 FUNCTION AND 2 DISABLED
  - 10 : X8, X8 - DEVICE 1 FUNCTION 1 ENABLE ; FUNCTION 2 DISABLED
  - 01 : RESERVED - (DEVICE 1 FUNCTION 1 DISABLED ; FUNCTION 2 ENABLED)
  - 00 : X8,X4,X4 - DEVICE 1 FUNCTION 1 AND 2 ENABLED

REMOVE  
CLK\_XDP\_CLKGEN\_DP  
CLK\_XDP\_CLKGEN\_DN

<b>INVENTEC</b>			
TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
CHANGE by xxx		DATE 21-OCT-2002	
SHEET 46		of 68	

REFERENCE 4700~4949(PCH)



INTVRMEN-INTEGRATE (SUS 1.05V VRM ENABLE)  
 1:ENABLE INTERNAL VRS  
 0:ENABLE EXTERNAL VRS

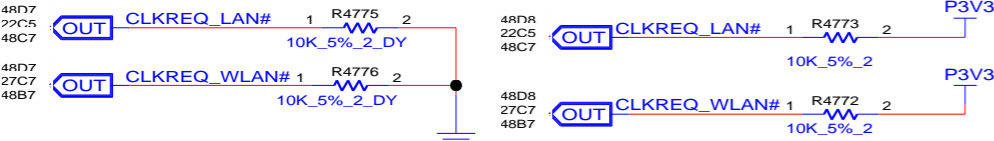
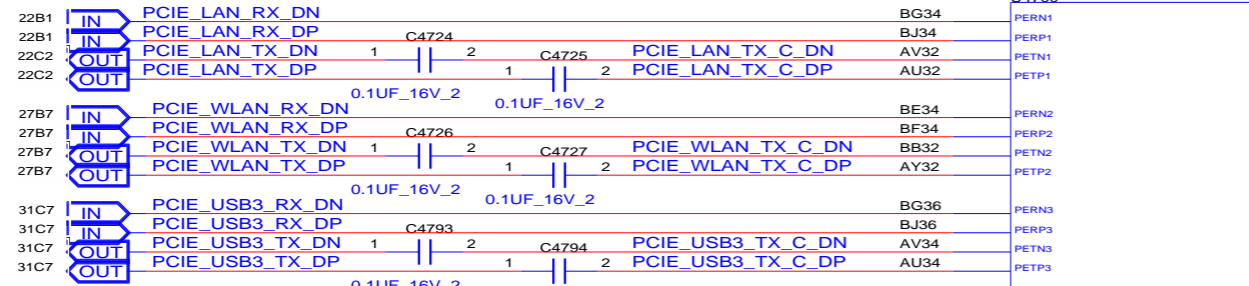
PCSPKR\_PCH\_3(NO REBOOT)  
 1 : NO REBOOT ENABLED  
 0 : (DEFAULT) NO REBOOT DISABLED

FLASH OVERRIDE  
 FLASH DESCRIPTOR SECURITY OVERRIDE  
 1:ENABLE  
 0:DISABLE : (DEFAULT INTERNAL PULL-DOWN)

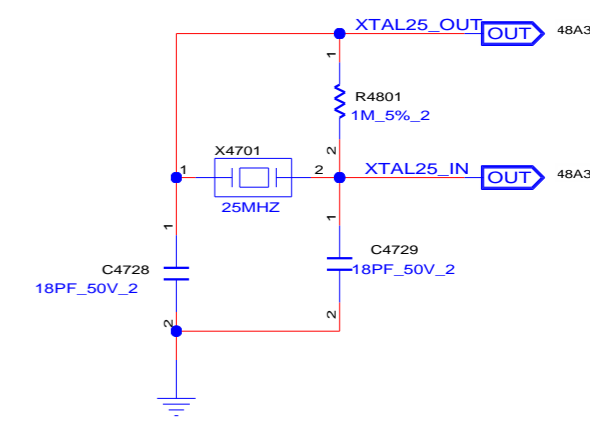
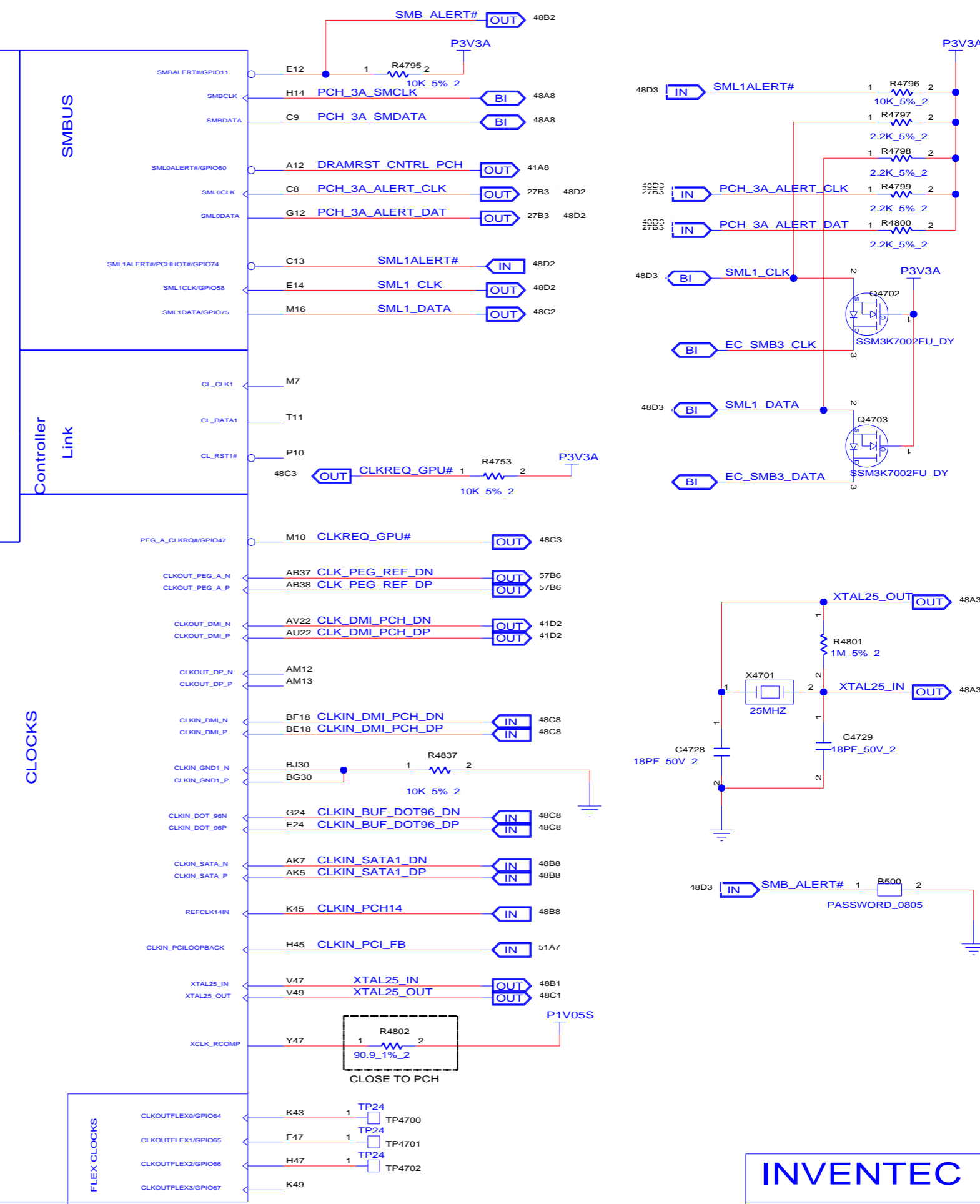
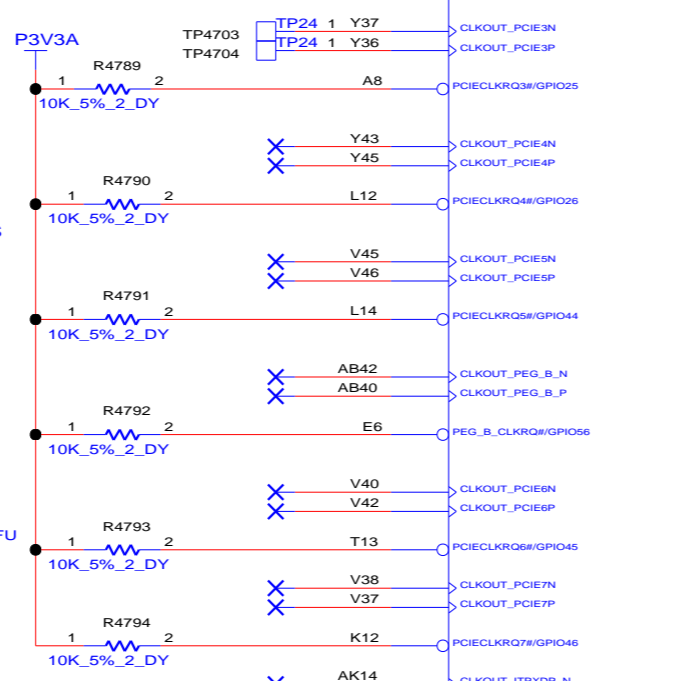
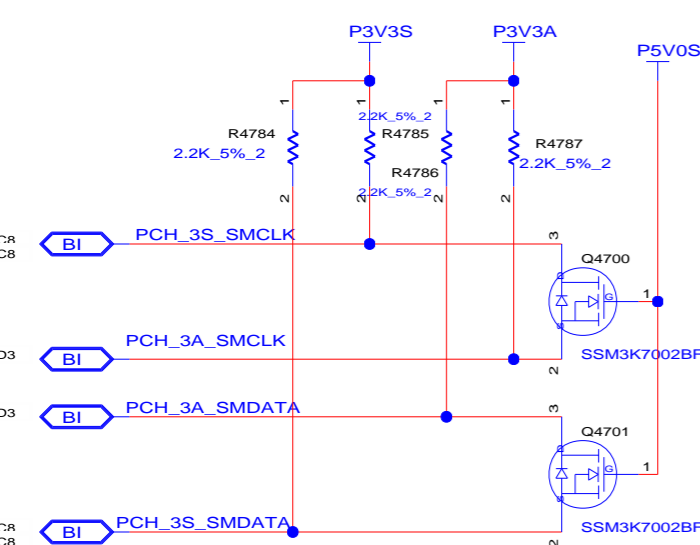
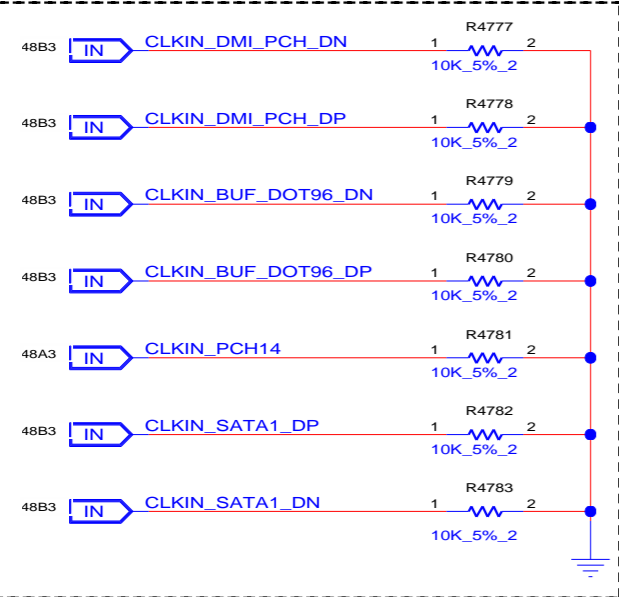
HDA\_3S\_SYNC\_R(PLL ODVR VOLTAGE)  
 1 : VCC VRM = 1.6V  
 0 : VCC VRM = 1.8V(DEFAULT)

<b>INVENTEC</b>			
TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01

REFERENCE 4700-4949(PCH)



CLOCK TERMINATION FOR FICM STUFF FOR INTEGRATED CLK



**INVENTEC**

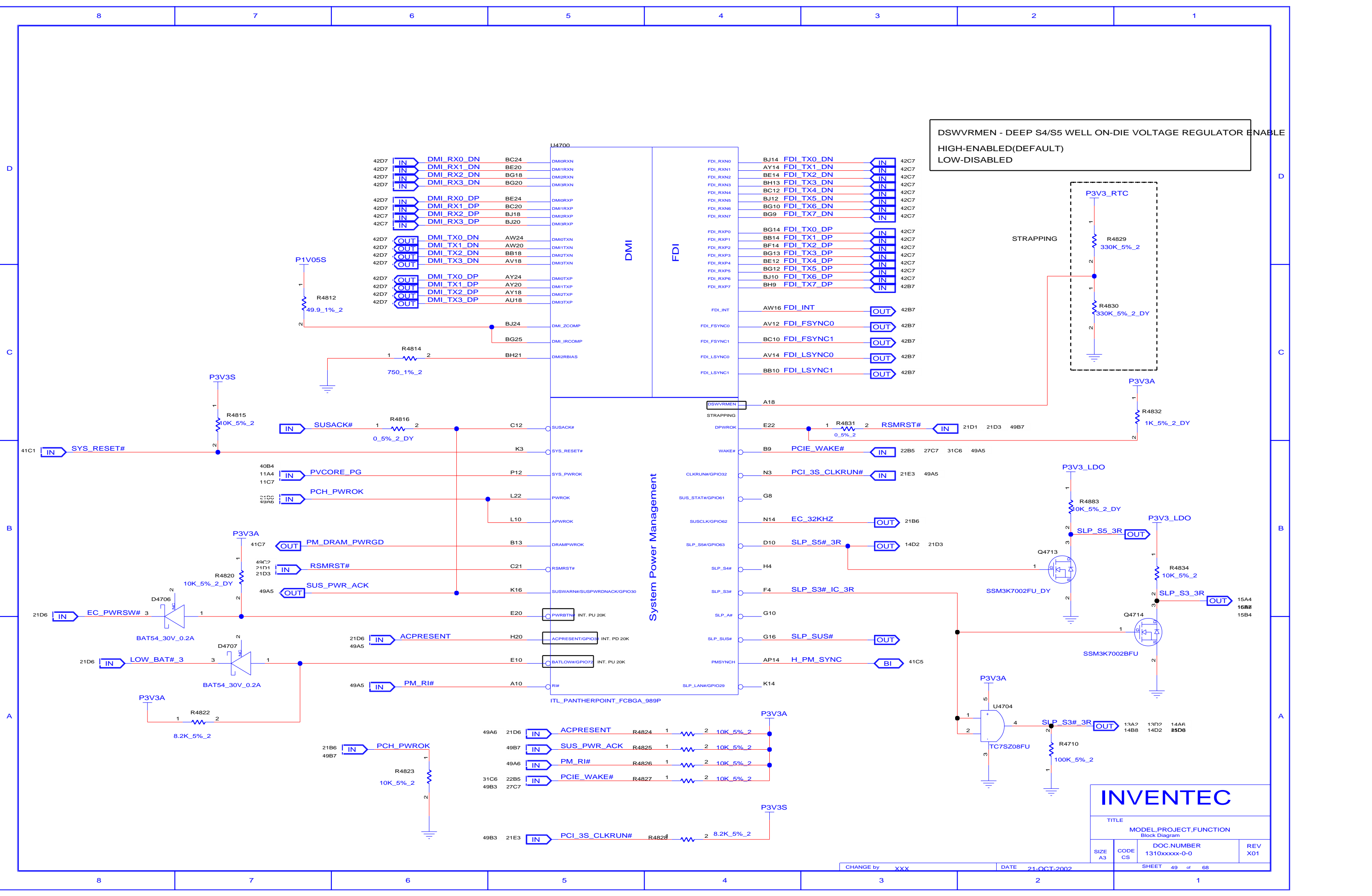
TITLE: MODEL\_PROJECT\_FUNCTION  
Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
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CHANGE by: xxx DATE: 21-OCT-2002 SHEET 48 of 68

ITL\_PANTHERPOINT\_FCBGA\_989P

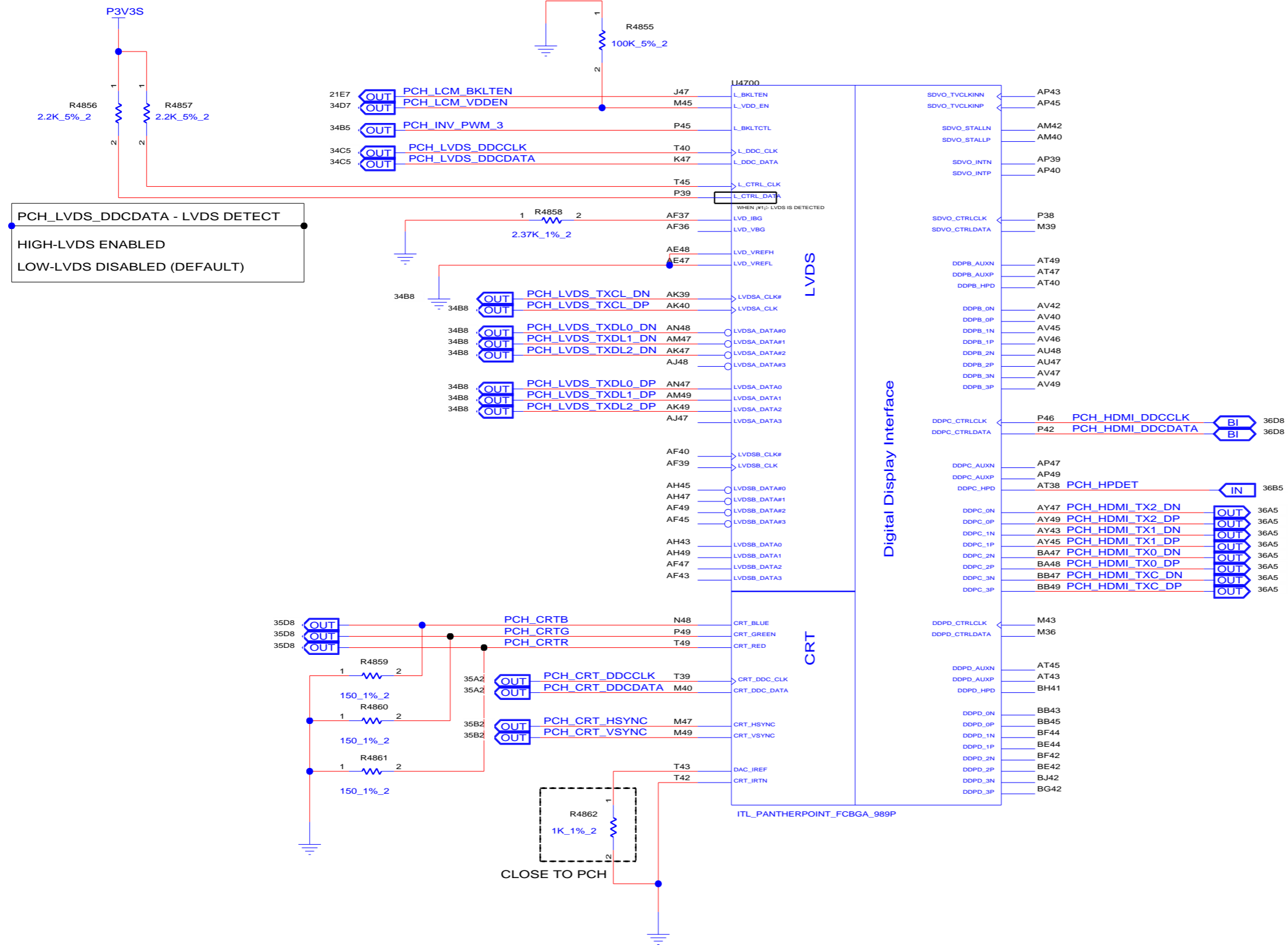




DSWVRMEN - DEEP S4/S5 WELL ON-DIE VOLTAGE REGULATOR ENABLE  
HIGH-ENABLED(DEFAULT)  
LOW-DISABLED

System Power Management

<b>INVENTEC</b>			
TITLE MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01



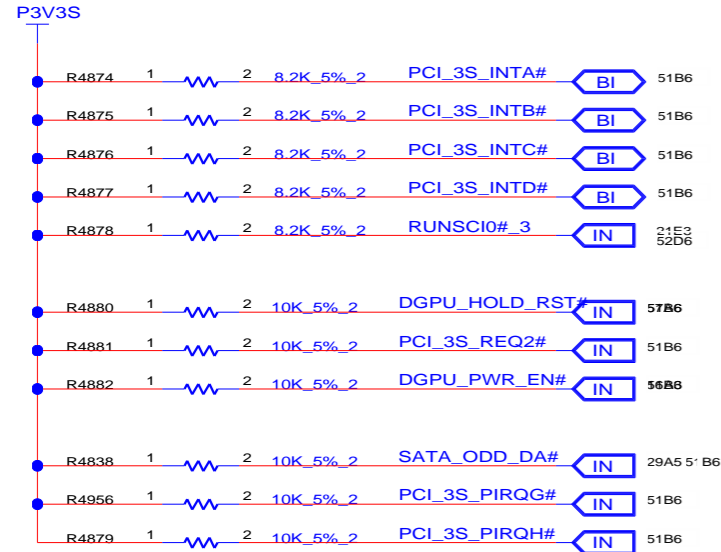
**INVENTEC**

TITLE  
MODEL\_PROJECT\_FUNCTION  
Block Diagram

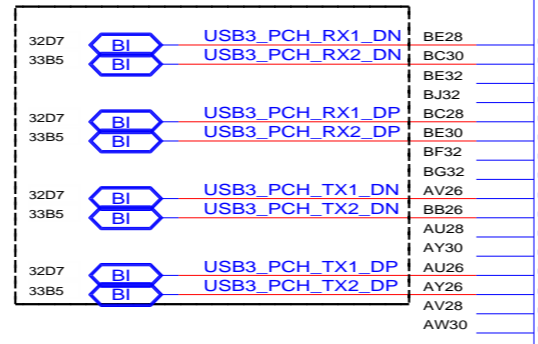
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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REFERENCE 4700~4949(PCH)

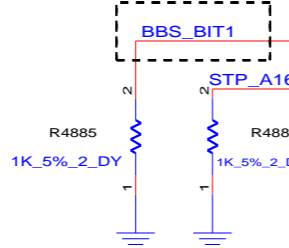
GPIO51 BBS_BIT1	GPIO19 BBS_BIT0	BOOT BIOS DESTINATION
0	1	RESERVED(NAND)
1	0	-----
1	1	SPI (DEFAULT)
0	0	LPC



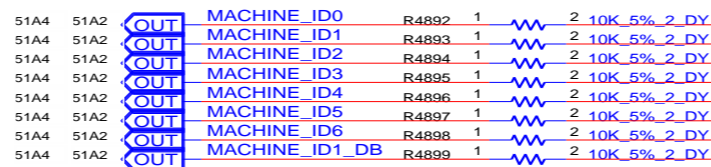
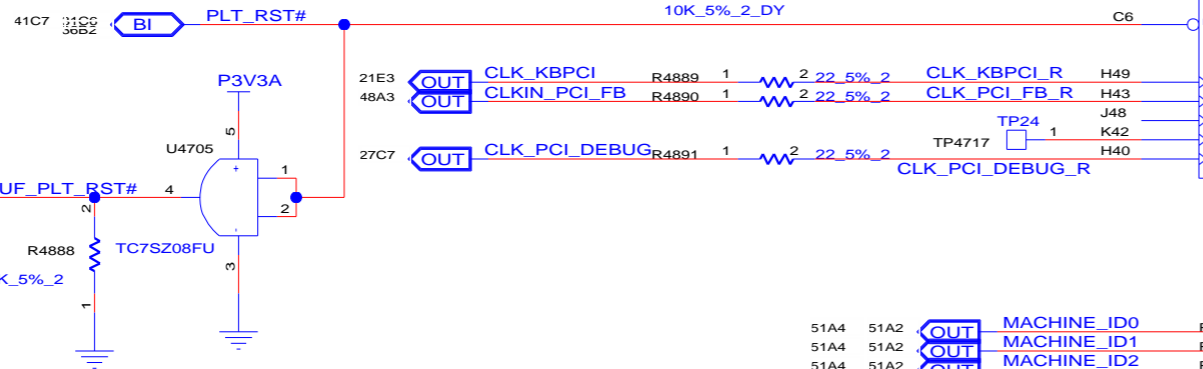
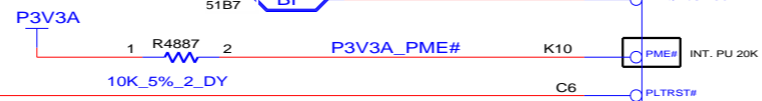
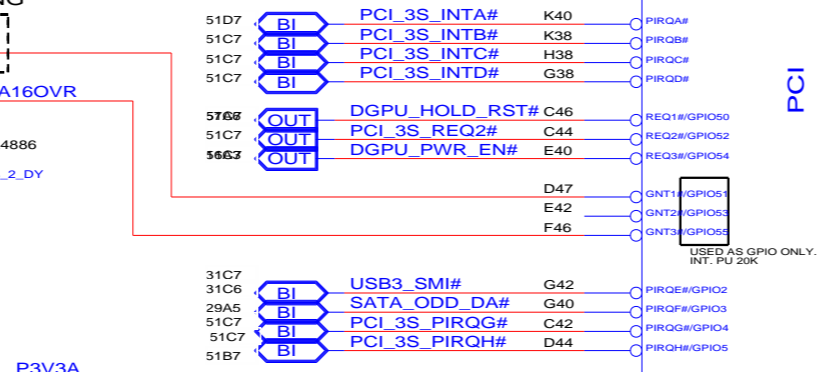
ROUTE WITH 90 OHMS IMPEDANCE  
TOTAL LENGTH NO LONGER THAN 11 INCHES



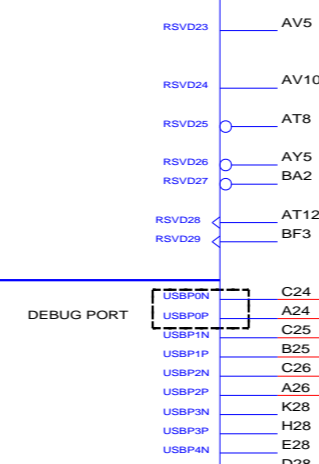
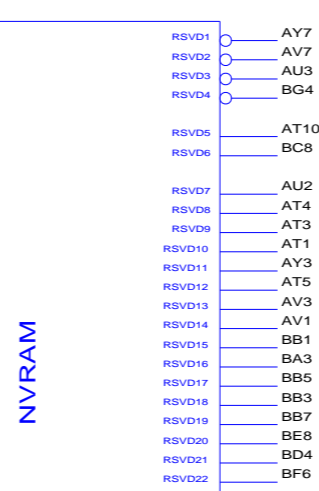
BBS STRAPING



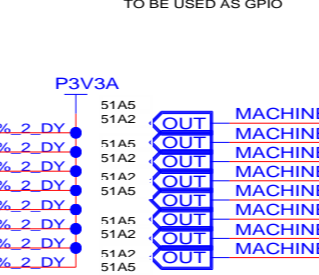
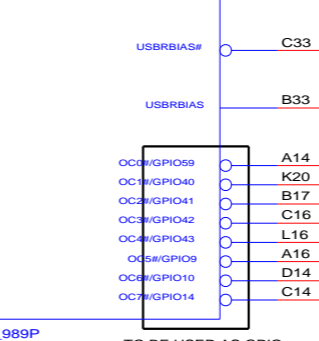
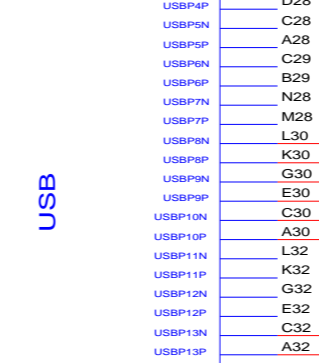
LOW=A16 SWAP OVERRIDE  
STP\_A16OVR  
TOP-BLOCK SWAP OVERRIDE  
HIGH=DEFAULT



NOTE:10K\_5%(60130B1030ZT)



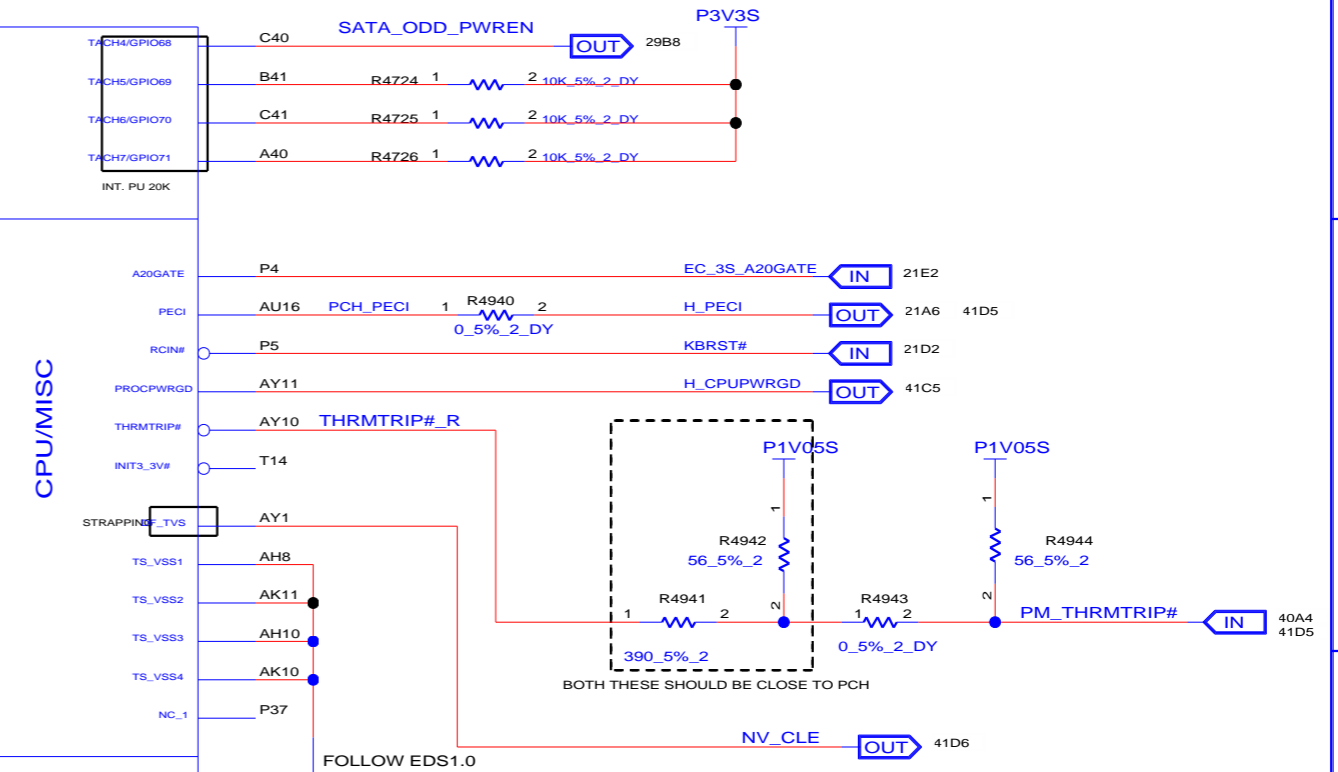
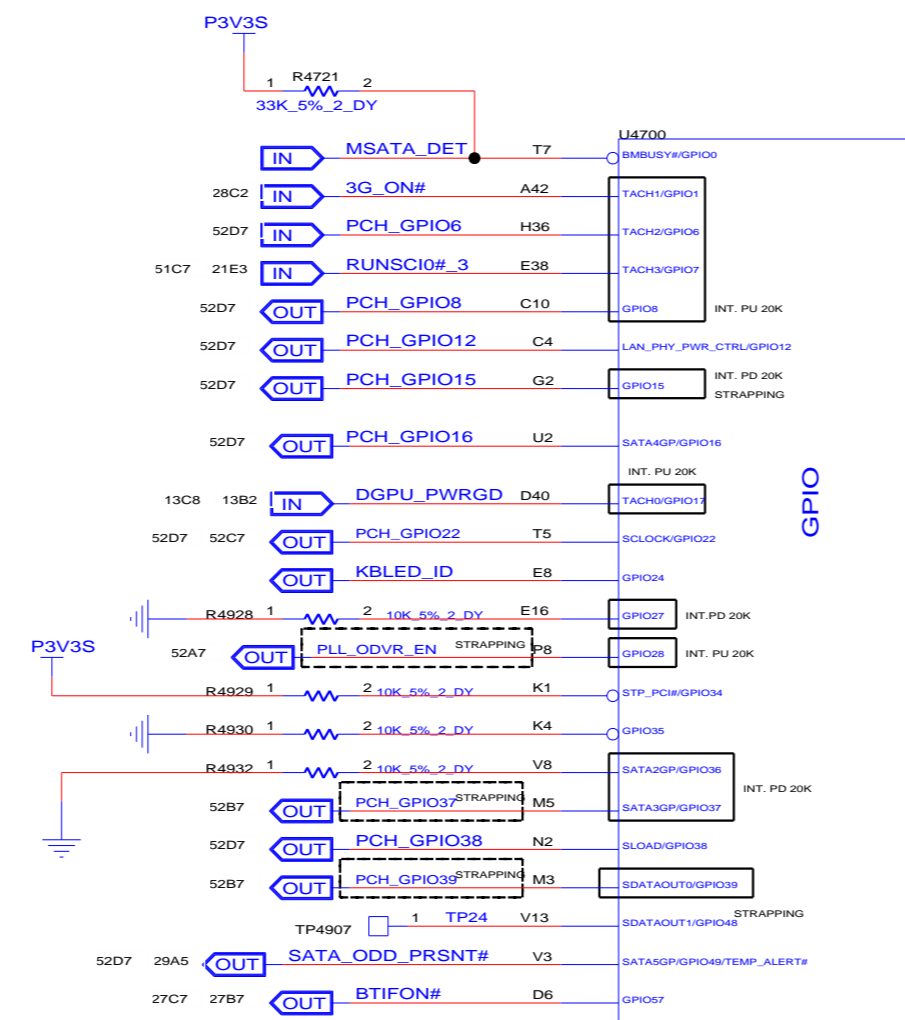
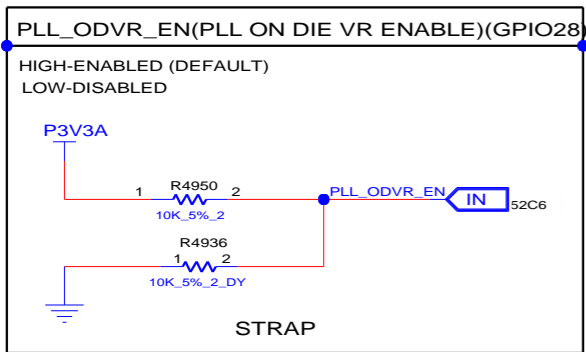
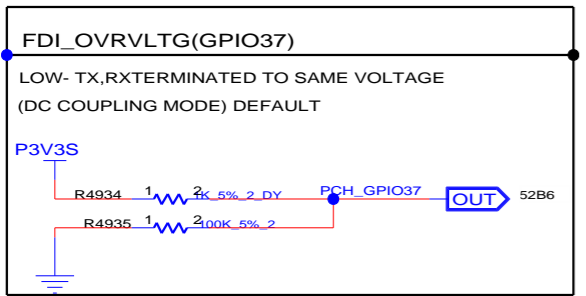
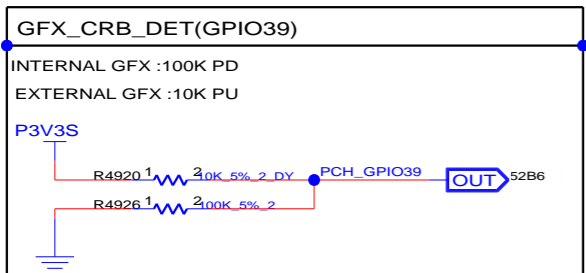
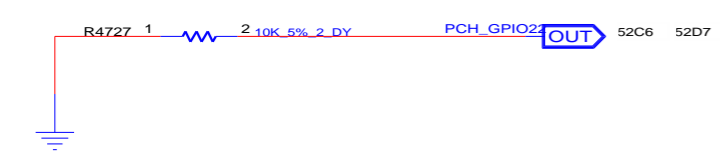
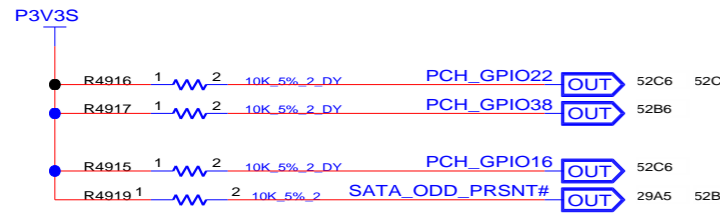
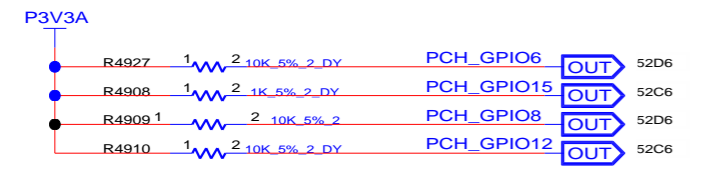
NOTE:  
USB2.0/3.0 COMBO-USB2.0 PORT 0,1 MAPPED USB3.0 PORT 1,2



NOTE:10K\_5%(60130B1030ZT)



TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01

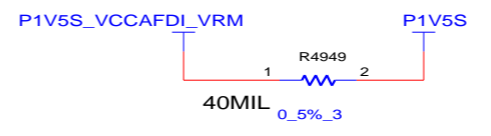
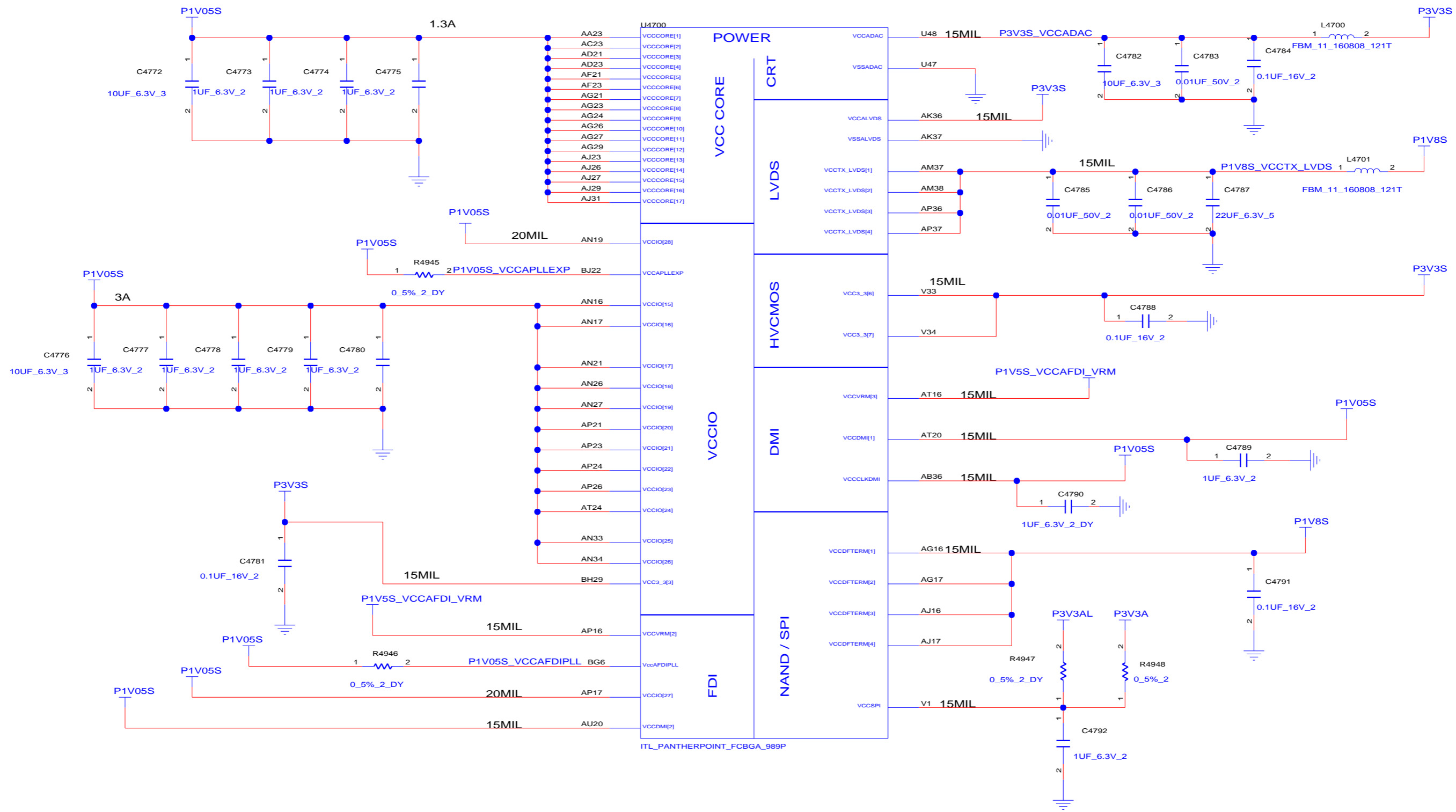


- NCTF**
- VSS\_NCTF\_1 A4
  - VSS\_NCTF\_2 A44
  - VSS\_NCTF\_3 A45
  - VSS\_NCTF\_4 A46
  - VSS\_NCTF\_5 A5
  - VSS\_NCTF\_6 A6
  - VSS\_NCTF\_7 B3
  - VSS\_NCTF\_8 B47
  - VSS\_NCTF\_9 BD1
  - VSS\_NCTF\_10 BD49
  - VSS\_NCTF\_11 BE1
  - VSS\_NCTF\_12 BE49
  - VSS\_NCTF\_13 BF1
  - VSS\_NCTF\_14 BF49
  - VSS\_NCTF\_15 BG2
  - VSS\_NCTF\_16 BG48
  - VSS\_NCTF\_17 BH3
  - VSS\_NCTF\_18 BH47
  - VSS\_NCTF\_19 BJ4
  - VSS\_NCTF\_20 BJ44
  - VSS\_NCTF\_21 BJ45
  - VSS\_NCTF\_22 BJ46
  - VSS\_NCTF\_23 BJ5
  - VSS\_NCTF\_24 BJ6
  - VSS\_NCTF\_25 C2
  - VSS\_NCTF\_26 C48
  - VSS\_NCTF\_27 D1
  - VSS\_NCTF\_28 D49
  - VSS\_NCTF\_29 E1
  - VSS\_NCTF\_30 E49
  - VSS\_NCTF\_31 F1
  - VSS\_NCTF\_32 F49

ITL\_PANTHERPOINT\_FCBGA\_989P

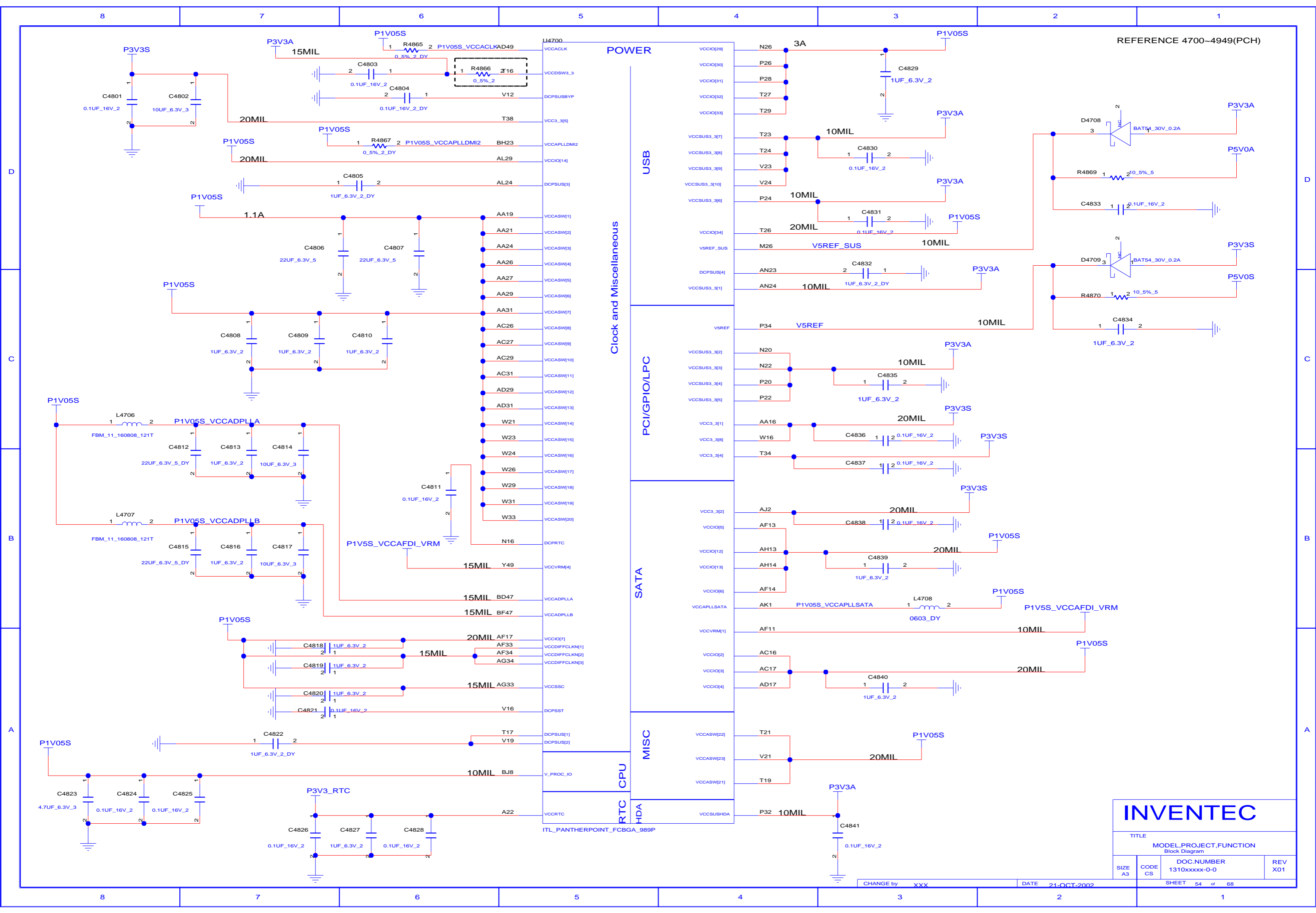
<b>INVENTEC</b>			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 52 of 68

REFERENCE 4700~4949(PCH)



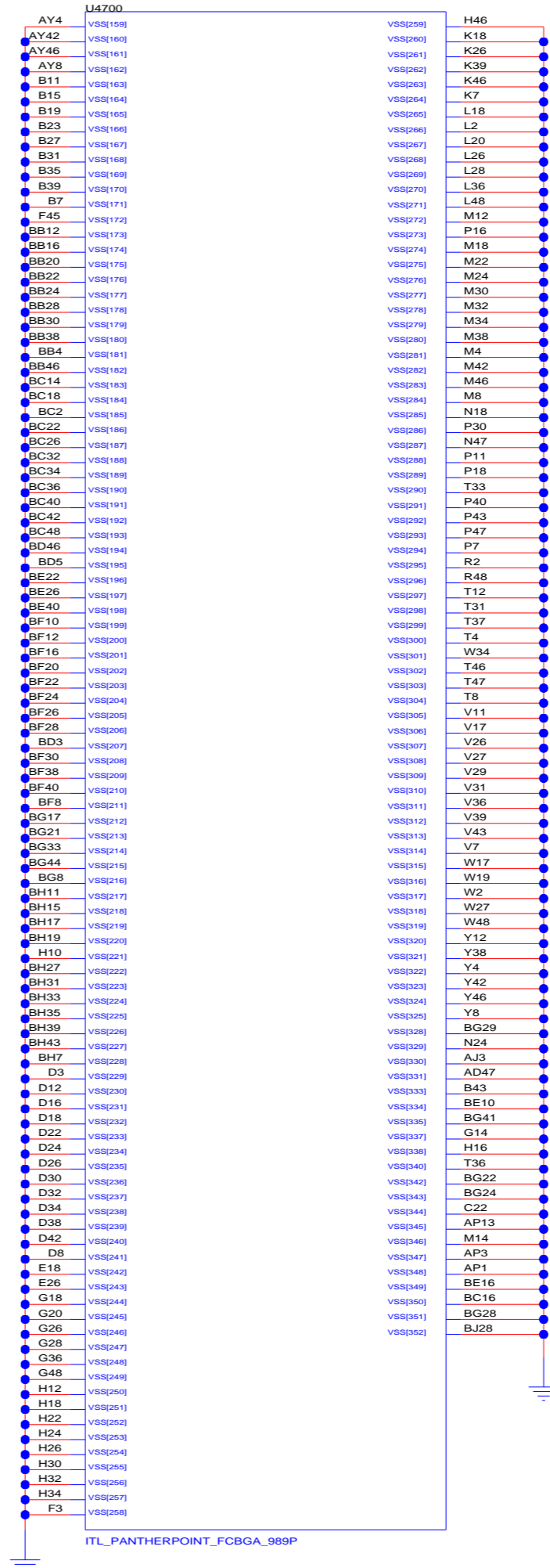
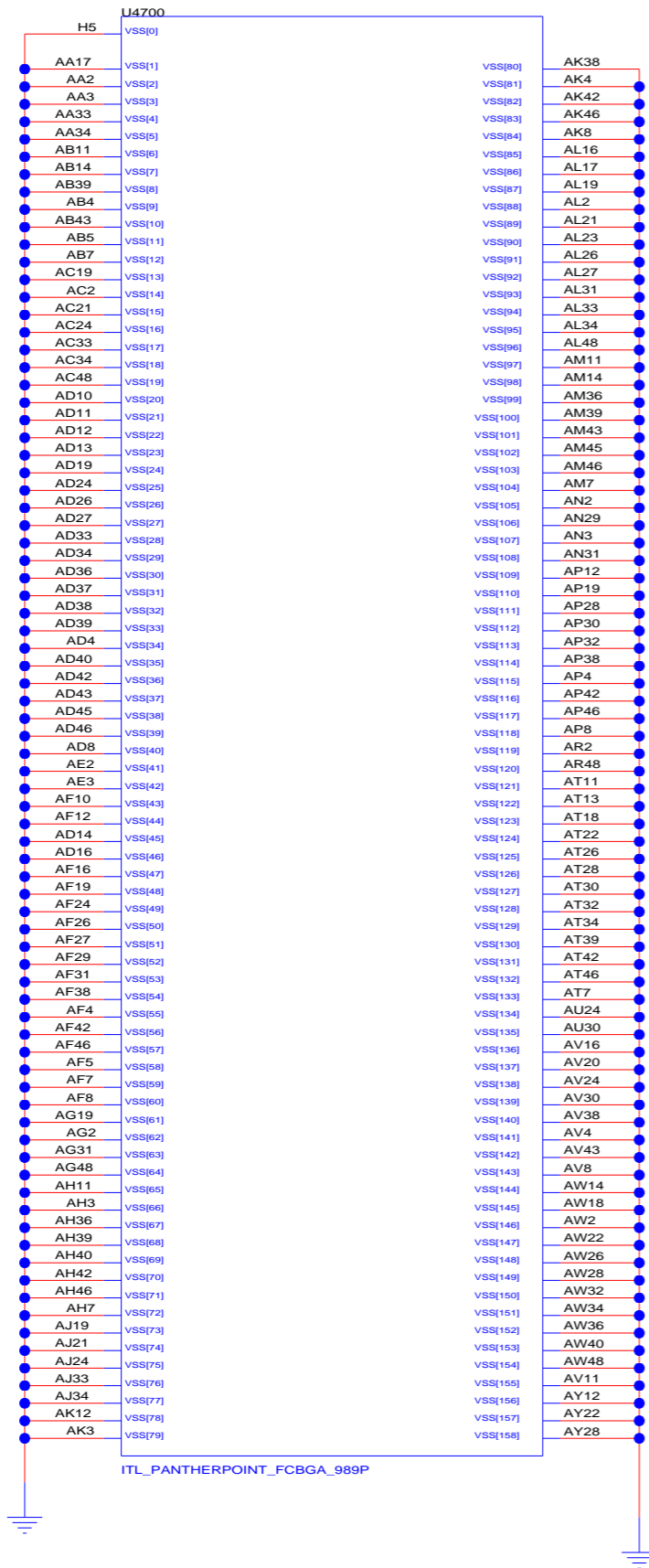
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TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 53 of 68



<b>INVENTEC</b>			
TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	SHEET 54 of 68

REFERENCE 4700-4949(PCH)



**INVENTEC**

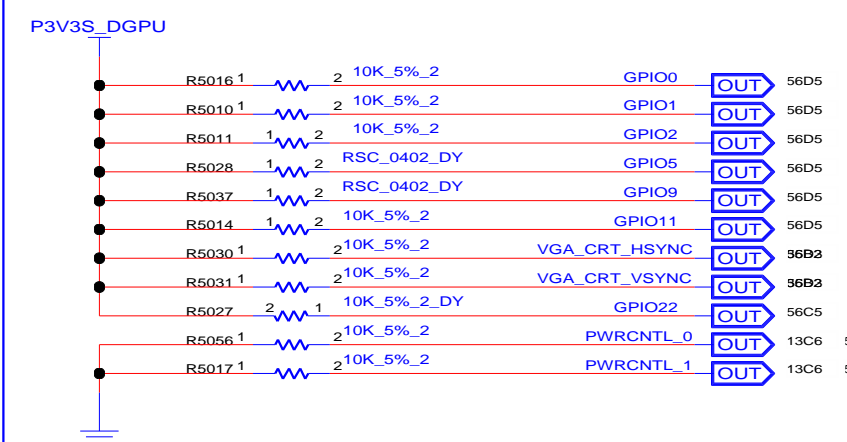
TITLE  
MODEL\_PROJECT\_FUNCTION  
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by XXX DATE 21-OCT-2002 SHEET 55 of 68

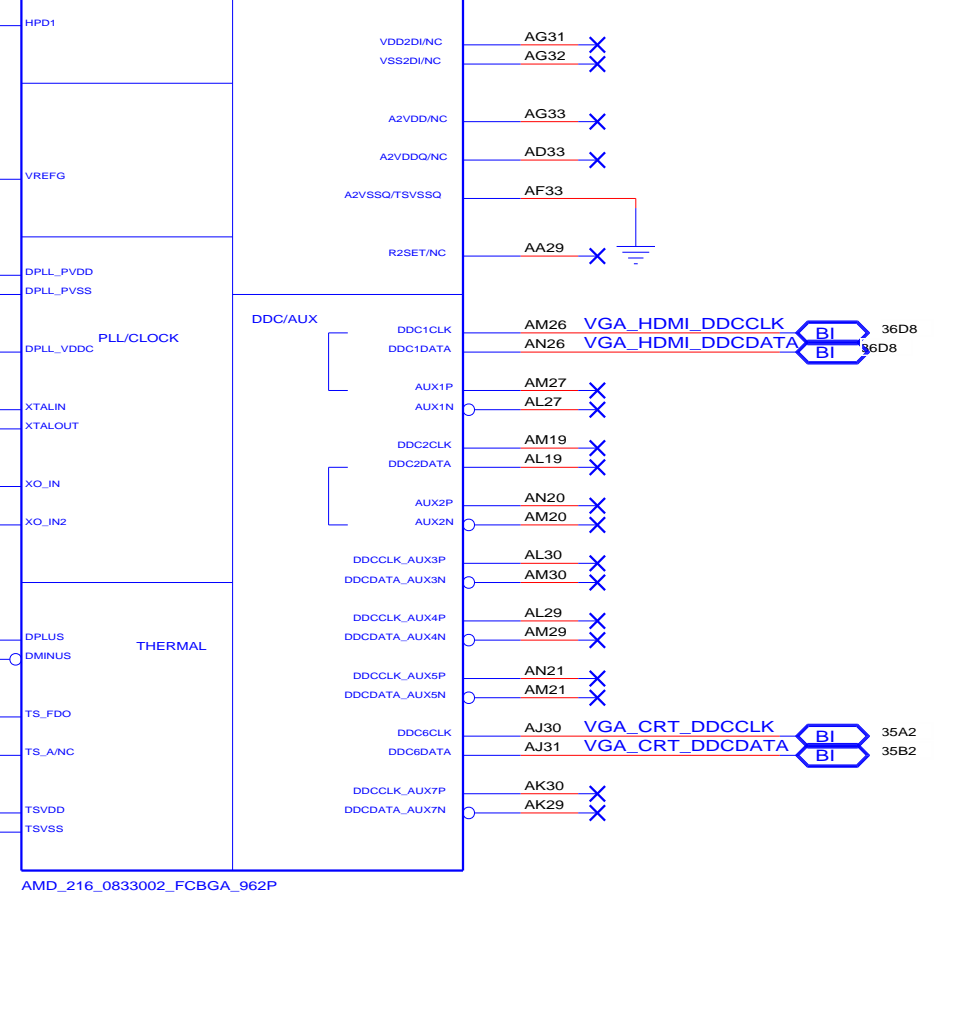
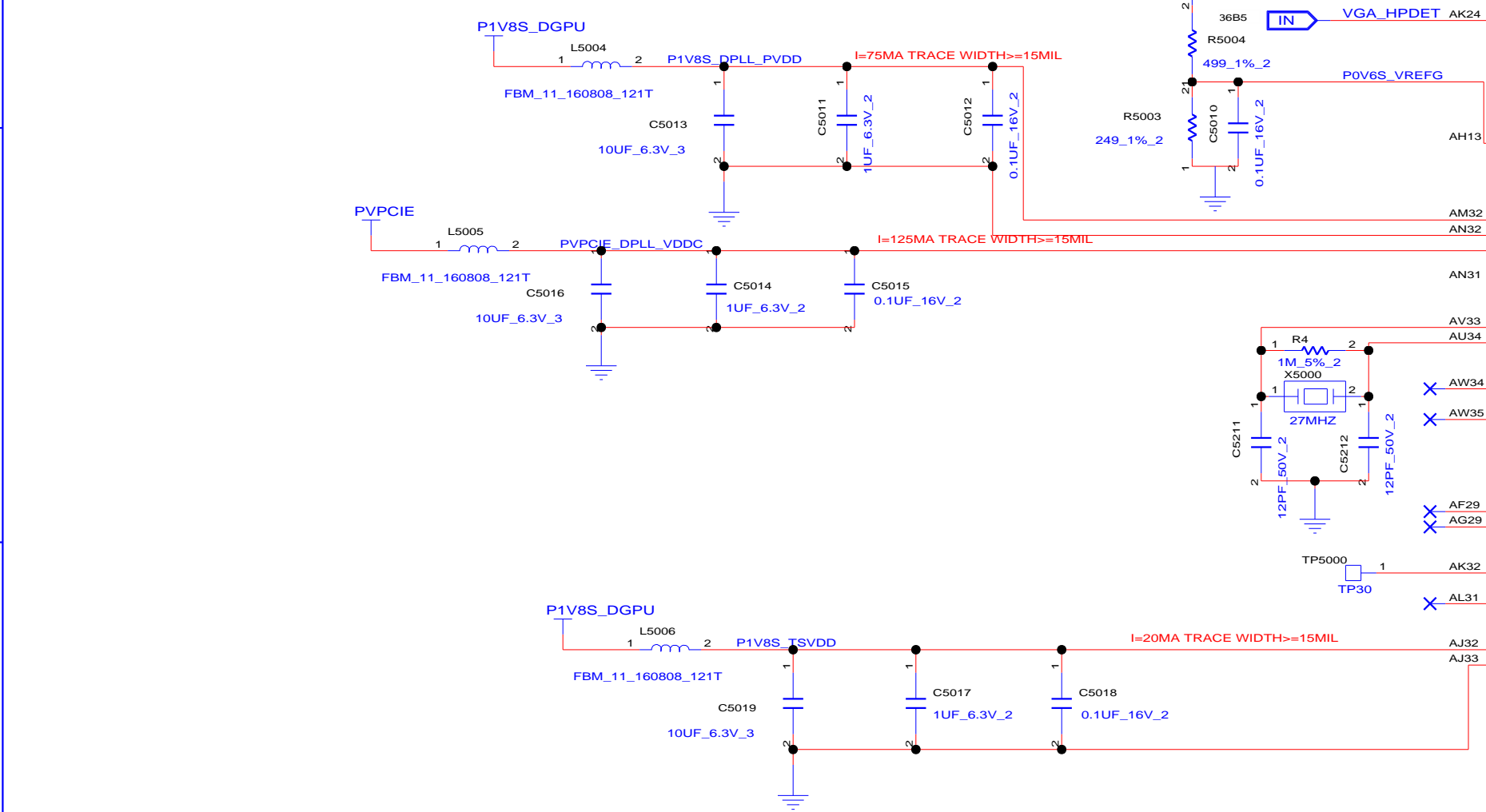
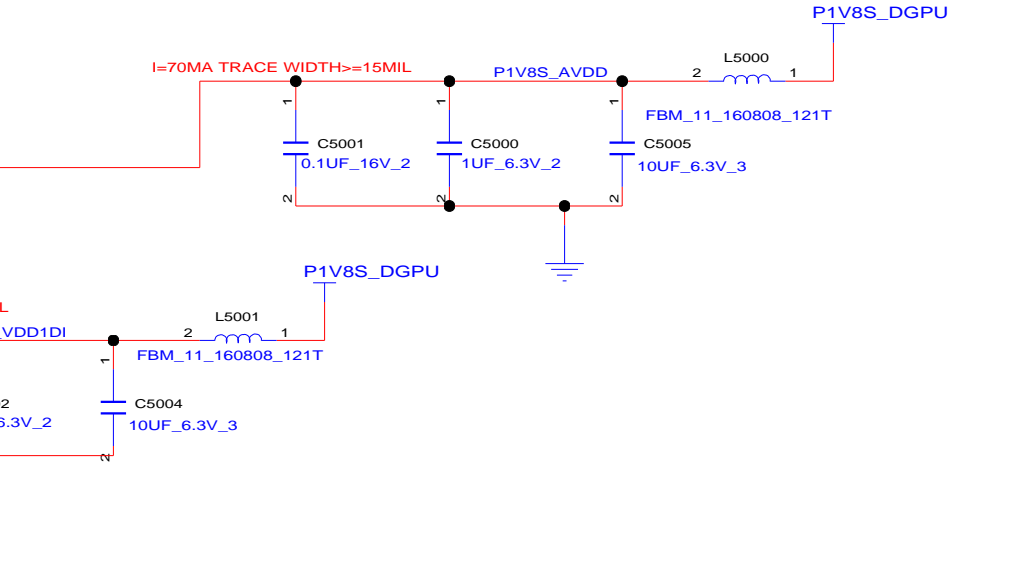
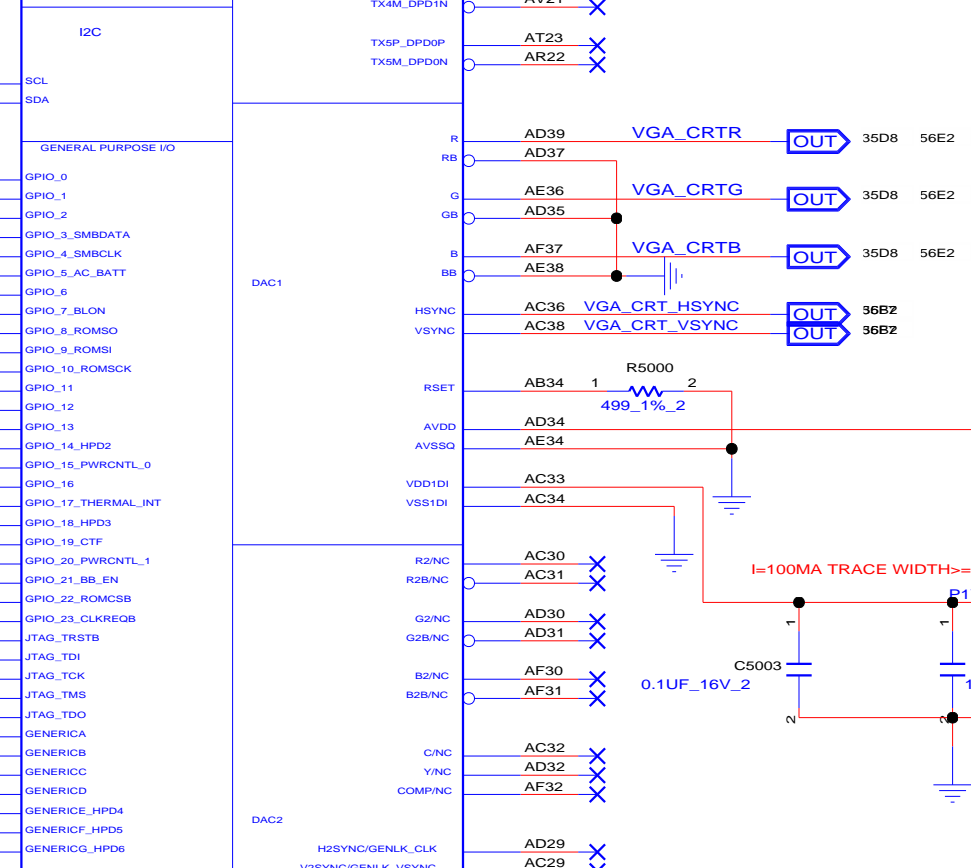
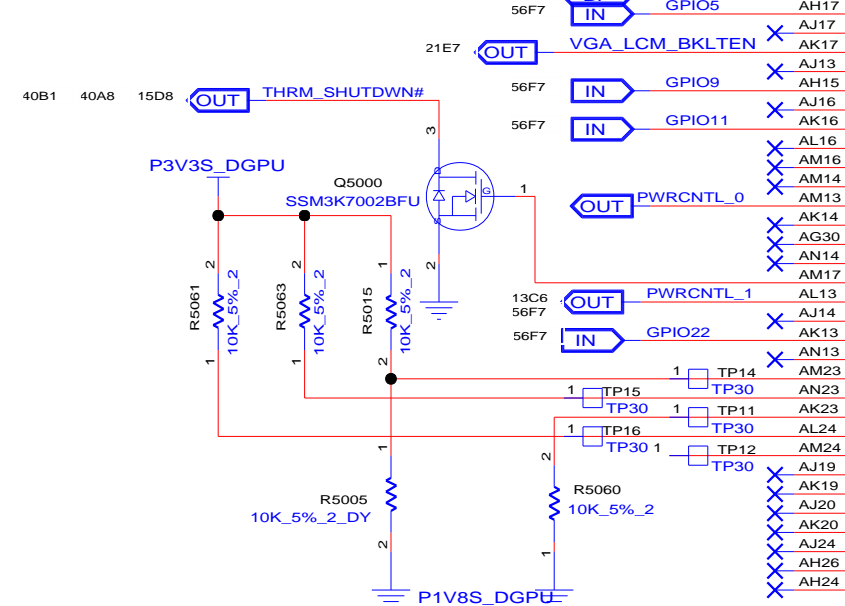
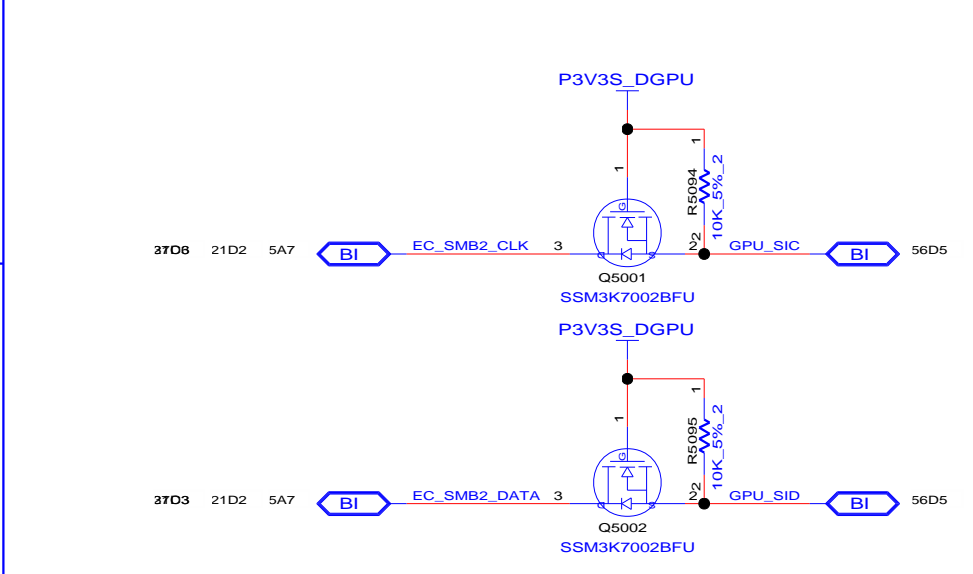
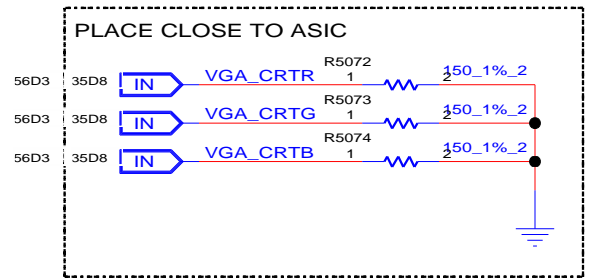
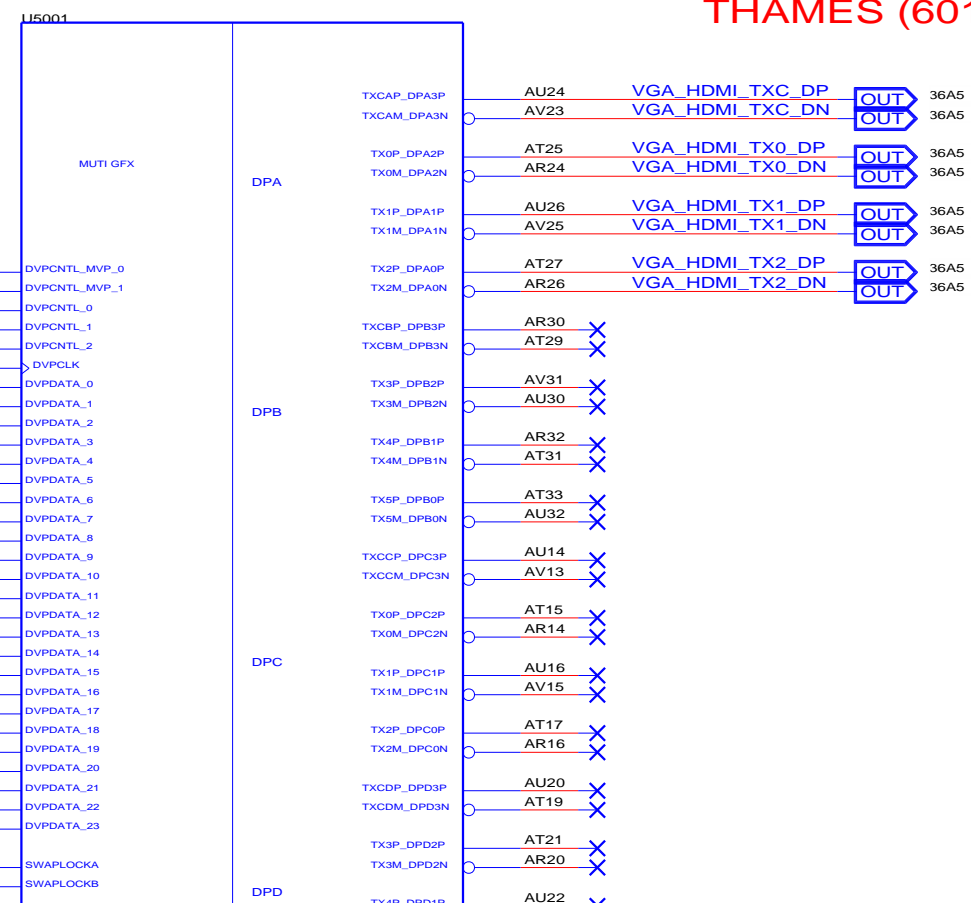
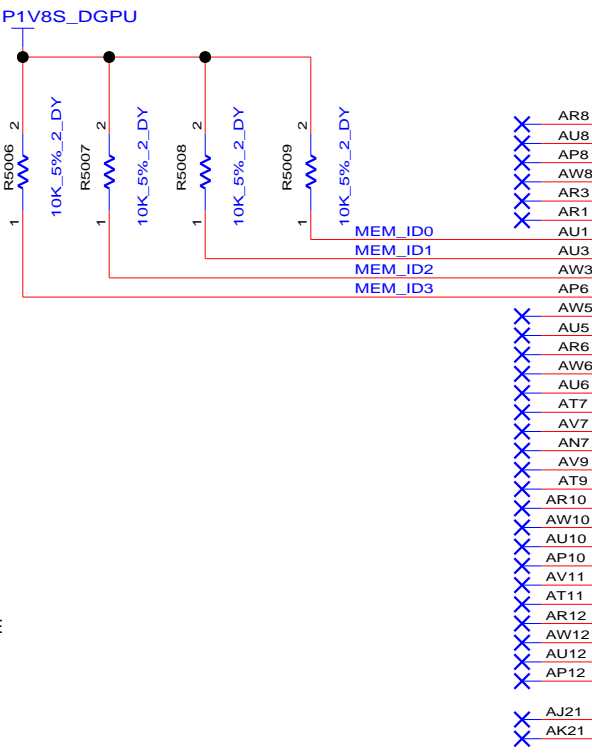


THAMES (6019B0917601)



PIN BASE STRAPS																					
GPIO_0	TRANSMITTER POWER SAVING ENABLE 0 : 50% TX OUTPUT SWING (DEFAULT) 1 : FULL TX OUTPUT SWING																				
GPIO_1	PCIE TRANSMITTER DE-EMPHASIS 0 : DE-EMPHASIS DISABLED (DEFAULT) 1 : DE-EMPHASIS ENABLED																				
GPIO_2	GEN1/GEN2 ENABLE 0 : GEN1 (DEFAULT) 1 : GEN2																				
GPIO_8 GPIO_21	MUST BE LOW DURING RESET LEFT UNCONNECTED																				
GPIO_9	VGA DISABLE 0 : ENABLE (DEFAULT) 1 : DISABLE																				
GPIO_[11:13]	MEMORY APERTURE SIZE																				
	<table border="1"> <thead> <tr> <th>GPIO_13</th> <th>GPIO_12</th> <th>GPIO_11</th> <th>MEMORY APERTURE SIZE</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>0</td> <td>128M</td> </tr> <tr> <td>0</td> <td>0</td> <td>1</td> <td>256M</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> <td>64M</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> <td>32M</td> </tr> </tbody> </table>	GPIO_13	GPIO_12	GPIO_11	MEMORY APERTURE SIZE	0	0	0	128M	0	0	1	256M	0	1	0	64M	0	1	1	32M
GPIO_13	GPIO_12	GPIO_11	MEMORY APERTURE SIZE																		
0	0	0	128M																		
0	0	1	256M																		
0	1	0	64M																		
0	1	1	32M																		
GPIO_22	ENABLE EXTERNAL BIOS ROM DEVICE 0 : DISABLE (DEFAULT) 1 : ENABLE																				
HSYNC[1] VSYNC[0]	AUDIO[1:0] 00 : NO AUDIO FUNCTION 01 : AUDIO FOR DP ONLY 10 : AUDIO FOR DP AND HDMI IF DONGLE IS DETECTED 11 : AUDIO FOR BOTH DP AND HDMI																				

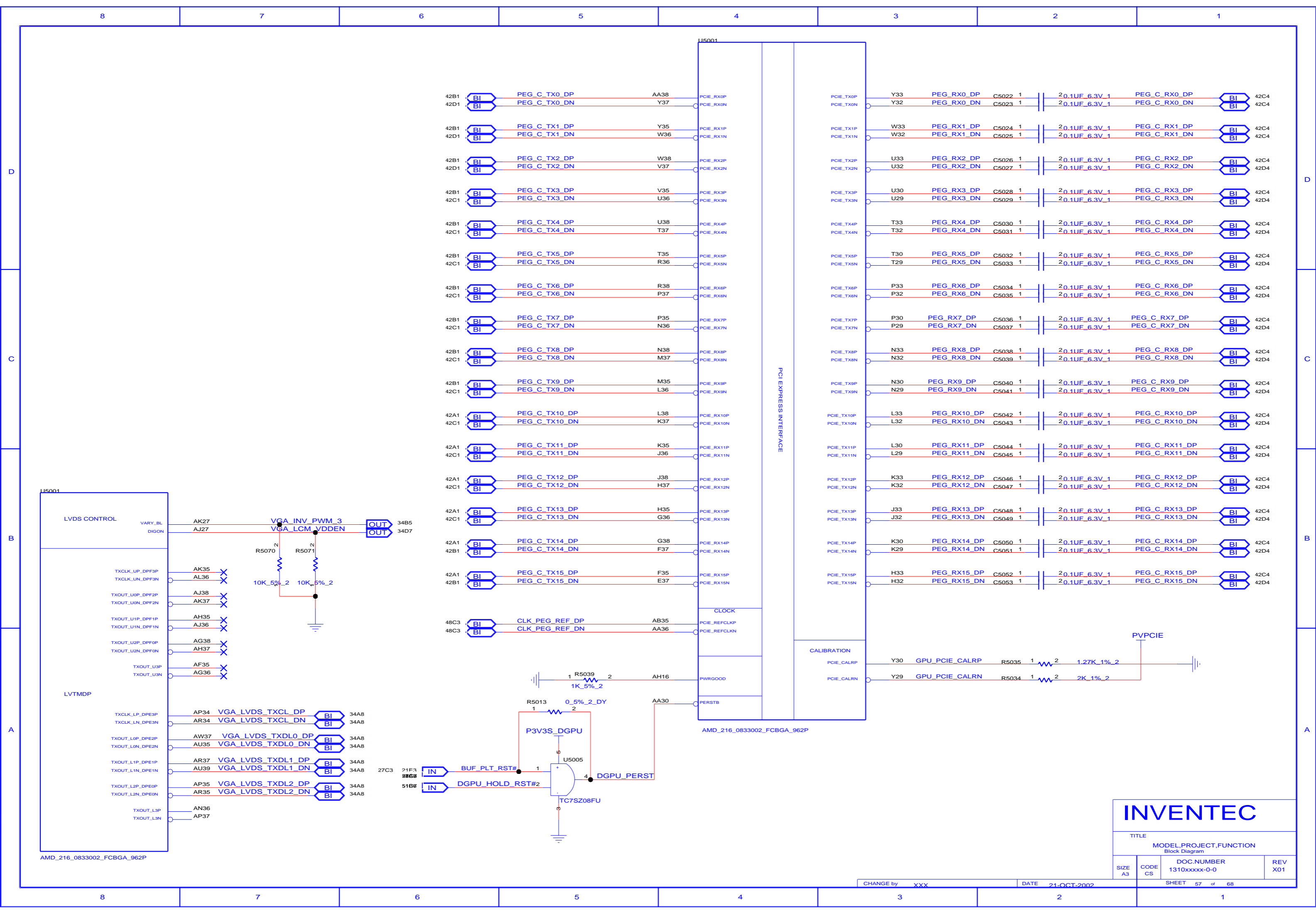
MEM_ID3	MEM_ID2	MEM_ID1	MEM_ID0	HYNIX	SAMSUNG
0	0	0	0	0	0
0	1	0	0	0	0



INVENTEC

TITLE			
MODEL_PROJECT.FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxx-0-0	X01
SHEET		56	of 68





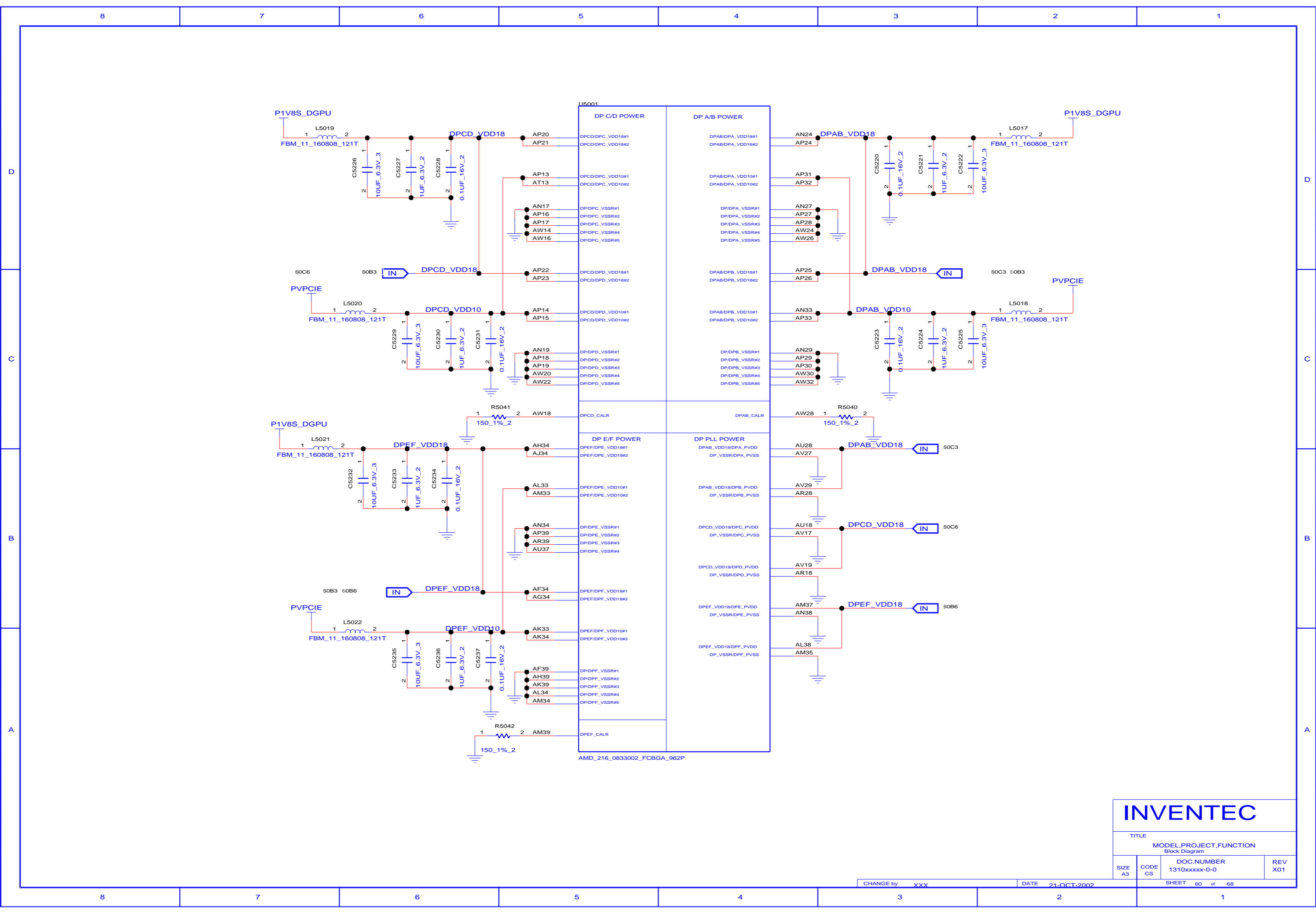
# INVENTEC

TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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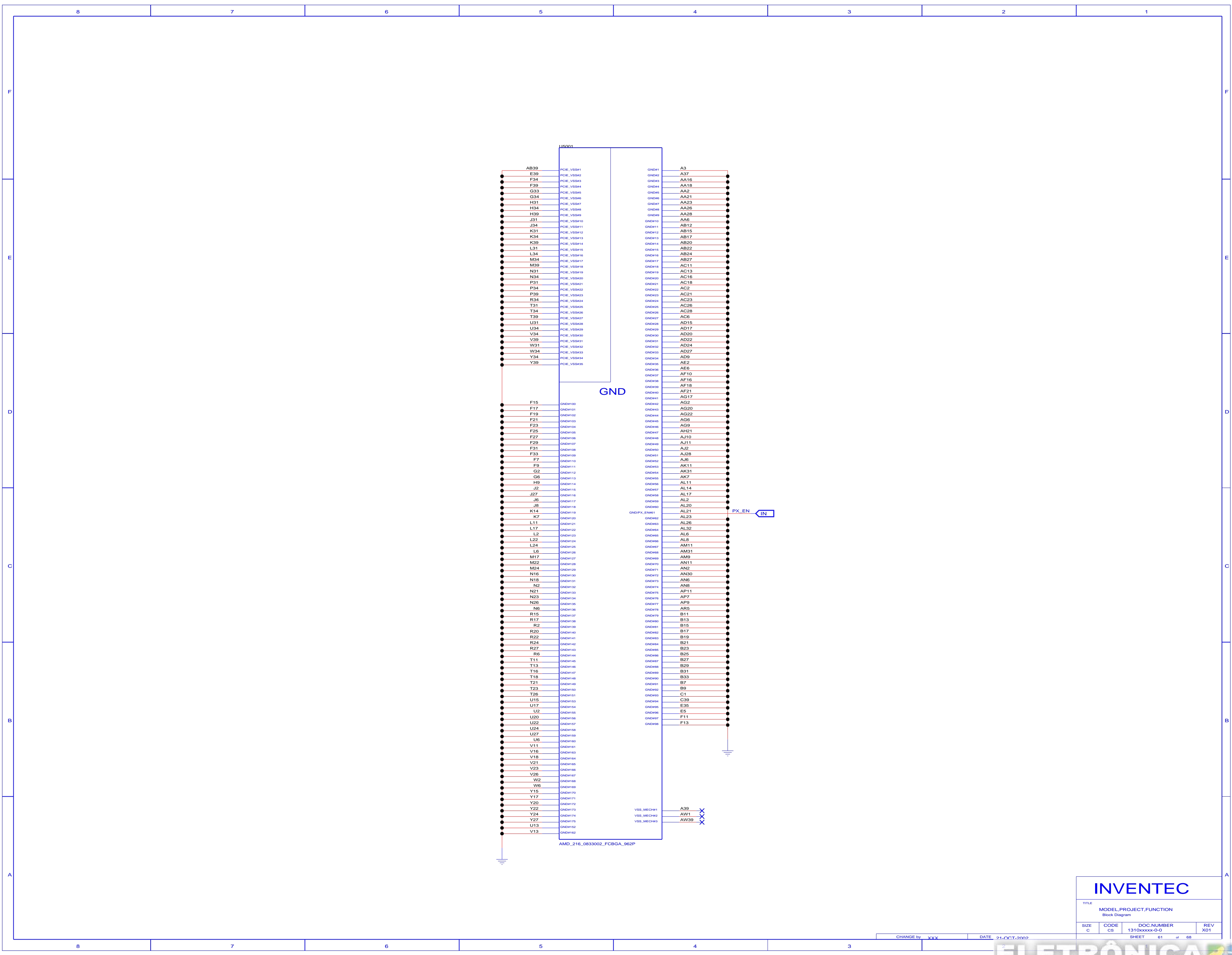






<b>INVENTEC</b>			
TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01
CHANGE by XXX		DATE 21-OCT-2002	
SHEET 60 of 68			

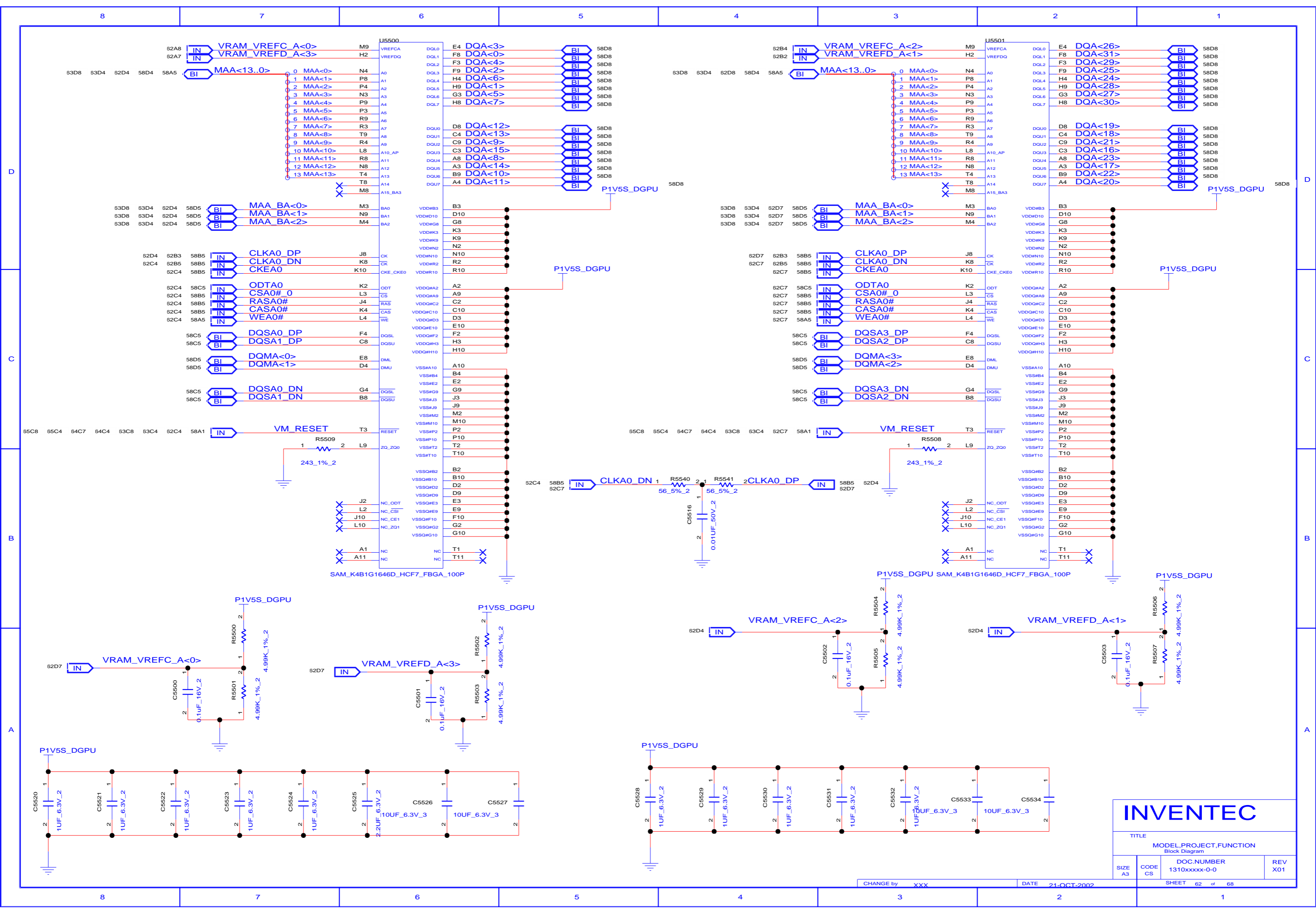
AMD\_216\_0833002\_FCBGA\_962P

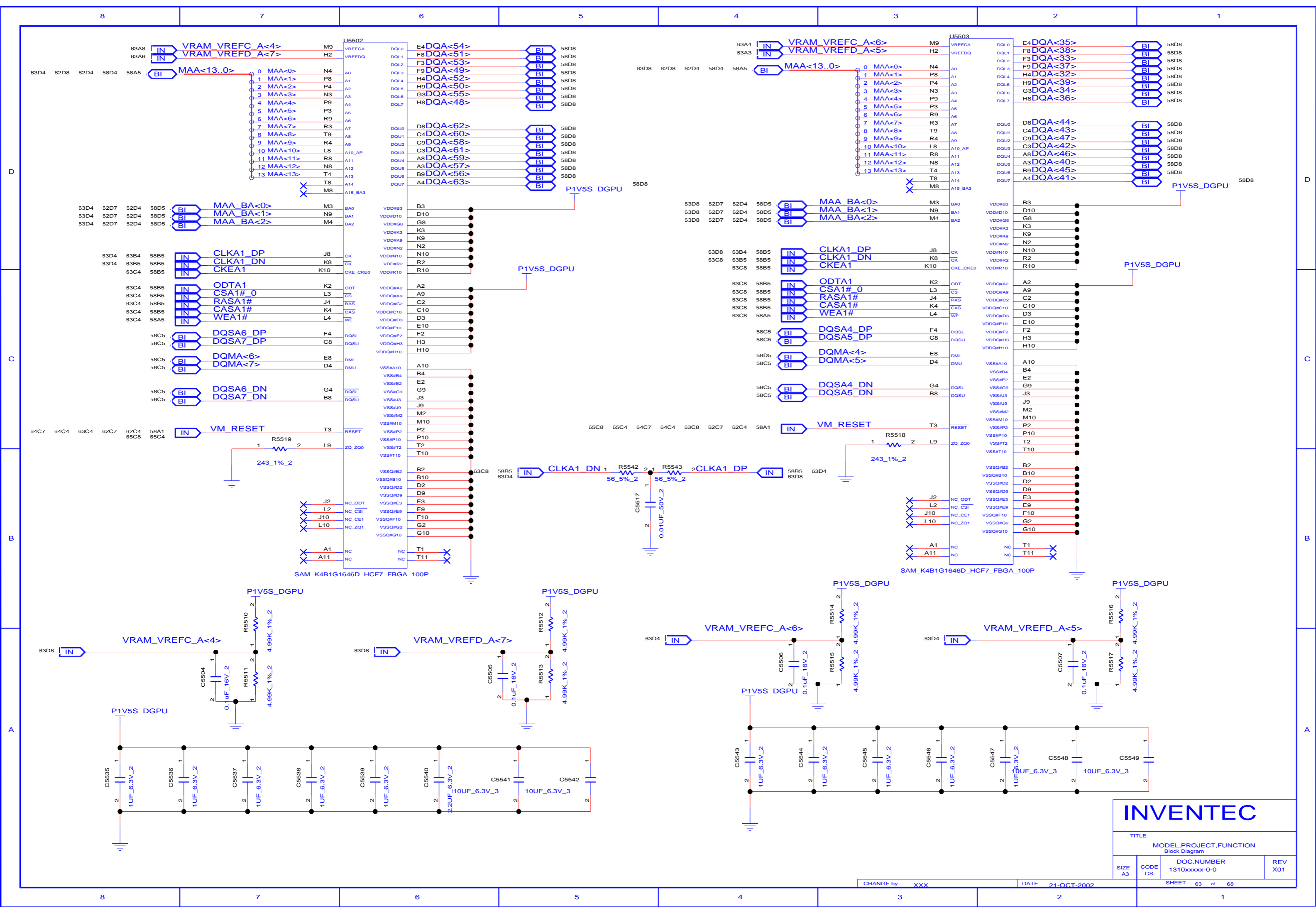


# INVENTEC

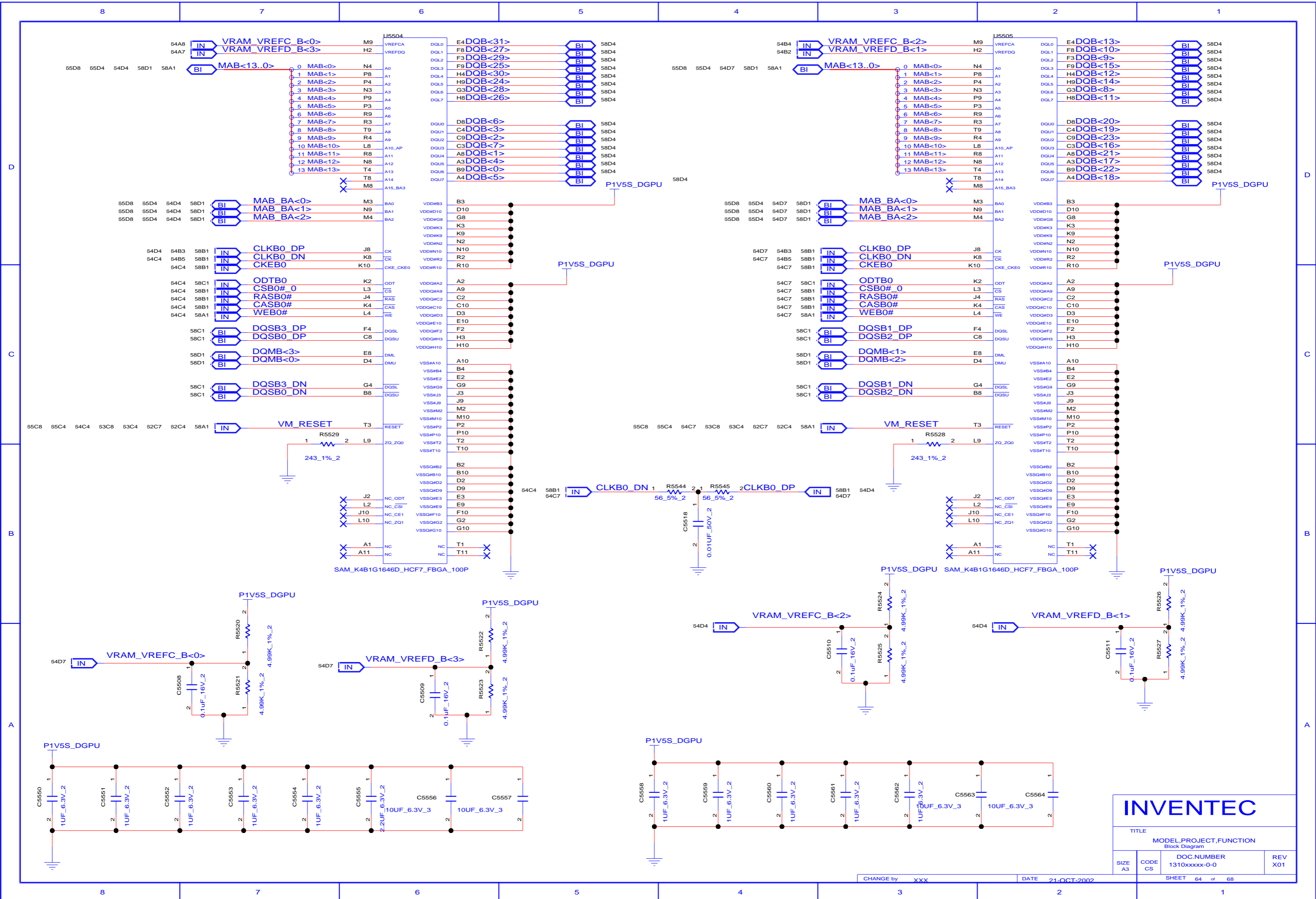
TITLE			
MODEL,PROJECT,FUNCTION			
Block Diagram			
SIZE	CODE	DOC NUMBER	REV
C	CS	1310xxxx-0-0	X01
CHANGE by xxx		DATE: 21-OCT-2002	SHEET 61 of 68







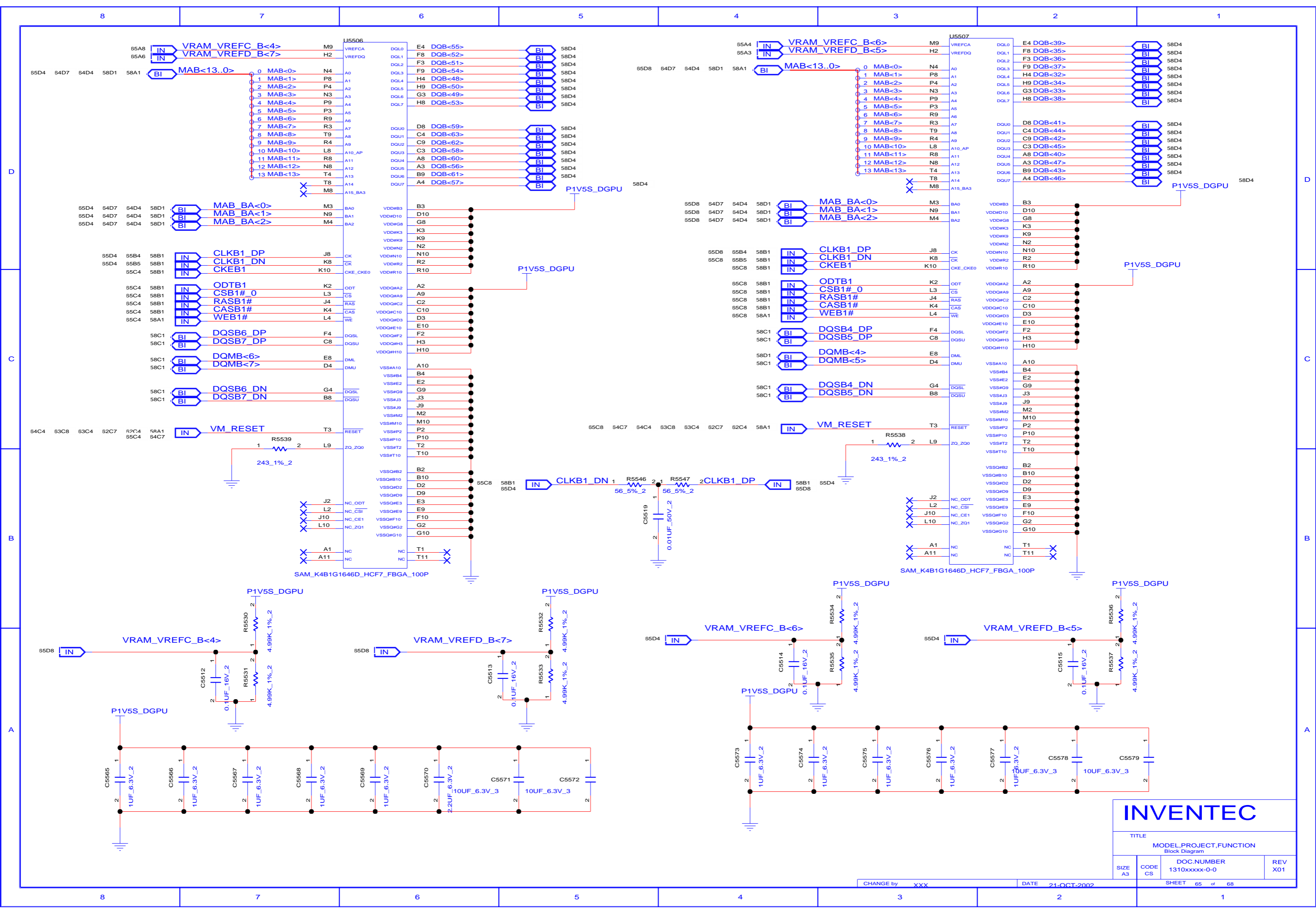
<b>INVENTEC</b>			
TITLE			
MODEL_PROJECT_FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by		DATE	SHEET
XXX		21-OCT-2002	63 of 68



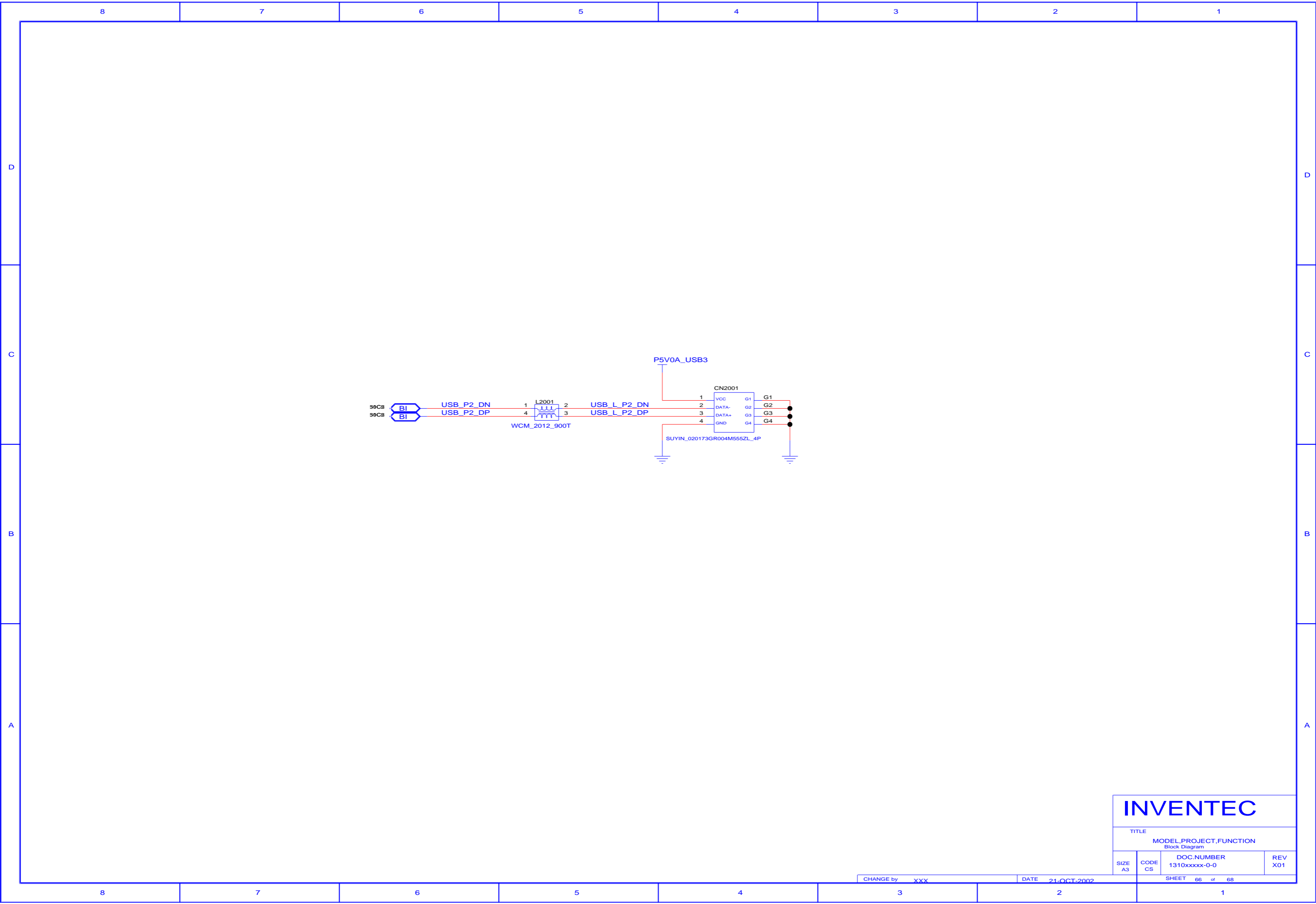
<b>INVENTEC</b>			
TITLE			
MODEL_PROJECT_FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV X01

CHANGE by XXX DATE 21-OCT-2002 SHEET 64 of 68





<b>INVENTEC</b>			
TITLE			
MODEL_PROJECT_FUNCTION			
Block Diagram			
SIZE	CODE	DOC.NUMBER	REV
A3	CS	1310xxxx-0-0	X01
CHANGE by		DATE	SHEET
XXX		21-OCT-2002	65 of 68



# INVENTEC

TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

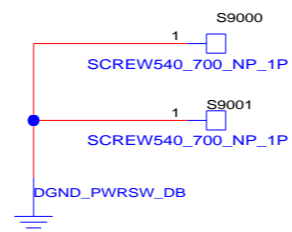
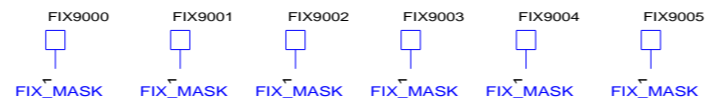
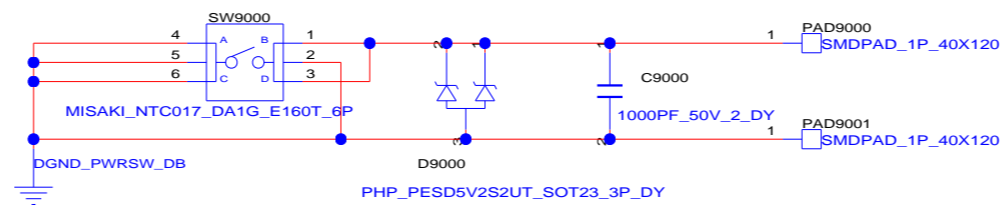
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by XXX DATE 21-OCT-2002

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REFERENCE 9000~9999(SMALL BOARD)

# POWER BUTTON



<b>INVENTEC</b>			
TITLE			
MODEL,PROJECT,FUNCTION Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01

8 7 6 5 4 3 2 1

D

D

C

C

B

B

A

A

# INVENTEC

TITLE  
MODEL,PROJECT,FUNCTION  
Block Diagram

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV X01
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CHANGE by XXX DATE 21-OCT-2002

SHEET 68 of 68

8 7 6 5 4 3 2 1