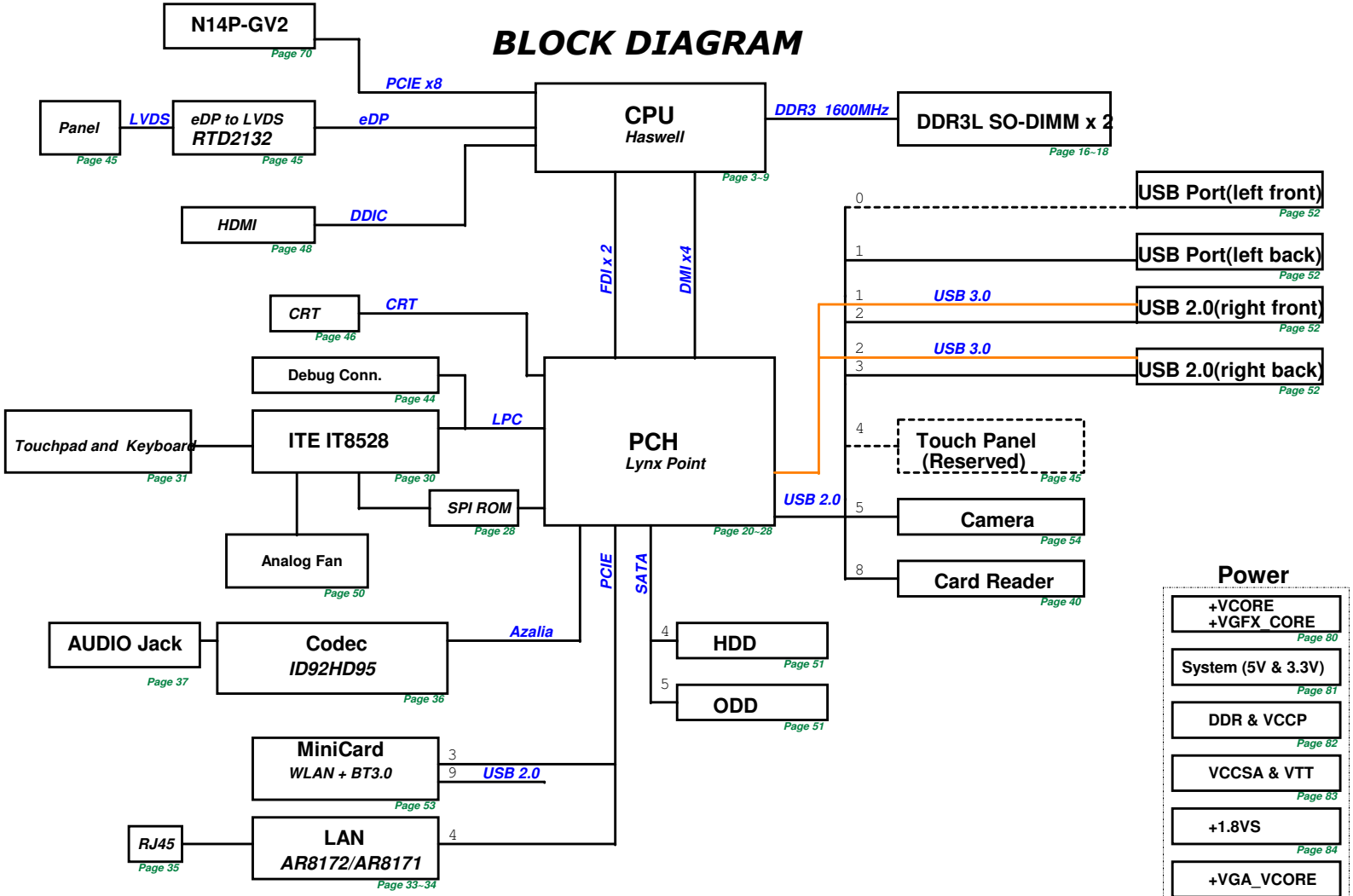
PT10SG platform Rev1.1

SYSTEM PAGE REF.

A01 Power SW
A03 TP
A04 IO_USB

BLOCK DIAGRAM



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Discharge Circuit — Page 57
DC & BATT. Conn. — Page 60
Reset Circuit — Page 32
Skew Holes — Page 65

PEGATRON Title : Block Diagram
BG\CORE Engineer: Ruby Tsai
Size C | Project Name PT10SG | Rev 1.1
Date: Tuesday, February 26, 2013 | Sheet 1 of 104

PCH_CPT GPIO

PCH_CPT GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00		PCB_ID2	EXT PD REV PU	+3VS
GPIO 01		PCB_ID3	EXT PD REV PU	+3VS
GPIO 02		PCB_ID10	REV PU REV PD	+3VS
GPIO 03		SATA_ODD_DA#	EXT PU	+3VS
GPIO 04		PCB_ID11	REV PU REV PD	+3VS
GPIO 05		PCB_ID8	EXT PU REV PD	+3VS
GPIO 06		PCB_ID4	EXT PU REV PD	+3VS
GPIO 07		PCB_ID5	REV PU REV PD	+3VS
GPIO 08		GPIO8	REV PU REV PD	+3VSUS_ORG
GPIO 09		OC5#/GPIO9	EXT PU	+3VSUS_ORG
GPIO 10		OC6#/GPIO10	EXT PU	+3VSUS_ORG
GPIO 11		SMLA_ALERT#	EXT PU	+3VSUS_ORG
GPIO 12		PM_LANPHY_EN	EXT PU	+3VSUS_ORG
GPIO 13		EXT_SCI#	EXT PU	+3VSUS_ORG
GPIO 14		OC7#/GPIO14	EXT PU	+3VSUS_ORG
GPIO 15		EXT_SMI#	EXT PU	+3VSUS+ORG
GPIO 16		GPIO16	EXT PU	+3VS
GPIO 17		DGPU_PWROK	EXT PU	+3VS
GPIO 18		CLK_REQ1#	EXT PU	+3VS
GPIO 19		BBS_BIT0_R	REV PU REV PD	+3VS
GPIO 20		CLK_REQ_WLAN#	EXT PU REV PD	+3VS
GPIO 21		SATA_DET0_R_N	EXT PU	+3VS
GPIO 22		WLAN_LED	EXT PD	
GPIO 23		SNN_LPC_DRQ#1	T2133	
GPIO 24		BT_ON/OFF#	EXT PU REV PD	+3VSUS+ORG
GPIO 25		CLK_REQ_LAN#	EXT PU REV PD	+3VSUS_ORG
GPIO 26		CLK_REQ4#	EXT PU	+3VSUS_ORG
GPIO 27		GPIO27	REV PU	+VCCDSW
GPIO 28		WLAN_ON	EXT PU	+3VSUS_ORG
GPIO 29		SLP_WLAN#	T2205	
GPIO 30		SUS_PWR_ACK_R	EXT PU	+3VSUS_ORG
GPIO 31		AC_PRESENT_R	EXT PU	+VCCDSW
GPIO 33		HDA_DOCK_EN#	T2001	
GPIO 34		+15.7V_PWRGD	EXT PU	+3VS
GPIO 35		CRT_IN#	EXT PU	+3VS
GPIO 36		GPIO36	EXT PD	
GPIO 37		FDI_OVRVLTG	EXT PD REV PU	+3VS
GPIO 38		PCB_ID0	EXT PD REV PU	+3VS
GPIO 39		PCB_ID1	REV PU EXT PD	+3VS
GPIO 40		OC1#/GPIO40	EXT PU	+3VSUS_ORG
GPIO 41		OC2#/GPIO41	EXT PU	+3VSUS_ORG
GPIO 42		OC3#/GPIO42	EXT PU	+3VSUS_ORG
GPIO 43		OC4#/GPIO43	EXT PU	+3VSUS_ORG
GPIO 44		CLK_TV_REQ#	EXT PU	+3VSUS_ORG
GPIO 45		CLK_REQ6#	EXT PU	+3VSUS_ORG
GPIO 46		CLK_REQ7#	EXT PU	+3VSUS_ORG
GPIO 47		CLKREQ_PEG#	EXT PU	+3VSUS_ORG
GPIO 48		PCB_ID6	REV PU REV PD	+3VS
GPIO 49		SATA_ODD_PRSNT#_R	EXT PU	+3VS
GPIO 50		DGPU_HOLD_RST#	EXT PU	+3VS
GPIO 51		BBS_BIT1	REV PU REV PD	+3VS
GPIO 52		PCB_ID9	REV PU REV PD	+3VS
GPIO 53		DGPU_PWM_SELECT#	REV PU	+3VS
GPIO 54		VGA_PWRON	EXT PU	+3VS
GPIO 55		STP_A16OVR	REV PD	
GPIO 56		CLK_REQ_PEG_B#	EXT PU	+3VSUS_ORG
GPIO 57		GPIO57	REV PU	+3VSUS_ORG
GPIO 58		SML1_CLK	EXT PU	+3VSUS_ORG
GPIO 59		OC0#/GPIO59	EXT PU	+3VSUS_ORG
GPIO 60		DRAMRST_CNTRL_PCH	EXT PU	+3VSUS_ORG
GPIO 61		PM_SUS_STAT#	T2203	
GPIO 62		SUSCLK_C	REV PD	
GPIO 63		SLP_S5#	T2204	
GPIO 64		KB_LED_ID	T2111	
GPIO 65		CLK_USB48_CR_R		
GPIO 66		PCB_ID14	EXT PU REV PD	+3VS
GPIO 67		PCB_ID12	REV PU REV PD	+3VS
GPIO 68		SATA_ODD_PWRGT	REV PU	+3VS
GPIO 69		LNB_EN	EXT PU	+3VS
GPIO 70		GPIO70	REV PU REV PD	+3VS
GPIO 71		PCB_ID7	EXT PU REV PD	+3VS
GPIO 72		GPIO72	EXT PU	+VCCDSW
GPIO 73		CLK_REQ0#	EXT PU	+3VSUS_ORG
GPIO 74		SML1_ALERT#	EXT PU	+3VSUS_ORG
GPIO 75		SML1_DAT	EXT PU	+3VSUS_ORG

EC ITE8528

EC GPIO	Use As	Signal Name
GPA0		PWR_WHITE_LED#
GPA1		BAT_ORG_LED#
GPA2		AOAC_RST#(test point)
GPA3		DC_IN_LED#
GPA4		FB_CLAMP_TGL_REQ#
GPA5		CHGCB2#
GPA6		THERM_ALERT#_EC
GPA7		PCH_FLASH_DESCRIPTOR
GPB0		NUM_LED#
GPB1		CAP_LED#
GPB2		THRO_CPU
GPB3		SMB0_CLK
GPB4		SMB0_DAT
GPB5		A20GATE
GPB6		RCIN#
GPB7		PM_RSMRST#
GPC0		RF_ON(Test point)
GPC1		SMB1_CLK
GPC2		SMB1_DAT
GPC3		KSO16
GPC4		AC_IN_OC
GPC5		KSO17
GPC6		BAT1_IN_OC#
GPC7		ME_AC_PRESENT
GPD0		PM_SUS8#
GPD1		PM_SUSC#
GPD2		BUF_PLT_RST#
GPD3		EXT_SCI#
GPD4		EXT_SMI#
GPD5		PM_PWROK
GPD6		FAN0_TACH
GPD7		USBP01_EN
GPE0		VSUS_ON
GPE1		SUSC_EC#
GPE2		SUSB_EC#
GPE3		CPU_VRON
GPE4		PWR_SW#_M
GPE5		USB_OC01#_EC
GPE6		LID_SW#
GPE7		USB_OC2#_EC
GPF0		BAT_LEARN
GPF1		ME_SUSPWRDNACK
GPF2		PM_PWRBTN#
GPF3		SUSACK#(Test_point)
GPF4		TP_CLK
GPF5		TP_DAT
GPF6		H_PECI_EC
GPF7		LCD_BACKOFF#
GPG0		HDMI_HPD_M
GPG1		FDIO2(Test point)
GPG2		AOAC_PWREN(Test point)
GPG6		FDIO3(Test point)
GPH0		PM_CLKRUN#
GPH1		CHGCB0#
GPH2		CHGCB1#
GPH3		SPI_CS#1
GPH4		SPI_CLK
GPH5		SPI_SO
GPH6		SPI_SI
GPI0		AD_IINP
GPI1		SUS_PWRGD
GPI2		ALL_SYSTEM_PWRGD
GPI3		VRM_PWRGD
GPI4		ADAPT_AD
GPI5		EC_SLP_SUS#(Test point)
GPI6		WLAN_WAKE#(Test point)
GPI7		IMON(Test point)
GPJ0		HDIO2(Test point)
GPJ1		HDIO3(Test point)
GPJ2		OP_SD#
GPJ3		USBSLP_EN
GPJ4		FB_CLAMP
GPJ5		CTL_FAN
GPJ6		SW_RTCRST
GPJ7		BACK_EN

EC Name	Use As	Signal Name
LAD0		LPC_AD0
LAD1		LPC_AD1
LAD2		LPC_AD2
LAD3		LPC_AD3
LCLK		CLK_KBCPCI_PCH
LFRAME#		LPC_FRAME#
LRESET#		BUF_PLT_RST#
SERIRQ		INT_SERIRQ
WRST#		EC_RST#
PECI		H_PECI_EC
FSCK		SCK
FMISO		SO
FMOSI		SI
FSCE#		SCE#
KSI0		KSI0
KSI1		KSI1
KSI2		KSI2
KSI3		KSI3
KSI4		KSI4
KSI5		KSI5
KSI6		KSI6
KSI7		KSI7
KSO0		KSO0
KSO1		KSO1
KSO2		KSO2
KSO3		KSO3
KSO4		KSO4
KSO5		KSO5
KSO6		KSO6
KSO7		KSO7
KSO8		KSO8
KSO9		KSO9
KSO10		KSO10
KSO11		KSO11
KSO12		KSO12
KSO13		KSO13
KSO14		KSO14
KSO15		KSO15

@	
N/A	
/UMA	UMA only
/VGA	Optimus only
/DSC	discrete only
/UMA/VGA	UMA,Optimus 都要上
/VGA/DSC	Optimus,Discrete 都要上
/EMI	EMI 要上
@/EMI	EMI 預留但 不上
/Giga	Giga要上 的
/EMIGiga	Giga EMI要上 的
/10_100	10_100 transformer
/CRT/UMA/VGA	CRT 在UMA,Optimus要上
/CRT/DSC	CRT Discrete only要上
/LVDS/UMA/VGA	LVDS 在UMA,Optimus要上
/LVDS/DSC	LVDS Discrete only要上
/HDMI	HDMI 要上
/HDMI/UMA/VGA	HDMI 在UMA,Optimus要上
/HDMI/DSC	HDMI Discrete only要上
/USB3.0_U	Right Up要上 USB3.0
/USB2.0_U	Right Up 要上 USB2.0
/USB3.0	Right down要上 USB3.0
/USB2.0	Right down 要上 USB2.0
/USBSLP	USB sleep charge
/NON-USBSLP	USB sleep don't charge
/TP_A	TouchPad Type A
/TP_B	TouchPad Type B
/WOWL	wake on WLAN
/non-WOWL	non wake on WLAN

SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)

PCIE 1	NC
PCIE 2	NC
PCIE 3	Minicard WLAN
PCIE 4	LAN
PCIE 5	NC
PCIE 6	NC
PCIE 7	NC
PCIE 8	NC

SATA0	NC
SATA1	NC
SATA2	NC
SATA3	NC
SATA4	SATA HDD
SATA5	SATA ODD

USB3 1	USB3.0 Port (1)
USB3 2	USB3.0 Port (2)
USB3 3	NC
USB3 4	NC
USB3 5	NC
USB3 6	NC

USB 0	USB2.0 Port(Reserved)
USB 1	USB2.0 Port(debug)
USB 2	USB3.0 Port (1)
USB 3	USB3.0 Port (2)
USB 4	Touch Panel (reserved)
USB 5	Camera
USB 6	NC
USB 7	NC
USB 8	Card Reader
USB 9	WiFi/WiMax
USB 10	NC
USB 11	NC
USB 12	NC
USB 13	NC

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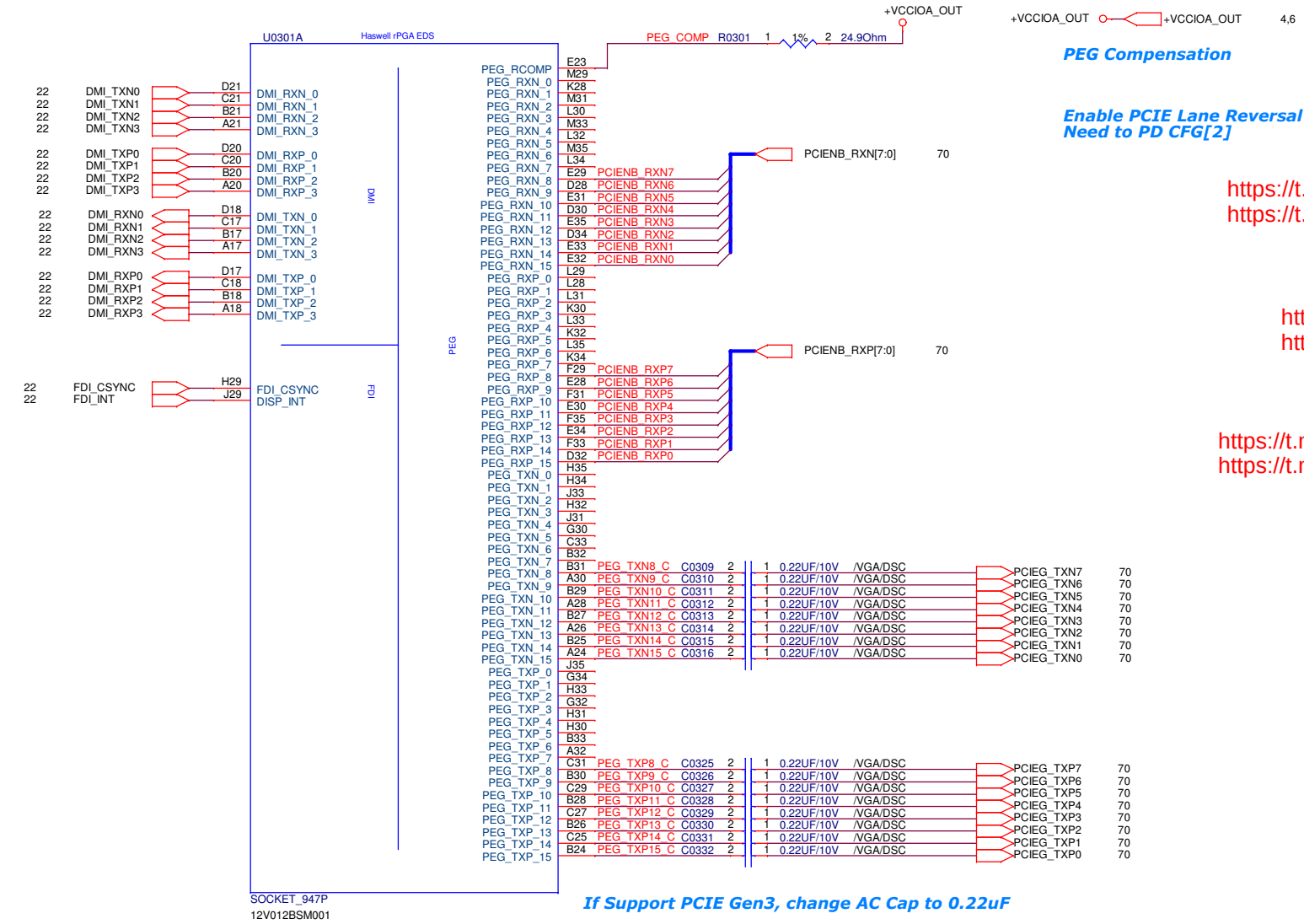
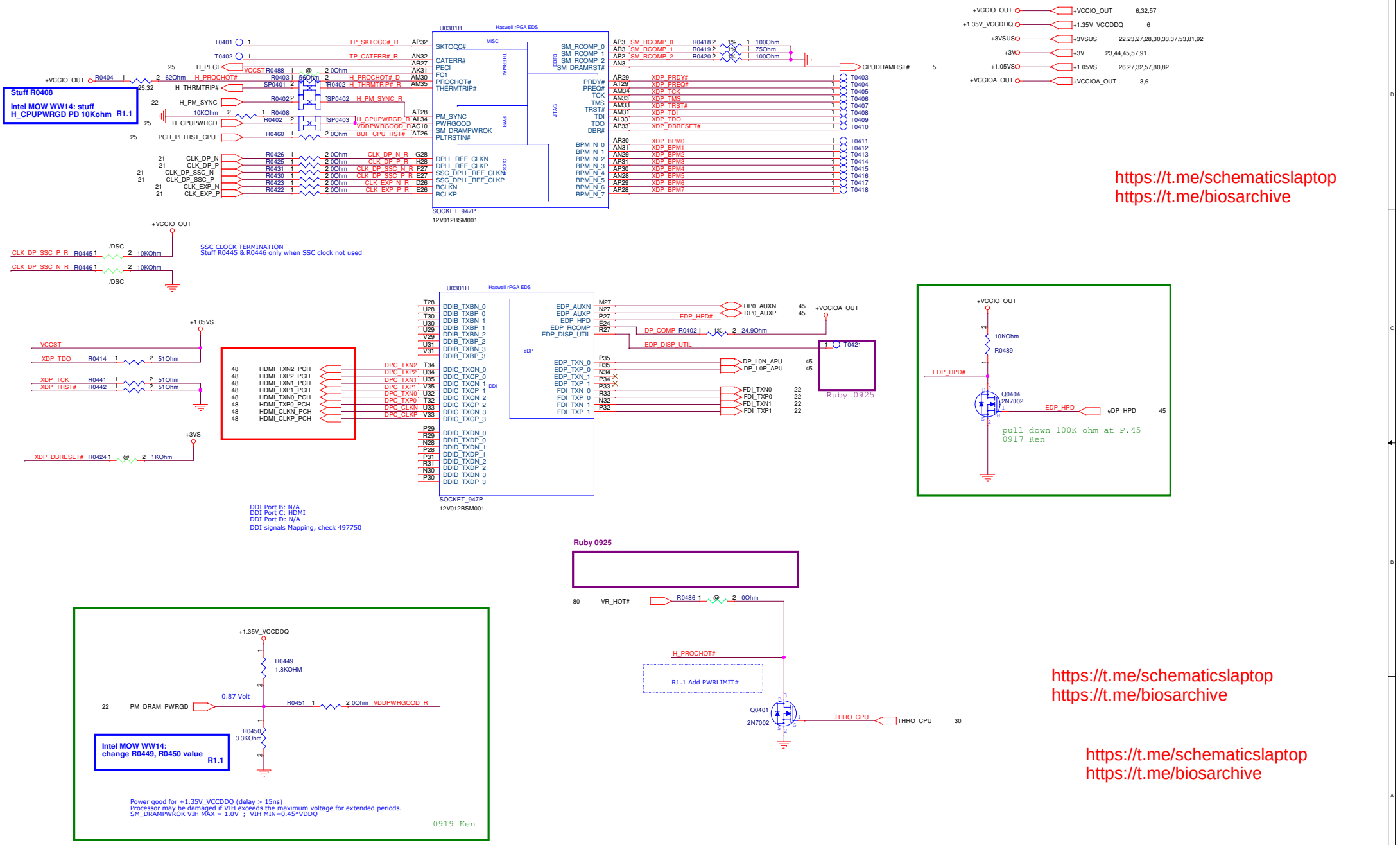
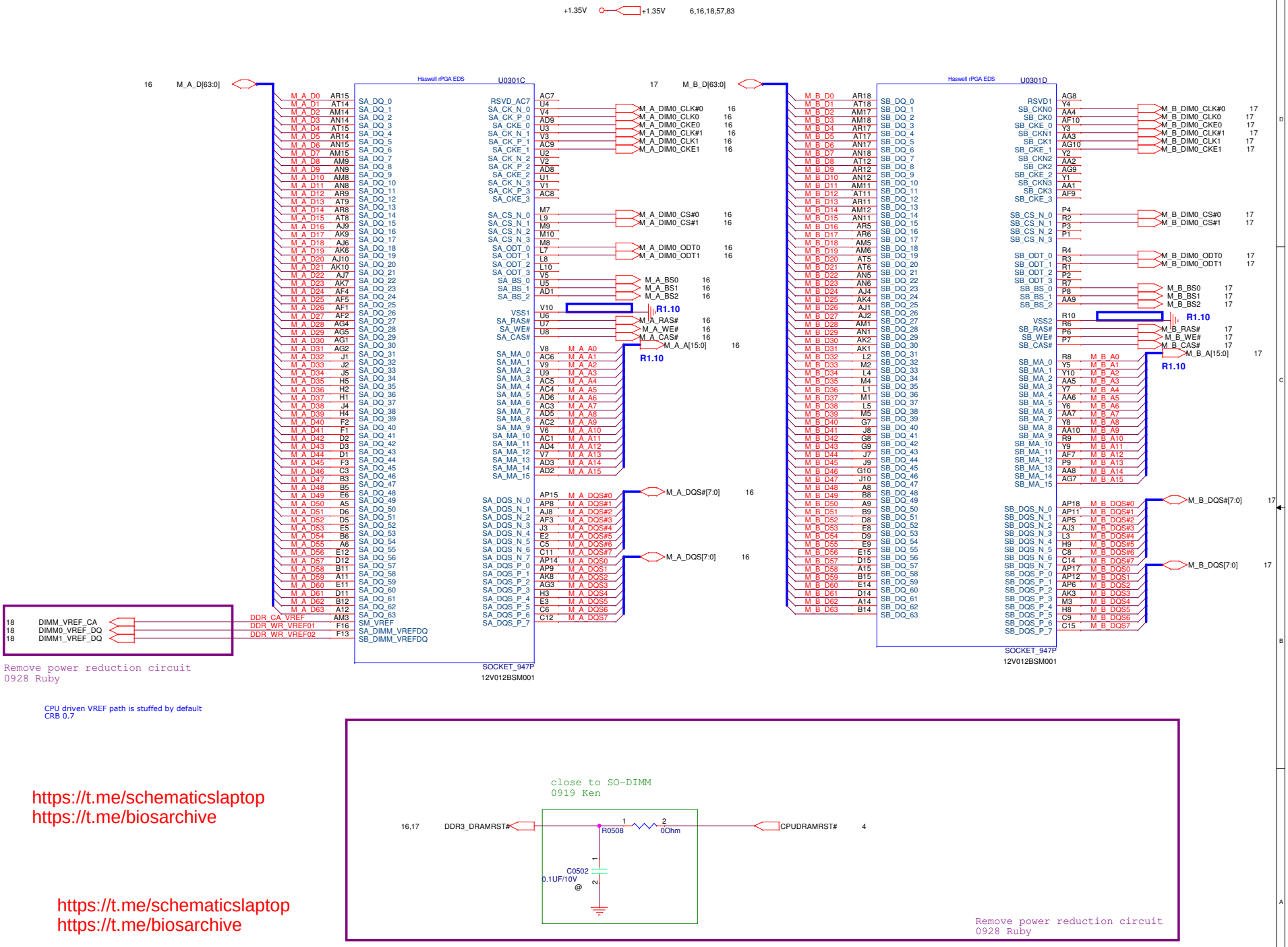
PEGATRON Title : System Setting
SOFTCORE Engineer: Ruby Tsai
Size: D | Project Name: PT10SG | Rev: 1.1
Date: Tuesday, February 26, 2013 | Sheet 2 of 104



PEGATRON	Title : CPU(1)_DMI,PEG,FDI
BG1\CORE	Engineer: Ruby Tsai
Size: B	Project Name: PT10SG
Rev: 1.1	
Date: Tuesday, February 26, 2013	Sheet 3 of 104



PEGATRON	Title :	CPU(2)_CLK,MISC,JTAG,DD	
BG1\CORE	Engineer:	Ruby Tsai	
Size: Custom	Project Name: PT10SG		Rev: 1.1
Date: Tuesday, February 26, 2013	Sheet 4 of 104		



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PEGATRON Title : CPU(2)_DDR3

BG1\CORE Engineer: Ruby Tsai

Size	Project Name	Rev
Custom	PT10SG	1.1

Date: Tuesday, February 26, 2013 Sheet 5 of 104

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+1.35V_VCCDDQ — +1.35V_VCCDDQ 4
+1.35V — +1.35V 16,18,57,83
+VCORE — +VCORE 9,57,80
+VCCIO_OUT — +VCCIO_OUT 4,32,57
+VCCIO2PCH — +VCCIO2PCH 27
+VCCIOA_OUT — +VCCIOA_OUT 3,4

Remove S3 power reduction circuit
0928 Ruby

JP0601
3MM_OPEN_5MIL

1009 Ruby remove 1/16 R1.1

R1.10

Decoupling guide from Intel (EE)
VDDQ 22uF * 2pcs (stuff)
10uF * 2pcs (stuff)
330uF * 1pcs (stuff)

Decoupling guide from Intel (EE)
+VCORE 10uF * 11pcs (stuff)
22uF * 19pcs (stuff)
470uF * 5pcs (stuff)

Placement note:
1. R0602 close to CPU
2. R0603 close to CPU
3. R0605 close to VR
4. R0608 close to CPU
5. R0607 close to VR
6. R0611 close to CPU

Unstuff R0622
Intel MOW WW09: renamed VCCIO2PCH to RSVD R1.1

100 ohm in power circuit
0921 Ken

Power team suggestion

If XDP not implemented, then Route Processor PWR_DEBUG as a test point. This Test point must be clearly labeled (shark bay check list 497750)

Cap of 470UF or more place at power schematic

U0301E Haswell rPGA EDS
SOCKET_947P
12V012BSM001

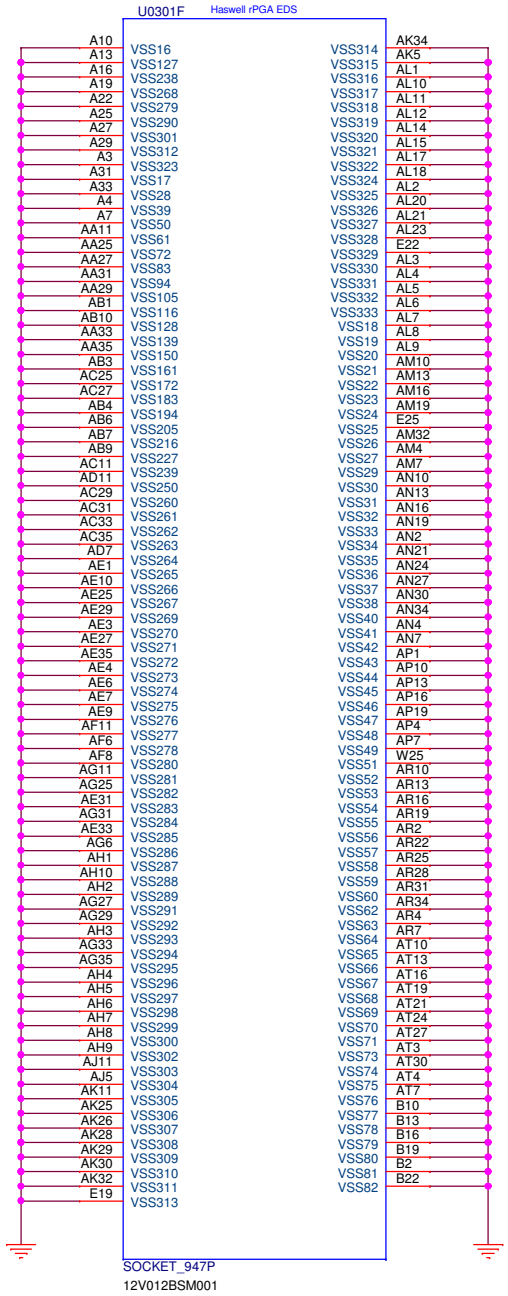
PEGATRON	Title : CPU(4)_PWR
BG1\CORE	Engineer: Ruby Tsai
Size: Custom	Project Name: PT10SG
Rev: 1.1	
Date: Tuesday, February 26, 2013	Sheet 6 of 104

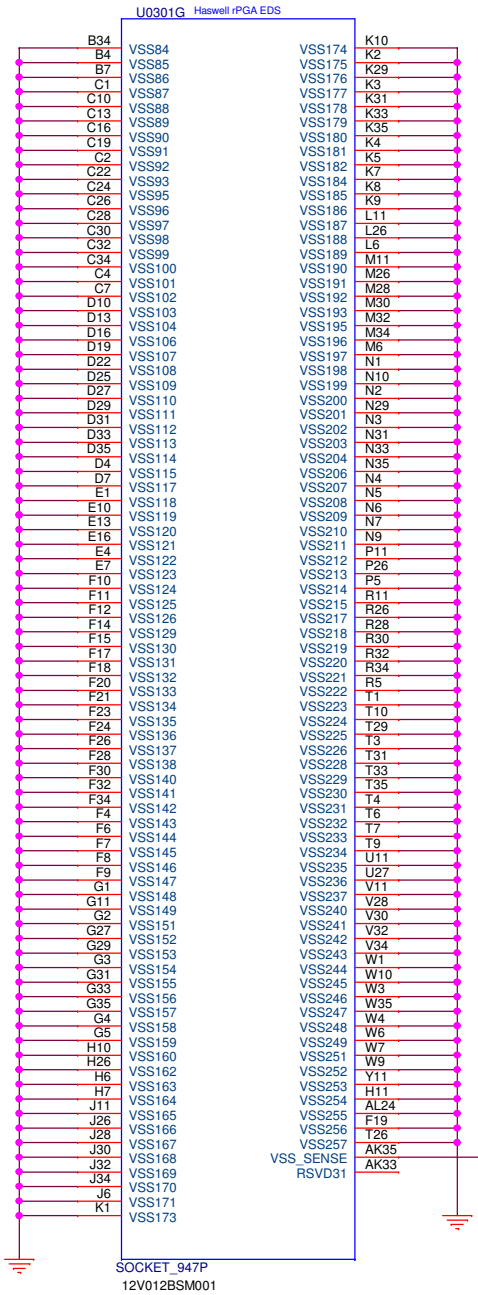
PEGATRON Title : CPU(4)_PWR

BG1\CORE Engineer: Ruby Tsai

Size	Project Name	Rev
Custom	PT10SG	1.1

Date: Tuesday, February 26, 2013 Sheet 7 of 104





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Placement note:
1. R0801 close to CPU

100 ohm in power circuit
0921 Ken

PEGATRON Title : CPU(6)_GND
BG1\CORE Engineer: Ruby Tsai

Size	Project Name	Rev
B	PT10SG	1.1

Date: Tuesday, February 26, 2013 Sheet 8 of 104

CFG strapping information: The CFG signals have a default value of '1'

CFG[1:0]: Reserved configuration lane.

CFG[2]: PCIE Static Numbering Lane Reversal- CFG[2] is for the 16x

- 1: (Default) Normal Operation, Lane # definition matches sockect pin map definition
- 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

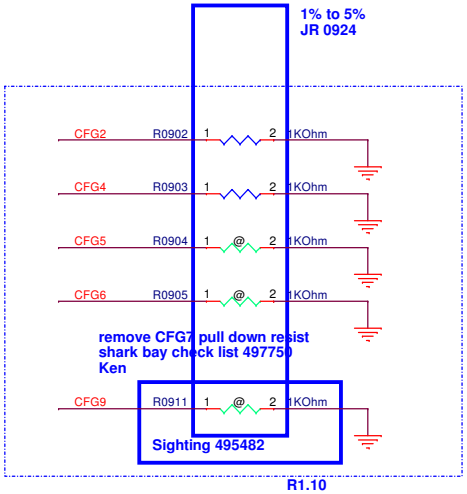
CFG[4]: eDP enable

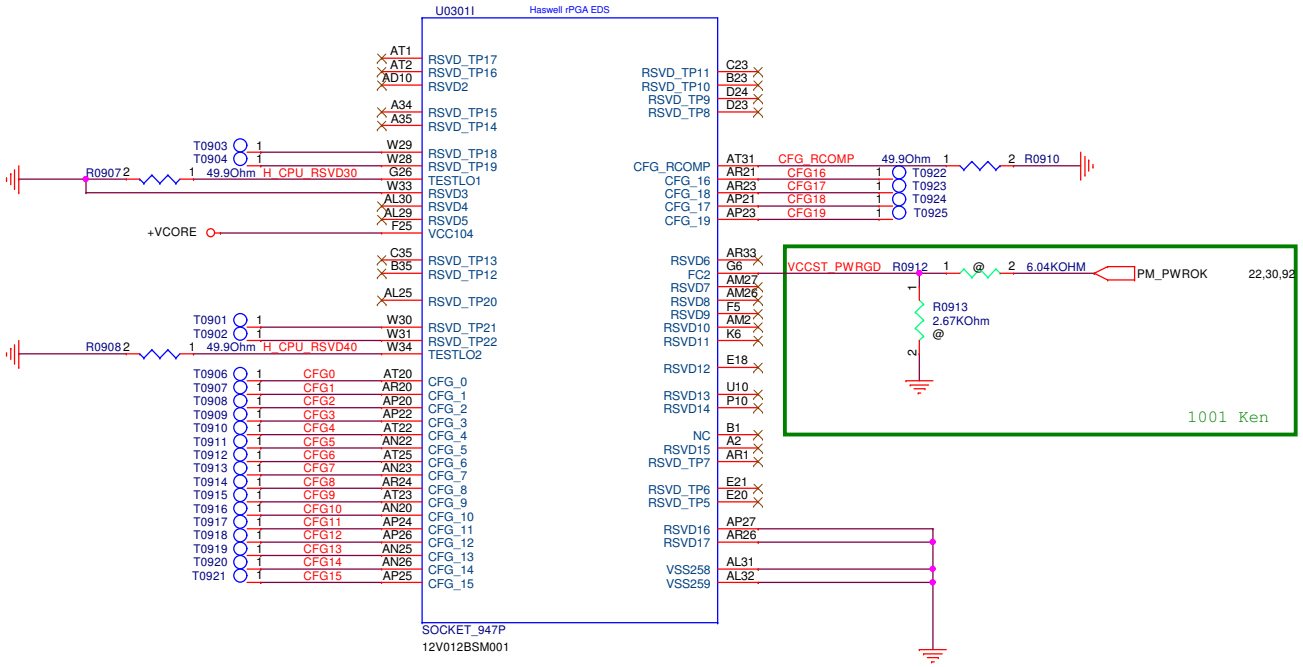
-1 = Disabled
-0 = Enabled

CFG[6:5]: PCI Express Port Bifurcation Straps

-00 = 1 x8, 2 x4 PCI Express*
-01 = reserved
-10 = 2 x8 PCI Express*
-11 = 1 x16 PCI Express*

CFG[19:7]: Reserved configuration lane.





+VCORE +VCORE 6,57,80

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PEGATRON Title : CPU(7)_RESERVED
BG1/HW RD Center Engineer: Ruby Tsai
Size: Custom | Project Name: PT10SG | Rev: 1.1
Date: Tuesday, February 26, 2013 | Sheet 9 of 104

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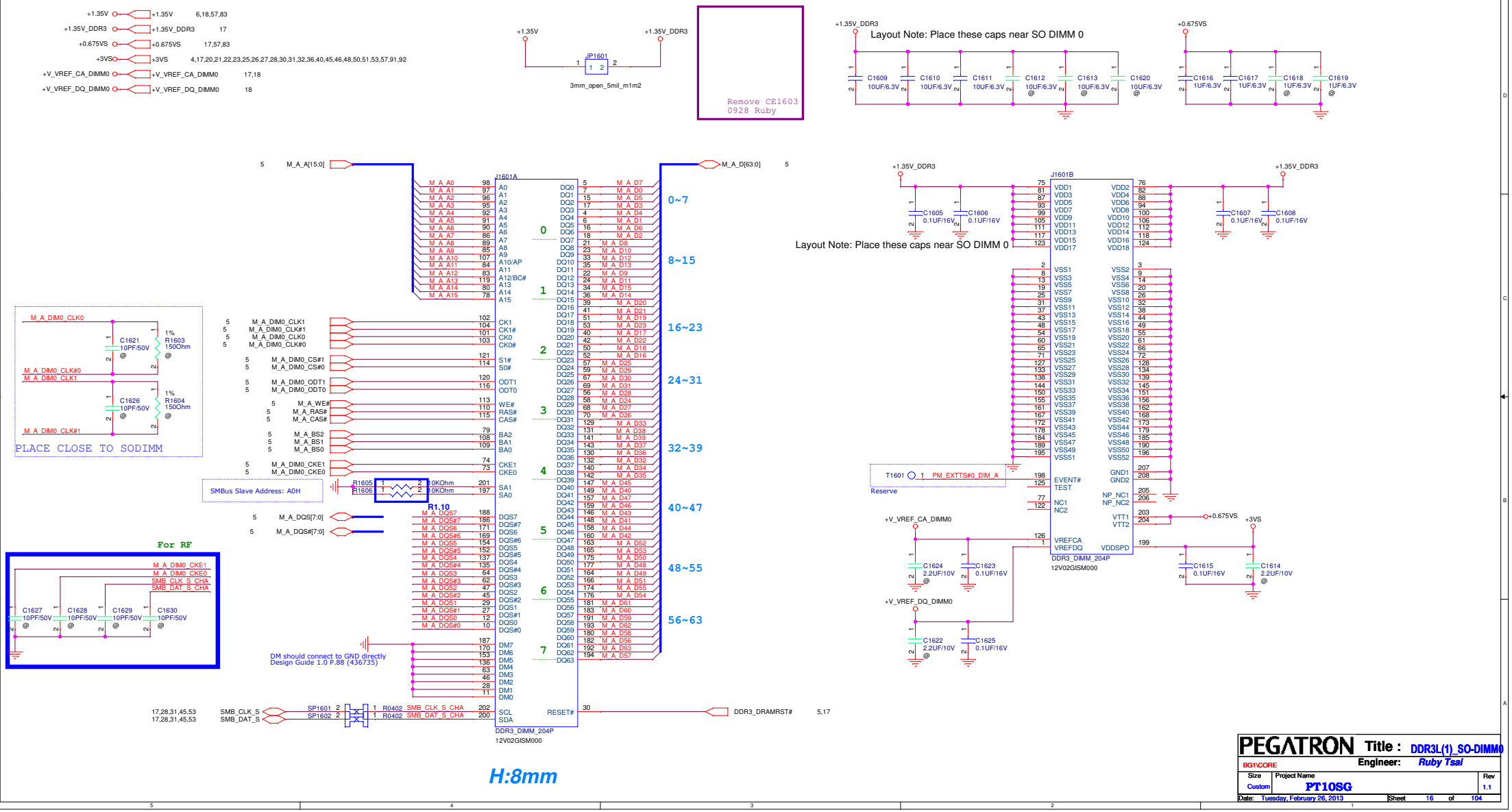
PEGATRON Title : CPU_PCH_XDP

BG1\CORE Engineer: Ruby Tsai

Size	Project Name	Rev
C	PT10SG	1.1

Date: Tuesday, February 26, 2013 Sheet 10 of 104



H:8mm

+1.35V_DDR3 +1.35V_DDR3 16

+0.675VS +0.675VS 16,57,83

+3VS +3VS 4,16,20,21,22,23,25,26,27,28,30,31,32,36,40,45,46,48,50,51,53,57,91,92

+V_VREF_CA_DIMM1 +V_VREF_CA_DIMM1 16,18

+V_VREF_DQ_DIMM1 +V_VREF_DQ_DIMM1 18

Remove CE1603
0928 Ruby

+1.35V_DDR3

Layout Note: Place these caps near SO DIMM 1

C1709 10UF/6.3V @ C1710 10UF/6.3V @ C1711 10UF/6.3V @ C1712 10UF/6.3V @ C1713 10UF/6.3V @ C1726 10UF/6.3V @

+0.675VS

C1716 1UF/6.3V @ C1717 1UF/6.3V @ C1718 1UF/6.3V @ C1719 1UF/6.3V @

5 M_B_A[15:0]

J1701A

M_B_A0 98 A0
M_B_A1 97 A1
M_B_A2 96 A2
M_B_A3 95 A3
M_B_A4 92 A4
M_B_A5 91 A5
M_B_A6 90 A6
M_B_A7 86 A7
M_B_A8 89 A8
M_B_A9 85 A9
M_B_A10 107 A10/AP
M_B_A11 84 A11
M_B_A12 83 A12/BC#
M_B_A13 119 A13
M_B_A14 80 A14
M_B_A15 78 A15

M_B_D[63:0] 5

M_B_D0 5 DQ0
M_B_D7 7 DQ1
M_B_D3 15 DQ2
M_B_D2 17 DQ3
M_B_D1 4 DQ4
M_B_D5 6 DQ5
M_B_D4 16 DQ6
M_B_D6 18 DQ7
M_B_D10 21 DQ8
M_B_D14 23 DQ9
M_B_D12 33 DQ10
M_B_D13 35 DQ11
M_B_D8 22 DQ12
M_B_D9 24 DQ13
M_B_D11 34 DQ14
M_B_D15 36 DQ15
M_B_D16 39 DQ16
M_B_D17 41 DQ17
M_B_D18 51 DQ18
M_B_D23 53 DQ19
M_B_D20 40 DQ20
M_B_D21 42 DQ21
M_B_D19 52 DQ22
M_B_D29 57 DQ23
M_B_D28 59 DQ24
M_B_D26 67 DQ25
M_B_D31 69 DQ26
M_B_D30 56 DQ27
M_B_D25 58 DQ28
M_B_D27 68 DQ29
M_B_D24 70 DQ30
M_B_D33 129 DQ31
M_B_D37 131 DQ32
M_B_D34 141 DQ33
M_B_D35 143 DQ34
M_B_D32 130 DQ35
M_B_D36 132 DQ36
M_B_D39 140 DQ37
M_B_D38 142 DQ38
M_B_D44 147 DQ39
M_B_D45 149 DQ40
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M_B_D56 183 DQ56
M_B_D58 191 DQ57
M_B_D63 193 DQ58
M_B_D62 180 DQ59
M_B_D61 182 DQ60
M_B_D57 192 DQ61
M_B_D59 194 DQ62
DQ63

0~7 8~15 16~23 24~31 32~39 40~47 48~55 56~63

5 M_B_DIM0_CLK1 102 CK1
5 M_B_DIM0_CLK#1 104 CK1#
5 M_B_DIM0_CLK0 101 CK0
5 M_B_DIM0_CLK#0 103 CK0#

5 M_B_DIM0_CS#1 121 S1#
5 M_B_DIM0_CS#0 114 S0#

5 M_B_DIM0_ODT1 120 ODT1
5 M_B_DIM0_ODT0 116 ODT0

5 M_B_WE# 113 WE#
5 M_B_RAS# 110 RAS#
5 M_B_CAS# 115 CAS#

5 M_B_BS2 79 BA2
5 M_B_BS1 108 BA1
5 M_B_BS0 109 BA0

5 M_B_DIM0_CKE1 74 CKE1
5 M_B_DIM0_CKE0 73 CKE0

+3VS R1705 1 2 10KOhm 201 SA1
R1706 1 2 10KOhm 197 SA0

SMBus Slave Address: A4H

R1.10

5 M_B_DQS[7:0]
5 M_B_DQS#[7:0]

M_B_DQS7 188 DQS7
M_B_DQS#7 186 DQS#7
M_B_DQS6 171 DQS6
M_B_DQS#6 169 DQS#6
M_B_DQS5 154 DQS5
M_B_DQS#5 152 DQS#5
M_B_DQS4 137 DQS4
M_B_DQS#4 135 DQS#4
M_B_DQS3 64 DQS3
M_B_DQS#3 62 DQS#3
M_B_DQS2 47 DQS2
M_B_DQS#2 45 DQS#2
M_B_DQS1 29 DQS1
M_B_DQS#1 27 DQS#1
M_B_DQS0 12 DQS0
M_B_DQS#0 10 DQS#0

187 DM7
170 DM6
153 DM5
136 DM4
63 DM3
46 DM2
28 DM1
11 DM0

16,28,31,45,53 SMB_CLK_S SP1701 2 1 R0402 SMB_CLK_S_CHB 202 SCL
16,28,31,45,53 SMB_DAT_S SP1702 2 1 R0402 SMB_DAT_S_CHB 200 SDA

RESET# 30 DDR3_DRAMRST# 5,16

DDR3_DIMM_204P
12V02GISM001

M_B_DIM0_CLK0
C1720 10PF/50V @ 1% 150Ohm R1707 @
M_B_DIM0_CLK#0
M_B_DIM0_CLK1
C1721 10PF/50V @ 1% 150Ohm R1708 @
M_B_DIM0_CLK#1

PLACE CLOSE TO SODIMM

For RF

M_B_DIM0_CKE1
M_B_DIM0_CKE0
SMB_CLK_S_CHB
SMB_DAT_S_CHB
C1727 10PF/50V @ C1728 10PF/50V @ C1729 10PF/50V @ C1730 10PF/50V @

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H:4mm

+1.35V_DDR3

C1705 0.1UF/16V @ C1706 0.1UF/16V @

Layout Note: Place these caps near SO DIMM 1

C1707 0.1UF/16V @ C1708 0.1UF/16V @

J1701B

VDD1 75 VDD2 76
VDD3 81 VDD4 82
VDD5 87 VDD6 88
VDD7 93 VDD8 94
VDD9 99 VDD10 100
VDD11 105 VDD12 106
VDD13 111 VDD14 112
VDD15 117 VDD16 118
VDD17 123 VDD18 124

VSS1 2 VSS2 3
VSS3 8 VSS4 9
VSS5 13 VSS6 14
VSS7 19 VSS8 20
VSS9 25 VSS10 26
VSS11 31 VSS12 32
VSS13 37 VSS14 38
VSS15 43 VSS16 44
VSS17 48 VSS18 49
VSS19 54 VSS20 55
VSS21 60 VSS22 61
VSS23 65 VSS24 66
VSS25 71 VSS26 72
VSS27 127 VSS28 128
VSS29 133 VSS30 134
VSS31 138 VSS32 139
VSS33 144 VSS34 145
VSS35 150 VSS36 151
VSS37 155 VSS38 156
VSS39 161 VSS40 162
VSS41 167 VSS42 168
VSS43 172 VSS44 173
VSS45 178 VSS46 179
VSS47 184 VSS48 185
VSS49 189 VSS50 190
VSS51 195 VSS52 196

T1701 1 PM_EXTTS#0_DIM_B 198 EVENT#
Reserve 125 TEST

GND1 207
GND2 208

NP_NC1 205
NP_NC2 206

77 NC1
122 NC2

VTT1 203
VTT2 204

+0.675VS

+V_VREF_CA_DIMM1
C1724 2.2UF/10V @ C1723 0.1UF/16V

126 VREFCA
1 VREFDQ

VDDSPD 199

+3VS
C1715 0.1UF/16V C1714 2.2UF/10V @

DDR3_DIMM_204P
12V02GISM001

+V_VREF_DQ_DIMM1
C1722 2.2UF/10V @ C1725 0.1UF/16V

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PEGATRON Title : DDR3(2)_SO-DIMM1

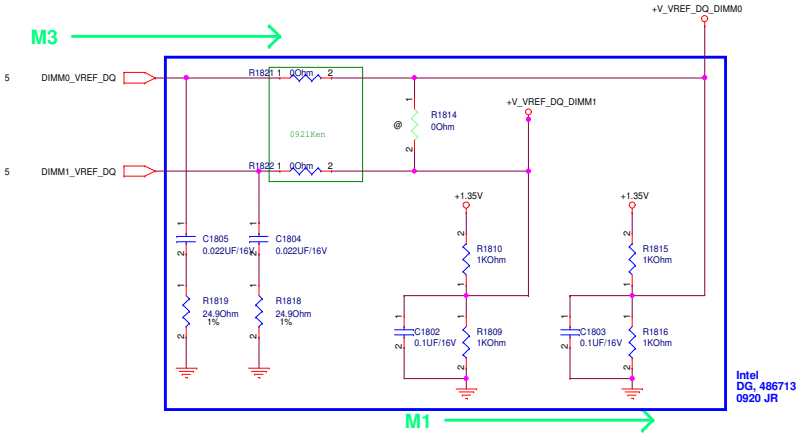
BG1\CORE Engineer: Ruby Tsai

Size	Project Name	Rev
Custom	PT10SG	1.1

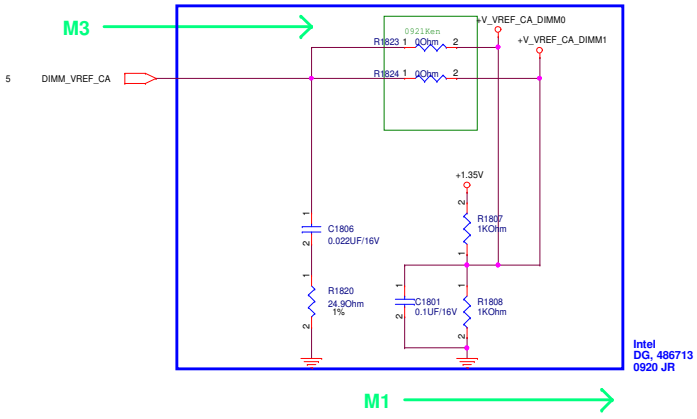
Date: Tuesday, February 26, 2013 Sheet 17 of 104

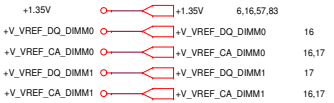
DDR3L Vref

M3: CPU driven VREF path is stuffed be default.
M1: VREF_DQ driven by a Voltage Divider Network during Processor power-off



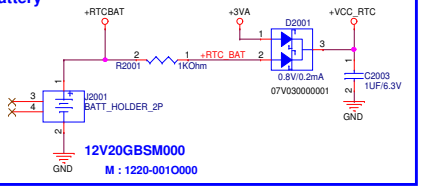
Intel 0203
M3+M1: Default Recommendation





PEGATRON Title : DDR3(3)_CA/DQ Voltage
BG1\CORE Engineer: Ruby Tsai
Size C | Project Name PT10SG | Rev 1.1
Date: Tuesday, February 26, 2013 | Sheet 18 of 104

RTC battery



12V20GBSM000

M : 1220-001O000

+VCC_RTC	+VCC_RTC 22,27
+3VA	+3VA 27,30,33,57,60,65,81,88,93
+3VS	+3VS 4,16,17,21,22,23,25,26,27,28,30,31,32,36,40,45,46,48,50,51,53,57,91,92
+3VSUS_ORG	+3VSUS_ORG 21,22,24,25,26,27
+12VS	+12VS 28,48,57,91
+1.5VS	+1.5VS 21,22,24,26,27,53,57,84

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+VCC_RTC RTCRST# RC delay should be 18ms~25ms

R2003 20KOhm, C2004 1UF/6.3V, JRST2001 SGL_JUMP @

R2005 1MOhm, R2004 20KOhm, C2005 1UF/6.3V, JRST2002 SGL_JUMP @

TPM Settings	JRST2001
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

Request by CSC for CMOS clear function

CMOS Settings	JRST2002
Clear CMOS	Shunt
Keep CMOS	Open (Default)

Q2001 2N7002, R2026 10KOhm, SW_RTCRST

EC reset CMOS feature

C2001 15PF/50V, XTAL 32K X1_C, SP2005, R0402, X2001 32.768KHZ, NC 0920 JR, R2002 10MOhm, C2002 15PF/50V

T2015, T2012, T2011, R2006 330KOhm PCH_INTVRMEN

U2001A LPT_PCH_M_EDS

XTAL_32K_X1	B5	RTCX1
XTAL_32K_X2	B4	RTCX2
SRTC_RST#	B9	SRTCRST#
SM_INTRUDER#	A8	INTRUDER#
PCH_INTVRMEN	G10	INTVRMEN
RTC_RST#	D9	RTCRST#
HDA_BCLK_R	B25	HDA_BCLK
HDA_SYNC_R	A22	HDA_SYNC
	AL10	SPKR
HDA_RST# R	C24	HDA_RST#
	L22	HDA_SDI0
	K22	HDA_SDI1
	G22	HDA_SDI2
HDA_SDI3	F22	HDA_SDI3
HDA_SDO_R	A24	HDA_SDO
HDA_DOCK_EN#	B17	DOCKEN#/GPIO33
	C22	HDA_DOCK_RST#/GPIO13
PCH_JTAG_TCK_BUF	AB3	JTAG_TCK
PCH_JTAG_TMS	AD1	JTAG_TMS
PCH_JTAG_TDI	AE2	JTAG_TDI
PCH_JTAG_TDO	AD3	JTAG_TDO
	F8	TP25
	C26	TP22
PM_TEST_RST_N	AB6	TP20

POINT 02V000000013

SATA_RXN_0 SATA_RXP_0	BC8 BE8	
SATA_TXN_0 SATA_TXP_0	AW8 AY8	
SATA_RXN_1 SATA_RXP_1	BC10 BE10	
SATA_TXN_1 SATA_TXP_1	AW10 AY10	
SATA_RXN_2 SATA_RXP_2	BB9 BD9	
SATA_TXN_2 SATA_TXP_2	AY13 AW13	
SATA_RXN_3 SATA_RXP_3	BC12 BE12	
SATA_TXN_3 SATA_TXP_3	AR13 AT13	
SATA_RXN4/PERN1 SATA_RXP4/PERP1	BD13 BB13	SATA_RXN0 51, SATA_RXP0 51 — SATA HDD
SATA_TXN4/PETN1 SATA_TXP4/PETP1	AV15 AW15	SATA_TXN0 51, SATA_TXP0 51
SATA_RXN5/PERN2 SATA_RXP5/PERP2	BC14 BE14	SATA_RXN2 51, SATA_RXP2 51 — SATA ODD
SATA_TXN5/PETN2 SATA_TXP5/PETP2	AP15 AR15	SATA_TXN2 51, SATA_TXP2 51
SATA_RCOMP	AY5	SATA_COMP R2007 7.5KOhm +1.5VS
SATALED#	AP3	SATA_LED# R2025 10KOhm +3VS
SATA0GP/GPIO21	AT1	SATA_DET0_R_N T2028
SATA1GP/GPIO19	AU2 Int. PU	BBS_BIT0_R R2057 0Ohm BBS_BIT0 23
SATA_IREF	BD4	SATA_IREF R2056 0Ohm +1.5VS
TP9	BA2	
TP8	BB2	

0927 Ruby

INTVRMEN: Integrated SUS 1.05V VRM Enables
Low: Enable External VRs
High:Enable Internal VRs

PCH_INTVRMEN R2030 330KOhm @ R1.10

R1.0
For JTAG to pull high and low.

+3VSUS_ORG

PCH_JTAG_TMS	R2040	220Ohm /XDP
PCH_JTAG_TDO	R2038	220Ohm /XDP
PCH_JTAG_TDI	R2039	220Ohm /XDP
	R2041	100Ohm /XDP
	R2042	100Ohm /XDP
	R2043	100Ohm /XDP
PCH_JTAG_TCK_BUF	R2044	51Ohm /XDP

Strap information:

HDA_SPKR: No reboot strap
Low: Disable (Default)
High:Enable

SB_SPKR R2020 1KOhm +3VS

Ruby 0925

HDA_SDO:
1.Flash descriptor security:
Sampled Low: in effect.
Sampled High: override

2.HDA_SDO which sample high on the rising edge of PWROK
Will also disable Intel ME.

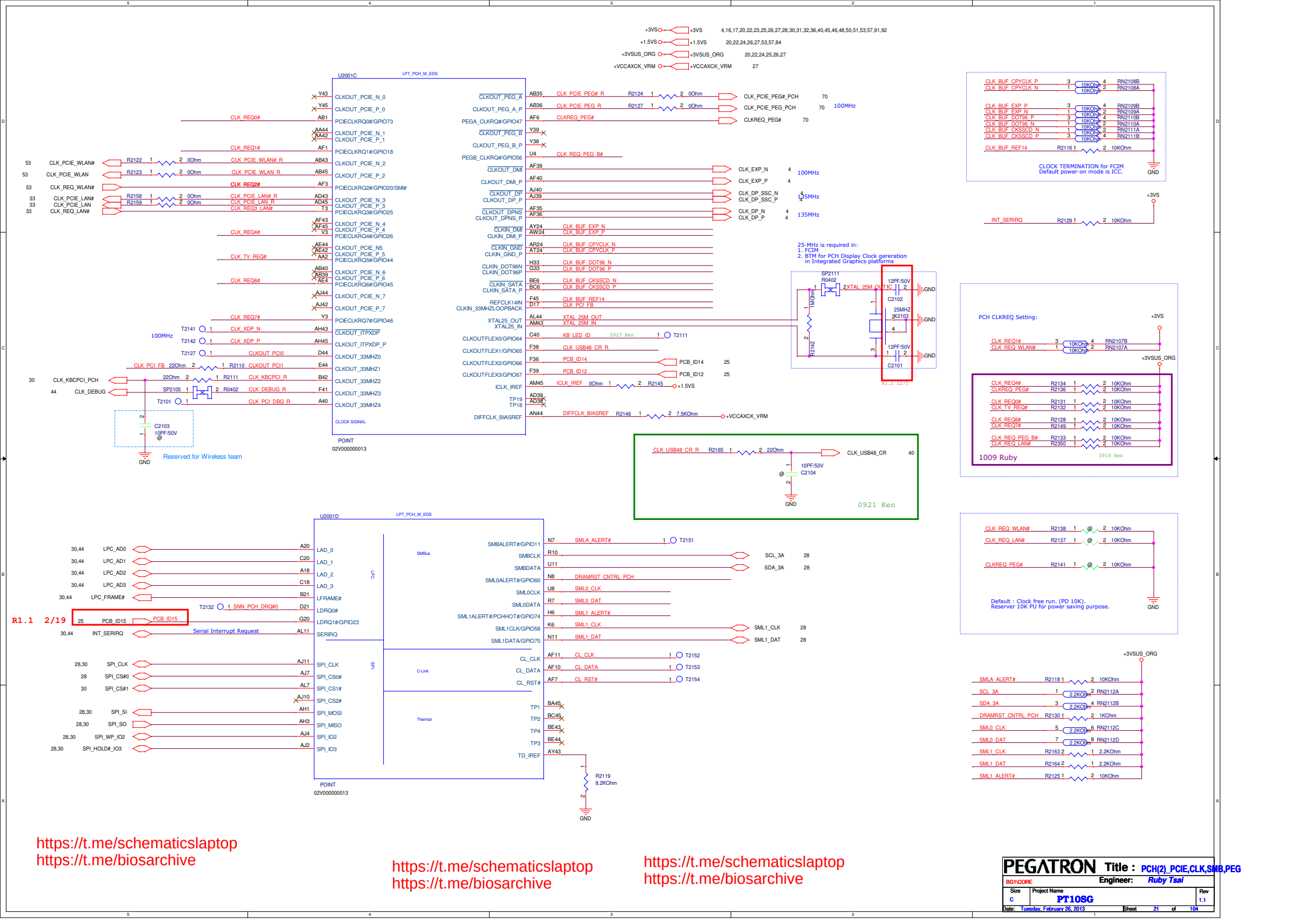
HDA_SDO_R R2034 1KOhm +3VSUS_ORG

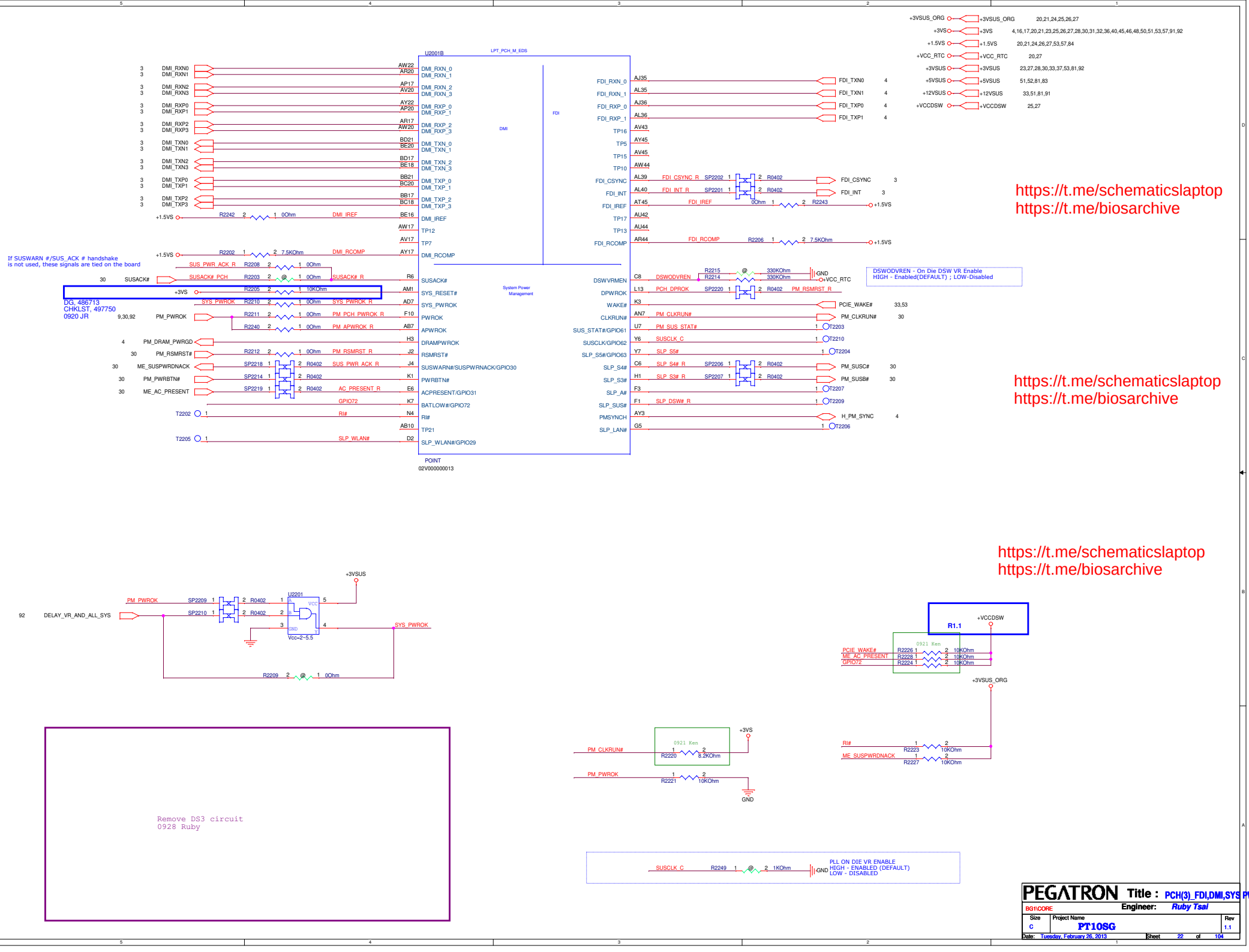
HDA_DOCK_EN#:
Reserved

[0216] : ACZ_SYNC strap is no longer supported on LPT, by Intel FAE Stu.

+3VS SATA_DET0_R_N R2037 10KOhm R1.10

PEGATRON	Title : PCH(1)_SATA,IHDA,RTC,LPC		
BG1\CORE	Engineer: Ruby Tsai		
Size: Custom	Project Name: PT10SG		Rev: 1.1
Date: Tuesday, February 26, 2013	Sheet 20 of 104		




U2001B
LPT_PCH_M_EDS
DMI
FDI
System Power Management
DMI_RXN_0
DMI_RXN_1
DMI_RXN_2
DMI_RXN_3
DMI_RXP_0
DMI_RXP_1
DMI_RXP_2
DMI_RXP_3
DMI_TXN_0
DMI_TXN_1
DMI_TXN_2
DMI_TXN_3
DMI_TXP_0
DMI_TXP_1
DMI_TXP_2
DMI_TXP_3
DMI_IREF
DMI_RCOMP
SUSACK#
SYS_RESET#
SYS_PWROK
PWROK
APWROK
DRAMPWROK
RSMRST#
SUSWARN#/SUSPWRNACK/GPIO30
PWRBTN#
ACPRESENT/GPIO31
BATLOW#/GPIO72
RI#
TP21
SLP_WLAN#/GPIO29
FDI_RXN_0
FDI_RXN_1
FDI_RXP_0
FDI_RXP_1
TP16
TP5
TP15
TP10
FDI_CSYNC
FDI_INT
FDI_IREF
TP17
TP13
FDI_RCOMP
DSWVRMEN
DPWROK
WAKE#
CLKRUN#
SUS_STAT#/GPIO61
SUSCLK/GPIO62
SLP_S5#/GPIO63
SLP_S4#
SLP_S3#
SLP_A#
SLP_SUS#
PMSYNCH
SLP_LAN#
POINT
02V000000013
+3VSUS_ORG
+3VS
+1.5VS
+VCC_RTC
+3VSUS
+5VSUS
+12VSUS
+VCCDSW
If SUSWARN #/SUS_ACK # handshake is not used, these signals are tied on the board
DG_486713
CHKLST_497750
0920 JR
DSWODVREN - On Die DSW VR Enable
HIGH - Enabled(DEFAULT) ; LOW-Disabled
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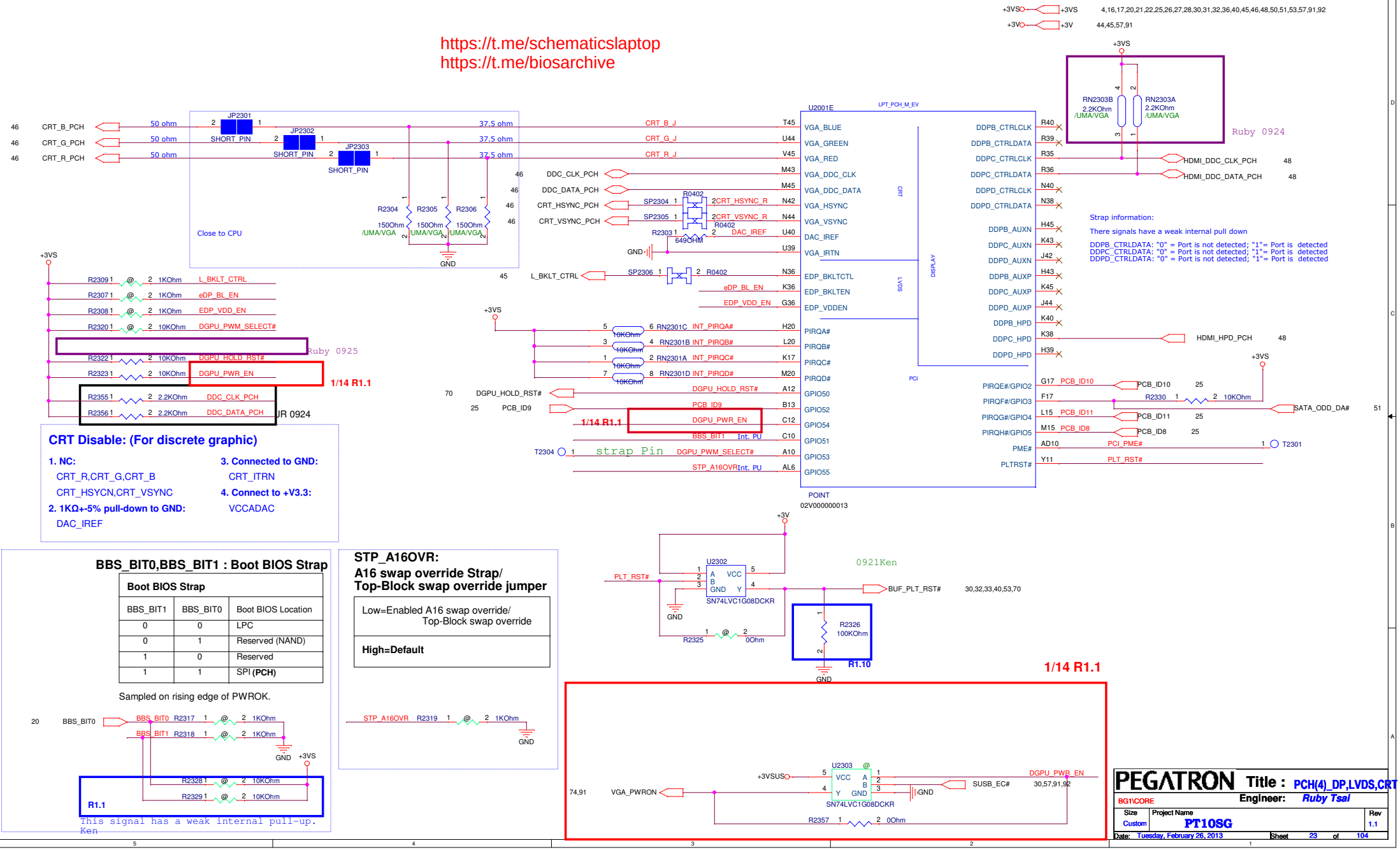
https://t.me/schematicslaptop
https://t.me/biosarchive
Remove DS3 circuit
0928 Ruby
PLL ON DIE VR ENABLE
HIGH - ENABLED (DEFAULT)
LOW - DISABLED
0921 Ken
PEGATRON
Title : PCH(3)_FDI,DMI,SYS PWR
BG1\CORE
Engineer: Ruby Tsai
Size C
Project Name PT10SG
Rev 1.1
Date: Tuesday, February 26, 2013
Sheet 22 of 104



CRT Disable: (For discrete graphic)

1. NC:
   CRT_R,CRT_G,CRT_B
   CRT_HSYCN,CRT_VSYNC
2. 1KΩ+-5% pull-down to GND:
   DAC_IREF
3. Connected to GND:
   CRT_ITRN
4. Connect to +V3.3:
   VCCADAC

BBS_BIT0,BBS_BIT1 : Boot BIOS Strap

Boot BIOS Strap		
BBS_BIT1	BBS_BIT0	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	Reserved
1	1	SPI **(PCH)**

Sampled on rising edge of PWROK.

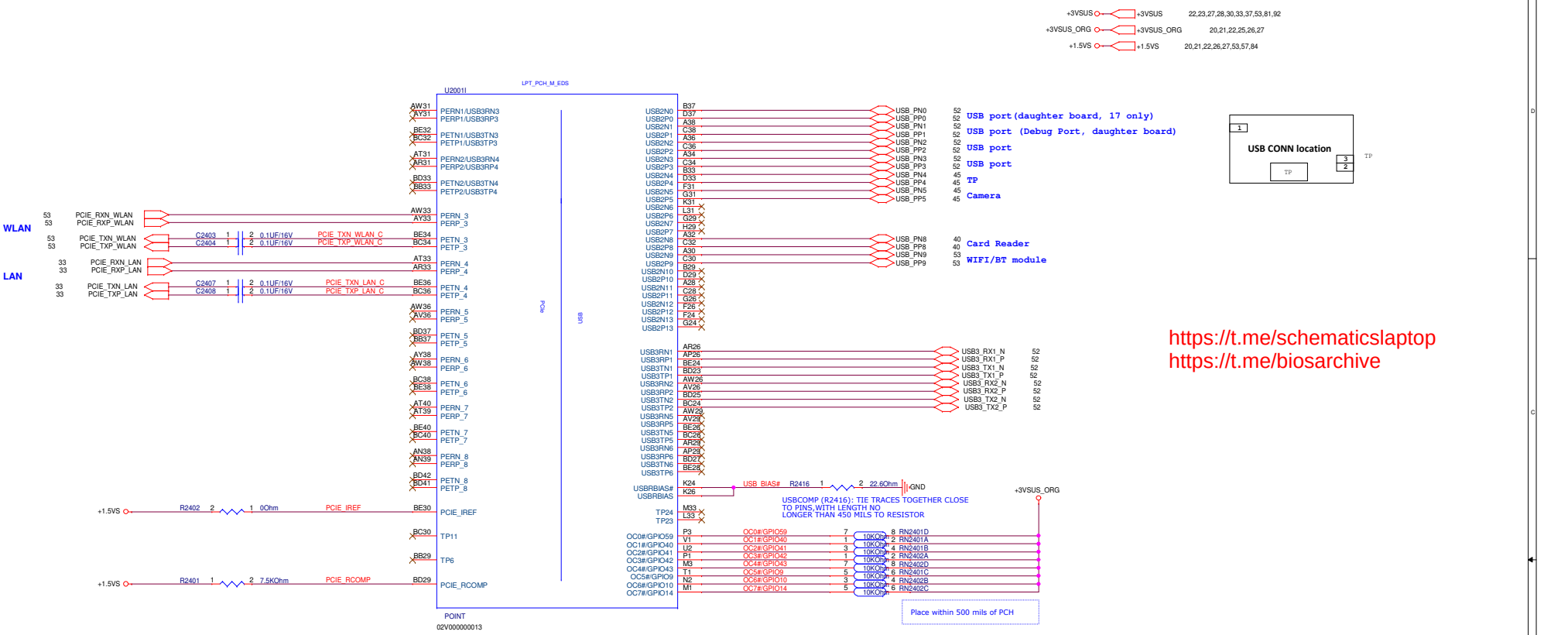
STP_A16OVR:

A16 swap override Strap/ Top-Block swap override jumper

Low=Enabled A16 swap override/ Top-Block swap override
High=Default

1/14 R1.1

PEGATRON Title : PCH(4)_DP,LVDS,CRT
BG1\CORE Engineer: Ruby Tsai
Size: Custom | Project Name: PT10SG | Rev: 1.1
Date: Tuesday, February 26, 2013 Sheet 23 of 104



PEGATRON	Title :	PCH(5)_PCI,NVRAM,USB	
BG1\CORE	Engineer:	Ruby Tsai	
Size: C	Project Name: PT10SG		Rev: 1.1
Date: Tuesday, February 26, 2013	Sheet 24 of 104		

BIOS Rev. SKU

ID0	ID1	ID2	PCB Rev.
0	0	0	R1.0
1	0	0	R1.1
0	1	0	R2.0
1	1	0	R2.1
0	0	1	TBD
1	0	1	TBD
0	1	1	TBD
1	1	1	TBD

CPU. PWR

ID7	ID8	CPU PWR.
0	0	CPU 17W
1	0	CPU 35W
0	1	CPU 45W
1	1	TBD

+3VS 4,16,17,20,21,22,23,26,27,28,30,31,32,36,40,45,46,48,50,51,53,57,91,92
+3VSUS_ORG 20,21,22,24,26,27
+VCCDSW 22,27

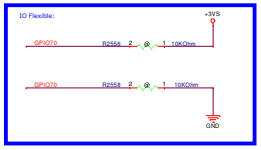
PCB_ID3	PCB_ID4	PCB_ID5	PCB_ID6	PCB_ID9	PCB_ID10	PCB_ID11	PCB_ID12	PCB_ID13	PCB_ID14	PCB_ID15
1: Starndard	1: Premium	1:USB3.0*2	1: HDMI	1: Zero_ODD	1: UMA	1: S&M	1: eDP	1. Disable KB_LED	1: USB3.0	1: PS/2+SMBUS TP
0: Entry	0: Mainstream	0:USB3.0*1	0: no HDMI	0: Non Zero ODD	0: PX	0: NoS&M	0: LVDS	0. Enable KB_LED	0: non USB3.0	0: PS/2 TP

R1.1 2/19

THRMTRIP#
Intel is recommended that motherboard designs implement a pull-up resistor site on the THRMTRIP# signal to the PCH 1.05V Core VR
0917 Ken

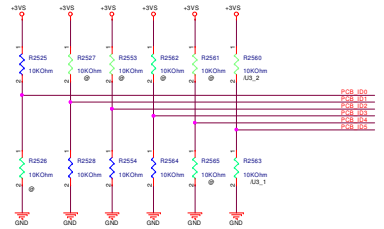
B2538:
Stuff -> non Intel LAN
No stuff -> Intel LAN(Pull up on chip side)

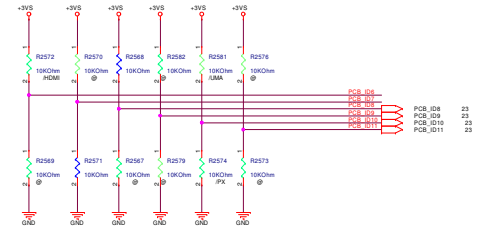
remove DDR_VOLT_DEL
0920 Ken

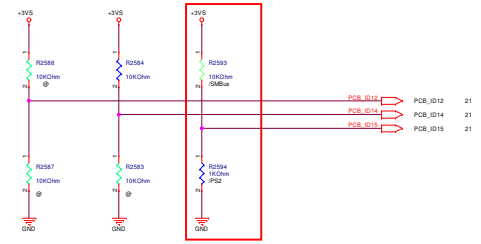


USB3 Port 3 PCIE Port2 Mode (USB3P3_PCIEP2_MODE)
USB3p3_tach6_gp70 pin is a '0', then Root Port 2 is assigned to USB3 Port 3, else it is assigned to PCI Express.

USB3 Port 2 PCIE Port1 Mode (USB3P2_PCIEP1_MODE)
USB3p2_tach7_gp71 pin is a '0', then Root Port 1is assigned to USB3 Port 2, else it is assigned to PCI Express.







R1.1 2/19

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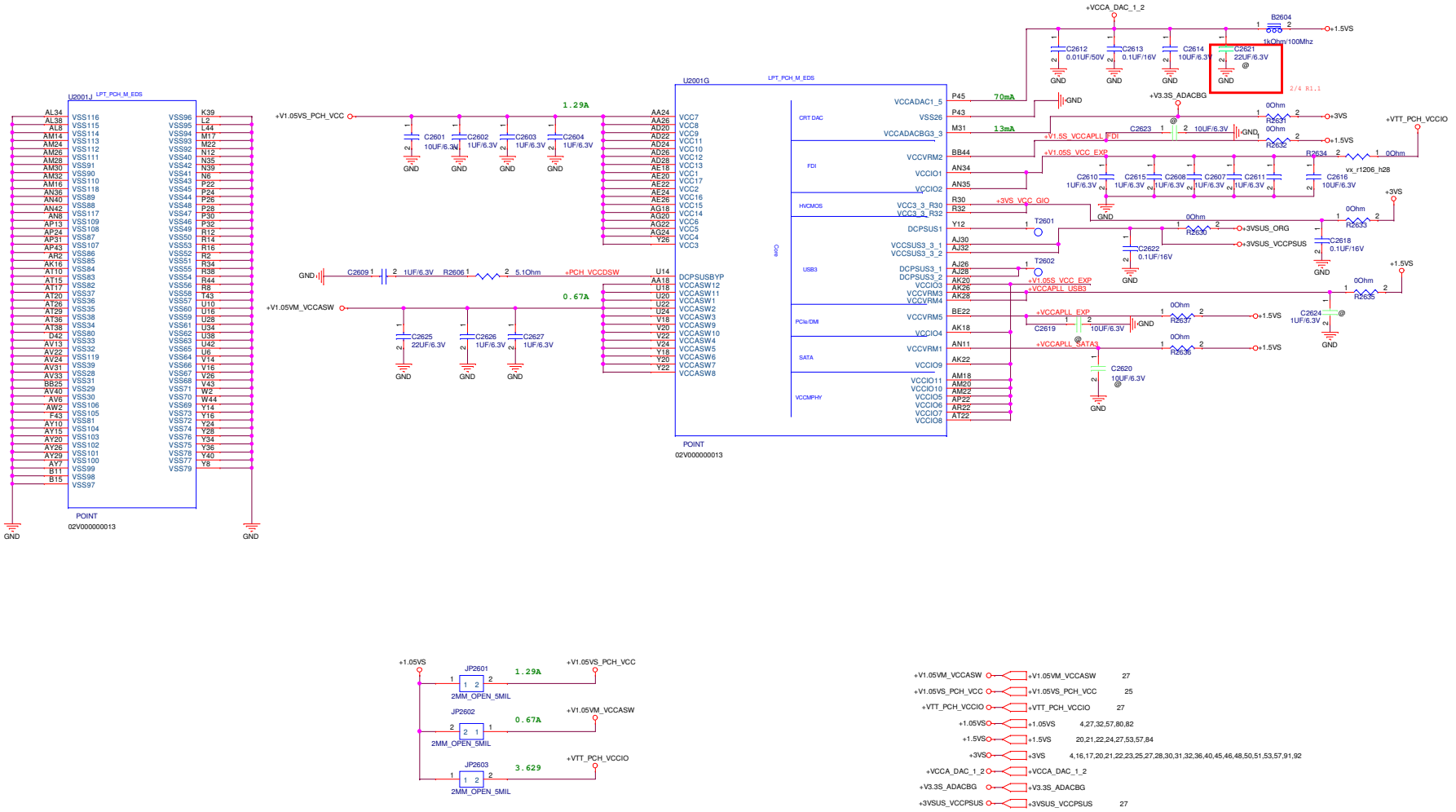
PEGATRON Title : PCH(6) CPU,GPIO,MISC
SOI CORE Engineer: Ruby Tsai
Size: D | Project Name: PT10SG | Rev: 1.1
Date: Tuesday, February 26, 2013 | Sheet 25 of 104



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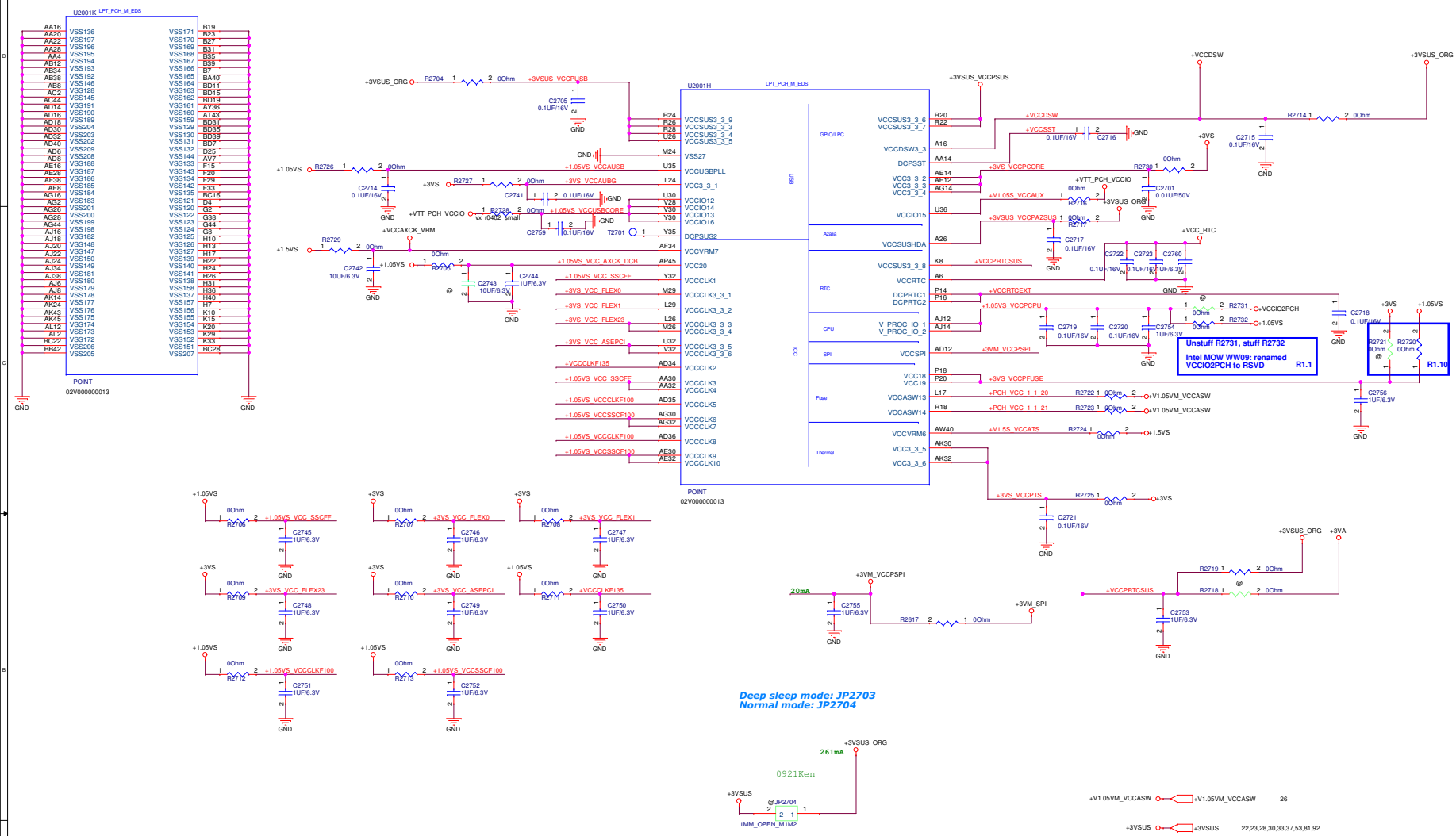
PEGATRON Title : PCH(7)_POWER,GND

BG1\CORE Engineer: Ruby Tsai

Size	Project Name	Rev
Custom	PT10SG	1.1

Date: Tuesday, February 26, 2013 Sheet 26 of 104



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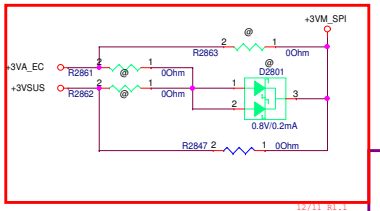
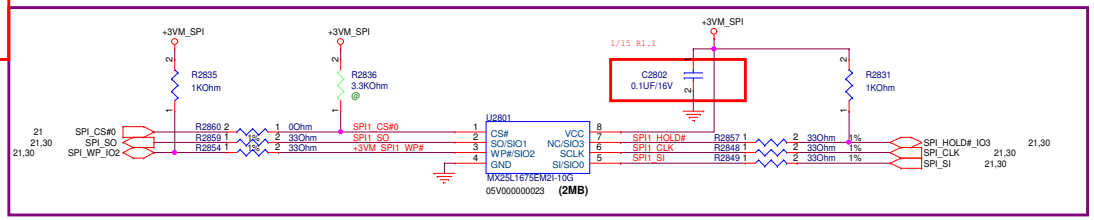
+V1.05VM_VCCASW	+V1.05VM_VCCASW 26
+3VSUS	+3VSUS 22,23,28,30,33,37,53,81,92
+3VSUS_ORG	+3VSUS_ORG 20,21,22,24,25,26
+1.5VS	+1.5VS 20,21,22,24,26,53,57,84
+3VS	+3VS 4,16,17,20,21,22,23,25,26,28,30,31,32,36,40,45,46,48,50,51,53,57,91,92
+1.05VS	+1.05VS 4,26,32,57,80,82
+VTT_PCH_VCCIO	+VTT_PCH_VCCIO 26
+VCCAXCK_VRM	+VCCAXCK_VRM 21
+3VSUS_VCCPSUS	+3VSUS_VCCPSUS 26
+3VA	+3VA 20,30,33,57,60,65,81,88,93
+VCC_RTC	+VCC_RTC 20,22
+VCCIO2PCH	+VCCIO2PCH 6

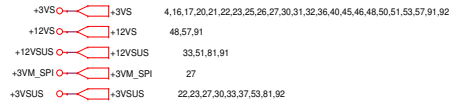
PEGATRON Title : PCH(8)_POWER,GND
BGTICORE Engineer: Ruby Tsai
Size: Custom | Project Name: PT10SG | Rev: 1.1
Date: Tuesday, February 26, 2013 | Sheet 27 of 104

PCH SPI ROM

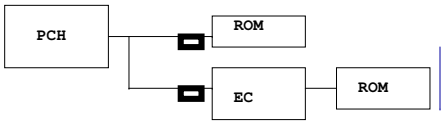




For QUAD I/O
Ruby 0928 update



	16Mb	32Mb
QUAD	05V000000023	05V000000022
DUAL	05V000000010	05V000000005

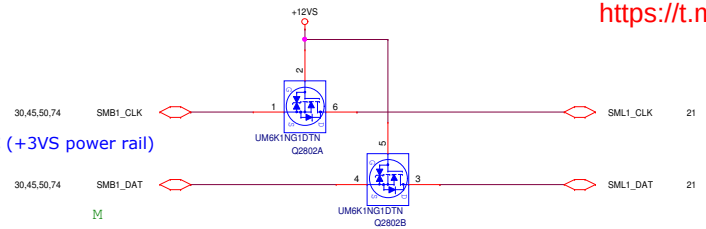


change DP to LVDS SMBus
to SCL_3A, SDA_3A
JR 0924

SMB1 Link device (+3VS)

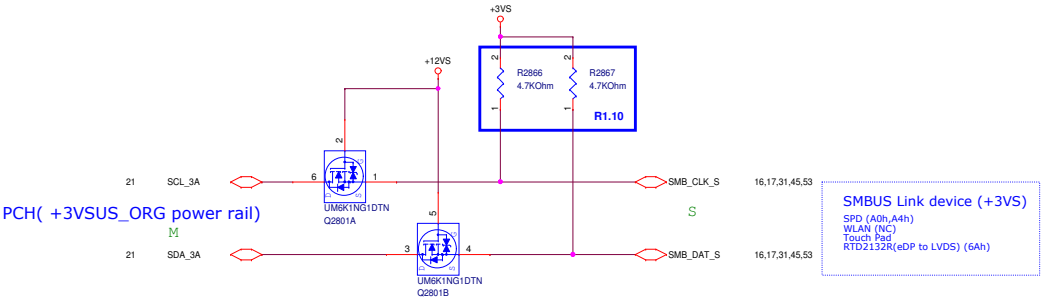
DGPU
DGPU Thermal sensor
RTD2132R(eDP to LVDS)

EC (+3VS power rail)



PCH(+3VSUS_ORG power rail)

M



PCH(+3VSUS_ORG power rail)

M

S

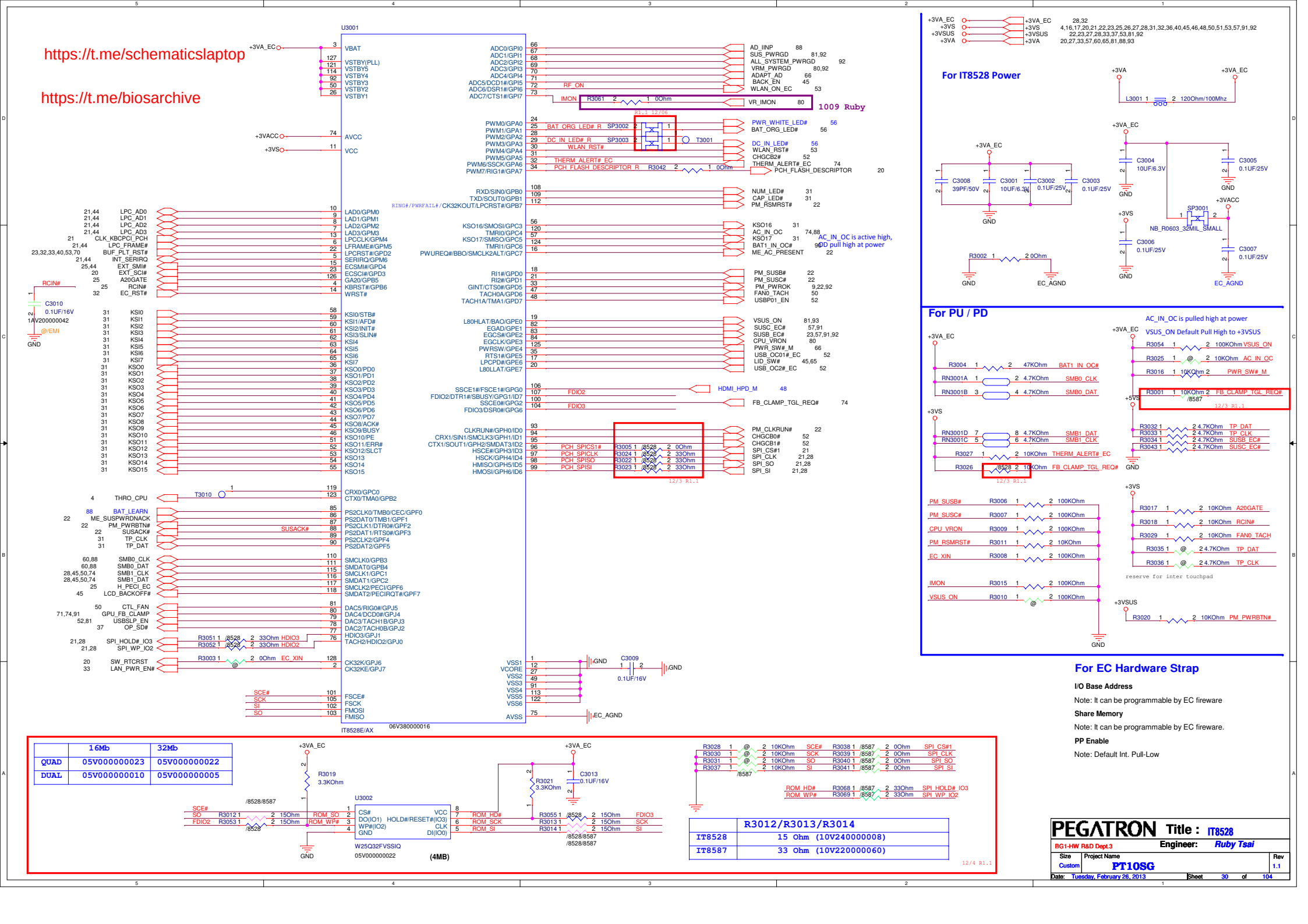
SMBUS Link device (+3VS)

SPD (A0h,A4h)
WLAN (NC)
Touch Pad
RTD2132R(eDP to LVDS) (6Ah)

remove
JR 0924

S

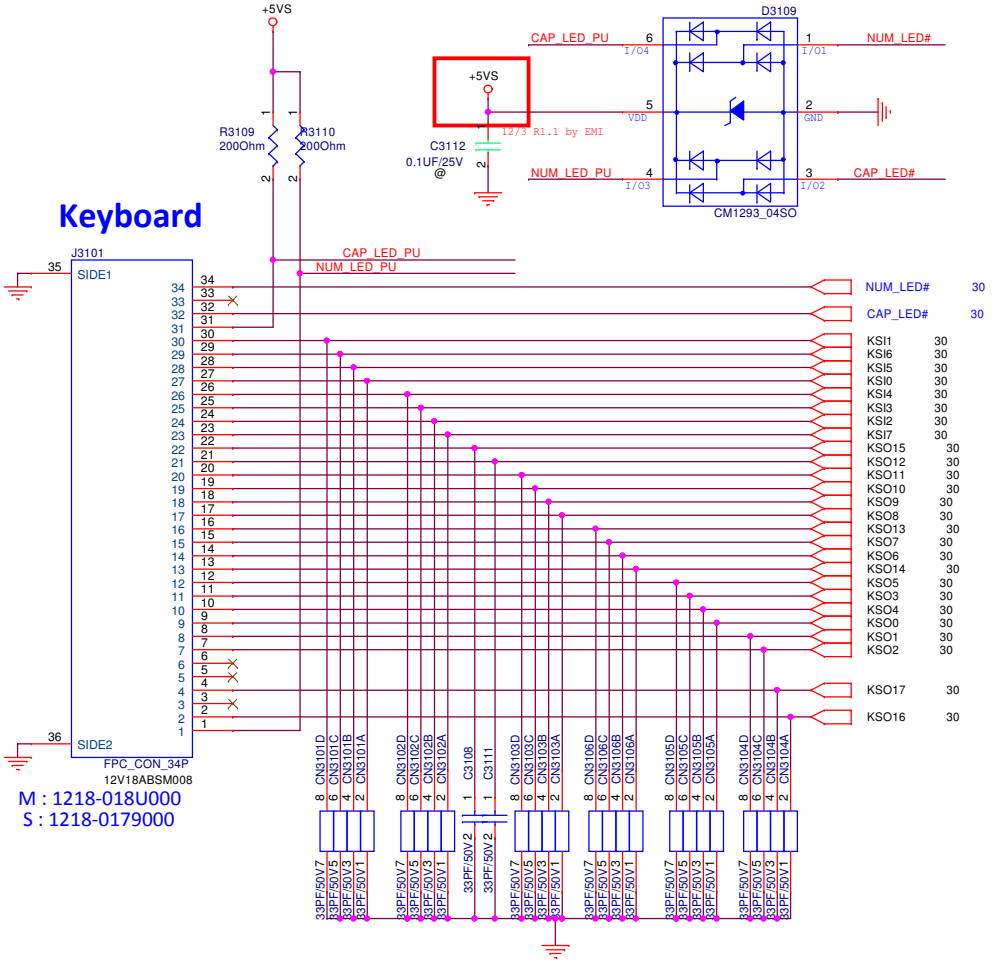
PEGATRON Title : PCH(9)_SPI,SMB
BG\CORE Engineer: Ruby Tsai
Size C | Project Name PT10SG | Rev 1.1
Date: Tuesday, February 26, 2013 | Sheet 28 of 104



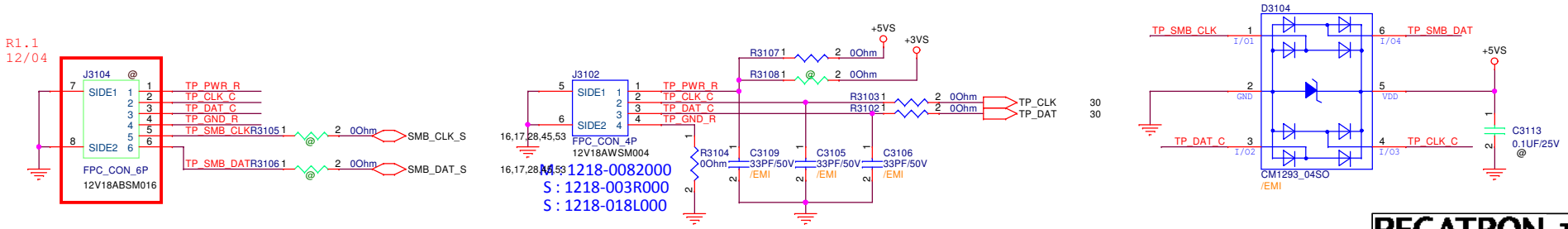
	16Mb	32Mb
QUAD	05V000000023	05V000000022
DUAL	05V000000010	05V000000005

KB CONNECTER FOR 15"

Keyboard



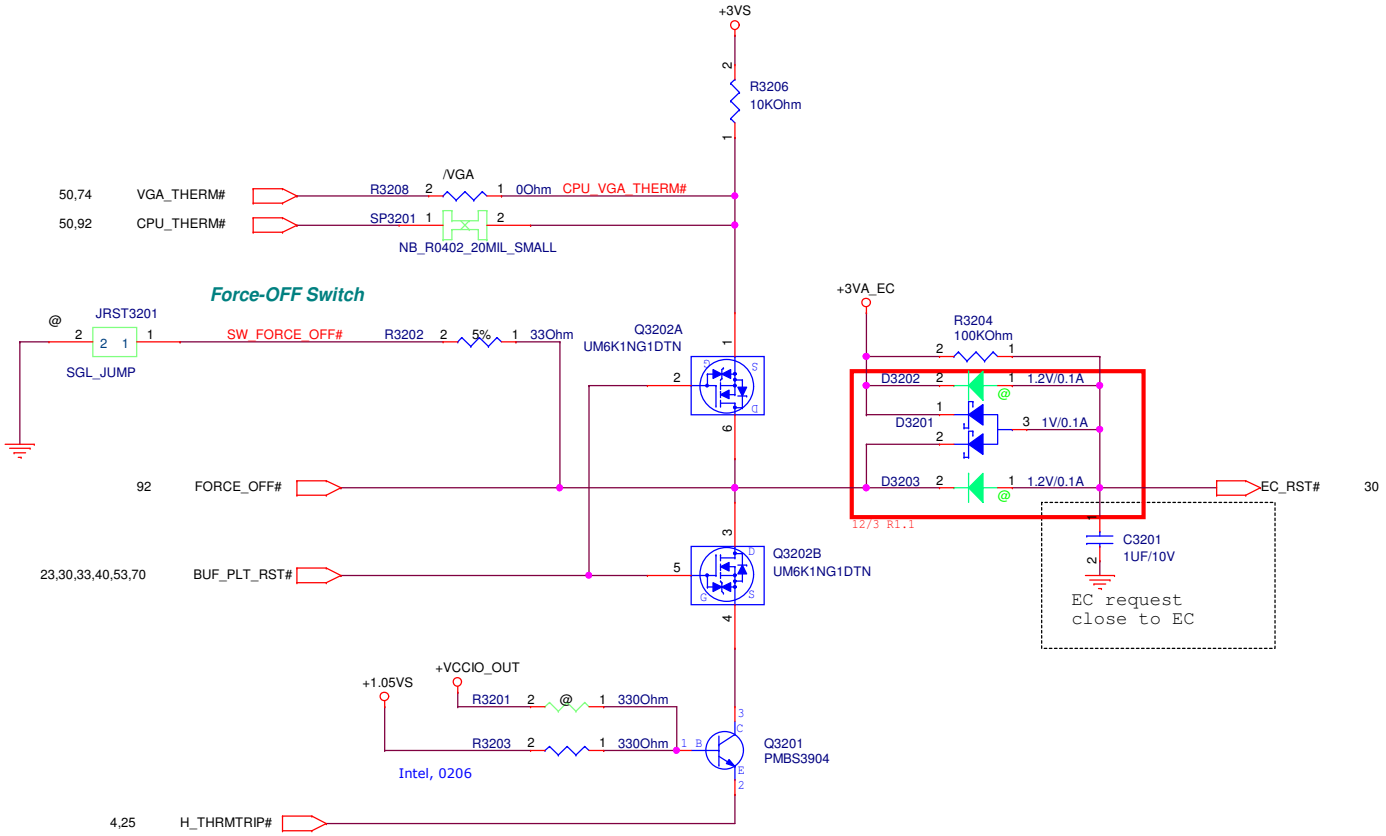
Touch Pad Module



PEGATRON	Title : KB/ TP/ FLASH	
BG1-HW R&D Dept.3	Engineer:	
Size: Custom	Project Name: PT10SG	Rev: 1.1
Date: Tuesday, February 26, 2013	Sheet 31 of 102	

Thermal Policy

+3VA_EC ——— +3VA_EC 28,30
+3VS ——— +3VS 4,16,17,20,21,22,23,25,26,27,28,30,31,36,40,45,46,48,50,51,53,57,91,92

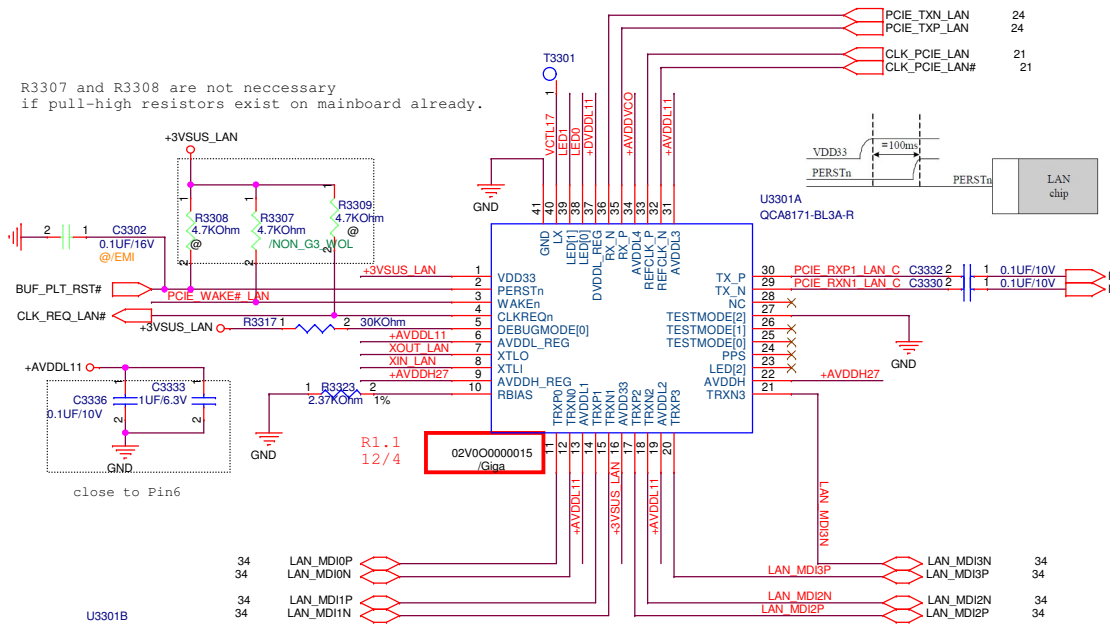


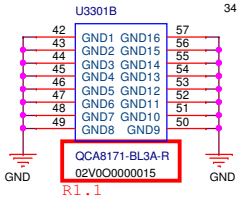
PEGATRON	Title : RST_Reset Circuit		
BG1\CORE	Engineer: Ruby Tsai		
Size: B	Project Name: PT10SG		Rev: 1.1
Date: Tuesday, February 26, 2013	Sheet 32 of 104		

ATHEROS/QCA8171(gigaLAN)	02V0O0000015
ATHEROS/QCA8172(100LAN)	02V0O0000016

3.3V Current/Power	QCA8171	QCA8172
LDO mode	277mA/915mW	111mA/366mW
SWR mode	136mA/448 mW	56mA/183mW

R3307 and R3308 are not neccessary
if pull-high resistors exist on mainboard already.



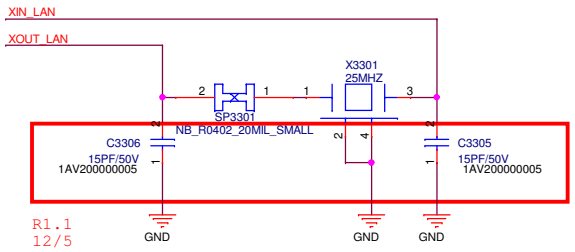


R1.1
12/4

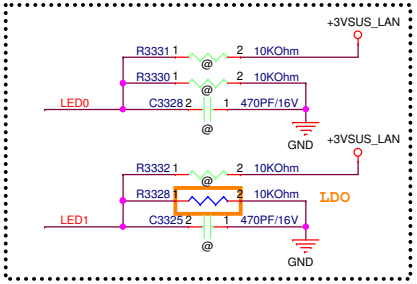
close to Pin6

LED[0] -> 1:High core voltage ; 0:Low core voltage
LED[1] -> 1:SWR ; 0:LDO

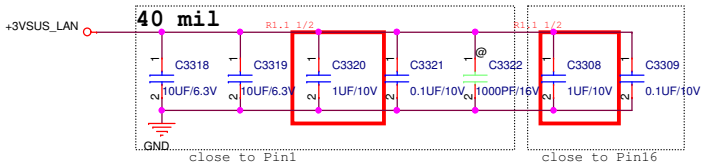
Both LEDO and LED1 with internal pull-high resistors in the chip,
R3328, R3330, R3331 and R3332 must be removed.

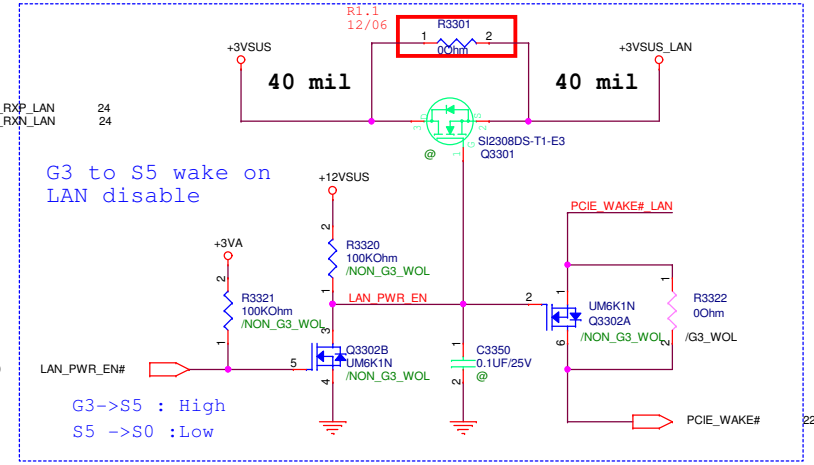


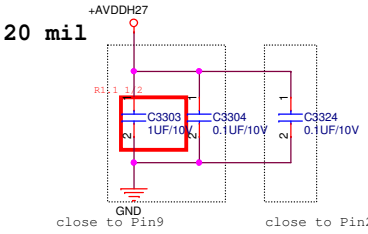
R1.1
12/5

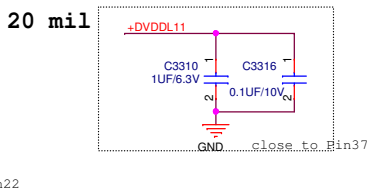


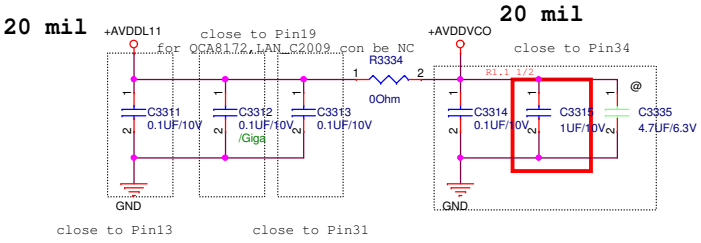
For QCA8171-C, it can
only work at high core
voltage mode











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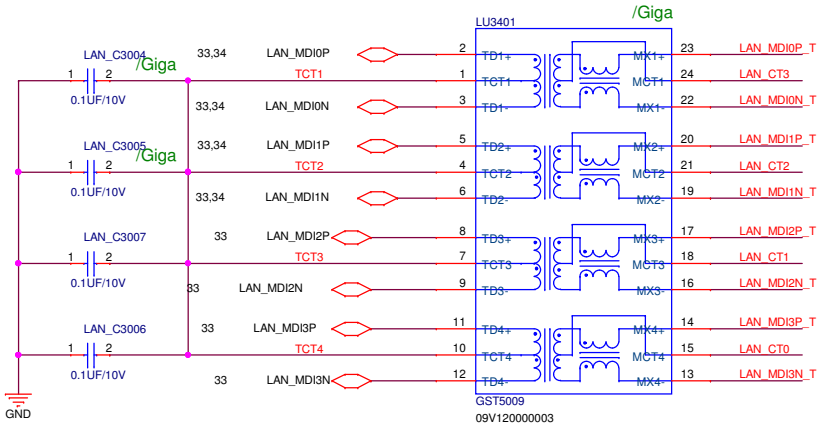
PEGATRON
Title : Atheros QCA8171-C
PEGATRON · UNIHAN CORP.
Engineer: Tina_Lee
Size: Custom
Project Name: PT10SG
Rev: 1.1
P/N:
Date: Tuesday, February 26, 2013
Sheet 33 of 99



Transformer 1G close J3401

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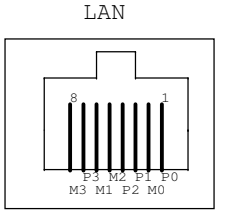
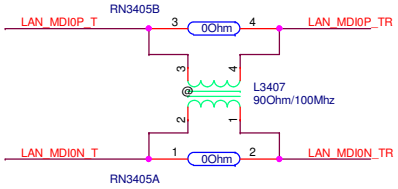
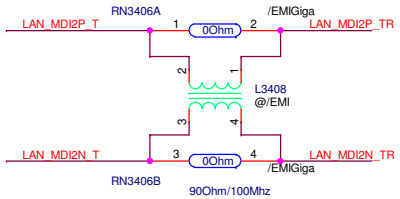
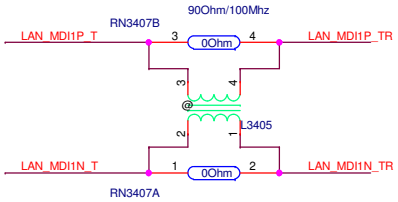
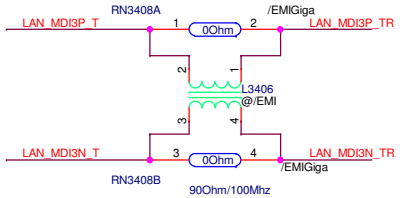
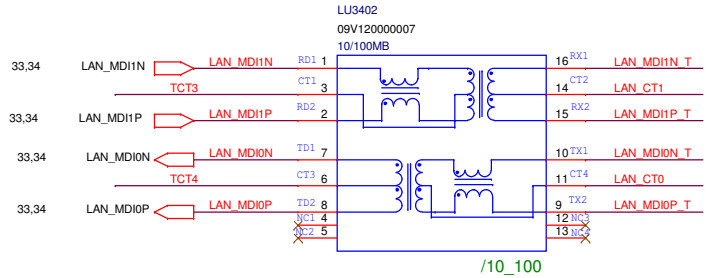






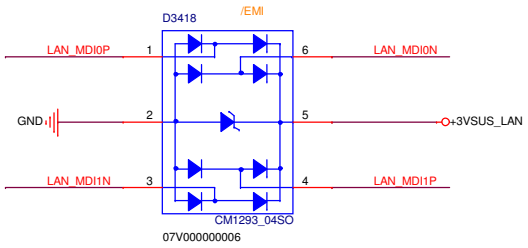


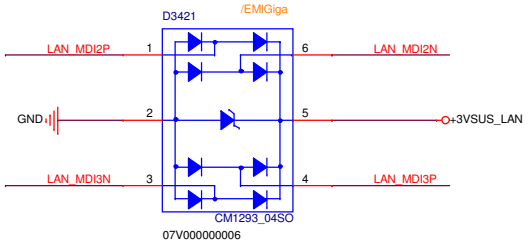


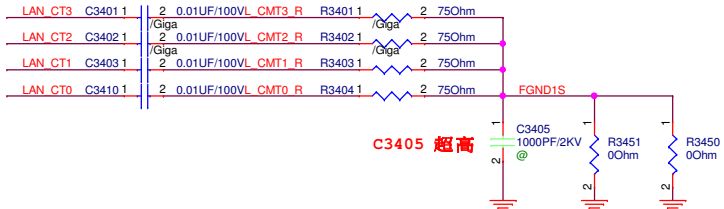


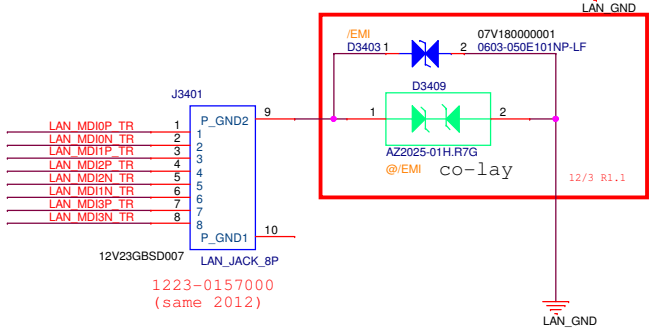
Transformer close J3401

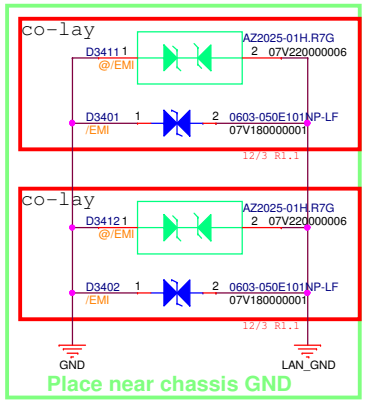
10M/100M











PEGATRON	Title : RJ45		
PEGATRON · UNIHAN CORP.	Engineer: Tina Lee		
Size: Custom	Project Name: PT10SG		Rev: 1.1
	P/N		
Date: Tuesday, February 26, 2013	Sheet 34 of 95		

Audio Codec

Intel 1.01 Design Guide update #440484
R1.3 use dual mosfet

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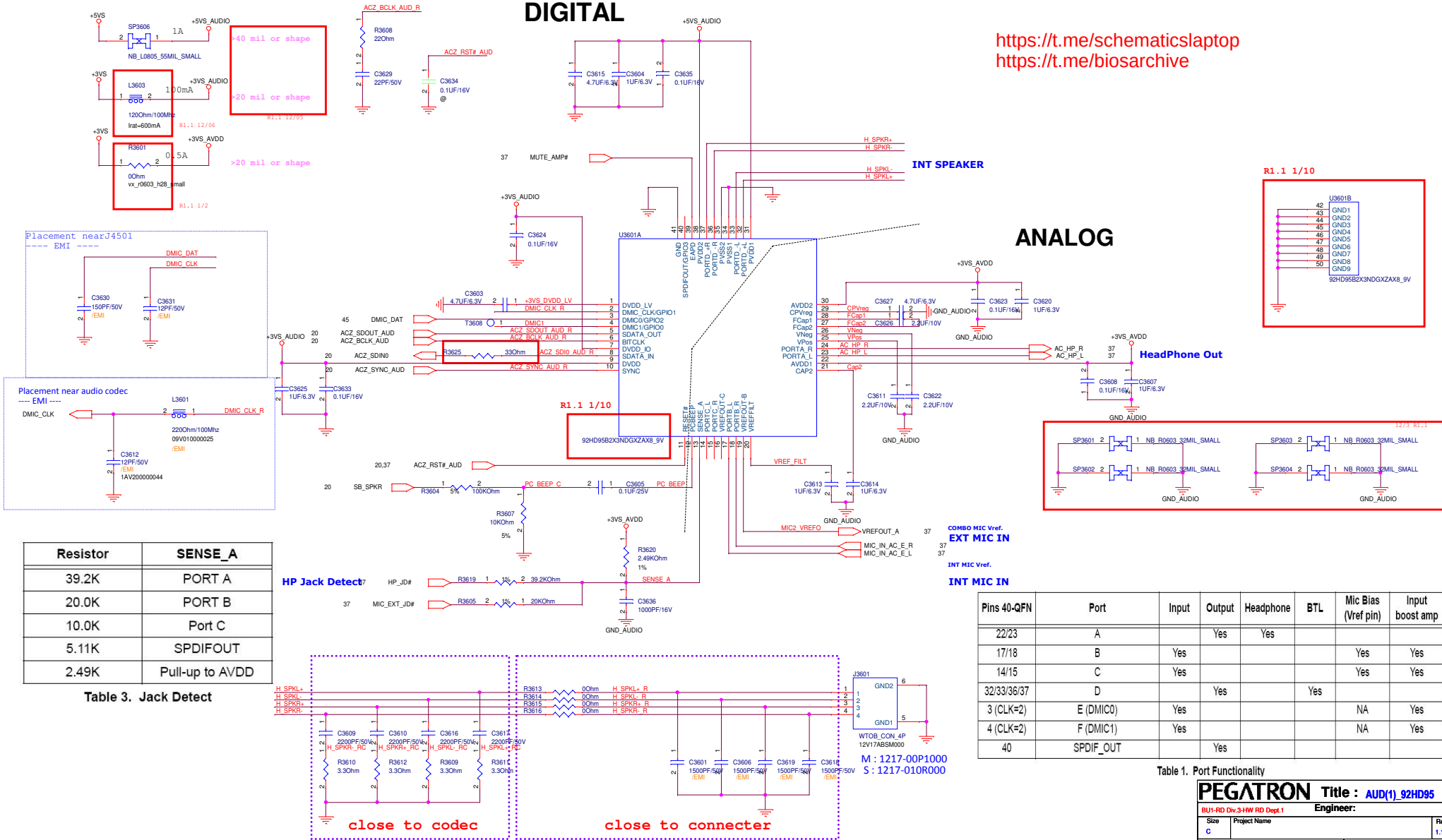
+5VS → +5VS 30,31,46,48,50,51,56,57,66,80,87,91
+3VS → +3VS 4,16,17,20,21,22,23,25,26,27,28,30,31,32,40,45,46,48,50,51,53,57,91,92

DIGITAL

ANALOG

https://t.me/schematicslaptop
https://t.me/biosarchive



Resistor	SENSE_A
39.2K	PORT A
20.0K	PORT B
10.0K	Port C
5.11K	SPDIFOUT
2.49K	Pull-up to AVDD

Table 3. Jack Detect

Pins 40-QFN	Port	Input	Output	Headphone	BTL	Mic Bias (Vref pin)	Input boost amp
22/23	A		Yes	Yes			
17/18	B	Yes				Yes	Yes
14/15	C	Yes				Yes	Yes
32/33/36/37	D		Yes		Yes		
3 (CLK=2)	E (DMIC0)	Yes				NA	Yes
4 (CLK=2)	F (DMIC1)	Yes				NA	Yes
40	SPDIF_OUT		Yes				

Table 1. Port Functionality

PEGATRON Title : AUD(1)_92HD95
BU1-RD Div.3-HW RD Dept.1 Engineer:
Size C | Project Name | Rev 1.1
Date: Tuesday, February 26, 2013 | Sheet 36 of 99

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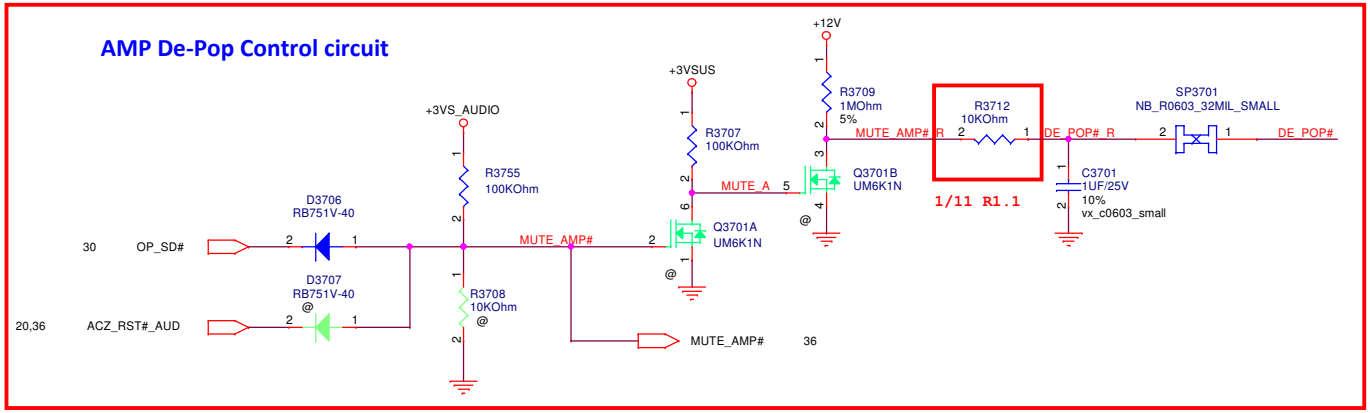
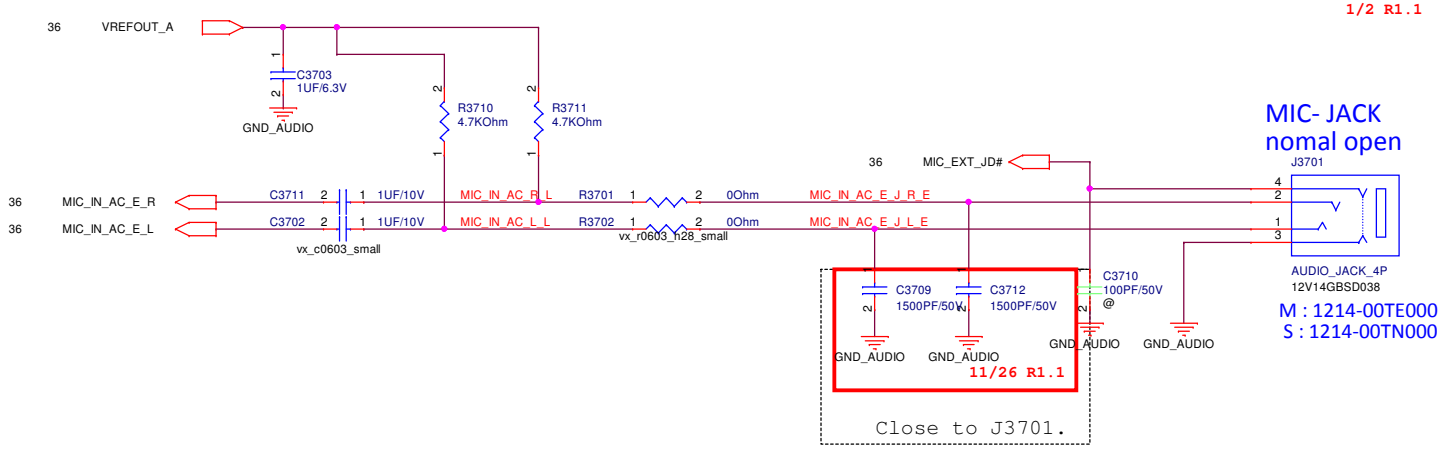
AMP De-Pop Control circuit

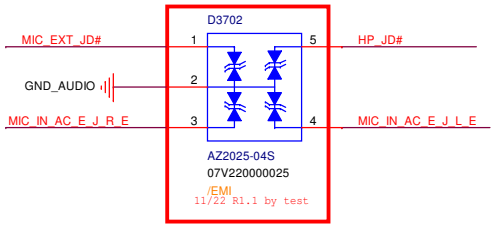


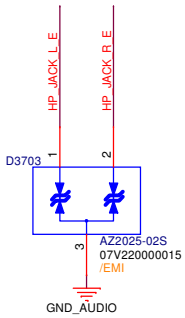
1/2 R1.1

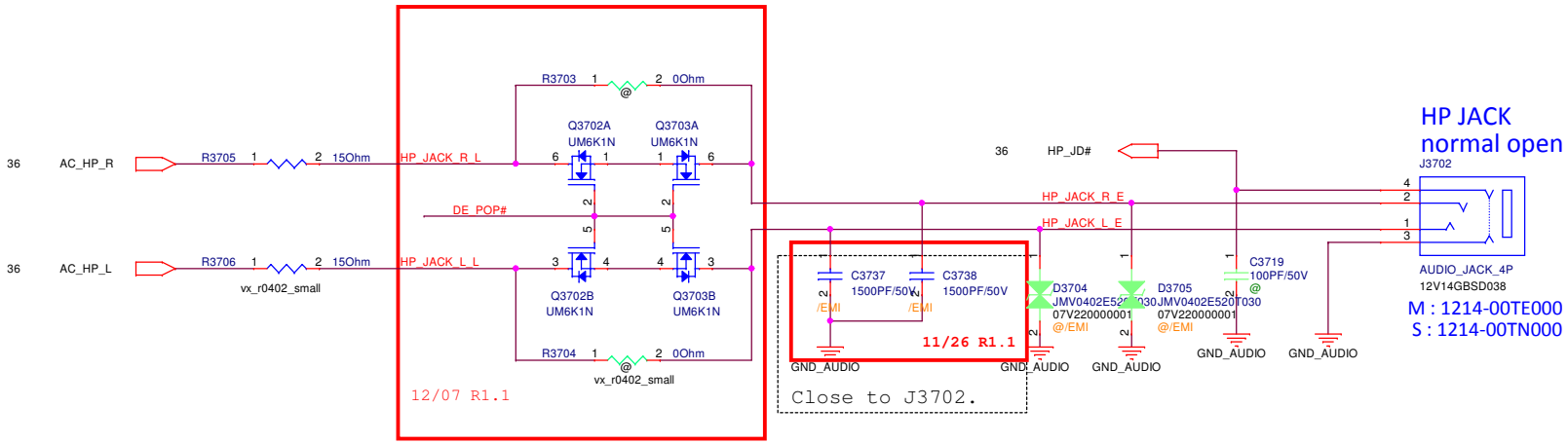


MIC- JACK
nomal open

M : 1214-00TE000
S : 1214-00TN000



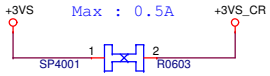


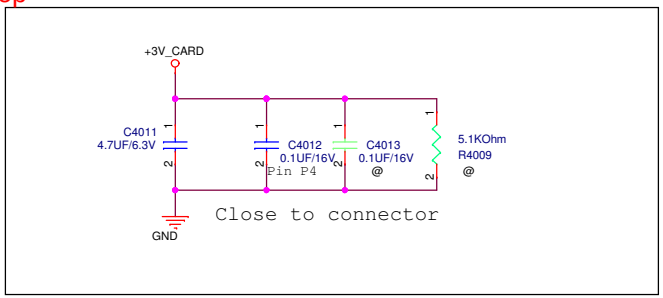


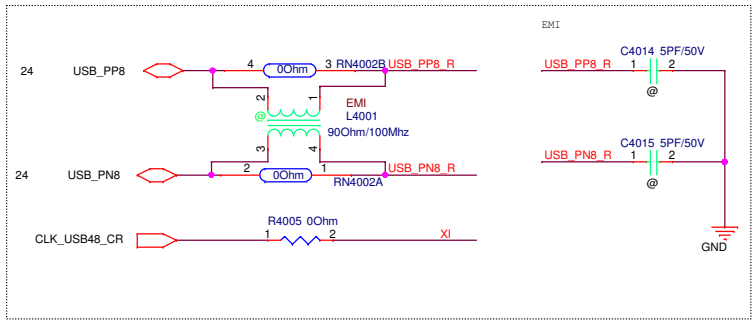
HP JACK
normal open

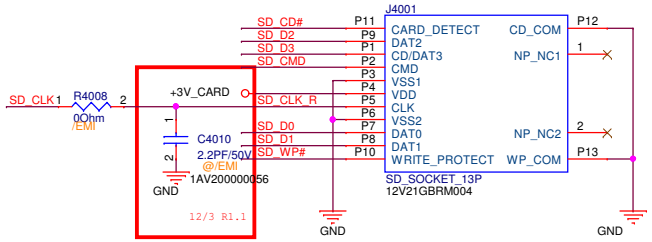
M : 1214-00TE000
S : 1214-00TN000

PEGATRON	Title : AUDIO ALC269		
BG1-CSC-HW R&D Dept.5	Engineer:		
Size: Custom	Project Name: PT10SG		Rev: 1.1
Date: Tuesday, February 26, 2013	Sheet 37 of 104		

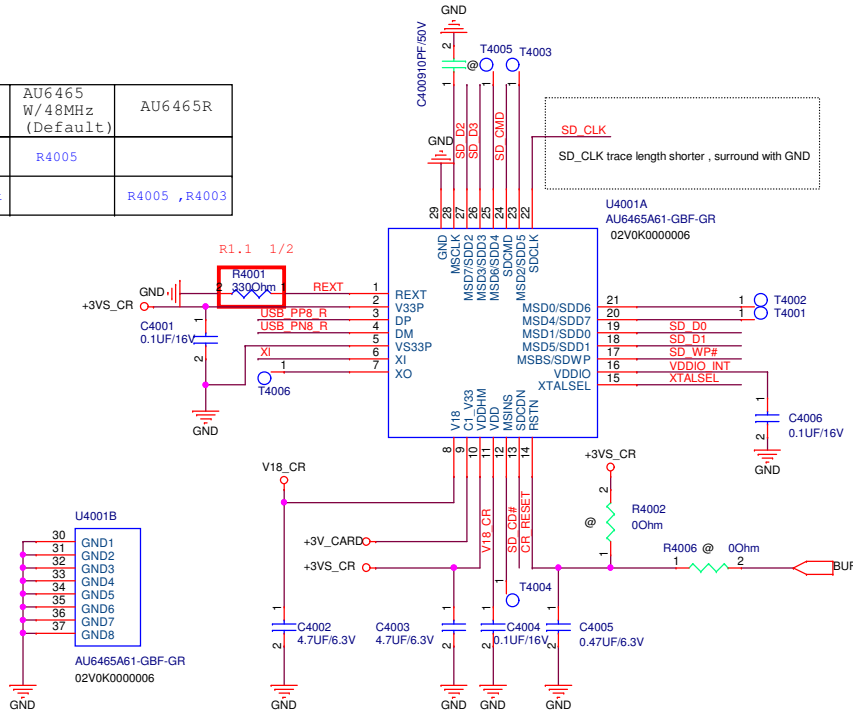


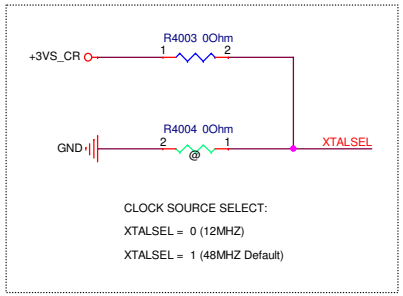






	AU6465 W/48MHz (Default)	AU6465R
Mount	R4005	
Unmount		R4005 ,R4003

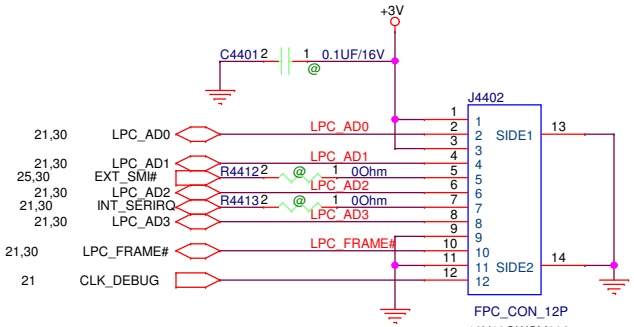




remove 12/3 R1.1

PEGATRON	Title : AU6465	
BG1-CSC-HW R&D Dept.5	Engineer: Tina_Lee	
Size: Custom	Project Name: PT10SG	Rev: 1.1
Date: Tuesday, February 26, 2013	Sheet 40 of 104	

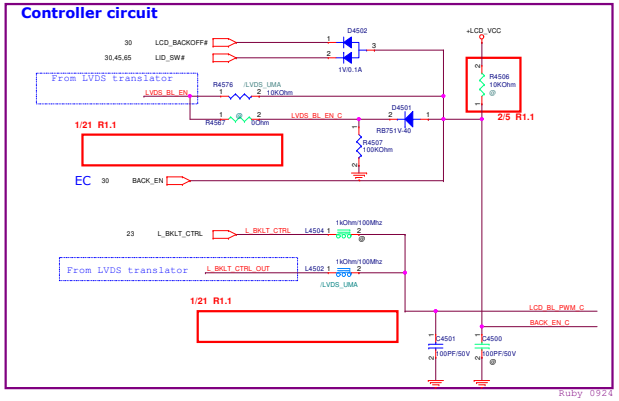
DEBUG CARD CONN.



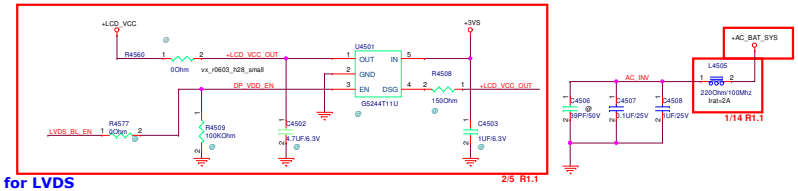
M : 1218-008L000
S : 1218-004X000
S : 1218-00AB000
S : 1218-01BX000
S : 1218-0193000

PEGATRON	Title : BUG_Debug	
BG1-CSC-HW R&D Dept.5	Engineer: Ruby Tsai	
Size: B	Project Name: PT10SG	Rev: 1.1
Date: Tuesday, February 26, 2013	Sheet 44 of 104	

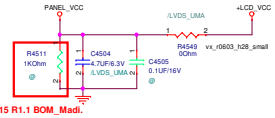
Controller circuit



LCD_VCC for eDP

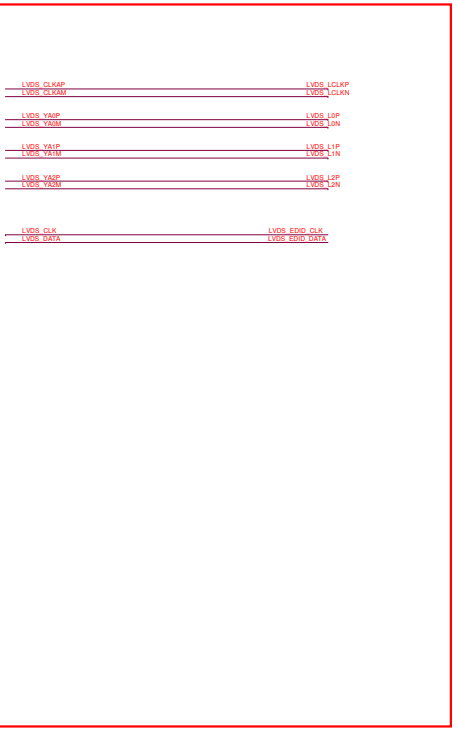


LCD_VCC for LVDS

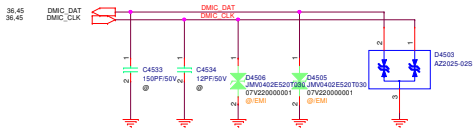


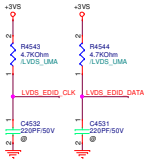
NOTE:
1. Entire trace of Panel VCC should be wider than 80-mil

12/3 R1.1 Remove

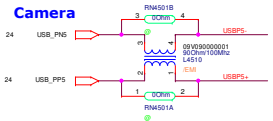


DMIC





Camera



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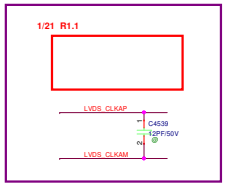
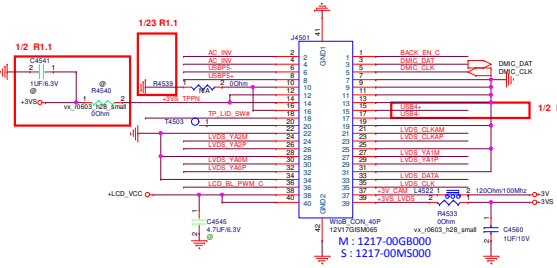
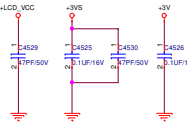
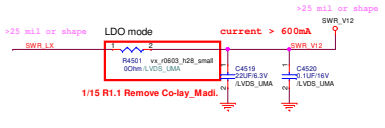
Ruby 0924

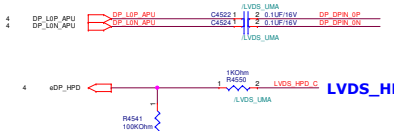


LVDS Connector

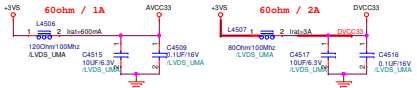




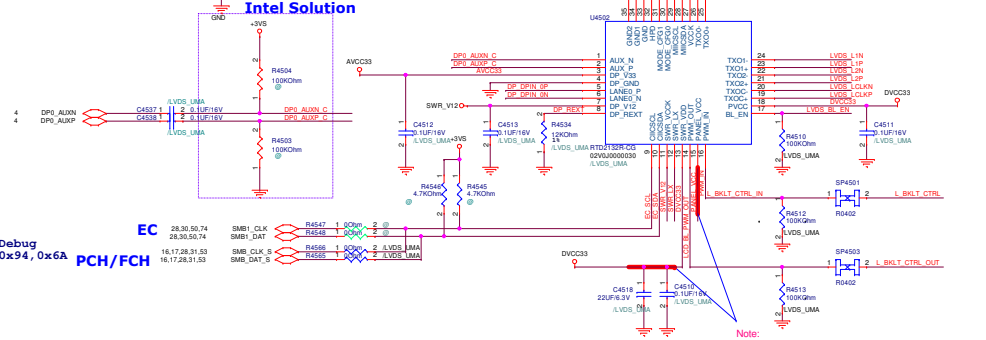




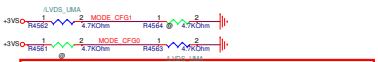
LVDS_HPD



Intel Solution



Initial Code EEPROM



1/15 R1.1 Remove EEPROM_Madi.

For RTD2132R CONFIG:

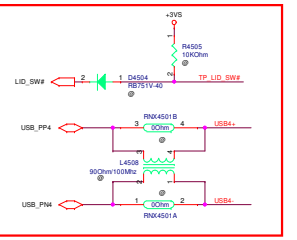
Table 2 Operation Mode Table

	PIN30	
	0	1
PIN31 0	X	EP Mode
PIN31 1	ROM	EEPROM

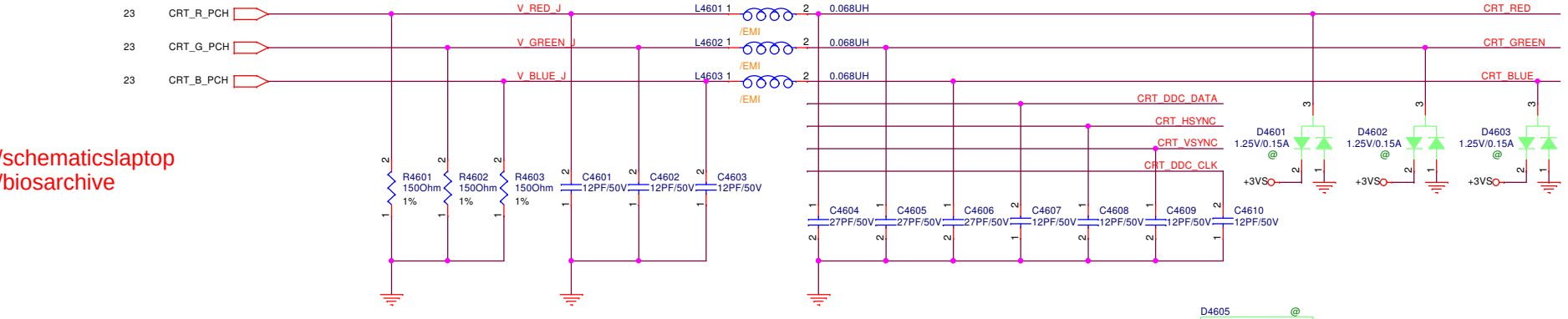
Program Debug address=0x94, 0x6A

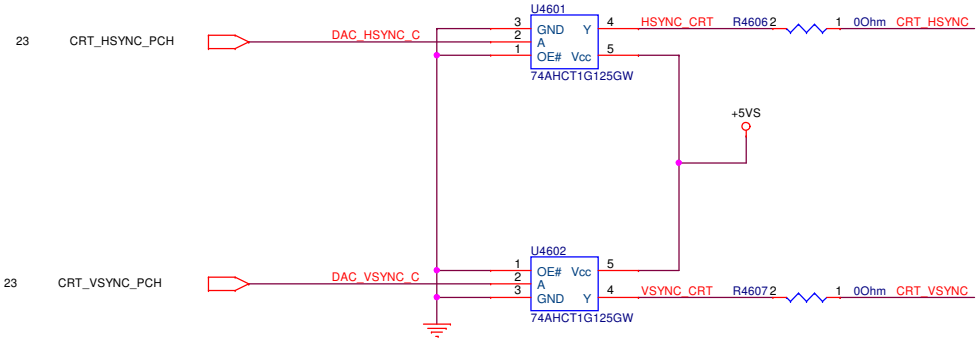
EC 28,30,50,74 SMB1_CLK
28,30,50,74 SMB1_DAT
PCH/FCH 16,17,28,31,53 SMB_CLK_S
16,17,28,31,53 SMB_DAT_S
R4547 0Ohm
R4548 0Ohm
R4566 0Ohm
R4565 0Ohm
/LVDS_UMA

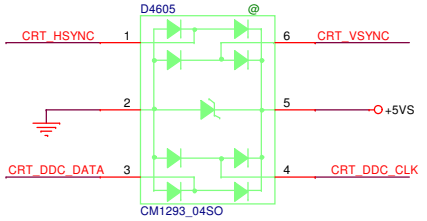
Note:
1. Entire trace of Panel VCC should be wider than 80-mil

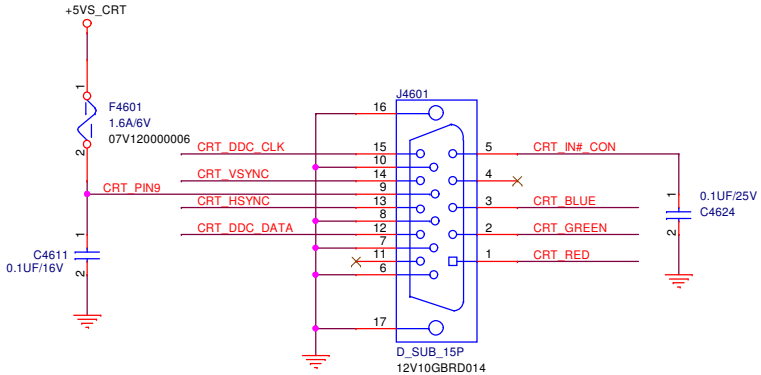


PEGATRON	Title : LVDS OUT	
	Engineer:	
Size	Project Name	Rev
Date: Tuesday, February 26, 2013	Sheet 45 of 104	

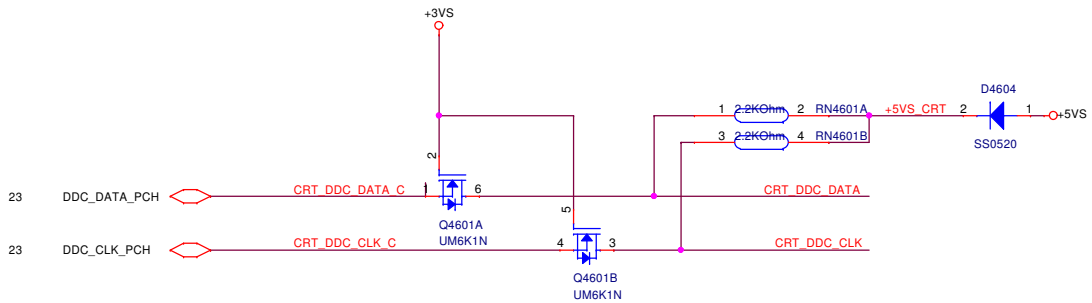


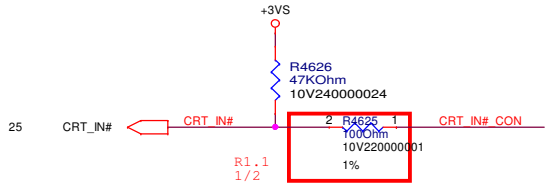






M:1210-00GB000



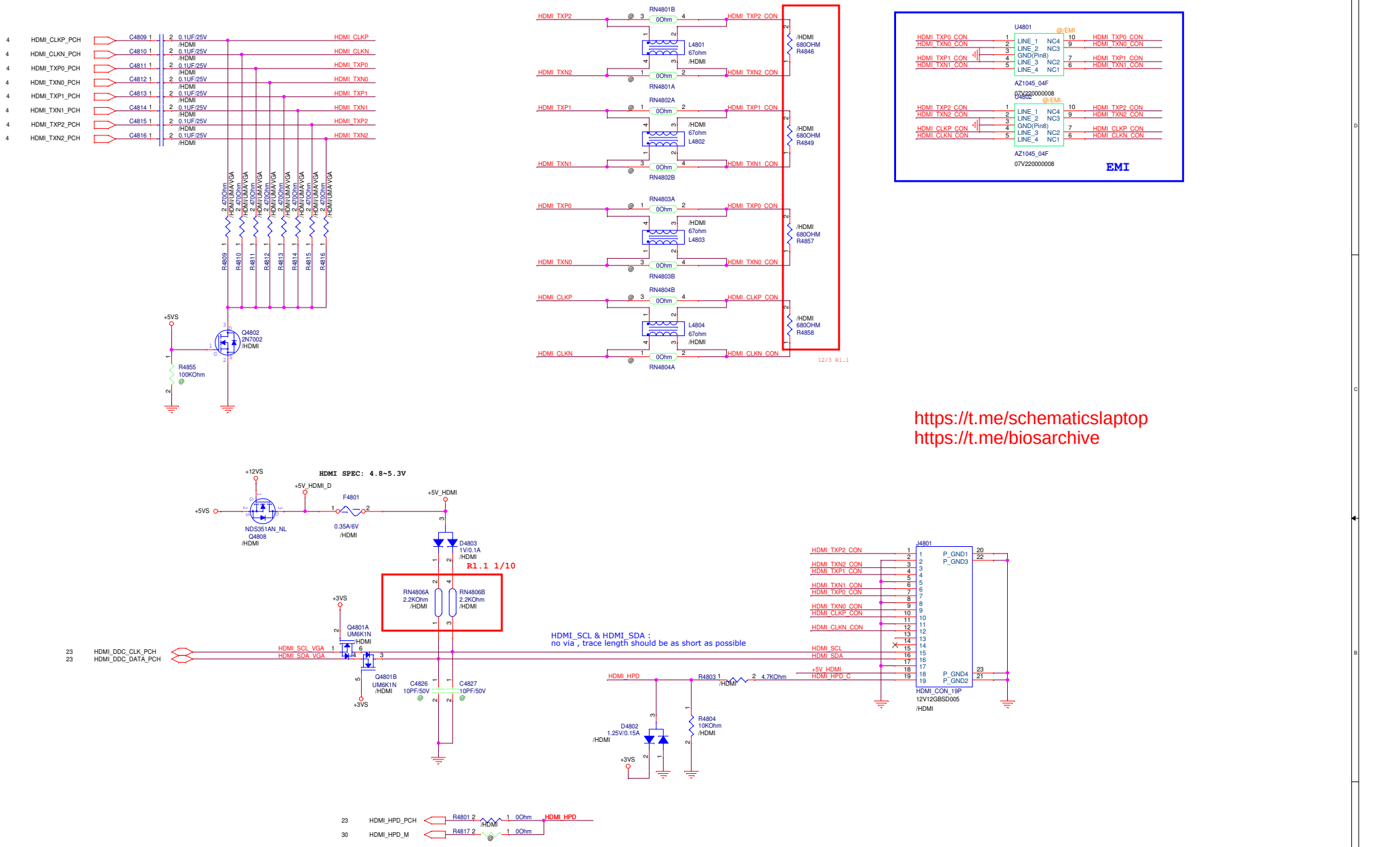


PEGATRON Title : CRT

BG1-HW R&D Dept.3 Engineer:

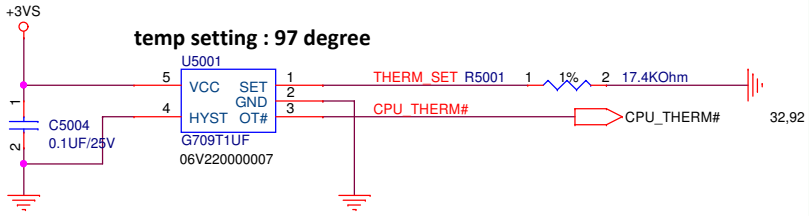
Size	Project Name	Rev
Custom	PT10SG	1.1

Date: Tuesday, February 26, 2013 Sheet 46 of 102

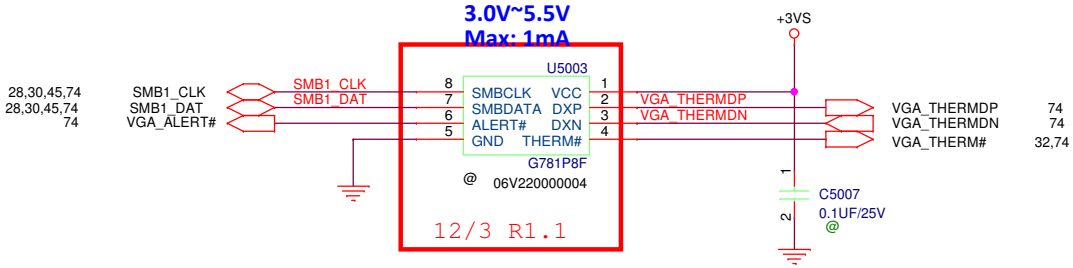


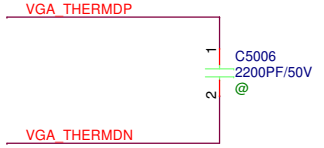
PEGATRON	Title : HDMI&CEC		
BG1-HW RD Div.2-NB RD Dept.5	Engineer: William2 Lin		
Size: C	Project Name		Rev: 1.1
Date: Tuesday, February 26, 2013	Sheet 48 of 104		

U5001 Close to CPU

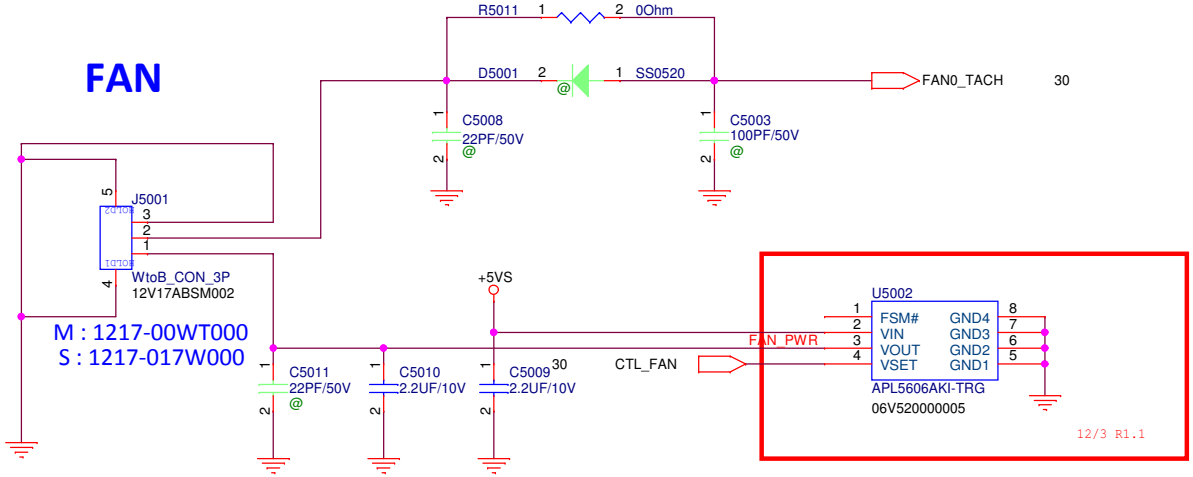


U5003 Close to GPU





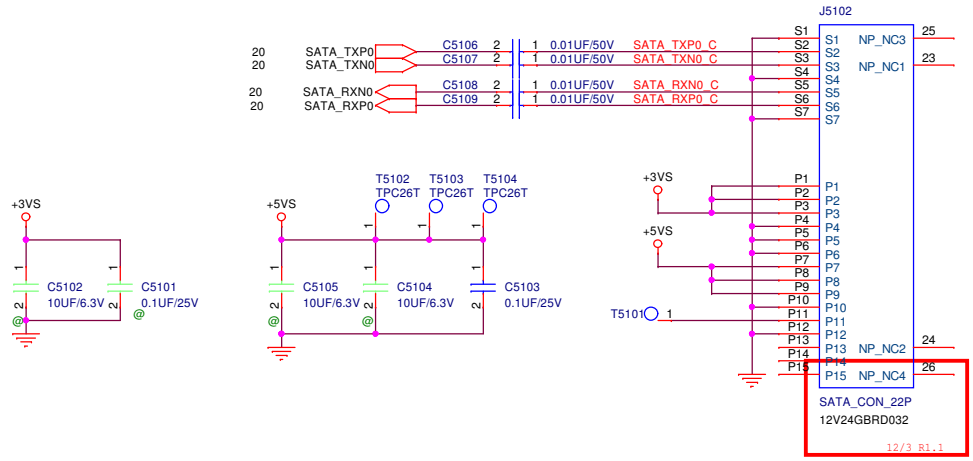
FAN



https://t.me/schematicslaptop
https://t.me/biosarchive

PEGATRON	Title : FAN / Thermal Sensor	
	Engineer: Tina Lee	
Size: Custom	Project Name: PT10SG	Rev: 1.1
Date: Tuesday, February 26, 2013	Sheet 50 of 102	

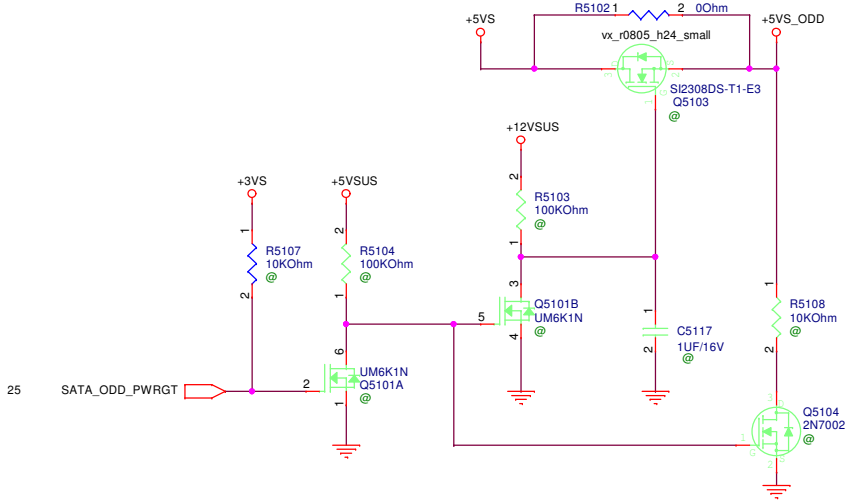
HDD



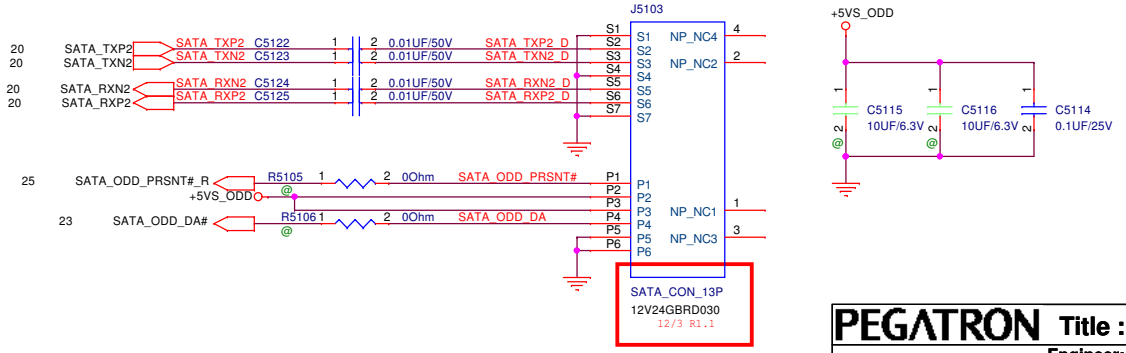
+5VS and +5VS_ODD Trace need more width to avoid blue Ray DVD rush current

ZERO POWER ODD SUPPORT

support Hokey turn off ODD power



ODD



PEGATRON

Title : SATA HDD/ ODD

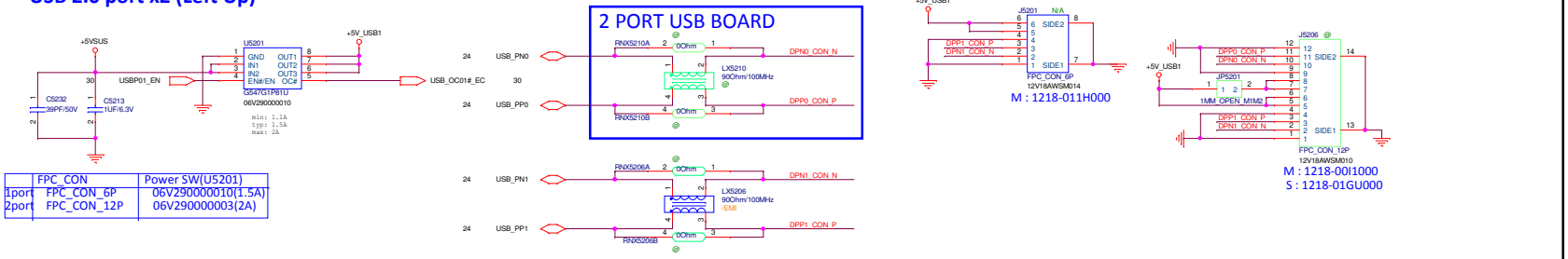
BG1-CSC-HW R&D Dept.5

Engineer:

Size	Project Name	Rev
Custom	PT10SG	1.1

Date: Tuesday, February 26, 2013 Sheet 51 of 104

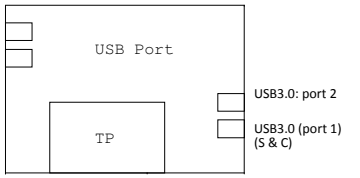
USB 2.0 port x2 (Left Up)



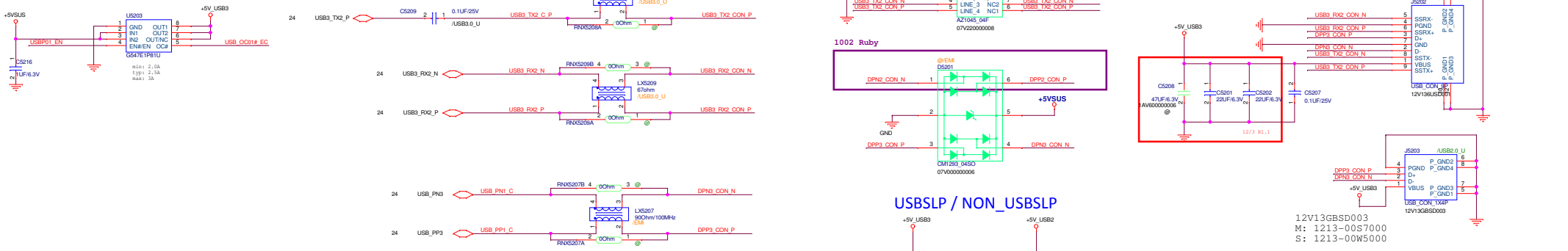
	FPC_CON	Power SW(U5201)
1port	FPC_CON_6P	06V290000010(1.5A)
2port	FPC_CON_12P	06V290000003(2A)

For 2port USB Board

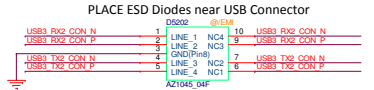
For 2port USB Board



USB 3.0 ports x 1 (Right Up)

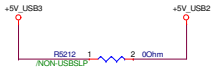


PLACE ESD Diodes near USB Connector

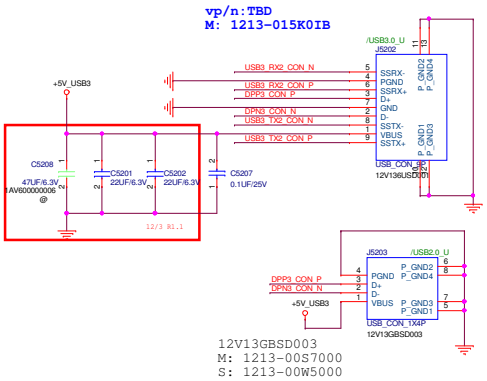


1002 Ruby

USBSLP / NON_USBSLP



vp/n:TBD
M: 1213-015K0IB



12V13GBSD003
M: 1213-00S7000
S: 1213-00W5000

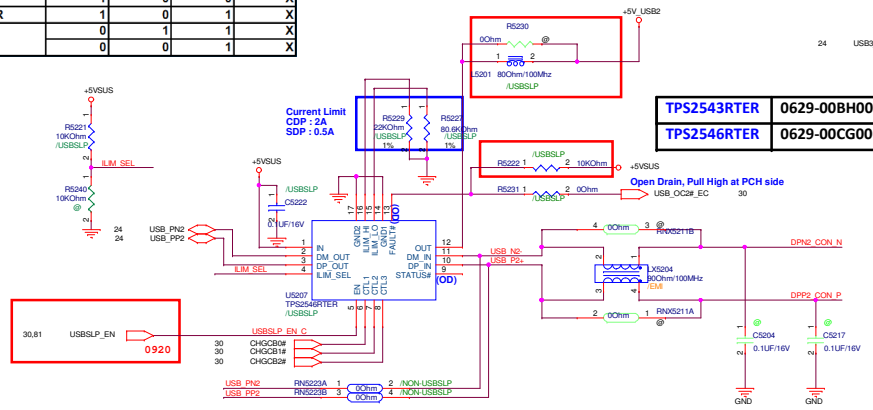
USB 3.0 ports x 1 with Sleep & Charge (Right Down)

Standard --> TPS2546RTER

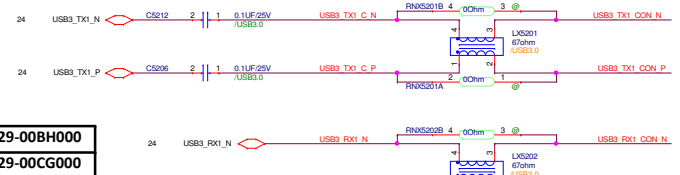
	Device Control Pins			
Flow Line Condition	CTL1	CTL2	CTL3	ILIM_SEL
DCH	0	0	0	X
CDP	1	1	1	1
SDP2	1	1	1	0
SDP1	1	1	0	X
	0	1	0	X
DCP_SHORT	1	0	0	X
DCP_DIVIDER	1	0	1	X
DCP_Auto	0	0	1	X

Tod's spec

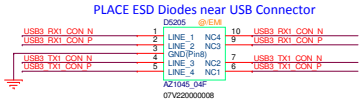
Battery Charge mode	
Apple 1.0A mode	Yes
DCP mode	Yes
Apple 2.0A mode	Yes



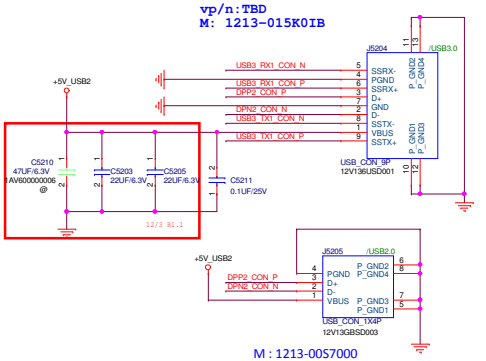
TPS2543RTER	0629-00BH000
TPS2546RTER	0629-00CG000



PLACE ESD Diodes near USB Connector



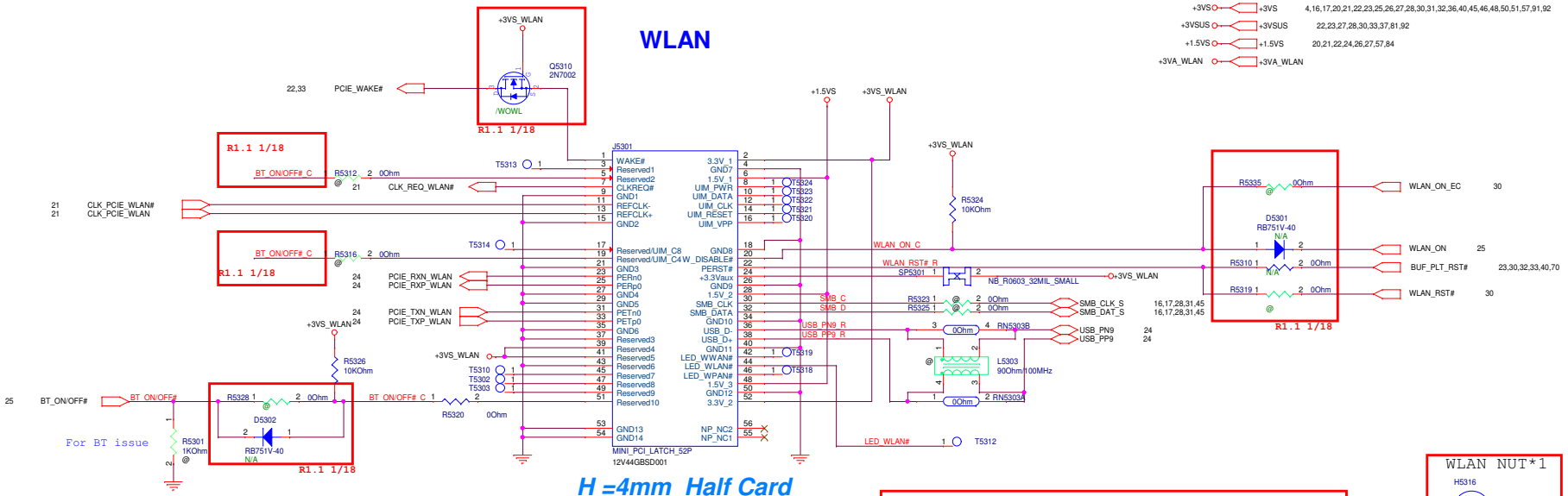
vp/n:TBD
M: 1213-015K0IB



M : 1213-00S7000
S : 1213-00R9000

PEGATRON Title : USB JACK
BGI-CSC-HW R&D Dept.5 Engineer: Ruby Tsai
Size: Custom Project Name: PT10SG Rev: 1.1
Date: Tuesday, February 26, 2013 Sheet 52 of 104

WLAN



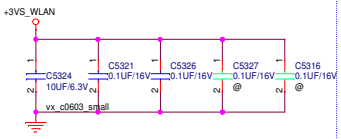
+3VS 4,16,17,20,21,22,23,25,26,27,28,30,31,32,36,40,45,46,48,50,51,57,91,92
+3VSUS 22,23,27,28,30,33,37,81,92
+1.5VS 20,21,22,24,26,27,57,84
+3VA_WLAN

H =4mm Half Card

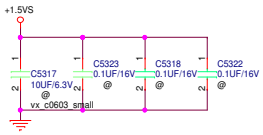
WLAN +3VS bypass capactor:

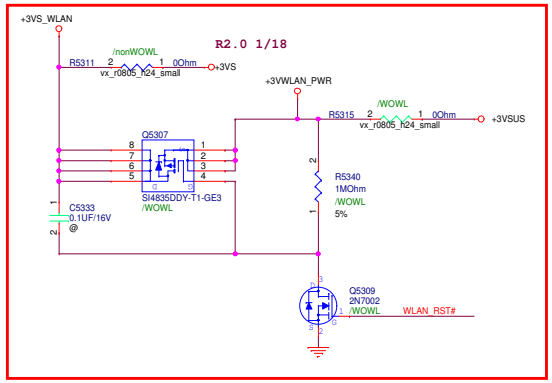
Place 0.1UF near pin 2,24,52,39 41.

Place 10UF near +3VS_WLAN source side.



WLAN +1.5VS bypass capactor:

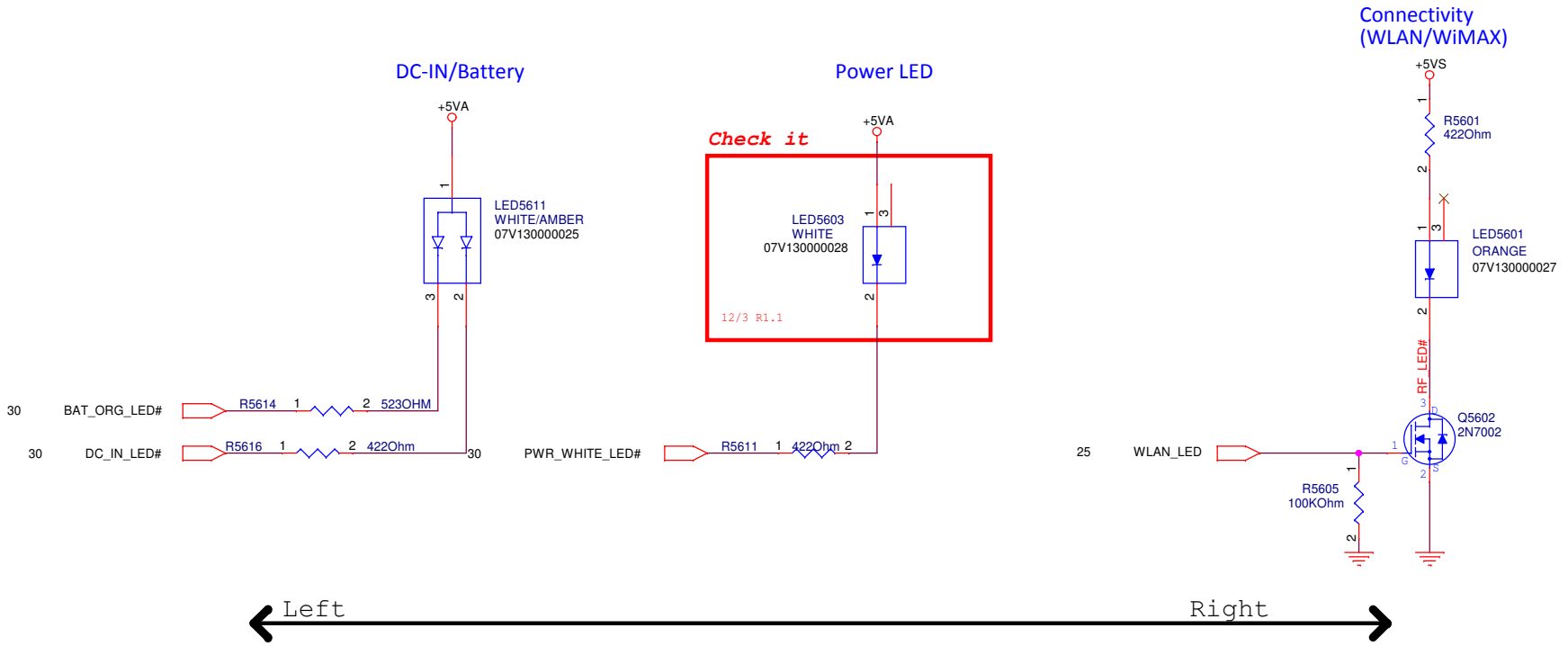




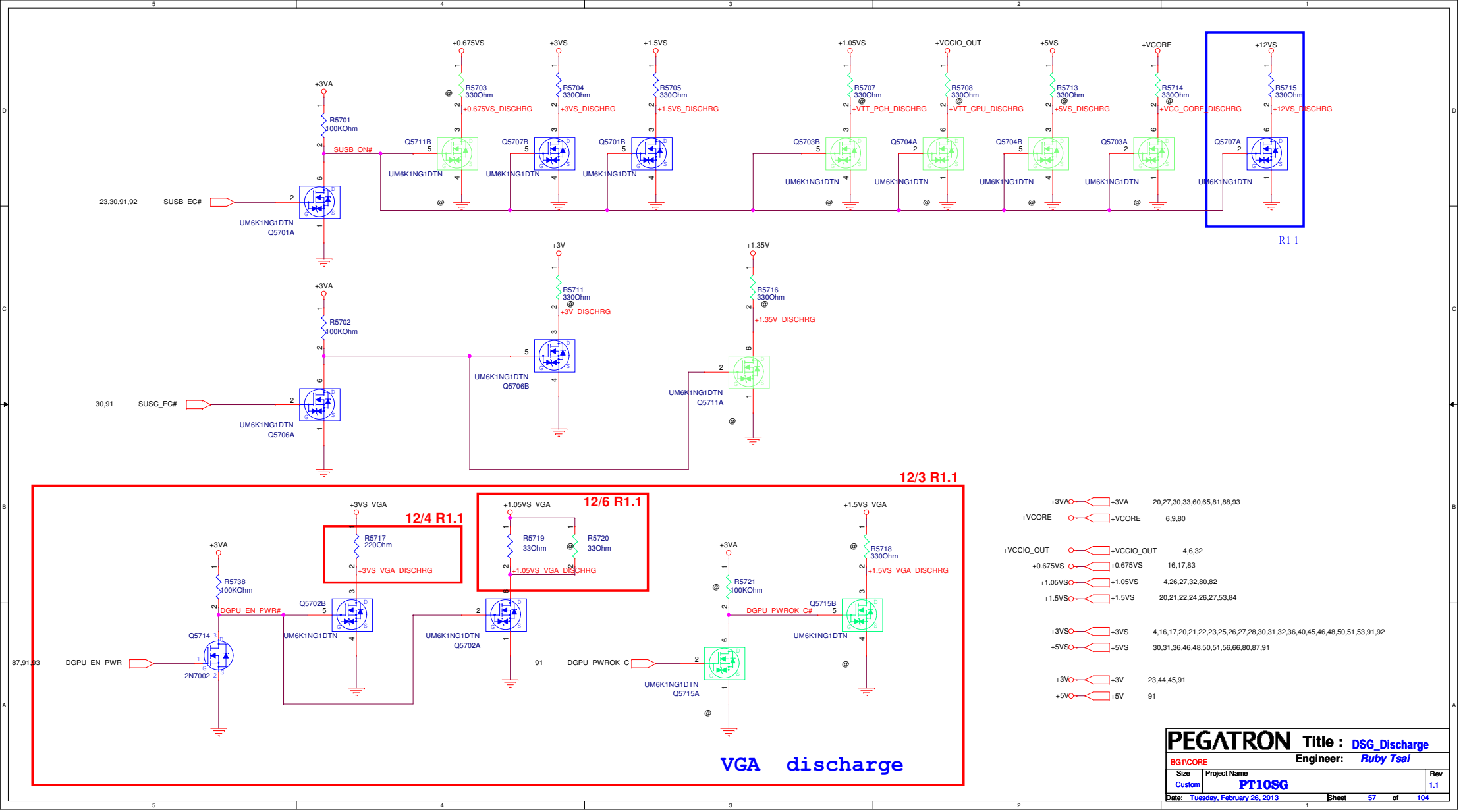
WLAN NUT*1

PEGATRON	Title : WIFI+3G		
BG1-CSC-HW R&D Dept.5	Engineer:		
Size: C	Project Name: PT10SG		Rev: 1.1
Date: Tuesday, February 26, 2013	Sheet 53 of 104		

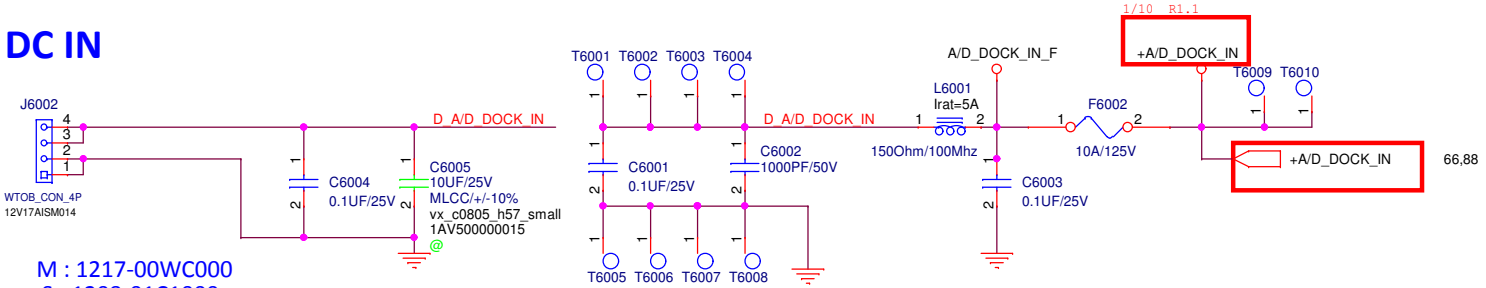
Order of Indicator LEDs
DC-IN/Battery Power WiFi



PEGATRON	Title : LED/ CIR/ FN/ SCREW	
BG1-HW R&D Dept.3	Engineer: Tina Lee	
Size: Custom	Project Name: PT10SG	Rev: 1.1
Date: Tuesday, February 26, 2013	Sheet 56 of 102	

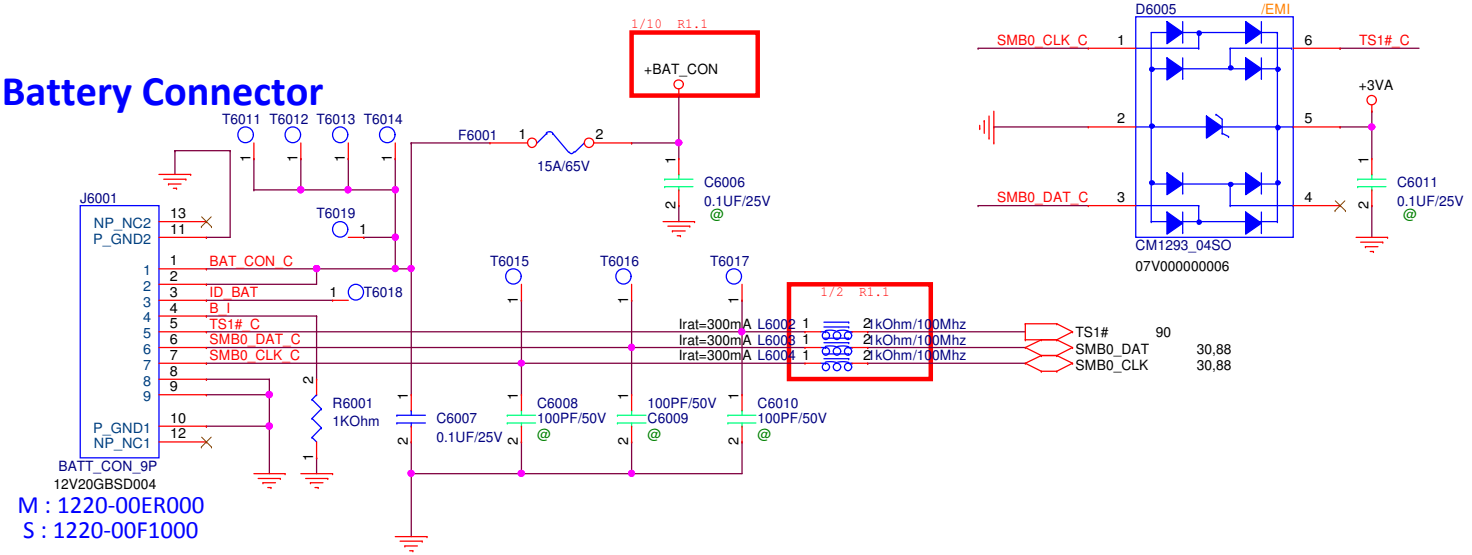


DC IN



M : 1217-00WC000
S : 1208-01C1000

Battery Connector



M : 1220-00ER000
S : 1220-00F1000

PEGATRON Title : DC-IN/ DISCHARGE

BG1-CSC-HW R&D Dept.5 Engineer: Tina Lee

Size	Project Name	Rev
Custom	PT10SG	1.1

Date: Tuesday, February 26, 2013 Sheet 60 of 104

CPU : Screw Ex4

DXF : DETAIL A

H6507 — CRT276X319B256D142
H6508 — CRT276X319B256D142
H6509 — CRT276X319B256D142
H6510 — CRT276X319B256D142

VGA : Screw Fx2

DXF : DETAIL B
TOP Side

H6511 — CT260B176D146
13V08C33B300
H6512 — CT260B176D146
13V08C33B300

1/23 R1.1

PCB : Screw Ax10

DXF : ITEAM A

H6516 — C335D98
H6501 — C335D98
H6506 — CR378x335D98
H6520 — CRT337x335CB335D98
H6521 — CRT337x335CB335D98

Locate : Screw Dx1

DXF : ITEAM D

H6525 — C335D126

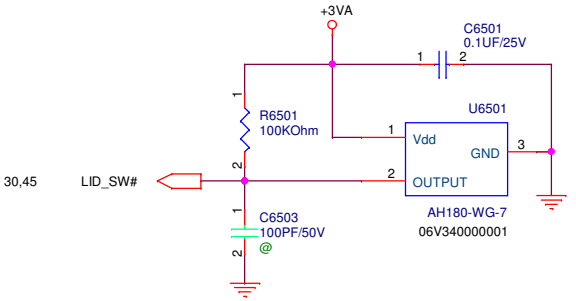
TOP/BOT : GND Cx5

DXF : ITEAM C

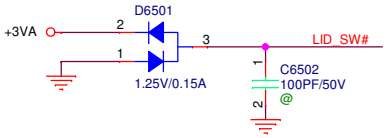
H6522 — C236
H6523 — C236
H6524 — C236
H6527 — C236
H6528 — C236
H6530 — C236
H6529 — C236
H6533 — C236
H6532 — C236

0921

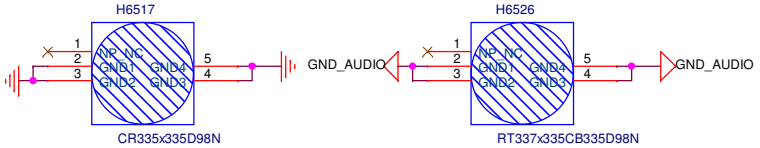
LID Switch(Hall sensor)

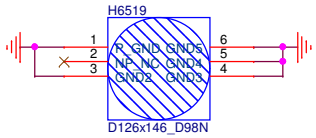


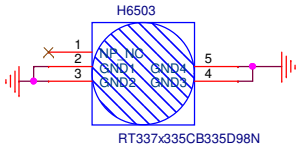
close toU3001



Note:
LID_SW# is easy to cause high voltage damage when plugging inverter board connector to M/B with AC present.
Need to add bidirectional diode to protect this pin.





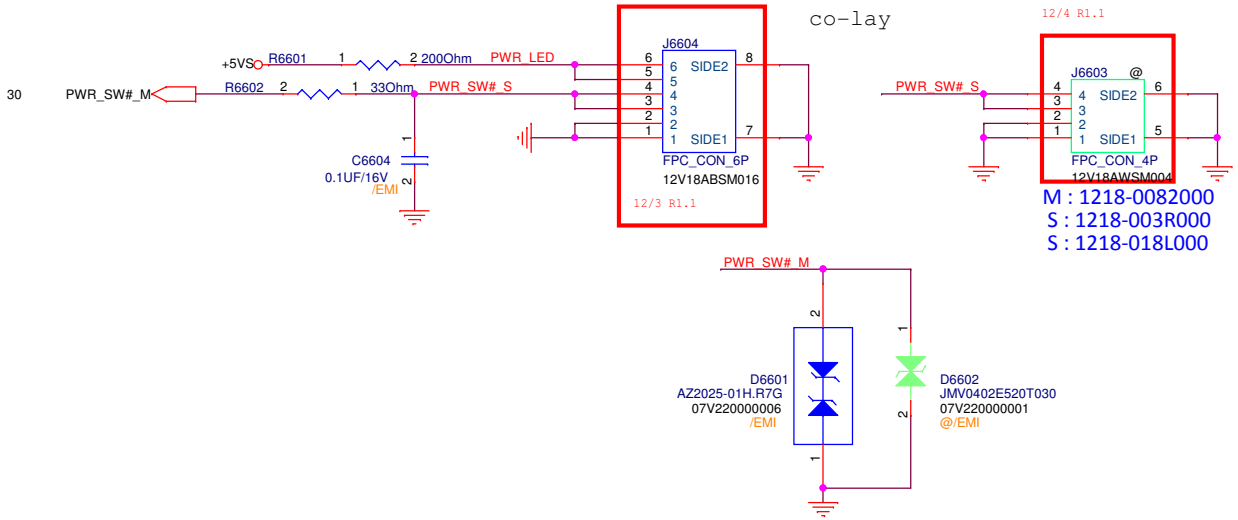


PEGATRON Title : ME_CONN,Skew Hole
Engineer: Tina Lee

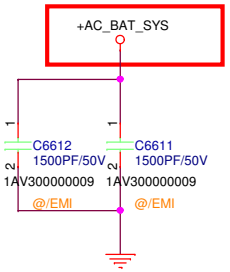
Size	Project Name	Rev
B	PT10SG	1.1

Date: Tuesday, February 26, 2013 Sheet 65 of 104

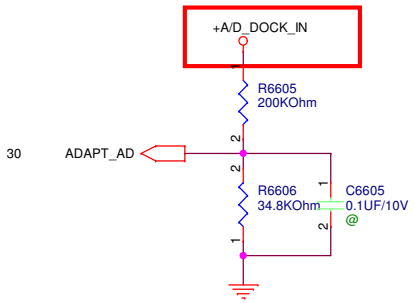
PWR BRD



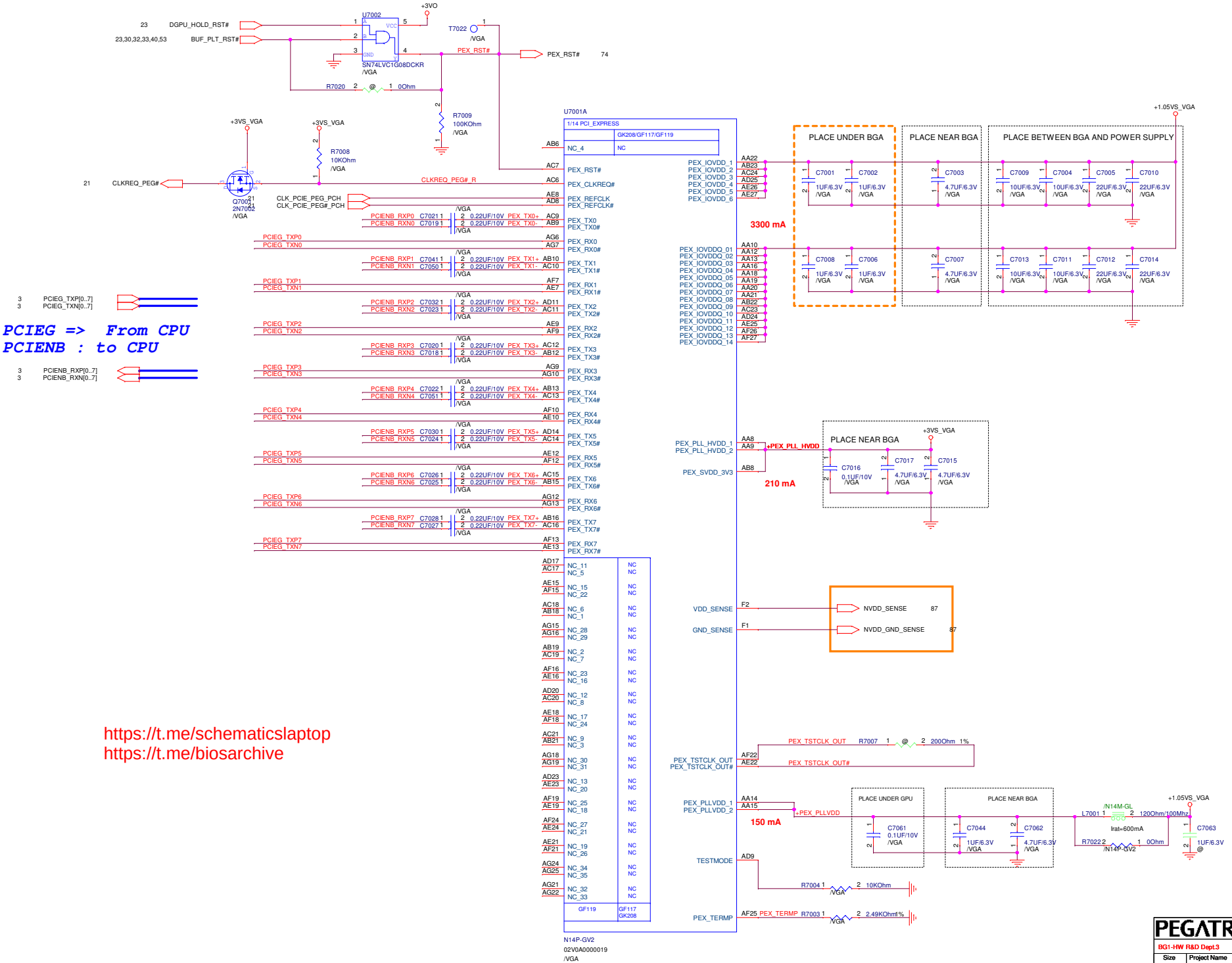
EMI



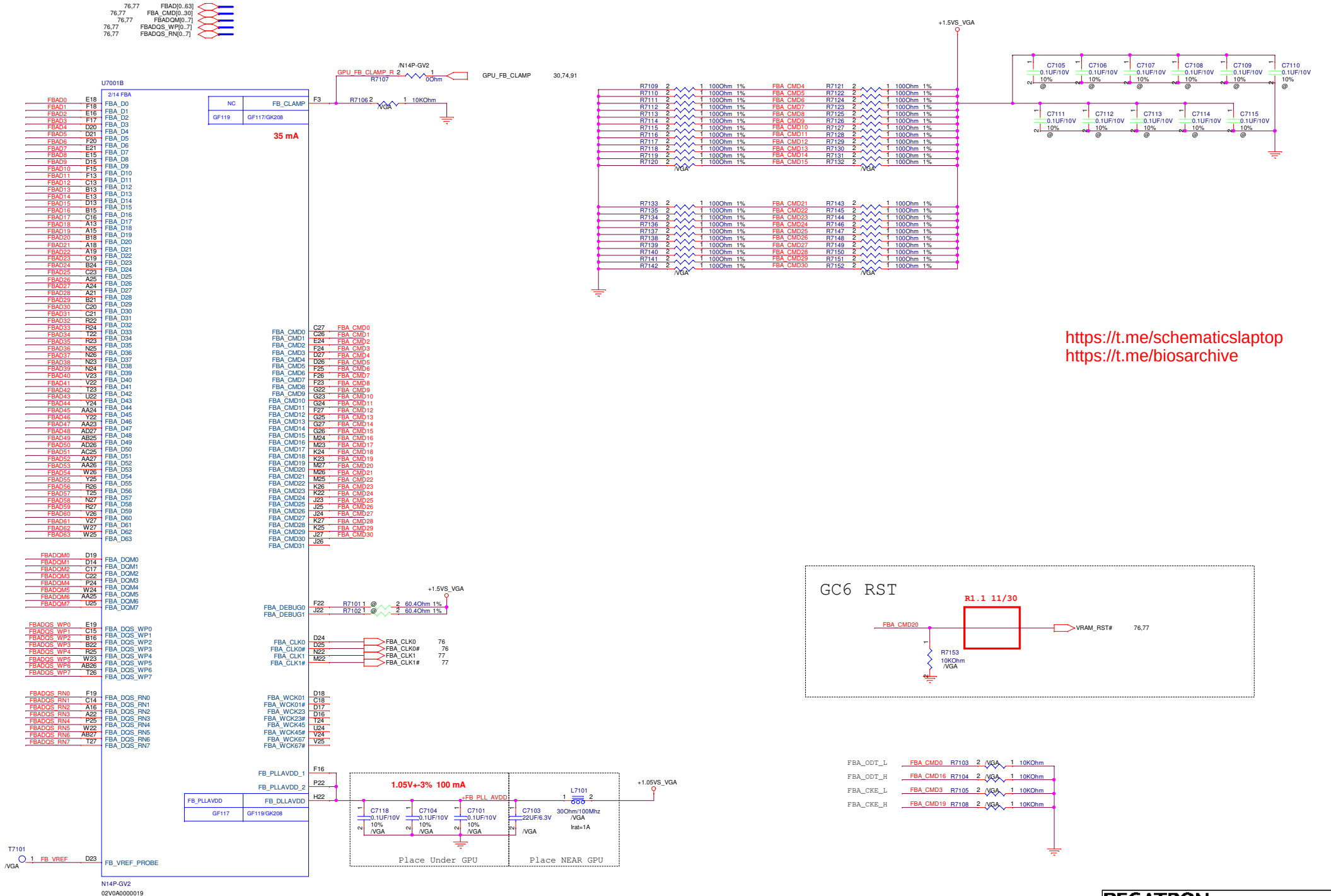
ADAPTOR VOLTAGE DETECTOR.

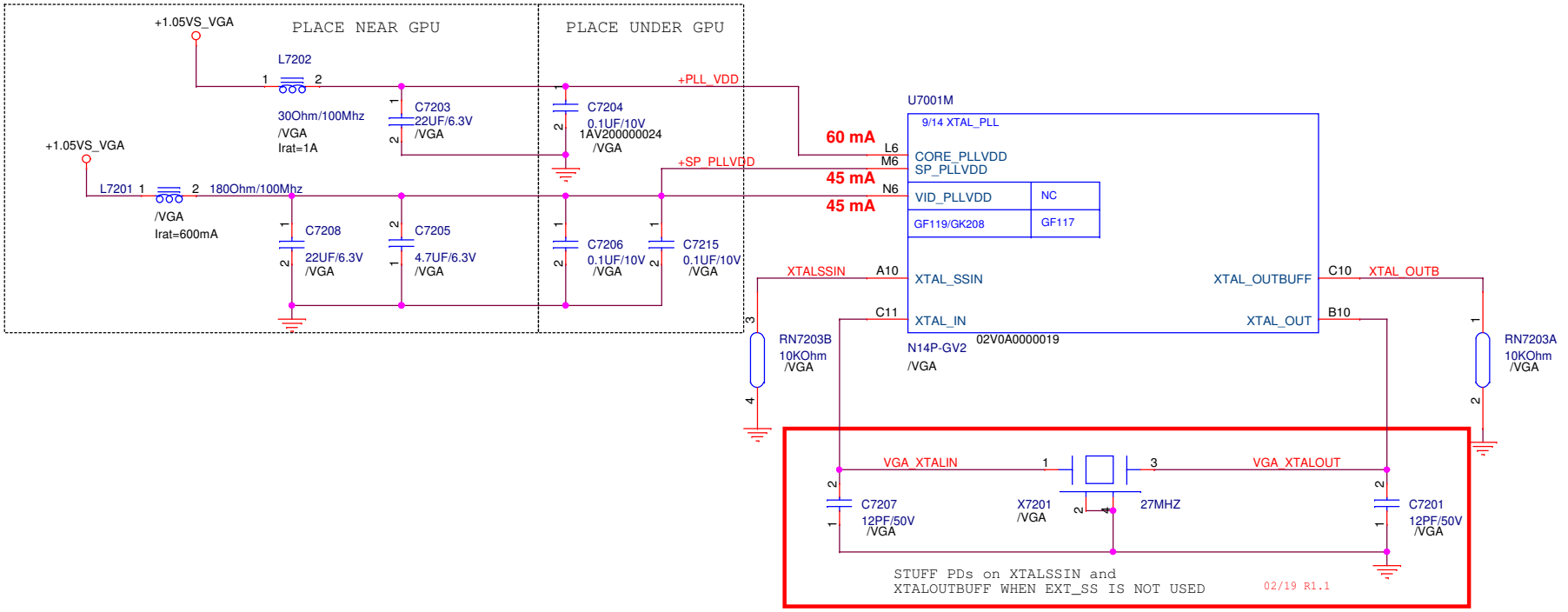


PEGATRON	Title : PEW BRD/IO BRD	
BG1-CSC-HW R&D Dept.5	Engineer: Tina Lee	
Size: B	Project Name: PT10SG	Rev: 1.1
Date: Tuesday, February 26, 2013	Sheet 66 of 104	



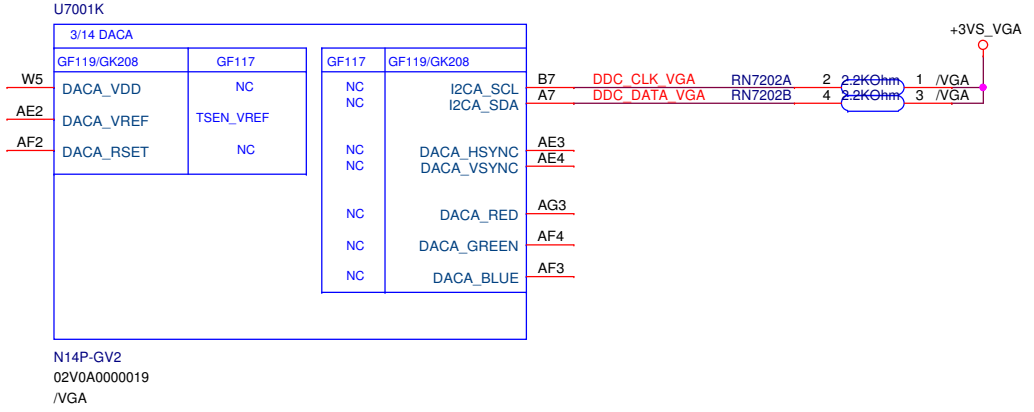
PEGATRON Title : VGA_PCIE
BG1-HW R&D Dept.3 Engineer: Tina_Lee
Size: Custom | Project Name: PT10SG | Rev: 1.1
Date: Tuesday, February 26, 2013 | Sheet 70 of 102


76,77 FBAD[0..63]
76,77 FBA_CMD[0..30]
76,77 FBADQM[0..7]
76,77 FBADQS_WP[0..7]
76,77 FBADQS_RN[0..7]
U7001B
2/14 FBA
NC
FB_CLAMP
GF119
GF117/GK208
35 mA
GPU_FB_CLAMP_R
/N14P-GV2
R7107
0Ohm
GPU_FB_CLAMP
30,74,91
R7106
10KOhm
/VGA
+1.5VS_VGA
C7105 C7106 C7107 C7108 C7109 C7110
C7111 C7112 C7113 C7114 C7115
0.1UF/10V
10%
@
R7109 R7110 R7111 R7112 R7113 R7114 R7115 R7116 R7117 R7118 R7119 R7120
R7121 R7122 R7123 R7124 R7125 R7126 R7127 R7128 R7129 R7130 R7131 R7132
R7133 R7135 R7134 R7136 R7137 R7138 R7139 R7140 R7141 R7142
R7143 R7145 R7144 R7146 R7147 R7148 R7149 R7150 R7151 R7152
100Ohm 1%
FBA_CMD4 FBA_CMD5 FBA_CMD6 FBA_CMD7 FBA_CMD8 FBA_CMD9 FBA_CMD10 FBA_CMD11 FBA_CMD12 FBA_CMD13 FBA_CMD14 FBA_CMD15
FBA_CMD21 FBA_CMD22 FBA_CMD23 FBA_CMD24 FBA_CMD25 FBA_CMD26 FBA_CMD27 FBA_CMD28 FBA_CMD29 FBA_CMD30
FBAD0 FBAD1 FBAD2 FBAD3 FBAD4 FBAD5 FBAD6 FBAD7 FBAD8 FBAD9 FBAD10 FBAD11 FBAD12 FBAD13 FBAD14 FBAD15 FBAD16 FBAD17 FBAD18 FBAD19 FBAD20 FBAD21 FBAD22 FBAD23 FBAD24 FBAD25 FBAD26 FBAD27 FBAD28 FBAD29 FBAD30 FBAD31 FBAD32 FBAD33 FBAD34 FBAD35 FBAD36 FBAD37 FBAD38 FBAD39 FBAD40 FBAD41 FBAD42 FBAD43 FBAD44 FBAD45 FBAD46 FBAD47 FBAD48 FBAD49 FBAD50 FBAD51 FBAD52 FBAD53 FBAD54 FBAD55 FBAD56 FBAD57 FBAD58 FBAD59 FBAD60 FBAD61 FBAD62 FBAD63
E18 F18 E16 F17 D20 D21 F20 E21 E15 D15 F15 F13 C13 B13 E13 D13 B15 C16 A13 A15 B18 A18 A19 C19 B24 C23 A25 A24 A21 B21 C20 C21 R22 R24 T22 R23 N25 N26 N23 N24 V23 V22 T23 U22 Y24 AA24 Y22 AA23 AD27 AB25 AD26 AC25 AA27 AA26 W26 Y25 R26 T25 N27 R27 V26 V27 W27 W25
FBA_D0 FBA_D1 FBA_D2 FBA_D3 FBA_D4 FBA_D5 FBA_D6 FBA_D7 FBA_D8 FBA_D9 FBA_D10 FBA_D11 FBA_D12 FBA_D13 FBA_D14 FBA_D15 FBA_D16 FBA_D17 FBA_D18 FBA_D19 FBA_D20 FBA_D21 FBA_D22 FBA_D23 FBA_D24 FBA_D25 FBA_D26 FBA_D27 FBA_D28 FBA_D29 FBA_D30 FBA_D31 FBA_D32 FBA_D33 FBA_D34 FBA_D35 FBA_D36 FBA_D37 FBA_D38 FBA_D39 FBA_D40 FBA_D41 FBA_D42 FBA_D43 FBA_D44 FBA_D45 FBA_D46 FBA_D47 FBA_D48 FBA_D49 FBA_D50 FBA_D51 FBA_D52 FBA_D53 FBA_D54 FBA_D55 FBA_D56 FBA_D57 FBA_D58 FBA_D59 FBA_D60 FBA_D61 FBA_D62 FBA_D63
FBA_CMD0 FBA_CMD1 FBA_CMD2 FBA_CMD3 FBA_CMD4 FBA_CMD5 FBA_CMD6 FBA_CMD7 FBA_CMD8 FBA_CMD9 FBA_CMD10 FBA_CMD11 FBA_CMD12 FBA_CMD13 FBA_CMD14 FBA_CMD15 FBA_CMD16 FBA_CMD17 FBA_CMD18 FBA_CMD19 FBA_CMD20 FBA_CMD21 FBA_CMD22 FBA_CMD23 FBA_CMD24 FBA_CMD25 FBA_CMD26 FBA_CMD27 FBA_CMD28 FBA_CMD29 FBA_CMD30 FBA_CMD31
C27 C26 E24 F24 D27 D26 F25 F26 F23 G22 G23 G24 F27 G25 G27 G26 M24 M23 K24 K23 M27 M26 M25 K26 K22 J23 J25 J24 K27 K25 J27 J26
FBADQM0 FBADQM1 FBADQM2 FBADQM3 FBADQM4 FBADQM5 FBADQM6 FBADQM7
D19 D14 C17 C22 P24 W24 AA25 U25
FBA_DQM0 FBA_DQM1 FBA_DQM2 FBA_DQM3 FBA_DQM4 FBA_DQM5 FBA_DQM6 FBA_DQM7
FBADQS_WP0 FBADQS_WP1 FBADQS_WP2 FBADQS_WP3 FBADQS_WP4 FBADQS_WP5 FBADQS_WP6 FBADQS_WP7
E19 C15 B16 B22 R25 W23 AB26 T26
FBA_DQS_WP0 FBA_DQS_WP1 FBA_DQS_WP2 FBA_DQS_WP3 FBA_DQS_WP4 FBA_DQS_WP5 FBA_DQS_WP6 FBA_DQS_WP7
FBADQS_RN0 FBADQS_RN1 FBADQS_RN2 FBADQS_RN3 FBADQS_RN4 FBADQS_RN5 FBADQS_RN6 FBADQS_RN7
F19 C14 A16 A22 P25 W22 AB27 T27
FBA_DQS_RN0 FBA_DQS_RN1 FBA_DQS_RN2 FBA_DQS_RN3 FBA_DQS_RN4 FBA_DQS_RN5 FBA_DQS_RN6 FBA_DQS_RN7
FBA_WCK01 FBA_WCK01# FBA_WCK23 FBA_WCK23# FBA_WCK45 FBA_WCK45# FBA_WCK67 FBA_WCK67#
D18 C18 D17 D16 T24 U24 V24 V25
FB_PLLAVDD_1
FB_PLLAVDD_2
F16 P22 H22
FB_PLLAVDD
FB_DLLAVDD
GF117
GF119/GK208
1.05V+-3% 100 mA
+FB_PLL_AVDD
C7118 C7104 C7101 C7103
0.1UF/10V
22UF/6.3V
10%
/VGA
L7101
300hm/100Mhz
Irat=1A
+1.05VS_VGA
Place Under GPU
Place NEAR GPU
T7101
FB_VREF
D23
FB_VREF_PROBE
/VGA
N14P-GV2
02V0A0000019
/VGA
FBA_DEBUG0 FBA_DEBUG1
F22 J22
R7101 R7102
60.4Ohm 1%
FBA_CLK0 FBA_CLK0# FBA_CLK1 FBA_CLK1#
D24 D25 N22 M22
76 76 77 77
GC6 RST
R1.1 11/30
FBA_CMD20
VRAM_RST#
76,77
R7153
10KOhm
/VGA
FBA_ODT_L FBA_ODT_H FBA_CKE_L FBA_CKE_H
FBA_CMD0 FBA_CMD16 FBA_CMD3 FBA_CMD19
R7103 R7104 R7105 R7108
https://t.me/schematicslaptop
https://t.me/biosarchive
PEGATRON
Title : VGA_FRAME BUFFER
BG1-HW R&D Dept.3
Engineer: Tina_Lee
Size Custom
Project Name PT10SG
Rev 1.1
Date: Tuesday, February 26, 2013
Sheet 71 of 102



UNconnected
Leave DACA_VDD floating
DACA_VREF,DACA_RSET,IO floating

120 mA



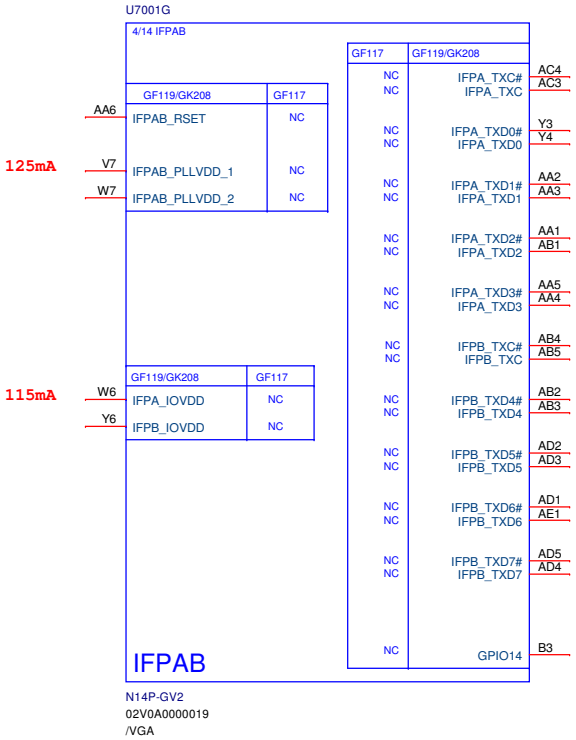
PEGATRON Title :VGA_RGB.XTAL

BG1-HW R&D Dept.3 Engineer: Tina_Lee

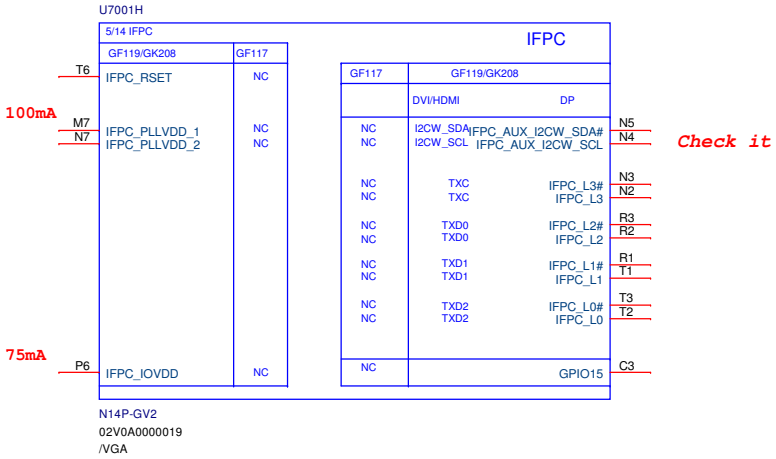
Size	Project Name	Rev
Custom	PT10SG	1.1

Date: Tuesday, February 26, 2013 Sheet 72 of 102

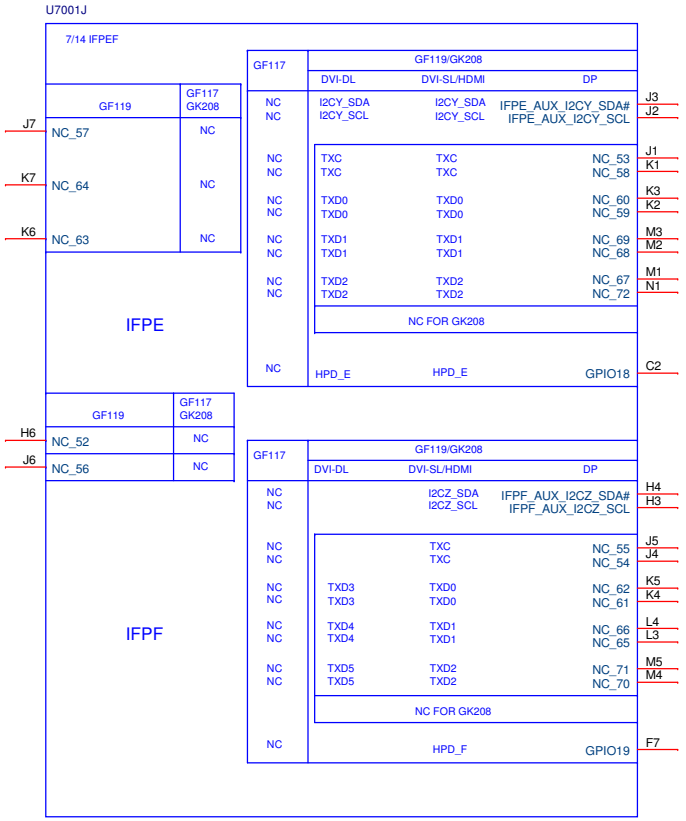
LVDS

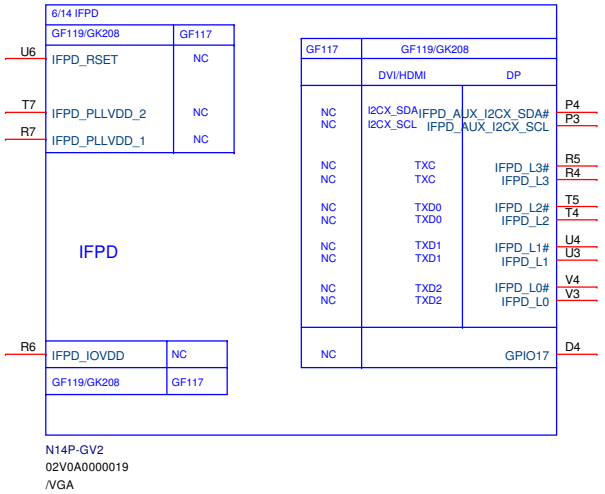


HDMI



Check it



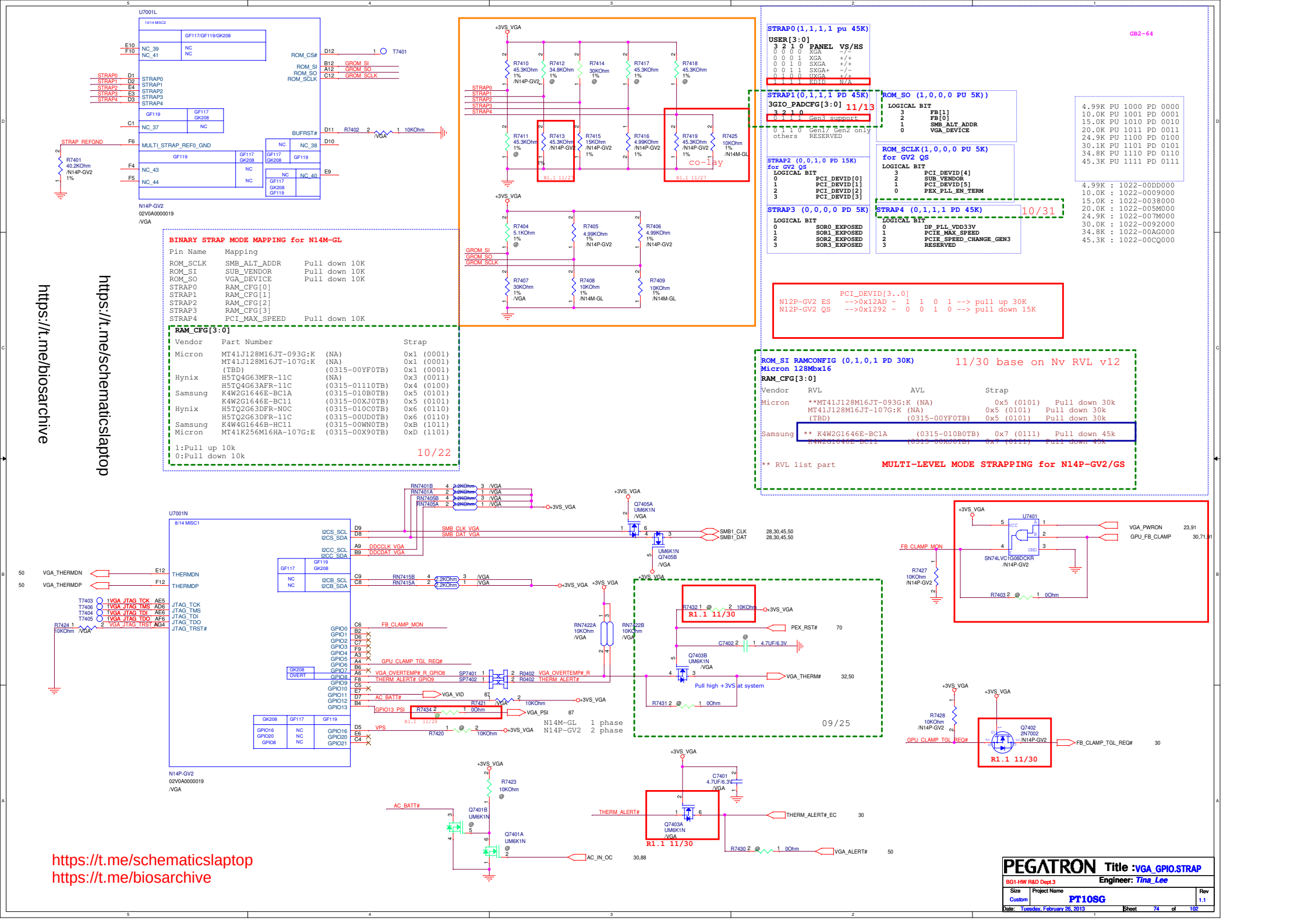


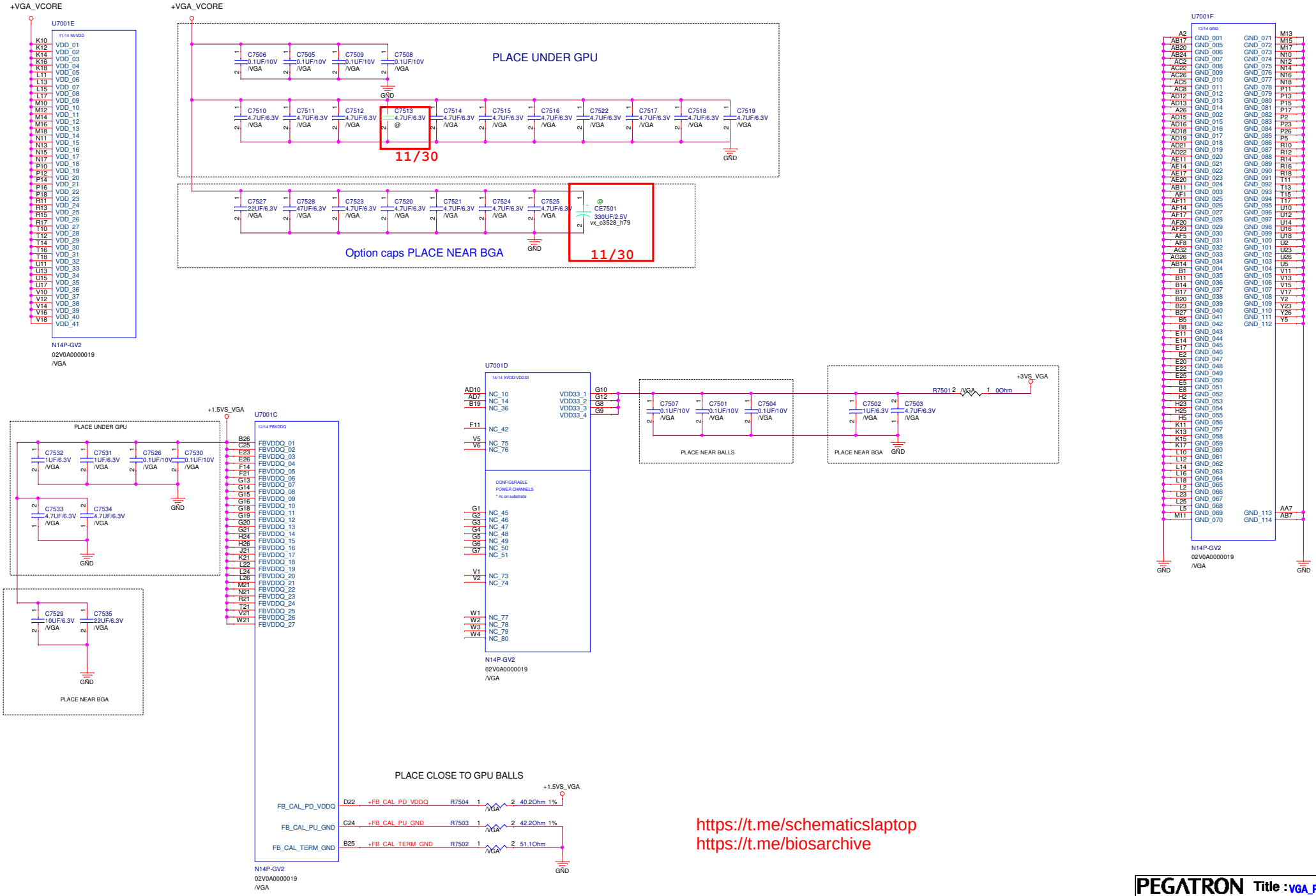
PEGATRON Title : VGA_LVDS.HDMI

BG1-CSC-HW R&D Dept.5 Engineer: Tina_Lee

Size	Project Name	Rev
Custom	PT10SG	1.1

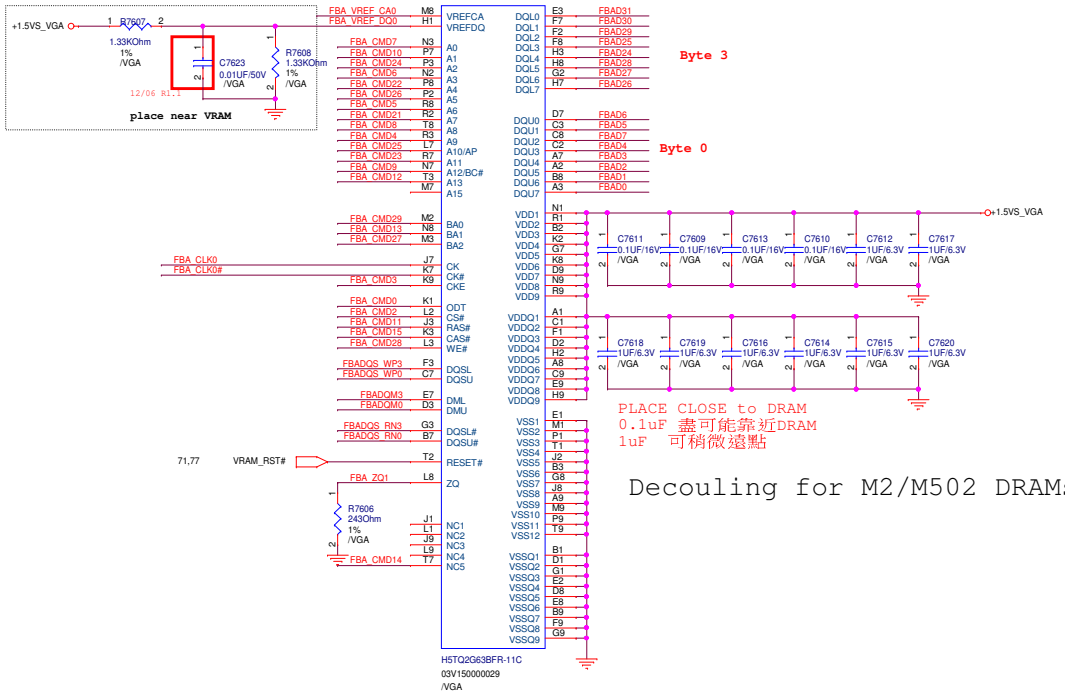
Date: Tuesday, February 26, 2013 Sheet 73 of 102


U7001L
N14P-GV2
02V0A0000019
/VGA
STRAP_REFGND
R7401 40.2KOhm /N14P-GV2 1%
ROM_CS#
ROM_SI
ROM_SO
ROM_SCLK
BUFRST#
MULTI_STRAP_REF0_GND
STRAP0
STRAP1
STRAP2
STRAP3
STRAP4
GROM_SI
GROM_SO
GROM_SCLK
R7410 45.3KOhm 1% /N14P-GV2
R7412 34.8KOhm 1% @
R7414 30KOhm 1% @
R7417 45.3KOhm 1% @
R7418 45.3KOhm 1% @
R7411 45.3KOhm 1% @
R7413 45.3KOhm /N14P-GV2 1%
R7415 15KOhm /N14P-GV2 1%
R7416 4.99KOhm /N14P-GV2 1%
R7419 45.3KOhm /N14P-GV2 1%
R7425 10KOhm 1% /N14M-GL
R1.1 11/27
co-lay
R7404 5.1KOhm 1% @
R7405 4.99KOhm 1% /N14P-GV2
R7406 4.99KOhm 1% /N14P-GV2
R7407 30KOhm 1% /VGA
R7408 10KOhm 1% /N14M-GL
R7409 10KOhm 1% /N14M-GL
STRAP0(1,1,1,1 pu 45K)
USER[3:0]
3 2 1 0 PANEL VS/HS
0 0 0 0 XGA -/-
0 0 0 1 XGA +/+
0 0 1 0 SXGA +/+
0 0 1 1 SXGA+ -/-
0 1 0 0 UXGA +/+
1 1 1 1 EDID N/A
STRAP1(0,1,1,1 PD 45K)
3GIO_PADCFG[3:0] 11/13
3 2 1 0
0 1 1 1 Gen3 support
0 1 1 0 Gen1/ Gen2 only
others RESERVED
STRAP2 (0,0,1,0 PD 15K)
for GV2 QS
LOGICAL BIT
0 PCI_DEVID[0]
1 PCI_DEVID[1]
2 PCI_DEVID[2]
3 PCI_DEVID[3]
STRAP3 (0,0,0,0 PD 5K)
LOGICAL BIT
0 SOR0_EXPOSED
1 SOR1_EXPOSED
2 SOR2_EXPOSED
3 SOR3_EXPOSED
ROM_SO (1,0,0,0 PU 5K))
LOGICAL BIT
3 FB[1]
2 FB[0]
1 SMB_ALT_ADDR
0 VGA_DEVICE
ROM_SCLK(1,0,0,0 PU 5K)
for GV2 QS
LOGICAL BIT
3 PCI_DEVID[4]
2 SUB_VENDOR
1 PCI_DEVID[5]
0 PEX_PLL_EN_TERM
STRAP4 (0,1,1,1 PD 45K) 10/31
LOGICAL BIT
0 DP_PLL_VDD33V
1 PCIE_MAX_SPEED
2 PCIE_SPEED_CHANGE_GEN3
3 RESERVED
GB2-64
4.99K PU 1000 PD 0000
10.0K PU 1001 PD 0001
15.0K PU 1010 PD 0010
20.0K PU 1011 PD 0011
24.9K PU 1100 PD 0100
30.1K PU 1101 PD 0101
34.8K PU 1110 PD 0110
45.3K PU 1111 PD 0111
4.99K : 1022-00DD000
10.0K : 1022-0009000
15.0K : 1022-0038000
20.0K : 1022-005M000
24.9K : 1022-007M000
30.0K : 1022-0092000
34.8K : 1022-00AG000
45.3K : 1022-00CQ000
PCI_DEVID[3..0]
N12P-GV2 ES -->0x12AD ~ 1 1 0 1 --> pull up 30K
N12P-GV2 QS -->0x1292 ~ 0 0 1 0 --> pull down 15K
BINARY STRAP MODE MAPPING for N14M-GL
Pin Name Mapping
ROM_SCLK SMB_ALT_ADDR Pull down 10K
ROM_SI SUB_VENDOR Pull down 10K
ROM_SO VGA_DEVICE Pull down 10K
STRAP0 RAM_CFG[0]
STRAP1 RAM_CFG[1]
STRAP2 RAM_CFG[2]
STRAP3 RAM_CFG[3]
STRAP4 PCI_MAX_SPEED Pull down 10K
RAM_CFG[3:0]
Vendor Part Number Strap
Micron MT41J128M16JT-093G:K (NA) 0x1 (0001)
MT41J128M16JT-107G:K (NA) 0x1 (0001)
(TBD) (0315-00YF0TB) 0x1 (0001)
Hynix H5TQ4G63MFR-11C (NA) 0x3 (0011)
H5TQ4G63AFR-11C (0315-01110TB) 0x4 (0100)
Samsung K4W2G1646E-BC1A (0315-010B0TB) 0x5 (0101)
K4W2G1646E-BC11 (0315-00XJ0TB) 0x5 (0101)
Hynix H5TQ2G63DFR-N0C (0315-010C0TB) 0x6 (0110)
H5TQ2G63DFR-11C (0315-00UD0TB) 0x6 (0110)
Samsung K4W4G1646B-HC11 (0315-00WN0TB) 0xB (1011)
Micron MT41K256M16HA-107G:E (0315-00X90TB) 0xD (1101)
1:Pull up 10k
0:Pull down 10k
10/22
ROM_SI RAMCONFIG (0,1,0,1 PD 30K)
Micron 128Mbx16
11/30 base on Nv RVL v12
RAM_CFG[3:0]
Vendor RVL AVL Strap
Micron **MT41J128M16JT-093G:K (NA) 0x5 (0101) Pull down 30k
MT41J128M16JT-107G:K (NA) 0x5 (0101) Pull down 30k
(TBD) (0315-00YF0TB) 0x5 (0101) Pull down 30k
Samsung ** K4W2G1646E-BC1A (0315-010B0TB) 0x7 (0111) Pull down 45k
** RVL list part
MULTI-LEVEL MODE STRAPPING for N14P-GV2/GS
U7001N
8/14 MISC1
N14P-GV2
02V0A0000019
/VGA
THERMDN
THERMDP
VGA_THERMDN
VGA_THERMDP
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST#
I2CS_SCL
I2CS_SDA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
SMB_CLK_VGA
SMB_DAT_VGA
DDCCLK_VGA
DDCDAT_VGA
RN7401B 2.2KOhm /VGA
RN7401A 2.2KOhm /VGA
RN7405B 2.2KOhm /VGA
RN7405A 2.2KOhm /VGA
RN7415B 2.2KOhm /VGA
RN7415A 2.2KOhm /VGA
Q7405A UM6K1N /VGA
Q7405B UM6K1N /VGA
SMB1_CLK
SMB1_DAT
FB_CLAMP_MON
GPU_CLAMP_TGL_REQ#
VGA_OVERTEMP#_R_GPIO8
THERM_ALERT#_GPIO9
R0402_VGA_OVERTEMP#_R
R0402_THERM_ALERT#
SP7401
SP7402
AC_BATT#
VGA_VID
VGA_PSI
GPIO13_PSI
VPS
RN7422A 10KOhm /VGA
RN7422B 10KOhm /VGA
R7432 10KOhm
R1.1 11/30
PEX_RST#
C7402 4.7UF/6.3V
Q7403B UM6K1N /VGA
VGA_THERM#
Pull high +3VS at system
R7431 0Ohm
R7434 0Ohm
R1.1 11/29
R7421 10KOhm /VGA
R7420 10KOhm
N14M-GL 1 phase
N14P-GV2 2 phase
09/25
U7401
SN74LVC1G08DCKR /N14P-GV2
VGA_PWRON
GPU_FB_CLAMP
R7427 10KOhm /N14P-GV2
R7403 0Ohm
R7428 10KOhm /N14P-GV2
Q7402 2N7002 /N14P-GV2
FB_CLAMP_TGL_REQ#
R1.1 11/30
R7423 10KOhm
Q7401B UM6K1N
Q7401A UM6K1N
AC_IN_OC
C7401 4.7UF/6.3V /VGA
Q7403A UM6K1N /VGA
THERM_ALERT#_EC
VGA_ALERT#
R7430 0Ohm
PEGATRON
Title :VGA_GPIO.STRAP
BG1-HW R&D Dept.3
Engineer: Tina_Lee
Size Custom
Project Name PT10SG
Rev 1.1
Date: Tuesday, February 26, 2013
Sheet 74 of 102
https://t.me/biosarchive
https://t.me/schematicslaptop
https://t.me/schematicslaptop
https://t.me/biosarchive


+VGA_VCORE
U7001E
11/14 NVVDD
K10 K12 K14 K16 K18 L11 L13 L15 L17 M10 M12 M14 M16 M18 N11 N13 N15 N17 P10 P12 P14 P16 P18 R11 R13 R15 R17 T10 T12 T14 T16 T18 U11 U13 U15 U17 V10 V12 V14 V16 V18
VDD_01 VDD_02 VDD_03 VDD_04 VDD_05 VDD_06 VDD_07 VDD_08 VDD_09 VDD_10 VDD_11 VDD_12 VDD_13 VDD_14 VDD_15 VDD_16 VDD_17 VDD_18 VDD_19 VDD_20 VDD_21 VDD_22 VDD_23 VDD_24 VDD_25 VDD_26 VDD_27 VDD_28 VDD_29 VDD_30 VDD_31 VDD_32 VDD_33 VDD_34 VDD_35 VDD_36 VDD_37 VDD_38 VDD_39 VDD_40 VDD_41
N14P-GV2
02V0A0000019
/VGA
+VGA_VCORE
PLACE UNDER GPU
C7506 C7505 C7509 C7508 0.1UF/10V /VGA
C7510 C7511 C7512 C7513 C7514 C7515 C7516 C7522 C7517 C7518 C7519 4.7UF/6.3V /VGA
C7513 @
11/30
GND
C7527 C7528 C7523 C7520 C7521 C7524 C7525 22UF/6.3V 47UF/6.3V 4.7UF/6.3V /VGA
@ CE7501 330UF/2.5V vx_c3528_h79
Option caps PLACE NEAR BGA
11/30
U7001F
13/14 GND
A2 AB17 AB20 AB24 AC2 AC22 AC26 AC5 AC8 AD12 AD13 A26 AD15 AD16 AD18 AD19 AD21 AD22 AE11 AE14 AE17 AE20 AB11 AF1 AF11 AF14 AF17 AF20 AF23 AF5 AF8 AG2 AG26 AB14 B1 B11 B14 B17 B20 B23 B27 B5 B8 E11 E14 E17 E2 E20 E22 E25 E5 E8 H2 H23 H25 H5 K11 K13 K15 K17 L10 L12 L14 L16 L18 L2 L23 L25 L5 M11
GND_001 GND_005 GND_006 GND_007 GND_008 GND_009 GND_010 GND_011 GND_012 GND_013 GND_014 GND_002 GND_015 GND_016 GND_017 GND_018 GND_019 GND_020 GND_021 GND_022 GND_023 GND_024 GND_003 GND_025 GND_026 GND_027 GND_028 GND_029 GND_030 GND_031 GND_032 GND_033 GND_034 GND_004 GND_035 GND_036 GND_037 GND_038 GND_039 GND_040 GND_041 GND_042 GND_043 GND_044 GND_045 GND_046 GND_047 GND_048 GND_049 GND_050 GND_051 GND_052 GND_053 GND_054 GND_055 GND_056 GND_057 GND_058 GND_059 GND_060 GND_061 GND_062 GND_063 GND_064 GND_065 GND_066 GND_067 GND_068 GND_069 GND_070
M13 M15 M17 N10 N12 N14 N16 N18 P11 P13 P15 P17 P2 P23 P26 P5 R10 R12 R14 R16 R18 T11 T13 T15 T17 U10 U12 U14 U16 U18 U2 U23 U26 U5 V11 V13 V15 V17 Y2 Y23 Y26 Y5 AA7 AB7
GND_071 GND_072 GND_073 GND_074 GND_075 GND_076 GND_077 GND_078 GND_079 GND_080 GND_081 GND_082 GND_083 GND_084 GND_085 GND_086 GND_087 GND_088 GND_089 GND_090 GND_091 GND_092 GND_093 GND_094 GND_095 GND_096 GND_097 GND_098 GND_099 GND_100 GND_101 GND_102 GND_103 GND_104 GND_105 GND_106 GND_107 GND_108 GND_109 GND_110 GND_111 GND_112 GND_113 GND_114
N14P-GV2
02V0A0000019
/VGA
U7001D
14/14 XVDD/VDD33
AD10 AD7 B19 F11 V5 V6
NC_10 NC_14 NC_36 NC_42 NC_75 NC_76
VDD33_1 VDD33_2 VDD33_3 VDD33_4
G10 G12 G8 G9
CONFIGURABLE POWER CHANNELS
* nc on subbinate
G1 G2 G3 G4 G5 G6 G7 V1 V2 W1 W2 W3 W4
NC_45 NC_46 NC_47 NC_48 NC_49 NC_50 NC_51 NC_73 NC_74 NC_77 NC_78 NC_79 NC_80
N14P-GV2
02V0A0000019
/VGA
C7507 C7501 C7504 0.1UF/10V /VGA
PLACE NEAR BALLS
C7502 1UF/6.3V /VGA
C7503 4.7UF/6.3V /VGA
PLACE NEAR BGA
+3VS_VGA
R7501 2 /VGA 1 0Ohm
GND
+1.5VS_VGA
U7001C
12/14 FBVDDQ
PLACE UNDER GPU
C7532 C7531 C7526 C7530 1UF/6.3V 0.1UF/10V /VGA
C7533 C7534 4.7UF/6.3V /VGA
C7529 10UF/6.3V /VGA
C7535 22UF/6.3V /VGA
PLACE NEAR BGA
B26 C25 E23 E26 F14 F21 G13 G14 G15 G16 G18 G19 G20 G21 H24 H26 J21 K21 L22 L24 L26 M21 N21 R21 T21 V21 W21
FBVDDQ_01 FBVDDQ_02 FBVDDQ_03 FBVDDQ_04 FBVDDQ_05 FBVDDQ_06 FBVDDQ_07 FBVDDQ_08 FBVDDQ_09 FBVDDQ_10 FBVDDQ_11 FBVDDQ_12 FBVDDQ_13 FBVDDQ_14 FBVDDQ_15 FBVDDQ_16 FBVDDQ_17 FBVDDQ_18 FBVDDQ_19 FBVDDQ_20 FBVDDQ_21 FBVDDQ_22 FBVDDQ_23 FBVDDQ_24 FBVDDQ_25 FBVDDQ_26 FBVDDQ_27
N14P-GV2
02V0A0000019
/VGA
PLACE CLOSE TO GPU BALLS
+1.5VS_VGA
FB_CAL_PD_VDDQ D22 +FB_CAL_PD_VDDQ R7504 1 /VGA 2 40.2Ohm 1%
FB_CAL_PU_GND C24 +FB_CAL_PU_GND R7503 1 /VGA 2 42.2Ohm 1%
FB_CAL_TERM_GND B25 +FB_CAL_TERM_GND R7502 1 /VGA 2 51.1Ohm
https://t.me/schematicslaptop
https://t.me/biosarchive
PEGATRON
Title : VGA_Power.GND
BG1-HW R&D Dept.3
Engineer: Tina_Lee
Size Custom
Project Name PT10SG
Rev 1.1
Date: Tuesday, February 26, 2013
Sheet 75 of 102

FBA Patyition 31..0 RANK 0

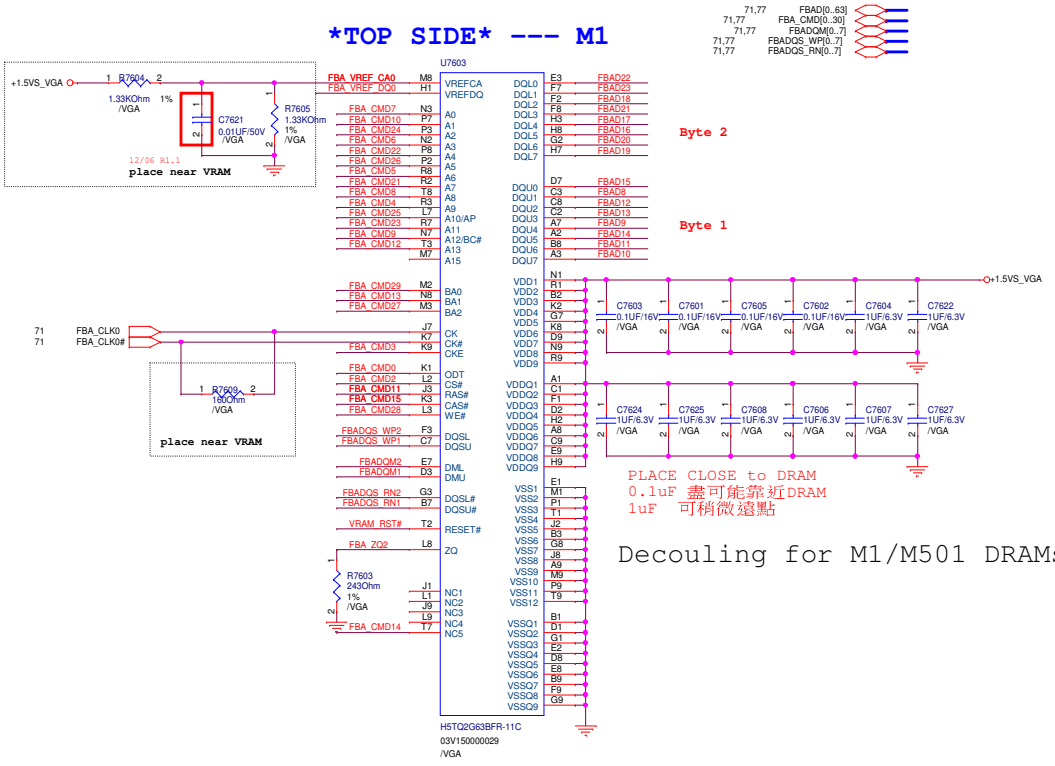
TOP SIDE --- M2



PLACE CLOSE to DRAM
0.1uF 盡可能靠近DRAM
1uF 可稍微遠點

Decouling for M2/M502 DRAMs

TOP SIDE --- M1

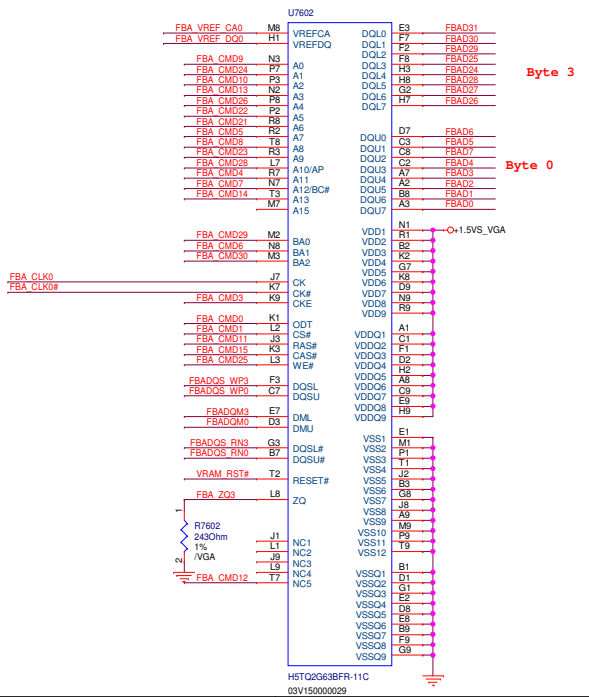


PLACE CLOSE to DRAM
0.1uF 盡可能靠近DRAM
1uF 可稍微遠點

Decouling for M1/M501 DRAMs

FBA Patyition 31..0 RANK 1

BOT SIDE --- M502



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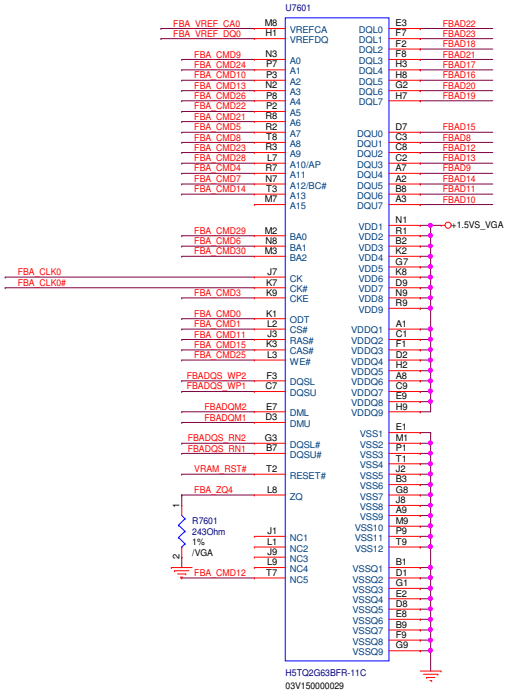
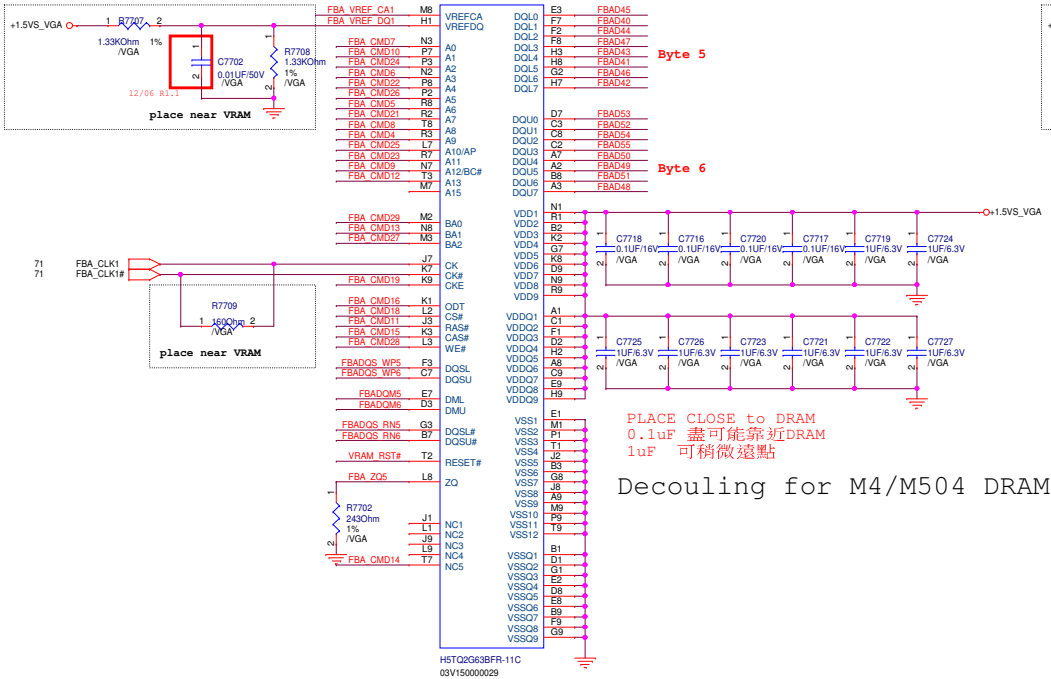
BOT SIDE --- M501



PEGATRON	Title : VGA_VRAM[31:0]	
BG1-HW R&D Dept.3	Engineer: Tina_Lee	
Size: Custom	Project Name: PT10SG	Rev: 1.1
Date: Tuesday, February 26, 2013	Sheet 76 of 102	

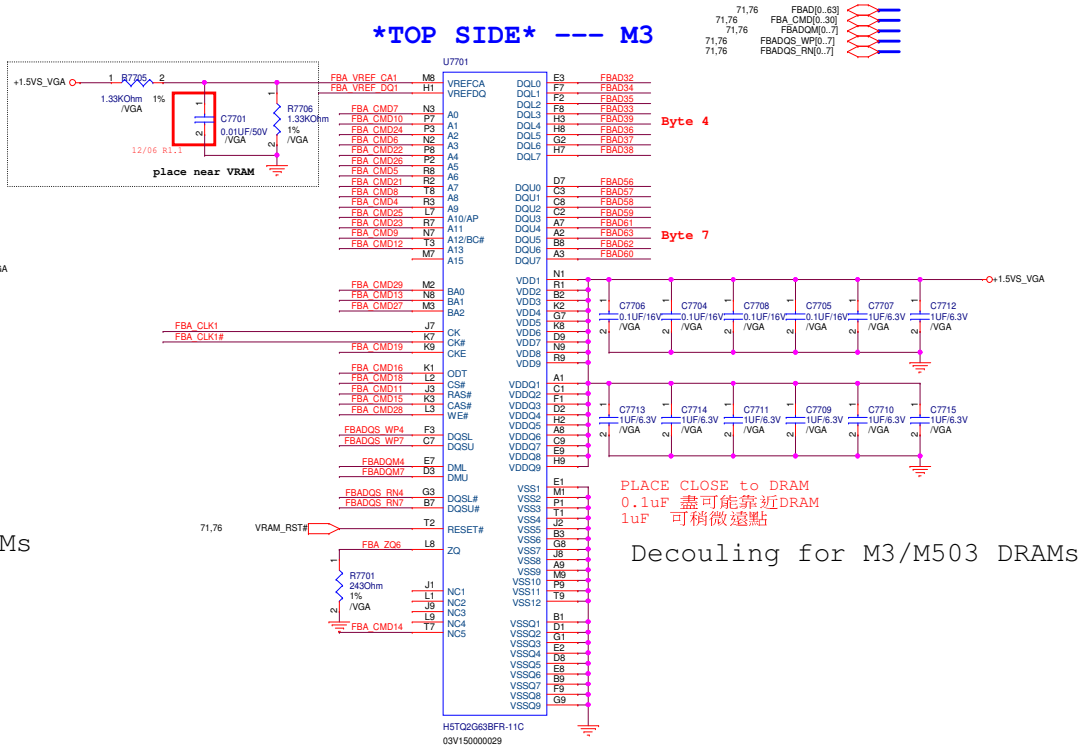
FBA Patyition 63..32 RANK 0

TOP SIDE --- M4



Decouling for M4/M504 DRAMs

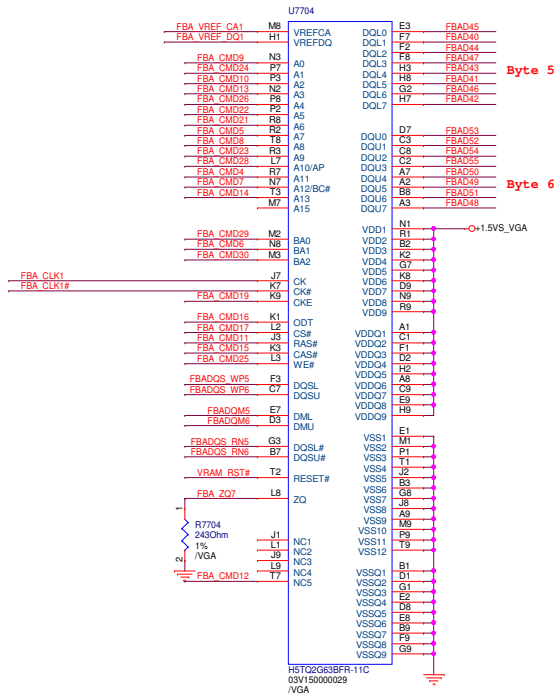
TOP SIDE --- M3



Decouling for M3/M503 DRAMs

FBA Patyition 63..32 RANK 1

BOT SIDE --- M504



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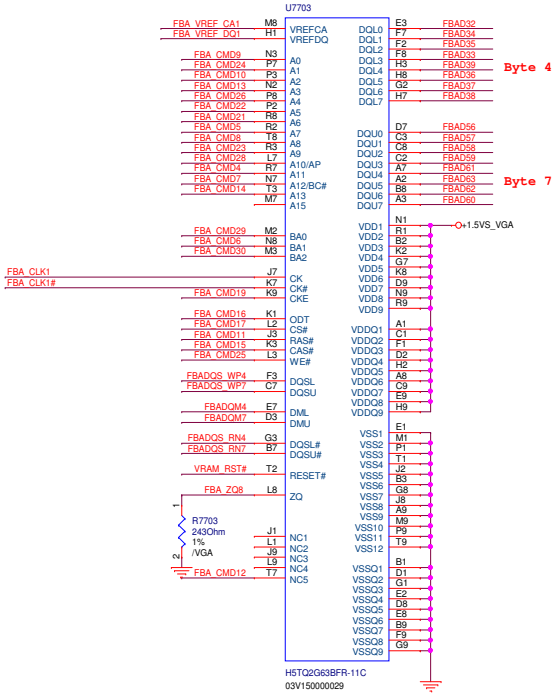
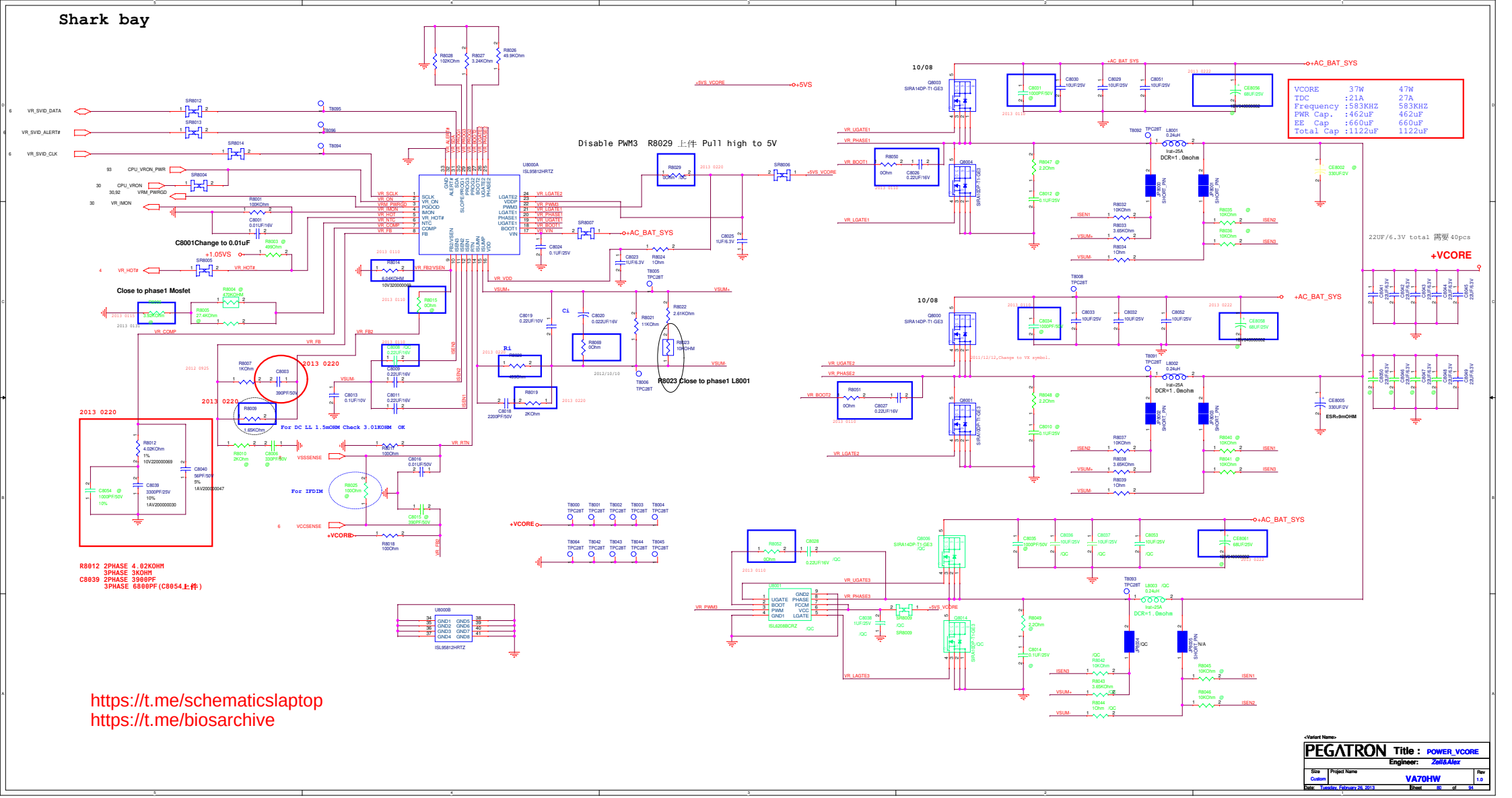
BOT SIDE --- M503



PEGATRON	Title : VGA_VRAM[63:32]		
BG1-HW R&D Dept.3	Engineer: Tina_Lee		
Size: Custom	Project Name: PT10SG		Rev: 1.1
Date: Tuesday, February 26, 2013	Sheet 77 of 102		

Shark bay



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https://t.me/biosarchive

<Variant Name>

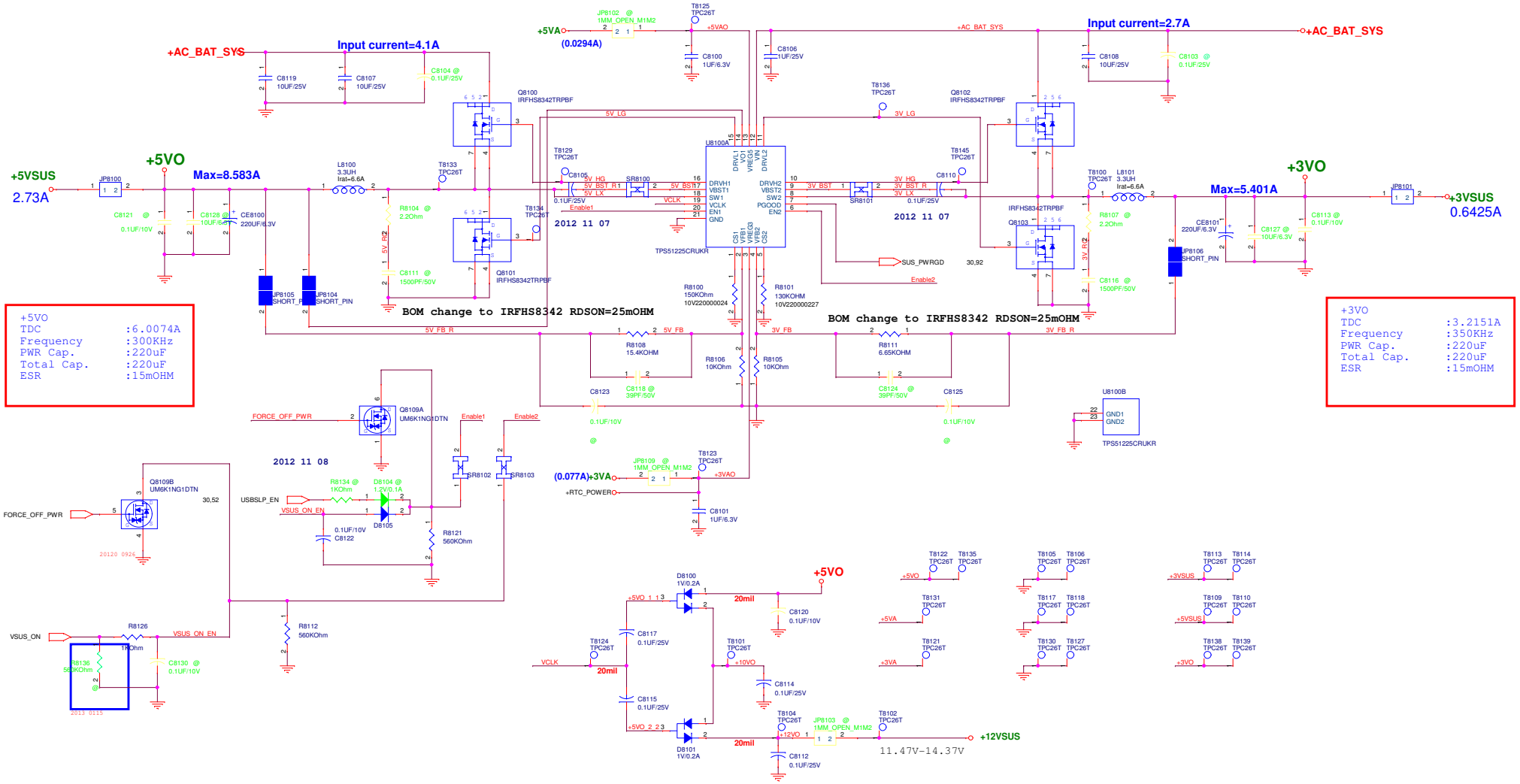
PEGATRON Title : POWER_VCORE

Engineer: Zell&Alex

Size	Project Name	Rev
Custom	VA70HW	1.0

Date: Tuesday, February 26, 2013 Sheet 80 of 94

+5VO & +3VO POWER SUPPLY



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https://t.me/biosarchive

<Variant Name>

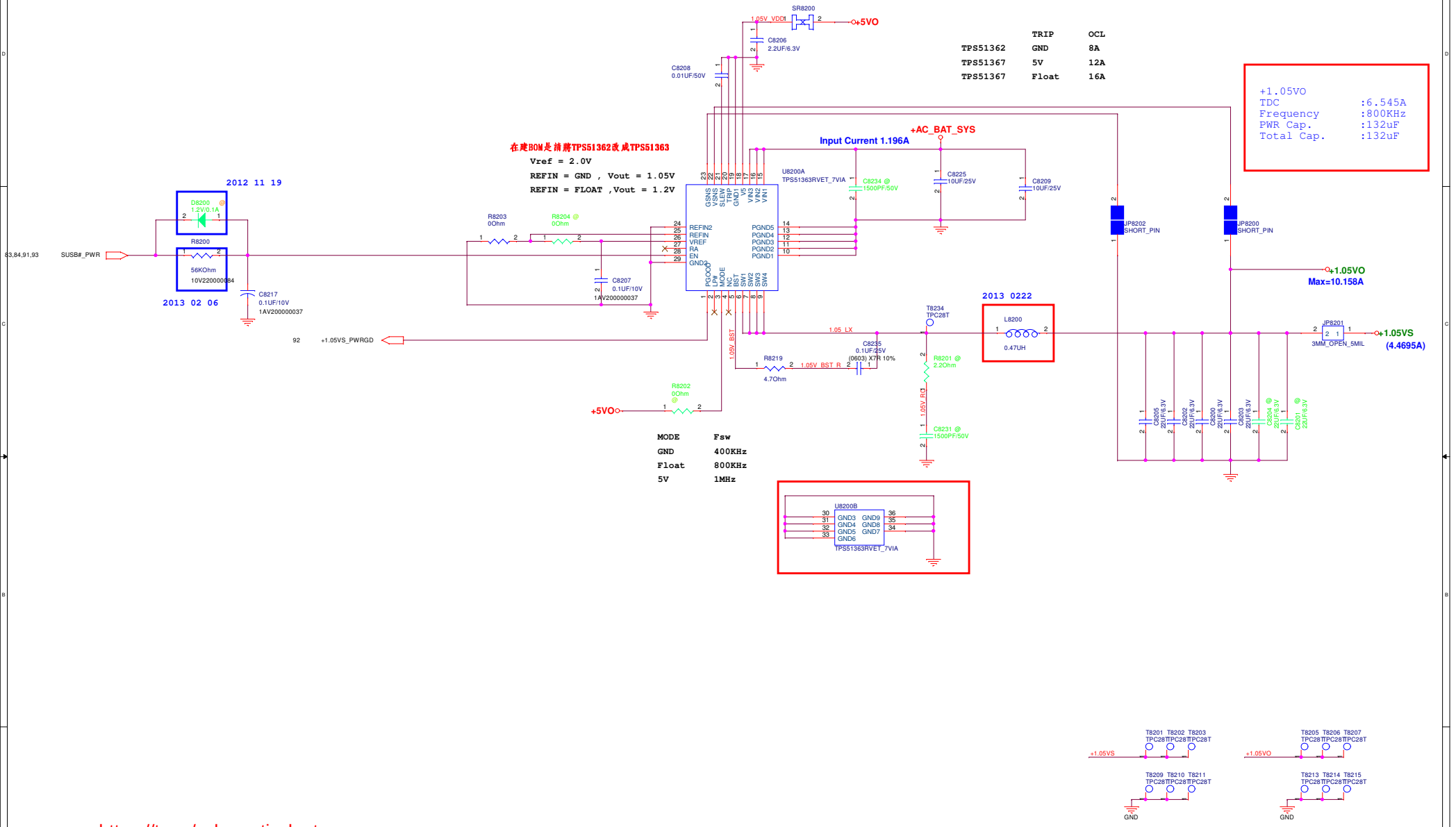
PEGATRON Title : POWER_SYSTEM

Engineer: Adams Lin

Size	Project Name	Rev
Custom	TOD'S	1.0

Date: Tuesday, February 26, 2013 Sheet 81 of 99

+1.05VS POWER SUPPLY



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https://t.me/biosarchive

<Variant Name>

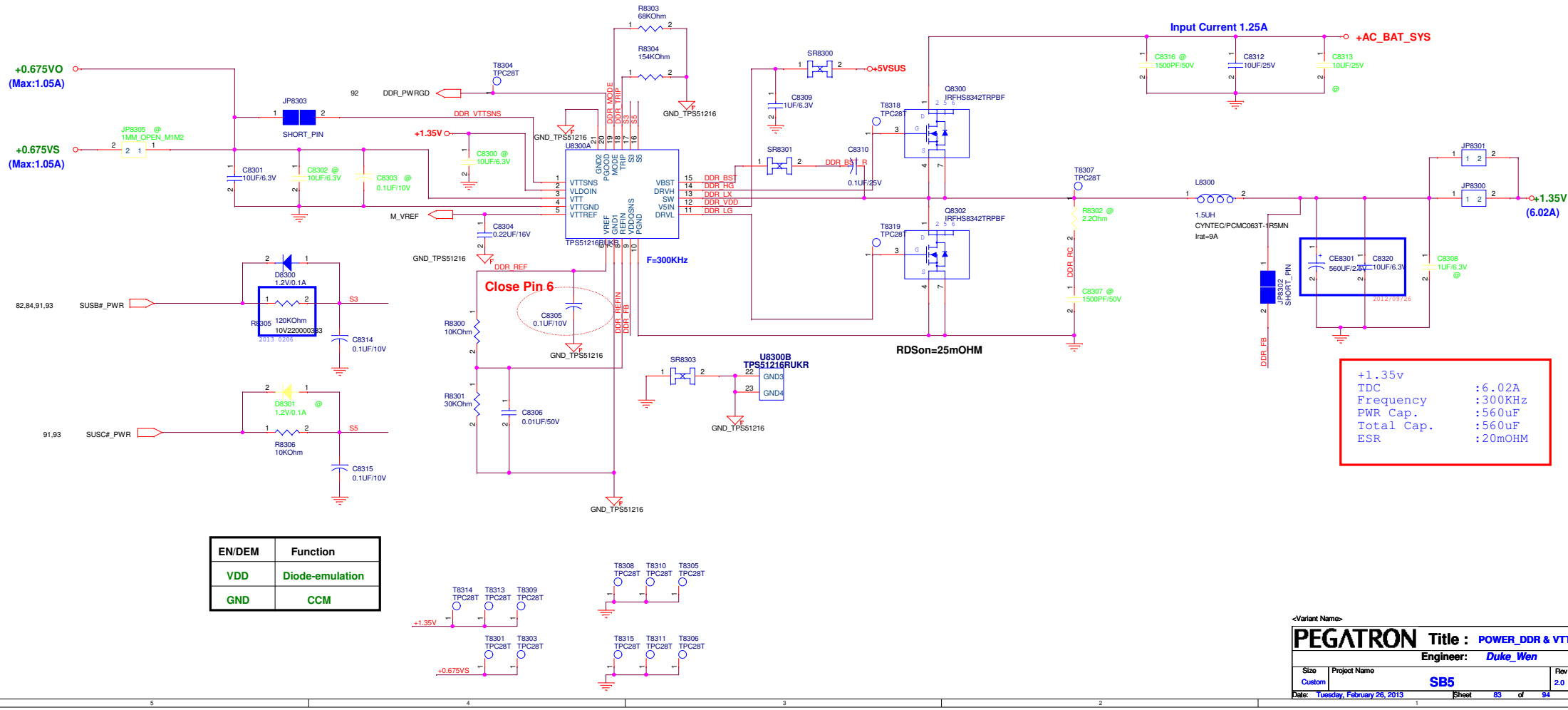
PEGATRON Title : POWER_+1.05VS

Engineer: Duke_Wen

Size	Project Name	Rev
Custom	SB5	1.1

Date: Tuesday, February 26, 2013 Sheet 82 of 94

DDR & VTT POWER SUPPLY



EN/DEM	Function
VDD	Diode-emulation
GND	CCM

<Variant Name>

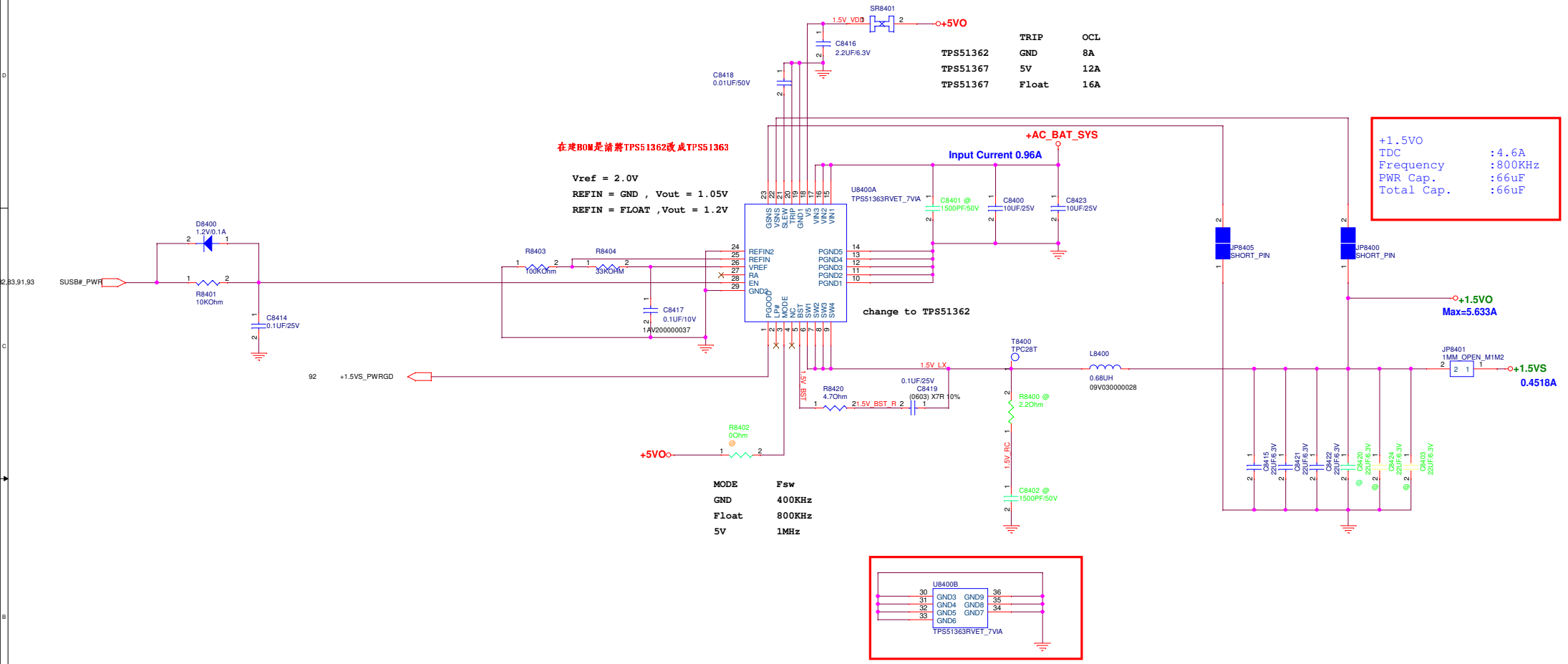
PEGATRON Title : POWER_DDR & VTT

Engineer: Duke_Wen

Size	Project Name	Rev
Custom	SB5	2.0

Date: Tuesday, February 26, 2013 Sheet 83 of 94

1.5VS POWER SUPPLY



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<Variant Name>

PEGATRON Title : POWER_1.5VS

Engineer: Kevin_Chang

Size	Project Name	Rev
Custom	BA50	1.0

Date: Tuesday, February 26, 2013 Sheet 84 of 94

<Variant Name>

PEGATRON Title : POWER_N/A

Engineer:

Size	Project Name	Rev
Custom		1.1

Date: Tuesday, February 26, 2013 Sheet 86 of 94

VGA_CORE POWER SUPPLY

	N14M-GL	N14P-GV2
R8723	39K	20K
R8721	30K	20K
R8716	3K	2K
R8713	27K	18K
C8720	2.2nF	2.7nF
R8727	22K	20K
Vmin	0.65V	0.6V
Vmax	1.15V	1.2V
Vboot	0.9V	0.9V
L8701	0.47uH	0.36uH
L8702	0.47uH	0.36uH
Q8701	SIRA14	SIRA10
Q8704	SIRA14	SIRA10
optional naming	/N14M-GL	/N14P-GV2

VGA_PSI#	VO_action
~ 0.8V	1 Phase DEM
1.2 ~ 1.8V	1 Phase FCCM
2.4V ~	2 Phase FCCM

1 PHASE	2 PHASE	2 PHASE
N14M-GL	N14P-GV2	N14P-GS
EDP=24.33A	EDP=33A	EDP=36A
TDC=17.72A	TDC=28A	TDC=28A
OCP:40A	OCP:70A	OCP:70A

+VGA_VCORE (2 Phase)
TDC :28A
Frequency :305KHz
PWR Cap. :940uF
EE Cap. :139.5uF
Total Cap. :1079.5uF
ESR :3mOHM

+VGA_VCORE (1 Phase)
TDC :17.72A
Frequency :305KHz
PWR Cap. :940uF
EE Cap. :139.5uF
Total Cap. :1079.5uF
ESR :3mOHM

R8727 在1phase時上的阻值是27K

C8703 在GL時上的阻值是2200pF

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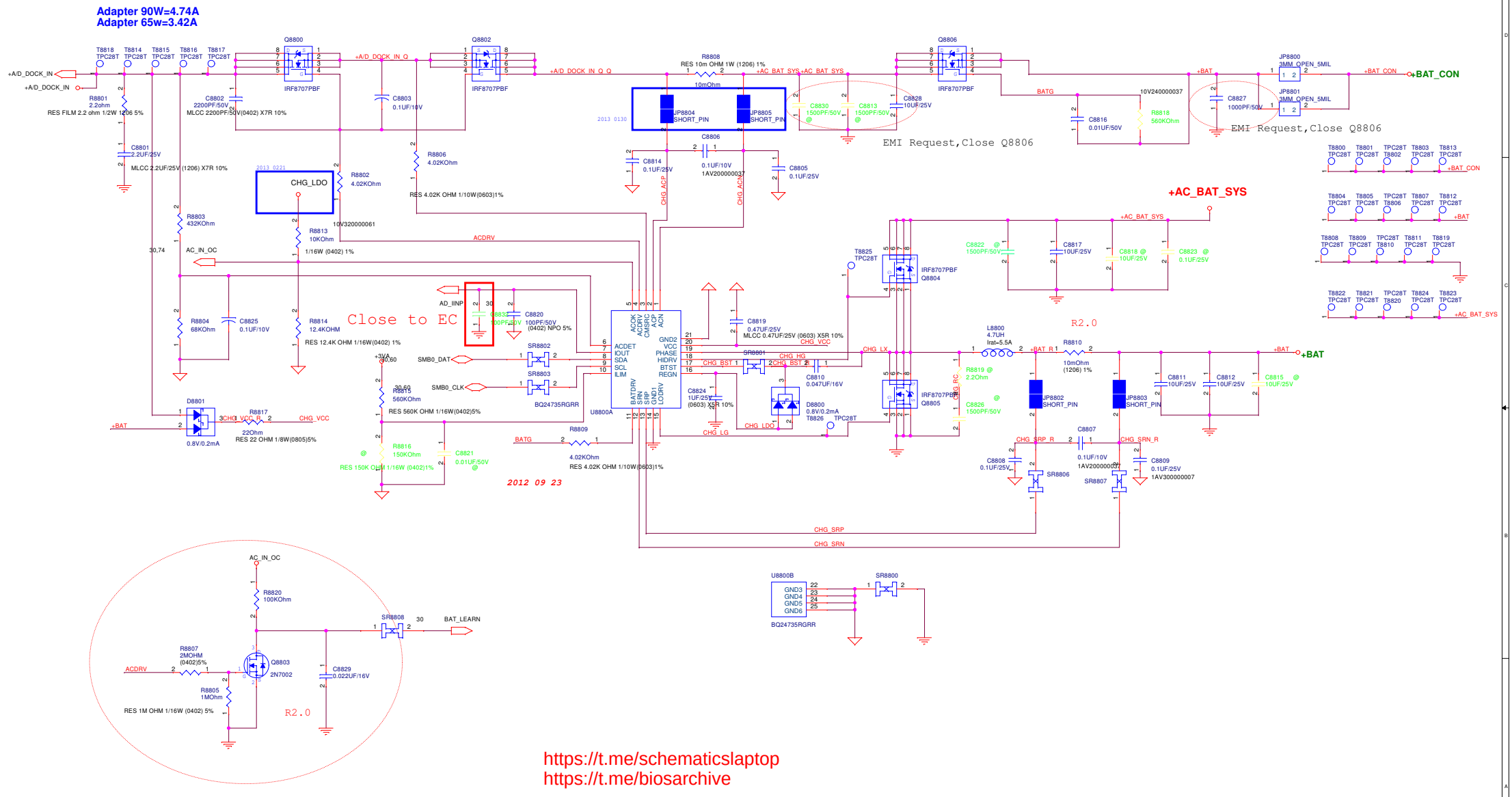
<Variant Name>
PEGATRON Title : POWER_VGACORE
Engineer: Adams Lin
Size: Custom | Project Name: TODS | Rev: 1.0
Date: Tuesday, February 26, 2013 Sheet 87 of 99

BATTERY CHARGER



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<Variant Name>

PEGATRON Title :POWER_CHARGER

Engineer: Duke_Wen

Size	Project Name	Rev
Custom	SB5	2.0

Date: Tuesday, February 26, 2013 Sheet 88 of 15

<Variant Name>

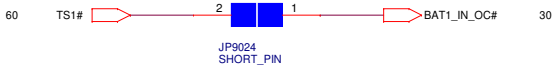
PEGATRON Title : POWER_N/A

Engineer:

Size	Project Name	Rev
A		1.1

Date: Tuesday, February 26, 2013 Sheet 89 of 99

BATTERY IN DETECT



<Variant Name>

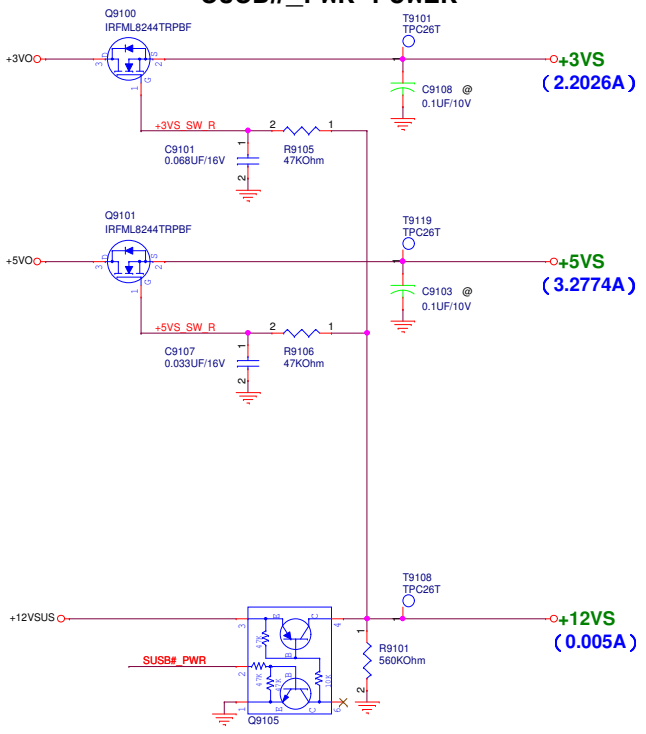
PEGATRON Title : POWER_DETECT

Engineer: Duke_Wen

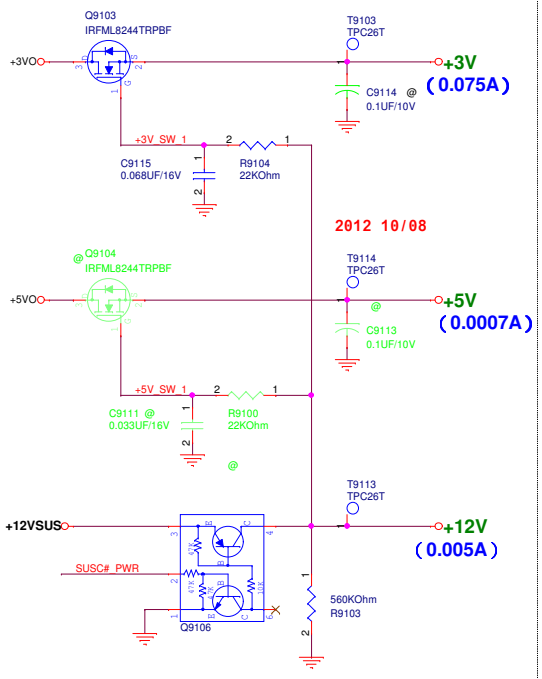
Size	Project Name	Rev
Custom	SB5	1.1

Date: Tuesday, February 26, 2013 Sheet 90 of 99

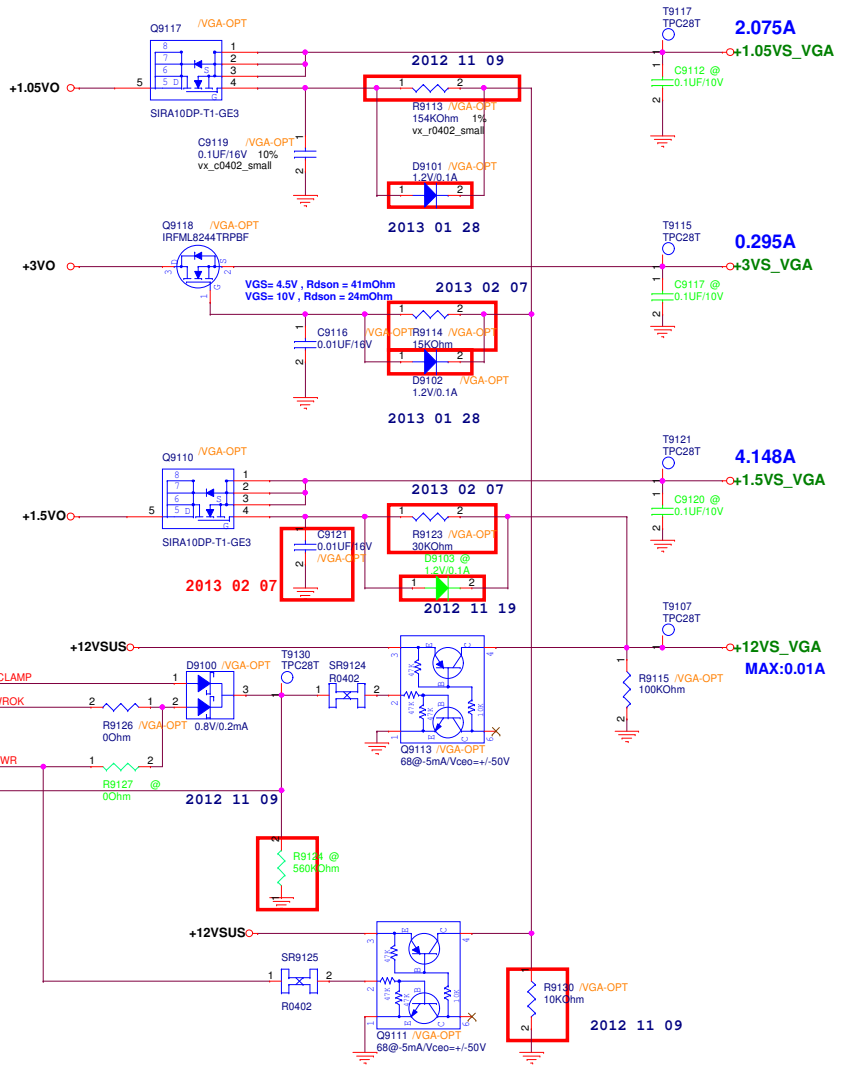
SUSB#_PWR POWER



SUSC#_PWR POWER 2012 09 21



DSC#_PWR POWER(DGPU)



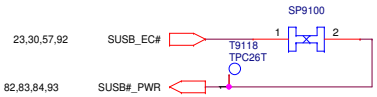
30,71,74 GPU_FB_CLAMP

25,87,92 DGPU_PWROK

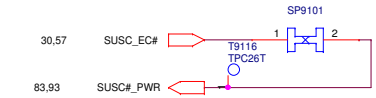
57,87,91,93 DGPU_EN_PWR

57 DGPU_PWROK_C

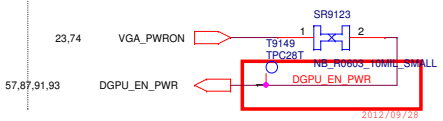
SUSB#_PWR POWER Control



SUSC#_PWR POWER Control



DSC_VGA_PWR POWER Control



<Variant Name>

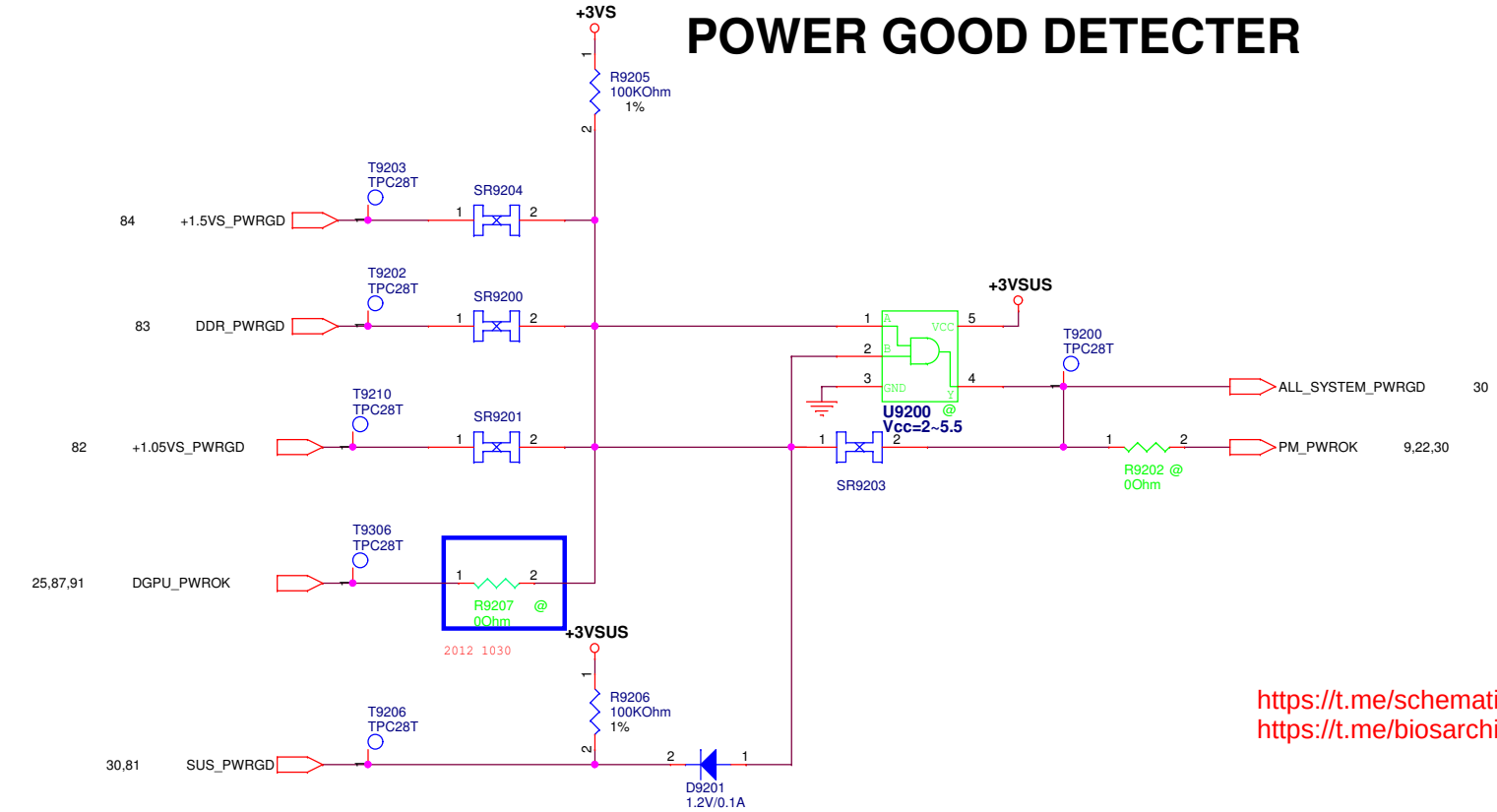
PEGATRON Title :POWER_LOAD SWITCH

Engineer: Mario_tsai

Size	Project Name	Rev
Custom	CP1	1.0

Date: Tuesday, February 26, 2013 Sheet 91 of 94

POWER GOOD DETECTER



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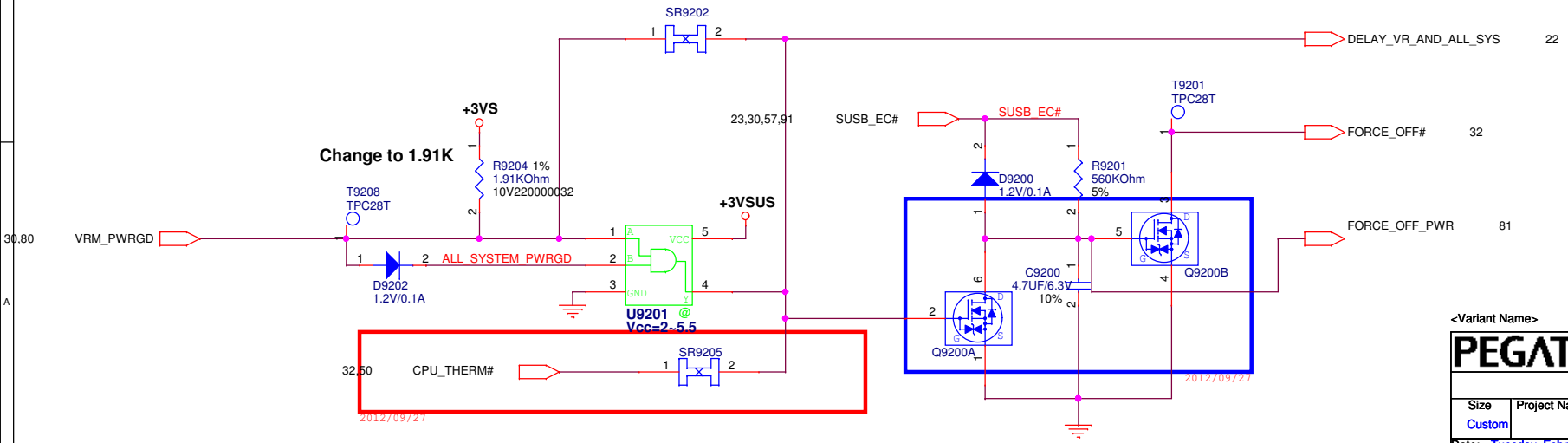


<Variant Name>

PEGATRON Title : POWER_PROTECT

Engineer: Duke_Wen

Size	Project Name	Rev
Custom	SB5	2.0

Date: Tuesday, February 26, 2013 Sheet 92 of 94

+AC_BAT_SYS → +AC_BAT_SYS 45,66,80,81,82,83,84,87,88

+BAT_CON → +BAT_CON 60,88

+5VA → +5VA 56,81

+3VA → +3VA 20,27,30,33,57,60,65,81,88

+5VO → +5VO 81,82,84,91

+3VO → +3VO 70,81,91

+1.05VSUS → +1.05VSUS

+1.05VO → +1.05VO 82,91

+12VSUS → +12VSUS 33,51,81,91

+5VSUS → +5VSUS 51,52,81,83

+3VSUS → +3VSUS 22,23,27,28,30,33,37,53,81,92

+12V → +12V 37,91

+5V → +5V 91

+3V → +3V 23,44,45,57,91

+12VS → +12VS 28,48,57,91

+5VS → +5VS 30,31,36,46,48,50,51,56,57,66,80,87,91

+3VS → +3VS 4,16,17,20,21,22,23,25,26,27,28,30,31,32,36,40,45,46,48,50,51,53,57,91,92

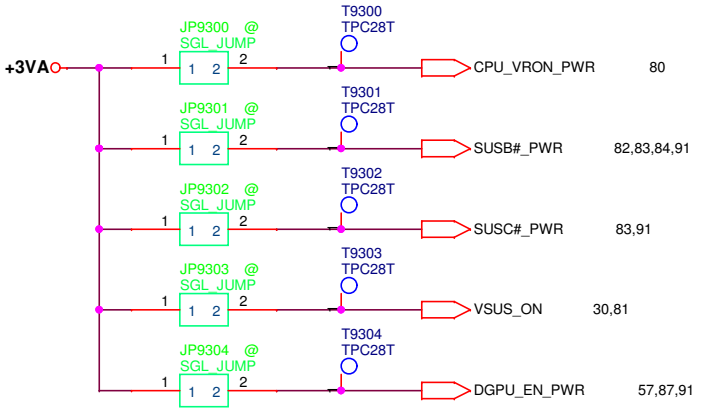
+1.5VS → +1.5VS 20,21,22,24,26,27,53,57,84

+1.05VS → +1.05VS 4,26,27,32,57,80,82

+3VA_WLAN → +3VA_WLAN

+VCORE → +VCORE 6,9,57,80

FOR POWER TEST



<Variant Name>

PEGATRON Title : POWER_SIGNAL

Engineer: Duke_Wen

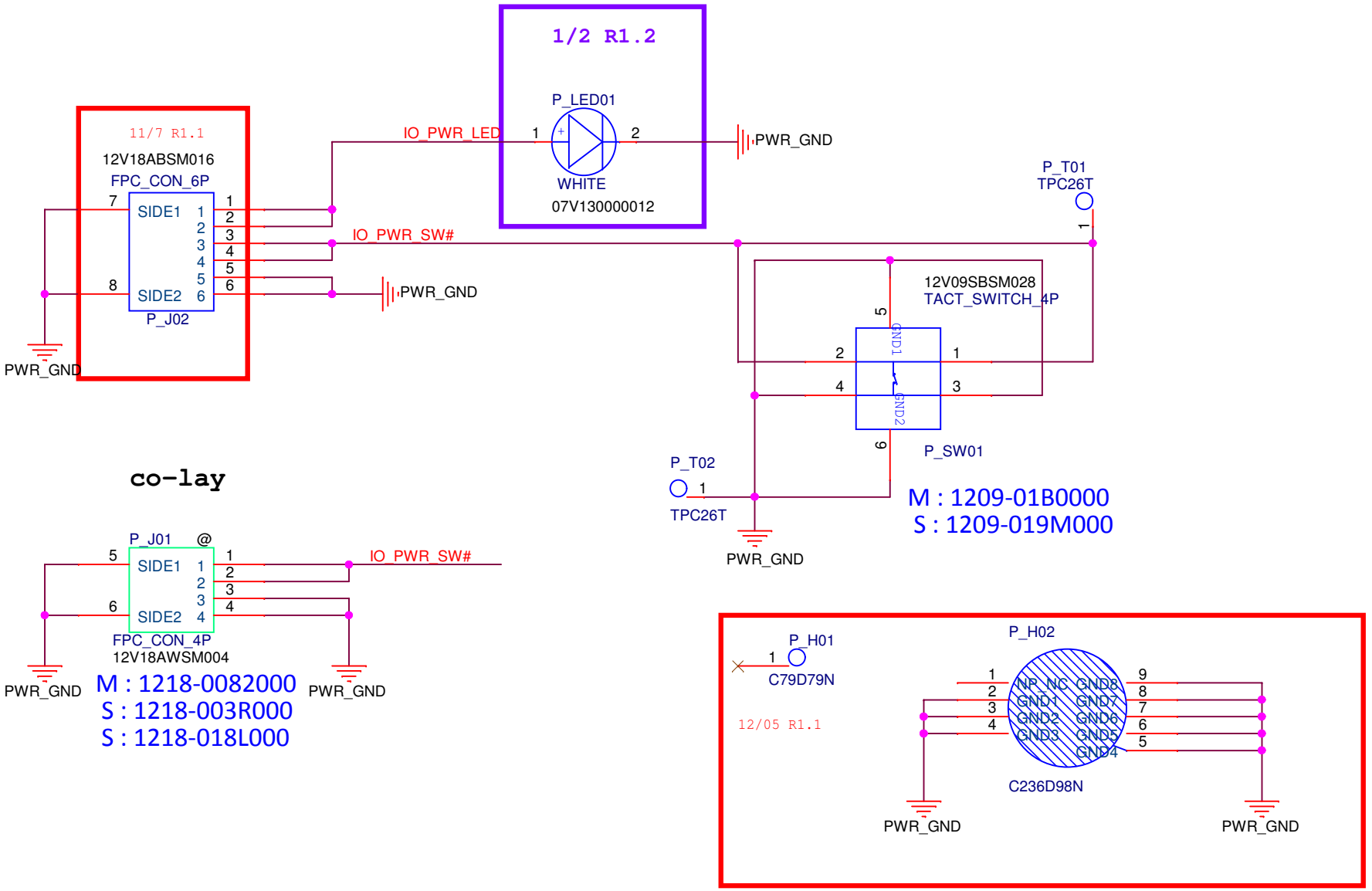
Size	Project Name	Rev
Custom	SB5	2.0

Date: Tuesday, February 26, 2013 Sheet 93 of 94

modify notice

Version Date	Description
2012/09/27	
Page 81	Delete D8106 circuit
Page 92	Add CPU_THERMAL# signal (Add SR9205) to pull low FPRCE_OFF#
Page all	Updata all the circuit optional table
Page 92	Update Q9200 footprint
2012/09/28	
Page 80	Reserve Input CAP C8057/ C8059 / C8060 =10UF/25V CE8056/ CE8058/ CE8061 = 68UF/25V
Page 81	Update FORCE_OFF_PWR net shape
Page 82	Change Output CAP C8204 optional attribute to @ Change SR8201 to R8219=4.7ohm Change U8200 to thermal pad attribute
Page 84	Change Output CAP C8420 optional attribute to @ Change SR8400 to R8420=4.7ohm Change U8400 to thermal pad attribute Remove LP# control
Page 91	Add SR9123 for DGPU_EN_PWR net shape Change C9119(0.033UF/16V) R9113(22K) to 0.22UF/16V 68K Change C9116(0.033UF/16V) R9114(22K) to 0.01UF/16V 10K Change C9121(0.33UF/16V) R9123 (22K) to 0.01UF/16V 15K Delete Q9114 Q9115 R9129 R9123 R9125 R9116 Add R9128 =100K Change R9126=0ohm to SR9126
2012/10/19	
Page 82	Change L8200 from 0.68UH to 0.47UH for
Page 82	Add C8204/ C8201
2012/10/10	
Page 82/84	Change U8200/U8400 footprint
Page 80	Change part reference from R9207 to R8069
2012/10/11	
Page 91	Change Q9117/Q9107 from SIR166 to SIRA10
Page 88	Change C8827 from 1500PF/50V to 1000PF/50V
2012/10/12	
Page 82	Add U8200B(GND 2VIA)
2012/10/30	
Page 92	Change SR9206 from shootpin to R9207
2012/11/2	
Page 91	Change C9121 from mount to unmount
2012/11/6	
Page 81	Change C8105 and C8110 from 0.1uF/10V to 0.1uF/25V
Page 82	Change C8235 from 0.1uF/10V to 0.1uF/25V
Page 83	Change C8310 from 0.1uF/10V to 0.1uF/25V
2012/11/7	
Page 81	Change C8105 and C8110 from 1AV200000041 to 1AV200000045
Page 82	Change C8235 from 1AV200000041 to 1AV200000045
Page 83	Change C8310 from 1AV200000041 to 1AV200000045
2012/11/8	
Page 81	Change Bom option of R8134 and D8104 from N/A to /USBSLP
Page 87	Remove R8702 and discrete only circuit
2012/11/9	
Page 87	unmout D8700 and C8713 Change R8722 from 20kohm to 0ohm Change R8727 from 16.5kohm to 20kohm (2Phase) Change R8727 from 18kohm to 27kohm (1Phase)
Page 91	Change R9113 from 68kohm to 71.5kohm Change R9123 from 15kohm to 17.4kohm Change R9130 from 100kohm to 10kohm
2012/11/12	
Page 87	Change R8722 from 0ohm to short pin
2012/11/19	
Page 82	Change D8200 optional attribute to @ for EE request
Page 91	Reserve D9102/D9103/D9101 for N14 discharge timing
Page 91	Add net DGPU_PWROK_C for VGA discharge
2012/11/23	
Page 88	Change size of R8802 R8806 and R8809 from 0402 to 0603 for power dissipation heat
2012/11/28	
Page 87	Change Optional of R8724 to /VGA from @ for EE request change net name from AC_BAT_SYS to +AC_BAT_SYS change net name from BAT_CON to +BAT_CON
2012/11/30	
Page 87	Change SR8701 to R8701 (0ohm) and unmount change C8720 from 1500pF/50V to 2700pF/50V and mount (GL C8720 change to 2200pF/50V) Unmount C8703 Increase C8729(4.7uF/6.3V),R8729(16K),R8730(43K) and R8730 (80.6K) but all unmout for co-lay UPI1658Q
2012/12/13	
Page 87	Charge C8721 PIN2 to GND from GND_RT8813A for FAE request.
2012/12/18	
Page 82/84	Change U8200/U8400 from TPS51362 to TPS51363,‧(pin to pin)
2013/01/30	
Page 82	Charge size of C8235 from 0402 to 0603.
Page 87	Charge option of R8729 from N/A to @ .
Page 88	Charge net name from A/D_DOCK_IN to +A/D_DOCK_IN .
2013/02/06	Page 80 1.R8012 for 2Phase to 4.02KOhm，for 3Phase to 3KOhm 2.C8054 for 3Phase to 1500pF/50V to mount 3.R8014 change to 6.04KOhm 4.C8031、C8034、C8035 to unmount Page 81 1.C8107上件 2. R8101 change to 130KOhm 3. R8100 change to 150KOhm 3.PT10 project不支援USB charger，R8134、D8104 to unmount 4.C8110、C8105 size change to 0603 from 0402 Page 82 1.電感放置0.68uH 2.輸出電容放置22uF/6.3V 6PCS*4 3.U8200 thermal pad footprint Page 83 1.C8310 size change to 0603 from 0402 2.C8320 to mount Page 87 1.C8729 change to 4700pF/25V Page 91 1.C9119 change to 0.1uF from 0.22uF 2.R9113 change to 154KOhm from 71.5KOhm 3.D9101、D9102 Optional change to /N14P-GV2 Page 92 1.R9204 change to 1.91Kohm
2013/02/07	Page 91 1.R9114 change to 15KOhm from 10KOhm 2.R9123 change to 30KOhm from 17.4KOhm 3.C9121 Optional change to /VGA-OPT

PEGATRON	Title : Power History
<OrgName>	Engineer: Duke_Wen
Size: Custom	Project Name: SB5 — Rev 2.0
Date: Tuesday, February 26, 2013	Sheet 95 of 99



PEGATRON

Title : PWR BD

BG1-HW R&D Dept.3

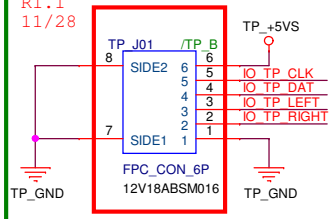
Engineer:

Size	Project Name	Rev
A	PT10SG	1.1

Date: Tuesday, February 26, 2013 Sheet 100 of 102

For TM-01146-003 TEX

R1.1
11/28



For 515-001540-01 p3

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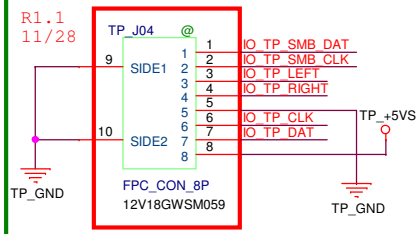

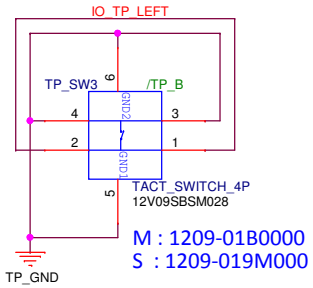

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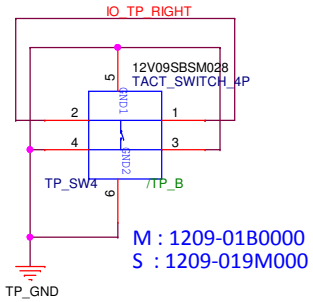

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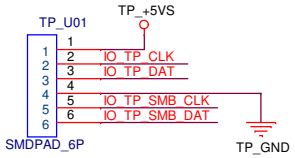

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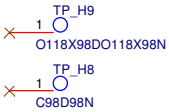

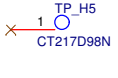

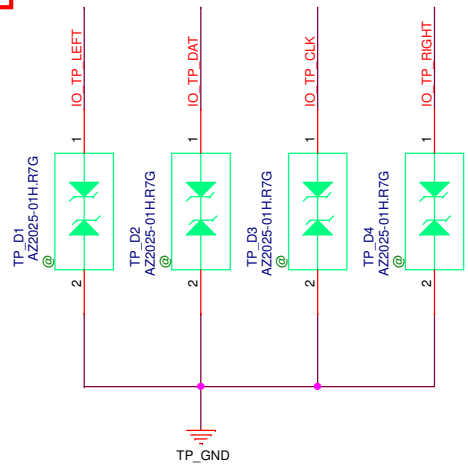

https://t.me/schematicslaptop
https://t.me/biosarchive

PEGATRON **Title : TP**

BG1-HW R&D Dept.3 **Engineer: *Tina Lee***

Size	Project Name	Rev
B	PT10SG	1.1

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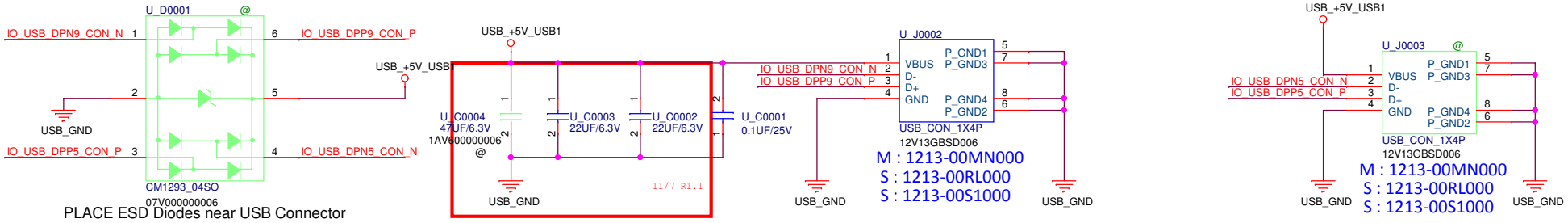

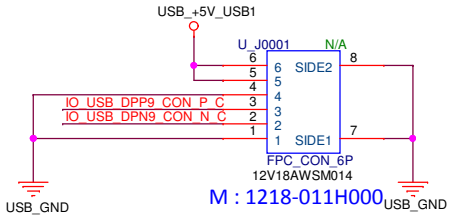

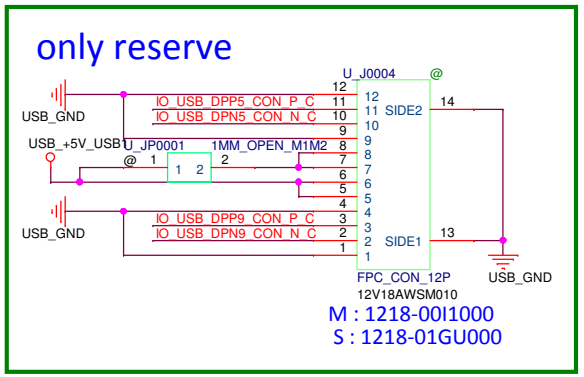

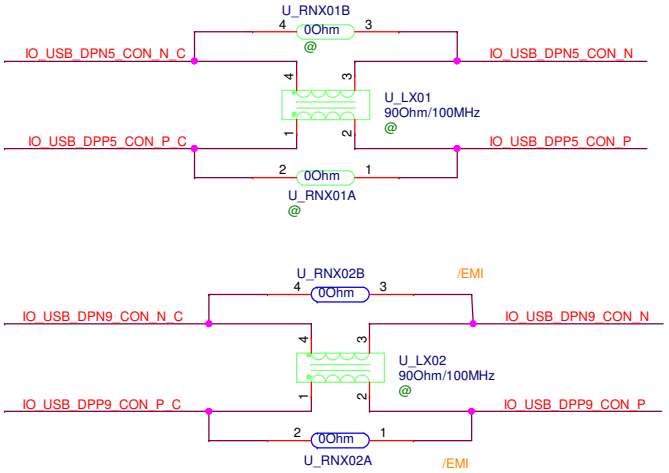

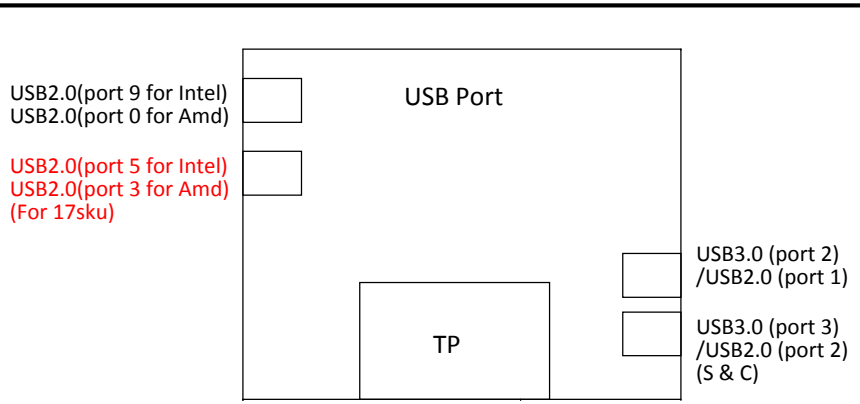

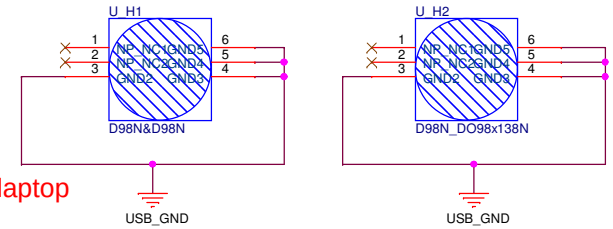

PEGATRON Title :IO_USB

BG1-HW R&D Dept.3 Engineer: Tina Lee

Size	Project Name	Rev
B	PT10SG	1.1

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