

# IAYAA

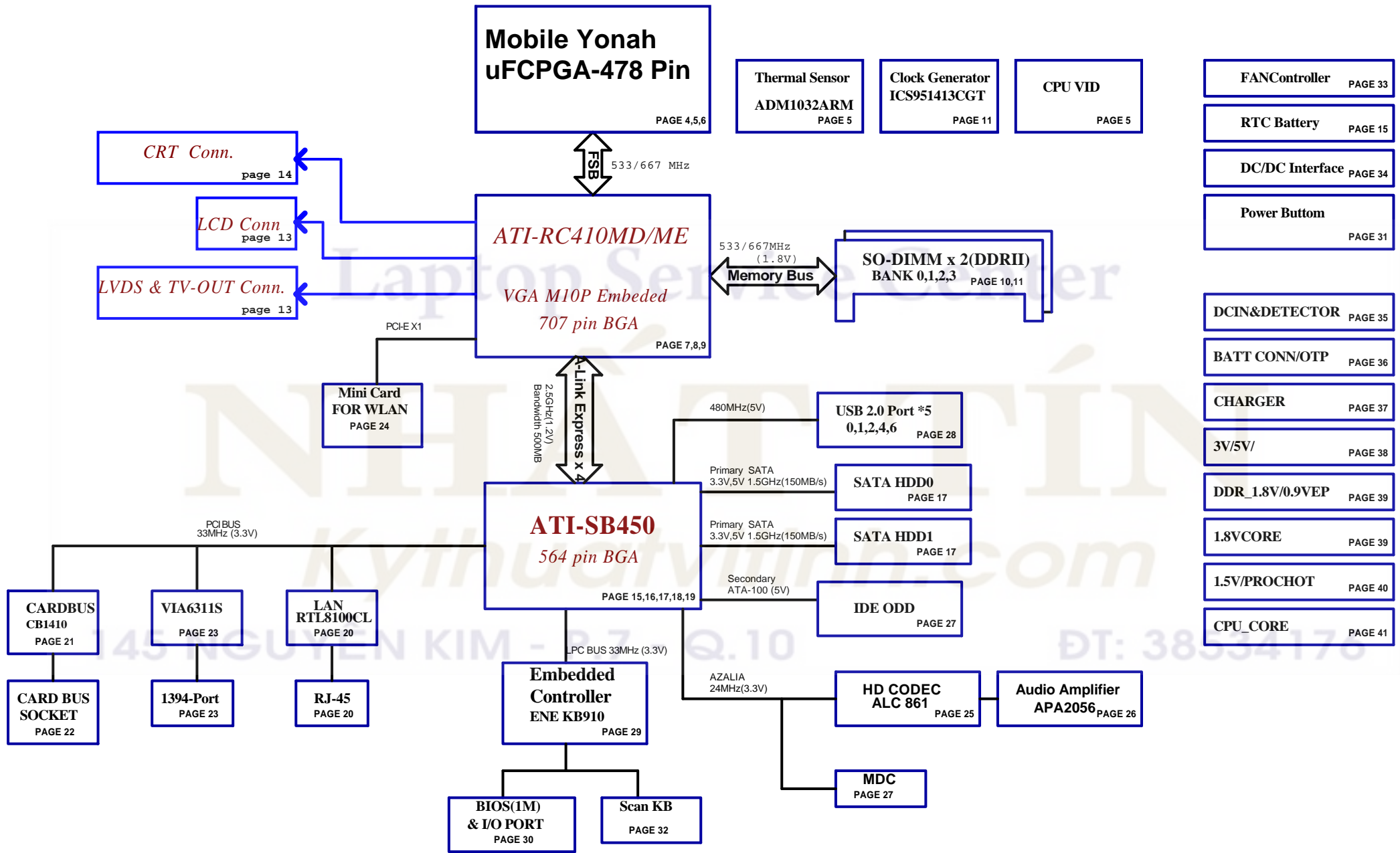
## LA-3391P REV 0.3 Schematic

UFC-PGA Yonah/ RC410MD(ME) / SB450

2006-10-05 Rev. 0.3

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2006/05/18	Deciphered Date	2007/05/18	Title	Black Diagram
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# IVYAA LA-3391P FUNCTION BLOCK DIAGRAM



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## Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	ON	ON	ON
B+	AC or battery power rail for power circuit.	ON	ON	ON
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+CPUVID	1.2V switched power rail for CPU AGTL Bus	ON	OFF	OFF
+VGA_CORE	1.0V/1.2V switched power rail for VGA chip	ON	OFF	OFF
+1.2VS	1.2VS for PCI-Express	ON	OFF	OFF
+0.9VS	0.9V switched power rail	ON	OFF	OFF
+1.5VS	DOTHAN B	ON	OFF	OFF
+1.8VS	1.8VS switched power rail	ON	OFF	OFF
+1.8VALW	1.8V always on power rail	ON	ON	ON*
+1.8V	1.8V power rail	ON	ON	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF.

## External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
Card Bus	AD20	2	PIRQB
LAN	AD22	1	PIRQG
1394	AD16	0	PIRQA

## EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b

## EC SM Bus2 address

## SB450 SM Bus address

Device	Address
Clock Generator (ICS951413CGLFT)	1101 001Xb
DDR DIMM0	1010 0100b A4
DDR DIMM1	1010 0110b A6

STATE	SIGNAL	SLP_S3#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)		HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	ON	OFF	OFF	OFF

## Board ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

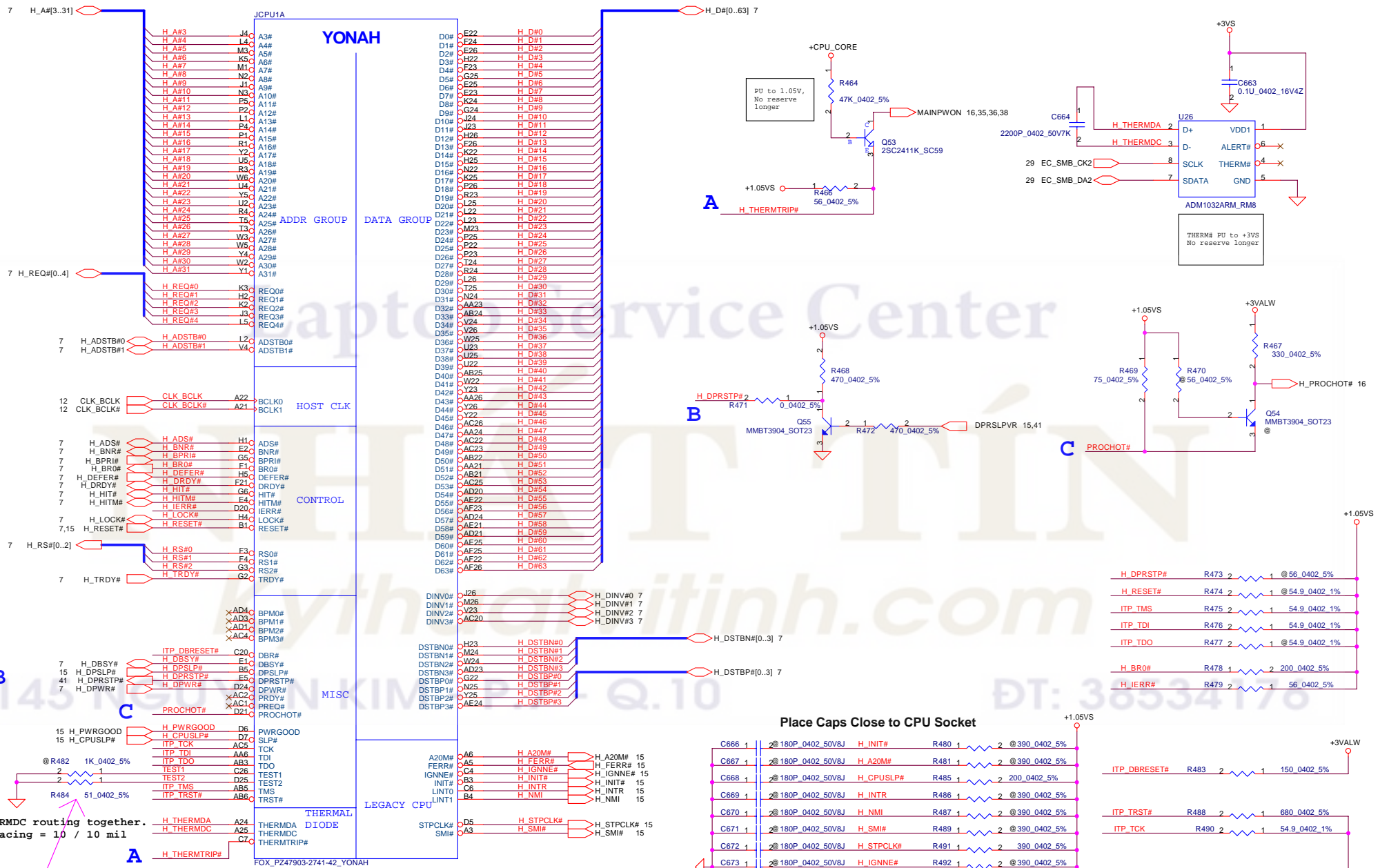
Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	1.0
4	
5	
6	
7	

BTO	BOM STURCTURE
WIRELESS	WLAN@
1394	1394@
MIC	MIC@, 45 MIC@
Second HDD	2H@
NB Chipset	MD@, ME@
MDC	MDC@

SKU ID	BTN_ID
0	1 Buttons
1	
2	
3	
4	7 Buttons
5	
6	
7	

SKU_ID	
0	WW
1	
2	
3	
4	JP
5	
6	
7	

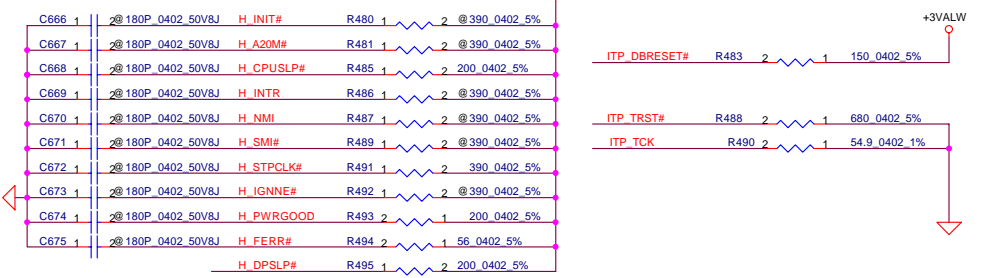
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H\_THERMDA, H\_THERMDC routing together.  
Trace width / Spacing = 10 / 10 mil

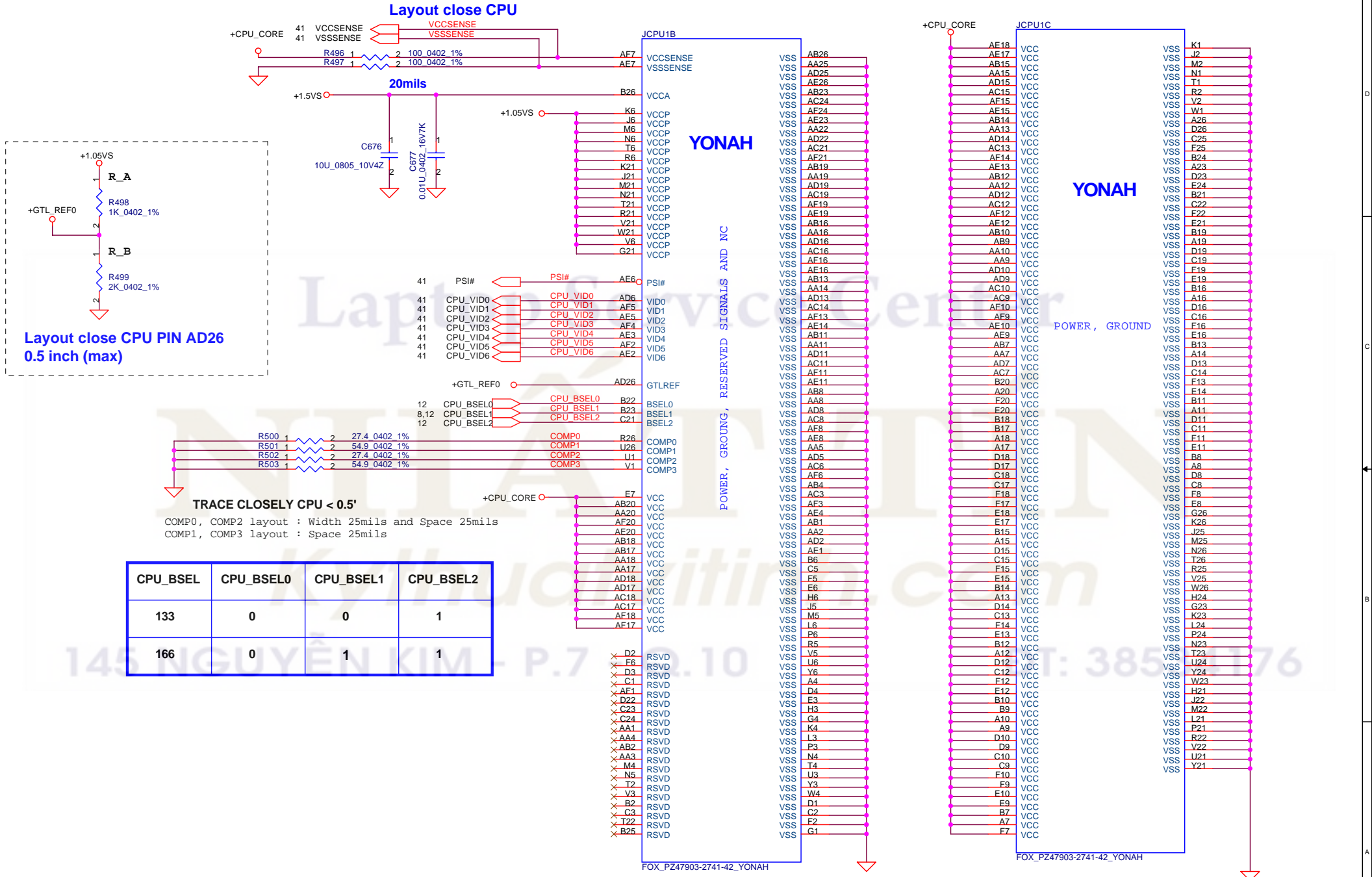
For B-0 stepping engineering samples (ES) of Celeron M processor need to pop this 51 ohm resistor.

**Place Caps Close to CPU Socket**

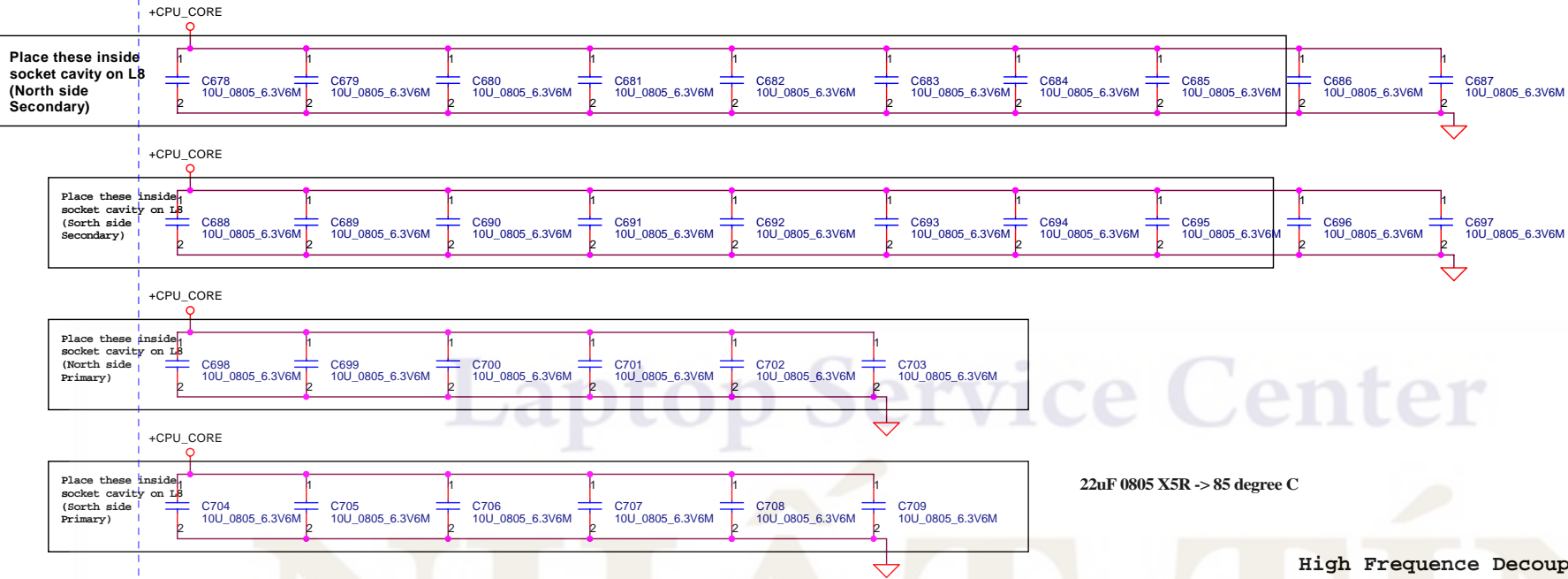


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Length match within 25 mils



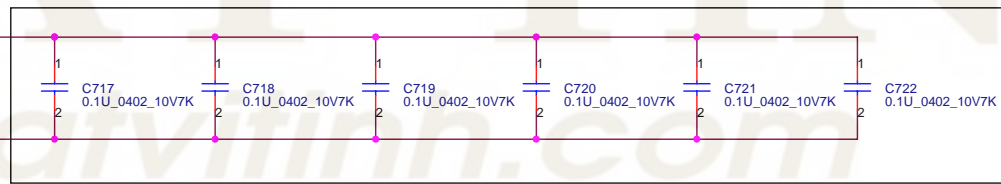
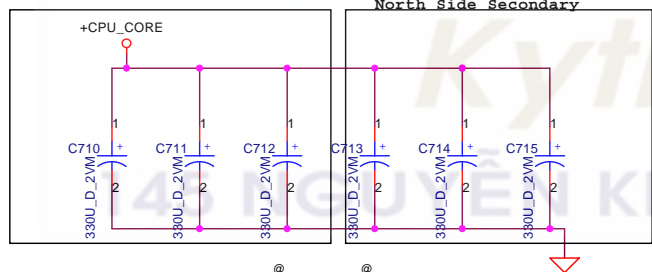
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**Near VCORE regulator.**

South Side Secondary

North Side Secondary



@ @

9mOhm 9mOhm 9mOhm 9mOhm 9mOhm 9mOhm

7343 7343 7343 7343 7343 7343

PS CAP PS CAP PS CAP PS CAP PS CAP PS CAP

**ESR <= 1.5m ohm**

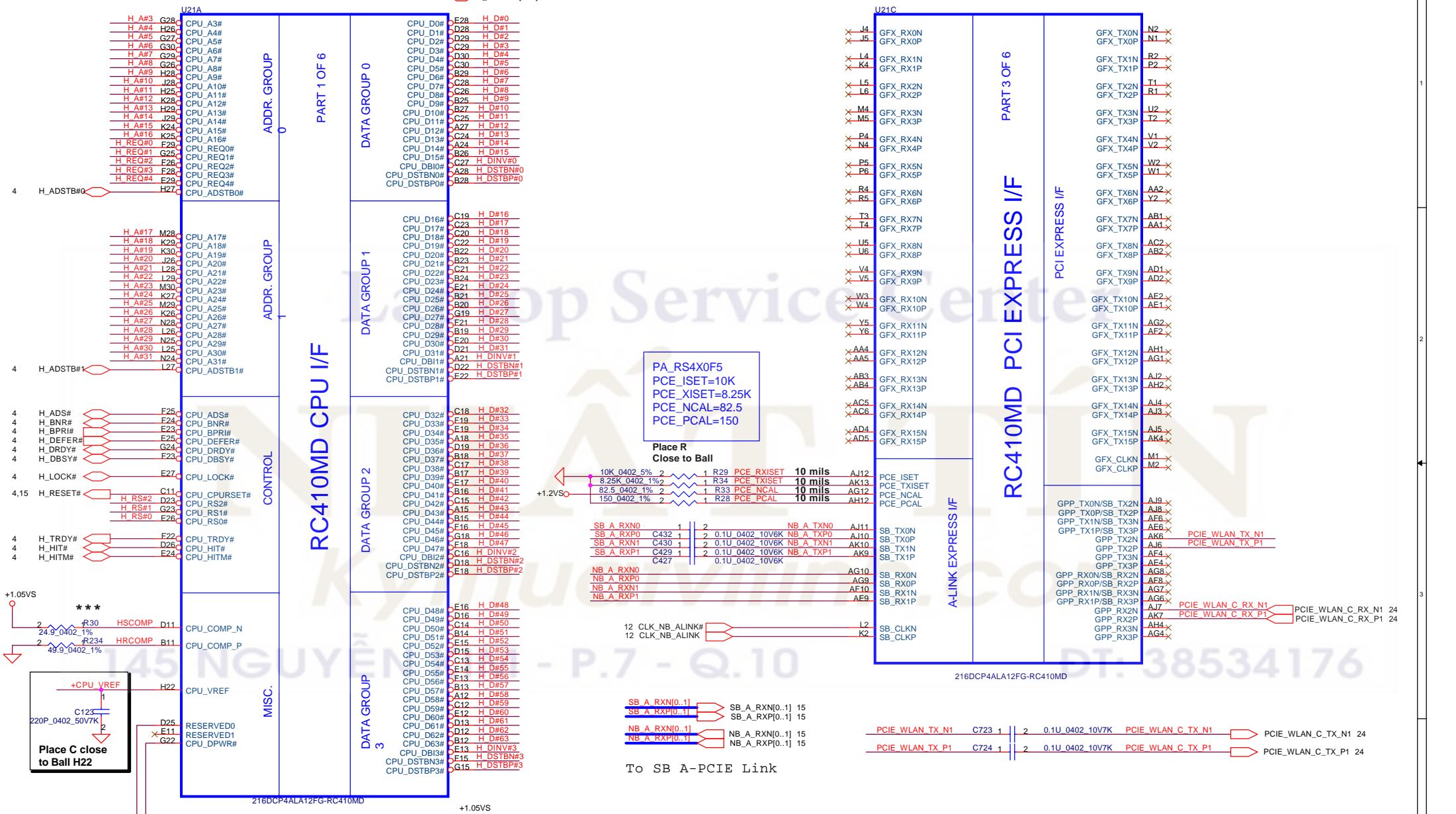
**Capacitor > 1980uF**

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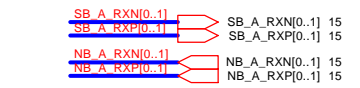
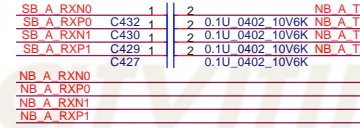
4 H\_A#[3..31]  
4 H\_REQ#[0..4]  
4 H\_RS#[0..2]

H\_D#[0..63] 4  
H\_DINV#[0..3] 4  
H\_DSTB#[0..3] 4  
H\_DSTBP#[0..3] 4

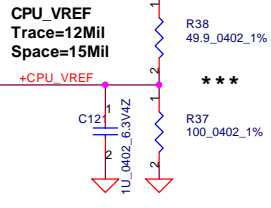
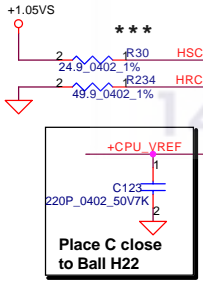


PA\_RS4X0F5  
PCE\_ISET=10K  
PCE\_XISET=8.25K  
PCE\_NCAL=82.5  
PCE\_PCAL=150

Place R  
Close to Ball

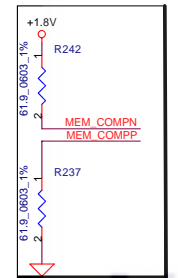
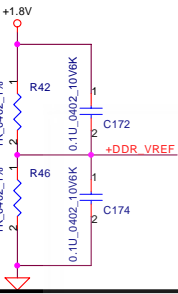
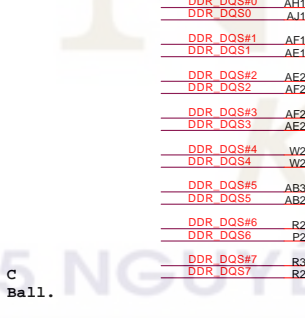
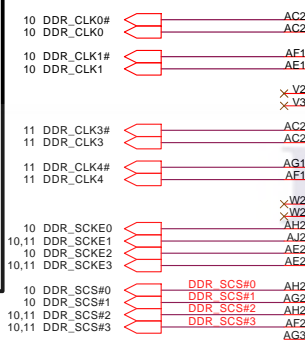
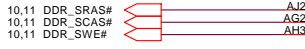
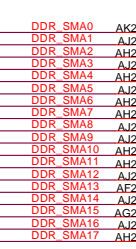
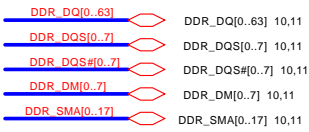


To SB A-PCIE Link

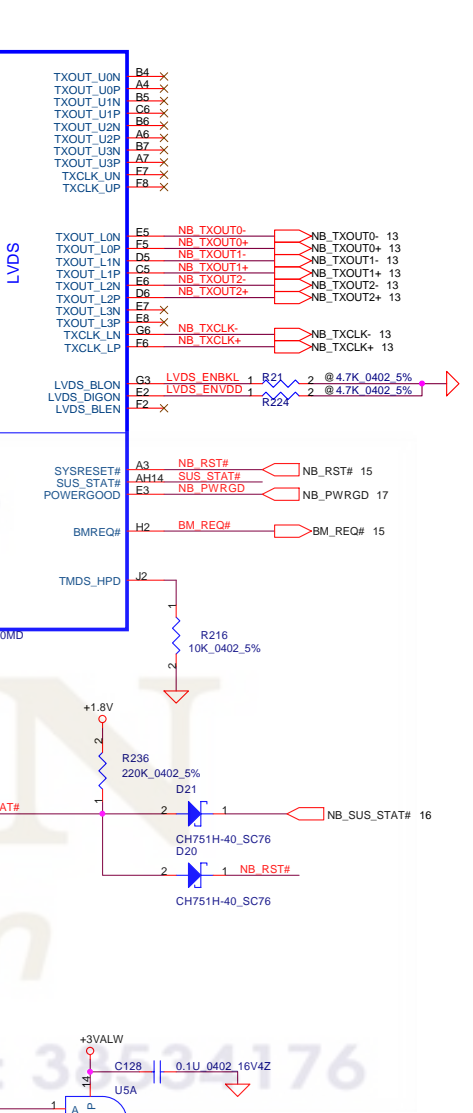
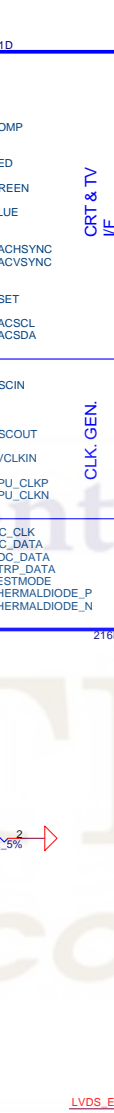
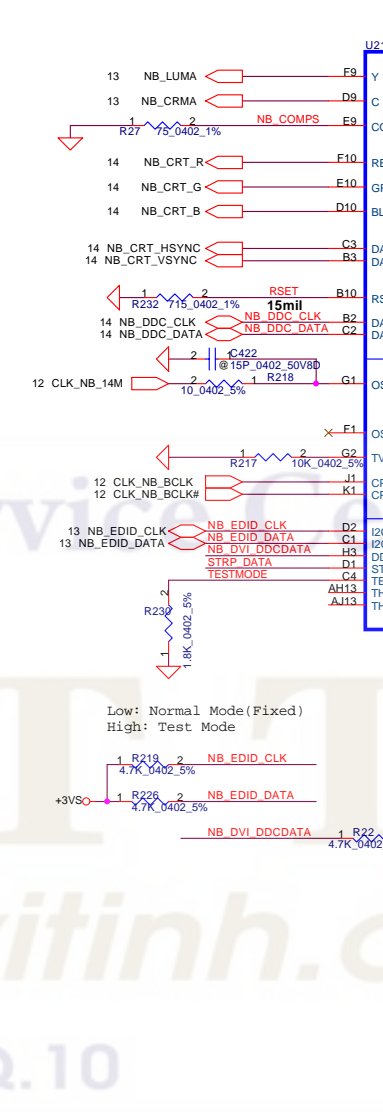
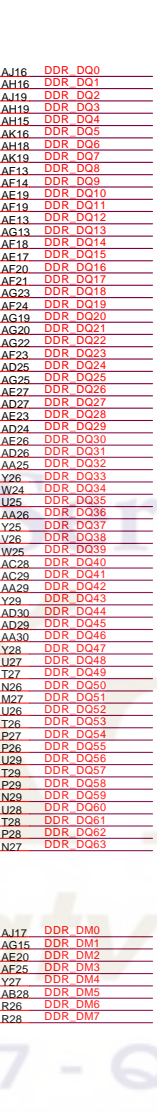
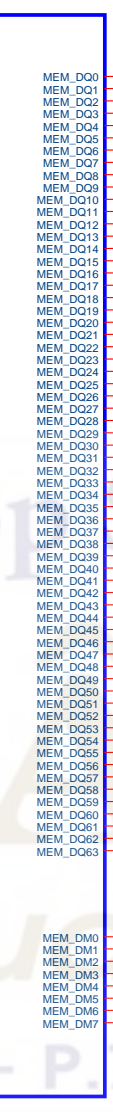


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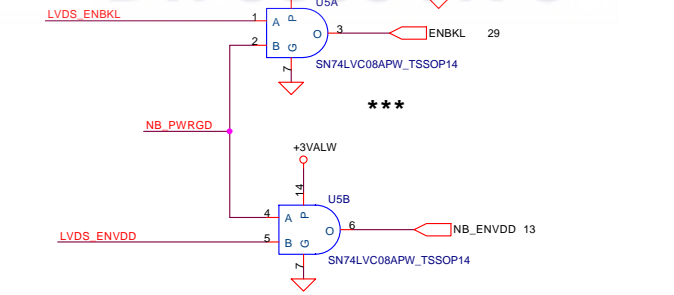
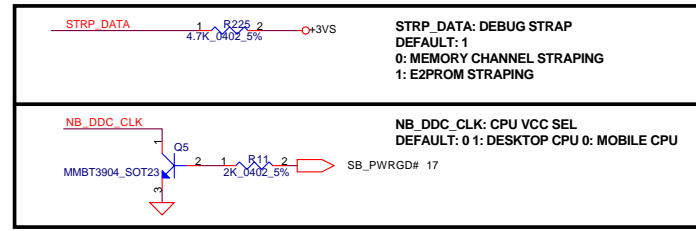
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Place these R and C close to relative Ball.

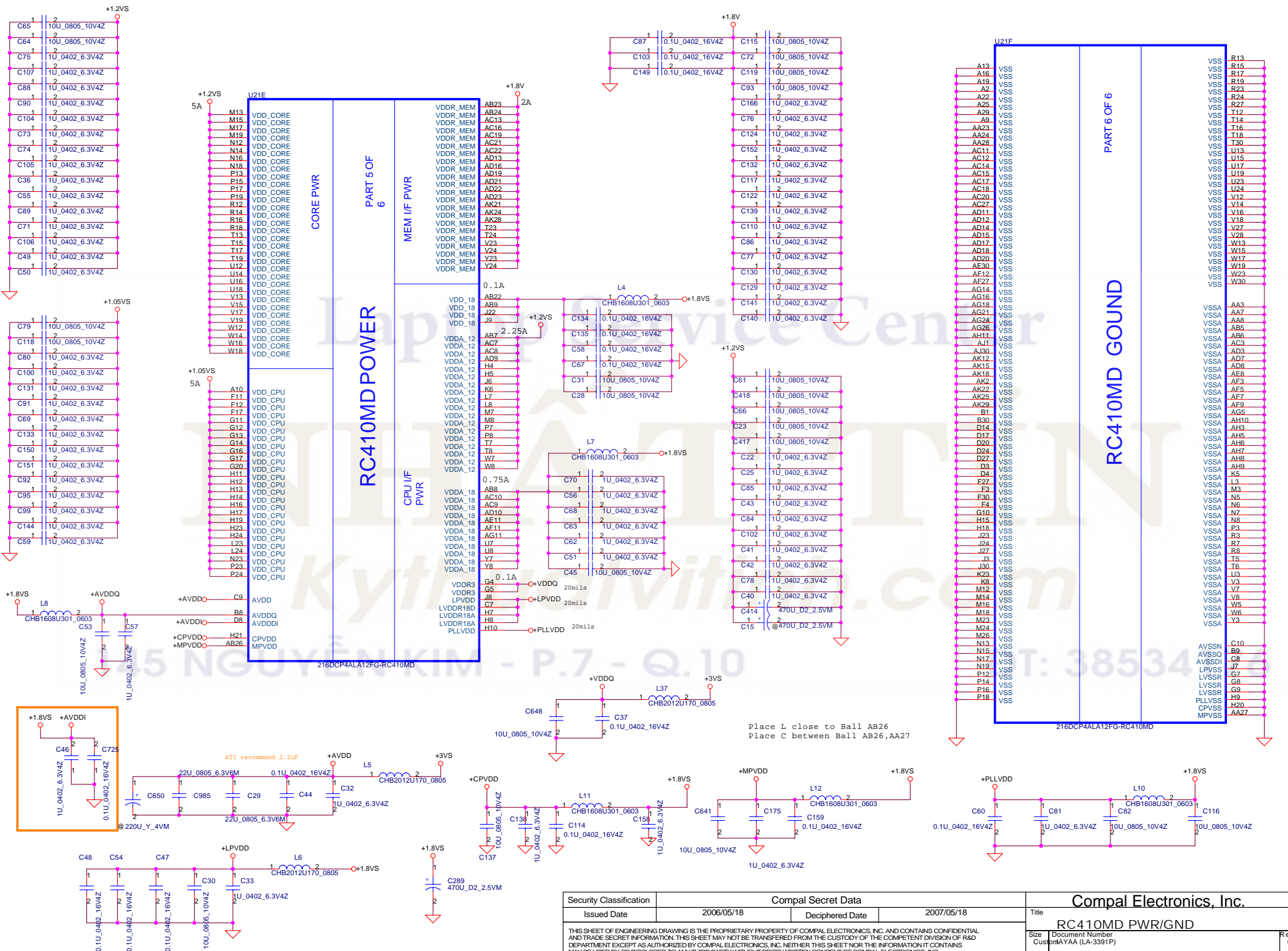


FSB SPEED	NB STRAPING PINS		
	BM_REQ#	NB_CRT_HSYNC	NB_CRT_VSYNC
1.66MHz	0	1	1
1.33MHz	0	0	1

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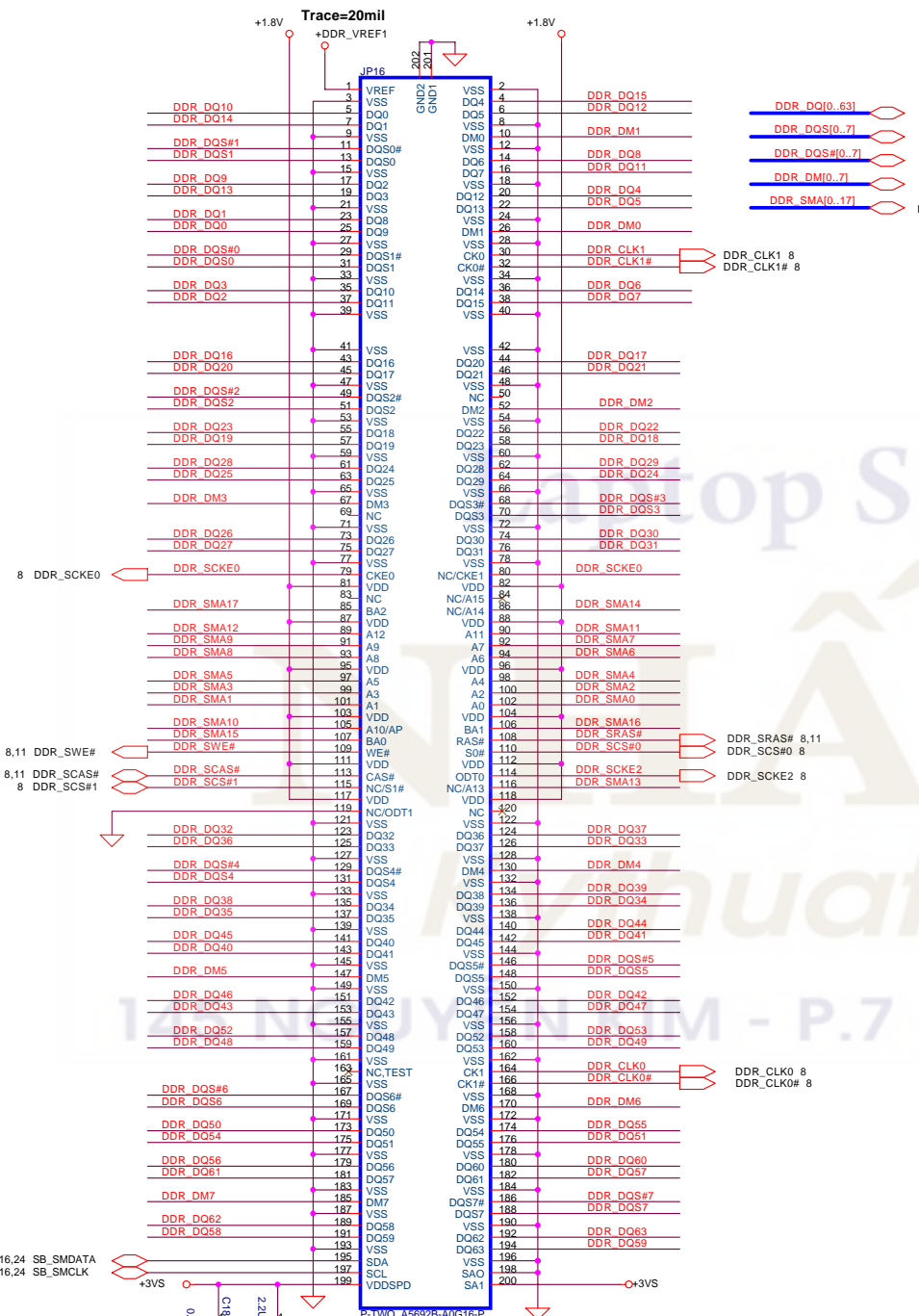




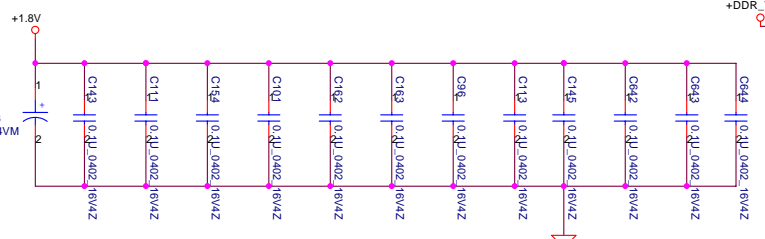
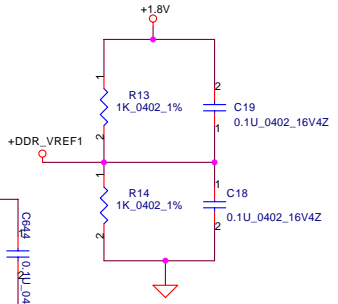
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RC410MD PWR/GND		
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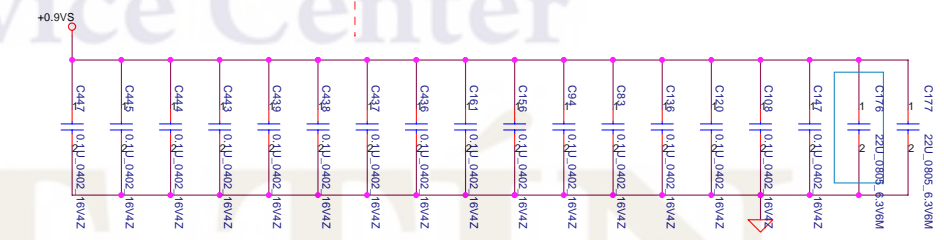
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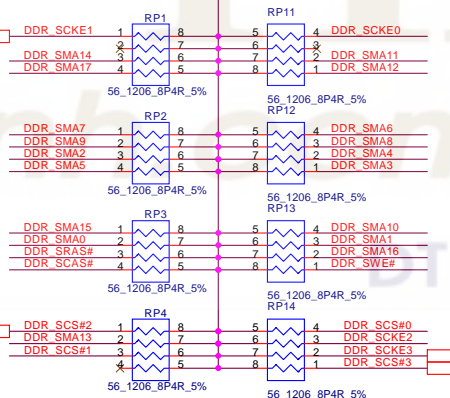
**Layout Note:**  
Place near JDIM1



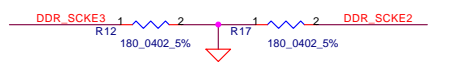
**Layout Note:**  
Place one cap close to every 2 pullup resistors terminated to V\_DDR\_MCH\_REF



**Layout Note:**  
Place these resistor closely JDIM2, all trace length < 750 mil



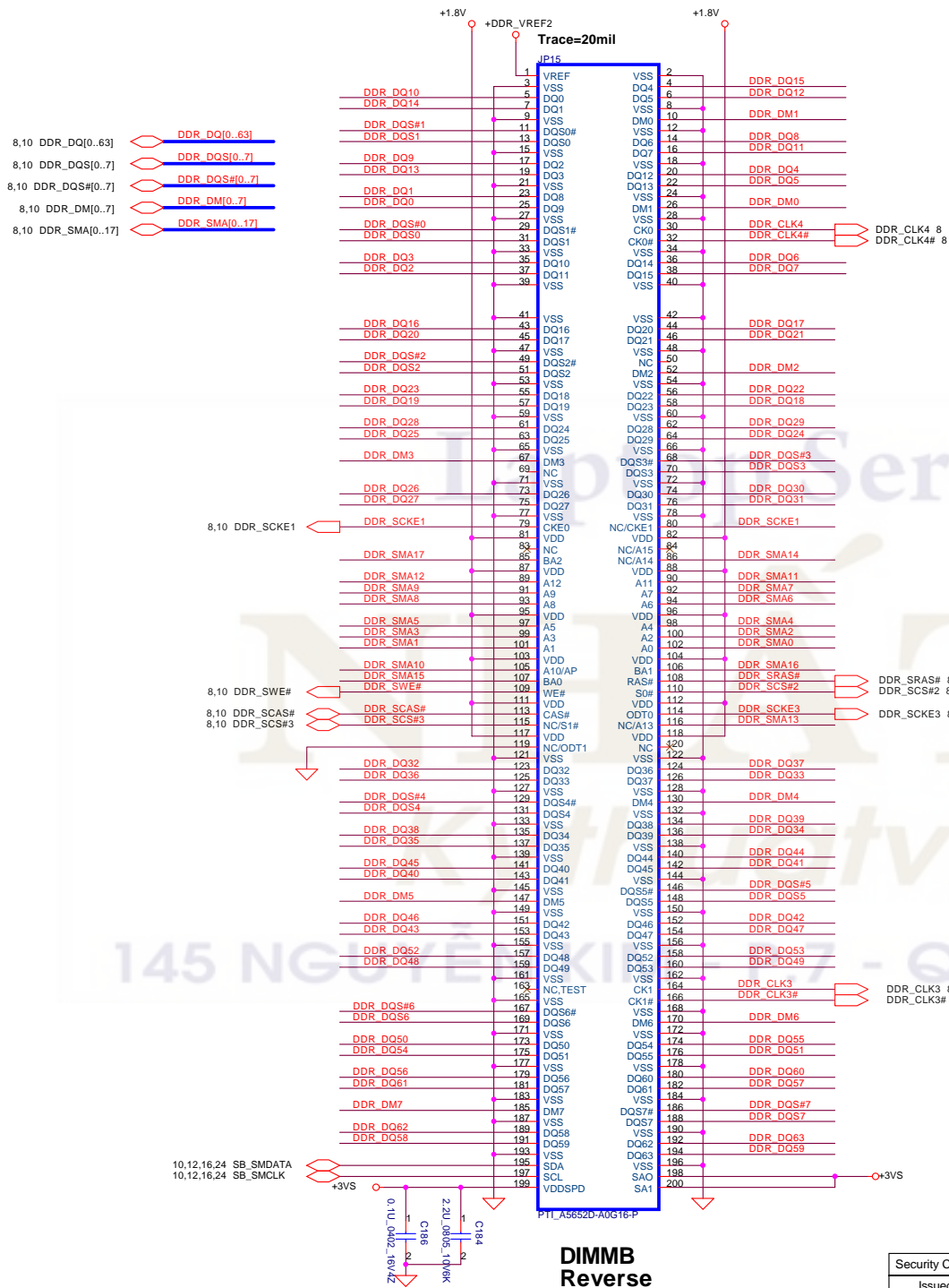
**Layout Note:**  
Place these resistor closely JDIM2, all trace length Max=1.3"



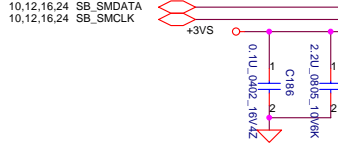
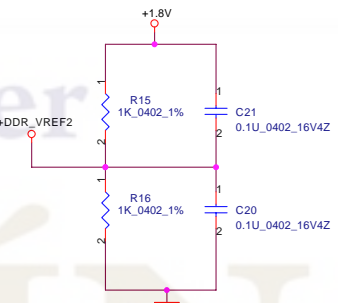
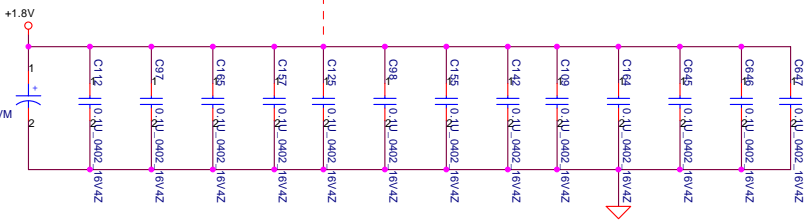
**Layout Note:**  
Place R12, R17 between JP15 and RP14

**DIMMA Reverse**

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**Layout Note:**  
Place near JDIM1



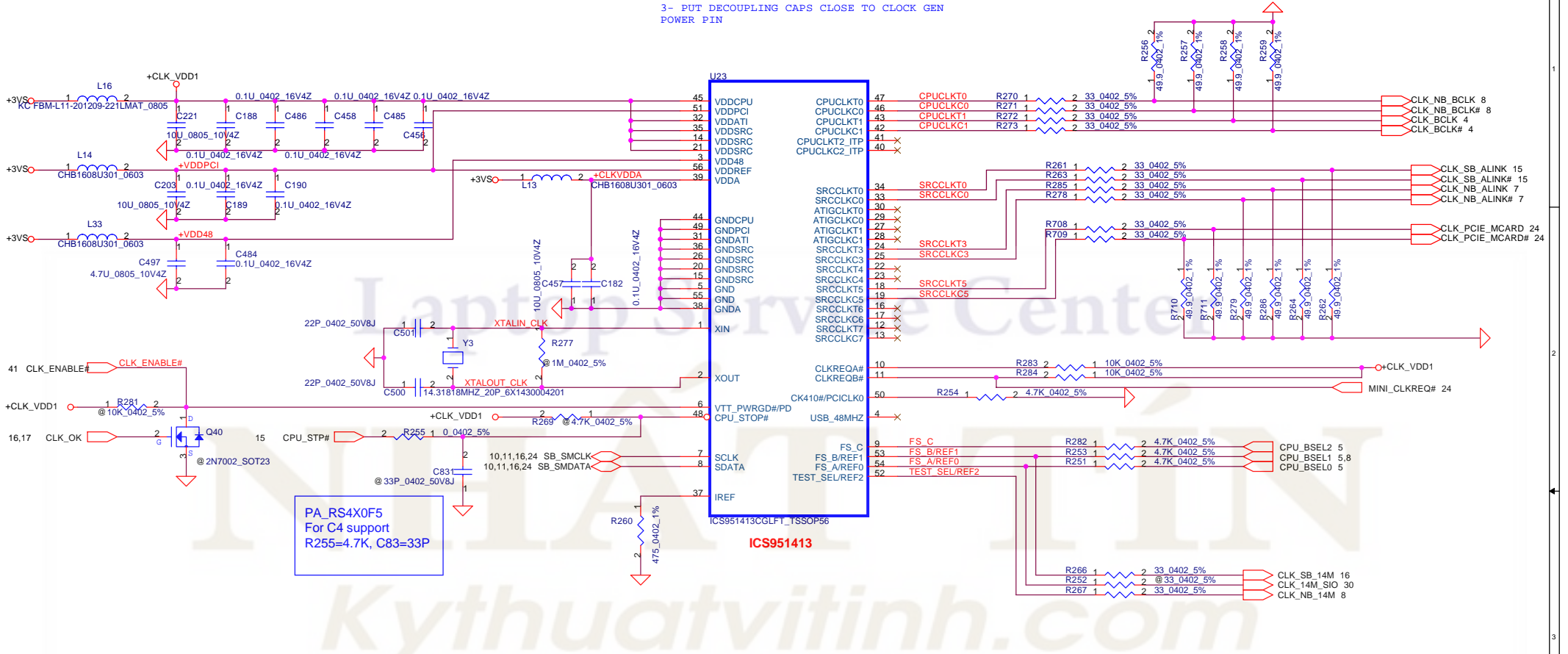
**DIMMB Reverse**

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# Clock Generator

- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO CLOCK GEN AS POSSIBLE
- 2- ROUTE ALL CPUCLK/#, NBCLK/#, ITPCLK/# AND SCR/# ,AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLOCK GEN POWER PIN



PA\_RS4X0F5  
For C4 support  
R255=4.7K, C83=33P

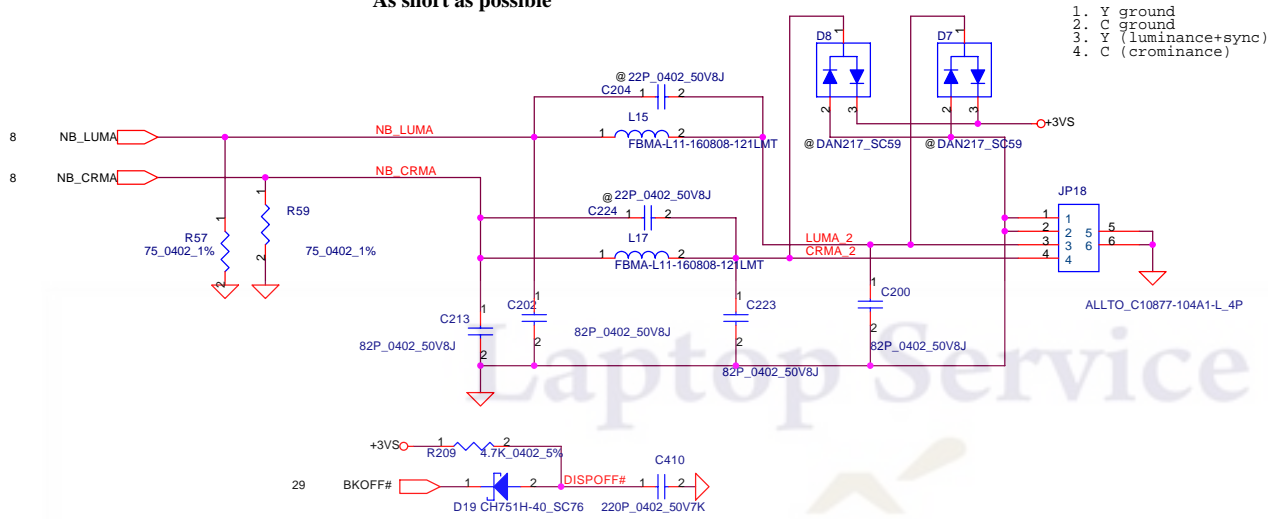
FS_C	FS_B	FS_A	CPU	SRC	PCI	REF	USB
1	0	1	100.00	100.00	33.33	14.318	48.000
0	0	1	133.33	100.00	33.33	14.318	48.000
0	1	1	166.66	100.00	33.33	14.318	48.000

145 NGUYỄN KIM

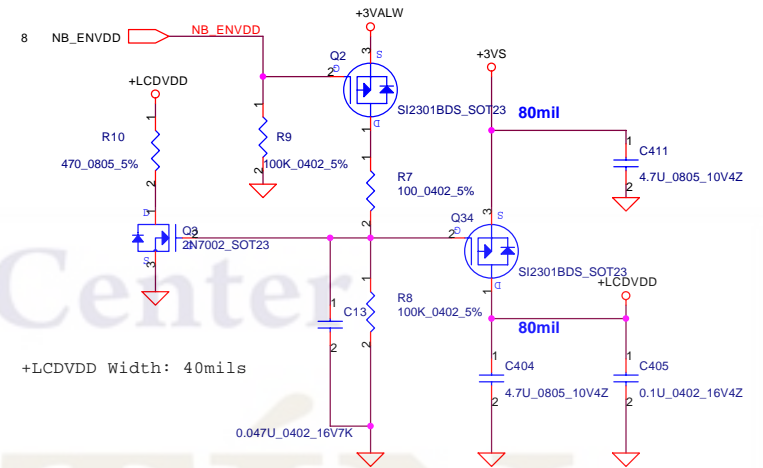
ĐT: 38534176

# TV-OUT CONNECTOR

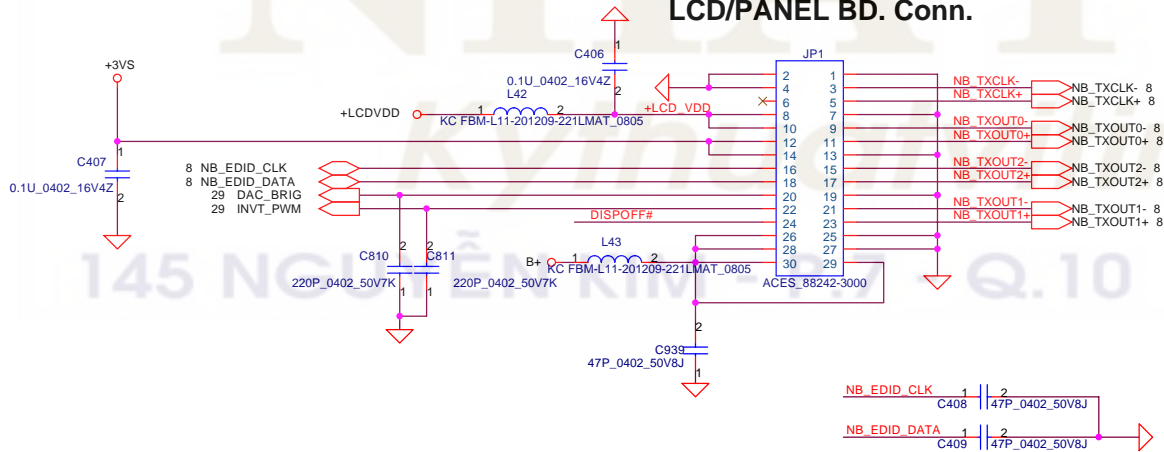
Reduce LUMA\_1 and CRMA\_1 length  
As short as possible



# PANEL +LCDVDD CTRL CKT

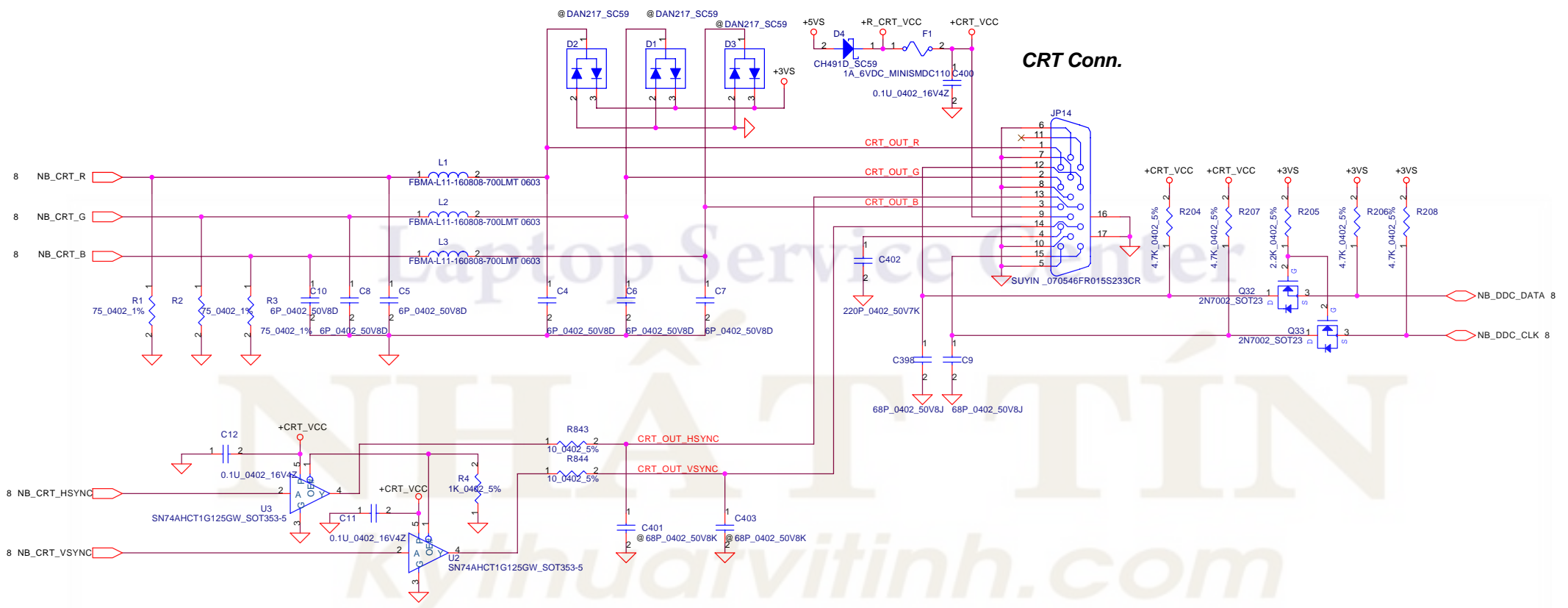


# LCD/PANEL BD. Conn.



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Size	B	Document Number	IAYAA (LA-3391P)	Rev	0.3
Date:	Thursday, October 05, 2006		Sheet	13	of 48

# CRT CONNECTOR

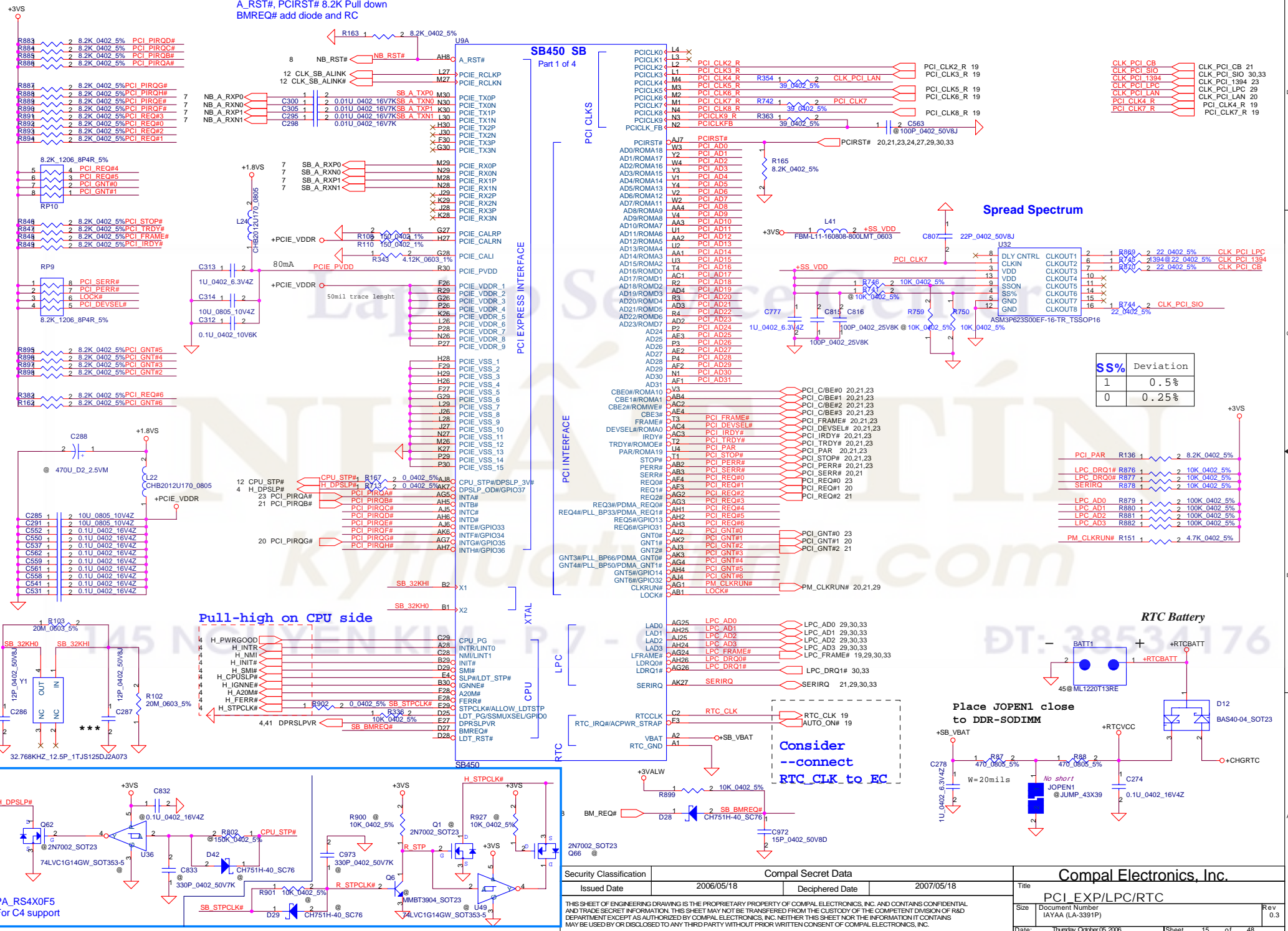


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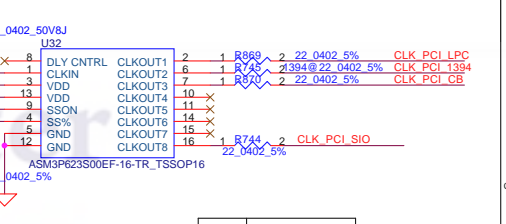
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PA\_IXP400AC16  
C300, C305, C295, C298=10nF  
A\_RST#, PCIRST# 8.2K Pull down  
BMREQ# add diode and RC

19,20,21,23 PCI\_AD[0..31] PCI\_AD[0..31]

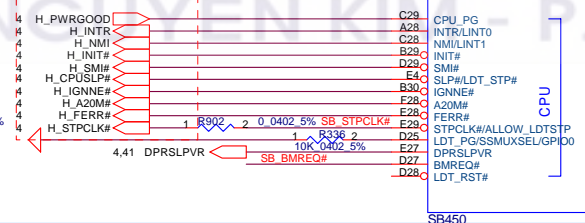


**Spread Spectrum**



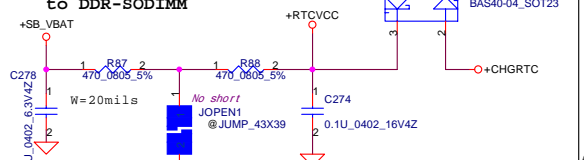
SS%	Deviation
1	0.5%
0	0.25%

**Pull-high on CPU side**



**Consider --connect RTC\_CLK to EC**

**Place JOPEN1 close to DDR-SODIMM**

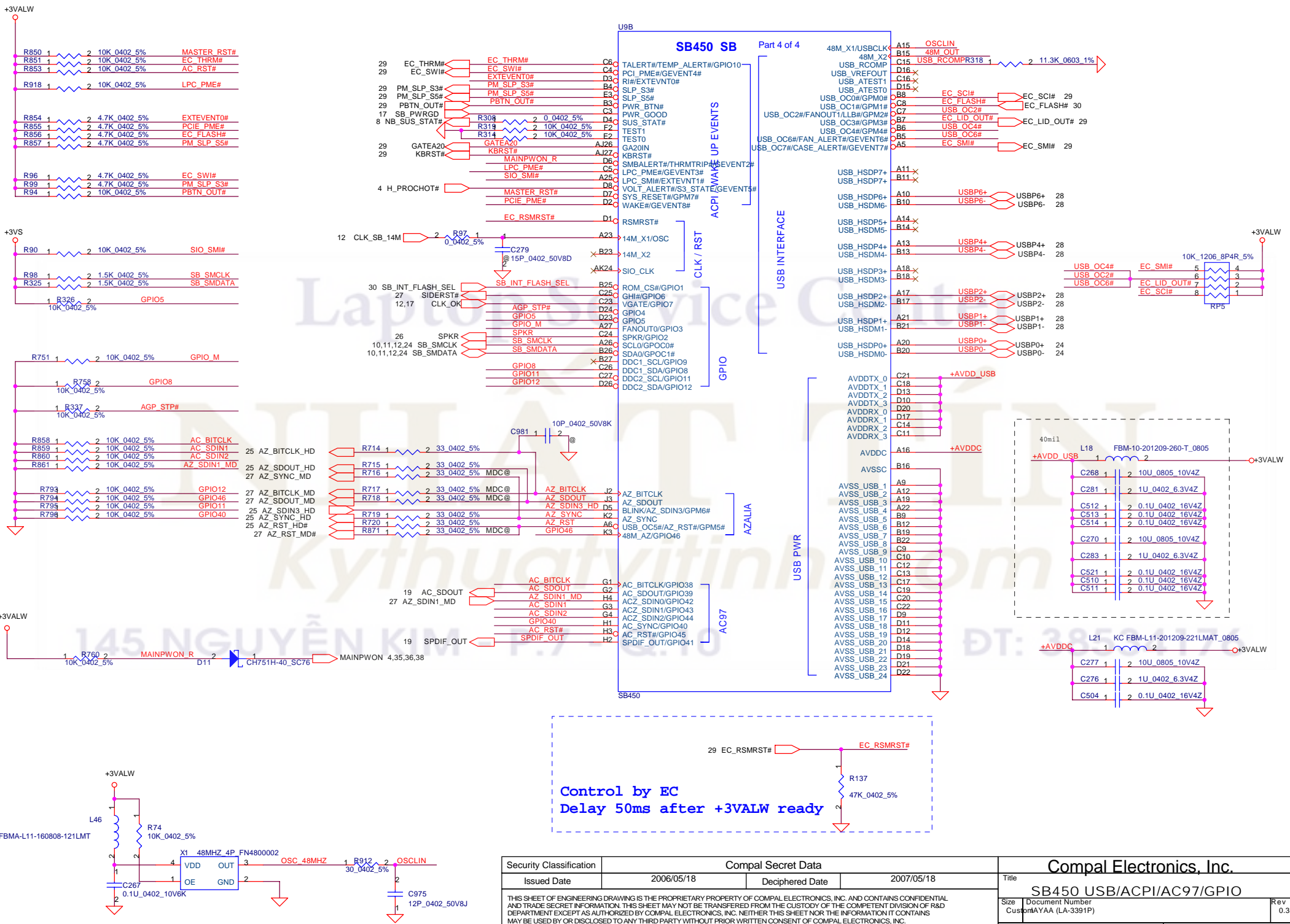


PA\_RS40X05 For C4 support

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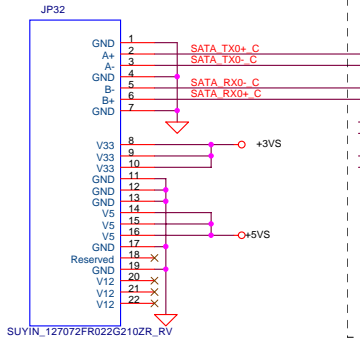
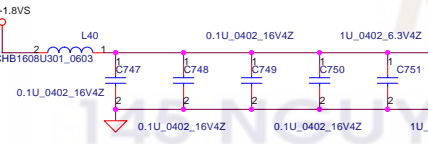
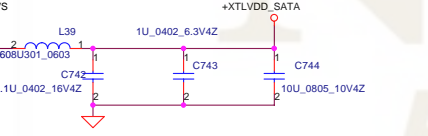
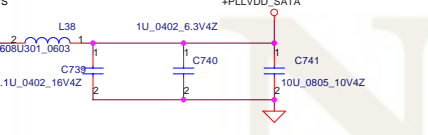
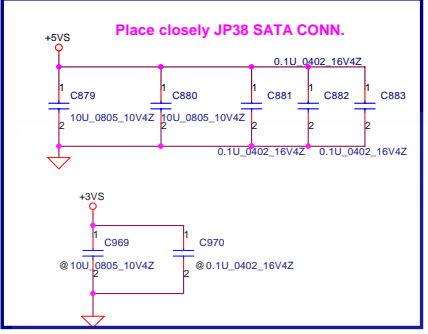
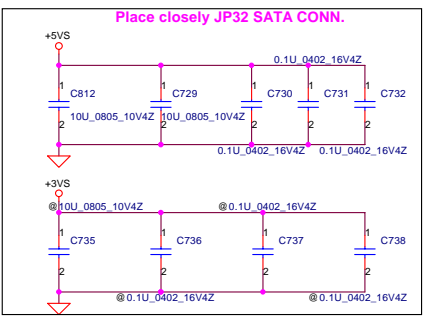
Compal Electronics, Inc.	
Title: PCI_EXP/LPC/RTC	
Size: Document Number IAYAA (LA-3391P)	Rev: 0.3
Date: Thursday, October 06, 2006	Sheet: 15 of 48



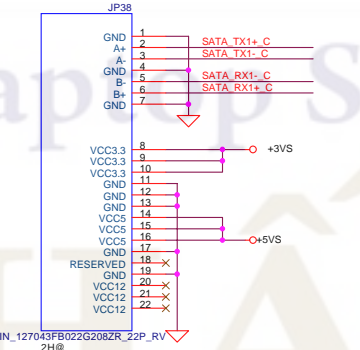
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Issued Date	2006/05/18	Deciphered Date	2007/05/18
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Compal Electronics, Inc.			
Title: SB450 USB/ACPI/AC97/GPIO			
Size	Document Number	Rev	
Customer	A1AA (LA-3391P)	0.3	
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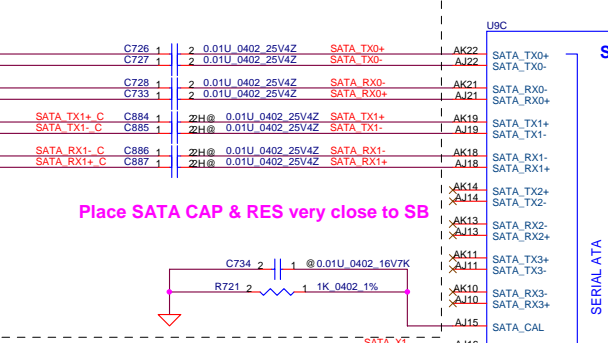




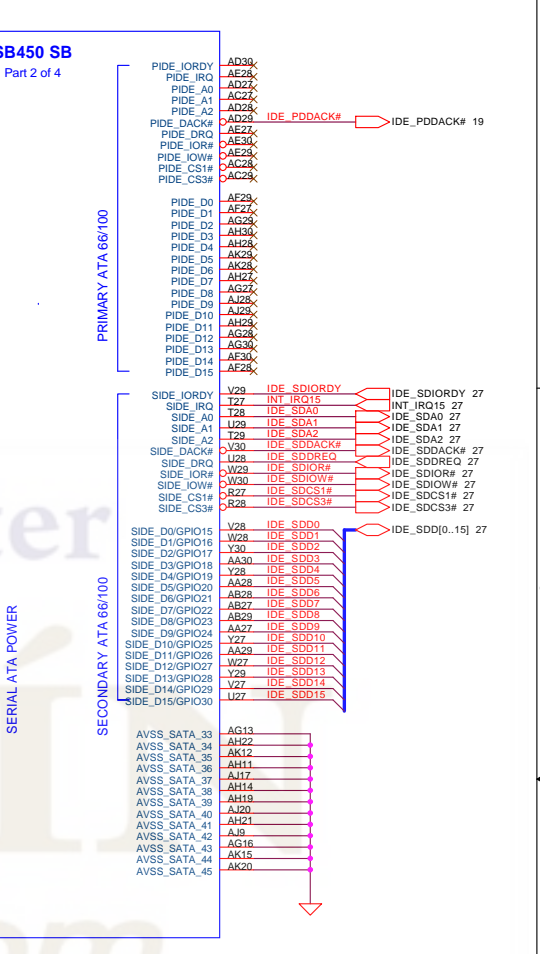
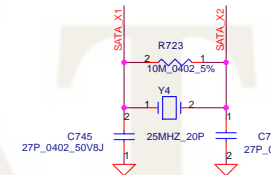
**SATA HDD CONNECTOR**



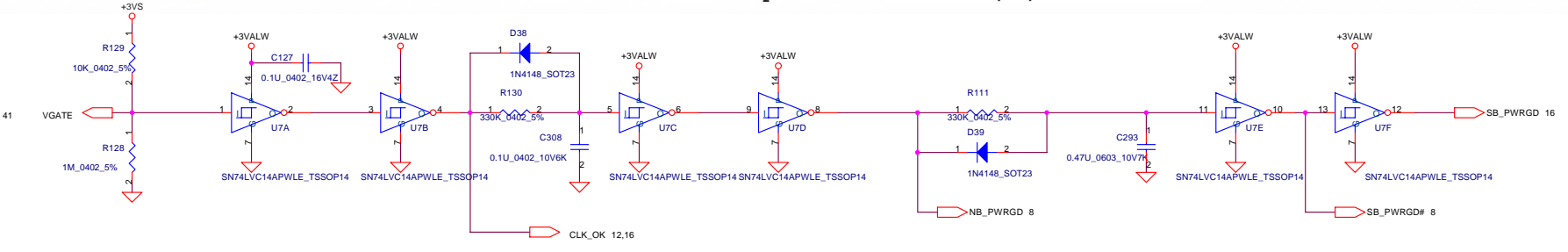
**SATA HDD CONNECTOR**

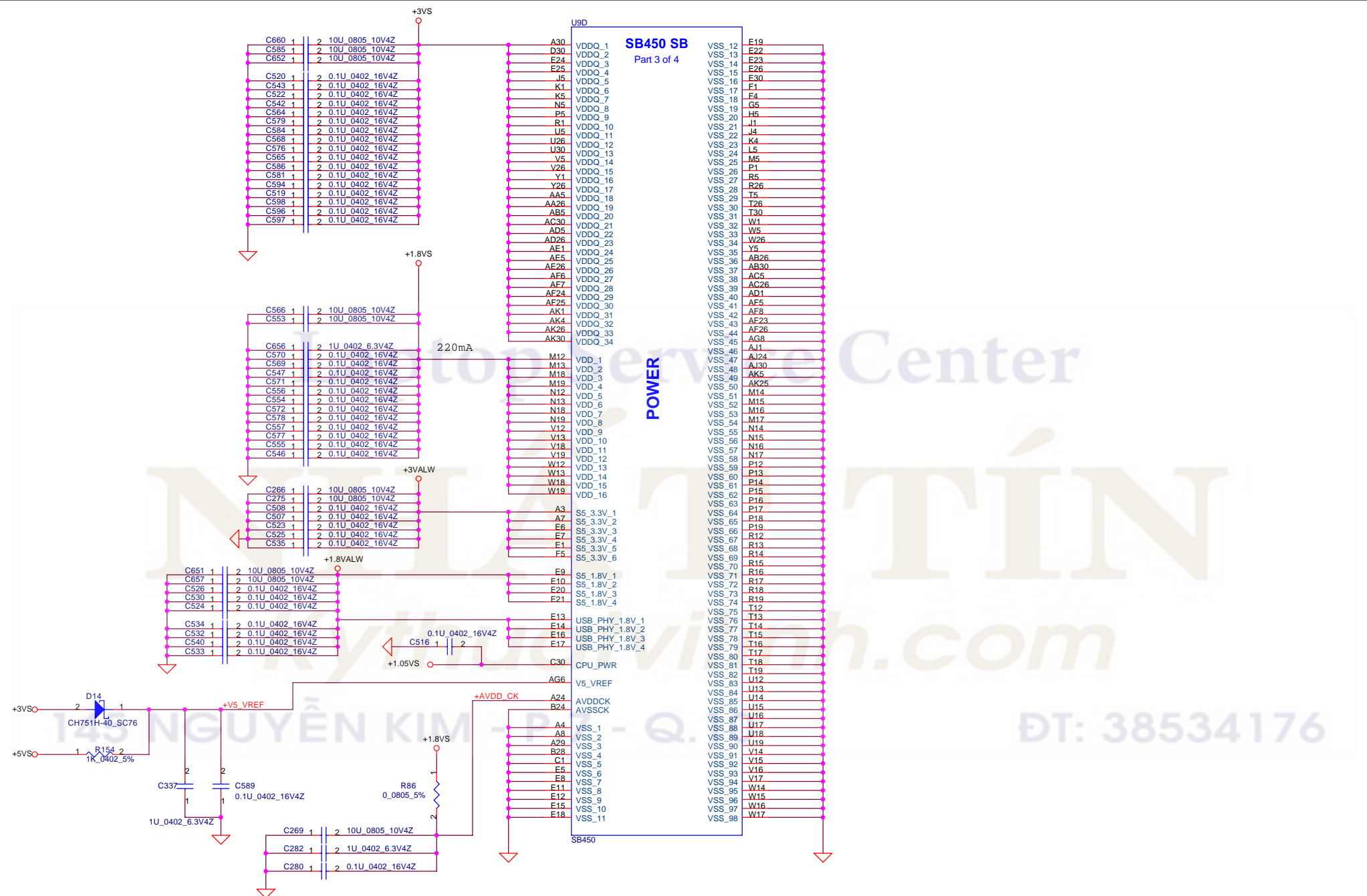


SATA Accessed	Port
Primary Master	Port 0
Primary Slave	Port 2
Secondary Master	Port 1
Secondary Slave	Port 3

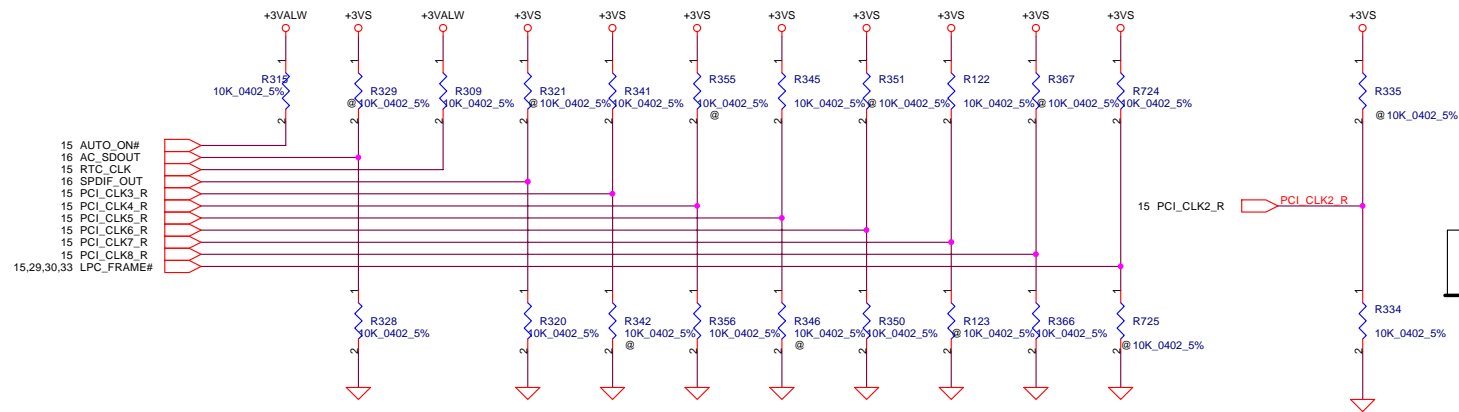


U7-->please close to SB450(U9)



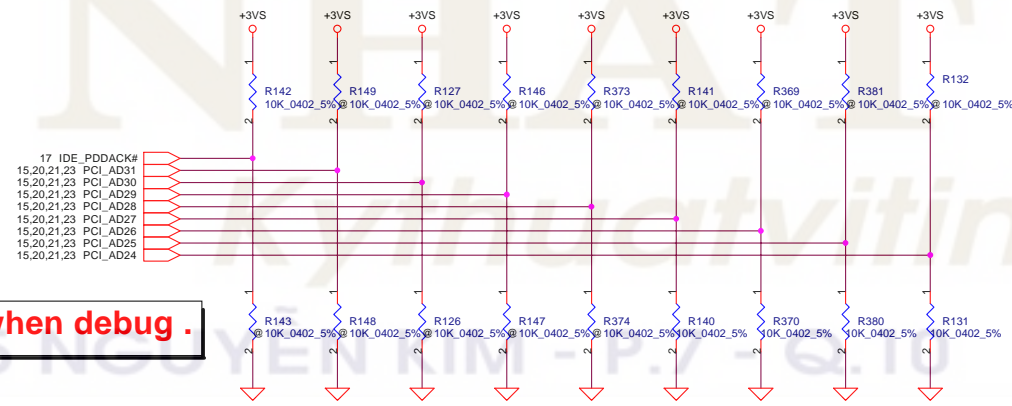


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	AUTO_ON#	AC97_SDOUT	RTC_CLK	SPDIF_OUT	CLK_PCI3	CLK_PCI_LAN	CLK_PCI_LPC	PCI_CLK6	PCI_CLK7	PCI_CLK8	PCI_CLK2_R	LFRAME#
<b>PULL HIGH</b>	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	USB PHY PWRDOWN DISABLE	Internal PLL	PCIE CM_SET low DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = LPC ROM I		Crystal Pad	THERMTIP# ENABLE
<b>PULL LOW</b>	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHZ DEFAULT	USB PHY PWRDOWN ENABLE DEFAULT	External Clock DEFAULT	PCIE CM_SET HIGH	CPU I/F = P4 DEFAULT	L,H = LPC ROM II L,L = FWH ROM		Clock input buffer DEFAULT	THERMTIP# DISENABLE

**REQUIRED STRAPS**



**Pop R634 when debug .**

**DEBUG STRAPS**

	DE_PDDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24
<b>PULL HIGH</b>	USE LONG RESET DEFAULT	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS
<b>PULL LOW</b>	USE SHORT RESET					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT

AD33 strapping  
No reserve longer

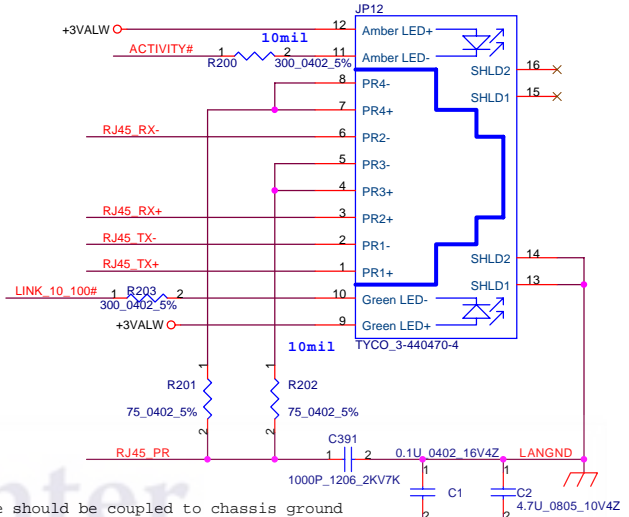
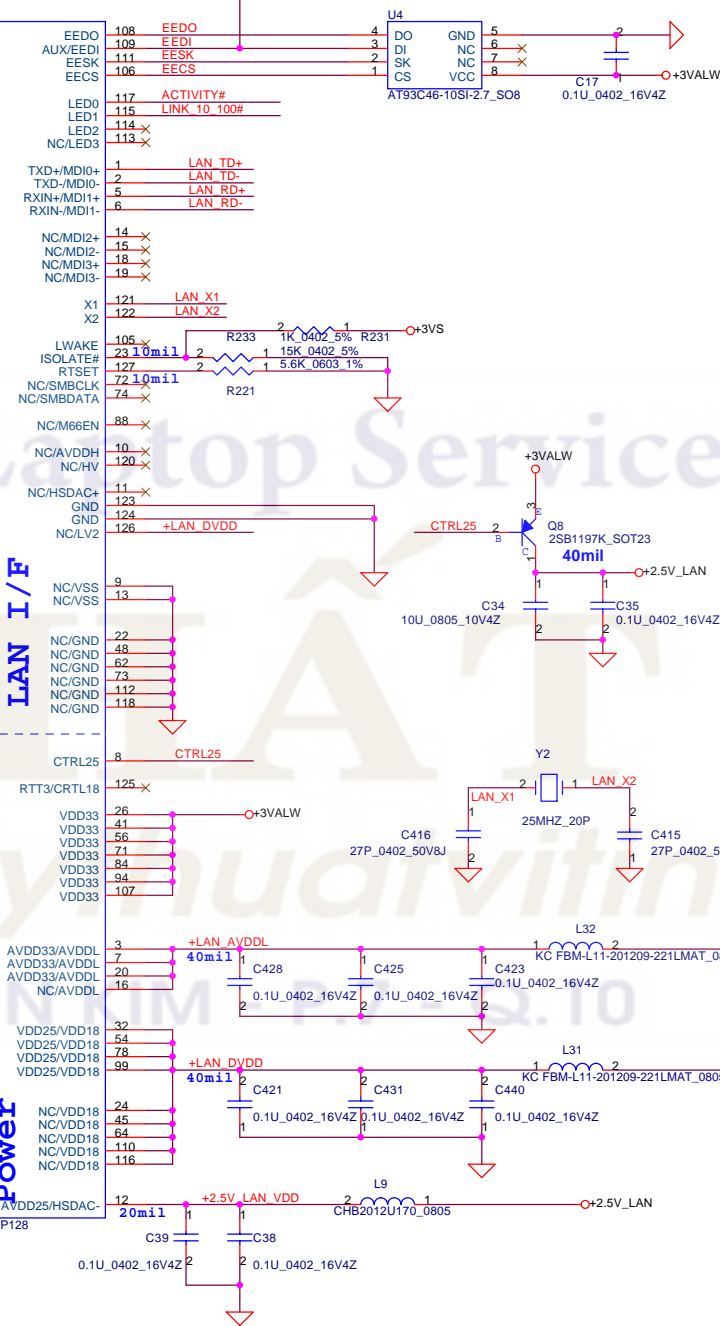
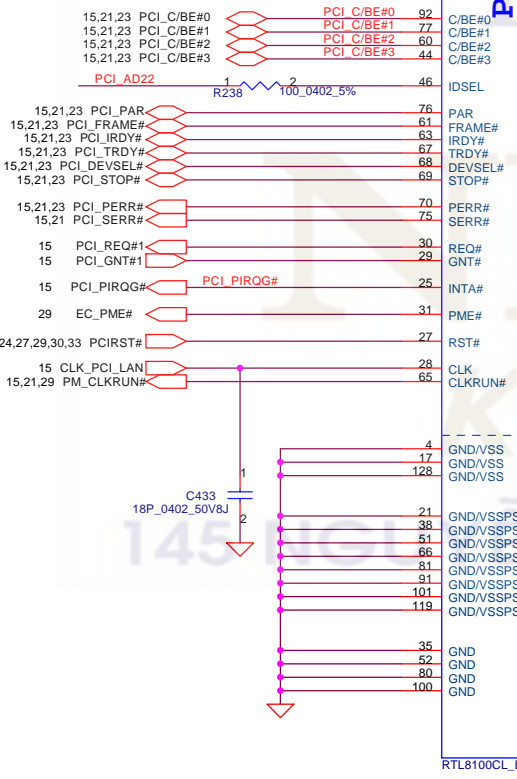
15,19,21,23 PCI\_AD[0..31] PCI\_AD[0..31]

PCI AD0	104	AD0
PCI AD1	103	AD1
PCI AD2	102	AD2
PCI AD3	98	AD3
PCI AD4	97	AD4
PCI AD5	96	AD5
PCI AD6	95	AD6
PCI AD7	93	AD7
PCI AD8	90	AD8
PCI AD9	89	AD9
PCI AD10	87	AD10
PCI AD11	86	AD11
PCI AD12	85	AD12
PCI AD13	83	AD13
PCI AD14	82	AD14
PCI AD15	79	AD15
PCI AD16	59	AD16
PCI AD17	58	AD17
PCI AD18	57	AD18
PCI AD19	55	AD19
PCI AD20	53	AD20
PCI AD21	50	AD21
PCI AD22	49	AD22
PCI AD23	47	AD23
PCI AD24	43	AD24
PCI AD25	42	AD25
PCI AD26	40	AD26
PCI AD27	39	AD27
PCI AD28	37	AD28
PCI AD29	36	AD29
PCI AD30	34	AD30
PCI AD31	33	AD31

PCI I/F

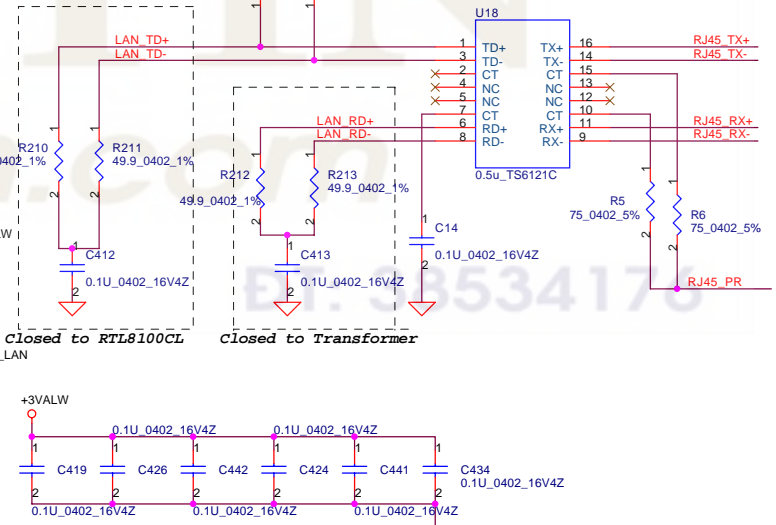
LAN I/F

Power



Termination plane should be coupled to chassis ground

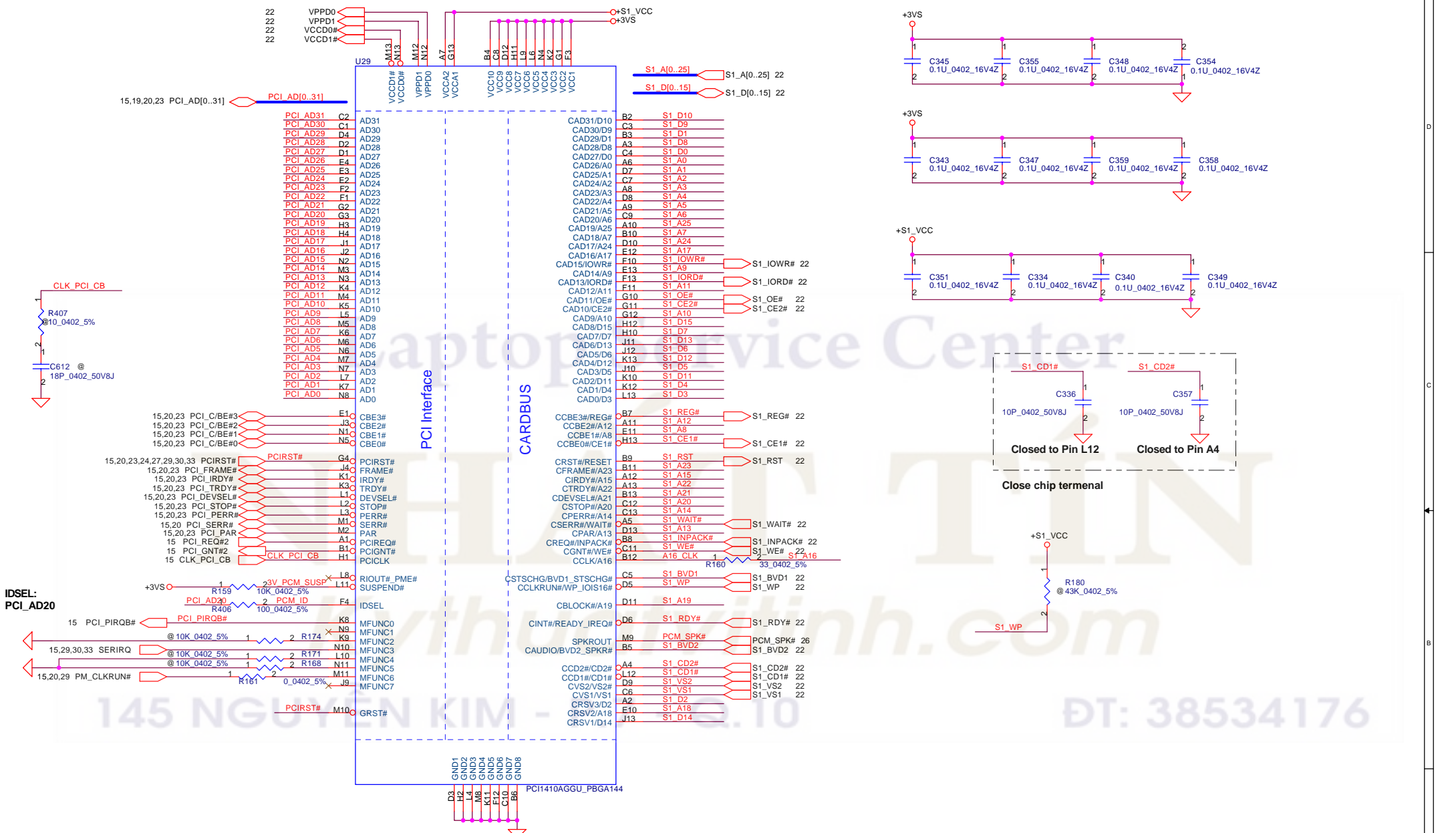
Layout Note  
TS6121 pls close to conn.



Closed to RTL8100CL

Closed to Transformer

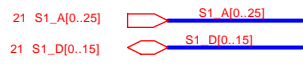
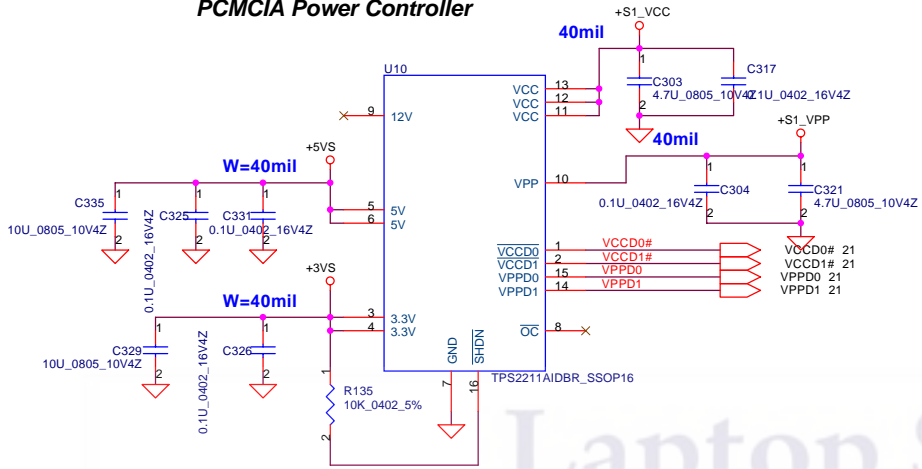
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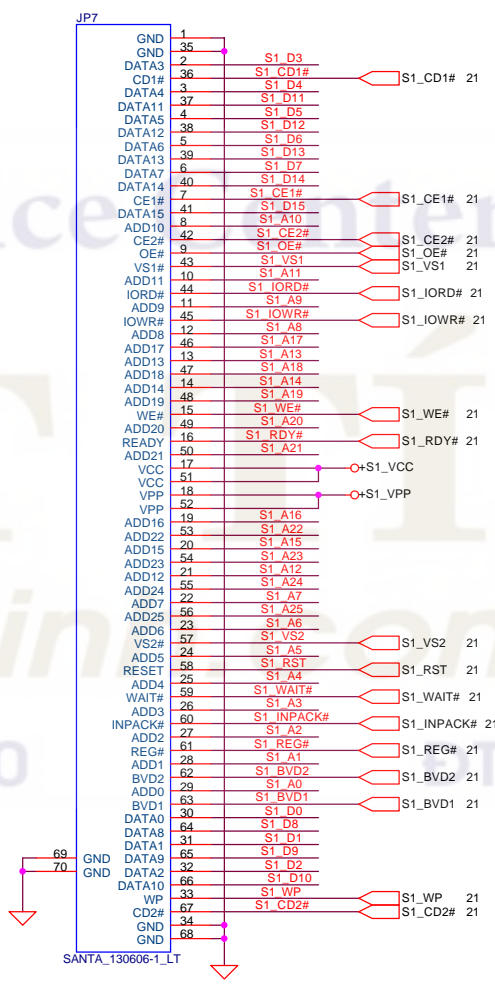
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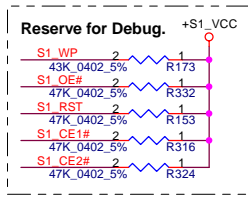
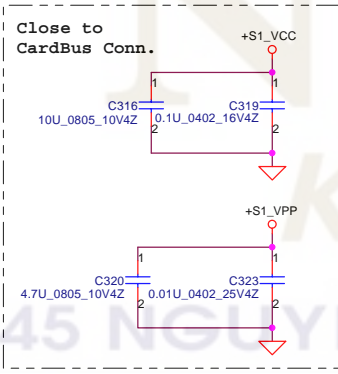
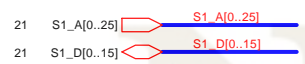
**PCMCIA Power Controller**



**CardBus Socket**

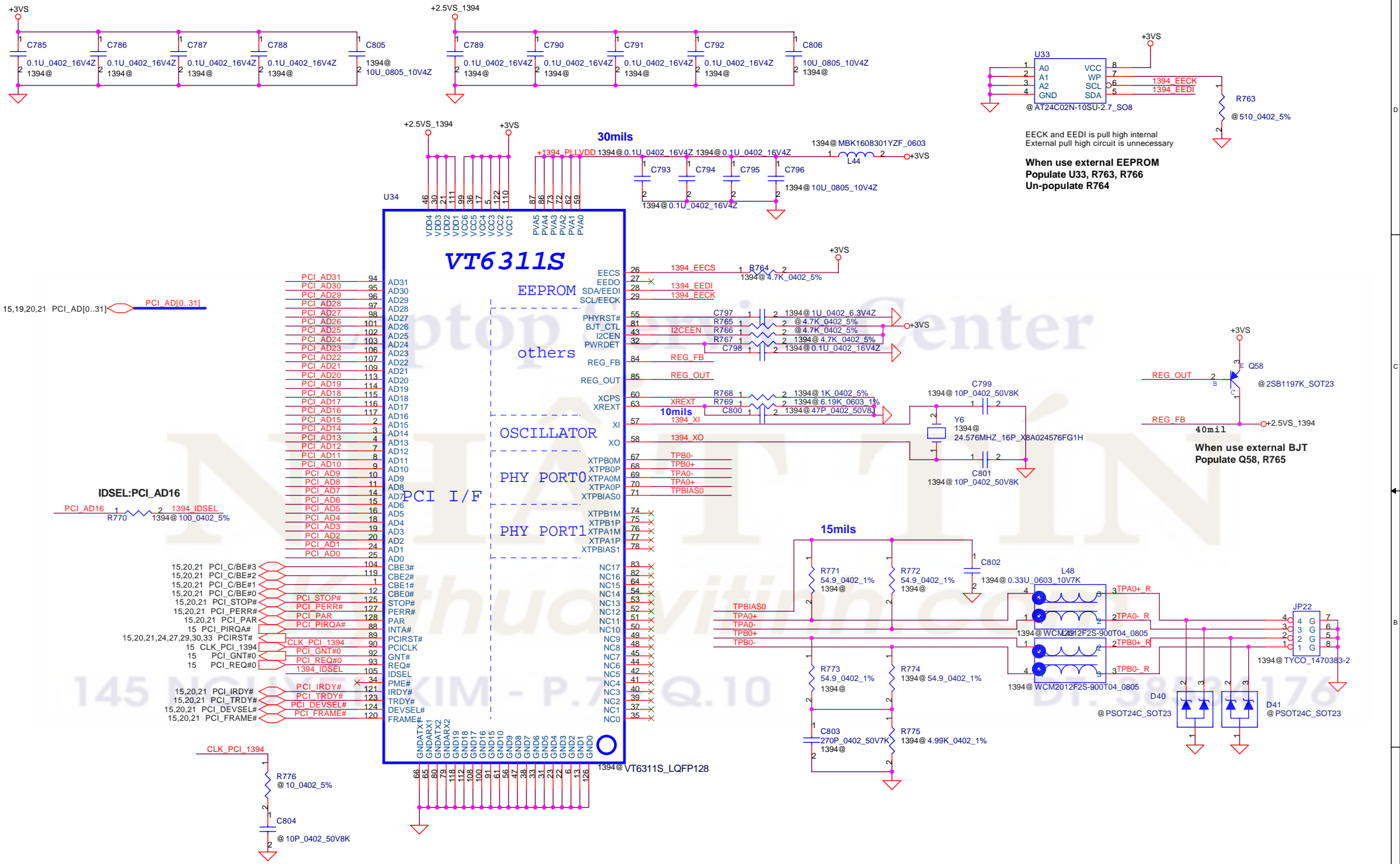


**CardBus Socket**



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 Kythuatviti.com  
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 Hotline: 38534176

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U33  
 1 A0 VCC  
 2 A1 WP  
 3 A2 SCL  
 4 GND SDA  
 5  
 6 1394 EECK  
 7 1394 EEDI

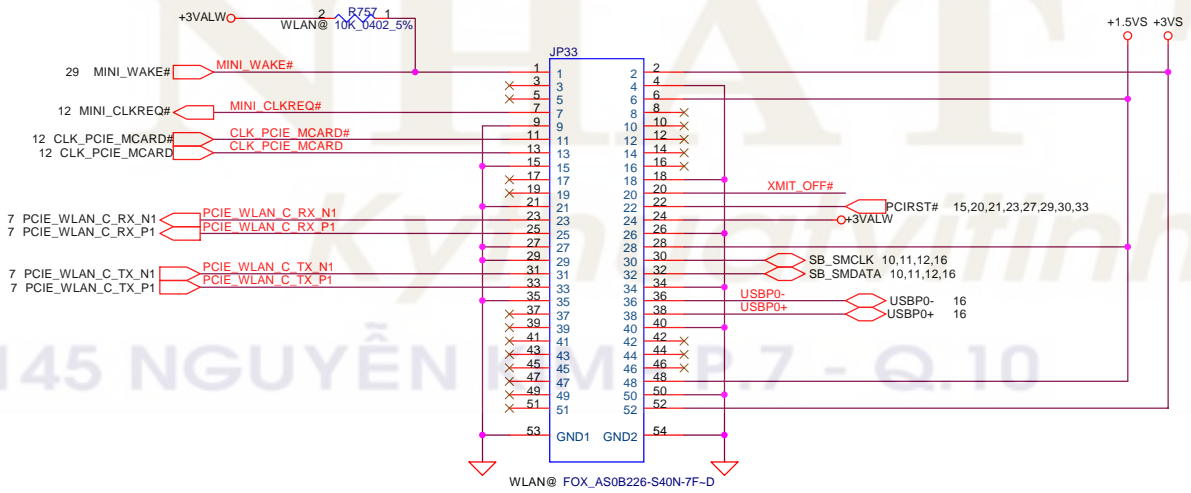
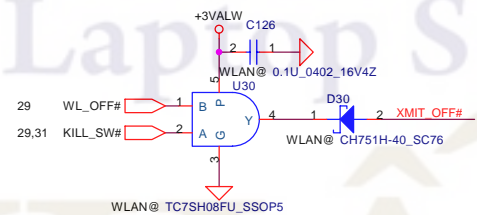
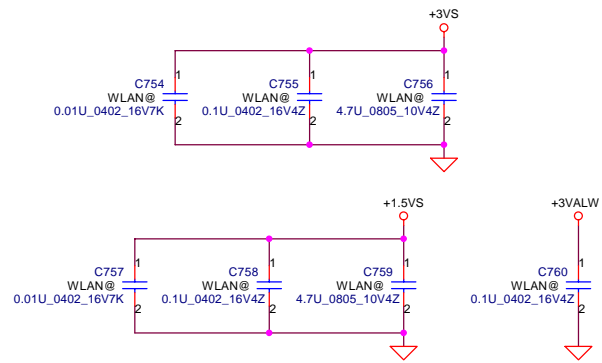
@ AT24C02N-10SU-2.7\_S08

EECK and EEDI is pull high internal  
 External pull high circuit is unnecessary

**When use external EEPROM  
 Populate U33, R763, R766  
 Un-populate R764**

**When use external BJT  
 Populate Q58, R765**

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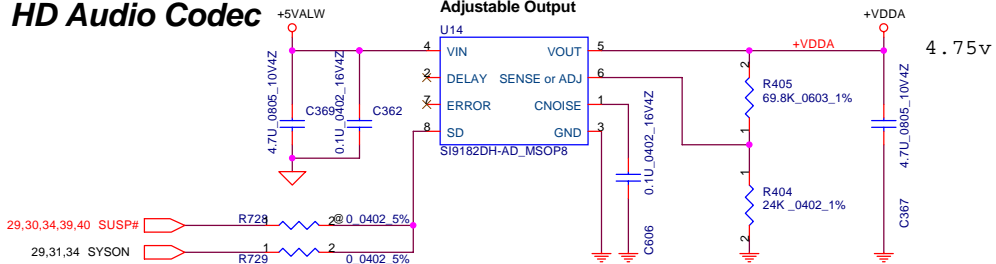
**Mini-Express Card**

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Size	Document Number		Rev	
B	IAYAA (LA-3391P)		0.3	
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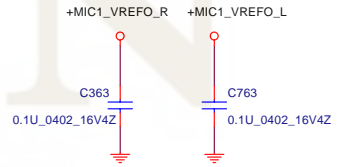
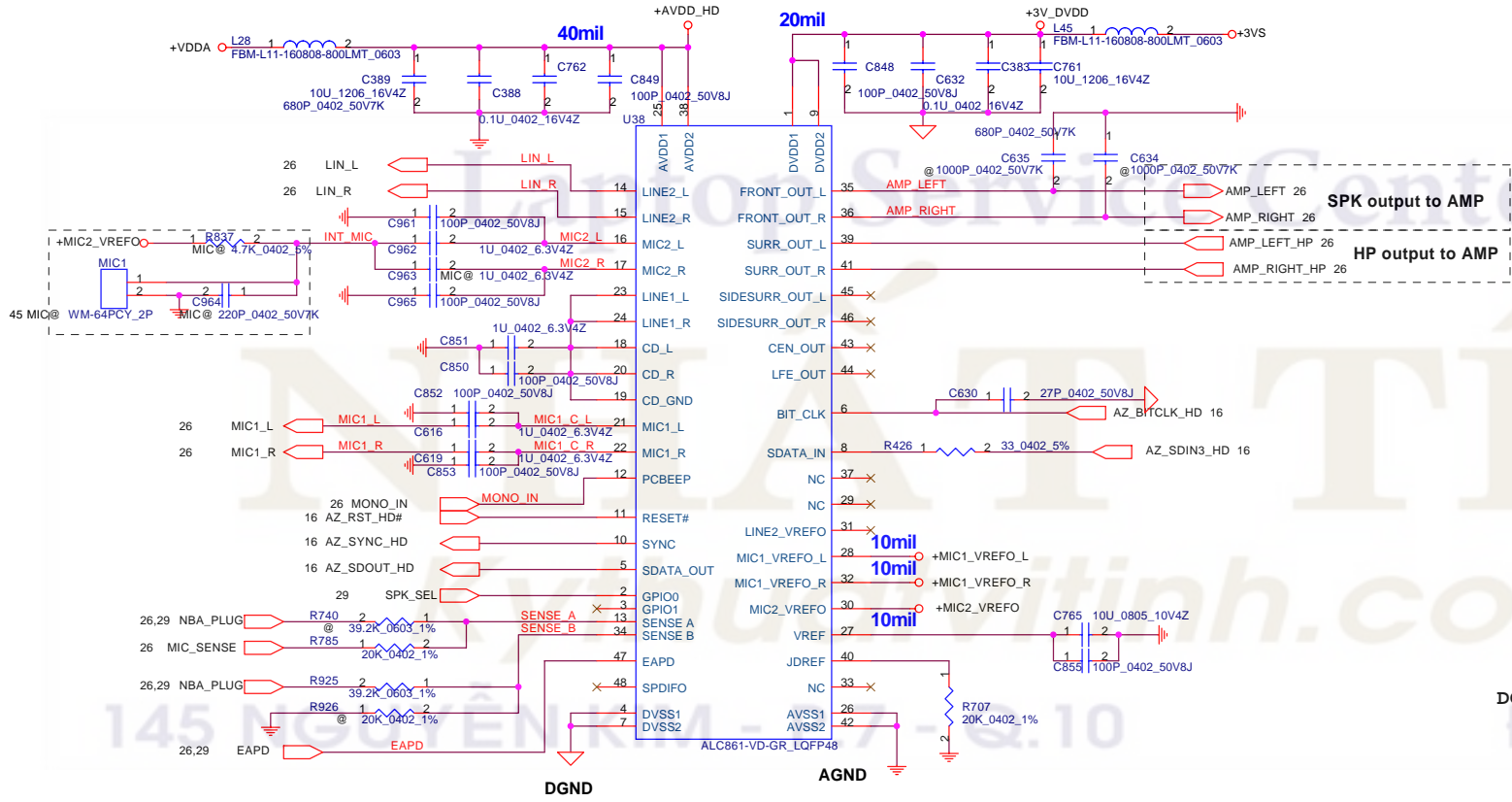


# HD Audio Codec

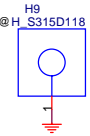
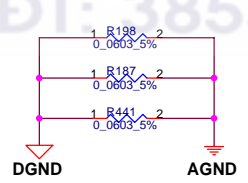
## Adjustable Output



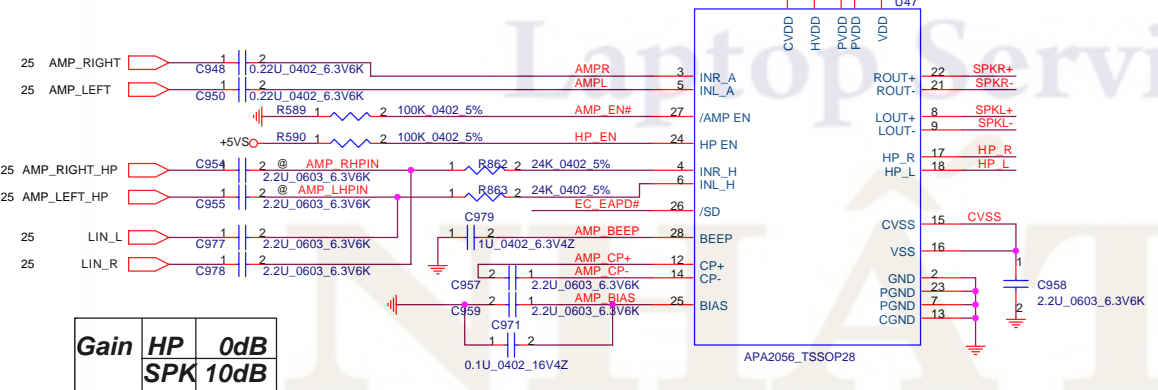
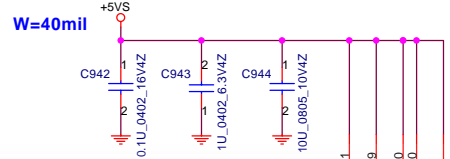
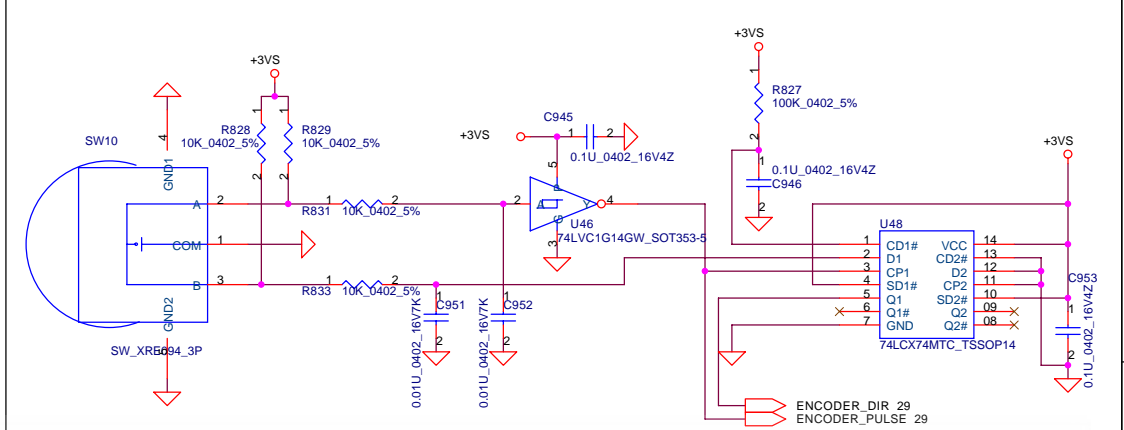
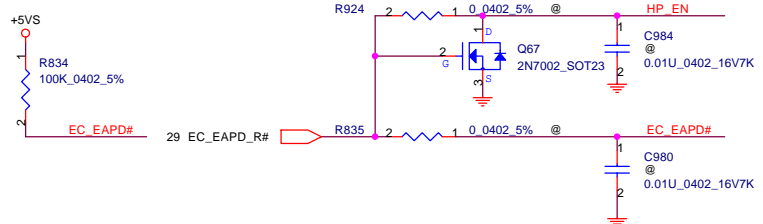
Sense Pin	Impedance	Codec Signals
SENSE A	39.2K	PORT-A (PIN 39, 41)
	20K	PORT-B (PIN 21, 22)
	10K	PORT-C (PIN 23, 24)
SENSE B	5.1K	PORT-D (PIN 35, 36)
	39.2K	PORT-E (PIN 14, 15)
	5.1K	PORT-H (PIN 45, 46)
	20K	PORT-F (PIN 16, 17)



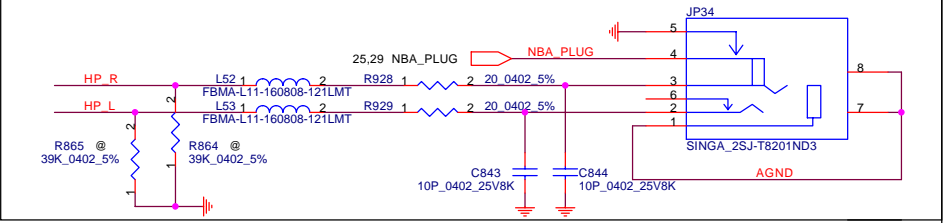
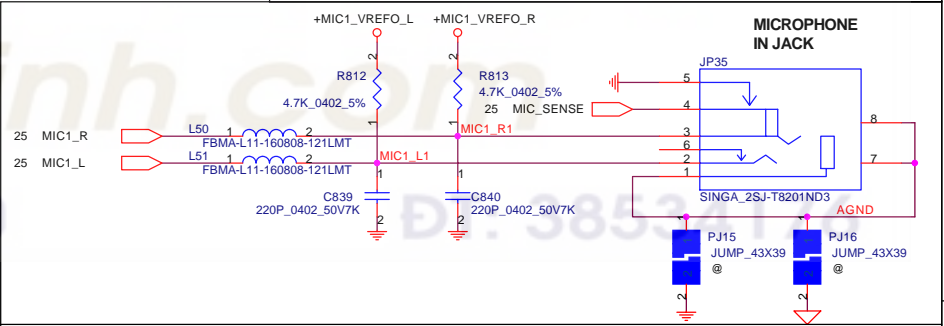
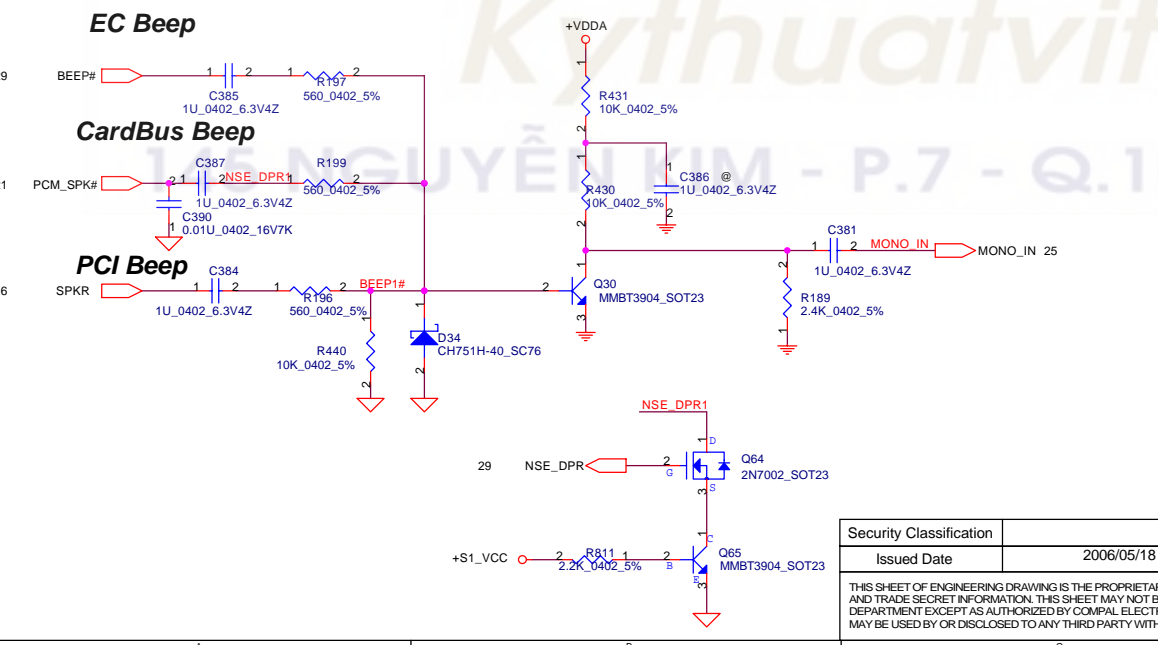
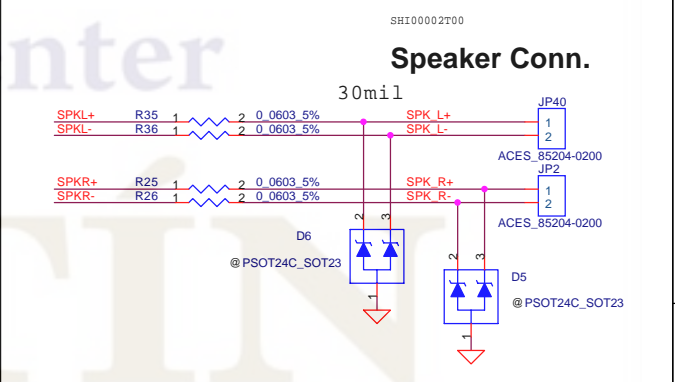
### DGND To AGND Bypass



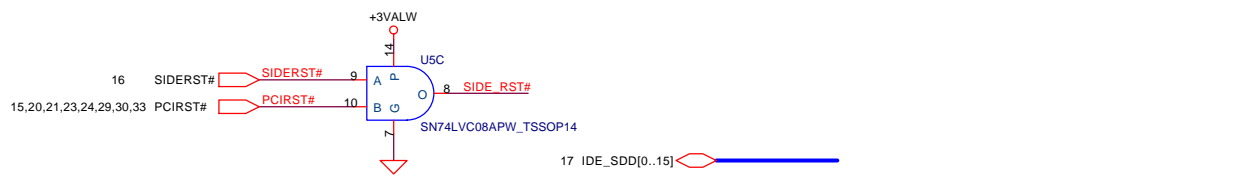
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Size	Document Number			Rev	
B	IAYAA (LA-3391P)			0.3	
Date:	Thursday, October 05, 2006	Sheet	25	of	48



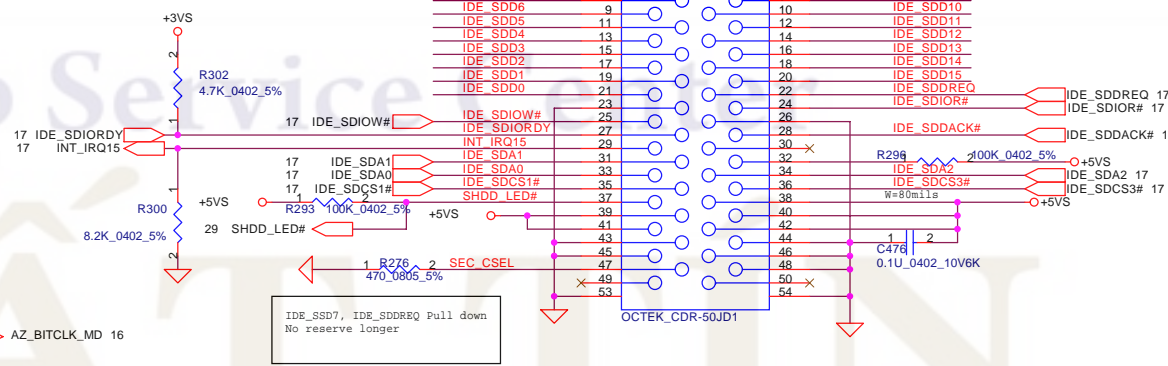
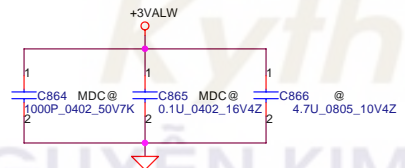
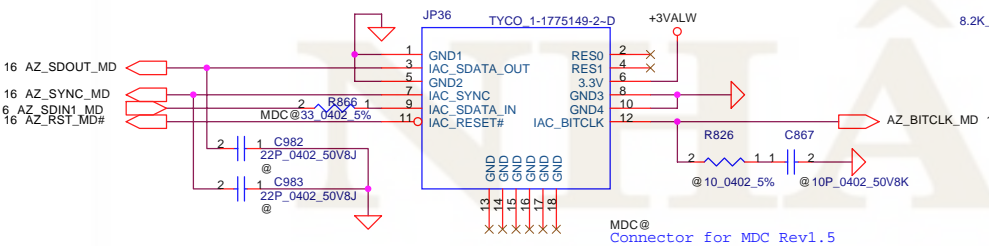
Gain	HP	0dB
	SPK	10dB



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Size	B	Document Number	IAYAA (LA-3391P)	Rev	0.3
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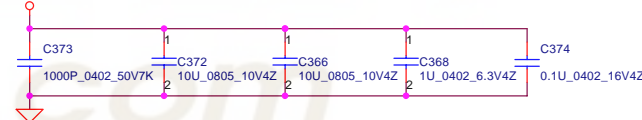


### MDC 1.5 Conn.



IDE\_SSD7, IDE\_SDDREQ Pull down  
No reserve longer

Place caps. near ODD CONN.

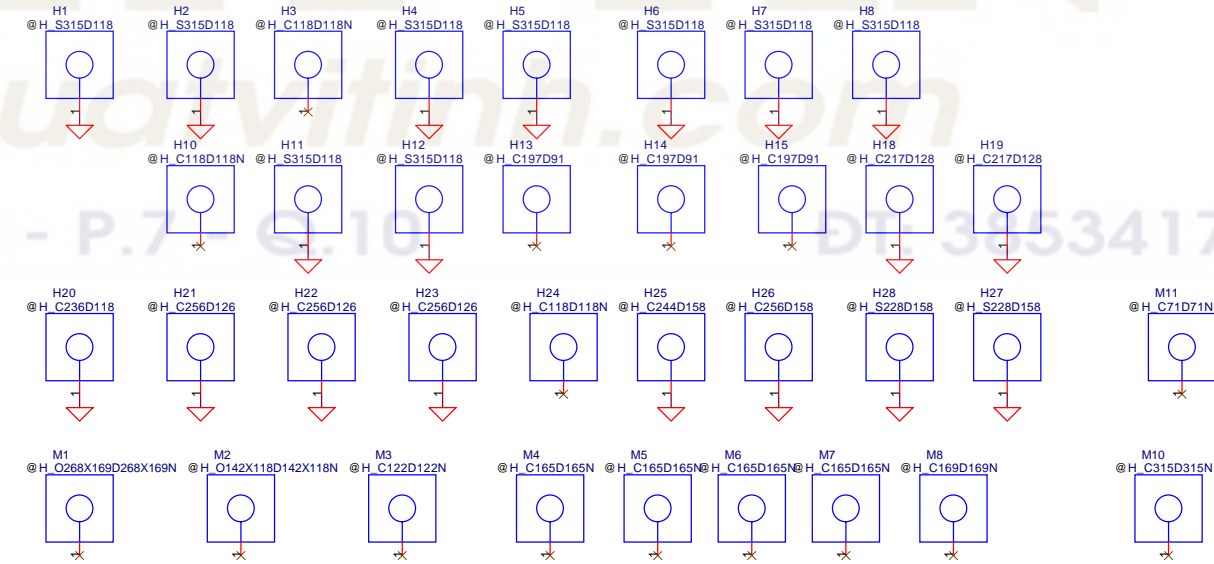
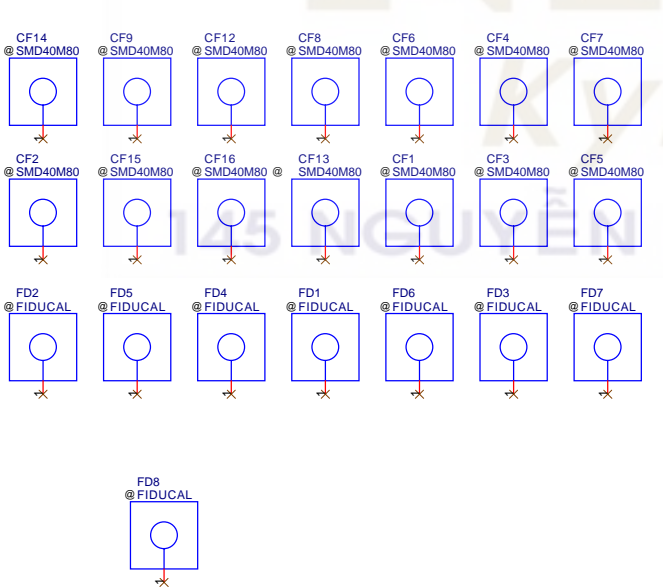
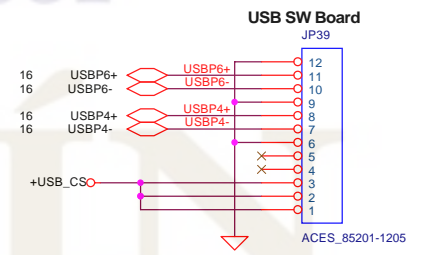
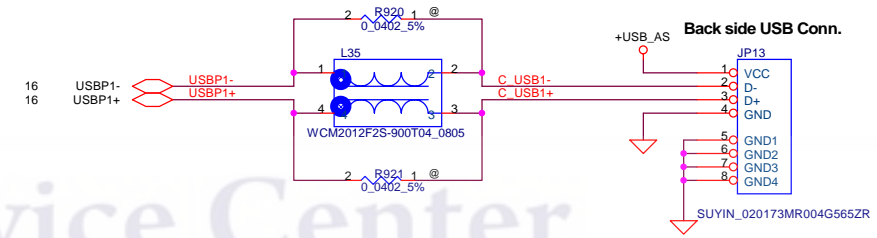
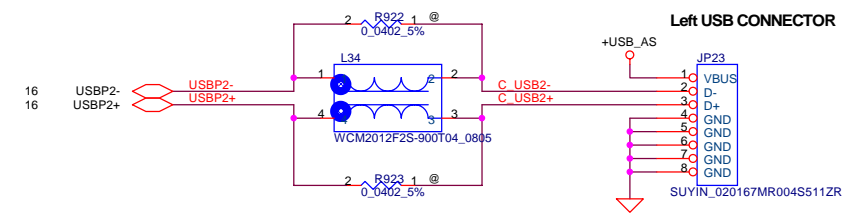
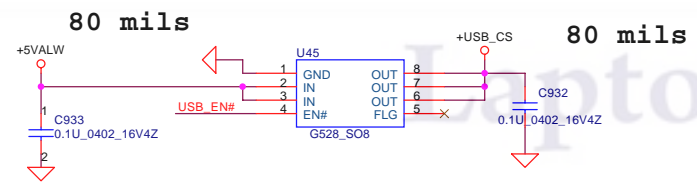
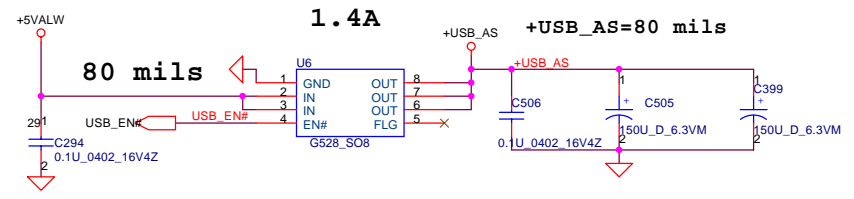


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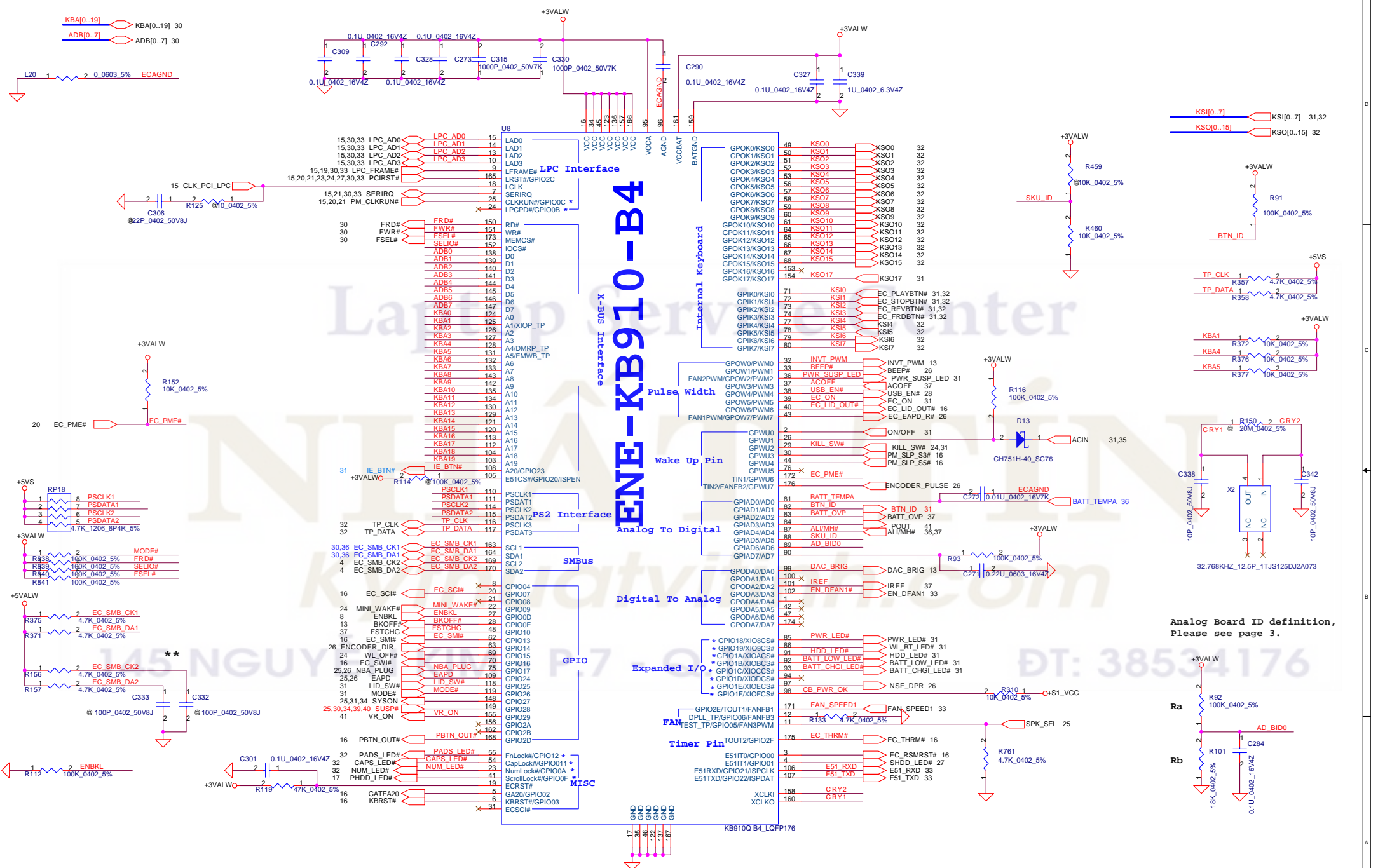
ĐT: 38534176

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Keep 20 mils minimum spacing between USB signals and others signals



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Size	B	Document Number	IAYAA (LA-3391P)	Rev
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# ENE-KB910-B4

X-BUS Interface

Internal keyboard

Pulse Width

Wake Up Pin

Analog To Digital

Digital To Analog

Expanded I/O

Timer Pin

MISC

KSI[0..7] 31,32  
KSO[0..15] 32

TP\_CLK 1 2  
TP\_DATA 1 2

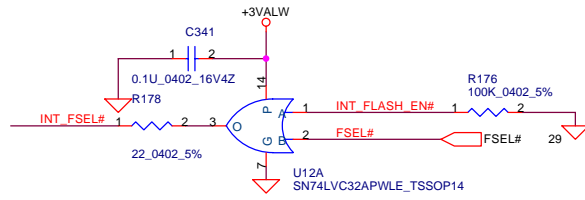
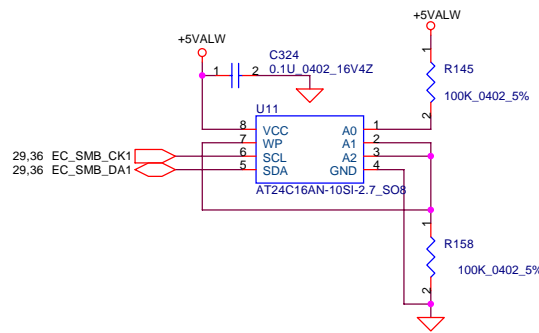
KBA1 1 2  
KBA4 1 2  
KBA5 1 2

CRY1 1 2  
CRY2 1 2

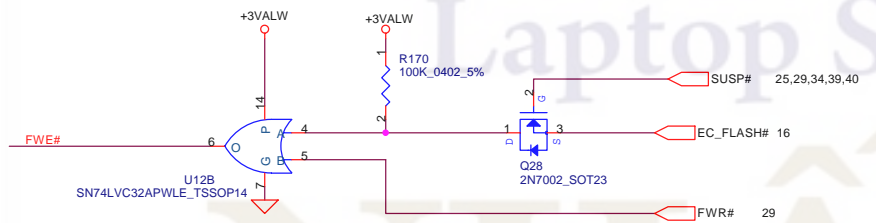
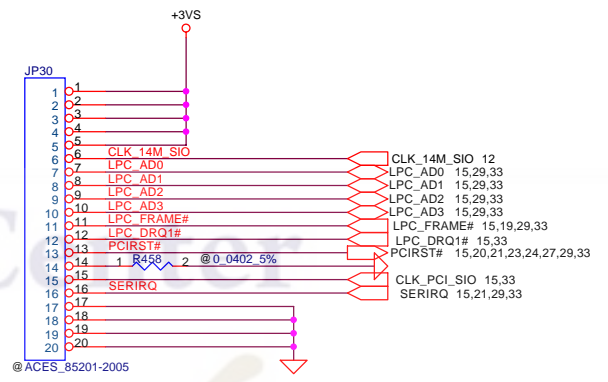
Analog Board ID definition,  
Please see page 3.

Ra 1 2  
Rb 1 2

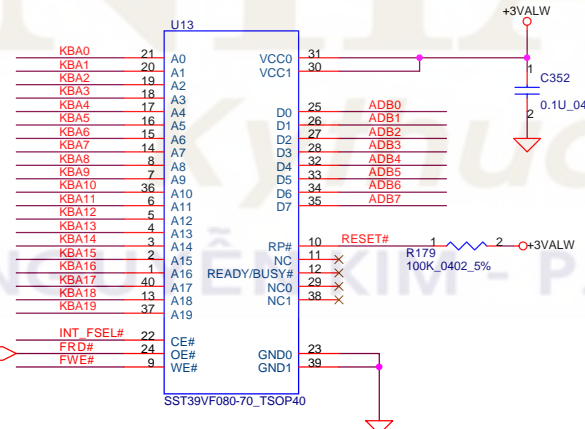
Security Classification	Compal Secret Data		Date
Issued Date	2006/05/18	Deciphered Date	2007/05/18
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Title			ENE-KB910
Size			Document Number
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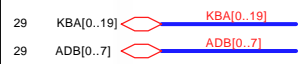
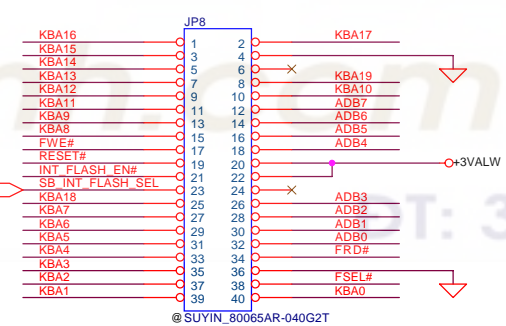
### LPC Debug Port



### 1MB Flash ROM

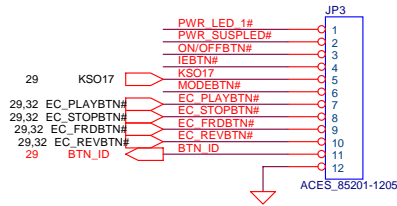


### 1MB ROM Socket



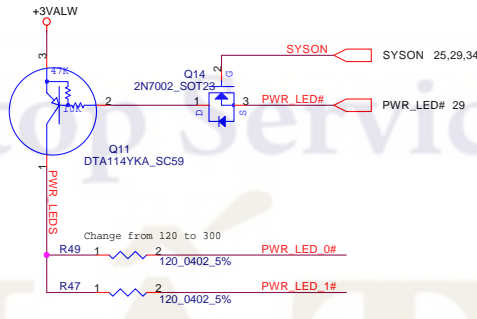
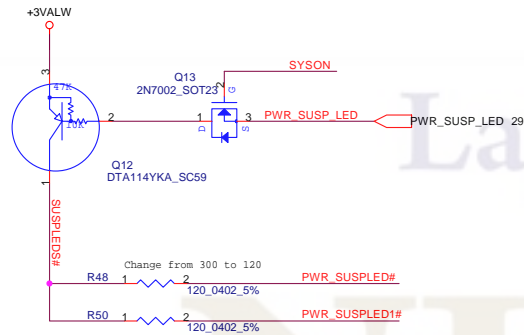
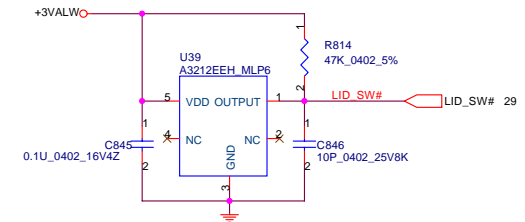
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Size B	Document Number IAYAA (LA-3391P)			Rev 0.3
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# Switch Board Conn.

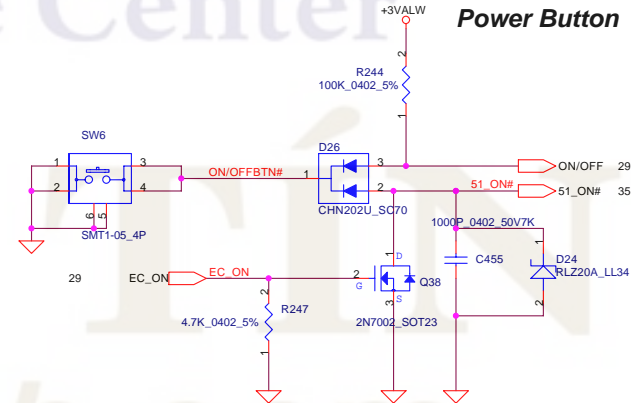


KSO17				C178	1	2	220P_0402_50V7K	C178	1	2	220P_0402_50V7K	
ON/OFFBTN#	C173	1	2	220P_0402_50V7K	C181	1	2	220P_0402_50V7K	C181	1	2	220P_0402_50V7K
PWR_LED_1#												
PWR_SUSP_LED#	C179	1	2	220P_0402_50V7K	C169	1	2	220P_0402_50V7K	C169	1	2	220P_0402_50V7K
IEBTN#												
MODEBTN#	C168	1	2	220P_0402_50V7K	C146	1	2	220P_0402_50V7K	C146	1	2	220P_0402_50V7K
EC_PLAYBTN#												
EC_STOPBTN#												
EC_FRDBTN#	C153	1	2	220P_0402_50V7K	C167	1	2	220P_0402_50V7K	C167	1	2	220P_0402_50V7K
EC_REVBTN#												
EC_PLAYBTN#												
EC_STOPBTN#	C160	1	2	220P_0402_50V7K								

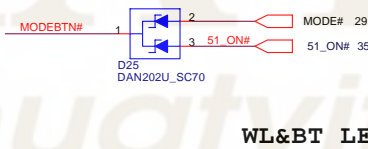
## LID Switch



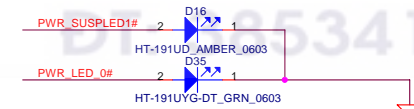
## Power Button



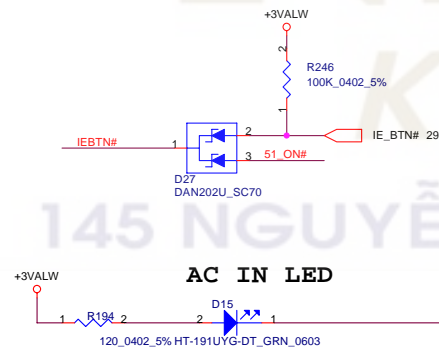
## WL&BT LED



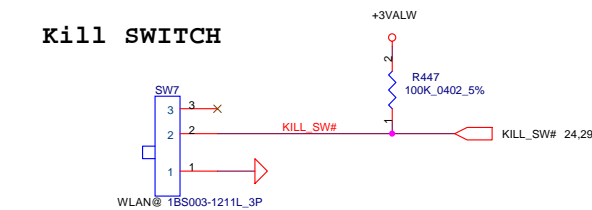
## POWER/ON LED



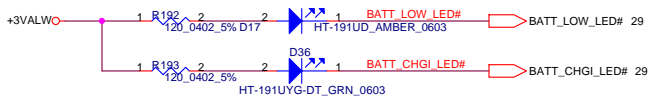
## AC IN LED



## Kill SWITCH



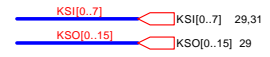
## BATTERY CHG



## HDD LED

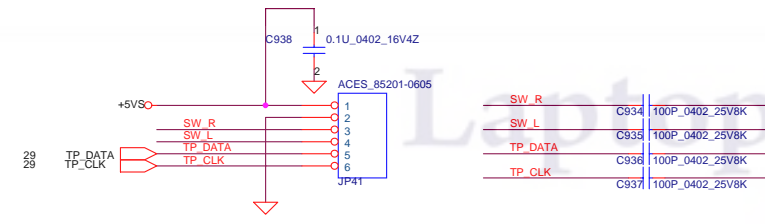


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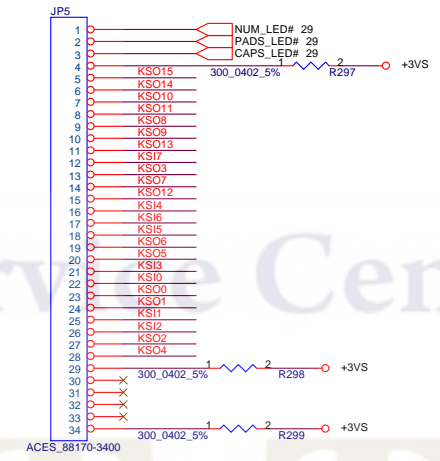
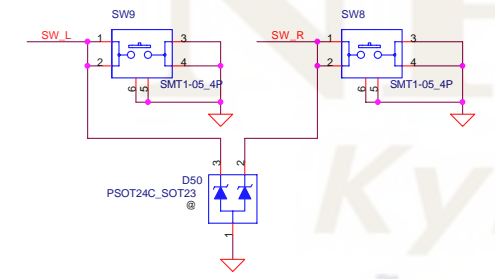


### INT\_KBD CONN.

### TP Conn.



### T/P Button

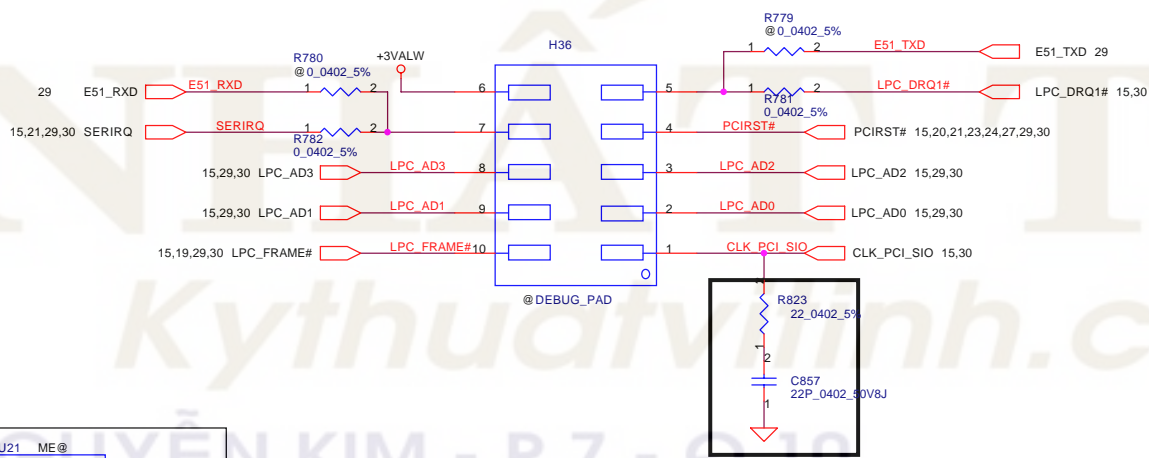
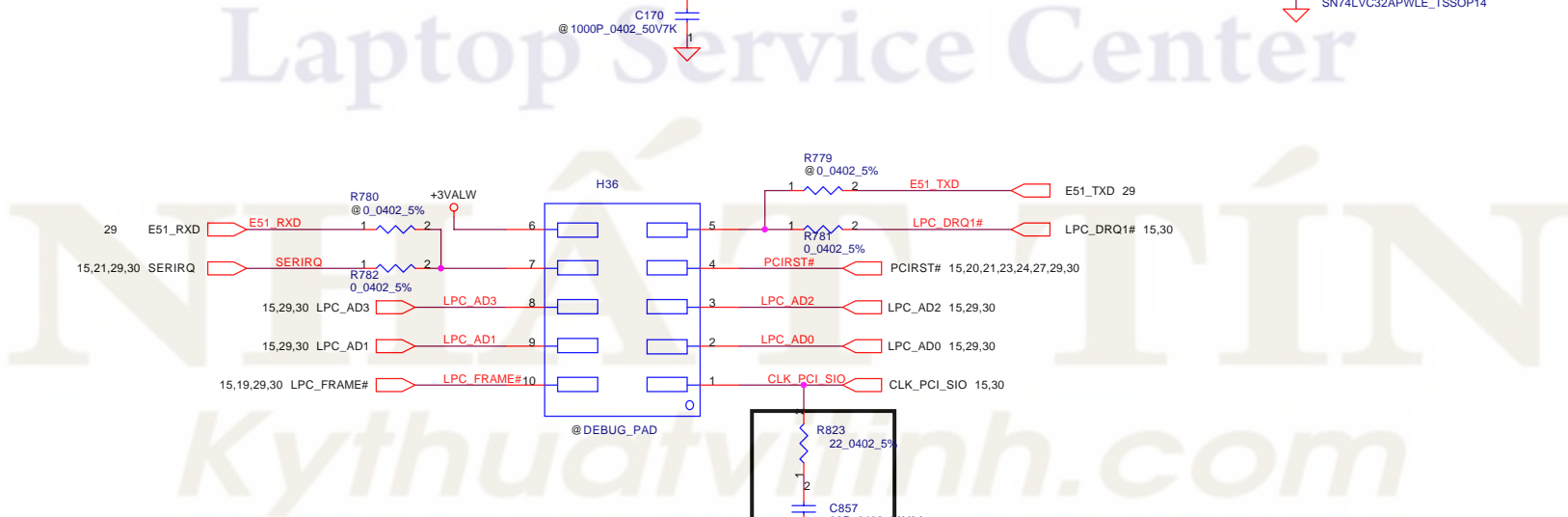
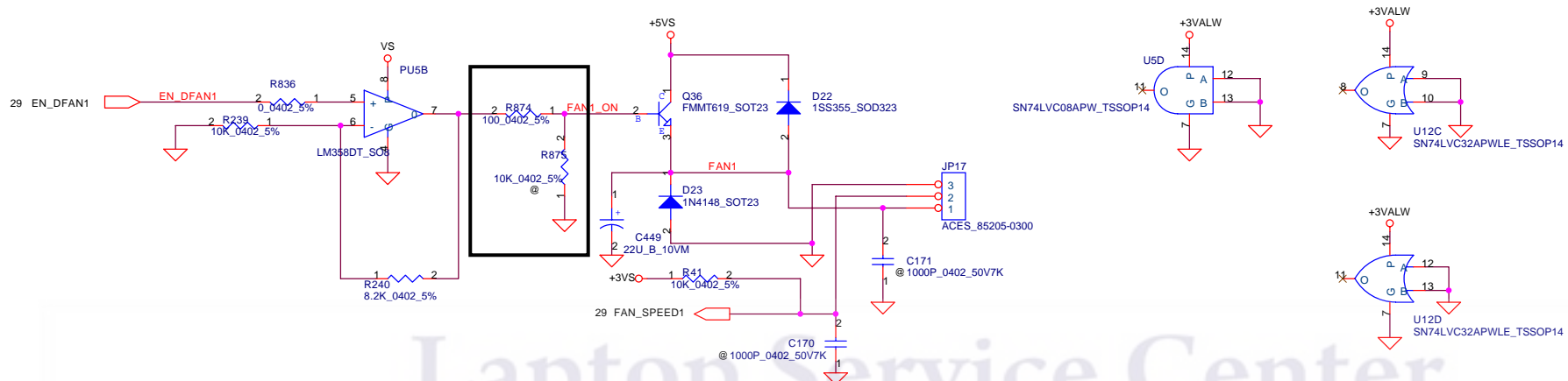


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Size	Document Number	Date		Rev	0.3
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# FAN Conn



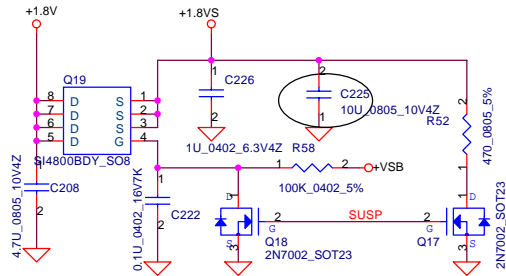
LPC Debug card

## BOM

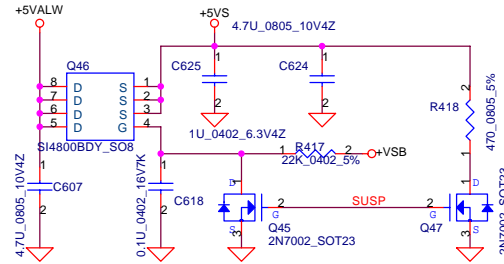
ZZZ1	PJP1 45@	U21 ME@
PCB ZHH LA-3391P REV0 M/B	DCJACK-MB	216ECP4ALA13FG-RC410ME

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Date:	Thursday, October 05, 2006	Sheet	33 of 48	Rev	0.3

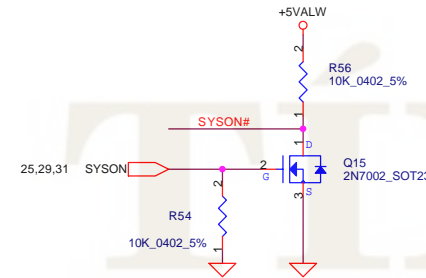
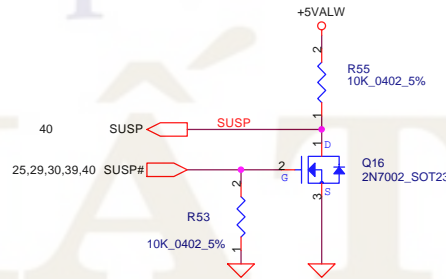
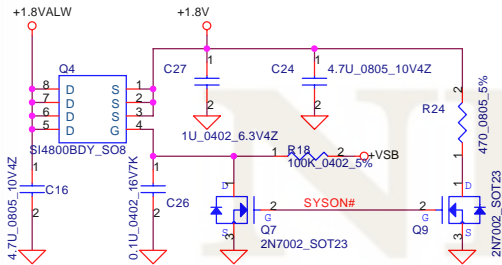
**+1.8V TO +1.8VS**



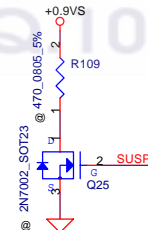
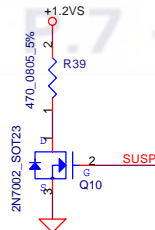
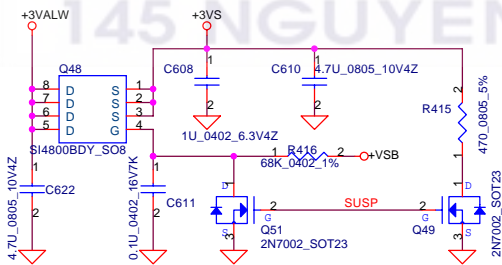
**+5VALW TO +5VS**



**+1.8VALW TO +1.8V**



**+3VALW TO +3VS**



Laptop Service Center

KHÁNH AN

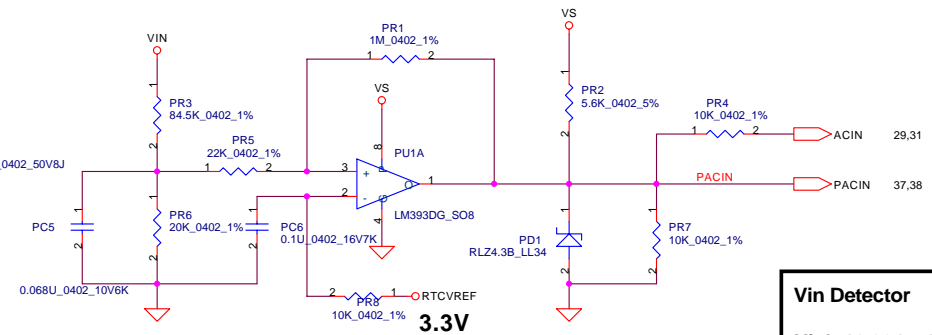
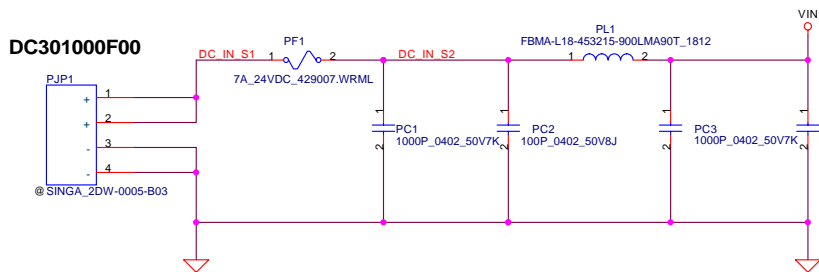
Kythuatvitinh.com

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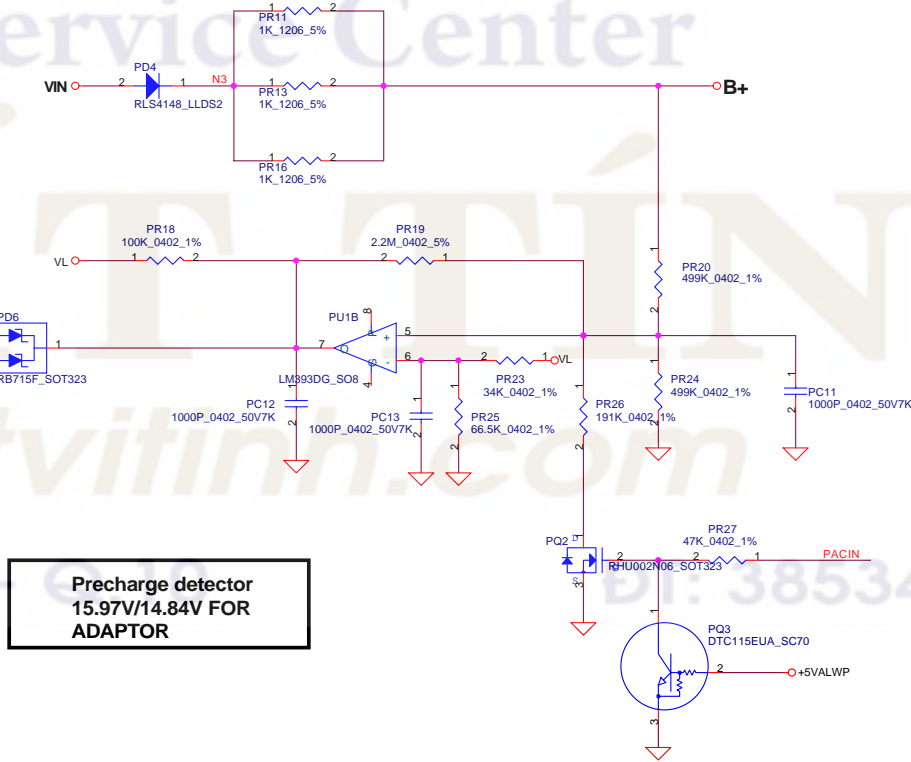
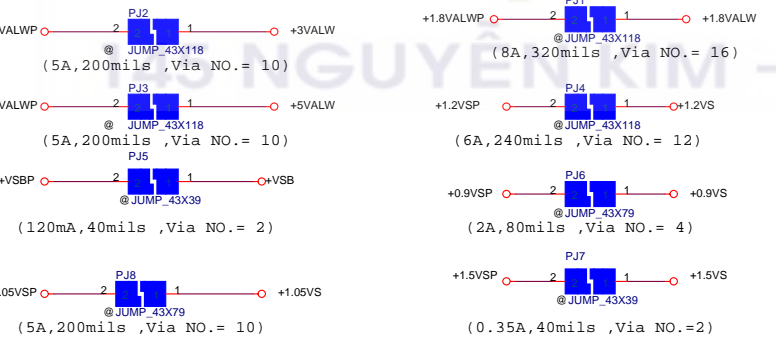
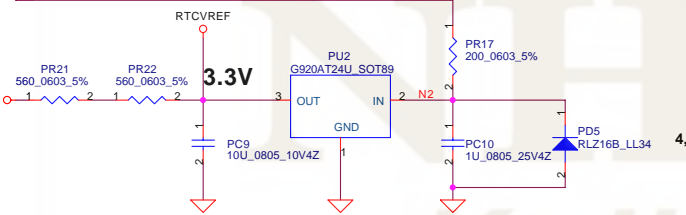
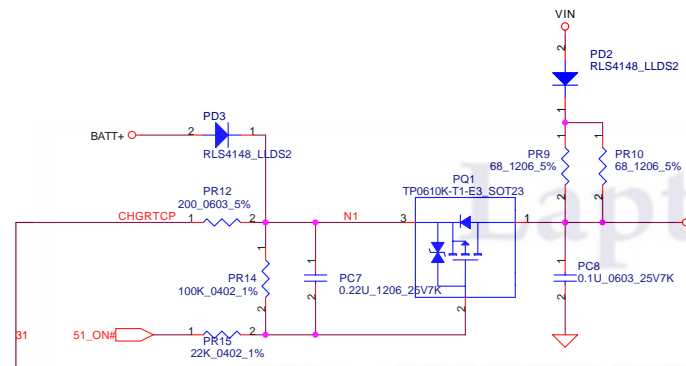
ĐT: 38534176

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				DC-DC INTERFACE	
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**DC301000F00**



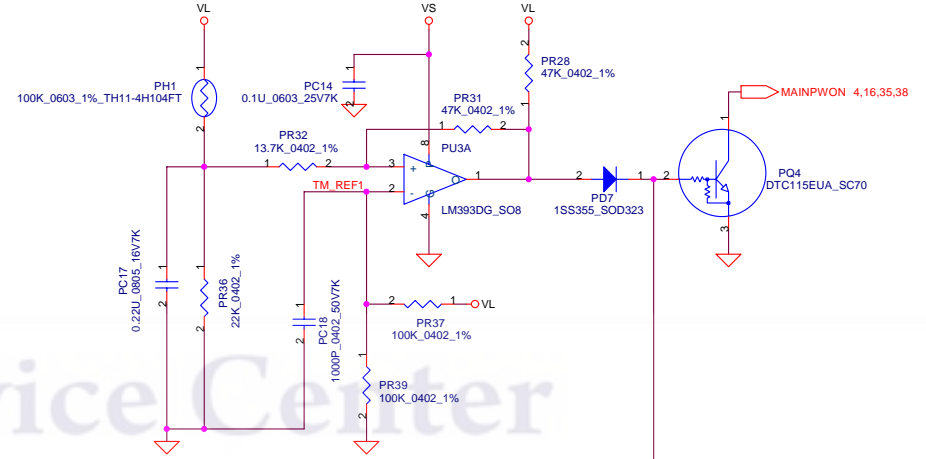
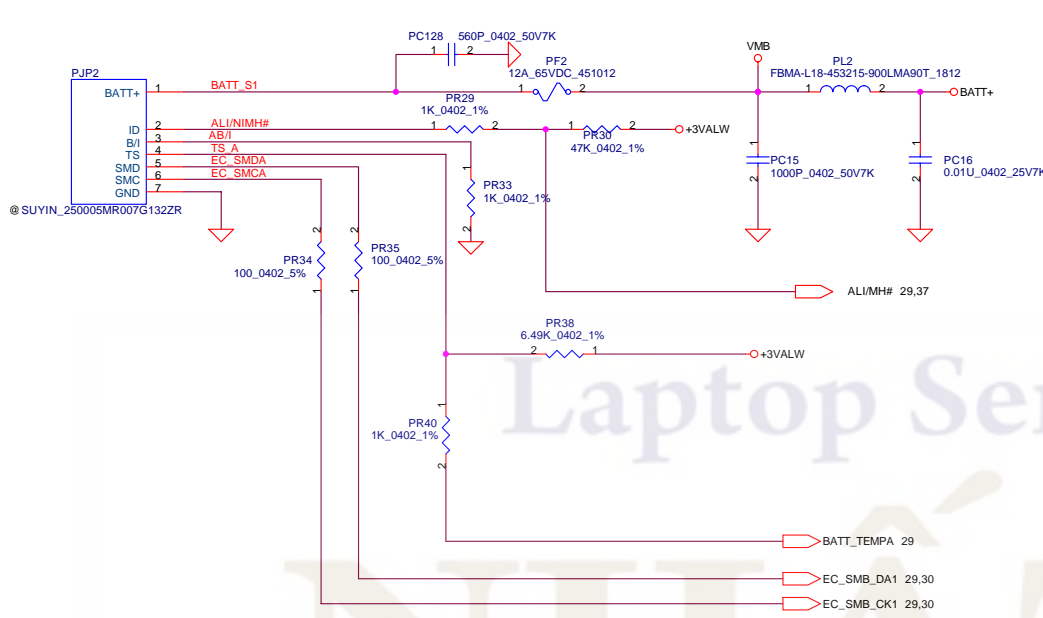
**Vin Detector**  
 High 18.384 17.901 17.430  
 Low 17.728 17.257 16.976



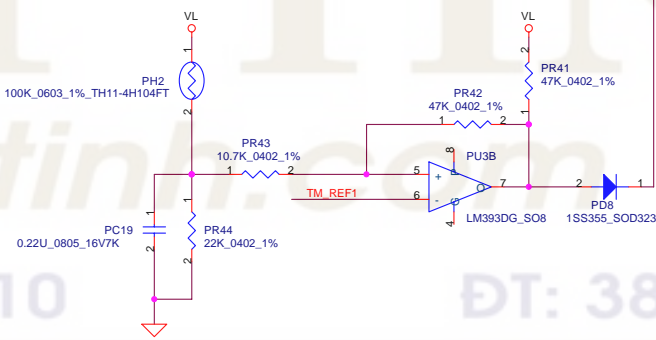
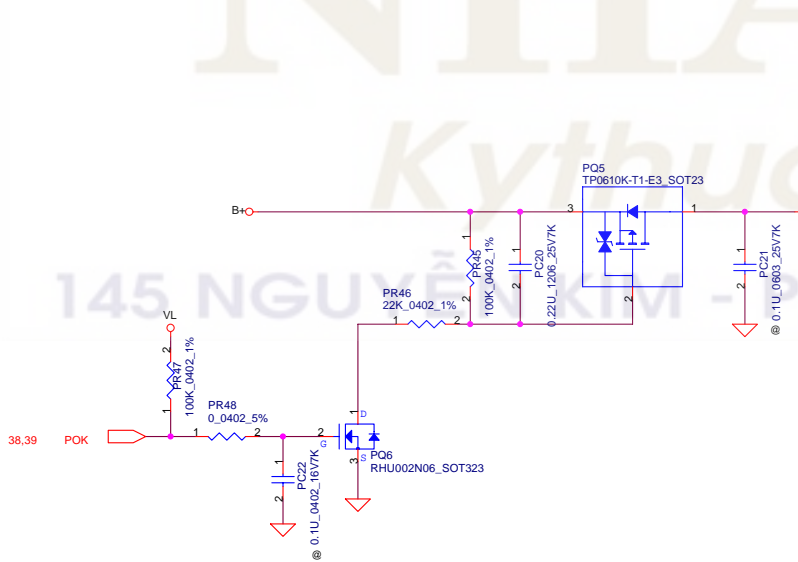
**Precharge detector**  
 15.97V/14.84V FOR  
 ADAPTOR

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**PH1 under CPU botten side :**  
 CPU thermal protection at 84 degree C  
 Recovery at 45 degree C



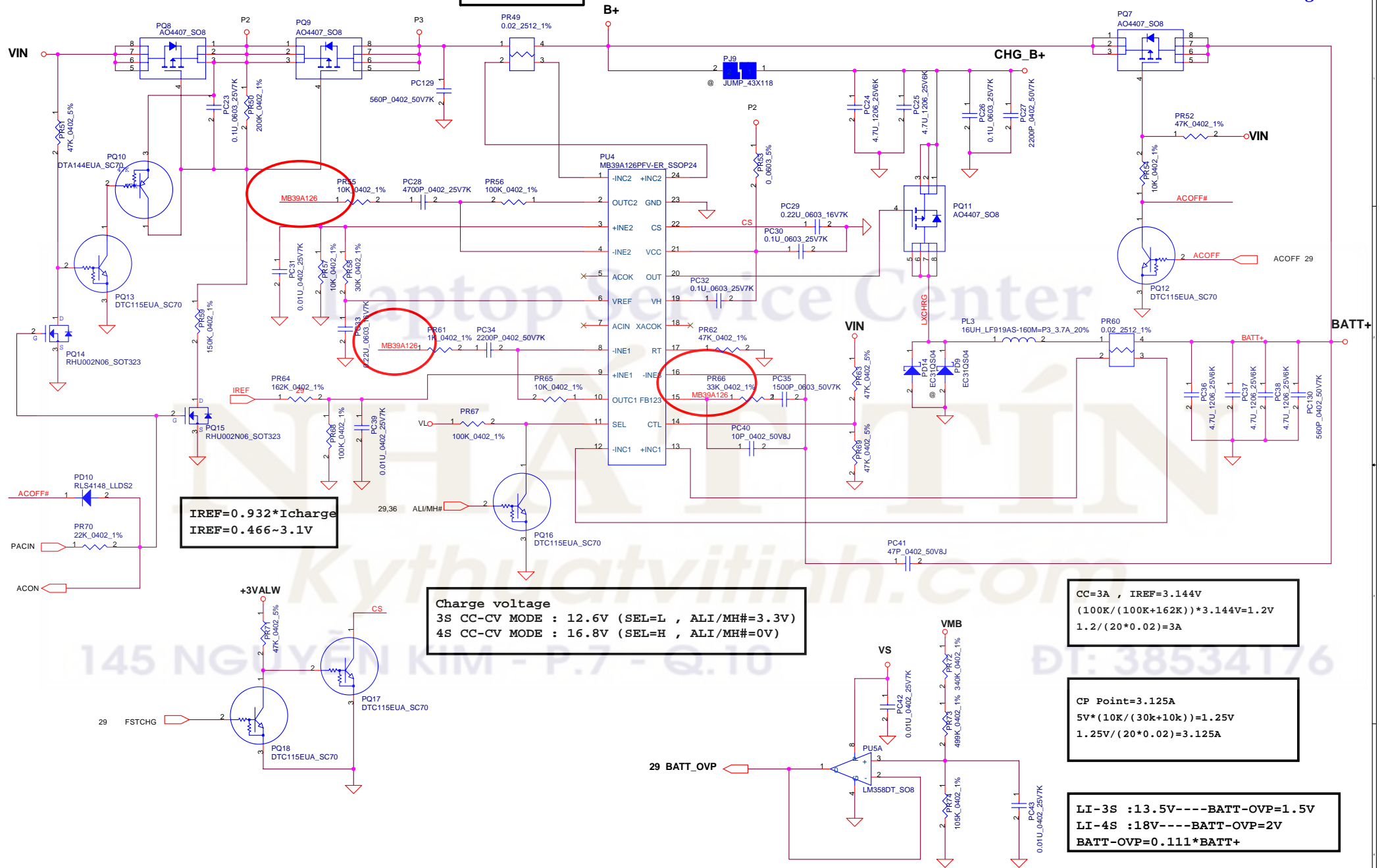
**PH2 near main Battery CONN :**  
 BAT. thermal protection at 79 degree C  
 Recovery at 45 degree C



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$I_{adp} = 0 \sim 3.125A$

$F_{osc} = 14100 / R_t = 14100 / 47 = 300KHz$



$I_{REF} = 0.932 * I_{charge}$   
 $I_{REF} = 0.466 \sim 3.1V$

**Charge voltage**  
 3S CC-CV MODE : 12.6V (SEL=L , ALI/MH#=3.3V)  
 4S CC-CV MODE : 16.8V (SEL=H , ALI/MH#=0V)

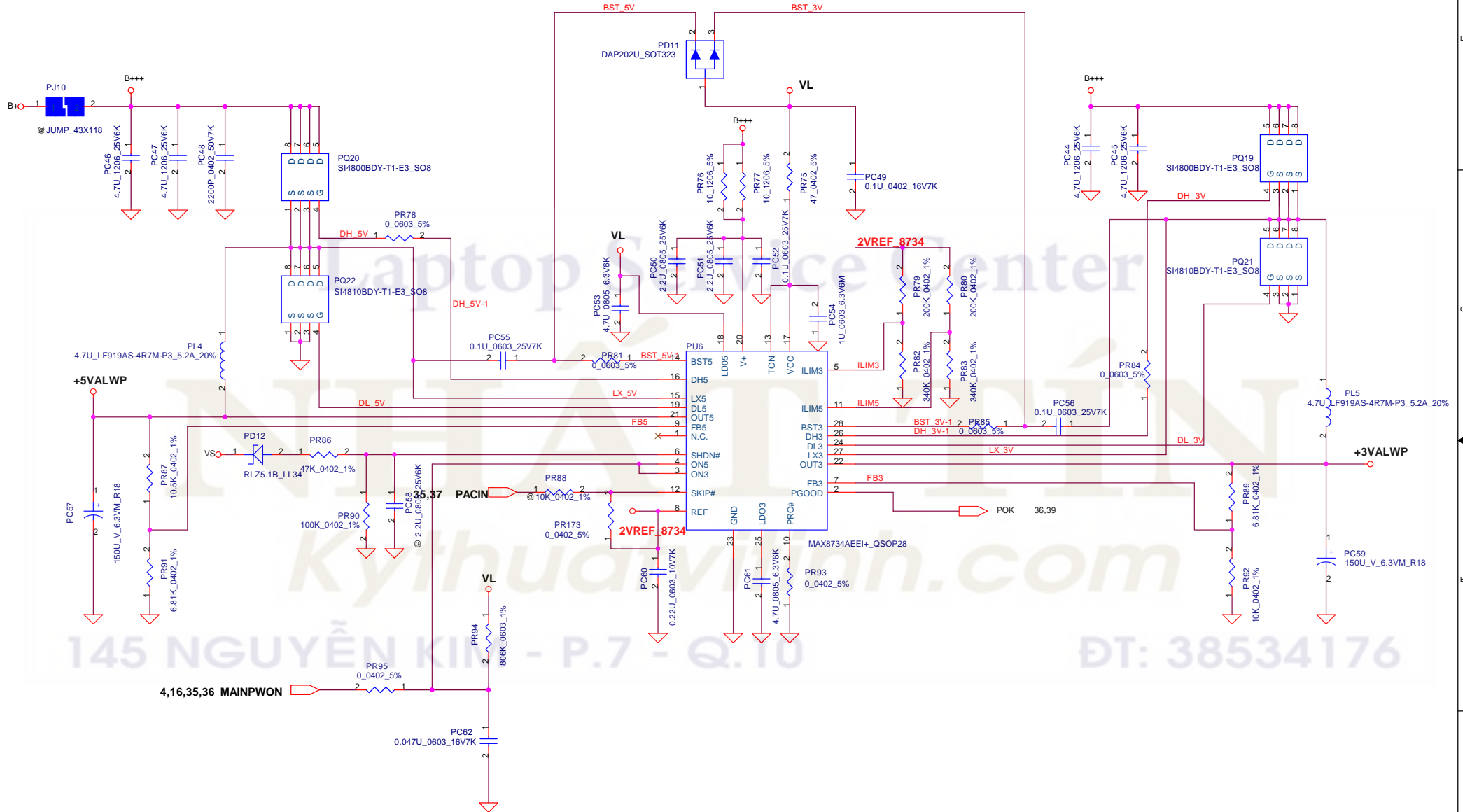
$CC = 3A , I_{REF} = 3.144V$   
 $(100K / (100K + 162K)) * 3.144V = 1.2V$   
 $1.2V / (20 * 0.02) = 3A$

**CP Point = 3.125A**  
 $5V * (10K / (30K + 10K)) = 1.25V$   
 $1.25V / (20 * 0.02) = 3.125A$

**LI-3S : 13.5V --- BATT-OVP = 1.5V**  
**LI-4S : 18V --- BATT-OVP = 2V**  
 $BATT-OVP = 0.111 * BATT+$

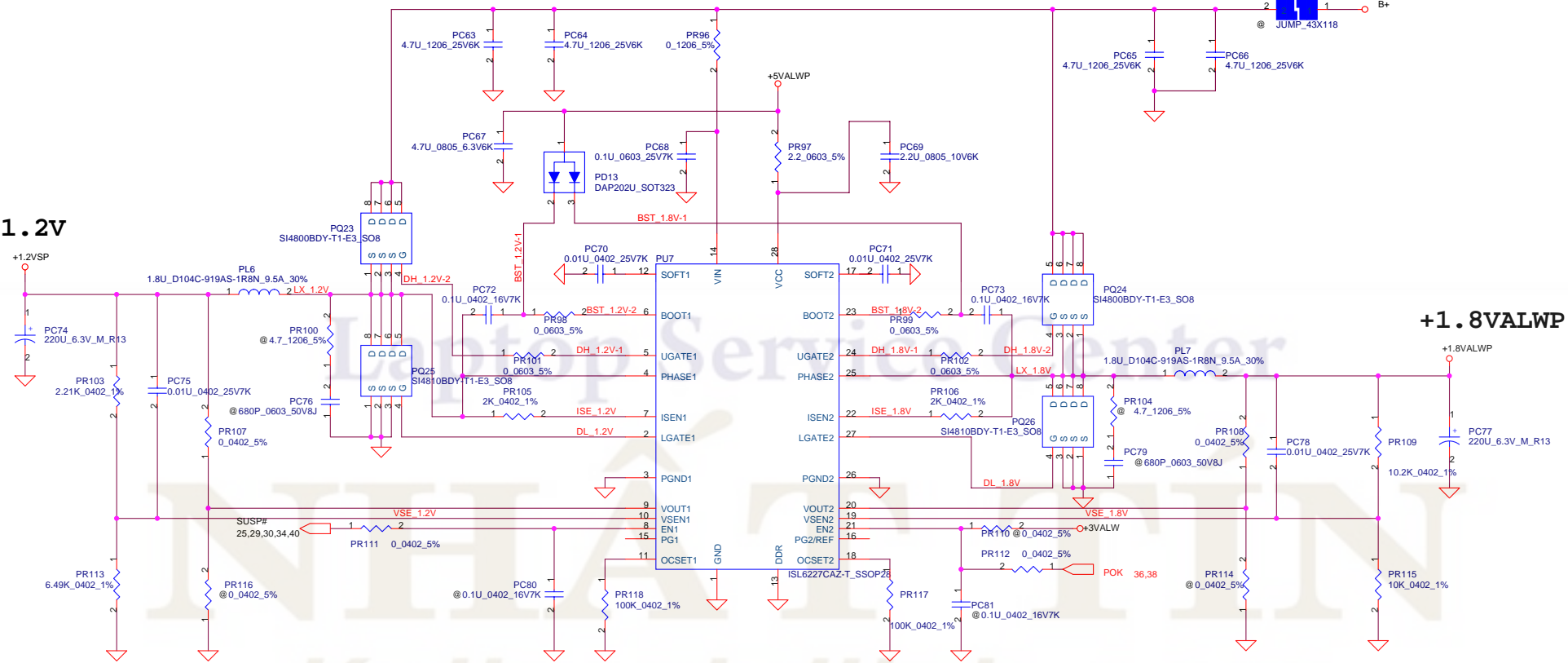
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**+3.3VALWP/+5VALWP**



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+1.2V



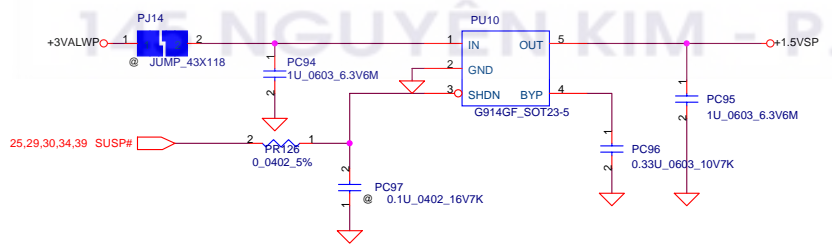
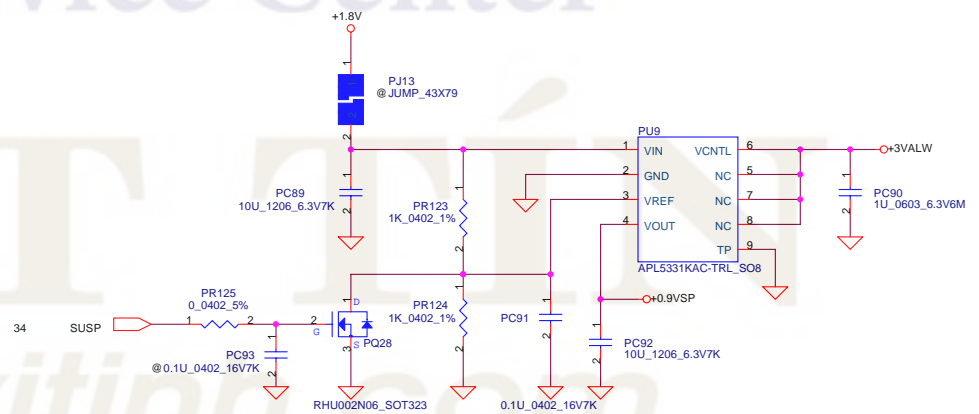
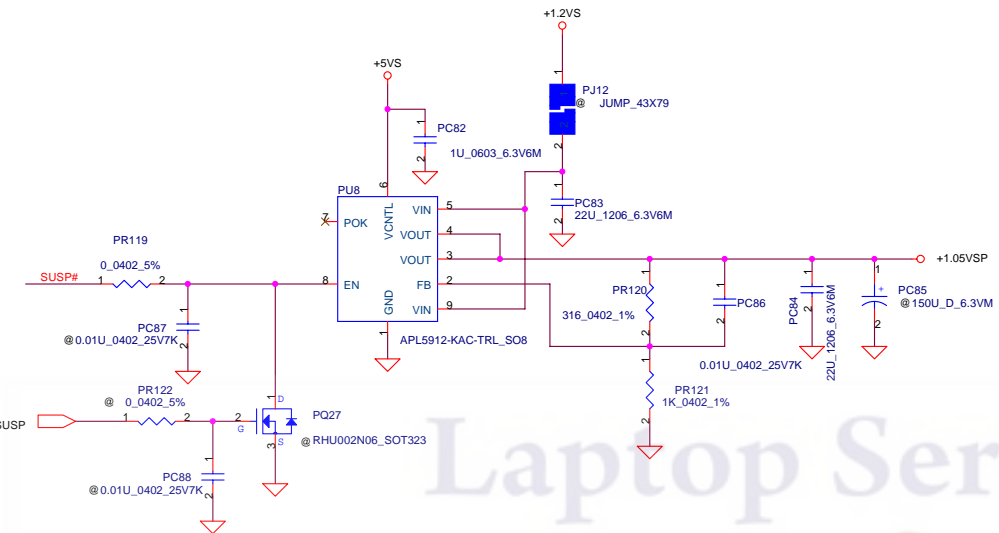
+1.8VALWP

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Laptop Service Center

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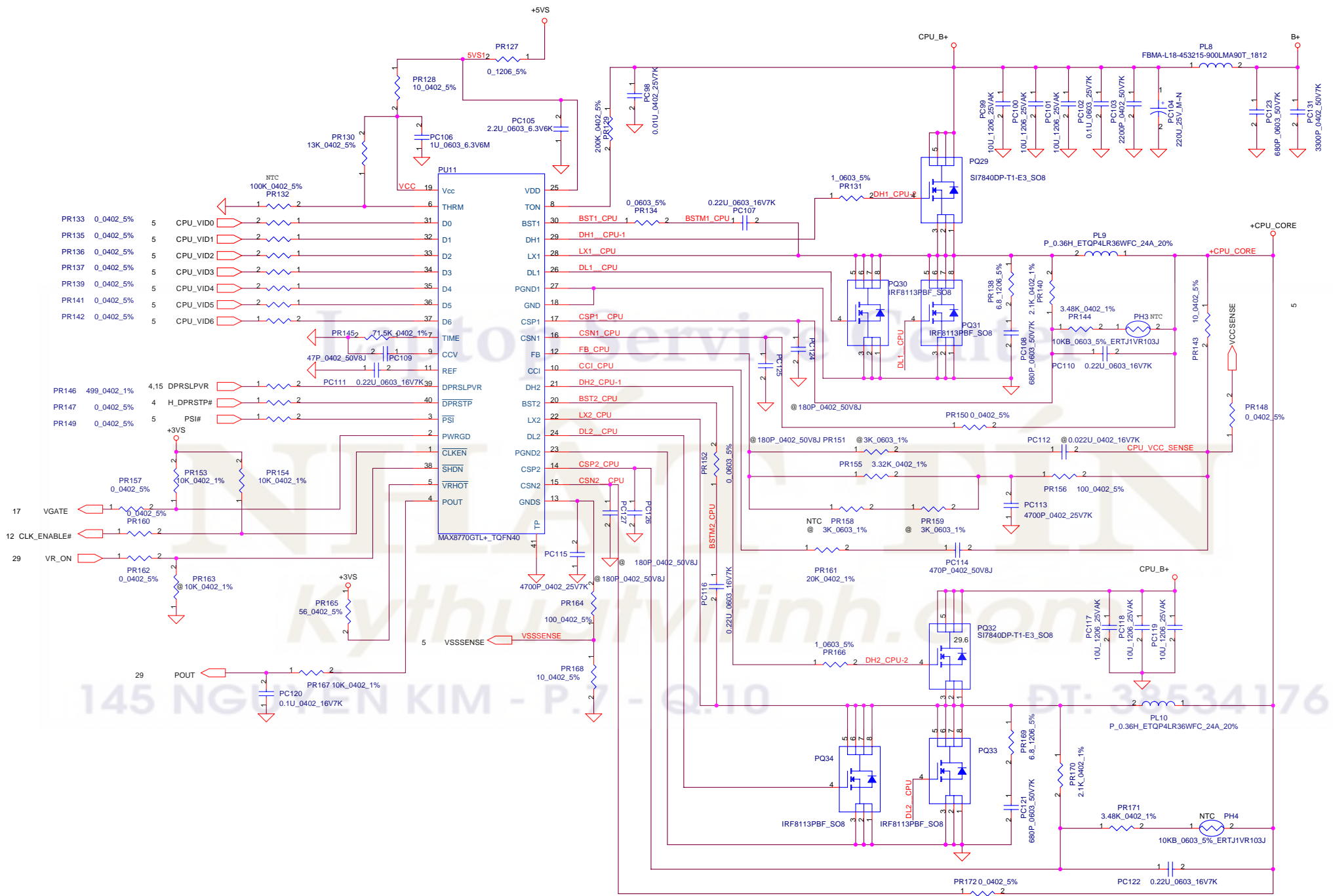
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**+CPU\_CORE**

# HW4 Product Improvement Record (P.I.R.)

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Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
8	Net connection	U21.AG30 (MEM_ODT0) U21.AE28 (MEM_ODT1) U21.AC30 (MEM_ODT2) U21.Y30 (MEM_ODT3)	DDR_ODT0 DDR_ODT1 DDR_ODT2 DDR_ODT3	NC NC NC NC	DDR 667 workaround, ATI recommend (PA_RS400R2)	0.2	
10	Net connection	JP16.80 (DIMMA_CKE1)	DDR_SCKE1	DDR_SCKE0			
11	Net connection	JP15.79 (DIMMB_CKE0) JP15.79 (DIMMB_CKE1)	DDR_SCKE2 DDR_SCKE3	DDR_SCKE1 DDR_SCKE1			
10	Net connection	JP16.114 (DIMMA_ODT0) JP16.119 (DIMMA_ODT1) JP15.114 (DIMMB_ODT0) JP16.119 (DIMMB_ODT1) RP1.4 (CKE3 PU) RP1.1 (CKE2 PU) RP4.4 (ODT3 PU) RP14.3 (ODT0 PU) RP14.2 (ODT1 PU) R40 (ODT2 PU) R12 (CKE2 PD) R17 (CKE3 PD)	DDR_ODT0 DDR_ODT2 DDR_ODT1 DDR_ODT3 DDR_SCKE3 DDR_SCKE2 DDR_ODT3 DDR_ODT0 DDR_ODT1	DDR_SCKE2 GND DDR_SCKE3 GND NC NC NC DDR_SCKE2 DDR_SCKE3			
	Del part		56_0402_5%				
	Add part			180_0402_5% 180_0402_5%			
9	Change part	C70, C68, C63, C62, C51	0.1U_0402_6.3V4Z	1U_0402_6.3V4Z	VDDA_18 decoupling, ATI recommend	0.2	
15	Change part	C295, C298, C300, C305	0.1U_0402_6.3V4Z	0.01U_0402_16V7K	ALINK coupling cap for differential signal, ATI recommend	0.2	
16	Net connection	U9.A21(USB_HSDP1+) U9.B21(USB_HSDM1-)	USBP1- USBP1+	USBP1+ USBP1-	Fix USB function fail	0.2	
16	Net connection	R760.1 (MAINPWONR PU)	+3VS	+3VALW	For SB mainpwron (Gevent) is S5 power pin	0.2	
25	Net connection	R740.2 (PH sensor) R785 (Mic sensor)	N17081292 N16810569	NBA_PLUG MIC_SENSE	For audio jack change to normal open	0.2	
	Del part	R872, R873 R786, R842 Q59, Q67	0_0402_5%(@) 100K_0402_5% 2N7002_SOT23				
	Change part	JP34, JP35	FOX_JA6033L-B5S3-7F	FOX_JA6333L-B3T0-7F			
26	Net connection	U47.16 (VSS)	GND	CVSS	Fix audio left channel no function	0.2	
29	Change part	R116	10K_0402_5%	100K_0402_5%	Fix BATT charge LED always light, for power workaround	0.2	

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# HW4 Product Improvement Record (P.I.R.)

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Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
15	Add part  Net connection	D28 R899 C972 U9.D27 (SB BMREQ#)	_____ _____ _____ BM_REQ#	CH751H-40_SC76 10K_0402_5% 15P_0402_50V8D SB_BM_REQ#	For C3 pop-up and Cle HW rework. ATI recommend (PA_IXP400AC16)	0.2	
15	Change part  Add part  Net connection BOM Structure	U36 R802 R900, R901 C973 D29 Q6 Q1 R902 U9.E29 (SB STPCLK#) Q62, U36, C832, C833, D42	TC7SH00FU_SSOP5 200K_0402_5%(@) _____ _____ _____ _____ H_STPCLK# @	74LVC1G14GW_SOT353-5 150K_0402_5% 10K_0402_5% 330P_0402_50V7J CH751H-40_SC76 MMBT3904_SOT23 2N7002_SOT23 0_0402_5% SB_STPCLK#	C4 timing on Yonah-M platforms workaround, ATI recommend (PA_IXP400BR4)	0.2	
12	Change part BOM Structure	R255 C831	0_0402_5% @	4.7K_0402_5%			
7,8,9	Change part	U21	216CPP4AKA21HK RC410ME	216DCP4ALA12FG RC410MD	For Product spec	0.2	
9 10 11	Change part	C650 C148 C52	220U_D_6.3VM(@) 220U_D2_4VM 220U_D2_4VM	220U_Y_4VM(@) 220U_Y_4VM 220U_Y_4VM	For height limit, change to 2mm	0.2	
17	BOM Structure	C884, C885, C886, C887	_____ _____ _____	2H@	For 2 HDD configuration	0.2	
26	Change part	SW10	EVQWA4001_6P	XRE094_2	For new digital VR	0.2	
26 25	Add part BOM Structure Net connection	C977, C978 C954, C955 U38.14 (LINE2_L) U38.15 (LINE2_R)	_____ _____ NC NC	1U_0402_6.3V4Z @ LIN_L LIN_R	Reserve for ALC861D/ ALC268 HP out, for Vista integrate driver	0.2	
4 8 19	DEL PART DEL PART DEL PART	R463 R465 R762 R23 R138, R139	47K_0402_5%(@) 10K_0402_5%(@) 4.7K_0402_5% 4.7K_0402_5%(@) 10K_0402_5%(@)	_____ _____ _____ _____ _____	Remove useless parts	0.2	

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Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
27 4 12	Delete part	R305 R304 C665 R268	10K_0402_5%(@) 5.6K_0603_1%(@) 0.1U_0402_16V4Z(@) 4.7K_0402_5%(@)	_____	Remove useless parts	0.2	
14	Net rename	DVI_R DVI_G DVI_B DVI_HSYNC DVI_VSYNC	DVI_R DVI_G DVI_B DVI_HSYNC DVI_VSYNC	CRT_OUT_R CRT_OUT_G CRT_OUT_B CRT_OUT_HSYNC CRT_OUT_VSYNC	For designer check	0.2	
29	Net connection	X2.1(X'tal X1) X2.2(X'tal X2)	CRY1 CRY2	CRY2 CRY1	For layout smooth	0.2	
16	Add part  BOM structure	Y7  C974, C975 R910 R911, R912 L46, R74, C267, X1, R335 R334	_____	48MHZ 20PF X6G048000FK3H-H 20P_0402_50V8J 1M_0402_5% 0_0402_5% @	Chnage USB clock from osciallor to crystal	0.2	
16	Net connection	R326.1 (GPIO5 PU) R751.1 (GPIO_M_PD)	GND +3VS	+3VS GND	For ATi requirement	0.2	
13	BOM structure	C406, C407, C810, C811	@	_____	EMI solution for LVDS	0.2	
14	Change Part BOM structure	L1, L2, L3 C1, C2, C3	FCM2012C-800_0805 @	BK1608LL121-T 0603	EMI solution for CRT	0.2	
14	Change Part	JP23	SUYIN 020133MR004S529ZL~N	SUYIN 020167MR004S511ZR	ME change	0.2	
20	Add part	R913, R914 C976	_____	49.9_0402_1%(@) 0.1U_0402_16V4Z(@)	For LAN reverse	0.2	
4	Change part	R475, R476 R490	40.2_0402_1% 150_0402_5% 27.4_0402_1%	54.9_0402_1% 54.9_0402_1% 54.9_0402_1%	For CPU ITP	0.2	
29	Change part	L20, L23	FBM-L11 160808-800LMT_0603	0_0603_5%	Change EC power sorce and gnd source	0.2	
23	Net rename	U34.26(E ECS) U34.28(E EDI) U34.29(E ECK)	E ECS E EDI E ECK	1394_E ECS 1394_E EDI 1394_E ECK	Name Name duplication	0.2	

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Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
29	Del part Add part Net Rename	Q66 C980 EC_EAPD	2N7002 EC_EAPD	0.01U_0402_16V7K(@) EC_EAPD_R#	For Audio EAPD	0.2	
29	Add part	C979 Q67 R915 R916 R917 R919		1U_0402_6.3V4Z(@) 2N7002_SOT23(@) 8.2K_0402_5%(@) 20K_0402_5%(@) 2.4K_0402_5%(@) 1K_0402_5%(@)	For POST BEEP no sound issue	0.2	
16	Del part	R384(GATE20 PU) R385(KBRST# PU)	10_0402_5% 10_0402_5%		No need external pull up	0.2	
16	Net connection Add part	U9.D6(LPC_PME#) R918	EC_PME#	LPC_PEM# 10K_0402_5%	Disconnect SB PME# to EC PME#	0.2	
16 27	Add part	C981 C982, C983		10P_0402_50V8K(@) 22P_0402_50V8J(@)	For EMI reserve	0.2	
12	Del part Net connector	R712 U23.11 (Clock REQ B)	0_0402_5%(@) N19175427	MINI_CLKREQ#	For mini card clock request	0.2	
28	BOM Structure	C712, C715		@	Transion test pass	0.2	
29	Change part	U46	NC7SZ14M5X_SOT23-5	74LVC1G14GW SOT353-5	Change package for logic IC standard	0.2	
29	Del part Net connection	R867, R868 R714.2 (BITCLK to HD) R715.2 (BITCLK to MDC)	0_0402_5% N52707434 N52707448	AZ_BITCLK_HD AZ_BITCLK_MD	Azalia signal, no need two serial reisistor	0.2	
28	Add part	R920, R921, R922, R923		0_0402_5%(@)	Reserve resistor for USB signal	0.2	
26	Add part	R924 C984		0_0402_5% (@) 0.01U_0402_16V7K(@)	Reserve function for EC control HP_EN	0.2	
26	BOM Structure	C406, C407, C810, C811	@		For LVDS EMI solution	0.2	
29	Change part	R101	0_0402_5%	8.2K_0402_5%	Board ID change to 1 for Rev0.2	0.2	
25	Add part	R925		39.2K_0603_5%	For ALC861 +Vista driver	0.3	
26	BOM Sturcture	C977, C978 C954, C955	@	@	For Vista intergated driver	0.3	

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Phase: A to B		Date: 2006/07/29			Writer: Gino Lu		
Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
26	Del part	R919 R916 R917 Q67	1K_0402_5%(@) 20K_0402_5%(@) 2.4K_0402_5%(@) 2N7002_SOT23(@)	_____	Remove POST BEEP no sound issue	0.3	
29	Change part	R101	8.2_0402_5%	18_0402_5%	PCB revision ID	0.3	
4 15	BOM Sturcture	R491 R167 R713	@ _____ @	_____ @ _____	For C4 timing	0.3	
19	BOM Sturcture	R334 R335	@ _____	_____ @	48M oscillator select	0.3	
20	Del part Change part	R235 C433	10_0402_5%(@) 22P_0402_50V8J(@)	_____ 18P_0402_50V8J(@)	LAN PCI clock for EMI	0.3	
15	BOM Structure	C832, C833, C973, D29, D42, Q1, Q6, Q62, R802, R900, R901, U36 R713, R902	_____ @	_____ @	No need C4 support	0.3	
12 15	Change part BOM Structure Add part	R255 C831 Q66 U49 R927	4.7K_0402_5% _____ _____ _____ _____	0_0402_5% @ 2N7002_SOT23(@) 74LVC1G14GW_SOT353-5(@) 10K_0402_5%(@)			
20	Add part	R926	_____ _____	20K_0402_1%(@)	Internal MIC sensor	0.3	
20	Change part	C286, C287	18P_0402_50v8D	12P_0402_50v8J	RTC timing	0.3	
20	Del part	L23	0_0603_5%	_____	Component reduce (EC A-power)	0.3	
15	Del part	R317	0_0402_5%(@)	_____	Layout reduce (SB H_RESET#)	0.3	
15	Change part	R318	11.8K_0603_1%	11.3K_0603_1%	USB adjust and EMI	0.3	
16 27	BOM Sturcture	R716, R717, R718, R871 R886, C864, C865, JP36	_____ _____ _____	MDC@ _____ MDC@	MDC option	0.3	
26	Add part Change part	R928, R929 R862, R863	_____ 39K_0402_5%	20_0402_5% 24K_0402_5%	HP serial resistor for AP2056 noise when use mono HP gain adjust	0.3	

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# HW4 Product Improvement Record (P.I.R.)

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Page#	Action Plan (add; del; change)	Location or Net_List	Before value (Attached file)	After value (Attached file)	Detail Discretion and Root Cause	Rev.	DL/DM Check
16	Del part	C974 Y7 R910 R911	20P_0402_50V8J 48MHZ_20PF_ 1M_0402_5% 0_0402_5%	_____	For USB logo and EMI	0.3	
	Change part	C975 R912	20P_0402_50V8J 0_0402_5%	12P_0402_50V8J 30_0402_5%			
	Net connect	R912.1 (48MHz source) X1.3 (48MHz source) C975.2 (48MHz source)	48M_XTAL1 48M_XTAL1 48M_XTAL1	OSC_48MHZ OSC_48MHZ OSC_48MHZ			
	BOM Structure	L46, R74, C267, X1	@	_____			
26	Add part	Q67	_____	2N7002_SOT23	De- Bo noise	0.3	
26	Change part	C954, C955 C977, C978 C957	1U_0603_6.3V4Z(@) 1U_0603_6.3V4Z 1U_0603_16V6K	2.2U_0603_6.3V6K(@) 2.2U_0603_6.3V6K 2.2U_0603_6.3V6K	Audio precision	0.3	
	Del part	R830, R832 C947, C949	1.5K_0402_5% 1U_0402_6.3V4Z	_____			
	Change part	C948, C950	1U_0402_6.3V4Z	0.22U_0402_6.3V6K			
33	Change part	C449	10U 10V M A NOJ H1.6	22U 10V M B NOJ H1.9	For De-fan noise	0.3	
13	Net connect	_____	_____	B+	For dual lamp LCD	0.3	
33	Net connect	PU5.5 (OP+) PU5.6 (OP-) R240.2	N19688420 (FAN FB) N19688478 (EC_FANCTRL) FAN1	N19688478 (EC_FANCTRL) N19688420 (FAN FB) N19688714 (FAN FB)	Update FAN control circuit	0.3	
	Change part	R836 R240 R874	10K_0402_5% 5.1K_0402_5% 5.1K_0402_5%	0_0402_5% 8.2K_0402_5% 100_0402_5%			
	BOM Structure	R875, C449	@	_____			

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# IA YAA POWER Product Improvement Record (P.I.R.)

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1.	0807	P.39	Change net susp# to pok and pok to susp#	
2.	0807	P.41	Add PC124,PC125,PC126,PC127	reserve for in-phase issue
3.	0929	P.36,37	Add PC128,PC129,PC130	For EMI solve 200MHz-300MHz Broad band
4.	0929	P.41	Add PC131	For EMI solve 80MHz-100MHz Broad band

Laptop Service Center

**NHẤT TÍN**

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