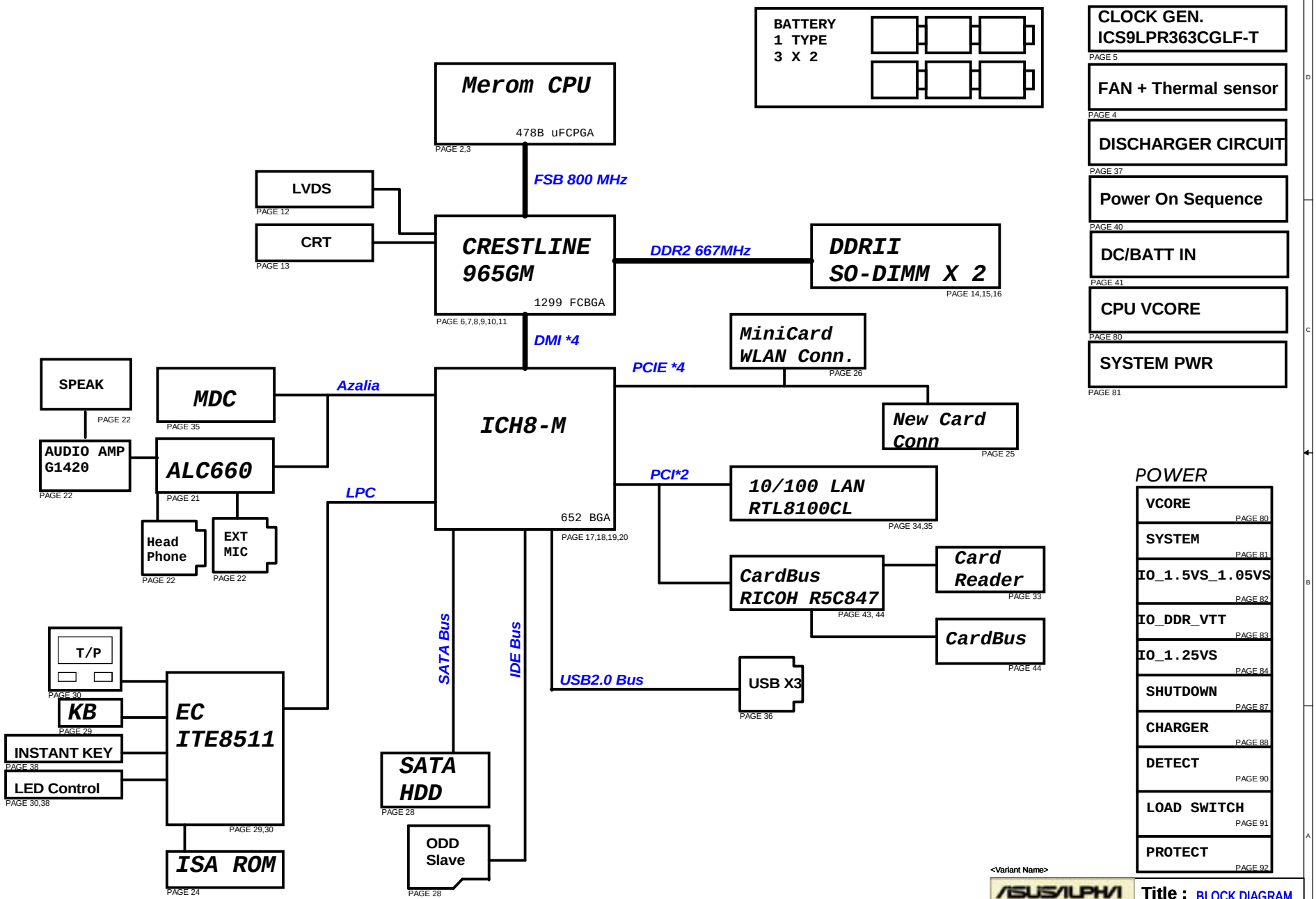
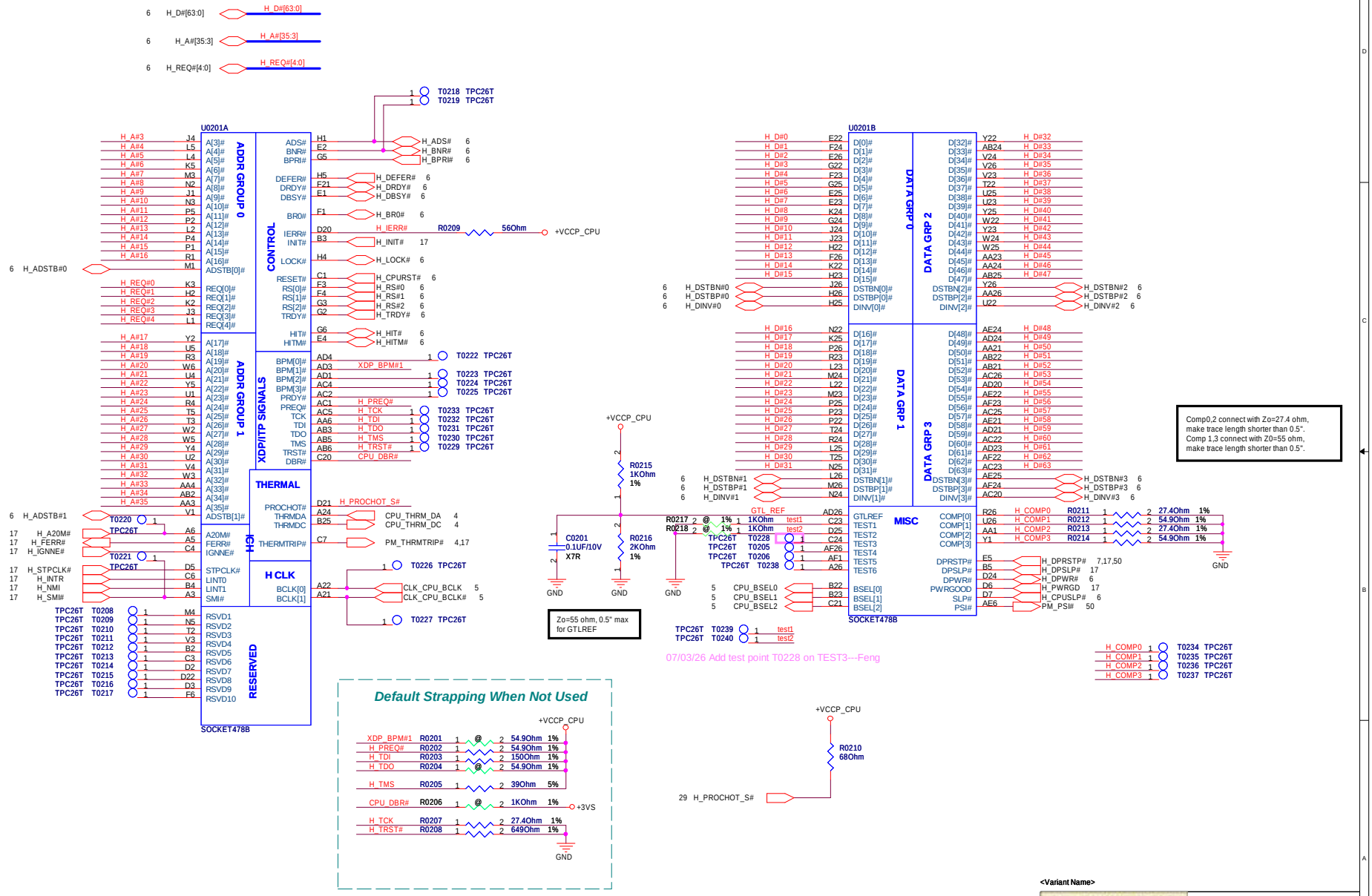
TERESA20 Main BD. R2.0 BLOCK DIAGRAM



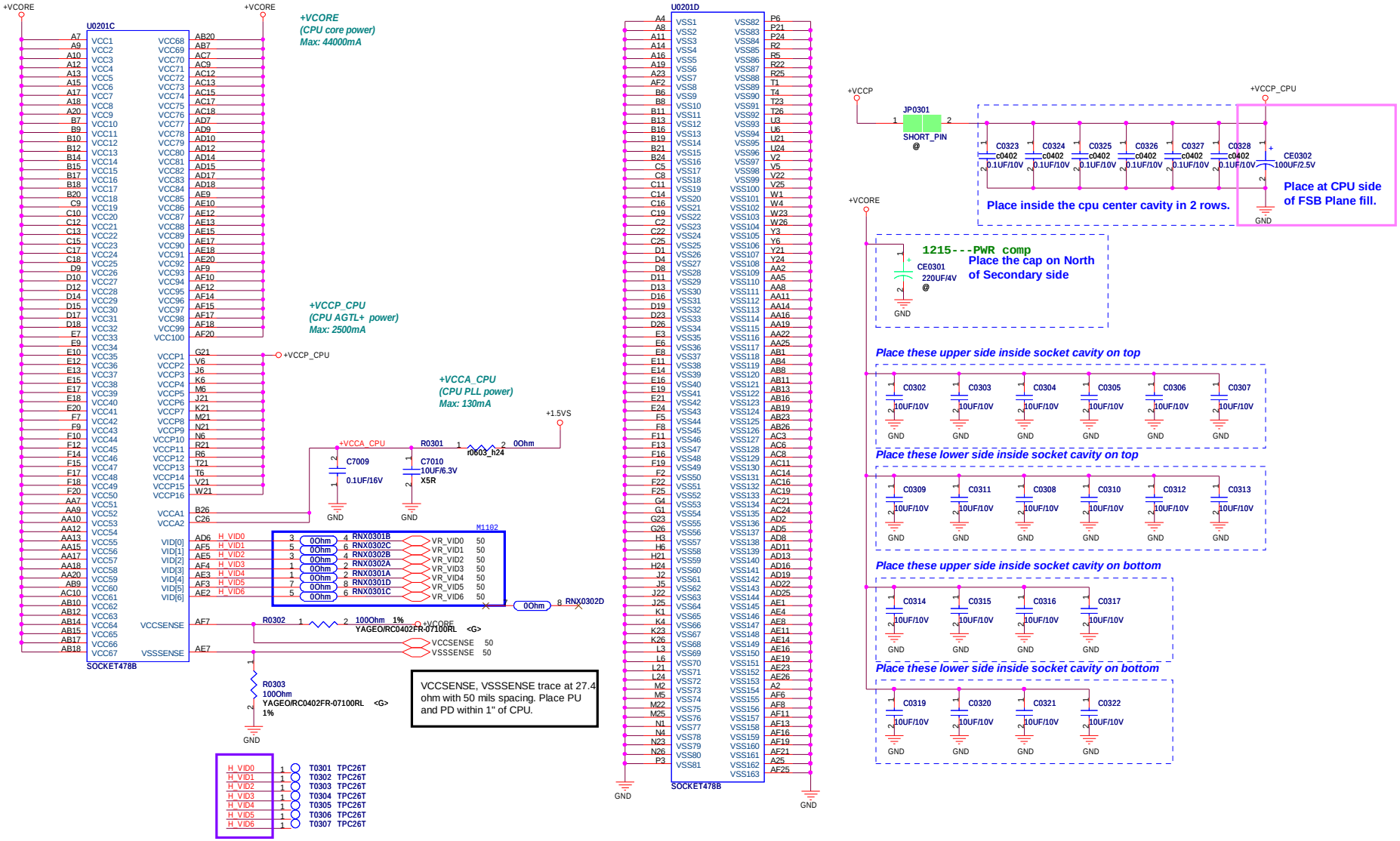


Decoupling guide from INTEL Schematic Design Checklist Rev 1.6

VCORE	22uF/10V	*32pcs
	330uF/2V	*6pcs

Decoupling guide from INTEL Layout Checklist Rev 2.0

VCCP	0.1uF	* 6pcs
	220uF	* 1pcs



<Variant Name>

ASUSALPHA

Title : MEROM CPU (2)

ASUSALPHATeK COMPUTER INC. Engineer: Julian Kuo

Size	Project Name	Rev
Custom	TERESA20	2.0

Date: Thursday, July 05, 2007 Sheet 3 of 66

Fan Speed Control

+5VS, +3VS, +3VA → +5VS, +3VS, +3VA
13,19,20,21,22,28,29,30,34,37,38,50,61
2,5,7,10,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,43,50,61,62
12,19,29,37,38,41,51,63

KBC will issue a analog (a voltage level) signal.

SW: FAN_DA1 must be low during S3

07/04/06 Remove the CE0401 and D0401 --- Iverson

+5VS, +3VS, R0402 10KOhm, C0408 10UF/10V, C0402 0.1UF/10V, GND

29 FAN_PWM → FAN_PWM

WtoB_CON_4P (NC2, NC1, CON0401), C0403 100PF/50V @, GND

+3VS, R0403 10KOhm

29 FAN0_TACH → FAN0_TACH

C0401 2200PF/50V, GND

THERMAL PROTECTION
PLACE UNDER CPU

(85 DEGREE C)

07/04/06 105 -> 85, R411 need to be tuned
maybe R411=14.7K Ohm(10G213147213010) --- Iverson

+3VA, T0403 Do Not Stuff, R0411 14.7KOhm

R0412, R0413, R0414, R0415, R0416 100KOhm (R0413, R0414, R0415 @)

07/05/16 Don't stuff R0415, but stuff R0416 ---Feng

T0402 Do Not Stuff, C0407 0.01UF/50V

U0402 PST9013NR (NC, VCC, SUB, GND, VOUT)

FORCE_OFF# 29,38,41,51,62

T0401 Do Not Stuff

+3VS, +3VS_THM, R0408 0Ohm r0402, C0405 0.1UF/10V c0402

Standby Mode: 3uA(Max. 10uA)
Full Active: 0.5 mA(Max. 1mA)

+3VS, R0406 1MOhm, VSUS_ON_G, Q0402 PMBS3904, C0404 0.22UF/6.3V

+3VA, R0405 10KOhm r0402 @, VSUS_ON → VSUS_ON 25,29,51,63

Q0401 2N7002

2,17 PM_THRMTRIP# → R0407 330Ohm, TRIP_R

7 GMCH_THRMTRIP# → R0417 0Ohm

U0401 G781P8F (SCLK, SDATA, ALERT#, GND, VDD, D+, D-, THERM#)

29 SMB1_CLK, 29 SMB1_DAT, SMBALERT#

+3VS, R0410 4.7KOhm

CPU_THRM_DA, CPU_THRM_DC

4"-8", C0406 2200PF/50V, CPU_THRM_DA 2, CPU_THRM_DC 2

<Variant Name>

+3VS_THM, R0418 10KOhm, Q0404 2N7002 @, EC_RST_SW# 29,38,41,51,62

06G023048021

Route H_THERMDA and H_THERMDC on the same layer

----------OTHER SIGNALS
12 mils
==========GND
10 mils
========H_THERMDA(10 mils)
10 mils
========H_THERMDC(10 mils)
10 mils
========GND
12 mils
----------OTHER SIGNALS

Avoid BPSB,Power

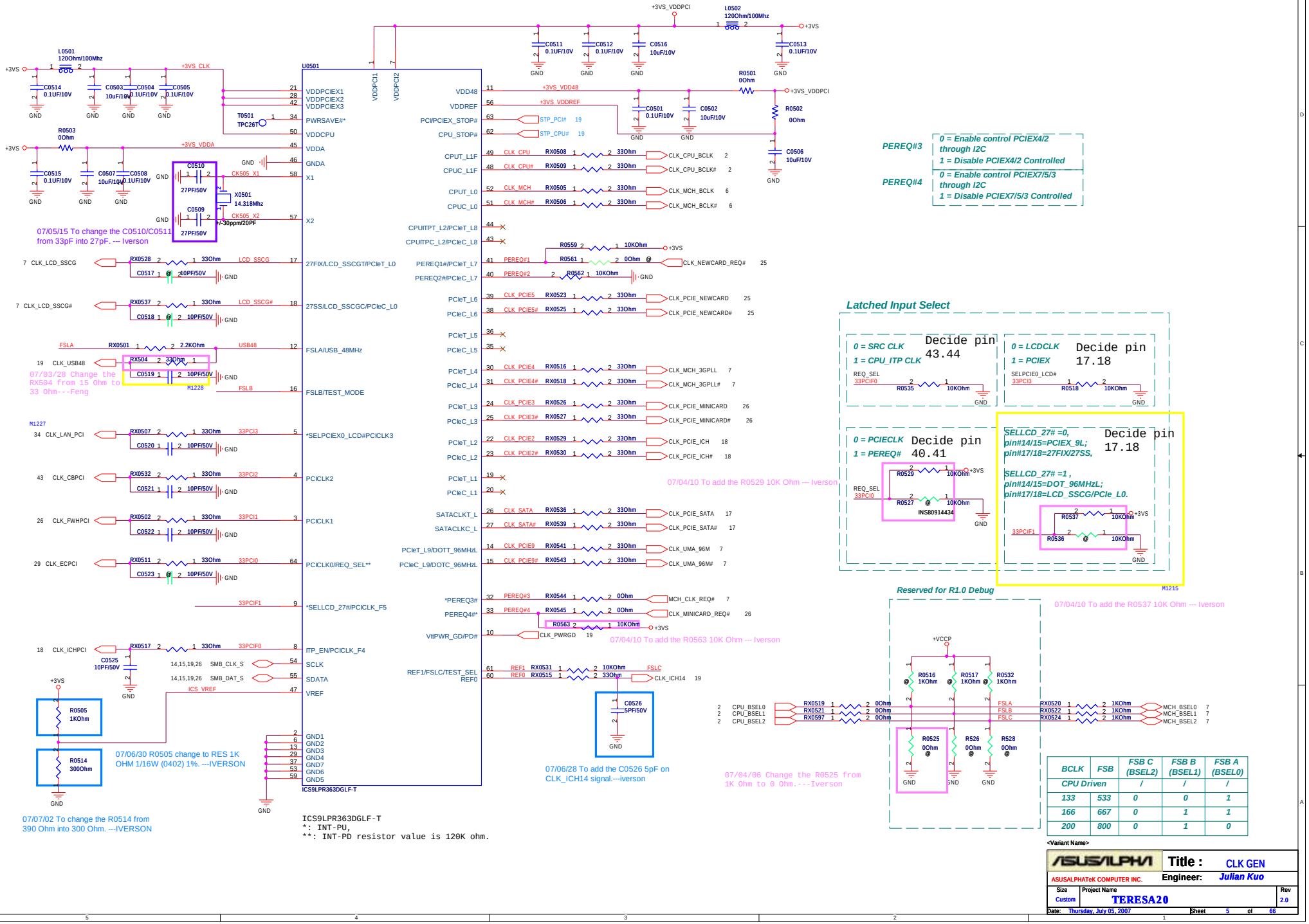
ASUSALPHA

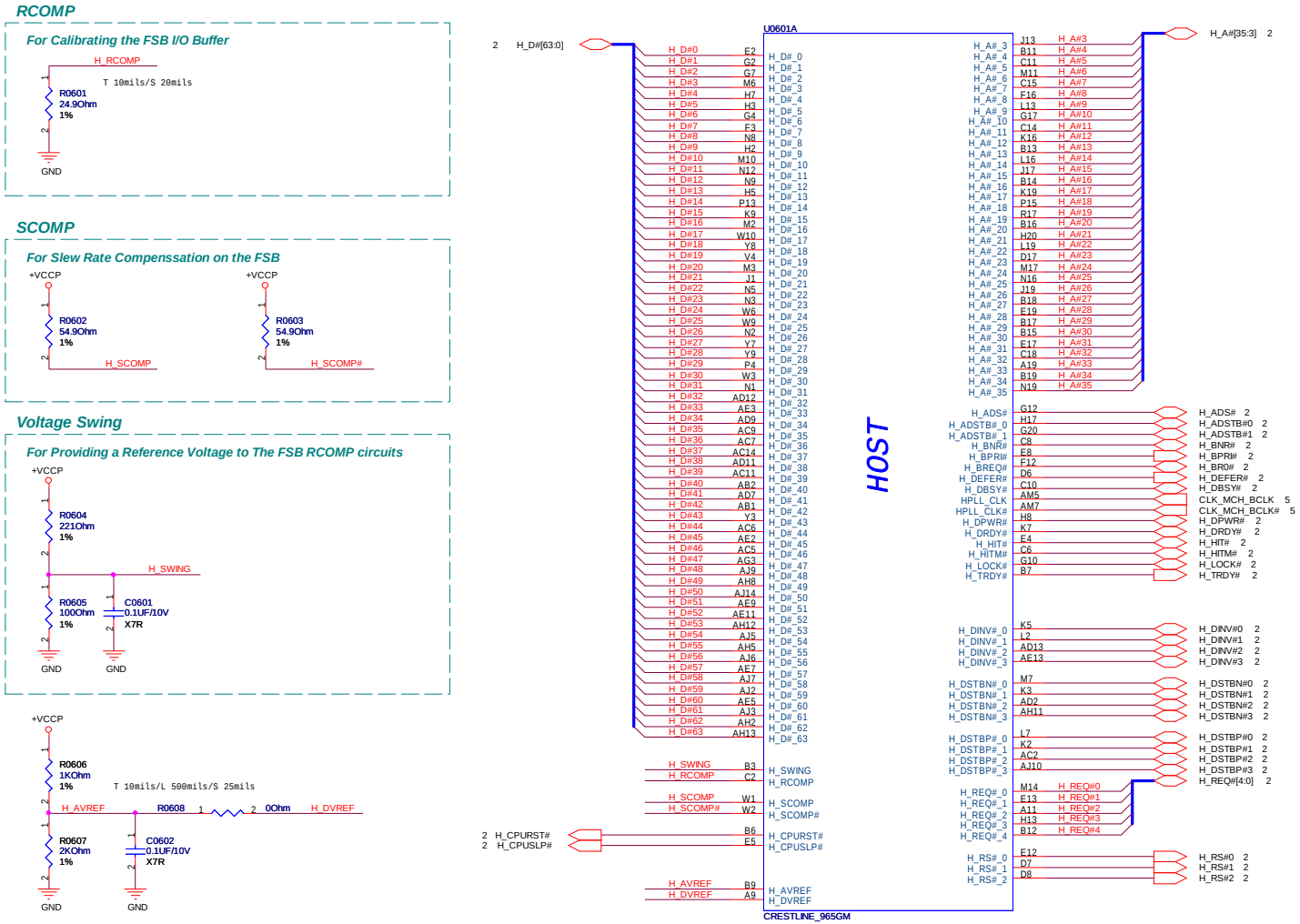
Title : THER-SENSOR,FAN

ASUSALPHATeK COMPUTER INC. Engineer: Feng Lin

Size	Project Name	Rev
Custom	TERESA20	2.0

Date: Thursday, July 05, 2007 Sheet 4 of 66





<Variant Name>

ASUSALPHA

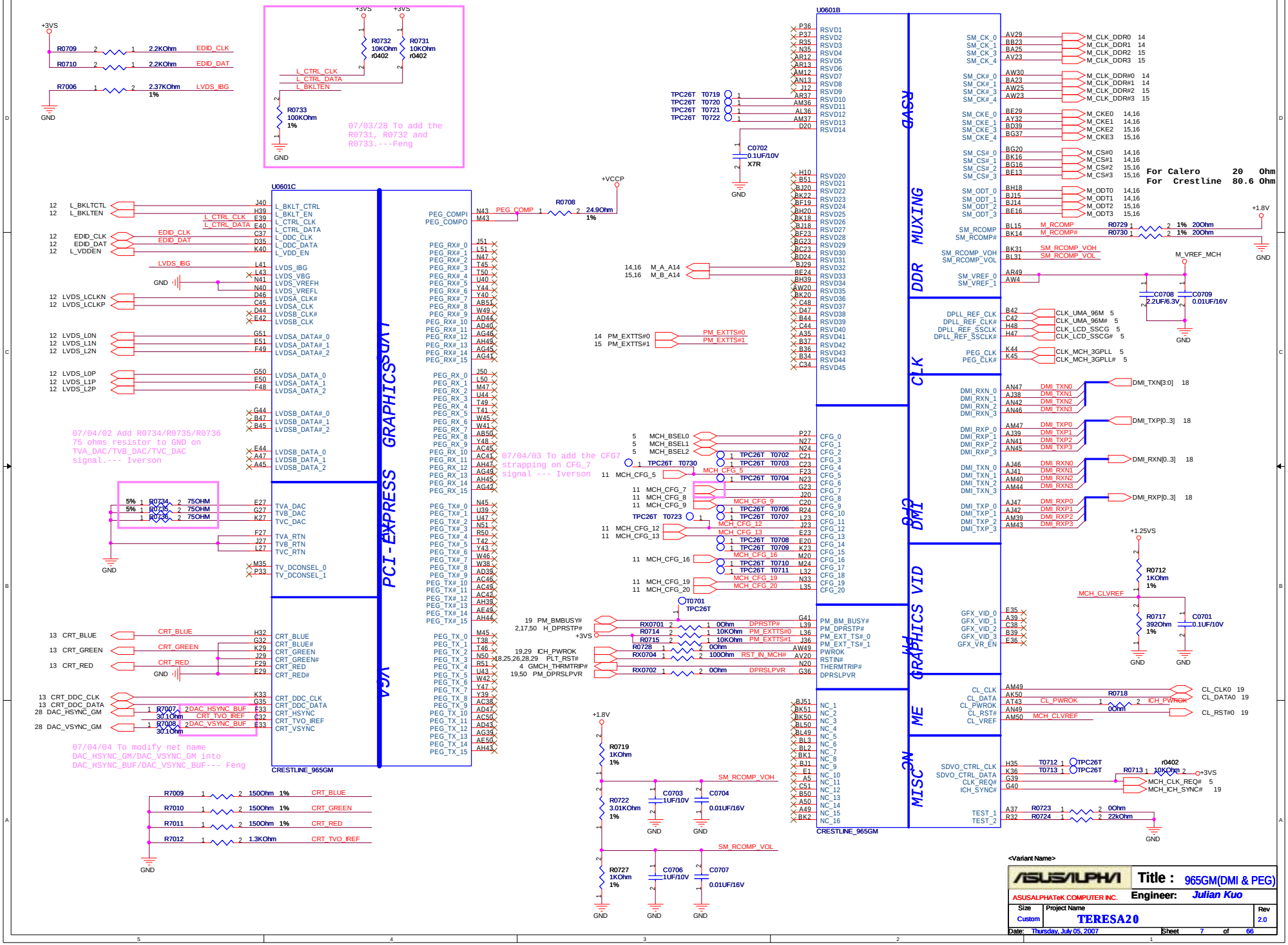
Title : NB-965GM (HOST)

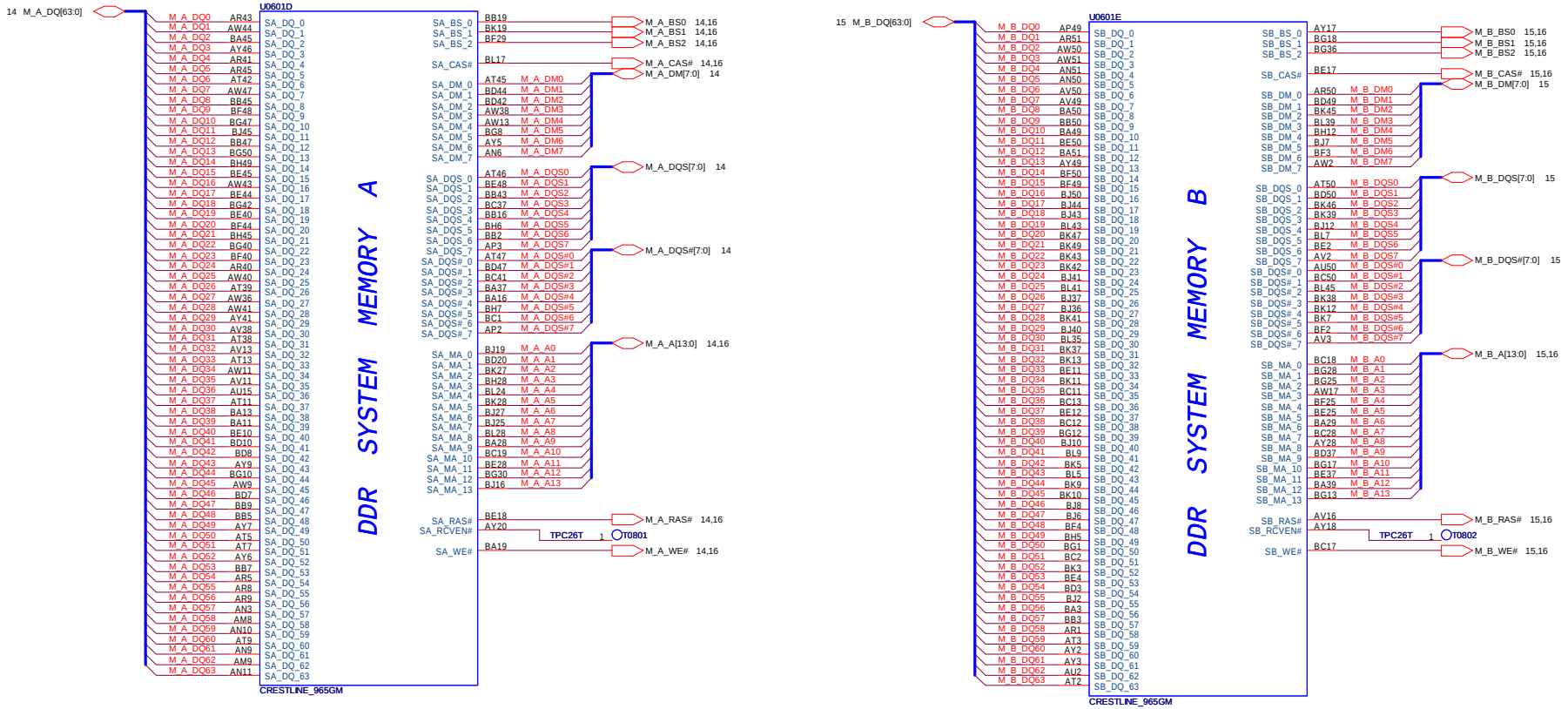
ASUSALPHATeK COMPUTER INC.

Engineer: Julian Kuo

Size	Project Name	Rev
Custom	TERESA20	2.0

Date: Thursday, July 05, 2007 Sheet 6 of 66





<Variant Name>

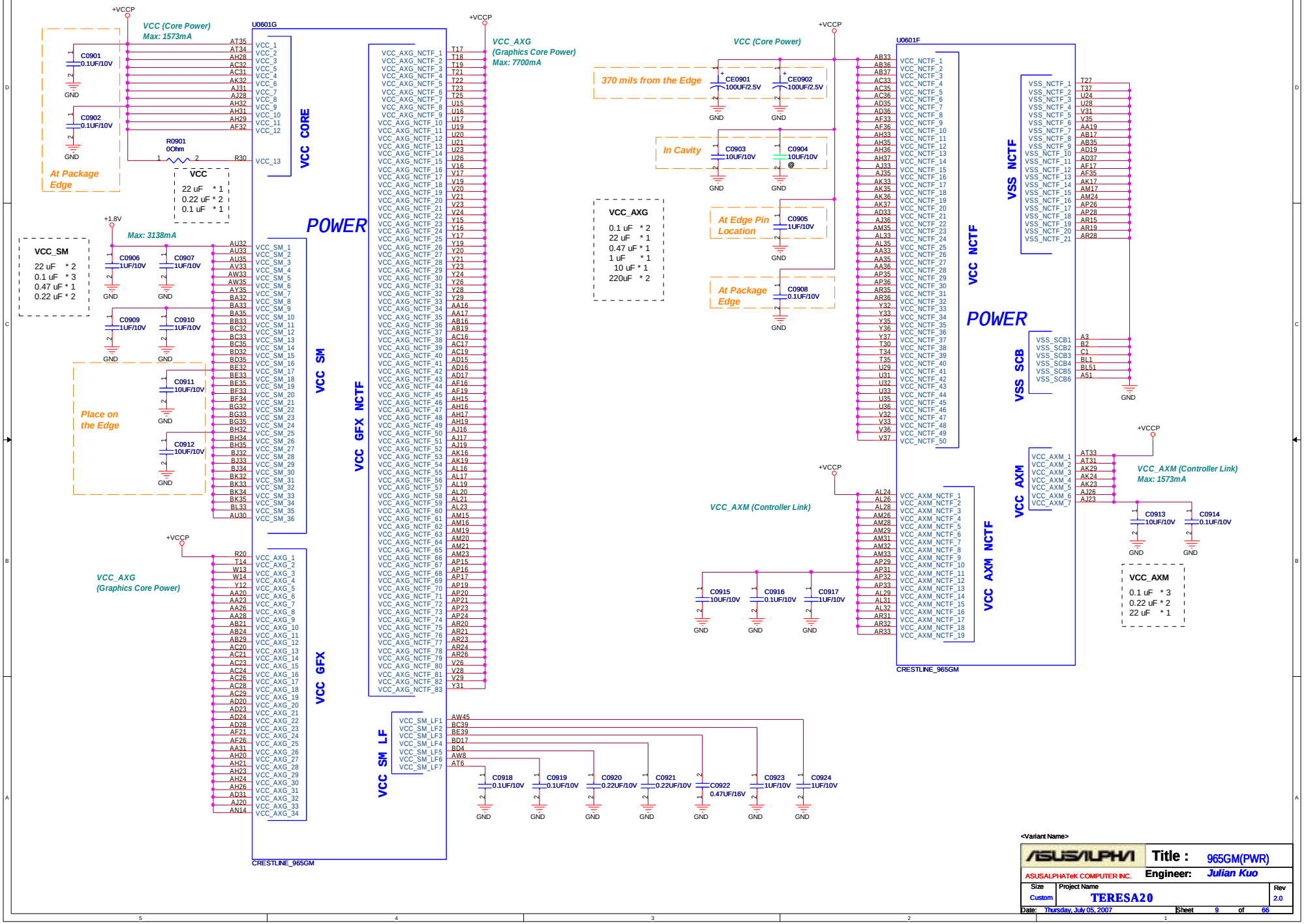
ASUSALPHA

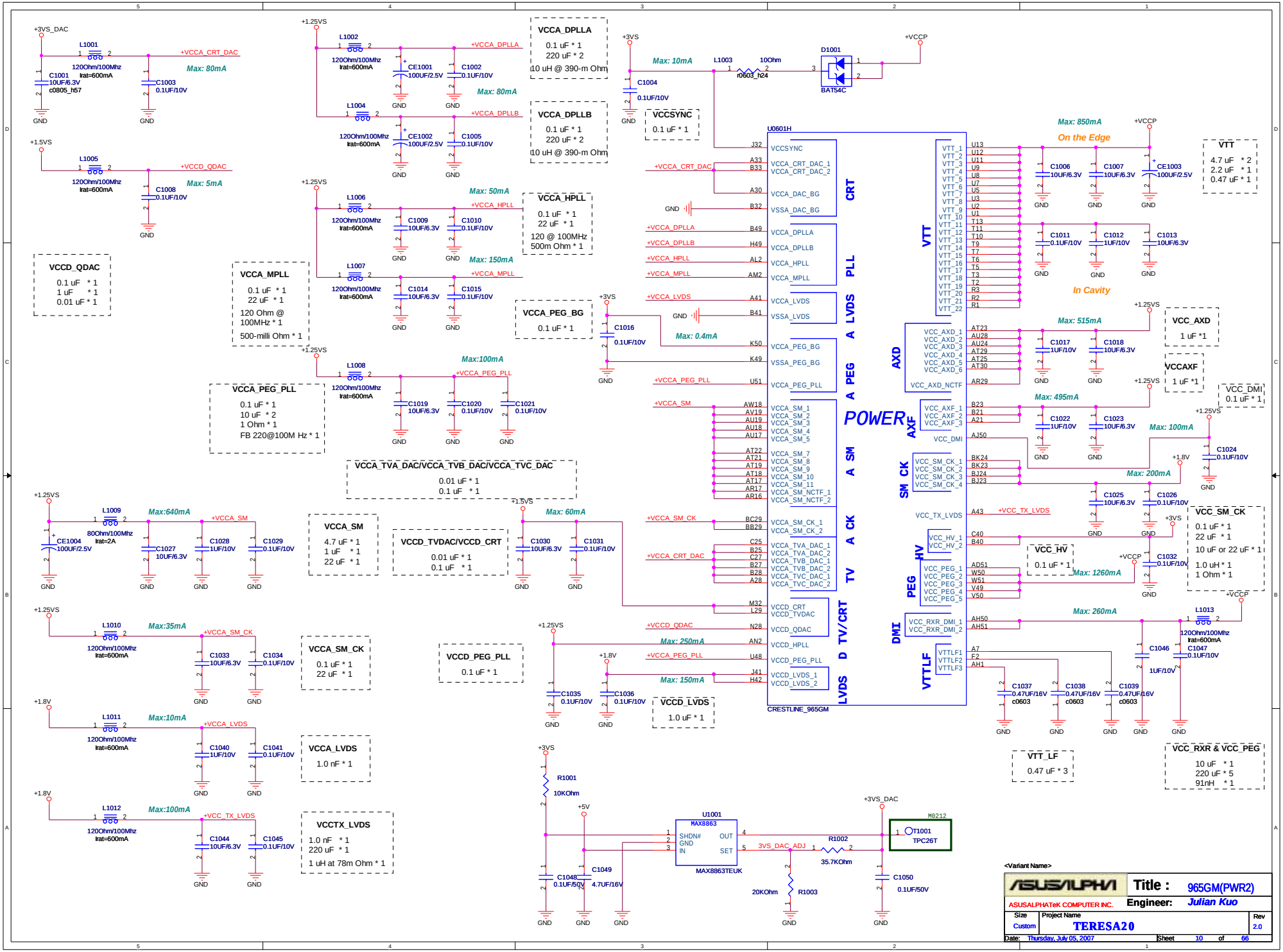
Title : 965GM(DDR2)

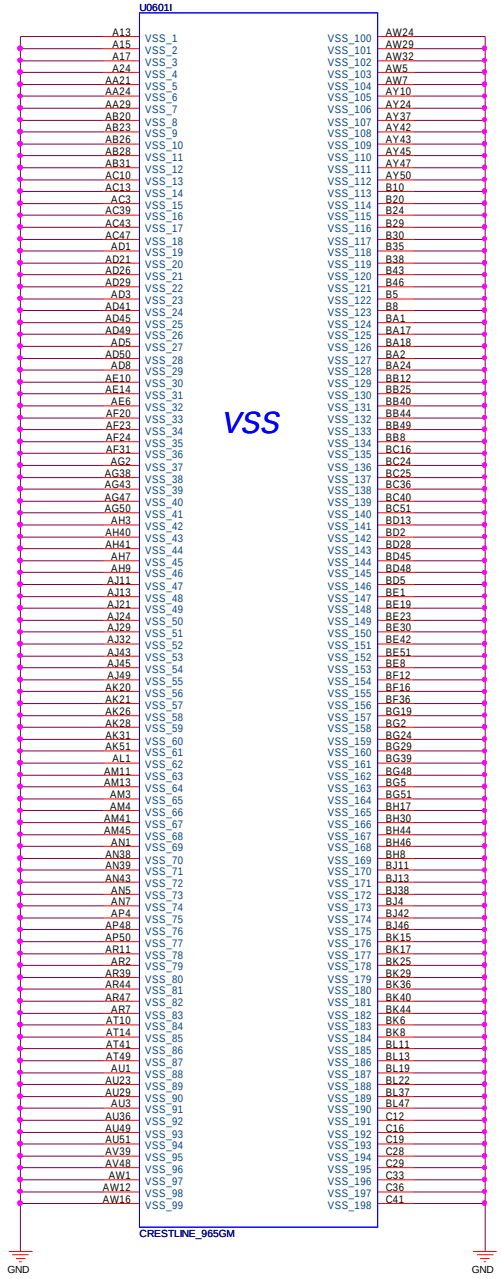
ASUSALPHATeK COMPUTER INC. Engineer: Julian Kuo

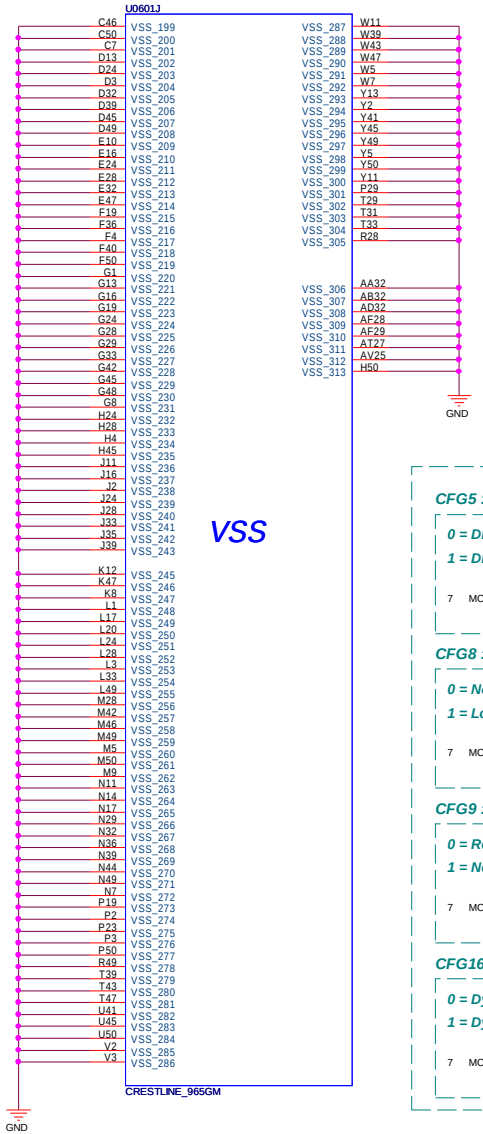
Size	Project Name	Rev
Custom	TERESA20	2.0

Date: Thursday, July 05, 2007 Sheet 8 of 66









07/04/03 To change name from Partial CLK Gating Disable into Reserved --- Iverson

GMCH Strapping

CFG5 : DMI Strap

- 0 = DMI x2
- 1 = DMI x4 (D)

CFG19 : DMI Lane Reversal

- 0 = Normal Operation (D)
- 1 = Lanes Reversed

CFG[13:12] : GMCH Test Mode

- 00= Reserved
- 01 = XOR Mode Enable
- 10 = All Z Mode Enable
- 11 = Normal Operation (D)

CFG8 : Low Power PCI-E

- 0 = Normal mode
- 1 = Low Power Mode (D)

CFG20 : Concurrent SDVO / PCIe

- 0 = Only one is operational (D)
- 1 = operate simultaneous

CFG9 : PCIE Graphic Lane

- 0 = Reverse Lane PCI-E (SDVO)
- 1 = Normal Operation (D)

- 0 = IntelR Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality
- 1= Intel Management Engine Crypto TLS Cipher Suite with confidentiality (D)

CFG16 : FSB Dynamic ODT

- 0 = Dynamic ODT Disable
- 1 = Dynamic ODT Enable (D)

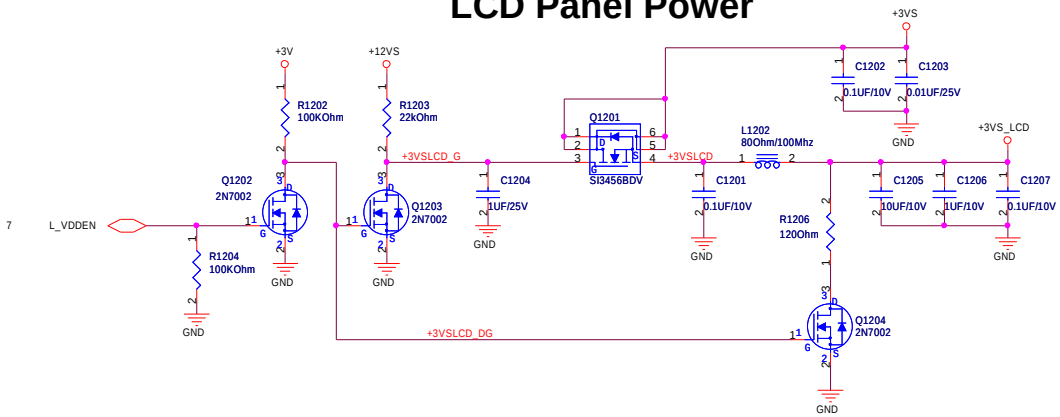
07/04/03 To add the R1127 to pull down on CFG_7 Signal.--- Iverson

<Variant Name>

ASUSALPHA	Title :	965GM(GND)
ASUSALPHATeK COMPUTER INC.	Engineer:	Julian Kuo
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 11 of 66	

LCD Panel Power

3~3.6V
Full Active: 410 mA(Max. 500 mA)
3~3.6V
S0-S1 M: 410 mA(Max. 500 mA)



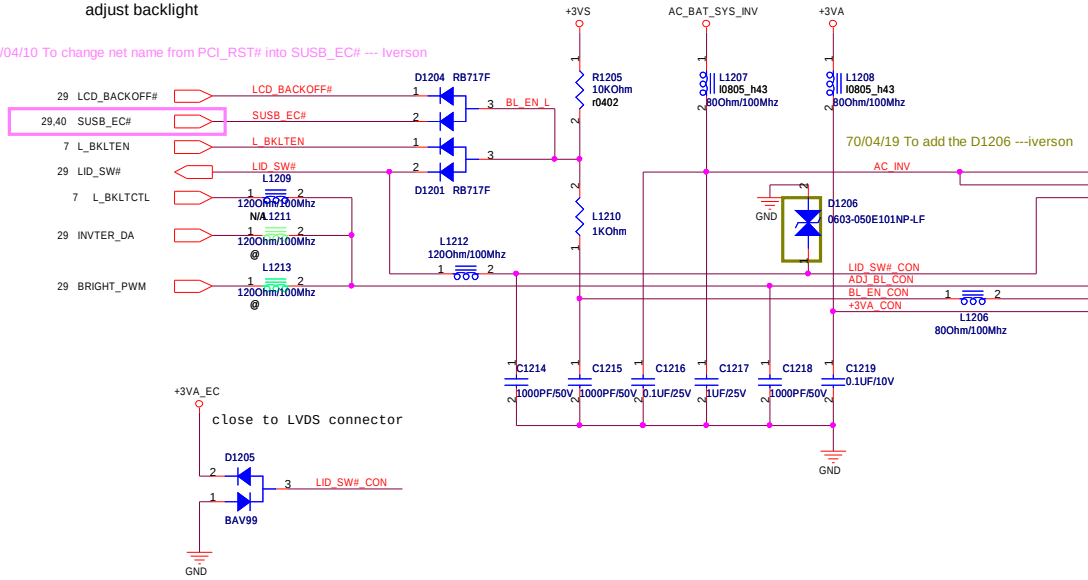
LCD Backlight Control

BIOS
LCD_BACKOFF#
When user push "Fn+F7" button
BIOS active this pin to turn On/Off backlight

EC
INVTER_DA:
EC output D/A signal (adjust voltage level) to adjust backlight

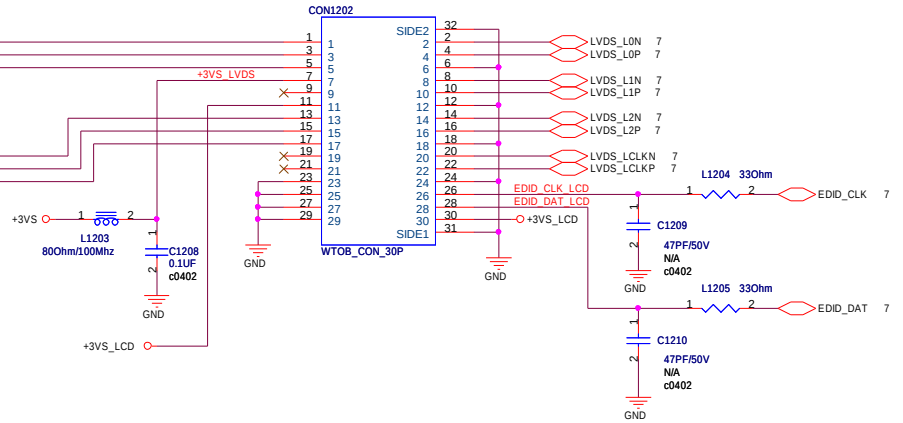
Inverter Board built in 15.4W LCD Panel

07/04/10 To change net name from PCI_RST# into SUSB_EC# --- Iverson



70/04/19 To add the D1206 ---iverson

LCD LVDS & INVERTER Interface



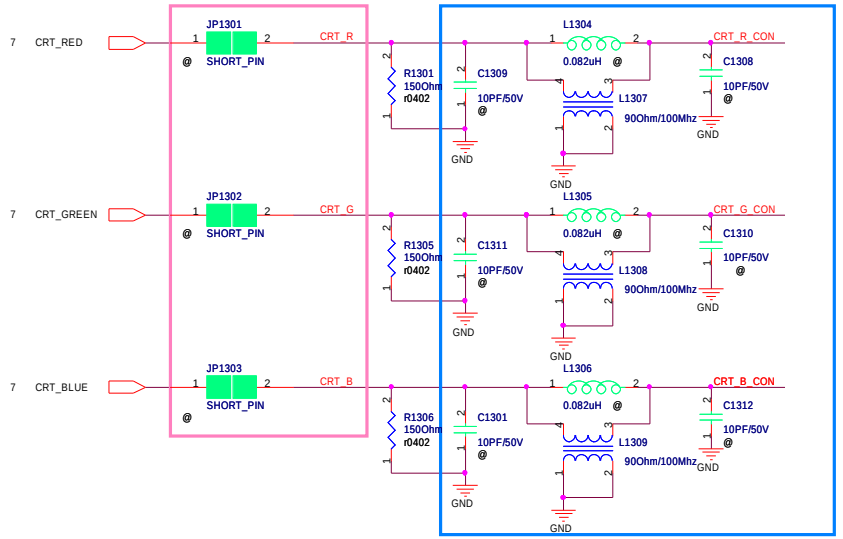
ASUSALPHA	Title : LVDS & INVERTER	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 12 of 66	

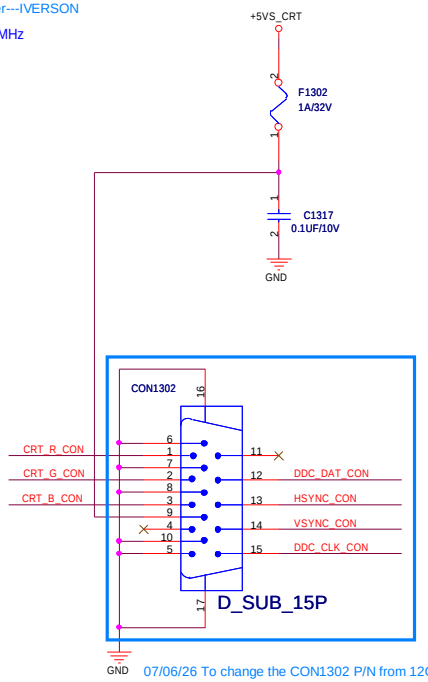
CRT OUT

07/07/02 To add the L1307 L1308 L1309. Remove the Pi-type filter---IVERSON

checklist suggests 47ohm/100MHz

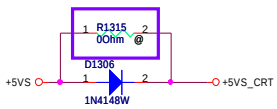
07/03/26 Modify Jump type---Feng

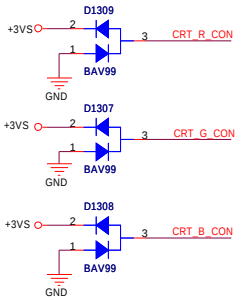


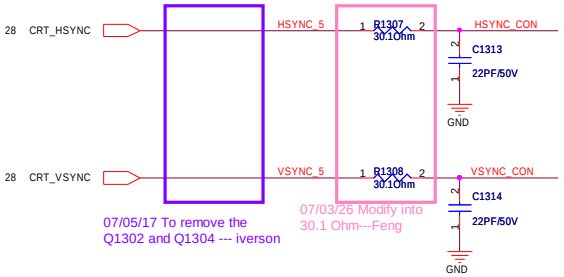


07/06/26 To change the CON1302 P/N from 12G10111015M into 12G10111215TTB --- iverson

070507 To add the R1315 0Ohm --- iverson.



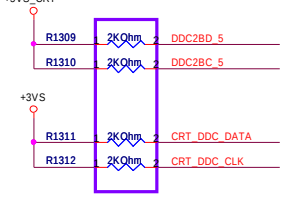


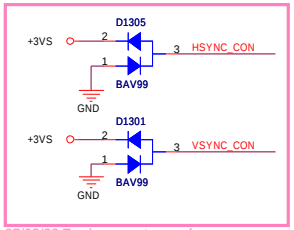


07/05/17 To remove the Q1302 and Q1304 --- iverson

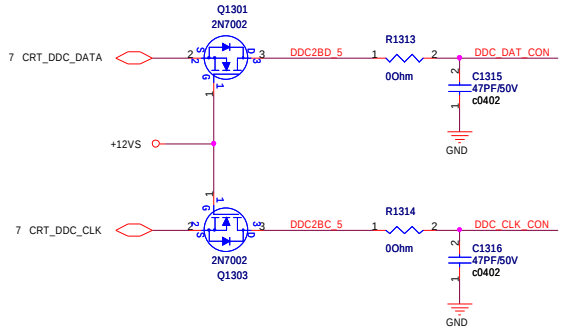
07/03/26 Modify into 30.1 Ohm---Feng

0705/23 To change the R1309/R1310/R1311/R1312 from 2.2KOhm into 2KOhm --- iverson.

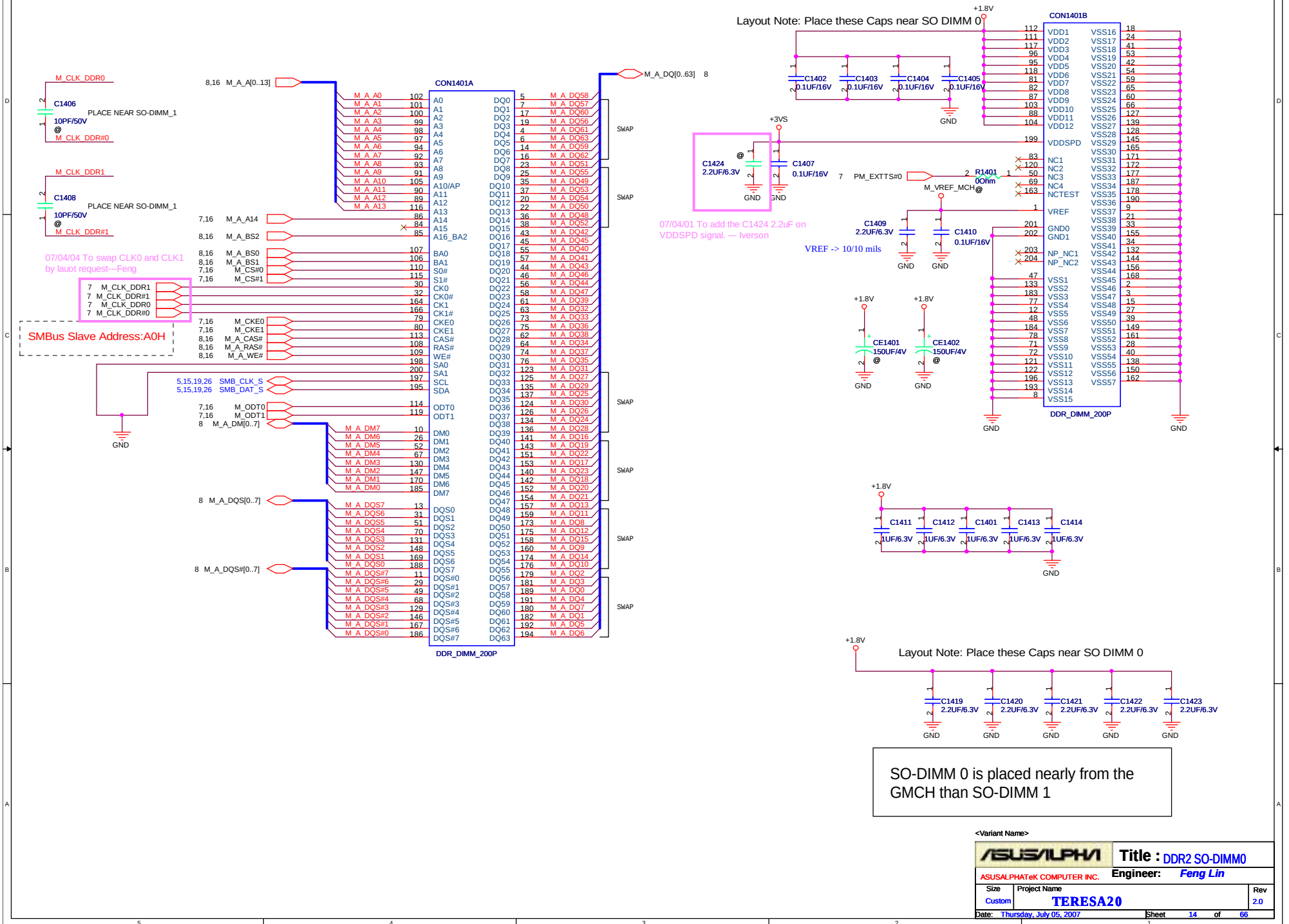


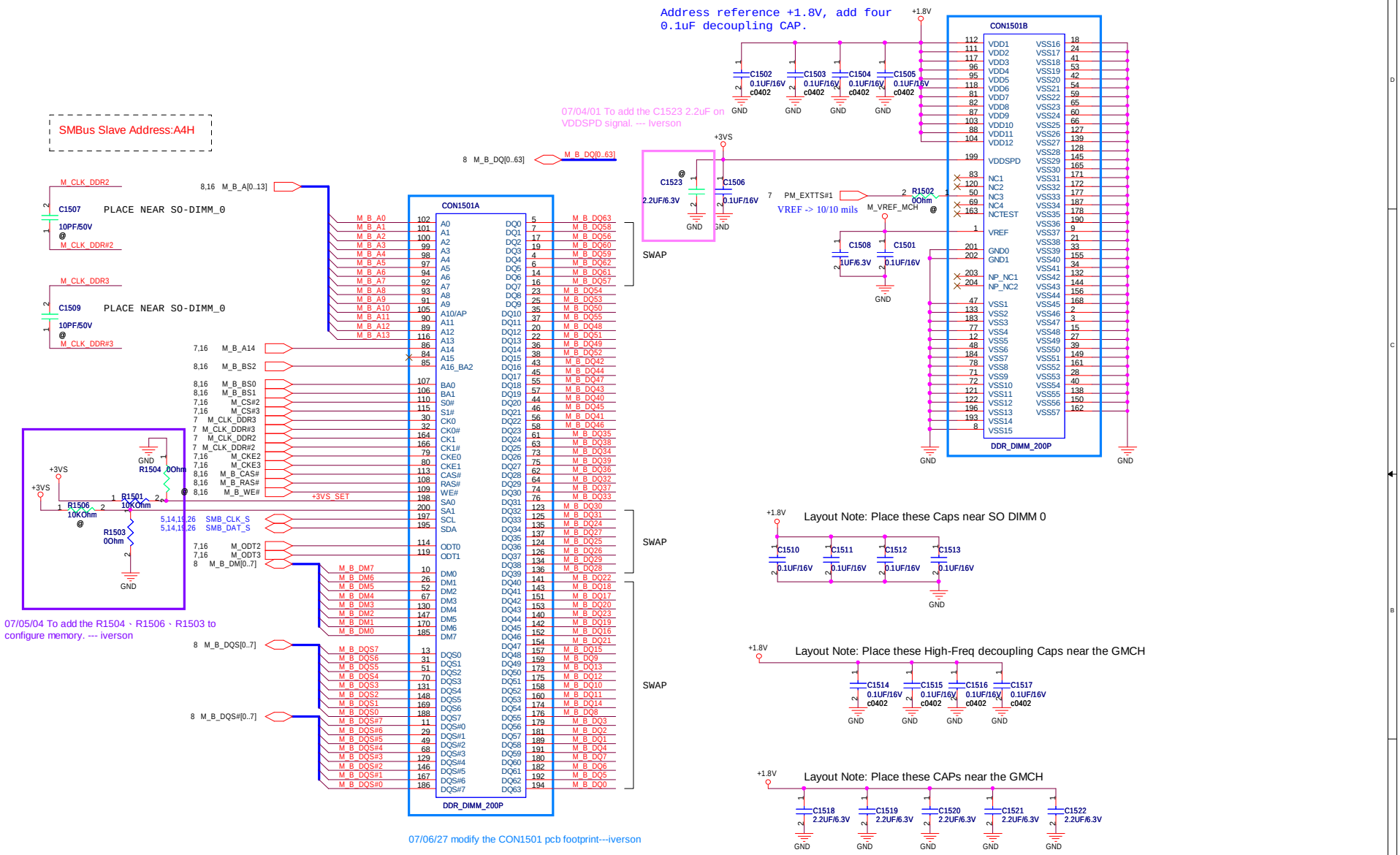


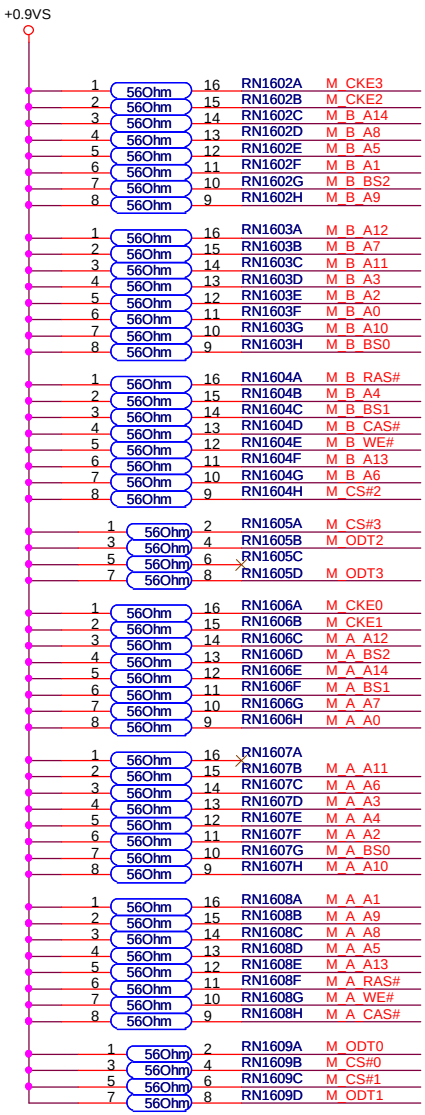
07/03/30 To change net name from VSYNC_5/HSYNC_5 into VSYNC_CON/HSYNC_CON---Feng

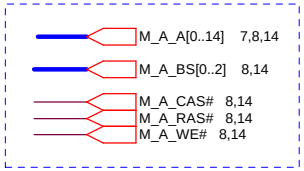


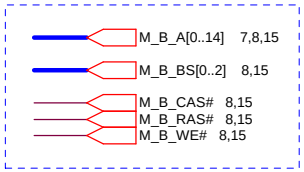
ASUSALPHA	Title : CRT	
ASUSALPHATeK COMPUTER INC.	Engineer: Feng Lin	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 13 of 66	

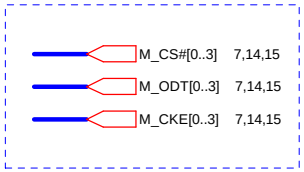


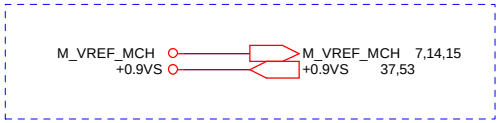


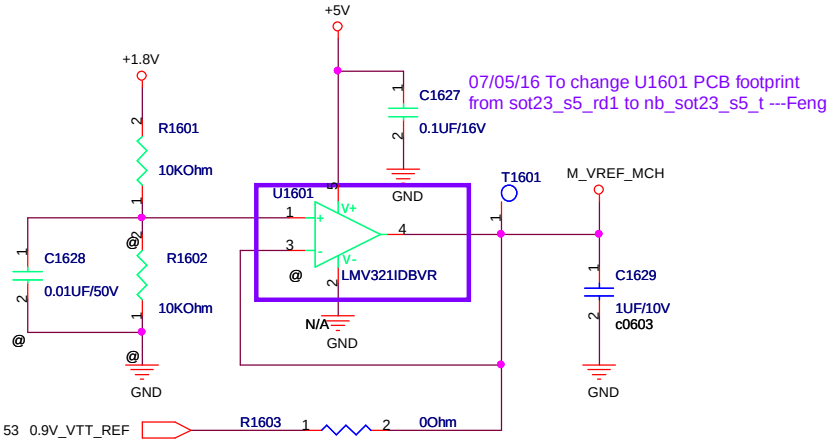


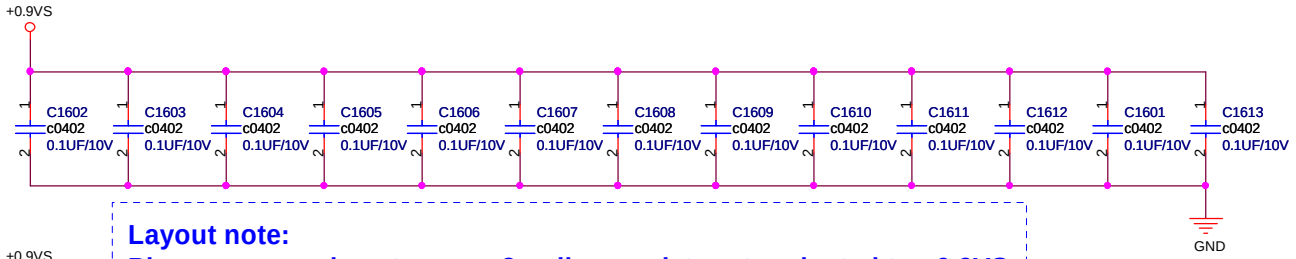




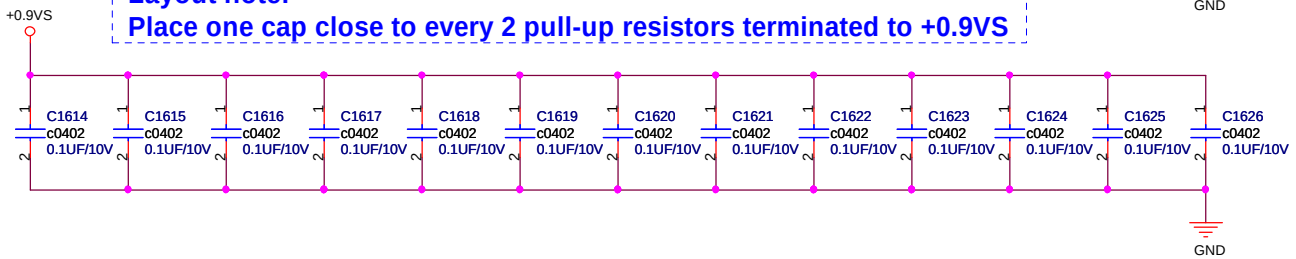








Layout note:
Place one cap close to every 2 pull-up resistors terminated to +0.9VS



<Variant Name>

ASUSALPHA

Title : DDR2 TERM

ASUSALPHATeK COMPUTER INC. Engineer: Feng Lin

Size	Project Name	Rev
Custom	TERESA20	2.0

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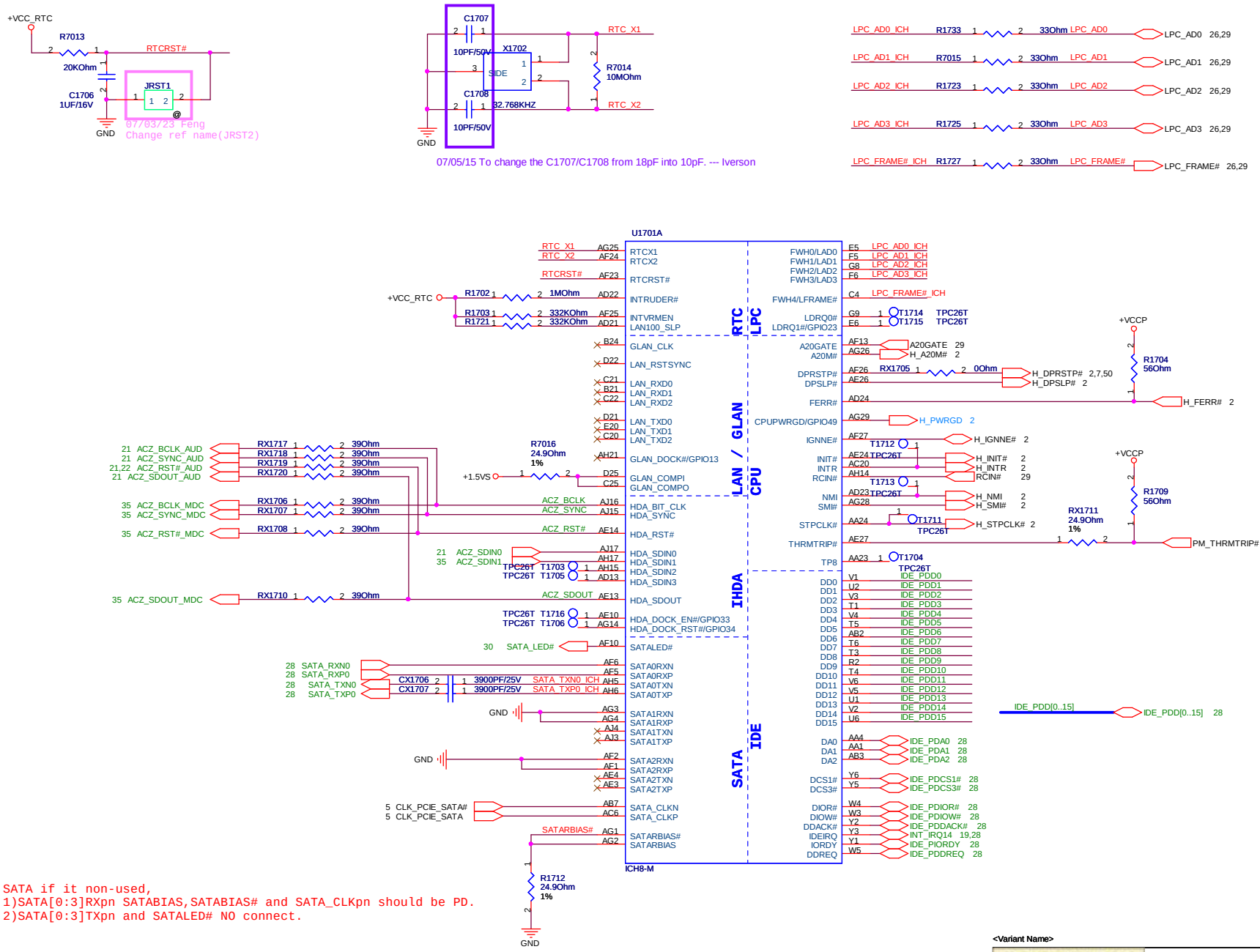
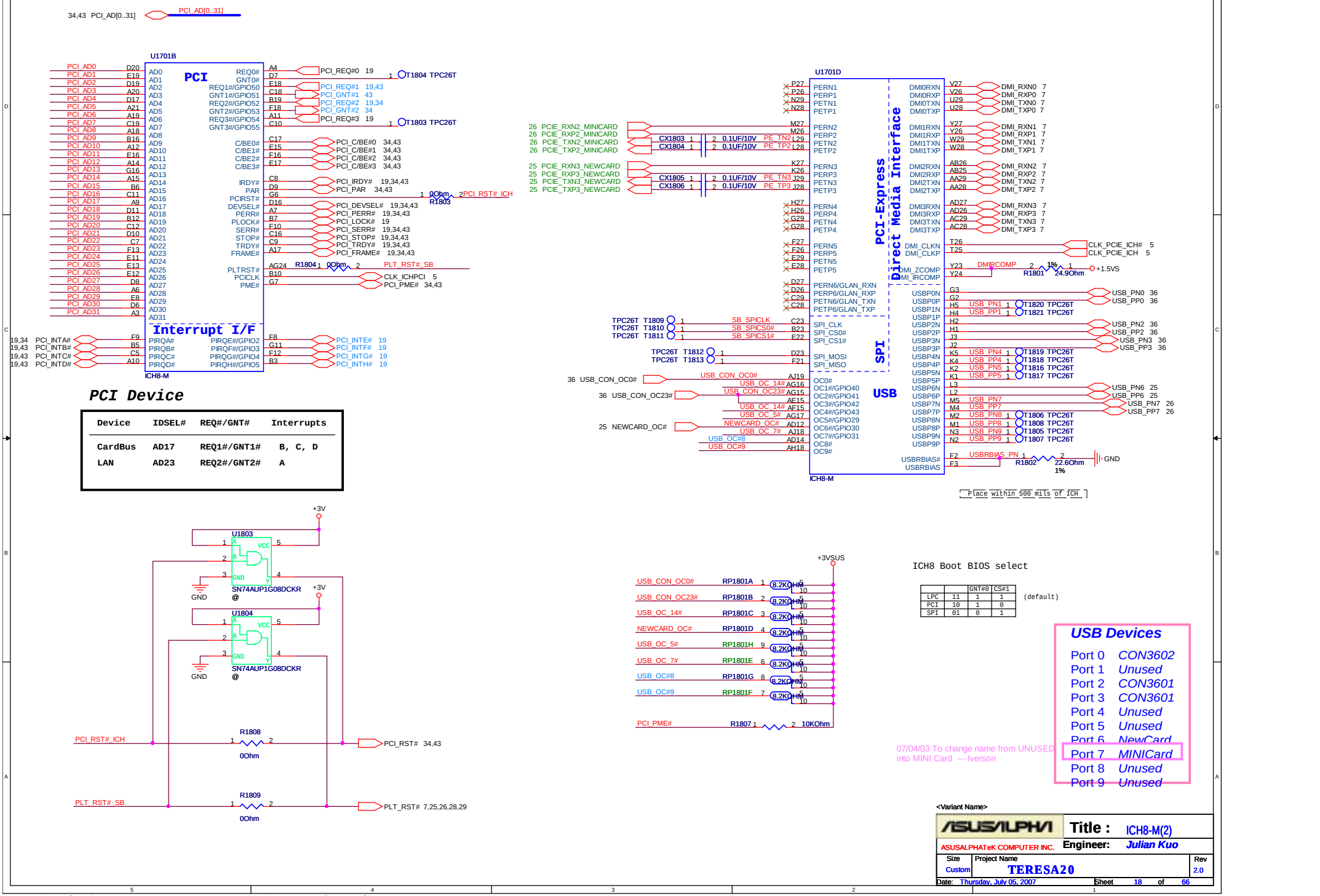




PCI Device

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD17	REQ1#/GNT1#	B, C, D
LAN	AD23	REQ2#/GNT2#	A

ICH8 Boot BIOS select

		GNT#0	CS#1	
LPC	11	1	1	(default)
PCI	10	1	0	
SPI	01	0	1	

USB Devices

Port 0	CON3602
Port 1	Unused
Port 2	CON3601
Port 3	CON3601
Port 4	Unused
Port 5	Unused
Port 6	NewCard
Port 7	MINICard
Port 8	Unused
Port 9	Unused

07/04/03 To change name from UNUSED into MINI Card --- Iverson

<Variant Name>

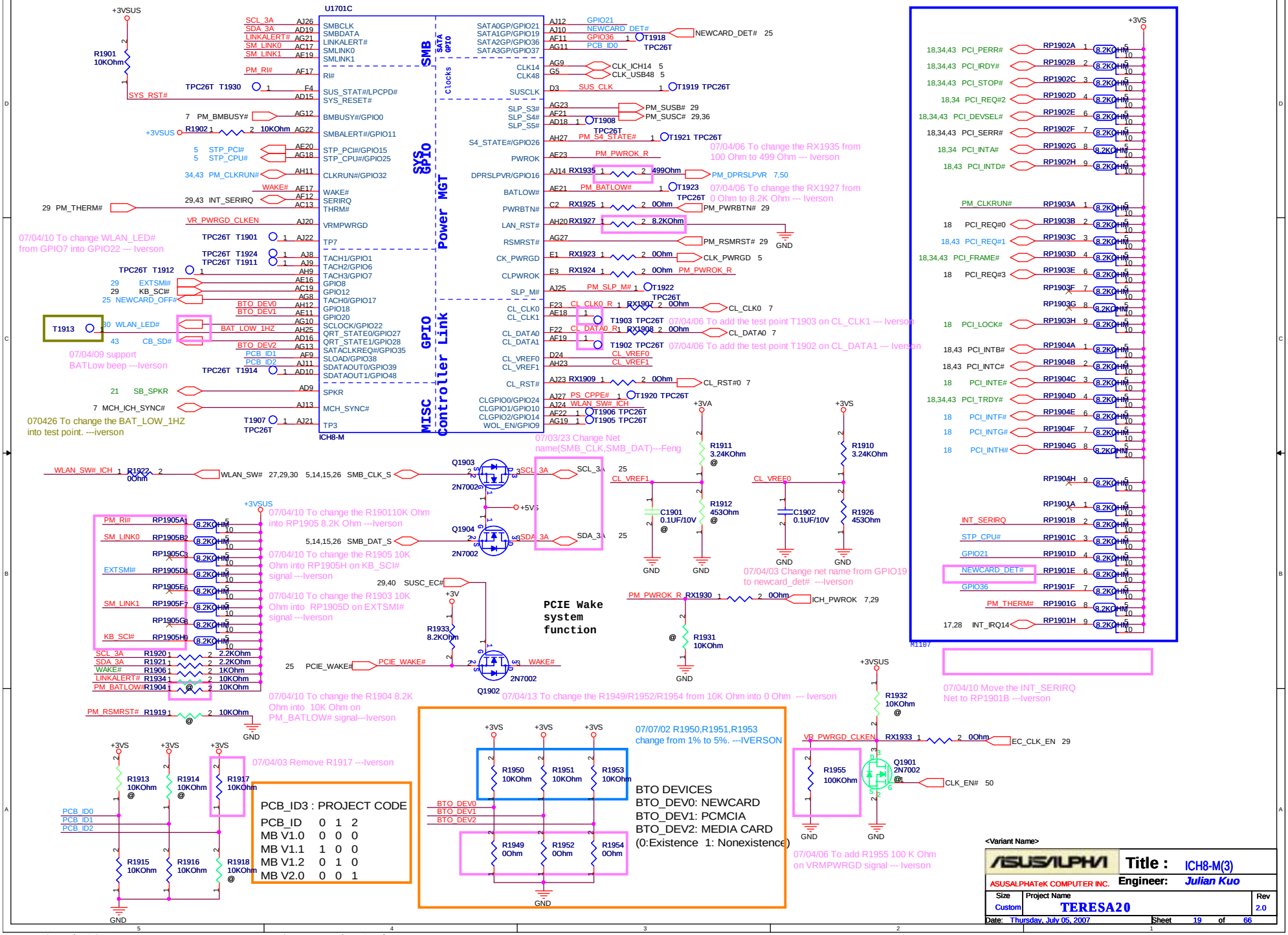
ASUSALPHA

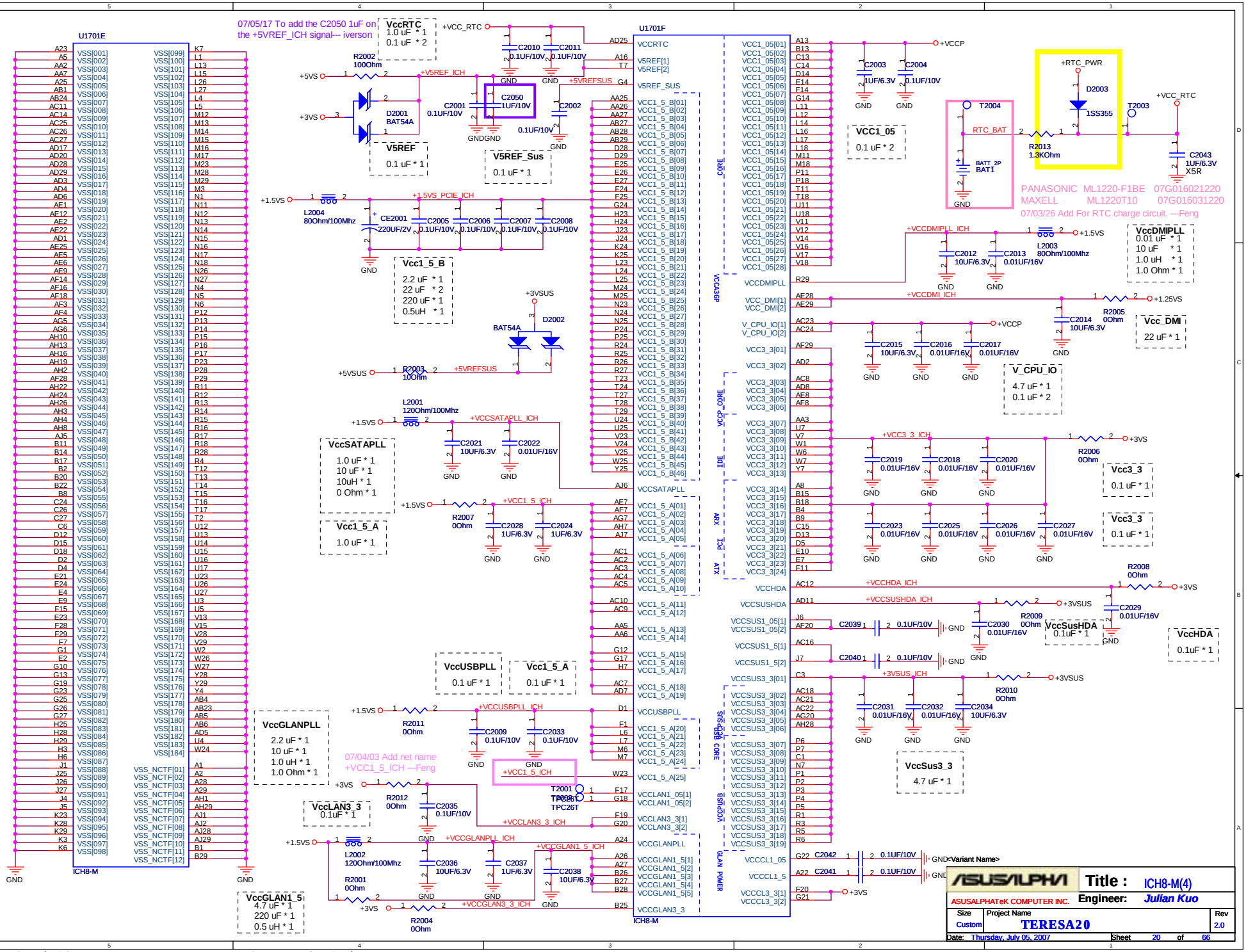
Title : ICH8-M(2)

ASUSALPHATeK COMPUTER INC. Engineer: Julian Kuo

Size	Project Name	Rev
Custom	TERESA20	2.0

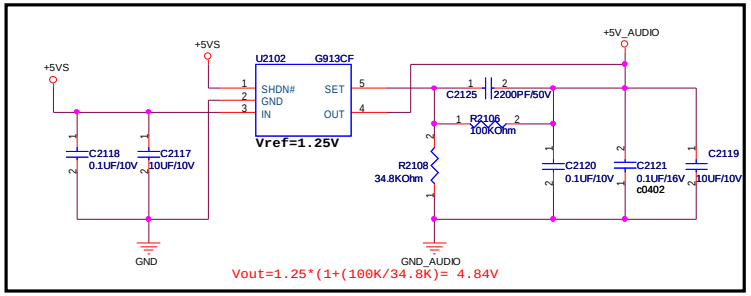
Date: Thursday, July 05, 2007 Sheet 18 of 66





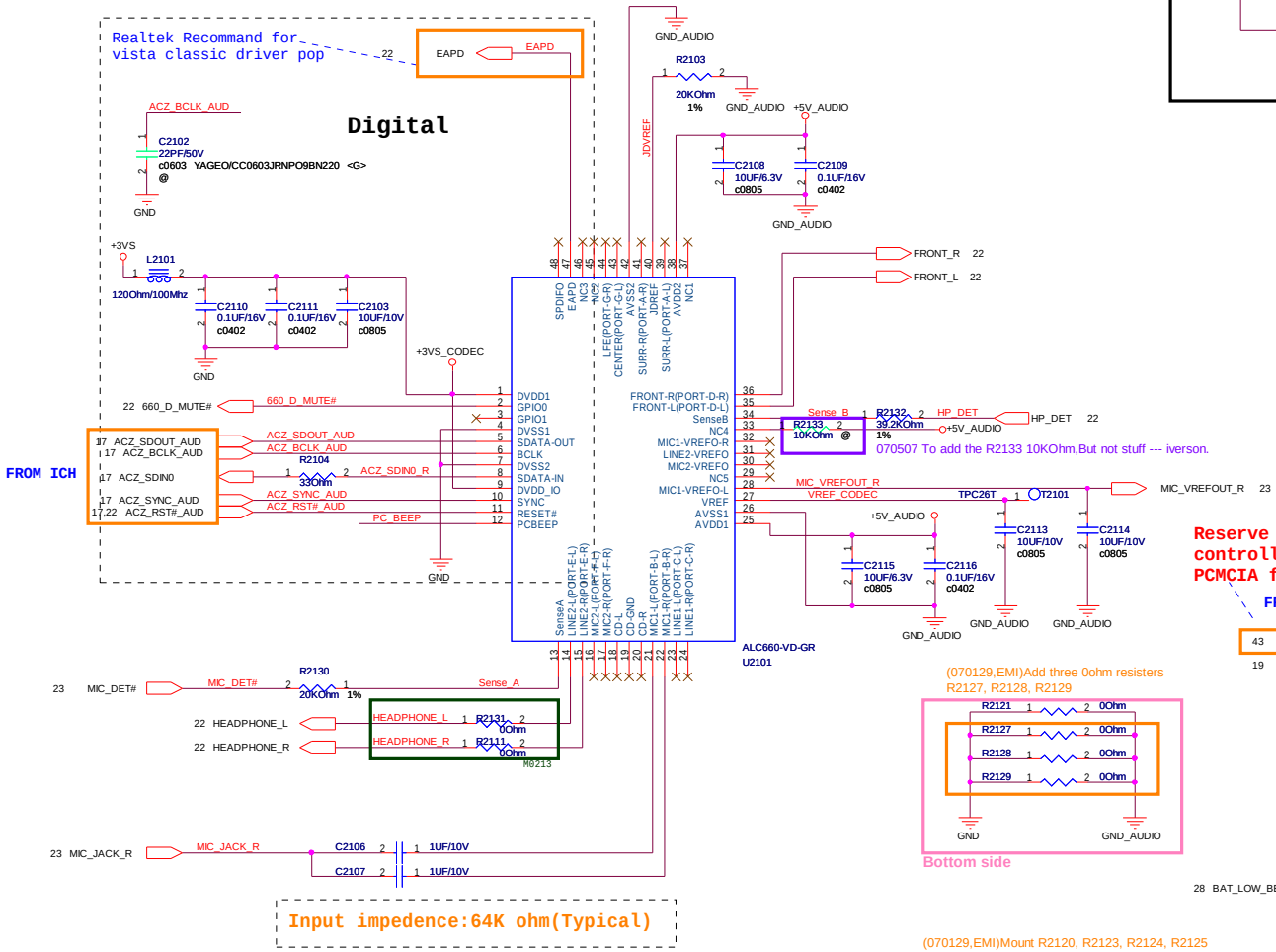
CODEC ALC660 REV:D

AUDIO POWER



Realtek Recommand for vista classic driver pop

Digital



FROM ICH

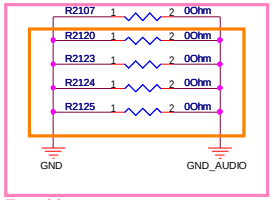
070507 To add the R2133 10KOhm,But not stuff --- iverson.

M0207

(070129,EMI)Add three 0ohm resisters R2127, R2128, R2129

Bottom side

(070129,EMI)Mount R2120, R2123, R2124, R2125

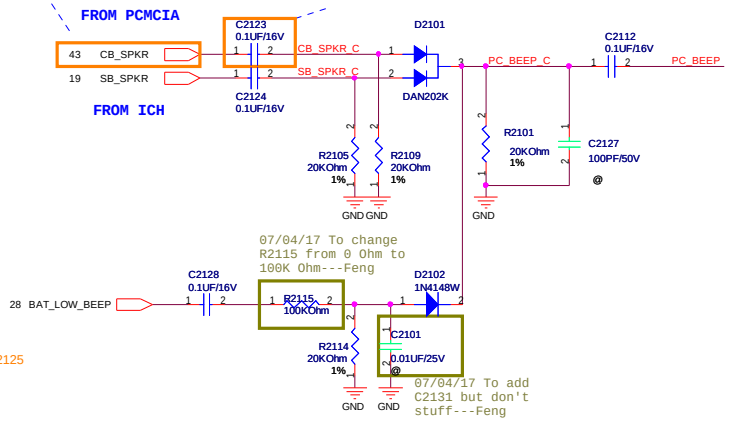


Top side

PC BEEP

Reserve for Cardbus controllor that has PCMCIA function.

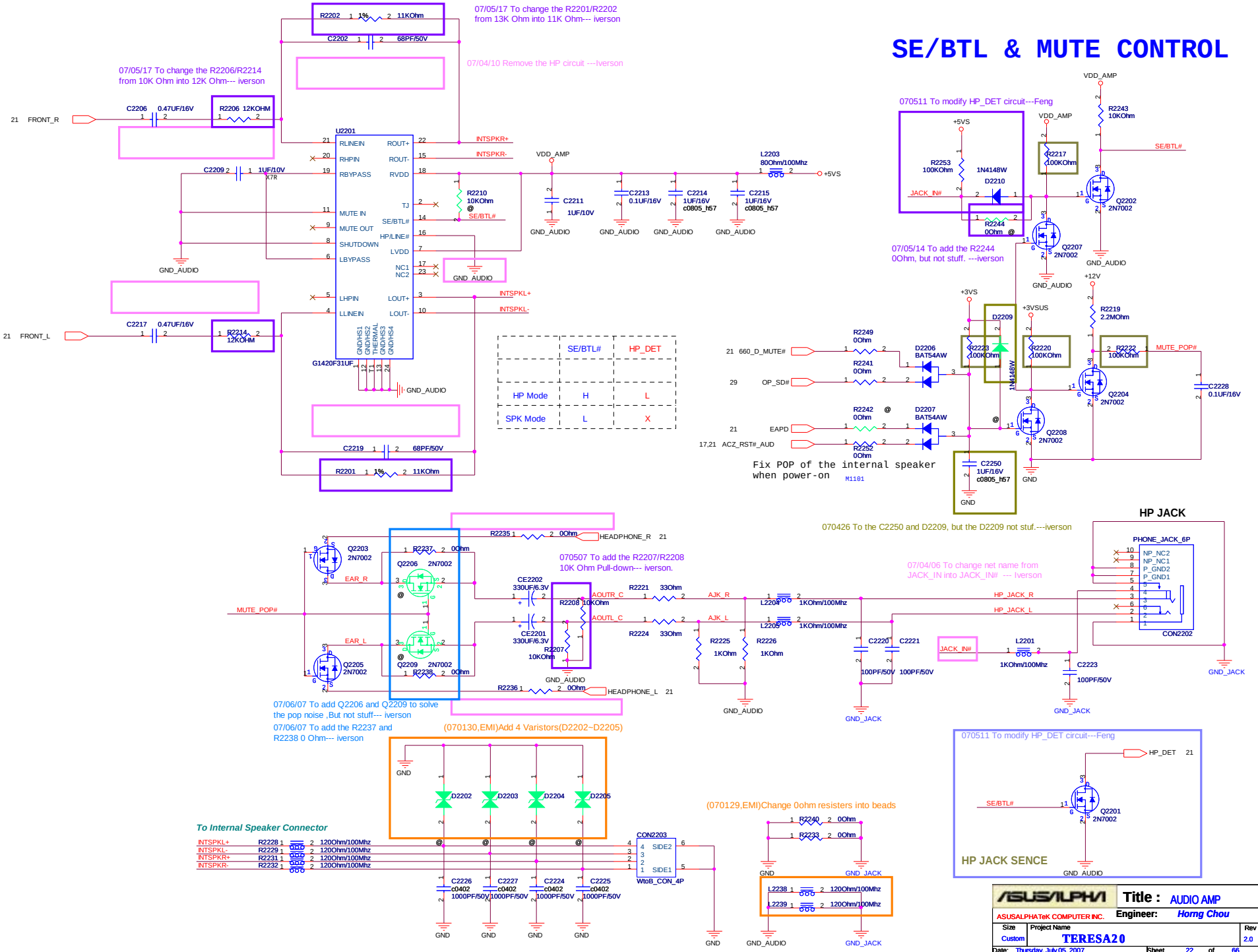
IF NO PCMCIA,UNMOUNT.



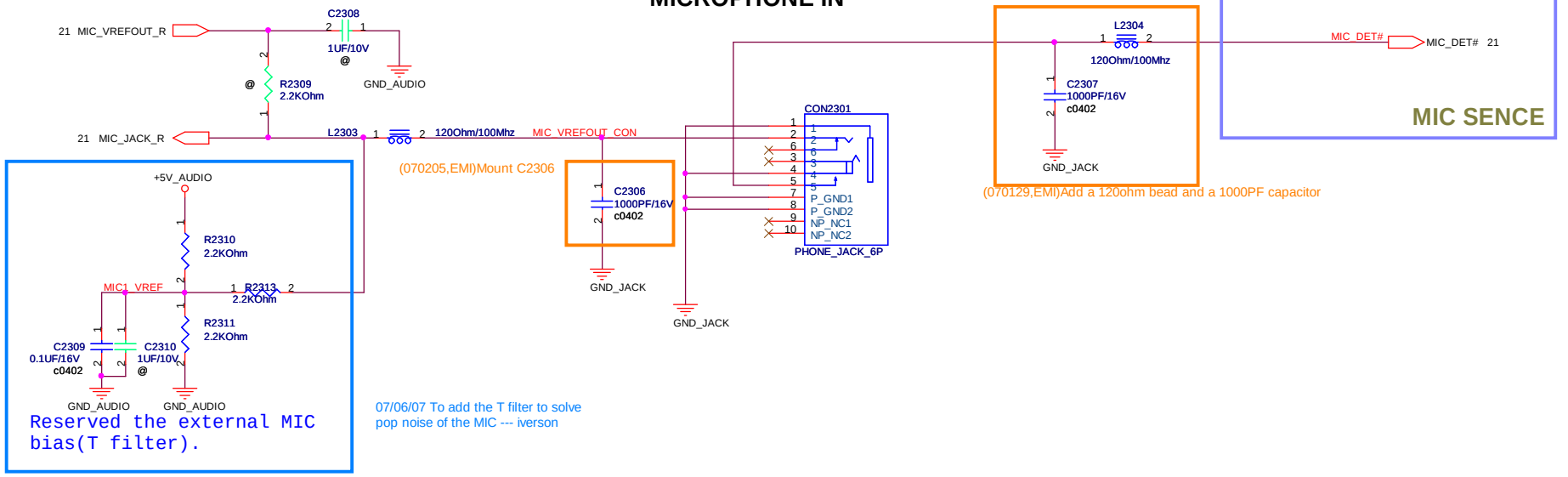
<Variant Name>

ASUSTeK COMPUTER INC. NB1	Title : CODEC ALC660(D)	
	Engineer: Feng	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 21 of 66	

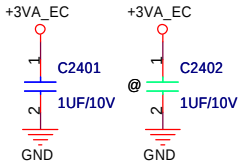
SE/BTL & MUTE CONTROL



MICROPHONE IN



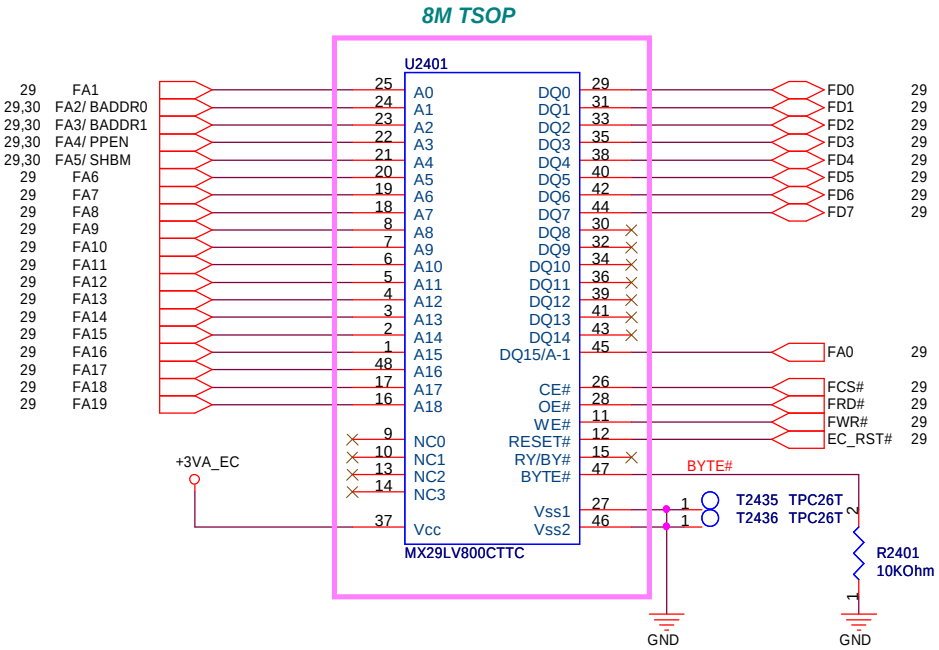
ASUSALPHA	Title : MIC JACK	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 23 of 66	



Note:

If you use 8M bits ROM, you need to connect FA19 to EC side.

For 8M bits ISA ROM



07/04/13 To change the U2401 from pn:05G001014110 into 05G001204043 --- Iverson

FD0	1	T2401 TPC26T
FD1	1	T2402 TPC26T
FD2	1	T2403 TPC26T
FD3	1	T2404 TPC26T
FD4	1	T2405 TPC26T
FD5	1	T2406 TPC26T
FD6	1	T2407 TPC26T
FD7	1	T2408 TPC26T
FA0	1	T2409 TPC26T
FA1	1	T2410 TPC26T
FA2/ BADDR0	1	T2411 TPC26T
FA3/ BADDR1	1	T2412 TPC26T
FA4/ PPEN	1	T2413 TPC26T
FA5/ SHBM	1	T2414 TPC26T
FA6	1	T2415 TPC26T
FA7	1	T2416 TPC26T
FA8	1	T2417 TPC26T
FA9	1	T2418 TPC26T
FA10	1	T2419 TPC26T
FA11	1	T2420 TPC26T
FA12	1	T2421 TPC26T
FA13	1	T2422 TPC26T
FA14	1	T2423 TPC26T
FA15	1	T2424 TPC26T
FA16	1	T2425 TPC26T
FA17	1	T2426 TPC26T
FA18	1	T2427 TPC26T
FA19	1	T2428 TPC26T
FCS#	1	T2429 TPC26T
FRD#	1	T2430 TPC26T
FWR#	1	T2431 TPC26T
EC_RST#	1	T2432 TPC26T
BYTE#	1	T2433 TPC26T
+3VA_EC	1	T2434 TPC26T

070507 To add test point on the ISA ROM --- iverson.

ASUSALPHA

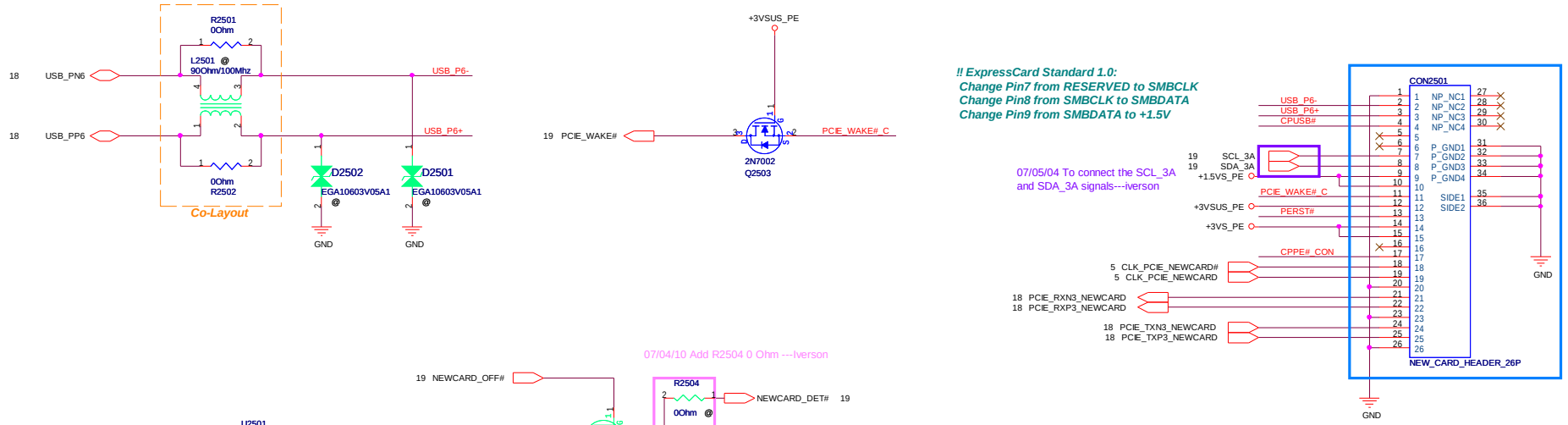
Title : ISA ROM

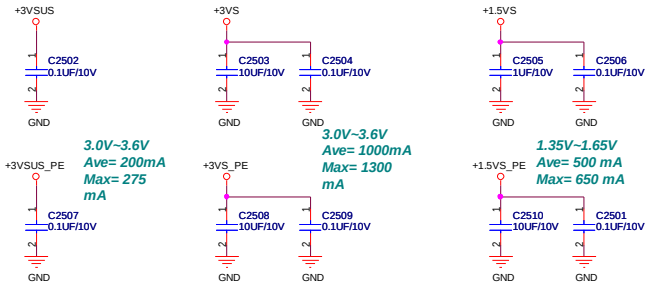
ASUSALPHATeK COMPUTER INC. **Engineer:** *Horng Chou*

Size	Project Name	Rev
Custom	TERESA20	2.0

Date: Thursday, July 05, 2007 Sheet 24 of 66

NewCard Header



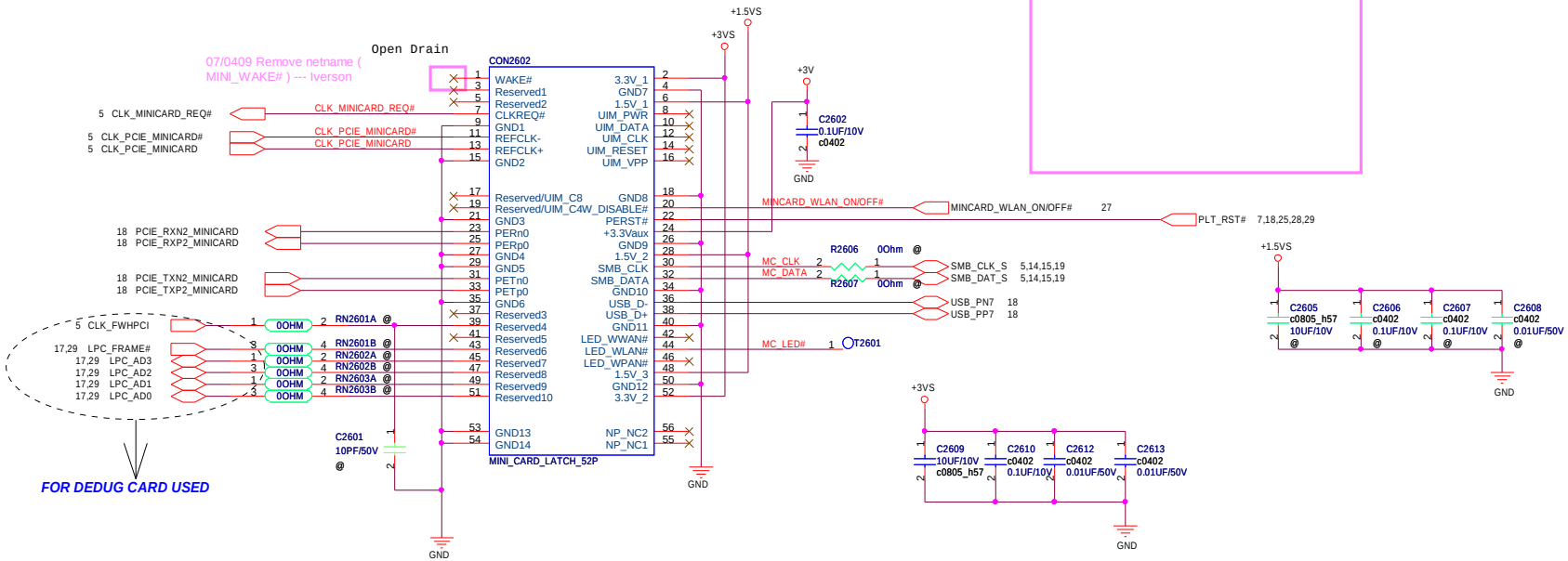


<Variant Name>

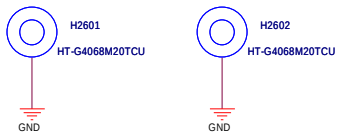
ASUSALPHA	Title : NEWCARD	
ASUSALPHATeK COMPUTER INC.	Engineer: Feng Lin	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 25 of 66	

07/04/09 Remove the PCIE Wake system function ---Iverson

MINI CARD CONNECTOR



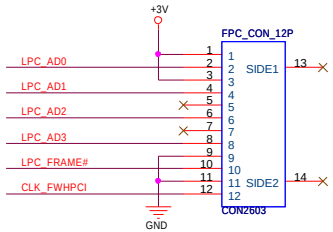
Instead of Mini-PCIE latch connecter.For cost down.



Power consumption of WLAN SPEC:

Vendor		ASKEY	ASKEY	ASKEY	Realtek
Chip Name		XB61	XB62	XB63	RTL8187
		WLL3140	WLL4080	WLL3141	WN6301L
Transmit Mode	11.a		550mA		
	11.b	525mA	560mA	2330mW	445mA
	11.g	560mA	550mA	2155mW	450mA
	11.n				
Receive Mode	11.a		280mA		
	11.b	430mA	270mA	1089mW	310mA
	11.g	460mA	280mA	1122mW	330mA
	11.n				
Sleep Mode Current		220mA	20mA		325mA
Supplied Voltage(VCC)	MIN	3.0V	3.0V	3.0V	3.3V-5%
	TYP	3.3V	3.3V	3.3V	3.3V
	MAX	3.6V	3.6V	3.6V	3.3V+5%

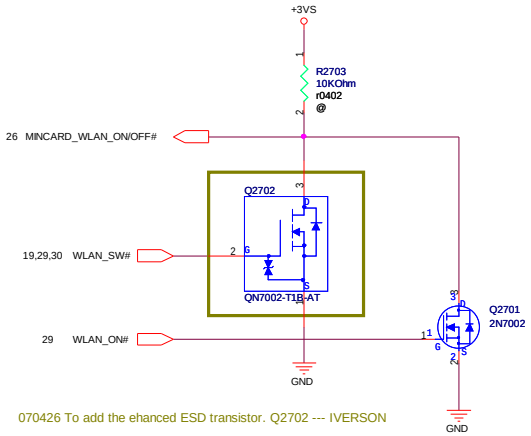
Debug Card CON



ASUSALPHA	Title : MINI PCIEX/DEBUG CON	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 26 of 66	

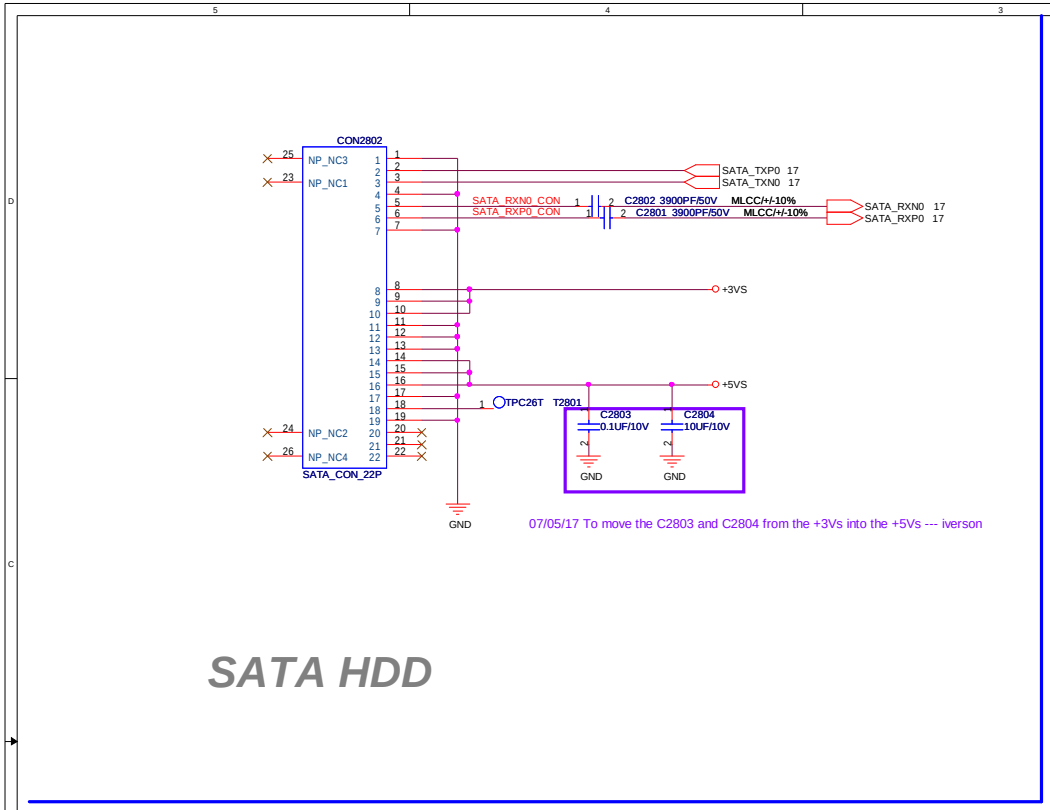
For Side SW

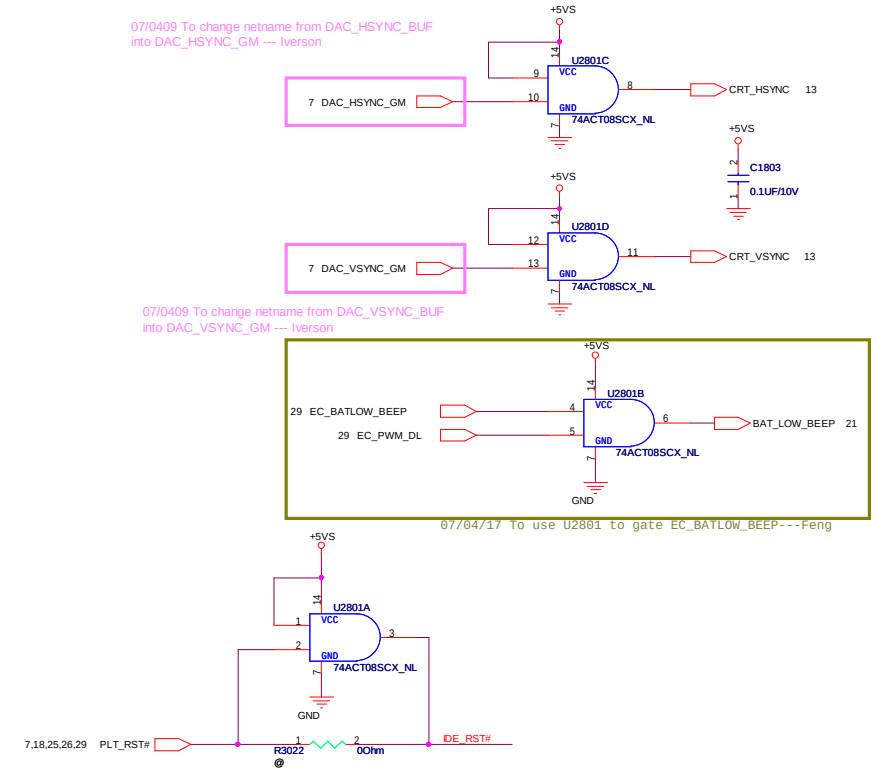
WLAN ON/OFF Control

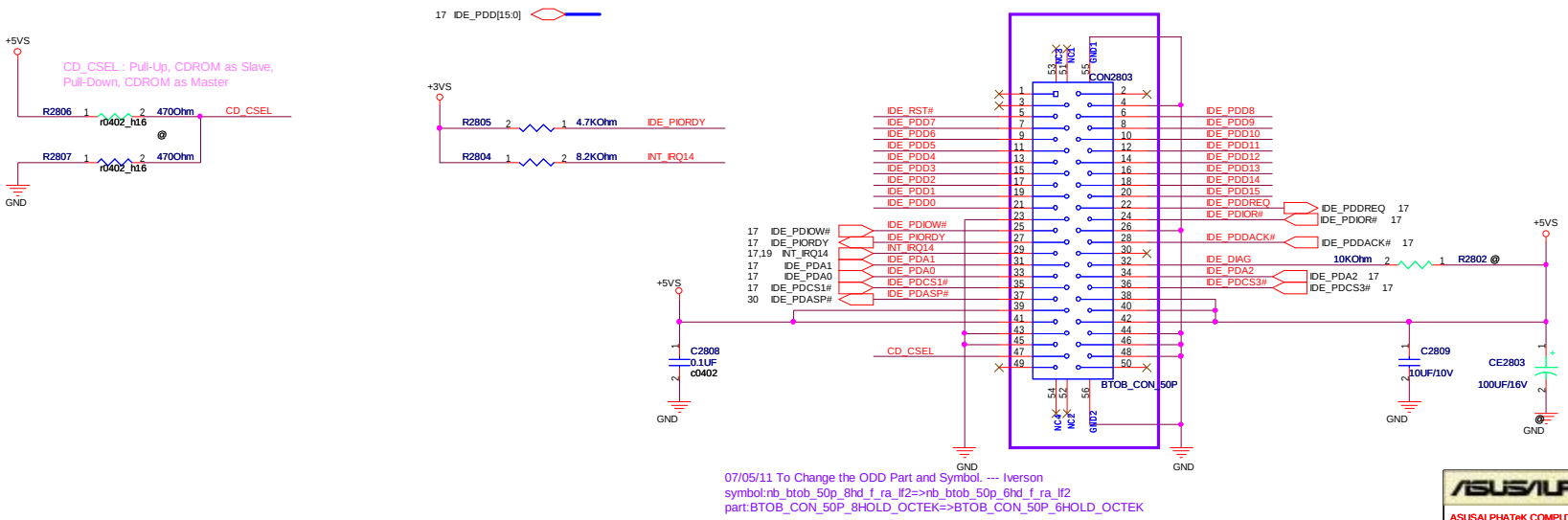


070426 To add the ehanced ESD transistor. Q2702 --- IVERSON

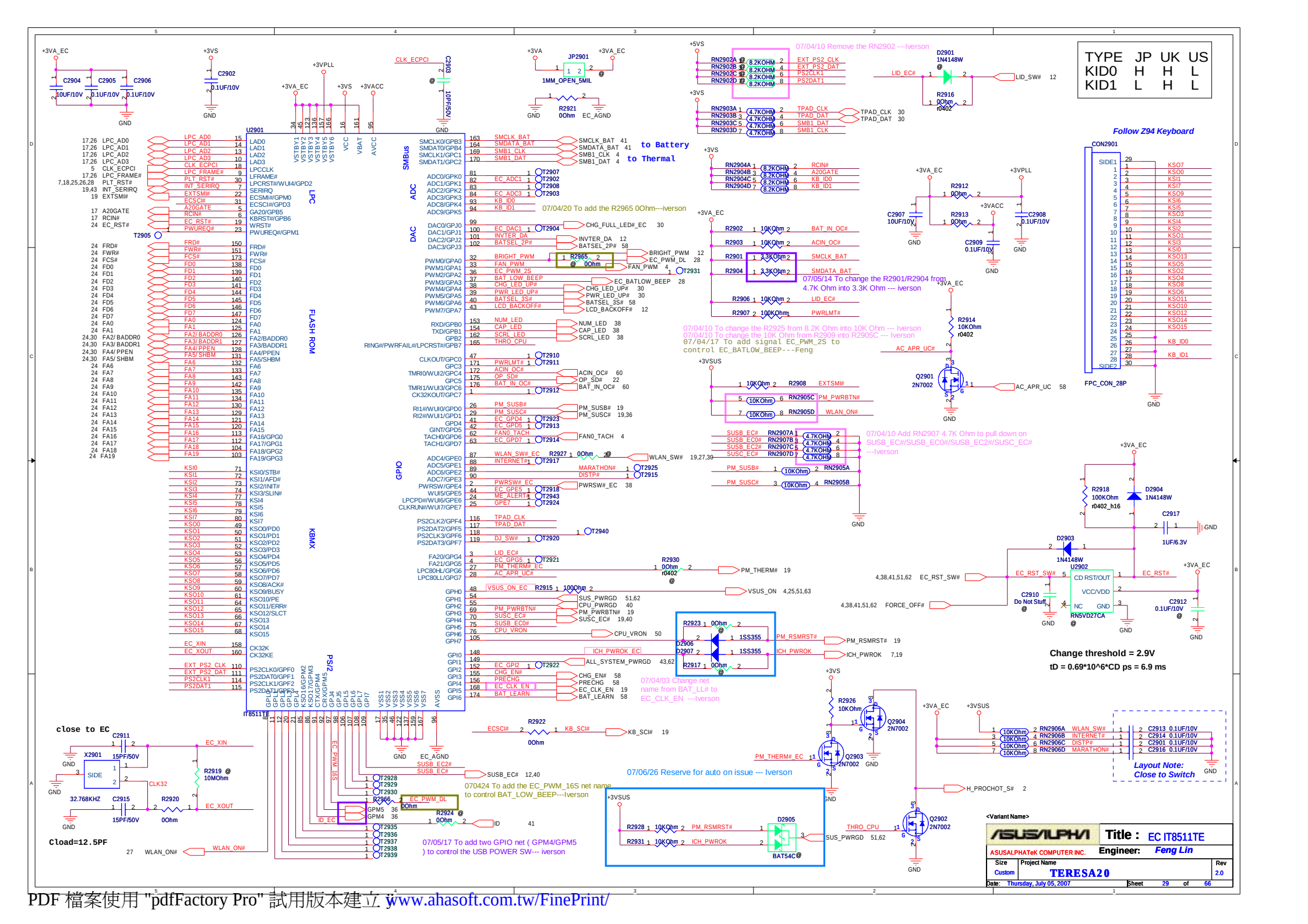
ASUSALPHA	Title :	WLAN CONTROL
ASUSALPHATeK COMPUTER INC.	Engineer:	Horng Chou
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 27 of 66	







ASUSALPHA	Title :	PATA-SATA & ODD	
ASUSALPHATeK COMPUTER INC.	Engineer:	Horng Chou	
Size: Custom	Project Name: TERESA20		Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 28 of 66		



EC Hardware Strap

Strap value sampled after VSTBY power up reset

PNPCFG base address set by SWCBAHR/SWCBALR

+3VA_EC
R3002 @ 10KOhm r0402
FA2/ BADDR0
FA2/ BADDR0 24,29
R3006 10KOhm r0402
GND

+3VA_EC
R3003 10KOhm r0402
FA3/ BADDR1
FA3/ BADDR1 24,29
R3007 @ 10KOhm r0402
GND

BADDR[1:0]

No pull up:	The register pair to access PNPCFG is 002Eh and 002Fh.
Ext 10K up on BADDR0:	The register pair to access PNPCFG is 004Eh and 004Fh.
Ext 10K up on BADDR1:	The register pair to access PNPCFG is determined by EC domain registers SWCBALR and SWCBAHR.

07/04/10 Remove the Adaptor --- Iverson

Share Memory

+3VA_EC
R3010 10KOhm r0402
FA5/ SHBM
FA5/ SHBM 24,29
R3013 @ 10KOhm r0402
GND

SHBM

No pull up:	Disable shared memory with host BIOS
Ext 10K up:	Enable shared memory with host BIOS

+3VA_EC
R3001 @ 10KOhm r0402
FA4/ PPEN
FA4/ PPEN 24,29
R3014 10KOhm r0402
GND

PPEN

No pull up:	Normal
Ext 10K up:	KBS interface pins are switched to parallel port interface for in-system programming.

07/04/10 Remove the Adaptor --- Iverson

LED Board Interface

(070131,EMI)New addition for EMI
(070205)mount

D3009
0603-050E101NP-LF
GND
+5VSUS
+5V
C3008 0.01UF/25V
C3007 0.1UF/10V
GND
HDD_LED#
802_LED#_R
CHG_LED#_R
PWR_LED#_R
SUSPEND_LED#
L3024 L3025 L3026 L3027 L3028 L3029 L3030 L3031 L3032
220Ohm/100Mhz
CON3001
SIDE2
SIDE1
FPC_CON_12P
+5VS
+5VS_TP
L3002
80Ohm/100Mhz
19,27,29 WLAN_SW#
WLAN_SW#
CHG_FULL_LED#
C3006 0.1UF/10V

Touchpad Board Interface

+5VS_TP
29 TPAD_DAT
29 TPAD_CLK
CON3002
SIDE2
SIDE1
FPC_CON_6P
C3009 0.1UF/10V
C3011 100PF/50V
C3012 100PF/50V
GND
(070129,EMI)add two 100PF capacitors

HDD LED

+3VS
+5VS
R3019 10KOhm
R3020 10KOhm @
D3005
17 SATA_LED#
28 IDE_PDASP#
HDD_LED#
DAP202K @
D3008
1N4148W

CHARGE LED

+5VSUS
R3015 10KOhm
CHG_LED#_R
ORANGE
Q3003
QN7002-T1B-AT
T3001
Q3001 2N7002
29 CHG_LED_UP#
GND
07/04/09 Remove Solution 1 ---Iverson
29 PWR_LED_UP#
CHG_FULL_LED#
GREEN
Q3005
QN7002-T1B-AT
R3023
10KOhm
+5VSUS
29 CHG_FULL_LED#_EC
Q3007 2N7002

POWER LED

070426 To remove the D3006, and To add the Q3011. --- IVERSON

+5V
R3017 10KOhm
PWR_LED#_R
GREEN
Q3008
QN7002-T1B-AT
37 SUSB
Q3011 2N7002
Q3002 2N7002
ORANGE
SUSPEND_LED#
Q3010
QN7002-T1B-AT

WLAN LED

+5VS
802_LED#_R
R3016 10KOhm
Q3009
QN7002-T1B-AT
19 WLAN_LED#
Q3004 2N7002

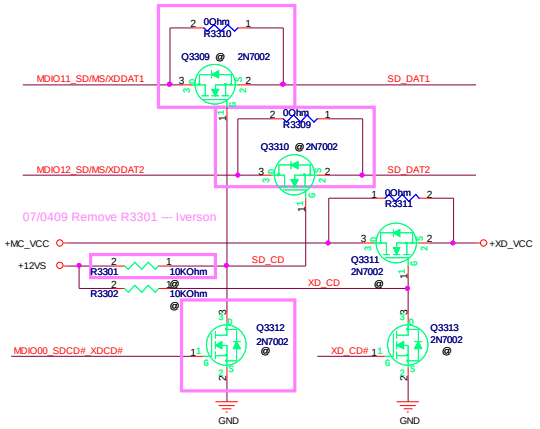
070426 To add the ehanced ESD transistor.
Q3003.Q3005.Q3008.Q3009.Q3010 --- IVERSON

ASUSALPHA	Title : EC IT8511/LED&TP CON.	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 30 of 66	

Title	<Title>		
Size A	Document Number <Doc>		Rev <RevCode>
Date: Thursday, July 05, 2007		Sheet 31 of 66	

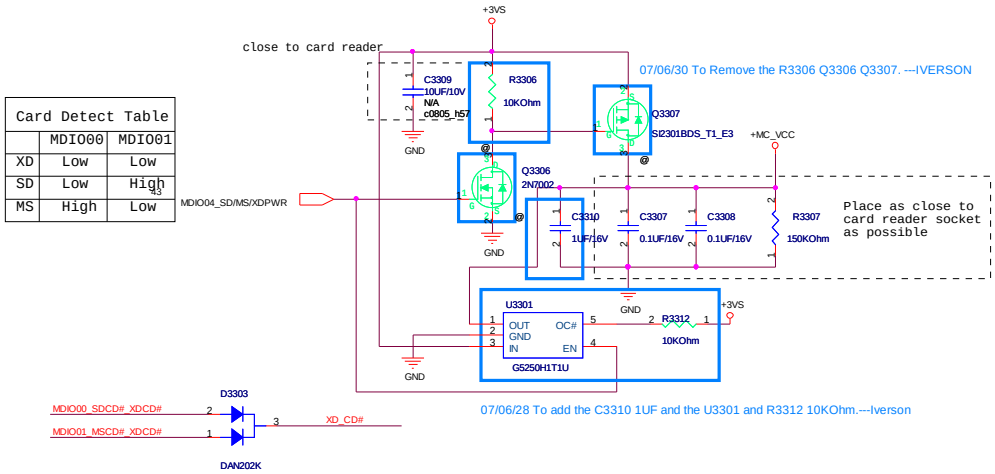
Title	<Title>	
Size A	Document Number <Doc>	Rev <RevCode>
Date: Thursday, July 05, 2007	Sheet 32 of 66	

Name	Drive	Name	Drive
MDIO00	I - PU	MDIO10	I/O - PU
MDIO01	I - PU	MDIO11	I/O - PU
MDIO02	O - PU	MDIO12	I/O - PU
MDIO03	I - PU	MDIO13	I/O - PU
MDIO04	O - 3V	MDIO14	I/O - PU
MDIO05	O - 3V	MDIO15	I/O - PU
MDIO06	O - 3V	MDIO16	I/O - PU
MDIO07	I - 3V	MDIO17	I/O - PU
MDIO08	I/O - PU	MDIO18	I/O - PU
MDIO09	I/O - PU	MDIO19	I/O - PU



07/04/06 Add R3310 0 Ohm between MDIO11_SD/MS/XDDAT1 and SD_DAT1.
Add R3311 0 Ohm between MDIO12_SD/MS/XDDAT2 and SD_DAT2.
Remove Q3309 Q3310 Q3312 --- Iverson

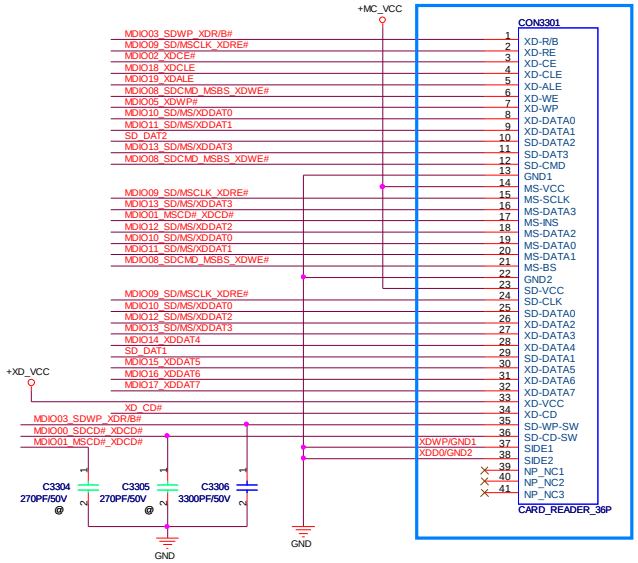
Card Detect Table		
	MDIO00	MDIO01
XD	Low	Low
SD	Low	High
MS	High	Low



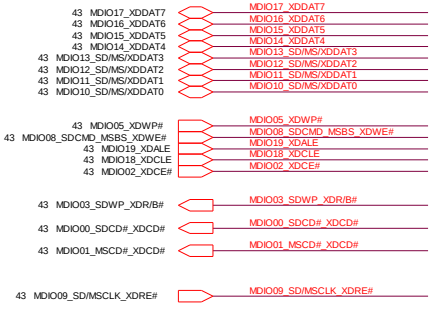
07/06/30 To Remove the R3306 Q3306 Q3307. ---IVERSON

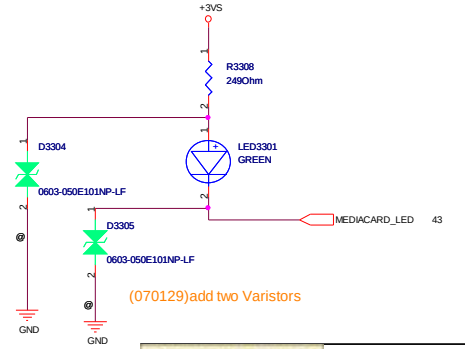
07/06/28 To add the C3310 1UF and the U3301 and R3312 10KOhm.---Iverson

MEDIA CARD SLOT



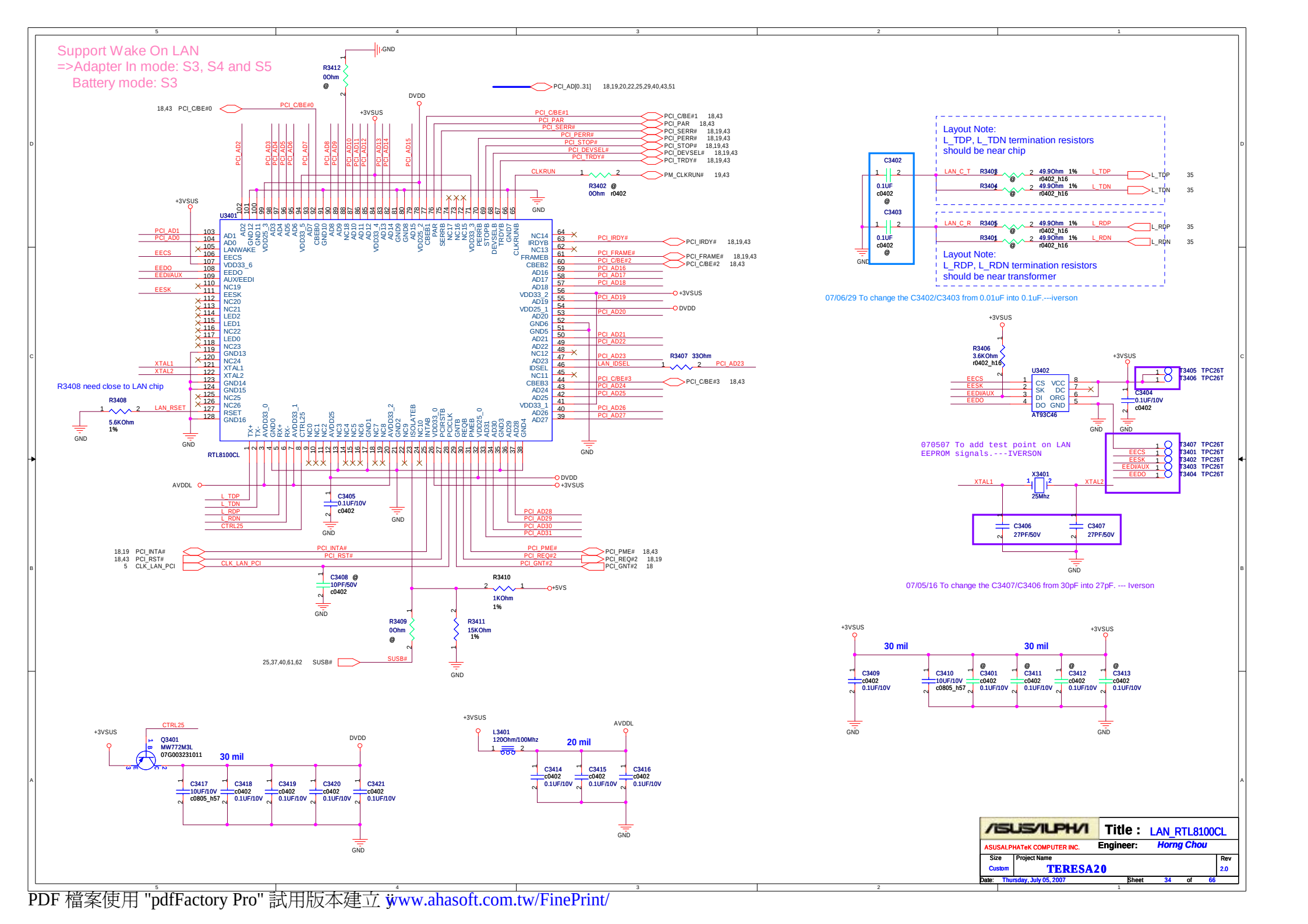
07/06/26 Modify CON3301 PCB footprint ---iverson





(070129)add two Varistors

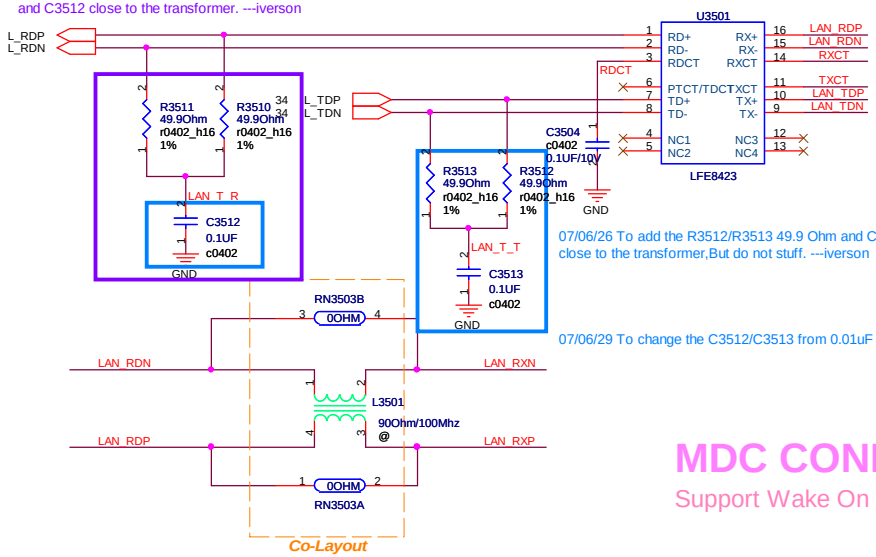
ASUSALPHA	Title : MEDIA CARD SLOT	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 33 of 66	



LAN PORT

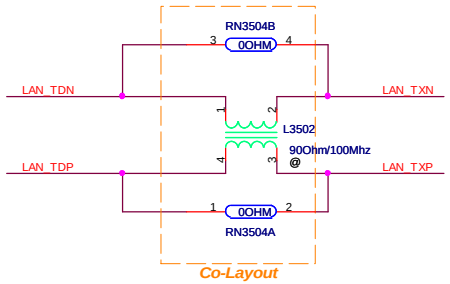
TRANSFORMER 10/100MB

07/05/14 To add the R3510/R3511 49.9 Ohm and C3512 close to the transformer. ---iverson

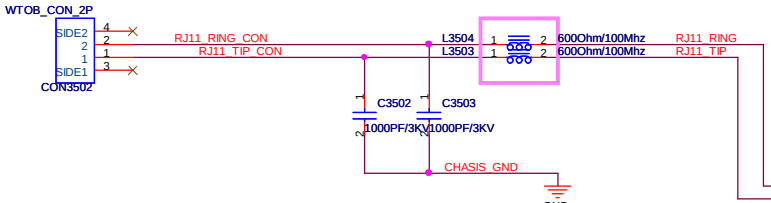


07/06/26 To add the R3512/R3513 49.9 Ohm and C3513 close to the transformer,But do not stuff. ---iverson

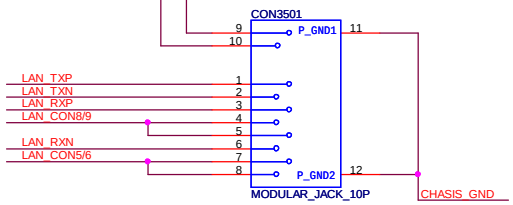
07/06/29 To change the C3512/C3513 from 0.01uF into 0.1uF.---iverson

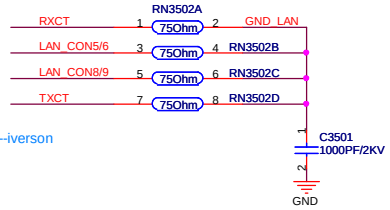


07/04/10 To change the L3504/L3503 from 1K Ohm/100M Hz into 600 Ohm/100M Hz by EMI request. --- Iverson



RJ11&RJ45



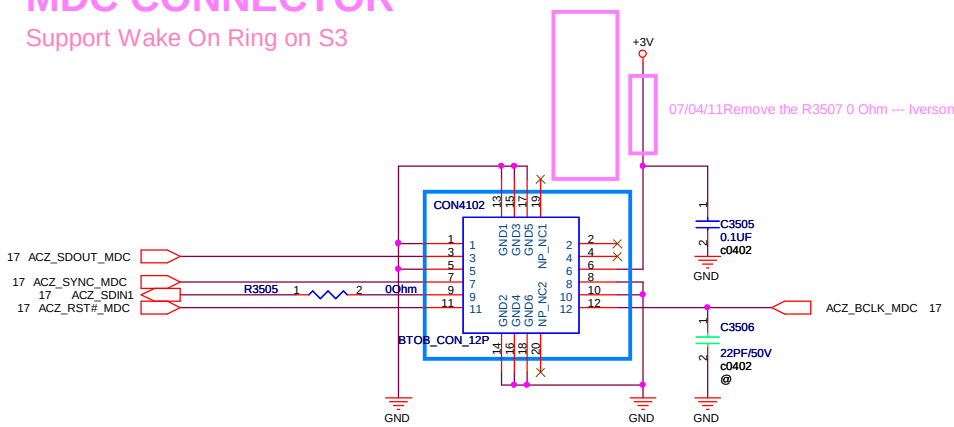


MDC CONNECTOR

Support Wake On Ring on S3

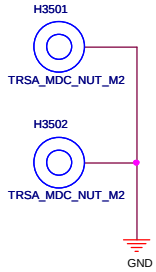
07/04/06 Remove R3506 0 ohm--- Iverson

07/04/11Remove the R3507 0 Ohm --- Iverson

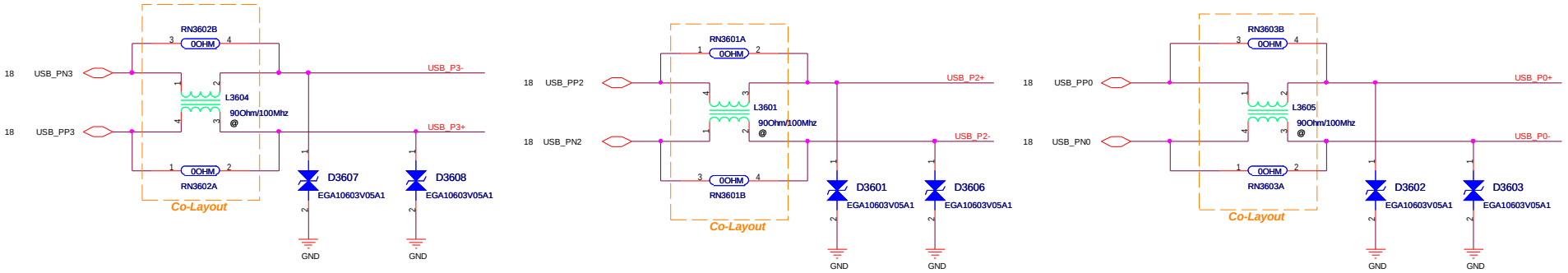


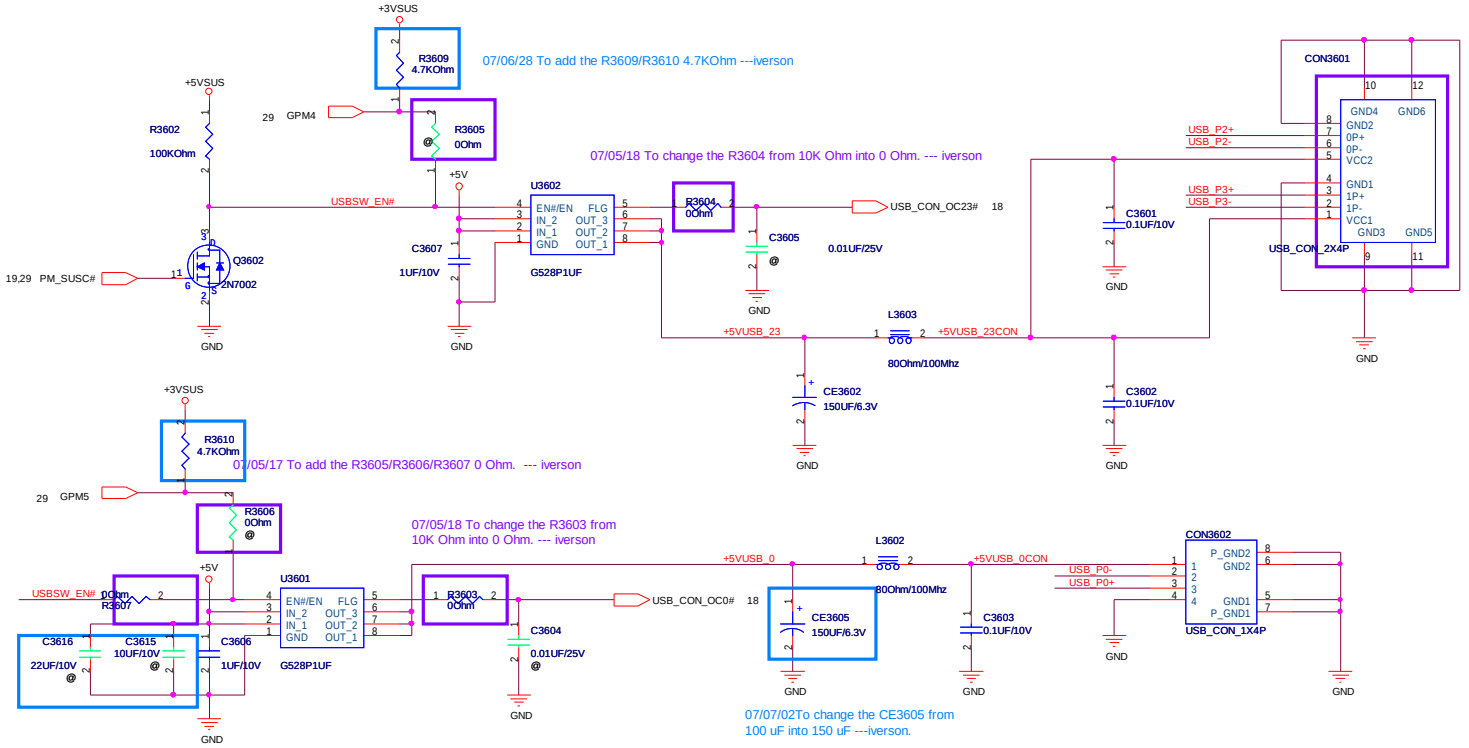
07/06/26 Modify the CON4102 PCB footprint --- iverson

B:MDC NUT

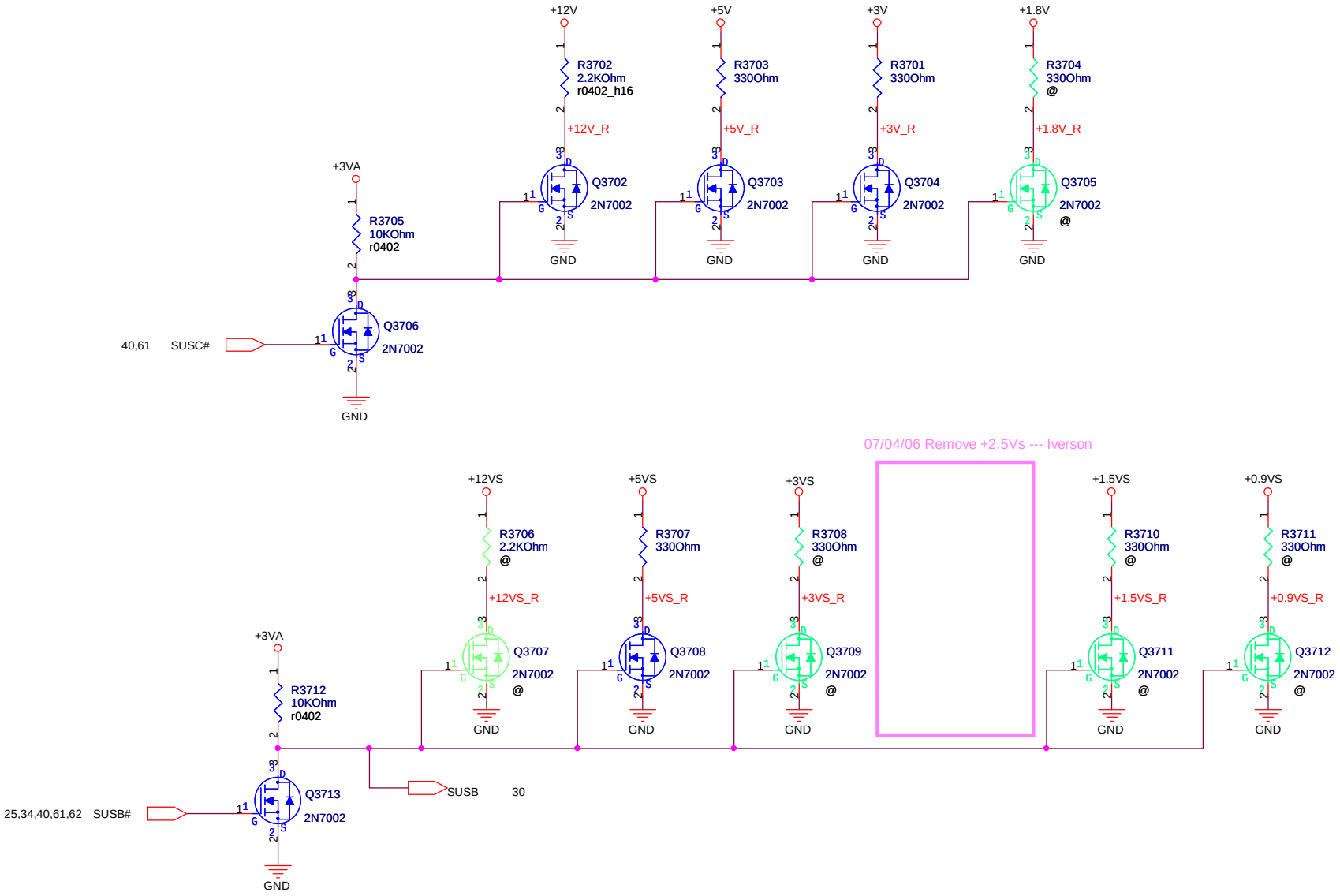


ASUSALPHA	Title : RJ45/RJ11/MDC	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 35 of 66	





ASUSALPHA	Title :	USB CONN x3
ASUSALPHATeK COMPUTER INC.	Engineer:	Horng Chou
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 36 of 66	



ASUSALPHA

Title : Discharge Circuit

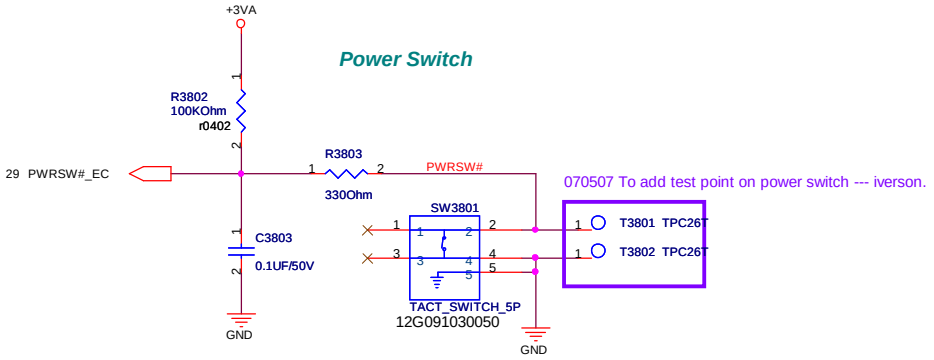
ASUSALPHATeK COMPUTER INC. Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA20	2.0

Date: Thursday, July 05, 2007 Sheet 37 of 66

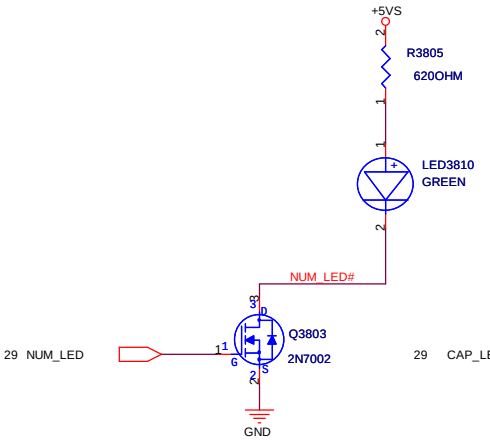
Main Board SW & LED

Power Switch

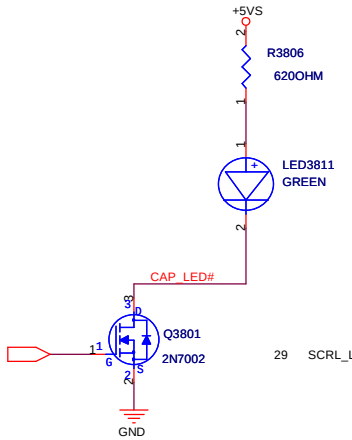


070507 To add test point on power switch --- iverson.

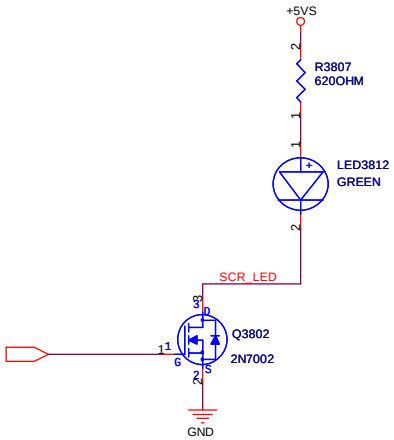
NUMBER LOCK LED



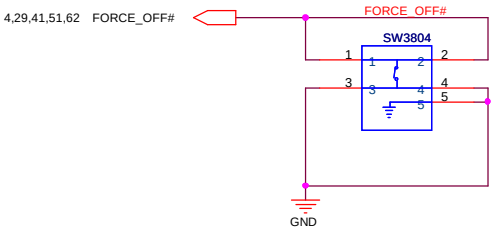
CAPS LOCK LED



SCROLL LOCK LED

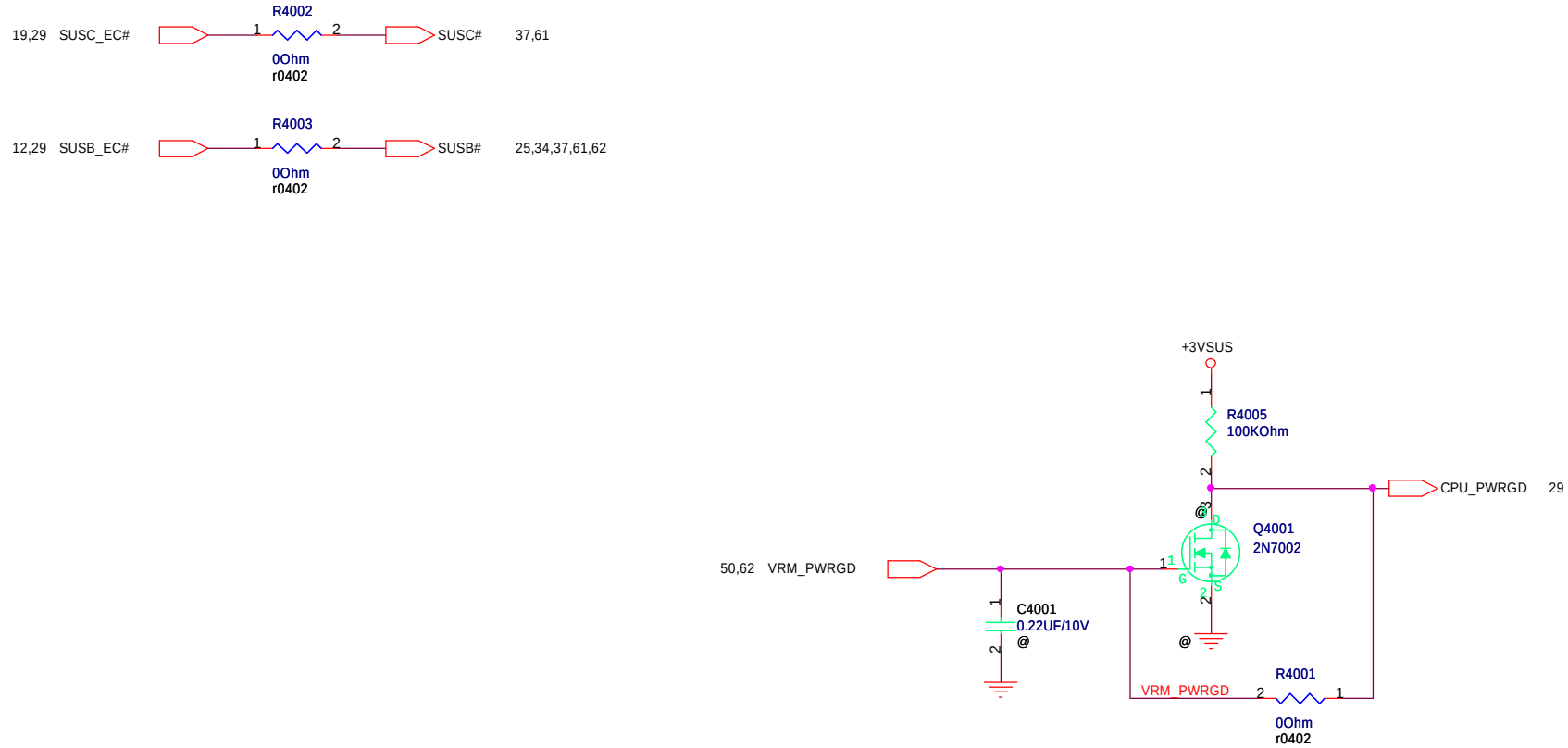


Reset Switch



ASUSALPHA	Title : SW/LED	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 38 of 66	

Title	<Title>		
Size A	Document Number <Doc>		Rev <RevCode>
Date: Thursday, July 05, 2007		Sheet 39 of 66	



<Variant Name>

ASUSALPHA

Title : POWER-ON SEQ.

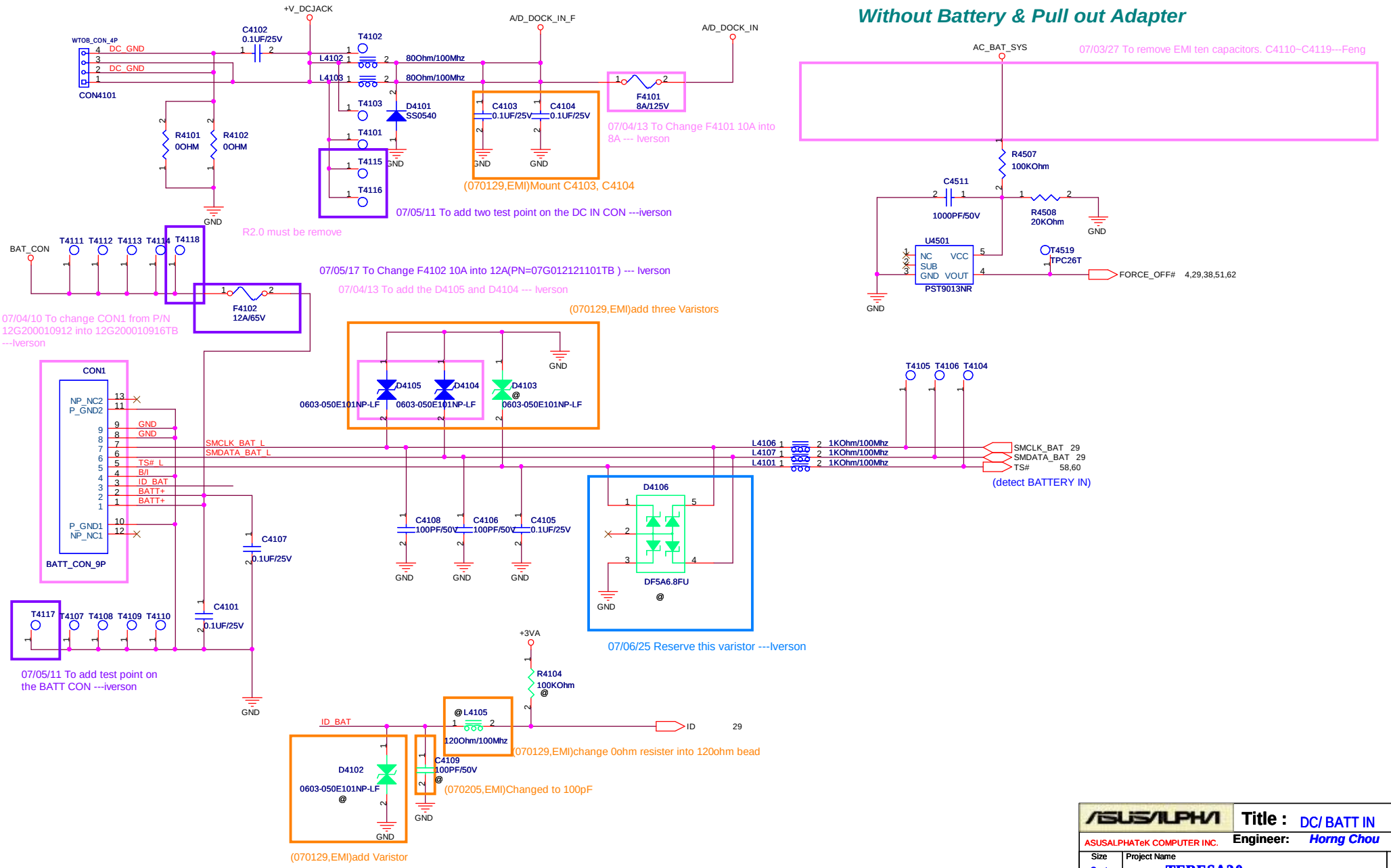
ASUSALPHATeK COMPUTER INC.

Engineer: Feng Lin

Size	Project Name	Rev
Custom	TERESA20	2.0

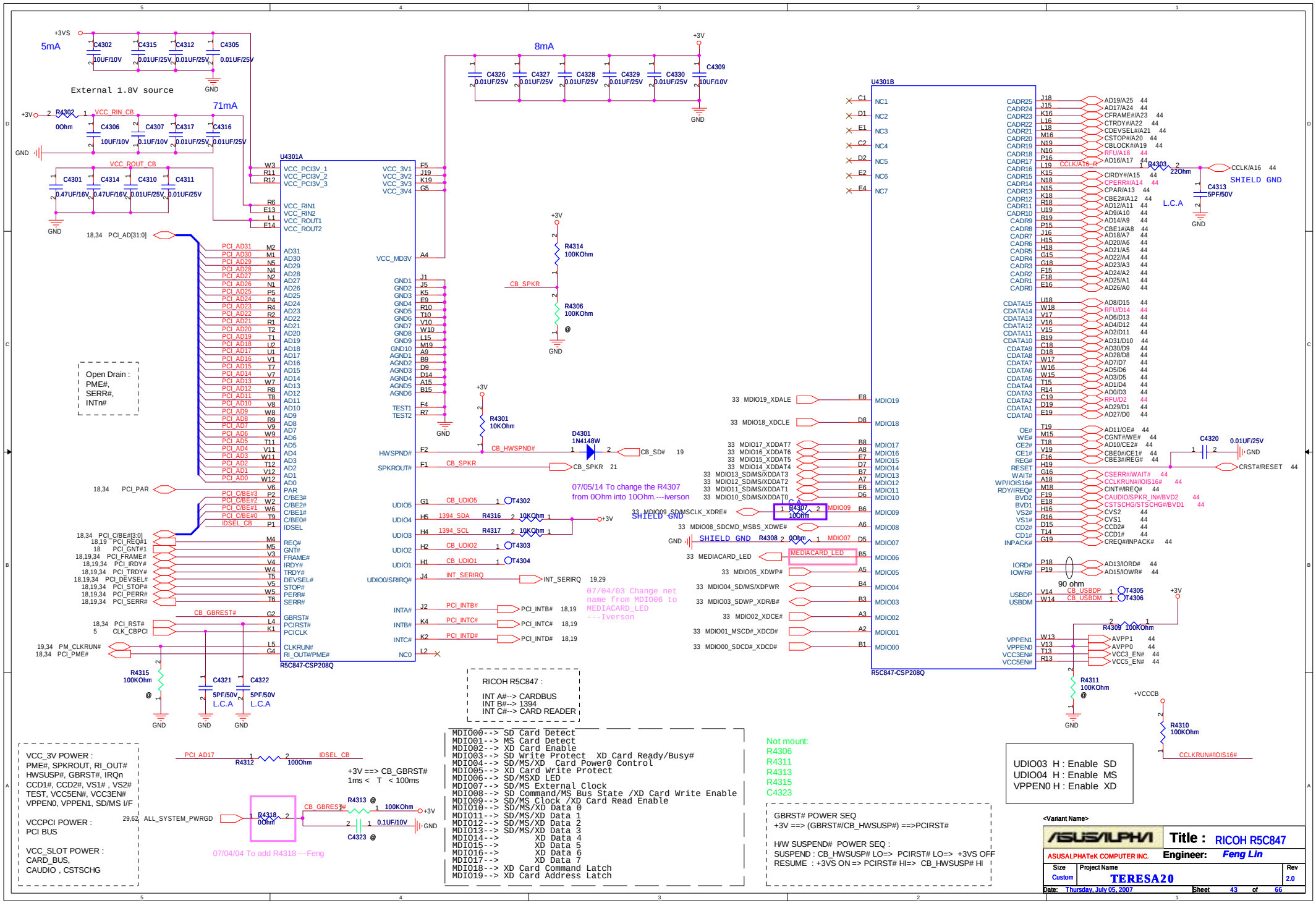
Date: Thursday, July 05, 2007 Sheet 40 of 66

DC Power Jack

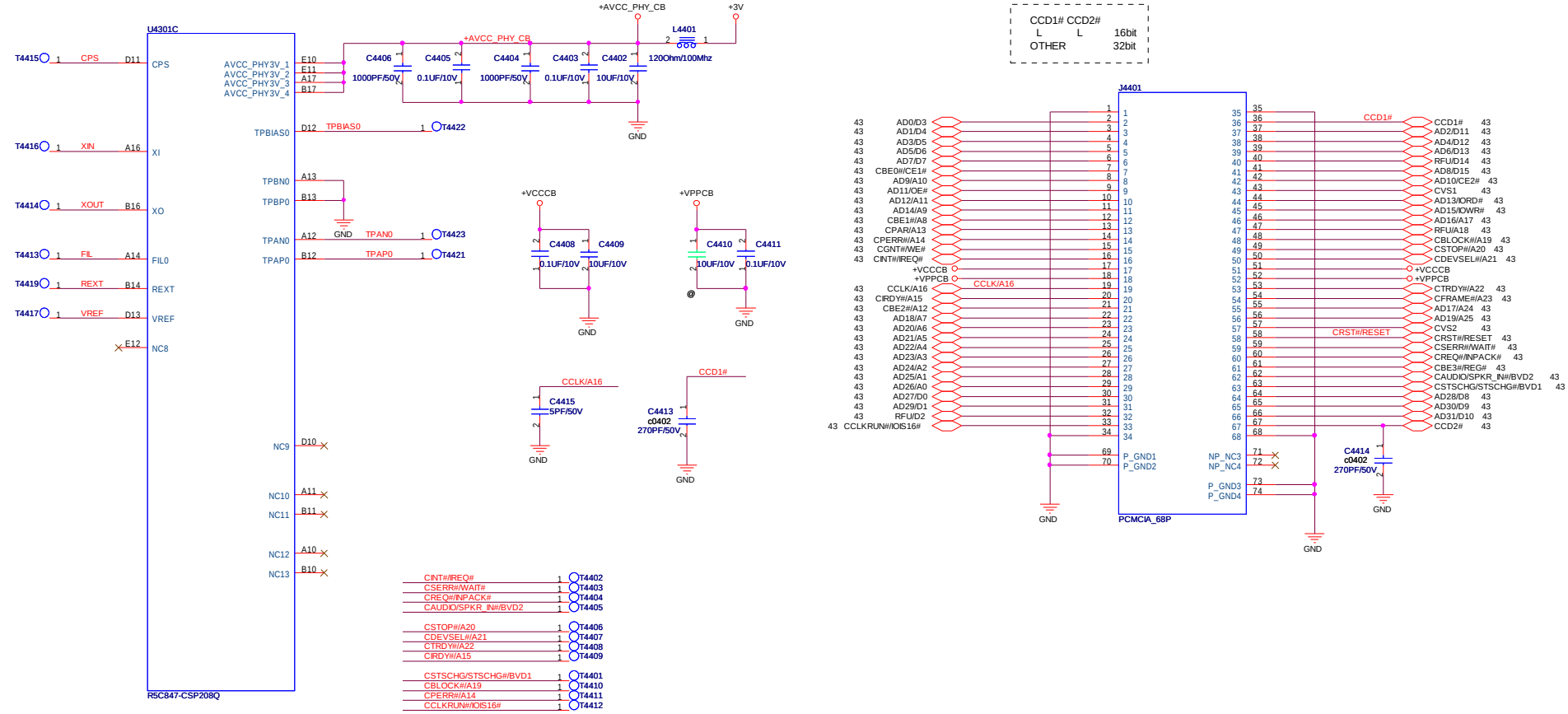


ASUSALPHA	Title : DC/ BATT IN	
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou	
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 41 of 66	

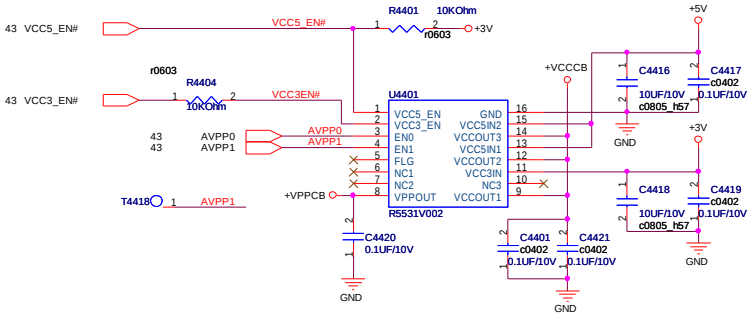
Title	<Title>		
Size A	Document Number <Doc>		Rev <RevCode>
Date: Thursday, July 05, 2007		Sheet 42 of 66	



PCMCIA SOCKET



CCD1# CCD2#
L L 16bit
OTHER 32bit



ASUSALPHA	Title : CARDBUS SOCKET		
ASUSALPHATeK COMPUTER INC.	Engineer: Horng Chou		
Size: Custom	Project Name: TERESA20		Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 44 of 66		

A:CPU BKT

PN:s01756

H4514 @ CT272CB276D138
H4515 @ CT272CB276D138
H4516 @ CT272CB276D138
H4517 @ CT272CB276D138
H4518 @ CT272CB276D138
H4519 @ CT272CB276D138
H4520 @ CT272CB276D138
GND

B:MDC NUT

MDC NUT put on page35
(H3501, H3502)

F:MINI CARD NUT

MINI CARD NUT put on
page26(H2601, H2602)

07/04/03 Add CPU BKT. H4518 ~ H4520 ---Iverson

C:TOP TO BTM

PN:S01912

H4524 @ CT276RB335X364D106N
GND

D:FIX MB

PN:s01769

H4510 @ 2DRILL_D98N_D98N
GND

E:TOP TO BTM

PN:S01911

H4512 @ RT276X461BD106N
GND

G:FIX MB

PN:s01783

H4508 @ CR295X325D98N
GND

H:SYS BOSS

PN:S01914

H4509 @ RT496X472D106N

I:MB TO IO BKT

PN:S01913

H4506 @ RT335X276D106N

J:SYS BOSS

PN:S01915

H4503 @ RT276x346BD106N
GND

K:MB TO IO BKT

PN:S01705

H4527 @ CT197B220x232D98N

L:TOP TO BTM

PN:S01916

H4504 @ RT276X354BD106N

M:SYS BOSS

PN:s01917

H4501 @ RT276x335RBD106N

N:TOP TO BTM

PN:S01851

H4507 @ RT335X276RBD98N

07/04/04 To add 2 pcs
U4508/U4509 EMI spring---Feng

O:ALIGNMENT HOLE

PN:temp_5262_gh15

H4528 @ C98D98N

07/04/03 Remove the T:NB SINK NUT --- Iverson

U:TOP TO BTM

PN:S01854

H4511 @ CT256RB256X244D98N

V:TOP TO BTM

PN:S01857

H4505 @ CT256B276X295D98N
GND

W:TOP TO BTM

PN:S01918

H4513 @ RT276x457RBD106N

EMI SPRING

PN:13G021034050

U4508 EMI_SPRING_PAD
U4509 EMI_SPRING_PAD
U4502 EMI_SPRING_PAD
U4504 EMI_SPRING_PAD
U4503 EMI_SPRING_PAD
U4505 EMI_SPRING_PAD
U4507 EMI_SPRING_PAD
U4506 EMI_SPRING_PAD
GND
GND

P:ALIGNMENT HOLE

PN:s01724

H4529 @ O138x98DO138x98N

EMI NUT

for LVDS cable
PN:13G021029050

H4533 @ A40M20-64AS
GND

ASUSALPHA

Title : SCREW HOLE

ASUSALPHATeK COMPUTER INC.

Engineer: Horng Chou

Size	Project Name	Rev
Custom	TERESA20	2.0

Date: Thursday, July 05, 2007 Sheet 45 of 66

R1.0 to R1.1

Page	Action
43	To add the varistor, but do not stuff. D4302~D4308
27	To add the ehanced ESD transistor.Q2702
30	To add the ehanced ESD transistor.Q3003.Q3005.Q3008.Q3009.Q3010
19	To change the BAT_LOW_1HZ into test point
12	To add the D1206
30	To remove the D3006, and To add the Q3011.
22	To add the C2250 and D2209, but the D2209 do not stuff
28	To Change the ODD Part andSymbol.
29	To add the EC_PWM_16S net name to control BAT_LOW_BEEP
28	To use U2801 to gate EC_BATLOW_BEEP
29	To add the R2965 0Ohm
21	To change codec from ADI1986 to ALC660.
22	To modify codec depop circuit.
23	To modify codec MIC peripheral circuit.
98	To add the ESD diode(D4302~D4308).

R1.2 to R2.0

Page	Action	Reason
22	To add Q2206 and Q2209 to solve the pop noise ,But do not stuff.	To solve pop noise of the codec
23	To add the T filter to solve pop noise of the MIC	To solve pop noise of the MIC
13	To change the CON1302 P/N from 12G10111015M into 12G10111215TTB	
29	Reserve for auto on issue	
35	To add the R3512/R3513 49.9 Ohm and C3513 close to the transformer,But do not stuff.	For RD verify
35	Modify the CON4102 PCB footprint	Slove SMT issue
25	Modify CON2501 PCB footprint	
33	Modify CON3301 PCB footprint	
15	Modify the CON1501 pcb footprint.	
05	To add the C0526 5pF on CLK_ICH14 signal.	
33	To add the C3310 1UF and the U3301 and R3312 10KOhm	
34	To change the C3402/C3403 from 0.01uF into 0.1uF	
35	To change the C3512/C3513 from 0.01uF into 0.1uF	
36	To add the C3616 22 uF and C3615 10uF.	
33	To Remove the R3306 Q3306 Q3307.	
19	R1950,R1951,R1953 change from 1% to 5%.	
05	R0505 change to RES 1K OHM 1/16W (0402) 1%.	
05	To change the R0514 from 390 Ohm into 300 Ohm.	
36	To change the CE3605 from 100 uF into 150 uF	
13	To add the L1307 L1308 L1309. Remove the Pi-type filter.	

R1.1 to R1.2

Page	Action
25	To connect the SCL_3A and SDA_3A signals.
36	To change the USB CON P/N from 12G13111108F into 12G13111108STB
3	To add test point on VID[0:6] signals.
15	To add the R1504、R1506、R1503 to configure memory
34	To add test point on LAN EEPROM signals.
21	To add the R2133 10KOhm,But do not stuff
22	To add the R2207/R2208 0Ohm Pull-down
13	To add the R1315 0Ohm
13	To change the R1309/R1310/R1311/R1312 from 2.2KOhm into 2KOhm
38	To add test point on power switch
24	To add test point on the ISA ROM
22	To modify HP_DET circuit
23	To modify MIC_DET circuit
41	To add two test point on the DC IN CON
41	To add test point on the BATT CON
22	To add the R2244 0Ohm, but do not stuff.
43	To change the R4307 from 0Ohm into 10 Ohm.
29	To change the R2901/R2904 from 4.7K Ohm into 3.3K Ohm
35	To add the R3510/R3511 49.9 Ohm and C3512 close to transformer.
36	To change the R3603/R3604 from 10K Ohm into 0 Ohm.
36	To add the R3605/R3606/R3607 0 Ohm
13	To remove the Q1302 and Q1304
20	To add the C2050 1uF on the +5VREF_ICH signal
22	To change the R2201/R2202 from 13K Ohm into 11K Ohm
22	To change the R2206/R2214 from 10K Ohm into 12K Ohm
29	To add two GPIO net (GPM4/GPM5) to control the USB POWER SW
28	To move the C2803 and C2804 from the +3Vs into the +5Vs
41	To Change F4102 10A into 12A(PN=07G012121101TB)
34	To change the C3407/C3406 from 30pF into 27pF
5	To change the C0510/C0511 from 33pF into 27pF.
17	To change the C1707/C1708 from 18pF into 10pF
4	Don't stuff R0415, but stuff R0416
16	To change U1601 PCB footprint from sot23_s5_rd1 to nb_sot23_s5_t

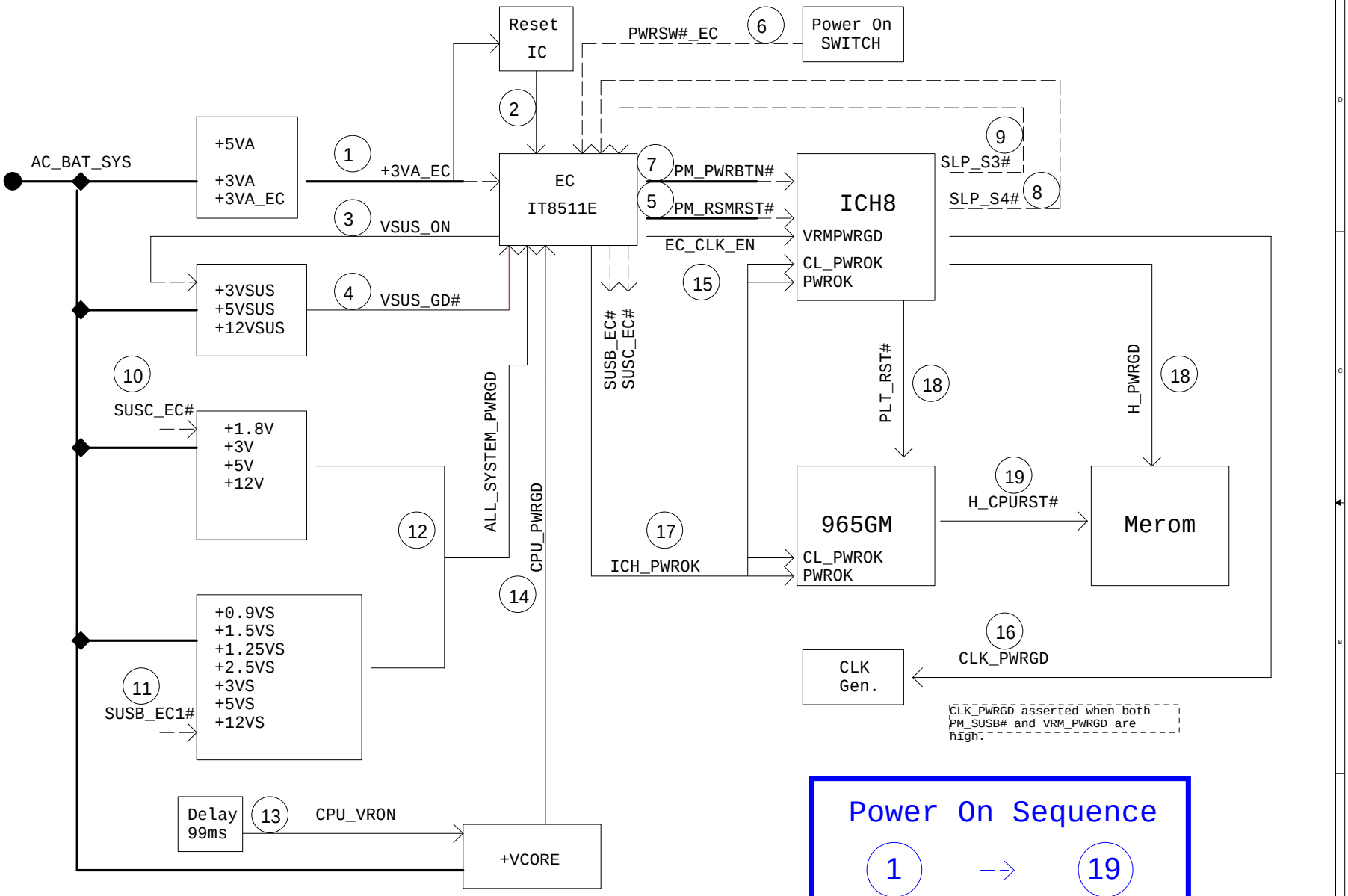
<Variant Name>

ASUSALPHA | Title : HISTORY

ASUSALPHATeK COMPUTER INC. | Engineer: Feng Lin

Size	Project Name	Rev
Custom	TERESA20	2.0

Date: Friday, July 06, 2007 | Sheet 46 of 66



<Variant Name>

ASUSALPHA

Title : PowerOn sequence

ASUSALPHATeK COMPUTER INC.

Engineer: Julian Kuo

Size	Project Name	Rev
Custom	TERESA20	2.0

Date: Thursday, July 05, 2007 Sheet 47 of 66

EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Pin	Pin Name	Signal Name	Type
32	PWM0/GPA0	BRIGHT_PWM	O	48	GPH0	VSUS_ON_EC	O
33	PWM1/GPA1	FAN_PWM	O	54	GPH1	SUS_PWRGD	I
36	PWM2/GPA2	/	O	55	GPH2	CPU_PWRGD	I
37	PWM3/GPA3	BAT_LOW_BEEP	O	69	GPH3	PM_PWRBTN#	O
38	PWM4/GPA4	CHG_LED_UP#	O	70	GPH4	SUSC_EC#	O
39	PWM5/GPA5	PWR_LED_UP#	O	75	GPH5	SUSB_EC0#	O
40	PWM6/GPA6	BATSEL_3S#	O	76	GPH6	CPU_VRON	O
43	PWM7/GPA7	LCD_BACKOFF#	O	105	GPH7	PM_RSMRST#	O
153	RXD/GPB0	NUM_LED	O	148	GPI0	ICH_PWROK_EC	O
154	TXD/GPB1	CAP_LED	O	149	GPI1	ALL_SYSTEM_PWRGD	O
162	GPB2	SCRL_LED	O	152	GPI2	/	
163	SMCLK0/GPB3	SMCLK_BAT	I/O	155	GPI3	CHG_EN#	O
164	SMDAT0GPB4	SMDATA_BAT	I/O	156	GPI4	PRECHG	O
5	GA20/GPB5	A20GATE	O	168	GPI5	EC_CLK_EN	O
6	KBRST#/GPB6	RCIN#	O	174	GPI6	BAT_LEARN	O
165	GPB7	THRO_CPU	O	109	GPI7	SUSB_EC2#	
47	CLKOUT/GPC0	/	O	99	DAC0/GPJ0	CHG_FULL_LED#_EC	O
169	SMCLK1/GPC1	SMB1_CLK	I/O	100	DAC1/GPJ1	/	
170	SMDAT1/GPC2	SMB1_DAT	I/O	101	DAC2/GPJ2	INVTER_DA	O
171	GPC3	/	I	102	DAC3/GPJ3	BATSEL_2P#	O
172	TMRI0/WUI2/GPC4	ACIN_OC#	I	97	GPJ4	EC_PWM_16S	
175	GPC5	OP_SD#	O	98	GPJ5	/	
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I				
1	CK32KOUT/GPC7	/	O				
26	RI1#/WUI0/GPD0	PM_SUSB#	I	81	ADC0/GPK0	/	I
29	RI2#/WUI1/GPD1	PM_SUSC#	I	82	ADC1/GPK1	/	
30	LPCRST#/WUI4//GPD2	PLT_RST#	I	83	ADC2/GPK2	/	I
31	ECSCI#/GPD3	ECSC#	O	84	ADC3/GPK3	/	
41	GPD4	/		93	ADC8/GPK4	KB_ID0	I
42	GINT/GPD5	/		94	ADC9/GPK5	KB_ID1	I
62	TACH0/GPD6	FAN0_TACH	I				
63	TACH1/GPD7	/	O				
87	ADC4/GPE0	WLAN_SW#_EC(Reserved)	I	8	GPL0	WLAN_ON#	O
88	ADC5/GPE1	/	I	11	GPL1	/	O
89	ADC6/GPE2	/	I	12	GPL2	/	I
90	ADC7/GPE3	/	I	20	GPL3	/	O
2	PWRSW/GPE4	PWRSW#_EC	I	21	GPL4	/	
44	WUI5/GPE5	/		106	GPL5	/	
24	LPCPD#/WUI6/GPE6	/	I	107	GPL6	/	
25	CLKRUN#/WUI7/GPE7	/	O	108	GPL7	SUSB_EC#	
110	PS2CLK0/GPF0	/		22	ECSMI#/GPM0	EXTSMI#	O
111	PS2DAT0/GPF1	/		23	PWUREQ#/GPM1	/	
114	PS2CLK1/GPF2	/	I/O	85	KSO16/GPM2	/	
115	PS2DAT1/GPF3	/	I/O	86	KSO17/GPM3	ID_EC (Reserved)	I
116	PS2CLK2/GPF4	TPAD_CLK		91	CTX/GPM4	GPM4	
117	PS2DAT2/GPF5	TPAD_DAT		92	CRX/GPM5	GPM5	
118	PS2CLK3/GPF6	/					
119	PS2DAT3/GPF7	/	I				
113	FA16/GPG0	FA16					
112	FA17/GPG1	FA17					
104	FA18/GPG2	FA18					
103	FA19/GPG3	FA19					
3	FA20/GPG4	LID_EC#	I				
4	FA21/GPG5	/					
27	LPC80HL/GPG6	PM_THERM#_EC(Reserved)	O				
28	LPC80LL/GPG7	AC_APR_UC#	I				

ICH8-M GPIO SETTING

Pin	Pin Name	Signal Name	Type
AG12	GPIO00/BM_BUSY#	PM_BMBUSY#	I
AJ8	GPIO01/TACH1	/	I
F8	GPIO02/PIRQE#	PCI_INTE#	I
G11	GPIO03/PIRQF#	PCI_INTF#	I
F12	GPIO04/PIRQG#	PCI_INTG#	I
B3	GPIO05/PIRQH#	PCI_INTH#	I
AC21	GPIO06	/	I/O
AH9	GPIO07	/	I
AE16	GPIO08	EXTSMI#	I
AG19	GPIO09	/	I
AJ24	GPIO10	WLAN_SW#_ICH	I
AG22	SMBALERT#/GPIO11	/	I
AC19	GPIO12	KBC_SCI#	I
AH21	GPIO13	/	I
AF22	GPIO14	/	I
AE20	GPIO15	STP_PCI#	O
AJ14	GPIO16	PM_DPRSLPVR	O
AG8	GPIO17	NEWCARD_OFF#	O
AH12	GPIO18	BTO_DEV0	O
AJ10	GPIO19/SATA1GP	NEWCARD_DET#	I
AE11	GPIO20	BTO_DEV1	O
AJ12	GPIO21/SATA0GP	/	I
AG10	REQ4#/GPIO22	WLAN_LED#	I
E6	LDRQ1#/GPIO23	/	
AJ27	GPIO24	/	
AG18	GPIO25	STP_CPU#	O
AH27	GPIO26	/	
AH25	GPIO27	BAT_LOW_1HZ	I
AD16	GPIO28	CB_SD#	O
AG17	GPIO29/OC#5	USB_OC_5#	I
AD12	GPIO30/OC#6	NEWCARD_OC#	I
AJ18	GPIO31/OC#7	USB_OC_7#	I
AH11	GPIO32/CLKRUN#	PM_CLKRUN#	I/O
AE10	GPIO33/AZ_DOCK_EN#	/	I
AG14	GPIO34/AZ_DOCK_RST#	/	I
AG13	GPIO35	BTO_DEV2	O
AF11	GPIO36/SATA2GP	/	
AG11	GPIO37/SATA3GP	PCB_ID0	I
AF9	GPIO38	PCB_ID1	I
AJ11	GPIO39	PCB_ID2	I
AD10	GNT4#/GPIO48	/	O
AG29	GPIO49/CPUPWRGD	H_PWRGD	O

Indigo: the same as T12EG
Pink: different from T12EG

PCI Device	IDSEL#	REQ/GNT#	Interrupts
10/100 RTL8100CL	AD23	2	A
CARDBUS	AD17	1	B
1394	AD17	1	C
CARD READER	AD17	1	D

PCIE Device	Bus		
MINI_CARD	PE(T/R)(p/n)2		
NEWCARD	PE(T/R)(p/n)3		

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2)
SO-DIMM 0	1010000x (A0)
SO-DIMM 1	1010001x (A2)
Thermal Sensor	1001100x (98)

<Variant Name>

ASUSALPHA

Title : GPIO Setting

ASUSALPHATeK COMPUTER INC. Engineer: Iverson Qiu

Size: Custom | Project Name: TERESA20 | Rev: 2.0

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Title	<Title>		
Size A	Document Number <Doc>		Rev <RevCode>
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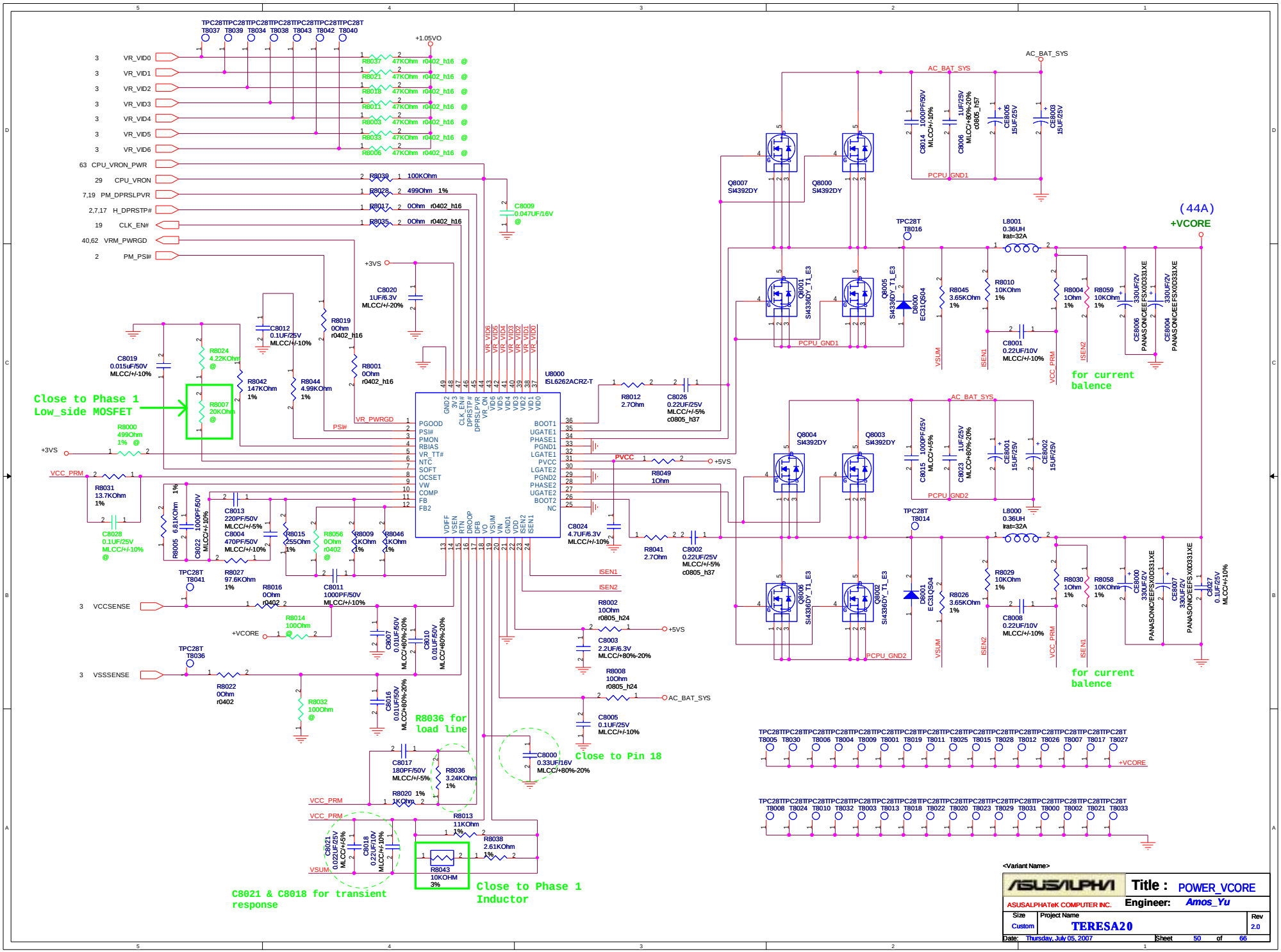
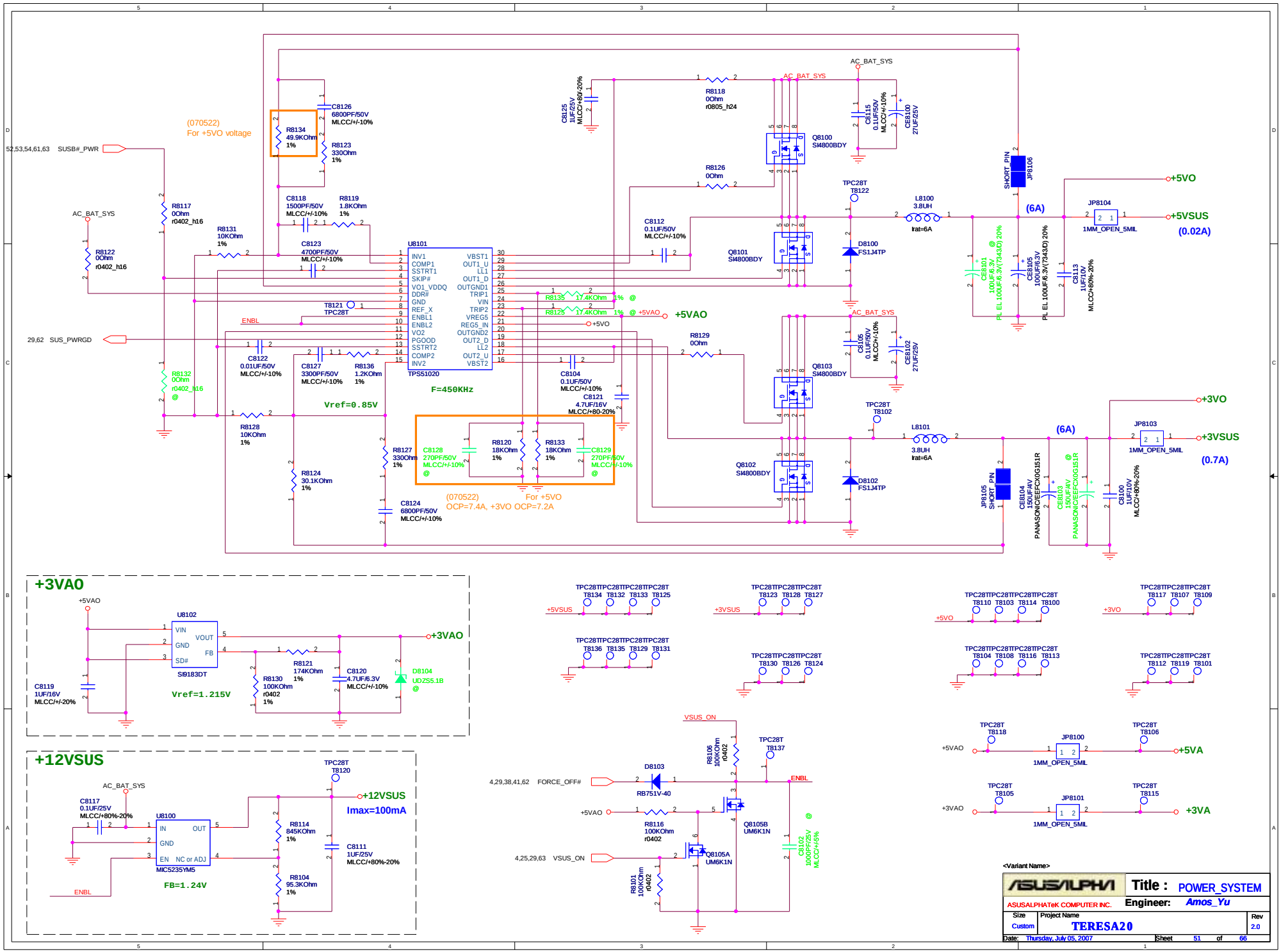
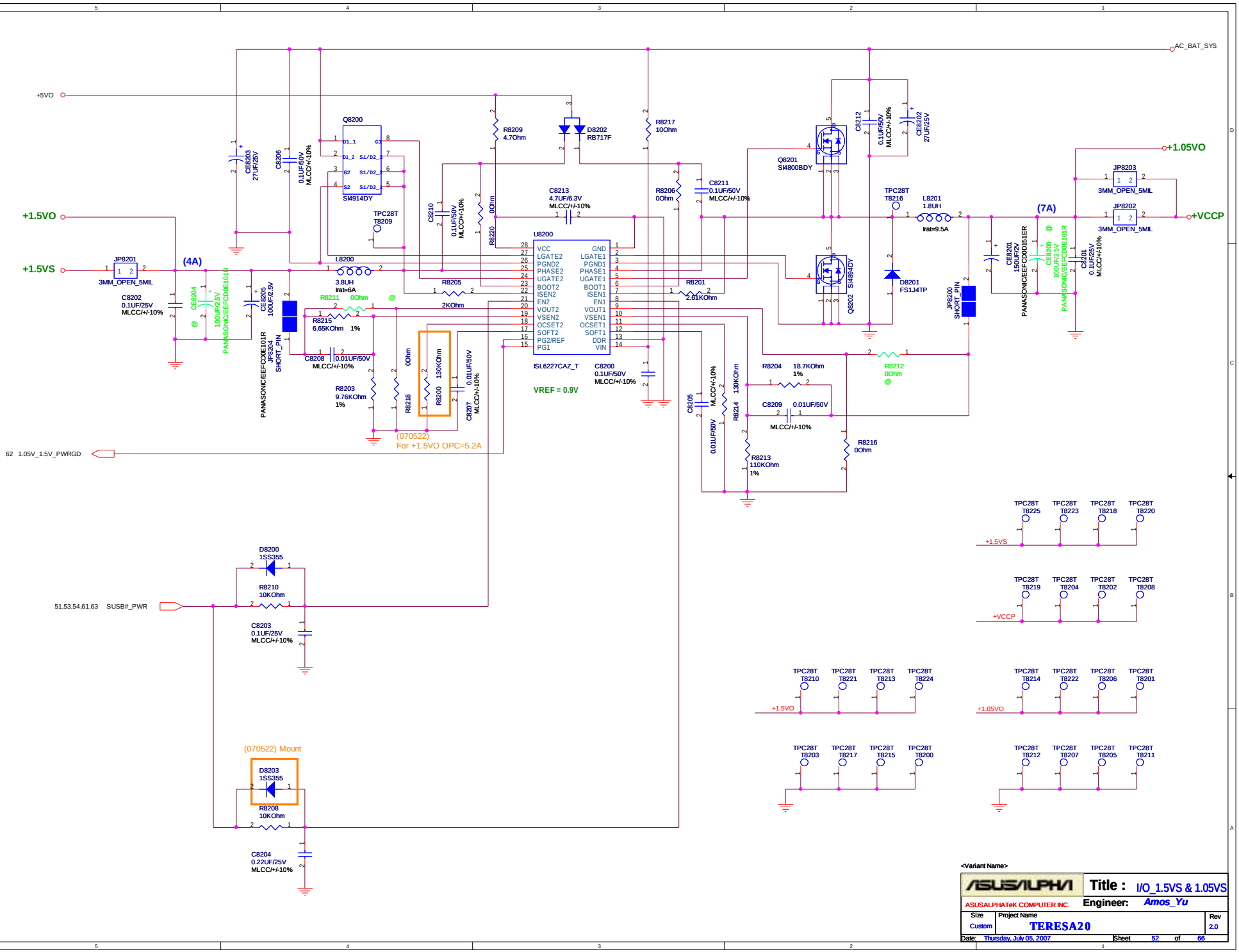
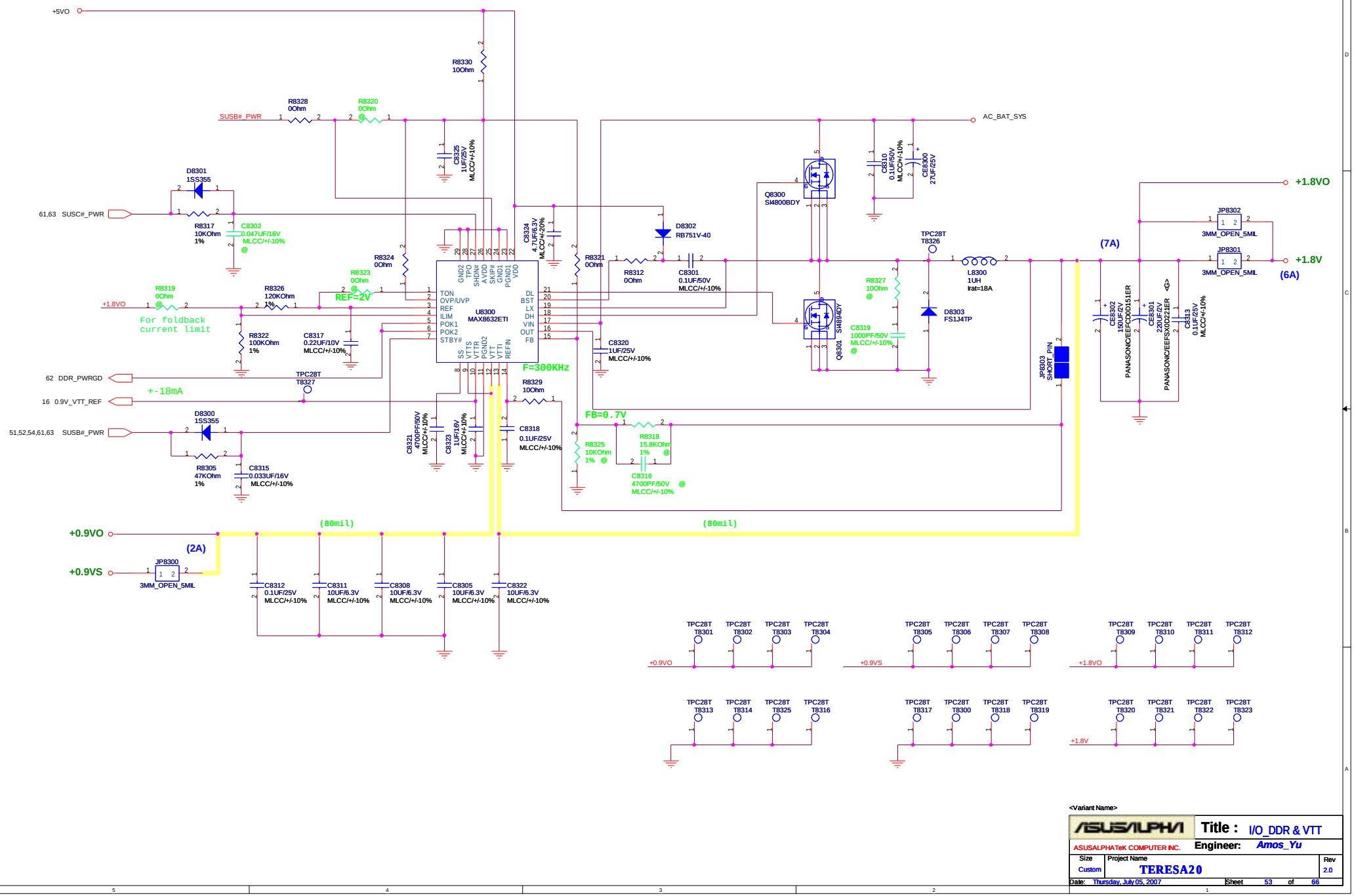
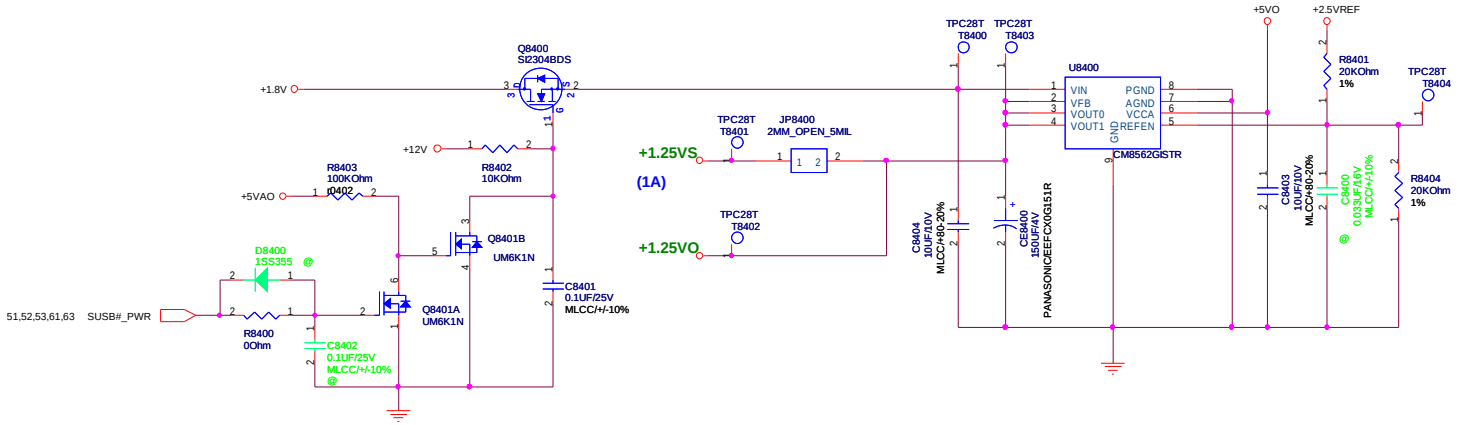




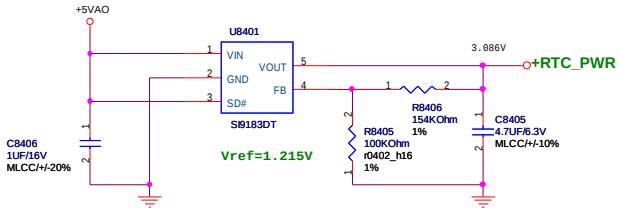




+1.25VS



+RTC_PWR



<Variant Name>

ASUSALPHA	Title :	POWER_I/O_1.25VS & RTC_PWR
ASUSALPHATeK COMPUTER INC.	Engineer:	Amos_Yu
Size: Custom	Project Name: TERESA20	Rev: 2.0
Date: Thursday, July 05, 2007	Sheet 54 of 66	

<Variant Name>

/ASUSALPHA	Title : POWER_Empty
ASUSALPHATeK COMPUTER INC.	Engineer: Amos_Yu
Size: C	Project Name: TERESA20
Rev: 2.0	
Date: Thursday, July 05, 2007	Sheet 55 of 66

<Variant Name>

ASUSALPHATeK COMPUTER INC.

Title : POWER_Empty

Engineer: Amos_Yu

Size	Project Name	Rev
B	TERESA20	2.0

Date: Thursday, July 05, 2007 Sheet 56 of 66

R1.1 to R1.2

Page	Action
81	To modify +5VO output voltage, modify R8134 to 49.9K Ohm,
81	To modify +5VO and +3VO OCP, un-mount C8128, C8129 and modify R8120, R8133 to 18K Ohm
82	To modify +1.5VO OCP, modify R8200 to 130K Ohm
82	To modify +1.05VO Disable timing, mount D8203
88	Modify component, CE8800, CE8801
91	To modify +3VS timing, modify R9108 to 20K Ohm

<Variant Name>

ASUSALPHA

Title : POWER_HISTORY

ASUSALPHATeK COMPUTER INC.

Engineer: Amos_Yu

Size	Project Name	Rev
B	TERESA20	2.0

Date: Thursday, July 05, 2007 Sheet 56 of 66

<Variant Name>

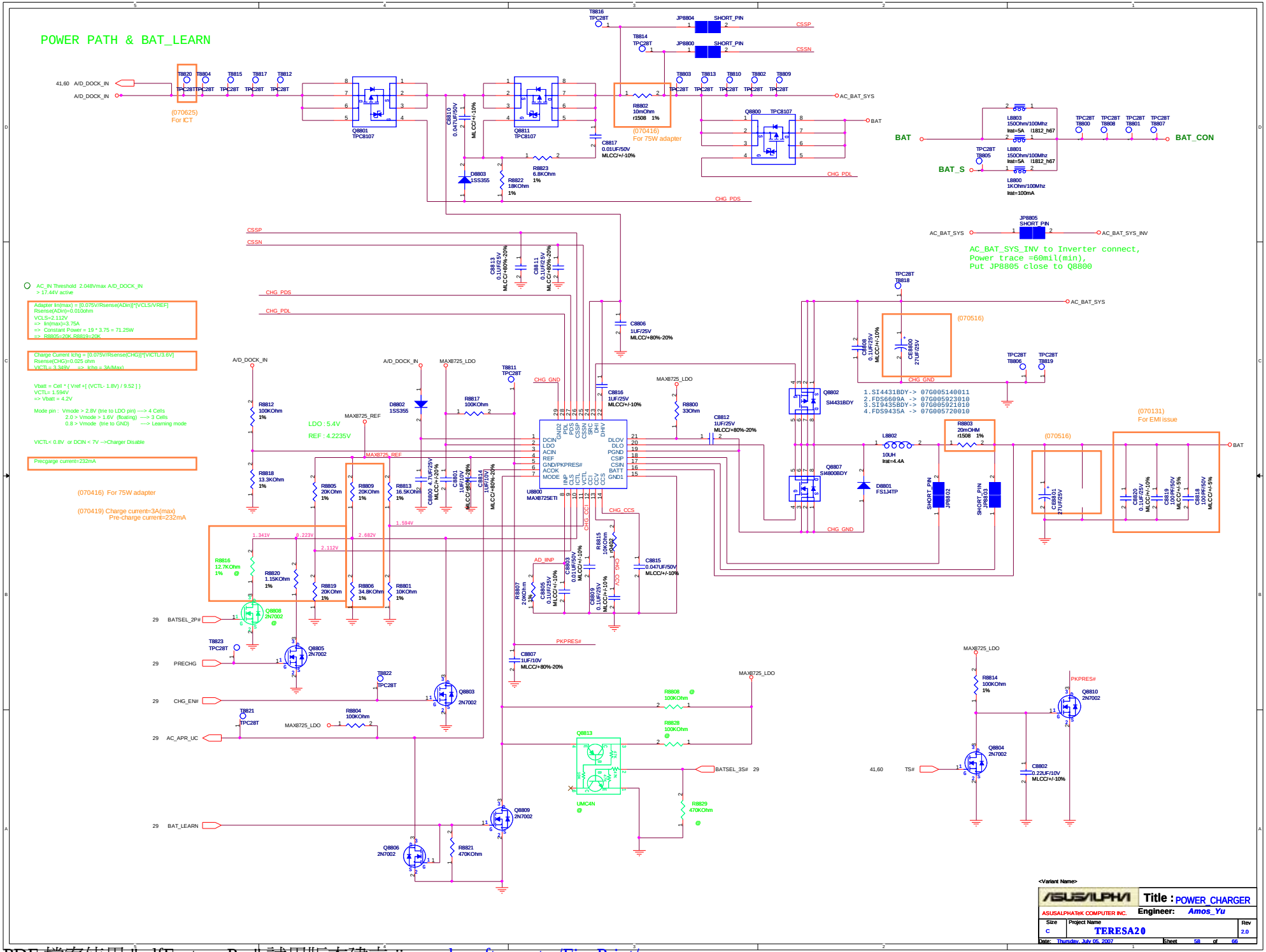
ASUSALPHATeK COMPUTER INC.

Title : POWER_Empty

Engineer: Amos_Yu

Size	Project Name	Rev
Custom	TERESA20	2.0

Date: Thursday, July 05, 2007 Sheet 57 of 66



<Variant Name>

ASUSALPHATeK COMPUTER INC.

Title : POWER_Empty

Engineer: Amos_Yu

Size	Project Name	Rev
Custom	TERESA20	2.0

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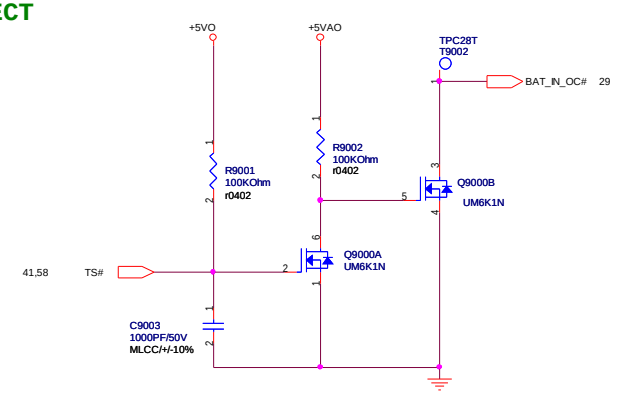
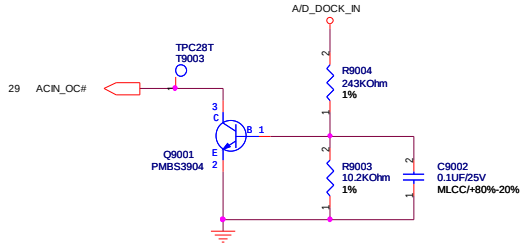
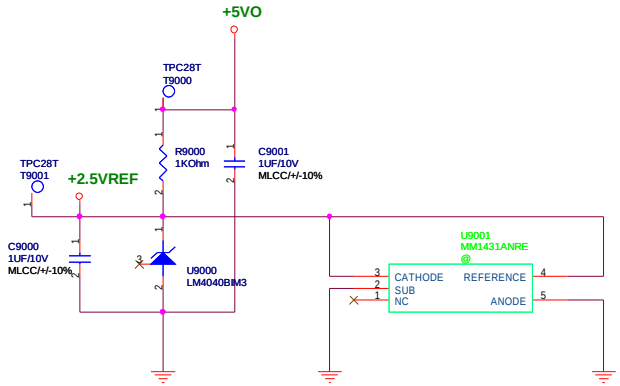
BATTERY IN DETECT



ADAPTER IN DETECT



+2.5VREF

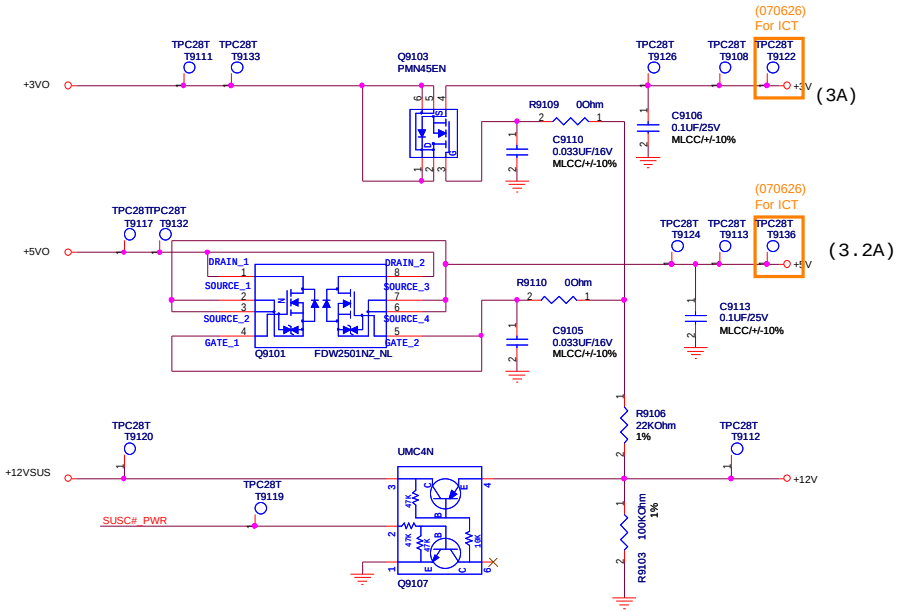


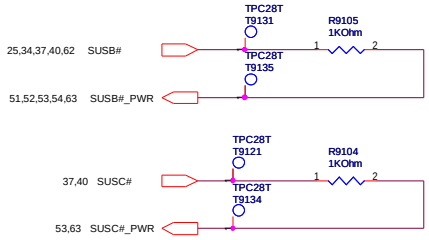
U9000 & U9001 colay

<Variant Name>

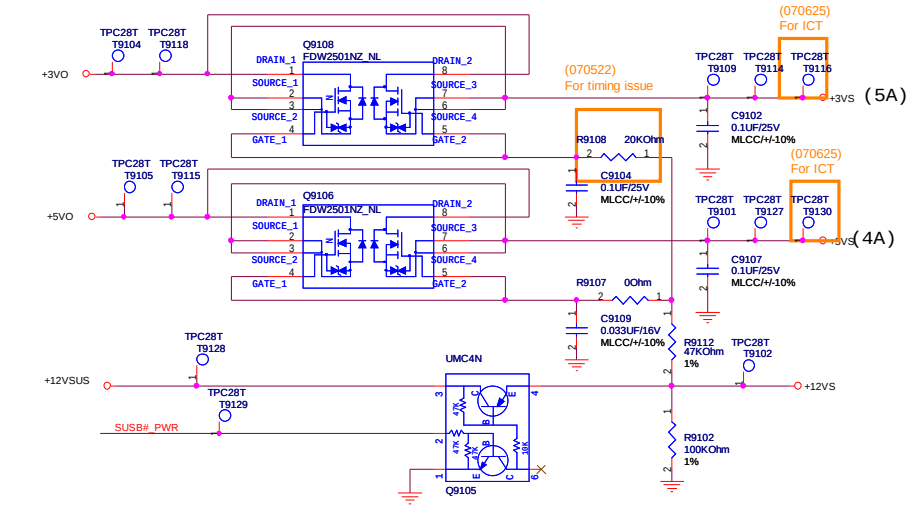
ASUSALPHA	Title : POWER_DETECT
ASUSALPHATeK COMPUTER INC.	Engineer: Amos_Yu
Size: Custom	Project Name: TERESA20
Rev: 2.0	
Date: Thursday, July 05, 2007	Sheet 60 of 66

SUSC#_PWR POWER





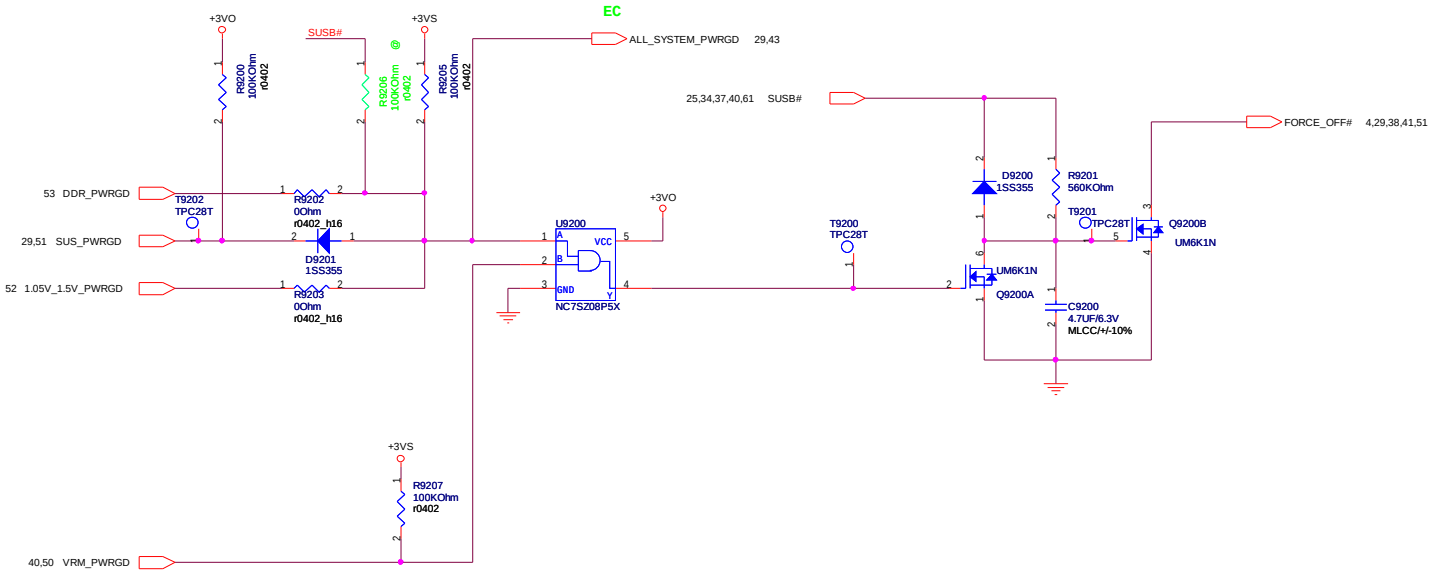
SUSB#_PWR POWER



<Variant Name>

ASUSALPHA	Title : LOAD SWITCH
ASUSALPHATeK COMPUTER INC.	Engineer: Amos_Yu
Size: Custom	Project Name: TERESA20
Rev: 2.0	
Date: Thursday, July 05, 2007	Sheet 61 of 66

POWER GOOD DETECTER



<Variant Name>

ASUSALPHA

Title : POWER_PROTECT

ASUSALPHATeK COMPUTER INC. Engineer: Amos_Yu

Size	Project Name	Rev
Custom	TERESA20	2.0

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AC_BAT_SYS → AC_BAT_SYS 41,50,51,52,53,58

BAT → BAT 58

BAT_CON → BAT_CON 41,58

+2.5VREF → +2.5VREF 54,60

+3VA → +3VA 4,12,19,29,37,38,41,51

+5VAO → +5VAO 51,54,60

+5VO → +5VO 51,52,53,54,60,61

+5VSUS → +5VSUS 20,30,36,51

+5V → +5V 10,16,30,36,37,44,61

+5VS → +5VS 4,13,19,20,21,22,28,29,30,34,37,38,50,61

+3VO → +3VO 51,61,62

+3VSUS → +3VSUS 18,19,20,22,25,29,34,40,51

+3V → +3V 12,18,19,26,35,37,43,44,61

+3VS → +3VS 2,4,5,7,10,11,12,13,14,15,19,20,21,22,25,26,27,28,29,30,33,37,43,50,61,62

+12VSUS → +12VSUS 51,61

+12V → +12V 22,37,54,61

+12VS → +12VS 12,13,33,37,61

+1.8VO → +1.8VO 53

+1.8V → +1.8V 7,9,10,14,15,16,37,53,54

+0.9VS → +0.9VS 16,37,53

+0.9VO → +0.9VO 53

+1.05VO → +1.05VO 50,52

+VCCP → +VCCP 3,5,6,7,9,10,17,20,52

+1.5VO → +1.5VO 52

+1.5VS → +1.5VS 3,10,17,18,20,25,26,37,52

+VCORE → +VCORE 3,50

+1.25VS → +1.25VS 7,10,20,54

FOR POWER TEST

+3VA

JP9300 (SGL_JUMP) → CPU_VRON_PWR 50

JP9301 (SGL_JUMP) → SUSB#_PWR → SUSB#_PWR 51,52,53,54,61

JP9302 (SGL_JUMP) → SUSC#_PWR → SUSC#_PWR 53,61

JP9303 (SGL_JUMP) → VSUS_ON → VSUS_ON 4,25,29,51

<Variant Name>

ASUSALPHA

Title : POWER_SIGNAL

ASUSALPHATeK COMPUTER INC. Engineer: Amos_Yu

Size	Project Name	Rev
Custom	TERESA20	2.0

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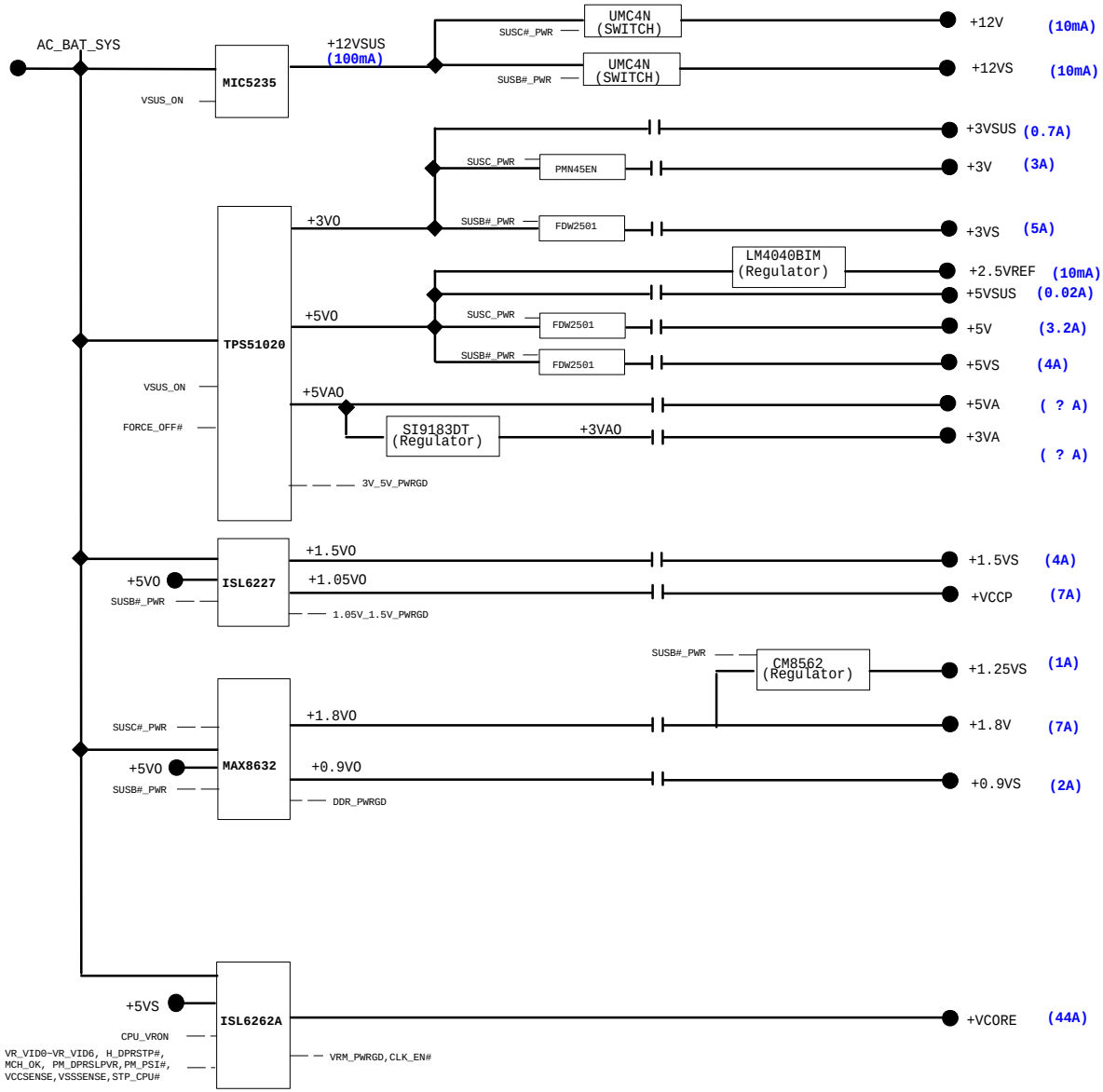

<Variant Name>

ASUSALPHATeK COMPUTER INC.

Title : POWER_FLOW

Engineer: Amos_Yu

Size	Project Name	Rev
Custom	TERESA20	2.0

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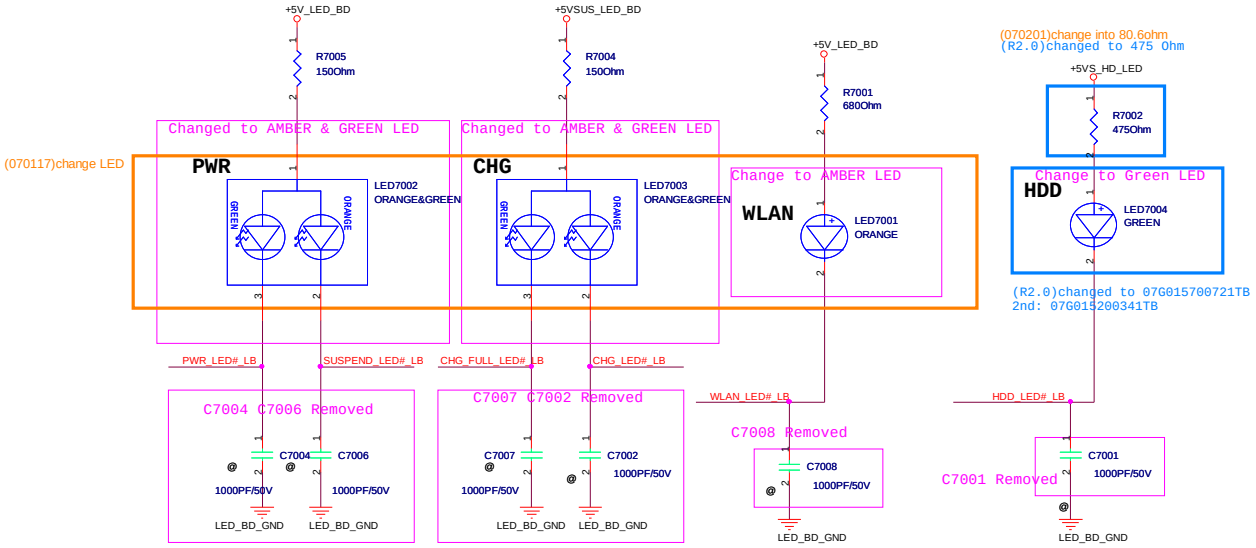
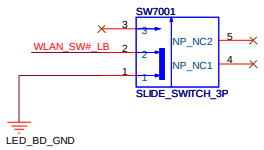
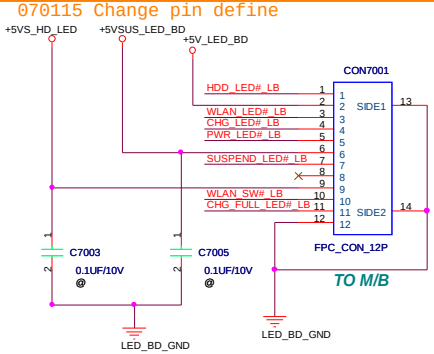
LEFT & RIGHT Button remove to TP BOARD



New added SW for Teresa

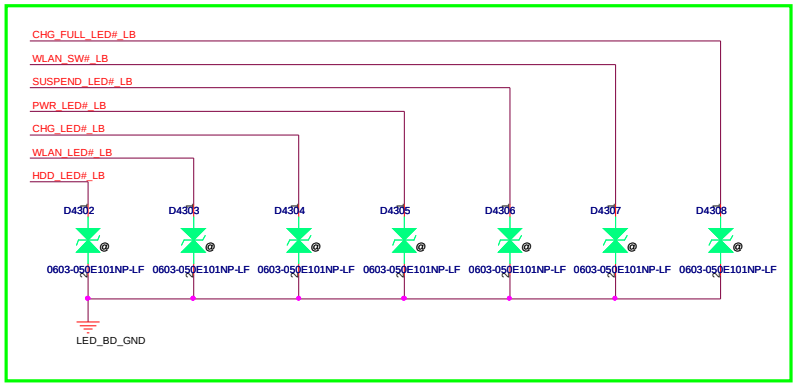


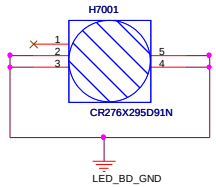
070115 Change pin define



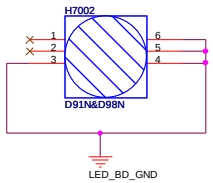
CON to T/P remove to TP BOARD

IR receive module removed





DETAIL: Q



DETAIL: S

ASUSALPHA	Title : LED Board	
ASUSALPHATeK COMPUTER INC.	Engineer: Potter_Huang	
Size: Custom	Project Name: TERESA20	Rev: 2.0
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TERESA20 SCHEMATIC V2.0

NC

ASUSALPHA

Title : Content & History

ASUSALPHATeK COMPUTER INC. Engineer: IVERSON QIU

Size	Project Name	Rev
Custom	TERESA20	2.0

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