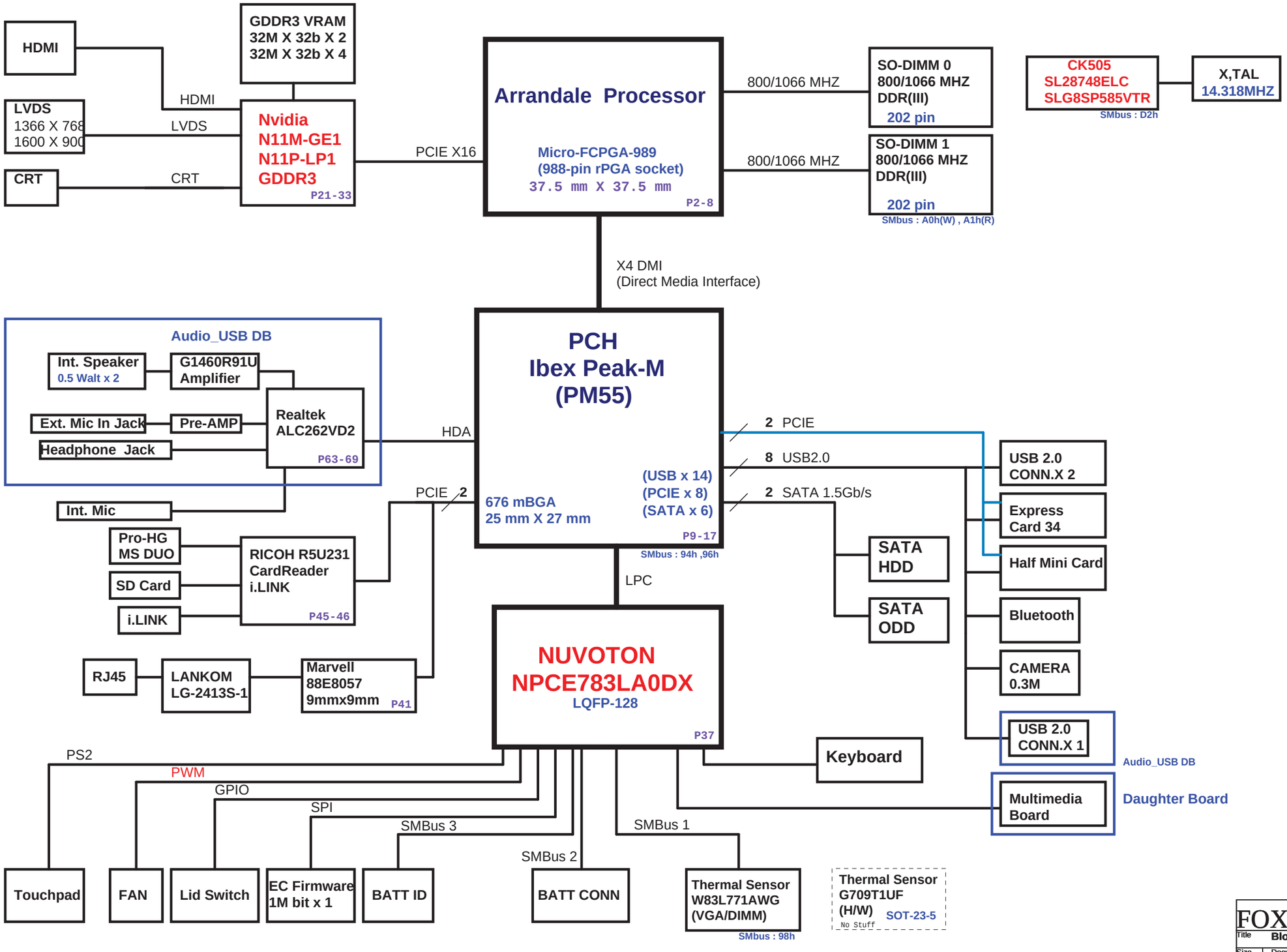
M-9A0 (Calpella + N11P/M Discrete Graphic)



TI CHARGER BQ24753 P.54

	OUTPUTS
DC_IN	BT+ DCBATOUT

SYSTEM DC/DC MAX17020ETJ+ P.55

INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC +12V

SYSTEM DC/DC SC412 P.56

INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VRUN

SYSTEM DC/DC SC412+G2998 P.57

INPUTS	OUTPUTS
DCBATOUT	+1_8VSUS
+1_8VSUS	+0_9VRUN

CPU DC/DC ISL6266A P.58

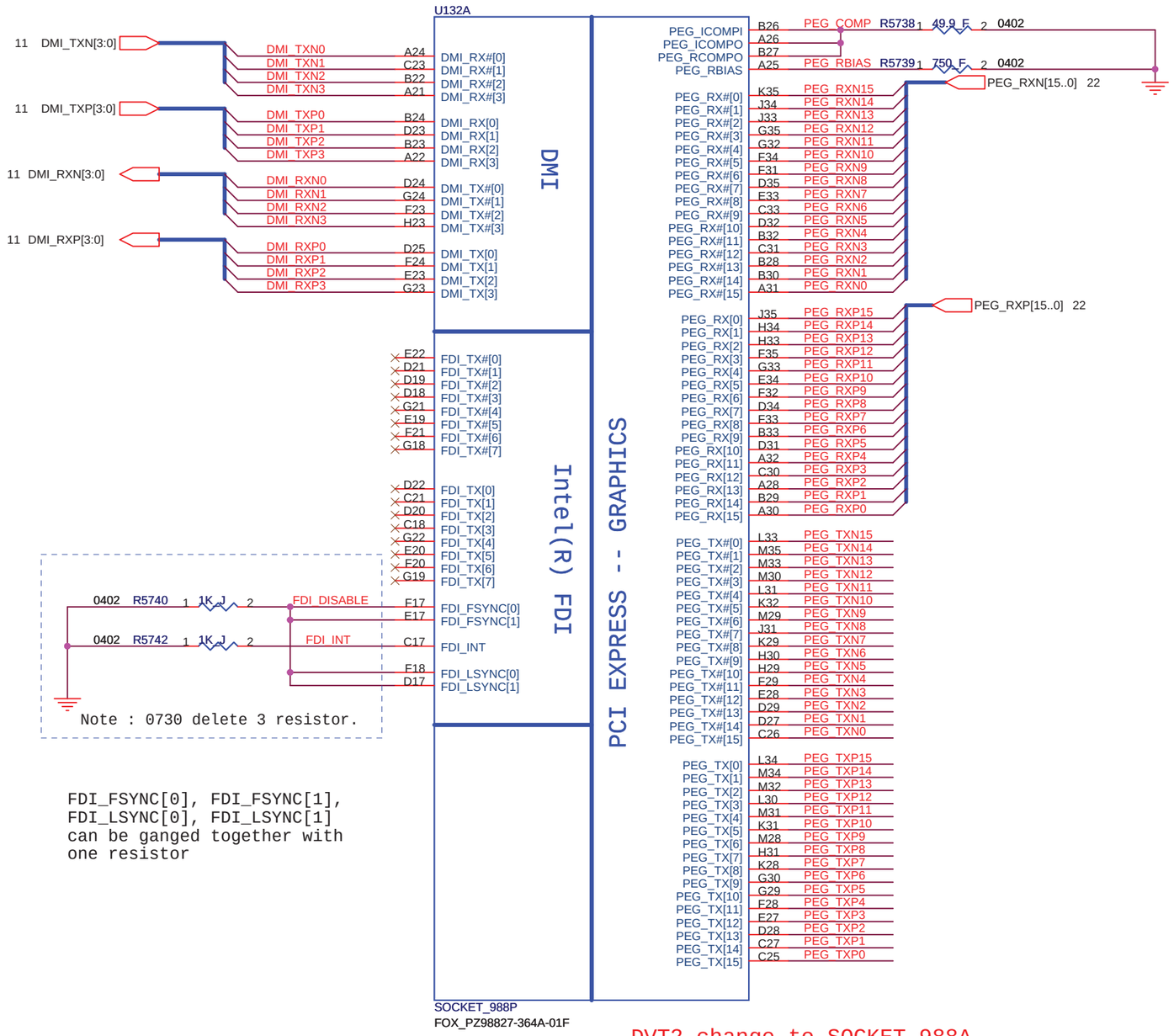
INPUTS	OUTPUTS
DCBATOUT	VHCORE

SYSTEM DC/DC SC411+APL5913 P.61

INPUTS	OUTPUTS
DCBATOUT	NV_VDD
+1_5VRUN	PEX_VDD

FOXCONN — HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

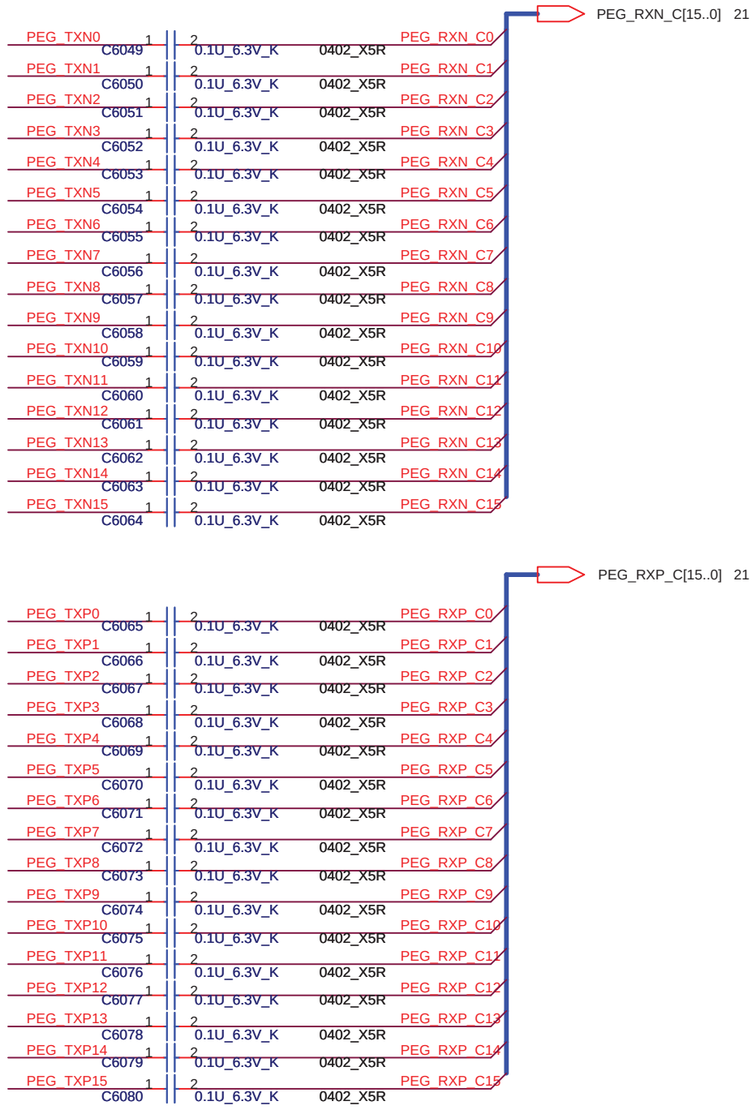
Title	Block Diagram	
Size: Custom	Document Number: M9A0_MP	Rev: 1.1
Date: Friday, October 23, 2009	Sheet 1 of 73	



FDI_FSYNC[0], FDI_FSYNC[1],
FDI_LSYNC[0], FDI_LSYNC[1]
can be ganged together with
one resistor

DVT2 change to SOCKET_988A

For Disable Arrandale Graphic
In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH.
FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).



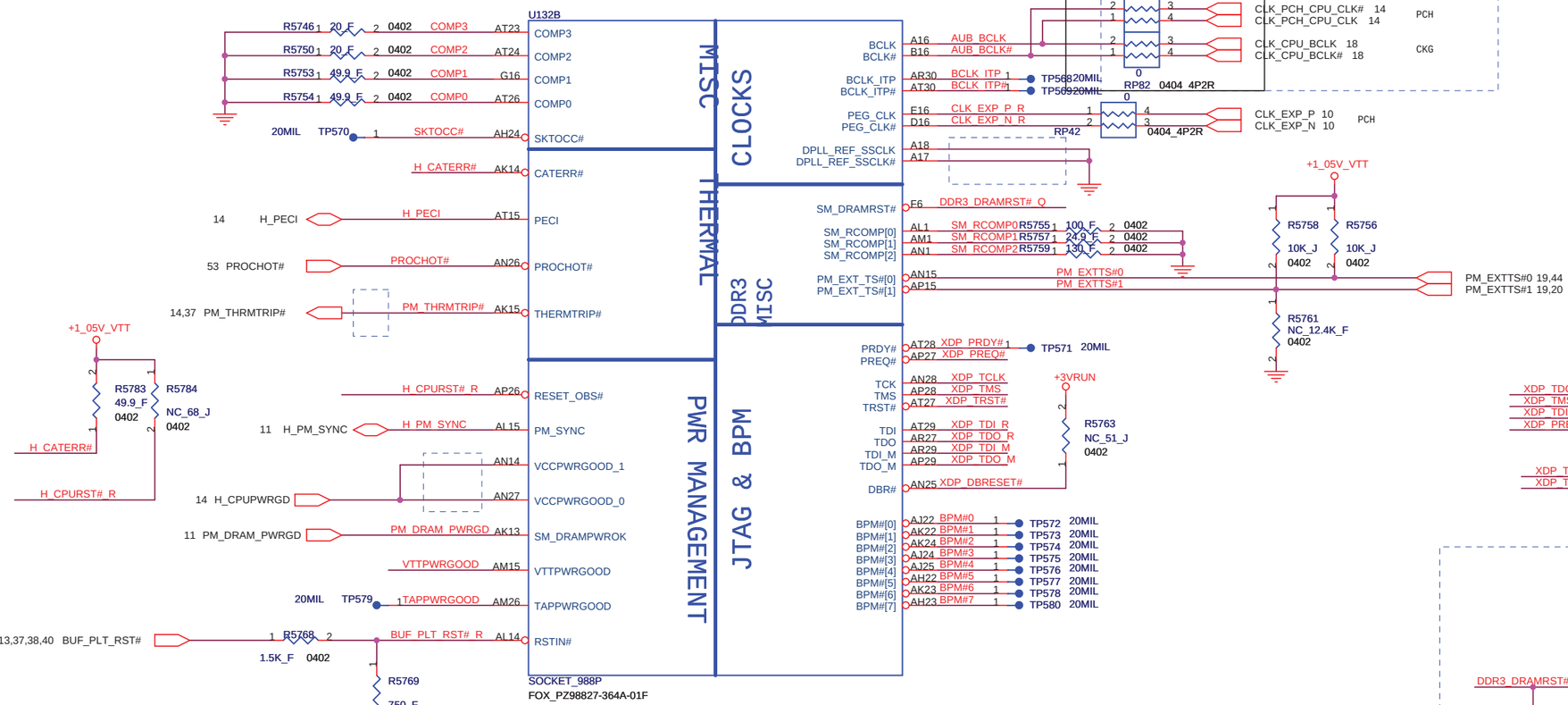
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	ARD (DMI,PEG,FDI)	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Thursday, November 19, 2009	Sheet 2 of 73	

For Disable Arrandale Graphic
DPLL_REF_SSCLK and DPLL_REF_SSCLK# can be connected to GND on
Arrandale directly if motherboard only supports discrete graphics.

Layout Note:
In order to minimize resistance, use thick traces to route all COMP signals, use 10-mils (0.254-mm) wide trace for routing less than 500 mils (12.7 mm), or 20-mils (0.508-mm) wide trace for routing between 500 mils (12.7 mm) and 1000 mils(25.4 mm). Keep 20-mils (0.508-mm) spacing to any other signals in order to minimize crosstalk.

2009.10.19
Change RP81 TO NC
Change RP82 TO mount



DVT2 change to SOCKET_988A

7/24 [DVT] INTEL S3 Power Reduction Solution.

7/24 [DVT] INTEL S3 Power Reduction Solution.

2009/09/10
Change C6131 from NC to 0.047U for DVT2

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD (CLK,MISC,JTAG)	
Size: Custom	Document Number: M9A0_MP	Rev: 1.1
Date: Thursday, November 19, 2009	Sheet 3 of 73	

U132C

DDR SYSTEM MEMORY A

19 M_A_DQ[63:0]

M_A_DQ0	A10	SA_DQ[0]
M_A_DQ1	C10	SA_DQ[1]
M_A_DQ2	C7	SA_DQ[2]
M_A_DQ3	A7	SA_DQ[3]
M_A_DQ4	B10	SA_DQ[4]
M_A_DQ5	D10	SA_DQ[5]
M_A_DQ6	E10	SA_DQ[6]
M_A_DQ7	A8	SA_DQ[7]
M_A_DQ8	D8	SA_DQ[8]
M_A_DQ9	F10	SA_DQ[9]
M_A_DQ10	E6	SA_DQ[10]
M_A_DQ11	F7	SA_DQ[11]
M_A_DQ12	E9	SA_DQ[12]
M_A_DQ13	B7	SA_DQ[13]
M_A_DQ14	E7	SA_DQ[14]
M_A_DQ15	C6	SA_DQ[15]
M_A_DQ16	H10	SA_DQ[16]
M_A_DQ17	G8	SA_DQ[17]
M_A_DQ18	K7	SA_DQ[18]
M_A_DQ19	J8	SA_DQ[19]
M_A_DQ20	G7	SA_DQ[20]
M_A_DQ21	G10	SA_DQ[21]
M_A_DQ22	J7	SA_DQ[22]
M_A_DQ23	J10	SA_DQ[23]
M_A_DQ24	L7	SA_DQ[24]
M_A_DQ25	M6	SA_DQ[25]
M_A_DQ26	M8	SA_DQ[26]
M_A_DQ27	L9	SA_DQ[27]
M_A_DQ28	L6	SA_DQ[28]
M_A_DQ29	K8	SA_DQ[29]
M_A_DQ30	N8	SA_DQ[30]
M_A_DQ31	P9	SA_DQ[31]
M_A_DQ32	AH5	SA_DQ[32]
M_A_DQ33	AE5	SA_DQ[33]
M_A_DQ34	AK6	SA_DQ[34]
M_A_DQ35	AK7	SA_DQ[35]
M_A_DQ36	AE6	SA_DQ[36]
M_A_DQ37	AG5	SA_DQ[37]
M_A_DQ38	AJ7	SA_DQ[38]
M_A_DQ39	AJ6	SA_DQ[39]
M_A_DQ40	AJ10	SA_DQ[40]
M_A_DQ41	AJ9	SA_DQ[41]
M_A_DQ42	AL10	SA_DQ[42]
M_A_DQ43	AK12	SA_DQ[43]
M_A_DQ44	AK8	SA_DQ[44]
M_A_DQ45	AL7	SA_DQ[45]
M_A_DQ46	AK11	SA_DQ[46]
M_A_DQ47	AL8	SA_DQ[47]
M_A_DQ48	AN8	SA_DQ[48]
M_A_DQ49	AM10	SA_DQ[49]
M_A_DQ50	AR11	SA_DQ[50]
M_A_DQ51	AL11	SA_DQ[51]
M_A_DQ52	AM9	SA_DQ[52]
M_A_DQ53	AN9	SA_DQ[53]
M_A_DQ54	AT11	SA_DQ[54]
M_A_DQ55	AP12	SA_DQ[55]
M_A_DQ56	AM12	SA_DQ[56]
M_A_DQ57	AN12	SA_DQ[57]
M_A_DQ58	AM13	SA_DQ[58]
M_A_DQ59	AT14	SA_DQ[59]
M_A_DQ60	AT12	SA_DQ[60]
M_A_DQ61	AL13	SA_DQ[61]
M_A_DQ62	AR14	SA_DQ[62]
M_A_DQ63	AP14	SA_DQ[63]

19 M_A_BS0	AC3	SA_BS[0]
19 M_A_BS1	AB2	SA_BS[1]
19 M_A_BS2	U7	SA_BS[2]

19 M_A_CAS#	AE1	SA_CAS#
19 M_A_RAS#	AB3	SA_RAS#
19 M_A_WE#	AE9	SA_WE#

SA_CK[0]	AA6	M_CLK_DDR0 19
SA_CK#[0]	AA7	M_CLK_DDR#0 19
SA_CKE[0]	P7	M_CKE0 19
SA_CK[1]	Y6	M_CLK_DDR1 19
SA_CK#[1]	Y5	M_CLK_DDR#1 19
SA_CKE[1]	P6	M_CKE1 19
SA_CS#[0]	AE2	M_CS#0 19
SA_CS#[1]	AE8	M_CS#1 19
SA_ODT[0]	AD8	M_ODT0 19
SA_ODT[1]	AF9	M_ODT1 19

SA_DM[0]	B9	M_A_DM0	M_A_DM[7:0] 19
SA_DM[1]	D7	M_A_DM1	
SA_DM[2]	H7	M_A_DM2	
SA_DM[3]	M7	M_A_DM3	
SA_DM[4]	AG6	M_A_DM4	
SA_DM[5]	AM7	M_A_DM5	
SA_DM[6]	AN10	M_A_DM6	
SA_DM[7]	AN13	M_A_DM7	

SA_DQS[0]	C9	M_A_DQS#0	M_A_DQS#[7:0] 19
SA_DQS[1]	F8	M_A_DQS#1	
SA_DQS[2]	J9	M_A_DQS#2	
SA_DQS[3]	N9	M_A_DQS#3	
SA_DQS[4]	AH7	M_A_DQS#4	
SA_DQS[5]	AK9	M_A_DQS#5	
SA_DQS[6]	AP11	M_A_DQS#6	
SA_DQS[7]	AT13	M_A_DQS#7	

SA_DQS[0]	C8	M_A_DQS0	M_A_DQS[7:0] 19
SA_DQS[1]	F9	M_A_DQS1	
SA_DQS[2]	H9	M_A_DQS2	
SA_DQS[3]	M9	M_A_DQS3	
SA_DQS[4]	AH8	M_A_DQS4	
SA_DQS[5]	AK10	M_A_DQS5	
SA_DQS[6]	AN11	M_A_DQS6	
SA_DQS[7]	AR13	M_A_DQS7	

SA_MA[0]	Y3	M_A_A0	M_A_A[15:0] 19
SA_MA[1]	W1	M_A_A1	
SA_MA[2]	AA8	M_A_A2	
SA_MA[3]	AA3	M_A_A3	
SA_MA[4]	V1	M_A_A4	
SA_MA[5]	AA9	M_A_A5	
SA_MA[6]	V8	M_A_A6	
SA_MA[7]	T1	M_A_A7	
SA_MA[8]	Y9	M_A_A8	
SA_MA[9]	U6	M_A_A9	
SA_MA[10]	AD4	M_A_A10	
SA_MA[11]	T2	M_A_A11	
SA_MA[12]	U3	M_A_A12	
SA_MA[13]	AG8	M_A_A13	
SA_MA[14]	T3	M_A_A14	
SA_MA[15]	V9	M_A_A15	

SOCKET_988P

FOX_PZ98827-364A-01F

DVT2 change to SOCKET_988A

U132D

DDR SYSTEM MEMORY - B

20 M_B_DQ[63:0]

M_B_DQ0	B5	SB_DQ[0]
M_B_DQ1	A5	SB_DQ[1]
M_B_DQ2	C3	SB_DQ[2]
M_B_DQ3	B3	SB_DQ[3]
M_B_DQ4	E4	SB_DQ[4]
M_B_DQ5	A6	SB_DQ[5]
M_B_DQ6	A4	SB_DQ[6]
M_B_DQ7	C4	SB_DQ[7]
M_B_DQ8	D1	SB_DQ[8]
M_B_DQ9	D2	SB_DQ[9]
M_B_DQ10	F2	SB_DQ[10]
M_B_DQ11	F1	SB_DQ[11]
M_B_DQ12	C2	SB_DQ[12]
M_B_DQ13	F5	SB_DQ[13]
M_B_DQ14	F3	SB_DQ[14]
M_B_DQ15	G4	SB_DQ[15]
M_B_DQ16	H6	SB_DQ[16]
M_B_DQ17	G2	SB_DQ[17]
M_B_DQ18	J6	SB_DQ[18]
M_B_DQ19	J3	SB_DQ[19]
M_B_DQ20	G1	SB_DQ[20]
M_B_DQ21	G5	SB_DQ[21]
M_B_DQ22	J2	SB_DQ[22]
M_B_DQ23	J1	SB_DQ[23]
M_B_DQ24	J5	SB_DQ[24]
M_B_DQ25	K2	SB_DQ[25]
M_B_DQ26	L3	SB_DQ[26]
M_B_DQ27	M1	SB_DQ[27]
M_B_DQ28	K5	SB_DQ[28]
M_B_DQ29	K4	SB_DQ[29]
M_B_DQ30	M4	SB_DQ[30]
M_B_DQ31	N5	SB_DQ[31]
M_B_DQ32	AF3	SB_DQ[32]
M_B_DQ33	AG1	SB_DQ[33]
M_B_DQ34	AJ3	SB_DQ[34]
M_B_DQ35	AK1	SB_DQ[35]
M_B_DQ36	AG4	SB_DQ[36]
M_B_DQ37	AG3	SB_DQ[37]
M_B_DQ38	AJ4	SB_DQ[38]
M_B_DQ39	AH4	SB_DQ[39]
M_B_DQ40	AK3	SB_DQ[40]
M_B_DQ41	AK4	SB_DQ[41]
M_B_DQ42	AM6	SB_DQ[42]
M_B_DQ43	AN2	SB_DQ[43]
M_B_DQ44	AK5	SB_DQ[44]
M_B_DQ45	AK2	SB_DQ[45]
M_B_DQ46	AM4	SB_DQ[46]
M_B_DQ47	AM3	SB_DQ[47]
M_B_DQ48	AP3	SB_DQ[48]
M_B_DQ49	AN5	SB_DQ[49]
M_B_DQ50	AT4	SB_DQ[50]
M_B_DQ51	AN6	SB_DQ[51]
M_B_DQ52	AN4	SB_DQ[52]
M_B_DQ53	AN3	SB_DQ[53]
M_B_DQ54	AT5	SB_DQ[54]
M_B_DQ55	AT6	SB_DQ[55]
M_B_DQ56	AN7	SB_DQ[56]
M_B_DQ57	AP6	SB_DQ[57]
M_B_DQ58	AP8	SB_DQ[58]
M_B_DQ59	AT9	SB_DQ[59]
M_B_DQ60	AT7	SB_DQ[60]
M_B_DQ61	AP9	SB_DQ[61]
M_B_DQ62	AR10	SB_DQ[62]
M_B_DQ63	AT10	SB_DQ[63]

20 M_B_BS0	AB1	SB_BS[0]
20 M_B_BS1	W5	SB_BS[1]
20 M_B_BS2	R7	SB_BS[2]

20 M_B_CAS#	AC5	SB_CAS#
20 M_B_RAS#	Y7	SB_RAS#
20 M_B_WE#	AC6	SB_WE#

SB_CK[0]	W8	M_CLK_DDR2 20
SB_CK#[0]	W9	M_CLK_DDR#2 20
SB_CKE[0]	M3	M_CKE2 20
SB_CK[1]	V7	M_CLK_DDR3 20
SB_CK#[1]	V6	M_CLK_DDR#3 20
SB_CKE[1]	M2	M_CKE3 20
SB_CS#[0]	AB8	M_CS#2 20
SB_CS#[1]	AD6	M_CS#3 20
SB_ODT[0]	AC7	M_ODT2 20
SB_ODT[1]	AD1	M_ODT3 20

SB_DM[0]	D4	M_B_DM0	M_B_DM[7:0] 20
SB_DM[1]	F1	M_B_DM1	
SB_DM[2]	H3	M_B_DM2	
SB_DM[3]	K1	M_B_DM3	
SB_DM[4]	AH1	M_B_DM4	
SB_DM[5]	AL2	M_B_DM5	
SB_DM[6]	AR4	M_B_DM6	
SB_DM[7]	AT8	M_B_DM7	

SB_DQS#[0]	D5	M_B_DQS#0	M_B_DQS#[7:0] 20
SB_DQS#[1]	F4	M_B_DQS#1	
SB_DQS#[2]	J4	M_B_DQS#2	
SB_DQS#[3]	L4	M_B_DQS#3	
SB_DQS#[4]	AH2	M_B_DQS#4	
SB_DQS#[5]	AL4	M_B_DQS#5	
SB_DQS#[6]	AR5	M_B_DQS#6	
SB_DQS#[7]	AR8	M_B_DQS#7	

SB_DQS[0]	C5	M_B_DQS0	M_B_DQS[7:0] 20
SB_DQS[1]	E3	M_B_DQS1	
SB_DQS[2]	H4	M_B_DQS2	
SB_DQS[3]	M5	M_B_DQS3	
SB_DQS[4]	AG2	M_B_DQS4	
SB_DQS[5]	AL5	M_B_DQS5	
SB_DQS[6]	AP5	M_B_DQS6	
SB_DQS[7]	AR7	M_B_DQS7	

SB_MA[0]	U5	M_B_A0	M_B_A[15:0] 20
SB_MA[1]	V2	M_B_A1	
SB_MA[2]	T5	M_B_A2	
SB_MA[3]	V3	M_B_A3	
SB_MA[4]	R1	M_B_A4	
SB_MA[5]	T8	M_B_A5	
SB_MA[6]	R2	M_B_A6	
SB_MA[7]	R6	M_B_A7	
SB_MA[8]	R4	M_B_A8	
SB_MA[9]	R5	M_B_A9	
SB_MA[10]	AB5	M_B_A10	
SB_MA[11]	P3	M_B_A11	
SB_MA[12]	R3	M_B_A12	
SB_MA[13]	AF7	M_B_A13	
SB_MA[14]	P5	M_B_A14	
SB_MA[15]	N1	M_B_A15	

SOCKET_988P

FOX_PZ98827-364A-01F

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	ARD (DDR3)	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Thursday, November 19, 2009	Sheet 4 of 73	

2009/09/12
Delete R5785 0ohm resistor for voltage drop problem

48A (ARD SV)

VHCORE
C6084 22U_6.3V_M 0805_X5R
C6085 22U_6.3V_M 0805_X5R
C6086 22U_6.3V_M 0805_X5R
C6087 22U_6.3V_M 0805_X5R
C6088 NC_22U_6.3V_M 0805_X5R

VHCORE
C6092 22U_6.3V_M 0805_X5R
C6093 22U_6.3V_M 0805_X5R
C6094 22U_6.3V_M 0805_X5R
C6098 22U_6.3V_M 0805_X5R
C6103 22U_6.3V_M 0805_X5R

VHCORE
C6104 22U_6.3V_M 0805_X5R
C6105 22U_6.3V_M 0805_X5R
C6106 NC_22U_6.3V_M 0805_X5R
C6107 22U_6.3V_M 0805_X5R
C6108 NC_22U_6.3V_M 0805_X5R

VHCORE
C6109 NC_22U_6.3V_M 0805_X5R
C6110 10U_10V_M 0805_X5R
C6111 10U_10V_M 0805_X5R
C6112 10U_10V_M 0805_X5R
C6113 10U_10V_M 0805_X5R

VHCORE
C6116 10U_10V_M 0805_X5R
C6117 10U_10V_M 0805_X5R
C6118 10U_10V_M 0805_X5R
C6119 10U_10V_M 0805_X5R
C6120 10U_10V_M 0805_X5R

VHCORE
C6121 10U_10V_M 0805_X5R
C6122 10U_10V_M 0805_X5R
C6123 10U_10V_M 0805_X5R
C6124 10U_10V_M 0805_X5R
C6125 10U_10V_M 0805_X5R

VHCORE
C6126 10U_10V_M 0805_X5R
C6127 10U_10V_M 0805_X5R
C6128 22P_50V_J 0402_NPO
C6129 22P_50V_J 0402_NPO

For RF Noise

U132F

VHCORE
AG35 AG34 AG33 AG32 AG31 AG30 AG29 AG28 AG27 AG26 AF35 AF34 AF33 AF32 AF31 AF30 AF29 AF28 AF27 AF26 AD35 AD34 AD33 AD32 AD31 AD30 AD29 AD28 AD27 AD26 AC35 AC34 AC33 AC32 AC31 AC30 AC29 AC28 AC27 AC26 AA35 AA34 AA33 AA32 AA31 AA30 AA29 AA28 AA27 AA26 Y35 Y34 Y33 Y32 Y31 Y30 Y29 Y28 Y27 Y26 V35 V34 V33 V32 V31 V30 V29 V28 V27 V26 U35 U34 U33 U32 U31 U30 U29 U28 U27 U26 R35 R34 R33 R32 R31 R30 R29 R28 R27 R26 P35 P34 P33 P32 P31 P30 P29 P28 P27 P26
VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21 VCC22 VCC23 VCC24 VCC25 VCC26 VCC27 VCC28 VCC29 VCC30 VCC31 VCC32 VCC33 VCC34 VCC35 VCC36 VCC37 VCC38 VCC39 VCC40 VCC41 VCC42 VCC43 VCC44 VCC45 VCC46 VCC47 VCC48 VCC49 VCC50 VCC51 VCC52 VCC53 VCC54 VCC55 VCC56 VCC57 VCC58 VCC59 VCC60 VCC61 VCC62 VCC63 VCC64 VCC65 VCC66 VCC67 VCC68 VCC69 VCC70 VCC71 VCC72 VCC73 VCC74 VCC75 VCC76 VCC77 VCC78 VCC79 VCC80 VCC81 VCC82 VCC83 VCC84 VCC85 VCC86 VCC87 VCC88 VCC89 VCC90 VCC91 VCC92 VCC93 VCC94 VCC95 VCC96 VCC97 VCC98 VCC99 VCC100

1.1V RAIL POWER

VTT0_1 VTT0_2 VTT0_3 VTT0_4 VTT0_5 VTT0_6 VTT0_7 VTT0_8 VTT0_9 VTT0_10 VTT0_11 VTT0_12 VTT0_13 VTT0_14 VTT0_15 VTT0_16 VTT0_17 VTT0_18 VTT0_19 VTT0_20 VTT0_21 VTT0_22 VTT0_23 VTT0_24 VTT0_25 VTT0_26 VTT0_27 VTT0_28 VTT0_29 VTT0_30 VTT0_31 VTT0_32
AH14 AH12 AH11 AH10 J14 J13 H14 H12 G14 G13 G12 G11 F14 F13 F12 F11 E14 E12 D14 D13 D12 D11 C14 C13 C12 C11 B14 B12 A14 A13 A12 A11

VTT0_33 VTT0_34 VTT0_35 VTT0_36 VTT0_37 VTT0_38 VTT0_39 VTT0_40 VTT0_41 VTT0_42 VTT0_43 VTT0_44
AE10 AE10 AC10 AB10 Y10 W10 U10 T10 J12 J11 J16 J15

18A(ARD SV) (VTT)

+1_05V_VTT
C6095 10U_10V_M 0805_X5R
C6082 10U_10V_M 0805_X5R
C6096 10U_10V_M 0805_X5R
C6097 10U_10V_M 0805_X5R
C6083 10U_10V_M 0805_X5R
C6089 22U_6.3V_M 0805_X5R
C6090 22U_6.3V_M 0805_X5R
C6091 22U_6.3V_M 0805_X5R
C6099 10U_10V_M 0805_X5R
C6100 10U_10V_M 0805_X5R
C6101 NC_10U_10V_M 0805_X5R
C6102 NC_10U_10V_M 0805_X5R

2009.10.23
Delete R5786 for PVT

18A(ARD SV) (VTT)

+1_05V_VTT
C6114 22U_6.3V_M 0805_X5R
C6115 22U_6.3V_M 0805_X5R
+1_05V_VTT_43
+1_05V_VTT_44
R5787 0 0603
R5788 0 0603
+1_05V_VTT

POWER
CPU VIDS

PSI# AN33 PSI# 53,54
VID[0] AK35 VID0 53,54
VID[1] AK33 VID1 53,54
VID[2] AK34 VID2 53,54
VID[3] AL35 VID3 53,54
VID[4] AL33 VID4 53,54
VID[5] AM33 VID5 53,54
VID[6] AM35 VID6 53,54
PROC_DPRSLPVR AM34 PM_DPRSLPVR 53,54
VTT_SELECT G15 1 TP689 20MIL

SENSE LINES

ISENSE AN35 IMVP_IMON 53
VCC_SENSE AJ34 VCCSENSE VCCSENSE 53
VSS_SENSE AJ35 VSSSENSE VSSSENSE 53
VTT_SENSE B15 VTT_SENSE 58
VSS_SENSE_VTT A15 VSS_SENSE_VTT TP581 20MIL

VHCORE
R5790 100_F 0402
R5791 100_F 0402

SOCKET_988P
FOX_PZ98827-364A-01F

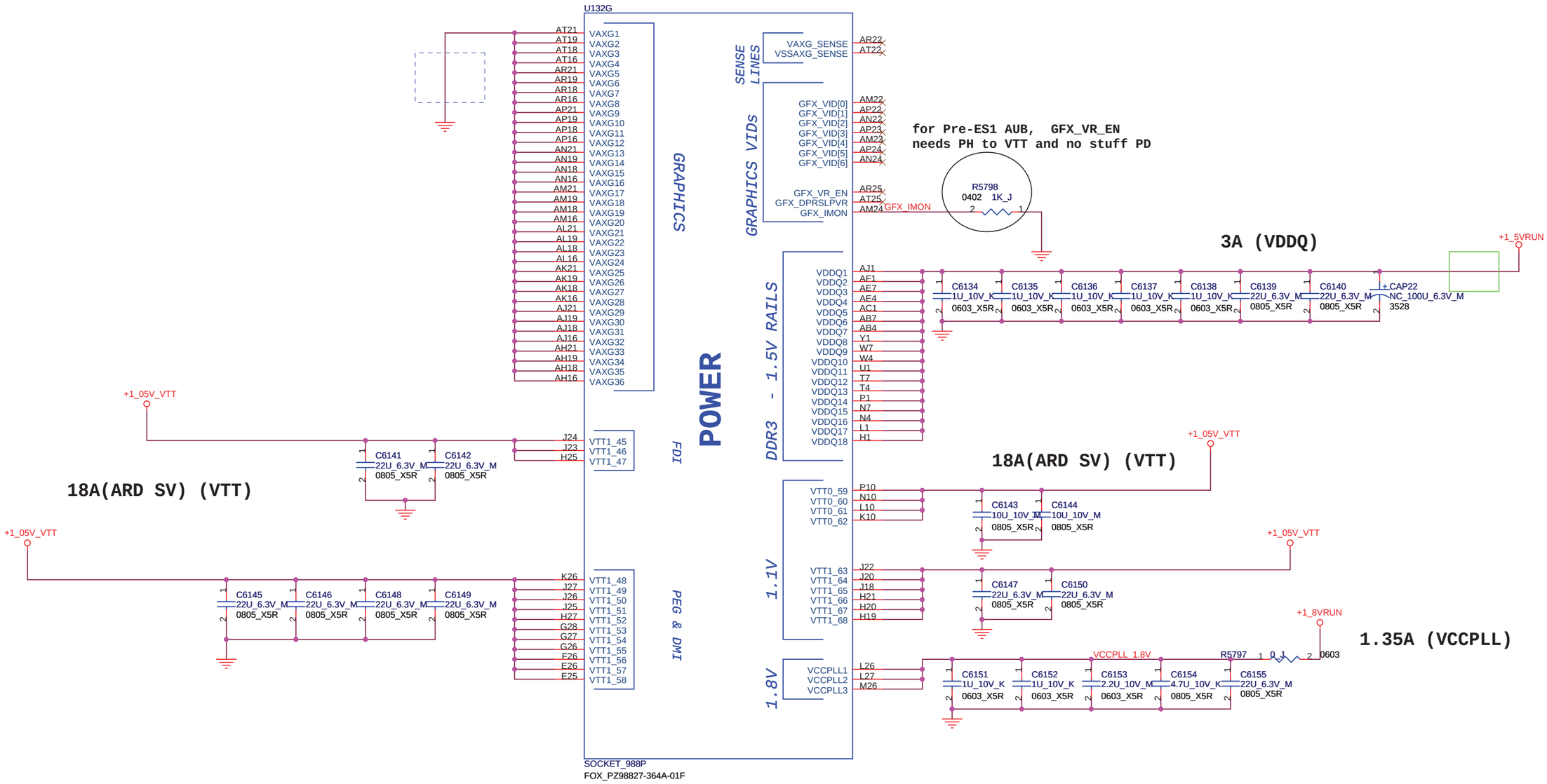
DVT2 change to SOCKET_988A

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	ARD(POWER)	
Size: Custom	Document Number: M9A0_MP	Rev: 1.1
Date: Wednesday, October 28, 2009	Sheet 5 of 73	

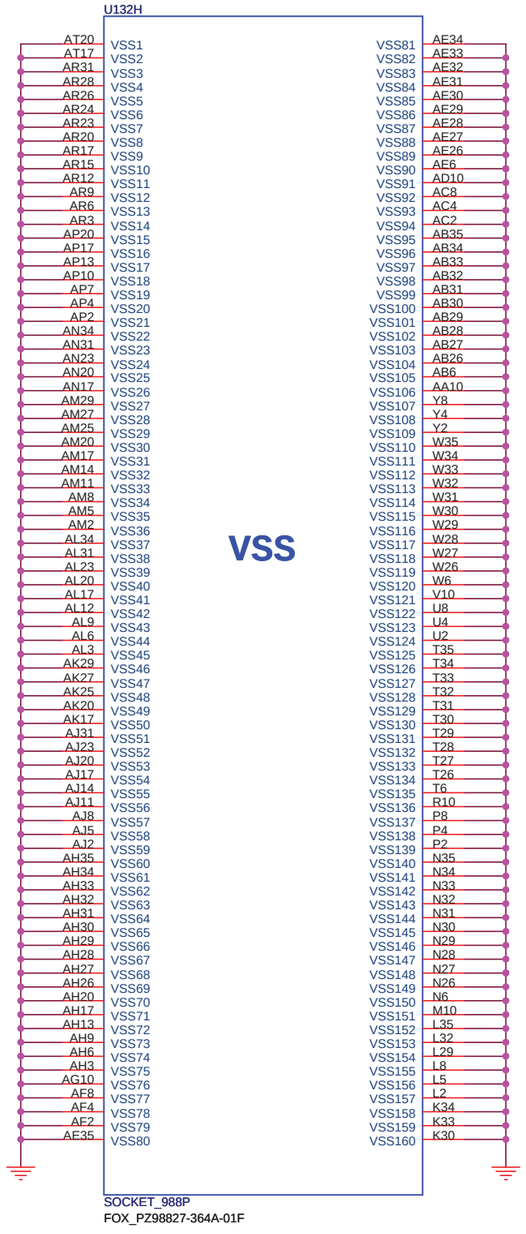
For Disable Arrandale Graphic
VAXG should be connected to GND when disable iGPU.

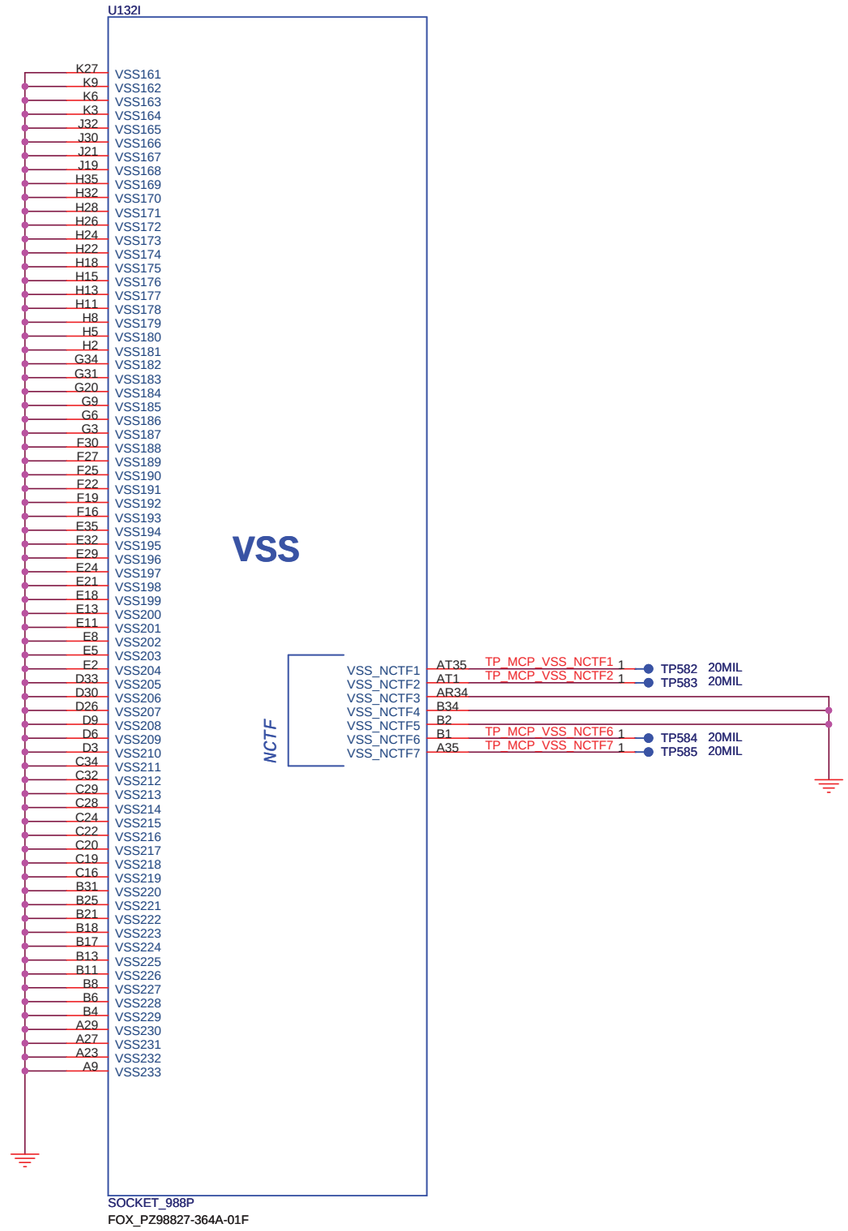
For Disable Arrandale Graphic
VAXG_SENSE and VSSAXG_SENSE on Arrandale can be left as no connect.



DVT2 change to SOCKET_988A

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD (GRAPHICS POWER)	
Size: Custom	Document Number: M9A0_MP	Rev: 1.1
Date: Wednesday, September 23, 2009	Sheet 6 of 73	





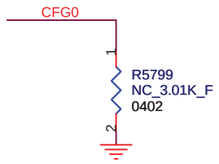
DVT2 change to SOCKET_988A

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD (GND)	
Size: Custom	Document Number: M9A0_MP	Rev: 1.1
Date: Wednesday, September 23, 2009	Sheet 7 of 73	

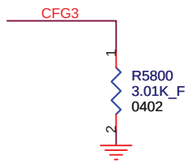
PCI Express Configuration Select
CFG0 1 : Single PEG * default
0 : Bifurcation enable

3393727 The VIL Voltage DC Specification for CFG[0] Pin is in Violation of the EDS Value by a Large Amount
The Clarksfield EDS Vol1 documents the CFG[1:0] pins for PCI Express Port Bifurcation, the straps may not work correctly when using a pull down resistor of value other than 250 Ohms to drive a value of zero on the CFG[0] pin. When left floating a value of one is sensed and there is no impact in this case.

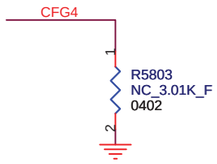
CFG pin is latch on the rising edge of CPU powergood.

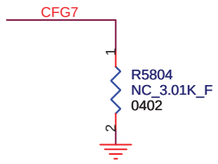


CFG3 PCI Express Static Lane Reversal
CFG3 1 : Normal
0 : Lane Numbers Reversed *
15 ->0 , 14-> 1 , ...



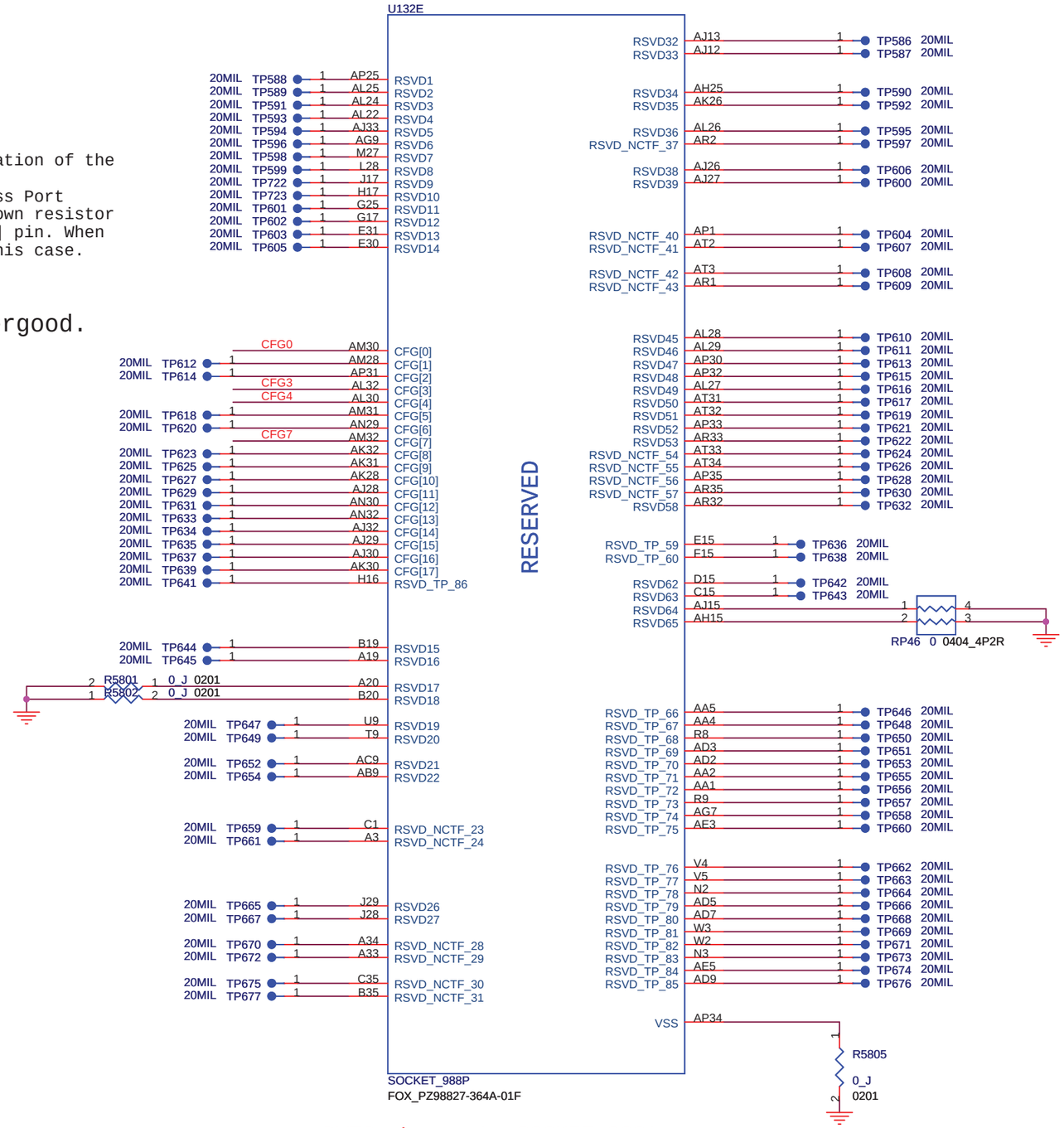
CFG4 Display Port Presence
CFG4 1 : Disabled ; No Physical Display Port attached to Embedded Display Port
0 : Enable ; An external Display Port device is connected to the Embedded Display Port





2611030 PCI Express Interface May Not Meet PCI Express 2.0 Jitter Specifications

Intel has determined that the workaround (3.01K pull down to Vss on signal CFG[7]) is not robust. Intel recommends not implementing this workaround at this time (CFG[7] should not be pulled down).
Intel recommends not to test for PCI-E Express 2.0 Jitter specification compliance for the affected steppings.



DVT2 change to SOCKET_988A

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	ARD (RESERVED)		
Size A3	Document Number M9A0_MP		Rev 1.1
Date: Wednesday, September 23, 2009	Sheet 8 of 73		

RTCRST#

VccRTC

18~25mS

The traces inside this block should be wider.

2009.0925
change C6156,C6157 from 12p to 15p for vendor requet

+ECVCC

VCCRTC

D24 SD103AWS

C6158 1U_6.3V_M 0402_X5R

R5810 20K_F 0402

C6159 1U_6.3V_K 0402_X5R

JP1 OPEN_JUMP_OPEN2

tpc40b_50 TP678

R5812 510_F 0402

R5813 1M_J 0402

RTC2

R5816 510_F 0402

CN49 FOX_HS8202E-LH HEADER_2P

RTC1

R5815 20K_J 0402

C6160 1U_6.3V_M 0402_X5R

C6156 0402_NPO 15P_50V_K

Y9 32.768KHZ_12.5P_10PPM Q13MC3061001800

C6157 15P_50V_K 0402_NPO

6 mils

R5807 10M_J 0402

RTC_32KX1

RTC_32KX2

RTCRST#

SRTCRST#

SM_INTRUDER#

VCCRTC R5814 330K_F 0402 INTVRMEN

U134A

RTC

RTCX1 B13
RTCX2 D13
RTCRST# C14
SRTCRST# D17
INTRUDER# A16
INTVRMEN A14

LPC

FWH0 / LAD0 D33 LPC_AD0 LPC_AD0 37,38
FWH1 / LAD1 B33 LPC_AD1 LPC_AD1 37,38
FWH2 / LAD2 C32 LPC_AD2 LPC_AD2 37,38
FWH3 / LAD3 A32 LPC_AD3 LPC_AD3 37,38
FWH4 / LFRAME# C34 LPC_FRAME# LPC_FRAME# 37,38
LDRQ0# A34 LPC_DRQ#0 LPC_DRQ#0 38
LDRQ1# / GPIO23 F34 TP679 20MIL
SERIRQ AB9 INT_SERIRQ INT_SERIRQ 37,38

IHDA

IHDA_BITCLK A30
IHDA_SYNC D29
43 HDA_SPKR HDA_SPKR P1
IHDA_RESET# C30
43 HDA_CODEC_SDATAIN0 G30
20MIL TP680 F30
20MIL TP681 E32
20MIL TP682 TP_HDA_SDIN3 F32
IHDA_SDATAO B29
HDA_DOCK_EN# H32
20MIL TP683 HDA_DOCK_RST# J30

HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN# / GPIO33
HDA_DOCK_RST# / GPIO13

SATA

SATA0RXN AK7 SATA_RXN0 SATA_RXN0 42
SATA0RXP AK6 SATA_RXP0 SATA_RXP0 42
SATA0TXN AK11 SATA_TXN0 SATA_TXN0 42
SATA0TXP AK9 SATA_TXP0 SATA_TXP0 42

HDD

SATA1RXN AH6 SATA_RXN1 SATA_RXN1 42
SATA1RXP AH5 SATA_RXP1 SATA_RXP1 42
SATA1TXN AH9 SATA_TXN1 SATA_TXN1 42
SATA1TXP AH8 SATA_TXP1 SATA_TXP1 42

ODD

SATA2RXN AE11
SATA2RXP AF9
SATA2TXN AF7
SATA2TXP AF6
SATA3RXN AH3
SATA3RXP AH1
SATA3TXN AF3
SATA3TXP AF1
SATA4RXN AD9
SATA4RXP AD8
SATA4TXN AD6
SATA4TXP AD5
SATA5RXN AD3
SATA5RXP AD1
SATA5TXN AB3
SATA5TXP AB1
SATAICOMPO AF16 VCC_SATA R5826 37.4_F 0402 +1.05V_VCC_SATA
SATAICOMPI AF15

JTAG

JTAG_TCK M3
JTAG_TMS K3
JTAG_TDI K1
JTAG_TDO J2
JTAG_RST# J4

20MIL TP684
20MIL TP685
20MIL TP686
20MIL TP687
20MIL TP688

SPI

SPI0_CLK BA2
SPI_ROM_CS0# AV3
20MIL TP692 AY3
SPI0_MOSI AY1
SPI_MISO_L AV1

SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO

SATALED# T3 SATA_LED# 50
SATA0GP / GPIO21 Y9 SATA0GP
SATA1GP / GPIO19 V1 SATA1GP

+3VRUN R5998 10K_J 0402

JTAG_TCK R5908 51R_F 0402

ibexpeak-M
null

For DVT2,
ARD(QS)+PM55(MP)+4M SPI ROM

+3VRUN

INT_SERIRQ R5806 10K_J 0201
SATA0GP R5808 10K_J 0201
SATA1GP R5809 10K_J 0201

[HDA_DOCK_EN#/GPIO33]
Low (0) – Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features.
High (1) – Security measure defined in the Flash Descriptor will be enabled

+3VRUN
+ECVCC
R5817 1K_J 0402
R5818 NC_4.7K_J 0402
R5819 0_J 0402
HDA_DOCK_EN#
37 FW_HW
R5820 100_J 0402
Q180 2N7002W
R5821 NC_1K_J 0402

+3VALW
R5822 10K_J 0201
HDA_DOCK_RST#

Stuff for No-reboot
Low=Default
High=No-reboot

+3VRUN
R5823 NC_10K_J 0201
HDA_SPKR

+3VRUN
R5828 NC_1K_J 0402

RP94 33 0404_4P2R
43 HDA_CODEC_SYNC
43 HDA_CODEC_SDATAOUT
IHDA_SYNC
IHDA_SDATAO

RP93 33 0404_4P2R
IHDA_BITCLK
IHDA_RESET#
HDA_CODEC_BITCLK 43
HDA_CODEC_RST# 43

When int. PLL VR is enabled, HDA_SYNC is VCCVRM 1.5V/1.8V strap (default: L for 1.8V)

SPI0_MISO_R R5832 15_F 0402 SPI_MISO_L

EXTERNAL SPI0 ROM INTERFACE(FOR U98)

+ECVCC
SPI0_CLK
SPI0_MOSI
SPI0_MISO_R
SPI_ROM_CS0#
MB_FLASH0_EN
CARD_INSERT0
14 MB_FLASH0_EN
CN50 FOX_GB5RF120-1203-7H FPC CONN_12P

+ECVCC
C6161 0.1U_16V_Y 0402_Y5V
U135 MC74HC1G32DTT1G
CARD_INSERT0
SPI_ROM_CS0#
SPI0_CS#
R5833 10K_J 0402
R5836 NC_0_J 0402

U98 SPI ROM-0

del R5835 and D25,
change VCC0 to +3VRUN

+3VRUN
R5834 1K_J 0402
HOLD0#
+3VRUN
C6163 4.7U_10V_K 0805_X5R
C6164 1U_10V_K 0603_X5R
+3VRUN
R5838 3.3K_J 0402
R5842 NC_1K_J 0402
SPI0_CS#
SPI0_MISO_R
WP#0
U98
CS# VCC
SO/SIO1 HOLD#
WP#/ACC SCLK
GND SI/SIO0
FLASH_SOP-8_85MHZ
MX25L3205DM2I-12G
+3VRUN
HOLD0#
SPI0_CLK
SPI0_MOSI

SPI ROM (BIOS)(4MB bit)

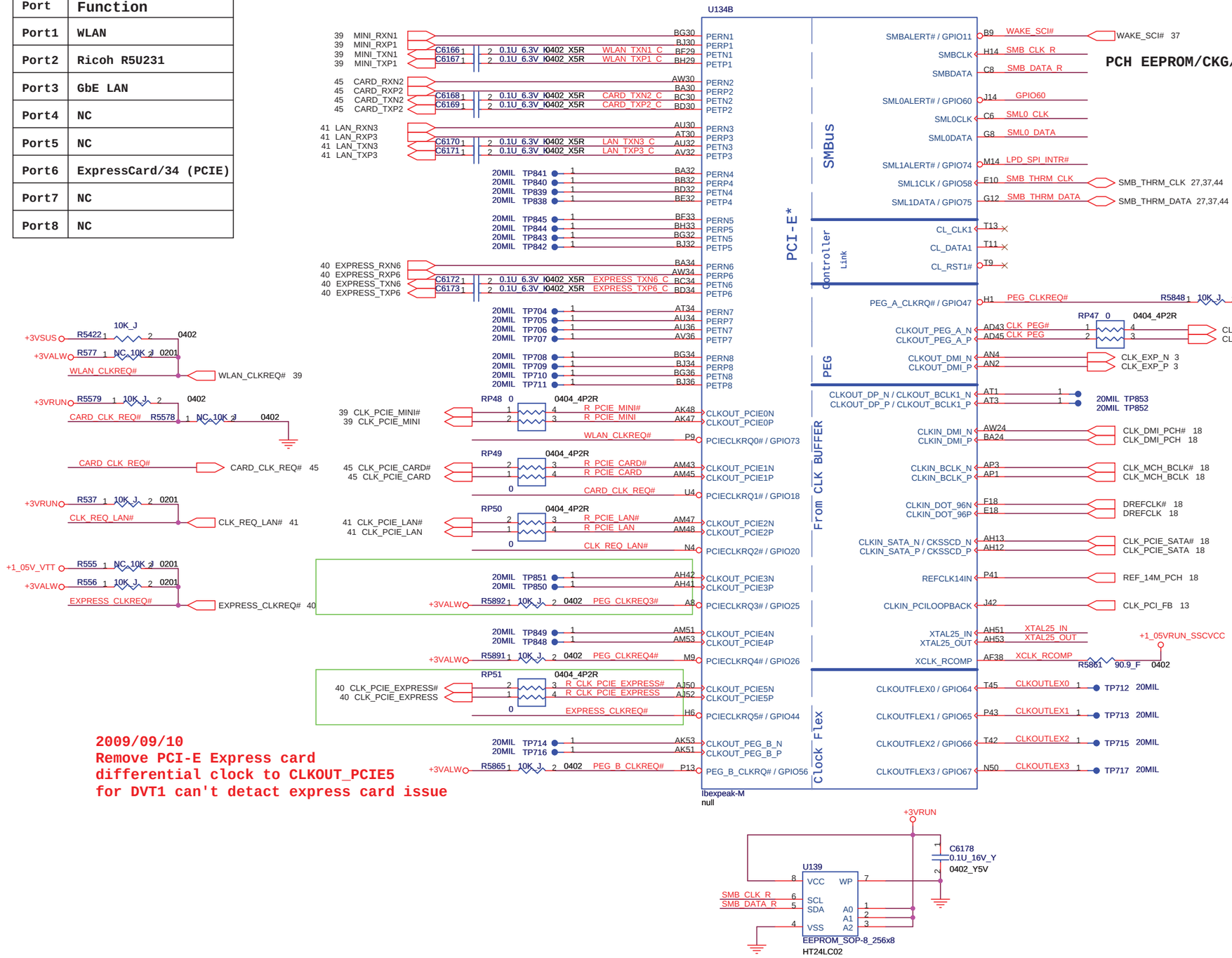
SPI0_CLK R6010 100K_J 0402
SPI0_MOSI R6011 100K_J 0402
SPI0_CS# R6012 100K_J 0402

add follow EDS

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (HDA,JTAG,SAT)	
Size: Custom	Document Number: M9A0_MP	Rev: 1.1
Date: Friday, October 23, 2009	Sheet 9 of 73	

PCI-E Port Table

Port	Function
Port1	WLAN
Port2	Ricoh R5U231
Port3	GbE LAN
Port4	NC
Port5	NC
Port6	ExpressCard/34 (PCIE)
Port7	NC
Port8	NC



2009/09/10
Remove PCI-E Express card differential clock to CLKOUT_PCIE5 for DVT1 can't detact express card issue

SMBus Address: AEH

Calpella Platform – Design Guide - Addendum / Update – Rev. 1.52 (Doc #414044).).
XTAL_IN should be pulled to GND via a 0ohm by default.
This pull-down resistor on XTAL_IN should only be un-stuffed when 25MHz crystal is used.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (PCI-E,SMBUS,CLK)	
Size: Custom	Document Number: M9A0_MP	Rev: 1.1
Date: Friday, October 23, 2009	Sheet 10 of 73	

For Disable Auburndale Graphic
In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH. FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The GFX_IMON,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).

U134C

DMI

2 DMI_RXN0 — DMI_RXN0 — BC24 — DMI0RXN
2 DMI_RXN1 — DMI_RXN1 — BJ22 — DMI1RXN
2 DMI_RXN2 — DMI_RXN2 — AW20 — DMI2RXN
2 DMI_RXN3 — DMI_RXN3 — BJ20 — DMI3RXN

2 DMI_RXP0 — DMI_RXP0 — BD24 — DMI0RXP
2 DMI_RXP1 — DMI_RXP1 — BG22 — DMI1RXP
2 DMI_RXP2 — DMI_RXP2 — BA20 — DMI2RXP
2 DMI_RXP3 — DMI_RXP3 — BG20 — DMI3RXP

2 DMI_TXN0 — DMI_TXN0 — BE22 — DMI0TXN
2 DMI_TXN1 — DMI_TXN1 — BF21 — DMI1TXN
2 DMI_TXN2 — DMI_TXN2 — BD20 — DMI2TXN
2 DMI_TXN3 — DMI_TXN3 — BE18 — DMI3TXN

2 DMI_TXP0 — DMI_TXP0 — BD22 — DMI0TXP
2 DMI_TXP1 — DMI_TXP1 — BH21 — DMI1TXP
2 DMI_TXP2 — DMI_TXP2 — BC20 — DMI2TXP
2 DMI_TXP3 — DMI_TXP3 — BD18 — DMI3TXP

+1_05V_VCC_EXP — R5869 1 49.9_F 2 0402 — DMI_COMP — BH25 — DMI_ZCOMP
BF25 — DMI_IRCOMP

FDI

FDI_RXN0 — BA18
FDI_RXN1 — BH17
FDI_RXN2 — BD16
FDI_RXN3 — BJ16
FDI_RXN4 — BA16
FDI_RXN5 — BE14
FDI_RXN6 — BA14
FDI_RXN7 — BC12

FDI_RXP0 — BB18
FDI_RXP1 — BF17
FDI_RXP2 — BC16
FDI_RXP3 — BG16
FDI_RXP4 — AW16
FDI_RXP5 — BD14
FDI_RXP6 — BB14
FDI_RXP7 — BD12

FDI_INT — BJ14
FDI_FSYNC0 — BF13
FDI_FSYNC1 — BH13
FDI_LSYNC0 — BJ12
FDI_LSYNC1 — BG14

System Power Management

38 SB_RST# — SB_RST# — T6 — SYS_RESET#
37,53 IMVP_PWRGD — R5894 1 2.2K_J 2 0402 — SYS_PWROK — M6 — SYS_PWROK
R5872 1 2.2K_J 2 0402 — PWROK — B17 — PWROK
3,37,57,58,59 RUN_PWRGD — R5874 1 0_J 2 0402 — R5873 1 NC_0_J 2 0402 — MPWROK_R — K5 — MEPWROK
R5875 1 NC_0_J 2 0402 — LAN_RST# — A10 — LAN_RST#
R5876 1 10K_J 2 0402
3 PM_DRAM_PWRGD — D9 — DRAMPWROK
37 PM_RSMRST# — R5877 1 2.2K_J 2 0402 — PM_RSMRST# R — C16 — RSMRST#
37 SUS_PWR_ACK — SUS_PWR_ACK — M1 — SUS_PWR_ACK / GPIO30
37 PWRBTN# — PWRBTN# — P5 — PWRBTN#
GPIO31 — P7 — ACPRESENT / GPIO31
PM_BATLOW# — A6 — BATLOW# / GPIO72
PM_RI# — F14 — RI#

WAKE# — J12 — PCIE_WAKE# F
CLKRUN# / GPIO32 — Y1 — PM_CLKRUN# — PM_CLKRUN# 37,38
SUS_STAT# / GPIO61 — P8 — PM_SUS_STAT# — PM_SUS_STAT# 38
SUSCLK / GPIO62 — E3 — PM_S4_STATE# — 1 TP718 20MIL
SLP_S5# / GPIO63 — E4 — PM_SLP_S5# — PM_SLP_S5# 37
SLP_S4# — H7 — PM_SLP_S4# — PM_SLP_S4# 37
SLP_S3# — P12 — PM_SLP_S3# — PM_SLP_S3# 36,37
SLP_M# — K8 — PM_SLP_ME# — PM_SLP_ME# 37
TP23 — N2 — PM_SLP_DSW# — 1 TP719 20MIL
PMSYNCH — BJ10 — H_PM_SYNC — H_PM_SYNC 3
SLP_LAN# — F6 — PM_SLP_LAN# — 1 TP720 20MIL

Ibexpeak-M
null

2009.0928
Add the Q7 as MOR request.

37,59 SUS_PWRGD — 2 — B — C — E — Q7 DTC144EUA — 3 — PCIE_WAKE# F
39,40,41 PCIE_WAKE#

+3VRUN
SB_RST# — R5878 1 8.2K_J 2 0201
PM_CLKRUN# — R5879 1 8.2K_J 2 0201

+3VALW
PCIE_WAKE# F — R5881 1 10K_J 2 0201
PM_RI# — R5882 1 10K_J 2 0201
PM_SLP_LAN# — R5883 1 NC_10K_J 2 0201
PM_BATLOW# — R5885 1 8.2K_J 2 0201
SUS_PWR_ACK — R5886 1 8.2K_J 2 0201
SB_RST# — R5888 1 NC_8.2K_J 2 0201
PM_RSMRST# — R5889 1 10K_J 2 0201
PWROK — R5890 1 10K_J 2 0201

2009/09/10 (DVT2)
Delete R5893, add R6007 to +3VALW
M9A0 use Ignition FW, no ACPRESENT function.
Intel FAE suggest this pin can configure it as GPIO.

+3VRUN — R5880 NC_10K_J 0402 — 2 — 1
+3VALW — R6007 1K_J 0402 — 2 — 1 — GPIO31
MPWROK_R — R5884 1 NC_0_J 2 0402 — LAN_RST#

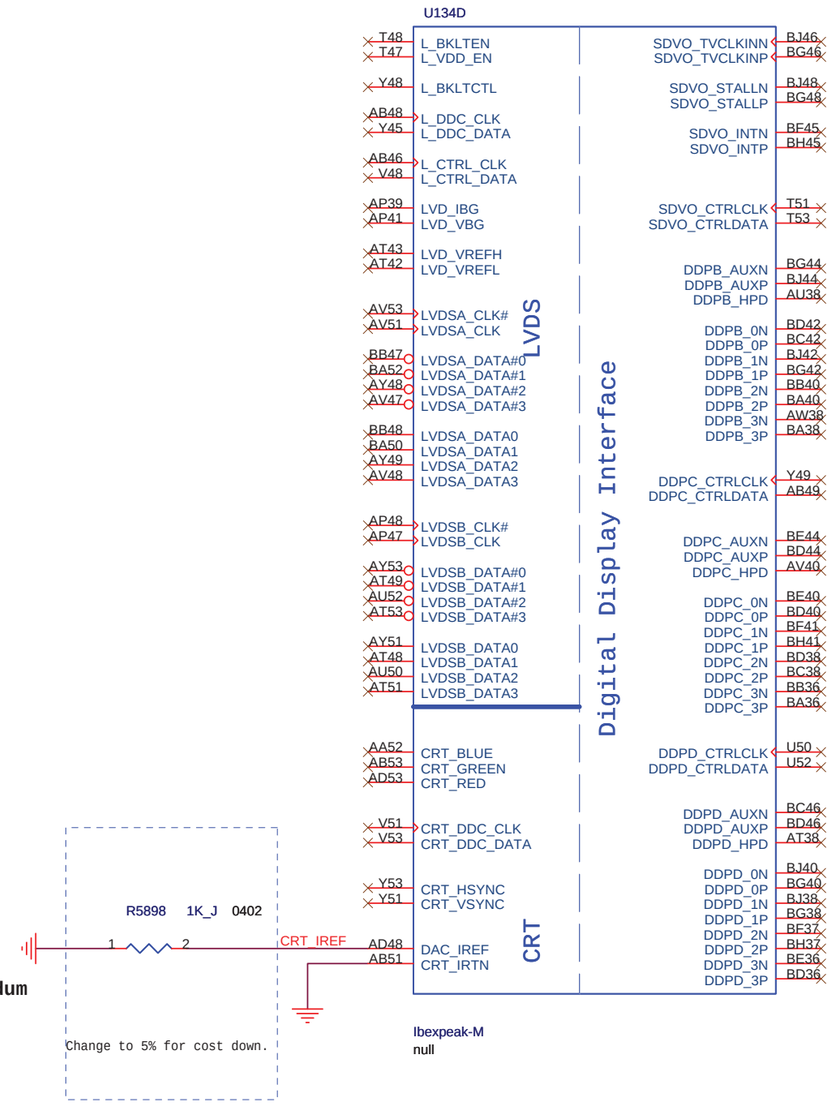
D33 — SYS_PWROK — 1 — 2 — NC_SD103AWS
D26 — PM_RSMRST# R — 1 — 2 — NC_SD103AWS — ALW_PWRGD 37,56
D27 — PWROK — 1 — 2 — NC_SD103AWS
NC for cost/No need to stuff

PM_SLP_ME# — 1 — TP721 20MIL

2009/09/10 (DVT2)
Delete R5887 and Net name AC_Present
M9A0 use Ignition FW, no ACPRESENT function.
Intel FAE suggest this pin can configure it as GPIO.

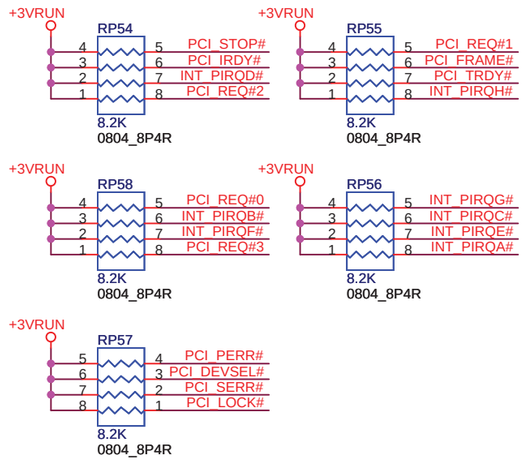
FOXCONN — HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

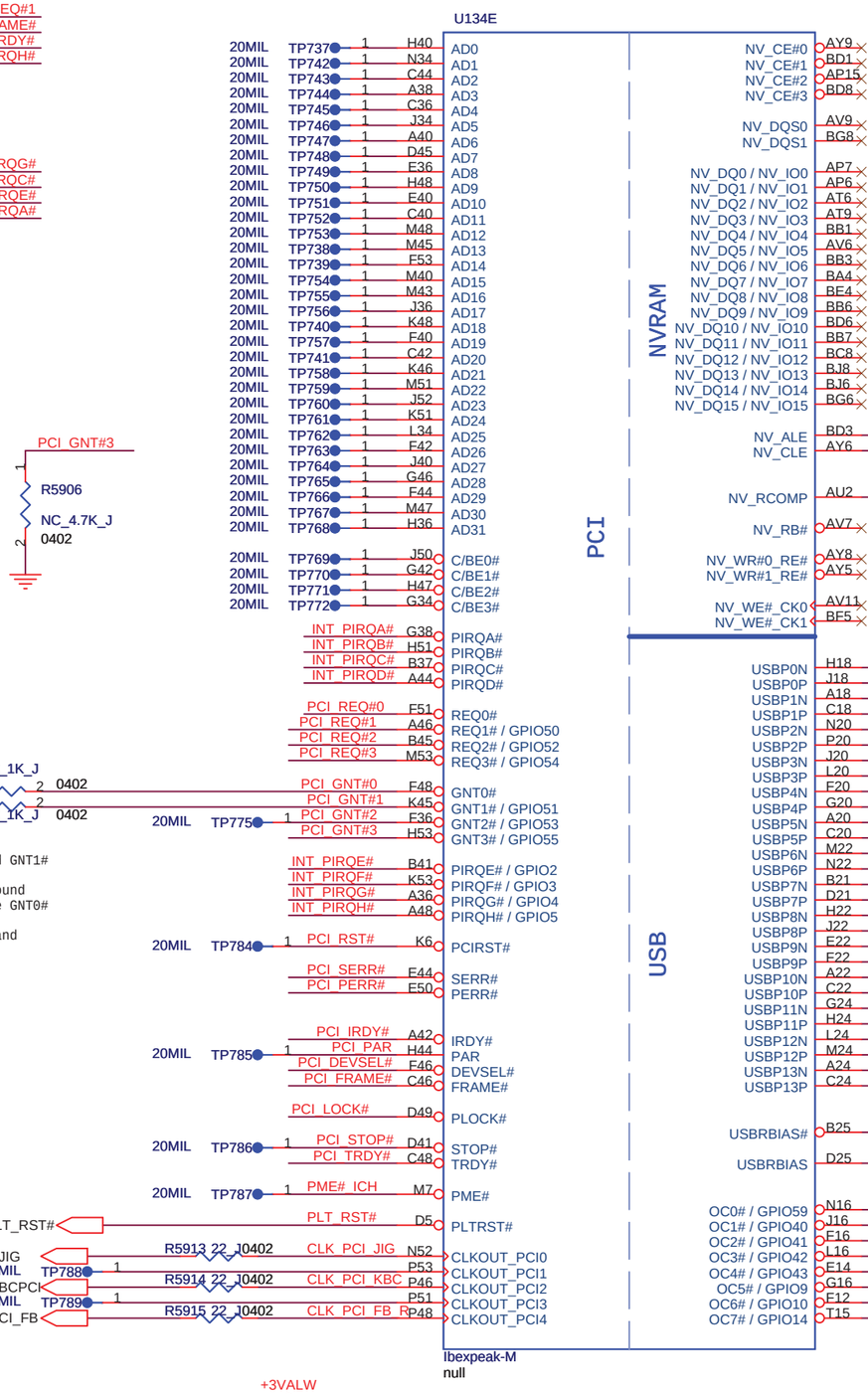
Title	PCH (DMI,FDI,GPIO)	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 11 of 73	



Calpella Platform – Design Guide - Addendum / Update – Rev. 1.52 (Doc #414044).).

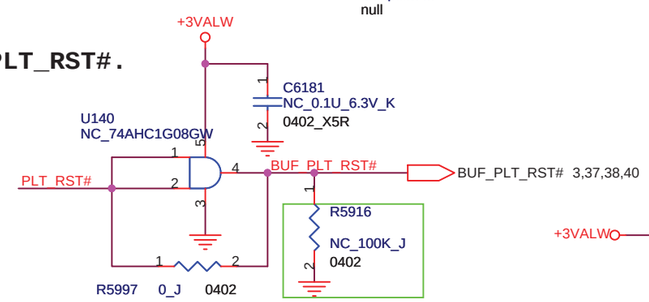
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	PCH (LVDS,DDI)		
Size: Custom	Document Number: M9A0_MP		Rev: 1.1
Date: Wednesday, September 23, 2009	Sheet 12 of 73		

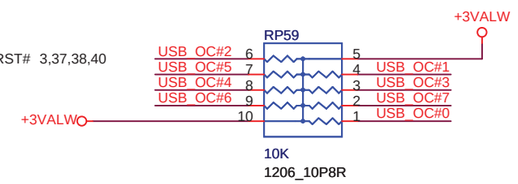




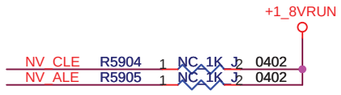
Default (SPI): Leave both GNT0# and GNT1# floating. No pull up required.
Boot from PCI: Connect GNT1# to ground with 1-k? pull-down resistor. Leave GNT0# Floating.
Boot from LPC: Connect both GNT0# and GNT1# to ground with 1K? pull-down resistor.

Buffer to reduce loading on PLT_RST#.





DMI Termination Voltage	
NV_CLE	Set to Vss when LOW Set to Vcc when HIGH



Intel Anti-Theft Technology
Disabled when Low , NC R1616
Enabled when High ,Stuff R1616

USB PORT	Function
PORT-0	External Port-0
PORT-1	External Port-1
PORT-2	
PORT-3	ExpressCard/34 (USB)
PORT-4	External Port-2
PORT-5	
PORT-6	
PORT-7	
PORT-8	
PORT-9	Camera
PORT-10	No finger print
PORT-11	
PORT-12	Wireless LAN (WiMAX)
PORT-13	Bluetooth

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	PCH (PCI,USB,NVRAM)	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 13 of 73	

+3VALW

R5917 1 1K_J 2 0402 GPIO15
R5918 1 10K_J 2 0402 GPIO28
R5919 1 10K_J 2 0402 GPIO12
RP96 10K 0404_4P2R
1 4 DRAMRST_CNTRL_PCH
2 3 GPIO45
RP97 10K 0404_4P2R
1 4 PCH_GPIO57
2 3 GPIO8

+3VRUN

R5995 1 10K_J 2 0201 FP_DET#
R5927 1 10K_J 2 0201 BMBUSY#
R5928 1 10K_J 2 0201 EXTSMI#
R5925 1 10K_J 2 0201 STP_PCI#
RP98 10K 0404_4P2R
1 4 H_RCIN#
2 3 GPIO39
R5926 1 NC_10K_J 2 0201 SATACLKREQ#
R5932 2 10K_J 1 0402 H_A20GATE

R5934 1 10K_J 2 0402 INV_EN
R5935 1 10K_J 2 0402 MB_FLASH0_EN
R5936 1 NC_10K_J 2 0402 GPIO27
R5937 1 NC_10K_J 2 0402 GPIO28
R5938 1 10K_J 2 0201 SATACLKREQ#

3 DRAMRST_CNTRL_PCH

RP60
ID_LPC_PCI# 6 5
DISPLAY_SEL 7 4
GPIO48 8 3
RUNTIME_SCI# D 9 2 CRIT_TEMP_REP#
+3VRUN 10 1
10K
1206_10P8R

+3VRUN

R6004 1 100K_J 2 0402 LCDID1
R6005 1 100K_J 2 0402 LCDID2
R6006 1 100K_J 2 0402 LCDID0

37 RUNTIME_SCI#
D28 SD103AWS

U134F

37 EXTSMI#	EXTSMI#	C38	TACH1 / GPIO1
38 ID_LPC_PCI#	ID_LPC_PCI#	D37	TACH2 / GPIO6
	RUNTIME_SCI# D	J32	TACH3 / GPIO7
	GPIO8	F10	GPIO8
	GPIO12	K9	LAN_PHY_PWR_CTRL / GPIO12
	GPIO15	T7	GPIO15
	DISPLAY_SEL	AA2	SATA4GP / GPIO16
	FP_DET#	F38	TACH0 / GPIO17
9 MB_FLASH0_EN	MB_FLASH0_EN	Y7	SCLOCK / GPIO22
35 INV_EN	INV_EN	H10	MEM_LED / GPIO24
	GPIO27	AB12	GPIO27
	GPIO28	V13	GPIO28
	STP_PCI#	M11	STP_PCI# / GPIO34
	SATACLKREQ#	V6	SATACLKREQ# / GPIO35
35 LCDID0	LCDID0	AB7	SATA2GP / GPIO36
35 LCDID1	LCDID1	AB13	SATA3GP / GPIO37
35 LCDID2	LCDID2	V3	SLOAD / GPIO38
	GPIO39	P3	SDATAOUT0 / GPIO39
	GPIO45	H3	PCIECLKRQ6# / GPIO45
3 DRAMRST_CNTRL_PCH		F1	PCIECLKRQ7# / GPIO46
	GPIO48	AB6	SDATAOUT1 / GPIO48
37 CRIT_TEMP_REP#	CRIT_TEMP_REP#	AA4	SATA5GP / GPIO49
	PCH_GPIO57	F8	GPIO57

MISC / GPIO / CPU

	CLKOUT_PCIE6N	AH45	TP791 20MIL
	CLKOUT_PCIE6P	AH46	TP792 20MIL
	CLKOUT_PCIE7N	AF48	TP793 20MIL
	CLKOUT_PCIE7P	AF47	TP790 20MIL
	A20GATE	U2 H_A20GATE	H_A20GATE 37
	CLKOUT_BCLK0_N / CLKOUT_PCIE8N	AM3 CLK_PCH_CPU_CLK# R	RP83 0404_4P2R NC_0 → CLK_PCH_CPU_CLK# 3
	CLKOUT_BCLK0_P / CLKOUT_PCIE8P	AM1 CLK_PCH_CPU_CLK R	→ CLK_PCH_CPU_CLK 3
	PECI	BG10 H_PECI	H_PECI 3
	RCIN#	T1 H_RCIN#	H_RCIN# 37
	PROCPWRGD	BE10 H_CPUPWRGD	H_CPUPWRGD 3
	THRMTRIP#	BD10	R5933 1 56_J 2 0402 → PM_THRMTRIP# 3,37

+1_05V_VTT → R5931 56_J 0402

	TP1	BA22	TP794 20MIL
	TP2	AW22	TP795 20MIL
	TP3	BB22	TP796 20MIL
	TP4	AY45	TP797 20MIL
	TP5	AY46	TP798 20MIL
	TP6	AV43	TP799 20MIL
	TP7	AV45	TP800 20MIL
	TP8	AF13	TP801 20MIL
	TP9	M18	TP802 20MIL
	TP10	N18	TP803 20MIL
	TP11	AJ24	TP804 20MIL
	TP12	AK41	TP805 20MIL
	TP13	AK42	TP806 20MIL
	TP14	M32	TP807 20MIL
	TP15	N32	TP808 20MIL
	TP16	M30	TP809 20MIL
	TP17	N30	TP810 20MIL
	TP18	H12	TP811 20MIL
	TP19	AA23	TP812 20MIL
	NC_1	AB45	TP813 20MIL
	NC_2	AB38	TP814 20MIL
	NC_3	AB42	TP815 20MIL
	NC_4	AB41	TP816 20MIL
	NC_5	T39	TP817 20MIL
	INIT3_3V#	P6	TP818 20MIL
	TP24	C10	TP819 20MIL

NCTF / RSVD

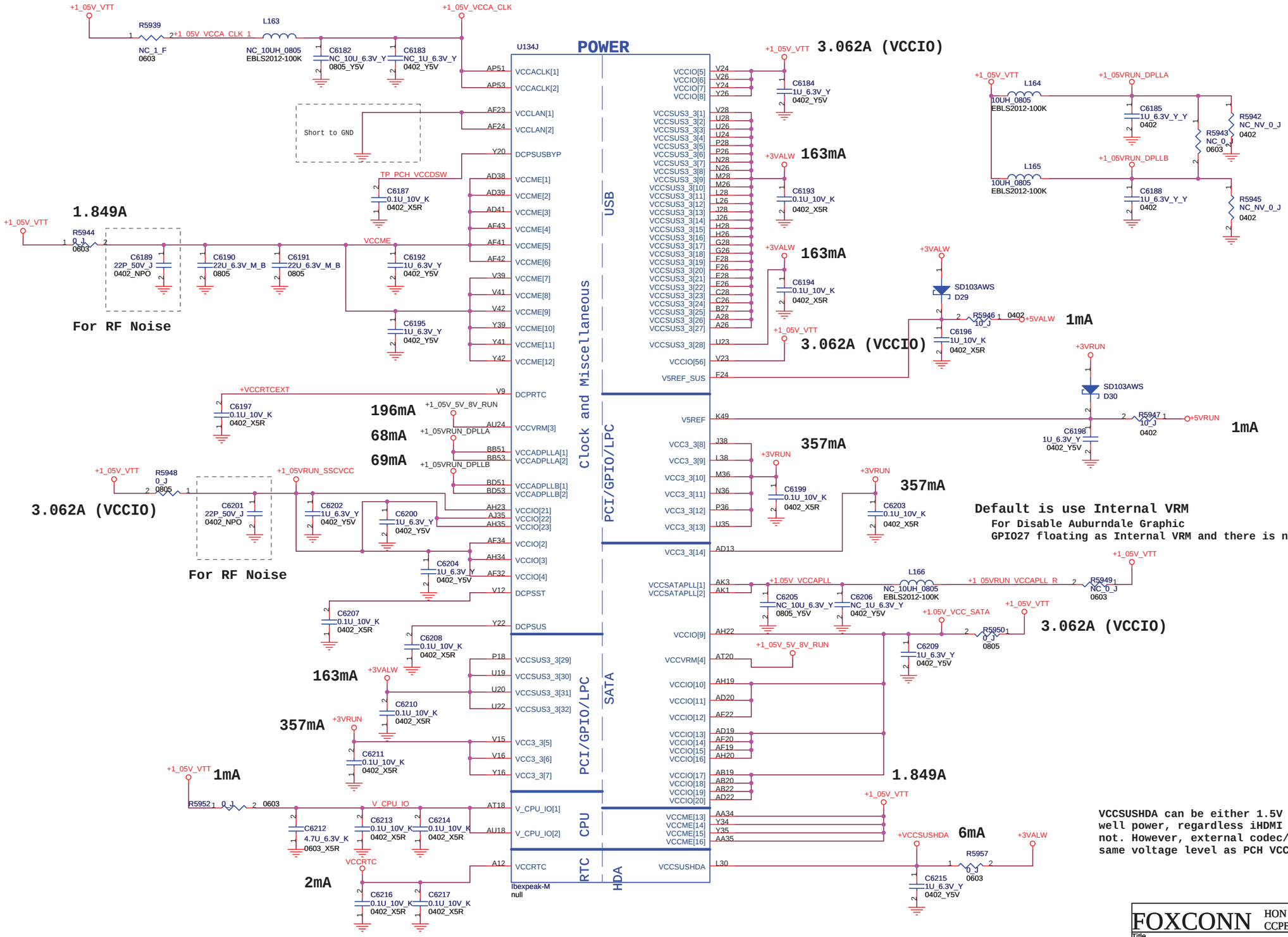
A4	VSS_NCTF_1
A49	VSS_NCTF_2
A5	VSS_NCTF_3
A50	VSS_NCTF_4
A52	VSS_NCTF_5
A53	VSS_NCTF_6
B2	VSS_NCTF_7
B4	VSS_NCTF_8
B52	VSS_NCTF_9
B53	VSS_NCTF_10
BE1	VSS_NCTF_11
BE53	VSS_NCTF_12
BF1	VSS_NCTF_13
BF53	VSS_NCTF_14
BH1	VSS_NCTF_15
BH2	VSS_NCTF_16
BH52	VSS_NCTF_17
BH53	VSS_NCTF_18
BJ1	VSS_NCTF_19
BJ2	VSS_NCTF_20
BJ4	VSS_NCTF_21
BJ49	VSS_NCTF_22
BJ5	VSS_NCTF_23
BJ50	VSS_NCTF_24
BJ52	VSS_NCTF_25
BJ53	VSS_NCTF_26
D1	VSS_NCTF_27
D2	VSS_NCTF_28
D53	VSS_NCTF_29
E1	VSS_NCTF_30
E53	VSS_NCTF_31

Ibexpeak-M
null

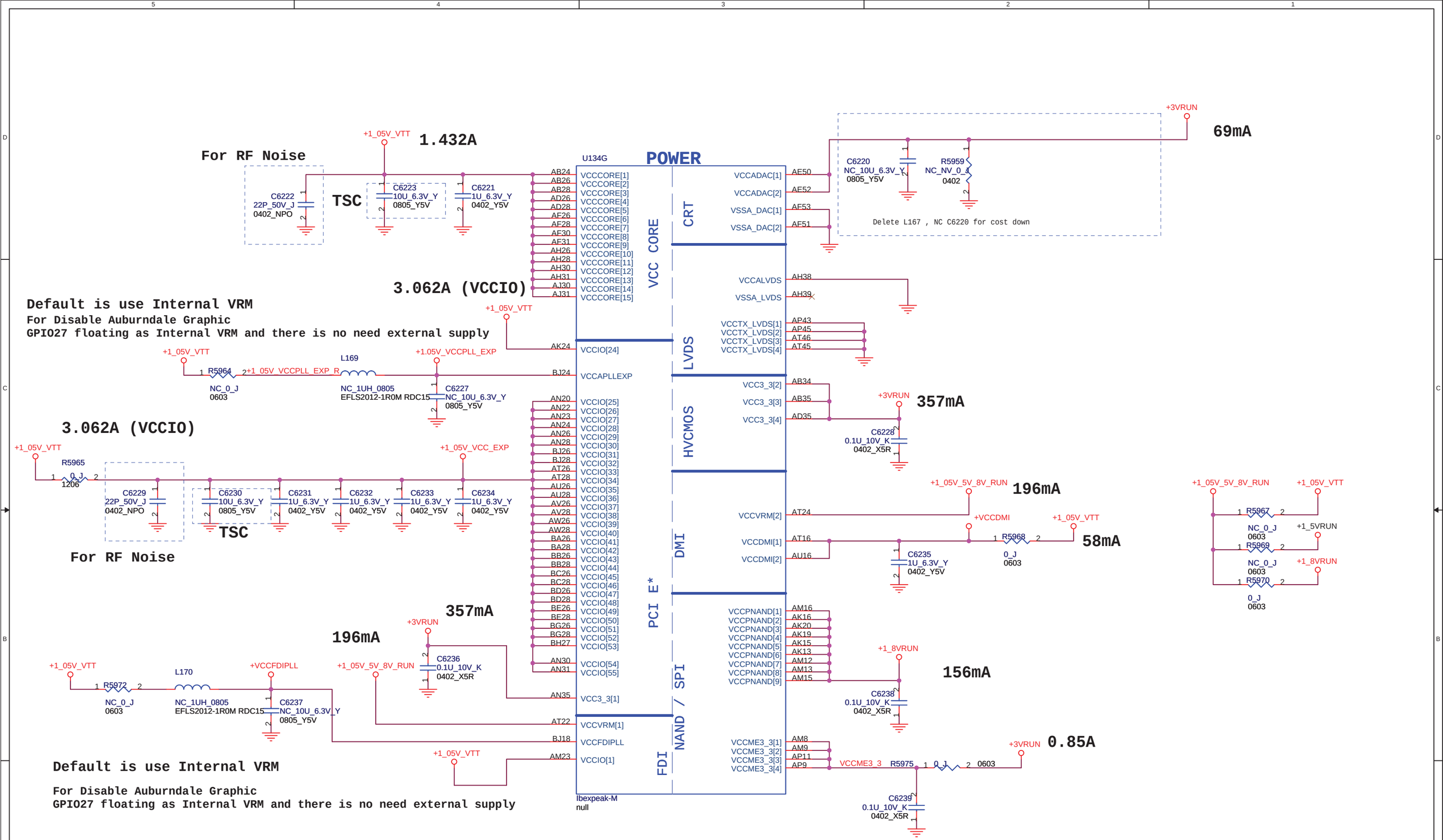
2009.10.31
Add RP83 NC_0 to escape crosstalk

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	PCH (GPIO,VSS_NCTF,RSVD)
Size A3	Document Number M9A0_MP
Rev	1.1
Date: Saturday, October 31, 2009	Sheet 14 of 73

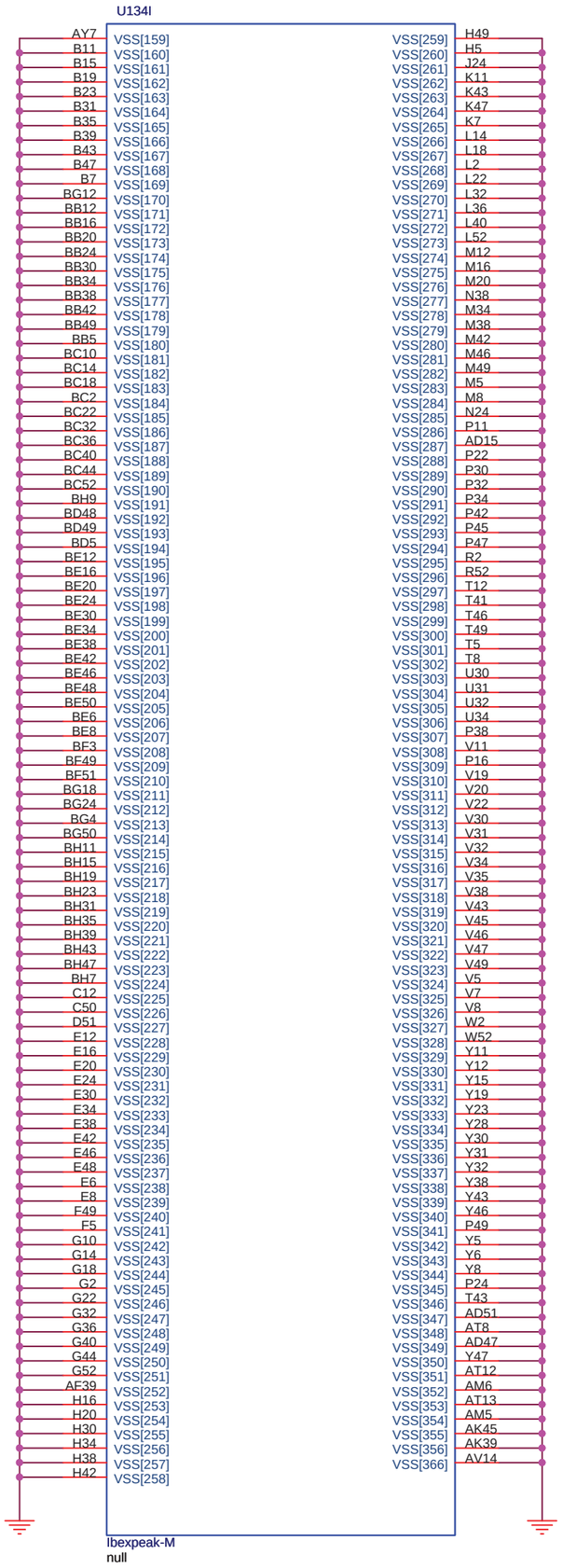
Default is use Internal VRM
For Disable Auburndale Graphic
GPIO27 floating as Internal VRM and there is no need external supply

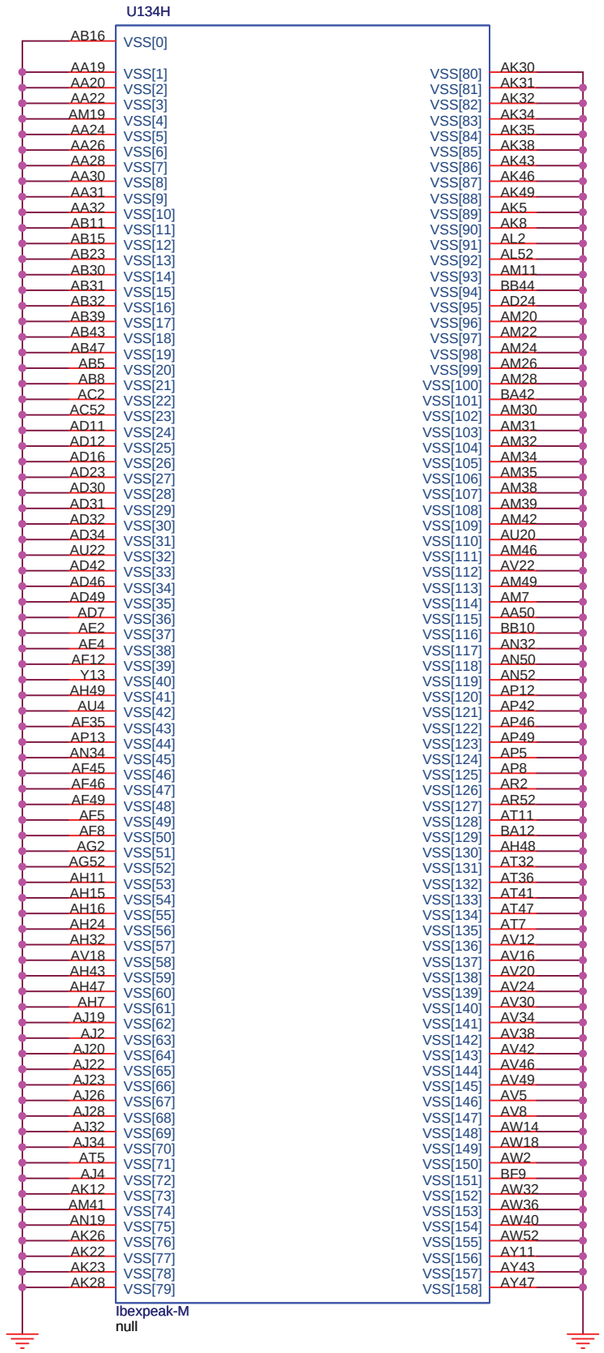


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	PCH (POWER) 1/2		
Size: Custom	Document Number: M9A0_MP		Rev: 1.1
Date: Friday, September 25, 2009	Sheet 15 of 73		



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (POWER) 2/2	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, September 23, 2009	Sheet 16 of 73	

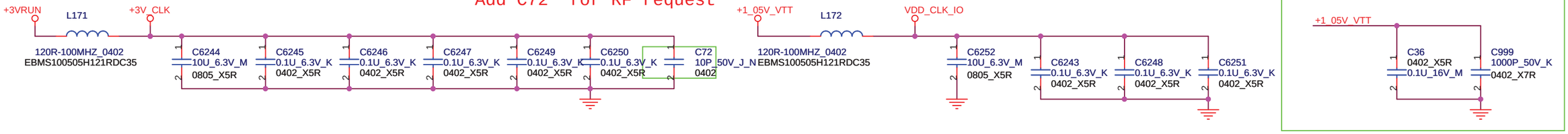


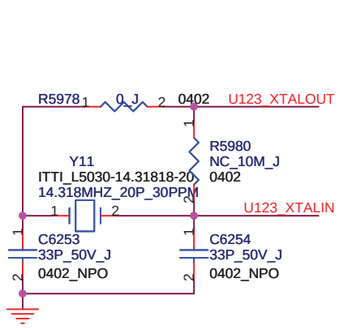


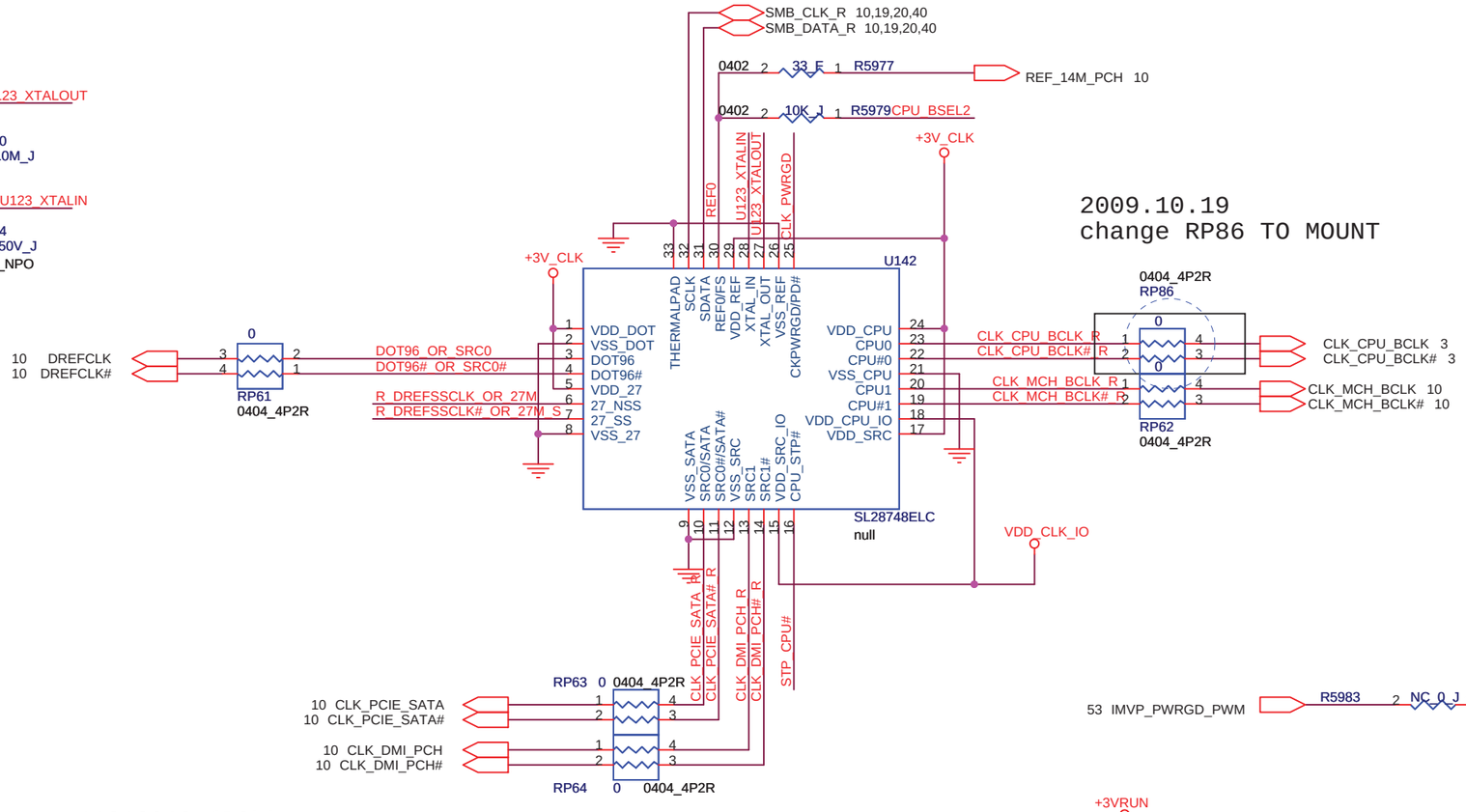
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (VSS)	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, September 23, 2009	Sheet 17 of 73	

2009.0925
ADD for EMI request

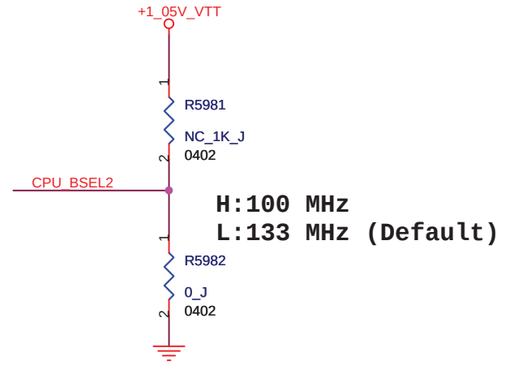
2009.0925
Add C72 for RF request

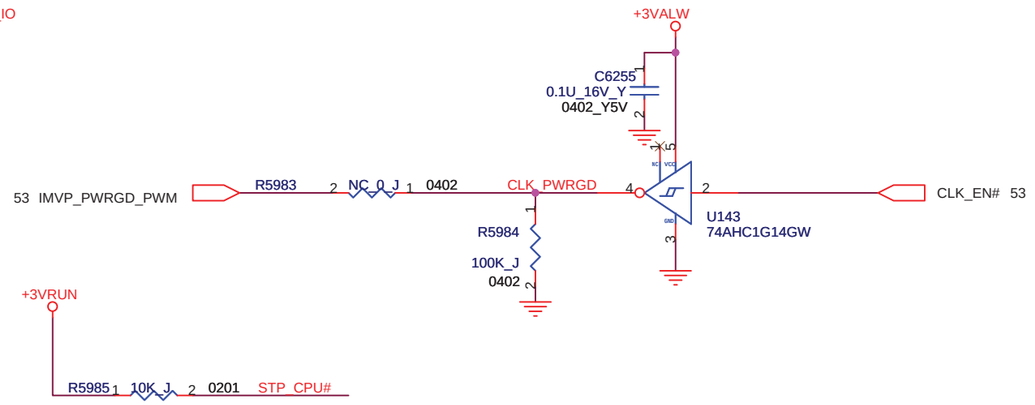






2009.10.19
change RP86 TO MOUNT



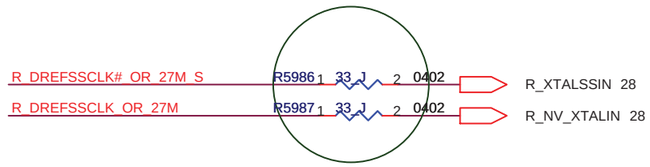


SMBUS Address: 11010010 (D2h)

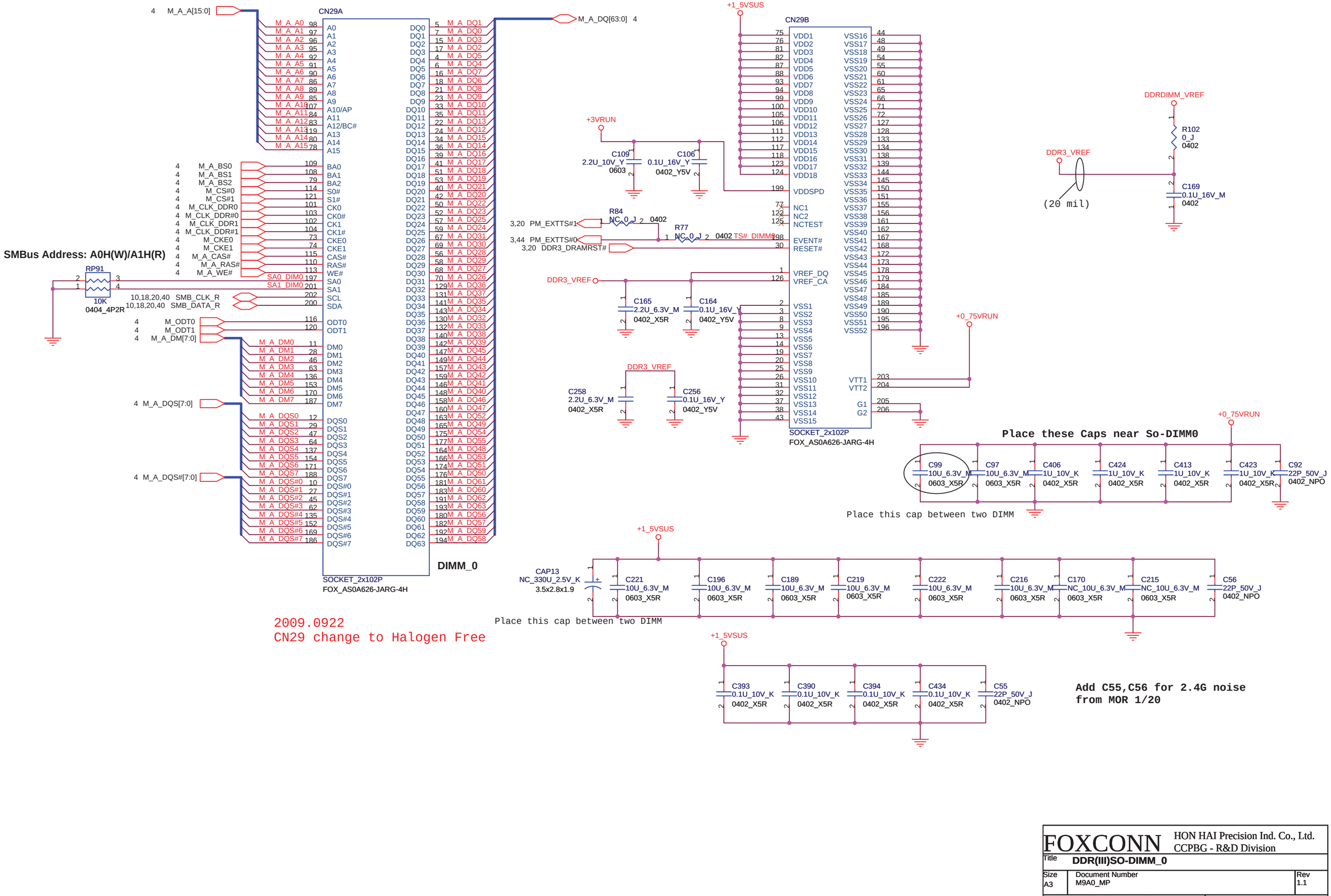
For N11M, SILEGO -SLG8SP585VTR (1F-GSLG8SP-5800)
For N11P, SLI -SL28748ELC (1F-GSL2874-8E00)
Check it by Model bit0

Frequency Select Pin (FS)

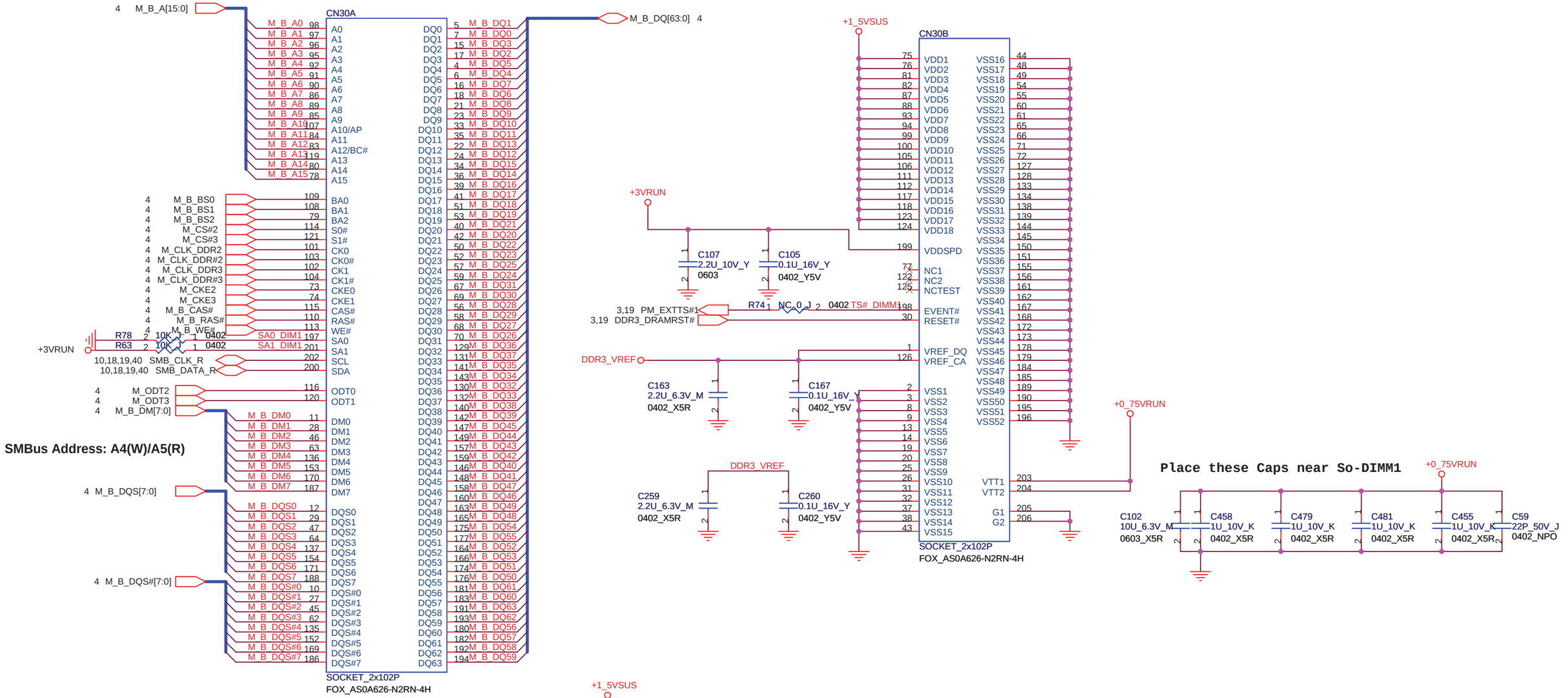
FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						



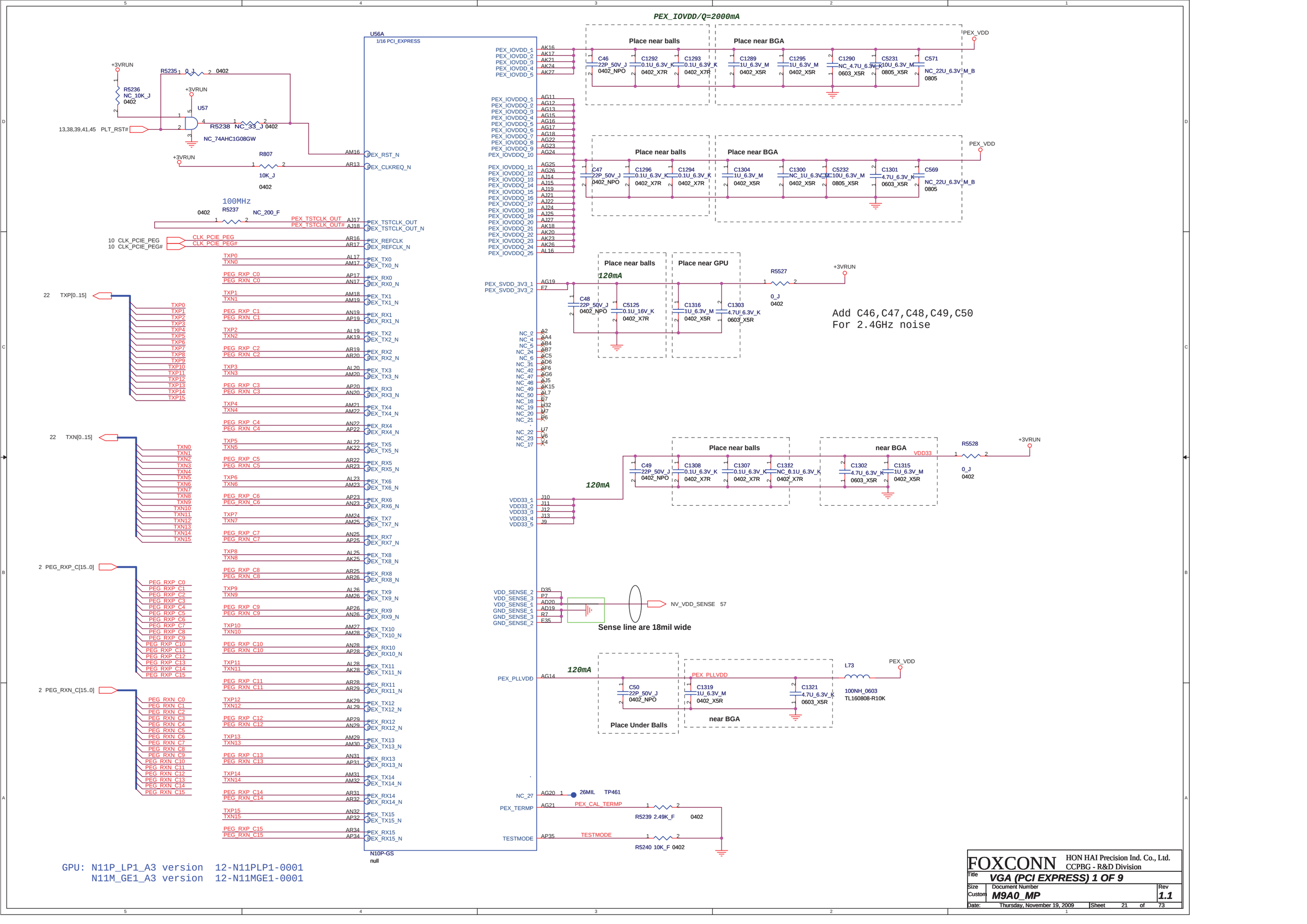
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: CLOCK GEN		
Size: A3	Document Number: M9A0_MP	Rev: 1.1
Date: Friday, October 23, 2009	Sheet 18 of 73	

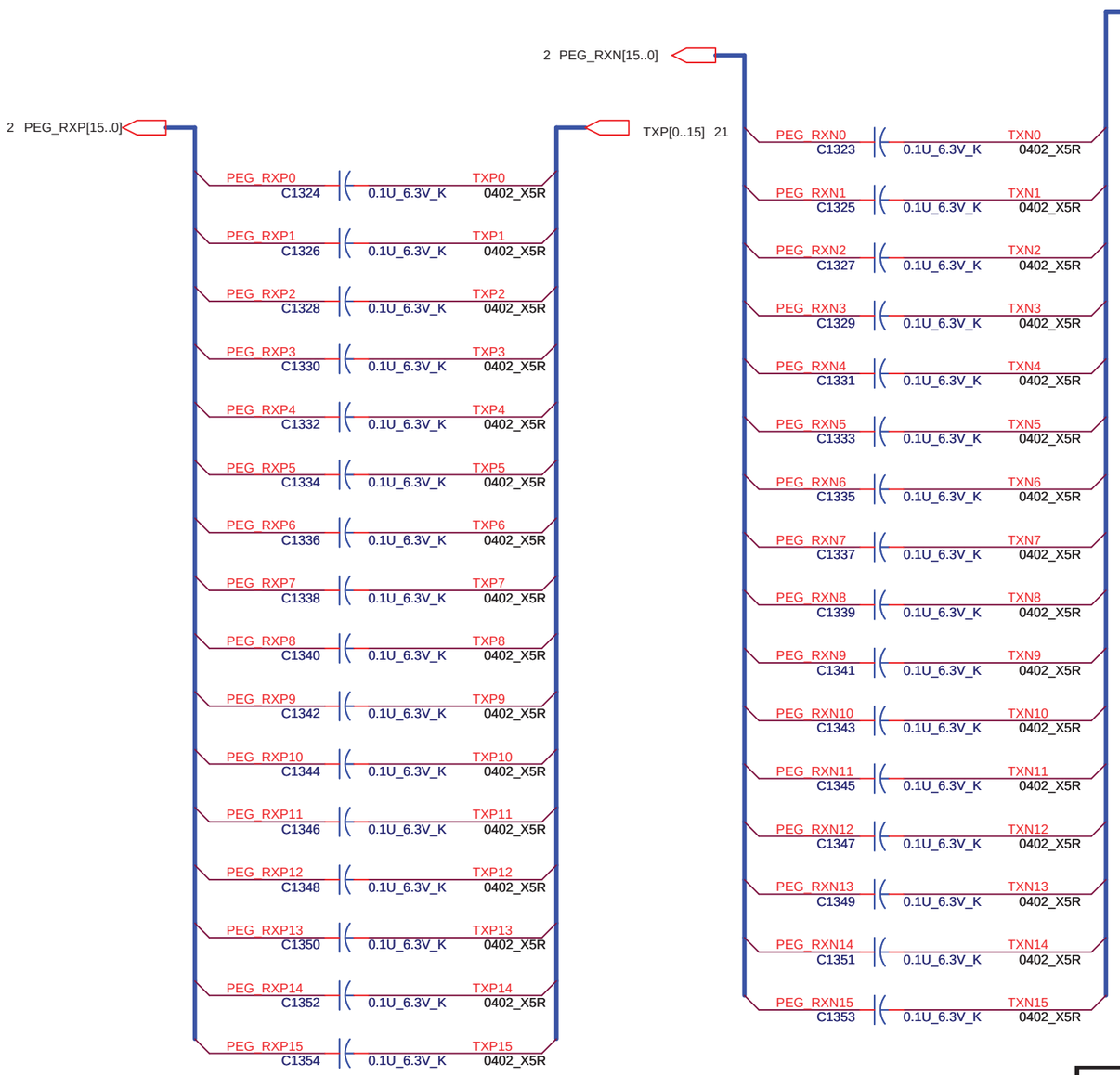


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	DDR(III)SO-DIMM_0
Size: A3	Document Number: M9A0_MP
Rev: 1.1	
Date: Thursday, November 19, 2009	Sheet 19 of 73



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDR(III)SO-DIMM_1	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Thursday, November 19, 2009	Sheet 20 of 73	


PEX_IOVDD/Q=2000mA
U56A
1/16 PCI_EXPRESS
Place near balls
Place near BGA
PEX_VDD
C46 22P_50V_J 0402_NPO
C1292 0.1U_6.3V_K 0402_X7R
C1293 0.1U_6.3V_K 0402_X7R
C1289 1U_6.3V_M 0402_X5R
C1295 1U_6.3V_M 0402_X5R
C1290 NC_4.7U_6.3V_K 0603_X5R
C5231 10U_6.3V_M 0805_X5R
C571 NC_22U_6.3V_M_B 0805
C47 22P_50V_J 0402_NPO
C1296 0.1U_6.3V_K 0402_X7R
C1294 0.1U_6.3V_K 0402_X7R
C1304 1U_6.3V_M 0402_X5R
C1300 NC_1U_6.3V_M 0402_X5R
C5232 10U_6.3V_M 0805_X5R
C1301 4.7U_6.3V_K 0603_X5R
C569 NC_22U_6.3V_M_B 0805
Place near balls
Place near GPU
120mA
R5527 0_J 0402
+3VRUN
C48 22P_50V_J 0402_NPO
C5125 0.1U_16V_K 0402_X7R
C1316 1U_6.3V_M 0402_X5R
C1303 4.7U_6.3V_K 0603_X5R
Add C46,C47,C48,C49,C50
For 2.4GHz noise
Place near balls
near BGA
VDD33
R5528 0_J 0402
C49 22P_50V_J 0402_NPO
C1308 0.1U_6.3V_K 0402_X7R
C1307 0.1U_6.3V_K 0402_X7R
C1312 NC_0.1U_6.3V_K 0402_X7R
C1302 4.7U_6.3V_K 0603_X5R
C1315 1U_6.3V_M 0402_X5R
120mA
Sense line are 18mil wide
NV_VDD_SENSE 57
Place Under Balls
near BGA
C50 22P_50V_J 0402_NPO
C1319 1U_6.3V_M 0402_X5R
C1321 4.7U_6.3V_K 0603_X5R
L73 100NH_0603 TL160808-R10K
PEX_PLLVDD
R5235 0_J 0402
R5236 NC_10K_J 0402
R5238 NC_33_J 0402
U57
NC_74AHC1G08GW
13,38,39,41,45 PLT_RST#
R807 10K_J 0402
100MHz
R5237 NC_200_F 0402
10 CLK_PCIE_PEG
10 CLK_PCIE_PEG#
22 TXP[0..15]
22 TXN[0..15]
2 PEG_RXP_C[15..0]
2 PEG_RXN_C[15..0]
PEX_RST_N
PEX_CLKREQ_N
PEX_TSTCLK_OUT
PEX_TSTCLK_OUT_N
PEX_REFCLK
PEX_REFCLK_N
PEX_TX0
PEX_TX0_N
PEX_RX0
PEX_RX0_N
PEX_TX1
PEX_TX1_N
PEX_RX1
PEX_RX1_N
PEX_TX2
PEX_TX2_N
PEX_RX2
PEX_RX2_N
PEX_TX3
PEX_TX3_N
PEX_RX3
PEX_RX3_N
PEX_TX4
PEX_TX4_N
PEX_RX4
PEX_RX4_N
PEX_TX5
PEX_TX5_N
PEX_RX5
PEX_RX5_N
PEX_TX6
PEX_TX6_N
PEX_RX6
PEX_RX6_N
PEX_TX7
PEX_TX7_N
PEX_RX7
PEX_RX7_N
PEX_TX8
PEX_TX8_N
PEX_RX8
PEX_RX8_N
PEX_TX9
PEX_TX9_N
PEX_RX9
PEX_RX9_N
PEX_TX10
PEX_TX10_N
PEX_RX10
PEX_RX10_N
PEX_TX11
PEX_TX11_N
PEX_RX11
PEX_RX11_N
PEX_TX12
PEX_TX12_N
PEX_RX12
PEX_RX12_N
PEX_TX13
PEX_TX13_N
PEX_RX13
PEX_RX13_N
PEX_TX14
PEX_TX14_N
PEX_RX14
PEX_RX14_N
PEX_TX15
PEX_TX15_N
PEX_RX15
PEX_RX15_N
N10P-GS
null
PEX_TERMP
PEX_CAL_TERMP
R5239 2.49K_F 0402
TESTMODE
R5240 10K_F 0402
26MIL TP461
GPU: N11P_LP1_A3 version 12-N11PLP1-0001
N11M_GE1_A3 version 12-N11MGE1-0001
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
VGA (PCI EXPRESS) 1 OF 9
M9A0_MP
1.1
Thursday, November 19, 2009
Sheet 21 of 73

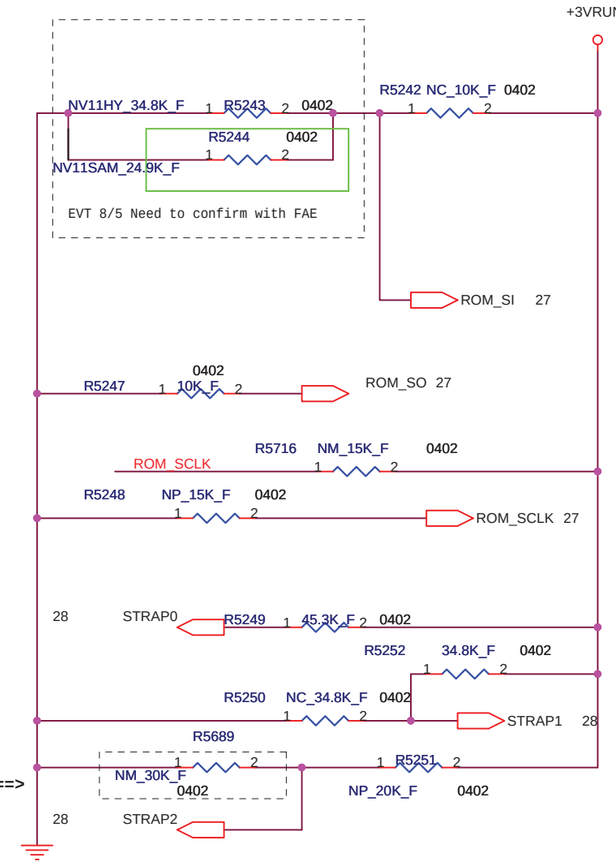


XCLK_417 0 (27M Hz) 1 (Reserved) FB_0_BAR_SIZE 0 256MB 1 (Reserved) SMB_ALT_ADDR 0 0x9E 1 0x9C(multi-GPU usage) VGA_DEVICE 0 3D device(class code 302h) 1 VGA device(class code 300h)	ROM_SO 0001
SUB_VENDOR 0 (No vedio BIOS ROM) 1 (BIOS ROM is present) SLOT_CLK_CFG 0 (GPU and MCH not share a common reference clk) 1 (GPU and MCH share a common reference clk) PEX_PLL_EN_TERM 0 (Disable) 1 (Enable)	ROM_SCLK N11P-LP1 0010 N11M-GE1 1010
USER[3:0] 1111	STRAP0 (1111)
N10x/N11x 3GIO_PADCFG[3:0] 1110	STRAP1 (1110)
N11X PCI_DEVID[3:0] N11P-LP1 1011b N11M-GE1 0101b PCI DEVICE IDs N11P-LP1 (0x0A2B) N11M-GE1 (0x0A75)	Strap2 N11P-LP1 1011 N11M-GE1 0101
0000 64-bit Reserved 1110 32Mx32 GDDR3 - 136 ball 64-bit Hynix - 35K pul Low. 0100 32Mx32 GDDR3 - 136 ball 64-bit Samsung- 25K pull Low ROM_SI	

8/3 [DVT] Revise the
Strap Pin value as FAE
provided for DVT Sample.

- N11M-GE1 x0A75
- N11P-LP1 0x0A2B

2009/9/10
N11P-LP1+SANSUNG(H2) SKU and
N11M-GE1 +SANSUANG(M2 SKU)need change BOM
R5244 change from 1R-0004532-F200(45.3K) to
1R-0002492-F200(24.9K) for nVIDIA FAE suggest



===>

Logical Strap bit Mapping

Resister values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

Strap Options

Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	+3VRUN	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

Refer to <GB1 Family Design Guide DG-04642-001_v01_secured>

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (PCI-EXPRESS/STRAP) 2 OF 9

Size: A3 | Document Number: M9A0_MP | Rev: 1.1

Date: Thursday, November 19, 2009 | Sheet 22 of 73

M9A0 FBVDDQ current N11P_LP1 is 6.5A . N11M_GE1 is 3.3A

U56B
2/16 FBA

30 FBAD[0:63]

FBAD0	L32	FBA_D00
FBAD1	N33	FBA_D01
FBAD2	L33	FBA_D02
FBAD3	N34	FBA_D03
FBAD4	N35	FBA_D04
FBAD5	P35	FBA_D05
FBAD6	P33	FBA_D06
FBAD7	P34	FBA_D07
FBAD8	K35	FBA_D08
FBAD9	K33	FBA_D09
FBAD10	K34	FBA_D10
FBAD11	H33	FBA_D11
FBAD12	G34	FBA_D12
FBAD13	G33	FBA_D13
FBAD14	E34	FBA_D14
FBAD15	E33	FBA_D15
FBAD16	G31	FBA_D16
FBAD17	F30	FBA_D17
FBAD18	G30	FBA_D18
FBAD19	G32	FBA_D19
FBAD20	K30	FBA_D20
FBAD21	K32	FBA_D21
FBAD22	H30	FBA_D22
FBAD23	K31	FBA_D23
FBAD24	L31	FBA_D24
FBAD25	L30	FBA_D25
FBAD26	M32	FBA_D26
FBAD27	N30	FBA_D27
FBAD28	M30	FBA_D28
FBAD29	P31	FBA_D29
FBAD30	R32	FBA_D30
FBAD31	R30	FBA_D31
FBAD32	AG30	FBA_D32
FBAD33	AG32	FBA_D33
FBAD34	AH31	FBA_D34
FBAD35	AF31	FBA_D35
FBAD36	AF30	FBA_D36
FBAD37	AE30	FBA_D37
FBAD38	AC32	FBA_D38
FBAD39	AD30	FBA_D39
FBAD40	AN33	FBA_D40
FBAD41	AL31	FBA_D41
FBAD42	AM33	FBA_D42
FBAD43	AL33	FBA_D43
FBAD44	AK30	FBA_D44
FBAD45	AK32	FBA_D45
FBAD46	AJ30	FBA_D46
FBAD47	AH30	FBA_D47
FBAD48	AH33	FBA_D48
FBAD49	AH35	FBA_D49
FBAD50	AH34	FBA_D50
FBAD51	AH32	FBA_D51
FBAD52	AJ33	FBA_D52
FBAD53	AL35	FBA_D53
FBAD54	AM34	FBA_D54
FBAD55	AM35	FBA_D55
FBAD56	AF33	FBA_D56
FBAD57	AE32	FBA_D57
FBAD58	AF34	FBA_D58
FBAD59	AE35	FBA_D59
FBAD60	AE34	FBA_D60
FBAD61	AE33	FBA_D61
FBAD62	AB32	FBA_D62
FBAD63	AC35	FBA_D63

30 FBADQM[7..0]

FBADQM0	P32	FBA_DQM0
FBADQM1	H34	FBA_DQM1
FBADQM2	J30	FBA_DQM2
FBADQM3	P30	FBA_DQM3
FBADQM4	AF32	FBA_DQM4
FBADQM5	AL32	FBA_DQM5
FBADQM6	AL34	FBA_DQM6
FBADQM7	AE35	FBA_DQM7

30 FBAWDQS[7..0]

FBAWDQS0	L34	FBA_DQS_WP0
FBAWDQS1	H35	FBA_DQS_WP1
FBAWDQS2	J32	FBA_DQS_WP2
FBAWDQS3	N31	FBA_DQS_WP3
FBAWDQS4	AE31	FBA_DQS_WP4
FBAWDQS5	AJ32	FBA_DQS_WP5
FBAWDQS6	AJ34	FBA_DQS_WP6
FBAWDQS7	AC33	FBA_DQS_WP7

30 FBARDQS[7..0]

FBARDQS0	L35	FBA_DQS_RN0
FBARDQS1	G35	FBA_DQS_RN1
FBARDQS2	H31	FBA_DQS_RN2
FBARDQS3	N32	FBA_DQS_RN3
FBARDQS4	AD32	FBA_DQS_RN4
FBARDQS5	AJ31	FBA_DQS_RN5
FBARDQS6	AJ35	FBA_DQS_RN6
FBARDQS7	AC34	FBA_DQS_RN7

P29	NC_45
R29	NC_46
L29	NC_43
M29	NC_44
AG29	NC_28
AH29	NC_29
AD29	NC_25
AE29	NC_26

TP492 26MIL 1 J27 FB_VREF

N10P-GS
null

FBVDDQ_25	J23
FBVDDQ_26	J24
FBVDDQ_27	J29
FBVDDQ_1	AA27
FBVDDQ_2	AA29
FBVDDQ_3	AA31
FBVDDQ_4	AB27
FBVDDQ_5	AB29
FBVDDQ_6	AC27
FBVDDQ_7	AD27
FBVDDQ_8	AE27
FBVDDQ_9	AJ28
FBVDDQ_10	B18
FBVDDQ_11	E21
FBVDDQ_12	G17
FBVDDQ_13	G18
FBVDDQ_14	G22
FBVDDQ_15	G8
FBVDDQ_16	G9
FBVDDQ_17	H29
FBVDDQ_18	J14
FBVDDQ_19	J15
FBVDDQ_20	J16
FBVDDQ_21	J17
FBVDDQ_22	J20
FBVDDQ_23	J21
FBVDDQ_24	J22

Place near BGA

C35 10P_50V_J 0402_NPO
C874 NC_0.1U_6.3V_K 0402_X7R
C875 0.1U_6.3V_K 0402_X7R
C876 NP_0.1U_6.3V_K 0402_X7R
C877 0.047U_10V_K 0402_X7R
C880 0.047U_10V_K 0402_X7R

08/12/26 Add C33 follow RF propose.

C6018 NP_0.047U_10V_K 0402_X7R
C6014 0.01U_10V_K 0402_X7R
C6015 0.01U_10V_K 0402_X7R
C6016 NP_0.01U_10V_K 0402_X7R
C6017 NP_0.01U_10V_K 0402_X7R

+1_8VRUN

Place near the chip

C2 22P_50V_J 0402_NPO
C6020 4.7U_6.3V_K 0603_X5R
C6019 NP_4.7U_6.3V_K 0603_X5R

08/12/25 Add C2(22P) against 2.4GHz noise.

C876,C6018,C6016,C6017,C6019 only for N11P

FBA_CMD0	V32	FBA_A4	
FBA_CMD1	W31	FBA_RAS#	FBA_RAS# 30
FBA_CMD2	U31	FBA_A5	
FBA_CMD3	Y32	FBA_BA1	FBA_BA1 30
FBA_CMD4	AB35	FBB_A2	
FBA_CMD5	AB34	FBB_A4	
FBA_CMD6	W35	FBB_A3	
FBA_CMD7	W33		FBB_CKE 30
FBA_CMD8	W30		FBB_CS0# 30
FBA_CMD9	T34	FBA_A11	
FBA_CMD10	T35	FBA_CAS#	FBA_CAS# 30
FBA_CMD11	AB31	FBA_WE#	FBA_WE# 30
FBA_CMD12	Y30	FBA_BA0	FBA_BA0 30
FBA_CMD13	Y34	FBB_A5	
FBA_CMD14	W32	FBA_A12	
FBA_CMD15	AA30	FBA_RESET	FBA_RESET 30
FBA_CMD16	AA32	FBA_A7	
FBA_CMD17	Y33	FBA_A10	
FBA_CMD18	U32	FBA_CKE	FBA_CKE 30
FBA_CMD19	Y31	FBA_A0	
FBA_CMD20	U34	FBA_A9	
FBA_CMD21	Y35	FBA_A6	
FBA_CMD22	W34	FBA_A2	
FBA_CMD23	V30	FBA_A8	
FBA_CMD24	U35	FBA_A3	
FBA_CMD25	U30	FBA_A1	
FBA_CMD26	U33	FBA_A13	1 26MIL TP419
FBA_CMD27	AB30	FBA_BA2	FBA_BA2 30
FBA_CMD28	AB33	FBA_RFU0	1 26MIL TP420
FBA_CMD29	T33	FBA_CS0#	FBA_CS0# 30
FBA_CMD30	W29	FBA_CMD30	1 26MIL TP463

FBA_CLK0	T32	FBA_CLK0	FBA_CLK0 30
FBA_CLK0_N	T31	FBA_CLK0#	FBA_CLK0# 30
FBA_CLK1	AC31	FBA_CLK1	FBA_CLK1 30
FBA_CLK1_N	AC30	FBA_CLK1#	FBA_CLK1# 30

FBA_DEBUG T30 FBB_CAS# FBB_CAS# 30

FB_DLLAVDD0 AG27
FB_DLLAVDD0 AF27

200mA

C6042 22P_50V_J 0402_NPO
C1371 1U_6.3V_M 0402_X5R
C5162 4.7U_6.3V_K 0603_X5R

FB_PLLAVDD

L74 300R-100MHZ_0603 TB160808U301N001

PEX_VDD

Near GPU

FBA_A[0..12] 30

FBA_A4
FBA_A5
FBA_A11
FBA_A12
FBA_A7
FBA_A10
FBA_A0
FBA_A9
FBA_A6
FBA_A2
FBA_A8
FBA_A3
FBA_A1

FBB_A[2..5] 30

FBB_A2
FBB_A4
FBB_A3
FBB_A5

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Title	VGA(GDDR)# 3/9		
Size Custom	Document Number M9A0_MP		Rev 1.1
Date: Thursday, November 19, 2009	Sheet 23 of 73		

M9A0 FBVDDQ current N11P_LP1 is 6.5A N11M_GE1 is 3.3A

Place near BGA

+1_8VRUN

C40 10P_50V_J 0402_NPO
C883 0.1U_6.3V_K 0402_X7R
C882 0.1U_6.3V_K 0402_X7R
C879 NP_0.1U_6.3V_K 0402_X7R
C6007 0.047U_10V_K 0402_X7R
C884 0.047U_10V_K 0402_X7R
C13 22P_50V_J 0402_NPO
C6013 4.7U_6.3V_K 0603_X5R
C6012 NP_4.7U_6.3V_K 0603_X5R

Place near the chip

08/12/26 Add C40 follow RF propose.

C6006 NP_0.047U_10V_K 0402_X7R
C6008 0.01U_10V_K 0402_X7R
C6009 0.01U_10V_K 0402_X7R
C6010 NP_0.01U_10V_K 0402_X7R
C6011 NP_0.01U_10V_K 0402_X7R

31 FBCD[0:63]

U56C
3/16 FBC

FBCD0 B13 FBC_D00
FBCD1 D13 FBC_D01
FBCD2 A13 FBC_D02
FBCD3 A14 FBC_D03
FBCD4 C16 FBC_D04
FBCD5 B16 FBC_D05
FBCD6 A17 FBC_D06
FBCD7 D16 FBC_D07
FBCD8 C13 FBC_D08
FBCD9 B11 FBC_D09
FBCD10 C11 FBC_D10
FBCD11 A11 FBC_D11
FBCD12 C10 FBC_D12
FBCD13 C8 FBC_D13
FBCD14 B8 FBC_D14
FBCD15 A8 FBC_D15
FBCD16 F8 FBC_D16
FBCD17 F8 FBC_D17
FBCD18 F10 FBC_D18
FBCD19 F9 FBC_D19
FBCD20 F12 FBC_D20
FBCD21 D8 FBC_D21
FBCD22 D11 FBC_D22
FBCD23 E11 FBC_D23
FBCD24 D12 FBC_D24
FBCD25 E13 FBC_D25
FBCD26 E13 FBC_D26
FBCD27 F14 FBC_D27
FBCD28 E15 FBC_D28
FBCD29 E16 FBC_D29
FBCD30 F16 FBC_D30
FBCD31 F17 FBC_D31
FBCD32 D29 FBC_D32
FBCD33 F27 FBC_D33
FBCD34 F28 FBC_D34
FBCD35 E28 FBC_D35
FBCD36 D26 FBC_D36
FBCD37 E25 FBC_D37
FBCD38 D24 FBC_D38
FBCD39 E25 FBC_D39
FBCD40 E32 FBC_D40
FBCD41 F32 FBC_D41
FBCD42 D33 FBC_D42
FBCD43 E31 FBC_D43
FBCD44 C33 FBC_D44
FBCD45 F29 FBC_D45
FBCD46 D30 FBC_D46
FBCD47 E29 FBC_D47
FBCD48 B29 FBC_D48
FBCD49 C31 FBC_D49
FBCD50 C29 FBC_D50
FBCD51 B31 FBC_D51
FBCD52 C32 FBC_D52
FBCD53 B32 FBC_D53
FBCD54 B35 FBC_D54
FBCD55 B34 FBC_D55
FBCD56 A29 FBC_D56
FBCD57 B28 FBC_D57
FBCD58 A28 FBC_D58
FBCD59 C28 FBC_D59
FBCD60 C26 FBC_D60
FBCD61 D25 FBC_D61
FBCD62 B25 FBC_D62
FBCD63 A25 FBC_D63

31 FBCDQM[7..0]

FBCDQM0 A16 FBC_DQM0
FBCDQM1 D10 FBC_DQM1
FBCDQM2 E11 FBC_DQM2
FBCDQM3 D15 FBC_DQM3
FBCDQM4 D27 FBC_DQM4
FBCDQM5 D34 FBC_DQM5
FBCDQM6 A34 FBC_DQM6
FBCDQM7 D28 FBC_DQM7

31 FBCWDQS[7..0]

FBCWDQS0 C14 FBC_DQS_WP0
FBCWDQS1 A10 FBC_DQS_WP1
FBCWDQS2 E10 FBC_DQS_WP2
FBCWDQS3 D14 FBC_DQS_WP3
FBCWDQS4 E26 FBC_DQS_WP4
FBCWDQS5 D32 FBC_DQS_WP5
FBCWDQS6 A32 FBC_DQS_WP6
FBCWDQS7 B26 FBC_DQS_WP7

31 FBCRDQS[7..0]

FBCRDQS0 B14 FBC_DQS_RN0
FBCRDQS1 B10 FBC_DQS_RN1
FBCRDQS2 D9 FBC_DQS_RN2
FBCRDQS3 E14 FBC_DQS_RN3
FBCRDQS4 F26 FBC_DQS_RN4
FBCRDQS5 D31 FBC_DQS_RN5
FBCRDQS6 A31 FBC_DQS_RN6
FBCRDQS7 A26 FBC_DQS_RN7

G14 NC_34
G15 NC_35
G11 NC_32
G12 NC_33
G27 NC_38
G28 NC_39
G24 NC_36
G25 NC_37

FBVDDQ_28 N27
FBVDDQ_29 P27
FBVDDQ_30 R27
FBVDDQ_31 T27
FBVDDQ_32 U27
FBVDDQ_33 U29
FBVDDQ_34 V27
FBVDDQ_35 V29
FBVDDQ_36 V34
FBVDDQ_37 W27
FBVDDQ_38 Y27

FBC_CMD0 C17 FBC_A4
FBC_CMD1 B19 FBC_RAS# → FBC_RAS# 31
FBC_CMD2 D18 FBC_A5
FBC_CMD3 F21 FBC_BA1 → FBC_BA1 31
FBC_CMD4 A23 FBD_A2
FBC_CMD5 D21 FBD_A4
FBC_CMD6 B23 FBD_A3
FBC_CMD7 E20 → FBD_CKE 31
FBC_CMD8 G21 → FBD_CS0# 31
FBC_CMD9 F20 FBC_A11
FBC_CMD10 F19 FBC_CAS# → FBC_CAS# 31
FBC_CMD11 F23 FBC_WE# → FBC_WE# 31
FBC_CMD12 A22 FBC_BA0 → FBC_BA0 31
FBC_CMD13 C22 FBD_A5
FBC_CMD14 B17 FBC_A12
FBC_CMD15 F24 FBC_RESET → FBC_RESET 31
FBC_CMD16 C25 FBC_A7
FBC_CMD17 F22 FBC_A10
FBC_CMD18 C20 FBC_CKE → FBC_CKE 31
FBC_CMD19 B22 FBC_A0
FBC_CMD20 A19 FBC_A9
FBC_CMD21 D22 FBC_A6
FBC_CMD22 D20 FBC_A2
FBC_CMD23 E19 FBC_A8
FBC_CMD24 D19 FBC_A3
FBC_CMD25 F18 FBC_A1
FBC_CMD26 C19 FBC_A13 — 1 — 26MIL TP423
FBC_CMD27 E22 FBC_BA2 → FBC_BA2 31
FBC_CMD28 C23 FBC_RFU0 — 1 — 26MIL TP424
FBC_CMD29 B20 FBC_CS0# → FBC_CS0# 31
FBC_CMD30 A20 — 1 — 26MIL TP465

FBC_CLK0 E17 FBC_CLK0 → FBC_CLK0 31
FBC_CLK0_N D17 FBC_CLK0# → FBC_CLK0# 31
FBC_CLK1 D23 FBC_CLK1 → FBC_CLK1 31
FBC_CLK1_N E23 FBC_CLK1# → FBC_CLK1# 31

FBC_DEBUG G19 FBD_CAS# → FBD_CAS# 31

NC_16 J19 — 1 — 26MIL TP462
NC_15 J18 — 1 — 26MIL TP464

R5256 56.2_F 0402 +1_8VRUN
FB_CAL_PD_VDDQ K27 FB_CAL_PD_VDDQ
FB_CAL_PU_GND L27 FB_CAL_PU_GND
R5257 26.7_F 0402
FB_CAL_TERM_GND M27 FB_CAL_TERMGND
R5258 40.2_F 0402

N10P-GS
null

FBC_A[0..12] 31

FBC_A4
FBC_A5
FBC_A11
FBC_A12
FBC_A7
FBC_A10
FBC_A0
FBC_A9
FBC_A6
FBC_A2
FBC_A8
FBC_A3
FBC_A1

FBD_A[2..5] 31

FBD_A2
FBD_A4
FBD_A3
FBD_A5

Place components close to the GPU

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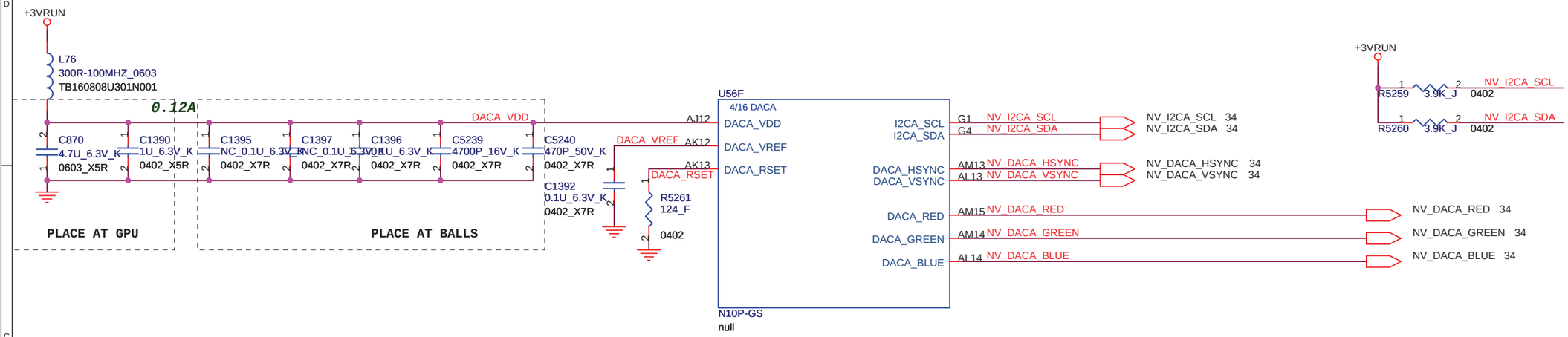
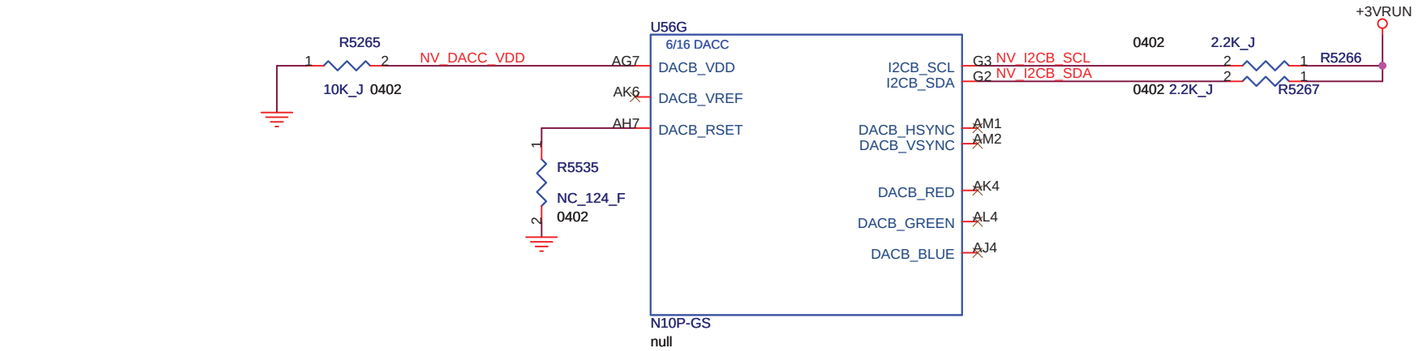
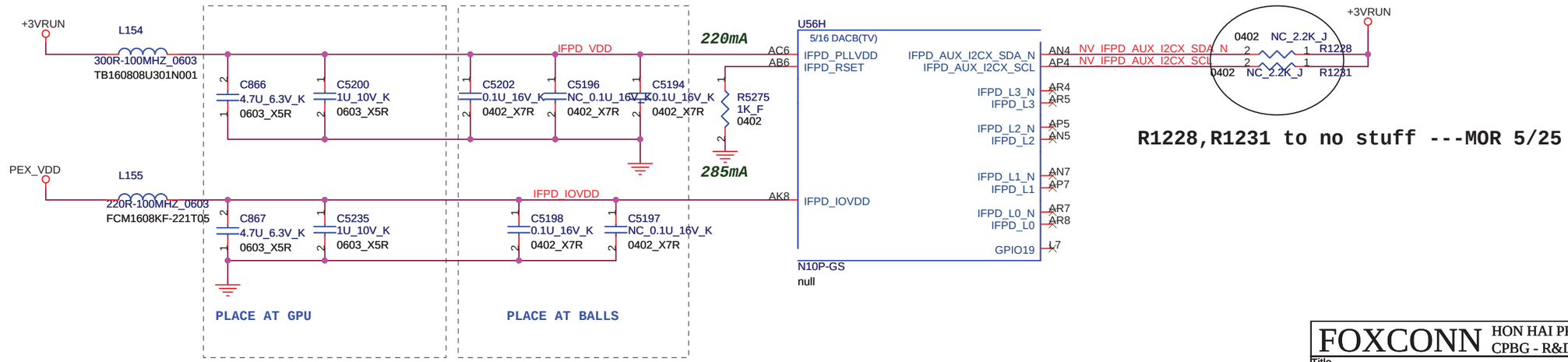
Title: VGA(GDDR)# 4/9
Size: Custom
Document Number: M9A0_MP
Rev: 1.1
Date: Thursday, November 19, 2009
Sheet 24 of 73





DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DDCCLK	SCL
	VGA-DDCDATA	SDA



R1228,R1231 to no stuff ---MOR 5/25

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Title: VGA (CRT)5/9

Size	Document Number	Rev
A3	M9A0_MP	1.1

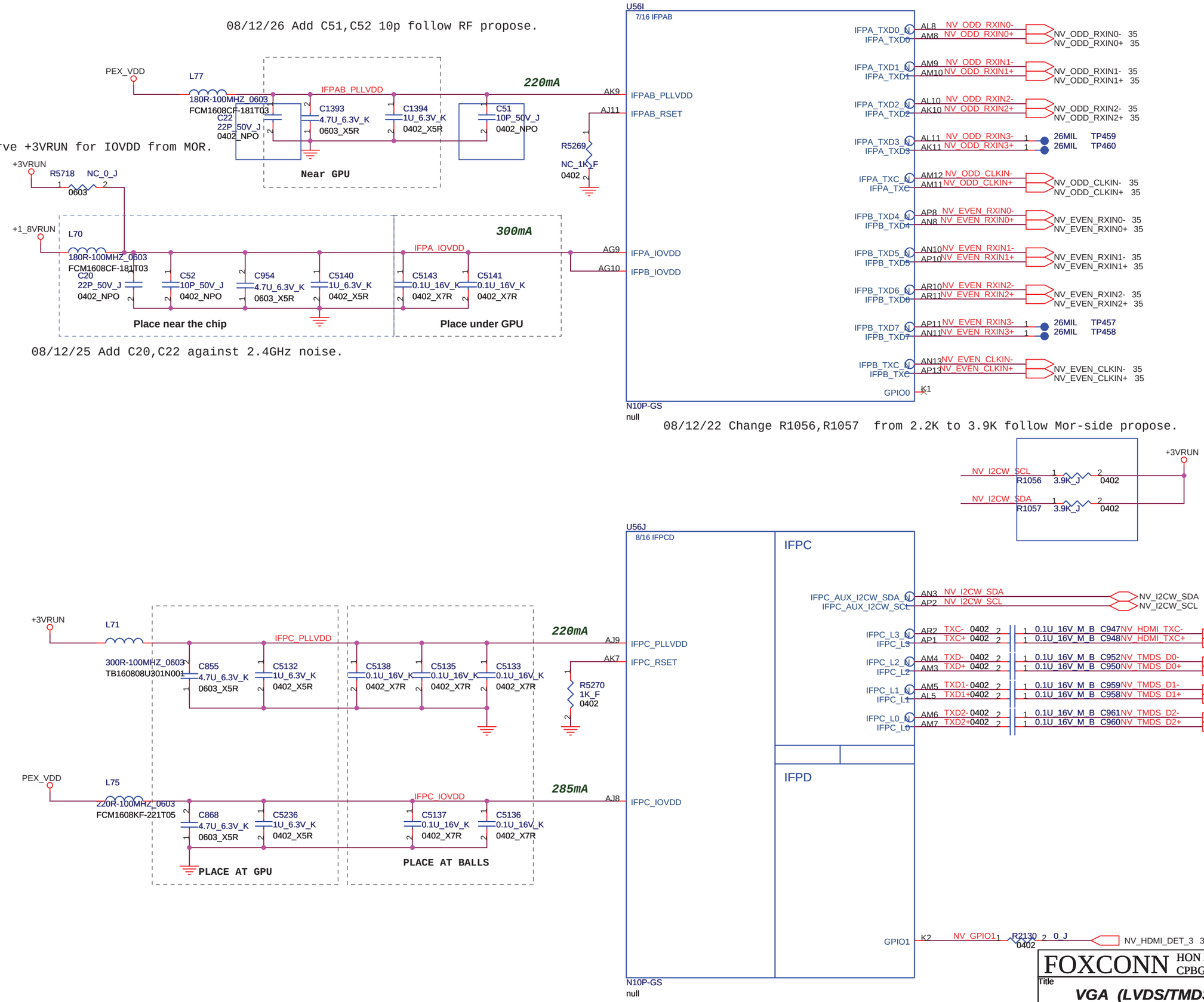
Date: Friday, October 23, 2009 Sheet 25 of 73

08/12/26 Add C51,C52 10p follow RF propose.

09/02/05 Reserve +3VRUN for IOVDD from MOR.

08/12/25 Add C20,C22 against 2.4GHz noise.

08/12/22 Change R1056,R1057 from 2.2K to 3.9K follow Mor-side propose.



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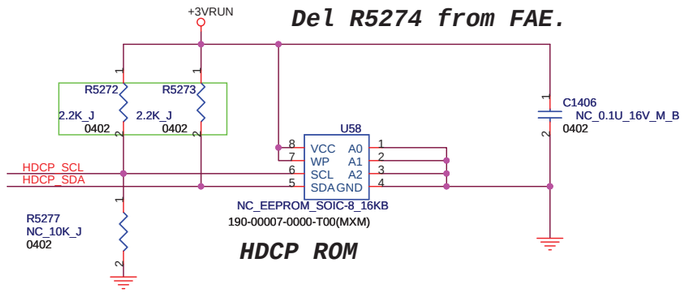
Title: VGA (LVDS/TMDS) 6/9

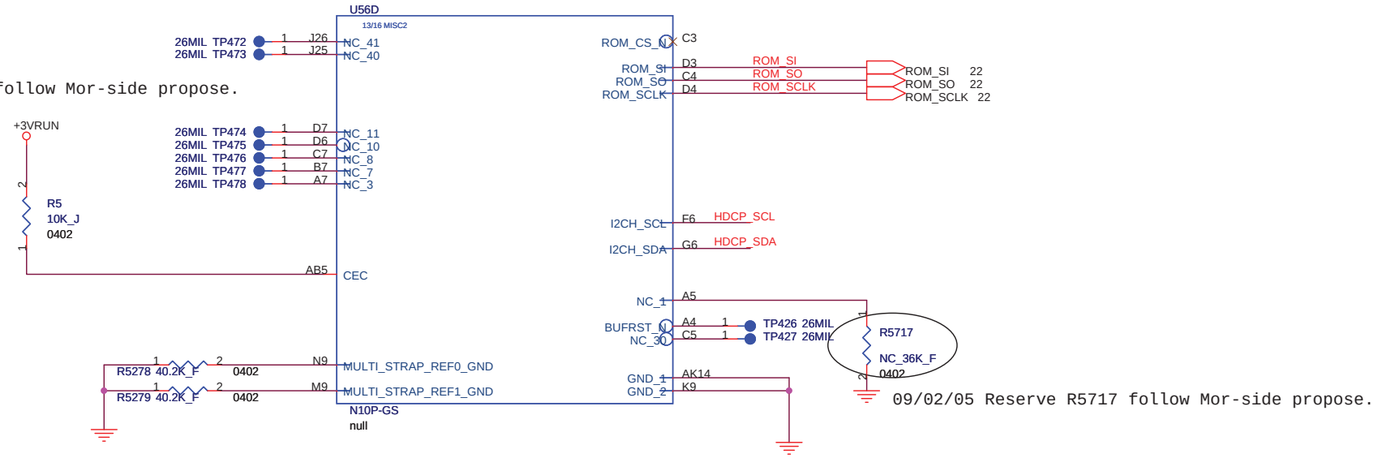
Size	Document Number	Rev
A3	M9A0_MP	1.1

Date: Friday, October 23, 2009 Sheet 26 of 73

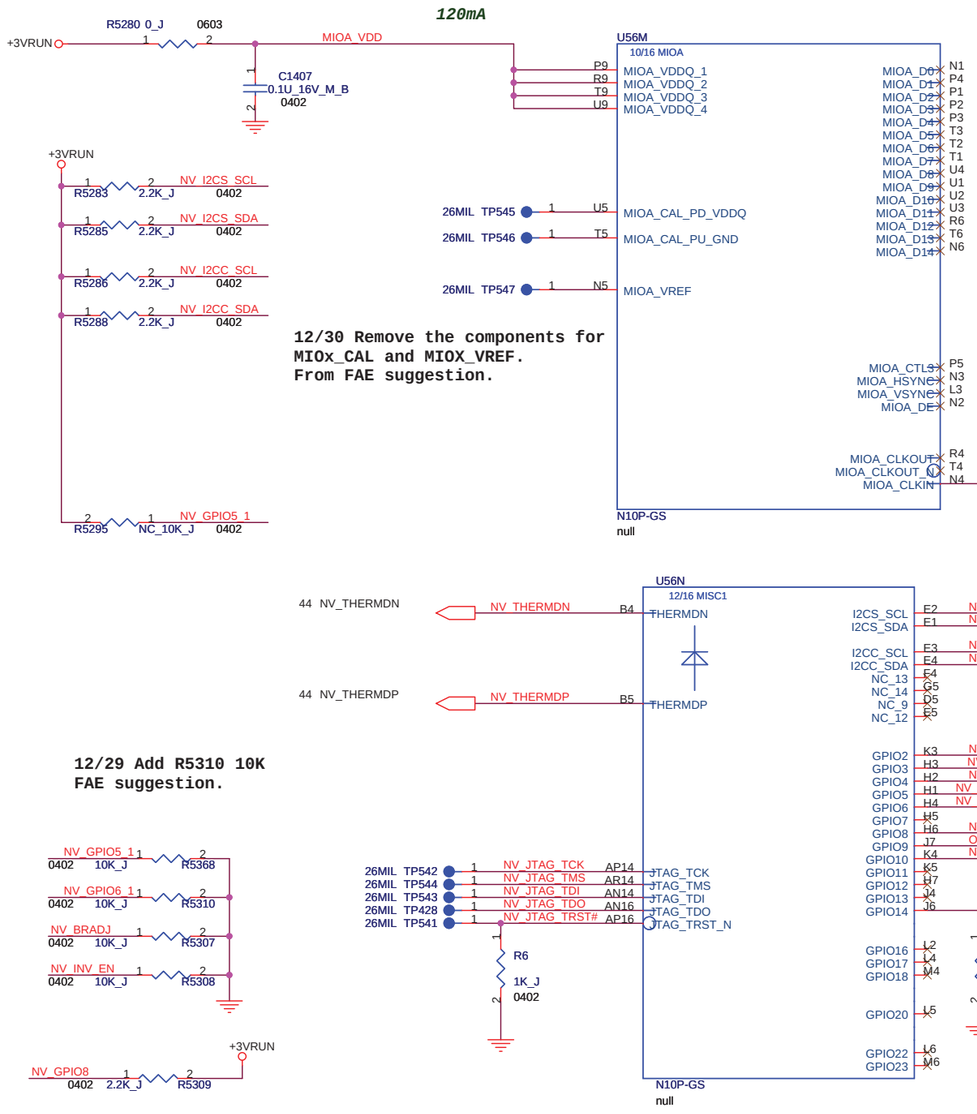


2009.0921
change R5272,R5273from NC to mount

08/12/26 Add R5 follow Mor-side propose.



09/02/05 Reserve R5717 follow Mor-side propose.



12/30 Remove the components for MIOx_CAL and MIOX_VREF. From FAE suggestion.

12/29 Add R5310 10K FAE suggestion.

12/29 Add 10K FAE suggestion.

GPIO	I/O	Internal pull low	GPIO TABLE	
GPIO0	I	YES		
GPIO1	I	Yes	HDMI Hot Plug Detect 0(HPD0)	**Active High**
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM)	**Active High**
GPIO3	O	No	Panel Power(LCD0_VDD)	**Active High**
GPIO4	O	Yes	LCD Backlight enable(LCD0_BL_EN)	**Active High**
GPIO5	O	Yes	FOR Power Control NVDD	
GPIO6	O	No	FOR Power Control NVDD	
GPIO8	O	No	reserve for reset EC	
GPIO9	I	No	System Power Limit Alert Input	**Active Low**

SIGNAL	I/O	Description
I2CA_SCL I2CA_SDA	I/O	For CRT VGA I2C_Compatibal Bus Signals
I2CB_SCL I2CB_SDA	I/O	NC(for DVI I2C_Compatibal Bus Signals)
I2CC_SCL I2CC_SDA	I/O	NC(Notebook DVI I2C_Compatibal Bus Signals)
I2CS_SCL I2CS_SDA	I/O	For VGA thermial I2C_Compatibal Bus Signals. Support a direct interface to the internal temperature sensor

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Title: VGA (XTAL/GPIO) 7/9

Size: Custom | Document Number: M9A0_MP | Rev: 1.1

Date: Friday, October 23, 2009 | Sheet 27 of 73

PEX_VDD
L81
C1410 1U_25V_K_B 0603
100NH_0603 TL160808-R10K
close GPU
C5152 1U_6.3V_K 0402_X5R
C861 4.7U_6.3V_K 0603_X5R
close GPU BALL
PLLVDD
C1412 0.1U_16V_M_B 0402
C1416 0.1U_16V_M_B 0402
105mA
45mA
PEX_VDD
L83
C1411 1U_25V_K_B 0603
100NH_0603 TL160808-R10K
C862 4.7U_6.3V_K 0603_X5R
C5153 1U_6.3V_K 0402_X5R
close GPU
2009.0921
add R5313 follow design guide
18 R_XTALSSIN
R797 0_J 0402 XTALSSIN
near GPU
R5313 10K_J 0402
18 R_NV_XTALIN
R5311 0_J 0402 NV_XTALIN
U56E
14/16 XTAL_PLL
AE9 PLLVDD
AD9 VID_PLLVDD
AE9 SP_PLLVDD
D2 XTAL_SSIN
B1 XTAL_IN
N10P-GS
null
XTAL_OUTBUFF D1 XTALOUTBUFF
XTAL_OUT B2 NV_XTALOUT
26MIL
TP429
R5312 10K_J 0402
+3VRUN
R815 0_J 0603
Place CAPS&RES CLOSE TO GPU PINS
120mA
MIOB_VDD
C1408 0.1U_16V_K 0402_X7R
U56L
11/16 MIOB
AA9 MIOB_VDDQ_1
AB9 MIOB_VDDQ_2
W9 MIOB_VDDQ_3
Y9 MIOB_VDDQ_4
AA7 MIOB_CAL_PD_VDDQ
AA6 MIOB_CAL_PU_GND
AF1 MIOB_VREF
MIOB_D0 Y1
MIOB_D1 Y2
MIOB_D2 Y3
MIOB_D3 AB3
MIOB_D4 AB2
MIOB_D5 AB1
MIOB_D6 AC4
MIOB_D7 AC1
MIOB_D8 AC2
MIOB_D9 AC3
MIOB_D10 AE3
MIOB_D11 AE2
MIOB_D12 U6
MIOB_D13 W6
MIOB_D14 Y6
STRAP0 W5 STRAP0
STRAP1 W7 STRAP1
STRAP2 V7 STRAP2
STRAP0 22
STRAP1 22
STRAP2 22
MIOB_CTL3 W3
MIOB_HSYNC W1
MIOB_VSYNC W2
MIOB_DE Y5
MIOB_CLKOUT V4
MIOB_CLKOUT_N W4
MIOB_CLKIN AE1
N10P-GS
null
R37 10K_J 0402
NVIDIA recommends in DG
+3VRUN
R5325 NC_10K_F 0402
R5323 10K_F 0402
R5367 NC_10K_F 0402
R5324 10K_F 0402
U56K
9/16 IFPEF
AJ6 IFPEF_PLLVDD
AL1 IFPEF_RSET
AE7 IFPE_IOVDD
AD7 IFPF_IOVDD
N10P-GS
null
IFPE
IFPE_AUX_I2CY_SDA_N AD4
IFPE_AUX_I2CY_SCL AE4
IFPE_L3_N AE5
IFPE_L3 AE6
IFPE_L2_N AF5
IFPE_L2 AF4
IFPE_L1_N AG4
IFPE_L1 AH4
IFPE_L0_N AH5
IFPE_L0 AH6
GPIO15 L1
IFPF
IFPF_AUX_I2CZ_SDA_N AF2
IFPF_AUX_I2CZ_SCL AF3
IFPF_L3_N AH3
IFPF_L3 AH2
IFPF_L2_N AH1
IFPF_L2 AJ1
IFPF_L1_N AJ2
IFPF_L1 AJ3
IFPF_L0_N AL3
IFPF_L0 AL2
GPIO21 K6

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA (INTER DISPLAY) 8/9

Size	Document Number	Rev
A3	M9A0_MP	1.1

Date: Friday, October 23, 2009 Sheet 28 of 73

M9A0 NVVDD current N11P_LP1 is 21.94A   N11M_GE1 is 16.29A

NV_VDD

NV_VDD

U56O

16/16 NVVDD

AB11	VDD_001	VDD_057	P21
AB13	VDD_002	VDD_058	P23
AB15	VDD_003	VDD_059	P25
AB17	VDD_004	VDD_060	R11
AB19	VDD_005	VDD_061	R12
AB21	VDD_006	VDD_062	R13
AB23	VDD_007	VDD_063	R14
AB25	VDD_008	VDD_064	R15
AC11	VDD_009	VDD_065	R16
AC12	VDD_010	VDD_066	R17
AC13	VDD_011	VDD_067	R18
AC14	VDD_012	VDD_068	R19
AC15	VDD_013	VDD_069	R20
AC16	VDD_014	VDD_070	R21
AC17	VDD_015	VDD_071	R22
AC18	VDD_016	VDD_072	R23
AC19	VDD_017	VDD_073	R24
AC20	VDD_018	VDD_074	R25
AC21	VDD_019	VDD_075	T12
AC22	VDD_020	VDD_076	T14
AC23	VDD_021	VDD_077	T16
AC24	VDD_022	VDD_078	T18
AC25	VDD_023	VDD_079	T20
AD12	VDD_024	VDD_080	T22
AD14	VDD_025	VDD_081	T24
AD16	VDD_026	VDD_082	V11
AD18	VDD_027	VDD_083	V13
AD22	VDD_028	VDD_084	V15
AD24	VDD_029	VDD_085	V17
L11	VDD_030	VDD_086	V19
L12	VDD_031	VDD_087	V21
L13	VDD_032	VDD_088	V23
L14	VDD_033	VDD_089	V25
L15	VDD_034	VDD_090	W11
L16	VDD_035	VDD_091	W12
L17	VDD_036	VDD_092	W13
L18	VDD_037	VDD_093	W14
L19	VDD_038	VDD_094	W15
L20	VDD_039	VDD_095	W16
L21	VDD_040	VDD_096	W17
L22	VDD_041	VDD_097	W18
L23	VDD_042	VDD_098	W19
L24	VDD_043	VDD_099	W20
L25	VDD_044	VDD_100	W21
M12	VDD_045	VDD_101	W22
M14	VDD_046	VDD_102	W23
M16	VDD_047	VDD_103	W24
M18	VDD_048	VDD_104	W25
M20	VDD_049	VDD_105	Y12
M22	VDD_050	VDD_106	Y14
M24	VDD_051	VDD_107	Y16
P11	VDD_052	VDD_108	Y18
P13	VDD_053	VDD_109	Y20
P15	VDD_054	VDD_110	Y22
P17	VDD_055	VDD_111	Y24
P19	VDD_056		

N10P-GS

null

NV_VDD

PLACE WHERE POSSIBLE UNDER BGA

C5230 0.01U_16V_K 0402_X7R

C5229 0.01U_16V_K 0402_X7R

C5228 0.01U_16V_K 0402_X7R

C5227 0.01U_16V_K 0402_X7R

C5226 0.01U_16V_K 0402_X7R

C5225 0.01U_16V_K 0402_X7R

C5206 0.047U_16V_K 0402_X7R

C5220 0.047U_16V_K 0402_X7R

C5209 0.047U_16V_K 0402_X7R

C5160 0.022U_16V_K 0402_X7R

C5161 0.022U_16V_K 0402_X7R

C5216 0.022U_16V_K 0402_X7R

C5243 1U_6.3V_K 0603_X7R

C6038 4700P_16V_K 0402_X7R

C6039 4700P_16V_K 0402_X7R

C5201 0.022U_16V_K 0402_X7R

C6040 0.22U_6.3V_K 0402_X5R

C6041 0.22U_6.3V_K 0402_X5R

C6021 4.7U_6.3V_K 0603_X5R

C5195 10U_6.3V_M 0603_X5R

C5199 10U_6.3V_M 0603_X5R

Near BGA

U56P

15/16 GND

AA11	GND_22	GND_18	E15
AA12	GND_125	GND_19	E18
AA13	GND_136	GND_20	E24
AA14	GND_147	GND_21	E27
AA15	GND_158	GND_24	E30
AA16	GND_169	GND_25	E6
AA17	GND_180	GND_26	E9
AA18	GND_191	GND_27	F2
AA19	GND_193	GND_28	F31
AA2	GND_23	GND_29	F34
AA20	GND_34	GND_30	F5
AA21	GND_45	GND_31	J2
AA22	GND_56	GND_32	J31
AA23	GND_67	GND_33	J34
AA24	GND_78	GND_35	J5
AA25	GND_89	GND_36	L9
AA34	GND_100	GND_37	M11
AA5	GND_111	GND_38	M13
AB12	GND_122	GND_39	M15
AB14	GND_126	GND_40	M17
AB16	GND_127	GND_41	M19
AB18	GND_128	GND_42	M2
AB20	GND_129	GND_43	M21
AB22	GND_130	GND_44	M23
AB24	GND_131	GND_46	M25
AC9	GND_132	GND_47	M31
AD11	GND_133	GND_48	M34
AD13	GND_134	GND_49	M5
AD15	GND_135	GND_50	N11
AD17	GND_137	GND_51	N12
AD2	GND_138	GND_52	N13
AD21	GND_139	GND_53	N14
AD23	GND_140	GND_54	N15
AD25	GND_141	GND_55	N16
AD31	GND_142	GND_57	N17
AD34	GND_143	GND_58	N18
AD5	GND_144	GND_59	N19
AE11	GND_145	GND_60	N20
AE12	GND_146	GND_61	N21
AE13	GND_148	GND_62	N22
AE14	GND_149	GND_63	N23
AE15	GND_150	GND_64	N24
AE16	GND_151	GND_65	N25
AE17	GND_152	GND_66	P12
AE18	GND_153	GND_68	P14
AE19	GND_154	GND_69	P16
AE20	GND_155	GND_70	P18
AE21	GND_156	GND_71	P20
AE22	GND_157	GND_72	P22
AE23	GND_159	GND_73	P24
AE24	GND_160	GND_74	R2
AE25	GND_161	GND_75	R31
AG2	GND_162	GND_76	R34
AG31	GND_163	GND_77	R5
AG34	GND_164	GND_79	T11
AG5	GND_165	GND_80	T13
AK2	GND_166	GND_81	T15
AK31	GND_167	GND_82	T17
AK34	GND_168	GND_83	T19
AK5	GND_170	GND_84	T21
AL12	GND_171	GND_85	T23
AL15	GND_172	GND_86	T25
AL18	GND_173	GND_87	U11
AL21	GND_174	GND_88	U12
AL24	GND_175	GND_90	U13
AL27	GND_176	GND_91	U14
AL30	GND_177	GND_92	U15
AL6	GND_178	GND_93	U16
AL9	GND_179	GND_94	U17
AN2	GND_181	GND_95	U18
AN34	GND_182	GND_96	U19
AP12	GND_183	GND_97	U20
AP15	GND_184	GND_98	U21
AP18	GND_185	GND_99	U22
AP21	GND_186	GND_101	U23
AP24	GND_187	GND_102	U24
AP27	GND_188	GND_103	U25
AP3	GND_189	GND_104	V12
AP30	GND_190	GND_105	V14
AP33	GND_192	GND_106	V16
AP6	GND_3	GND_107	V18
AP9	GND_4	GND_108	V2
B12	GND_5	GND_109	V20
B15	GND_6	GND_110	V22
B21	GND_7	GND_112	V24
B24	GND_8	GND_113	V31
B27	GND_9	GND_114	V5
B3	GND_10	GND_115	V9
B30	GND_11	GND_116	Y11
B33	GND_12	GND_117	Y13
B6	GND_13	GND_118	Y15
B9	GND_14	GND_119	Y17
C2	GND_15	GND_120	Y19
C34	GND_16	GND_121	Y21
E12	GND_17	GND_123	Y23
		GND_124	Y25

N10P-GS

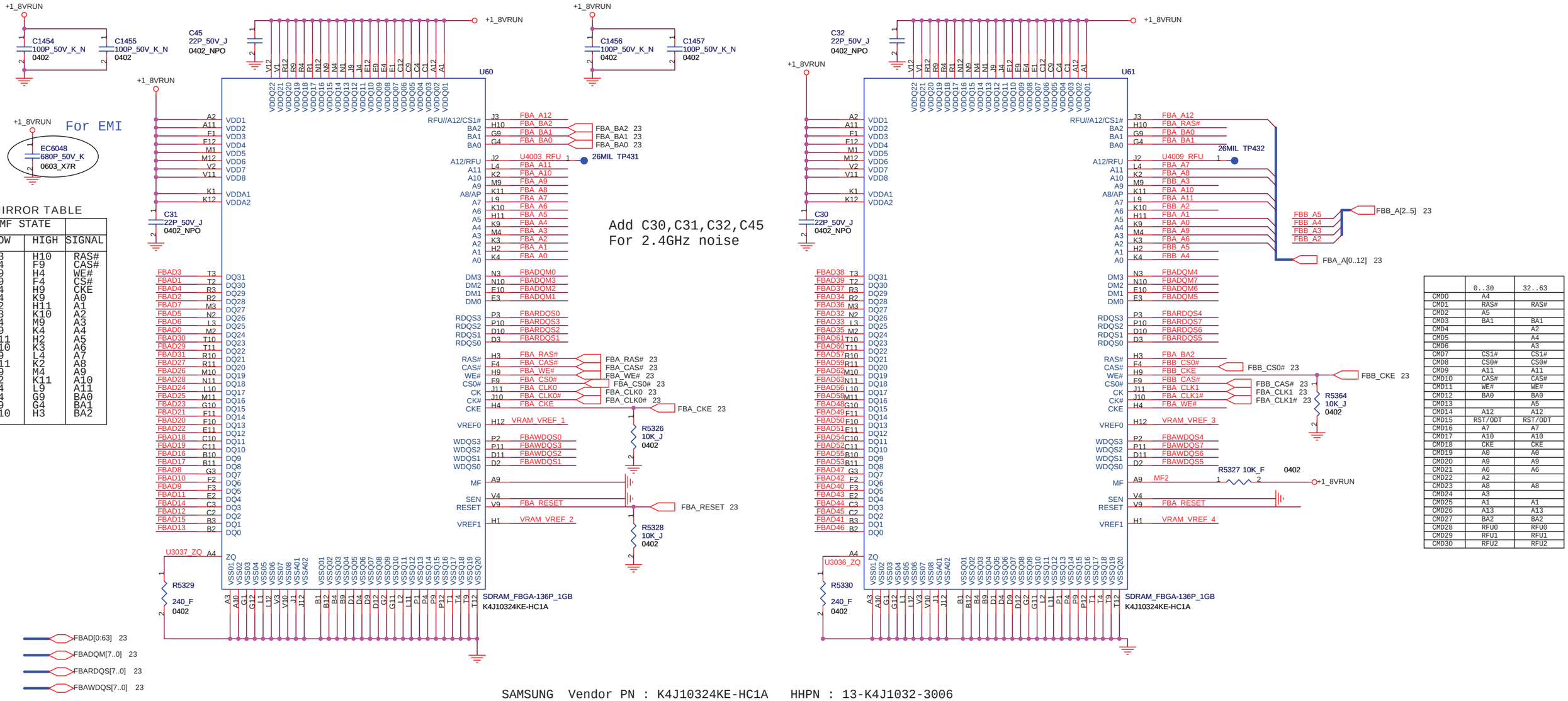
null

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: VGA(POWER/GROUND) 9/9

Size: A3 | Document Number: M9A0_MP | Rev: 1.1

Date: Tuesday, November 03, 2009 | Sheet 29 of 73



	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7	CS1#	CS1#
CMD8	CS0#	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST/ODT	RST/ODT
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	RFU0	RFU0
CMD29	RFU1	RFU1
CMD30	RFU2	RFU2

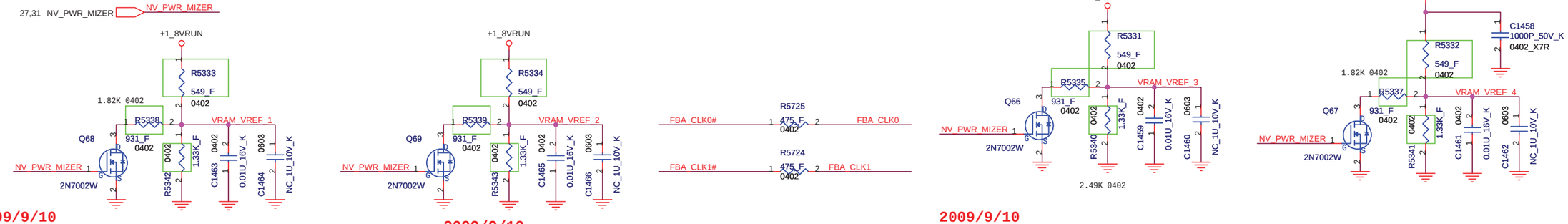
MIRROR TABLE

MF STATE		
LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F9	F4	CS#
H4	H9	CKE
K4	K9	A0
K3	K10	A1
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
G9	G4	BA1
H10	H3	BA2

Add C30,C31,C32,C45
For 2.4GHz noise

SAMSUNG Vendor PN : K4J10324KE-HC1A HHPN : 13-K4J1032-3006
HYNIX Vendor PN : H5RS1H23MFR-N0C HHPN : 13-H5RS1H2-3001

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V



2009/9/10
N11P-LP1+SAMSUNG(H2 SKU)
Change R5340,R5341,R5342,R5343 from 1R-0001331-F200(1.33K) to 1R-0000222-J200(2.2K) for nVIDIA FAE suggest.

2009/9/10
N11P-LP1+SAMSUNG(H2 SKU)
Change R5331,R5332,R5333,R5334 from 1R-0005490-F200(549ohm) to 1R-0009310-F200(931ohm) for nVIDIA FAE suggest.

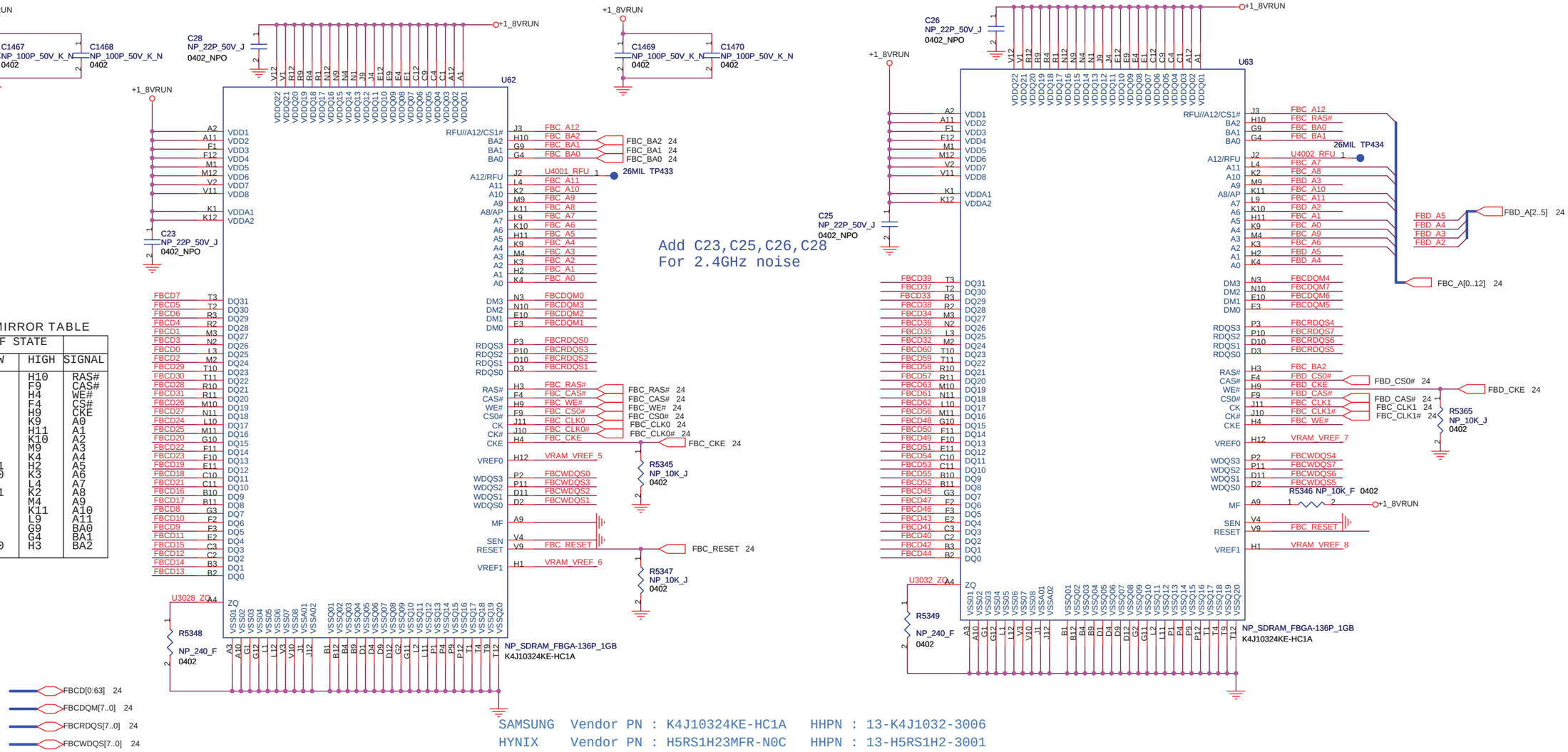
2009/9/10
N11P-LP1+SANSUNG(H2 SKU)
Change R5335,R5337,R5338,R5339 from 1R-0009310-F200(931ohm) to 1R-0000122-F200(1.2K) for nVIDIA FAE suggest.

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: *VRAM(GDDR)# 1/2*

Size: Custom | Document Number: *M9A0_MP* | Rev: *1.1*

Date: Thursday, November 19, 2009 | Sheet 30 of 73



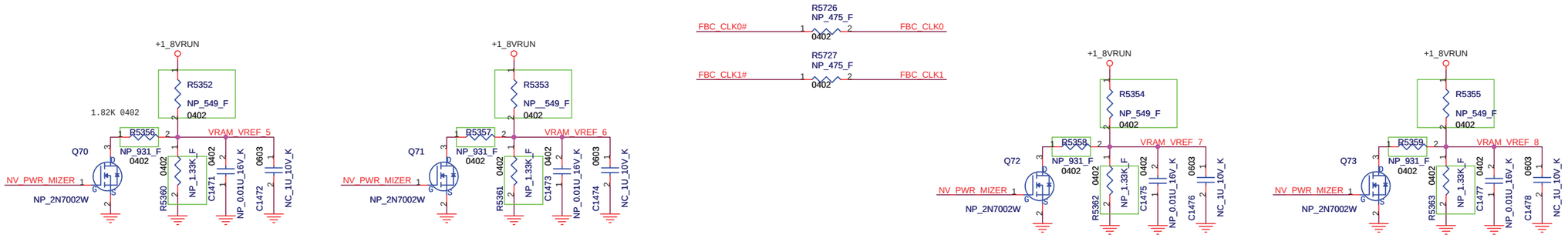
MIRROR TABLE

MF STATE		
LOW	HIGH	SIGNAL
H3	H10	RAS#
F4	F9	CAS#
H9	H4	WE#
F9	F4	CS#
H4	H9	CKE
K4	K9	A0
H2	H11	A1
K3	K10	A2
M4	M9	A3
K9	K4	A4
H11	H2	A5
K10	K3	A6
L9	L4	A7
K11	K2	A8
M9	M4	A9
K2	K11	A10
L4	L9	A11
G4	G9	BA0
G9	G4	BA1
H10	H3	BA2

	0..30	32..63
CMD0	A4	
CMD1	RAS#	RAS#
CMD2	A5	
CMD3	BA1	BA1
CMD4		A2
CMD5		A4
CMD6		A3
CMD7	CS1#	CS1#
CMD8	CS0#	CS0#
CMD9	A11	A11
CMD10	CAS#	CAS#
CMD11	WE#	WE#
CMD12	BA0	BA0
CMD13		A5
CMD14	A12	A12
CMD15	RST/ODT	RST/ODT
CMD16	A7	A7
CMD17	A10	A10
CMD18	CKE	CKE
CMD19	A0	A0
CMD20	A9	A9
CMD21	A6	A6
CMD22	A2	
CMD23	A8	A8
CMD24	A3	
CMD25	A1	A1
CMD26	A13	A13
CMD27	BA2	BA2
CMD28	RFU0	RFU0
CMD29	RFU1	RFU1
CMD30	RFU2	RFU2

SAMSUNG Vendor PN : K4J10324KE-HC1A HHPN : 13-K4J1032-3006
HYNIX Vendor PN : H5RS1H23MFR-N0C HHPN : 13-H5RS1H2-3001

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V



2009/9/10
N11P-LP1+SAMSUNG(H2 SKU)
Change R5356,R5357,R5358,R5359 from
1R-0009310-F200(931ohm) to 1R-0000122-F200(1.2K)
for nVIDIA FAE suggest.

2009/9/10
N11P-LP1+SAMSUNG(H2 SKU)
Change R5352,R5353,R5354,R5355 from
1R-0005490-F200(549ohm) to 1R-0009310-F200(931ohm)
for nVIDIA FAE suggest.

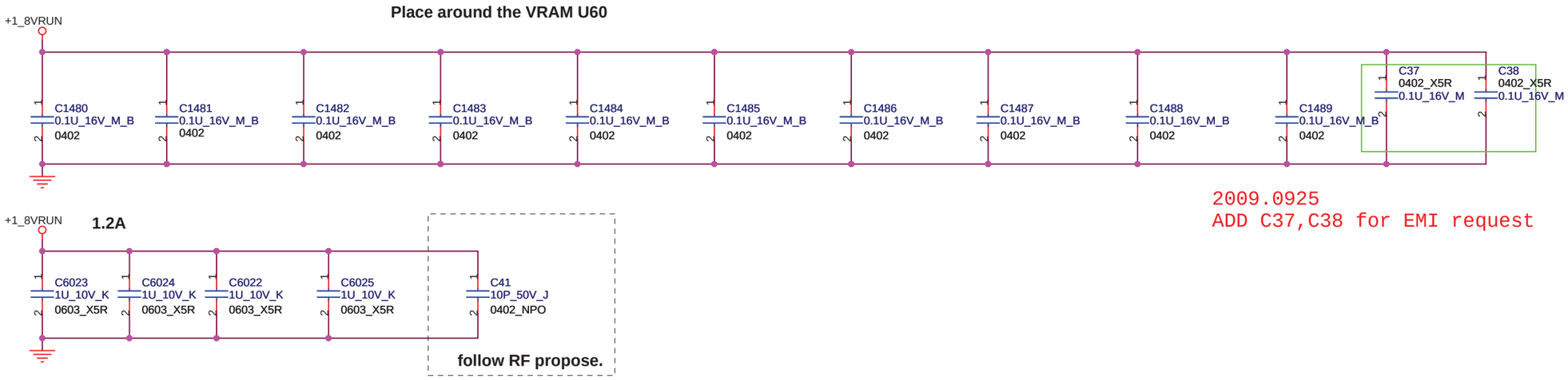
2009/9/10
N11P-LP1+SAMSUNG(H2 SKU)
Change R5360,R5361,R5362,R5363 from
1R-0001331-F200(1.33K) to 1R-0000222-J200(2.2K)
for nVIDIA FAE suggest.

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

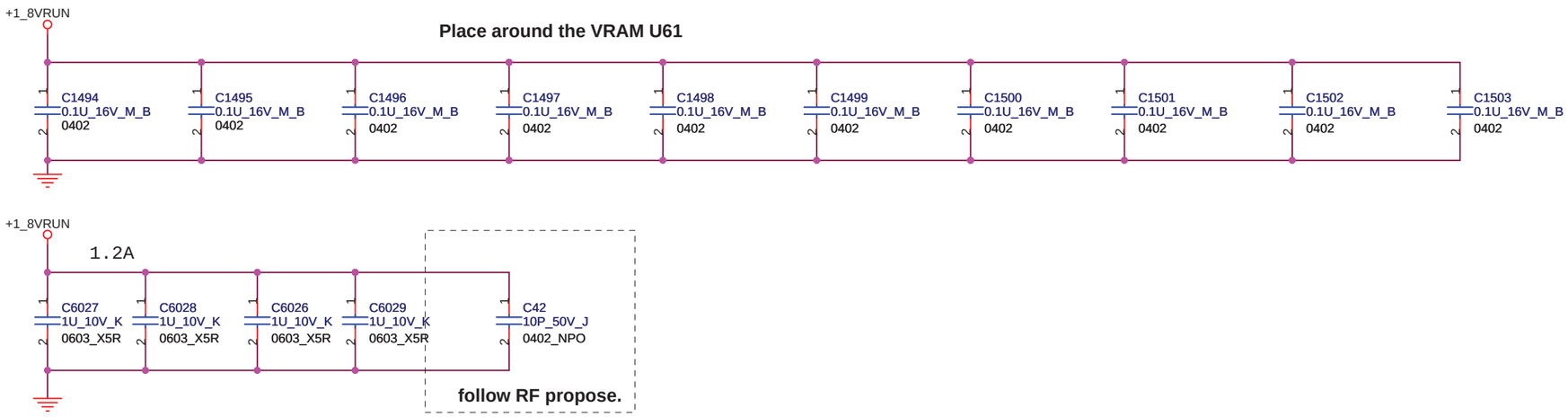
Title: VRAM(GDDR)# 2/2

Size: Custom | Document Number: M9A0_MP | Rev: 1.1

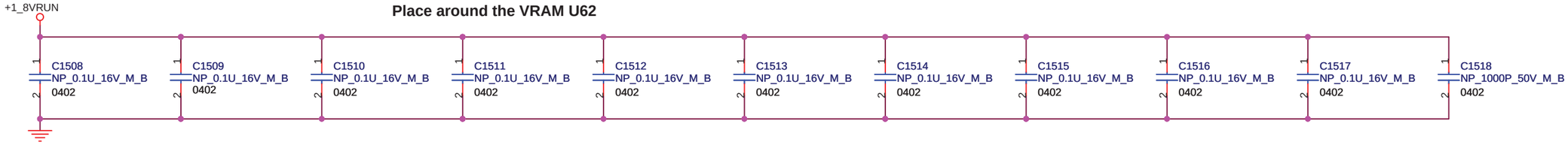
Date: Thursday, November 19, 2009 | Sheet 31 of 73

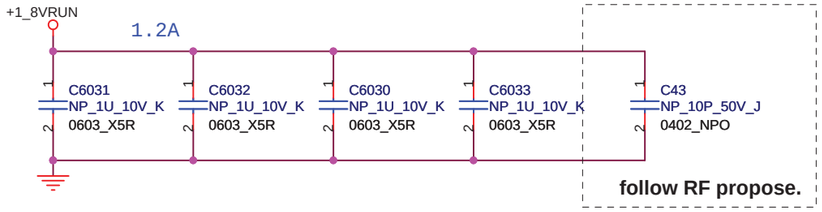


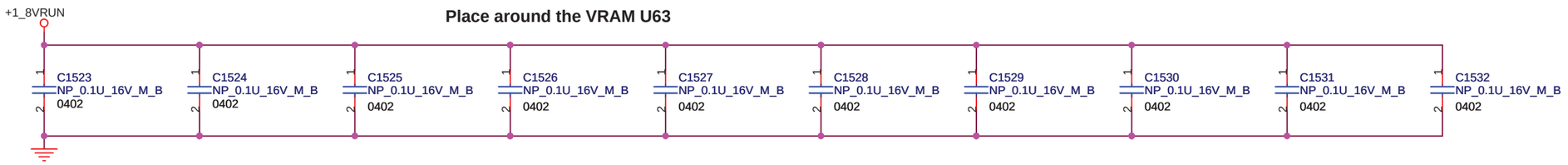
2009.0925
ADD C37,C38 for EMI request

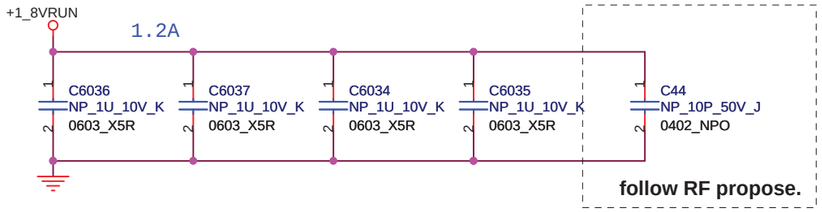


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***VRAM (POWERBYPASS) 1 OF 2***	
Size A3	Document Number ***M9A0_MP***	Rev ***1.1***
Date: Saturday, September 26, 2009	Sheet 32 of 73	









FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: ***VRAM (POWERBYPASS) 2 OF 2***

Size	Document Number	Rev
A3	***M9A0_MP***	***1.1***

Date: Friday, November 20, 2009 Sheet 33 of 73

D_SHIFT_+5VRUN
R417
2.2K_J
0402
CRT_DDCCLK_R
R413 2 0_J 1 0402 CRT_DDCCLK
C577
NC_220P_50V_J_N
0402

D_SHIFT_+5VRUN
R441
2.2K_J
0402
CRT_DDCDATA_R
R434 2 0_J 1 0402 CRT_DDCDATA
C592
NC_220P_50V_J_N
0402

For EMI

Semi-PnP Circuit

37 EN_EXT_DEV_SENSE
Q5
NC_PDTC144EU
VGA_CRT_DET#
D1
NC_BAT54S
+3VRUN

Semi-PnP

26,36 NV_HDMI_DET_3
(HDMI)
NV_HDMI_DET_3
NC_MC74VHC1G86DFT2G
U42
+3VRUN
C83
NC_0.1U_16V_Y
0402_Y5V
MB_CRT_DET#
MB_CRT_DET# 37
Semi-PnP(EC IN)
R627
NC_10K_J
0402
(CRT)
VGA_CRT_DET#
R284
NC_0_J
0402
R293
NC_10K_J
0402

+5VRUN
D11
SSM22LLPT
null
VR10
NC_MLVS0603M04_VR
D_SHIFT_+5VRUN
F4
15V-0.35A_1206
SMD1206P035TF/16

Change R83,R72,R64 to 75ohm --MOR 2/27

25 NV_DACA_RED
L17
120R-100MHZ_0603
EBMS160808A121
R83
75_F
0402
C84
NC_10P_50V_J_N
0402
C85
10P_50V_J_N
0402

25 NV_DACA_GREEN
L16
120R-100MHZ_0603
EBMS160808A121
R72
75_F
0402
C78
NC_10P_50V_J_N
0402
C79
10P_50V_J_N
0402

25 NV_DACA_BLUE
L14
120R-100MHZ_0603
EBMS160808A121
R64
75_F
0402
C75
NC_10P_50V_J_N
0402
C68
10P_50V_J_N
0402

CN2
J_RED
J_GREEN
J_BLUE
CRT_+5VRUN
R292 1 0_J 2 0402 VGA_CRT_DET#
CRT_DDCDATA
HSYNC13
VSYNC14
CRT_DDCCLK
D-SUB FEMALE CONN_15P
FOX_DZ11A91-MB229-9H

CRT CONNECTOR

+5VRUN
C602
0.1U_16V_Y
0402_Y5V
+3VRUN
C98
0.1U_16V_M_B
0402
D_SHIFT_+5VRUN
C77
0.1U_16V_Y
0402_Y5V
0.1U_16V_M_B

U7
CM2009-02QR
VCC_VIDEO
VCC_DDC
VCC_SYNC
BYP
DDC_IN1
DDC_IN2
SYNC_IN1
SYNC_IN2
DDC_OUT1
DDC_OUT2
SYNC_OUT1
SYNC_OUT2
GND

J_RED
J_BLUE
J_GREEN
25 NV_I2CA_SCL
25 NV_I2CA_SDA
25 NV_DACA_HSYNC
25 NV_DACA_VSYNC
NV_I2CA_SCL
NV_I2CA_SDA
NV_DACA_HSYNC
NV_DACA_VSYNC
BYP C93 1 2 0402
CRT_DDCCLK_R
CRT_DDCDATA_R
HSYNC R424 1 33_J 2 0402
VSYNC R418 1 33_J 2 0402
HSYNC13
VSYNC14
C583
NC_47P_50V_J_N
0402
C584
NC_47P_50V_J_N
0402

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: CRT		
Size: A3	Document Number: M9A0_MP	Rev: 1.1
Date: Thursday, October 29, 2009	Sheet 34 of 73	

LVDS CONNECTOR

2009.11.03
Add C60,C62,C63,C64

2009.1104
Add C65,C66,C67,C73,C74 for FAN issue

DCBATOUT

C537 0.1U_50V_K_B 0603 NC
C526 0.1U_25V_K 0603_X5R
C525 0.1U_50V_K_B 0603
C70 10P_50V_J_N 0402
C60 0.1U_50V_K_B 0603
C62 0.1U_50V_K_B 0603
C63 0.1U_50V_K_B 0603
C64 0.1U_50V_K_B 0603
C65 0.1U_50V_K_B 0603
C66 0.1U_50V_K_B 0603
C67 0.1U_50V_K_B 0603
C73 0.1U_50V_K_B 0603
C74 0.1U_50V_K_B 0603

2009.0925
Add C70 for RF request

2009.0925
ADD C53,C54,C61 for EMI request

DCBATOUT
C53 0.1U_50V_K_B 0603
C54 0.1U_50V_K_B 0603
C61 0.1U_50V_K_B 0603

+3VRUN
C543 0.1U_16V_Y_Y 0402
INV_BRADJ
C549 680P_50V_K 0402_X7R

U131D 74LCX08MTC
INV_EN
27 NV_BRADJ
NV_BRADJ
R383 NC_10K_J 0402

L43 NC_600R-100MHZ_0805 ACMS201209A601 2A

For rush current issue

DCBATOUT
Q177 SI2303BDS
R5736 47K_J 0402
C575 0.1U_50V_K_B 0603
R5737 47K_J 0402
F17 467002. 32V-2A_0603
C541 0.1U_50V_K_B 0603
DCBATOUT_L

2009.0926
ADD C549 680P for EMI request
place it near LVDS connector

CN18 FOX_GS12401-1011-9H
SMDFIX2 SMDFIX4 SMDFIX3 SMDFIX1
FPC CONN_40P

INV_ENABLE
INV_BRADJ

26 NV_EVEN_CLKIN- NV_EVEN_CLKIN-
26 NV_EVEN_CLKIN+ NV_EVEN_CLKIN+
26 NV_EVEN_RXIN0- NV_EVEN_RXIN0-
26 NV_EVEN_RXIN0+ NV_EVEN_RXIN0+
26 NV_EVEN_RXIN1- NV_EVEN_RXIN1-
26 NV_EVEN_RXIN1+ NV_EVEN_RXIN1+
26 NV_EVEN_RXIN2- NV_EVEN_RXIN2-
26 NV_EVEN_RXIN2+ NV_EVEN_RXIN2+
26 NV_ODD_CLKIN- NV_ODD_CLKIN-
26 NV_ODD_CLKIN+ NV_ODD_CLKIN+
26 NV_ODD_RXIN0- NV_ODD_RXIN0-
26 NV_ODD_RXIN0+ NV_ODD_RXIN0+
26 NV_ODD_RXIN1- NV_ODD_RXIN1-
26 NV_ODD_RXIN1+ NV_ODD_RXIN1+
26 NV_ODD_RXIN2- NV_ODD_RXIN2-
26 NV_ODD_RXIN2+ NV_ODD_RXIN2+

2009.0918
DVT2 CN18 change to Halogen Free

+3VRUN
C542 0.1U_16V_Y_Y 0402
U131A 74LCX08MTC
37,50 LIDIN# LIDIN#
27 NV_INV_EN NV_INV_EN
R5241 NC_10K_J 0402

+3VRUN
C540 0.1U_16V_Y_Y 0402
U131B 74LCX08MTC
14 INV_EN
INV_EN
NV_INV_EN1
R301 NC_10K_J 0402

+3VRUN
C547 0.1U_16V_Y_Y 0402
U131C 74LCX08MTC
37 BL_OFF#
INV_ENABLE_2
INV_ENABLE
R394 10K_J 0402
C539 680P_50V_K 0402_X7R
R10 NC_0_J 0402

2009.0926
Change C539 TO 680P for EMI request

LCDVCC
C570 0.1U_10V_K 0402_X5R
C1264 47P_50V_K 0402_NPO
C24 22P_50V_J 0402_NPO

follow RF propose.

2009.0928
change C1264 to 47P for RF request

Current limit is from 1.1A to 2.1A.

2009.10.23
Delete J2,J3

+3VRUN
C992 1000P_50V_K 0402_X7R
C249 4.7U_6.3V_K 0805_X5R
U31 G5281RC1U_V0.1
IN1 IN5
OUT IN4
EN IN3
GND IN2
THERMAL PAD

BFT test TOP
+3VRUN TP900 tpc40b_75
+3VRUN TP901 tpc40b_75
BFT test BOT

LCDID0 TP897 tpc40b_75
LCDID1 TP898 tpc40b_75
LCDID2 TP899 tpc40b_75
BFT test BOT

R5999 10K_F 0402
R6000 10K_F 0402
R6001 10K_F 0402
R6002 10K_F 0402
R6003 10K_F 0402
SW1 HDS506-E_SW-SMD12P
null ***PANEL ID***
LCDID0 14
LCDID1 14
LCDID2 14
DIS_FAN_MON# 37
INST_ON_SW# 37
TP418 20MIL

LCDVCC
C251 4.7U_10V_Y 0805_Y5V
C96 0.1U_16V_Y 0402_Y5V
27 NV_LCDVCC_EN NV_LCDVCC_EN
C250 0.1U_16V_Y 0402_Y5V
R5234 10K_J 0402

12/29 change to 10K
FAE suggestion.

2009.10.23
Add test point TP897,TP898,TP899 ,
TP900,TP901 for PVT

	DIS_FAN_MON#	LCDID2	LCDID1	LCDID0
AUO B140XW02 V1	0	0	0	1
LGD LP140WH2-TLN1	0	0	1	0
SAMSUNG LTN140AT08	0	0	1	1
AUO B140RW02 V0	0	1	0	0
DISABLE FAN LOCK FUNCTION	0	X	X	X

ON:0 , OFF:1

LCDID0 TP892 tpc40b_75
LCDID1 TP893 tpc40b_75
LCDID2 TP894 tpc40b_75
DIS_FAN_MON# TP895 tpc40b_75
INST_ON_SW# TP896 tpc40b_75
BFT Test TOP

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title **LVDS**
Size A3 | Document Number M9A0_MP | Rev 1.1
Date: Wednesday, November 04, 2009 | Sheet 35 of 73

HDMI CONNECTOR

26 NV_HDMI_TXC-
26 NV_HDMI_TXC+
26 NV_TMDS_D0-
26 NV_TMDS_D0+
26 NV_TMDS_D1-
26 NV_TMDS_D1+
26 NV_TMDS_D2-
26 NV_TMDS_D2+

0402 2 499_F 1 R22 NV_HDMI_TXC-
0402 2 499_F 1 R35 NV_HDMI_TXC+
0402 2 499_F 1 R33 NV_TMDS_D0-
0402 2 499_F 1 R23 NV_TMDS_D0+
0402 2 499_F 1 R24 NV_TMDS_D1-
0402 2 499_F 1 R26 NV_TMDS_D1+
0402 2 499_F 1 R25 NV_TMDS_D2-
0402 2 499_F 1 R28 NV_TMDS_D2+

Q1 2N7002W
+5VRUN
R27 NC_100K_J 0402

+3VRUN
R42 2.2K_J 0402
NV_HDMI_DET_3
NV_HDMI_DET_3 26,34
R38 2.2K_J 0402
Q9A 2N7002SPT
Q9B 2N7002SPT
NV_HDMI_DET_5

CN31
HDMI RECEPTACLE_19P
FOX_QJ1119L-NT10-4H
Data2+ / Data2- / TMDS Data1 Shield / Data0+ / Data0- / TMDS Clock Shield / CEC / SCL / DDC/CEC Ground / Hot Plug Detect / PTH1 / PTH3
TMDS Data2 Shield / Data1+ / Data1- / TMDS Data0 Shield / TMDS Clock+ / TMDS Clock- / Reserved / SDA / +5V Power / PTH2 / PTH4
NV_TMDS_D2+ NV_TMDS_D2- NV_TMDS_D0+ NV_TMDS_D0- GHDMI_SCL NV_HDMI_DET_5
NV_TMDS_D1+ NV_TMDS_D1- NV_HDMI_TXC+ NV_HDMI_TXC- GHDMI_SDA HDMI_+5VRUN

R522 100K_J 0402

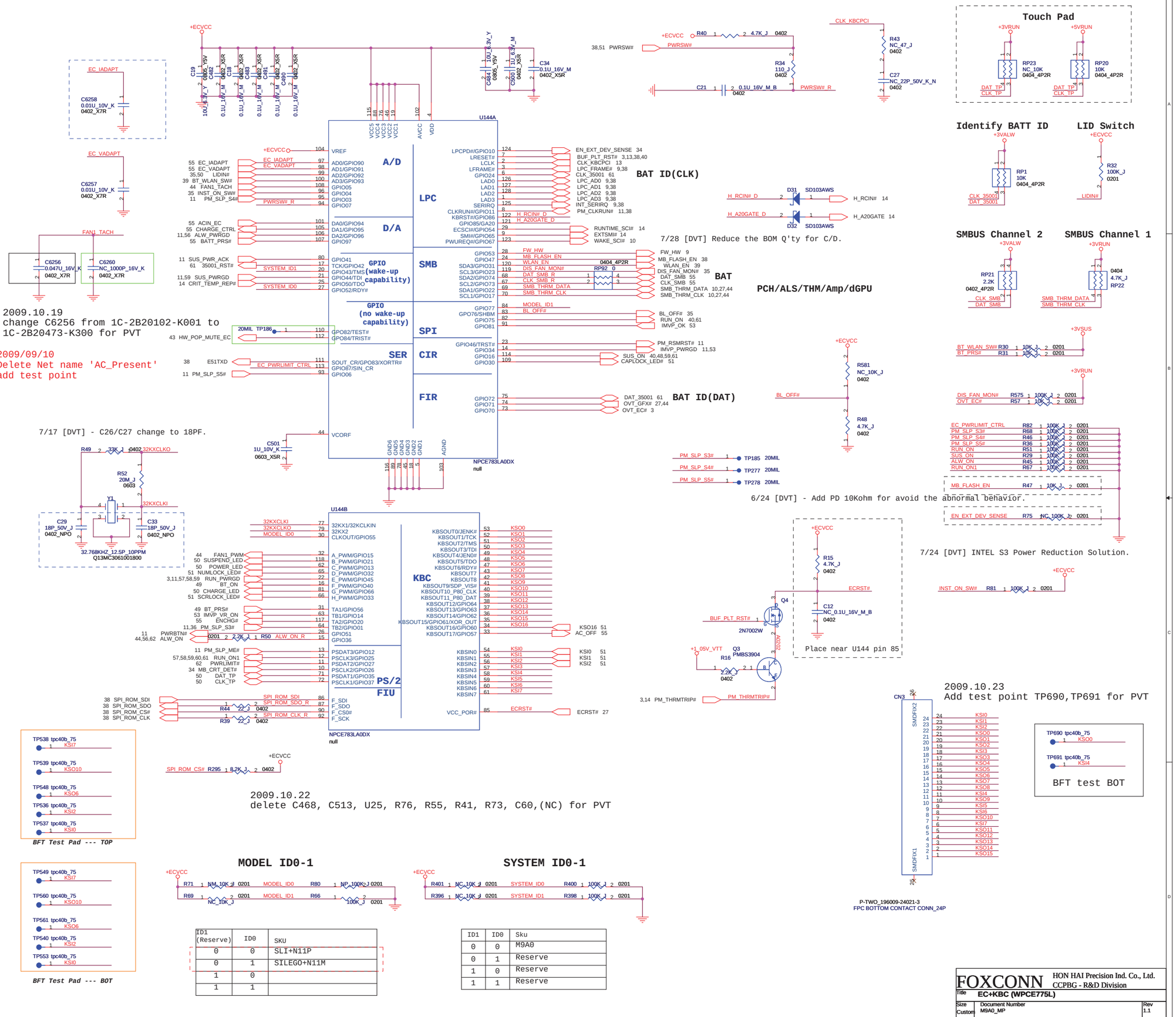
U130 Rclamp0504F
GHDMI_SDA GHDMI_SCL NV_HDMI_DET_5

+3VRUN
R512 1K_J 0402
R532 1K_J 0402
Q174A UPA672T-T1-A
Q174B UPA672T-T1-A
26 NV_I2CW_SCL
26 NV_I2CW_SDA
NV_I2CW_SCL
NV_I2CW_SDA
GHDMI_SCL
GHDMI_SDA

+5VRUN
BAS316PT D20
BAS316PT D23
R511 2.2K_J 0402
R506 2.2K_J 0402

+5VRUN
C997 1000P_50V_K 0402_X7R
F9 16V-0.25_1206 SMD1206P025TF
HDMI_+5VRUN_F
R347 NC_0_J 0402
D19 NC_CH551H-30PT
HDMI_+5VRUN1
Q52 SI2301BDS-T1-E3
L151 33R-100MHZ_0805 BCMS201209A330
C1615 NC_0.1U_16V_M_B 0402
R2373 10K_J 0402
HDMI_+5VRUN
C1536 0.1U_16V_Y 0402_Y5V
C998 0402_X7R NC_1000P_50V_K
11,37 PM_SLP_S3#
Q51 PDTC144EU.115 null

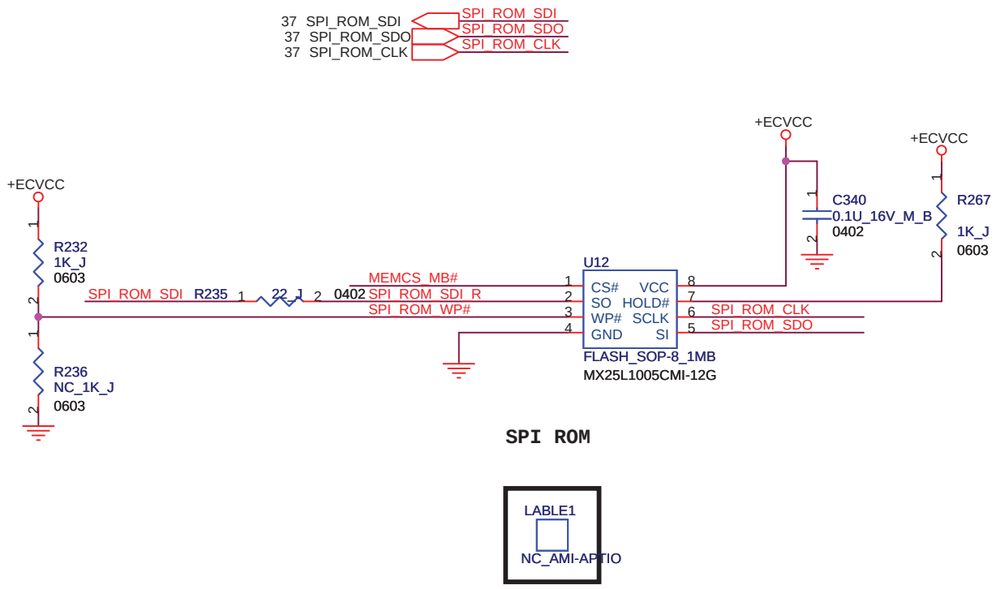
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HDMI	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 30, 2009	Sheet 36 of 73	

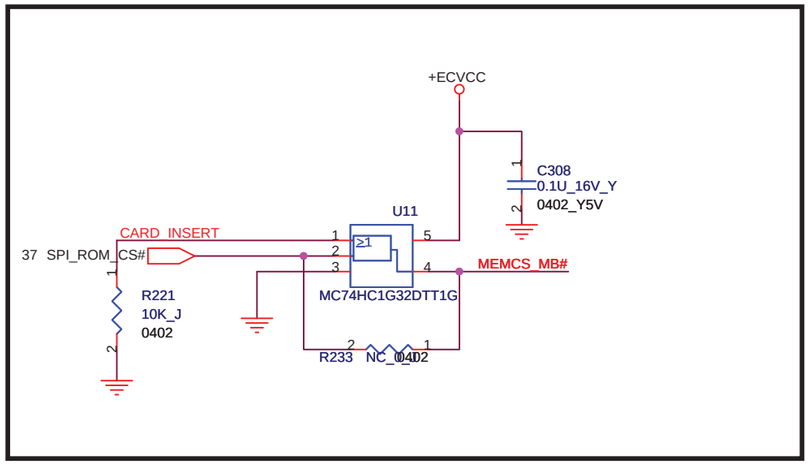


ID1 (Reserve)	ID0	SKU
0	0	SLI+N11P
0	1	SILEGO+N11M
1	0	
1	1	

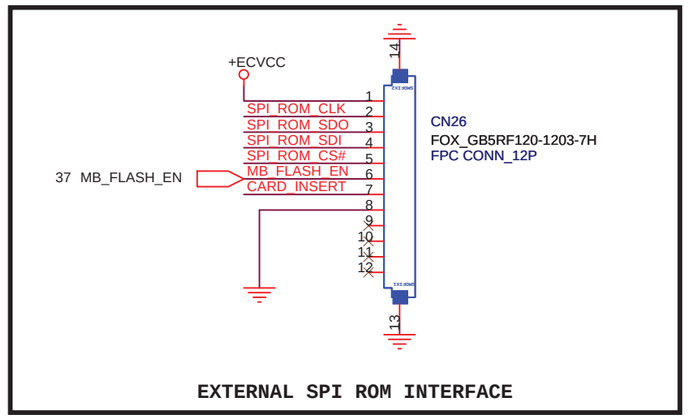
ID1	ID0	Sku
0	0	M9A0
0	1	Reserve
1	0	Reserve
1	1	Reserve

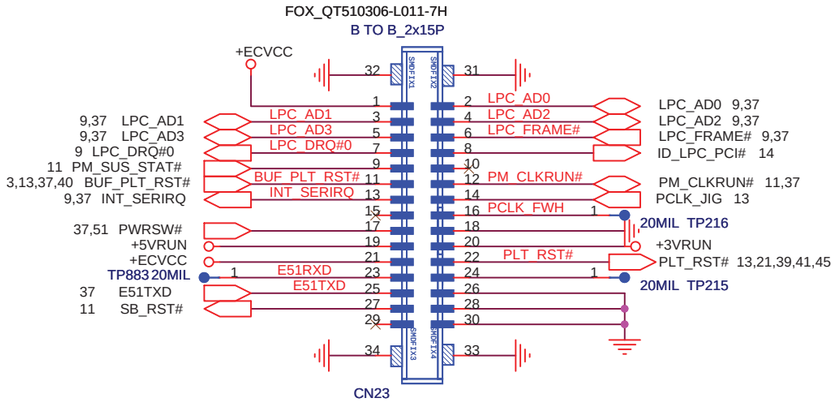
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	EC+KBC (WPCE775L)	
Size: Custom	Document Number: M9A0_MP	Rev: 1.1
Date: Friday, October 30, 2009	Sheet 37 of 73	





2009.10.23
Delete TP531,TP530,TP532,TP533,TP529,TP520,519,TP518





FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: Flash ROM/SPI		
Size: A3	Document Number: M9A0_MP	Rev: 1.1
Date: Friday, October 23, 2009	Sheet 38 of 73	

SW4.C pin delete and SW4.A connect to GND.

DVT

BOSS2
BOSS_2.3x4
null

BOSS1
BOSS_2.3x4
null

2009.0922
change BOSS1,BOSS2 to 1M-1F40M20-1500 for ME request

SW4
SSSS811101_SW-SMD7
BT_WLAN_SW#
BT_WLAN_SW# 37

TP640 tpc40t_50
BT_WLAN_SW#

CN21
MINI PCIE_52P
FOX_AS0B226_S40N_7F

11,40,41 PCIE_WAKE#	1	WAKE#	
	3	BT_DATA	
	5	BT_CHCLK	
10 WLAN_CLKREQ#	7	CLKREQ#	
	9	GND2	
10 CLK_PCIE_MINI#	11	REFCLK-	
10 CLK_PCIE_MINI	13	REFCLK+	
	15	GND3	
	17	RESERVED6	
	19	RESERVED7	
	21	GND5	
10 MINI_RXN1	23	PERn0	
10 MINI_RXP1	25	PERp0	
	27	GND7	
	29	GND8	
10 MINI_TXN1	31	PETn0	
10 MINI_TXP1	33	PETp0	
	35	GND10	
MINI_PCIE_+3_3V	37	RESERVED11	
	39	RESERVED13	
	41	RESERVED14	
	43	RESERVED15	
	45	RESERVED16	
	47	RESERVED17	
	49	RESERVED18	
	51	RESERVED19	
	55	SMDFIX1	
	53	NPTH1	
	54	SMDFIX2	
	56	NPTH2	
	2	+3_3V1	MINI_PCIE_+3_3V
	4	GND1	
	6	+1_5V1	MINI_PCIE_1_5V
	8	RESERVED1	
	10	RESERVED2	
	12	RESERVED3	
	14	RESERVED4	
	16	RESERVED5	
	18	GND4	
	20	W_DISABLE#	WLAN_EN 37
	22	PERST#	PLT_RST# 13,21,38,41,45
	24	+3_3Vaux	MINI_PCIE_+3_3V
	26	GND6	
	28	+1_5V2	
	30	RESERVED8	
	32	RESERVED9	
	34	GND9	
	36	RESERVED10	USB_PN12_L
	38	RESERVED12	USB_PP12_L
	40	GND11	
	42	LED_WWAN#	
	44	LED_WLAN#	MINI_CARD_LED#
	46	LED_WPAN#	A4311
	48	+1_5V3	
	50	GND12	
	52	+3_3V2	MINI_PCIE_+3_3V

49 WIRELESS_DATA
49 WIRELESS_CHCLK
R5710 100K_J 0402
R5711 100K_J 0402

20MIL TP159 1

Q21
SRK7002
D22
BAS316PT
Q20
DTA114YUB
null
+3VSUS
WLAN_EN
tpc40t_50 TP499
R386 120_J 0402
TP509 tpc40t_50
null
LTST-S321KGKT
LED3
49 BT_LED
Q49
PDTC144EU.115
null

2009.0922
change CN21 TO 1N-1052000-0000 for ME request

20MIL TP160 1 CLK_PCIE_MINI#
20MIL TP161 1 CLK_PCIE_MINI

For DVT SI validation,
Top-side and closer Pin11.13

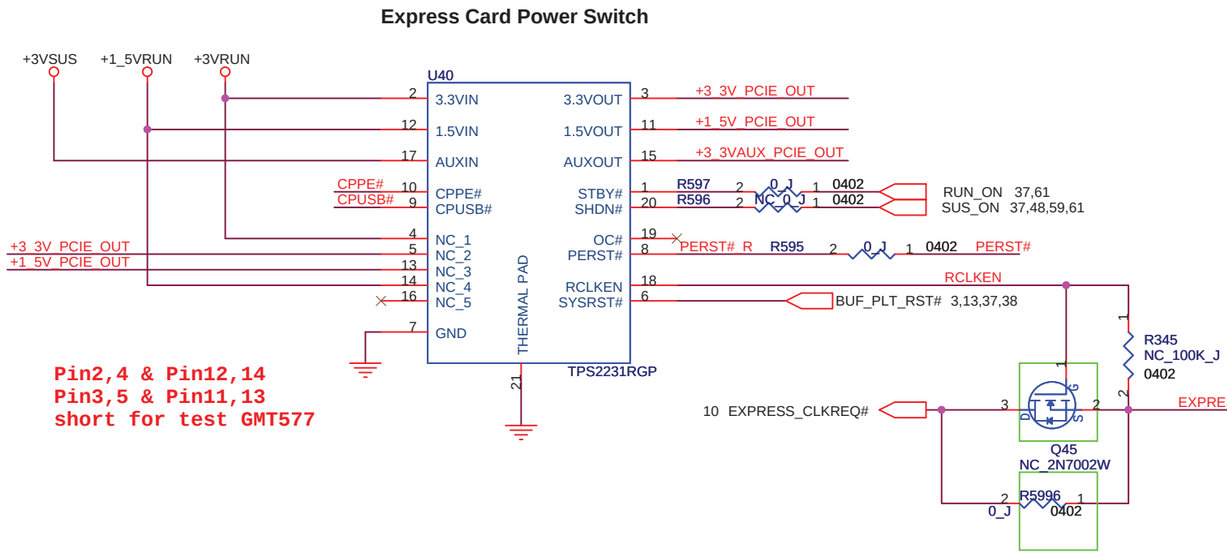
U24
NC_SN74CB3Q3305PW
C534 NC_0.1U_16V_Y 0402_Y5V
13 USB_PN12
USB_PP12 13
MINI_PCIE_+3_3V
USB_PN12_L
USB_PP12_L

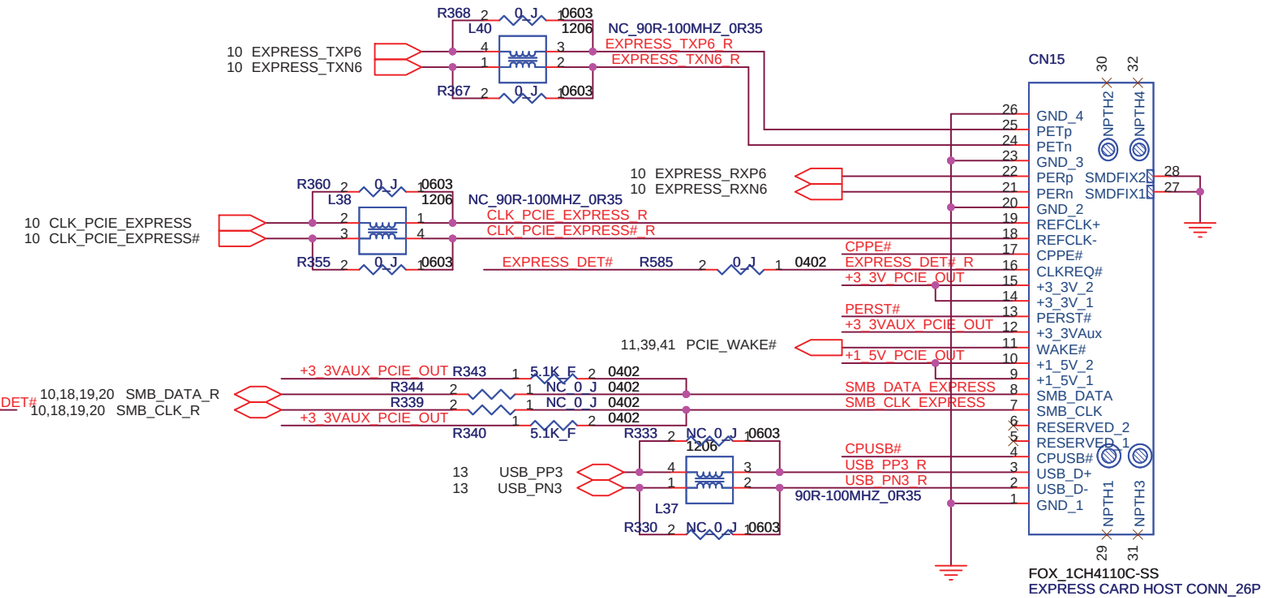
+3VSUS
R387 0_J 0805
MINI_PCIE_+3_3V
C538 NC_22U_6.3V_M 0805_X5R
C531 NC_0.1U_16V_Y 0402_Y5V
C546 NC_0.1U_16V_Y 0402_Y5V
C572 NC_0.1U_16V_Y 0402_Y5V
C573 NC_0.1U_16V_Y 0402_Y5V
C574 NC_0.1U_16V_Y 0402_Y5V
C529 10U_10V_M 0805_X5R
C548 10U_10V_M 0805_X5R

+1_5VRUN
R5730 NC_0_J 0603
MINI_PCIE_1_5V
C545 NC_0.1U_10V_K 0402_X5R
C544 NC_10U_10V_M 0805_X5R
C536 NC_10U_10V_M 0805_X5R

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Half Mini Card		
Size A3	Document Number M9A0_MP		Rev 1.1
Date: Friday, October 23, 2009	Sheet 39 of 73		

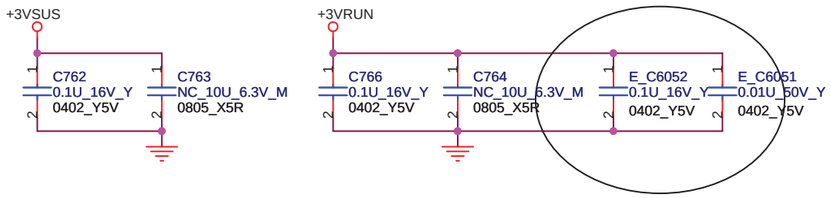
Express Card Power Switch



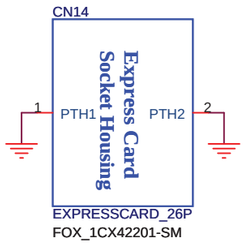


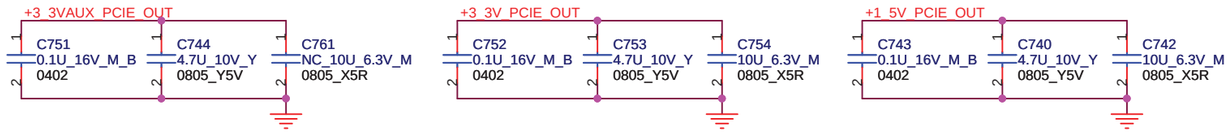
2009.0922
CHANGE Q45 TO NC ,R5996 TO MOUNT

Express Card Slot.



For EMI close C764





FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: EXPRESS CARD		
Size: A3	Document Number: M9A0_MP	Rev: 1.1
Date: Friday, October 23, 2009	Sheet 40 of 73	

Used EEPROM R5565 need mount.
No used EEPROM R5562/R5563/U129/C5170 need NC.

+3VSUS
60R-100MHZ_0603
L152 ACMS160808A600
+3V_S3_LAN
C5163 0.1U_10V_K 0402_X5R
C5164 10U_16V_Y 1206_Y5V
C5165 0.1U_10V_K 0402_X5R
C5166 0.1U_10V_K 0402_X5R
C5167 0.1U_10V_K 0402_X5R
C5168 0.1U_10V_K 0402_X5R
C5169 0.1U_10V_K 0402_X5R
E_C6055 1000P_16V_K 0402_X7R
For EMI close C5165

10 CLK_REQ_LAN#
CLK_REQ_LAN#
VPD_DATA
VPD_CLK
+3VRUN
+1_2V_VDD_LAN
+3V_S3_LAN

U4
MARVELL
88E8057

10 LAN_RXP3
10 LAN_RXN3
C5184 0.1U_6.3V_K 0402_X5R
C5185 0.1U_6.3V_K 0402_X5R
LAN_RXP3_C
LAN_RXN3_C
10 LAN_TXN3
10 LAN_TXP3
10 CLK_PCIE_LAN
10 CLK_PCIE_LAN#

TX_P 49
TX_N 50
NC10 51
NC11 52
RX_N 53
RX_P 54
REFCLKP 55
REFCLKN 56
NC12 57
VDD1 58
LED_ACTn 59
LED_LINK10/100n 60
VDDO_TTL 61
LED_LINK1000n 62
LED_DUPLEXn 63
NC13 64
thermal pad 65

VDD8 48
VMAIN_AVLBL 47
TESTMODE 46
VDDO_TTL4 45
VDD7 44
NC9 43
CLKREQn 42
VPD_DATA 41
VDDO_TTL3 40
VDD6 39
VPD_CLK 38
SPI_CLK 37
SPI_CS 36
SPI_DI 35
SPI_DO 34
VDD5 33

AVDD18_OUT 32
MDIN[3] 31
MDIP[3] 30
NC8 29
AVDDL2 28
MDIN[2] 27
MDIP[2] 26
NC7 25
NC6 24
NC5 23
NC4 22
MDIN[1] 21
MDIP[1] 20
AVDDL1 19
MDIN[0] 18
MDIP[0] 17

MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+

VDDO_TTL1 1
VDD2 2
CTRL12 3
PD18LDO 4
PERSTN/TSTPT 5
WAKEn 6
VDD3 7
AVDDH(3.3V) 8
NC1 9
LOM_DISABLEn 10
NC2 11
NC3 12
VDD4 13
XTALO 14
XTALI 15
RSET 16

88E8057-A0-NNC2C000
null

+1_8V_AVDD_LAN
C5183 10U_10V_M 0805_X5R
E_C6054 0.01U_50V_Y 0402_Y5V
For EMI close C5183

+1_2V_VDD_LAN
598mA
C5173 10U_6.3V_Y 0805
C5174 1U_6.3V_M 0402_X5R
0.1U_6.3V_K C5175 0402_X5R
0.1U_6.3V_K C5176 0402_X5R
0.1U_6.3V_K C5177 0402_X5R
0.1U_6.3V_K C5178 0402_X5R
0.1U_6.3V_K C5179 0402_X5R
0.1U_6.3V_K C5180 0402_X5R
0.1U_6.3V_K C5181 0402_X5R
0.1U_6.3V_K C5182 0402_X5R
Close to chip

+1_8V_AVDD_LAN
C5252 0.1U_10V_K 0402_X5R
C5253 0.1U_10V_K 0402_X5R
C5254 0.1U_10V_K 0402_X5R
C5255 0.1U_10V_K 0402_X5R

+1_2V_VDD_LAN
E_C6056 0.01U_50V_Y 0402_Y5V
For EMI close C5174

+3V_S3_LAN
E_C6057 0.01U_50V_Y 0402_Y5V
For EMI close C5181

+1_2V_VDD_LAN
E_C6058 1000P_16V_K 0402_X7R
For EMI close C5179

+3V_S3_LAN
R5564 4.7K_J 0402
null
BCP69.115
Q176
C5171 0402
C5172 10U_10V_M 0805_X5R
0.1U_16V_M_B
CTRL_1D2

+3V_S3_LAN
R5562 NC_4.7K_J 0402
R5563 NC_4.7K_J 0402
U129
NC_EEPROM_TSSOP-8_8KB
AT24C08A-10TU-2.7
C5170 NC_0.1U_10V_K 0402_X5R
VPD_CLK
VPD_DATA
R5565 0_J 0402
Use internal EEPROM 1/20

R5566 4.99K_F 0402
R5567 0_J 0402
R5568 0_J 0402
R5569 0_J 0402
XTALO
XTALI
2XTALO_B
XTALO_CHIP
RSET

+3V_S3_LAN
4.7K_J R5570 0402
LOM_DISABLEn
13,21,38,39,45 PLT_RST#
11,39,40 PCIE_WAKE#

R5571 NC_10M_J 0402
Y8 25MHZ_20P_30PPM FOX_7A25000058
C5186 27P_50V_J_N 0402
C5187 27P_50V_J_N 0402

+1_8V_AVDD_LAN
L153
60R-100MHZ_0603
ACMS160808A600
+1_8V_AVDD_LAN_1
C5188 1000P_16V_K 0603_X7R

C5189 0.1U_10V_K 0402_X5R
C5190 0.1U_10V_K 0402_X5R
C5191 0.1U_10V_K 0402_X5R
C5192 0.1U_10V_K 0402_X5R
L5
1-1_350UH
LG-2413S-1
TCT1 MCT1
TD1+ MX1+
TD1- MX1-
TCT2 MCT2
TD2+ MX2+
TD2- MX2-
TCT3 MCT3
TD3+ MX3+
TD3- MX3-
TCT4 MCT4
TD4+ MX4+
TD4- MX4-
TRD0P_RJ45
TRD0N_RJ45
TRD1P_RJ45
TRD1N_RJ45
TRD2P_RJ45
TRD2N_RJ45
TRD3P_RJ45
TRD3N_RJ45
R5572 75_J 0402
R5573 75_J 0402
R5574 75_J 0402
R5575 75_J 0402
C5193 1500P_2KV_K 1808_X7R

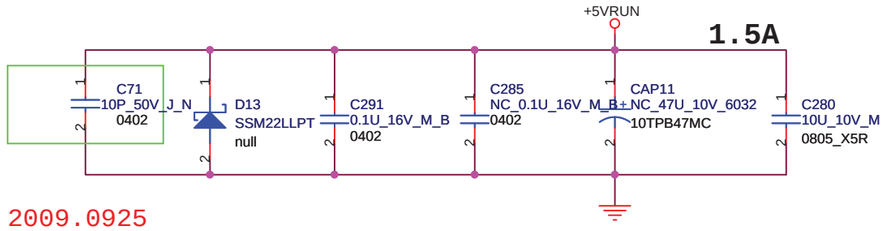
CN22
HEADER_8P
FOX_HS6108E-LH
TRD3N_RJ45
TRD3P_RJ45
TRD2N_RJ45
TRD2P_RJ45
TRD1N_RJ45
TRD1P_RJ45
TRD0N_RJ45
TRD0P_RJ45

TP524 tpc40b_75 TRD3N_RJ45
TP521 tpc40b_75 TRD3P_RJ45
TP523 tpc40b_75 TRD2N_RJ45
TP522 tpc40b_75 TRD2P_RJ45
TP526 tpc40b_75 TRD1N_RJ45
TP525 tpc40b_75 TRD1P_RJ45
TP528 tpc40b_75 TRD0N_RJ45
TP527 tpc40b_75 TRD0P_RJ45
BFT Test Pad --- BOT

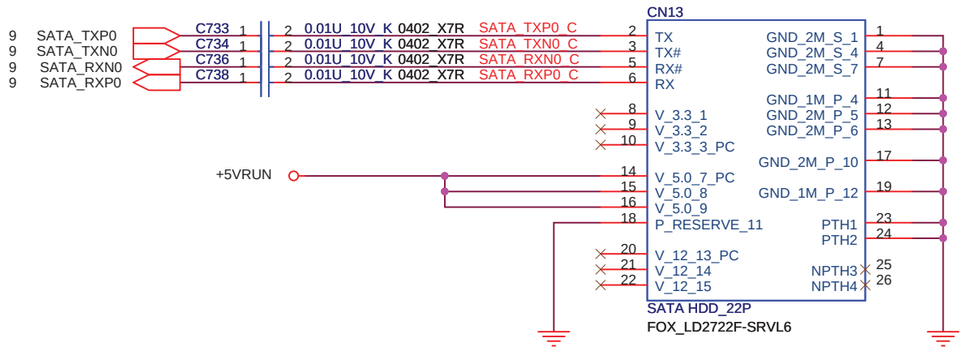
01/03 Change RJ45 From ME.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LAN (88E8057)	
Size C	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 41 of 73	

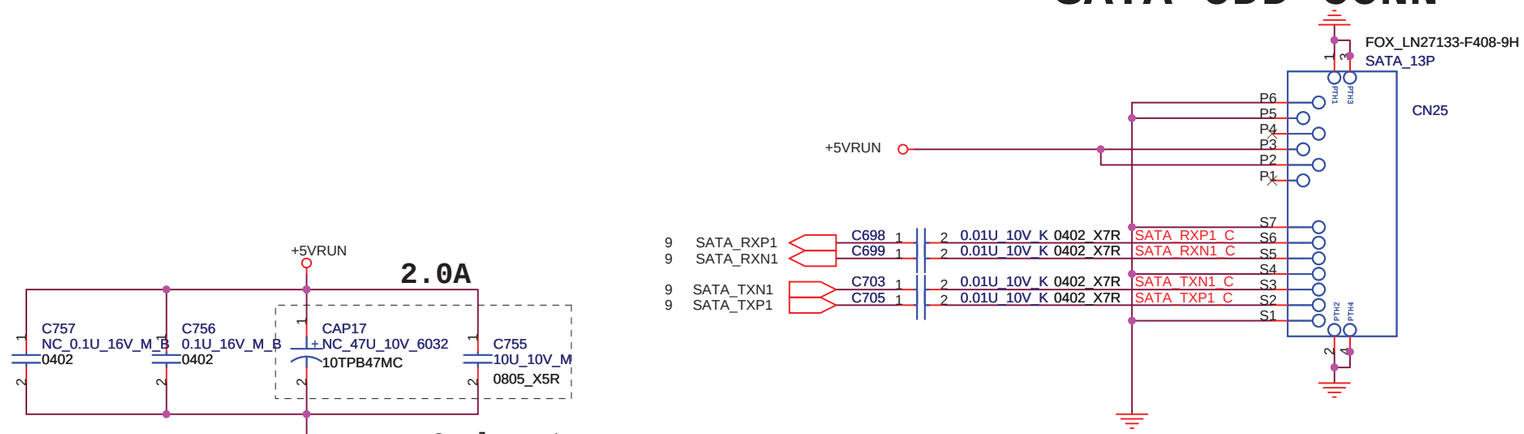
SATA HDD CONN



2009.0925
Add C71 for RF request

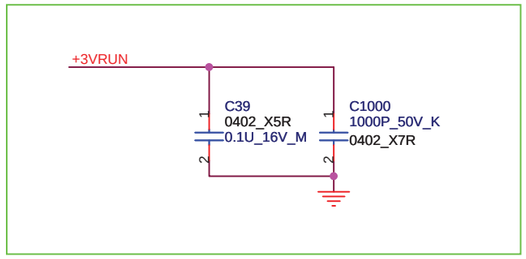


SATA ODD CONN

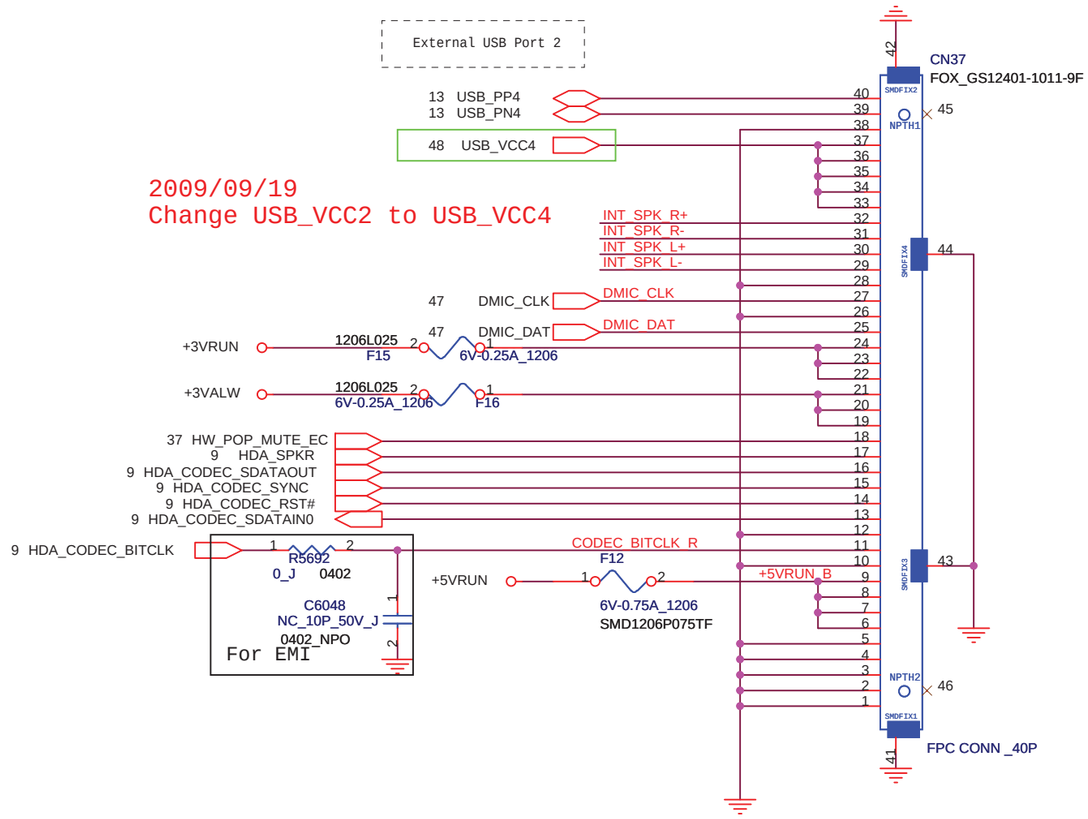


2009.0922
CN25 change to Halogen Free

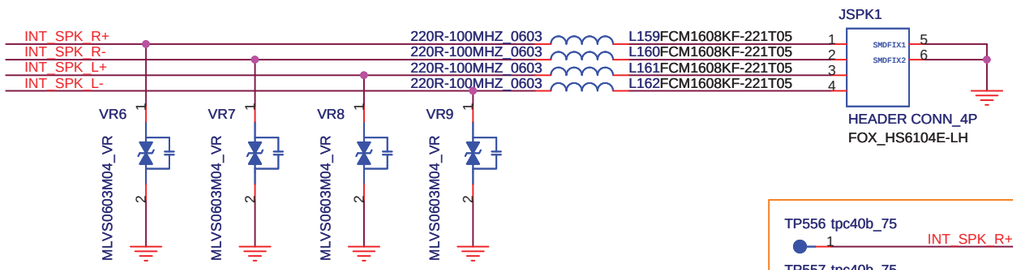
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: SATA HDD/ODD		
Size: A3	Document Number: M9A0_MP	Rev: 1.1
Date: Wednesday, October 28, 2009	Sheet 42 of 73	

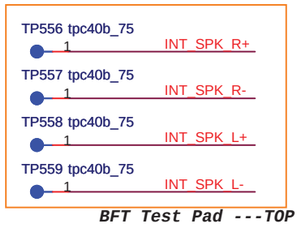


2009.0925
ADD for EMI request



INTERNAL SPEAKER

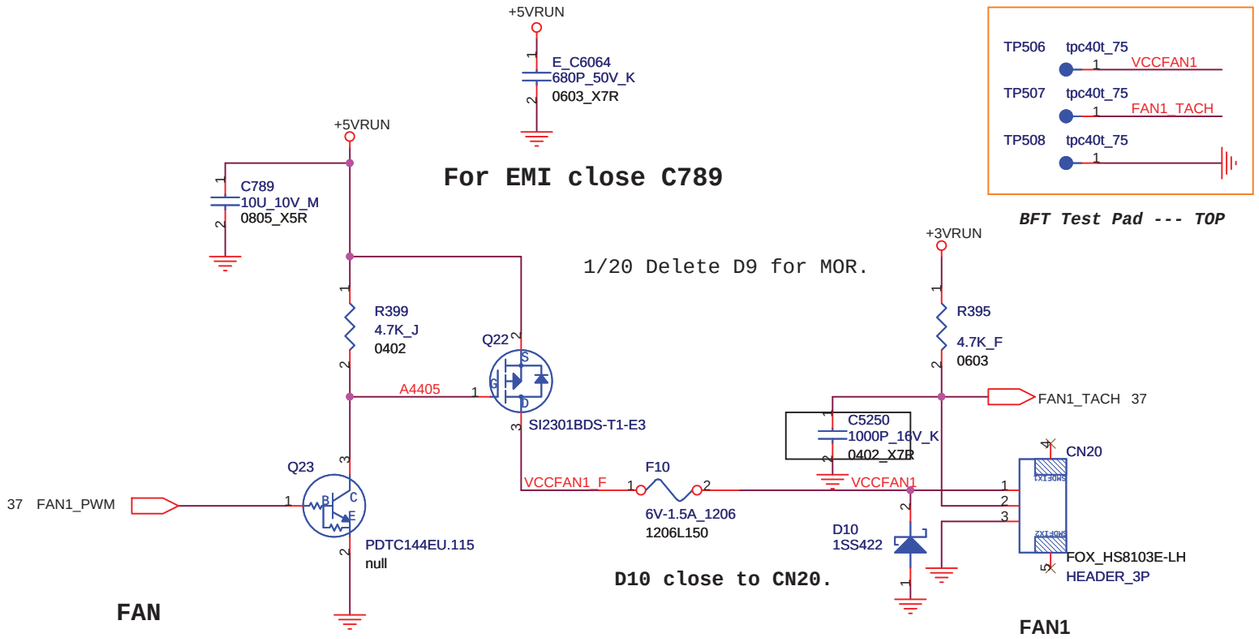




BFT Test Pad ---TOP

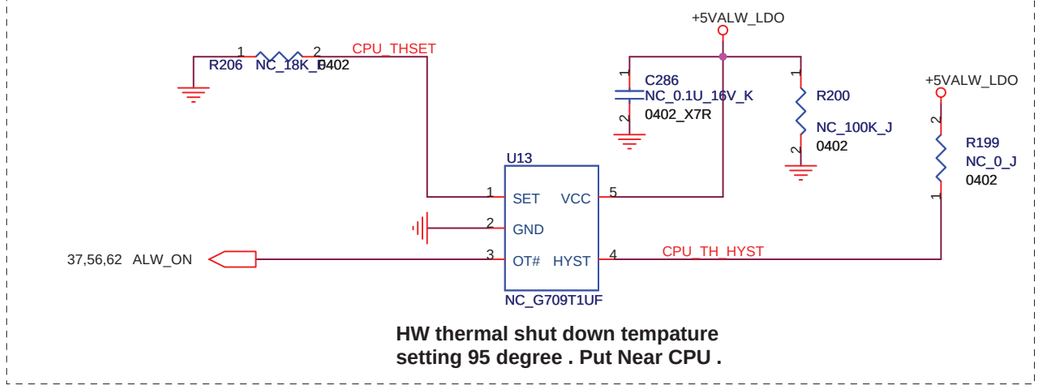
Audio & USB WTB CONN.

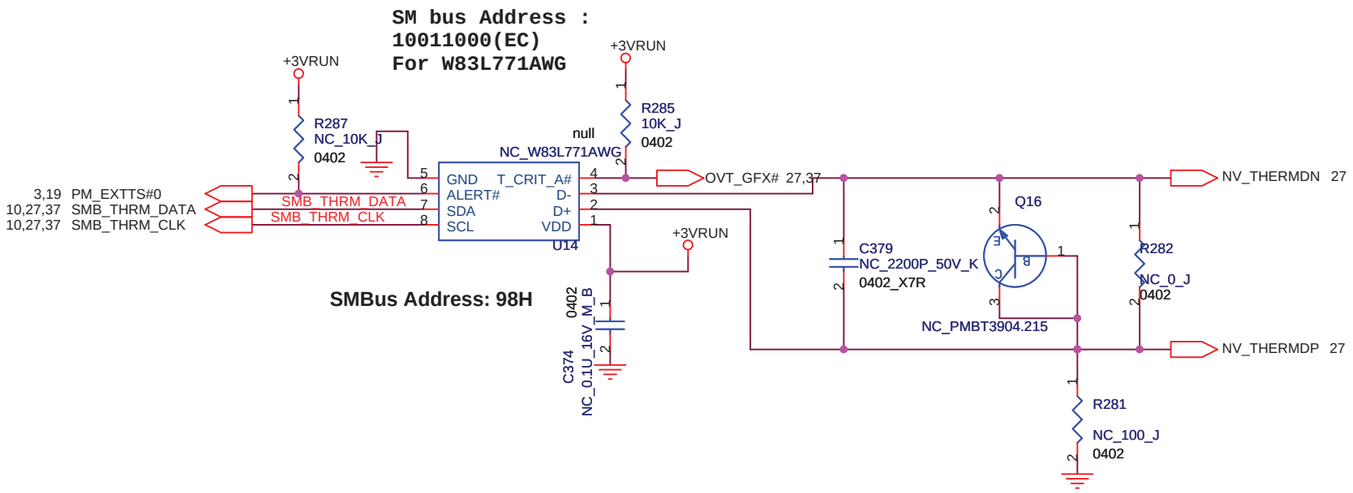
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title: **BTB CONN**		
Size: A3	Document Number: **M9A0_MP**	Rev: **1.1**
Date: Wednesday, November 04, 2009	Sheet 43 of 73	



2009.10.19
change C5250 from 1C-2B20473-K300 to
1C-2B20102-K001 for PVT

7/8 [DVT] Dummy the HW Thermal Protection for C/D.





FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	FAN/Thermal	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 44 of 73	

01/20 Add pin headers and resistors for PCIe protocol measurement for R5U231.

Delete parts for R5U231 protocol measurement.

C496 22P_50V_J 0402_NPO
C497 27P_50V_J_N 0402
Y3 24.576MHZ_16P_30PPM ITTI_L5030-24.576-16
XOUT_R
R605 0_J 0402
R604 NC_10M_J 0402
XIN
XOUT

MFIO14 R5691 0_J 0402 MS_CLK

MS_BS MS_DATA1 MS_DATA5 MS_DATA0 MS_DATA4 MS_DATA2 MS_DATA6 MS_DATA3 MS_DATA7 MS_CD#

U21

XIN XOUT
TPA0+ TPA0- TPBIAS0 TPB0+ TPB0-
CLK_PCIE_CARD CLK_PCIE_CARD#
CARD_RXP2 CARD_RXN2
CARD_TXP2 CARD_TXN2
13,21,38,39,41 PLT_RST#
SDBCMD SDBCLK SDBDAT3 SDBDAT2 SDBDAT1 SDBDAT0 SDBPWR SDBCD# SDBWP
UDIO0 UDIO1 UDIO2 UDIO3 UDIO4 TEST

R5U231
null

+3VRUN
C1963 0.1U_10V_K 0402_X7R
C1964 0.1U_10V_K 0402_X7R
C1965 0.1U_10V_K 0402_X7R
C1966 0.1U_10V_K 0402_X7R
C1967 0.1U_10V_K 0402_X7R
C1968 0.1U_10V_K 0402_X7R
C1969 10U_6.3V_M 0805_X5R
C1970 0.1U_16V_Y
C1973 0.1U_16V_Y
C1971 0.1U_10V_K 0402_X7R
C1972 1U_10V_K 0402_X5R
C1974 0.1U_10V_K 0402_X7R
SDMSXD_VCC
VCC_CTRL_SD
R5991 100K_J 0402
C488 0.01U_10V_K 0402_X7R
C489 1U_10V_K 0402_X5R
C476 NC_12P_50V_K_N 0402
C1976 0.022U_16V_M 0402_X7R
C1977 0402_X7R
C1975 1500P_25V_K
R5366 5.1K_F 0402

Close to U21

MS_DATA7R5700 33_F 0402 DATA7_M
MS_DATA6R5706 33_F 0402 DATA6_M
MS_DATA4R5699 33_F 0402 DATA4_M
MS_DATA5R5701 33_F 0402 DATA5_M
MS_DATA3R5707 33_F 0402 DATA3_M
MS_DATA2R5705 33_F 0402 DATA2_M
MS_DATA0R5704 33_F 0402 DATA0_M
MS_DATA1R5702 33_F 0402 DATA1_M
MS_BS R5703 75_F 0402 BS_M
MS_CD#

CN35 SOCKET_14P
YAMAICHI_JES014-2000-1

2009.0921
ADD R5991 follow design guide
change C476 TO NC_12P

2009.10.19
change R5703 from 68ohm to 75ohm for PVT

+3VRUN R818 4.7K_J 0402 MS_CD#
C864 1000P_50V_K 0402_X7R

2009/09/10
Add test point for for L6 TE request

TP512 TP513 TP514 TP515 tpc40b_75 TPB- TPB+ TPA- TPA+

BFT TEST PAD _BOT

+3VRUN R5369 NC_47K_J 0402 UDIO1 R5372 47K_J 0402

TPBIAS0 C1979 0.33UF_10V_K 0603_X7R
R376 54.9_F 0402
R373 54.9_F 0402
TPB0- TPB0+ TPA0- TPA0+
120R-100MHZ_0R12 6.0x6.5x3.3 L62
R5373 54.9_F 0402
R5374 54.9_F 0402
C505 270P_50V_K 0402_NPO
R379 5.1K_F 0402

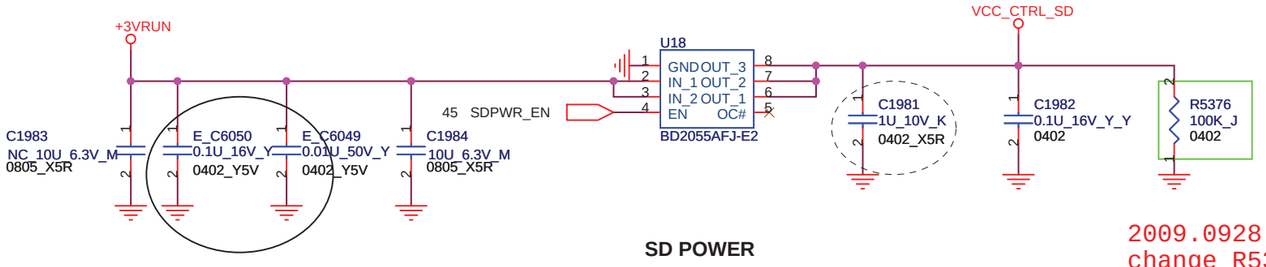
CN11 IEEE 1394 AV CONN_4P FOX_UV31413-WU82P-7H

2009.0918
DVT2 CN11 change to Halogen Free

+3VRUN R370 10K_J 0402 R369 10K_J 0402
C493 0.01U_10V_K 0402_X7R
U20 EEPROM_SOP-8_256x8 HT24LC02
R5U231_SCL R5U231_SDA

SROM: UDIO1
Pull-Hi: Disable
Pull-Lo: Enable (Default)

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCIE (PCIE BUS) 1/2	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Thursday, October 29, 2009	Sheet 45 of 73	



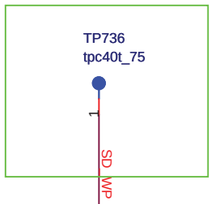
For EMI close C1983

SD POWER

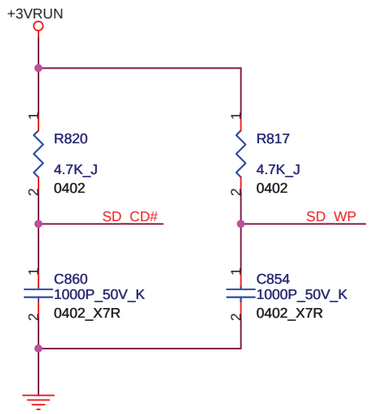
2009.0928
change R5376 to 100K follow design guide

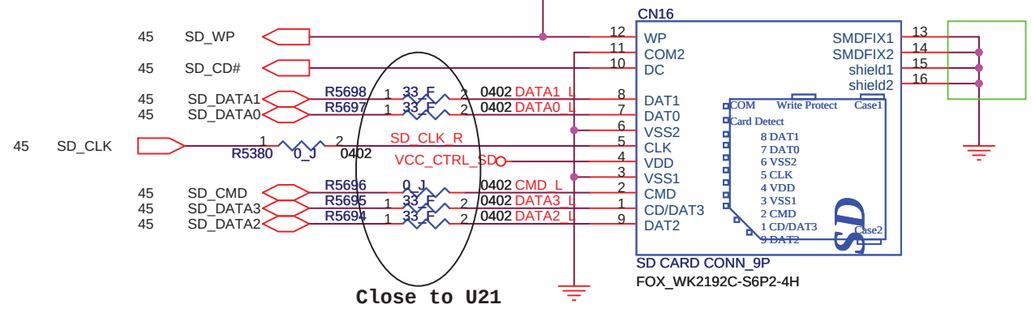
2009/09/10
Add test point for L6 TE request

BFT TEST PAD_ TOP



2009.10.23
change net SD_WP# to SD_WP

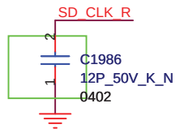




Close to U21

SD CONN.

For EMI

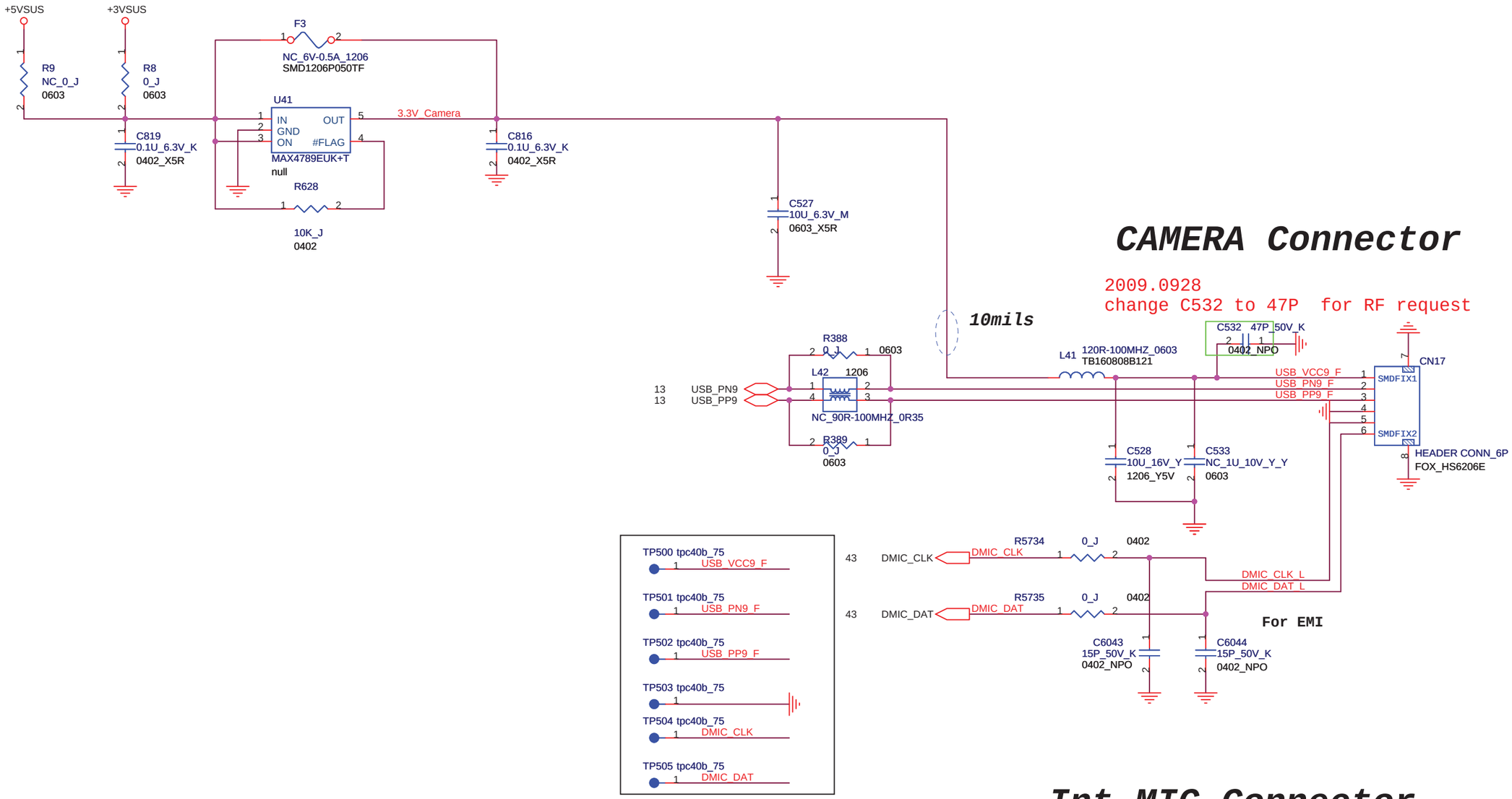


2009.0921
change C1986 to 12p

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: PCIE (MS/SD) 2/2		
Size: A3	Document Number: M9A0_MP	Rev: 1.1
Date: Wednesday, November 04, 2009	Sheet 46 of 73	

CAMERA Connector

2009.0928
change C532 to 47P for RF request



Int MIC Connector

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CAMERA/Int MIC.	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 47 of 73	

2009.0921
change D15,D21from NC to mount
Place them near connector

External USB Port 0

13 USB_PN0
13 USB_PP0
USB_PN0
USB_PP0
R565 1 0_J 2 0603
3.2X1.6X2.0
NC_90R-100M_1206
L61
R566 1 0_J 2 0603
USB_VCC0
CAP16
47U_6.3V_3528
6TPC47MB
C711
470P_50V_K_B
0402
D15
NC1
NC2
RSB12JS2
USB_VD0- F
USB_VD0+ F
CN9
VCC
V-
V+
GND
SMDFIX1
SMDFIX2
USB RECEPTACLE_4P
FOX_UB111M3-CA4S4-7H

External USB Port 1

13 USB_PN1
13 USB_PP1
USB_PN1
USB_PP1
R589 1 0_J 2 0603
3.2X1.6X2.0
NC_90R-100M_1206
L66
R588 1 0_J 2 0603
USB_VCC1
CAP18
47U_6.3V_3528
6TPC47MB
C716
47P_50V_K
0402_NPO
D21
NC1
NC2
RSB12JS2
USB_VD1- F
USB_VD1+ F
CN12
USB RECEPTACLE_4P
FOX_UB111M3-CA4S4-7H

2009.0928
change C716 to 47P for RF request

2009.0918
DVT2 CN9,CN12 change to Halogen Free

37,40,59,61 SUS_ON
+5VALW
F1
6V_2.6A_1812
R5732 1 0_J 2 0805
C381 miniSMDC260F-2
1U_25V_M_B
0603
+5VALW_F
U36
GND OUT_3
IN_1 OUT_2
IN_2 OUT_1
EN(EN#) OC#
G545B1P8U
C710
0402 0.1U_16V_Y_Y
TP552 tpc40t_75
USB_VCC0
USB_OC#0
USB_OC#0 13

C712
0402 0.1U_16V_Y_Y
TP555 tpc40t_75
U44
GND OUT_3
IN_1 OUT_2
IN_2 OUT_1
EN(EN#) OC#
G545B1P8U
USB_VCC1
USB_OC#1
USB_OC#1 13
C725

2009/09/19
Change USB_OC#0 to USB_OC#1

+5VALW
F11
6V_2.6A_1812
C6005 miniSMDC260F-2
1U_25V_M_B
0603
0402 0.1U_16V_Y_Y
TP554 tpc40t_75
U46
GND OUT_3
IN_1 OUT_2
IN_2 OUT_1
EN(EN#) OC#
G545B1P8U
USB_VCC4
USB_VCC4 43
USB_OC#2
USB_OC#2 13

2009/09/19
Change USB_VCC2 to USB_VCC4

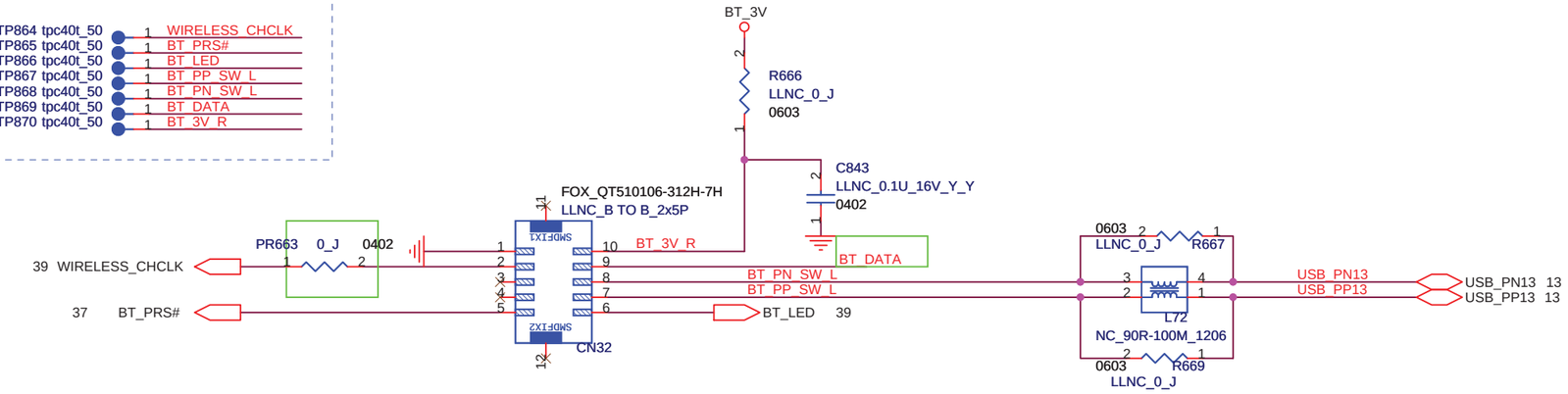
+5VALW
C809
0.1U_16V_Y
0402_Y5V
+5VALW_F
C807
0.1U_16V_Y
0402_Y5V
C808
0.1U_16V_Y
0402_Y5V
+5VALW
C818
0.1U_16V_Y
0402_Y5V

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	USB2.0	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Thursday, October 29, 2009	Sheet 48 of 73	

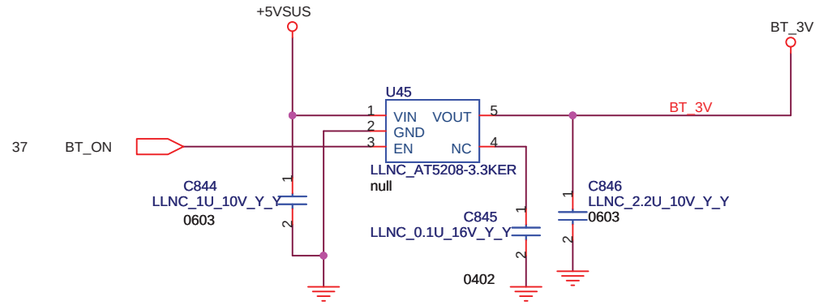
Bluetooth connector

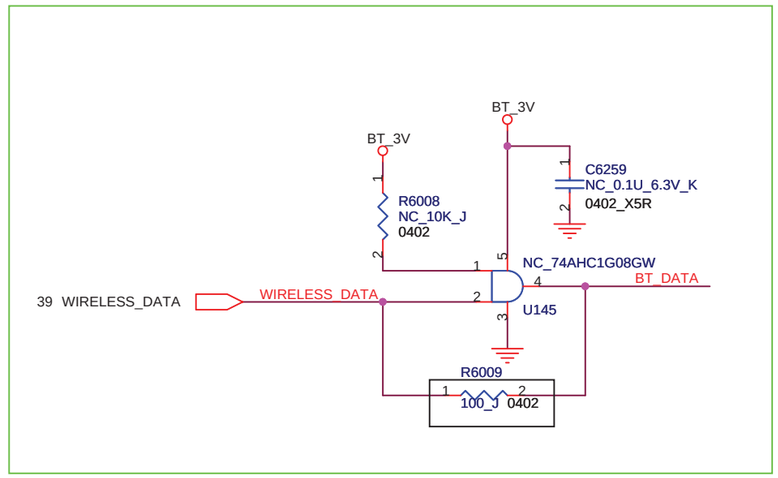
BOT Side PVT

TP864 tpc40t_50 1 WIRELESS_CHCLK
TP865 tpc40t_50 1 BT_PRS#
TP866 tpc40t_50 1 BT_LED
TP867 tpc40t_50 1 BT_PP_SW_L
TP868 tpc40t_50 1 BT_PN_SW_L
TP869 tpc40t_50 1 BT_DATA
TP870 tpc40t_50 1 BT_3V_R



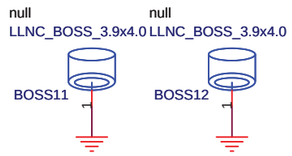
2009.0921
WIRELESS_DATA/WIRELESS_CHCLK follow M930





2009.11.19
Change R6009 from 1R-0000000-J200 to 1R-0000101-J200 for RF request

Bluetooth

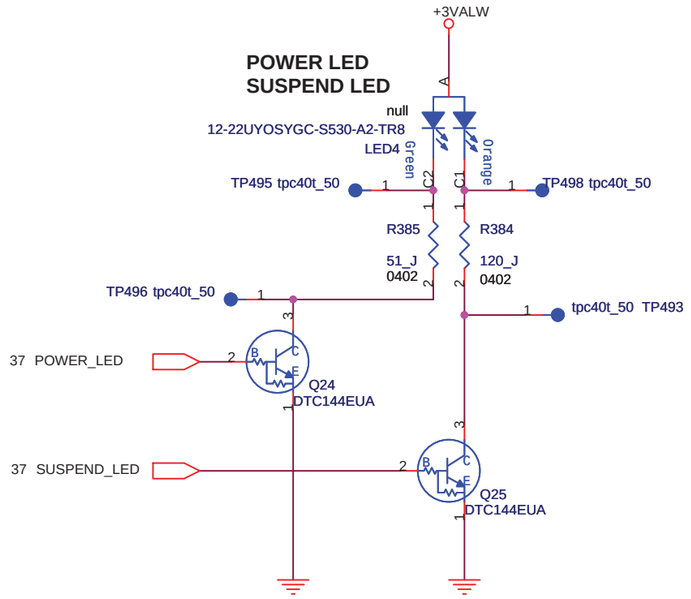


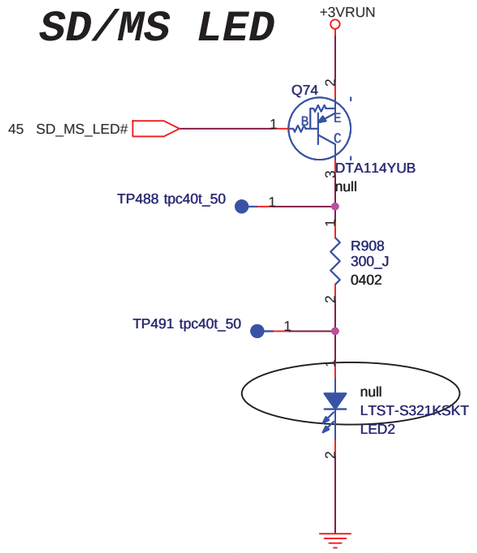
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

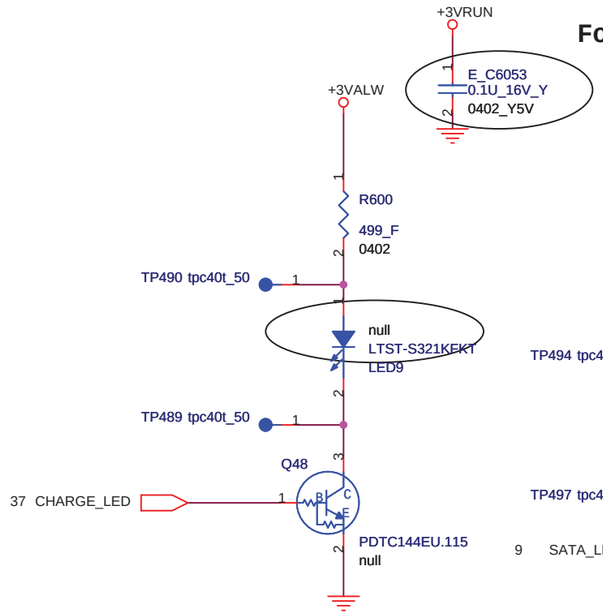
Title: **Bluetooth**

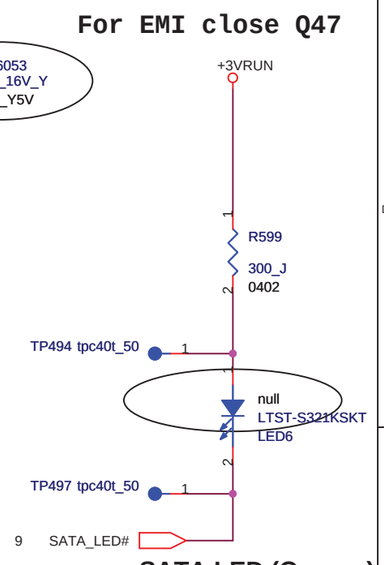
Size	Document Number	Rev
A3	M9A0_MP	1.1

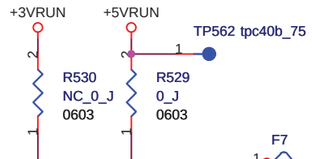
Date: Thursday, November 19, 2009 Sheet 49 of 73



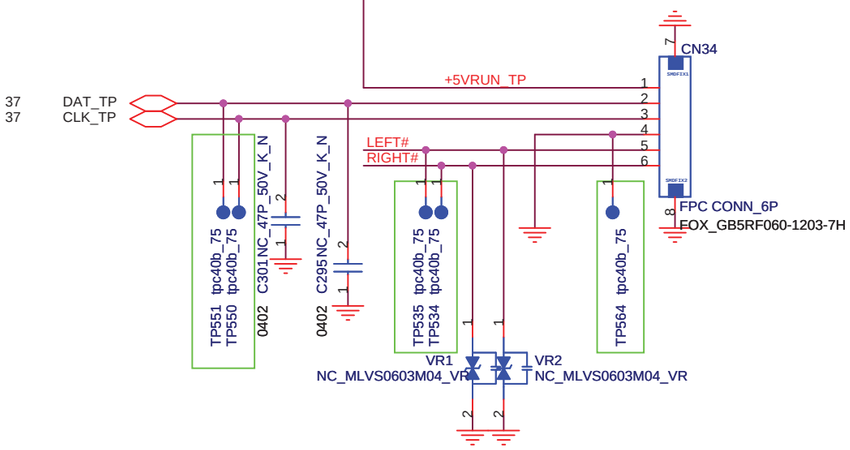


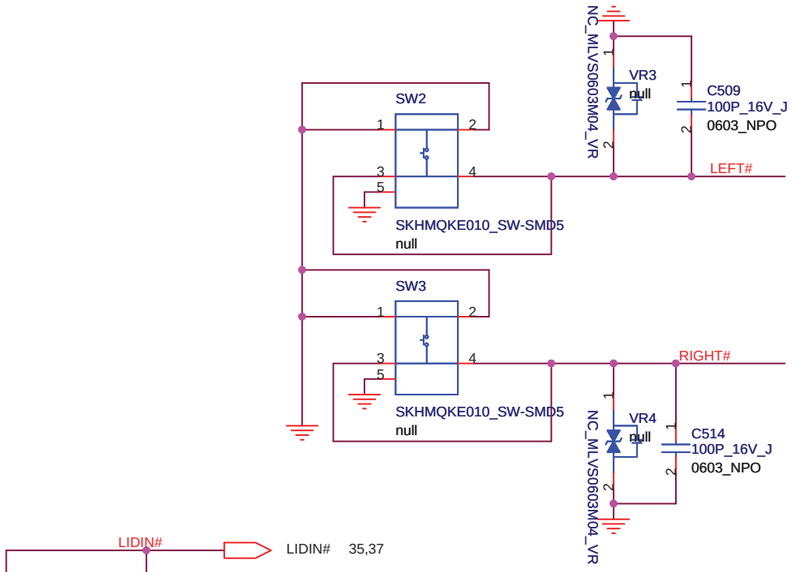


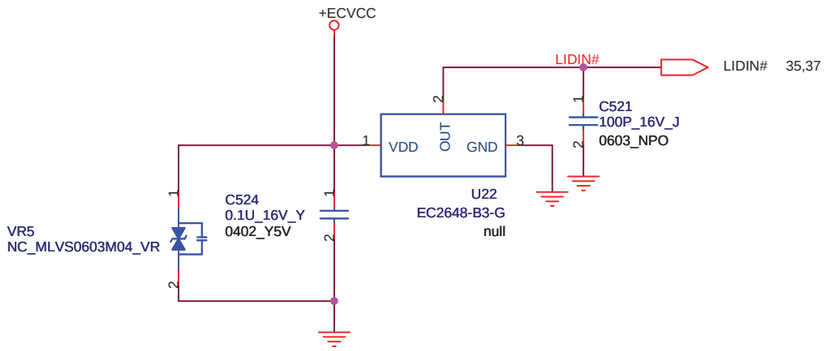




2009.0918
DVT2 CN34 change to Halogen Free

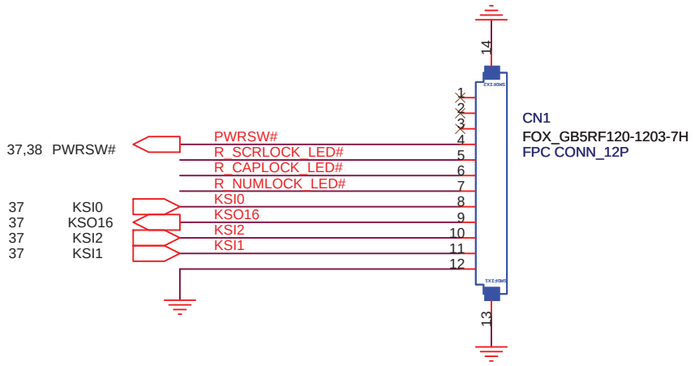


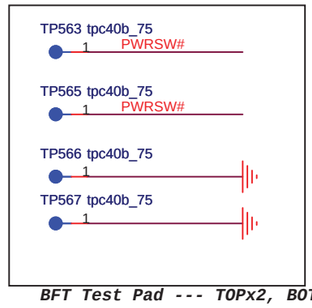




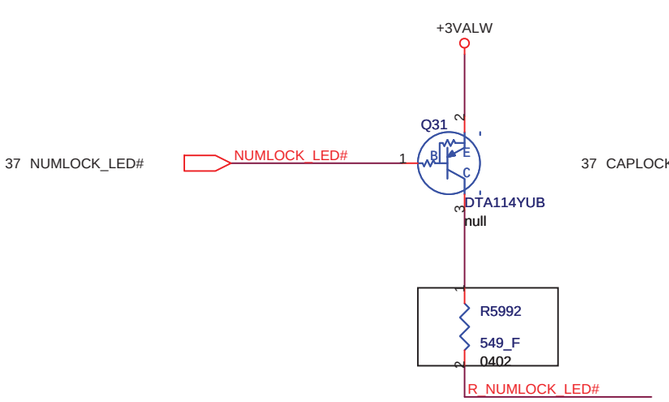
2009/09/10
Add test point for L6 TE request

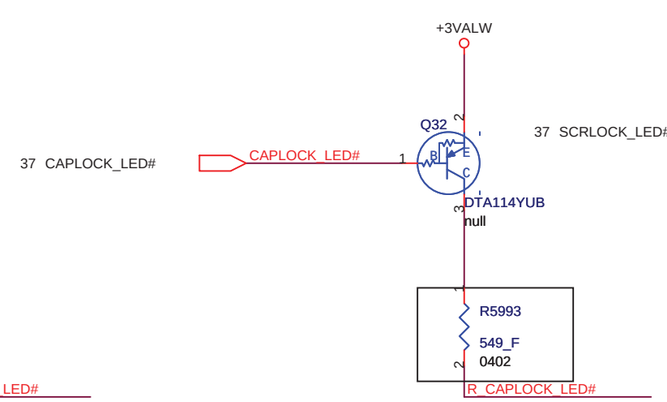
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LED & T/P & LID	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 50 of 73	

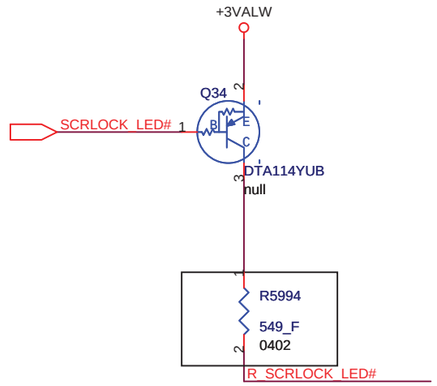




BFT Test Pad --- T0Px2, B0Tx2







2009.10.30
change R5992,R5993,R5994 from 120ohm to 549ohm follow M870

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**Power Board MB CONN**	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, November 04, 2009	Sheet 51 of 73	

Adaptor
19.5V / 90W

DCBATOUT

TI
bq24753A
Battery Charger
Switch Mode
PAGE 55

ENCHG#

Battery
Li-ion
11.1V
4800mAH

TI
SN0608098RHBR
Switch Mode
FOR System
PAGE 55

ALW_ON
EN1
EN2
LDO5
PGOOD
+5VALW_LDO
ALW_PWRGD

System
+5VALW/5A
SUS_ON
N-Channel transistor
+5VSUS/0.6A
RUN_ON
N-Channel transistor
+5VRUN/4.5A

System
+3VALW/5A
SUS_ON
N-Channel transistor
+3VSUS/2A
RUN_ON
N-Channel transistor
+3VRUN/3A

+12V/10mA
+5VALW_LDO
AT5208-3.3KER
LDO
+ECVCC/100mA

DCBATOUT

TI
TPS51218
Switch Mode
FOR DDR3
PAGE 59

SUS_ON
EN
PGOOD
SUS_PWRGD

+1_5VSUS/11A
N-Channel transistor
+1_5VRUN/4A
RUN_ON1

G2998
LDO
0.75VRUN/2A
DDRDIMM_VREF
RUN_ON1

OZ8033
LDO
PEX_VDD/700mA
RUN_ON1

DCBATOUT

TI
TPS51218DSCR
Switch Mode
FOR VTT=>+1_05V_VTT
PAGE 58

RUN_ON1
EN
PGOOD
RUN_PWRGD

+1_05V_VTT/19A

DCBATOUT

TI
TPS51218DSCR
Switch Mode
FOR VRAM
PAGE 60

RUN_ON1
EN/PSV
PGOOD

+1_8VRUN/8A

DCBATOUT

MAXIM
MAX17030
Switch Mode
FOR CPU Core
PAGE 53

IMVP_VR_ON
VR_ON
CLK_EN#
IMVP_OK

EC_CLK_EN#
IMVP_OK

VHCORE/40A

DCBATOUT

TI
TPS51217
Switch Mode
FOR VGA
PAGE 57

RUN_ON1
EN/PSV
PGOOD

NV_VDD/14A

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	Power Design Diagram	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, September 23, 2009	Sheet 52 of 73	

2009.10.22
change PC112 from 68U to 47U for power request

2009.0929
Add PC206 NC_0.1U reserve for Return patch

IMVP_PWRGD_PWM 1 TP891 tpc40t_50

IMVP_VR_ON 1 TP820 tpc40b_50

PU21

5,54 VID0 — D0 32
5,54 VID1 — D1 33
5,54 VID2 — D2 34
5,54 VID3 — D3 35
5,54 VID4 — D4 36
5,54 VID5 — D5 37
5,54 VID6 — D6 38
37 IMVP_VR_ON — PR304 0_J 0402 — 17036_SHDN# — SHDN# 13
5,54 PM_DPRSLPVR — DPRSLPVR 14
+3VRUN — PR307 10K_J 0402 — 17036_PGD_IN — PGD_IN 31
5,54 PSI# — PSI# 15

+5VRUN — PR313 10_J 0603 — PC295 2.2U_6.3V_M 0402_X5R — 17036_VCC — VCC 7 — VDD 26
PC297 1U_6.3V_M 0402_X5R
PR315 133K_F 0402 — 17036_ILIM — ILIM 5
PR316 16.9K_F 0402 — TIME 6
18 IMVP_PWRGD_PWM — IMVP_PWRGD_PWM — PWRGD 18
+3VRUN — PR317 1.8K_F 0402
NC_10K_J PR318 0402 — VRHOT# 25
3 PROCHOT# — PROCHOT# — CLKEN# 17
+3VALW — PR319 1.8K_F 0402
18 CLK_EN# — CLK_EN#

17036_IMON — PC303 0.022U_16V_K 0402_X7R — PR320 1.8K_F 0402 — 17036_IMONA — IMON 4
VSSSENSE — PR323 12K_F 0402
+5VRUN — PR324 8.45K_F 0402 — 17036_THRM — THRM 3
PR328 ERTJ0EV104J null

TON 16 — 17036_TON — PR295 200K_F 0402
BST1 30 — 17036_BOOT1 — PR297 0_J 0603 — 17036_BOOT1R
DH1 28 — 17036_UGATE1 — PR299 0_J 0603 — 17036_UGATE1_R
LX1 29 — 17036_PHASE1
DL1 27 — 17036_LGATE1
CSP1 39 — 17036_CSP1 — PC292 NC_1000P_16V_K 0402_X7R
CSN1 40 — PC293 NC_1000P_16V_K 0402_X7R
BST2 21 — 17036_BOOT2 — PR311 0_J 0603 — 17036_BOOT2R
DH2 23 — 17036_UGATE2 — PR314 0_J 0603 — 17036_UGATE2_R
LX2 22 — 17036_PHASE2
DL2 24 — 17036_LGATE2
CSP2 12 — 17036_CSP2 — PC298 NC_1000P_16V_K 0402_X7R
CSN2 11 — PC302 NC_1000P_16V_K 0402_X7R
PWM3 20 — TP822 tpc40b_50
DRVSKP# 19 — TP823 tpc40b_50 — PR321 1K_J 0402
CSP3 2 — M8791_CSP3 — PC304 NC_1000P_16V_K 0402_X7R — +5VRUN
CSN3 1 — TP824 tpc40b_50
FBAC 9 — 17030_FBAC — PR327 0_J 0402 — PR325 6.34K_F 0402
FB 8 — 17030_FB — PR331 NC_0_J 0402
GNDS 10
PGND 41
MAX17030GTL+ null

PC286 0.22U_25V_K 0603_X5R
PC291 NC_4700P_25V_K 0402_X7R
PC296 0.22U_25V_K 0603_X5R
PC310 1000P_16V_K 0402_X7R
PC311 NC_1000P_16V_K 0402_X7R
PC312 NC_1000P_16V_K 0402_X7R
PR334 0402 10_J
PR335 0_J 0402

VCCSENSE 5
VSSSENSE 5
Sense line are 18mil wide

Place these CAPS close to FETs

PQ59 SIR428DP-T1-GE3 null
PQ60 SIR158DP-T1-GE3 null

PC283 10U_25V_M 1206_X5R
PC284 10U_25V_M 1206_X5R
PC285 NC_0.1U_25V_M 0603_X5R
PC112 +47U_25V_6.3X5.9 25SVPF47M
PC206 NC_0.1U_25V_M 0603_X5R

4A
DCBATOUT

PL16 0.36UH_28A_0.00076R ETQP4LR36AFC

PR303 2.21K_F 0402
PR305 NC_3.9K_F 0402
PR308 4.02K_F 0402
PR309 ERTJ1VR103J
PR312 2.2_F 0603
PC294 0.22U_25V_K 0603_X5R

PC288 330U_2V_7.3x4.3 EEFSX0D331XE
PC289 330U_2V_7.3x4.3 EEFSX0D331XE
PC287 330U_2V_7.3x4.3 EEFSX0D331XE
PC290 0.1U_6.3V_K 0402_X5R

TP821 tpc40b_50
48A
VHCORE

Place these CAPS close to FETs

4A
DCBATOUT

PQ62 SIR428DP-T1-GE3 null
PQ63 SIR158DP-T1-GE3 null

PC299 10U_25V_M 1206_X5R
PC300 10U_25V_M 1206_X5R
PC301 NC_0.1U_25V_M 0603_X5R

PL17 0.36UH_28A_0.00076R ETQP4LR36AFC

PR322 2.21K_F 0402
PR326 NC_3.9K_F 0402
PR329 4.02K_F 0402
PR330 ERTJ1VR103J
PR332 2.2_F 0603
PC309 0.22U_25V_K 0603_X5R
PC308 NC_4700P_25V_K 0402_X7R

PC305 330U_2V_7.3x4.3 EEFSX0D331XE
PC306 330U_2V_7.3x4.3 EEFSX0D331XE
PC307 0.1U_6.3V_K 0402_X5R

Valley current limit:
V_TIME_LIM = 0.2 x PR561 / (PR560 + PR561) = 20.2mV
I_LIM = V_TIME_LIM / Rcs = 19A

Rcs:
DCR = 0.8mohm
Rcs = DCR x (PR557 + PR185) / (PR557 + PR185 + PR555) = 0.709mohm

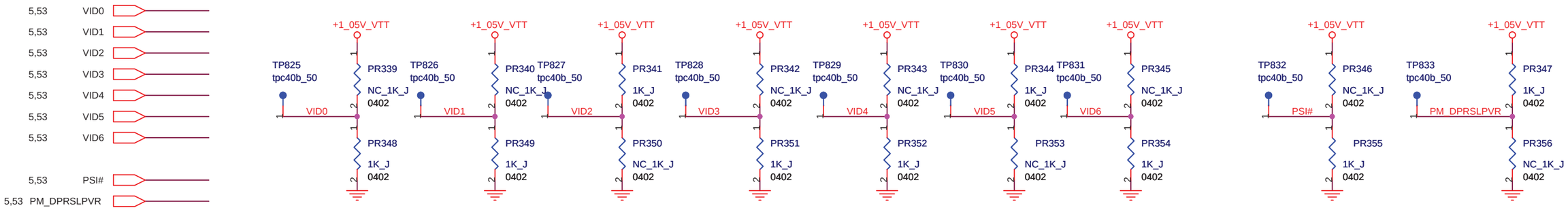
Load-Line R_FBAC: Loadl-Line=-1.9mV/A
Rcs = 0.709mohm
PR598 = (1.9mV/A) / (Rcs x 400us) = 6.34K

17036_IMON — PR336 0_J 0402 — IMVP_IMON 5
IMVP_PWRGD_PWM — PR337 NC_0_J 0402 — IMVP_PWRGD 11,37
PR338 0_J 0402 — IMVP_OK 37

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	CPU Power_VHCORE		
Size A3	Document Number M9A0_MP		Rev 1.1
Date: Wednesday, November 04, 2009	Sheet 53 of 73		

Default value of VID [6:0] = [0100100] , PSI = 0 , PROC_DPRSLPVR = 1

Market Segment Selection MSID[2:0] = [100] (SV)
- 416056_416056_Ard_EDS_Rev.1.1 - 403779_Clarksfield_MPG_Rev1.5



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	***CPU Power_VID***	
Size A3	Document Number ***M9A0_MP***	Rev ***1.1***
Date: Tuesday, November 03, 2009	Sheet 54 of 73	

For BFT Test (2 Top, 2 Bottom)

C_TP446 tpc40t_50
C_TP447 tpc40t_50
C_TP448 tpc40t_50
C_TP449 tpc40t_50
P+

C_PL7 60R-100MHZ_1806 BCMS451616A600 8A
C_PL8 60R-100MHZ_1806 BCMS451616A600 8A

DC_IN_1
DC_IN
7A
C_TP1 tpc40t_50
Co-layout

C_PQ26 NC_TPCC8102 null
C_PQ24 Si7121DN-T1-GE3 null
DC_IN_MOS

C_PR292 2.2_F 0805
C_PQ25 Si7121DN-T1-GE3 null
DC_IN_R
C_PR9 0.01_1W_F 1608
C_PQ27 NC_TPCC8102 null

ACP and ACN connections must be make using Kelvin-sense connections

DCBATOUT
C_PC1 1U_25V_M_B 0603
C_PC2 0.1U_50V_K 0603_X7R
C_PC33 680P_50V_K 0603_X7R
C_PC156 1000P_50V_M 0603_X7R
C_PR31 100K_F 0402

C_TP155 tpc40t_50
C_PQ9 NC_TPCC8102 null
C_PQ5 Si7121DN-T1-GE3 null
C_TP158 tpc40t_50
BT+
Co-layout

BATT_ID 61
DAT_SMB 37
CLK_SMB 37
BATT_PRS# 37
SYS_PRS# 62

C_PF1 0437007WR 32V-7A_1206
C_PC14 1000P_50V_M 0603_X7R
C_PC13 0.1U_50V_K 0603_X7R
C_PR32 2_F 1210
C_PR165 2_F 1210
C_PC134 1000P_50V_M 0603_X7R
C_PC135 0.1U_50V_K 0603_X7R
C_PCN2
P+
FOX_GS73041-10272-7H POWER BOARD SIDE_4P

C_TP450 tpc40t_50
C_TP451 tpc40t_50
C_TP452 tpc40t_50
C_TP453 tpc40t_50
For BFT Test (2 Top, 2 Bottom)

C_PR28 432K_F 0402
C_PR166 432K_F 0402
C_PR27 69.8K_F 0402
C_PR15 69.8K_F 0402
C_PC279 4.7U_50V_k 1206_X7R
C_PC29 4.7U_50V_k 1206_X7R

C_PR164 10K_F 0402
C_PC136 0.1U_50V_K 0603_X7R
C_PC25 0.1U_50V_K 0603_X7R
C_PC18 0.1U_25V_M 0603_X5R
C_PC16 0.1U_50V_K 0603_X7R
C_PC10 1U_25V_M_B 0603
DC_IN_G1
ACDRV#

DCBATOUT
C_EC6066 0.1U_50V_K_B 0603

10A

For EMI close C_PQ1 2A DCBATOUT

C_TP258 tpc40t_50
CHARGE_CTRL
C_TP298 tpc40t_50
ENCHG#
62 AC_OFF_3#
AC_OFF_3#
CH520S-30PT
C_PD6

C_PU1
ACN
ACP
ACDRV#
ACDET
AGND
ACGOOD#
OVPSET
SRSET
ACSET
VREF
LEARN
CELLS
CHGEN#
VDAC
VADJ
IADAPT
BQ24753ARHDR
null

PVCC
BATDRV#
HIDRV
PH
BTST
REGN
LODRV
PGND
SRP
SRN
BAT
ACOP
POWERPAD

PVCC
BATDRV#
C_PR136 0_J 0603
HIDRV_R
SI3424BDV-T1-E3
C_PQ1
C_PC132 10U_25V_K 1206_X5R
C_PC133 0.1U_50V_K 0603_X7R
C_PC3 0.1U_50V_K 0603_X7R

C_PL17 PCMB063T-100MS 10UH_4A_0.068R
BQ24751_PH
BT+_1
C_PC4 0.1U_50V_K_B 0603
C_PD1 CH500H-40PT
VREGN
C_PQ2 SI3424BDV-T1-E3
C_PR241 NC_4.7_J 0603
C_PC27 10U_25V_K 1206_X5R
C_PC21 10U_25V_K 1206_X5R
C_PC280 NC_680P_50V_K 0603_X7R
C_PC19 0.1U_25V_M 0603_X5R
C_PR14 0.02_F 1206
C_PC22 0.1U_25V_M 0603_X5R
C_PC24 0.1U_25V_M 0603_X5R
C_PC23 680P_50V_K 0603_X7R
C_PC17 10U_25V_K 1206_X5R

2A

C_PD3 PESD5V2S2UT
null TVS2315PT
C_PL4 NC_60R-100MHZ_1806 BCMS451616A600 8A
C_PD4
C_PL3 60R-100MHZ_1806 BCMS451616A600 8A
C_PCN1
BT+_L
BATT_ID
DAT_SMB
CLK_SMB
BATT_PRS#_1
SYS_PRS#_1
C_PR3 330_J 0402
C_PR5 330_J 0402
C_TP160 tpc40t_50
+ECVCC
C_PR4 10K_J 0402
C_PD2 PESD5V2S2UT
BATTERY CONN_7P FOX_BP91071-B62E3-7H

Battery CONN.

C_PC26 0.1U_25V_M 0603_X5R

SRP and SRN connections must be make using Kelvin-sense connections

C_TP161 C_TP176 C_TP177 C_TP178 C_TP179 C_TP180 tpc40t_50
BT+_L
DAT_SMB
CLK_SMB
BATT_PRS#_1
SYS_PRS#_1
BATT_ID
C_PC5 C_PC9 C_PC8 C_PC6 C_PC7 47P_50V_J 0402_NPO
C_PC20 0.1U_50V_K 0603_X7R

+ECVCC
C_PR33 10K_J 0402
C_PR22 10K_J 0402
+5VALW_LDO
ACIN_EC
C_PQ8 2N7002W null
ACGOOD#

CHARGE_CTRL
C_PR18 750K_F 0402
C_PR17 360K_F 0402
C_PR16 NC_226K_F 0402
C_PR19 20K_F 0402
ACSET
C_TP454 tpc40t_50
C_PR26 27.4K_F 0402
BQ24753A_VREF
C_PC31 1U_6.3V_M 0402_X5R
AC_OFF
C_PR8 0_J 0402
AC_OFF_R

+ECVCC
C_PR210K_J 0402
C_PR7 10K_J 0402
BQ24753A_VREF
C_PR6 10K_J 0402
C_PQ3 2N7002W
ENCHG#
ENCHG#_1

BQ24753A_IADAPT
C_PR12 null 0_J 0402
BQ24753A_IADAPT_1
C_PC30 120P_50V_J 0402_NPO
EC_IADAPT
C_PR35 0_J 0402
C_PR23 210K_F 0402
C_PR24 100K_F 0402
C_PR25 NC_0_J 0402
C_PC11 1U_10V_K 0603_X5R
C_PC32 0603_X5R 0.47U_16V_K

DCBATOUT
C_PR36 120K_F 0402
EC_VADAPT
C_PR37 20K_F 0402

charge current set table:

charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
0.8A	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF

VREF=3.3V->VDAC
Vbat=cell count*[4V+0.512*(Vadj/Vvadc)]=12.465V
(Vbat=4.2V when Vadj connected to REGN)
Icharge=(Vsrset/Vvdac)*(0.1/PR15)=1.5A
Iadapter=(Vacset/Vvdac)*(0.1/PR657)=4.22A
IADAPT=(Vacp - Vacn)*20
Input OCP: (VACP-VACN)max/PR4=100mV/10mohm=10A
Input OVP : 22.2V
Input UVP : 17V
Battery OCP : Icharge*145%
Battery OVP : Vbat*104%
Pre-charge : <2.9V/cell ===> Icharge/8
Battery OTP : Tshut=155 degree
Fsw : 300KHz
Time that input current limit :
t=(Cacop*2)/(18uA/V*V(PVCC-ACP))=0.48s

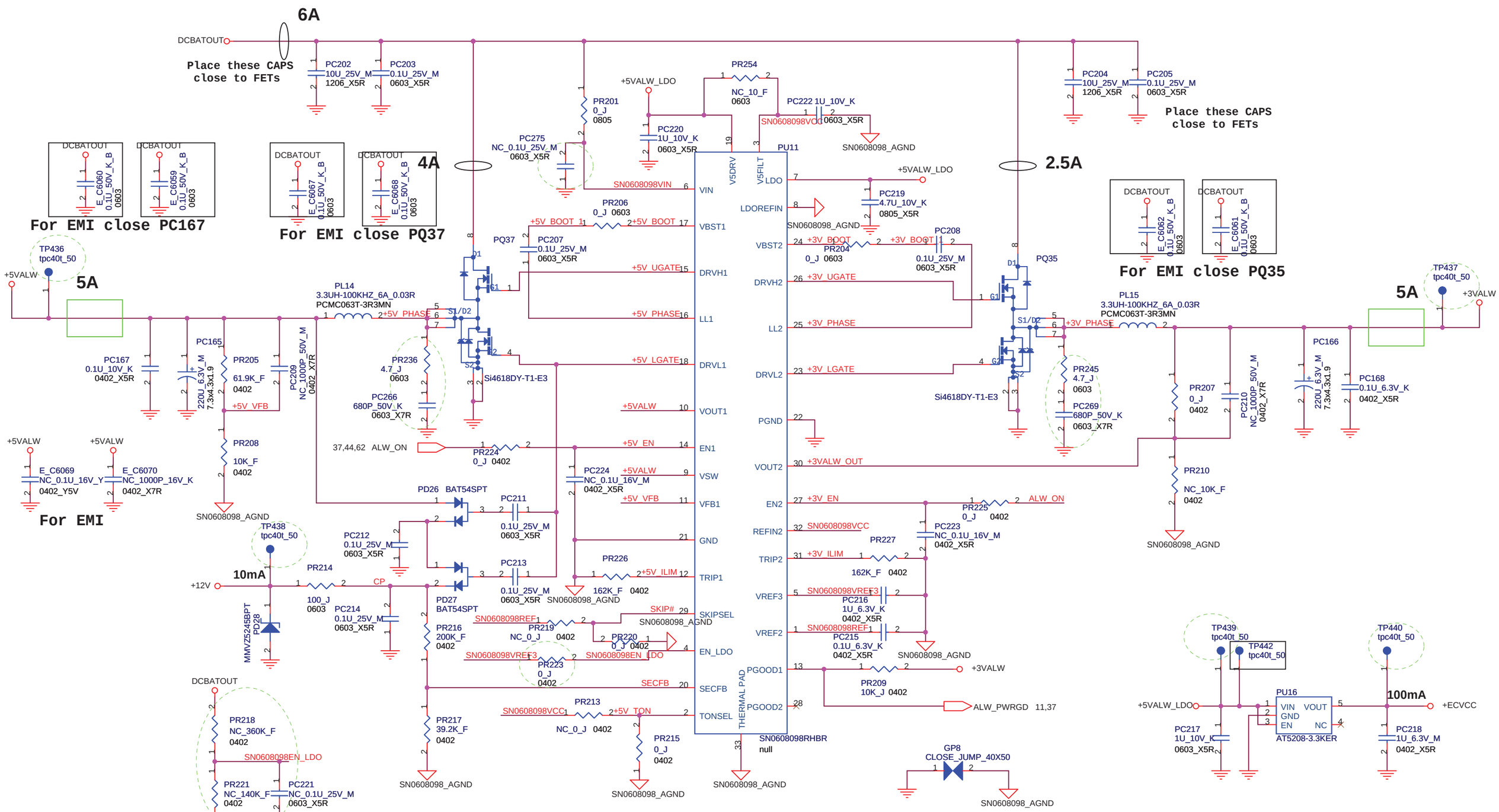
ENCHG# : Enable ==> L
Disable ==> H

ACGOOD# : Vacdet > 2.4V ==> L
Vacdet < 2.4V ==> H

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: DCIN&Charger
Size: A3
Document Number: M9A0_MP
Rev: 1.1
Date: Saturday, November 21, 2009
Sheet 55 of 73



TON	Operating Frequence (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF(OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

L=VOUT(VIN-VOUT)/(VIN*f*LIR*ILOAD(MAX))
Rocp=(Iocp-Iripple/2)*(10*Rds(on))/5u
+5VALW=((PR205/PR208)+1)*VFB1

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	SYS Power (+3_3V/+5V)	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, November 04, 2009	Sheet 56 of 73	

7/29 [DVT] Change PR176 to 1Kohm.

7/8 [DVT] PWM setting adjustment

3A

DCBATOUT

Place these CAPS close to FETs

PC325 0.1U_50V_K_B 0603
PC326 10U_25V_M_B 1206
PC327 10U_25V_M_B 1206

PQ78 SIR474DP-T1-GE3 null

TP856 tpc40b_50

14A

NV_VDD

3,11,37,58,59 RUN_PWRGD

PR372 NC_0_J 0402

TP854 tpc40t_50

+3VRUN

PC324 0402_X5R NC_0.1U_16V_M

PR370 NC_1K_J 0402

PU24

TPS51217DSCR null

PGOOD VBST
TRIP DRVH
EN SW
VFB V5IN
TRAN DRVL
GND

VGA_BST
VGA_DH
VGA_LX
VGA_FB
VGA_EN
VGA_DL
VGA_VOUT_R

PR371 2.2_J 0603
PC328 0.1U_50V_K_B 0603
PR373 0_J 0603
VGA_DH1

+5VSUS

1.0UH_11.5x10.4 PCMC104T-1R0MN PL21

PR375 4.7_J 0603
PC336 680P_50V_K 0603_X7R

PQ79 SI7170DP-T1-GE3 null

PC331 0.1U_6.3V_K 0402_X5R
PC332 330U_2.5V_K 3.5x2.8x1.9
PC333 330U_2.5V_K 3.5x2.8x1.9
PC350 NC_330U_2.5V_K 3.5x2.8x1.9

37,58,59,60,61 RUN_ON1

PR376 100_J 0402
PR374 NC_820K_F 0402

PC335 NC_0.1U_10V_K 0402_X5R

PR378 56K_F 0402

PC330 1U_6.3V_M 0402

PR377 12K_F 0402
PC334 220P_16V_J 0402_NPO

PR380 35.7K_F 0402

7/8 [DVT] OCP setting adjustment

PR379 1K_J 0402

PC337 22P_50V_J 0402_NPO
PWRCNTL_1_R

PC338 47P_50V_K 0402_NPO
PWRCNTL_0_R

7/8 [DVT] PWM setting adjustment

PR381 100_J 0402

PR382 0_J 0402

Sense line are 18mil wide

NV_VDD_SENSE 21

Imax = 15A
OCP = 20A
Fsw = 400KHz
Skip Mode
Vo=(1+(PR550/(PR551//PR210)))*0.6
OVP => VFB * 120%
UVP => VFB * 70%

VDD
PEX_VDD can ramp up any time
PEX_VDD
tNVVDD
NVVDD
tNV-FB
tFBVDDQ
FBVDDQ

Recommended Power sequencing order

+3VRUN

PR383 NM_31.6K_F 0402
PR384 NP_147K_F 0402

PR385 NP_0_J 0402
PR386 NM_110K_F 0402

PR387 NC_10K_J 0402
PR388 NC_10K_J 0402

PR389 110_F 0402
PR390 110_F 0402

27 PWRCNTL_0
27 PWRCNTL_1

PWRCNTL_0_R
PWRCNTL_1_R

PC339 1U_6.3V_M 0402_X5R
PC340 1U_6.3V_M 0402_X5R

PQ80 ME2N7002E
PQ81 ME2N7002E

PWRCNTL_0_R TP857 tpc40b_50
PWRCNTL_1_R TP858 tpc40b_50

[DVT] Add the TP221/TP248

[DVT] PR222, PR229 Feedback Loop Adjustment

+1_5VSUS

PC341 10U_6.3V_M 0805_X5R

+5VSUS

PR391 1K_F 0402
PC342 1U_10V_K 0603_X5R

PU25 OZ8033 null

VIN_1 VOUT2
VDDA VOUT1
POK FB
EN GND
VIN_2

PEG_POK
PEG_EN
PEG_FB

RUN_ON1

PR392 100_J 0402

PC346 0.1U_16V_M 0402_X5R

TP859 tpc40b_50

PEX_VDD

2.5A

PR393 3.3K_F 0402
PC343 0.01U_16V_K 0402_X7R

PC344 22U_6.3V_M 0805_X5R
PC345 22U_6.3V_M 0805_X5R

PR394 10K_F 0402

Vo=(1+(PR393/PR394))*0.8=1.05V

Power Control	GPIO
PWRCNTL_0	GPIO5
PWRCNTL_1	GPIO6

N11P-LP1

	PWRCNTL_0	PWRCNTL_1	GPU Voltage
Battery	0	0	0.8V
Balance	0	1	0.85V
Performance	0	1	0.85V

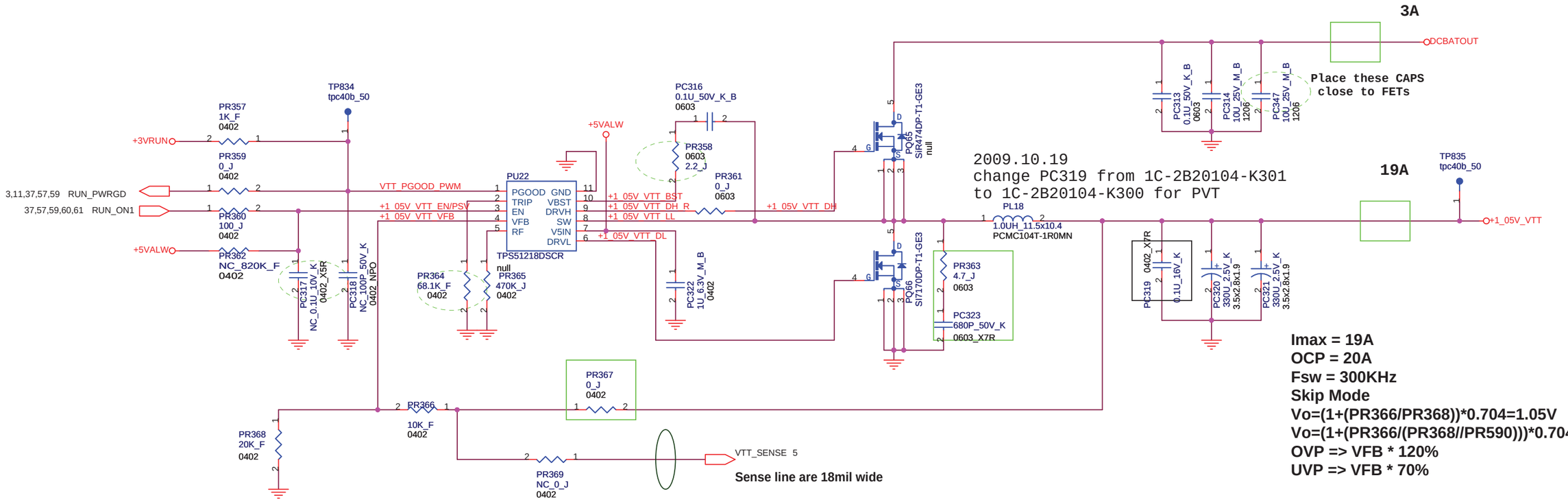
N11M-GE1

	PWRCNTL_0	PWRCNTL_1	GPU Voltage
Battery	0	1	0.85V
Balance	0	1	0.85V
Performance	1	0	1.03V

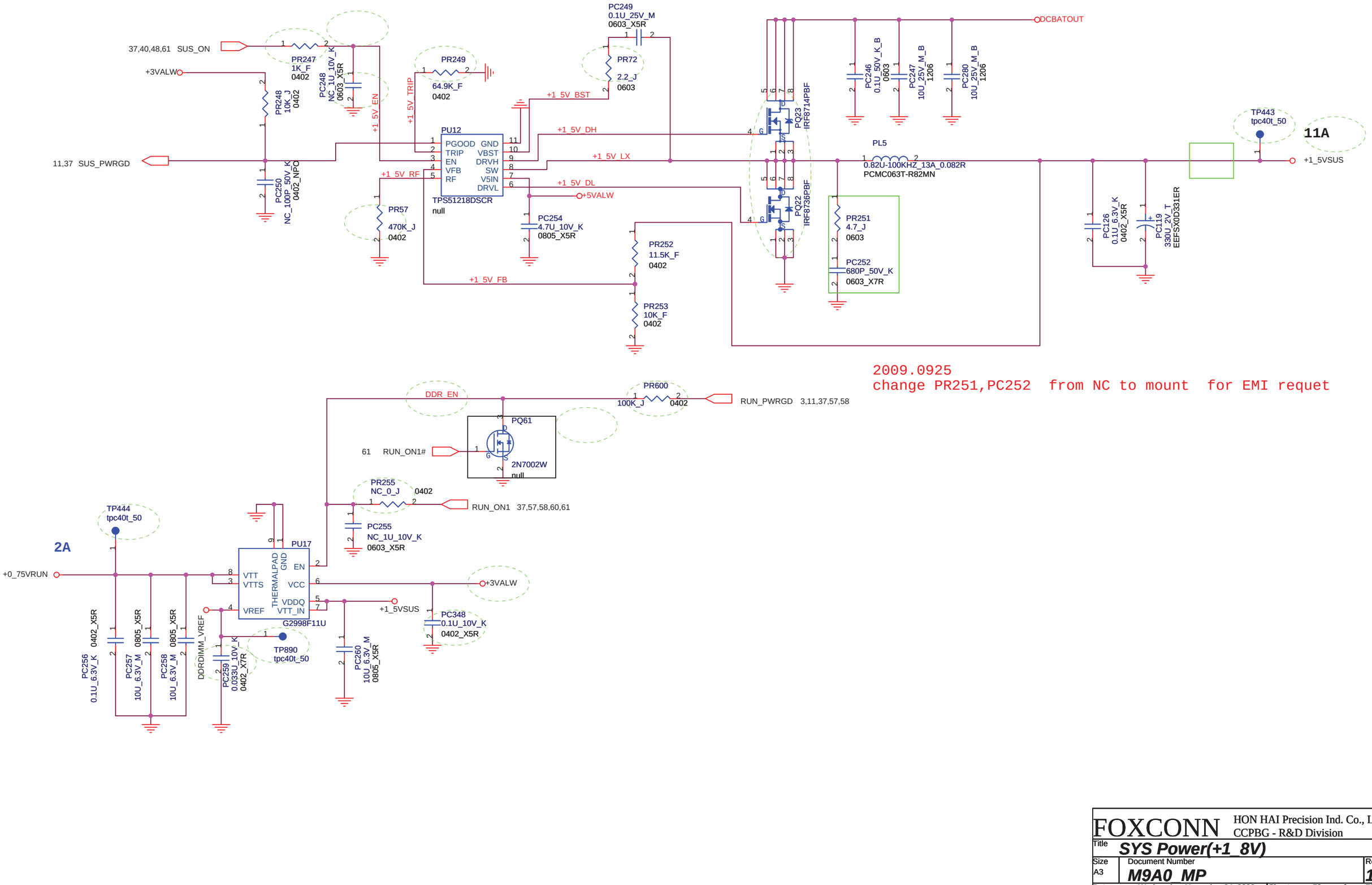
N11P-LP1	0xA2B 0.85V
N11M-GE1	0xA75 1.03V
P8 P12	0.85 V 0.8 V

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: SYS Power(+1_5V/+1_05V)
Size: Custom | Document Number: M9A0_MP | Rev: 1.1
Date: Wednesday, November 04, 2009 | Sheet 57 of 73



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDR3 Power(+1_5V/+0_75V)	
Size: Custom	Document Number: M9A0_MP	Rev: 1.1
Date: Wednesday, November 04, 2009	Sheet 58 of 73	



2009.0925
change PR251,PC252 from NC to mount for EMI requet

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SYS Power(+1_8V)	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, November 04, 2009	Sheet 59 of 73	

2009.11.03
Change PC225 TO mount

Fsw = 350KHz
Skip Mode
Vo=(1+(PR234/PR235))*0.704=1.816V
OVP => VFB * 120%
UVP => VFB * 70%

RF=470Kohm ,300KHz
200Kohm ,350KHz
100Kohm ,390KHz
47Kohm ,450KHz

Place these CAPS
close to FETs

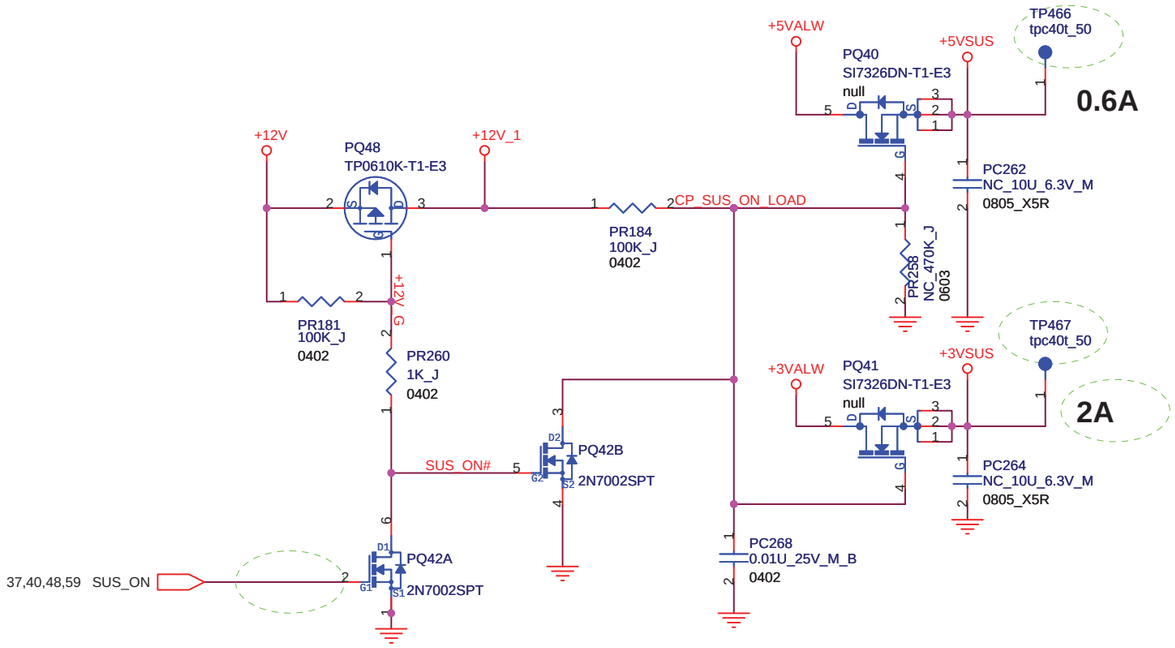
2A

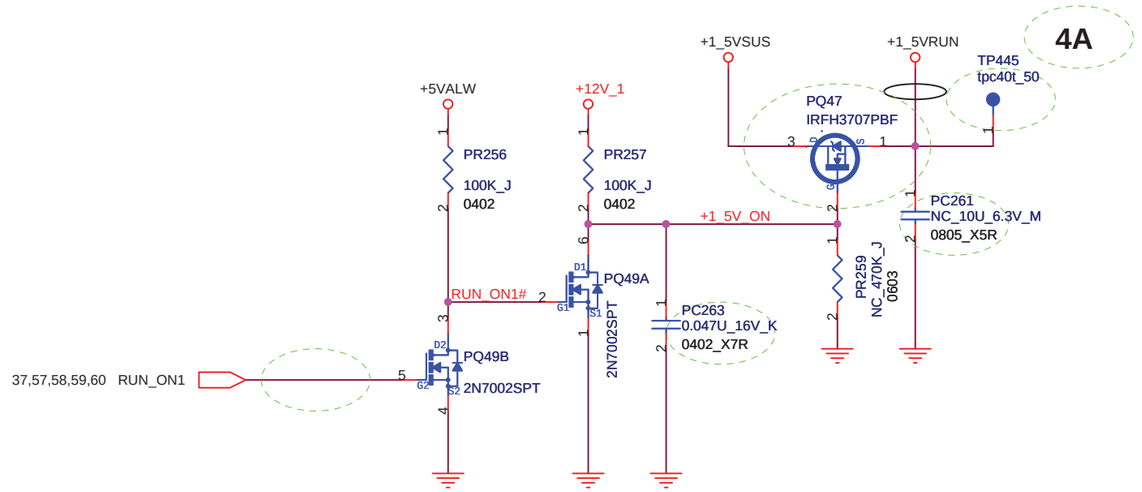
8A

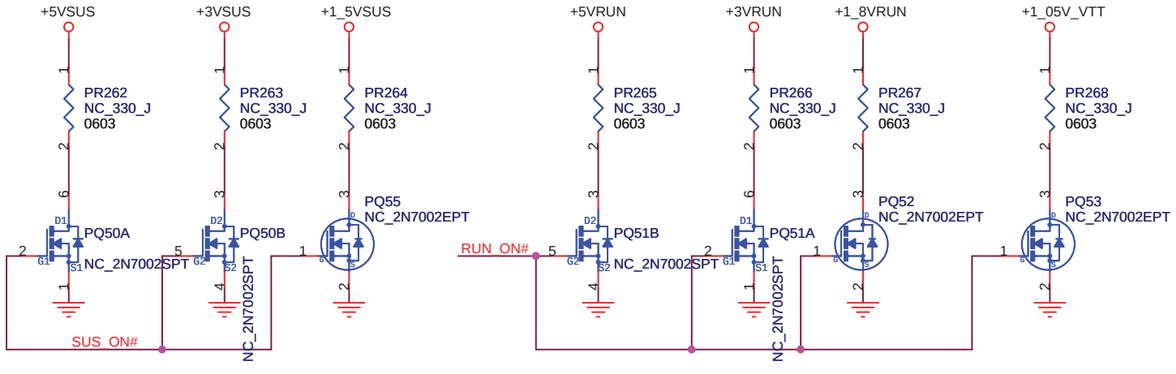
37,57,58,59,61 RUN_ON1
+3VRUN
PR229 1K_J 0402
PC225 0.22U_25V_K 0603_X5R
PC229 0402_X5R NC_0.1U_16V_M
PR231 NC_10K_J 0402
+1_8V_ILIM
PR230 53.6K_F 0402
PC230 0.1U_25V_M 0603_X5R
PR77 0603 2.2_J
+1_8V_EN
+1_8V_PGOOD
+1_8V_BST
+1_8V_DH
+1_8V_LX
+1_8V_DL
+1_8V_RF
+1_8V_FB
PU14
PGOOD GND
TRIP VBST
EN DRVH
VFB SW
RF V5IN
DRVL
TPS51218DSCR
null
PR89 470K_J 0402
+5VALW
PC234 4.7U_10V_K 0805_X5R
PR234 15.8K_F 0402
PR235 10K_F 0402
PQ72 IRF8714PBF
PQ82 IRF8736PBF
PC227 0.1U_50V_K_B 0603
PC228 10U_25V_M_B 1206
DCBATOUT
PL20 2.2UH_6.5*6.9*3 PCMC063T-2R2MN
PR233 4.7_J 0603
PC232 0603_X7R 680P_50V_K
PC170 0.1U_6.3V_K 0402_X5R
PC176 330U_2V_T EEFSX0D331ER
TP441 tpc40t_50
+1_8VRUN

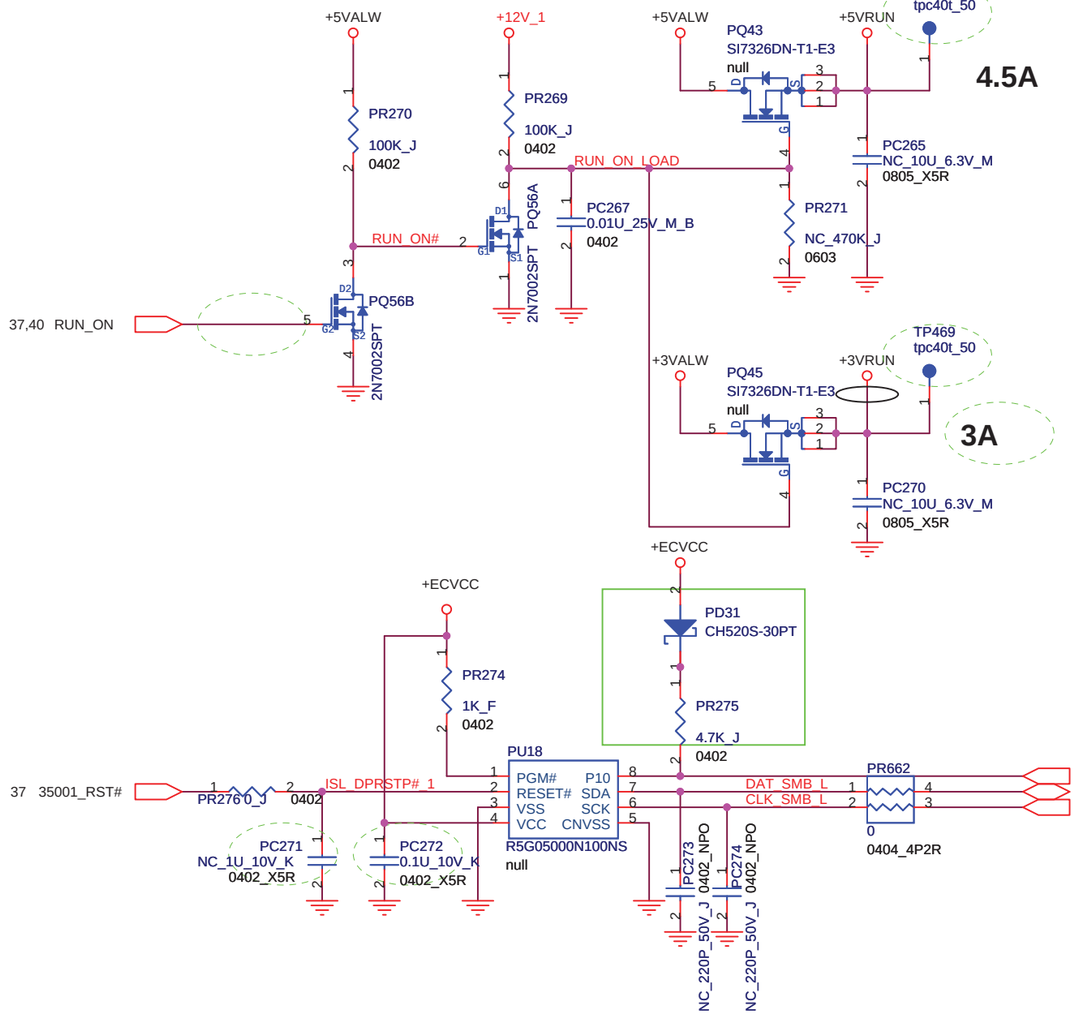
2009.0925
changePR233,PC232 from NC to mount for EMI requet

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Others power plan	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, November 04, 2009	Sheet 60 of 73	

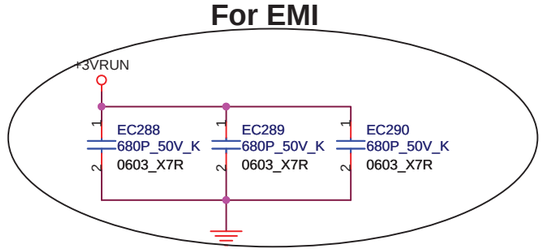


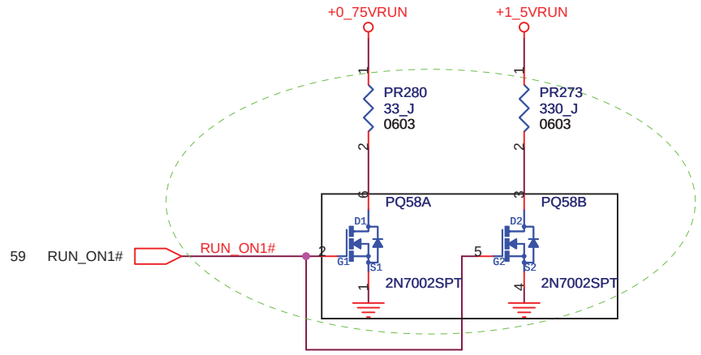






For EMI

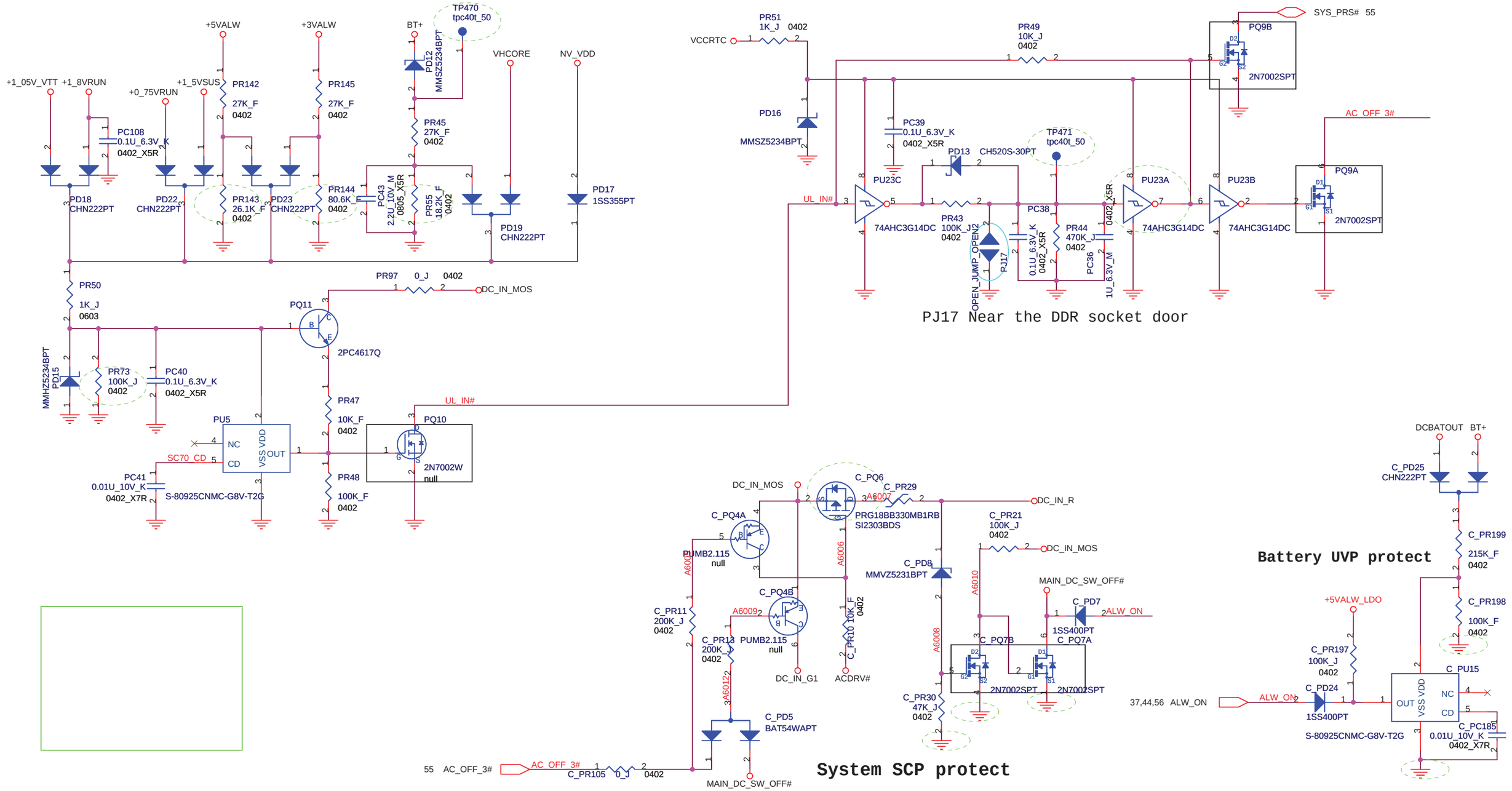




FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title **OVP protection**

Size	Document Number	Rev
A3	M9A0_MP	1.1
Date: Friday, October 30, 2009	Sheet 61 of 73	



VIINP	90W adaptor
PWRLIMIT	1.3V/85W

adapter max load : 5.7A/3000ms
adapter OCP : 7.5Amax

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	VGA Power(Fix +1_1V)	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Thursday, November 19, 2009	Sheet 62 of 73	

DVDD_IO=1.5V : For UMA HDMI
DVDD_IO=3.3V : For Discrete HDMI

For EMI

For EMI

Close to Pin21/22

Place these two capacitor together.

Place these two capacitor together.

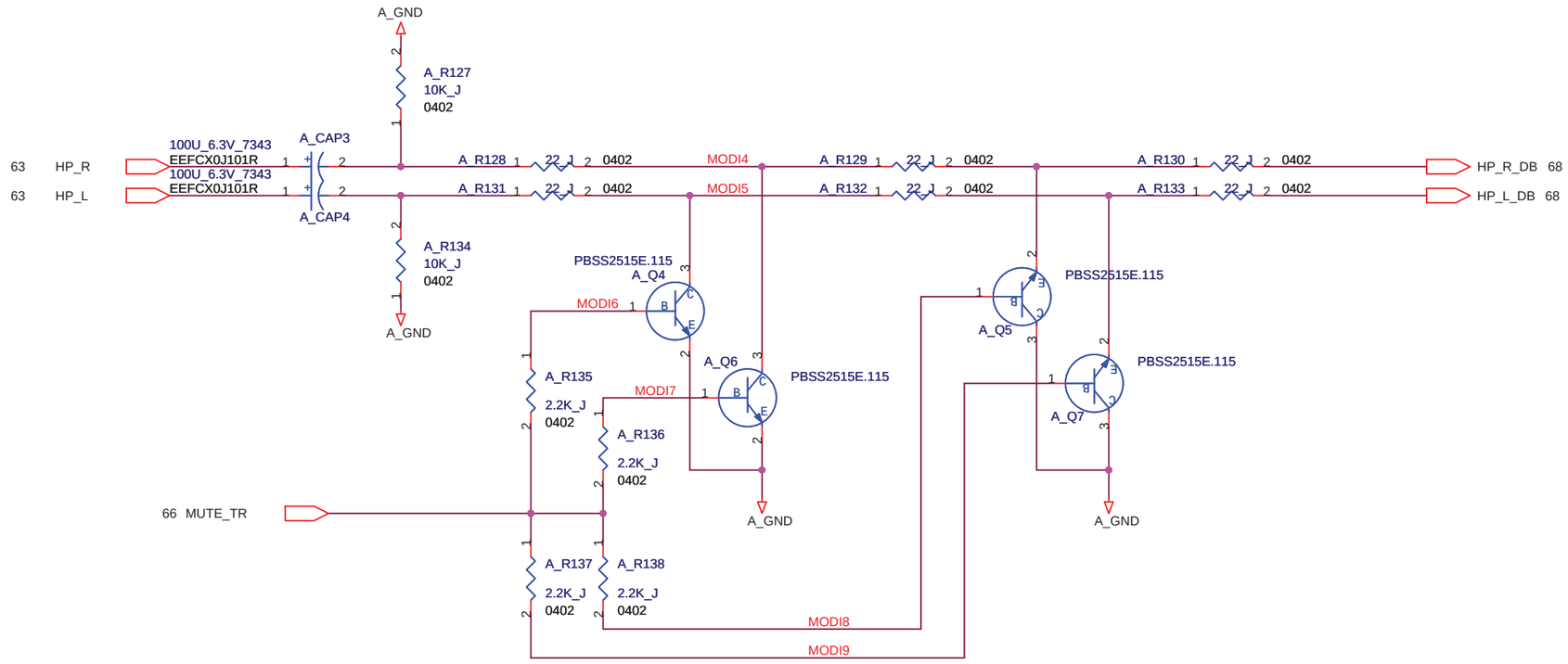
2009.11.03
change A_C23,A_C22 from 15PF to 22PF for EMI request

AUDIO POWER(4.75V/300mA)

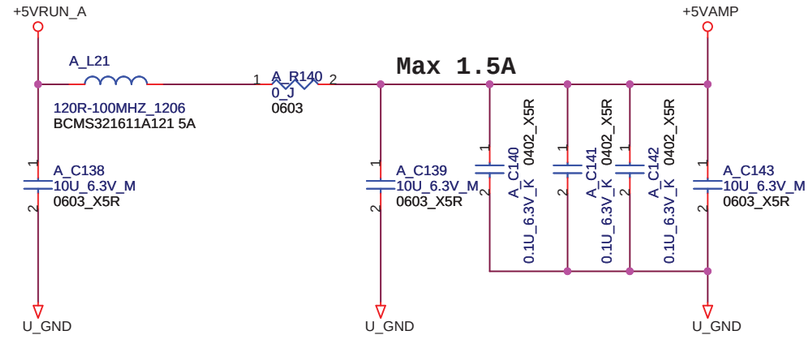
PC BEEP

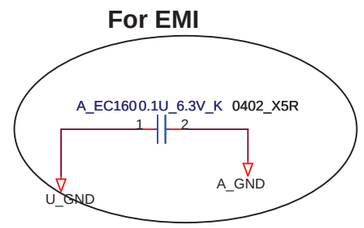
Change A_R123 to 200K from MOR 1/19

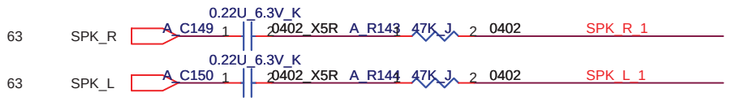
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Audio (CODEC & POWER)		
Size A3	Document Number M9A0_MP		Rev 1.1
Date: Tuesday, November 03, 2009		Sheet 63 of 73	

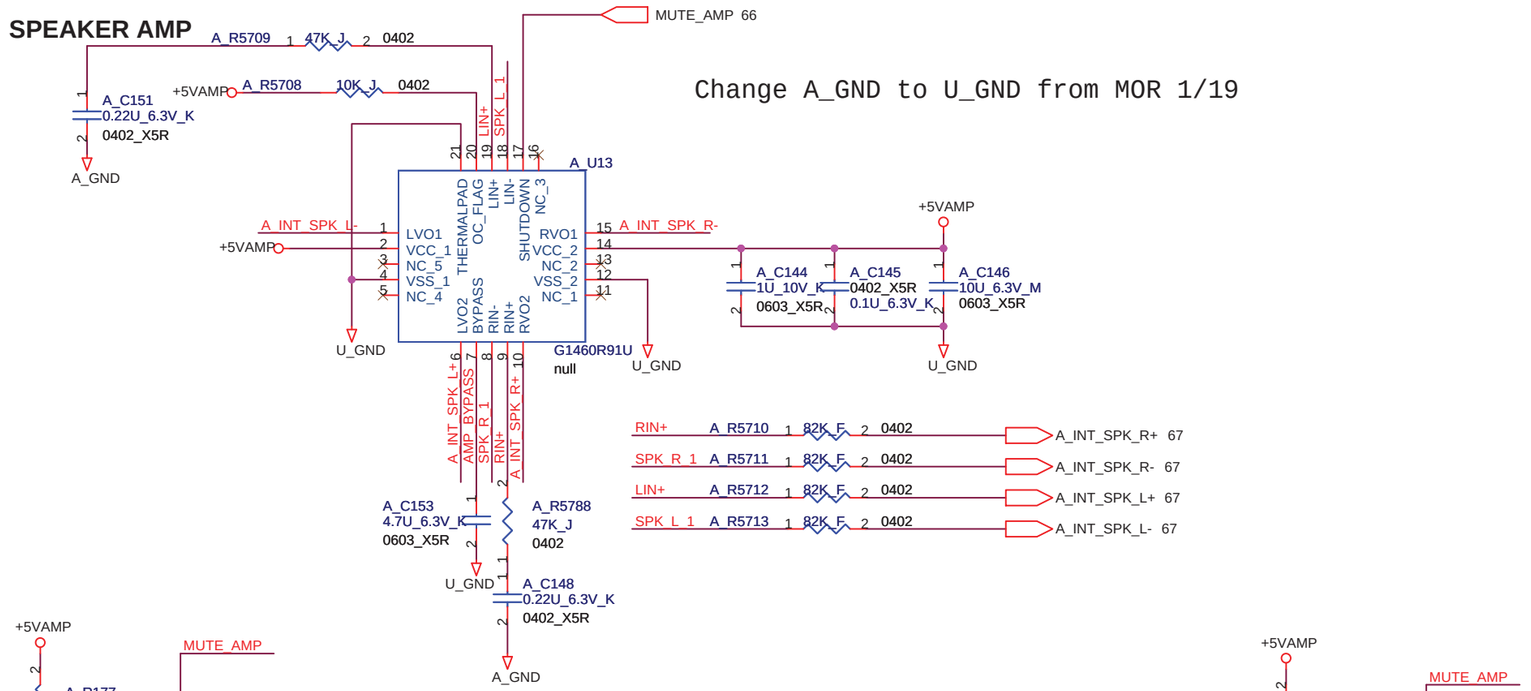


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**Audio (HP)**	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 64 of 73	

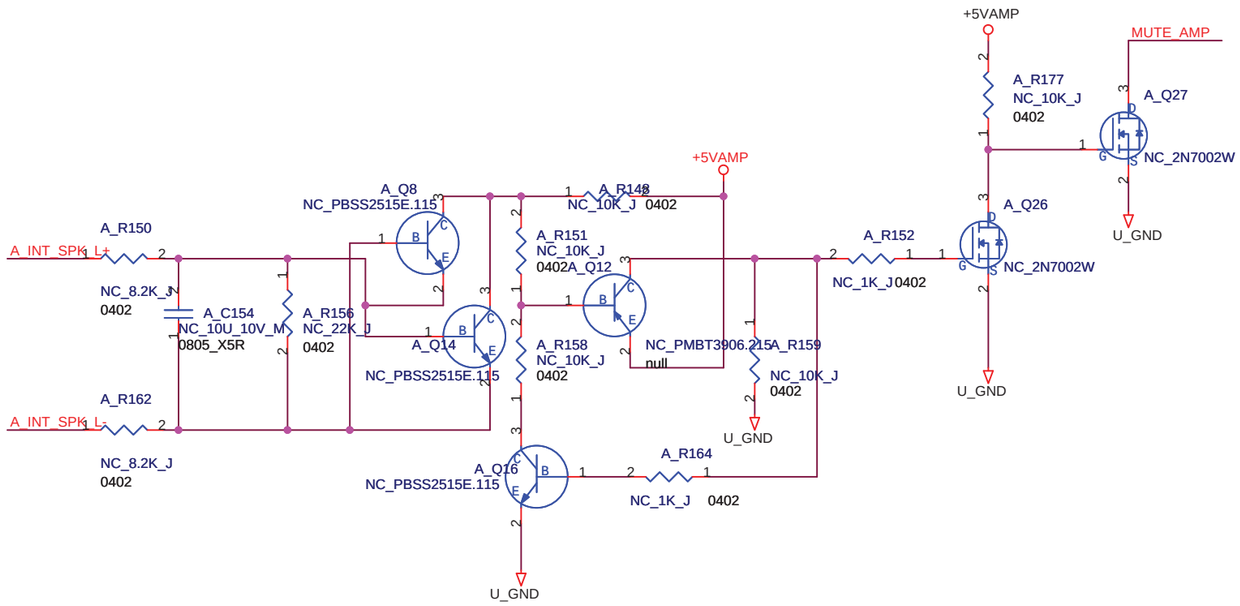


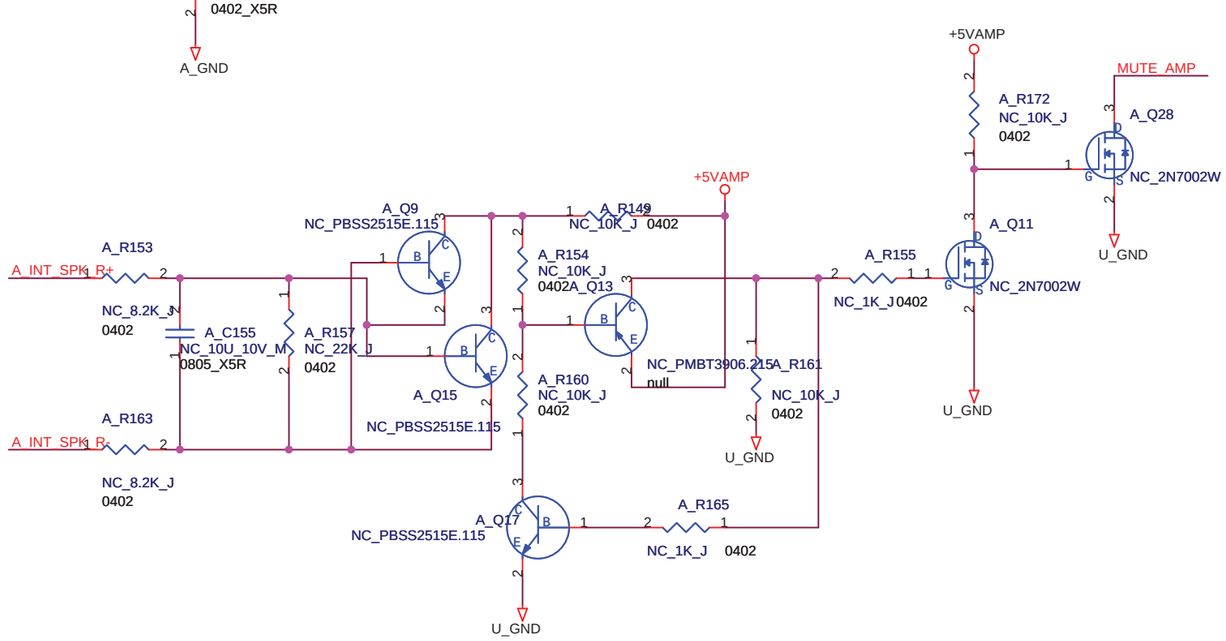






Change A_GND to U_GND from MOR 1/19



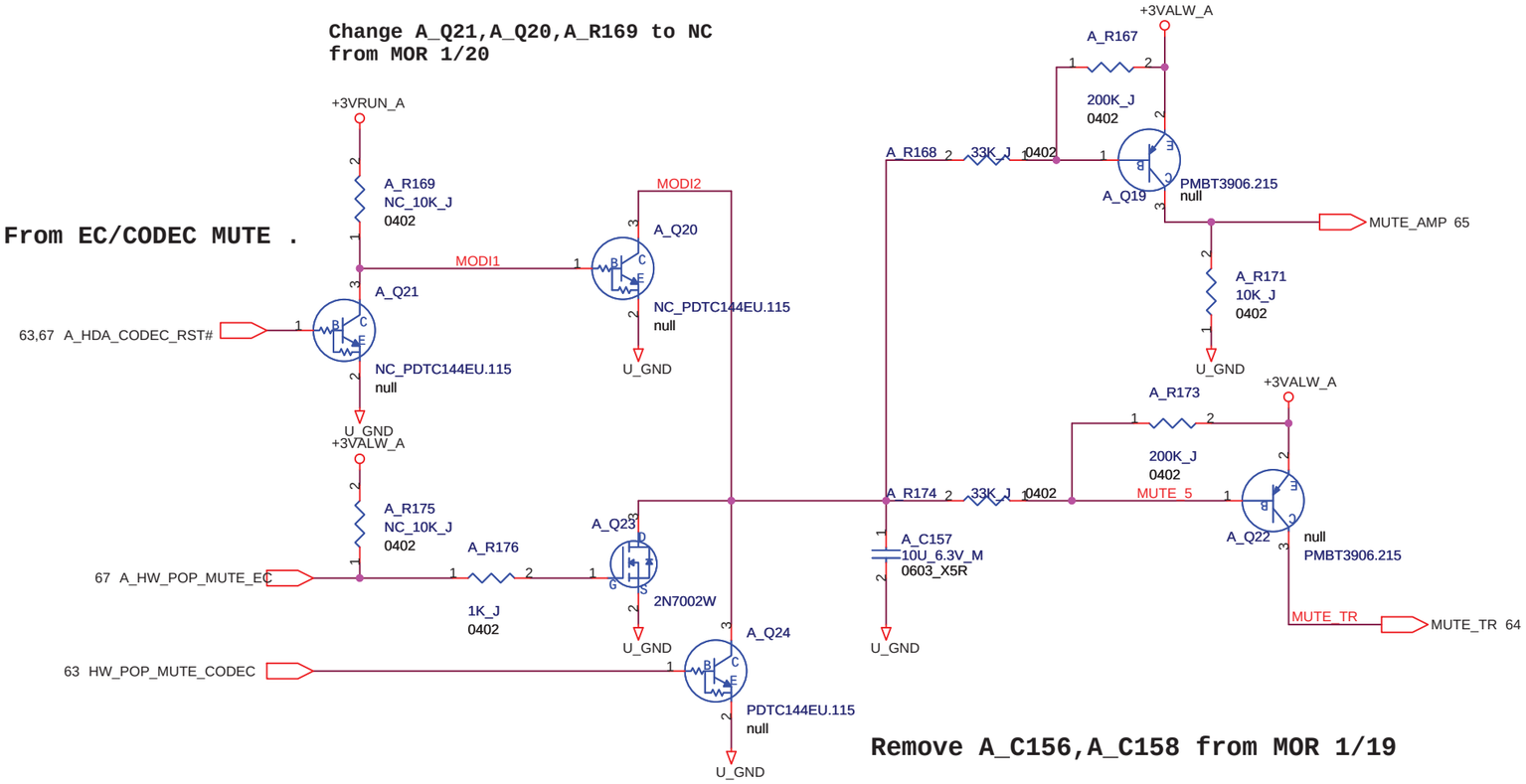


For Mor request,add the speaker cable short protection circuit

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	Audio (SPKR)		
Size A3	Document Number M9A0_MP		Rev 1.1
Date: Friday, October 23, 2009		Sheet 65 of 73	

Change A_Q21,A_Q20,A_R169 to NC from MOR 1/20

From EC/CODEC MUTE .

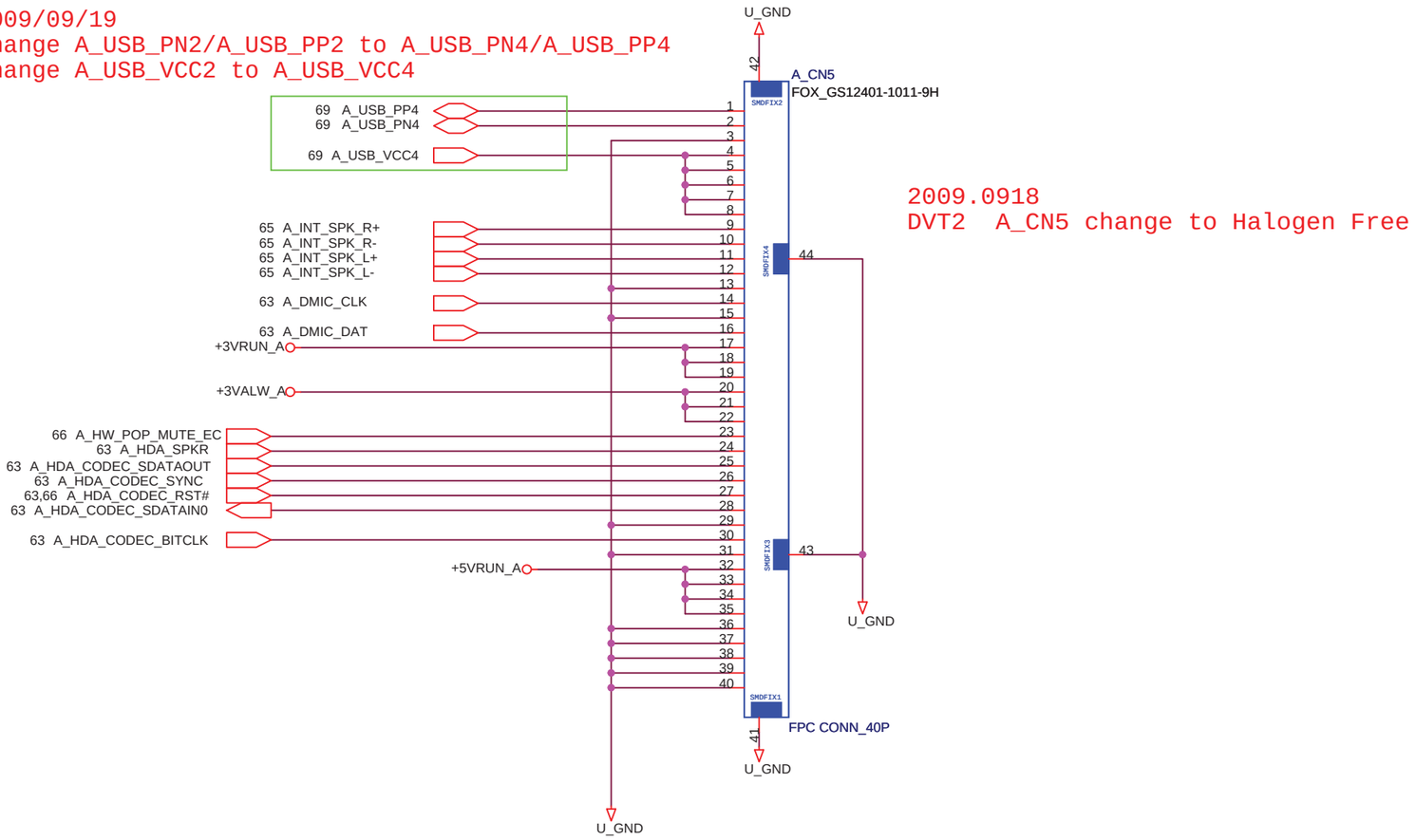


Remove A_C156,A_C158 from MOR 1/19

Delete A_R177+A_R178, change A_Q24 to DTC144EUA from MOR 1/20.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**Audio (MUTE)**	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Friday, October 23, 2009	Sheet 66 of 73	

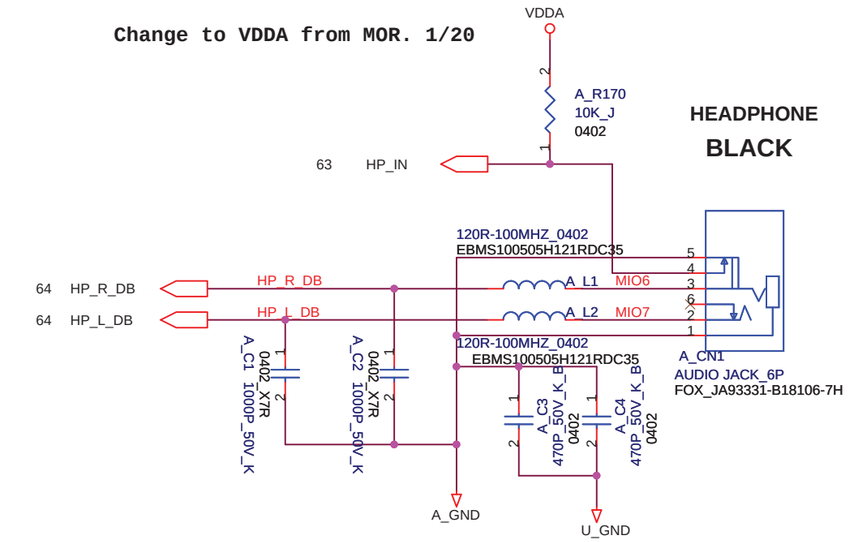
2009/09/19
Change A_USB_PN2/A_USB_PP2 to A_USB_PN4/A_USB_PP4
Change A_USB_VCC2 to A_USB_VCC4

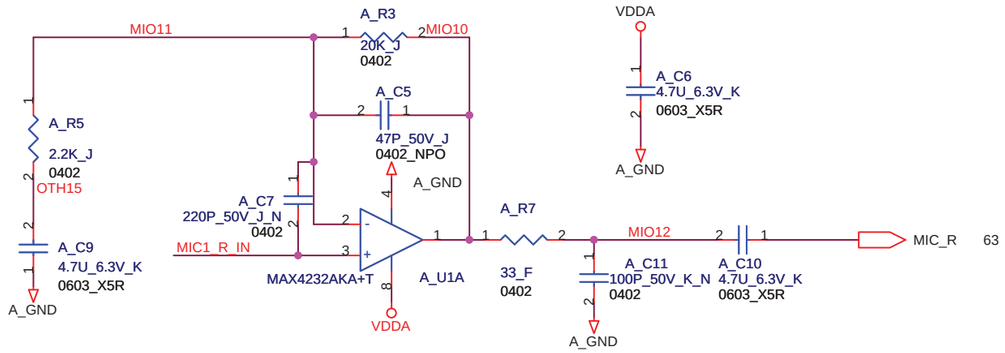


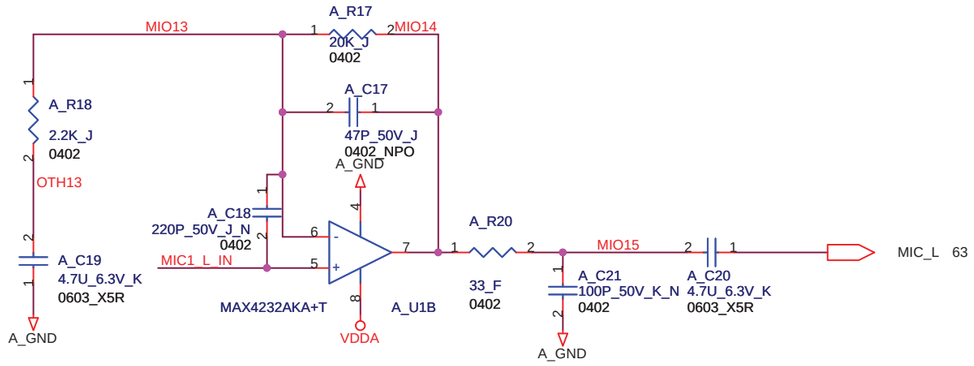
2009.0918
DVT2 A_CN5 change to Halogen Free

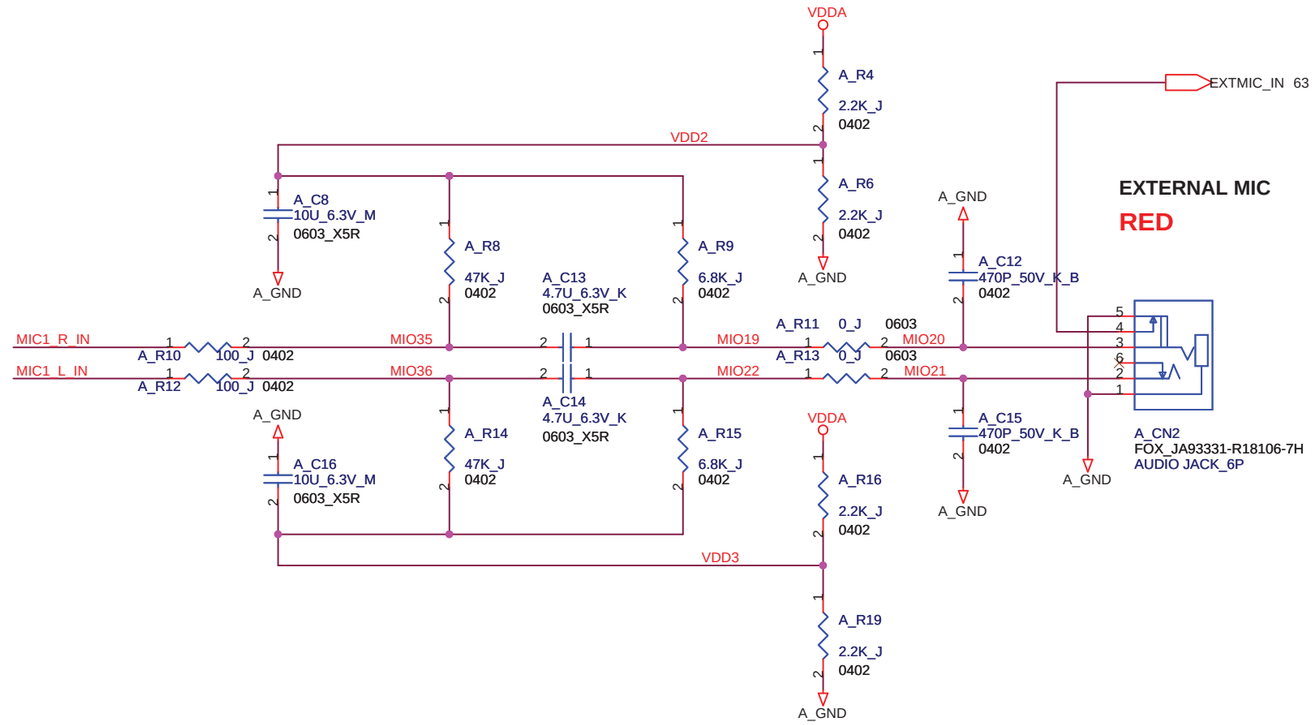
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	***Audio+USB DB CONN***		
Size A3	Document Number ***M9A0_MP***		Rev ***1.1***
Date: Friday, October 23, 2009	Sheet 67 of 73		

Change to VDDA from MOR. 1/20

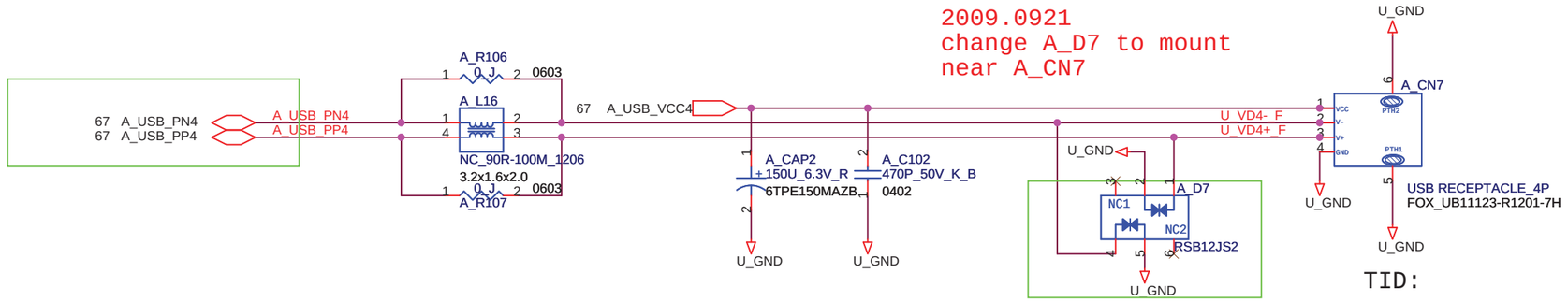








FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**Audio (HP, MIC Jack)**	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Wednesday, November 04, 2009	Sheet 68 of 73	



2009/09/19
Change A_USB_PN2/A_USB_PP2 to A_USB_PN4/A_USB_PP4
Change A_USB_VCC2 to A_USB_VCC4
Change U_VD2+_F/U_VD2-_F to U_VD4+_F/U_VD4-_F

2009.0918
DVT2 A_CN7 change to Halogen Free

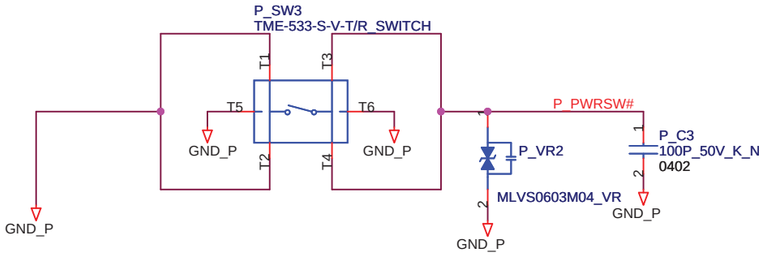
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: USB2.0		
Size: A3	Document Number: M9A0_MP	Rev: 1.1
Date: Friday, October 23, 2009	Sheet 69 of 73	

VespaCP no fingerprint function, so this page reserve

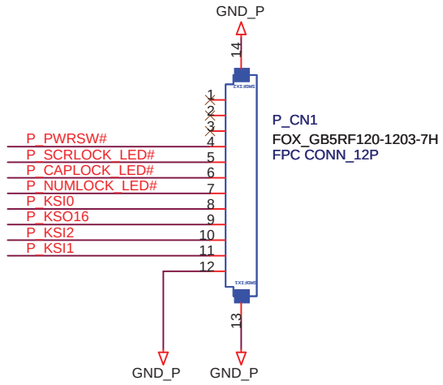
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

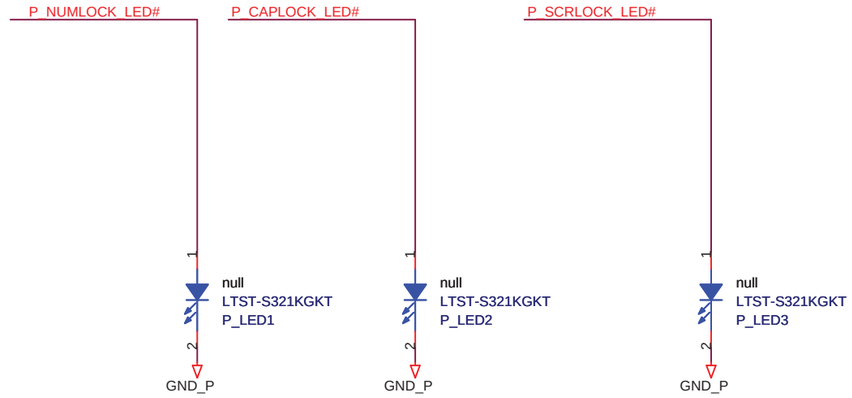
Title: FINGER PRINT		
Size: A3	Document Number: M9A0_MP	Rev: 1.1
Date: Wednesday, September 23, 2009	Sheet of 73	

POWER BUTTON



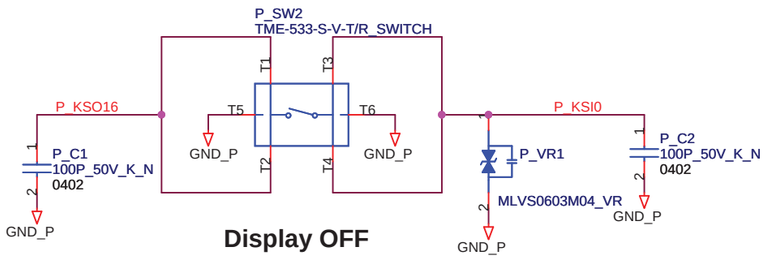
Power Button Board



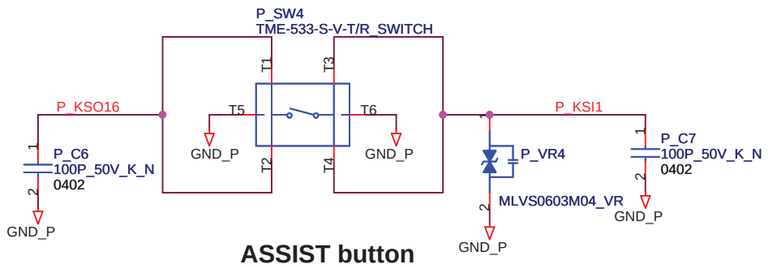


NUM LOCK LED CAP LED SCROLL LOCK LED

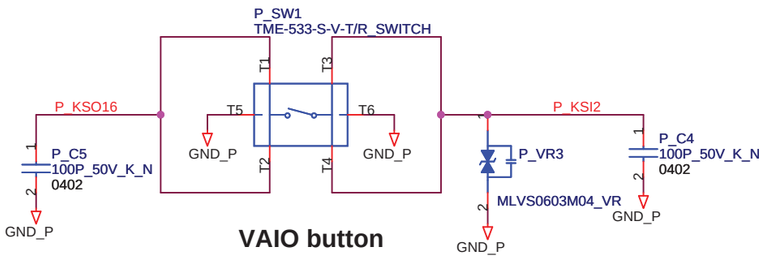
NUM/CAP/SCR LED (Green)



Display OFF

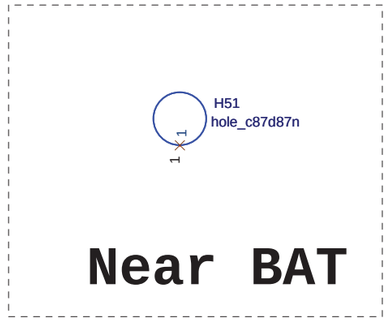


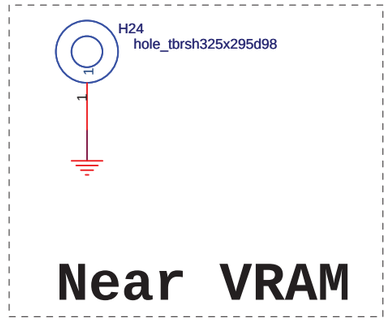
ASSIST button

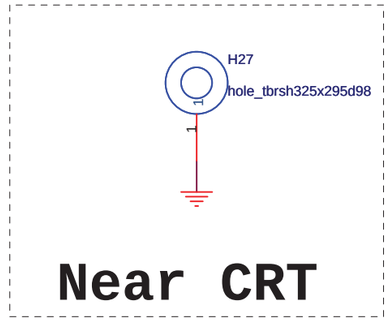


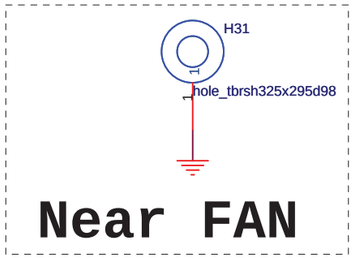
VAIO button

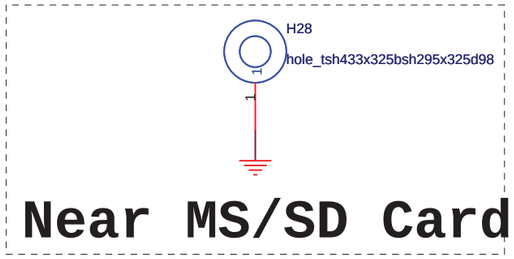
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	CONN & BUTTONS	
Size A3	Document Number M9A0_MP	Rev 1.1
Date: Monday, September 28, 2009	Sheet 71 of 73	

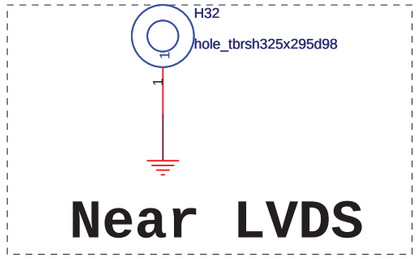


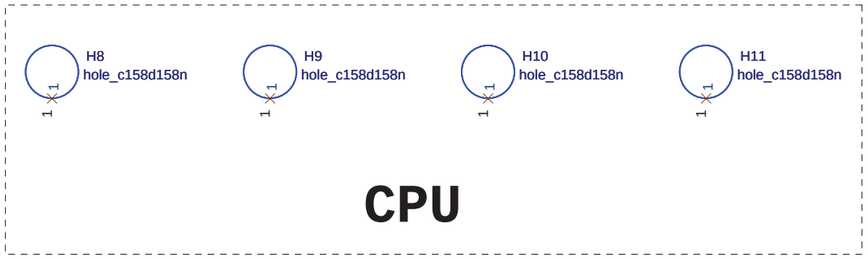


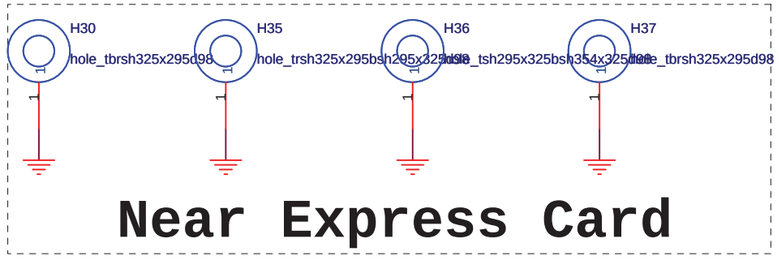


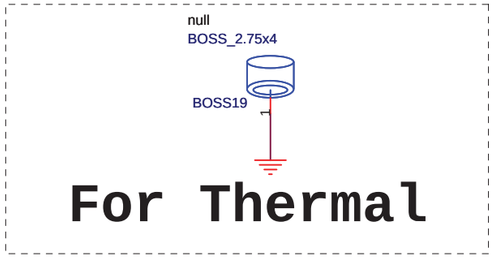


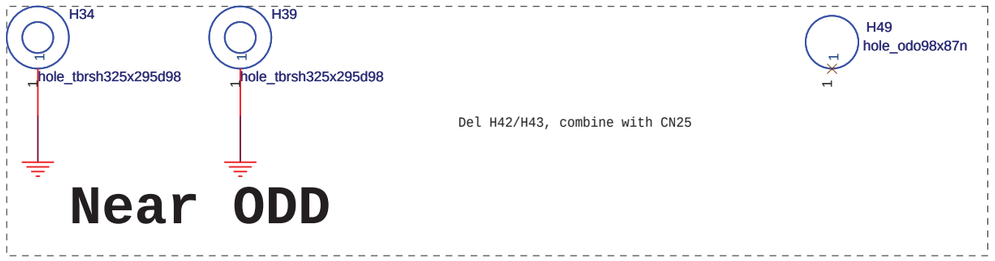


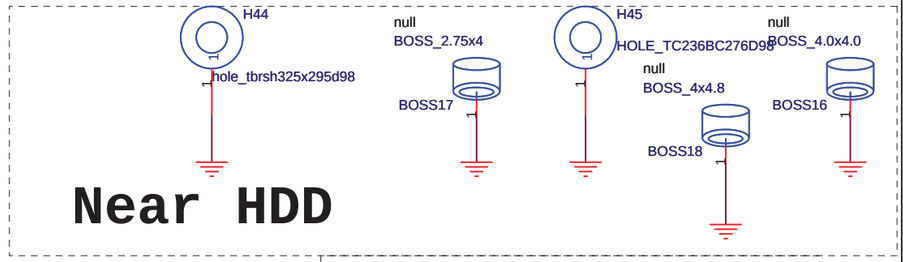


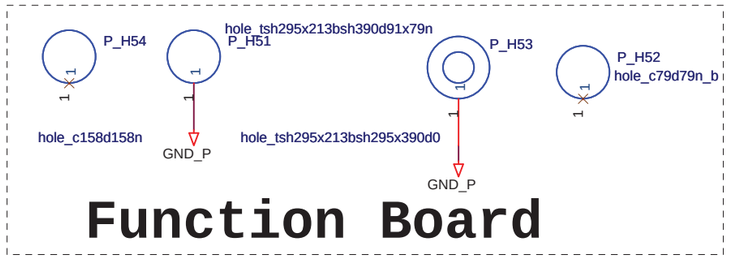


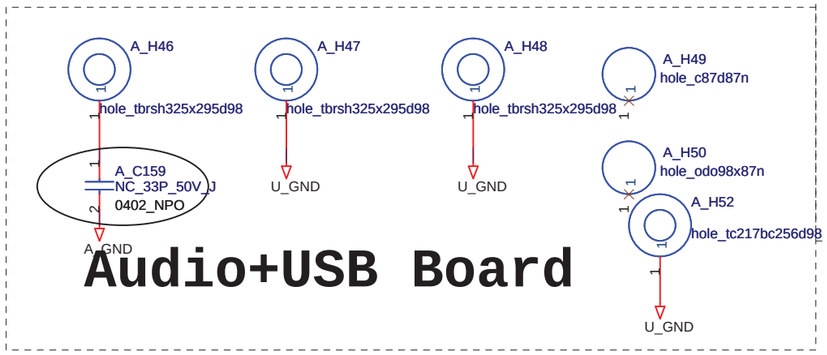




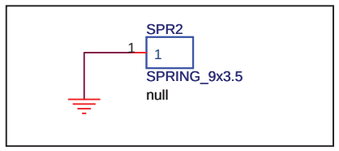








Near Charger Board for EMI



2009.10.20
change SPR2 to 9 X3.5

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: HOLE		
Size: A3	Document Number: M9A0_MP	Rev: 1.1
Date: Thursday, November 19, 2009	Sheet 72 of 73	

2009/0910

1. Add S/D CARD test point for L6 TE request
TP736

2. Add MS CARD test point for L6 TE request
TP690, TP691, TP693, TP694, TP695, TP696, TP697
TP702, TP724, TP698, TP699, TP700, TP701, TP703

delete

3. Add I_LINK test point for L6 TE request
TP512, TP513, TP514,TP515

4. Add TOUCHPAD test point for L6 TE request
TP551, TP550, TP535, TP534 ,TP562, TP564

5.Delete R5893, R5887 and trace AC PRESENT,
add R6007 to +3VALW in page 11, delete trace AC PRESENT,
add test point TP186 in page 37. VespaCP use Ignition FW,
no ACPRESENT function.
Intel FAE suggest this pin can configure as GPIO.

6.change C6131 from NC_470P_16V_K to 0.047U_16V_K follow Intel suggest

7. Change trace（CLK-PCIE-EXPRESS#,CLK-PCIE-EXPRESS,EXPRESS-CLKREQ#) from
U134(AH42,AH41,A8) to (AJ50,AJ52,H6) for DVT1 express card can't detect issue.

8. Change page 70 from finger print to reserve, VespaCP no this function.

2009/0912

9. Delete R5785 0ohm resistor for voltage drop problem

10. Change RP82 from NC to mount for SI test
Change RP81 from mount to NC for SI test
Change RP86 from NC to mount for SI test

2009/0914

11.delete finger print

12.delete TP417,link to gnd

13.CN16 PIN 15 LINK TO GND
14.CN35: change 0ohm to 33ohm

15.PCH: GNT0# and GNT1# change from pull high to +3vsus to pull low to gnd

16.DC_IN: DELETE C_PQ9 ,C_PR34
change C_PR36,C_PR37 from NC to mount
C_PF1 change to 0437007.WR

17.+1.05V: change PC319 from Y5V to X5R

18. VHCORE: change OVT_EC# to PROCHOT#

20.other: add PD31
change PR275 from 10K to 4.7K

21.OVP: DELETE PR78 ,PQ17
change PC35, PU2, PC37, PR240, PR108,PR39,
PR36 from mount to NC

22.N11P-LP1+SANSUNG(H2) SKU and
N11M-GE1 +SANSUANG(M2 SKU)need change BOM
R5244 change from 1R-0004532-F200(45.3K) to
1R-0002492-F200(24.9K) for nVIDIA FAE suggest

2009.0918
23. CN11, CN18, CN34, CN9, CN12, A_CN7, A_CN5 change to Halogen Free

2009/09/19
1.Change A_USB_PN2/A_USB_PP2 to A_USB_PN4/A_USB_PP4
Change A_USB_VCC2 to A_USB_VCC4 in page 67

2. Change A_USB_PN2/A_USB_PP2 to A_USB_PN4/A_USB_PP4
Change A_USB_VCC2 to A_USB_VCC4
Change U_VD2+_F/U_VD2-_F to U_VD4+_F/U_VD4-_F in page 69

3.Change USB_VCC2 to USB_VCC4
Change USB_OC#0 to USB_OC#1 in page 48

4.Add USB_OC#1
Change USB_PN10/USB_PP10 to test point in page 13

5.Change USB_VCC2 to USB_VCC4 in page 43

2009.0921
Page 50
1.R531 Delete,then pull CN34 pin4 to GND.
2.Remove the Test point TP562 to +5VRUN.

2009.0922
1.change R5272,R5273 from NC to mount
2.add R5313 for 10K_J
3.change R5916 TO NC
4.change D15,D21,A_D7 TO mount and place them near connector
5.WIRELESS_DATA/WIRELESS_CHCLK change，please refere to page 49
6.ADD R5991 for 100K_J
7.change C476 TO NC_12P
8.change C1986 TO 12P
9.ADD R6010,R6011,R6012 to pull-down SPI0_CLK,SPI0_MOSI,SPI0_CS# in page 09
10.change CN25,CN29,CN30 TO Halogen Free
11.change D13,D11 TO 16-SSM22LL_PT00
12.change R5910,R5911 to NC_1K
13.DELETE TP498,TP491,TP490,TP495,TP494,TP509
14.CHANGE Q45 TO NC ,R5996 TO MOUNT
15.change CN21 TO 1N-1052000-0000 for ME request
16.change BOSS1,BOSS2 to 1M-1F40M20-1500 for ME request
17.page 57:change net PWRCNTL_0_R TO PWRCNTL_1_R
change net PWRCNTL_1_R TO PWRCNTL_0_R
change PR389,PR380 TO 110 ohm
change PC334 to 220P_16V_J 0402
change PC337 to 220P_50V_J 0402
delete PJ23,PJ24,PJ25,PJ26

18.page 53:delete PJ18,PJ19
19.page 56:delete PJ1,PJ2
20.page 58:delete PJ20,PJ21,PJ22
ADD PR367/0 ohm
21.page 59:delete PJ5
22.page 60:delete PJ3
23.page 06:delete PJ43

2009.0923
ADD test point TP490,TP491,TP494,TP495,TP498,TP509

2009.0925
ADD C6260 NC_1000P_16V_K

2009.0925
For EMI request
1.Add Cap.C36 0.1U,C999 1000PF on net +1_05V_VTT
2.Add Cap.C37,C38 0.1U on net +1_8VRUN
3.Add Cap. C39 0.1U,C1000 1000PF on net +3VRUN
4.Add Cap.C53,C54,C61 0.1U on net DCBATOUT
5.Add SPR2

2009.0925
ADD C70,C71,C72 10P for RF request

2009.0925
change C6156,C6157 from 12p to 15p for vendor request

2009.0925
change PR245,PC269,PR236,PC266,PR363,PC323,PR251,
PC252,PR233,PC232 from NC to mount for EMI request

2009.0926
For EMI request
1.Add PC62 0.1U on net +1_8V_LX ,place it near PQ72
2.change C539 from NC to 680P
3.Add C549 680P on net INV_BRADJ,place it near LVDS connector

2009.0928
For RF request
change C1264,C716,C532 to 47P

2009.0928
change R5376 to 100K follow design guide

2009.0928
change PC337 to 22P

2009.0928
Add Q7 for MOR request

2009.0929
Add PC206 NC_0.1U reserve for Return patch

2009.0929
change RP86 ,RP82 TO NC
change RP81 TO mount

2009.10.19
1.Change PC319 from 1C-2B20104-K301 To 1C-2B20104-K300.
2.change R5703 from 68ohm to 75 ohm
3 NC RP81 for 1R-1010000-JP00
4. MOUNT RP82, RP86 for 1R-1010000-JP00
5. change C5250 from 1C-2B20473-K300 to 1C-2B20102-K001
6. change C6256 from 1C-2B20102-K001 to 1C-2B20473-K300

2009.10.20
change SPR2 from 4x3 to 7x2.5

2009.10.22
PAGE37:delete C468, C513, U25, R76, R55, R41, R73, C60（NC), TP871,
TP872,TP873,TP876,TP878,TP880,TP874.TP875,TP877,TP879,TP881,
TP882 for PVT
PAGE53:change PC112 from 68U to 47U for power request

2009.10.23
Page 35：deleteJ2,J3
Page 38：delete TP531,TP530,TP532,TP533,TP529,TP520,519,TP518
Page 05：delete R5786
Page 37：add TP690, TP690
PAGE 45,46:change net SD_WP# to SD_WP
Page 35：Add test point TP897,TP898,TP899 for PVT

page 35：add TP900,TP901 for +3VRUN

2009.10.28
page 57: Change PC344 to 1C-2B70226-M100.
Add PC345 1C-2B70226-M100.
Change PEX_VDD to 2.5A.

2009.10.30
page 55: Change C_PQ3,C_PQ8 to 17-2N7002W-0000.

page 59: Change PQ61 to 17-2N7002W-0000.

page 61: Change PQ58 to 17-2N7002S-PT00.

page 62: Change C_PQ7 to 17-2N7002S-PT00.
Change PQ10 to 17-2N7002W-0000.
Change PQ9 to 17-2N7002S-PT00.

Page 51:change R5992,R5993,R5994 from 120ohm to 549ohm follow M870

Page 36:change Q9 to 17-2N7002S-PT00.
Page 03:change Q179 to 17-2N7002S-PT00

Page 72 :change SPR2 to 9 X3.5

2009.10.31
page 57: Add PC350 1C-33U0337-KX00 NC_330U_2.5V_K.

Page 14 ：add RP83 NC_0 to escape crosstalk

2009.11.3
Page60：Change PC225 TO mount
page 60: Delete PC62.

page 60: Change PR229 to 1K_J.
Change PC225 to 0.22U_25V_K.

2009.11.03
Page 35:add C60,C62,C63,C64

For EMI request
1:Page 55 change C_PC14 to 4700pf
change C_PC13 to 0.1U
2: Page 55 change C_PC156 to 2200pf
3.Page 63 change A_C23,A_C22 from 15PF to 22PF

2009.11.4
Page 35:add C65,C66,C67,C73,C74 for FAN issue

page 55: Change C_EC6066 to 1C-2B30104-K000.

page 56: Add TP442.

page 56: Change E_C6060 to 1C-2B30104-K000.
Change E_C6059 to 1C-2B30104-K000.
Change E_C6067 to 1C-2B30104-K000.
Change E_C6068 to 1C-2B30104-K000.
Change E_C6062 to 1C-2B30104-K000.
Change E_C6061 to 1C-2B30104-K000.

2009.11.16
change C_PC14, C_PC156 to 1000P for EMI request

2009.11.19
Page49: Change R6009 from 1R-0000000-J200 to 1R-0000101-J200 for RF request

2009.11.19
Page 55: Add C_PQ26,C_PQ27,C_PQ9 NC_TPCC8102 for 2nd source.

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: History (1)

Size: A2 | Document Number: M9A0_MP | Rev: 1.0

Date: Friday, November 20, 2009 | Sheet 73 of 73