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P. Leader	Check by	Design by

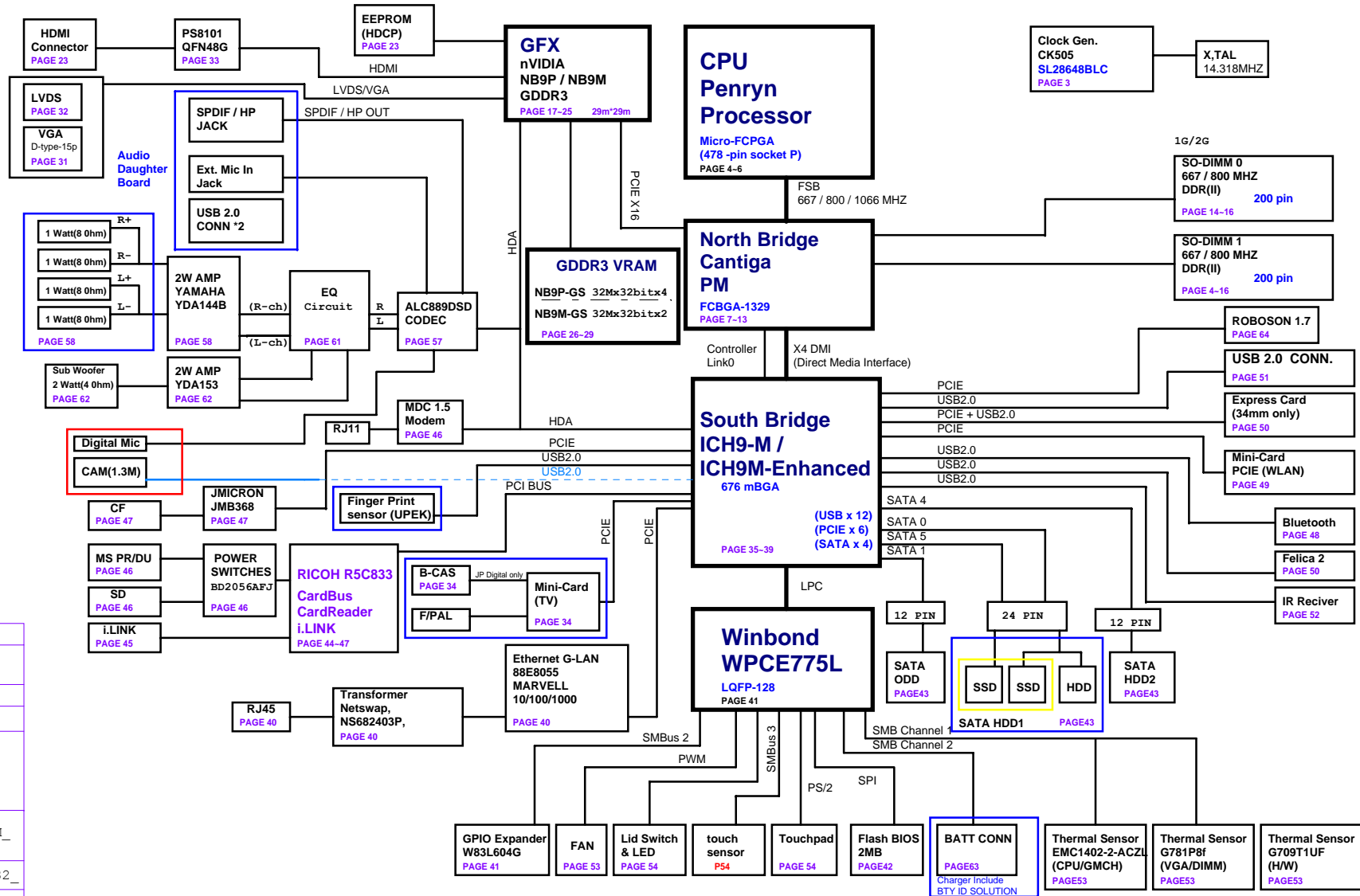
DVT to PVT

**Project Code & Schematics Subject:** M780 EVT Main Board

**PCB P/N:** FUBAI 1P-0086102-8010

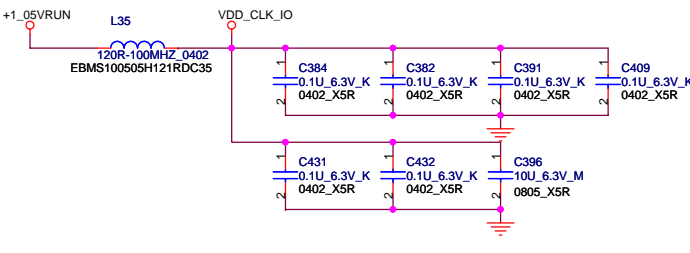
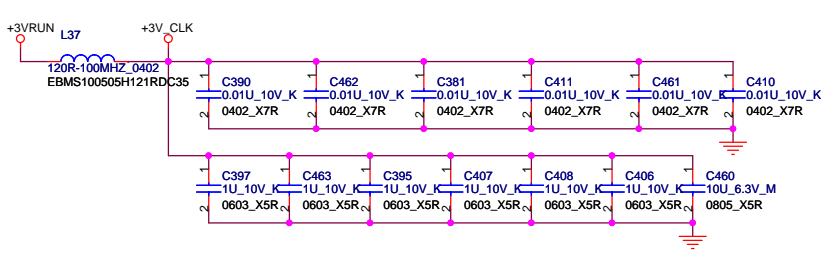
<b>FOXCONN</b> HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title <b>Index</b>		
Size A3	Document Number <b>M780(MBX-194)</b>	Rev <b>0.1</b>
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# M780 Montevina Block Diagram

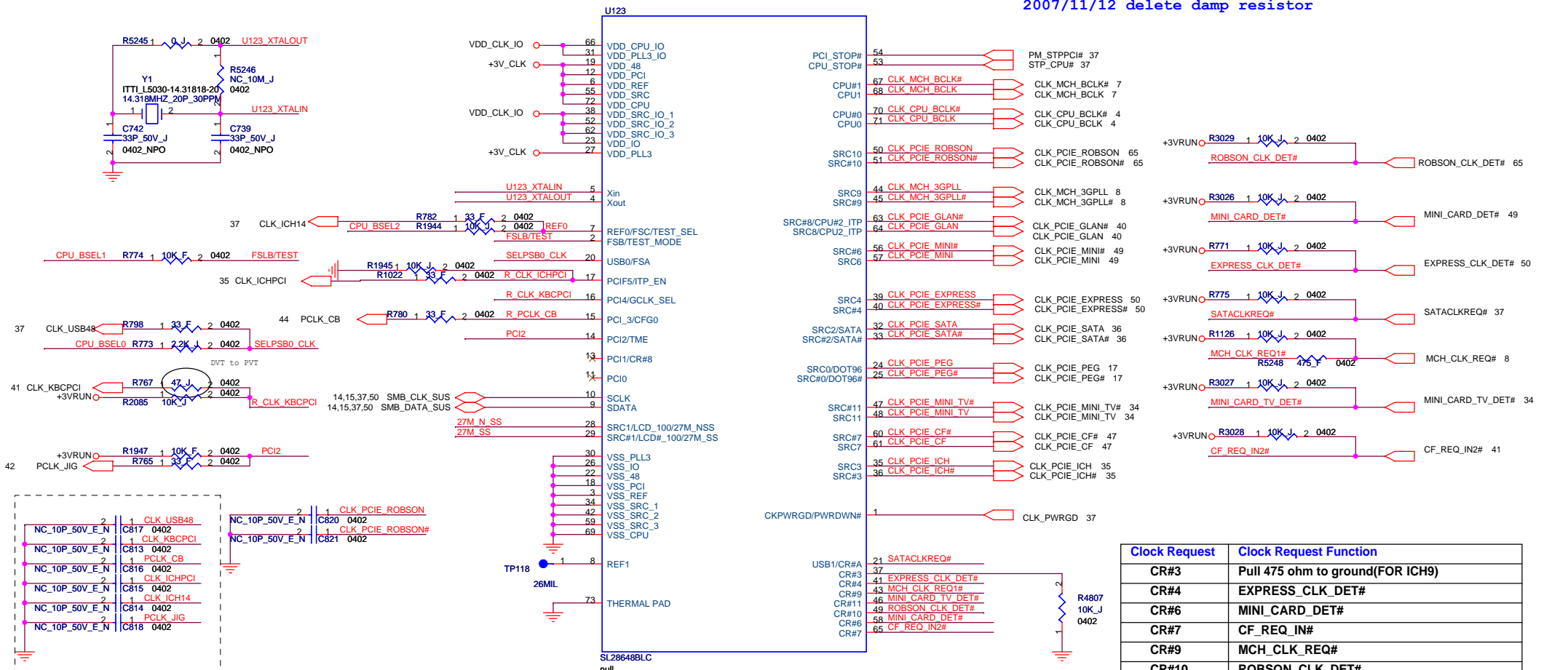


TI CHARGER	
BQ24751 P.63	
INPUTS	OUTPUTS
DC_IN	BT+ DCBATOUT
SYSTEM DC/DC	
ISL6236IRZA-T P.64	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC +15V_ALW
SYSTEM DC/DC	
SC411 P.65	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VM
SYSTEM DC/DC	
ISL6269A P.66	
INPUTS	OUTPUTS
DCBATOUT	+1_8VSDS
SYSTEM DC/DC	
G2998 P.66	
INPUTS	OUTPUTS
DCBATOUT	+0_9VRUN
CPU DC/DC	
ISL6266A P.67	
INPUTS	OUTPUTS
DCBATOUT	VHCORE
SYSTEM DC/DC	
APL5913 P.70	
INPUTS	OUTPUTS
+1_5VRUN	APL5913
SYSTEM DC/DC	
SC411 P.70	
INPUTS	OUTPUTS
DCBATOUT	NV_VDD

M780 BOM configuration	
unstuff	NC_
NB9P-GS + NB9M-GS	NV_
for L model	NV9L_
for M model	NV9M_
B-CAS Card, Felica module for J SKU stuff	LNC_
Roboson,TV Tuner, I.R. Receiver, CF Card Slot unstuff for L Model	
for H M model	NV9HM_
for L model 32Mx32 GDDR3	NV9L32_
for H model	NV9H_
for Qimonda VRAM	NV9QI_
for Samsung VRAM	NV9SAM_



2007/11/12 delete damp resistor

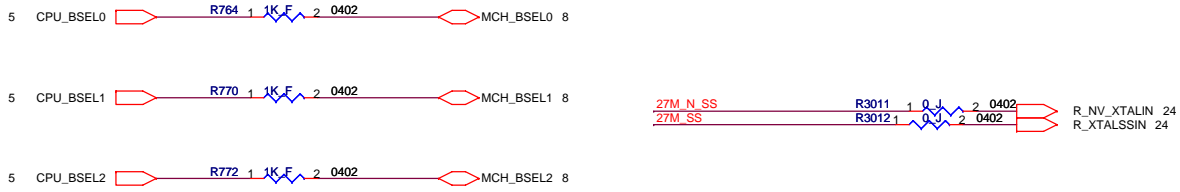


Clock Request	Clock Request Function
CR#3	Pull 475 ohm to ground(FOR ICH9)
CR#4	EXPRESS_CLK_DET#
CR#6	MINI_CARD_DET#
CR#7	CF_REQ_IN#
CR#9	MCH_CLK_REQ#
CR#10	ROBSON_CLK_DET#
CR#11	MINI_CARD_TV_DET#
CR#A	SATACLKREQ#

**FSB Frequency Table:**

FSLC	FSLB	FSLA	CPU	SRC	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33

close to clk gen (For EMI)



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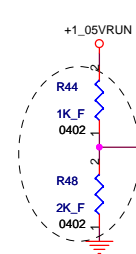
**CLOCK GEN (SL28648LFXC)**

Size: A3 Document Number: **M780(MBX-194)** Rev: **0.1**

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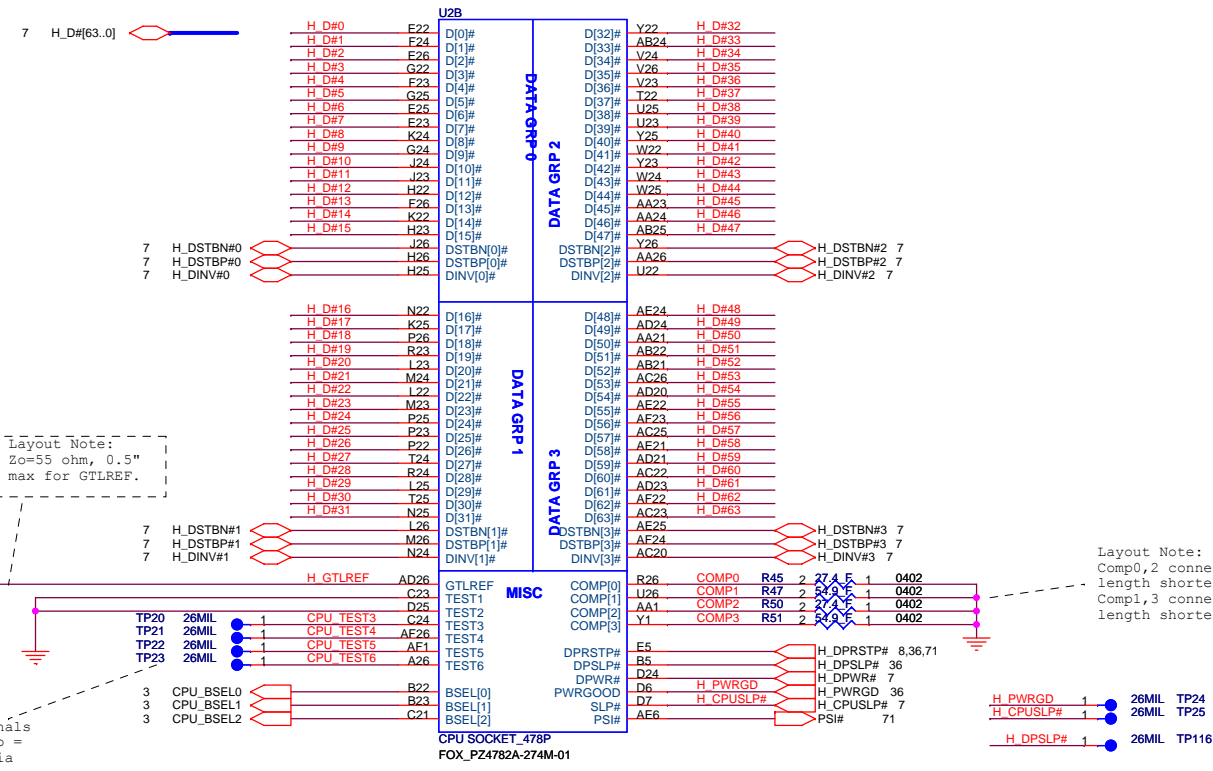


Place close to CPU

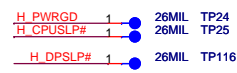


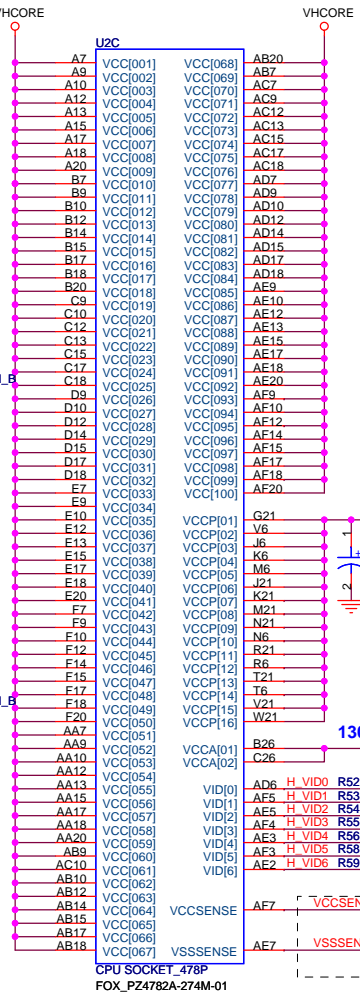
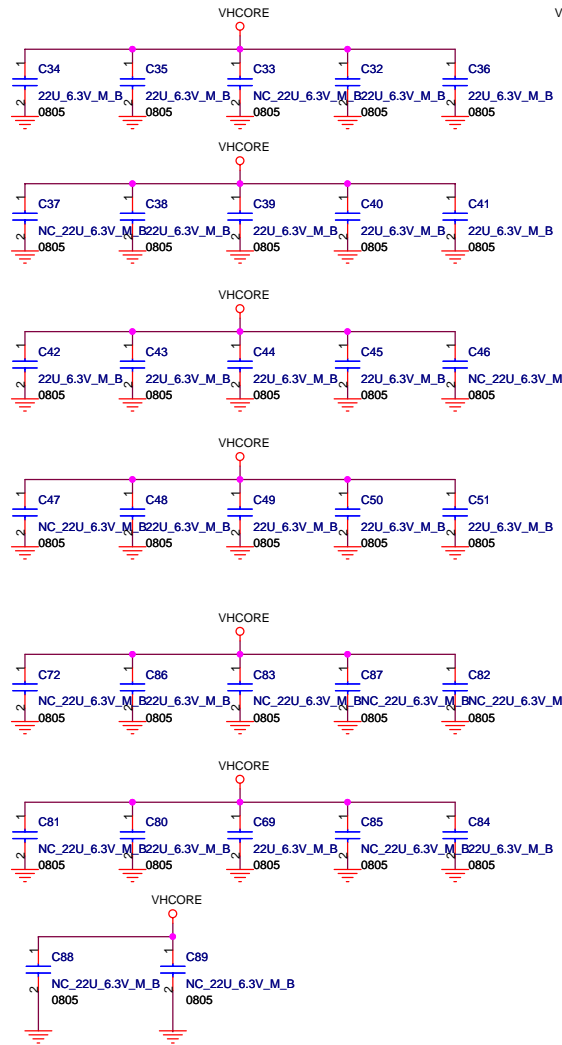
Layout Note:  
Zo=55 ohm, 0.5"  
max for GTLREF.

Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection. TEST4 and TEST6 and TEST7 pins can be left NC.

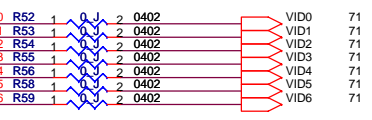
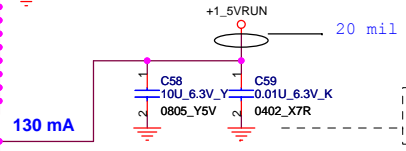
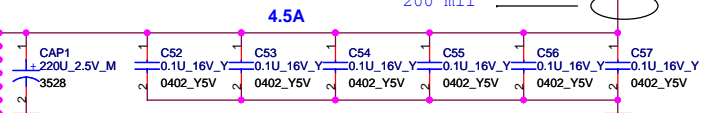


Layout Note:  
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5". Width=19mil(MS)  
Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5". Width=5mil(MS)



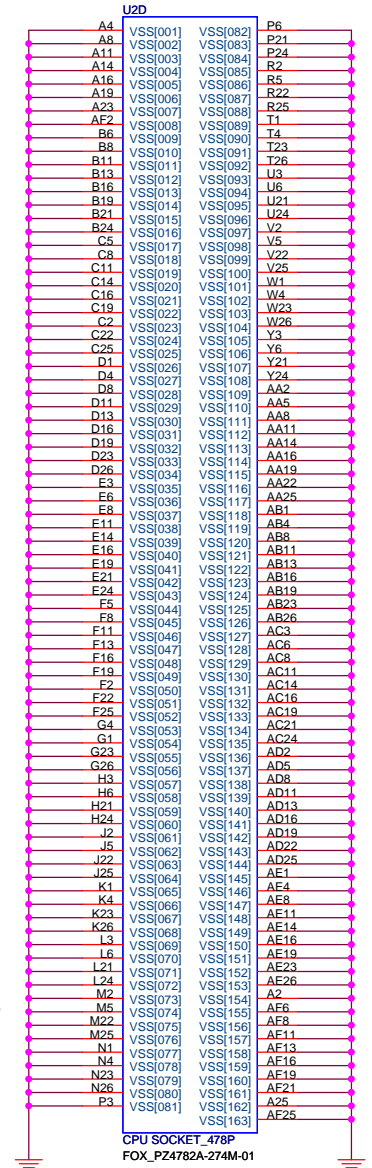


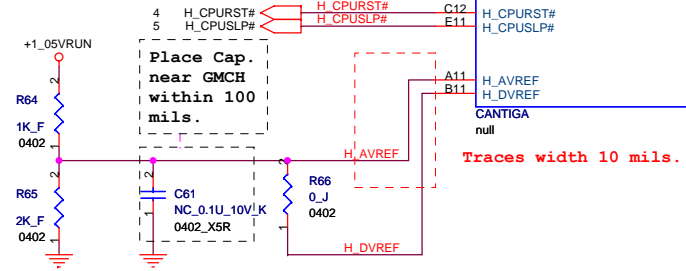
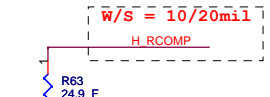
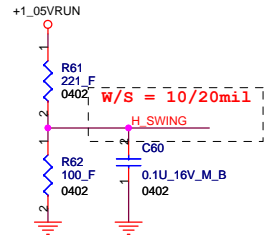
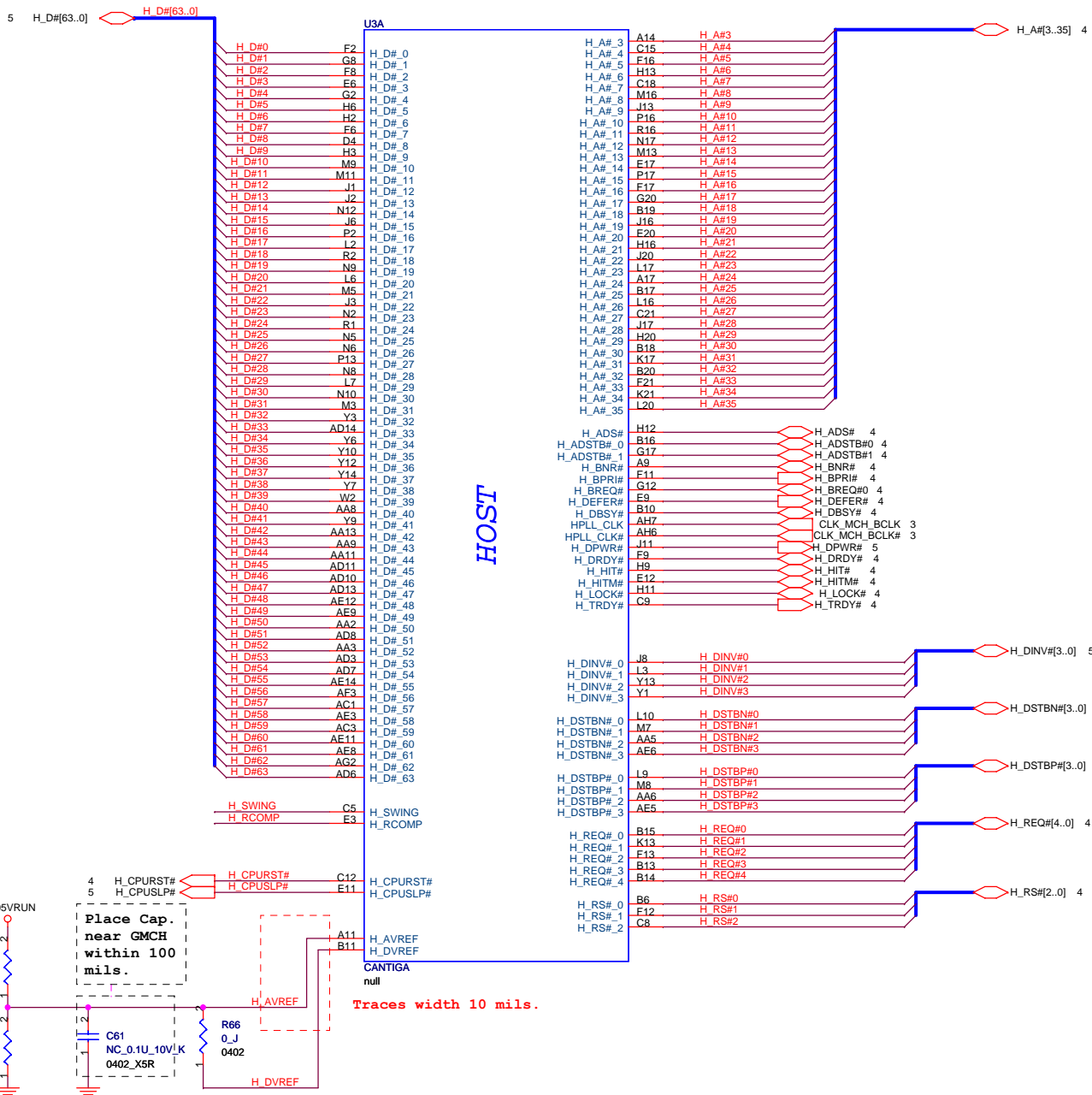
CPU\_VCCA---->0.13A  
 CPU\_VCCP---->4.5A  
 CPU\_VCC---->47A



Layout Note: Route VCCSENSE & VSSSENSE traces at 27.4 Ohms with 25 mil spacing to other signals. Place PU and PD within 2 inch of CPU.

Outer width=19 mil spacing=7 mil  
 Inner width=14 mil spacing=7 mil  
 Length match < 25 mil

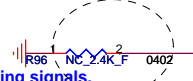




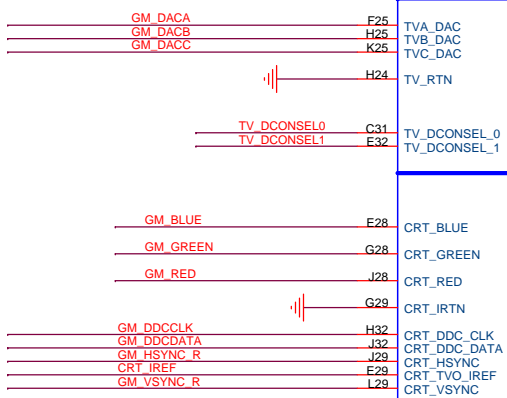
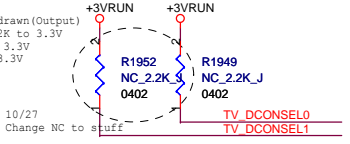




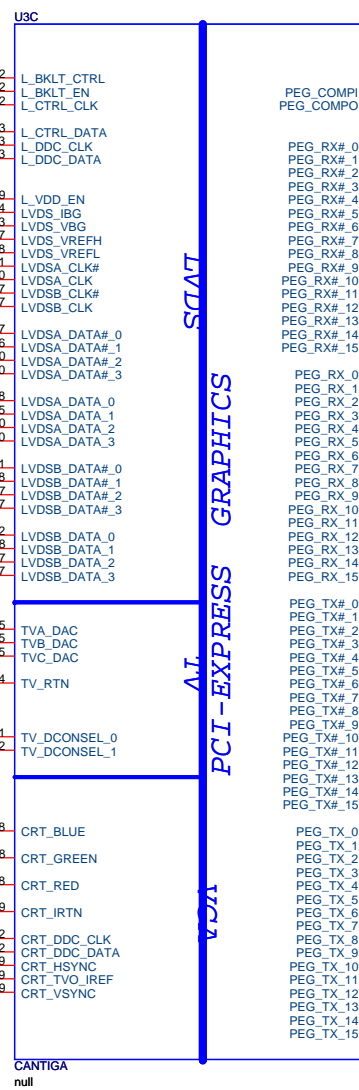
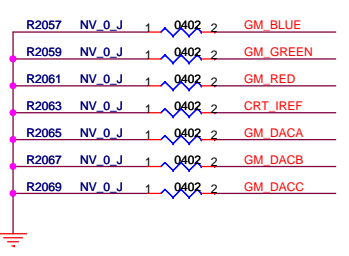
20 mils away from toggling signals.



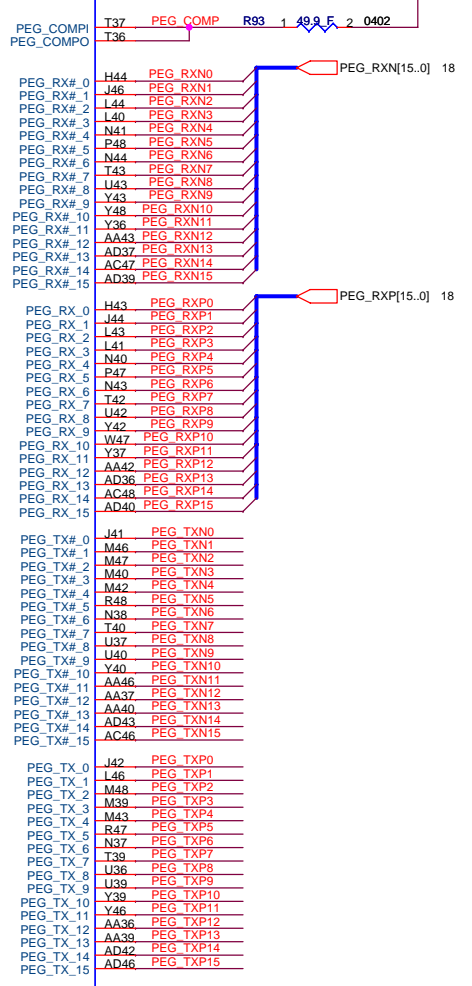
TYPE is open drawn(Output)  
Check list 2.2K to 3.3V  
MS90 2.2K to 3.3V  
CRB 2.2K to 3.3V



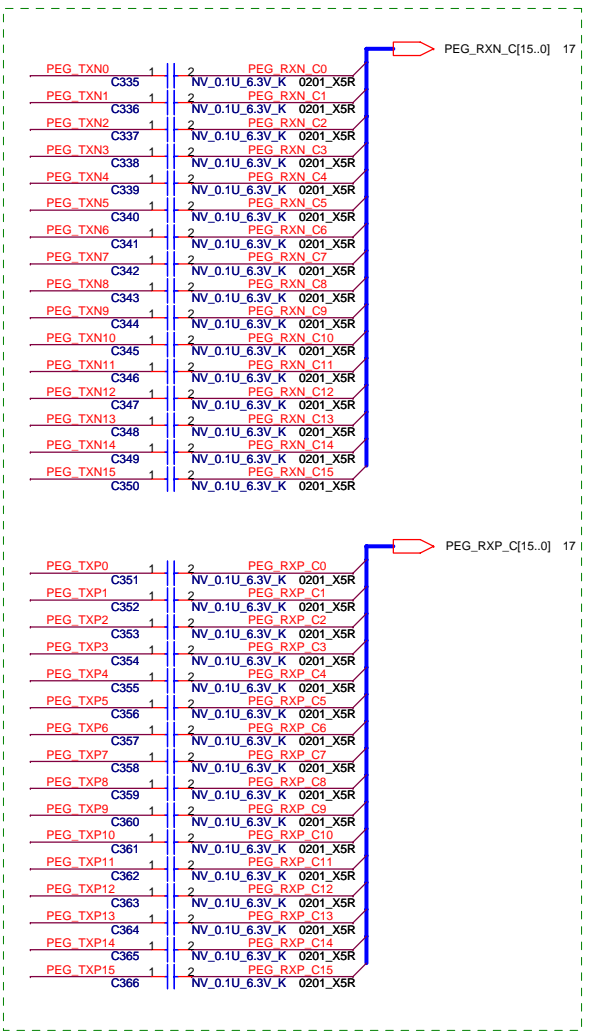
External Graphics (GMCH CRT/TVOUT Disable)



SATA  
PCI-EXPRESS  
GRAPHICS  
A.T.  
VIA



214. (Page 9) 07/11/28 Change PCIE Capacitor size from 0402 to 0201



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Title: **Cantiga (GRAPHIC) 3/7**

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14 M\_A\_DQ[63..0]

M A DQ0	AJ38	SA_DQ_0
M A DQ1	AJ41	SA_DQ_1
M A DQ2	AN38	SA_DQ_2
M A DQ3	AM38	SA_DQ_3
M A DQ4	AJ36	SA_DQ_4
M A DQ5	AJ40	SA_DQ_5
M A DQ6	AM44	SA_DQ_6
M A DQ7	AM42	SA_DQ_7
M A DQ8	AN43	SA_DQ_8
M A DQ9	AN44	SA_DQ_9
M A DQ10	AU40	SA_DQ_10
M A DQ11	AT38	SA_DQ_11
M A DQ12	AN41	SA_DQ_12
M A DQ13	AN39	SA_DQ_13
M A DQ14	AU44	SA_DQ_14
M A DQ15	AU42	SA_DQ_15
M A DQ16	AV39	SA_DQ_16
M A DQ17	AY44	SA_DQ_17
M A DQ18	BA40	SA_DQ_18
M A DQ19	BD43	SA_DQ_19
M A DQ20	AV41	SA_DQ_20
M A DQ21	AY43	SA_DQ_21
M A DQ22	BB41	SA_DQ_22
M A DQ23	BC40	SA_DQ_23
M A DQ24	AY37	SA_DQ_24
M A DQ25	BD38	SA_DQ_25
M A DQ26	AY37	SA_DQ_26
M A DQ27	AT36	SA_DQ_27
M A DQ28	AY38	SA_DQ_28
M A DQ29	BB38	SA_DQ_29
M A DQ30	AV36	SA_DQ_30
M A DQ31	AW36	SA_DQ_31
M A DQ32	BD13	SA_DQ_32
M A DQ33	AU11	SA_DQ_33
M A DQ34	BC11	SA_DQ_34
M A DQ35	BA12	SA_DQ_35
M A DQ36	AU13	SA_DQ_36
M A DQ37	AV13	SA_DQ_37
M A DQ38	BD12	SA_DQ_38
M A DQ39	BC12	SA_DQ_39
M A DQ40	BB9	SA_DQ_40
M A DQ41	BA9	SA_DQ_41
M A DQ42	AU10	SA_DQ_42
M A DQ43	AV9	SA_DQ_43
M A DQ44	BA11	SA_DQ_44
M A DQ45	BD9	SA_DQ_45
M A DQ46	AV8	SA_DQ_46
M A DQ47	BA6	SA_DQ_47
M A DQ48	AV5	SA_DQ_48
M A DQ49	AV7	SA_DQ_49
M A DQ50	AT9	SA_DQ_50
M A DQ51	AN8	SA_DQ_51
M A DQ52	AU5	SA_DQ_52
M A DQ53	AU6	SA_DQ_53
M A DQ54	AT5	SA_DQ_54
M A DQ55	AN10	SA_DQ_55
M A DQ56	AM11	SA_DQ_56
M A DQ57	AM5	SA_DQ_57
M A DQ58	AJ9	SA_DQ_58
M A DQ59	AJ8	SA_DQ_59
M A DQ60	AN12	SA_DQ_60
M A DQ61	AM13	SA_DQ_61
M A DQ62	AJ11	SA_DQ_62
M A DQ63	AJ12	SA_DQ_63

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DDR SYSTEM MEMORY A

SA_BS_0	BD21	M_A_BS0	14,16
SA_BS_1	BG18	M_A_BS1	14,16
SA_BS_2	AT25	M_A_BS2	14,16
SA_RAS#	BB20	M_A_RAS#	14,16
SA_CAS#	BD20	M_A_CAS#	14,16
SA_WE#	AY20	M_A_WE#	14,16
SA_DM_0	AM37	M_A_DM0	14
SA_DM_1	AT141	M_A_DM1	14
SA_DM_2	AY41	M_A_DM2	14
SA_DM_3	AU39	M_A_DM3	14
SA_DM_4	BB12	M_A_DM4	14
SA_DM_5	AY6	M_A_DM5	14
SA_DM_6	AT7	M_A_DM6	14
SA_DM_7	AJ5	M_A_DM7	14
SA_DQS_0	AJ44	M_A_DQS0	14
SA_DQS_1	AT144	M_A_DQS1	14
SA_DQS_2	BA43	M_A_DQS2	14
SA_DQS_3	BC37	M_A_DQS3	14
SA_DQS_4	AW12	M_A_DQS4	14
SA_DQS_5	BC8	M_A_DQS5	14
SA_DQS_6	AU8	M_A_DQS6	14
SA_DQS_7	AM7	M_A_DQS7	14
SA_DQS#_0	AJ43	M_A_DQS#0	14
SA_DQS#_1	AT143	M_A_DQS#1	14
SA_DQS#_2	BA44	M_A_DQS#2	14
SA_DQS#_3	BD37	M_A_DQS#3	14
SA_DQS#_4	AY12	M_A_DQS#4	14
SA_DQS#_5	BD8	M_A_DQS#5	14
SA_DQS#_6	AU9	M_A_DQS#6	14
SA_DQS#_7	AM8	M_A_DQS#7	14
SA_MA_0	BA21	M_A_A0	14,16
SA_MA_1	BC24	M_A_A1	14,16
SA_MA_2	BC24	M_A_A2	14,16
SA_MA_3	BH24	M_A_A3	14,16
SA_MA_4	BG25	M_A_A4	14,16
SA_MA_5	BA24	M_A_A5	14,16
SA_MA_6	BD24	M_A_A6	14,16
SA_MA_7	BG27	M_A_A7	14,16
SA_MA_8	BF25	M_A_A8	14,16
SA_MA_9	AW24	M_A_A9	14,16
SA_MA_10	BC21	M_A_A10	14,16
SA_MA_11	BG26	M_A_A11	14,16
SA_MA_12	BH26	M_A_A12	14,16
SA_MA_13	BH17	M_A_A13	14,16
SA_MA_14	AY25	M_A_A14	14,16

15 M\_B\_DQ[63..0]

M B DQ0	AK47	SB_DQ_0
M B DQ1	AH46	SB_DQ_1
M B DQ2	AP47	SB_DQ_2
M B DQ3	AP46	SB_DQ_3
M B DQ4	AJ46	SB_DQ_4
M B DQ5	AJ48	SB_DQ_5
M B DQ6	AM48	SB_DQ_6
M B DQ7	AP48	SB_DQ_7
M B DQ8	AJ47	SB_DQ_8
M B DQ9	AU46	SB_DQ_9
M B DQ10	BA48	SB_DQ_10
M B DQ11	AY48	SB_DQ_11
M B DQ12	AT147	SB_DQ_12
M B DQ13	AR47	SB_DQ_13
M B DQ14	BA47	SB_DQ_14
M B DQ15	BC47	SB_DQ_15
M B DQ16	BC46	SB_DQ_16
M B DQ17	BC44	SB_DQ_17
M B DQ18	BG43	SB_DQ_18
M B DQ19	BF43	SB_DQ_19
M B DQ20	BE45	SB_DQ_20
M B DQ21	BC41	SB_DQ_21
M B DQ22	BF40	SB_DQ_22
M B DQ23	BF41	SB_DQ_23
M B DQ24	BG38	SB_DQ_24
M B DQ25	BF38	SB_DQ_25
M B DQ26	BH35	SB_DQ_26
M B DQ27	BG35	SB_DQ_27
M B DQ28	BH40	SB_DQ_28
M B DQ29	BG39	SB_DQ_29
M B DQ30	BG34	SB_DQ_30
M B DQ31	BH34	SB_DQ_31
M B DQ32	BH14	SB_DQ_32
M B DQ33	BG12	SB_DQ_33
M B DQ34	BH11	SB_DQ_34
M B DQ35	BG8	SB_DQ_35
M B DQ36	BH12	SB_DQ_36
M B DQ37	BF11	SB_DQ_37
M B DQ38	BF8	SB_DQ_38
M B DQ39	BC7	SB_DQ_39
M B DQ40	BC5	SB_DQ_40
M B DQ41	BC6	SB_DQ_41
M B DQ42	AY3	SB_DQ_42
M B DQ43	AY1	SB_DQ_43
M B DQ44	BF6	SB_DQ_44
M B DQ45	BF5	SB_DQ_45
M B DQ46	BA1	SB_DQ_46
M B DQ47	BD3	SB_DQ_47
M B DQ48	AV2	SB_DQ_48
M B DQ49	AU3	SB_DQ_49
M B DQ50	AR3	SB_DQ_50
M B DQ51	AN2	SB_DQ_51
M B DQ52	AY2	SB_DQ_52
M B DQ53	AV1	SB_DQ_53
M B DQ54	AP3	SB_DQ_54
M B DQ55	AR1	SB_DQ_55
M B DQ56	AL1	SB_DQ_56
M B DQ57	AL2	SB_DQ_57
M B DQ58	AH1	SB_DQ_58
M B DQ59	AH1	SB_DQ_59
M B DQ60	AM2	SB_DQ_60
M B DQ61	AM3	SB_DQ_61
M B DQ62	AH3	SB_DQ_62
M B DQ63	AJ3	SB_DQ_63

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DDR SYSTEM MEMORY B

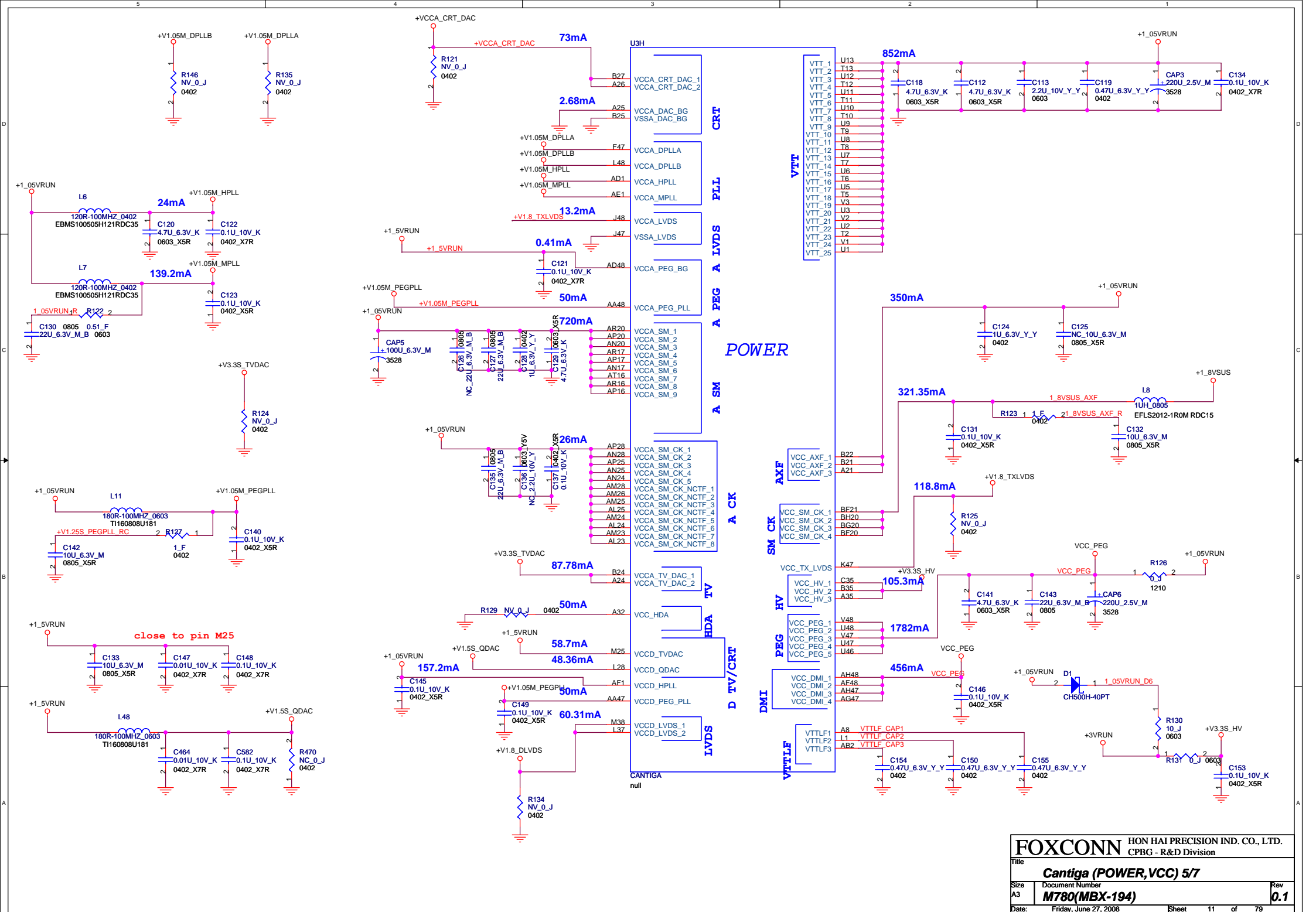
SB_BS_0	BC16	M_B_BS0	15,16
SB_BS_1	BB17	M_B_BS1	15,16
SB_BS_2	BB33	M_B_BS2	15,16
SB_RAS#	AU17	M_B_RAS#	15,16
SB_CAS#	BG16	M_B_CAS#	15,16
SB_WE#	BF14	M_B_WE#	15,16
SB_DM_0	AM47	M_B_DM0	15
SB_DM_1	AY47	M_B_DM1	15
SB_DM_2	BD40	M_B_DM2	15
SB_DM_3	BF35	M_B_DM3	15
SB_DM_4	BG11	M_B_DM4	15
SB_DM_5	BA3	M_B_DM5	15
SB_DM_6	AP1	M_B_DM6	15
SB_DM_7	AK2	M_B_DM7	15
SB_DQS_0	AJ47	M_B_DQS0	15
SB_DQS_1	AV48	M_B_DQS1	15
SB_DQS_2	BG41	M_B_DQS2	15
SB_DQS_3	BG37	M_B_DQS3	15
SB_DQS_4	BH9	M_B_DQS4	15
SB_DQS_5	BB2	M_B_DQS5	15
SB_DQS_6	AU1	M_B_DQS6	15
SB_DQS_7	AN6	M_B_DQS7	15
SB_DQS#_0	AL46	M_B_DQS#0	15
SB_DQS#_1	AV47	M_B_DQS#1	15
SB_DQS#_2	BH41	M_B_DQS#2	15
SB_DQS#_3	BH37	M_B_DQS#3	15
SB_DQS#_4	BG9	M_B_DQS#4	15
SB_DQS#_5	BC2	M_B_DQS#5	15
SB_DQS#_6	AT2	M_B_DQS#6	15
SB_DQS#_7	AN5	M_B_DQS#7	15
SB_MA_0	AV17	M_B_A0	15,16
SB_MA_1	BA25	M_B_A1	15,16
SB_MA_2	BC25	M_B_A2	15,16
SB_MA_3	AU25	M_B_A3	15,16
SB_MA_4	AW25	M_B_A4	15,16
SB_MA_5	BB28	M_B_A5	15,16
SB_MA_6	AU28	M_B_A6	15,16
SB_MA_7	AV28	M_B_A7	15,16
SB_MA_8	AT33	M_B_A8	15,16
SB_MA_9	BD33	M_B_A9	15,16
SB_MA_10	BB16	M_B_A10	15,16
SB_MA_11	AW33	M_B_A11	15,16
SB_MA_12	AY33	M_B_A12	15,16
SB_MA_13	BH15	M_B_A13	15,16
SB_MA_14	AU33	M_B_A14	15,16

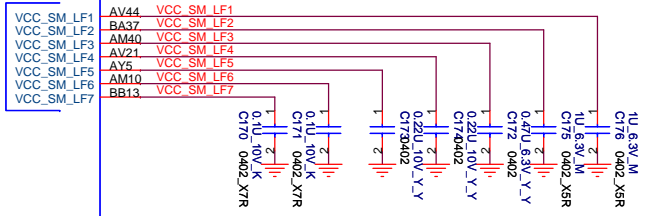
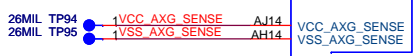
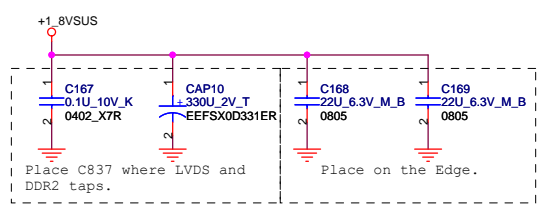
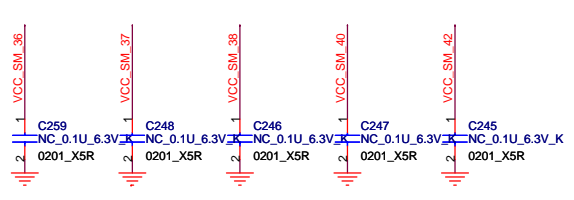
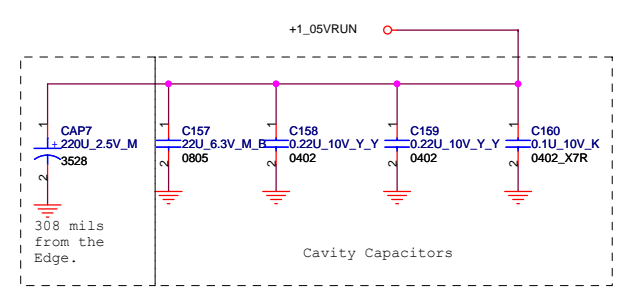
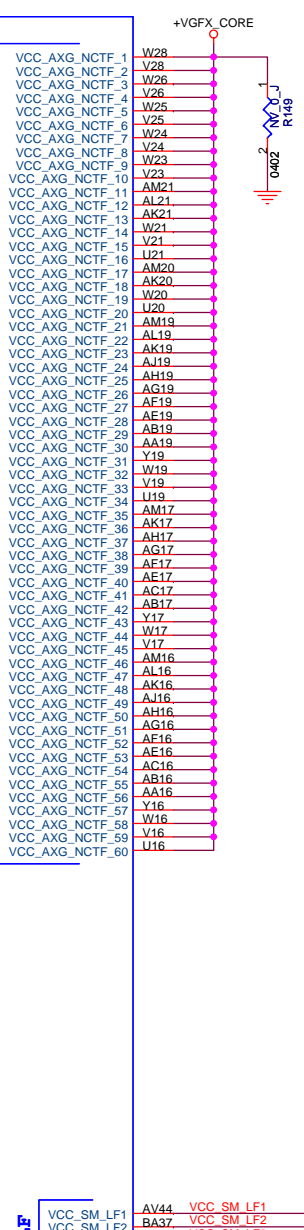
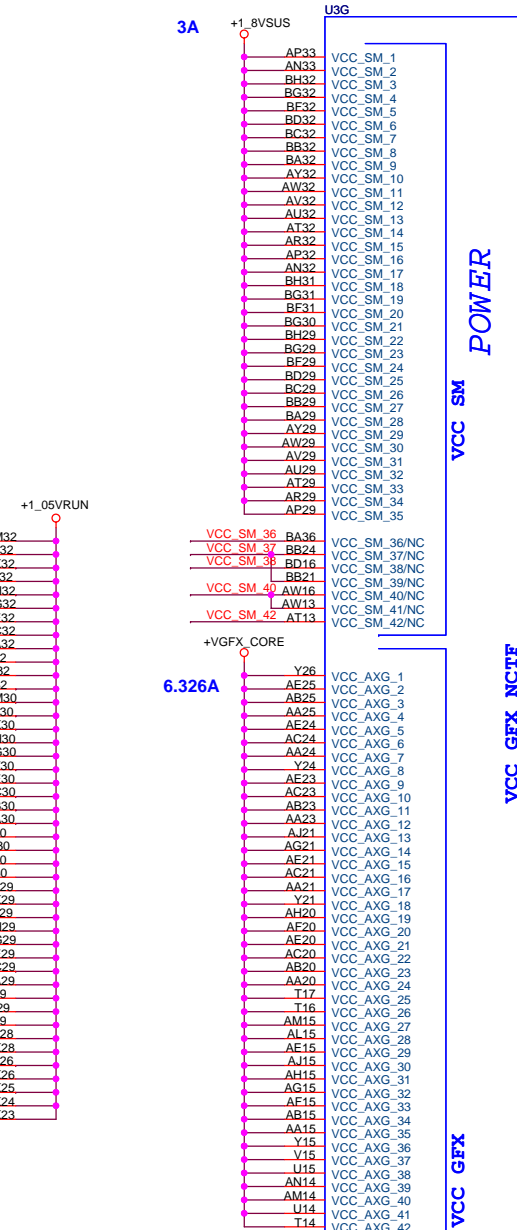
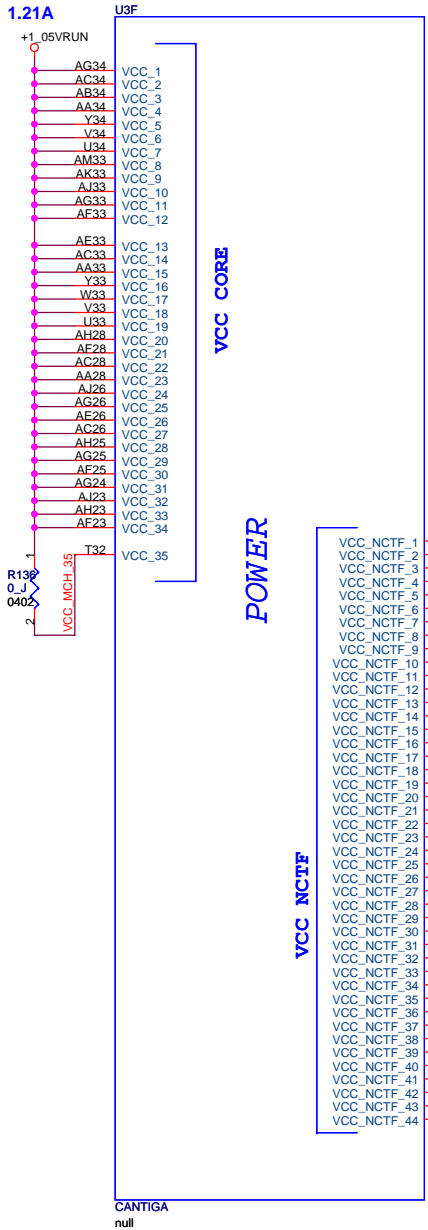
**FOXCONN** HON HAI PRECISION IND. CO., LTD.  
CPBG - R&D Division

Title: **Cantiga (DDRII) 4/7**

Size: A3 Document Number: **M780(MBX-194)** Rev: **0.1**

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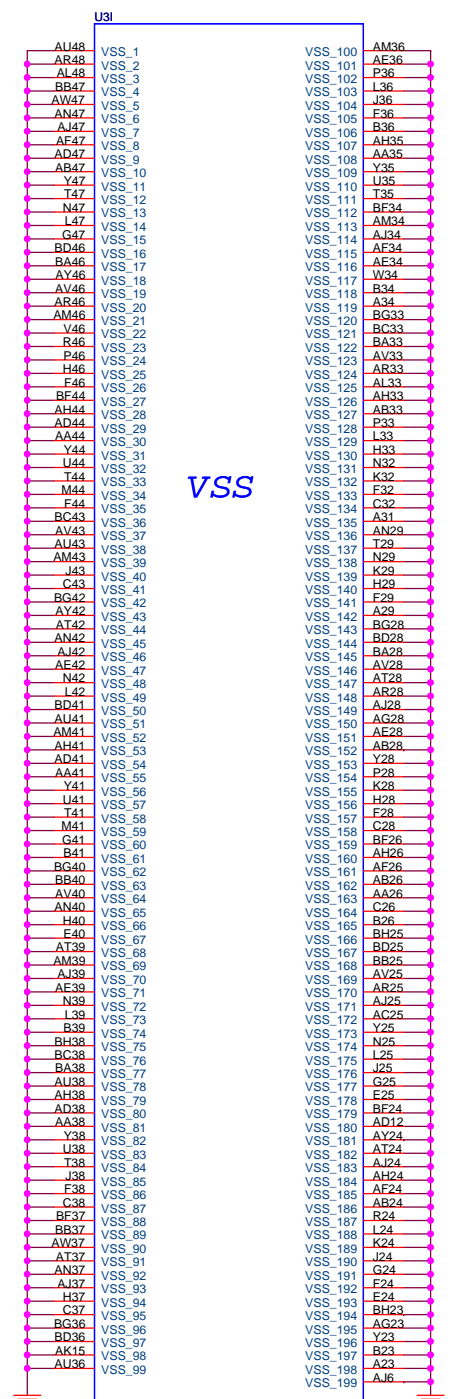


**FOXCONN** HON HAI PRECISION IND. CO., LTD.  
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Title: **Cantiga (VCC CORE) 6/7**

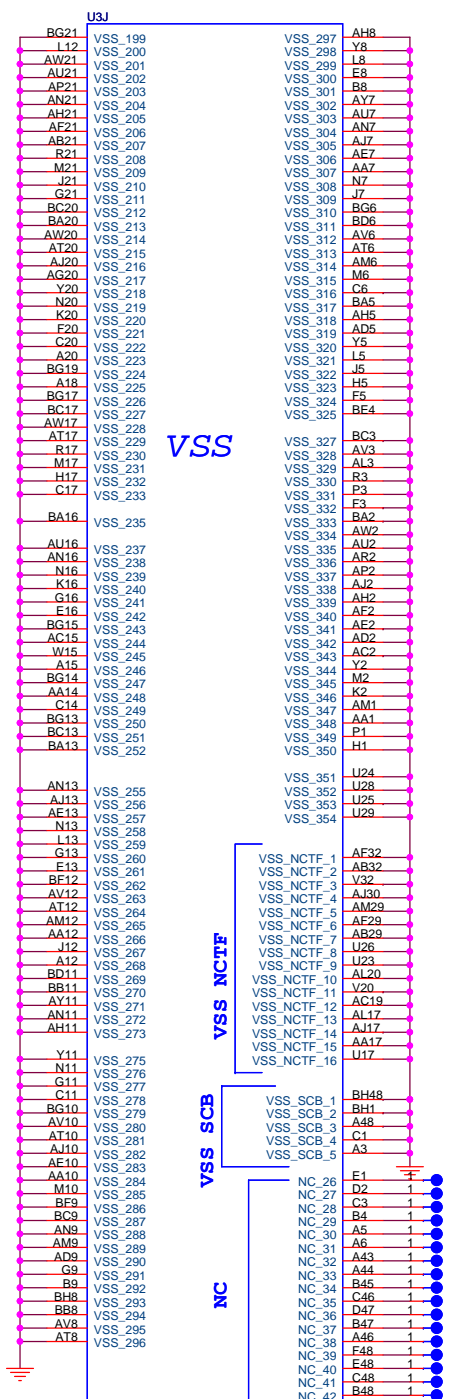
Size: A3 Document Number: **M780(MBX-194)** Rev: **0.1**

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VSS

CANTIGA null



VSS

VSS NCTF

VSS SCB

NC

CANTIGA null

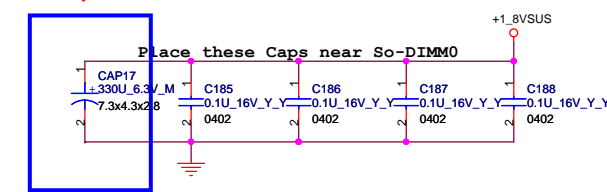
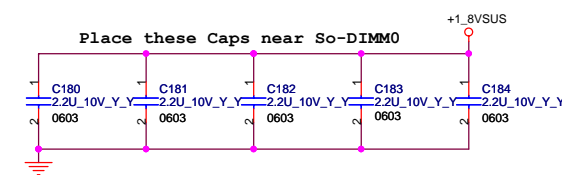
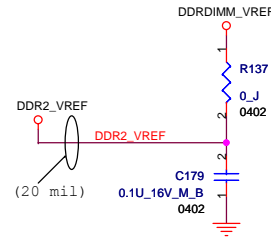
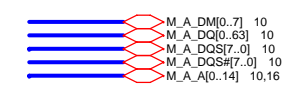
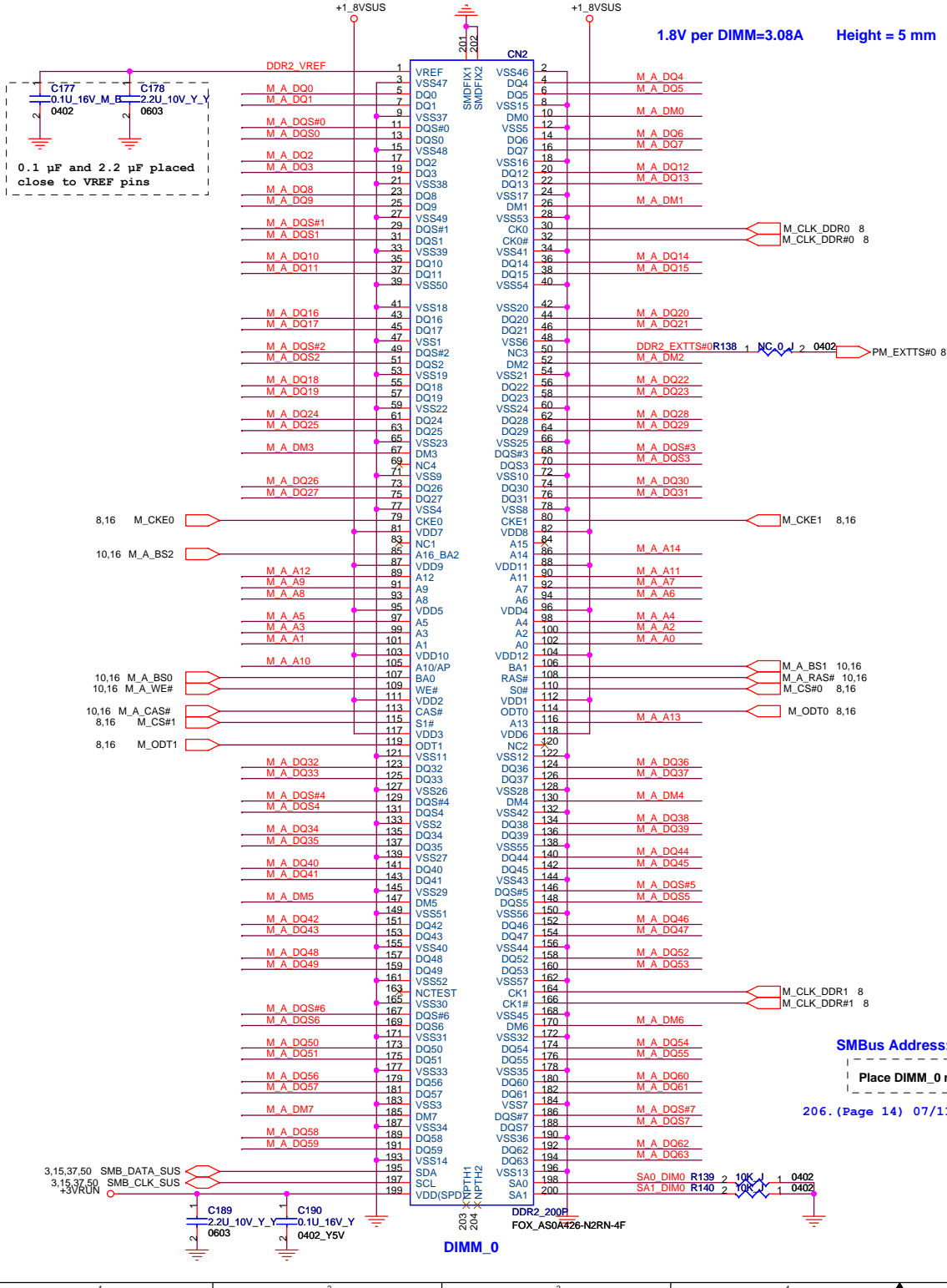


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Title: **Cantiga (VSS) 7/7**

Size: A3 Document Number: **M780(MBX-194)** Rev: **0.1**

Date: Friday, June 27, 2008 Sheet: 13 of 79

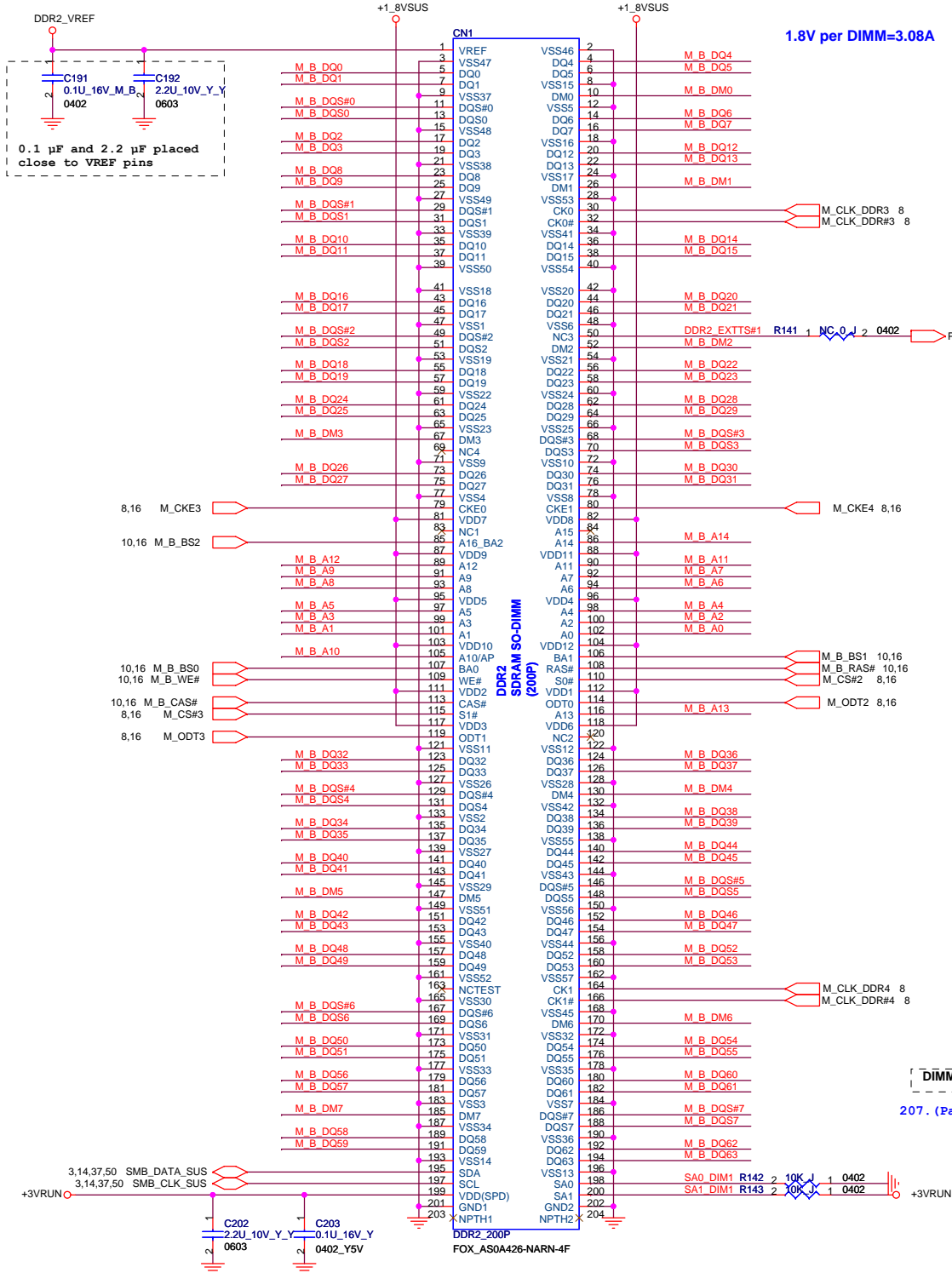


SMBus Address: A0H(W)/A1H(R)

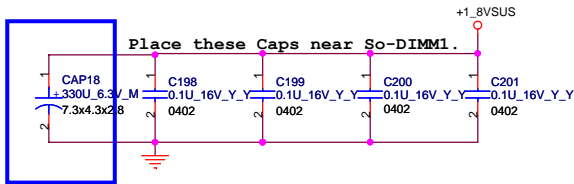
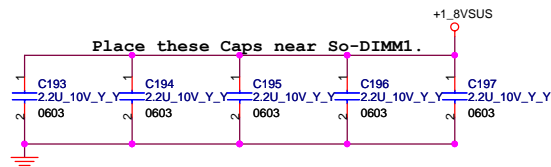
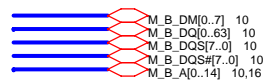
Place DIMM\_0 near GMCH

206. (Page 14) 07/11/27 change DDR2 CONN(CN1) from FOX\_AS0A426-N5SN-7F to FOX\_AS0A426\_MN2RN\_7F

<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title <b>DDR(II)SO-DIMM_0</b>			
Size Document Number			
Date: <b>M780(MBX-194)</b>			
Date: Friday, June 13, 2008		Sheet 14 of 79	
		Rev <b>0.1</b>	



1.8V per DIMM=3.08A Height = 4 mm

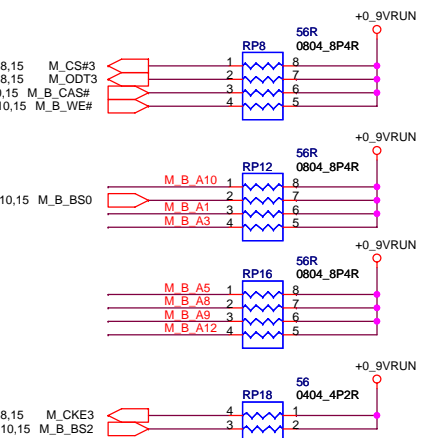
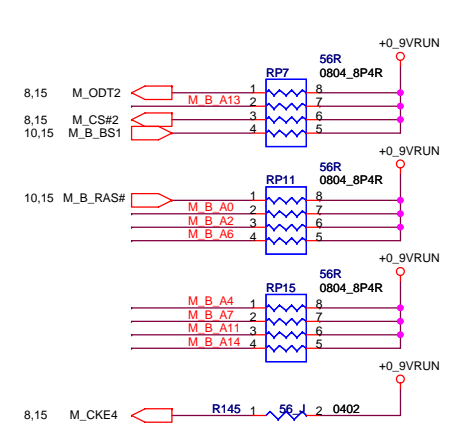
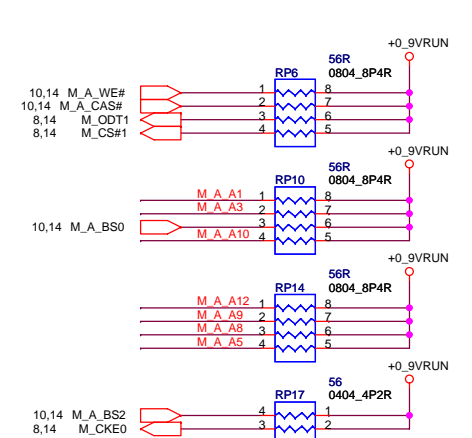
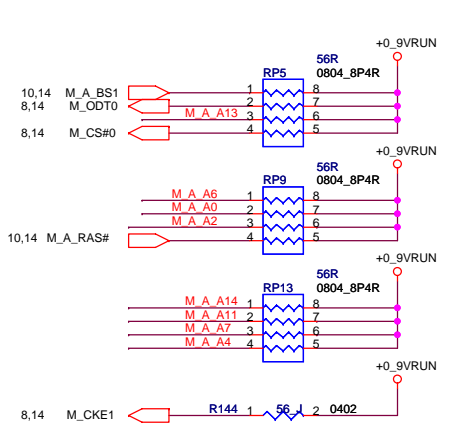
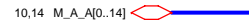
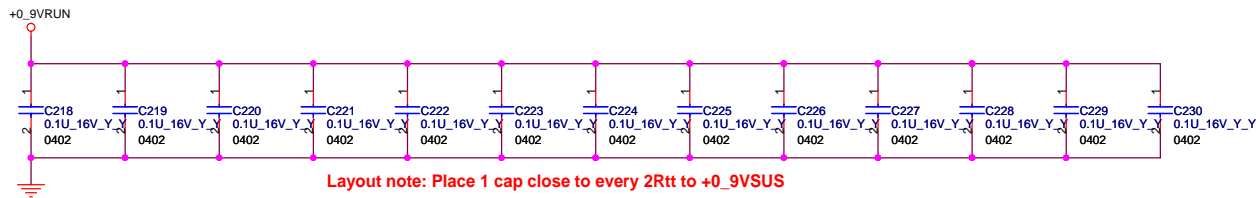
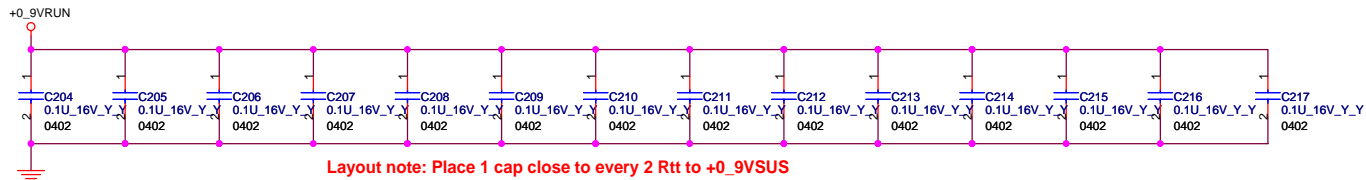


SMBus Address: A4(W)/A5(R)

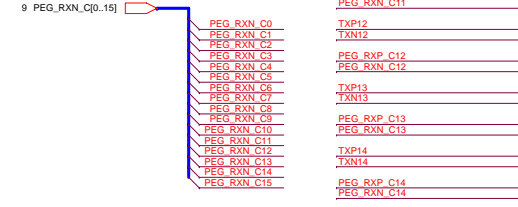
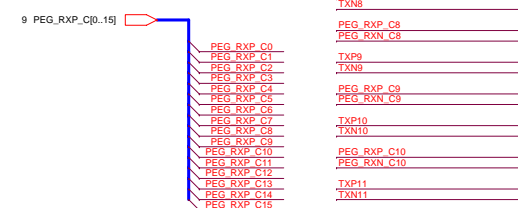
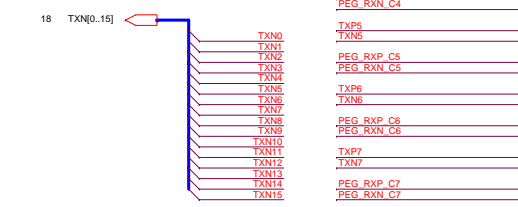
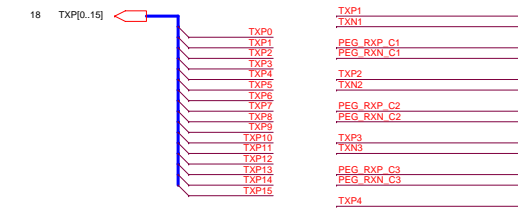
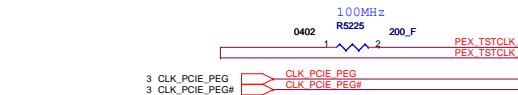
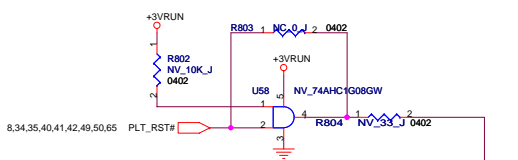
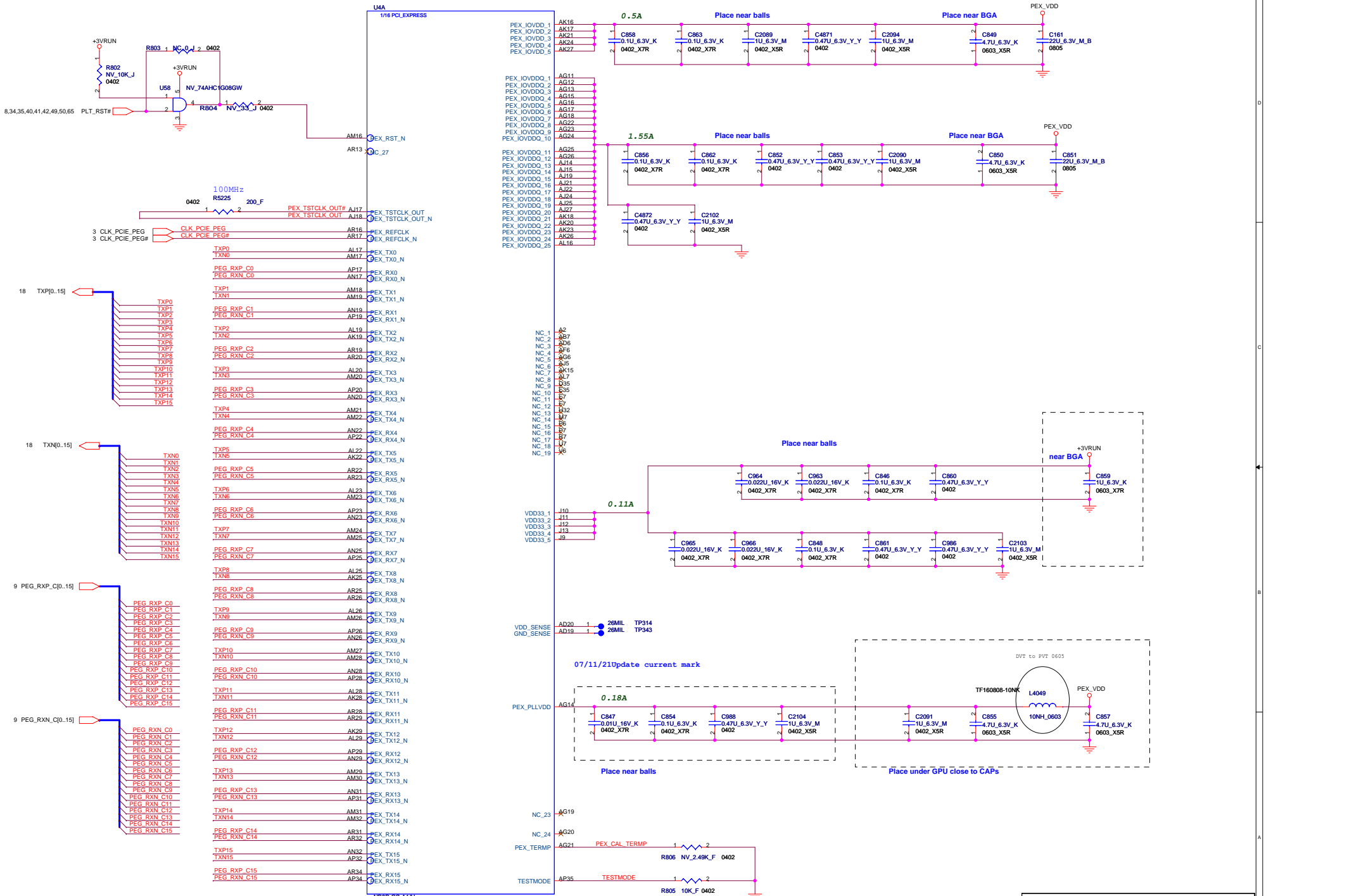
DIMM\_1 is placed farther from the GMCH than DIMM\_0

207. (Page 14) 07/11/27 change DDR2 CONN(CN2) from FOX\_AS0A426\_N4RC\_4F to FOX\_AS0A426\_MARN\_7F

<b>FOXCONN</b> HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		Title <b>DDR(II)SO-DIMM_1</b>
		Document Number <b>M780(MBX-194)</b>
Size A3	Date Friday, June 13, 2008	Rev <b>0.1</b>
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<b>XCLK_277</b>	
0 (Reserved)	
1 (27M Hz)	
<b>NB9X TVMODE[2:0]</b>	
000	
<b>SUB_VENDOR</b>	
0 (No vedio BIOS ROM)	ROM_SI (XXXX)
1 (BIOS ROM is present)	
<b>SLOT_CLK_CFG</b>	
0 (GPU and MCH not share a common reference clk)	ROM_SO (1000)
1 (GPU and MCH share a common reference clk)	
<b>PEX_PLL_EN_TERM</b>	
0 (Disable)	ROM_SCLK (0010)
1 (Enable)	
<b>USER[3:0]</b>	
1000	STRAP0 (1111)
<b>NB9X 3GIO_PADCFG[3:0]</b>	
0001	STRAP1 (0001)
<b>NB9X PCI_DEVID[4:0]</b>	
NB9P-GS X1001	STRAP2 (1001)
NB9M-GS X1001	

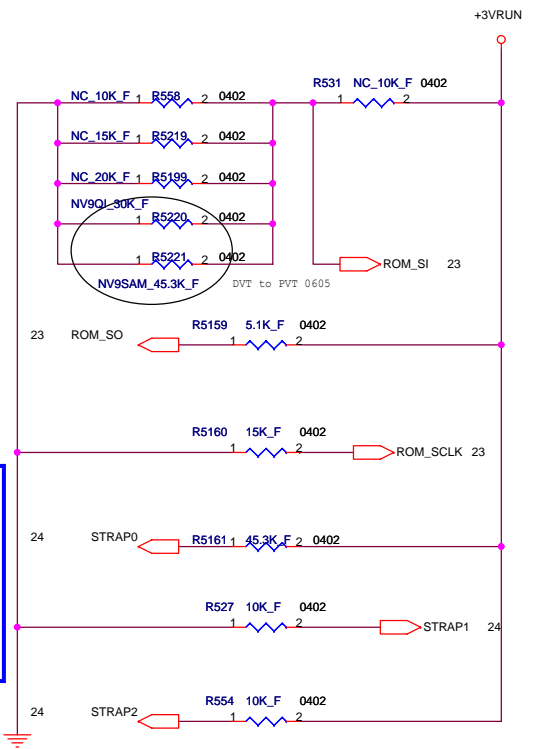
**<< ROM\_SI Setting condition >>**

**H Model**  
=> 32Mx32bx4 - 0101 Qimonda - 30K pull Low

**M Model**  
=> 32Mx32bx4 - 0101(Qimonda) - 30K pul Low

**L Model**  
=> 32Mx32bx2 - 0101 Qimonda - 30K pull Low

0100	64-bit Reserved
0101	32Mx32 GDDR3 - 136 ball - monolithic 64-bit Qimonda
0110	32Mx32 GDDR3 - 136 ball - monolithic 64-bit Hynix
0111	32Mx32 GDDR3 - 136 ball - monolithic 64-bit Samsung
0000	64-bit Reserved
0001	16Mx32 GDDR3 - 136 ball 64-bit Qimonda
0010	16Mx32 GDDR3 - 136 ball 64-bit Hynix
0011	16Mx32 GDDR3 - 136 ball 64-bit Samsung



**Logical Strap bit Mapping**

Resister values	Pull-up to VDD	Pull-down to GND
5KΩ	1000	0000
10KΩ	1001	0001
15KΩ	1010	0010
20KΩ	1011	0011
25KΩ	1100	0100
30KΩ	1101	0101
35KΩ	1110	0110
45KΩ	1111	0111

**Strap Options**

Physical Strapping pin	Power Rail	Logical Strapping pin3	Logical Strapping pin2	Logical Strapping pin1	Logical Strapping pin0
ROM_SI	+3VRUN	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
ROM_SO	+3VRUN	XCLK_277	TVMODE[2]	TVMODE[1]	TVMODE[0]
ROM_SCLK	+3VRUN	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
STRAP0	+3VRUN	USER[3]	USER[2]	USER[1]	USER[0]
STRAP1	+3VRUN	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP2	+3VRUN	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]

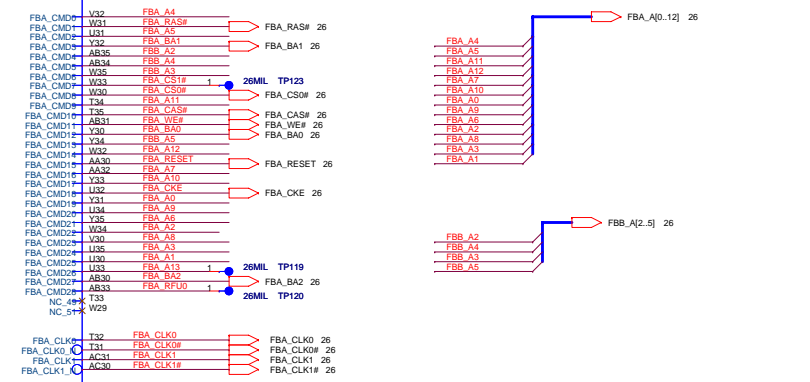
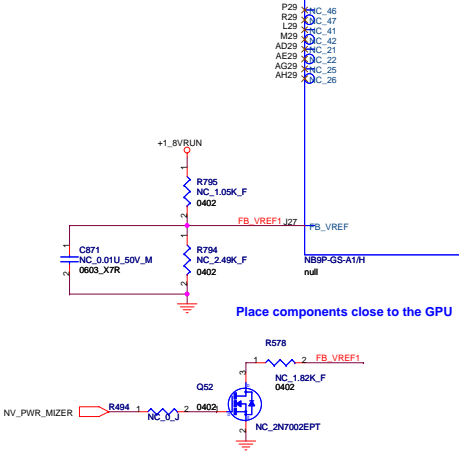
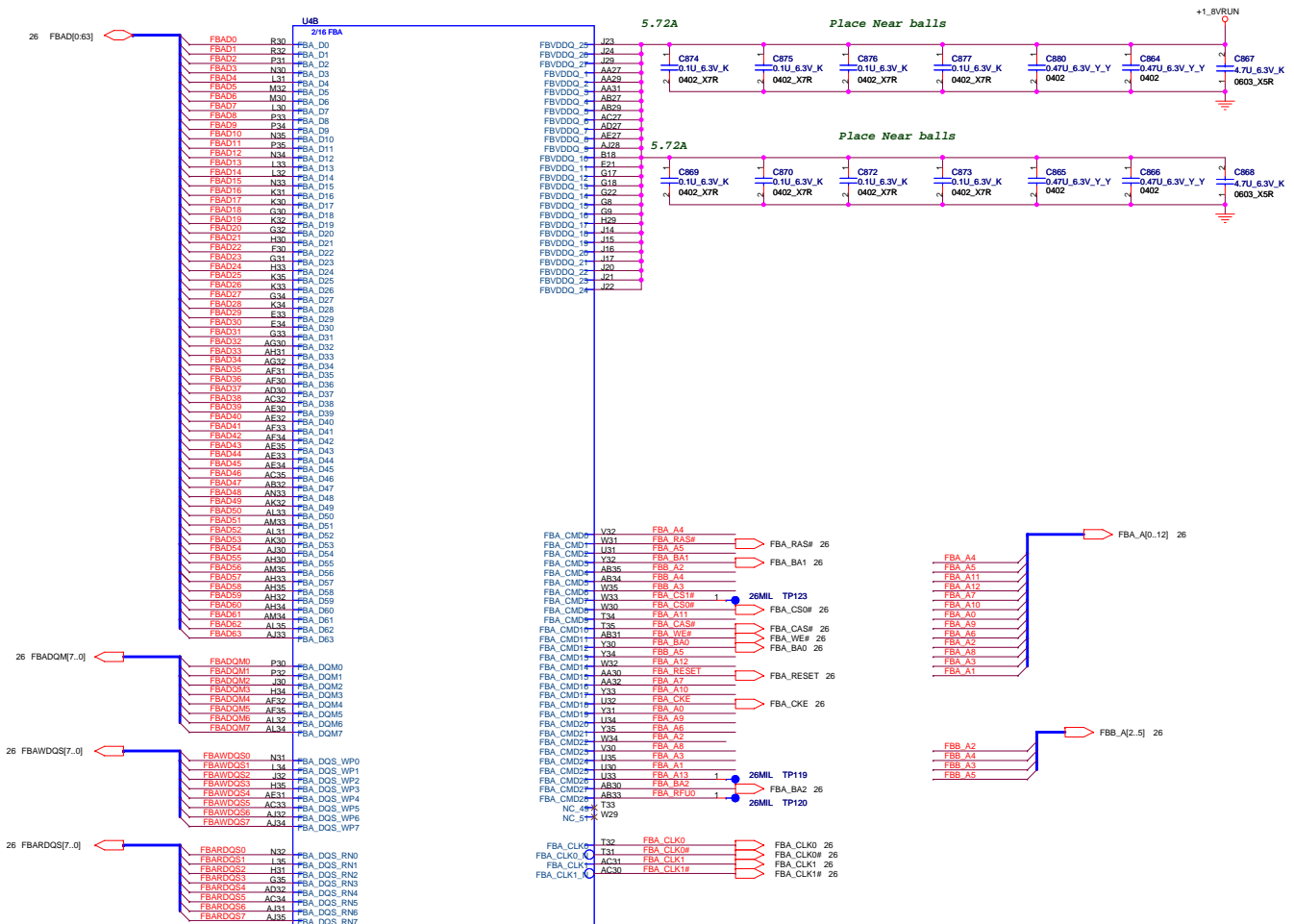
Refer to <GB1 Family Design Guide DG-03276-001\_v01\_secured>

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Title: **VGA (PCI-EXPRESS/STRAP) 2 OF 9**

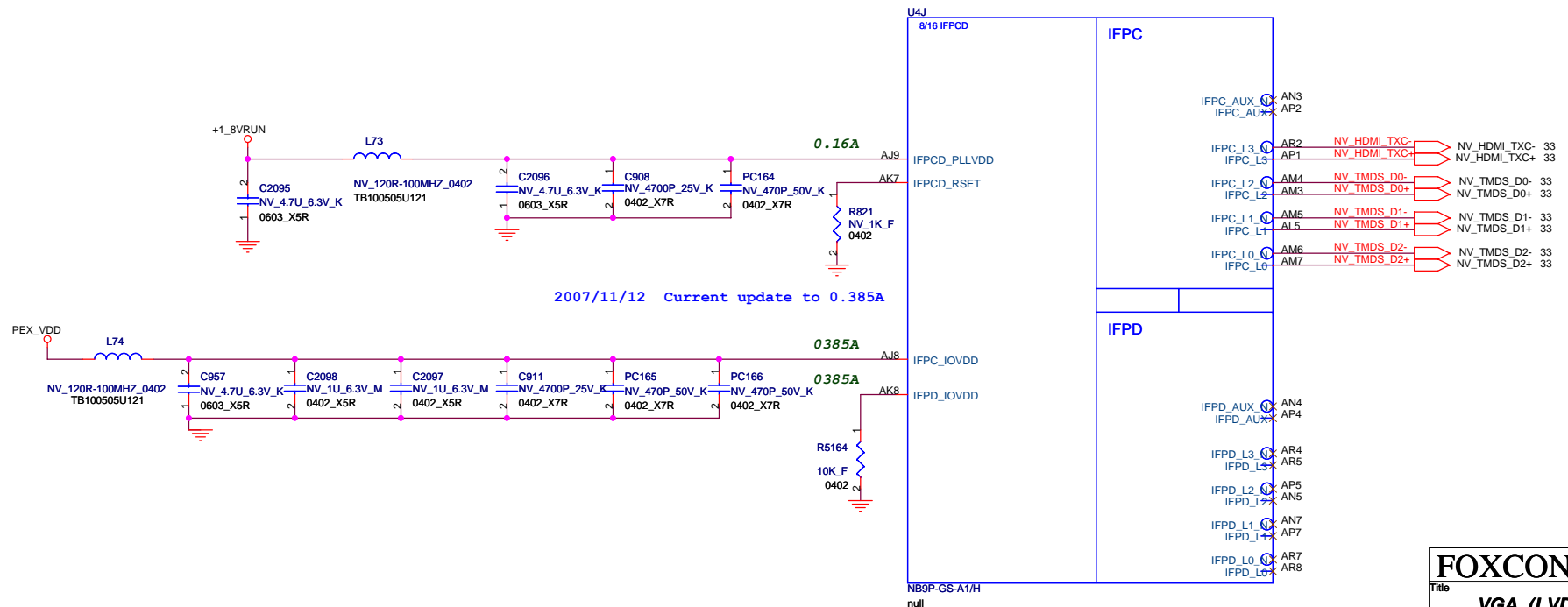
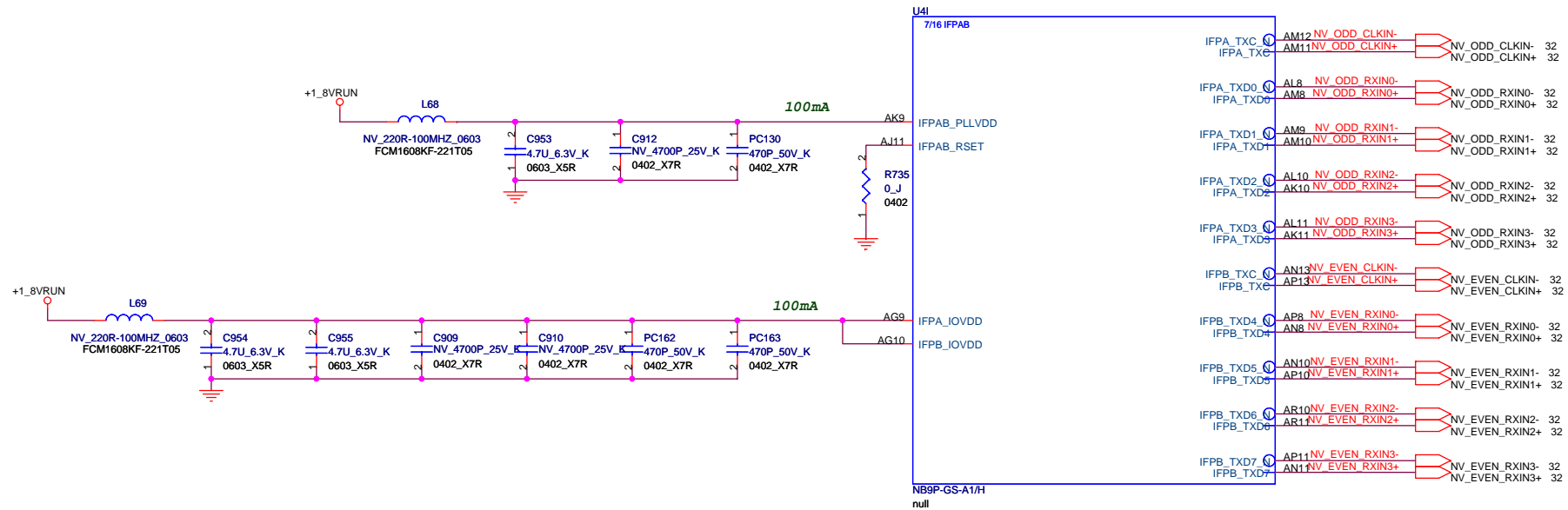
Size: Document Number **M780(MBX-194)** Rev **0.1**

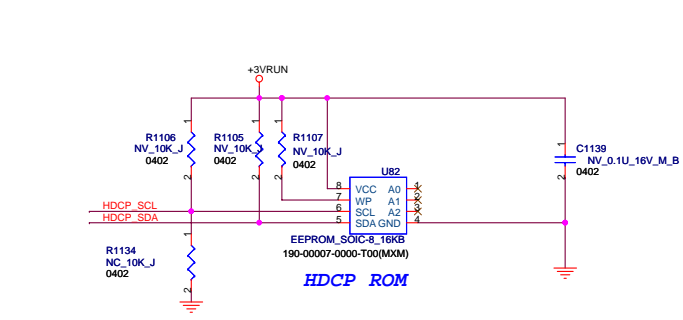
Date: Friday, June 13, 2008 Sheet 18 of 79



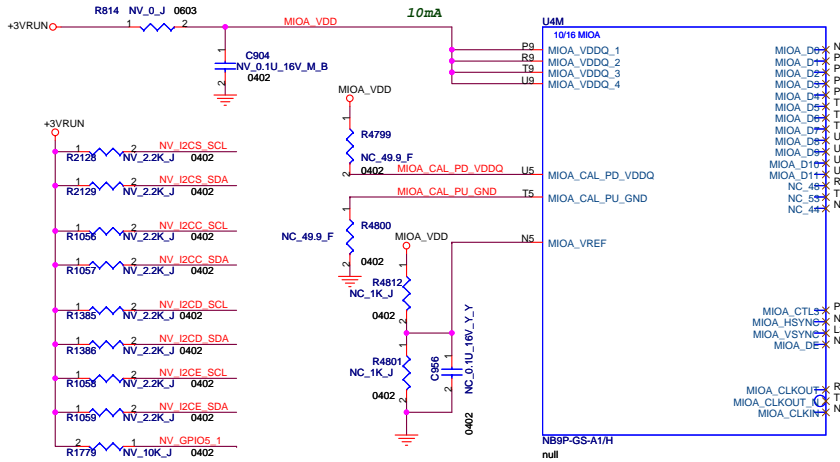
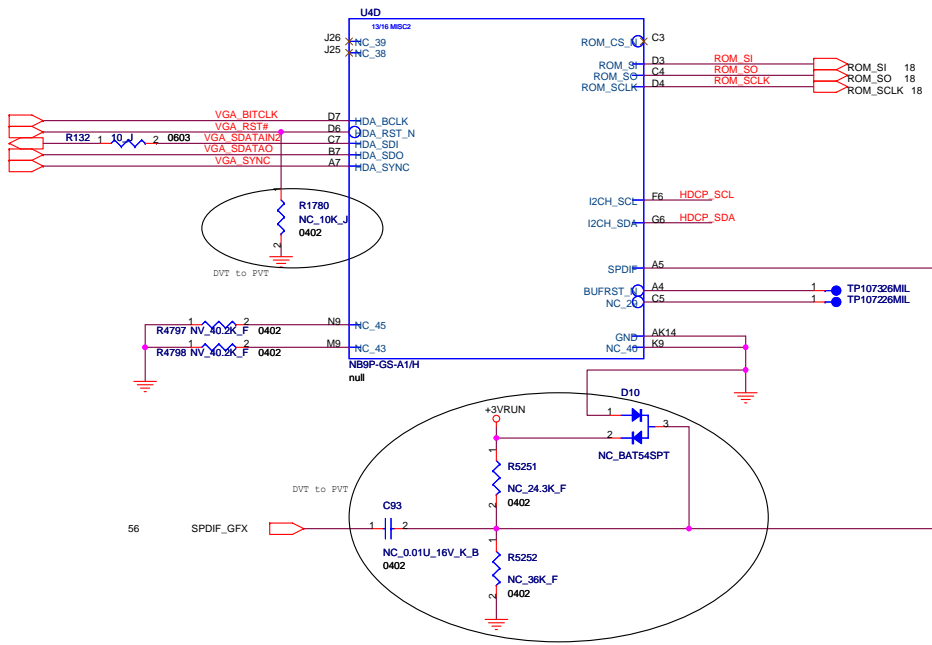




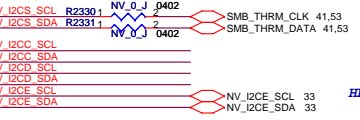
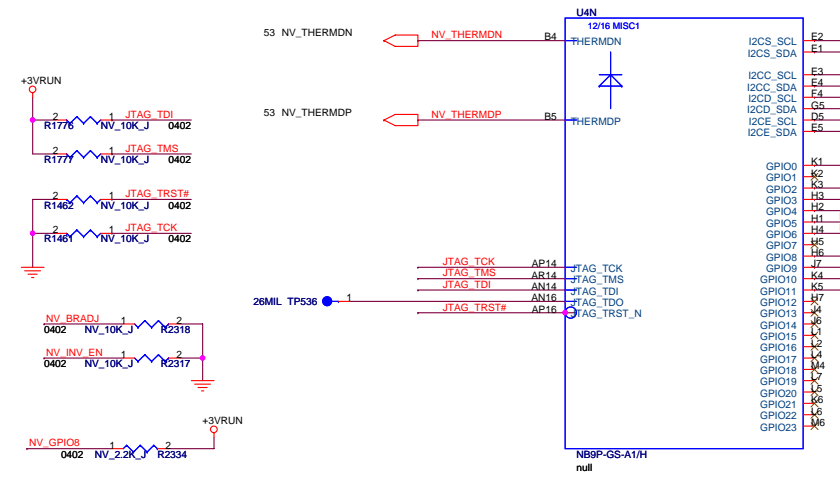




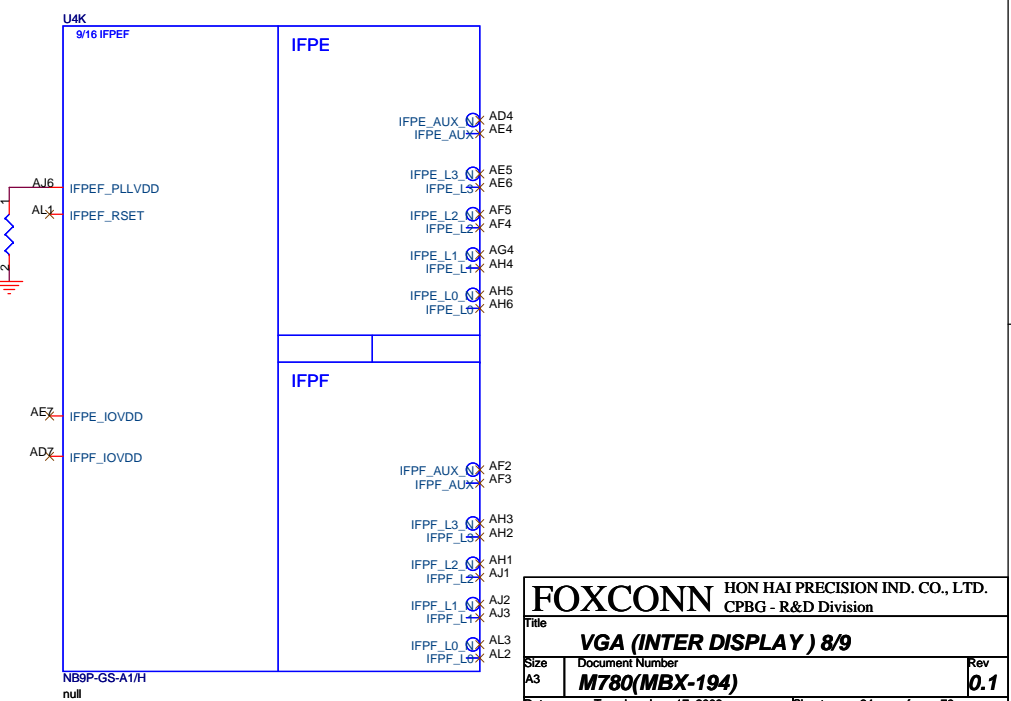
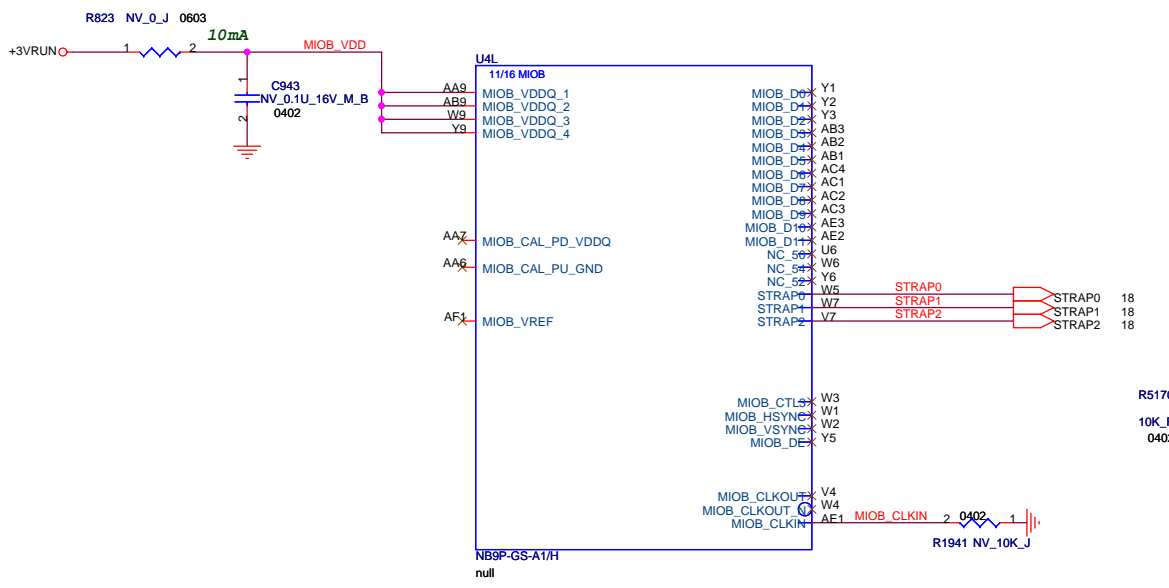
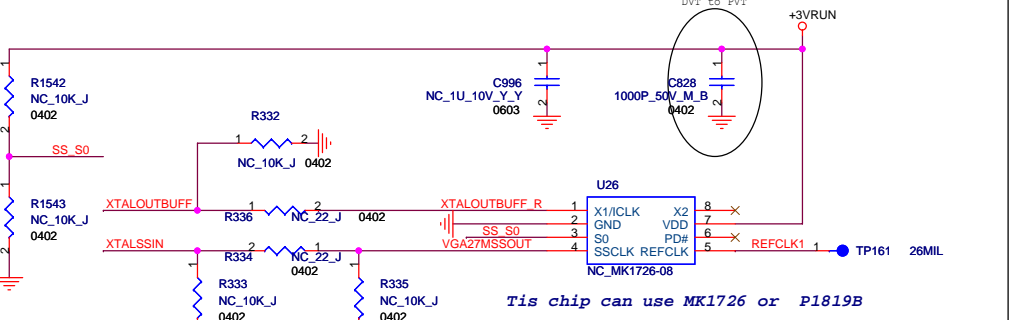
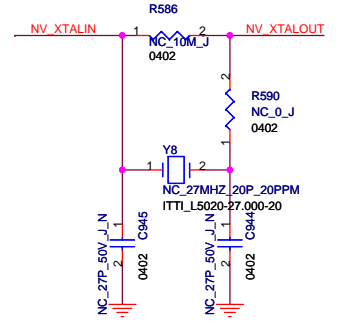
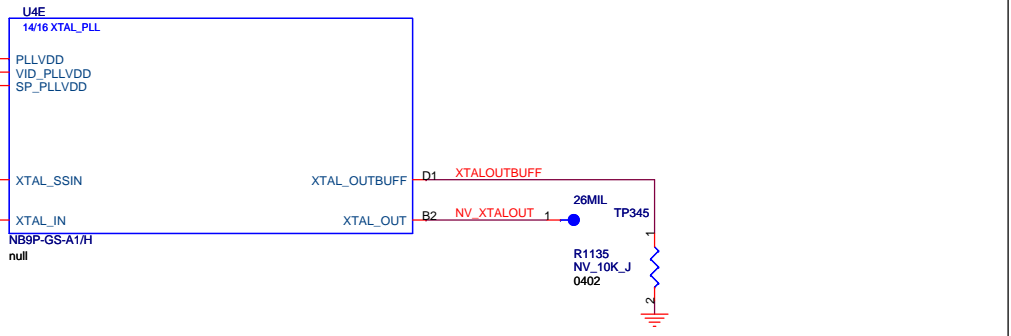
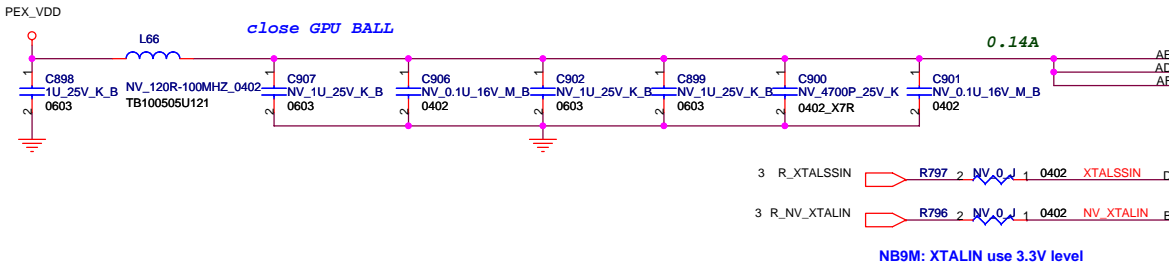
36 VGA\_BITCLK  
36 VGA\_RST#  
36 VGA\_SDATAIN1  
36 VGA\_SDATAO  
36 VGA\_SYNC



GPIO	I/O	Internal pull low	GPIO TABLE	
GPIO0	I	Yes	HDMI Hot Plug Detect 0 (HPD0)	Active High
GPIO1	I	Yes		
GPIO2	O	Yes	LCD BL Brightness(LCD0_BL_PWM)	Active High
GPIO3	O	No	Panel Power(LCD0_VDD)	Active High
GPIO4	O	Yes	LCD Backlight enable(LCD0_BL_EN)	Active High
GPIO5	O	Yes	FOR NVDD 0.9V-1.17V	Active High
GPIO6	O	No	reserve for NVDD adjust.	
GPIO8	O	No	reserve for reset EC	
GPIO9	I	No	System Power Limit Alert Input	Active Low
GPIO10	O	No	Memory Vref switch(MEM_VREF)	Active High
GPIO11	I/O	No	HDMI CEC Function Backup	



SIGNAL	I/O	Description
I2CA_SCL I2CA_SDA	I/O	For CRT VGA I2C_Compatibal Bus Signals
I2CB_SCL I2CB_SDA	I/O	NC(for DVI I2C_Compatibal Bus Signals)
I2CC_SCL I2CC_SDA	I/O	NC(All Other I2C_Compatibal Bus Signals)
I2CD_SCL I2CD_SDA	I/O	NC(Notebook DVI I2C_Compatibal Bus Signals)
I2CE_SCL I2CE_SDA	I/O	Notebook DVI I2C_Compatibal Bus Signals
I2CS_SCL I2CS_SDA	I/O	For VGA thermal I2C_Compatibal Bus Signals. Support a direct interface to the internal temperature sensor



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Title: **VGA (INTER DISPLAY) 8/9**

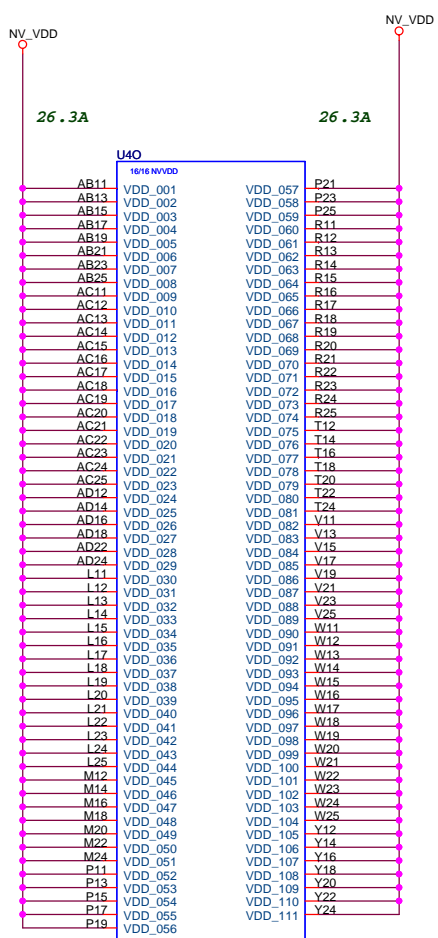
Size: Document Number  
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Date: Tuesday, June 17, 2008

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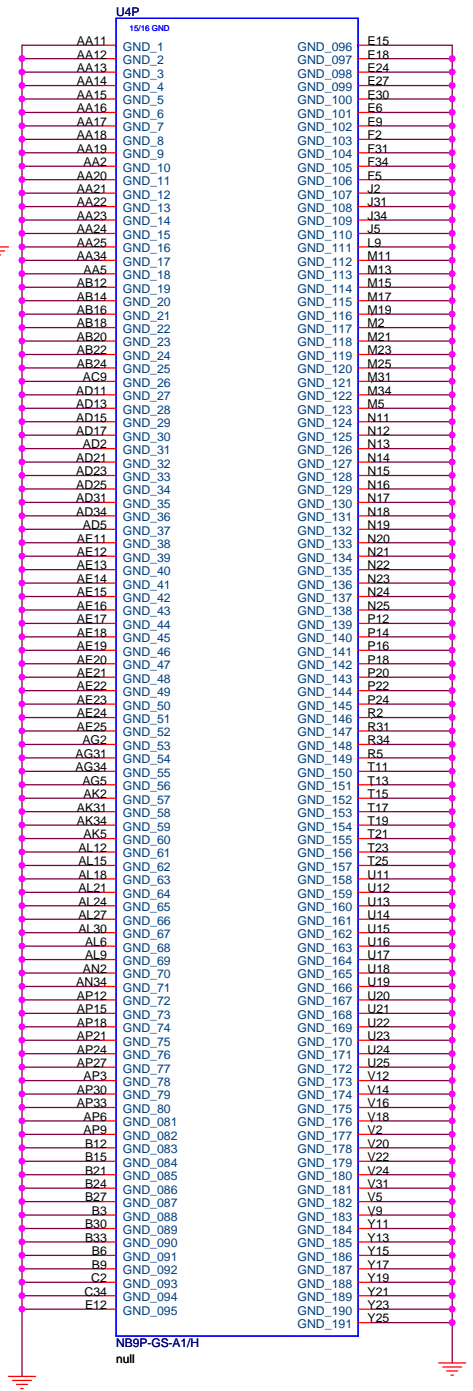
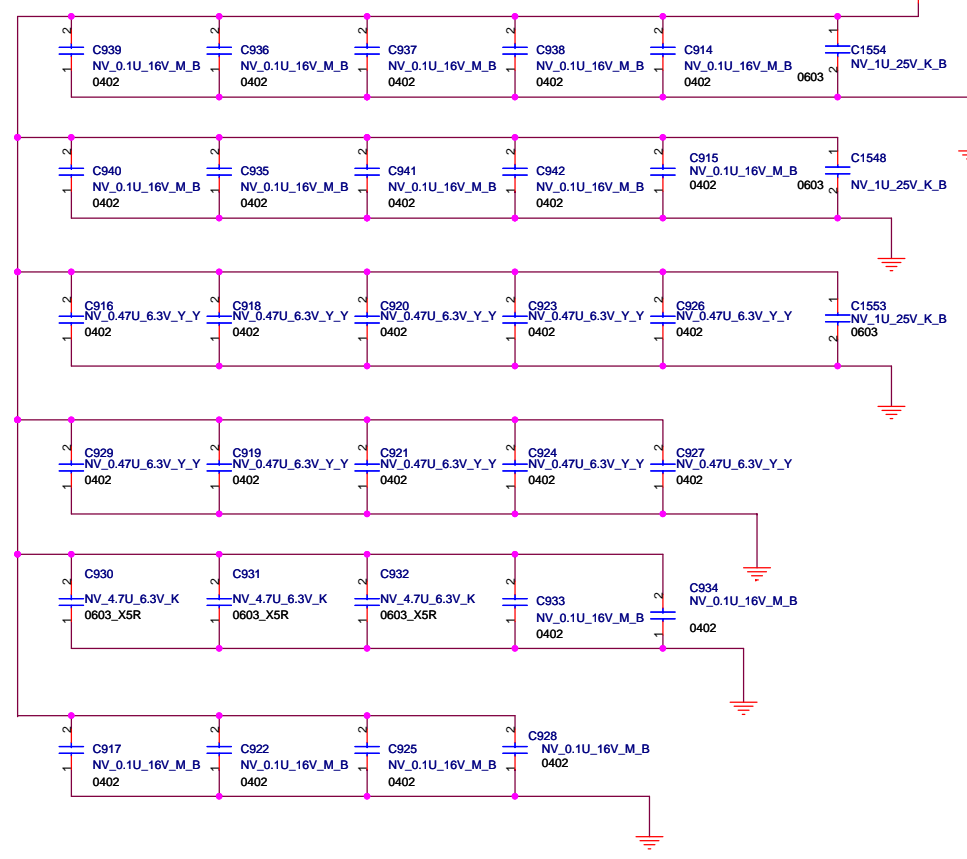
Rev **0.1**



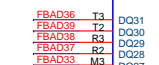
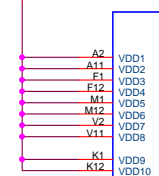
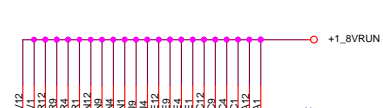
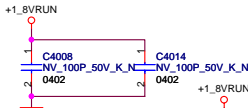
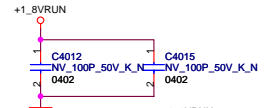


PLACE NEAR BALLS

NEAR BGA

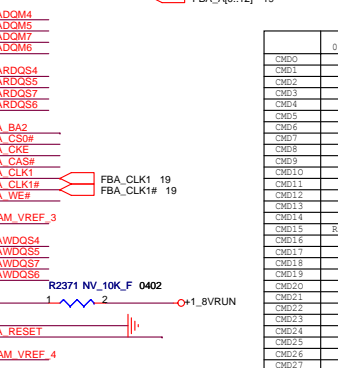
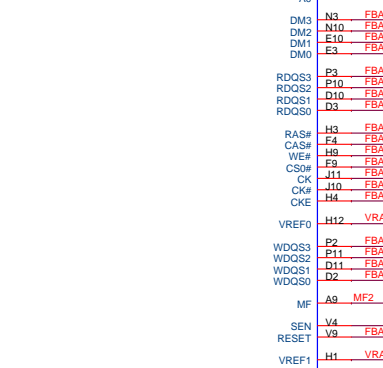
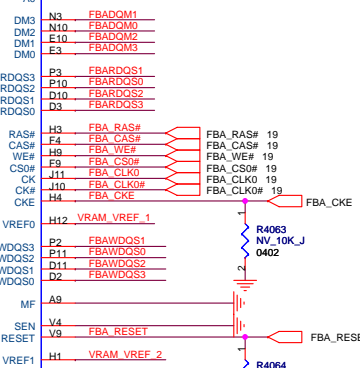


<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
<b>VGA(POWER/GROUND) 9/9</b>			
Size	Document Number		Rev
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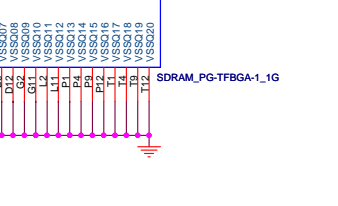
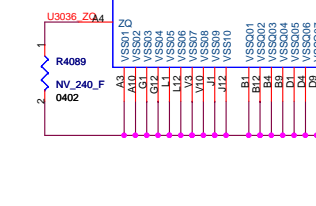
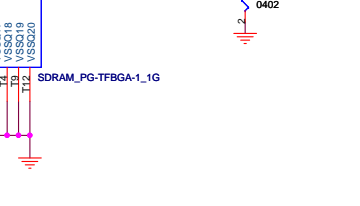
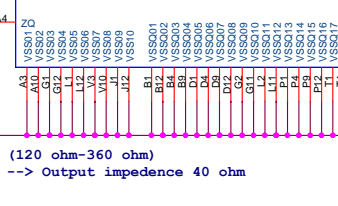
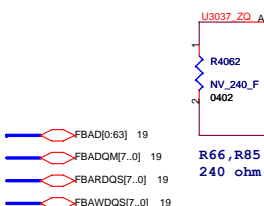


**MIRROR TABLE**

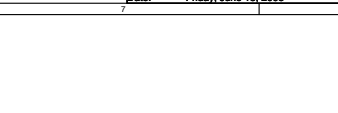
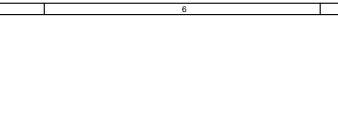
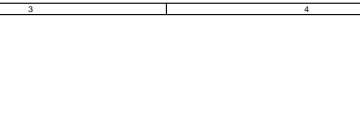
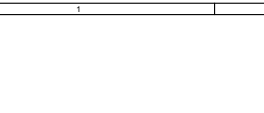
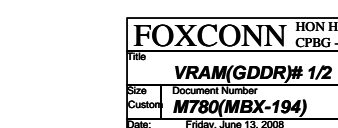
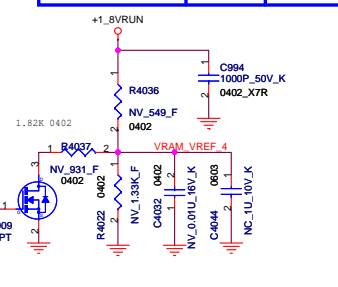
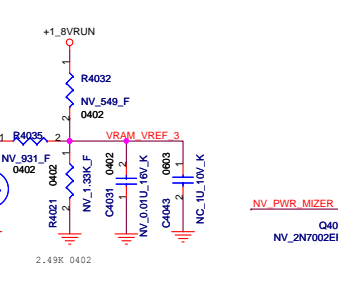
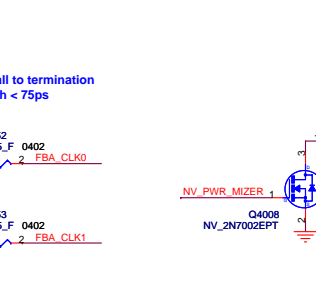
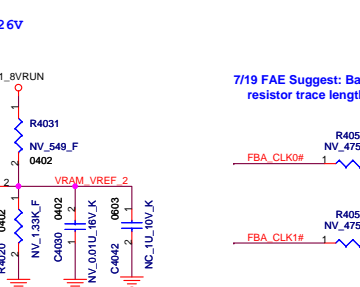
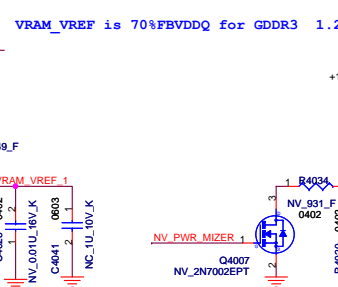
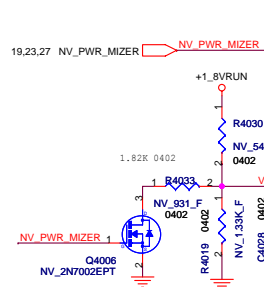
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F4	F9	CAS#	CAS#
H9	H4	WE#	WE#
F9	F4	CS#	CS#
H4	H9	CKE	CKE
K4	K9	A0	A0
H2	H1	A1	A1
K3	K10	A2	A2
M4	M9	A3	A3
K9	K4	A4	A4
H11	H2	A5	A5
K10	K3	A6	A6
L9	L4	A7	A7
K2	K2	A8	A8
M9	M4	A9	A9
K1	K11	A10	A10
L4	L9	A11	A11
G4	G9	BA0	BA0
G9	G4	BA1	BA1
H10	H3	BA2	BA2



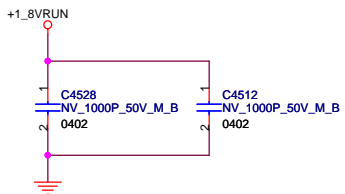
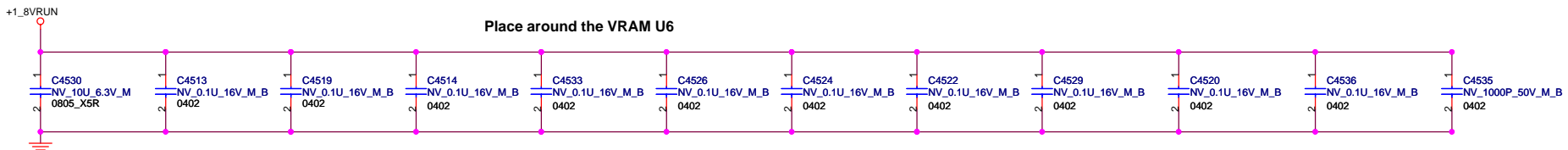
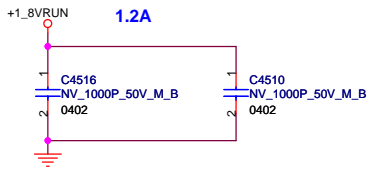
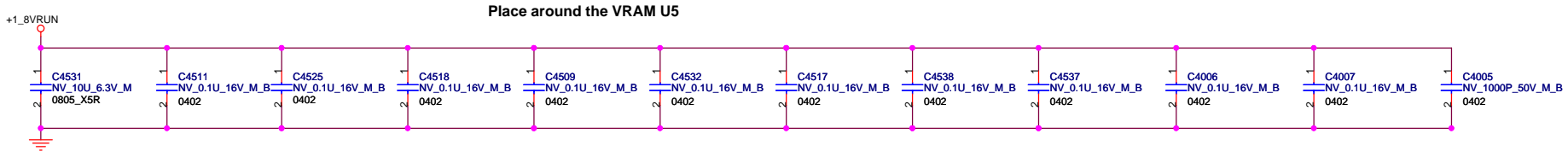
	0..30	32..63
CM00	A4	
CM01	RAS#	RAS#
CM02	A5	
CM03	BA1	BA1
CM04	BA2	BA2
CM05	A4	
CM06	A3	
CM07	CS1#	CS1#
CM08	CS0#	CS0#
CM09	A11	A11
CM10	CAS#	CAS#
CM11	WE#	WE#
CM12	BA0	BA0
CM13	A5	
CM14	A12	A12
CM15	RST/ODT	RST/ODT
CM16	A7	A7
CM17	A10	A10
CM18	CKE	CKE
CM19	A0	A0
CM20	A9	A9
CM21	A6	A6
CM22	A2	A2
CM23	A8	A8
CM24	A3	A3
CM25	A1	A1
CM26	A13	A13
CM27	BA2	BA2
CM28	REF0	REF0
CM29	REF1	REF1
CM30	REF2	REF2

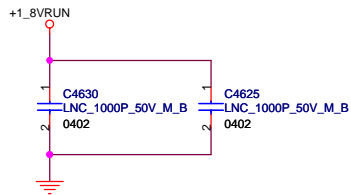
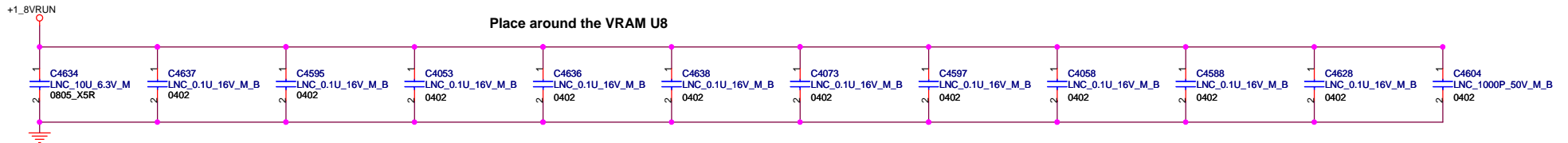
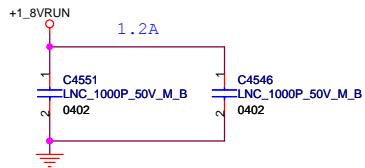
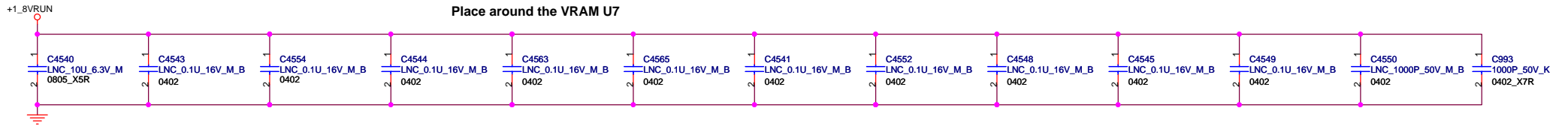


VREF	
H	50%
L	70%

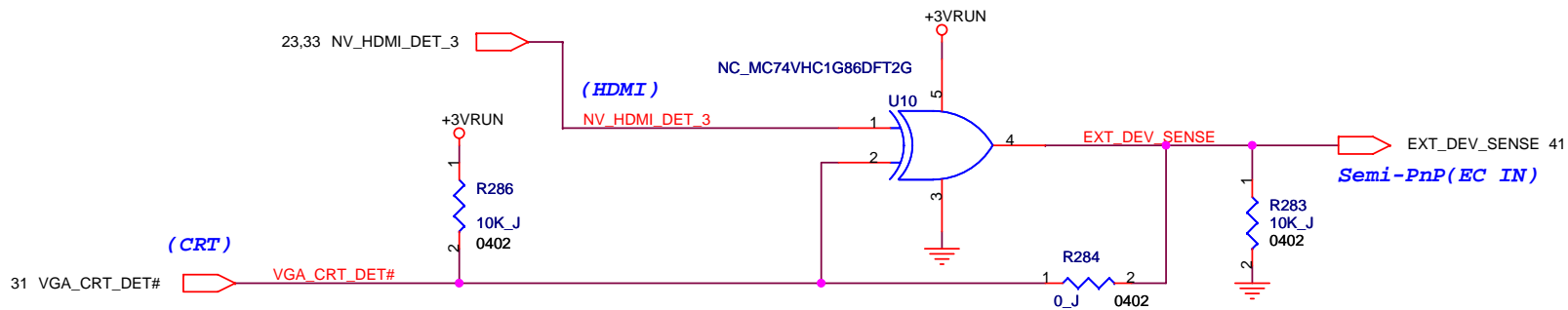




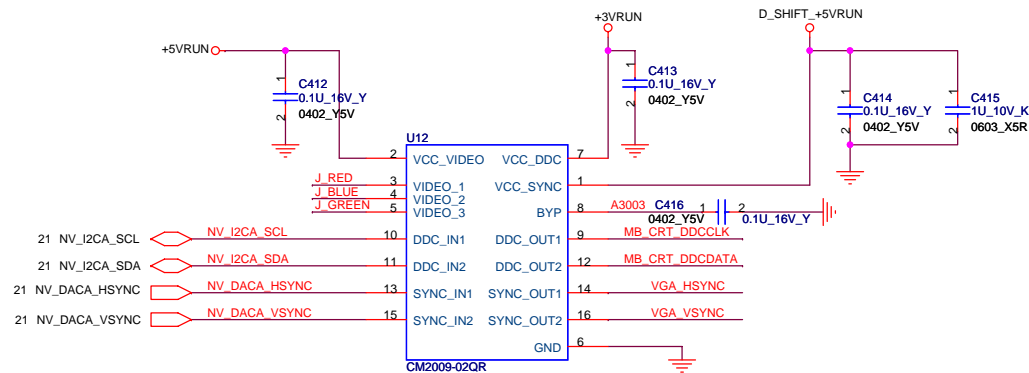
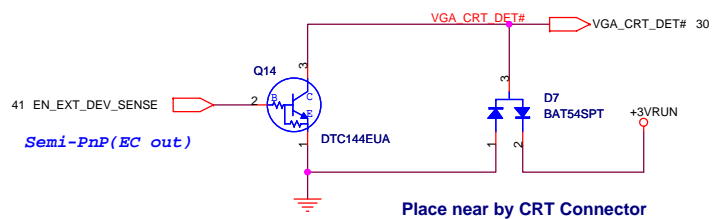




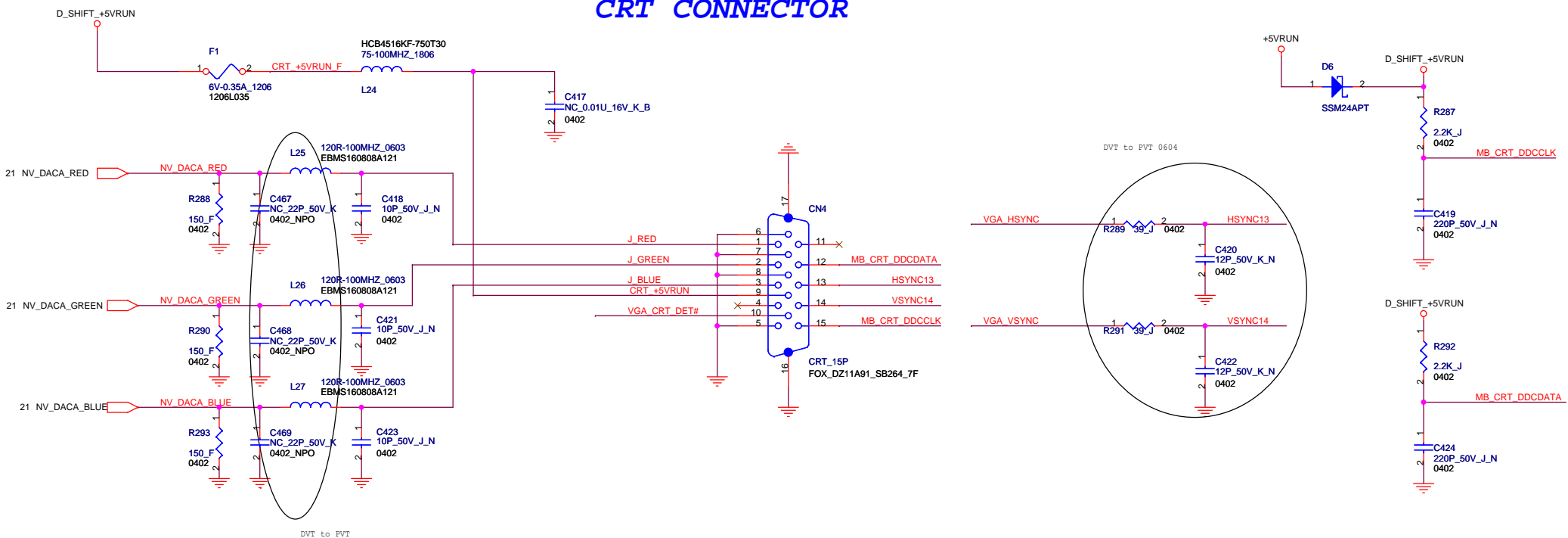
# Semi-PnP Circuit



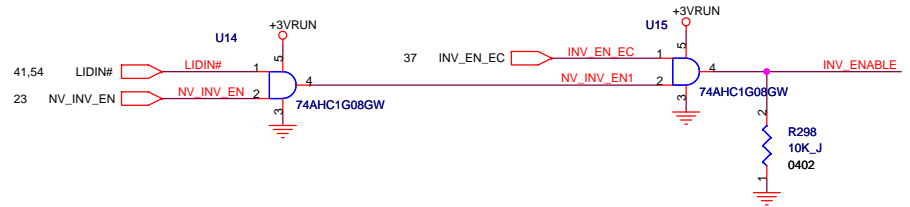
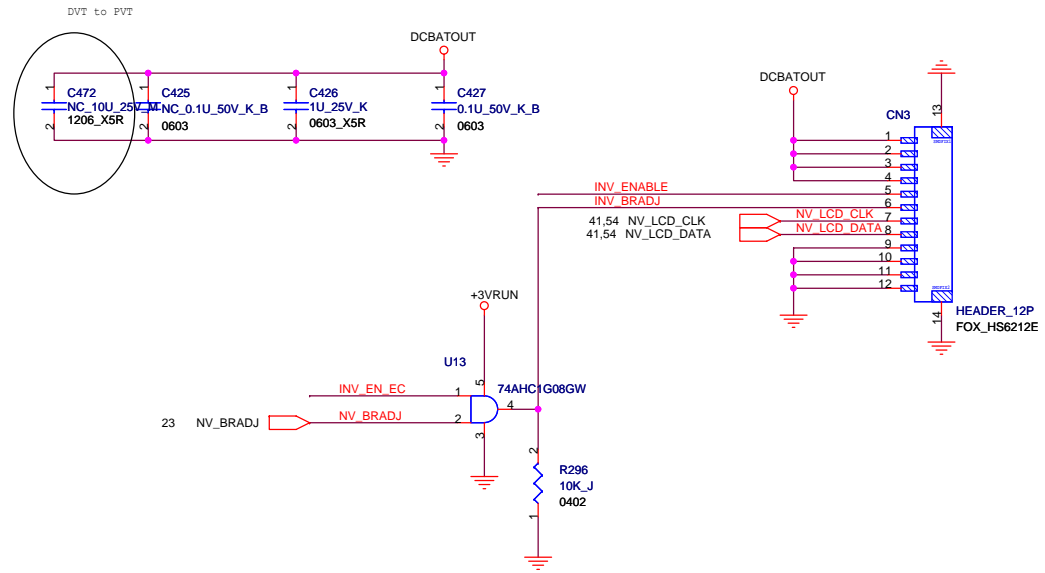
<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
<b>Semi-PnP</b>			
Size	Document Number		Rev
Custom	<b>M780(MBX-194)</b>		<b>0.1</b>
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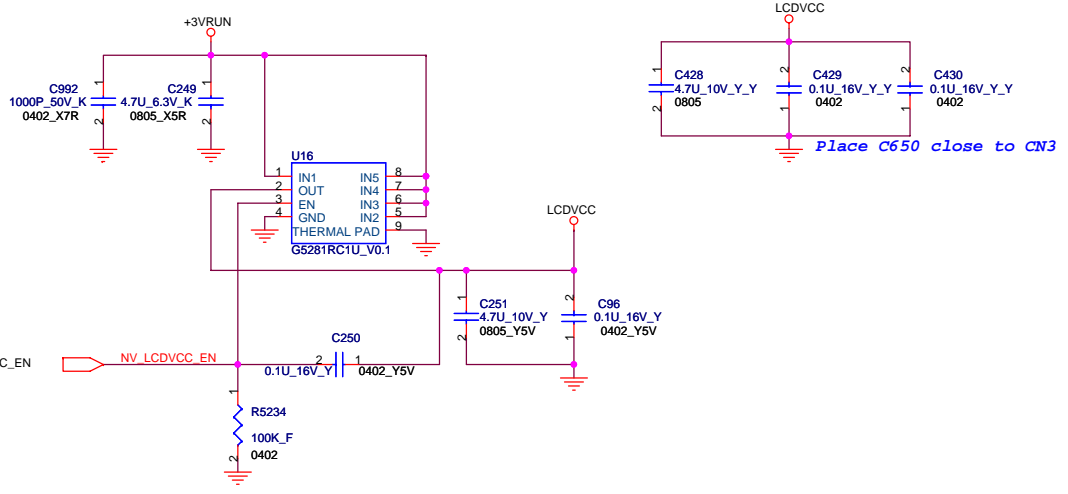
## CRT CONNECTOR



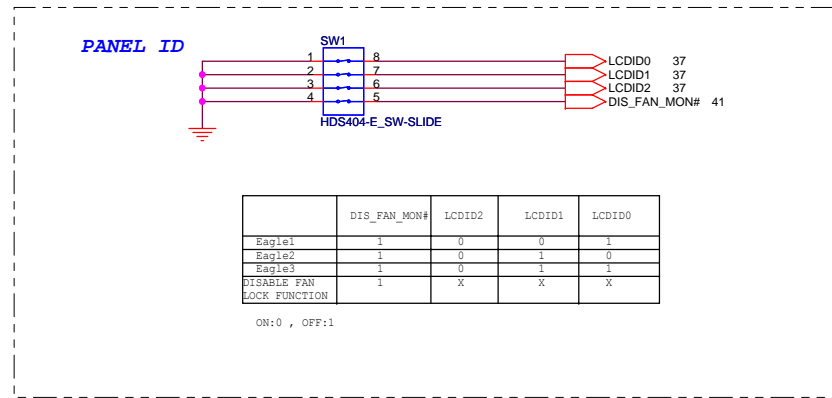
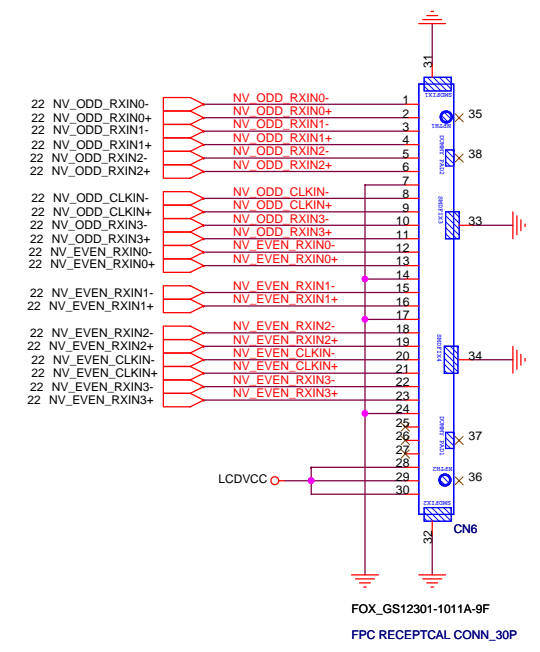
# BLU CONNECTOR



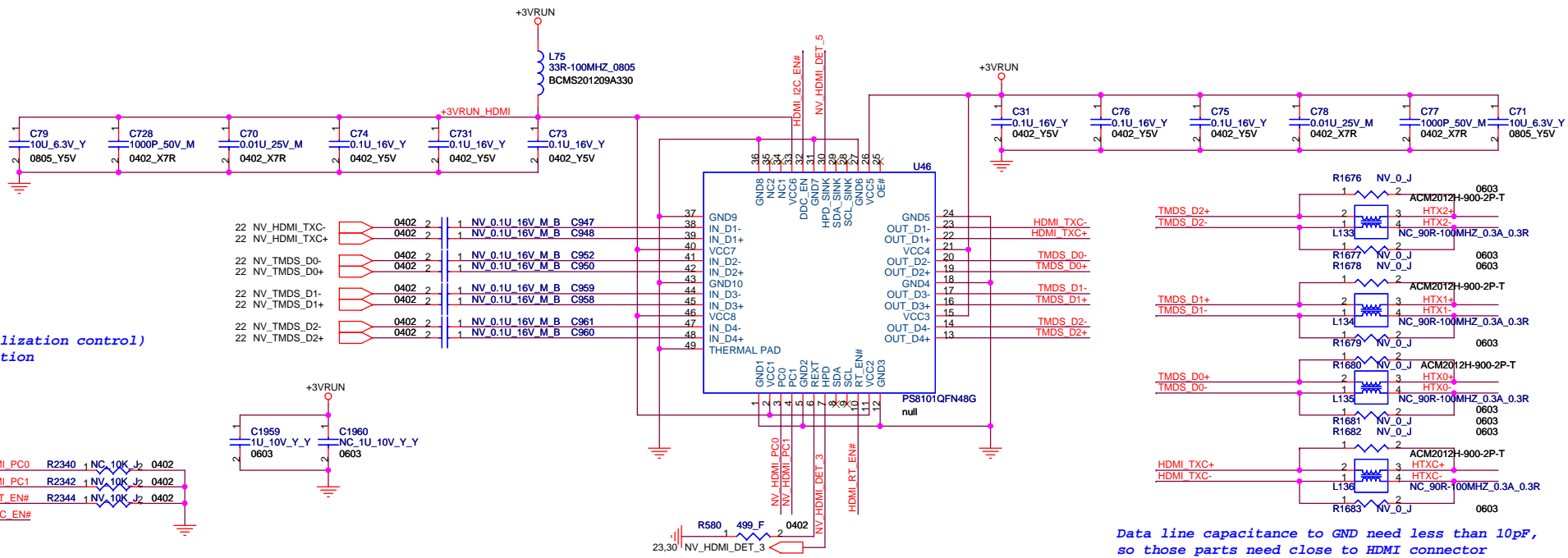
Current limit is from 1.1A to 2.1A.



# LVDS CONNECTOR

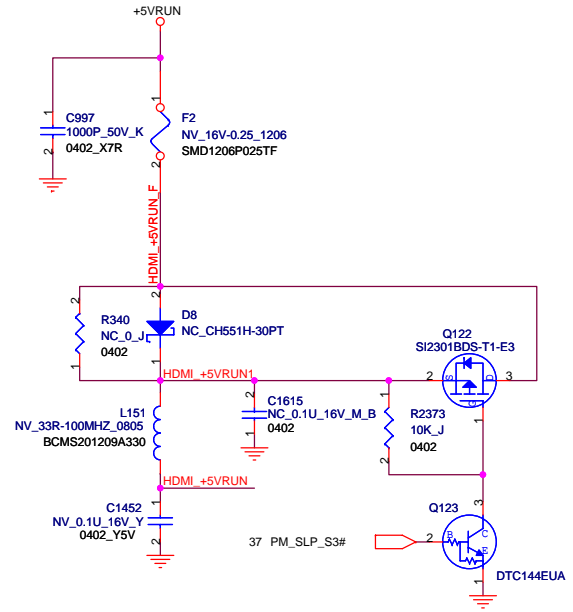
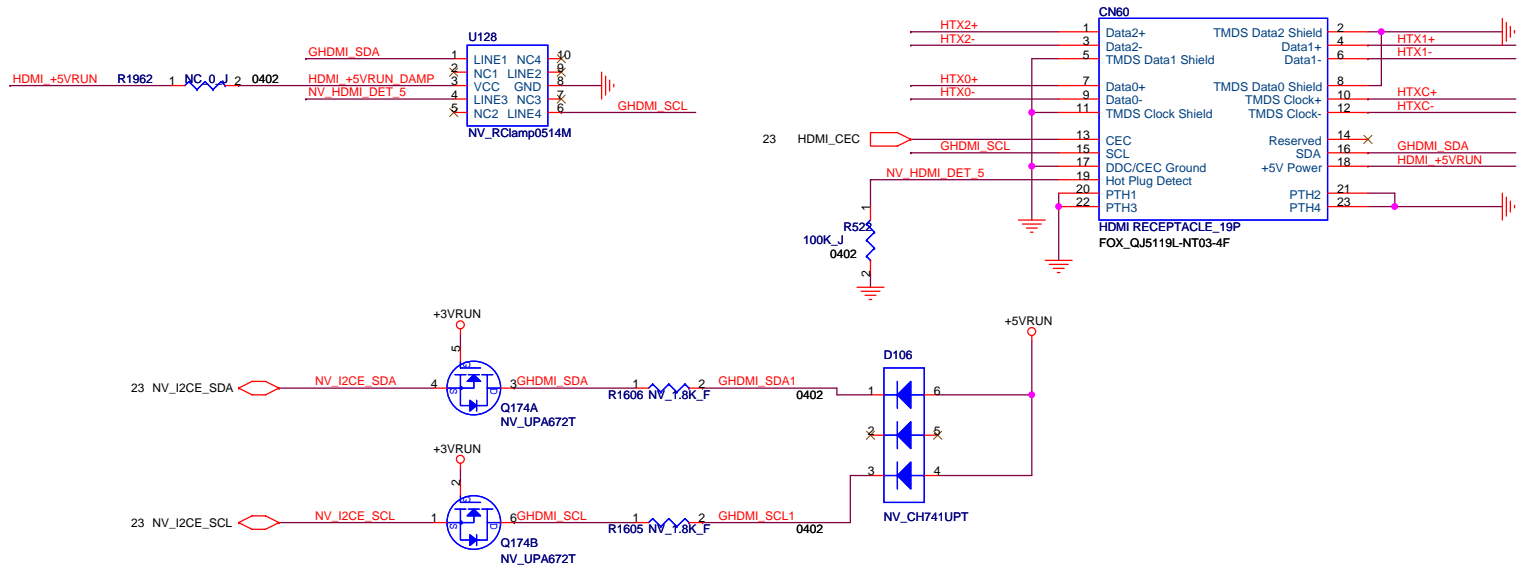


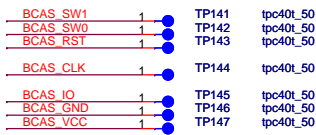
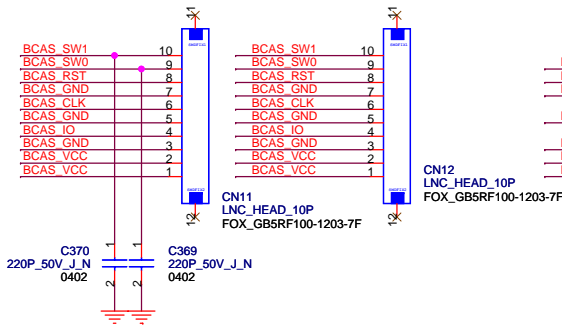
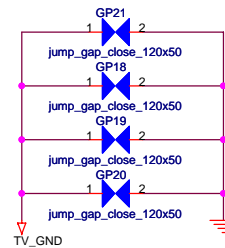
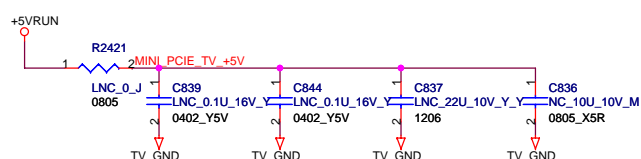
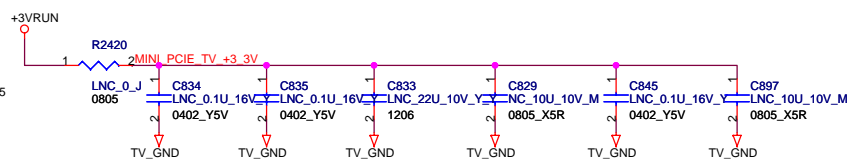
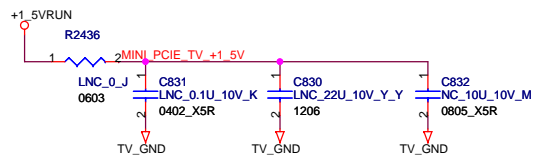
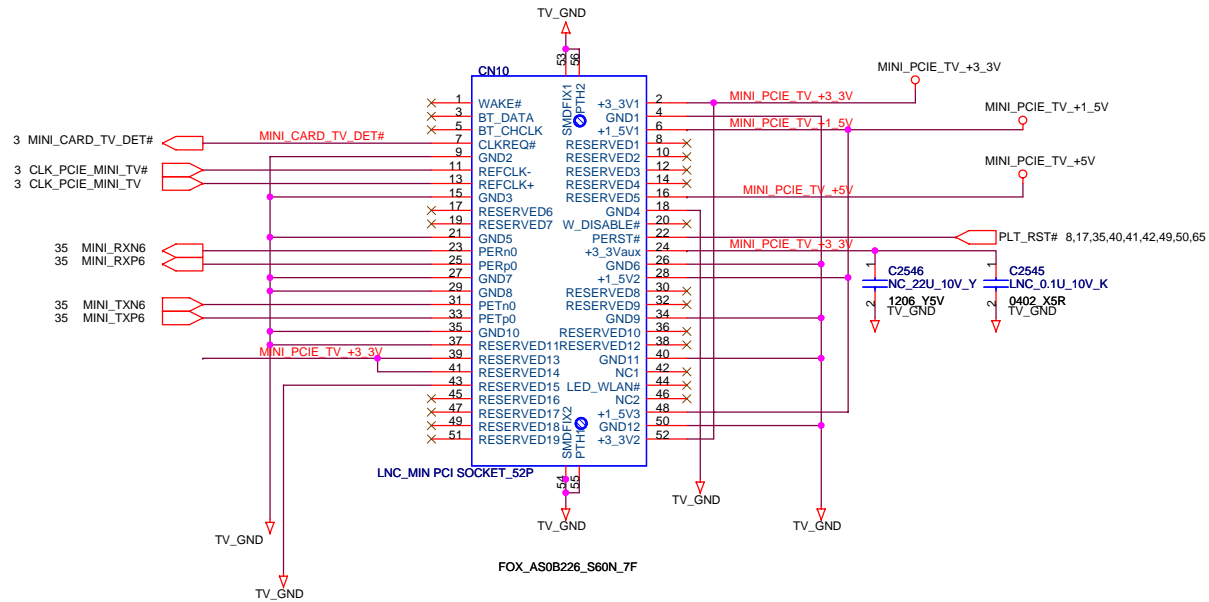


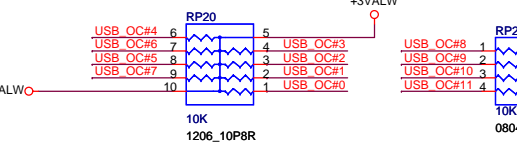
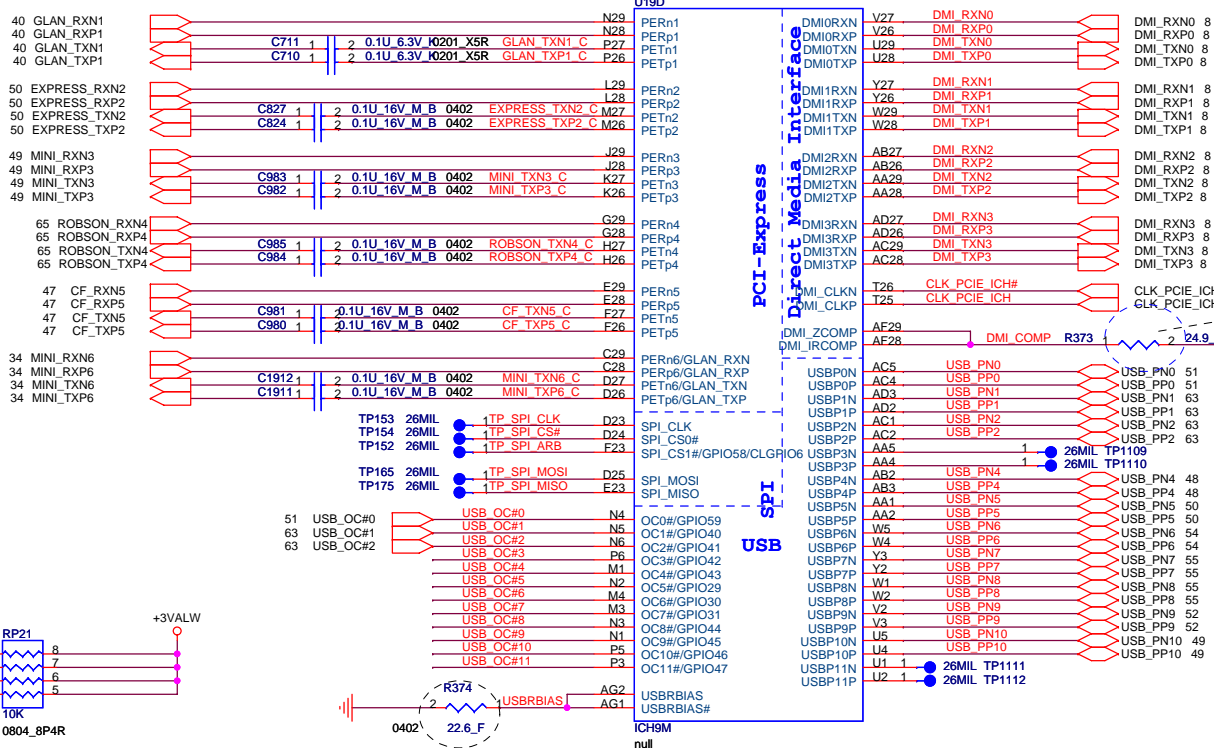
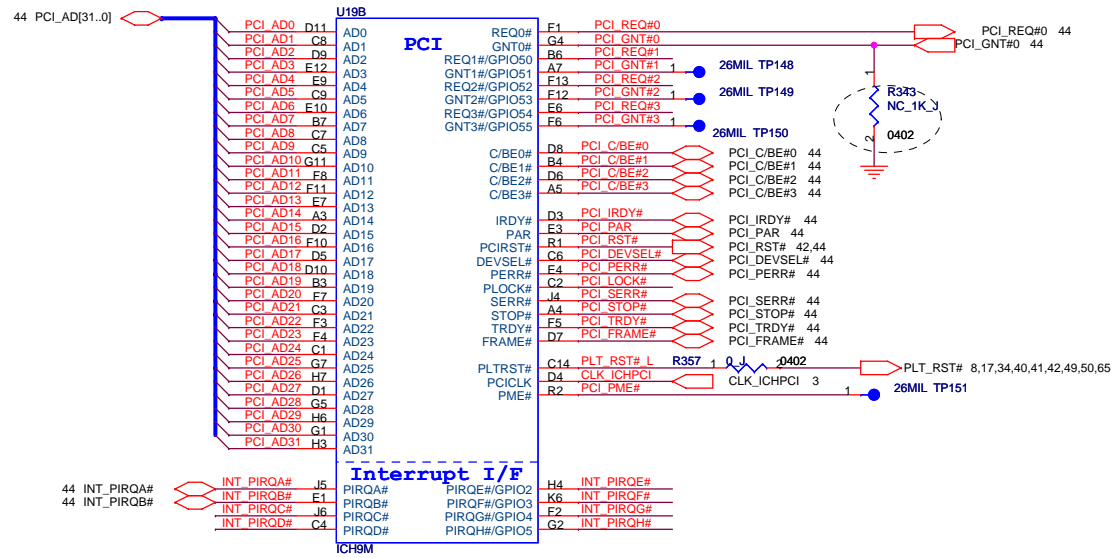
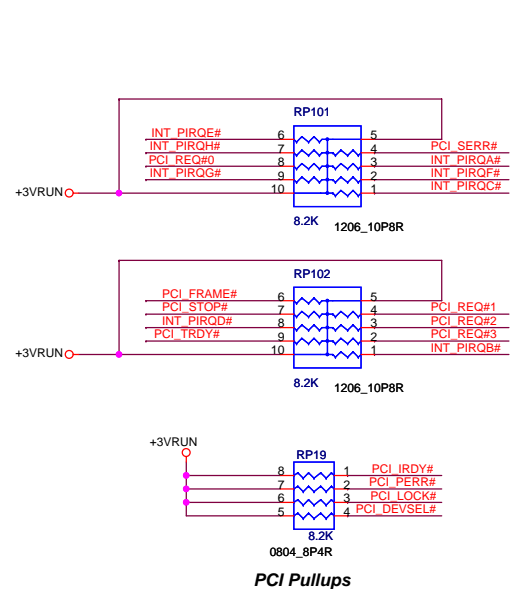


Data line capacitance to GND need less than 10pF, so those parts need close to HDMI connector

### HDMI CONNECTOR







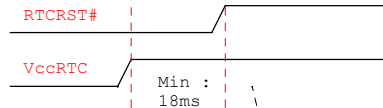
**Strap for Boot-BIOS**

IPC(Default)	GNT0#	SPI_CS1#
PCI	H1	LOW
SPI	LOW	H1

**Place within 500 mils of ICH**

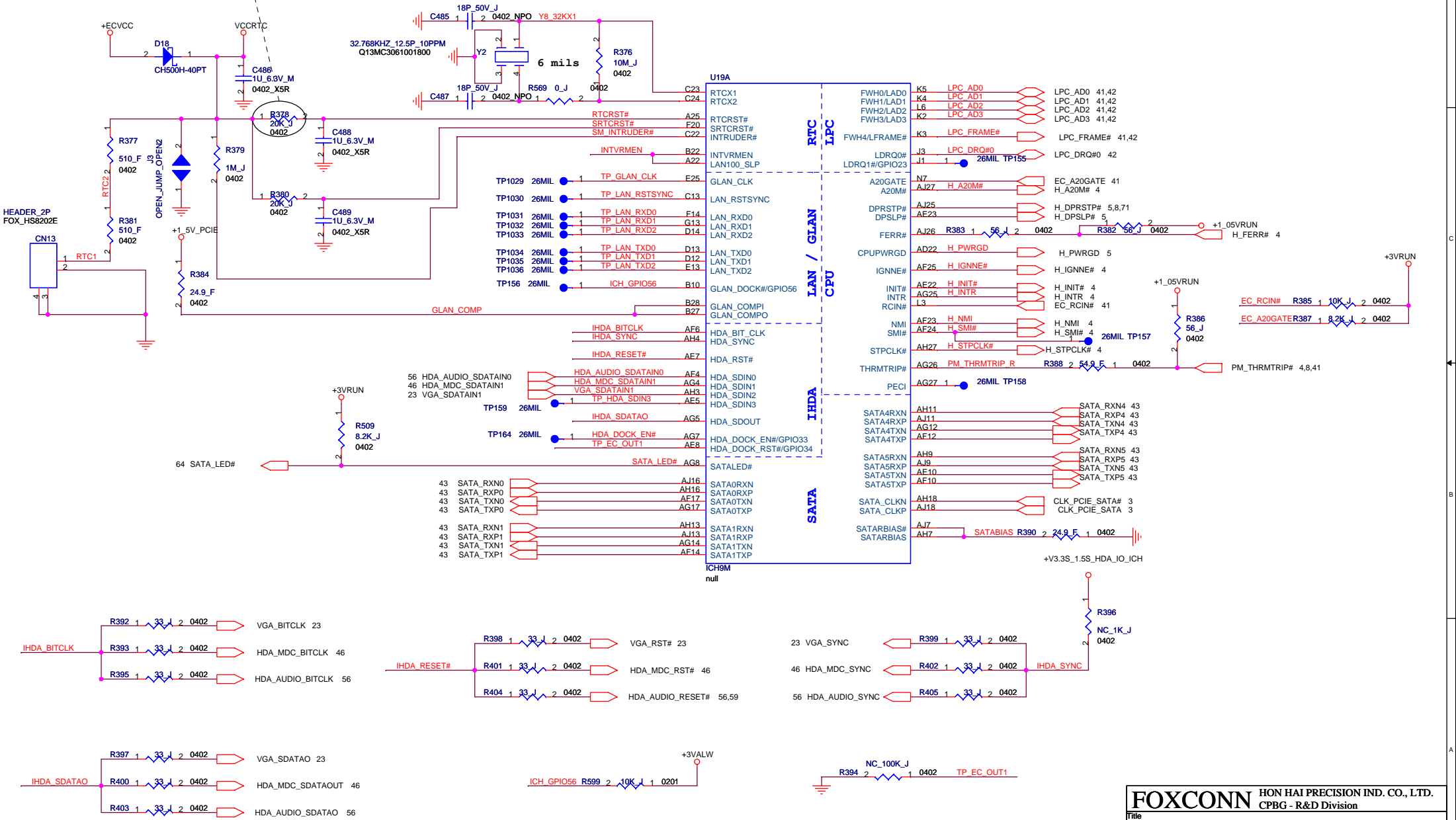
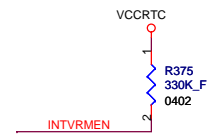
USB Port0 -- USB Port0  
 USB Port1 -- USB Port1  
 USB Port2 -- USB Port2  
 USB Port3 -- X  
 USB Port4 -- Bluetooth  
 USB Port5 -- Express Card  
 USB Port6 -- Finger print (BottomBoard)  
 USB Port7 -- Camera  
 USB Port8 -- OIDE  
 USB Port9 -- CIR  
 USB Port10 --WIMAX  
 USB Port11 -- X

Place within 500 mils of ICH and don't routing next to high speed signals



The traces inside this block should be wider.

Internal VRM enabled for VccSus1_05, VccSus1_5, VccCLL1_5, VccLAN1_05 and VccCLL1_05	
INTVRMEN	Low= Internal VR Disabled High= Internal VR Enabled(Default)



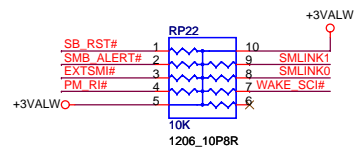
**FOXCONN** HON HAI PRECISION IND. CO., LTD.  
CPBG - R&D Division

Title: **ICH9-M (LPC,IDE,SATA) 2/5**

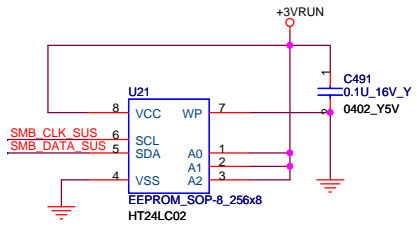
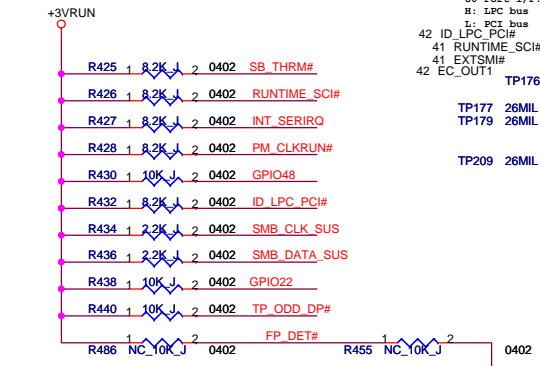
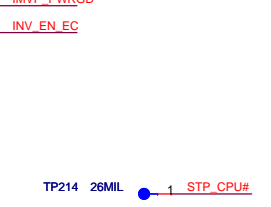
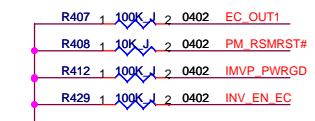
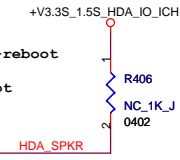
Size: Document Number  
A3: **M780(MBX-194)**

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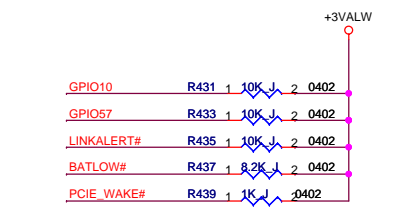
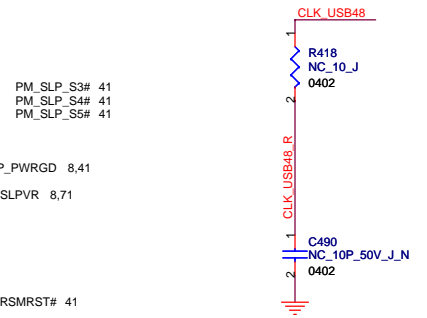
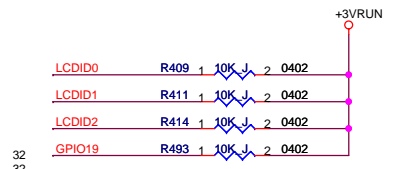
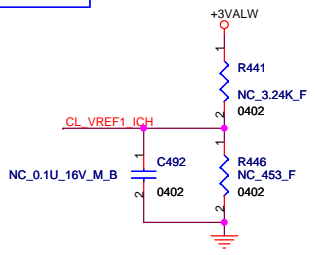
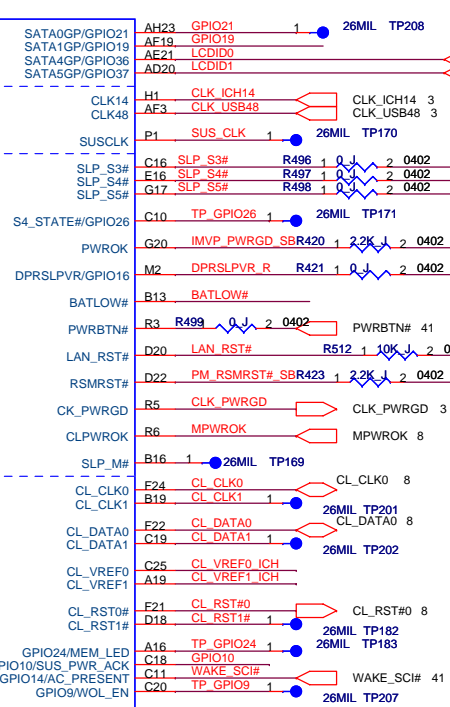
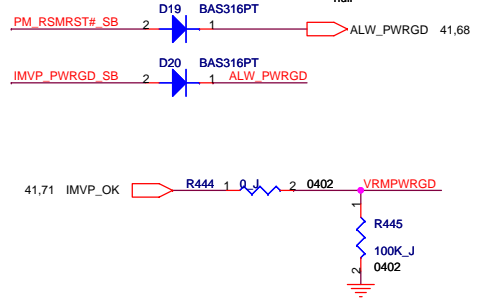
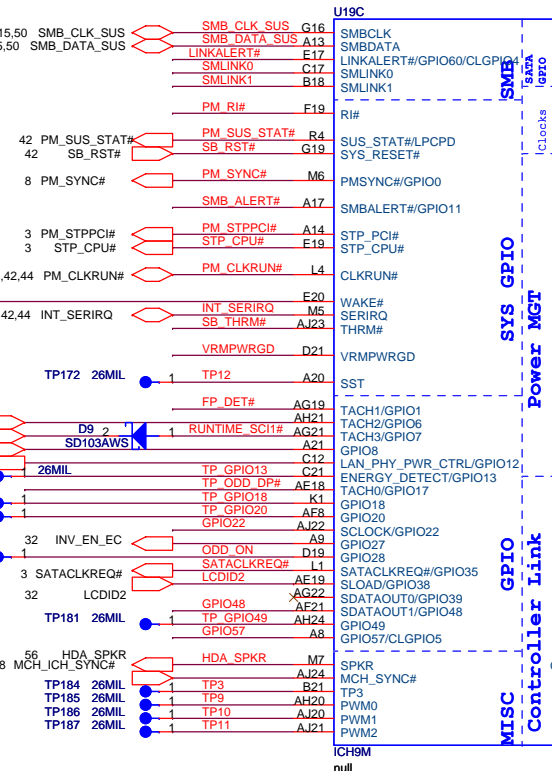
Rev: **0.1**



Stuff for No-reboot  
Low=Default  
High=No-reboot



SMBus Address: AEH



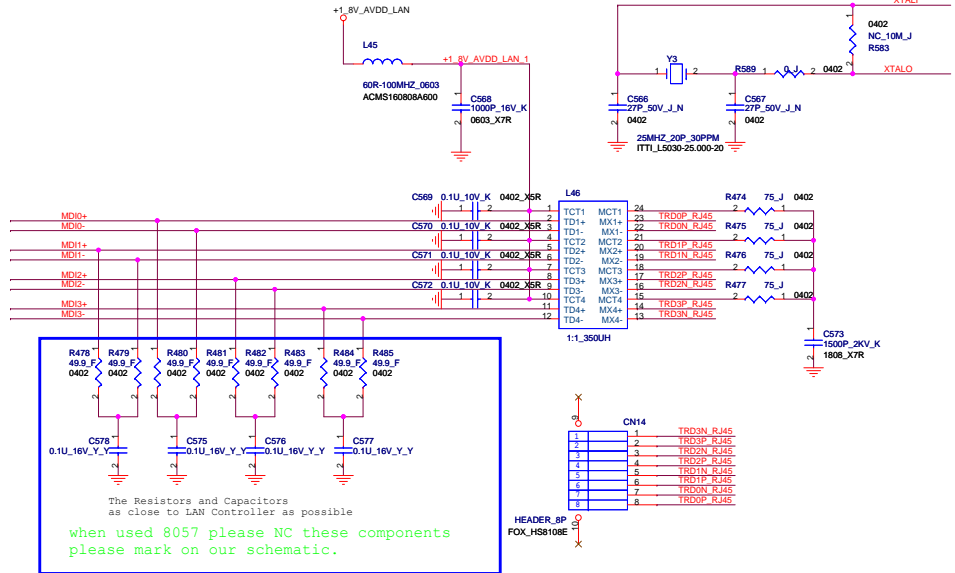
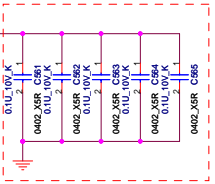
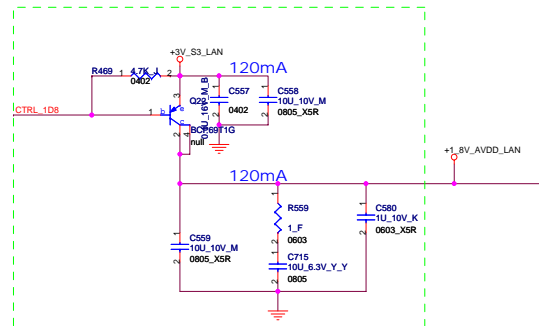
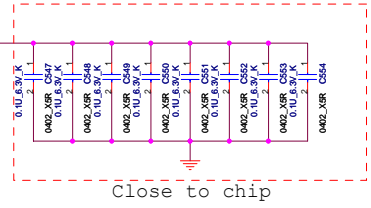
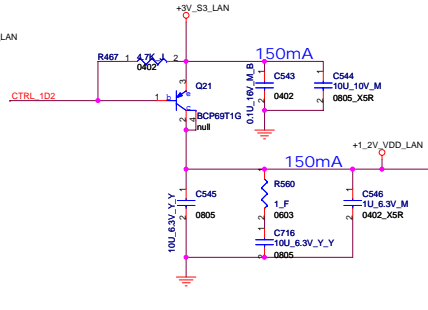
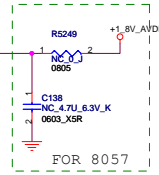
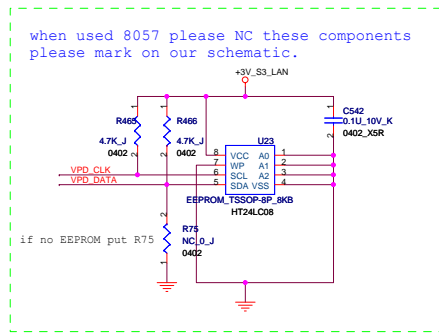
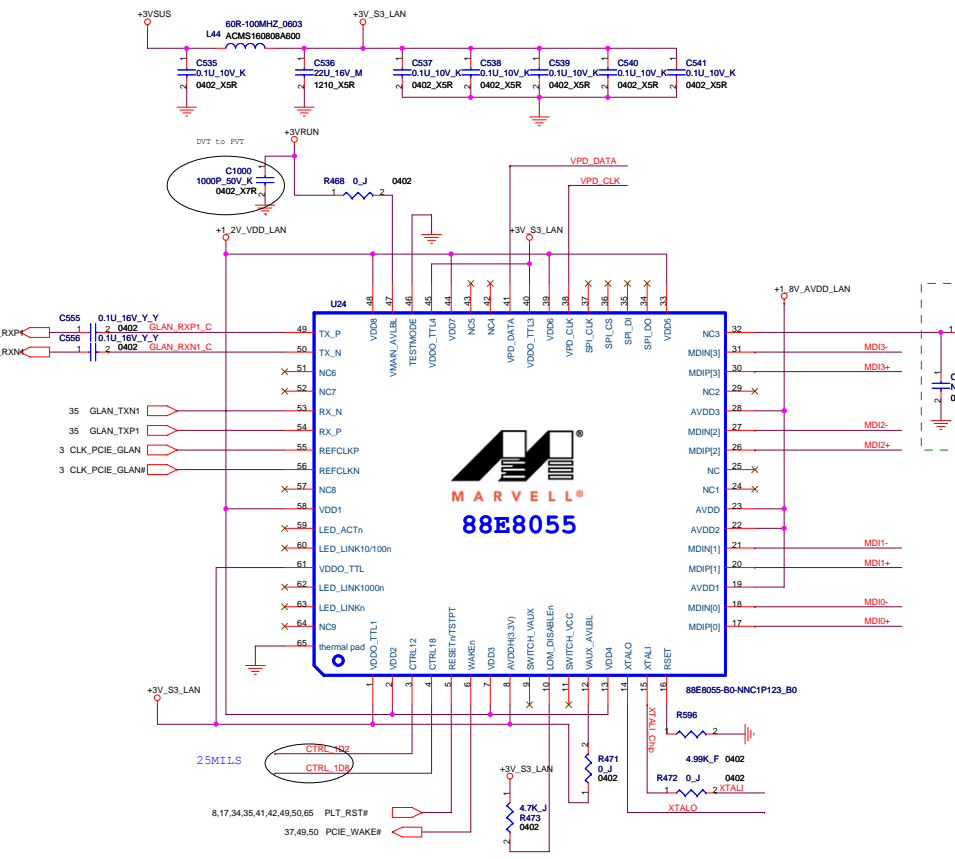
Change to 0402



U19E		H5	
AA26	VSS6	VSS126	H5
AA27	VSS7	VSS127	J23
AA3	VSS8	VSS128	J26
AA6	VSS9	VSS129	J27
AB1	VSS10	VSS16	AC22
AA23	VSS5	VSS130	K28
AB28	VSS11	VSS131	K29
AB29	VSS12	VSS132	L13
AB4	VSS13	VSS133	L15
AB5	VSS14	VSS134	L2
AC17	VSS15	VSS135	L26
AC26	VSS17	VSS136	L27
AC27	VSS18	VSS137	L5
AC3	VSS19	VSS138	L7
AD1	VSS20	VSS139	M12
AD10	VSS21	VSS140	M13
AD12	VSS22	VSS141	M14
AD13	VSS23	VSS142	M15
AD14	VSS24	VSS143	M16
AD17	VSS25	VSS144	M17
AD18	VSS26	VSS145	M23
AD21	VSS27	VSS146	M28
AD28	VSS29	VSS147	M29
AD29	VSS30	VSS148	N11
AD4	VSS31	VSS149	N12
AD5	VSS32	VSS150	N13
AD6	VSS33	VSS151	N14
AD7	VSS34	VSS152	N15
AD9	VSS35	VSS153	N16
AE12	VSS36	VSS154	N17
AE13	VSS37	VSS155	N18
AE14	VSS38	VSS156	N26
AE16	VSS39	VSS157	N27
AE17	VSS40	VSS158	P12
AE2	VSS41	VSS159	P13
AE20	VSS42	VSS160	P14
AE24	VSS43	VSS161	P15
AE3	VSS44	VSS162	P16
AE4	VSS45	VSS163	P17
AE6	VSS46	VSS164	P2
AE9	VSS47	VSS165	P23
AF13	VSS48	VSS166	P28
AF16	VSS49	VSS167	P29
AF18	VSS50	VSS168	P4
AF22	VSS52	VSS169	P7
AH26	VSS53	VSS170	R11
AE26	VSS54	VSS171	R12
AE27	VSS55	VSS172	R13
AF5	VSS56	VSS173	R14
AF7	VSS57	VSS174	R15
AF9	VSS58	VSS175	R16
AG13	VSS59	VSS176	R17
AG16	VSS60	VSS177	R18
AG18	VSS61	VSS178	R28
AG20	VSS62	VSS179	T12
AG23	VSS63	VSS180	T13
AG3	VSS64	VSS181	T14
AG6	VSS65	VSS182	T15
AG9	VSS66	VSS183	T16
AH12	VSS67	VSS184	T17
AH14	VSS68	VSS185	T23
AH17	VSS70	VSS186	B26
AH19	VSS71	VSS187	U12
AH2	VSS72	VSS188	U13
AH22	VSS73	VSS189	U14
AH25	VSS74	VSS190	U15
AH28	VSS75	VSS191	U16
AH5	VSS76	VSS192	U17
AH8	VSS78	VSS193	AD23
AJ12	VSS80	VSS194	U26
AJ14	VSS82	VSS195	U27
AJ17	VSS83	VSS196	U3
AJ8	VSS84	VSS197	V1
B11	VSS88	VSS198	V13
B14	VSS90	VSS199	V15
B17	VSS91	VSS200	V23
B2	VSS92	VSS201	V28
B20	VSS93	VSS202	V29
B23	VSS94	VSS203	V4
B5	VSS95	VSS204	V5
B8	VSS98	VSS205	W26
C26	VSS100	VSS206	W27
C27	VSS101	VSS207	W3
E11	VSS102	VSS208	Y1
E14	VSS103	VSS209	Y28
E18	VSS104	VSS210	Y29
E2	VSS105	VSS211	Y4
E21	VSS106	VSS212	Y5
E24	VSS107	VSS213	AG28
E5	VSS108	VSS214	AH6
F8	VSS109	VSS215	AF2
F16	VSS110	VSS216	B25
F28	VSS111	VSS217	
F29	VSS112	VSS218	
G12	VSS113	VSS219	A1
G14	VSS114	VSS220	A2
G18	VSS115	VSS221	A28
G21	VSS116	VSS222	A29
G24	VSS117	VSS223	AH
G26	VSS118	VSS224	AH29
G27	VSS119	VSS225	AJ1
H23	VSS120	VSS226	AJ2
H28	VSS121	VSS227	AJ28
H2	VSS122	VSS228	AJ29
H23	VSS123	VSS229	B1
H28	VSS124	VSS230	B29
H29	VSS125	VSS231	

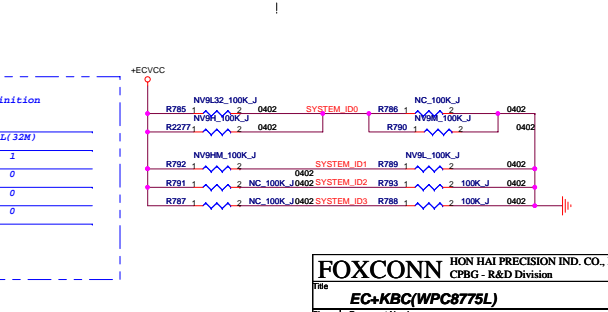
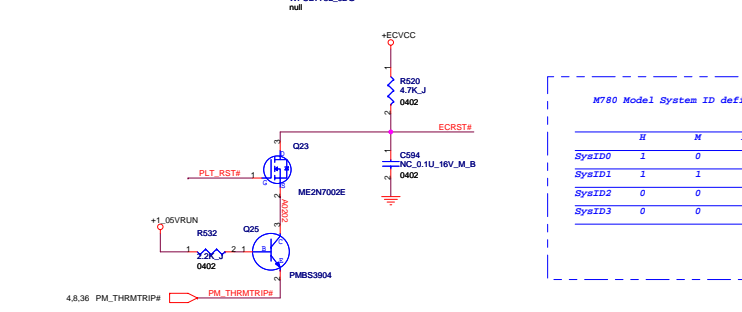
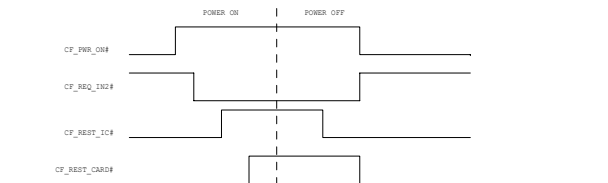
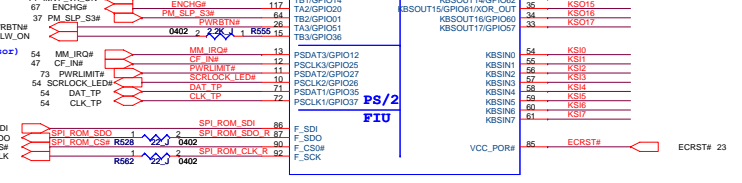
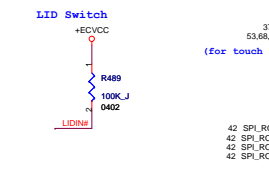
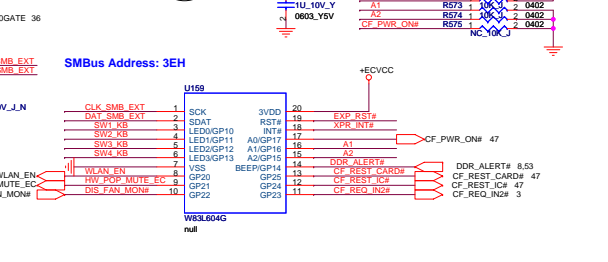
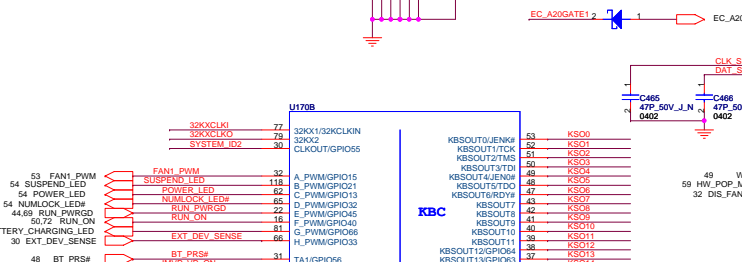
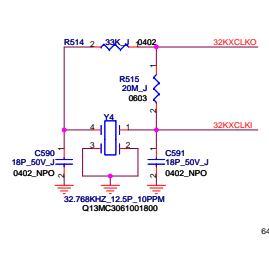
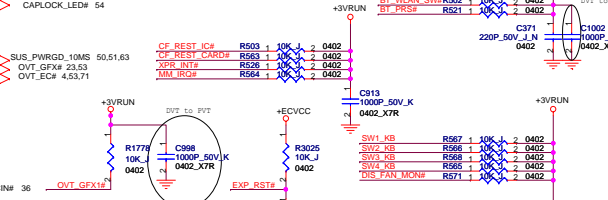
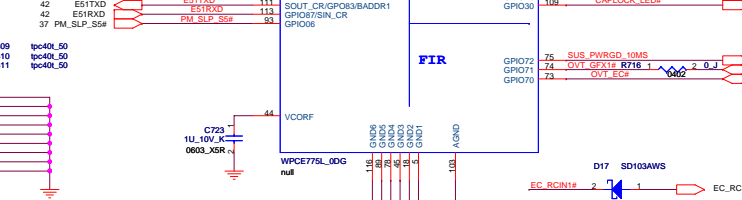
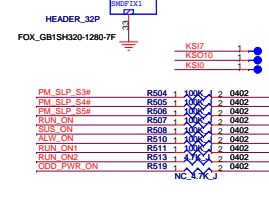
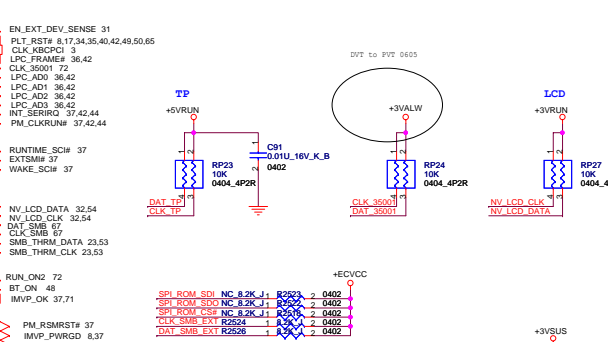
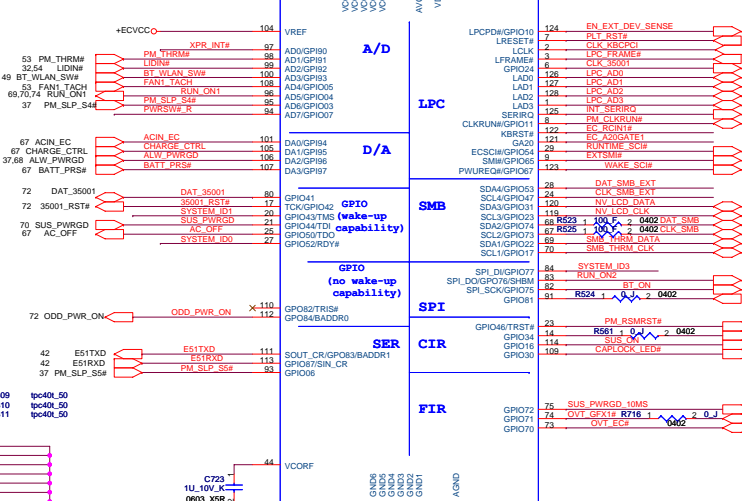
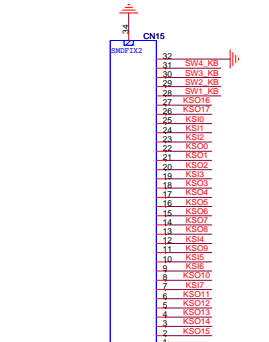
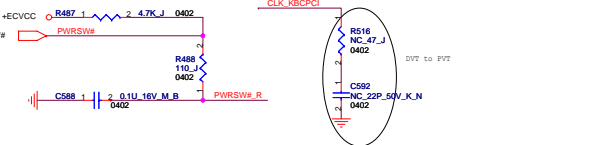
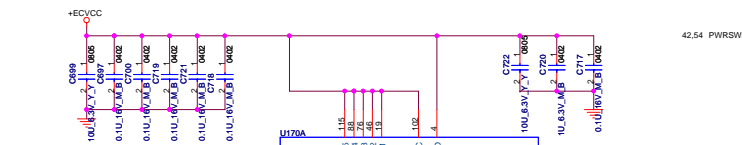
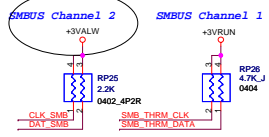
ICH9M  
null

<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
<b>ICH9-M( GND) 5/5</b>			
Size	Document Number		Rev
A3	<b>M780(MBX-194)</b>		<b>0.1</b>
Date:	Friday, June 13, 2008	Sheet	39 of 79

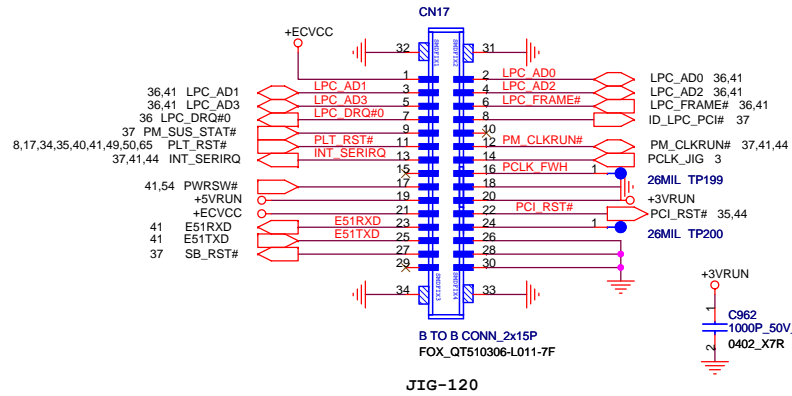
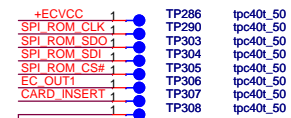
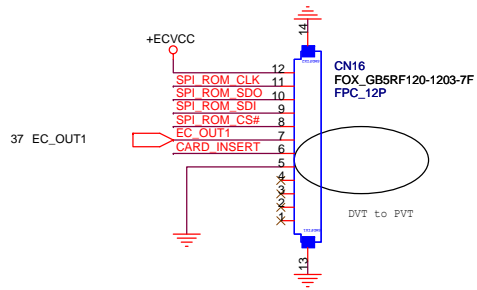
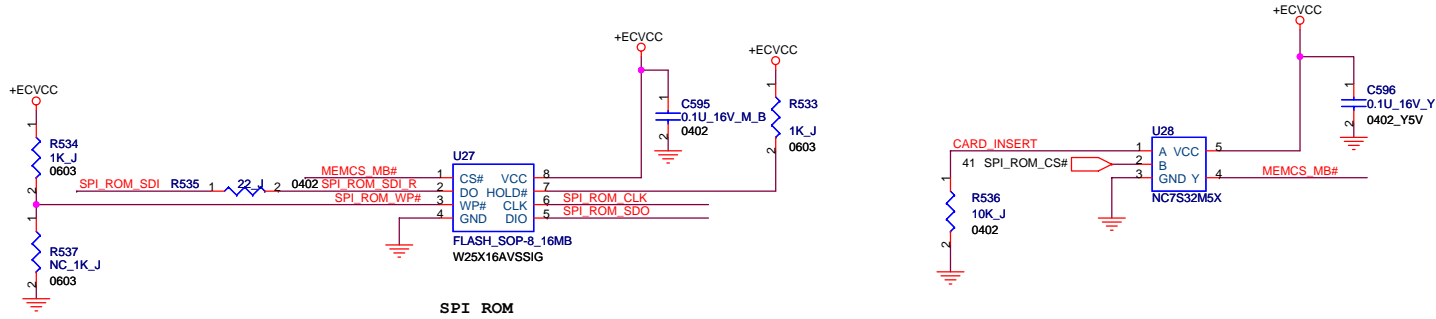


- BFT Test Pad**
- TRD3N\_RJ45 1 TP191 ipc40L50
  - TRD3P\_RJ45 1 TP206 ipc40L50
  - TRD2N\_RJ45 1 TP193 ipc40L50
  - TRD2P\_RJ45 1 TP194 ipc40L50
  - TRD1N\_RJ45 1 TP195 ipc40L50
  - TRD1P\_RJ45 1 TP196 ipc40L50
  - TRD0N\_RJ45 1 TP197 ipc40L50
  - TRD0P\_RJ45 1 TP198 ipc40L50

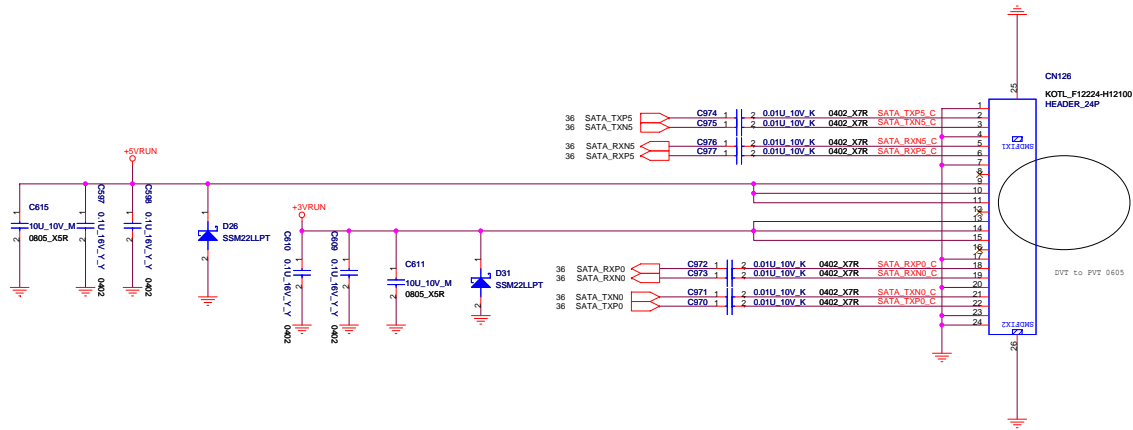




41 SPI\_ROM\_SDI <math>\rightarrow</math> SPI\_ROM\_SDI  
 41 SPI\_ROM\_SDO <math>\rightarrow</math> SPI\_ROM\_SDO  
 41 SPI\_ROM\_CLK <math>\rightarrow</math> SPI\_ROM\_CLK

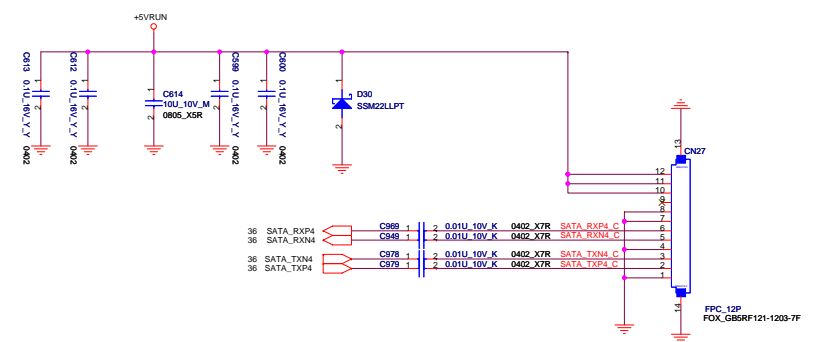


### SATA HDD CONN (FPC)

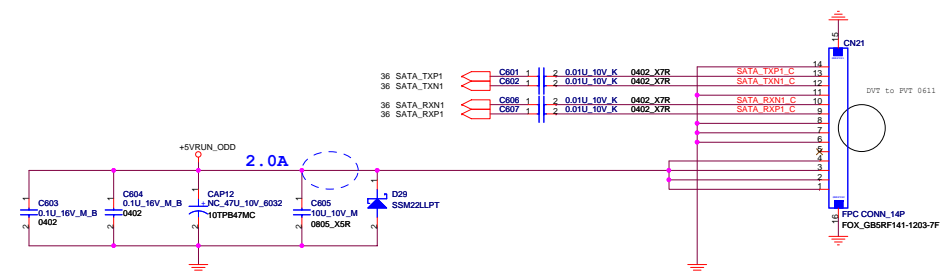


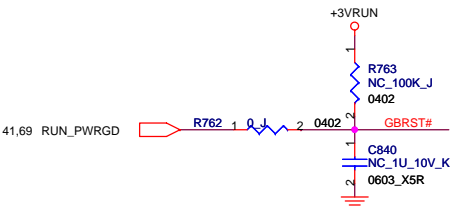
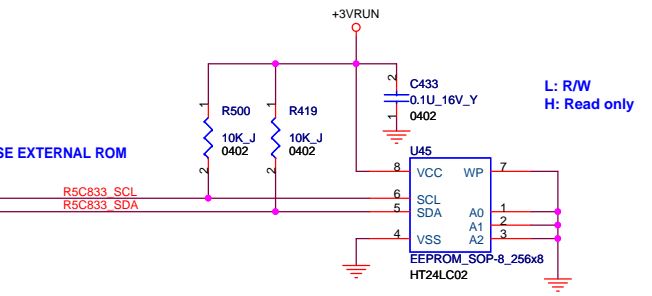
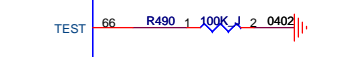
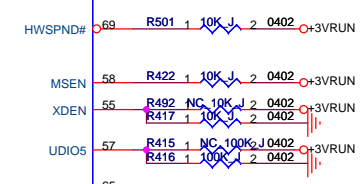
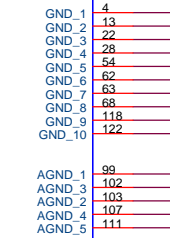
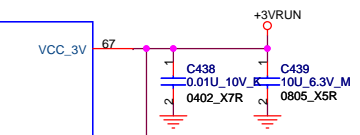
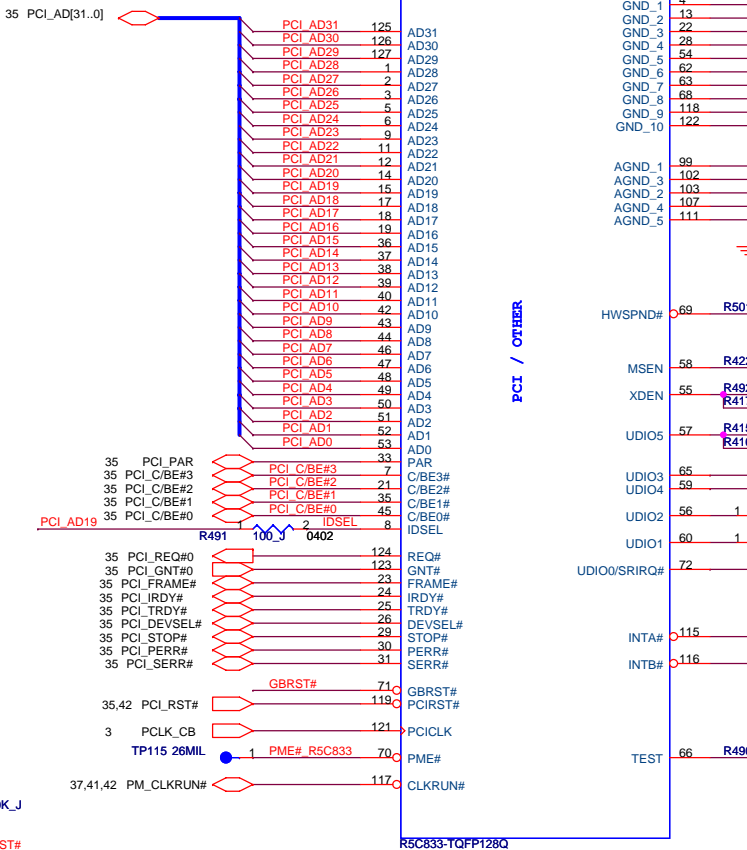
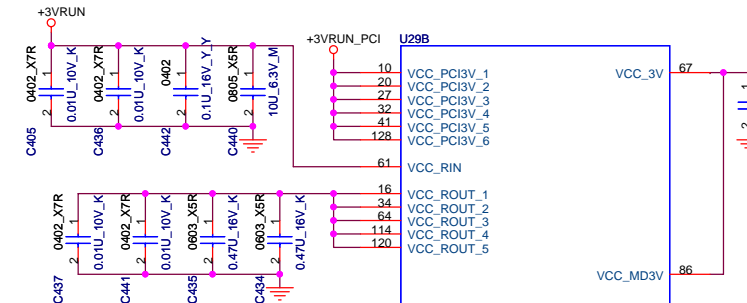
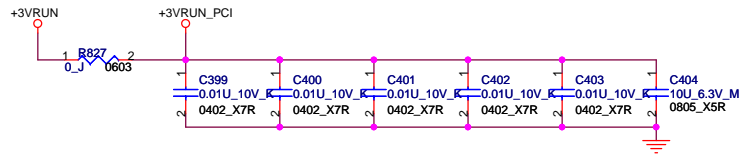
SATA0 : HDD or SSD (just connect to 24 Pin connector)  
 SATA1 : ODD (fixed)  
 SATA4 : HDD.(fixed for Single HDD connector)  
 SATA5 : SSD.(just connect to 24 Pin connector)

### SATA HDD CONN1 (FPC)

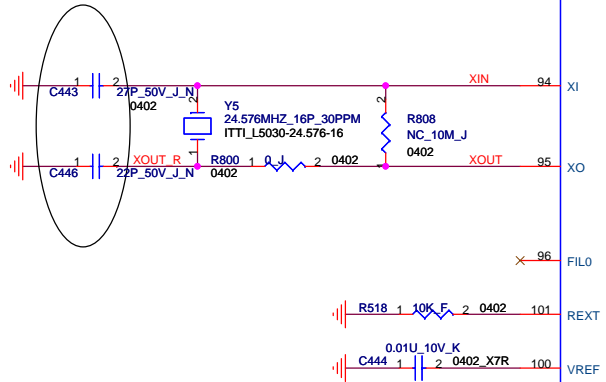


### SATA ODD CONN (FPC)

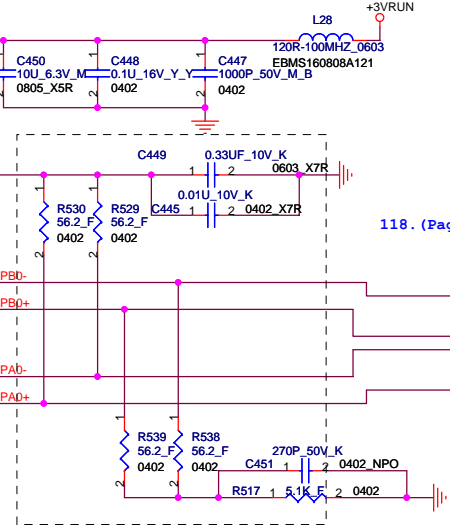
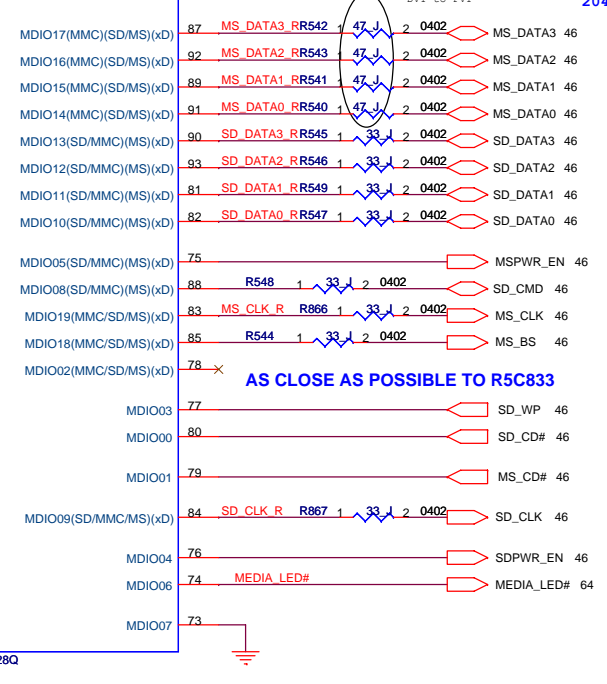




DVT to PVT 0612

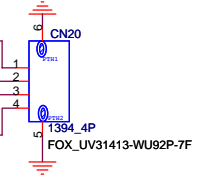


IEEE1394/SD



iLink CONN.

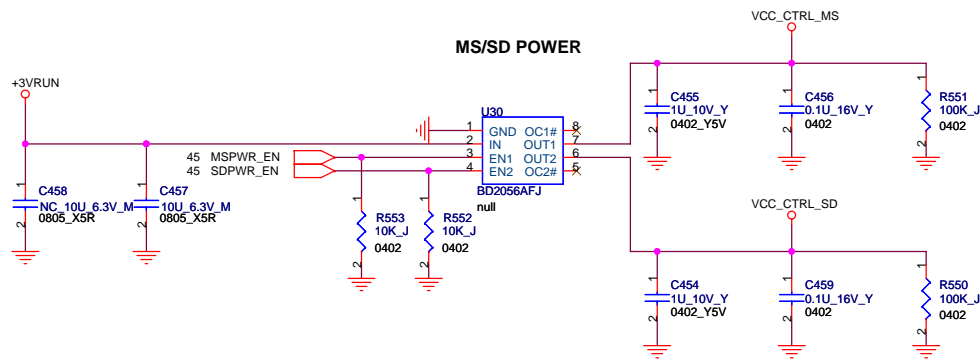
118. (Page 30) 07/11/12 Change L29 from 1L-FTR1DB6-5600 to 1L-F0D6560-TE00.



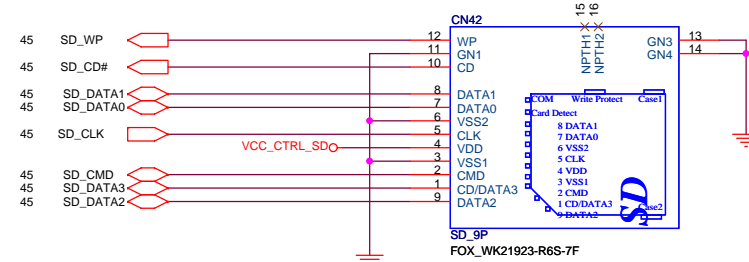
iLink CONN.

204. (Page 45) 07/11/27 change iLink CONN from FOX\_UV31413-WR56P-7F to FOX\_UV31413-WZ03P-7F.

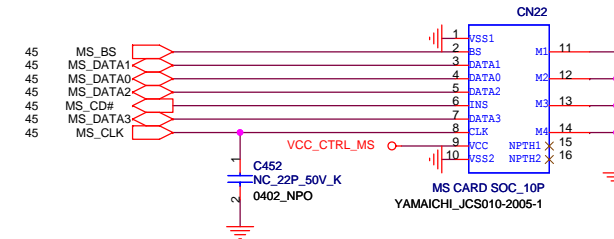
<b>FOXCONN</b> HON HAI PRECISION IND. CO., LTD.	
CPBG - R&D Division	
Title <b>PCI ( ILink )</b>	
Size A3	Document Number <b>M780(MBX-194)</b>
Date: Sunday, June 29, 2008	Rev <b>0.1</b>
Sheet 45	of 79



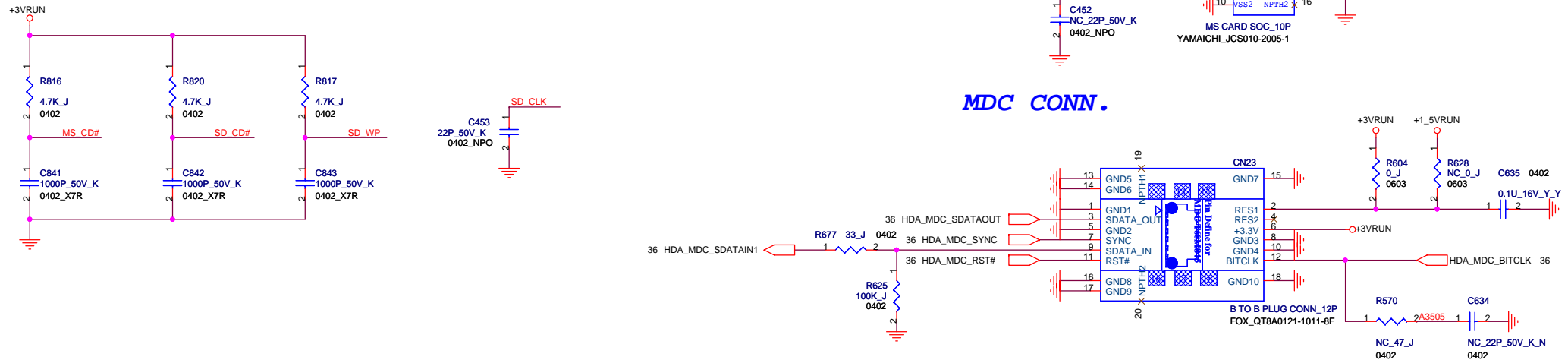
### SD CONN.

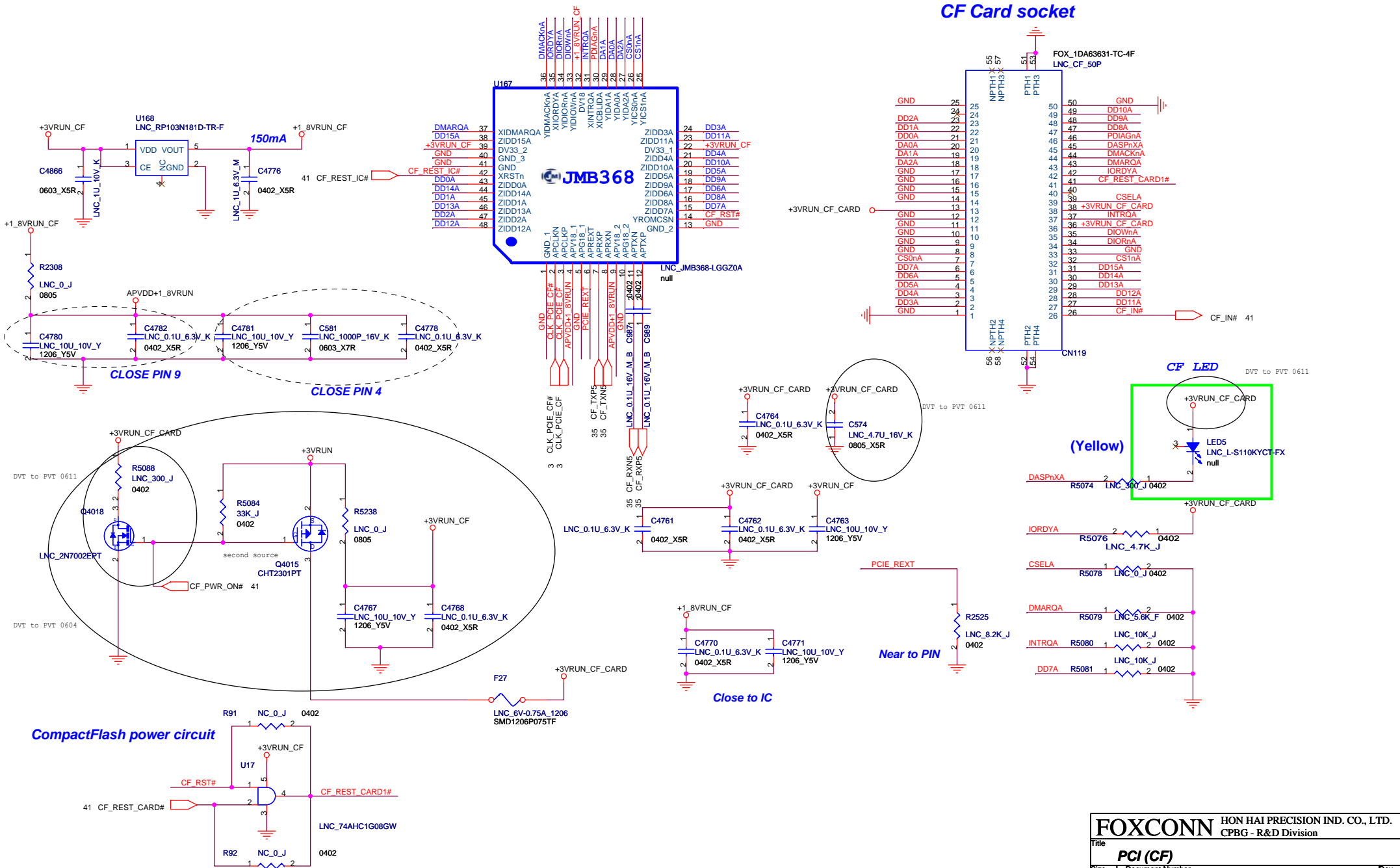


### MS STD/DUO CONN.

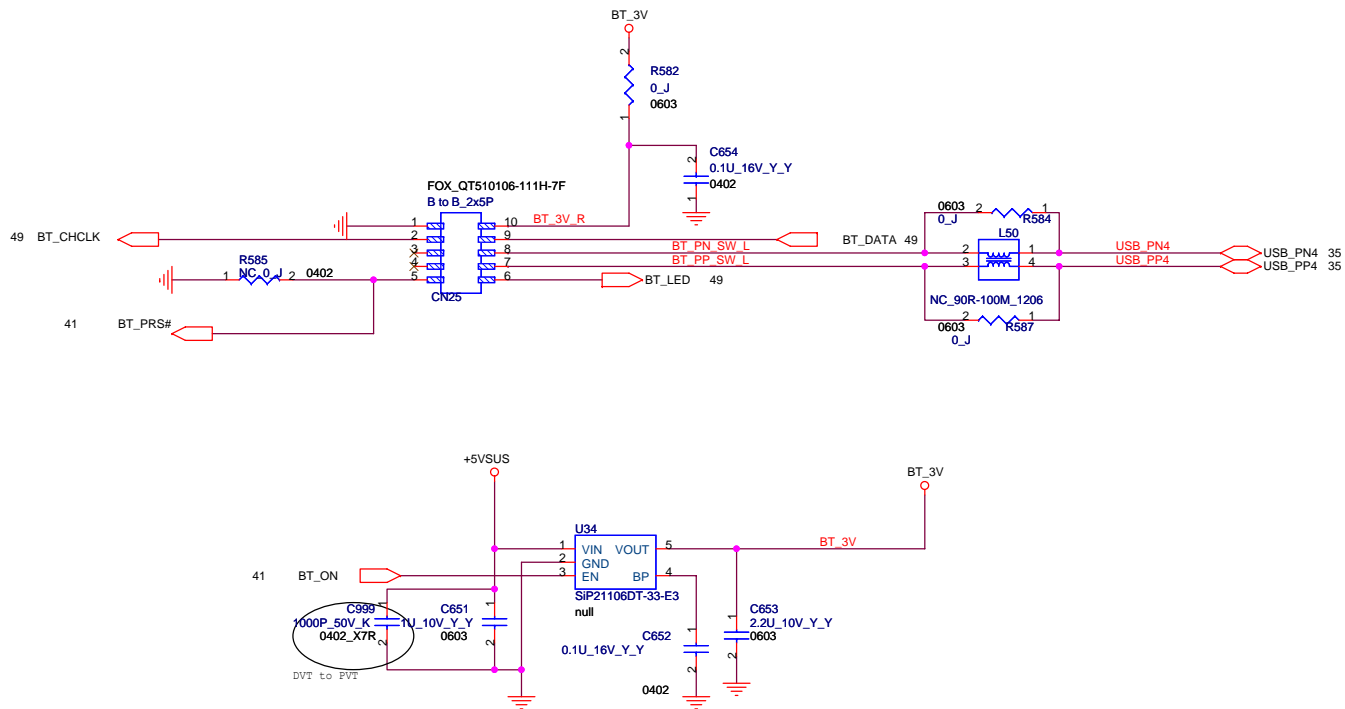


### MDC CONN.





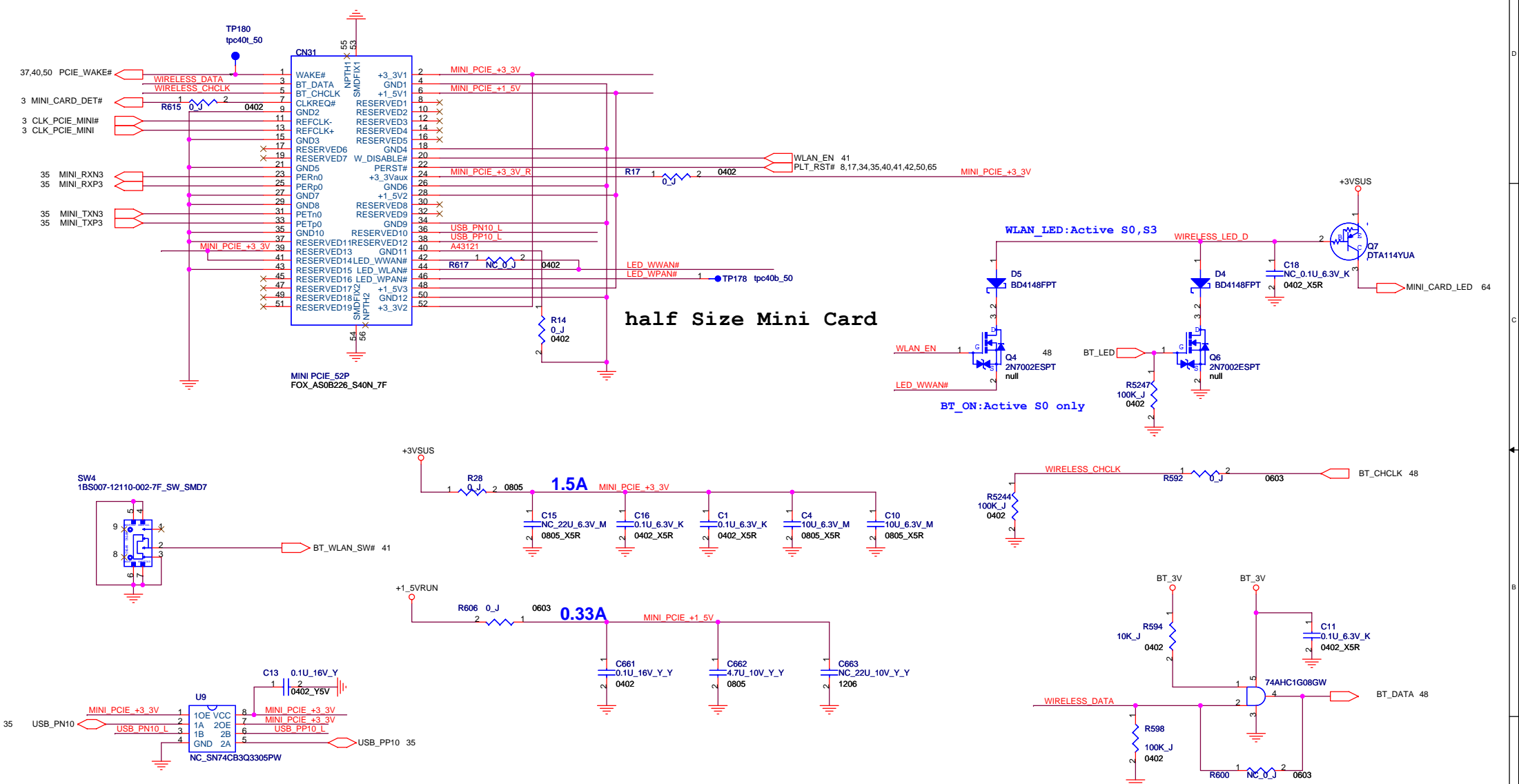
# Bluetooth connector



<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
<b>Bluetooth</b>			
Size	Document Number		
A3	<b>M780(MBX-194)</b>		
Date:	Tuesday, June 17, 2008	Sheet	48 of 79
			Rev <b>0.1</b>



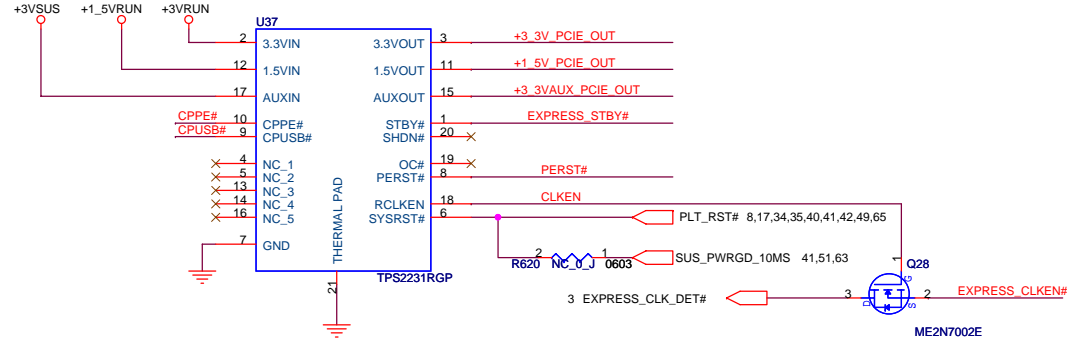
# Mini-PCIE Card connector(WLA)



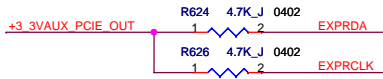
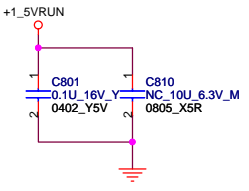
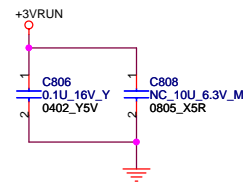
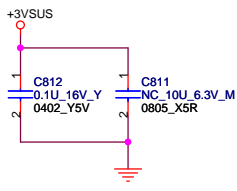
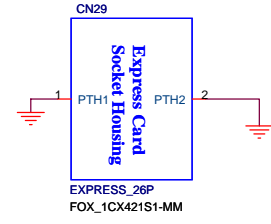
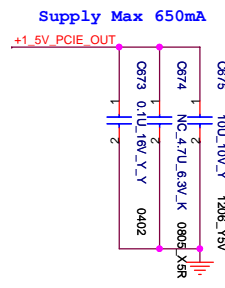
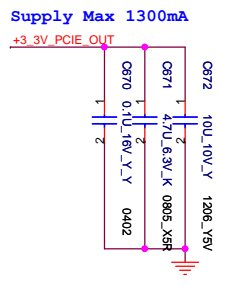
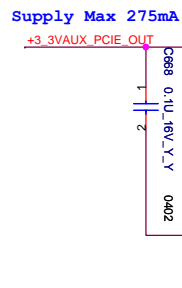
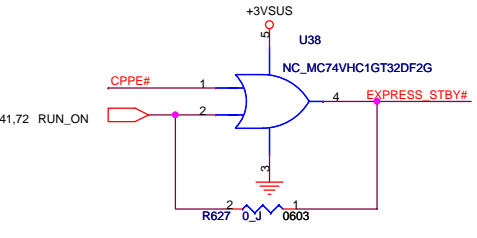
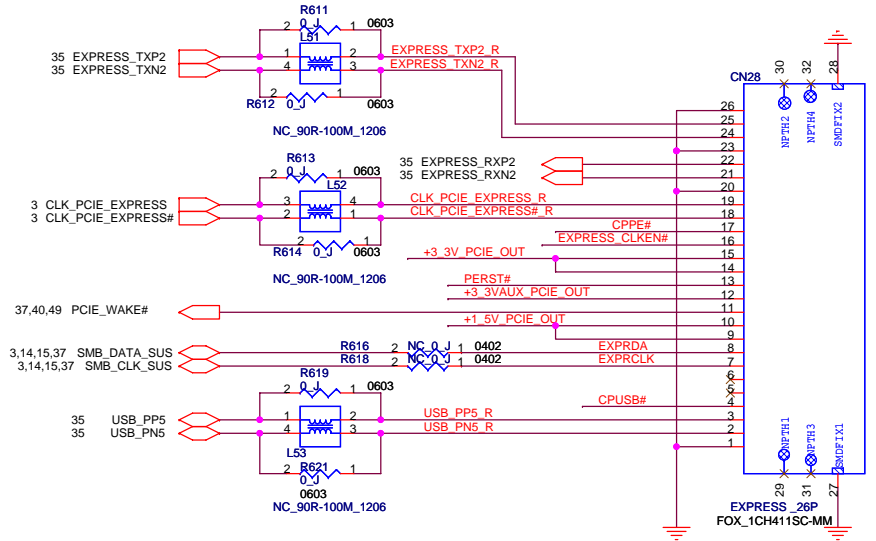
FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title <b>Mini-PCIE Card(WLA)</b>		
Size	Document Number	Rev
A3	<b>M780(MBX-194)</b>	<b>0.1</b>
Date:	Friday, June 13, 2008	Sheet 49 of 79

VOLTAGE INPUTS <sup>(1)</sup>					LOGIC INPUTS			VOLTAGE OUTPUTS <sup>(2)</sup>			MODE <sup>(3)</sup>
AUXIN	3.3VIN	1.5VIN	SHDN	STBY	CP <sup>(4)</sup>	AUXOUT	3.3VOUT	1.5VOUT			
Off	x	x	x	x	x	Off	Off	Off			OFF
On	x	x	0	x	x	GND	GND	GND			Shutdown
On	x	x	1	x	1	GND	GND	GND			No Card
On	On	On	1	0	0	Off	Off	Off			Standby
On	On	On	1	1	0	On	On	On			Card Inserted

+1\_5V=>0.65A  
+3\_3VAux=>0.275A  
+3\_3V=>1.3A

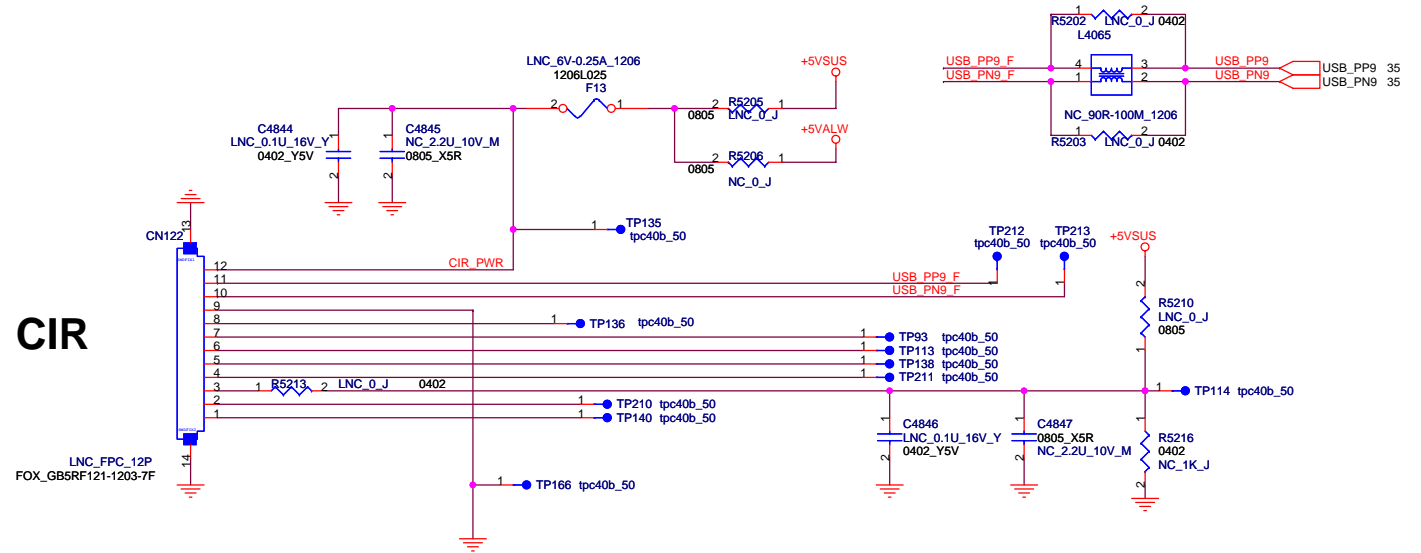


# EXPRESS Card Slot



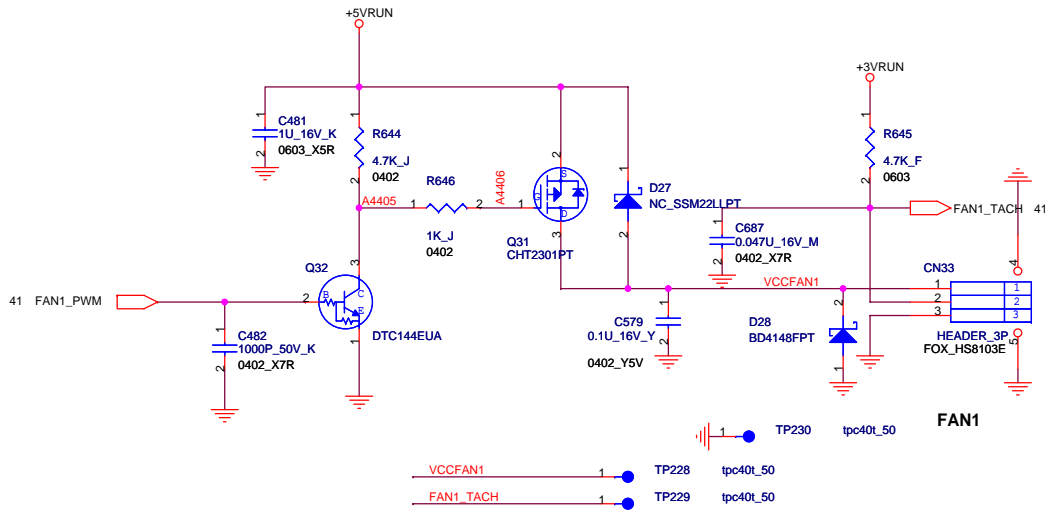


# IR Receiver connector

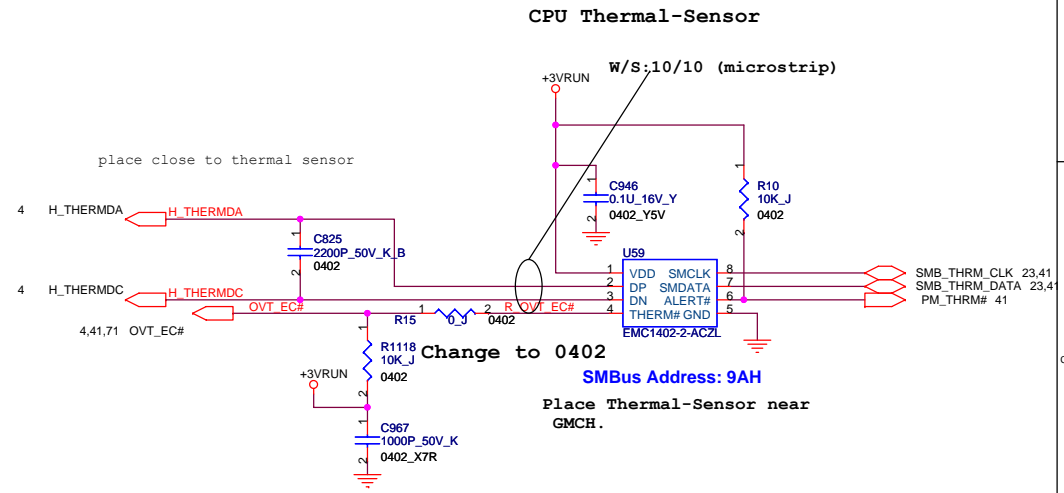


<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
<b>CIR Reciver</b>			
Size	Document Number		Rev
A3	<b>M780(MBX-194)</b>		<b>0.1</b>
Date:	Friday, June 13, 2008	Sheet	52 of 79

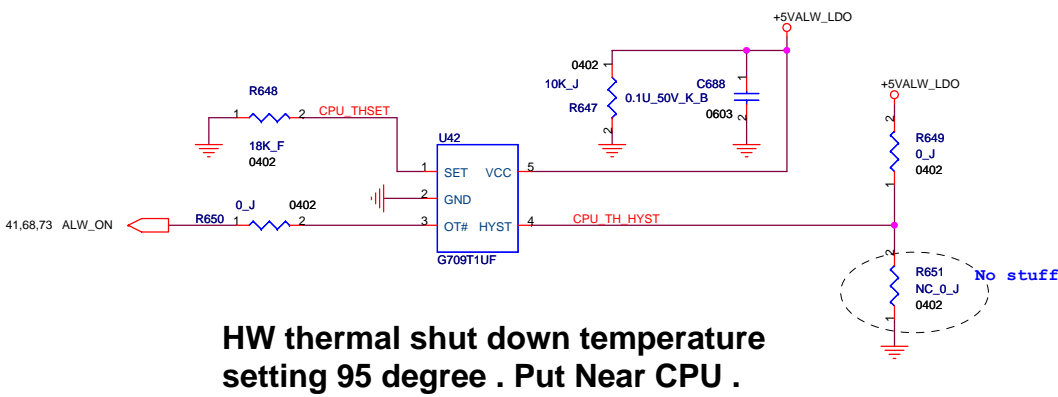
## FAN circuit



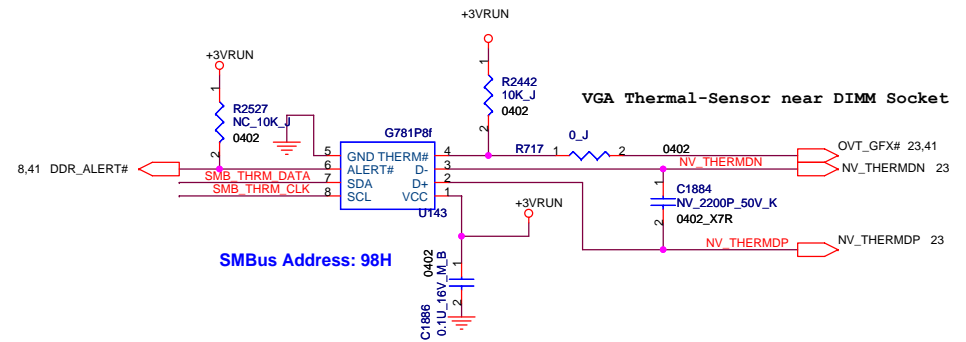
## CPU Thermal-Sensor



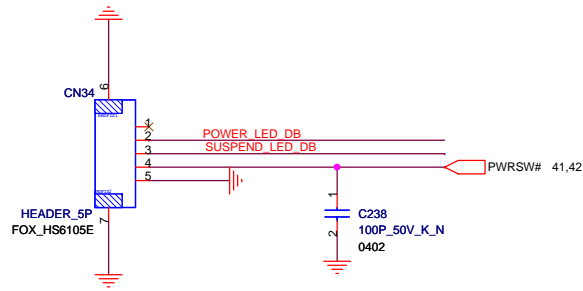
## HW THERMAL PROTECTION



## VGA Thermal-Sensor



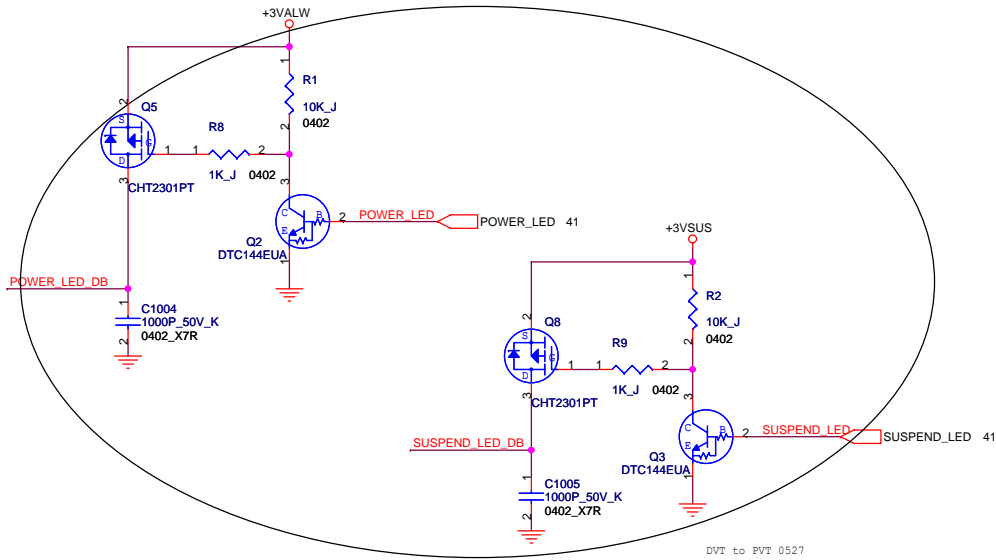
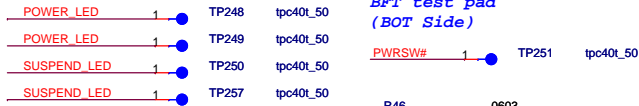
### To Power Button Board Connector



BFT test pad  
(TOP Side)



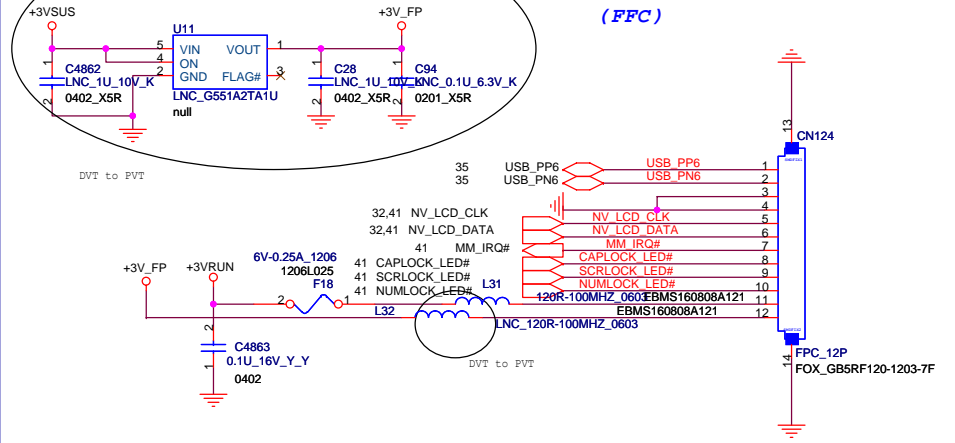
BFT test pad  
(BOT Side)



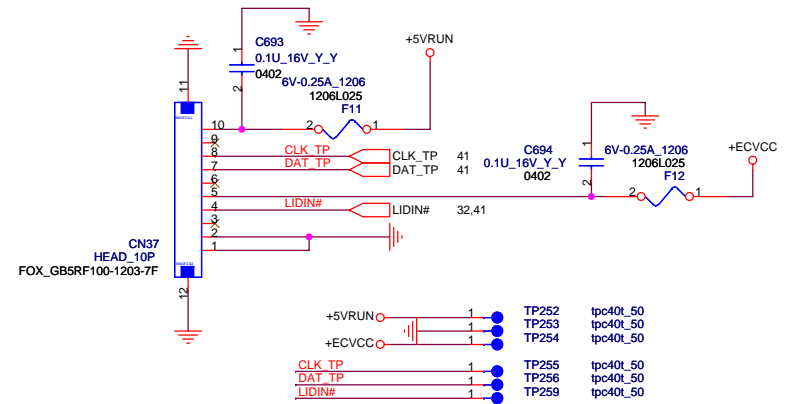
DVT to FVT 0527

### To TV Function Board Connector

(FFC)

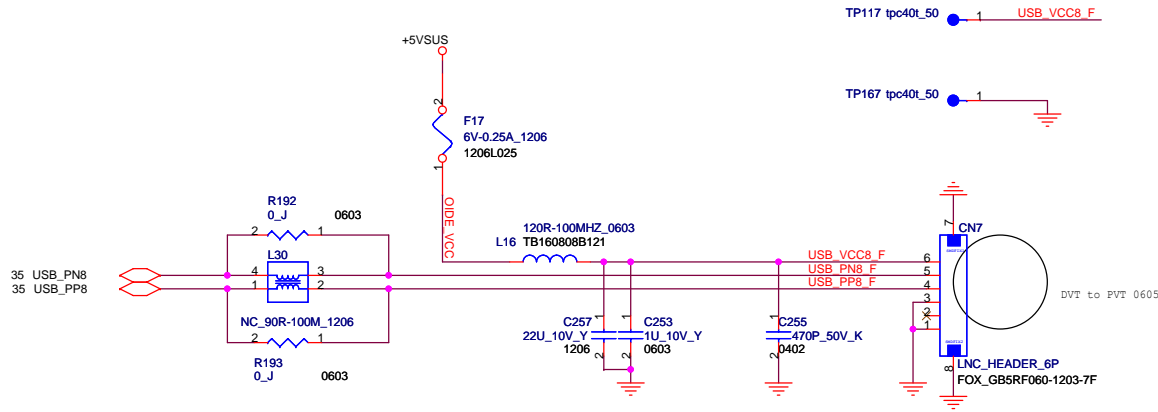


### To Touch Pad Board Connector (FFC)



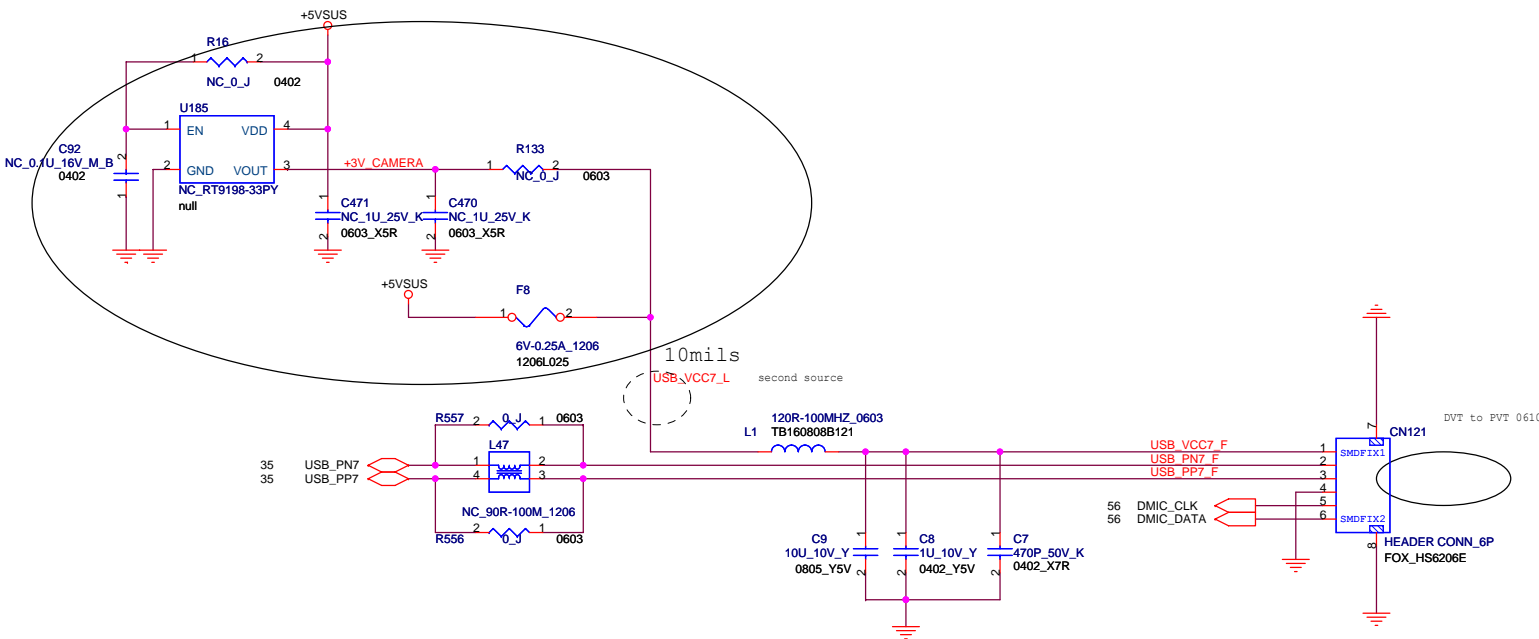
<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title <b>POWER+ FP+ T/P+LED CONNECTOR</b>			
Size	Document Number		Rev
A3	<b>M780(MBX-194)</b>		<b>0.1</b>
Date:	Friday, June 27, 2008	Sheet	54 of 79

# OIDE Connector



# CAMERA +MIC CONN.

DVT to PVT 0611



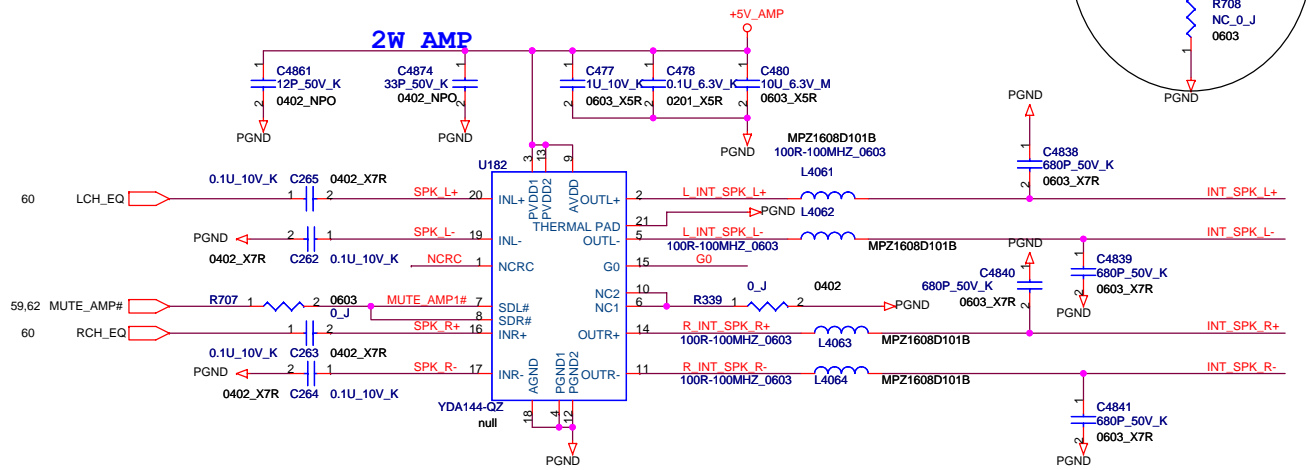
- TP51 tpc40t\_50 1 USB\_VCC7\_F
- TP126 tpc40t\_50 1 USB\_PN7\_F
- TP128 tpc40t\_50 1 USB\_PP7\_F
- TP127 tpc40t\_50 1
- TP139 tpc40t\_50 1 DMIC\_CLK
- TP160 tpc40t\_50 1 DMIC\_DATA

<b>FOXCONN</b> HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	<b>OIDE/CAM</b>	
Size	Document Number	Rev
A3	<b>M780(MBX-194)</b>	<b>0.1</b>
Date:	Friday, June 13, 2008	Sheet 55 of 79

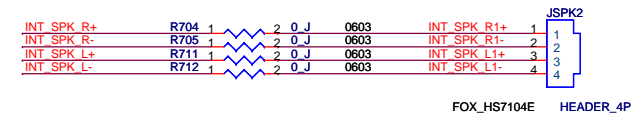




# SPEAKER AMP



# INTERNAL SPEAKER Connector

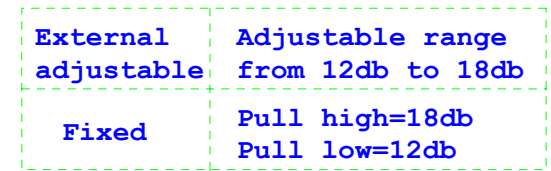


(20mil)

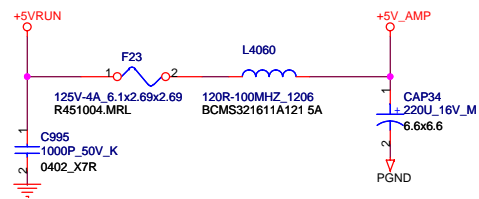
### BFT Test Pad



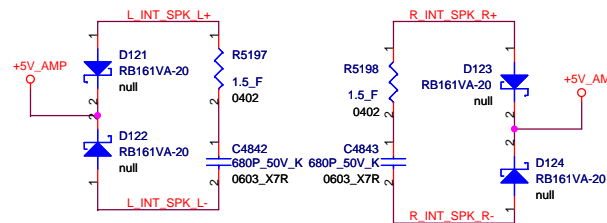
### GAIN

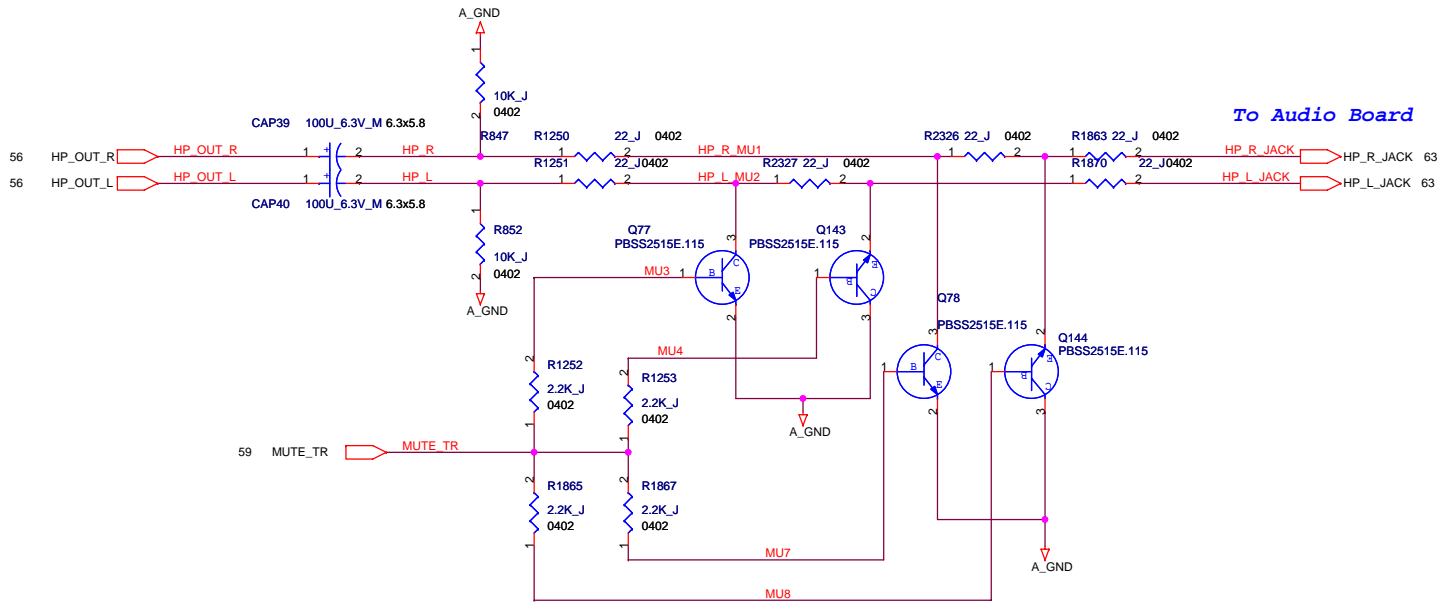


# SPEAKER POWER

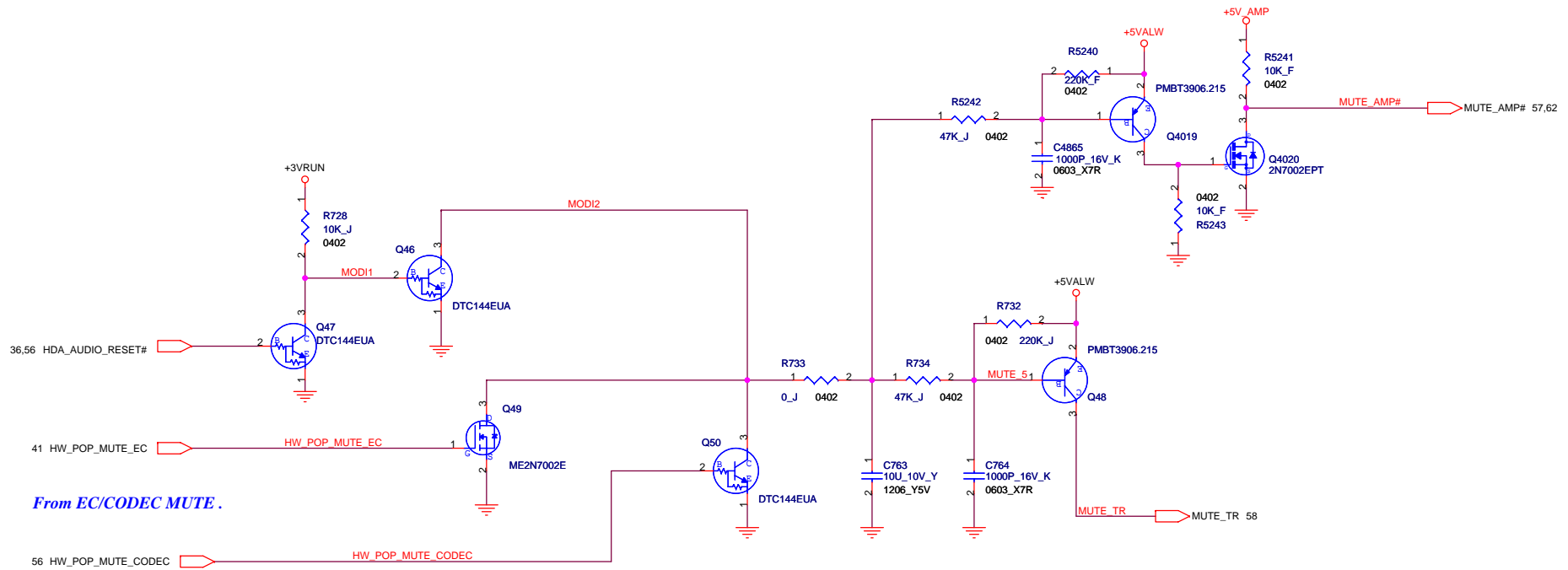


### Close to Amp





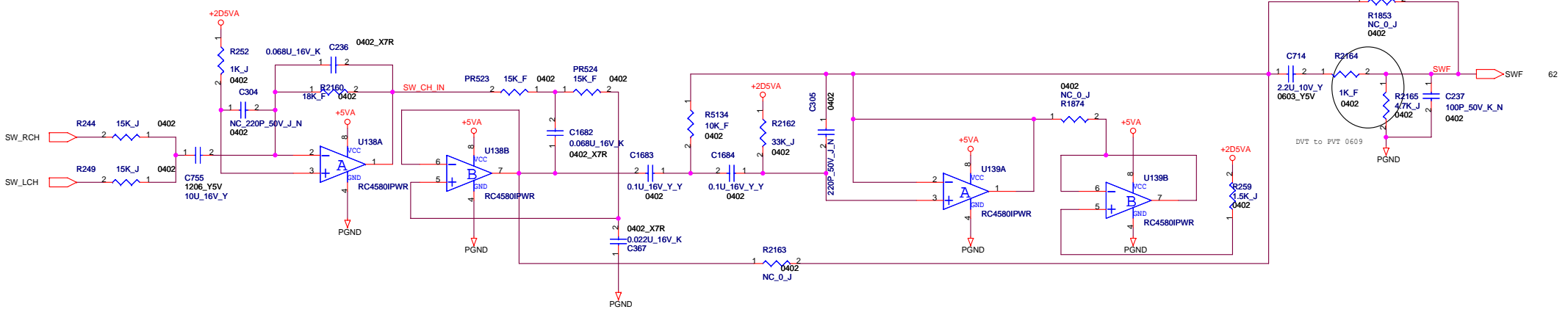
<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
<b>AUDIO (HP)</b>			
Size	Document Number		Rev
A3	<b>M780(MBX-194)</b>		<b>0.1</b>
Date:	Friday, June 13, 2008	Sheet	58 of 79





## Filter Circuit

Vendor recommendation not use for  
 1) Input impedance  
 As described in the datasheet (P5), match input impedance at IN+ and IN-.  
 We are afraid of pop noise on this board.  
 Current SWF impedance is too big, so we recommend to reduce SWF output impedance.  
 Does R2164, R2165 and C237 Circuit need?

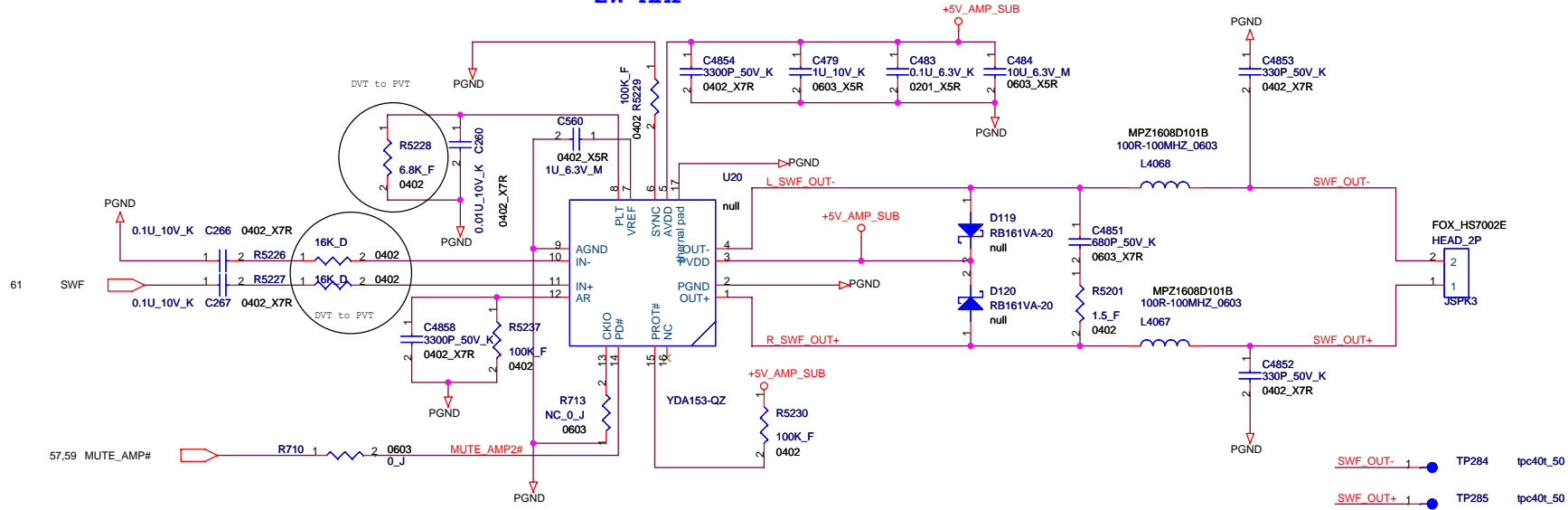


<b>FOXCONN</b> HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title <b>Filter Circuit</b>	
Size Custom	Document Number <b>M780(MBX-194)</b>
Date Friday, June 13, 2008	Rev <b>0.1</b>
Sheet 61 of 79	

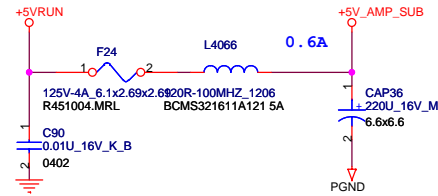
# SUB\_WOOFER AMP

C479,C484  
Locate them close to PVDD pin

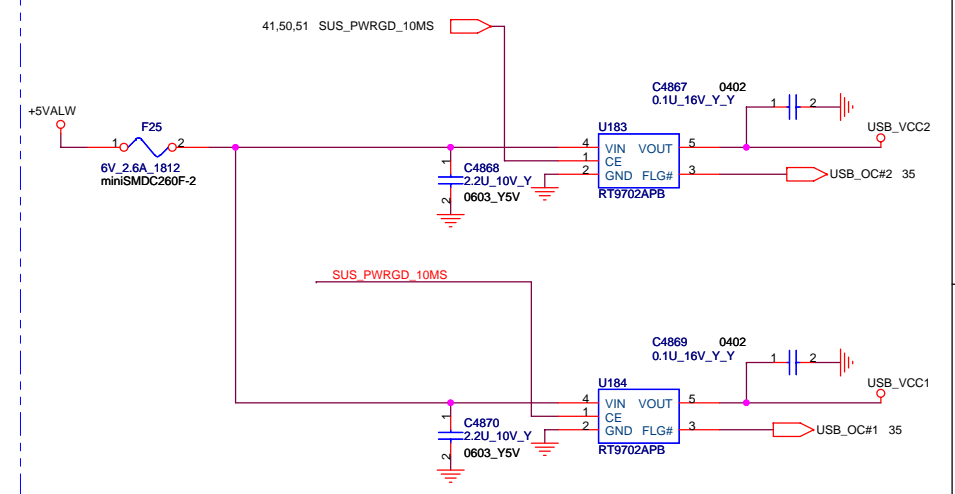
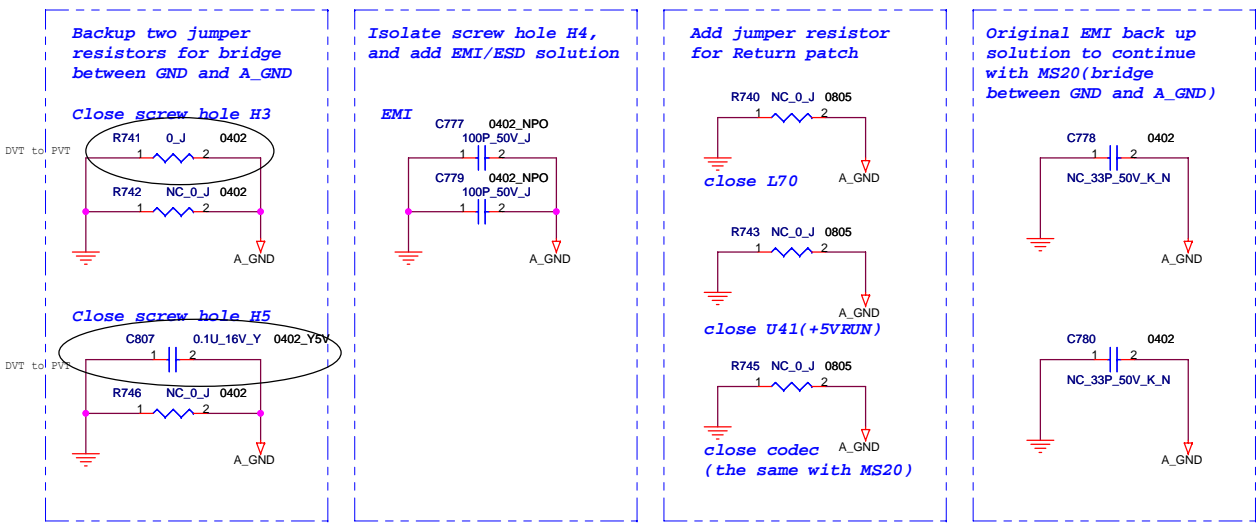
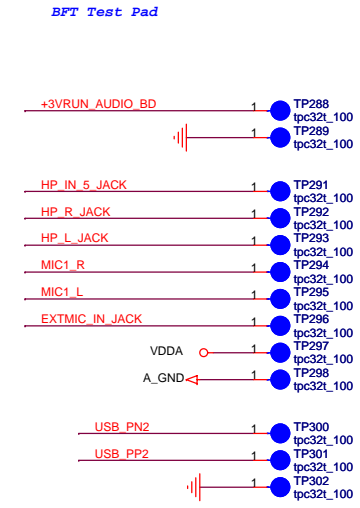
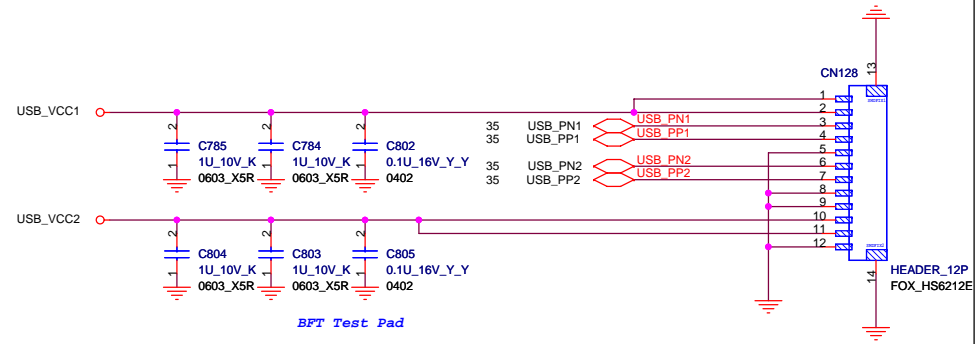
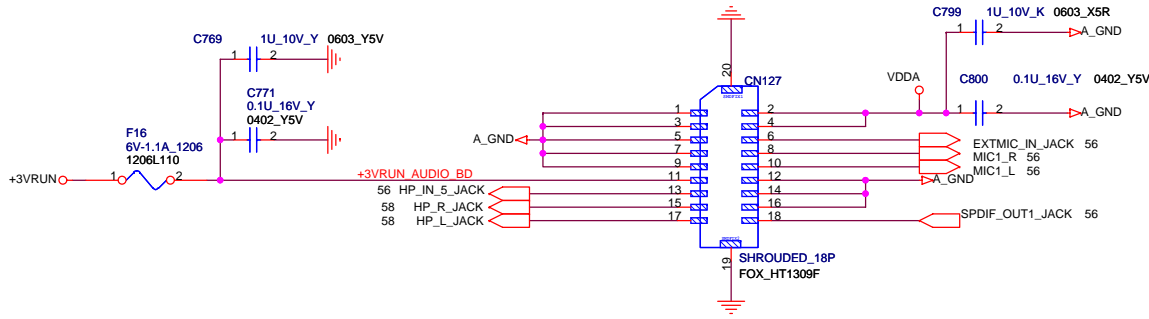
## 2W AMP



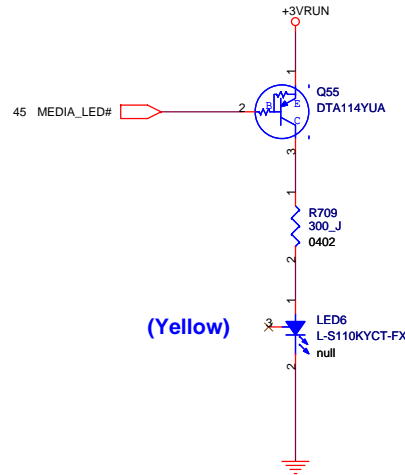
# SUB\_WOOFER POWER



# Audio Board connector

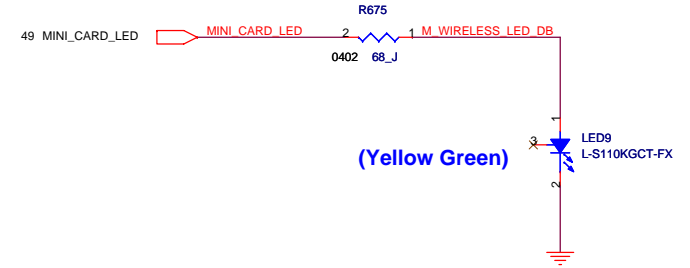


### MS/SD LED



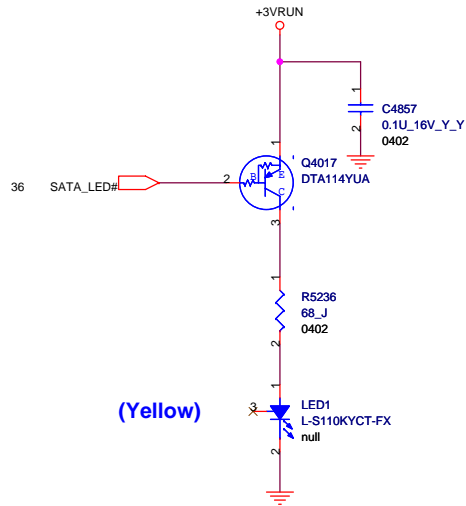
230. (Page 64) 07/12/05 Change MS/SD LED control signal share one LED

### WLAN/BLUETOOTH LED

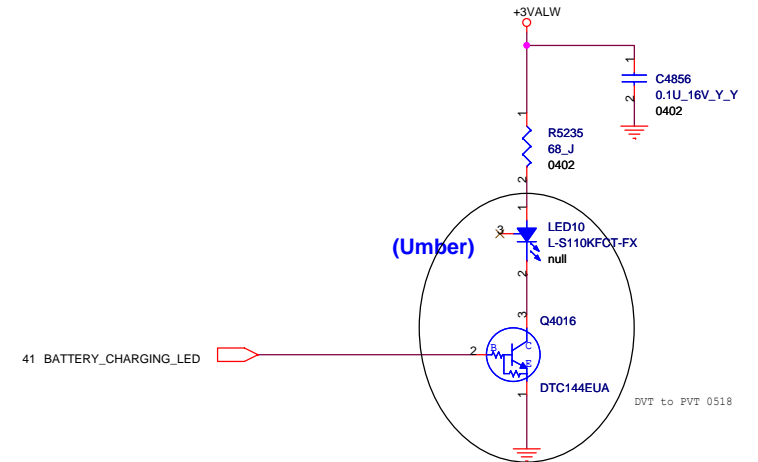


232. (Page 64) 07/12/05 Change Wireless/Bluetooth LED control signal share one LED

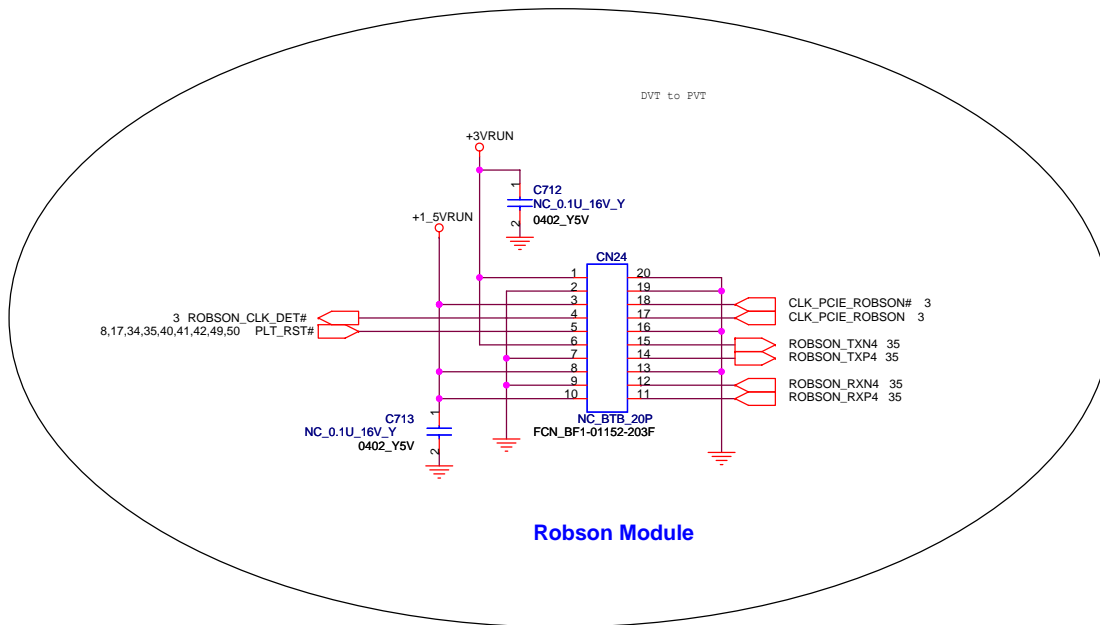
### HDD/ODD LED



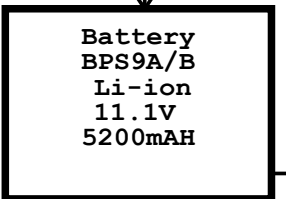
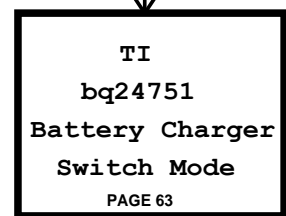
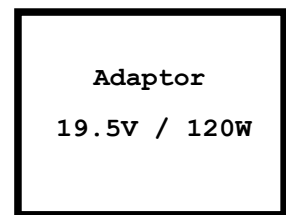
### Charge LED







<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
<b>Robson1.6 Connector</b>			
Size	Document Number		Rev
A3	<b>M780(MBX-194)</b>		<b>0.1</b>
Date:	Wednesday, June 25, 2008	Sheet	65 of 79



DCBATOUT

ALW\_ON

DCBATOUT

SUS\_ON

DCBATOUT

RUN\_ON1

DCBATOUT

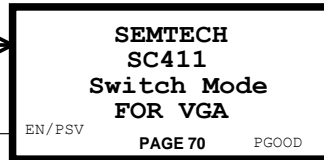
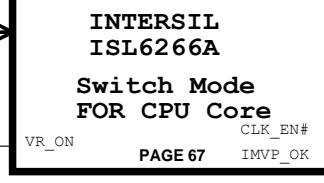
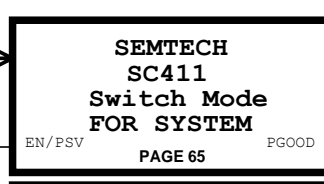
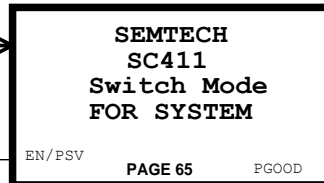
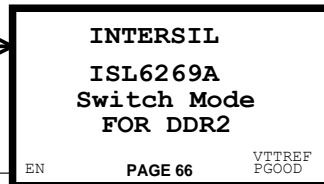
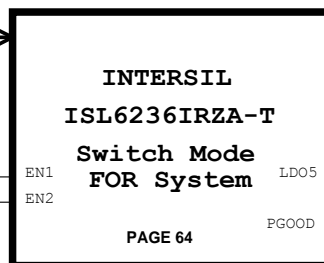
RUN\_ON1

DCBATOUT

IMVP\_VR\_ON

DCBATOUT

RUN\_ON1



System

+5VALW/6A

System

+3VALW/5A

+12V For Load switch

+1\_8VSUS/12A

+1\_05VRUN/5A

+1\_5VRUN/4.5A

VHCORE/50A

NV\_VDD (0.9V/1.2V)/21A

SUS\_ON

RUN\_ON

SUS\_ON

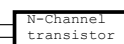
RUN\_ON

+5VALW\_LDO

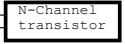
RUN\_ON2

RUN\_ON1

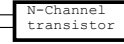
RUN\_ON1



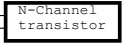
+5VSUS/1A



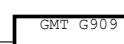
+5VRUN/4.5A



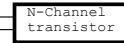
+3VSUS/1A



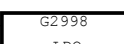
+3VRUN/3.5A



+ECVCC/100mA



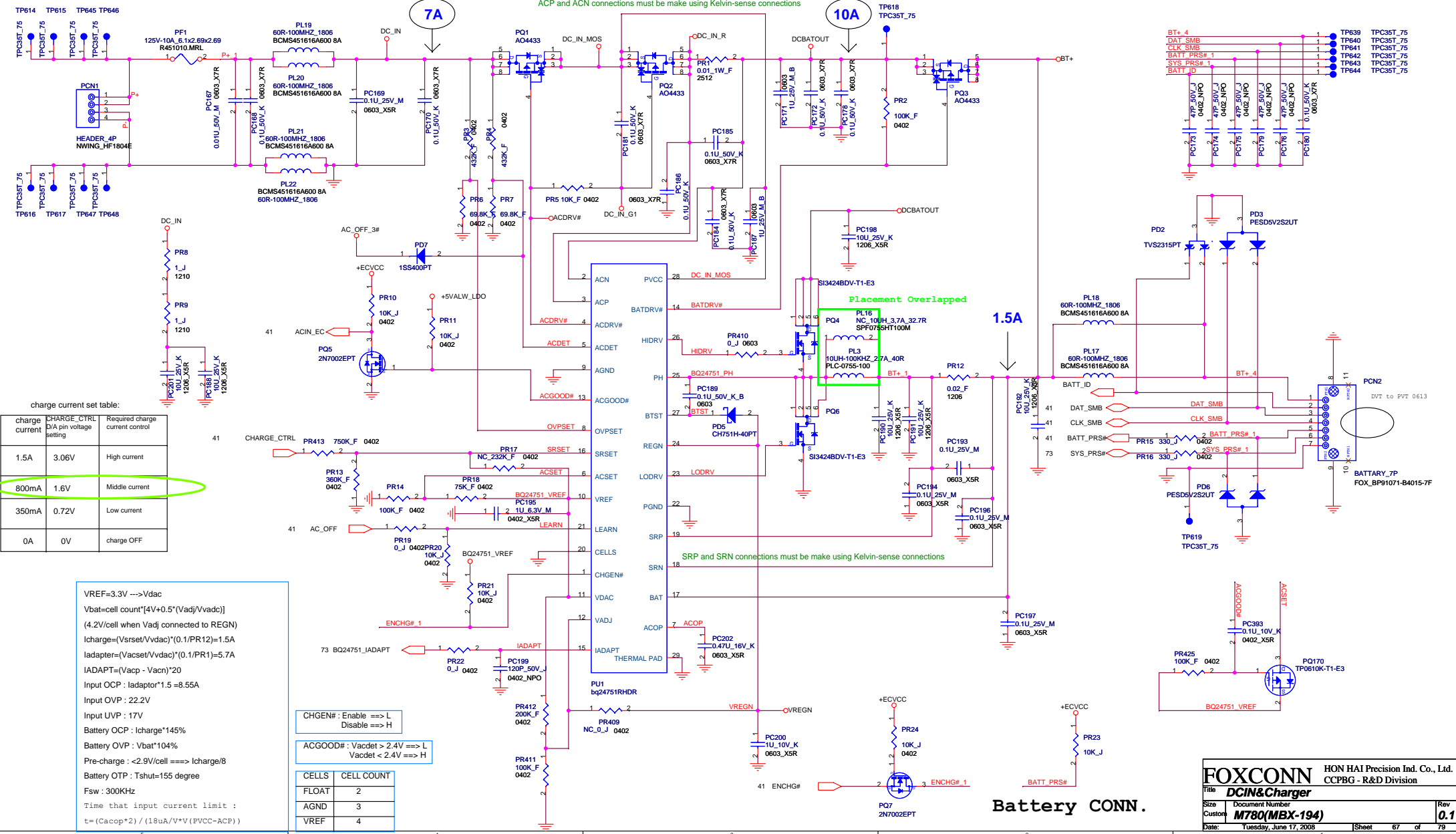
+1\_8VRUN/5A



PEX\_VDD (0.9V)/2A



PEX\_VDD (1.113V)/1.6A



charge current set table:

Charge current	CHARGE_CTRL D/A pin voltage setting	Required charge current control
1.5A	3.06V	High current
800mA	1.6V	Middle current
350mA	0.72V	Low current
0A	0V	charge OFF

VREF=3.3V --->Vdac  
 $V_{bat} = \text{cell count} * [4V + 0.5 * (V_{adj} / V_{vdac})]$   
 (4.2V/cell when Vadj connected to REGN)  
 $I_{charge} = (V_{srset} / V_{vdac}) * (0.1 / PR12) = 1.5A$   
 $I_{adaptor} = (V_{vacset} / V_{vdac}) * (0.1 / PR1) = 5.7A$   
 $IADAPT = (V_{vacp} - V_{vacn}) * 20$   
 Input OCP :  $I_{adaptor} * 1.5 = 8.55A$   
 Input OVP : 22.2V  
 Input UVP : 17V  
 Battery OCP :  $I_{charge} * 145\%$   
 Battery OVP :  $V_{bat} * 104\%$   
 Pre-charge :  $< 2.9V / \text{cell} ==> I_{charge} / 8$   
 Battery OTP :  $T_{shut} = 155 \text{ degree}$   
 $F_{sw} = 300KHz$   
 Time that input current limit :  
 $t = (C_{acop} * 2) / (18uA / V * V (PVCC - ACP))$

CHGEN# : Enable ==> L	Disable ==> H
ACGOOD# : Vacdet > 2.4V ==> L	Vacdet < 2.4V ==> H
CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

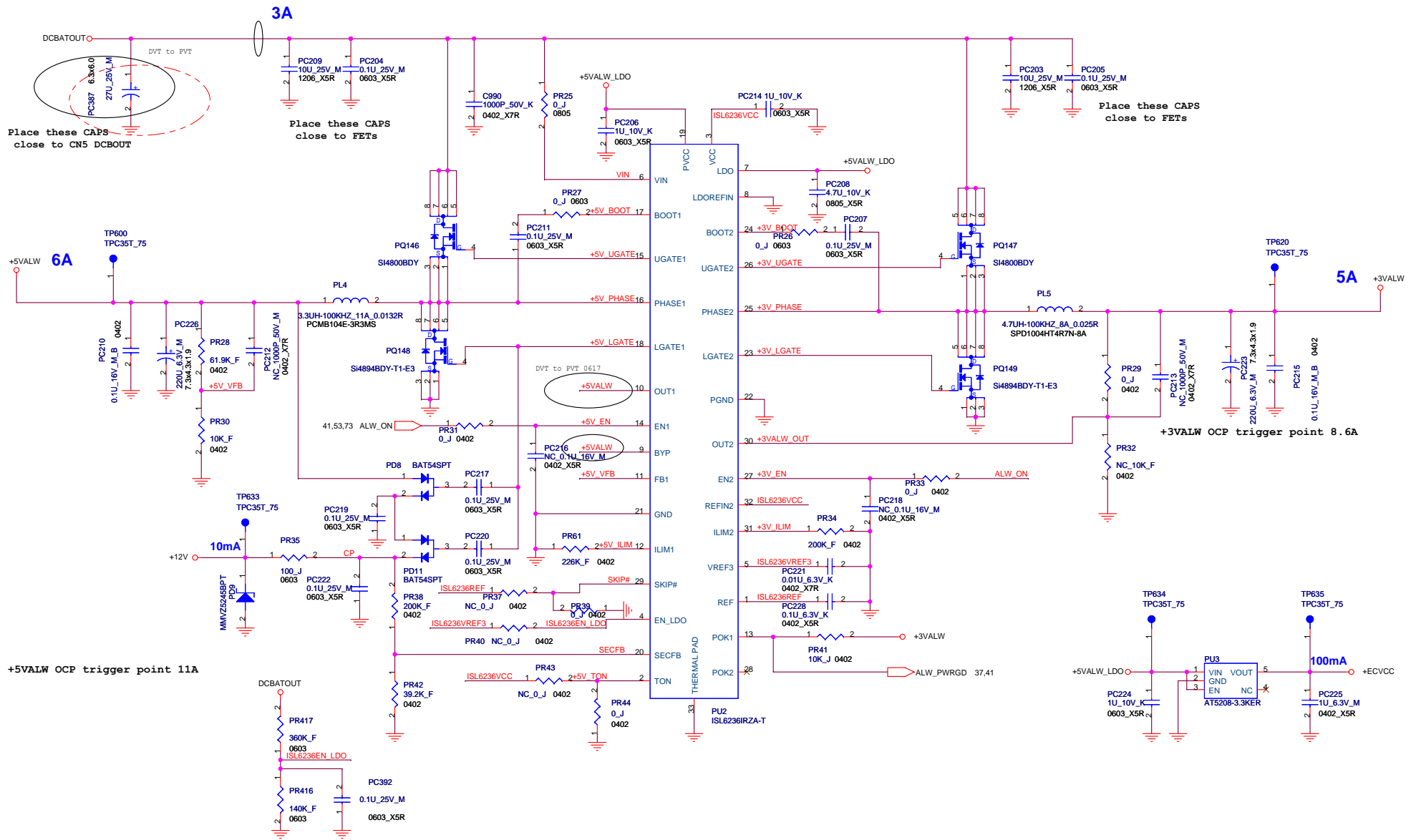
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

Title: **DCIN&Charger**

Size: Document Number  
 Custom: **M780(MBX-194)** Rev: **0.1**

Date: Tuesday, June 17, 2008 | Sheet: 67 of 79

**Battery CONN.**



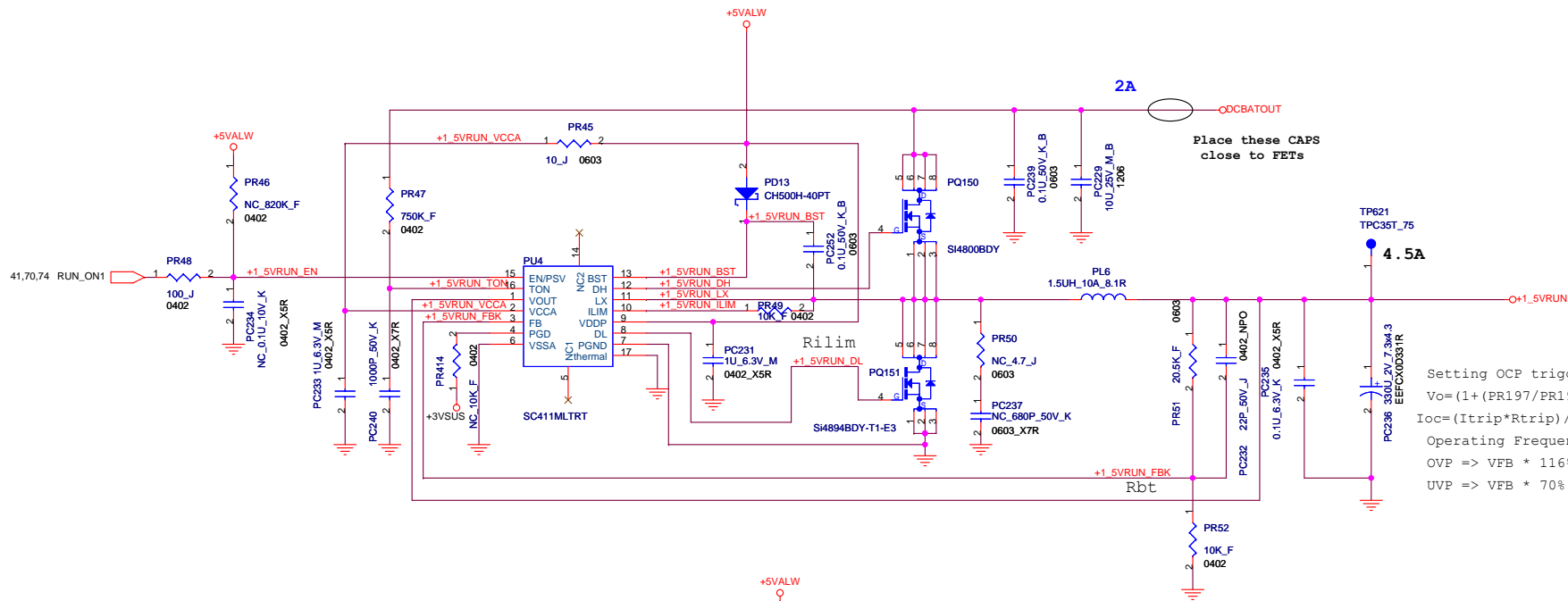
TON	Operating Frequency (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

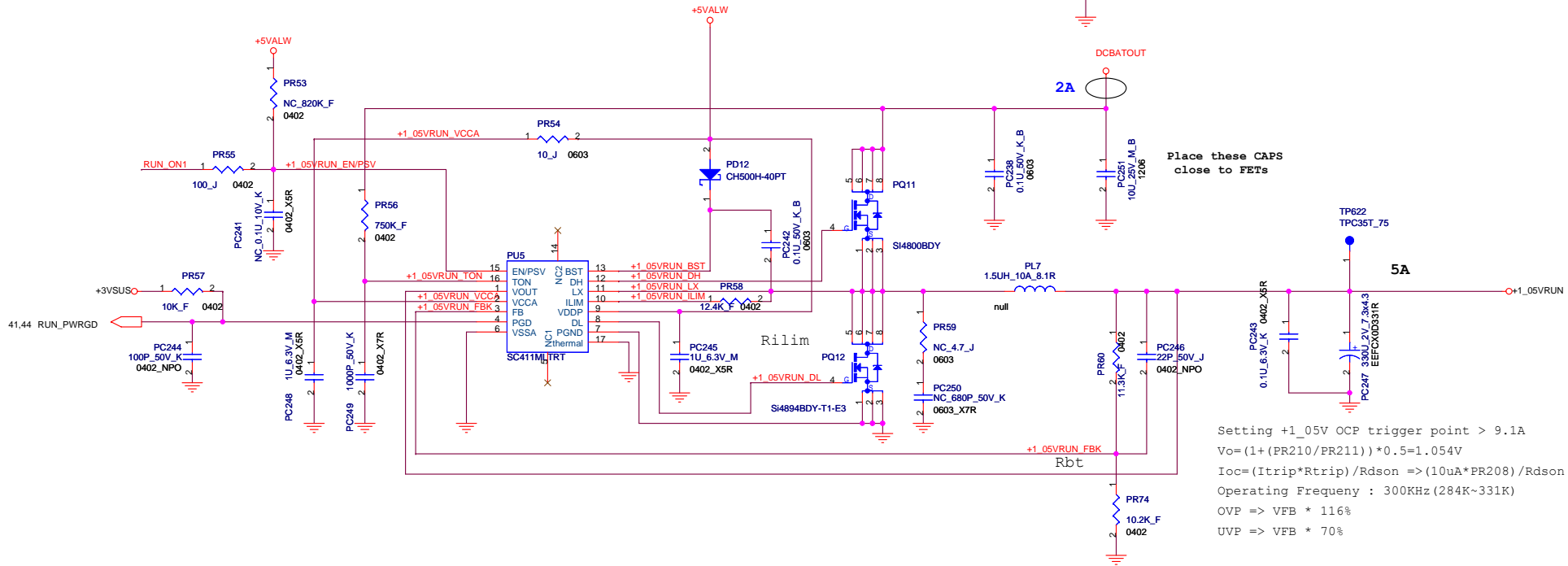
$$L = VOUT (VIN - VOUT) / (VIN * f * LIR * ILOAD (MAX))$$

$$Rocp = (Iocp - Iripple / 2) * (10 * Rds(on)) / 5u$$

$$+5VALW = ((PR28 / PR30) + 1) * VFB1$$

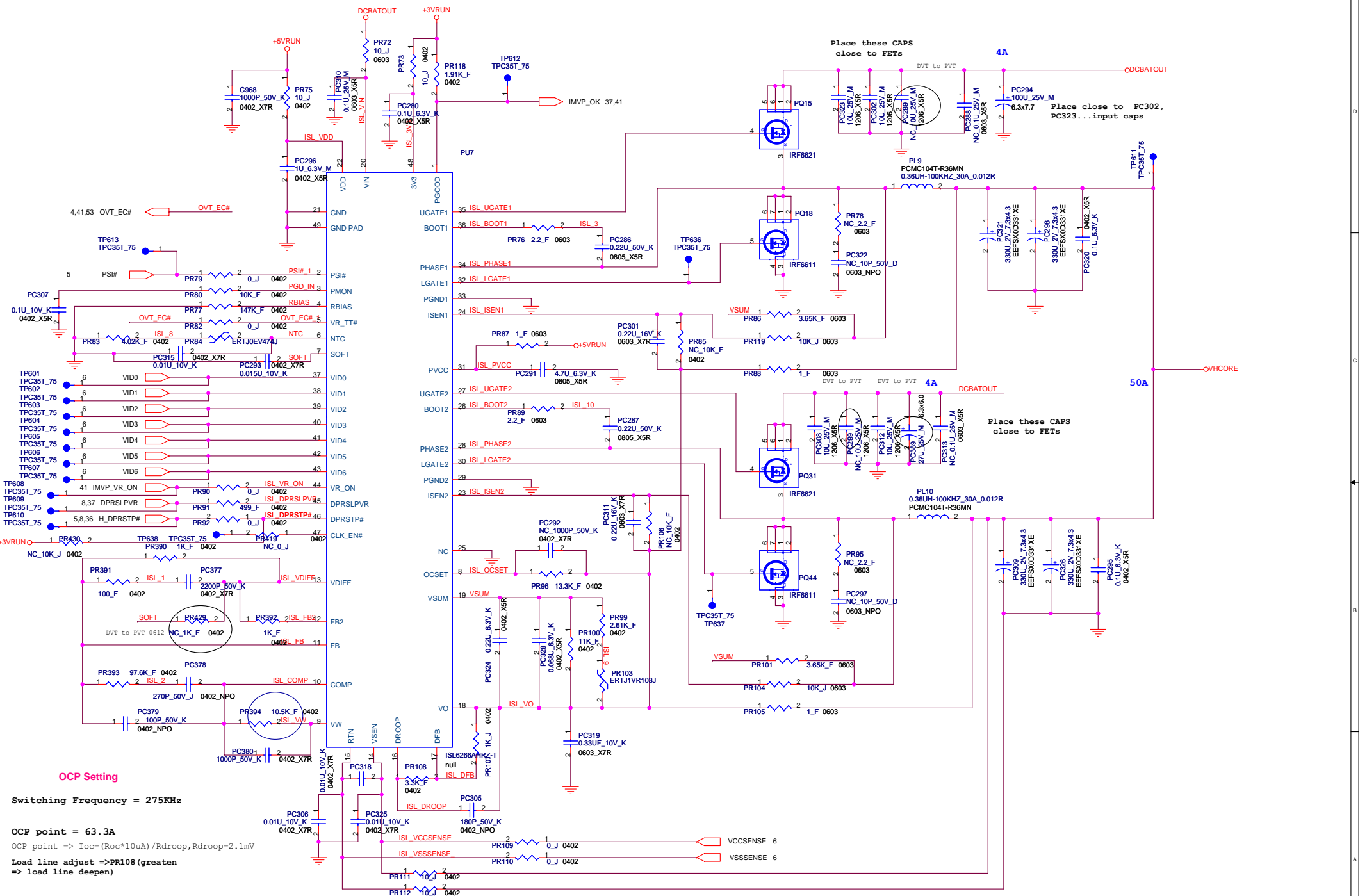


Setting OCP trigger point > 7.5A  
 $V_o = (1 + (PR197/PR198)) * 0.5 = 1.525V$   
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} = (10\mu A * PR194) / R_{dson}$   
 Operating Frequency : 330KHz (308K~345K)  
 OVP => VFB \* 116%  
 UVP => VFB \* 70%



Setting +1.05V OCP trigger point > 9.1A  
 $V_o = (1 + (PR210/PR211)) * 0.5 = 1.054V$   
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} = (10\mu A * PR208) / R_{dson}$   
 Operating Frequency : 300KHz (284K~331K)  
 OVP => VFB \* 116%  
 UVP => VFB \* 70%





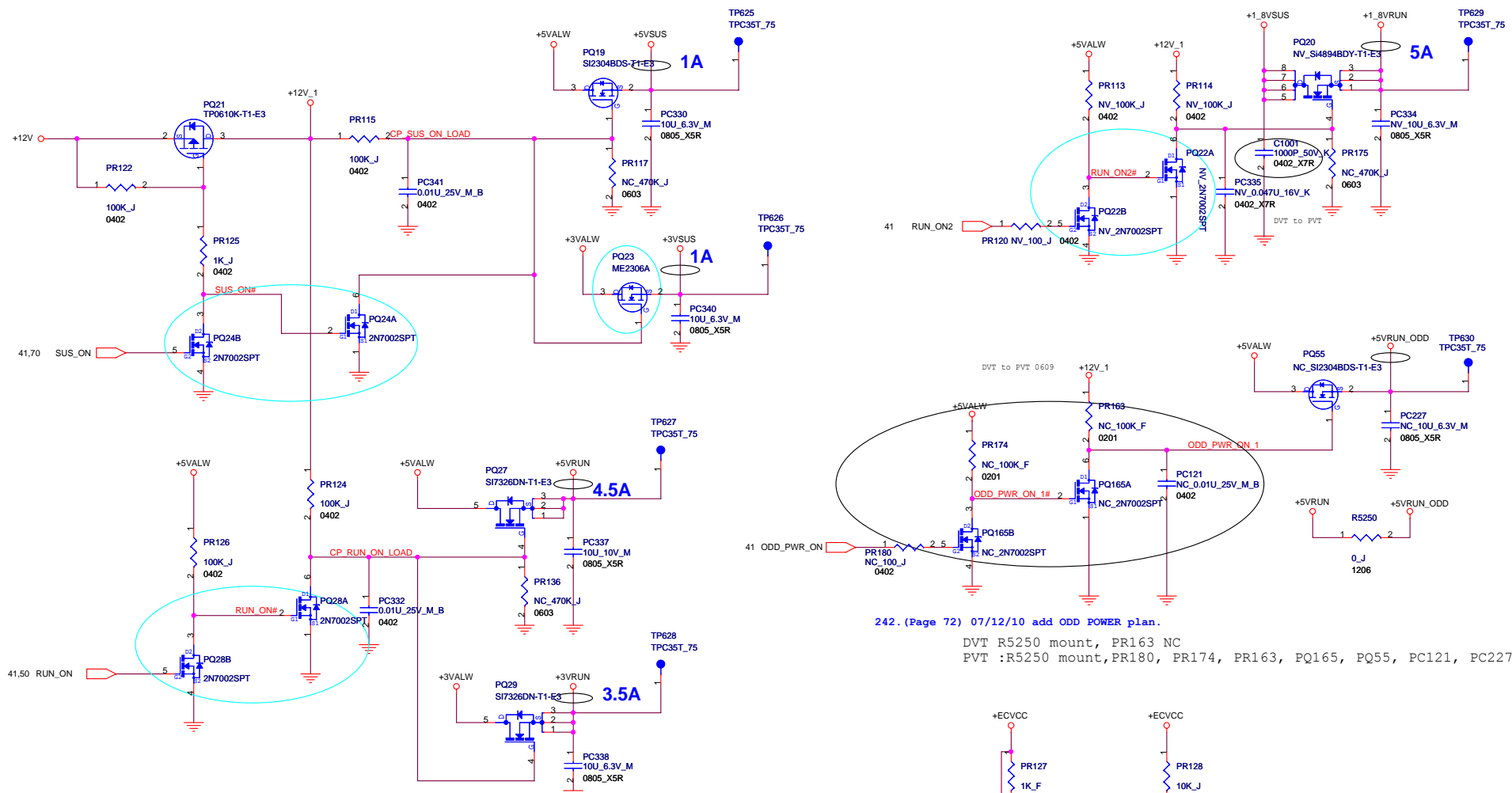
**OCP Setting**

Switching Frequency = 275KHz

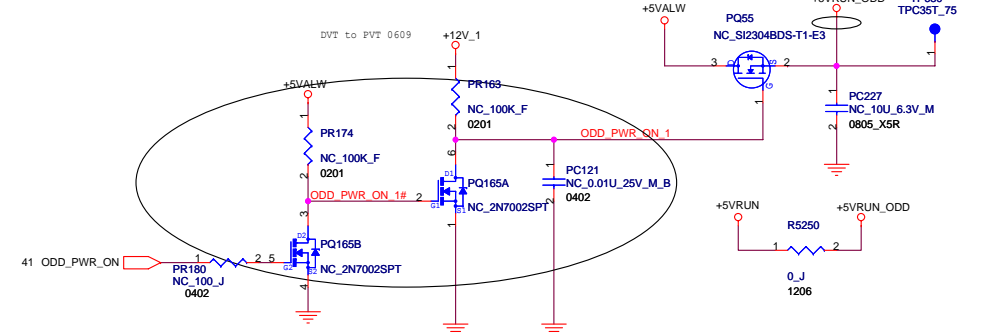
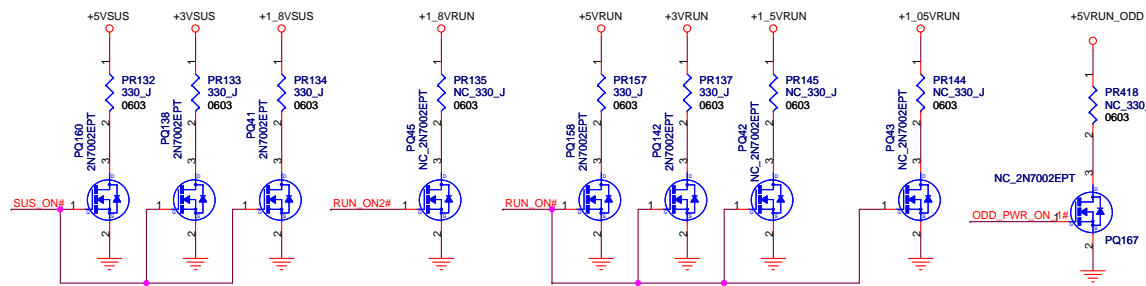
OCP point = 63.3A

OCP point =>  $I_{oc} = (R_{oc} * 10\mu A) / R_{droop}$ ,  $R_{droop} = 2.1m\Omega$

Load line adjust => PR108 (greater => load line deepen)

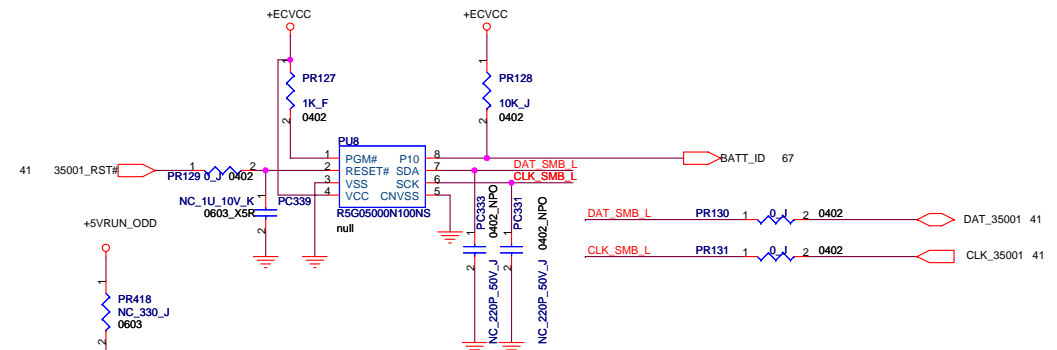


Discharge circuit for power-off

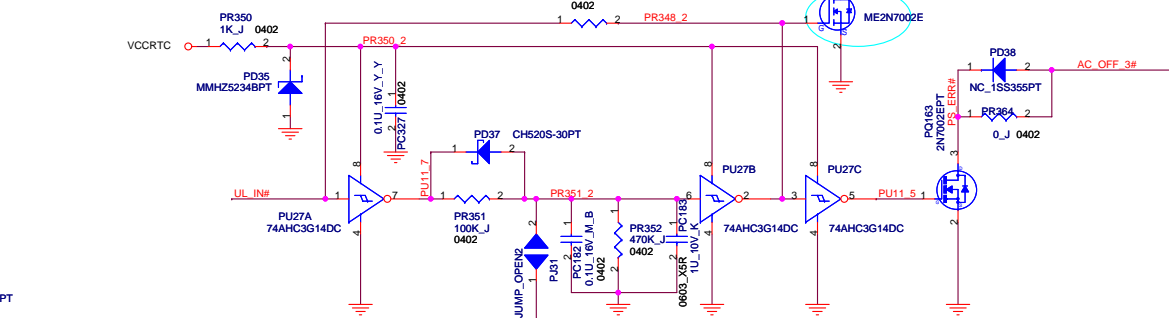
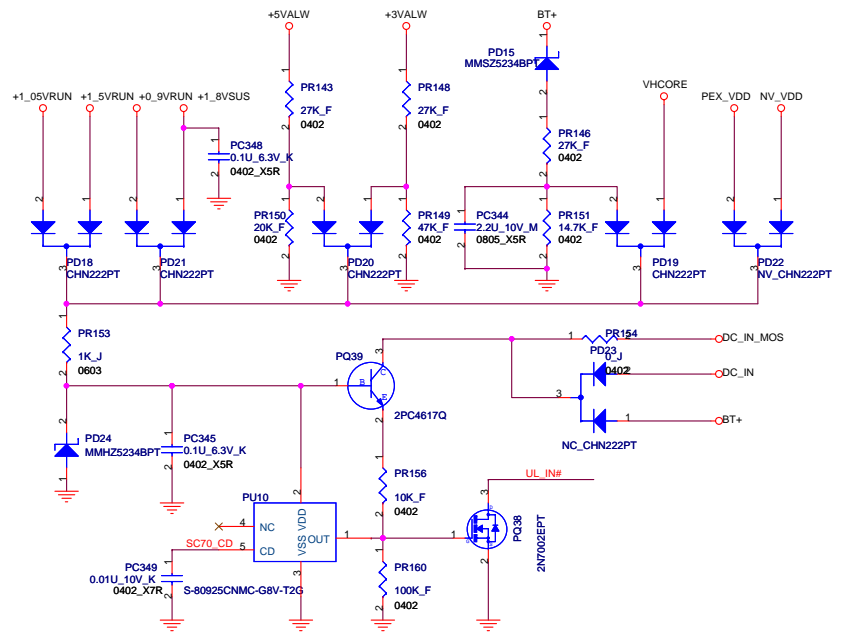


242. (Page 72) 07/12/10 add ODD POWER plan.

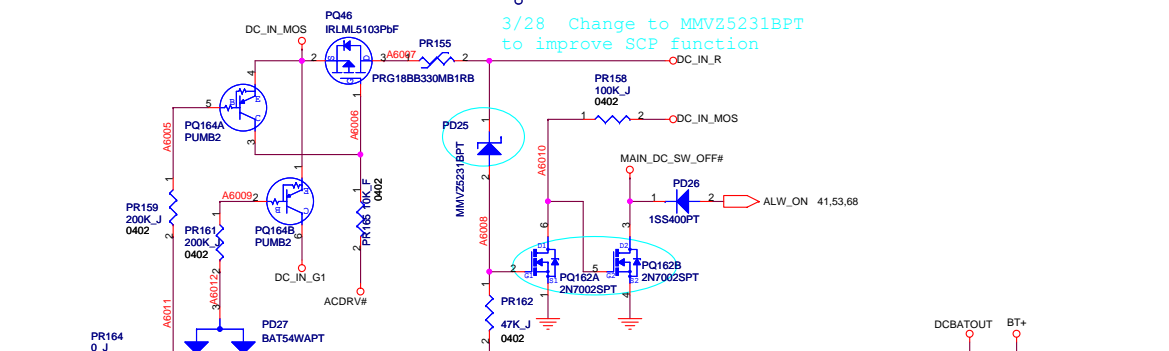
DVT R5250 mount, PR163 NC  
PVT :R5250 mount,PR180, PR174, PR163, PQ165, PQ55, PC121, PC227 all NC







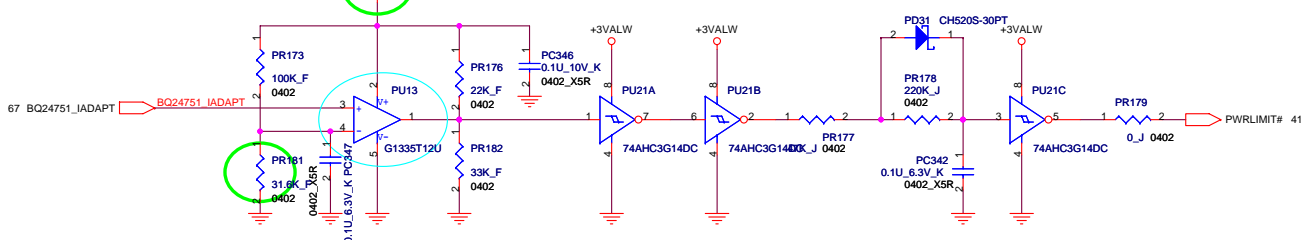
3/28 Change to MMV25231BPT to improve SCP function



**System SCP protect**

**Battery UVP protect**

Change VREGN to +5VALW\_LDO



120W adaptor

PWRLIMIT	1.2V/114W
----------	-----------

Adaptor max load: 7.7A under 3 sec  
Adaptor OCP: 9.7A typ  
11A max

3/28 Add battery UVP protect circuit to separate SCP and OCP function.

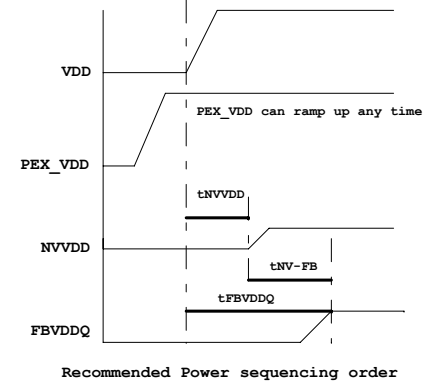
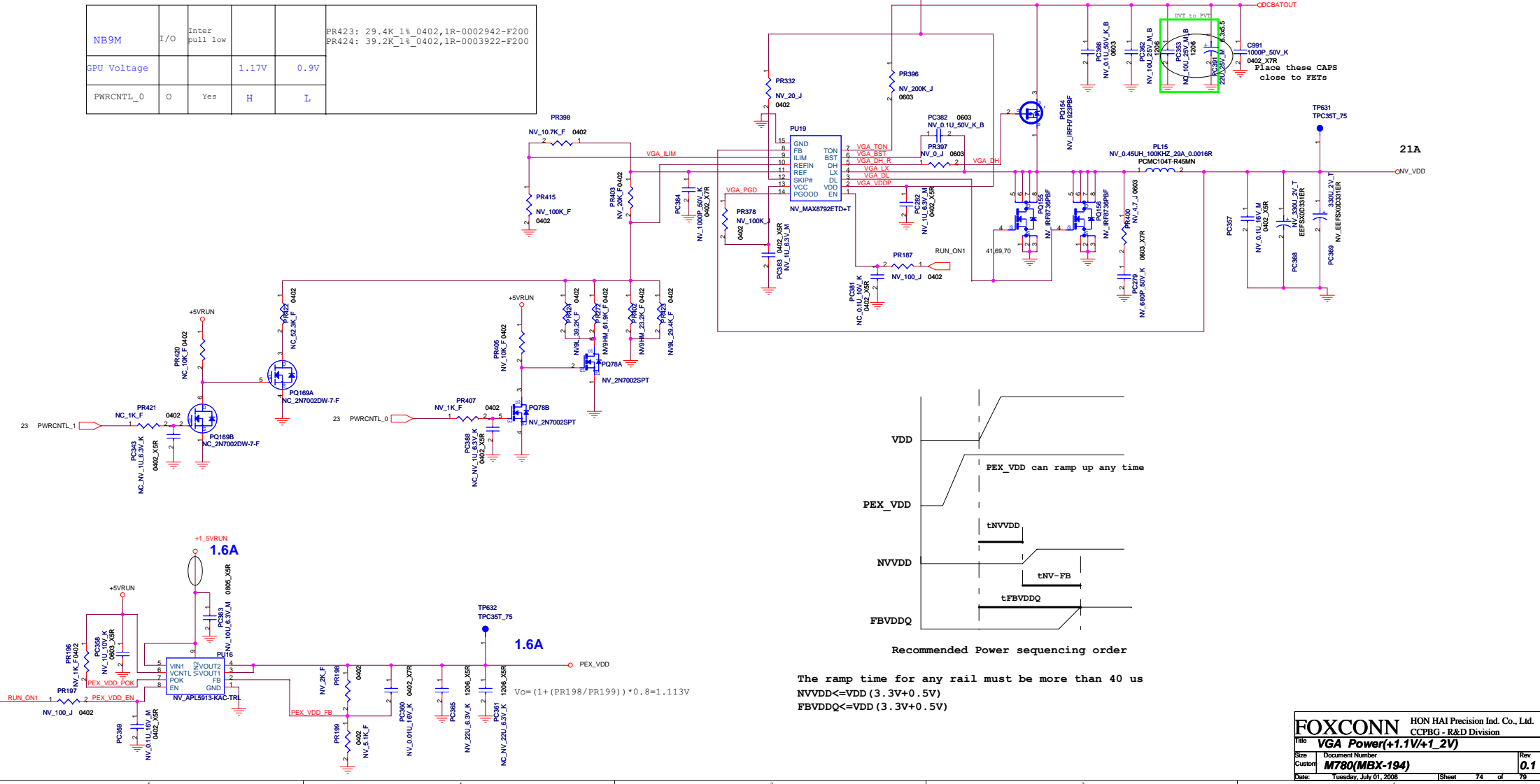
<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
<b>OVP protection</b>			
Size	Document Number	Rev	
Custom	<b>M780(MBX-194)</b>	<b>0.1</b>	
Date:	Friday, June 13, 2008	Sheet	73 of 79

TABLE (01/08)

NB9P	I/O	Inter pull low			PR402: 23.2K 1%_0402,1R-0002322-F200 PR272: 61.9K 1%_0402,1R-0006192-F200
GPU Voltage			1.05V	0.9V	
PWRCNTL_0	O	Yes	H	L	

NB9M	I/O	Inter pull low			PR423: 29.4K 1%_0402,1R-0002942-F200 PR424: 39.2K 1%_0402,1R-0003922-F200
GPU Voltage			1.17V	0.9V	
PWRCNTL_0	O	Yes	H	L	

Setting current limit trigger point >25A  
 $V_o = V_i$ ;  $V_f = ((PR272 + PR402) / (PR403 + PR272 + PR402)) * 2$   
 $V_{lim} = 20 [I_o - I_r / 2] * R_{low-dsn} * 1.2$   
 Operating Frequency : 300KHz  
 OVP =>  $V_o + 0.25V$   
 UVP =<  $V_{FB} - 0.16V$



The ramp time for any rail must be more than 40 us  
 $NVVDD \leq VDD (3.3V + 0.5V)$   
 $FBVDDQ \leq VDD (3.3V + 0.5V)$

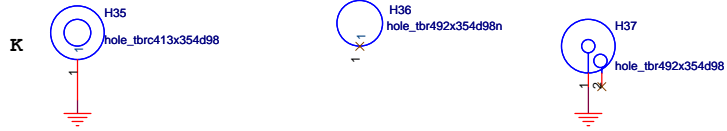
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

File	VGA Power(+1.1V/+1.2V)	
Size	Document Number	Rev
Custom	M780(MBX-194)	0.1
Date:	Tuesday, July 01, 2008	Sheet 74 of 78

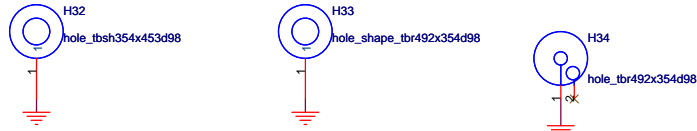
**HOLE (TOP SIDE)**

**HOLE (BOTTOM SIDE)**

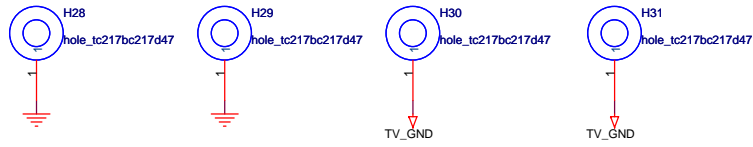
**Type 1**



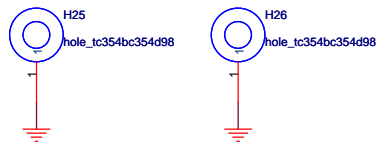
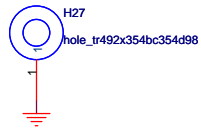
**Type 2**



**Type 3**



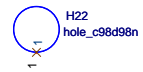
**Type 4**



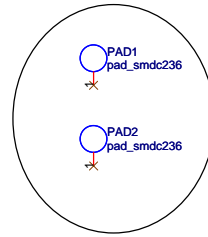
**Type 5**



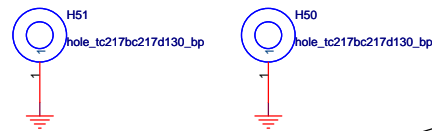
**Type 6**



DVT to PVT 0617



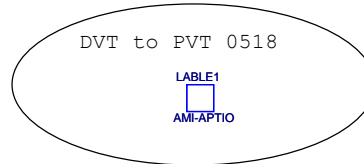
**Robason Hole**



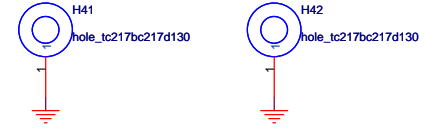
DVT to PVT



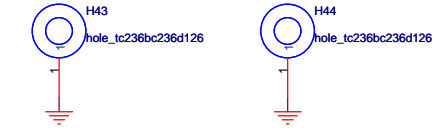
DVT to PVT 0518



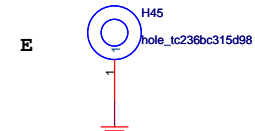
**Type 2**



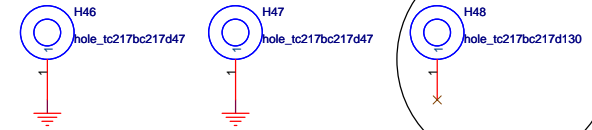
**Type 3**



**Type 4**



**Type CPU**



DVT to PVT 0611

<b>FOXCONN</b> HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title	<b>HOLE &amp; BOSS</b>	
Size	Document Number	Rev
A3	<b>M780(MBX-194)</b>	<b>0.1</b>
Date:	Wednesday, June 25, 2008	Sheet 75 of 79

M780 EVT Change History

- (Page 37) 07/08/21 As IC9N LAN\_RST# need to pull low to GND, Add 10K to GND.
(Page 41) 07/08/21 Change EC Ping3(RUN GM2) pull low value from 100K to 4.7K.
(Page 38) 07/08/29 Put to HDA bus is changed to 1.5V level, HDA\_CODEC\_RST# signal is not floating...

POWER Change History

- (Page 44) 07/09/28 Change Pq6 IR7904 to Pq146/Pq148:SI4800B/SI4894 ==>component cost down
(Page 44) 07/09/28 Change P14 from 3.30(CV) to 4.70(A05)==>component cost down
(Page 44) 07/09/28 Change Pq9 IR7904 to Pq147/Pq149:SI4800B/SI4894==>component cost down...

- (Page 20) 07/11/06 delete head 171 for ITPAN\_OVDD0.
(Page 22) 07/11/06 delete H172 for ITPAN\_OVDD0.
(Page 22) 07/11/06 add 100ohm pull to GND for ITPAN\_OVDD0.
(Page 27) 07/11/06 Change R4799,R4800,R4812,R4801 and C556 to MC.
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(Page 33) 07/11/12 Delete R2193,R2194,R2190,C1616,U1336 for Cost down evaluation.
(Page 34) 07/11/12 Change R1 from 1.50(CV) to 1.50(DELTA) ==>component cost down.
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(Page 43) 07/11/12 Change P29 FDS8880 to ST73220W.
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(Page 3) 07/10/05 Update R2087 Pull High to +3VRUN.
(Page 3) 07/10/05 Change resistor(1947) to unstuff.
(Page 64) 07/09/29 reserve PC387,ECAPC:100G(NC) near CN5 DCBOOTUP NOISE debug.
(Page 3) 07/10/08 Change CLK gen from IC59LPR8365 to IC59LPR8392.
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(Page 49) 07/11/12 Add U9 for wireless and usb power switch.
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(Page 49) 07/11/12 delete R4597.
(Page 49) 07/11/12 Add C10.
(Page 50) 07/11/12 Change U37 from TP82211PW to TP82211HP for Cost down.
(Page 50) 07/11/12 delete R622,R630,R623,R629,C664,C665.
(Page 50) 07/11/12 Update power plan.
(Page 50) 07/11/12 delete Constant-voltage +1.5VRUN Circuit.
(Page 51) 07/11/12 remove R41 power switch to Function board.
(Page 53) 07/11/12 Add C481,C482,C579 for stable voltage.
(Page 53) 07/11/12 Change Q31 from M9E2301 to CRT2301PT.
(Page 53) 07/11/12 Change D27 from populate to NC.
(Page 57) 07/11/12 delete C732 for double part.
(Page 57) 07/11/12 Change C785,C784,C705 to R5222,R5223,R5224.
(Page 47) 07/11/12 Update U1619 (Flash) for CF solution.
(Page 62) 07/11/12 Change sub\_volt for amp to YAMADA(YDA153A).
(Page 47) 07/11/12 Delete HP circuit.
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EE Change History

- (Page 41) 07/11/12 change power plane from +5VRUN to +5VRUN
(Page 51) 07/11/12 change power plane from +5VRUN to +5VALL
(Page 64) 07/11/12 change power plane from +5VRUN to +5VALL
(Page 53) 07/11/12 change power plane from +5VRUN to +5VRUN
(Page 45) 07/11/12 change Liink CONN from FOX\_UV31413-WR569-7F to FOX\_UV31413-WR039-7F.
(Page 31) 07/11/12 change CRT CONN from D211A91-WR205-4F to FOX\_D211A91-WR281-4F.
(Page 14) 07/11/12 change DNR2 CONN(CN16) from FOX\_A0A0426-WR58N-7F to FOX\_A0A0426-WR28N-7F
(Page 15) 07/11/12 change DNR2 CONN(CN2) from FOX\_A0A0426-WR49C-4F to FOX\_A0A0426-WR28N-7F
(Page 43) 07/11/12 change QID CONN(CN21) from FOX\_U122131-0001-9F to FOX\_QBSRPI20-1200-7F
(Page 34) 07/11/12 change TV CONN(CN16) from FOXCONN\_A002216-R52N-7F to FOX\_A0A0224-R60N-7F
(Page 53) 07/11/12 change PAN CONN(CN33) from FOX\_H8B104E to FOX\_H8B103E
(Page 32) 07/11/12 change PAN CONN(CN33) from FOX\_H8B2122E to FOX\_H8B112E
(Page 56) 07/11/12 delete logo LED circuit.
(Page 32) 07/11/12 add pull low resistor 100K to ground.
(Page 9) 07/11/28 Change PCIE Capacitor size from 0402 to 0201
(Page 18) 07/11/28 Change PCIE Capacitor size from 0402 to 0201
(Page 64) 07/11/28 delete CAPLOCK\_LED#,SCHLOCK\_LED#,HUNGLOCK\_LED# and remove to LED BOARD.
(Page 43) 07/11/28 Add STAT HDO Connector for ME request.
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(Page 41) 07/11/28 Add Expander I8Mbus Pull H to +5VCCVCC.
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(Page 41) 07/11/28 Remove SYSTEM\_ID for Logo LED removing.
(Page 59) 07/11/28 All plane chage to ALN.
(Page 59) 07/11/28 Change Q47,Q49 due to the BJT internal resistor and EC output level concern.
(Page 41) 07/11/28 Change R525,R526,R527 to MC.
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EVT TO DVT

Page 20 .Add power source for FB\_DLLAVDD1 & FB\_PLLAVDD1

Page 61. change R2164 from 1K to 2.7K for MOR request

Page 57. change SPK AMP Gain setting to 18dB for MOR request

Page 48,49. change BT LED control signal source from BT module directly

Page 32,41. Use SW1 one pin to disable Fan monitor function

Page 54. F11,F12,F18,F19 change from 350mA to 250mA

Page 59. Change Q4019 pin 2 from +3VALW to +5VALW

Page 37. Change EC\_OUV1 pin to GPIO12

Page 41. Add R572,R573,R574 pull low

Page 61. R259 NC

Page 41. Add C465,C466 47pF pull low

Page 24. Add R586,R590 for MOR request.

Page 3. Add R5248 in series for MCH\_CLK\_REQ#.

Page 47. Add F27 Poly switch for CF card protection.

Page 37. Add D9 diode for RUNTIME\_SCI# leakage.

Page 41. Add D17,D24 for EC\_RCIN#,EC\_A20GATE leakage.

Page 23. Add R1779 for PWR\_CNTL\_0 pull high.

Page 37. Add R455 for Finger print Detect.

Page 60,63. Remove C4830,R740,R743,R745 for MOR request.

Page 33. Add R340,Q122,R2373,Q123 for HDMI drop issue.

Page 3. Add C820 ,C821 for Robson CLK to match rising and falling time spec.

Page 52. Add F13 for CIR FFC protection.

Page 40. Add R75 ,R5249,C138 for 8057 used

Page 49. Remove C18,add R617 for MOR request.

Page 41. Add C913 for EMI.

Page 42. Add C962 for EMI.

Page 53. Add C967 for EMI.

Page 71. Add C968 for EMI.

Page 68. Add C990 for EMI.

Page 74. Add C991 for EMI.

Page 32. Add C992 for EMI.

Page 56. Add C368 for TV .

Page 60. change C4820,C4822,C4825,C4827 to 0.047U  
R5146,R5151 to 1.8k R151,R5152 t o5.6k

Page 61. change R244,R249 to 15k R2160 to 18k, PR523,PR524 to 15k, C367 to 0.022U, R2164 to 1.8k.

Page 31. Add C467,C468,C469 for EMI.

Page 46. Mount C453 for EMI.

Page 41. Add R575 for CF always power on.

Page 37. Remove R455,R486 for FP\_DET#,change by BIOS detect.

Page 6. add C88,C89 for MOR request.

Page 72. add R5250 for MOR request.

Page 34. add C370,C369 for EMI

Page 41. add C371 for EMI

Page 29. add C993 for EMI

Page 26. add C994 for EMI

Page 41. change charge LED to high active.

Page 57. add C995 for EMI.

Page 33. add C997 for EMI.

Page 62. add C90 for EMI.

Page 41. add C91 for EMI.

Page 54. add C238 for EMI.

Page 47. add U17 ,R91,R92 for CF solution.

Page 73. change PR181 from 34k to 31.6k for changing power limit from 118W to 114W

DVT to PVT

Page 64(LED Status) .charging LED logic change

Page 75(HOLE & BOSS) .Add AMI label on M/BD

Page 31(CRT) .change VSYNC and HSYNC resistor and capacitor for SI test fail.

Page 54(Daughter Board Conn) .change PWR and Suspend LED logic same as M760 for more brightness.

Page 47(PCI CF ) .separate CF controller power and card power for hot-plug issue.

Page .change NV9P,9M ,HDCP KEY HH P/N

Page 17(VGA (PCI-E) 1/9) .L4049 change vendor

Page 41(EC+KBC (WPCE775L) .change RP24,RP25 to +3VALW

Page 67(DCIN&Charger) .Delete P11 and P12

Page 68(SYS Power (+3 3V/+5V) .Delete PJ3 and PJ4

Page 69(SYS Power(+1 5V/+1 05V) .Delete PJ7 and PJ8

Page 70(DDR2 Power(+I 8V/+0 9V) .Delete PJ10 and PJ13

Page 71(CPU Vcore---ISL6266A) .Delete PJ12

Page 74(VGA Power(0.9V/+1 05V) .Delete PJ15,PJ16,PJ17

Page 43(SATA HDD/CD-ROM) .change CN126 to KOTL

Page 3(CLOCK GEN (SL28648BLC) .U123 change HH P/N

Page 18(VGA (PCI-E BUS)Strap 2/9) .add samsung VRAM strap pin

Page 55(OIDE/CAM) .change OIDE connector to LNC PVT 0605.pdf

Page 60(AUDIO(EQ) .C4820,C4822,C4825,C4827; Change from 0.047u/50V to 0.015u/25V,R5146,R5151; Change from 1.8k to 3.3k

Page 61(AVD20 (Filter Circuit) .R2164 change to 1k,R2165 change to 4.7k

Page 72(Others power plan) .R5250 mount,PR180, PR174, PR163, PQ165, PQ55, PC121, PC227 all NC

Page 51(USB 2.0) .add USB connector TID No.

Page 55(OIDE/CAM) .change camera connector for easy to unplug.

Page 43(SATA HDD/CD-ROM) .change ODD connector to 14 pin

Page 75(HOLE & BOSS) .change H48 to PTH type

Page 55(OIDE/CAM) .reserve 3.3V for camera module.

Page 47(PCI CF ) .change discharge circuit for CF card power,add 4.7U for CF card power ,change CF card LED power source.

Page 45(PCI (LINK) .change Y5 capacitor for accuracy.

Page 71(CPU Vcore---ISL6266A) .PR429 NC

Page 67(DCIN&Charger) .PCN2 add two pillars to fix position for our production line smoothly. PVT 0613.pdf

Page 1(index) .change HH P/N

Page 75(HOLE & BOSS) .add two PAD for ME request

Page 68(SYS Power (+3 3V/+5V) .PU2 Pin9 ,pin10 connect from +5VALW\_PWM to +5VALW PVT 0617.pdf

Page 41(EC+KBC (WPCE775L) .mount R516,C592 for EMI

Page 24(VGA (INTER DISPLAY ) 8/9) .mount C828 for EMI

Page 41(EC+KBC (WPCE775L) .add C998 for EMI

Page 48(blueetooth) .add C999 for EMI

Page 40(Marvell GLAN(88E8055) .add C1000 for EMI

Page 72(Others power plan) .add C1001 for EMI

Page 41(EC+KBC (WPCE775L) .add C1002 for EMI

Page 56(AUDIO(CODEC & POWER) .add C1003 for EMI

Page 54(Daughter Board Conn) .add C1004,C1005 for EMI

Page 54(Daughter Board Conn) .add L31,L32 for EMI

Page 23(VGA (XTAL/GPIO) 7/9) . reserve D10,R5251,R5252,C93,R1780 for HDMI Audio issue.

Page 56(AUDIO(CODEC & POWER) . reserve R749,C12 for HDMI Audio issue.

Page 63(Audio BOARD conn) . mount R741,change R744 to C807 0.1u for EMI

Page 56(AUDIO(CODEC & POWER) .change R5222 to C809 0.1uf for EMI.

Page 42(AUDIO(Flash ROM/SPI) .CN16 change from 1200 to 1203 for EOL issue.

Page 65(Robson 1.7 Connector) .remove CN24,C712,C713 for Robson no used.

Page 65(AUDIO (SUBWOOFER AMP) .change R5228 from 68k to 6.8k for MOR request.

Page 75(HOLE & BOSS) .Add PAD 3 for ME request.

Page 75(LVDS) .reserve C472 for invertor power PVT 0625.pdf

Page 31(CRT) .change L25,L26,L27 to 120R bead,C467,C468,C469 to NC.

Page 62(AUDIO (SUBWOOFER AMP) .change R5226,R5227 to 0.5% resistors

Page 54(Daughter Board Conn) .add U11 for finger print protection. PVT 0627.pdf

Page 71(CPU Vcore---ISL6266A) .PC389 NC,PC299,PC289 mount for solid cap issue.

Page 68(SYS Power (+3 3V/+5V) .PC387 NC for solid cap issue

Page 74(VGA Power(0.3V/+1 05V) .PC391 NC,PC353 mount for solid cap issue.

Page 32(LVDS) .Add C472 for solid cap issue.

Page 45(PCI (LINK) .change R540-R543 to 47 ohm for MS overshoot and undershoot issue.

Page 41(EC+KBC (WPCE775L) .R516,C592 NC for signal quality.

Page 3(CLOCK GEN (SL28648BLC) .change R767 to 47 ohm for EMI issue. PVT 0629.pdf

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