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07	ARD (GRAPHICS POWER)	SA		49	Audio/USB DB Conn.	SA
08	ARD (GND)	SA		50	Switch (Botton & KB LED)	SA
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11	PCH (PCI-E,SMBUS,CLK)	SA		53	Audio (Power)	SA
12	PCH (DMI,FDI,GPIO)	SA		54	Audio (Audio & USB Conn.)	SA
13	PCH (LVDS,DDI)	SA		55	Audio (Head Phone Jack)	SA
14	PCH (PCI,USB,NVRAM)	SA		56	Audio (Ext MIC Jack)	SA
15	PCH (GPIO,VSS_NCTF,RSVD)	SA		57	Audio (USB Port)	SA
16	PCH (POWER) 1/2	SA		58	Power Design Diagram	SA
17	PCH (POWER) 2/2	SA		59	DCIN&Charger	SA
18	PCH (VSS)	SA		60	Discharge Circuit	SA
19	CLOCK GEN	SA		61	Identify IC	SA
20	DDRIII(SO-DIMM 0) 1/3	SA		62	SYS Power (+3_3V/+5V)	SA
21	DDRIII(SO-DIMM 1) 2/3	SA		63	VTT&PCH Power(1_05V)	SA
22	CRT	SA		64	DDR3 Power(+1_5V/+0_75V)	SA
23	LVDS	SA		65	SYS Power(+1_8V)	SA
24	Inverter CONNECTOR	SA		66	CPU Power VHCORE	SA
25	LVDS CONNECTOR	SA		67	CPU Power VID	SA
26	HDMI	SA		68	VGFX Power GFXCORE	SA
27	EC+KBC (NPCE783L)	SA		69	Others power plane	SA
28	KB Connector	SA		70	OVP protection	SA
29	SPI Flash ROM	SA		71	HOLE & AMI LABEL	SA
30	Debug Port	SA		72	History(1)	SA
31	Express Card	SA		73	History(2)	SA
32	Mini-PCIE Card (WLAN)	SA		74	History(3)	SA
33	LAN (88E8059) 1/2	SA		75	History(4)	SA
34	LAN (Transformer) 2/2	SA		76	History(5)	SA
35	SATA HDD	SA		77	History(6)	SA
36	SATA CD-ROM	SA		78	History(7)	SA
37	eSATA COMBO CONN.	SA		79	History(8)	SA
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39	PCIE (SD) 2/2	SA		81		
40	Camera Connector	SA		82		
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Project Code & Schematics Subject: **M960&M970 L Model**

PCB P/N:
1P-0099J00-60SB (IRIS MB)
1P-1099J00-60SB (IRIS AUDIO)
1P-1099J01-60SB (IRIS PWR)
1P-0099500-60SB (HANNSTAR MB)
1P-1099500-60SB (HANNSTAR Audio)
1P-1099501-60SB (HANNSTAR PWR)

P. Leader	Check by	Design by

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Title: ***Index Page***

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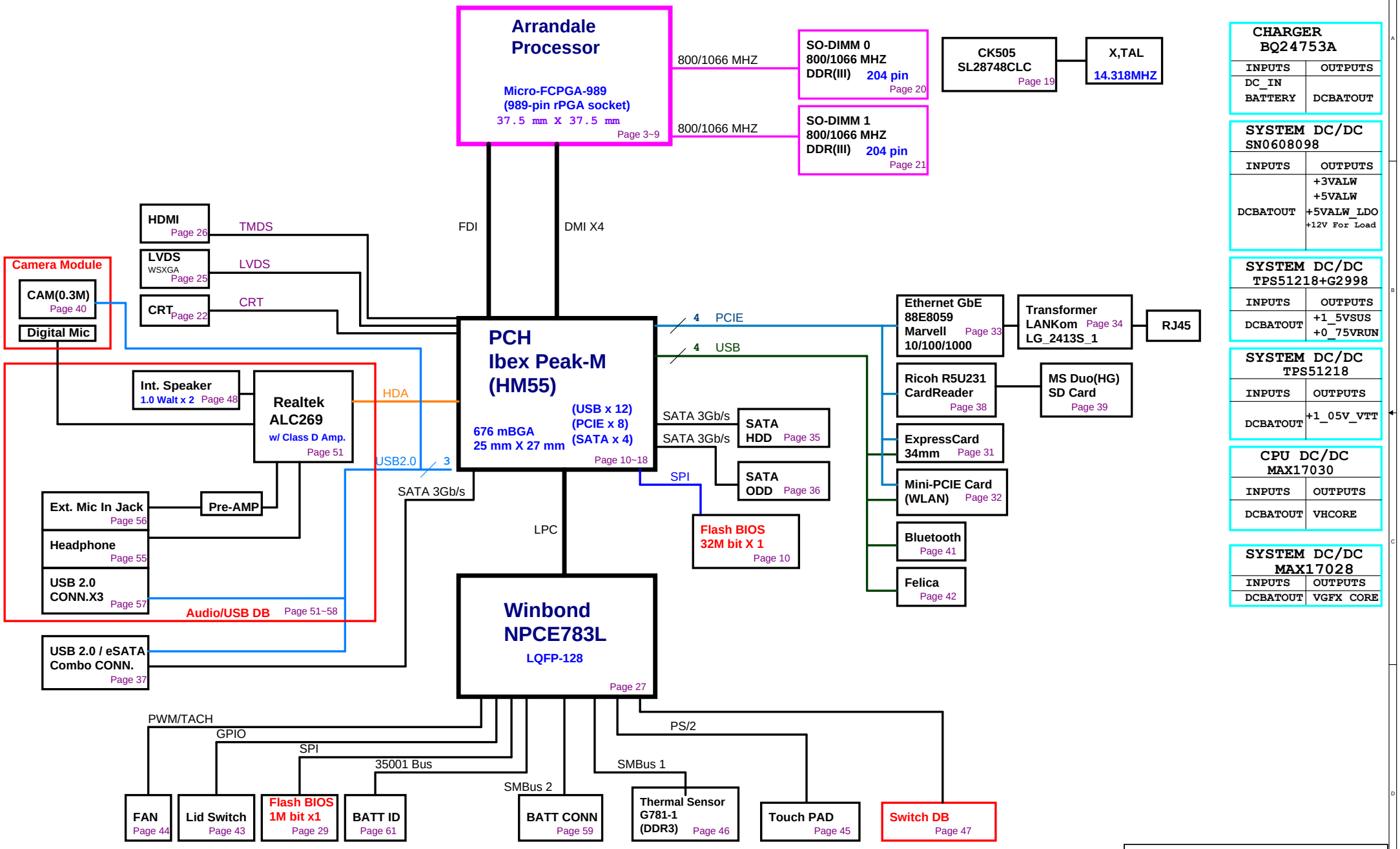
M960&M970 L Model Calpella Platform UMA Graphic



CHARGER BQ24753A	
INPUTS	OUTPUTS
DC_IN BATTERY	DCBATOUT

SYSTEM DC/DC SN0608098	
INPUTS	OUTPUTS
DCBATOUT	+3VALW +5VALW +5VALW_LDO +12V For Load

SYSTEM DC/DC TPS51218+G2998	
INPUTS	OUTPUTS
DCBATOUT	+1_5VSUS +0_75VRUN

SYSTEM DC/DC TPS51218	
INPUTS	OUTPUTS
DCBATOUT	+1_05V_VTT

CPU DC/DC MAX17030	
INPUTS	OUTPUTS
DCBATOUT	VHCORE

SYSTEM DC/DC MAX17028	
INPUTS	OUTPUTS
DCBATOUT	VGFX CORE

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Title: Block Diagram

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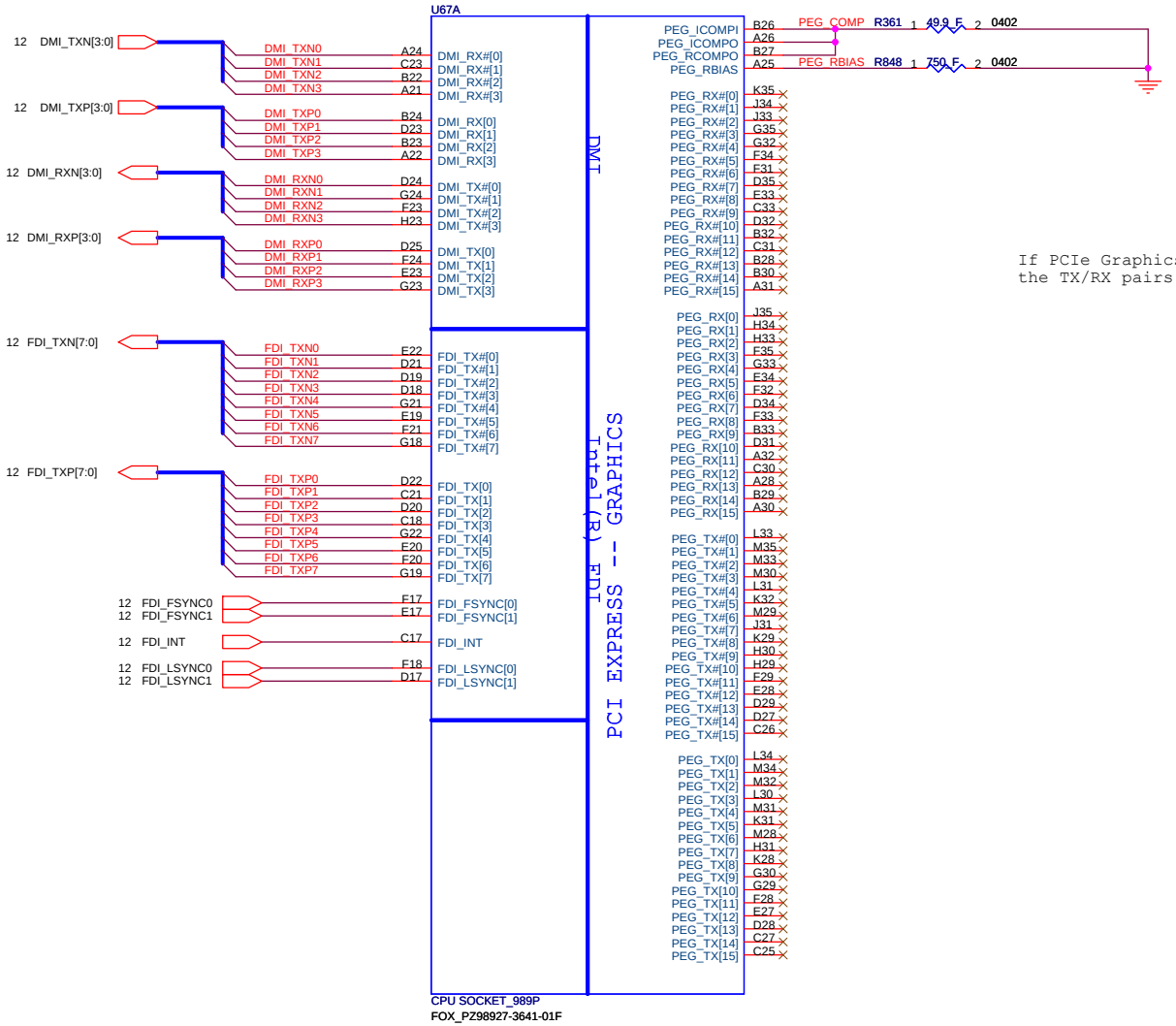

If PCIe Graphics is not implemented,
the TX/RX pairs can be left as No Connect.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD (DMI,PEG,FDI)	
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Layout Note:
Comp0,1 connect with Zo=49.9 ohm,
Comp2,3 connect with Zo=20 ohm,
In order to minimize resistance,
use thick traces to route all
COMP signals, use 10-mils
(0.254-mm) wide trace for
routing less than 500 mils (12.7
mm), or 20-mils (0.508-mm)
wide trace for routing between
500 mils (12.7 mm) and
1000 mils (25.4 mm). Keep 20-mils
(0.508-mm) spacing to
any other signals in order to
minimize crosstalk.

U67B

MISC THERMAL
CLOCKS
DDR3 MISC
JTAG & BPM
PWR MANAGEMENT

R849 1 20_F 2 0402 COMP3 AT23 COMP3
R850 1 20_F 2 0402 COMP2 AT24 COMP2
R851 1 49.9_F 2 0402 COMP1 G16 COMP1
R852 1 49.9_F 2 0402 COMP0 AT26 COMP0
20MIL TP60 1 SKTOCC# AH24 SKTOCC#
H_CATERR# AK14 CATERR#
15 H_PECI H_PECI AT15 PECI
DVT
66 PROCHOT# PROCHOT# AN26 PROCHOT#
15,27 PM_THRMTRIP# R939 1 0_J 2 0402 PM_THRMTRIP#_1 AK15 THERMTRIP#
MP
H_CPURST#_R AP26 RESET_OBS#
12 H_PM_SYNC H_PM_SYNC AL15 PM_SYNC
H_CPUPWRGD AN14 VCCPWRGOOD_1
15 H_CPUPWRGD H_CPUPWRGD AN27 VCCPWRGOOD_0
12 PM_DRAM_PWRGD PM_DRAM_PWRGD AK13 SM_DRAMPWROK
VTTPWRGOOD AM15 VTTPWRGOOD
20MIL TP94 1 TAPPWRGOOD AM26 TAPPWRGOOD
14,27,30,31 BUF_PLT_RST# 1 R925 2 BUF_PLT_RST#_R AL14 RSTIN#
1.5K_F 0402
R926 750_F 0402

CPU SOCKET_989P
FOX_PZ98927-3641-01F

BCLK A16 ARD_BCLK
BCLK# B16 ARD_BCLK#
R1450 1 0_J 2 0402
R1451 1 NC_0_J 2 0402
R1452 1 NC_0_J 2 0402
R1453 1 0_J 2 0402
CLK_PCH_CPU_CLK 15
CLK_CPU_BCLK 19
CLK_CPU_BCLK# 19
CLK_PCH_CPU_CLK# 15
EVT
BCLK_ITP AR30 BCLK_ITP 1 TP61 20MIL
BCLK_ITP# AT30 BCLK_ITP# 1 TP63 20MIL
PEG_CLK E16
PEG_CLK# D16
CLK_EXP_P 11
CLK_EXP_N 11
DPLL_REF_SSCLK A18
DPLL_REF_SSCLK# A17
CLK_DP_P 11
CLK_DP_N 11

SM_DRAMRST# F6 DDR3_DRAMRST#_Q
SM_RCOMP[0] AL1 SM_RCOMP0 R854 1 100_F 2 0402
SM_RCOMP[1] AM1 SM_RCOMP1 R853 1 24.9_F 2 0402
SM_RCOMP[2] AN1 SM_RCOMP2 R855 1 130_F 2 0402
PM_EXT_TS#[0] AN15 PM_EXTTS#0
PM_EXT_TS#[1] AP15 PM_EXTTS#1
+1_05V_VTT
R932 10K_J 0402
R933 10K_J 0402
PM_EXTTS#0 20
PM_EXTTS#1 20,21
R962 1 0_J 2 0402 DDR_ALERT# 46
R1231 NC_12.4K_F 0402

PRDY# AT28 XDP_PRDY# 1 TP75 20MIL
PREQ# AP27 XDP_PREQ#
TCK AN28 XDP_TCLK
TMS AP28 XDP_TMS
TRST# AT27 XDP_TRST#
+3VRUN
R1292 NC_51_J 0402
TDI AT29 XDP_TDI_R
TDO AR27 XDP_TDO_R
TDI_M AR29 XDP_TDI_M
TDO_M AP29 XDP_TDO_M
DBR# AN25 XDP_DBRESET#
BPM#[0] AJ22 BPM#0 1 TP64 20MIL
BPM#[1] AK22 BPM#1 1 TP65 20MIL
BPM#[2] AK24 BPM#2 1 TP66 20MIL
BPM#[3] AJ24 BPM#3 1 TP67 20MIL
BPM#[4] AJ25 BPM#4 1 TP68 20MIL
BPM#[5] AH22 BPM#5 1 TP69 20MIL
BPM#[6] AK23 BPM#6 1 TP70 20MIL
BPM#[7] AH23 BPM#7 1 TP71 20MIL
+1_05V_VTT
XDP_TDO_R R1290 1 51_J 2 0402
XDP_TMS R1258 1 NC_51_J 2 0402
XDP_TDI_R R1259 1 NC_51_J 2 0402
XDP_PREQ# R1260 1 NC_51_J 2 0402
XDP_TCLK R1261 1 NC_51_J 2 0402
XDP_TRST# R1262 2 51_J 1 0402
XDP_TDO_M
R969 0_J 0402
XDP_TDI_M

JTAG Mapping -Scan Chain (Default)

+1_05V_VTT
R258 68_J 0402
PROCHOT#
Q14A
+3VRUN
R262 4.7K_J 0402
A0205
Q14B
2N7002DW null
27 OVT_EC# 2

For Intel S3 Power Reduction issue
R5948 1 NC_0_J 2 0402
Q72 2N7002W null
+1_5VSUS
0402 1K_J R5923
DDR3_DRAMRST# Q
DDR3_DRAMRST#
DDR3_DRAMRST# 20,21
R5949 100K_J 0402
C6326 0.047U_16V_K 0402_X7R
DVT
15 RST_GATE
DVT

For Intel S3 Power Reduction issue
+1_5VRUN
+3VALW
R5950 NC_1.1K_F 0402
C6327 0.1U_6.3V_K 0402_X5R
U217
R5951 10K_J 0402
PM_DRAM_PWRGD
R5924 1 4 0402 1.5K_F
74AHC1G08GW
0402 750_F R5925
RUN_PWRGD 12,27,63,64
DVT

+3VRUN
R14 10K_J 0402
C13 0.1U_6.3V_K 0402_X5R
U2
12,27,63,64 RUN_PWRGD
RUN_PWRGD
4VTTPW_R R1572 1 2K_F 2 0402 VTTPWRGOOD
74AHC1G08GW
R970 1 NC_0_J 2 0402
R1573 1K_F 0402

+1_05V_VTT
R861 49.9_F 0402
R936 NC_68_J 0402
H_CATERR#
H_CPURST#_R

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Title	ARD (CLK,MISC,JTAG)	
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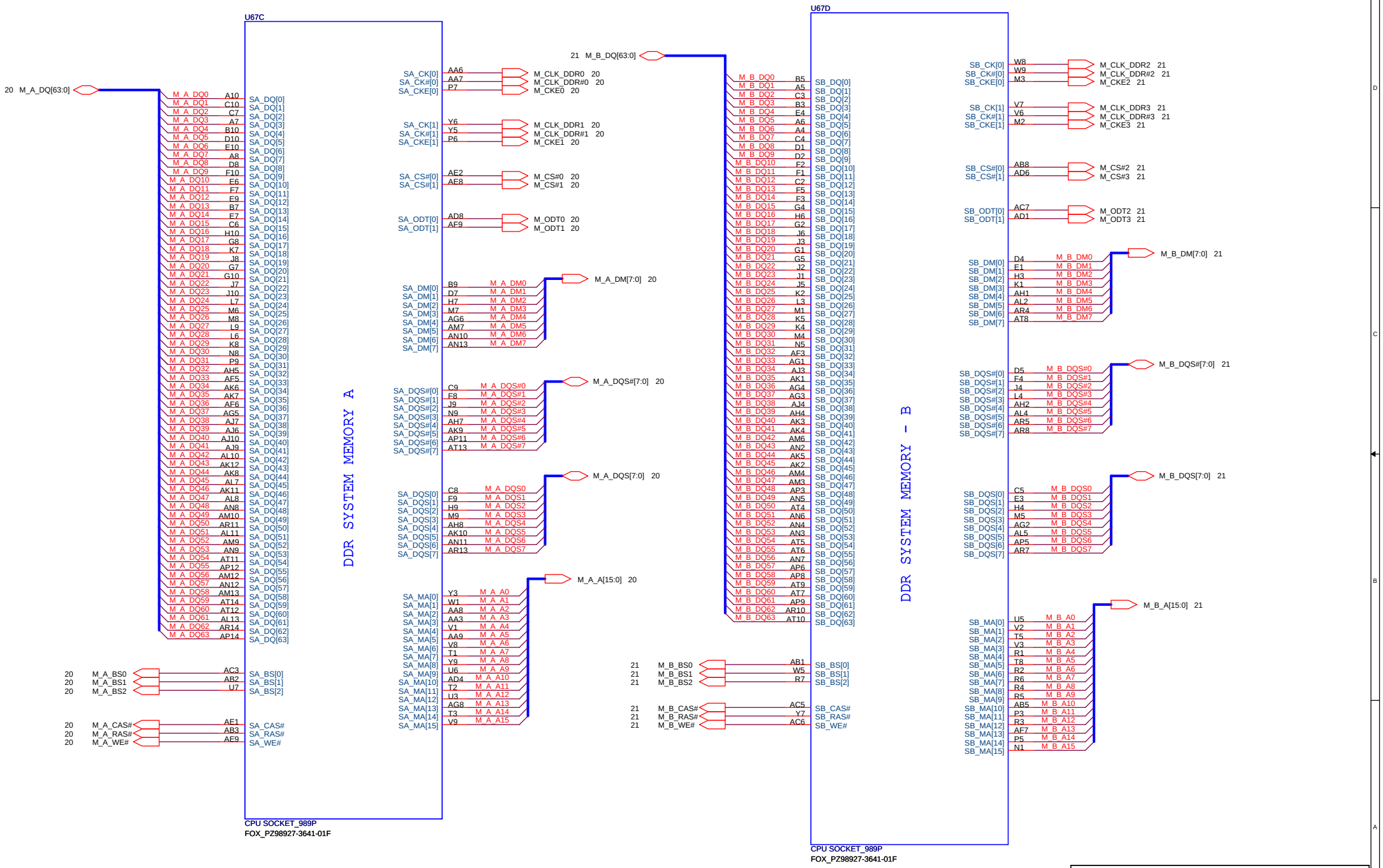

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	ARD (DDR3)		
Size A3	Document Number M960&M970 L Model		Rev SA
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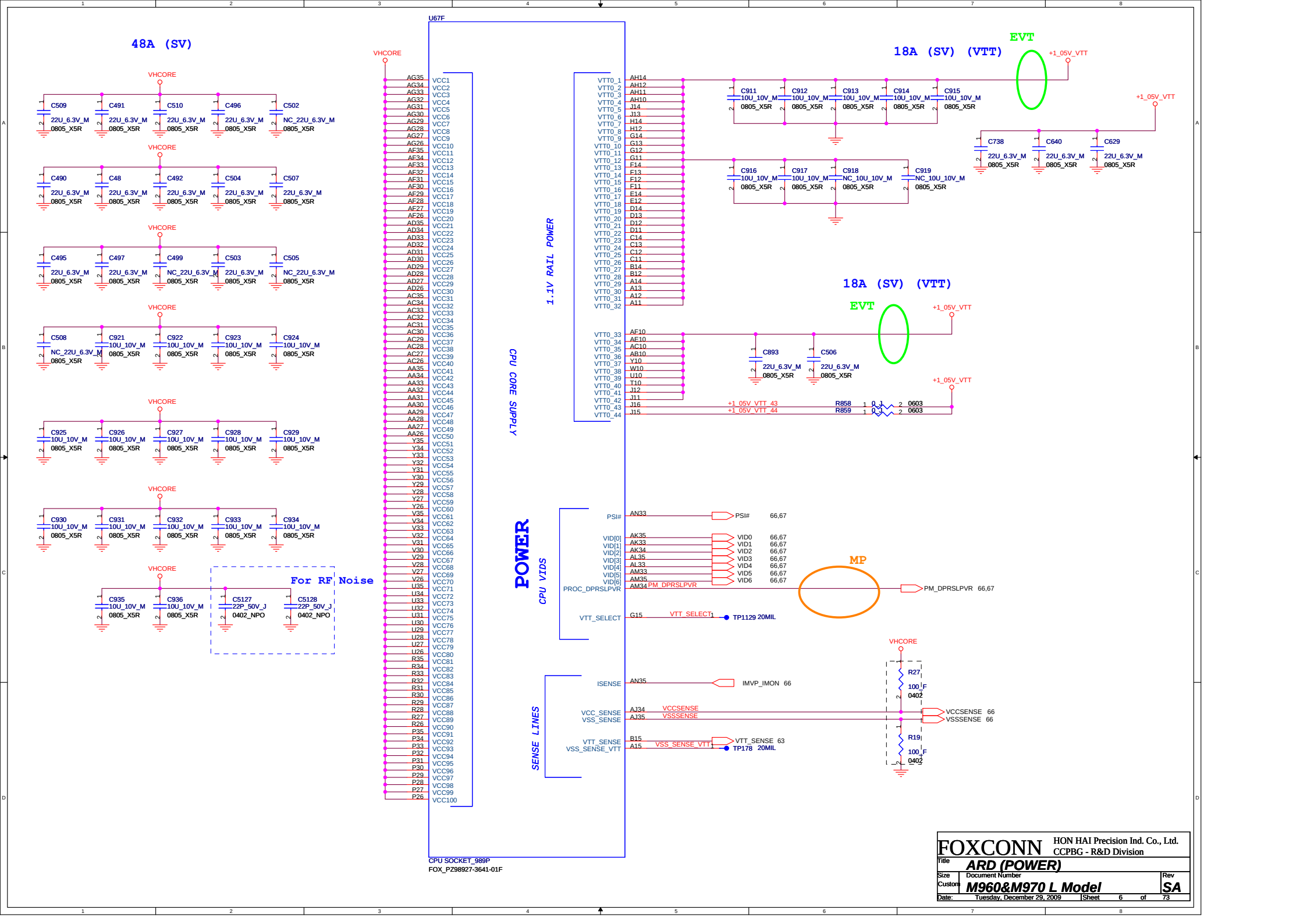
48A (SV)
VHCORE
C509 C491 C510 C496 C502
22U_6.3V_M 0805_X5R
NC_22U_6.3V_M 0805_X5R
C490 C48 C492 C504 C507
22U_6.3V_M 0805_X5R
C495 C497 C499 C503 C505
NC_22U_6.3V_M 0805_X5R
C508 C921 C922 C923 C924
10U_10V_M 0805_X5R
C925 C926 C927 C928 C929
C930 C931 C932 C933 C934
C935 C936 C5127 C5128
22P_50V_J 0402_NPO
For RF Noise
U67F
CPU SOCKET_989P
FOX_PZ98927-3641-01F
1.1V RAIL POWER
CPU CORE SUPPLY
POWER
CPU VIDS
SENSE LINES
18A (SV) (VTT)
EVT
+1_05V_VTT
C911 C912 C913 C914 C915
C916 C917 C918 C919
NC_10U_10V_M
C738 C640 C629
C893 C506
R858 R859 0603
+1_05V_VTT_43
+1_05V_VTT_44
PSI# AN33 PSI# 66,67
VID[0] AK35 VID0 66,67
VID[1] AK33 VID1 66,67
VID[2] AK34 VID2 66,67
VID[3] AL35 VID3 66,67
VID[4] AL33 VID4 66,67
VID[5] AM33 VID5 66,67
VID[6] AM35 VID6 66,67
PROC_DPRSLPVR AM34 PM_DPRSLPVR PM_DPRSLPVR 66,67
MP
VTT_SELECT G15 VTT_SELECT TP1129 20MIL
ISENSE AN35 IMVP_IMON 66
VCC_SENSE AJ34 VCCSENSE VCCSENSE 66
VSS_SENSE AJ35 VSSSENSE VSSSENSE 66
VTT_SENSE B15 VTT_SENSE 63
VSS_SENSE_VTT A15 VSS_SENSE_VTT TP178 20MIL
R27 R19 100_F 0402
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title ARD (POWER)
Size Custom
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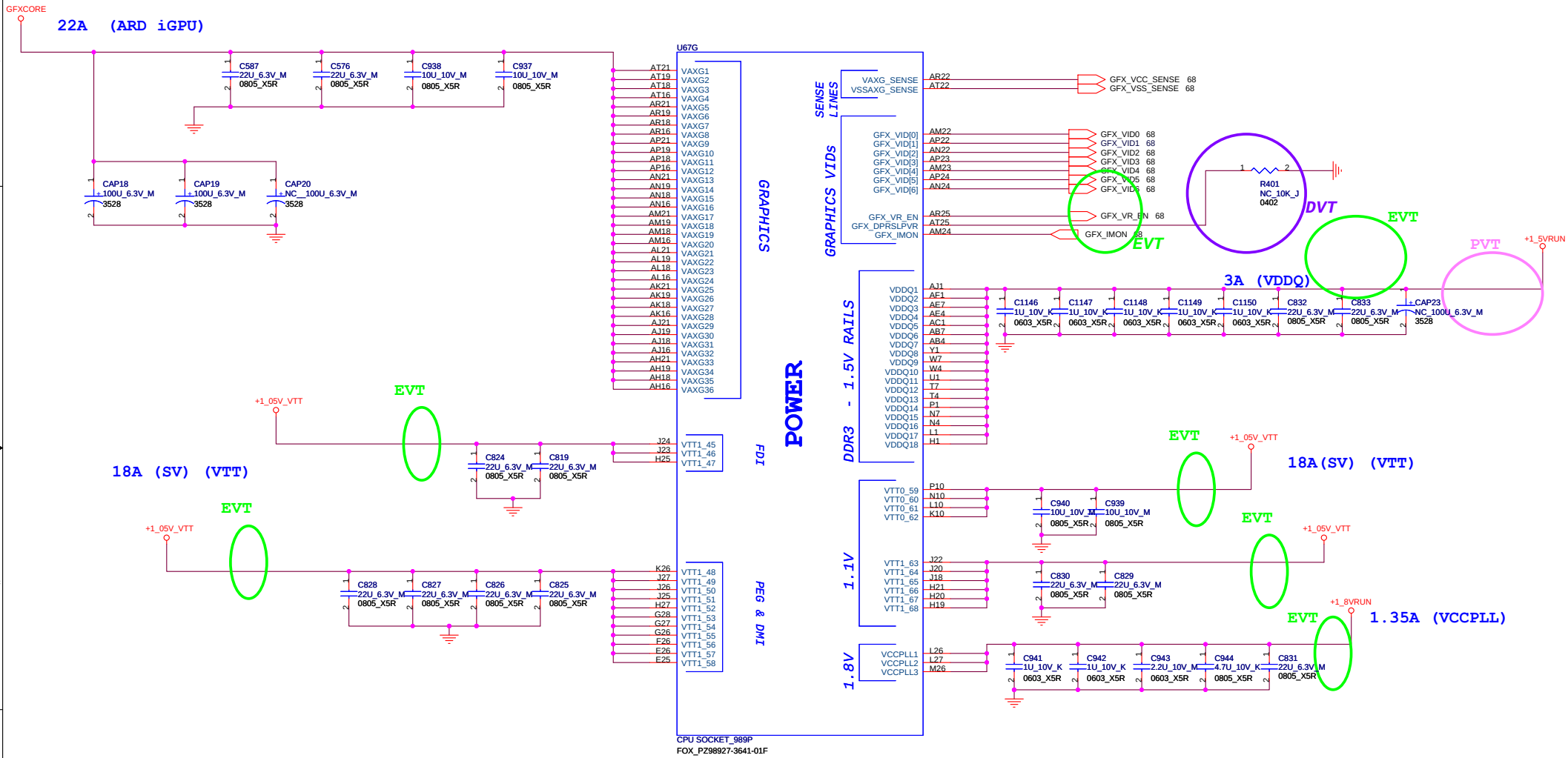

FOXCONN HON HAI Precision Ind. Co., Ltd.
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Title: ARD (GRAPHICS POWER)

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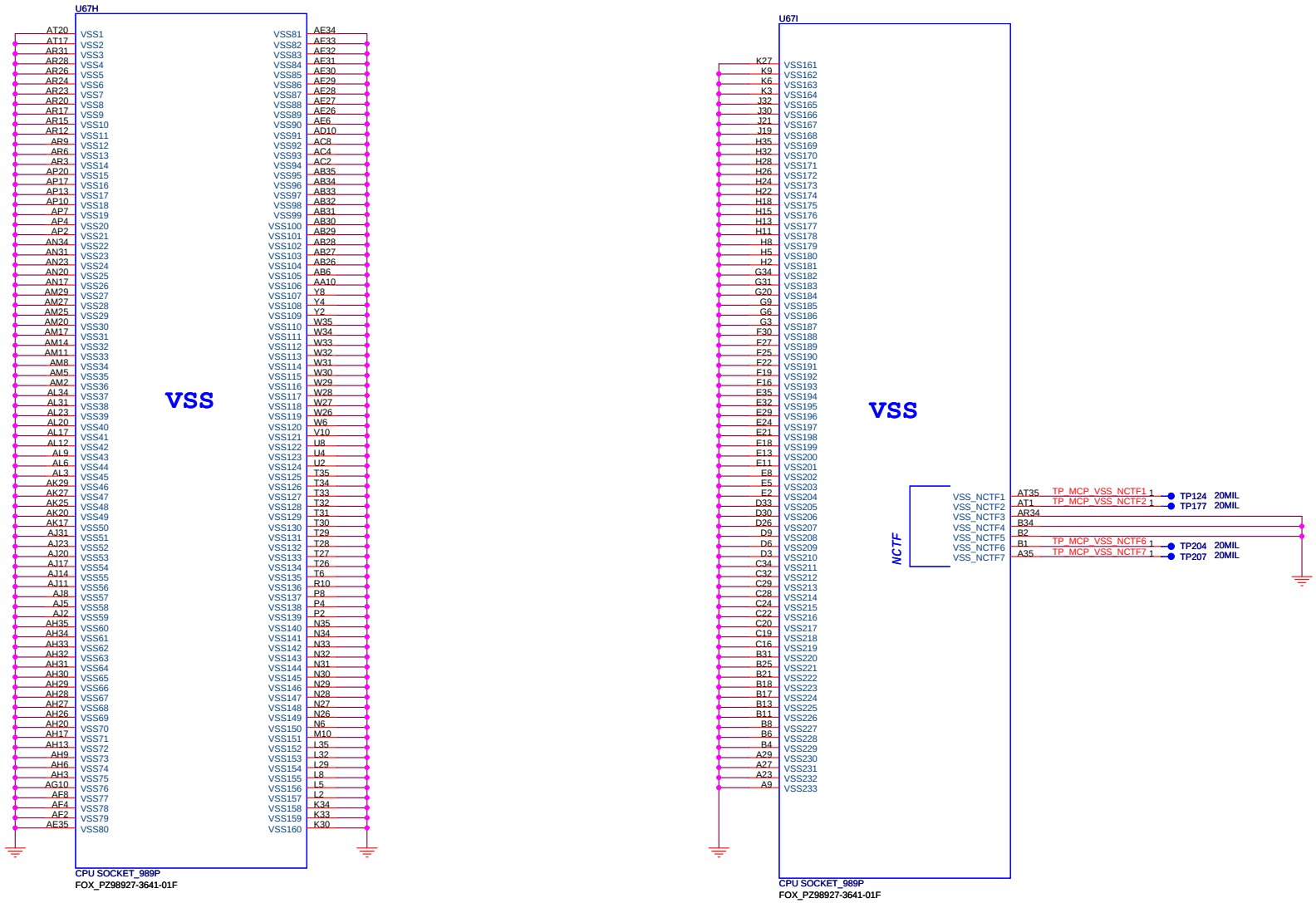

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: ARD (GND)		
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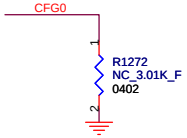
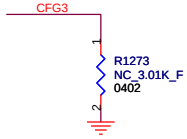
PCI Express Configuration Select
CFG0 1 : Single PEG
0 : Bifurcation enable

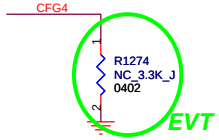
3393727 The VIL Voltage DC Specification for CFG[0] Pin is in Violation of the EDS Value by a Large Amount
The Clarksfield EDS Vol1 documents the CFG[1:0] pins for PCI Express Port Bifurcation, the straps may not work correctly when using a pull down resistor of value other than 250 Ohms to drive a value of zero on the CFG[0] pin. When left floating a value of one is sensed and there is no impact in this case.

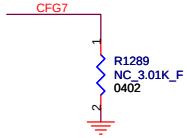


CFG3 PCI Express Static Lane Reversal
CFG3 1 : Normal Operation
0 : Lane Numbers Reversed
15 ->0 , 14-> 1 , ...



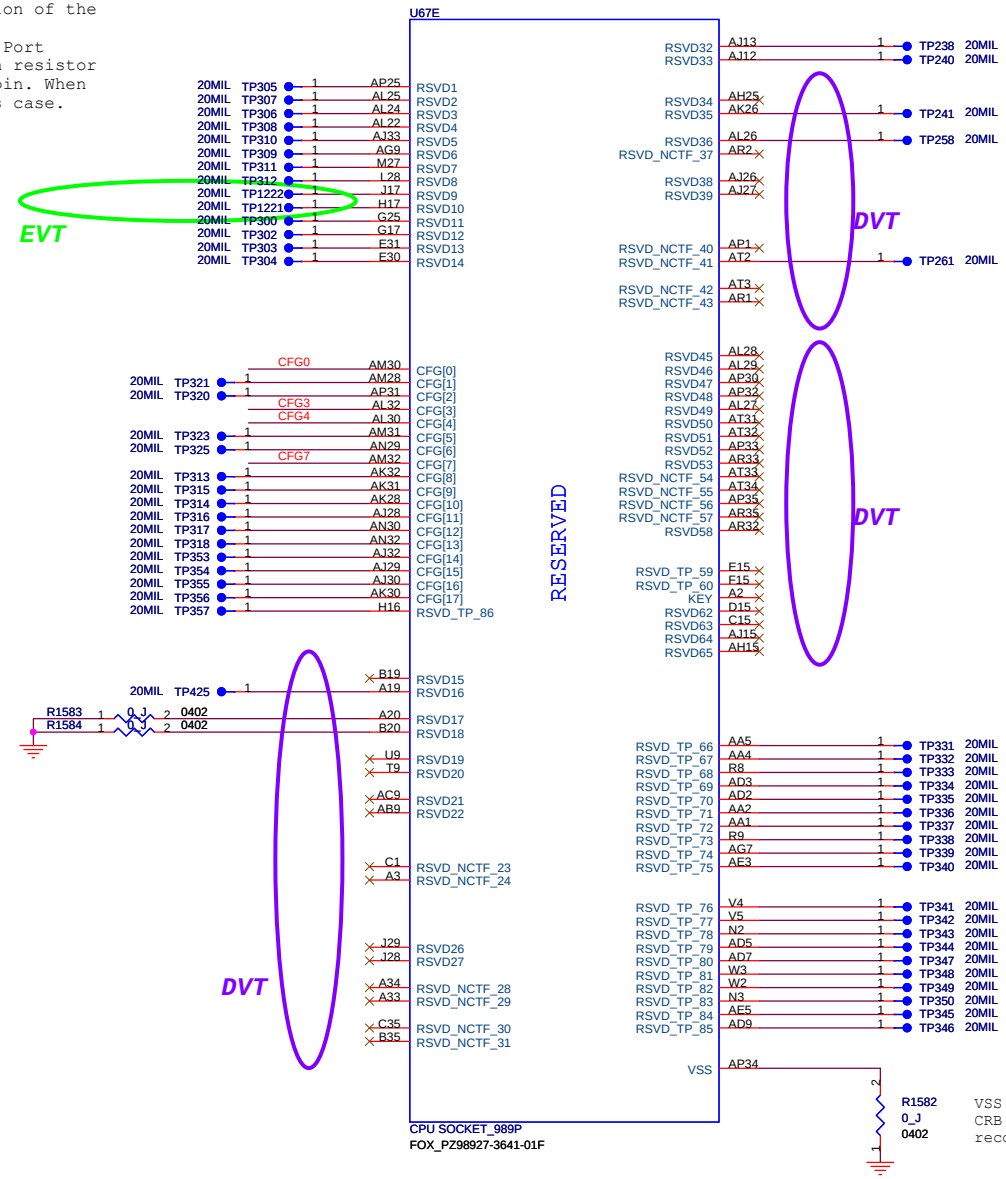
CFG4 Display Port Presence
CFG4 1 : Disabled ; No Physical Display Port attached to Embedded Display Port
0 : Enable ; An external Display Port device is connected to the Embedded Display Port





2611030 PCI Express Interface May Not Meet PCI Express 2.0 Jitter Specifications

Intel has determined that the workaround (3.01K pull down to Vss on signal CFG[7]) is not robust. Intel recommends not implementing this workaround at this time (CFG[7] should not be pulled down).
Intel recommends not to test for PCI-E Express 2.0 Jitter specification compliance for the affected steppings.



VSS (AP34) can be left NC is CRB implementation; EDS/DG recommendation to GND

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	ARD (RESERVED)	
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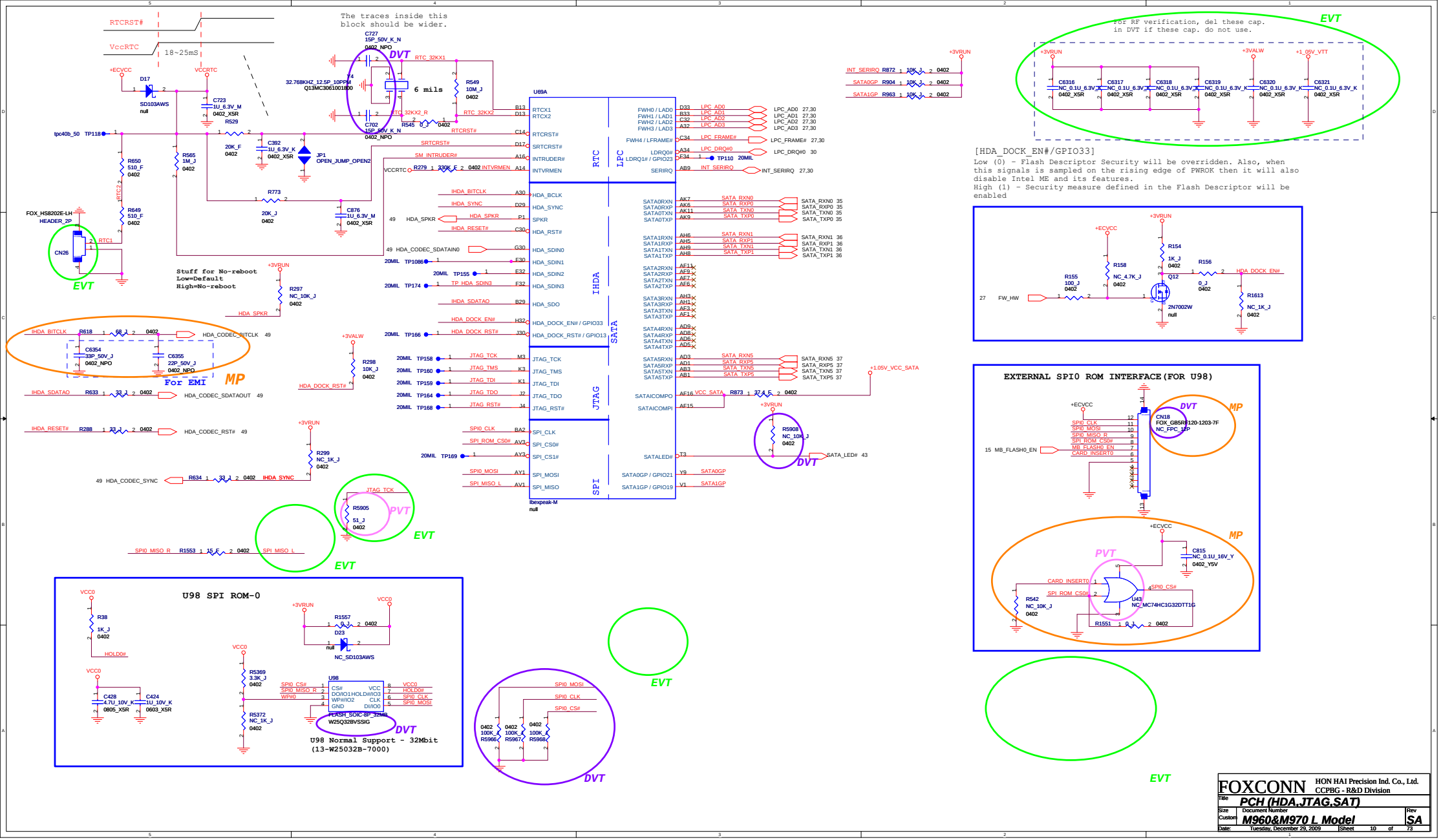

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	PCH (HDA,JTAG,SAT)		
Size: Custom	Document Number: M960&M970 L Model		Rev: SA
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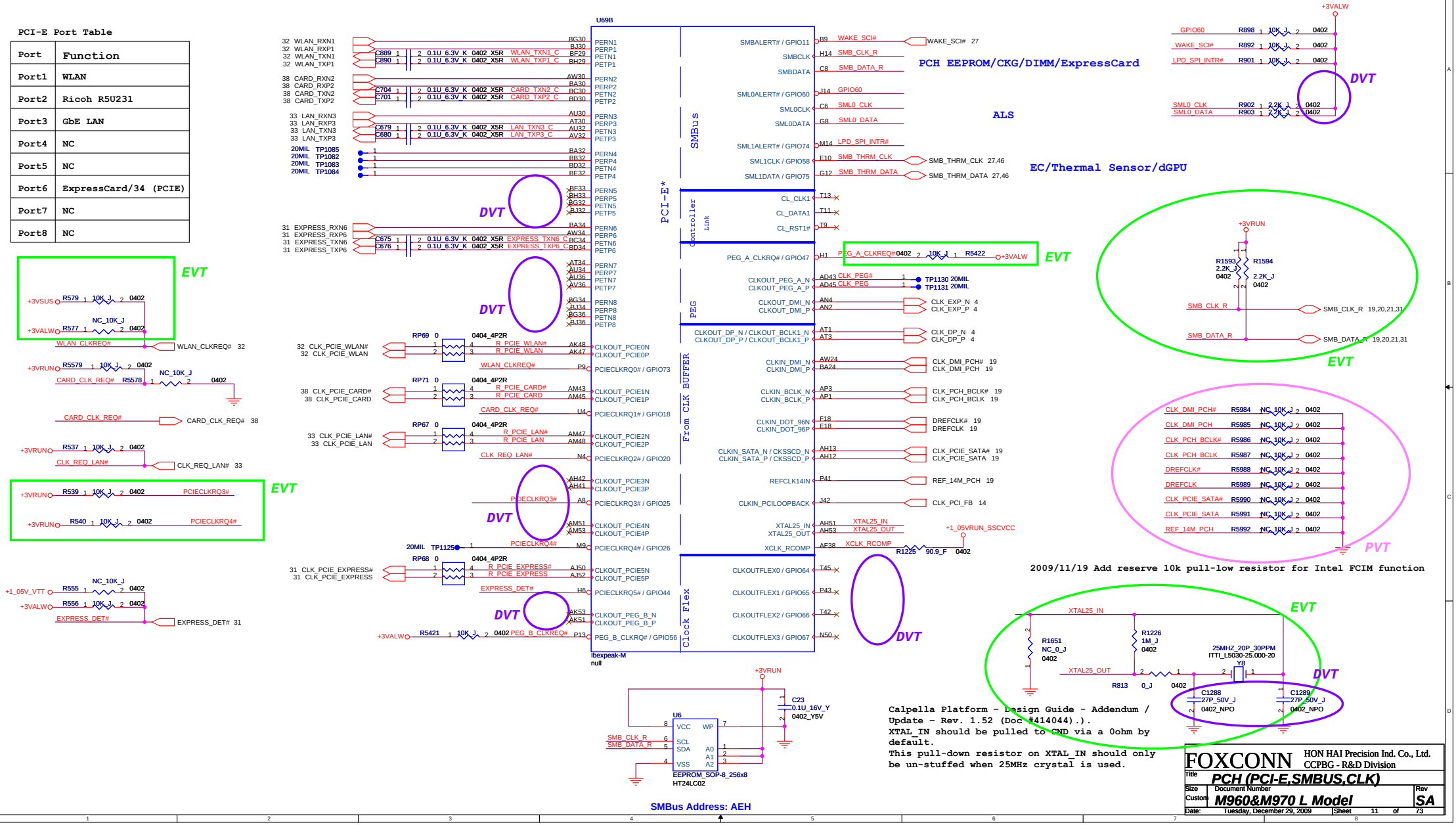
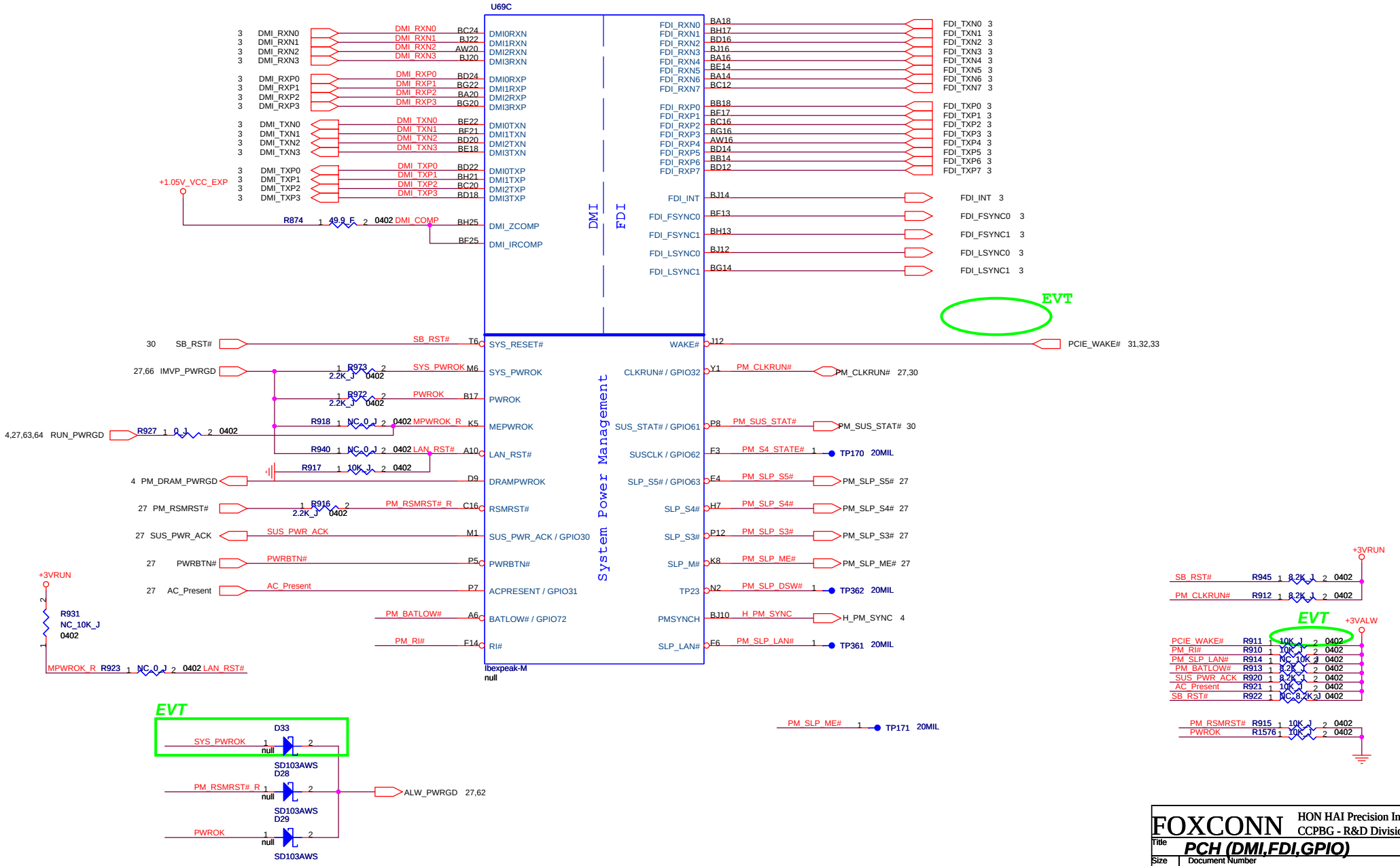
PCI-E Port Table

Port	Function
Port1	WLAN
Port2	Ricoh R5U231
Port3	GbE LAN
Port4	NC
Port5	NC
Port6	ExpressCard/34 (PCIE)
Port7	NC
Port8	NC



For Disable Arrandale Graphic
In addition, FDI_RXN_[7:0] and FDI_RXP_[7:0] can be left floating on the PCH.
FDI_TX[7:0] and FDI_TX#[7:0] can be left floating on the Arrandale. The
GFX_IMON,FDI_FSYNC[0], FDI_FSYNC[1], FDI_LSYNC[0], FDI_LSYNC[1], and FDI_INT
signals on the Arrandale side should be tied to GND (through 1-kΩ ±5% resistors).



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (DMI,FDI,GPIO)	
Size A3	Document Number M960&M970 L Model	Rev SA
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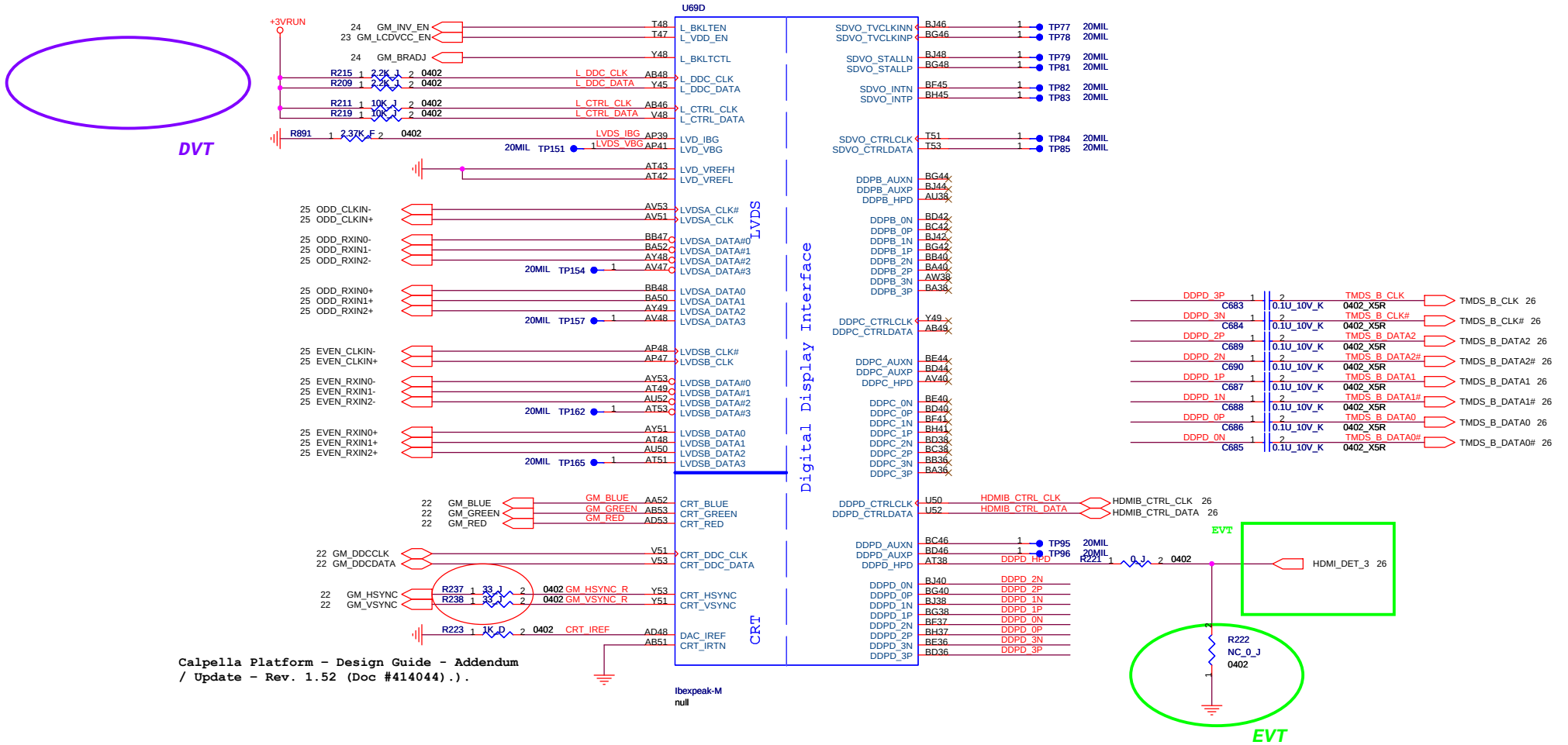
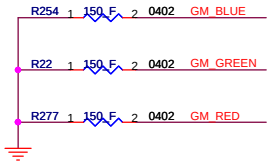


Calpella Platform – Design Guide – Addendum / Update – Rev. 1.52 (Doc #414044).).



Place resistor close to PCH (U69).

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Title	PCH (LVDS,DDI)	
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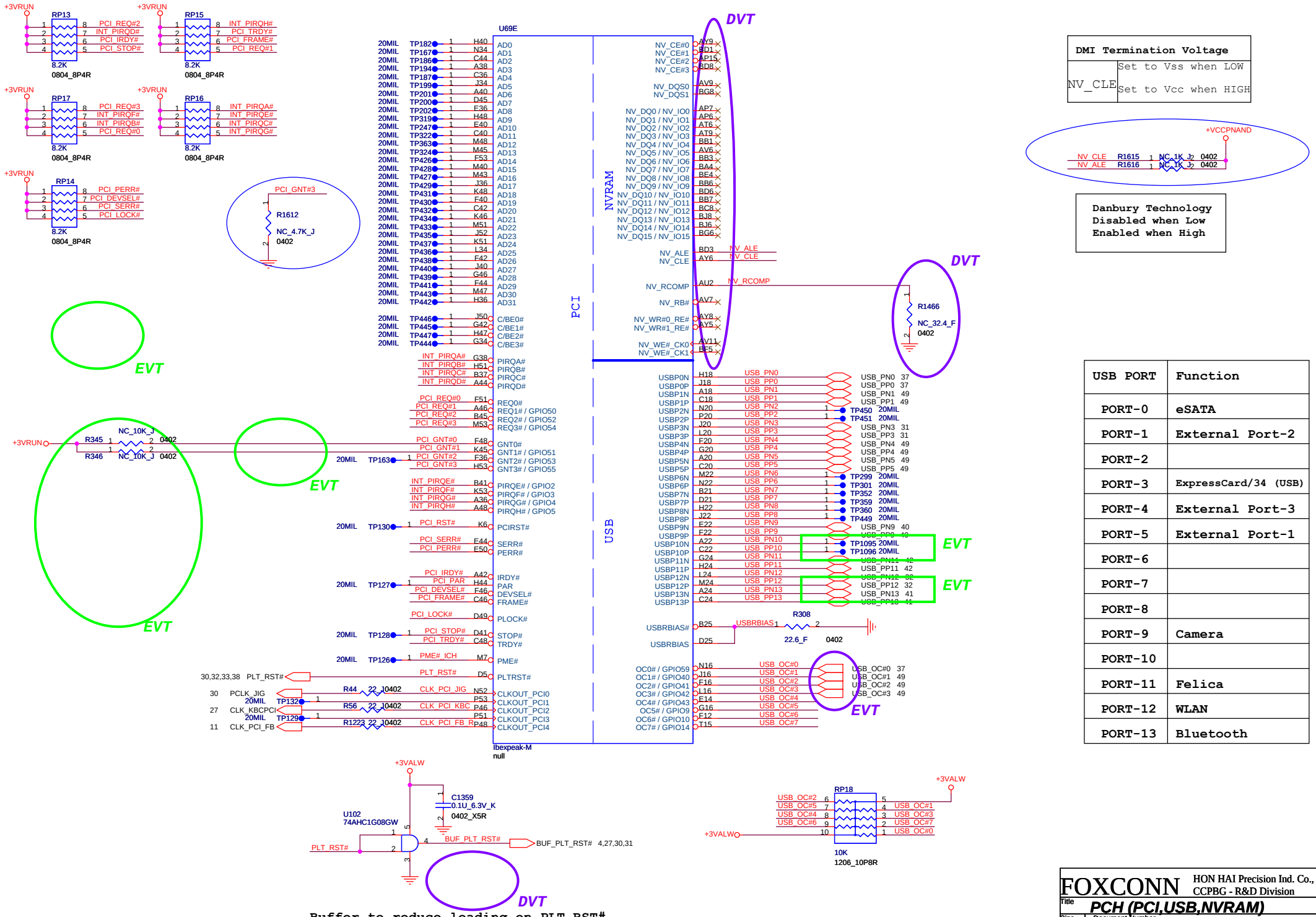

USB PORT	Function
PORT-0	eSATA
PORT-1	External Port-2
PORT-2	
PORT-3	ExpressCard/34 (USB)
PORT-4	External Port-3
PORT-5	External Port-1
PORT-6	
PORT-7	
PORT-8	
PORT-9	Camera
PORT-10	
PORT-11	Felica
PORT-12	WLAN
PORT-13	Bluetooth

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CCPBG - R&D Division

Title: PCH (PCI,USB,NVRAM)
Size: A3 | Document Number: M960&M970 L Model | Rev: SA
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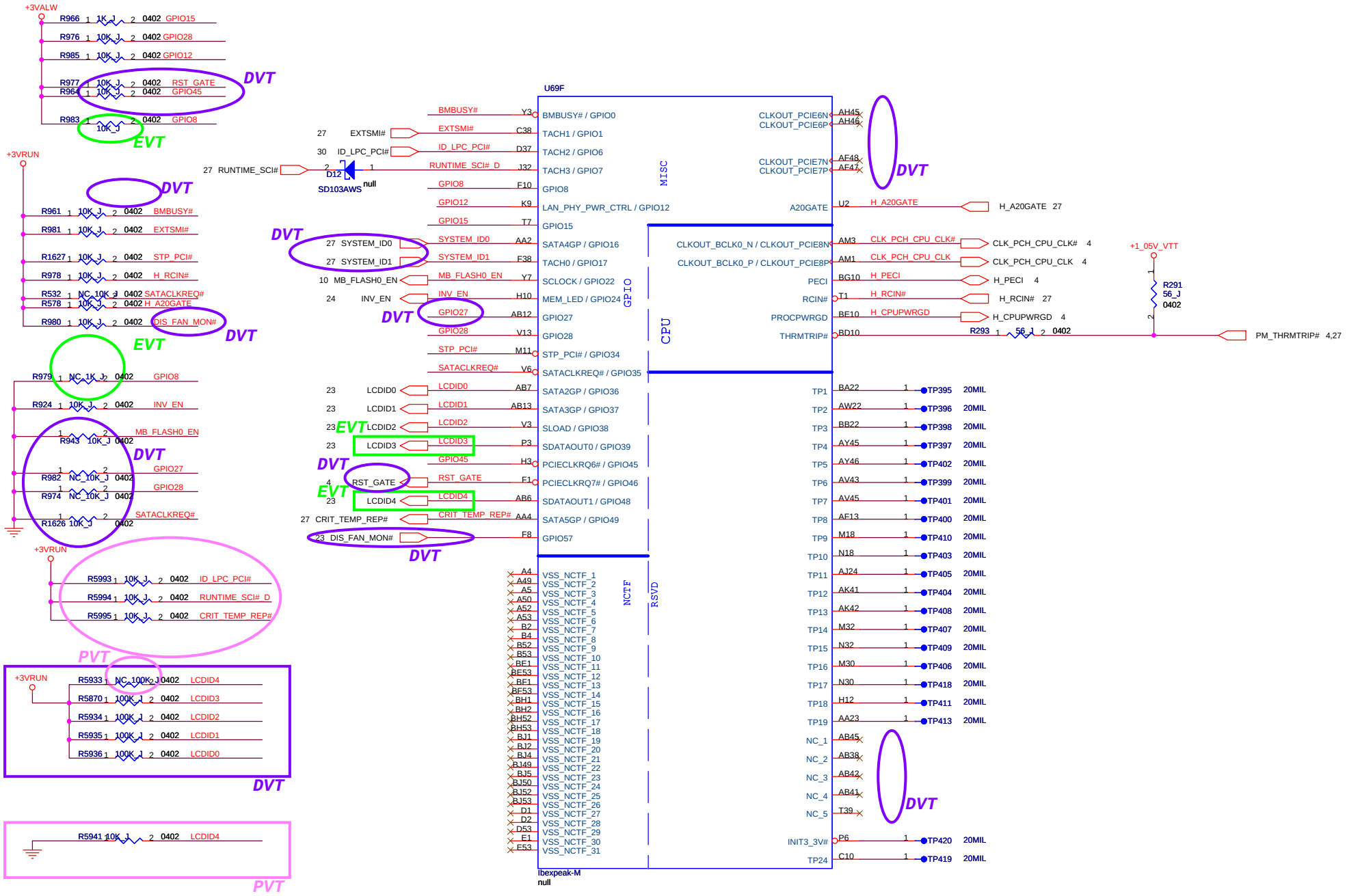


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (GPIO,VSS_NCTF,RSVD)	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 15 of 73	

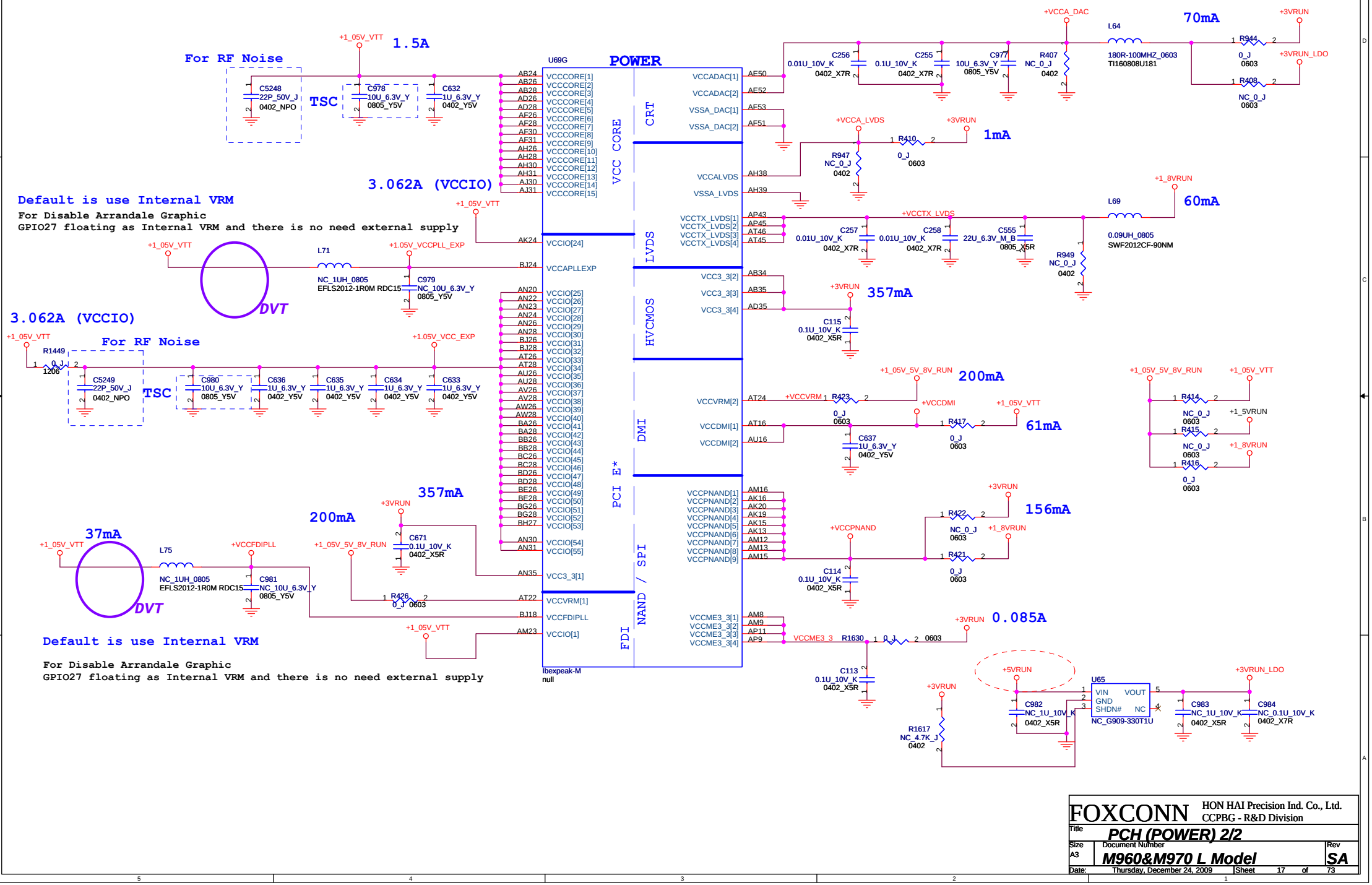
Default is use Internal VRM
For Disable Arrandale Graphic
GPIO27 floating as Internal VRM and there is no need external supply

POWER

DVT
320mA
1.85A
For RF Noise
3.062A (VCCIO)
For RF Noise
196mA
68mA
69mA
163mA
357mA
1mA
2mA
3A (VCCIO)
163mA
163mA
3A (VCCIO)
1mA
EVT
1mA
EVT
357mA
357mA
31mA
DVT
3A (VCCIO)
For EMI
PVT
1.85A
6mA

VCCSUSHDA can be either 1.5V or 3.3V Resume well power, regardless iHDMI is implemented or not. However, external codec/MDC must have the same voltage level as PCH VCCSUSHDA power.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (POWER) 1/2	
Size: Custom	Document Number: M960&M970 L Model	Rev: SA
Date: Thursday, December 24, 2009	Sheet 16 of 73	


POWER
U69G
VCC CORE
CRT
LVDS
HVCMOS
DMI
PCI E*
NAND / SPI
FDI
Ibexpeak-M
null
For RF Noise
1.5A
TSC
3.062A (VCCIO)
Default is use Internal VRM
For Disable Arrandale Graphic
GPIO27 floating as Internal VRM and there is no need external supply
DVT
70mA
1mA
60mA
357mA
200mA
61mA
156mA
0.085A
37mA
+VCCA_DAC
+VCCA_LVDS
+VCCTX_LVDS
+VCCDMI
+VCCPNAND
+VCCFDIPLL
+VCCVRM
+1_05V_VTT
+1.05V_VCC_EXP
+1.05V_VCCPLL_EXP
+1_05V_5V_8V_RUN
+3VRUN
+3VRUN_LDO
+1_8VRUN
+1_5VRUN
+5VRUN
L64
180R-100MHZ_0603
TI160808U181
L69
0.09UH_0805
SWF2012CF-90NM
L71
L75
NC_1UH_0805
EFLS2012-1R0M RDC15
U65
VIN
VOUT
GND
SHDN#
NC
NC_G909-330T1U
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
PCH (POWER) 2/2
Size
A3
Document Number
M960&M970 L Model
Rev
SA
Date:
Thursday, December 24, 2009
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17
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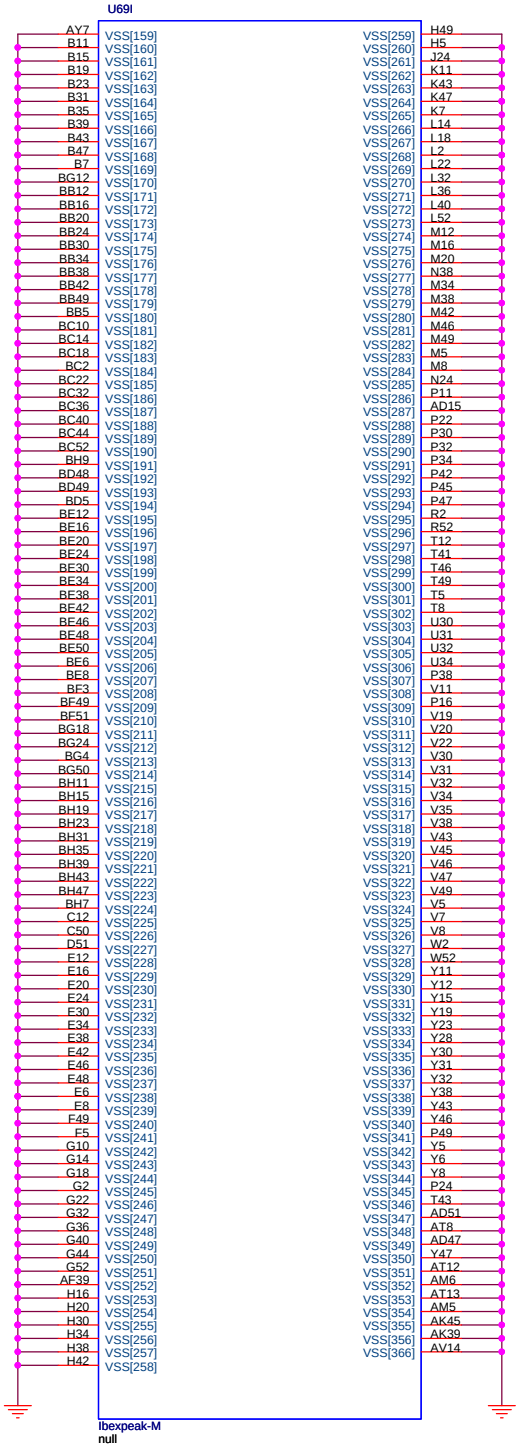
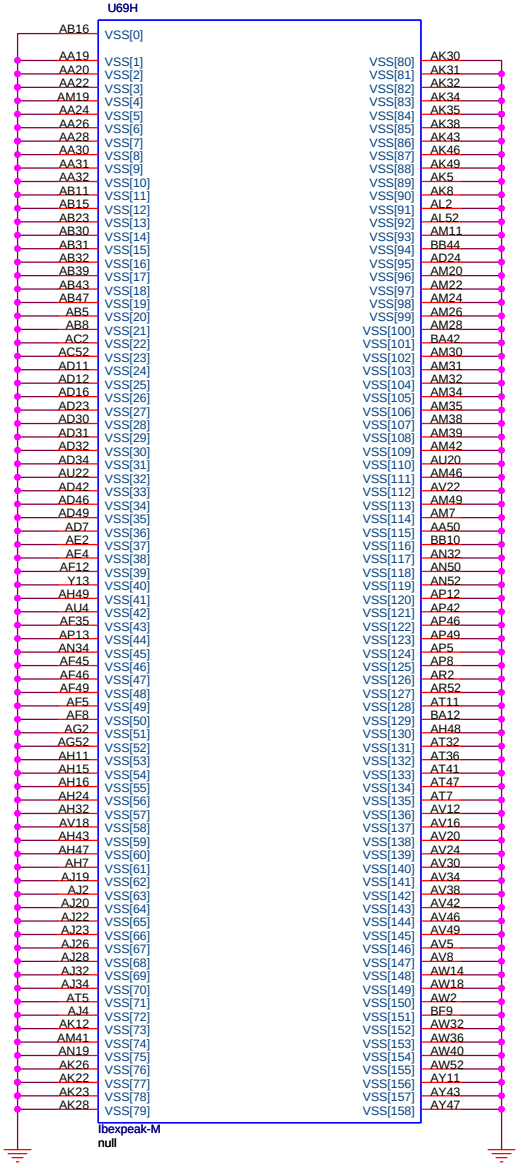
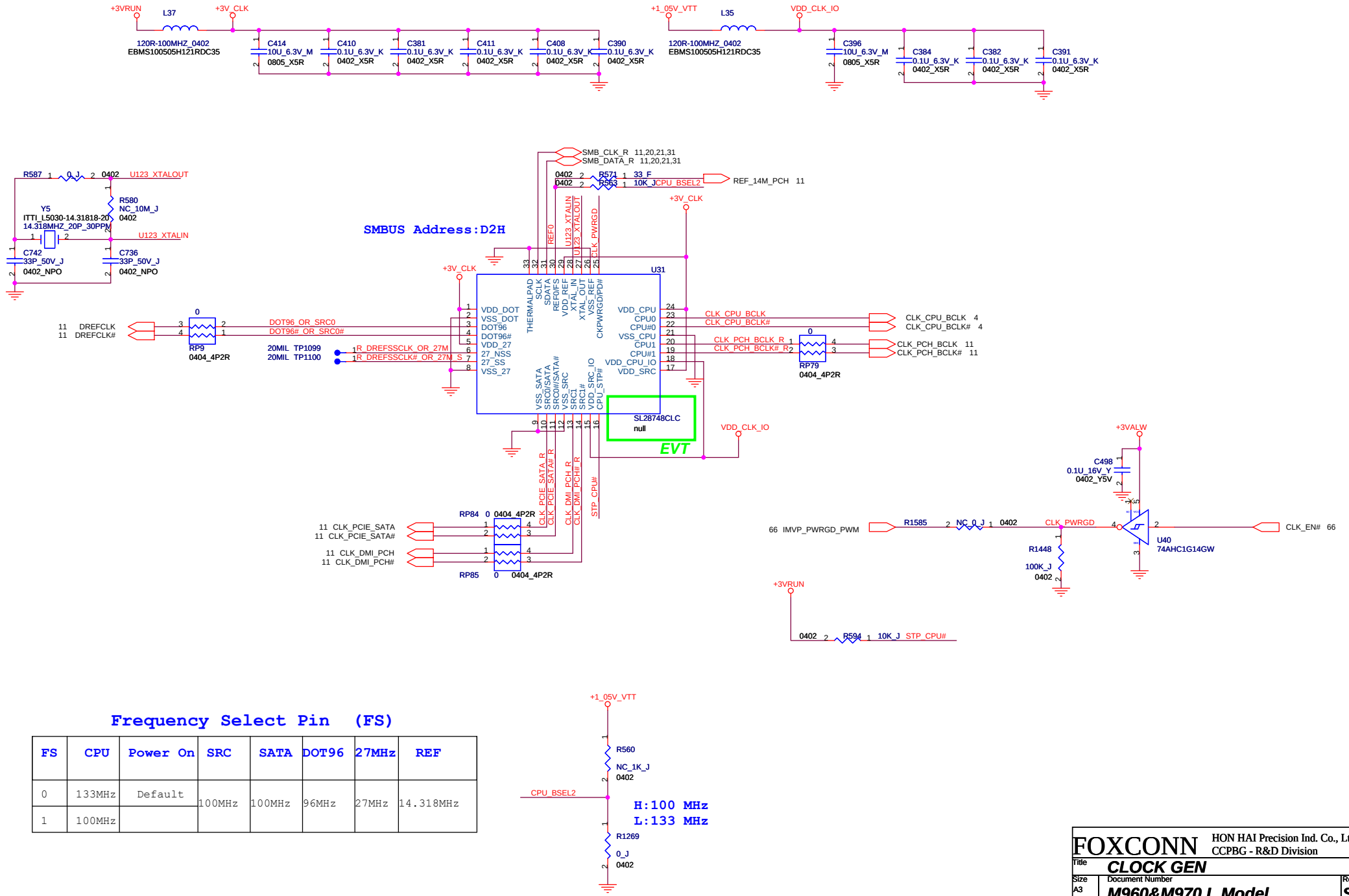
73





FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCH (VSS)	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Thursday, December 24, 2009	Sheet 18 of 73	

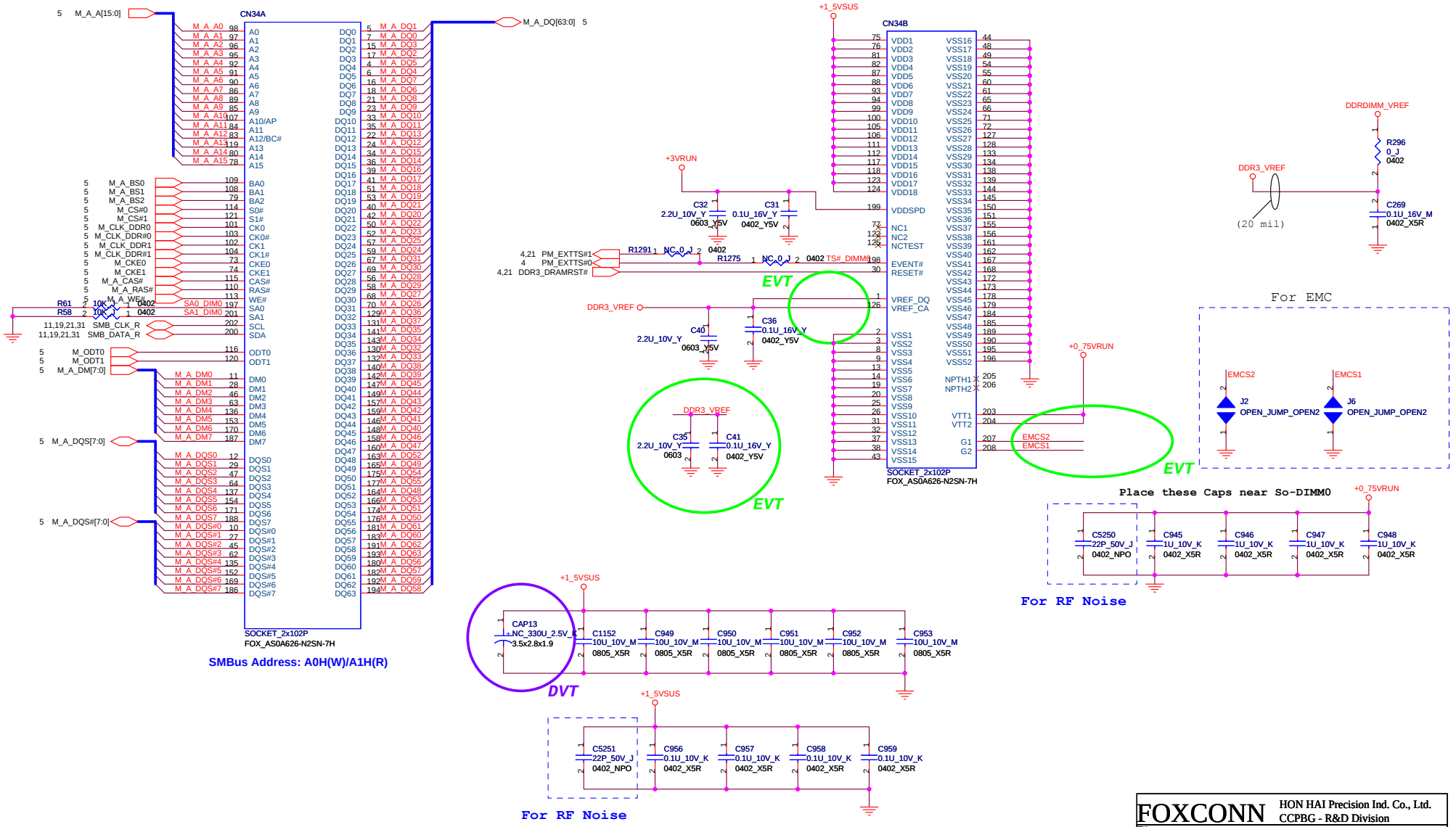


Frequency Select Pin (FS)

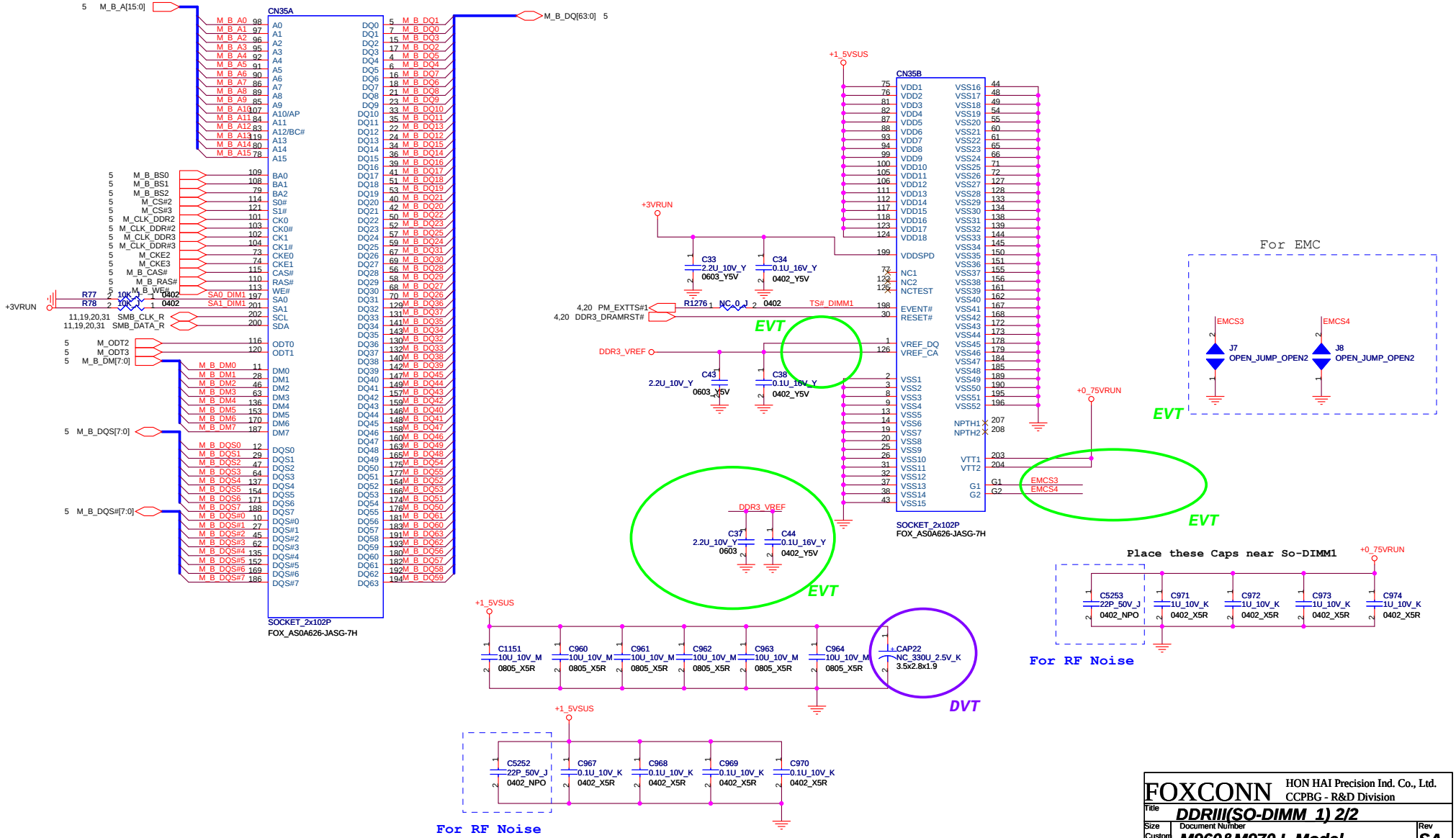
FS	CPU	Power On	SRC	SATA	DOT96	27MHz	REF
0	133MHz	Default	100MHz	100MHz	96MHz	27MHz	14.318MHz
1	100MHz						

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	CLOCK GEN	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 19 of 73	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	DDRIII(SO-DIMM_0) 1/2
Size: Custom	Document Number: M960&M970 L Model
Rev	SA
Date: Tuesday, December 29, 2009	Sheet 20 of 73


CN35A
SOCKET_2x102P
FOX_AS0A626-JASG-7H
CN35B
SOCKET_2x102P
FOX_AS0A626-JASG-7H
EVT
DVT
For EMC
Place these Caps near So-DIMM1
For RF Noise
For RF Noise
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
DDRIII(SO-DIMM_1) 2/2
M960&M970 L Model
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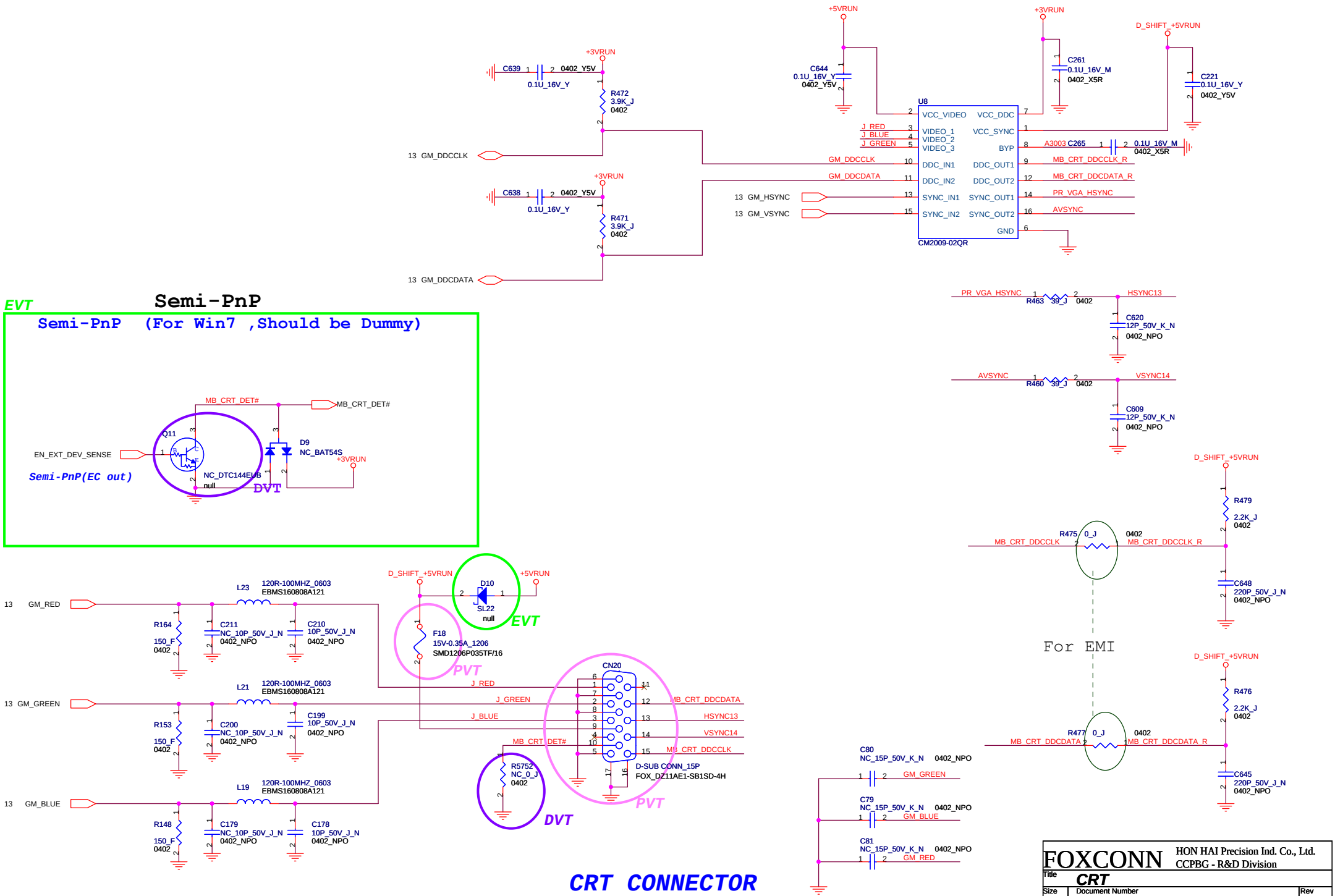
+5VRUN
+3VRUN
D_SHIFT_+5VRUN
C639 0.1U_16V_Y 0402_Y5V
R472 3.9K_J 0402
13 GM_DDCCLK
C638 0.1U_16V_Y 0402_Y5V
R471 3.9K_J 0402
13 GM_DDCDATA
C644 0.1U_16V_Y 0402_Y5V
C261 0.1U_16V_M 0402_X5R
C221 0.1U_16V_Y 0402_Y5V
U8
VCC_VIDEO
VCC_DDC
J_RED
J_BLUE
J_GREEN
VIDEO_1
VIDEO_2
VIDEO_3
VCC_SYNC
BYP
A3003 C265 0.1U_16V_M 0402_X5R
GM_DDCCLK
GM_DDCDATA
DDC_IN1
DDC_IN2
DDC_OUT1
DDC_OUT2
MB_CRT_DDCCLK_R
MB_CRT_DDCDATA_R
13 GM_HSYNC
13 GM_VSYNC
SYNC_IN1
SYNC_IN2
SYNC_OUT1
SYNC_OUT2
PR_VGA_HSYNC
AVSYNC
GND
CM2009-02QR
EVT
Semi-PnP
Semi-PnP (For Win7 ,Should be Dummy)
MB_CRT_DET#
Q11
EN_EXT_DEV_SENSE
Semi-PnP(EC out)
NC_DTC144EUB
null
D9
NC_BAT54S
DVT
PR_VGA_HSYNC
R463 39_J 0402
HSYNC13
C620 12P_50V_K_N 0402_NPO
AVSYNC
R460 39_J 0402
VSYNC14
C609 12P_50V_K_N 0402_NPO
D_SHIFT_+5VRUN
R479 2.2K_J 0402
R475 0_J 0402
MB_CRT_DDCCLK
MB_CRT_DDCCLK_R
C648 220P_50V_J_N 0402_NPO
For EMI
R476 2.2K_J 0402
R477 0_J 0402
MB_CRT_DDCDATA
MB_CRT_DDCDATA_R
C645 220P_50V_J_N 0402_NPO
13 GM_RED
L23 120R-100MHZ_0603 EBMS160808A121
R164 150_F 0402
C211 NC_10P_50V_J_N 0402_NPO
C210 10P_50V_J_N 0402_NPO
D10
SL22
null
EVT
F18 15V-0.35A_1206 SMD1206P035TF/16
PVT
13 GM_GREEN
L21 120R-100MHZ_0603 EBMS160808A121
R153 150_F 0402
C200 NC_10P_50V_J_N 0402_NPO
C199 10P_50V_J_N 0402_NPO
13 GM_BLUE
L19 120R-100MHZ_0603 EBMS160808A121
R148 150_F 0402
C179 NC_10P_50V_J_N 0402_NPO
C178 10P_50V_J_N 0402_NPO
J_RED
J_GREEN
J_BLUE
MB_CRT_DET#
CN20
MB_CRT_DDCDATA
HSYNC13
VSYNC14
MB_CRT_DDCCLK
D-SUB CONN_15P
FOX_DZ11AE1-SB1SD-4H
PVT
R5752 NC_0_J 0402
DVT
C80 NC_15P_50V_K_N 0402_NPO
GM_GREEN
C79 NC_15P_50V_K_N 0402_NPO
GM_BLUE
C81 NC_15P_50V_K_N 0402_NPO
GM_RED
CRT CONNECTOR
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
CRT
Size
A3
Document Number
M960&M970 L Model
Rev
SA
Date: Tuesday, December 29, 2009
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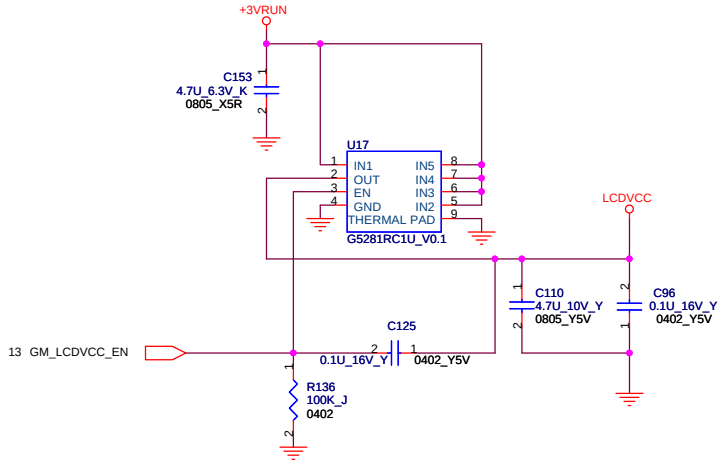

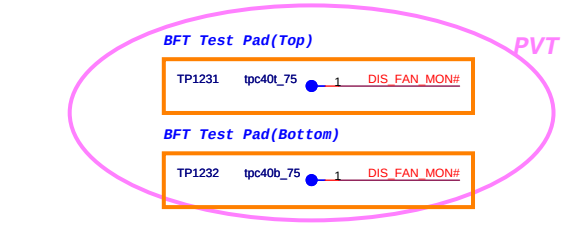

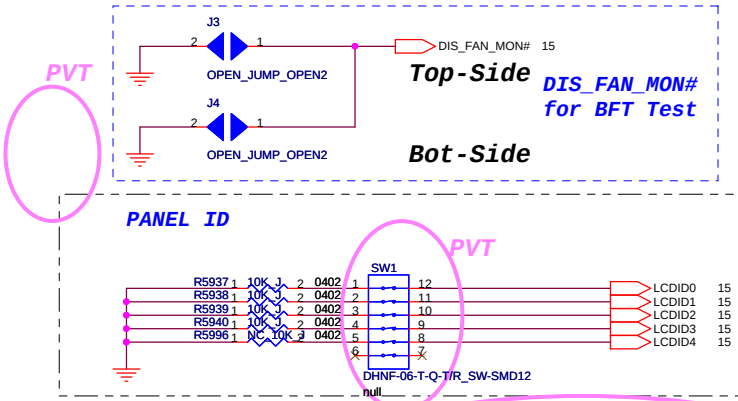

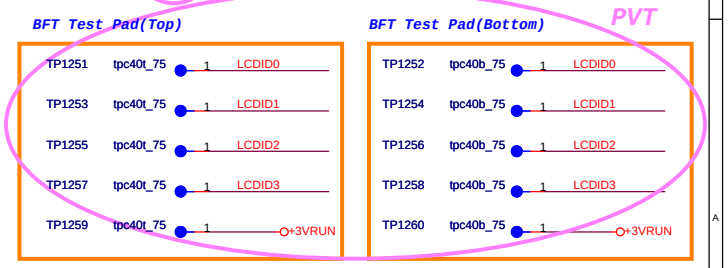

PANEL ID

Type		LED	LED	LED	LED	1	1	1	LED	LED	LED
Size	14	14	14	14	14	15.5	15.5	15.5	15.5	17.3	17.3
Vendor	No LCD	AUO	Samsung	LGD	AUO	LGD	CPT	Samsung	LGD	CPT	AUO
Model Name		B140XW02	LTN140AT08	LP140WH2	B140RW02	LP156WH1	CLAA156WA01A	LTN156AT01	LP156WF1	CLAA173UA01A	B173HW01
Panel ID [4.3.2.1.0]	00000	00001	00010	00011	00100	00110	00111	01000	01001	01011	01100

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: LVDS
Size: A3
Document Number: M960&M970 L Model
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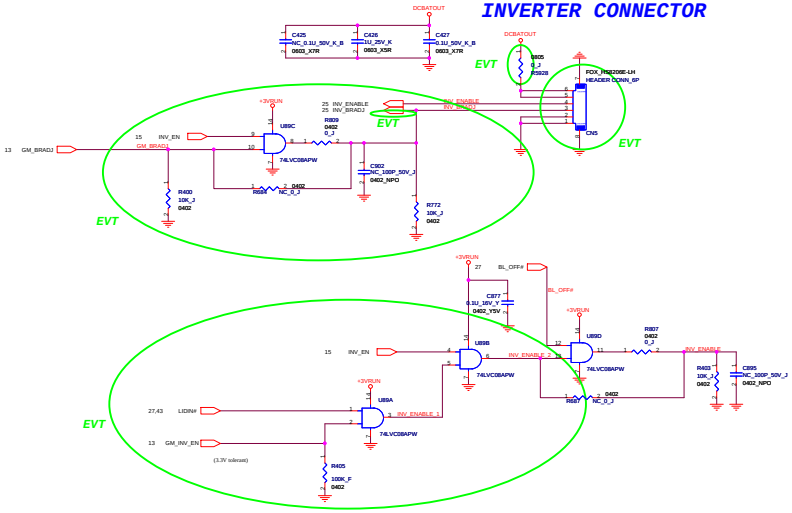
INVERTER CONNECTOR



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
File:	Inverter Connector	
Size: A3	Document Number: M960&M970 L Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 24 of 73	

EVT

For RF verification, del these cap. in DVT if these cap. do not use.

13 ODD_RXIN0-
C6306 NC_3.3P_25V_C 0201_NPO
13 ODD_RXIN0+
13 ODD_RXIN1-
C6307 NC_3.3P_25V_C 0201_NPO
13 ODD_RXIN1+
13 ODD_RXIN2-
C6308 NC_3.3P_25V_C 0201_NPO
13 ODD_RXIN2+
13 ODD_CLKIN-
C6309 NC_3.3P_25V_C 0201_NPO
13 ODD_CLKIN+
13 EVEN_RXIN0-
C6310 NC_3.3P_25V_C 0201_NPO
13 EVEN_RXIN0+
13 EVEN_RXIN1-
C6311 NC_3.3P_25V_C 0201_NPO
13 EVEN_RXIN1+
13 EVEN_RXIN2-
C6312 NC_3.3P_25V_C 0201_NPO
13 EVEN_RXIN2+
13 EVEN_CLKIN-
C6313 NC_3.3P_25V_C 0201_NPO
13 EVEN_CLKIN+

EVT

LVDS CONNECTOR

For RF Noise

LCDVCC
C5255 22P_50V_J 0402_NPO
C1364 4.7U_10V_Y 0805_Y5V
C1365 0.1U_16V_Y 0402_Y5V

1A

DVT

CN13 FOX_GS12401-1012-9H

PVT

ODD_RXIN0-
ODD_RXIN0+
ODD_RXIN1-
ODD_RXIN1+
ODD_RXIN2-
ODD_RXIN2+
ODD_CLKIN-
ODD_CLKIN+
EVEN_RXIN0-
EVEN_RXIN0+
EVEN_RXIN1-
EVEN_RXIN1+
EVEN_RXIN2-
EVEN_RXIN2+
EVEN_CLKIN-
EVEN_CLKIN+

44
43
41
FPC CONN_40P

For rush current issue

L83 NC_600R-100MHZ_0805
ACMS201209A601 2A
DCBATOUT
Q177 SI2303BDS
DCBATOUT_L
F16 32V-2A_0603 467002.
R5736 47K_J 0402
C575 0.1U_50V_K_B 0603
C6305 0.1U_50V_K_B 0603
R5737 47K_J 0402

DVT

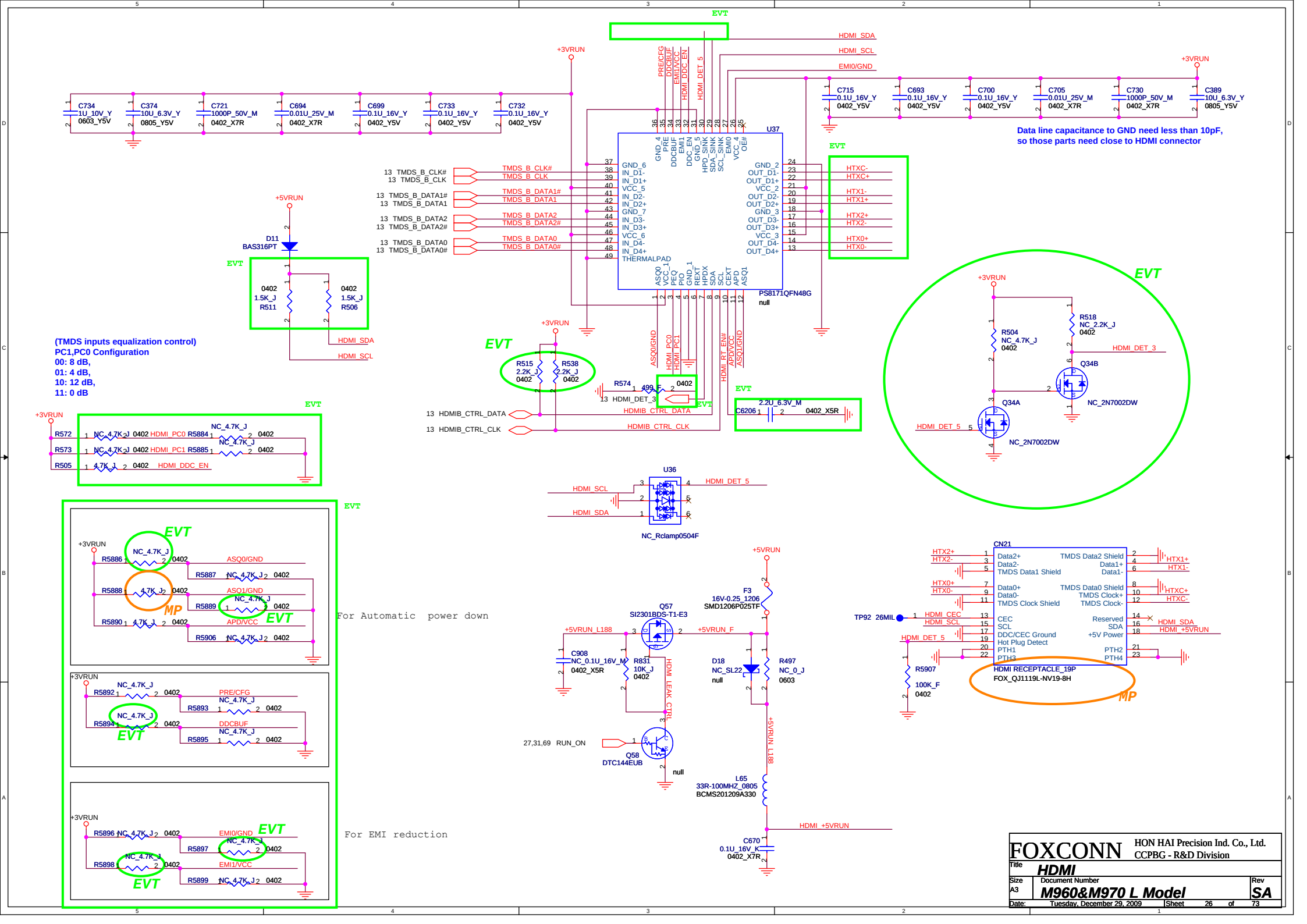
24 INV_BRADJ
24 INV_ENABLE

C6335 680P_50V_K 0603_X7R
C6334 680P_50V_K 0603_X7R

DVT For EMI

Close to CN13

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LVDS Connector	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 25 of 73	


EVT
HDMI_SDA
HDMI_SCL
EMI0/GND
+3VRUN
C734 1U_10V_Y 0603_Y5V
C374 10U_6.3V_Y 0805_Y5V
C721 1000P_50V_M 0402_X7R
C694 0.01U_25V_M 0402_X7R
C699 0.1U_16V_Y 0402_Y5V
C733 0.1U_16V_Y 0402_Y5V
C732 0.1U_16V_Y 0402_Y5V
C715 0.1U_16V_Y 0402_Y5V
C693 0.1U_16V_Y 0402_Y5V
C700 0.1U_16V_Y 0402_Y5V
C705 0.01U_25V_M 0402_X7R
C730 1000P_50V_M 0402_X7R
C389 10U_6.3V_Y 0805_Y5V
Data line capacitance to GND need less than 10pF, so those parts need close to HDMI connector
U37
PS8171QFN48G
null
13 TMDS_B_CLK#
13 TMDS_B_CLK
13 TMDS_B_DATA1#
13 TMDS_B_DATA1
13 TMDS_B_DATA2
13 TMDS_B_DATA2#
13 TMDS_B_DATA0
13 TMDS_B_DATA0#
HTXC-
HTXC+
HTX1-
HTX1+
HTX2+
HTX2-
HTX0+
HTX0-
+5VRUN
D11
BAS316PT
0402 1.5K_J R511
0402 1.5K_J R506
(TMDS inputs equalization control)
PC1,PC0 Configuration
00: 8 dB,
01: 4 dB,
10: 12 dB,
11: 0 dB
R515 2.2K_J 0402
R538 2.2K_J 0402
R574 499_F 0402
13 HDMI_DET_3
13 HDMIB_CTRL_DATA
13 HDMIB_CTRL_CLK
C6206 2.2U_6.3V_M 0402_X5R
R572 NC_4.7K_J 0402 HDMI_PC0
R573 NC_4.7K_J 0402 HDMI_PC1
R505 4.7K_J 0402 HDMI_DDC_EN
R5884 NC_4.7K_J 0402
R5885 NC_4.7K_J 0402
R504 NC_4.7K_J 0402
R518 NC_2.2K_J 0402
HDMI_DET_3
Q34B
Q34A
NC_2N7002DW
HDMI_DET_5
U36
NC_Rclamp0504F
R5886 NC_4.7K_J 0402 ASQ0/GND
R5887 NC_4.7K_J 0402
R5888 4.7K_J 0402 ASQ1/GND
R5889 NC_4.7K_J 0402
R5890 4.7K_J 0402 APD/VCC
R5906 NC_4.7K_J 0402
MP
For Automatic power down
R5892 NC_4.7K_J 0402 PRE/CFG
R5893 NC_4.7K_J 0402
R5894 NC_4.7K_J 0402 DDCBUF
R5895 NC_4.7K_J 0402
R5896 NC_4.7K_J 0402 EMI0/GND
R5897 NC_4.7K_J 0402
R5898 NC_4.7K_J 0402 EMI1/VCC
R5899 NC_4.7K_J 0402
For EMI reduction
Q57
SI2301BDS-T1-E3
+5VRUN_L188
+5VRUN_F
F3
16V-0.25_1206
SMD1206P025TF
C908 NC_0.1U_16V_M 0402_X5R
R831 10K_J 0402
HDMI_LEAK_CTRL
D18
NC_SL22
null
R497 NC_0_J 0603
27,31,69 RUN_ON
Q58
DTC144EUB
L65
33R-100MHZ_0805
BCMS201209A330
C670 0.1U_16V_K 0402_X7R
HDMI_+5VRUN
CN21
HDMI RECEPTACLE_19P
FOX_QJ1119L-NV19-8H
TP92 26MIL
R5907 100K_F 0402
HTX2+
HTX2-
HTX1+
HTX1-
HTX0+
HTX0-
HTXC+
HTXC-
HDMI_CEC
HDMI_SCL
HDMI_SDA
HDMI_+5VRUN
HDMI_DET_5
Data2+
Data2-
TMDS Data1 Shield
Data0+
Data0-
TMDS Clock Shield
CEC
SCL
DDC/CEC Ground
Hot Plug Detect
PTH1
PTH3
TMDS Data2 Shield
Data1+
Data1-
TMDS Data0 Shield
TMDS Clock+
TMDS Clock-
Reserved
SDA
+5V Power
PTH2
PTH4
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
HDMI
Size
A3
Document Number
M960&M970 L Model
Rev
SA
Date: Tuesday, December 29, 2009
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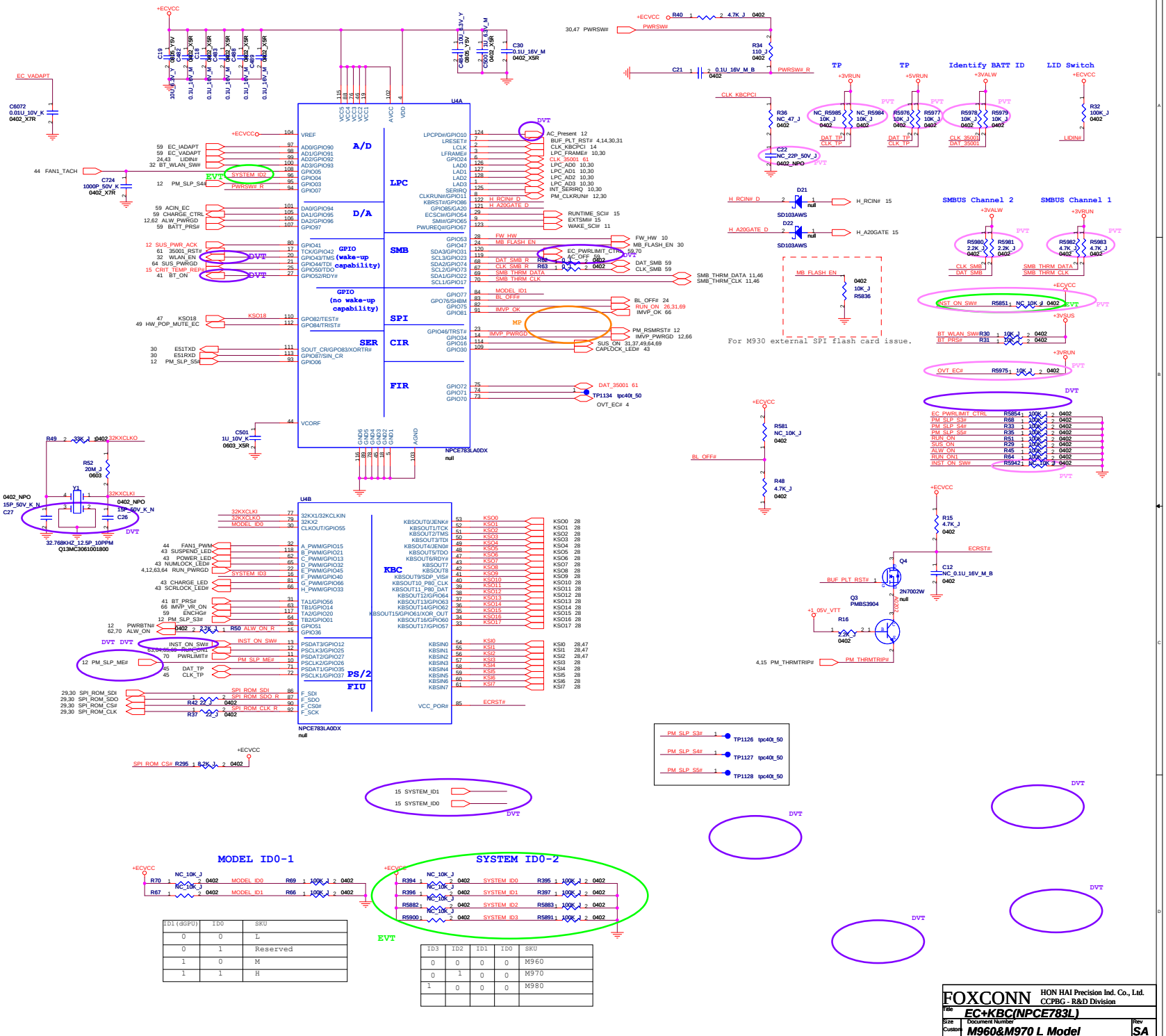

ID1(dGPU)	ID0	SKU
0	0	L
0	1	Reserved
1	0	M
1	1	H

ID3	ID2	ID1	ID0	SKU
0	0	0	0	M960
0	1	0	0	M970
1	0	0	0	M980

FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: EC+KBC(NPCE783L)

Size: Custom | Document Number: M960&M970 L Model | Rev: SA

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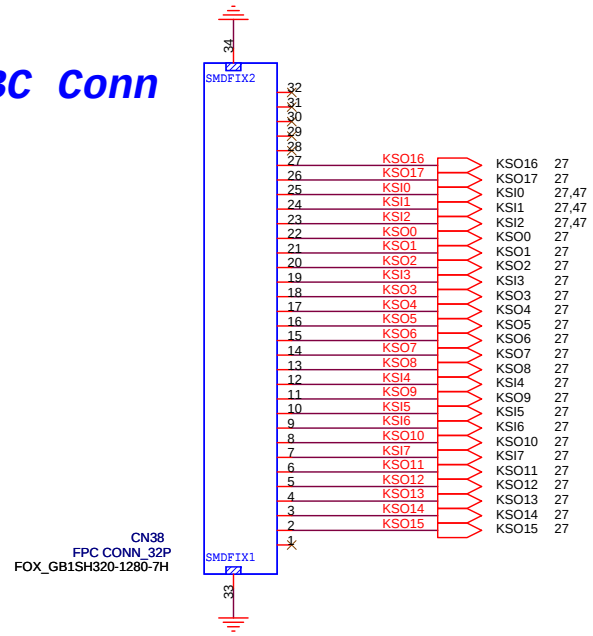
KBC Conn



CN38
FPC CONN_32P
FOX_GB1SH320-1280-7H

BFT Test Pad(Top)

TP1198	tpc40t_75	1	KSI7
TP1200	tpc40t_75	1	KSO10
TP1202	tpc40t_75	1	KSO6
TP1204	tpc40t_75	1	KSI2
TP1206	tpc40t_75	1	KSI0
TP1233	tpc40t_75	1	KSI3
TP1234	tpc40t_75	1	KSO13

PVT

BFT Test Pad(Bottom)

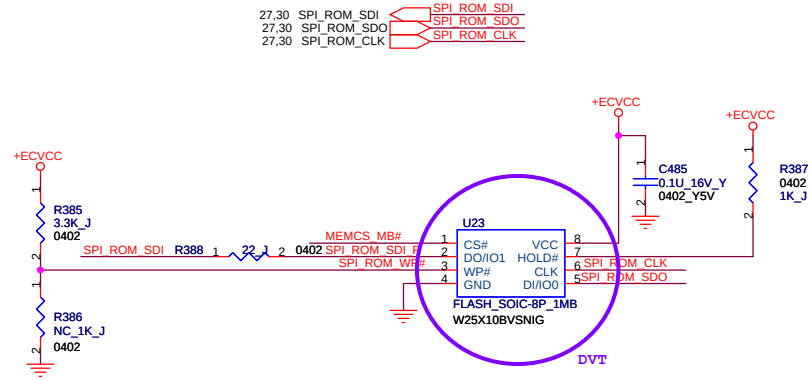
TP1199	tpc40b_75	1	KSI7
TP1201	tpc40b_75	1	KSO10
TP1203	tpc40b_75	1	KSO6
TP1205	tpc40b_75	1	KSI2
TP1207	tpc40b_75	1	KSI0

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

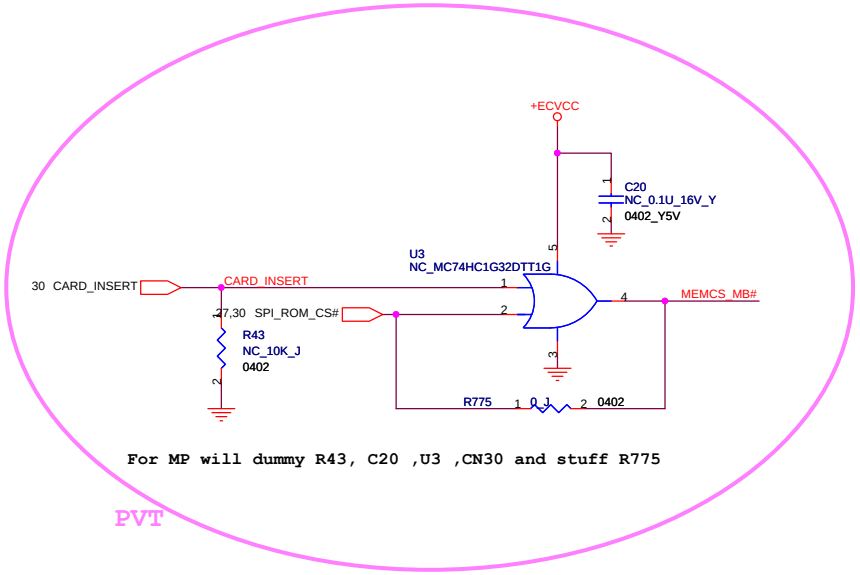
Title: **KB Connector**

Size: B | Document Number: **M960&M970 L Model** | Rev: **SA**

Date: Tuesday, December 29, 2009 | Sheet 28 of 73

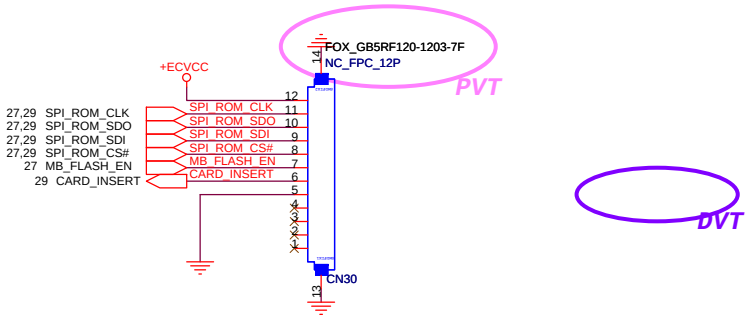


SPI ROM (EC Firmware) (1Mb)

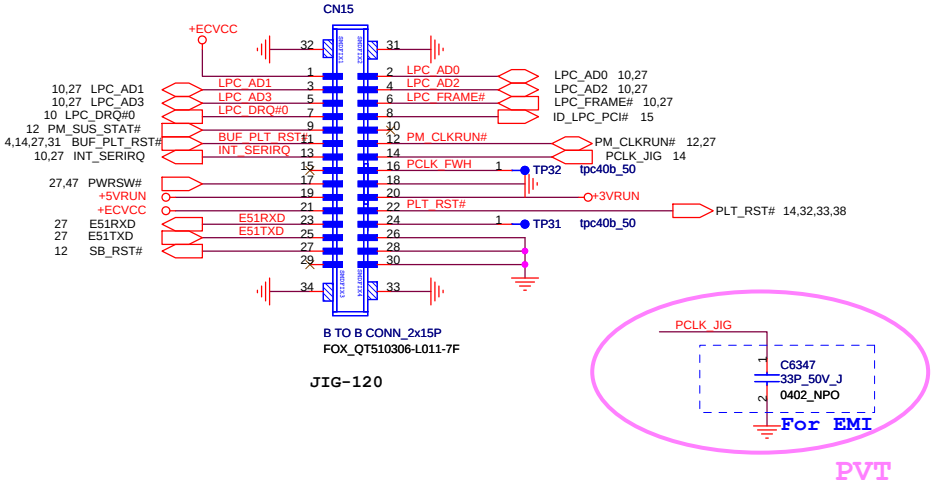


For MP will dummy R43, C20 ,U3 ,CN30 and stuff R775

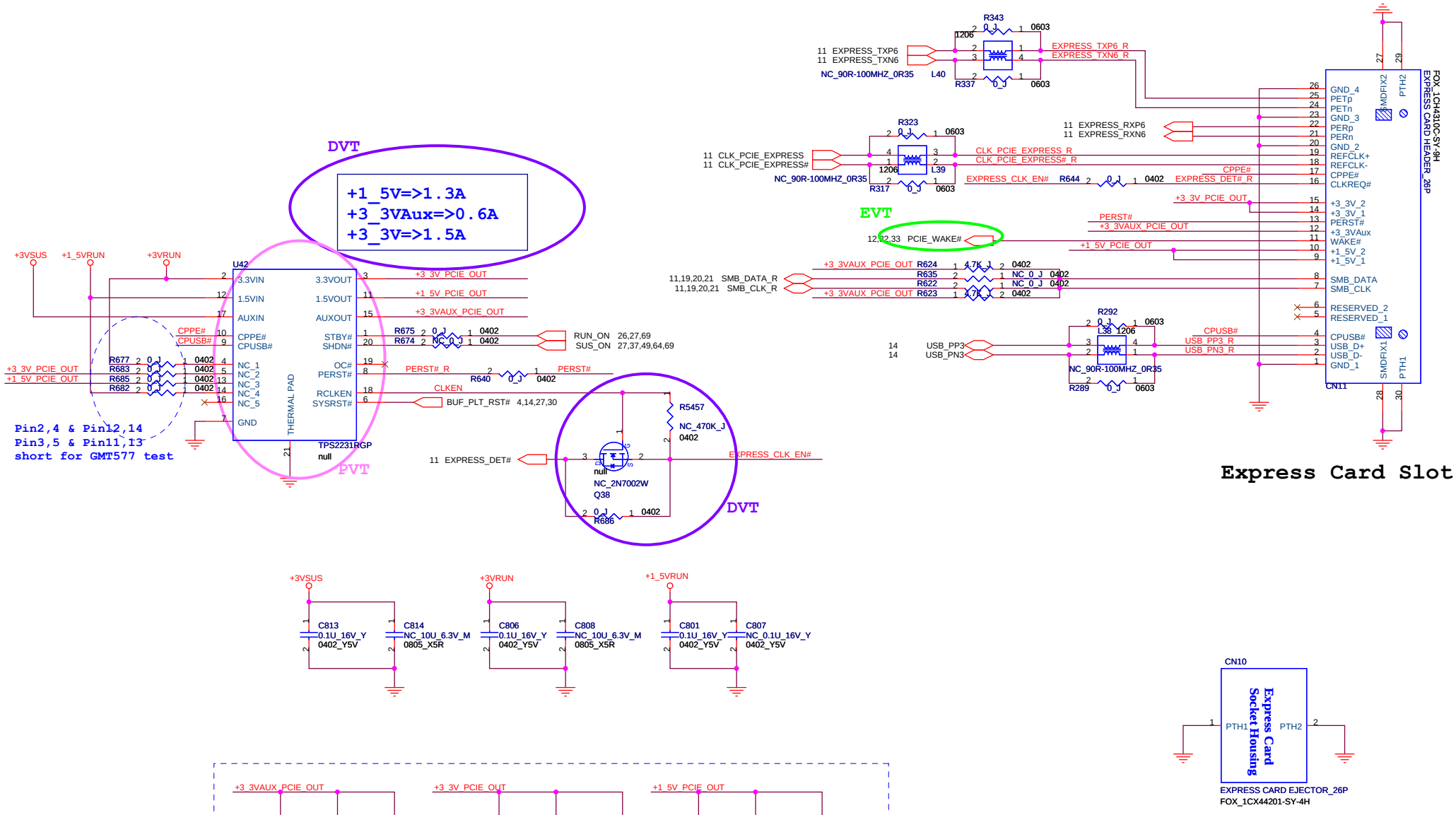
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SPI Flash ROM	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 29 of 73	



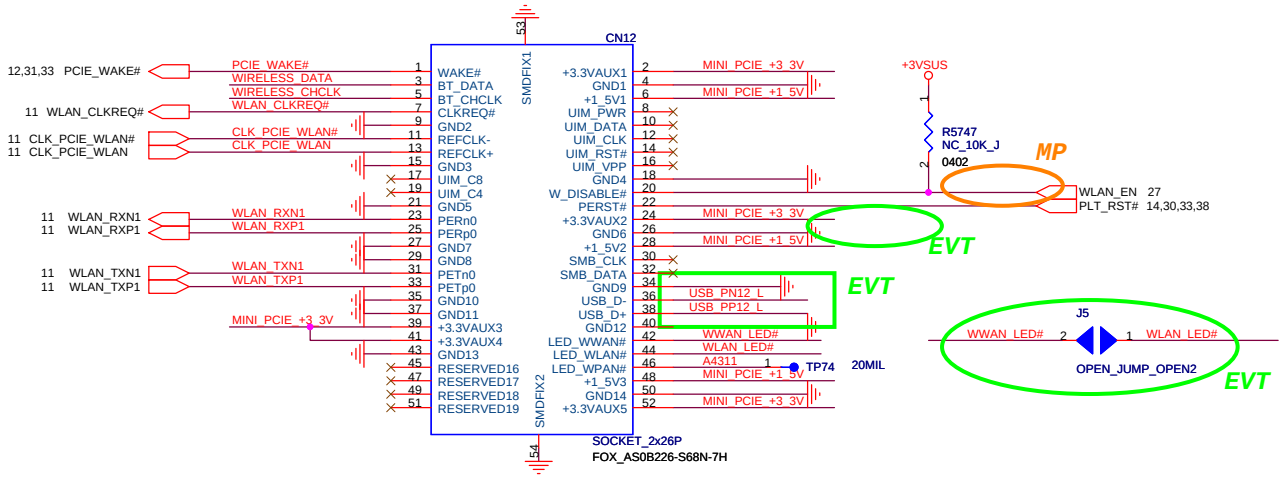
EXTERNAL SPI ROM INTERFACE (EC)

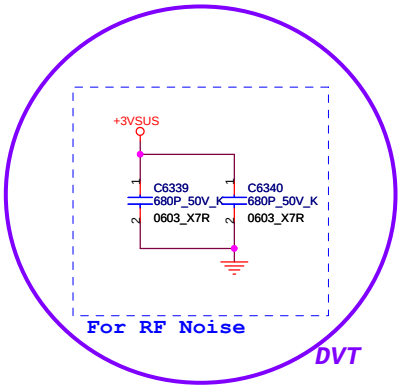


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**Debug Port**	
Size A3	Document Number **M960&M970 L Model**	Rev **SA**
Date: Tuesday, December 29, 2009	Sheet 30 of 73	

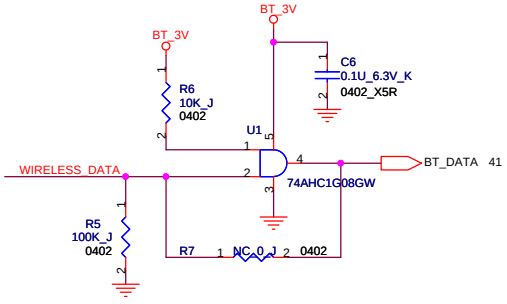


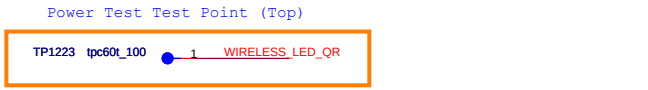
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	EXPRESS CARD	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 31 of 73	

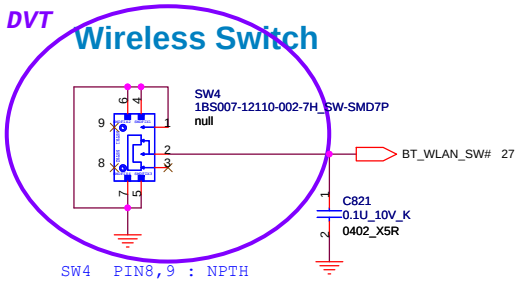


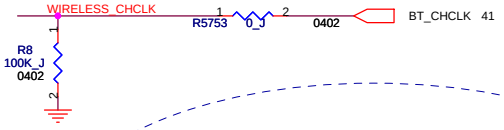


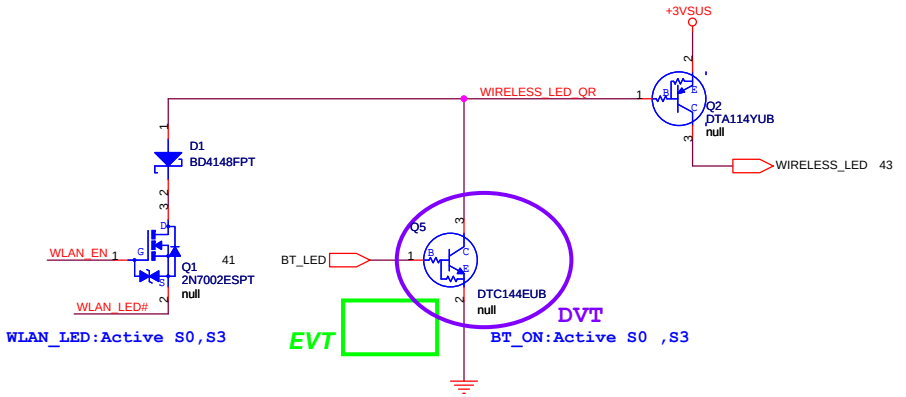
Half Size Mini Card



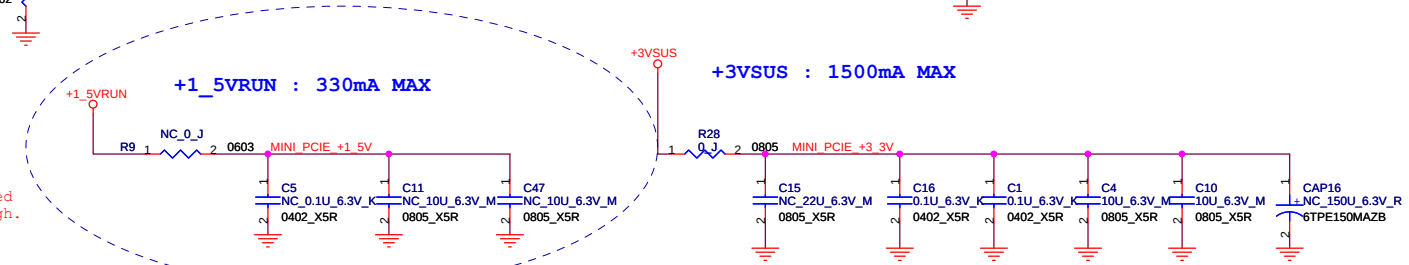


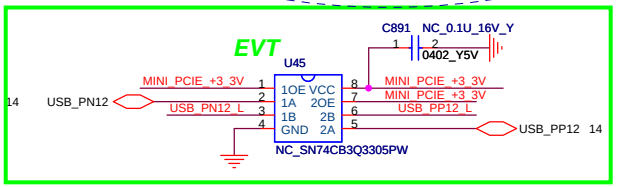




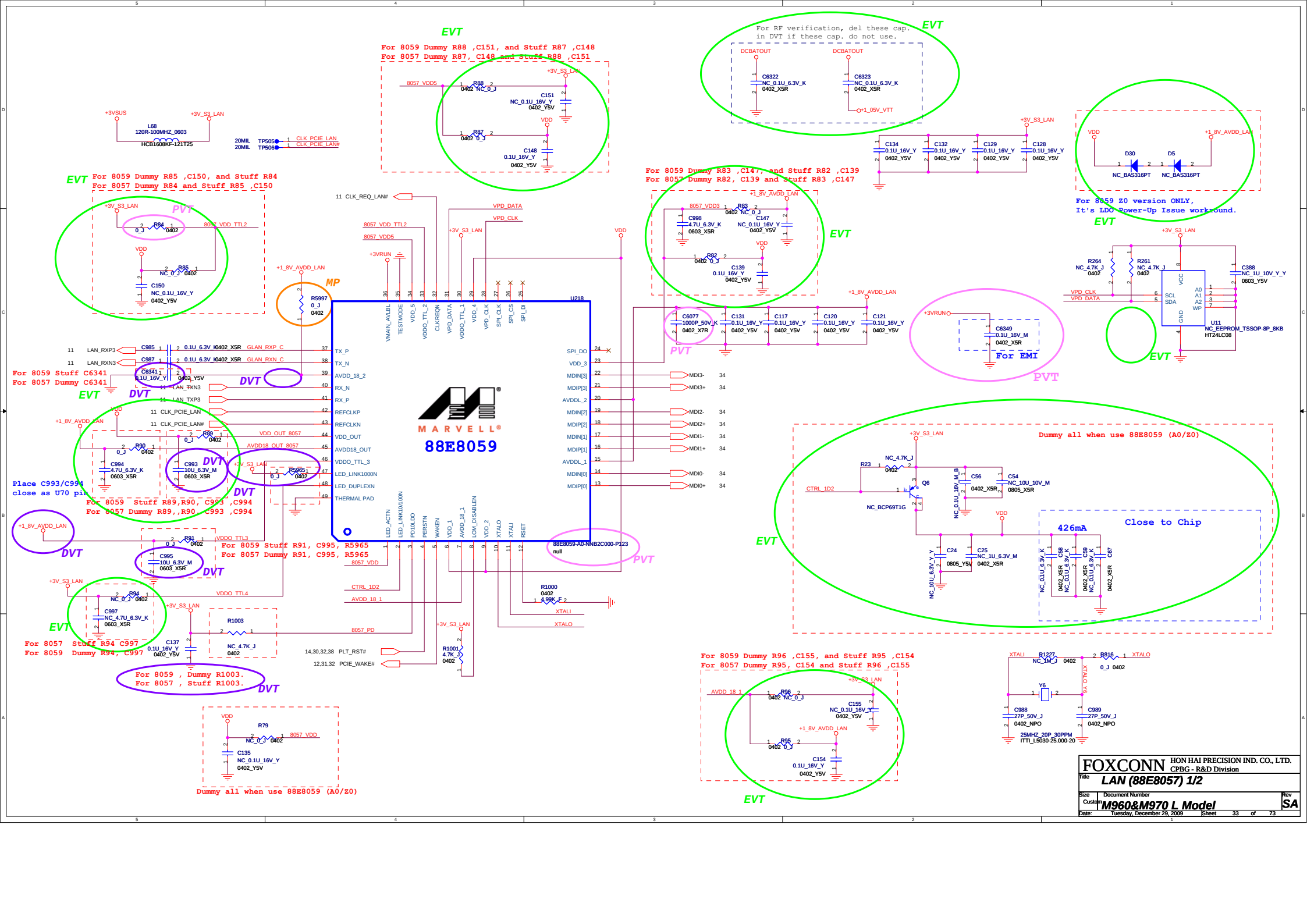


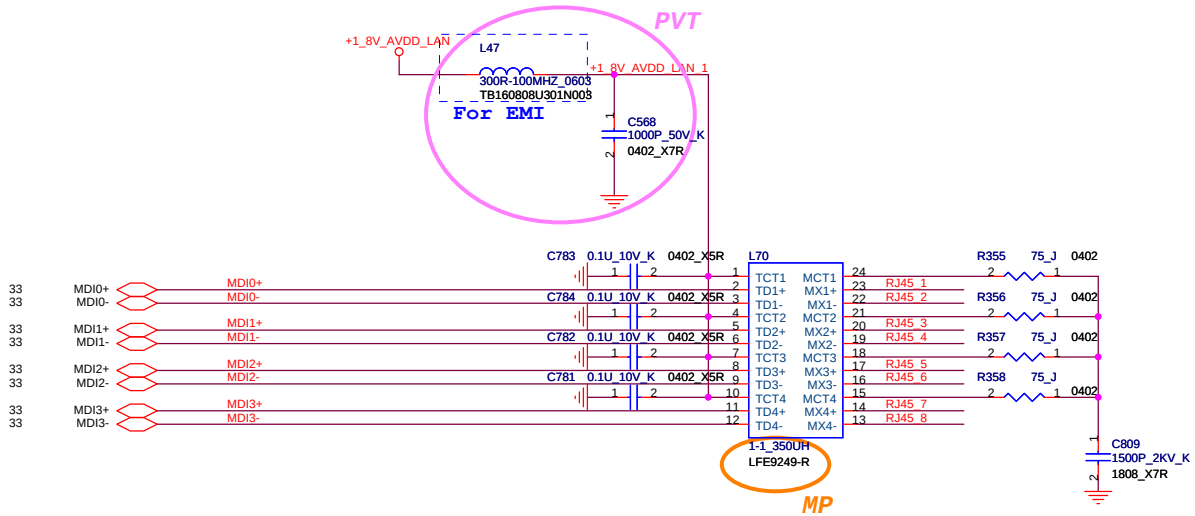
This is a reserved circuit.
According to RF comment,
this circuit could be deleted
if Layout space is not enough.

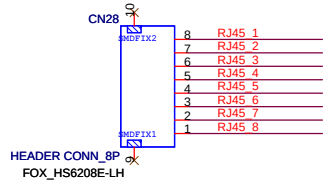




FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Mini-PCIE Card (WLAN)	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 32 of 73	


EVT
For 8059 Dummy R88 ,C151, and Stuff R87 ,C148
For 8057 Dummy R87, C148 and Stuff R88 ,C151
For RF verification, del these cap.
in DVT if these cap. do not use.
EVT
DCBATOUT
DCBATOUT
C6322
NC_0.1U_6.3V_K
0402_X5R
C6323
NC_0.1U_6.3V_K
0402_X5R
+1_05V_VTT
+3V_S3_LAN
C134
0.1U_16V_Y
0402_Y5V
C132
0.1U_16V_Y
0402_Y5V
C129
0.1U_16V_Y
0402_Y5V
C128
0.1U_16V_Y
0402_Y5V
VDD
+1_8V_AVDD_LAN
D30
D5
NC_BAS316PT
NC_BAS316PT
For 8059 Z0 version ONLY,
It's LDO Power-Up Issue workround.
EVT
+3V_S3_LAN
R264
NC_4.7K_J
0402
R261
NC_4.7K_J
0402
VPD_CLK
VPD_DATA
SCL
SDA
VCC
GND
A0
A1
A2
WP
C388
NC_1U_10V_Y_Y
0603_Y5V
U11
NC_EEPROM_TSSOP-8P_8KB
HT24LC08
EVT
L68
120R-100MHZ_0603
HCB1608KF-121T25
+3VSUS
+3V_S3_LAN
20MIL
TP505
20MIL
TP506
CLK_PCIE_LAN
CLK_PCIE_LAN#
EVT
For 8059 Dummy R85 ,C150, and Stuff R84
For 8057 Dummy R84 and Stuff R85 ,C150
PVT
+3V_S3_LAN
R84
0_J
0402
8057_VDD_TTL2
VDD
R85
NC_0_J
0402
C150
NC_0.1U_16V_Y
0402_Y5V
For 8059 Dummy R83 ,C147, and Stuff R82 ,C139
For 8057 Dummy R82, C139 and Stuff R83 ,C147
EVT
+1_8V_AVDD_LAN
8057_VDD3
R83
0402
NC_0_J
C998
4.7U_6.3V_K
0603_X5R
C147
NC_0.1U_16V_Y
0402_Y5V
VDD
R82
0402
0_J
C139
0.1U_16V_Y
0402_Y5V
11 CLK_REQ_LAN#
VPD_DATA
VPD_CLK
8057_VDD_TTL2
8057_VDD5
+3VRUN
+3V_S3_LAN
VDD
+1_8V_AVDD_LAN
MP
R5997
0_J
0402
U218
VMAIN_AVLBL
TESTMODE
VDD_5
VDDIO_TTL_2
CLKREQN
VPD_DATA
VDDIO_TTL_1
VDD_4
VPD_CLK
SPI_CLK
SPI_CS
SPI_DI
C6077
1000P_50V_K
0402_X7R
C131
0.1U_16V_Y
0402_Y5V
C117
0.1U_16V_Y
0402_Y5V
C120
0.1U_16V_Y
0402_Y5V
C121
0.1U_16V_Y
0402_Y5V
PVT
+3VRUN
C6349
0.1U_16V_M
0402_X5R
For EMI
PVT
11 LAN_RXP3
11 LAN_RXN3
C985
C987
0.1U_6.3V_K
0402_X5R
GLAN_RXP_C
GLAN_RXN_C
C6341
0.1U_16V_Y
0402_Y5V
For 8059 Stuff C6341
For 8057 Dummy C6341
EVT
DVT
11 LAN_TXP3
11 LAN_TXN3
11 CLK_PCIE_LAN
11 CLK_PCIE_LAN#
TX_P
TX_N
AVDD_18_2
RX_N
RX_P
REFCLKP
REFCLKN
VDD_OUT
AVDD18_OUT
VDDO_TTL_3
LED_LINK1000N
LED_DUPLEXN
THERMAL PAD
SPI_DO
VDD_3
MDIN[3]
MDIP[3]
AVDDL_2
MDIN[2]
MDIP[2]
MDIN[1]
MDIP[1]
AVDDL_1
MDIN[0]
MDIP[0]
MDI3-
MDI3+
MDI2-
MDI2+
MDI1-
MDI1+
MDI0-
MDI0+
MARVELL
88E8059
VDD
+1_8V_AVDD_LAN
R90
0_J
0402
R89
0_J
0402
VDD_OUT_8057
AVDD18_OUT_8057
C994
4.7U_6.3V_K
0603_X5R
C993
10U_6.3V_M
0603_X5R
+3V_S3_LAN
R5965
0_J
0402
DVT
Place C993/C994
close as U70 pin
For 8059 Stuff R89,R90, C993 ,C994
For 8057 Dummy R89,,R90, C993 ,C994
LED_ACTN
LED_LINK10/100N
PD10LDO
PERSTN
WAKEN
VDD_1
AVDD_18_1
LOW_DISABLEN
VDD_2
XTALO
XTALI
RSET
88E8059-A0-NNB2C000-P123
null
PVT
+1_8V_AVDD_LAN
R91
0_J
0402
VDDO_TTL3
C995
10U_6.3V_M
0603_X5R
For 8059 Stuff R91, C995, R5965
For 8057 Dummy R91, C995, R5965
DVT
8057_VDD
CTRL_1D2
AVDD_18_1
R1000
0402
4.99K_F
XTALI
XTALO
+3V_S3_LAN
R94
NC_0_J
0402
VDDO_TTL4
C997
NC_4.7U_6.3V_K
0603_X5R
EVT
For 8057 Stuff R94 C997
For 8059 Dummy R94, C997
+3V_S3_LAN
R1003
NC_4.7K_J
0402
C137
0.1U_16V_Y
0402_Y5V
8057_PD
14,30,32,38 PLT_RST#
12,31,32 PCIE_WAKE#
R1001
4.7K_J
0402
+3V_S3_LAN
For 8059 , Dummy R1003.
For 8057 , Stuff R1003.
DVT
VDD
R79
NC_0_J
0402
8057_VDD
C135
NC_0.1U_16V_Y
0402_Y5V
Dummy all when use 88E8059 (A0/Z0)
Dummy all when use 88E8059 (A0/Z0)
+3V_S3_LAN
R23
NC_4.7K_J
0402
CTRL_1D2
Q6
NC_BCP69T1G
C56
NC_0.1U_16V_M_B
0402_X5R
C54
NC_10U_10V_M
0805_X5R
VDD
426mA
Close to Chip
C24
0805_Y5V
C25
NC_1U_6.3V_M
0402_X5R
NC_10U_6.3V_Y
C58
NC_0.1U_6.3V_K
0402_X5R
C59
NC_0.1U_6.3V_K
0402_X5R
C67
0402_X5R
EVT
For 8059 Dummy R96 ,C155, and Stuff R95 ,C154
For 8057 Dummy R95, C154 and Stuff R96 ,C155
AVDD_18_1
+3V_S3_LAN
R96
0402
NC_0_J
C155
NC_0.1U_16V_Y
0402_Y5V
+1_8V_AVDD_LAN
R95
0402
0_J
C154
0.1U_16V_Y
0402_Y5V
EVT
XTALI
R1227
NC_1M_J
0402
R816
0_J
0402
XTALO
Y6
C988
27P_50V_J
0402_NPO
C989
27P_50V_J
0402_NPO
25MHZ_20P_30PPM
ITTI_L5030-25.000-20
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
LAN (88E8057) 1/2
Size
Custom
Document Number
M960&M970 L Model
Rev
SA
Date:
Tuesday, December 29, 2009
Sheet
33
of
73





RJ45

BFT Test Point(TOP)

TP1166	tpc40t_75	1	RJ45_8	TP1174	tpc40t_75	1	RJ45_4
TP1168	tpc40t_75	1	RJ45_7	TP1176	tpc40t_75	1	RJ45_3
TP1170	tpc40t_75	1	RJ45_6	TP1178	tpc40t_75	1	RJ45_2
TP1172	tpc40t_75	1	RJ45_5	TP1180	tpc40t_75	1	RJ45_1

BFT Test Point(Bottom)

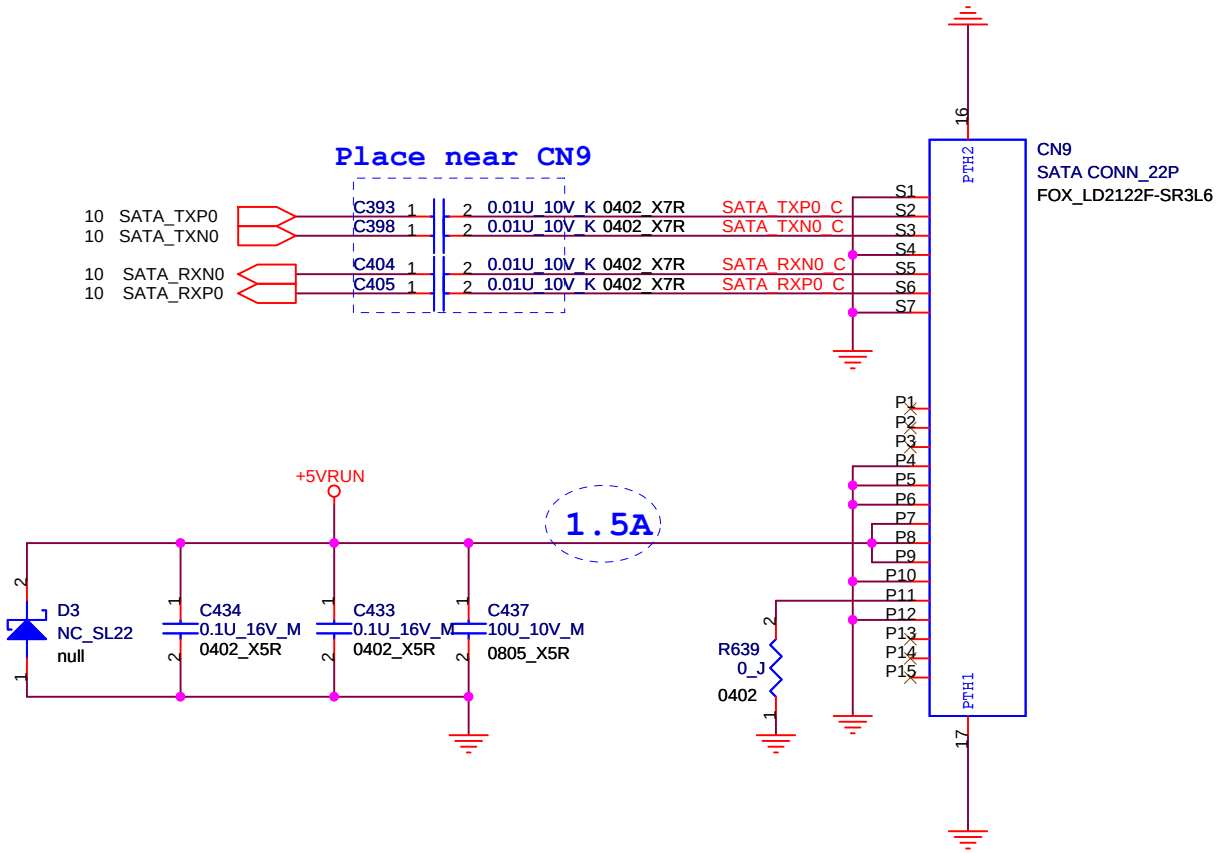
TP1167	tpc40b_75	1	RJ45_8	TP1175	tpc40b_75	1	RJ45_4
TP1169	tpc40b_75	1	RJ45_7	TP1177	tpc40b_75	1	RJ45_3
TP1171	tpc40b_75	1	RJ45_6	TP1179	tpc40b_75	1	RJ45_2
TP1173	tpc40b_75	1	RJ45_5	TP1181	tpc40b_75	1	RJ45_1

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: LAN (Transfomer)(2/2)

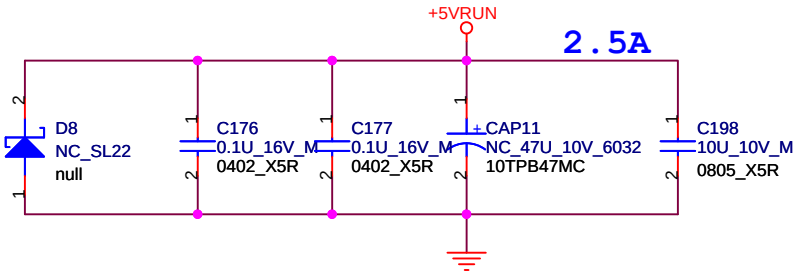
Size: A3 | Document Number: M960&M970 L Model | Rev: SA

Date: Tuesday, December 29, 2009 | Sheet 34 of 73

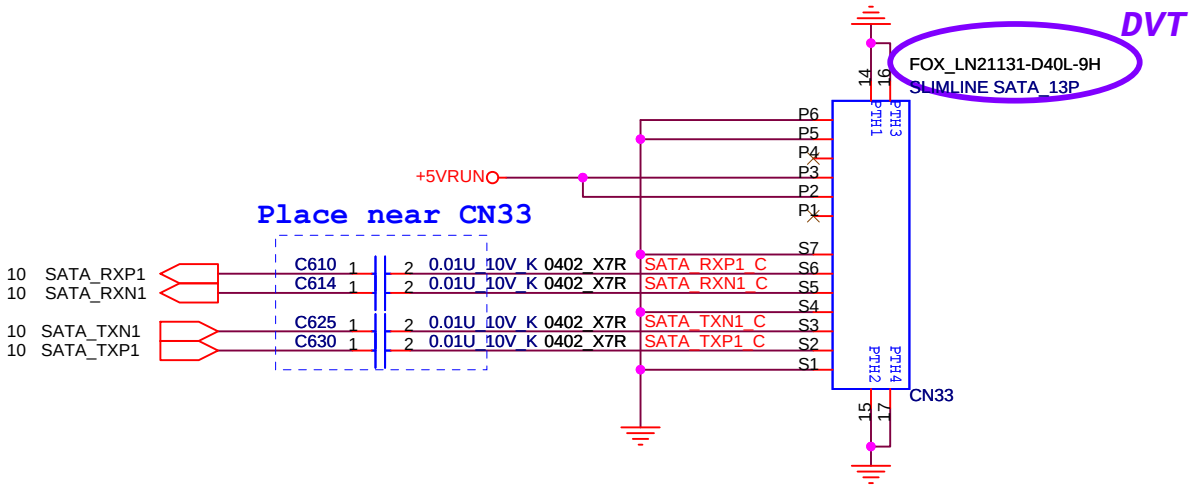


SATA HDD CONN

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: SATA HDD		
Size: A4	Document Number: M960&M970 L Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 35 of 73	



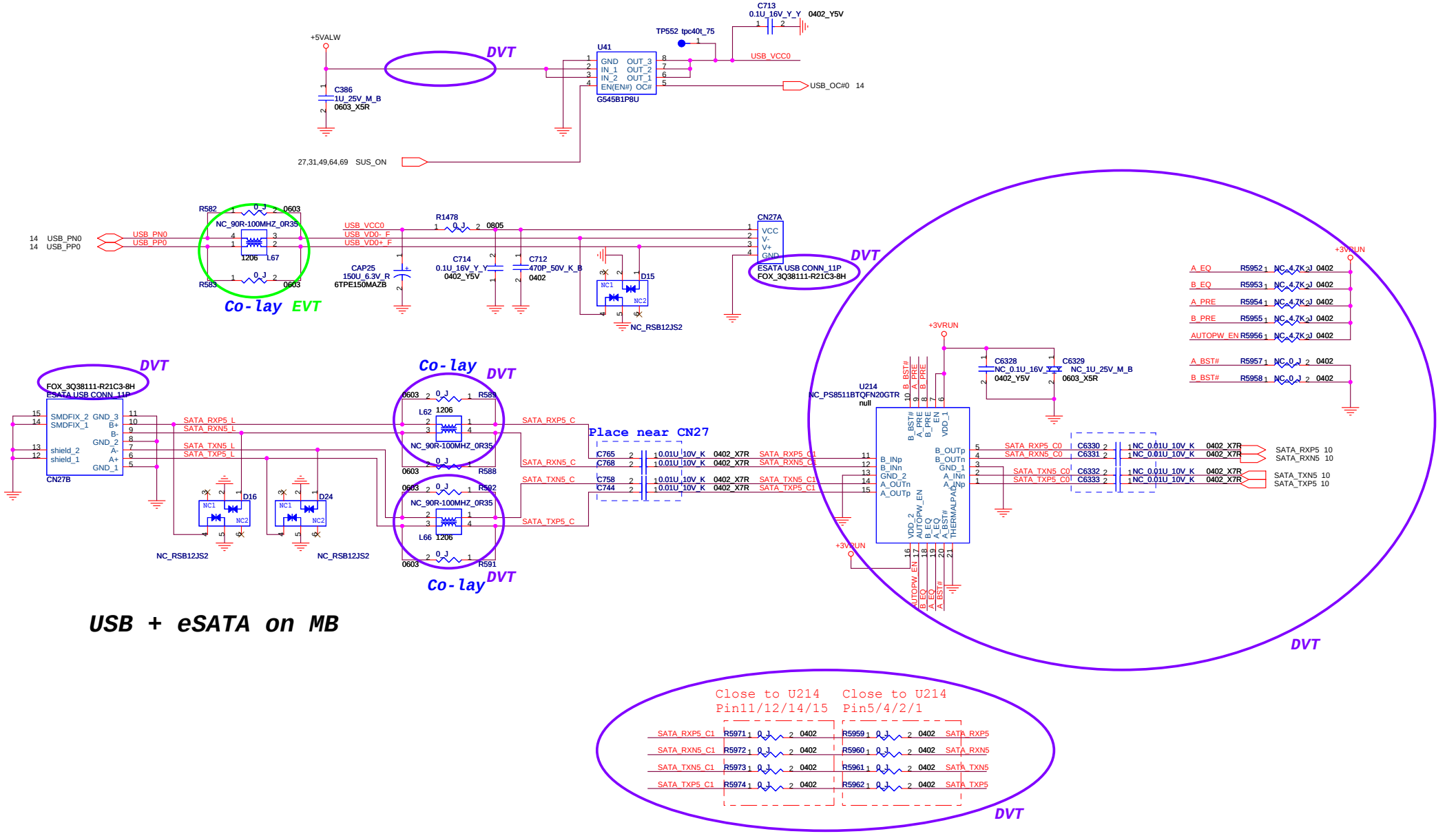
DVT



SATA ODD CONN

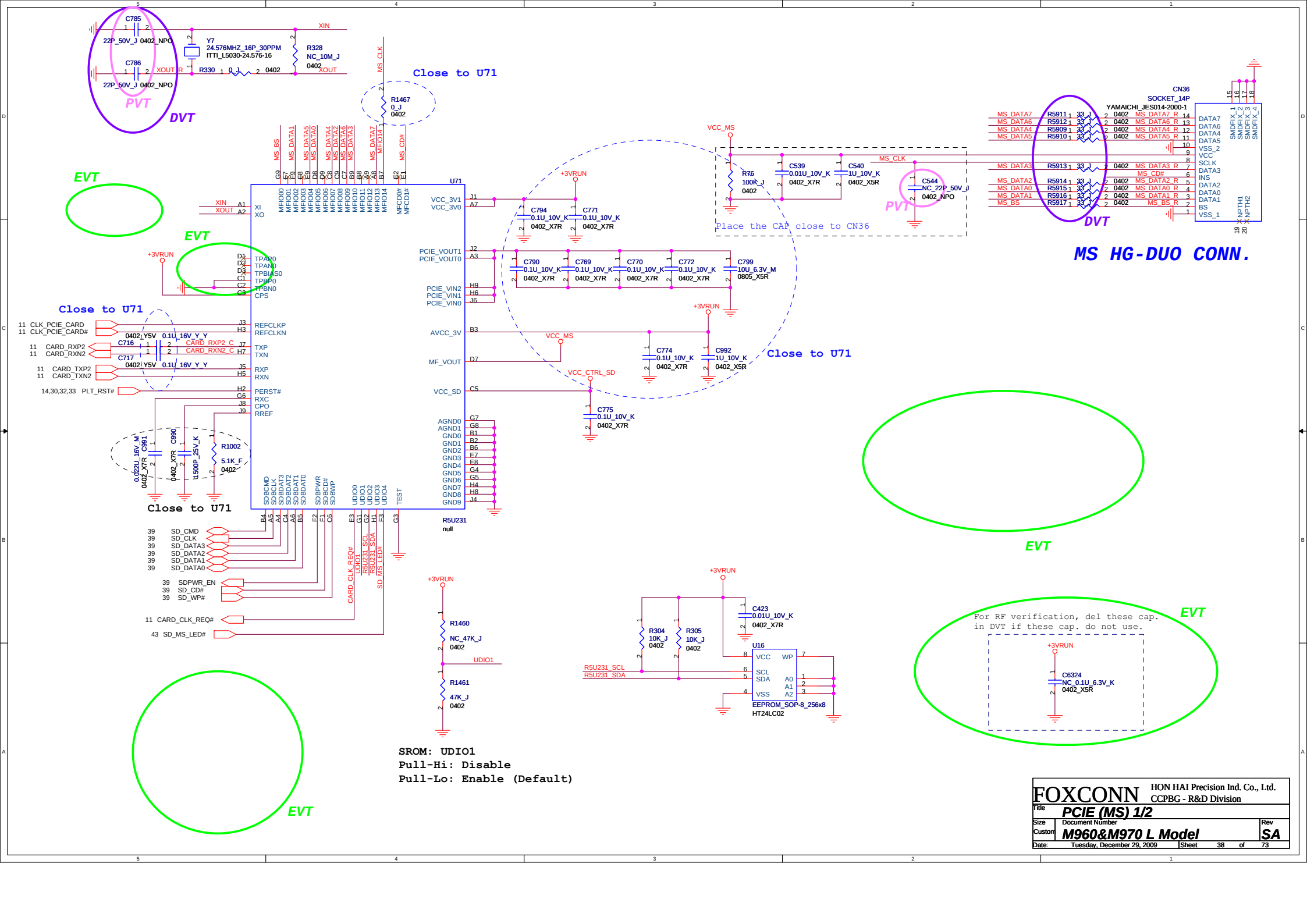
DVT

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: SATA ODD		
Size: A4	Document Number: M960&M970 L Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 36 of 73	



FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	eSATA Combo Conn.	
Size: Custom	Document Number: M960&M970 L Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 37 of 80	


C785
22P_50V_J 0402_NPO
C786
22P_50V_J 0402_NPO
Y7
24.576MHZ_16P_30PPM
ITTI_L5030-24.576-16
R330 0_J 0402
R328
NC_10M_J
0402
XIN
XOUT
PVT
DVT
Close to U71
R1467
0_J
0402
MS_CLK
EVT
U71
XIN
XOUT
XI
XO
+3VRUN
TPAP0
TPAN0
TPBIAS0
TPBP0
TPBN0
CPS
Close to U71
CLK_PCIE_CARD
CLK_PCIE_CARD#
REFCLKP
REFCLKN
C716
CARD_RXP2_C
CARD_RXN2_C
TXP
TXN
C717
CARD_TXP2
CARD_TXN2
RXP
RXN
PLT_RST#
PERST#
RXC
CPO
RREF
R1002
5.1K_F
0402
Close to U71
SD_CMD
SD_CLK
SD_DATA3
SD_DATA2
SD_DATA1
SD_DATA0
SDPWR_EN
SD_CD#
SD_WP#
CARD_CLK_REQ#
SD_MS_LED#
VCC_3V1
VCC_3V0
PCIE_VOUT1
PCIE_VOUT0
PCIE_VIN2
PCIE_VIN1
PCIE_VIN0
AVCC_3V
MF_VOUT
VCC_SD
AGND0
AGND1
GND0
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
R5U231
null
C794 0.1U_10V_K 0402_X7R
C771 0.1U_10V_K 0402_X7R
C790 0.1U_10V_K 0402_X7R
C769 0.1U_10V_K 0402_X7R
C770 0.1U_10V_K 0402_X7R
C772 0.1U_10V_K 0402_X7R
C799 10U_6.3V_M 0805_X5R
C774 0.1U_10V_K 0402_X7R
C992 1U_10V_K 0402_X5R
C775 0.1U_10V_K 0402_X7R
VCC_MS
VCC_CTRL_SD
Close to U71
VCC_MS
R76 100K_J 0402
C539 0.01U_10V_K 0402_X7R
C540 1U_10V_K 0402_X5R
C544 NC_22P_50V_J 0402_NPO
MS_CLK
PVT
Place the CAP close to CN36
CN36
SOCKET_14P
YAMAICHI_JES014-2000-1
MS_DATA7 R5911 33_J 0402 MS_DATA7_R
MS_DATA6 R5912 33_J 0402 MS_DATA6_R
MS_DATA4 R5909 33_J 0402 MS_DATA4_R
MS_DATA5 R5910 33_J 0402 MS_DATA5_R
MS_DATA3 R5913 33_J 0402 MS_DATA3_R
MS_DATA2 R5914 33_J 0402 MS_DATA2_R
MS_DATA0 R5915 33_J 0402 MS_DATA0_R
MS_DATA1 R5916 33_J 0402 MS_DATA1_R
MS_BS R5917 33_J 0402 MS_BS_R
MS_CD#
DVT
MS HG-DUO CONN.
EVT
EVT
For RF verification, del these cap.
in DVT if these cap. do not use.
+3VRUN
C6324
NC_0.1U_6.3V_K
0402_X5R
+3VRUN
R1460
NC_47K_J
0402
UDIO1
R1461
47K_J
0402
+3VRUN
R304 10K_J 0402
R305 10K_J 0402
C423 0.01U_10V_K 0402_X7R
U16
VCC
WP
SCL
SDA
A0
A1
A2
VSS
EEPROM_SOP-8_256x8
HT24LC02
R5U231_SCL
R5U231_SDA
SROM: UDIO1
Pull-Hi: Disable
Pull-Lo: Enable (Default)
EVT
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
PCIE (MS) 1/2
Size
Custom
Document Number
M960&M970 L Model
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Date: Tuesday, December 29, 2009
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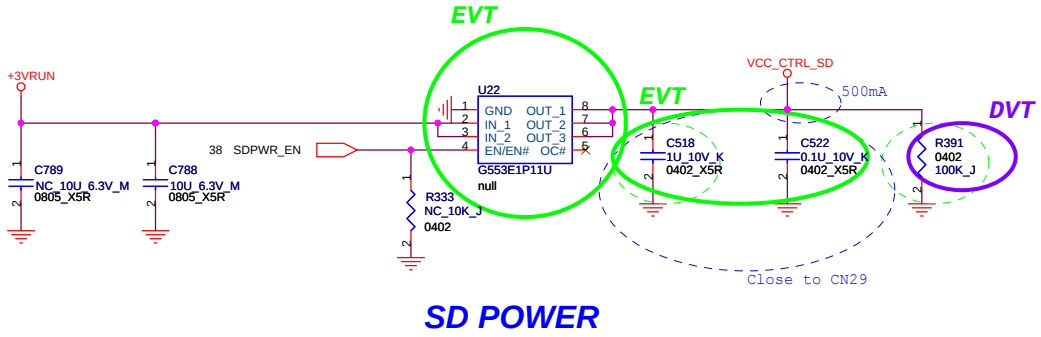
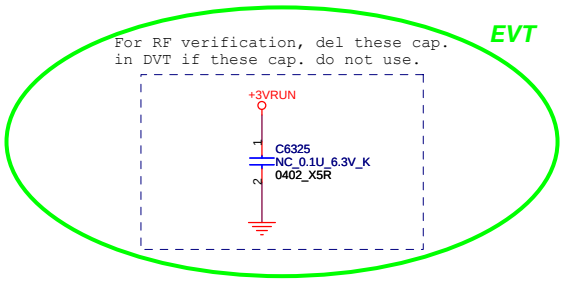
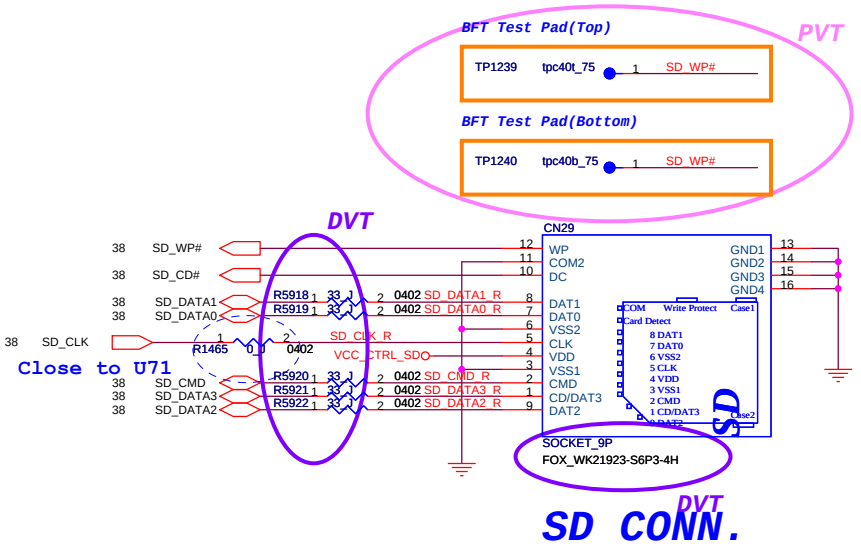
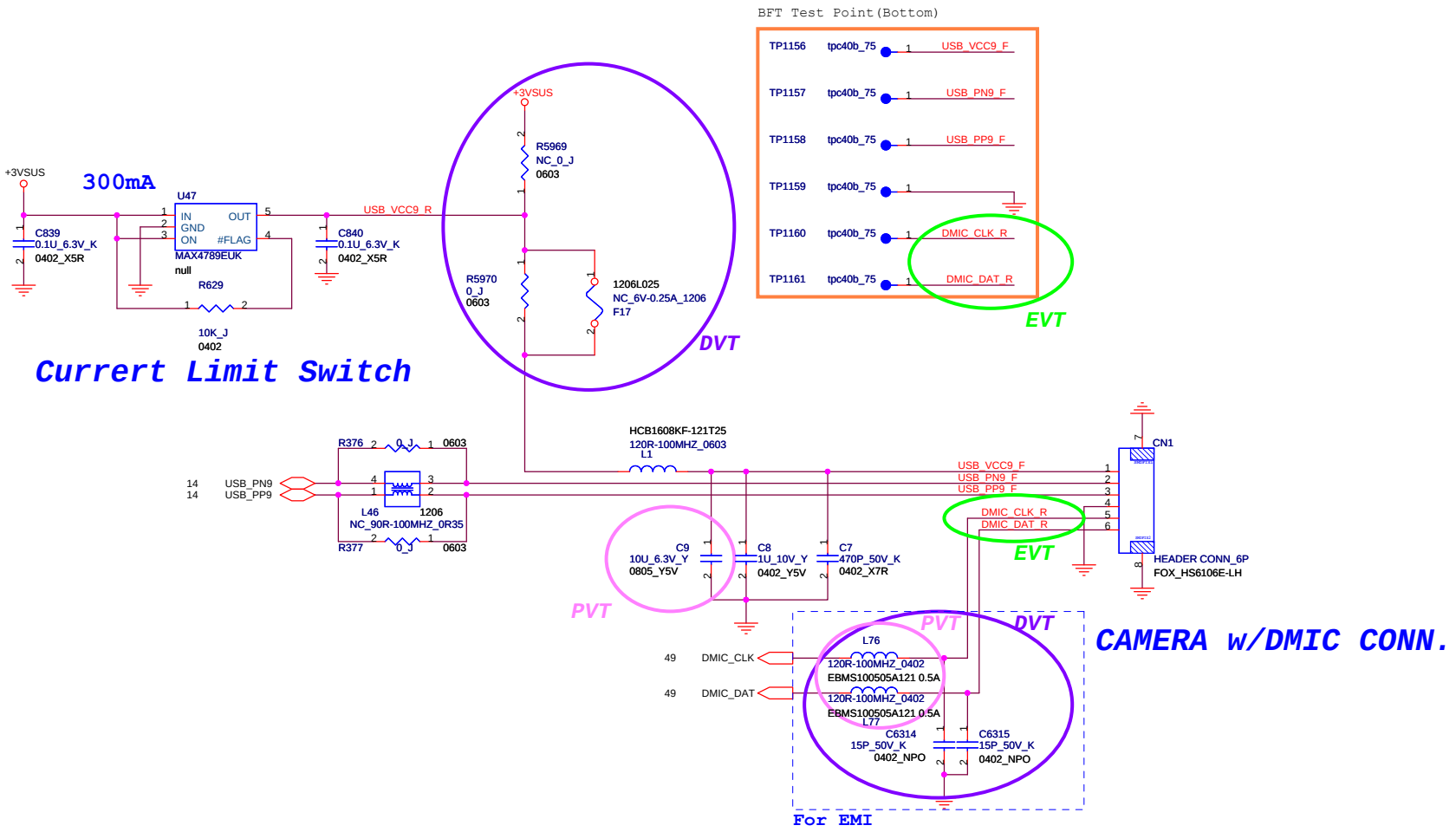


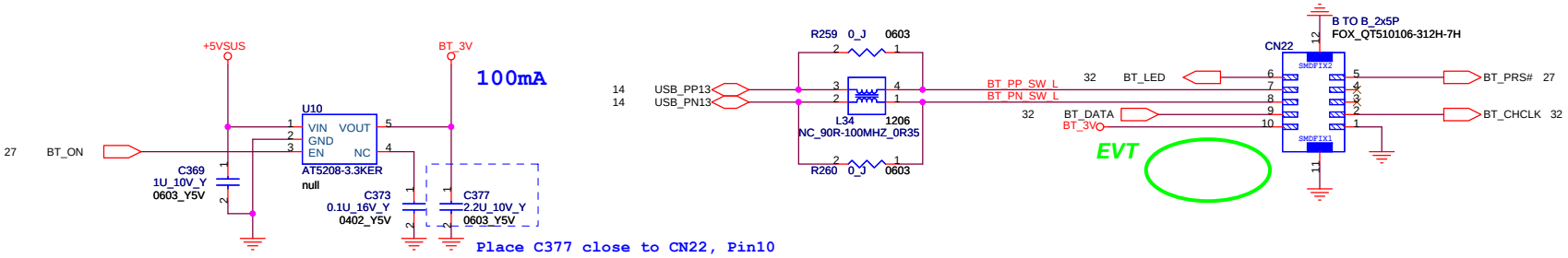




FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	PCIE (SD) 2/2	
Size: Custom	Document Number: M960&M970 L Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 39 of 73	

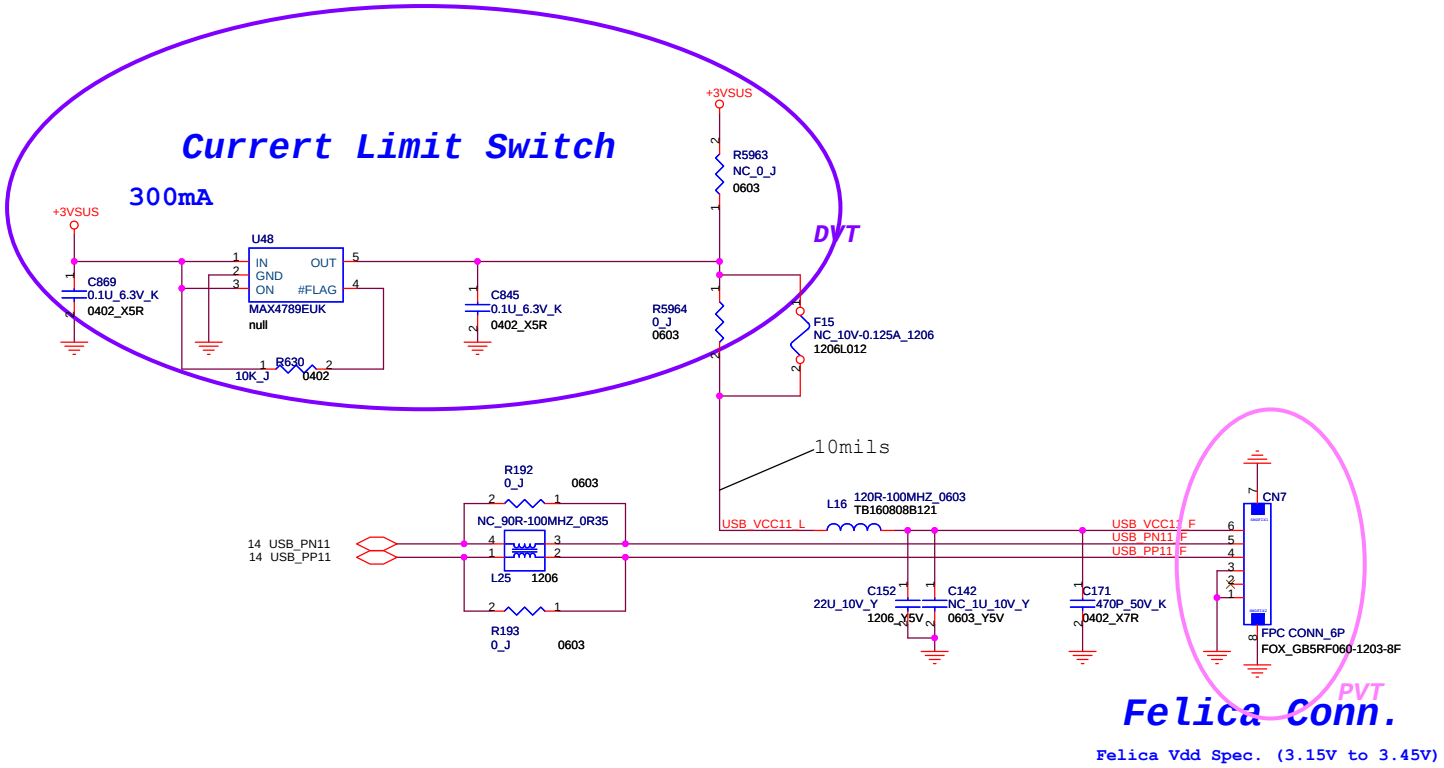


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Camera w/DMIC Connector	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 40 of 73	



Bluetooth CONN.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: Bluetooth Connector		
Size: Custom	Document Number: M960&M970 L Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 41 of 73	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Felica Connector	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 42 of 73	

Power Test Test Point (Top)
TP1227 tpc60t_100 1 WIRELESS_LED_TP

Power Test Test Point (Top)
TP1224 tpc60t_100 1 CHARGE_LED
TP1228 tpc60t_100 1 CHARGE_LED_TP

Power Test Test Point (Top)
TP1225 tpc60t_100 1 SATA_LED#
TP1229 tpc60t_100 1 SATA_LED#_TP

BFT Test Point (Top)
TP1226 tpc60b_100 1 SD_MS_LED#
TP1230 tpc60b_100 1 SD_MS_LED#_TP

PVT

WIRELESS LED

32 WIRELESS_LED
WIRELESS_LED
R689 300_J 0402
WIRELESS_LED_TP
LED1 LTST-S321KGKT null

BATT LED

+3VALW
R692 909_F 0402
CHARGE_LED_TP
LED2 LTST-S321KFKT null
27 CHARGE_LED
Q50 DTC114EUB null

DVT

HDD LED

+3VRUN
Q49 DTA114YUB null
10 SATA_LED#
R693 300_J 0402
SATA_LED#_TP
LED3 12-21-Y2C-AL2N1LY-2C null

LID Switch

+ECVCC
C477 0.1U_16V_Y 0402_Y5V
U21 EC2618NLB1GR null
VDD OUT GND
2 LIDIN#
LIDIN# 24,27

SD/MS LED

+3VRUN
Q75 DTA114YUB null
38 SD_MS_LED#
R919 300_J 0402
SD_MS_LED#_TP
LED4 12-21-Y2C-AL2N1LY-2C null

EVT

POWER LED
SUSPEND LED

+3VALW
R694 10K_J 0402
R695 1K_J 0402
Q51 CHT2301PT
27 POWER_LED
Q21 DTC114EUB null
R390 261_F 0402
47 PWR_LED 47

Q48 CHT2301PT
R691 1K_J 0402
R690 10K_J 0402
0402 120_J R384
47 SUS_LED
Q18 DTC114EUB null
SUSPEND_LED 27

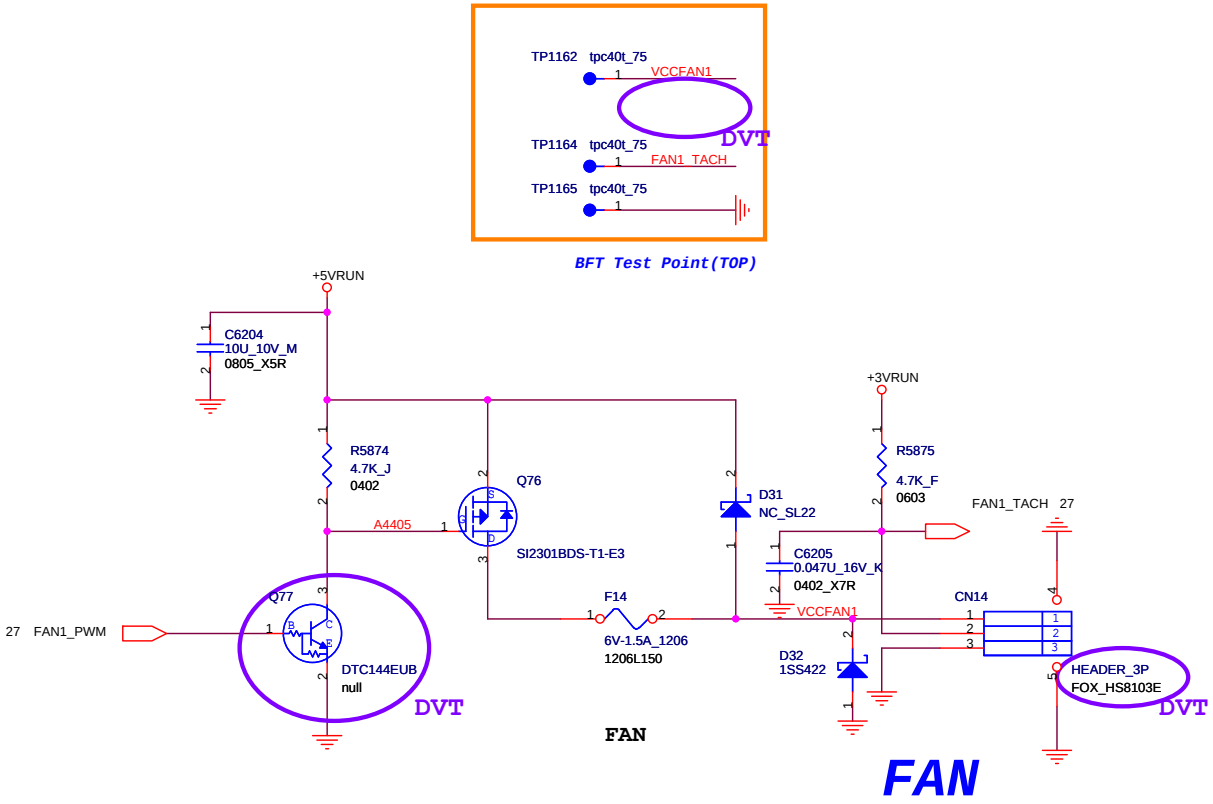
SCRLOCK / CAPLOCK / NUMLOCK

27 SCRLOCK_LED#
27 CAPLOCK_LED#
27 NUMLOCK_LED#
Q179 Q180 Q181 DTA114YUB null
R5946 R5947 R5945 649_F 0402
47 NUMLOCK_LED#_QR 47
47 CAPLOCK_LED#_QR 47
SCRLOCK_LED#_QR

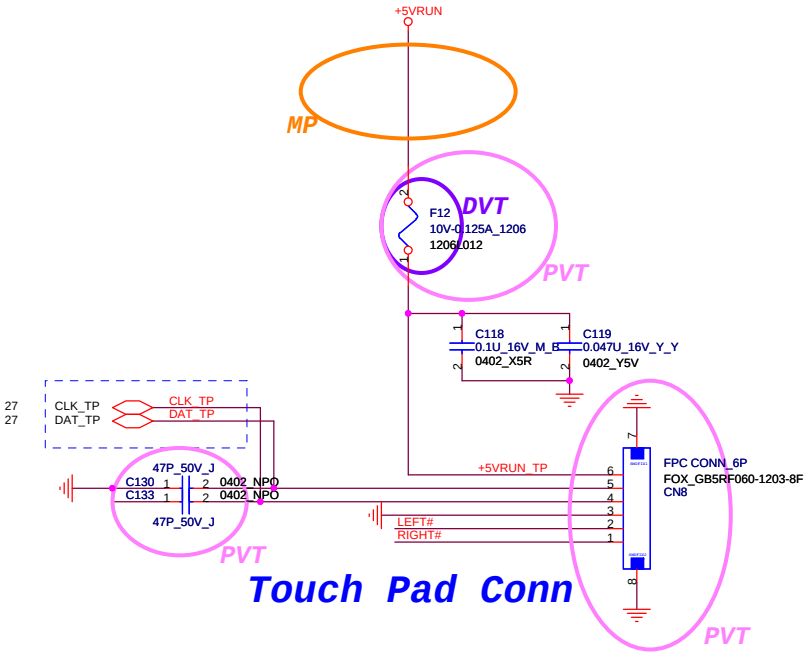
DVT

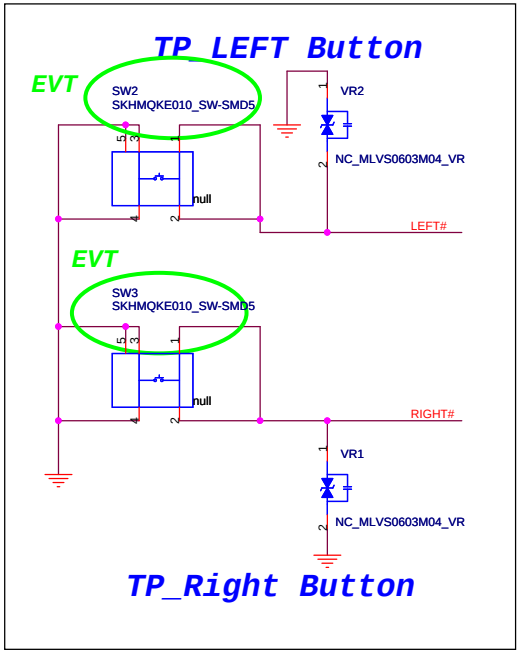
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title	Status LED & LID	
Size B	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 43 of 73	

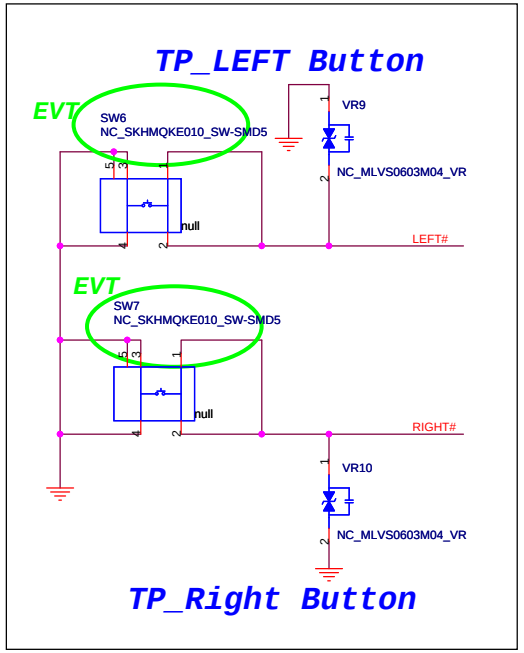


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: FAN		
Size: B	Document Number: M960&M970 L Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 44 of 73	





For M960 Only



For M970 Only

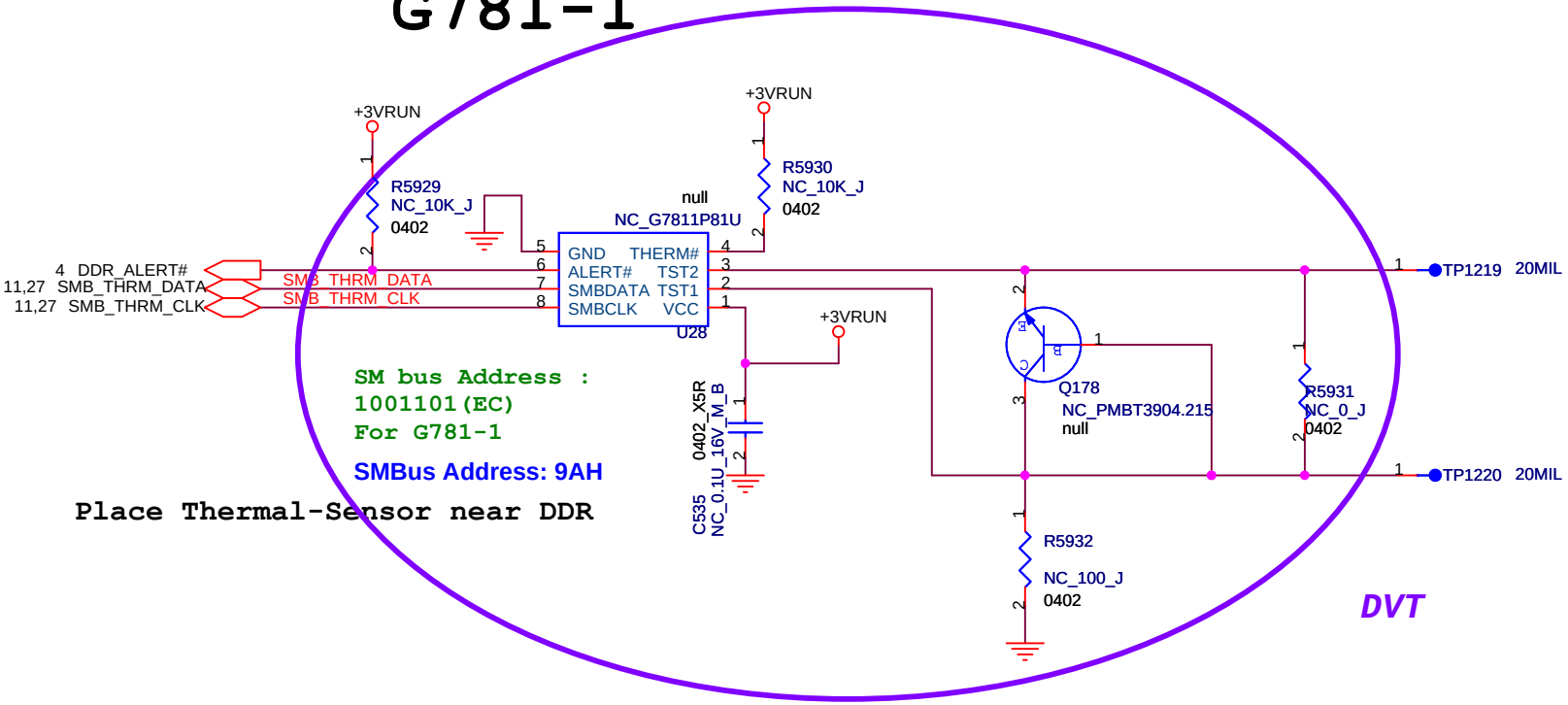
M960/M970 T/P Control Table

	SW2	SW3	SW6	SW7				
M960	Stuff	Stuff	Dummy	Dummy				
M970	Dummy	Dummy	Stuff	Stuff				

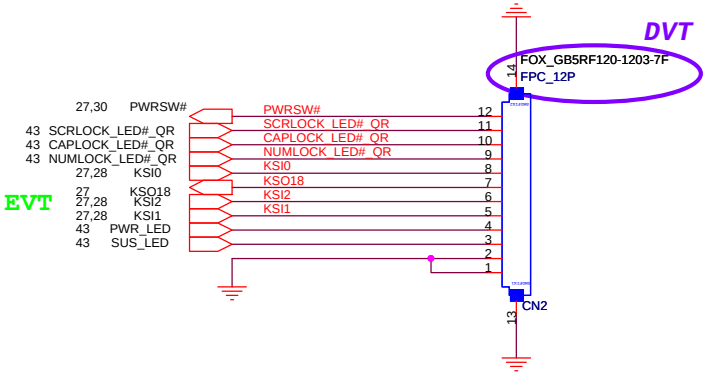
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

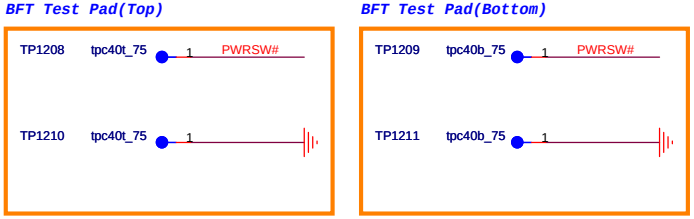
Title	Touch Pad	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 45 of 73	

DDR Thermal SENSOR
G781-1



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Thermal Sensor & Protection	
Size: A4	Document Number: M960&M970 L Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 46 of 73	





Switch DB Conn.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: SWITCH DB Connector		
Size: Custom	Document Number: M960&M970 L Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 47 of 73	

BFT Test Pad(Bottom)

TP1194	tpc40b_75	1	R_INT_SPK_R-
TP1195	tpc40b_75	1	R_INT_SPK_R+
TP1196	tpc40b_75	1	R_INT_SPK_L-
TP1197	tpc40b_75	1	R_INT_SPK_L+

INTERNAL SPEAKER

49 INT_SPK_R+ → INT_SPK_R+ → 220R-100MHZ_0603 L78 FCM1608KF-221T05 R_INT_SPK_R+
49 INT_SPK_R- → INT_SPK_R- → 220R-100MHZ_0603 L79 FCM1608KF-221T05 R_INT_SPK_R-
49 INT_SPK_L+ → INT_SPK_L+ → 220R-100MHZ_0603 L80 FCM1608KF-221T05 R_INT_SPK_L+
49 INT_SPK_L- → INT_SPK_L- → 220R-100MHZ_0603 L81 FCM1608KF-221T05 R_INT_SPK_L-

JSPK1 (SMDFIX1, SMDFIX2) — POWER CONN_4P FOX_HS6204E

DVT

For EMI

VR4 NC_MLVS0603M04_VR null
VR5 NC_MLVS0603M04_VR null
VR3 NC_MLVS0603M04_VR null
VR6 NC_MLVS0603M04_VR null

BFT Test Pad

If use ALC275 Codec, for Shut-down Codec Amp. power (PVDD1 and PVDD2)

PVT

C6350 1000P_50V_K 0402_X7R
R3 8.2K_J 0402
INT_SPK_L+
C3 10U_10V_M 0805_X5R
R370 22K_J 0402
Q25 PBSS2515E.115
Q2527_R
Q24 PBSS2515E.115
INT_SPK_L- R4 8.2K_J 0402
C6352 1000P_50V_K 0402_X7R

EVT

PVT

C6351 1000P_50V_K 0402_X7R
R2 8.2K_J 0402
INT_SPK_R+
C2 10U_10V_M 0805_X5R
R371 22K_J 0402
Q27 PBSS2515E.115
Q2527_R
Q26 PBSS2515E.115
INT_SPK_R- R1 8.2K_J 0402
C6353 1000P_50V_K 0402_X7R

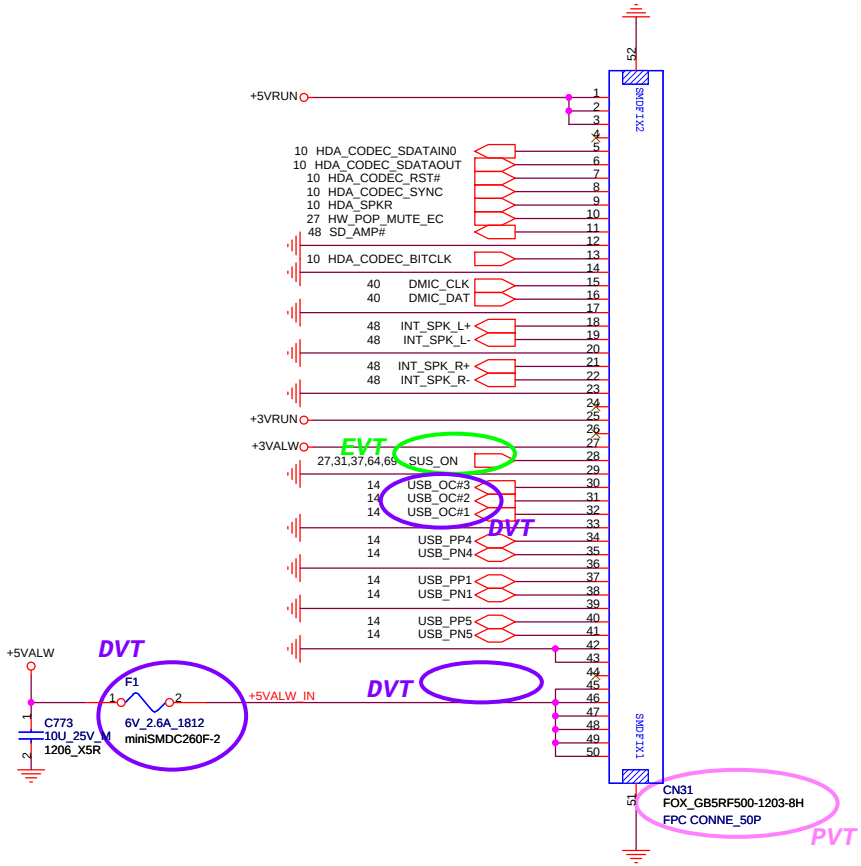
+5VRUN

R375 10K_J 0402
R374 10K_J 0402
Q29 PMBT3906.215 null
R708 NC_10K_J 0402
R380 10K_J 0402
Q54 NC_PBSS2515E.115
R833 NC_1K_J 0402

+12V
0402 100K_J R5774
49 SD_AMP#
DVT
PBSS2515E.115 Q31
R381 1K_J 0402

For Mor request,add the speaker cable short protection circuit

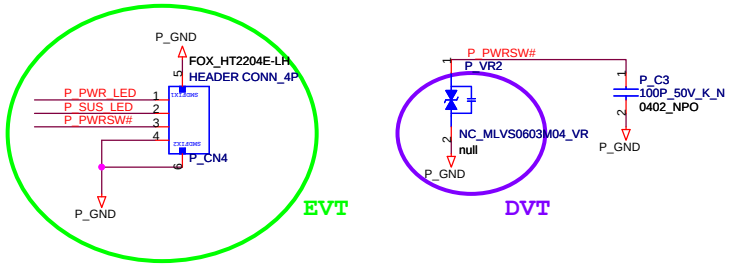
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO SPEAKER CONNECTOR	
Size B	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 48 of 73	

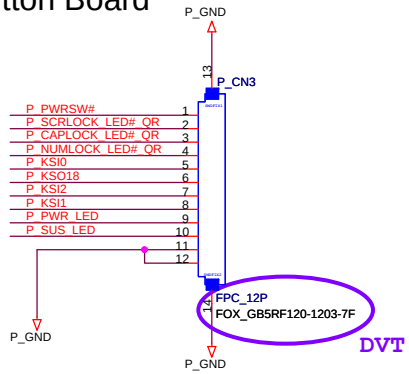


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO/USB DB Conn.	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 49 of 73	

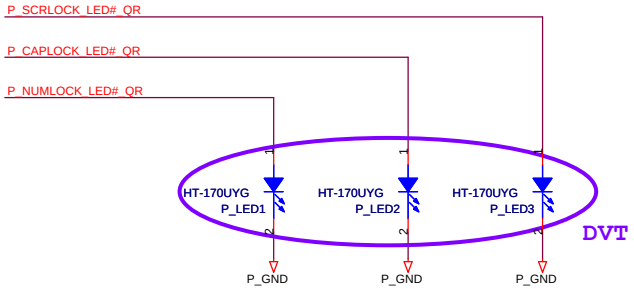
Power Button Board

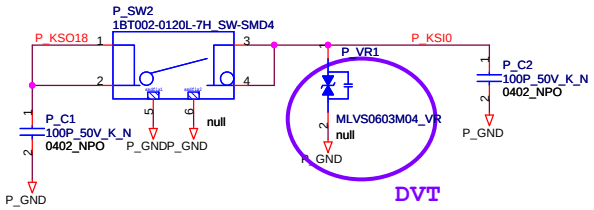
POWER BUTTON

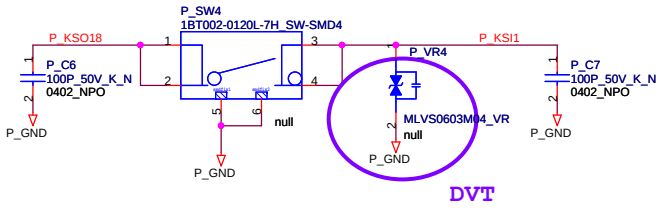


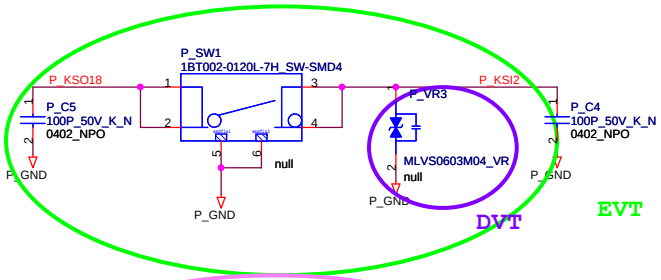


NUM LOCK LED CAP LED SCROLL LOCK LED









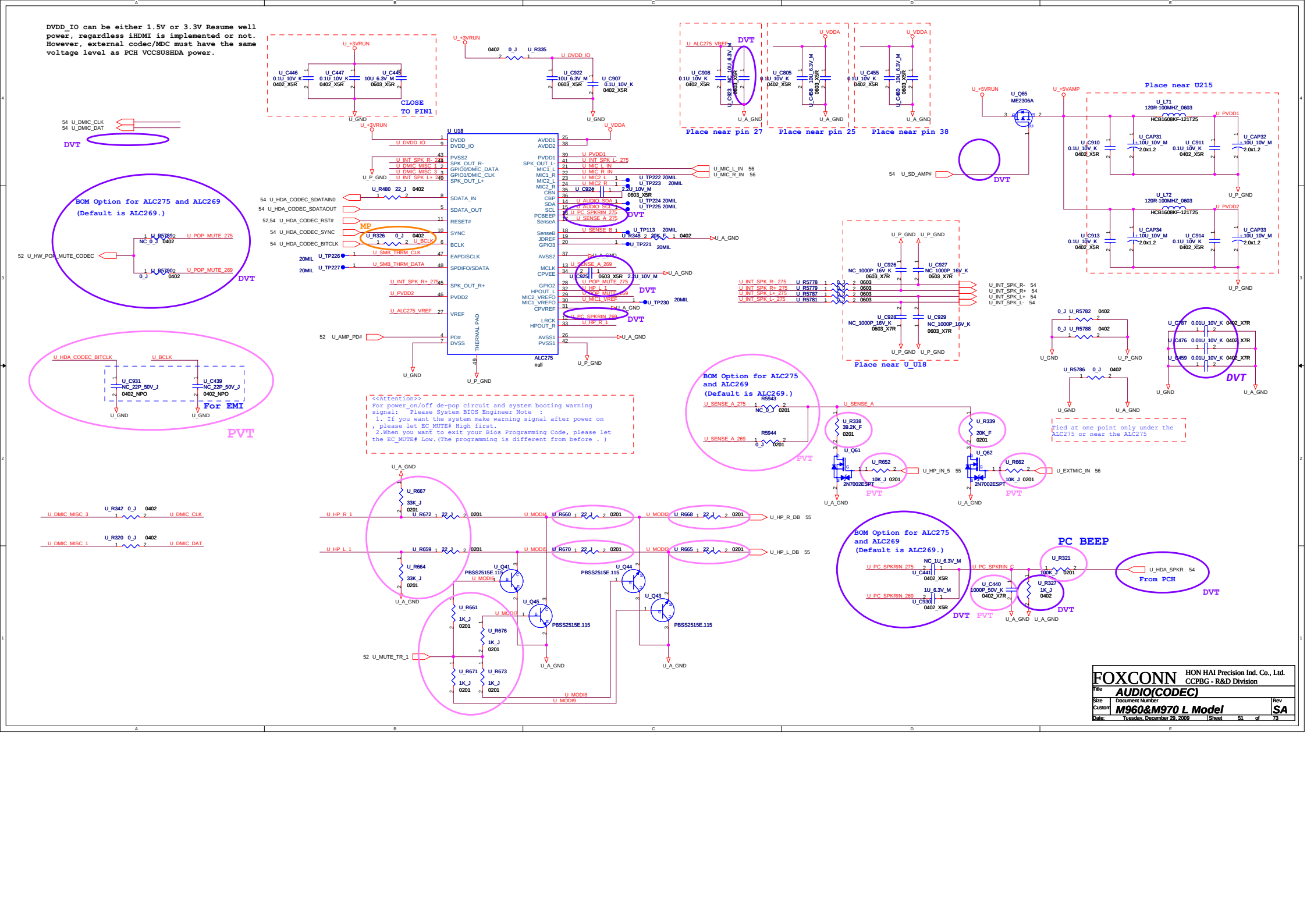
Assist EVT PVT

VAIO

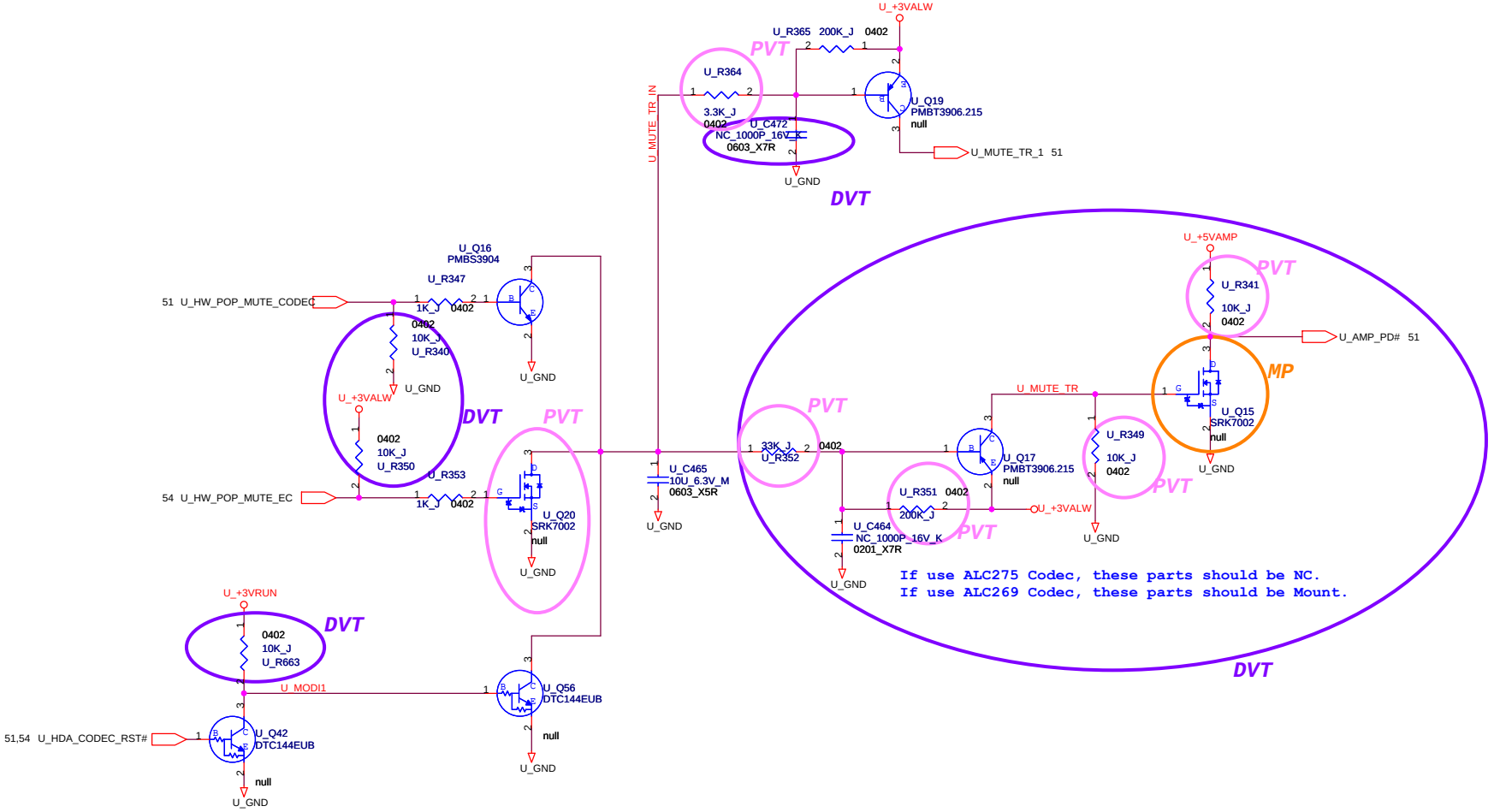
Web(Instant On) PVT

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SWITCH (BOTTON & KB LED)	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Thursday, December 24, 2009	Sheet 50 of 73	

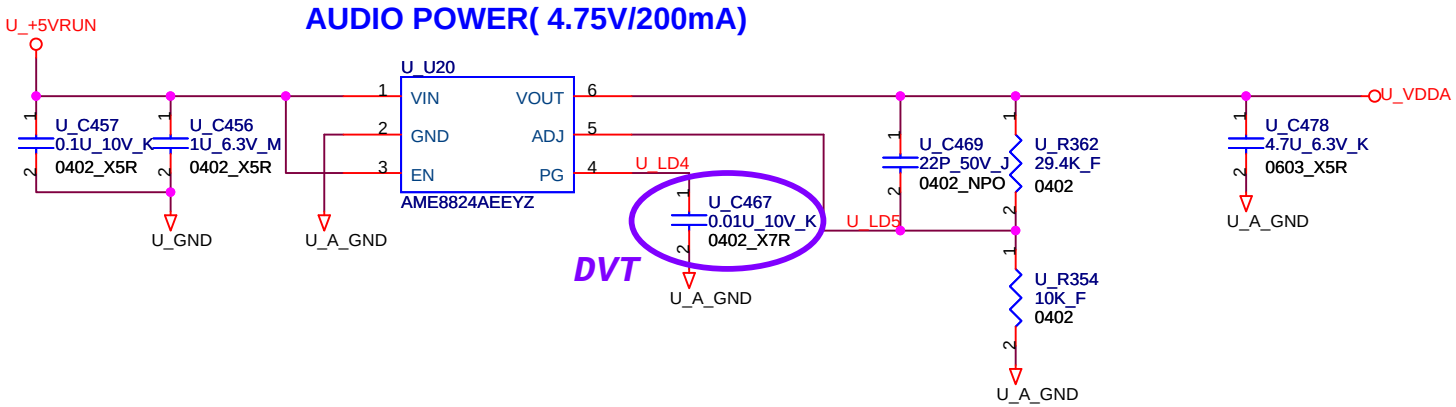
DVDD_IO can be either 1.5V or 3.3V Resume well power, regardless iHDMI is implemented or not. However, external codec/MDC must have the same voltage level as PCH VCCSUSHDA power.



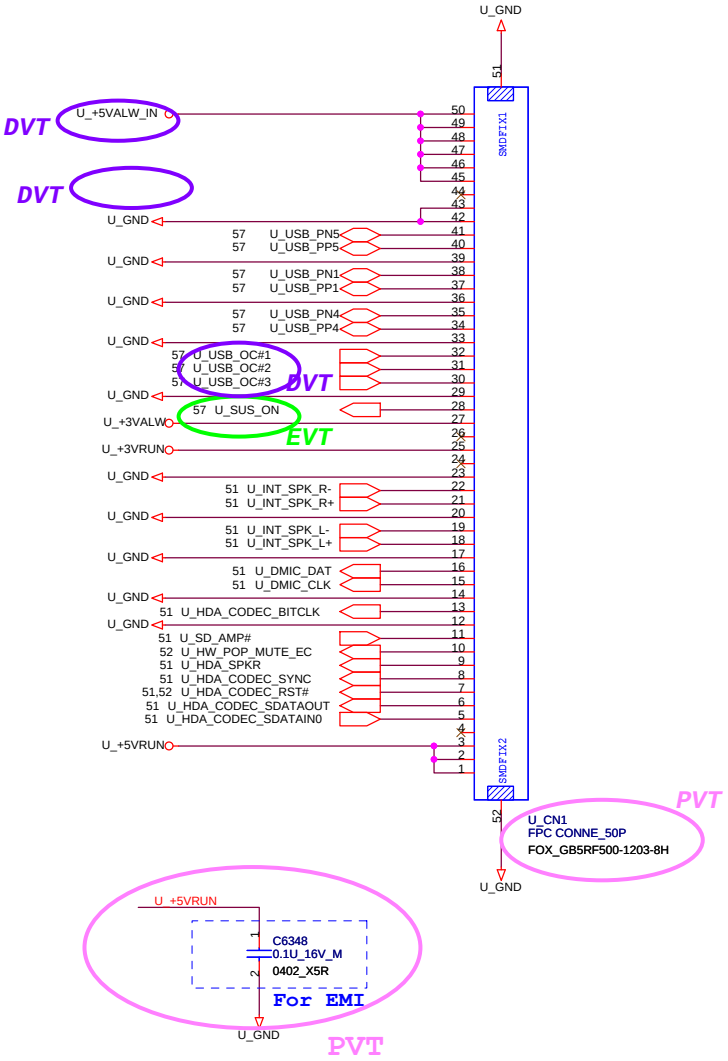
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO(CODEC)	
Size: Custom	Document Number: M960&M970 L Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 51 of 73	



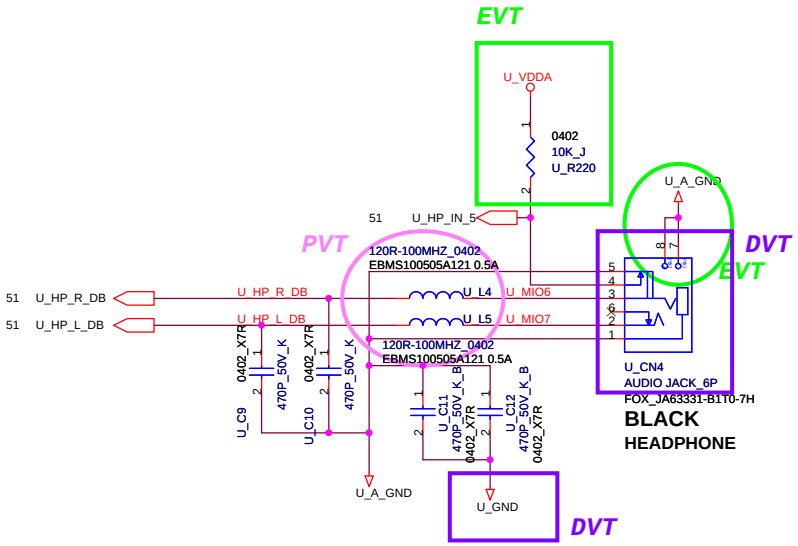
FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	AUDIO (MUTE)	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 52 of 73	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	**AUDIO POWER**	
Size A4	Document Number **M960&M970 L Model**	Rev **SA**
Date: Thursday, December 24, 2009	Sheet 53 of 73	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Audio (AUDIO & USB Conn)	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 54 of 73	



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	***Audio (Head Phone Jack)***	
Size A3	Document Number ***M960&M970 L Model***	Rev ***SA***
Date: Tuesday, December 29, 2009	Sheet 55 of 73	

EVT

EVT

DVT

U_R5791
U_MIC1_R_IN 1 0_J 2 0402 U_MIC_R_IN 51

DVT

U_R5792
U_MIC1_L_IN 1 0_J 2 0402 U_MIC_L_IN 51

EVT

U_VDDA
0402
10K_J
U_R222
U_EXTMIC_IN 51

U_A_GND
U_C19
470P_50V_K_B
0402_X7R

U_A_GND

DVT

U_R31 0_J 0603
U_MIC0_R_IN 1 2 U_MIO20
U_R33 0_J 0603
U_MIC0_L_IN 1 2 U_MIO21

U_C23
470P_50V_K_B
0402_X7R
U_A_GND

U_CN5
AUDIO_JACK_6P
FOX_JA63331-R110-7H

U_A_GND
EXTERNAL MIC
RED

U_VDDA
U_C506
0402_X5R
1U_6.3V_M
U_A_GND

DVT

U_VDDA
U_R40
2.2K_J
0402

U_VDD2
U_C34
10U_6.3V_M
0603_X5R
U_A_GND

U_R42
NC_47K_J
0402

EVT

U_C35
4.7U_10V_K
0805_X5R

U_R43
6.8K_J
0402

U_R41
2.2K_J
0402
U_A_GND

U_MIC1_R_IN 1 U_R44 100_F 0402 2 U_MIO35
U_MIO35 2 1 U_MIC0_R_IN
U_MIC1_L_IN 1 U_R45 100_F 0402 2 U_MIO36
U_MIO36 2 1 U_MIC0_L_IN

U_C36
4.7U_10V_K
0805_X5R

U_A_GND

U_C37
10U_6.3V_M
0603_X5R

U_R46
NC_47K_J
0402

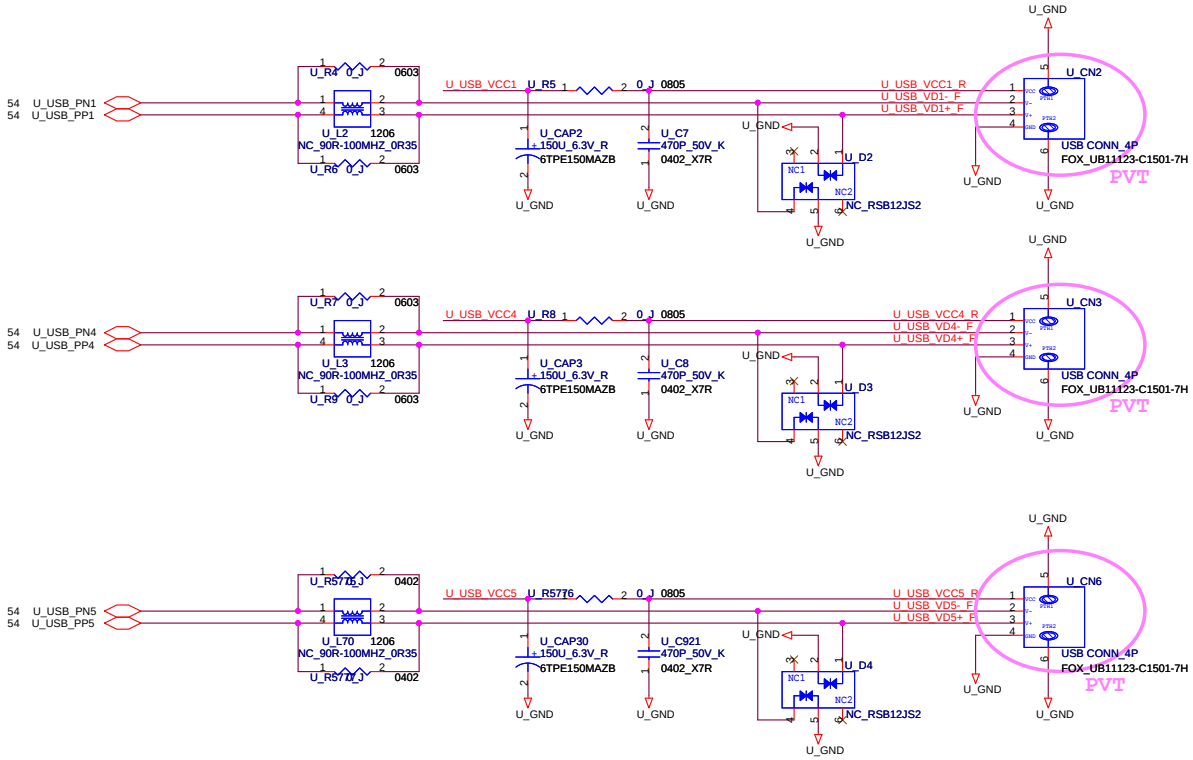
U_R47
6.8K_J
0402

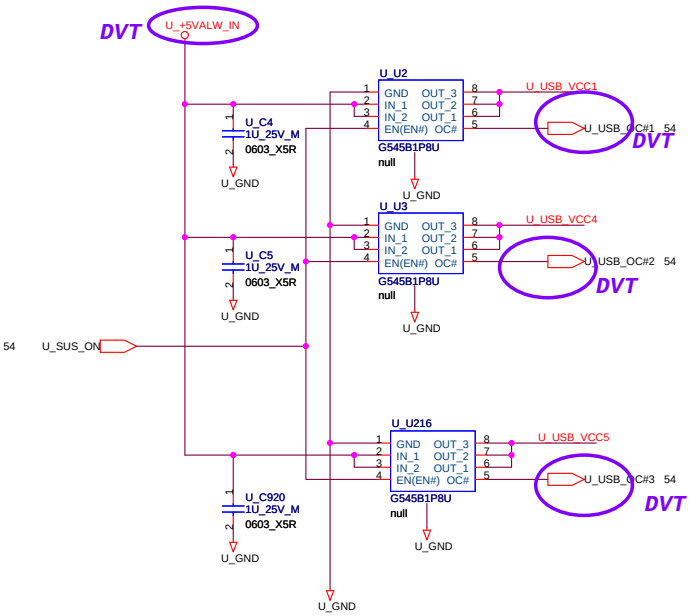
U_VDDA
U_R48
2.2K_J
0402

U_VDD3

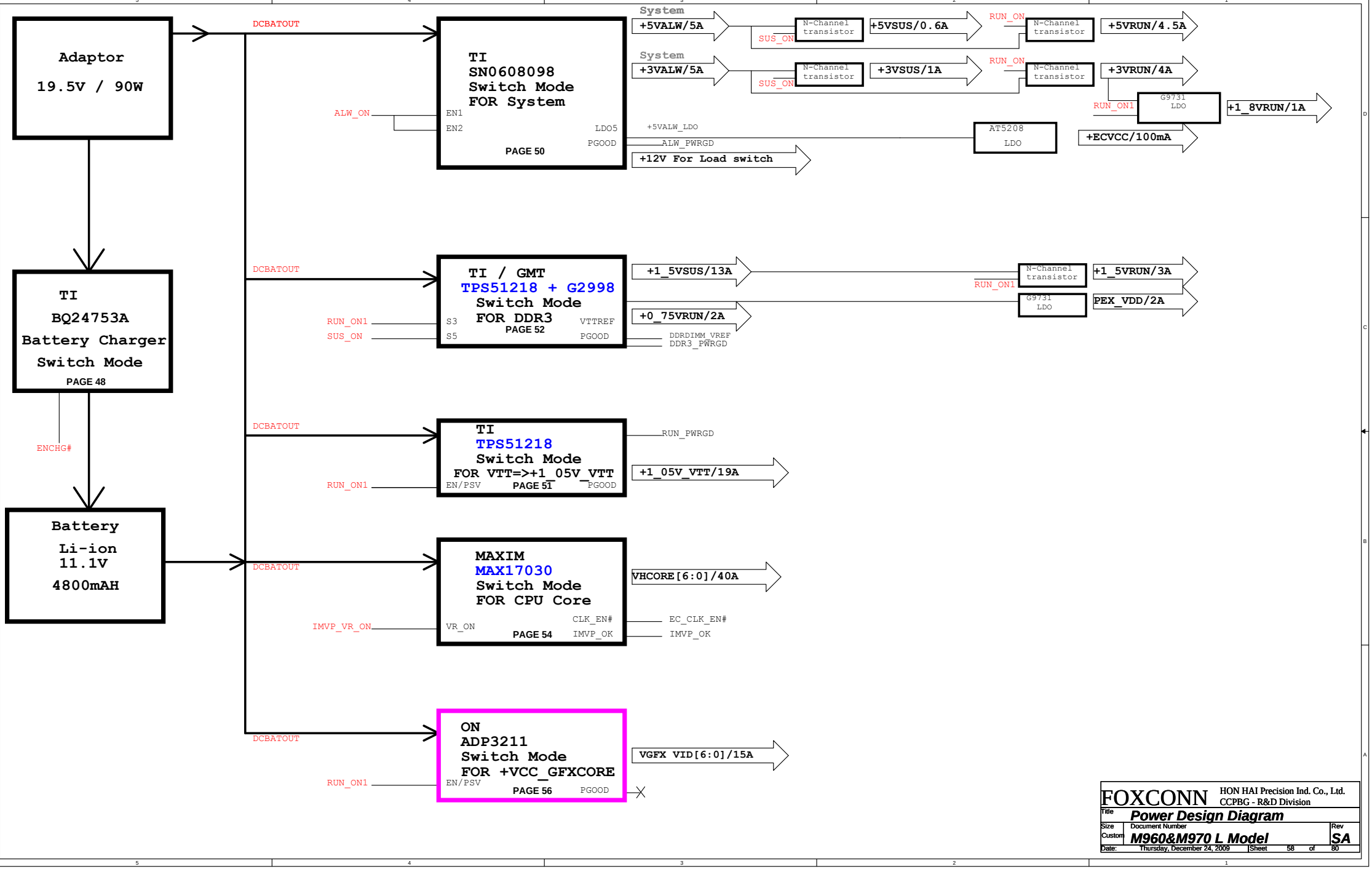
U_R49
2.2K_J
0402
U_A_GND

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Audio (Ext MIC Jack)	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 56 of 73	





FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: Audio (USB Port)		
Size: Custom	Document Number: M960&M970 L Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 57 of 73	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Power Design Diagram	
Size: Custom	Document Number: M960&M970 L Model	Rev: SA
Date: Thursday, December 24, 2009	Sheet 58 of 80	

ACP and ACN connections must be make using Kelvin-sense connections

09/11/21 Dcbatout Add PC574 0.1uf,PC575 0.1uf,PC576 4700pf ,PC577 4700pf for EMI request
BT+ add PC580 0.1uf,PC581 0.1uf,PC582 4700pf ,PC583 4700pf for EMI request

5A

10A

PVT

For EMI

PU3 BQ24753ARHDR

SRP and SRN connections must be make using Kelvin-sense connections

Charge Current Set Table:

Charge Current	CHARGE_CTRL Voltage setting	Battery Temperature
1.5A	3.06V	
800mA(Max)	1.6V	
350mA (Min)	0.72V	
0A	0V	T> 60 ℃ or T< 0 ℃

L --> 75W
H --> 64W

VREF=3.3V->VDAC
Vbat=cell count*[4V+0.512*(Vadj/Vvadc)]=12.465V
(Vbat=4.2V when Vadj connected to REGN)
Icharge=(Vsrset/Vvdac)*(0.1/PR15)=1.5A
Iadapter=(Vacset/Vvdac)*(0.1/PR657)=4.22A
IADAPT=(Vacp - Vacn)*20
Input OCP: (VACP-VACN)max/PR4=100mV/10mohm=10A
Input OVP : 22.2V
Input UVP : 17V
Battery OCP : Icharge*145%
Battery OVP : Vbat*104%
Pre-charge : <2.9V/cell ===> Icharge/8
Battery OTP : Tshut=155 degree
Fsw : 300KHz
Time that input current limit :
t=(Cacop*2)/(18uA/V*V(PVCC-ACP))=0.48s

ENCHG# : Enable ==> L
Disable ==> H

ACGOOD# : Vacdet > 2.4V ==> L
Vacdet < 2.4V ==> H

CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

	CP	DPPM	PWRLIMIT	Input OCP
90W	4.22A	4.22A/80.18W	4.52A/85.88W	10A

TABLE 1

DVT For CP	PQ16	PR220	PR79
	NO NC	45.3K	5.36K

TABLE 2

DVT	CP	DPPM	PWRLIMIT	Input OCP
H M/B(75W)	3.59A	3.59A/68.19W	3.76A/71.41W	9.46A
L M/B(64W)	3.06A	3.06A/58.19W	3.2A/60.82W	8.12A

TABLE 3

Battery CONN.

BFT Test Point (TOP)

BFT Test Point (Bottom)

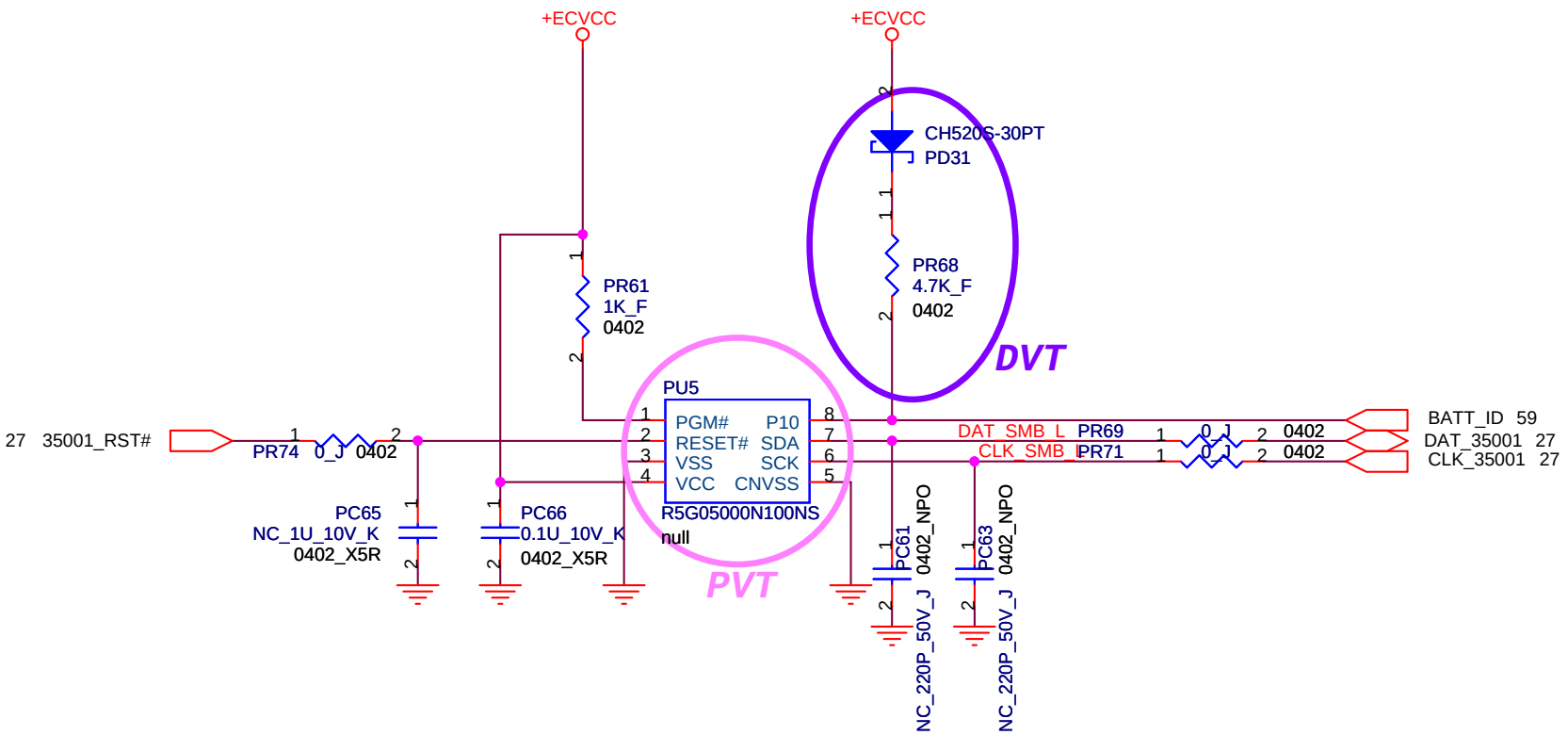
POWER BOARD SIDE_4P FOX_GS73041-10272-7H

FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

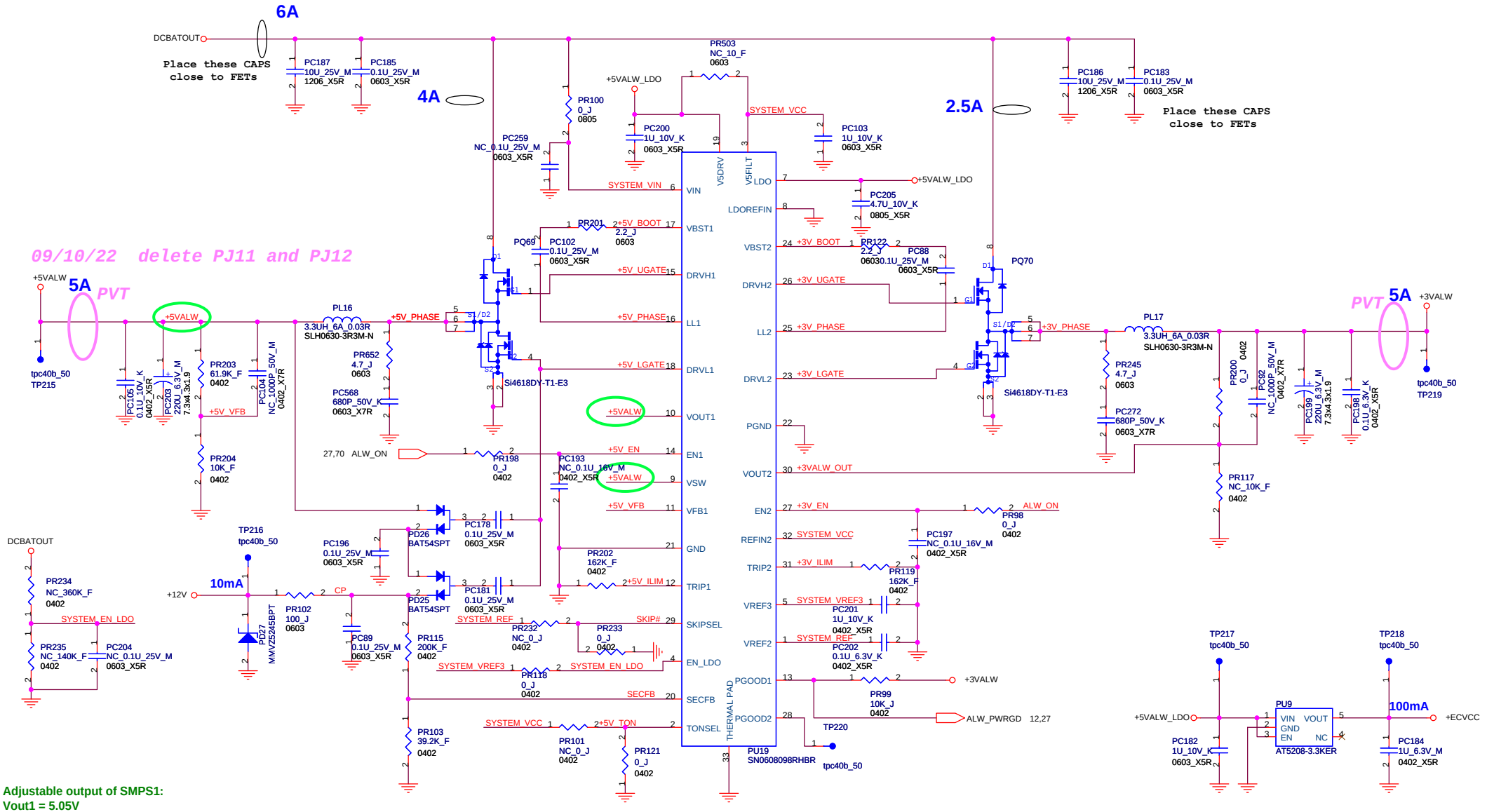
Title: DCIN&Charger
Size: Custom | Document Number: M960&M970 L Model | Rev: SA
Date: Tuesday, December 29, 2009 | Sheet 59 of 80

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title	**DISCHARGE CIRCUIT**
Size: A	Document Number: **M960&M970 L Model**
Rev: **SA**	
Date: Thursday, December 24, 2009	Sheet 60 of 80

9/8 Add PD31 and change PR68 to 4.7K for MOR request.



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	***Identify IC***	
Size A	Document Number ***M960&M970 L Model***	Rev ***SA***
Date: Tuesday, December 29, 2009	Sheet 61 of 80	



Adjustable output of SMPS1:
Vout1 = 5.05V
PR204 = 10K, PR203 = P204 x (Vout1 / 0.7V - 1) =61.9Kohm

Second Feedback :
Vout_sec = 12V, PR103 = 20Kohm
PR115 = PR103 x (Vout_sec / 2V - 1) =100Kohm

TON	Operating Frequence (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF(OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

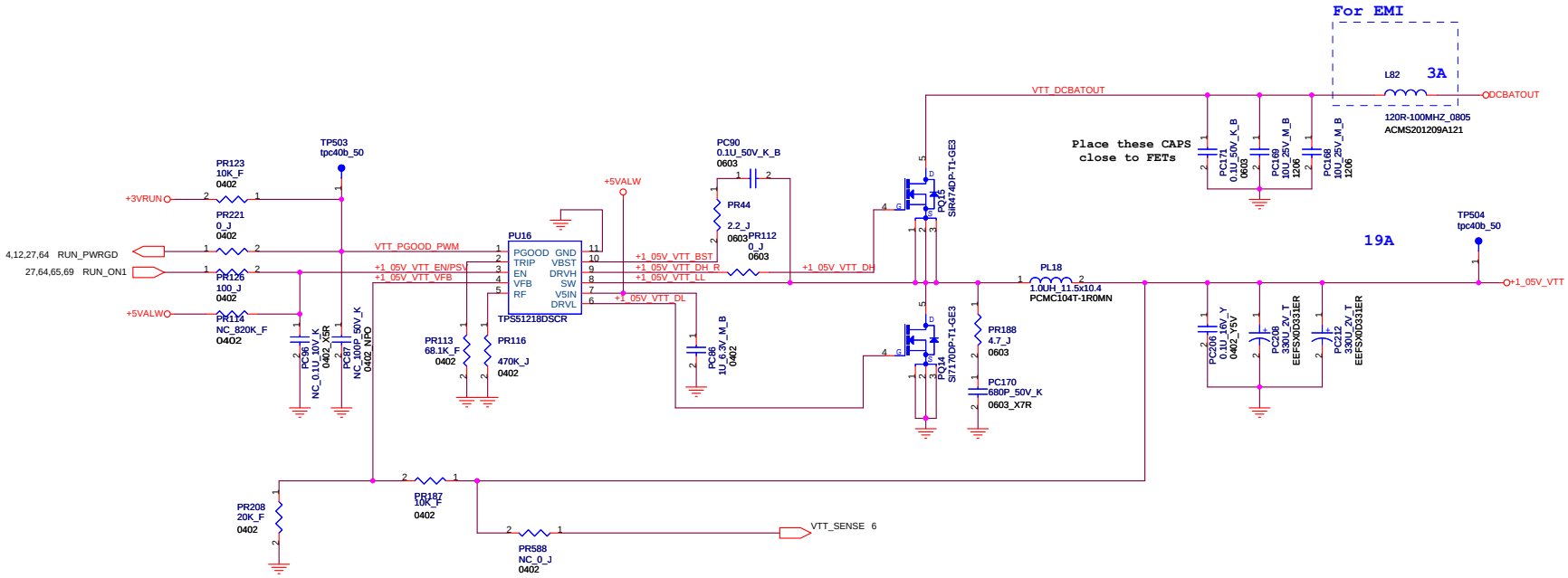
L=VOUT(VIN-VOUT)/(VIN*f*LIR*ILOAD(MAX))
Rocp=(Iocp-Iripple/2)*(10*Rds(on))/5u
+5VALW=((PR186/PR188)+1)*VFB1

Current limit resistor for SMPS1 :
Ivalley_5 = 5.775A, Rcs_5 = Rds1 = 10.8mohm
PR202 = (10 x Ivalley_5 x Rcs_5) / 5uA = 162K

Current limit resistor for SMPS2 :
Ivalley_3 = 5.525A, Rcs_3 = Rds2 = 10.8mohm
PR119 = (10 x Ivalley_3 x Rcs_3) / 5uA = 162K

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

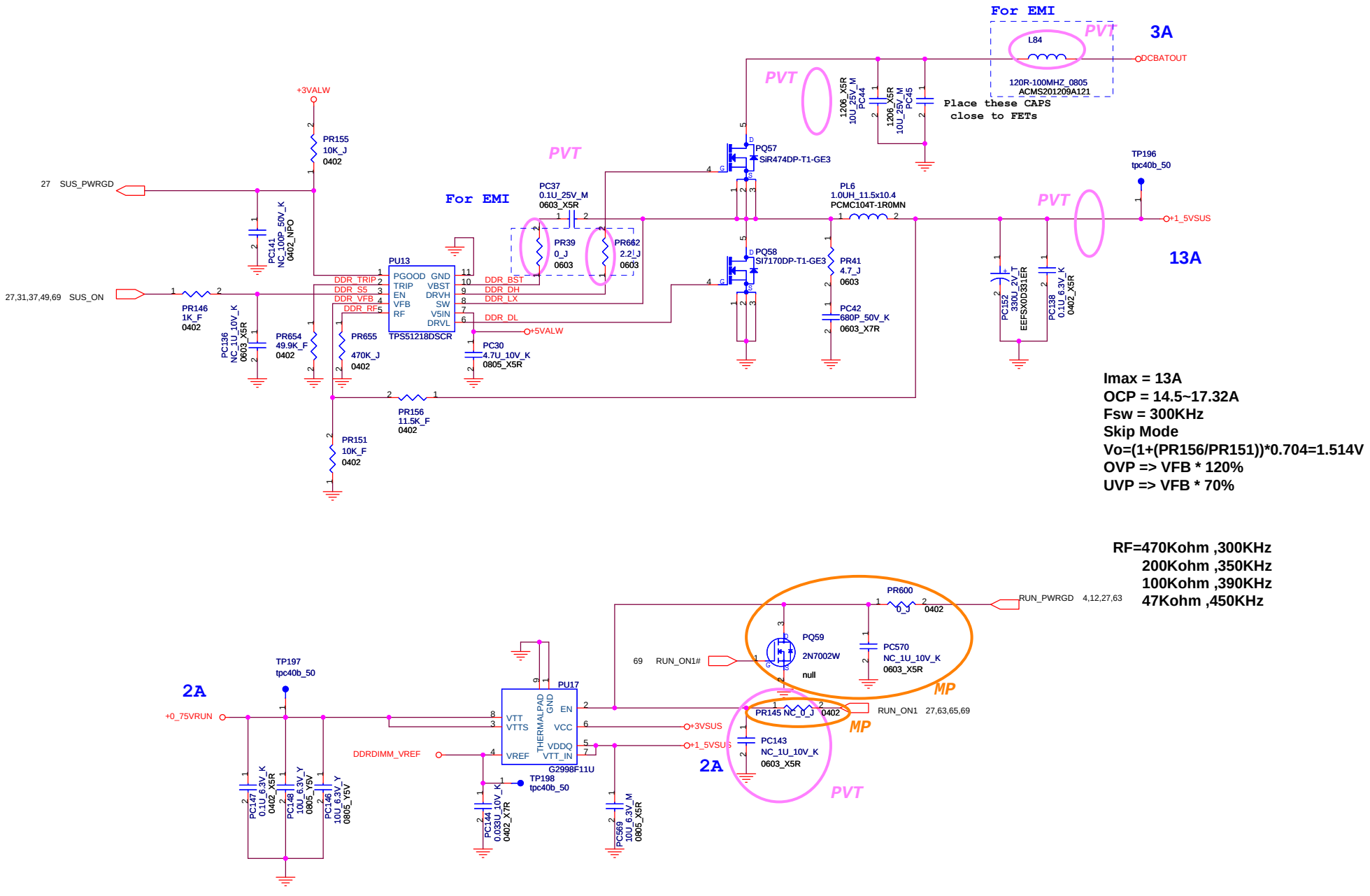
Title	SYS Power (+3_3V/+5V)	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 62 of 80	



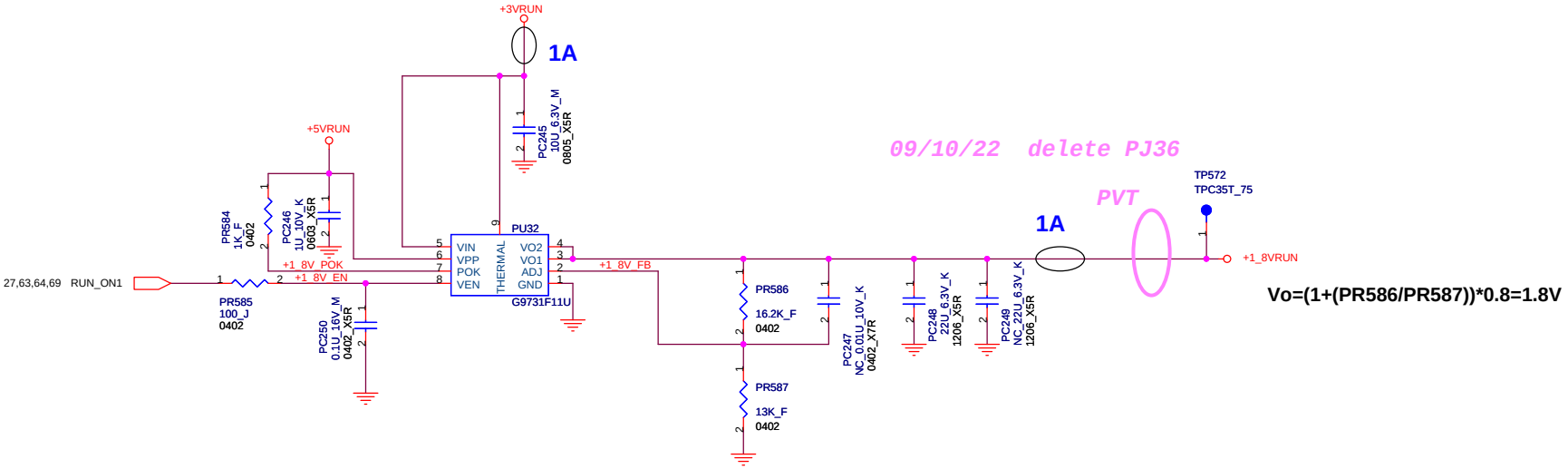
Imax = 19A
Fsw = 390KHz
Skip Mode
Vo=(1+(PR187/PR208))*0.704=1.05V
OVP => VFB * 120%
UVP => VFB * 70%

RF=470Kohm ,300KHz
200Kohm ,350KHz
100Kohm ,390KHz
47Kohm ,450KHz

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SYS Power(+1_05V_VTT)	
Size: Custom	Document Number: M960&M970 L Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 63 of 80	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDR3 Power(+1_5V/+0_75V)	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 64 of 80	



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	SYS Power(+1_8V)	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 65 of 80	

09/11/21 change PC151 and PC156 from NC to no NC for EMI request

Placement TOP and BOTTOM Overlapped

Place these CAPS close to FETs

4A

DCBATOUT

PC112 47U_25V_6.3x5.9 25SVPF47M

PVT For EMI

PU28

MAX17030GTL+

PQ40 SIR428DP-T1-GE3

PQ38 SIR158DP-T1-GE3

PL8 0.36UH_28A_0.00076R ETQP4LR36AFC

PQ36 SIR428DP-T1-GE3

PQ37 SIR158DP-T1-GE3

PL5 0.36UH_28A_0.00076R ETQP4LR36AFC

TP507 tpc40b_50

40A

VHCORE

TP223 tpc40b_50

TP224 tpc40b_50

Valley current limit:
V_TIME_LIM = 0.2 x PR561 / (PR560 + PR561) = 22.54mV
I_LIM = V_TIME_LIM / Rcs = 21.26A

Rcs:
DCR = 0.76mohm
Rcs = DCR x (PR557 + PR185) / (PR557 + PR185 + PR555) = 0.6061mohm

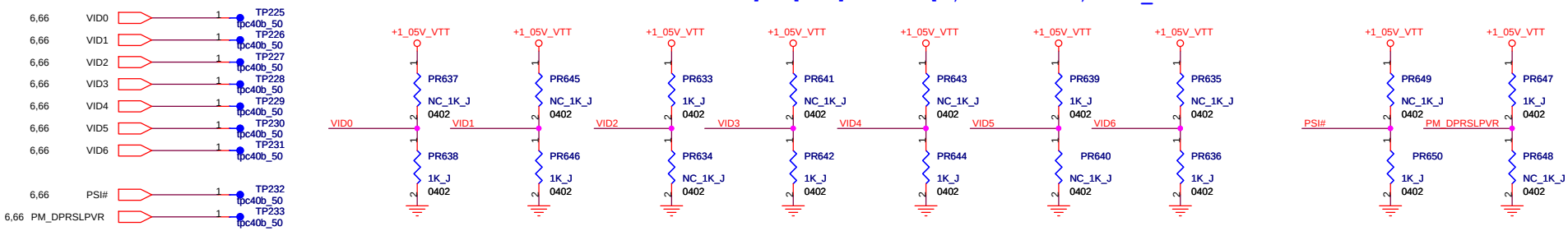
Load-Line R_FBAC: Loadl-Line=-1.9mV/A
Rcs = 0.709mohm
PR598 = (1.9mV/A) / (Rcs x 400us) = 6.34K

Sense line are 18mil wide
Zo=27.4ohm

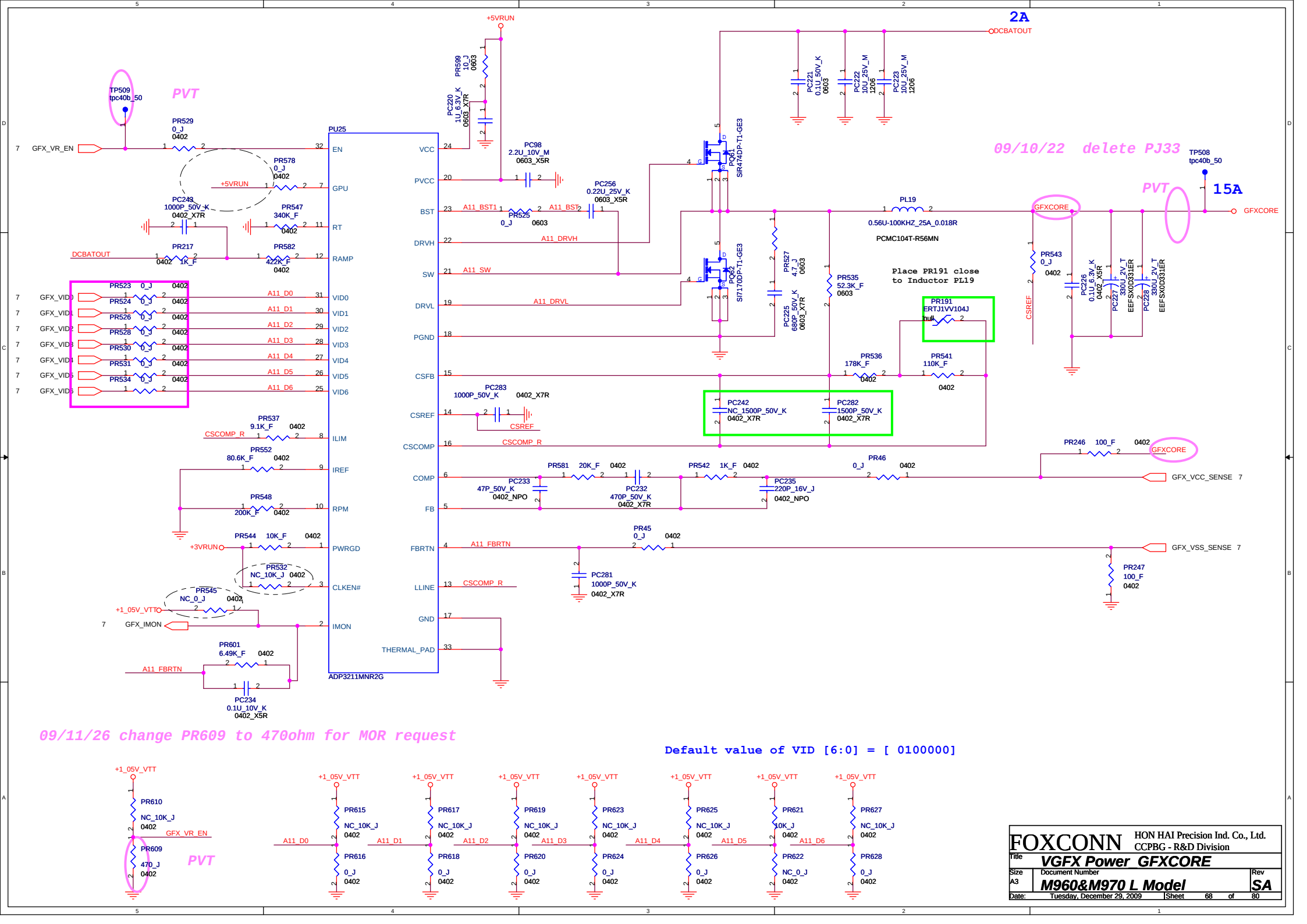
09/11/13 change pc253 from 1000P_16V_0402_X7R to 1000pF_50V_0402_X7R for MOR request

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	CPU Power VHCORE		
Size A3	Document Number M960&M970 L Model		Rev SA
Date: Tuesday, December 29, 2009	Sheet 66 of 80		

Default value of VID [6:0] = [0100100] , PSI = 0 , PROC_DPRSLPVR = 1



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: CPU Power VID		
Size: A3	Document Number: M960&M970 L Model	Rev: SA
Date: Tuesday, December 29, 2009	Sheet 67 of 80	


2A
DCBATOUT
+5VRUN
TP509
tpc40b_50
PVT
PR529
0_J
0402
GFX_VR_EN
PU25
EN
GPU
RT
RAMP
VID0
VID1
VID2
VID3
VID4
VID5
VID6
ILIM
IREF
RPM
PWRGD
CLKEN#
IMON
VCC
PVCC
BST
DRVH
SW
DRVL
PGND
CSFB
CSREF
CSCOMP
COMP
FB
FBRTN
LLINE
GND
THERMAL_PAD
ADP3211MNR2G
PR578
340K_F
PR547
PR217
1K_F
PR582
422K_F
PC243
1000P_50V_K
0402_X7R
PR523
PR524
PR526
PR528
PR530
PR531
PR534
A11_D0
A11_D1
A11_D2
A11_D3
A11_D4
A11_D5
A11_D6
PR537
9.1K_F
CSCOMP_R
PR552
80.6K_F
PR548
200K_F
PR544
10K_F
+3VRUN
PR532
NC_10K_J
PR545
NC_0_J
+1_05V_VTT
GFX_IMON
PR601
6.49K_F
A11_FBRTN
PC234
0.1U_10V_K
0402_X5R
PR599
10_J
0603
PC220
1U_6.3V_K
0603_X7R
PC98
2.2U_10V_M
0603_X5R
PC256
0.22U_25V_K
0603_X5R
A11_BST1
PR525
0_J
0603
A11_BST
A11_DRVH
A11_SW
A11_DRVL
PC283
1000P_50V_K
0402_X7R
CSREF
CSCOMP_R
PR581
20K_F
PC233
47P_50V_K
0402_NPO
PC232
470P_50V_K
0402_X7R
PR542
1K_F
PC235
220P_16V_J
0402_NPO
PR45
0_J
PC281
1000P_50V_K
0402_X7R
PC221
0.1U_50V_K
0603
PC222
10U_25V_M
1206
PC223
10U_25V_M
1206
Q24
SIR474DP-T1-GE3
Q25
SI7170DP-T1-GE3
PR527
4.7_J
0603
PC225
680P_50V_K
0603_X7R
PR535
52.3K_F
0603
PL19
0.56U-100KHZ_25A_0.018R
PCMC104T-R56MN
Place PR191 close
to Inductor PL19
PR191
ERTJ1VV104J
null
PR536
178K_F
PR541
110K_F
PC242
NC_1500P_50V_K
0402_X7R
PC282
1500P_50V_K
0402_X7R
09/10/22 delete PJ33
TP508
tpc40b_50
15A
GFXCORE
PR543
0_J
PC226
0.1U_6.3V_K
0402_X5R
PC227
330U_2V_T
EEFSX0D331ER
PC228
330U_2V_T
EEFSX0D331ER
CSREF
PR246
100_F
PR46
0_J
GFX_VCC_SENSE
GFX_VSS_SENSE
PR247
100_F
09/11/26 change PR609 to 470ohm for MOR request
Default value of VID [6:0] = [0100000]
PR610
NC_10K_J
PR609
470_J
PR615
PR616
PR617
PR618
PR619
PR620
PR623
PR624
PR625
PR626
PR621
PR622
PR627
PR628
0_J
FOXCONN
HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division
Title
VGFX Power GFXCORE
Size
A3
Document Number
M960&M970 L Model
Rev
SA
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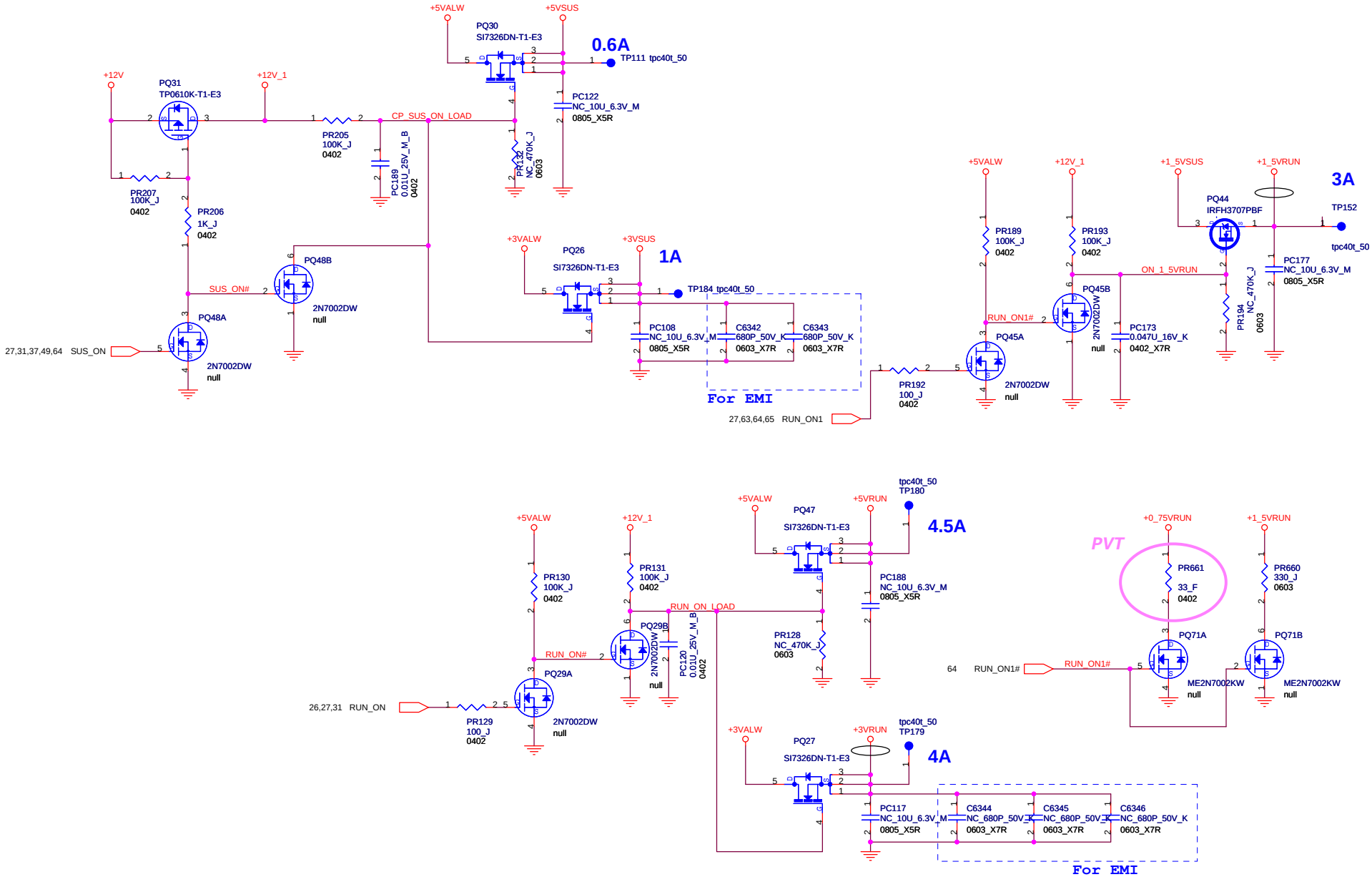
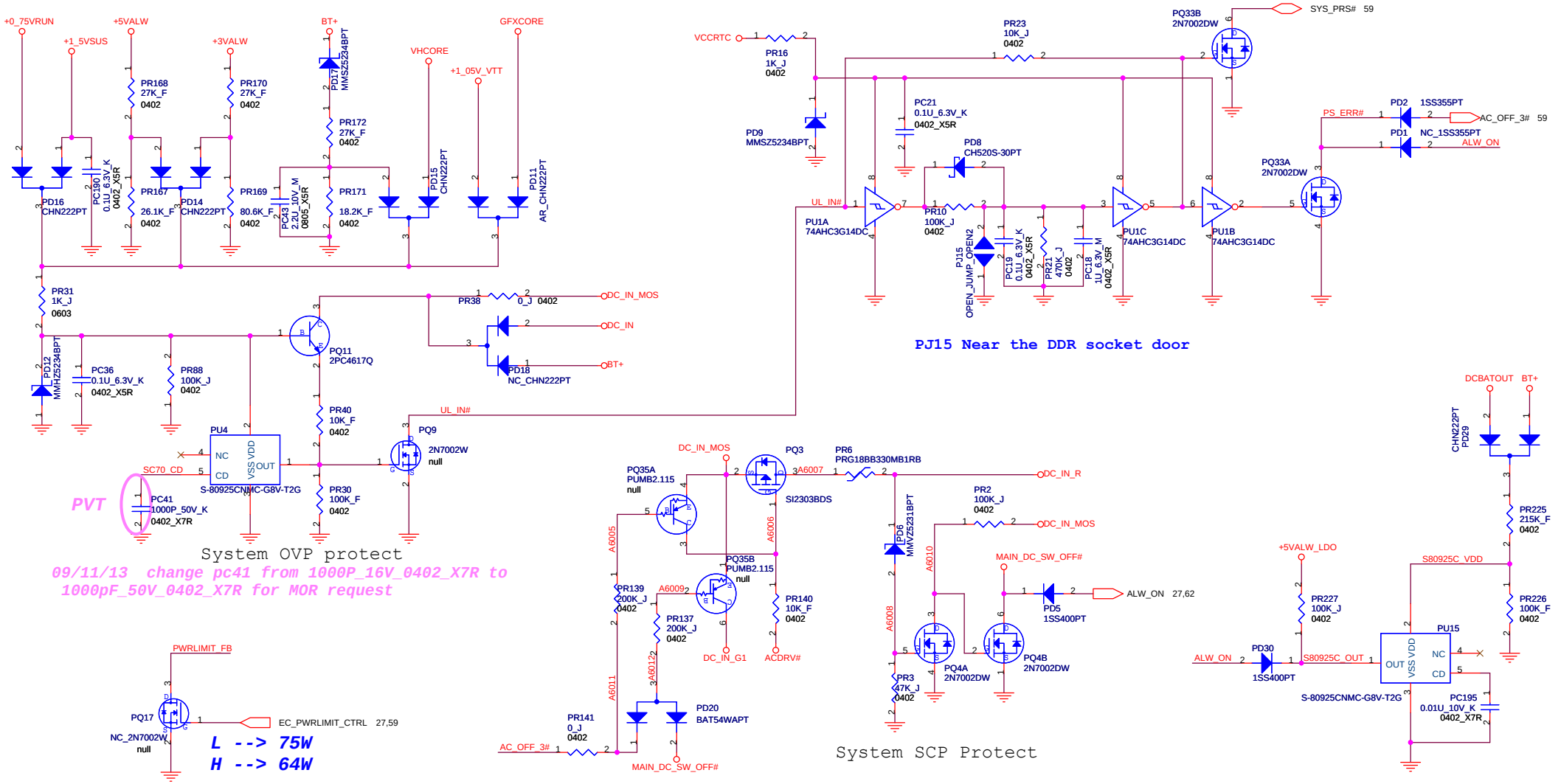
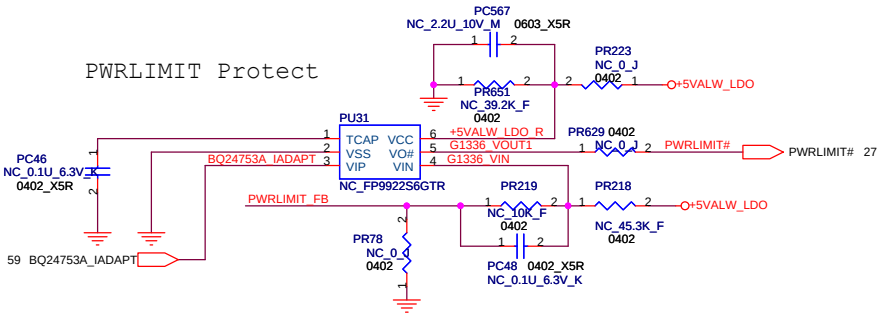


FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Others power plan	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Tuesday, December 29, 2009	Sheet 69 of 80	



DVT	PQ18	PR219	PR79
For Power limit	NO NC	68.1K	2.05K

DVT	PWRLIMIT
H M/B(75W)	3.76A/71.41W
L M/B(64W)	3.2A/60.82W

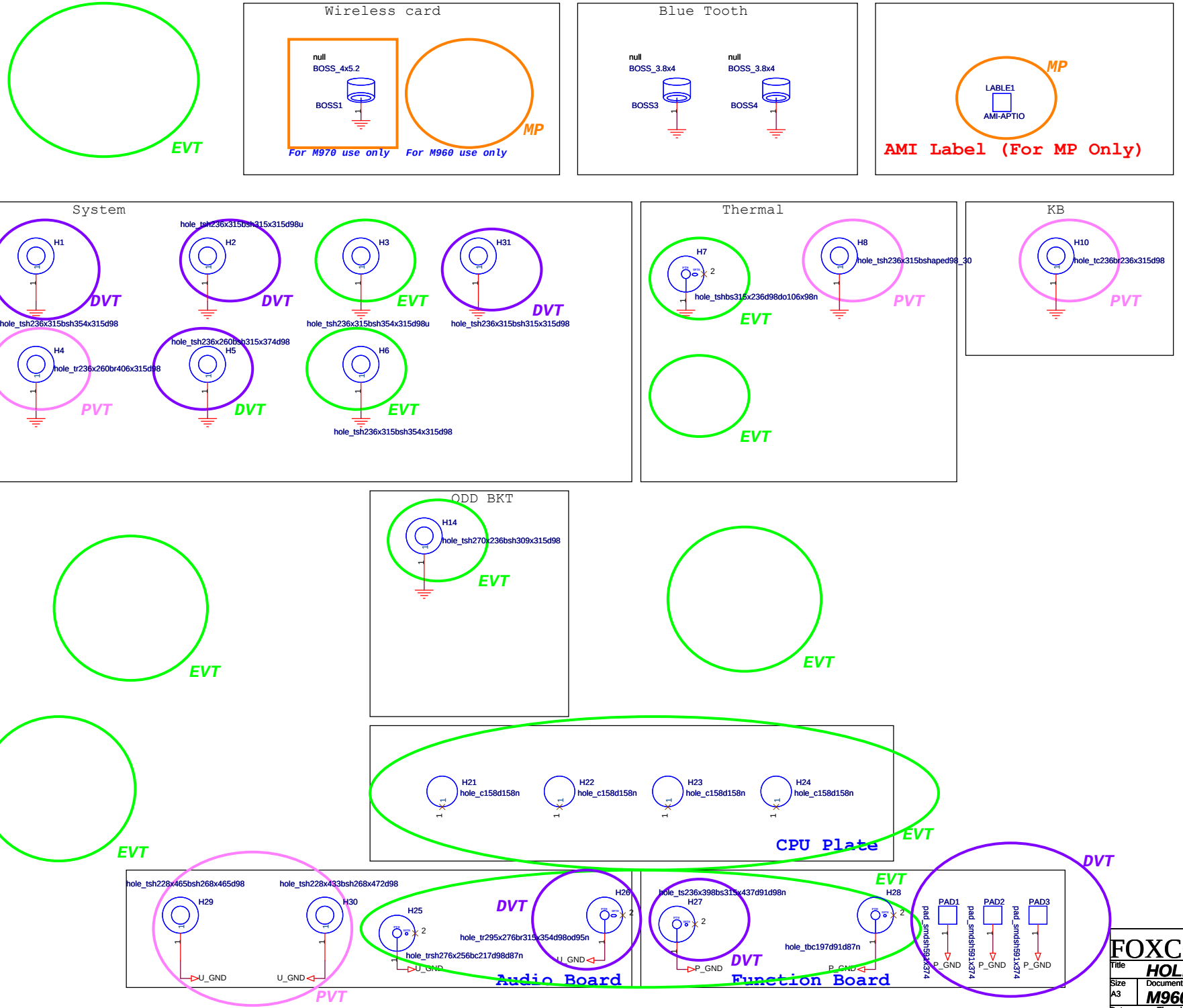


FOXCONN HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division

Title: OVP protection

Size: A3 | Document Number: M960&M970 L Model | Rev: SA

Date: Tuesday, December 29, 2009 | Sheet 70 of 80



FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	HOLE	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Thursday, December 24, 2009	Sheet 71 of 73	

M960/M970 EVT

(2009/06/22)

P.23 [CRT]Change D10 from S24 to SSM24PT for same as M930.

(2009/06/23)

P.61 [DCIN & Charger]Add test points TP1148~TP1155 for BFT test.
P.41 [Camera Connector]Add test points TP1156~TP1161 for BFT test.
P.45 [FAN]Add test points TP1162~TP1165 for BFT test.
P.47 [LAN]Add test points TP1166~TP1181 for BFT test.
P.31 [Debug Port]Add test points TP1186~TP1193 for BFT test.
P.49 [AUDIO Speaker Conn]Add test points TP1194~TP1197 for BFT test.
P.29 [KB Connector]Add test points TP1198~TP1207 for BFT test.
P.48 [SWITCH DB Conn.]Add test points TP1208~TP1211 for BFT test.
P.61 [DCIN&Charger]Add test points TP1212~TP1218 for BFT test.
P.29 [KB Connector]Del CN4 because M960 and M970 KB connectors are decided to co-use.
P.55 [AUDIO Speaker AMP]Del this page because AMP is combined with ALC275
P.51 [PCIE (MS&iLINK)]Change the net name from "SDMS_VCC" to "VCC_MS" because this net is for MS power only.
P.13 [PCH (LVDS,DDI)]Del R1571 because it is a over-design part.
P.27 [HDMI]Del R507,R508,R568,R569,RP53,RP77 for redundant design.
P.23 [CRT]Add Semi-PNP schematic
P.27 [HDMI]Del R567,R504 and change Q34 to 2N7002EPT for PS8101 and PS8171 co-lay.
P.27 [HDMI]Change R515,R538 from 3.9K to 1.5K for PS8101 and PS8171 co-lay.
P.27 [HDMI]Del R496 for PS8101 and PS8171 co-lay.
P.13 [PCH (LVDS,DDI)]Del Q72,R1578,R1577
P.27 [HDMI]Change R511,R506 from 2.2K to 1.5K for PS8101 and PS8171 co-lay.
P.25 [Inverter Connector]Del R400 because it is useless.
P.27 [HDMI]Add R5884~R5899,C6206 for PS8101 and PS8171 co-lay.

P.23 [CRT]NC R5752 for Semi-PNP schematic.

(2009/06/24)

P.23 [CRT]Del U9,R767,C279 for Semi-PNP.
P.23 [CRT]Change net name "VGA_CRT_DET#" to MB_CRT_DET# for Semi-PNP.
P.23 [CRT]Stuff R5752 for Semi-PNP schematic.
P.27 [HDMI]Change R572,R573,R505,R5884,R5885 from 2.2K_J to 4.7K_J for PS8171 only design.
P.27 [HDMI]NC R572,R573,R5884,R5885 for PS8171 only design.
P.27 [HDMI]Del R570 for PS8171 only design.
P.27 [HDMI]Del RP53 for PS8171 only design.
P.27 [HDMI]Stuff R5886,R5890,R5889 for PS8171 only design.
P.27 [HDMI]Stuff R5894 for PS8171 only design.
P.10 [PCH (HDA,JTAG,SAT)]Del R302 for redundant design.
P.27 [HDMI]Stuff R5897,R5898 for PS8171 only design.

P.27 [HDMI]Del R481,R482,R484,R485,R486,R490,R491,R493,L56,L59,L61,L73 for PS8171 only design.
P.27 [HDMI]Del R518,Q34 for PS8171 only design.
P.27 [HDMI]Add R5900 on HDMI_DET_5 and connect it to GND for Intel recommend.
P.43 [Felica Connector]Del F13,R5873,R5872 because the F13 related circuit is out of Felica spec.
P.43 [Felica Connector]Stuff C869,U48,R630,C845 because F14 related circuit is out of Felica spec.
P.60 [DCIN&CHARGE]Change DC-IN current form 8A to 5A.
P.60 [DCIN&CHARGE]Change PD7 from SMD15C to TVS2315PT.
P.62 [Idendify ID]Change PC61 from 1Uf_10V_k to 220Pf_50v_J,then NC PC61.
P.64 [VTT&PCH Power(+1_05V)]Change PR116 from 100k to 470k.
P.65 [DDR3 Power(+1_5V/+0_75V)]Change PR655 from 100k to 470k.
P.67 [CPU Power_VHCORE]Delete PC67,PC155.
P.70 [Other plane power]Change PQ29,PQ45,PQ48: from 2N7002DW to 2N7002SPT.
P.71 [OVP protection]Change PC41 from 0.01Uf to 1000Pf.
P.07 [ARD (GRAPHICS POWER)]Del R5811 and connect a off page to GFX_VR_EN.
P.25 [Inverter Connector]Add and NC R400 on GM_BRADJ to GND for Intel recommend.

(2009/06/25)

P.33 [Mini-PCIE Card (WLAN)]Add R5901 on WLAN_EN for RF VEDS test.
P.51 [SWITCH (Botton & KB LED)*]Change P_VR1,P_VR2,P_VR3,P_VR4,P_VR5 for EMC team request.
P.20 [DDRIII(SO-DIMM_0) 1/2]Del SPR1,J1.
P.20 [DDRIII(SO-DIMM_0) 1/2]Connect CN34 207 Pin to GND.
P.21 [DDRIII(SO-DIMM_0) 2/2]Connect CN35 G2 Pin to GND.
P.07 [ARD (GRAPHICS POWER)]Connector a pull-low resistor "R401" to GFX_DPRSLPVR.
P.34 [LAN (88E8057) 1/2]Del R1462 for Marvell comment.
P.34 [LAN (88E8057) 1/2]NC C997,R94 for Marvell comment.
P.07 [ARD (GRAPHICS POWER)]NC R401 and del GFX_DPRSLPVR off-page.
P.25 [Inverter Connector]Add U89C,R809,R684,C902,R772 for MOR's request.
P.25 [Inverter Connector]Change the off-page from "BL_OFF#" to "INV_EN" for MOR's request.
P.25 [Inverter Connector]Add U89A,U89B,C877,R687 for MOR's request.
P.25 [Inverter Connector]Add an off-page of BL_OFF# on U89D for MOR's request.
P.13 [PCH (LVDS,DDI)]Connect AT38 of U69 to HDMI_DET_5 for MOR's request.
P.10 [PCH (HDA,JTAG,SAT)]Add R5905 to let JTAG_TCK pull down for MOR's request.
P.11 [PCH (PCI-E,SMBUS,CLK)]Add R539,R540 to let PCIECLKRQ3#,PCIECLKRQ4# to pull high to +3VRUN for MOR's request.
P.11 [PCH (PCI-E,SMBUS,CLK)]Add R579 to connect WLAN_CLKREQ# to +3VSUS for MOR's request.
P.11 [PCH (PCI-E,SMBUS,CLK)]NC R577 for MOR's request.
P.14 [PCH (PCI,USB,NVRAM)]Change Bluetooth function from port 13 to port10 to meet Freedom Project Product Specifications.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Del GPIO39 related circuit because this pin is for LCDID3
P.39 [PCIE (MS&iLINK) 1/2]Delete i-Link function from Freedom_specV0.6.

(2009/06/26)

P.19 [CLOCK GEN]Change U31 from SL28748ALC to SL28748CLC.
P.14 [PCH (PCI,USB,NVRAM)]Del USB_PN12,USB_PP12 off-page and add TP365,TP452 on tha same ports.
P.33 [Mini-PCIE Card (WLAN)]Del U45,C891 for disable WIMAX function
P.33 [Mini-PCIE Card (WLAN)]NC 36pin,38pin of CN12 for disable WIMAX function
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Add an off-page "LCDID4" on GPIO48 and change the net name to LCDID4 for LCDID[4:0].
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Del R5902 for LCDID[4:0].
P.51 [SWITCH (Botton & KB LED)*]Del "VAIO" button from Freedom Project Product Specifications V0.6.
P.51 [SWITCH (Botton & KB LED)*]Change the names "Web" and "Display Off" to "Instant On" and "VAIO" from Freedom Project Specifications V0.6.
P.39 [PCIE (MS&iLINK) 1/2]Connect TPB+/- to GND and NC TPAP0/TPAN0/TPBIAS0 to disable i-Link function for Realtek comment.
P.39 [PCIE (MS&iLINK) 1/2]Add R1468 and NC it to disable i-Link function for Realtek comment.
P.11 [PCH (PCI-E,SMBUS,CLK)]Add a +3VALW pull-high resistor R5422 on PEG_A_CLKREQ# pin for MOR's request.
P.12 [PCH (DMI,FDI,GPIO)]Connect SYS_PWROK line to ALW_PWRGD through D33 for MOR's request.
P.32 [Express Card]Add R5457 between the gate and the source of Q38 for MOR's request.
P.56 [AUDIO (Head Phone Jack)*]Add U_R220 pull-high to U_VDDA on U_HP_IN_5 for Realtek comment.
P.56 [AUDIO (Head Phone Jack)*]Change U_GND ground to U_A_GND for Realtek comment.
P.57 [AUDIO (Ext MIC Jack)*]Add U_R222 pull-high to U_VDDA on U_EXTMIC_IN for Realtek comment.

FOXCONN	HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	EVT History(1)	
Size A3	Document Number M960&M970 L Model	Rev SA
Date: Thursday, December 24, 2009	Sheet 72 of 73	

M960/M970 EVT

(2009/06/26)

P.57 [AUDIO (Ext MIC Jack)*]Change U_C35/U_C36 to 4.7u X5R for Realtek comment.
P.27 [HDMI]Change HDMI Repeater from PS8101 to PS8171 for MOR's request.
P.72 [HOLE & AMI LABEL]Add H1~H20 for ME request.

(2009/06/29)

P.25 [Inverter Connector]Change the net name "GM_BRADJ" of CN5 Pin4 to INV_BRADJ.
P.26 [LVDS Connector]Change the net name "GM_BRADJ" to INV_BRADJ.
P.56 [AUDIO (Head Phone Jack)*]Change U_A_GND which is connected to U_C11 pin2 to U_GND.
P.38 [DCIN&Charger]Change PCN1 connector to BP91071-B51E3-7H for ME request.
P.38 [eSATA Combo Conn.]Change CN27 connector to 3Q38111-R21C3-8H for ME request.
P.46 [Touch Pad]Change SW2/SW3/SW6/SW7 to 19-SKRPABE-1000 for ME request.
P.22 [Braidwood Connector]Change NC39 to 1N-0078002-F1G0 for ME request.
P.27 [HDMI]NC R5886,R5889,R5894,R5897,R5898 for PS8171 vendor's comment.
P.39 [PCIE (MS&iLINK) 1/2]Del R1468 and connect XOUT to U71 A2 for Ricoh's comment.
P.16 [PCH (POWER) 1/2]Change R366,R325 to 100 ohm for Intel'comment.
P.16 [PCH (POWER) 1/2]Change C141 to 1U for Intel'comment.
P.27 [HDMI]Change R515 to 2.2K for Intel's comment.
P.09 [ARD (RESERVED)]Change R1274 to 3.3K for Intel's comment.

(2009/06/30)

P.68 [CPU Power_VID]Stuff PR638,PR646 for Power request.
P.68 [CPU Power_VID]NC PR637,PR645 for Power request.
P.33 [Mini-PCIE Card (WLAN)]Del R824 for MOR's request.
P.12 [PCH (DMI,FDI,GPIO)]Change R911 to 10K for MOR's request.
P.42 [Bluetooth Connector]Del C378 for MOR's request.
P.33 [Mini-PCIE Card (WLAN)]NC CN12 15pin and del R18 for RF request.
P.44 [Status LED & LID]Add LED6/LED7/LED8/LED9 for M970 only.
P.33 [Mini-PCIE Card (WLAN)]Add R17 and NC it for MOR's request.

(2009/07/01)

P.72 [HOLE & AMI LABEL]Del BOSS9,BOSS10 for ME request.
P.72 [HOLE & AMI LABEL]Add CPU hole H21,H22,H23,H24 for CPU socket.
P.38 [eSATA Combo Conn.]Del eSATA repeater schematic (U214,C766,C776,C759,C745, R5754,R5835,R5756,R5755,R5757,R5758,R5759,C718,C387) for over-design.
P.10 [PCH (HDA,JTAG,SAT)]Del U27,U28,C817,C838,R5371,R1555,R1556 because this part is for SW reserve design.
P.10 [PCH (HDA,JTAG,SAT)]Change SPI_CLK_SW/SPI_MOSI_SW/SPI_MISO_SW to SPI_CLK_L/SPI_MOSI_L/SPI_MISO_L for modifing the SW reserve design.
P.13 [PCH (LVDS,DDI)]Add two connection L_DDC_CLK/L_DDC_DATA to CN13 5/6 pin for SW request to add EDID function.

(2009/07/02)

P.26 [LVDS Connector]Connect CN13 Pin1 to LCDVCC for LCD power supply.
P.26 [LVDS Connector]Connect CN13 Pin34 to GND for LCD power supply.
P.39 [PCIE (MS&iLINK) 1/2]NC R820/C868/R817/C865/R818/C864 because SD_CD#/SD_WP#/MS_CD# has an internal pull-up resistor and the debouching circuit.
P.24 [LVDS]Update Panel ID and related information.

(2009/07/03)

P.10 [PCH (HDA,JTAG,SAT)]Del TP119/TP123/TP133/TP136/TP137/TP138 and R442 because this is SW reserve design.
P.14 [PCH (PCI,USB,NVRAM)]Del Q39/Q37/R5456/SW5/R300 for changing GNT1#/GNT0# control method.
P.14 [PCH (PCI,USB,NVRAM)]Add R345/R346 pull-high to +3VRUN for controling GNT1#/GNT0#.
P.14 [PCH (PCI,USB,NVRAM)]Change R344/R392/R345/R346 to 10K ohm.
P.33 [Mini-PCIE Card (WLAN)]Del R17 and change the net name "MINI_PCIE_+3_3V_R" to "MINI_PCIE_+3_3V" to del RF reserve circuit.
P.58 [AUDIO (USB)*]Change U_CN2/U_CN3/U_CN6 to 2N-0004009-MKG0 for ME request.
P.27 [HDMI]Reverce Q34A/Q34B/R504/R518 and connect HDMI_DET_3 to AT38 of U69 for MOR's request.
P.22 [Braidwood Connector]Del CN39 and its related schematic for disabling Braidwood function.
P.22 [Braidwood Connector]Del Page.22 and change page number 23~74 to 22~73.
P.51 [AUDIO (CODEC)*]Change U_R5774 to 100K ohm and change the power source on it from U_VDDA to U_+12V because Gate voltage of U_Q55 is too low.
P.54 [AUDIO (AUDIO & USB Conn)*]Move U_SUS_ON to U_CN1 Pin22 and add U_+12V on Pin7.
P.49 [AUDIO/USB DB Conn.]Move SUS_ON to CN31 Pin29 and add +12V on Pin44.
P.25 [LVDS Connector]Add Q177/Q178/R5736/R5737/C575 and change L98 for rush current issue.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Add a NC resistor R979 to let GPIO8 pull-low to GND.
P.14 [PCH (PCI,USB,NVRAM)]Change Bluetooth USB port to port13.
P.14 [PCH (PCI,USB,NVRAM)]Change USB External Port-1 to USB port5 and eSATA change to port0.
P.26 [HDMI]Change R538 to 2.2k in order to equal to R515.

(2009/07/04)

P.32 [Mini-PCIE Card (WLAN)]Restore U45,C891 for WIMAX function.
P.32 [Mini-PCIE Card (WLAN)]Connect 36pin,38pin of CN12 to USB_PN12_L/USB_PP12_L for WIMAX function.
P.32 [Mini-PCIE Card (WLAN)]Add J5 to connect Pin42 and Pin44 of CN12 for MOR's request.

(2009/07/06)

P.11 [PCH (PCI-E,SMBUS,CLK)]Stuff Y8,C1288,C1289,R1226,R813 for M930 HDMI complication test issue.
P.11 [PCH (PCI-E,SMBUS,CLK)]NC R1651 for M930 HDMI complication test issue.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Stuff R979 and NC R983 for M930 HDMI complication test issue.

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(2009/07/07)

P.41 [Bluetooth Connector]Add C378 pull-low to GND refer to M930.
P.43 [Status LED & LID]Del POWER/SUSPEND LED and its related circuit for ID changing.
P.13 [PCH (LVDS,DDI)]Add R222 pull-low resistor connect to HDMI_DET_3 for MOR's comment.
P.12 [PCH (DMI,FDI,GPIO)]Change R973 to 2.2K ohm for MOR's requirement.
P.25 [LVDS Connector]Add Q177 and related RC for protecting rush current.
P.48 [AUDIO Speaker Conn]Del Q28/Q30/Q53 and connect Q25 and Q27 because short protection circuit can marge L channel and R channel.
P.04 [ARD (CLK,MISC,JTAG)]Add Q72 for Intel S3 Power Reduction issue.
P.59 [DCIN&Charger]Delete PR17.
P.62 [SYS Power (+3_3V/+5V)]Delete close_jump GP2.
P.64 [DDR3 Power(+1_5V/+0_75V)]Change 1.5VSUS full load from 12A to 13A.
P.64 [DDR3 Power(+1_5V/+0_75V)]Change PR654 from 46.4k to 49.9k.
P.68 [VGFX Power_GFXCORE]Delete PR195.
P.69 [Others power plane]Change 1.5VRUN full load form 6A to 3A.
P.69 [Others power plane]Add 1.5VRUN discharge circuit (add PR660 330ohm,PQ71 2N7002EPT).
P.13 [PCH (LVDS,DDI)]Del L_DDC_CLK/L_DDC_DATA off-page for disabling EDID.

(2009/07/08)

P.43 [Status LED & LID]Add Q18/Q21/Q48/Q51/R384/R390/R690/R691/R694/R695 for POWER/SUSPEND LED location changing.
P.41 [Bluetooth Connector]Del C378 because C377 has the same function.
P.27 [EC+KBC(NPCE783L)]Add SYSTEM_ID3 (R5891/R5900) for SKU control.
P.25 [LVDS Connector]NC CN13 Pin3 because EDID is disabled.
P.43 [Status LED & LID]Change Q18/Q21/Q50 to DTC114EUB for MOR's request.
P.50 [SWITCH (Botton & KB LED)*]Del P_SW3 and add P_CN4 for POWER/SUSPEND LED location changing.
P.07 [ARD (GRAPHICS POWER)]Change VDDQ power source from +1_5VSUS to +1_5VRUN for Intel S3 Power Reduction issue.
P.47 [SWITCH DB Conn.]Change CN2 to 14pin type for POWER/SUSPEND LED location changing.
P.50 [SWITCH (Botton & KB LED)*]Change P_CN3 to 14pin type for POWER/SUSPEND LED location changing.
P.38 [PCIE (MS&iLINK) 1/2]Change CN36 type for ME request.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Set GPIO27 as RST_GATE for Intel S3 Power Reduction issue.
P.62 [SYS Power (+3_3V/+5V)]Change NC PR118 to NO NC PR118 and NC PR234,PR235.
P.68 [VGFX Power_GFXCORE]Change NC PC281 to NO NC PC281.
P.70 [OVP protection]Delete reserved Power limit circuit (delete PU2,PU11,PD22,PR22,PR24,PR142,PR143,PR149,PR153,PR159,PR213,PR214,PC26,PC27,PC28).
P.70 [OVP protection]Change PR218 from 37k to 45.3k.
P.11 [PCH (PCI-E,SMBUS,CLK)]Del R1590/R1591/R1592/Q73/Q74 and rename SMB_DATA_SB/SMB_CLK_SB to SMB_DATA_R/SMB_CLK_R refer to M930.
P.10 [PCH (HDA,JTAG,SAT)]Del R1552/R1554 and rename SPI_CLK_L/SPI_MOSI_L to SPI0_CLK/SPI0_MOSI for redundant design.
P.10 [PCH (HDA,JTAG,SAT)]Add R5908 on SATA_LED# which is pull-high to +3VRUN for Intel comment.
P.04 [ARD (CLK,MISC,JTAG)]NC R1451/R1452 and stuff R1450/R1453 refer to M930.
P.39 [PCIE (SD) 2/2]Change CN29 type for ME request.
P.45 [Touch Pad]Change SW2/SW3/SW6/SW7 type for ME request.

(2009/07/09)

P.55 [AUDIO (Head Phone Jack)*]Change Pin7/Pin8 of U_CN4 to U_A_GND for Layout request.
P.07 [ARD (GRAPHICS POWER)]Add a Open-Jump PJ43 between +1_5VRUN to VDDQ.
P.06 [ARD (POWER)]Del R856/R857 for MOR's request.
P.07 [ARD&CFD (GRAPHICS POWER)]Del R864/R866/R868/R869/R871 for MOR's request.
P.38 [PCIE (MS&iLINK) 1/2]Add damping resistors (R5909~R5917) on each MS signal.
P.39 [PCIE (SD) 2/2]Change C518/C522 to X5R type for MOR's request.
P.39 [PCIE (SD) 2/2]Add damping resistors (R5918~R5922) on each SD signal for MOR's request.
P.39 [PCIE (SD) 2/2]Change C767 to 10pF for MOR's request.
P.56 [Status LED & LID]Del LED7/LED8/LED10 for ME request.
P.25 [LVDS Connector]Add NC Cap. (C6306~C6313) between each LVDS differential lane.
P.33 [LAN (88E8057) 1/2]Modify R94/R97/C997 description.
P.33 [LAN (88E8057) 1/2]Change all resistors and caps to 88E8059 setting.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Change R979 to 1k ohm for Intel suggestion.
P.71 [HOLE & AMI LABEL]Add H25/H26/H27/H28 for ME request.
P.22 [CRT]Change CN20 type for ME request.
P.57 [AUDIO (USB)*]Change U_CN2/U_CN3/U_CN6 type for ME request.
P.71 [HOLE & AMI LABEL]Del H11/H12/H13/H15/H16/H17/H18/H19/H20 for ME request.
P.31 [Express Card]Rename PCIE_EXPRESS_WAKE# to PCIE_WAKE# to del reserve design.
P.12 [PCH (DMI,FDI,GPIO)]Del R290 and PCIE_EXPRESS_WAKE# off-page to del reserve design.
P.59 [DCIN&Charger]Renamed resistor PR657 to PR4.
P.68 [VGFX Power_GFXCORE]Change NC PR523,NC PR523,NC PR526,NC PR528,NC PR530,NC PR531,NC PR534 to No NC.
P.69 [Others power plane]Add 0.75V_RUN discharge circuit(add PR661 330ohm).
P.69 [Others power plane]Change PQ71 from 2N7002EPT to ME2N7002KW.
P.04 [ARD (CLK,MISC,JTAG)]Del the description of RST_GATE and add a 1k ohm resister R5923 between +1_5VSUS and DDR3_DRAMRST#.
P.04 [ARD (CLK,MISC,JTAG)]Add R5924/R5925/U217 for Intel S3 Power Reduction issue.
P.04 [ARD (CLK,MISC,JTAG)]Del R928/R929 and related description for Intel S3 Power Reduction issue.
P.40 [Camera Connector]Add R5926/R5927/C6314/C6315 For EMI verification.
P.24 [Inverter Connector]Add R5928 For EMI verification.

(2009/07/10)

P.37 [eSATA Combo Conn.]Swap L66/L67 for layout request.
P.46 [Thermal Sensor]Change thermal sensor to G781-1 for SW request.
P.50 [SWITCH (Botton & KB LED)*]Change the description "Instant On" to "Web(Instant On) for SW request"
P.38 [PCIE (MS&iLINK) 1/2]Del R820/C868/R817/C865/R818/C864 for Ricoh's FAE suggest.
P.38 [PCIE (MS&iLINK) 1/2]Add description of C794/C771/C774/C992 for Ricoh's FAE suggest.
P.38 [PCIE (MS&iLINK) 1/2]Add description of C790/C769/C770/C772/C799 for Ricoh's FAE suggest.
P.38 [PCIE (MS&iLINK) 1/2]Add description of C716/C717 for Ricoh's FAE suggest.
P.26 [HDMI]Connect Q57 D/S to +5VRUN_L188/+5VRUN_F.
P.25 [LVDS Connector]Connect Q144 D/S to DCBATOUT_L/DCBATOUT.
P.27 [EC+KBC(NPCE783L)]Change net name "KB_PRESENCE#" to "INST_ON_SW#" for SW request.
P.59 [DCIN&Charger]Delete NC PR12.
P.59 [DCIN&Charger]Change charge voltage form 12.48V to 12.465V for MOR request (change PR25 form 200k_F to 210K_F, change PR27 from 100K_F to 100K_D).
P.61 [Identify IC]Change PC66 from 0.1u_16v_0402_Y5V to 0.1u_10v_0402_X5R.
P.61 [Identify IC]Change NC PC65 1u_10v_0603_X5R to NC PC65 1u_10v_0402_X5R.
P.66 [CPU Power_VHCORE]Change PC112 from 100U_25V_M_Φ6.3*7.7mm to 68uF_25V_M_Φ6.3*5.8mm.

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(2009/07/11)

P.24 [Inverter Connector]Reverse CN5.
P.50 [SWITCH (Botton & KB LED)*]Reverse P_CN3.
P.25 [LVDS Connector]Add description on the circuit for inrush current issue of M870.
P.22 [CRT]Change F2 type for PUR request.
P.51 [AUDIO (CODEC)*]Change U_C459/U_C476/U_C787 type for PUR request.
P.07 [ARD (GRAPHICS POWER)]Add net name "+1_5VRUN_J".
P.14 [PCH (PCI,USB,NVRAM)]Del R344/R392 and the description about Boot-BIOS for SW request.
P.40 [Camera Connector]Add net name DMIC_CLK_R/DMIC_DAT_R and connect TP1160/TP1161 to the new net for TE request.
P.20 [DDRIII(SO-DIMM_0) 1/2]Reconnect SPR2/J2 to CN34 and CN35 for EMC request.
P.10 [PCH (HDA,JTAG,SAT)]Reverse CN26.
P.26 [HDMI]Change CN21 type for ME request.
P.48 [AUDIO Speaker Conn]Swap JSPK1 for ME request.

(2009/07/13)

P.39 [PCIE (SD) 2/2]Change U22 to G553E1P11U to meet MOR's request for SD.
P.45 [Touch Pad]Reverse CN8 for ME request.
P.50 [SWITCH (Botton & KB LED)*]NC P_VR2 for EMC reserve.
P.38 [PCIE (MS) 1/2]Del all i-Link related description.
P.24 [Inverter Connector]Reverse CN5.
P.71 [HOLE & AMI LABEL]Change H2/H3/H4/H5/H6/H7/H10/H14 type for ME request.
P.26 [HDMI]Swap U37 for Layout request.
P.59 [DCIN&Charger]Delete EC3 and C907.
P.66 [CPU Power_VHCORE]Change PC566 from 0.1U_6.3V_K to 0.1U_16V_K (HH PN:1C-2B20104-K300).
P.68 [VGFX Power_GFXCORE]Change PC98 from 2.2U_6.3V_K to 2.2U_10V_M (HH PN:1C-2B30225-M201).
P.70 [OVP protection]Change PQ3 from IRLML5103TRPbF to SI2303BDS.
P.04 [ARD (CLK,MISC,JTAG)]Change U217 SUS_PWRGD to RUN_PWRGD.
P.71 [HOLE & AMI LABEL]Del H9 for ME request.
P.04 [ARD (CLK,MISC,JTAG)]Change R5924/R5925 to 1.5K/750 ohm for intel's comment.
P.69 [Others power plane]Change PR661 from 330ohm to 33ohm.

(2009/07/14)

P.25 [LVDS Connector]Swap Pin1 CN13 to Pin3 CN13 for cable design.
P.71 [HOLE & AMI LABEL]Change H4/H5/H7 footprint for ME request.
P.59 [DCIN&Charger]NC PR76 and PR77.
P.66 [CPU Power_VHCORE]Change PR555 and PR569 from 2.7K to 2.21K.
P.66 [CPU Power_VHCORE]NC PC260 ,NC PC261.
P.27 [EC+KBC(NPCE783L)]Pull-high INST_ON_SW# to +ECVCC for SW request.
P.64 [DDR3 Power(+1_5V/+0_75V)]Add PQ59(2N7002EPT)/PR600(100K)/PC570(1U_10V_K), then NC PQ59/PR600/PC570.
P.10 [PCH (HDA,JTAG,SAT)]Add C6316/C6317/C6318/C6319/C6320/C6321 for EMC reserve.
P.33 [LAN (88E8057) 1/2]Add C6322/C6323 for EMC reserve.
P.39 [PCIE (SD) 2/2]Add C6325 for EMC reserve.
P.38 [PCIE (MS) 1/2]Add C6324 for EMC reserve.

(2009/07/15)

P.36 [SATA CD-ROM]NC CN37 for ME request.
P.10 [PCH (HDA,JTAG,SAT)]Connect C6321 to +1_05V_VTT for EMC request.
p.66 [CPU Power_VHCORE]change PC112 from NOCHICON to Panasonic.
P.20 [DDRIII(SO-DIMM_0) 1/2]Del SPR2 for EMC request.
P.20 [DDRIII(SO-DIMM_0) 1/2]Del EMCS1/EMCS2 off-page and add J6 for EMC request.
P.21 [DDRIII(SO-DIMM_1) 2/2]Rename EMCS1/EMCS2 to EMCS3/EMCS4 and add J7/J8 for EMC request.
P.68 [VGFX Power_GFXCORE]change PC242 and PC282 form 1C-2B20152-M000 to 1C-2B20152-K600.
P.09 [ARD (RESERVED)]Del RP83/DQ_VREF off-page and add two test point to CPU for Intel's comment.
P.20 [DDRIII(SO-DIMM_0) 1/2]Del C35/C41/R1283 and DQ_VREF0 off-page for Intel's comment.
P.20 [DDRIII(SO-DIMM_0) 1/2]Connect VREF_DQ ato VREF_CA for Intel's comment.
P.21 [DDRIII(SO-DIMM_1) 2/2]Del C37/C44/R1284 and DQ_VREF1 off-page for Intel's comment.
P.21 [DDRIII(SO-DIMM_1) 2/2]Connect VREF_DQ ato VREF_CA for Intel's comment.
P.83 [HOLE & AMI LABEL]Add H29/H30/PAD1/PAD2/PAD3 for EMC request.
P.71 [HOLE & AMI LABEL]Change H28/H25 type for ME request.

(2009/07/16)

P.71 [HOLE & AMI LABEL]Change PAD1/PAD2/PAD3 for CIS request.
P.68 [VGFX Power_GFXCORE]change PR191 vendor numbler form NT731JTTD104J3800J to ERTJ1VV104J.
P.20 [DDRIII(SO-DIMM_0) 1/2]Restore C35/C41 for MOR's request.
P.21 [DDRIII(SO-DIMM_1) 2/2]Restore C37/C44 for MOR's request.

(2009/07/17)

P.66 [CPU Power_VHCORE]Change PR565 from 10k to 1.8k, change PC566 from 0.1u to 0.022u.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Mount R983 and NC R979 for Intel suggestion.

(2009/07/21)

p.1~76 [Page Data]Update all page data.

(2009/07/24)

P.72 [Braidwood Connector]Add CN39 and its related schematic for layout estimation.
P.14 [PCH (PCI,USB,NVRAM)]Add Braidwood related schematic for layout estimation.

(2009/07/30)

P.72 [Braidwood Connector]Del CN39 and its related schematic for layout estimation.
P.66 [CPU Power_VHCORE]Delete PJ42
P.68 [VGFX Power_GFXCORE]Delete PJ38.

(2009/08/13)

P.27 [EC+KBC(NPCE783L)]Del R5852 for OVT_EC# double pull-high.
P.48 [AUDIO Speaker Conn]Change JSPK1 to 1N-0004003-M1T0 for ME request.
P.54 [AUDIO (AUDIO & USB Conn)*]Reverse U_CN1 for moving U_CN1 from TOP to BOT side.
P.55 [AUDIO (Head Phone Jack)*]Changen U_CN4 to 2N-000600N-FKG0.
P.56 [AUDIO (Ext MIC Jack)*]Change U_CN5 to 2N-000600C-FRG0.
P.57 [AUDIO (USB)*]Change U_USB_OC#1/2/3 to U_USB_OC#0/2.
P.54 [AUDIO (AUDIO & USB Conn)*]NC U_USB_OC#3 and Change U_USB_OC#1/2 to U_USB_OC#0/2.
P.49 [AUDIO/USB DB Conn.]NC U_USB_OC#3 and Change U_USB_OC#1/2 to U_USB_OC#0/2.
P.14 [PCH (PCI,USB,NVRAM)]Del off-page USB_OC#1/3.
P.04 [ARD (CLK,MISC,JTAG)]Change Q72 to 17-2N7002W-0000 for PUR request.
P.66 [CPU Power_VHCORE]Delete NC_PC260, NC_PC261.

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(2009/08/18)

P.22 [CRT]Change F2 to 0.35A.
P.83 [HOLE & AMI LABEL]Add H31 and change H1/H27/PAD1/PAD2/PAD3 for ME request.
P.37 [eSATA Combo]Swap CN27B.
P.31 [Express Card]Change R5457 to 470K and add NC R686 for MOR request.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Change RST_GATE from GPIO27 to GPIO46 , Stuff R982, NC R977.
P.34 [LAN (Transformer) 2/2]Change L70 for cost down.
P.51 [AUDIO (CODEC)*]Change U_U215.
P.43 [Status LED & LID]Change U21 to 15-EC2648B-0000 for cost down.
P.59 [DCIN&Charger] Change PQ5,PQ16,PQ34 to 17-2N7002W-0000 for materials shortage.
P.64 [DDR3 Power(+1_5V/+0_75V)] Change PQ59 to 17-2N7002W-0000 for materials shortage.
P.70 [OVP protection] Change PQ9,PQ17 to 17-2N7002W-0000 for materials shortage.
P.69 [Others power plane] Change PQ29,PQ45,PQ48 to 17-2N7002D-W001 for materials shortage.
P.69 [Others power plane] Change PQ72A to PQ71A.
P.83 [HOLE & AMI LABEL]Change H29/H30 for ME request.

(2009/08/24)

P.57 [AUDIO (USB)*]Change U_CN2/U_CN3/U_CN6 for ME request.
P.48 [AUDIO Speaker Conn]Change JSPK1 for ME request.
P.22 [CRT]Change CN20 for ME request.
P.37 [eSATA Combo Conn.]Reverse L62/L66 for Layout request.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Change R977 from NC to Stuff and change R982 from Stuff to NC.

(2009/08/25)

P.71 [HOLE & AMI LABEL]Change H26 for ME request.

(2009/08/27)

P.71 [HOLE & AMI LABEL]Change H30 for ME request.

(2009/08/31)

P.59 [DCIN&Charger]Change PCN1 to BP92071-B81E2-7H for ME request.
P.36 [SATA HDD]Change CN33 to LN21131-D40L-9H for ME request.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Add R5933/R5934/R5935/R5936 and change R5870 to 100K to pull-high LCDID for PE request.
P.23 [LVDS]Add R5937/R5938/R5939/R5940/R5941/R5942 to pull-low LCDID for PE request.

(2009/09/01)

P.44 [FAN]Del TP1163.
P.51 [AUDIO (CODEC)*]Add ALC269 co-lay schematic and del U_TP229, U_TP231, U_TP228.
P.14 [PCH (PCI,USB,NVRAM)]Del R1575 for redundant design (double pull-low).
P.52 [AUDIO (MUTE)*]Add ALC265 co-lay schematic.
P.10 [PCH (HDA,JTAG,SAT)]NC R5908 for redundant design (double pull-high).
P.62 [SYS Power (+3_3V/+5V)]Move TP215 from +5VALW_PWM to +5VALW for power test.
P.62 [SYS Power (+3_3V/+5V)]Move TP219 from +3VALW_PWM to +3VALW for power test.
P.63 [SYS Power(+1_05V_VTT)]Add TP504 for +1.05V_VTT power test.
P.66 [CPU Power_VHCORE]Add TP507,TP223,TP224 for VHCORE power test.
P.67 [CPU Power_VID]Add TP225~ TP233 for power test.
P.68 [VGFX Power_GFXCORE]Add TP508 for GFXCORE power test.

(2009/09/03)

P.43 [Status LED & LID]Move R390/R384 to Drain side of Q51/Q48 for MOR comment.
P.25 [LVDS Connector]Change CN13 to M870 type (1N-0040000-FWG0).
P.47 [SWITCH DB Conn.]Change CN2 to 12pin type (1N-0012002-F0T0).
P.50 [SWITCH (Botton & KB LED)*]Change P_CN3 to 12pin type (1N-0012002-F0T0).
P.50 [SWITCH (Botton & KB LED)*]Move NUM LOCK LED/CAP LED/SCROLL LOCK LED driving circuit to MB for MOR comment.
P.43 [Status LED & LID]Add NUM LOCK LED/CAP LED/SCROLL LOCK LED driving circuit for MOR comment.
P.09 [ARD (RESERVED)]Del test points for MOR comment.
P.11 [PCH (PCI-E,SMBUS,CLK)]Del test points for MOR comment.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Del test points for MOR comment.
Test Points[TP109/TP193/TP181/TP208/TP209/TP211/TP210/TP212/T213/TP214/ TP235/TP236/TP265/TP266/TP237/TP239/TP327/TP328/TP329/TP256/TP257/TP259/ TP260/TP262/TP263/TP264/TP284/TP287/TP288/TP289/TP290/TP291/TP292/TP293/ TP294/TP295/TP296/TP297/TP298/TP425/TP1116/TP1117/TP1118/TP1119/TP140/ TP147/TP148/TP149/TP148/TP145/TP144/TP134TP1120/TP1121/TP1122/TP1123/ TP1124/TP188/TP183/TP88/TP91/TP93/TP101/TP412/TP416/TP415/TP417/TP414/ TP421/TP422/TP423/TP424]
P.09 [ARD (RESERVED)]Del RP87 for MOR and Intel comment.
P.43 [Status LED & LID]Add LED test points TP1223/TP1224/TP1225/TP1226/TP1227/ TP1228/TP1229/TP1230.
P.10 [PCH (HDA,JTAG,SAT)]Change U98 to W25Q32BVSSIG.
P.51 [AUDIO (CODEC)*]Del U_U7 and U_C155 for Realtek suggestion.
P.16 [PCH (POWER) 1/2]Del R897, R989 for MOR comment.
P.17 [PCH (POWER) 2/2]Del R428, R958 for MOR comment.
P.04 [ARD (CLK,MISC,JTAG)]Add R5950, C6327, R5951, R5949, R5948, C6326 for Intel S3 issue.

(2009/09/08)

P.51 [AUDIO (CODEC)*]Change U_R327 to 1K.
P.59 [DCIN&Charger]NC PR33 for costdown.
P.70 [OVP protection]PR167 change to 26.1K, PR169 change to 80.6K , PR171 change to 18.2K for OVP Adjust
P.70 [OVP protection]Use SW PWRLIMIT function replaced HW PWRLIMIT circuit for costdown.(NC PU31,PC567,PR223,PR629,PR219,PR218,PR78,PC46.)
P.50 [SWITCH (Botton & KB LED)*]Change P_VR1/P_VR2/P_VR3/P_VR4 to 19-MLVS060-5000.
P.27 [EC+KBC(NPCE783L)]Change C27/C26 to 15p for Crystal vendor comment.
P.10 [PCH (HDA,JTAG,SAT)]Change C727/C702 to 15p for Crystal vendor comment.
P.38 [PCIE (MS) 1/2]Change C785/C786 to 22p for Crystal vendor comment.
P.11 [PCH (PCI-E,SMBUS,CLK)]Change C1288/C1289 to 27p for Crystal vendor comment.
P.43 [Status LED & LID]Change TP1228 to connect to R692 pin2.
P.37 [eSATA Combo Conn.]Add eSATA reperater schematic and NC it.
P.10 [PCH (HDA,JTAG,SAT)]Change CN18 to GB5RF120-1203-7F for Halgen Free.
P.30 [Debug Port]Change CN30 to GB5RF120-1203-7F for Halgen Free.
P.42 [Felica Connector]Add Felica power supply schematic as Pokerman type for MOR request.
P.14 [PCH (PCI,USB,NVRAM)]Change USB_OC# signal to EVT type for MOR request.
P.29 [SPI Flash ROM]Change U23 to W25X10BVSNIG for SW comment.
P.51 [AUDIO (CODEC)*]Move U_R5774 to P.48 and rename to R5774.
P.49 [AUDIO/USB DB Conn.]NC +12V and add a +5VALW pin for USB VEVS test.
P.54 [AUDIO (AUDIO & USB Conn)*]NC U_+12V and add a U_+5VALW pin for USB VEVS test.
P.49 [AUDIO/USB DB Conn.]Change CN31 to 1N-0050004-F0T0 for ME request.
P.54 [AUDIO (AUDIO & USB Conn)*]Change U_CN1 to 1N-0050004-F0T0 for ME request.
P.33 [LAN (88E8057) 1/2]Add R5965/R5966/R5967 for 88E8057/88E8059 co-lay.
P.49 [AUDIO/USB DB Conn.]Change CN31 Pin 43 to GND.
P.54 [AUDIO (AUDIO & USB Conn)*]Change U_CN1 Pin 43 to GND.

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(2009/09/08)

P.43 [Status LED & LID]Change Q49/Q179/Q180/Q181 to 17-DTA114Y-UB00 for PUR suggest.
P.32 [Mini-PCIE Card (WLAN)]Change Q5 to 17-DTC144E-UB00 for PUR suggest.
P.22 [CRT]Change Q11 to 17-DTC144E-UB00 for PUR suggest.
P.44 [FAN]Change Q77 to 17-DTC144E-UB00 for PUR suggest.
P.59 [DCIN&Charger]Change TP1148,TP1149,TP1150,TP1151 from DC_IN_1 to P+ for power test.
P.59 [DCIN&Charger]Change PQ16,PR76,PR77 from NC to mount for EC PWRLIMIT function.
P.59 [DCIN&Charger]Change PR79 from 0 to 3.48K, change PR11 from 20K to 12K for EC PWRLIMIT function.
P.61 [Identify IC]Add PD31 and change PR68 from 10K to 4.7K for MOR side request.
P.69 [Others power plan]Delete TP189,TP203 for power test.

(2009/09/09)

P.30 [Debug Port]Del TP1186~TP1193.
P.25 [LVDS Connector]Add L_DDC_CLK/L_DDC_DATA for EDID function.
P.13 [PCH (LVDS,DDI)]Add L_DDC_CLK/L_DDC_DATA for EDID function.
P.62 [SYS Power (+3_3V/+5V)]Change PR652,PR245 from NC to mount 4.7ohm. Change PC568,PC272 from NC to mount 680pF for EMI suggest.
P.63 [SYS Power(+1_05V_VTT)]Change PR188 from NC to mount 4.7ohm, Change PC170 from NC to 680pF for EMI suggest.
P.64 [DDR3 Power(+1_5V/+0_75V)]Change PR41 from NC to mount 4.7ohm, Change PC42 from NC to mount 680pF for EMI suggest.
P.68 [VGFX Power_GFXCORE]Change PR527 from NC to mount 4.7ohm, Change PC225 from NC to mount 680pF for EMI suggest.
P.40 [Camera Connector]Del R5926/R5927 and add L76/L77 for EMC request for DMIC noise.
P.40 [Camera Connector]Mount C6314/C6315 for EMC request for DMIC noise.
P.48 [AUDIO Speaker Conn]Del RR5876, R5877, R5878, R5879 and Add L78, L79, L80, L81 for EMC request to filtrate SPK noise.
P.25 [LVDS Connector]Add C6334/C6335 for EMC request for 150MHz powerbase issue.
P.42 [Felica Connector]Change Felica power supply from +5VSUS to +3VSUS.
P.39 [PCIE (SD) 2/2]Change R391 to 100K for MOR request.
P.31 [Express Card]NC Q38, R5457 and mount R686 for MOR comment.

(2009/09/10)

P.25 [LVDS Connector]Add CN13 Pin40 for EDID function.
P.32 [Mini-PCIE Card (WLAN)]Add C6339/C6340 for EMI request.
P.16 [PCH (POWER) 1/2]Add C6336/C6337/C6338 for EMI request.
P.50 [SWITCH (Botton & KB LED)*]Change P_LED1/P_LED2/P_LED3 to HT-170UYG.
P.63 [VTT&PCH Power(+1_05V)]Del PJ22 and add L82 for EMI request for 150MHz powerbase issue.
P.69 [Others power plane]Add C6342/C6343 on +3VSUS for EMI request.
P.69 [Others power plane]Add C6344/C6345/C6346 on +3VRUN for EMI request.
P.33 [LAN (88E8059) 1/2]Del R97 and add C6341 for Marvell FAE request.
P.33 [LAN (88E8059) 1/2]Del R5966, R5967 for Marvell FAE request.
P.45 [LAN (88E8059) 1/2]Change C993 to 10u for Marvell FAE request.
P.31 [Express Card]Correct Express Card SPEC.
P.46 [Thermal Sensor]NC U28 and related schematic for MOR request.
P.36 [SATA CD-ROM]Del CN37 for MOR request.
P.49 [AUDIO/USB DB Conn.]Add F1 for MOR comment.
P.54 [AUDIO (AUDIO & USB Conn)*]rename U_+5VALW to U_+5VALW_IN for MOR comment.
P.57 [AUDIO (USB)*]Del U_F1 and rename U_+5VALW to U_+5VALW_IN for MOR comment.
P.71 [HOLE & AMI LABEL]Del BOSS2 for MOR request.
P.51 [AUDIO (CODEC)*]Change U_R321 to 100K for MOR request.
P.52 [AUDIO (MUTE)*]NC U_C472 for MOR comment.
P.56 [AUDIO (Ext MIC Jack)*]NC U_R42, U_R46 for MOR comment.
P.56 [AUDIO (Ext MIC Jack)*]Del U_C26, U_C31 and add U_R5791, U_R5792 for MOR comment.
P.56 [AUDIO (Ext MIC Jack)*]NC U_R42, U_R46 for MOR comment.
P.63 [AUDIO (CODEC)*]NC U_C923.
P.55 [AUDIO (Head Phone Jack)*]Change U_GND to U_A_GND for Realtek FAE suggest.
P.25 [LVDS Connector]NC CN13 Pin7.

(2009/09/11)

P.59 [DCIN&Charger]Change PR15 to RLM12FTSR020 for PUR request.
P.59 [DCIN&Charger]Change PF1 to 0437007.WR for PUR request.
P.25 [LVDS Connector]Change CN13 for Halgen-free.
P.48 [AUDIO Speaker Conn]Swap JSPK1 for layout concern.
P.32 [Mini-PCIE Card (WLAN)]Change SW4 to 1BS007-12110-002-7H for ME request.
P.43 [Status LED & LID]Change LED3/LED4 vendor to Everlight.
P.55 [AUDIO (Head Phone Jack)*]Change U_A_GND to U_GND for Realtek FAE suggest.
P.51 [PCIE (SD) 2/2]Change CN29 to WK21923-S6P3-4H for ME request.
P.10 [PCH (HDA,JTAG,SAT)]Change CN18 to No Halgen-free.
P.30 [Debug Port]Change CN30 to No Halgen-free.
P.50 [SWITCH (Botton & KB LED)*]Change P_CN3 to No Halgen-free.
P.47 [SWITCH DB Conn.]Change CN2 to No Halgen-free.
P.44 [FAN]Change CN14 to No Halgen-free.
P.48 [AUDIO Speaker Conn]Change JSPK1 to No Halgen-free.
P.71 [HOLE & AMI LABEL]Change H2/H4/H5 for ME request.
P.27 [EC+KBC(NPCE783L)]NC U216 Pin8 and del R575.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect DIS_FAN_MON# to U69F GPIO57 and pull-high to +3VRUN.
P.27 [EC+KBC(NPCE783L)]NC U4A Pin20 and add SYSTEM_ID1 off-page.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect SYSTEM_ID1 to U69F GPIO17 and del R965.
P.27 [EC+KBC(NPCE783L)]NC U4A Pin27 and add SYSTEM_ID0 off-page.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect SYSTEM_ID0 to U69F GPIO16 and NC RP19 Pin7.
P.27 [EC+KBC(NPCE783L)]NC U216 Pin9.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Connect PM_SLP_ME# to U4B GPIO26.
P.27 [EC+KBC(NPCE783L)]Del R5853 and connect INST_ON_SW# to GPIO12.
P.27 [EC+KBC(NPCE783L)]NC U216 Pin3 and connect WLAN_EN to U4A Pin20.
P.27 [EC+KBC(NPCE783L)]NC U216 Pin4 and connect BT_ON to U4A Pin27.
P.27 [EC+KBC(NPCE783L)]NC U216 Pin5/Pin6 and connect AC_OFF/EC_PWRLIMIT_CTRL to U4A Pin119/Pin120.
P.27 [EC+KBC(NPCE783L)]Del R5855/R5856/C6201/C6202.
P.27 [EC+KBC(NPCE783L)]Connect AC_Present to U4A Pin124.
P.27 [EC+KBC(NPCE783L)]Del U216/R5857/C6203.
P.22 [CRT]Del F2 for MOR comment.
P.51 [AUDIO (CODEC)*]Del U_R5773/U_Q64/U_R5771/U_R5783/U_U215/U_R5784 for MOR comment.
P.51 [AUDIO (CODEC)*]Move U_AMP_PD# to U_U18 Pin4.
P.52 [AUDIO (MUTE)*]Mount U_R352/U_R351/U_Q17/U_R349/U_Q15/U_R341 for MOR comment.
P.22 [CRT]NC R5752 for no need of semi-PNP function.

(2009/09/12)

P.01 [Index page]Update information.
P.02 [BLOCK DIAGRAM]Update information.
P.10 [PCH (HDA,JTAG,SAT)]Update SPI ROM information.
P.37 [eSATA Combo Conn.]Del F10 for no need.
P.25 [LVDS Connector]Add F16/L83 to follow M870.
P.10 [PCH (HDA,JTAG,SAT)]Add 100K pull-low resistors R5966/R5867/R5968 on SPI0_MOSI/SPI0_CLK/SPI0_CS# for Intel EDS request.
P.07 [ARD (GRAPHICS POWER)]Change R401 to 1R-0000103-J200.
P.15 [PCH (GPIO,VSS_NCTF,RSVD)]Change R943/R974/R982/R1626 to 1R-0000103-J200.
P.52 [AUDIO (MUTE)*]Change U_R340/U_R350/U_R663 to 1R-0000103-J200.
P.51 [AUDIO (CODEC)*]Change U_R652/U_R662 to 1R-0000103-J200.
P.40 [Camera Connector]Add R5969/F17 for adding fuse solution.
P.25 [LVDS Connector]NC CN13 Pin1/Pin5/Pin6 for del EDID function.
P.13 [PCH (LVDS,DDI)]Del L_DDC_CLK/L_DDC_DATA for del EDID function.
P.20 [DDRIII(SO-DIMM_0) 1/2]NC CAP13 for no need.
P.21 [DDRIII(SO-DIMM_1) 2/2]NC CAP22 for no need.
P.37 [eSATA Combo Conn.]Swap L62/L66 for layout request.

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(2009/09/12)

P.51 [AUDIO (CODEC)*]Change the setting to ALC269
(NC: U_C441/R5943/U_R5789, Stuff U_C930/R5944/U_R5790).
P.59 [DCIN&Charger]Change PL3 to NC for costdown.
P.63 [VTT&PCH Power(+1_05V)]Change PR44 from 0ohm to 2.2ohm
for vendor suggest.
P.64 [DDR3 Power (+1_5V/+0_75V)]Change PR39 from 0ohm to 2.2ohm
for vendor suggest.

P.45 [Touch Pad]Del F12 for no need.
P.23 [LVDS]Update Panel ID information.
P.51 [AUDIO (CODEC)*]Change U_C787/U_C476/U_C459 to 1C-2B20103-K200
for MOR comment to use the same kind of Capacitor.
P.65 [SYS Power(+1_8V)]Change PC247 to 1C-2B20103-K200 for MOR comment
to use the same kind of Capacitor.
P.53 [AUDIO (Power)*]Change U_C467 to 1C-2B20103-K200 for MOR comment
to use the same kind of Capacitor.
P.38 [PCIE (MS) 1/2]Change R5911/R5912/R5909/R5910/R5913/R5914/R5915/R5916/R5917
to 33ohm for correcting SI test fail.
P.39 [PCIE (SD) 2/2]Change R5918/R5919/R5920/R5921/R5922
to 33ohm for correcting SI test fail.

(2009/09/13)

P.22 [CRT]Change CN20 to DZ11A91-SB281-4H for different package.
P.56 [AUDIO (Ext MIC Jack)*]Change U_CN5 to JA63331-R1T0-7H for ME request.

(2009/09/14)

P.63 [VTT&PCH Power(+1_05V)]Del PJ23 for layout space lack.
P.33 [LAN (88E8059) 1/2]Change C995 to 10uF for Marvell comment.
P.62 [SYS Power (+3_3V/+5V)] Change PR122/PR201 to 2.2 ohm for RF noise.
P.66 [CPU Power_VHCORE] Change PR563 to NC, change PU28 pin25 connect
to PROCHOT# for design change.
P.04 [ARD (CLK,MISC,JTAG)]Add off-page PROCHOT#.
P.42 [Felica Connector]NC R5963/F15, stuff C869/U48/R630/C845/R5964
for Felica fuse solution fail.
P.37 [eSATA Combo Conn.]Add R5971/R5972/R5973/R5974 to reduce the trace length
on U214 for vendor request.

(2009/09/15)

P.11 [PCH (PCI-E,SMBUS,CLK)]Make R902/R903 from +3VRUN pull-high
to +3VALW pull-high for Intel recommendation.
P.26 [HDMI]Change CN21 to DF03-577-1931.

(2009/09/16)

P.14 [PCH (PCI,USB,NVRAM)]NC R1466 for Intel Braidwood disable guideline.

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(2009/11/4)

P.07 [ARD (GRAPHICS POWER)] Delete PJ43 for redundant design of
EVT & DVT
P.22 [CRT] Add F18 for current limit by MOR comment
P.62 [SYS Power (+3_3V/+5V)] Delete PJ11 and PJ12 for redundant
design of EVT & DVT
P.64 [DDR3 Power(+1_5V/+0_75V)] Delete PJ26 and PJ27 for redundant
design of EVT & DVT
P.65 [SYS Power(+1_8V)] Delete PJ36 for redundant design of
EVT & DVT
P.66 [CPU Power_VHCORE] Change PC112 from 68u_25V to OS_Con cap 47u_25V
P.68 [VGFX Power_GFXCORE] Delete PJ33 for redundant
design of EVT & DVT

(2009/11/12)

P.27 [EC+KBC(NPCE783L)] Add R5975 on OVT_EC# for GPIO70
need pull high
P.50 [SWITCH (Botton & KB LED)*] Exchange function name for Assist &
Web button
P.23 [LVDS] No mount R5942 to cancell Instant_On function by MOR request
P.27 [EC+KBC(NPCE783L)] No mount R5851 to cancell Instant_On function
by MOR request
P.43 [Status LED & LID] R689 change resistor value to 300 Ohm, R692 change
resistor value to 909 Ohm, R693 change value to 300 Ohm, R5945~R5947
change resistor value to 392 Ohm for LED brightness by MOR request
P.25 [LVDS Connector] Change CN13 to 1N-004000E-FKG0 for better L6 process
P.28 [KB Connector] Add TP1233,TP1234 for BFT test
P.23 [LVDS] Add TP1231,TP1232 for BFT test
P.39 [PCIE(SD) 2/2] Add TP1235,TP1236 for BFT test
P.45 [Touch Pad] Add TP1241~TP1246 for BFT test
P.42 [Felica Connector] Add TP1237~TP1240 for BFT test

(2009/11/16)

P.59 [DCIN&Charger] change pc126 from 1000P_50V_0603_X7R to 1000pF_50V_0402_X7R
for MOR request
P.66 [CPU Power_VHCORE] change pc253 from 1000P_16V_0402_X7R to
1000pF_50V_0402_X7R for MOR request
P.70 [OVP protection] change pc41 from 1000P_16V_0402_X7R to 1000pF_50V_0402_X7R
for MOR request
P.61 [Identify IC] Update PU5 schematic symbol
P.10 [PCH (HDA,JTAG,SAT)] Update U43 schematic symbol
P.61 [Identify IC] Update PU5 schematic symbol
P.40 [Camera Connector] L76,L77 change to Bead,MAX ECHO,EBMS100505A121 0.5A,
120ohm/100MHz,25%,0402(1005mm) by MOR request
P.55 [Audio (Head Phone Jack)*] U_L4,U_L5 change to Bead, MAX ECHO,
EBMS100505A121 0.5A,120ohm/100MHz,25%,0402(1005mm) by MOR request
P.33 [LAN (88E8059) 1/2] C6077 change to SMD,MLCC,X7R,1000pF,50V,10%,0402
by MOR request
P.51 [AUDIO (CODEC)*] U_C440 change to SMD,MLCC,X7R,1000pF,50V,10%,0402
by MOR request
P.34 [LAN (Transformer) 2/2] C568 change to SMD,MLCC,X7R,1000pF,50V,10%,0402
by MOR request
P.45 [Touch Pad] C130,C133 change to SMD,MLCC,NPO,47pF,50V,5%,0402
by MOR request
P.27 [EC+KBC(NPCE783L)] C22 change to SMD,MLCC,NPO,22pF,50V,5%,0402
by MOR request
P.38 [PCIE (MS) 1/2] C544,C785,C786 change to SMD,MLCC,NPO,22pF,50V,5%,0402
by MOR request
P.51 [AUDIO (CODEC)*] U_C439 change to SMD,MLCC,NPO,22pF,50V,5%,0402
by MOR request
P.52 [AUDIO (MUTE)*] U_R351 change to SMD,RES,200K,1/16W,5%,0402
by MOR request
P.52 [AUDIO (MUTE)*] U_R352 change to SMD,RES,33K,1/16W,5%,0402
by MOR request
P.52 [AUDIO (MUTE)*] U_R341,U_R349, change to SMD,RES,10K,1/16W,5%,0402
by MOR request
P.10 [PCH (HDA,JTAG,SAT)] R5905, change to SMD,RES,51ohm,1/16W,5%,0402
by MOR request
P.27 [EC+KBC(NPCE783L)] RP1,RP20,RP90 change to SMD,RES,10K,1/16W,5%,0402
and locations are R5984,R5985 & R5976~R5979 by MOR request

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(2009/11/16)

P.27 [EC+KBC(NPCE783L)] RP21, change to SMD,RES,2.2K,1/16W,5%,0402
and locations are R5982,R5983 by MOR request
P.27 [EC+KBC(NPCE783L)] RP22, change to SMD,RES,4.7K,1/16W,5%,0402
and locations are R5980,R5981 by MOR request
P.31 [Express Card] Update U42 Schematic symbol
P.43 [Status LED & LID] Change TP1224~TP1230 to TOP for BFT test

(2009/11/17)

P.71 [HOLE & AMI LABEL] Add BOSS2 for M960 wireless card use only
P.32 [Mini-PCIE Card (WLAN)] Add TP1235~TP1238 on BT_WLAN_SW# &
GND for BFT test
P.33 [LAN (88E8059) 1/2] LAN chip 88E8059 change packing method to
tapping for better L6 process
P.23 [LVDS] SW1 change from 12-pin to 8-pin panel ID SW
P.15 [PCH (GPIO,VSS_NCTF,RSVD)] NC_R5933 & move R5941 from P.23
to P.15
P.27 [EC+KBC(NPCE783L)] Move R5942 from P.23 to P.27

(2009/11/18)

P.45 [Touch Pad] Add F12 for cable short test fail
P.23 [LVDS] Add test point from TP1251~TP1260 for panel ID switch BFT test
P.43 [Status LED & LID)] Change U21 to E-CMOS EC2618NLB1GR for distance can't
meet MOR spec

(2009/11/19)

P.11 [PCH (PCI-E,SMBUS,CLK)] Reserve R5984~R5992 for Intel FCIM function
P.64 [DDR3 Power(+1_5V/+0_75V)] Add L84 (3A/120ohm/100MHz,25%,0805) and
PR662 2.2ohm, change PR39 from 2.2ohm to 0ohm for EMI request
P.66 [CPU Power_VHCORE] Change PR554 and PR558 from 0ohm to 2.20hm for
EMI request
P.68 [VGFX Power_GFXCORE] Add test point TP509 for low MB GFXCORE voltage
SMT power test request

(2009/11/20)

P.15 [PCH]Change R5941 to mount for Panel ID setting requirement
P.52 [Audio(Mute)]Change U_R364 from 33kohm to 3.3kohm for satisfy hFE under
100 as MOR's suggestion.
P.33 [LAN]Change R84 from 4.7kohm to 0ohm for vendor modification

(2009/11/21)

P.57 [Audio (USB)*]Change the footprint of U_CN2,U_CN3,U_CN6 as SMT suggestion.
P.30 [Debug Port]Add C6347 for EMI request.
P.16 [PCH(POWER)]Change C6336,C6337,C6338 from 680p to 2200p and change to mount
for EMI request.
P.54 [AUDIO]Add C6348 for EMI request.
P.33 [LAN]Add C6349 for EMI request.
P.34 [LAN]Change L47 from 100R to 300R for EMI request.
P.59 [DCIN&Charger]: Dcbatout Add PC574 0.1uf,PC575 0.1uf,PC576 4700pf ,
PC577 4700pf for EMI request,
BT+ add PC580 0.1uf,PC581 0.1uf,PC582 4700pf ,PC583 4700pf for EMI request
P.66 [CPU Power_VHCORE]:change PC151 and PC156 from NC to mount 0.1uf
for EMI request

(2009/11/22)

P.48 [Audio]Add C6350~C6353 for speaker noise issue.
P.10 [PCH]Add C6354,C6355 and NC them, reserve for EMI request.
P.51 [AUDIO]NC U_C439 and add U_C931(NC) for EMI request.
P.43 [LED]Change R5945,R5946,R5947 from 392ohm to 649ohm and R390 from
120ohm to 261ohm as DQA&ME request.
P.51 [Audio]Change U_R668,U_R665,U_R660,U_R670,U_R672,U_R659(22ohm)
from 0402 to 0201 for implement ME solution and layout space is not enough.
And change U_R667,U_R664(33kohm), and R5943(NC),R5944(0ohm),
and U_R339(20kohm), and U_R338(39.2kohm), and U_R652,U_662(10kohm)
from 0402 to 0201 for implement ME solution and layout space is not enough.

(2009/11/22)

P.64 [DDR3 Power]Delete PC40 for layout space concern.

(2009/11/23)

P.69 [Other power plane]Change PR661 from 0603 to 0402 for MOR request
to cost down.
P.15 [PCH]Delete RP19 and add R5993,R5994,R5995 for MOR request to cost down.
P.40 [Camera]Change C9 from 1C-2Y70106-Y001 to 1C-2Y70106-Y000 for MOR request
to cost down.
P.52 [Audio]Change U_Q20 form 2N7002W to SRK7002 for ESD issue.
P.71 [HOLE]Change H30,H29,H8,H10,H4 hole size as ME's request.
P.22 [CRT]Change CN20 from FOX_DZ11A91-SB281-4H to FOX_DZ11AE1-SB1SD-4H
as ME's request.
P.49 [Audio/USB DB CONN]Change CN31 from FOX_GB5RF500-1203-7H to
FOX_GB5RF500-1203-8H for ME's request.
P.54 [Audio (Audio/USB CONN)*]Change U_CN1 from FOX_GB5RF500-1203-7H to
FOX_GB5RF500-1203-8H as ME's request.
P.42 [Felica]Change CN7 from FOX_GB5RF060-1203-7H to
FOX_GB5RF060-1203-8F as ME's request.
P.45 [TouchPad]Change CN8 from FOX_GB5RF060-1203-7H to
FOX_GB5RF060-1203-8F as ME's request.
P.10 [PCH]Change C6354 from 0.1uF to 33pF(mount) and R618 from 33ohm
to 47ohm as EMC request.
P.51 [Audio]Change U_R661,U_R671,U_R676,U_673,U_R321 from 0402 to 0201 for
layout space concern.

(2009/11/24)

P.23 [LVDS]Change SW1 from DHNF-04-T-Q-T-R_SW-SMD8P to
DHNF-06-T-Q-T/R_SW-SMD12 for shortage issue.

(2009/11/28)

P.16 [PCH]Change C6336,C6337,C6338 from 1C-2B30222-K000 to 1C-2B30222-M000
for PUR's suggestion.
P.34 [LAN]Change L47 from 1L-BACMS16-0809 to 1L-BTB1608-080D for PUR's suggestion.
P.30 [Debug Port]NC CN30 for EMC solution.
P.29 [SPI Flash ROM]NC U3,R43,C20 and mount R775 for EMC solution.
P.68 [VGFX Power_GFXCORE]:change PR609 to 470ohm for Intel
(#3622146 A Voltage Spike on Graphics Core Rail (Vaxg) to 1.5V seen during
System shutdown) request.

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(2009/12/22)

P.26 [HDMI] Mount R5888 to fix HDMI issue by MOR request
P.64 [DDR3 Power(+1_5V/+0_75V)] Mount PQ59, change PR600 resistor to 0 Ohm &
no mount PR145 to change the enable signal to RUN_PWRGD by MOR request.
P.26 [HDMI] Change CN21 symbol from 2N-0019007-MKG0 to 2N-0019003-MKG0
to improve factory process

(2009/12/23)

P.71 [HOLE & AMI LABEL] Mount AMI label for AMI certifcate
P.10 [PCH (HDA,JTAG,SAT)] No mount CN18, U43, C815, R542 & Mount R1551 for
needless in MP
P.52 [AUDIO (MUTE)*] Change U_Q15 with ESD protection for factory ESD issue

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(2009/12/24)

P.71 [HOLE & AMI LABEL]Delete BOSS2 for needless from ME's request
P.34 [LAN(Transformer)]Change L70 from LANKOM to DELTA for LANKOM transformer issue in PVT
P.33 [LAN]Add R5997 reserve for 8057 solution
P.04 [ARD]Delete R937,R930 for MOR's request
P.06 [ARD]Delete R860 for MOR's request
P.27 [EC]Delete R39,R46 for MOR's request
P.32 [Mini-PCIE Card]Delete R5901 for MOR's request
P.45 [Touch Pad]Delete R5869,R5868 for MOR's request

(2009/12/28)

P.10 [PCH]Change R618 from 47ohm to 68ohm and Change C6355 from NC_0.1uF to mount 22pF for EMC audio FFC issue
P.51 [Audio]Change U_R326 from 22ohm to 0ohm for EMC audio FFC issue

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