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**DVT2 BOM Control Table**

VALUE Head	CA_	AT_	M86_	M82_	NC_
<b>UMA</b>	Stuff	Un-stuff	Un-stuff	Un-stuff	Un-stuff
Discrete VGA with M86	Un-stuff	Stuff	Stuff	Un-stuff	Un-stuff
Discrete VGA with M82	Un-stuff	Stuff	Un-stuff	Stuff	Un-stuff

Project Code & Schematics Subject: M760 Main Board      PCB P/N: FUBAI 1P-0083101-8010)  
HANNSTAR (1P-0083500-8010)  
IRIS (1P-0083J01-8010)

P. Leader	Check by	Design by
JERRY HSIAO	JERRY HSIAO	TONY CHENG

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

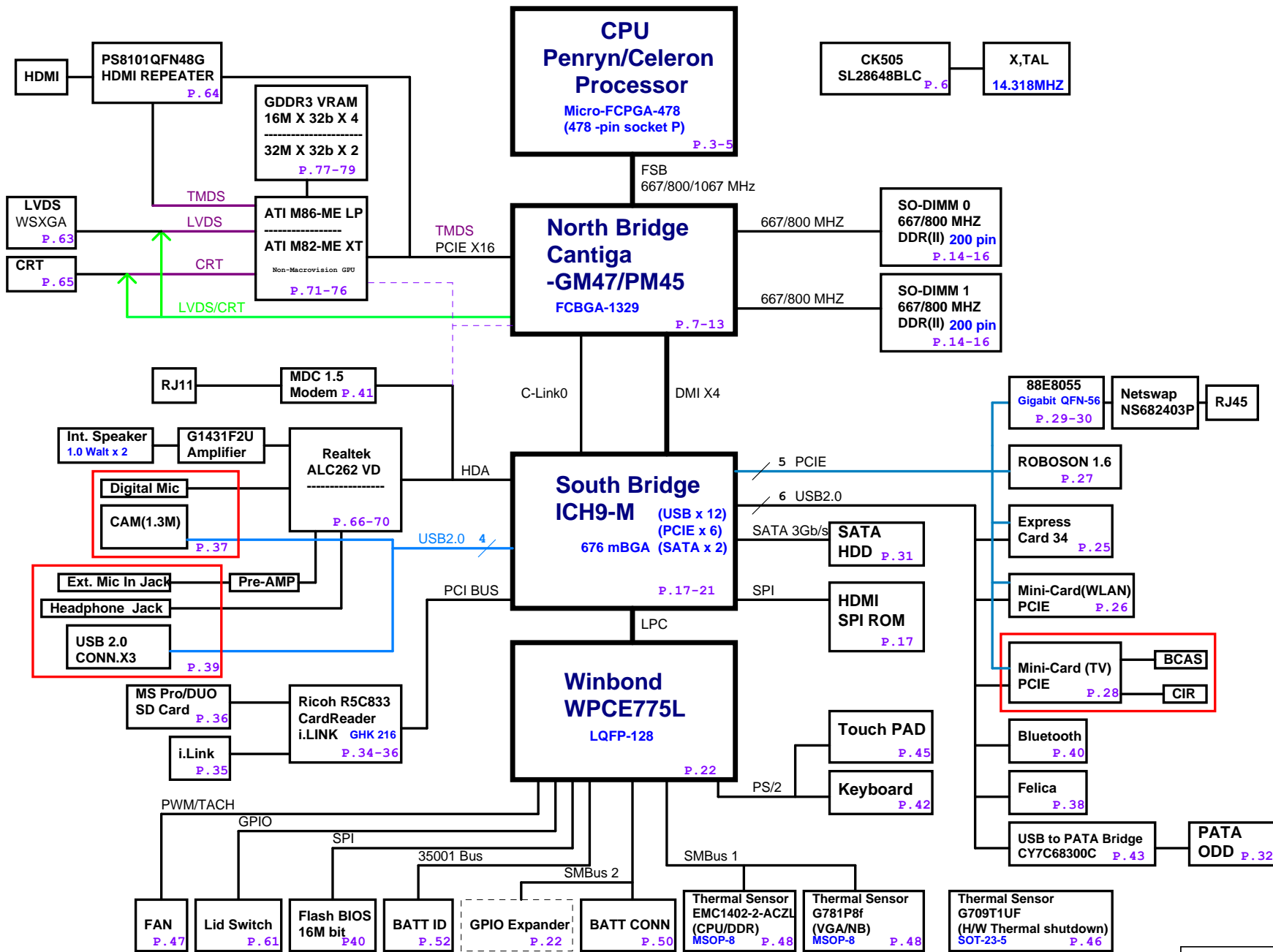
Title: **Index Page**

Size: Document Number      Rev: 1.0

Custom: **M760**

Date: Thursday, March 27, 2008      Sheet 1 of 89

# M760 (IRX-4370) Montevina + M86-LP/M82-XT



TI CHARGER	
BQ24751 P.63	
INPUTS	OUTPUTS
DC_IN	BT+ DCBATOUT

SYSTEM DC/DC	
TPS51125RGER P.64	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC +15V_ALW

SYSTEM DC/DC	
SC411 P.65	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VRUN

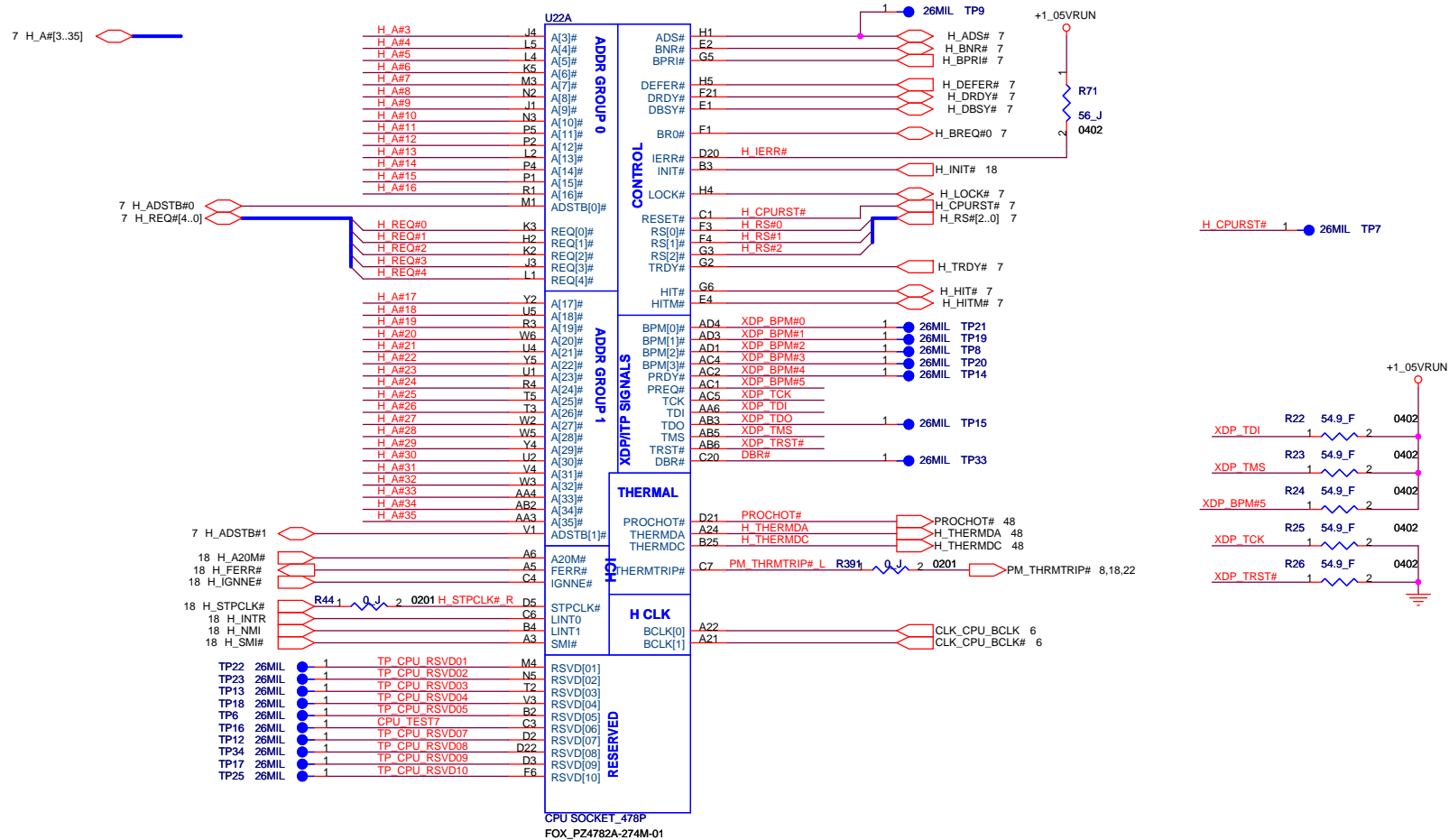
SYSTEM DC/DC	
TPS51116RGER P.66	
INPUTS	OUTPUTS
DCBATOUT	+1_8VSUS +0_9VSUS

CPU DC/DC	
ISL6266A P.67	
INPUTS	OUTPUTS
DCBATOUT	VHCCORE

SYSTEM DC/DC	
APL5912 P.70	
INPUTS	OUTPUTS
+1_5VRUN	PEX_VDD

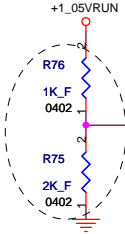
SYSTEM DC/DC	
SC411 P.70	
INPUTS	OUTPUTS
DCBATOUT	NV_VDD

SYSTEM DC/DC	
MAX8776 P.71	
INPUTS	OUTPUTS
DCBATOUT	+VGF_X_CORE



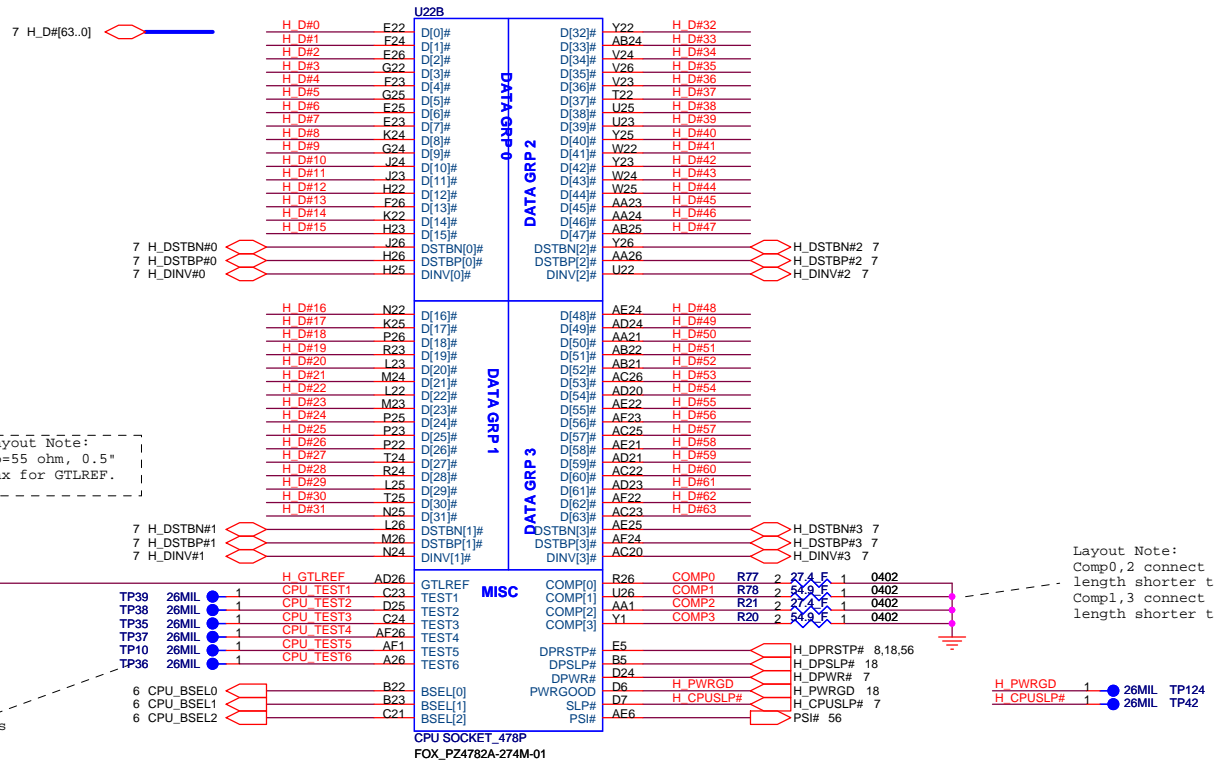
Place close to CPU

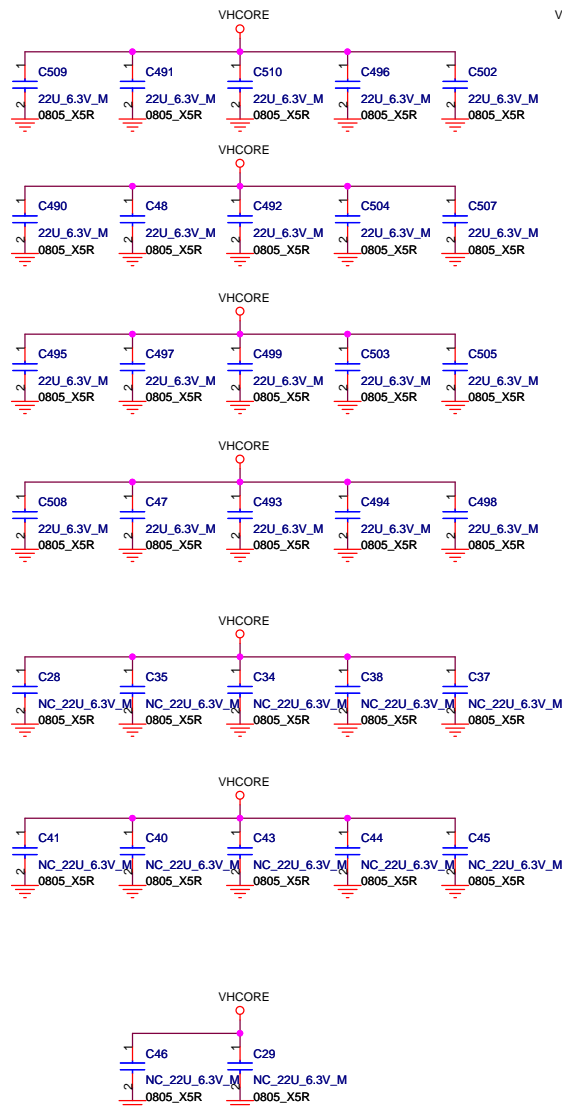
2K ohm for Dual-Core ;  
1.74K ohm for Quad-Core



Route the TEST3 and TEST5 signals through a ground referenced Zo = 55-ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection. TEST4 and TEST6 and TEST7 pins can be left NC.

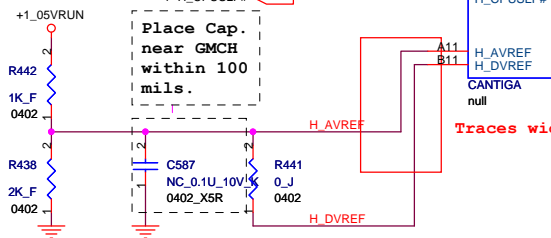
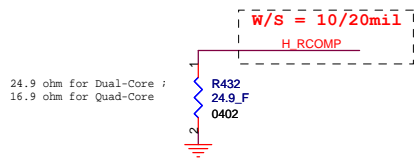
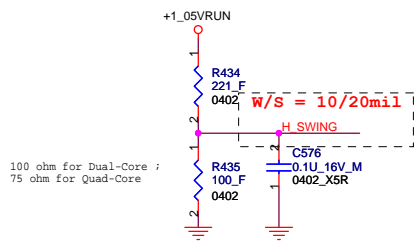
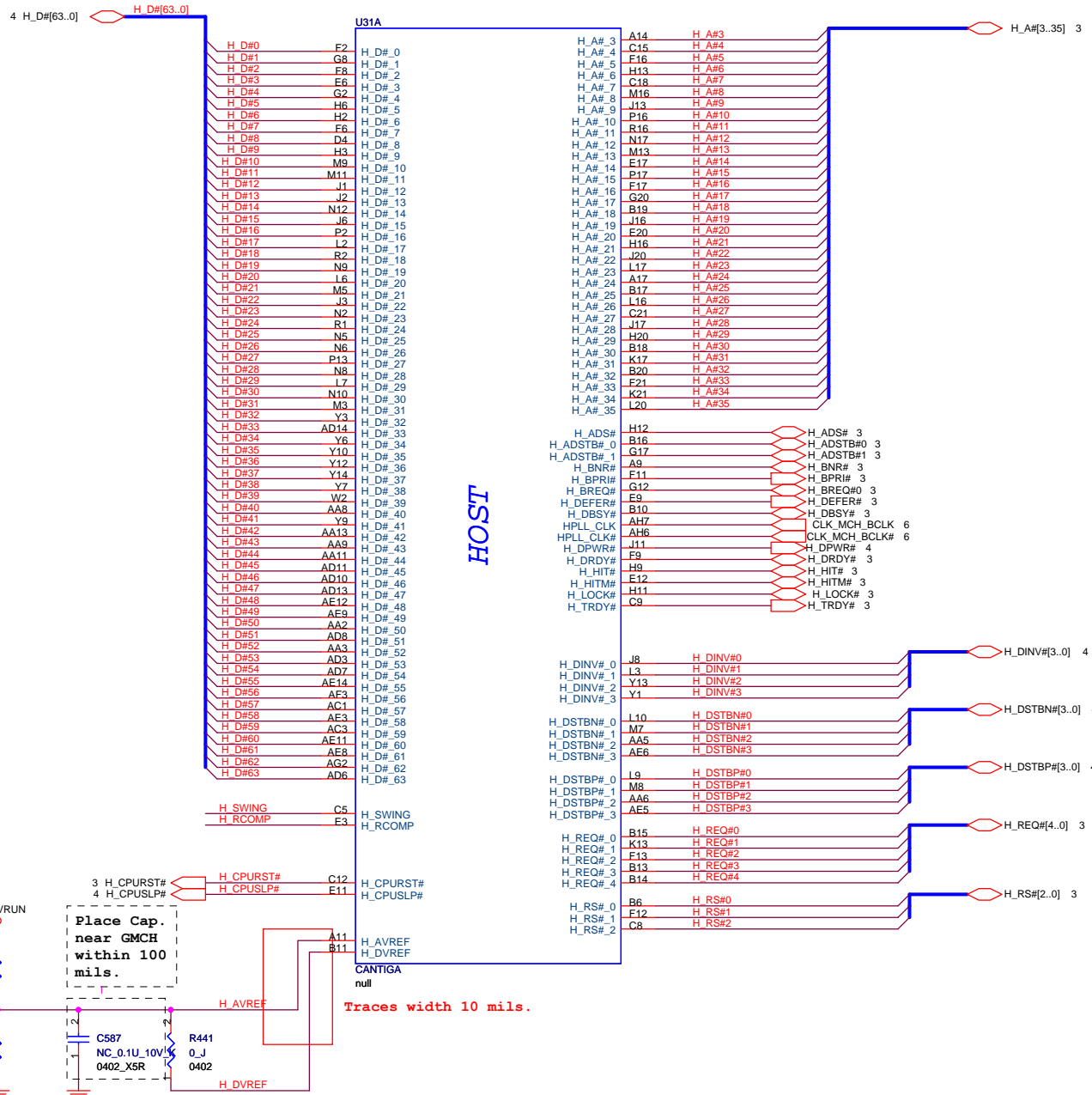
Layout Note:  
Zo=55 ohm, 0.5" max for GTLREF.





Pin	Signal	Signal	Signal
A7	VCC[001]	VCC[068]	AB20
A9	VCC[002]	VCC[069]	AB7
A10	VCC[003]	VCC[070]	AC7
A11	VCC[004]	VCC[071]	AC9
A12	VCC[005]	VCC[072]	AC12
A15	VCC[006]	VCC[073]	AC13
A17	VCC[007]	VCC[074]	AC15
A18	VCC[008]	VCC[075]	AC17
A20	VCC[009]	VCC[076]	AC18
B7	VCC[010]	VCC[077]	AD7
B9	VCC[011]	VCC[078]	AD9
B10	VCC[012]	VCC[079]	AD10
B12	VCC[013]	VCC[080]	AD12
B14	VCC[014]	VCC[081]	AD14
B15	VCC[015]	VCC[082]	AD15
B17	VCC[016]	VCC[083]	AD17
B18	VCC[017]	VCC[084]	AD18
B20	VCC[018]	VCC[085]	AE9
C9	VCC[019]	VCC[086]	AE10
C10	VCC[020]	VCC[087]	AE12
C12	VCC[021]	VCC[088]	AE13
C13	VCC[022]	VCC[089]	AE15
C15	VCC[023]	VCC[090]	AE17
C17	VCC[024]	VCC[091]	AE18
C18	VCC[025]	VCC[092]	AE20
D8	VCC[026]	VCC[093]	AF9
D10	VCC[027]	VCC[094]	AF10
D12	VCC[028]	VCC[095]	AF12
D14	VCC[029]	VCC[096]	AF14
D15	VCC[030]	VCC[097]	AF15
D17	VCC[031]	VCC[098]	AF17
D18	VCC[032]	VCC[099]	AF18
E7	VCC[033]	VCC[100]	AF20
E9	VCC[034]		
E10	VCC[035]	VCCP[01]	G21
E12	VCC[036]	VCCP[02]	V6
E13	VCC[037]	VCCP[03]	J6
E17	VCC[038]	VCCP[04]	K6
E18	VCC[039]	VCCP[05]	M6
E20	VCC[040]	VCCP[06]	J21
F7	VCC[041]	VCCP[07]	K21
F8	VCC[042]	VCCP[08]	M21
F9	VCC[043]	VCCP[09]	N21
F10	VCC[044]	VCCP[10]	R21
F14	VCC[045]	VCCP[11]	R6
F15	VCC[046]	VCCP[12]	T21
F17	VCC[047]	VCCP[13]	T6
F18	VCC[048]	VCCP[14]	T7
F20	VCC[049]	VCCP[15]	V21
F21	VCC[050]	VCCP[16]	W21
AA9	VCC[051]		
AA10	VCC[052]	VCCA[01]	B26
AA12	VCC[054]	VCCA[02]	C26
AA13	VCC[055]		
AA15	VCC[056]		
AA17	VCC[057]		
AA18	VCC[058]		
AA20	VCC[059]		
AB9	VCC[060]		
AC10	VCC[061]		
AB10	VCC[062]		
AB12	VCC[063]		
AB14	VCC[064]		
AB15	VCC[065]		
AB17	VCC[066]		
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	VCCP[02]		





MCH_CFG_0-2 FSB Frequency	000 = FSB1066 ; 010 = FSB800; 011 = FSB667 ; Others = Reserved
MCH_CFG_3-4	Reserved
MCH_CFG_5 DMI X2 Select	Low = DMI X2 High = DMI X4 (Default)
MCH_CFG_6 ITPM Host Interface	Low =The ITPM Host Interface is enabled2 High = The ITPM Host Interface is disabled (default)
MCH_CFG_7 Intel Management Engine Crypto Transport Layer Engine Crypto Strap	Low = Intel Management Engine Crypto Transport Layer Security (TLS) cipher suite with no confidentiality High = Intel Management Engine Crypto TLS cipher suite with confidentiality (default)
MCH_CFG_8	Reserved
MCH_CFG_9 PCIe Graphics Lane	Low = Reverse Lane High = Normal operation
MCH_CFG_10 PCIe Loopback enable	Low = Enabled3 High = Disabled (default)
MCH_CFG_11	Reserved
MCH_CFG_12 ALLZ	Low = ALLZ mode enabled3 High = Disabled (default)
MCH_CFG_13 XOR	Low = XOR mode enabled3 High = Disabled (default)
MCH_CFG_14-15	Reserved
MCH_CFG_16 FSB Dynamic ODT	Low = Dynamic ODT disabled High = Dynamic ODT enabled (default)
MCH_CFG_17-18	Reserved
MCH_CFG_19 DMI Lane Reversal	Low = Normal operation (Default): Lane Numbered in Order High = Reverse Lanes DMI x4 mode [(G)MCH->ICH]: (3->0, 2->1, 1->2 and 0->3) DMI x2 mode [(G)MCH ->ICH]: (3->0, 2->1)
MCH_CFG_20 Digital Display Port (SDVO/DP/iHDMI) and Concurrent with PCIe	Low = Only digital display port (SDVO/DP/iHDMI) or PCIe is operational (default) High = Digital display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via the PEG port

U31B

- X M36
- X N36
- X R33
- X T33
- X AH9
- X AH10
- X AH12
- X AH13
- X K12
- X AL34
- X AK34
- X AN35
- X AM35
- X T24
- X B31
- X B2
- X M1
- X AY21
- X BG23
- X BF23
- X BH18
- X BF18

- X BG23
- X BF23
- X BH18
- X BF18

- T25
- R25
- P25
- P20
- C25
- N24
- M24
- C23
- C24
- N21
- P21
- T21
- R20
- M20
- L21
- P29
- C28
- R28
- T28
- C23
- R29
- N33
- P32
- AT40
- AT11
- R32

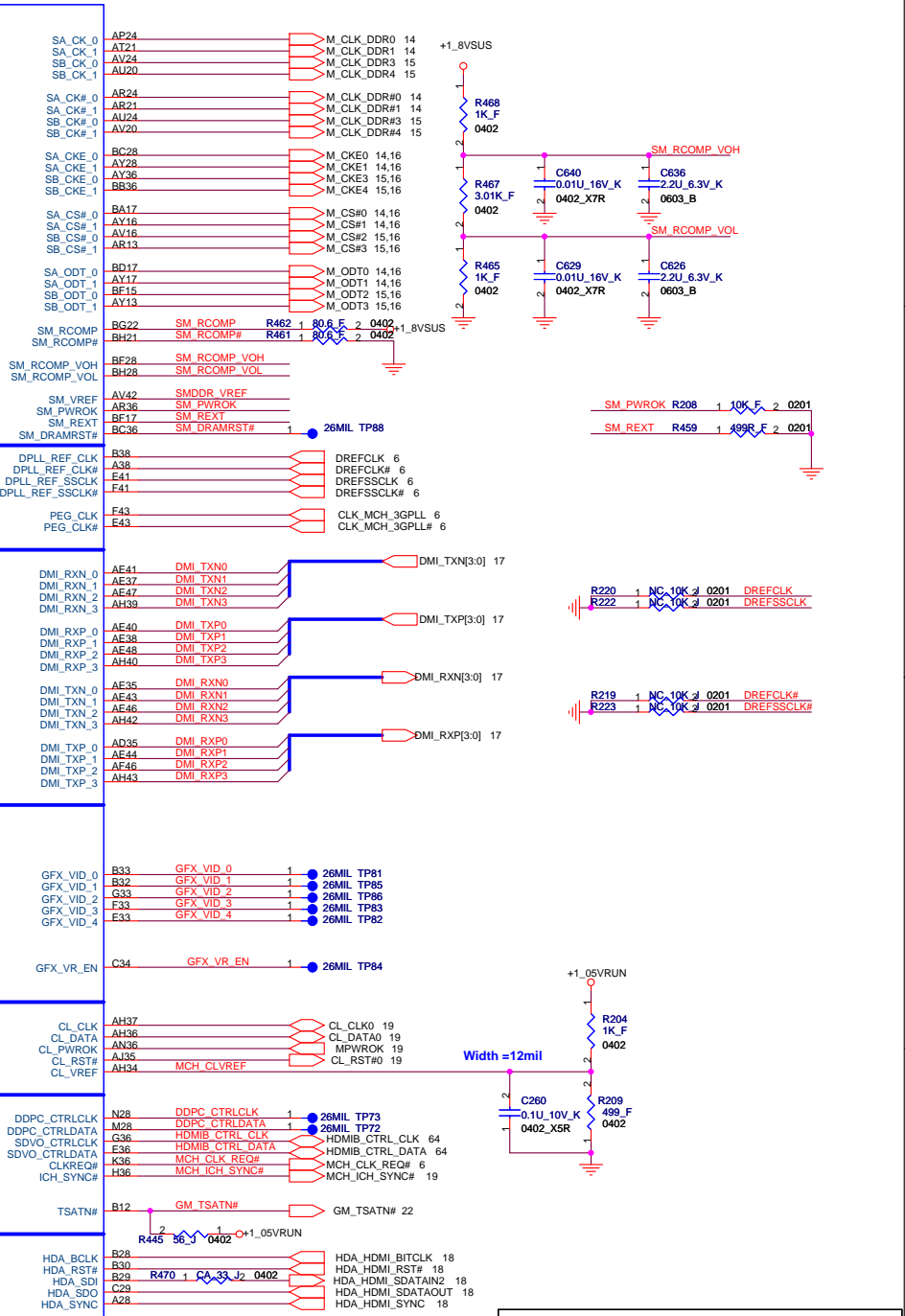
- R29
- N33
- P32
- AT40
- AT11
- R32

- NC\_1
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- NC\_4
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- NC\_18
- NC\_19
- NC\_20
- NC\_21
- NC\_22
- NC\_23
- NC\_24
- NC\_25
- NC\_26

CANTIGA

null

CLASS  
DDR CLK/ CONTROL/ COMPENSATION  
CLK  
DMI  
ME  
MISC  
HDA







14 M\_A\_DQ[63..0]

M_A_DQ0	AJ38	SA_DQ_0
M_A_DQ1	AJ41	SA_DQ_1
M_A_DQ2	AN38	SA_DQ_2
M_A_DQ3	AM38	SA_DQ_3
M_A_DQ4	AJ36	SA_DQ_4
M_A_DQ5	AJ40	SA_DQ_5
M_A_DQ6	AM44	SA_DQ_6
M_A_DQ7	AM42	SA_DQ_7
M_A_DQ8	AN43	SA_DQ_8
M_A_DQ9	AN44	SA_DQ_9
M_A_DQ10	AU40	SA_DQ_10
M_A_DQ11	AT38	SA_DQ_11
M_A_DQ12	AN41	SA_DQ_12
M_A_DQ13	AN39	SA_DQ_13
M_A_DQ14	AU44	SA_DQ_14
M_A_DQ15	AU42	SA_DQ_15
M_A_DQ16	AV39	SA_DQ_16
M_A_DQ17	AY44	SA_DQ_17
M_A_DQ18	BA40	SA_DQ_18
M_A_DQ19	BD43	SA_DQ_19
M_A_DQ20	AV41	SA_DQ_20
M_A_DQ21	AY43	SA_DQ_21
M_A_DQ22	BB41	SA_DQ_22
M_A_DQ23	BC40	SA_DQ_23
M_A_DQ24	AY37	SA_DQ_24
M_A_DQ25	BD38	SA_DQ_25
M_A_DQ26	AV37	SA_DQ_26
M_A_DQ27	AT36	SA_DQ_27
M_A_DQ28	AY38	SA_DQ_28
M_A_DQ29	BB38	SA_DQ_29
M_A_DQ30	AV36	SA_DQ_30
M_A_DQ31	AW36	SA_DQ_31
M_A_DQ32	BD13	SA_DQ_32
M_A_DQ33	AU11	SA_DQ_33
M_A_DQ34	BC11	SA_DQ_34
M_A_DQ35	BA12	SA_DQ_35
M_A_DQ36	AU13	SA_DQ_36
M_A_DQ37	AV13	SA_DQ_37
M_A_DQ38	BD12	SA_DQ_38
M_A_DQ39	BC12	SA_DQ_39
M_A_DQ40	BD9	SA_DQ_40
M_A_DQ41	BA9	SA_DQ_41
M_A_DQ42	AU10	SA_DQ_42
M_A_DQ43	AV9	SA_DQ_43
M_A_DQ44	BA11	SA_DQ_44
M_A_DQ45	BD9	SA_DQ_45
M_A_DQ46	AY8	SA_DQ_46
M_A_DQ47	BA6	SA_DQ_47
M_A_DQ48	AV5	SA_DQ_48
M_A_DQ49	AV7	SA_DQ_49
M_A_DQ50	AT9	SA_DQ_50
M_A_DQ51	AN8	SA_DQ_51
M_A_DQ52	AU5	SA_DQ_52
M_A_DQ53	AU6	SA_DQ_53
M_A_DQ54	AT5	SA_DQ_54
M_A_DQ55	AN10	SA_DQ_55
M_A_DQ56	AM11	SA_DQ_56
M_A_DQ57	AM5	SA_DQ_57
M_A_DQ58	AJ9	SA_DQ_58
M_A_DQ59	AJ8	SA_DQ_59
M_A_DQ60	AM12	SA_DQ_60
M_A_DQ61	AM13	SA_DQ_61
M_A_DQ62	AJ11	SA_DQ_62
M_A_DQ63	AJ12	SA_DQ_63

DDR SYSTEM MEMORY A

SA_BS_0	BD21	M_A_BS0	14,16
SA_BS_1	BG18	M_A_BS1	14,16
SA_BS_2	AT25	M_A_BS2	14,16
SA_RAS#	BB20	M_A_RAS#	14,16
SA_CAS#	BD20	M_A_CAS#	14,16
SA_WE#	AY20	M_A_WE#	14,16
SA_DM_0	AM37	M_A_DM0	14
SA_DM_1	AT41	M_A_DM1	
SA_DM_2	AY41	M_A_DM2	
SA_DM_3	AU39	M_A_DM3	
SA_DM_4	BB12	M_A_DM4	
SA_DM_5	AY6	M_A_DM5	
SA_DM_6	AT7	M_A_DM6	
SA_DM_7	AJ5	M_A_DM7	
SA_DQS_0	AJ44	M_A_DQS0	14
SA_DQS_1	AT44	M_A_DQS1	
SA_DQS_2	BA43	M_A_DQS2	
SA_DQS_3	BC37	M_A_DQS3	
SA_DQS_4	AW12	M_A_DQS4	
SA_DQS_5	BC8	M_A_DQS5	
SA_DQS_6	AU8	M_A_DQS6	
SA_DQS_7	AM7	M_A_DQS7	
SA_DQS#_0	AJ43	M_A_DQS#0	14
SA_DQS#_1	AT43	M_A_DQS#1	
SA_DQS#_2	BA44	M_A_DQS#2	
SA_DQS#_3	BD37	M_A_DQS#3	
SA_DQS#_4	AY12	M_A_DQS#4	
SA_DQS#_5	BD8	M_A_DQS#5	
SA_DQS#_6	AU9	M_A_DQS#6	
SA_DQS#_7	AM8	M_A_DQS#7	
SA_MA_0	BA21	M_A_A0	14,16
SA_MA_1	BC24	M_A_A1	
SA_MA_2	BG24	M_A_A2	
SA_MA_3	BH24	M_A_A3	
SA_MA_4	BG25	M_A_A4	
SA_MA_5	BA24	M_A_A5	
SA_MA_6	BD24	M_A_A6	
SA_MA_7	BG27	M_A_A7	
SA_MA_8	BF25	M_A_A8	
SA_MA_9	AW24	M_A_A9	
SA_MA_10	BC21	M_A_A10	
SA_MA_11	BH26	M_A_A11	
SA_MA_12	BH17	M_A_A12	
SA_MA_13	AY25	M_A_A13	
SA_MA_14			

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15 M\_B\_DQ[63..0]

M_B_DQ0	AK47	SB_DQ_0
M_B_DQ1	AH46	SB_DQ_1
M_B_DQ2	AP47	SB_DQ_2
M_B_DQ3	AP46	SB_DQ_3
M_B_DQ4	AJ46	SB_DQ_4
M_B_DQ5	AJ48	SB_DQ_5
M_B_DQ6	AM48	SB_DQ_6
M_B_DQ7	AP48	SB_DQ_7
M_B_DQ8	AU47	SB_DQ_8
M_B_DQ9	AU46	SB_DQ_9
M_B_DQ10	BA48	SB_DQ_10
M_B_DQ11	AY48	SB_DQ_11
M_B_DQ12	AT47	SB_DQ_12
M_B_DQ13	AR47	SB_DQ_13
M_B_DQ14	BA47	SB_DQ_14
M_B_DQ15	BC47	SB_DQ_15
M_B_DQ16	BC46	SB_DQ_16
M_B_DQ17	BC44	SB_DQ_17
M_B_DQ18	BG43	SB_DQ_18
M_B_DQ19	BF43	SB_DQ_19
M_B_DQ20	BE45	SB_DQ_20
M_B_DQ21	BC41	SB_DQ_21
M_B_DQ22	BF41	SB_DQ_22
M_B_DQ23	BF41	SB_DQ_23
M_B_DQ24	BG38	SB_DQ_24
M_B_DQ25	BF38	SB_DQ_25
M_B_DQ26	BH35	SB_DQ_26
M_B_DQ27	BG35	SB_DQ_27
M_B_DQ28	BH40	SB_DQ_28
M_B_DQ29	BG39	SB_DQ_29
M_B_DQ30	BG34	SB_DQ_30
M_B_DQ31	BH34	SB_DQ_31
M_B_DQ32	BH14	SB_DQ_32
M_B_DQ33	BG12	SB_DQ_33
M_B_DQ34	BH11	SB_DQ_34
M_B_DQ35	BG8	SB_DQ_35
M_B_DQ36	BH12	SB_DQ_36
M_B_DQ37	BF11	SB_DQ_37
M_B_DQ38	BF8	SB_DQ_38
M_B_DQ39	BG7	SB_DQ_39
M_B_DQ40	BC5	SB_DQ_40
M_B_DQ41	BC5	SB_DQ_41
M_B_DQ42	AY3	SB_DQ_42
M_B_DQ43	AY1	SB_DQ_43
M_B_DQ44	BF6	SB_DQ_44
M_B_DQ45	BF5	SB_DQ_45
M_B_DQ46	BA1	SB_DQ_46
M_B_DQ47	BD3	SB_DQ_47
M_B_DQ48	AV2	SB_DQ_48
M_B_DQ49	AU3	SB_DQ_49
M_B_DQ50	AR3	SB_DQ_50
M_B_DQ51	AN2	SB_DQ_51
M_B_DQ52	AY2	SB_DQ_52
M_B_DQ53	AV1	SB_DQ_53
M_B_DQ54	AP3	SB_DQ_54
M_B_DQ55	AR1	SB_DQ_55
M_B_DQ56	AL1	SB_DQ_56
M_B_DQ57	AL2	SB_DQ_57
M_B_DQ58	AJ1	SB_DQ_58
M_B_DQ59	AH1	SB_DQ_59
M_B_DQ60	AM2	SB_DQ_60
M_B_DQ61	AM3	SB_DQ_61
M_B_DQ62	AH3	SB_DQ_62
M_B_DQ63	AJ3	SB_DQ_63

DDR SYSTEM MEMORY B

SB_BS_0	BC16	M_B_BS0	15,16
SB_BS_1	BB17	M_B_BS1	15,16
SB_BS_2	BB33	M_B_BS2	15,16
SB_RAS#	AU17	M_B_RAS#	15,16
SB_CAS#	BG16	M_B_CAS#	15,16
SB_WE#	BF14	M_B_WE#	15,16
SB_DM_0	AM47	M_B_DM0	15
SB_DM_1	AY47	M_B_DM1	
SB_DM_2	BD40	M_B_DM2	
SB_DM_3	BF35	M_B_DM3	
SB_DM_4	BG11	M_B_DM4	
SB_DM_5	BA3	M_B_DM5	
SB_DM_6	AP1	M_B_DM6	
SB_DM_7	AK2	M_B_DM7	
SB_DQS_0	AL47	M_B_DQS0	15
SB_DQS_1	AV48	M_B_DQS1	
SB_DQS_2	BG41	M_B_DQS2	
SB_DQS_3	BG37	M_B_DQS3	
SB_DQS_4	BH9	M_B_DQS4	
SB_DQS_5	BB2	M_B_DQS5	
SB_DQS_6	AU11	M_B_DQS6	
SB_DQS_7	AN6	M_B_DQS7	
SB_DQS#_0	AL46	M_B_DQS#0	15
SB_DQS#_1	AV47	M_B_DQS#1	
SB_DQS#_2	BH41	M_B_DQS#2	
SB_DQS#_3	BH37	M_B_DQS#3	
SB_DQS#_4	BG9	M_B_DQS#4	
SB_DQS#_5	AT2	M_B_DQS#5	
SB_DQS#_6	AN5	M_B_DQS#6	
SB_DQS#_7			
SB_MA_0	AV17	M_B_A0	15,16
SB_MA_1	BA25	M_B_A1	
SB_MA_2	BC25	M_B_A2	
SB_MA_3	AU25	M_B_A3	
SB_MA_4	AW25	M_B_A4	
SB_MA_5	BB28	M_B_A5	
SB_MA_6	AU28	M_B_A6	
SB_MA_7	AW28	M_B_A7	
SB_MA_8	AT33	M_B_A8	
SB_MA_9	BD33	M_B_A9	
SB_MA_10	BB16	M_B_A10	
SB_MA_11	AW33	M_B_A11	
SB_MA_12	AY33	M_B_A12	
SB_MA_13	BH15	M_B_A13	
SB_MA_14	AU33	M_B_A14	

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U31I		U31J	
ALJ48	VSS_1	VSS_100	AM36
AR48	VSS_2	VSS_101	AE36
AL48	VSS_3	VSS_102	P36
BB47	VSS_4	VSS_103	L36
AW47	VSS_5	VSS_104	J36
AN47	VSS_6	VSS_105	F36
AF47	VSS_7	VSS_106	B36
AD47	VSS_8	VSS_107	AE21
AB47	VSS_9	VSS_108	AH35
Y47	VSS_10	VSS_109	AA35
T47	VSS_11	VSS_110	Y35
N47	VSS_12	VSS_111	U35
L47	VSS_13	VSS_112	T35
G47	VSS_14	VSS_113	BF34
BD46	VSS_15	VSS_114	AM34
BA46	VSS_16	VSS_115	AJ34
AY46	VSS_17	VSS_116	AF34
AV46	VSS_18	VSS_117	AE34
AR46	VSS_19	VSS_118	W34
AM46	VSS_20	VSS_119	Y20
V46	VSS_21	VSS_120	B34
R46	VSS_22	VSS_121	A34
P46	VSS_23	VSS_122	BG33
H46	VSS_24	VSS_123	F20
F46	VSS_25	VSS_124	BC33
BF44	VSS_26	VSS_125	BA33
AH44	VSS_27	VSS_126	AV33
AD44	VSS_28	VSS_127	AR33
AA44	VSS_29	VSS_128	AL33
Y44	VSS_30	VSS_129	AH33
U44	VSS_31	VSS_130	AB33
T44	VSS_32	VSS_131	P33
M44	VSS_33	VSS_132	L33
F44	VSS_34	VSS_133	H33
BC43	VSS_35	VSS_134	N32
AV43	VSS_36	VSS_135	K32
AM43	VSS_37	VSS_136	F32
I43	VSS_38	VSS_137	C32
C43	VSS_39	VSS_138	A31
BG42	VSS_40	VSS_139	AM29
AY42	VSS_41	VSS_140	T29
AT42	VSS_42	VSS_141	N29
AN42	VSS_43	VSS_142	K29
A42	VSS_44	VSS_143	H29
AE42	VSS_45	VSS_144	F29
N42	VSS_46	VSS_145	E16
I42	VSS_47	VSS_146	BG28
BD41	VSS_48	VSS_147	BD28
U41	VSS_49	VSS_148	W15
AM41	VSS_50	VSS_149	AV28
AH41	VSS_51	VSS_150	AT28
AD41	VSS_52	VSS_151	AR28
AA41	VSS_53	VSS_152	AJ28
Y41	VSS_54	VSS_153	AG28
T41	VSS_55	VSS_154	AE28
N41	VSS_56	VSS_155	BC13
G41	VSS_57	VSS_156	BA13
B41	VSS_58	VSS_157	Y28
BG40	VSS_59	VSS_158	AN13
BB40	VSS_60	VSS_159	A113
AV40	VSS_61	VSS_160	AE13
AN40	VSS_62	VSS_161	F28
H40	VSS_63	VSS_162	C28
E40	VSS_64	VSS_163	N13
AT39	VSS_65	VSS_164	L13
AM39	VSS_66	VSS_165	BF26
AJ39	VSS_67	VSS_166	G13
AE39	VSS_68	VSS_167	E13
N39	VSS_69	VSS_168	AB26
I39	VSS_70	VSS_169	BF12
B39	VSS_71	VSS_170	AV12
BH38	VSS_72	VSS_171	C26
BC38	VSS_73	VSS_172	AM12
BA38	VSS_74	VSS_173	AA12
AU38	VSS_75	VSS_174	J12
AH38	VSS_76	VSS_175	A12
AD38	VSS_77	VSS_176	BD11
AA38	VSS_78	VSS_177	BB11
Y38	VSS_79	VSS_178	AY11
U38	VSS_80	VSS_179	AN11
T38	VSS_81	VSS_180	AH11
I38	VSS_82	VSS_181	Y11
F38	VSS_83	VSS_182	N11
C38	VSS_84	VSS_183	G11
BF37	VSS_85	VSS_184	C11
BB37	VSS_86	VSS_185	BG10
AW37	VSS_87	VSS_186	BF24
AT37	VSS_88	VSS_187	AD12
AN37	VSS_89	VSS_188	AY24
AJ37	VSS_90	VSS_189	AT24
H37	VSS_91	VSS_190	AJ24
C37	VSS_92	VSS_191	AE10
BG36	VSS_93	VSS_192	AH10
BD36	VSS_94	VSS_193	M10
AK15	VSS_95	VSS_194	VSS_285
AU36	VSS_96	VSS_195	BF9
	VSS_97	VSS_196	BC9
	VSS_98	VSS_197	AN9
	VSS_99	VSS_198	AM9
		VSS_199	J24
			G24
			B9
			BH8
			BB8
			AV8
			AT8

VSS

VSS

VSS NCTF

VSS SCB

NC

U31J		AH8	
BG21	VSS_199	VSS_297	Y8
L12	VSS_200	VSS_298	LR
AW21	VSS_201	VSS_299	ER
AU21	VSS_202	VSS_300	BR
AP21	VSS_203	VSS_301	AN7
AN21	VSS_204	VSS_302	AJ7
F36	VSS_205	VSS_303	AU7
AE21	VSS_206	VSS_304	AN7
AB21	VSS_207	VSS_305	AJ7
R21	VSS_208	VSS_306	AE7
M21	VSS_209	VSS_307	AA7
J21	VSS_210	VSS_308	N7
T35	VSS_211	VSS_309	J7
G21	VSS_212	VSS_310	BG6
BC20	VSS_213	VSS_311	BD6
BA20	VSS_214	VSS_312	AV6
AW20	VSS_215	VSS_313	AT6
AT20	VSS_216	VSS_314	AM6
AJ20	VSS_217	VSS_315	M6
AG20	VSS_218	VSS_316	C6
W34	VSS_219	VSS_317	BA5
Y20	VSS_220	VSS_318	AH5
N20	VSS_221	VSS_319	AD5
K20	VSS_222	VSS_320	Y5
F20	VSS_223	VSS_321	L5
BC33	VSS_224	VSS_322	J5
BA33	VSS_225	VSS_323	H5
A20	VSS_226	VSS_324	F5
BG19	VSS_227	VSS_325	BE4
AR33	VSS_228		
AL33	VSS_229	VSS_327	BC3
AH33	VSS_230	VSS_328	AV3
AB33	VSS_231	VSS_329	AL3
P33	VSS_232	VSS_330	R3
L33	VSS_233	VSS_331	P3
H33	VSS_234	VSS_332	F3
N32	VSS_235	VSS_333	BA2
K32		VSS_334	AW2
F32		VSS_335	AU2
C32		VSS_336	AB2
A31		VSS_337	AP2
AM29		VSS_338	AJ2
T29		VSS_339	AH2
N29		VSS_340	AF2
K29		VSS_341	AE2
H29		VSS_342	AD2
F29		VSS_343	AC2
E16		VSS_344	Y2
BG28		VSS_345	M2
BD28		VSS_346	K2
W15		VSS_347	AM1
AV28		VSS_348	AA1
AT28		VSS_349	P1
AR28		VSS_350	H1
AJ28			
AG28		VSS_351	U24
AE28		VSS_352	U28
BC13		VSS_353	U25
BA13		VSS_354	U29
Y28			
AN13	VSS_255		
A113	VSS_256		
AE13	VSS_257		
F28	VSS_258		
C28	VSS_259		
N13	VSS_260		
L13	VSS_261		
BF26	VSS_262		
G13	VSS_263		
E13	VSS_264		
AB26	VSS_265		
BF12	VSS_266		
AV12	VSS_267		
C26	VSS_268		
AM12	VSS_269		
AA12	VSS_270		
J12	VSS_271		
A12	VSS_272		
BD11	VSS_273		
BB11	VSS_274		
AY11	VSS_275		
AN11	VSS_276		
AH11	VSS_277		
Y11	VSS_278		
N11	VSS_279		
G11	VSS_280		
C11	VSS_281		
BG10	VSS_282		
BF24	VSS_283		
AD12	VSS_284		
AY24	VSS_285		
AT24	VSS_286		
AJ24	VSS_287		
AE10	VSS_288		
AH10	VSS_289		
M10	VSS_290		
VSS_285	VSS_291		
BF9	VSS_292		
BC9	VSS_293		
AN9	VSS_294		
AM9	VSS_295		
J24	VSS_296		
G24			
B9			
BH8			
BB8			
AV8			
AT8			

VSS_NCTF_1	AF32
VSS_NCTF_2	AB32
VSS_NCTF_3	V32
VSS_NCTF_4	AL30
VSS_NCTF_5	AM29
VSS_NCTF_6	AF29
VSS_NCTF_7	AB29
VSS_NCTF_8	U26
VSS_NCTF_9	U23
VSS_NCTF_10	AL20
VSS_NCTF_11	AC19
VSS_NCTF_12	AL17
VSS_NCTF_13	AL17
VSS_NCTF_14	AA17
VSS_NCTF_15	U17
VSS_NCTF_16	U17

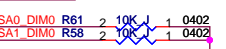
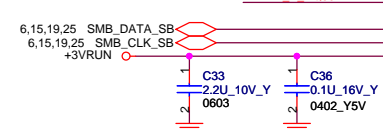
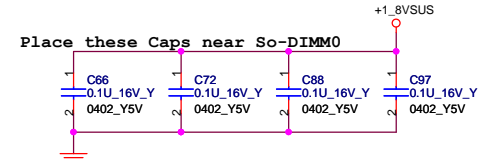
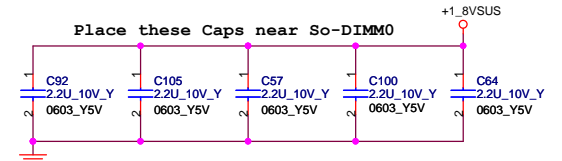
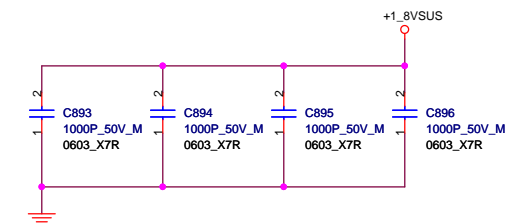
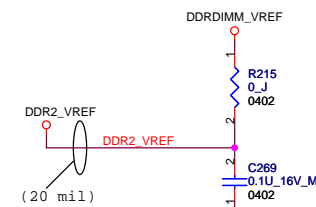
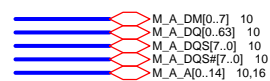
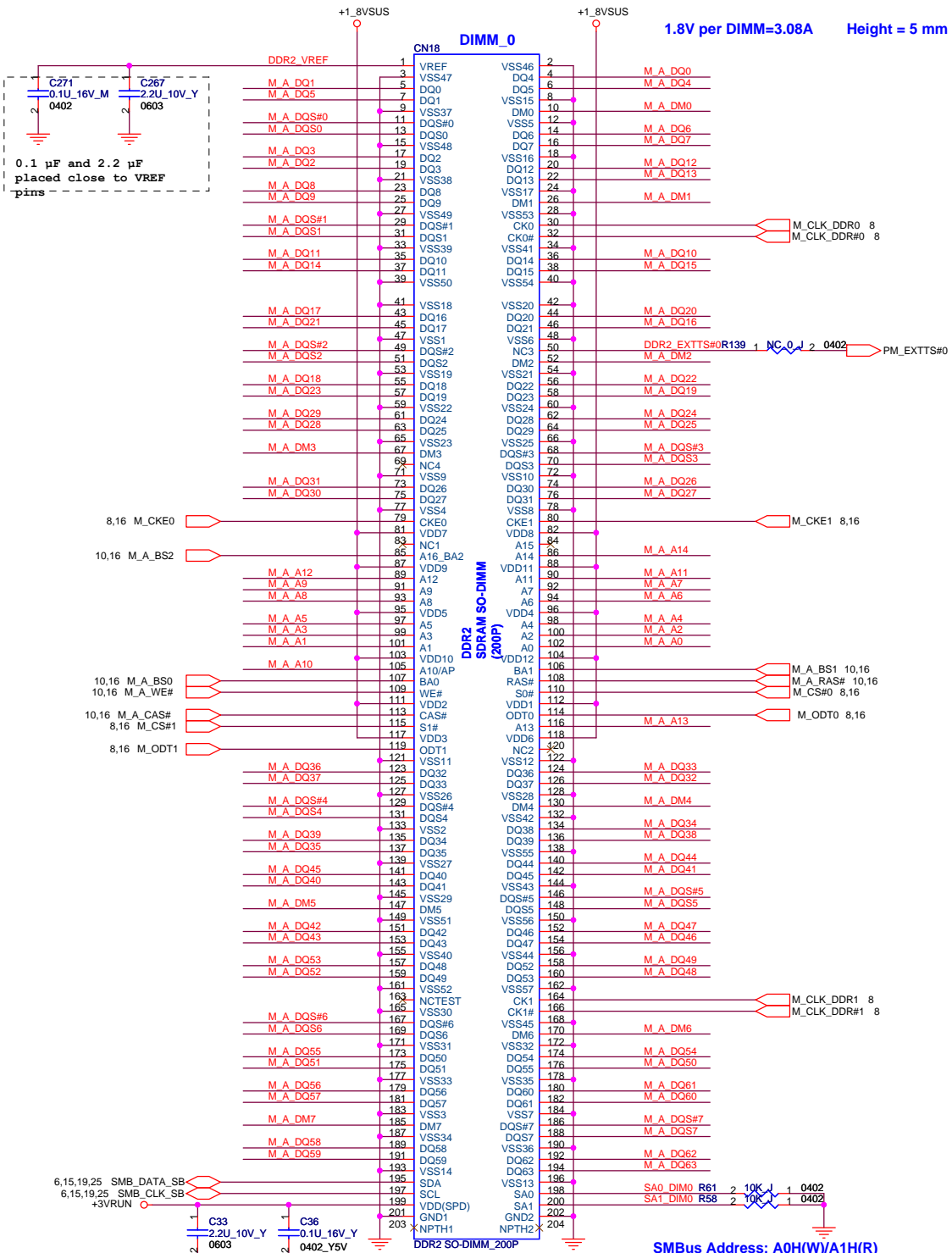
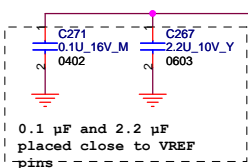
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VSS_SCB_2	BH1
VSS_SCB_3	A48
VSS_SCB_4	C1
VSS_SCB_5	A3

NC_26	D2
NC_27	C3
NC_28	D3
NC_29	B4
NC_30	A5
NC_31	AE
NC_32	A43
NC_33	A44
NC_34	B45
NC_35	C46
NC_36	D47
NC_37	B47
NC_38	A46
NC_39	F48
NC_40	E48
NC_41	C48
NC_42	B48

CANTIGA null

CANTIGA null

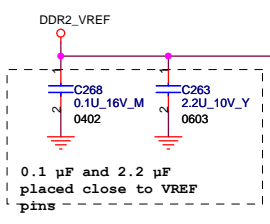
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>Cantiga (VSS) 777</b>			
Size	Document Number		Rev
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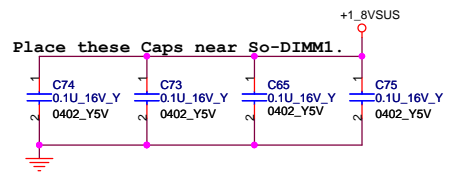
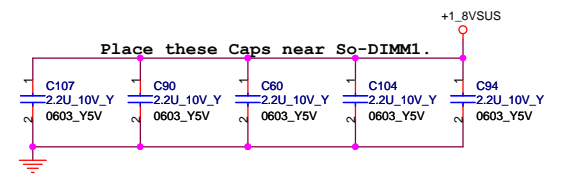
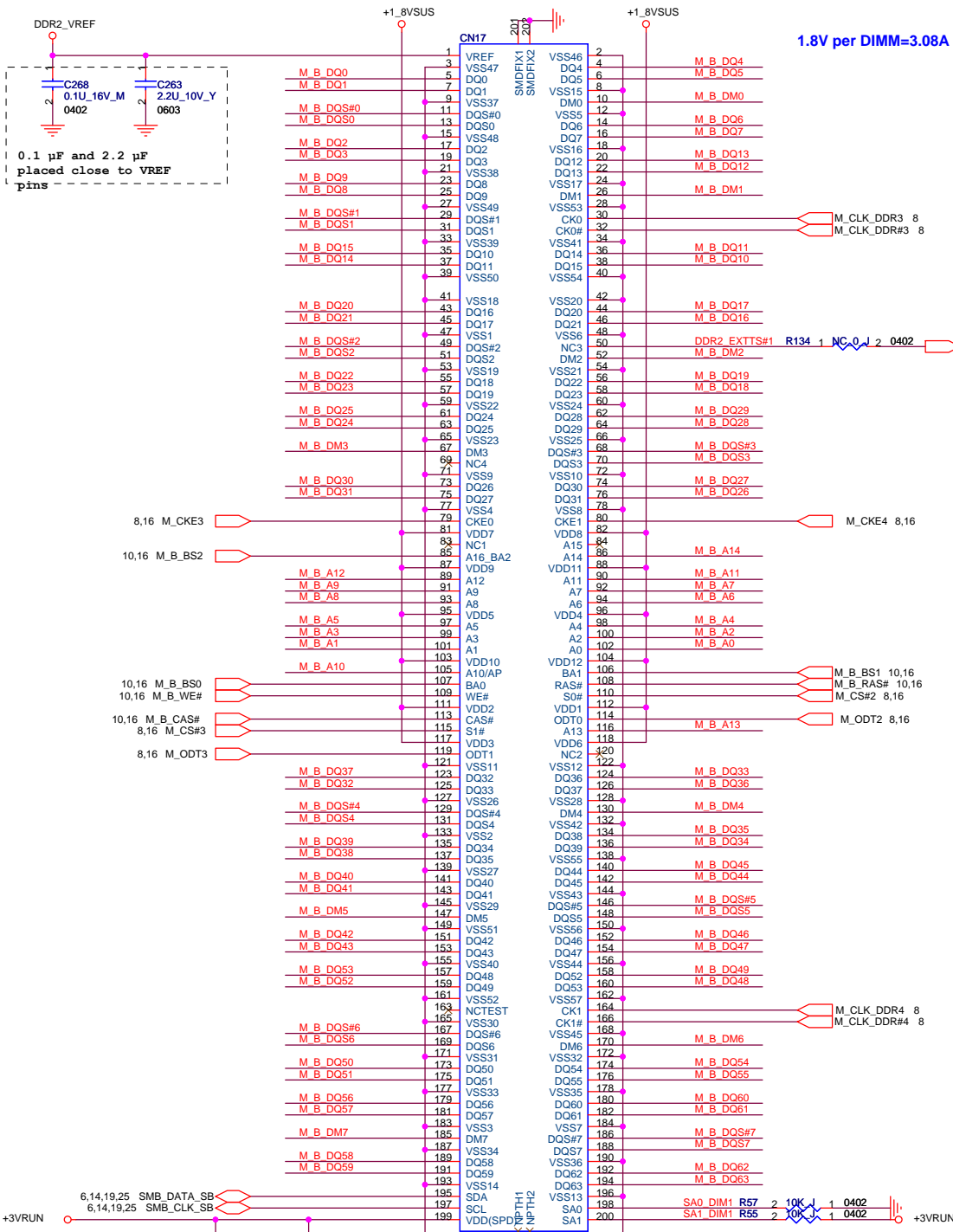
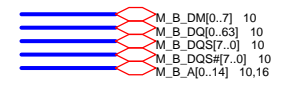
SMBus Address: A0H(W)/A1H(R)

Place DIMM\_0 near GMCH

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
<b>Title: DDR(II)SO-DIMM_0</b>			
Size	Document Number		Rev
A3	<b>M760</b>		1.0
Date:	Thursday, March 27, 2008	Sheet	14 of 89

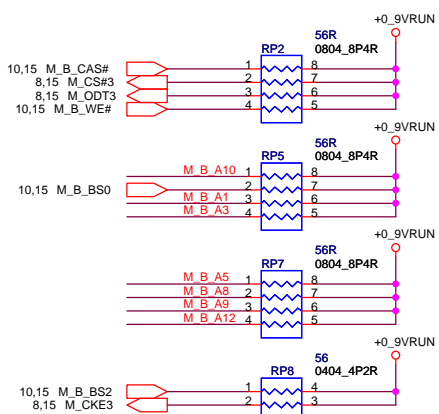
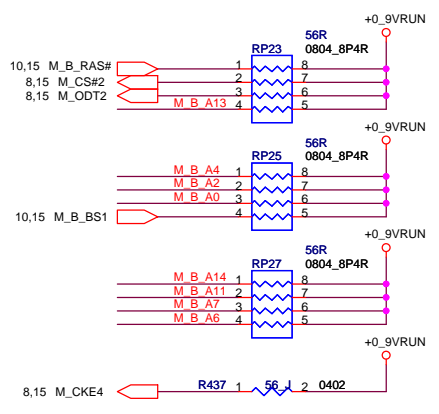
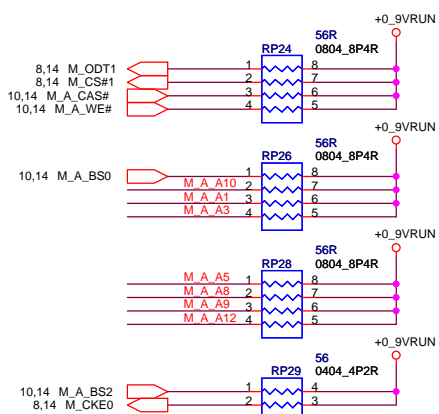
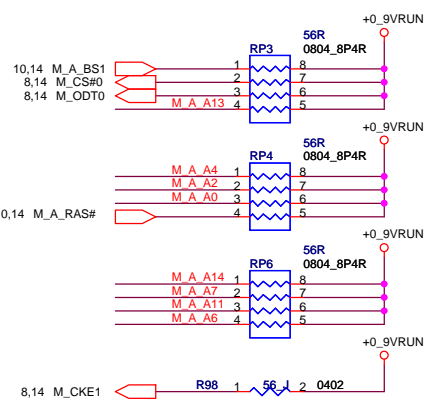
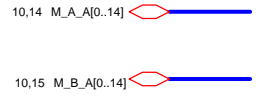
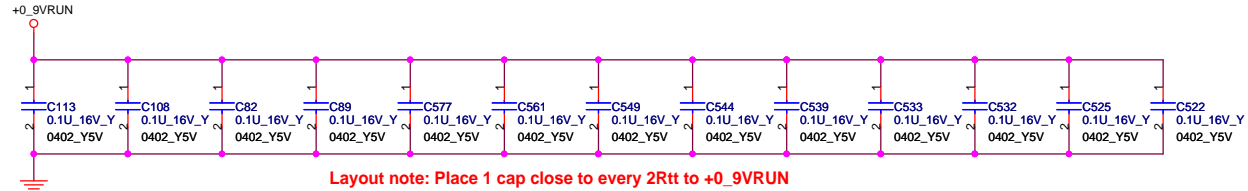
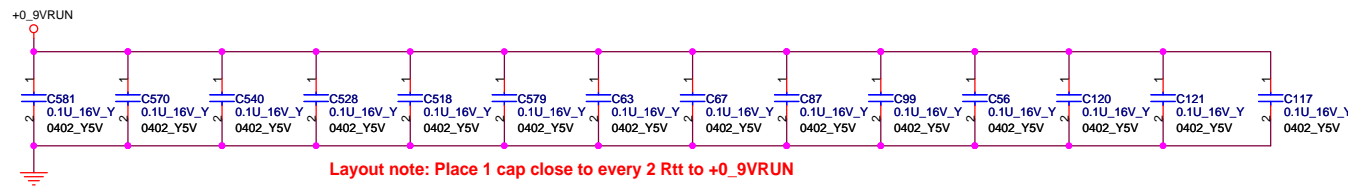


1.8V per DIMM=3.08A Height = 4 mm

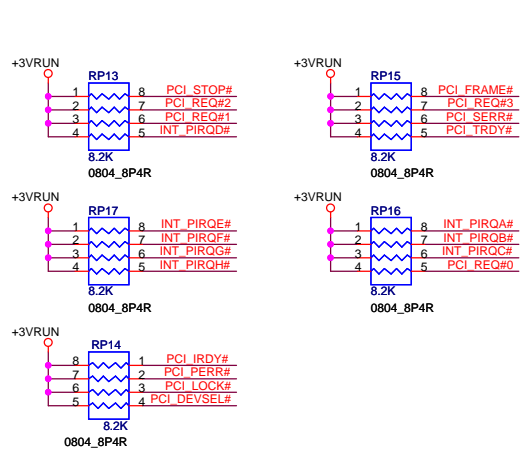


DIMM\_1 is placed farther from the GMCH than DIMM\_0

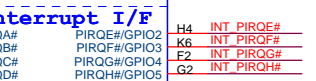
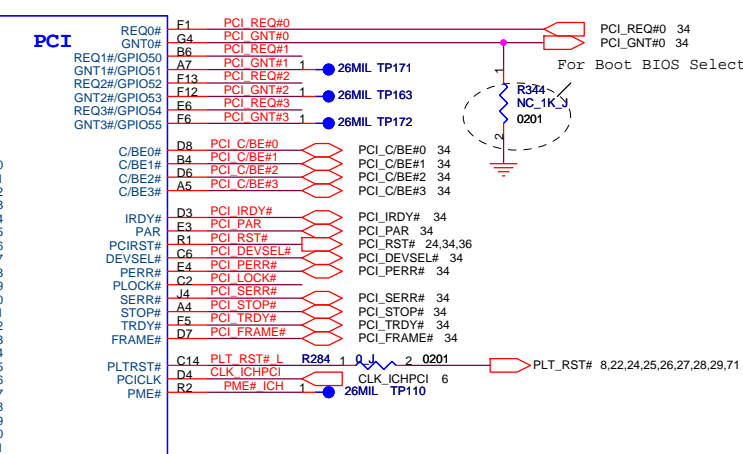
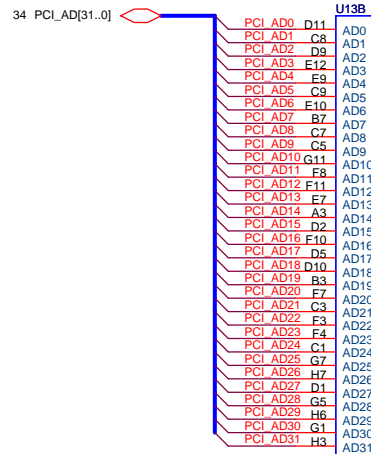
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>DDR(II)SO-DIMM_1</b>			
Size	Document Number		Rev
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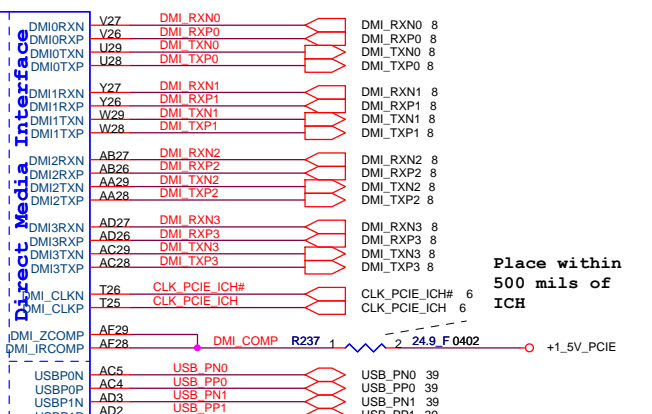
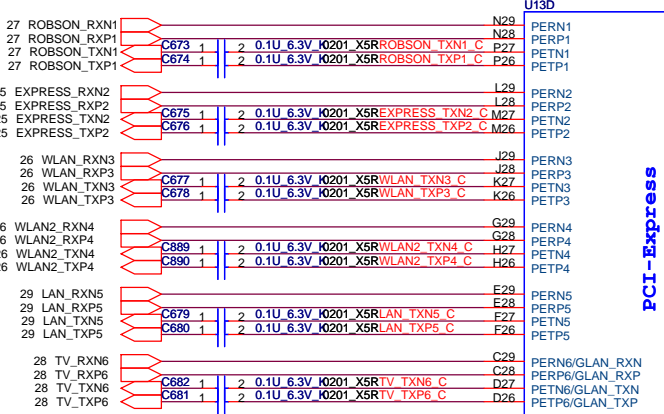
PCI Pullups



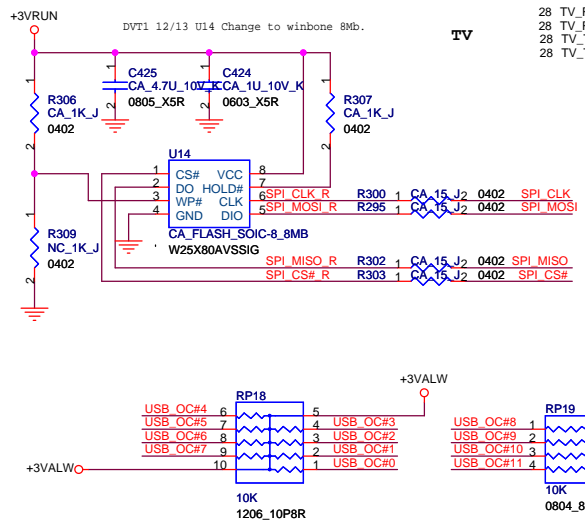
**Strap for Boot-BIOS**

	GNT0#	SPI_CS1#
IPC(Default)	HI	HI
PCI	HI	LOW
SPI	LOW	HI

- Robson
- Express Card
- WLAN
- LAN
- TV



USB PORT	Function
PORT-0	SIDE-1
PORT-1	SIDE-2
PORT-2	SIDE-3
PORT-3	EXPRESS CARD
PORT-4	Bluetooth
PORT-5	PATA ODD Bridge
PORT-6	Wireless LAN2
PORT-7	Camera
PORT-8	Felica
PORT-9	CIR
PORT-10	Wireless LAN
PORT-11	



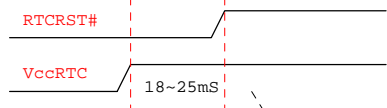
Place within 500 mils of ICH and don't routing next to high speed signals

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title: **ICH9-M (PCI/USB) 1/5**

Size: A3 Document Number: **M760** Rev: 1.0

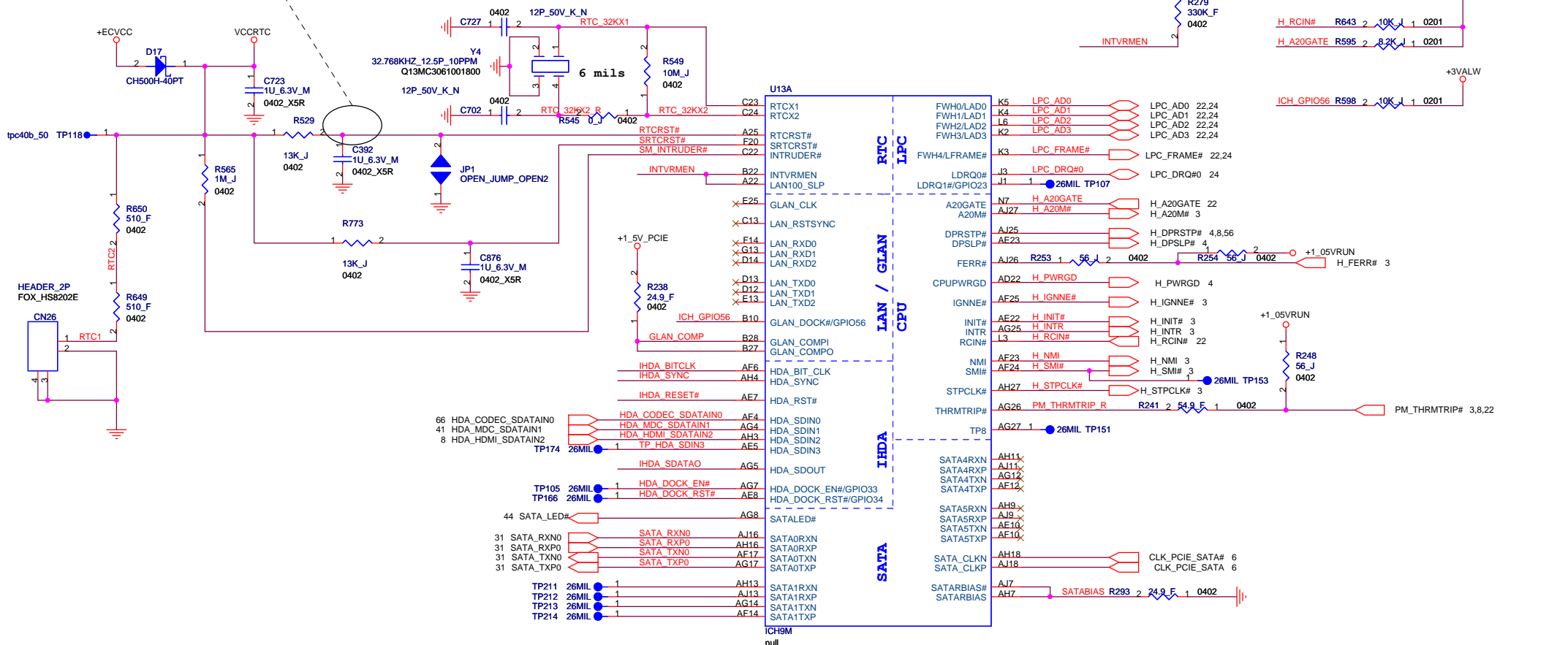
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The traces inside this block should be wider.

Internal VRM enabled for VccSua1\_05, VccSua1\_5, VccCL1\_5, VccLAN1\_05 and VccCL1\_05

INTVRMEN	Low= Internal VR Disabled High= Internal VR Enabled(Default)
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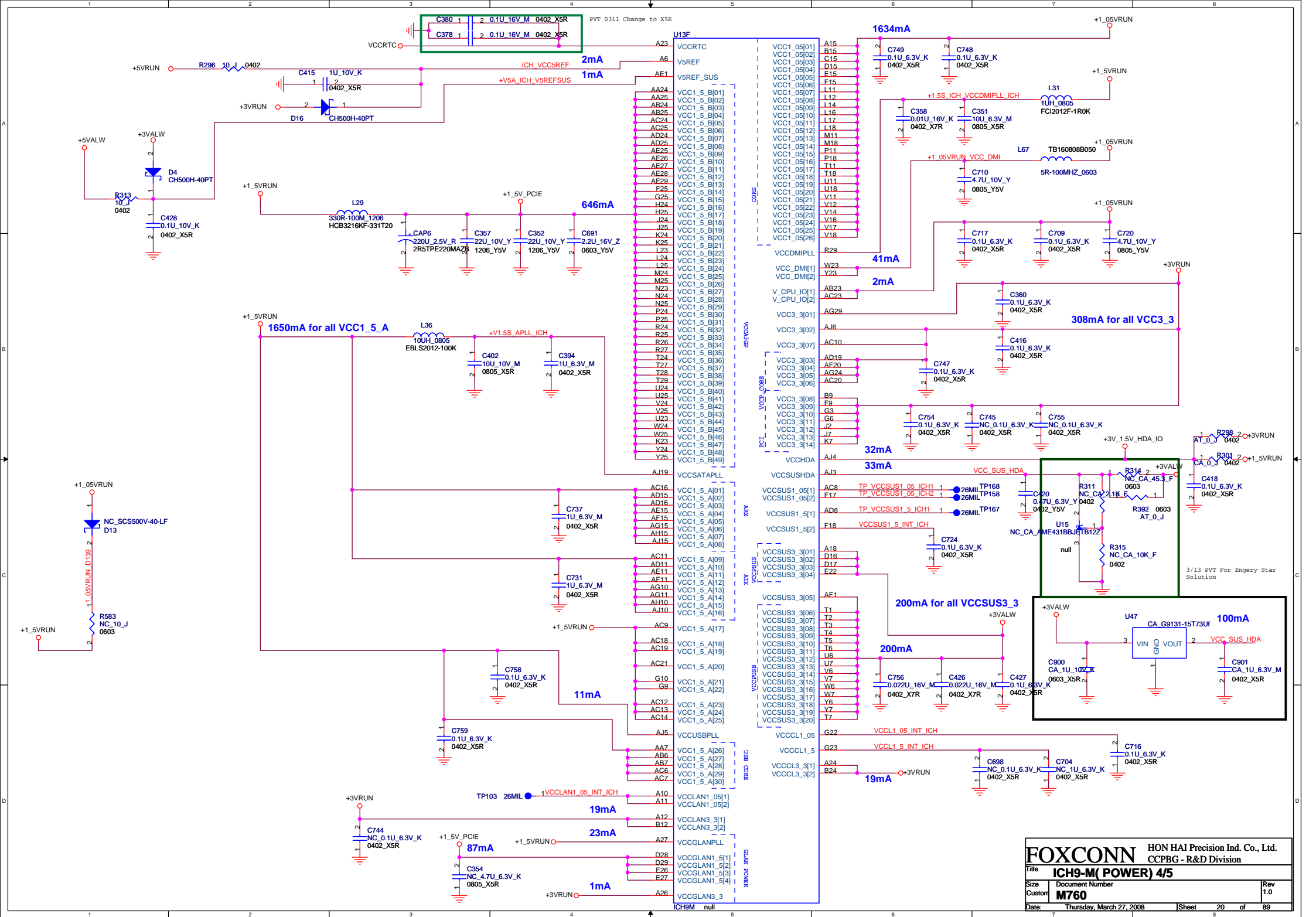


**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title: **ICH9-M (LPC,IDE,SATA) 2/5**

Size A3	Document Number <b>M760</b>	Rev 1.0
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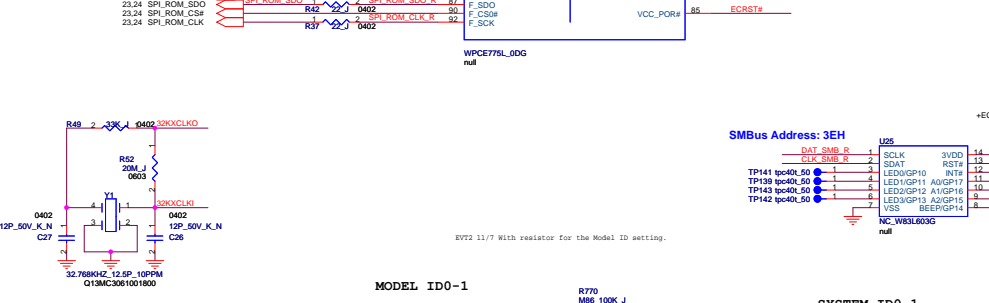
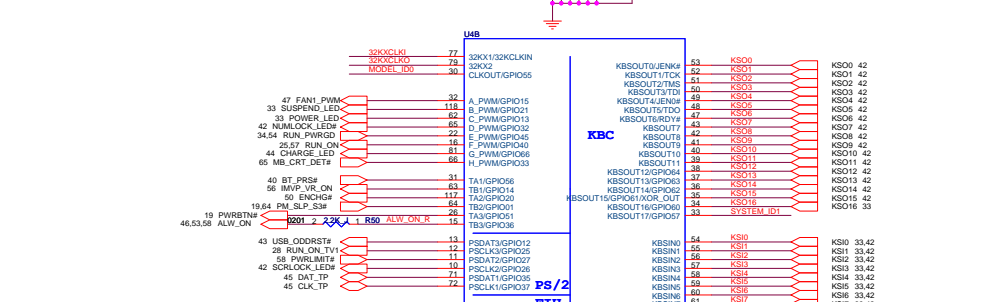
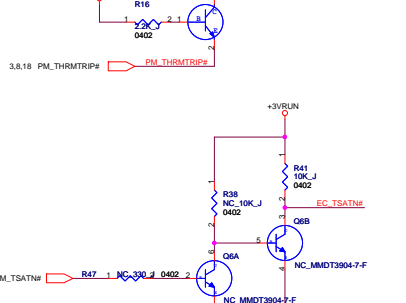
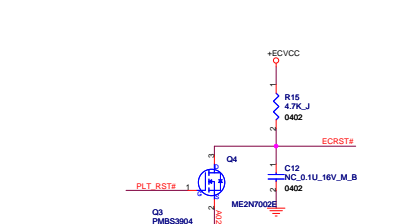
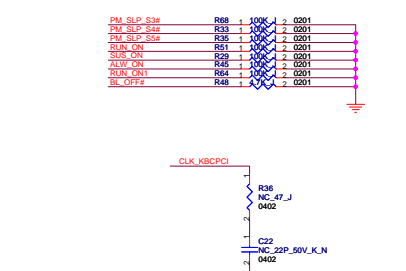
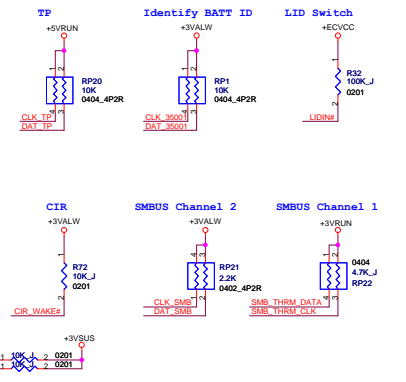
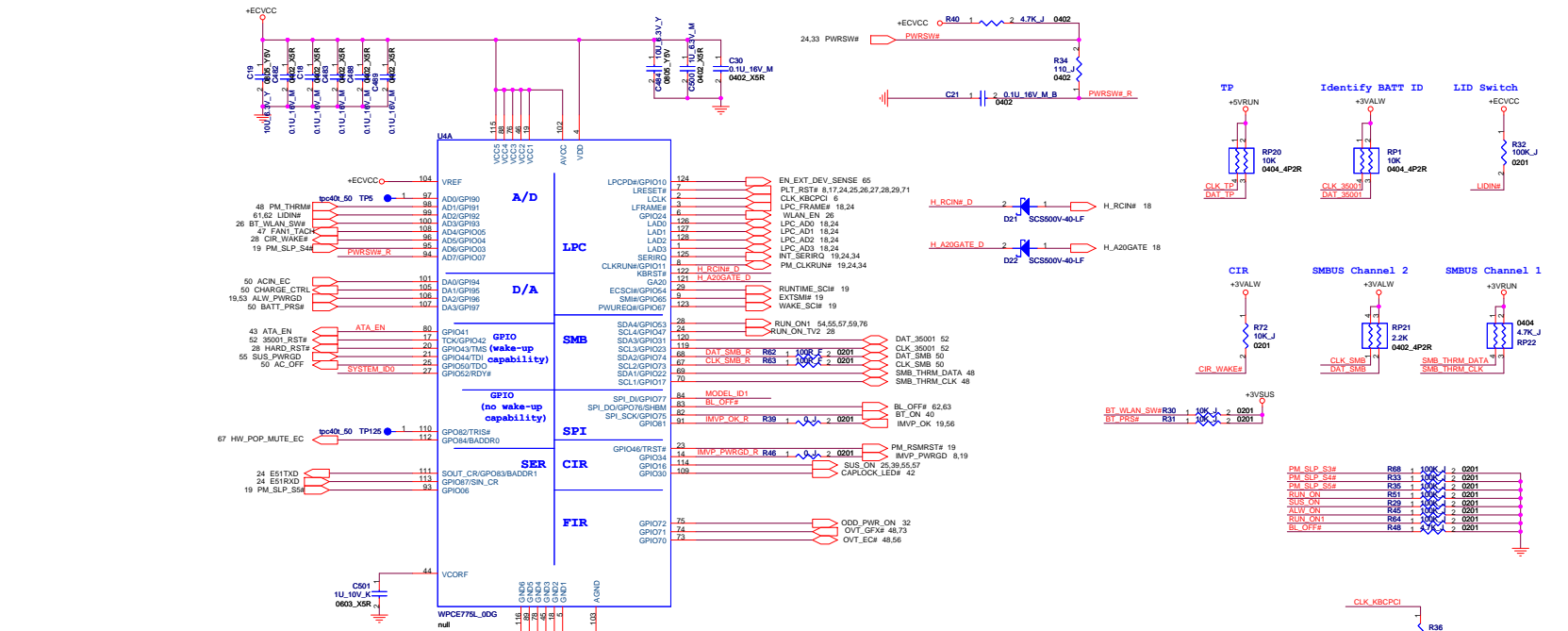




U13E		H5	
AA26	VSS[001]	VSS[107]	J23
AA27	VSS[002]	VSS[108]	J26
AA3	VSS[003]	VSS[109]	J27
AA6	VSS[004]	VSS[110]	AC22
AB1	VSS[005]	VSS[111]	K28
AA23	VSS[006]	VSS[112]	K29
AB28	VSS[007]	VSS[113]	L13
AB29	VSS[008]	VSS[114]	L15
AB4	VSS[009]	VSS[115]	L2
AB5	VSS[010]	VSS[116]	L26
AC17	VSS[011]	VSS[117]	L27
AC26	VSS[012]	VSS[118]	L5
AC27	VSS[013]	VSS[119]	L7
AC3	VSS[014]	VSS[120]	M12
AD1	VSS[015]	VSS[121]	M13
AD10	VSS[016]	VSS[122]	M14
AD12	VSS[017]	VSS[123]	M15
AD13	VSS[018]	VSS[124]	M16
AD14	VSS[019]	VSS[125]	M17
AD17	VSS[020]	VSS[126]	M23
AD18	VSS[021]	VSS[127]	M28
AD21	VSS[022]	VSS[128]	M29
AD28	VSS[023]	VSS[129]	N11
AD29	VSS[024]	VSS[130]	N12
AD4	VSS[025]	VSS[131]	N13
AD5	VSS[026]	VSS[132]	N14
AD6	VSS[027]	VSS[133]	N15
AD7	VSS[028]	VSS[134]	N16
AD9	VSS[029]	VSS[135]	N17
AE12	VSS[030]	VSS[136]	N18
AE13	VSS[031]	VSS[137]	N26
AE14	VSS[032]	VSS[138]	N27
AE16	VSS[033]	VSS[139]	P12
AE17	VSS[034]	VSS[140]	P13
AE2	VSS[035]	VSS[141]	P14
AE20	VSS[036]	VSS[142]	P15
AE24	VSS[037]	VSS[143]	P16
AE3	VSS[038]	VSS[144]	P17
AE4	VSS[039]	VSS[145]	P2
AE6	VSS[040]	VSS[146]	P23
AE9	VSS[041]	VSS[147]	P28
AF13	VSS[042]	VSS[148]	P29
AF16	VSS[043]	VSS[149]	P4
AF18	VSS[044]	VSS[150]	P7
AF22	VSS[045]	VSS[151]	R11
AH26	VSS[046]	VSS[152]	R12
AF26	VSS[047]	VSS[153]	R13
AF27	VSS[048]	VSS[154]	R14
AF5	VSS[049]	VSS[155]	R15
AF7	VSS[050]	VSS[156]	R16
AF9	VSS[051]	VSS[157]	R17
AG13	VSS[052]	VSS[158]	R19
AG18	VSS[053]	VSS[159]	R28
AG20	VSS[054]	VSS[160]	T12
AG23	VSS[055]	VSS[161]	T13
AG3	VSS[056]	VSS[162]	T14
AG6	VSS[057]	VSS[163]	T15
AG9	VSS[058]	VSS[164]	T16
AH12	VSS[059]	VSS[165]	T17
AH14	VSS[060]	VSS[166]	T23
AH17	VSS[061]	VSS[167]	B26
AH19	VSS[062]	VSS[168]	U12
AH2	VSS[063]	VSS[169]	U13
AH22	VSS[064]	VSS[170]	U14
AH25	VSS[065]	VSS[171]	U15
AH28	VSS[066]	VSS[172]	U16
AH5	VSS[067]	VSS[173]	U17
AH8	VSS[068]	VSS[174]	AD23
AH8	VSS[069]	VSS[175]	U26
AJ12	VSS[070]	VSS[176]	U27
AJ14	VSS[071]	VSS[177]	U3
AJ17	VSS[072]	VSS[178]	V1
AJ8	VSS[073]	VSS[179]	V13
B11	VSS[074]	VSS[180]	V15
B14	VSS[075]	VSS[181]	V23
B17	VSS[076]	VSS[182]	V28
B2	VSS[077]	VSS[183]	V29
B20	VSS[078]	VSS[184]	V4
B23	VSS[079]	VSS[185]	V5
B5	VSS[080]	VSS[186]	W26
B8	VSS[081]	VSS[187]	W27
C26	VSS[082]	VSS[188]	W3
C27	VSS[083]	VSS[189]	Y1
E11	VSS[084]	VSS[190]	Y28
E14	VSS[085]	VSS[191]	Y29
E18	VSS[086]	VSS[192]	Y4
E2	VSS[087]	VSS[193]	Y5
E21	VSS[088]	VSS[194]	AG28
E24	VSS[089]	VSS[195]	AH6
E5	VSS[090]	VSS[196]	AF2
E8	VSS[091]	VSS[197]	B25
F16	VSS[092]	VSS[198]	
F28	VSS[093]		
F29	VSS[094]	VSS_NCTF[01]	A1
G12	VSS[095]	VSS_NCTF[02]	A2
G14	VSS[096]	VSS_NCTF[03]	A28
G18	VSS[097]	VSS_NCTF[04]	A29
G21	VSS[098]	VSS_NCTF[05]	AH1
G24	VSS[099]	VSS_NCTF[06]	AH29
G26	VSS[100]	VSS_NCTF[07]	AJ1
G27	VSS[101]	VSS_NCTF[08]	AJ2
G8	VSS[102]	VSS_NCTF[09]	AJ28
H2	VSS[103]	VSS_NCTF[10]	AJ29
H23	VSS[104]	VSS_NCTF[11]	B1
H28	VSS[105]	VSS_NCTF[12]	B29
H29	VSS[106]		

ICH9M  
null

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	<b>ICH9-M (GND) 5/5</b>		
Size	Document Number	Rev	
A3	<b>M760</b>	1.0	
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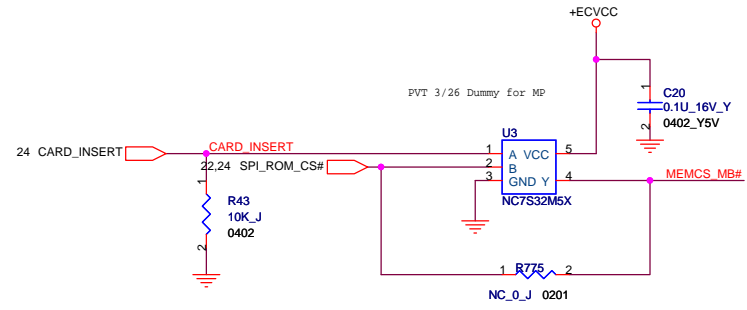
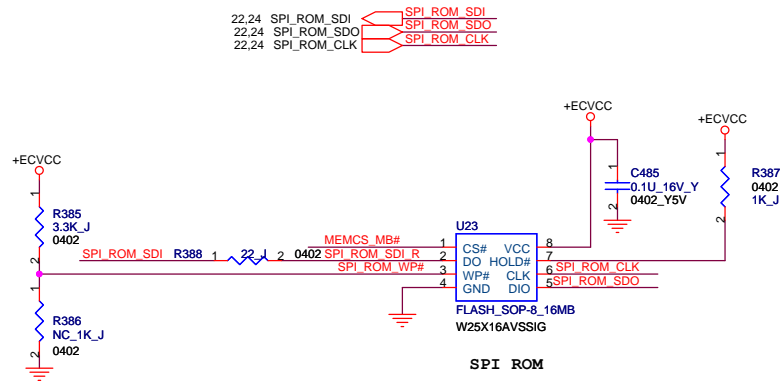


DVT1 12/10 Adjust for clock accuracy.

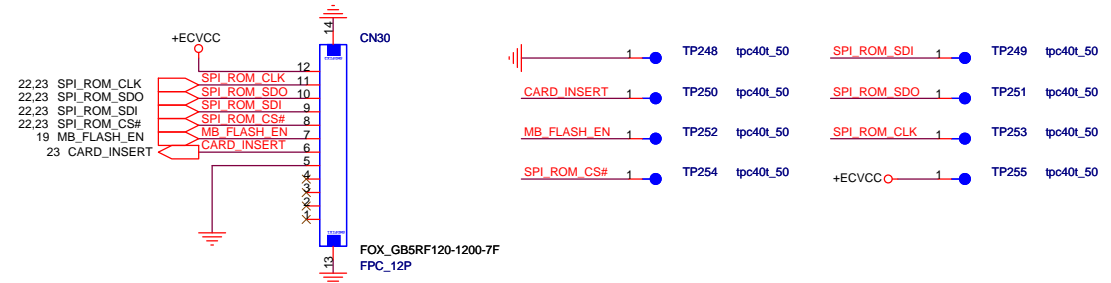
DVT2 11/7 With resistor for the Model ID setting.

ID1	ID0	SKU
0	0	UMA
0	1	DISCRETE (M82)
1	0	DISCRETE (M86)

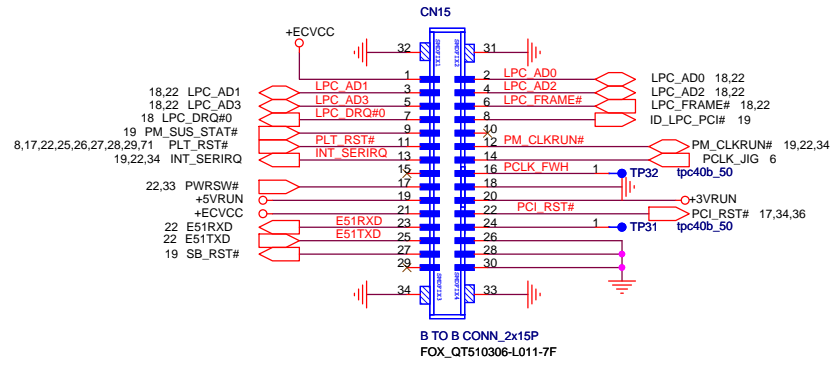
ID1	ID0	SKU
0	0	RESERVED
0	1	RESERVED
1	0	RESERVED



PVT 3/26 Dummy for MP



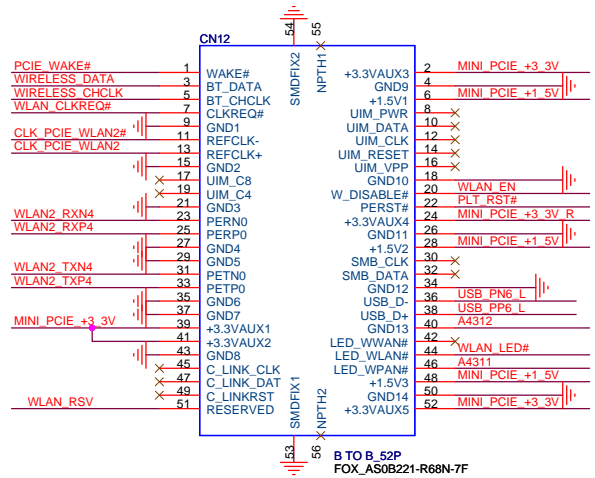
**EXTERNAL SPI ROM INTERFACE**



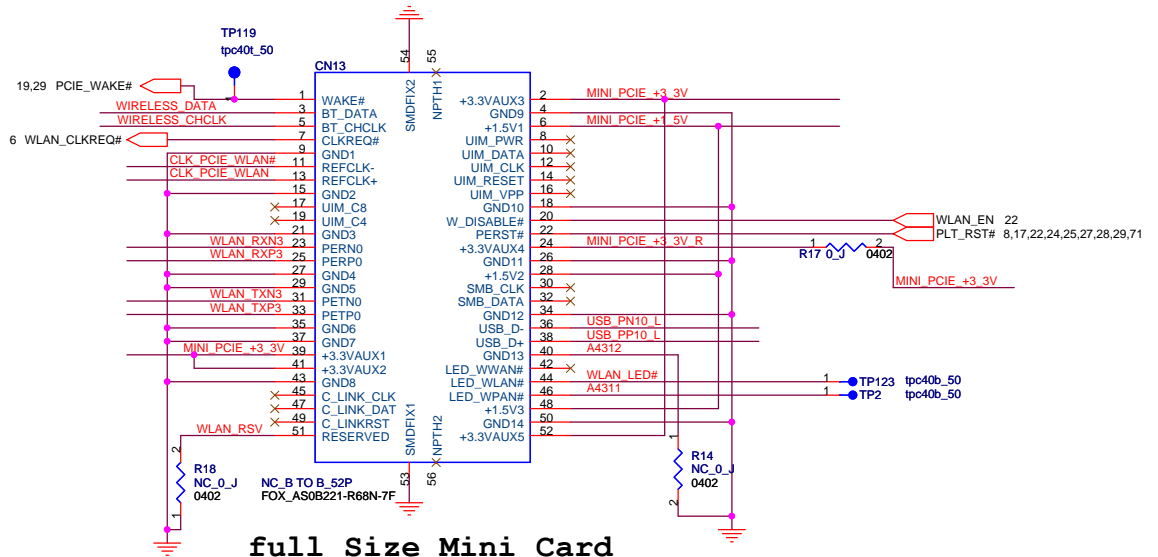
**JIG-120**



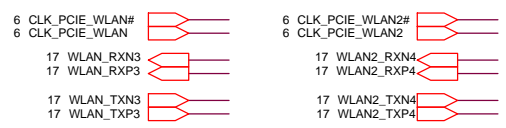




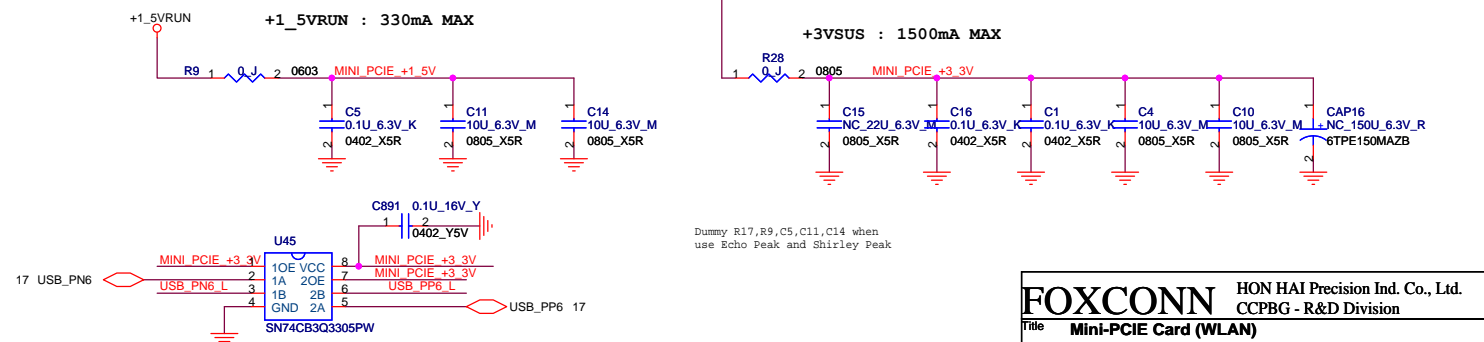
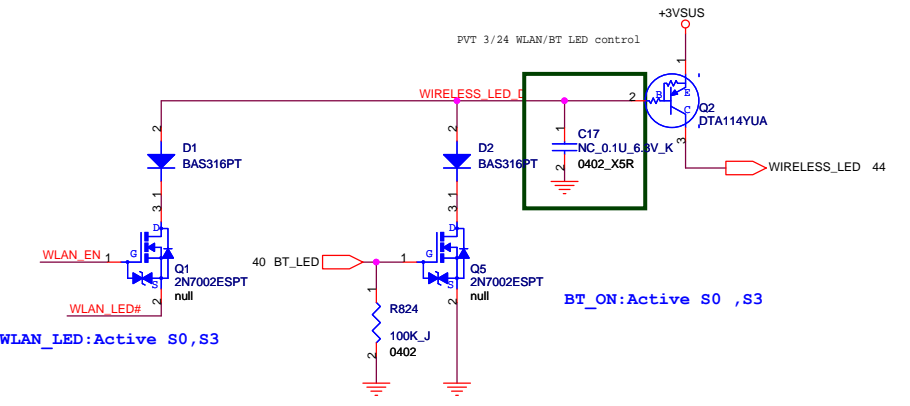
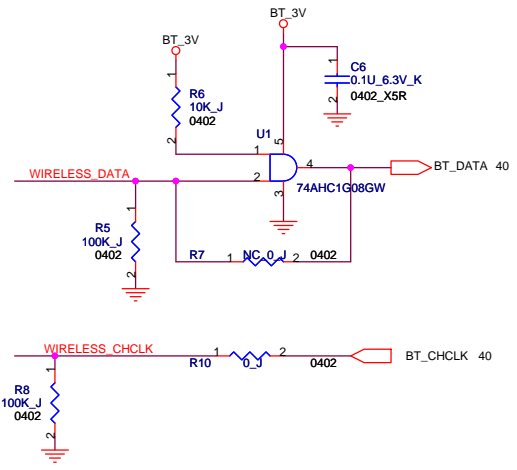
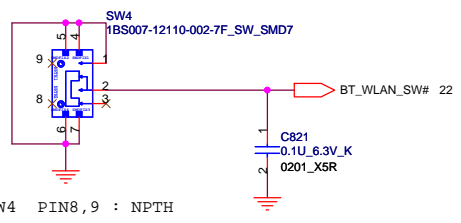
Half Size Mini Card



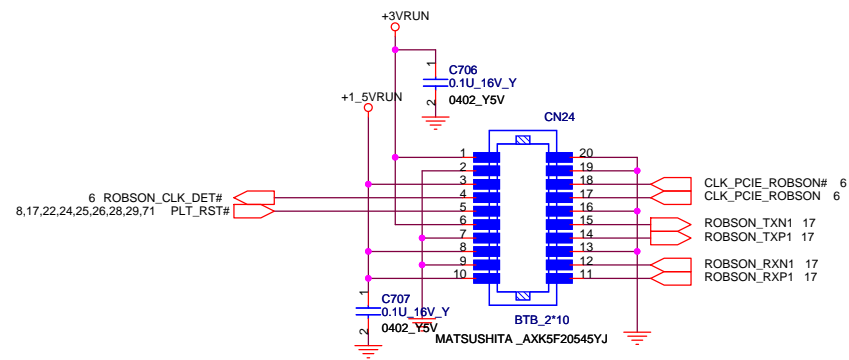
full Size Mini Card



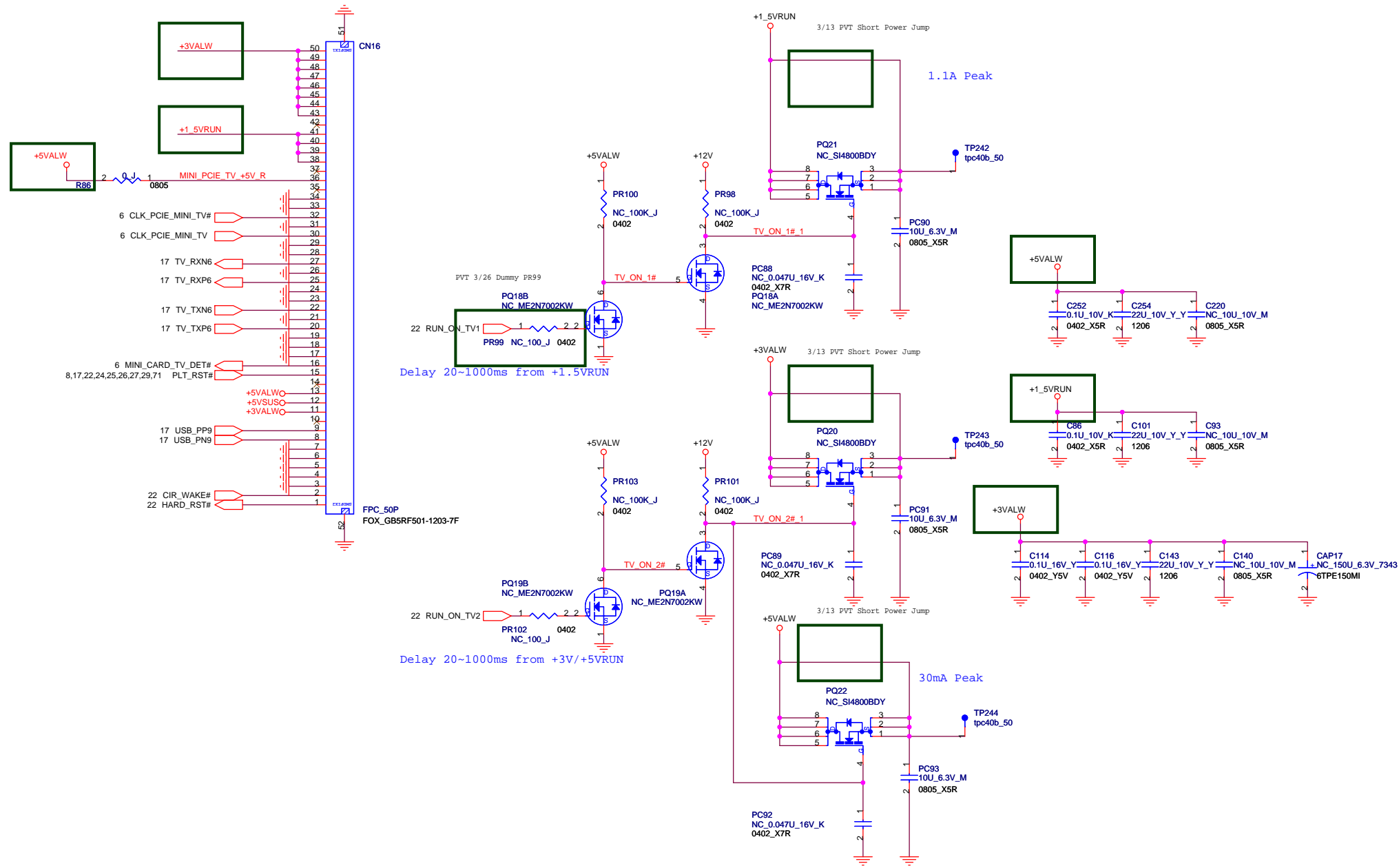
WLAN Switch

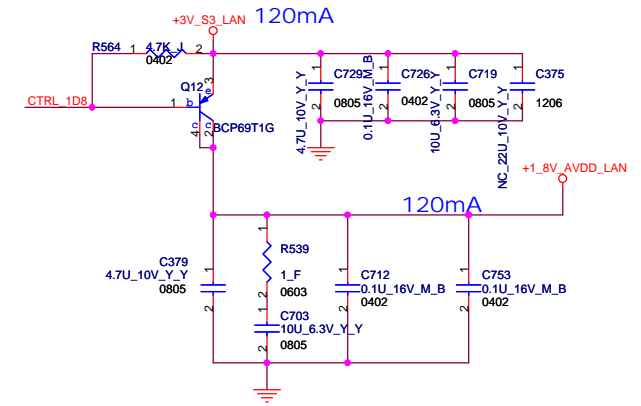
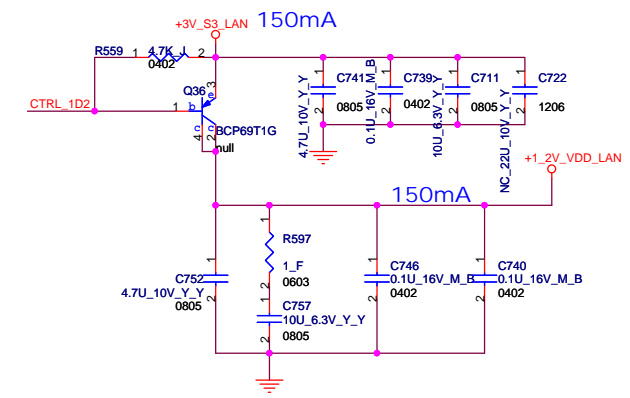
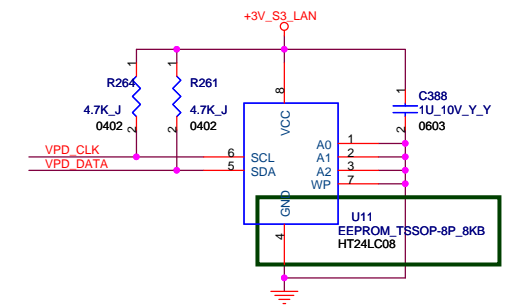
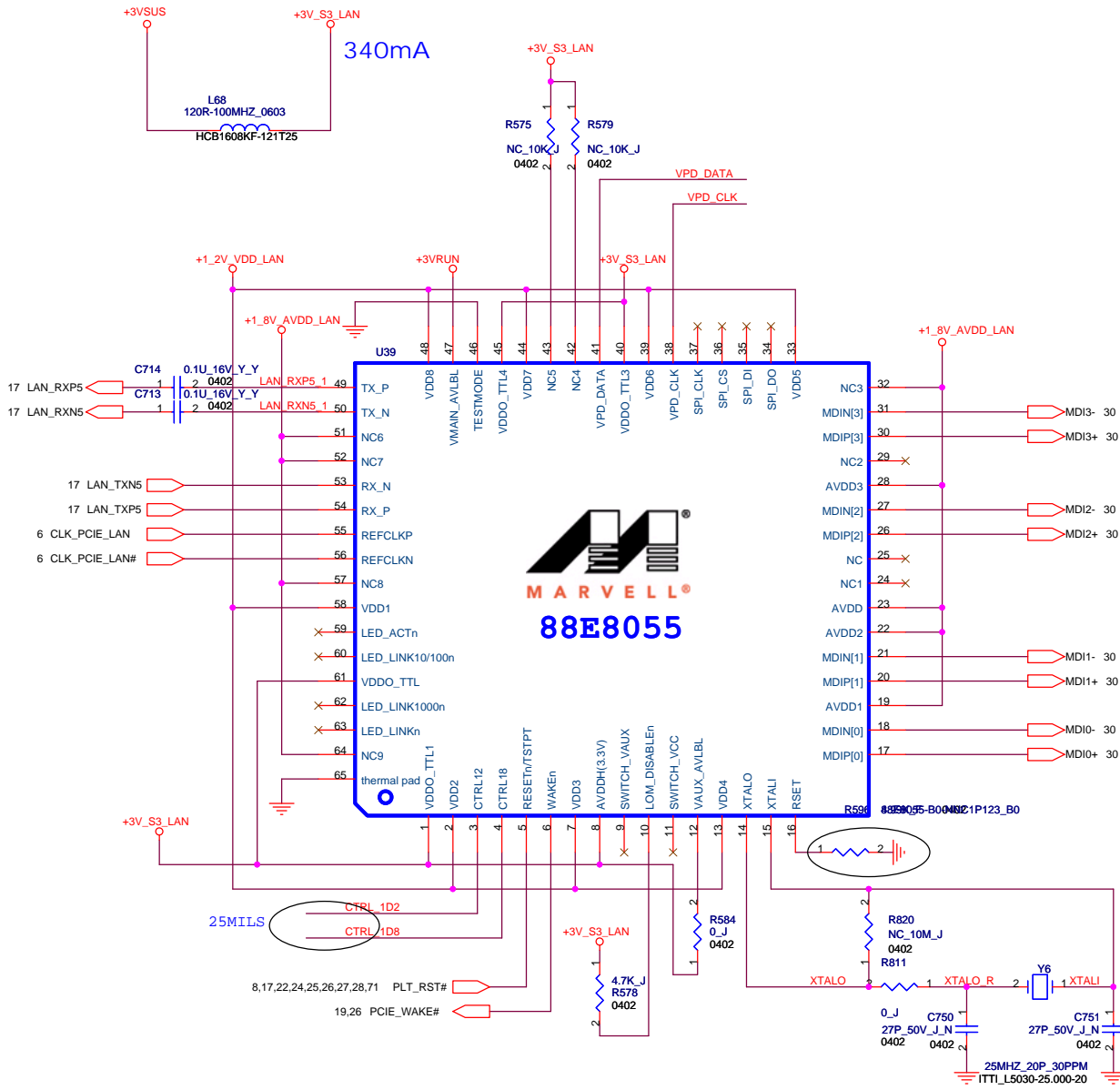


<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	<b>Mini-PCIE Card (WLAN)</b>		
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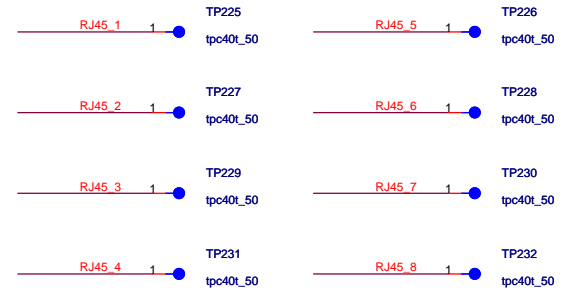
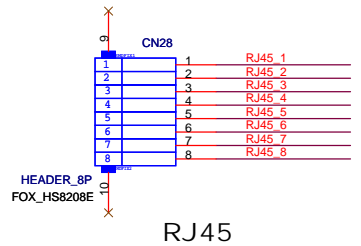
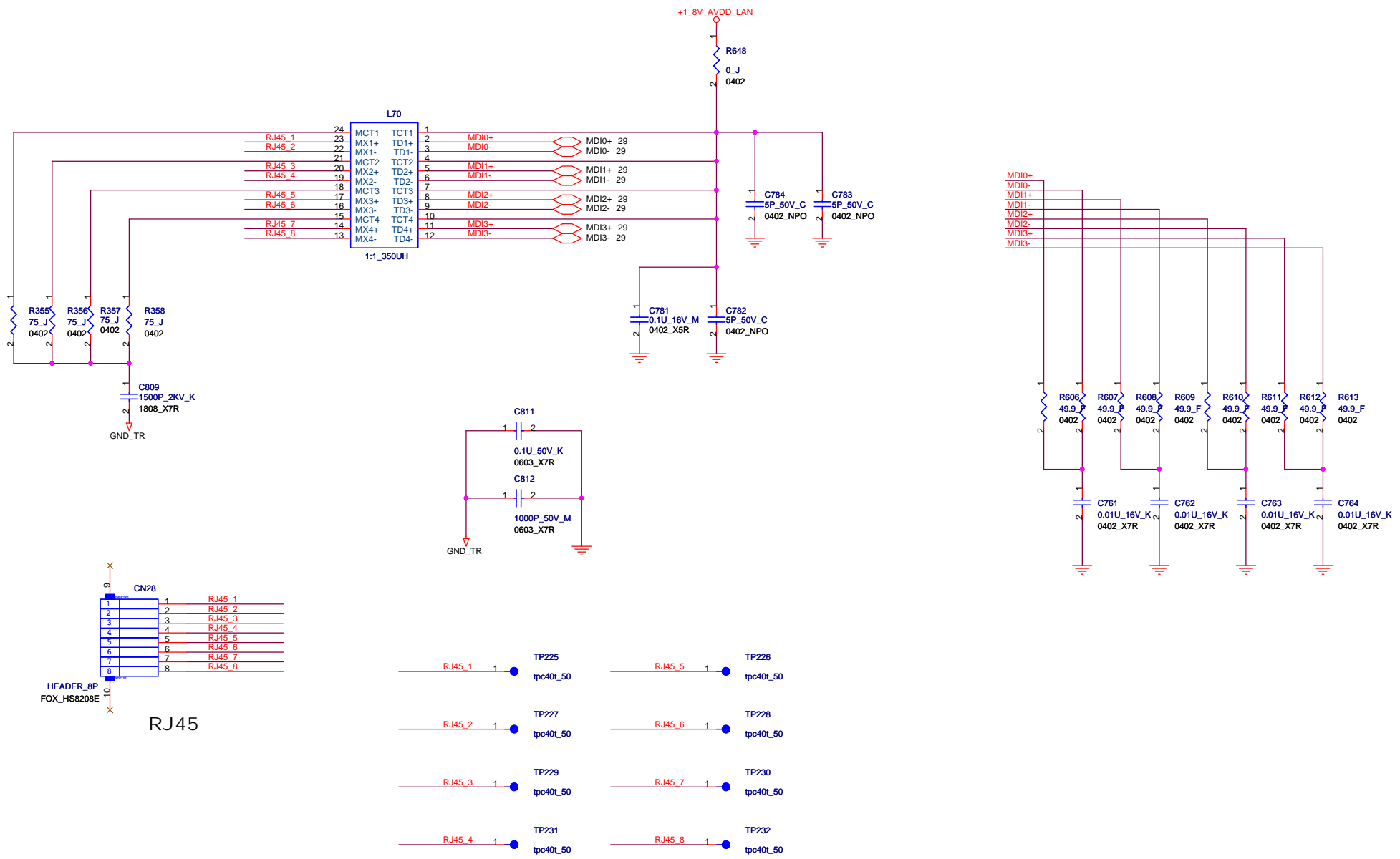
**Robson 1.6 Module**

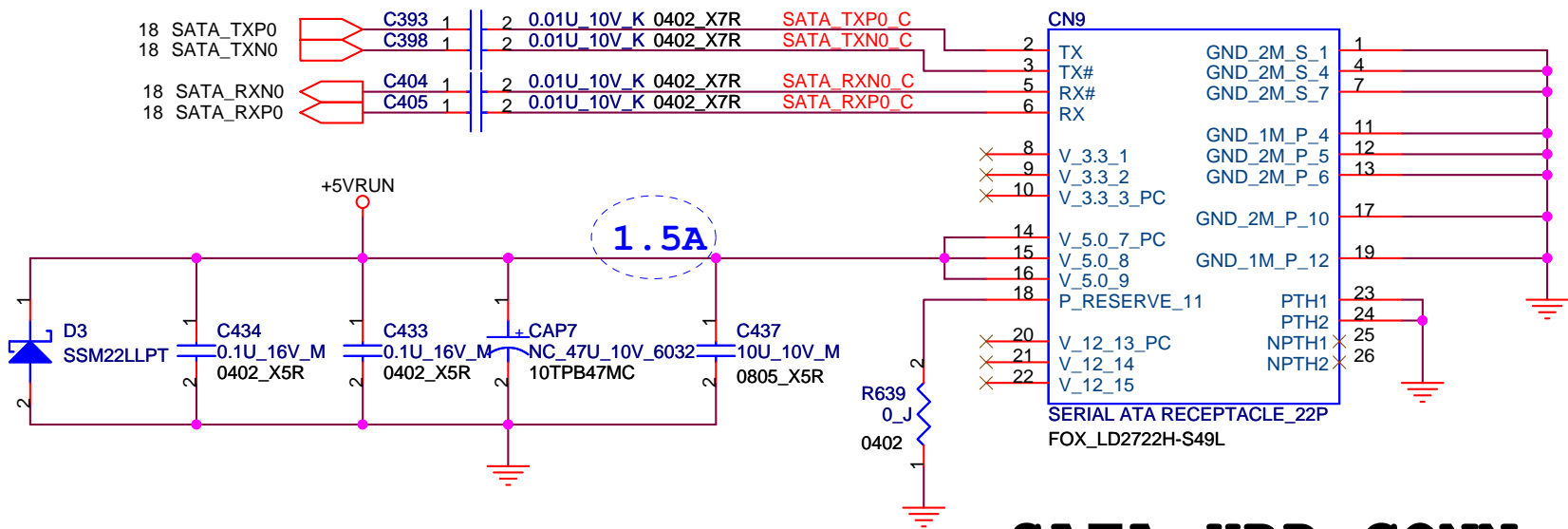




DVT1 12/18 Add series resistor for frequency adjust.

<b>FOXCONN</b> HON HAI PRECISION IND. CO., LTD.	
CPBG - R&D Division	
Title <b>LAN (88E8055)(1/2)</b>	
Size A3	Document Number M760
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# SATA HDD CONN

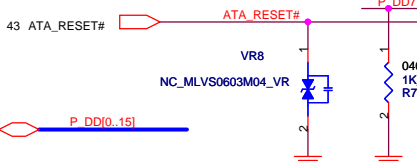
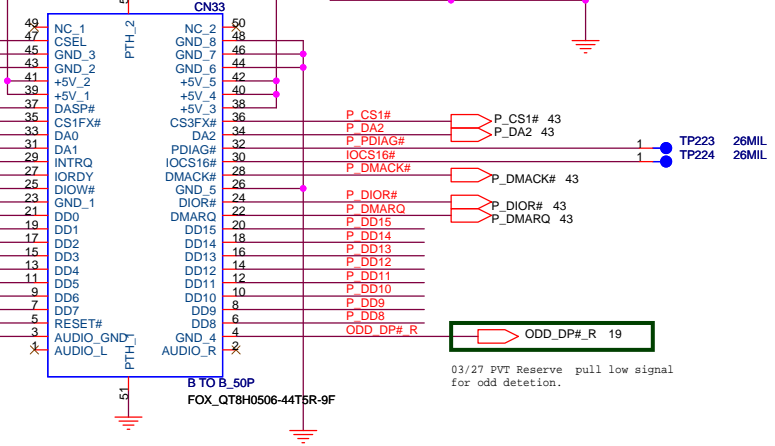
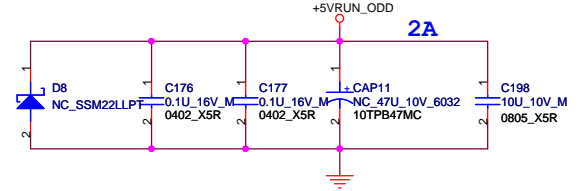
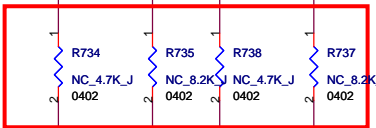
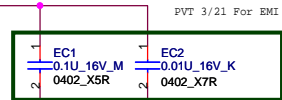
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>SATA HDD</b>			
Size A	Document Number M760	Rev 1.0	
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4/17 (MS90)  
Follow Adoi san suggest ODD: Master/HDD:Slave

H: Slave  
L: Master  
ODD must Master

- 44 ODD\_LED#
- 43 P\_CS0#
- 43 P\_DA0
- 43 P\_DA1
- 43 P\_INTRQ
- 43 P\_IORDY
- 43 P\_DIOW#

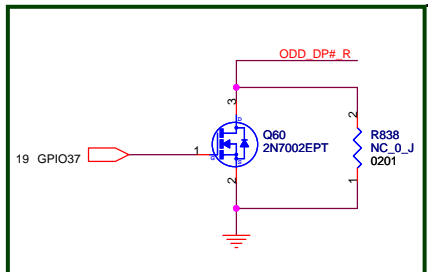
- ODD\_LED#
- P\_CS0#
- P\_DA0
- P\_DA1
- P\_INTRQ
- P\_IORDY
- P\_DIOW#



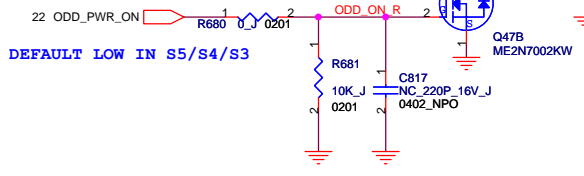
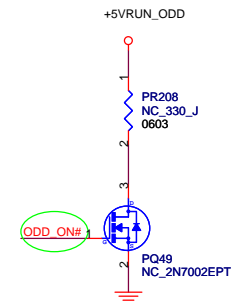
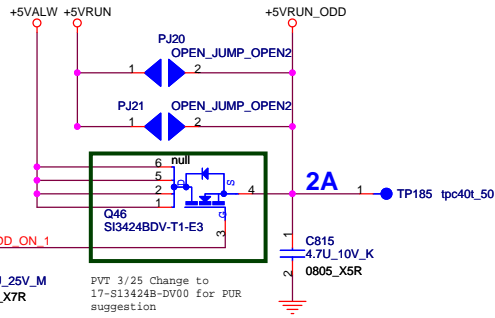
03/27 PVT Reserve pull low signal for odd detection.

For ESD.

### PATA ODD CONN

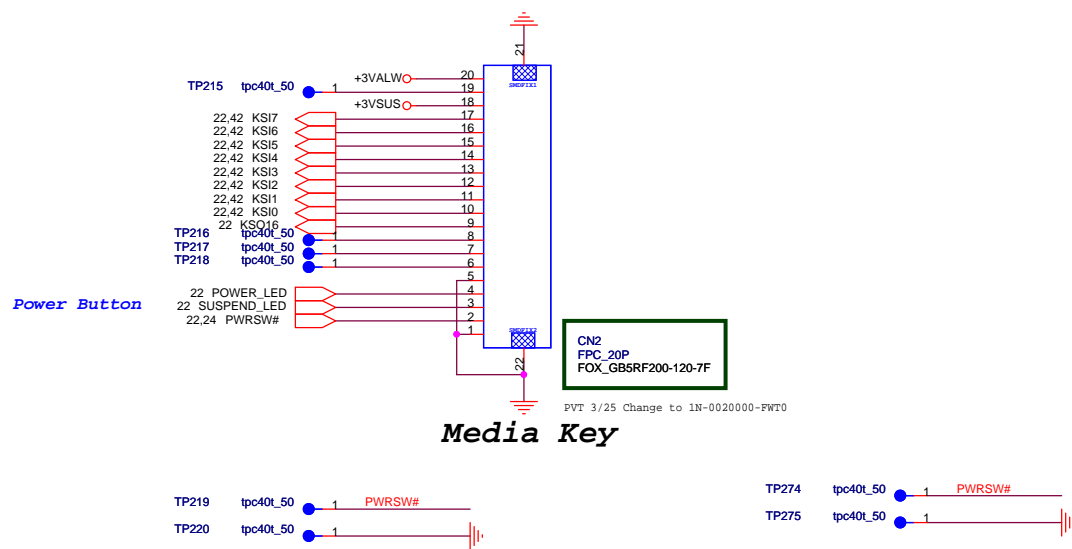


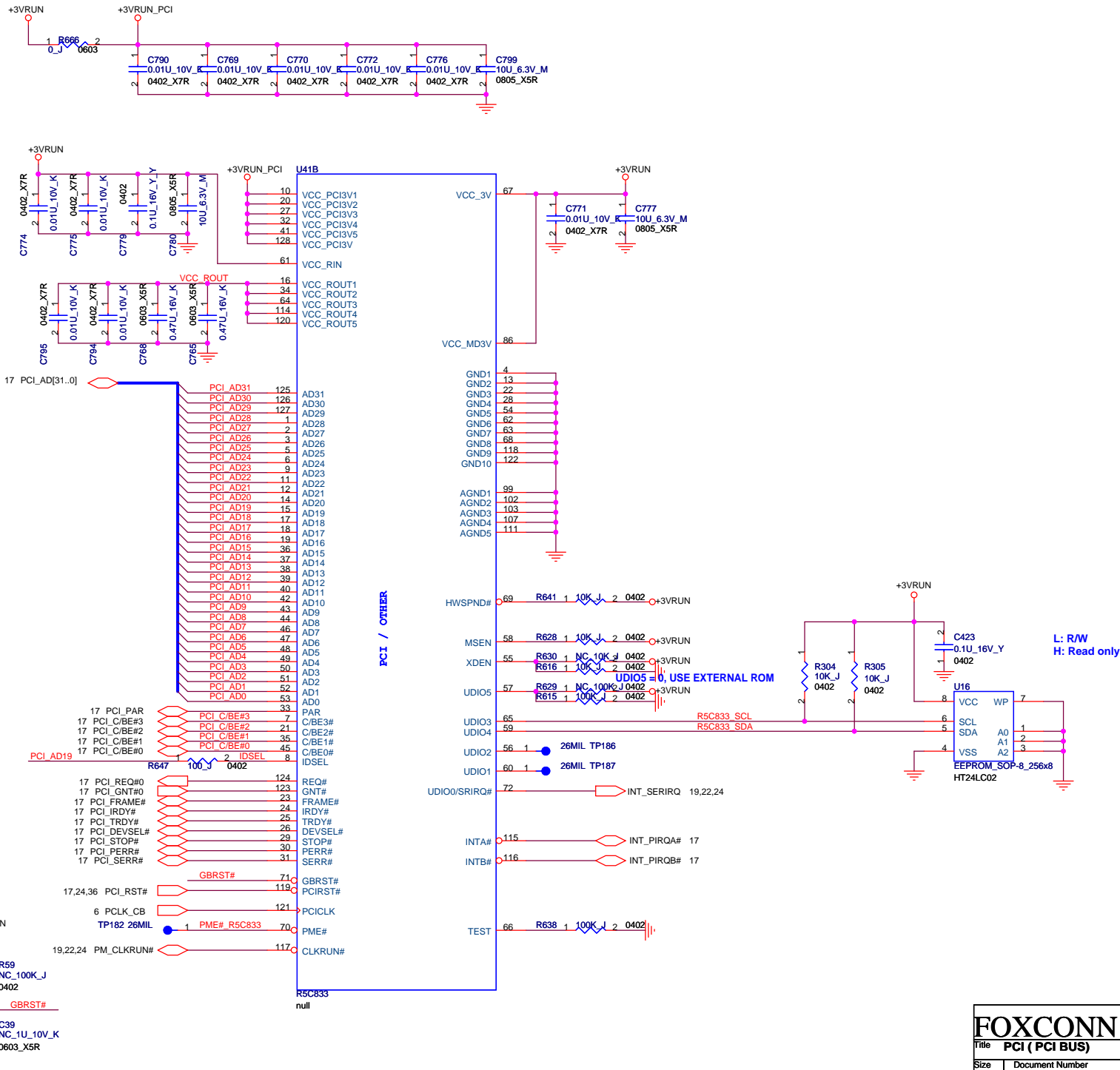
PVT 3/27 For ODD\_DP# function improvement

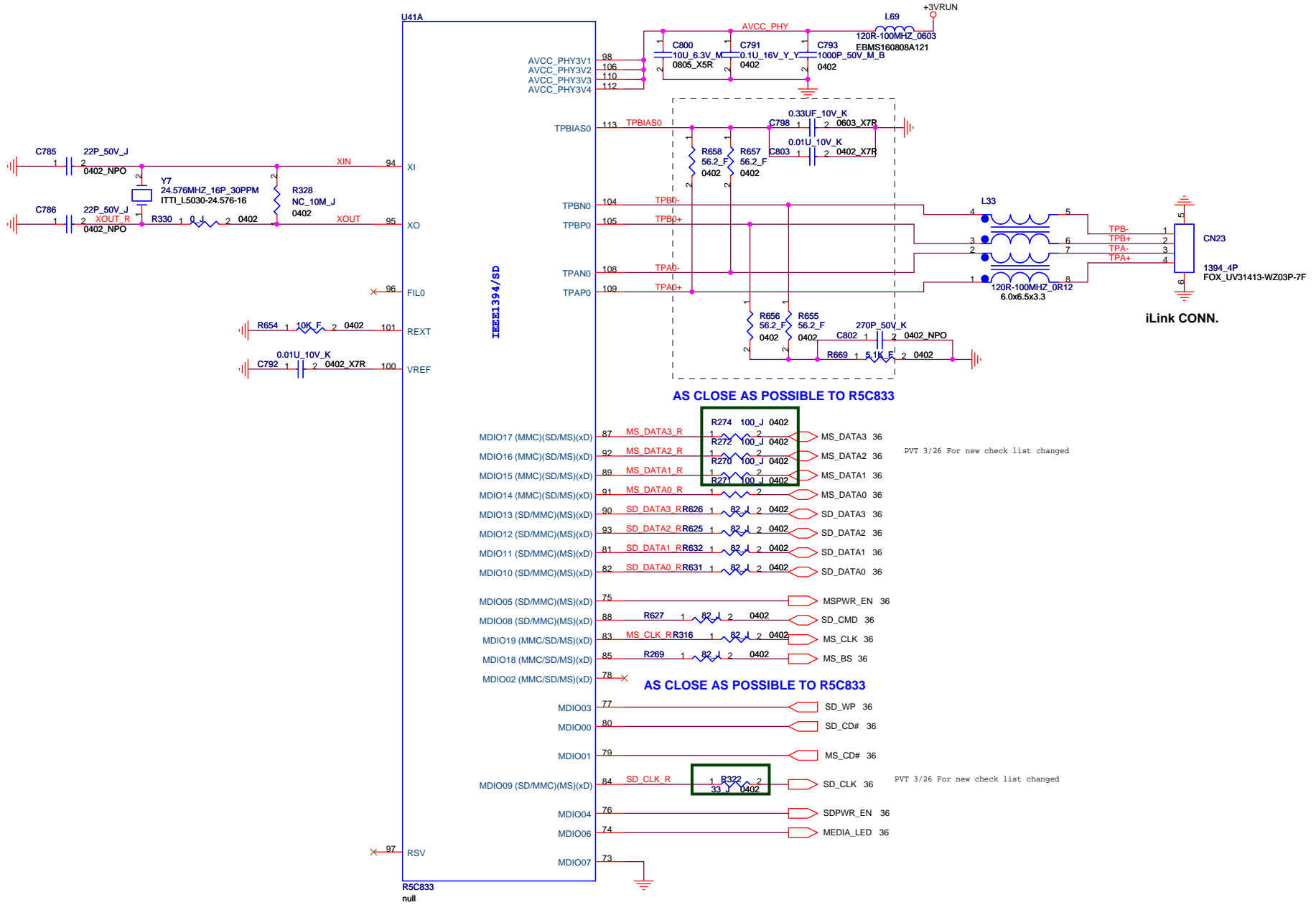


DEFAULT LOW IN S5/S4/S3









AS CLOSE AS POSSIBLE TO R5C833

PVT 3/26 For new check list changed

AS CLOSE AS POSSIBLE TO R5C833

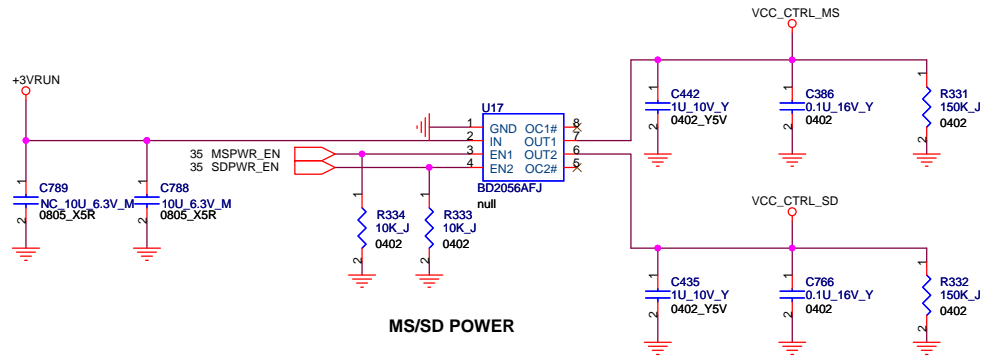
PVT 3/26 For new check list changed

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

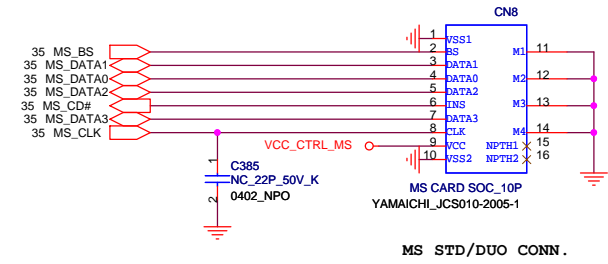
Title **PCI (iLINK)**

Size A3	Document Number M760	Rev 1.0
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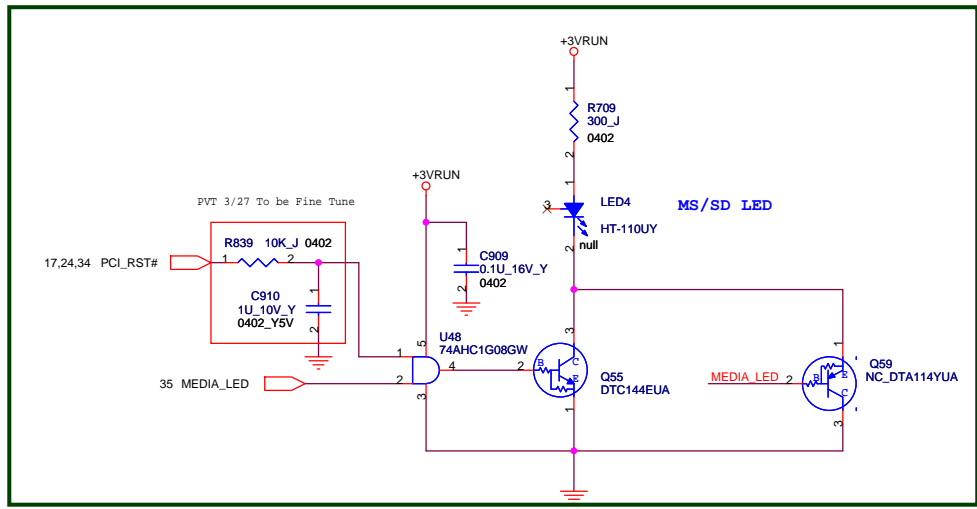
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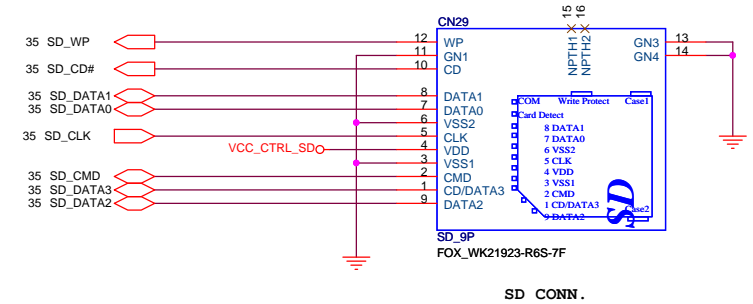
MS/SD POWER



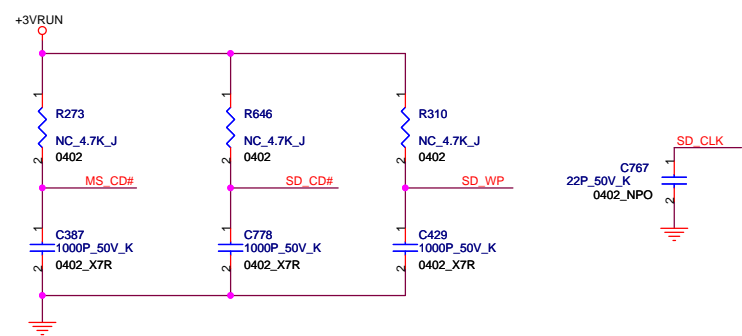
MS STD/DUO CONN.



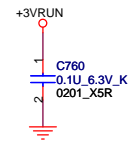
PVT 3/27 Reserve the MEDIA\_LED control Active Low Schematic

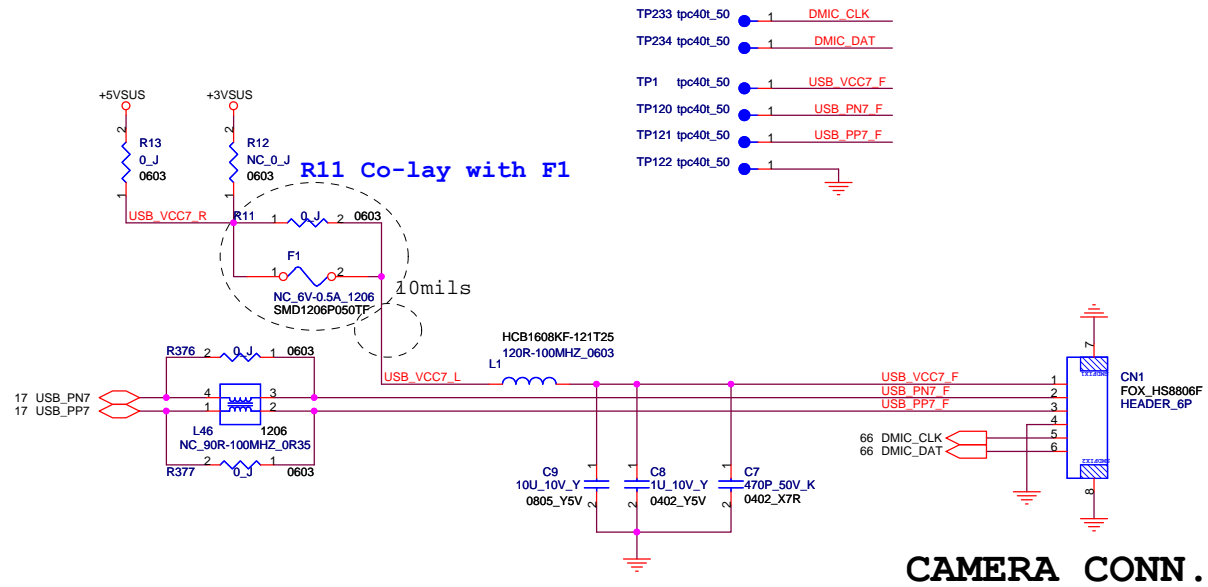


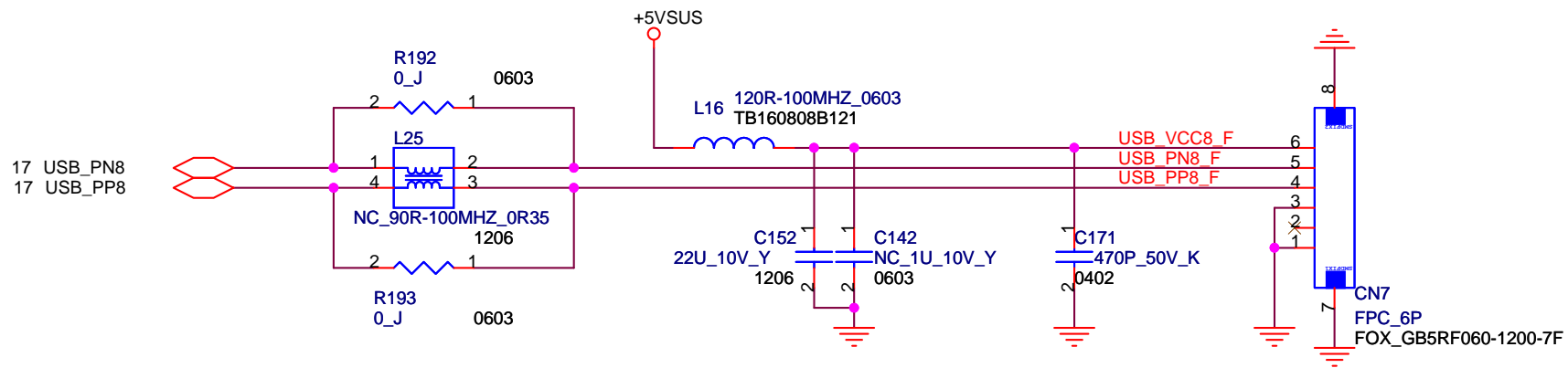
SD CONN.



For EMI

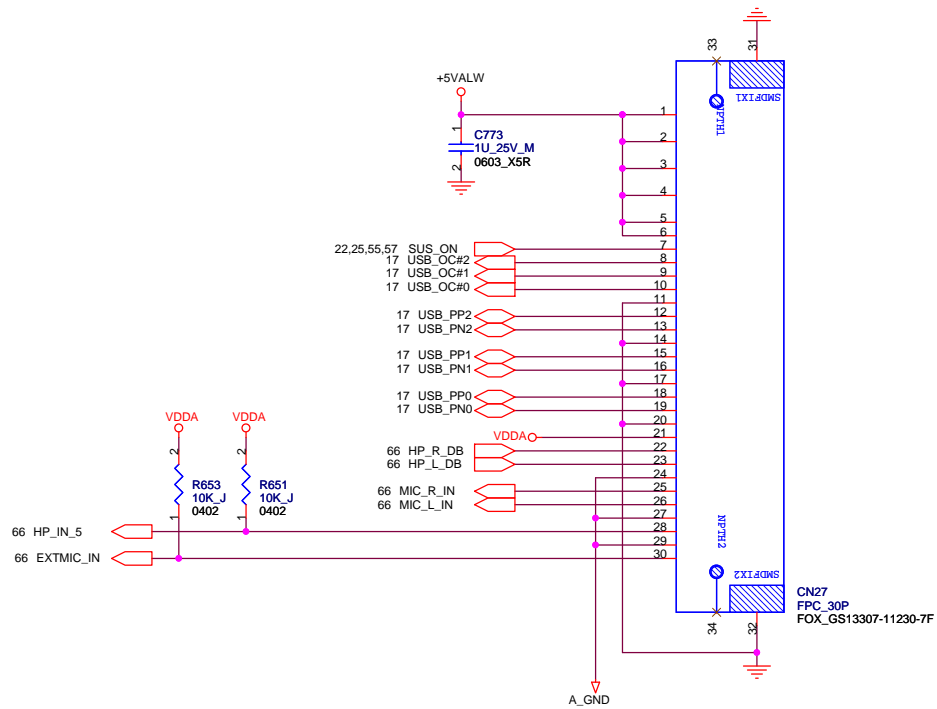


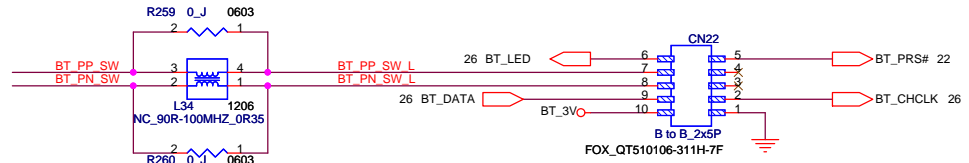
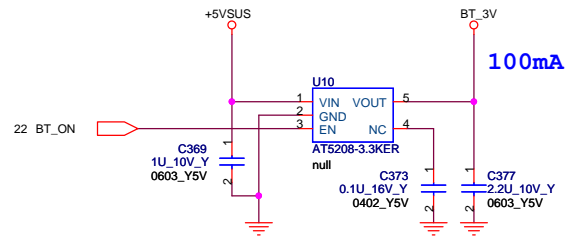




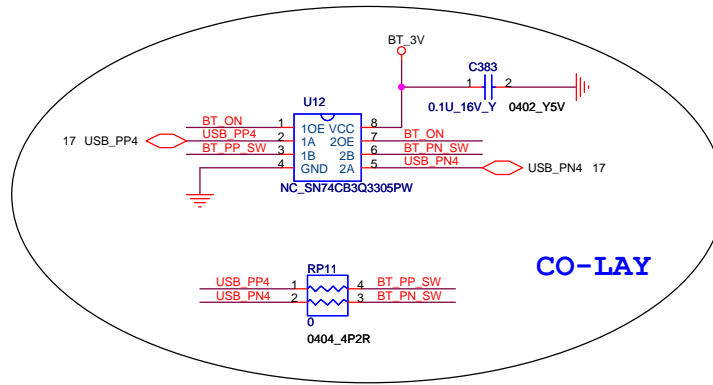
# Felica Connector

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>FELICA</b>			
Size	Document Number	Rev	
A	M760	1.0	
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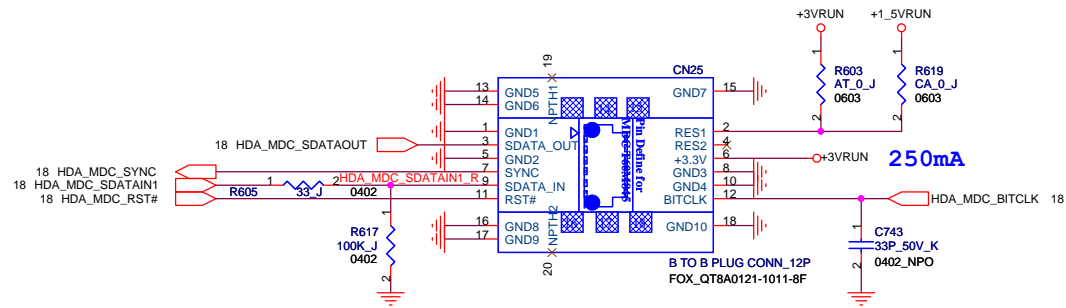
## Bluetooth CONN.



<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title <b>Bluetooth</b>		
Size A3	Document Number M760	Rev 1.0
Date: Thursday, March 27, 2008	Sheet 40	of 89

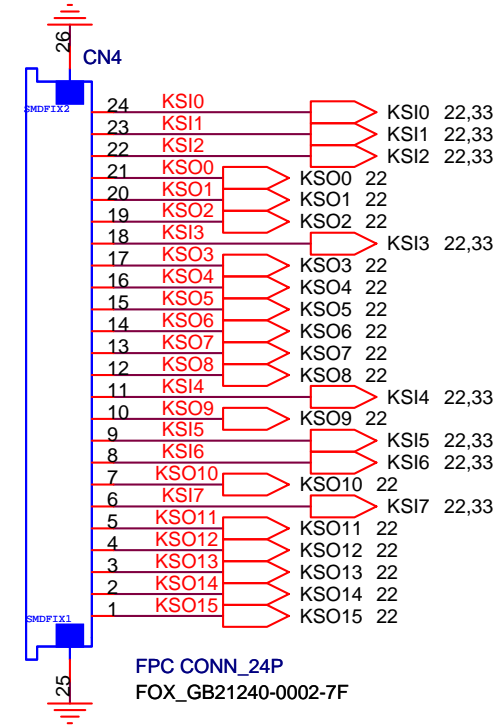
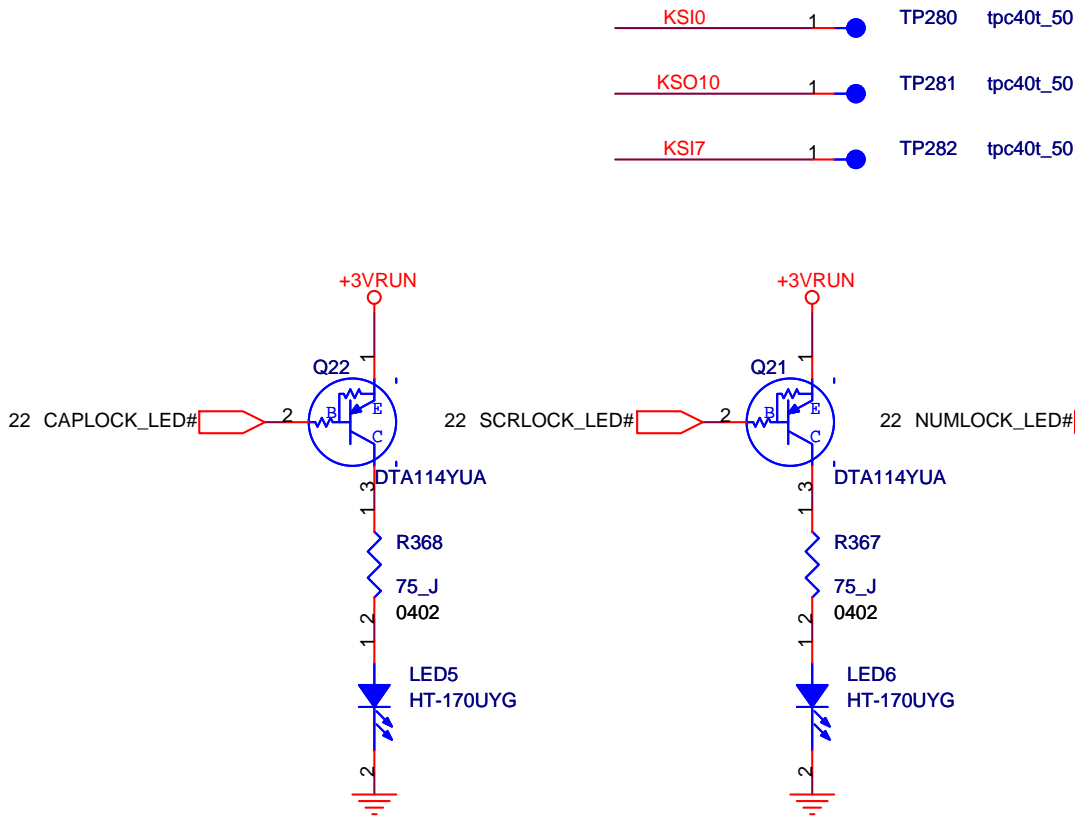


# MDC CONN.



MS90 modem module only (1.5V)

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>MDC</b>			
Size A3	Document Number M760	Rev 1.0	
Date:	Thursday, March 27, 2008	Sheet	41 of 89

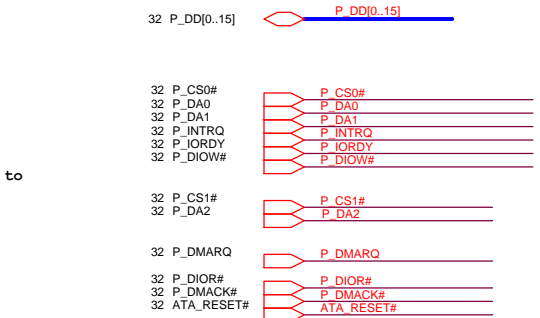
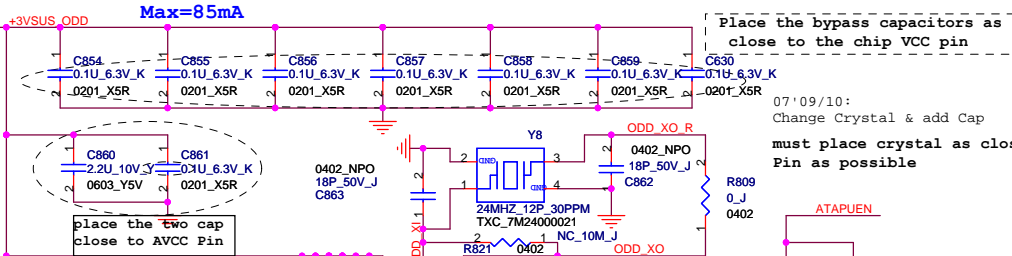


**KBC CNN**

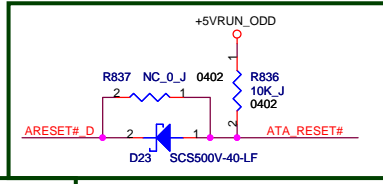
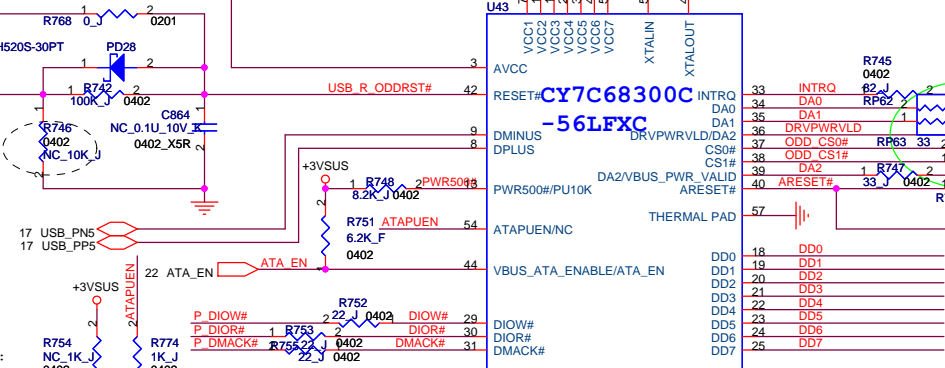
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>KB Connector</b>			
Size A	Document Number M760	Rev 1.0	
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# USB2.0-->PATA BRIDGE

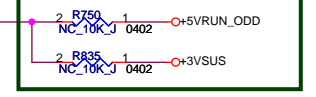
20070829(ODD\_RESET#):  
 1. Change from 0.22uF to 0.1uF net-work with a 10ms time constant;  
 2. Add a diode to avoid potential voltage feedback.



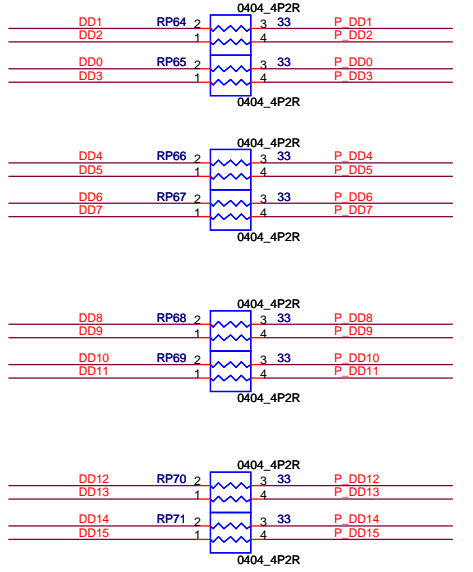
07'09/03:  
 Reserve discharge R



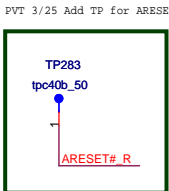
PVT 3/27 Add the power leakage solution



PVT 3/25 Reserve the Power Source to +3VSUS by MOR



\*Layout Note:  
 Please place these Series R close IC Pin

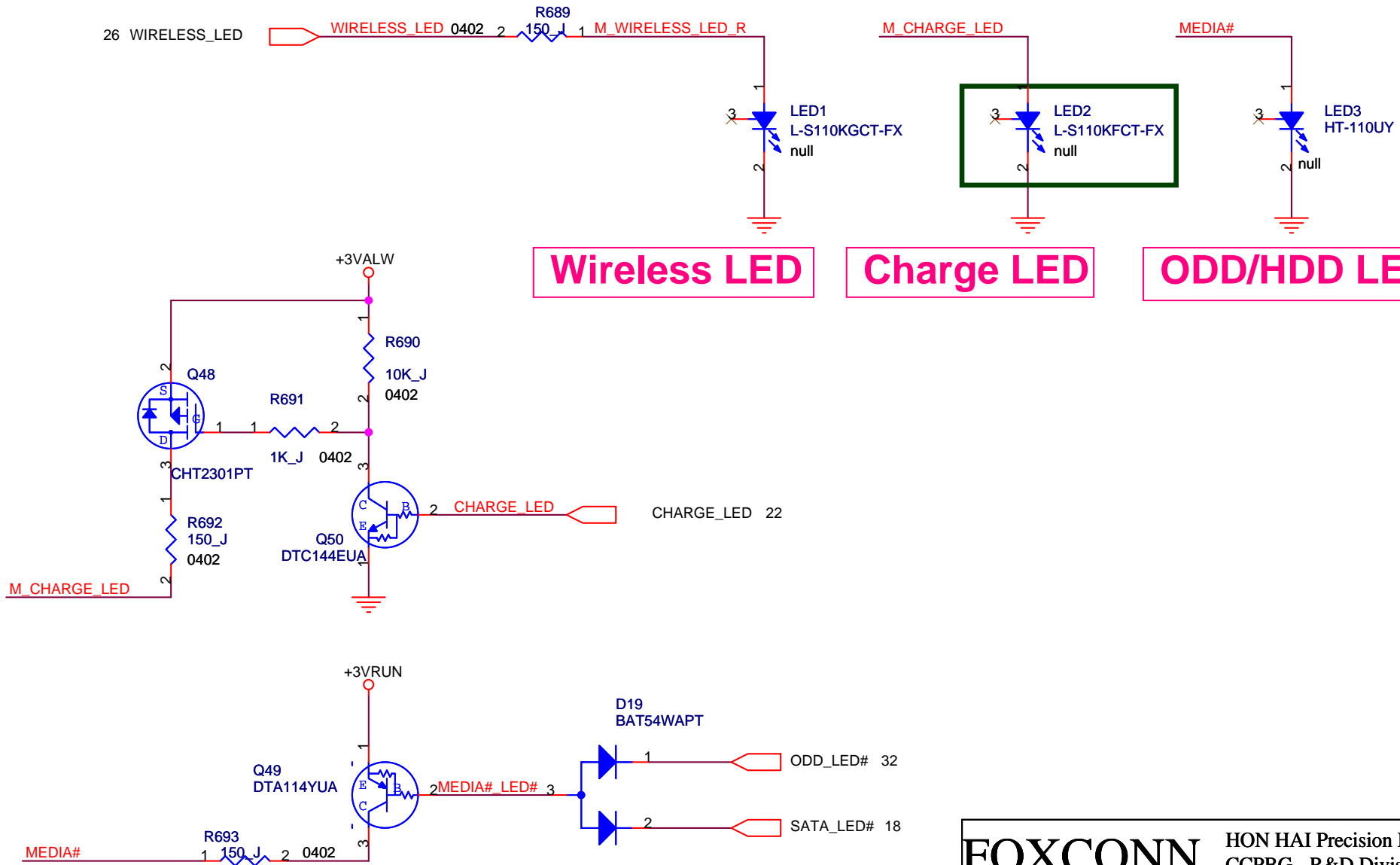


07'0924:  
 For part not approve, Change

PVT 3/25 Add TP for ARESET#\_R

07'0928:  
 Follow PAE suggestion, connect ARESET# instead of GND.  
 CY7C68300 Ver. A has issue: EEPROM Data will lost.  
 07'08/30(follow demo SCH):  
 1. Address : '100';  
 2. WP connect to ARESET#

PVT 3/18 Change back to DVT1 solution

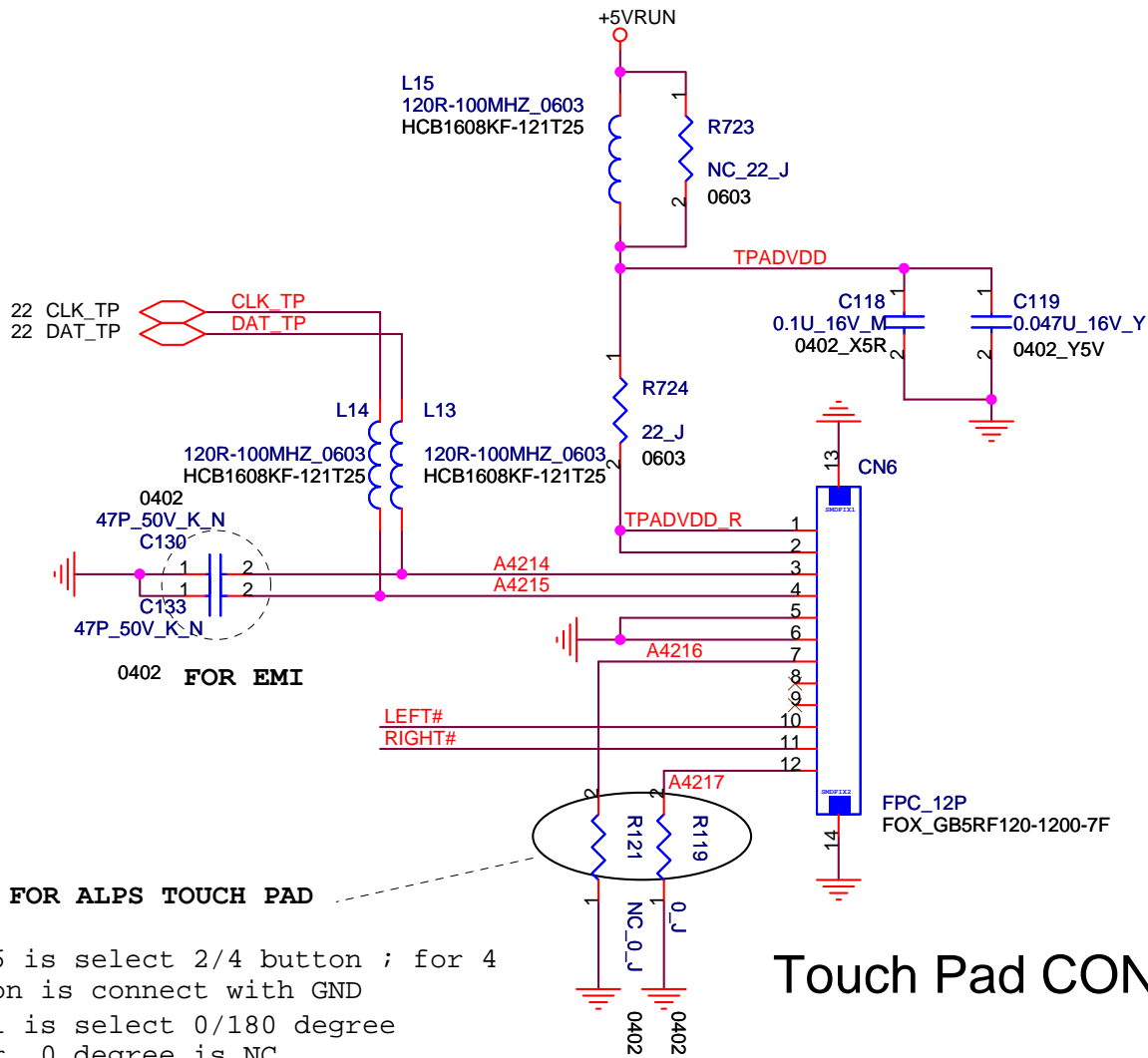


Wireless LED

Charge LED

ODD/HDD LED

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>Status LED</b>			
Size A	Document Number M760	Rev 1.0	
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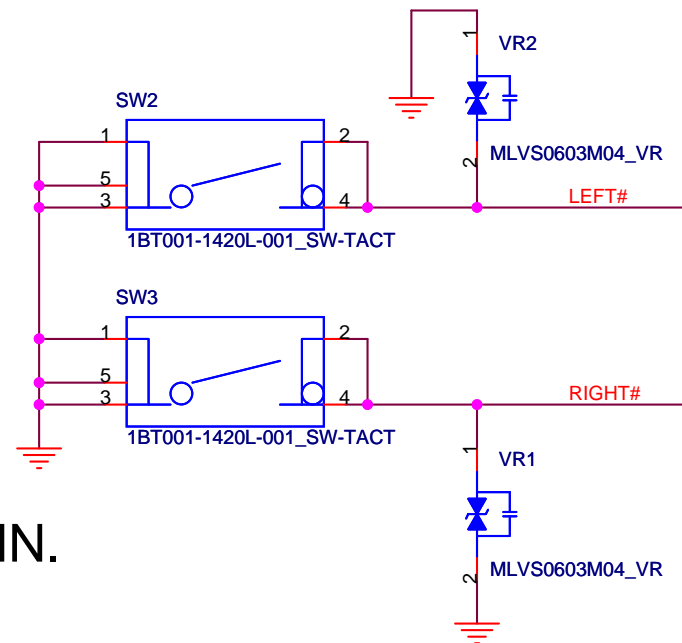


FOR ALPS TOUCH PAD

PIN 6 is select 2/4 button ; for 4 button is connect with GND  
 PIN 1 is select 0/180 degree ; for 0 degree is NC

### Touch Pad CONN.

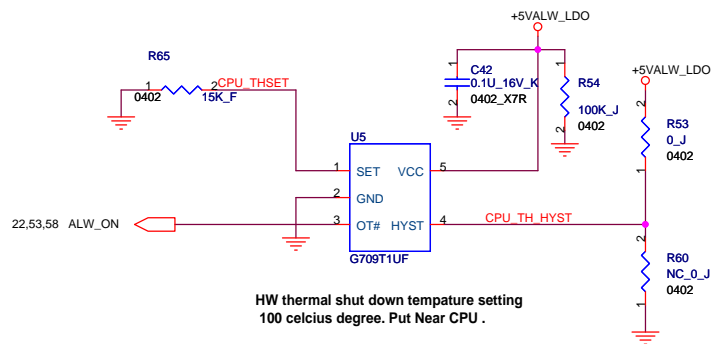
### TP\_LEFT Button



### TP\_Right Button

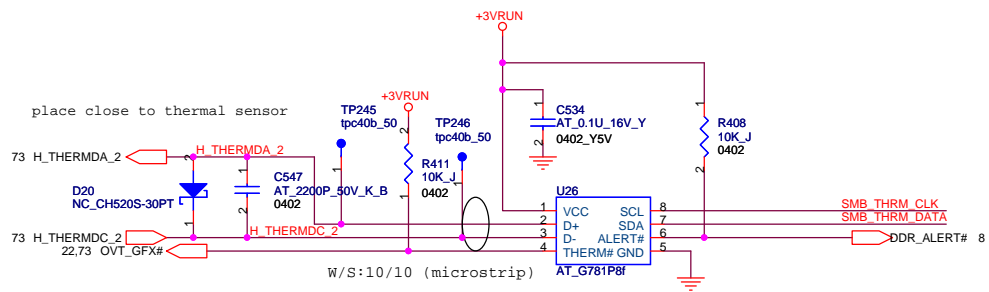
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>Touch Pad</b>			
Size A	Document Number M760	Rev 1.0	
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# HW THERMAL PROTECTION





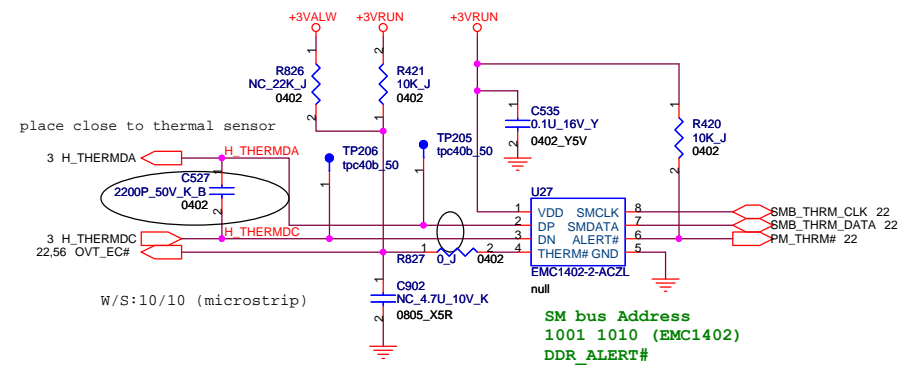
## GMCH/VGA SENSOR G781P8f



SM bus Address  
1001 1000 (G781)

Place Thermal-Sensor near NB

## CPU/GMCH/DDR SENSOR EMC1402-2-ACZL

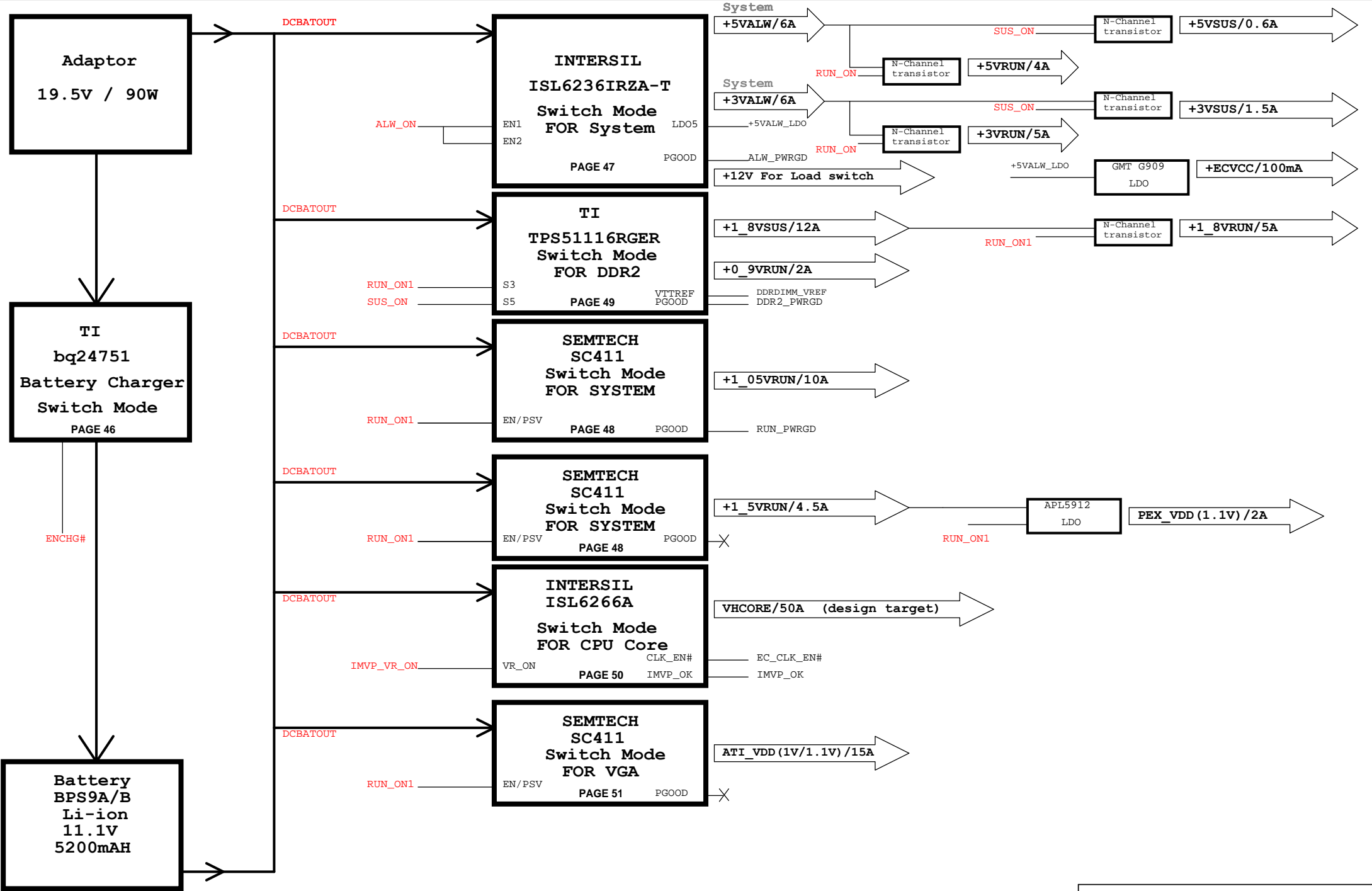


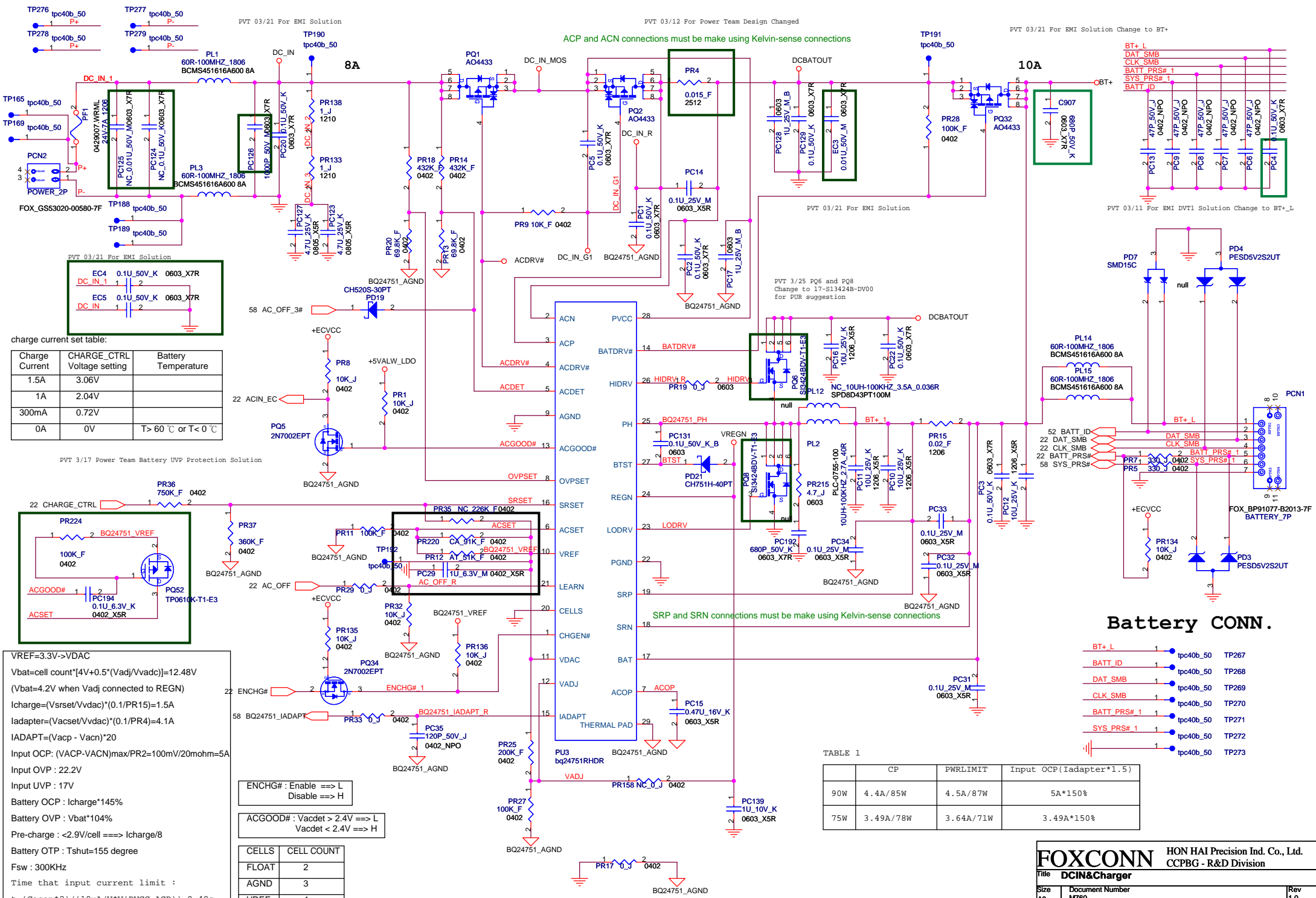
SM bus Address  
1001 1010 (EMC1402)  
DDR\_ALERT#

Place Thermal-Sensor near DDR

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title <b>Thermal-Sensor</b>		
Size A3	Document Number M760	Rev 1.0
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charge current set table:

Charge Current	CHARGE_CTRL Voltage setting	Battery Temperature
1.5A	3.06V	
1A	2.04V	
300mA	0.72V	
0A	0V	T > 60 °C or T < 0 °C

VREF=3.3V->VDAC  
 $V_{bat} = \text{cell count} * [4V + 0.5 * (V_{adj} / V_{vdc})] = 12.48V$   
 $(V_{bat} = 4.2V \text{ when } V_{adj} \text{ connected to REGN})$   
 $I_{charge} = (V_{srset} / V_{vdc}) * (0.1 / PR15) = 1.5A$   
 $I_{adapter} = (V_{acset} / V_{vdc}) * (0.1 / PR4) = 4.1A$   
 $IADAPT = (V_{acp} - V_{vacn}) * 20$   
 Input OCP:  $(V_{acp} - V_{vacn})_{max} / PR2 = 100mV / 20m\Omega = 5A$   
 Input OVP: 22.2V  
 Input UVP: 17V  
 Battery OCP:  $I_{charge} * 145\%$   
 Battery OVP:  $V_{bat} * 104\%$   
 Pre-charge:  $< 2.9V / \text{cell} \implies I_{charge} / 8$   
 Battery OTP:  $T_{shut} = 155 \text{ degree}$   
 $F_{sw} = 300KHz$   
 Time that input current limit:  $t = (C_{acop} * 2) / (18\mu A / V * (V_{vdc} - ACP)) = 0.48s$

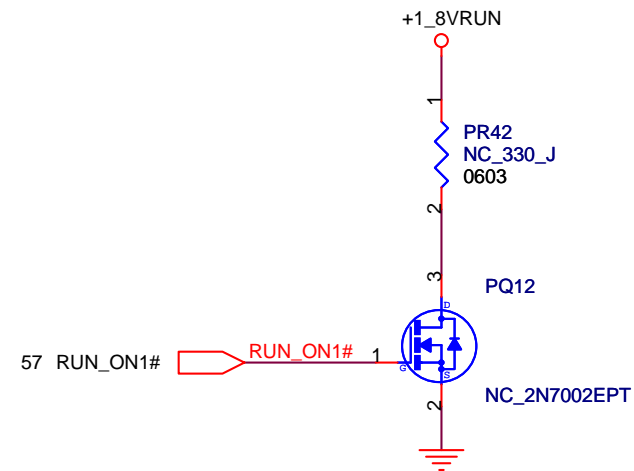
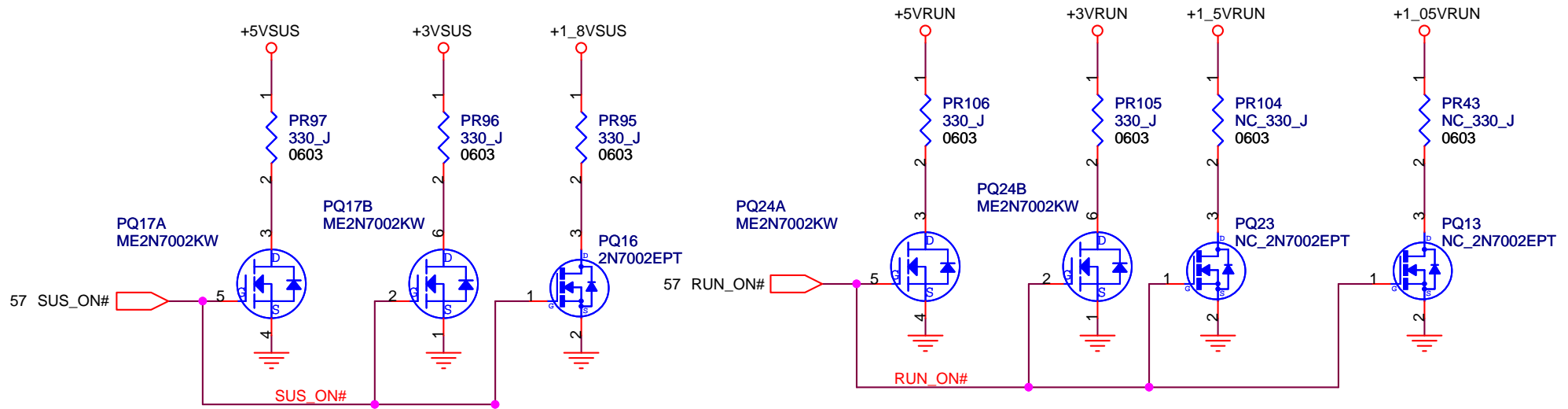
ENCHG# : Enable ==> L  
 Disable ==> H

ACGOOD# :  $V_{acdet} > 2.4V \implies L$   
 $V_{acdet} < 2.4V \implies H$

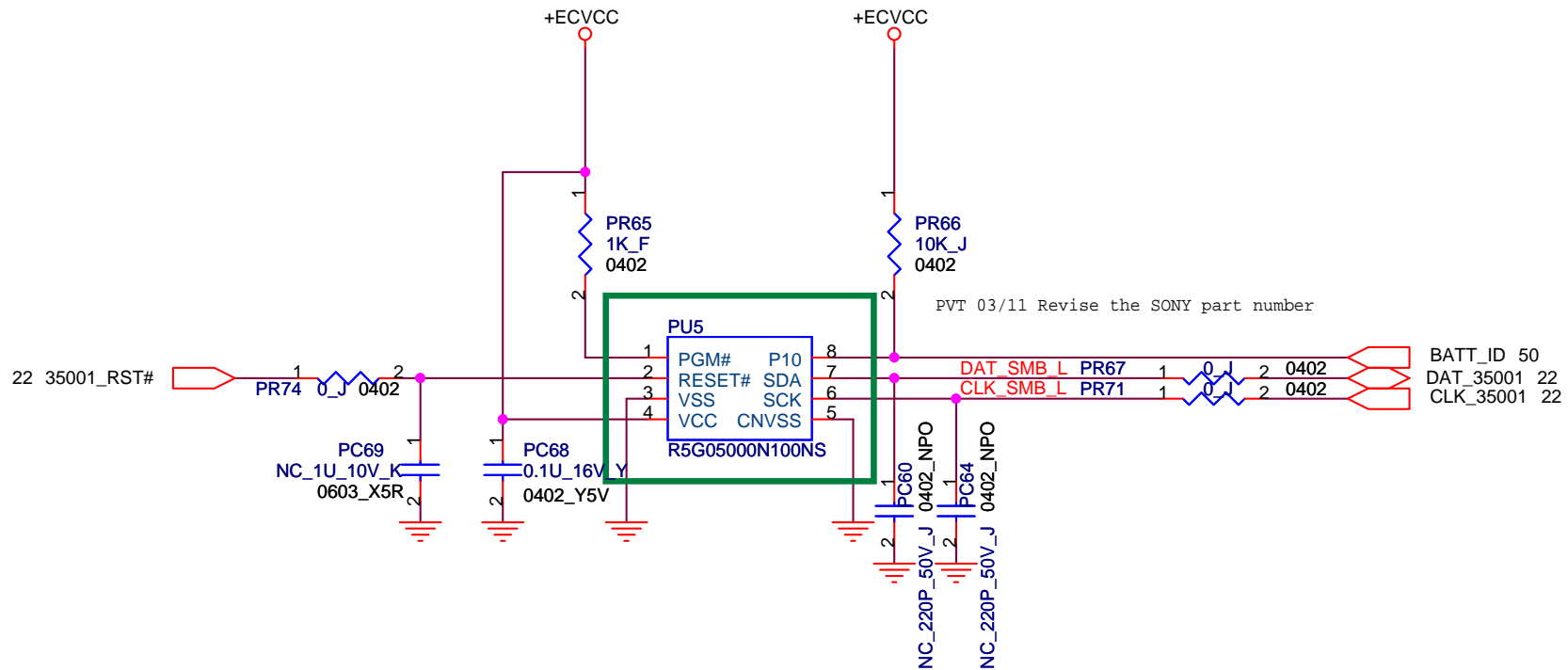
CELLS	CELL COUNT
FLOAT	2
AGND	3
VREF	4

TABLE 1

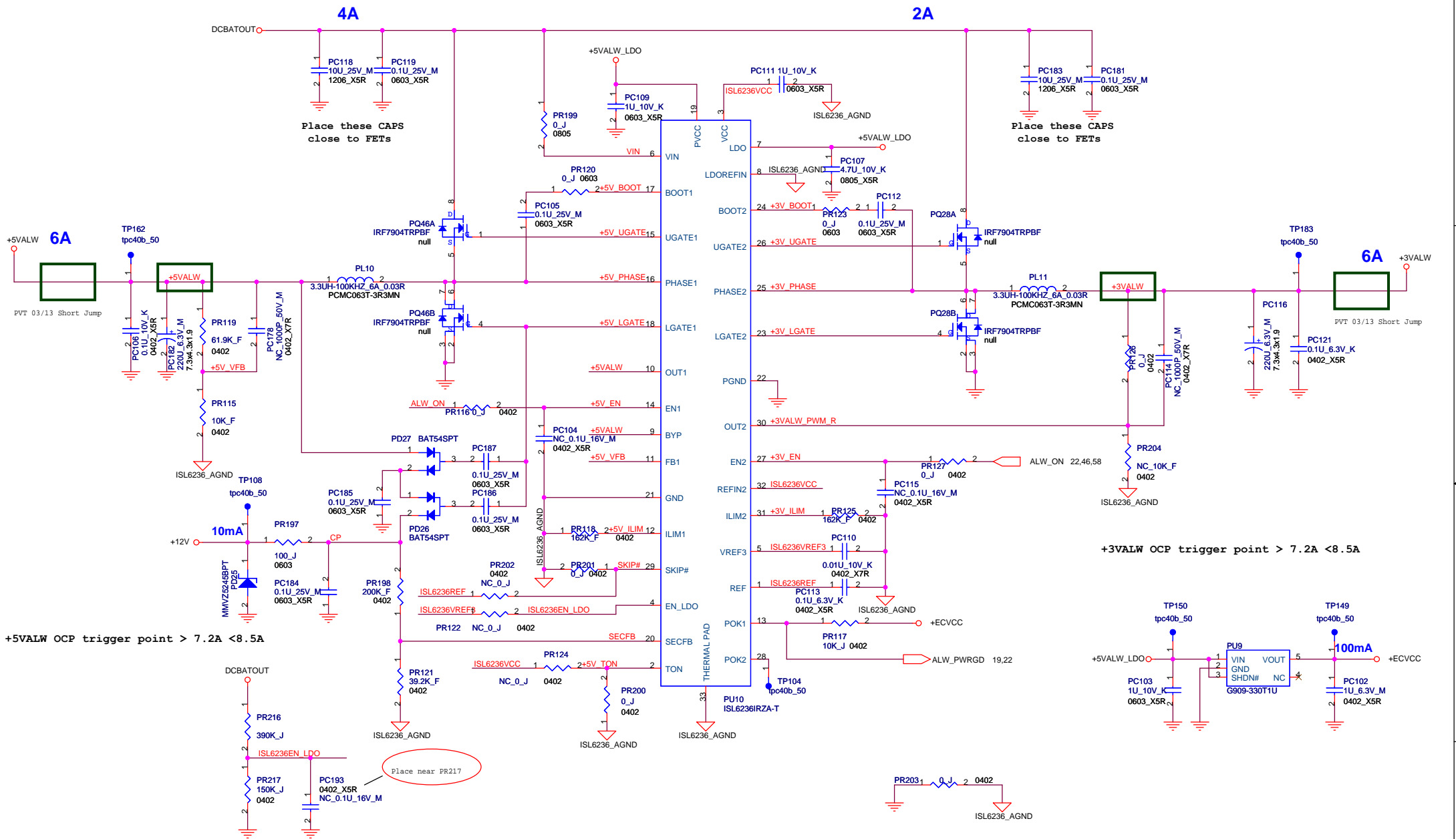
	CP	PWRLIMIT	Input OCP (Iadapter*1.5)
90W	4.4A/85W	4.5A/87W	5A*150%
75W	3.49A/78W	3.64A/71W	3.49A*150%



<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>DISCHARGE CIRCUIT</b>			
Size A	Document Number M760	Rev 1.0	
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<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title			
<b>Identify IC</b>			
Size	Document Number		Rev
A	M760		1.0
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+5VALW OCP trigger point > 7.2A < 8.5A

+3VALW OCP trigger point > 7.2A < 8.5A

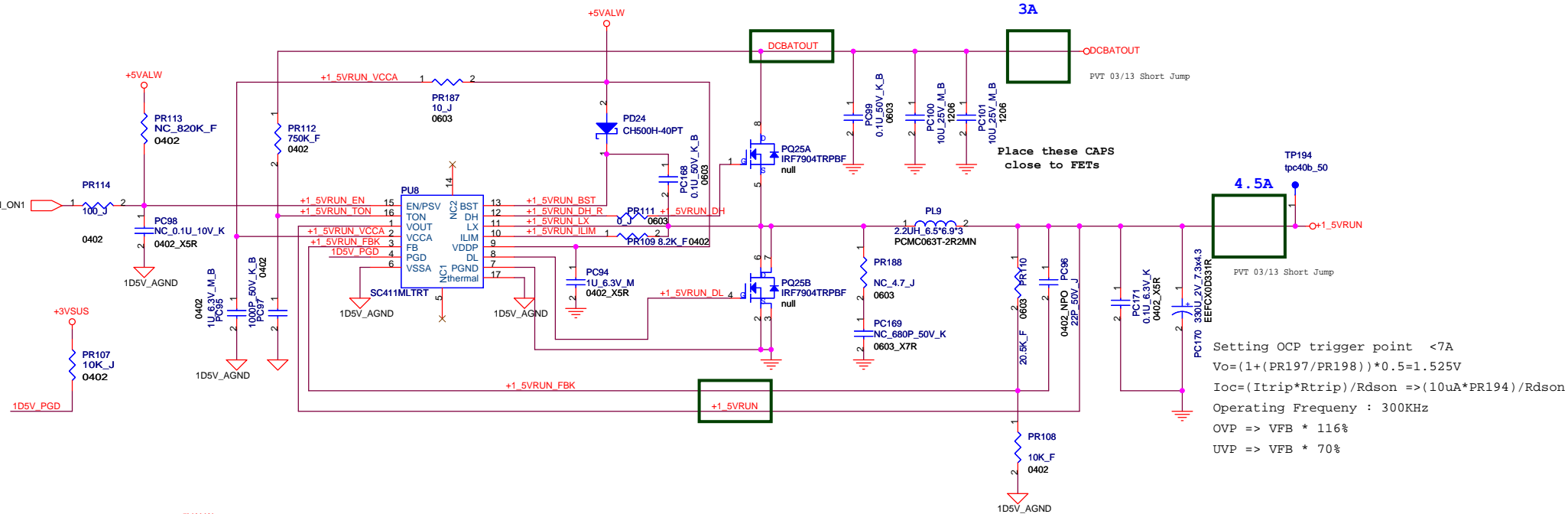
TON	Operating Frequency (+5VALW/+3VALW)
VCC	200KHz/300KHz
REF (OPEN)	400KHz/300KHz
GND	400KHz/500KHz

SKIP#	Operating Mode
GND	Pulse-Skipping
REF	Ultrasonic-Skip
VCC	PWM

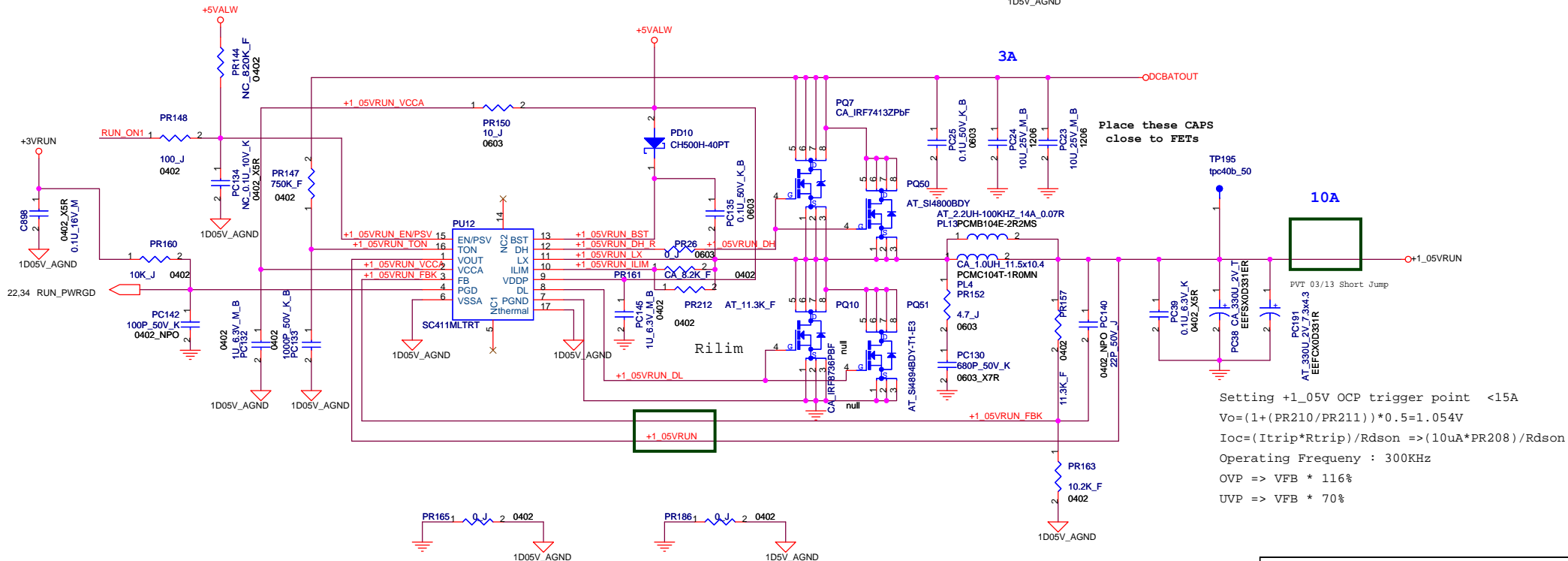
$$L = VOUT(VIN - VOUT) / (VIN * F * LIR * ILOAD(MAX))$$

$$Rocp = (Iocp - Iripple/2) * (10 * Rds(on)) / 5u$$

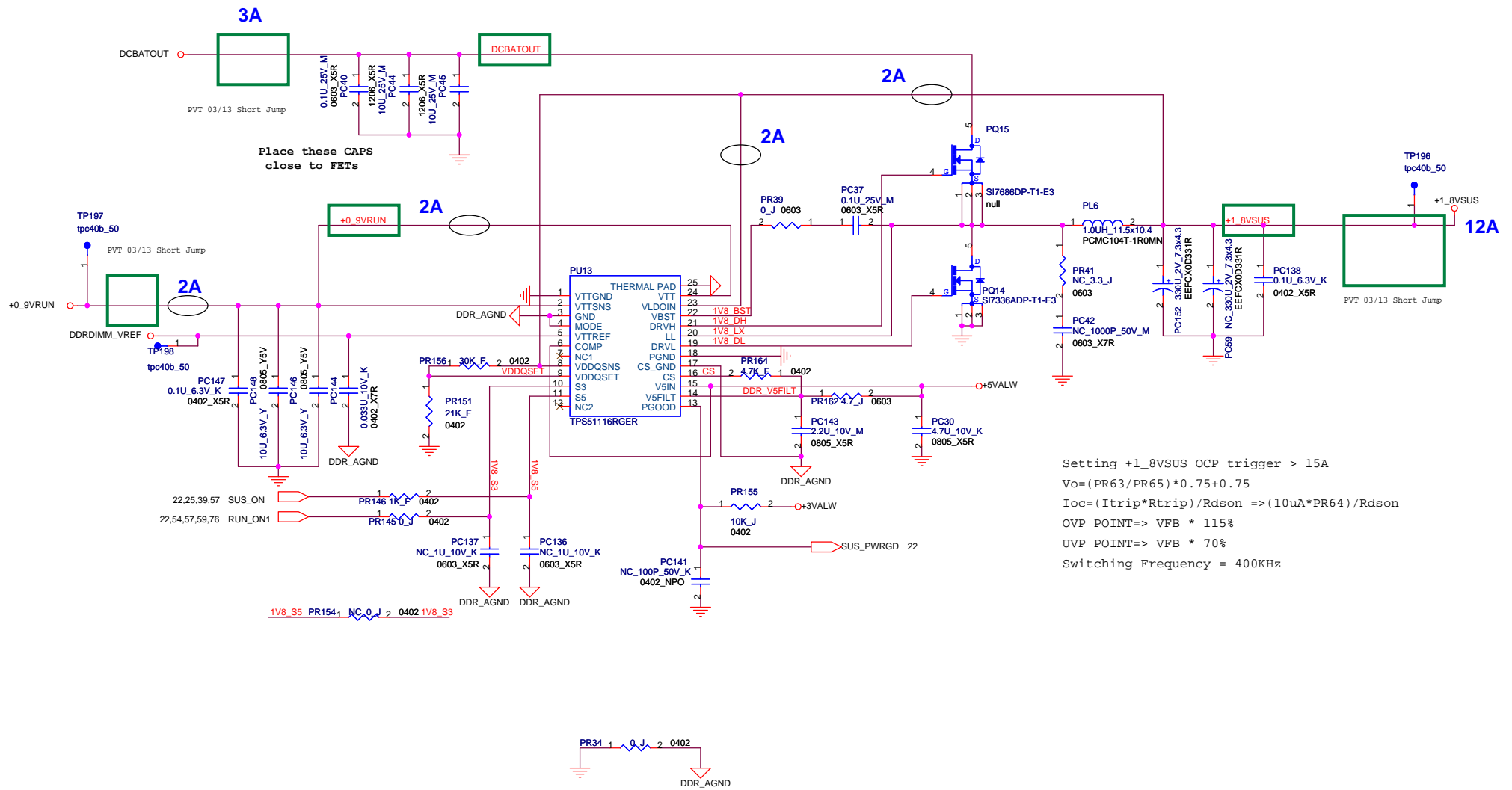
$$+5VALW = ((PR233 / PR235) + 1) * VFB1 = 5.033V$$



Setting OCP trigger point <7A  
 $V_o = (1 + (PR197/PR198)) * 0.5 = 1.525V$   
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} = (10\mu A * PR194) / R_{dson}$   
 Operating Frequency : 300KHz  
 OVP => VFB \* 116%  
 UVP => VFB \* 70%



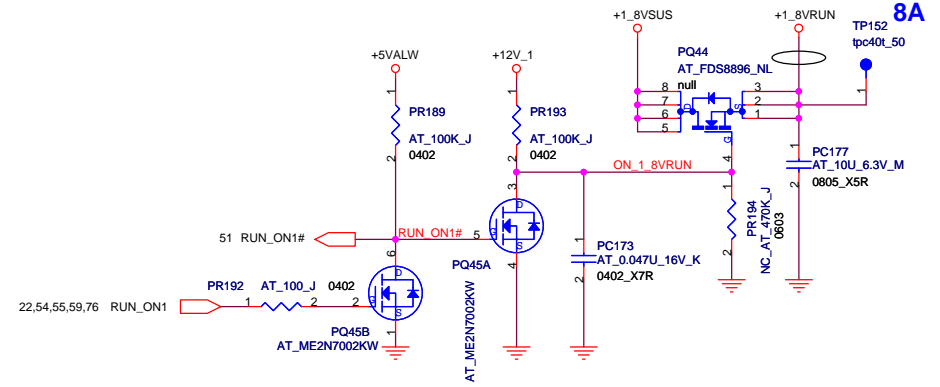
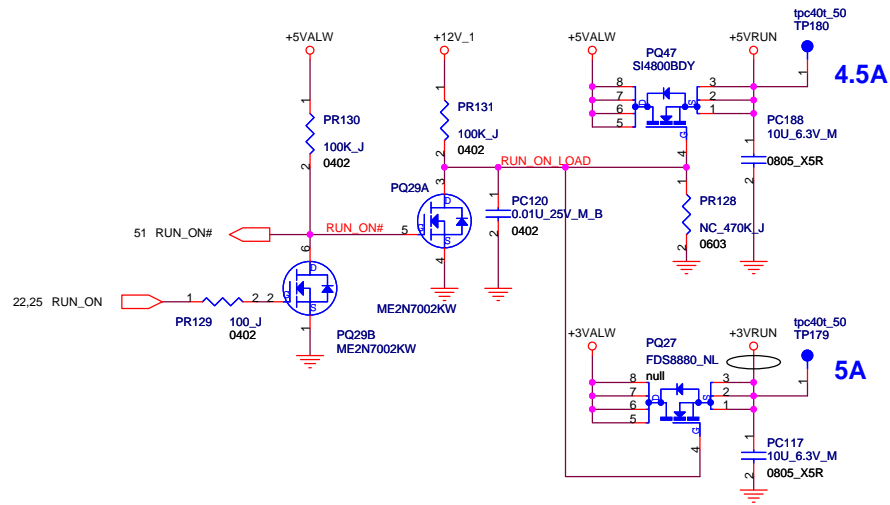
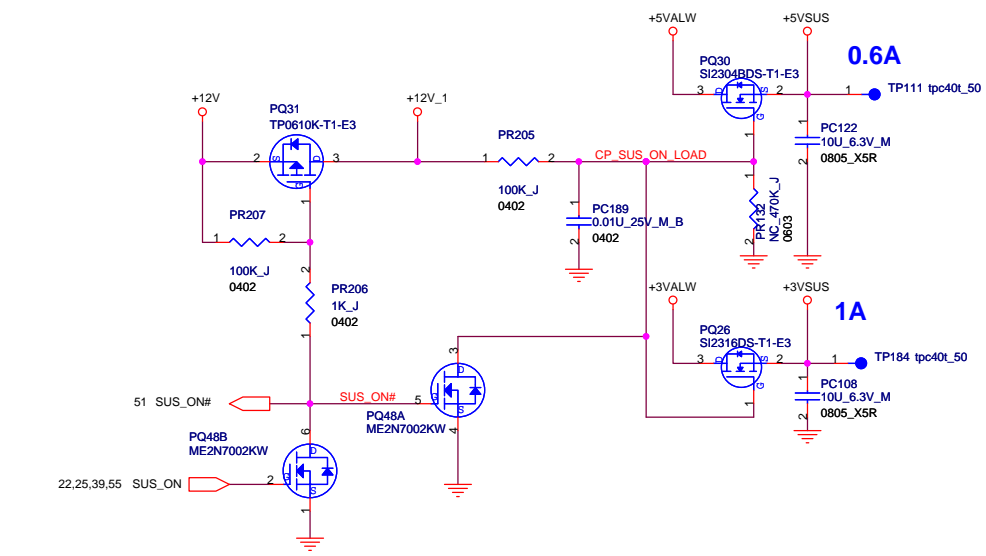
Setting +1.05V OCP trigger point <15A  
 $V_o = (1 + (PR210/PR211)) * 0.5 = 1.054V$   
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} = (10\mu A * PR208) / R_{dson}$   
 Operating Frequency : 300KHz  
 OVP => VFB \* 116%  
 UVP => VFB \* 70%



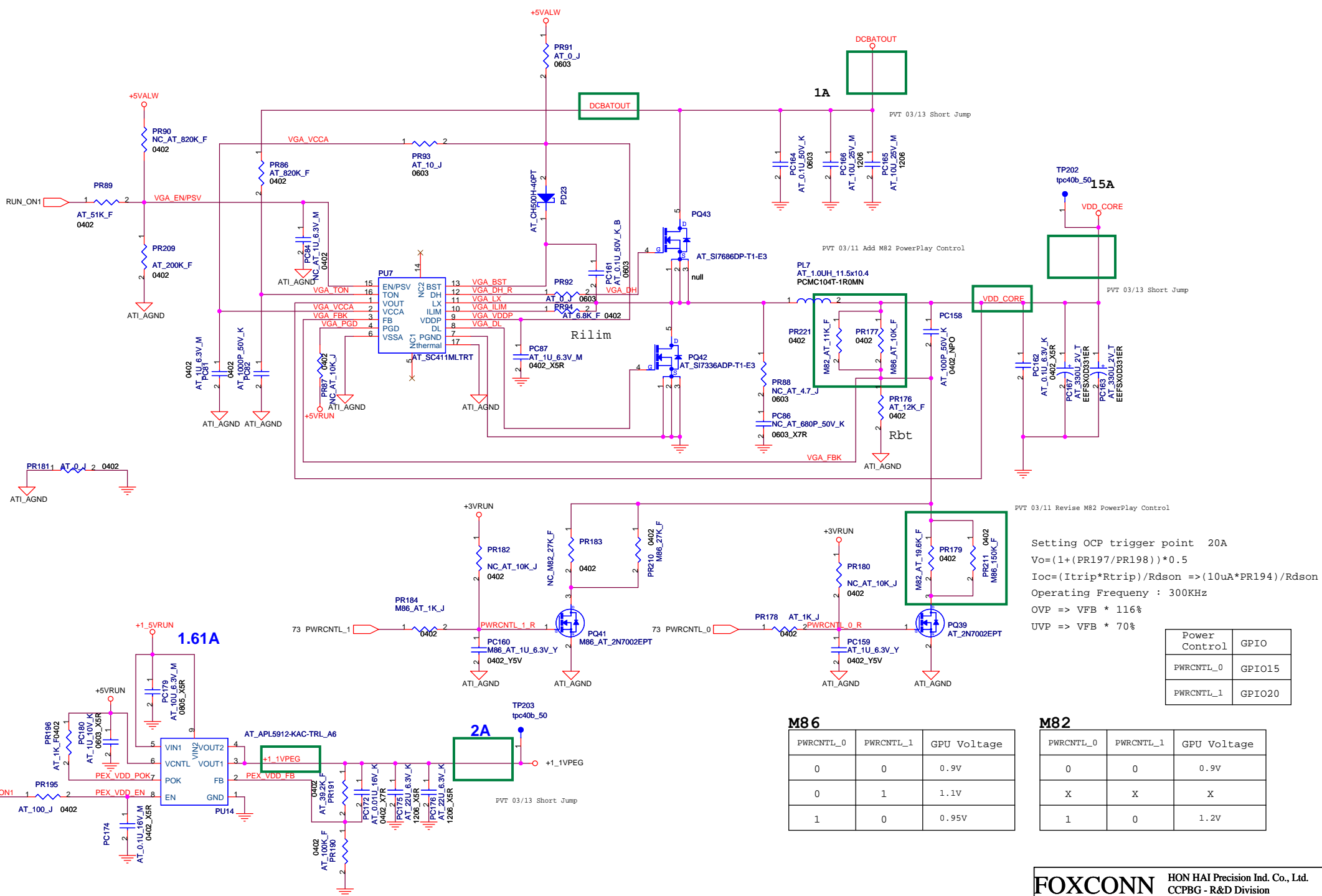
Setting +1.8VSUS OCP trigger > 15A  
 $V_o = (PR63/PR65) * 0.75 + 0.75$   
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} => (10\mu A * PR64) / R_{dson}$   
 OVP POINT=> VFB \* 115%  
 UVP POINT=> VFB \* 70%  
 Switching Frequency = 400KHz











PVT 03/11 Revise M82 PowerPlay Control

Setting OCP trigger point 20A  
 $V_o = (1 + (PR197/PR198)) * 0.5$   
 $I_{oc} = (I_{trip} * R_{trip}) / R_{dson} \Rightarrow (10\mu A * PR194) / R_{dson}$   
 Operating Frequency : 300KHz  
 OVP => VFB \* 116%  
 UVP => VFB \* 70%

Power Control	GPIO
PWRCNTL_0	GPIO15
PWRCNTL_1	GPIO20

**M86**

PWRCNTL_0	PWRCNTL_1	GPU Voltage
0	0	0.9V
0	1	1.1V
1	0	0.95V

**M82**

PWRCNTL_0	PWRCNTL_1	GPU Voltage
0	0	0.9V
X	X	X
1	0	1.2V

5

4

3

2

1

D

D

C

C

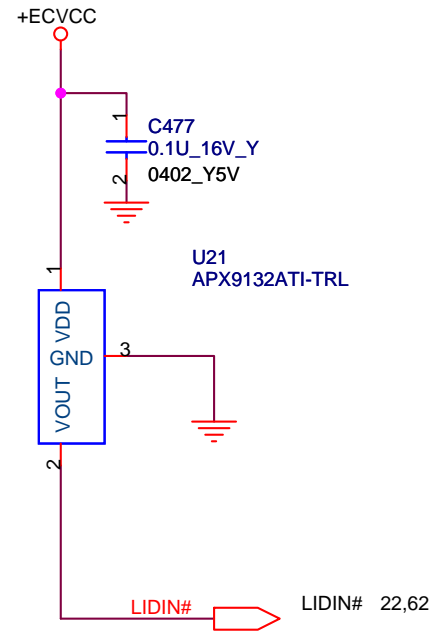
B

B

A

A

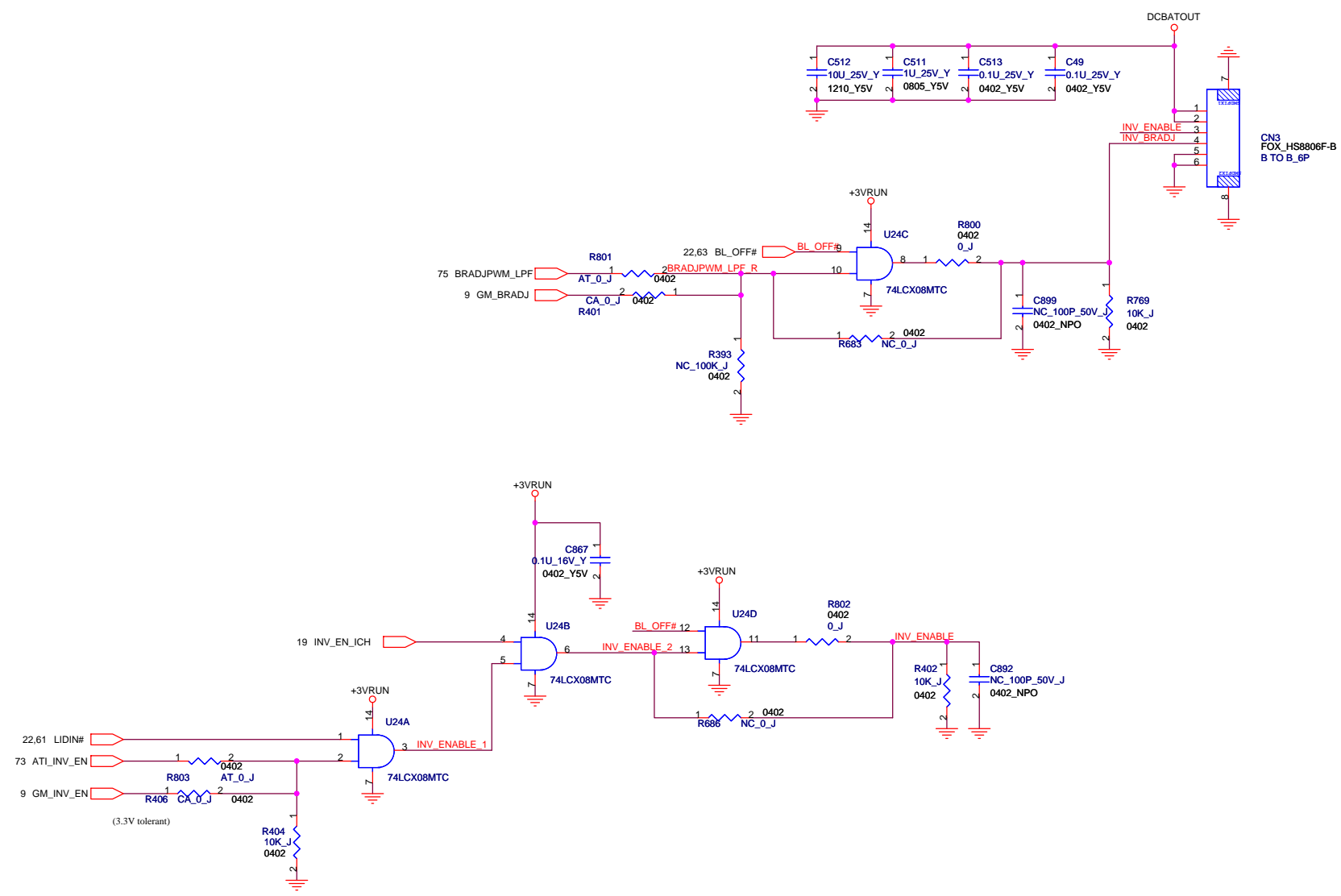
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>GMCH Power</b>		CCPBG - R&D Division	
Size A3	Document Number M760	Rev 1.0	
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## LID Switch

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>LID SWITCH</b>			
Size A	Document Number M760	Rev 1.0	
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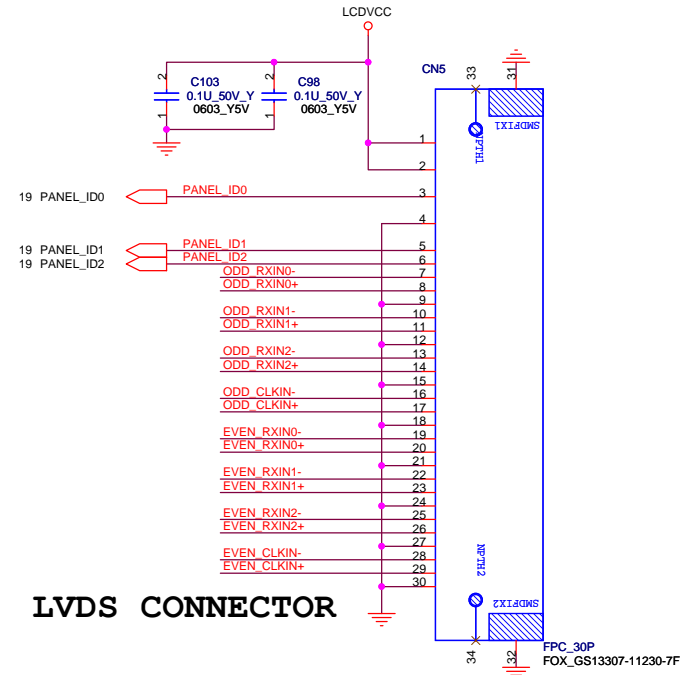
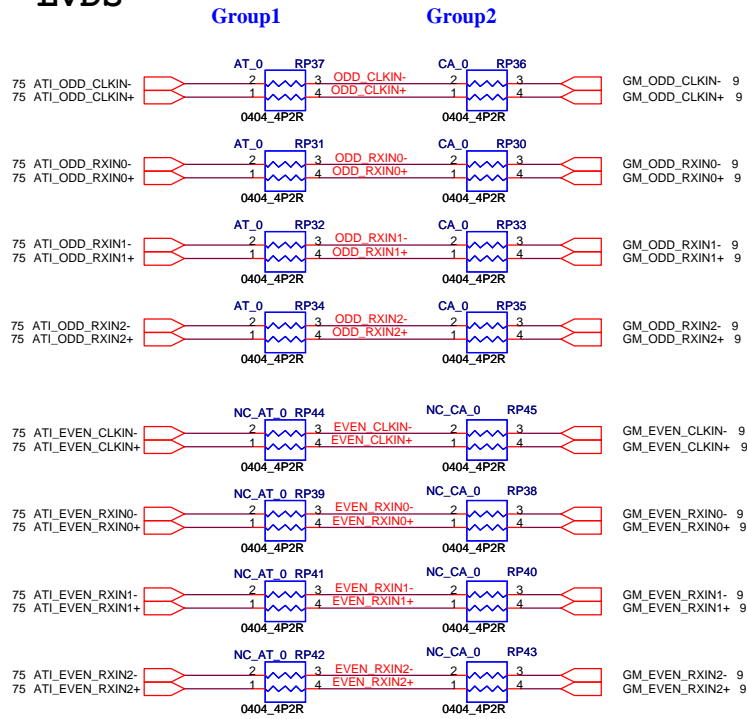
# INVERTER CONN.



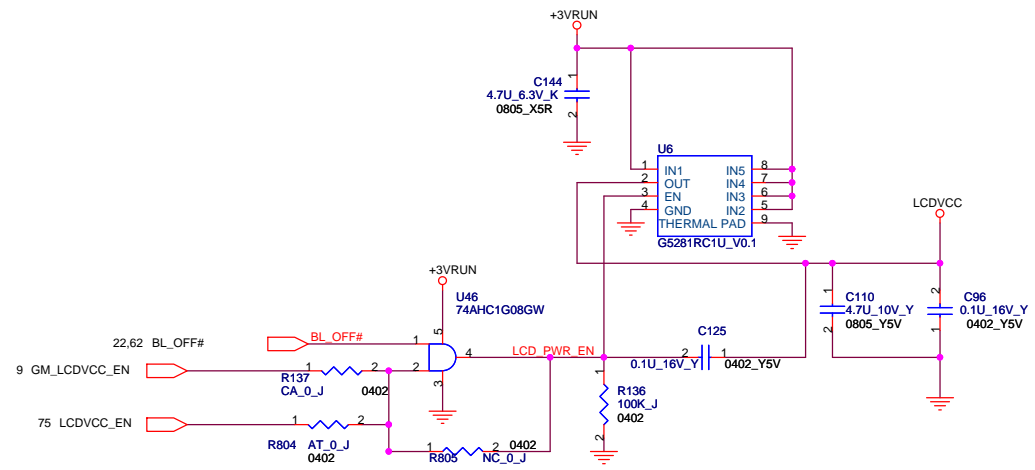
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	<b>Inverter</b>		
Size	Document Number	Rev	
A3	<b>M760</b>	1.0	
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Group1, Group2 should be close

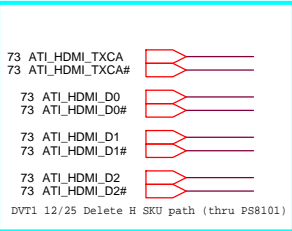
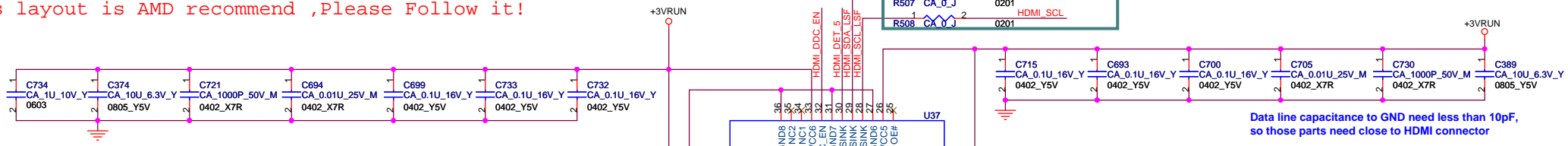
# LVDS



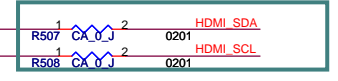
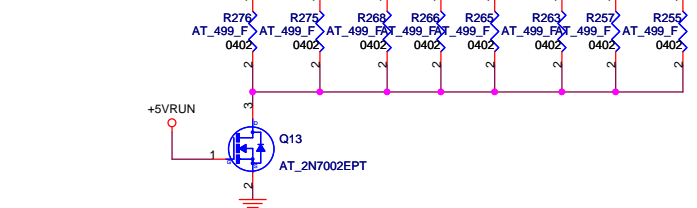
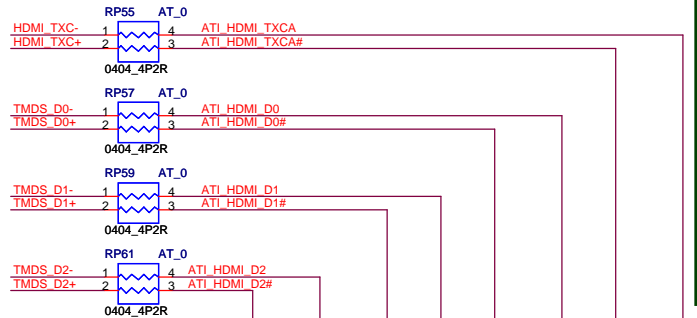
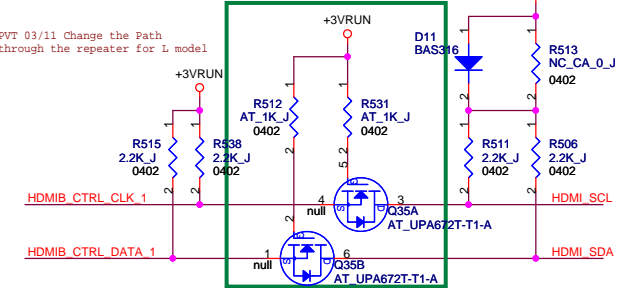
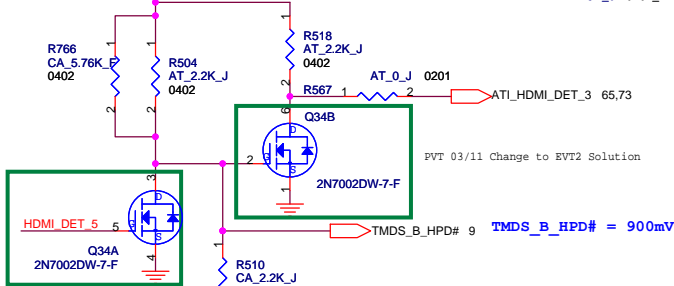
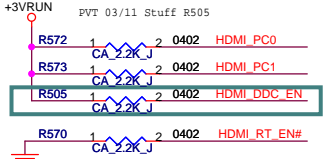
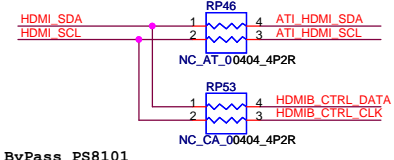
## LVDS CONNECTOR



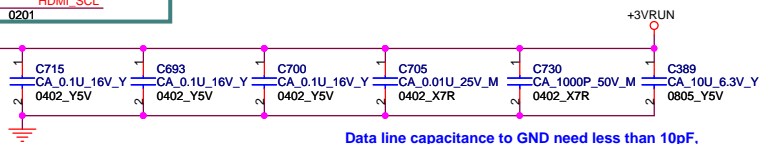
This layout is AMD recommend ,Please Follow it!



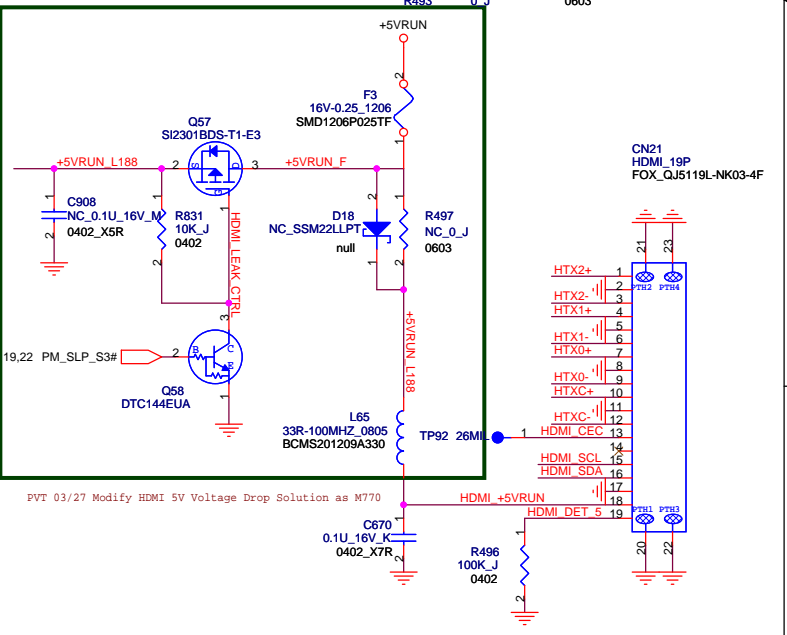
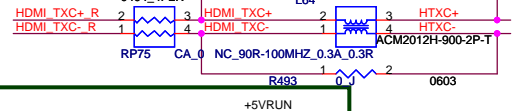
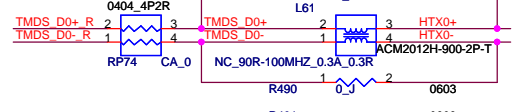
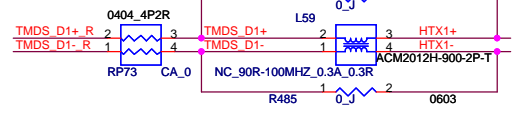
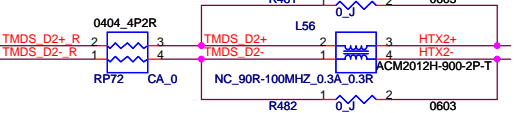
(TMDS inputs equalization control)  
PC1,PC0 Configuration  
00: 8 dB,  
01: 4 dB,  
10: 12 dB,  
11: 0 dB



PVT 03/11 Change the Path through the repeater for L model

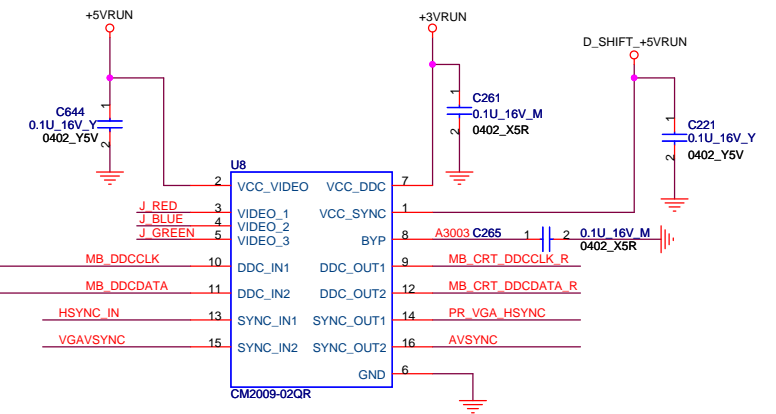
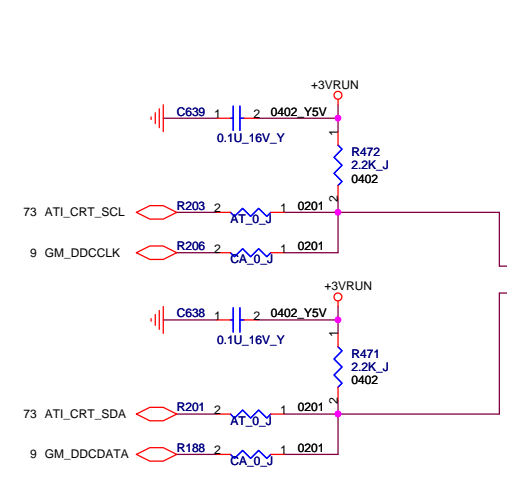
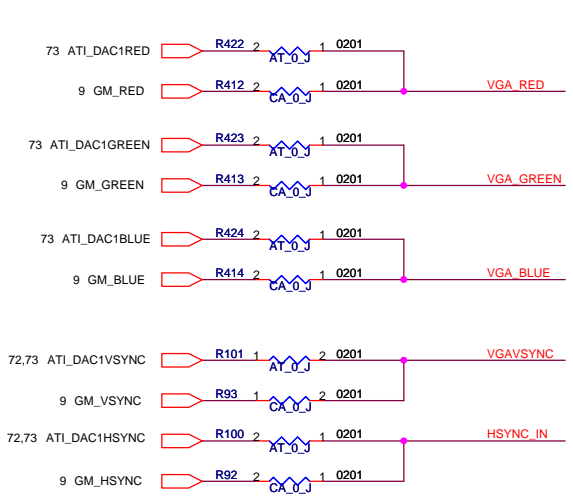


Data line capacitance to GND need less than 10pF, so those parts need close to HDMI connector

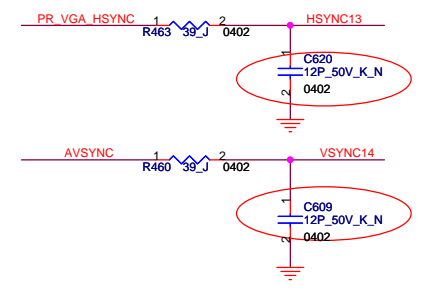
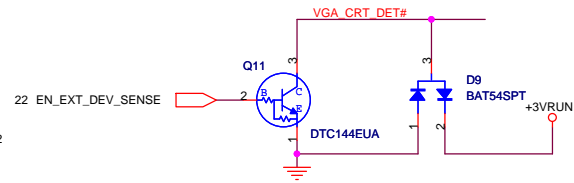
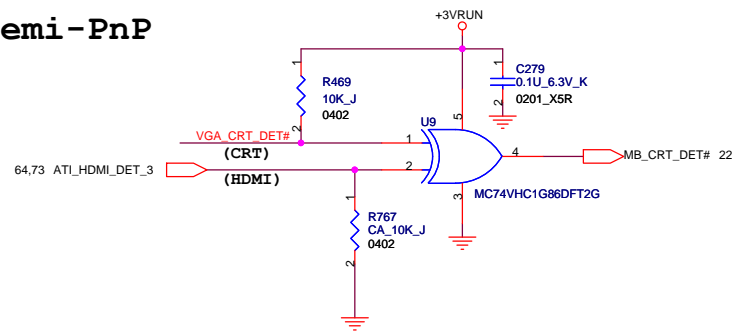


PVT 03/27 Modify HDMI 5V Voltage Drop Solution as M770

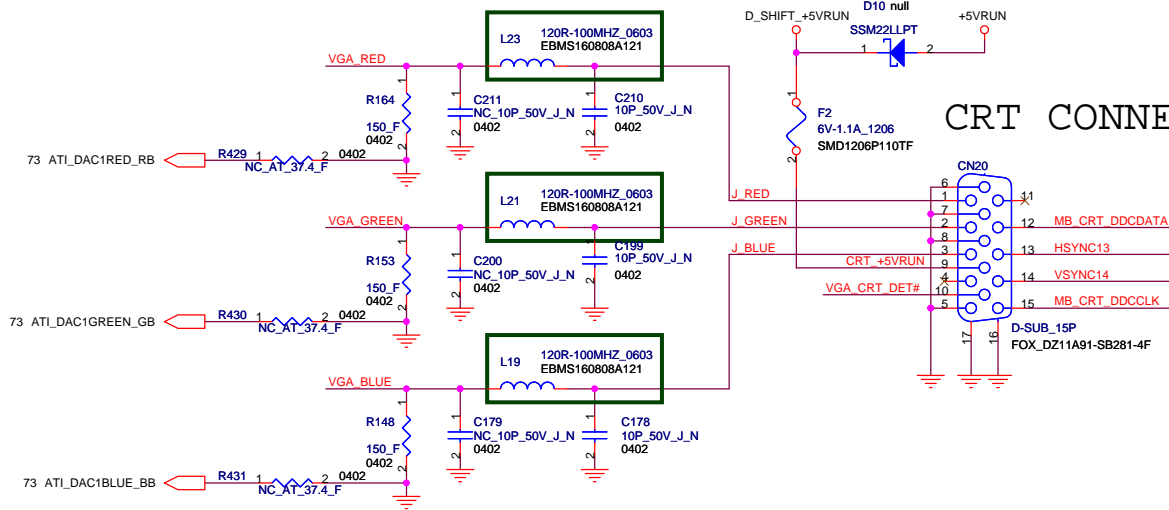




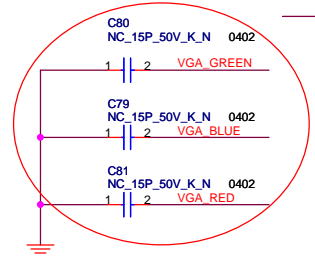
**Semi-PnP**



PVT 3/21 EMI Request

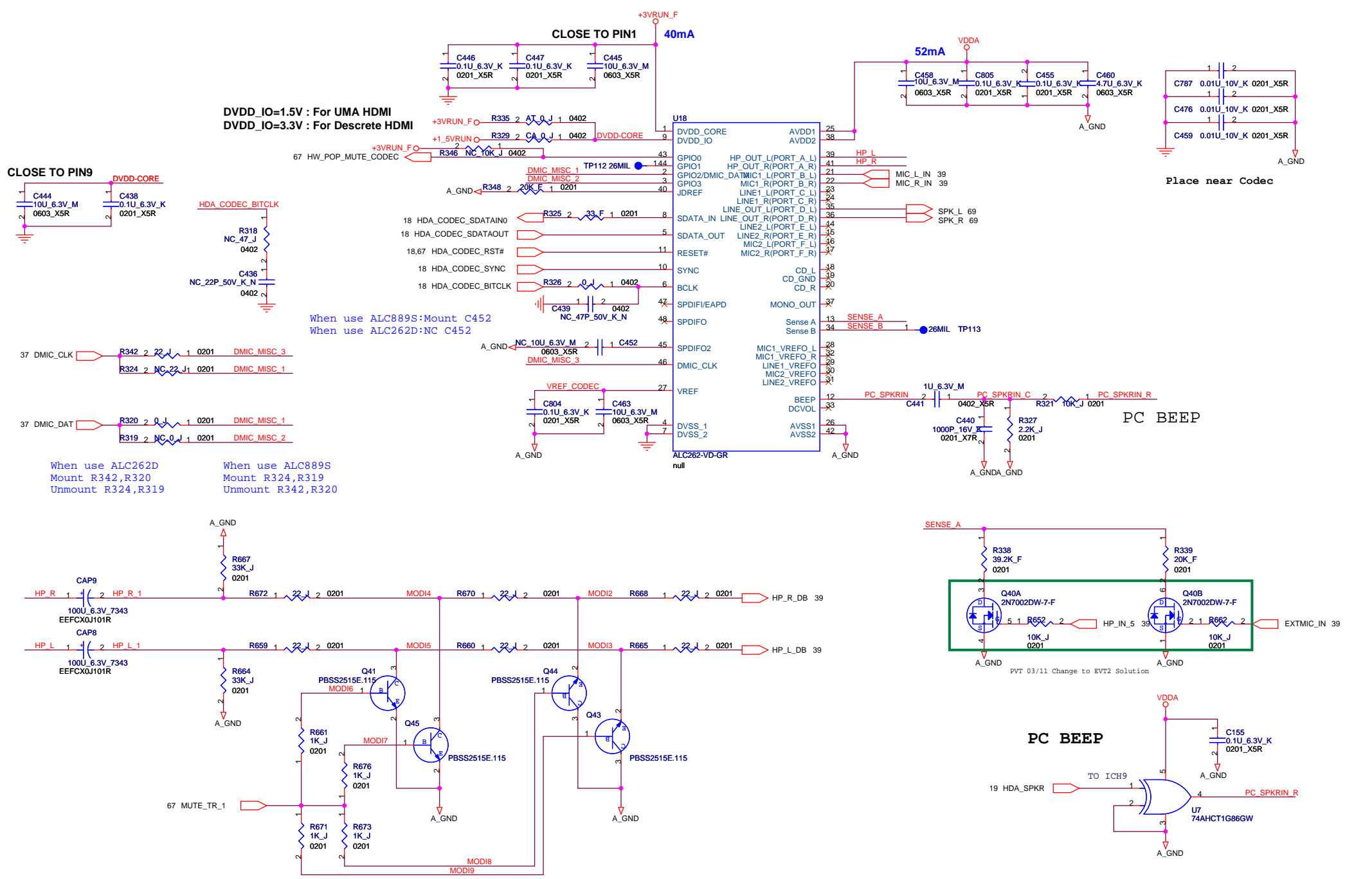


**CRT CONNECTOR**



For EMI

<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title	<b>CRT</b>	
Size	Document Number	Rev
A3	M760	1.0
Date:	Thursday, March 27, 2008	Sheet 65 of 89



DVDD\_IO=1.5V : For UMA HDMI  
 DVDD\_IO=3.3V : For Descrete HDMI

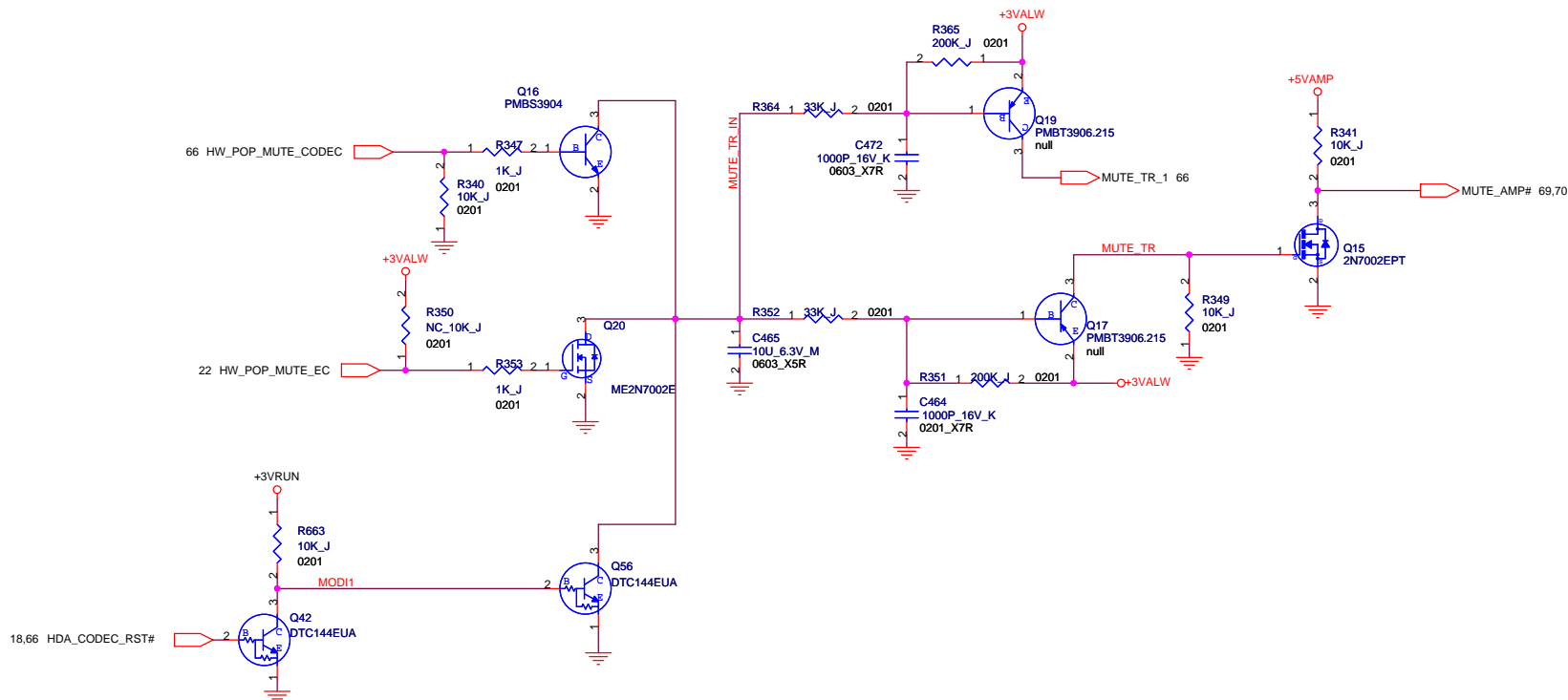
52mA

40mA

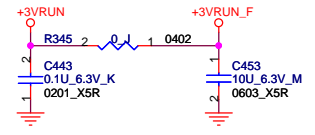
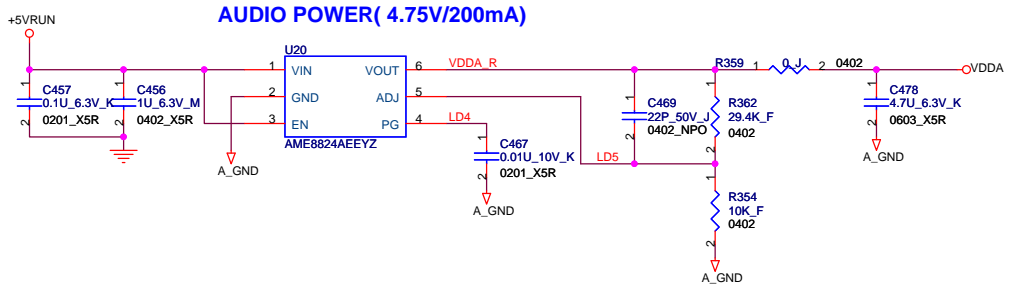
Place near Codec

PC BEEP

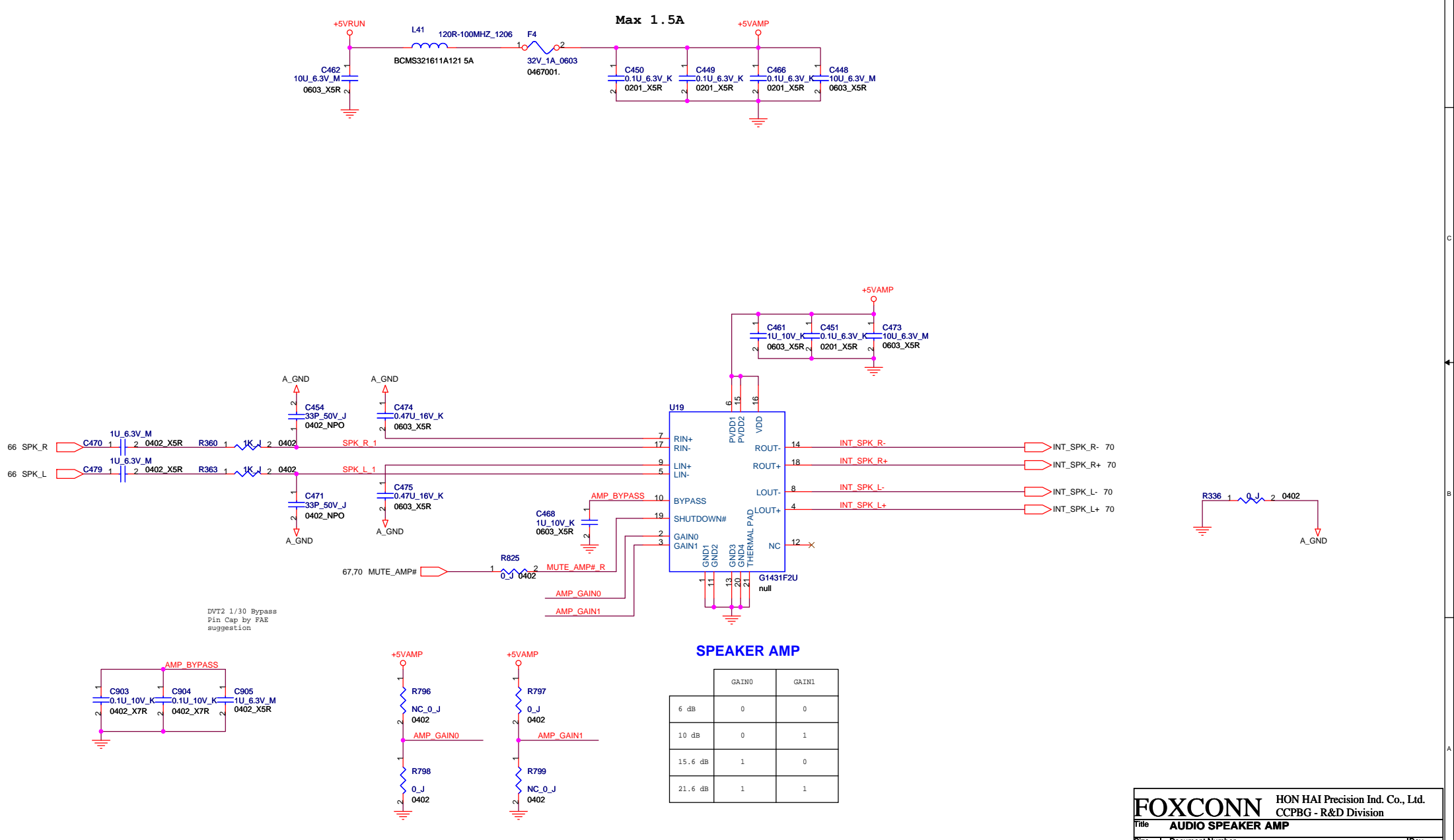
PC BEEP



Q42 for 1.5V power level

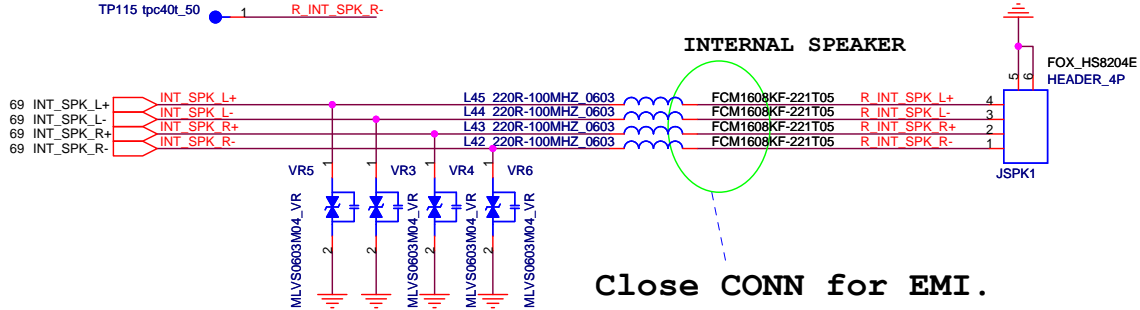


<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.
Title		CCPBG - R&D Division
<b>AUDIO POWER</b>		
Size	Document Number	Rev
A3	M760	1.0
Date:	Thursday, March 27, 2008	Sheet 68 of 89

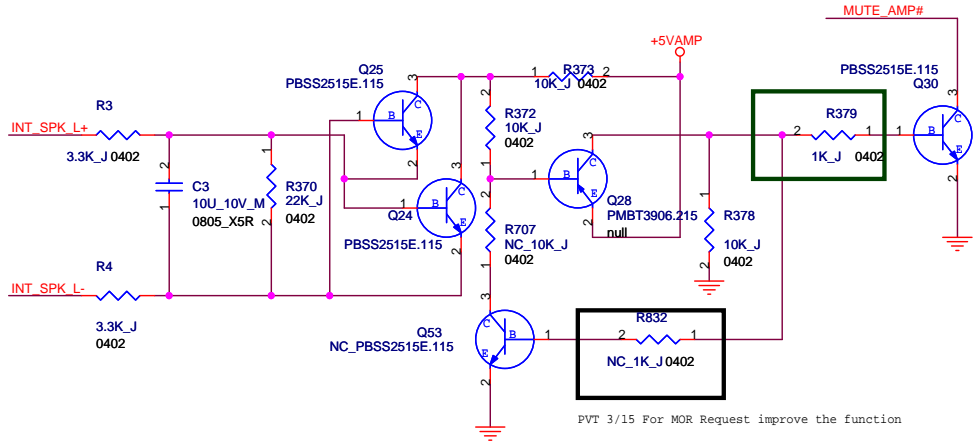


	GAIN0	GAIN1
6 db	0	0
10 db	0	1
15.6 db	1	0
21.6 db	1	1

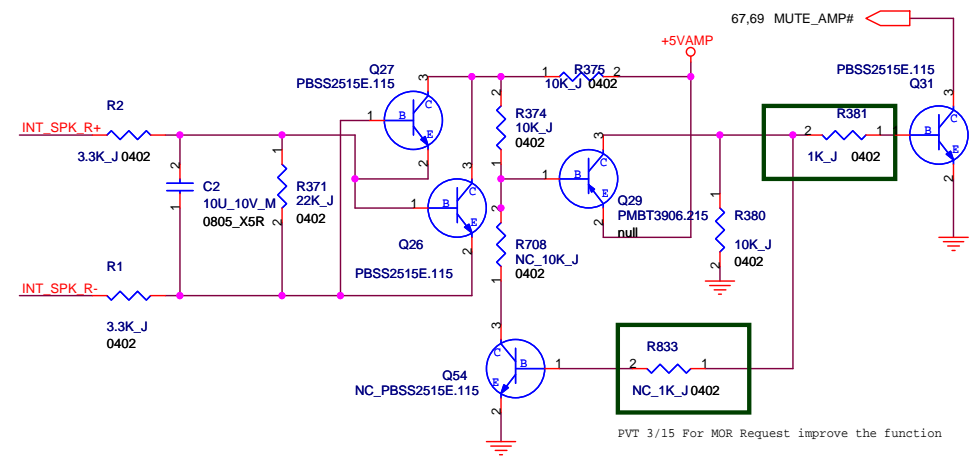
- TP114 tpc40L\_50 ● 1 R\_INT\_SPK\_L+
- TP117 tpc40L\_50 ● 1 R\_INT\_SPK\_L-
- TP116 tpc40L\_50 ● 1 R\_INT\_SPK\_R+
- TP115 tpc40L\_50 ● 1 R\_INT\_SPK\_R-



Close CONN for EMI.



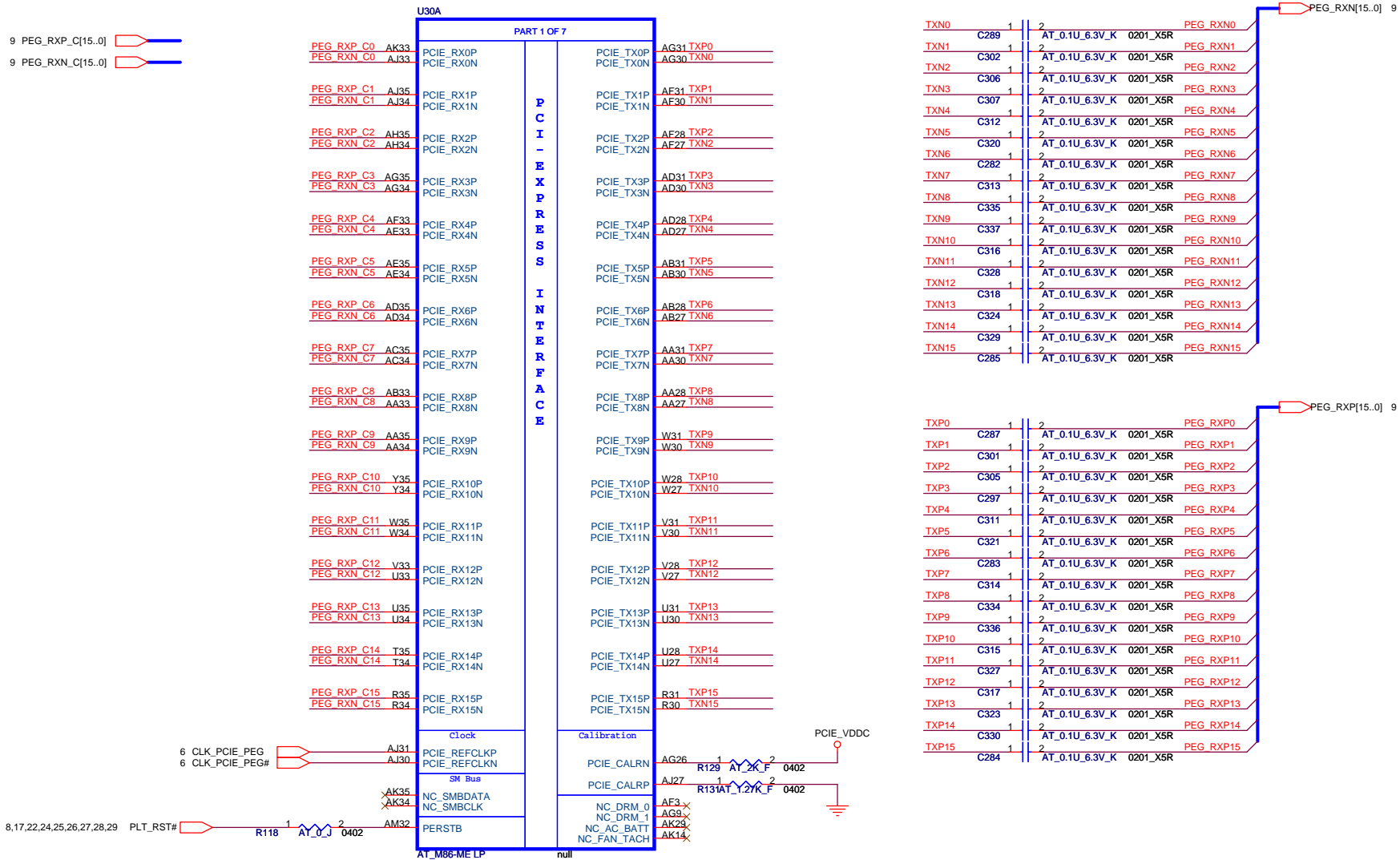
PVT 3/15 For MOR Request improve the function



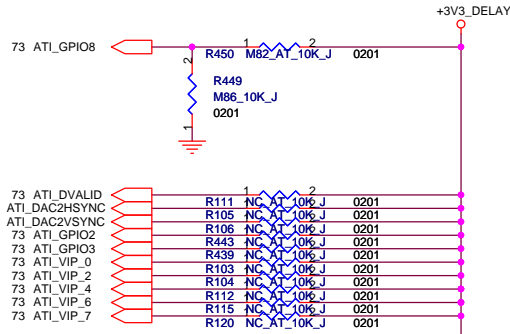
PVT 3/15 For MOR Request improve the function

For Mor request, add the speaker cable short protection circuit

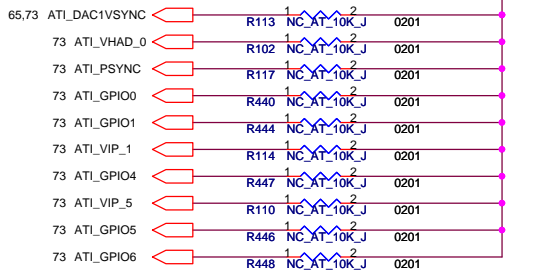
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title		AUDIO SPEAKER CONNECTOR	
Size	Document Number	Rev	
B	M760	1.0	
Date:	Thursday, March 27, 2008	Sheet	70 of 89



R450 for M82 only  
 1 ENABLE HD AUDIO  
 0 DISABLE HD AUDIO



Internal use only. Other logic must not affect this signal during RESET.



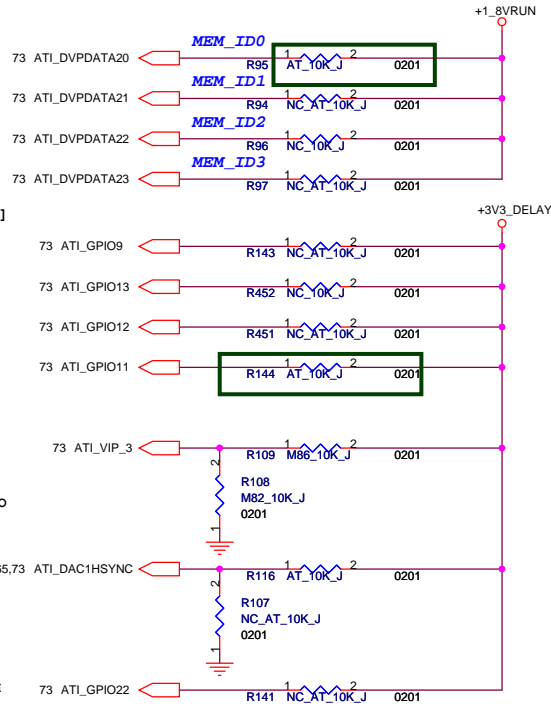
Strap for GDDR3-136ball  
 ATIDVDPDATA[23 : 20]

- 0001 16Mx32 Qimonda
- 0010 16Mx32 Hynix
- 0011 16Mx32 Samsung
- 0101 32Mx32 Qimonda
- 0110 32Mx32 Hynix
- 0111 32Mx32 Samsung

PVT03/14 Set strap pin for PVT HHL SKU M86-LP 256MB 32Mx32 Qimonda.

If no ROM attached, GPIO[9:13:12:11]

- CONFIG{3:0} controls the memory aperture size.
- 128MB X000
  - 256MB X001
  - 64MB X010
  - 32MB X011
  - 512MB X100
  - 1GB X101
  - 2GB X110
  - 4GB X111



R109 for M86 only  
 1 ENABLE HD AUDIO  
 0 DISABLE HD AUDIO

1 HDMI ENABLE  
 0 HDMI DISABLE

1 ENABLE EXTERNAL BIOS ROM  
 0 Disable EXTERNAL BIOS ROM

### CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
 0= DO NOT INSTALL RESISTOR  
 1= INSTALL 10K RESISTOR  
 X = DESIGN DEPENDANT  
 NA = NOT APPLICABLE

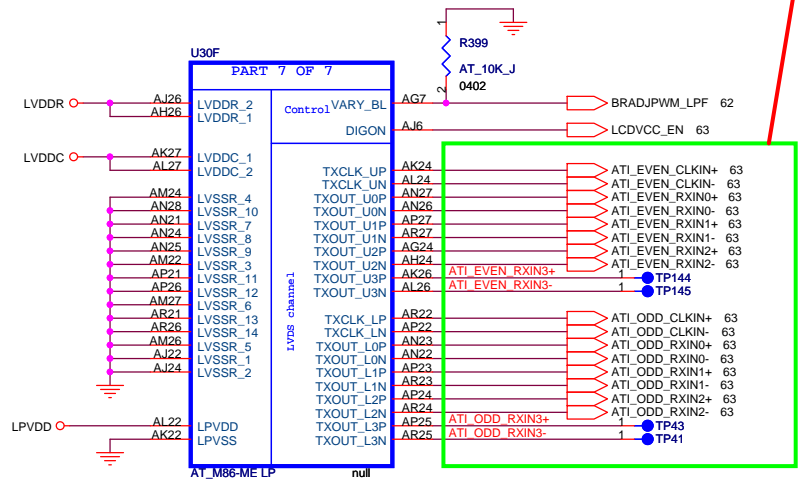
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO (SEE NOTE 1)	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING (0: 50% Tx output swing, 1: Full Tx output swing)	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS NOT MUXED OUT	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	1
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	0
BIF_VGA_DIS	PSYNC	VGA ENABLED	0
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE, MAKE AND SIZE INFO	X X X X
BIF_GEN2_EN_A	GPIO_5	1 = Advertises the PCI-E device as 5.0 GT/s capable at power-on. 0 = Advertises the PCI-E device as 2.5 GT/s capable at power-on	0
DEBUG_I2C_ENABLE	GPIO_6	Disable DEBUG_I2C	0



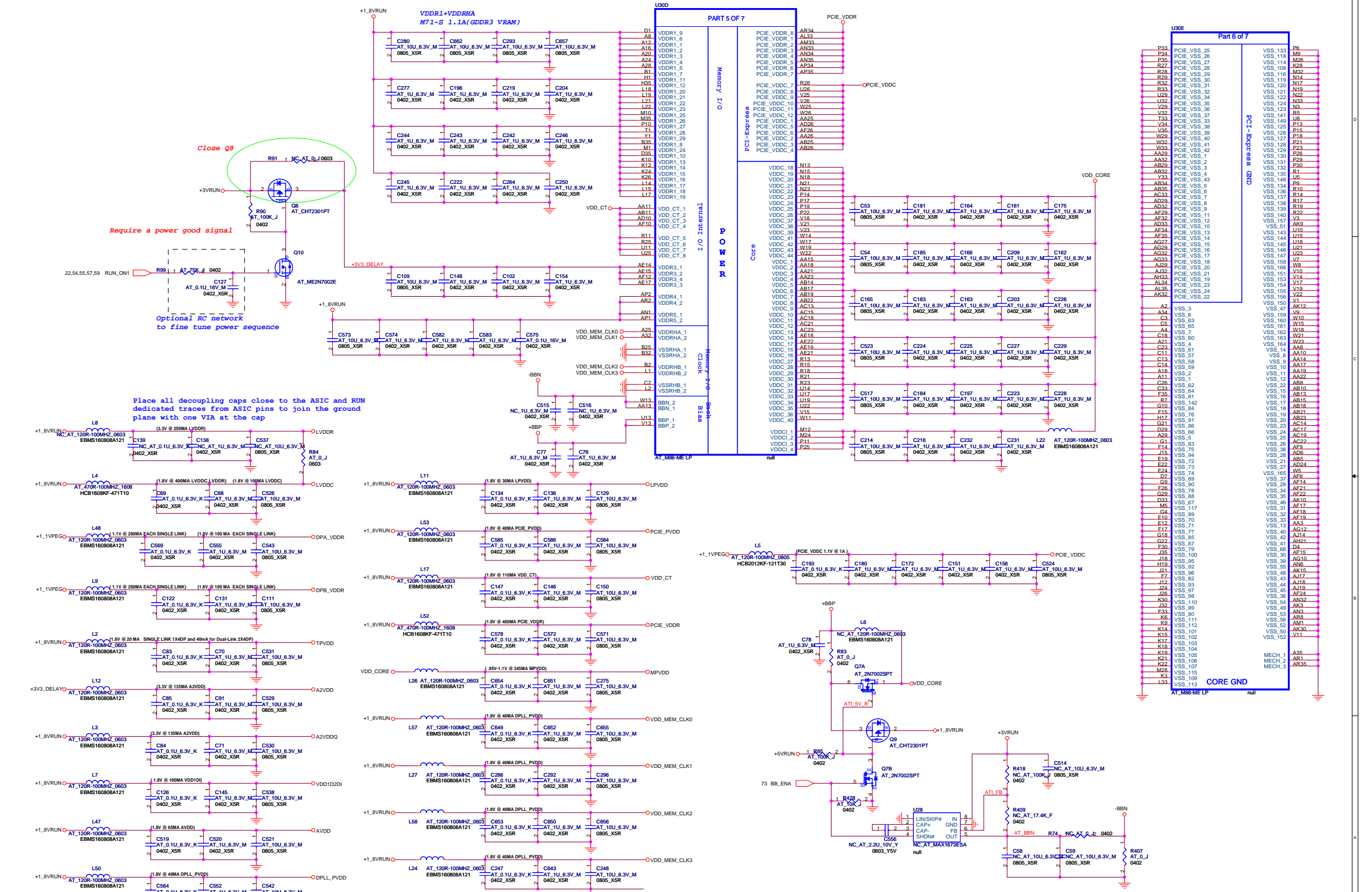


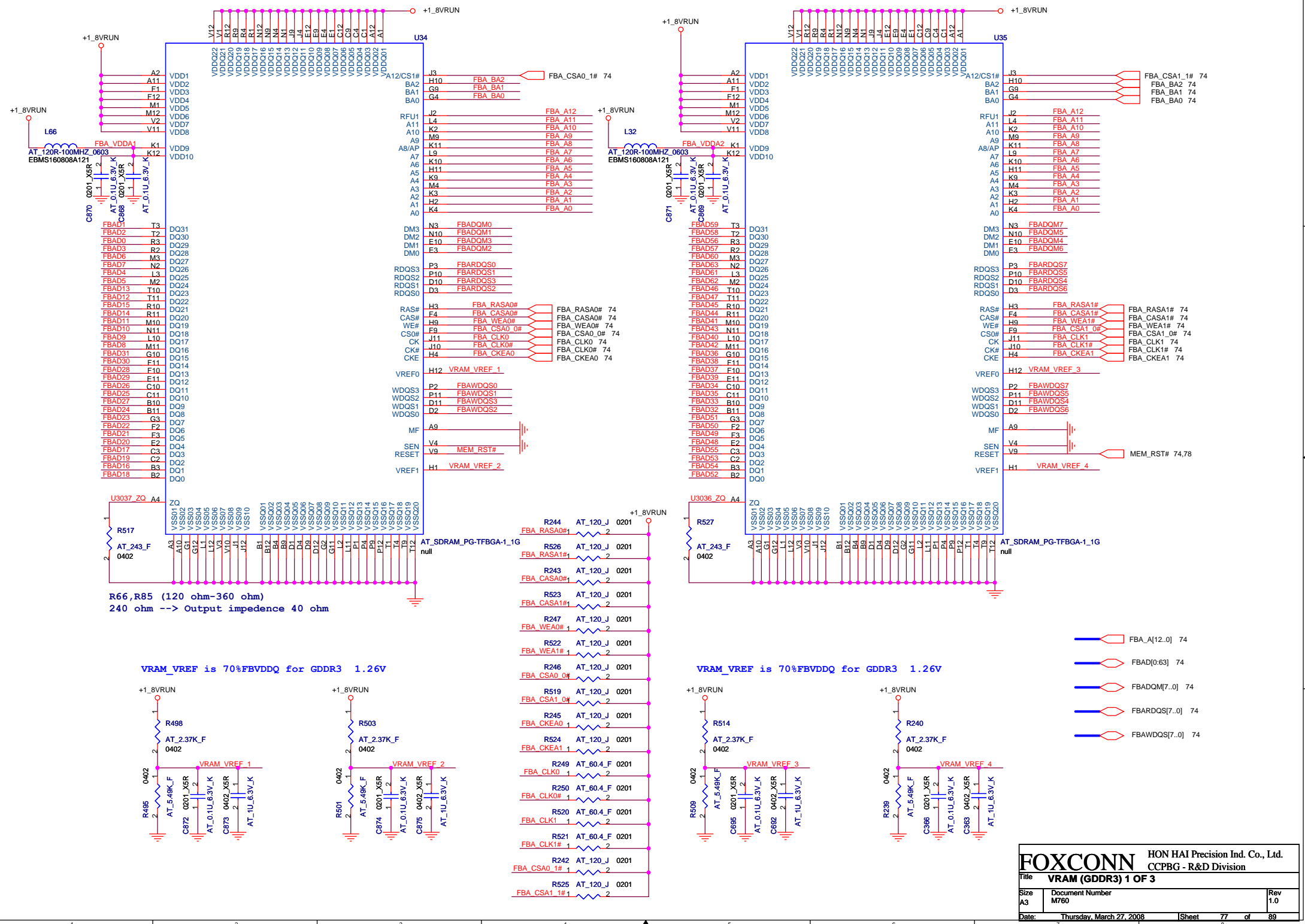


This layout is AMD recommend ,Please Follow it!



TXCLK =U=EVEN  
 TXOUT=U=EVEN  
 TXCLK =L=ODD  
 TXOUT=L=ODD



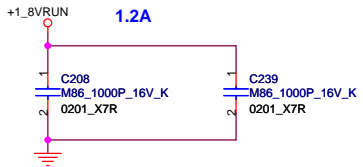
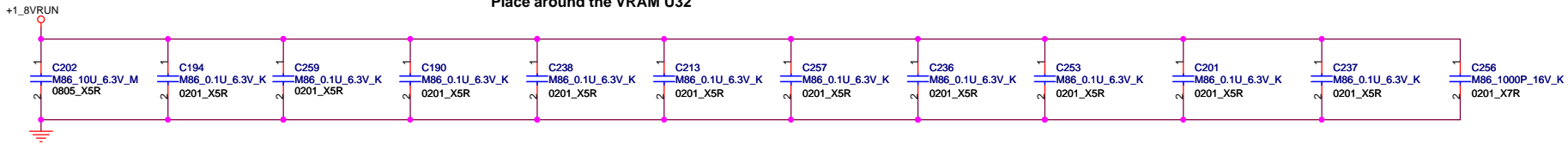


VRAM\_VREF is 70%FBVDDQ for GDDR3 1.26V

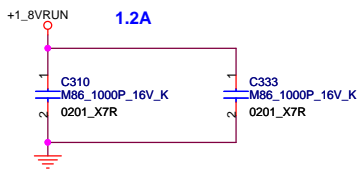
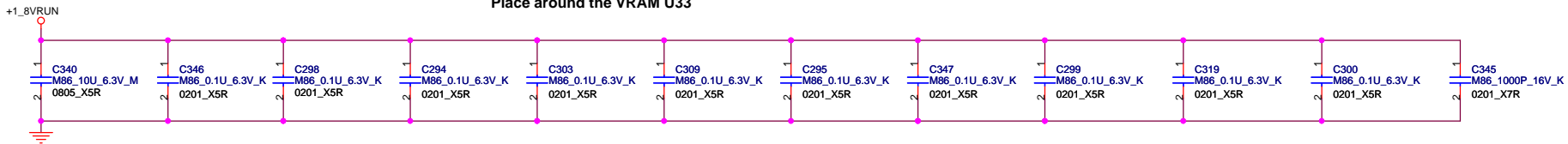
VRAM\_VREF is 70%FBVDDQ for GDDR3 1.26V



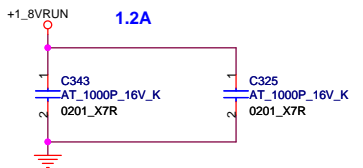
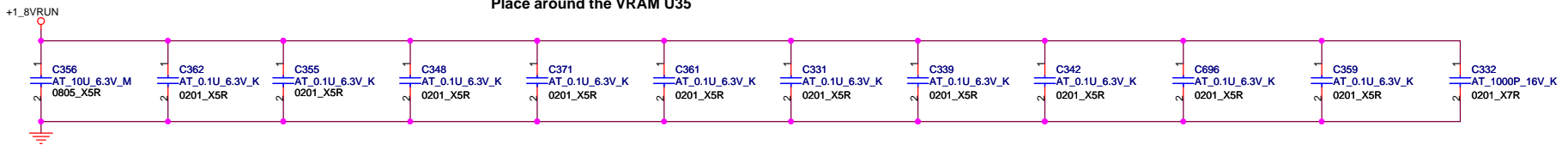
Place around the VRAM U32



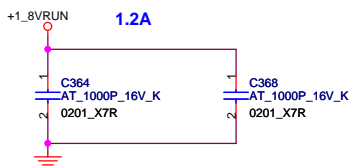
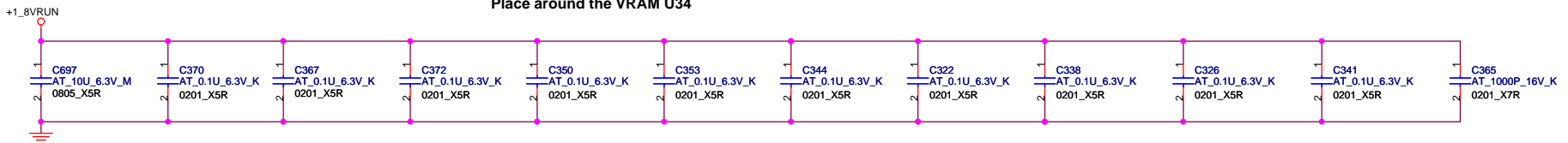
Place around the VRAM U33

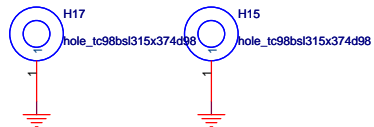
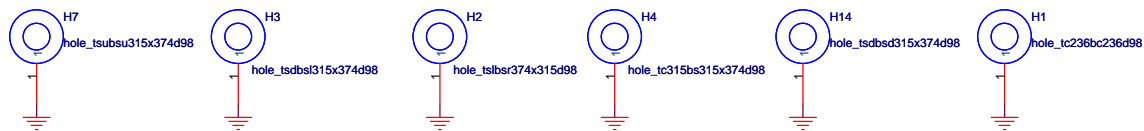
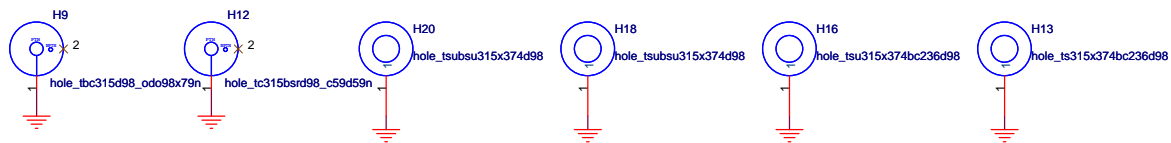
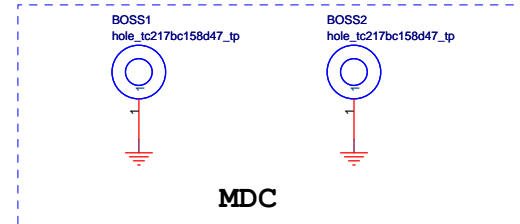
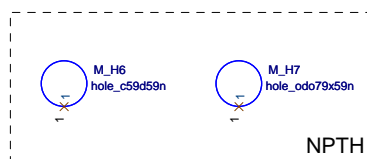
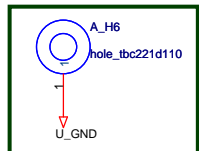
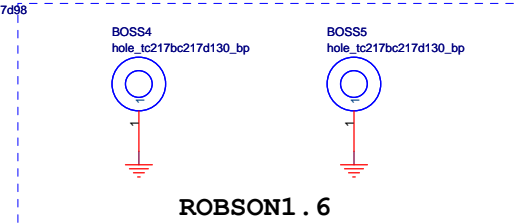
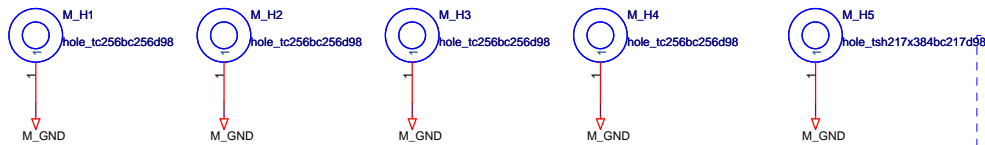
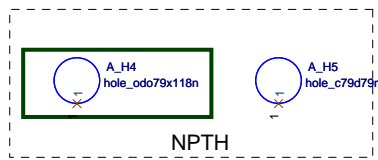
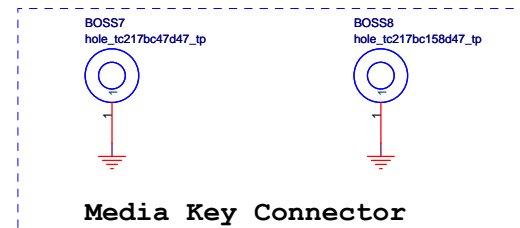
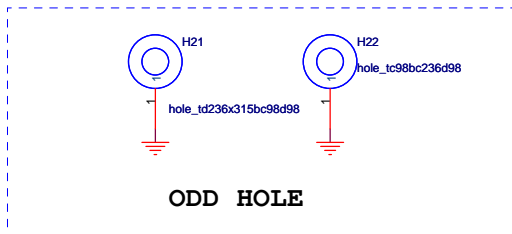
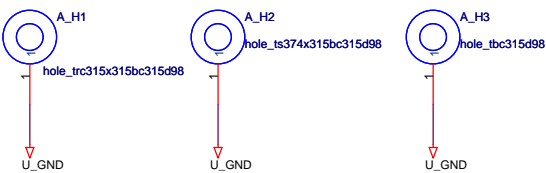
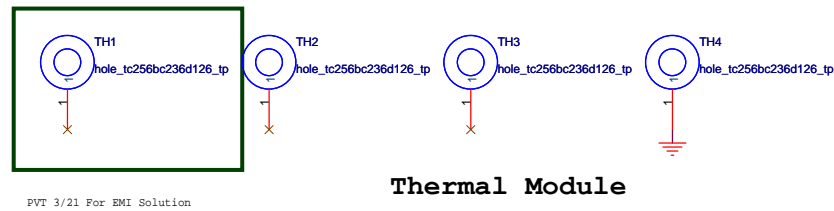
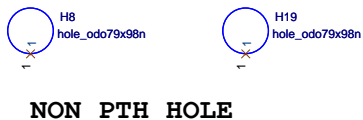
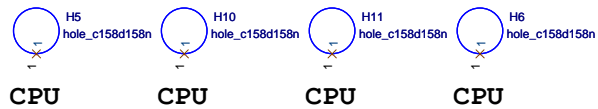


Place around the VRAM U35



Place around the VRAM U34





<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>HOLE</b>		CCPBG - R&D Division	
Size A3	Document Number M760	Rev 1.0	
Date: Thursday, March 27, 2008	Sheet 80	of 89	



2007/09/03  
P.9:Reverse PCIE I/F  
P.39:Change CN17 P/N  
P.44:Add Power Button Connector  
P.63:Change LVDS Connector P/N

2007/09/05  
P.25:Change U14 P/N from Rohm to TI  
P.25:Change R333,R335,R338 from 0603 to 0402  
P.34:Add R762,R763,C840 for GBRST#

2007/09/07  
P35,36 modify netname for MS/SD card  
P14,15,16 swap DDR net for layout

2007/09/11  
P.4:Delete R11,R14 and change to TP  
P.8:Delete R74,R75 and change VGFX\_VR\_EN to TP  
P.8:Delete R76 for double pull high  
P.18:Delete R199,R201,Q3A/B  
P.19:Change R217 from GPIO12 to GPIO13 (GPIO12 default=GPO,GPIO13 default=GPI)  
P.20:Delete C290,C291,C292 and Add TP  
P.20:Delete L16,C294,C295 and connect to +1.05V directly  
P.22:Change RP25 from S3 power to S0 power  
P.33:Delete G-Sensor function  
P.35:Change R413-417,R419-423 from 0R to 33R  
P.49:Change R442 from 1K to 68R  
P.62:Delete R461 for simplify circuit  
P.62:Change U29C-9 from VCC to INV\_EN\_EC  
P.63:Delete R470,R471 for simplify circuit  
P.63:Add C853,C854

2007/09/13  
P.5:Add C855-C866 for reserved

2007/09/14  
P.8:Delete R70 (Unuse) and add TP  
P.8:Change R69,R71 from +1.05V to GND  
P.9:Add R771-773 for H/L function  
P.11:Delete R127  
P.13:Delete all TP in this page  
P.17:Delete R144-R146,R148-R160 and Add RP62-RP65  
P.17:Delete R175,R.176,R178-R182,U5,C242,C244 and change to TP  
P.17:Delete SW1,Q1,Q2,R162,R163,R166,R167,R170  
P.18:Add R774  
P.19:Add R775,R776 for panel ID2,3  
P.19:Delete R254,R258,C254 and add TP  
P.41:Add R783,R784 for H/L sku option  
P.42:Add Q41-Q43,R780-R782,CAPS\_LED,NUM\_LED,CTRL\_LED  
P.50:Add PR248 for EC Charging

2007/09/15  
P.6:Add R793 for enable SRC3  
P.26:Delete R346 (double pull high)  
P.26:Delete R779,C337,C338 (Intel WLAN spec)  
P.40:Delete R431 (double pull high)  
P.66:Change U37 to ALC262D (MOR drop ALC889S)

2007/09/17  
P.19:Delete TP91,TP92 and change to CH+,CH-  
P.19:Add GPIO18 net:TV\_EEC  
P.22:Delete R309,R310 and change to RUN\_ON\_TV1,2  
P.43:Delete CIR parts and move to TV DB

2007/09/19  
P.20:Add R275,R810,R811,U53 for 1.5VALW power needed  
P.20:Change VCC\_HDA from 3V to 1.5V  
P.26:Delete SW3 (Move to Media key DB)  
P.44:Delete CN26 (Move to Media key DB)  
P.50:Add PR254-256,261,262 for power wave adjust  
P.54:Add PR253,PR259 for power wave adjust  
P.59:Add PR257-258,260 for power wave adjust  
P.64:Move R618 from P.73 to here (Close to connector)  
P.72:Add R816,R817,R818 for disable use  
P.74:Change R650 from 243R to 240R  
P.77:Add R812,R813 for 32Mx32Bit RAM config  
P.78:Add R814,R815 for 32Mx32Bit RAM config

2007/09/20  
Page all:Modify MON\_,ATI\_ to CA\_,AT\_  
P.11:Delete R116

<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
Title <b>Power Design Diagram</b>		
Size A3	Document Number M760	Rev 1.0
Date:	Thursday, March 27, 2008	Sheet 81 of 89

2007/10/23  
P.32: Add SATA GDD power saving feature circuit.  
P.18: Delete SATA GDD circuit at SB side.  
P.33: Move the WL & ST switch and Status LED signal to MB side.  
P.44: Move the Status LED to MB side.  
P.26: Move the WL & ST switch to MB side.  
P.32: Change GDD from SATA to SATA.

2007/10/24  
P.44: Change Status LED type.  
P.34: Change the MS/SD LED control signal.  
P.36: Change MS/SD LED control signal share one LED.  
P.35: Change the MS/SD LED control signal.  
P.72: Change the strap pin stuff and IC for default M86.  
P.04: Use SBCH for PCIe SATA bridge clock.  
P.70: Change Internal speaker connector form HS6204E to HS8204E.

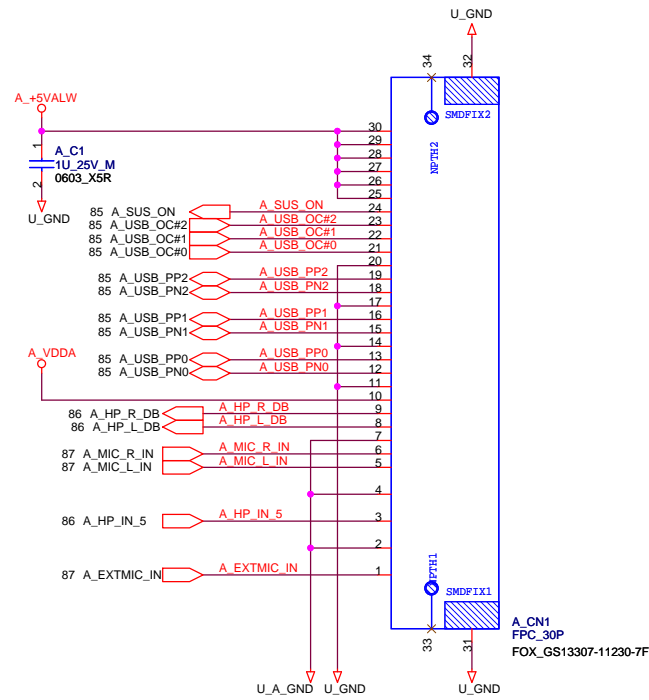
2007/10/29  
P.57: Change \*L\_SVRUN power control signal to RUN\_ON1.  
P.51: Change discharge signal to RUN\_ON1.  
P.73/10/29 Change pull high power to \*L\_SVRUN for VGA Vref correction.  
P.87: Reverse the Function switch connector for EVT1 mistake.

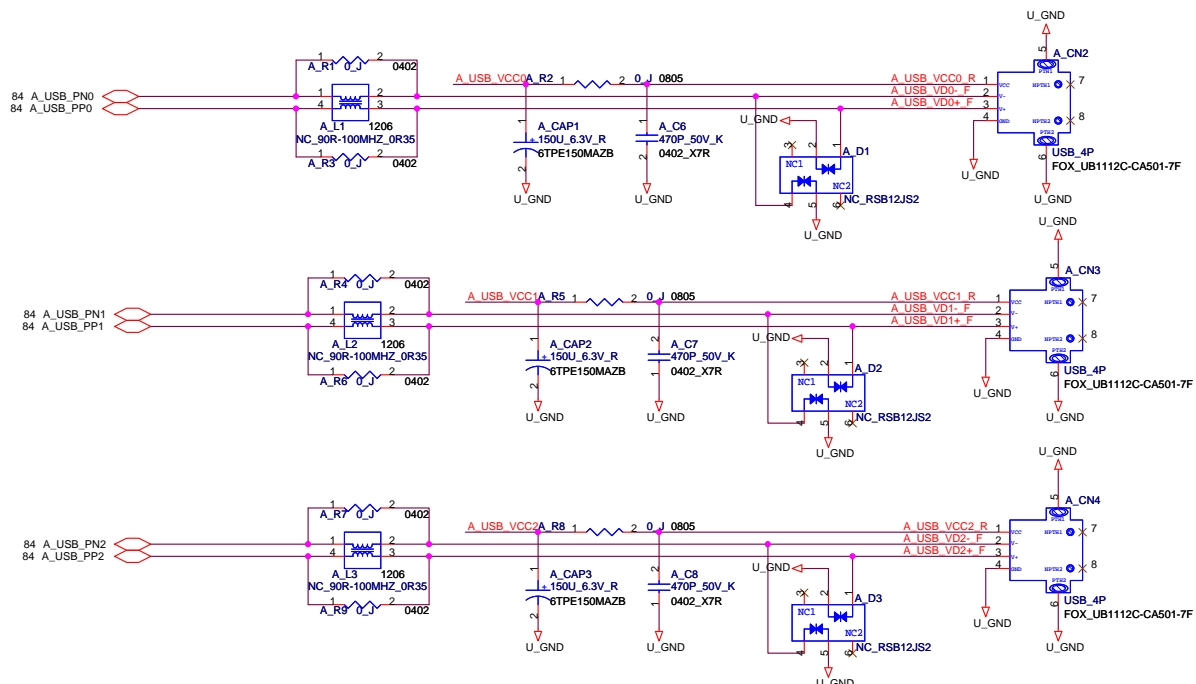
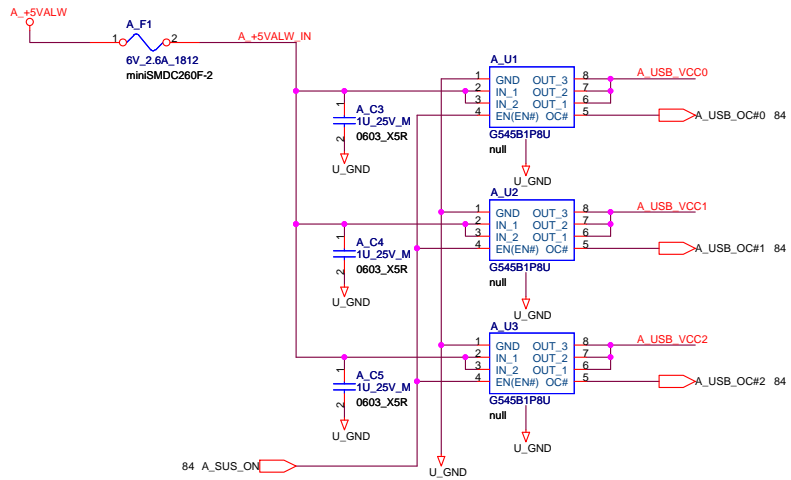
2007/10/30  
P.45: Add 22 ohm resistor for countermeasure of possible power line short.  
P.45: Change P14 for the Power team test result of EVT1.  
P.20: Change CLK0 to 0.87uF for customer schematic review.  
P.50: Change Battery charging set table.  
P.53: Change PR200 to 0 ohm for the PWM frequency change to 400KHz/500KHz.  
P.59: Reserve PR209 for VGA\_EN/P5V pull low.

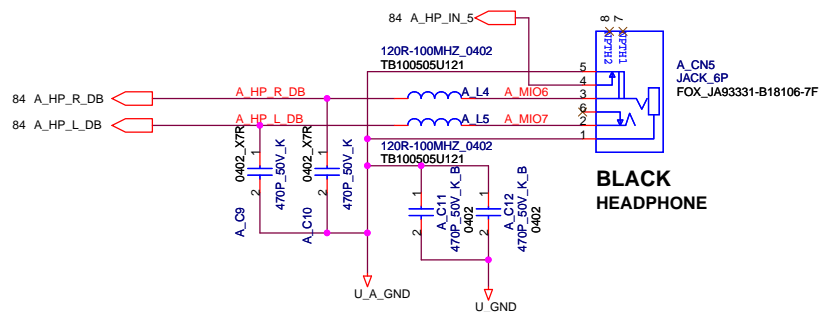
2007/10/31  
P.25: Change Express card CN10 and CN11 connector to correct part.  
P.56: Change WL connector CN12 and CN13 to correct part.

2007/11  
P.64: Change the net connection of SP46 and SP53 for EVT1 net mistake.  
P.75: Change the LVDS change net connection for EVT1 net mistake.  
P.23: Co-Lay B775 with U3, Default is NC.  
P.22: 35.17: Adjust for clock accuracy.  
P.17: Stuff for HDDP function.  
P.50: Adjust charges voltage to 12.48V  
P.64: Change Q35 value to CA.  
P.67: Change Q30 to 2N7002E For solve the EVT1 hang '11' issue.  
P.09: Reserve 150 ohm termination resistor at P/S signal, modify layout to shorten the trace stub.  
P.27: Update Robson connector type.  
P.22: Connect UA pin 80 for GDD power saving feature control.  
P.59: Change PC158 to 100uF for power team request.  
P.18: Intel recommend to add RC delay for SDR10678 timing.  
P.87: Move 150 ohm resistor to power switch cable board.  
P.44: Modify schematic for GDD/HDD share the LED.

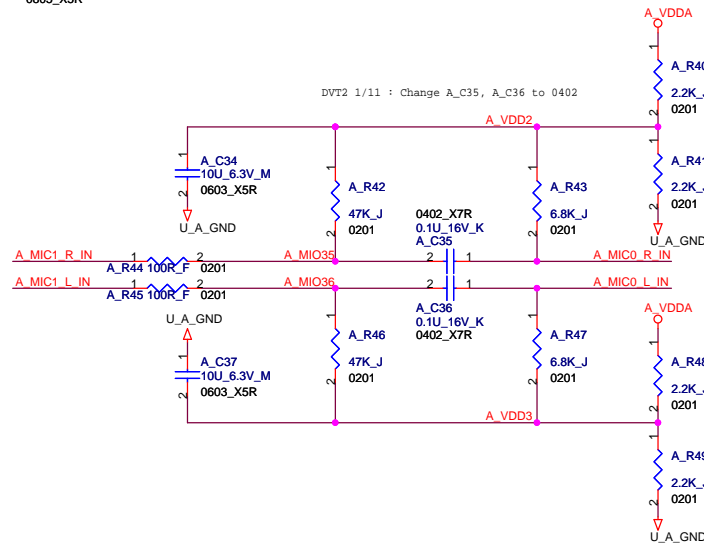
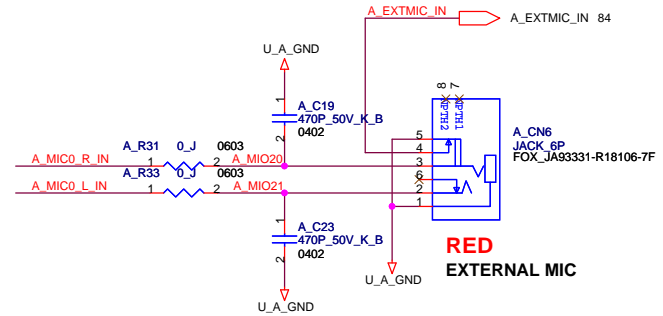
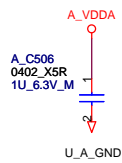
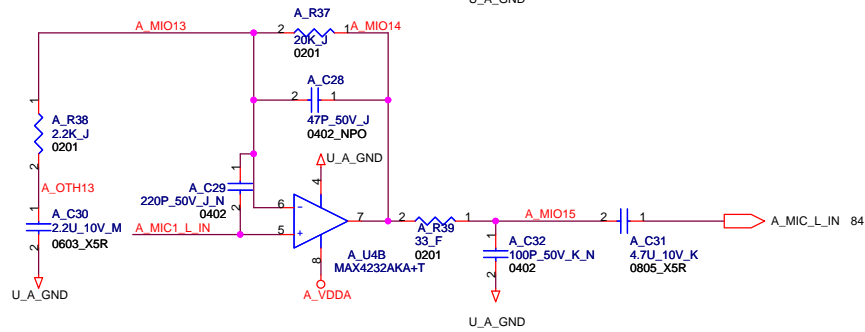
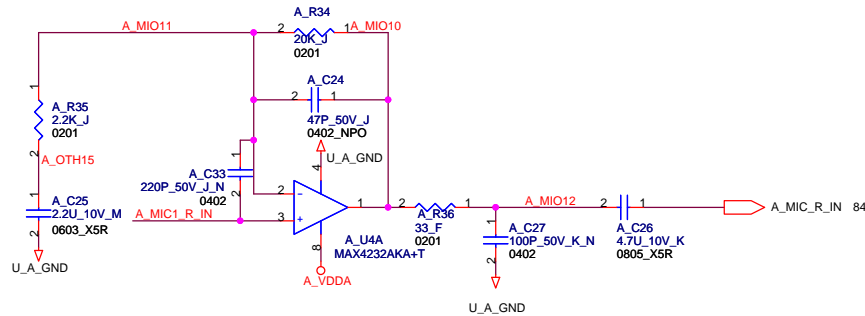
1/21-1/31  
 1.006 - Clk gen - B version ,RL28648RLC  
 2.006 - Clk gen - CLK\_PCIE\_MCAM29/CLK\_PCIE\_MLAN2 pin swap  
 3.003 - CPU - R26 change to 649ohm  
 4.026 - Expresscard - Change path to EXPRESS\_CLK\_ENH  
 5.064 - HMC1 - Change D11 to RA3116 for low equal cap value  
 6.007 - Ext MIC Jack - Change A\_235, A\_236 to 0402  
 7.020 - IC93(PONER) - Change 415/102/258  
 8.011 - Cautiga(power,vcc) - Connect to Vcc3\_3 no filter CA\_00hm (R822) MC\_C621 and C622  
 9.019 - IC93(GPIO) - Add R833 - If Q3 -- 85 MUX is not supported, GPIO9/WGL\_EN can be connected to ground  
 10.058 - OVP Protection - Power Limit Protect Setting 90M for AT - Stuff PR24 / PR22 ,75W for CA - Stuff PR218 / PR219  
 11.098 - OVP Protection - Power Limit Protect Setting 80m change to +VDDM\_LDO  
 12.019 - IC93-M(GPIO) - CRT ID - 111 - 15.4" LCD change to 000  
 13.050 - DCIM/ Charger - Total Power Setting PWL2 AT\_2JK for ROM,PR220 CA\_44.2K for 75W  
 14.026/P40 - SF - C622 Pin# as BT\_LDO MIC\_PCIE\_LAN - 08 pin# change to SF\_LDO and add pull low R824  
 15.066 - HP Jack - Revised the net name to HP\_R\_1/HP\_L\_1  
 16.069 - Audio Amp - Add R825 for reserved  
 17.028 - TV Tuner - Reserved the CA217 for TV Power  
 18.028 - Mini PCIE M2M - Reserved the CA216 for M2M Power  
 19.022 - ECMPCT75 - Add the diode D21/D22 to prevent the Leakage  
 20.069 - Audio Amp - U19 change to G1431F20,78500-20(PD),2W Stereo Audio Amplifier  
 21.064 - Vcc power +1\_OV0 R31 Delete  
 22.017 - IC93M - U14 BOM Changed from W25X80V8S10 to W25X80AV8S10  
 23.023 - IC93M - U13 BOM Changed from W25X16V8S10 to W25X16AV8S10  
 24.080 - Hole - Confirm ME, Delete H23  
 25.028 - Expresscard - Revised CW10 Symbol footprint  
 26.048 - Thermal Sensor - Reserved the HMC1402 workaround - OVT\_EC# for Output Glitch on THERM# Pin During Power Up. (Vendor Suggestion)  
 27.042 - Keyboard Connector- LED Display Brightness change R367,R368,R369 - 150ohm to 75ohm  
 28.044 - Status LED - Change vendor of LED2 and LED3  
 29.070 - Audio SPK Connector - Revised cable short schematic -Dummy Q83/Q84/R707/R708  
 30.069 - Audio Amp - U19 pin10 change to 2.2uF for C446/C902/C903/C904  
 31.088 - Function SW - M\_C1-M\_C9 change to 100pF  
 32.064 - HMC1 - Add HMC switch path and H/C bridge  
 33.019 - IC93M - Add Panel ID Jumpers R828/R829/R830  
 34.026 - SF - Comment change BT\_ON:Active S0 ,s3  
 35.058 - OVP - p015 change to PR13.2 as NDR request



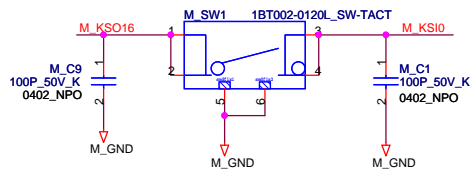




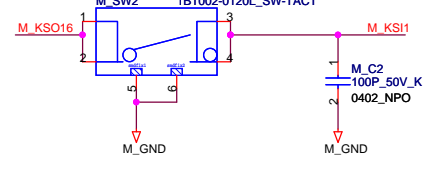
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		CPBG - R&D Division	
Title			
<b>Head Phone Jack</b>			
Size	Document Number		Rev
A3	<b>M760 AUSB DB (CNX-409)</b>		1.0
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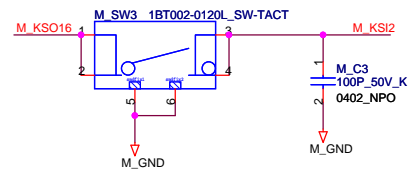
### S1 (Short Cut)



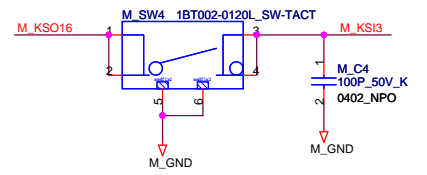
### VOL-



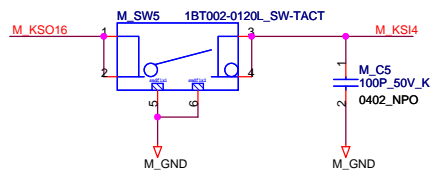
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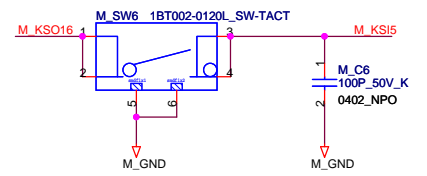
### STOP



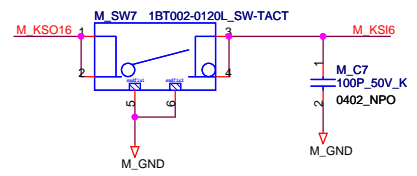
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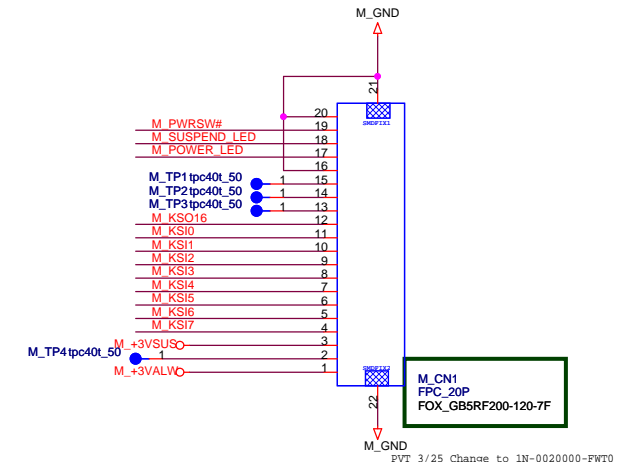
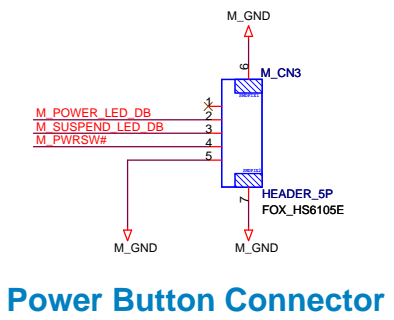
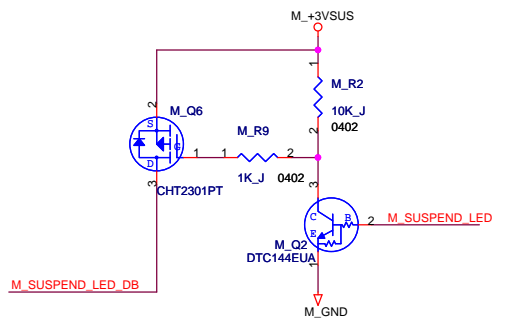
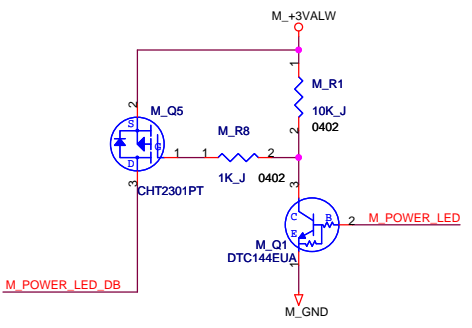
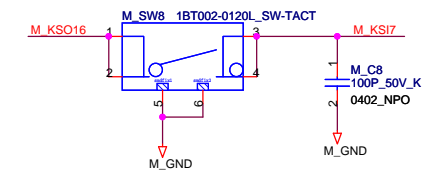
### FR



### FF



### AV MODE



Power Button Connector

Media Key Connector



3/13~3/15

- P52. PU5 change part number to 15-R5G0500-0000
- P64. Stuff R505 for U37 HDMI\_DCC\_EN enable
- P20. C380 and C378 change to 1C-2B20104-M000
- P64. Delete Q35 and R152 ,R531 of L SKU
- P64. Stuff R507 ,R508 R568 and R569
- P59. Add PR221 for M82 PowerPlay Control
- P59. Change PR179 from 16.9K to 19.6Kohm
- P66. P64. Q34 and Q40 change to EVT2 solution
- P50. PC4 change net to BT+\_L for EMI request
- P50. Add C906 and C907 for EMI request
- P50. Change PR4 to 1R-200015T-FJ00
- P50. Add PR222 and PR223 for Power Team Solution
- P32. Change ODD\_DP# pin to pin23
- P20. For Engery Star Dummy U15 and R315,R314 and Stuff U47 ,C900 and C901
- P72. Change VRAM Strap pin to Q256M 32x32
- P70. Add R832/R833 for MOR request -cable short function
- P64. Add Q57 and Q58 for HDMI 5V Votage Drop Solution and Dummy D18
- P43. Add R834 +5VRUN\_ODD Path 0ohm

Title		
PVT History		
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