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18	VGA(STRAP)	1.1	07'01'29	53	SYS Power(+1 5V/+1 05V)	1.1	07'01'24
19	VGA(GDDR) #	1.1	07'01'29	54	DDR2 Power(+1 8V/+0 9V)	1.1	07'01'24
20	VGA(MULTIUSE)	1.3	07'03'23	55	CPU Vcore---ISL6262A	1.2	07'03'23
21	VGA(LVDS/VDAC )	1.1	07'01'24	56	Others power plane	1.0	07'01'09
22	VRAM(GDDR) # 1/2	1.2	07'03'23	57	OVP protection	1.0	07'01'09
23	VRAM(GDDR) # 2/2	1.2	07'03'23	58	VGA POWER(+1 1V/ +1 2V)	1.2	07'03'23
24	VGA(POWER) 1/3	1.1	07'01'29	59	GMCH power	1.0	07'01'09
25	VGA(POWER) 2/3	1.1	07'01'29	60	HOLE	1.1	07'01'24
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29	TVIN and OUT/Semi-PnP#	1.1	07'01'24	64	LED/Touch/Lid	1.2	07'03'14
30	CRT	1.2	07'03'23	65	History ( 1 )	1.0	07'01'09
31	LVDS	1.1	07'03'23	66	History ( 2 )	1.0	07'01'09
32	ICH8-M( PCI/USB ) 1/5	1.1	07'01'24	67	History ( 3 )	1.0	07'01'09
33	ICH8-M( LPC,IDE,SATA ) 2/5	1.1	07'01'24	68	History ( 4 )	1.0	07'01'09
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				71	History ( 7 )	1.2	07'01'29
				72	History ( 8 )	1.3	07'03'23
				73			
				74			
				75			

P. Leader	Check by	Design by

**Project Code & Schematics Subject:** MS90 Main Board

**PCB P/N:** 1P-0073100-8012(FUBAI)  
 1P-0073500-8012(HANNSTAR)  
 1P-0073200-8012(NAN YA)

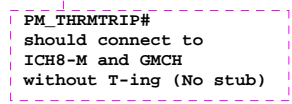
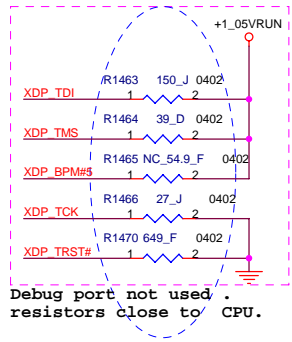
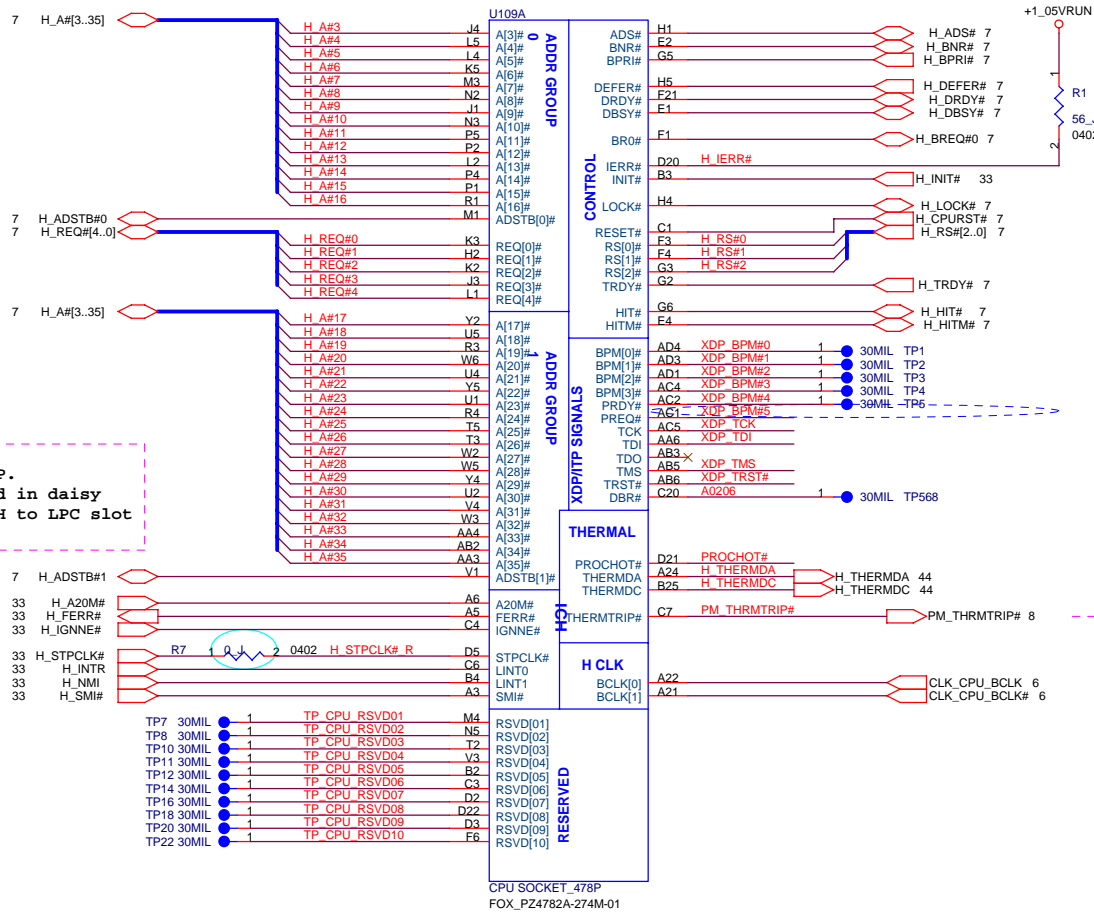
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

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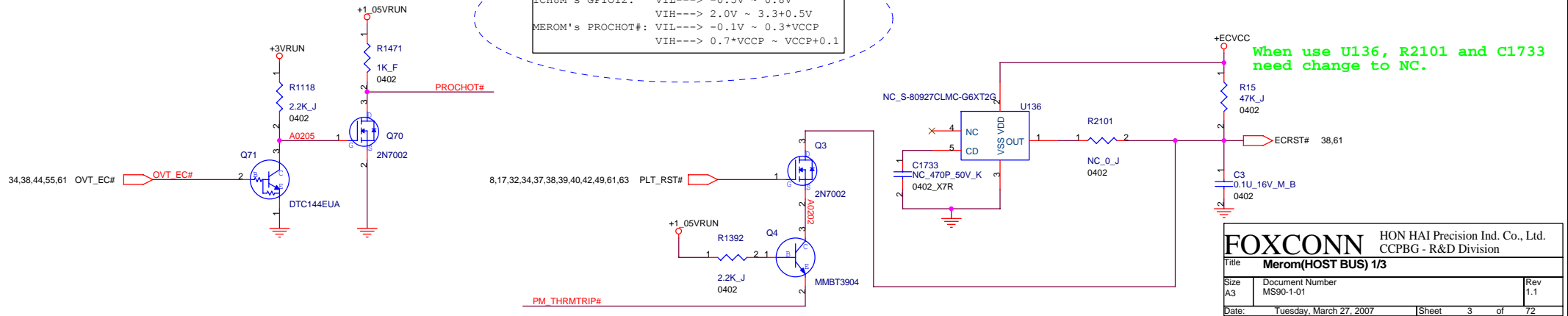


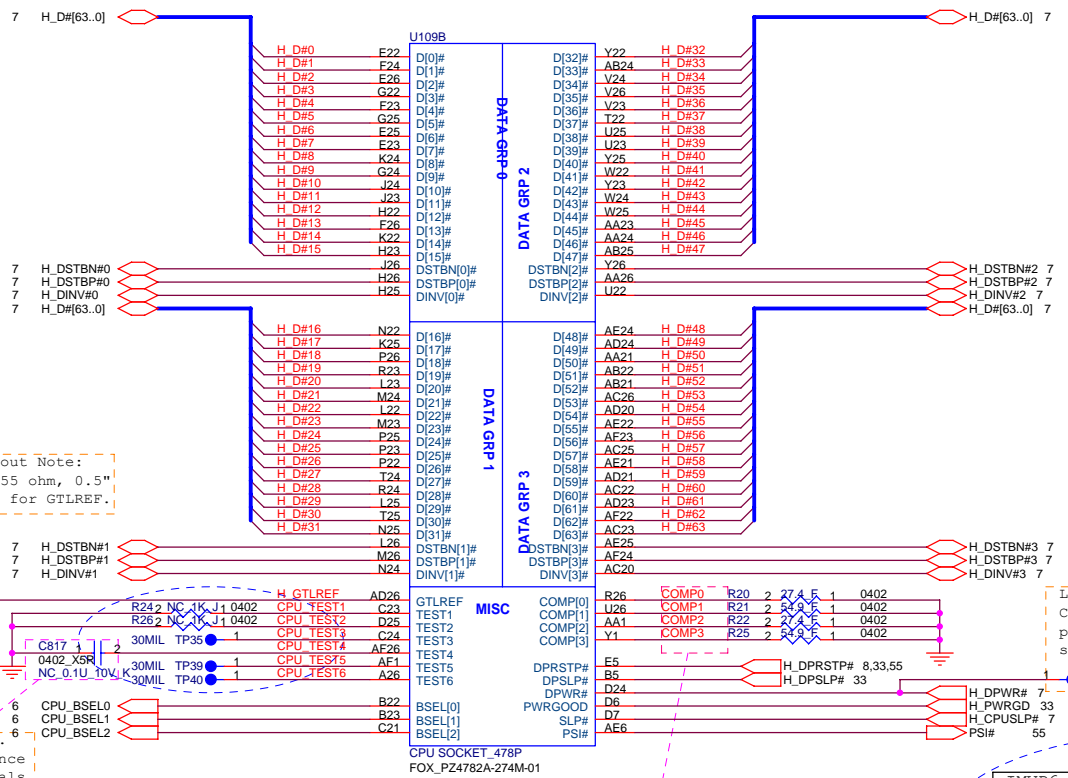


Layout note:  
no stub on H\_STPCLK TP.  
H\_STPCLK# to be routed in daisy chain fashion from ICH to LPC slot and then to CPU.

ICH8M's GPIO12: VIL----> -0.5V ~ 0.8V  
VIH----> 2.0V ~ 3.3+0.5V  
MEMROM's PROCHOT#: VIL----> -0.1V ~ 0.3\*VCCP  
VIH----> 0.7\*VCCP ~ VCCP+0.1

When use U136, R2101 and C1733 need change to NC.





Layout Note:  
 $Z_0=55$  ohm, 0.5"  
 max for GTLREF.

Layout:  
 Connect test  
 point with no  
 stub

Layout Note:  
 Comp0,2 connect with  $Z_0=27.4$  ohm, make  
 trace length shorter than 0.5".  
 Comp1,3 connect with  $Z_0=55$  ohm, make  
 trace length shorter than 0.5".

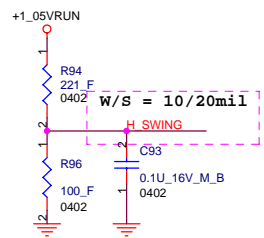
IMVP6 (ISL6262ACRZ-T)  
 cpu PSI# <-> ISL6262ACRZ-T PSI#  
 ISL6262ACRZ-T: VIHmin=0.315V  
 VILmax=0.735V  
 (ref. IMVP-6 NO:18904)

Place close to CPU

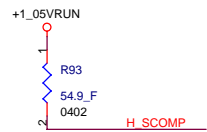
Place C817 close to the CPU\_TEST4 pin.  
 Make sure CPU\_TEST4 routing is reference  
 to GND and away from other noisy signals.



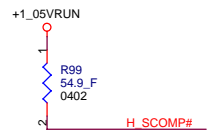




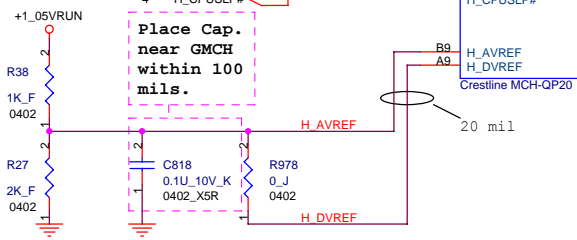
W/S = 10/20mil  
H\_RCOMP



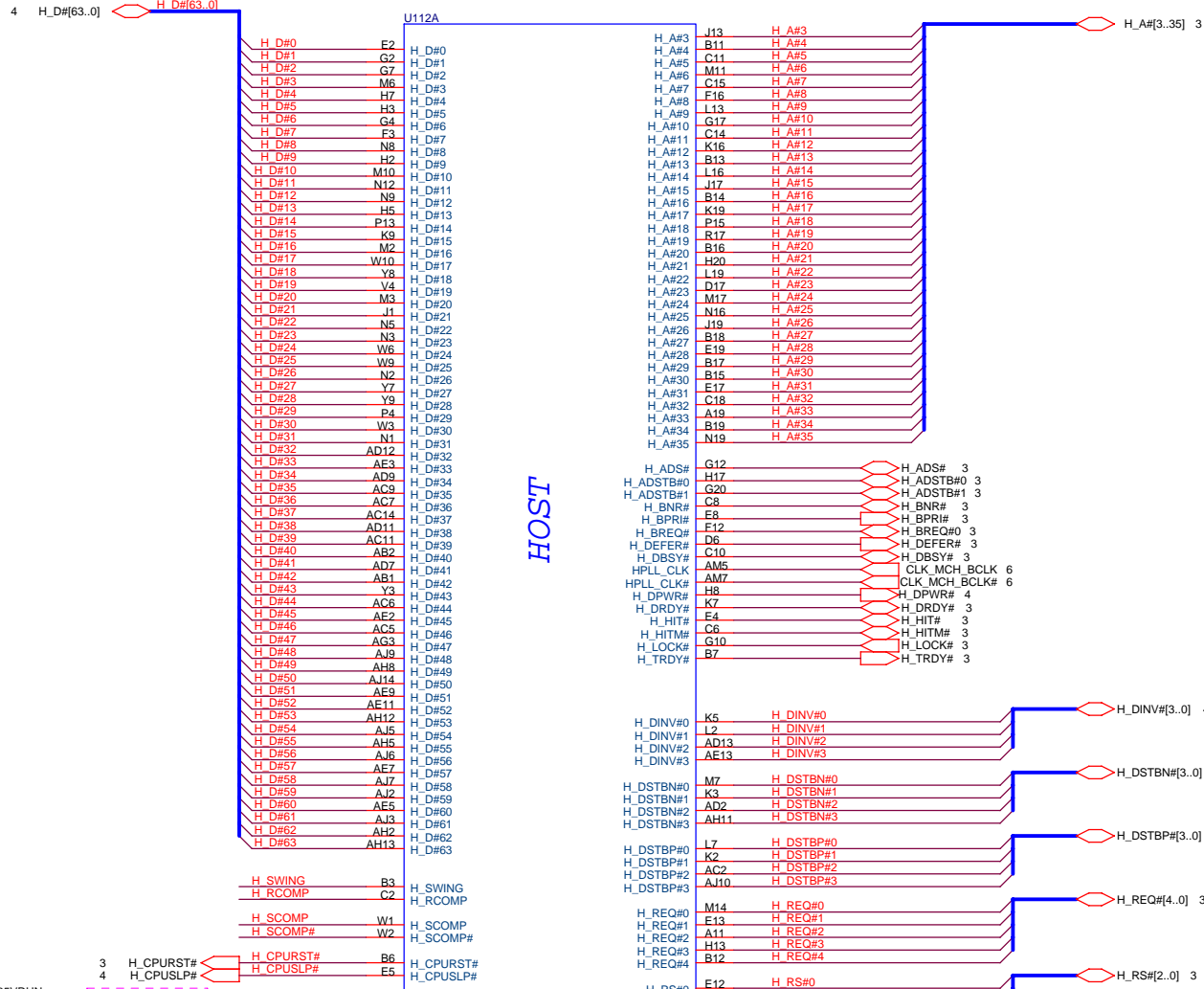
H\_SCOMP



H\_SCOMP#

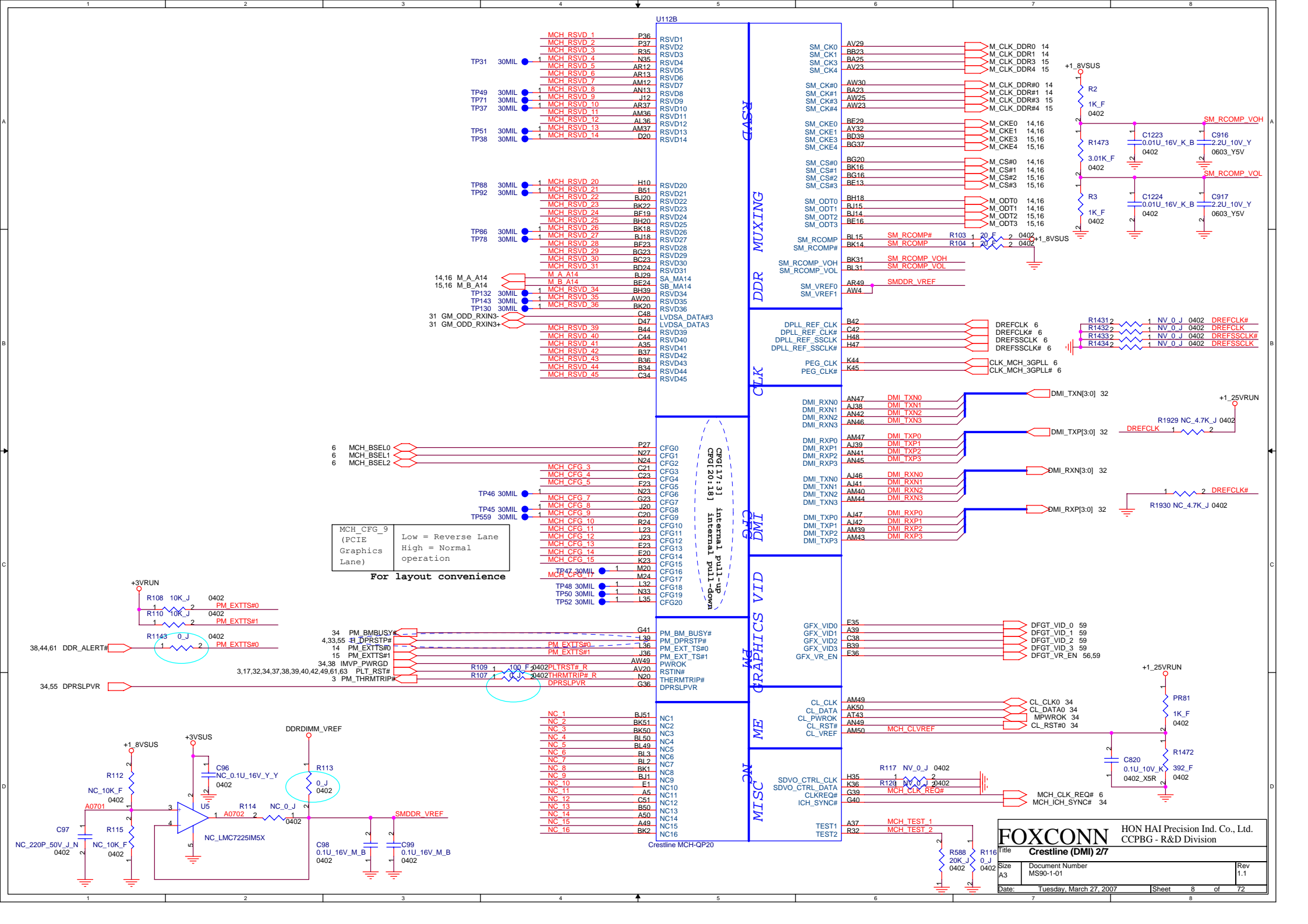


Place Cap.  
near GMCH  
within 100  
mils.



HOST

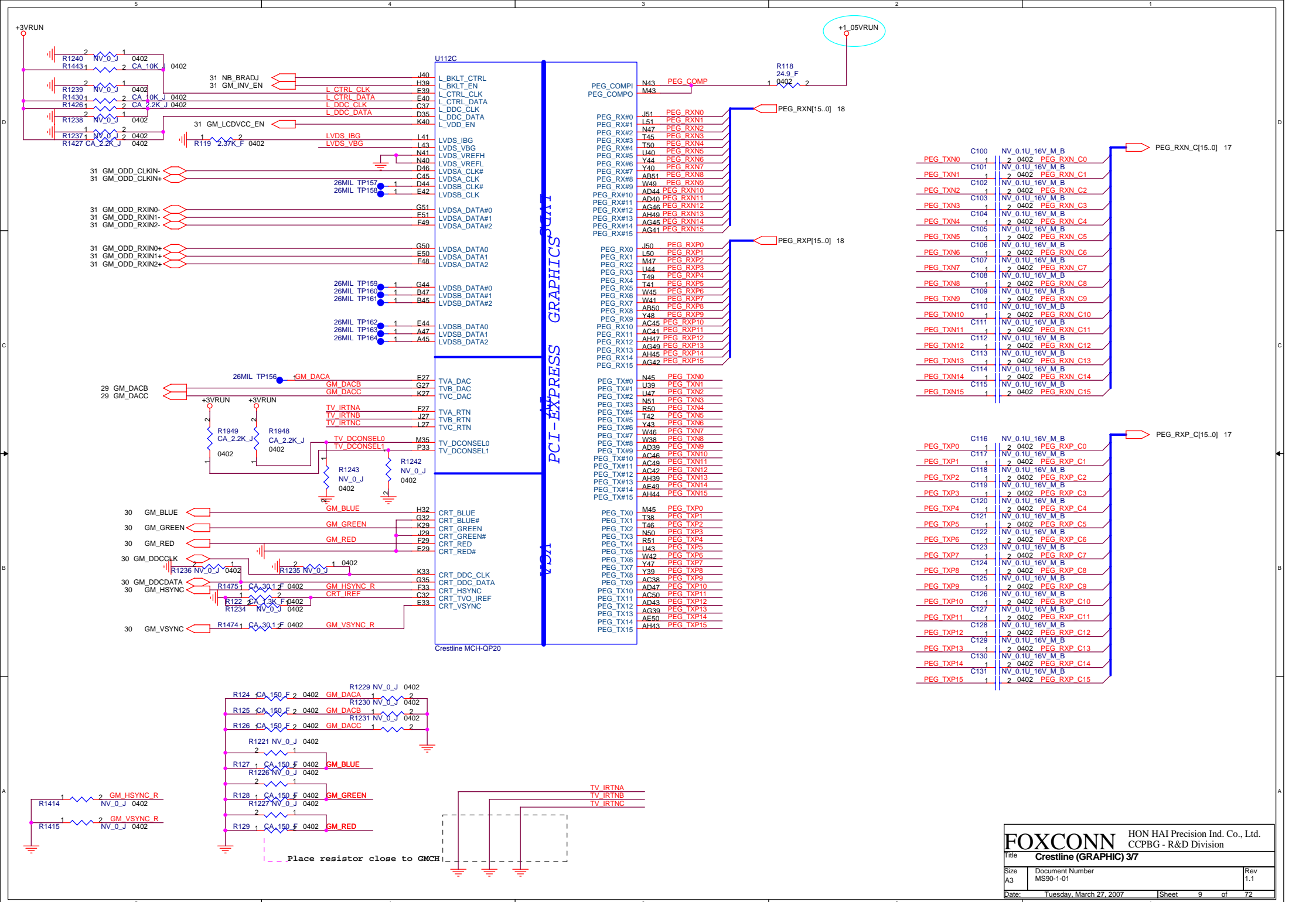




MCH\_CFG\_9  
(PCIe Graphics Lane)  
Low = Reverse Lane  
High = Normal operation

**For layout convenience**





14 M\_A\_DQ[63..0]

- M\_A DQ0 AR43
- M\_A DQ1 AW44
- M\_A DQ2 BA45
- M\_A DQ3 AY46
- M\_A DQ4 AR41
- M\_A DQ5 AR45
- M\_A DQ6 AT42
- M\_A DQ7 AW47
- M\_A DQ8 BB45
- M\_A DQ9 BF48
- M\_A DQ10 BG47
- M\_A DQ11 BJ45
- M\_A DQ12 BB47
- M\_A DQ13 BG50
- M\_A DQ14 BH49
- M\_A DQ15 BE45
- M\_A DQ16 AW43
- M\_A DQ17 BE44
- M\_A DQ18 BG42
- M\_A DQ19 BE40
- M\_A DQ20 BE44
- M\_A DQ21 BH45
- M\_A DQ22 BG40
- M\_A DQ23 BF40
- M\_A DQ24 AR40
- M\_A DQ25 AW40
- M\_A DQ26 AT39
- M\_A DQ27 AW36
- M\_A DQ28 AW41
- M\_A DQ29 AY41
- M\_A DQ30 AV38
- M\_A DQ31 AT38
- M\_A DQ32 AV13
- M\_A DQ33 AT13
- M\_A DQ34 AW11
- M\_A DQ35 AV11
- M\_A DQ36 AU15
- M\_A DQ37 AT11
- M\_A DQ38 BA13
- M\_A DQ39 BA11
- M\_A DQ40 BE10
- M\_A DQ41 BD10
- M\_A DQ42 BD8
- M\_A DQ43 AY9
- M\_A DQ44 BG10
- M\_A DQ45 AW9
- M\_A DQ46 BD7
- M\_A DQ47 AR50
- M\_A DQ48 BB5
- M\_A DQ49 AY7
- M\_A DQ50 AT5
- M\_A DQ51 AT7
- M\_A DQ52 AY6
- M\_A DQ53 BB7
- M\_A DQ54 AR5
- M\_A DQ55 AR8
- M\_A DQ56 AR9
- M\_A DQ57 AN3
- M\_A DQ58 AM8
- M\_A DQ59 AN10
- M\_A DQ60 AT9
- M\_A DQ61 AN8
- M\_A DQ62 AM9
- M\_A DQ63 AN11

U112D

DDR SYSTEM MEMORY A

- SA\_BS0 BB19
- SA\_BS1 BK19
- SA\_BS2 BF29
- SA\_CAS# BL17
- SA\_DM0 AT45
- SA\_DM1 BD44
- SA\_DM2 BD42
- SA\_DM3 AW38
- SA\_DM4 AW13
- SA\_DM5 BG8
- SA\_DM6 AY5
- SA\_DM7 AN6
- SA\_DQS0 AT46
- SA\_DQS1 BE48
- SA\_DQS2 BB43
- SA\_DQS3 BC37
- SA\_DQS4 BB16
- SA\_DQS5 BH6
- SA\_DQS6 BB2
- SA\_DQS7 AP3
- SA\_DQS8 AT47
- SA\_DQS9 BD47
- SA\_DQS10 BC41
- SA\_DQS11 BC37
- SA\_DQS12 BA16
- SA\_DQS13 BH7
- SA\_DQS14 BC1
- SA\_DQS15 AP2
- SA\_MA0 BJ19
- SA\_MA1 BD20
- SA\_MA2 BK27
- SA\_MA3 BH28
- SA\_MA4 BL24
- SA\_MA5 BK28
- SA\_MA6 BJ27
- SA\_MA7 BJ25
- SA\_MA8 BL28
- SA\_MA9 BA28
- SA\_MA10 BC19
- SA\_MA11 BE28
- SA\_MA12 BG30
- SA\_MA13 BJ16
- SA\_RAS# BE18
- SA\_RCVEN# AY20
- SA\_WE# BA19
- M\_A\_BS0 14,16
- M\_A\_BS1 14,16
- M\_A\_BS2 14,16
- M\_A\_CAS# 14,16
- M\_A\_DM[7..0] 14
- M\_A\_DQS[7..0] 14
- M\_A\_DQS#[7..0] 14
- M\_A\_A[13..0] 14,16
- M\_A\_RAS# 14,16
- M\_A\_WE# 14,16

Crestline MCH-QP20

15 M\_B\_DQ[63..0]

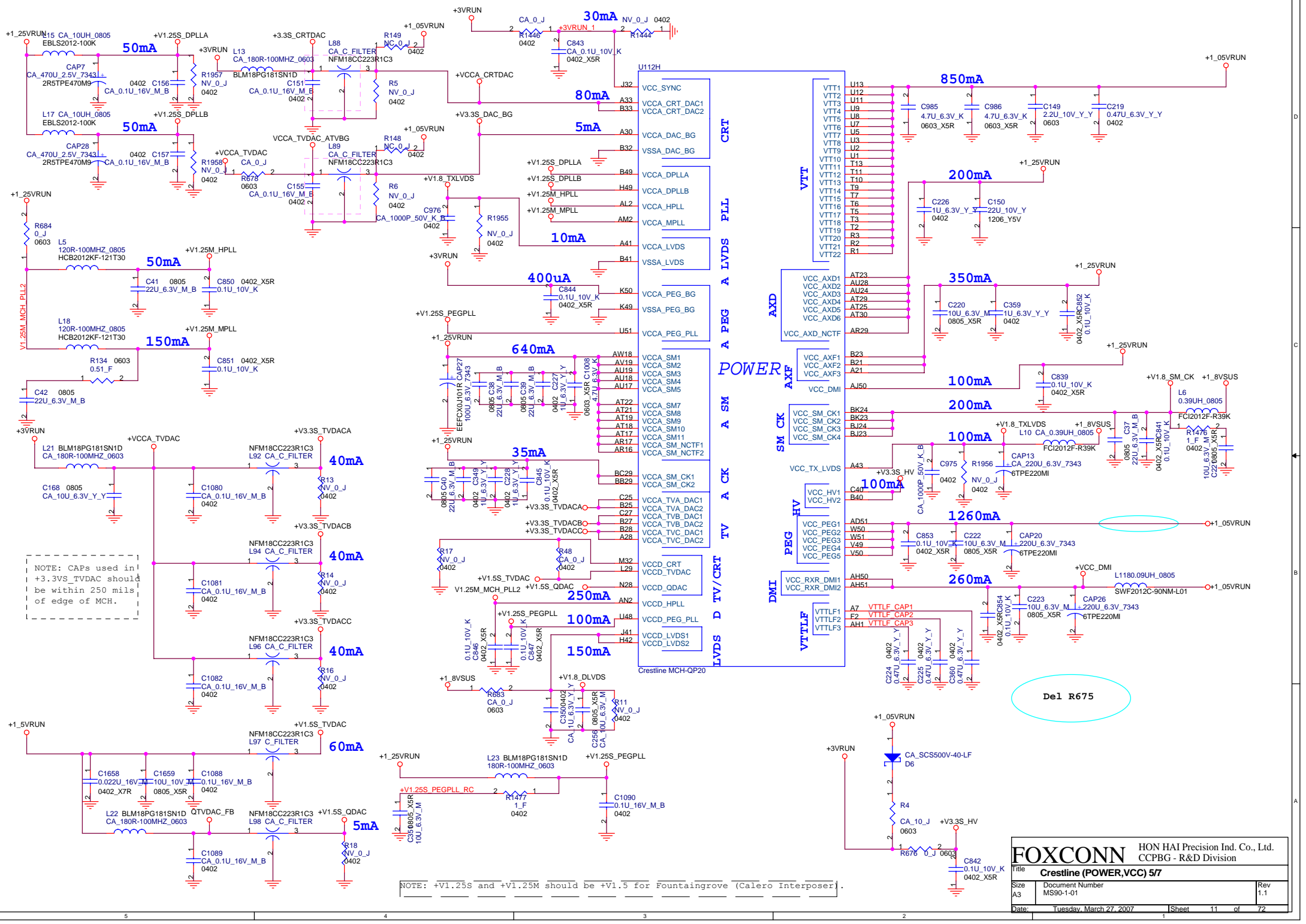
- M\_B DQ0 AP49
- M\_B DQ1 AR51
- M\_B DQ2 AW50
- M\_B DQ3 AW51
- M\_B DQ4 AN61
- M\_B DQ5 AN50
- M\_B DQ6 AV50
- M\_B DQ7 AV49
- M\_B DQ8 BA50
- M\_B DQ9 BB50
- M\_B DQ10 BA49
- M\_B DQ11 BE50
- M\_B DQ12 BA51
- M\_B DQ13 AY49
- M\_B DQ14 BF50
- M\_B DQ15 BF49
- M\_B DQ16 BJ50
- M\_B DQ17 BJ44
- M\_B DQ18 BJ43
- M\_B DQ19 BL43
- M\_B DQ20 BK47
- M\_B DQ21 BK49
- M\_B DQ22 BK43
- M\_B DQ23 BK42
- M\_B DQ24 BK42
- M\_B DQ25 BL41
- M\_B DQ26 BJ37
- M\_B DQ27 BJ36
- M\_B DQ28 BK41
- M\_B DQ29 BJ40
- M\_B DQ30 BL35
- M\_B DQ31 BK37
- M\_B DQ32 BK13
- M\_B DQ33 BE11
- M\_B DQ34 BK11
- M\_B DQ35 BC11
- M\_B DQ36 BC13
- M\_B DQ37 BE12
- M\_B DQ38 BC12
- M\_B DQ39 BG12
- M\_B DQ40 BJ10
- M\_B DQ41 BL9
- M\_B DQ42 BK5
- M\_B DQ43 BL5
- M\_B DQ44 BK9
- M\_B DQ45 BK10
- M\_B DQ46 BJ8
- M\_B DQ47 BJ6
- M\_B DQ48 BF4
- M\_B DQ49 BH5
- M\_B DQ50 BG1
- M\_B DQ51 BC2
- M\_B DQ52 BK3
- M\_B DQ53 BE4
- M\_B DQ54 BD3
- M\_B DQ55 BJ2
- M\_B DQ56 BA3
- M\_B DQ57 BB3
- M\_B DQ58 AR1
- M\_B DQ59 AT3
- M\_B DQ60 AY2
- M\_B DQ61 AY3
- M\_B DQ62 AU2
- M\_B DQ63 AT2

U112E

DDR SYSTEM MEMORY B

- SB\_DQ0 AP49
- SB\_DQ1 AR51
- SB\_DQ2 AW50
- SB\_DQ3 AW51
- SB\_DQ4 AN61
- SB\_DQ5 AN50
- SB\_DQ6 AV50
- SB\_DQ7 AV49
- SB\_DQ8 BA50
- SB\_DQ9 BB50
- SB\_DQ10 BA49
- SB\_DQ11 BE50
- SB\_DQ12 BA51
- SB\_DQ13 AY49
- SB\_DQ14 BF50
- SB\_DQ15 BF49
- SB\_DQ16 BJ50
- SB\_DQ17 BJ44
- SB\_DQ18 BJ43
- SB\_DQ19 BL43
- SB\_DQ20 BK47
- SB\_DQ21 BK49
- SB\_DQ22 BK43
- SB\_DQ23 BK42
- SB\_DQ24 BK42
- SB\_DQ25 BL41
- SB\_DQ26 BJ37
- SB\_DQ27 BJ36
- SB\_DQ28 BK41
- SB\_DQ29 BJ40
- SB\_DQ30 BL35
- SB\_DQ31 BK37
- SB\_DQ32 BK13
- SB\_DQ33 BE11
- SB\_DQ34 BK11
- SB\_DQ35 BC11
- SB\_DQ36 BC13
- SB\_DQ37 BE12
- SB\_DQ38 BC12
- SB\_DQ39 BG12
- SB\_DQ40 BJ10
- SB\_DQ41 BL9
- SB\_DQ42 BK5
- SB\_DQ43 BL5
- SB\_DQ44 BK9
- SB\_DQ45 BK10
- SB\_DQ46 BJ8
- SB\_DQ47 BJ6
- SB\_DQ48 BF4
- SB\_DQ49 BH5
- SB\_DQ50 BG1
- SB\_DQ51 BC2
- SB\_DQ52 BK3
- SB\_DQ53 BE4
- SB\_DQ54 BD3
- SB\_DQ55 BJ2
- SB\_DQ56 BA3
- SB\_DQ57 BB3
- SB\_DQ58 AR1
- SB\_DQ59 AT3
- SB\_DQ60 AY2
- SB\_DQ61 AY3
- SB\_DQ62 AU2
- SB\_DQ63 AT2
- SB\_BS0 AY17
- SB\_BS1 BG18
- SB\_BS2 BG36
- SB\_CAS# BE17
- SB\_DM0 AR50
- SB\_DM1 BD49
- SB\_DM2 BK45
- SB\_DM3 BL39
- SB\_DM4 BH12
- SB\_DM5 BJ7
- SB\_DM6 BF1
- SB\_DM7 AW2
- SB\_DQS0 AT50
- SB\_DQS1 BD50
- SB\_DQS2 BK46
- SB\_DQS3 BK39
- SB\_DQS4 BJ12
- SB\_DQS5 BL7
- SB\_DQS6 BE2
- SB\_DQS7 AV2
- SB\_DQS8 AU50
- SB\_DQS9 BC50
- SB\_DQS10 BL45
- SB\_DQS11 BK38
- SB\_DQS12 BK12
- SB\_DQS13 BK7
- SB\_DQS14 BE2
- SB\_DQS15 AV3
- SB\_MA0 BC18
- SB\_MA1 BG28
- SB\_MA2 BG25
- SB\_MA3 AW17
- SB\_MA4 BF25
- SB\_MA5 BE25
- SB\_MA6 BA29
- SB\_MA7 BC28
- SB\_MA8 AY28
- SB\_MA9 BD37
- SB\_MA10 BG17
- SB\_MA11 BE37
- SB\_MA12 BA39
- SB\_MA13 BG13
- SB\_RAS# AV16
- SB\_RCVEN# AY18
- SB\_WE# BC17
- M\_B\_BS0 15,16
- M\_B\_BS1 15,16
- M\_B\_BS2 15,16
- M\_B\_CAS# 15,16
- M\_B\_DM[7..0] 15
- M\_B\_DQS[7..0] 15
- M\_B\_DQS#[7..0] 15
- M\_B\_A[13..0] 15,16
- M\_B\_RAS# 15,16
- M\_B\_WE# 15,16

Crestline MCH-QP20

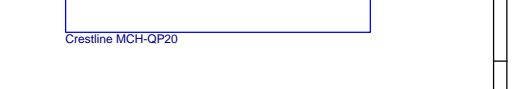
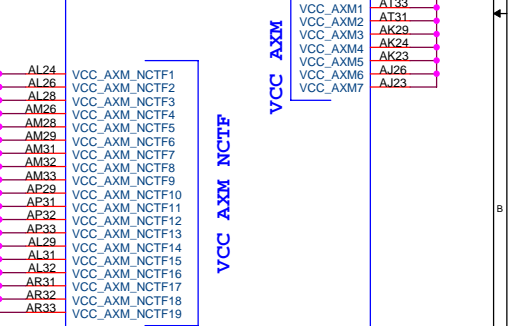
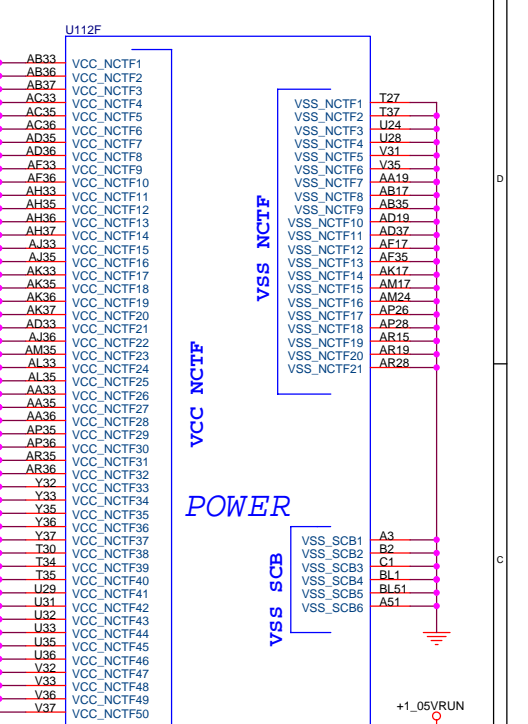
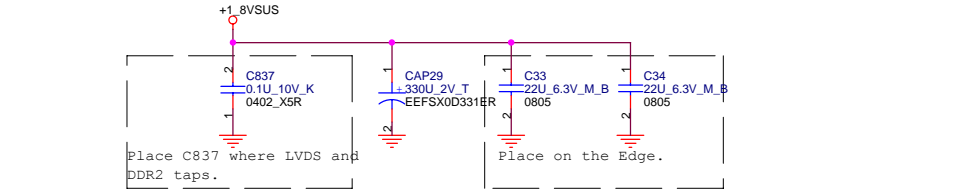
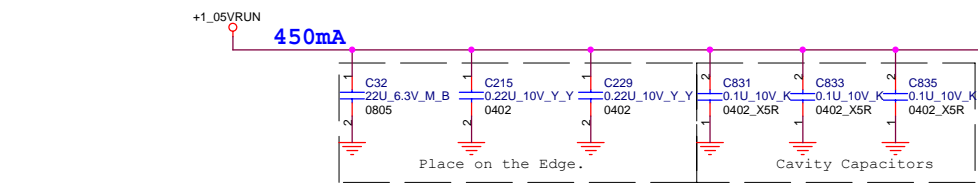
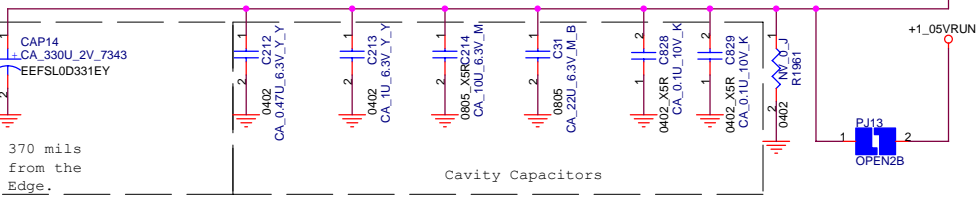
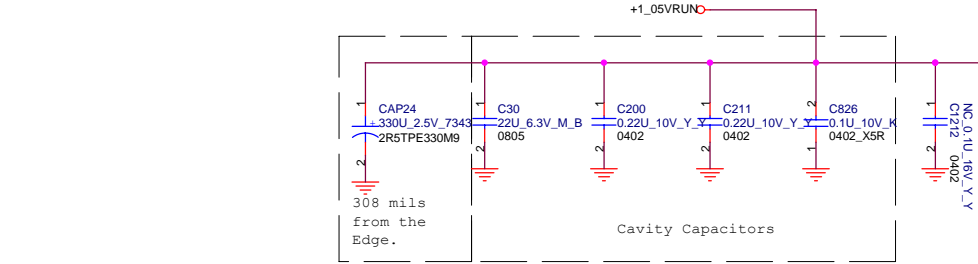
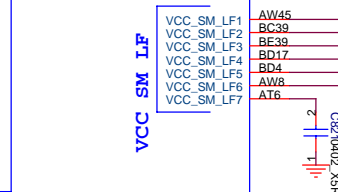
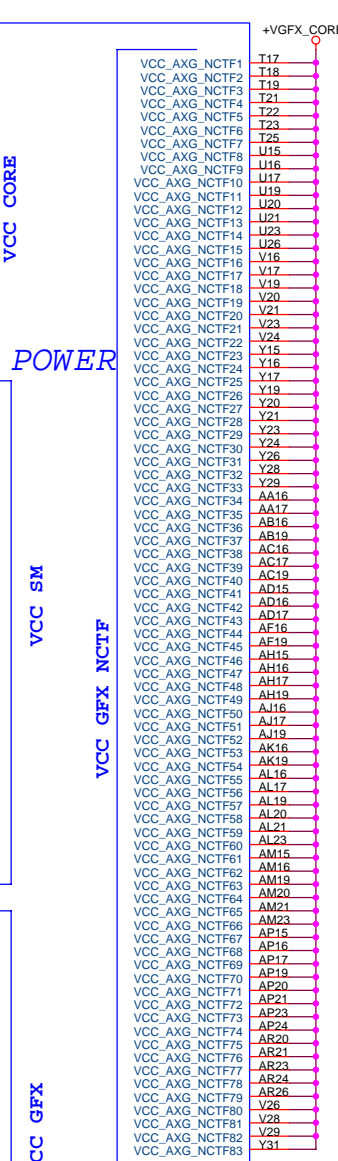
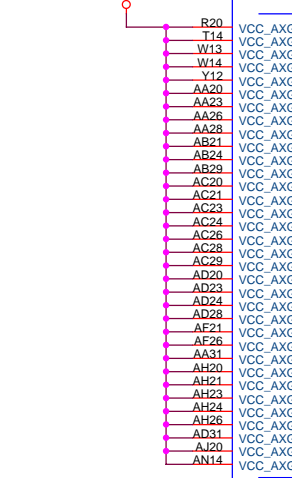
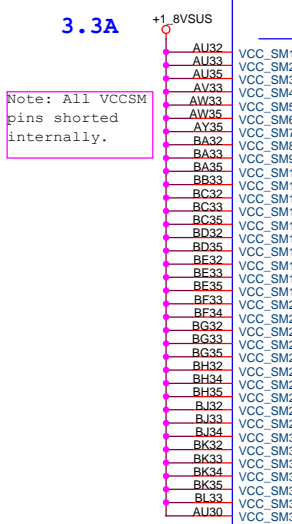
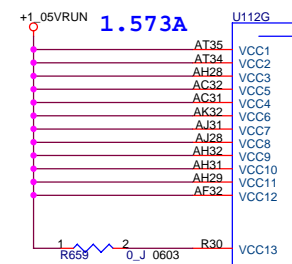


NOTE: CAPs used in +3.3VS TVDAC should be within 250 mils of edge of MCH.

NOTE: +V1.25s and +V1.25M should be +V1.5 for Fountaingrove (Calero Interposer).

De1 R675

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
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Crestline MCH-QP20

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U112I		U112J	
A13	VSS1	VSS100	AW24
A15	VSS2	VSS101	AW29
A17	VSS3	VSS102	AW32
A24	VSS4	VSS103	AW5
AA21	VSS5	VSS104	AW7
AA24	VSS6	VSS105	AX10
AA29	VSS7	VSS106	AY24
AB20	VSS8	VSS107	AY37
AB23	VSS9	VSS108	AY42
AB26	VSS10	VSS109	AY43
AB28	VSS11	VSS110	AY45
AB31	VSS12	VSS111	AY47
AC10	VSS13	VSS112	AY50
AC13	VSS14	VSS113	B10
AC3	VSS15	VSS114	B20
AC39	VSS16	VSS115	B24
AC43	VSS17	VSS116	B29
AC47	VSS18	VSS117	B30
AD1	VSS19	VSS118	B35
AD21	VSS20	VSS119	B38
AD26	VSS21	VSS120	B43
AD29	VSS22	VSS121	B46
AD3	VSS23	VSS122	B5
AD41	VSS24	VSS123	B8
AD45	VSS25	VSS124	BA1
AD49	VSS26	VSS125	BA17
AD5	VSS27	VSS126	BA18
AD50	VSS28	VSS127	BA2
AD8	VSS29	VSS128	BA24
AE10	VSS30	VSS129	BE12
AE14	VSS31	VSS130	BB25
AE6	VSS32	VSS131	BB40
AF20	VSS33	VSS132	BB44
AF23	VSS34	VSS133	BB49
AF24	VSS35	VSS134	BB8
AF31	VSS36	VSS135	BC16
AG2	VSS37	VSS136	BC24
AG38	VSS38	VSS137	BC25
AG43	VSS39	VSS138	BC36
AG47	VSS40	VSS139	BC40
AG50	VSS41	VSS140	BC51
AH3	VSS42	VSS141	BD13
AH40	VSS43	VSS142	BD2
AH41	VSS44	VSS143	BD28
AH7	VSS45	VSS144	BD45
AH9	VSS46	VSS145	BD48
AJ11	VSS47	VSS146	BD5
AJ13	VSS48	VSS147	BE1
AJ21	VSS49	VSS148	BE19
AJ24	VSS50	VSS149	BE23
AJ29	VSS51	VSS150	BE30
AJ32	VSS52	VSS151	BE42
AJ43	VSS53	VSS152	BE51
AJ45	VSS54	VSS153	BE8
AJ49	VSS55	VSS154	BF12
AK20	VSS56	VSS155	BF16
AK21	VSS57	VSS156	BF36
AK26	VSS58	VSS157	BF39
AK28	VSS59	VSS158	BG2
AK31	VSS60	VSS159	BG24
AK51	VSS61	VSS160	BG29
AL1	VSS62	VSS161	BG39
AM11	VSS63	VSS162	BG48
AM13	VSS64	VSS163	BG5
AM3	VSS65	VSS164	BG51
AM4	VSS66	VSS165	BH17
AM41	VSS67	VSS166	BH30
AM45	VSS68	VSS167	BH44
AN1	VSS69	VSS168	BH46
AN38	VSS70	VSS169	BH8
AN39	VSS71	VSS170	BJ11
AN43	VSS72	VSS171	BJ13
AN5	VSS73	VSS172	BJ38
AN7	VSS74	VSS173	BJ4
AP4	VSS75	VSS174	BJ42
AP48	VSS76	VSS175	BJ46
AP50	VSS77	VSS176	BK15
AR11	VSS78	VSS177	BK17
AR2	VSS79	VSS178	BK25
AR39	VSS80	VSS179	BK29
AR44	VSS81	VSS180	BK36
AR47	VSS82	VSS181	BK40
AR7	VSS83	VSS182	BK44
AT10	VSS84	VSS183	BK6
AT14	VSS85	VSS184	BK8
AT41	VSS86	VSS185	BL11
AT49	VSS87	VSS186	BL13
AU1	VSS88	VSS187	BL19
AU23	VSS89	VSS188	BL22
AU29	VSS90	VSS189	BL37
AU3	VSS91	VSS190	BL47
AU36	VSS92	VSS191	C12
AU49	VSS93	VSS192	C16
AU51	VSS94	VSS193	C19
AV39	VSS95	VSS194	C28
AV48	VSS96	VSS195	C29
AW1	VSS97	VSS196	C33
AW12	VSS98	VSS197	C36
AW16	VSS99	VSS198	C41

VSS

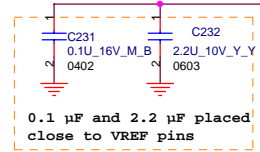
VSS

U112J		W11	
C46	VSS199	VSS287	W39
C50	VSS200	VSS288	W43
C7	VSS201	VSS290	W47
D13	VSS202	VSS291	W5
D24	VSS203	VSS292	W7
D3	VSS204	VSS293	Y13
D32	VSS205	VSS294	Y2
D39	VSS206	VSS295	Y41
D45	VSS207	VSS296	Y45
D49	VSS208	VSS297	Y49
E10	VSS209	VSS298	Y5
E16	VSS210	VSS299	Y50
E24	VSS211	VSS300	Y11
E28	VSS212	VSS301	P29
E32	VSS213	VSS302	T29
E47	VSS214	VSS303	T31
F19	VSS215	VSS304	T33
F36	VSS216	VSS305	R28
F40	VSS217		
F40	VSS218		
F50	VSS219		
G1	VSS220		
G13	VSS221	VSS306	AA32
G16	VSS222	VSS307	AB32
G19	VSS223	VSS308	AD32
G24	VSS224	VSS309	AF28
G28	VSS225	VSS310	AF29
G29	VSS226	VSS311	AT27
G33	VSS227	VSS312	AV25
G42	VSS228	VSS313	H50
G45	VSS229		
G48	VSS230		
G8	VSS231		
H24	VSS232		
H28	VSS233		
H4	VSS234		
H45	VSS235		
J11	VSS236		
J16	VSS237		
J2	VSS238		
J24	VSS239		
J28	VSS240		
J33	VSS241		
J35	VSS242		
J39	VSS243		
K12	VSS245		
K47	VSS246		
K6	VSS247		
L1	VSS248		
L17	VSS249		
L20	VSS250		
L24	VSS251		
L28	VSS252		
L3	VSS253		
L33	VSS254		
L49	VSS255		
M28	VSS256		
M42	VSS257		
M46	VSS258		
M49	VSS259		
M5	VSS260		
M50	VSS261		
M9	VSS262		
N11	VSS263		
N14	VSS264		
N17	VSS265		
N29	VSS266		
N32	VSS267		
N36	VSS268		
N39	VSS269		
N44	VSS270		
N49	VSS271		
N7	VSS272		
P19	VSS273		
P2	VSS274		
P23	VSS275		
P3	VSS276		
P50	VSS277		
R49	VSS278		
T39	VSS279		
T43	VSS280		
T47	VSS281		
U41	VSS282		
U45	VSS283		
U50	VSS284		
V2	VSS285		
V3	VSS286		

Crestline MCH-QP20

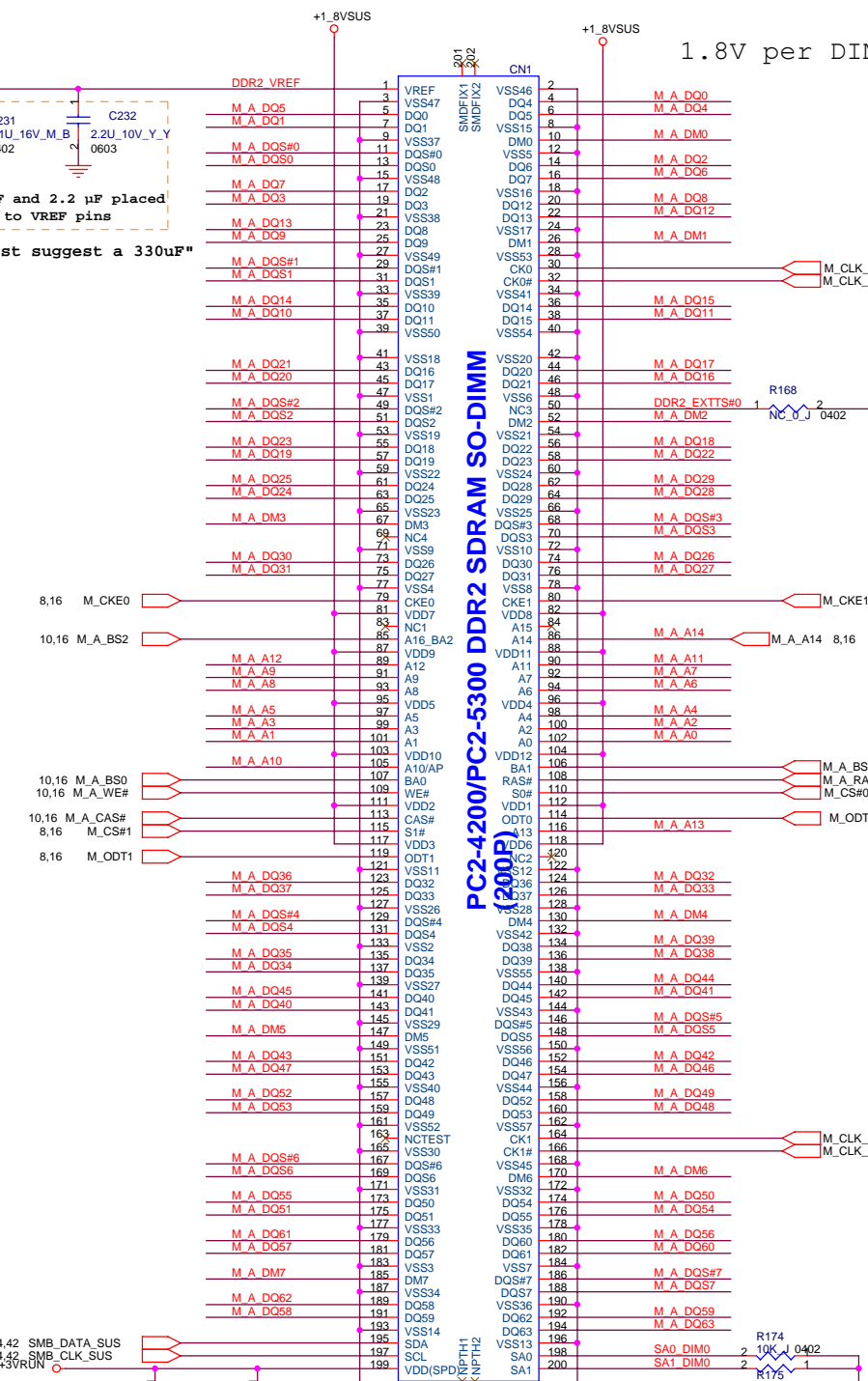
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>Crestline (VSS) 7/7</b>			
Size	Document Number	Rev	
A3	MS90-1-01	1.1	
Date:	Tuesday, March 27, 2007	Sheet	13 of 72





"Intel check list suggest a 330uF"

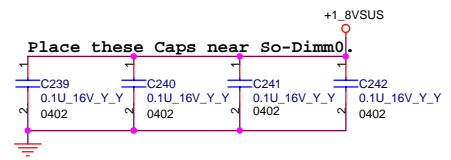
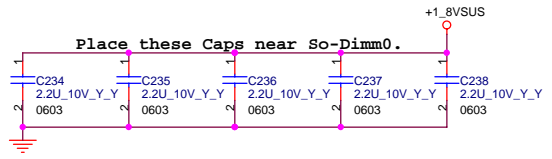
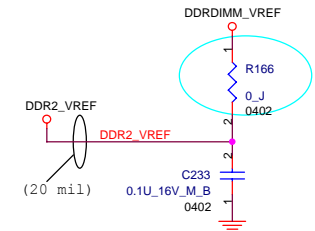
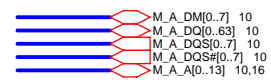
1.8V per DIMM=3.08A



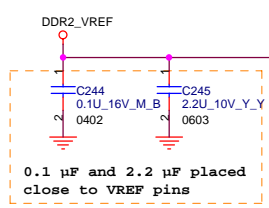
PC2-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)

DDR2 SO-DIMM\_200P  
FOX\_AS0426-N5RN-7F  
SMBus Address: A0(W)/A1(R)

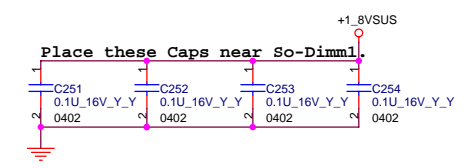
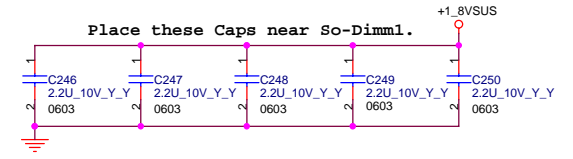
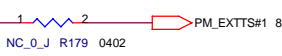
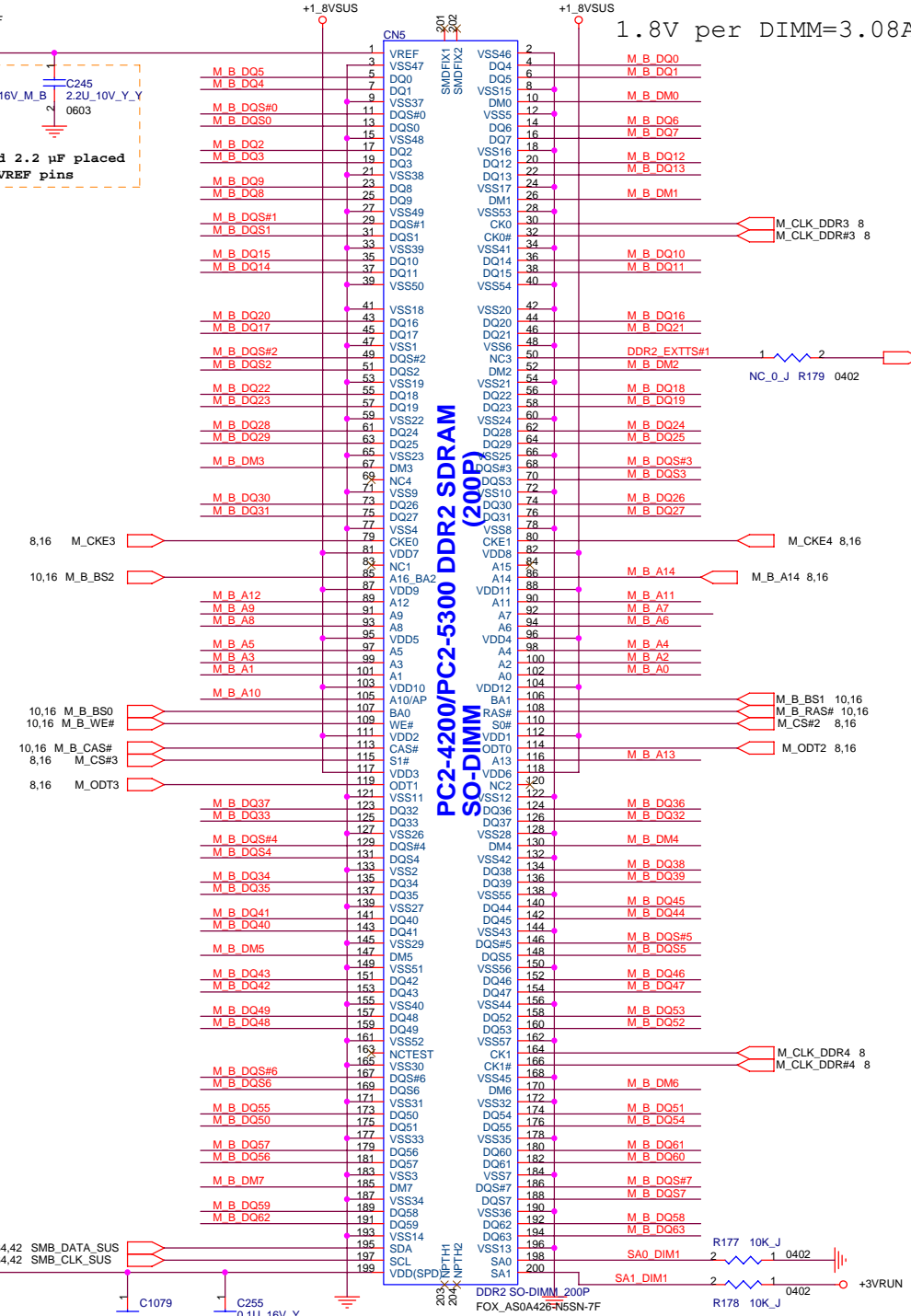
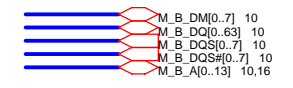
DIMM\_0  
Place DIMM\_0 near GMCH



<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title: <b>DDR(I)SO-DIMM_0</b>		CCPBG - R&D Division	
Size: A3	Document Number: MS90-1-01	Rev: 1.1	
Date: Tuesday, March 27, 2007	Sheet: 14	of: 72	



1.8V per DIMM=3.08A

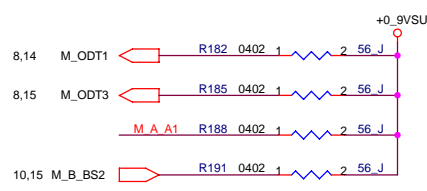
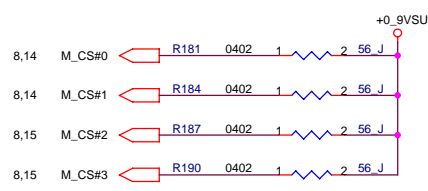
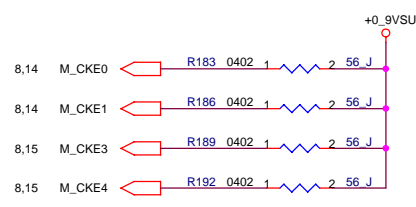
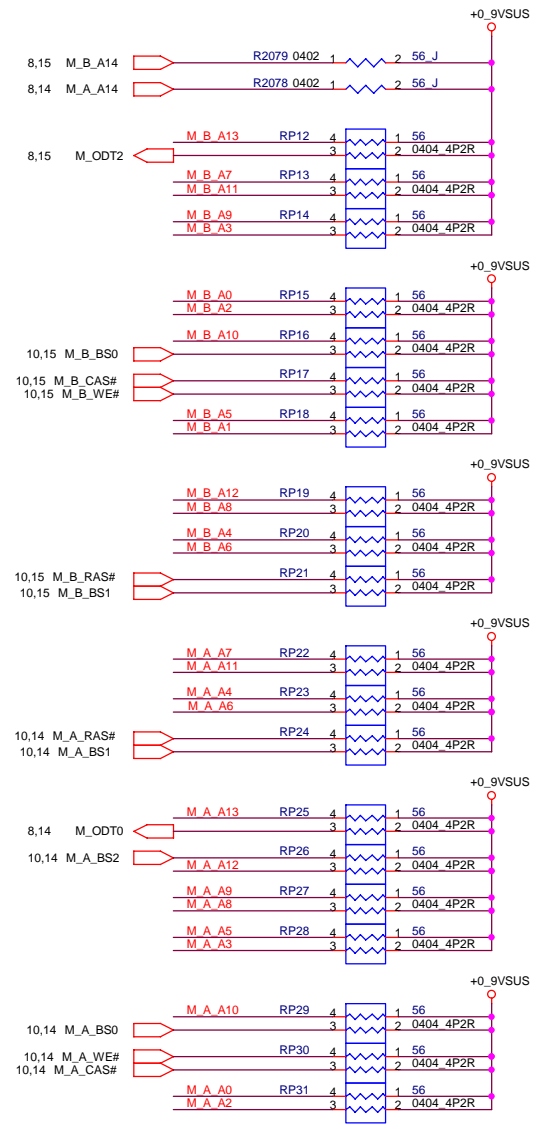
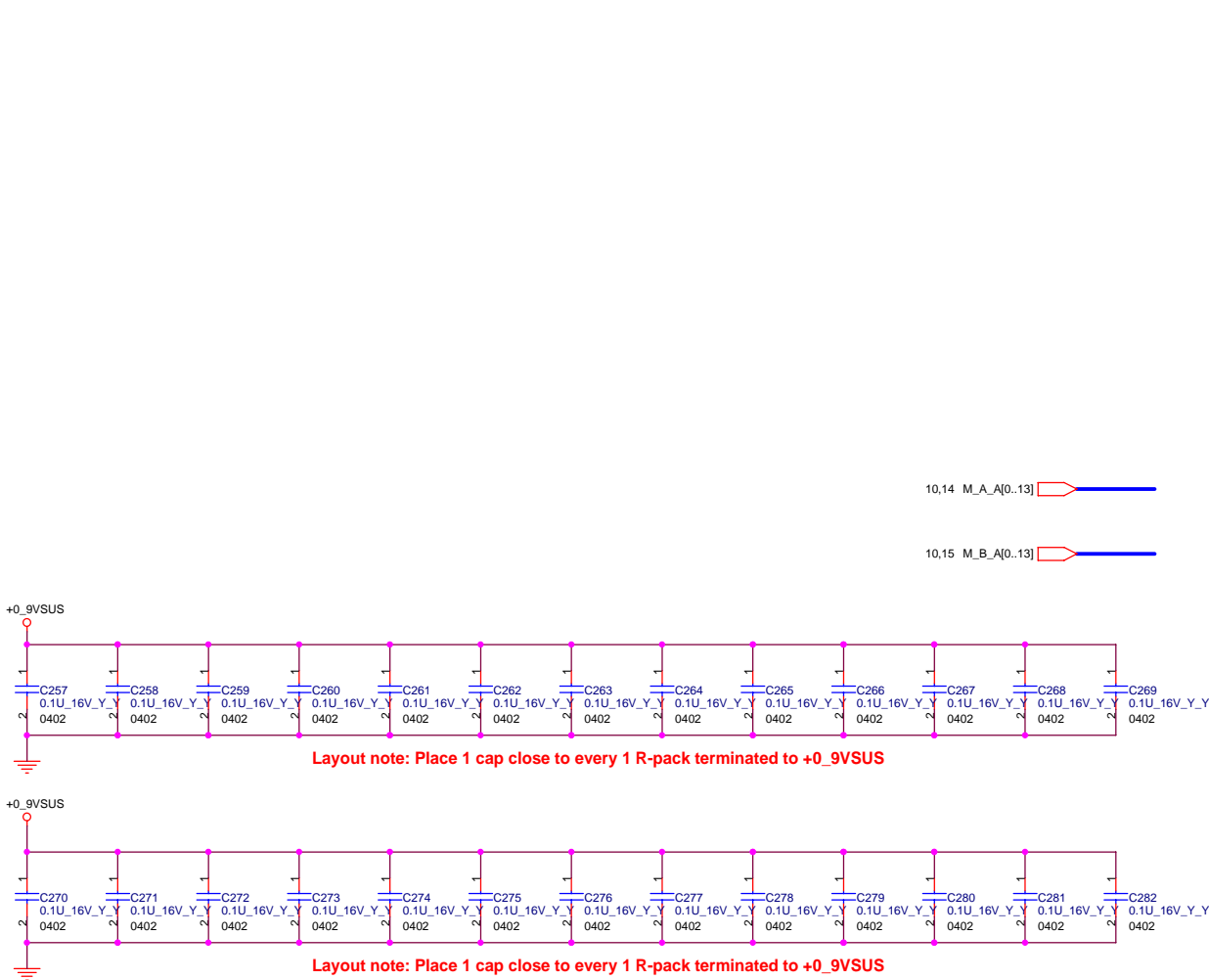


**DIMM\_1**  
SMBus Address: A4(W)/A5(R)

DIMM\_1 is placed farther from the GMCH than DIMM\_0

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	DDR(I)SO-DIMM_1		
Size	Document Number	Rev	
A3	MS90-1-01	1.0	
Date:	Tuesday, March 27, 2007	Sheet	15 of 72

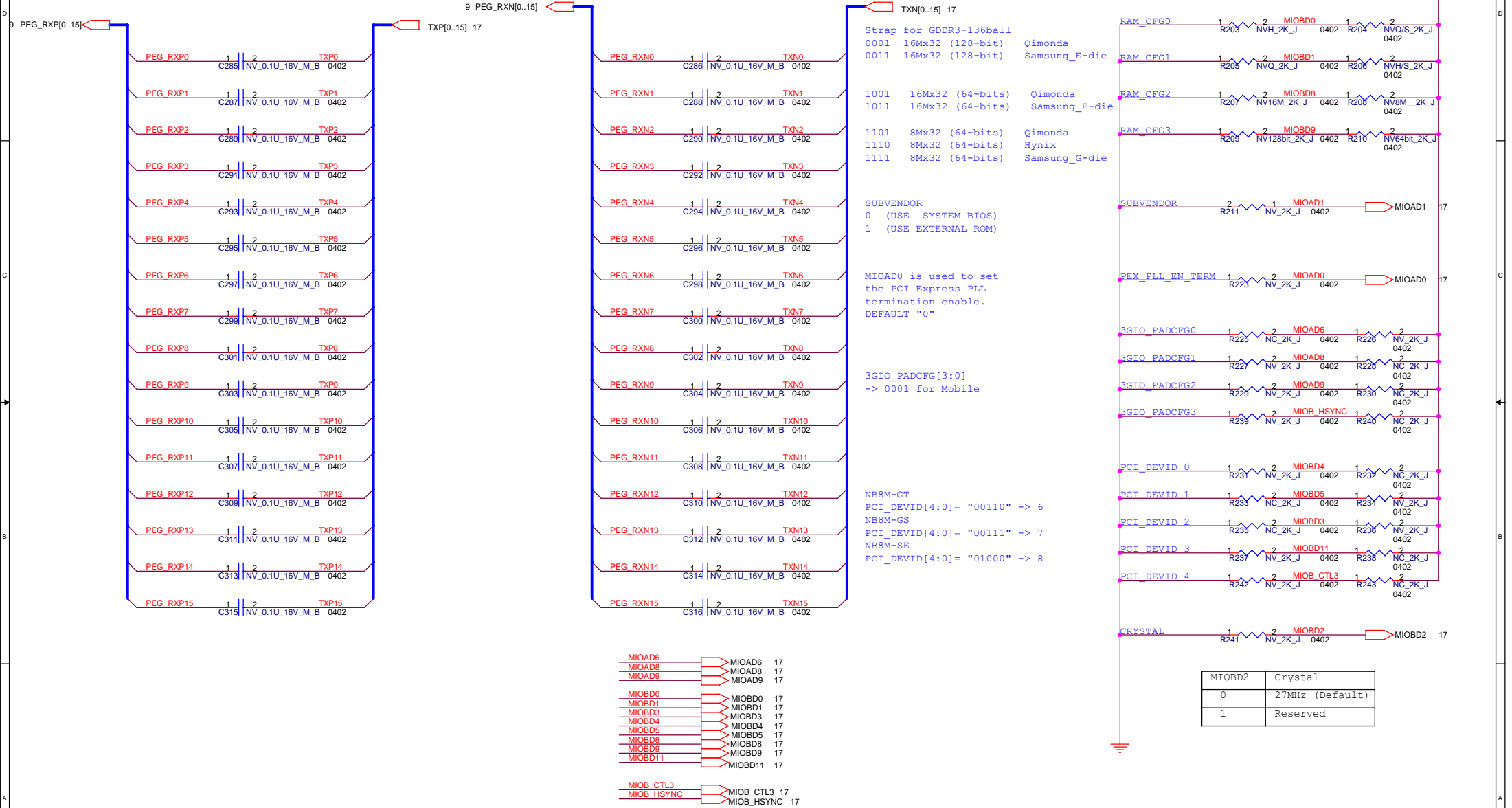




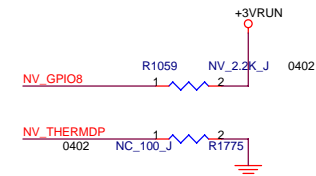
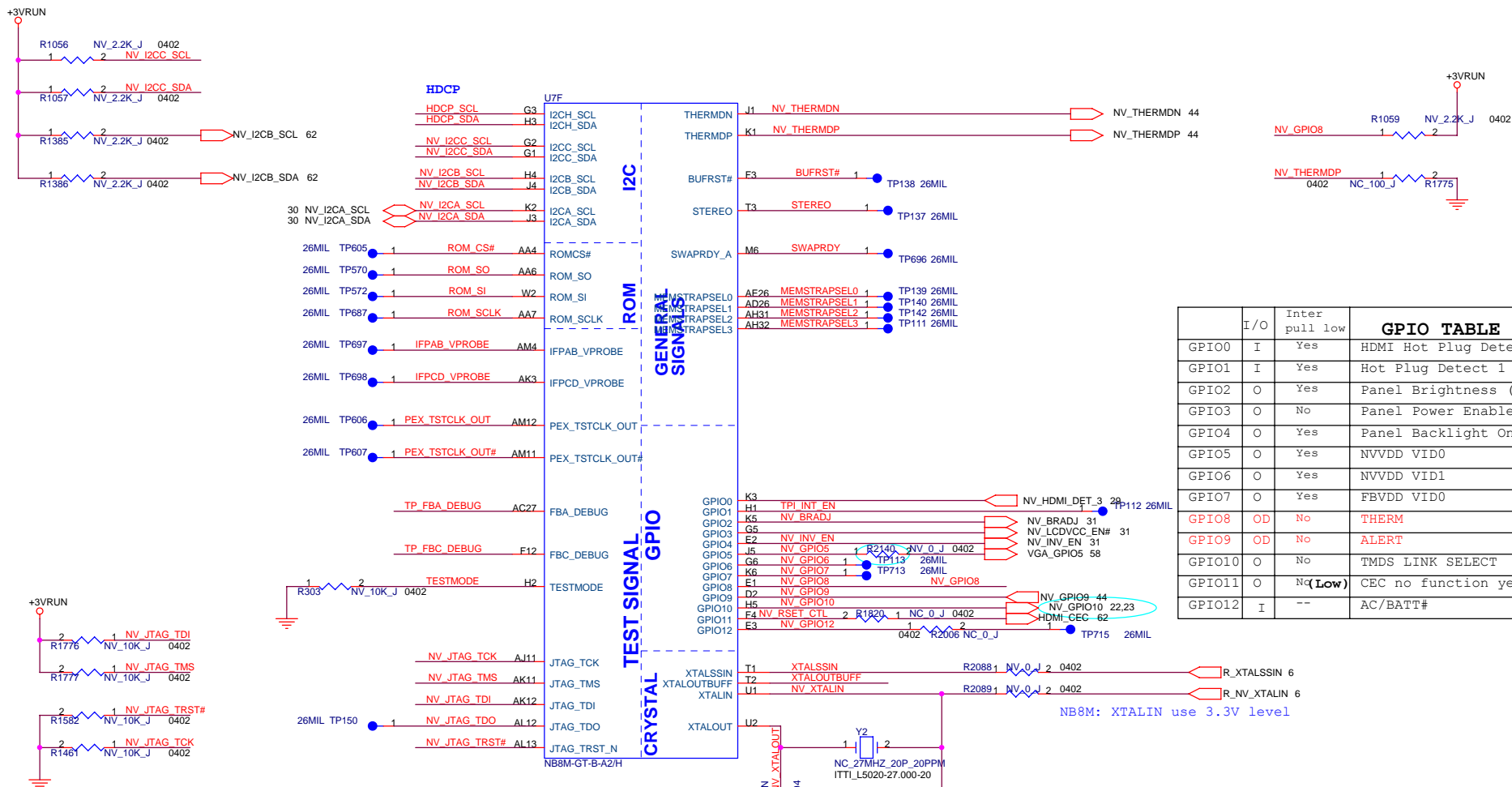


SKU	HH		H		M		
Vender	Qimonda	Samsung	Qimonda	Samsung	Qimonda	Samsung	Hynix
Vendor PN	HYB18H512321BF-14	K4J52324QE-BC14	HYB18H512321BF-14	K4J52324QE-BC14	HYB18H256321AFL16	K4J55323QG-BC14	HY5RS573225AFP-14
H.H PN	13-HYB18H5-3003	13-K4J5232-3001	13-HYB18H5-3003	13-K4J5232-3001	13-HYB18H2-4000	13-K4J5532-3002	13-HY5RS57-3002
Configuration	NB8M-GT with 4pcs (16Mx32) GDDR3		NB8M-GT with 2pcs (16Mx32) GDDR3		NB8M-GT with 2pcs (8Mx32) GDDR3		
LOCATION	Stuff U11,U12,U13,U14		Stuff U11,U12; No stuff U13,U14		Stuff U11,U12; No stuff U13,U14		

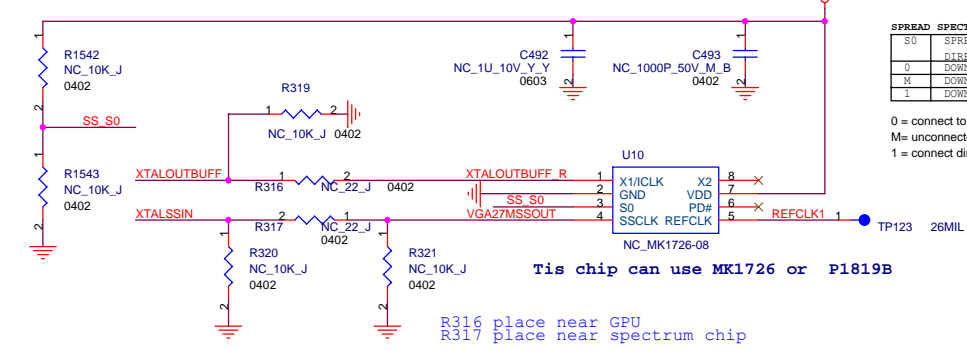
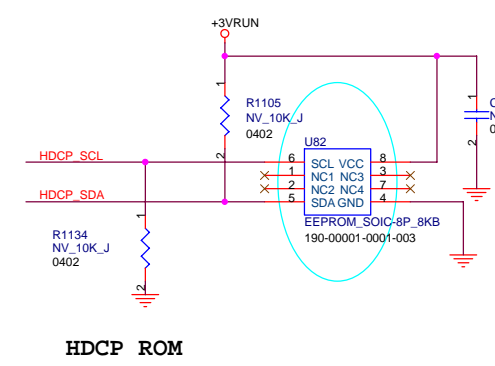
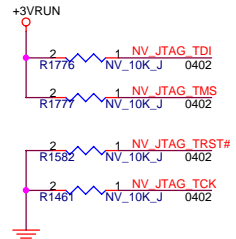
FAB: TV Mode Strap no use, remove.  
(MIOAD7, MIOAD10, MIOBD6)







	I/O	Inter pull low	GPIO TABLE
GPIO0	I	Yes	HDMI Hot Plug Detect 0 (HPD0)
GPIO1	I	Yes	Hot Plug Detect 1 (HPD1)
GPIO2	O	Yes	Panel Brightness (PWM) <b>Active High</b>
GPIO3	O	No	Panel Power Enable <b>Active Low</b>
GPIO4	O	Yes	Panel Backlight On/Off <b>Active High</b>
GPIO5	O	Yes	NV_VDD VID0
GPIO6	O	Yes	NV_VDD VID1
GPIO7	O	Yes	FB_VDD VID0
GPIO8	OD	No	THERM <b>Active Low</b>
GPIO9	OD	No	ALERT <b>Active Low</b>
GPIO10	O	No	TMDS LINK SELECT
GPIO11	O	NC(Low)	CEC no function yet
GPIO12	I	--	AC/BATT#



SPREAD SPECTRUM SETTING FOR MK

S0	SPREAD	Spread
	DIRECTION	Percentage(%)
0	DOWN	-1.8
M	DOWN	-0.6
1	DOWN	-2.5

SPREAD SPECTRUM SETTING FOR P1819B

SRS	SPREAD	Spread
PIN3	DIRECTION	Percentage(%)
0	DOWN	-1.25
1	DOWN	-1.75

0 = connect to GND  
M = unconnected  
1 = connect directly to VDD

nVidia support Down -1.25%

Tis chip can use MK1726 or P1819B

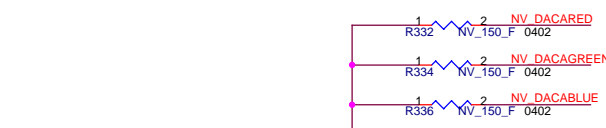
R316 place near GPU  
R317 place near spectrum chip

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

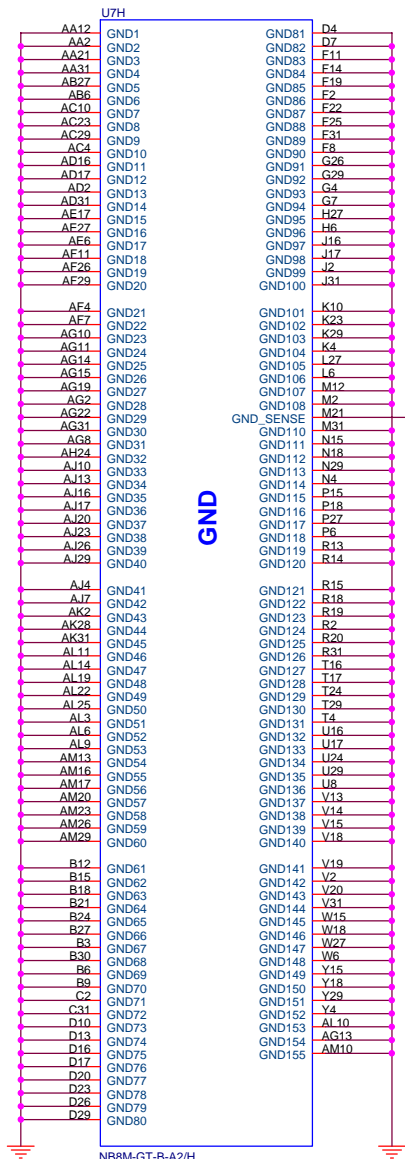
Title: **VGA(MULTIUSE)**

Size: A3  
Document Number: MS90-1-01  
Rev: 1.3

Date: Tuesday, March 27, 2007 | Sheet: 20 of 72

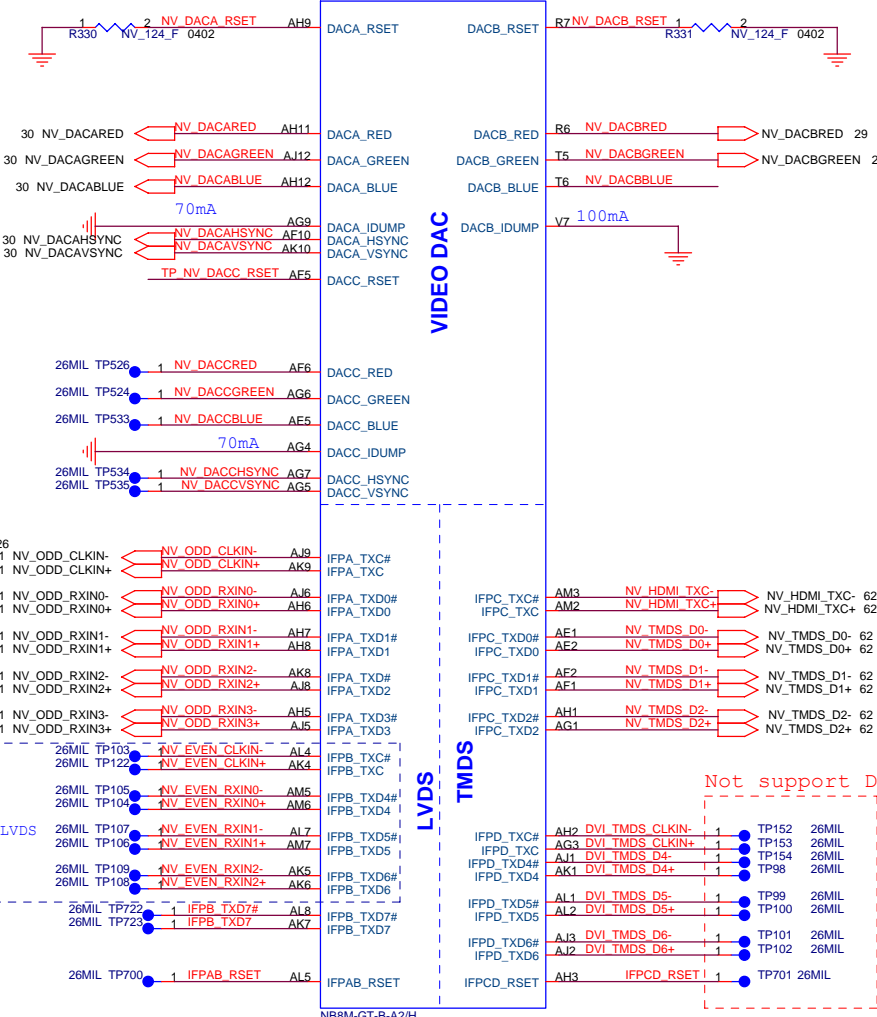


CLOSE TO GPU

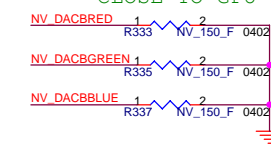


GND

Only support one channel



CLOSE TO GPU



DACA	VGA-CRT	I2CA
DACA-RED	R	
DACA-GREEN	G	
DACA-BLUE	B	
DACA-HSYNC	HSYNC	
DACA-VSYNC	VSYNC	
	VGA-DCLK	SCL
	VGA-DDATA	SDA

DACB	S-VIDEO
DACB-RED	C
DACB-GREEN	
DACB-BLUE	Y

Not support DVI

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 Title **VGA(LVD/DAC)** CCPBG - R&D Division  
 Size A3 Document Number MS90-1-01 Rev 1.1  
 Date: Tuesday, March 27, 2007 Sheet 21 of 72

+1\_8VRUN

+1\_8VRUN

+1\_8VRUN

+1\_8VRUN

U12  
Mirror function on

A2 VDD1  
A11 VDD2  
F1 VDD3  
F12 VDD4  
M1 VDD5  
M12 VDD6  
V2 VDD7  
V11 VDD8  
K1 VDD9  
K12 VDD10

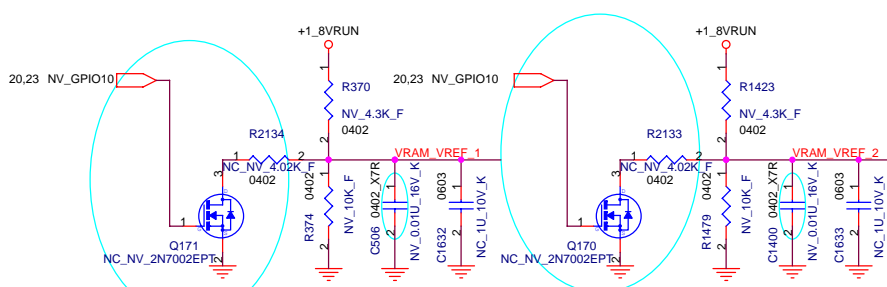
FBAD23 T3 DO31  
FBAD22 T2 DO30  
FBAD19 R3 DO29  
FBAD21 R2 DO28  
FBAD16 M3 DO27  
FBAD18 N2 DO26  
FBAD17 L3 DO25  
FBAD20 M2 DO24  
FBAD29 T10 DO23  
FBAD26 T11 DO22  
FBAD30 R10 DO21  
FBAD31 R11 DO20  
FBAD25 M10 DO19  
FBAD28 N11 DO18  
FBAD27 L10 DO17  
FBAD24 M11 DO16  
FBAD4 G10 DO15  
FBAD7 F11 DO14  
FBAD6 F10 DO13  
FBAD5 E11 DO12  
FBAD2 C10 DO11  
FBAD3 C11 DO10  
FBAD0 B10 DO9  
FBAD1 B11 DO8  
FBAD12 C3 DO7  
FBAD10 F2 DO6  
FBAD13 F3 DO5  
FBAD14 E2 DO4  
FBAD15 C2 DO3  
FBAD11 C2 DO2  
FBAD8 B3 DO1  
FBAD9 B2 DO0

U11 ZQ A4  
VSS01 NV\_SSD01  
VSS02 NV\_SSD02  
VSS03 NV\_SSD03  
VSS04 NV\_SSD04  
VSS05 NV\_SSD05  
VSS06 NV\_SSD06  
VSS07 NV\_SSD07  
VSS08 NV\_SSD08  
VSS09 NV\_SSD09  
VSS10 NV\_SSD10  
VSS01 NV\_SSD01  
VSS02 NV\_SSD02  
VSS03 NV\_SSD03  
VSS04 NV\_SSD04  
VSS05 NV\_SSD05  
VSS06 NV\_SSD06  
VSS07 NV\_SSD07  
VSS08 NV\_SSD08  
VSS09 NV\_SSD09  
VSS10 NV\_SSD10

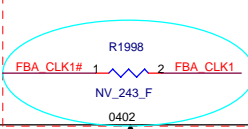
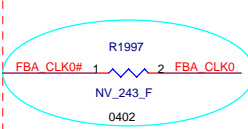
R1690 (120 ohm-360 ohm)  
240 ohm --> Output impedance 40 ohm

FAE: Remove termination resistor for A2,A3,A4,A5  
Remove 16M/8M selection strap.

VRAM\_VREF is 70%FBVDDQ for GDDR3 1.26V



7/19 FAE Suggest: Ball to termination resistor trace length < 75ps

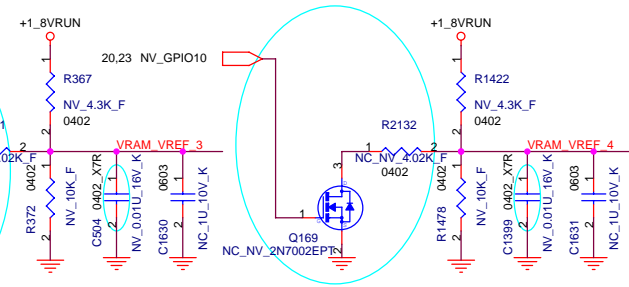


A2 VDD1  
A11 VDD2  
F1 VDD3  
F12 VDD4  
M1 VDD5  
M12 VDD6  
V2 VDD7  
V11 VDD8  
K1 VDD9  
K12 VDD10

FBAD56 T3 DO31  
FBAD58 T2 DO30  
FBAD59 R3 DO29  
FBAD60 R2 DO28  
FBAD63 M3 DO27  
FBAD62 N2 DO26  
FBAD61 L3 DO25  
FBAD57 M2 DO24  
FBAD47 T10 DO23  
FBAD40 T11 DO22  
FBAD46 R10 DO21  
FBAD45 R11 DO20  
FBAD44 M10 DO19  
FBAD42 N11 DO18  
FBAD43 L10 DO17  
FBAD41 M11 DO16  
FBAD50 G10 DO15  
FBAD49 F11 DO14  
FBAD48 F10 DO13  
FBAD51 E11 DO12  
FBAD52 C10 DO11  
FBAD53 C11 DO10  
FBAD55 B10 DO9  
FBAD54 B11 DO8  
FBAD33 C3 DO7  
FBAD34 E2 DO6  
FBAD32 F3 DO5  
FBAD35 E2 DO4  
FBAD39 C3 DO3  
FBAD36 C2 DO2  
FBAD38 B3 DO1  
FBAD37 B2 DO0

U12 ZQ A4  
VSS01 NV\_SSD01  
VSS02 NV\_SSD02  
VSS03 NV\_SSD03  
VSS04 NV\_SSD04  
VSS05 NV\_SSD05  
VSS06 NV\_SSD06  
VSS07 NV\_SSD07  
VSS08 NV\_SSD08  
VSS09 NV\_SSD09  
VSS10 NV\_SSD10  
VSS01 NV\_SSD01  
VSS02 NV\_SSD02  
VSS03 NV\_SSD03  
VSS04 NV\_SSD04  
VSS05 NV\_SSD05  
VSS06 NV\_SSD06  
VSS07 NV\_SSD07  
VSS08 NV\_SSD08  
VSS09 NV\_SSD09  
VSS10 NV\_SSD10

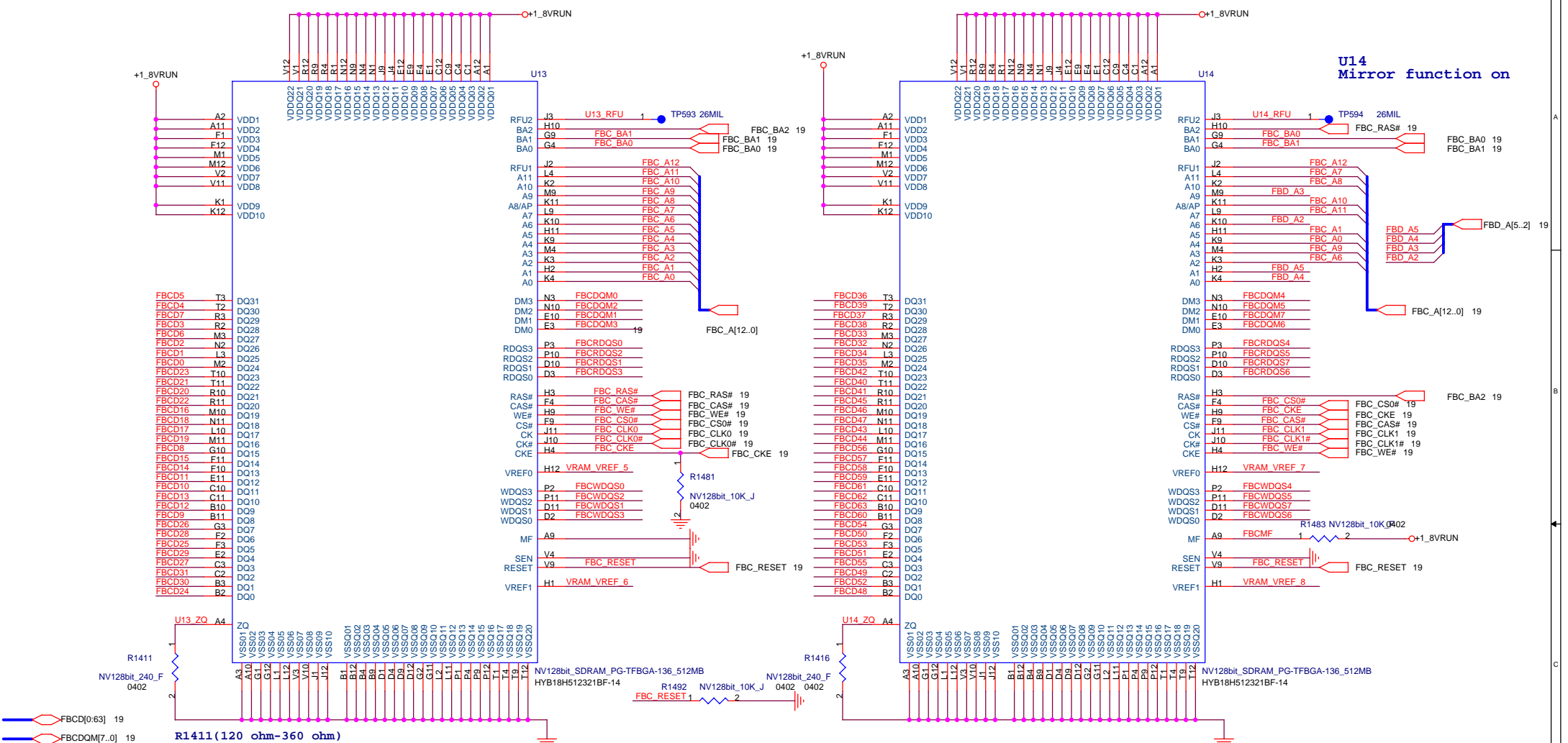
R1700 (120 ohm-360 ohm)  
240 ohm --> Output impedance 40 ohm



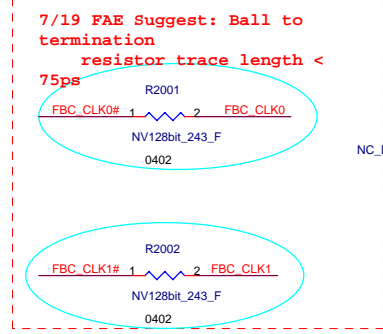
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		CCPBG - R&D Division	
<b>Title VRAM(GDDR)# 1/2</b>			
Size A3	Document Number MS90-1-01	Rev 1.2	
Date: Tuesday, March 27, 2007	Sheet 22	of 72	



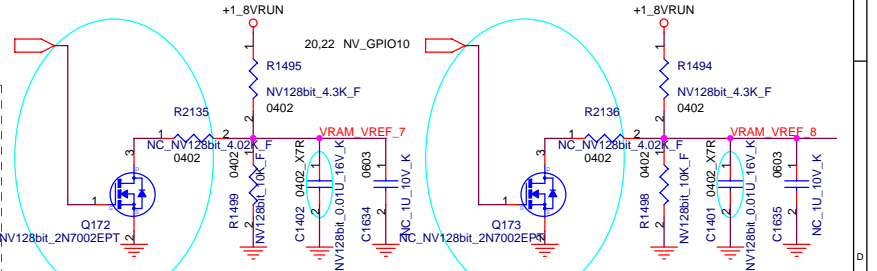
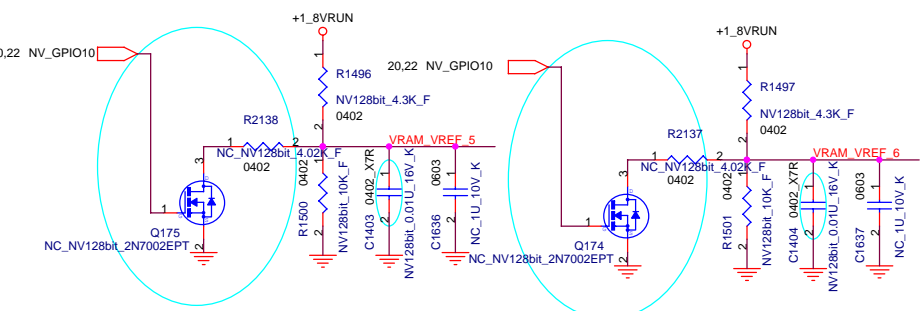
**U14 Mirror function on**

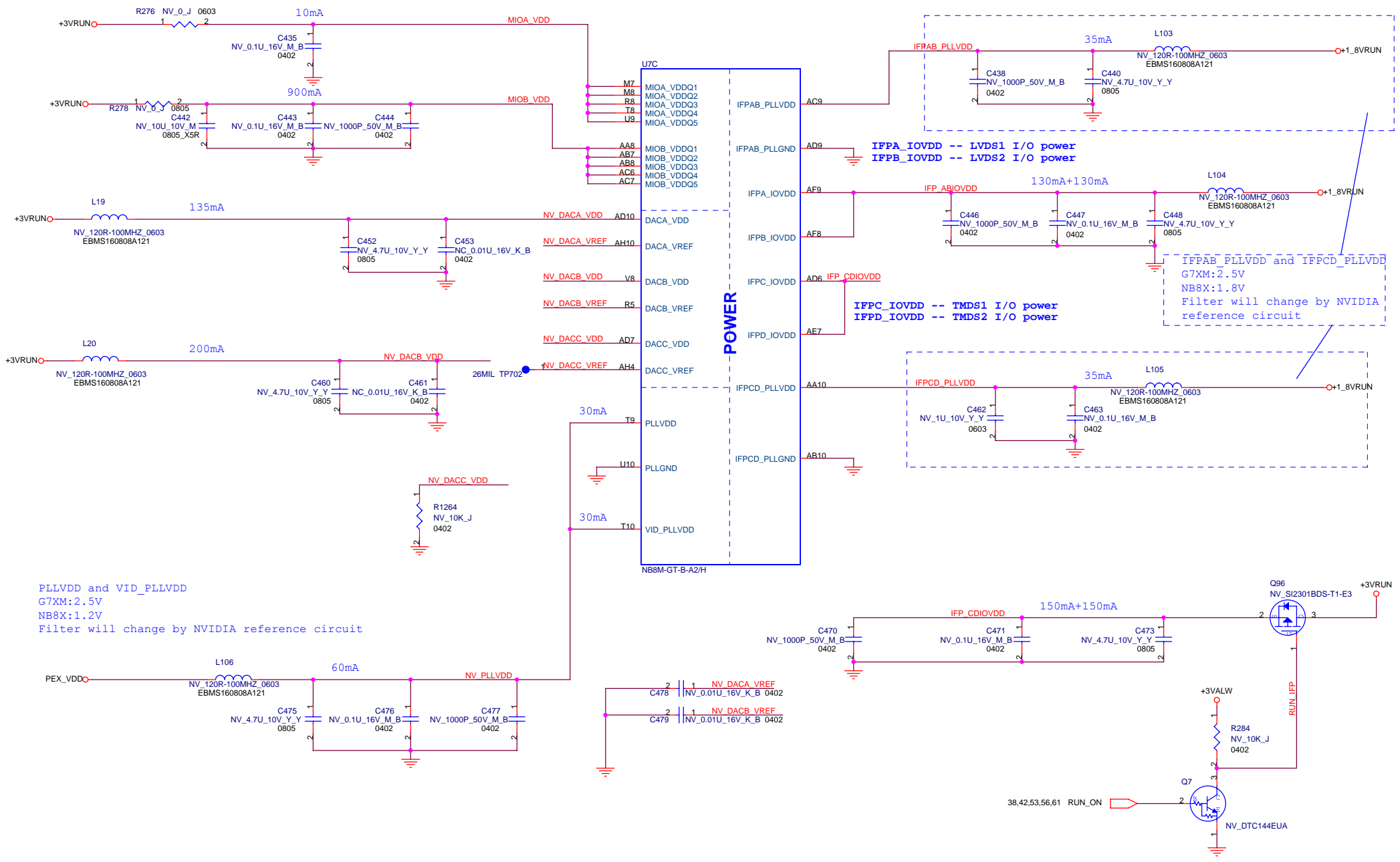


**FAB: Remove termination resistor for A2,A3,A4,A5  
Remove 16M/8M selection strap.**



**VRAM\_VREF is 70%FBVDDQ for GDDR3 1.26V**

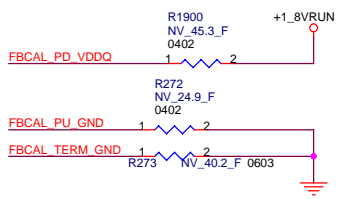
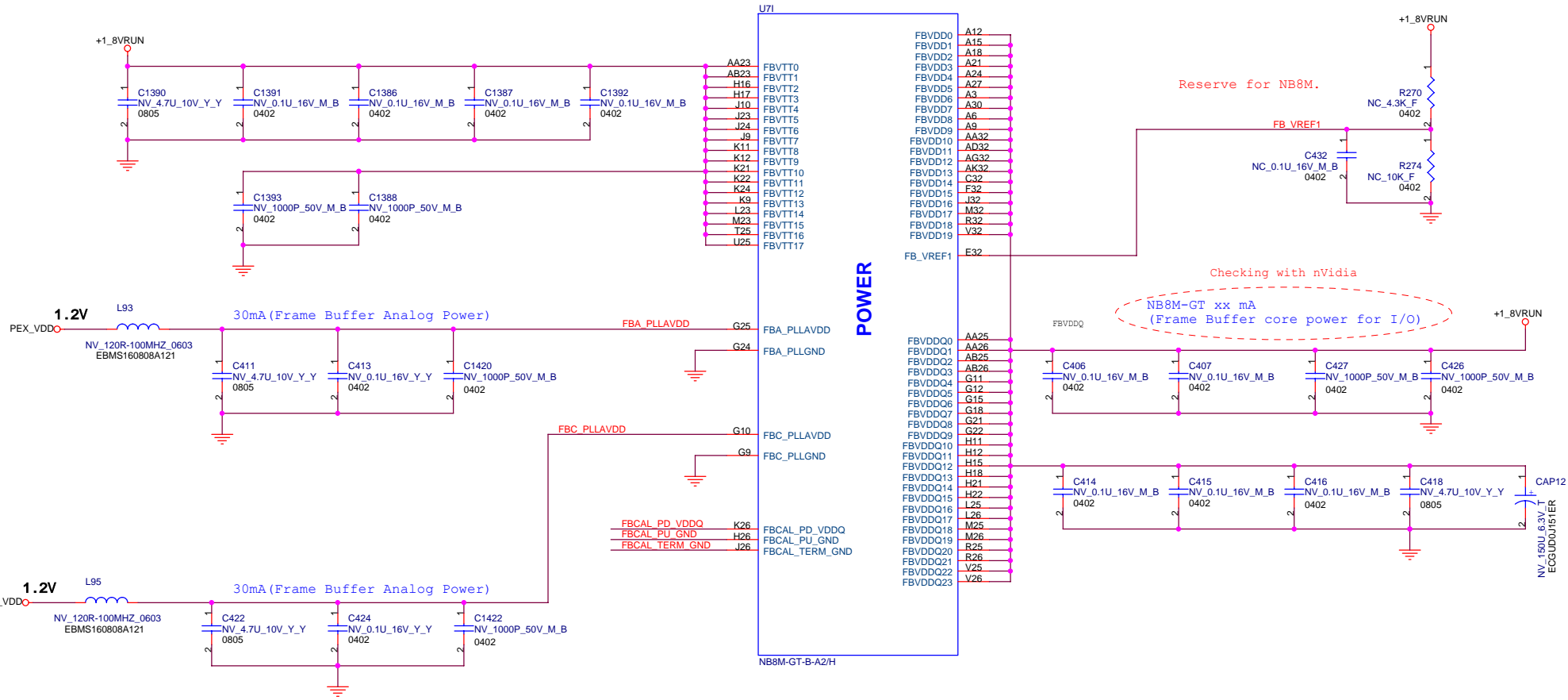




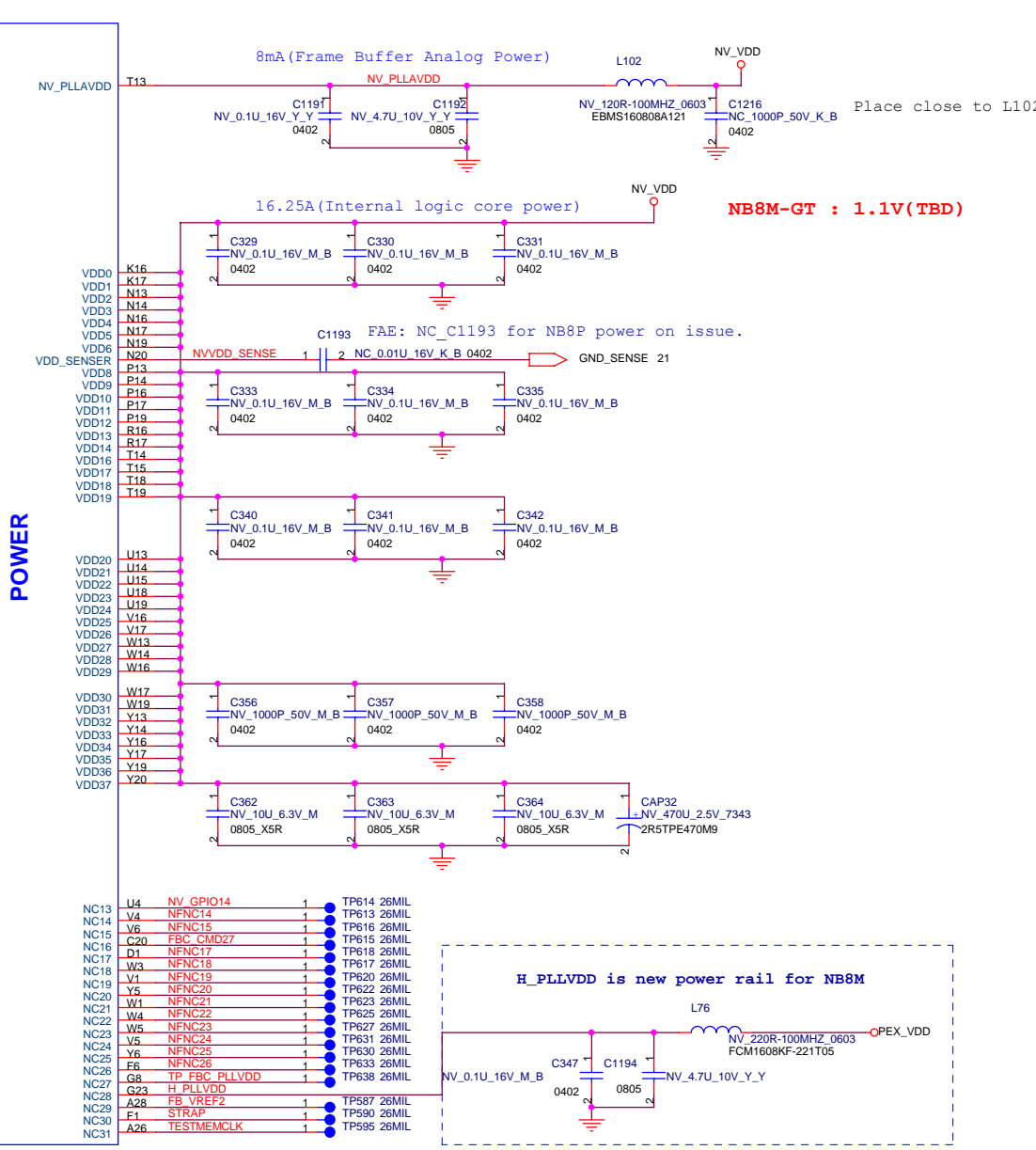
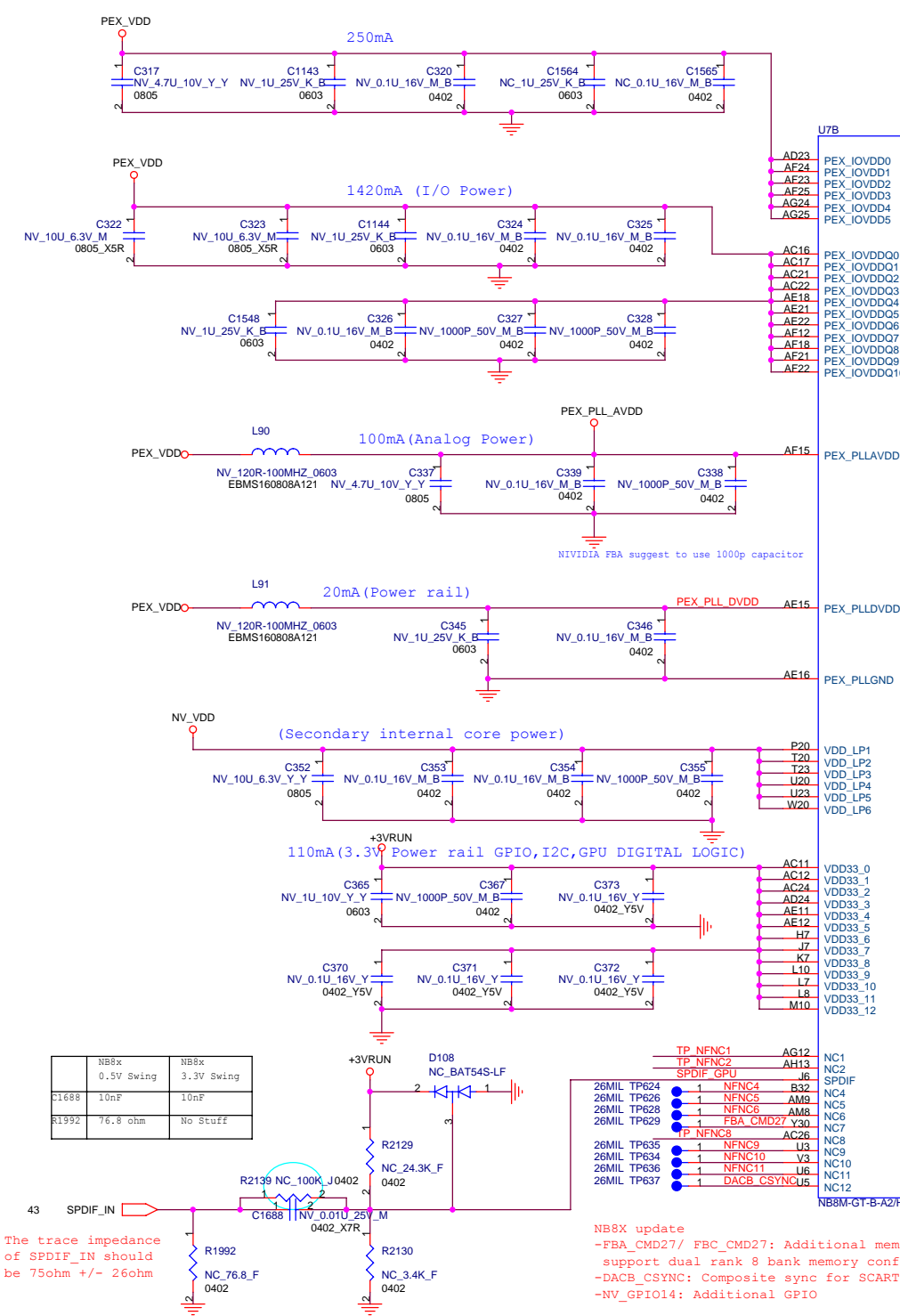
PLLVDD and VID\_PLLVDD  
 G7XM:2.5V  
 NB8X:1.2V  
 Filter will change by NVIDIA reference circuit

IFPAB\_PLLVDD and IFPCD\_PLLVDD  
 G7XM:2.5V  
 NB8X:1.8V  
 Filter will change by NVIDIA reference circuit

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	<b>VGA(POWER) 1/3</b>		
Size	Document Number	Rev	
A3	MS90-1-01	1.1	
Date:	Tuesday, March 27, 2007	Sheet	24 of 72



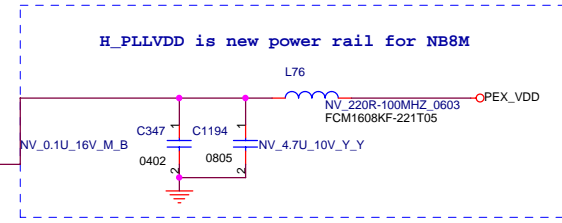
	GDDR3/BGA136
FBCAL_PD_VDDQ	45.3 ohm
FBCAL_PU_GND	24.9 ohm
FBCAL_TERM_GND	40.2 ohm

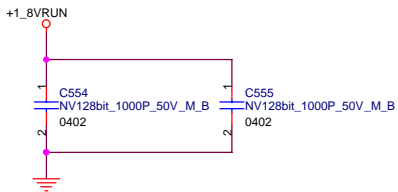
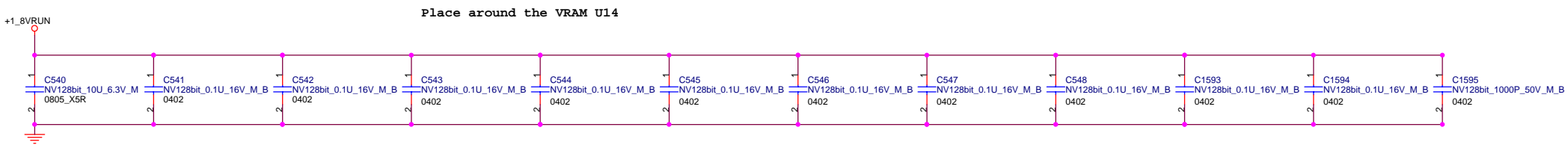
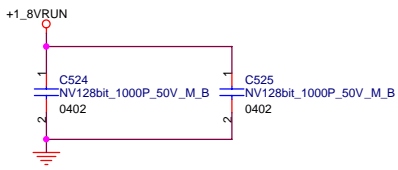
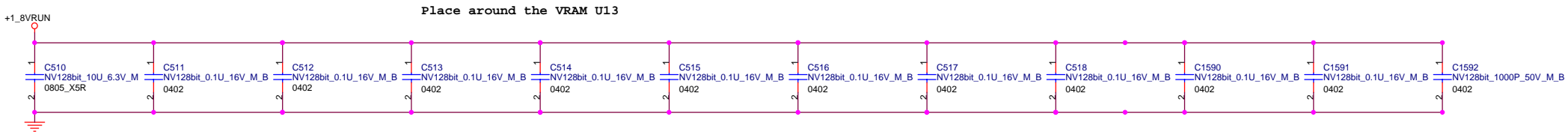


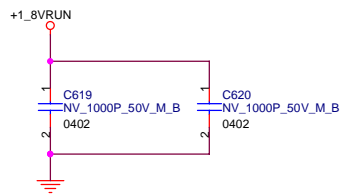
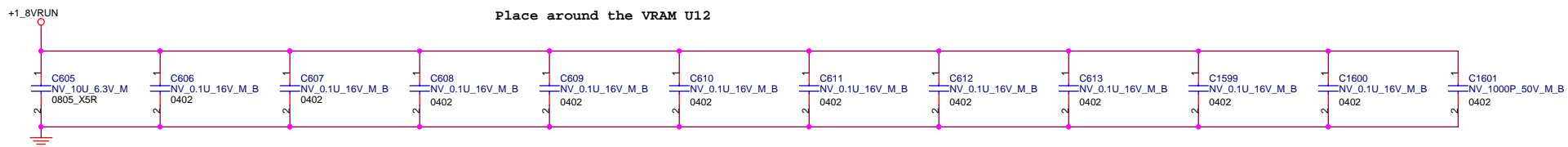
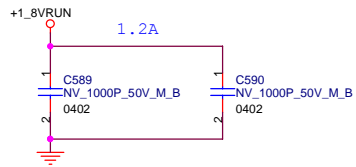
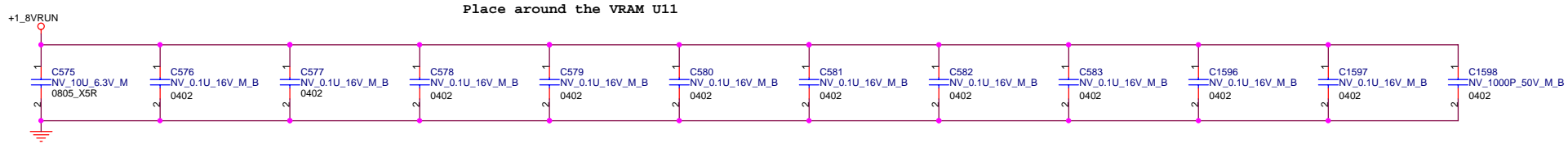
	NB8x 0.5V Swing	NB8x 3.3V Swing
C1688	10nF	10nF
R1992	76.8 ohm	No Stuff

The trace impedance of SPDIF\_IN should be 75ohm +/- 26ohm

**NB8X update**  
 -FBA\_CMD27/ FBC\_CMD27: Additional memory address bit to support dual rank 8 bank memory configuration.  
 -DACB\_CSYNCSU5: Composite sync for SCART support  
 -NV\_GPIO14: Additional GPIO

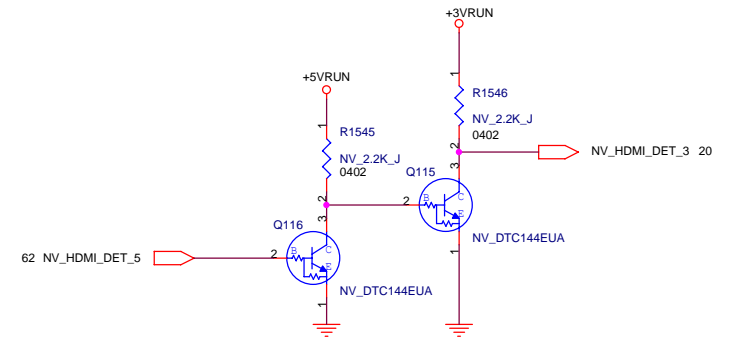
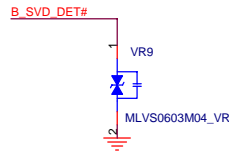
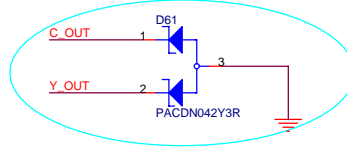
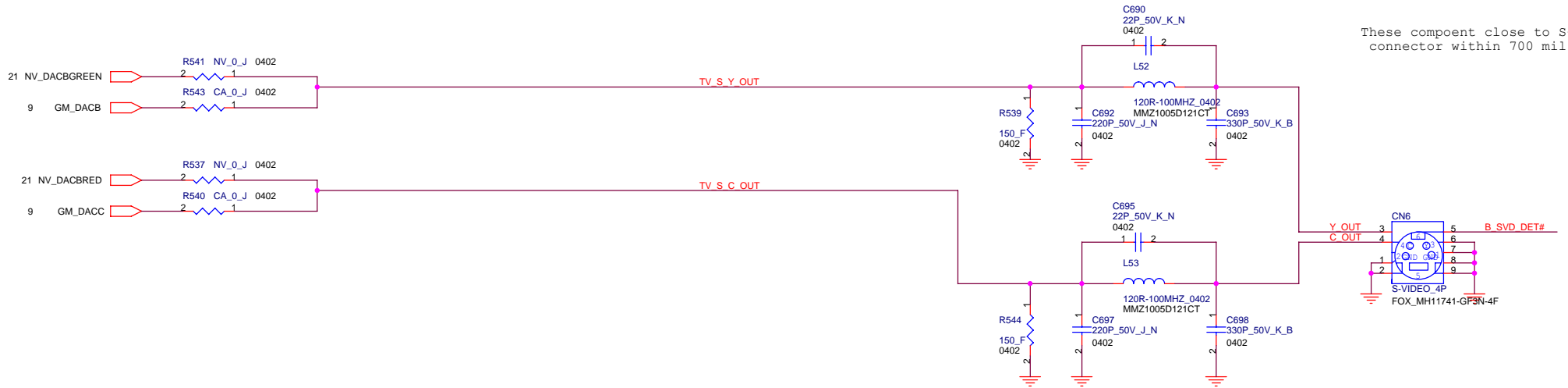




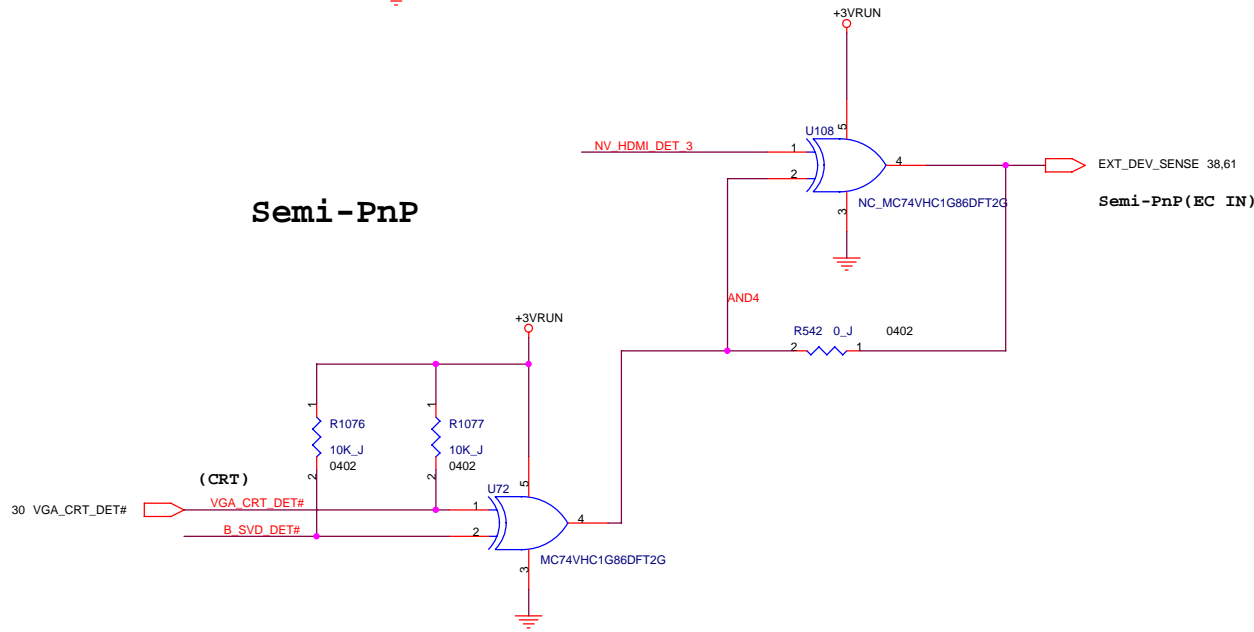


# S-VIDEO

These component close to S-Video connector within 700 mil

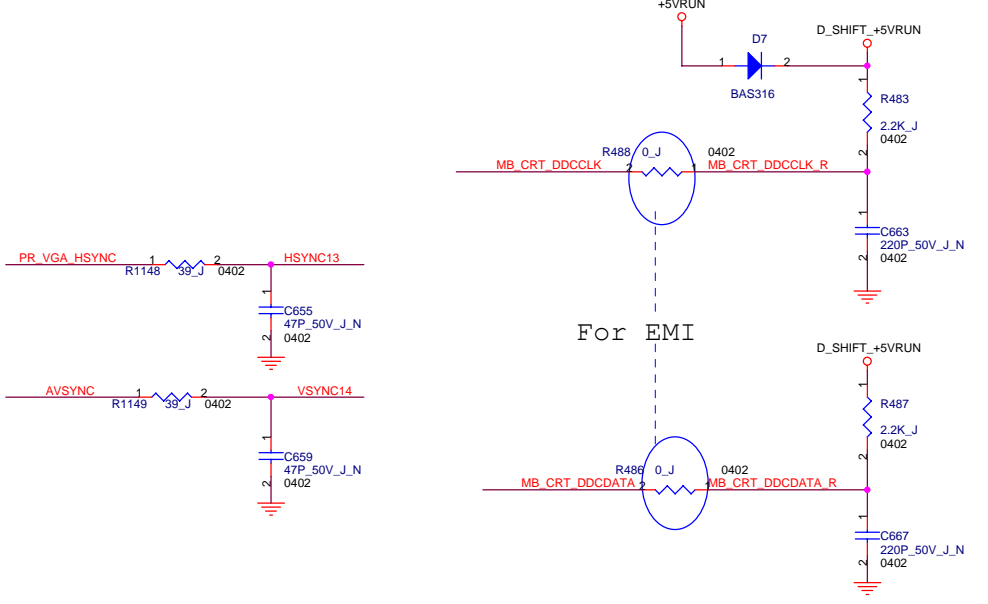
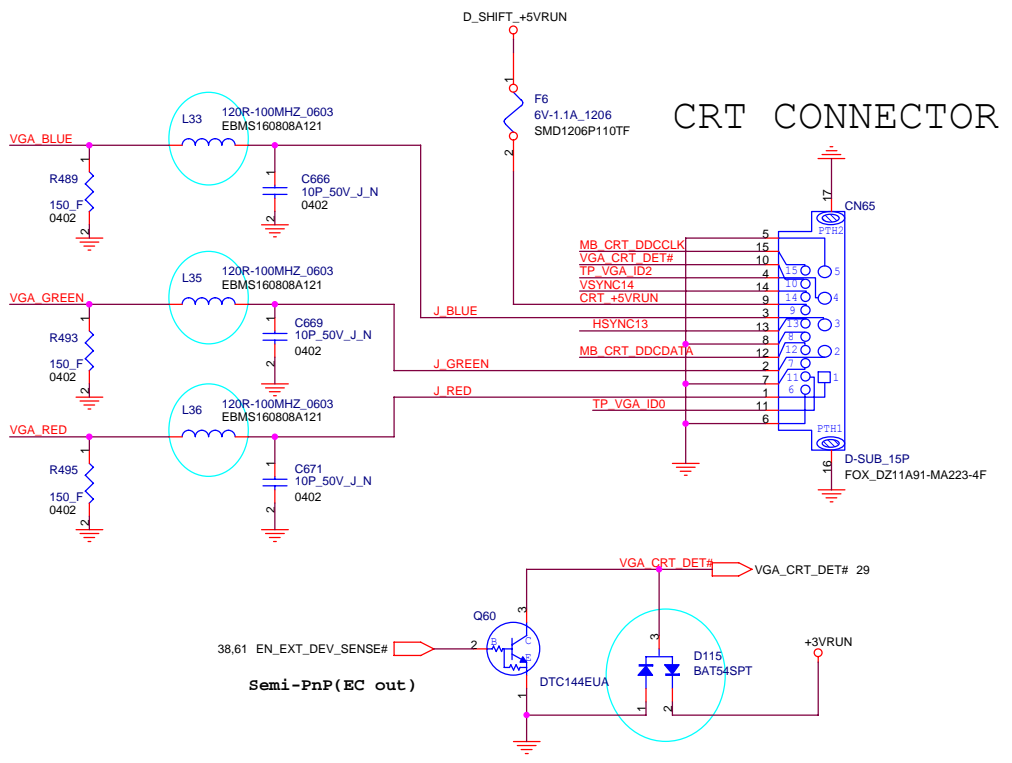
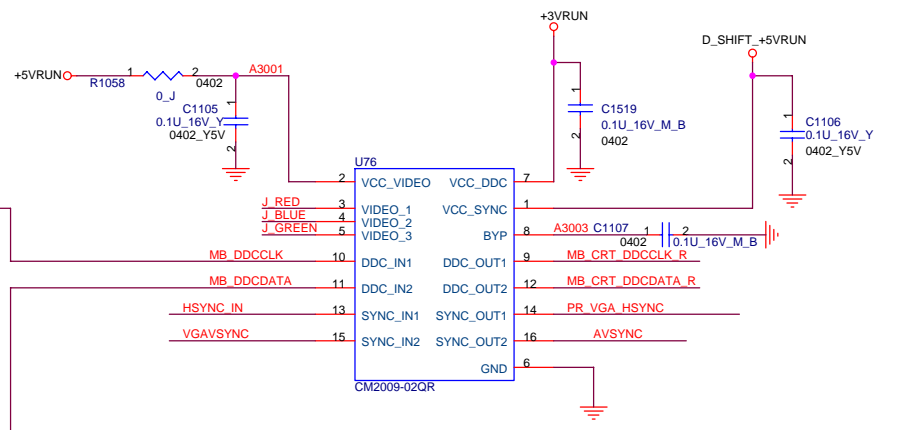
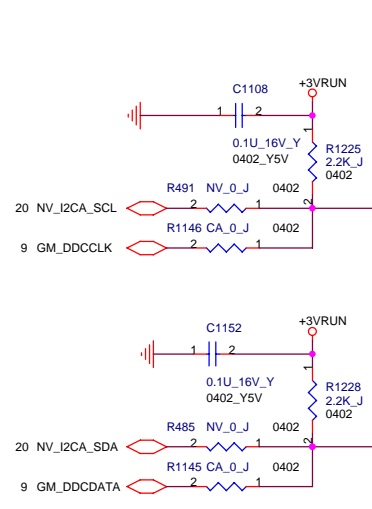
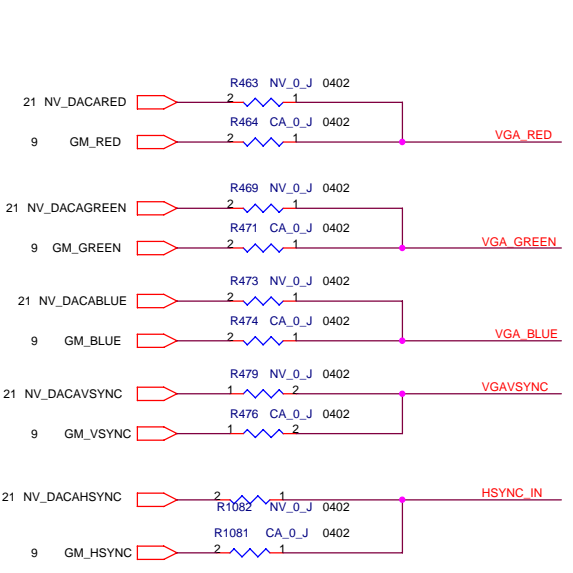


## Semi-PnP



<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	TWIn and OUT/Semi-PnP#		
Size	Document Number	Rev	
A3	MS90-1-01	1.1	
Date:	Tuesday, March 27, 2007	Sheet	29 of 72





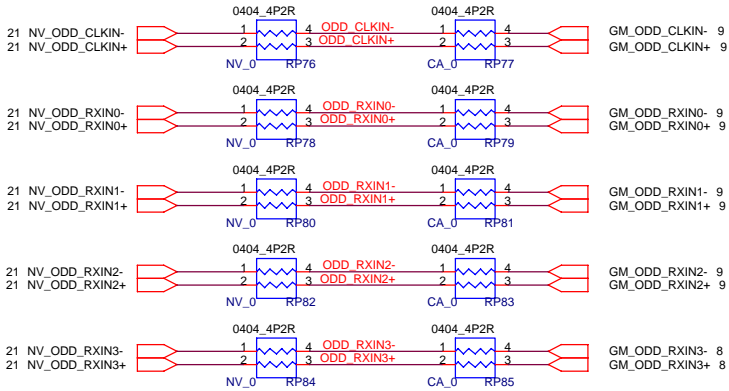
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division			
Title	CRT		
Size	Document Number	Rev	
A3	MS90-1-01	1.2	
Date:	Tuesday, March 27, 2007	Sheet	30 of 72

Group1, Group2 should be close

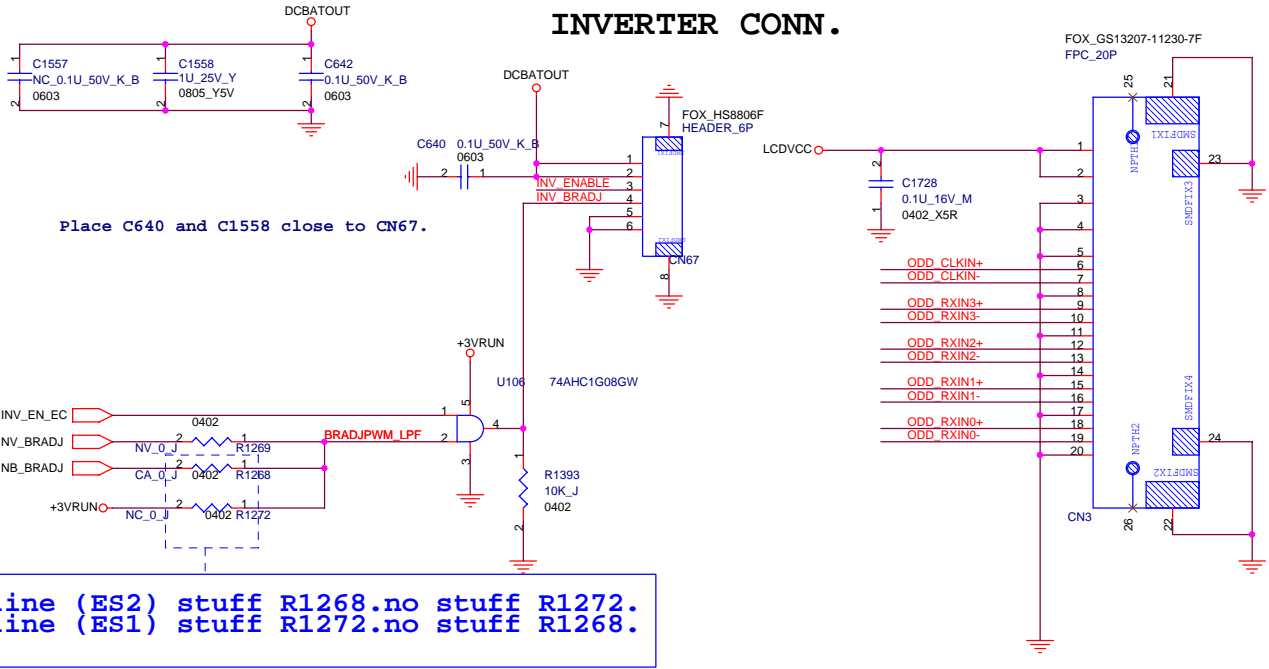
# LVDS

## Group1

## Group2

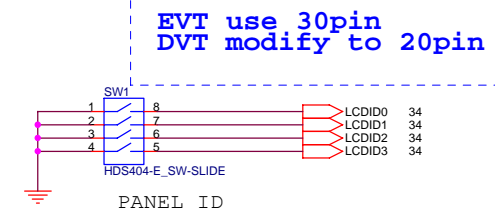


# INVERTER CONN.



Crestline (ES2) stuff R1268.no stuff R1272.  
Crestline (ES1) stuff R1272.no stuff R1268.

# LVDS CONNECTOR



Type	WXGA	WXGA	WXGA	WXGA
Size	15.4"W	15.4"W	15.4"W	15.4"W
Vender	Samsung (2 lamp)	CPT (1 lamp)	AUO (2 lamp)	AUO (1 lamp)
Device Name	LTN154XB-L01	CLAA154WA05AN	B154EW07	QD15TL07
Panel ID [2..0]	001	101	010	100

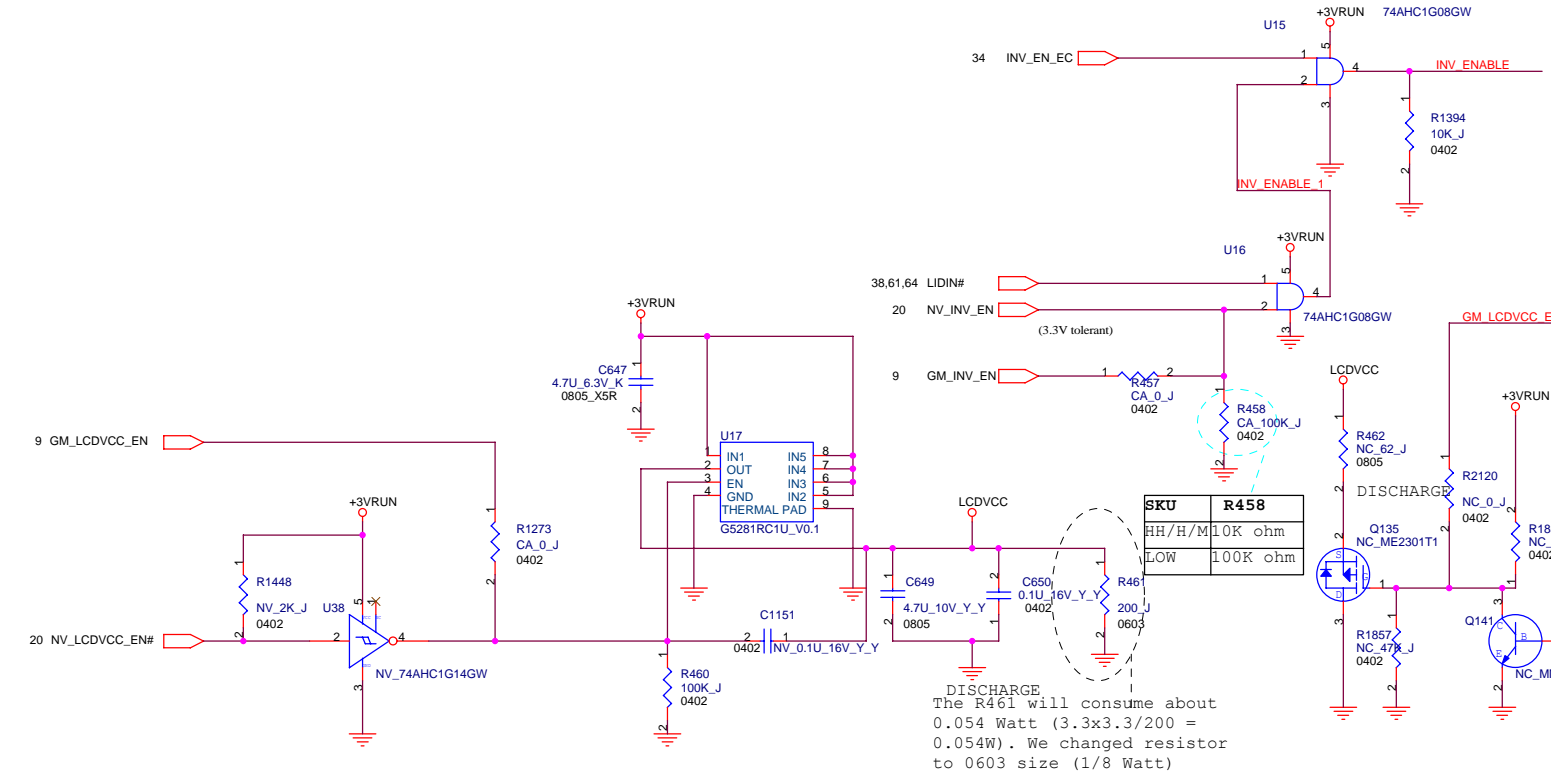
LCDID3 is for InstantOn switch  
Enable: 0  
Disable: 1

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

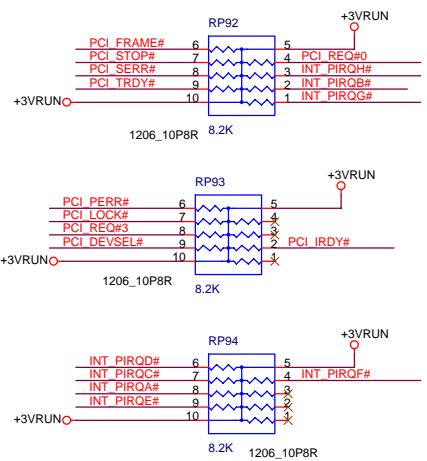
Title: **LVDS**

Size: A3 Document Number: MS90-1-01 Rev: 1.1

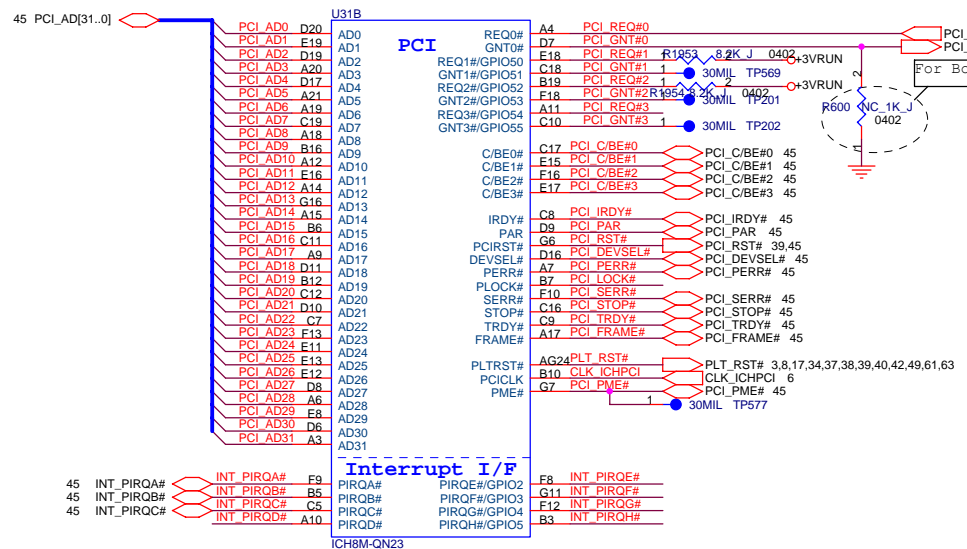
Date: Tuesday, March 27, 2007 Sheet: 31 of 72



DISCHARGE  
The R461 will consume about  
0.054 Watt (3.3x3.3/200 =  
0.054W). We changed resistor  
to 0603 size (1/8 Watt)

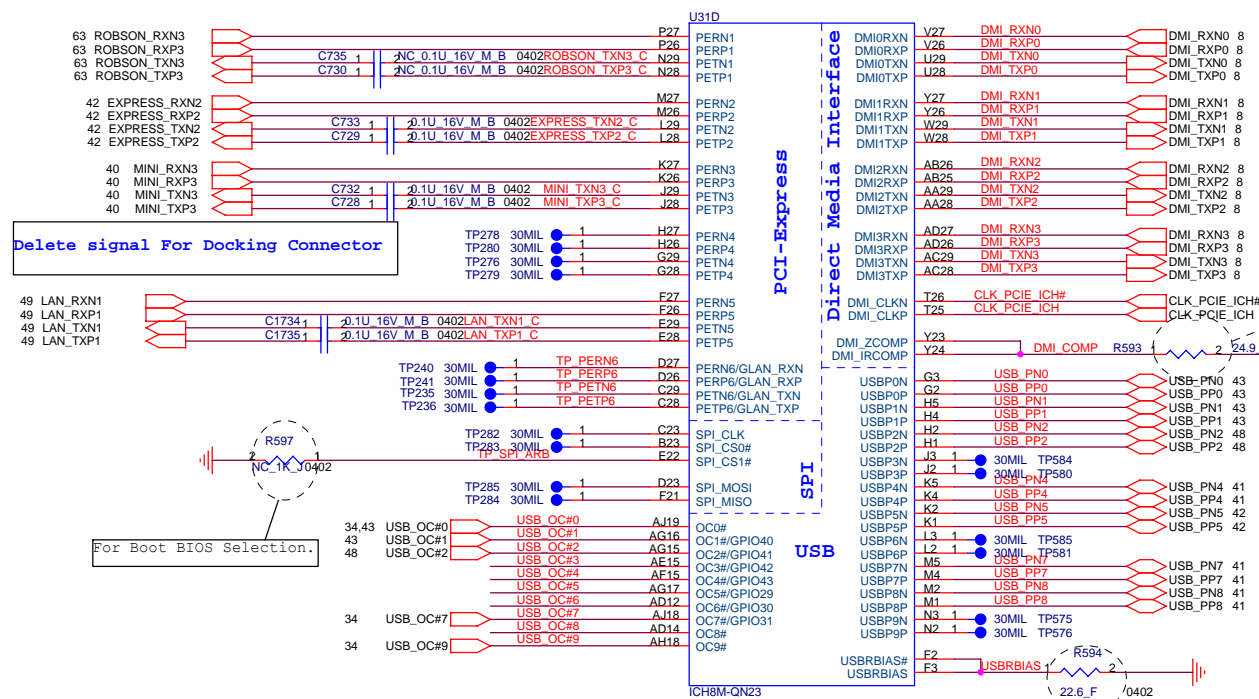


PCI Pullups



Strap for Boot-BIOS

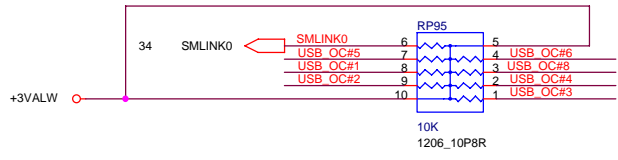
	GNT0#	SPI_CS1#
LPC (Default)	Hi	Hi
PCI	Hi	LOW
SPI	LOW	Hi



Delete signal For Docking Connector

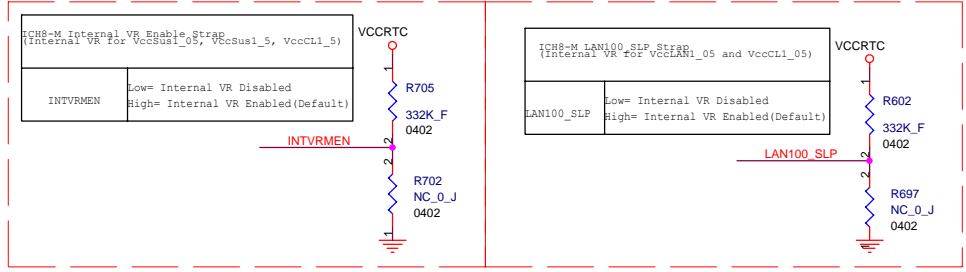
Place within 500 mils of ICH

Place within 500 mils of ICH and don't routing next to high speed signals





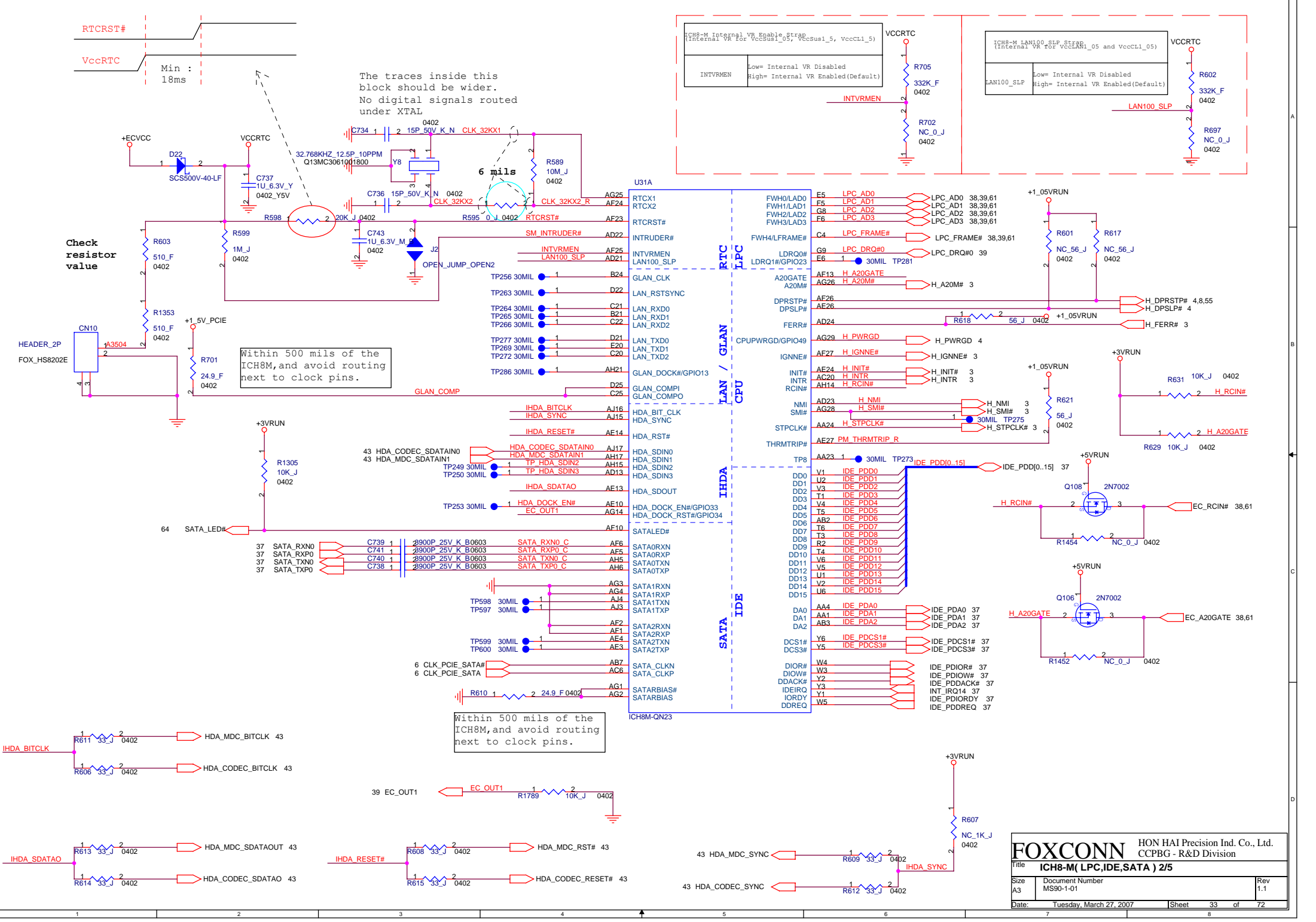
The traces inside this block should be wider. No digital signals routed under XTAL



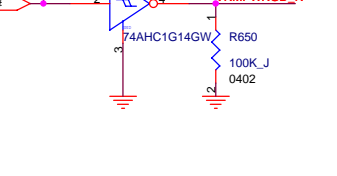
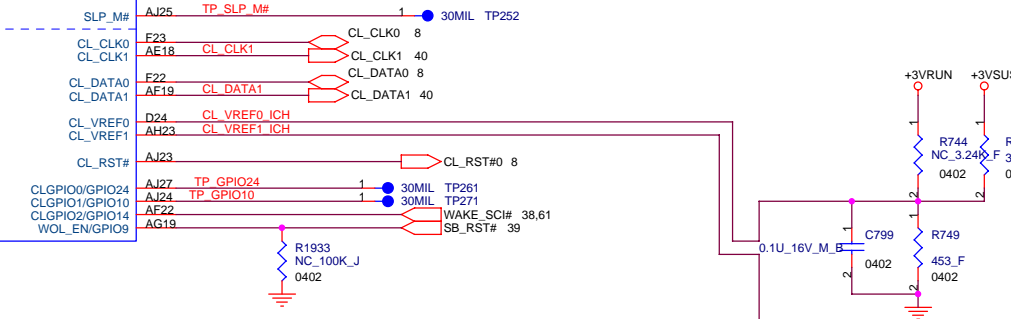
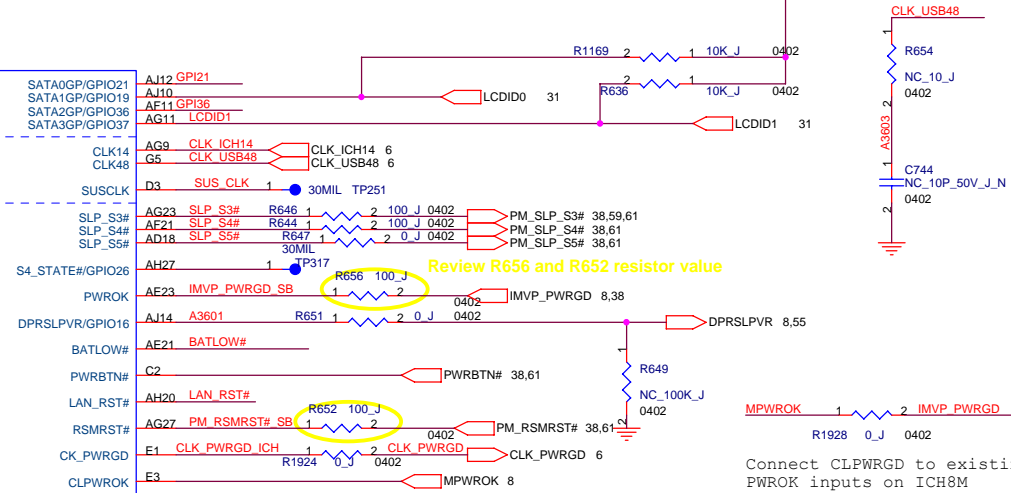
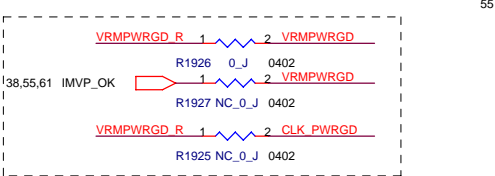
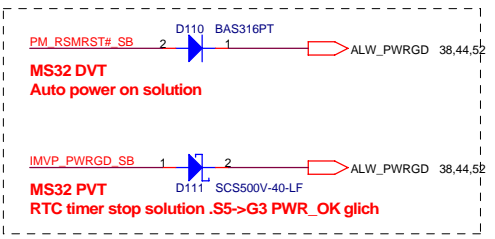
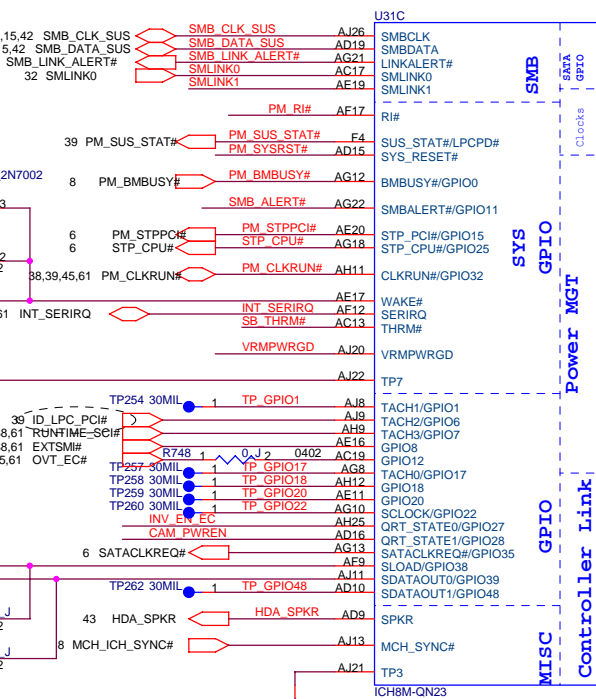
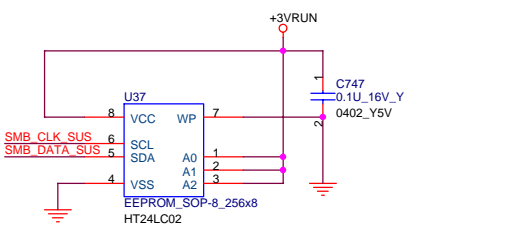
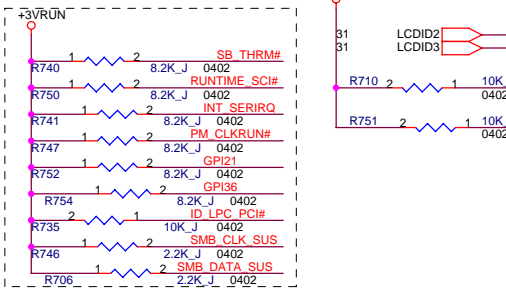
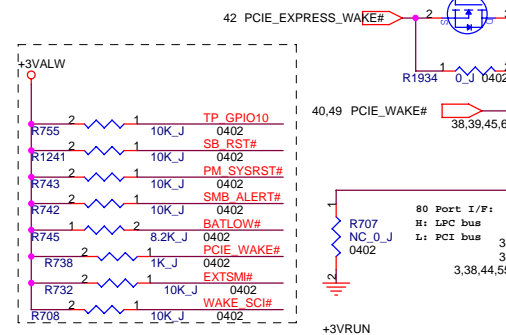
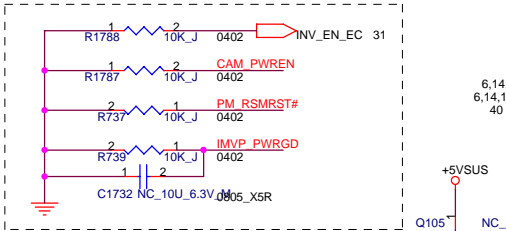
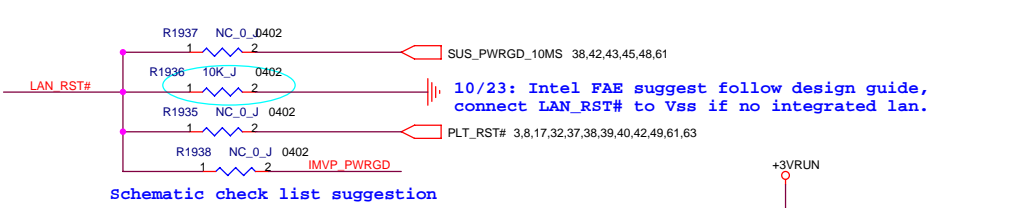
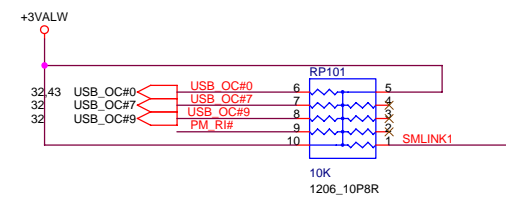
Check resistor value

Within 500 mils of the ICH8M, and avoid routing next to clock pins.

Within 500 mils of the ICH8M, and avoid routing next to clock pins.

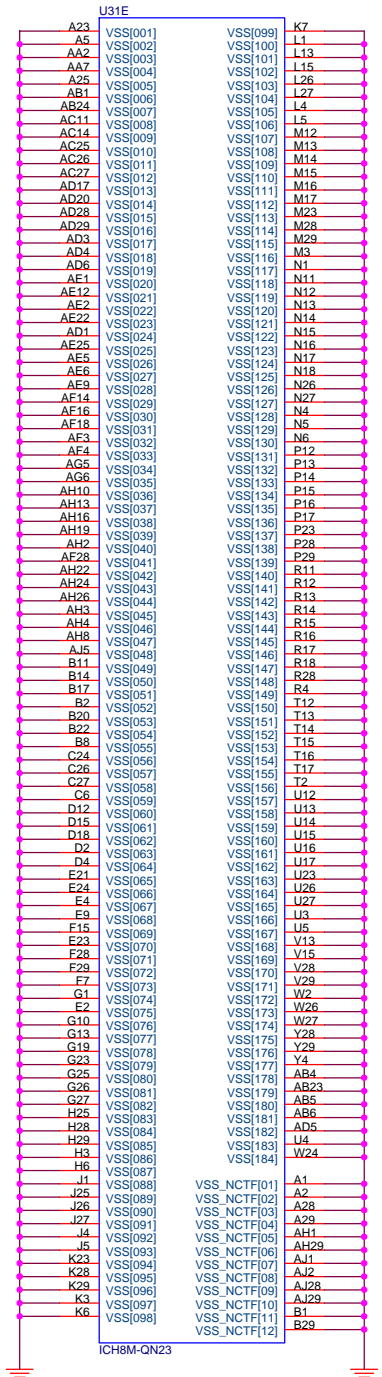


<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title: <b>ICH8-M(LPC,IDE,SATA) 2/5</b>			
Size: A3	Document Number: MS90-1-01	Rev: 1.1	
Date: Tuesday, March 27, 2007		Sheet: 33	of: 72











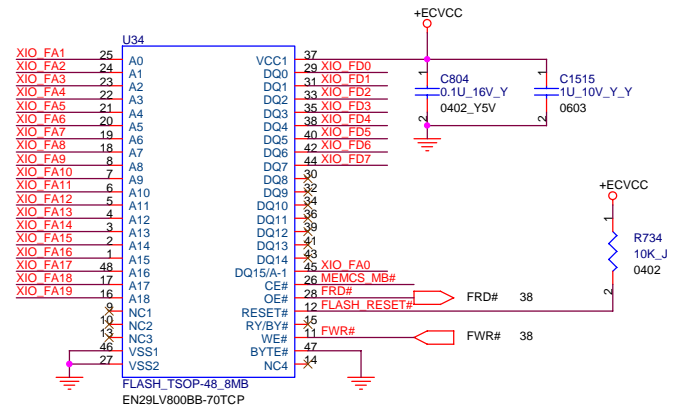
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>ICH8-M( GND) 5/5</b>			
Size A3	Document Number MS90-1-01		Rev 1.1
Date: Tuesday, March 27, 2007	Sheet 36	of 72	



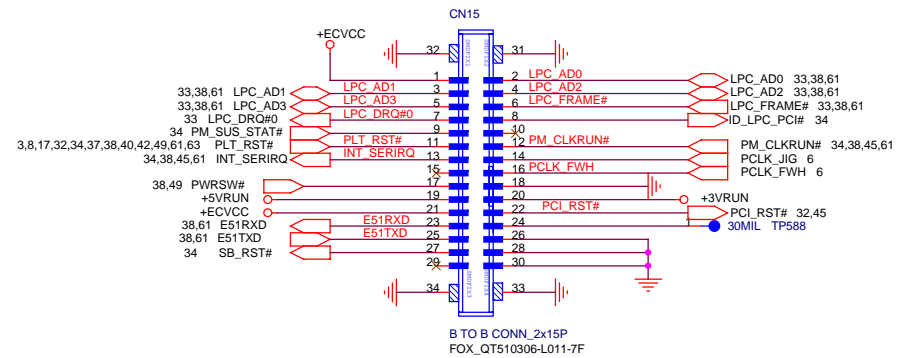




38 XIO\_FA[19..0]   
 38 XIO\_FD[7..0] 

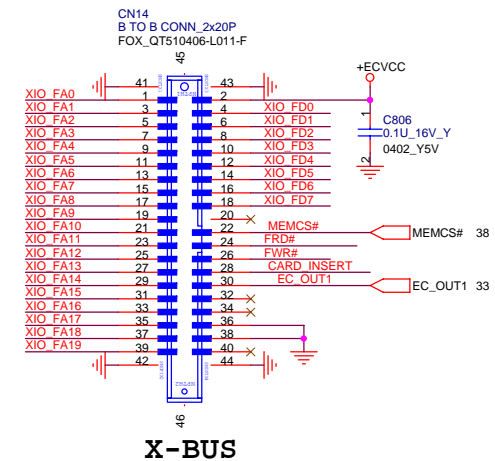


### FLASH BIOS



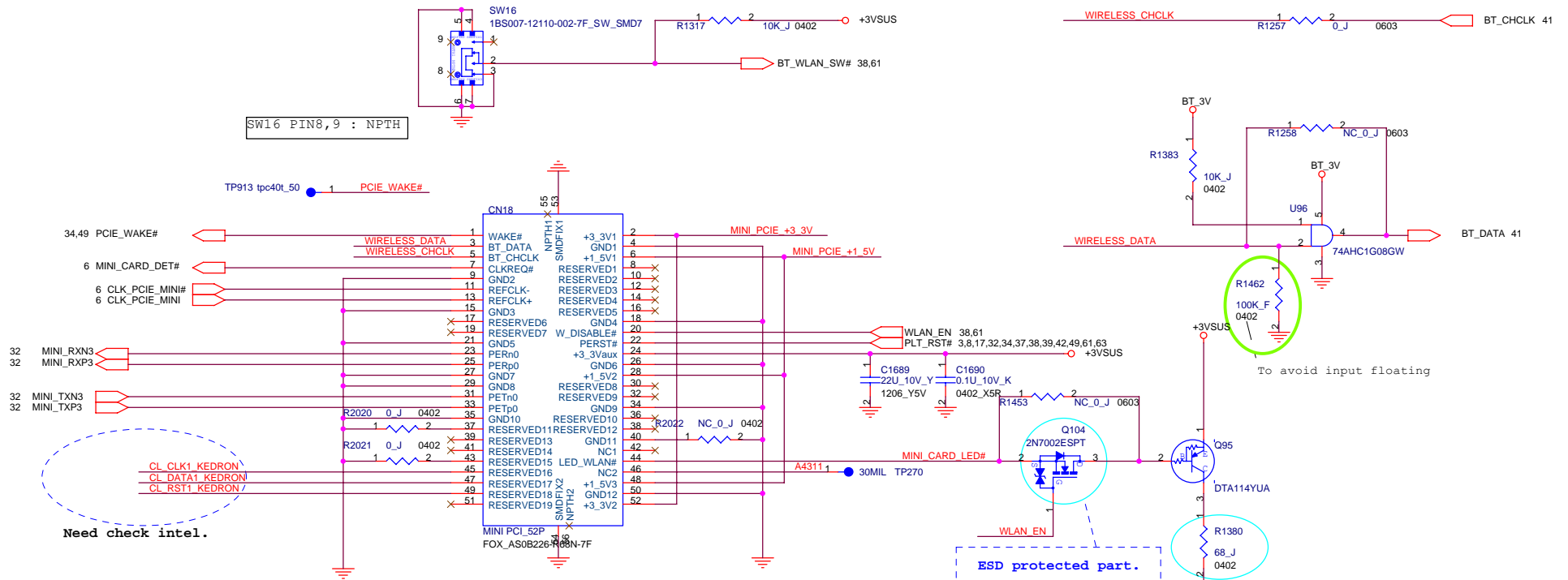
### JIG-120

Pin 18 of JIG-120 is useless in debug board,  
 so we let pin 18 NC.



### X-BUS

# WLAN Switch



SW16\_PIN8,9 : NPTH

TP913 ipc40t\_50 1 PCIE\_WAKE#

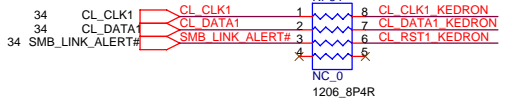
To avoid input floating

LED IF SPEC:  
20mA (TYP) , 30mA (MAX)

Green

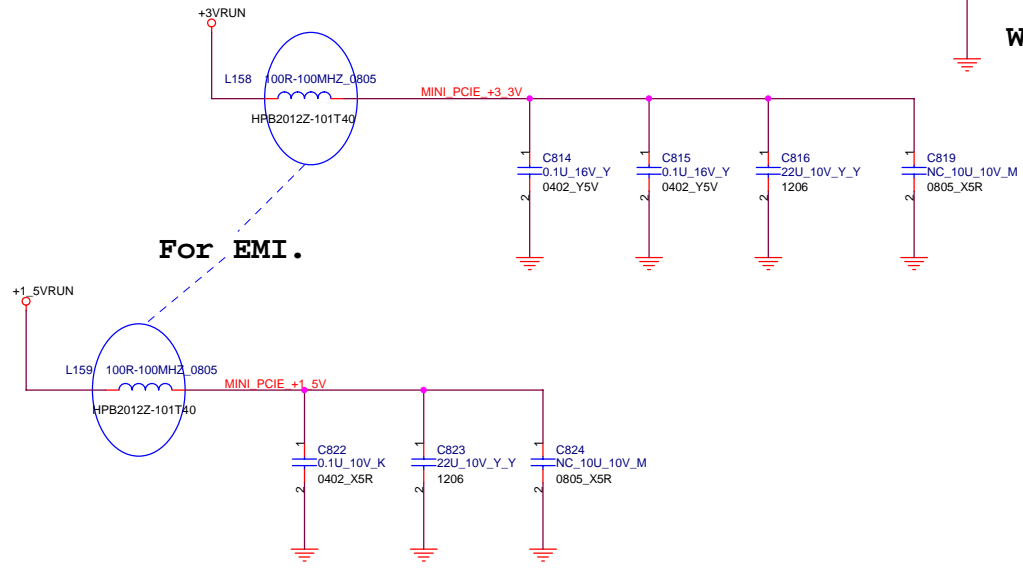
WLAN LED.

## Mini Card. WLAN

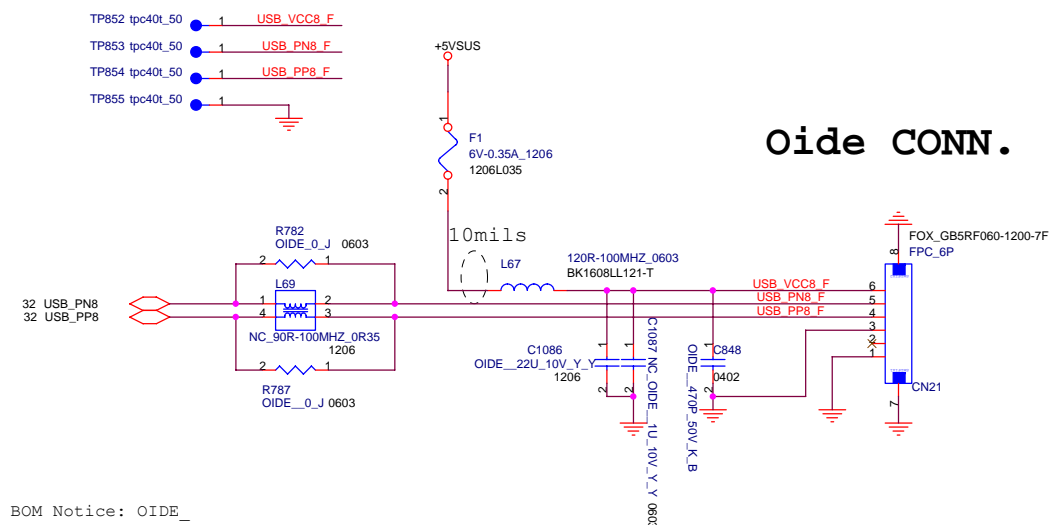


For EMI.

+1\_5V=>0.5A  
+3\_3VAux=>0.33A  
+3\_3V=>1A

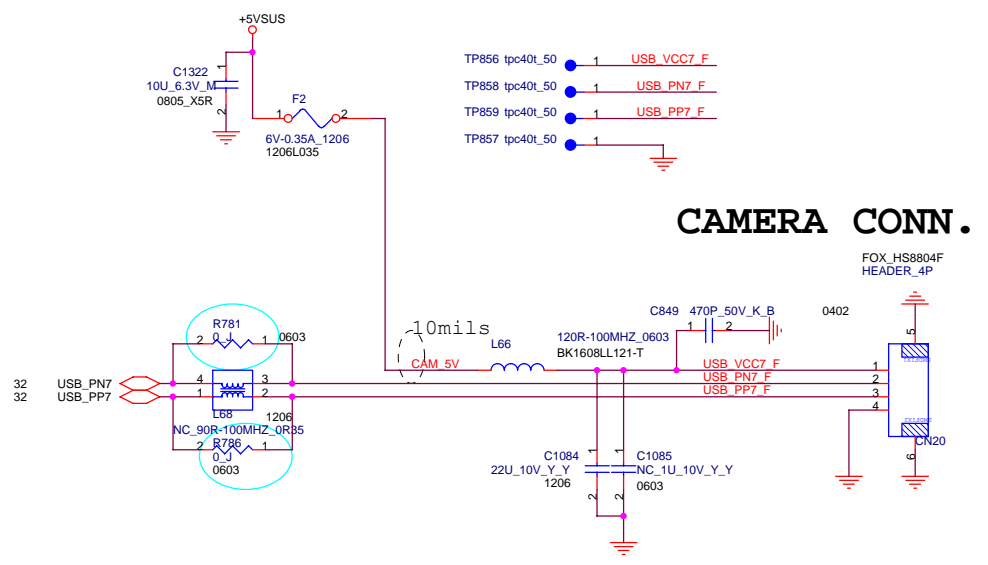


<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	Mini-PCIE Card		
Size	Document Number	Rev	
A3	MS90-1-01	1.0	
Date:	Tuesday, March 27, 2007	Sheet	40 of 72

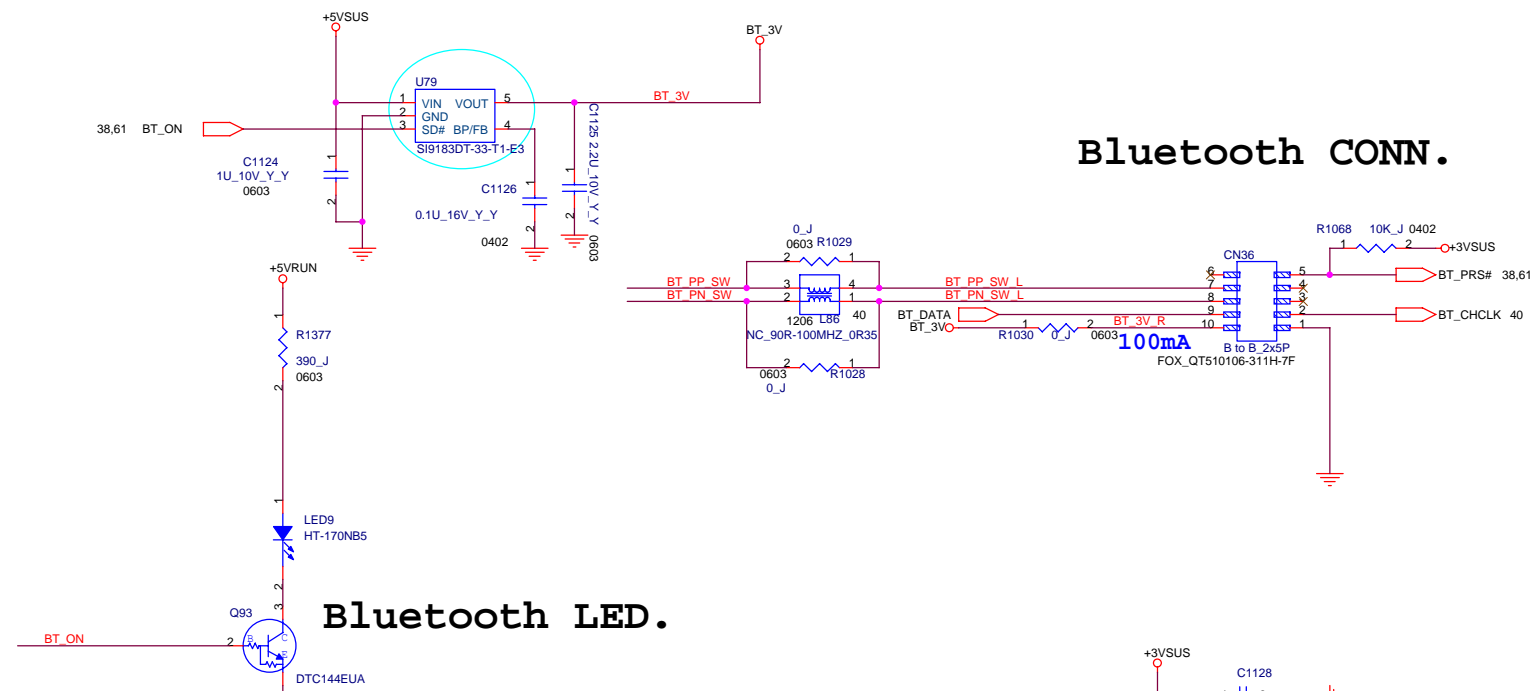


BOM Notice: OIDE\_

W/ Oide SKU	R782,R787,L67,C1086,C1087,C848,CN21	stuff
W/O Oide SKU	R782,R787,L67,C1086,C1087,C848,CN21	no stuff



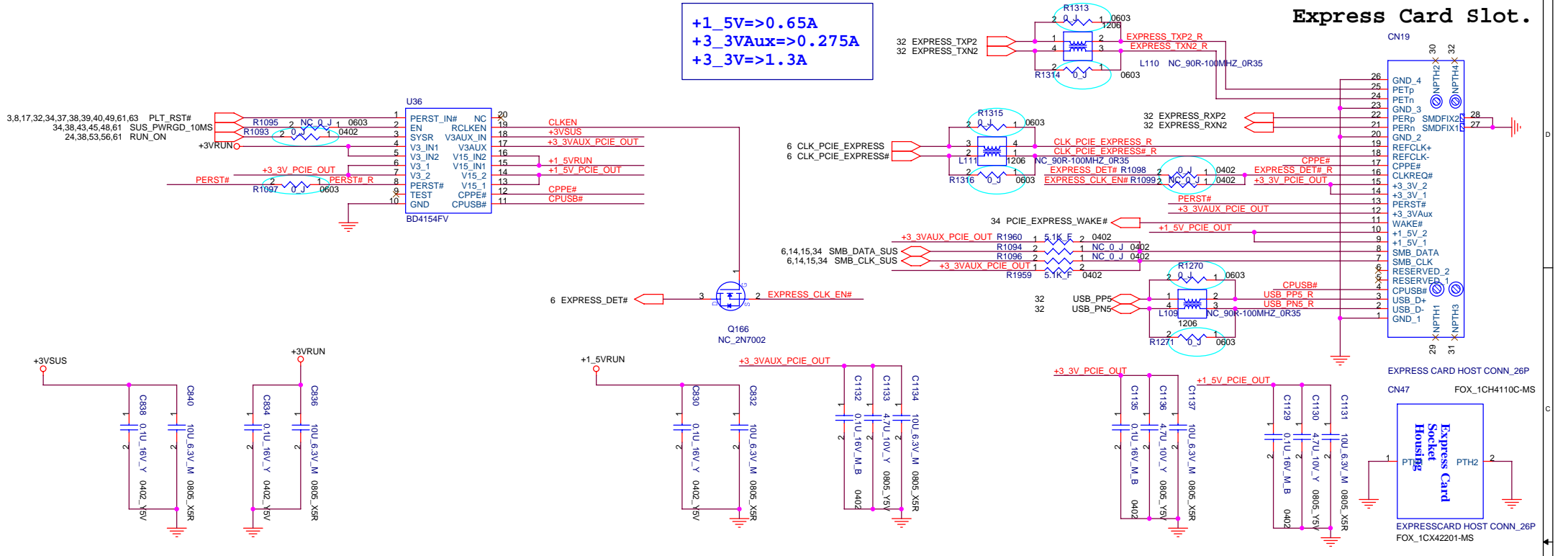
### Bluetooth CONN.



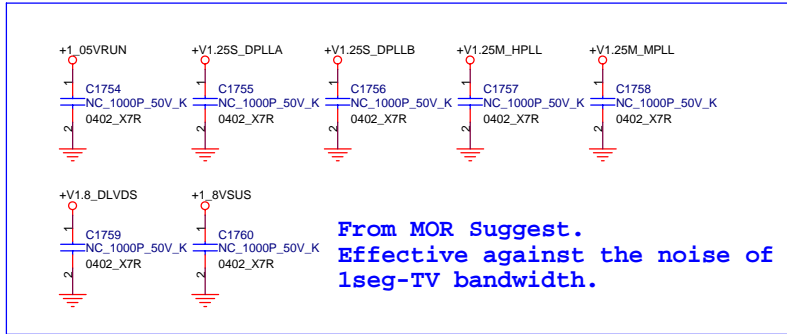
BOM Notice: BT\_

W/ BT SKU	Q93,LEDE9,R1377,U79,C1124,C1125,C1126,C1128,U80,R1068,R1028,R1029,R1030,CN36	stuff
W/O BT SKU	Q93,LEDE9,R1377,U79,C1124,C1125,C1126,C1128,U80,R1068,R1028,R1029,R1030,CN36	no stuff

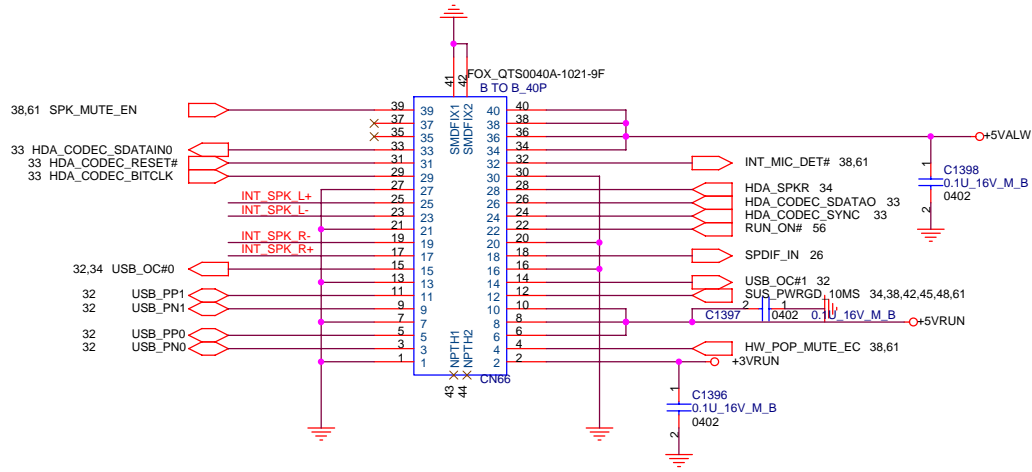
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title: <b>Bluetooth/CAM/OIDE</b>			
Size: A3	Document Number: MS90-1-01	Rev: 1.1	
Date: Tuesday, March 27, 2007	Sheet: 41	of 72	



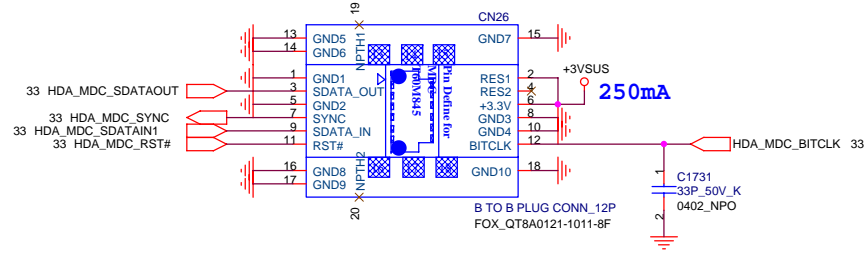
**+1\_5V=>0.65A**  
**+3\_3VAux=>0.275A**  
**+3\_3V=>1.3A**



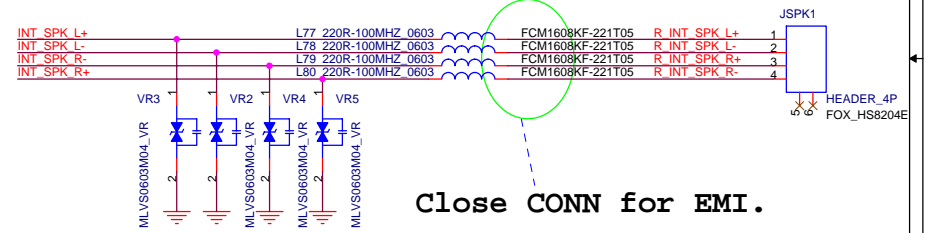
# Audio & USB Board CONN.



# MDC CONN.



# INTERNAL SPEAKER



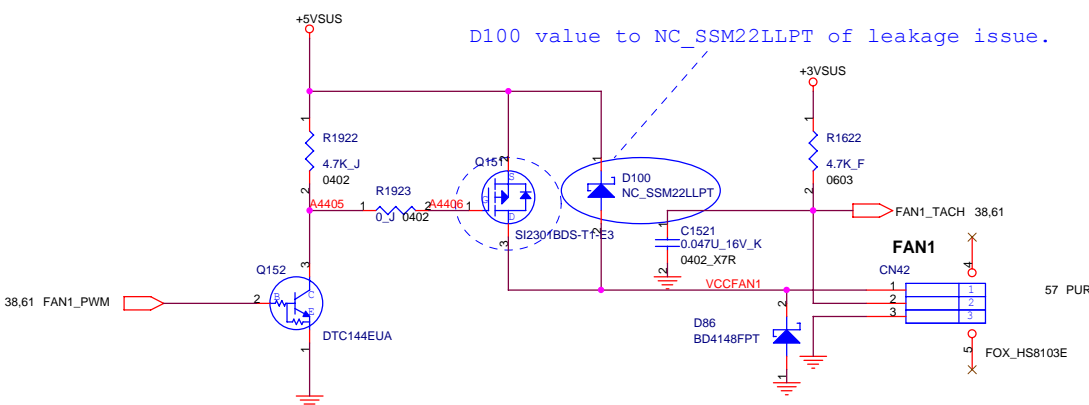
- TP863 tpc40t\_50 ● 1 R\_INT\_SPK L+
- TP864 tpc40t\_50 ● 1 R\_INT\_SPK L-
- TP866 tpc40t\_50 ● 1 R\_INT\_SPK R+
- TP865 tpc40t\_50 ● 1 R\_INT\_SPK R-



0331: Add diode for inverse current and change pull-high resistor from 10K to 4.7K.

0331: Change C1521 from Y5V to X7R.

D100 value to NC\_SSM22LLPT of leakage issue.

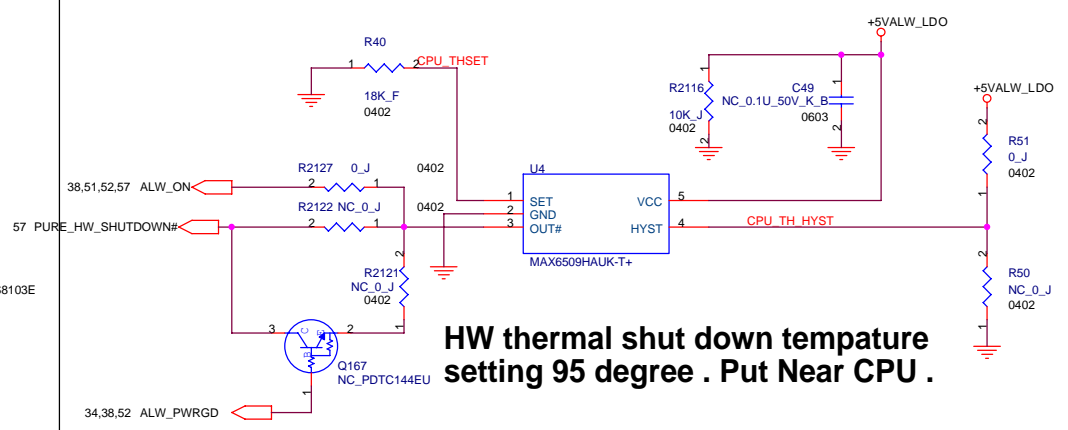


- TP860 tpc40t\_50 1 VCCFAN1
- TP862 tpc40t\_50 1 FAN1\_TACH
- TP861 tpc40t\_50 1

D86 close to CN42.

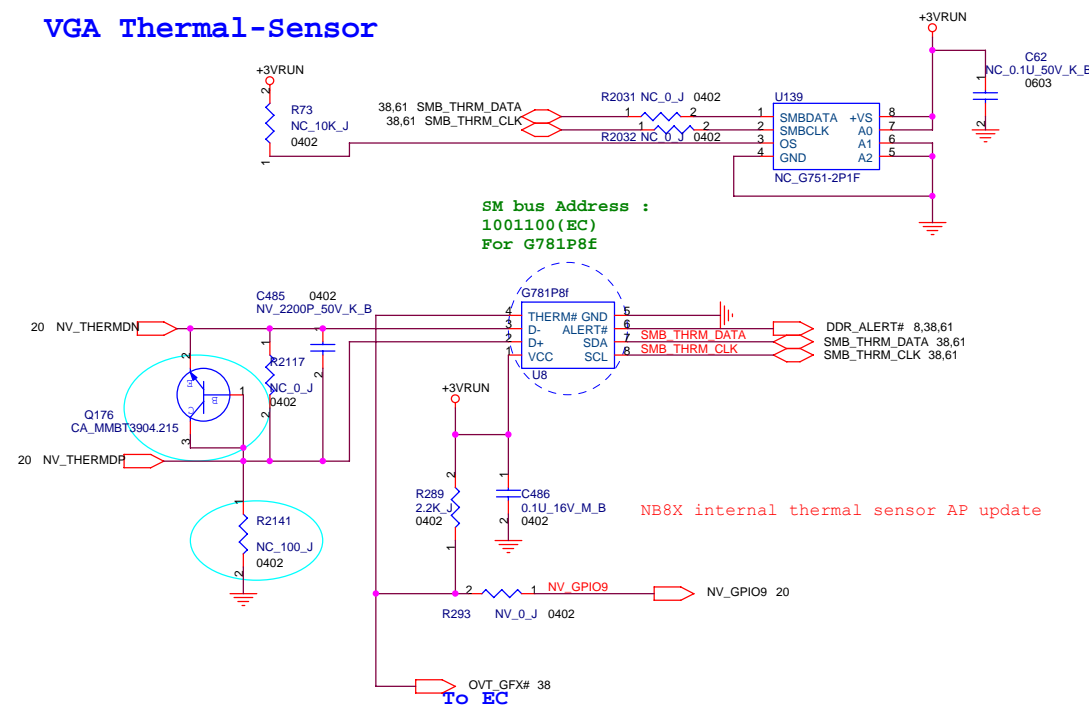
### FAN

## HW THERMAL PROTECTION



HW thermal shut down tempature setting 95 degree . Put Near CPU .

### VGA Thermal-Sensor



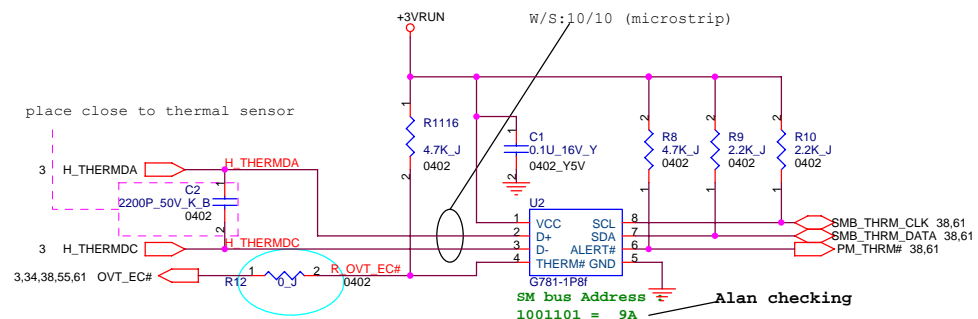
SM bus Address :  
1001100 (EC)  
For G781P8f

NB8X internal thermal sensor AP update

Close to U7

- TP914 tpc40t\_50 H\_THERMDA
- TP915 tpc40t\_50 H\_THERMDC

### CPU Thermal-Sensor

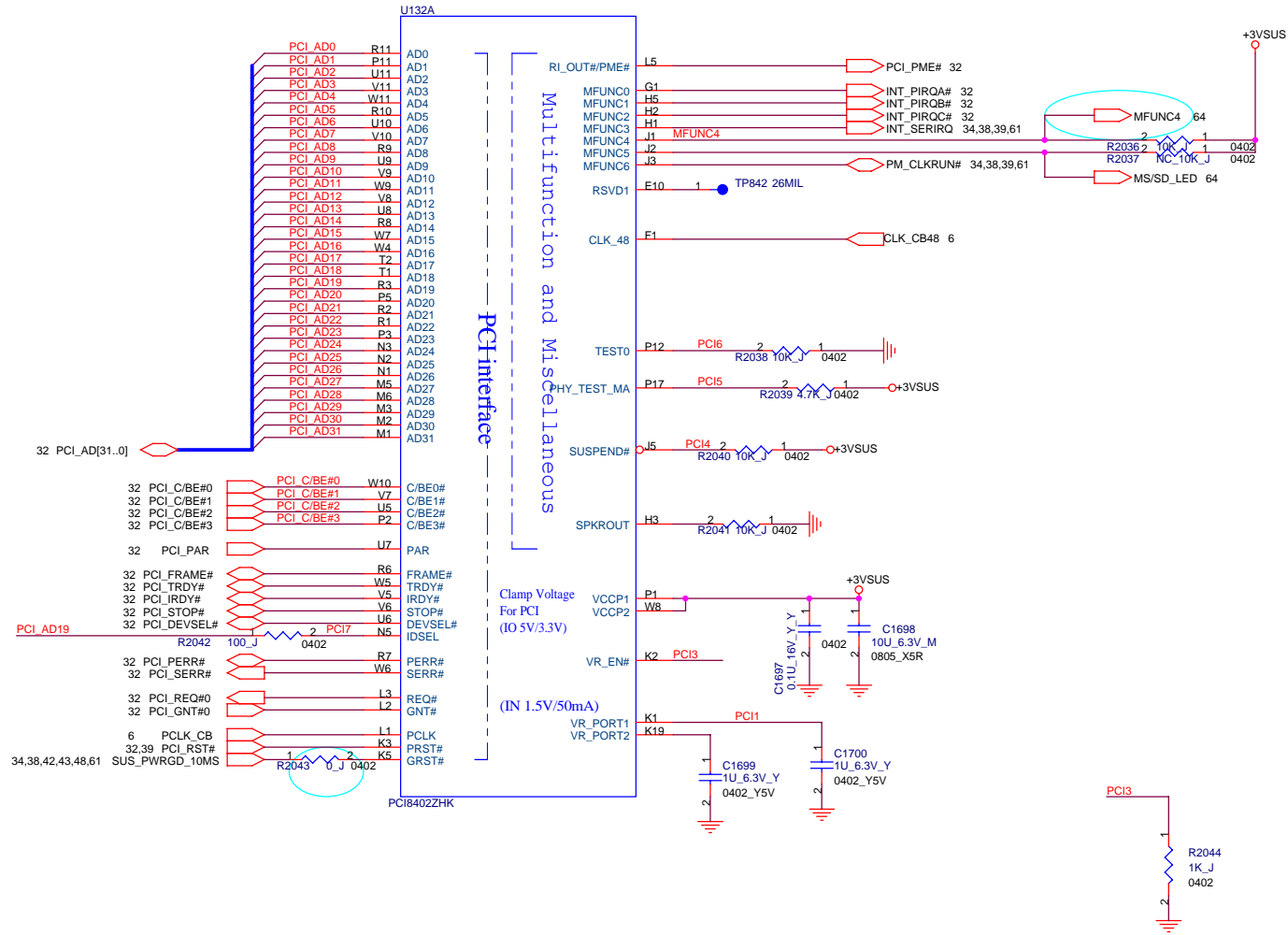


SM bus Address 1001101 = 9A Alan checking

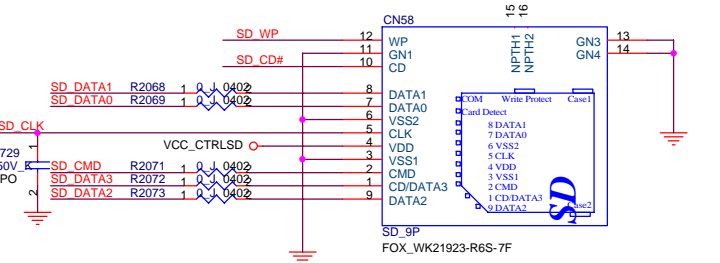
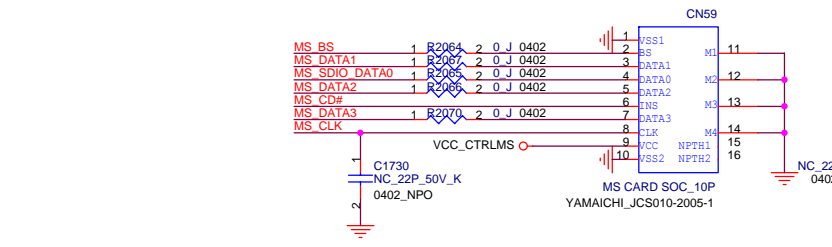
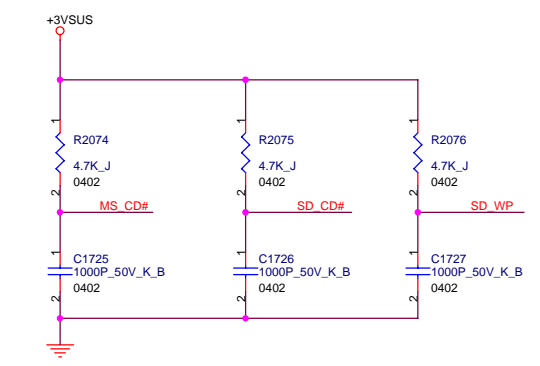
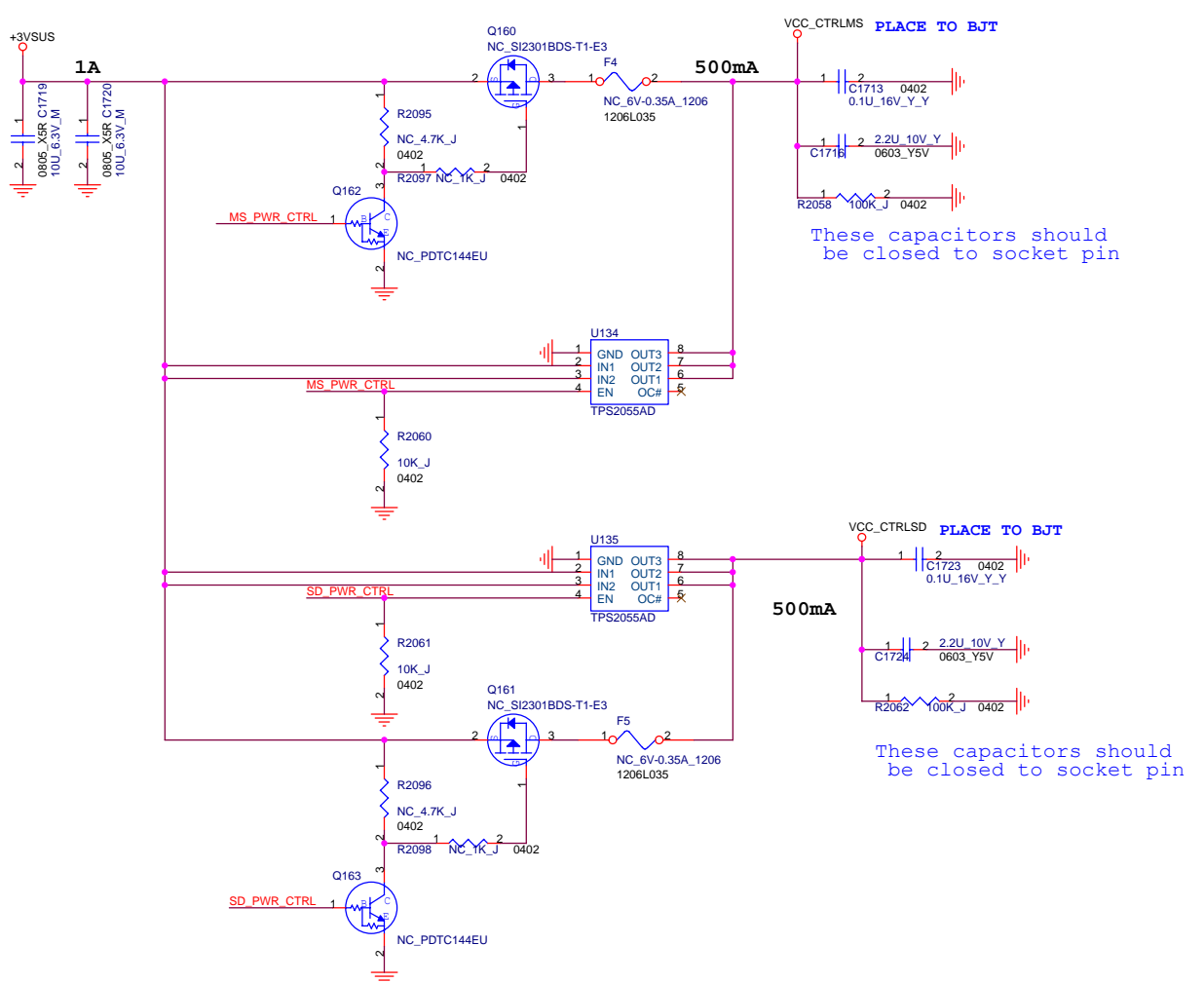
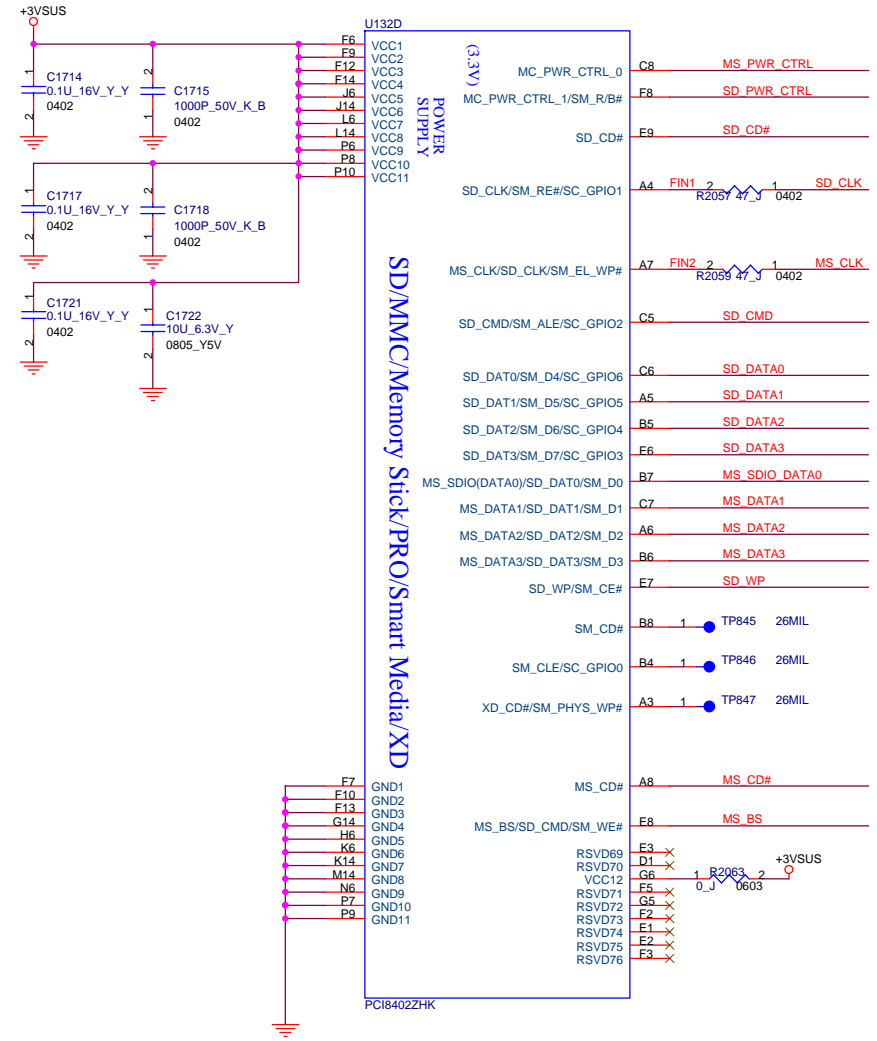
Place Thermal-Sensor near CPU & GMCH.

Close to U109

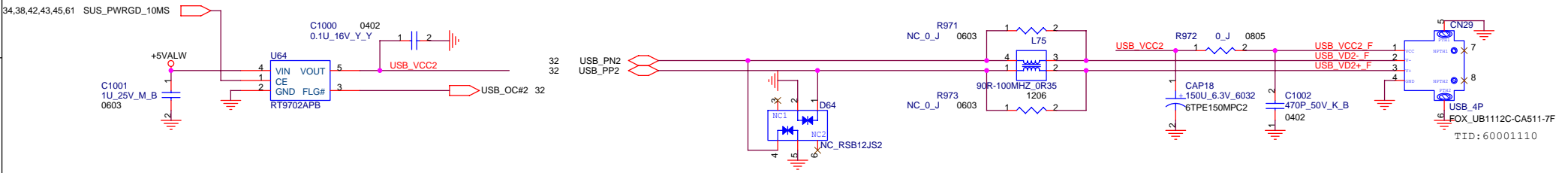
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title <b>FAN/Thermal-Sensor</b>		CCPBG - R&D Division	
Size A3	Document Number MS90-1-01	Rev 1.1	
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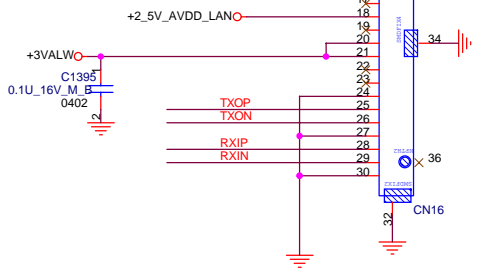


# USB CONN.

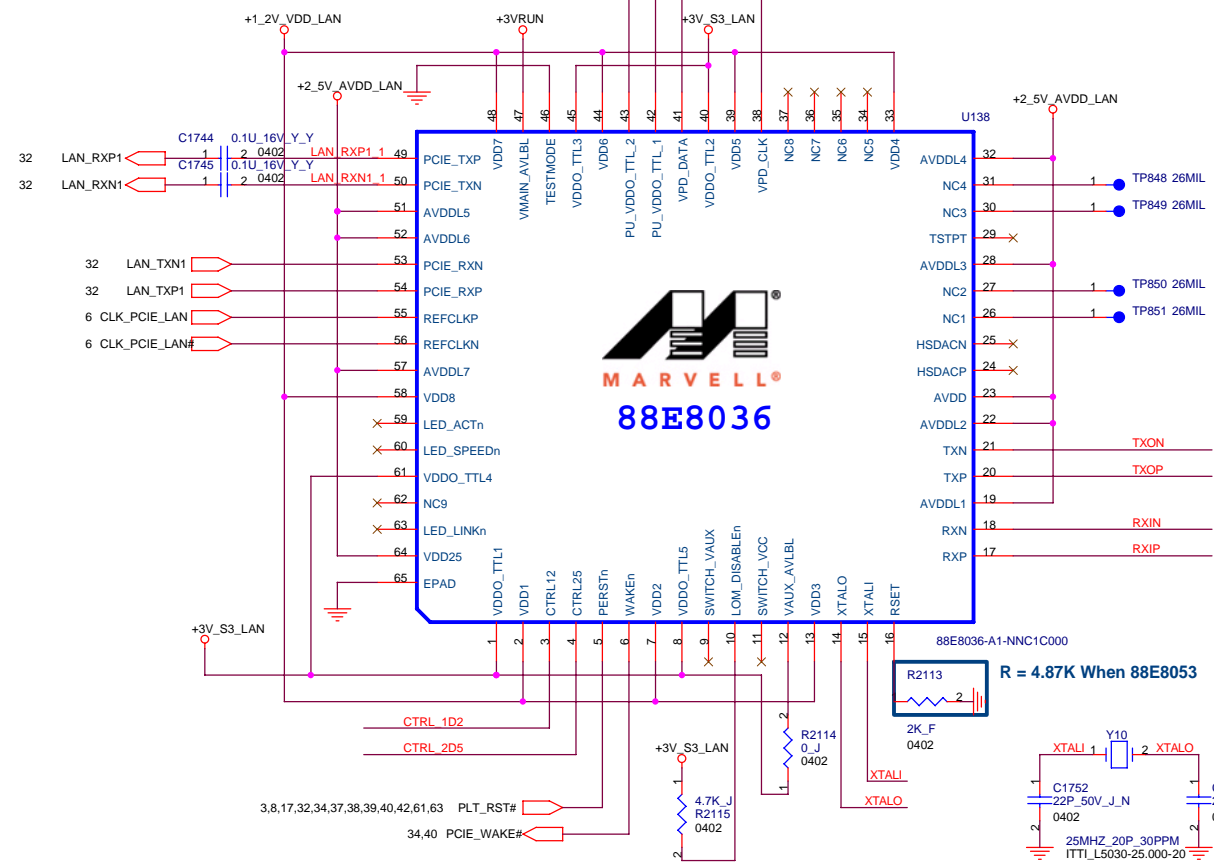
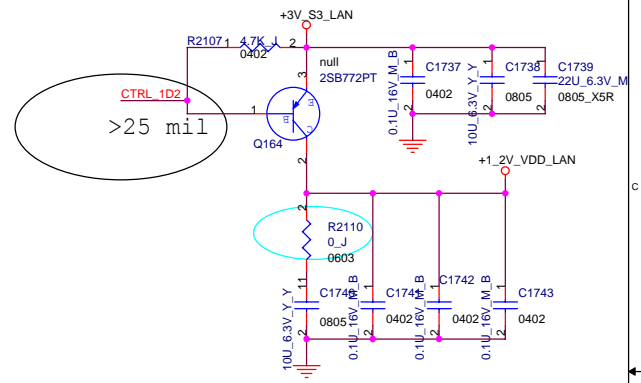
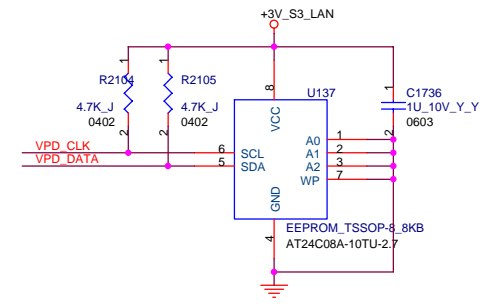
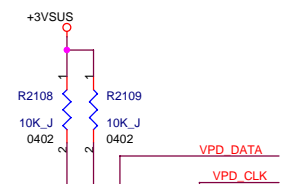
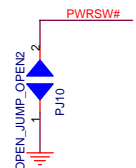


- TP867 tpc40t\_50 1 PWRSW#
- TP912 tpc40t\_50 1 PWRSW#
- 38 KSO16
- 38,39 PWRSW#
- 38,61 SCROLL\_LOCK\_LED#
- 38,61 CAP\_LED#
- 38,61 KSI4
- 38,61 KSI2
- 38,61 KSI1
- 38,61 KSI3
- 38,61 KSO15
- 38,61 KSI7
- 38,61 KSI6
- 38,61 KSI5
- 38,61 NUM\_LOCK\_LED#

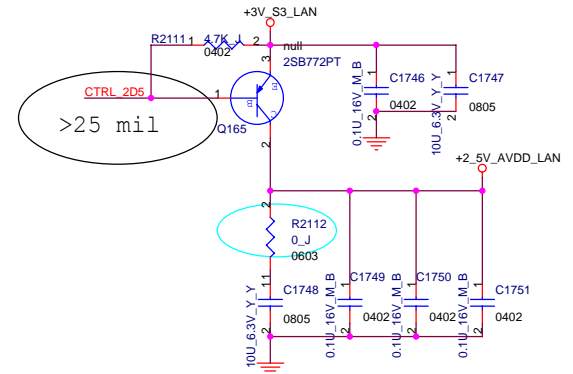
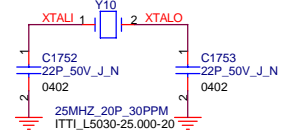
FOX\_GS12301-1011A-9F  
FPC RECEPTAL CONN\_30P



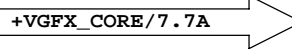
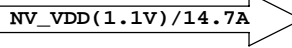
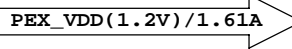
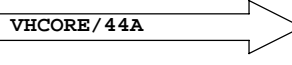
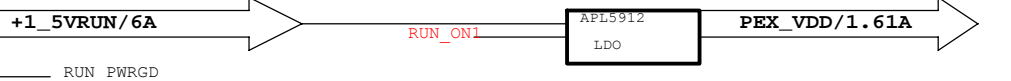
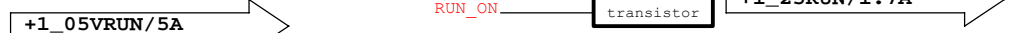
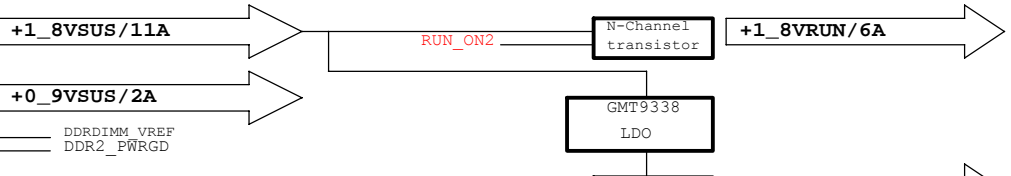
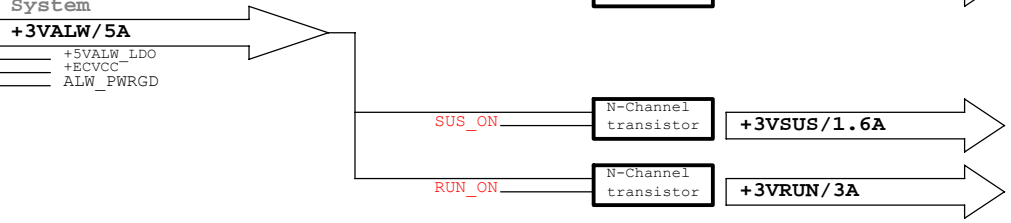
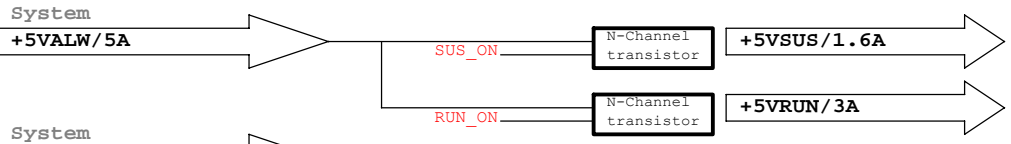
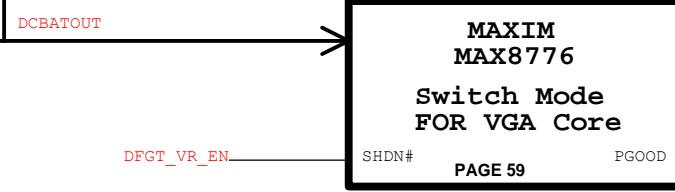
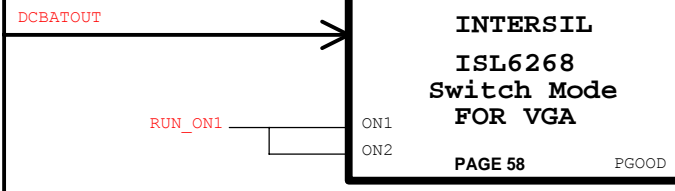
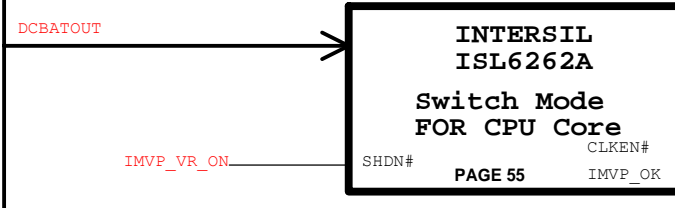
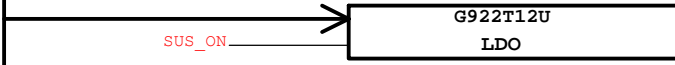
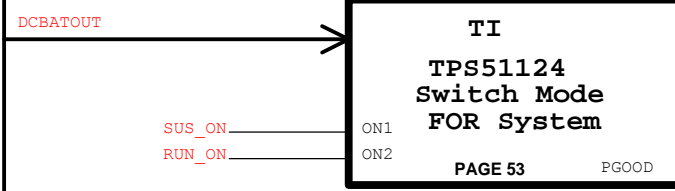
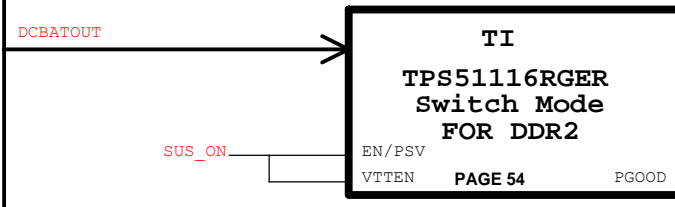
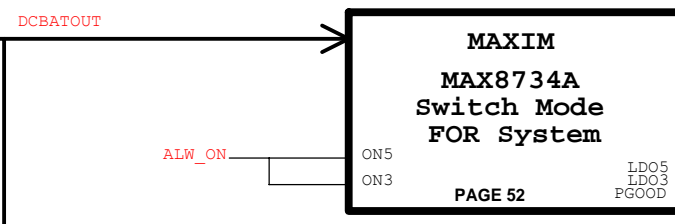
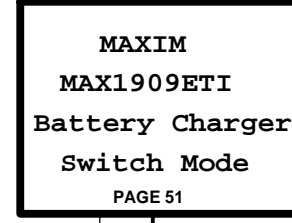
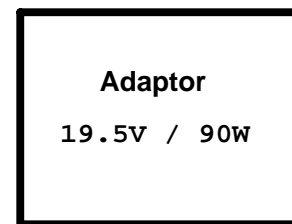
Switch Board CONN.



R2113 R = 4.87K When 88E8053



FOXCONN HON HAI PRECISION IND. CO., LTD.	
CPBG - R&D Division	
Title LAN (88E8036)	
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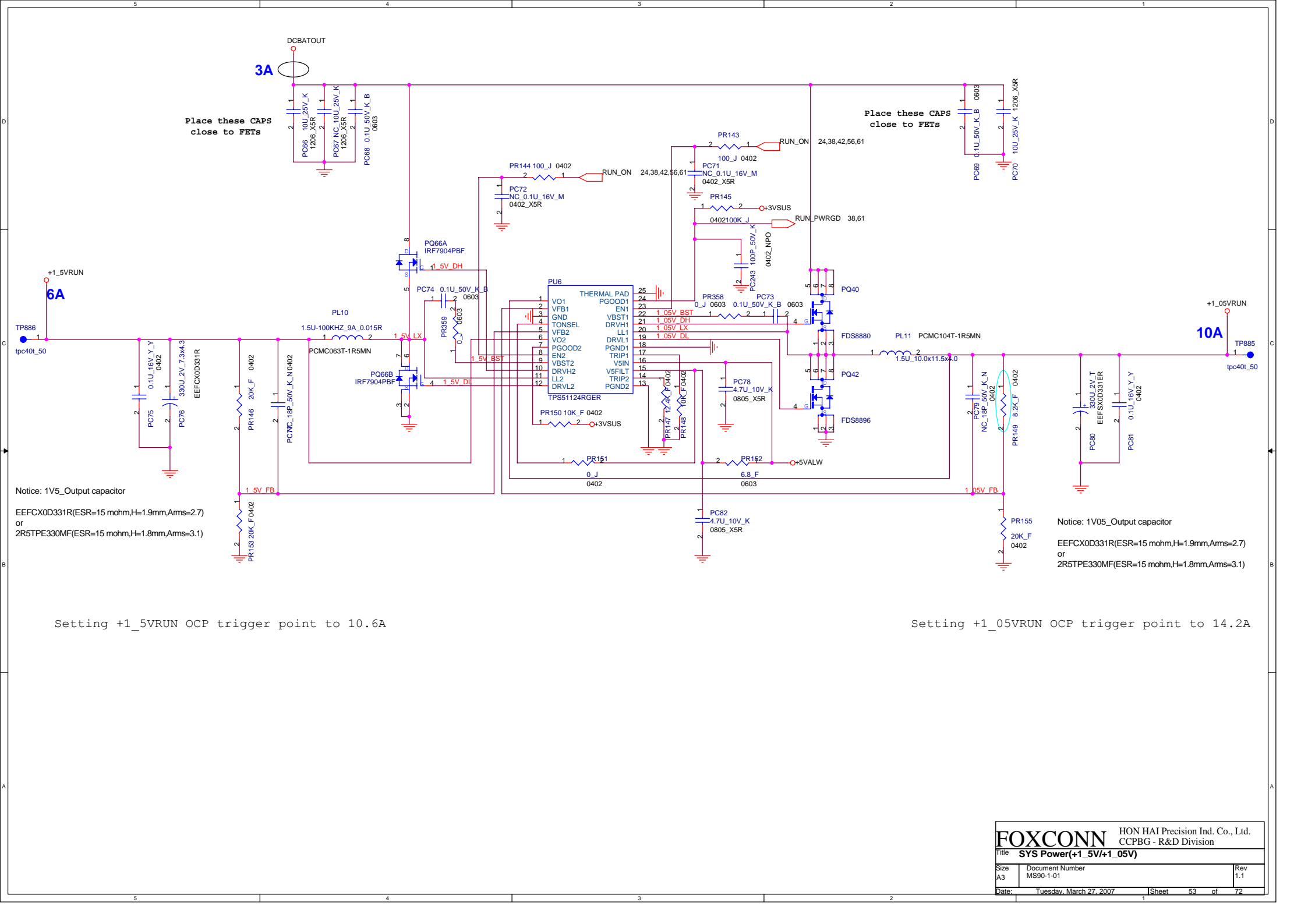


<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>Power Design Diagram</b>			
Size A3	Document Number MS90-1-01	Rev 1.0	
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Place these CAPS close to FETs

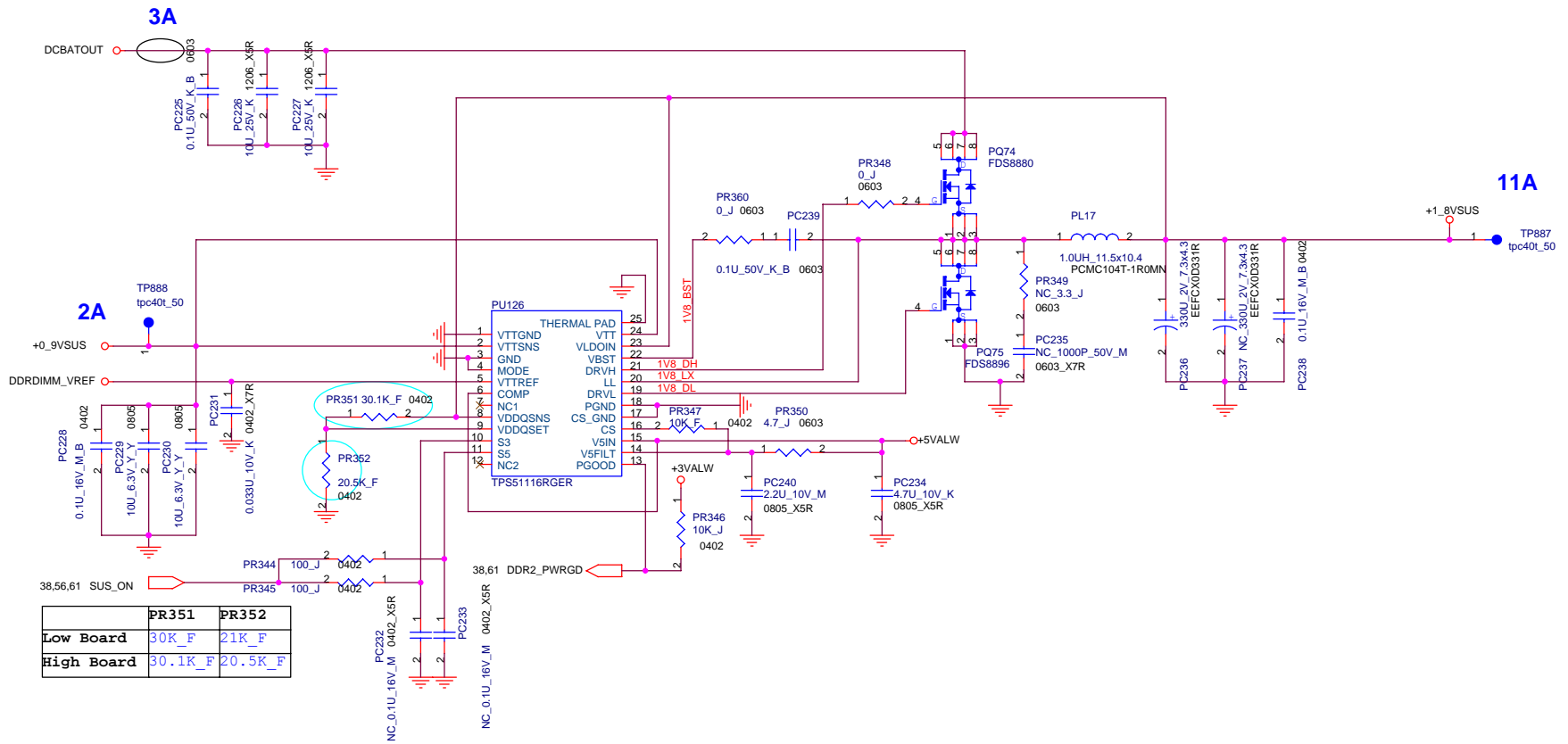
Place these CAPS close to FETs

Notice: 1V5\_Output capacitor  
 EEFCX0D331R(ESR=15 mohm,H=1.9mm,Arms=2.7)  
 or  
 2R5TPE330MF(ESR=15 mohm,H=1.8mm,Arms=3.1)

Notice: 1V05\_Output capacitor  
 EEFCX0D331R(ESR=15 mohm,H=1.9mm,Arms=2.7)  
 or  
 2R5TPE330MF(ESR=15 mohm,H=1.8mm,Arms=3.1)

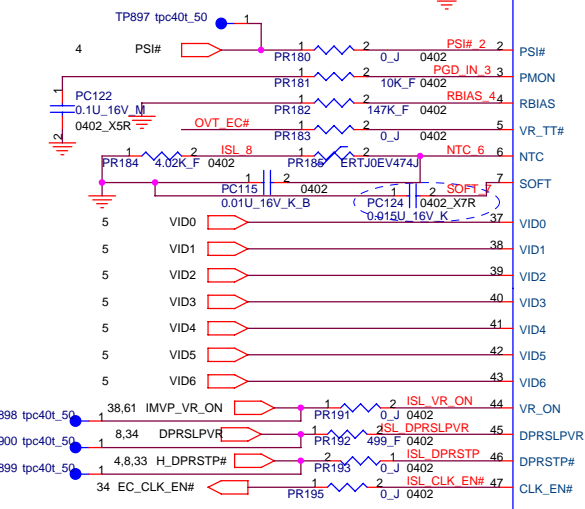
Setting +1\_5VRUN OCP trigger point to 10.6A

Setting +1\_05VRUN OCP trigger point to 14.2A



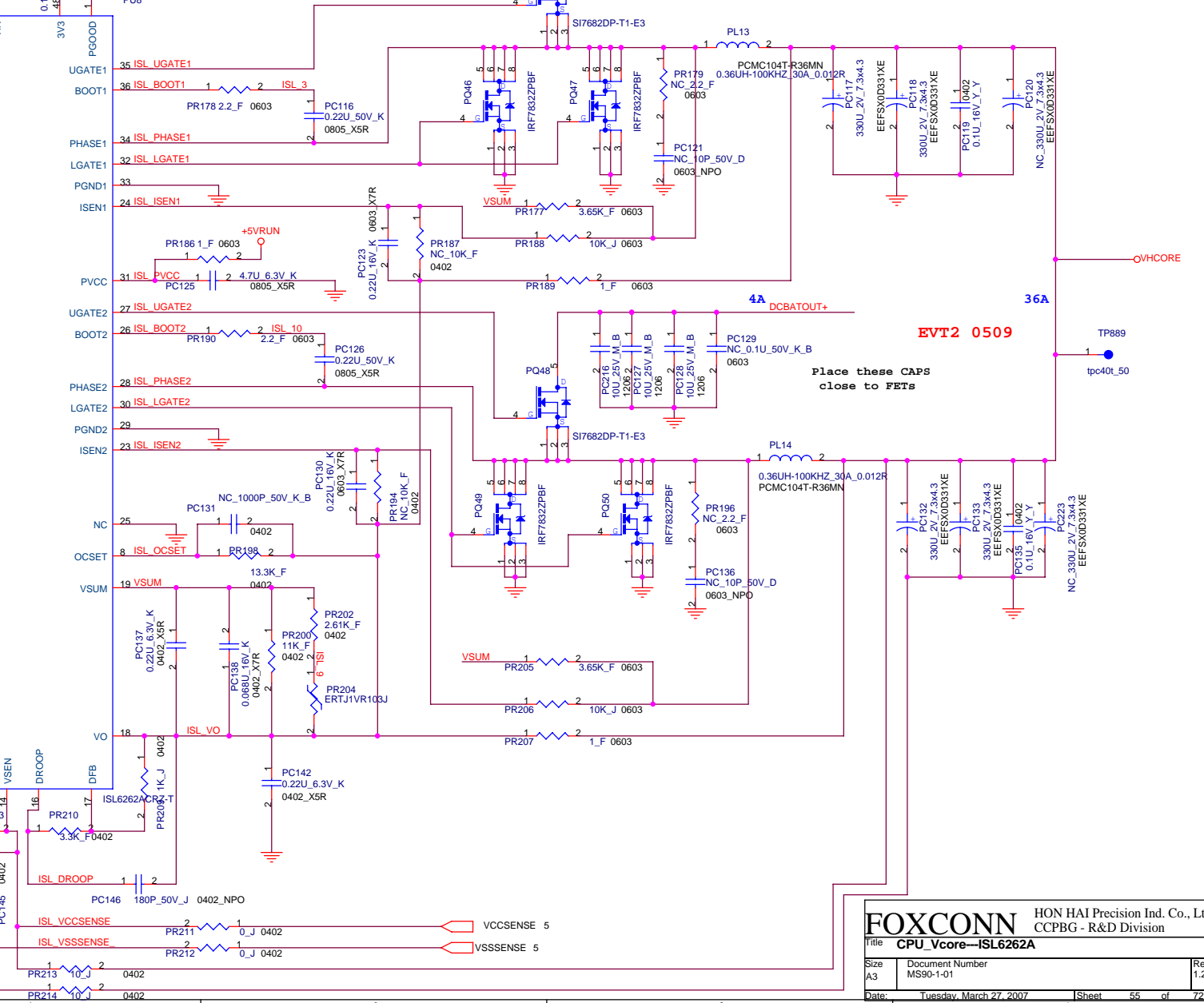
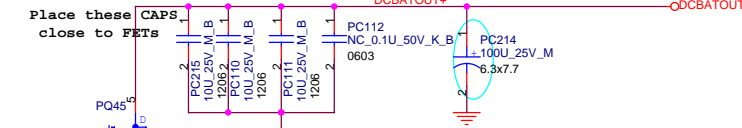
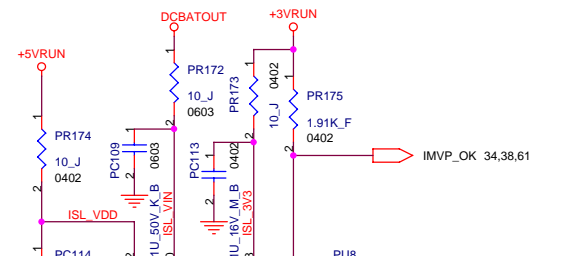
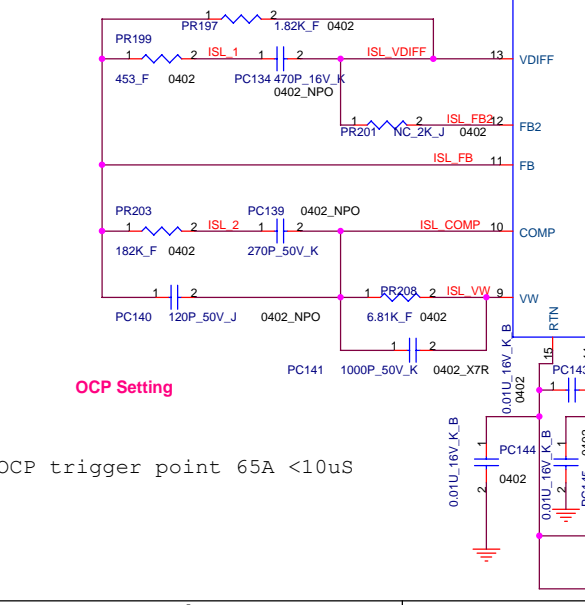
Setting +1\_8VSUS OCP trigger point to 16A

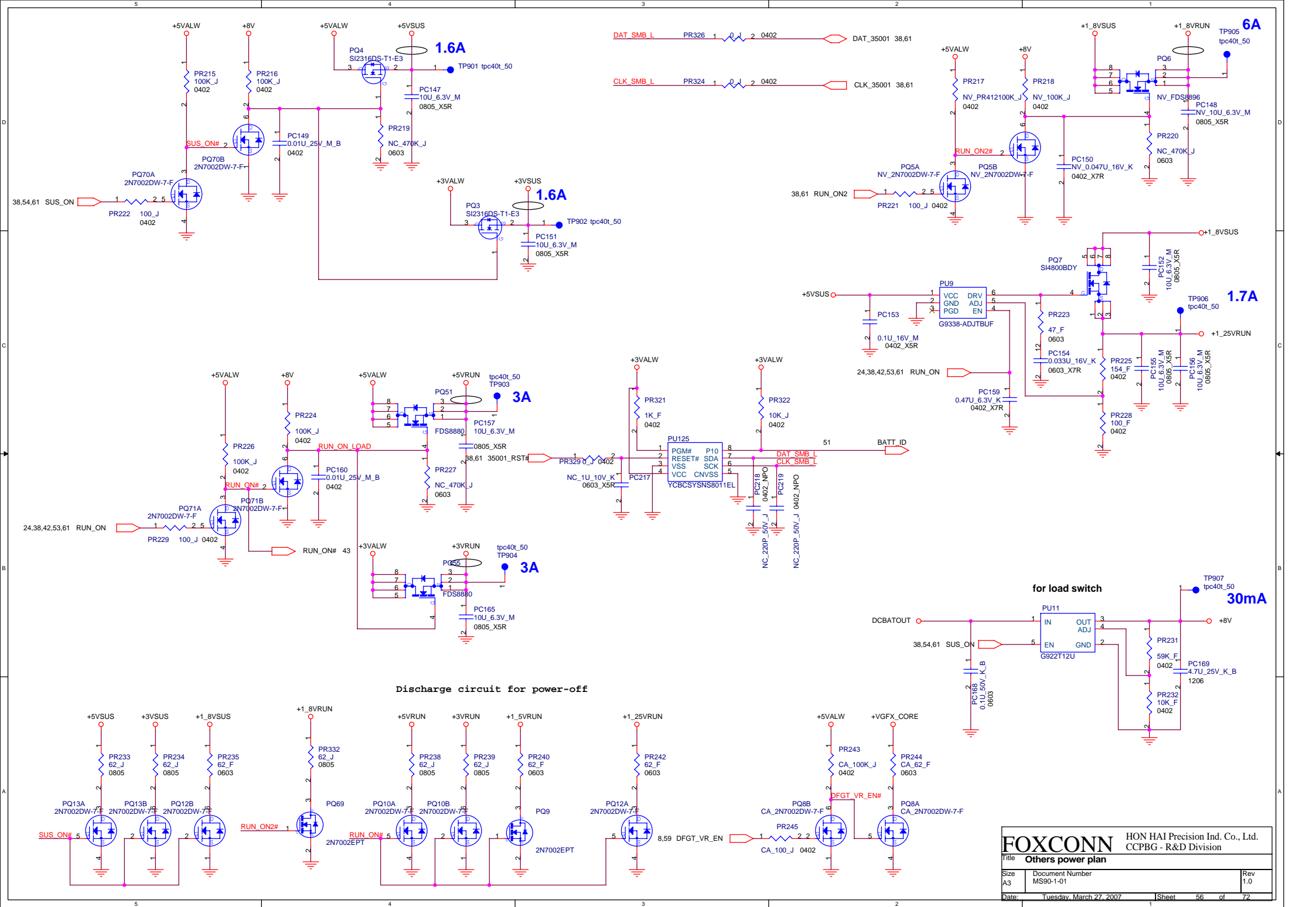
3.34,38,44,61 OVT\_EC#



**OCP Setting**

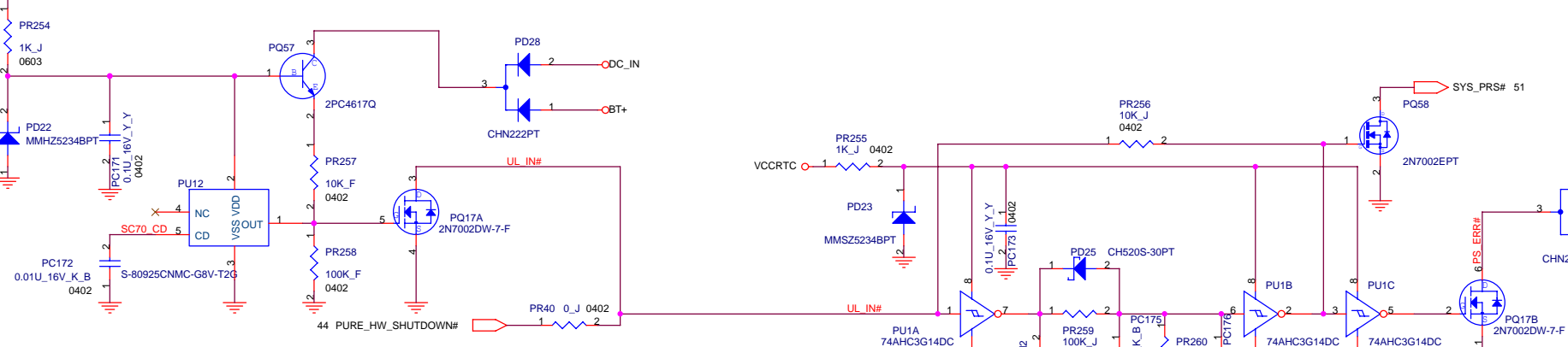
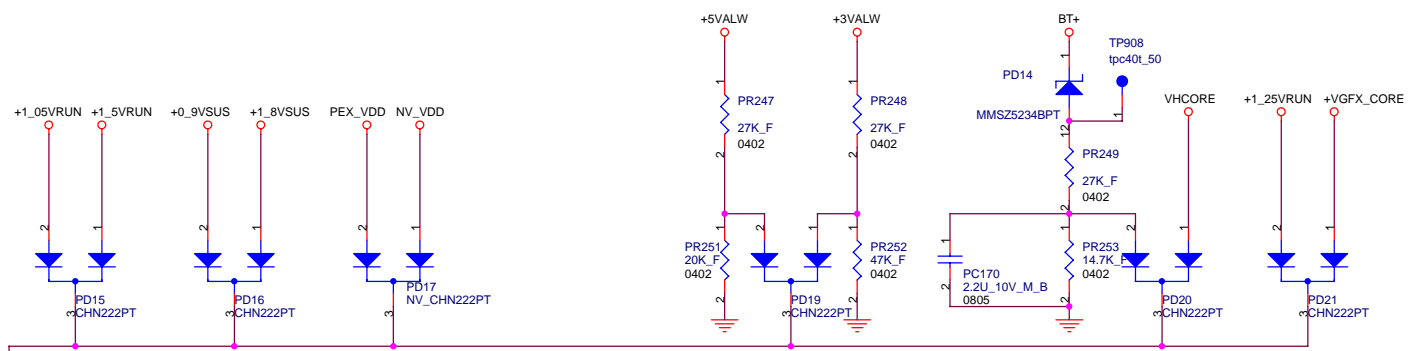
OCP trigger point 65A <10uS



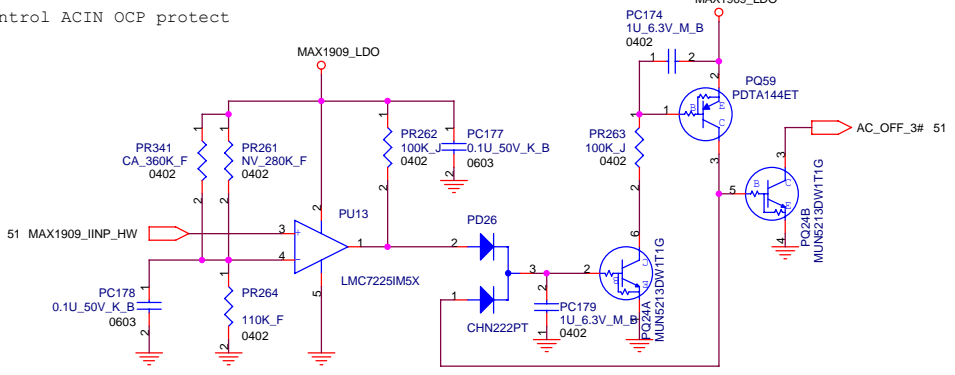


**Discharge circuit for power-off**

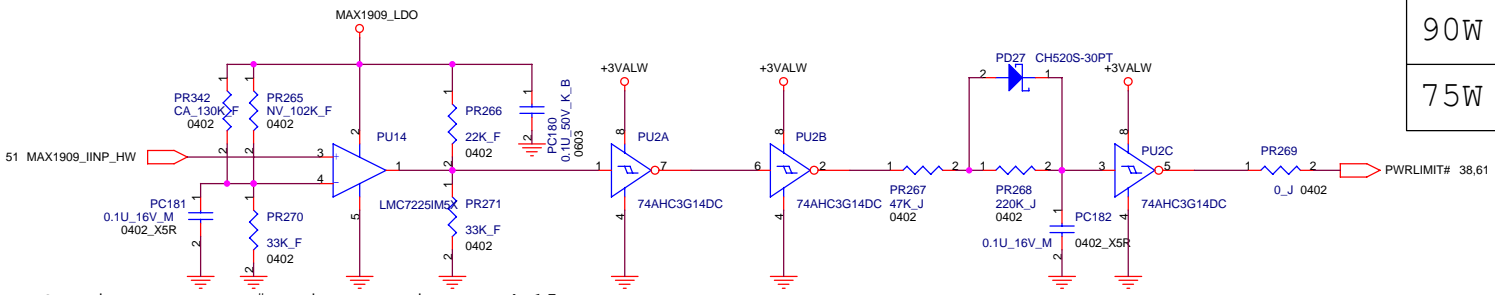
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
<b>Others power plan</b>			
Title	Document Number	Rev	
Size A3	MS90-1-01	1.0	
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Control ACIN OCP protect



Setting ACIN OCP trigger point to 5.077A



Setting PWRLIMIT# trigger point to 4.15A

		ACIN OCP
90W	PR261:NV_280K	5.07A/98.9W
75W	PR341:CA_360K	4.21A/82.1W

		PWRLIMIT
90W	PR265:NV_102K	4.4A/85.8W
75W	PR342:CA_130K	3.64A/71W

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

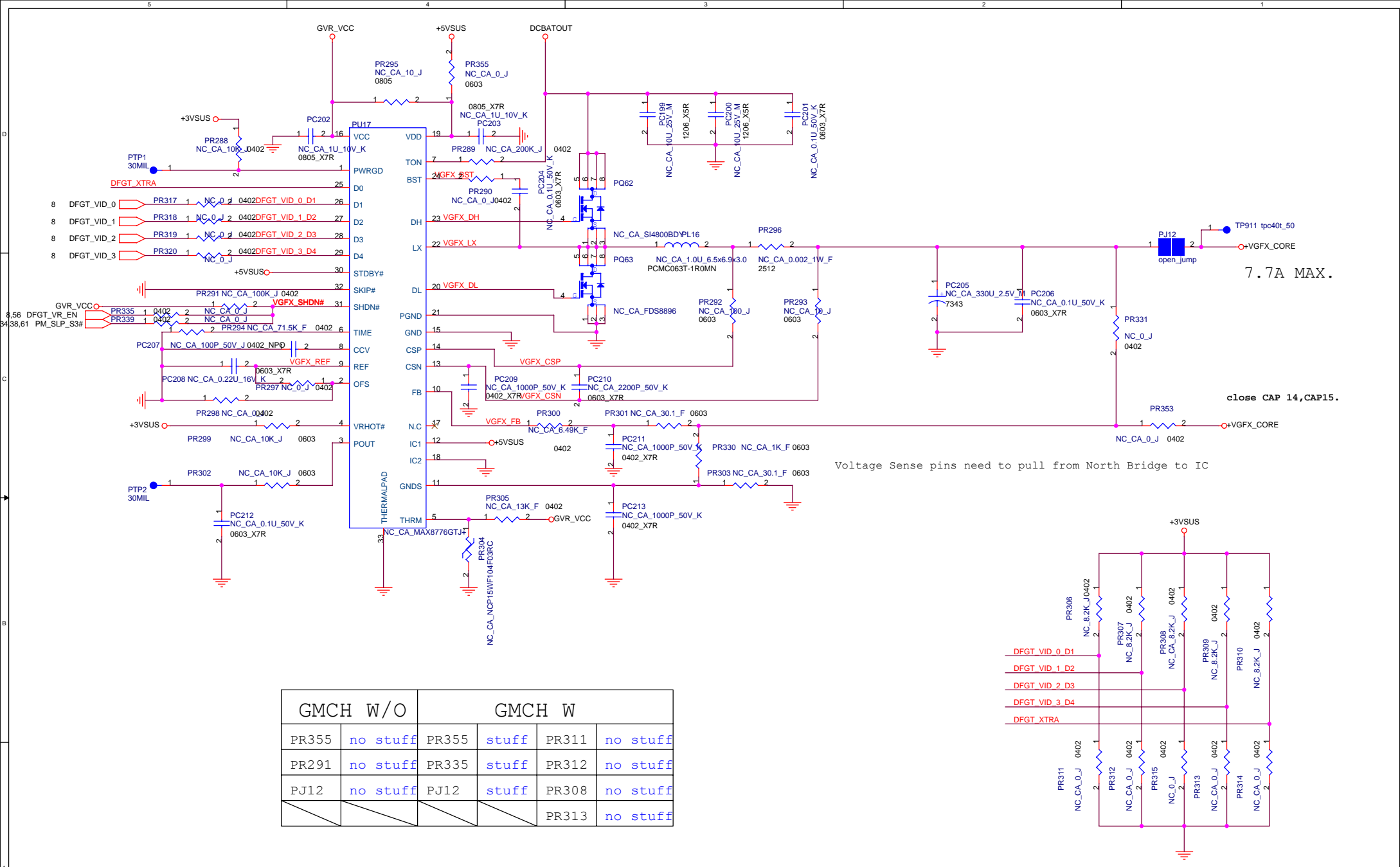
Title: **OVP protection**

Size: A3	Document Number: MS90-1-01	Rev: 1.0
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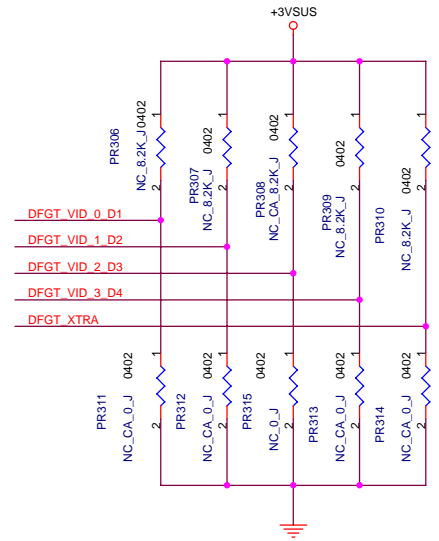
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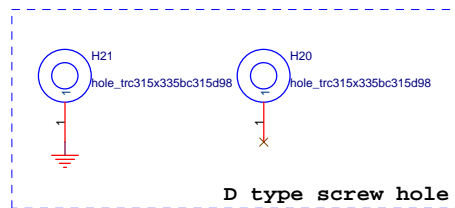
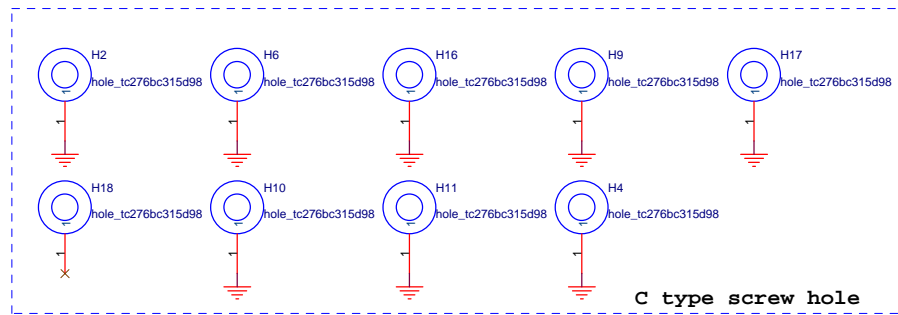
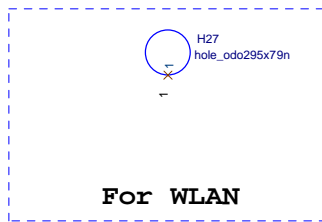
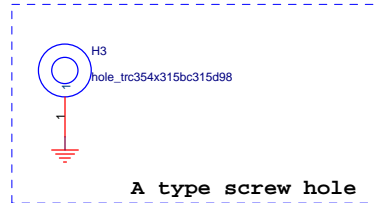
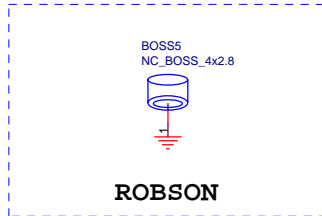
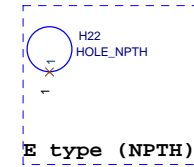
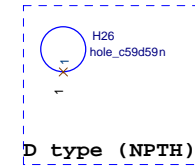
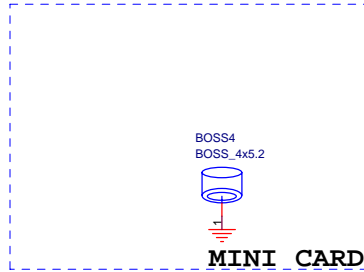
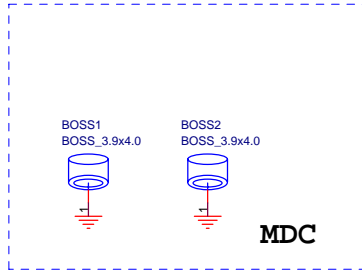
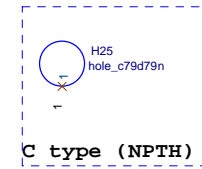
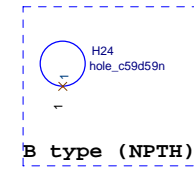
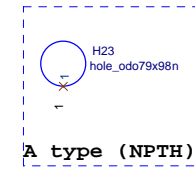
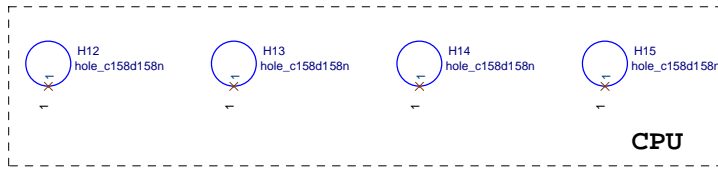




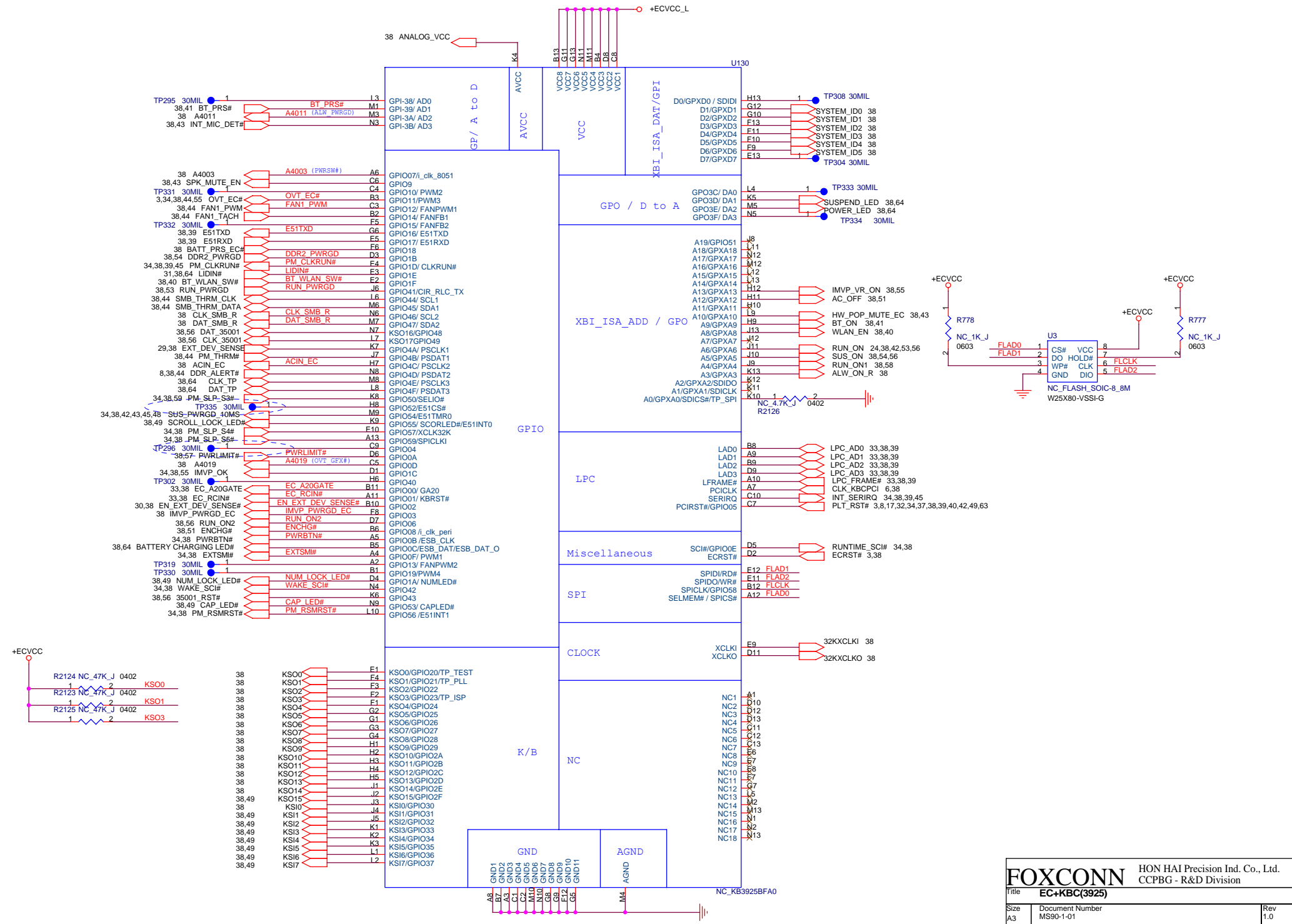


	GMCH W/O	GMCH W				
	PR355	no stuff	PR355	stuff	PR311	no stuff
	PR291	no stuff	PR335	stuff	PR312	no stuff
	PJ12	no stuff	PJ12	stuff	PR308	no stuff
					PR313	no stuff

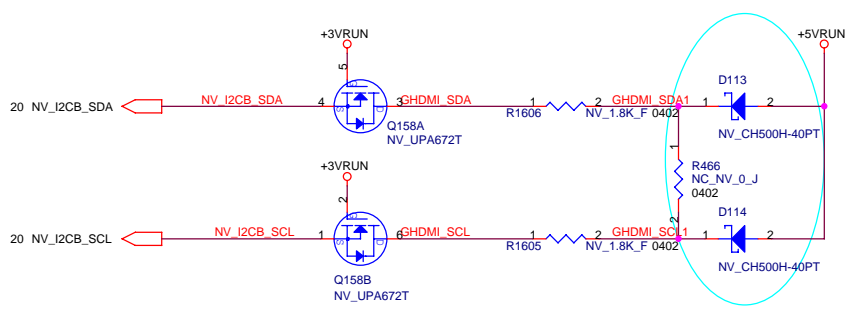
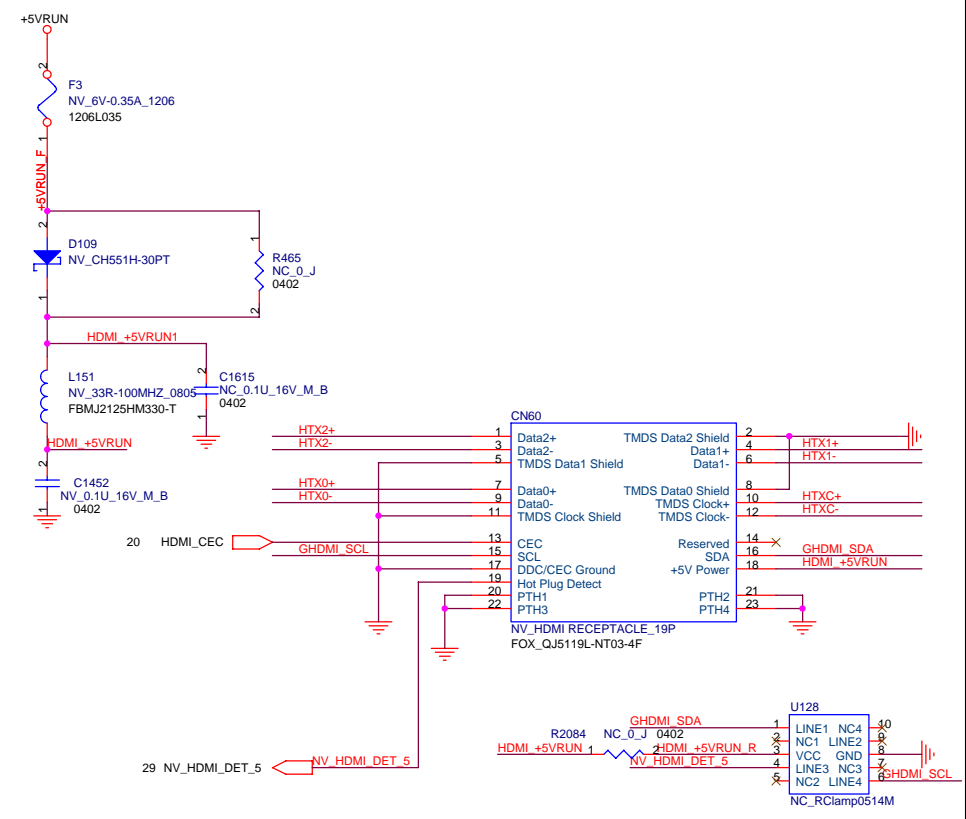
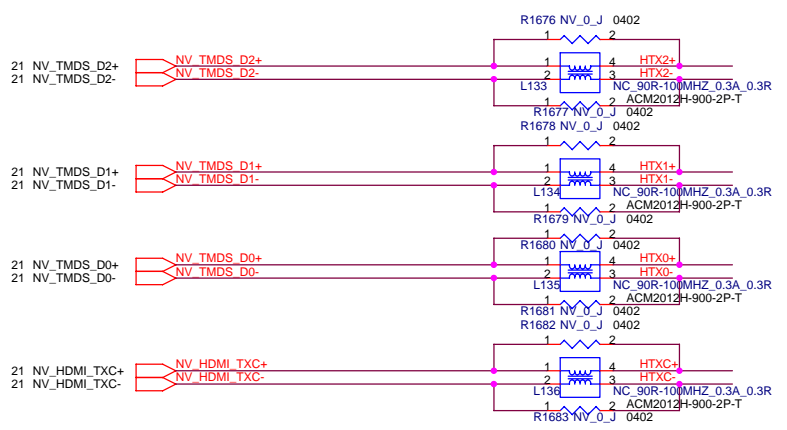




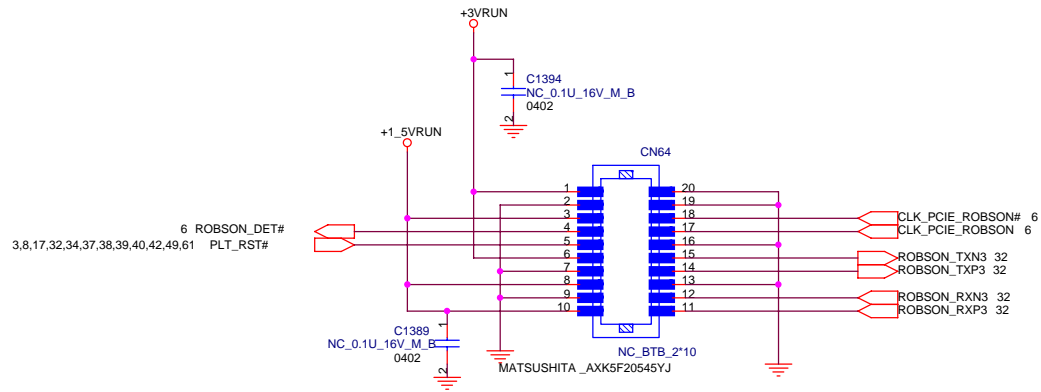
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Title	<b>HOLE</b>		
Size	Document Number	Rev	
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		CCPBG - R&D Division	
Title	<b>EC+KBC(3925)</b>		
Size	Document Number		Rev
A3	MS90-1-01		1.0
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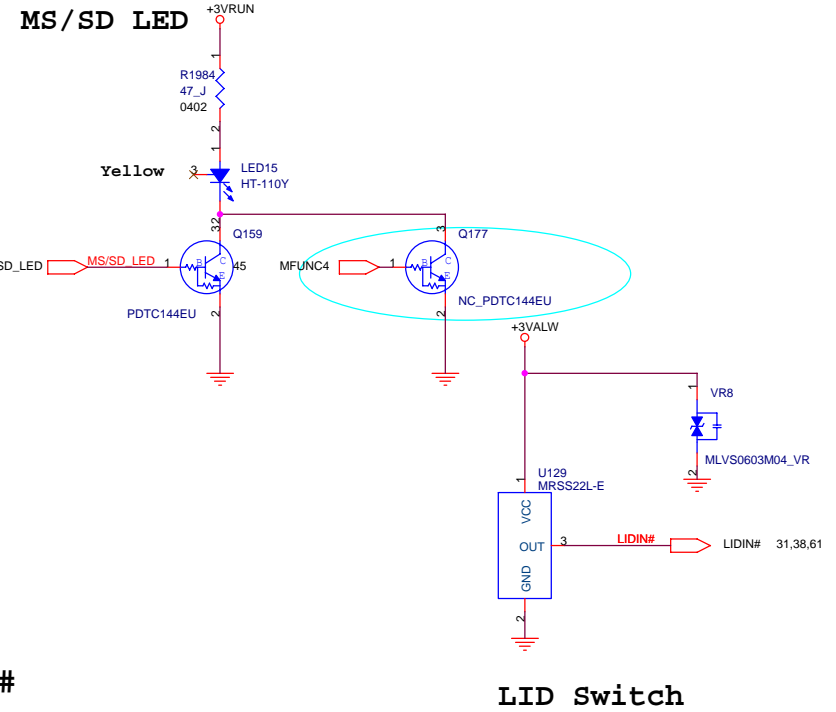
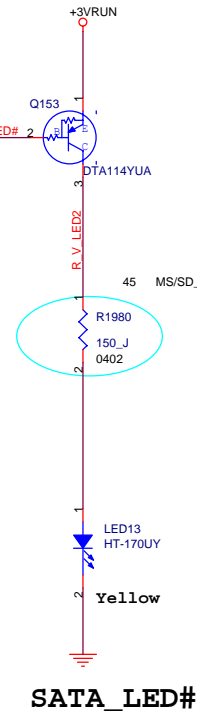
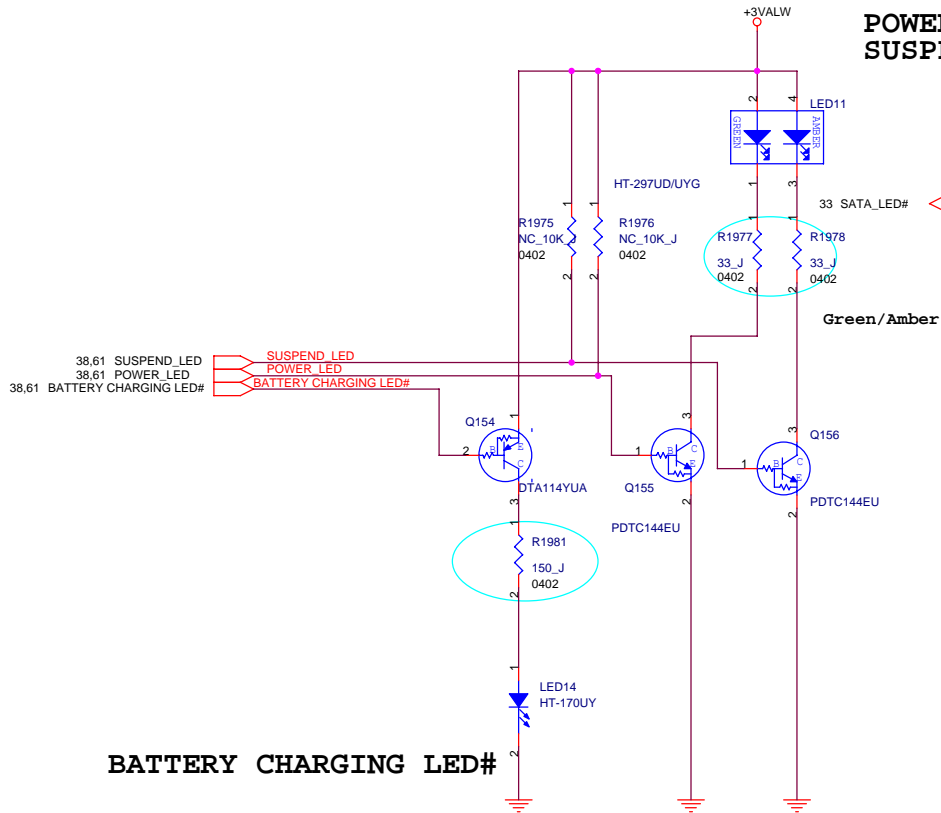


### ROBSON Board CONN

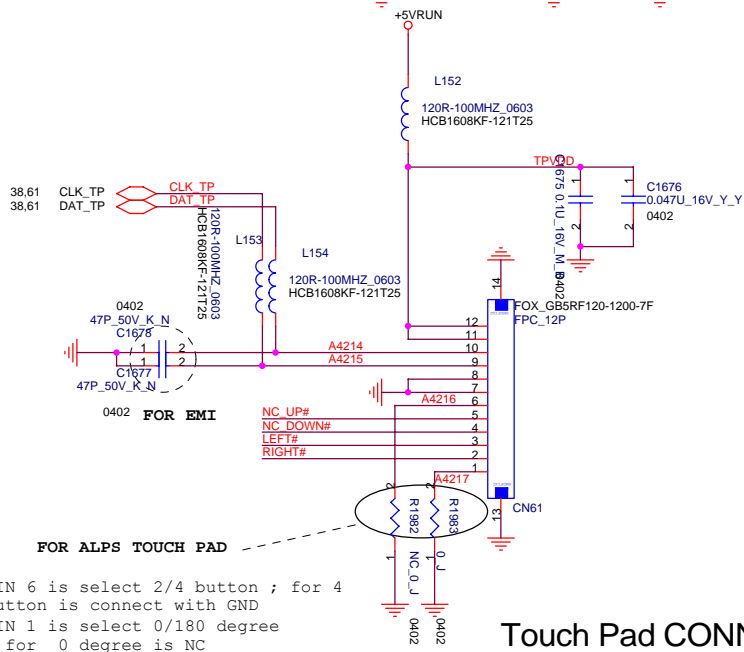


C1389,C1394 close to CN64.

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title <b>ROBSON B to B Connector</b>			
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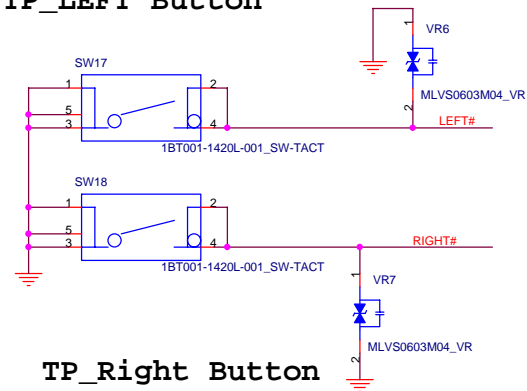
### BATTERY CHARGING\_LED#



### Touch Pad CONN.

PIN 6 is select 2/4 button ; for 4 button is connect with GND  
PIN 1 is select 0/180 degree ; for 0 degree is NC

### TP\_Left Button



<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division	
Title	LED/Touch/Lid		
Size	Document Number	Rev	
A3	MS90-1-01	1.2	
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**MS90 EVT**

**(2006/04/14)**

P.34 Change value R1926 NC 0 to 0,R1447NC 2K to 2K,U33 NC SN74AHC1G14DCK to SN74AHC1G14DCK,R1927 0 to NC\_0 for inTel desgin guide-rev:0.9

P.35 C884 change value 0.01uF\_5%\_1/16W\_X7R to 0.01U\_16V\_K, because value error.

**(2006/04/17)**

P.25,26 Change VRAM DDR to DDR3

**(2006/04/20)**

P.07~13 Update U112 symbol.  
P.32~38 Update U31 symbol.

**(2006/05/04)**

P.29 Change U106 value NV\_74AHC1G08GW to 74AHC1G08GW.

P.11 Change L23 value CA\_180R-100MHZ\_0603 to 180R-100MHZ\_0603.

**(2006/05/23)**

P.65 Del PR295,adding PR1964 100K pull high +3.3VSUS from Intel Crestline sightings report (Rev: 1) open issue.  
P.33 SYSTEM ID modify Remove R725, R716,Adding R717, R719, R724 100K ohm for Low.  
Change R1036,R104 80.6 ohm to 20 ohm from Intel CRB Rev:1.201  
Remove PR436,R437,R439,R440,PJ32~PJ36,Adding PR1965~PR1968 for VID issue.  
Change R71: DFN-33 ohm to 22 ohm from north bridge for VID issue.  
Adding R650,R100K ohm pull down resistor on VRMPWRGD from CRB Rev:1.0.  
Remove R483,R487 from CRB Rev:1.201  
Remove RP3 for Clock signal voltage level is not correct issue.

**(2006/05/29)**

P.45,48 Change Q77,Q78,Q84,Q85Q89~Q92 PBSS2515F.115 to PBSS2515E.115 because will be EOL 31.Dec.2006.

P.51 Change CN58 Molex to Foxconn the same MS70.  
P.45 Change CAP22,CAP23 SHOEI to Panasonic because SHOEI parts will be EOL.

**(2006/06/02)**

P.58 Change PU6 MAX8743EEI+ to TPS51124RGER for layout space.  
P.60 Change MAX8771 to ISL6262ACRZ-T for Layout Space.  
P.63 Change MAX8743EEI+ to ISL6269ACRZ-T(PU15) & APL5912-KAC-TRL\_A6(PU16) for layout space

**(2006/06/05)**

P.09 Change R119 2.4K 1% to 2.37K 1% from CRB 1.201a.  
Remove docking function.

**(2006/06/07)**

P.49~51 Modify CardBus chip TI8402 to R5C847  
P.54 Modify LAN Chip RTL8101E-GR\_1.0 to 82562v.

**(2006/06/08)**

P.51 Adding MS card power circuit.  
P.71 Adding Robson circuit.  
P.72 Adding Touch pad circuit.  
P.73 Adding Switch circuit.  
P.100 Adding one extra bit for 3GIO PADCFG strapping  
P.101 Adding one extra bit for PCI DEVID strapping.  
P.102 Adding New 7Os signals, I2CS\_SDA and I2CS\_SCL  
P.103 Adding IFFPAB\_PLLVDD, IFFCD\_PLLVDD, PLLVDD and VID\_PLLVDD power rail change  
P.104 Adding NB8M pin-G23, is H\_PLLVDD connect to 1.2v  
P.105 Adding New feature: FBA\_COM27, NV\_GPIO13, NV\_GPIO14, FBC\_CMD27  
P.106 Adding special circuit for HDMI function  
P.107 Adding Connect HDMI hot plug signal to GPIO  
P.108 Delete External HDMI unnecessary net (single net).  
P.66 Update KB3920 library

**(2006/06/09)**

P.49 Delete R776 from R5C847 damo circuit.  
P.61 Delete power +1\_05VVRUN & +1\_25VVRUN circuite.  
P.05 Del R28 0 ohm for layout space  
P.11 Del R661,R673,R674,R677,R679,R680,R682,R696,R695 0 ohm for layout space.  
P.12 Del R670,R671,R672 0 ohm for layout space.

**(2006/06/12)**

P.35 DelR764,R770~R775,R1931,R758R762,R766,R752,R755,R757,R768,R765 for layout space.  
P.68 Change R1676~R1683;R1692,R1921,R1892~R1895,R1685,R1684 0 ohm 0603 size to 0 ohm 0402 for layout spacing saving.  
P.51 Adding R1844,R1857 0 ohm resistor from vendor suggest.  
P.30 Delete C644,C645 for docking function  
P.20 Change C661 0.47u to 0.33u from R5C847 demo circuit suggest.  
P.38 Adding AV function  
P.38 Delete R681 for layout space.

**(2006/06/13)**

P.57 Change P036,P037 to P065, Change P035,P038 to P064 for layout space  
Modify U125VSUS to +1\_05VSUS to +1\_05VVRUN & +1\_05VVRUN  
P.34 R1936 to NC 0 J,adding R1938 0 ohm for intel LAN w/S0 only support (no WOL).  
P.33,34 Change EC OUT1 output from U31.AH27 to U31.AG14 for debug card to M/B burring issue.  
P.31~33 Remove LVDS\_GPIO circuit.

**(2006/06/14)**

P.35 Change R664 1 F to 0 J from CRB Rev:1.201  
P.06 Change R1844 2.2K to 10K from check list Rev:1\_201a.  
P.50 Change L73 120R-100MHZ\_OR12 to 90R-100M\_0.06R from Vendor FAE suggest.

P.18 Remove R200,R201, because TV MODE strap is no use.  
P.22 Remove R1456,R1457,R1421, because don't need 16M/8M selection strap.  
P.22,23 Remove VRAM address (A2/A3/A4/A5) termination.  
P.23 Remove R1482,R1480,R1493, because don't need 16M/8M selection strap.  
P.22,23 modify FBCLK Termination  
P.68 Modify HDMI circuit  
P.29 Modify semi-pnp circuit  
P.38 Add R1763 and R1764 for NB8M's internal thermal sensor  
P.38 Update MS90 & MS20 GPIO different table

**(2006/06/15)**

P.54 Remove R1971,R1970,TP95~97,TP281,PLT\_RST signal because no supprot LAN disable function.  
P.61 Add PU125:YBCSYSNS8011EL, PR321:1K, PR322:10K,PR323:0,PR324:0,PC217:1UF,PC218,PC219:220PF For battery identify.

P.12 Remove R666~R669 for layout space.

**(2006/06/16)**

P.64 Change PC208 from 0.1u to 0.22u for PU17 reference voltage .  
Change PR300 from 8.87k to 6.49k based on GPU load line spec.  
add PR330:1K for Gnds Offset voltage

P.61 Adding new battery chip(PU125) & EC communicate circuit.

P.20 Change U8 F75383M to G781P8f  
Because thermal-sensor should be same vendor.

P.37 Remove +3VRUN(pin8,9,10) from CN11; adding R1450;  
CN32 Pin3 connect to GND from MOR suggest.

P.43 Adding R1094,R1096 resistor no stuff from MOR suggest.

P.41 Adding C1689,C1690 ; remove R1067 from intel CRB rev:1.201a.

**(2006/06/19)**

P.26 Changy L76 NV\_NB8M\_120R-100MHZ\_0603 to NV\_220R-100MHZ\_0603 for NB8M.

**(2006/06/20)**

P.43 Change U36 TPS2231PWP to TPS2231PW from MOR suggest.  
P.54,33 LAN signal adding R2004~R2009 from MOR suggest.

**(2006/06/21)**

P.61 Add =1\_8RUN discharge schematic.  
P.63 Reserve PR333,PC221 snubber schematic.  
P.58 change PR149 from 8.2K to 7.87K for +1\_05VVRUN level  
P.51 Adding R2010 pull-down resistor from vendor FAE suggest.  
P.52 Move USB port 0 & 1 circuit to Audio & USB daughter board.  
P.44~46 Move Audio circuit to Audio & USB daughter board.  
P.25 Adding CAP32 in NV\_VDD for reduce ripple noise.  
P.05,11,12 Change CAP1,CAP14,CAP15,CAP25 capacitor H=1.9mm to H-1.8mm for ME high limit.  
P.06 Adding U123 Pin4 Pull high 10K ohm to +3VRUN.  
P.71 Change Robson connector Mini card to B to B connector.

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**(2006/06/22)**

P.43 L110 swap for layout convenient.  
P.54,32 Adding U131 for LAN EEPROM circuit.  
P.08 Adding M A A14 & M B A14 connect to P.14 CN1 Pin A14 &  
P.15 CN5 Pin A14 for 2GB Technology and width=8 DIMMs support.  
P.74 Remove AV Function Circuit to switch board.  
P.73 Remove Vol +/- & Mute button circuit to switch board.

**(2006/06/23)**

P.43 CN18 Pin37,40,43 adding 0 ohm to GND for WLAN 3945.  
P.51 Modify MS/SD power circuit change to power switch TPS2055AD form MOR suggest for OCP.  
P.65 Adding H1~H11 screw.  
P.72 Change touch pad switch SW17,SW18 for ME request.  
P.51 Change SD Slot CN58 for ME request.  
P.30 Change CRT connector CN4 for ME request.  
P.72 Change Touch pad connector CN61 for ME request.  
P.43 Change OIDE connector CN21 for ME request.

**(2006/06/24)**

P.08 Delete R1309, because EXTTS1# is no longer multiplexed with DPRSLPVR input.  
P.15 Delete R176, because EXTTS1# is no longer multiplexed with DPRSLPVR input.  
P.43 Put R1094 and R1096 into the left of the pull-up resistor.  
P.65 Add H12~H15 for CPU bracket hole.

**(2006/06/28)**

P.56 Change DC-IN connector PCN1 for ME request.  
P.68 Change HDMI connector CN60 for ME request.  
P.09 Remove R1409, R1410 and +1\_05VRUN for CRT BLUE#/GREEN#/RED# and connect these signals directly to GND from MOR.Crestline design guide Rev:1.0  
P.75 Adding TV tuner circuit.

**(2006/06/29)**

P.34 LAN\_RST#: IMVP\_PWRGD ==> SUS\_PWRGD\_10MS (stuff R1937 ,no stuff R1938).  
P.35 VccLAN3\_3: +3VRUN ==> +3VSUS;VccCL3\_3: +3VRUN ==> +3VSUS. for wake up S3.  
P.31 Inverter circuit adding to LVDS connector.

**(2006/06/30)**

P.57 delete PR138 ,add PR142:0 for getting higher efficiency  
P.61 change PQ51,PQ55 from IRF7807 to IRF7823 FOR low drop out voltage  
P.63 change PR278 from 3.65K to 2.37K FOR NV\_VDD ocp setting.  
P.63 add PQ72:IRF7832Z for NV-VDDP power rating  
P.63 ADD PR334:1K for PEX\_VDD power good .  
P.60 change PQ46,PQ47,PQ49,PQ50 fromsi4856 TO IRF7836 for SI4856 shortage issue  
P.61 PUL25 pin8 change net from BATT\_PR# to BATT\_ID

**(2006/07/03)**

P.61 Delete PR323,PR328,because Identify Battery IC from EC GPIO control.  
P.15 Modify CN5 FOX\_AS0A426\_N4SC\_4F to FOX\_AS0A426-N6SN-7F from ME request.  
P.14 Modify CN1 FOX\_AS0A426\_N4RC\_4F to FOX\_AS0A426\_N6RN\_7F from ME request.  
P.31 Reserve R1272 for Intel Crestline Rev:A01 brightness no output issue.

**(2006/07/04)**

P.51 Adding R1858~R1865 0 ohm resistor from vendor suggest.

**(2006/07/05)**

P.38 Change R1762 0 ohm to 1K ohm for protect EC output when powr protection circuit work.

**(2006/07/06)**

P.31 CN3 LVDS signal swap for layout convenient.  
P.75 Remove TV Tuner Circuit for meet MS90 SPEC.  
P.31 Remove C641/C643 EMI confirmation.  
P.33 U31A Pin E6 adding TP237.  
P.12 Adding 0 ohm 0805 resistor +VGFX\_CORE connect to +1\_05VRUN from intel sighting report(Rev:8)  
specification THERMTRIP# signal stays at an intermediate level of 680~700mv.

**(2006/07/07)**

P.38 Modify system ID R717 no stuff ; R716 stuff.  
P.16 RP12,RP14~21 Pin3 & Pin4 swap for layout convenient.  
P.16 CN5 pin5 & pin4 Swap for layout convenient.  
P.15 Swap CN1 signal for layout convenient.

**(2006/07/10)**

P.51 Change CN58 SD slot to WK21923-S6P-7F from ME request.  
P.54 Move LAN Transformer circuit to Switch Board from ME suggest.  
P.22,23 Swap U11,U12,U13,U14 Data signal for layout convenient.

**(2006/07/11)**

P.33 Add TP599,TP600 test point for BGA package.  
P.57 Change PL5 to PLC-0755-100 for layout space.  
P.38 Add R2023,R2024 pull high 2.2K resistor for SW modify EC GPIO table.

**(2006/07/12)**

P.65 Change screw H1~H11,H16~H18 fro ME request.  
P.49 Add R2025~R2027 0 ohm resistor for leakage current from R5C847 to MS, SD and PCI signals while Vcc was ramping up issue.

P.51 Move R2011 connect to SD PWR\_CTRL,R2012 connect to MC\_PWR\_CTRL\_0 from MS70 RD.resistor should be place EN# not output.

**(2006/07/13)**

P.35 Update ICH8M Current Rating.  
P.22 Add "NV\_" for R1996, R1997, R1998, R1999.  
P.23 Add "NV73\_" for R2000, R2001, R2002, R2003.  
P.25 L95, C422, C424, C1422 change from "NV73" to "NV".  
P.26 Add "NV\_" for CAP32, remove R1544 and add TP for A26.  
P.27,28 Add VRAM location description and modify "NV\_" and "NV73\_".

**(2006/07/14)**

P.16 Swap DDR signal (Pull high resistor) for layout convenient.  
P.43 Change CN20 CAM connector for layout placement.  
P.54 Add CN16 WTB (Switch Board) M/B for layout placement.  
P.44 Add CN66 Audio BTB connector for layout placement.  
P.26 Add 0 ohm resistor R2028 for G73M using.  
P.44 Add R2091,R2030 0 ohm connect to CN66.3,4 from MOR.

**(2006/07/14)**

P.30 Change CN65 to FOX\_DZ11A91-MW222-4F from ME request.  
P.38 Change CN12 to FOX\_GB20240-0001-7F from ME request.  
P.50 Change CN23 to FOX\_UV31413-RU81P-7F from ME request.  
P.17,P19~21,P24~26 Change U7 Symbol to G73M\_B01.

**(2006/07/17)**

P.44 Change JPSK1 to FOX\_HS8204E from ME request.  
P.08 Add 1 pair LVDS DATA3 for 8-bit support form MOR request.

**(2006/07/18)**

P.53 Change U131 to SST25VF512A,add R2031~R2032 from demo circuit.  
P.31 Change CN3 LVD Connector to FOX\_GS13307-11230-7F from ME request.  
P.04 Add THERMAL PROTECTION circuit from Thermal team suggest.  
P.56 Change PCN2 battery connector to FOX\_BP9107A-B2013-7F from ME request.

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**(2006/07/19)**

P.43 Change CN20 to FOX\_HS8806F from ME request.  
P.29 Change CN6 to FOX\_MH11741-BF3N-4F from ME request.  
P.54 Change U131 power net +3VRUN to +3VSUS\_LAN;  
add C1691,C1692 0.1u from CRB circuit.  
P.40 Delete CN44 of original switch board connector.  
P.20 U82 change from NC to mount.  
P.20 Change off-page connection for R1995 pin2 from  
NV\_HDMI\_DET5 to NV\_HDMI\_DET3. (Level shift)  
P.68 Add R2034, R2035, Q158 for HDMI I2C Level Shift  
P.41 Change CN18 to FOX\_AS0B226-R66N-7F from ME request.  
P.52 Change CN29 to FOX\_UB1112C-CA501-7R from ME request.  
P.07~13 Update U112 parts change signal name(U112.C48,D47,BJ29,BE24)  
for Crestline chipset EDS 1.0

**(2006/07/20)**

P.22,23 Update FB\_CLK termination circuit for layout issue.  
P.41 Del CN39 MINI Socket from ME request.  
P.30 Change CN65 to FOX\_DZ11A91-MA222-4F from ME request.  
P.20 Change U82 value EEPROM\_SOIC-8\_8 K to NV\_EEPROM\_SOIC-8\_8 K of nVIDIA use.  
P.49~P51 Change Card read circuit R5C847 to TI8402 from MOR.  
P.06 Add CLK\_CB48 signal for TI8402.  
P.65 Update Screw hole from ME request.  
R231,R232,R277,R279,R280,R282,R2028,PD18,PC162~PC164,PQ9A,PR230,PR241,  
PR246,PR250,PU10 change value to NV73\_\*  
R279,R281,R283,L76,C347,C1194 change value to NVNB8M for BOM.  
P.23 U13,U14 signal swap for layout convenient.  
P.32,34 RP95,RP101 signal swap for layout convenient.  
P.06 Swap RP11 for layout convenient.  
P.43 Swap L69 for layout convenient.  
P.22,23 Change C1693~C1696 value 0.01U\_16V\_K to NV\_0.01U\_16V\_K for nVIDIA chip.  
P.32 Add U31.C10 test point TP202 of BGA chip.  
P.30 Add R486,R488 0 ohm for EMI request.  
P.31 LCDVCC Add C1728 pull down for EMI request.

**(2006/07/21)**

P.31 Swap CN3 signal for layout convenient.  
P.54 Remove R2031 because resistor need close ICH8 from CRB.  
P.38,44 Change INT\_MIC\_DET to INT\_MIC\_DET# this signal is low active.  
P.38 Add R718,R2077 0 ohm of +ECVCC.

**(2006/07/24)**

P,32~36 Update U31(ICH8) Symbol.  
P.42 Change Q96 to ME2301T1,because MMC2301 EOL.

**(2006/07/25)**

P.42 Change U79 Si9183DT-33-T1-E3 to G914Df for convenient order.  
P.59 Change PQ44 from IR7832T to IR7832Z for convenient order.  
P.60 Change PC214 from vender:SANYO to MATSUSHITA for convenient order.  
P.56, P.62 Change PQ30,PQ58 from diode 2N7002 to diode 2N7002EPT for convenient order.  
P.64 Reserve PR291, ADD PR335:0 for modify GMCH power enable from +3SUS to DEGT\_VREN  
P.61 Change PC218,PC219 value to NC\_\* for Identiy battery IC.  
P.38 R2023,R2024 change 2.2K to 1K for Identiy battery IC.  
P.65 Modify screw hole for ME request.  
P.03 Remove PR176 from MOR,because OVT\_EC# has two pull-ups.  
P.06 Change R68 12 ohm to 22 ohm from Intel's recommended.  
P.08 Change R109 0 ohm to 100 ohm 1% from CRB.R1929,R1930 to NC from Design guide.  
C96,C97,U5,R112,R115 change value to NC.  
P.11 Remove L119,L121 from CRB.Remove D5,R665 because D5 & D6 are same function.  
P.12 R1961 change value to NC.CAP14&15 to CA\_.

**(2006/07/25)**

P.16 Add 2 resistor(R2078,R2079) for M\_B\_A14, M\_A\_A14.  
P.20 Change Y2 value to NV\_  
Change U7 Value GF-GO7600-H-N-B1\_B1 to NV\_GF-GO7600-H-N-B1\_B1 for nVIDIA.  
P.68 CN60,U128 value add NV\_\*.  
P.65 Add H22 & H23 for DXF 0724.  
P.72 Add SD LED Function for MOR request.  
P.44,49 Delete CB\_SPKOUT# signal because Since there isn't CardBus slot,  
CB\_SPKOUT# is unnecessary from MOR.  
P.38 R718.1 change +ECVCC to +ECVCC\_L for power plane convenient.  
P.66 U130 +ECVCC change to +ECVCC\_L for power plane convenient.  
P.66 Add TP308,319,320,321~329 test point for BGA chip.  
P.29 Change D60, D61, D81 value NV\_SM05.TCT to SM05.TCT.  
R1546 NV\_2.2K to 2.2K from MOR.

**(2006/07/26)**

P.56 Remove PU124 because the function same Q149.  
P.37 Change CN32 ODD connector to FOX\_QT8H0506-E111R-9F ME request.  
P.68 Change U128 value NV\_RClamp0514M to NC\_RClamp0514M from EMI request.  
P.51 SD,MS clock reserve 22P(C1729,C1730),MDC clock add 33P(C1731)  
from EMI request.  
P.44 JSPK1 add 0 ohm resistor(R2080~R2083) fro EMI request.  
P.37 Add VR1 for EMI request.  
P.37 Remove C791,C792.because HDD no +3VRUN power.  
P.41 Remove R760,R761,add L158,L159 from EMI request.  
P.56 PD6.1 connect to BATT\_ID from MOR suggest.  
P.31 Resereve the FET at discharge circuit from MOR suggest.  
P.68 Resereve R2084 HDMI +5VRUN connect U128.3

**(2006/07/27)**

P.20 Change U82 description & value2,HH P/N no modify for convenient order.  
P.38,66 Delete APR\_AMP\_MUTE for docking function.  
P.66 Delete TP321~329, TP305, TP309 for layout spacing issue.  
P.66 OVT\_EC --> GPIO11, DAT 35001 -->GPIO48,  
CLK\_35001 --> GPIO49, 35001\_RST# -->GPIO43 for SW suggestion.  
P.66 A4003 -->GPIO7 for SW suggestion  
P.66 INT\_MIC\_DET#\_R --> GPI\_3B/AD#, SPK\_MUTE\_EN\_R --> GPIO9  
P.38 Change CN12 KB connector same MS60 from ME request.  
P.71 Add C1389,C1394 for EMI request.  
P.54 Add C1395 for EMI request.  
P.44 Add C1396~C1698 for EMI request.  
P.43 Change C849 value to stuff for EMI request.  
P.72 Change LED11(power LED) to HT-297-UD-UYG for ME request.  
P.29 Remove R1686, R1687, R1688, R1689 because no use.  
P.20 Remove R301,R1819 because no DVI function.

**(2006/07/28)**

P.54 Change CN16 to FOX\_QTS0030A-1021-9F for ME request.  
P.65 Add BOSS1~BOSS4 for MDC & MINI CARD for ME request.  
P.63 Change PC198,PC196 from 1210size to 1206 sizefor  
1210 size shortage issue.  
P.60 Change PC123,PC130 from 0402 X5R to 0603 X7R

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**(2006/07/31)**

P.54 Delete CN16.KSI0,Mute\_LED,Mute\_button signal, add KSI1 for Switch Board.

P.6, P.20 For Clock Gen Co-layout for 9LPR358, Change value R1946 to "CA\_10K\_J" and R2085 to ""NV\_10K\_J; Change RP109.1 to "DOT96#" & RP109.2 net to "DOT96"; RP9 for DOT96, RP109 for nVIDIA PCIE CLK; RP10 for GMCH "DREFSSCLK", R2086,R2087,R2088,R2089 for nVIDIA 27M Hz option.

P.6 Swap RP11 for Layout smoothly.

P.71 CN64 swap pin for differential Layout rule.

P.20 Change components value to "NC \*" for 27M Hz of nVIDIA from CK505 - Y2,C492,C493,C494,C495,R316,R317,R3T9,R320,R321,U10.

P.34 Add C1732 for IMVP\_PWRGD glitch in MS10.

P.26 Remove R262 0 ohm for layout space.

**(2006/08/01)**

P.42 Q151 Change ME2301T1 to SI2301BDS-T1-E3 for MS70 FAN issue.

P.24 Change Q96 ME2301T1 to SI2301BDS-T1-E3 for convenient order.

P.38,62 Delete MUTE\_LED,MUTE\_SW# signal.

P.31: U17 change to G5281 (H.H P/N: 15-G5281RC-V000) For LCD Panel timing concern.

P.68. F3 change to (H.H P/N: 1M-F006A35-F000) For HDMI over-current protection.

P.68. Add Diode D109 on HDMI\_+5VRUN1 MOR request for reverse current protection

**(2006/08/02)**

P.06 Swap RP9 pin for Layout convenient.

P.51 Move MDC connector to P.44 for function BOM.

P.65 Delete H1,H8,H22,H23.

P.44 Change CN66 to QTS0040A for ME request.

P.34 Change U33 to 74AHC1G14GW for order convenient.

P.31 Add CN67 inverter connector HS8806F for ME request.

P.31 Modify CN3 LVDS connector pin define.

P.03 Move CPU Thermal-Sensor to Page 45 for function BOM.

P.20 Move VGA Thermal-Sensor to Page 45 for function BOM.

P.04 Move HW THERMAL PROTECTION circuit to Page.45 for function BOM.

P.61 Delete H5 for ME request  
[Modify circuit page for Function BOM.](#)

**(2006/08/03)**

P.20 Add R2090, R2091, R2092 for XTALIN signal level divided (3.3V -> 1.2V)

P.63 Change CN60 to FOX\_QJ5119C-NT03-4F for ME request.

P.06 Change U123 to ICS9LPR358YGLFT for add 27Mhz clock.

**(2006/08/04)**

P.05 Add C50~C59 22U\_6.3V from IMVP-6 VR Specification Rev:1.2

P.31 Change CN3 LVDS connector to FOX\_GS13207-11230-7F from ME request.

P.11 Add C852~C854 0.1U\_10V for better power signal.

P.31 Change R1268 value to NC\_0\_J,R1272 to CA\_0\_J for ES1 chip.

P.31 Reserve R1273 for checking NV\_LCDVCC\_EN# can be active\_High.

P.42 Delete R28,CN20.5 this GPIO net for camera on or off control, camera module not support.

P.56 Add PC22:0.22U 0603 for solving adaptor plug in/out issue

P.64 change PU17 pin 31 enable from +3VSUS to GVR\_VCC,and add PR291 :100K 0402 ,delete PR335

P.64 add PR311,PR312,PR313: 0, PR308:8.2k for chip set initial vid setting

P.64 add PU17 pin 31 enable signal:PM\_SLP\_S3#

P.60 change PC117,PC118,PC132,PC133 from 330u 2v 9 m to 330u 2v 6m and delete PC120 based on INTEL requirement

**(2006/08/07)**

[Modify page number \(remove P.65\) for Function BOM.](#)

P.35 Remove description for "No use integraed Lan"

P.31 Add Panel ID Table

P.56 Change PR245 value to CA\_100\_J.

P.05 Add C60,C61 22U\_6.3V from IMVP-6 VR Specification Rev:1.2

**(2006/08/07)**

P.51 Add PC46 BATT\_ID signal of ESD.

P.51 ,57 modify PR109 from 7.15k to 10k,PR261 from 31.6K to 280K, PR264 from 10k TO 110K, PR265 from 41.2k TO 110K, PR270 from 10K to 33K due to the ACIN OCP point is 5.077A for 90W,PWRLIMIT point is4.15A

P.55 modify PR198 11.5K to 13.3k for ocp setting

P.55 leave PC223

P.26 Change D108 value to NC\_BAT54S-LF because no external SPDIF port support.

P.06 Delete R\_DOCK\_SATA\_AND\_LAN\_CLKREQ# signal of docking function.

**(2006/08/08)**

P.43 Add CN13 for Sub Woofer function.

P.56 Change PC217 value to NC\_1U\_10V\_K from MOR.

P.41 Change CN20 to FOX\_HS8804F from ME request.

P.34 Change R767 value NC\_3.24K\_F to 3.24K\_F;R744 3.24K\_F to NC\_3.24K\_F for WOL support.

P.64 CN61 mirror vertically for touch pad module define

P.41 Change CN20 Pin define for Camera module.

P.34 Remove SMB\_LINK\_ALERT# pull high from CRB Rev:1.301.

**(2006/08/09)**

P.34 Add R752,R754 8.2K ohm pull-high to +3VRUN from Intel check list suggest.

P.43 CN66 mirror vertically for layout convenient.

P.37 Change CN11 to LD2722F-S499 from ME request.

P.37 Change VR1 to MS06A05T1V1\_VR of ESD.

P.51 Add PR340:23.2K for 75W CP setting

P.57 Add PR341:360K for 75W ACIN OCP setting

P.51 Add PR342:130K for 75W PWRLIMIT setting ; change PR265 from 110k to 102k for 90W PWRLIMIT SETTING

**(2006/08/10)**

P.43 Swap CN66 pin for layout convenient.

P.38 Add Q107 and R712 NC for RTC can't count issue has new solution.

P.34 C1732 change to NC for RTC can't count issue has new solution

**(2006/08/11)**

P.43 Swap CN66 pin define for Audio Board.

P.12 Add R49 history from Intel sighting report version:11

P.44 Change D100 value to NC\_SSM22LLPT of leakage issue.

P.25 Change CAP12 to NV\_150U\_6.3V\_T for VGA chip.

P.26 Change C317 value to NV\_4.7U\_10V\_Y\_Y of VGA chip.

P.21,22 Change U11,U12,U13,U14,R1411,R1416,R1492,R1481,R1499,R1498,R1500,R1501,R1483,R1496,R1495,R1494,R1497,C1401,C1402,C1403,C1404 value NV73\_\* to NV\_\* Because NB8M use too.

P.27 Change C510~C518,C1590~C1595,C524,C525,C540~C548,C554,C555 value NV73\_\* to NV\_\* because NB8M use too.

P.06 R1951 change to NC\_10K check list do not have this rule.

P.61 U130 Change to KBC3925 for SPI EC.

**(2006/08/14)**

P.06 Remove R1951 from CLK GEN FAE suggest.

P.06 Add R1963,R1962 475\_F on U123 Pin33,44;R1162 move to P.06 change to 475\_F from CLK GEN FAE suggest.

P.49 Delete CN16 pin6,8 because switch board not have power led & suspend led.

P.51 Change PR87 1K\_F to 20K\_F for OVP issue same MS60.

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(2006/08/15)

- P.30 Change CN65 to DZ11A91-MW223-4F for ME request.
- P.60 Change BOSS1,BOSS2 to A40M20\_31BS from ME request.
- P.26 Change CAP32 to 470U\_2.5V for Layout ME high limit.

(2006/08/16)

- P.41 C1322,F2 change to stuff,C1314,U122 change to no stuff same MS11 camera solution.
- P.29 Remove D81.D81 pin2 B\_SVD\_DET# move to D61 pin2 from EMI RD suggest.
- P.31 Change CN3 LVDS Connector to FOX\_GS13307-11230-7F because materiel shortage.
- P.03 Change Q4 to 17-MMBT390-4001 for order convenient.
- P.51 Update PCN2 orcad symbol.

(2006/08/17)

- P.49 Remove R2032,R2033 from Intel 965 rev:1.1 SPI General Routing Guidelines.
- P.51 ADD PR343 for changing PQ73 from TR to MOS
- P.51 Update PCN2 footprint.
- P.63 Change CN64 to NC\_B TO B CONN\_20P because EVT Robson function no use.
- P.37 Remove TP572 for layout space.
- P.64 Change LED12~14 HT-110Y to HT-170UY for ME request.
- P.40 Change LED10 HT-110UYG to HT-170UYG for ME request.
- P.41 Change LED9 to HT-170UYG for layout placement.
- P.51 PCN2 mirror vertically for layout convenient.
- P.52 Reserve PC224,P.34 add D110 for autio power on issue.

(2006/08/18)

- P.60 Add H22~H26 (NPTH) for ME request.
- P.41 Change LED9 to HT-170NB5 for ME suggest.
- P.49 Change CN16 to FOX\_GS12301-1011A-9F from ME suggest.

(2006/08/19)

- P.49 Swap CN16 pin for layout convenient.
- P.49 Add R2093,R2094 pull high resistor from Intel FAE suggest.
- P.49 Swap CN16 pin25,26 & 27,28 for layout convenient.
- P.30 R486 pin1,2 signal wap;R488 pin1,2 signal swap for EMI suggest.

(2006/08/24)

- P.12 Remove R49,add R1961 from Intel design guide Rev:1.0. for disable internal VGA.
- P.11 R4 change to 0 ohm avoid +V3.3S\_HV voltage drop.

## [DVT]

(2006/08/25)

- P.47 Update U134,U135 symbol.Change TPS2055 pin4 from EN# to EN because schematic part error different data sheet.
- P.48 Change CN29 Value FOX\_UB1112C-CA501-7R to FOX\_UB1112C-CA501-7F Because F---lead free.

(2006/08/28)

- P.50 Power Design Diagram modify PEX VDD from 2A to 1.61A NV\_VDD from 16A to 14.7A,remove +1\_25VSUS/1.5A for Power\_Budget update.

(2006/09/12)

- P.60 Change BOSS3,BOSS4 for new mini card connector.
- P.37 Change VR1 to MLVS0603M04\_VR because ODD ESD test fail.
- P.12 Remove R1961,add R49 for PM\_THRMTRIP# no enable issue.
- P.31 Remove Q10,R459 add R1273 because U17 is active high.
- P.49 Change U131 to MX25L8005MC-15G original SPI flash density 64KB is too small.
- P.55 Change PC137,PC142 0.22U\_10V to 0.22U\_6.3V PC124 to 0.015U\_16V\_K for order convenient.

(2006/09/25)

- P.11 R4 Change to 10 ohm +3VRUN connect to R4 pin2 from Intel CRB.

(2006/10/02)

- P.63 Change C1389,C1394 to NC\_\* ,Robson function not support MS90.

(2006/10/11)

- P.49 Modify CN16 pin define because it's too many. some GND can be NC - Pin1, 2, 17,18, 19. Because we only have 2 pins of power. Then we only need 22 pieces of cable.
- P.47 Reserved BJT circuit for power switch materiel convenient.
- P.44 Change R1923 from 1K to 0 ohm for FAN spin up noise.
- P.43 Delete CN13 because Sub Woofer function not need MS90.
- P.63 Change CN64 to MATSUSHITA\_AXK5F20545YJ from ME request.

(2006/10/12)

- P.41 Change OIDE & Camera power from +5VRUN to +5VSUS for vista

(2006/10/13)

- P49 Add SUS\_PWRGD\_10MS net to U125 for Intel FAE suggestion.
- P.31 Change LVDS connector to FOX\_GS13207-11230-7F for ME request.
- P.63 Modify CN64 pin define for layout convenient.
- P.52 Modify PR125 from NC to 6.95k;PR127 from 0 to 10K for changing 3.3V from to reserve if system need.But the adjustable voltage is the same as the original 3V/5V value.
- P.52 Modify PR126 from NC to 16k;PR129 from 0 to 10.2K for changing 5V from fixed to adjustable
- P.54 change SC486 solution toTPS51116 solution for common solution as MS70 and material convenient
- P.55 change PC138 from 0.033u to 0.068u for decrease transient
- P.56 change PQ51,PQ55 from IRF7823 to FDS8880,change PQ6 from NV\_IR7836 to NV\_FDS8896 for material convenient
- P.59 Add debug resistor PR353:0 ; change PQ62 from IRF7413Z to SI4800B for material convenient
- P.58 Add debug resistor PR276:0 ; change PU15 from ISL6229A to ISL6228 for material convenient
- P.56 Change +5VSUS/+3VSUS from 1.2A to 1.6A for HW require

(2006/10/16)

- P.41 Remove U122,C1314 because Camera is internal USB current limit small not need power switch current support 1.1A.
- P.03 Reserve U136,R2101,C1733 for RTC stop issue.
- P.38 Add R2099,R2100 for RTC stop issue.
- P.38 Reserve D111 for RTC stop issue.
- P.60 Remove BOSS3 for ME request.

(2006/10/19)

- P.38 Add PC241:2200PF 50V for EMI require.
- P.51 change PQ25,PQ26,PQ27from SI4835B to AO4433 for material convenient
- P.58 Change PQ60 from IR7832 to FDS8880 ;change PQ61,PQ72 from IR7836 to FDS8896 for material convenient

(2006/10/20)

- P.18 Remove R244 for nVidia crystal setting update.
- P.18 R242 and R239 change from NC to NV for nVidia strap update.
- P.6,32,49 Change LAN solution from 82562V to 88E8036.
- P.64 Remove MS LED circuit & add R2036.Because ME suggest integrate MS & SD LED.
- P.64 Add R1983 for Touch pad change.from 0 to 180 degree.
- P.53 Change PQ40 from SI4800B to FDS8880 ;change PQ42 from SI4810B to FDS8896 Change PL11 from PCMC063-2R2MN to MPO1R5 ,change PR148 from 18.7k to 10k for upgrade 1.05v rating for reserve GPU power combine to 1.05V

(2006/10/23)

- P.35 VCCCL3\_3 and VCCLAN3\_3 change from +3VSUS to +3VRUN for no integrated lan.
- P.33 Delete GLAN\_DOCK#, ICH8M library update.
- P.34 ICH8M LAN RST# connect to GND when no integrated lan.
- P.30 Add F6 for CRT +5V power.
- P.44 Add R2116,remove C49 for HW UL Lock abnormally issue.
- P.30 Change F6 value to FOX\_HS8108E.
- P.64 LED11 pin1,2 & pin3,4 swap because color error.

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**(2006/10/24)**  
P.64 Remove D101~D103.Add VR6~VR8 from ESD suggest of layout convenient.  
P.43 Remove R2080~R2083.Add L77~L80 from EMI suggest.  
P.43 Remove D68,D69.Add VR2~VR5 from ESD suggest of layout convenient.  
P.60 Add BOSS5 for Robson.

**(2006/10/25)**  
P.37 Reserve R991,R992.Add R993,R994 pull-up +5VRUN.  
Because optical drives have internal pull-up resistors to 5V.  
P.06 Change R1947 & R2103 to 475 ohm from checklist.  
P.58 Add PC242:2200PF\_0402,PR333:4.7\_0603,PC221:680P\_0603 for EMI required  
P.59 Add PR355:0\_0603 debug resister

**(2006/10/26)**  
P.42 Add Q166 for Express card sequence issue.  
P.64 Remove R780 because LIDIN# have pull up +ECVCC.

**(2006/10/27)**  
Remove component for G73M.  
P.18 Reserve R203~R210 because VRAM indefinite.  
P.56 deletePR24,change PQ9 from 2N7002DW to 2N7002EPT,delete PU10,PC162,PR230,PC163,PC164  
for NV8M no need +2.5Vrun  
P.57 delete PR246,PR250,PD18 for NV8M no need +2.5Vrun

**(2006/10/30)**  
P.60 Add H27 for WLAN switch from ME request.  
P.41 Change C1085,C1087 to NC\_\* from MS90 EVT PI simulation report.  
P.12 Change CAP15 value CA\_330U\_2V\_7343 to NC\_330U\_2V\_7343 for PI simulation report.  
P.11 Remove CAP25 PI simulation report.  
P.12 Add OPEN\_JUMP PJ13,remove R49,Add R1961 from guideline for internal GFX disabled.  
P.14 Change CN1 to AS0A426-N5RN-7F from ME request.  
P.15 Change CN5 to AS0A426-N5SN-7F from ME request.  
P.31 Add reverse circuit for NV\_LCDVCC\_EN#.

**(2006/10/31)**  
P.41 Change CN36 to AXK5F10547YG for new bluetooth module.  
P.09 Change R1948,R1949 value to CA\_2.2K\_J;Add R1242,R1243 from design guide.  
P.27 Delete D60 add VR9 from EMC suggest.  
P.51 PD7,PD8 change to PESD5V2S2UT from EMC suggest.

**(2006/11/01)**  
P.34, 38 NC R2100, R2099, Q107, mount R656, R712 for MS32 RTC timer stop solution.  
P.42 Add R1098,reseve R1099 for express card time issue.  
P.44 Add D112 because Thermal-Sensor should not floating.

**(2006/11/02)**  
P.40 Change value RP34 to NC\_\* because MS90 doest not support NetDetect.

**(2006/11/03)**  
P.48 Change CAP18 to 6TPE150MPC2 for ME high limit.  
P.44,56 Change C1521,PC150 from 0.047U\_16V\_M to 0.047U\_16V\_K for PUR convenient.  
P.56 Change PC159 from 0.47U\_6.3V\_M to 0.47U\_6.3V\_K for PUR convenient.  
P.59 Change PC210 from CA\_2200P\_50V\_M to CA\_2200P\_50V\_K for PUR convenient.  
P.59 Change PC208 from CA\_0.22U\_16V\_K to CA\_0.22U\_16V\_K for PUR convenient.  
P.58 Change PC221 from 0603\_NPO to 0603\_X7R for PUR convenient.  
P.55 Change PC140 from 120P\_50V\_J to 120P\_50V\_J for PUR convenient.  
P.59 Remove PR355,PR291 for internal GFX disabled.  
P.49 Add +2\_5V\_AVDD\_LAN on CN36.20 for switch board LAN function.  
P.49 Change U138.47 to +3VRUN for wake-up LAN function.  
P.42 Change U36 to BD4154FV for Express card Short Mode Test Fail issue.  
P.33,34 Update 2 pin name by ICH8M EDS update.  
P.26 Change U7B.T13 power from PEX\_VDD to NV\_VDD because NV\_VDD for NB8x.  
P.47 Change R2058,R2062 from 1M to 100K ohm from MOR suggest.  
P.42 Reverse C1754-C1760 from MOR suggest. effective against the noise of  
lseg-TV bandwidth.  
P.24 Change R283 value NVNB8M\_0\_J to NV\_0\_J for high only.

**(2006/11/03)**  
P.17 Remove R197 from MOR suggest.  
P.19 Add R2118,R2119 pull-high to +3VRUN from MOR suggest.  
P.24 Remove R281,R283,R279 from MOR suggest.  
P.33 Change C743 from 1U\_25V to 1U\_6.3V from MOR suggest.  
P.34 Change C799 0.1u\_10% to 0.1U\_16V from MOR suggest.  
P.62 Add D113,D114 from MOR suggest.  
P.58 Change PL15 value from 1.0UH\_30A\_0.003R to NV\_1.0UH\_30A\_0.003R  
becausePL15 for NVIDIA only.  
P.31 Reserve R2120 from MOR suggest.  
P.52 Reserve PR356,PR357:0 on bootst portionfor EMI  
P.53 Reserve PR358,PR359:0 on bootst portionfor EMI  
P.53 Reserve PR360:0 on bootst portionfor EMI

**(2006/11/04)**  
P.59 PJ12 change to new OPEN\_JUMP 1X-JUMP000-0011  
P.12 PJ13 change to new OPEN\_JUMP 1X-JUMP000-0011

**(2006/11/06)**  
P.44 Change R2116 to 10 Kohm,reserve Q167,R2121 for  
HW UL\_Lock abnormally issue.  
P.49 Add OPEN\_JUMP PJ10 by PE request.  
P.44 Add R2122 for option U:\_Lock solution.  
P.62 Remove D113,add R466 from vendor suggest.  
P.61 Some mistake on SPI interface U3.2:FLAD2 -->FLAD1 U3.5:FLAD1-->FLAD2

**(2006/11/07)**  
P.41 Change CN36 pin define BT\_CHCLK to pin2.Pin3,6 NC,BT\_PR# to pin #5  
delete PLT\_RST# from MOR.  
P.54 Change PR347 to 10k,because 1.8v OCP to 16A  
P.41 Swap L86 for MOR suggest.  
P.31 Update LCDID Table  
P.29 U108 to NC,R542 stuff from MOR suggest.  
P.44 Add R2127 option R for ALW\_ON. R2122 to NC.

**(2006/11/08)**  
P.29 Change R1546 value 2.2K\_J to NV\_2.2K\_J for high only.

**(2006/11/09)**  
P.30 Change R1148 and R1149 from 0 ohm to 39 ohm  
for CRT V-sync and H-sync overshoot and undershoot issue.

**(2006/11/10)**  
P.18 Update R203 ~ R210 for VRAM Strap  
P.26 NC C1193 for NB8P power on issue.  
P.61 Change R2126 from NC\_100K to NC\_4.7K for EC HW strap pin.

**(2006/11/13)**  
P.07~13 change U112 to 12-CRESTL1-ES03 for ES2 P/N

**(2006/11/15)**  
P.11 Change L120 to 0 ohm resistor for Voltage Drop fail issue.  
P.11 Change L6,L10 from 1uH to 0.39uH because 1uH rated current small.  
P.06 Change CAP32 value 470U\_2.5V\_7343 to NV\_470U\_2.5V\_7343  
for NVIDIA chip only.  
P.20 Change R1775 to NC\_100 due to VGA Thermal-Sensor add D112.

**(2006/12/05)**  
P.18 Update VRAM Strap pin  
P.27 Add title "NV128bit\_" for cap of 128-bit VRAM configuration.  
P.31 Update LCD panel configuration  
P.23 Add title "NV128bit\_" for 128-bit

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**(2006/12/06)**

P.31 Delete R1272,stuff R1268 for Crestline ES2 Sample.  
P.58 Change PR277 value from 0\_J to NV\_0\_J for high board only.  
P.62 Change R466 value from 0\_J to NV\_0\_J for high board only.  
P.31 Change CN32 to FOX\_QT8H0506-E115R-9F from ME request.  
P.62 Change CN60 vendor P/N from FOX\_QJ5119C-NT03-4F to FOX\_QJ5119L-NT03-4F from ME request.

**(2006/12/07)**

P.46 Change CN23 from UV31413-RU81P-7F to UV31413-GU81P-7F fro ME request modify connector color.  
P.48 Change CN29 from UB1112C-CA501-7F to UB1112C-CA511-7F for ME request modify connector color.  
P.29 Change CN6 from MH11741-BF3N-4F to MH11741-GF3N-4F for ME request modify connector color.  
P.37 Change CN11 from LD2722F-S499 to LD2722H-S49L fro ME request.  
P.30 Change CN65 from DZ11A91-MM223-4F to DZ11A91-MA224-4F for ME request modify connector color.  
P.11 Change R4 value from 10\_J to CA\_10\_J for low board only.

**(2006/12/18)**

P.25 Change R1900 from 49.9Ω to 40.2Ω; R272 from 40.2Ω to 30Ω for Update frame buffer calibration resistor to fit with NVIDIA NB8M-PUN.  
P.58 Change PR283 from 2.05KΩ to 2.43KΩ for Update NVVDD voltage level from 1.1V to 1.2V to fit with NVIDIA NB8M sampling notice.

**(2006/12/19)**

P.23 Change R1411,R1416 value from NV\_240\_F to NV128bit\_240\_F for VRAM 128bit only.

**PVT**

**(2006/12/20)**

P.49 Move CN16 Pin20(+2.5V\_AVDD\_LAN) & Pin21,22(+3VALW) to Pin19~21 for avoid power & GND damage.  
P.41 Modify CN21 pin define for ME Assembly issue.

**(2006/12/21)**

P.51 Change PR82,PR99 footprint from 2512 to 2512\_h37 for SMT request.  
P.63 Change CN64,C1389,C1393 to NC\_ for remove ROBSON function.

**(2006/12/22)**

P.44 Add U139, C62, R2031, R2032, R73 for DDR local thermal sensor.  
P.20/44 Modify NV\_GPIO8 original connection to NV\_GPIO9 for NB8x internal thermal sensor AP.

**(2006/12/26)**

P.41 Change CN36 to FOX\_QT510106-311H-7F for ME request.

**(2006/12/27)**

P.30 Change CN65 to DZ11A91-MA223-4F from ME request.

**(2006/12/27)**

P.53 Change PR145 from 10K to 100K,add PC243 100P for glitch disapper

**(2006/12/28)**

P.20 Add R1059 for NV\_GPIO8 pull up to +3VRUN.

P.20 Remove R2005 and TP115

**(2006/12/29)**

P.08~10 Add some signal for Crestline rework yield.add U112.P36,P37,R35,AR12,AR13,AM12, AM36,AL36,AM37,BJ20,BK22,BF19,BH20,BF23,BG23,BC23,BD24,B44,C44,A35,B37,B36,B34,C34, C21,C23,F23,G23,R24,L23,J23,E23,E20,K23,M24,BJ51,BK51,BK50,BL50,BL49,BL3,BL2,BK1,BJ1 ,E1,A5,C51,B50,A50,A49,BK2,L43,AY20,AY18

**(2007/01/02)**

P.59 Remove PR295,PC203,PC199,PC200,PC201,PQ62,PQ63,PL16,PR296,PC205,PC206,PR331,PR289, PR290,PC204,PC210,PC209,PR292,PR293,PR300,PC211,PR301,PR330,PR303,PC213,PR305,PR304, PC212,PR299,PR298,PR297,PC208,PC207,PR294,PR339,PR335,PR291,PR288,PC202,PU17 due to remove GMCH regulator

P.26 Add R2129, R2130 for HDMI audio noise backup solution.

P.34 Add R755 for Intel checklist 6.15, CPIO10 should be pull-up 10-K Ohm to VccSUS3\_3

P.32 Change C730,C735 to NC\_0.1U\_16V\_M\_B for remove ROBSON function.

P.51 Change PCN2 vendor P/N to BP91077-B2013-7F from ME request.

P.44 Add TP914,TP915 of CPU Thermal-Sensor.

**(2007/01/04)**

P.25 R1900: 40.2 ohm -> 45.3 ohm; R272: 30 ohm -> 24.9 ohm by nVIDIA reference schematic update.

**(2007/01/09)**

P.59 Delete PR301 due to remove GMCH regulator.  
P.03 Remove R7 add close jump(GP1) of common project using.  
P.44 Remove R12 add close jump(GP2) of common project using.  
P.05 Remove R29~R33,R35,R36 add close jump(GP3~GP9) of common project using.  
P.08 Remove R107,R113,R1143 add close jump(GP10~GP12) of common project using.  
P.14 Remove R166 add close jump(GP14) of common project using.  
P.33 Remove R595 add close jump(GP14) of common project using.  
P.37 Remove R987 add close jump(GP15) of common project using.  
P.38 Remove R718 add close jump(GP16) of common project using.  
P.42 Remove R1098,R1093,R1097,R1270,R1271,R1314-R1316 add close jump(GP17~GP19,GP22~GP27) of common project using.

P.45 Remove R2043 add close jump(GP28) of common project using.  
P.46 Remove R2052 add close jump(GP29) of common project using.

**(2007/01/11)**

P.12 Change PJ13 JUMP size from smd5932 to open2b  
P.52~55,58 Delete PJ2,PJ1,PJ3,PJ4,PJ5,PJ7,PO9,PJ11 JUMP

**(2007/01/12)**

P.43 Change VR2~VR5 value from NC MLVSO603M04\_VR to MLVSO603M04\_VR for EMC solution.  
P.12 Delete NC\_CAP15 for Layout space.

**(2007/01/16)**

P.07~13 Change U112 symbol of OS sample.  
P.60 Delete BOSS5 because not using ROBSON function.  
P.32~36 Change U31 symbol of OS sample.  
P.05 Remove GP3~GP9, Add R29~R33,R35,R36 for debug convenient.  
P.03 Remove GP1, Add R7 for debug convenient.  
P.44 Remove GP2, Add R12 for debug convenient

**(2007/01/17)**

P.41 Remove GP20,GP21, Add R781,R786 for debug convenient.  
P.42 Remove GP22~GP27, Add R1314~r1316,R1270,R1271 for debug convenient.

**(2007/01/18)**

P.29 Change D61 from SM05.TCT to PACDN042Y3R because SM05.TCT forbid from MOR.

P.20 Delete R1995,R2004 of common project using.  
P.08 Remove GP10~GP12, Add R107,R1143,R113 for debug convenient.  
P.14 Remove GP13, Add R166 for debug convenient.  
P.33 Remove GP14, Add R595 for debug convenient.  
P.37 Remove GP15, Add R987 for debug convenient.  
P.38 Remove R718, Add R718 for debug convenient.  
P.42 Remove GP17~GP19, Add R1098,R1093,R1097 for debug convenient.

P.45 Remove GP28, Add R2043 for debug convenient.  
P.46 Remove GP29, Add R2052 for debug convenient.  
P.22 Delete C1693,C1694,R1996,R1999,change R1997,R1998 value NV\_240\_F to NV\_243\_F from nVIDIA suggest.

P.23 Delete C1696,C1695,R2000,R2003,change R2001,R2002 value NV128bit\_240\_F to NV128bit\_243\_F from nVIDIA suggest.

P.20 Add signal NV\_GPIO10 for nVIDIA suggest.  
P.22,23 Reverse R2132~R2138,Q168~Q175 for nVIDIA suggest.  
P.58 Reserve PR361,PR362,PC244,PO76 for nVIDIA suggest.  
P.11 Remove R2128 of common project using.

**(2007/01/19)**

P.26 Reverse R2139 for HDMI audio backup solution .  
P.44 Add Q176 VGA Thermal-Sensor from FAE suggest.  
P.52 change PR130,PR131 from 100 to 3K, add PC64,PC65:0.1U for SAG test require

P.20 Add R2140 0 ohm for debug use.  
P.17 Delete TP692 for layout space.  
P.41 Delete R675 for +VCC DMI has L118 already  
P.44 Delete D112 for it's-not used.

**(2007/01/20)**

P.30 Reserve D115 for hang up or no display issue.  
P.44 Reserve R2141 for VGA Thermal-Sensor use.

**(2007/01/23)**

P.41 Change U79 from G914DF to SI9183DT-33-T1-E3 for power switch power issue.

**(2007/01/24)**

P.55 Reserve PC214 for C4 noise.

**(2007/01/25)**

P.30 Change D115 value from NC BAT54SPT to BAT54SPT for hang up or no display issue.  
P.64 Change R1977,R1978 value 47\_J to 33\_J for LED light issue.  
P.53 Change R1991 resistor from 7.8K to 8.2K for +1 OSVRUN low voltage issue.  
P.64 Change R1980,R1981 resistor from 47 ohm to 150 ohm for LED light issue.  
P.40 Change R1380 resistor from 130 ohm to 68 ohm for LED light issue.

**(2007/01/26)**

P.40 Change Q104 from 2N7002 to 2N7002ESPT for ESD protect.

**(2007/01/29)**

P.18 Change R203 value from NC 2K\_J to NVH 2K\_J for Hynex VRAM strap.  
P.18 Change R204 value from NV-2K\_J to NVQ/S 2K\_J for add Hynix VRAM strap.  
P.18 Change R205 value from NVS 2K\_J to NVH/S 2K\_J for Hynex VRAM strap.  
P.62 Remove R466,stuff D113,D113,DI14 change to NV\_CH500H-40PT for HDMI DDC/CEC capacitance test issue.

P.38 Delete R1914 due to it's duplicated function with PR128.

P.49 Change R2110,R2112 1 ohm to 0 ohm for low voltage issue.

**(2007/02/05)**

P.54 Change PR352 from 21K to 20.5K;  
PR351 from 30K to 30.1K for +1\_8VSUS low voltage issue.

P.58 Change PR283 from 2.43K to 2.55K for NV\_VDD low voltage issue.

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**(2007/02/26)**

P.58 Change PL15 value from 1.0UH\_11.5x10.4 to NV\_1.0UH\_11.5x10.4 because low board doesn't need it.

**(2007/02/28)**

P.34 Change R1936 0 ohm to 10K ohm from MOR ( Intel MOW)

**(2007/03/14)**

P.64 Reserve Q177 to support CPRM for SD Card from MOR.

P.20 Change U82 from 190-00001-0001-002 to 190-00001-0001-003 for vendor PN of HDCP ROM have been revised.

**(2007/03/15)**

P.51 Change PC1 from 0.01U\_25V to 0.01U\_50V for In order to prevent the MS1X serious burn issue happen when the abnormal failure happened.

**(2007/03/19)**

P.31 Add R458 notice for LCD panel screen flash issue.

**(2007/03/20)**

P.30 L33,L35,L36 change from 75ohm bead to 120ohm bead for EMI issue.

P.22,23 C504, C506, C1400, C1399, C1401, C1402, C1403, C1404 change from 0.1uF to 0.01uF according to NVIDIA PUN update.

**(2007/03/23)**

P.55 Add PC214 100U 25V for power noise issue.

**(2007/03/27)**

P.06 Change RP11 value from 33\_J to NC\_33\_J because ROBSON MS90 doesn't need it.

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