

Schematics Page Index (Title / Revision / Change Date)

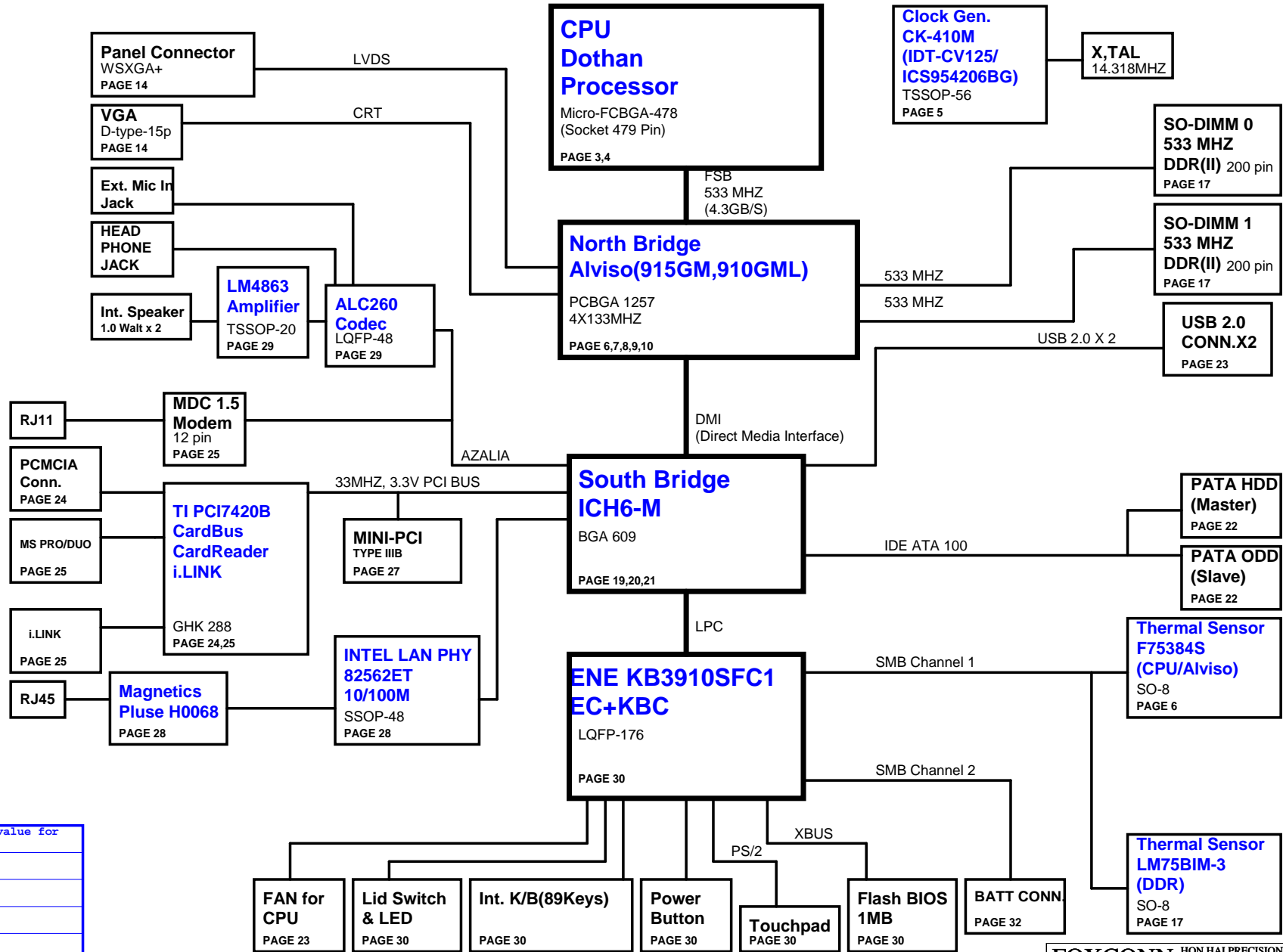
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P. Leader	Check by	Design by

Project Code & Schematics Subject: MSS1 M/B-FUBAI	PCB P/N: 1P-005B100-80SA
Project Code & Schematics Subject: MSS1 M/B-HANNSTAR	PCB P/N: 1P-005B500-80SA
Project Code & Schematics Subject: MSS1 M/B-NAN YA	PCB P/N: 1P-005B200-80SA

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MSS1(915GM/GML Block Diagram)



	Symbol ahead of value for NC components
ALL	NC_
915PM + NV44M	NV_
915GM or 910GML	AL_
910GML	LNC_
915GM	MNC_

BOM configuration

Dothan

1 OF 3

REQUEST PHASE SIGNALS

DATA PHASE SIGNALS

ERROR SIGNALS

ARBITRATION PHASE SIGNALS

SNOOP PHASE SIGNALS

RESPONSE PHASE SIGNALS

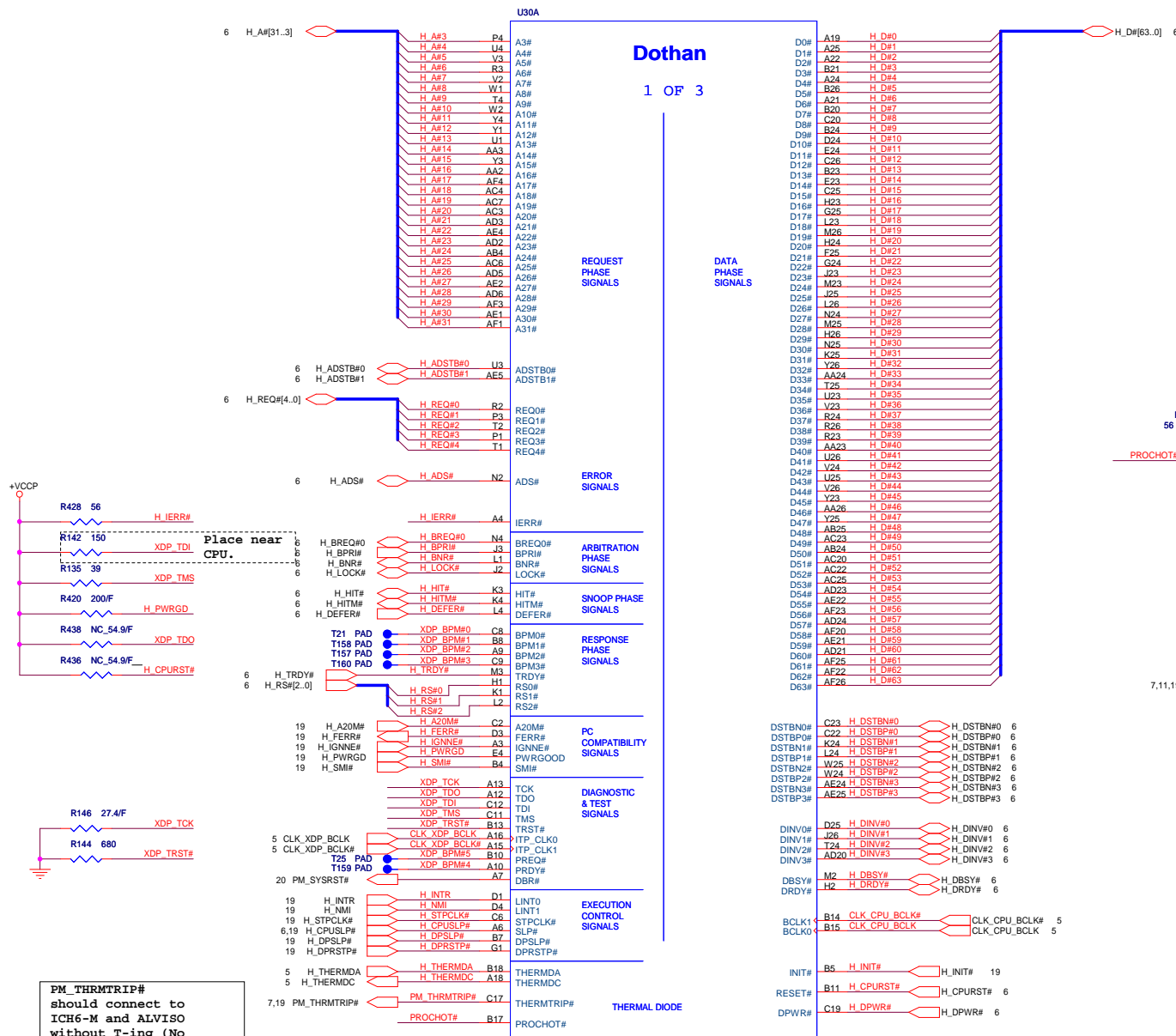
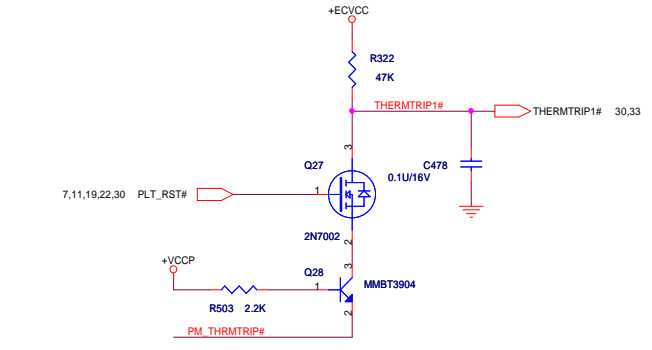
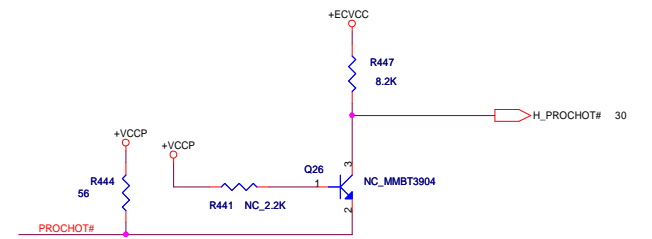
PC COMPATIBILITY SIGNALS

DIAGNOSTIC & TEST SIGNALS

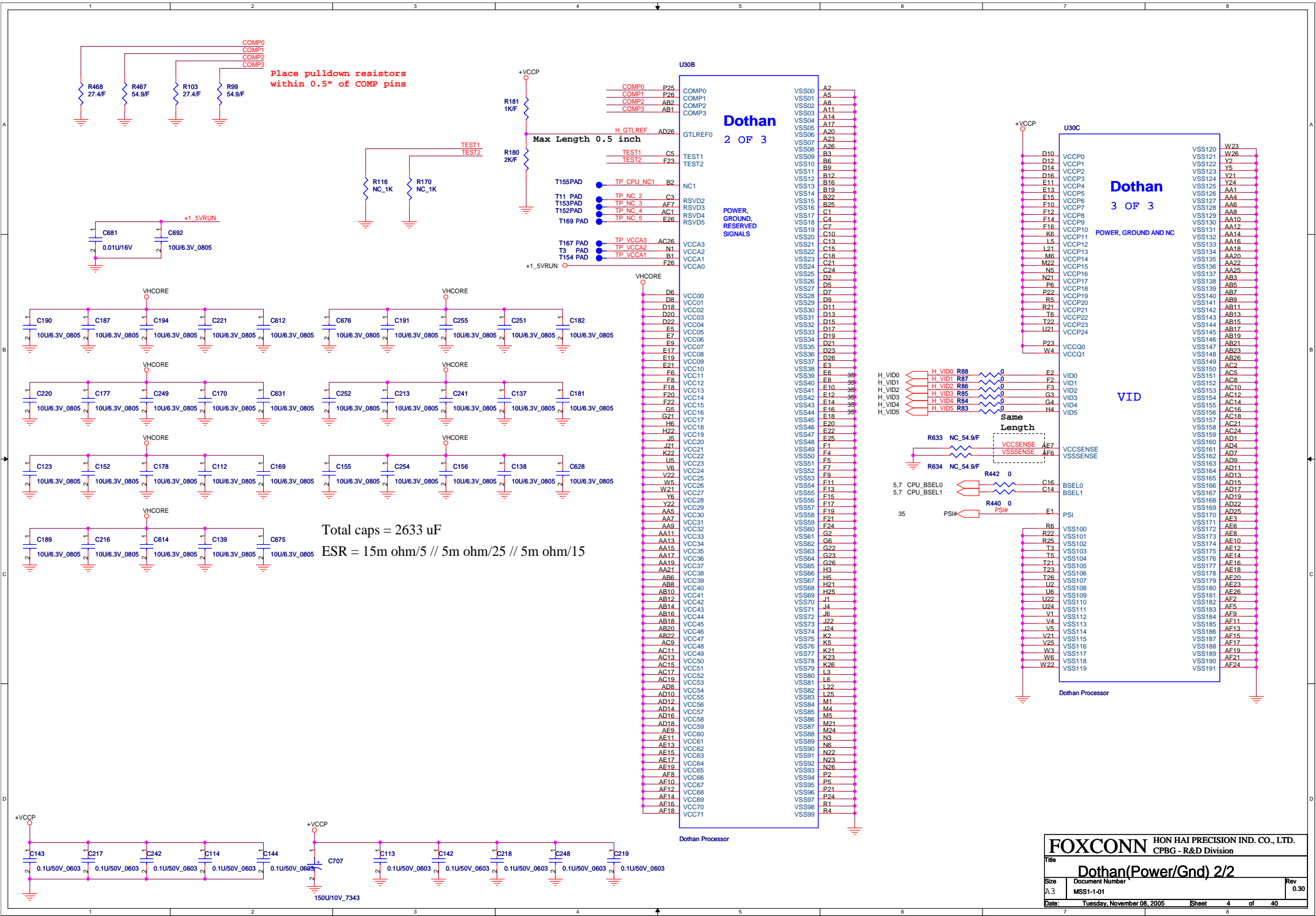
EXECUTION CONTROL SIGNALS

THERMAL DIODE

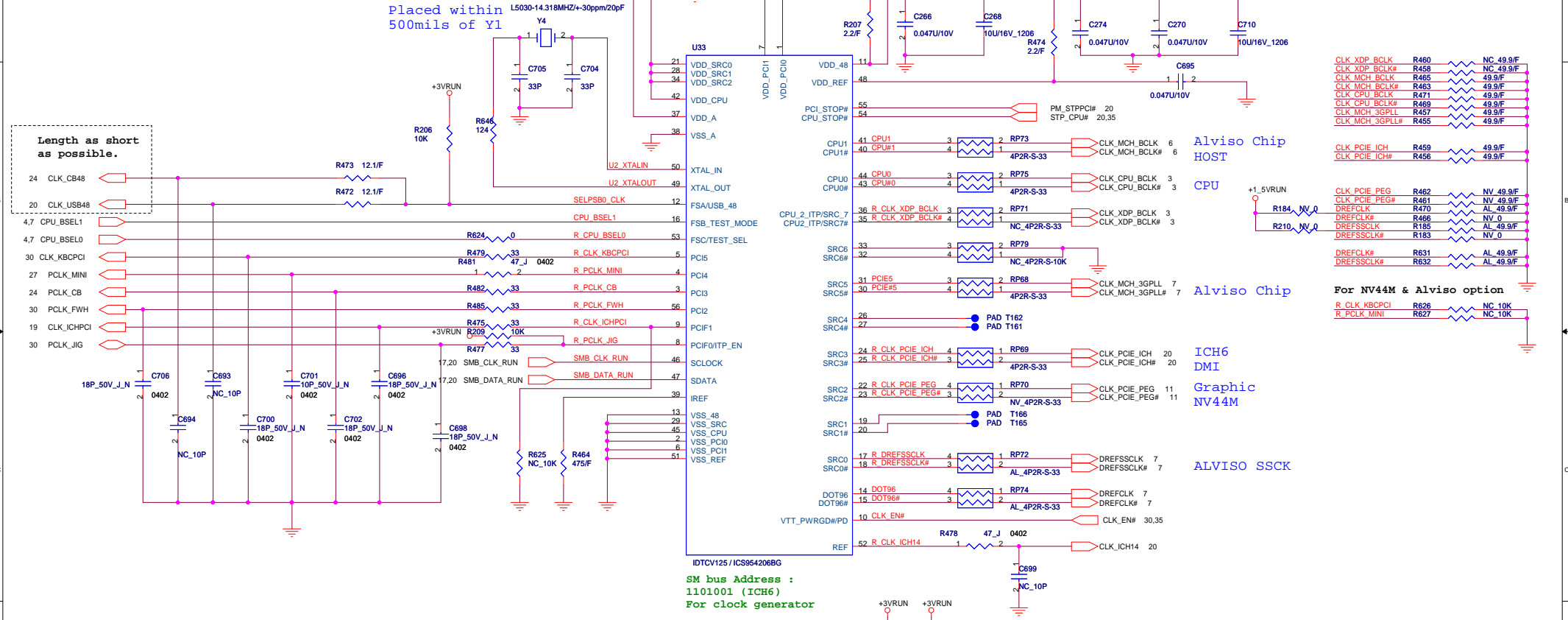
Dothan Processor



PM_THRMTRIP#
should connect to ICH6-M and ALVISO without T-ing (No stub)



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33



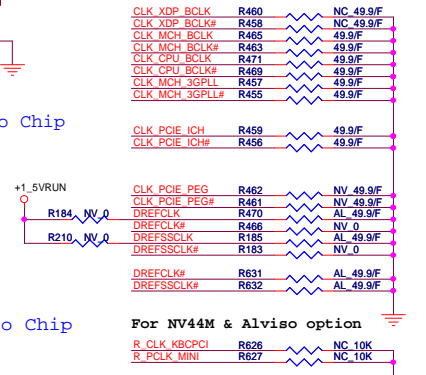
Length as short as possible.

Placed within 500mils of Y1

IDTCV125 / ICS854206BG
 SM bus Address : 1101001 (ICH6)
 For clock generator

SM bus Address : 1001101 (EC)
 For F75384S

Place Thermal-Sensor near CPU & GMCH.



Alviso Chip HOST

CPU

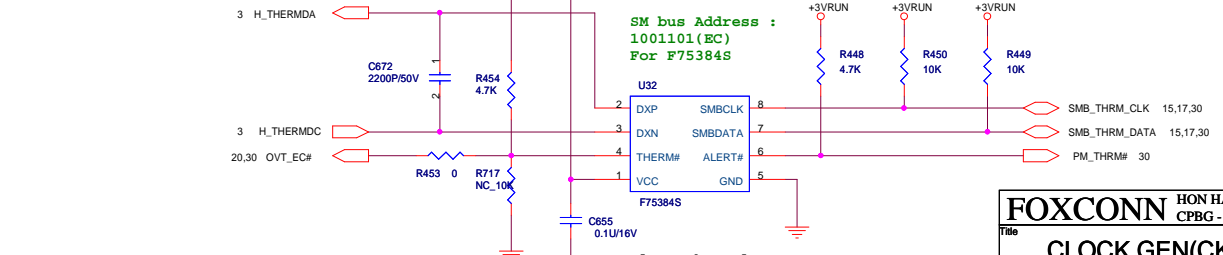
Alviso Chip

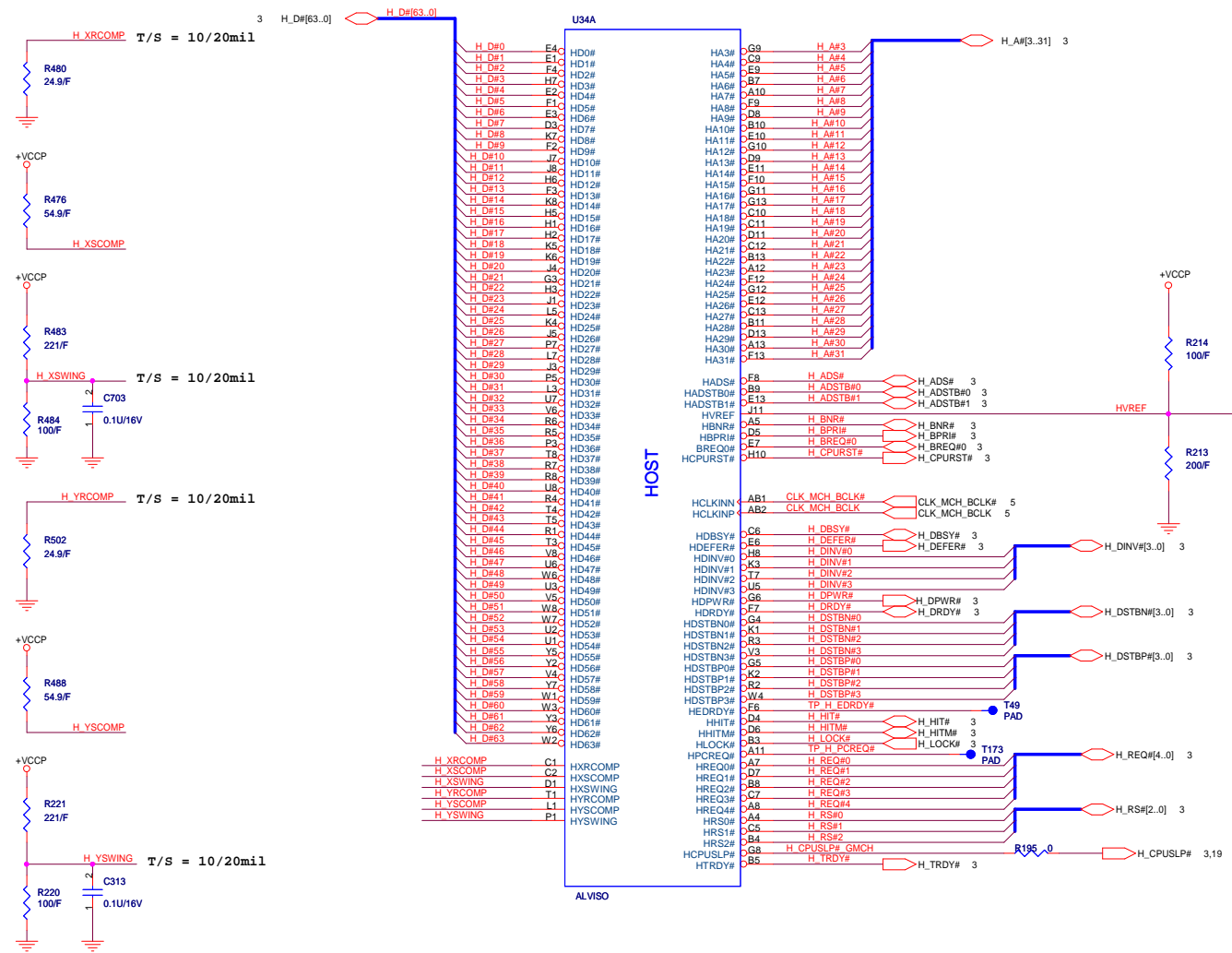
ICH6 DMI

Graphic NV44M

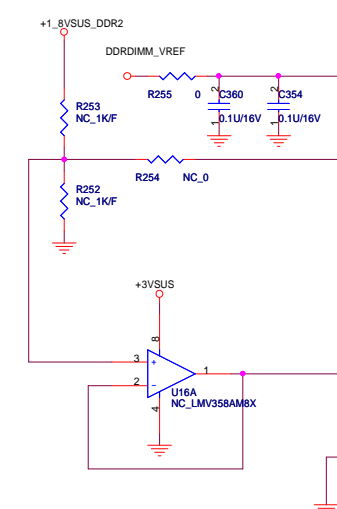
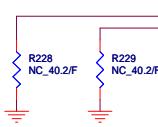
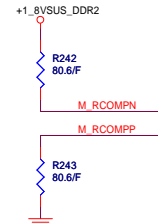
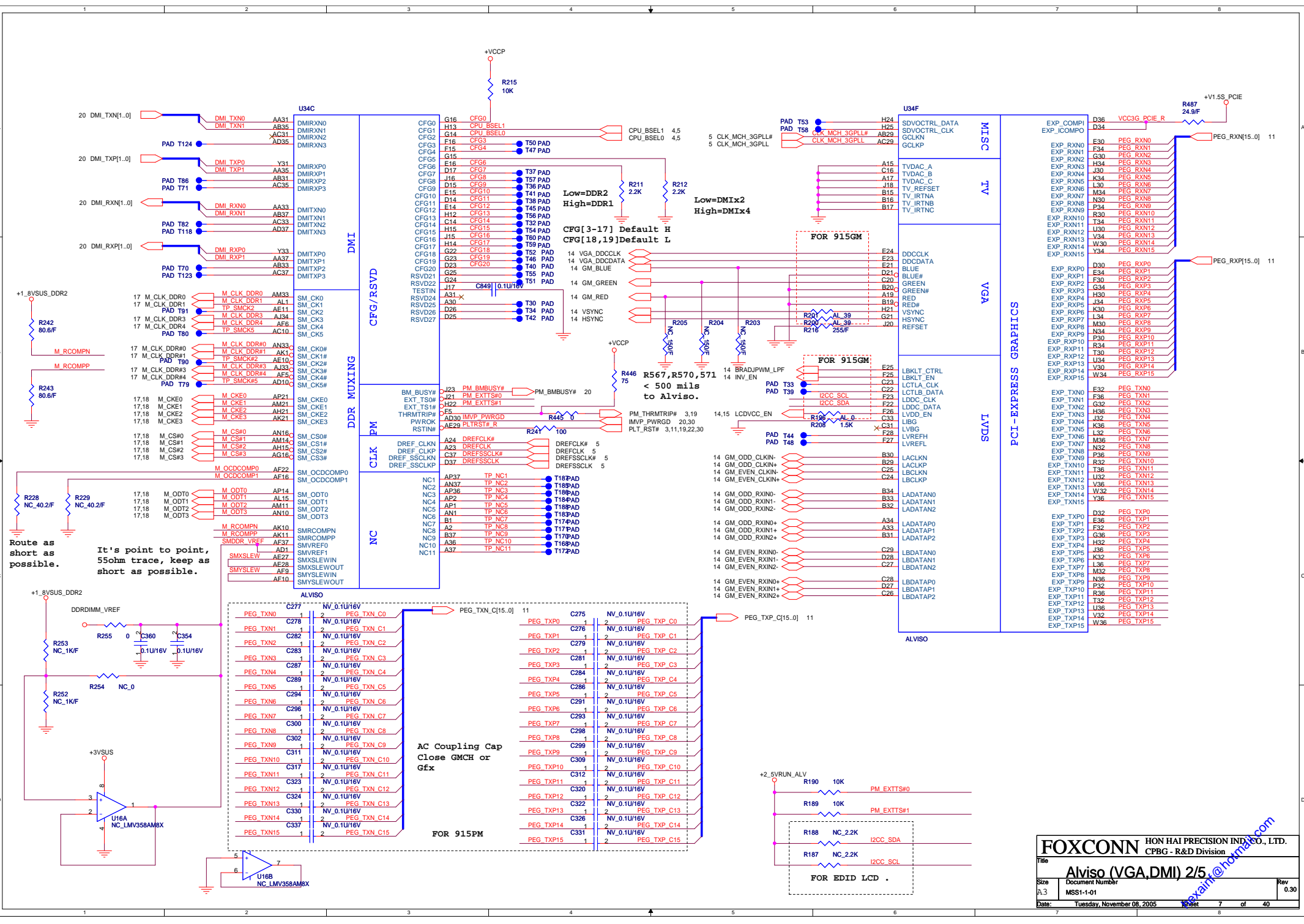
ALVISO SSK

For NV44M & Alviso option
 R_CLK_KBCPCI R26
 R_PCLK_MINI R627





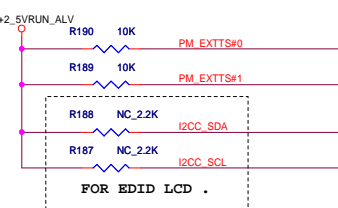
Place Cap. near GMCH within 100 mils.

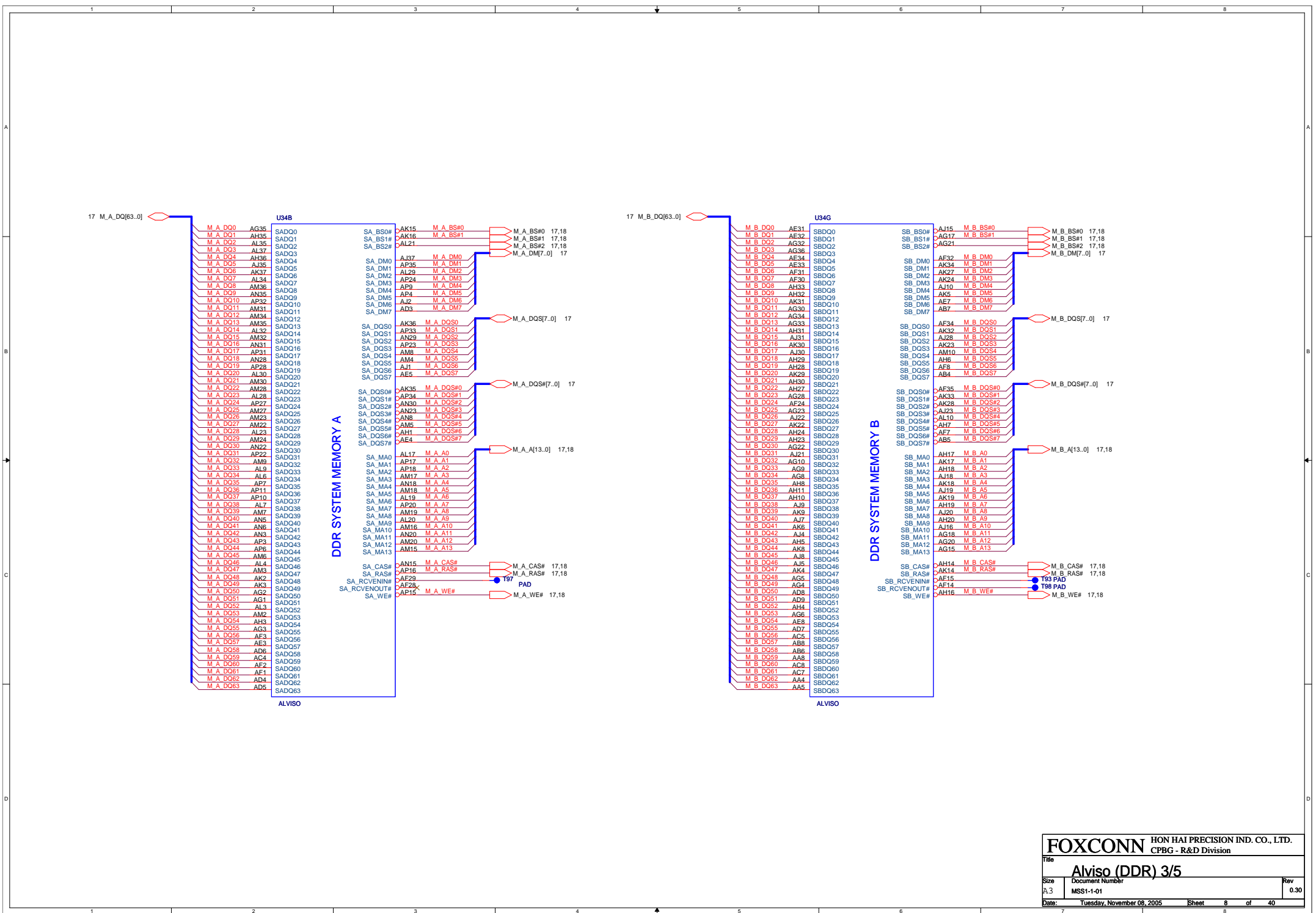


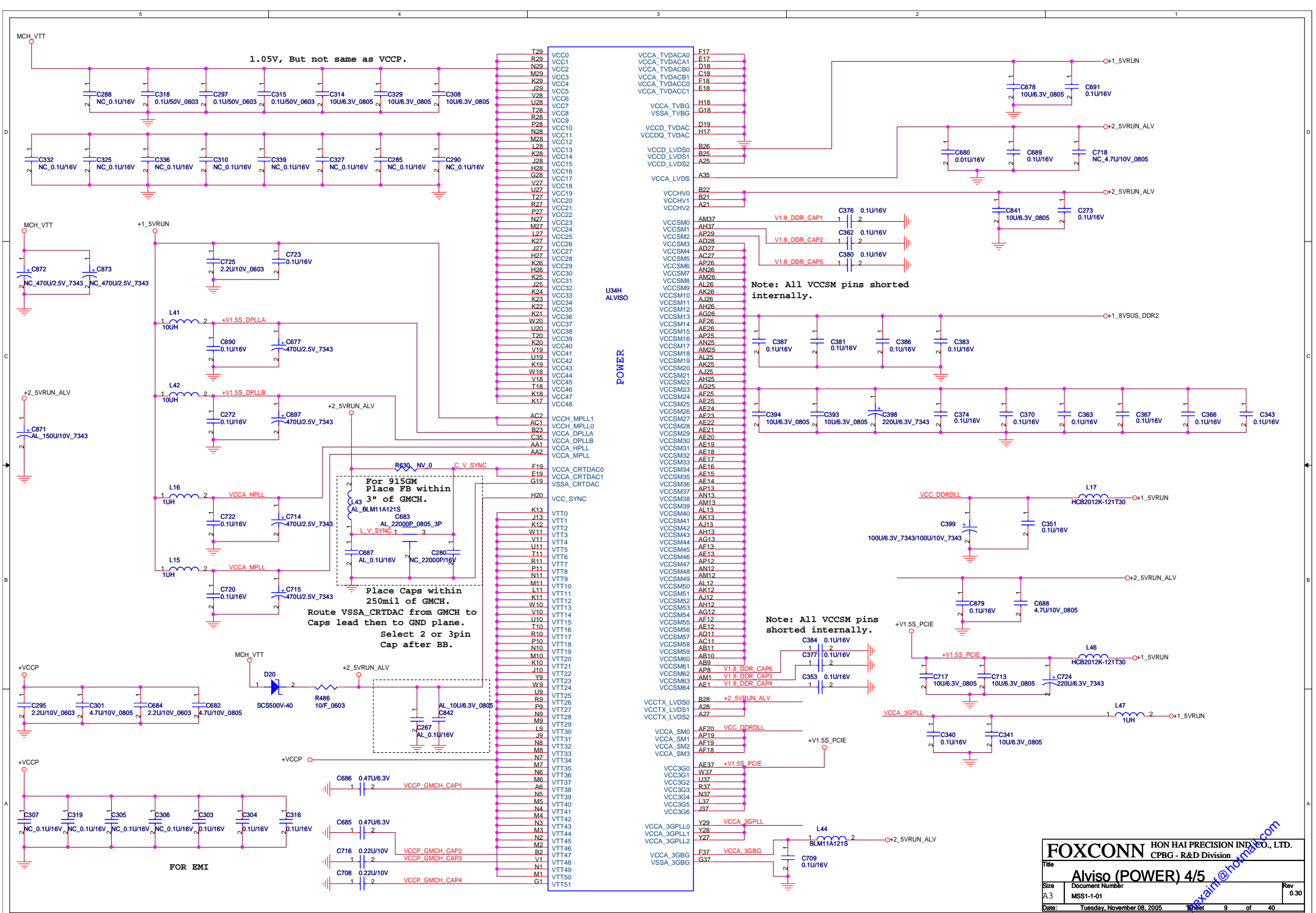
AC Coupling Cap
Close GMCH or
GEx

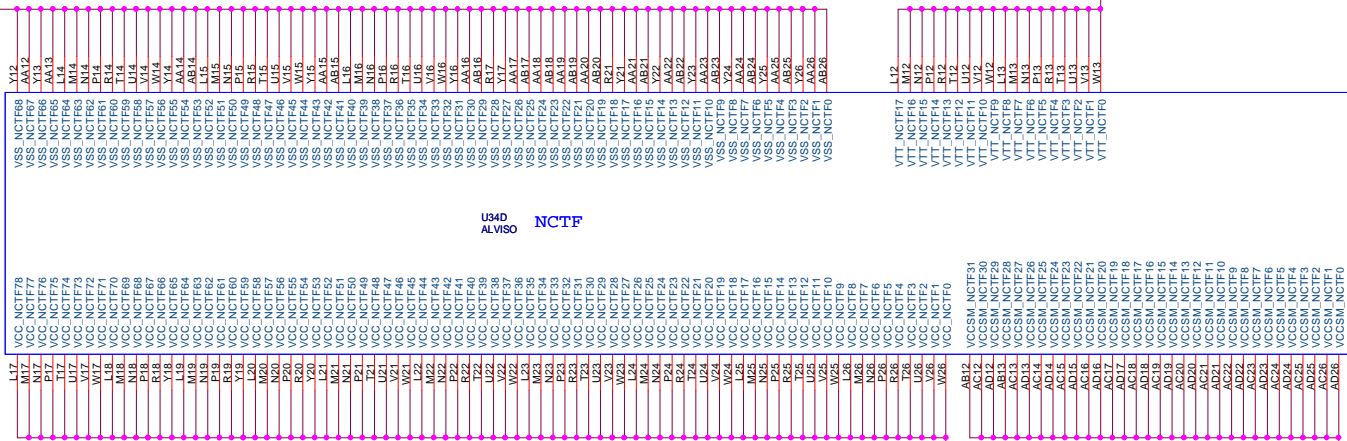
FOR 915PM

PEG TXN0	C277	NV_0.1u/16V	1	2	PEG_TXN_C0	11
PEG TXN1	C278	NV_0.1u/16V	1	2	PEG_TXN_C1	11
PEG TXN2	C282	NV_0.1u/16V	1	2	PEG_TXN_C2	11
PEG TXN3	C283	NV_0.1u/16V	1	2	PEG_TXN_C3	11
PEG TXN4	C287	NV_0.1u/16V	1	2	PEG_TXN_C4	11
PEG TXN5	C289	NV_0.1u/16V	1	2	PEG_TXN_C5	11
PEG TXN6	C294	NV_0.1u/16V	1	2	PEG_TXN_C6	11
PEG TXN7	C296	NV_0.1u/16V	1	2	PEG_TXN_C7	11
PEG TXN8	C300	NV_0.1u/16V	1	2	PEG_TXN_C8	11
PEG TXN9	C302	NV_0.1u/16V	1	2	PEG_TXN_C9	11
PEG TXN10	C311	NV_0.1u/16V	1	2	PEG_TXN_C10	11
PEG TXN11	C317	NV_0.1u/16V	1	2	PEG_TXN_C11	11
PEG TXN12	C323	NV_0.1u/16V	1	2	PEG_TXN_C12	11
PEG TXN13	C324	NV_0.1u/16V	1	2	PEG_TXN_C13	11
PEG TXN14	C330	NV_0.1u/16V	1	2	PEG_TXN_C14	11
PEG TXN15	C337	NV_0.1u/16V	1	2	PEG_TXN_C15	11

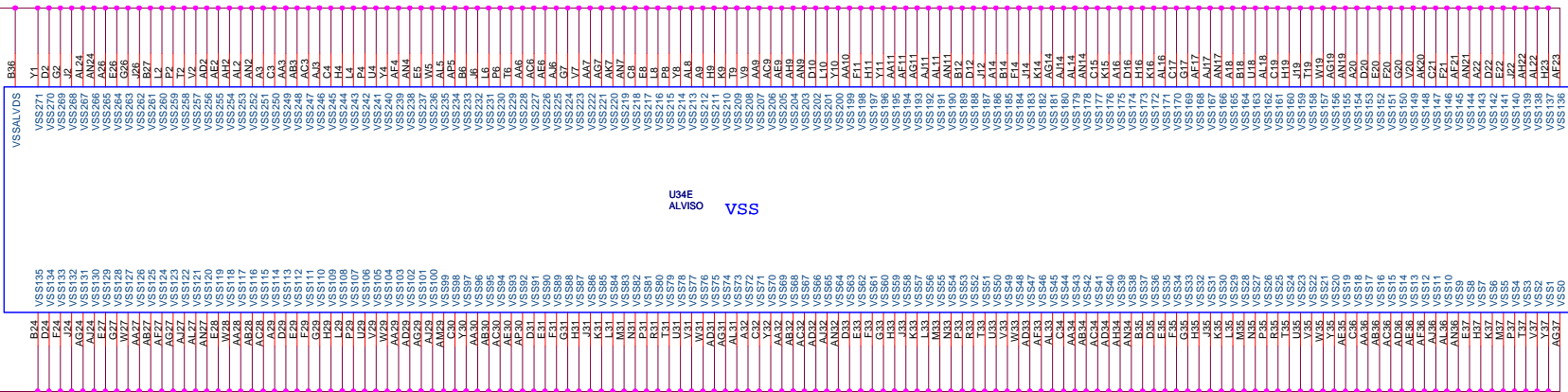




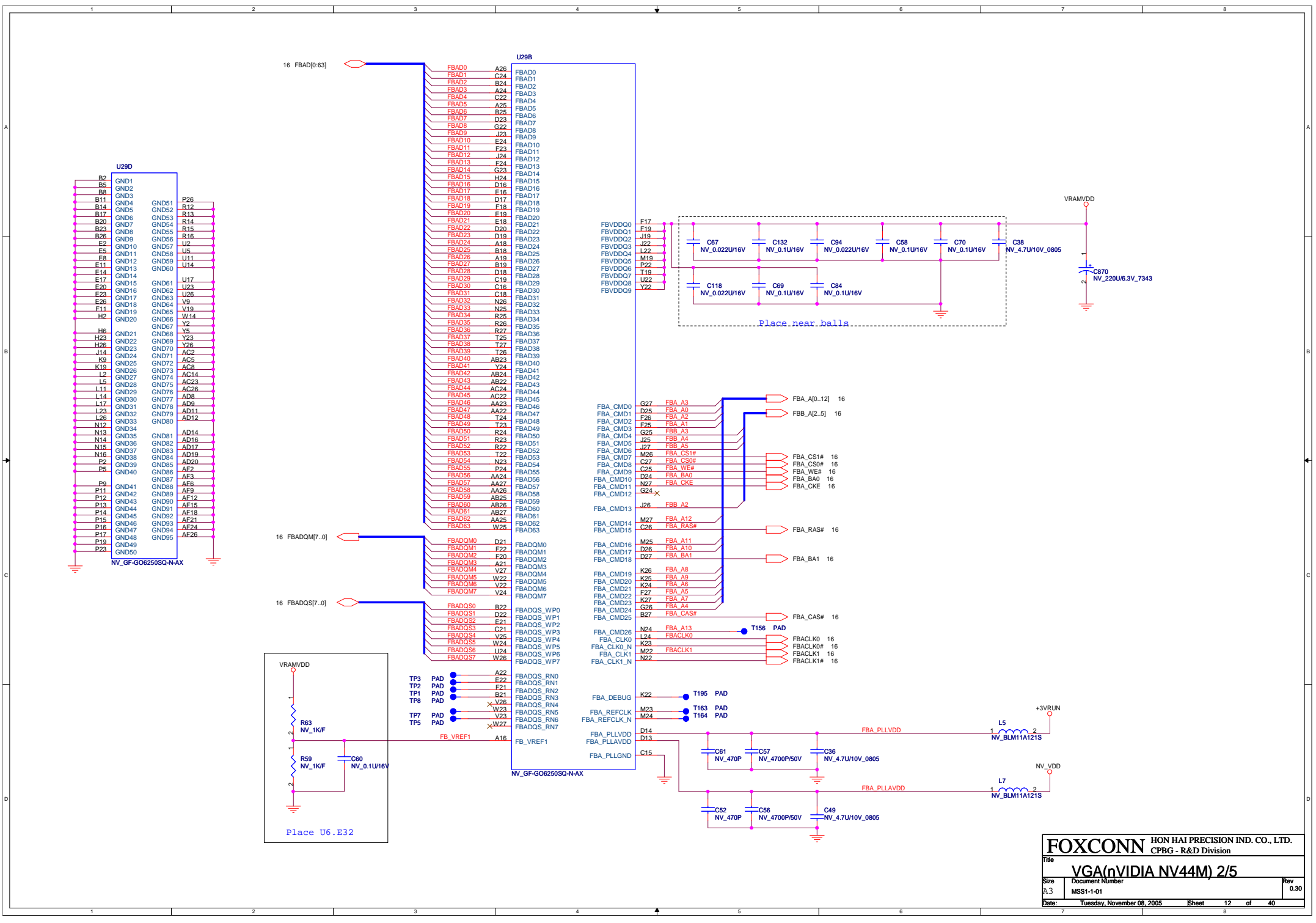


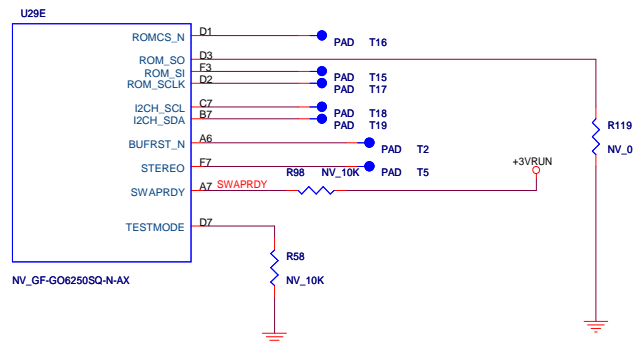
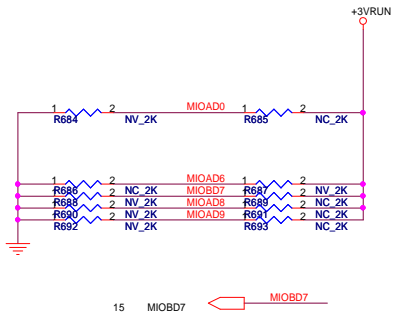
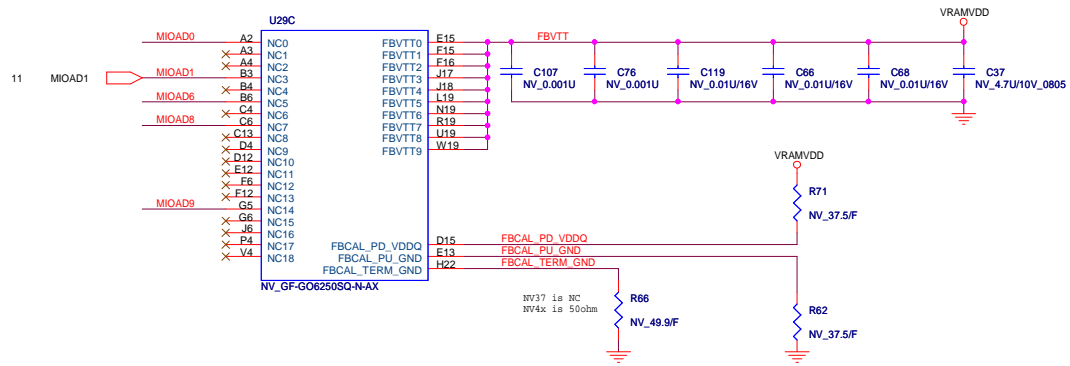


U34D
ALVISO NCTF



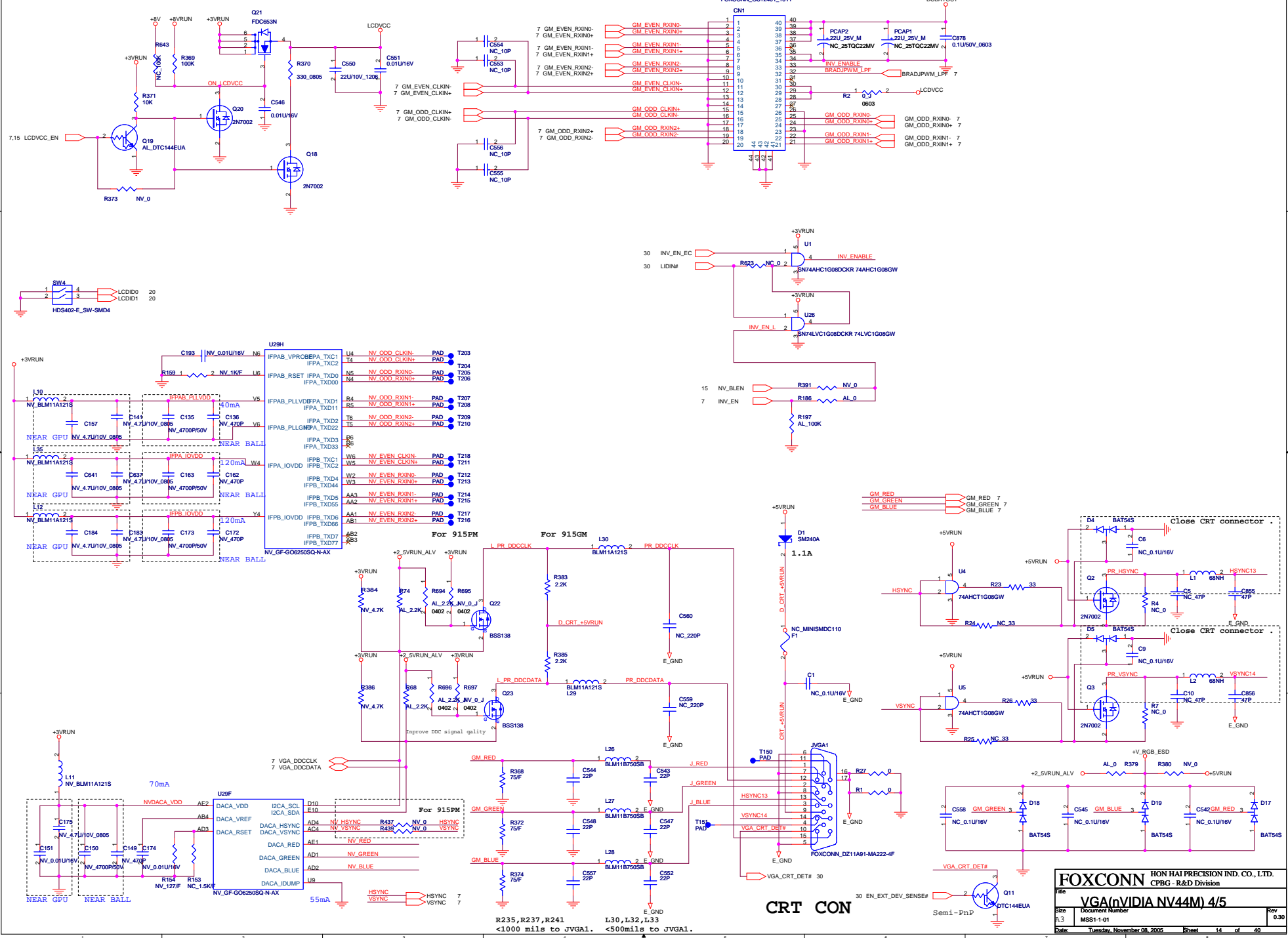
U34E
ALVISO VSS





LVDS CONNECTOR

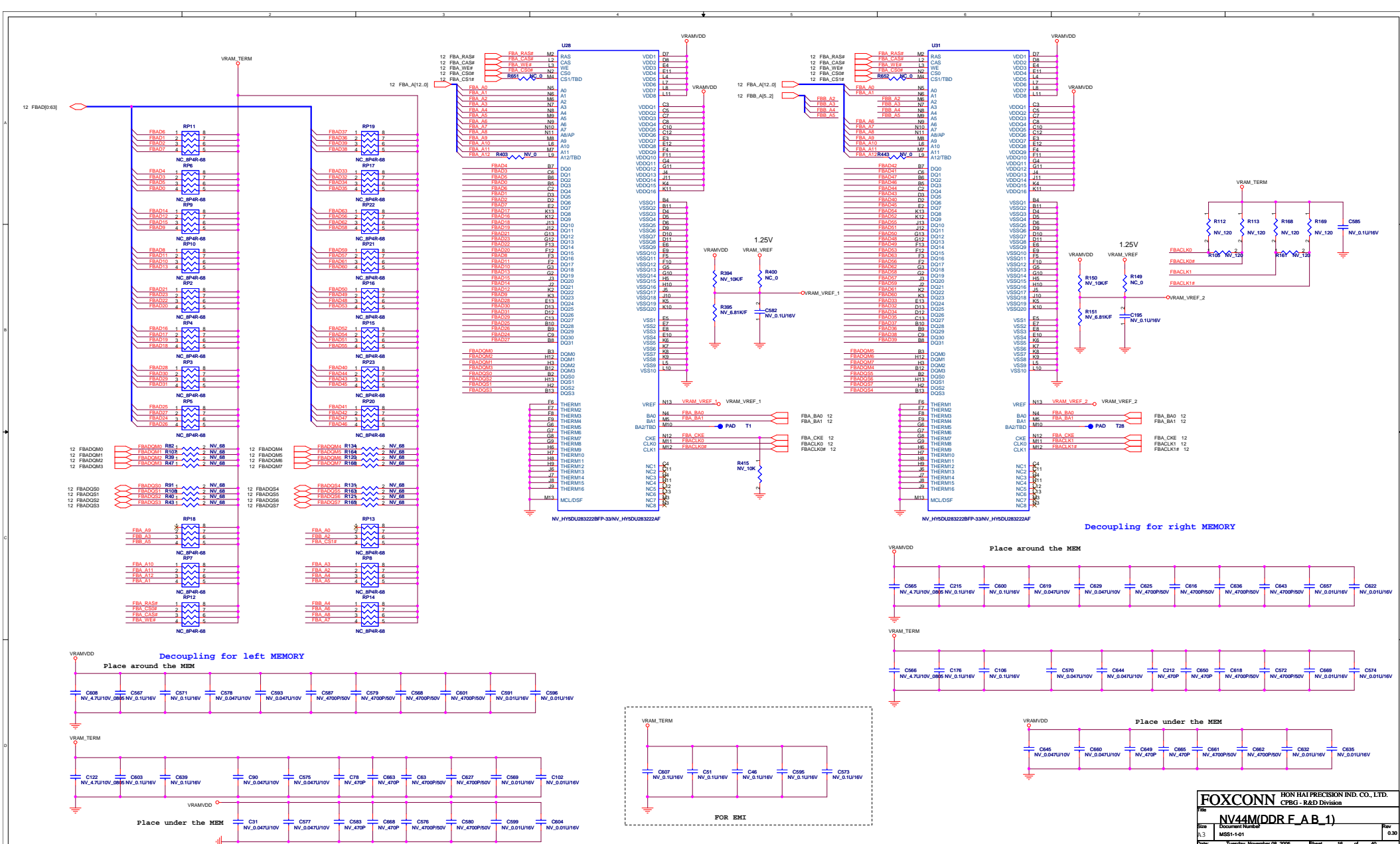
FOXCONN_GS12401_1011



CRT CON

R235, R237, R241 L30, L32, L33
 <1000 mils to JVG1. <500mils to JVG1A1.

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
File	VGA(nVIDIA NV44M) 4/5		
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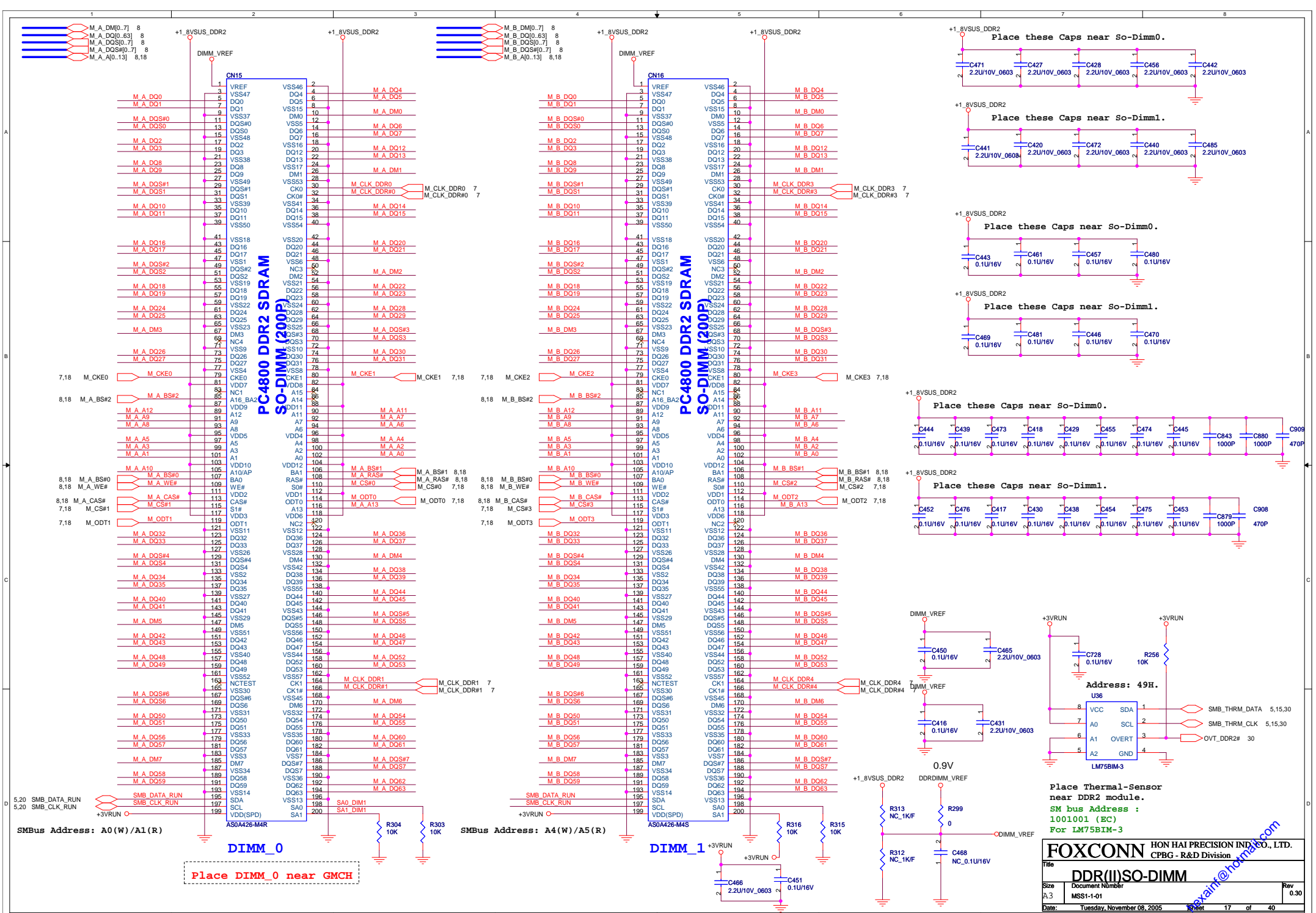
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CPBG - R&D Division

Part No. **NV44M(DDR F_AB 1)**

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Place these Caps near So-Dimm0.

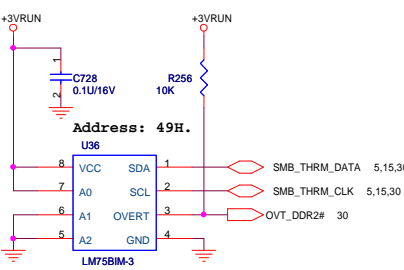
Place these Caps near So-Dimm1.

Place these Caps near So-Dimm0.

Place these Caps near So-Dimm1.

Place these Caps near So-Dimm0.

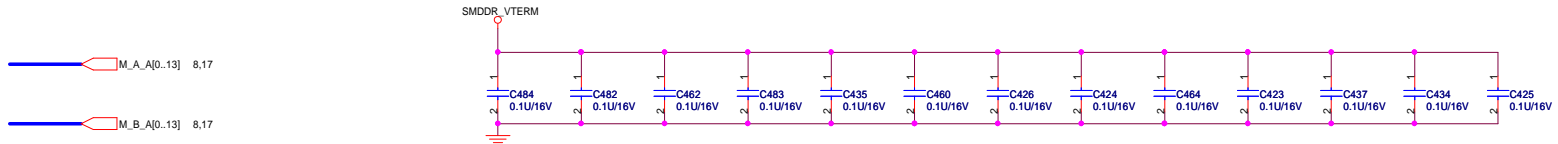
Place these Caps near So-Dimm1.



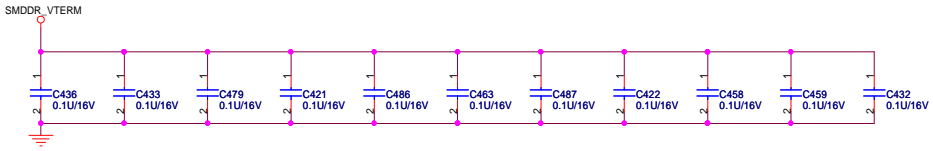
Place Thermal-Sensor near DDR2 module.
 SM bus Address is: 1001001 (EC)
 For LM75BIM-3

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
CPCBG - R&D Division			
DDR(II)SO-DIMM			
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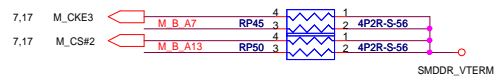
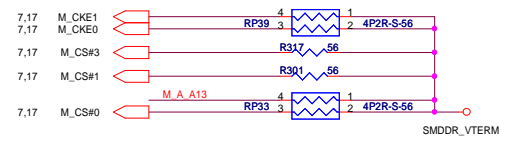
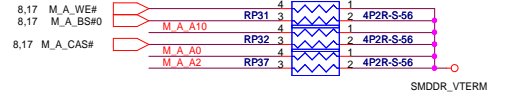
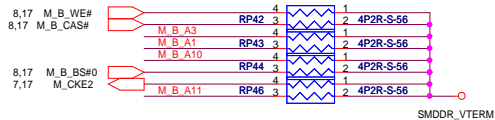
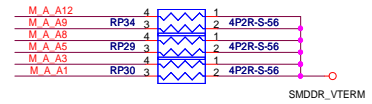
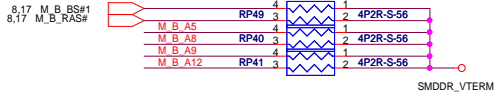
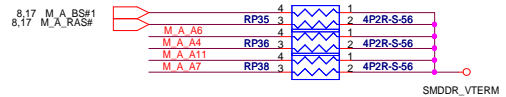
Place DIMM_0 near GMCH

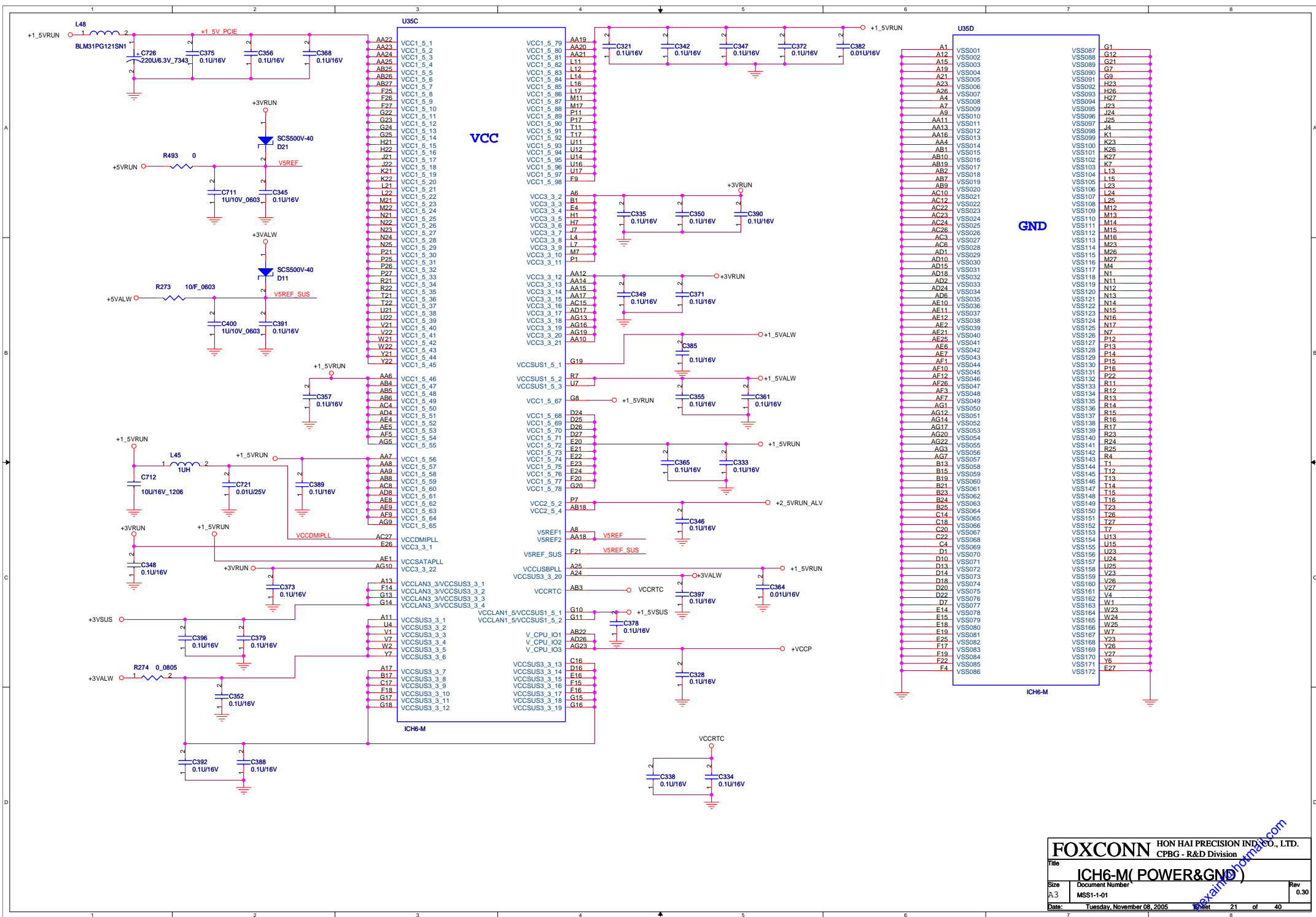


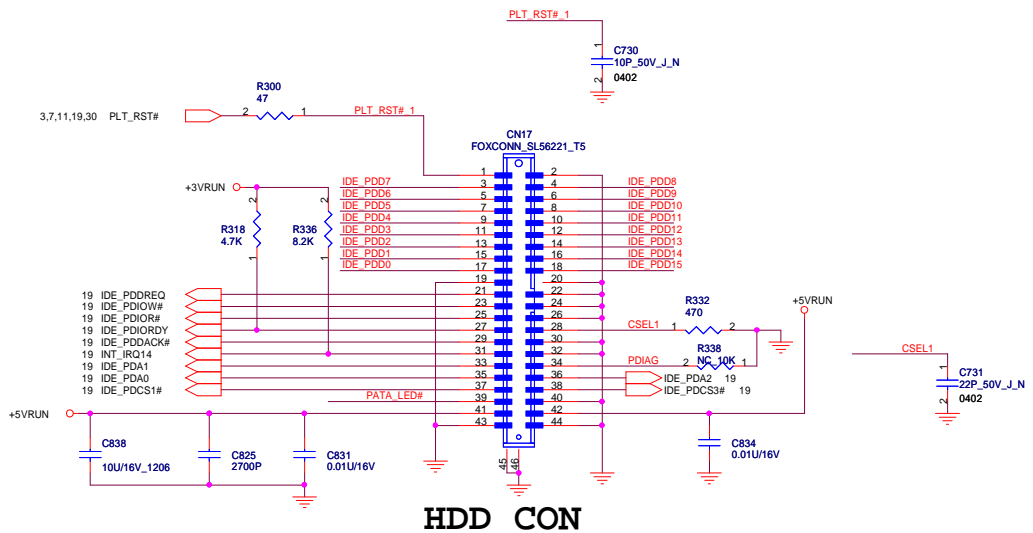
Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.



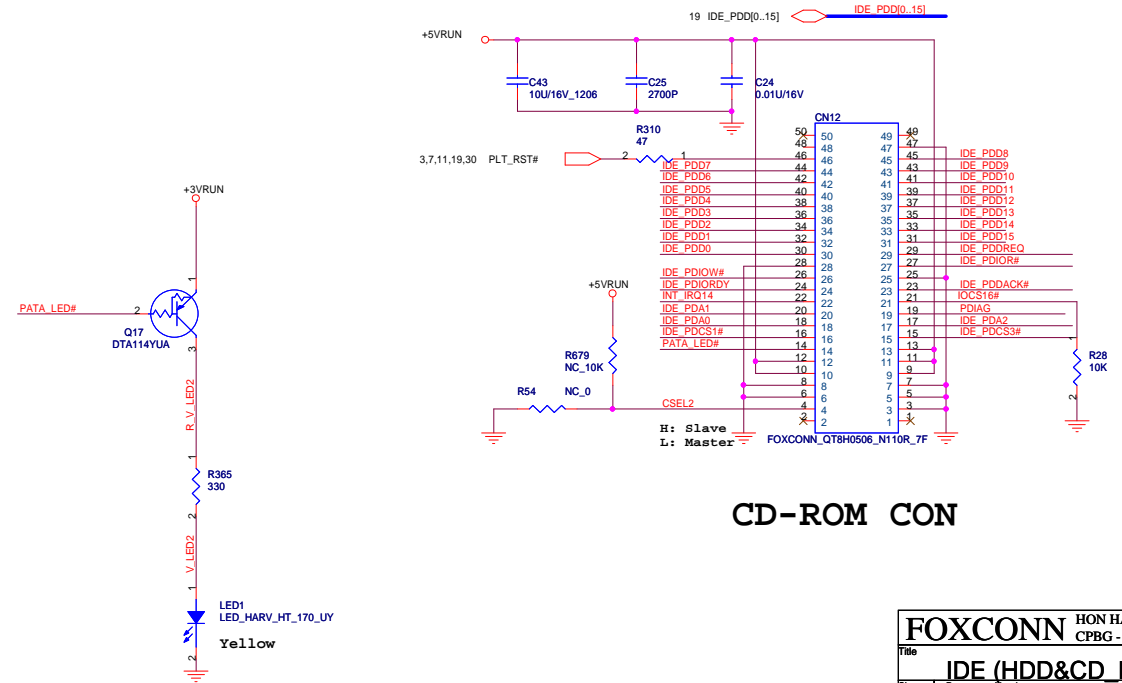
Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.







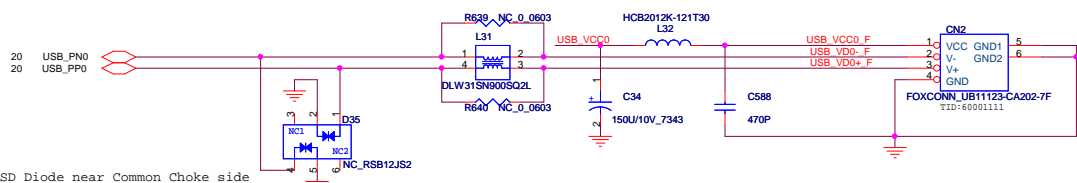
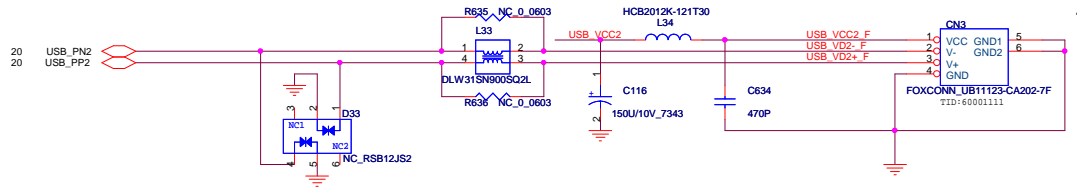
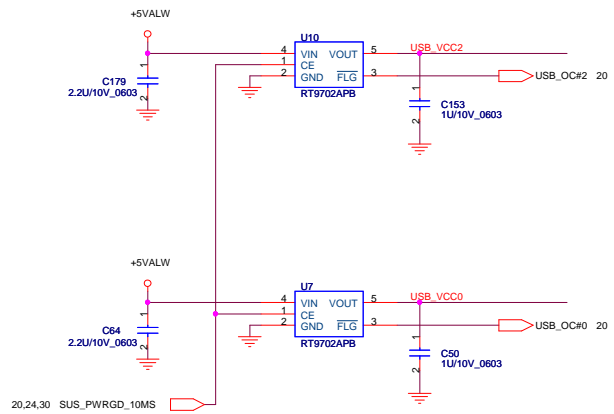
HDD CON



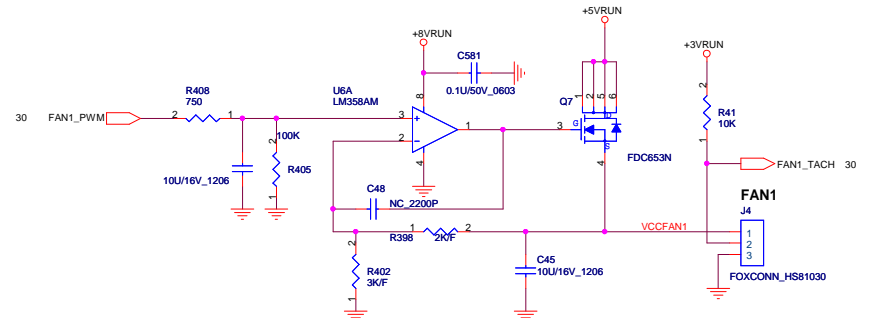
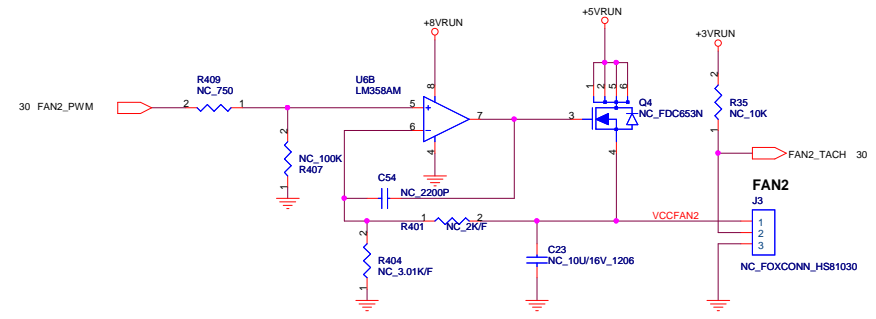
CD-ROM CON

FOXCONN HON HAI PRECISION IND. CO., LTD.	
CPBG - R&D Division	
Title: IDE (HDD&CD ROM)	
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USB2.0 X 2



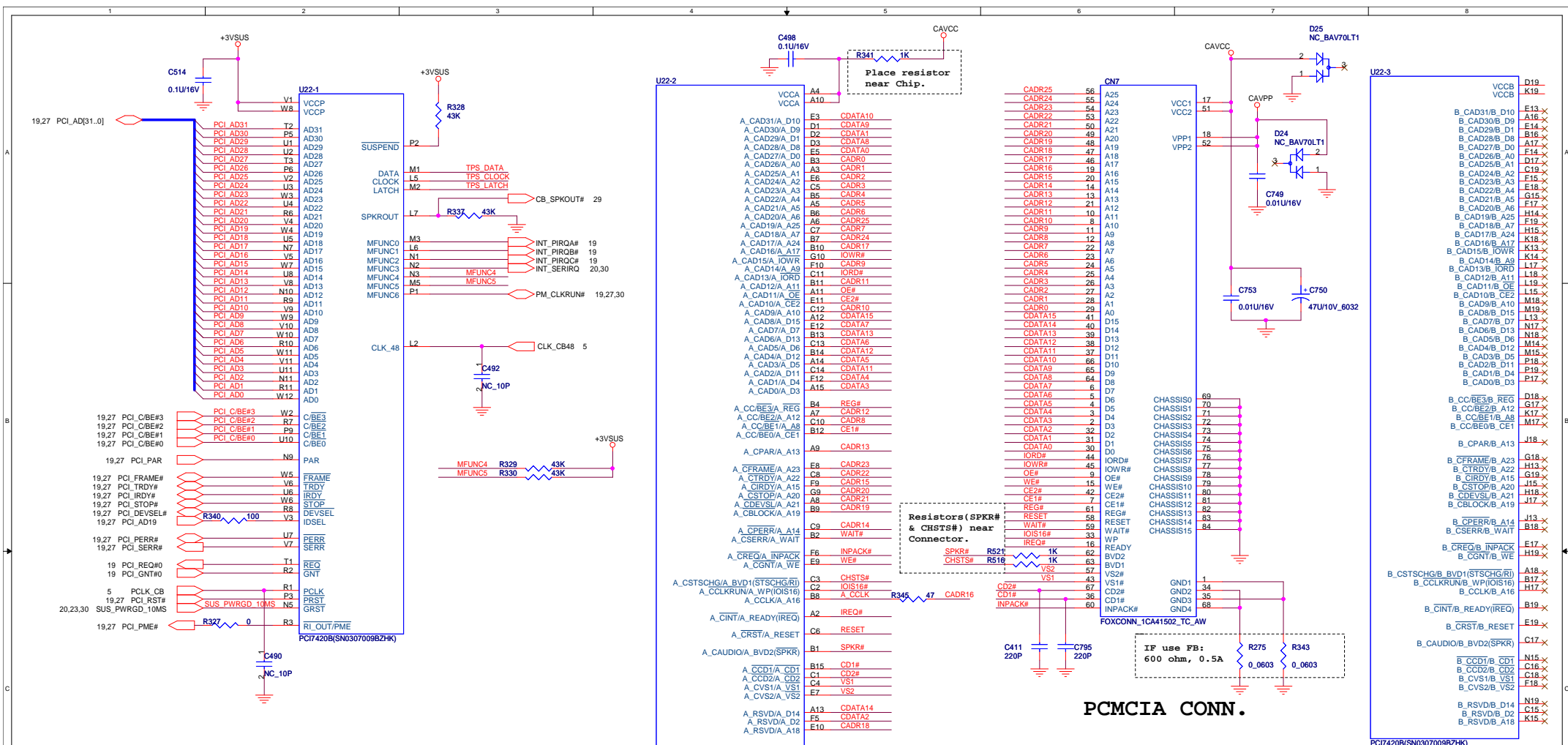
Place ESD Diode near Common Choke side



FAN

FOXCONN		HON HAI PRECISION IND. CO., L.TD.	
Title		CPBG - R&D Division	
USB2.0/FAN			
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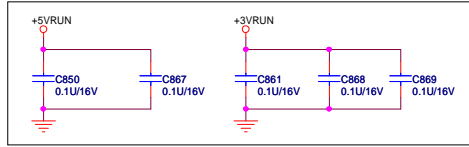
PCMCIA CONN.

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Part Number: **PC17420B(PCMCIA)**

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For EMI .



Near RPS1 ,
for EMI .



Near R607 ,
for EMI .



Near Q7 ,
for EMI .



Near Q4 ,
for EMI .



Near U37 ,
for EMI .



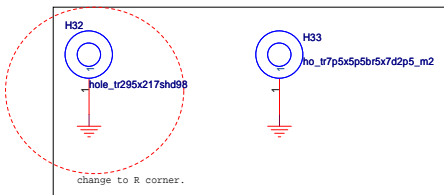
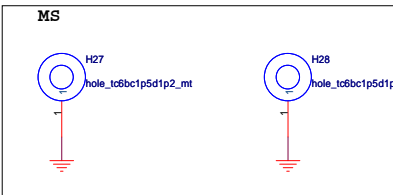
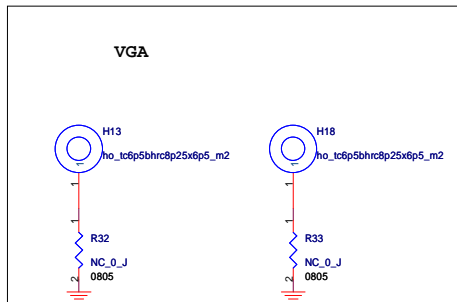
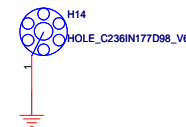
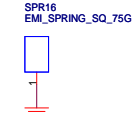
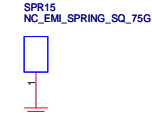
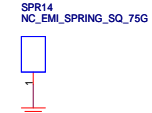
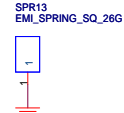
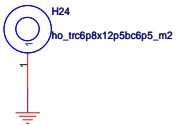
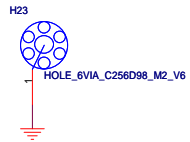
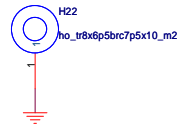
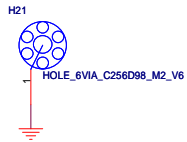
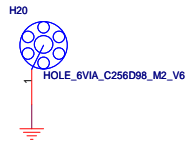
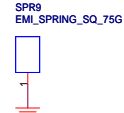
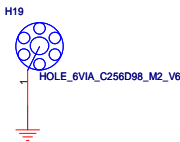
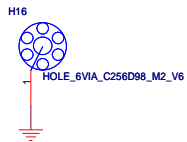
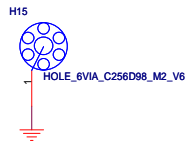
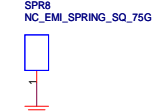
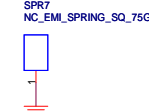
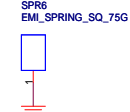
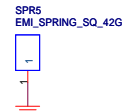
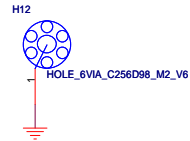
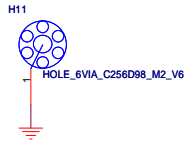
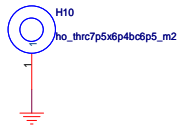
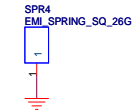
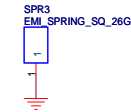
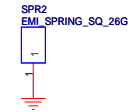
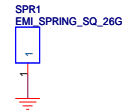
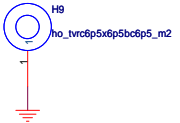
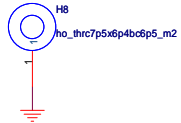
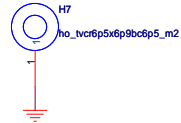
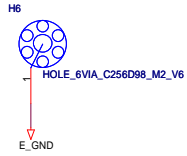
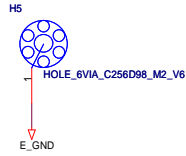
Near Q3 ,
for EMI .



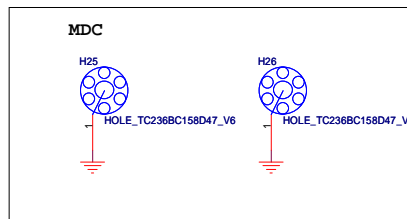
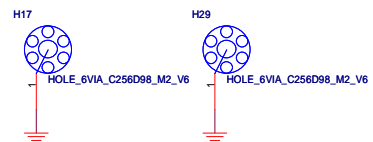
Near Q4 ,
for EMI .



Near D8 ,
for EMI .



change to R corner.

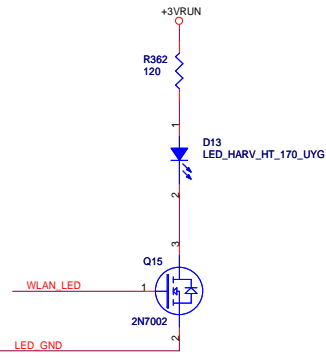
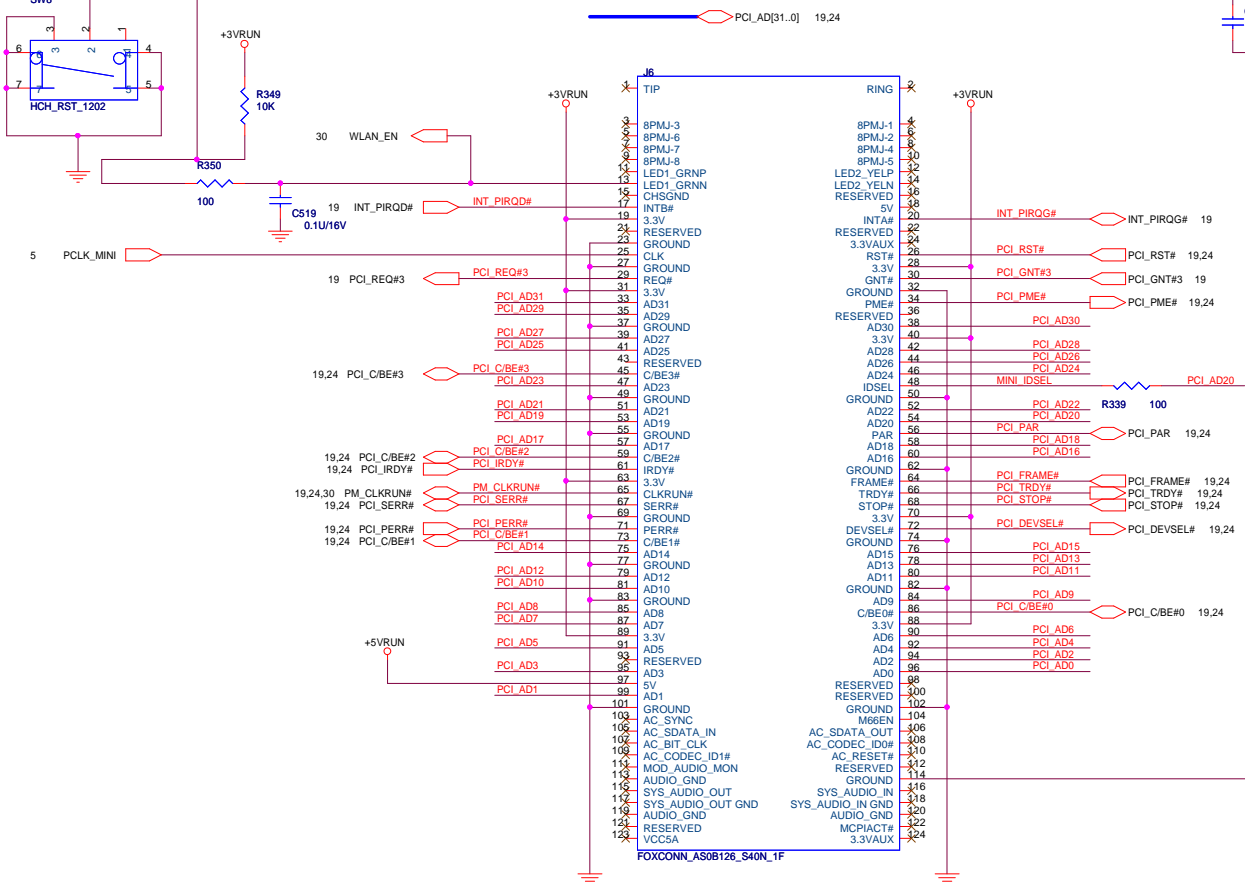
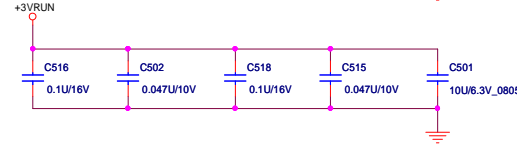
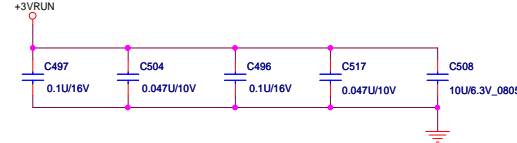
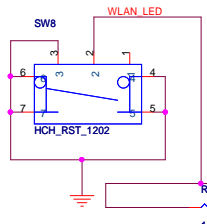


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Title: **SCREW HOLE & PAD**

Size: A3 Document Number: MSS1-1-01 Rev: 0.30

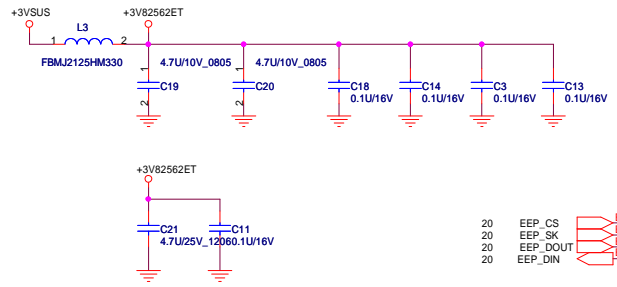
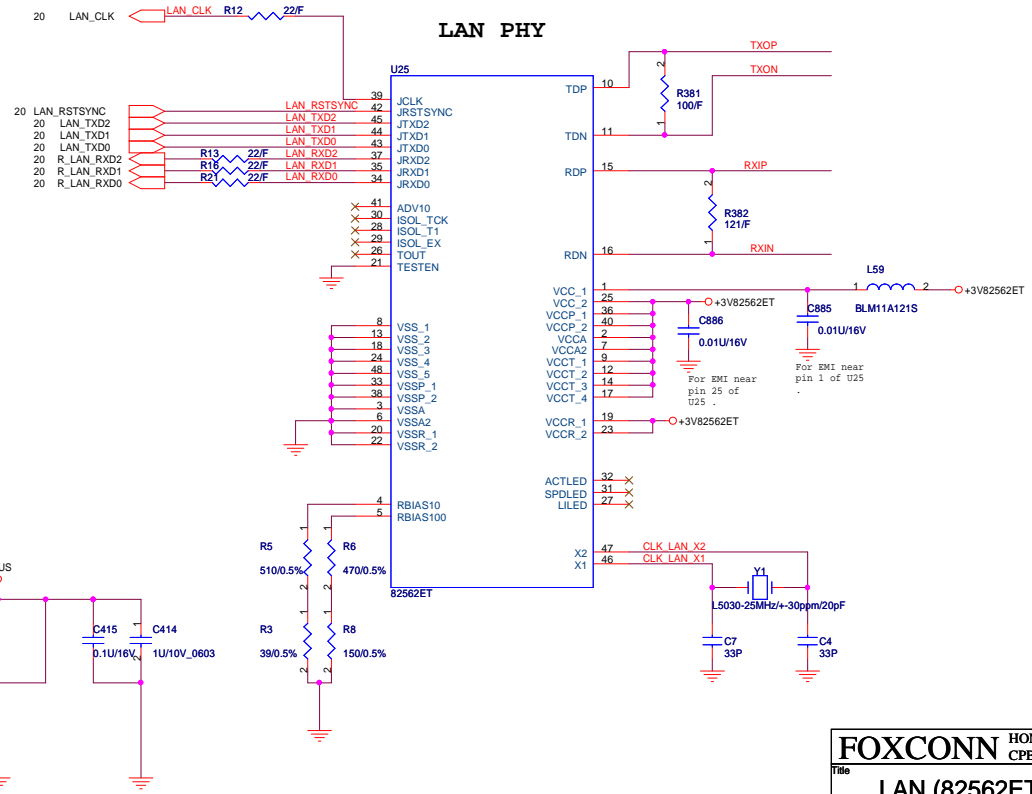
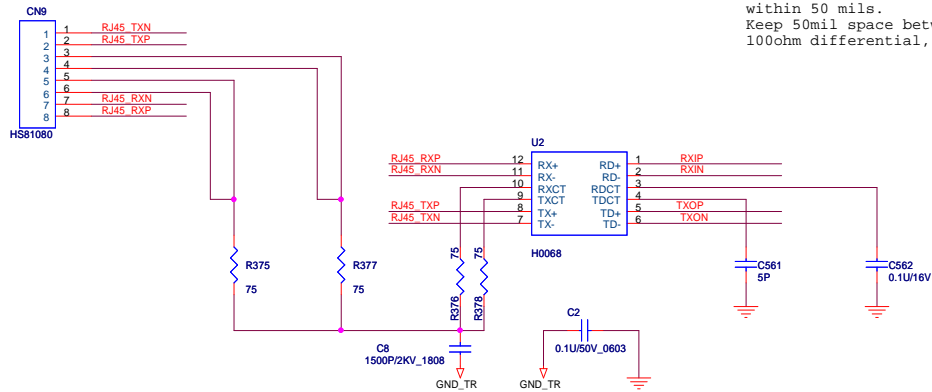
Date: Tuesday, November 08, 2005 Sheet: 26 of 40

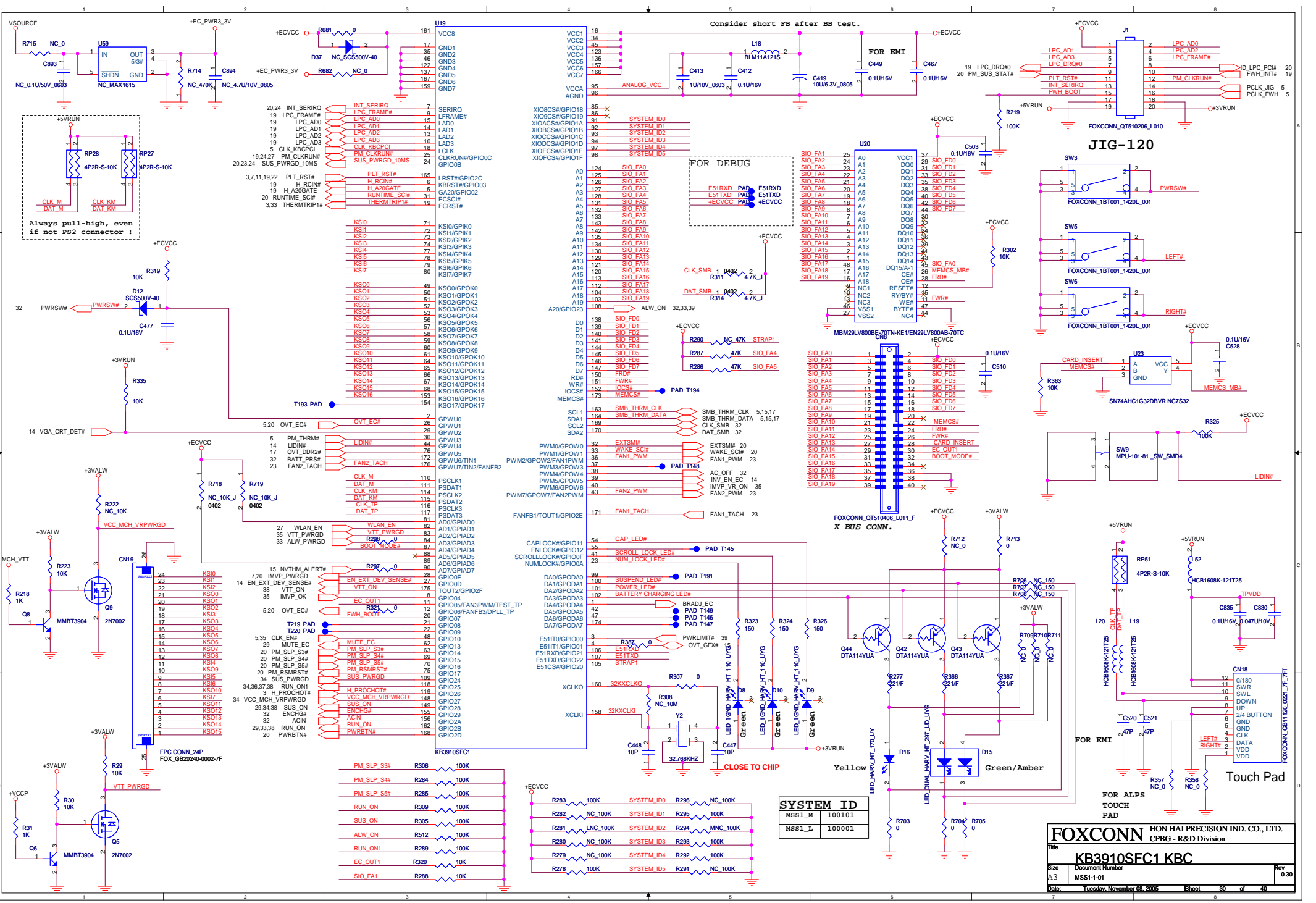


Match trace length

LAYOUT NOTES:

Match total length of chip side Rx and Tx pair traces +/-50mil
 Match length of cable side Rx and Tx pair traces +/- 50 mil
 Total line TX+ to TX- and RX- and RX+ should be matched within 50 mils.
 Keep 50mil space between pairs and other traces. Pairs are 100ohm differential,





Always pull-high, even if not PS2 connector!

Consider short FB after BB test.

JIG-120

SYSTEM ID	
MSS1_M	100101
MSS1_L	100001

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File: **KB3910SF1 KBC**

Size: A3 Document Number: MSS1-1-01 Rev: 0.30

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R283	100K	SYSTEM_ID0	R296	100K	NC_100K
R282	100K	SYSTEM_ID1	R295	100K	NC_100K
R281	100K	SYSTEM_ID2	R294	100K	MNC_100K
R280	100K	SYSTEM_ID3	R293	100K	NC_100K
R279	100K	SYSTEM_ID4	R292	100K	NC_100K
R278	100K	SYSTEM_ID5	R291	100K	NC_100K

R306	100K	PM_SLP_S3#
R284	100K	PM_SLP_S4#
R285	100K	PM_SLP_S5#
R309	100K	RUN_ON
R305	100K	SUS_ON
R512	100K	ALW_ON
R289	100K	RUN_ON1
R320	100K	EC_OUT1
R288	100K	SIO_FA1

Touch Pad

FOR ALPS TOUCH PAD

FOR EMI

FOR EMI

FOR EMI

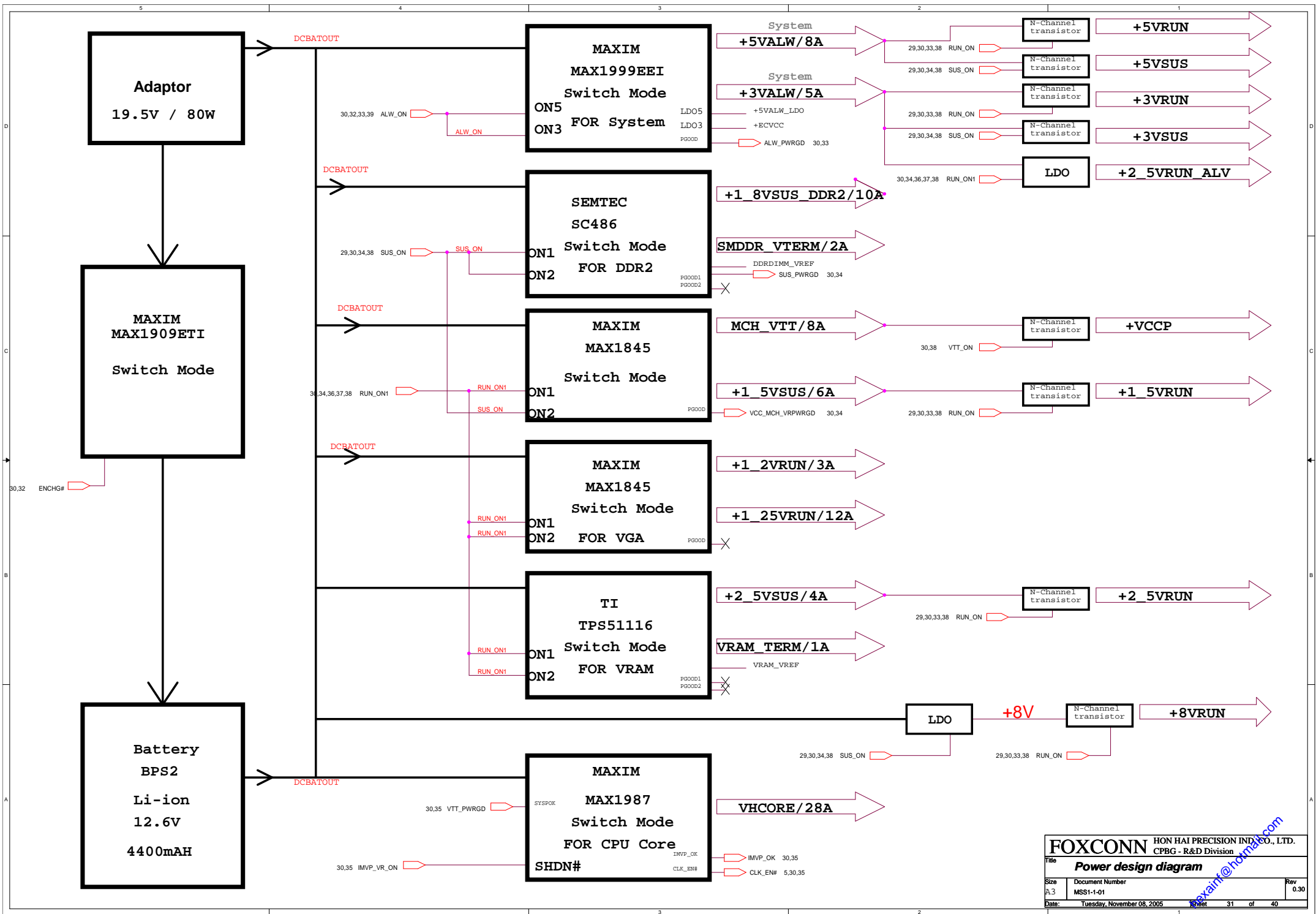
FOR EMI

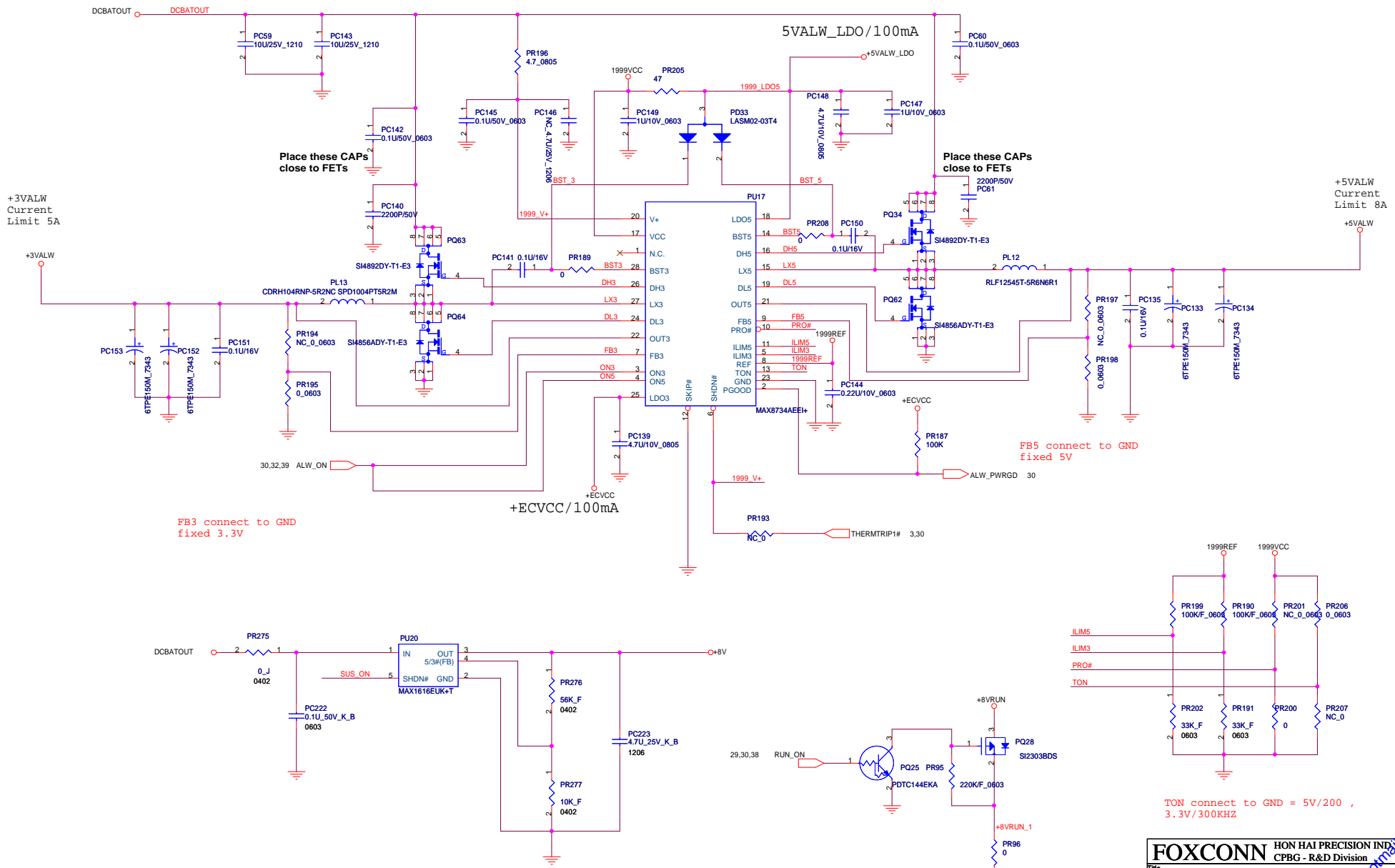
FOR EMI

FOR EMI

FOR EMI

FOR EMI

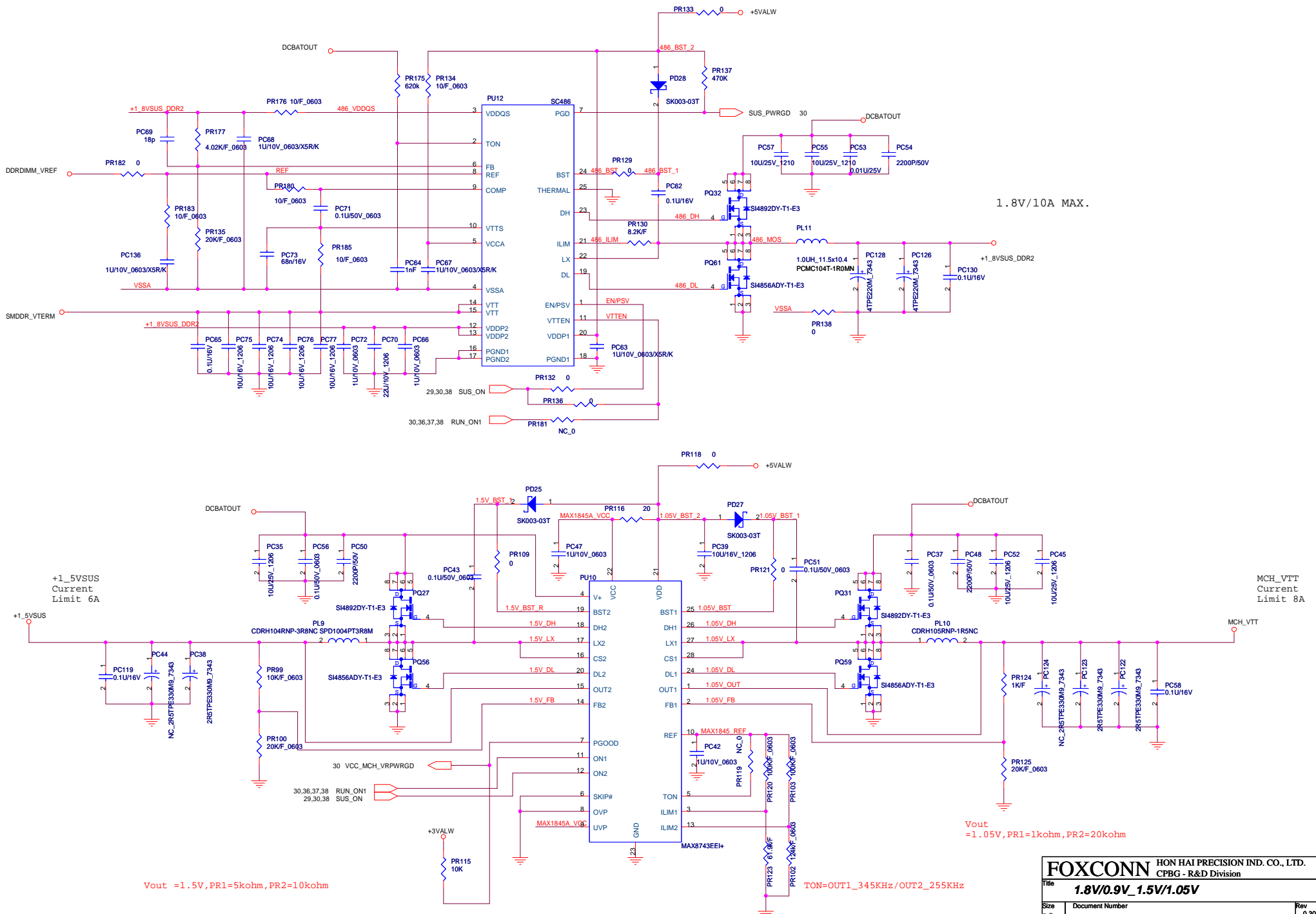




FB5 connect to GND fixed 5V

FB3 connect to GND fixed 3.3V

TON connect to GND = 5V/200, 3.3V/300KHZ



1.8V/10A MAX.

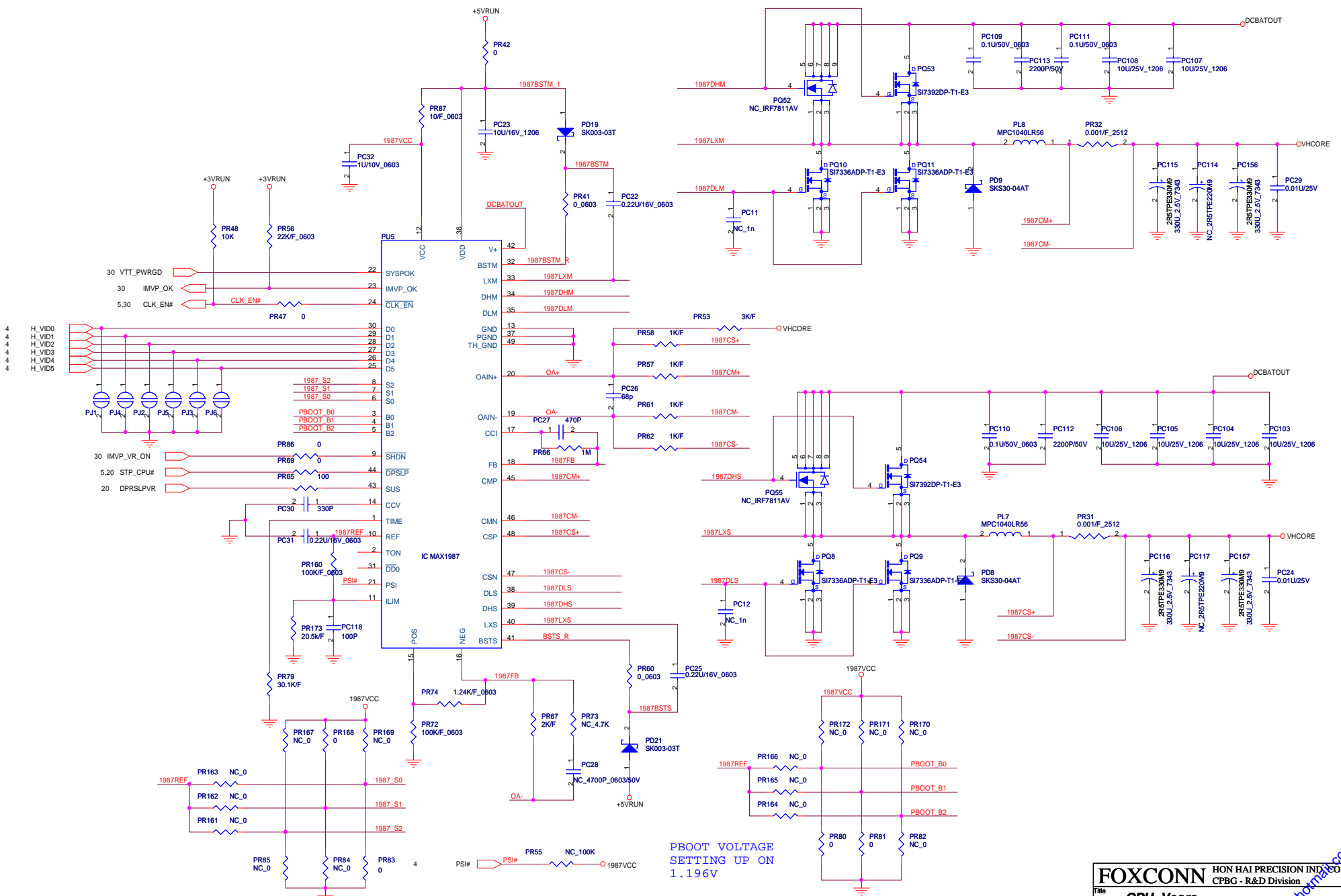
MCH_VTT
Current
Limit 8A

Vout = 1.05V, PR1=1kohm, PR2=20kohm

Vout = 1.5V, PR1=5kohm, PR2=10kohm

TON=OUT1_345KHz/OUT2_255KHz

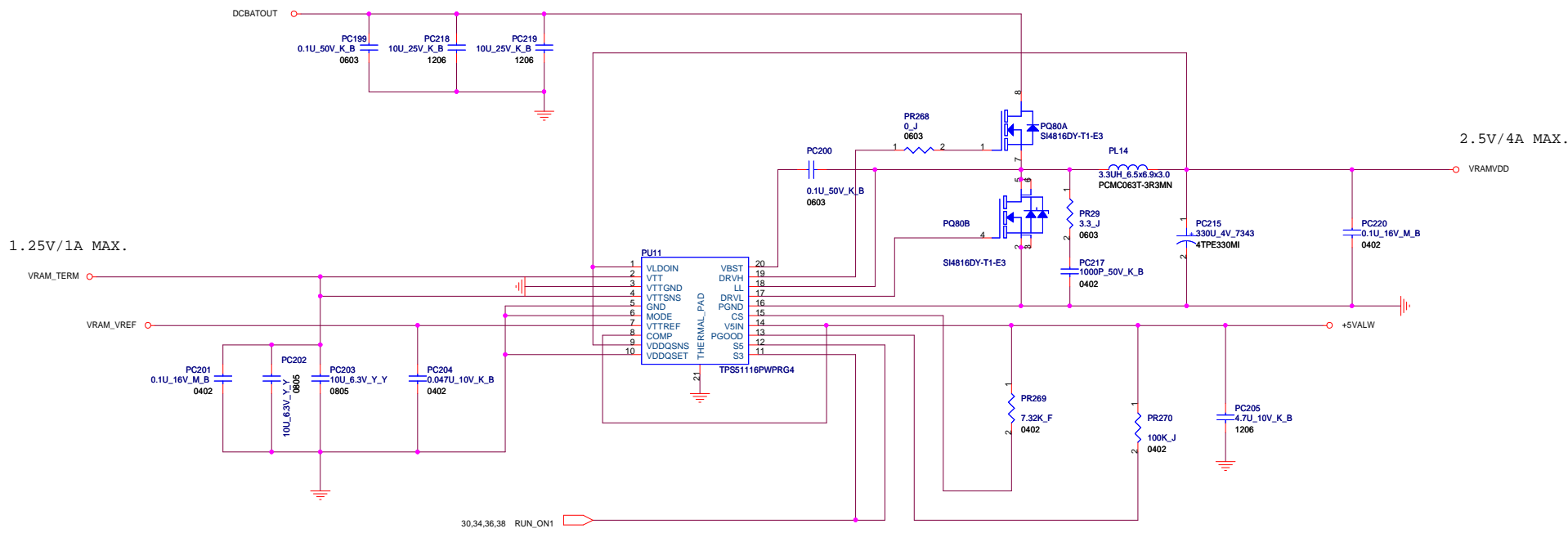
FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
1.8V/0.9V_1.5V/1.05V		
Size	Document Number	Rev
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Date:	Tuesday, November 08, 2006	Sheet 34 of 40



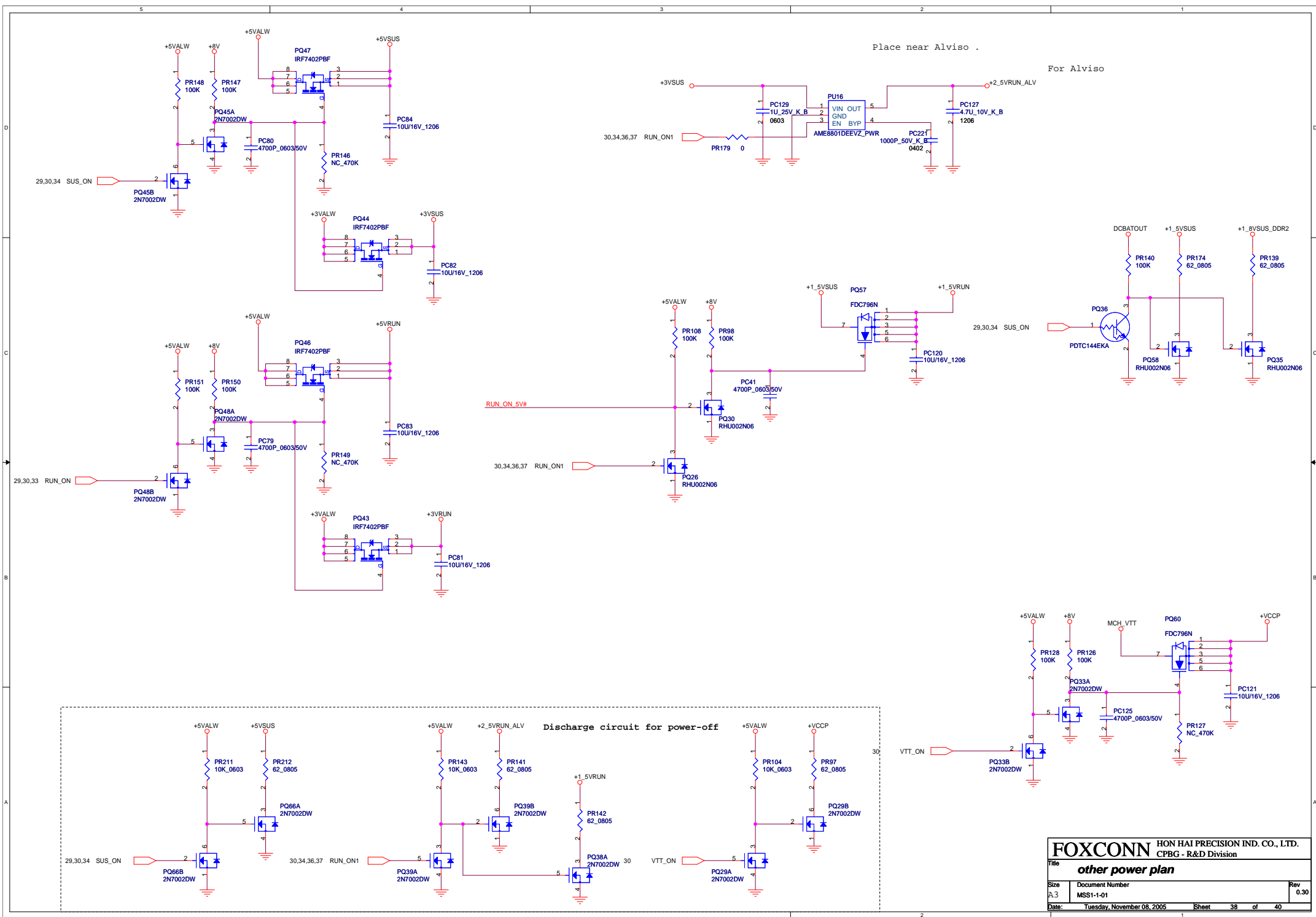
The C4 mode voltage is 0.748V TON= 300KHZ

BBOOT VOLTAGE
SETTING UP ON
1.196V

FOXCONN HON HAI PRECISION IND. CO., LTD.	
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Title CPU_Vcore	
Size A.3	Document Number MSS1-1-01
Date: Tuesday, November 08, 2006	Sheet 35 of 40



FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
VRAM 2.5V/1.25V		
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Date:	Tuesday, November 08, 2005	Sheet 37 of 40

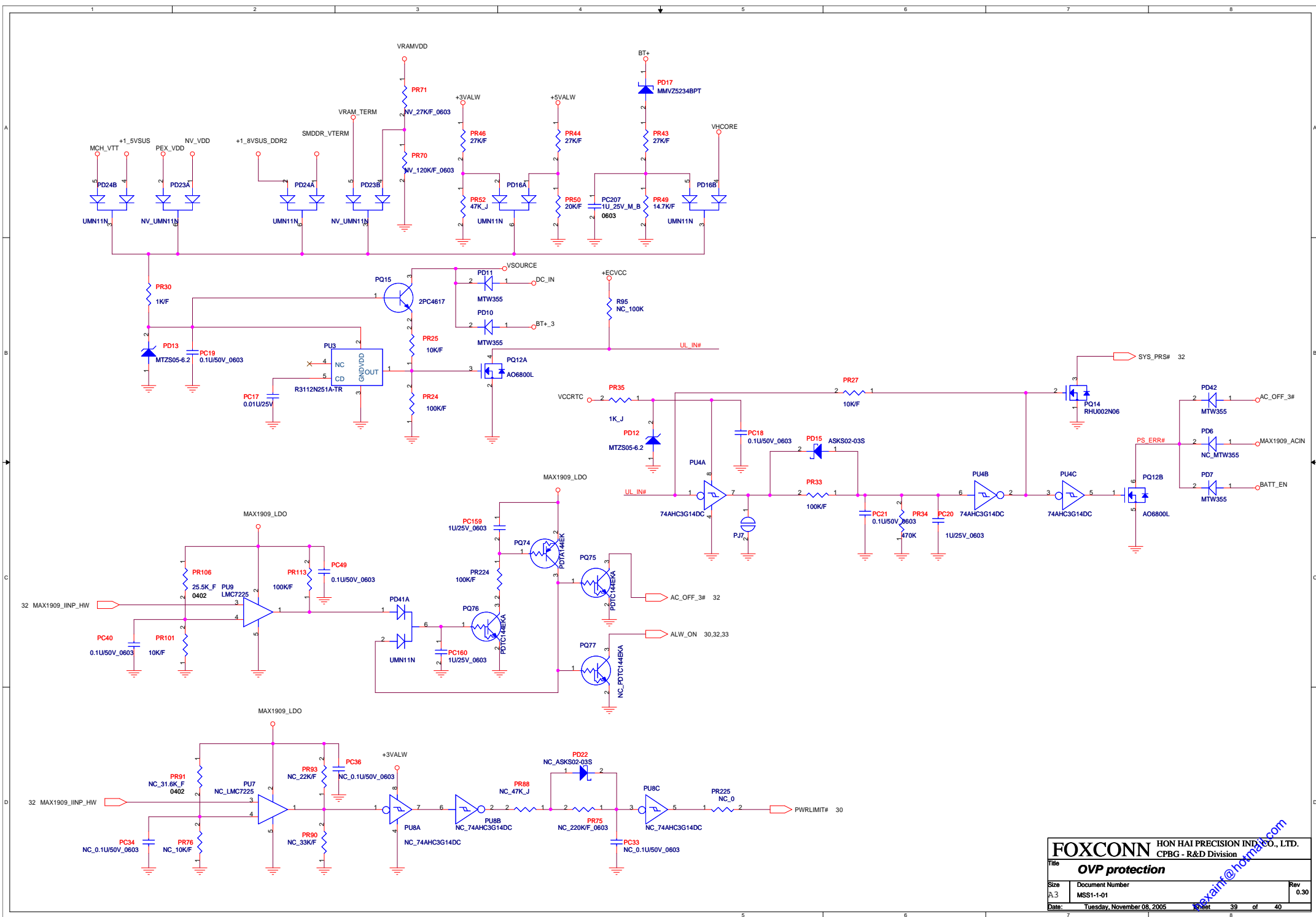


Place near Alviso .

For Alviso

Discharge circuit for power-off

FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	other power plan	
Size	Document Number	Rev
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Date:	Tuesday, November 08, 2005	Sheet 38 of 40



HISTORY

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
HISTORY (1)			
Size	Document Number	Rev	
A3	MSS1-1-01	0.30	
Date:	Tuesday, November 08, 2005	Sheet	40 of 40