Schematics Page Index (Title / Revision / Change Date)

Value	MS50/GM	MS50/PM	MS30/GM	MS30/PM
MS30_			V	V
MS50_	V	V		
CA_	V		V	
NV_		V		V
NC_	V	V	V	V

P. Leader	Check by	Design by

PCB P/N: __-_____-__SA
__-_____-__SA
__-_____-__SA

Project Code & Schematics Subject: MS31/51 Main Board

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: ***Index Page***

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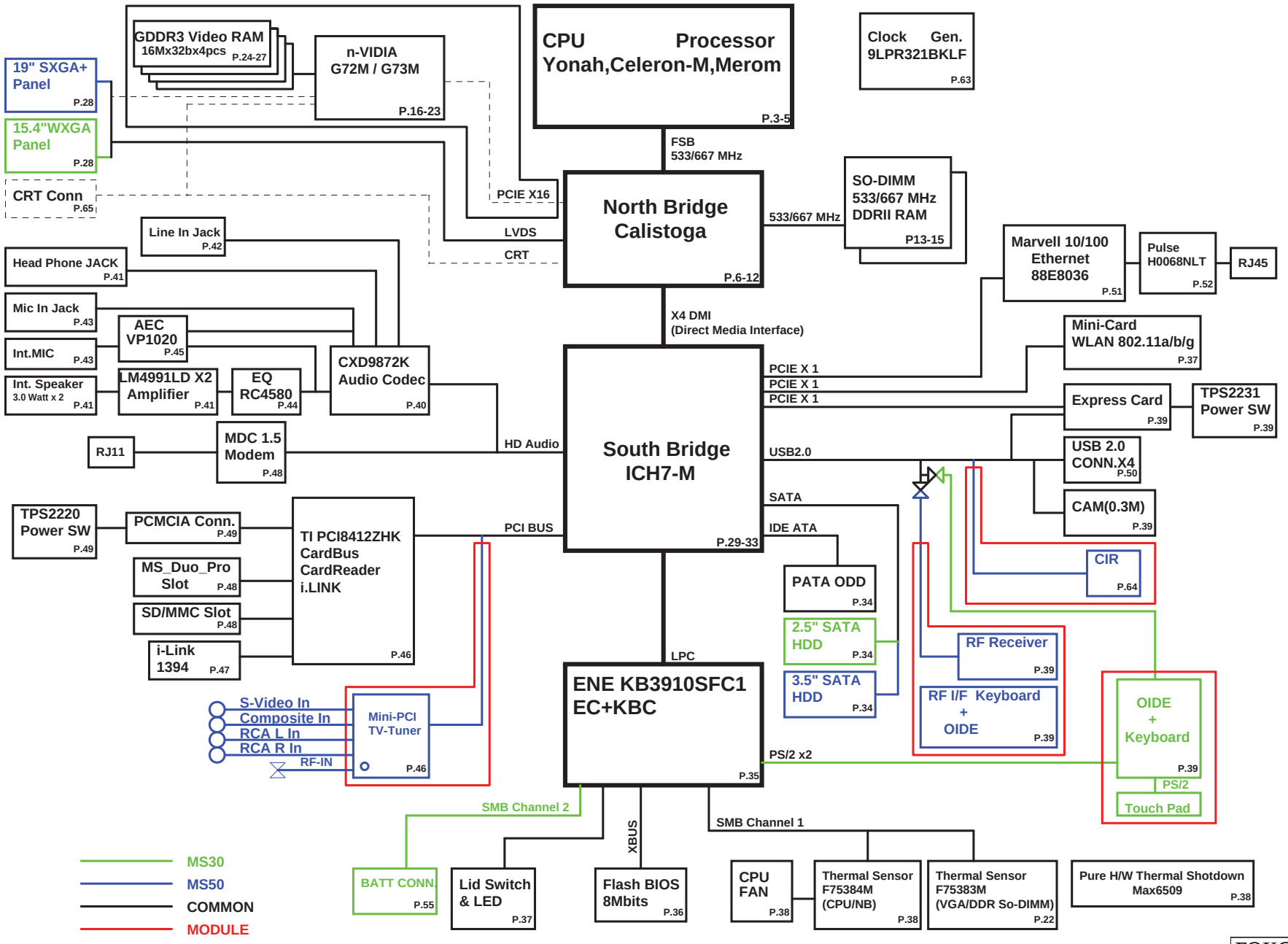
http://laptop-motherboard-schematic.blogspot.com/

MBX-152(CALISTOGA PM/GM+Gfx Block Diagram



SYSTEM DC/DC MAX8734A P.56

INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC

SYSTEM DC/DC MAX8743

INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VRUN

SC486

DCBATOUT	+1_8VSUS +0_9VRUN

CPU DC/DC MAX8771 P.59

INPUTS	OUTPUTS
DCBATOUT	VHCORE

AMP DC/DC MAX668 P.60

INPUTS	OUTPUTS
+5VALW	+12VRUN

SYSTEM DC/DC SC1470/GMT966 (external VGA Core) P.63

INPUTS	OUTPUTS
DCBATOUT +1_5VRUN	PEX_VDD NV_VDD

MAXIM CHARGER MAX1909 P.54

INPUTS	OUTPUTS
AD+	BT+ DCBATOUT

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Title: Block Diagram (All)

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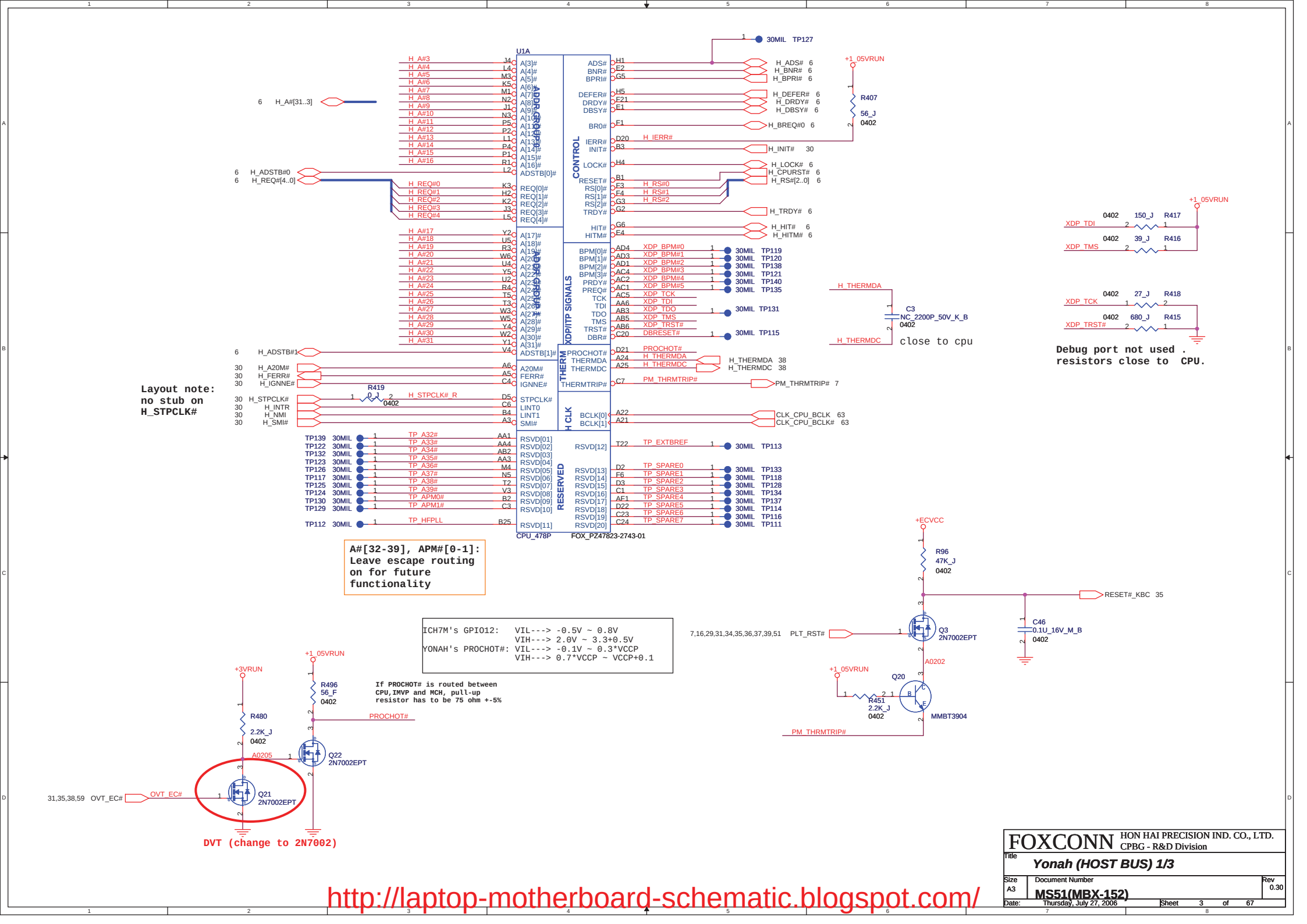
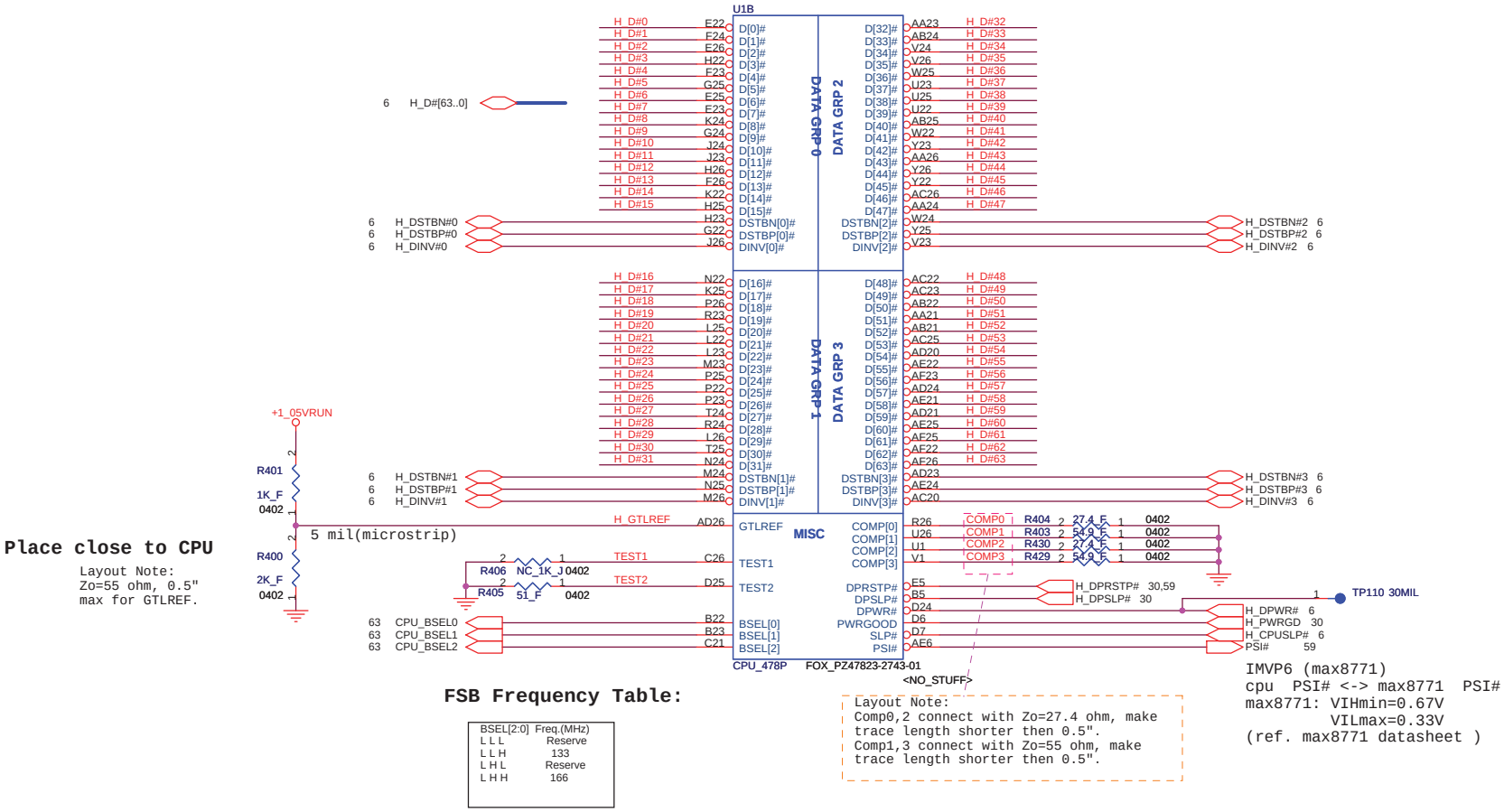


http://laptop-motherboard-schematic.blogspot.com/



Place close to CPU

Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

FSB Frequency Table:

BSEL[2:0]	Freq.(MHz)
L L L	Reserve
L L H	133
L H L	Reserve
L H H	166

Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5".
Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5".

IMVP6 (max8771)
cpu PSI# <-> max8771 PSI#
max8771: VIHmin=0.67V
VILmax=0.33V
(ref. max8771 datasheet)

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Title: *Yonah (HOST BUS) 2/3*

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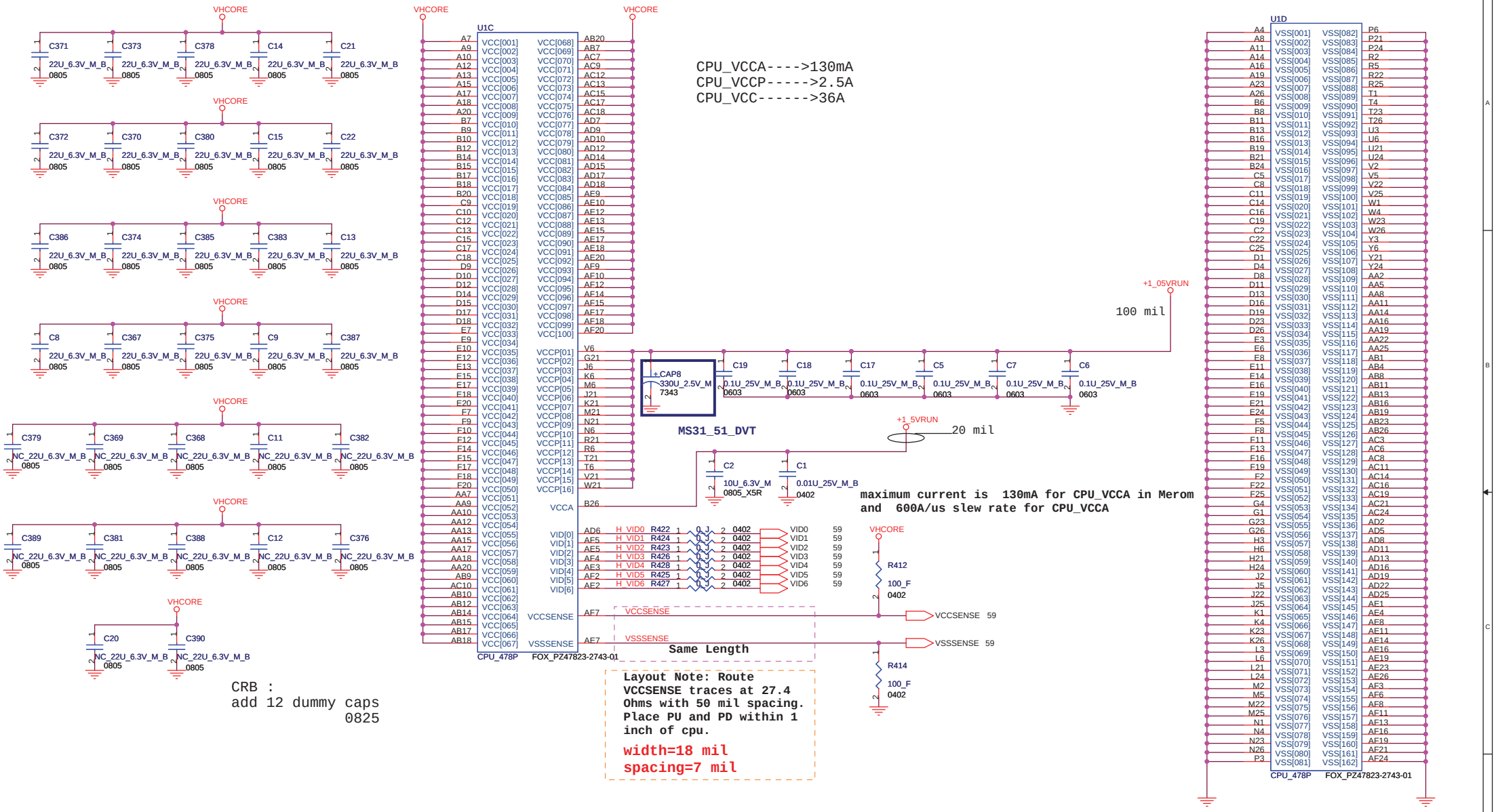

CRB :
add 12 dummy caps
0825

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FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*Yonah (POWER/GROUND) 3/3*	
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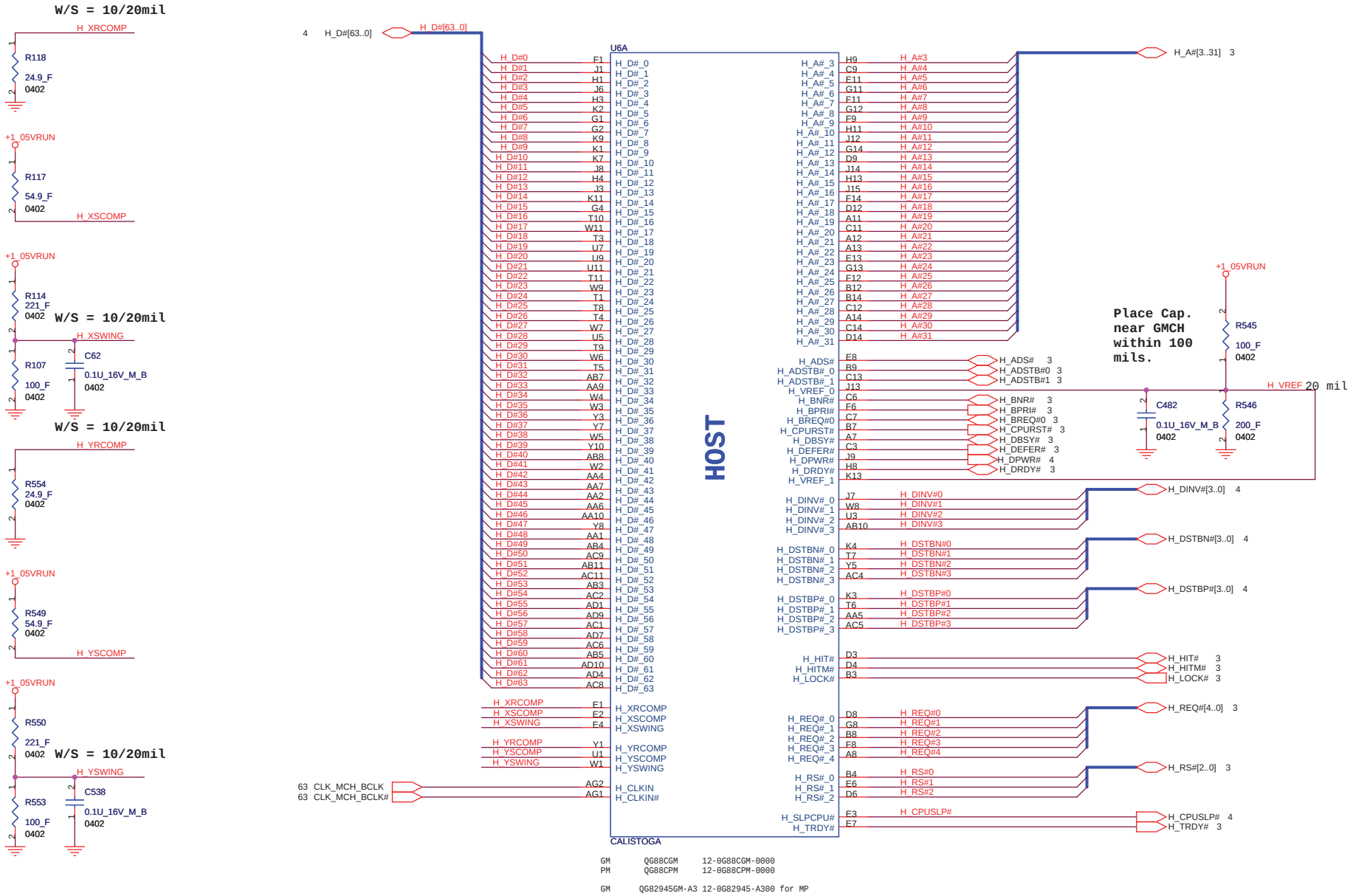

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	CALISTOHA (HOST)		
Size A3	Document Number MS51(MBX-152)		Rev 0.30
Date: Thursday, July 27, 2006	Sheet 6 of 67		

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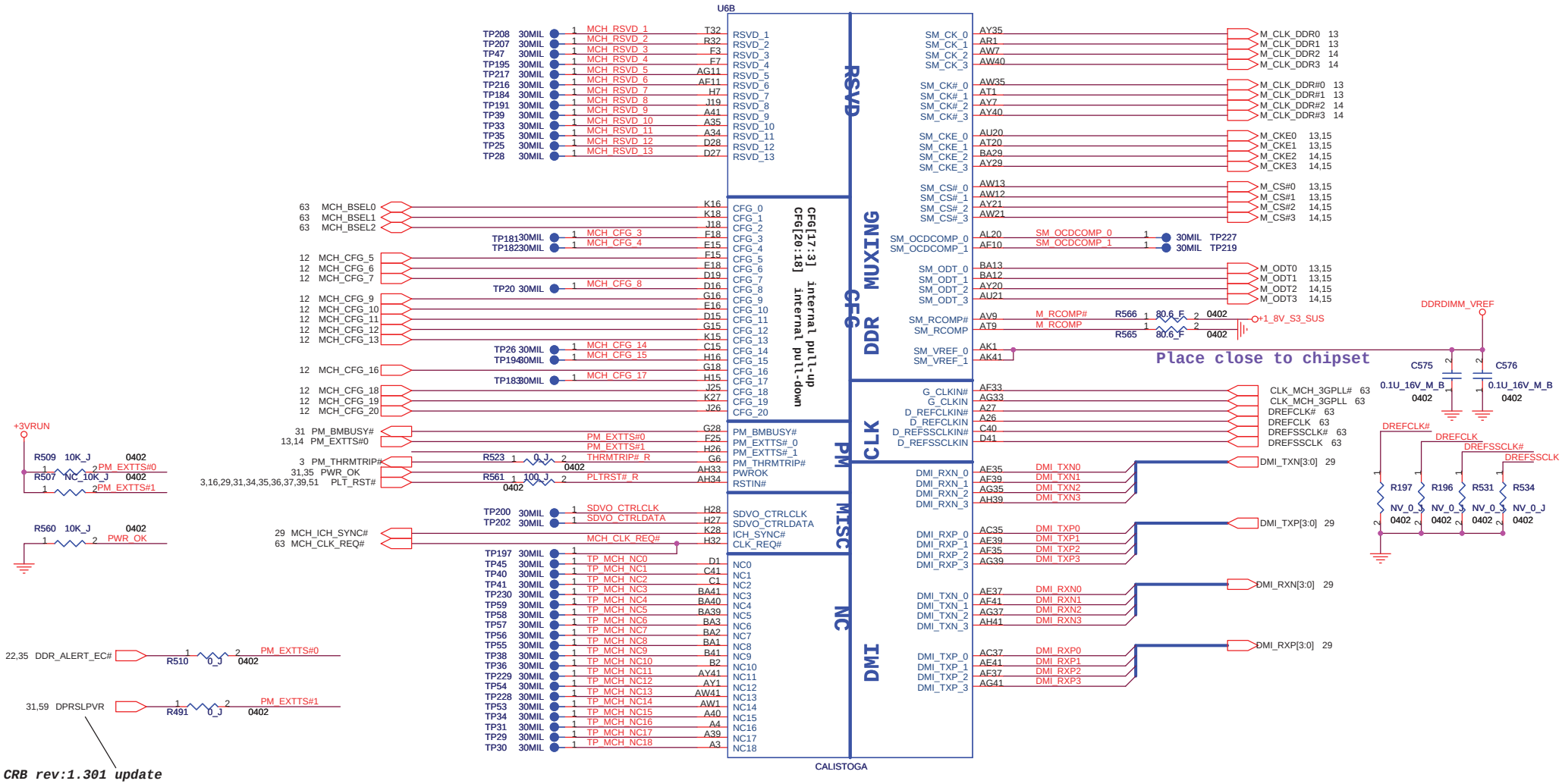

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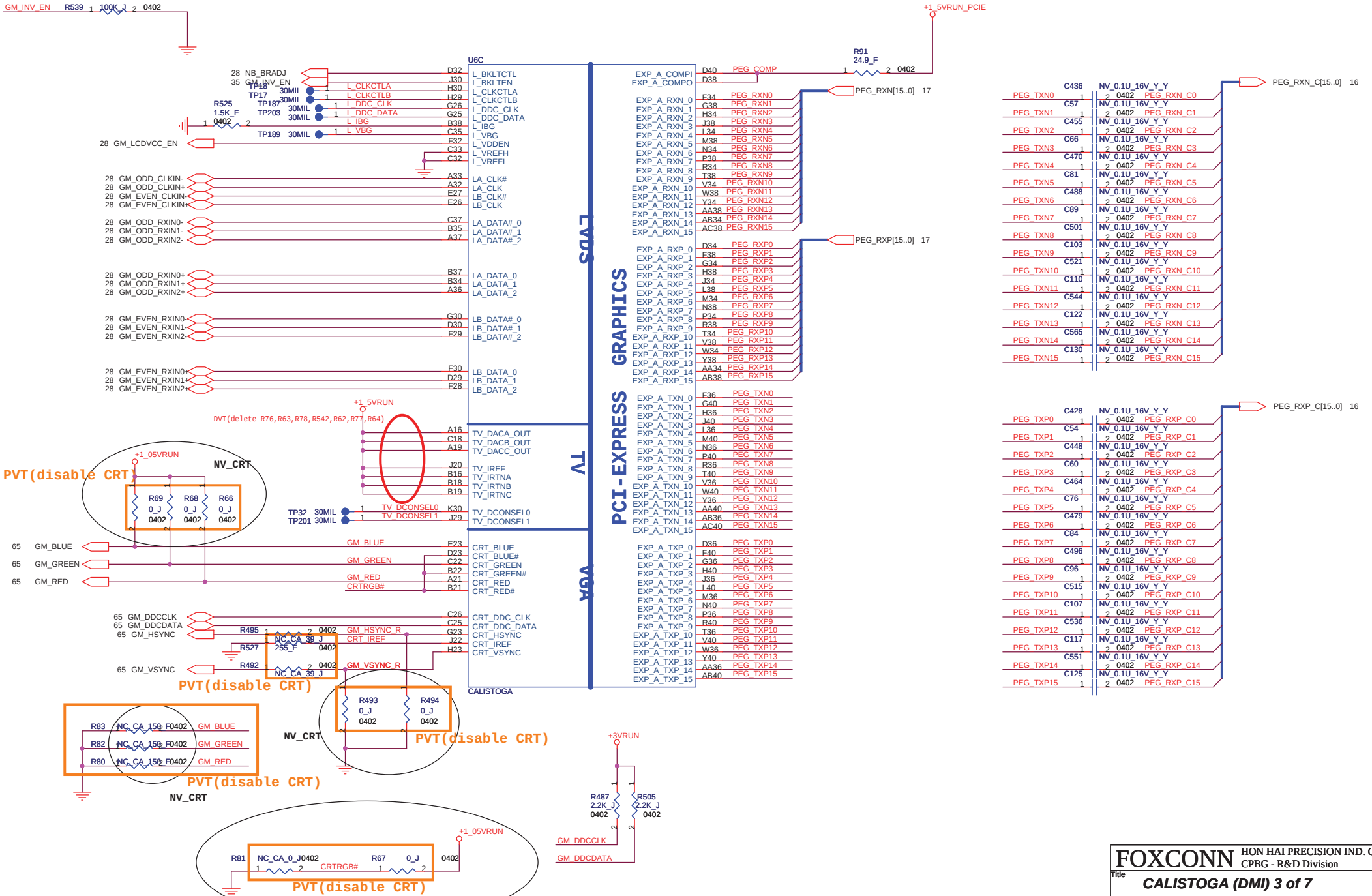
Title: CALISTOGA (DMI) 2 of 7

Size: A3 | Document Number: MS51(MBX-152) | Rev: 0.30

Date: Thursday, July 27, 2006 | Sheet 7 of 67



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Title: CALISTOGA (DMI) 3 of 7

Size: A3 | Document Number: MS51(MBX-152) | Rev: 0.30

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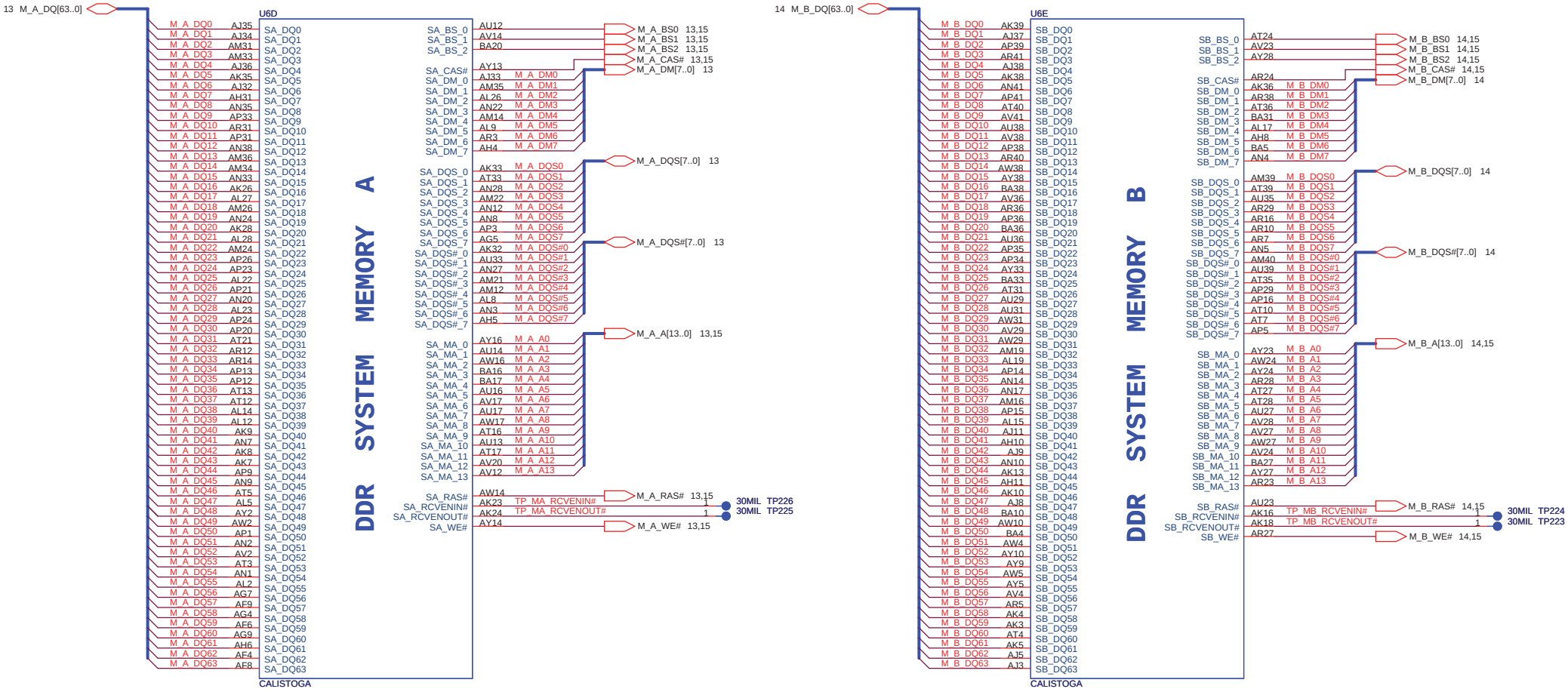

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Title: CALISTOGA (DDRII) 4 of 7

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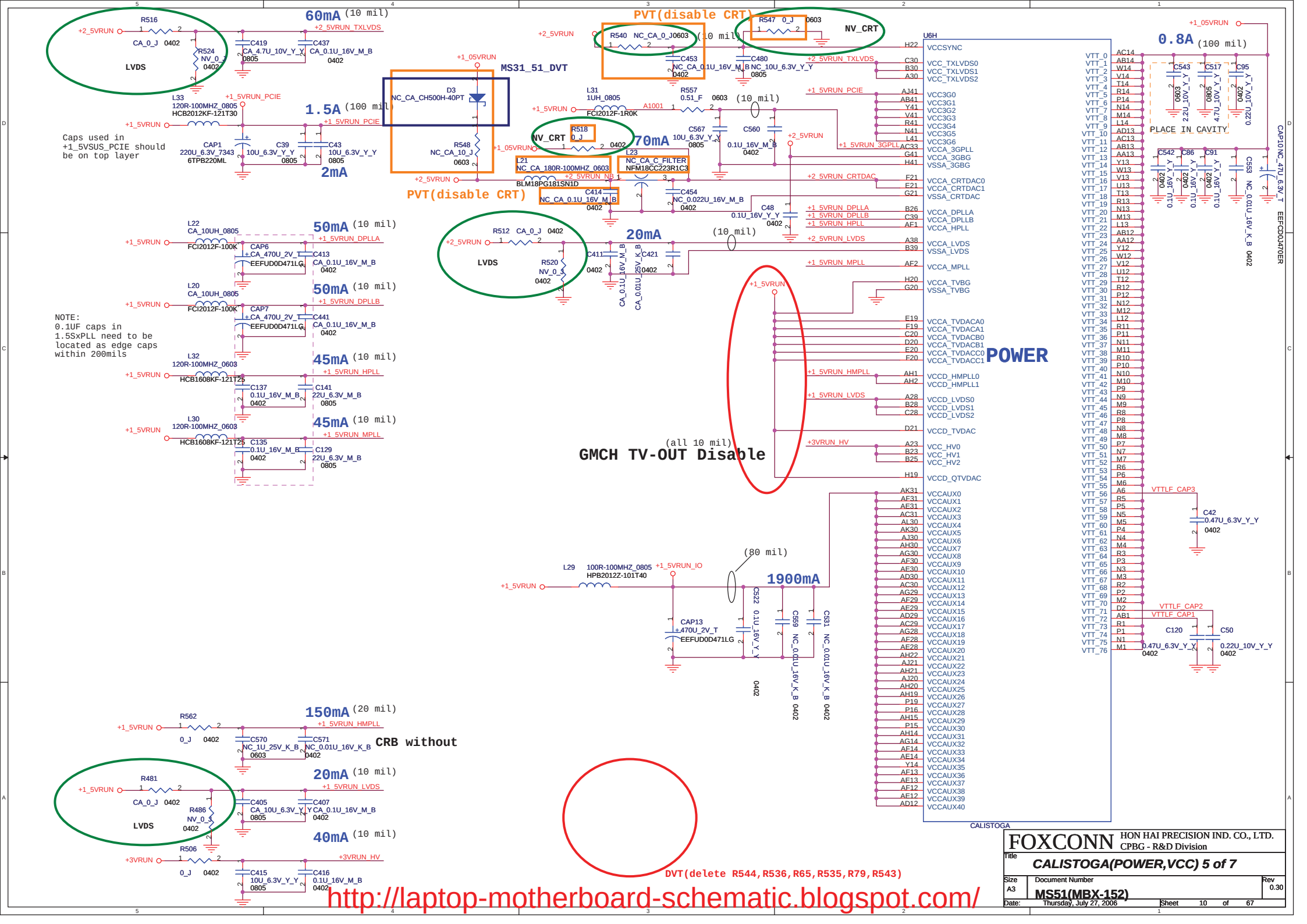

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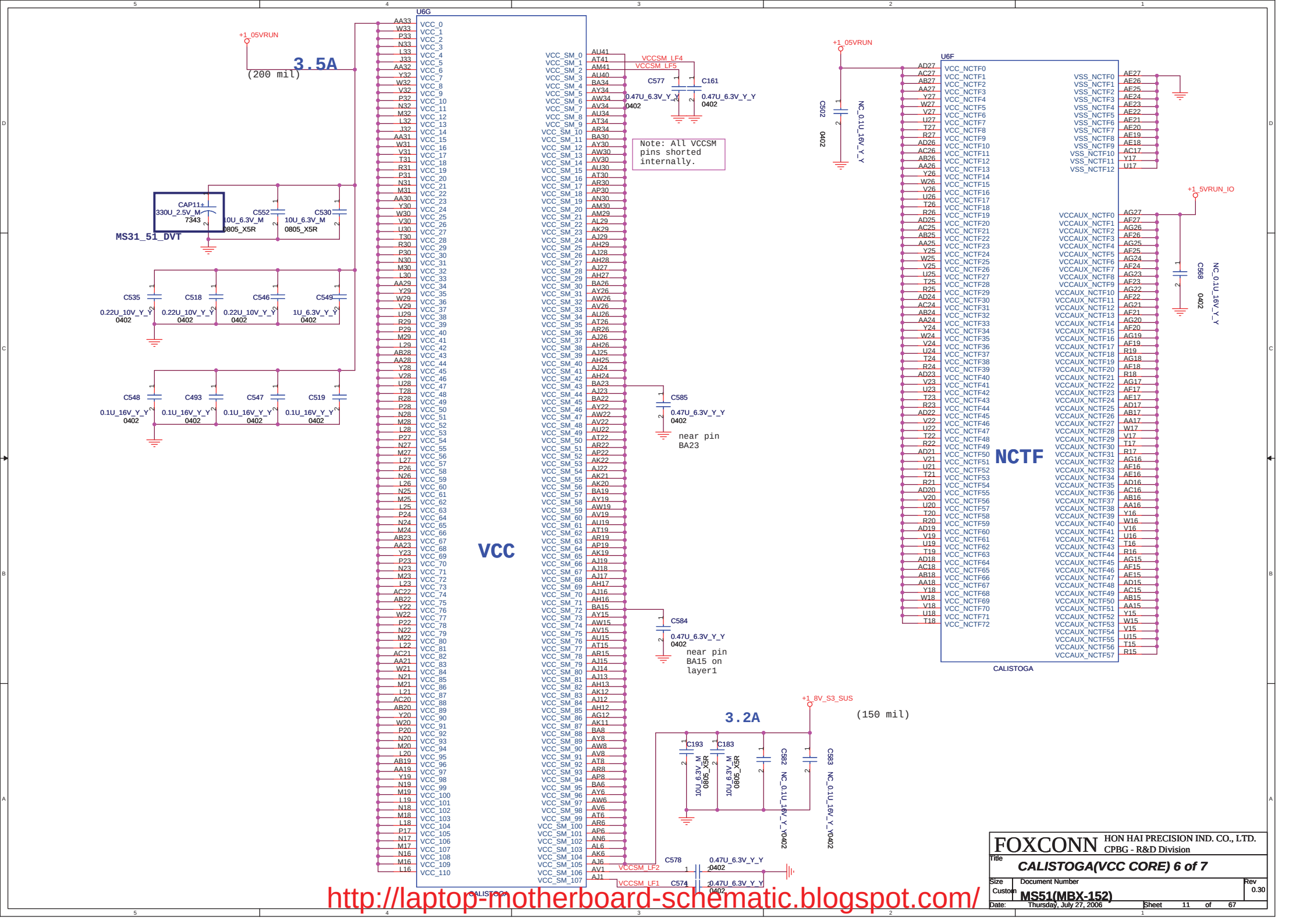

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Title: CALISTOGA(VCC CORE) 6 of 7

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7 MCH_CFG_5 — 1 — 30MIL TP193

MCH_CFG_5	Low = DMIx2 High = DMIx4

7 MCH_CFG_6 — 1 — 30MIL TP180

MCH_CFG_6	Low = Moby Dick High = Calistoga

DDR2 select (default high)

7 MCH_CFG_7 — 1 — 30MIL TP15

MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor

7 MCH_CFG_9 — 1 — 30MIL TP250

DVT (delete R514,add TP)

MCH_CFG_9 (PCIE Graphics Lane)	Low = Reverse Lane High = Normal operation

For layout convenience

7 MCH_CFG_10 — 1 — 30MIL TP192

MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY

7 MCH_CFG_11

MCH_CFG_11 (PSB 4x CLK ENABLE)	Low = Reserved High= Calistoga

R85 NC_2.2K_J 0402

7 MCH_CFG_12 — 1 — 30MIL TP185
7 MCH_CFG_13 — 1 — 30MIL TP205

MCH_CFG_[13:12] (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)

7 MCH_CFG_16 — 1 — 30MIL TP178

MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable

MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V

7 MCH_CFG_18 — 1 — 30MIL TP248

DVT (delete R508,add TP)

MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED

7 MCH_CFG_19 — 1 — 30MIL TP249

DVT (delete R541,add TP)

MCH_CFG_20 (PCIe Backward Interpoerability mode)	Low = Only SDVO or PCIE x1 is operational (defaults)) High = SDVO and PCIE x1 are operating simultaneously via the PEG port

7 MCH_CFG_20 — 1 — 30MIL TP204

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub

Check CALISTOGA version , after A2 version , if systec can't boot up then NC the pull low R

U6I

VSS

CALISTOGA

U6J

VSS

CALISTOGA

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Title: CALISTOGA(VSS) 7 of 7

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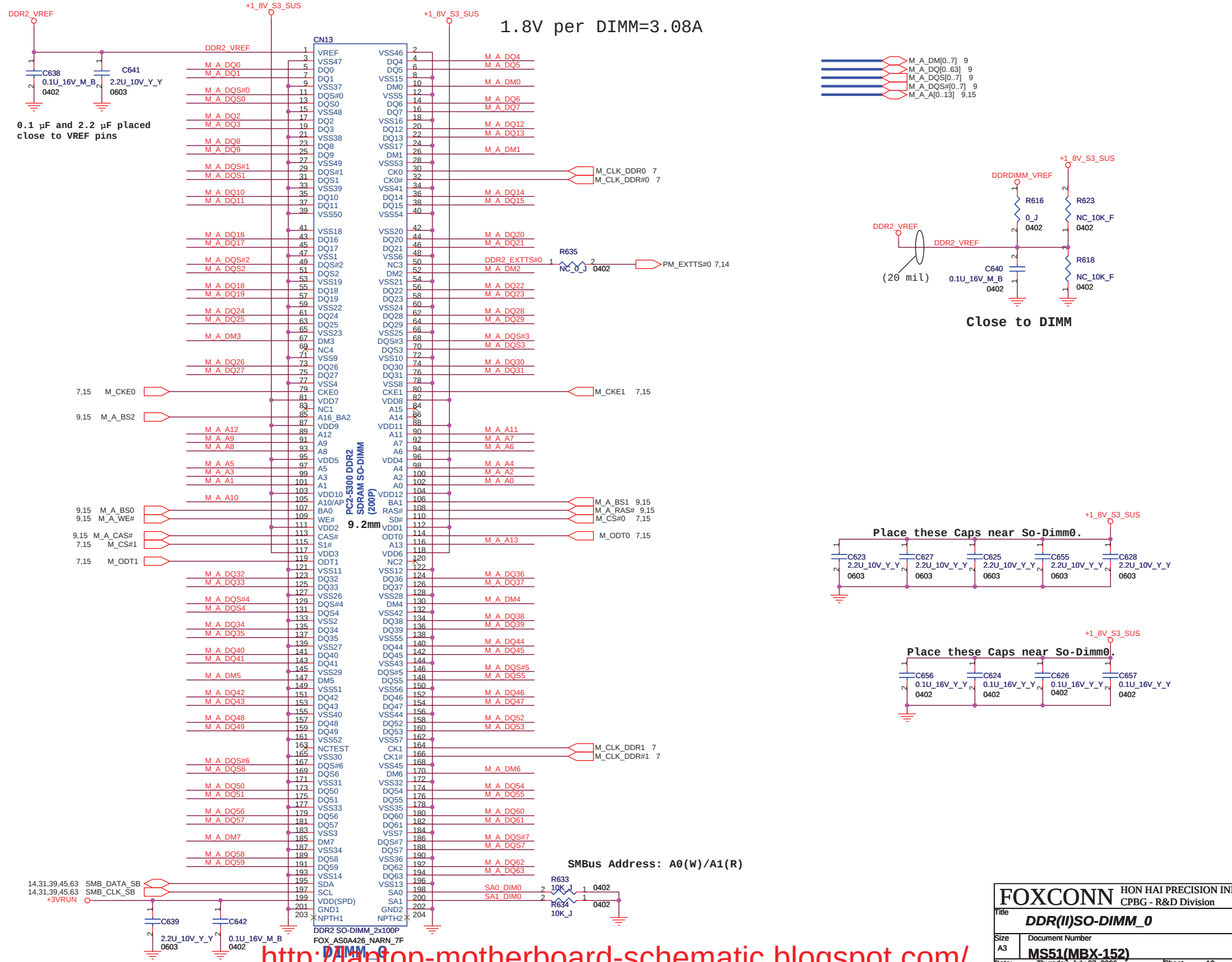

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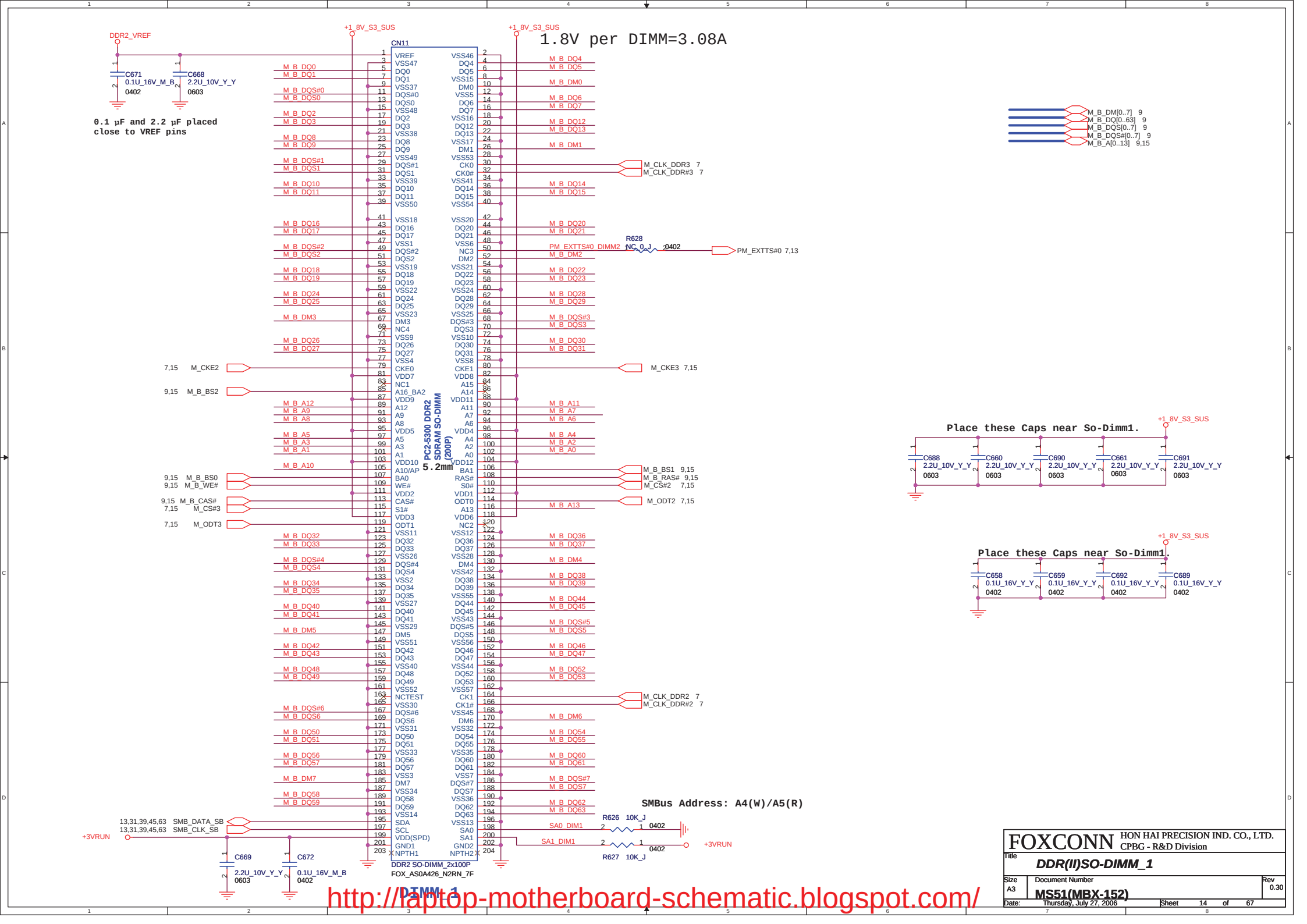

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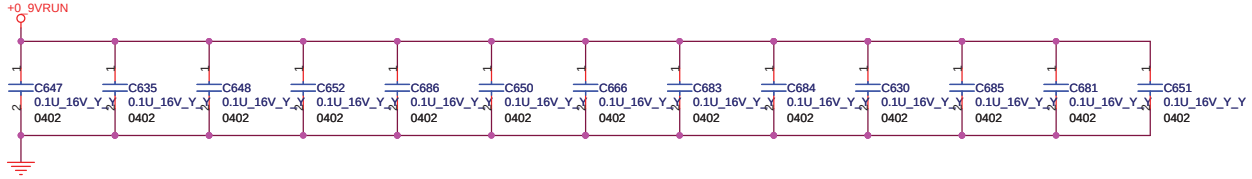
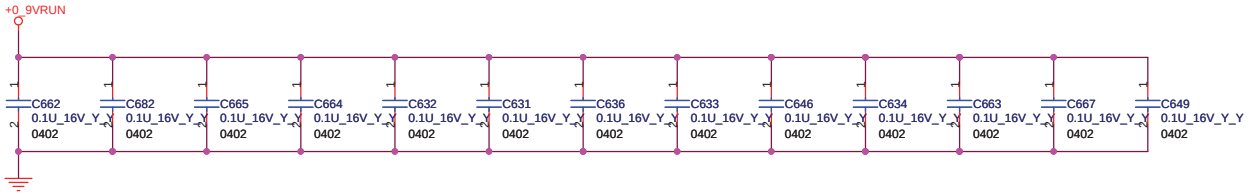
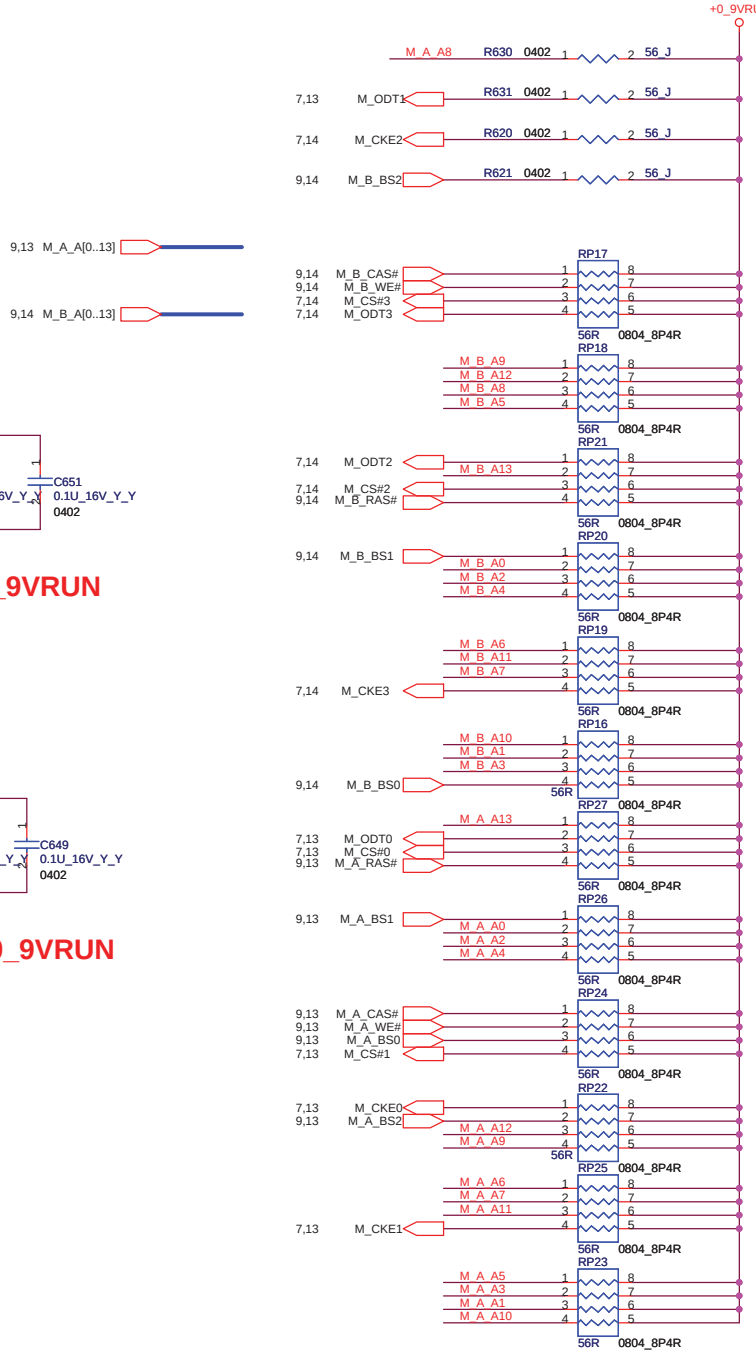


Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



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Title: ***DDR(II)Termination***

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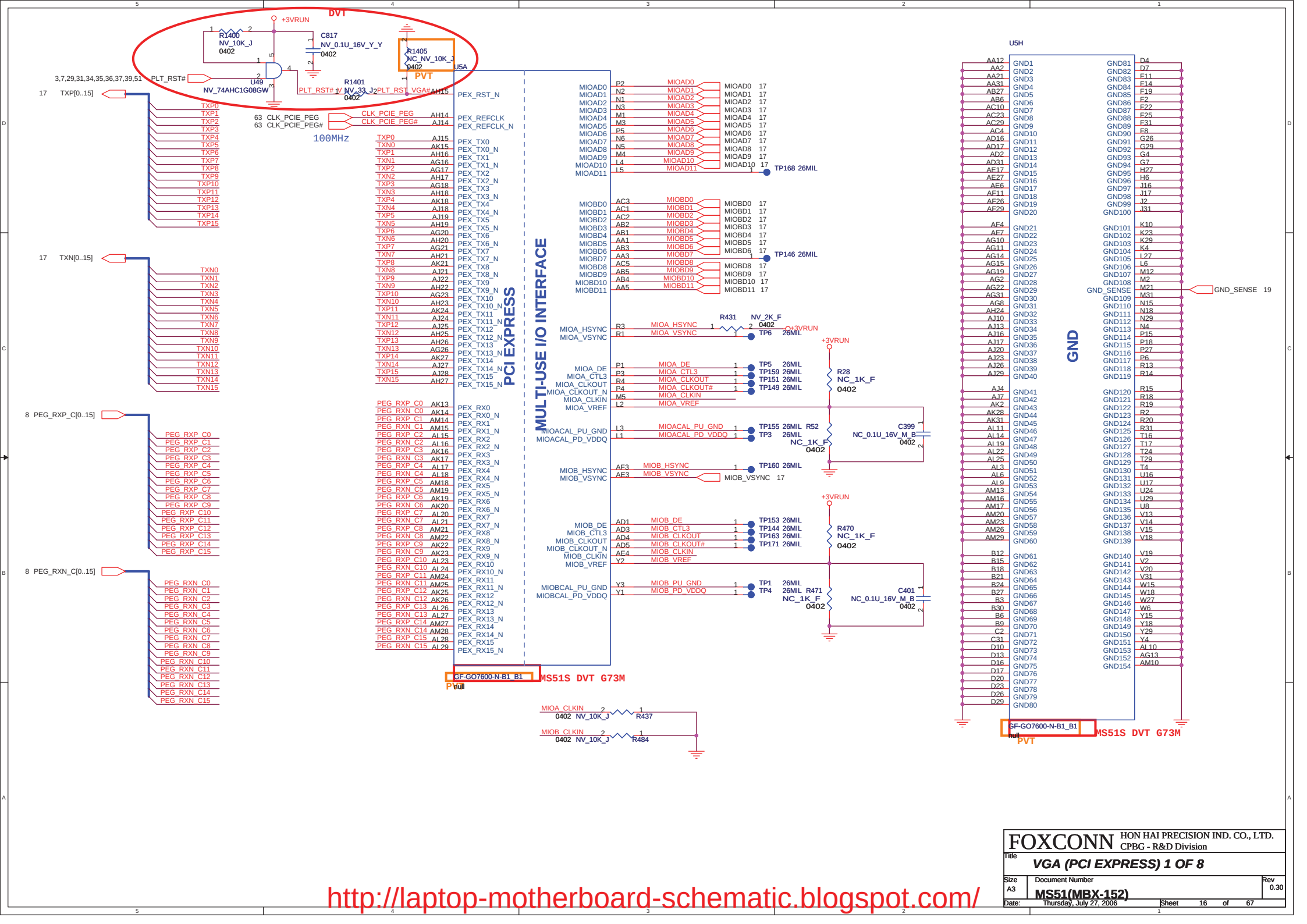

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Title: VGA (PCI EXPRESS) 1 OF 8

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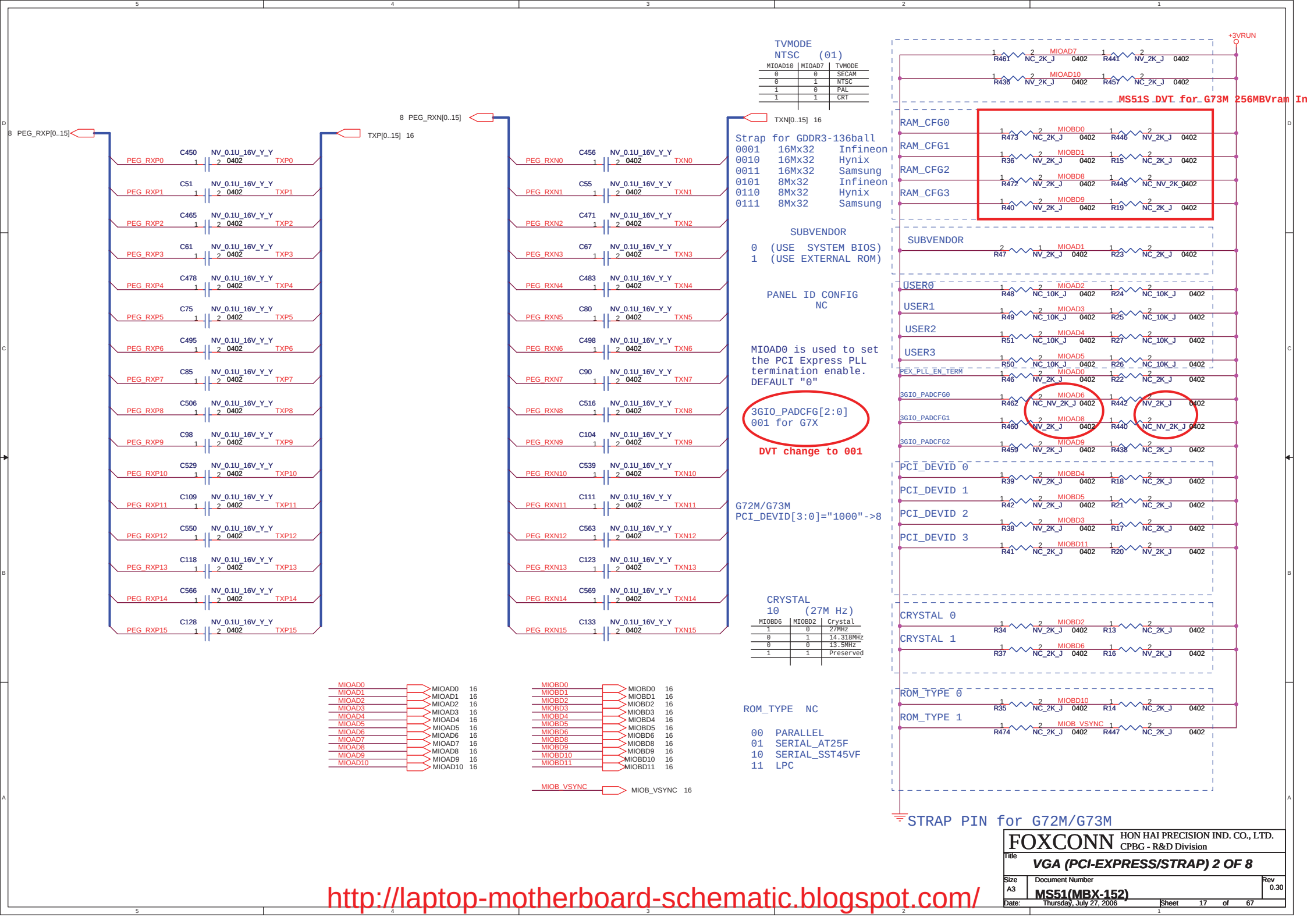

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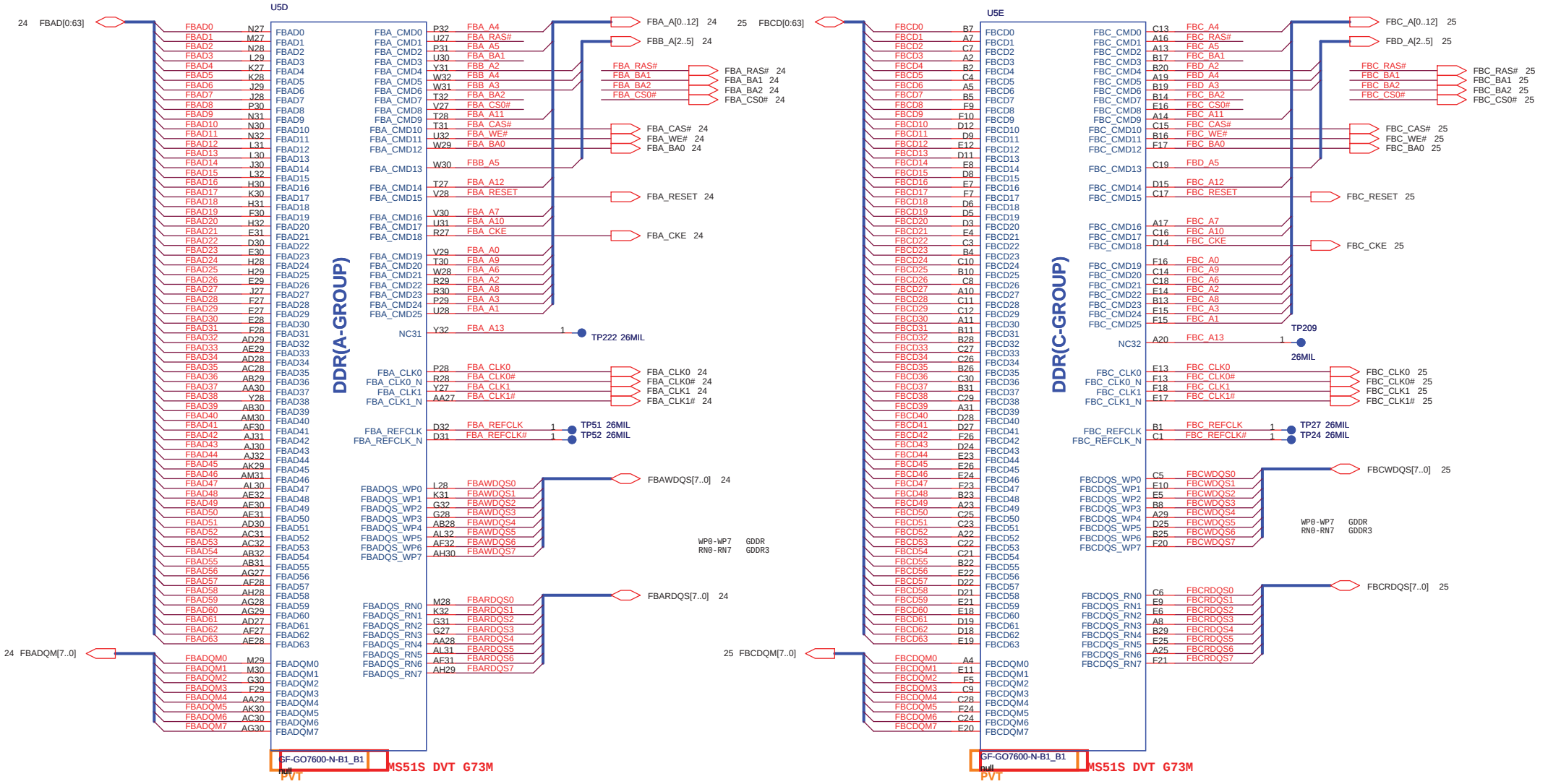

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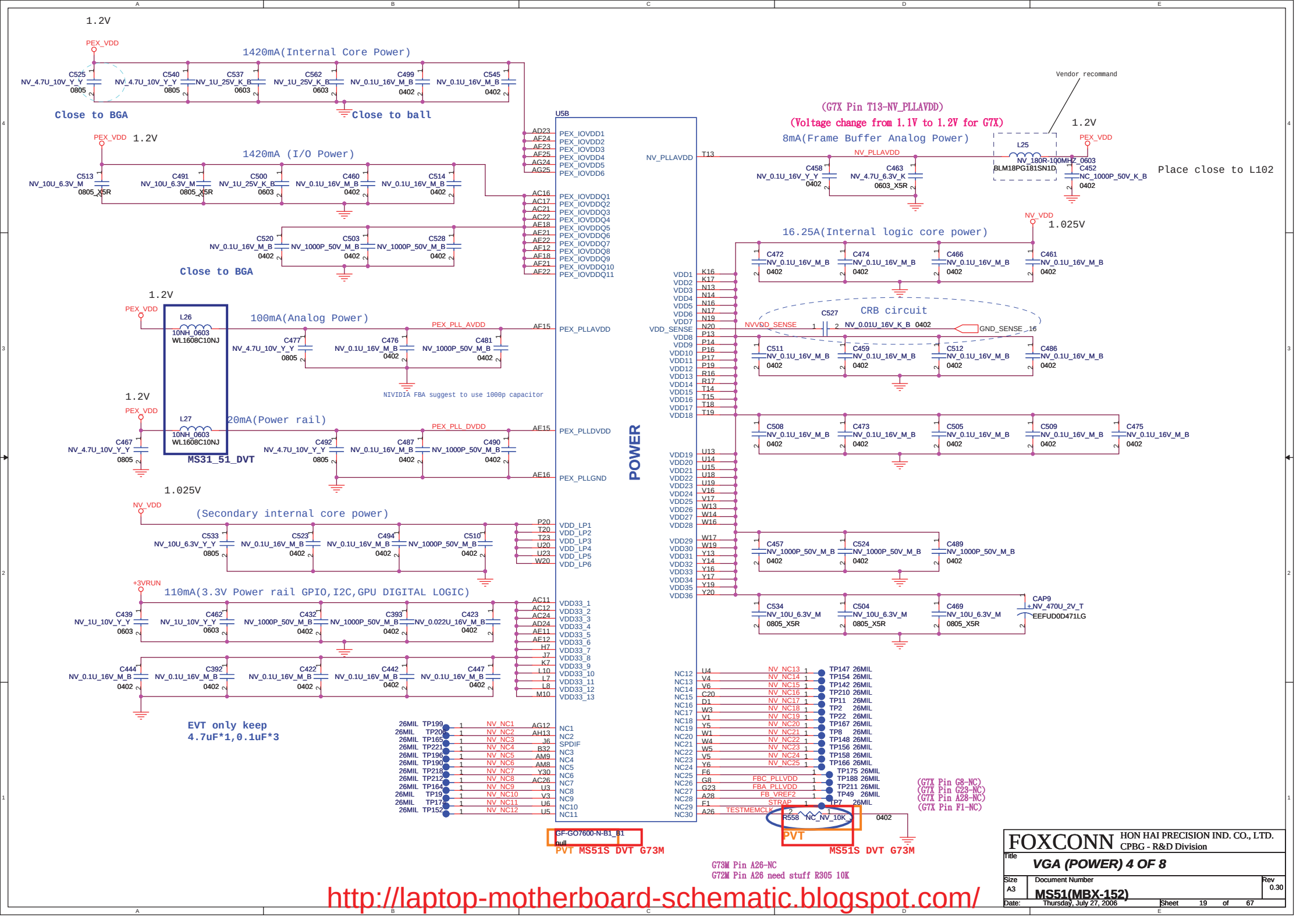

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Title	VGA (POWER) 4 OF 8
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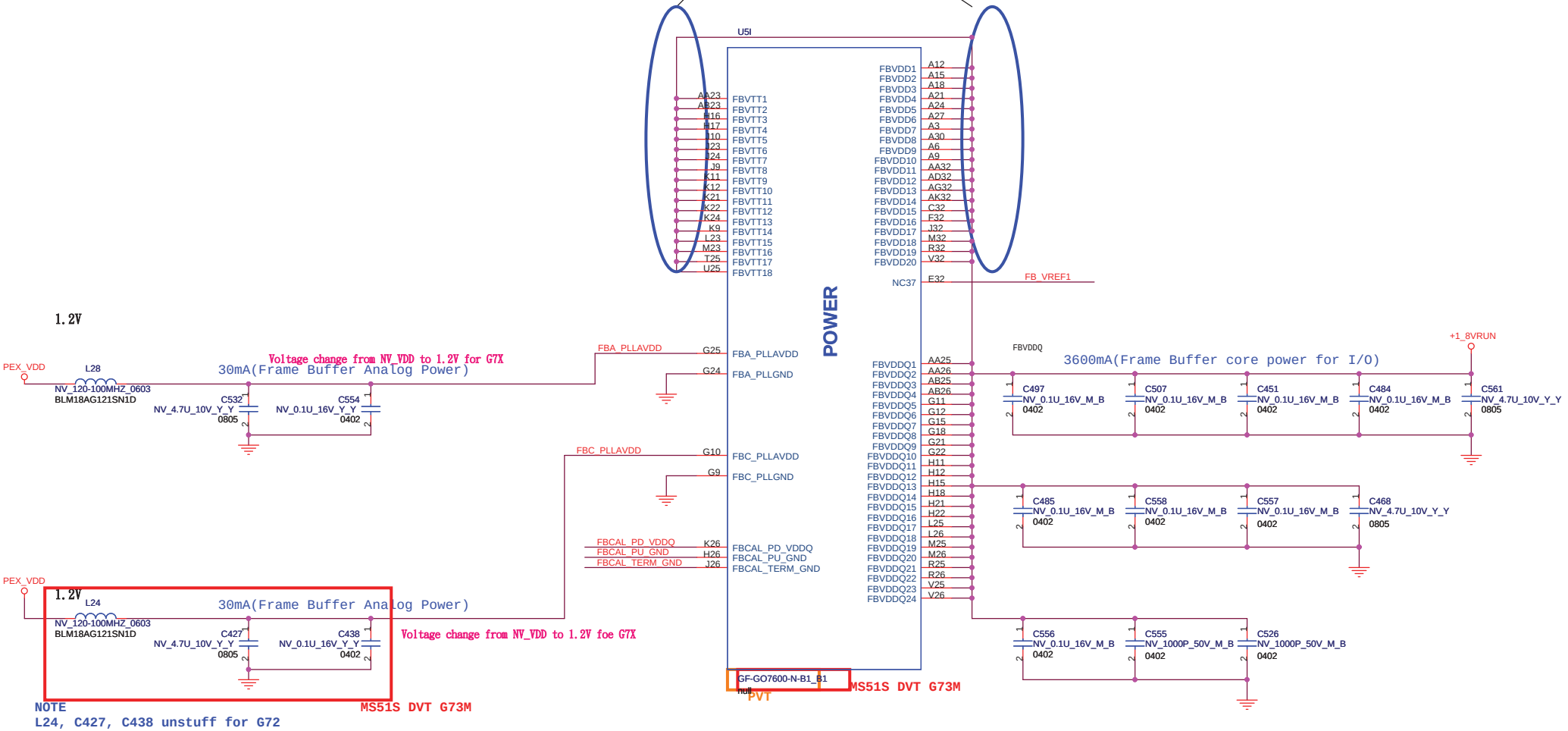
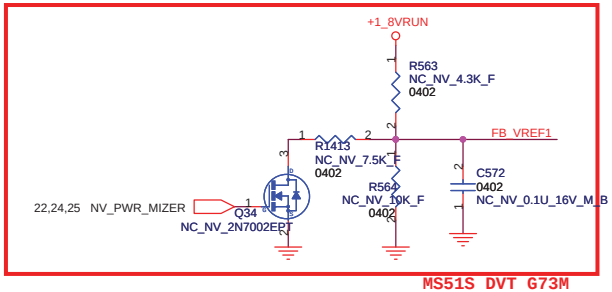
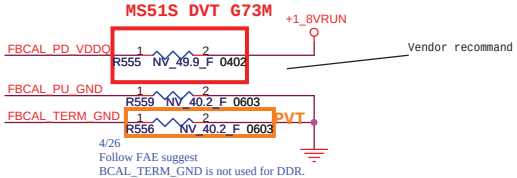
Follow FAE suggest the design guide table 4-4 and 4-5.
DDR1 underminated solution,so FBVTT/FBVDDQ/FBVDD can connect together.
for the power rails decoupling,FBVTT/FBVDD do not require caps decoupling.
only FVDDQ power rail required.







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Title: VGA (POWER) 5 OF 8

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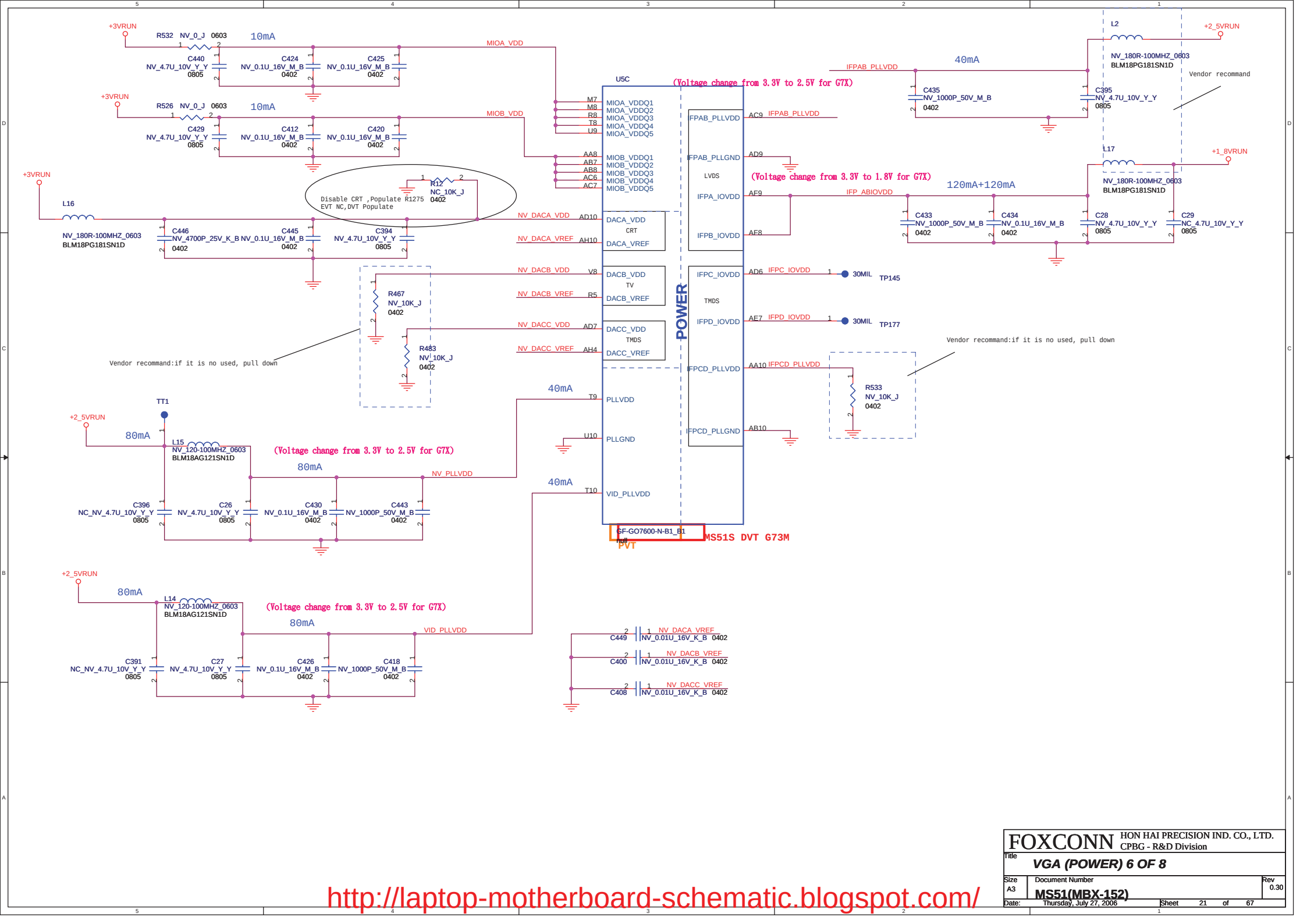

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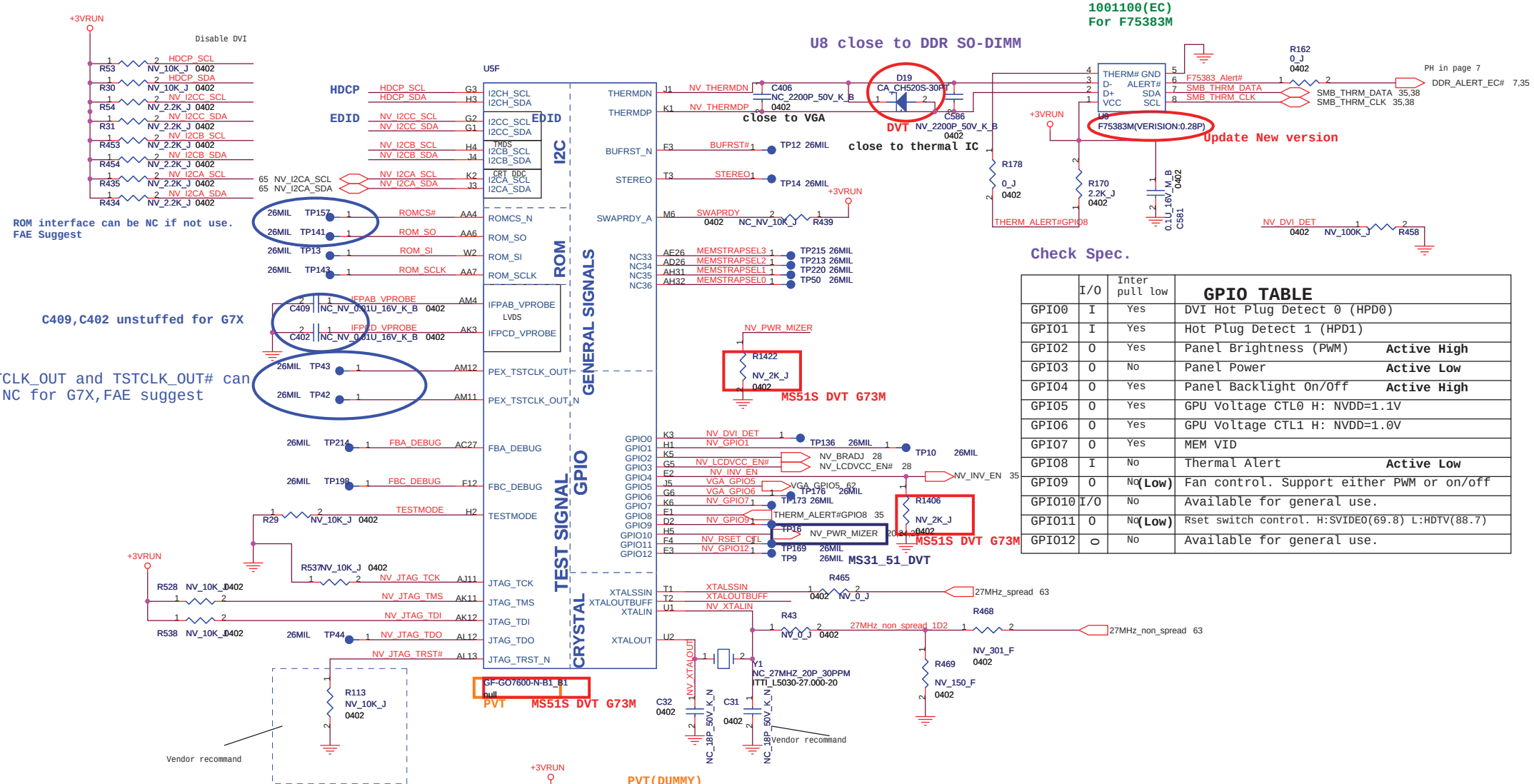
SM bus Address :
1001100(EC)
For F75383M

U8 close to DDR SO-DIMM



GPIO TABLE	I/O	Inter pull low	
GPIO0	I	Yes	DVI Hot Plug Detect 0 (HPD0)
GPIO1	I	Yes	Hot Plug Detect 1 (HPD1)
GPIO2	O	Yes	Panel Brightness (PWM) **Active High**
GPIO3	O	No	Panel Power **Active Low**
GPIO4	O	Yes	Panel Backlight On/Off **Active High**
GPIO5	O	Yes	GPU Voltage CTL0 H: NVDD=1.1V
GPIO6	O	Yes	GPU Voltage CTL1 H: NVDD=1.0V
GPIO7	O	Yes	MEM VID
GPIO8	I	No	Thermal Alert **Active Low**
GPIO9	O	No(Low)	Fan control. Support either PWM or on/off
GPIO10	I/O	No	Available for general use.
GPIO11	O	No(Low)	Rset switch control. H:SVIDEO(69.8) L:HDTV(88.7)
GPIO12	O	No	Available for general use.

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Title: VGA (POWER) 7 OF 8

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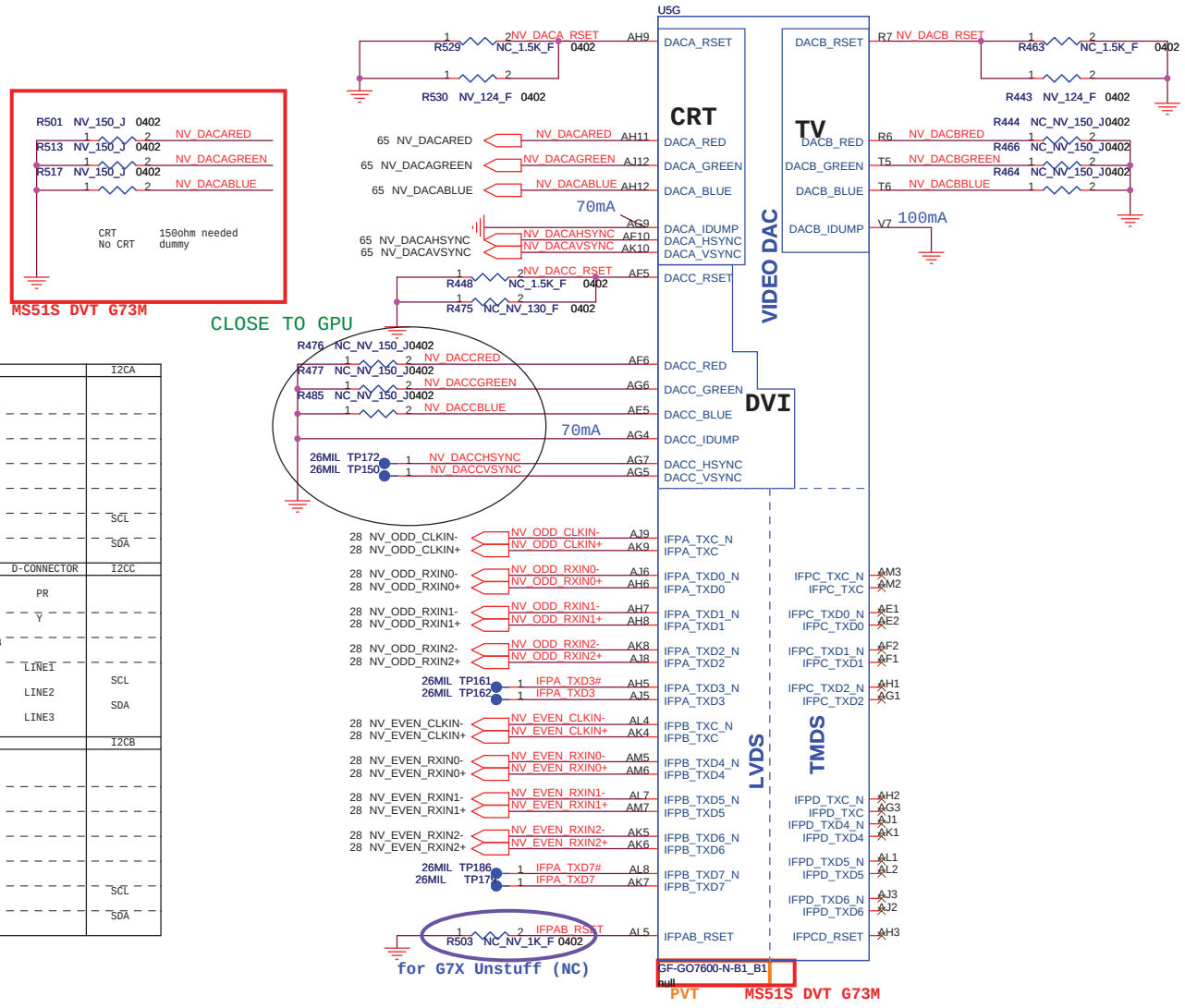

DACA	VGA-CRT			I2CA
DACA-RED	R			
DACA-GREEN	G			
DACA-BLUE	B			
DACA-HSYNC	HSYNC			
DACA-VSYNC	VSYNC			
	VGA-DDCCLK			SCL
	VGA-DDCDATA			SDA
DACB	**S-VIDEO**	**COMPOSITE**	**D-CONNECTOR**	**I2CC**
DACB-RED	C		PR	
DACB-GREEN	Y		Y	
DACB-BLUE		COMPOSITE		
			LINE1	SCL
			LINE2	SDA
			LINE3	
DACC	**DVI-I**			**I2CB**
DACC-RED	R			
DACC-GREEN	G			
DACC-BLUE	B			
DACC-HSYNC	HSYNC			
DACC-VSYNC	VSYNC			
	DVI-DDCCLK			SCL
	DVI-DDCDATA			SDA

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Title: VGA (POWER) 8 OF 8

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Address / Command on Die termination is set to 120 ohm.

U30

U31

DLL POWER --- Add decoupling C and L ?

Minimum 200us delay required prior to applying any executable command after stable power and clock.

MS51S DVT G73M

For 16Mx32 Bit stuff
8Mx32 Bit no stuff

For 8Mx32 Bit Stuff
16Mx32 Bit no stuff

VRAM_VREF is 70%FBVDDQ for GDDR3

VRAM_VREF is 70%FBVDDQ for GDDR3 1.26V

MS31_51_DVT

FAE suggestion on 8/16==>120 ohm
For garbage display ===>80.6 ohm
Demo circuit ===>40.2 ohm
FAE suggestion in DVT ===>240 ohm

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Title: VRAM (GDDR3) 1 OF 4

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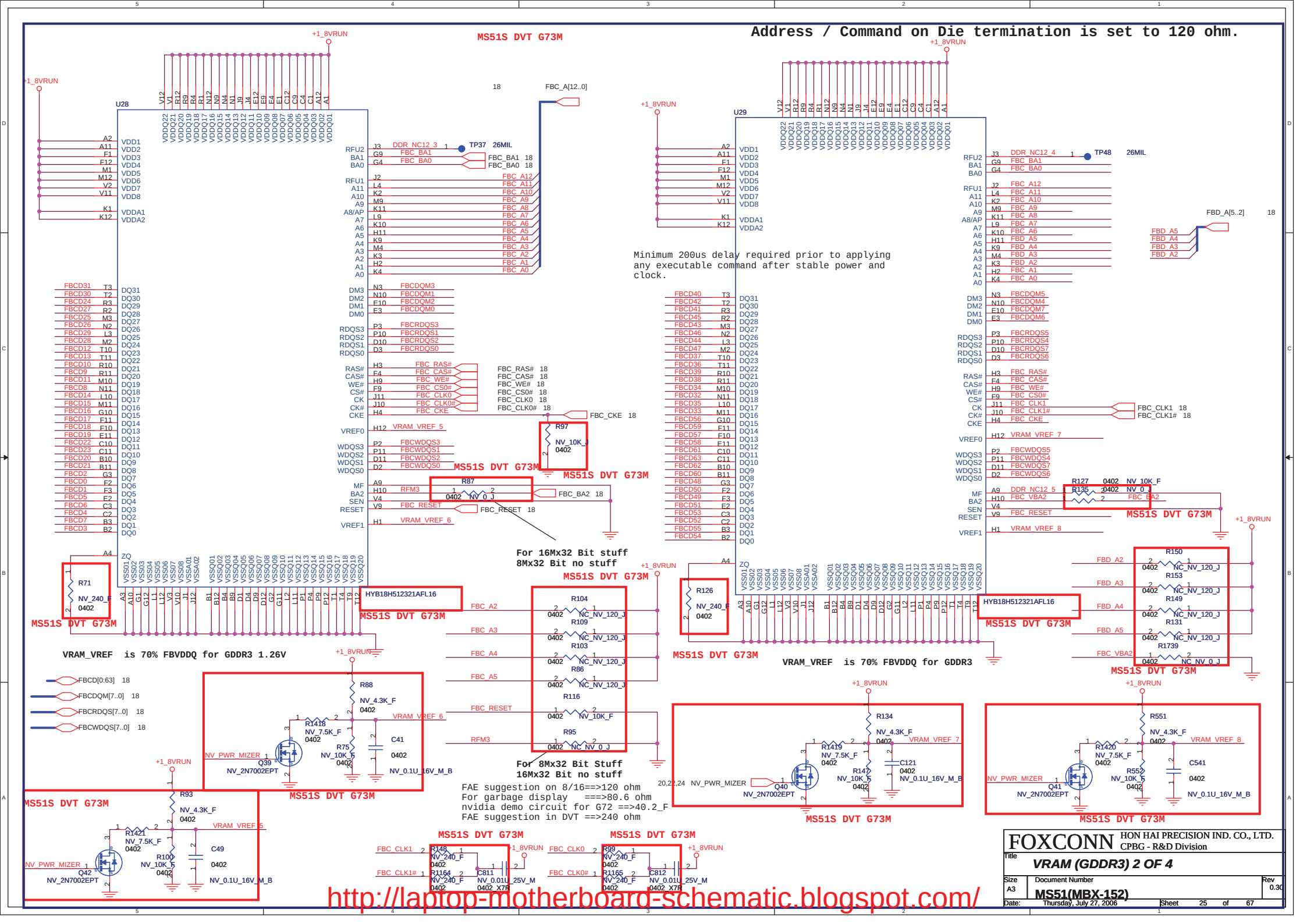
Address / Command on Die termination is set to 120 ohm.
MS51S DVT G73M
U28
U29
+1_8VRUN
HYB18H512321AFL16
Minimum 200us delay required prior to applying any executable command after stable power and clock.
For 16Mx32 Bit stuff
8Mx32 Bit no stuff
For 8Mx32 Bit Stuff
16Mx32 Bit no stuff
VRAM_VREF is 70% FBVDDQ for GDDR3 1.26V
VRAM_VREF is 70% FBVDDQ for GDDR3
FAE suggestion on 8/16==>120 ohm
For garbage display ===>80.6 ohm
nvidia demo circuit for G72 ==>40.2_F
FAE suggestion in DVT ==>240 ohm
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HON HAI PRECISION IND. CO., LTD.
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VRAM (GDDR3) 2 OF 4
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Title: *VRAM (GDDR) 3 OF 4*

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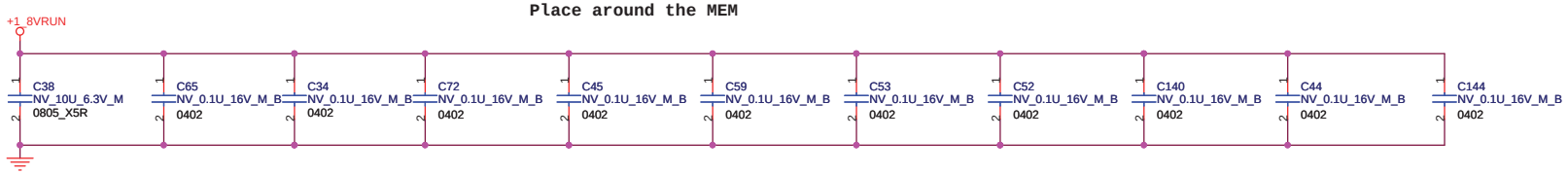
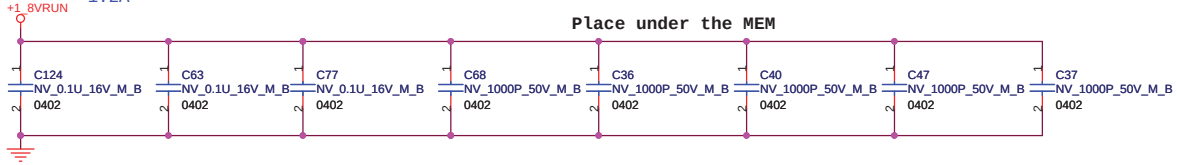
Decoupling for right MEMORY

Place around the MEM



1.2A

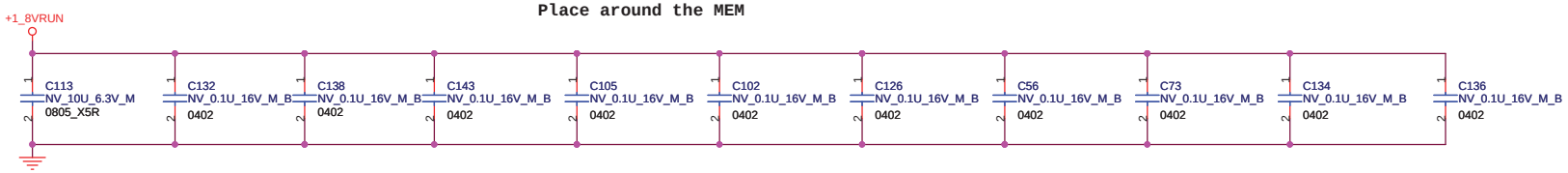
Place under the MEM



NO USE

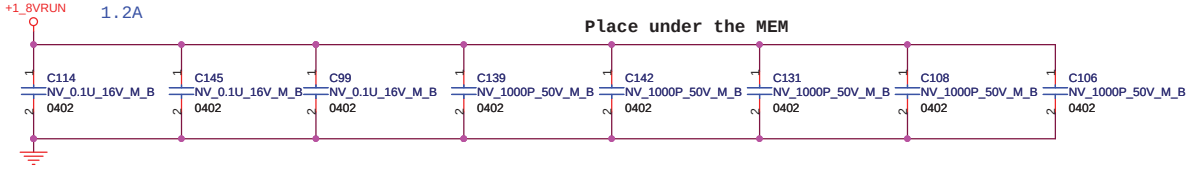
Decoupling for right MEMORY

Place around the MEM



1.2A

Place under the MEM



MS51S DVT G73M

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	VRAM (POWERBYPASS) 4 OF 4	
Size A3	Document Number MS51(MBX-152)	Rev 0.30
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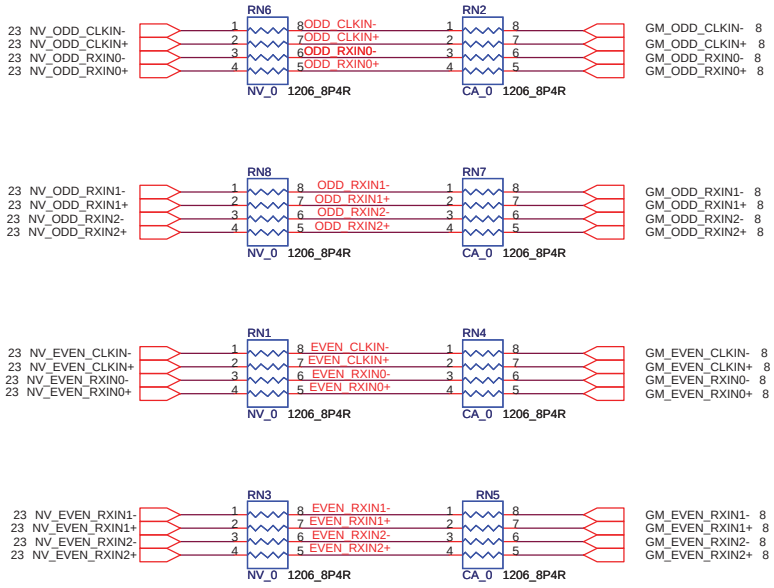
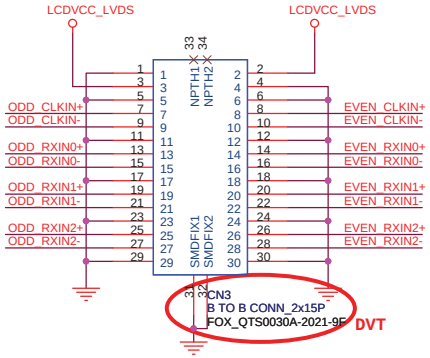
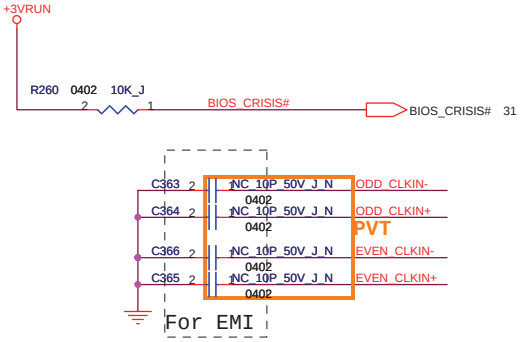
http://laptop-motherboard-schematic.blogspot.com/

LVDS

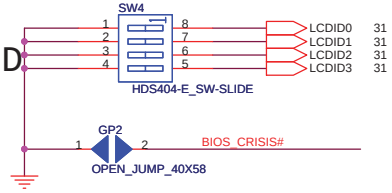




LVDS CONNECTOR

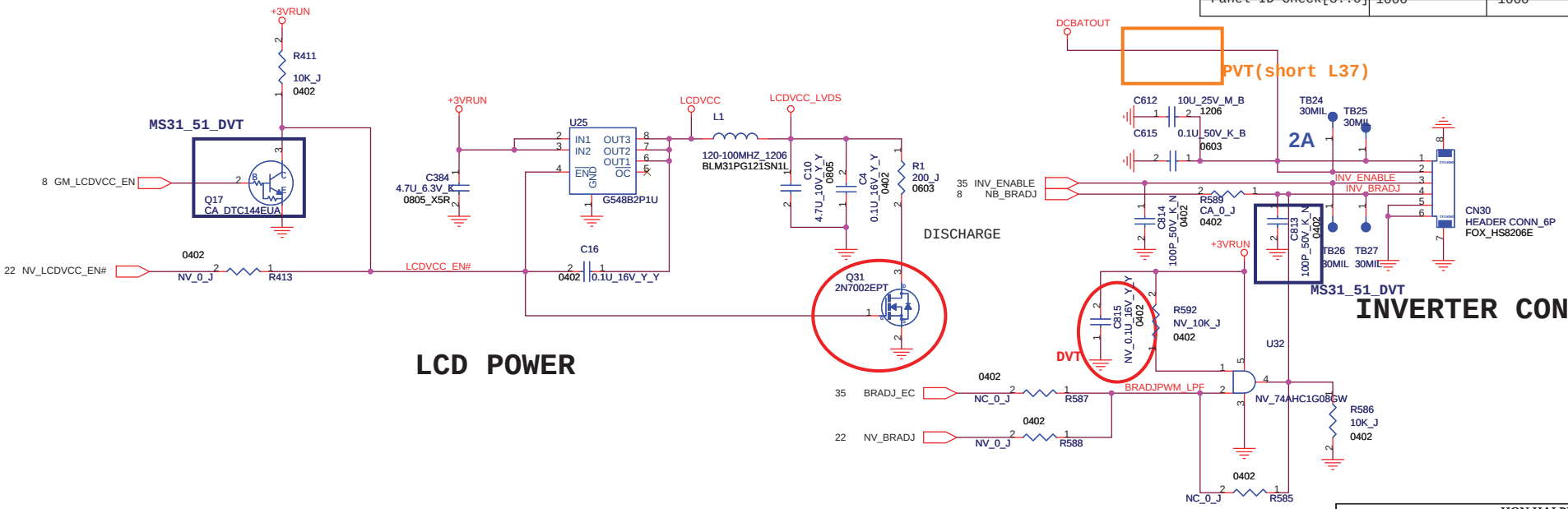


PANEL ID



ON=0

Type	WXGA	WXGA-HC	WSXGA+
Size	15.4" wide	15.4" wide	15.4" wide
Vender	Hitach	Hitachi	Hitachi
Device Name	TX39D81VC1AAA	TX39D80VC1GAA	TX39D90VC1GAA
Panel ID Check[3..0]	1000	1000	1100



LCD POWER

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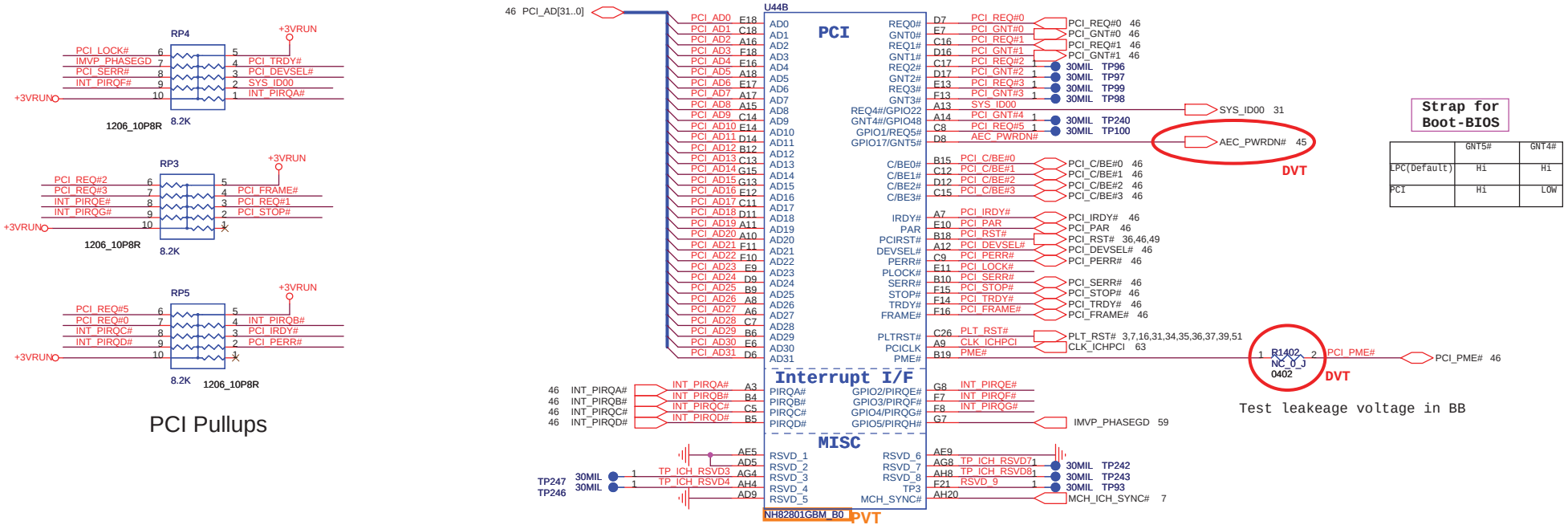
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: LVDS

Size: A3 | Document Number: MS51(MBX-152) | Rev: 0.30

Date: Thursday, July 27, 2006 | Sheet 28 of 67



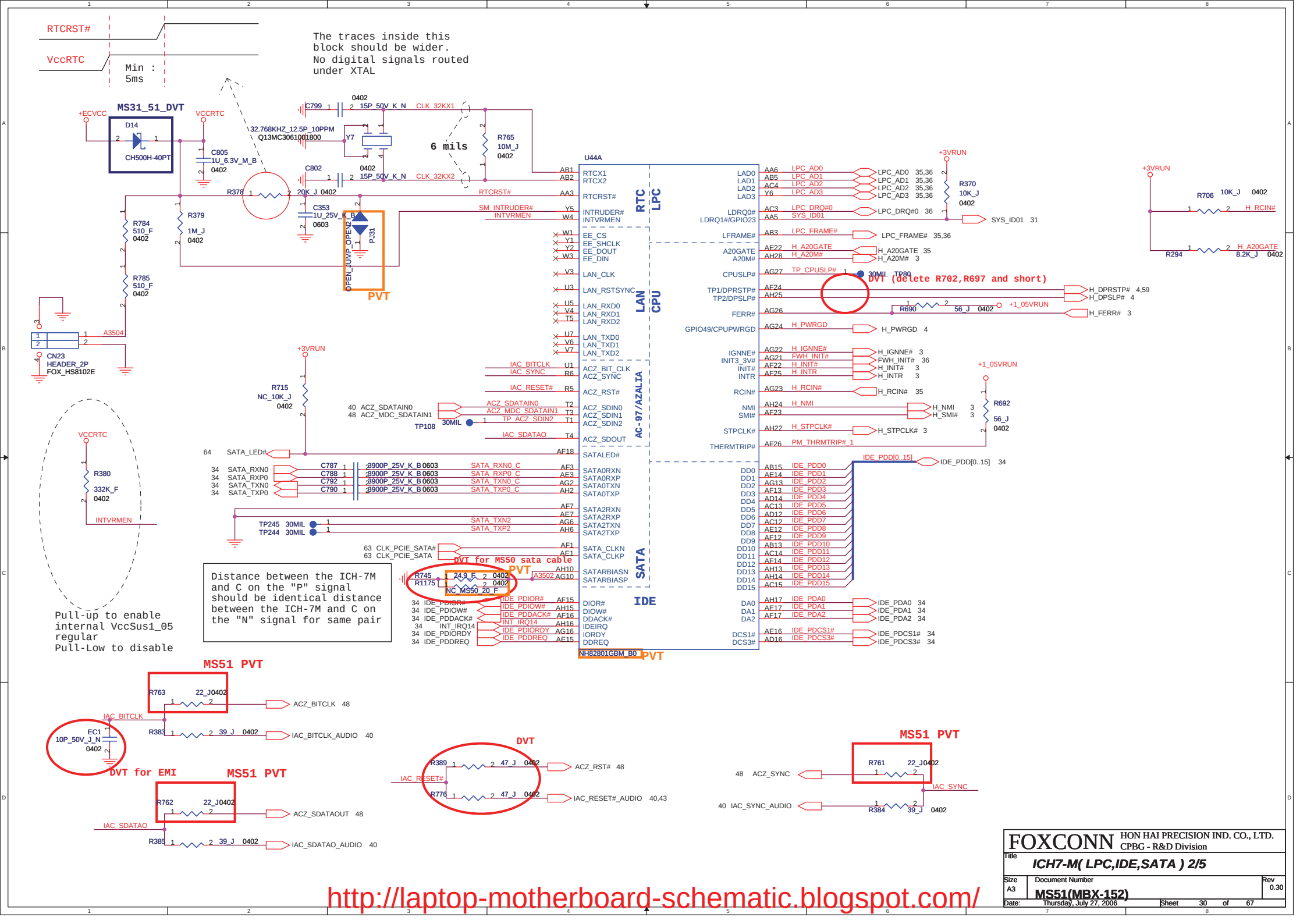
http://laptop-motherboard-schematic.blogspot.com/

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

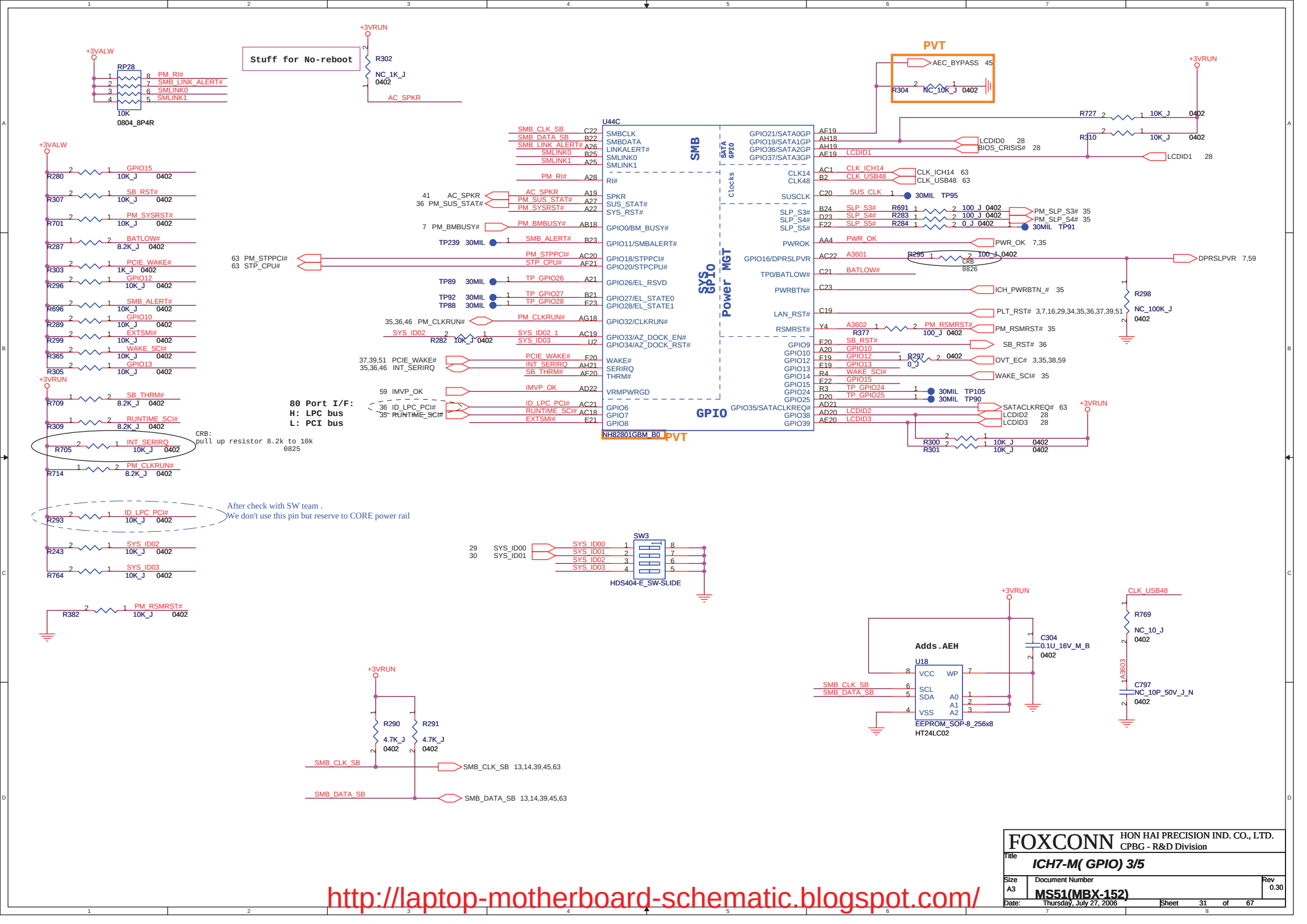
Title: ICH7-M(PCI/DMI/USB/PCIE) 1/5

Size: A3 | Document Number: MS51(MBX-152) | Rev: 0.30

Date: Thursday, July 27, 2006 | Sheet 29 of 67

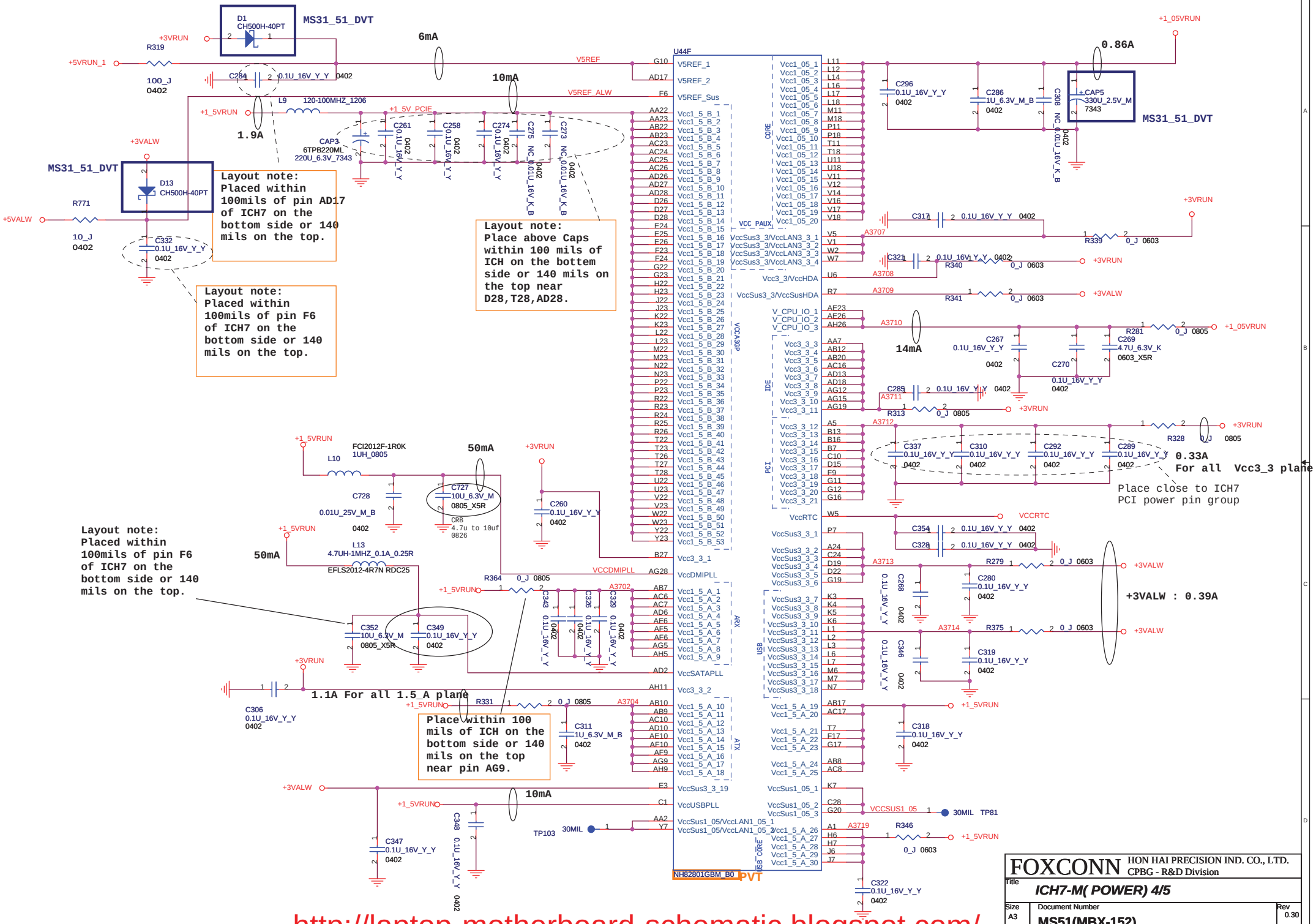


http://laptop-motherboard-schematic.blogspot.com/

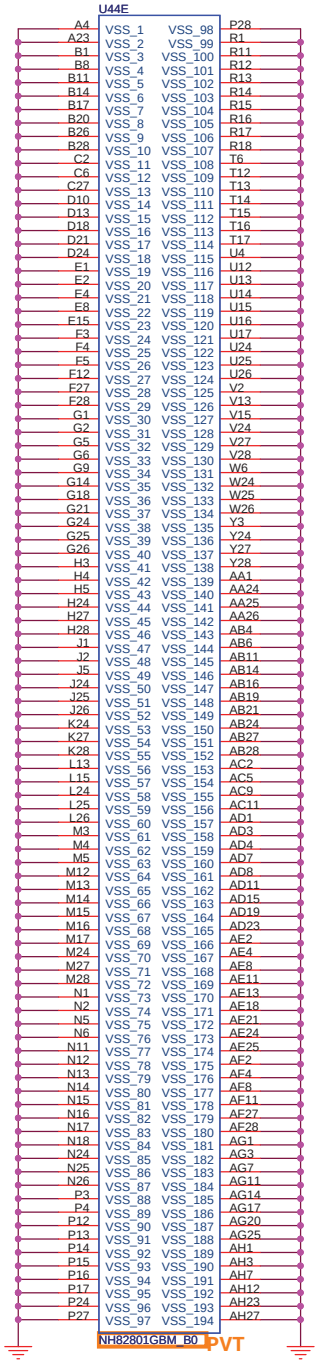


http://laptop-motherboard-schematic.blogspot.com/

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	ICH7-M(GPIO) 3/5
Size	A3
Document Number	MS51(MBX-152)
Rev	0.30
Date:	Thursday, July 27, 2006
Sheet	31 of 67



http://laptop-motherboard-schematic.blogspot.com/



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	*ICH7-M(GND) 5/5*	
Size A3	Document Number **MS51(MBX-152)**	Rev 0.30
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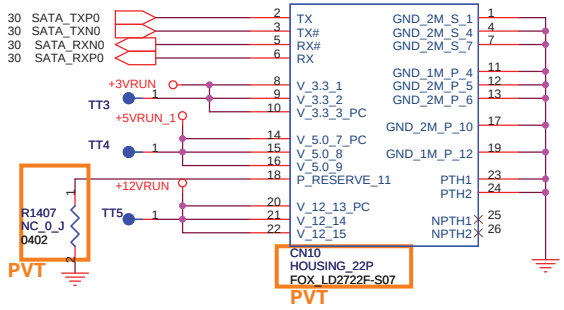
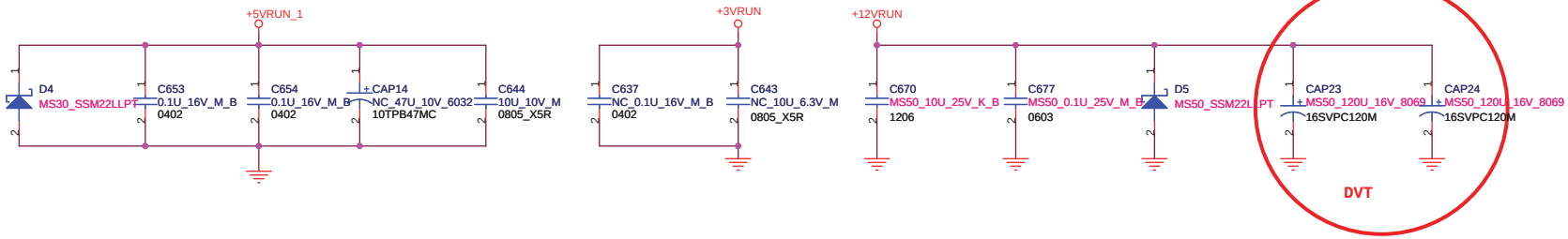
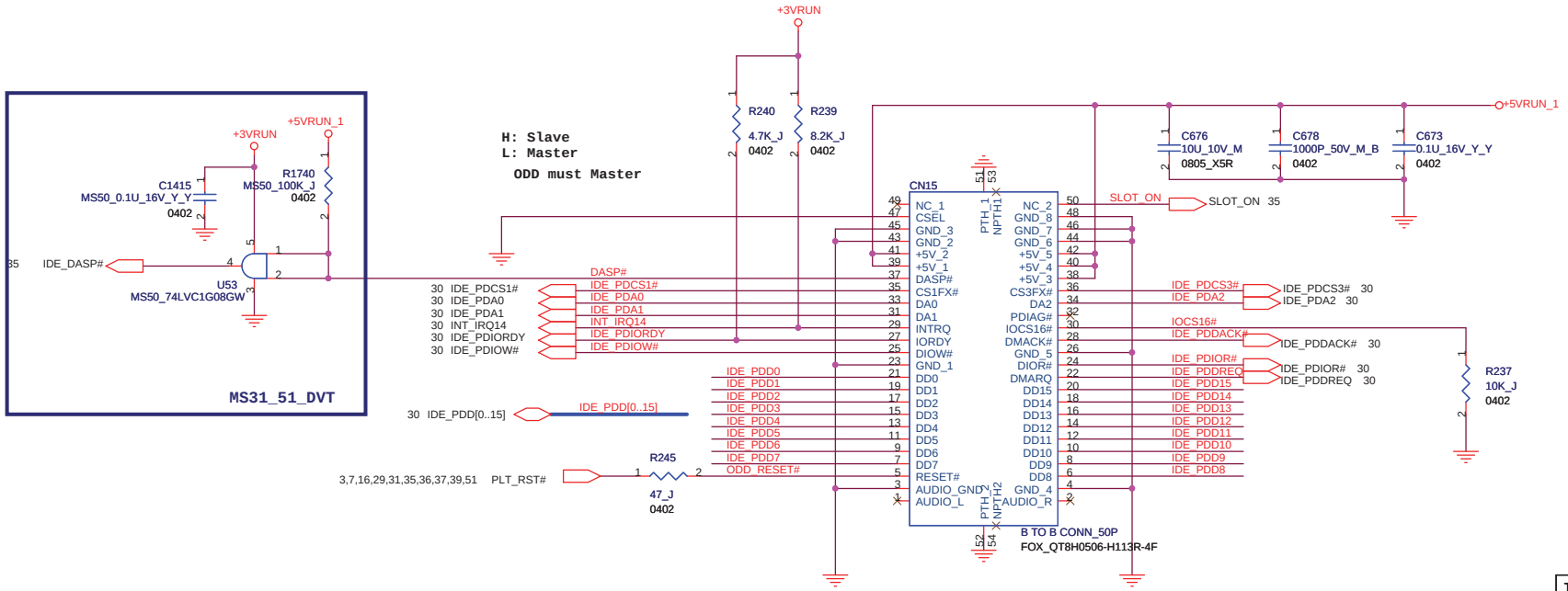
SATA HDD CONN



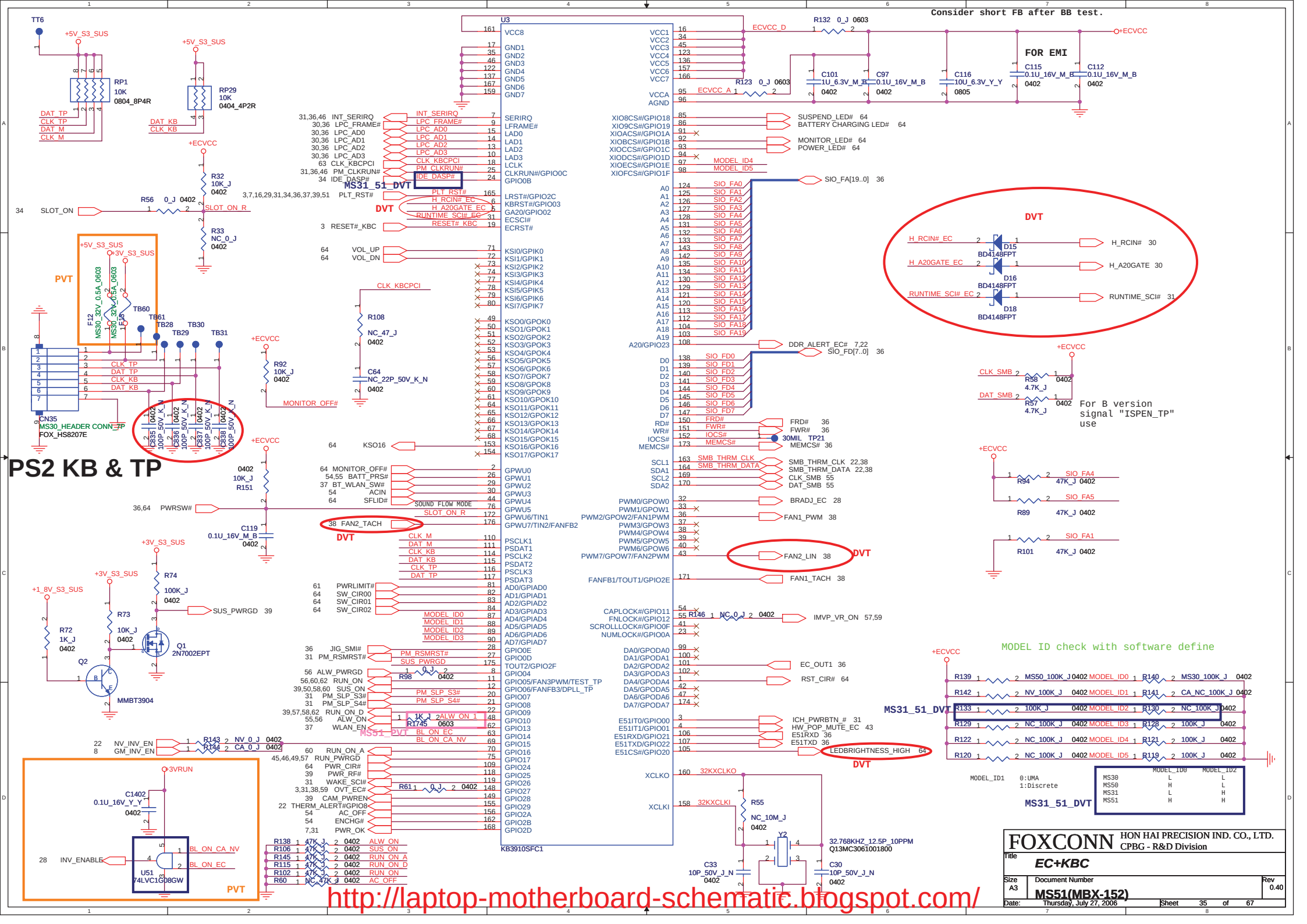




CD-ROM CONN

http://laptop-motherboard-schematic.blogspot.com/

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	SATA HDD/CD-ROM	
Size A3	Document Number MS51(MBX-152)	Rev 0.30
Date: Thursday, July 27, 2006	Sheet 34 of 67	


Consider short FB after BB test.
PS2 KB & TP
U3
KB3910SFC1
FOR EMI
DVT
PVT
MS31_51_DVT
MODEL ID check with software define
For B version signal "ISPEN_TP" use
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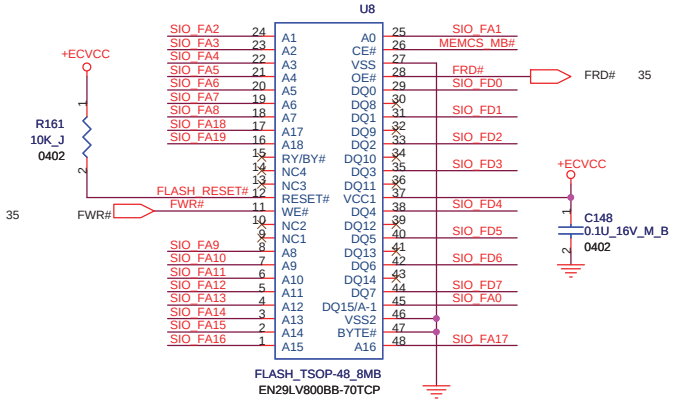
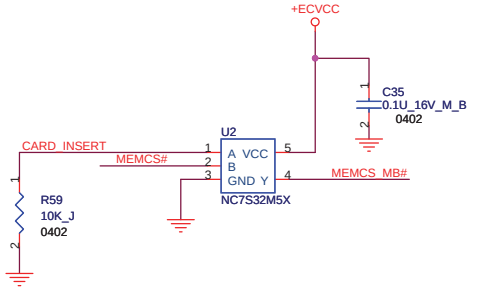
EC+KBC
MS51(MBX-152)
Thursday, July 27, 2006
http://laptop-motherboard-schematic.blogspot.com/

35 SIO_FA[19..0]

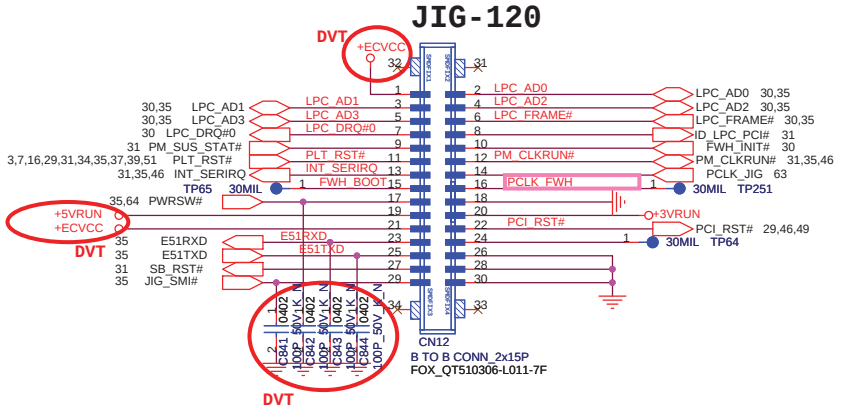
35 SIO_FD[7..0]

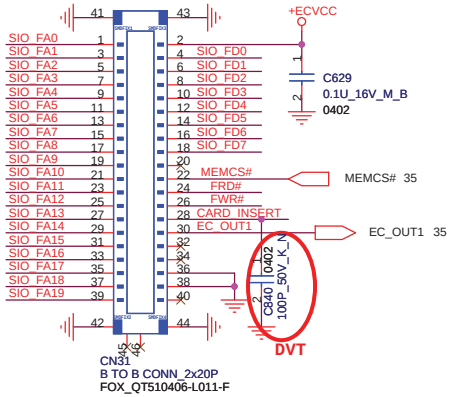


BIOS ROM



JIG-120





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Title: *Flash ROM/X-Bus CONN*

Size: A3 | Document Number: MS51(MBX-152) | Rev: 0.40

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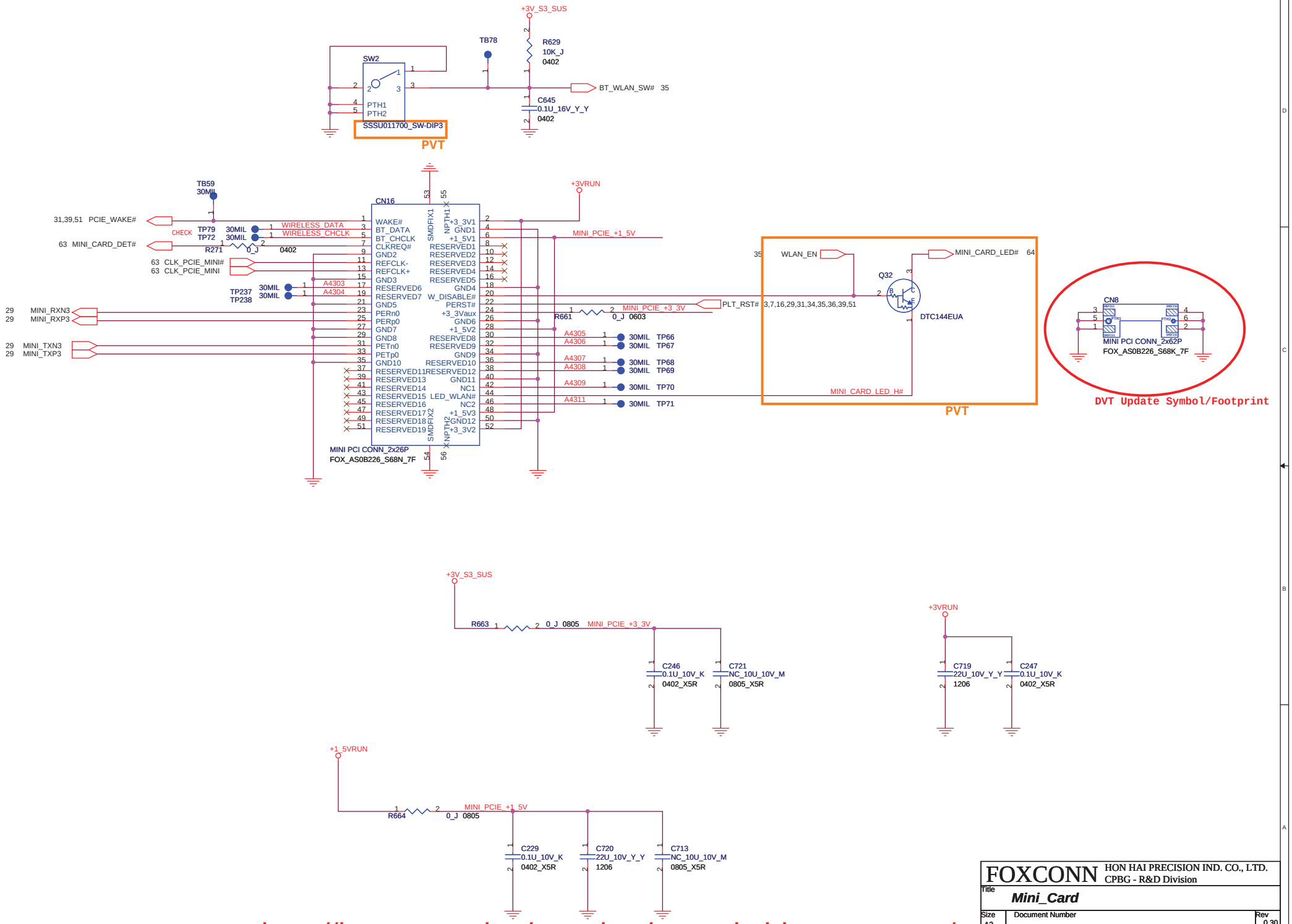

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FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	*Mini_Card*
Size	A3
Document Number	MS51(MBX-152)
Rev	0.30
Date:	Thursday, July 27, 2006
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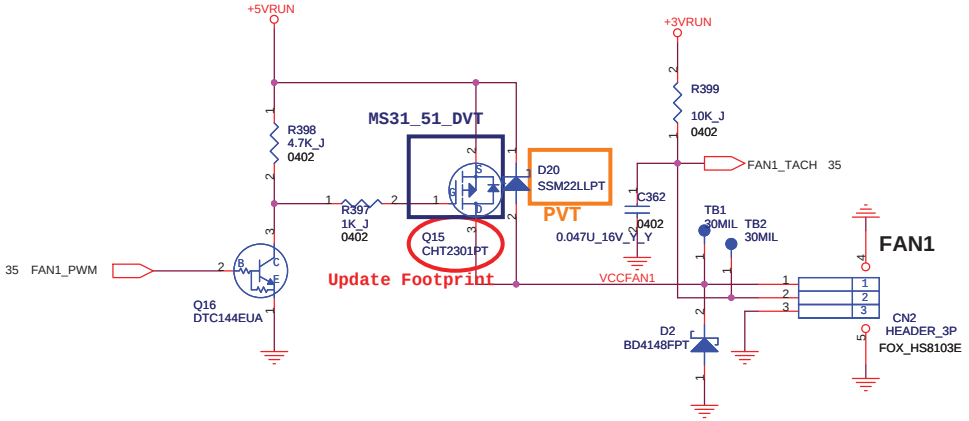
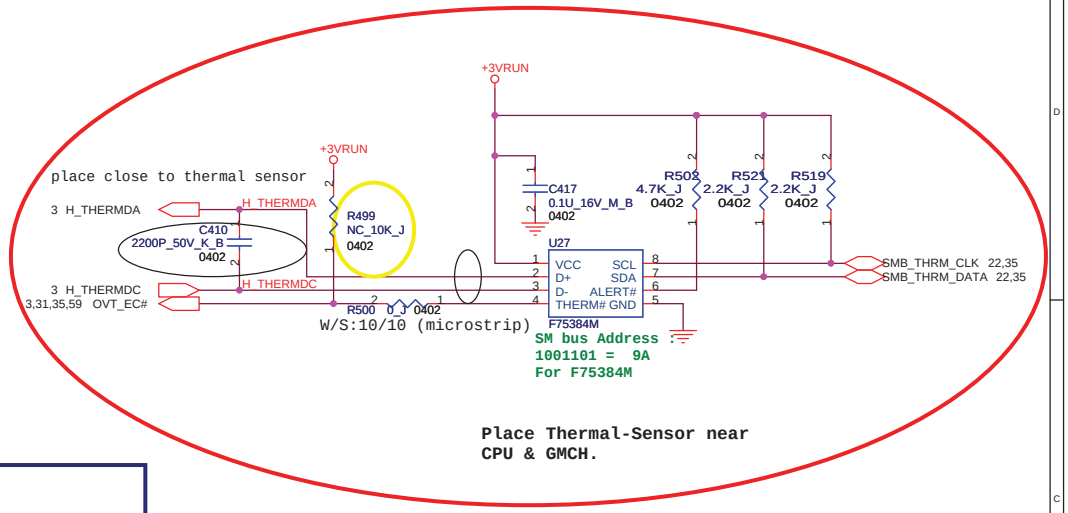
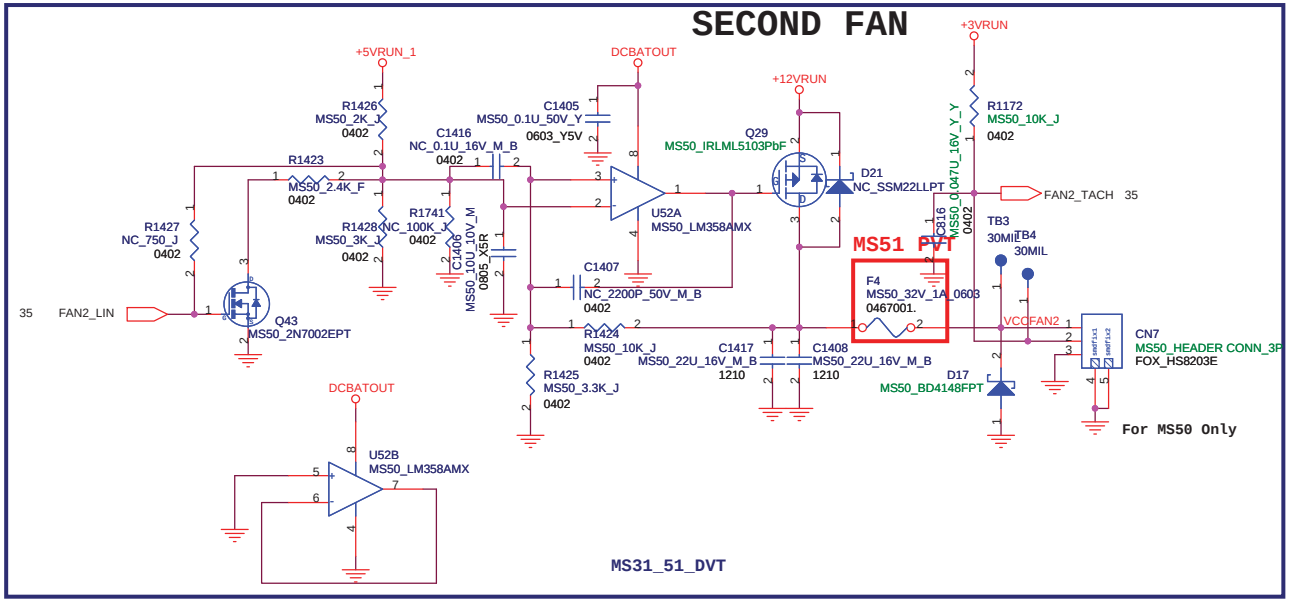
FAN



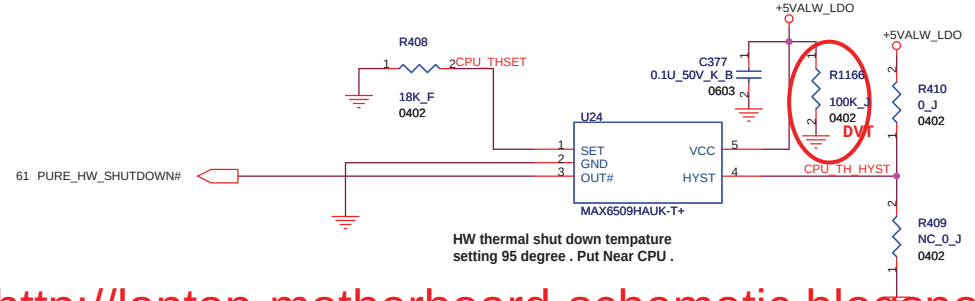
CPU SENSOR



SECOND FAN



HW THERMAL PROTECTION



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FOXCONN HON HAI PRECISION IND. CO., LTD.
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Title: FAN/HW THERMAL PROTECT

Size	Document Number	Rev
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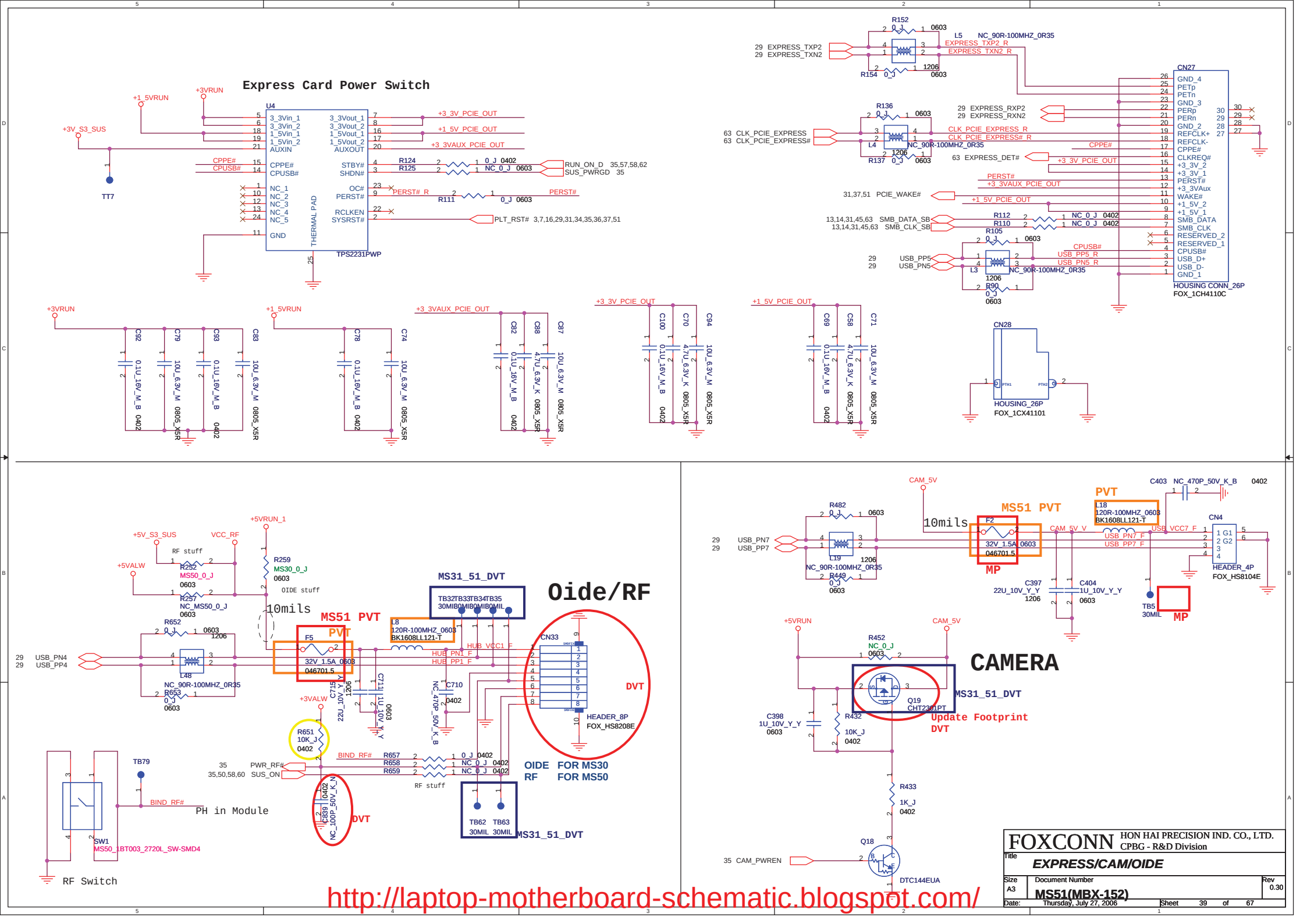
Express Card Power Switch
U4
TPS2231PWP
THERMAL PAD
+1_5VRUN
+3VRUN
+3V_S3_SUS
+3_3V_PCIE_OUT
+1_5V_PCIE_OUT
+3_3VAUX_PCIE_OUT
CPPE#
CPUSB#
PERST#
PERST# R
RUN_ON_D 35,57,58,62
SUS_PWRGD 35
PLT_RST# 3,7,16,29,31,34,35,36,37,51
TT7
CN27
HOUSING CONN_26P
FOX_1CH4110C
CN28
HOUSING_26P
FOX_1CX41101
EXPRESS_TXP2
EXPRESS_TXN2
EXPRESS_RXP2
EXPRESS_RXN2
CLK_PCIE_EXPRESS
CLK_PCIE_EXPRESS#
EXPRESS_DET#
PCIE_WAKE#
SMB_DATA_SB
SMB_CLK_SB
USB_PP5
USB_PN5
Oide/RF
MS31_51_DVT
MS51 PVT
PVT
DVT
MP
10mils
HEADER_8P
FOX_HS8208E
OIDE RF
FOR MS30
FOR MS50
PH in Module
RF Switch
SW1
MS50_1BT003_2720L_SW-SMD4
CAMERA
Update Footprint
Q19
CHT2301PT
Q18
DTC144EUA
CAM_PWREN
CAM_5V
HEADER_4P
FOX_HS8104E
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
EXPRESS/CAM/OIDE
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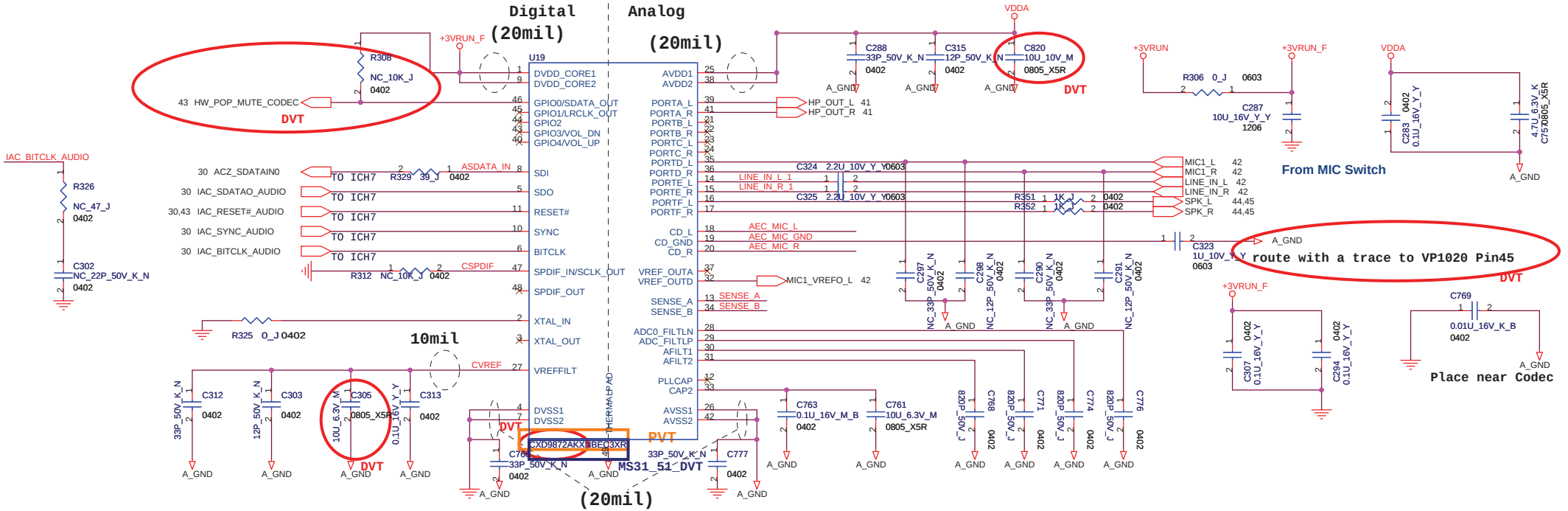
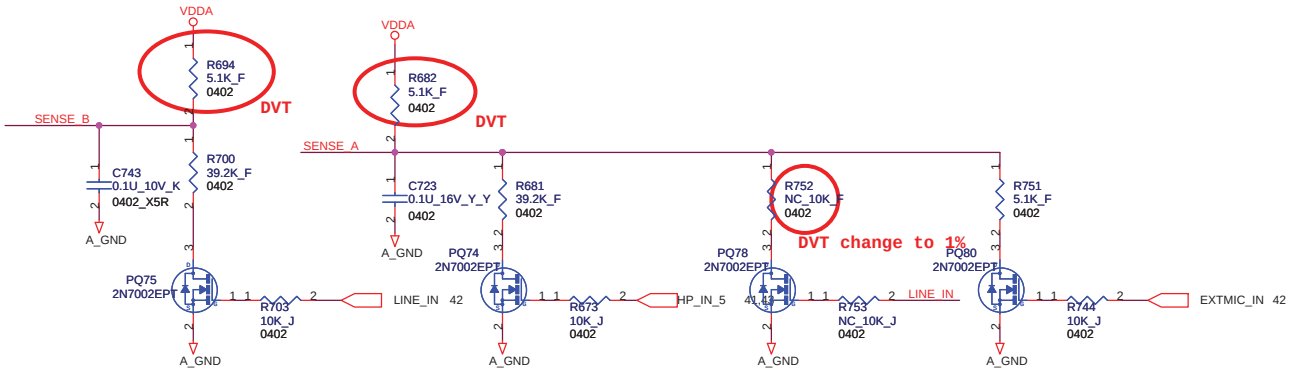
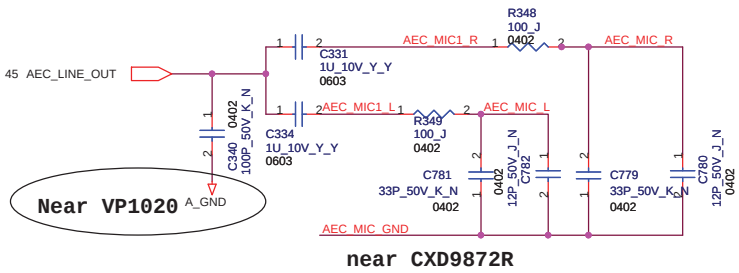
http://laptop-motherboard-schematic.blogspot.com/

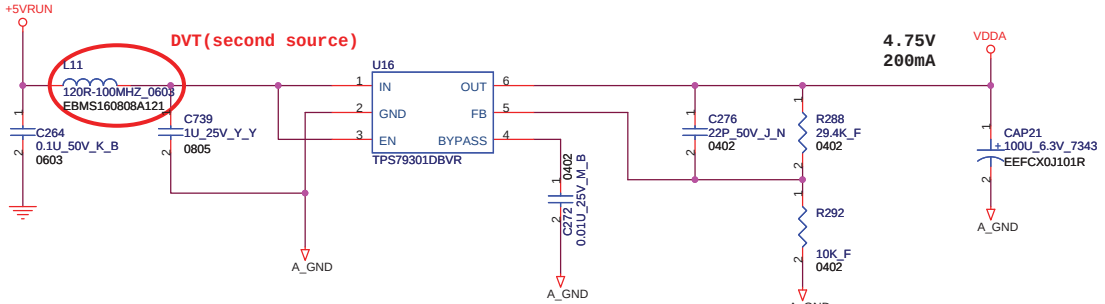


R692,C723 put near SENSE_A(pin13)
R694,C743 put near SENSE_B(pin34)





Int MIC amp circuit



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	AUDIO(CODEC & POWER)	
Size A3	Document Number MS51(MBX-152)	Rev 0.30
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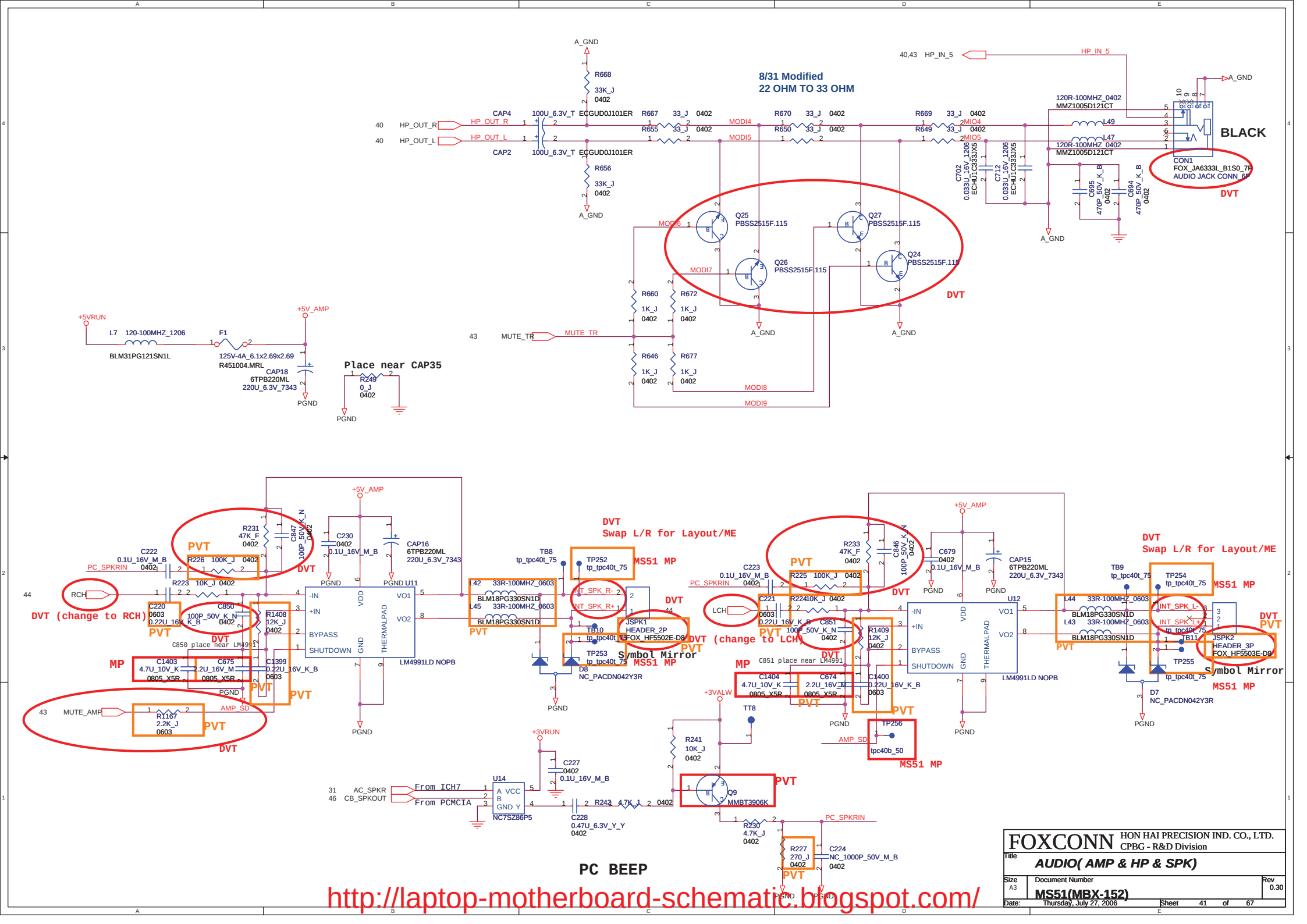
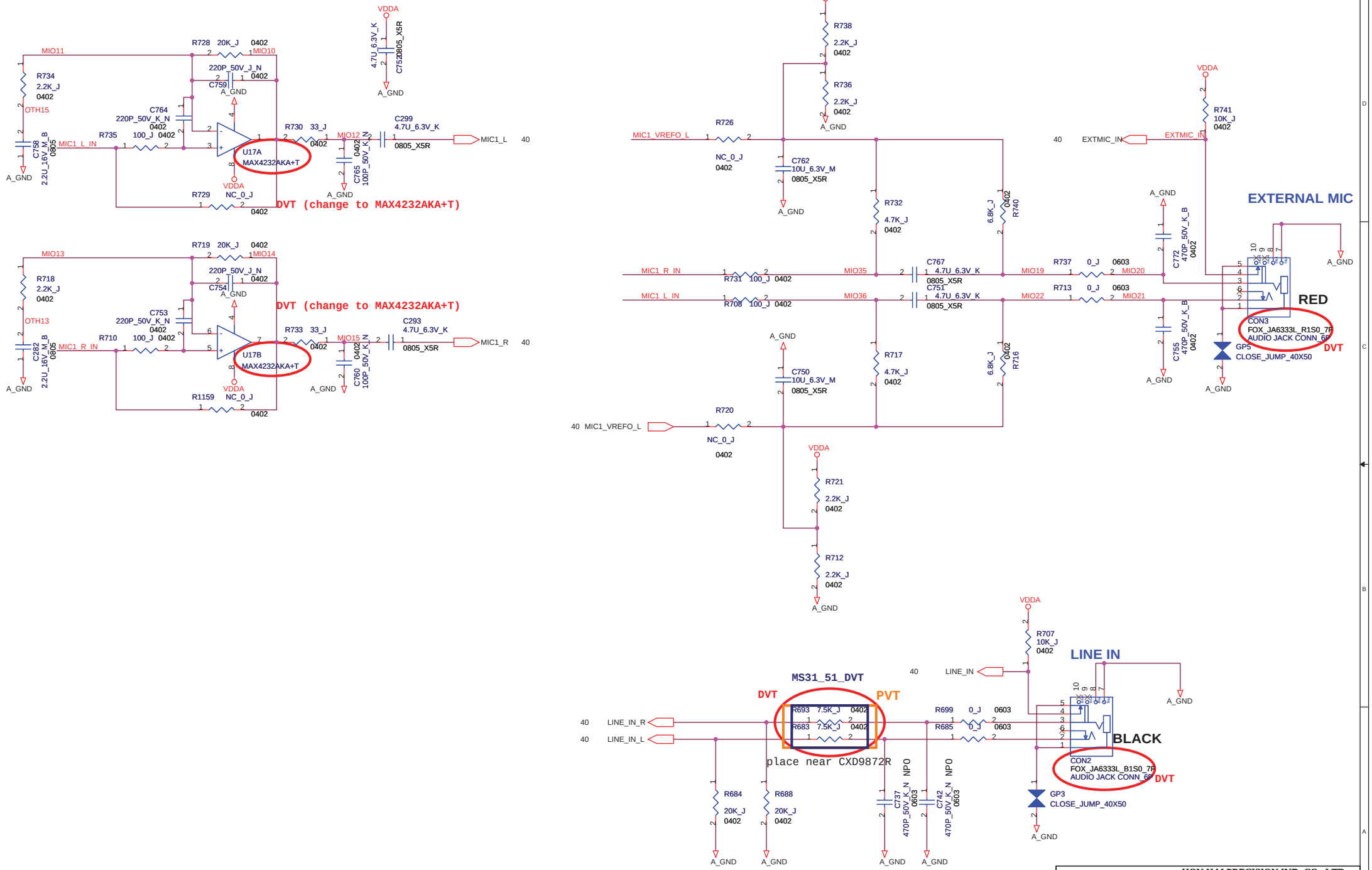


http://laptop-motherboard-schematic.blogspot.com/



FOXCONN HON HAI PRECISION IND. CO., LTD.
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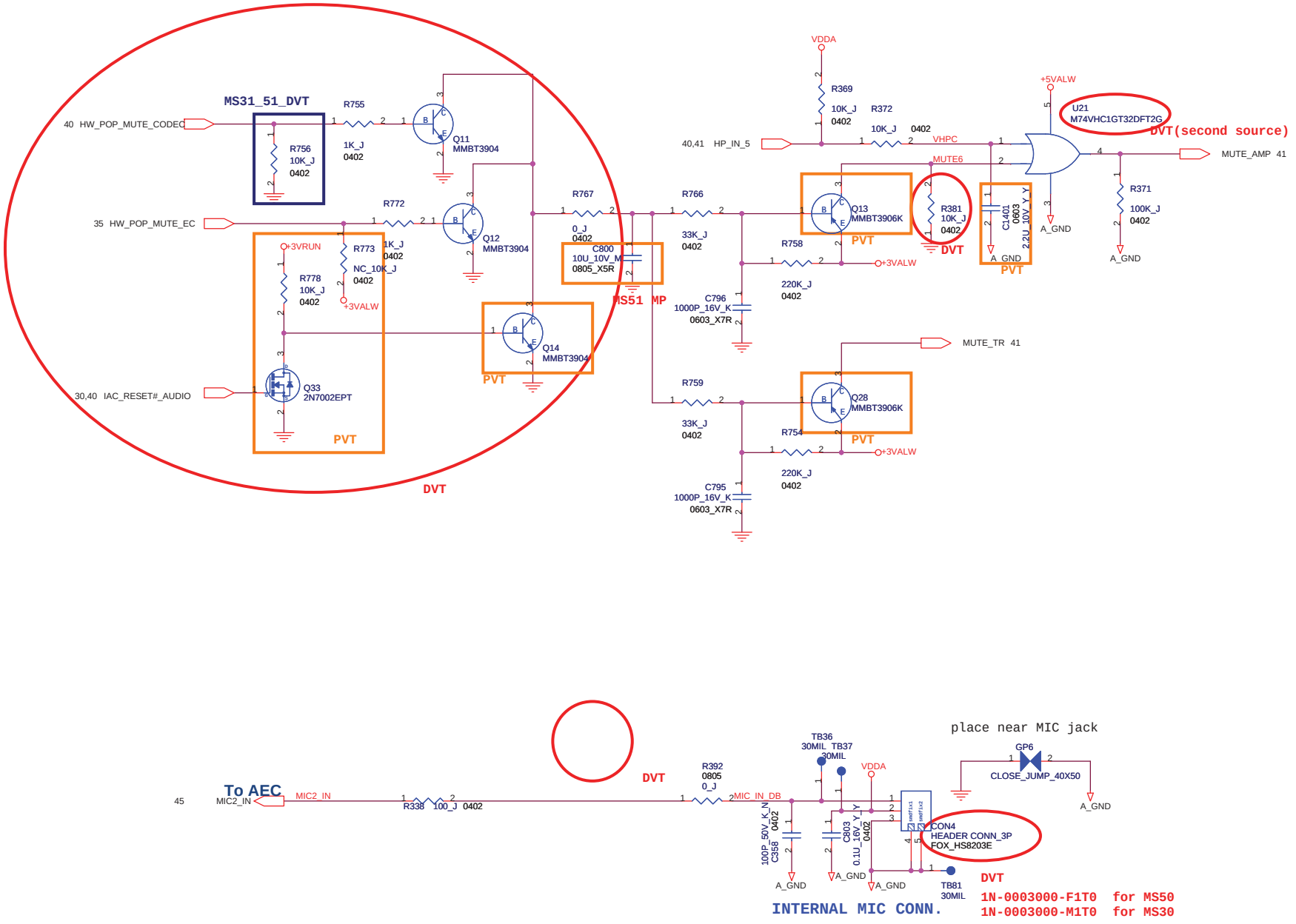
Title: *AUDIO(EXT MIC & PHONE OUT)*

Size	Document Number	Rev
A3	MS51(MBX-152)	0.30

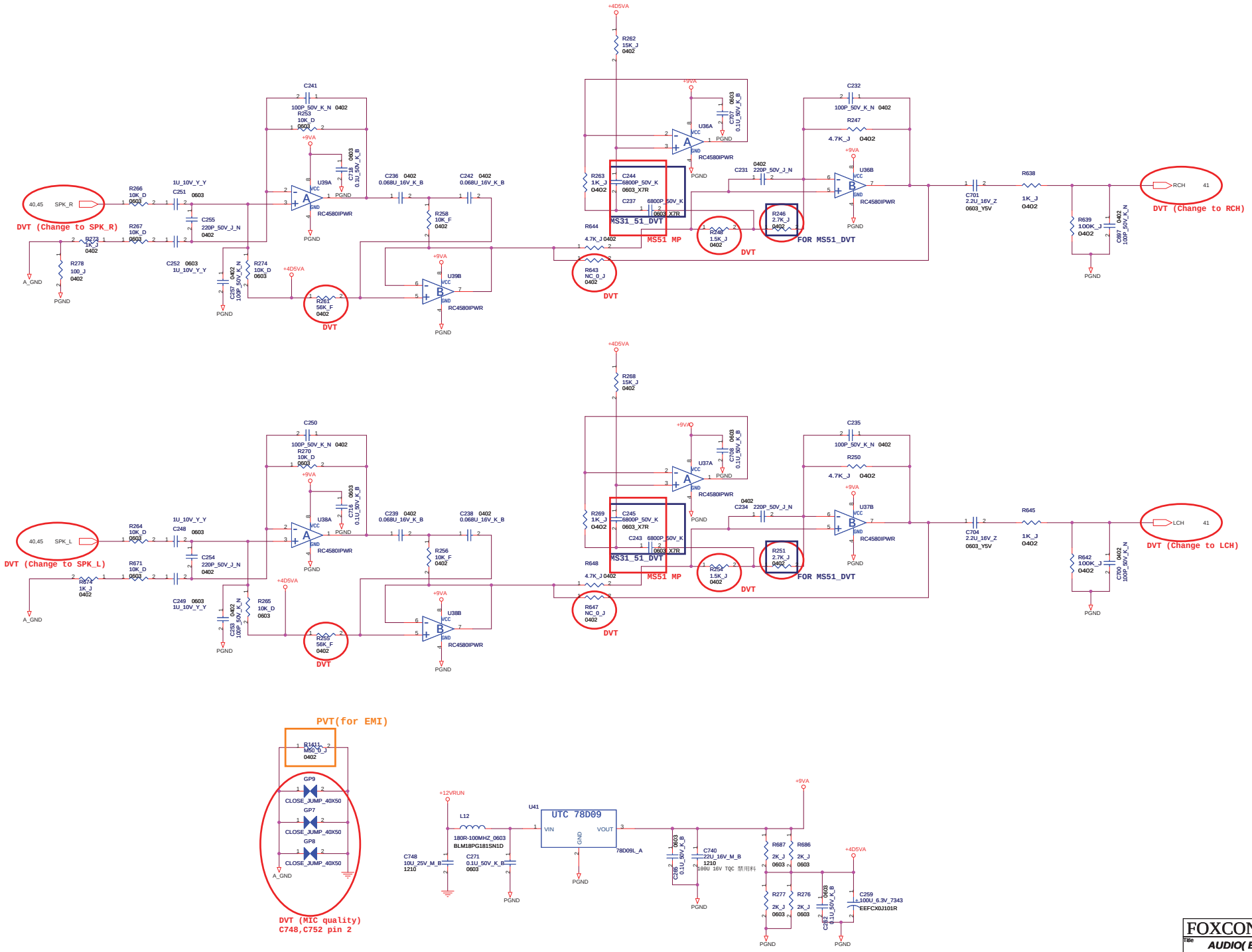
Date: Thursday, July 27, 2006 Sheet 42 of 67

http://laptop-motherboard-schematic.blogspot.com/



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	AUDIO (MUTE & INTMIC)	
Size A3	Document Number MS51(MBX-152)	Rev 0.30
Date: Thursday, July 27, 2006	Sheet 43 of 67	

http://laptop-motherboard-schematic.blogspot.com/



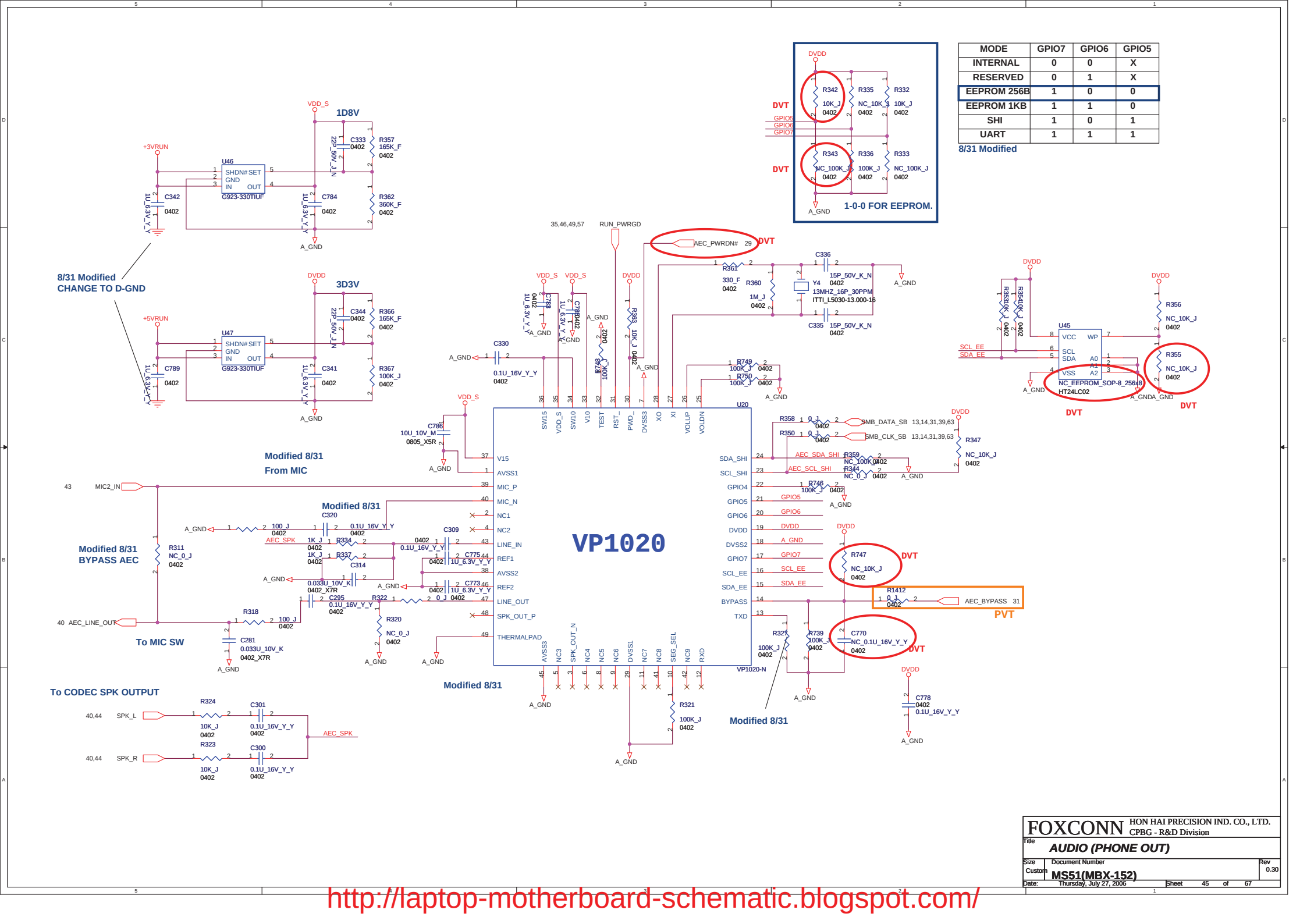
http://laptop-motherboard-schematic.blogspot.com/

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: AUDIO(EQ)

Size: A2 | Document Number: MS51(MBX-152) | Rev: 0.30

Date: Thursday, July 27, 2006 | Sheet 44 of 67



MODE	GPIO7	GPIO6	GPIO5
INTERNAL	0	0	X
RESERVED	0	1	X
EEPROM 256B	1	0	0
EEPROM 1KB	1	1	0
SHI	1	0	1
UART	1	1	1

8/31 Modified

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	AUDIO (PHONE OUT)
Size: Custom	Document Number: MS51(MBX-152)
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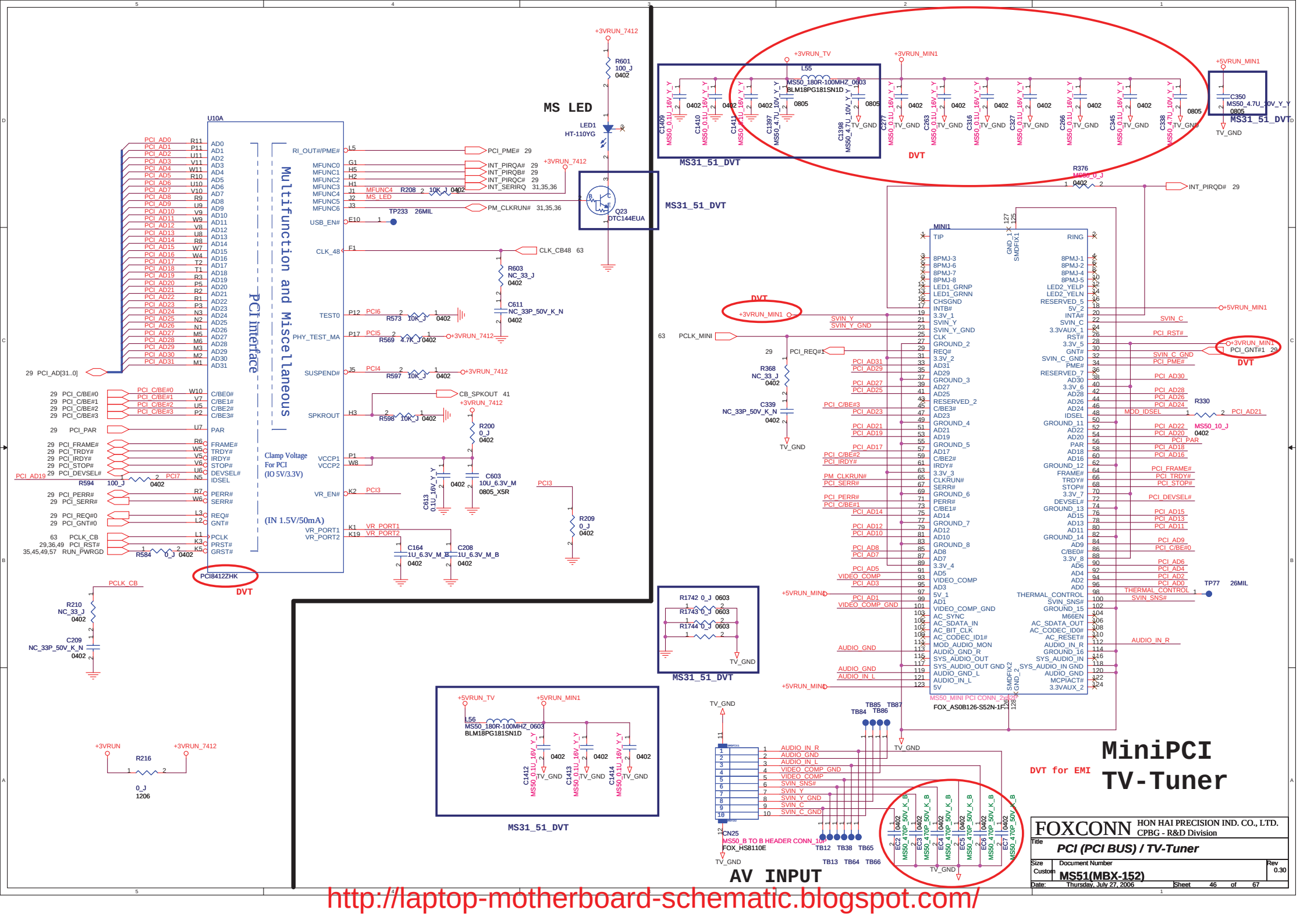
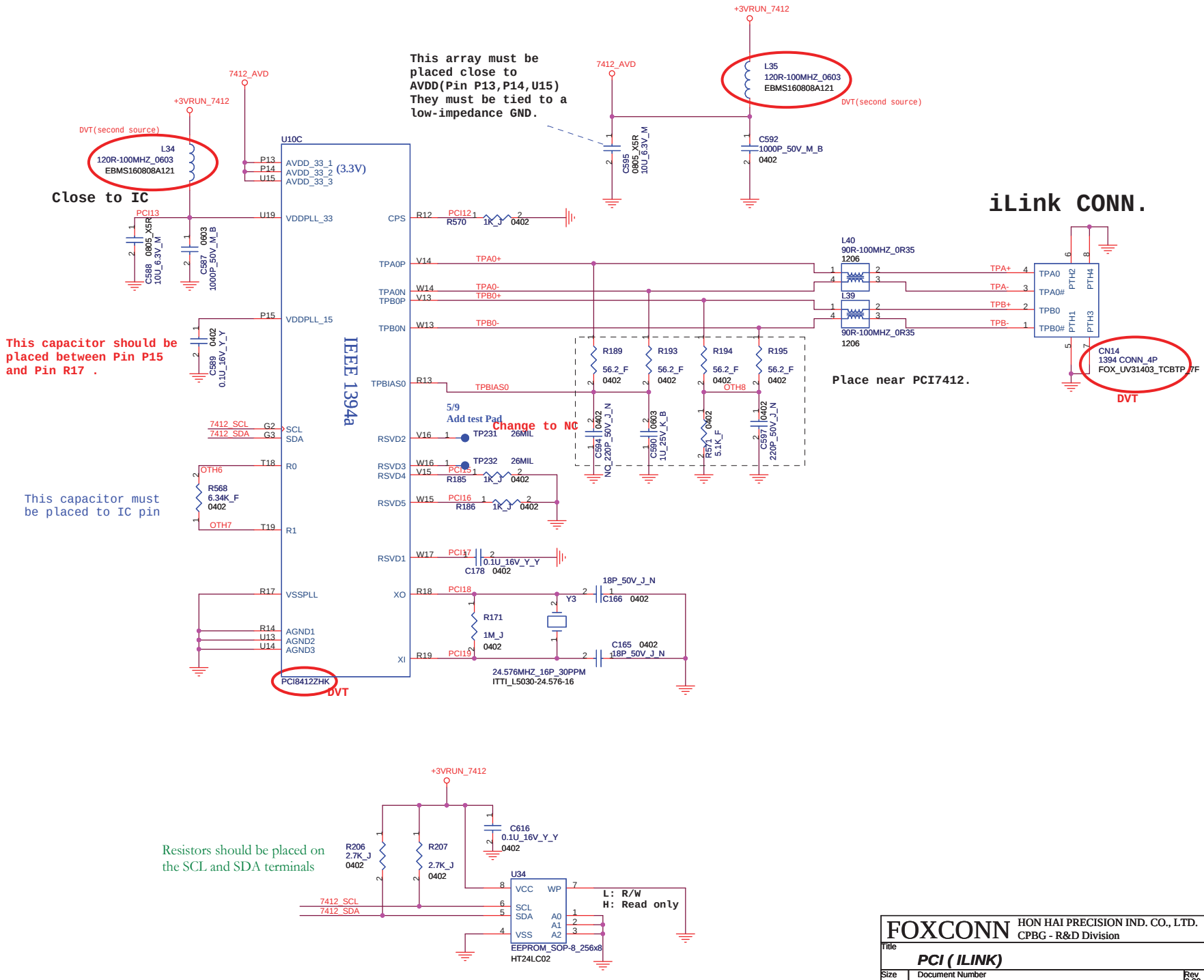
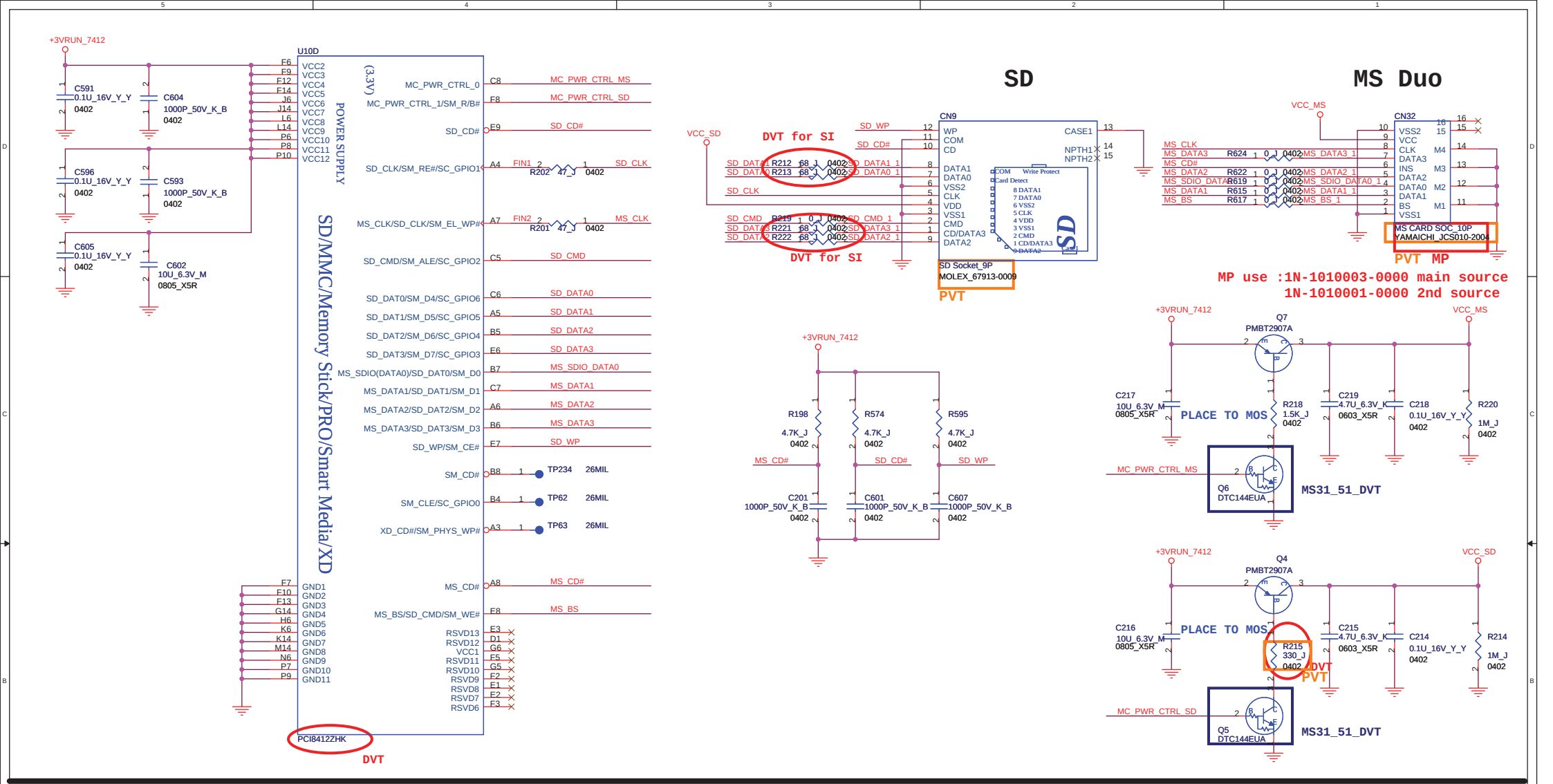
Date: Thursday, July 27, 2006	Sheet 45 of 67

http://laptop-motherboard-schematic.blogspot.com/


MS LED
U10A
PCI interface
Multifunction and Miscellaneous
PCI8412ZHK
DVT
Clamp Voltage For PCI (IO 5V/3.3V)
(IN 1.5V/50mA)
MS31_51_DVT
MINI1
MS50_MINI PCI CONN_2x42X
FOX_AS0B126-S52N-1F
AV INPUT
CN25
MS50_B TO B HEADER CONN_10P
FOX_HS8110E
DVT for EMI
MiniPCI
TV-Tuner
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
PCI (PCI BUS) / TV-Tuner
MS51(MBX-152)
Thursday, July 27, 2006
http://laptop-motherboard-schematic.blogspot.com/



http://laptop-motherboard-schematic.blogspot.com/



http://laptop-motherboard-schematic.blogspot.com/

FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title	PCI (MS-DUO/SD/MDC)	
Size A3	Document Number MS51(MBX-152)	Rev 0.30
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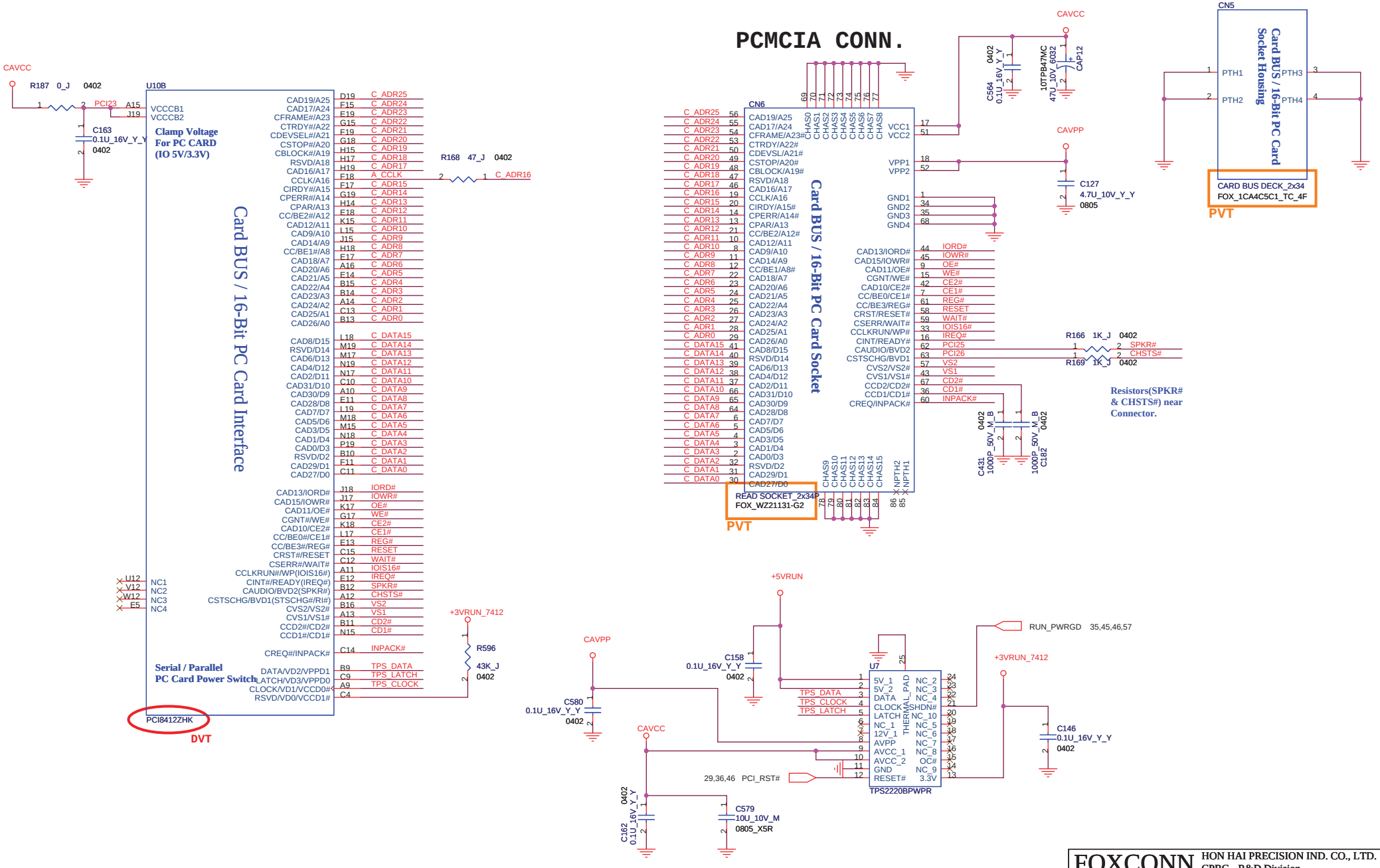
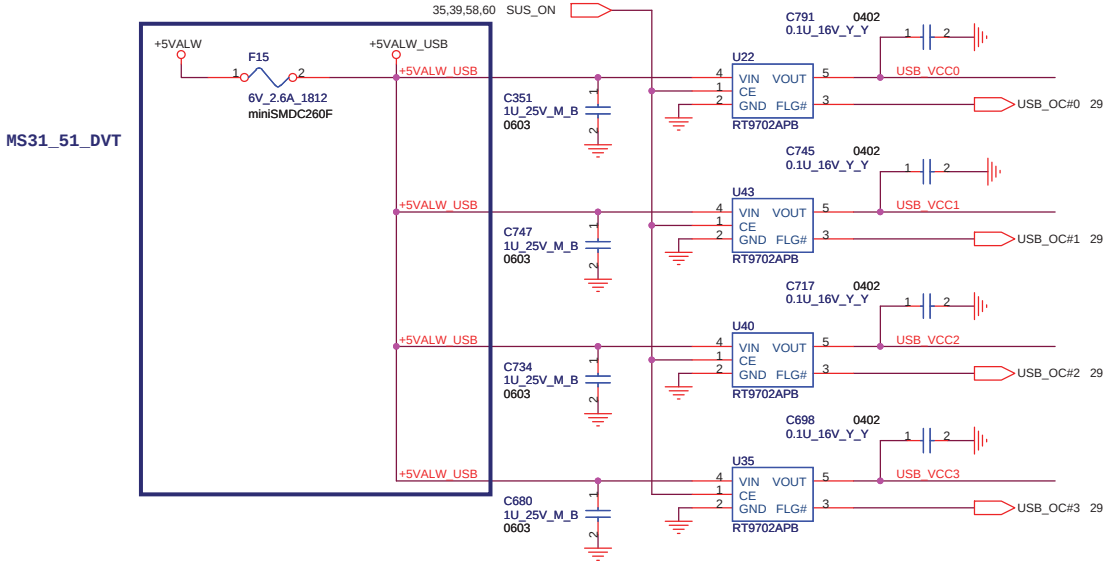
PCMCIA CONN.

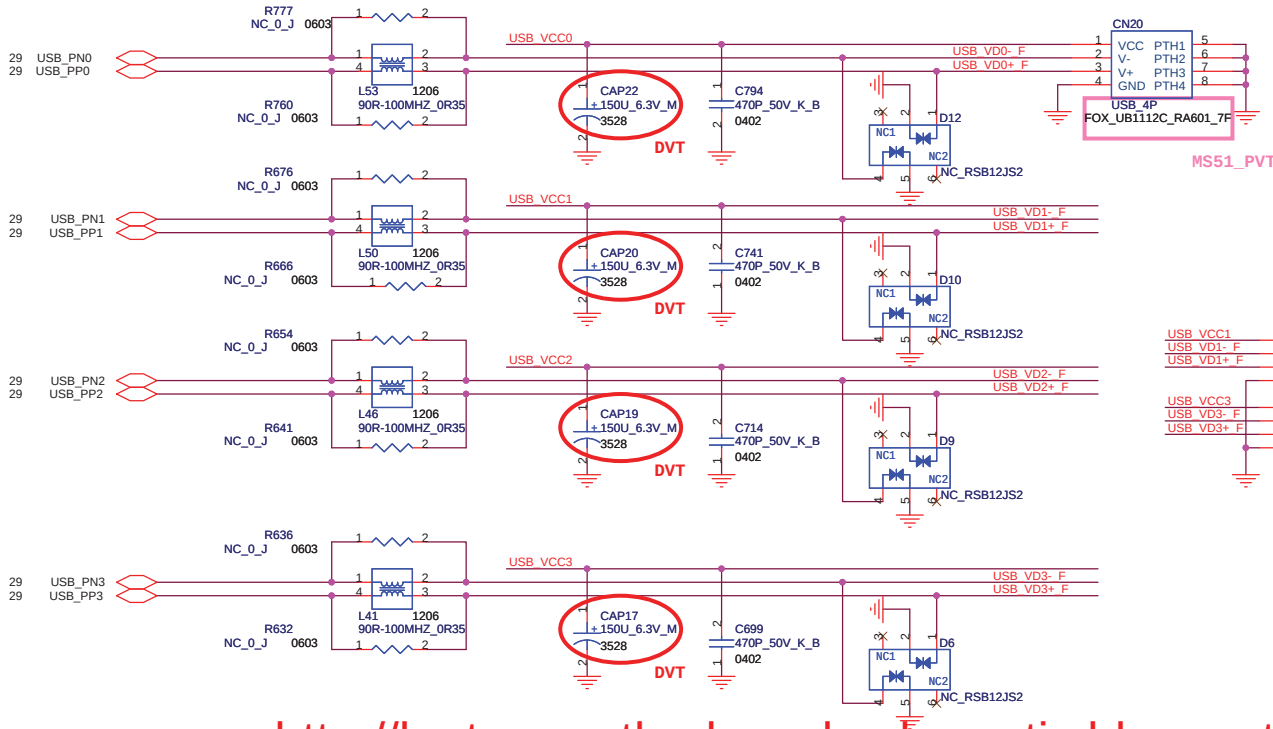


FOXCONN	HON HAI PRECISION IND. CO., LTD.	
	CPBG - R&D Division	
Title	PCI (PCMCIA)	
Size A3	Document Number MS-30/50(MBX-152)	Rev 0.30
Date: Thursday, July 27, 2006	Sheet 49 of 67	

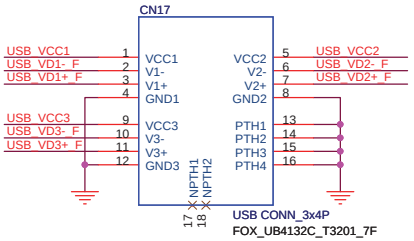
http://laptop-motherboard-schematic.blogspot.com/



Use Power Switch

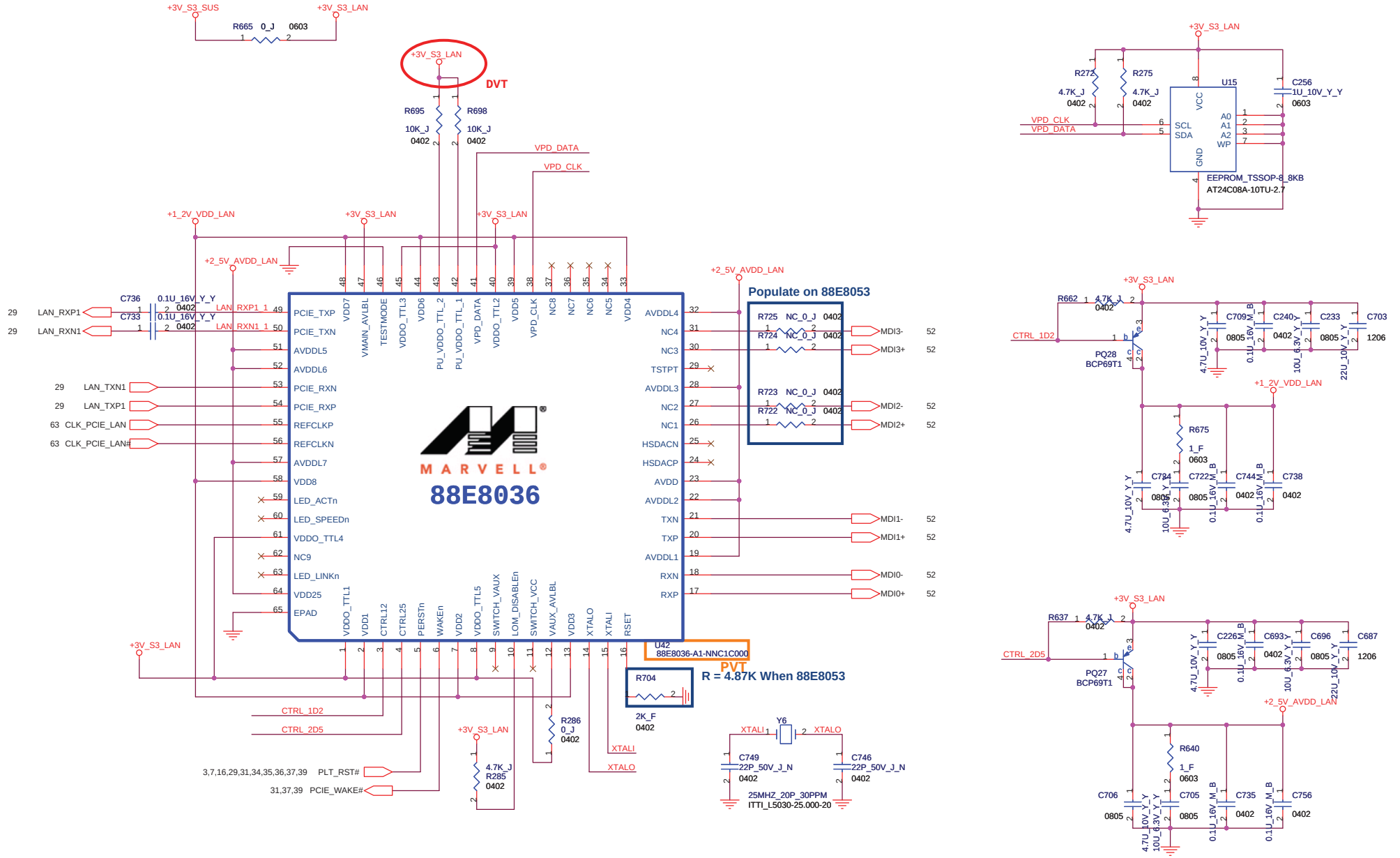


USB CONN X 4



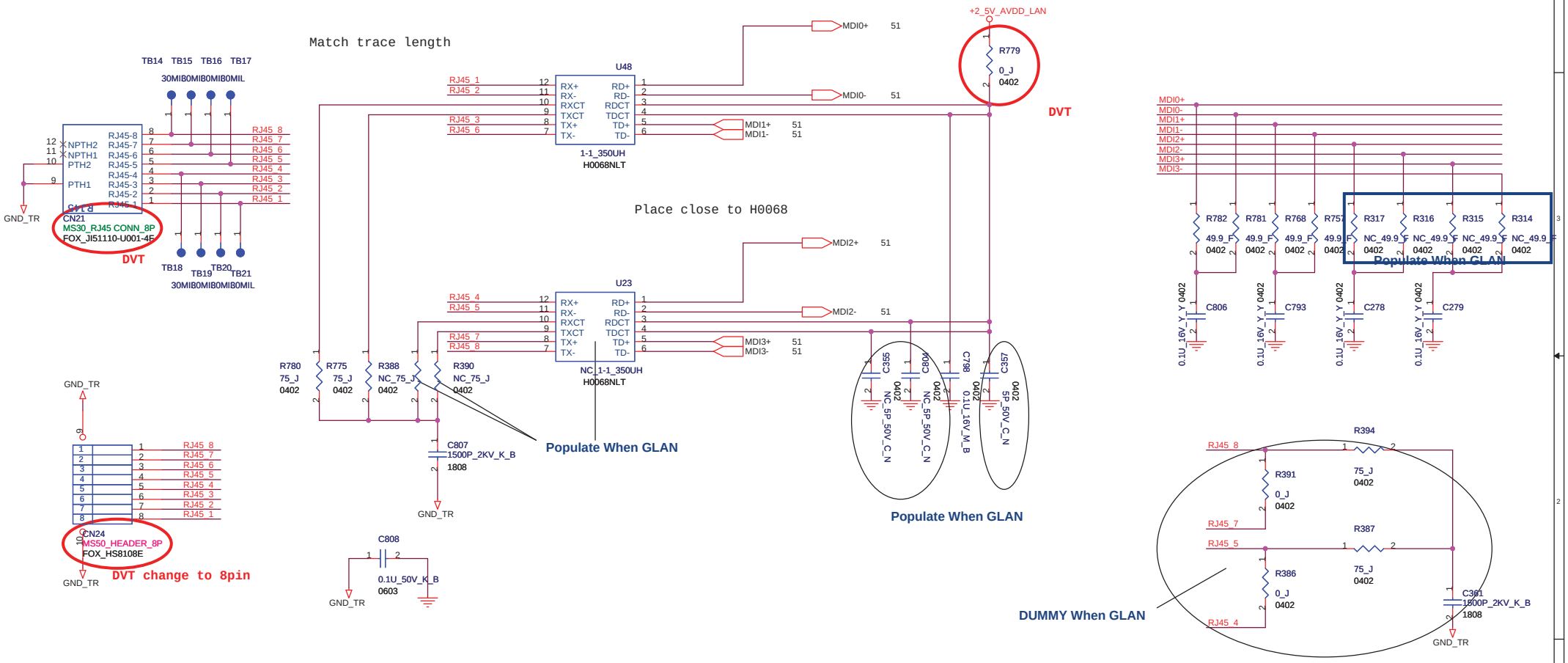
http://laptop-motherboard-schematic.blogspot.com/

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	USB2.0/DOCKING CONN.	
Size A3	Document Number MS51(MBX-152)	Rev 0.40
Date: Thursday, July 27, 2006	Sheet 50 of 67	



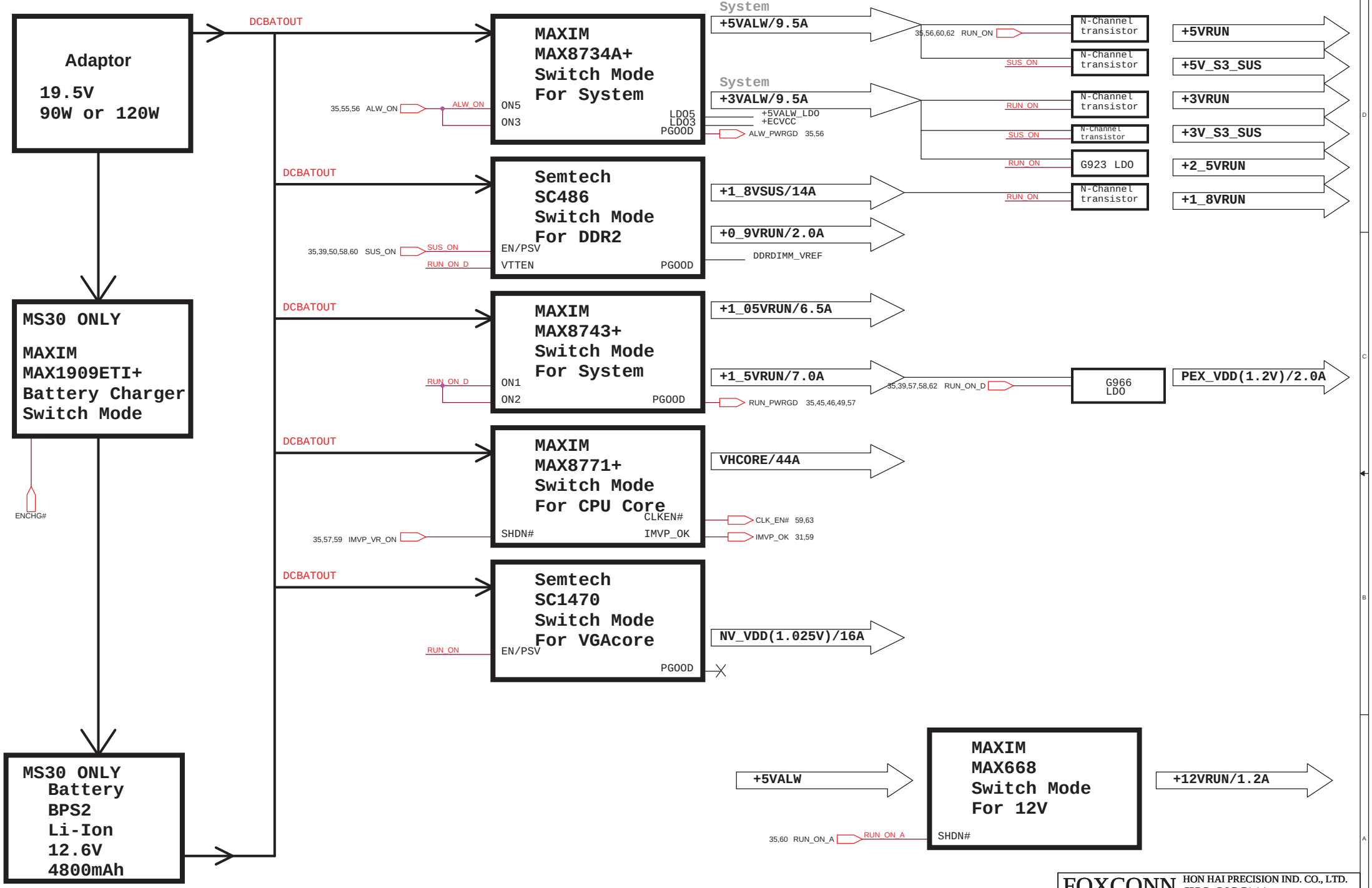
FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title	Marvell_LAN (1/2)		
Size A3	Document Number MS51(MBX-152)		Rev 0.30
Date: Thursday, July 27, 2006	Sheet 51 of 67		

http://laptop-motherboard-schematic.blogspot.com/



FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	*Marvell_LAN (2/2)*
Size A3	Document Number MS51(MBX-152) Rev 0.30
Date: Thursday, July 27, 2006	Sheet 52 of 67

http://laptop-motherboard-schematic.blogspot.com/



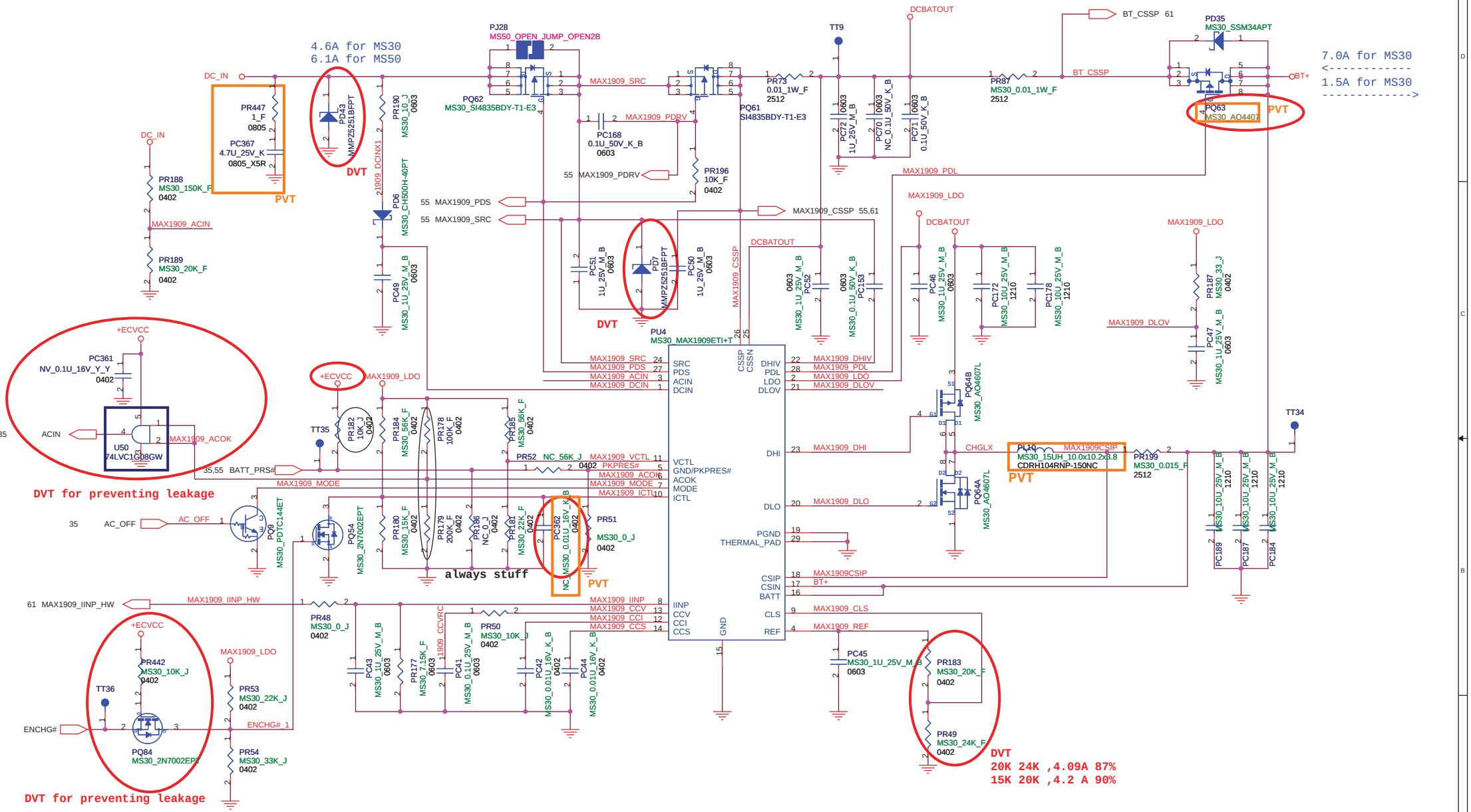
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: *Power Design Diagram-ZG*

Size: A3 | Document Number: MS51(MBX-152) | Rev: 0.30

Date: Thursday, July 27, 2006 | Sheet 53 of 67

http://laptop-motherboard-schematic.blogspot.com/



FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: Charger Max1909

Size: A3 | Document Number: MS51(MBX-152) | Rev: 0.30

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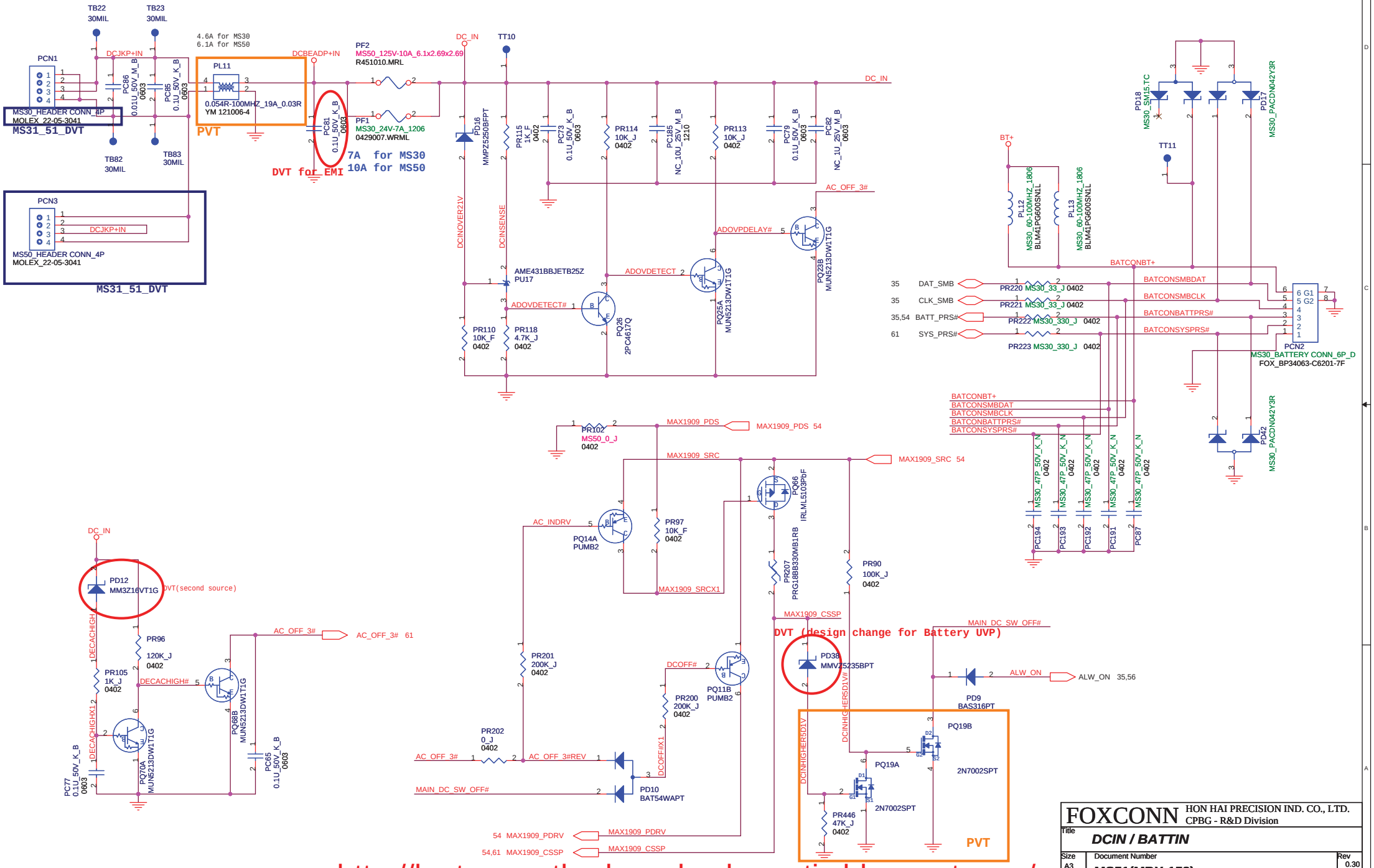

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	DCIN / BATTIN	
Size A3	Document Number MS51(MBX-152)	Rev 0.30
Date: Thursday, July 27, 2006	Sheet 55 of 67	

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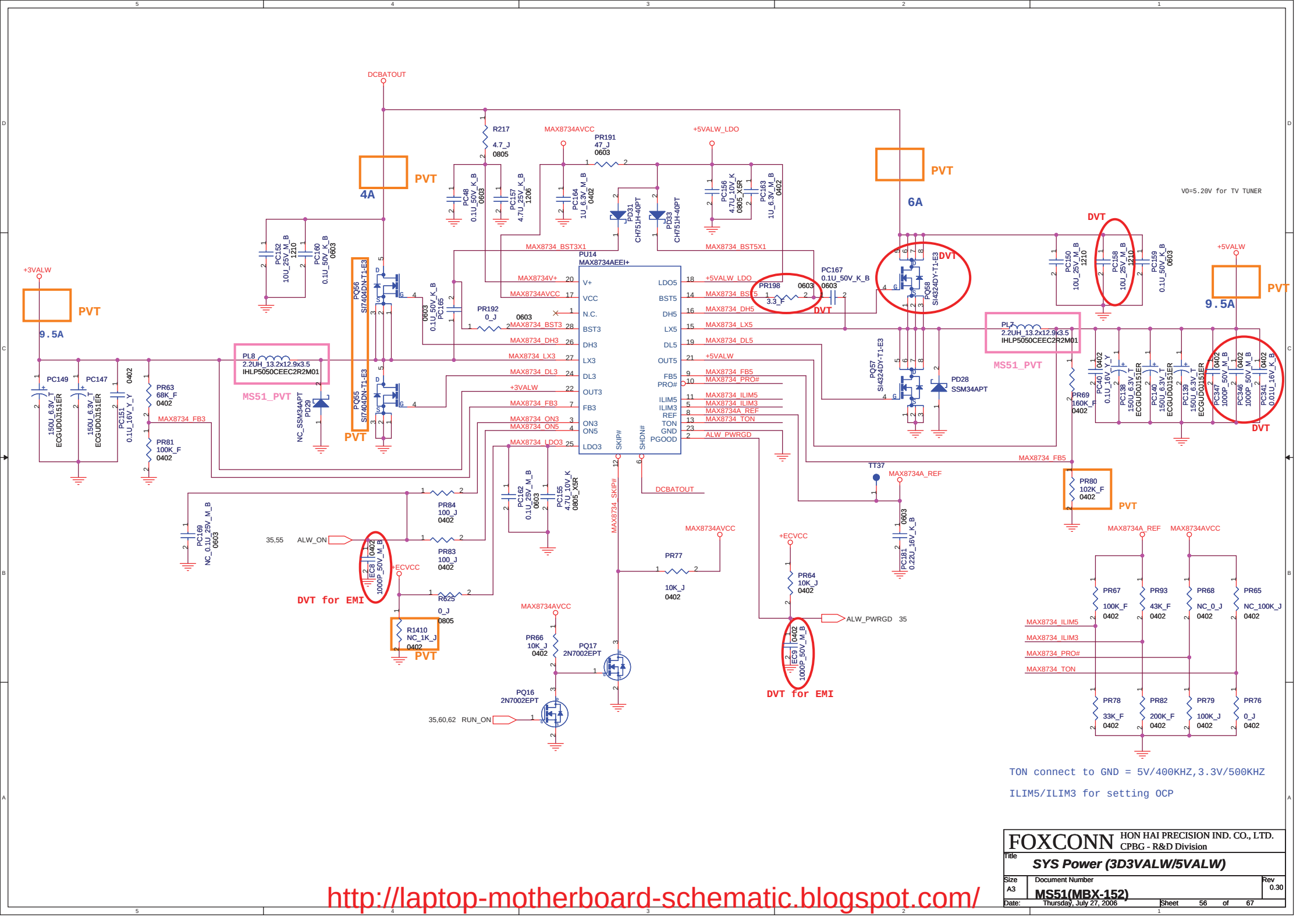

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FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	SYS Power (3D3VALW/5VALW)
Size	A3
Document Number	MS51(MBX-152)
Rev	0.30
Date:	Thursday, July 27, 2006
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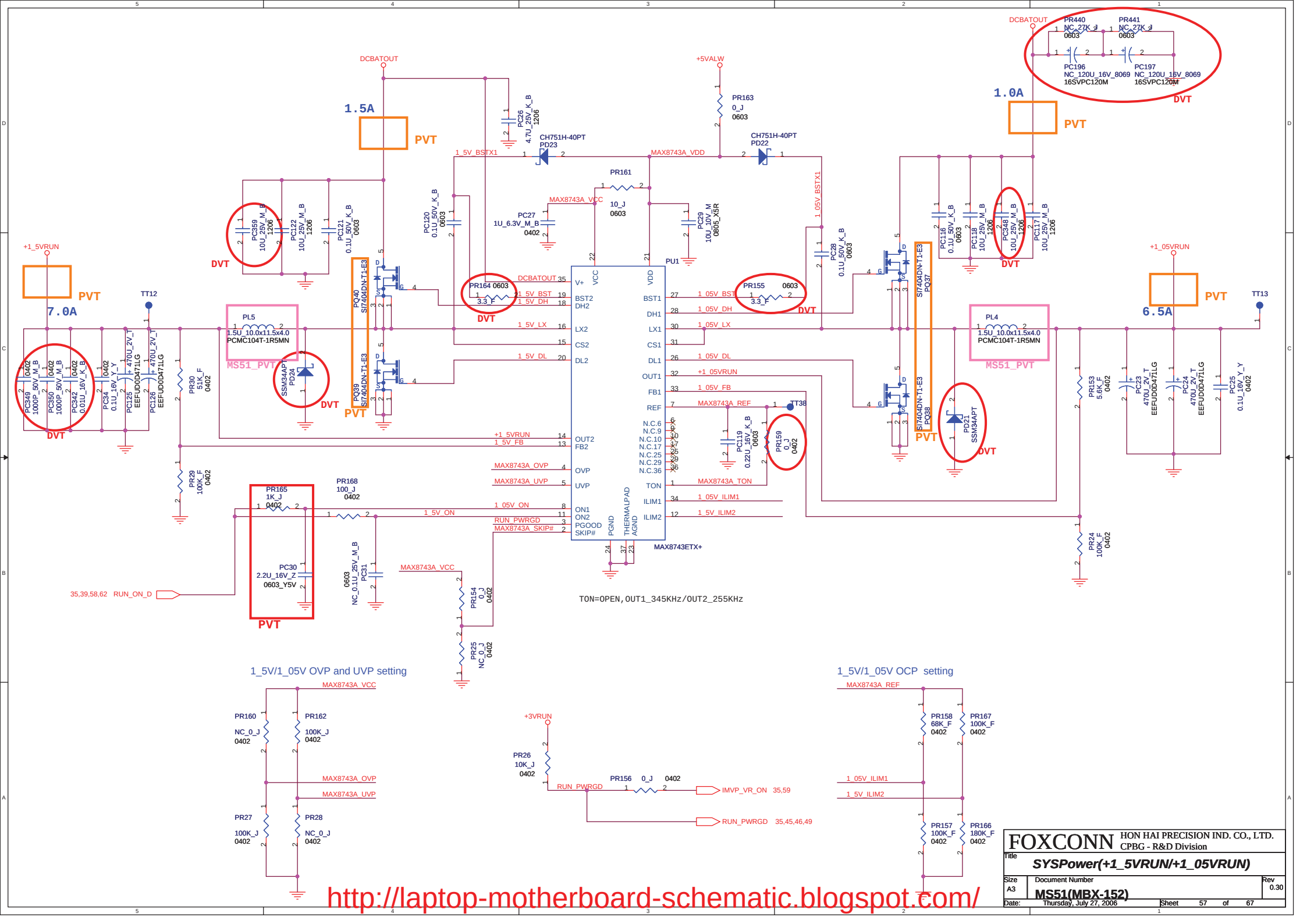
DCBATOUT
+5VALW
+1_5VRUN
+1_05VRUN
1.5A
1.0A
7.0A
6.5A
PVT
DVT
MS51_PVT
TT12
TT13
TT38
PL5
PL4
1.5U_10.0x11.5x4.0
PCMC104T-1R5MN
PU1
MAX8743ETX+
TON=OPEN,OUT1_345KHz/OUT2_255KHz
1_5V/1_05V OVP and UVP setting
1_5V/1_05V OCP setting
35,39,58,62 RUN_ON_D
IMVP_VR_ON 35,59
RUN_PWRGD 35,45,46,49
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
SYSPower(+1_5VRUN/+1_05VRUN)
MS51(MBX-152)
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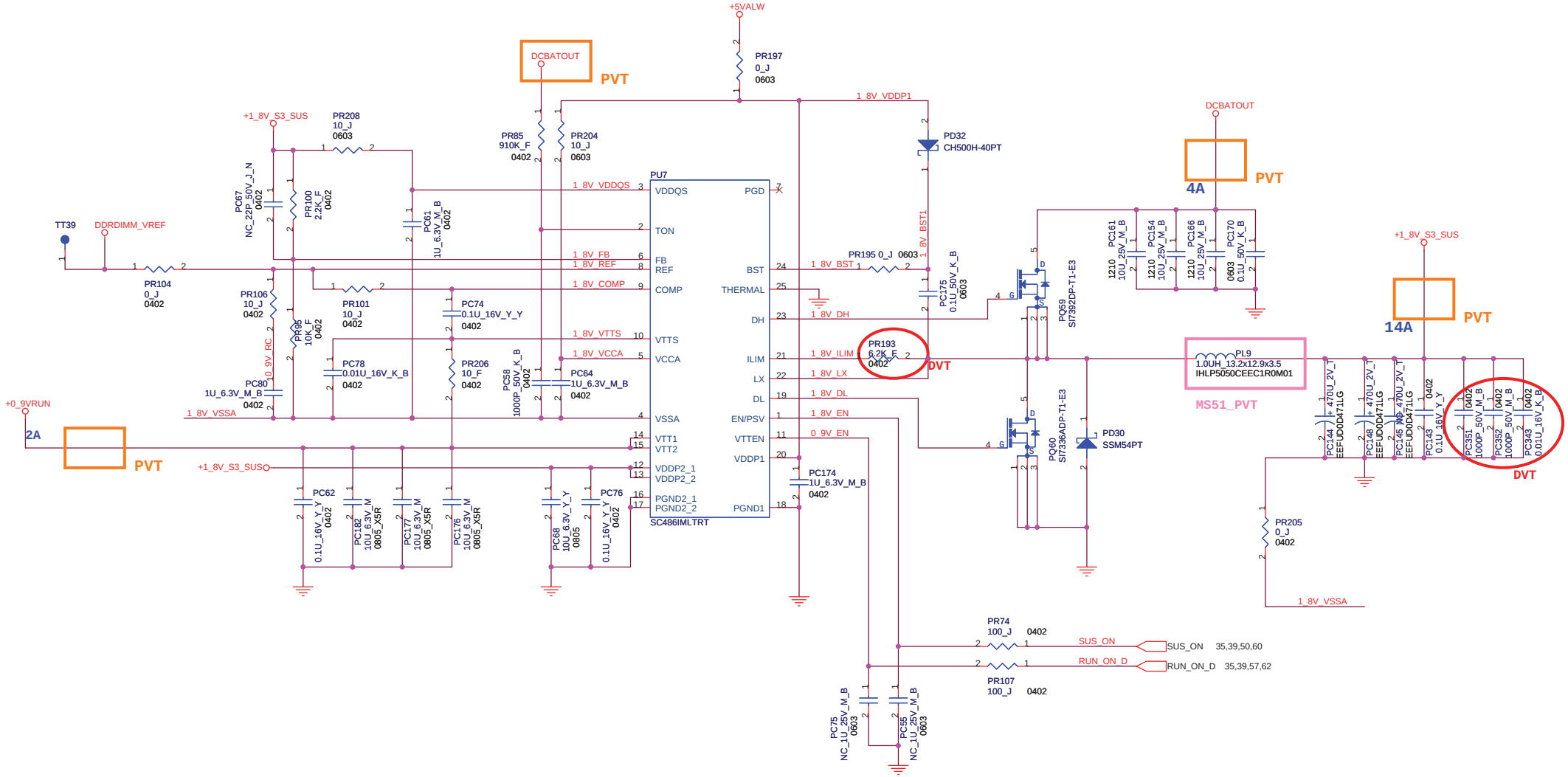
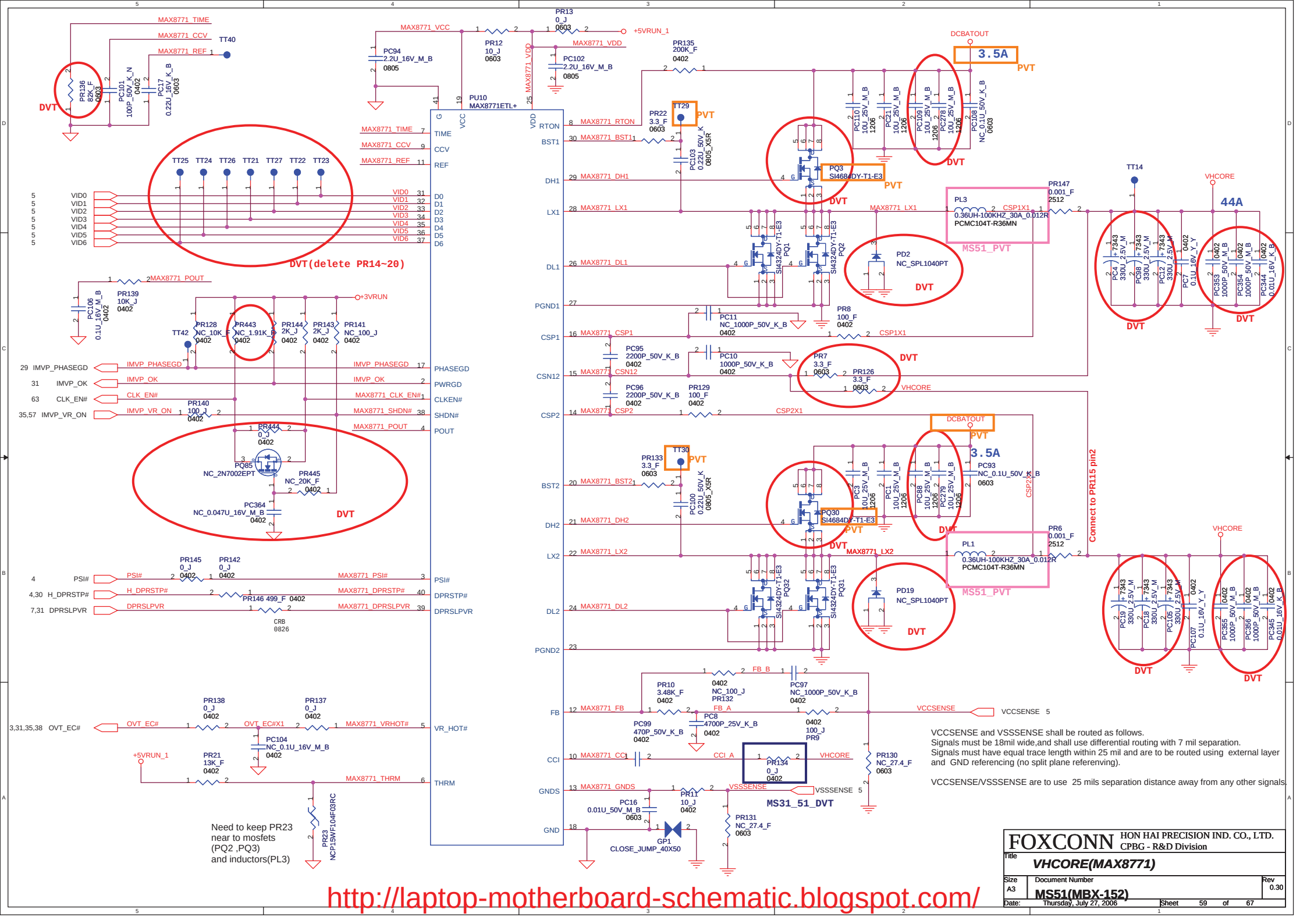
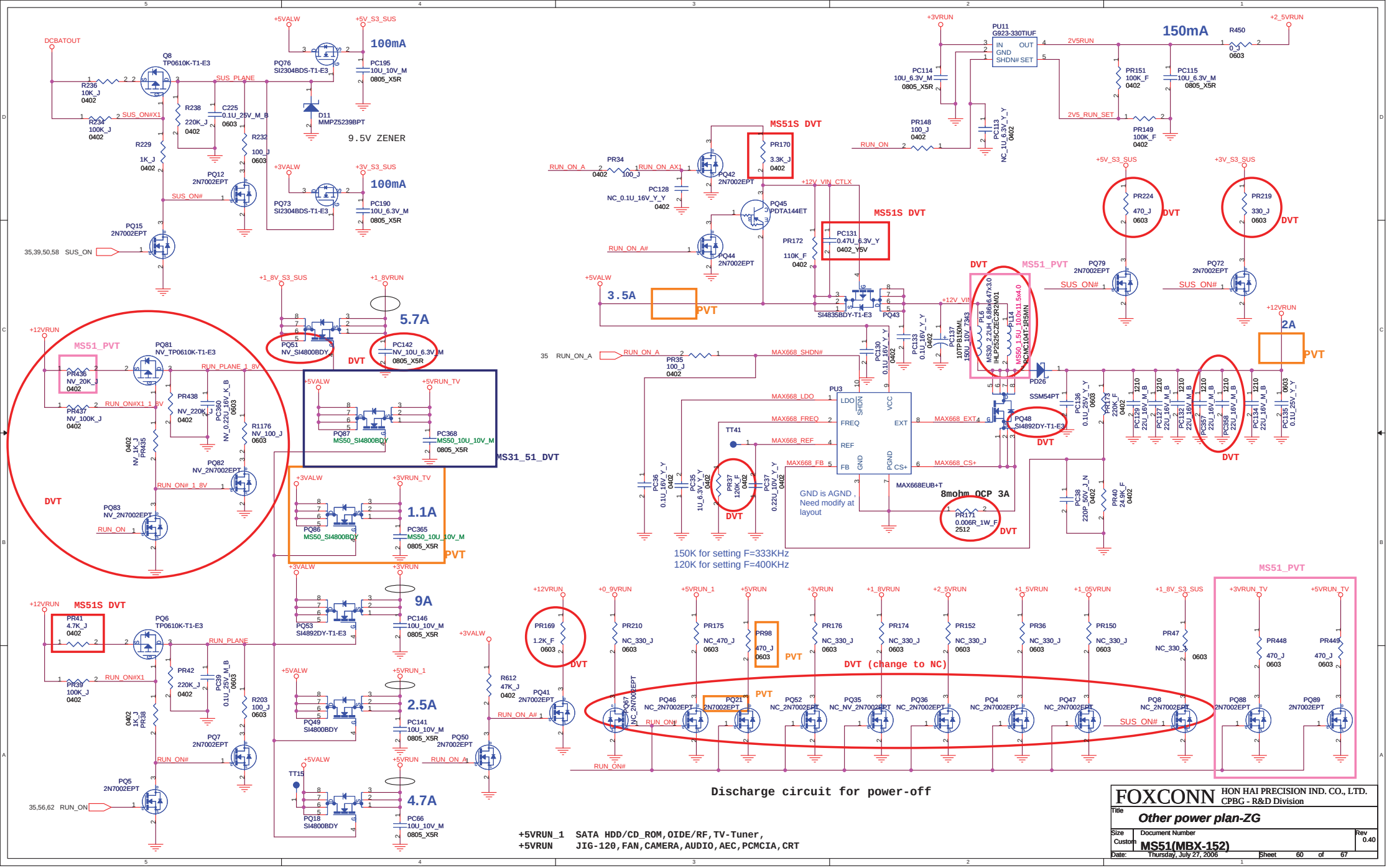


FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	DDR2Power(+1_8V_S3_SUS/+0_9VRUN)	
Size A3	Document Number MS51(MBX-152)	Rev 0.30
Date: Thursday, July 27, 2006	Sheet 58 of 67	

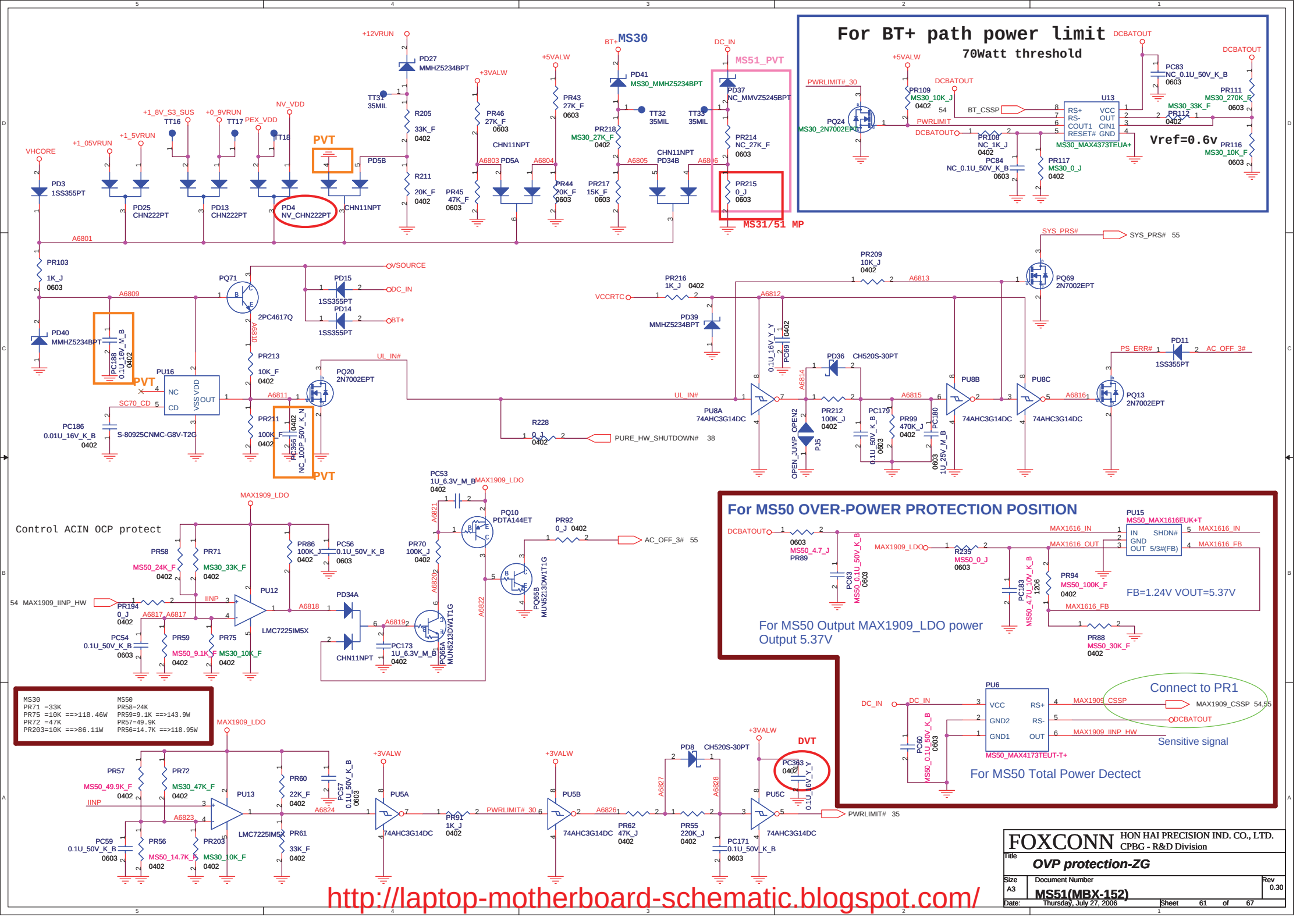
http://laptop-motherboard-schematic.blogspot.com/



http://laptop-motherboard-schematic.blogspot.com/



http://laptop-motherboard-schematic.blogspot.com/


For BT+ path power limit
70Watt threshold
Vref=0.6v
MS51_PVT
MS31/51 MP
PVT
DVT
Control ACIN OCP protect
For MS50 OVER-POWER PROTECTION POSITION
For MS50 Output MAX1909_LDO power Output 5.37V
FB=1.24V VOUT=5.37V
Connect to PR1
Sensitive signal
For MS50 Total Power Dectect
MS30 PR71 =33K PR75 =10K ==>118.46W PR72 =47K PR203=10K ==>86.11W
MS50 PR58=24K PR59=9.1K ==>143.9W PR57=49.9K PR56=14.7K ==>118.95W
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
OVP protection-ZG
MS51(MBX-152)
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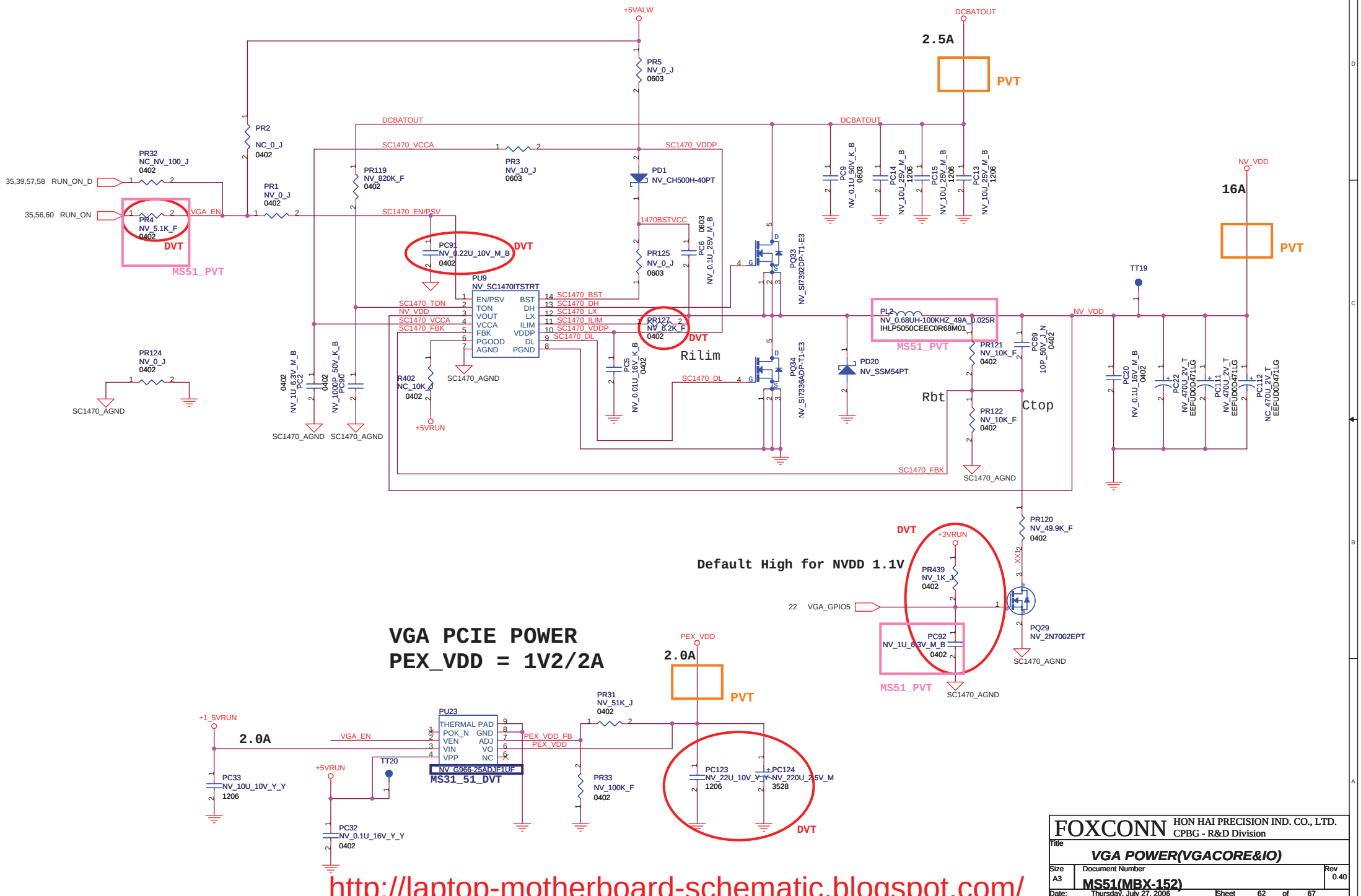

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FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division
Title	VGA POWER(VGACORE&IO)
Size	A3
Document Number	MS51(MBX-152)
Rev	0.40
Date:	Thursday, July 27, 2006
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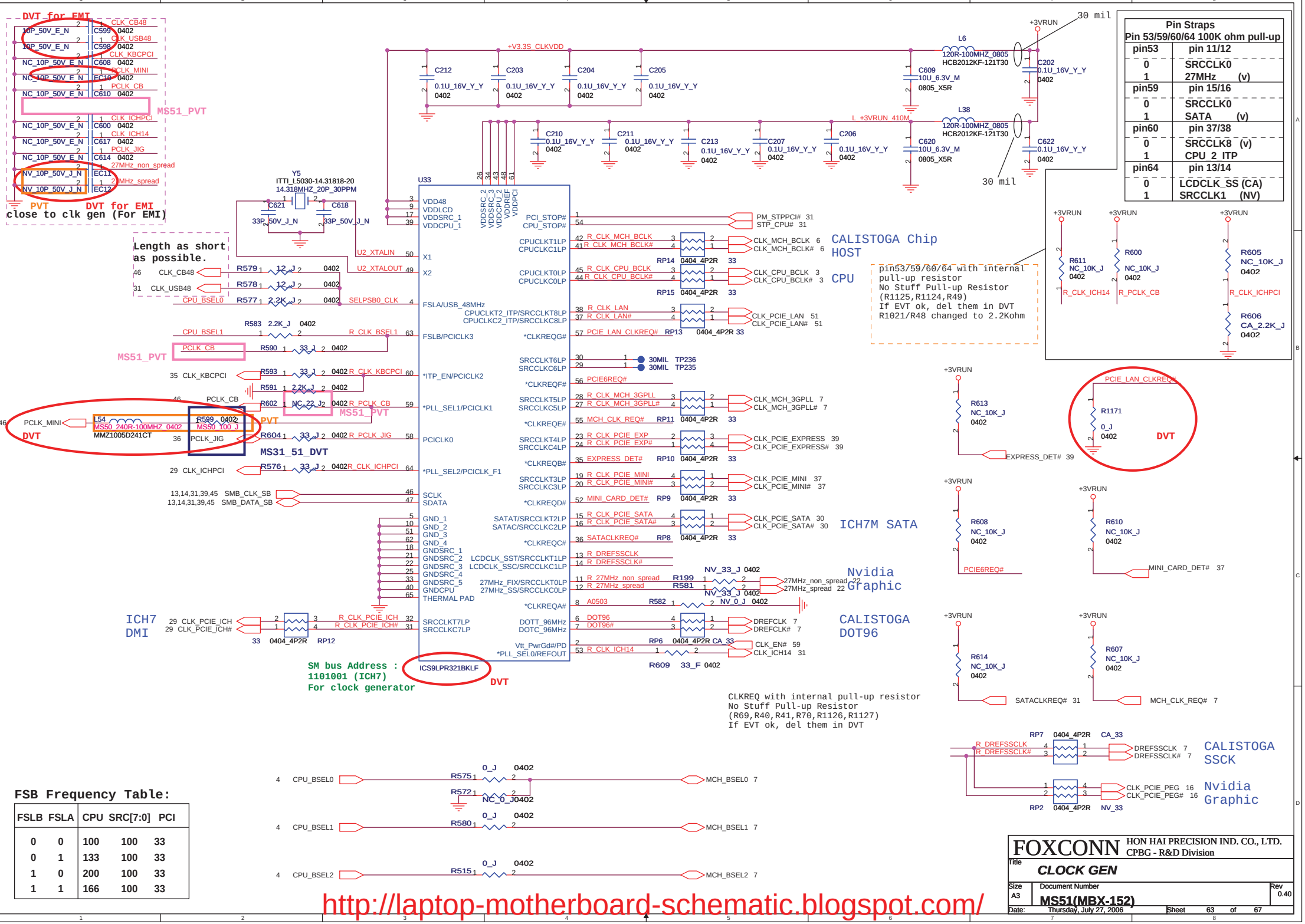
DVT for EMI
MS51_PVT
PVT
DVT for EMI
close to clk gen (For EMI)
Length as short as possible.
Y5
ITTI_L5030-14.31818-20
14.318MHZ_20P_30PPM
U33
ICS9LPR321BKLF
DVT
SM bus Address :
1101001 (ICH7)
For clock generator
MS31_51_DVT
CALISTOGA Chip HOST CPU
ICH7M SATA
Nvidia Graphic
CALISTOGA DOT96
ICH7 DMI
CALISTOGA SSCK
Nvidia Graphic
pin53/59/60/64 with internal pull-up resistor
No Stuff Pull-up Resistor
(R1125,R1124,R49)
If EVT ok, del them in DVT
R1021/R48 changed to 2.2Kohm
CLKREQ with internal pull-up resistor
No Stuff Pull-up Resistor
(R69,R40,R41,R70,R1126,R1127)
If EVT ok, del them in DVT
30 mil
30 mil
Pin Straps
Pin 53/59/60/64 100K ohm pull-up
pin53
0 SRCCLK0
1 27MHz (v)
pin59
pin 15/16
0 SRCCLK0
1 SATA (v)
pin60
pin 37/38
0 SRCCLK8 (v)
1 CPU_2_ITP
pin64
pin 13/14
0 LCDCLK_SS (CA)
1 SRCCLK1 (NV)
FSB Frequency Table:
FSLB FSLA CPU SRC[7:0] PCI
0 0 100 100 33
0 1 133 100 33
1 0 200 100 33
1 1 166 100 33
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
Title
CLOCK GEN
Size A3
Document Number
MS51(MBX-152)
Rev 0.40
Date: Thursday, July 27, 2006
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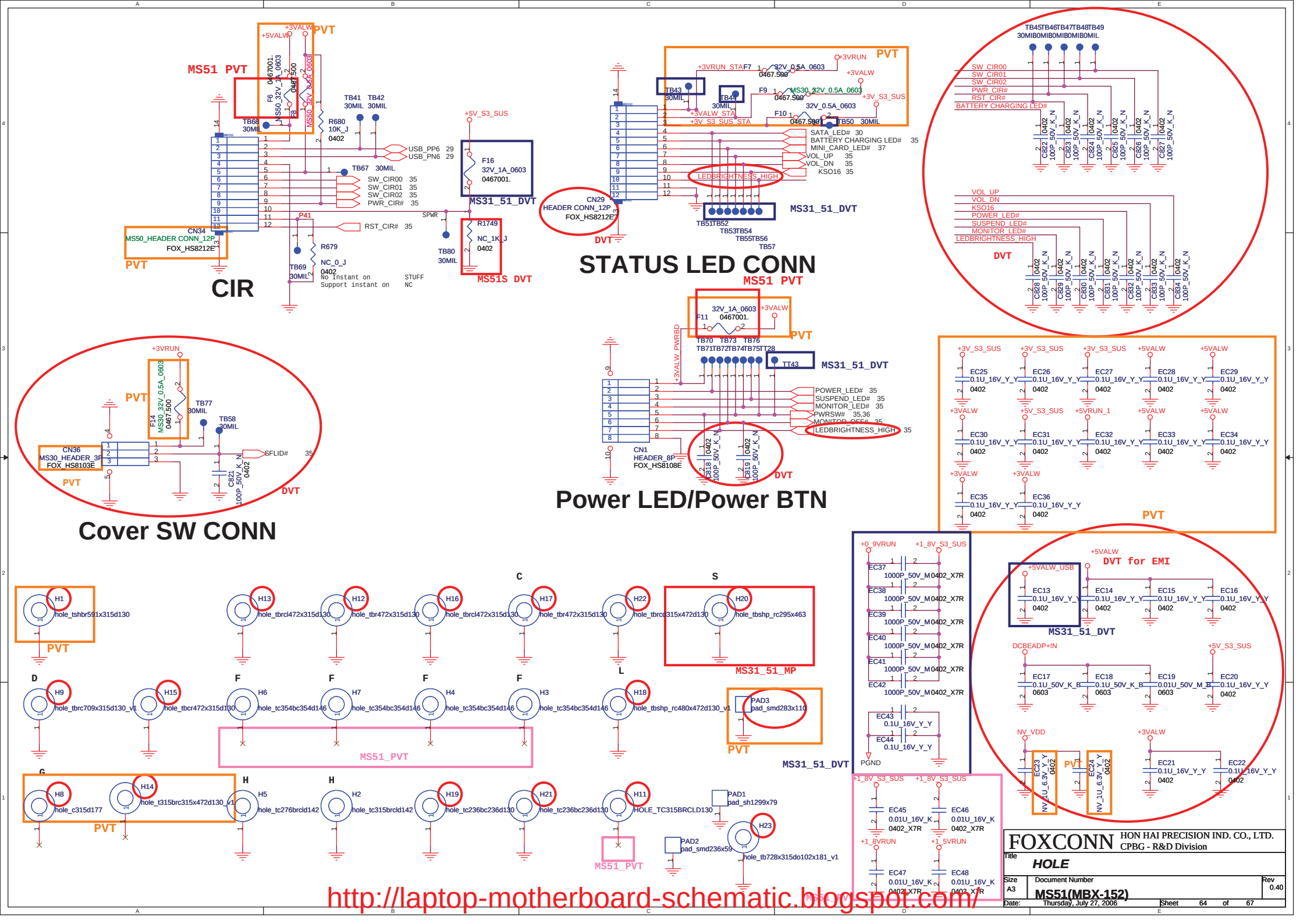
CIR
STATUS LED CONN
Power LED/Power BTN
Cover SW CONN
MS51 PVT
MS51_PVT
MS31_51_DVT
MS31_51_MP
MS51S DVT
DVT
PVT
DVT for EMI
CN34
MS50_HEADER CONN_12P
FOX_HS8212E
CN29
HEADER CONN_12P
FOX_HS8212E
CN1
HEADER_8P
FOX_HS8108E
CN36
MS30_HEADER_3P
FOX_HS8103E
SW_CIR00
SW_CIR01
SW_CIR02
PWR_CIR#
RST_CIR#
BATTERY CHARGING LED#
SATA_LED#
MINI_CARD_LED#
VOL_UP
VOL_DN
KSO16
POWER_LED#
SUSPEND_LED#
MONITOR_LED#
PWRSW#
LEDBRIGHTNESS_HIGH
SFLID#
USB_PP6
USB_PN6
PGND
FOXCONN
HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division
HOLE
MS51(MBX-152)
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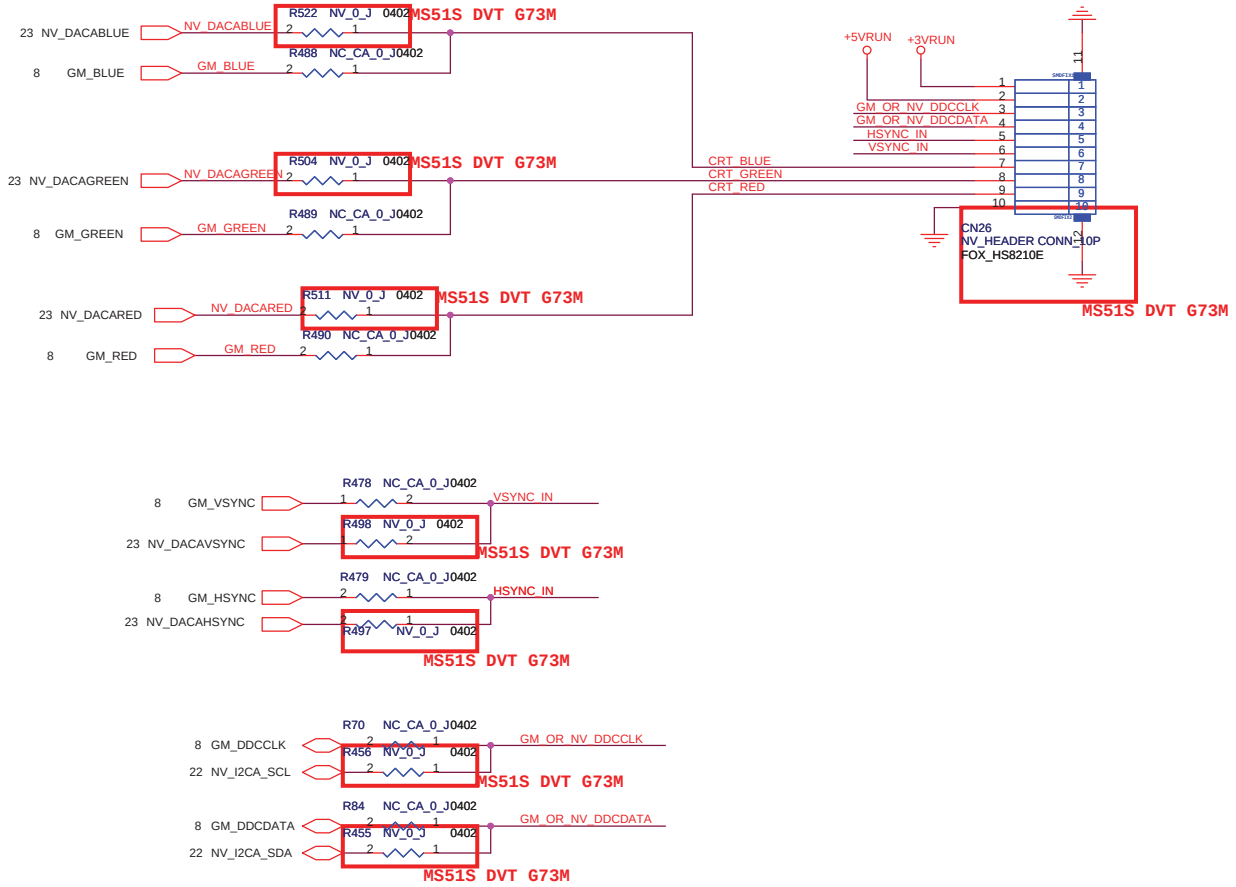

FOXCONN	HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title	CRT	
Size A3	Document Number MS51(MBX-152)	Rev 0.30
Date: Thursday, July 27, 2006	Sheet 65 of 67	

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P50 Connect U67,U63,U64,U114 pin 1 from RST_SUS# to SUS_ON
P39 Add CN21 signals for both OIDE (MS_30) and RF(MS_50)
P64 Add CN36 for CIR I/F

9/6
P30 remove R584 ,short CLK_32KX2 and CLK_32KX2_R
P63 remove R1055,short U2_XTALOUT and A0501
P39 remove Q79,R1266,C1222,R1267,Q80 ,connecto L66 to +5VRUN
P46 change CN59 to 10p and pin define
P47 add U59,C969 for reserved 1394 EEPROM
P64 (1)remove CN44,CN45,CN46,
(2)R756 pin 1 connect to +3VRUN
(3)change CN61 pin define
P46 Add U58A pin J2 as MS_LED
P34 CN32 pin 37 change to test pad

9/6 Power
P54 (1)remove PR314,PR315,PR316,PR317,PQ92A,PQ92B,PQ93A,
PQ93B,PC2,PR318,PR313,PQ21,PC336,PR24,PQ8
rename MAX1909_BATT to BT+ for delete BATT_EN function
(2)remove PR319
P62 (1)add PC1640,PR1802,PR1804,PQ76, for VGA power dynamic switch
(2)add PC197 for VGA power input caps
P65 remove C1152,move R1225,R1228 to Page8
P61 remove PD36 for delete net BATT_EN function

9/7
P52 remove R1305 and R1309 for duplicate with R1750 and R1754
P29 change GPIO IMVP_PHASEGD to SB GPIO5,
P31 (1)SB GPIO 10,12,13,15 PH 10K to +3VALW(R649,R650,R671,R672)
(2)SB GPIO 21 PH 10K(R1168) to +3VRUN
P37 BT_WLAN_SW# PH 10K(R1317) from +3VRUN to +3V_S3_SUS and add C1637
for ESD
P35 (1)Remove D26,R1108
(2)ALW_ON,SUS_ON,RUN_ON,RUN_ON_A,RUN_ON_D,SIO_FA1 PL 47K(R1805,R1806,
R1807,R1808,R1809,R705)to GND
(3)U32 pin106(E51RXD)connect to CN15 pin23, U32 pin107(E51TXD)
connect to CN15 pin25
(4)change U32 Pin176 to NC for reserved fan2
(5)change U32 Pin23 to NC
(6)change U32 Pin24 to NC
(7)change U32 Pin28 to JIG_SMI#
(8)change U32 Pin41 to NC
(9)change U32 Pin54 to NC
(10)change U32 Pin91 to NC
(11)change U32 Pin105 to FWH_BOOT
(12)change U32 Pin109 to PWR_CIR#
(13)change U32 Pin118 to PWR_RF#
(14)change U32 Pin168 to PWR_OK
(15)change U32 Pin171 to FAN1_TACH
(16)change U32 Pin175 to NC
(17)change U32 Pin71 to VOL_UP
(18)change U32 Pin72 to VOL_DN
(19)change U32 Pin73 to NC
(20)change U32 Pin74 to NC
(21)change U32 Pin99 to NC
(22)change U32 Pin100 to NC
(23)change U32 Pin1 to RST_CIR#
(24)change U32 Pin82 to SW_CIR00
(25)change U32 Pin83 to SW_CIR01
(26)change U32 Pin84 to SW_CIR02
(27)change U32 Pin36 to FAN1_PWM

P56 ALW_PWRGD PH 10K(PR328) from 3D3V_OUT to +ECVCC
P64 CN36 pin9 PWR_CIR# PH 10K(R1786) to +3VALW
P39 RN31 pin2 PWR_RF# PH 10K(R1791) to +3VALW
P35 (1)Add U32 pin97 as SYSTEM_ID4,pin 98 as SYSTEM_ID5,
(2)change U32 pin175 to NC
P16 (1)remove R262 short L_NV_VDD and NV_VDD to NV_VDD
(2)remove R259 short L_PEX_VDD and PEX_VDD to PEX_VDD
P21 Add L107,C483,C484,C486,C482 for VGA VID_PLLVDD power rail
P44 Add C1088 for filter
P24 (1)U12, Group4->Group5,Group6->Group4,Group5->Group7,Group7->Group6
(2)U11,Group3->Group3,Group2->Group2,Group1->Group1,Group0->Group0
P25 (1)U13,Group1->Group1,Group0->Group3,Group3->Group0,Group2->Group2
(2)U14,Group5->Group7,Group6->Group5,Group4->Group6,Group7->Group4

9/7 Power
P53 Add +5V_S3_SUS and +3V_S3_SUS in power block diagram
P55 Add PR342 for MS50
P56 (1)change PR65 from 270K to 200K 1% 0402
(2)change PL9 from 2.2UH_6.86x6.47x3.0 to 2.2UH_13.2x12.9x3.5
(3)change PQ27,PQ109 from SI4800BDY to SI7404DY-T1-E3
P45 change U122,U123 from G913 to G923-330TIUF
P41 (1)change C876 from 10U_6.3V_M to 10U_25V_M_B
(2)change CAP13 from 47U_6.3V_3528 to 10U_25V_M_B
P59 (1)change PQ118,PQ120 from SI7392DP-T1-E3 to SI4684DY-T1-E3
(2)change PQ117,PQ119,PQ121,PQ122 from SI7336ADP-T1-E3 to SI4324DY-T1-E3
P60 change PQ52 from SI4800BDY to SI4892DY-T1-E3
P61 Add U132 for BT+ path power limit

9/8
P3 add C3 close to chip for sensor
P22 add C487 close to chip for sensor
P35 U32 pin24 change to NC
P7 Add C1396 for DDRDIMM_VREF
P52 remove C1602,C1614,C1616,C1618 for duplicate parts

9/13
P48 add Q57 for SD power
P5 short R1415
p31 add R673 for reserved OVT_EC# to SB GPIO12
P3 R1404 change to 56ohm
P3 remove R1400 ,add TP(TP596) for DBRESET#
P7 add RN32 for external vga use
P3 add text note for VCCA_CPU
P8 remove R1633,R1634 adn add test pad for L_CLKCTLA,L_CLKCTLB
remove R1632
P08 add R1810,R1811 for CRT disable
P12 remove R1774 and add test pad for MCH_CFG_20
P19 add value NV_ for C322,C323,CAP10
P21 add value NV_ for L136,C1633
P22 R321,R317,C495,C494,Y2 to NC,
Mount R1132,R1131
C496 value remove NV_
P25.26 change C605,C575 value to NV
P28 C1151 value remove NV
P29 SPI_CS#/SPI_MOSI/SPI_MISO add test and remove pH resistors
P30 remove R590, R591, R607, and R1205
P30 C1530-1533 remove
P31 add R675,R1762,R1761,PQ78,PQ79 for lan SMbus S3_SUS power
change U31 power source to +3VRUN and SMbus connect to
SMB_CLK_SB,SMB_DATA_SB
P32 change R1384 to 0603 size
P34 R987 short to GND
CN32 pin 3 connect to GND
pin 32 NC , remove R1510
P35 R698,R699 pull up to +ECVCC
P61 add PURE_HW_SHUTDOWN# to OVP
P39 U36 pin21 connect to +3V_S3_SUS
P48 remove R1778
P49 add R1812 ph 10K to +3VRUN for U58B pinC4
P51 add C311,C349 for PCIE AC couple caps
P56 remove U130 connect ON3_ON5 to ALW_ON
P22 add R1819,R1818 for 27MHz_non_spread 3.3V level to 1.2V
P40 (1)change U39 pin25,38 power source to +5VRUN
(2)C1249,C1250 value add NC_ and connect to MIC_L
C1251,C1252 value add NC_ and connect to MIC_R
(3)chagne U39 pin37 to NC
(4)C1270,R799 connect to Digital GND
(5)remove GP3 and add C1638
(6)change U41 to 78D05
P41 (1)R847,R852 change to 33K
P42 (1)R1171,R1172 change to 4.7K
(2)R1635,R1637 change to 11K
R1639,R1640 change to 20K
(3)MIC1_VREFO_R change to MIC1_VREFO_L
(4)add GP16,GP17
P43 (1)move R1319,R1360,C1255,R1321,U127A,U127B,R1329,C1230,
R1318 to IntMIC Board
(2)remove U103,U105,D67,C1188,Q87,Q42,U104,R1370,R1361,
U50,R1376,Q86,R1156
add R1823,R1824,R1826,R1822,R1825,Q88,Q89,Q90,R1827,
R1828,R1829,C1640,Q91,C1639
(3)MIC1_VREFO_R change to MIC1_VREFO_L
(4)change C1088 to 10u_10V_Y_Y,
change R1323 to 6.8K
add R1821
P45 (1)connect U122,U123 pin 2 to A_GND
P46 (1)connect U58 pinK5 to PWR_OK
(2)add R1830
(3)modify CN59 pin define
P51 (1)add R1831,R1832,remove U129 pin42.43(SMbus) interface to
SB SMbus
(2)add R1833
P38 connect OVT_EC# to U131 pin4
P60 R1602,PR426 change to 470K
P61 PD34 change to MMHZ5234BPT, R1796= 33K 1% 0402, R1797 20K 1% 0402,
PR185 = 15K 1% 0603
P31 add SW2 for SYSTEM_ID0~03 on SB GPIO 22,23,33,34
P35 RP110 PH +5V_S3_SUS
P62 PR1804 change to 10K
P61 change PR199 to 33K
change PR207 to 47K
add PR1834,PR1835,PR1836,PR1837 for MS50
P30 R1304 change to NC_
P35 Add R702 for Monitor_off# PH
P28 add L138,L137
P47 L73 change to 90R-100MHZ_0R35 and add L141

9/14
P24 change U12 to no mirror setting
P25 change U14 to no mirror setting
P44 change R1868 to 2K
change R1869 to 2K
add R1870,R1872 for power rating

9/15
P50 Swap L87 for layout
P38 add L140
P45 populate R1783,R1784
Dummy R1663,R1782,R1662
P40 change U41 to TPS79301DBVR
P45 change U58 pinK5 to RUN_PWRGD
P46 add R1873 for separate 7412 power
P63 change PR418 to 820K 1%
change PR421 to 10K 1%
change PC210 to 10pF
P58 change PR333 to 910K 1%
change PR305 to 9.1K 1%
change PC374 to NC_470U
P10 change L117,CAP27,C1386,L120,CAP28,C1389 value to CA_*
P31 rename SMB_CLK_SUS to SMB_CLK_ALW,SMB_DATA_SUS to SMB_DATA_ALW
P29 RSVD1,2,5,6 connect to GND
P60 R1602,PR426 change to 220K
P41 change amp to LM4991LD

9/16
P22 U8 pin 4 connect to THERM_ALERT#GPIO8
U8 pin6 connect DDR_ALERT_EC#
P38 add R769 for OVT_EC# PH resistor
P50 change CN37 pin connection
P48 correct CN55 symbol
P52 change CN63 pin define
P55 change PCN4 pin define

9/20
P29 Swap net of RP92-RP95
P31 Del PQ62,PQ67,R635,R669 and R637
Change Net name SMB_CLK_SB , SMB_DATA_SB of U29C-Pin C22 and B22
P32 Change L119 to 4.7uH
P34 Add Net : SLOT_IN at CN32-Pin50
P35 Add Net : SLOT_IN and add R1884-1886 at U32-Pin172
Del Net : FWH_BOOT, Change to TP785 of U32-Pin105
P36 Del R735 and del Net : FWH_BOOT of CN15-Pin15 , Change to TP786 ,
Change symbol : CN15
P38 Change symbol : U20
P39 Del RN31,Add R1881(ON),R1882(Dummy),R1883(Dummy)
Change R784 power from +5VALW to +5V_S3_SUS
Change R1800 power from +5VALW to +5V_S3_SUS
P40 Change Net name : MIC1_L ,MIC1_R of U39-Pin35 and Pin36
Del C861,C1248 and del NET: PC_SPKRIN
Del C1574,C1575,R797,R799 and C865
Change Net name PCBEEPPL to AEC_MIC_L
Change Net name PCBEEPPR to AEC_MIC_R
Add R1887-R1890 , D80 , Q103,Q104 and CN66
P41 Change symbol & value : C910,C911 to 0.033uF
Change symbol : U141,U112
P43 Change Q89 and Q90 to Dummy
Del U100,R1322 and C894
P44 Change symbol : U133,U134,U135 and U137
P46 Change symbol : LED4
P48 Change symbol : CN26
P50 Del R969,R972,R1044 and R1525
Change Package CAP17,CAP18 and CAP34
P53 Change +12VRUN/1.5A to +12VRUN/1.2A
Change +3VALW/7.0A to +3VALW/9.5A
Change +1_8VSUS/16A to +1_8VSUS/14A
P54 Add R1838,R1839 at PU1-Pin5
Add R1840,R1841 at PQ11-Pin1
P57 Change PL10&PL11 to 1.5uH
P58 PD16 Change to CH500H-40PT
P59 Change PL13&PL21 to 0.36uH
P60 D79 change from NC to mount
Change +5VALW from 4.2A to 3.5A
Change +12VRUN from 1.4A to 1.2A
Del PC380,PC381(22uF POS CAP)
Add PC380,PC381,PC401 and PC402 to 22uF MLCC type cap
Change PR174,PR182 and PR187 to Dummy
P61 Del PD2A/B,PD27A/B and PD30A/B
Add CHN222PT for PD2,PD27 and PD30
P62 Change PD53 to CH500H-40PT
P63 Vertically RP10&RP109

0921
P48 add R1892,R1893 for discharge path
P03 change Q100 to MMBT3904 and add R1891
P64 Connect CN36 pin5 to +3VALW
P34 Change D77,D78 to SSM22LLPT
P56 change PR49 to 160K_F,PR52 to 100K_F for TV-TUNER
P39 add R785,R784 for reserved +5VALW for RF
P58 change PC89 to 0.1uF,PR335 to 10 ohm ,PC90 to 10nF
P17 change R205 value to NV_,R206 to NC_ for Infineon
P24,25 change U11,U12,U13,U14 to Infineon HYB18H512321AFL20
P36 change BIOS ROM(U34) to EN29LV800BB-70TCP(EON)
P60 change D79 to 9.5V Zener MMPZ5239BPT
P28 change U17 to G548B2P1U
P40 (1)remove L112, connect U39 AVDD1,AVDD2 to VDDA
(2)C1576,C1577 change to 2.2UF
(3)serial R1896,R1897 for SPK_L,SPK_R
(4)change C1238,C1239,C1270 to 1UF
(5)add C1687,C1688,C1689,C1690 for AEC_MIC_L,AEC_MIC_R
(6)replace C869 with CAP38(100U_6.3V_7343)
(7)add R1898,R1899,C1691,PQ128,R1901,R1900,C1692,R1902,PQ129,R1905,R1903,
PQ131,R1906,
R1904,PQ136,R1907
P41 (1)change amp gnd to PGND,
(2)add L142,L143,L144,L145
P60 change PR427,R1603 to 100K
add PQ126,PQ115,R1911,R1912
P48 CN26 pin2 connect to +3VRUN
P45 U124 pin 31 connect to RUN_PWRGD
P22 C487 change to NC_
P31 add R635 for protect GPIO33
P34 C791,C792 change value to NC_
P35 rename SLOT_IN to SLOT_ON
P46 change R32 to 100 ohm
P61 add R361 for merge Power Limit
P21 add R1275 for reserve disable CRT

0921 Audio
P40 (1)add sense_A,SENSE_B related schematic
(2)remove Buzzer schematic
(3)add C1687,C1688,C1689,C1690 for ACE_MIC_L,AEC_MIC_R
(4)serial R1896 on SPK_L,serial R1897 on SPK_R
(5)bypass L112, and connect to VDDA
(6)add L76 for U41 power
(7)add CAP38 for VDDA Output caps
(8)change R801 to 29.4K_F for adjust VDDA voltage to 4.75V
P41 (1)add R1908 for GND and PGND
(2)change AMP GND to PGND
(3)mix LCH and PC_SPKRIN,mix RCH and PC_SPKRIN
(4)add L142,L143,L144,L145 for speaker EMI
(5)NC D70 and D71
P42 add Line_in signal on CON4 pin4
P43 (1)reverse the polarity of HW_POP_MUTE_EC to HW_POP_MUTE_EC#
(2)separate MUTE signal (MUTE_AMP and MUTE_TR)
P44 (1)change EQ GND sourse to PGND
(2)change R1840,R1846,R1849,R1836 to 10K_D
(3)change R1857,R1863,R1853,R1865 to 10K_D
(4)change R1851,R1867 to 33K
(5)change R1858,R1841 to 10K_F 1%
(6)correct C1649,C1655,C1665,C1670,C1666,C1651 symbol
(7)replace C1678 with 22U_16V_M_B(100U/16V TQC 禁用料)
(8)replace C1680 with 100U_6.3V_7343
P45 connect U124 pin 31 to RUN_PWRGD

0922
P10 (1)bypass R1475,R1470
(2)change L115 to HCB2012KF-121T30
P19 (1)change C1192 to 0603 size
P22 remove R1133
P28 (1)change R461 to 200_J 0603
(2)add INV_BRADJ PL resistor R773
(3)connect NB_BRADJ to Cn49 pin4
P32 bypass R655
P39 (1)remove R774,R772,Q35,R1096
(2)connect CN19 to EXPRESS_DET#
(3)U36 pin23 change to NC
P46 separate C954,C955
P47 change R934,R940,R942 to 1K
P22 add R307 for NV_JTAG_TMS PH +3VRUN
add R309 for NV_JTAG_TDI PH +3VRUN
add R306 for NV_JTAG_TCK PL GND
P48 modify SD/MS card power
P64 change CN36 pin10 to CN+5V_S3_SUS
P10 change C1381,C1382 to 10U_6.3V_Y_Y
P52 connect CN40,CN63 GND to GND_TR
P55 (1)change PR373,PR374 to 10K
(2)change PR408 to 4.7K_J
(2)change PR15,PR16 to 33_J
(3)PC9,PC10,PC11,PC12,PC13 change to 47P

0923
P43 add C1695 for EMI
P59 change PR272 to 2K_J
P07 add R1444

0924
P41 change F1 to 125V-4A_6.1x2.69x2.69
P40 add R1913,R1914
P41 connect C865 to P_GND
P43 add R1871,C1641,R1917,Q92 for MUTE_TR
P43 change Q89 to NC_MMBT3904,change HW_POP_MUTE_EC# to HW_POP_MUTE_EC
P35 change HW_POP_MUTE_EC# to HW_POP_MUTE_EC
P23 change R1592,R1593,R1594,R1580,R1582,R1584 to NC
P05 bypass R1416
P07 mount R1443,NC R1441
P28 change U106,R1390 to NV_
P29 remove R577, add test pad for RSVD_9
P30 change R589 to 510_F,add R1916
P35 connect R707,R706 to +3V_S3_SUS
P35 remove U121,R1629,R1628,R1630
P61 remove PR368
P39 remove R1800
P39 change SW17 value to MS50_*
P39 add Q79,R1267,R1266,C1222,Q80,R788 for camera power
P35 add CAM_PWREN for camera power
P46 Mini1 Pin11,13 change to NC
P60 add PC399
P38 remove C827,add D80,C1696 for fan speed

0926
P63 R48 pin 1 connect to R_CLK_ICHPCI because swap R_CLK_ICHPCI and
R_PCLK_JIG
P35 remove R723
P43 remove R943
P60 (1)add +5VRUN_1 for layout,
(2)+5VRUN in P32,P34,P42,P59 change to +5VRUN_1,
(3)add PQ90,R191 for +5VRUN_1 discharge path

0926
P63 R48 pin 1 connect to R_CLK_ICHPCI because swap R_CLK_ICHPCI and
R_PCLK_JIG
P35 remove R723
P43 remove R943
P60 (1)add +5VRUN_1 for layout,
(2)+5VRUN in P32,P34,P42,P59 change to +5VRUN_1,
(3)add PQ90,R191 for +5VRUN_1 discharge path

0927
P60 add PC403,PR1797 for PQ135 soft start
P39 pin 3 connect to SUS_PWRGD
P48 add R1920~R1924,R1926~R1930 for MS DUo and SD signals
add R967,C1005 for SD_WP
P49 R965,R966 change to 1K
U62 pin 21 connect to RUN_PWRGD
P50 change USB power switch enable pin to SUS_ON
P41 add U142,R798,Q93,R1918,C1697 ,remove C1575
P42 (1)R848,R857 change to 20K
(2)mount R1639,R1640,and change C1578,C1579 to 470P
(3)move GP14 close to INT MIC jack
P43 connect R1825 pin2 to +3VALW
P44 connect C1676 pin2 to PGND,conenct C1675 pin2 to GND,put L139
between C1676 pin1 and C1675 pin1
P40 connect C873 pin2 to A_GND,conenct C1154 pin2 to GND,put L176
between C873 pin1 and C1154 pin1
P46 change Q1 to PDTC144EU
P62 reserve R1931 PH +5VRUN for VGA power good
P60 change PR406 to 0.008_1W_F
P36 correct U34 pin45 to SIO_FA0

0928
P60 change PR361 to 1K 0402
P46 change R1141 to 0 ohm
P60 (1)add PQ137,PQ67,
(2)change PR1797 to 1K,PR1795 to 110K
P51 connect LAN_TXP1 to U129 pin54
connect LAN_TXN1 to U129 pin53
connect C311 pin2 to U129 pin50
connect C349 pin2 to U129 pin49
P42 add R816,R814 for jack detect
P60 mount R1445

0929
P62 (1)add PR228 for vga power,
(2)PR415 pin1,PR416 pin1 connect to +5VALW
P47 mount U59,C969

0930(after rename)
P40 connect U19 pin49 to A_GND
P35 change CN35 value to MS30_HEADER CONN_7P

1001(after rename)
P34 cn10 pin 25,26 change to NC
P46 mini1 pin128,127 change to NC
P48 cn32 pin15,16 change to NC
P39 cn27 pin29,30 change to NC
P49 cn6 pin85,86 change to NC

1005R
P39 change R651 value to 10K_J
P38 change R499 value to NC_10K_J

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DVT
P64 CN1 pin1 change to +3VALW for leakage
P52 mount R779 for lan get ip fail
P40 net name HW_POP_MUTE_CODEC# change to
    HW_POP_MUTE_CODEC
P43 (1)net name HW_POP_MUTE_CODEC# change to
    HW_POP_MUTE_CODEC
    (2)change Q11 from MMBT3906 to MMBT3904
P60 mount PR224 for +5V_S3_SUS discharge too slow
P57 (1)change PR155,PR164 from 0ohm to 3.3 ohm for
    decrease 1.5V/1.05 noise
    (2)mount PD21,PD24 for decrease 1.5V/1.05 noise
P59 mount PC278,PC279; mount PC88,PC109 for
    decrease Vcore noise
P62 mount PC92 for decrease VGA power noise
P40 (1)mount R682,R694 for sense_B,sense_A detect
    (2)NC R308
P44 NC R643,R647
P43 mount R381 for amp abnormal be mute
P41 change JSPK1,JSPK2 from 2N-0002000-M0N0 to
    2N-0002001-M1T0
P39 change CN33 from 1N-0008000-M1T0 to
    1N-0008001-M1T0
P64 change CN36 from 1N-0002001-M1T0 to
    1N-0002000-M1T0
P46~49 change U10 to PCI8412ZHK
P59 change PQ3,PQ30 to 17-S14324D-YT00
P40 U19 change to CXD9872AR
P29~P33 for EVT2 U6 is 12-CALIST0-A300(GML)
P41,P42 CON1,2,3 change to 2N-0006002-FKX0
P22 R567 change to 16-CH5205S-0P00
P59 PQ58 change to 17-S14324D-YT00
P58 PR193 change to 6.2K_F,PR136 change to 82K_F
P62 PR127 change to 6.2K_F
P60 PR37 change to 120K_F,PR171 change to 6mohm,
    PL6 change to 2.2uH
P24,P25 Change R99,R148,R165,R167 from 120 Ohm to
    80.6Ohm 1%
P60 change PQ51,PC142,PQ35 value to NV_
P43 add Q12,R772,R773 for adding EC to control
    mute function
P45 (1)add R342,NC R343 for Change VP1020
    initialization to SHI mode
    (2)NC U45,R355
P59 NC PD2,PD19
P60 add PR219,PR169
P24 change R165 to 40.2_F and add R1160,C809,
    R1163,C810 for nvidia latest demo board for G72
P25 change R148,R99 to 40.2_F and add R1164,R1165,
    C811,C812 for nividia latest demo board for G72
P43 change U21 to M74VHC1GT32DFT2G for shortage of
    toshiba parts
P41 change Q24,Q25,Q26,Q27 to PBSS2515F.115 for toshiba
    parts shortage
P16 add U49 for PLT_RST# to VGA
P28 add C815,C813,C814
P29,45  connect GPIO17 to AEC pin30 powerdown
P35 (1)add D15,D16,D17 for preventing leakage
     from EC before power on
    (2)reserved U3 pin 176 for second fan FB,pin43
     for second fan PWM
    (3)add U3 P105 as EC_LED to control LED brightness
P36 change CN12 pin1,pin21 to +ECVCC
P38 (1)add R1166 for discharge path of +5VALW_LDO
P39 update Q19 footprint
P43 change Q11 to MMT3904
P34 add CAP23,CAP24
P62 add PR439,delete PR123,NC PC92  for preventing
    VGA_GPIO5 floating
P63 delete R204,add R1171 for PCIE_LAN_CLKREQ# pull low
P45 delete PQ77
P48 change CN18 to smaller size
P47 change CN14 to 1394 normal type
P42 change CON3 to Red color
P41 JSKP1 change to 3 pin for manufacture
P43 delete R396,R393,C359,R395,C360
P54 add PC340
P55 change PD38 to MMVZ5235BPT for battery in UVP fail
P38 change second fan to adjustable
P56 add PC347,PC346,PC341,PC158 for +5VALW
P57 add PC349,PC350,PC342 for +1_5VRUN
P58 add PC351,PC352,PC343 for +1_8V_S3_SUS
P59 add PC353,PC354,PC344,PC355,PC356,PC345,PC278,
    PC279  for VGCORE
P57 add PC348,PC196,PC197,PC359
P59 change PD2,PD19 to NC_SPL1040PT (10A)
P60 (1)change PQ48 to SI4892DY-T1-E3
    (2)add PL14 for MS50,PL6 for MS30
    (3)add PC357,PC358 for +12VRUN
P34 add CAP23,CAP24 for MS50 HDD
P30 add R1175 for MS50 SATA Cable
P64 (1) delete R783
    (2) CN1 add EC_LED to control LED brightness
    (3)CN1 pin 1 change to +5VALW
P60 add Pr436,PR437,PQ81,PR435,PQ83,PR438,
    PC360,PQ82,R1176 for +1_8VRUN timing
P54 (1)add PR442,PQ84,U50 and connect PR182 pin2 to
    +ECVCC for preventing leakage of charger LDO
P56,57,58,59,60  Update PL6,PL9,PL7,PL8,PL2,PL4
    PL5,PL14,PL1,PL3 footprint for shaking test

1201
P40,41 Swap SPK_L,SPK_R at source and speaker cnn side
P64 add C818,C819 for ESD
P40 CN19 change to CXD9872AK

1202
P40 Follow FAE suggestions
    (1)add C820(10U_10V_M) for AVDD
    (2)change C305 to 10U_6.3V for VREFFILT
    (3)change R752 to 1% tolerence

1205
P29 change GP4 to R1402
P51 add R1403,NC R665 for LAN S4 wake up
P54 add PC362
P57 add PR440,PR441 for balence 2 caps voltage
P22 U9 update new version

1206
P22 rename R567 to D19
P45 NC C770
P51 change R665 value to MS30_0_J,R1403 value to MS50_0_J
P60 NC PQ67,PQ46,PQ21,PQ52,PQ35,PQ36,PQ4,PQ47,PQ8
P62 change PC123 to 22U_10V_Y_Y,PC124 to 220U_2.5V_M
    for reduce PEX_VDD ripple
P64 add C821~C834 for protecting EC from ESD
P35 add C835~C838 for protecting EC from ESD
P39 add C839 for protecting EC from ESD
P36 add C840~C844 for protecting EC from ESD
P41 change R233,R231 to 47K_F,addC850,C847
    C851,C846
P44 (1)R261,R255 change to 56K_F
    (2)R248,R254 change to 2.4K_F
    (3)R246,R251 change to 2.2K_J
Add TB1~TP77,TT1~20 for manufacture TE test
P44 add GP7.GP8.GP9 for MIC quality
P57 mount PR159

1206_1
P3 change Q21 to 2N7002
1206_2
P59 PC4,PC12,PC18,PC19,PC98,PC105 change to
    330U_2.5V_M

1207
P28 change CN3 to 1N-0030000-FWG0
P42 change R693,R683  from 11K_F to 7.5K_F
P38 change second fan(CN7) source(R1173,Q29) to +12VRUN

1208
P52 CN24 chnage from 10pin to 8pin
P51 change R665 value to 0_J,delete R1403

1209
P59 add TT21~TT27 for manufacture
P61 add PC363 for PU5 power bypass
P38 add R1403 for reserve 12V path to second fan
P42 update U17 to MAX4232AKA+T
P59 delete PR14~PR20 ,and short
P08 delete R76,R63,R78,R542,R62,R77,R64,and short
P10 delete R544,R536,R65,R535,R79,R543 ,and short
P12 delete R514,R508,R541,add TP248,TP249,TP250
P30 delete R702,R697 and short
P41 (1)change R225,R226 from 22K_J to 47K_J
    (2)change TB8~TB11 to 40mil
P46 (1)add R1404,C1397(NC),C1398(NC) for separate power
for reduce
   noise of tv-tuner
P60 add R1415,C1400(NC),C1401(NC)    for separate power
for reduce
   noise of tv-tuner
P63 change R599 to 100_J,add L54 for PCLK_MIN1
P57 change PR440,PR441 from 2.2K_J to 100K_J
P54 (1)PQ63 change to SI4825
    (2)mount PD7

1212
P63 mount C598,C599 for EMI
P55 mount PC81 for EMI
P30,P46,P56,P63,P64 Add EC1~EC24 for EMI solution
P59 reserve PR444,PQ85,PR445,PC364,PR443 for
    max8771 CLKEN# abnormal
P29 change R389,R776 from 39_J to 47_J for SI

1213
P28 add Q31 for LCD_VDD discharge path
P46 change EC2~EC7 value to MS50_*
P43 mount R778,Q14
P44 (1)change R248,R254 from 2.4K_F to 1.5K_J
    (2)change R246,R251 from 2.2K_J to 2.4K_F
P48 (1)change R212,R213,R221,R222 from 0_J to 68_J for SI
    (2)change R215 from 1.5K_J to 1K_J from customer suggestion
P54 (1)change PR183 from 15.4K_F to 20K_F
    (2)change PR49 from 20K_F to 24K_F
    to set constant power to 4.09A(87%)
P57 (1)NC PC196,PC197
    (2)change PR440,PR441 to NC_27K_J

1214
P50 change CAP17,CAP19,CAP20,CAP22 to 100U_6.3V_M for vendor suggestion
P54 add PD43
P59 change PR7,PR126 to 3.3_J

1215
P61 change PD4 value to NV_*

1219
P54 change PD7,PD43 from 16-MMP2525-3B00 to 16-MMP2525-1B00
P63 change EC11,EC12 to 10P_50V_J_N
P51 change CN21 to MS30_*

1227
P42,P59 Update c282,C758,PC94,PC102

0110 for PVT BOM
P50 change CAP17,CAP19,CAP20,CAP22 to 150U_6.3V_M(NEC/TOKIN)
P54 (1)change PQ63 to AO4407
    (2)NC PC362 for battery issue
P41 change L42,L43,L44,L45 to BLM18PG330SN1D
P20 (1)change R555 to 49.9 ohm 1%
    (2)mount R556
P24 (1)change R165,R1160,R1163,R167 to 240_F
    (2)change C809,C810 to 0.01U
P25 (1)change R148,R1164,R1165,R99 to 240_F
    (2)change C811,C812 to 0.01u
P16~23 update U6 P/N to 12-G73NA20-A200
P43 NC R773 for +5VRUN leakage
P64 (1)change EC23,EC24 value to NV_*
    (2)change CN36 value to MS30_*
P60 mount PR98,PQ21 for +5VRUN leakage
P56 change PR80 to 102K_F for meet TV-tuner power spec
P59 change PQ3,PQ30 for better VHcore design

0120
P37 add Q32 for wireless led always on
P38 add D20,D21 for fan reverse current to damage Q5
P49 update CN6,CN5 footprint
P55 add PR446,combine PQ22A/PQ19B to PQ19(2N7002DW) for abnormal ALW_ON
P60 add PQ86 for improve rf quality
P43 add Q33,and change Q14 to MMBT3904 for leakage
P37 change SW2 to SSSU011700_SW-DIP3
P48 change CN9 to MOLEX_67913-0009 for factory repair

0121
P64 change CIR connector value to MS50_* for ms50 only
P39 change L8,L18 to 120R-100MHZ_0603 for curren rating
P8  mount R69,R68,R66,R493,R494 ;NC R83,R82,R80 for disable CRT
P10 mount R547,R518,C454 ;NC R540,C453,D3,R548,L21,L23,C414 for disable CRT

0123
P8  change R67 value to 0_J,dummy R495,R492,R81 for CRT disable
P65 dummy R488,R489,R490,R478,R479,R70,R84 for CRT disable
P19 dummy R558 for G73M
P61 change PC188 to X5R type
P22 dummy R5,R2,R8,R7,R10,C23,C25,C24,U26,R11
P63 change R599 to 100ohm 0402 1%
P30 add PJ31 for RTCRST#
P61 add PC366 for reserve ;PD5B pin 4 connect to GND for preventing floating

0125
P64 change PAD3 to pad_smd283x110
P54 update PL10,PL11 footprint for cold solder issue
P63 update L54 vendor to TDK
P28 delete L37 and short for inverter fuse current rating
P60 change PQ86,PC365 value to MS50_*
P56~62 delete PJ1~PJ4,PJ6~PJ27,PJ29,PJ30 and shot
P54,P56~61 add TT29~41 for power test

0207
P48 change CN32 to 1N-1010003-0000
P34 change CN10 to 2N-0022000-MKG0(shorter pin length)
P41 (1)change JSPK1 to 2N-0002002-M1T0(shorter pin length)
    (2)change JSPK2 to 2N-0003001-M1T0(shorter pin length)
P39 add F2 for protection
P16 reserve R1405 for new G73M
P22 reserve R1406 for new G73M

0208
P38 mount R1403,dummy Q30,R1173,R1174,Q29,D21 for fix mode by
    cusomer suggeston
P50 update U42 part number to 12-88E8036-A100 for manufacture
P64 change H1,H8,H14 footprint
P59 add TT42 for power test
P63 change R599 from 100ohm to 47ohm(1R-0000470-J200)
P39 change F2 to 1M-F24V0A2-0000(24V-0.2A_1206)
P34 reserve R1407 for Staggered spin-up disable by customer suggestion
P43 add C1401 by customer suggestion
P41 (1)change C220,C221 from 0.47u to 0.22u
    (2)change C675,C674 from 1u to 0.8u
    (3)change R1167 from 1K to 2.2K
    (4)add R1403,C1399,R1409,C1400 by customer suggestion
P48 NC CN18 pin1,4 and remove R742,R743,L51,L52 by customer suggestion
P22 mount R1406
P40 change U19 to CXD9872K

0209
P56 reserve R1410 for discharge path

0210
P28 mount C363,C364,C365,C366 for EMI
P41 (1)change R225,R226 from 47K to 100K,
    (2)change R227 from 2.2k t 270 ohm
P65 add EC25~EC36 for EMI
P44 add GP10 for EMI
P35 add U51,C1402 by customer suggestion
P55 change PQ19 to 17-2N7002S-PT00
P30 (1)change R745 value from MS30_24.9_F to 24.9_F
    (2)dummy R1175
P48 change R215 from 1K_J to 330_J for SD card power drop

0213
P44 change GP10 to R1411(MS50_0_J) for EMI
P38 add F3,F4 for cable short protection
P39 add F5 for cable short protection
P64 add F6~F11 for cable short protection
P31 (1)connect GPIO21 to U20 pin14 for bypass AEC
    (2)dummy R304 for double pull low
P45 connect U20 pin14 to SB GPIO21 for bypass AEC
P54 add PR447,PC367(snubber circuit) for dc_in inrush voltage/current

0214
P38 delete F3,F4
P64 add F14 for cable short protection
P35 add F12,F13 for cable short protection
P45 add R1412 for hardware disable

0214_1
P38 add F4
P60 correct PQ6,PQ81,Q8 part number(TP610K-T1-E3) to TP0610K-T1-E3
P56 correct PQ55,PQ56 value to SI7404DN-T1-E3
P57 correct PQ37.PQ38,PQ39,PQ40 to SI7404DN-T1-E3

0215
P39,P38,P35,P64 change F2,F4~F14 size from 1206 to 0603
P60 correct PQ6,PQ81,Q8 vendor part number(TP610K-T1-E3) to TP0610K-T1-E3

0216
P39,P38,P35,P64 change F2,F4~F14 to 1M-F32VA75-F001   FUSE,Littelfuse,0467.750,32V, 0.75A

0223_SMT
P28 dummy C363,C364,C365,C366 for LVDS timing by customer
P42 change R693,R683 from 7.5K to 13.7K for Line in FSIV
P39 change F5 to 32V_1A_0603,F2 to 32V_0.5A_0603
P29~P33 update U44 part number to NH82801GBM_B0
P54 update PR447 to 1_F 0805,1R-0000010-F500
P38,P38,P35,P64 change F2,F4~F14 to 1M-F32V0A5-F000 FUSE Littelfuse,0467.500,32V, 0.5A

MP

0302
P48 change CN32 to Yamaichi_JCS010_2005_1 for vendor shortage

0303
P41 (1)change C675,C674 to 1C-2B70225-M000 for 6.8U_6.3V_M shortage
    (2)add C1403,C1404(1C-2B70475-K201) for 6.8U_6.3V_M shortage
P39 remove TB6,TB7 for manufacture test issue

0311
P39 change F2 to 32V_1A_0603 for cureent rating
P41,43 Change Q9,Q13,Q28 from 17-MMBT390-6000 to 17-MMBT390-6K00
P57 change PR165 to 1K_F,PC30 to 2.2uF,16V for adjusting 1D05V power on/off sequence


MS31_51_DVT
04/20
P19 change L26,L27 to 10uH inductor(CS0603-10NJ-S) by vendor suggestion
P24 add GPIO NV_PWR_MIZER
    (1)add R1416,Q37,R1415,R1414,Q35,R1417,Q38,Q36
P25 add GPIO NV_PWR_MIZER
    (1)add R1420,Q41,R1419,Q40,R1418,Q39,R1421,Q42
P20 add GPIO NV_PWR_MIZER
    (1)change R563 to NV_4.3K_F,R564 to NV_10K_F
    (2)add Q34,R1413
P22 add GPIO NV_PWR_MIZER
    (1) add USF GPIO10 to NV_PWR_MIZER and PL R1412
P64 replace R678 with F16(32V_1A_0603)
P63 change R599 to 100_J for tv-tuner quality
P64 add EC37~EC44 for EMI
P50 add F15 for USB EU standard

0427 for G72M
P20 change R555 to 60.4_F by vendor suggestion for G72M
P24 (1)dummy R184,R181,R176,R160,R179,R177,R172,R159 for G72M
    (2)change R165,R167,R1160,R1163 to 60.4_F for G72M
    (3)change C809,C810 to 0_J for G72M
P24,P25 cahnge U28,U29,U30,U31 to HYB18H256321AFL20(256Mbit) for G72M
P25 dummy all parts for G72M
P27 dummy all parts for G72M
P28 dummy L24,C427,C438 for G72M
P19 mount R558 for G72M
P16~23 change U5 to G72M (12-GFG0740-A300)

0428
P64 EC13 power rail change to +5VALW_USB
P35,34 connect CN15 pin 37 to U3 pin 24 to detect ODD operation for 2nd fan control

0502
P38 (1)delete Q30,R1173,R1174,R1403,D21
    (2)add R1426,R1428,R1423,R1427,Q43,C1406,C1405,C1407,C1425,R1424,U52,C1408 for
    2nd fan control

0503
P42 change R693,R683 to 7.5K for CXD9872AK_4TH+ Line in FSIV
P24 mount R163,add R1737,dummy R174,R164 for 8M X32 Vram
P25 reserve R1739 for 8M X 32 Vram support
P35 change netname FAN2_PWM to FAN2_LIN
P60 add PQ87,PC368 for TV
P46 add C1409,C1410,C1411,R1738,C1412,C1413,C1414 for TV
P55 reserve PCN3 for new TV card ME interference
0504
P55 change PCN1 value to MS30_‧PCN3 value to MS50_
P40 change U19 to CXD9872AK 4TH+
P28 connect C813 to R589 pin1 and change value to 100P*
P35 add U53,C1415,R1470 for leve shift
0505
P38 reserve D21 for reverse current
P59 change PR134 to 0_J for phasegd abnormal behavior
P38 reserve PL R1741
P39 change Q19 to CHT2301PT for MMC2301 shortage
P38 change Q15 to CHT2301PT for MMC2301 shortage
P39,64 change CN29,CN33 test pad to tpc47t_67 by TE request
P64 add TT43 for PWRSW# by TE request
0508
P38 reserve C1416,C1417 for FAN VDD ripple
0509
P46 P46 add moat:TV_GND(R1742,R1743,R1744) for
    reduce GND noise
0510
P24 dummy C809,C810 for new G72M
P46 change R1406,R1738 as beads L55,L56
P38 mount C1417 for fan vdd ripple

0511
P34 change R1740 from PL to PH +5VRUN_1
audio
P43 mount R756 and change to 1R-0000103-J200 ,10K,1/16W,5%,0402
P44 (1)change C244,C237,C245,C243 from 1C-2B30153-M000,0.015uF,25V to
    1C-2B30682-M0000 6800pF,50V,06003,X7R Murata
    (2)for MS51:change R246,R251 from 1R-0000242-F200 ,2.4K,1%,0402
    to 1R-0000272-J200 ,2.7K,1/16W,5%,0402

0515
P62 update PU23
0516
P24 change L25,L26 to 1L-DWL1608-C100 ,Inductor,EIKAKU(SEC),WL1608C10NJ
    for no yageo inductor source
0517
P35 dummy R130,mount R133 for 31/51 MODEL ID
P10 change D3 from SECOS,SCS500V-40-LF to CHTS00H_40PT for simply BOM
P30 change D14 from SECOS,SCS500V-40-LF to CHTS00H_40PT for simply BOM
P32 change D1,D13 from SECOS,SCS500V-40-LF to CHTS00H_40PT for simply BOM
P48 change Q6,Q5 from PDTC144EU,Philips to DTC144EUA,ROHM for simply BOM
P28 change Q17 from PDTC144EU,Philips to DTC144EUA,ROHM for simply BOM
P46 change Q23 from PDTC144EU,Philips to DTC144EUA,ROHM for simply BOM
P32 change CAP5 from Panasonic,EEFSX0D331ER to NEC,330U_2.5V_M for simply BOM
P5  change CAP8 from Panasonic,EEFSX0D331ER to NEC,330U_2.5V_M for simply BOM
P11 change CAP11 from Panasonic,EEFSX0D331ER to NEC,330U_2.5V_M for simply BOM

0518
P35,P54,P34 change U50,U51,U53 to 74LVC1G08GW,Philips,


PVT
0607
P63 delete c606 ,PCLK_FWH,and connect PCLK_CB to R590 pin1 for separate PCLK_MINI
P36 change CN12 pin 16 PCLK_FWH to test pad TP251
P62 mount PC92 for VGA voltage switch
P50 update CN20 footprint for SMT hand mount

0609
P63 dummy R602 for TV issue
P62 change PR4 to 5.1K_F for VGA timing
P60 change PR436 to 20K_J for VGA timing
P35 add R1745 for protect U3 pin 48

0612
P64 (1)H3,H4,H5,H6,H11 don't connect to GND
    (2)add EC45~48 for EMI
P60 add PR448,PR449,PQ88,PQ89 for +3VRUN_TV and +5VRUN_TV discharge circuit

0614
P62 change PC92 from Y5V to X5R

P57 update PL4,PL5 footprint
P59 update PL1,PL3 footprint
P60 update PL14 footprint

P56 update PL7,Pl8 vendor P/N and value
P58 update PL9 vendor P/N and value
P60 update PL6 vendor P/N and value
P62 update PL2 vendor P/N and value

0615
P24 mount C809,C810 for Hynix warm boot fail
P61 dummy PR214,PR215,PD37 for disable DC_IN OVP Protection
P30,48 change R761,R762,R763,R374 from 39ohm to 22ohm for MDC SI test fail
P39 Change F2,F5 from 1M-F32V1A0-F000 to 1M-F32V1A5 -F0000
P38,64 Change F4,F6,F11 from 1M-F32V0A5-F000 to  1M-F32V1A0-F000


MP
0621
P41 add TP252,TP253,TP254,TP255 for audio power test

0623
P48 Del TB39,TB40
P43 Change C800 size from 1206 to 0805

0625
P61 Change PR215 from NC to 0 ohm

0627
P64 Change H20 dimension
P44 change C237,C243,C244,C245 from 1C-2B30682-M000 to 1C-2B30682-K000

0629
P41 add TP256 for audio test

0701
P23 dummy R501,R513,R517 for disable CRT function
P65 dummy R455,R456,R497,R498,R504,R511,R522,CN26 for disable CRT function

0703
P48 Correct CN32 Vender PN as YAMAICHI_JCS010-2004
P64 add R1749 for SMK S4/S5 issue

MS51S DVT
0710
P60 change PR170 from 1K to 3.3K, change PC131 from 0.1uF to 0.47uF for power drop issue
    change PR41 from 10K to 4.7K for RUN power timing shift

P17 populate R40,R472,R36,R446
    dummy R473,R19,R445,R15 for G73M Infineon(16Mx32bit) VRAM

P24,25 change VRAM to Infineon 512M/16Mx32bit, 13-HYB18H5-3001
P64 dummy R1749

0727
Vender's suggestion to modify G73M circuit
P20 dummy R563,R564,R1413,Q34,C572
P24,25 dummy R184,R176,R181,R160,R179,R177,R172,R159,R1737,R104,R109,R103,R86,R150,
       R153,R149,R131,R1739
P22 change R1422,R1406 from 10K to 2K,
   1R-0000202-J200, SMD,RES,2K,1/16W,5%,0402
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