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PCB P/N: 1P-0075503-6010  
1P-0075103-6010

Project Code & Schematics Subject: M620 Main Board

Value	M620GM	M620GML
NC_		

P. Leader	Check by	Design by

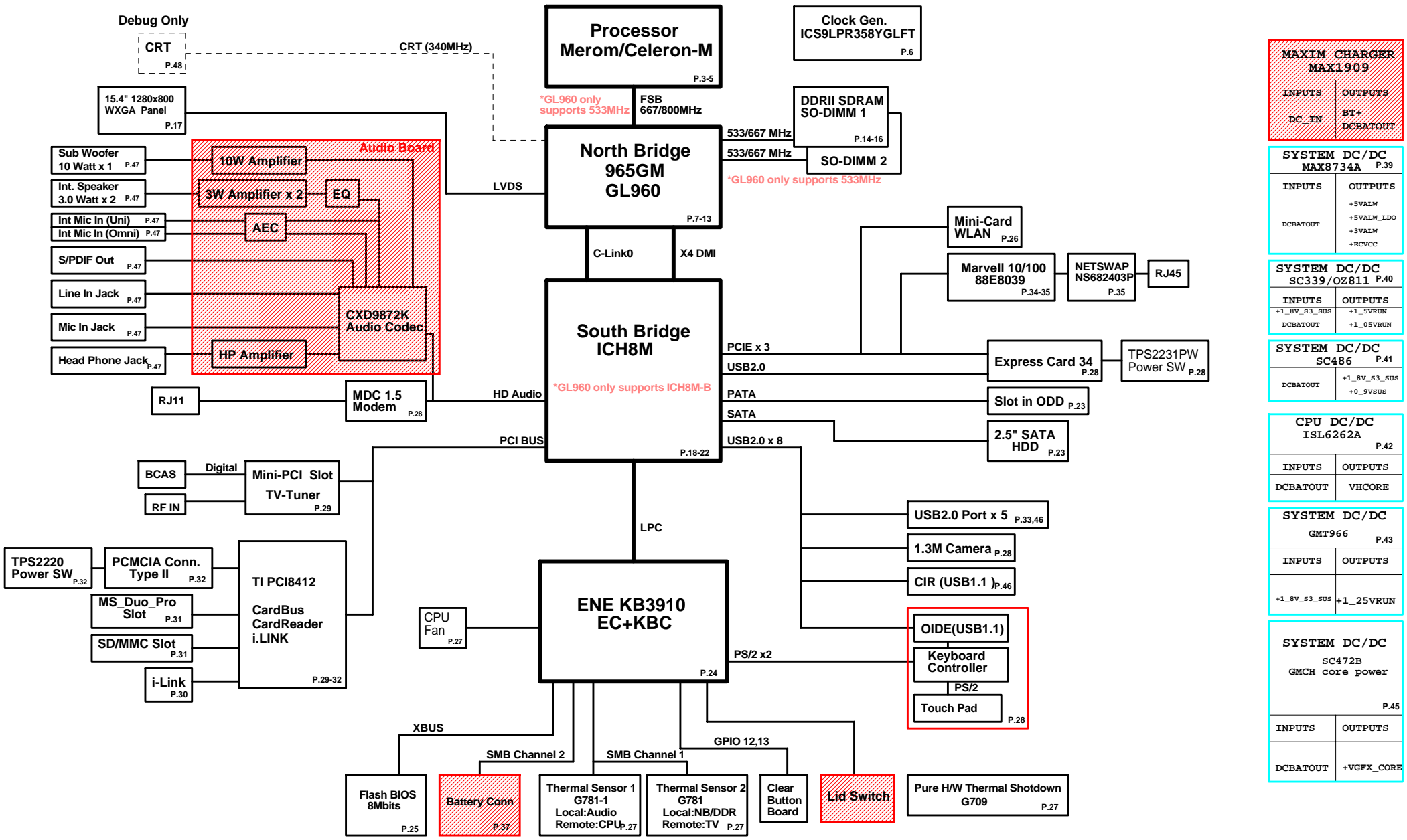
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# MBX-178 M620 Block Diagram (15.4" Wide Screen)



MAXIM CHARGER MAX1909	
INPUTS	OUTPUTS
DC_IN	BT+
	DCBATOUT

SYSTEM DC/DC MAX8734A P.39	
INPUTS	OUTPUTS
DCBATOUT	+5VALW
	+5VALW_LDO
	+3VALW
	+BCVCC

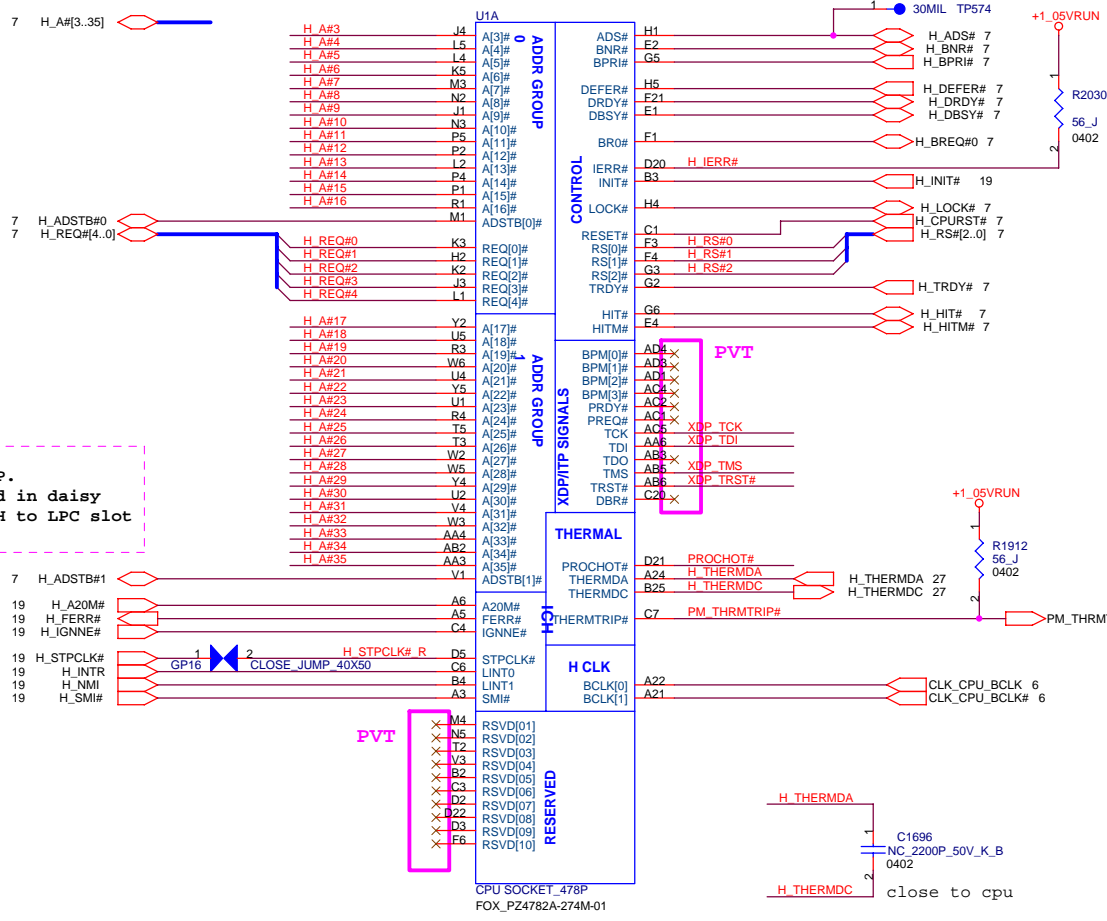
SYSTEM DC/DC SC339/OZ811 P.40	
INPUTS	OUTPUTS
+1.8V_S3_SUS	+1_SVRUN
DCBATOUT	+1_0SVRUN

SYSTEM DC/DC SC486 P.41	
INPUTS	OUTPUTS
DCBATOUT	+1.8V_S3_SUS
	+0_9VSUS

CPU DC/DC ISL6262A P.42	
INPUTS	OUTPUTS
DCBATOUT	VHORE

SYSTEM DC/DC GMT966 P.43	
INPUTS	OUTPUTS
+1.8V_S3_SUS	+1_25VRUN

SYSTEM DC/DC SC472B GMCH core power P.45	
INPUTS	OUTPUTS
DCBATOUT	+VGF_X_CORE

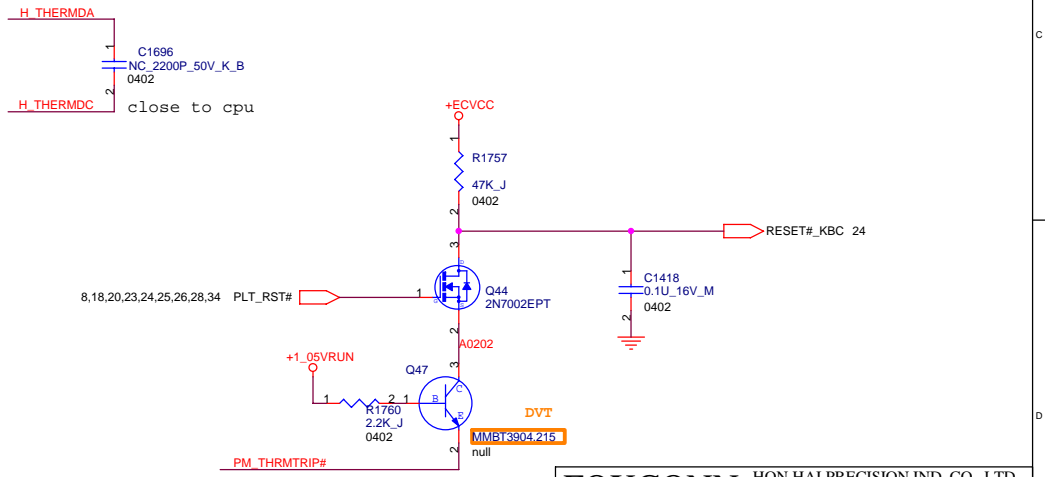
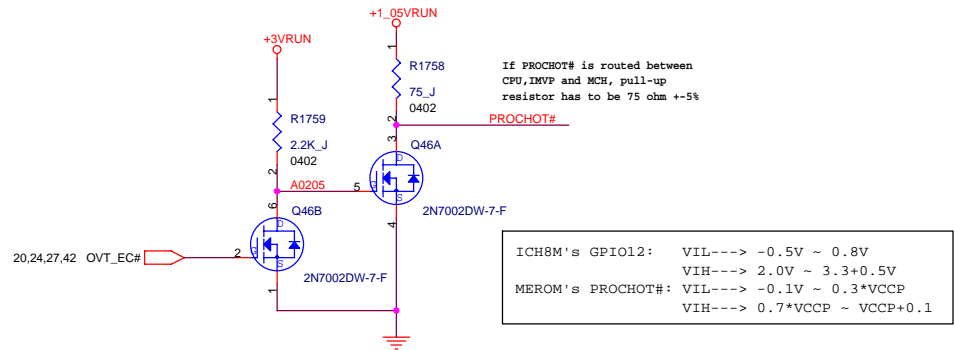


Layout note:  
no stub on H\_STPCLK TP.  
H\_STPCLK# to be routed in daisy chain fashion from ICH to LPC slot and then to CPU.

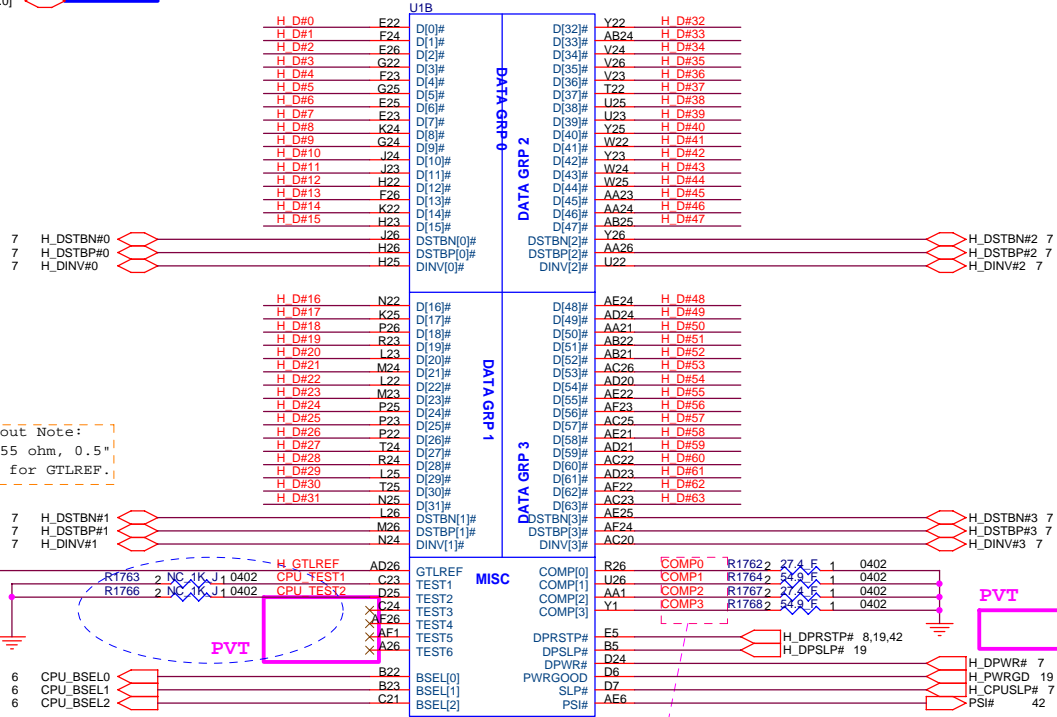
Layout note:  
no stub on H\_STPCLK#

Debug port not used .  
resistors close to CPU.

PM\_THRMTRIP#  
should connect to ICH8-M and GMCH without T-ing (No stub)

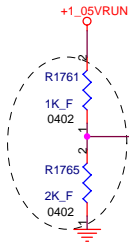


7 H\_D#[63..0]



Layout Note:  
Zo=55 ohm, 0.5"  
max for GTLREF.

Place close to CPU

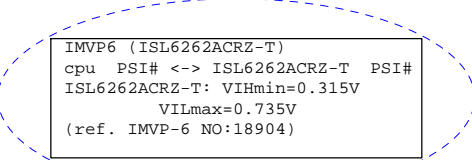


7 H\_DSTBN#1  
7 H\_DSTBP#1  
7 H\_DINV#1

6 CPU\_BSEL0  
6 CPU\_BSEL1  
6 CPU\_BSEL2

Layout Note:  
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5".  
Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5".

Layout:  
Connect test point with no stub



**FSB Frequency Table:**

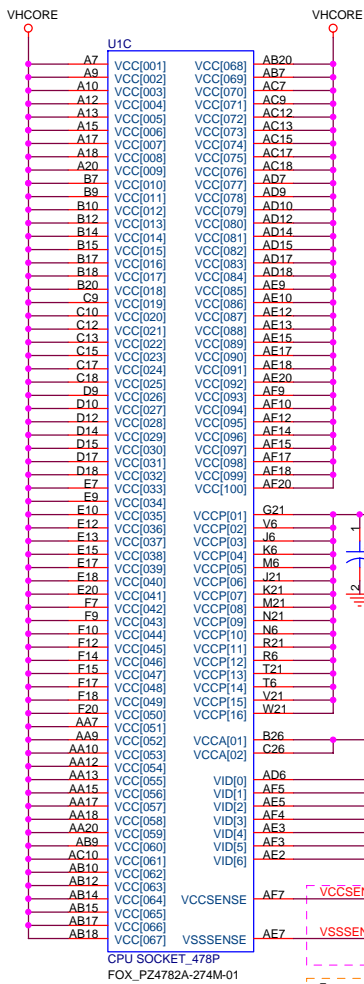
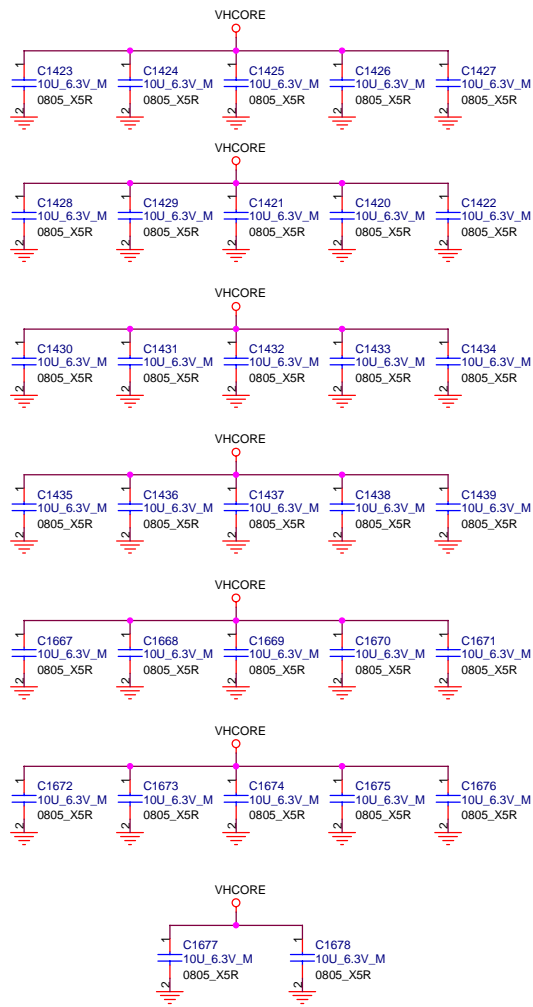
BSEL[2:0]	Freq.(MHz)
LLL	266MHz
LLH	133MHz
LHH	166MHz
LHL	200MHz
HHL	400MHz
HHH	Reserve
H LH	100MHz
H LL	333MHz

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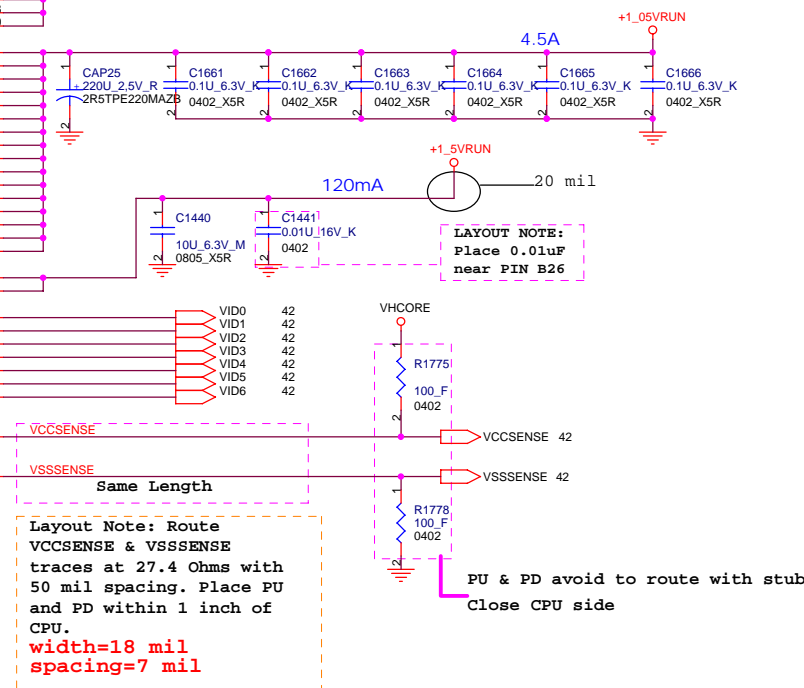
Title **Merom (HOST BUS) 2/3**

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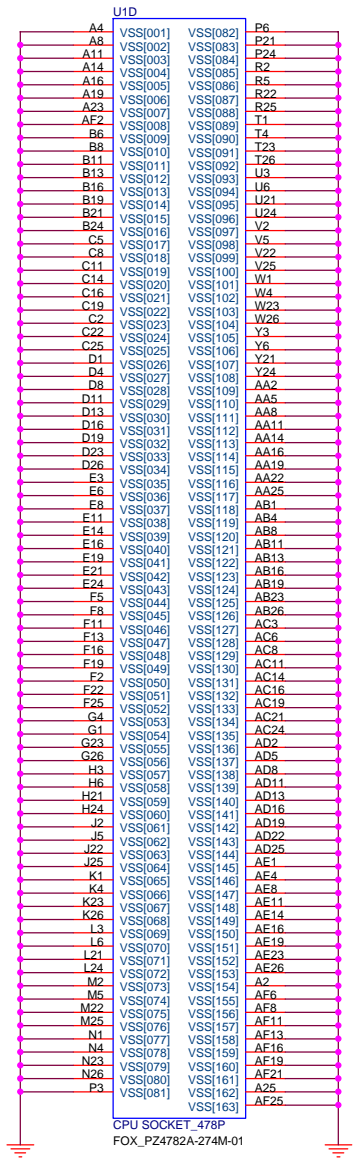


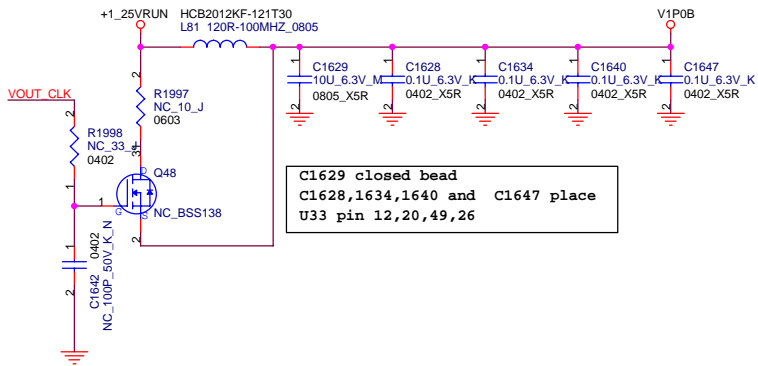
CPU\_VCCA---->120mA  
 CPU\_VCCP----->4.5A  
 CPU\_VCC----->44A



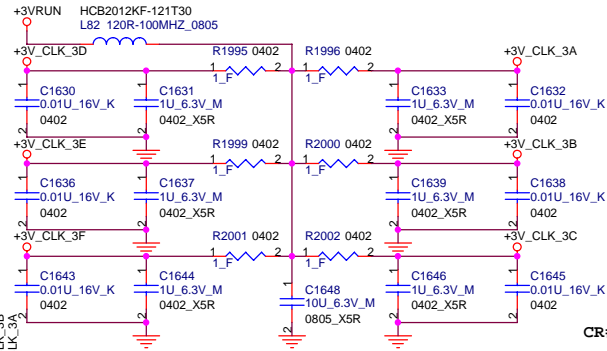
LAYOUT NOTE:  
 Place 0.01uF  
 near PIN B26

Layout Note: Route  
 VCCSENSE & VSSSENSE  
 traces at 27.4 Ohms with  
 50 mil spacing. Place PU  
 and PD within 1 inch of  
 CPU.  
 width=18 mil  
 spacing=7 mil





C1629 closed bead  
C1628,1634,1640 and C1647 place  
U33 pin 12,20,49,26



C1633,1639,1646 closed Resistor  
Then C1632,1638,1645 closed 1uF

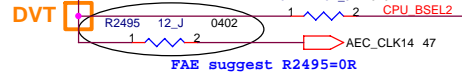
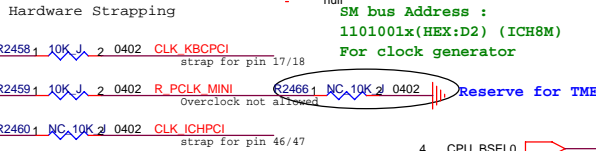
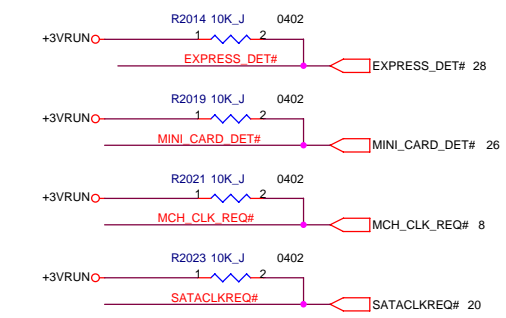
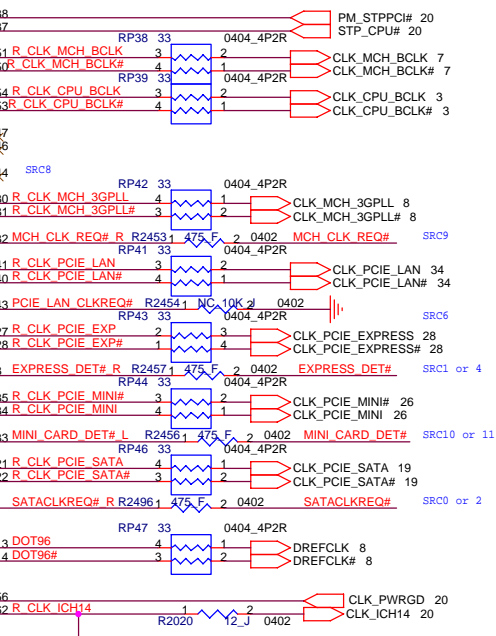
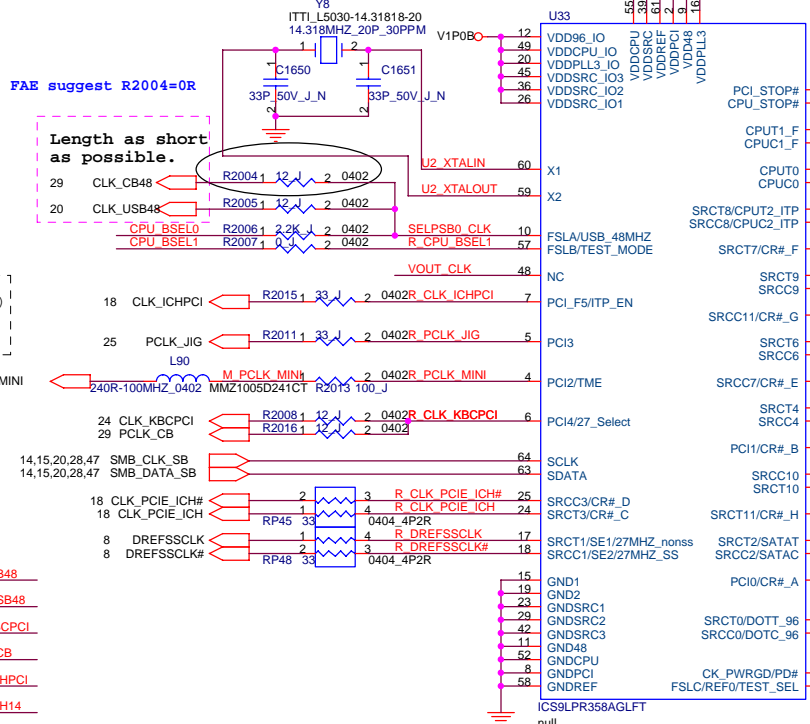
CR#\_E/F/G/H pins control SRC output Table

CR#\_E:Byte6:bit7=0, disable CR#\_E; 1, enable CR#\_E SRC6  
CR#\_F:Byte6:bit6=0, disable CR#\_F; 1, enable CR#\_F SRC8  
CR#\_G:Byte6:bit5=0, disable CR#\_G; 1, enable CR#\_G SRC9  
CR#\_H:Byte6:bit4=0, disable CR#\_H; 1, enable CR#\_H SRC10

FAE suggest R2004=0R

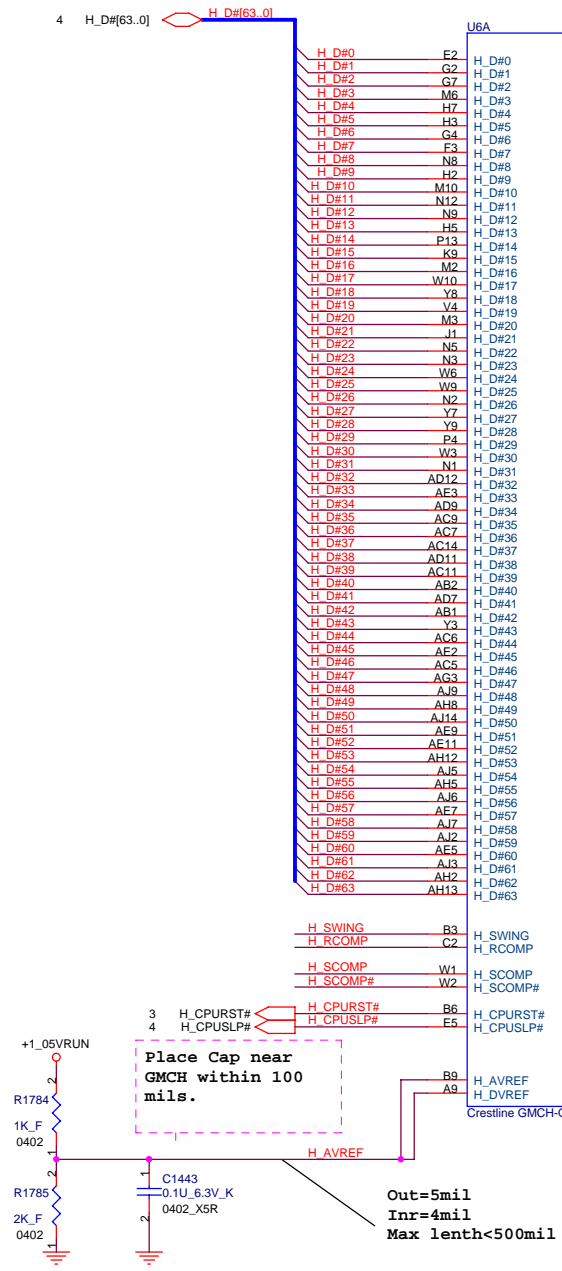
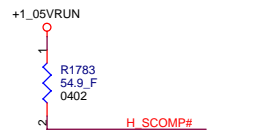
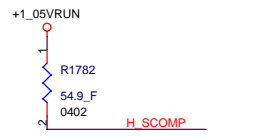
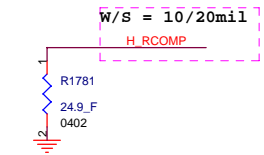
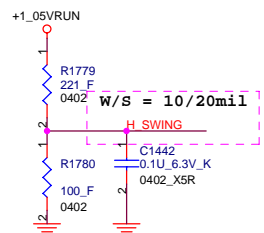
Length as short as possible.

Dual mode of PCI clock (pin3,4,6,7) should link to on-board device.



**FSB Frequency Table:**

FSLC	FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	0	266.66	100	33
0	0	1	133.33	100	33
0	1	0	200	100	33
0	1	1	166.66	100	33
1	0	0	333.33	100	33
1	0	1	100	100	33
1	1	0	400	100	33



HOST

GM965=12-CRESTL1-ES03  
 GL960=12-CRESTL1-ES04

Notes:  
 CFG[17:3] = Internal Pull-ups  
 CFG[19:18] = Internal Pull-downs

MCH_CFG_[2:0] (FSB Frequency)	[2:0] = 010 = 800MT/s [2:0] = 011 = 667MT/s [2:0] = 001 = 533MT/s
MCH_CFG_5 (DMI Type)	Low = DMIX2 High = DMIX4 (Default)
MCH_CFG_7 (Intel Management Engine Crypto Strap)	Low = Intel Management Engine Crypto Transport Layer Security (TLS cipher suite with no confidentiality) High = Intel Management Engine Crypto TLS cipher suite with confidentiality(Default)
MCH_CFG_9 (PCIe Graphics Lane)	Low = Reverse Lane High = Normal operation (Default)
MCH_CFG_[13:12] (Test Mode Type)	[13:12] = 11 = Normal Operating (Default) [13:12] = 10 = All Z Mode [13:12] = 01 = XOR Mode [13:12] = 00 = Reserved
MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable (Default)
MCH_CFG_19 (DMI Lane Reversal)	Low = Normal operation (Default) High = Lane Reversed
MCH_CFG_20 (Concurrent SDVO/PCIe)	Low = Only SDVO or PCIe is operational (Default) High = SDVO & PCIe operate simultaneously through the PCI Express Graphics attach port

- × P36 RSV21
- × P37 RSV22
- × R35 RSV23
- × N35 RSV24
- × AR12 RSV25
- × AR12 RSV26
- × AM12 RSV27
- × AN13 RSV28
- × J12 RSV29
- × AR37 RSV30
- × AM36 RSV31
- × AL36 RSV32
- × AM37 RSV33
- × D20 RSV34
- × H10 RSV20
- × B51 RSV21
- × BJ20 RSV22
- × BK22 RSV23
- × BF19 RSV24
- × BH20 RSV25
- × BK18 RSV26
- × BJ18 RSV27
- × BF23 RSV28
- × BG23 RSV29
- × BC23 RSV30
- × BD24 RSV31
- × BJ29 RSV32
- × BE24 RSV33
- × BH39 RSV34
- × AW20 RSV35
- × BK20 RSV36
- × C48 LVDSA\_DATA#3
- × D47 LVDSA\_DATA#3
- × B44 RSV40
- × C44 RSV41
- × A35 RSV42
- × B37 RSV43
- × B36 RSV44
- × B34 RSV45
- × C34 RSV46

14,16 M\_A A14  
 15,16 M\_B A14

- 6 MCH\_BSEL0
- 6 MCH\_BSEL1
- 6 MCH\_BSEL2
- TP318 30MIL 1 MCH CFG 3
- TP319 30MIL 1 MCH CFG 4
- TP347 30MIL 1 MCH CFG 5
- TP575 30MIL 1 MCH CFG 6
- TP576 30MIL 1 MCH CFG 7
- TP602 30MIL 1 MCH CFG 8
- TP577 30MIL 1 MCH CFG 9
- TP578 30MIL 1 MCH CFG 10
- TP579 30MIL 1 MCH CFG 11
- TP321 30MIL 1 MCH CFG 12
- TP322 30MIL 1 MCH CFG 13
- TP580 30MIL 1 MCH CFG 14
- TP320 30MIL 1 MCH CFG 15
- TP354 30MIL 1 MCH CFG 16
- TP323 30MIL 1 MCH CFG 17
- TP348 30MIL 1 MCH CFG 18
- TP581 30MIL 1 MCH CFG 19
- TP582 30MIL 1 MCH CFG 20
- CFG0
- CFG1
- CFG2
- CFG3
- CFG4
- CFG5
- CFG6
- CFG7
- CFG8
- CFG9
- CFG10
- CFG11
- CFG12
- CFG13
- CFG14
- CFG15
- CFG16
- CFG17
- CFG18
- CFG19
- CFG20
- G41
- L39
- L36
- J36
- AW49
- AV20
- N20
- G36

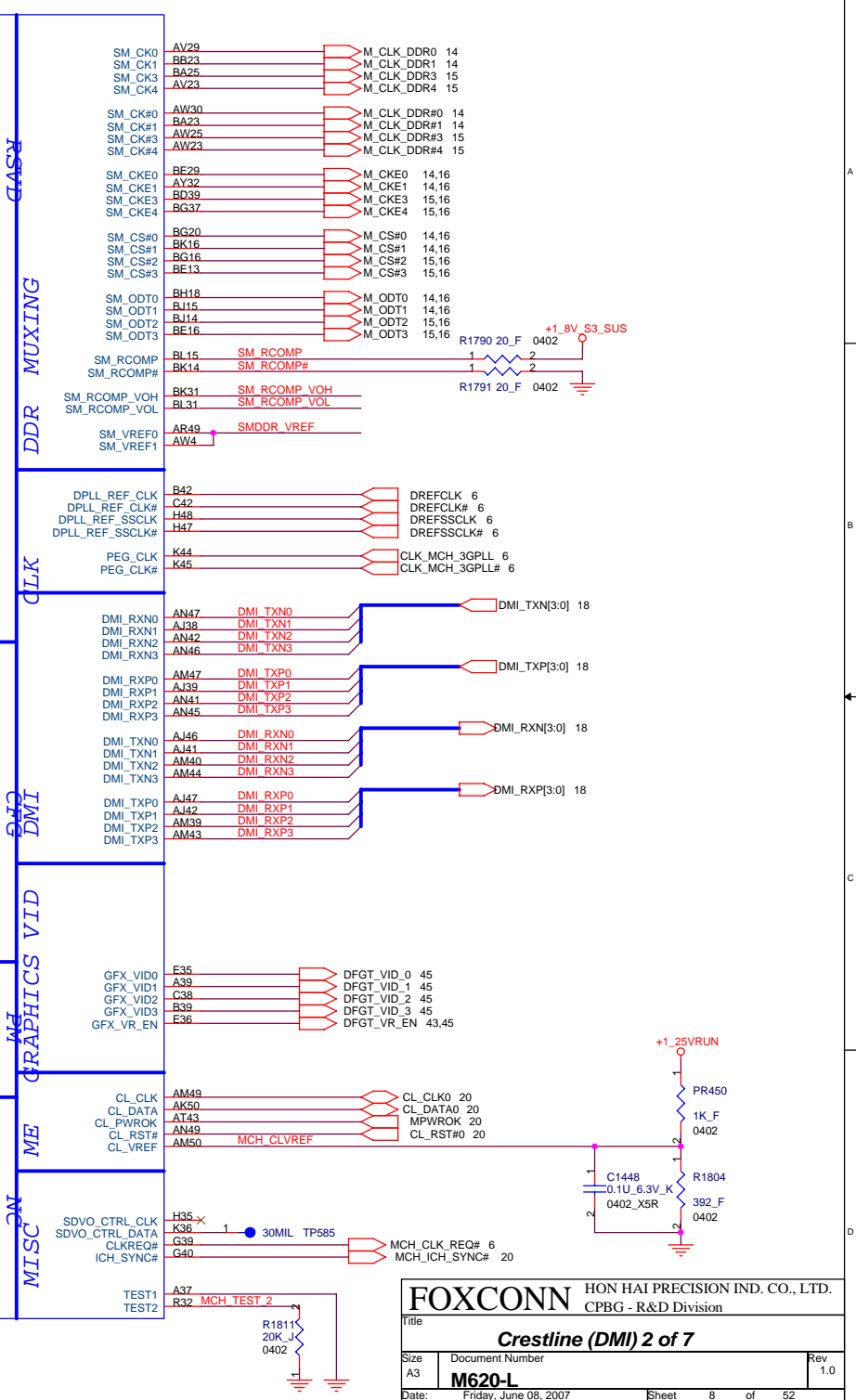
CFG[17:3] Internal Pull-up  
 CFG[20:18] Internal Pull-down

- 20 PM\_BM\_BUSY#
- 4,19,42 H\_DPRSTP#
- 14 PM\_EXTTS#0
- 15 PM\_EXTTS#1
- 20,24 IMVP\_PWRGD
- 3,18,20,23,24,25,26,28,34 PLT\_RST#
- 3,19 PM\_THRMTRIP#
- 20,42 DPRSLPVR
- G41
- L39
- L36
- J36
- AW49
- AV20
- N20
- G36

DVT

- × BJ51 NC1
- × BK51 NC2
- × BK50 NC3
- × BL50 NC4
- × BL49 NC5
- × BL2 NC6
- × BL2 NC7
- × BK1 NC8
- × BJ1 NC9
- × E11 NC10
- × A5 NC11
- × C51 NC12
- × B50 NC13
- × A50 NC14
- × A49 NC15
- × BK2 NC16

Crestline GMCH-QN12\_ES2



Place C1453 close C1452

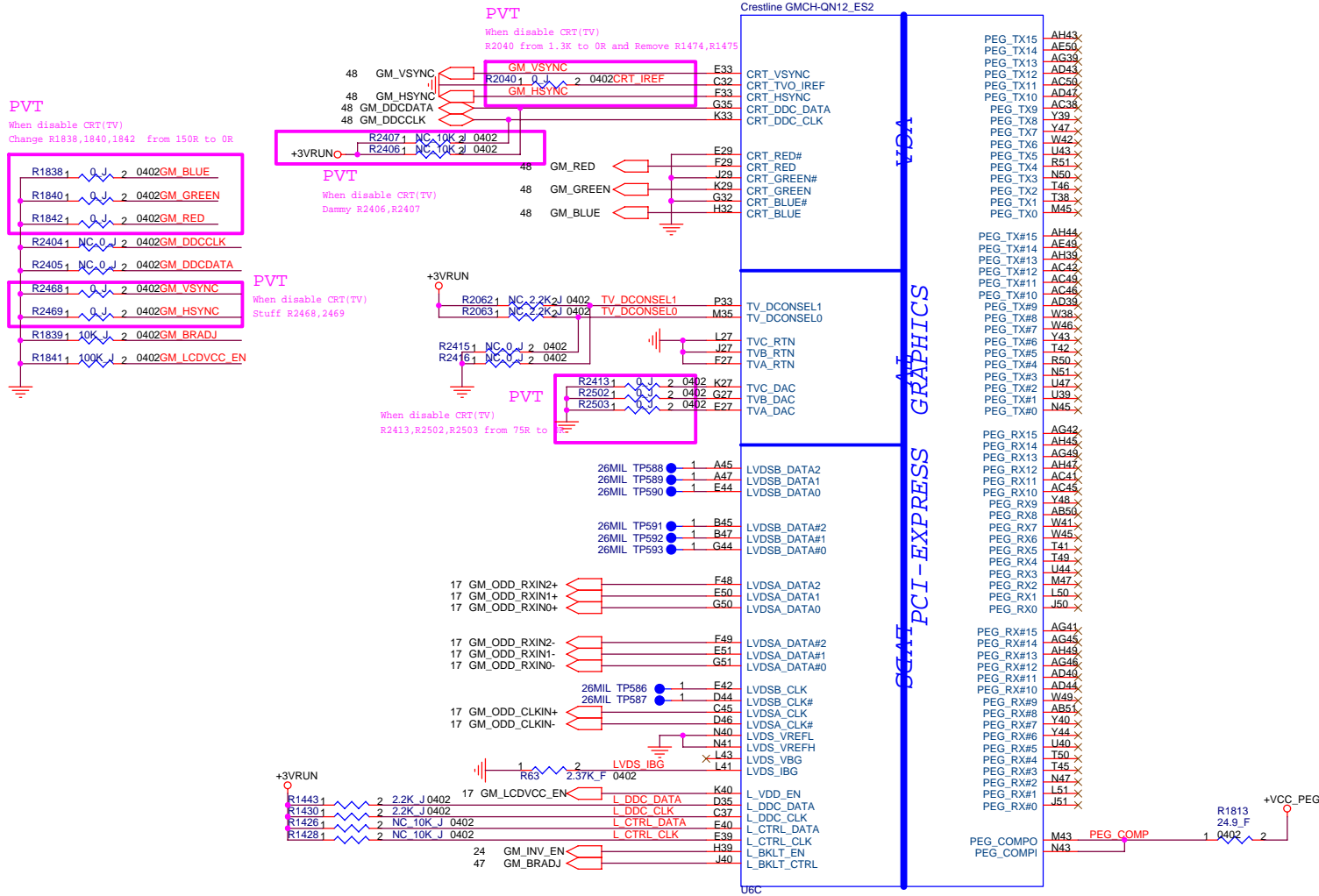
DVT

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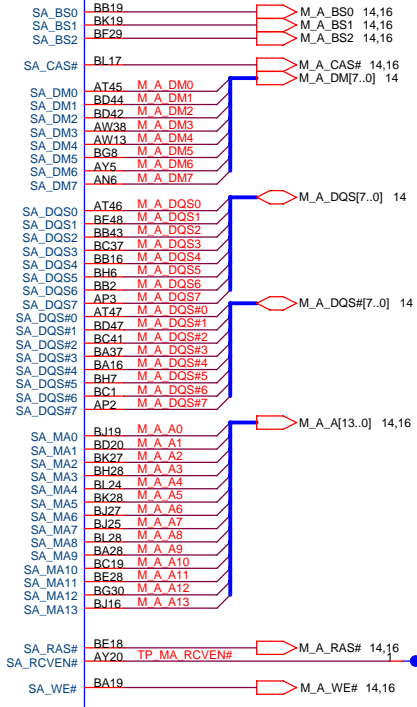




14 M\_A\_DQ[63..0]



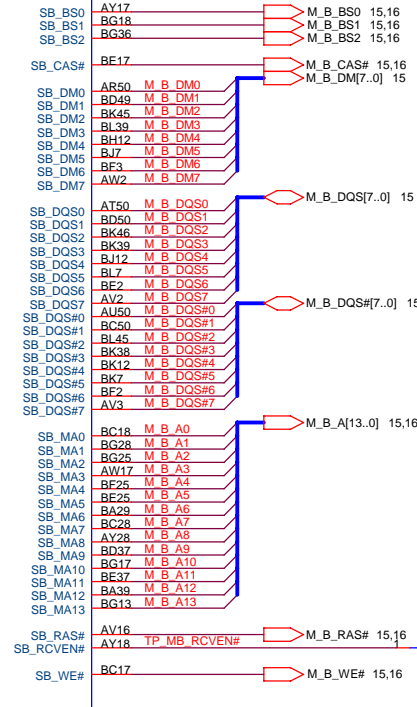
DDR SYSTEM MEMORY A



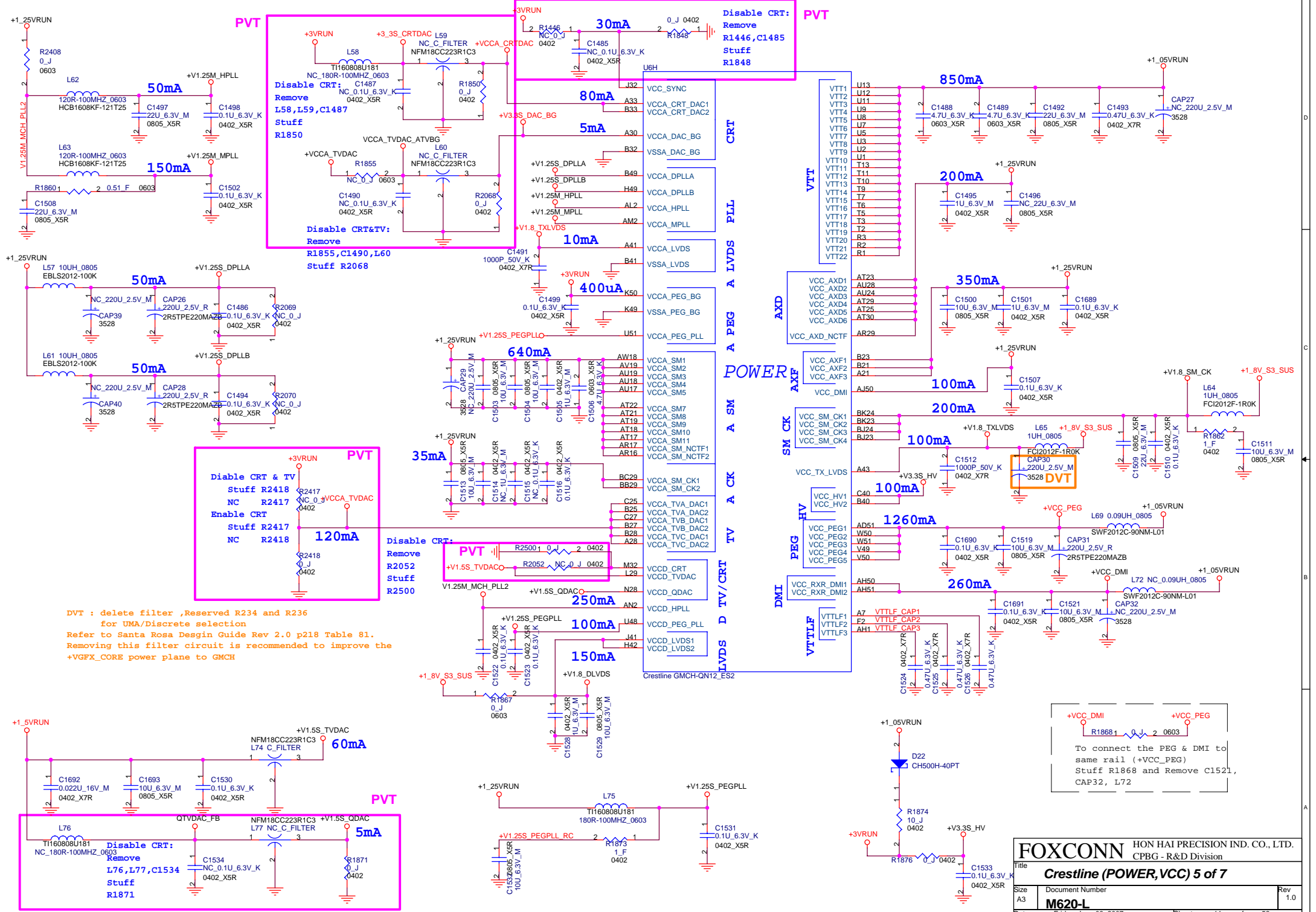
15 M\_B\_DQ[63..0]



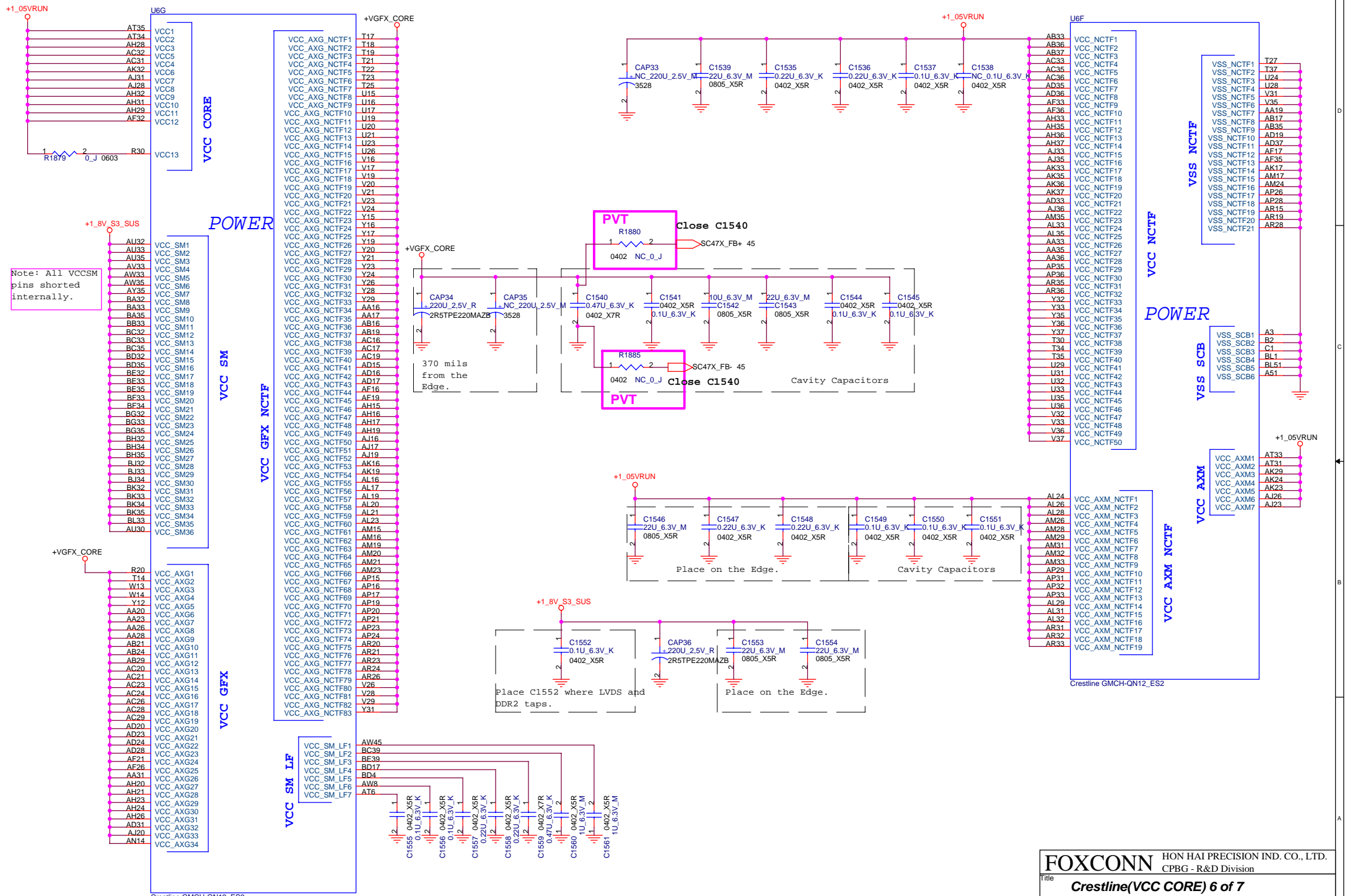
DDR SYSTEM MEMORY B



30MIL TP344

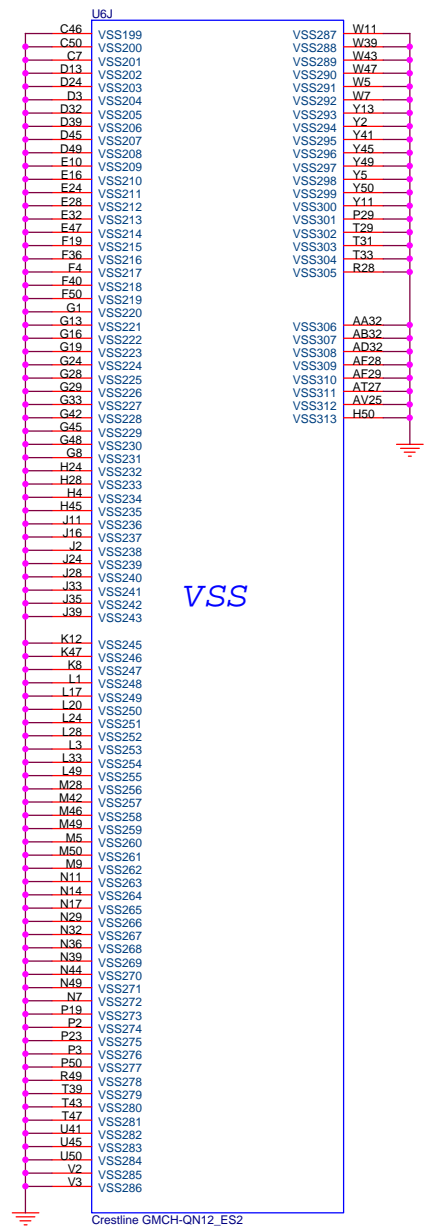
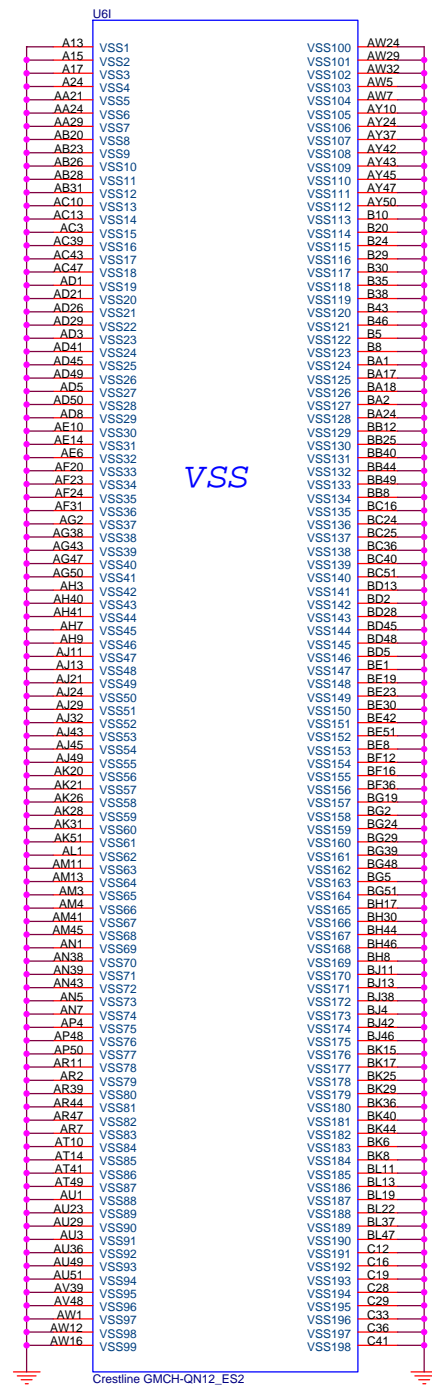


To connect the PEG & DMI to same rail (+VCC\_PEG) Stuff R1868 and Remove C1521, CAP32, L72

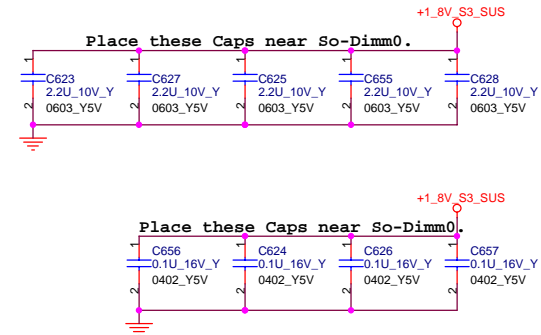
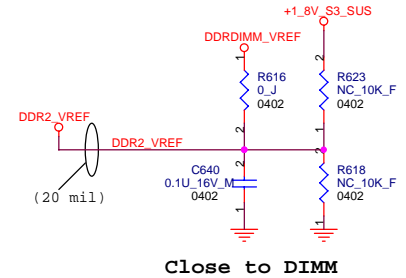
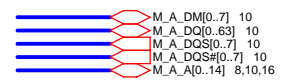
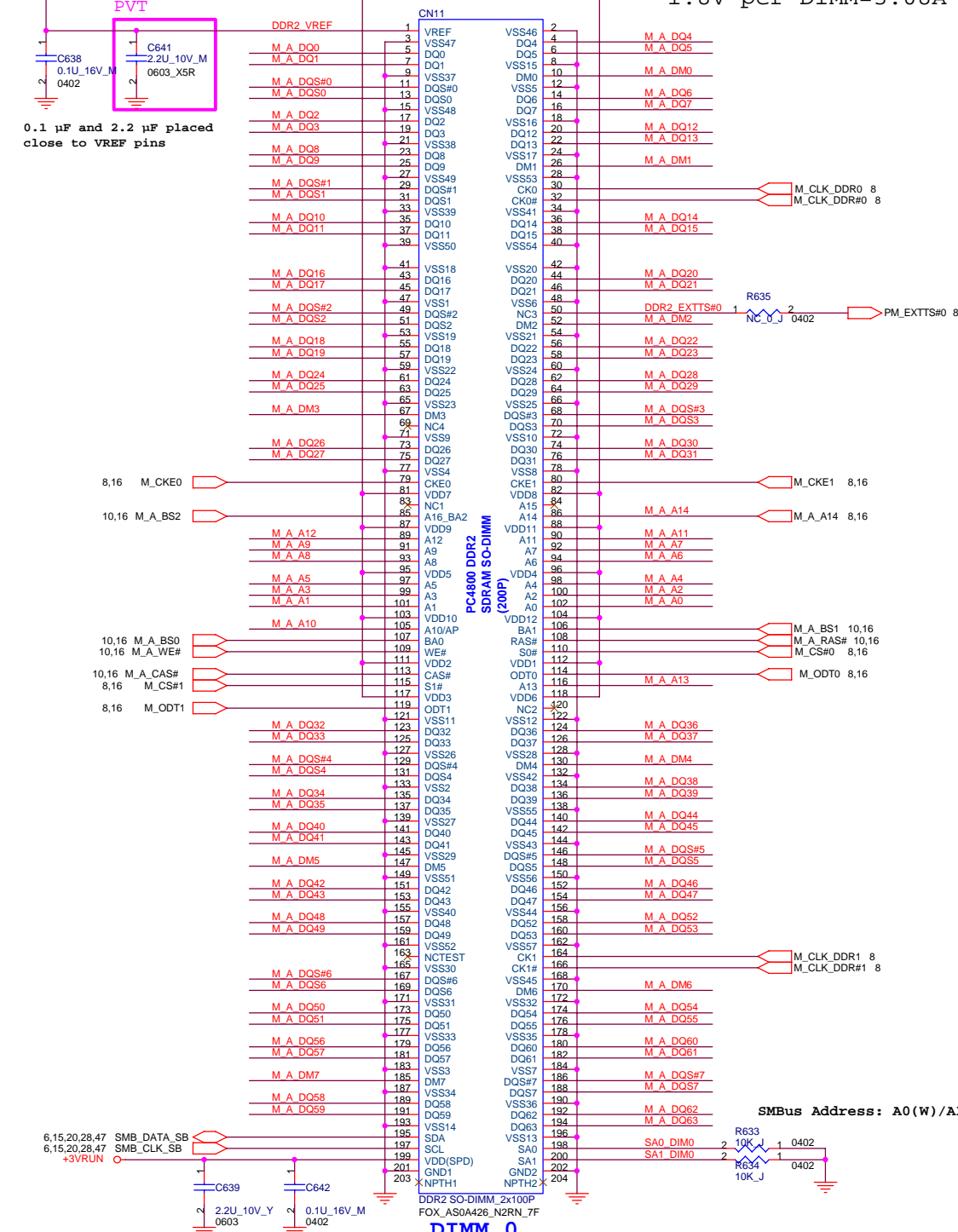


Crestline GMCH-QN12\_ES2

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Title <b>Crestline(VCC CORE) 6 of 7</b>			
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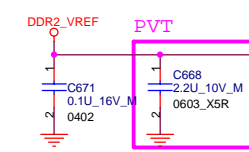


DDR2\_VREF +1.8V\_S3\_SUS +1.8V\_S3\_SUS 1.8V per DIMM=3.08A

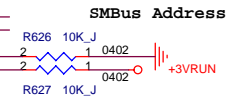
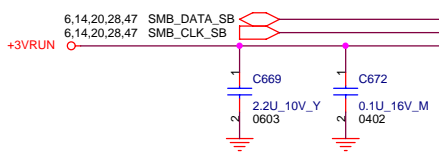
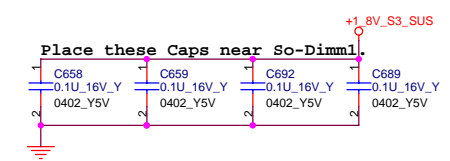
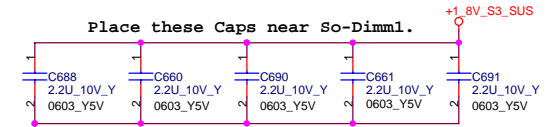
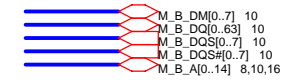
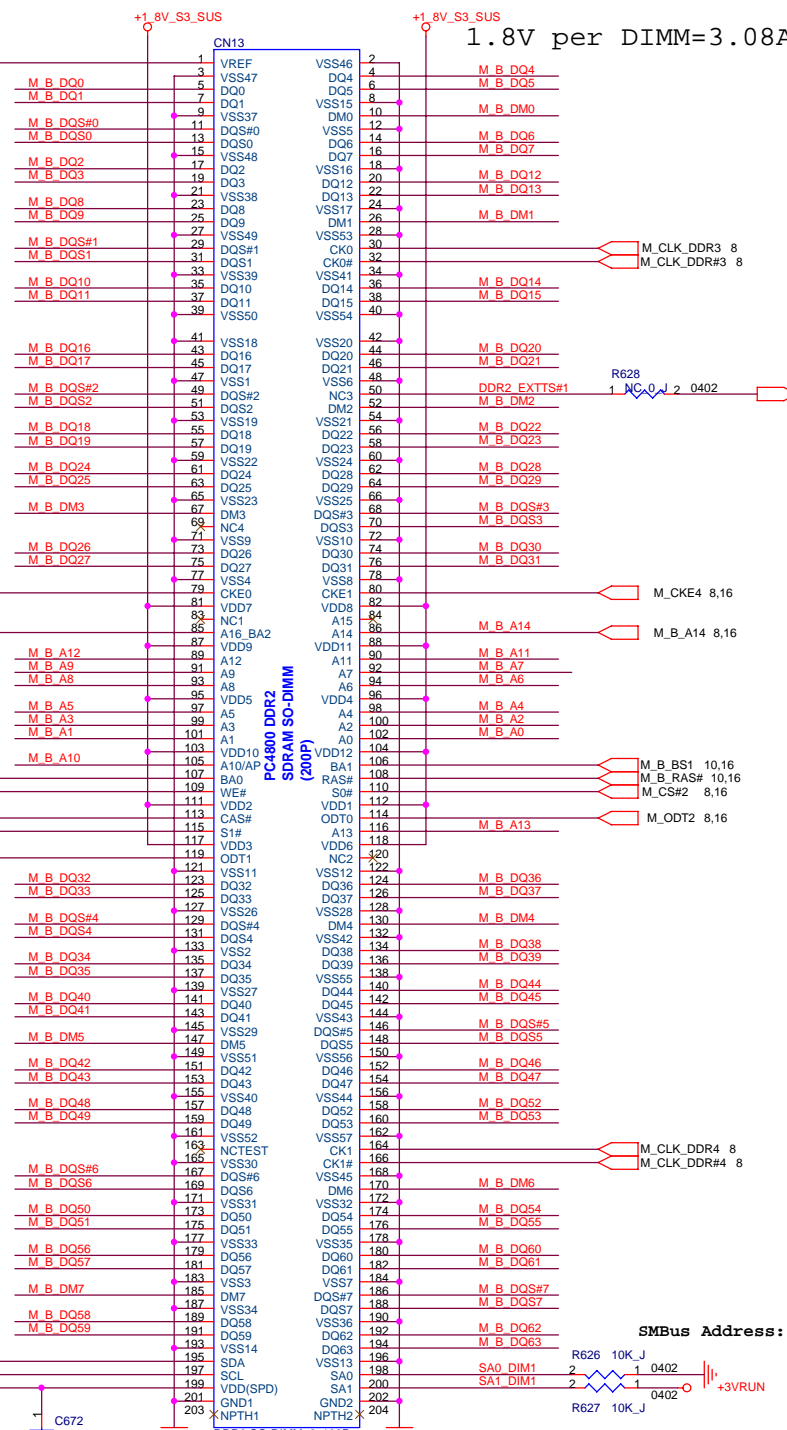


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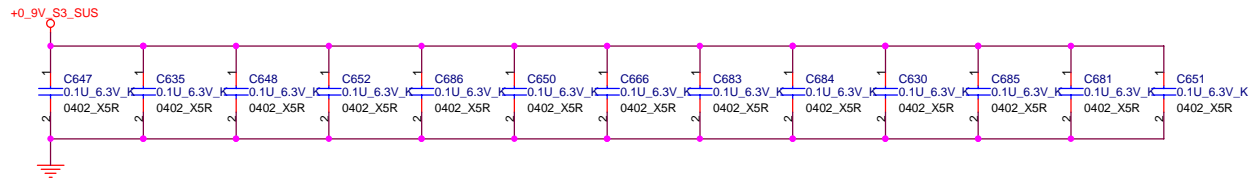
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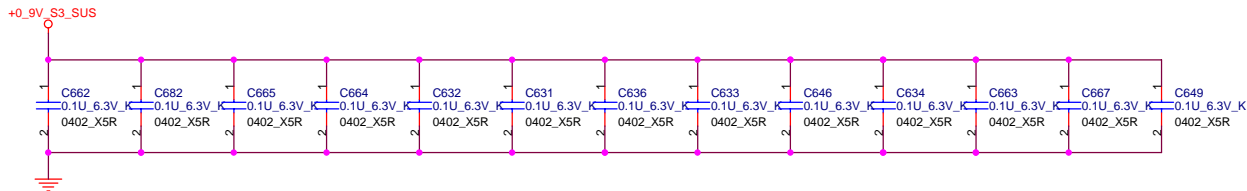
0.1  $\mu$ F and 2.2  $\mu$ F placed close to VREF pins



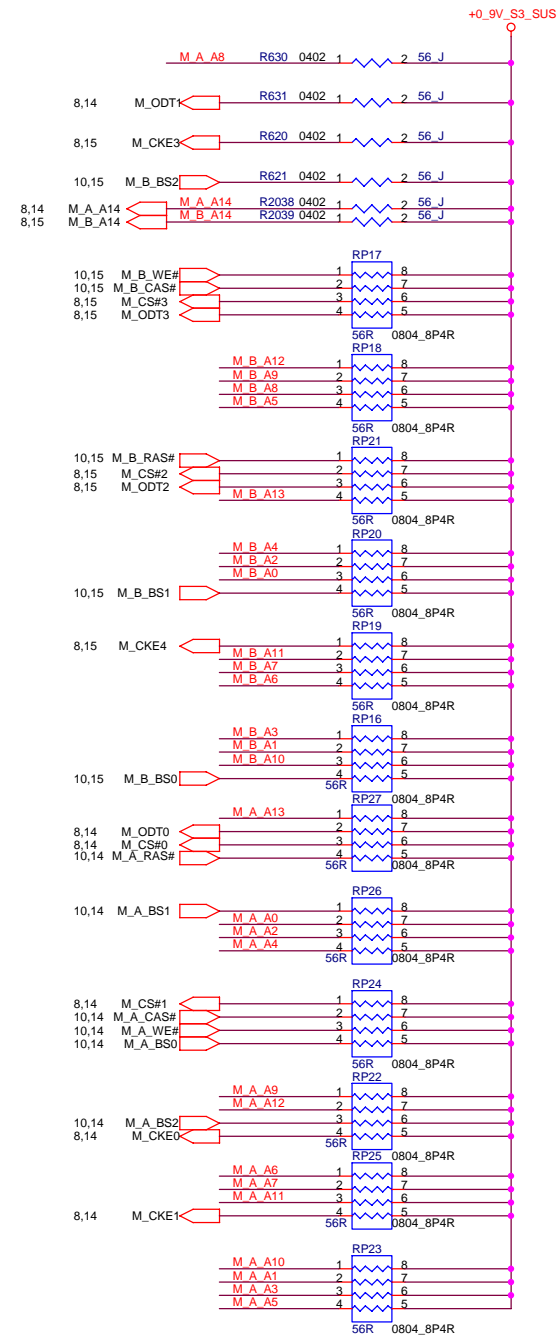
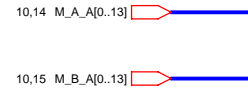
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15	52



Layout note: Place 1 cap close to every 1 R-pack terminated to +0.9V\_S3\_SUS

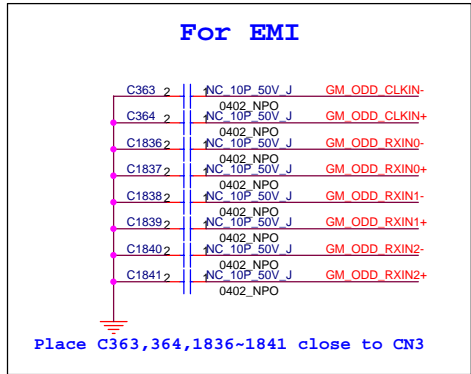
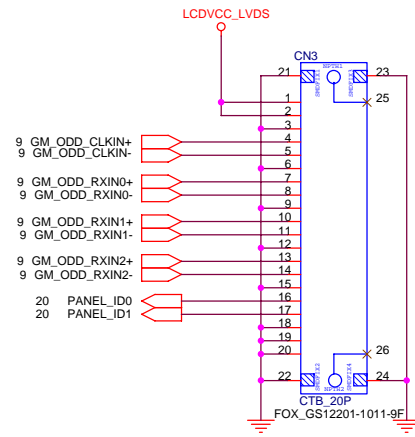


Layout note: Place 1 cap close to every 1 R-pack terminated to +0.9V\_S3\_SUS



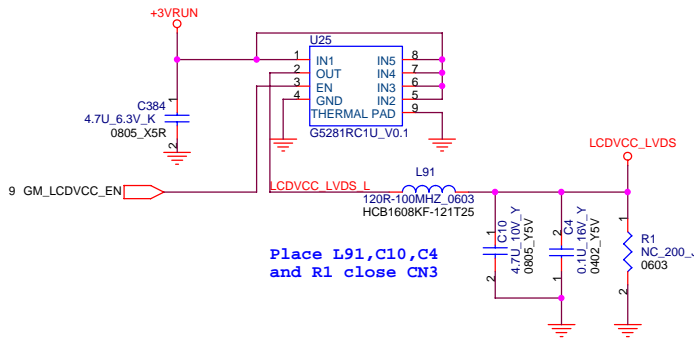


# LVDS CONNECTOR



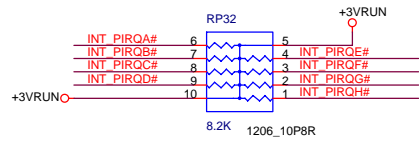
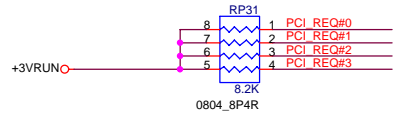
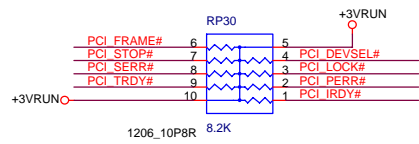
Cable ID(1:0)	0	0	1	1	0	1	1
Vendor	CPT						
Type							
Model Name	CLAA154WA05AN						
Size	15.4"	15.4"	15.4"	15.4"	15.4"	15.4"	15.4"

# LCD POWER

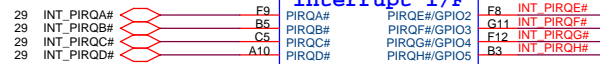
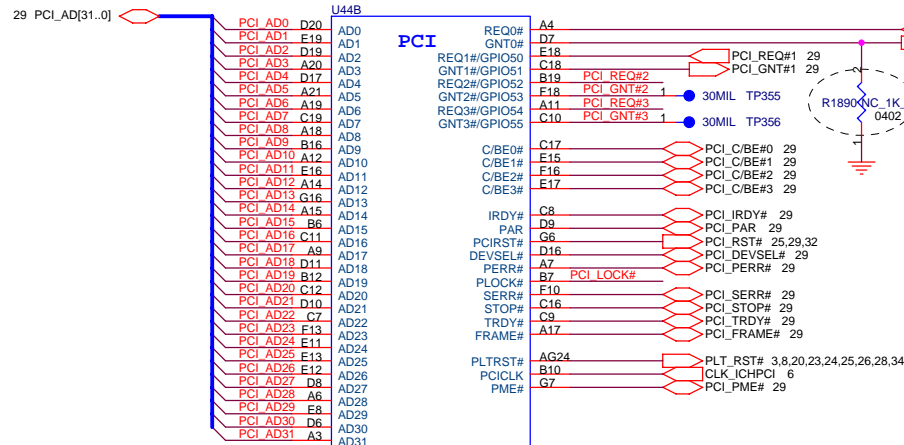


DISCHARGE  
DISCHARGE

The R1 will consume about 0.054 Watt (3.3x3.3/200 = 0.054W). We changed resistor to 0603 size (1/8 Watt)



PCI Pullups



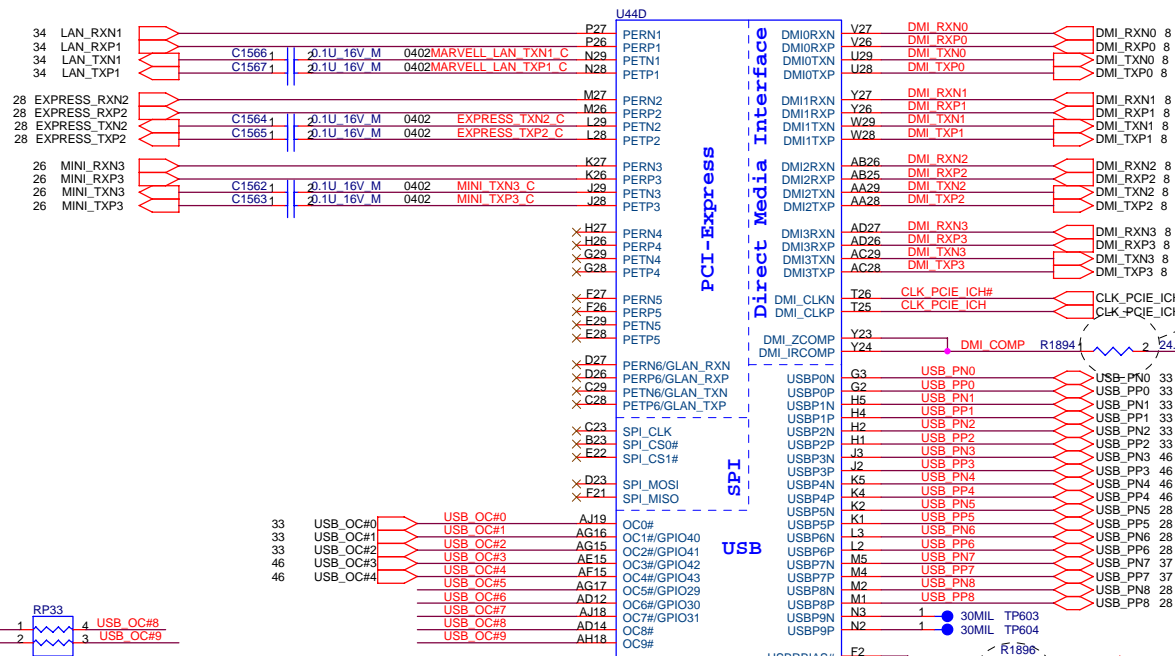
Interrupt I/F

ICH8M-QM73\_ES1  
null

For SPI Boot BIOS Selection.  
(Need to tune the resistor value)

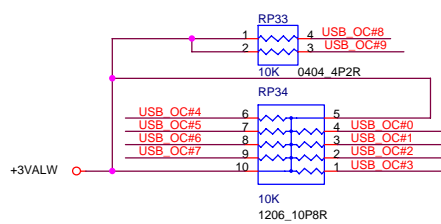
Strap for Boot-BIOS

	GNT0#	SPI_CS1#
LPC(Default)	Hi	Hi
PCI	Hi	LOW
SPI	LOW	Hi



Place within 500 mils of ICH

USB PORT	Function
PORT-0	REAR-1
PORT-1	REAR-2
PORT-2	REAR-3
PORT-3	SIDE-1
PORT-4	SIDE-2
PORT-5	EXPRESS CARD
PORT-6	CAMERA
PORT-7	CIR
PORT-8	OIDE
PORT-9	NC



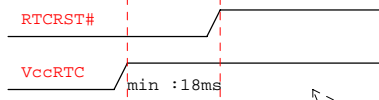
Place within 500 mils of ICH and don't routing next to high speed signals

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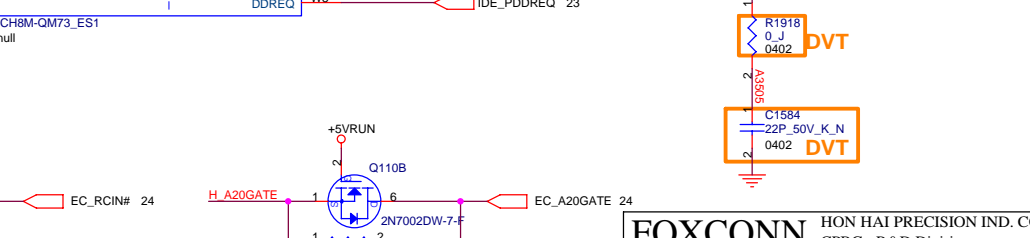
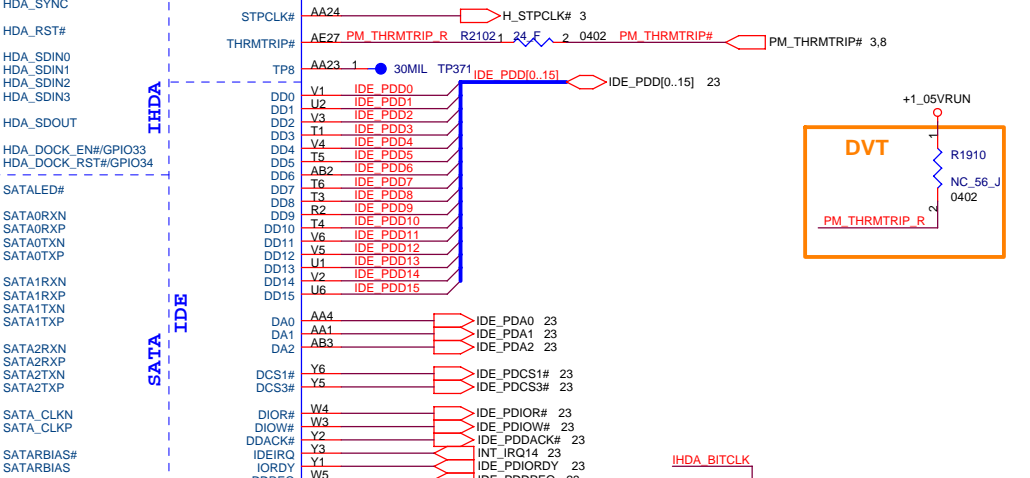
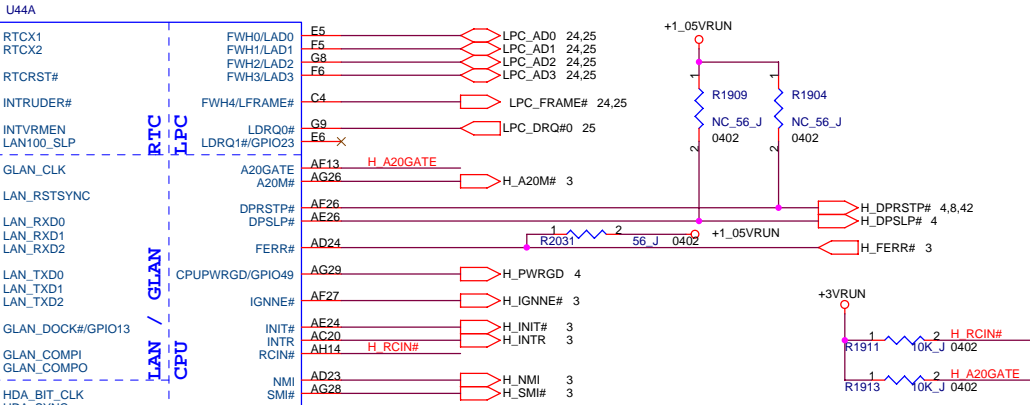
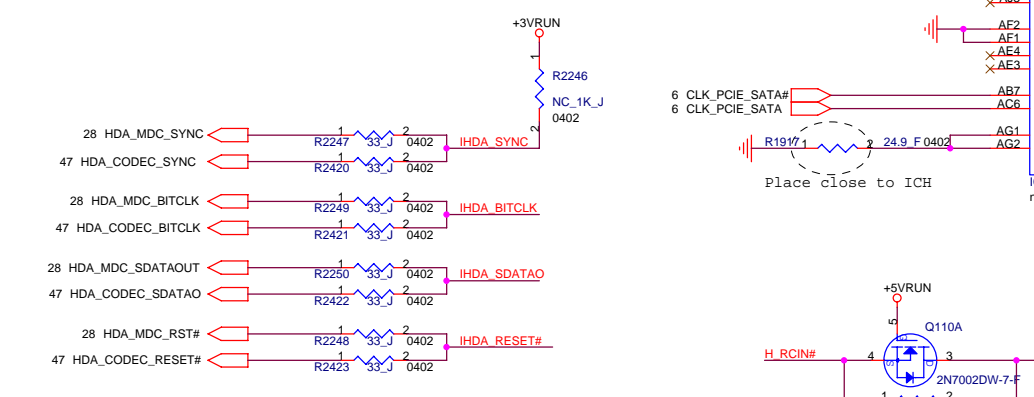
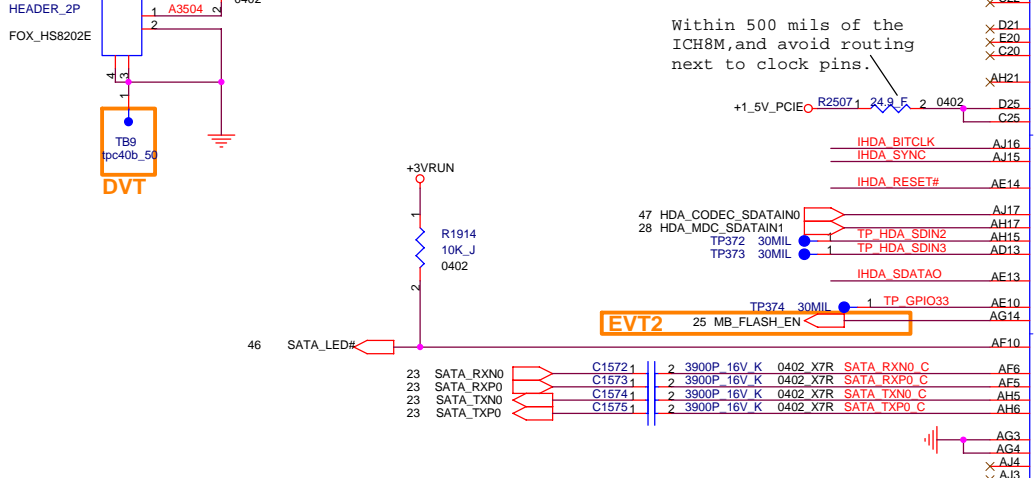
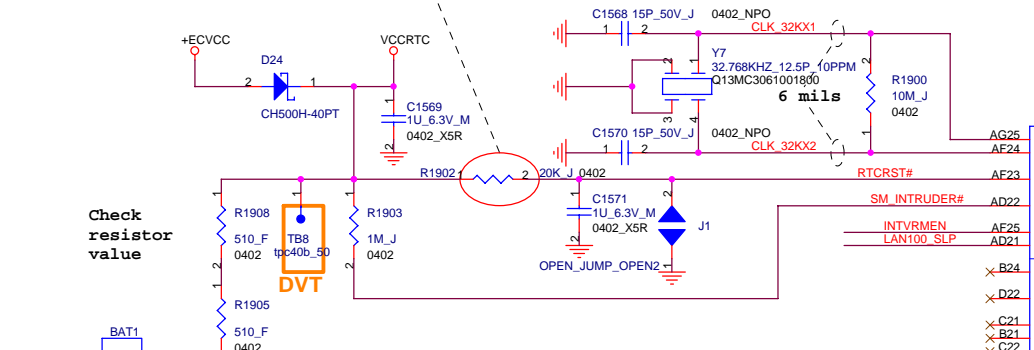
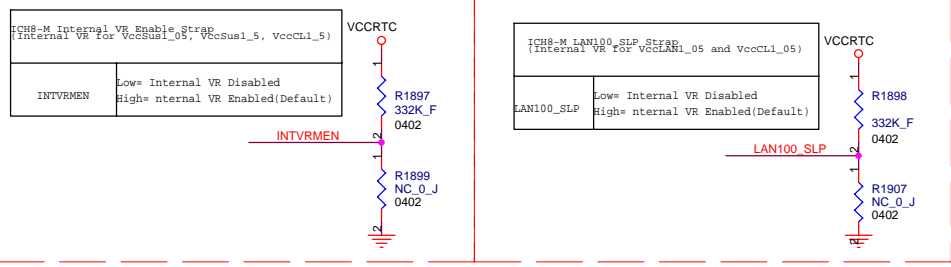
Title: **ICH8-M (PCI/DMI/USB/PCIE) 1/5**

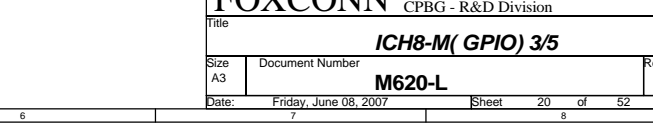
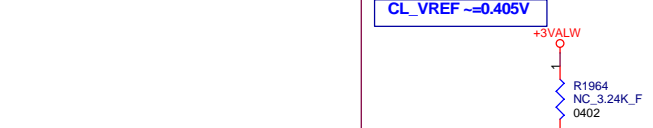
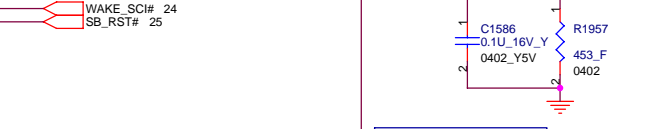
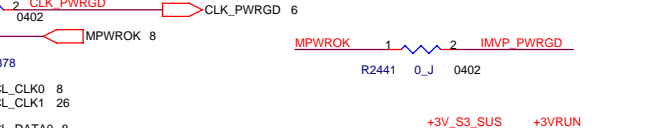
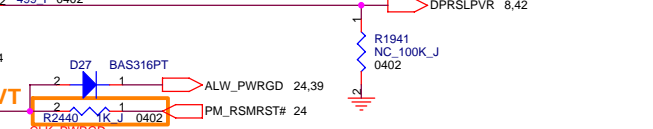
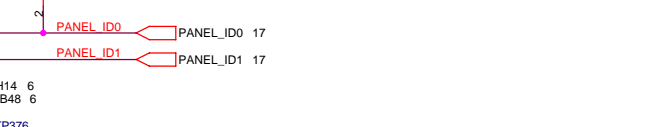
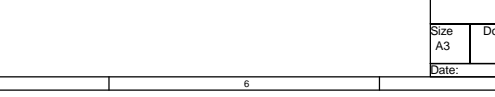
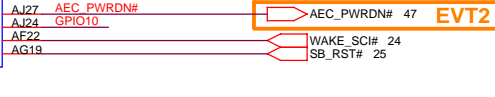
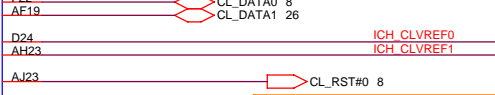
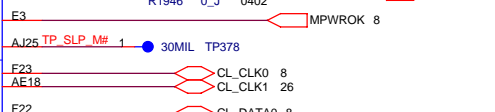
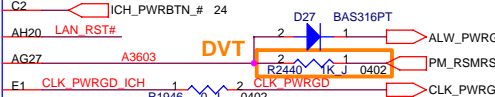
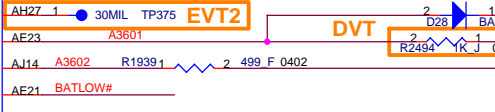
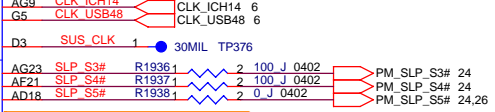
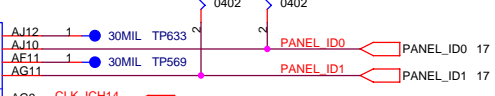
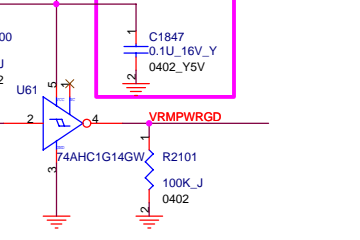
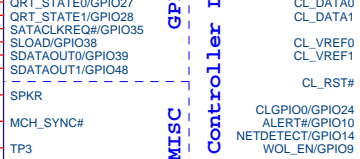
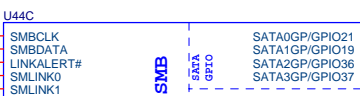
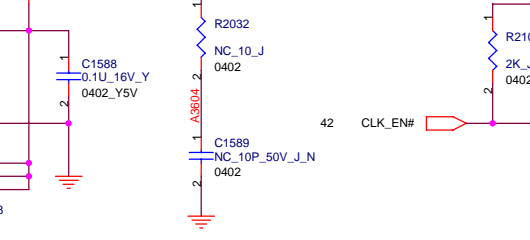
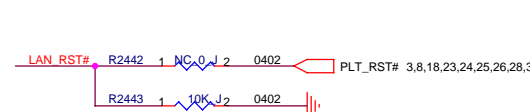
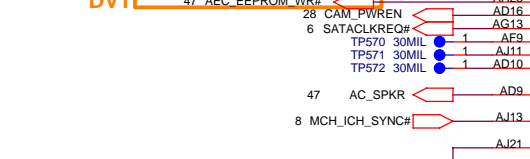
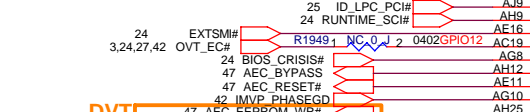
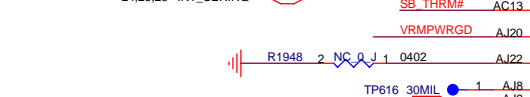
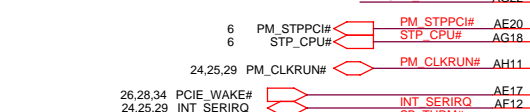
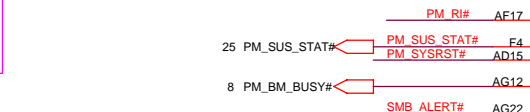
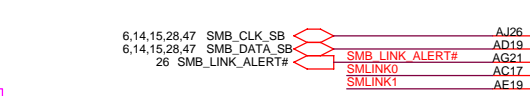
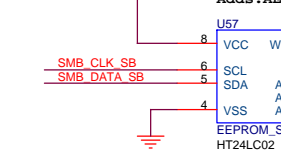
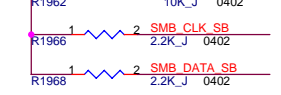
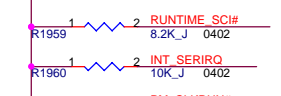
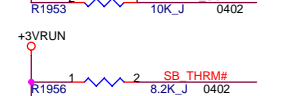
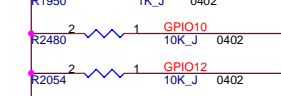
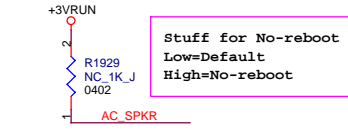
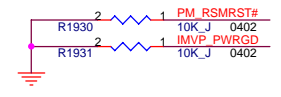
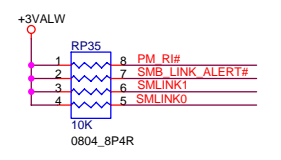
Size: A3 Document Number: **M620-L** Rev: 1.0

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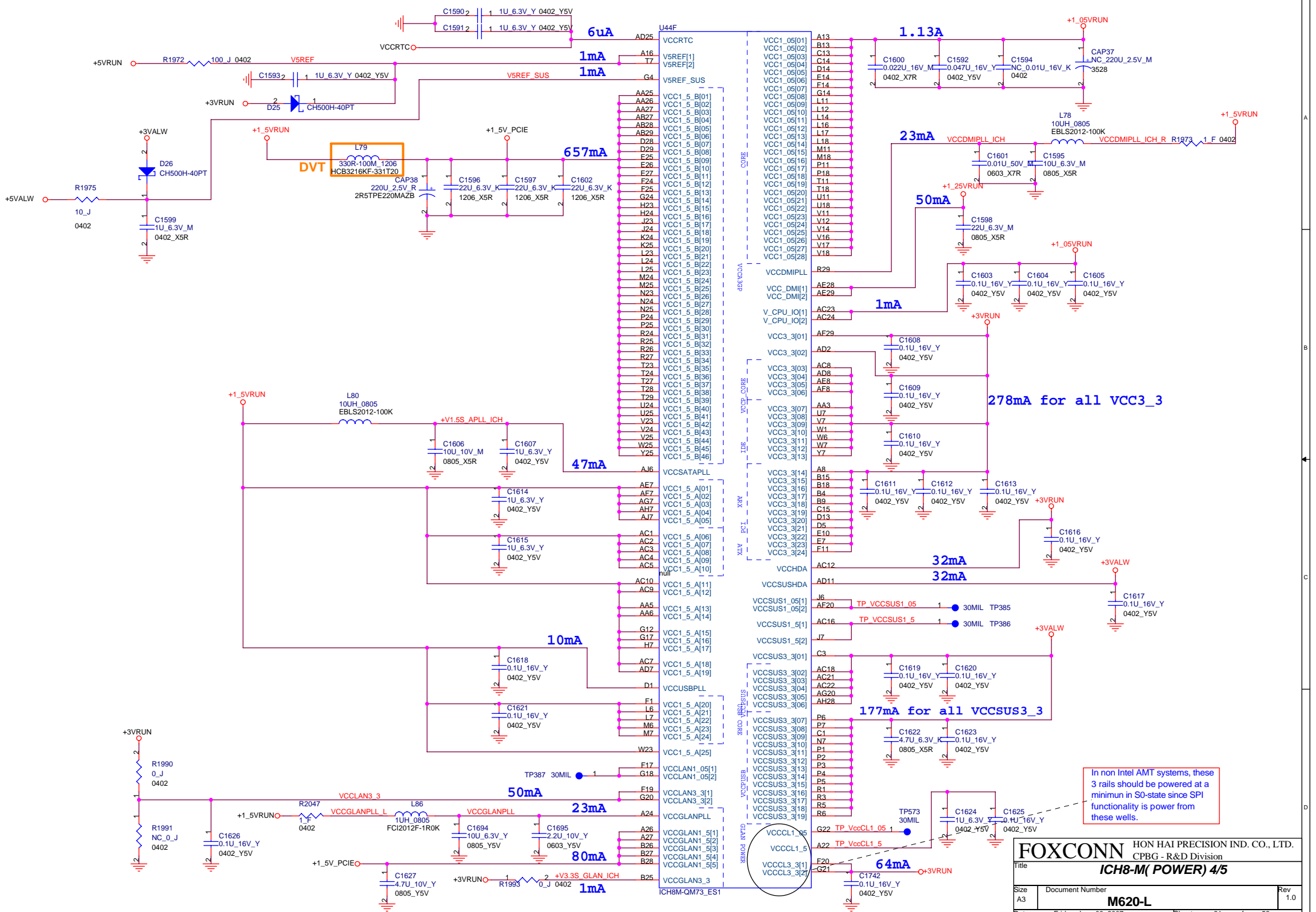


The traces inside this block should be wider. No digital signals routed under XTAL

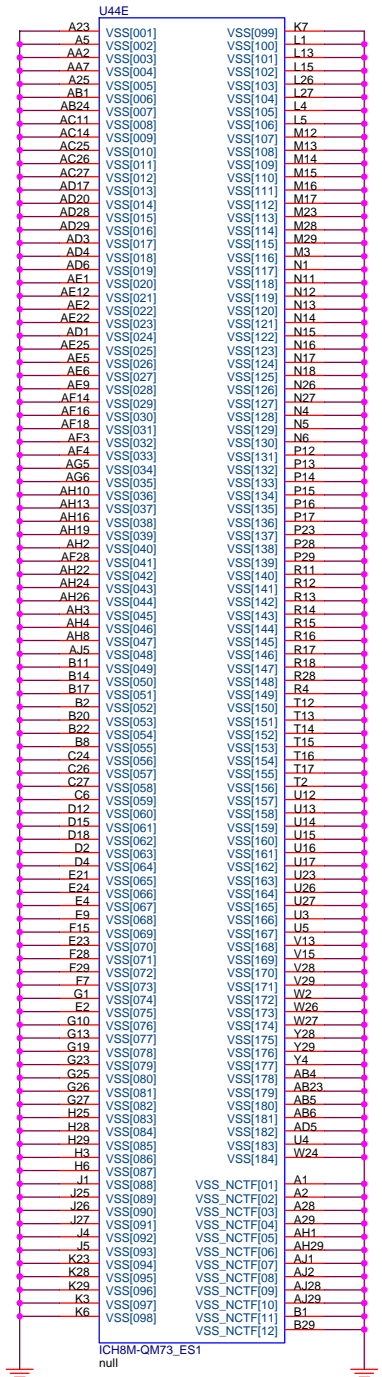




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		CPBG - R&D Division	
Title			
ICH8-M(GPIO) 3/5			
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In non Intel AMT systems, these 3 rails should be powered at a minimum in S0-state since SPI functionality is power from these wells.

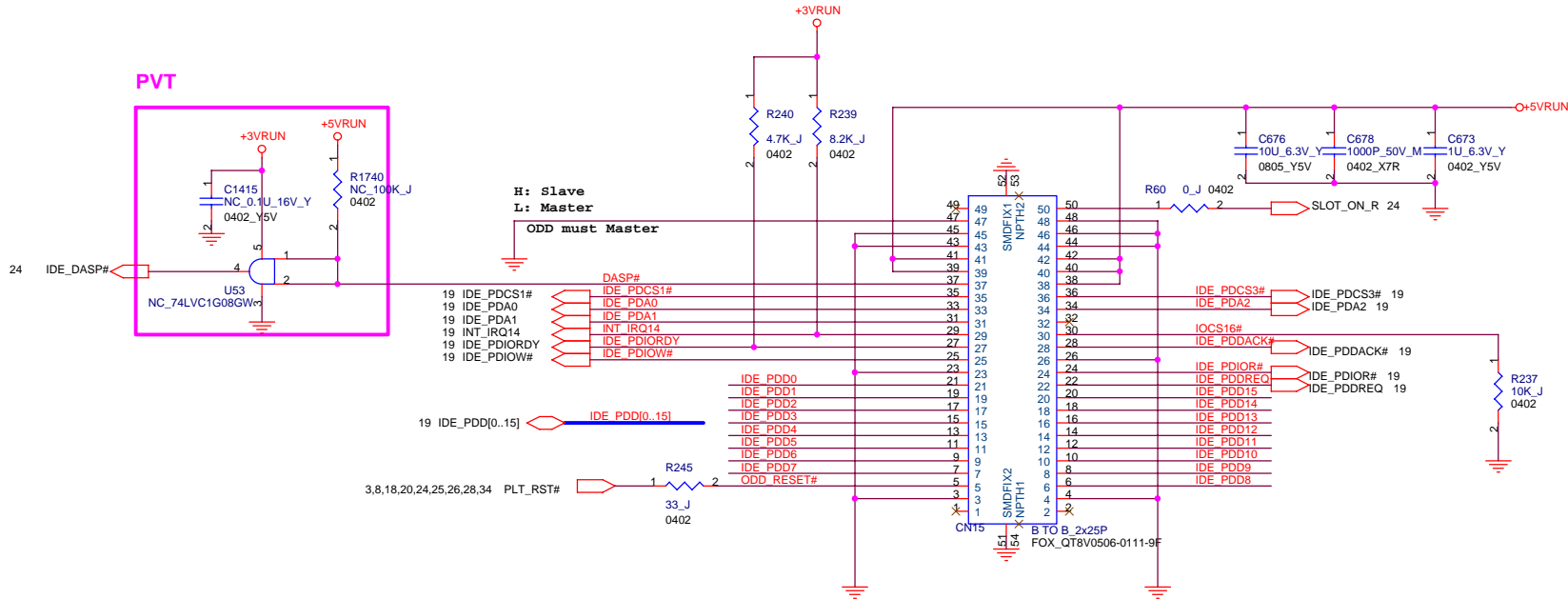
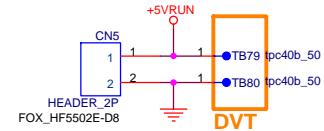
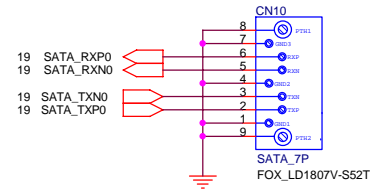
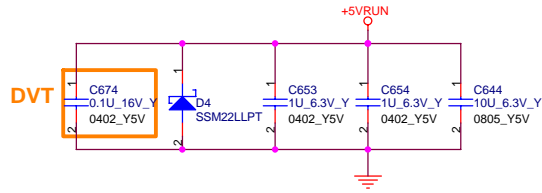


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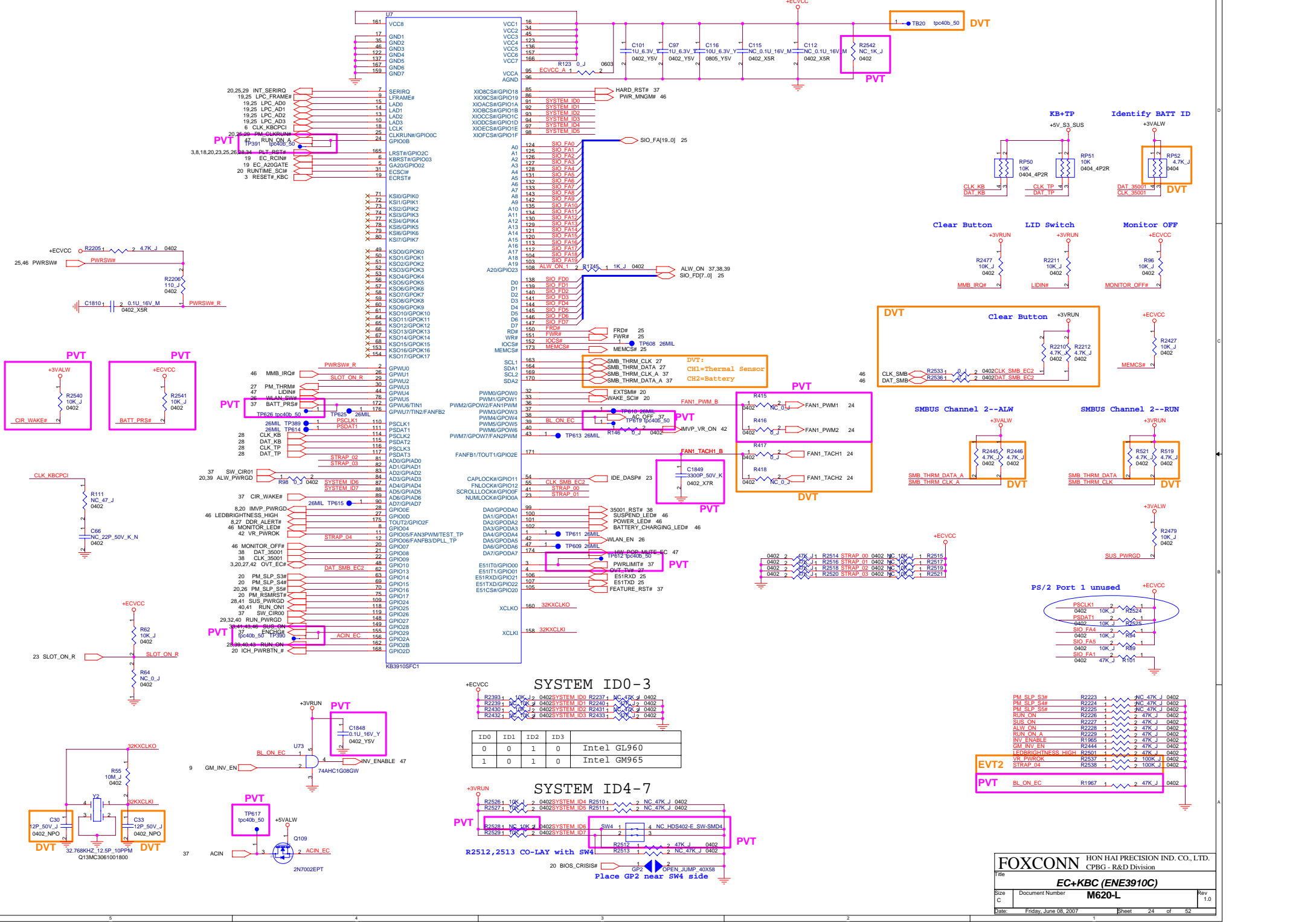
Title: **ICH8-M( GND) 5/5**

Size: A3	Document Number: <b>M620-L</b>	Rev: 1.0
Date: Friday, June 08, 2007	Sheet: 22	of 52

# SATA HDD CONN



# CD-ROM CONN



### SYSTEM ID0-3

ID0	ID1	ID2	ID3
0	0	1	0
1	0	1	0

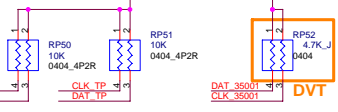
Intel GL960  
Intel GM965

### SYSTEM ID4-7

ID4	ID5	ID6	ID7
0	0	1	0
1	0	1	0

Place GP2 near SW4 side

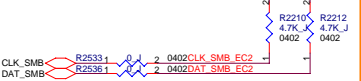
### Identify BATT ID



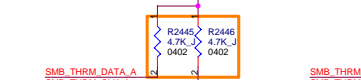
### Clear Button LID Switch Monitor OFF



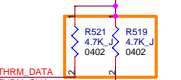
### DVT Clear Button +3VRUN



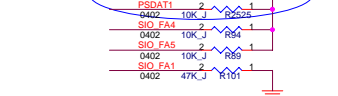
### SMBUS Channel 2--ALW



### SMBUS Channel 2--RUN



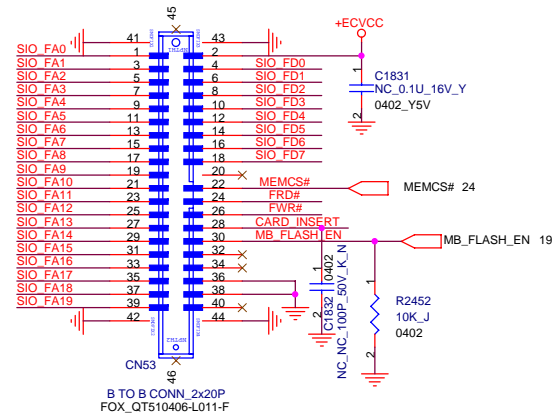
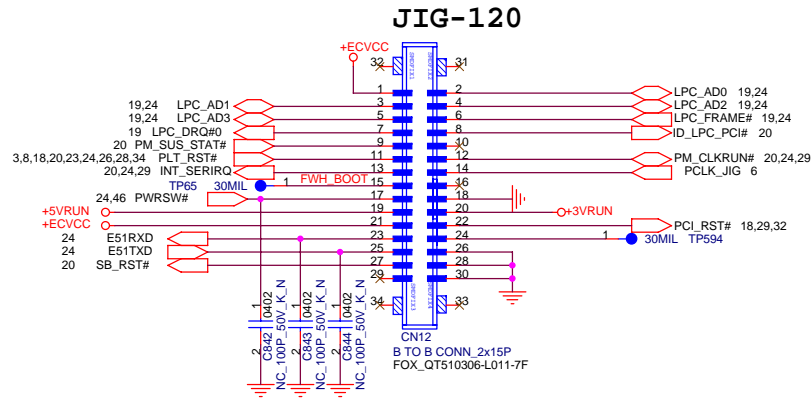
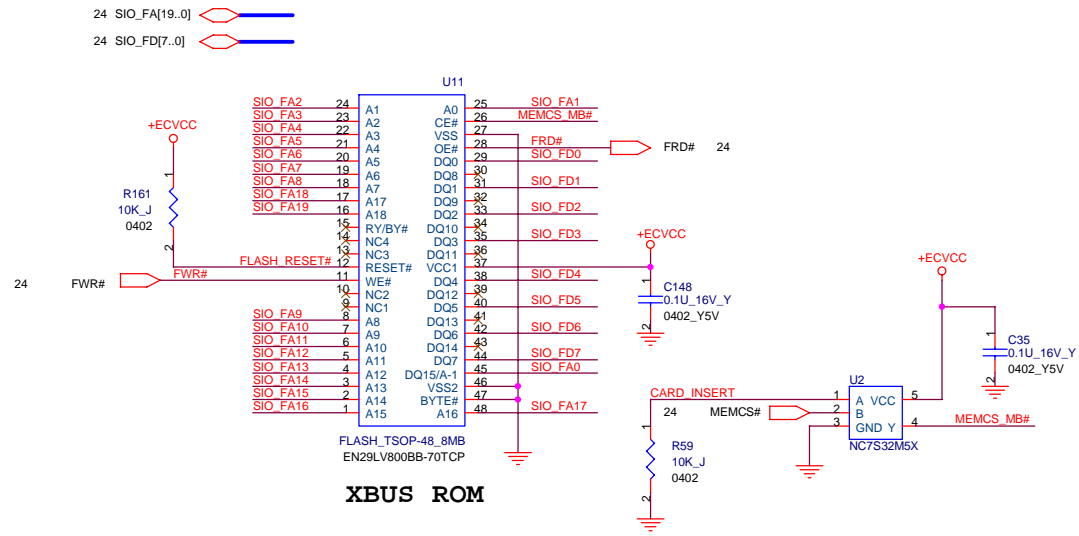
### PS/2 Port 1 unused

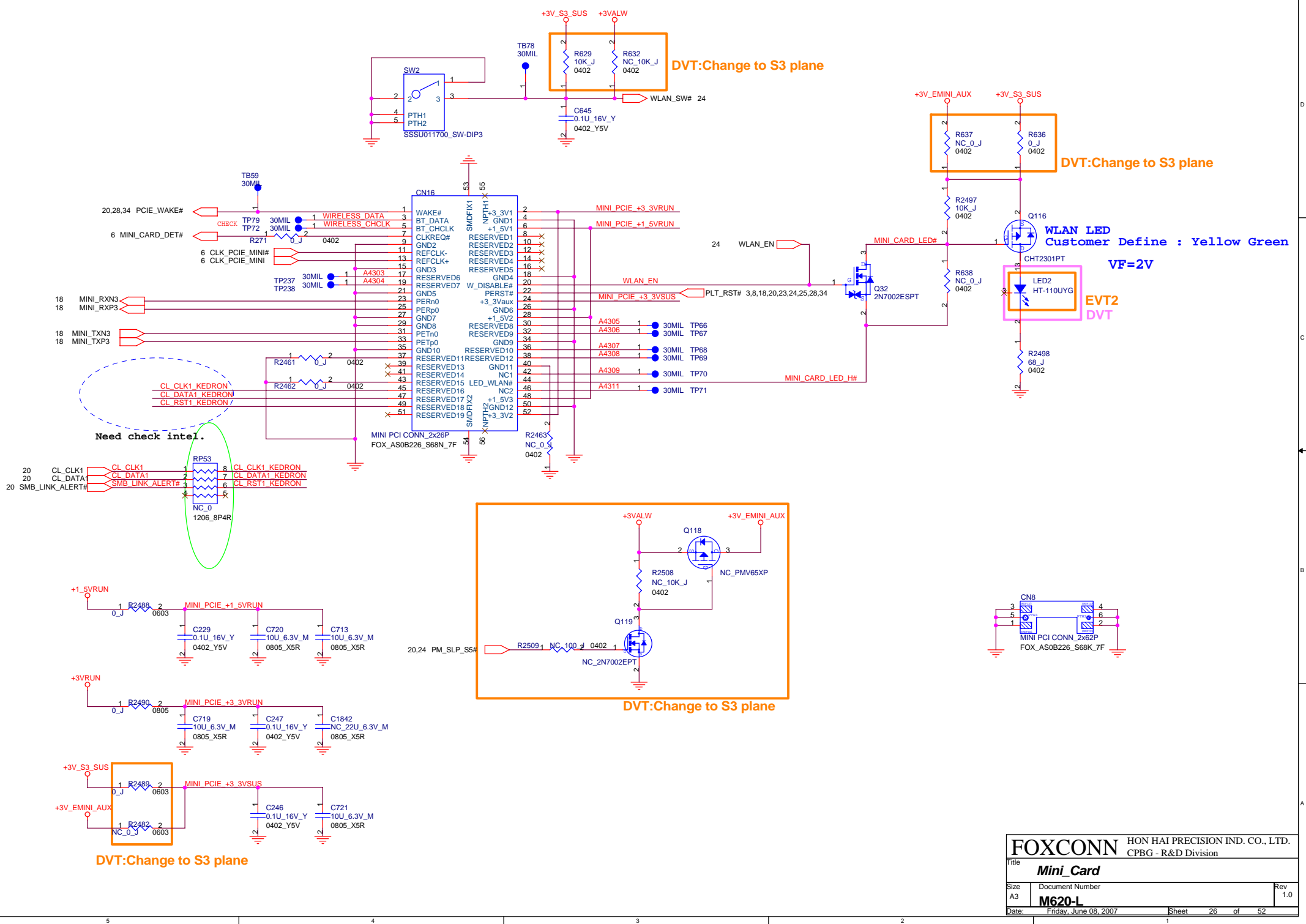


### EVT2 PVT









DVT:Change to S3 plane

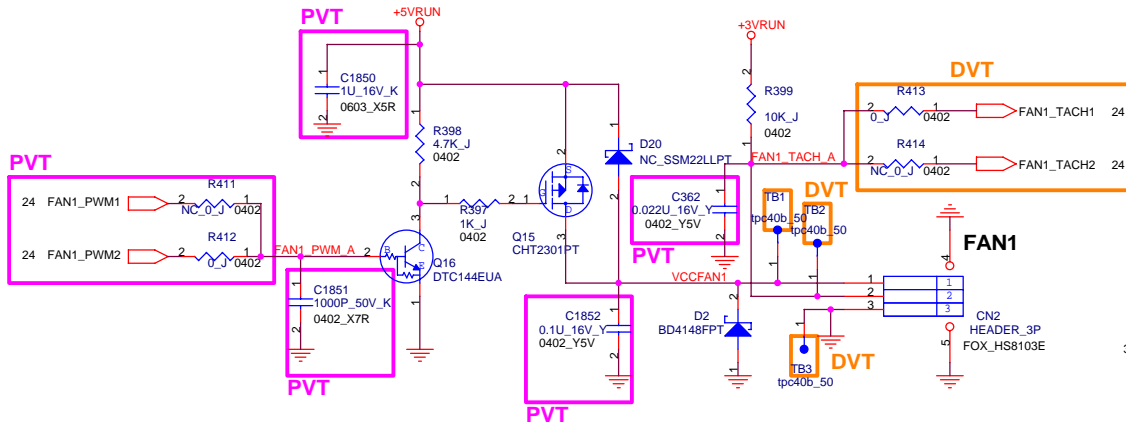
DVT:Change to S3 plane

DVT:Change to S3 plane

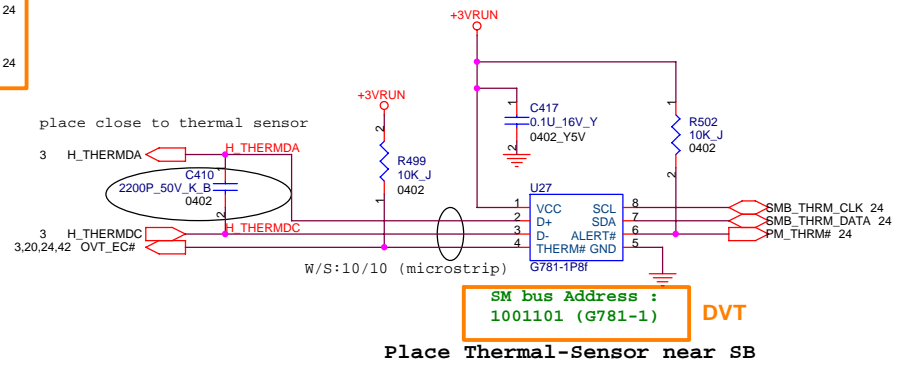
DVT:Change to S3 plane

<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
<b>Mini Card</b>			
Size	Document Number	Rev	
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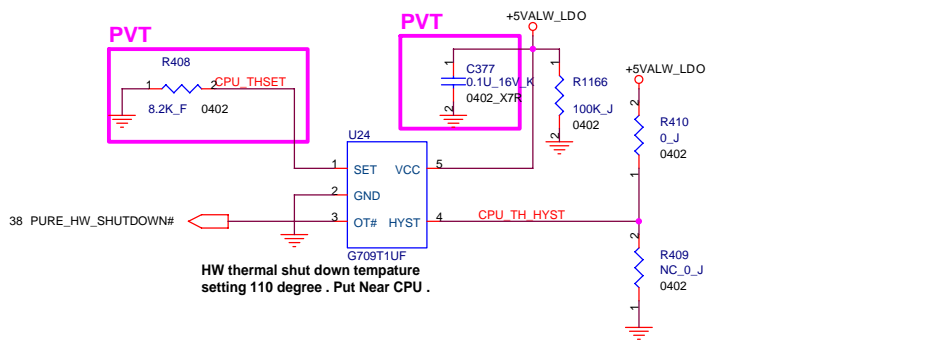
# FAN



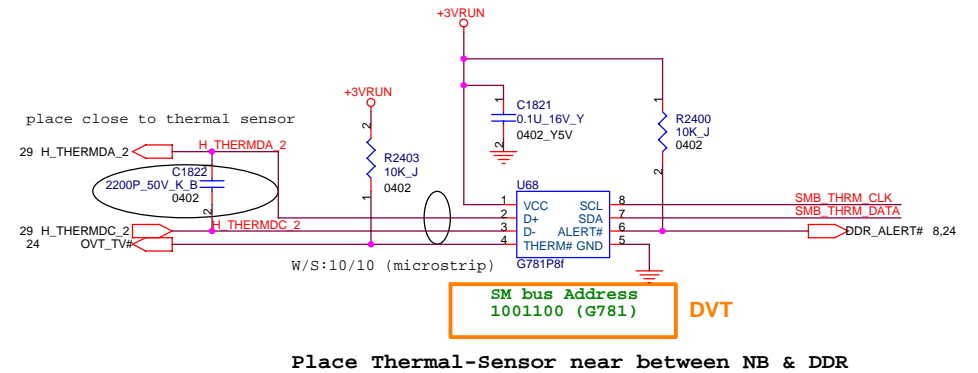
# CPU/AUDIO SENSOR G781-1



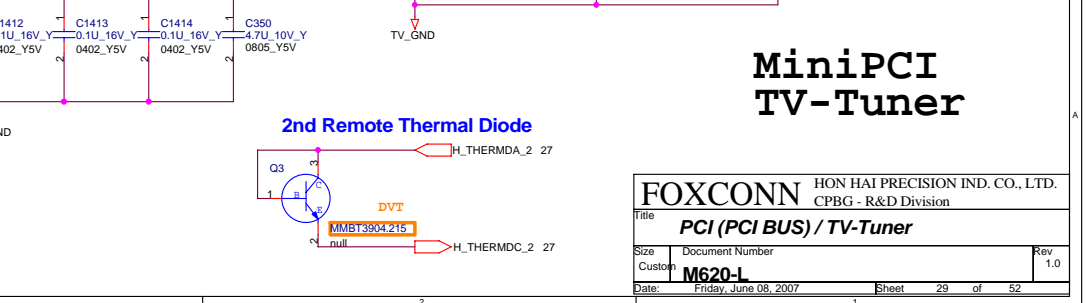
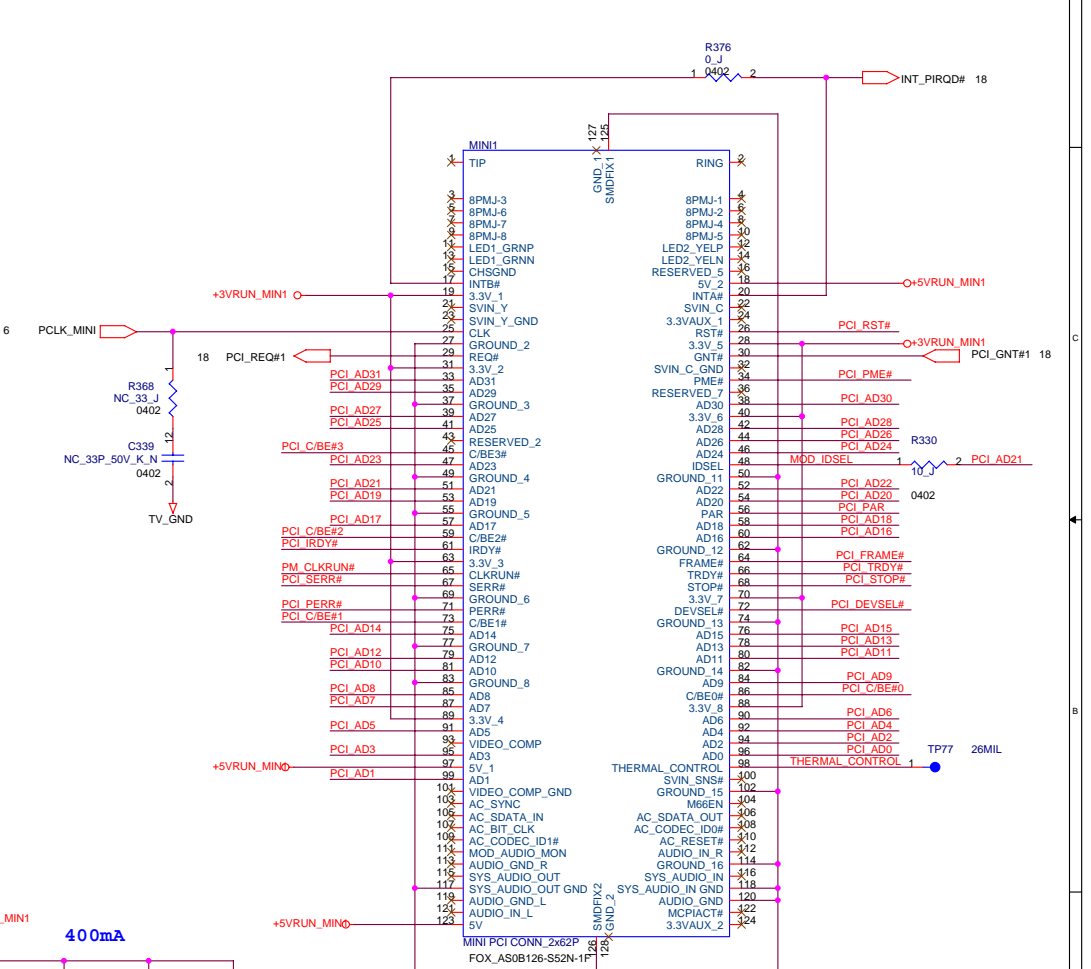
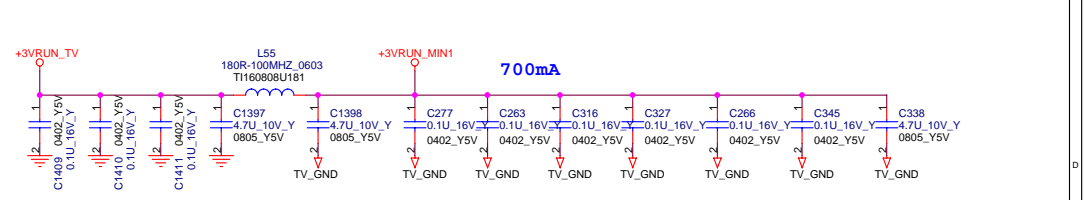
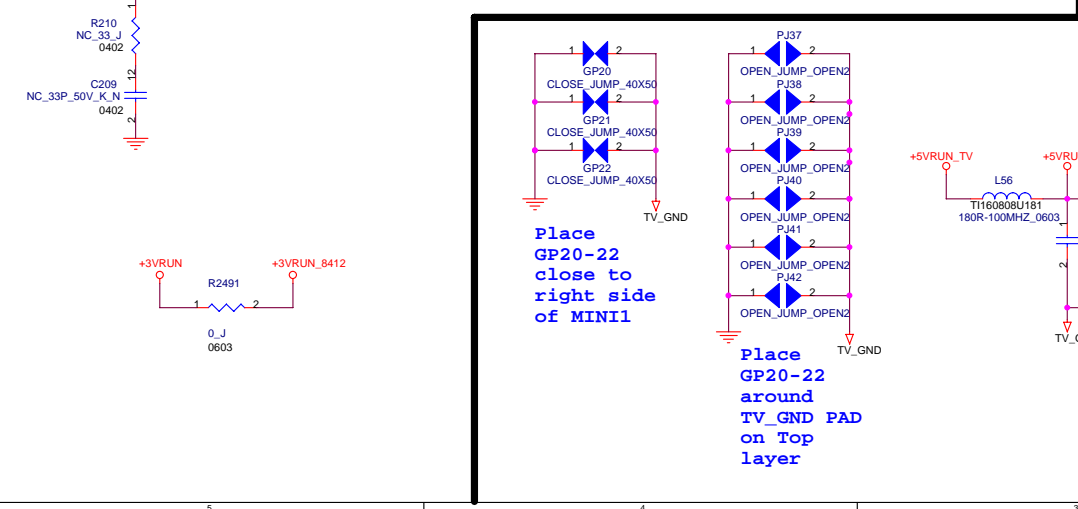
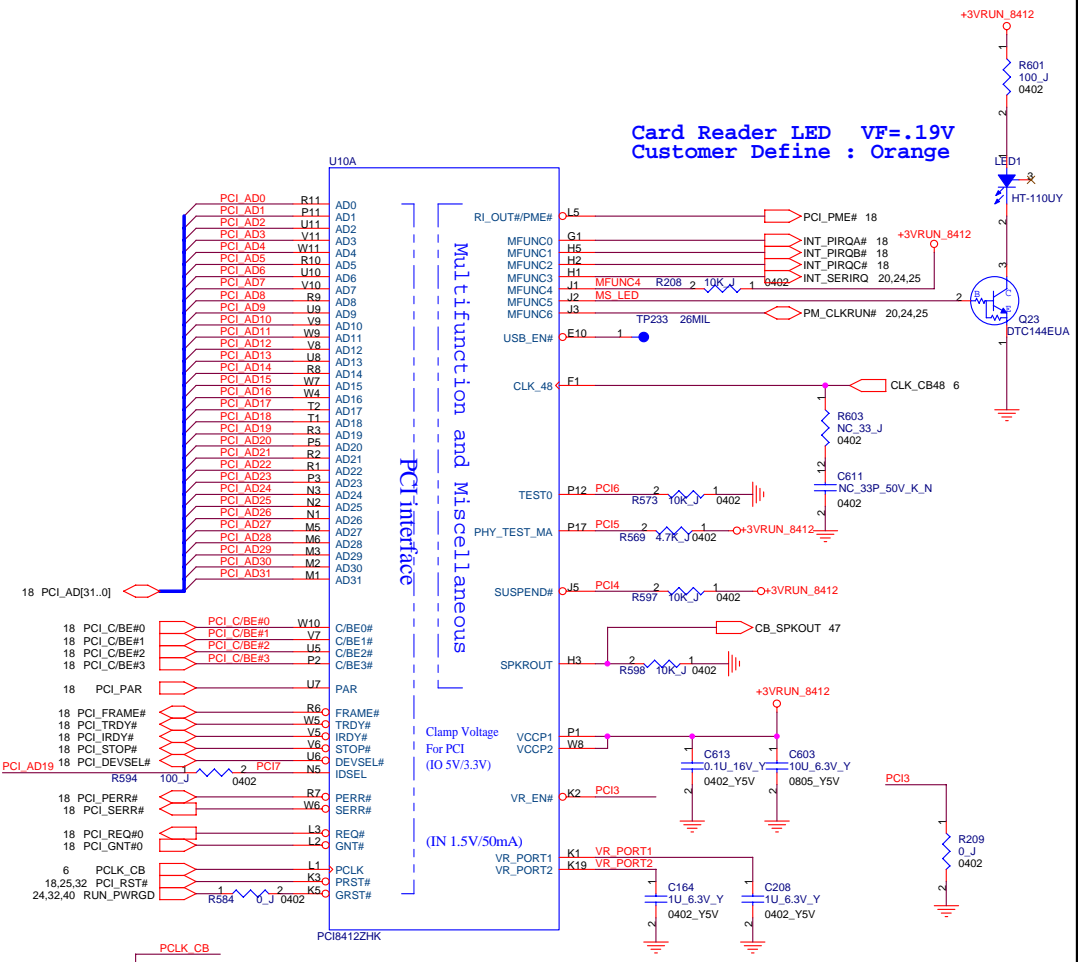
# HW THERMAL PROTECTION



# GMCH/DDR/TV SENSOR G781







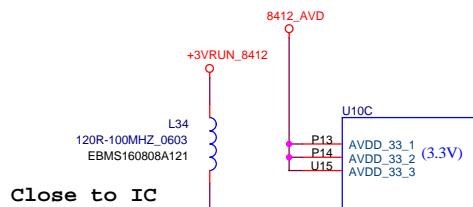
# MiniPCI TV-Tuner

**FOXCONN** HON HAI PRECISION IND. CO., LTD.  
CPBG - R&D Division

Title: **PCI (PCI BUS) / TV-Tuner**

Size: Document Number  
Custom: **M620-L**

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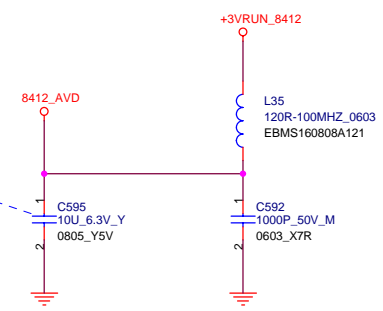


Close to IC

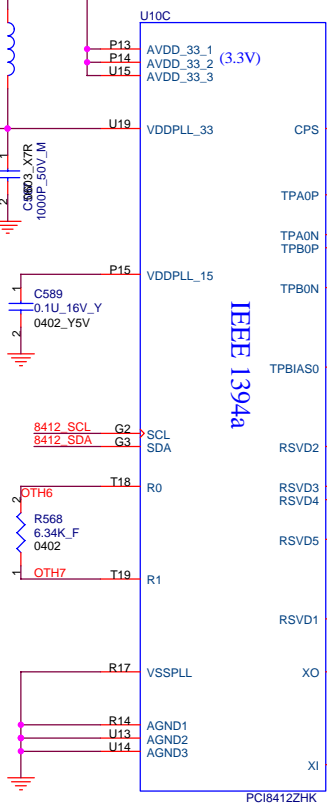
This capacitor should be placed between Pin P15 and Pin R17 .

This capacitor must be placed to IC pin

This array must be placed close to AVDD(Pin P13,P14,U10) They must be tied to a low-impedance GND.

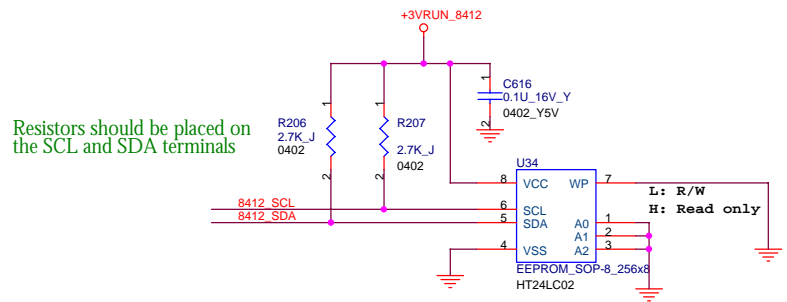
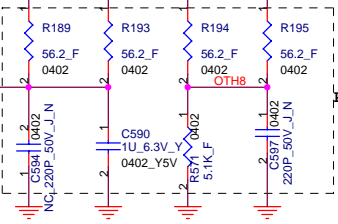
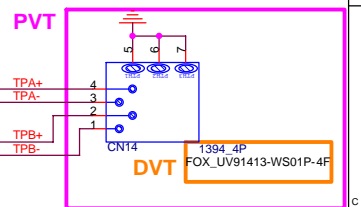


IEEE 1394a



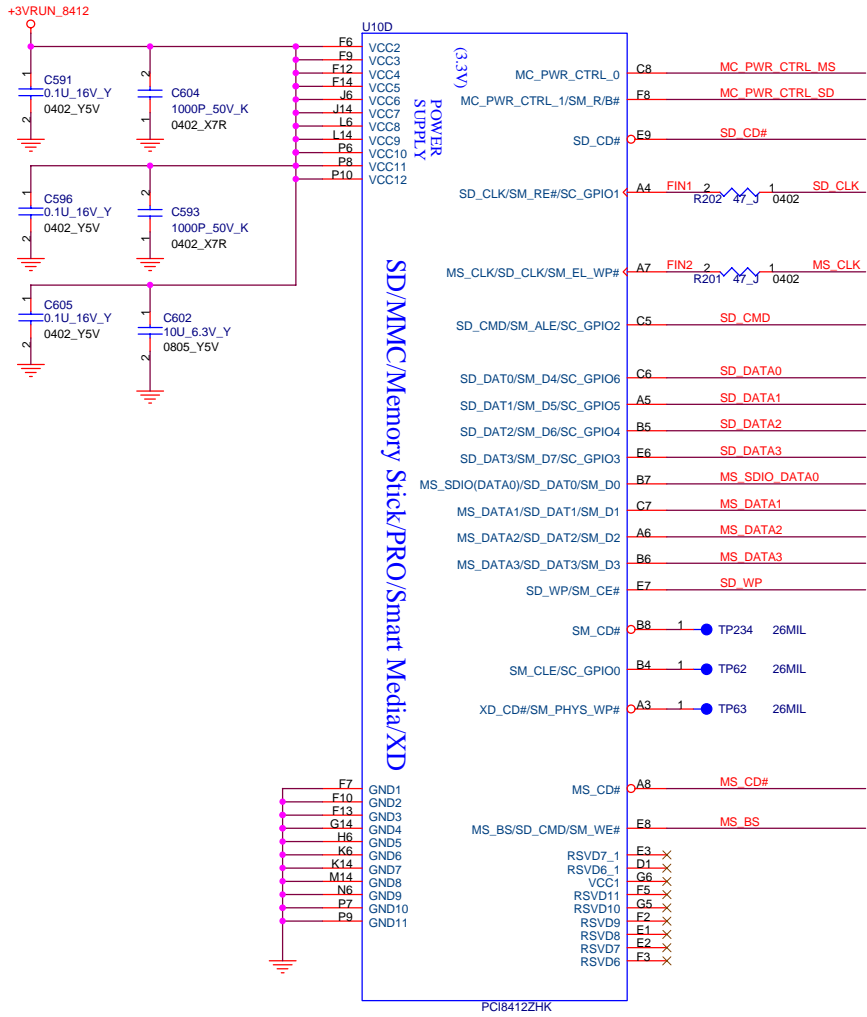
Place near PCI8412.

iLink CONN.



Resistors should be placed on the SCL and SDA terminals

<b>FOXCONN</b> HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division	
Title <b>PCI (ILINK)</b>	
Size A3	Document Number <b>M620-L</b>
Date: Friday, June 08, 2007	Sheet 30 of 52



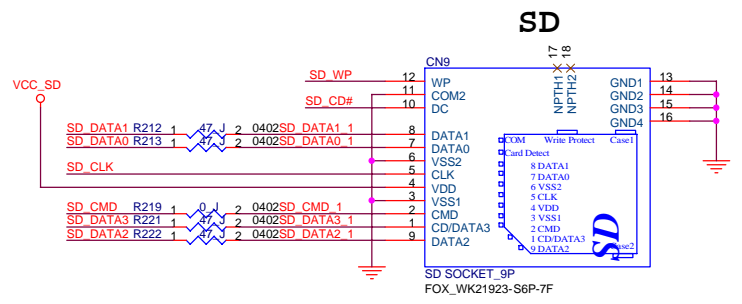
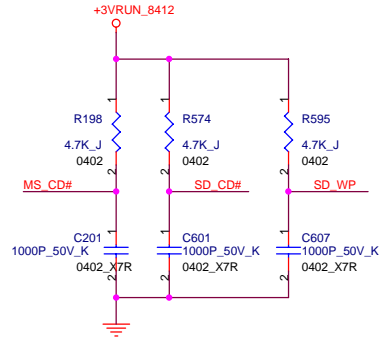
SD/MMC/Memory Stick/PRO/Smart Media/XD

+3VRUN\_8412

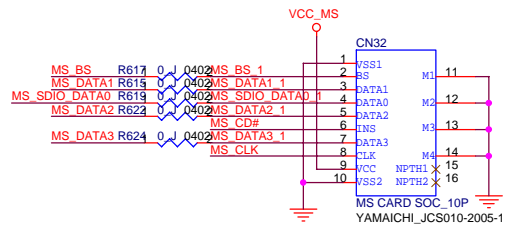
U10D  
POWER SUPPLY

(3.3V)

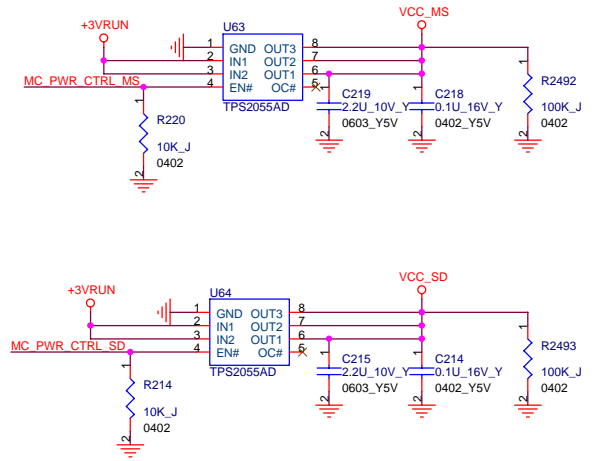
PCI8412ZHK

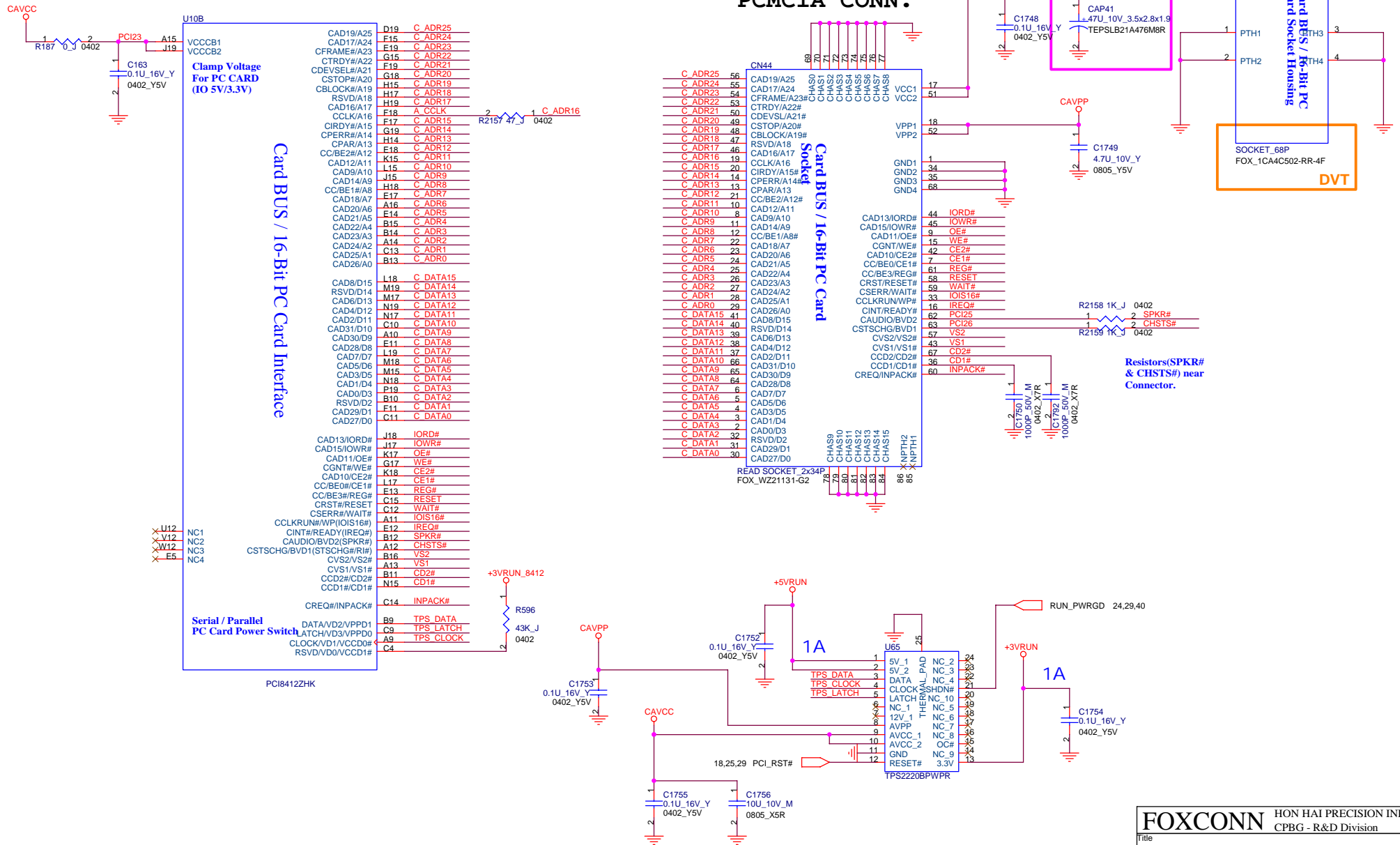


SD



MS Duo





**PCMCIA CONN.**

**PVT**

**Card BUS / 16-Bit PC Card Socket Housing**

**Card BUS / 16-Bit PC Card**

**Clamp Voltage For PC CARD (IO 5V/3.3V)**

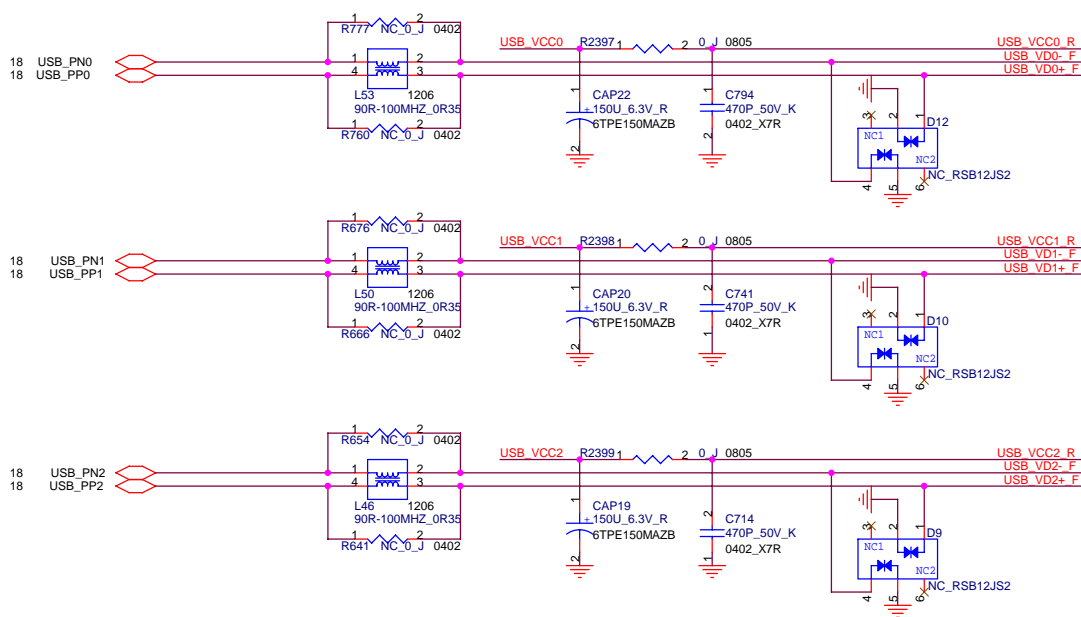
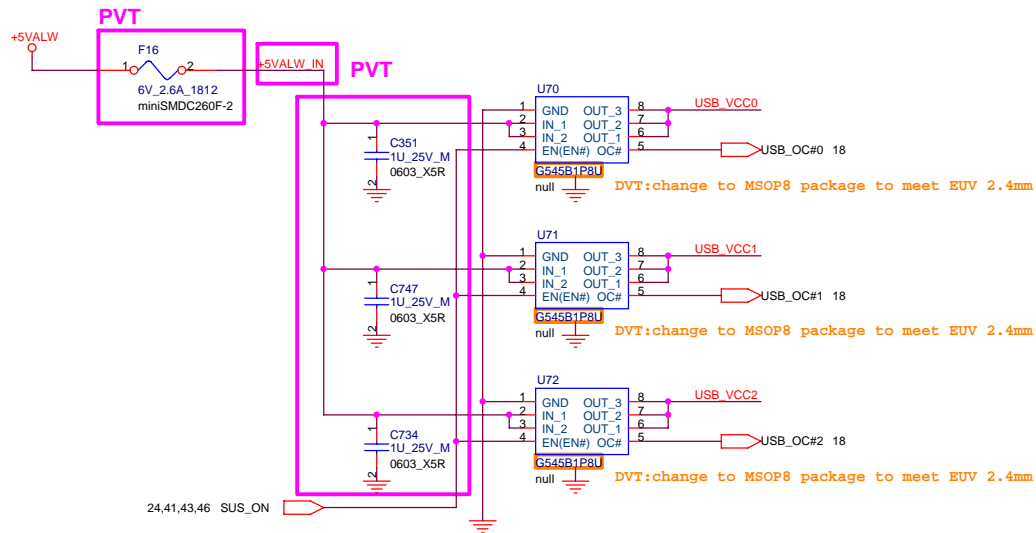
**Card BUS / 16-Bit PC Card Interface**

**Serial / Parallel PC Card Power Switch**

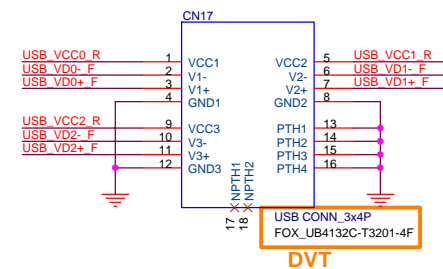
**Resistors (SPKR# & CHSTS#) near Connector.**

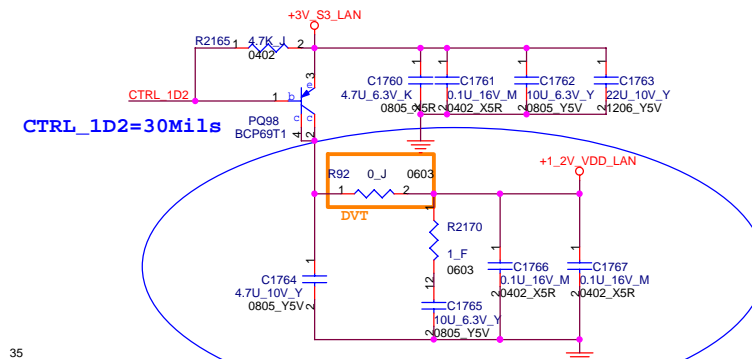
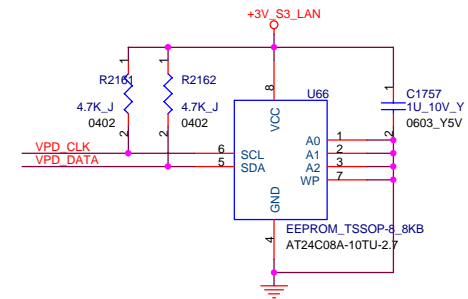
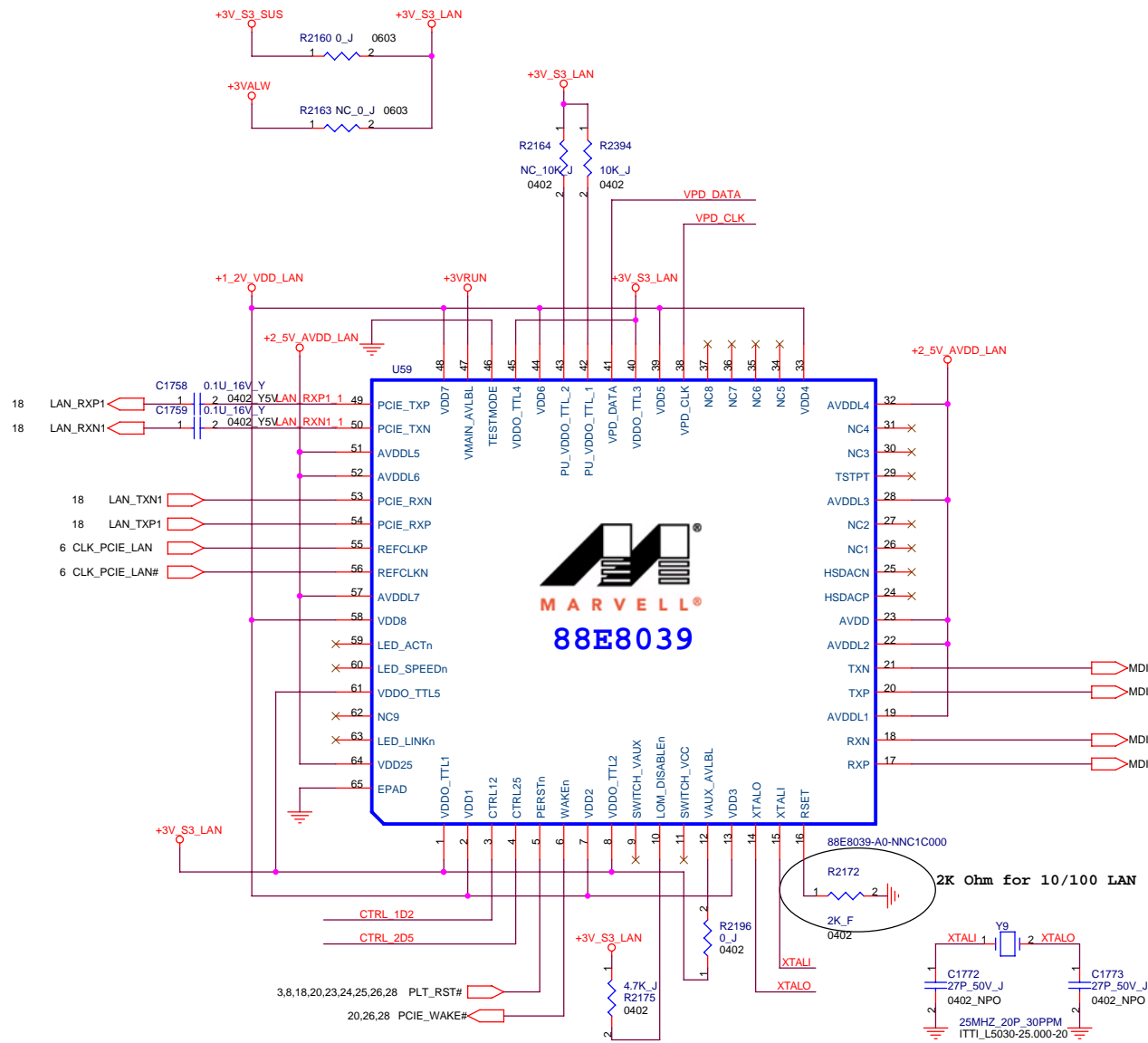
<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
<b>PCI ( PCMCIA )</b>			
Size	Document Number	Rev	
A3	<b>M620-L</b>	1.0	
Date:	Friday, June 08, 2007	Sheet	32 of 52



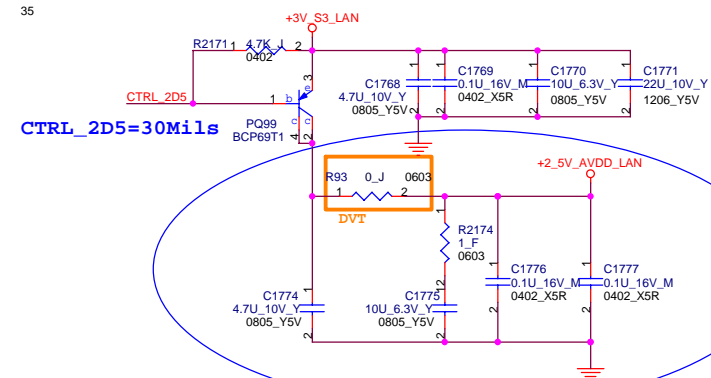


## REAR USB CONN X 3



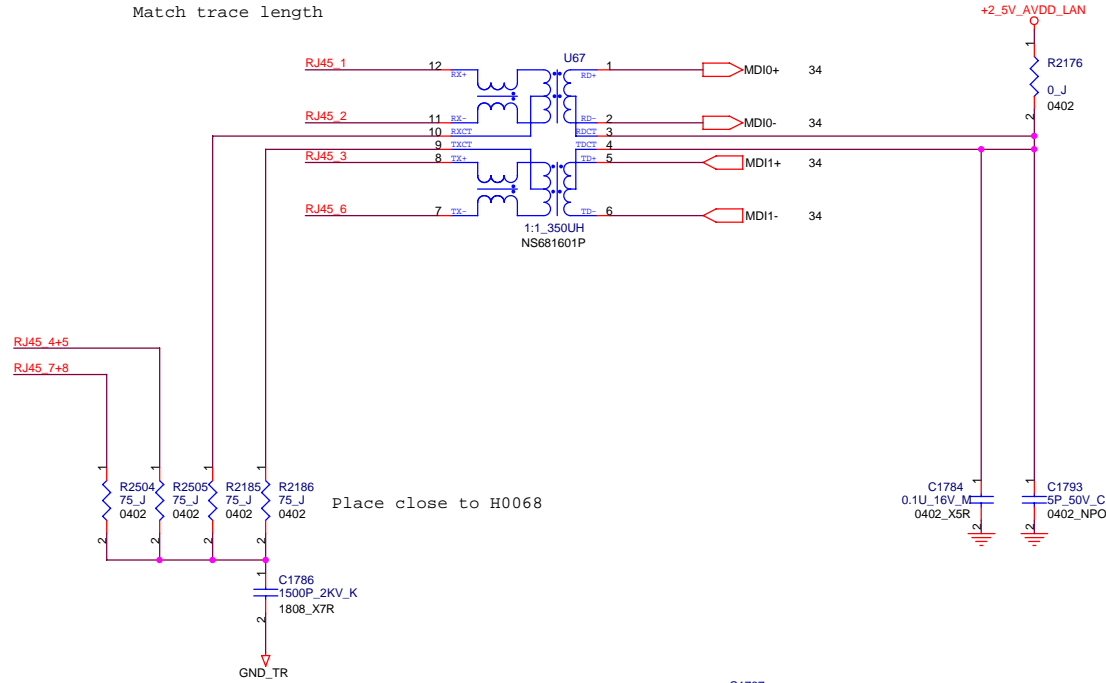


Place these components close to U59

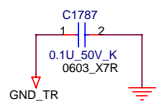
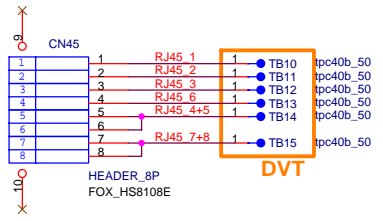
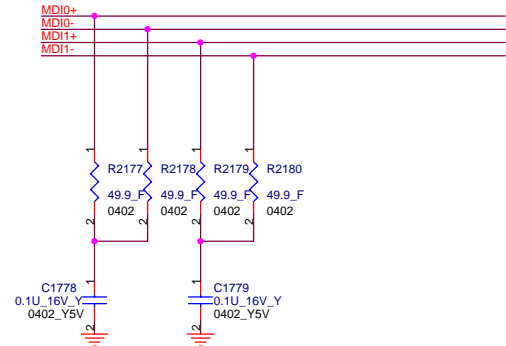


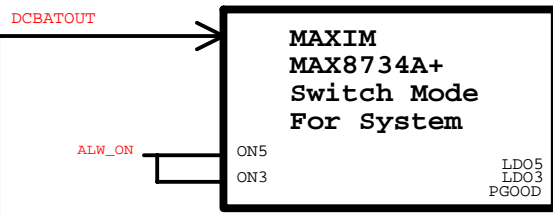
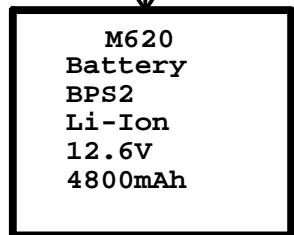
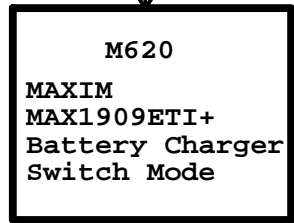
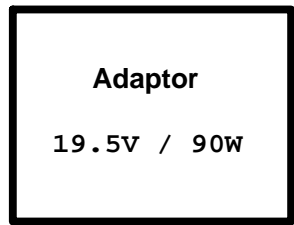
Place these components close to U59

Match trace length



Place close to H0068



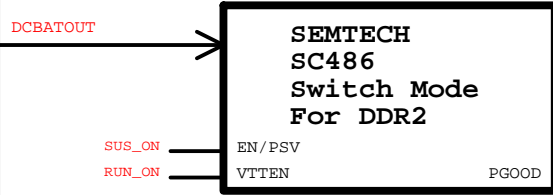
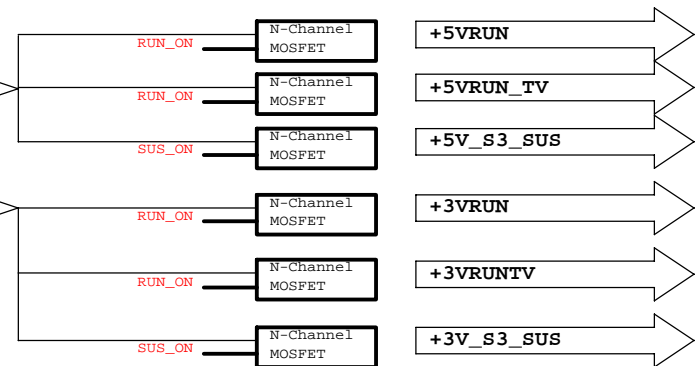


System

+5VALW 7A

System

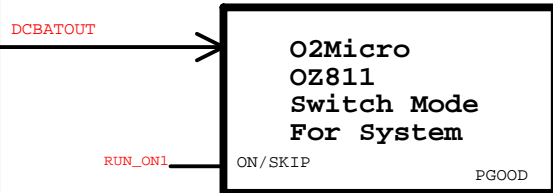
+3VALW/7A



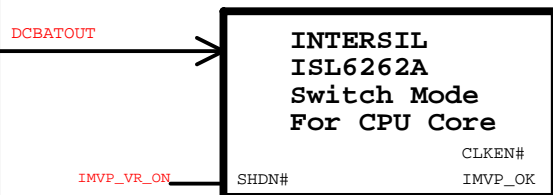
+1\_8V\_S3\_SUS/10A

+0\_9V\_S3\_SUS/3.0A

DDRDIMM\_VREF



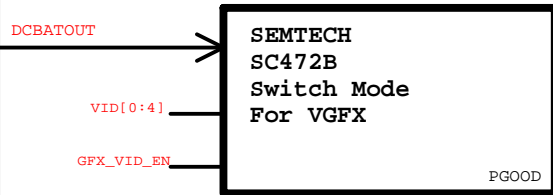
+1\_05VRUN/ 7.5A / 15A



VHORE/44A

CLK\_EN#

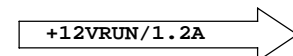
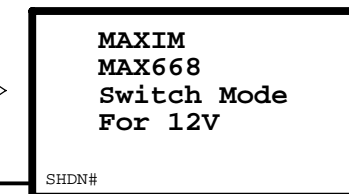
IMVP\_OK

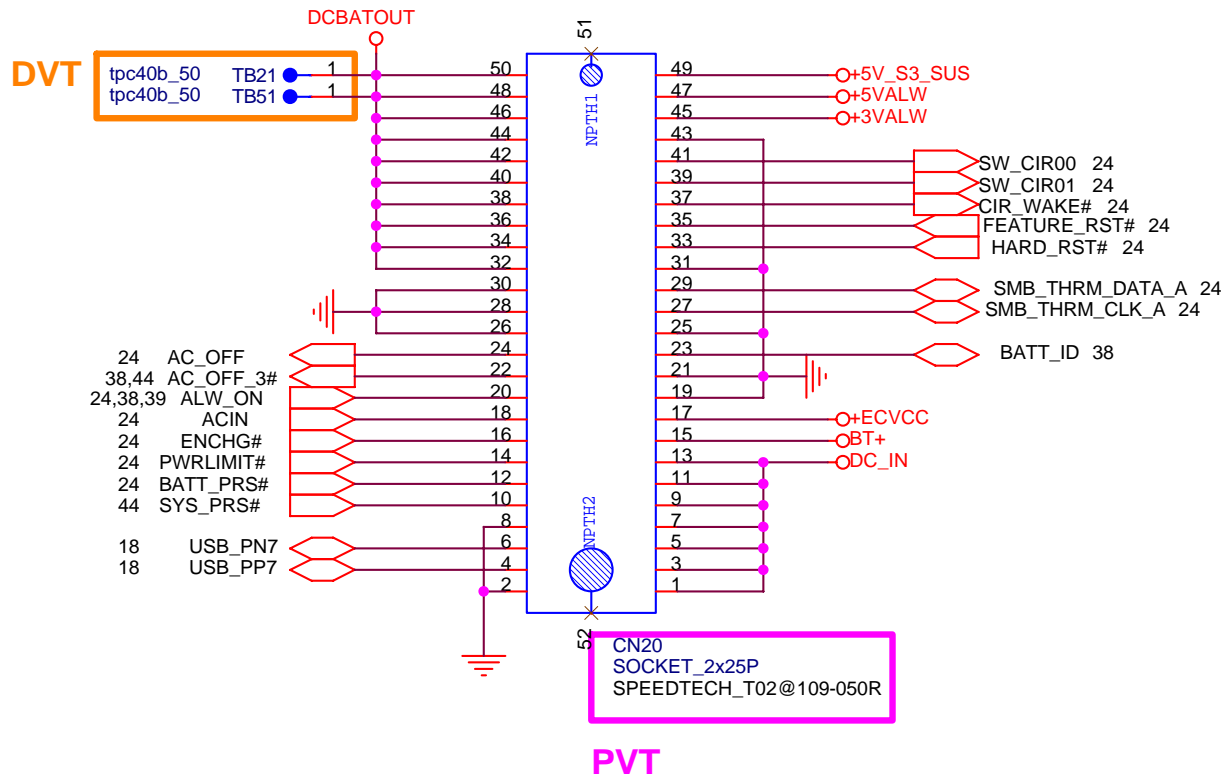


VGFX(1.05V)/7.5A

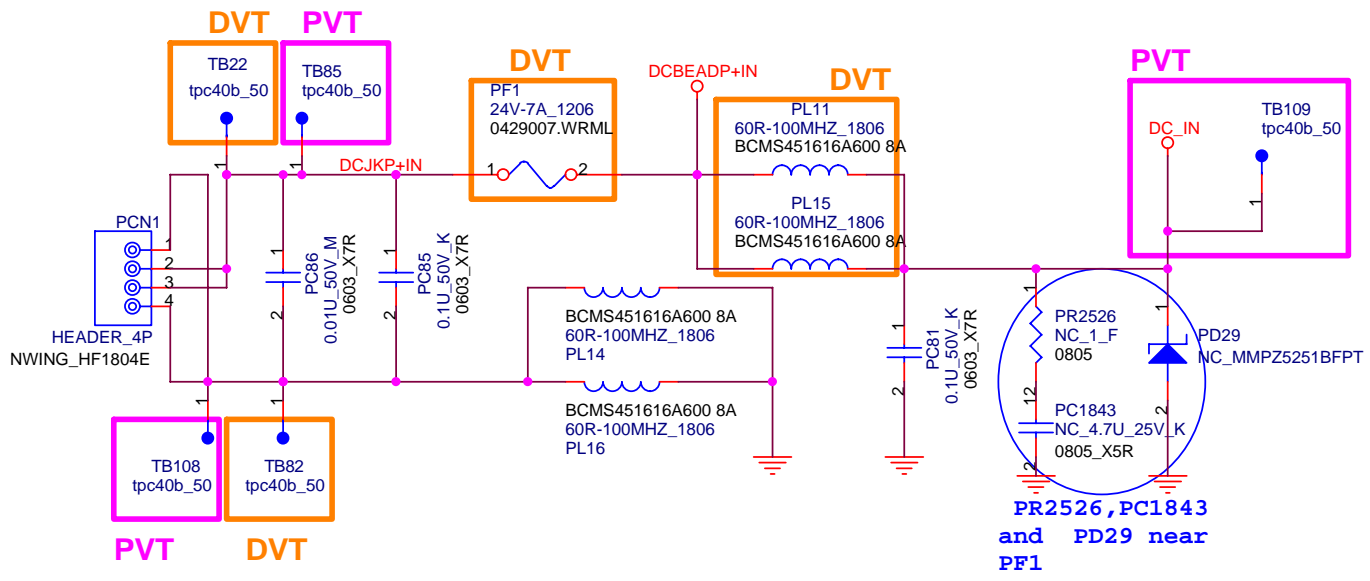


RUN\_ON\_A →

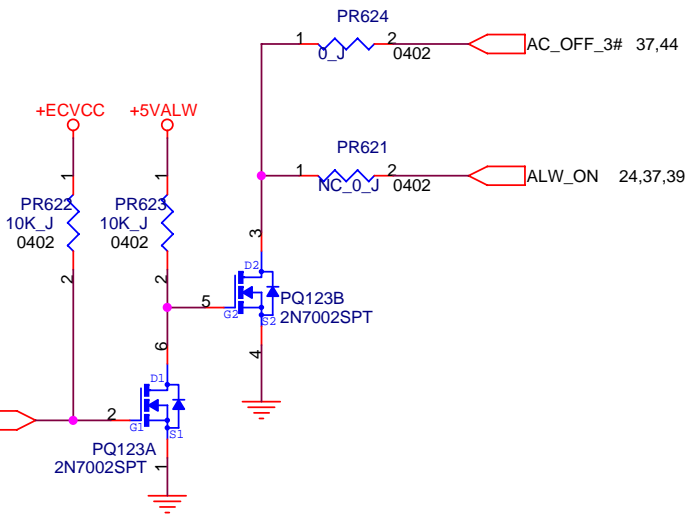




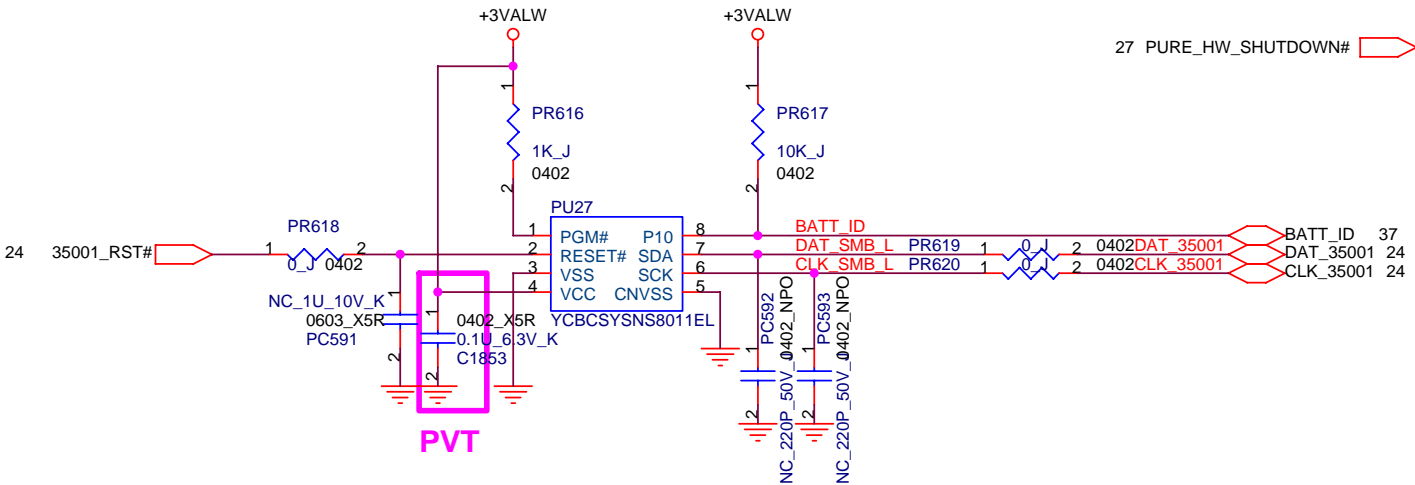
<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title			
<b>Battery DB Connector</b>			
Size	Document Number	Rev	
A	<b>M620-L</b>	1.0	
Date:	Friday, June 08, 2007	Sheet	37 of 52



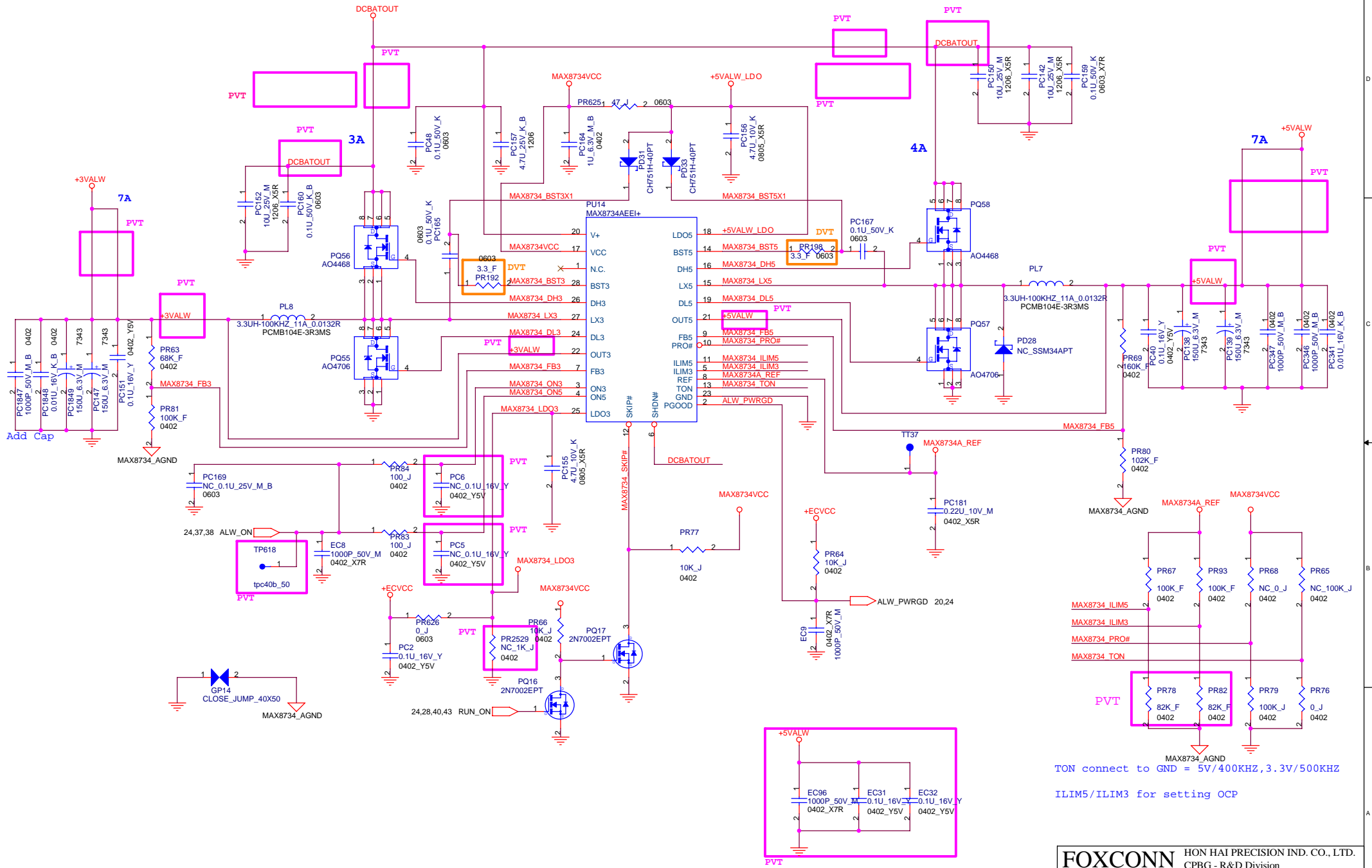
PR2526, PC1843 and PD29 near PF1



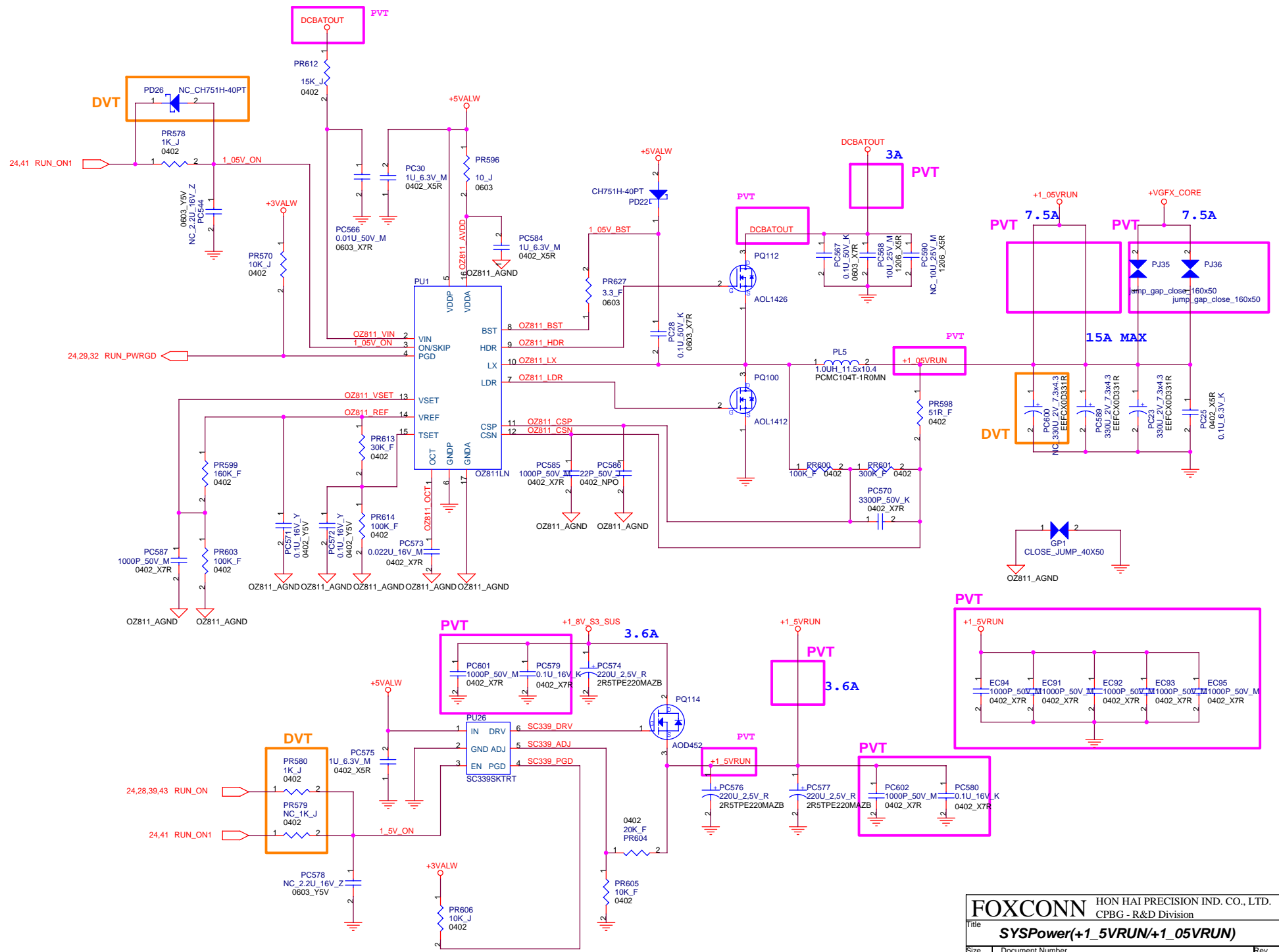
### Identify Battery



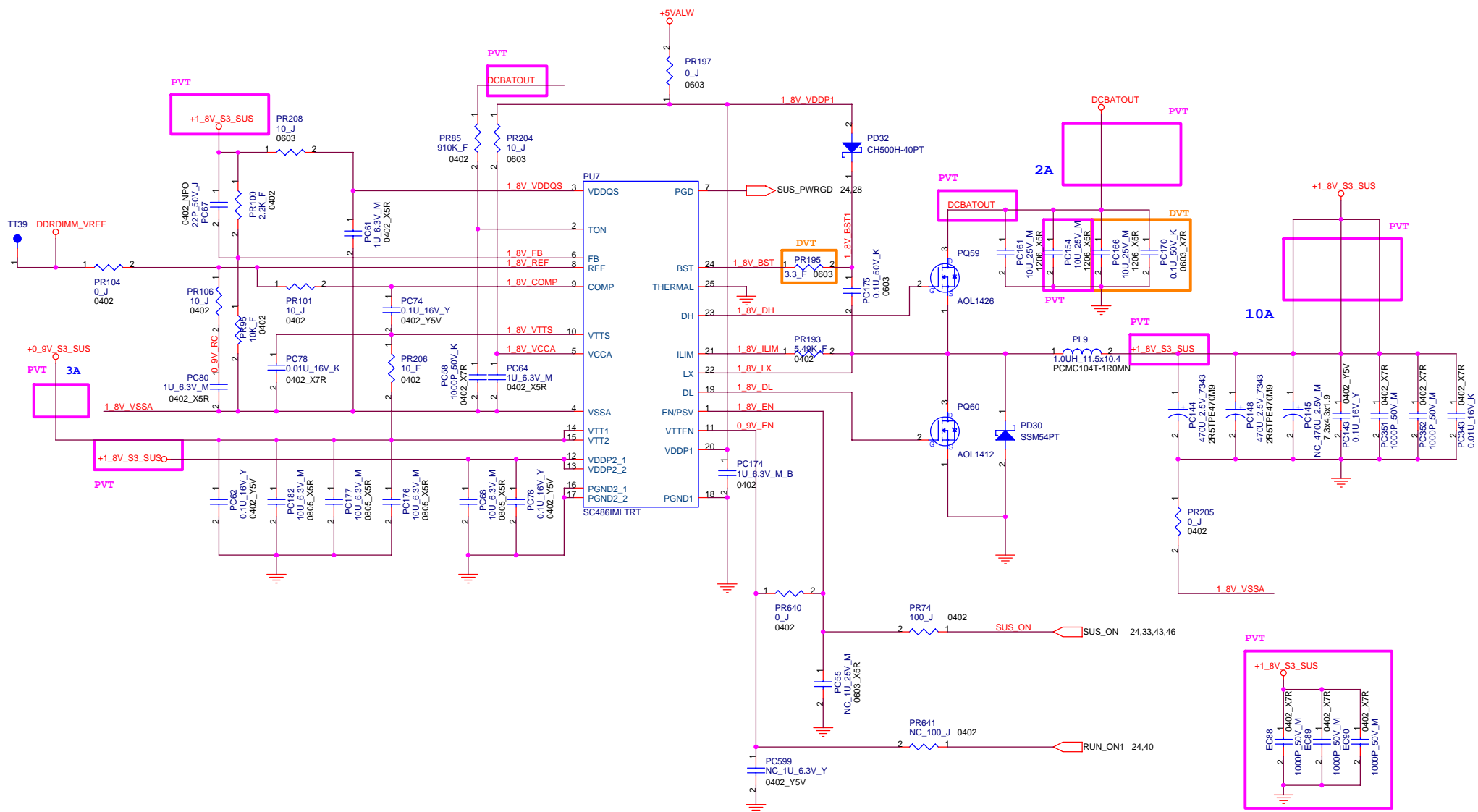
<b>FOXCONN</b>		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title <b>DCIN</b>			
Size A4	Document Number <b>M620-L</b>		Rev 1.0
Date: Friday, June 08, 2007	Sheet 38 of 52		

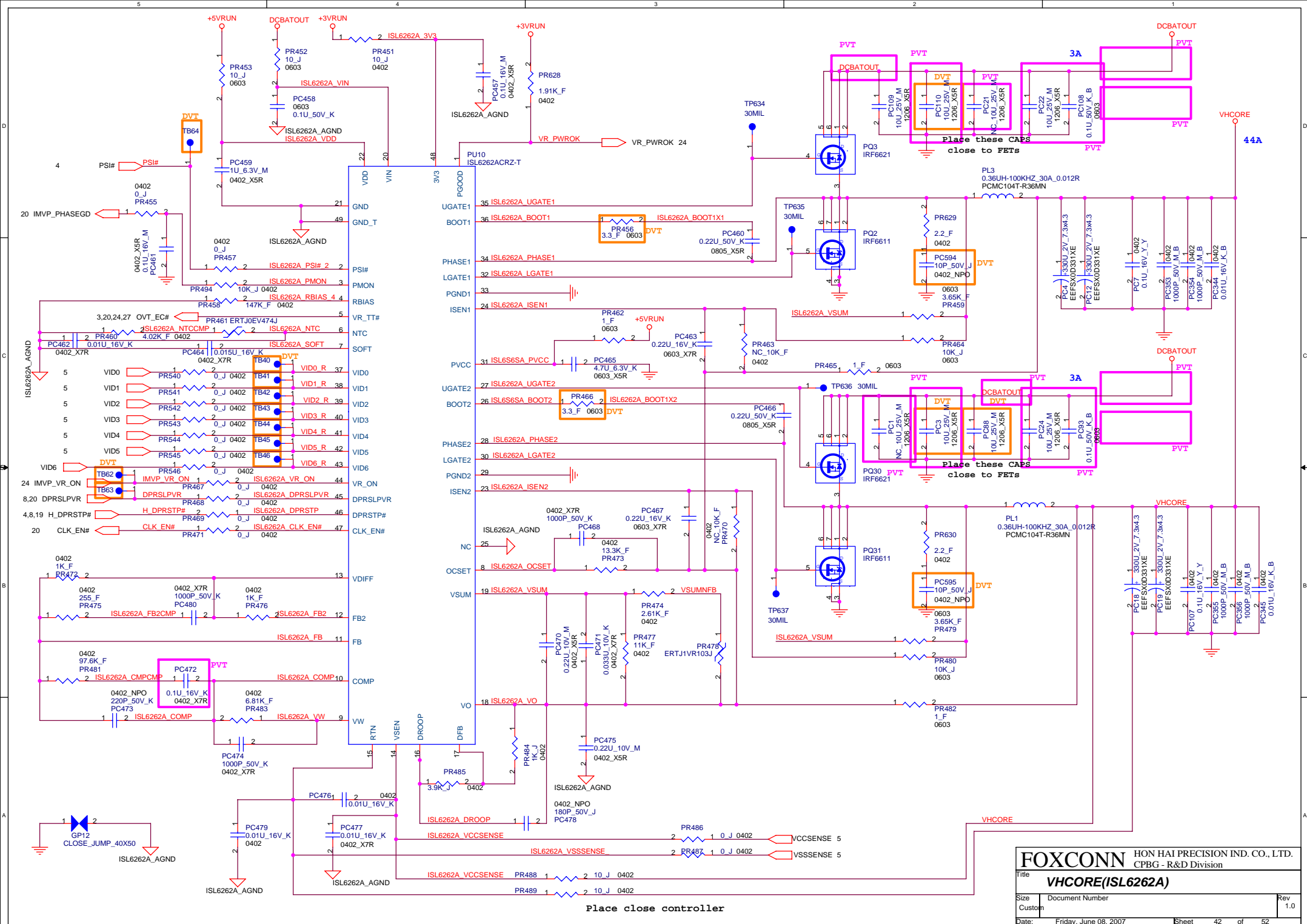


TON connect to GND = 5V/400KHZ, 3.3V/500KHZ  
 ILIM5/ILIM3 for setting OCP









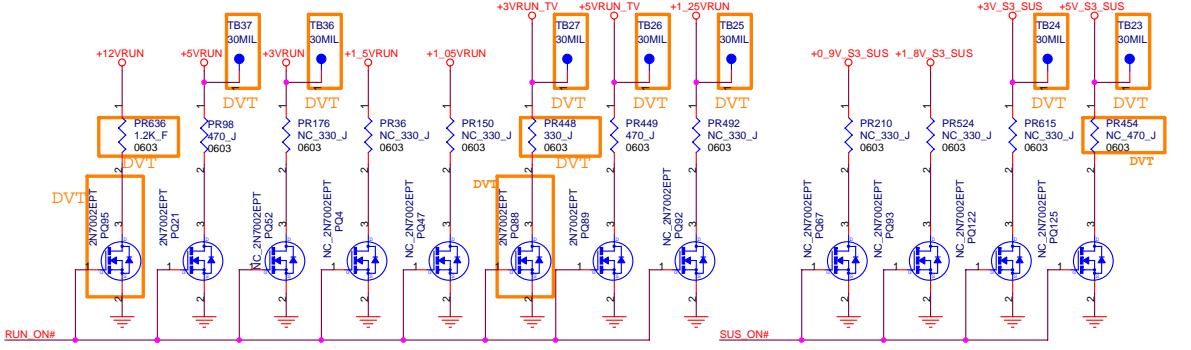
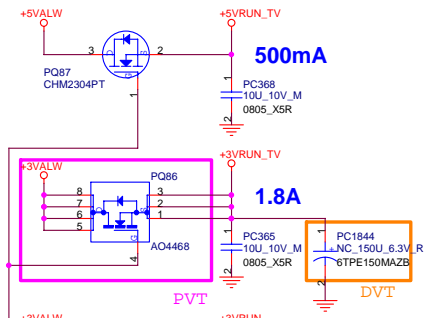
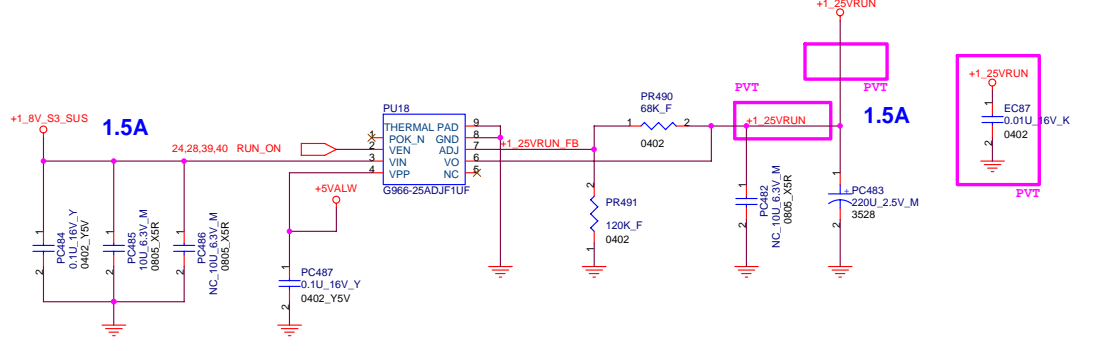
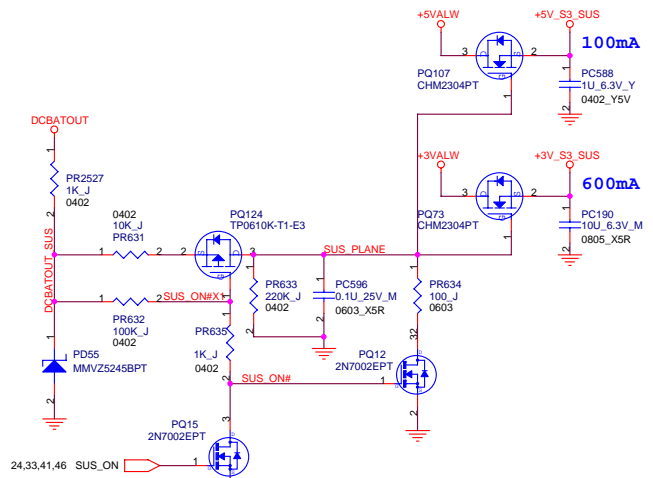
**FOXCONN** HON HAI PRECISION IND. CO., LTD.  
 CPBG - R&D Division

Title: **VHCORE(ISL6262A)**

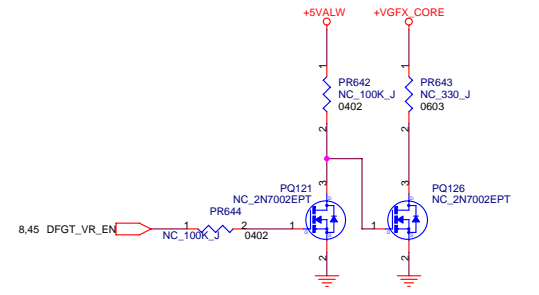
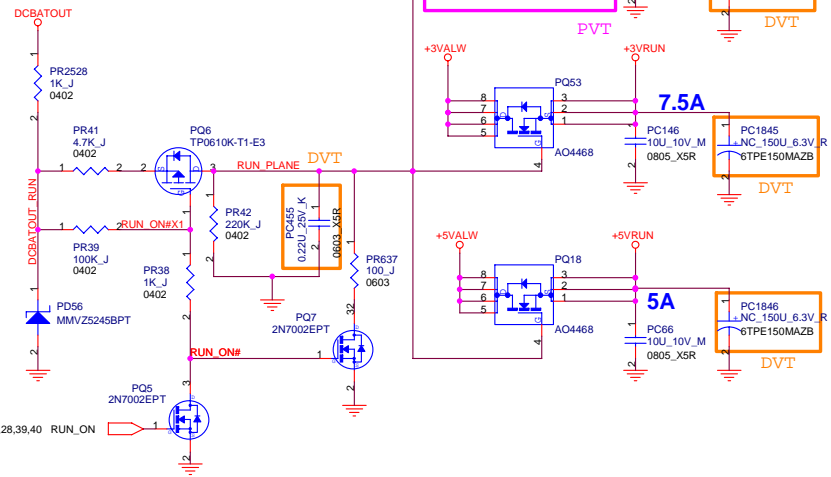
Size	Document Number	Rev
Custom		1.0

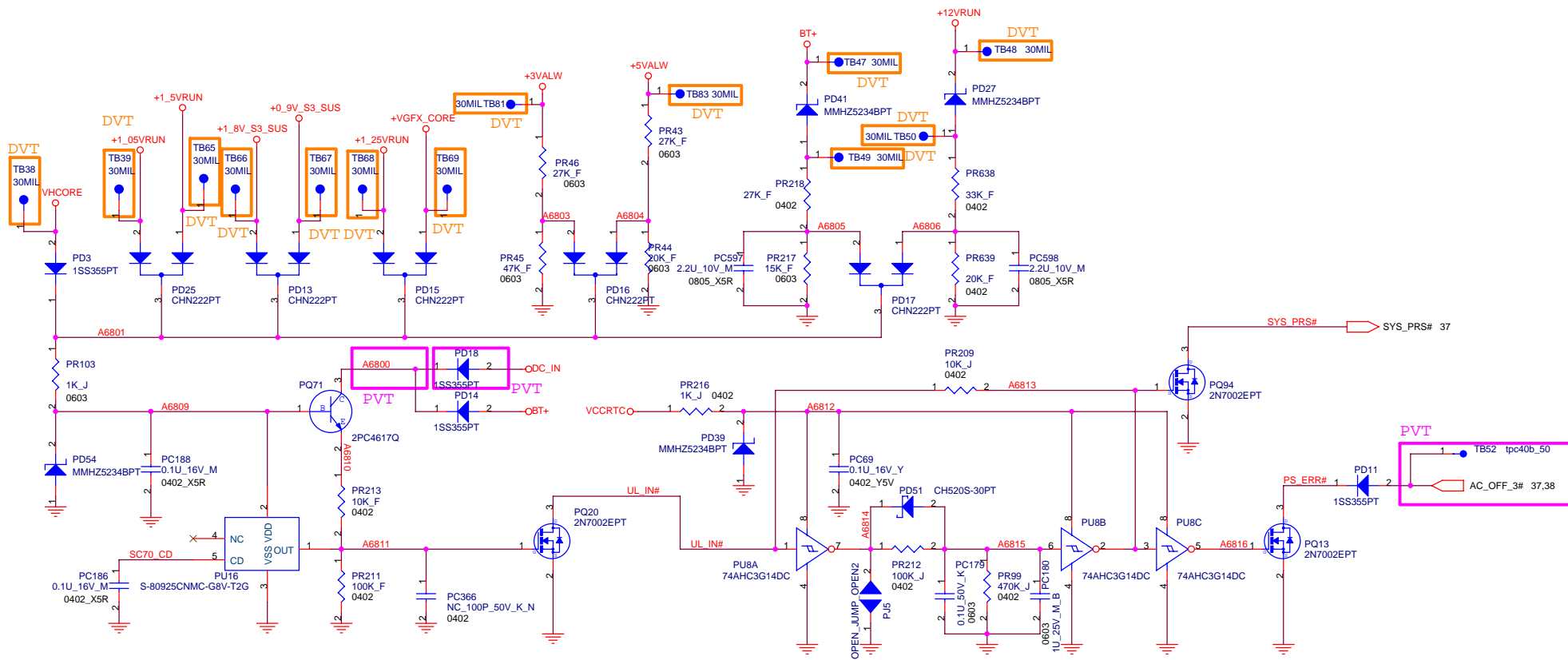
Date: Friday, June 08, 2007 Sheet 42 of 52

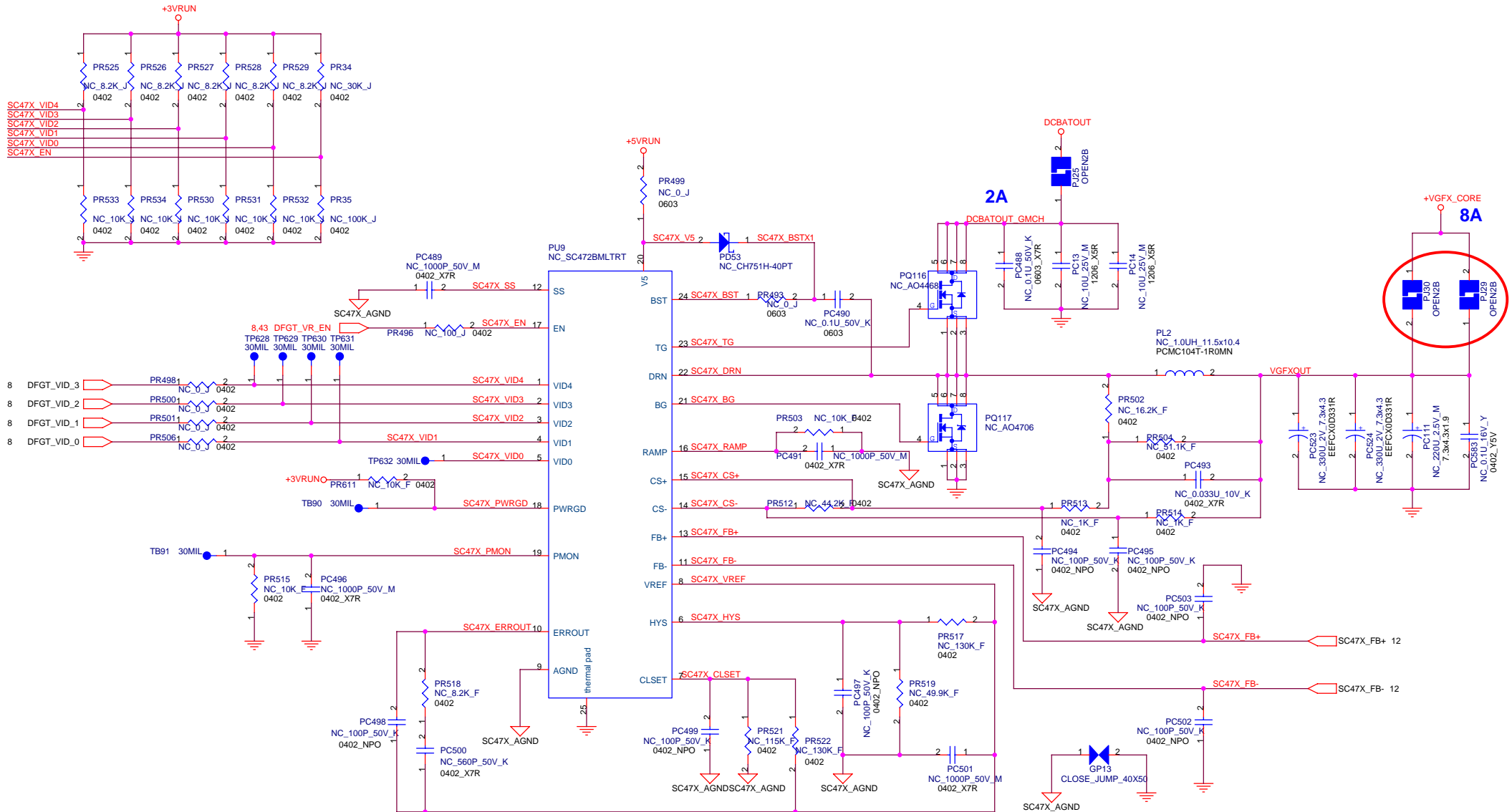
Place close controller



Discharge circuit for power-off

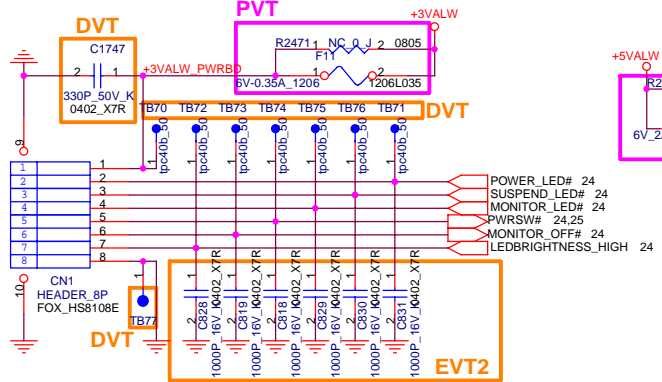






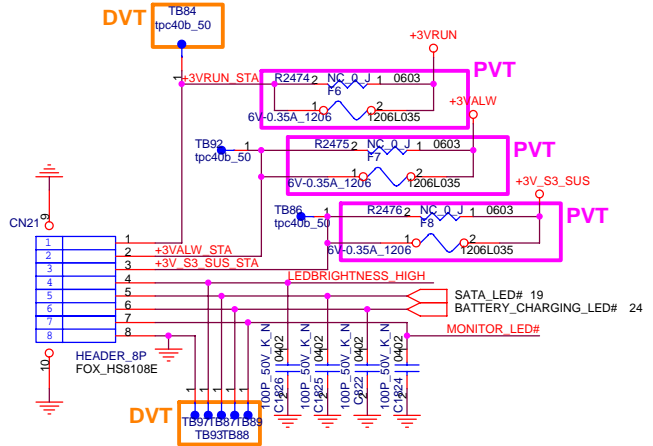
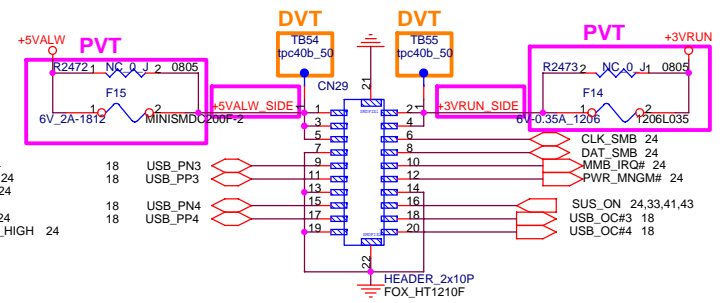
Dummy This page! (2007/03/28)

<b>FOXCONN</b> HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title <b>GMCH POWER</b>		
Size A3	Document Number <b>M620-L</b>	Rev 1.0
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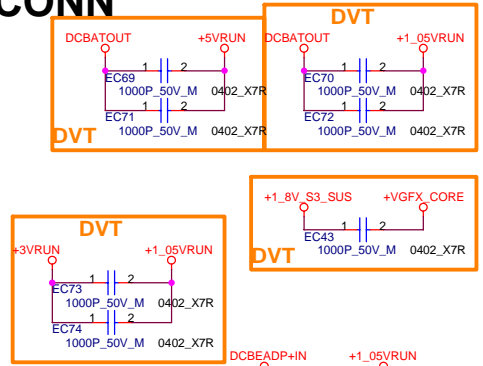
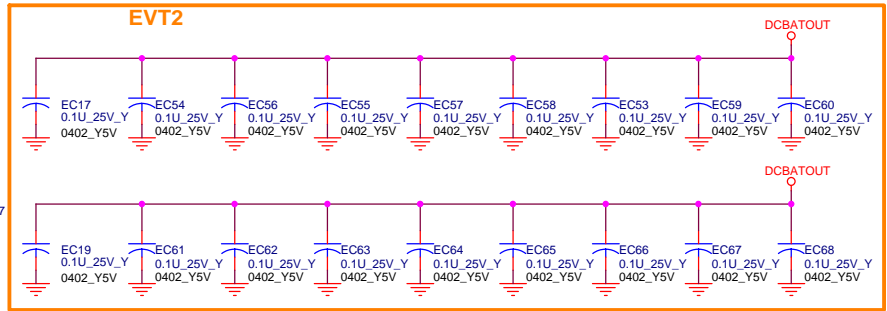
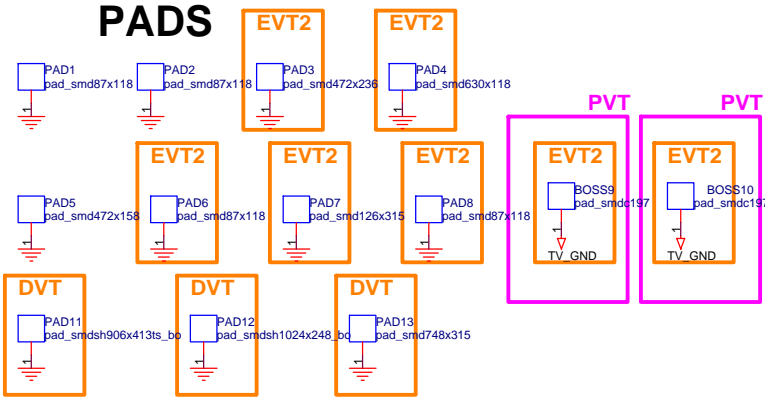
### Power LED/Power BTN

### SIDE USB CONN

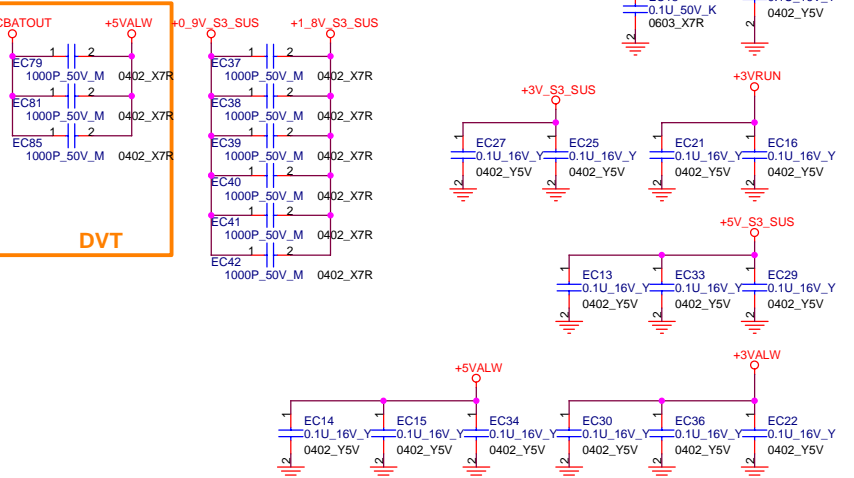
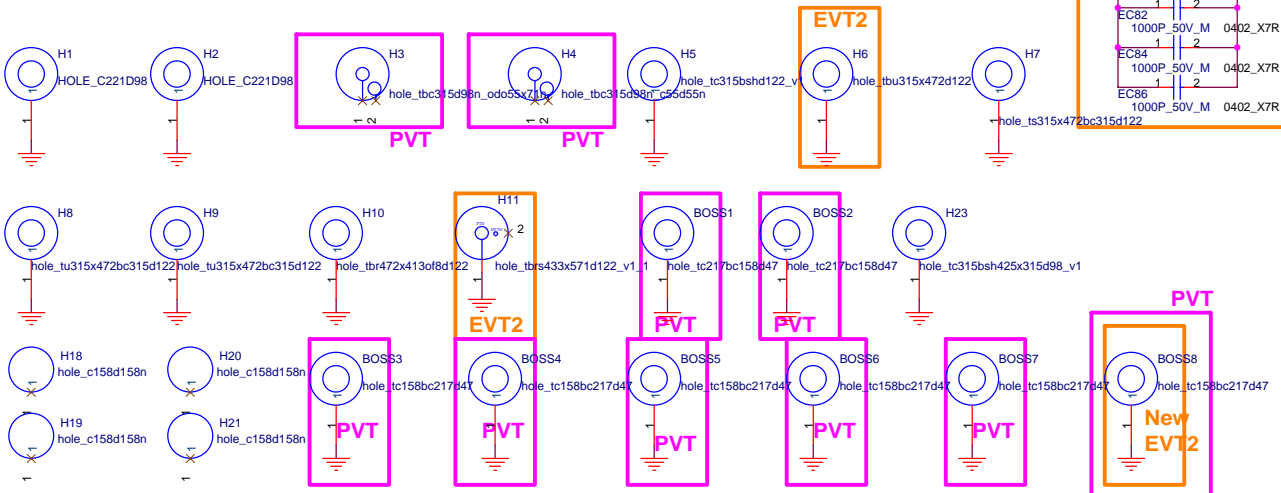


### STATUS LED CONN

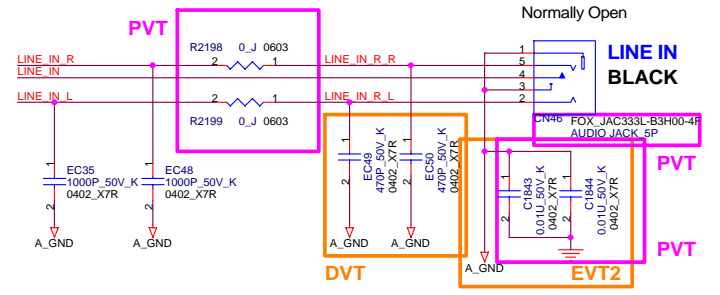
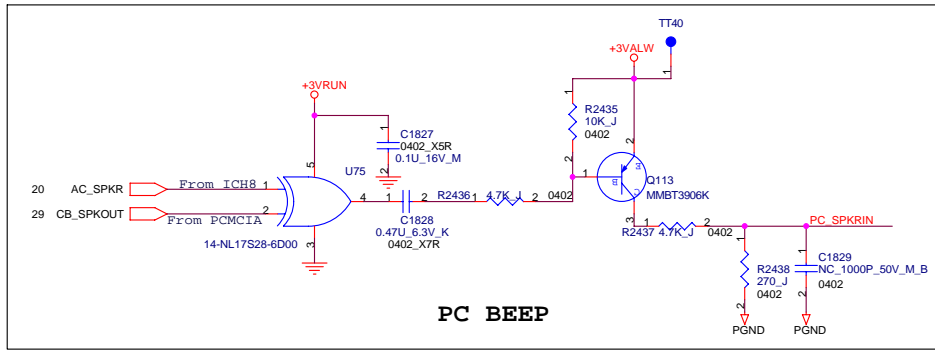
### PADS



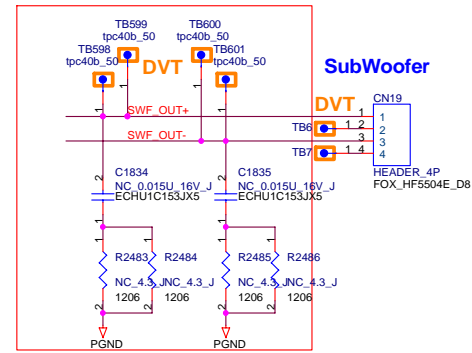
### HOLES



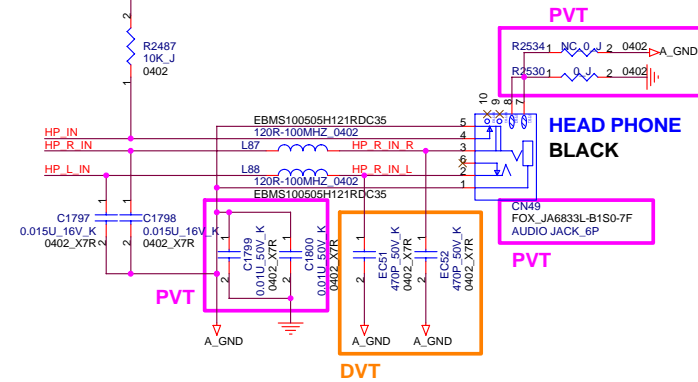
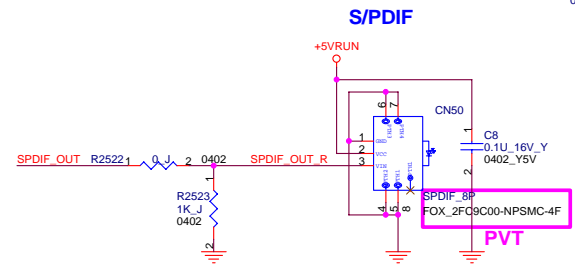
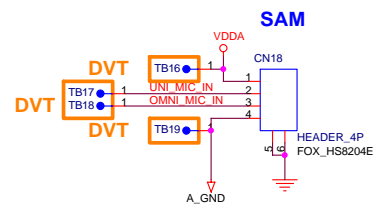
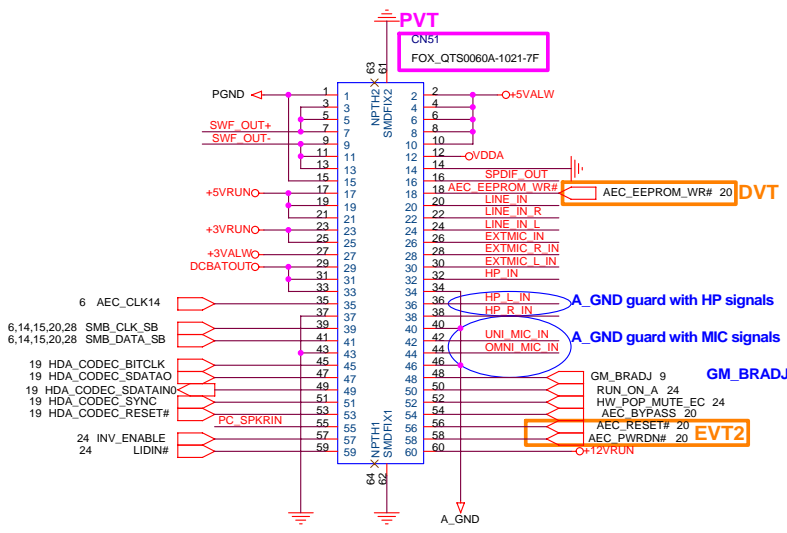
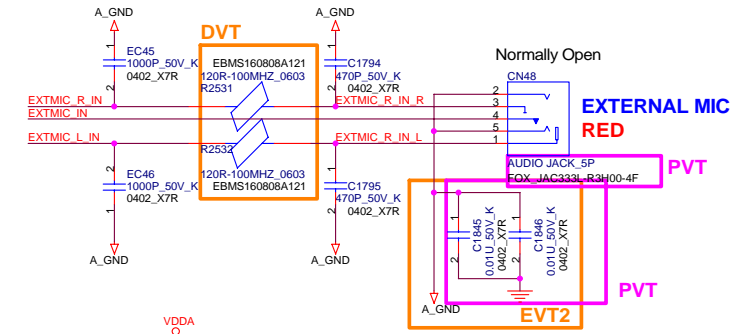
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Title <b>HOLE</b>			
Size A3	Document Number <b>M620-L</b>	Rev 1.0	
Date: Friday, June 08, 2007	Sheet 46	of 52	



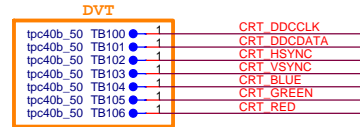
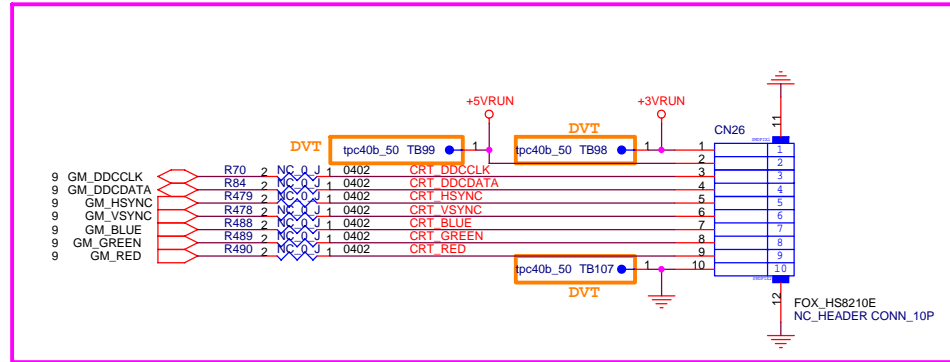
**C1834,C1835,R2483,2484,2485 and R2486 Dummy when Audio DB was placed**



1. Please place these components close to CN19
2. Trace: SWF\_OUT+/- and PGND layout width=40Mils



PVT





2006/12/15  
P.6:Change C1631,1633,1637,1639,1644,1646 from 25V to 6.3V range  
P.9:Add R1839 10K Ohm pull-down  
P.9:Add R1841 100K Ohm pull-down  
P.17:Add C1836-1841 dummy 10pF caps for EMI used  
P.17:Modify LVDS power from G5841 to G5281 and delete L91  
P.24:Exchange SPI ROM trace resistor R2411 for SDI and SDO  
P.25:Exchange SPI ROM SDI and SDO trace  
P.25:Dummy this page  
P.26:Dummy ISA ROM and ISA Debug port  
P.27:Add Power plane select function R632,636,637,2482 for customer request  
P.29:Change CN28 symbol  
P.30:Change R2491 from 1206 to 0603 size (sync to M630/640)  
P.34:Change back USB Power from SUS power to ALW power  
P.34:Update USB Vertical conn P/N  
P.35:Add +3VALW power R2163 0R Ohm for customer request  
P.35:Change back 1.8V to 2.5V power (follow vendor suggestion)  
P.36:Change CN45 from HS8104E to HS8108E  
P.36:Add R2504,2505 75R to GND for LAN Design rule  
P.47:Update all HOLES and PADS  
P.47:Change back Side-USB Power from SUS power to ALW power  
P.48:Delete U74 and net:CSDFIDF for customer request  
P.48:Change CN46,48 connector type=normal open and delete R2197,R2200

2006/12/16  
P.6:Delete R1994,L83-85,C1635,1641,1649 (By ICS FAE suggest)  
P.9:Change R1471 and R1475 from 39R to 30R(follow Schematic check list V1.5)  
P.20:Exchange GPIO24 and GPIO28 by S/W require  
P.24:Move R1930 to P.20 and change 47K to 10K(follow Schematic check list V1.5)  
P.24:Change GPIO pin by S/W require  
P.31:Update CN14 P/N  
P.32:Update CN32 P/N  
P.41:Delete PR602 and Add GP1  
P.41:Change PR601 package from 0603 to 0402  
P.43:Change PR468 from 499R to 0R(Double same serial resistor with R1939)  
P.47:Delete H16,17,22 and change H18-21 shape  
P.48:Update CN50 symbol

2006/12/19  
P.6:Delete PC29 (By Power require)  
P.27:Add Q118,Q119,R2508,R2509 and Change +3VALW power to +3V\_EMINI\_AUX power (Follow customer require)  
P.27:Delete Q117,R2499 and change R2498 from 470R to 68R (Follow Software Spec P.8)

2006/12/20  
P.20:Change SW4 from HDS406E to HDS404E  
P.20:Delete R2428,2429  
P.24:Add SW3  
P.24:Delete R2232  
P.24:Delete R2237,2240,2431,2433 and Change Model ID to System ID  
P.24:Change R2393,2239,2430,2432 from NC to 100K  
P.25:Add RP54 for SYSTEM ID4-7  
P.25:Delete R2481  
P.26:Delete CN12 PIN29 (JIG\_SMI#)  
P.33:Update CN43 P/N  
P.40:Update PQ55,56,57,58 Symbol  
P.44:Update PQ18,53 Symbol  
P.48:Change CN19 from SMD to DIP Type  
P.48:Update CN50 part description  
P.48:Add R2522,2523 and change CN50 AGND to GND (for customer require)

2006/12/21  
P.24:Change GPIO signal: R2507 is connect from WLAN\_EN# to HARD\_RST#  
P.24:Delete R2478 (Double Pull High)  
P.24:Add R2481 for EC strap  
P.24:Delete R1932 Pull-down resistor (HW\_POP\_MUTE\_EC)  
P.24:Change RP51 to R2526-2529 resistors  
P.27:Change Q32 type with ESD protection  
P.27:Change Q118 type (Change to meet SPEC)  
P.27:Change NET:MINI\_PCIE\_+1\_5V to MINI\_PCIE\_+1\_5VRUN  
P.27:Change MINI\_PCIE\_+3\_3V to MINI\_PCIE\_+3\_3VSUS  
P.27:Add C1842 (Follow customer require)  
P.39:Change PR622 connect Power from +5VALW to +ECVCC  
P.39:Move B\_PR2,B\_PC5 and B\_PD2 from ChargerBoard to MainBoard and rename to PR2526,PC1843 and PD29 (Follow customer require)  
P.42:Change PR193 from 6.8K to 5.49K (For OCP setting)  
P.42:Fix PU7 PGD signal=SUS\_PWRGD (Original is missing trace)  
P.43:Change PC464 P/N from 1C-2B20153-M000 to 1C-2B20153-K000 (BOM)  
P.47:Fix error CN21 Pin-7 from MONITOR\_OFF# to MONITOR\_LED#  
P.48:Change C1797,C1798 P/N from 1C-2B20153-M000 to 1C-2B20153-K000 (BOM)

2006/12/22  
P.17:Add L91 for EMI require  
P.20:Change SW4 from 4-DIP to 2-DIP SMD Switch  
P.24:Delete SW5  
P.33:Change CAP41 package (Power team require)  
P.35:Add L92,93 for EMI require  
P.36:Delete CN45 Pin9,10 net from GND\_TR to NC  
P.48:Add R2531 and R2532 for EMI require  
P.48:Add EC49 and EC50 for EMI require  
P.48:Add EC51 and EC52 for EMI require  
P.48:Move P.47 EC35,EC48 to this page and connect to LINE\_IN\_L and LINE\_IN\_R  
P.48:Move P.47 EC45,EC46 to this page and connect to EXTMIC\_R\_IN and EXTMIC\_L\_IN

2006/12/23  
P.44:Add PR2527,PD55 in SUS\_ON circuit (For power spec)  
P.44:Add PR2528,PD56 in RUN\_ON circuit (For power spec)

2006/12/25  
P.20:Add net name:ICH\_CLVREF0 and ICH\_CLVREF1 for layout  
P.29:L3 SWAP 1,4 and 2,3 (Layout issue)  
P.38:Fix CN20 NPTH connect to GND issue  
P.47:Update H10,H11 Hole symbol (ME modify)  
P.48:Change EC35,45,46 and EC48 from 0.01uF to 0.001uF (Customer require)  
P.48:C1834,C1835,R2483,2484,2485 and R2486 Dummy (Customer require same parts on the Audio board)

2006/12/26  
P.25:Change DAT\_35001,CLK\_35001 net name to DAT\_35001\_R1,CLK\_35001\_R1  
P.25:Delete TP612,TP620  
P.25:Add R2533 and R2536 for 2nd clear button GPIO use and Add net DAT\_35001\_R2,CLK\_35001\_R2  
P.46:Change PR496,PR498,PR500,PR501,PR506,PR35,PR532 to NC  
P.46:Change PR526,PR529,PR530,PR531,PR533 from NC to mount  
P.46:Change PR530,PR531,PR533,PR534 from OR to 10K  
P.47:Update H1,H2 footprint size (HOLE impact LVDS Connector issue)

2006/12/27  
P.11:Replace R1848,R205 (missing)  
P.19:Replace R2507 to +1\_05V\_PCIE (Missing)  
P.19:Delete R1919,C1585 and net:HDA\_CODEX\_BITCLK (Double components)  
P.20:Delete R1934,R1954,R1955,R2424 and exchange net to TP569,TP570,TP571,TP572 (EC change)  
P.24:Delete this Page (For customer require)  
P.25:Swap RP52 Pin3,4 net  
P.25:Move SW4 and GP2 to EC side,And change pull-up power from +ECVCC to +3VRUN  
P.25:Add R2506,R2507 for SYSTEM\_ID  
P.26:Delete SPI ROM and SPI Debug port circuit (For customer require)  
P.48:Change CN51 Pin33 from GND to DCBATOUT (For customer new panel spec infomation)

2006/12/28  
P.3:Change R1757 from 4.7K to 47K (EC change)  
P.25:Change R2210,R2212 Pin-1 net from CLK/DAT\_SMB to CLK/DAT\_SMB\_EC2  
P.25:Change Q109 from +ECVCC to +5VALW  
P.39:Change PD29,PR2526 and PC1843 to dummy  
P.48:Swap CN51 Pin36,38 net (For layout)

2006/12/29  
P.8:Delete TP584 (Layout issue)  
P.25:R2103,R2104,R2534,R2535 Dummy and R2210,R2212,R2533,R2536 Mount (For Clear Button Interface)  
P.47:Delete EC26

2007/02/03  
 Del P.24 (Winbond EC) page and add History for EVT2  
 P.19:Change net name TP\_GPIO34 to MB\_FLASH\_EN  
 P.20:Change net name MB\_FLASH\_EN to TP375  
 P.20 and P.48:Rename GPIO20 from AEC\_PWRDN# to AEC\_RESET#  
 P.20:Del TP596 and rename GPIO24 to AEC\_PWRDN#  
 P.25:Add R2537,R2538 pull-down for EC strap  
 P.25:Del TP621  
 P.26:Change LED 2 type (Customer require)  
 P.39:Add PL17 and PL18 (Power issue)  
 P.39:Add PC1847,PC1848 and PC1849 (Power issue)  
 P.40:Change PR627 from 0R to 3.3R (Power issue)  
 P.40:Change PR601 from 604K to 300K (Power issue)  
 P.42:Change PR485 from 3.3K to 3.9K (Power issue)  
 P.43:Add PC1844,PC1845 and PC1846 (Power issue)  
 P.43:Change PR615.1(+5V\_S3\_SUS) to (+3V\_S3\_SUS)  
 P.45:Change PR526,PR611,PR499 and PR34 to NC  
 P.47:Del GP24 and add C1843,C1844 (For EMI issue)  
 P.47:Del GP25 and add C1845,C1846 (For EMI issue)  
 P.48:Rename RUN\_PWRGD to AEC\_PWRDN#

2007/02/07  
 P.42:Add TP634~TP637 for Power test use  
 P.47:Add EC53~EC68 for EMI require  
 P.47:Change EC17 and EC19 from DCBEADP+IN to DCBATOUT

2007/02/08  
 P:47:Change CN49 Pin7,8 from A\_GND to GND (Customer require)

2007/02/09  
 P.28:Change CN4 type from HS8204E to HS8104E  
 P.29:Add PJ37-42 open jumper for EMI require  
 P.46:Change CN21 type from HS8208E to HS8108E  
 P.46:Change PAD3,4 type and add PAD6,7,9,10 for ME require  
 P.46:Change H3,H4,H6,H11 type and add H29 for ME require

2007/02/26  
 P.39:Change PC139,PC159,PC160,PC341,PC346,PC347 from NC to mount  
 P.39:Change PC147 from 330uF to 150uF  
 P.40:Change PR627 from 0R to 3.3R  
 P.40:Change PR601 from 604K to 300K  
 P.41:Change PC343,PC351,PC352 from NC to mount  
 P.42:Change PR485 from 3.3K to 3.9K  
 P.42:Change PC7,PC107,PC344,PC345,PC353,PC354,PC355,PC356 from NC to mount

2007/02/28  
 P.5:Change CAP25 P/N (substitute materiel)  
 P.11:Change D22,L58,L66,L75,L76,CAP26,CAP28,CAP31 P/N (substitute materiel)  
 P.12:Change CAP34,CAP36 P/N (substitute materiel)  
 P.19:Change D24 P/N (substitute materiel)  
 P.20:Change R2443 from 0R to 10K (Intel spec)  
 P.21:Change D25,D26,CAP38 P/N (substitute materiel)  
 P.29:Change L55,L56 P/N (substitute materiel)  
 P.33:Change CAP19,CAP20,CAP22 P/N (substitute materiel)  
 P.35:Change U67 P/N (substitute materiel)  
 P.38:Change PL11,PL14,PL15,PL16 P/N (substitute materiel)  
 P.39:Change PL17,PL18 P/N (substitute materiel)  
 P.40:Change PC23,PC589,PC574,PC576,PC577 P/N (substitute materiel)  
 P.41:Change PC144,PC148 P/N (substitute materiel)  
 P.43:Change PC1844,PC1845,PC1846 P/N (substitute materiel)  
 P.45:Change PC523,PC524 P/N (substitute materiel)  
 P.47:Change U75,L87,L88 P/N (substitute materiel)

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2007/03/08  
P.3:Change Q3 P/N (Buyer require)  
P.6:Update U33 symbol from ICS9LPR358YGLFT to ICS9LPR358AGLFT  
P.17:Change CN3 type for cost down  
P.24:Change R2538 from 47K to 100K  
P.27:Swap U27(G781),U68(G781-1) for S/W require  
P.28:Change CN27,CN28 form normal type to reverse type (Customer require)  
P.28:Change R2409 to NC and change R2410 to mount (Follow M6340)  
P.28:Add TB94,TB95,TB96 (For BFT)  
P.28:Mirror vertical L4,L5 (For layout require)  
P.29:Change Q47 P/N (Buyer require)  
P.32:Change CN43,CN44 form normal type to reverse type (Customer require)  
P.33:Change U70,U71,U72 package (EUV spec require)  
P.39:Dummy PL17,PL18 (Cost down)  
P.43:Dummy PR454,PQ88

2007/03/13  
P.6:Modify R2022.1 connection from AEC\_CLK14 to R\_CLK\_ICH14  
Page:All:Add Test point for BFT

2007/03/16  
P.24:Change RP52 from 10K to 4.7K (To meet S/W spec)  
P.24:Swap SMB-1 and SMB-2 signals  
P.28:Change R152,R154,R136,R137,R482,R449,R105,R90 from NC to mount  
P.28:Change L3,L4,L5,L9 from mount to NC  
P.32:Change back CN44 symbol (ME turn 180drgee)  
P.34:Del L92,L93 and change to R92,R93

2007/03/20  
P.2:Update Block Diagram  
P.24:Change R519,R521,R2445,R2446 from 10K to 4.7K (To meet S/W spec)

2007/03/22  
P.39:Change PR192,PR198 from 0R to 3.3R (For EMI issue)  
P.41:Change PR195 from 0R to 3.3R (For EMI issue)  
P.42:Change PR456,PR466 from 0R to 3.3R (For EMI issue)  
P.42:Add TB62,TB63 (Power request)  
P.42:Change TT20,TT21,TT22,TT23,TT24,TT25,TT26 to TB40,TB41,TB42,TB43,TB44,TB45,TB46 (Power request)  
P.43:Add TB23,TB24,TB25,TB26,TB27,TB36,TB37 (Power request)  
P.44:Change TP:TT45,TT46,TT57,TT16,TT17,TT18,TT19,TT44,TT43,TT42,TT32,TT41 to TB38,TB39,TB65,TB66,TB67,TB68,TB69,TB81,TB83,TB47,TB49,TB50,TB48 (For BFT test)  
P.46:Add EC43,EC69-74,EC78-82,EC84-86 for decrease noise  
P.47:Change R2531,R2532,R2198,R2199 from 0R resister to 120R-100MHZ bead (EMI Request)  
P.47:Change EC49,EC50,EC51,EC52 from NC to Mount(EMI Request)

2007/03/23  
P.17:Change back CN3 connector type to EVT used  
P.23:Add C674 (EMI Request)  
P.41:Change PC166,PC170 from NC to mount (EMI Request)  
P.42:Add bead PL19,PL20 (EMI Request)  
P.46:Add cap C1747 (EMI Request)  
P.46:Add cap EC6,EC7 (EMI Request)

2007/03/26  
P.8:Add C1453 (For power test fail)  
P.19:Change R1918 from NC\_47R to 0R (EMI Request)  
P.19:Change C1584 from NC to mount (EMI Request)  
P.24:Correct SMBUS Definition  
P.28:Change R2253 from NC\_47R to 0R (EMI Request)  
P.28:Change C1818 from NC to mount (EMI Request)  
P.32:Change CN43 type (ME new tooling)  
P.38:Move PF1 from right side to left side of PL11 and PL15  
P.43:Change PR448,PR636,PQ88,PQ95 from NC to mount (For discharge too slow)  
P.46:Add PAD11,PAD12,PAD13 (RF Request)  
P.46:Change all TestPoint from 30mils to 40mils (For BFT test)  
P.47:Change CN50 type (ME new tooling)

2007/03/27  
P.11:Del L66,L67,L70,L73,C1517,C1518,C1520,C1527,R2419 (Intel Layout Guide V2.0)  
P.11:Modify VCCA\_TVA/B/C\_DACL/2 circuit (Intel Layout Guide V2.0)  
P.19:Change BAT1 TestPoint type to 40mils  
P.23:Change CN5 TestPoint type to 40mils  
P.26:Change WOL function form S5 to S3 status  
P.27:Change CN2 TestPoint type to 40mils  
P.28:Change CN35 TestPoint type to 40mils  
P.28:Change CN4 TestPoint type to 40mils  
P.28:Update CN52 connector  
P.28:Stuff R2253,C1818 (For EMI request)  
P.35:Change CN45 TestPoint type to 40mils  
P.38:Change PCN1 TestPoint type to 40mils  
P.40:Add RUN\_ON net and PR580 for power sequency  
P.40:Change PR579 from stuff to NC (For can't boot from ext debug board issue)  
P.47:Change CN18,CN19 TestPoint type to 40mils  
P.48:Change CN26 TestPoint type to 40mils

2007/03/29  
P.20:Change R2494 from 4.7K to 1K (Follow M6340)  
P.20:Change R2440 from 4.7K to 1K (Follow M6340)  
P.24:Add TestPoint for BFT test  
P.24:Change C30,C33 from 10pF to 12pF (Vendor suggest)  
P.37:Add TestPoint for BFT test

2007/03/30  
P.21:Change L79 from 10uH choke to 330R bead (Follow intel schematic)

2007/03/31  
P.40 Add PC600 for power leakage issue (Default is NC)  
P.40 Add PD26 for power leakage issue (Default is NC)

2007/04/02  
P.08:Add R1803 to isolate PM\_THRMTRIP#\_R side (Intel sighting report #30678)  
P.19:Add R1910 for reserve disable ThermalTrip function  
P.24:Add R415,R416,R417,R418 for FAN PWM layout path select  
P.27:Add R411,R412,R413,R414 for FAN TACH layout path select  
P.41:NC PC154 (Power reserved)

2007/04/03  
P.42:Change PC472 type for cost and common parts  
P.47:Add R2530,R2534 for ground path select (Customer request and default is connect to A\_GND)

2007/04/04  
P.8:Change R1803 from NC to stuff  
P.42:Change PC594,PC595 P/N from +/-10% to +/-5%

2007/04/18  
P.26:Change LED2 color from Green to Yellow Green  
P.39:Change PR78,PR82 from 68K to 82K (3/5V power limit up)  
P.42:Dummy PC110,PC3 and mount PC21,PC88 (Power request)  
P.43:Change PC1844,PC1845,PC1846 from 220uF/2.5V to 150uF/6.3V (Spec error)  
P.47:Change CN50 type from high-speed to low-speed (Customer request)

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