SW9 (14") BLOCK DIAGRAM

01

PCB STACK UP

6L Dis. & UMA

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : BOT

CPU
Arrandale 45nm processor
PAGE 3~6

DDRIII-SODIMM1 PAGE 12 — DDRIII 800/1066 MT/s, 1333MT/s CFD only

DDRIII-SODIMM2 PAGE 13 — DDRIII 800/1066 MT/s, 1333MT/s CFD only

PCI-Express 16X

27MHz

nVIDIA (40nm)
N11M-GE1 512MB
64 Bit
533p
PAGE 14~18

HDMI CON PAGE 20

CRT PAGE 20

Dual Link

LCD CONN PAGE 19

DMI LINK

32.768KHz 25MHz

HDMI Level Shifter
Chrontel CH7318C-BF-TR
PAGE 2

CRT
LVDS

SATA - HDD PAGE 25 — SATA0 150MB

SATA - CD-ROM PAGE 25 — SATA1 150MB

E-SATA PAGE 26 — SATA5 150MB

PCH
Ibex-M(Intel HM55)
PAGE 7~11

CLOCK GEN
9LRS3197
PAGE 2
14.318MHz

Mini PCI-E Card x2
Express Card x1
6,8,10

USB2.0

0,1,2 USB2.0 Ports X2 PAGE 21

12 BlueTooth PAGE 22

5 Webcam PAGE 19

4 RTS5159 PAGE 21

PCI-E

X1 Mini PCI-E Card (Wireless LAN / Robson) PAGE 28

SIM Card PAGE 28

X1 LAN Atheros PCIE-LAN AR8131(M) GagaLAN PAGE 24

25MHz

RJ45/RJ11 PAGE 24

X1 Express Card

32.768KHz

Keyboard PAGE 26
Touch Pad PAGE 25

ENE KBC
KB3926 C0
PAGE 27

LPC

GMT G9931P1U FAN PAGE 26

SPI PAGE 27

SPI PAGE 7

MDC CONN PAGE 23

Azalia

Analog
ALC272
PAGE 22

microphone PAGE 22

Audio Jacks (Phone/ MIC) PAGE 22

AUDIO Amplifier TPA6017A2 PAGE 23

Jack to Speaker PAGE 23

- UMA GPU CORE (RT8152A) PAGE 31
- SYSTEM POWER RT8206B PAGE 32
- VCCP +1.1VTT(RT8208A) AND PCH 1.05V(RT8204) PAGE 33
- CPU CORE ADP3212 PAGE 34
- VGACORE(1.025V) RT8208A PAGE 35
- DDR III SMDDR_VTERM 1.5V/1.5VSUS(RT8207) PAGE 36
- SYSTEM CHARGER(ISL6251AHAZ-T) PAGE 38

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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CLOCK GENERATOR

+1.05V L28 HCB1608KF-181T15_6 +VDDIO_CLK

C640 .1U/10V_4
C644 .1U/10V_4
C643 10U/6.3V_6S
C642 *10U/6.3V_6S

Place each 0.1uF cap as close as possible to each VDD IO pin. Place the 10uF caps on the VDD_IO plane.

U17 RTM875N-632-GRT QFN32

+3V
C646 4.7U/6.3V_6
C654 4.7U/6.3V_6
C652 .1U/10V_4
C641 .1U/10V_4
C645 .1U/10V_4
C651 .1U/10V_4
C653 .1U/10V_4

+VDDIO_CLK

VDD_USB VDD_LCD VDD_SRC VDD_CPU VDD_REF VDD_CPU_IO VDD_SRC_IO SDATA SCLK CPU_STOP# REF_0/CPU_SEL CK_PWRGD/PD#_3.3 XOUT XIN VSS_SATA VSS_USB VSS_LCD

CPU-0 CPU-0# CPU-1 CPU-1# DOT96T_LPR DOT96C_LPR SRC-1 SRC-1# SATA SATA# 27MHz_nonSS 27MHz_SS GND VSS_REF VSS_CPU VSS_SRC

CLK_BUF_BCLK_P [8]
CLK_BUF_BCLK_N [8]
133 or 100 Mhz output to PCH

CLK_BUF_DREFCLK [8]
CLK_BUF_DREFCLK# [8]
96Mhz output for generate 48Mhz (USB) and 24 Mhz (HDA)clk

CLK_BUF_PCIE_3GPLL [8]
CLK_BUF_PCIE_3GPLL# [8]
100Mhz output for DMI reference clk

CLK_BUF_DREFSSCLK [8]
CLK_BUF_DREFSSCLK# [8]
100Mhz output for SATA reference clk

CLK_VGA_27M_NONSS R280 *33_4
CLK_VGA_27M_SS R278 *33_4
Discrete Only
CLK_27M_NONSS [16]
CLK_27M_SS [16]

C647 18P/50V_4 EMI 11/26

[8,12,13] CGDAT_SMB
[8,12,13] CGCLK_SMB

[8] CLK_ICH_14M R273 10K/F_4 R295 33_4 CPU_SEL
C389 10P/50V_4 EMI 11/26

CK_PWRGD_R
XTAL_OUT
XTAL_IN

Place the 33 ohm resistors close to the CK 505

+3V R297 1K/F_4 CK_PWRGD_R
Q28 2N7002E
[34] VR_PWRGD_CLKEN#
R298 100K/F_4

Y3 XTAL_IN XTAL_OUT 14.318MHZ
C388 33P/50V_4
C387 33P/50V_4

+3V R294 *10K/F_4 CPU_SEL R296 10K/F_4

	0	1
CPU_SEL	CPU0/1=133MHz (default)	CPU0/1=100MHz

CPU bracket Hole.

H19 *h-c256d165p2
H20 *h-c256d165p2
H35 *h-c256d165p2
H34 *h-c256d165p2

PAD and HOLE

H31 *h-s276d118p2
H7 *H-C236D162P2
H17 *h-c315d118p2
H11 *h-c315d118p2
H12 *h-c315d118p2
H36 H-C236D63P2
H5 *O-SW9-4
AGND
H24 *H-c98d98n
H9 *O-sw9-2
H10 *O-sw9-3
H21 *O-sw9-5
H22 *O-sw9-5

MINI CARD Hole.

H6 *H-C236D162P2
H8 *H-C236D162P2
H2 *H-C236D63P2
H1 *H-C236D63P2

MDC Hole.

H40 H-C236D62P2
H39 H-C236D62P2

EMI capacitive

+VIN 10/12
C336 .1U/25V_4
C481 .1U/25V_4
C565 .1U/25V_4
C570 .1U/25V_4
C572 .1U/25V_4
C637 .1U/25V_4
C638 .1U/25V_4
C639 .1U/25V_4
EMI
C378 *.22U/10V_4
C350 *.22U/10V_4
C374 *.22U/10V_4
+3VO
C31 *.1U/10V_4
C323 *.1U/10V_4
C133 *.1U/10V_4
C427 *.1U/10V_4

VGA bracket Hole.

H14 *h-c256d165p2
H15 *h-c256d165p2

H37 H-C236D63P2
H16 *h-c315d118p2
H13 *h-c315d118p2
H38 *H-C315D118P2
H32 *o-sw9-7
H18 *h-c315d118p2
H33 *o-sw9-6

PAD2 MDC_SPRING
PAD3 MDC_SPRING
PAD6 MDC_SPRING
PAD4 MDC_SPRING
PAD5 MDC_SPRING
PAD1 *EMI PAD
PAD7 *EMI PAD
PAD8 *PAD-RE406X157
H3 *h-o110x130d110x130n
H4 *h-o039x102d39x102n

[7,8,9,11,27,31,33,34,39] +1.05V
[3,7,8,9,10,11,12,13,19,20,21,22,23,24,25,26,27,28,29,30,34,37,39] +3V

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK & Screw Holes	1A

Date: Wednesday, December 02, 2009 Sheet 2 of 44

	DIS	UMA
Ra	NA	0 ohm
Rb	0 ohm	NA
Rc	0 ohm	NA

03

U22A

DMI

Intel(R) FDI

PCI EXPRESS -- GRAPHICS

IC,AUB_CFD_rPGA,R1P0

2.7GT/s data rate

Discrete Only

FDI_FSYNC can gang all these 4 signals together and tie them with only one 1K resistor to GND (Check list 1.0).

U22B

MISC

THERMAL

CLOCKS

DDR3 MISC

PWR MANAGEMENT

JTAG & BPM

IC,AUB_CFD_rPGA,R1P0

For ITP CLk

JTAG MAPPING

Scan Chain (Default)	STUFF -> R97, R89, R90 NO STUFF -> R84, R512
CPU Only	STUFF -> R97, R84 NO STUFF -> R89, R512, R90
GMCH Only	STUFF -> R512, R90 NO STUFF -> R97, R84, R89

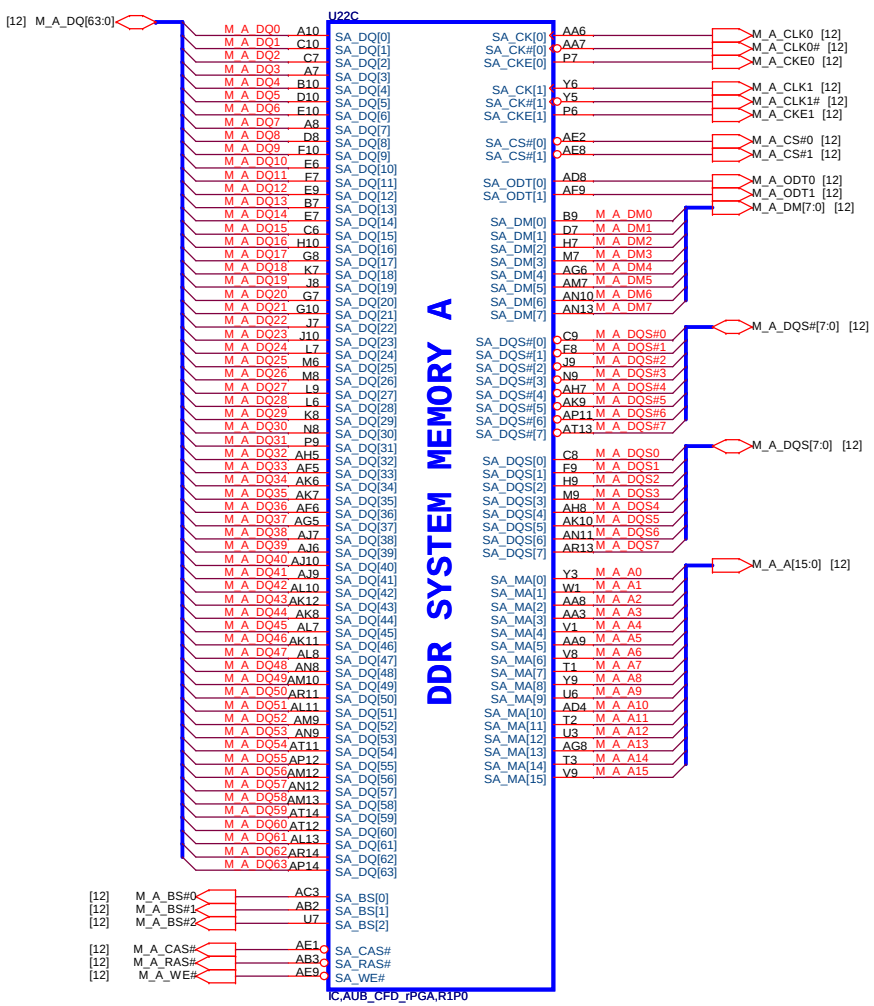
Use a voltage divider with VDDQ (1.5V) rail (ON in S3) and resistor combination of 4.75K (to VDDQ)/12K(to GND) to generate the required voltage.
Note: CRB uses a 3.3V (always ON) rail with 2K and 1K combination.

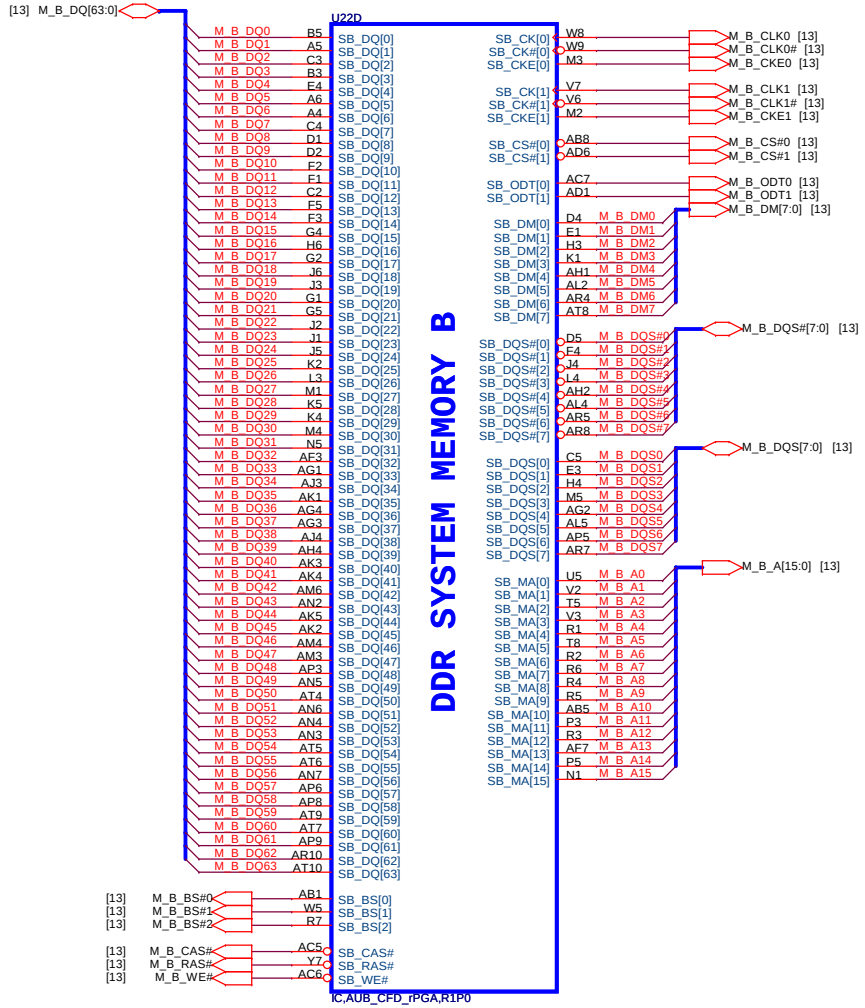
PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 1/4(HOST&PEX)	1A

Date: Wednesday, December 02, 2009 Sheet 3 of 44

AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)





PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 2/4(DDR)	1A

Date: Wednesday, December 02, 2009 Sheet 4 of 44

	DIS	UMA
Rc	NA	4.7K
Rd	NA	0 ohm
Re	NA	0 ohm
Rf	NA	NA

	DIS	UMA
Ra	0 ohm	NA

Please note that +VCC_GFX_CORE should be 1.05V in Auburndale

VTT Rail Values are
Auburndal VTT=1.05V
Clarksfield VTT=1.1V

H_VTTVID1=Low, 1.1V
H_VTTVID1=High, 1.05V

HFM_VID : Max 1.4V
LFM_VID : Min 0.65V

10/12

10/05

7/22

U22F — IC,AUB_CFD_rPGA,R1P0

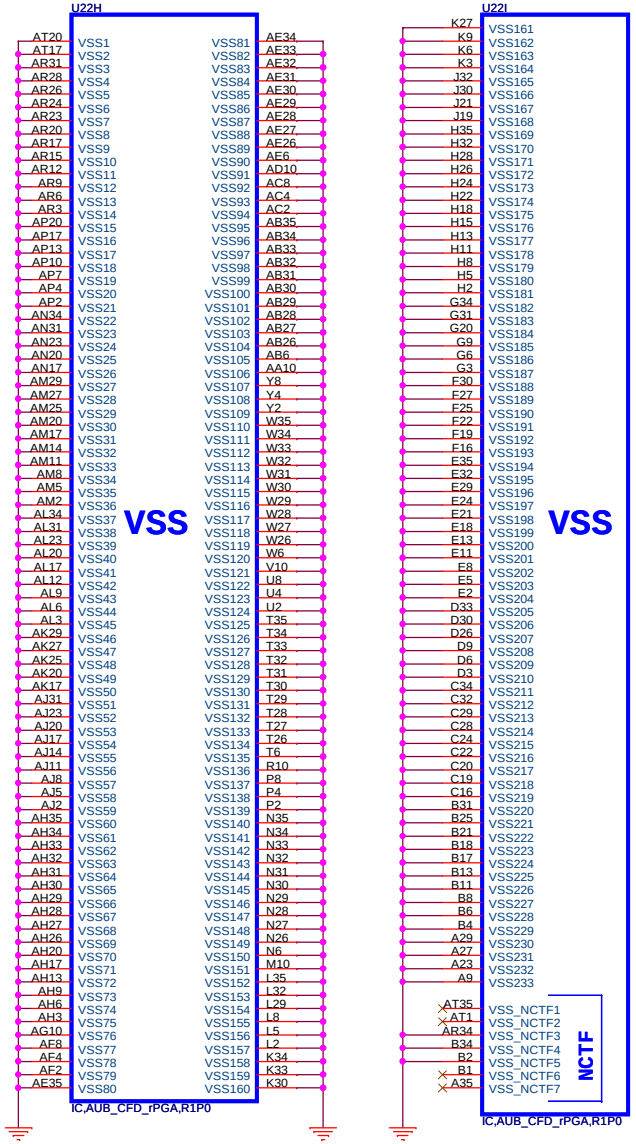
U22G — IC,AUB_CFD_rPGA,R1P0

PROJECT : SW9
Quanta Computer Inc.

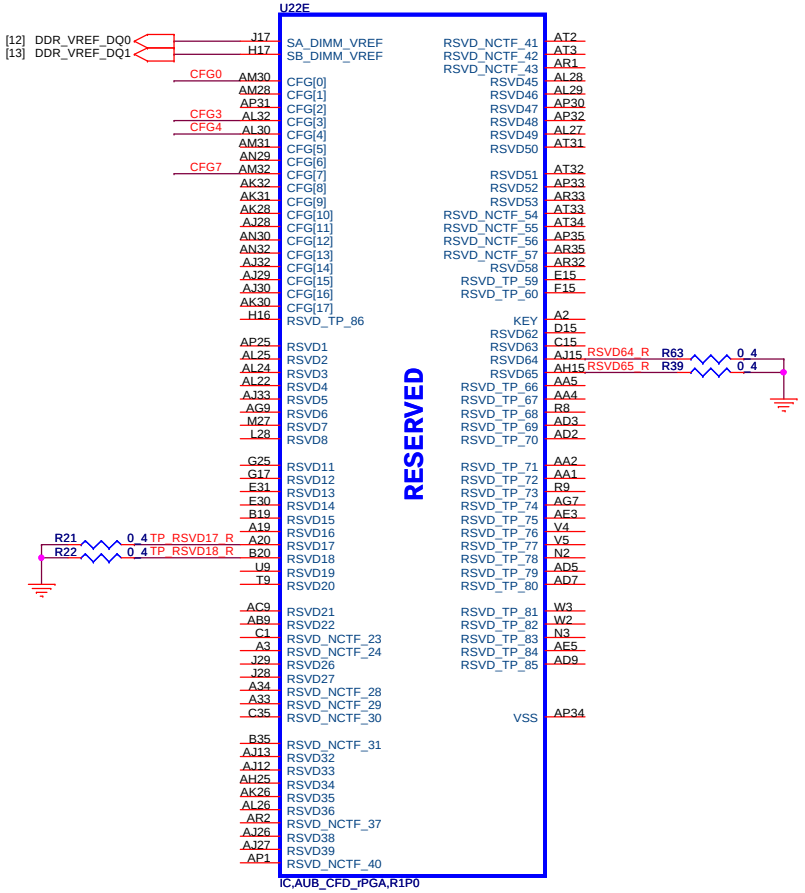
Size	Document Number	Rev
Custom	PROCESSER 3/4(POWER)	1A

Date: Wednesday, December 02, 2009 Sheet 5 of 44

AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



For discrete only

CFG[1:0] - PCI_Epress Configuration Select
*** 11= 1 x 16 PEG**
*** 10= 2 x 8 PEG**

	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed 15 -> 0 , 14 -> 1

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PROCESSER 4/4(GND)	1A

Date: Wednesday, December 02, 2009 Sheet 6 of 44

INTVRMEN - Integrated SUS 1.1V VRM Enable
High - Enable Internal VRs

IBEX PEAK-M (HDA,JTAG,SATA)

U29A

Ibex-M 1 OF 10

RTC
RTCX1
RTCX2
RTCRST#
SRTCRST#
INTRUDER#
INTVRMEN

LPC
FWH0 / LAD0
FWH1 / LAD1
FWH2 / LAD2
FWH3 / LAD3
FWH4 / LFRAME#
LDRQ0#
(+3V) LDRQ1# / GPIO23
SERIRQ

SATA HDD1
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP

SATA ODD
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP

SATA
SATA3RXN
SATA3RXP
SATA3TXN
SATA3TXP
SATA4RXN
SATA4RXP
SATA4TXN
SATA4TXP
SATA5RXN
SATA5RXP
SATA5TXN
SATA5TXP
SATAICOMPO
SATAICOMPI
SATALED#
(+3V) SATA0GP / GPIO21
(+3V_S5) SATA1GP / GPIO19

E-SATA

IHDA
HDA_BCLK
HDA_SYNC
SPKR
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDO
HDA_DOCK_EN# / GPIO33 (+3V)
HDA_DOCK_RST# / GPIO13 (+3V_S5)

JTAG
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
TRST#

SPI
SPI_CLK
SPI_CS0#
SPI_CS1#
SPI_MOSI
SPI_MISO

IbexPeak-M_Rev1_0

IBEX PEAK-M (LVDS,DDI)

U29D

Ibex-M 4 OF 10

SDVO
SDVO_TVCLKINN
SDVO_TVCLKINP
SDVO_STALLN
SDVO_STALLP
SDVO_INTN
SDVO_INTP
SDVO_CTRLCLK
SDVO_CTRLDATA

Digital Display Interface

DISPLAY PORT B
DDPB_AUXN
DDPB_AUXP
DDPB_HPD
DDPB_0N
DDPB_0P
DDPB_1N
DDPB_1P
DDPB_2N
DDPB_2P
DDPB_3N
DDPB_3P

DISPLAY PORT C
DDPC_CTRLCLK
DDPC_CTRLDATA
DDPC_AUXN
DDPC_AUXP
DDPC_HPD
DDPC_0N
DDPC_0P
DDPC_1N
DDPC_1P
DDPC_2N
DDPC_2P
DDPC_3N
DDPC_3P

DISPLAY PORT D
DDPD_CTRLCLK
DDPD_CTRLDATA
DDPD_AUXN
DDPD_AUXP
DDPD_HPD
DDPD_0N
DDPD_0P
DDPD_1N
DDPD_1P
DDPD_2N
DDPD_2P
DDPD_3N
DDPD_3P

LVDS--A
LVDSA_CLK#
LVDSA_CLK
LVDSA_DATA#0
LVDSA_DATA#1
LVDSA_DATA#2
LVDSA_DATA#3
LVDSA_DATA0
LVDSA_DATA1
LVDSA_DATA2
LVDSA_DATA3

LVDS--B
LVDSB_CLK#
LVDSB_CLK
LVDSB_DATA#0
LVDSB_DATA#1
LVDSB_DATA#2
LVDSB_DATA#3
LVDSB_DATA0
LVDSB_DATA1
LVDSB_DATA2
LVDSB_DATA3

CRT
CRT_BLUE
CRT_GREEN
CRT_RED
CRT_DDC_CLK
CRT_DDC_DATA
CRT_HSYNC
CRT_VSYNC
DAC_IREF
CRT_IRTN

IbexPeak-M_Rev1_0

UMA LVDS & CRT signals

UMA HDMI signals

Q24
2N7002K

UMA ony

1205 The SATALED# signal is open-collector and requires a weak external pull-up (8.2 k to 10 k) to +V3.3.

For AUDIO

For MDC

RTC

20 mil

2M byte SPI ROM for ME

4M byte SPI ROM for ME
MXIC AKE39FP0Z00

2M byte SPI ROM for ME
MXIC: AKE38FP0Z00
WINBOND: AKE38FP0N01
AIT: AKE38ZN0800

SPI ROM Socket
DG008000031

2M SPI ROM
AKE39FP0Z00
X6179-10XXXX-8P-SOCKET

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 1/5 (SATA,HDA,LPC)	1A

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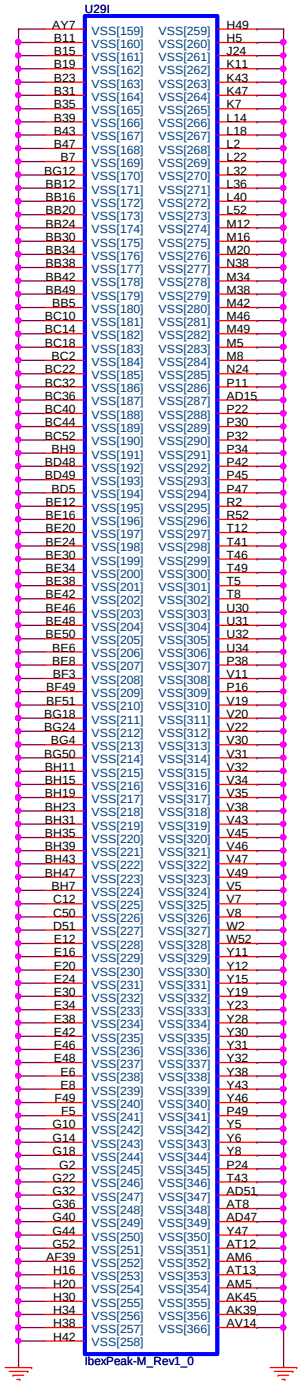
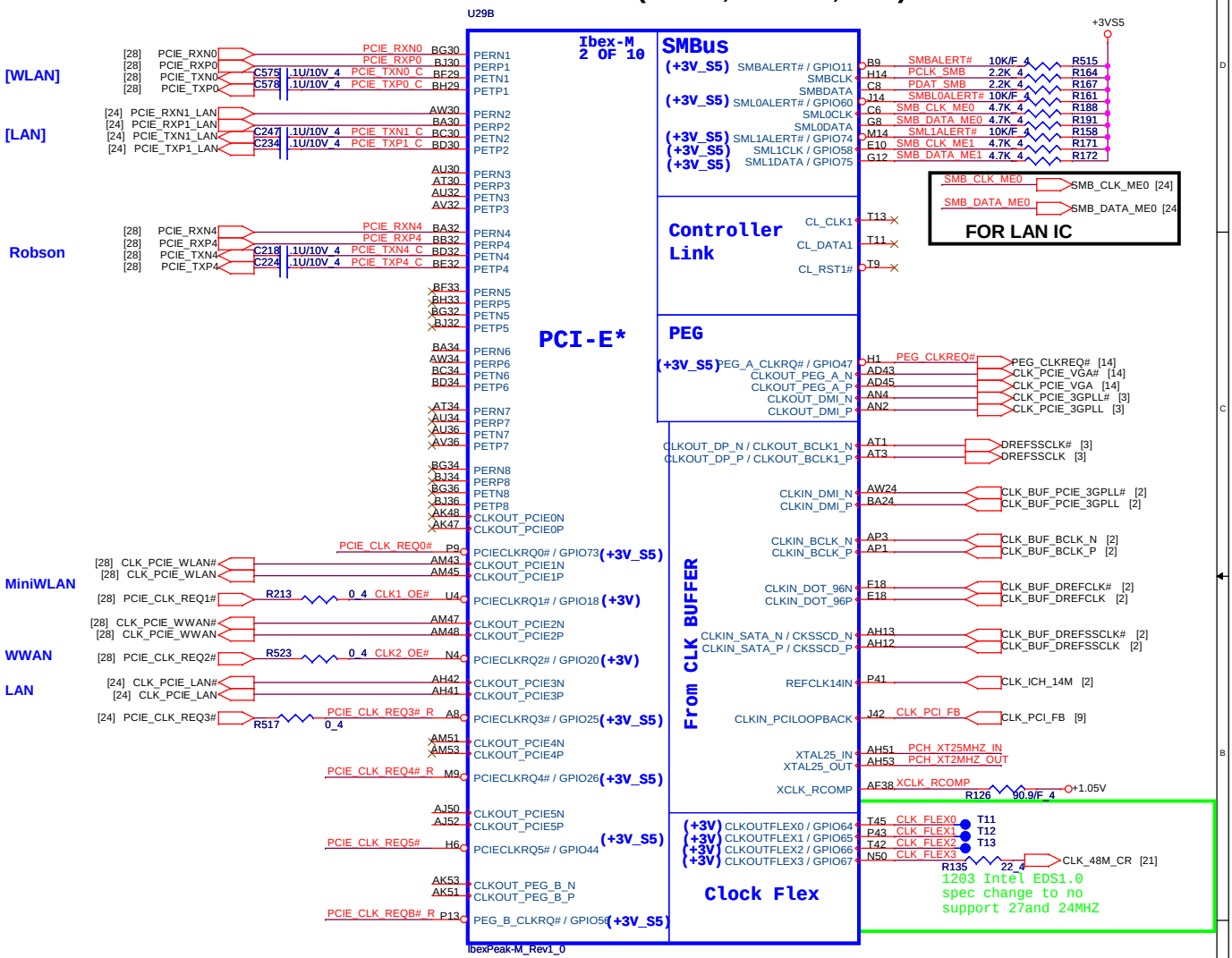
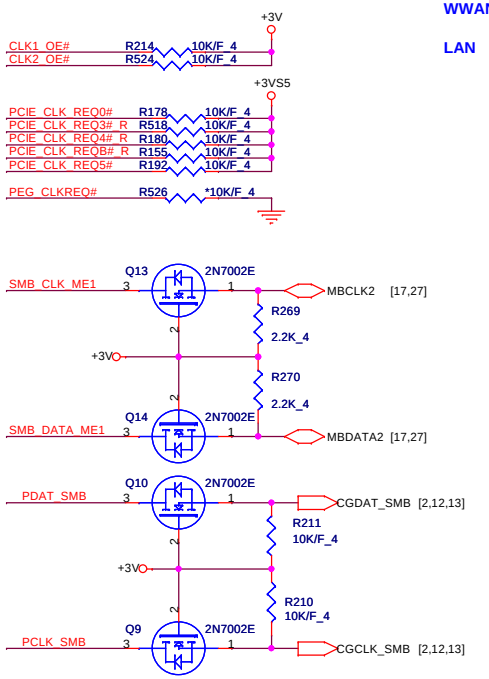
IBEX PEAK-M (GND)

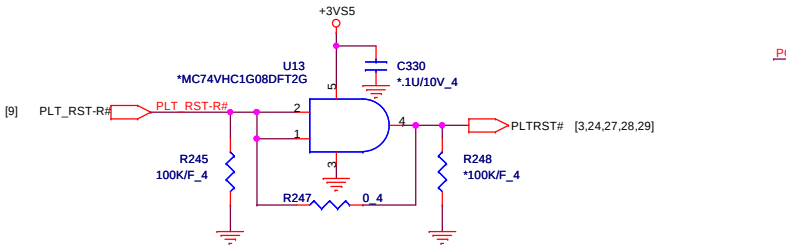


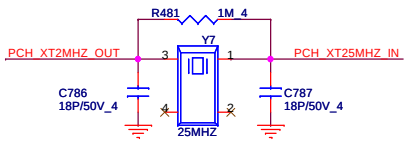
IBEX PEAK-M (PCI-E,SMBUS,CLK)

08





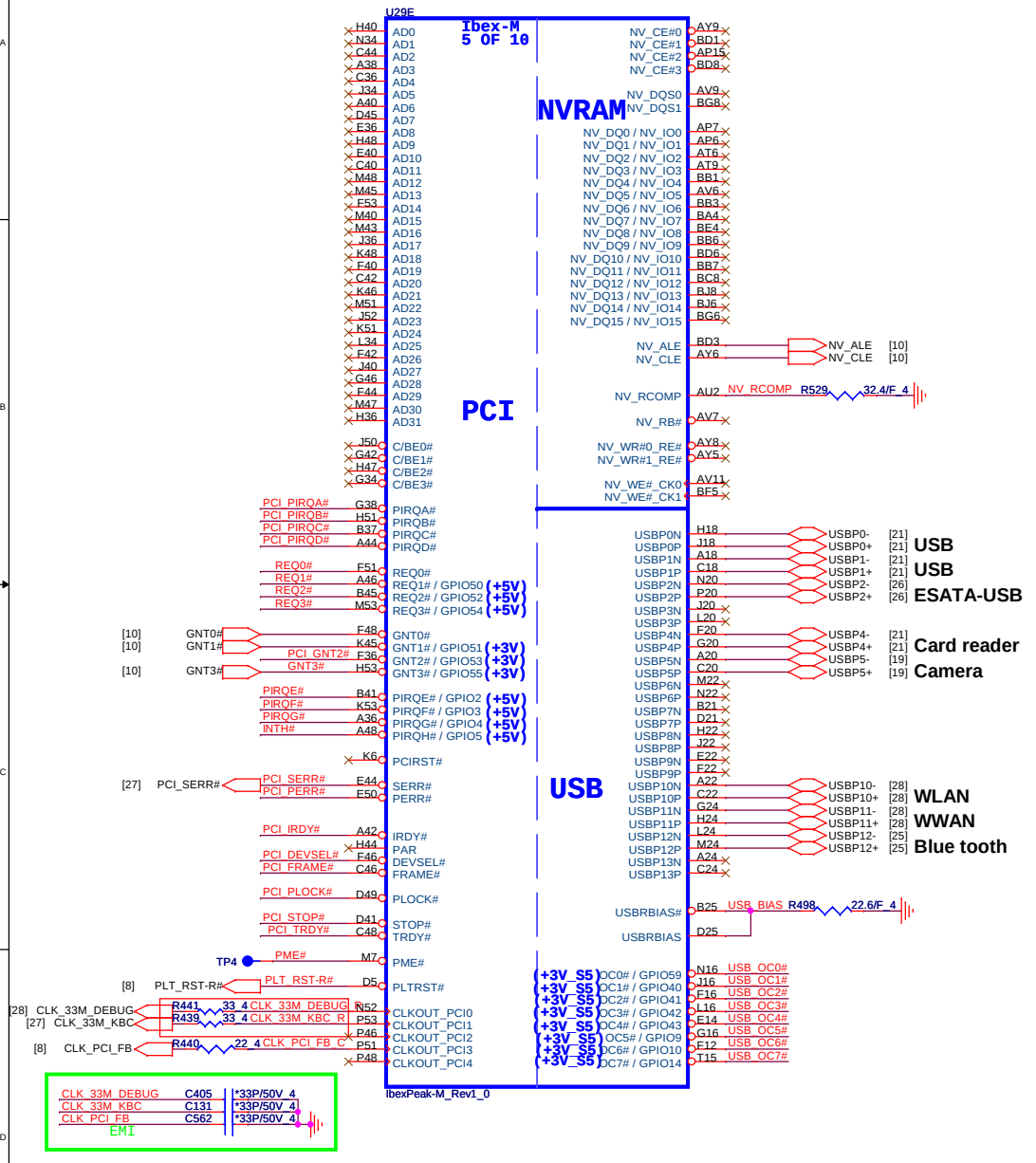




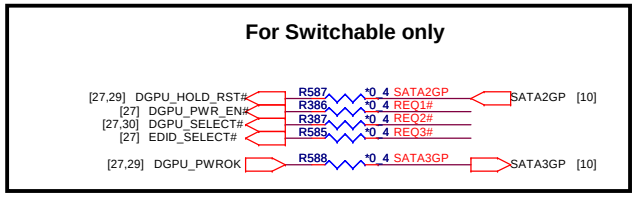
[3,9,10,11,14,37] +3VS5
[2,7,9,11,27,31,33,34,39] +1.05V
[2,3,7,9,10,11,12,13,19,20,21,22,23,24,25,26,27,28,29,30,34,37,39] +3V

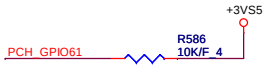
PROJECT : SW9 Quanta Computer Inc.		
Size: Custom	Document Number: PCH 2/5 (PCIE, SMBUS,CK)	Rev: 1A
Date: Wednesday, December 02, 2009	Sheet 8 of 44	

IBEX PEAK-M (PCI,USB,NVRAM)

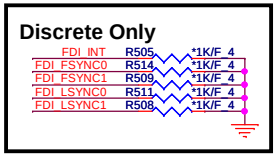


For Switchable only

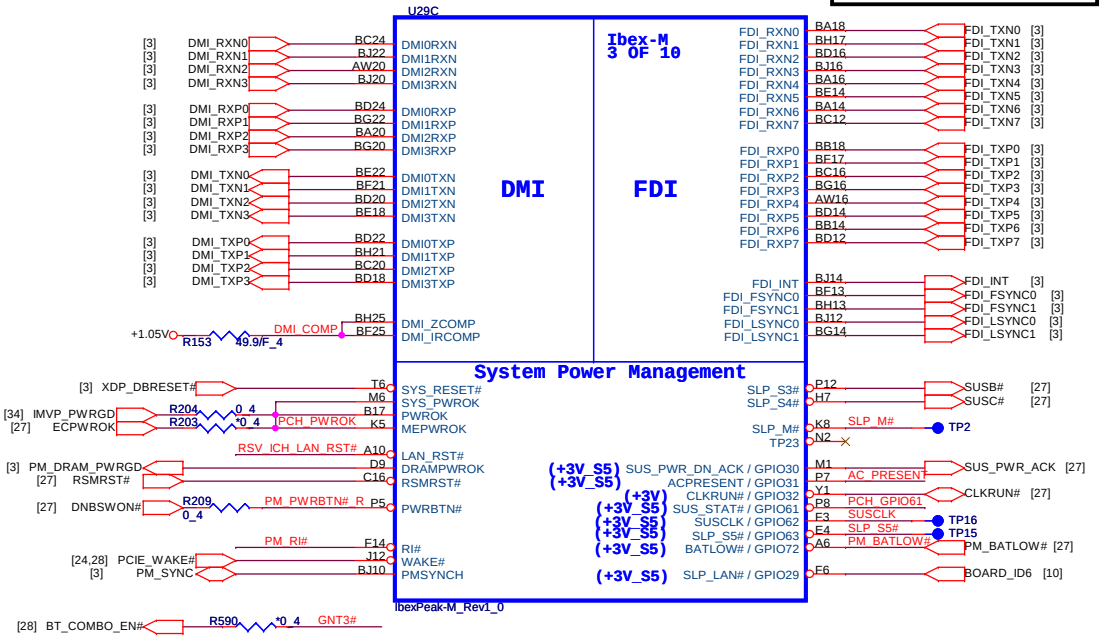


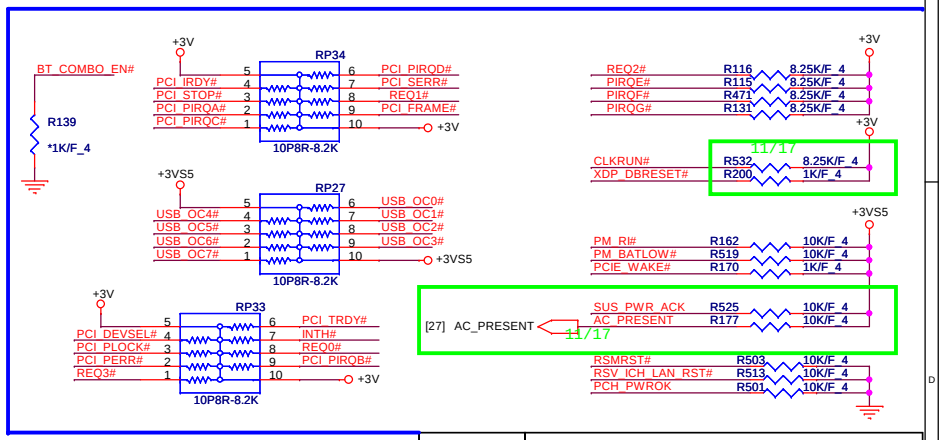


Discrete Only



IBEX PEAK-M (DMI,FDI,GPIO)





[2,7,8,11,27,31,33,34,39] +1.05V
[2,3,7,8,10,11,12,13,19,20,21,22,23,24,25,26,27,28,29,30,34,37,39] +3V
[3,8,10,11,14,37] +3VS5

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 3/5(PCI,ONFI,USB,DMI)	1A

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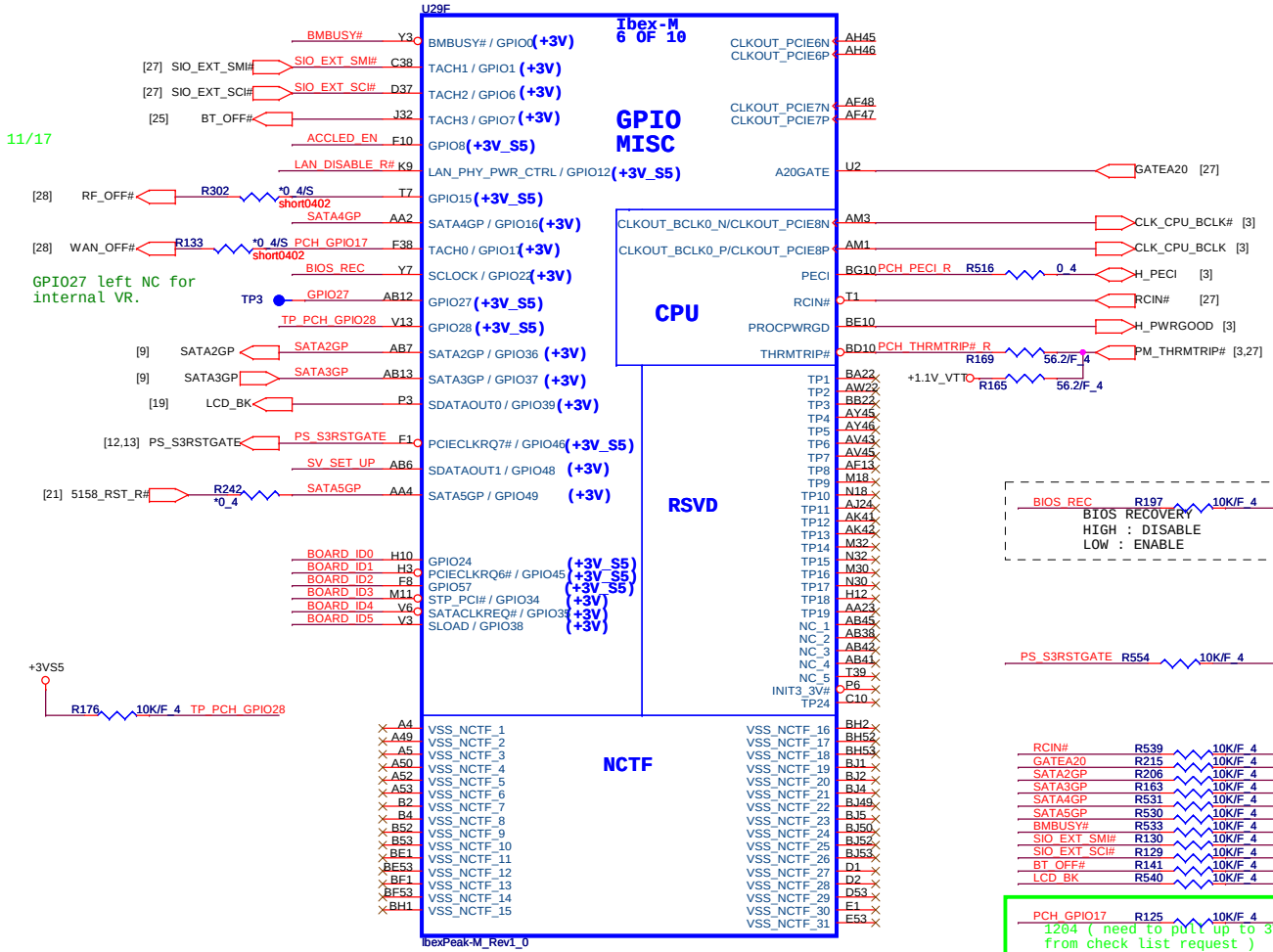
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



11/17

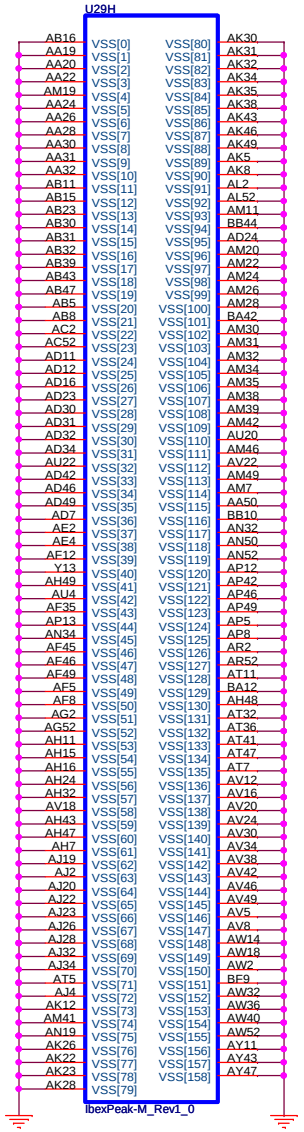
GPIO27 left NC for internal VR.

Board ID	ID0	ID1	ID2	ID3	ID4	ID5	ID6
LG/CB	0=LG 1=CB						
UMA/Dis.		0=UMA 1=Dis.					
15.6"/ 14"			0=QL4/TW9 1=QL2/SW9				
MDC				0=YES 1=NO			

BOARD ID SETTING

Board ID	ID6	ID5	ID4	ID3	ID2	ID1	ID0
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RD2 (0)	RU1 (1)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RD1 (0)	RU0 (1)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RD0 (0)
TBD	RD6 (0)	RD5 (0)	RD4 (0)	RD3 (0)	RU2 (1)	RU1 (1)	RU0 (1)

IBEX PEAK-M (GND)



10

A16 swap override Strap/Top-Block Swap Override jumper

GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

SV_SET_UP	1-X High = Strong (Default)

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

Danbury Technology Enabled

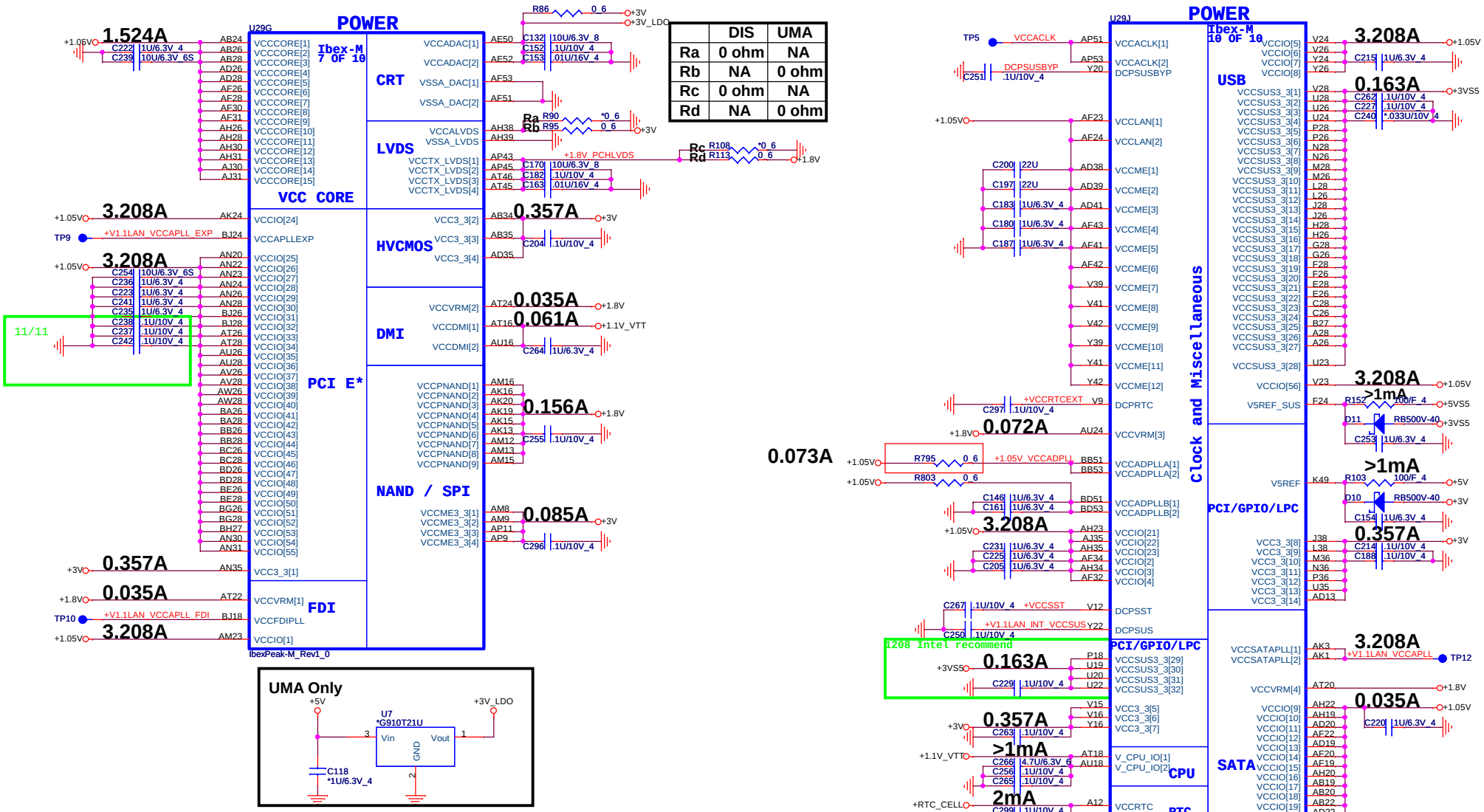
NV_ALE	High = Enable Low = Disable

DMI Termination Voltage

NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

No Reboot Strap

PROJECT : SW9		
Quanta Computer Inc.		
Size: Custom	Document Number: PCH 4/5 (GPIO & Strap)	Rev: 1A
Date: Wednesday, December 02, 2009	Sheet: 10of	44



	DIS	UMA
Ra	0 ohm	NA
Rb	NA	0 ohm
Rc	0 ohm	NA
Rd	NA	0 ohm

[2,7,8,9,27,31,33,34,39] +1.05V
[3,5,10,31,34,35] +1.1V_VTT
[5,10,33,37,39] +1.8V
[2,3,7,8,9,10,12,13,19,20,21,22,23,24,25,26,27,28,29,30,34,37,39] +3V
[3,8,9,10,14,37] +3VS5
[19,20,22,23,25,26,28,30,37] +5V
[37] +5VS5

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 5/5 (POWER)	1A

Date: Wednesday, December 02, 2009 Sheet 11of 44

SO-DIMMA SPD Address is 0XA0
SO-DIMMA TS Address is 0X30

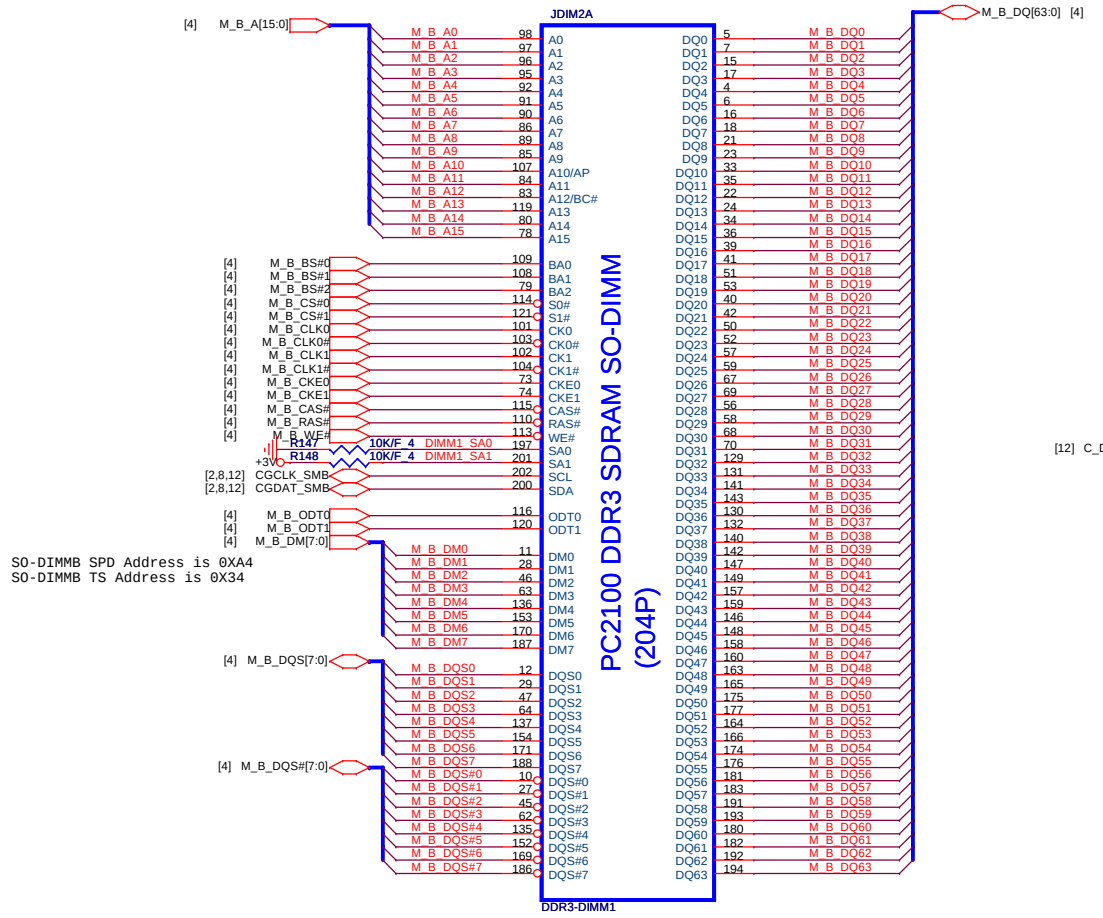
JDIM1A
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM0

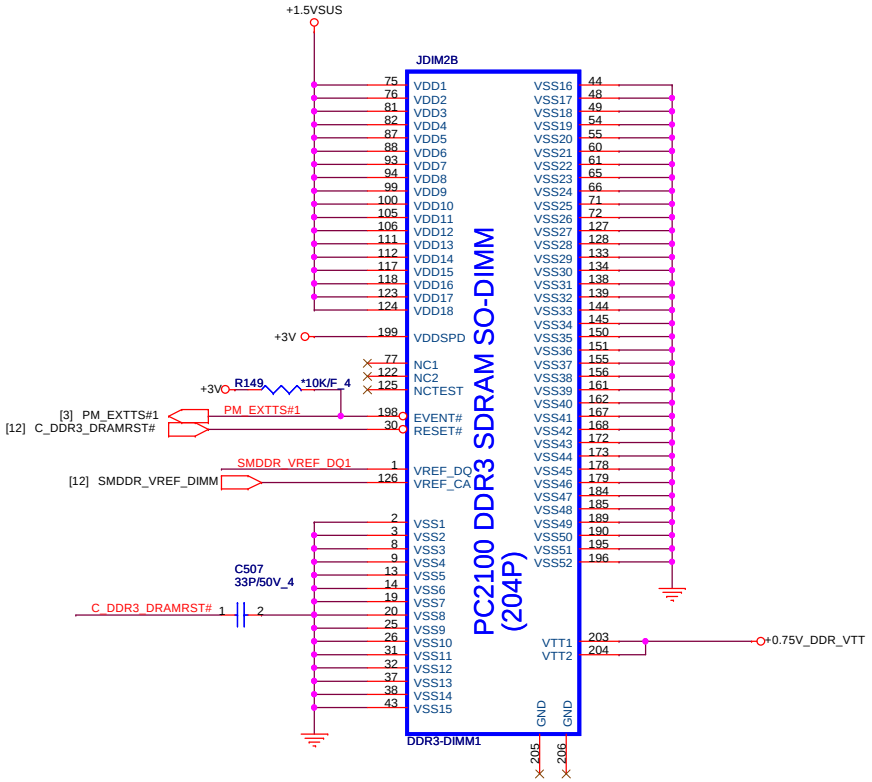
JDIM1B
PC2100 DDR3 SDRAM SO-DIMM (204P)
DDR3-DIMM0

EMI

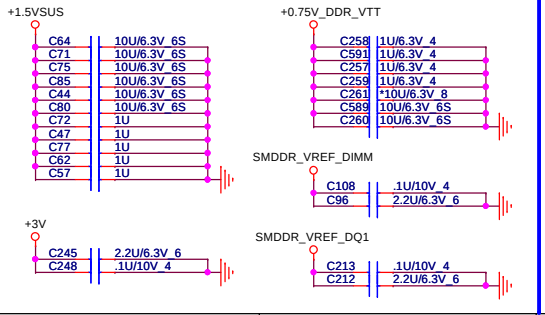
Place these Caps near So-Dimm0.

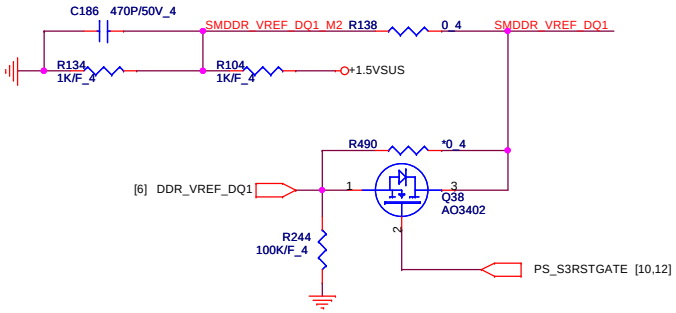
11/6





Place these Caps near So-Dimm1.



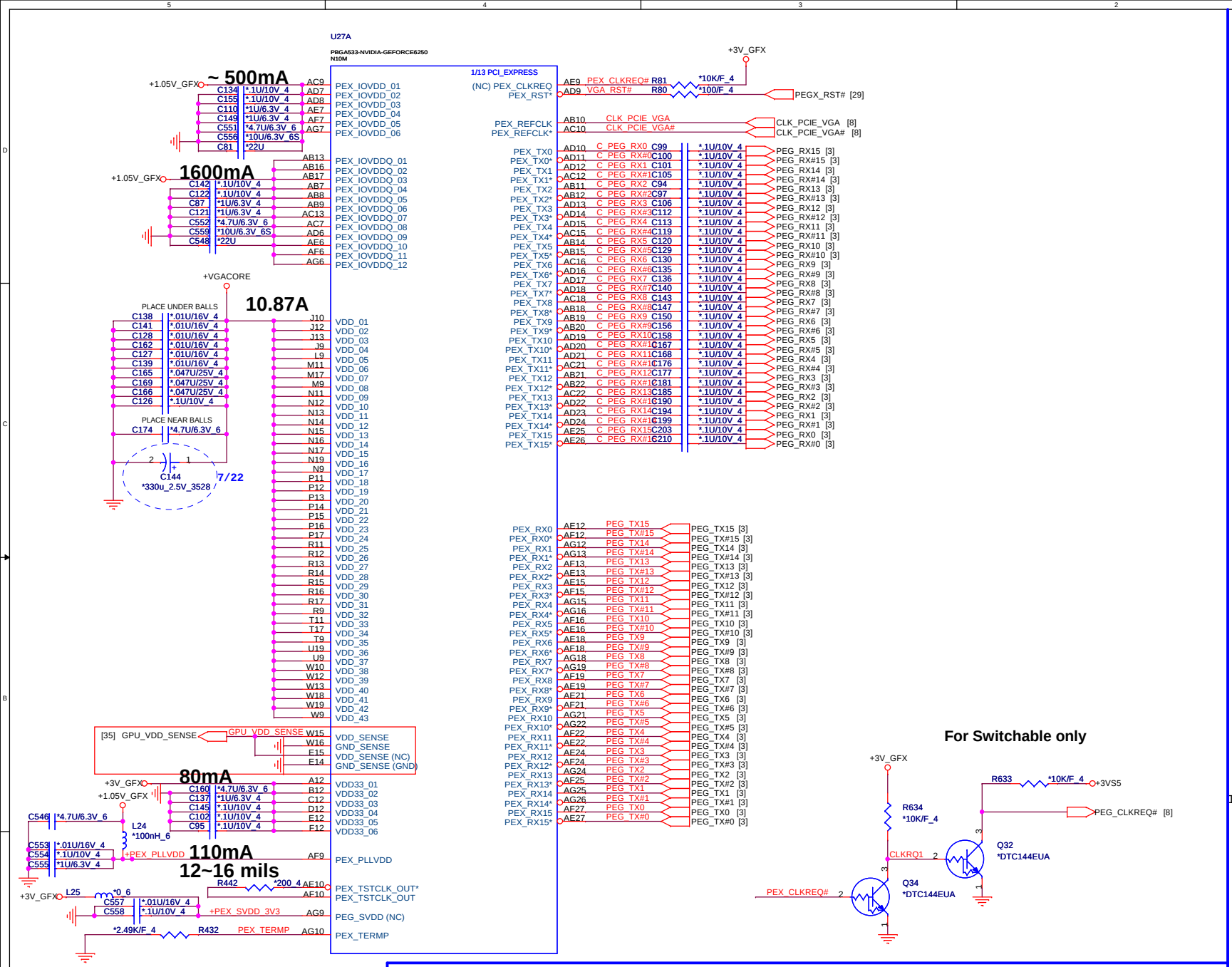


[12,36] +0.75V_DDR_VTT
[5,12,36,37,39] +1.5VSUS
[2,3,7,8,9,10,11,12,19,20,21,22,23,24,25,26,27,28,29,30,34,37,39] +3V
[7,19,21,23,26,27,28,31,32,33,35,37,38,39] +3VPCU
[27,31,32,33,34,35,36,37] +5VPCU

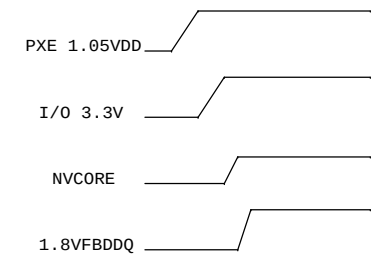
PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM-1	1A

Date: Wednesday, December 02, 2009 Sheet 13 of 44

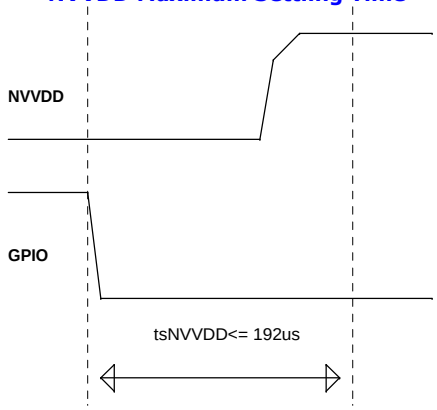


power up sequence

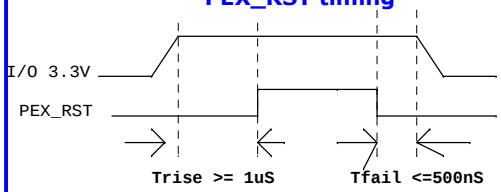


NB9M: VGACORE +0.90V (Normal) , +1.09V

NVVDD Maximum Settling Time



PEX_RST timing

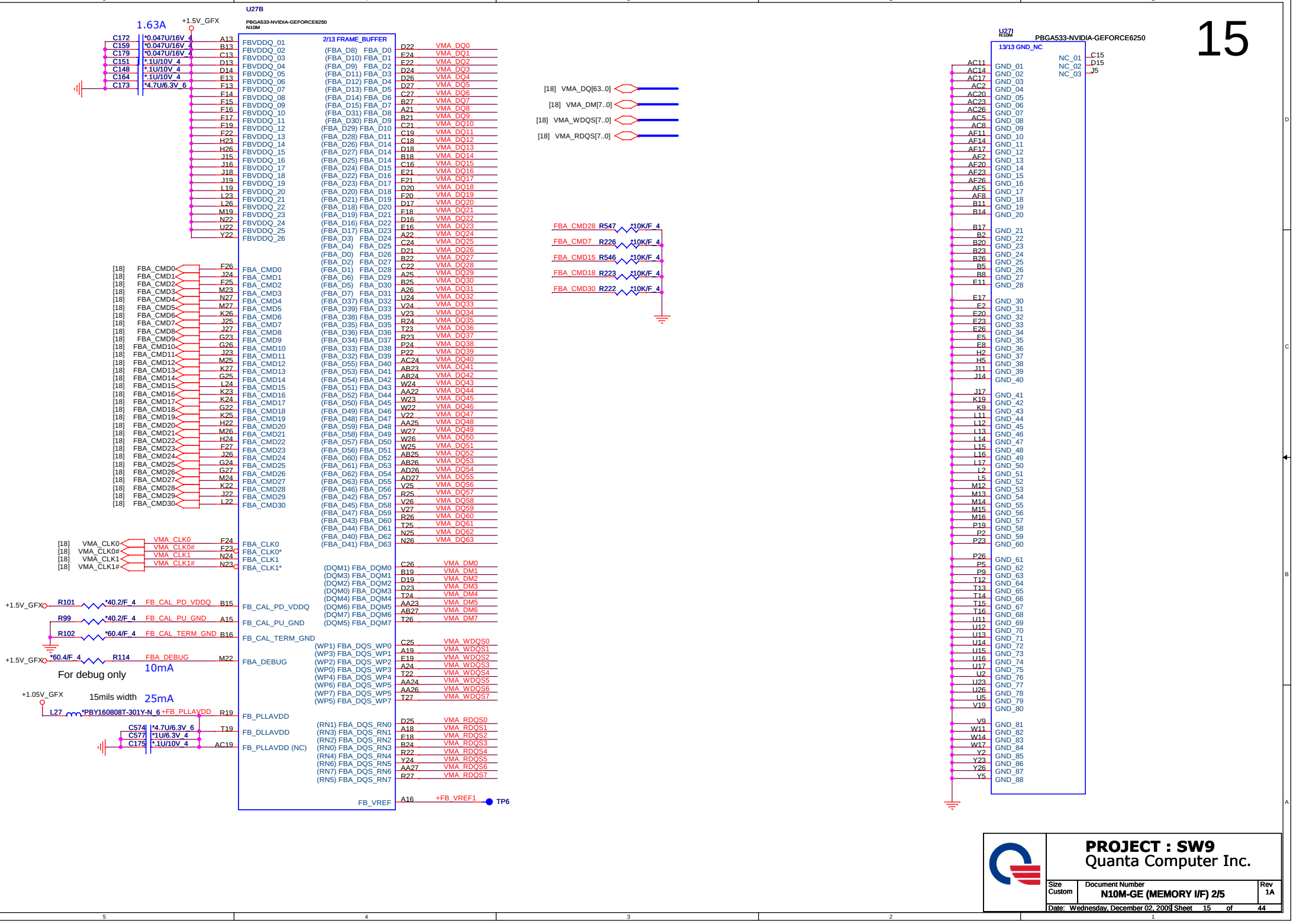


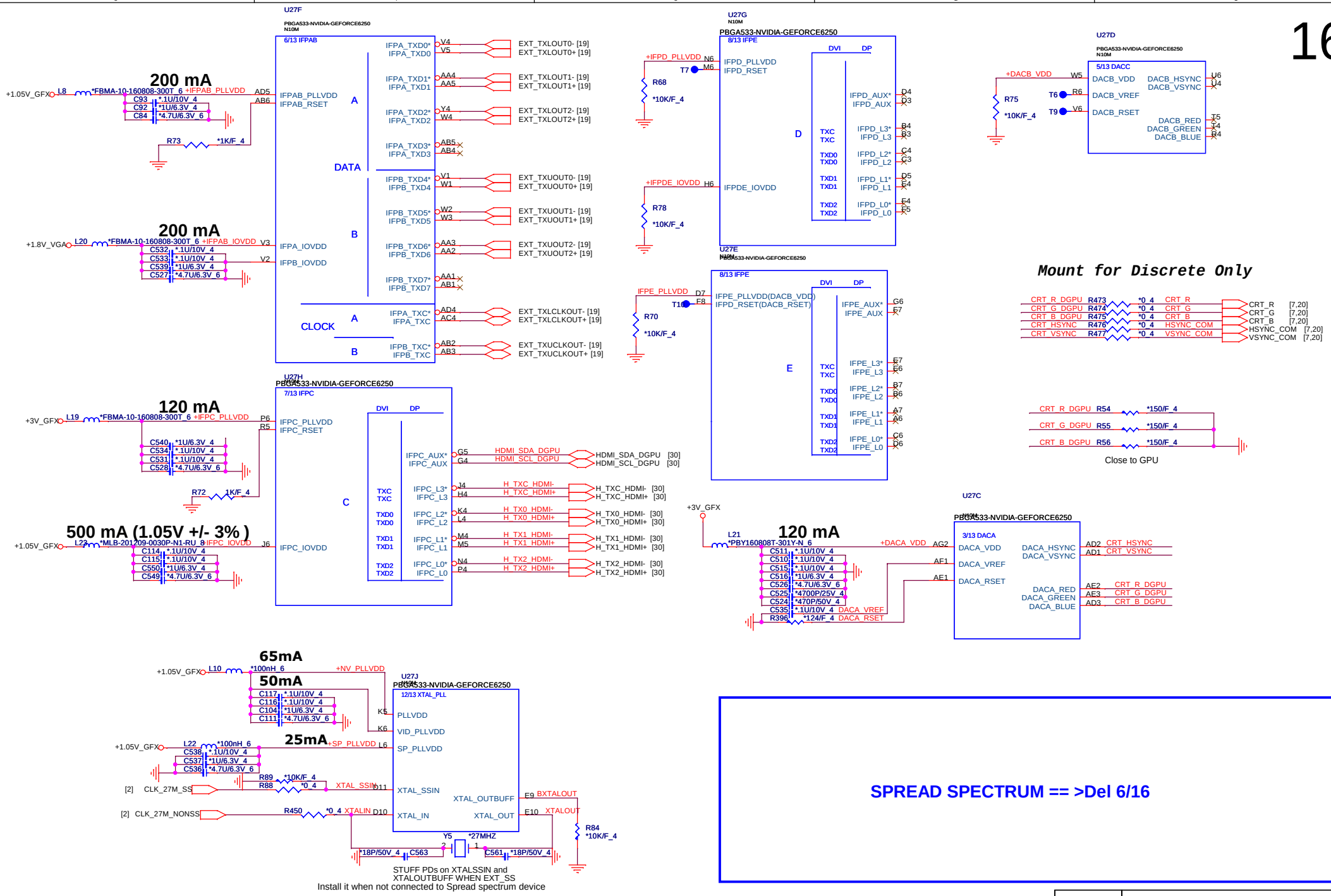
VGA Thermal Circuit ==> Del 6/16

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M-GE (PCIE I/F) 1/5	1A

Date: Wednesday, December 02, 2009 Sheet 14 of 44


U27B
PBGA533-NVIDIA-GEFORCE6250
N10M
2/13 FRAME_BUFFER
1.63A
+1.5V_GFX
FBVDDQ_01
FBVDDQ_02
FBVDDQ_03
FBVDDQ_04
FBVDDQ_05
FBVDDQ_06
FBVDDQ_07
FBVDDQ_08
FBVDDQ_09
FBVDDQ_10
FBVDDQ_11
FBVDDQ_12
FBVDDQ_13
FBVDDQ_14
FBVDDQ_15
FBVDDQ_16
FBVDDQ_17
FBVDDQ_18
FBVDDQ_19
FBVDDQ_20
FBVDDQ_21
FBVDDQ_22
FBVDDQ_23
FBVDDQ_24
FBVDDQ_25
FBVDDQ_26
C172 *0.047U/16V_4
C159 *0.047U/16V_4
C179 *0.047U/16V_4
C151 *.1U/10V_4
C148 *.1U/10V_4
C164 *.1U/10V_4
C173 *4.7U/6.3V_6
A13
B13
C13
D13
D14
E13
F13
F14
F15
F16
F17
F19
F22
H23
H26
J15
J16
J18
J19
L19
L23
L26
M19
N22
U22
Y22
[18] VMA_DQ[63..0]
[18] VMA_DM[7..0]
[18] VMA_WDQS[7..0]
[18] VMA_RDQS[7..0]
FBA_CMD28 R547 *10K/F_4
FBA_CMD7 R226 *10K/F_4
FBA_CMD15 R546 *10K/F_4
FBA_CMD18 R223 *10K/F_4
FBA_CMD30 R222 *10K/F_4
[18] FBA_CMD0
[18] FBA_CMD1
[18] FBA_CMD2
[18] FBA_CMD3
[18] FBA_CMD4
[18] FBA_CMD5
[18] FBA_CMD6
[18] FBA_CMD7
[18] FBA_CMD8
[18] FBA_CMD9
[18] FBA_CMD10
[18] FBA_CMD11
[18] FBA_CMD12
[18] FBA_CMD13
[18] FBA_CMD14
[18] FBA_CMD15
[18] FBA_CMD16
[18] FBA_CMD17
[18] FBA_CMD18
[18] FBA_CMD19
[18] FBA_CMD20
[18] FBA_CMD21
[18] FBA_CMD22
[18] FBA_CMD23
[18] FBA_CMD24
[18] FBA_CMD25
[18] FBA_CMD26
[18] FBA_CMD27
[18] FBA_CMD28
[18] FBA_CMD29
[18] FBA_CMD30
F26
J24
F25
M23
N27
M27
K26
J25
J27
G23
G26
J23
M25
K27
G25
L24
K23
K24
G22
K25
H22
M26
H24
F27
J26
G24
G27
M24
K22
J22
L22
FBA_CMD0
FBA_CMD1
FBA_CMD2
FBA_CMD3
FBA_CMD4
FBA_CMD5
FBA_CMD6
FBA_CMD7
FBA_CMD8
FBA_CMD9
FBA_CMD10
FBA_CMD11
FBA_CMD12
FBA_CMD13
FBA_CMD14
FBA_CMD15
FBA_CMD16
FBA_CMD17
FBA_CMD18
FBA_CMD19
FBA_CMD20
FBA_CMD21
FBA_CMD22
FBA_CMD23
FBA_CMD24
FBA_CMD25
FBA_CMD26
FBA_CMD27
FBA_CMD28
FBA_CMD29
FBA_CMD30
[18] VMA_CLK0
[18] VMA_CLK0#
[18] VMA_CLK1
[18] VMA_CLK1#
VMA_CLK0 F24
VMA_CLK0# F23
VMA_CLK1 N24
VMA_CLK1# N23
FBA_CLK0
FBA_CLK0*
FBA_CLK1
FBA_CLK1*
+1.5V_GFX
R101 *40.2/F_4 FB_CAL_PD_VDDQ B15
R99 *40.2/F_4 FB_CAL_PU_GND A15
R102 *60.4/F_4 FB_CAL_TERM_GND B16
+1.5V_GFX
*60.4/F_4 R114 FBA_DEBUG M22
For debug only
10mA
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CAL_TERM_GND
FBA_DEBUG
+1.05V_GFX
15mils width
25mA
L27 *PBY160808T-301Y-N_6 +FB_PLLAVDD R19
C574 *4.7U/6.3V_6
C577 *1U/6.3V_4
C175 *.1U/10V_4
T19
AC19
FB_PLLAVDD
FB_DLLAVDD
FB_PLLAVDD (NC)
(DQM1) FBA_DQM0
(DQM3) FBA_DQM1
(DQM2) FBA_DQM2
(DQM0) FBA_DQM3
(DQM4) FBA_DQM4
(DQM6) FBA_DQM5
(DQM7) FBA_DQM6
(DQM5) FBA_DQM7
C26 VMA_DM0
B19 VMA_DM1
D19 VMA_DM2
D23 VMA_DM3
T24 VMA_DM4
AA23 VMA_DM5
AB27 VMA_DM6
T26 VMA_DM7
(WP1) FBA_DQS_WP0
(WP3) FBA_DQS_WP1
(WP2) FBA_DQS_WP2
(WP0) FBA_DQS_WP3
(WP4) FBA_DQS_WP4
(WP6) FBA_DQS_WP5
(WP7) FBA_DQS_WP5
(WP5) FBA_DQS_WP7
C25 VMA_WDQS0
A19 VMA_WDQS1
E19 VMA_WDQS2
A24 VMA_WDQS3
T22 VMA_WDQS4
AA24 VMA_WDQS5
AA26 VMA_WDQS6
T27 VMA_WDQS7
(RN1) FBA_DQS_RN0
(RN3) FBA_DQS_RN1
(RN2) FBA_DQS_RN2
(RN0) FBA_DQS_RN3
(RN4) FBA_DQS_RN4
(RN6) FBA_DQS_RN5
(RN7) FBA_DQS_RN6
(RN5) FBA_DQS_RN7
D25 VMA_RDQS0
A18 VMA_RDQS1
E18 VMA_RDQS2
B24 VMA_RDQS3
R22 VMA_RDQS4
Y24 VMA_RDQS5
AA27 VMA_RDQS6
R27 VMA_RDQS7
FB_VREF
A16 +FB_VREF1 TP6
U27I
N10M
PBGA533-NVIDIA-GEFORCE6250
13/13 GND_NC
NC_01 C15
NC_02 D15
NC_03 J5
AC11 GND_01
AC14 GND_02
AC17 GND_03
AC2 GND_04
AC20 GND_05
AC23 GND_06
AC26 GND_07
AC5 GND_08
AC8 GND_09
AE11 GND_10
AE14 GND_11
AE17 GND_12
AE2 GND_13
AE20 GND_14
AE23 GND_15
AE26 GND_16
AE5 GND_17
AE8 GND_18
B11 GND_19
B14 GND_20
B17 GND_21
B2 GND_22
B20 GND_23
B23 GND_24
B26 GND_25
B5 GND_26
B8 GND_27
E11 GND_28
E17 GND_30
E2 GND_31
E20 GND_32
E23 GND_33
E26 GND_34
E5 GND_35
E8 GND_36
H2 GND_37
H5 GND_38
J11 GND_39
J14 GND_40
J17 GND_41
K19 GND_42
K9 GND_43
L11 GND_44
L12 GND_45
L13 GND_46
L14 GND_47
L15 GND_48
L16 GND_49
L17 GND_50
L2 GND_51
L5 GND_52
M12 GND_53
M13 GND_54
M14 GND_55
M15 GND_56
M16 GND_57
P19 GND_58
P2 GND_59
P23 GND_60
P26 GND_61
P5 GND_62
P9 GND_63
T12 GND_64
T13 GND_65
T14 GND_66
T15 GND_67
T16 GND_68
U11 GND_69
U12 GND_70
U13 GND_71
U14 GND_72
U15 GND_73
U16 GND_74
U17 GND_75
U2 GND_76
U23 GND_77
U26 GND_78
U5 GND_79
V19 GND_80
V9 GND_81
W11 GND_82
W14 GND_83
W17 GND_84
Y2 GND_85
Y23 GND_86
Y26 GND_87
Y5 GND_88
PROJECT : SW9
Quanta Computer Inc.
Size Custom
Document Number
N10M-GE (MEMORY I/F) 2/5
Rev 1A
Date: Wednesday, December 02, 2009 Sheet 15 of 44



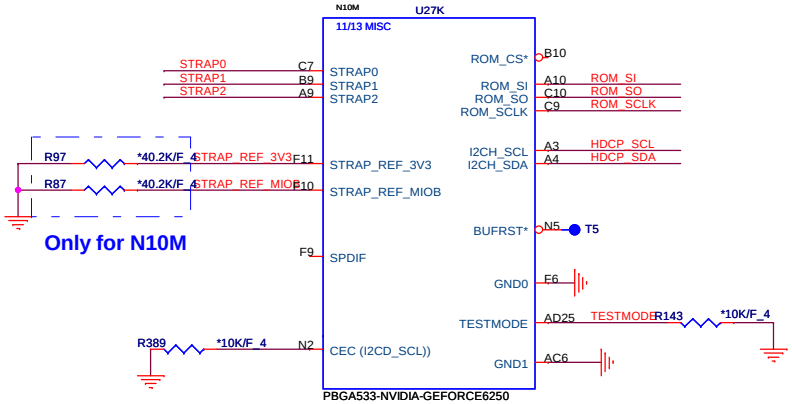
PROJECT : SW9 Quanta Computer Inc.		
Size: Custom	Document Number: N10M-GE (DISPLAY) 3/5	Rev: 1A
Date: Wednesday, December 02, 2009	Sheet 16 of 44	

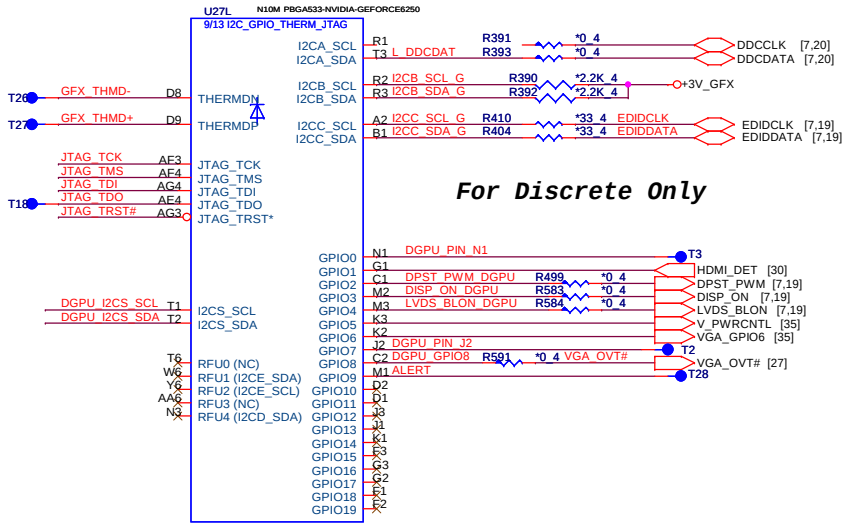
CHIP	PCI_DEVID:	STRAP2
N11P-GE1	0x0A29	1001 PU 10K
N11M-GE1	0x0A75	1010 PD 30K

SEE Datasheet for details on N10P Straps!

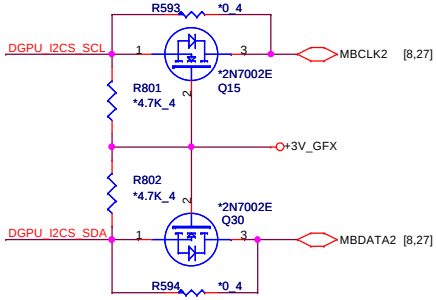
Logical Strap Bit Mapping

	PU-VDD	PD
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



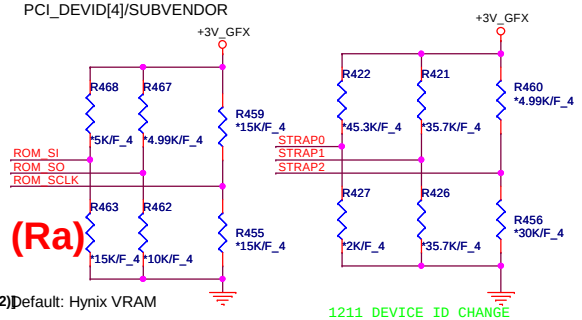


For Discrete Only



Mount Q15 , Q30 , R801 , R802
For Switchable only

PCI_DEVID[4]/SUBVENDOR



(Ra)

1211 DEVICE ID CHANGE

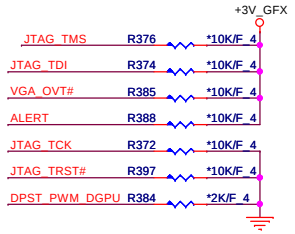
4.99K/F_4: CS24992FB26 [RES CHIP 4.99K 1/16W +1%(0402)] Default: Hynix VRAM
10K/F_4: CS31002FB26 [RES CHIP 10K 1/16W +1% (0402)]
15K/F_4: CS31502FB24 [RES CHIP 15K 1/16W +1% (0402)]
30.1K/F_4: CS33012FB18 [RES CHIP 30.1K 1/16W +-1%(0402)]
35.7K/F_4: CS33572FB13 [RES CHIP 35.7K 1/16W +-1%(0402)]
45.3K/F_4: CS34532FB18 [RES CHIP 45.3K 1/16W +-1% (0402)]

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SO NB10X	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE	0001
ROM_SCLK	PCI_DEVIDE[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM	0010
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]	1000
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]	0001
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]	1111

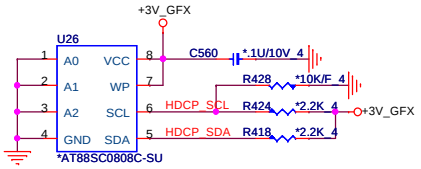
VRAM Configuration Table

	RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	ROM_SI
	0000		Reserved		
AKD58GGT^01	0001	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Qimonda	IDGH1G-04A1F1C-16X	PD 10K
AKD5LZGTW00	0010	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Hynix	H5TQ1G63BFR-12C	PD 15K
AKD5LGGT502	0011	DDR3 64Mx16x8, 128bit, 1GB,800MHz	Samsung	K4W1G1646E-EC12	PD 20K
	0101		Reserved		
	0110				
	XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Hynix	H5TQ1G63AFR-14C	
	XXXX	DDR3 64Mx16x8, 128bit, 1GB,667MHz	Samsung	K4W1G1646D-EC12	

(Ra)



HDCP ROM



DHCP ROM	
HDCP_SCL	Low: Crypto ROM Hi: I2C ROM

GPIO ASSIGNMENTS

GPIO	I/O	ACTIVE	USAGE
0	N/A	N/A	
1	IN	N/A	Hot plug detect for IFP link C
2	OUT	HIGH	PANEL BACKLIGHT PWM
3	OUT	HIGH	PANEL POWER ENABLE
4	OUT	HIGH	PANEL BACKLIGHT ENABLE
5	OUT	N/A	NVVDD VID0
6	OUT	N/A	NVVDD VID1
7	OUT	N/A	NVVDD VID2 11/13
8	I/O	LOW	OVERT
9	I/O	LOW	ALERT
10	OUT	N/A	FBVREF SELECT
11	OUT	N/A	SLI SYNC0
12	IN	N/A	PWR_LEVEL 11/13
13	OUT	N/A	MEM_VID or power supply control
14	OUT	N/A	PS CONTROL

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M-GE (GPIO&STRAPS) 4/5	1A

Date: Wednesday, December 02, 2009 Sheet 17 of 44

CHANNEL A: 256MB/512MB DDR3

[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]

U11 / U30 / U12 / U31 — 96-BALL SDRAM DDR3 *VRAM _DDR3

3/27 Swap

+1.5V_GFX

11/12

3/27 Swap

11/17 Swap

Should be 240 Ohms +-1%

R166 *243/F_4
R543 *243/F_4
R231 *243/F_4
R507 *243/F_4

2/19

VMA_CLK0 — R216 *243/F_4 — VMA_CLK0#

11/11 +1.5V_GFX

R545 *1.33K/F_4 — VREFC_VMA1 — R544 *1.33K/F_4 — C602 *.1U/10V_4

R220 *1.33K/F_4 — VREFD_VMA1 — R221 *1.33K/F_4 — C309 *.1U/10V_4

2/19

VMA_CLK1 — R217 *243/F_4 — VMA_CLK1#

11/11 +1.5V_GFX

R224 *1.33K/F_4 — VREFC_VMA3 — R225 *1.33K/F_4 — C317 *.1U/10V_4

R549 *1.33K/F_4 — VREFD_VMA3 — R548 *1.33K/F_4 — C607 *.1U/10V_4

[15,29,39] +1.5V_GFX

+1.5V_GFX
C604 C585 C584 C601 *1U/6.3V_4

+1.5V_GFX
C318 C298 C610 C315 C316 C314 *10U/6.3V_6S *.1U/10V_4

+1.5V_GFX
C603 C313 C609 C596 C598 C611 C608 C595 *.1U/10V_4

+1.5V_GFX
C599 C605 C597 C606 C612 C600 C308 C613 *.1U/10V_4

+1.5V_GFX
C311 C295 C310 C312 *.1U/10V_4

1211 for Nvidia request add transition cap

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N10M-GE VRAM-1(DDR3 BGA96	1A

Date: Wednesday, December 02, 2009 Sheet 18 of 44

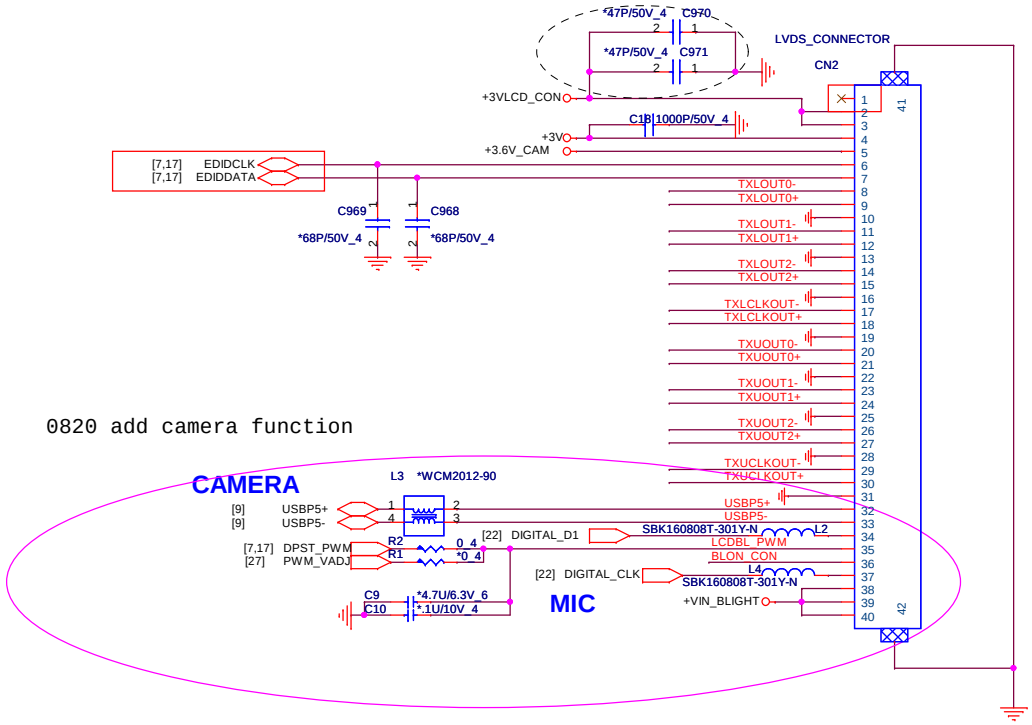
1. If LCD connector near GPU, then place these series Resistors near GPU
2. If LCD connector near N/B, then place these series Resistors near N/B

OPTION SIGNAL FROM NB FOR UMA VGA

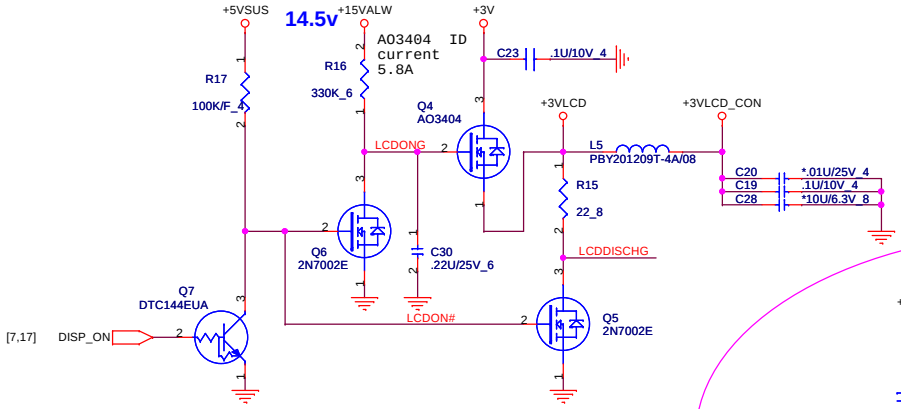
[7]	LA_CLK	RP8	4P2R-S-0	TXLCLKOUT+	
[7]	LA_CLK#			TXLCLKOUT-	
[7]	LA_DATAP0	RP6	4P2R-S-0	TXLOUT0+	
[7]	LA_DATAN0			TXLOUT0-	
[7]	LA_DATAP1	RP5	4P2R-S-0	TXLOUT1+	
[7]	LA_DATAN1			TXLOUT1-	
[7]	LA_DATAP2	RP7	4P2R-S-0	TXLOUT2+	
[7]	LA_DATAN2			TXLOUT2-	
[7]	LB_CLK#	RP1	4P2R-S-0	TXUCLKOUT-	
[7]	LB_CLK			TXUCLKOUT+	
[7]	LB_DATAP0	RP4	4P2R-S-0	TXUOUT0+	
[7]	LB_DATAN0			TXUOUT0-	
[7]	LB_DATAP1	RP2	4P2R-S-0	TXUOUT1+	
[7]	LB_DATAN1			TXUOUT1-	
[7]	LB_DATAP2	RP3	4P2R-S-0	TXUOUT2+	
[7]	LB_DATAN2			TXUOUT2-	

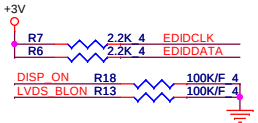
OPTION SIGNAL FROM Nvidia to VGA

[16] EXT_TXLCLKOUT-	*4P2R-S-0	RP16	TXLCLKOUT-	
[16] EXT_TXLCLKOUT+			TXLCLKOUT+	
[16] EXT_TXLOUT0+	*4P2R-S-0	RP14	TXLOUT0+	
[16] EXT_TXLOUT0-			TXLOUT0-	
[16] EXT_TXLOUT1-	*4P2R-S-0	RP13	TXLOUT1-	
[16] EXT_TXLOUT1+			TXLOUT1+	
[16] EXT_TXLOUT2-	*4P2R-S-0	RP15	TXLOUT2-	
[16] EXT_TXLOUT2+			TXLOUT2+	
[16] EXT_TXUCLKOUT-	*4P2R-S-0	RP9	TXUCLKOUT-	
[16] EXT_TXUCLKOUT+			TXUCLKOUT+	
[16] EXT_TXUOUT0-	*4P2R-S-0	RP12	TXUOUT0-	
[16] EXT_TXUOUT0+			TXUOUT0+	
[16] EXT_TXUOUT1-	*4P2R-S-0	RP10	TXUOUT1+	
[16] EXT_TXUOUT1+			TXUOUT1-	
[16] EXT_TXUOUT2-	*4P2R-S-0	RP11	TXUOUT2-	
[16] EXT_TXUOUT2+			TXUOUT2+	

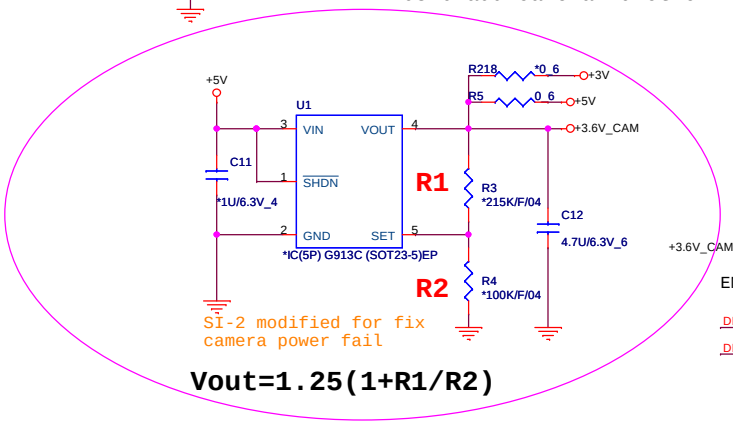


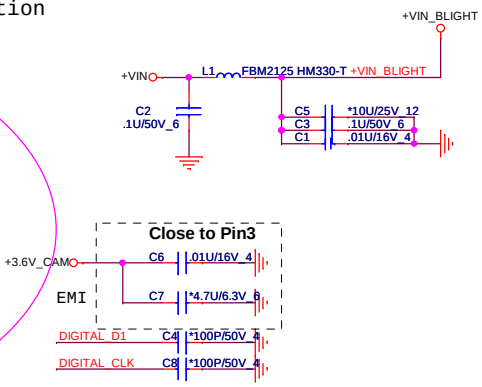
0820 add camera function

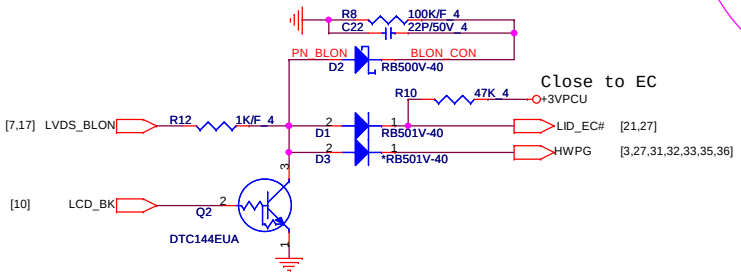




0820 add camera function







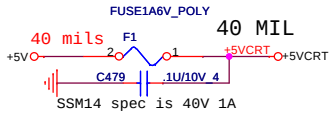
[11,20,22,23,25,26,28,30,37] +5V
[2,3,7,8,9,10,11,12,13,20,21,22,23,24,25,26,27,28,29,30,34,37,39] +3V
[7,21,23,26,27,28,31,32,33,35,37,38,39] +3VPCU
[21,25,26,37] +5VSUS
[32,37] +15VALW
[2,31,32,33,34,35,36,37,38,39] +VIN

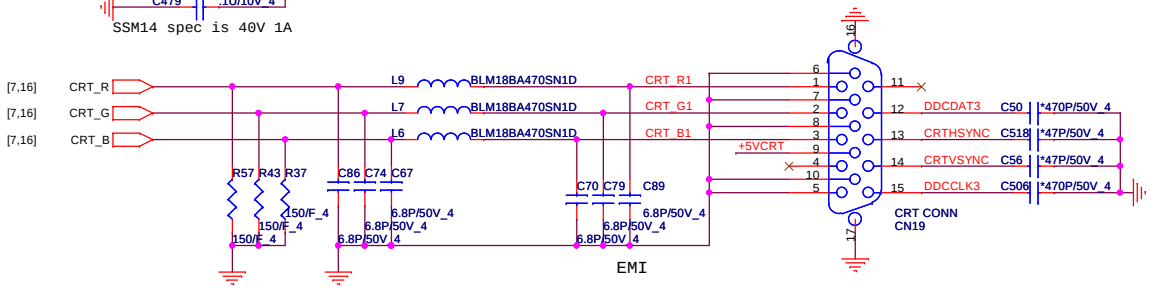
PROJECT : SW9
Quanta Computer Inc.

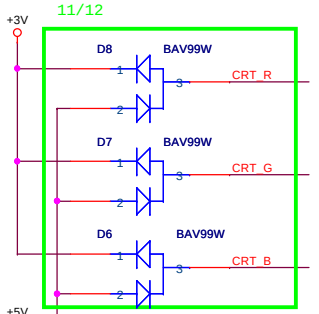
Size	Document Number	Rev
Custom	LCD CONN	1A

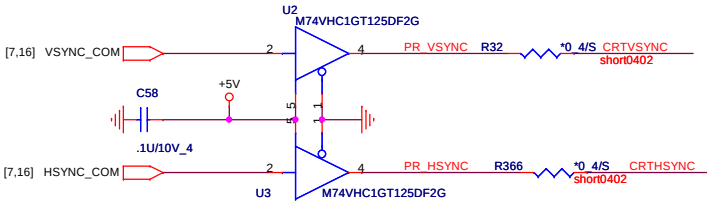
Date: Thursday, December 03, 2009 Sheet 19 of 44

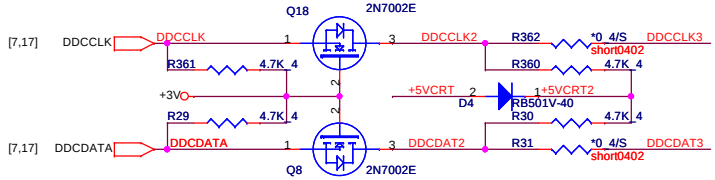
CRT PORT

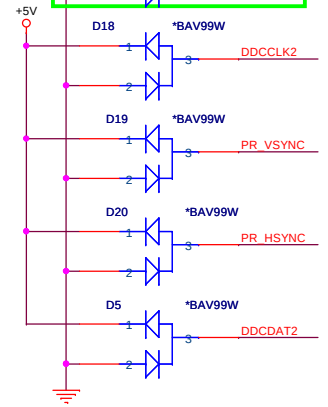












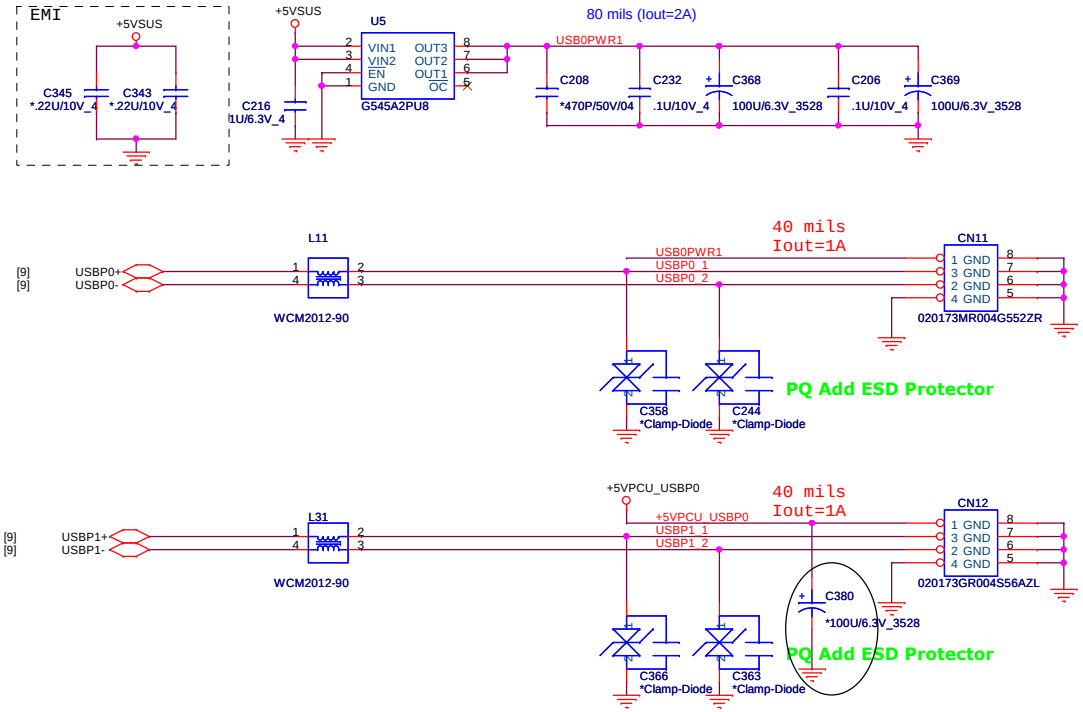
[2,3,7,8,9,10,11,12,13,19,21,22,23,24,25,26,27,28,29,30,34,37,39] +3V
[11,19,22,23,25,26,28,30,37] +5V

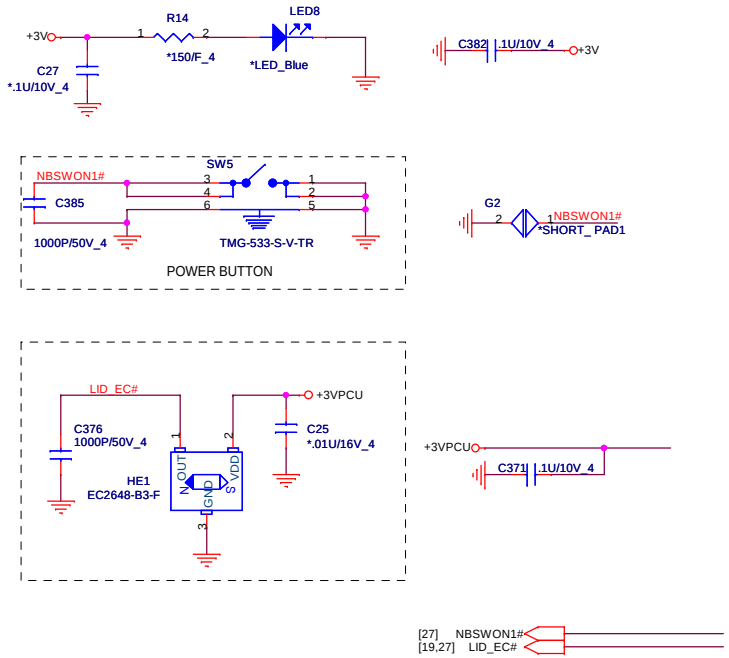
PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT/HDMI Conn	1A

Date: Wednesday, December 02, 2009 Sheet 20 of 44

USB CONNECTOR

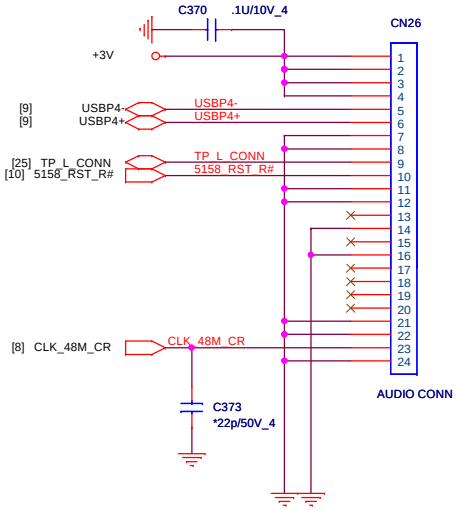




1. NBSWON1#
2. GND
3. GND
4. LID_EC#
5. +3V
6. +3VPCU

TO M/B CON.

PV Change CN2 footprint 88501-2001-24p-l-nb5



[7,19,23,26,27,28,31,32,33,35,37,38,39] +3VPCU
[2,3,7,8,9,10,11,12,13,19,20,22,23,24,25,26,27,28,29,30,34,37,39] +3V

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5159 &CR SOCKET	1A

Date: Wednesday, December 02, 2009 Sheet 21 of 44

Close to Pin1

C411 1U/6.3V_4
C410 1U/10V_4
C400 10U/6.3V_8

+4.75VAVDD
L29 *0_8
+5V
AGND
C418 10U/6.3V_8
C683 .1U/10V_4
C673 4.7U/6.3V_6
C684 .1U/6.3V_4
U35
Vout Vin
BYP
GND EN
TPS793475
C669 10U/6.3V_8
C672 .1U/10V_4
C670 1U/6.3V_4
C671 .047U/25V_4
R563 10K_4
Vset=1.242V

Close to Pin9
C409 .1U/10V_4
Close to Pin38
C431 10U/6.3V_8
C688 .1U/10V_4
C676 .1U/10V_4
Close to Pin1
C698 1U/10V_4
C417 10U/6.3V_8

U37
ALC272
DVDD DVDD-I/O AVDD2 AVDD1
SDATA-OUT BIT-CLK SDATA-IN SYNC RESET#
GPIO0-DMIC-12 DMIC-CLK
EAPD
MONO SURR-L SURR-R NC DMIC-CLK3/4 SPDIFO2 SPDIFO1 GPIO3/DMIC-34
PCBEEP
FRONT-R FRONT-L HPOUT-R HPOUT-L
LINE1-R LINE1-L LINE2-VREFO MIC2-VREFO LINE1-VREFO MIC2-R MIC2-L LINE2-R LINE2-L MIC1-R MIC1-L Sense A Sense B CBN CBP
DVSS DVSS-I/O
CPVEE JDREF AVSS2 AVSS1 VREF MIC1-VREFO-L

[7] ACZ_SDOUT_AUDIO
[7] BIT_CLK_AUDIO
[7] ACZ_SDIN0
[7] ACZ_SYNC_AUDIO
[7] ACZ_RST#_AUDIO
R271 *22_4
ACZ_SDIN0_ADC
R565 33_4
[19] DIGITAL_D1
[19] DIGITAL_CLK
L30 BK1005HS601-T_4
[23] EAPD#

HP-R C407 .47U/10V_6 HP_R_C [23]
HP-L C434 .47U/10V_6 HP_L_C [23]
EARPO_R R581 75/F_4 EARP_R
EARPO_L R332 75/F_4 EARP_L
AGND SHIELD

To Internal Speakers

BIT_CLK_AUDIO C674 *27P/50V_4
ACZ_SDIN0_ADC C675 *27P/50V_4
FOR EMI

MIC1_R1 C691 2.2U/6.3V_6 R577 1K/F_4 EXT_MIC_R R579 2.2K_4 D26 RB501V-40 VREFOUT_B_L
MIC1_L1 C689 2.2U/6.3V_6 R576 1K/F_4 EXT_MIC_L R575 2.2K_4 D25 RB501V-40
SENSE_A R574 20K/F_4 SA_MIC#
SENSE_B R582 5.1K/F_4 SA_HP#
C422 2.2U/6.3V_6
TO Audio Jack MIC
TO AUDIO/B CON.

+3V_DVDD
C412 0.047U/10V
[7,10] SPKR
[27] PC_BEEP_EC
U20 NC7SZ86
R328 100K_4
C401 .1U/10V_4
C408 100P/50V_4
R316 10K/F_4
R326 10K_4
R321 150K/F_4

VREFOUT_B_L C696 *1U/6.3V_4
VREF_FLT C430 *10U/6.3V_8
C697 .1U/10V_4
R573 20K/F_4
C699 2.2U/6.3V_6

[19,21,25,26,37] +5VSUS
[11,19,20,23,25,26,28,30,37] +5V
[2,3,7,8,9,10,11,12,13,19,20,21,23,24,25,26,27,28,29,30,34,37,39] +3V

R324 0_6
R322 0_6
C415 1000P/50V_4
C414 1000P/50V_4

AUDIO CONNECTOR

10/07

EARP_L L34 0_6 EARP_L1
EARP_R L35 0_6 EARP_R1
R266 22K/F_6
R267 22K/F_6
R265 *1K/F_4
R263 *1K/F_4
C15 100P/50V_4
C16 100P/50V_4
C29 Clamp-Diode
C26 Clamp-Diode
Change HP-PLG link

CN1
HP-JACK-GREEN
Normal close
headphone close to USB Port
SA_HP# SA_HP# C
D30 *3301D-ESD

+4.75VAVDD
R336 *10K_4
Q44 DMN601K-7

AUDIO JACKS CHANGE TO NORMAL OPEN

C17 100P/50V_4
EXT_MIC_L L32 0_6 MIC_IN_L
EXT_MIC_R L33 0_6 MIC_IN_R
C24 100P/50V_4
CN4
MIC-JACK-PINK
Normal close
Mic close to front side
SA_MIC# SA_MIC# C
D31 *3301D-ESD

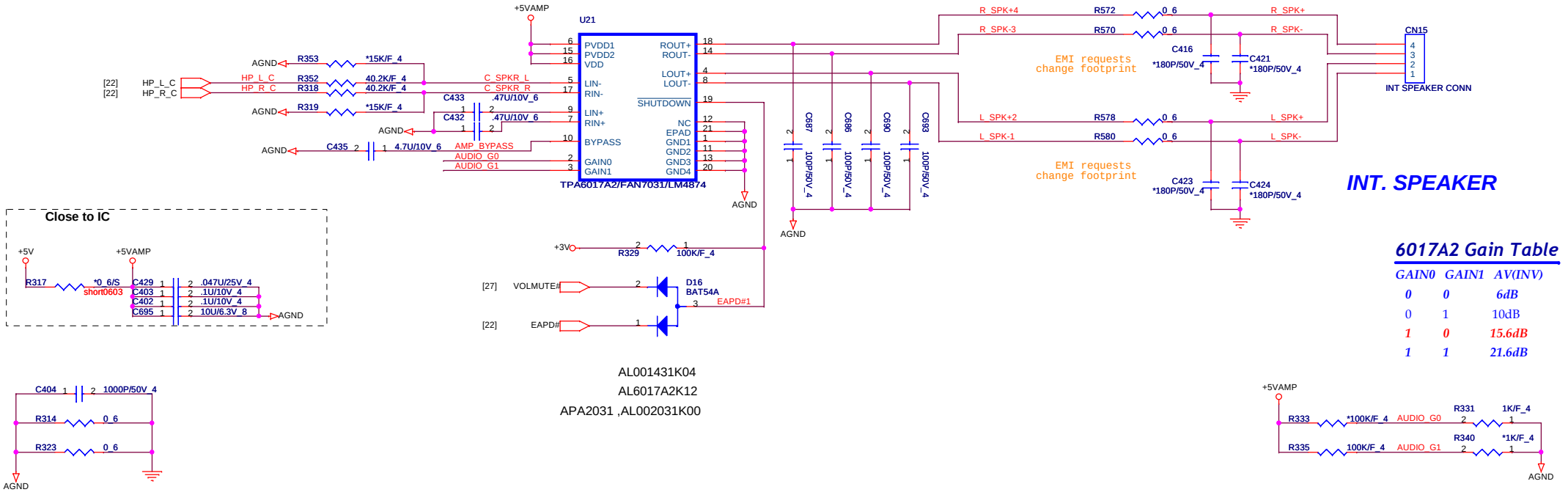
R337
Q43 DMN601K-7
10K_4

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Azalia ALC272/BT CONN	1A

Date: Wednesday, December 02, 2009 Sheet 22 of 44

AUDIO AMPLIFIER



INT. SPEAKER

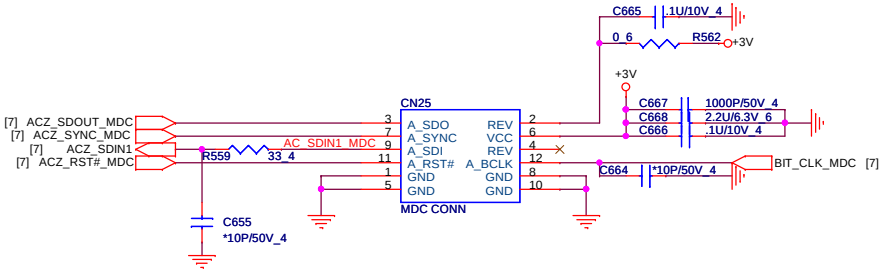
Close to IC

6017A2 Gain Table

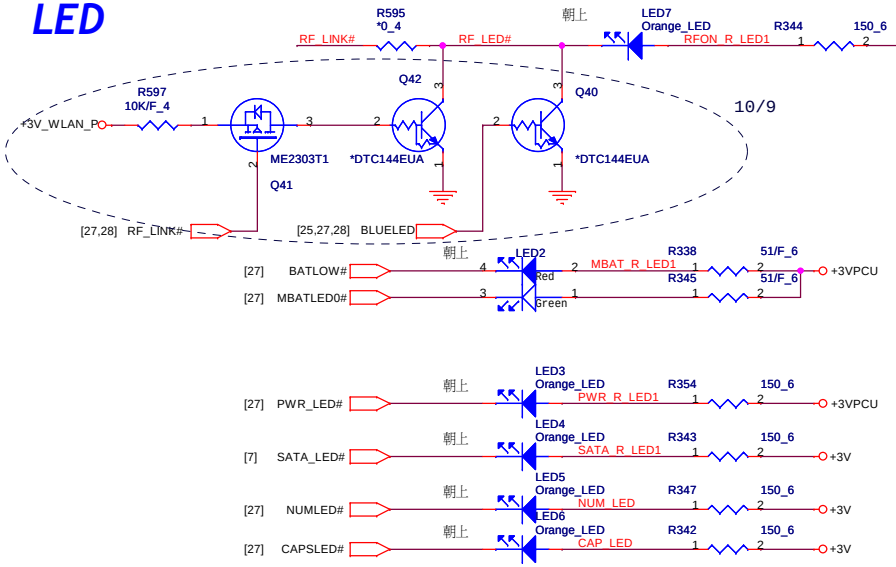
GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

AL001431K04
AL6017A2K12
APA2031 ,AL002031K00

MDC CONNECTOR



LED

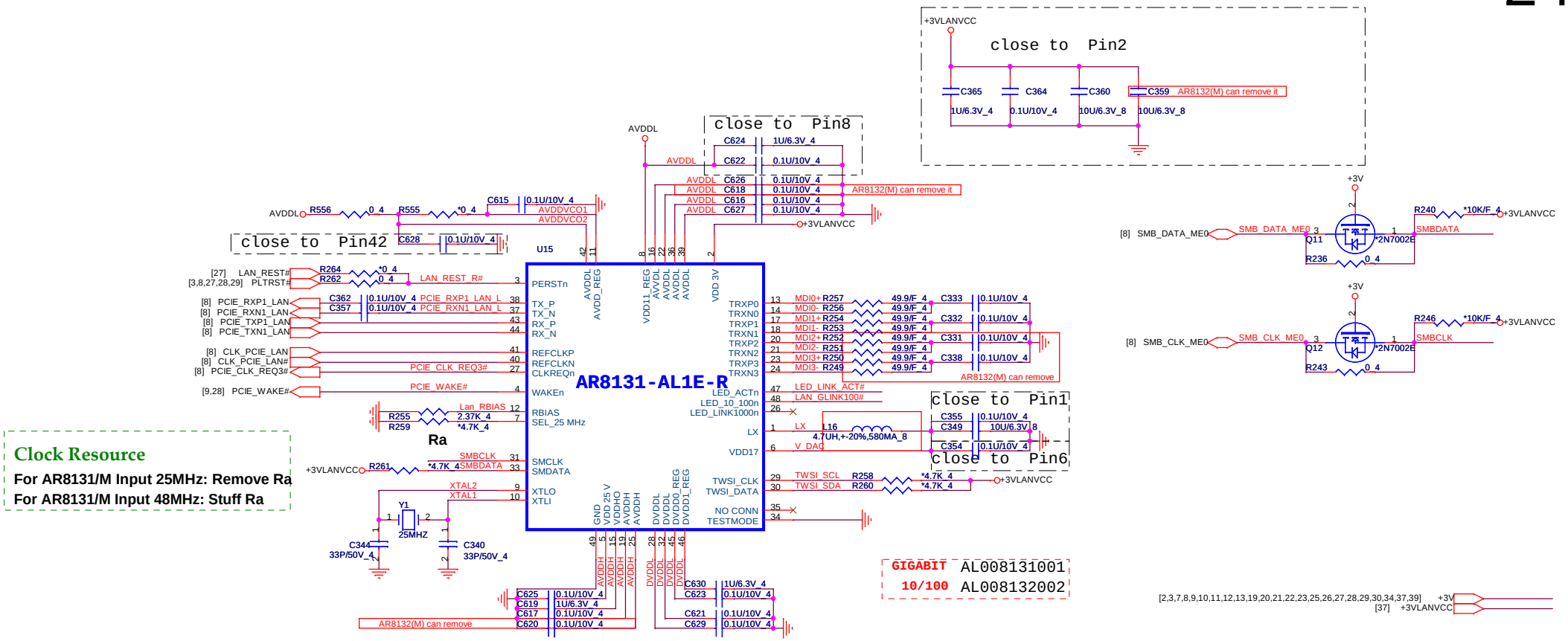


[11,19,20,22,25,26,28,30,37] +5V
[7,19,21,26,27,28,31,32,33,35,37,38,39] +3VPCU
[2,3,7,8,9,10,11,12,13,19,20,21,22,24,25,26,27,28,29,30,34,37,39] +3V

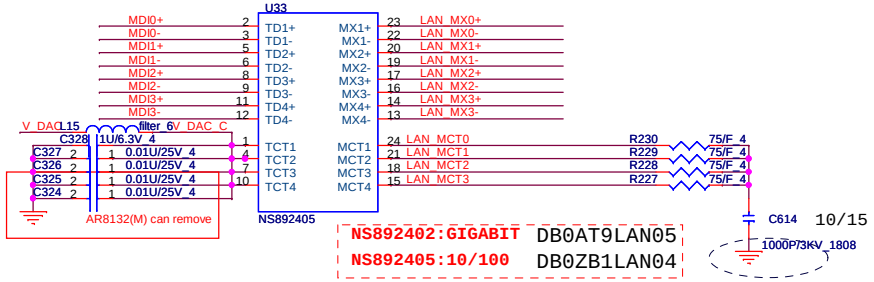
PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA6017/SPK/MDC/LED	1A

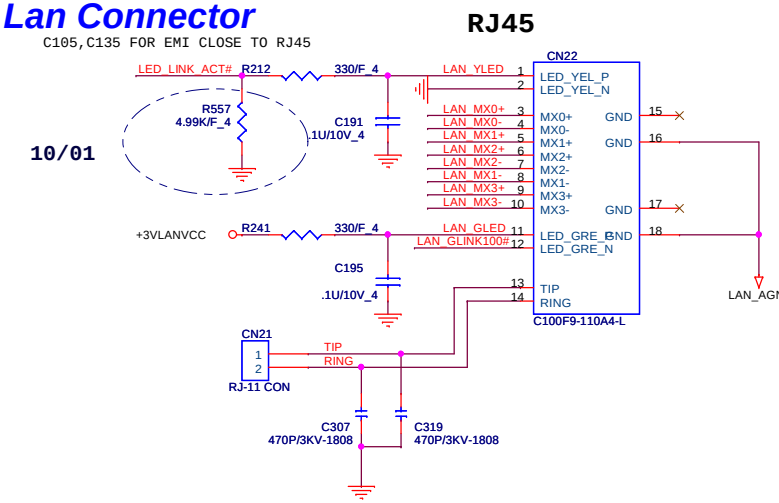
Date: Wednesday, December 02, 2009 Sheet 23 of 44



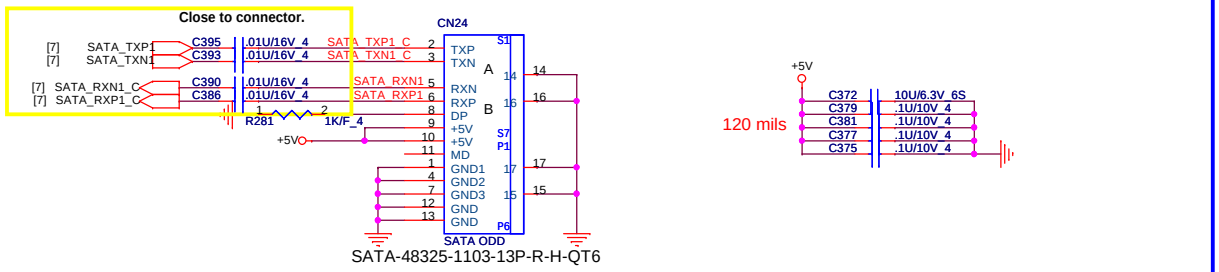
Transformer for 10/100/1000



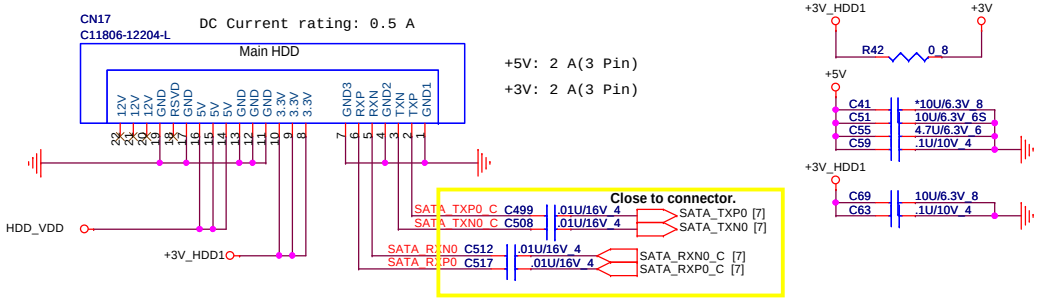
Lan Connector



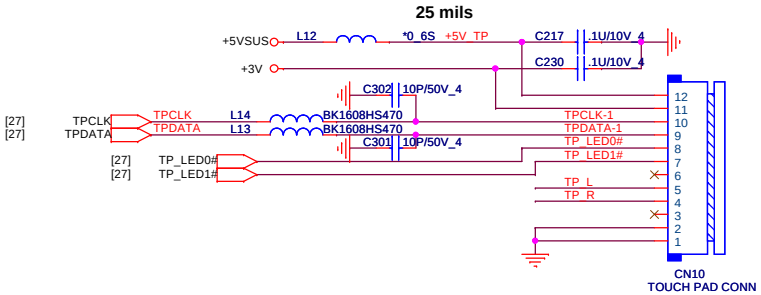
SATA ODD

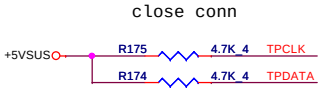


SATA_1 CONNECTOR

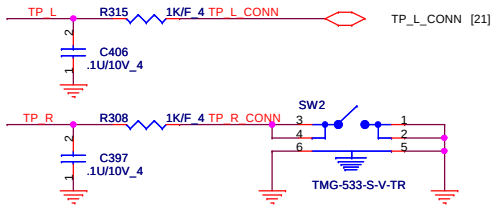


TOUCH PAD CONNECTOR

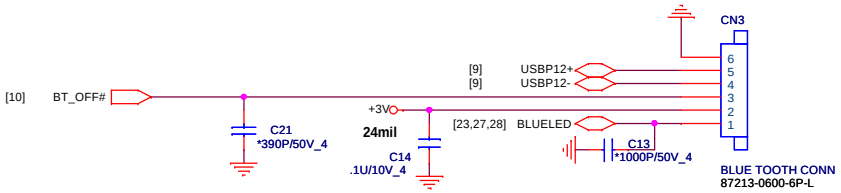




TOUCH PAD L/R SW1,SW2 in QL2 use, SW3,SW4 in SW9 use



Bluetooth



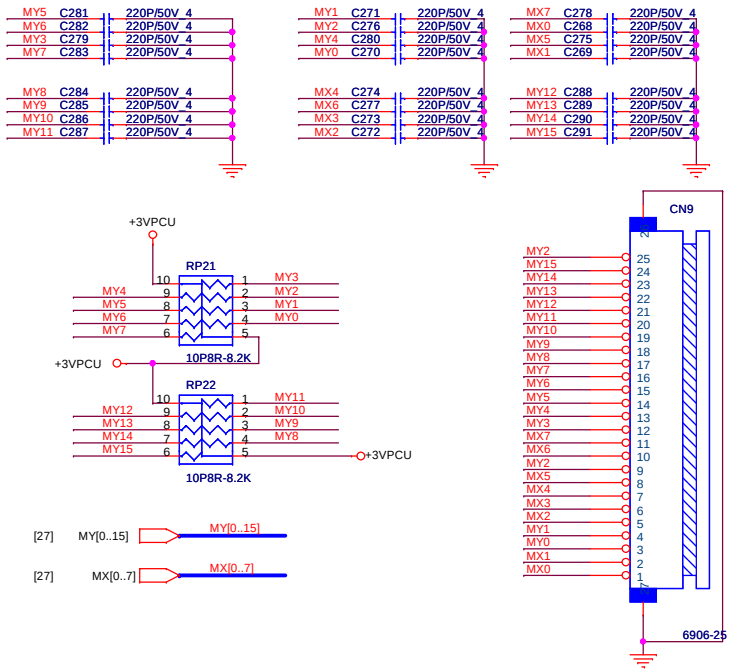
[2,3,7,8,9,10,11,12,13,19,20,21,22,23,24,26,27,28,29,30,34,37,39] +3V
[11,19,20,22,23,26,28,30,37] +5V
[19,21,26,37] +5VSUS

PROJECT : SW9
Quanta Computer Inc.

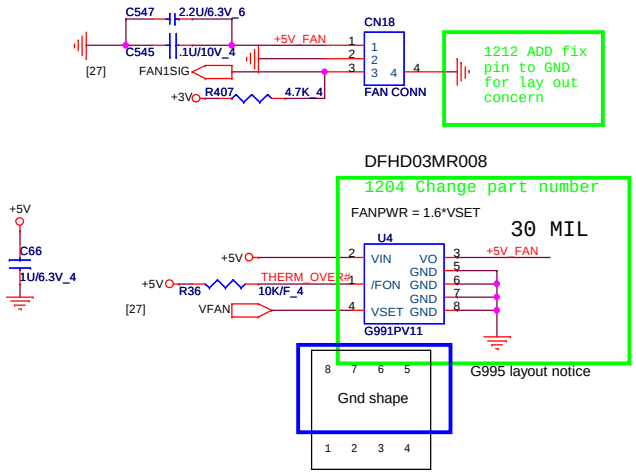
Size	Document Number	Rev
Custom	ODD/HDD/NEW CARD/TP	1A

Date: Wednesday, December 02, 2009 Sheet 25 of 44

KEYBOARD Con.

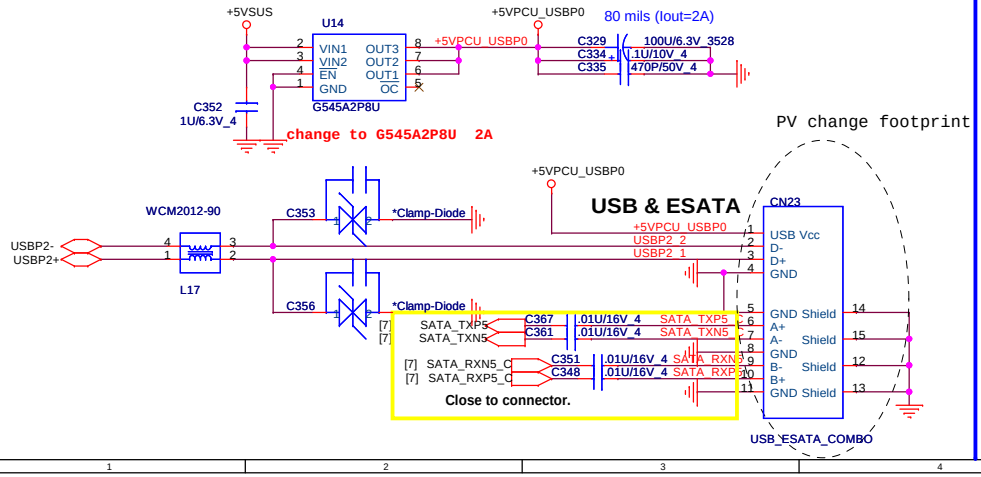


CPU FAN



Capacity board Con.

E-SATA/USB COMBO

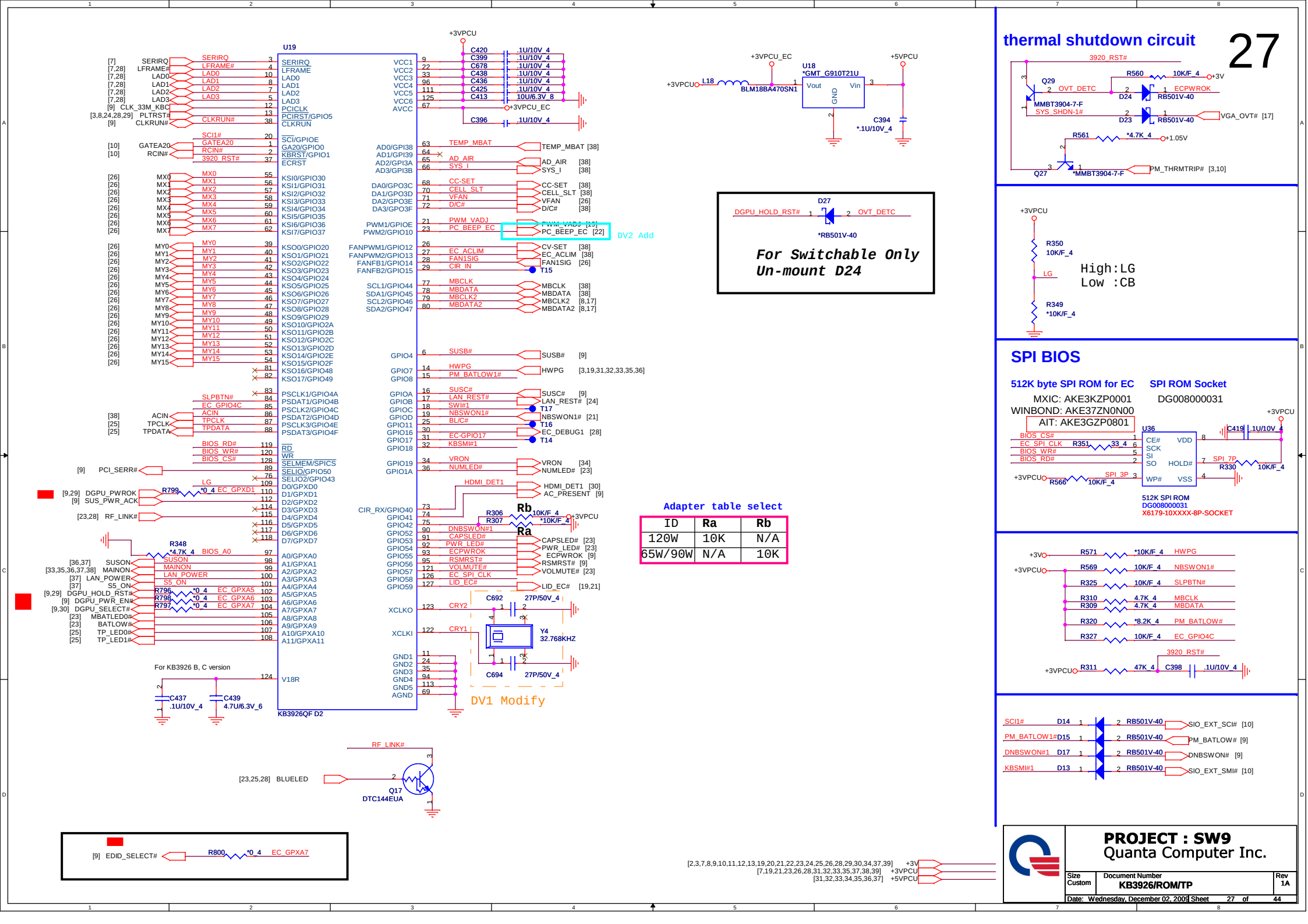


[11,19,20,22,23,25,28,30,37] +5V
[2,3,7,8,9,10,11,12,13,19,20,21,22,23,24,25,27,28,29,30,34,37,39] +3V
[7,19,21,23,27,28,31,32,33,35,37,38,39] +3VPCU
[27,31,32,33,34,35,36,37] +5VPCU

PROJECT : SW9
Quanta Computer Inc.

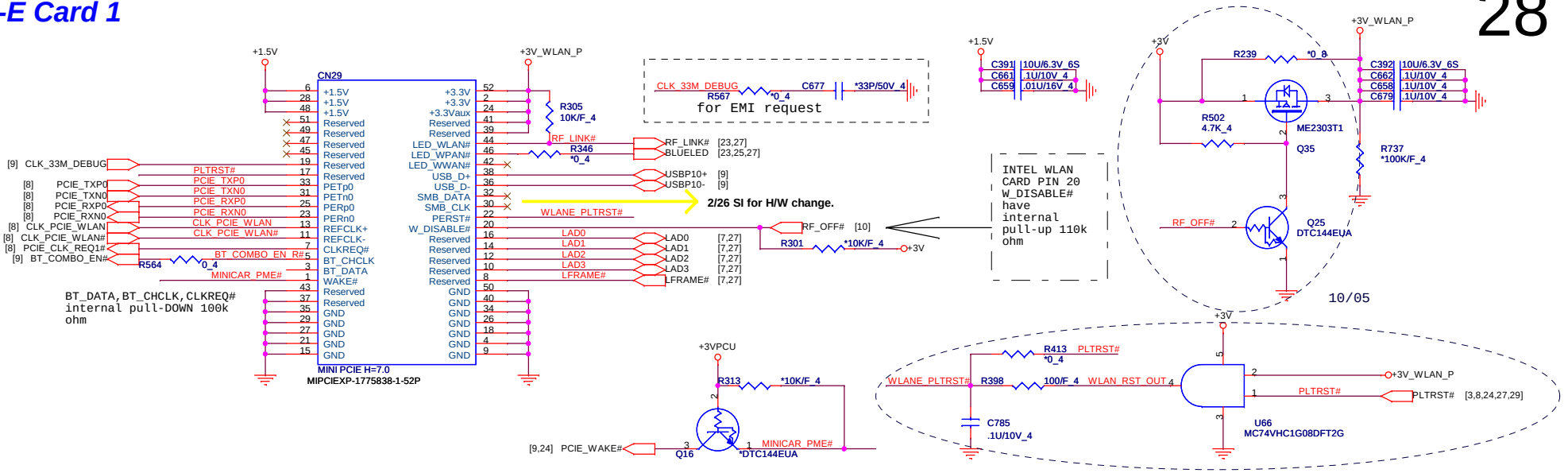
Size	Document Number	Rev
Custom	KB/PWR/ESATA/FAN/CAM/MIC	1A

Date: Wednesday, December 02, 2009 Sheet 26 of 44


U19
KB3926QF D2
SERIRQ
LFRAME#
LAD0
LAD1
LAD2
LAD3
CLK_33M_KBC
PLTRST#
CLKRUN#
SCI1#
GATEA20
RCIN#
3920_RST#
MX0
MX1
MX2
MX3
MX4
MX5
MX6
MX7
MY0
MY1
MY2
MY3
MY4
MY5
MY6
MY7
MY8
MY9
MY10
MY11
MY12
MY13
MY14
MY15
SLPBTN#
EC_GPIO4C
ACIN
TPCLK
TPDATA
BIOS_RD#
BIOS_WR#
BIOS_CS#
PCI_SERR#
LG
DGPU_PWROK
SUS_PWR_ACK
RF_LINK#
R799
*0_4
EC_GPXD1
R348
*4.7K_4
BIOS_A0
SUSON
MAINON
LAN_POWER
S5_ON
DGPU_HOLD_RST#
DGPU_PWR_EN#
DGPU_SELECT#
MBATLED0#
BATLOW#
TP_LED0#
TP_LED1#
EC_GPXA5
EC_GPXA6
EC_GPXA7
For KB3926 B, C version
C437
.1U/10V_4
C439
4.7U/6.3V_6
+3VPCU
C420
C399
C678
C438
C436
C425
C413
.1U/10V_4
10U/6.3V_8
+3VPCU_EC
C396
TEMP_MBAT
AD_AIR
SYS_I
CC-SET
CELL_SLT
VFAN
D/C#
PWM_VADJ
PC_BEEP_EC
EC_ACLIM
FAN1SIG
CIR_IN
MBCLK
MBDATA
MBCLK2
MBDATA2
SUSB#
HWPG
PM_BATLOW1#
SUSC#
LAN_REST#
SWI#1
NBSWON1#
BL/C#
EC-GPIO17
KBSMI#1
VRON
NUMLED#
HDMI_DET1
AC_PRESENT
R306
R307
10K/F_4
*10K/F_4
Rb
Ra
DNBSWON#1
CAPSLED#
PWR_LED#
ECPWROK
RSMRST#
VOLMUTE#
EC_SPI_CLK
LID_EC#
C692
27P/50V_4
C694
27P/50V_4
Y4
32.768KHZ
CRY2
CRY1
DV1 Modify
DV2 Add
RF_LINK#
[23,25,28] BLUELED
Q17
DTC144EUA
R800
EDID_SELECT#
+3VPCU_EC
U18
*GMT_G910T21U
Vout
Vin
GND
L18
BLM18BA470SN1
+5VPCU
C394
*.1U/10V_4
D27
DGPU_HOLD_RST#
OVT_DETC
*RB501V-40
For Switchable Only
Un-mount D24
Adapter table select
ID
Ra
Rb
120W
10K
N/A
65W/90W
N/A
10K
thermal shutdown circuit
27
3920_RST#
Q29
OVT_DETC
ECPWROK
MMBT3904-7-F
SYS_SHDN-1#
R560
10K/F_4
D24
RB501V-40
D23
RB501V-40
VGA_OVT# [17]
R561
*4.7K_4
+1.05V
Q27
*MMBT3904-7-F
PM_THRMTRIP# [3,10]
+3VPCU
R350
10K/F_4
LG
High:LG
Low :CB
R349
*10K/F_4
SPI BIOS
512K byte SPI ROM for EC
SPI ROM Socket
MXIC: AKE3KZP0001
WINBOND: AKE37ZN0N00
AIT: AKE3GZP0801
DG008000031
U36
BIOS_CS#
EC_SPI_CLK
BIOS_WR#
BIOS_RD#
CE#
SCK
SI
SO
WP#
VDD
HOLD#
VSS
R351
33_4
R566
10K/F_4
SPI_3P
SPI_7P
R330
10K/F_4
C419
.1U/10V_4
512K SPI ROM
DG008000031
X6179-10XXXX-8P-SOCKET
+3V
+3VPCU
R571
*10K/F_4
HWPG
R569
10K/F_4
NBSWON1#
R325
10K/F_4
SLPBTN#
R310
4.7K_4
MBCLK
R309
4.7K_4
MBDATA
R320
*8.2K_4
PM_BATLOW#
R327
10K/F_4
EC_GPIO4C
3920_RST#
R311
47K_4
C398
.1U/10V_4
SCI1#
D14
RB501V-40
SIO_EXT_SCI# [10]
PM_BATLOW1#
D15
PM_BATLOW# [9]
DNBSWON#1
D17
DNBSWON# [9]
KBSMI#1
D13
SIO_EXT_SMI# [10]
[2,3,7,8,9,10,11,12,13,19,20,21,22,23,24,25,26,28,29,30,34,37,39] +3V
[7,19,21,23,26,28,31,32,33,35,37,38,39] +3VPCU
[31,32,33,34,35,36,37] +5VPCU
PROJECT : SW9
Quanta Computer Inc.
Size
Custom
Document Number
KB3926/ROM/TP
Rev
1A
Date: Wednesday, December 02, 2009
Sheet
27
of
44

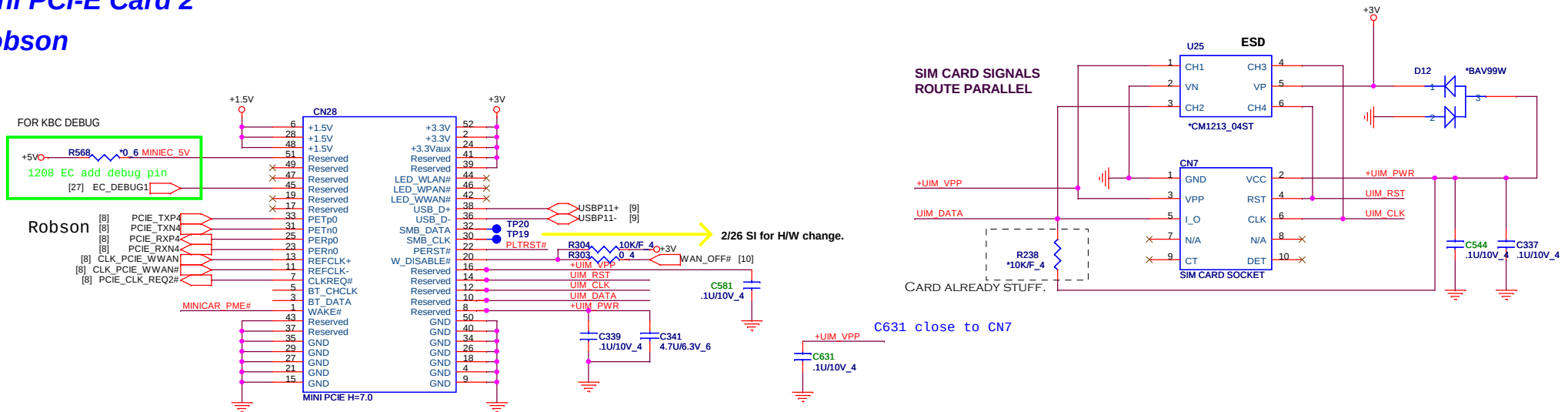
Mini PCI-E Card 1

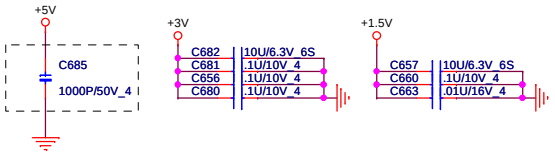
WLAN

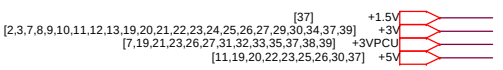


Mini PCI-E Card 2

Robson







PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCIE CONN X2	1A

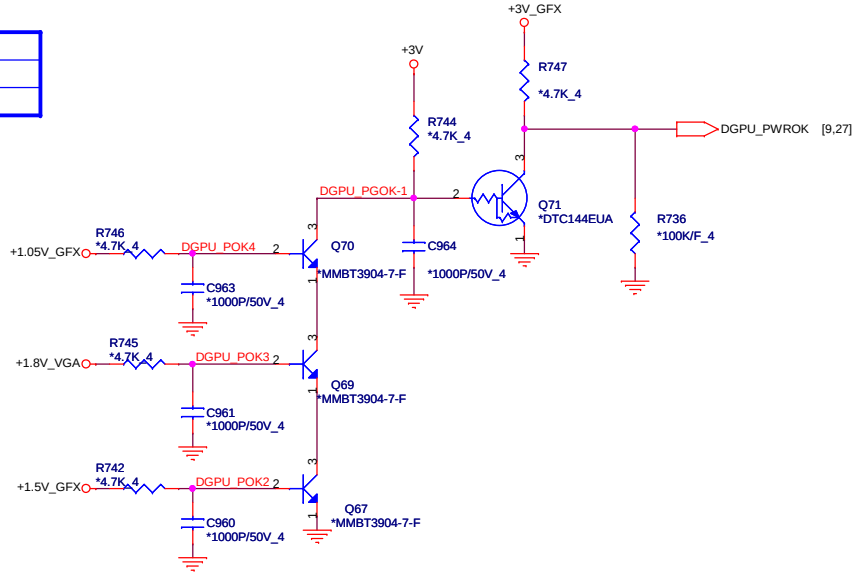
Date: Wednesday, December 02, 2009 Sheet 28of 44

DEL Switch IC

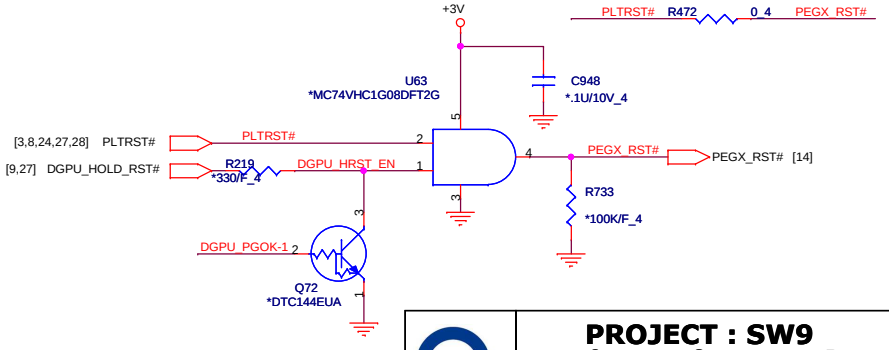
DEL Switch IC

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

SELx	Ay
LOW	B1
HIGH	B2



Discrete Only



PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LVDS / CRT Switch	1A

Date: Wednesday, December 02, 2009 Sheet 29 of 44

DGPU_HDMI

[16] H_TX2_HDMI+ C226 *.1U/10V_4 DGPU_TX2_HDMI+
[16] H_TX2_HDMI- C233 *.1U/10V_4 DGPU_TX2_HDMI-
[16] H_TX1_HDMI+ C219 *.1U/10V_4 DGPU_TX1_HDMI+
[16] H_TX1_HDMI- C209 *.1U/10V_4 DGPU_TX1_HDMI-
[16] H_TX0_HDMI+ C243 *.1U/10V_4 DGPU_TX0_HDMI+
[16] H_TX0_HDMI- C252 *.1U/10V_4 DGPU_TX0_HDMI-

[16] H_TXC_HDMI+ C202 *.1U/10V_4 DGPU_TXC_HDMI+
[16] H_TXC_HDMI- C193 *.1U/10V_4 DGPU_TXC_HDMI-

HDMISwitch

U64 PI3HDMI201

DGPU_TXC_HDMI- 55 CLK-A
DGPU_TXC_HDMI+ 56 CLK+A
DGPU_TX0_HDMI- 2 D0-A
DGPU_TX0_HDMI+ 3 D0+A
DGPU_TX1_HDMI- 5 D1-A
DGPU_TX1_HDMI+ 6 D1+A
DGPU_TX2_HDMI- 8 D2-A
DGPU_TX2_HDMI+ 9 D2+A

HPD_SINK 47 HDMI_DET_S
SDA_SINK 46 HDMI_SDATA
SCL_SINK 45 HDMI_SCLK

CLK- 43 C_TXC_HDMI-
CLK+ 42 C_TXC_HDMI+
D0- 40 C_TX0_HDMI-
D0+ 39 C_TX0_HDMI+
D1- 37 C_TX1_HDMI-
D1+ 36 C_TX1_HDMI+
D2- 34 C_TX2_HDMI-
D2+ 33 C_TX2_HDMI+

[17] HDMI_DET 51 HPDA
[16] HDMI_SDA_DGPU 52 SDAA
[16] HDMI_SCL_DGPU 53 SCLA
[7] HDMI_HPD_CON 23 HPDB
[7] SDVO_DATA 24 SDAB
[7] SDVO_CLK 25 SCLB

PAD_GND 57
GND 4, 10, 16, 22, 32, 38, 44, 54

[7] IN_CLK# 11 CLK-B
[7] IN_CLK 12 CLK+B
[7] IN_D0# 14 D0-B
[7] IN_D0 15 D0+B
[7] IN_D1# 17 D1-B
[7] IN_D1 18 D1+B
[7] IN_D2# 20 D2-B
[7] IN_D2 21 D2+B

EQ_S1 26, EQ_S0 28, OC_S2 29, OC_S1 30, OC_S0 31, OE# 50, SEL2 27, SEL1 49

HSW_EQS1 26, HSW_EQS0 28, HSW_OCS2 29, HSW_OCS1 30, HSW_OCS0 31, HSW_ON# 50, HSW_SEL2 27, HSW_SEL1 49

+3V → VDD 48, 41, 35, 19, 13, 7, 1

To HDMI Conn.

IGPU_HDMI

+3V
R486 2K/F_4 SDVO_DATA
R500 2K/F_4 SDVO_CLK

+3V
C955 0.1U/10V_4
C954 0.1U/10V_4
C945 0.1U/10V_4
C950 0.1U/10V_4

OC SETTING
S2 S1 S0 = 1 : 1 : 1 500mV 0dB Defualt
S2 S1 S0 = 1 : 1 : 0 750mV 0dB
S2 S1 S0 = 1 : 0 : 1 1000mV 0dB
S2 S1 S0 = 1 : 0 : 0 600mV 0dB
S2 S1 S0 = 0 : 1 : 1 500mV 0dB
S2 S1 S0 = 0 : 1 : 0 500mV 1.5dB
S2 S1 S0 = 0 : 0 : 1 500mV 3.5dB
S2 S1 S0 = 0 : 0 : 0 500mV 6dB

EQ SETTING
S1 S0 = 1 : 1 3dB Defualt
S1 S0 = 1 : 0 8dB
S1 S0 = 0 : 1 3dB
S1 S0 = 0 : 0 15dB

HSW_EQS1 R628 *4.7K_4
HSW_EQS0 R627 *4.7K_4
HSW_OCS2 R626 *4.7K_4
HSW_OCS1 R625 *4.7K_4
HSW_OCS0 R624 *4.7K_4
HSW_ON# R623 4.7K_4

OE#	SEL2	SEL1	Ay
0	X	1	A
0	1	0	B

+3V
R630 *4.7K_4
HSW_SEL1
Q33 *DTC144EUA
R629 4.7K_4
DGPU_SELECT# DGPU_SELECT# [9,27]
R631 *0_4 HSW_SEL2
R632 4.7K_4
+3V

SEL	FUNCTION
LOW	DGPU
HIGH	IGPU

Mount R629 / R632 for UMA only

Only for NVIDIA

+3V_GFX
Q26 *2N7002E
R146 *499/F_4 DGPU_TXC_HDMI-
R150 *499/F_4 DGPU_TXC_HDMI+
R144 *499/F_4 DGPU_TX0_HDMI-
R137 *499/F_4 DGPU_TX0_HDMI+
R151 *499/F_4 DGPU_TX1_HDMI-
R156 *499/F_4 DGPU_TX1_HDMI+
R136 *499/F_4 DGPU_TX2_HDMI-
R124 *499/F_4 DGPU_TX2_HDMI+

DGPU_TXC_HDMI- RP35 *0_4P2R C_TXC_HDMI-
DGPU_TXC_HDMI+ C_TXC_HDMI+
DGPU_TX0_HDMI- RP38 *0_4P2R C_TX0_HDMI-
DGPU_TX0_HDMI+ C_TX0_HDMI+
DGPU_TX1_HDMI- RP36 *0_4P2R C_TX1_HDMI-
DGPU_TX1_HDMI+ C_TX1_HDMI+
DGPU_TX2_HDMI- RP37 *0_4P2R C_TX2_HDMI-
DGPU_TX2_HDMI+ C_TX2_HDMI+

HDMI_DET R469 *0_4 HDMI_DET_S
HDMI_SCL_DGPU R458 *4.7K_4 HDMI_SCLK
HDMI_SDA_DGPU R457 *4.7K_4 HDMI_SDATA
D21 *RB501V-40
D28 *RB501V-40
*FDV301N Q23
*FDV301N Q22
+3V_GFX
+3V

For Switchable Only

HDMI PORT

CN20 HDMI CONN
C_TX2_HDMI+ 1 D2+
C_TX2_HDMI- 3 D2 Shield
C_TX1_HDMI+ 4 D2-
C_TX1_HDMI- 6 D1+
C_TX0_HDMI- 9 D1 Shield
C_TX0_HDMI+ 7 D1-
C_TXC_HDMI- 12 D0+
C_TXC_HDMI+ 10 D0 Shield
D0-
CK+
CK Shield
CK-
CE Remote
NC
DDC CLK 15 HDMISCL
DDC DATA 16 HDMISDA
GND 17, 18
+5V 19
HP DET
SHELL1 20
SHELL2 21

+5V_HDMIC
D9 RB501V-40
D29 RB501V-40
R112 2.2K/F_4
R109 2.2K/F_4
R111 0_4
R110 0_4
C567 *10P/50V_4
C566 *10P/50V_4
HDMI_SCLK
HDMI_SDATA
+5V
F2 FUSE1A6V_POLY
[27] HDMI_DET1
R464 *0_4
HDMI_DET_S
R461 10K/F_4
HDMI_DET_N
L26 BLM18BA470SN1D
HDMI_DET_C
C564 220P/50V_4
D22 BAV99W
R488 110K/F_4

+5V_HDMIC
C157 *.01U/16V_4
for EMI request

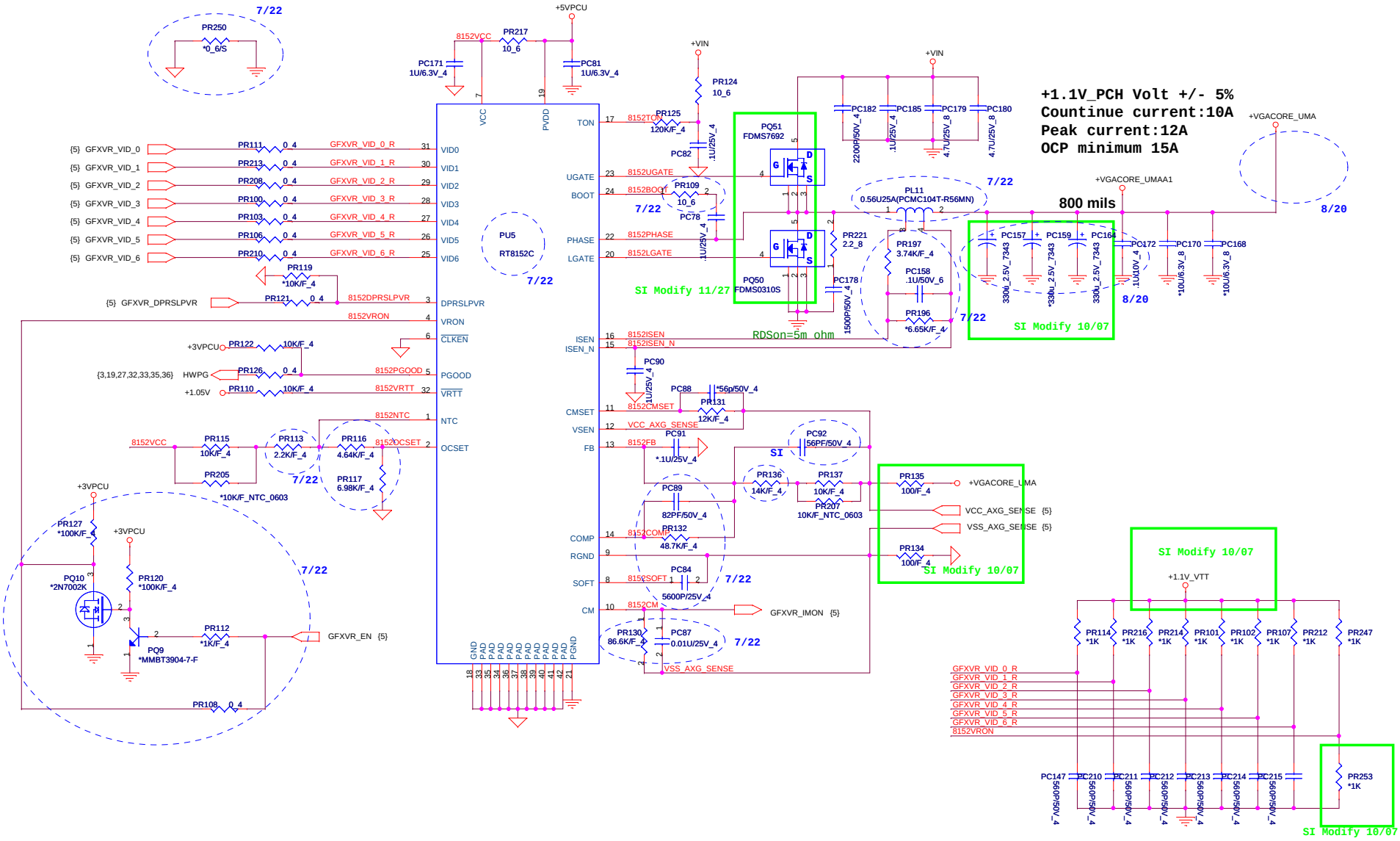
R806 *100/F_4 C_TX2_HDMI+ / C_TX2_HDMI-
R807 *100/F_4 C_TX1_HDMI+ / C_TX1_HDMI-
R808 *100/F_4 C_TX0_HDMI+ / C_TX0_HDMI-
R809 *100/F_4 C_TXC_HDMI+ / C_TXC_HDMI-

Close to CN20

PROJECT : SW9
Quanta Computer Inc.

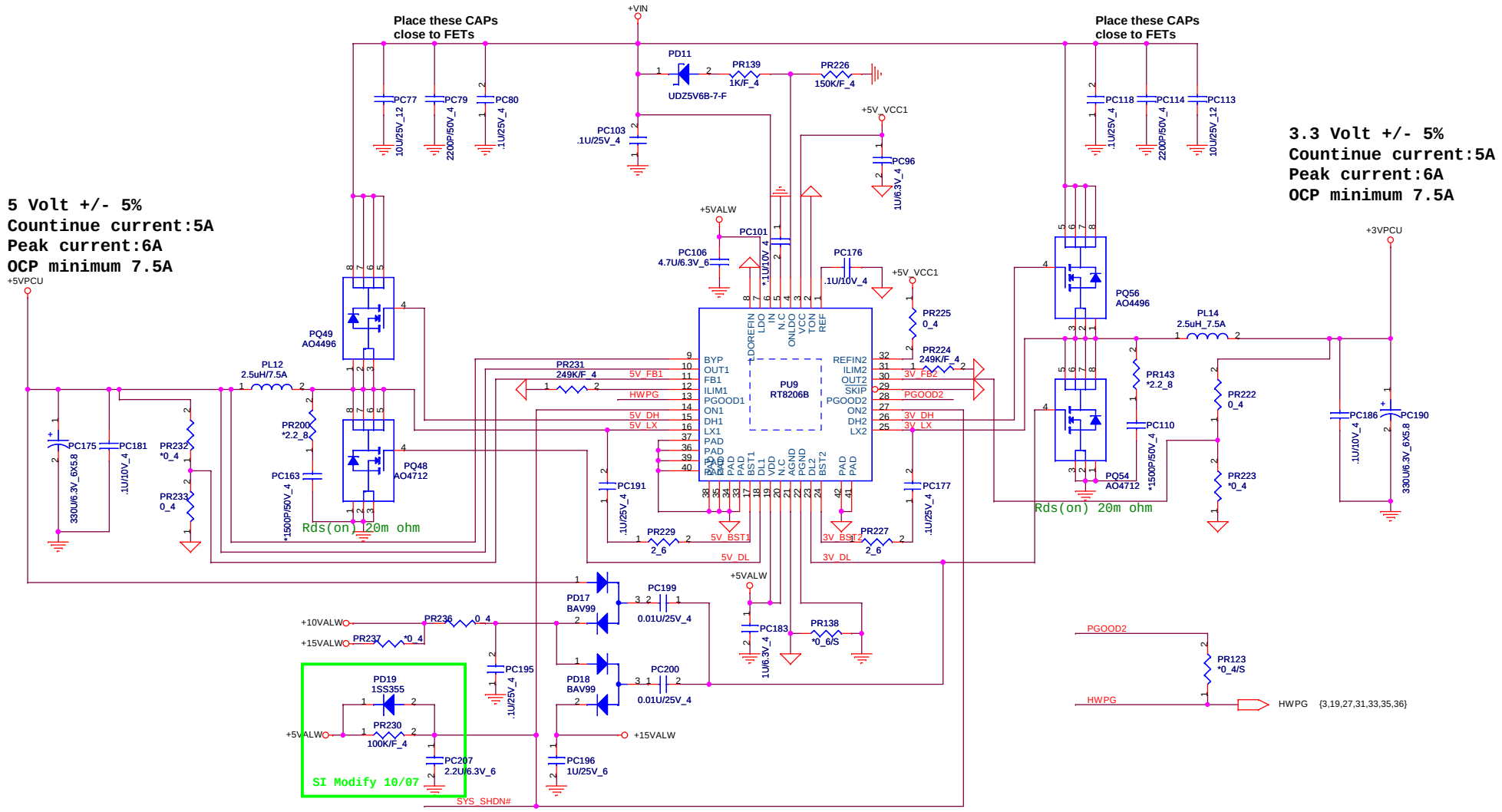
Size	Document Number	Rev
A3	HDMI Switch	1A

Date: Wednesday, December 02, 2009 Sheet 30 of 44

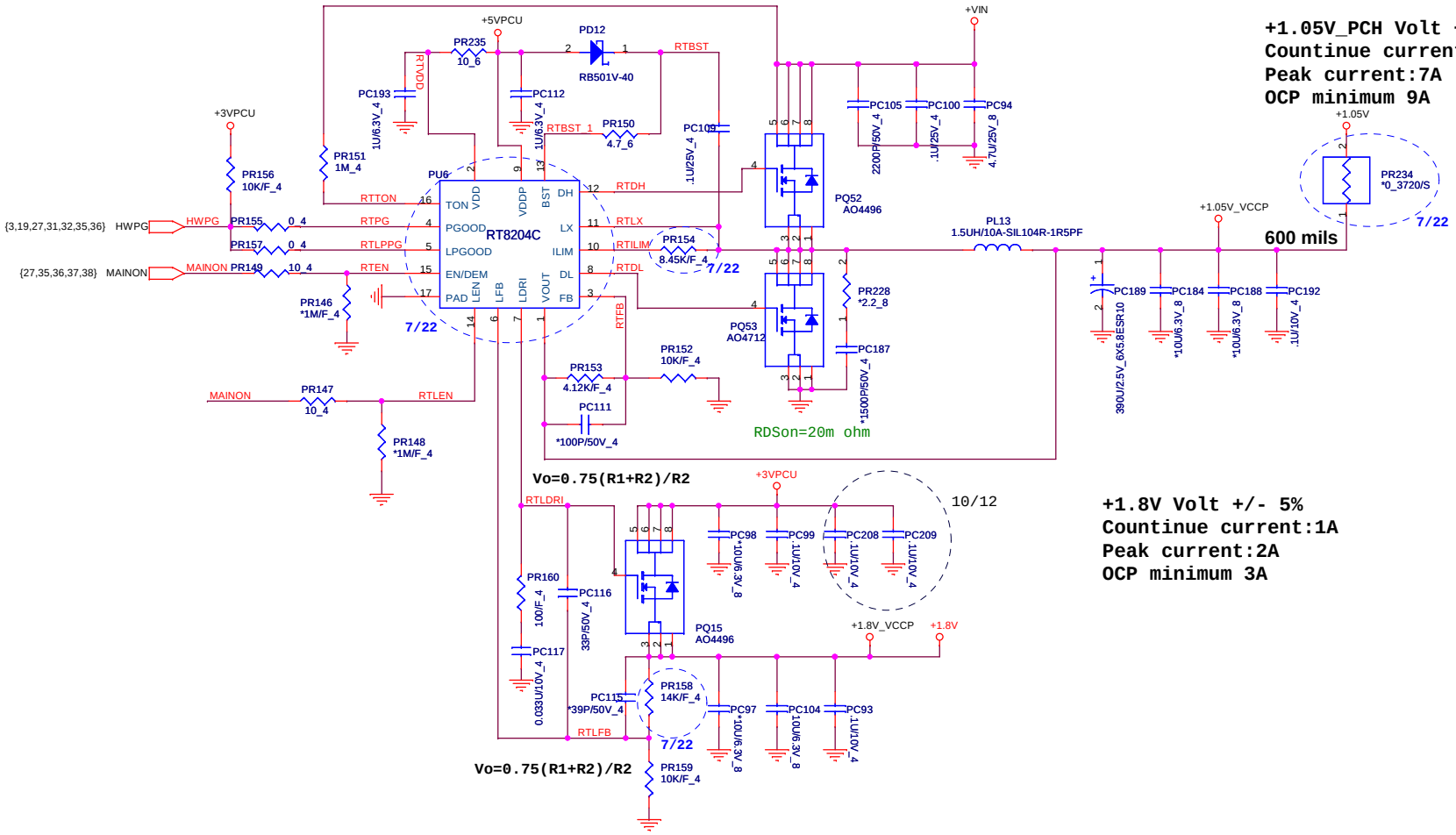


PROJECT : SW9	
Quanta Computer Inc.	
Size: Custom	Document Number: UMA GPU CORE (RT8152A)
Rev: 1A	
Date: Wednesday, December 02, 2009	Sheet 31 of 44

DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW



PROJECT : SW9	
Quanta Computer Inc.	
Size: Custom	Document Number: +5V/+3V (RT8206B)
Rev: 1A	
Date: Wednesday, December 02, 2009	Sheet 32 of 44



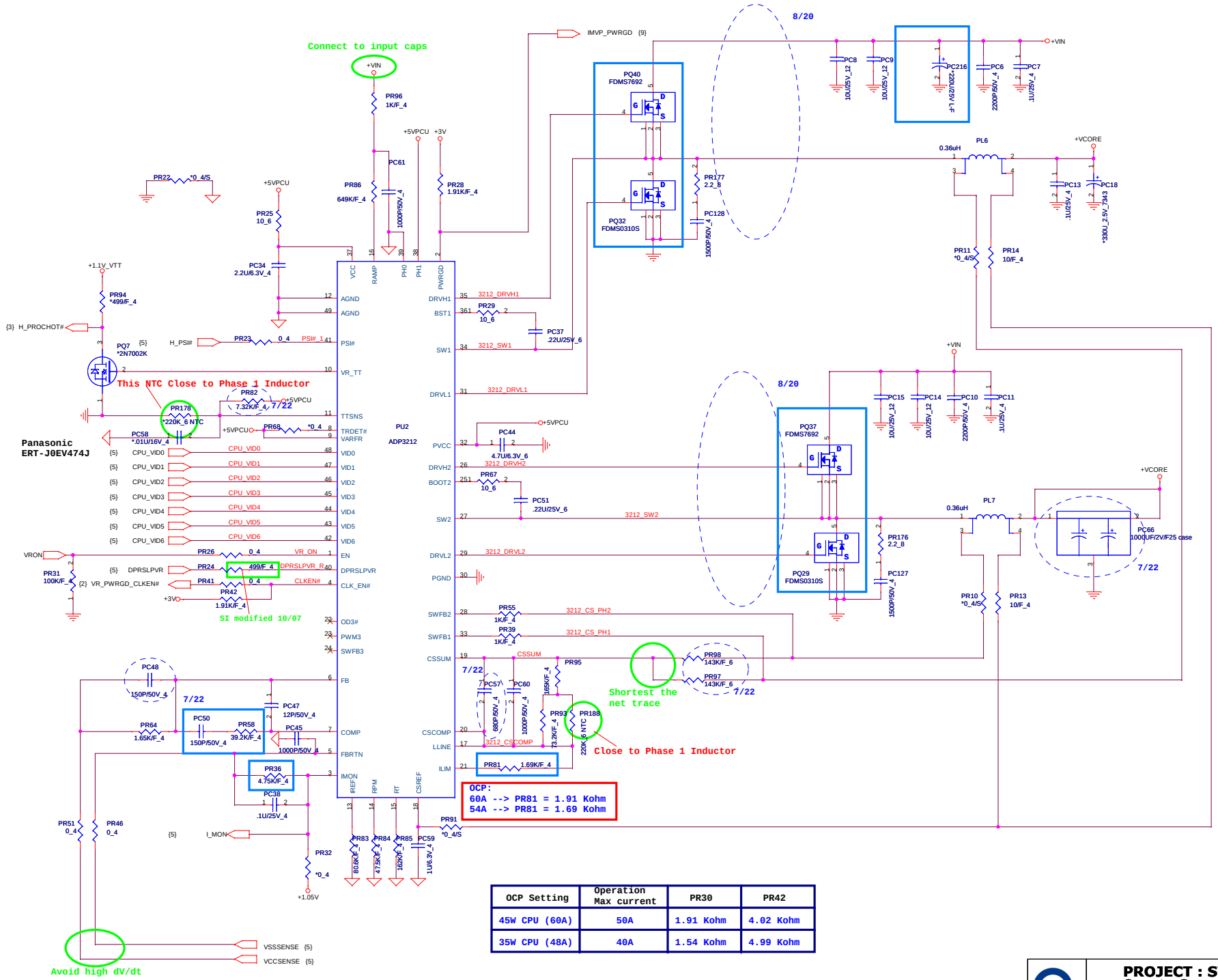
+1.05V_PCH Volt +/- 5%
Countinue current:4A
Peak current:7A
OCP minimum 9A

+1.8V Volt +/- 5%
Countinue current:1A
Peak current:2A
OCP minimum 3A

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH +1.05V (RT8204)	1A

Date: Wednesday, December 02, 2009 Sheet 33 of 44



OCP Setting	Operation Max current	PR30	PR42
45W CPU (60A)	50A	1.91 Kohm	4.02 Kohm
35W CPU (48A)	40A	1.54 Kohm	4.99 Kohm

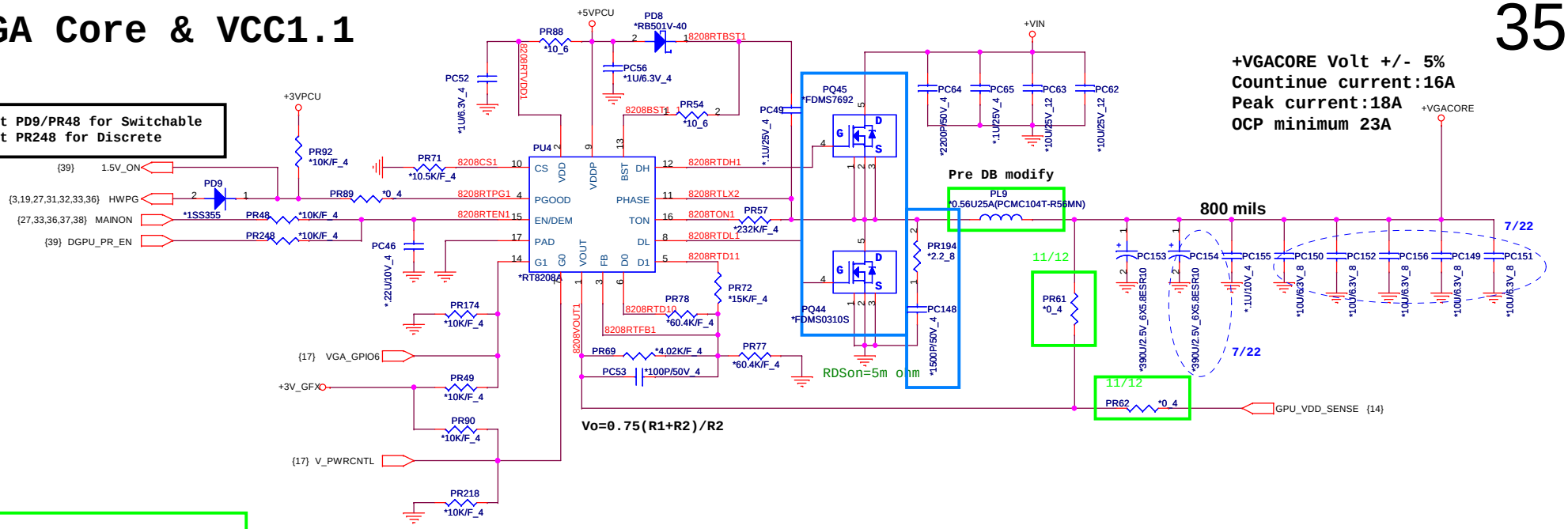
PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core (ADP3212)	1A

Date: Wednesday, December 02, 2009 Sheet 34 of 44

VGA Core & VCC1.1

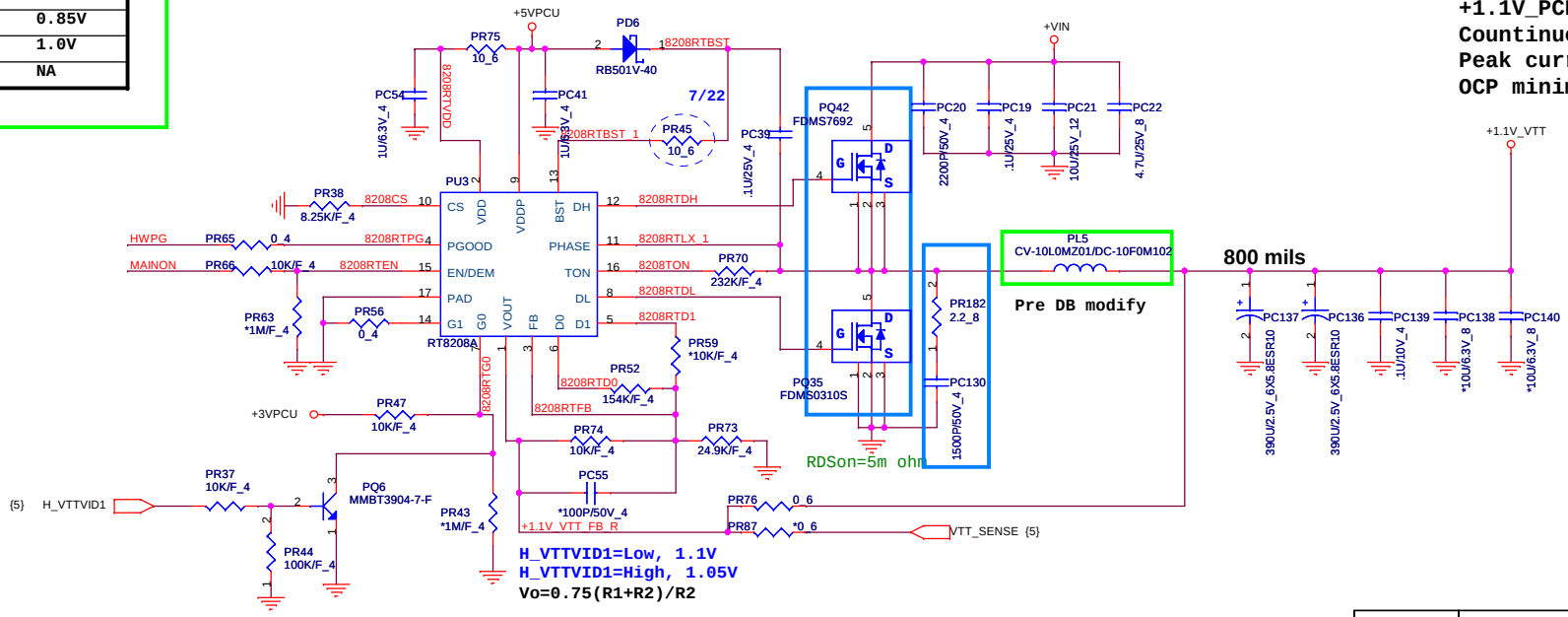
1 : un-Mount PD9/PR48 for Switchable
2 : un-Mount PR248 for Discrete



+VGACORE Volt +/- 5%
Countinue current:16A
Peak current:18A
OCP minimum 23A

4/1

VGA_GPIO6 GPIO6	V_PWRCNTL GPIO5	N10M-GS
0	0	0.8V
0	1	0.85V
1	0	1.0V
1	1	NA

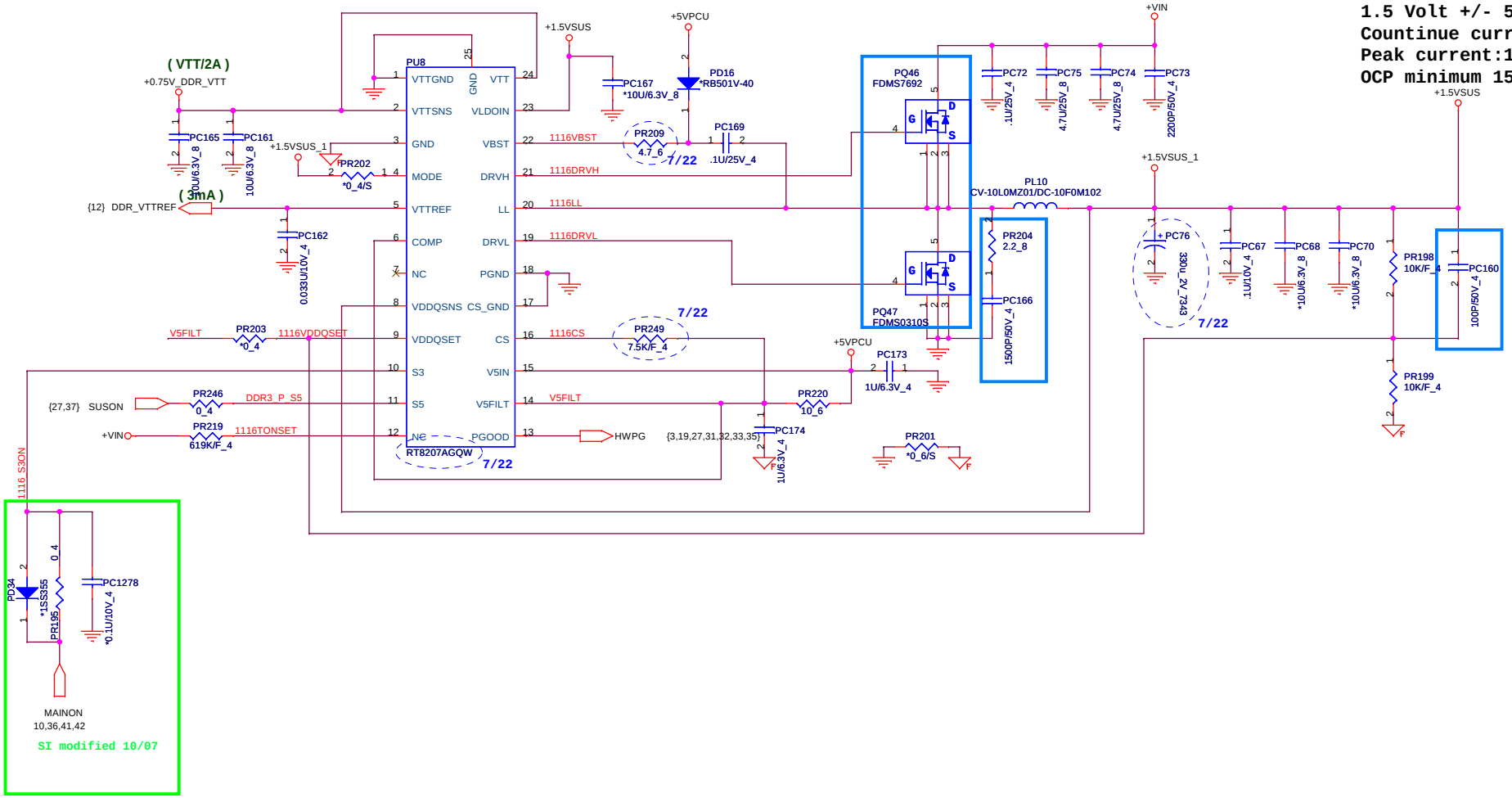


+1.1V_PCH Volt +/- 5%
Countinue current:12A
Peak current:15A
OCP minimum 18A

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1V_VTT/VGA Core RT820A	1A

Date: Wednesday, December 02, 2009 Sheet 35 of 44

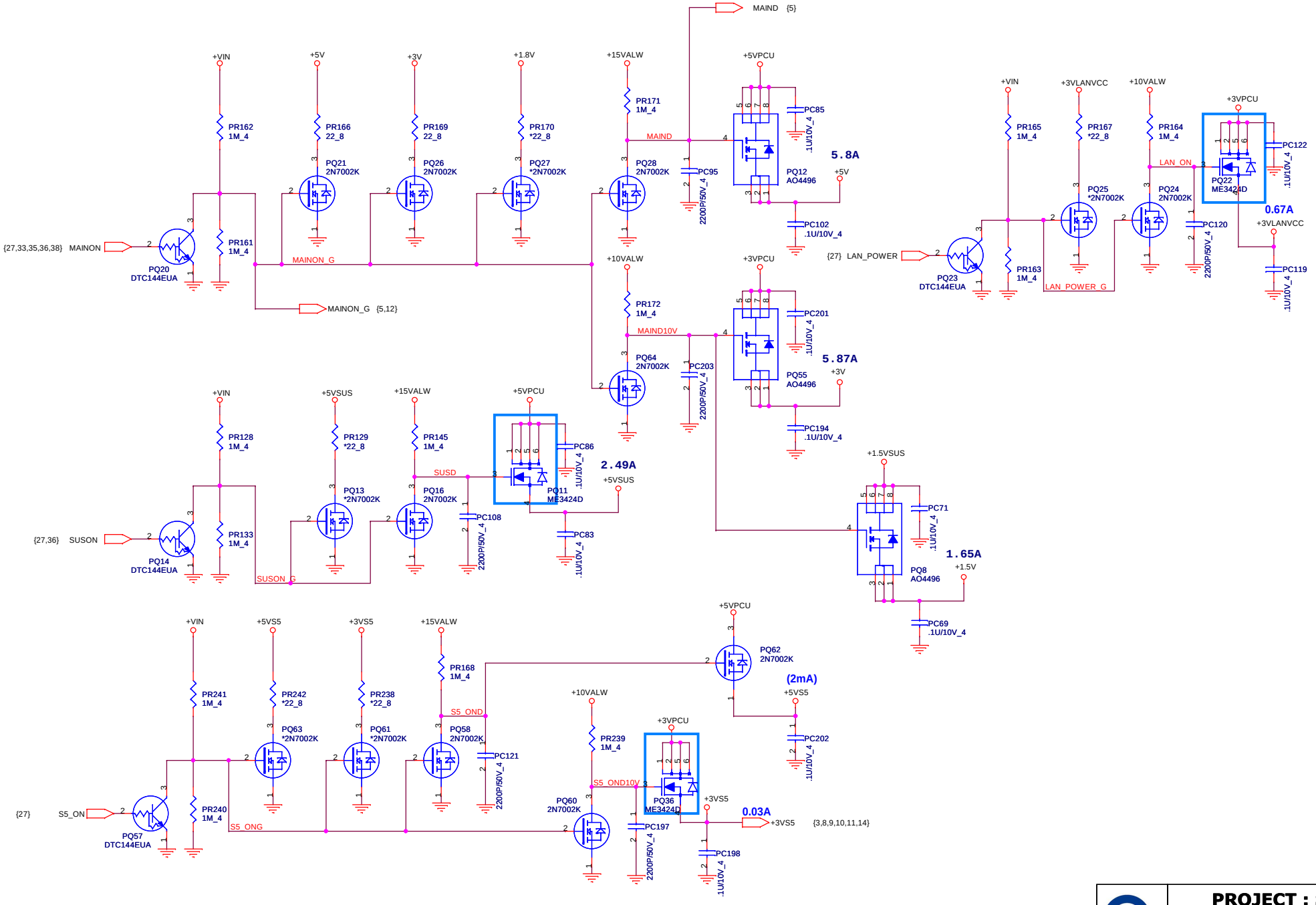


1.5 Volt +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 (RT8207)	1A

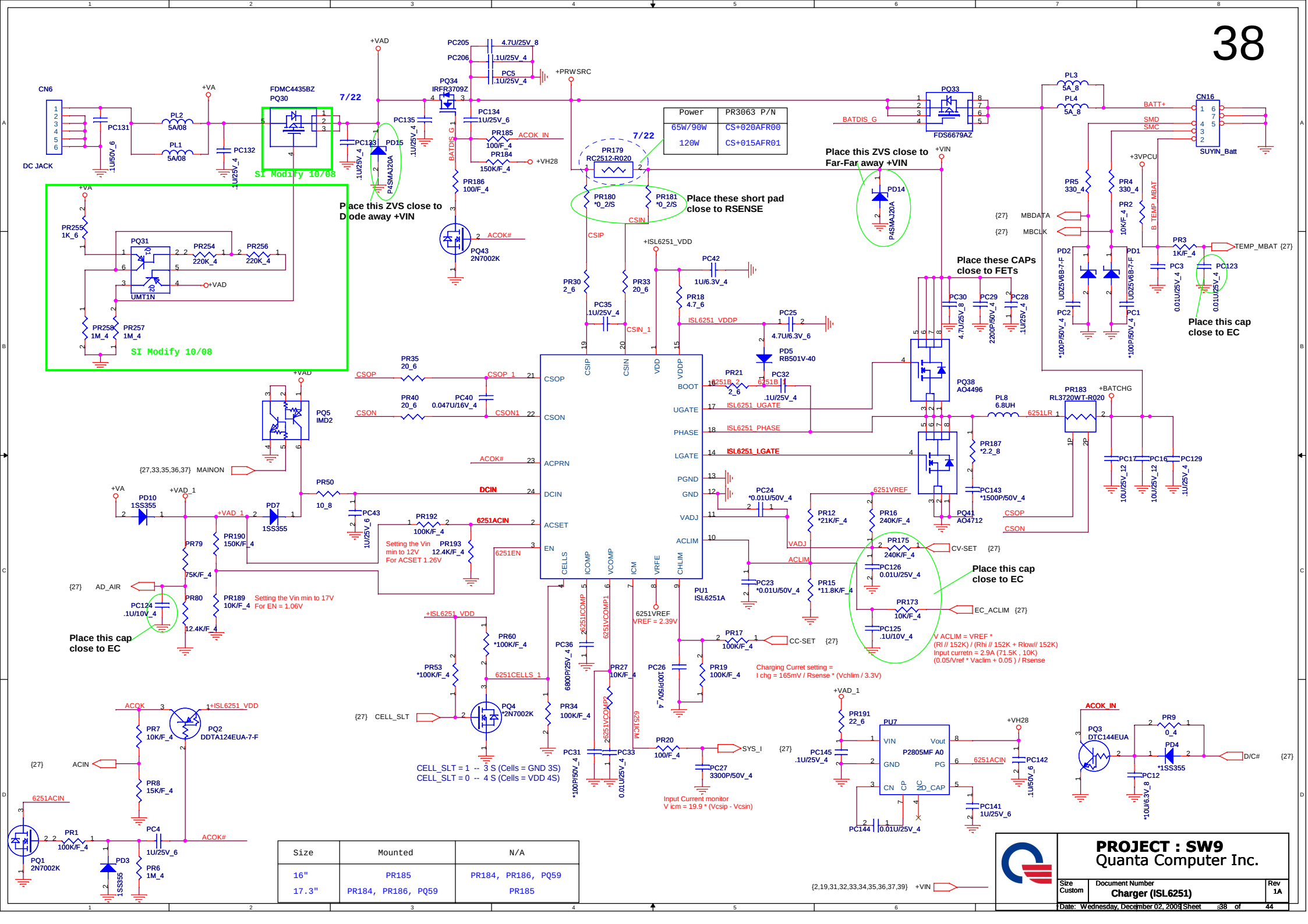
Date: Wednesday, December 02, 2009 Sheet 36 of 44



PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE/3VS5/5VS5/LAN	1A

Date: Wednesday, December 02, 2009 Sheet 37 of 44



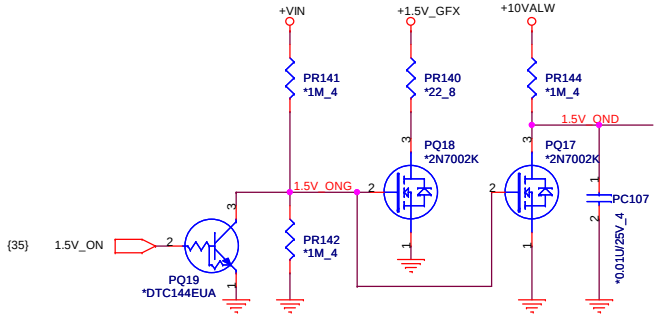
Size	Mounted	N/A
16"	PR185	PR184, PR186, PQ59
17.3"	PR184, PR186, PQ59	PR185

PROJECT : SW9
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (ISL6251)	1A

Date: Wednesday, December 02, 2009 Sheet 38 of 44

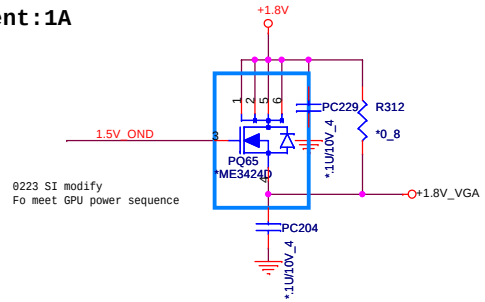
For Discrete or switchable Only

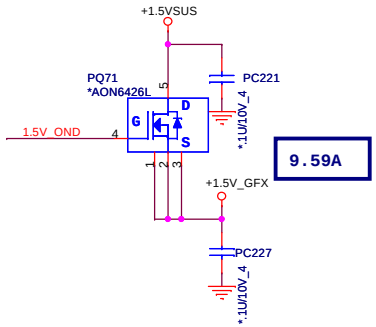


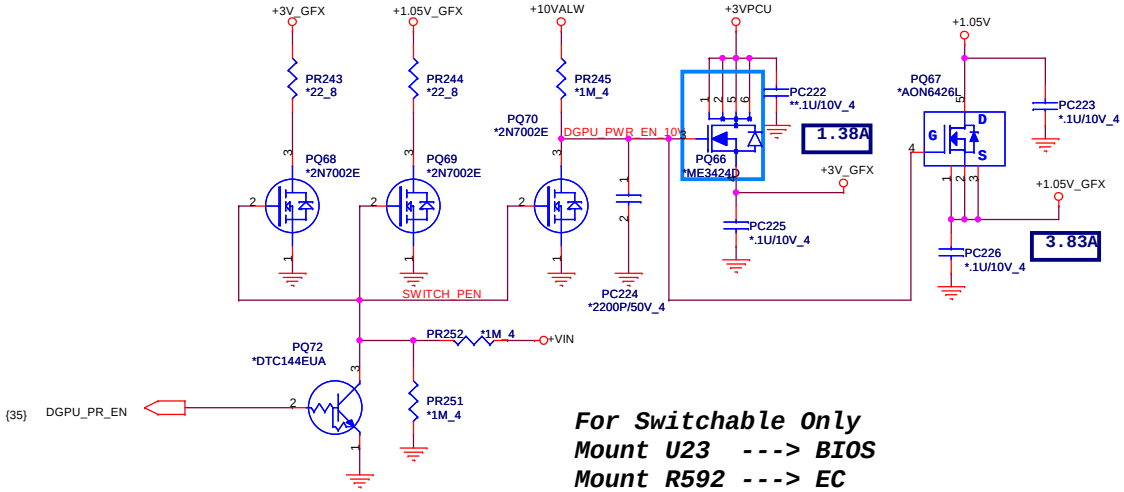
Change PC119 to 0.01u/25v as Discrete power sequence

For Discrete or switchable Only

+1.8 Volt +/- 0.1V
Countinue current:0.3A
Peak current:1A



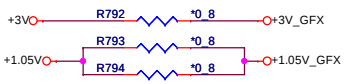




For Switchable Only
Mount U23 ---> BIOS
Mount R592 ---> EC

R51 co-lay PQ71
R53/R54 co-lay PQ68

For Discrete Only



For Hybrid DGPU Power Rails Sequence
1. +3V_GFX, +1.05V_GFX
2. +VGA_CORE -> DGPU_PG
3. 1.5V_GFX, +1.8V_GFX

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A3	Switchable Power	1A

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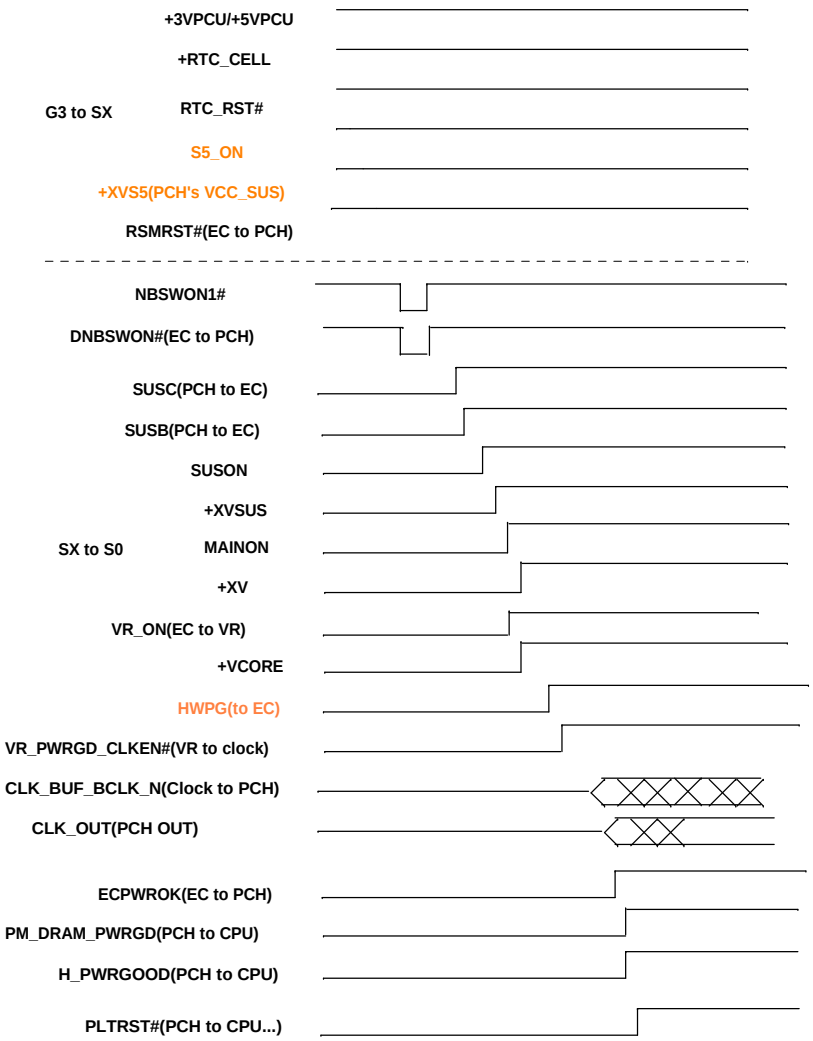
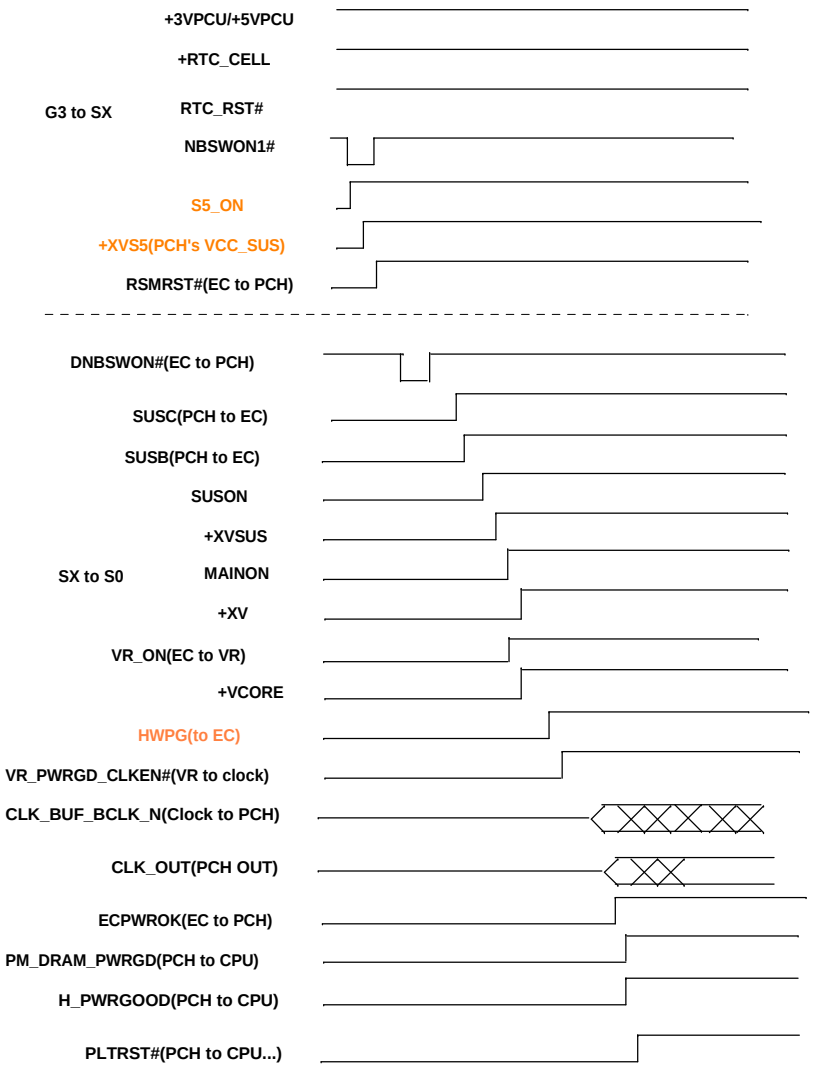
Power up sequence

LAN/RTC WAKE UP ENABLE.



LAN/RTC WAKE UP DISABLE.



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Size	Document Number	Rev
Custom	Power up sequence	1A

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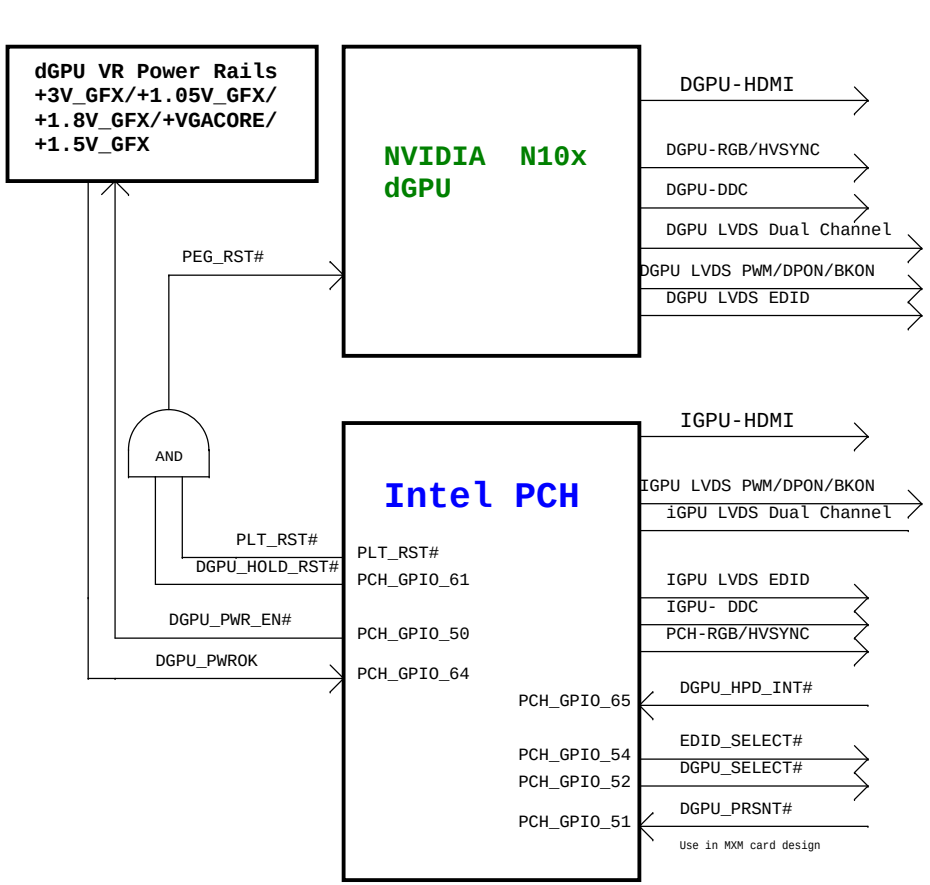
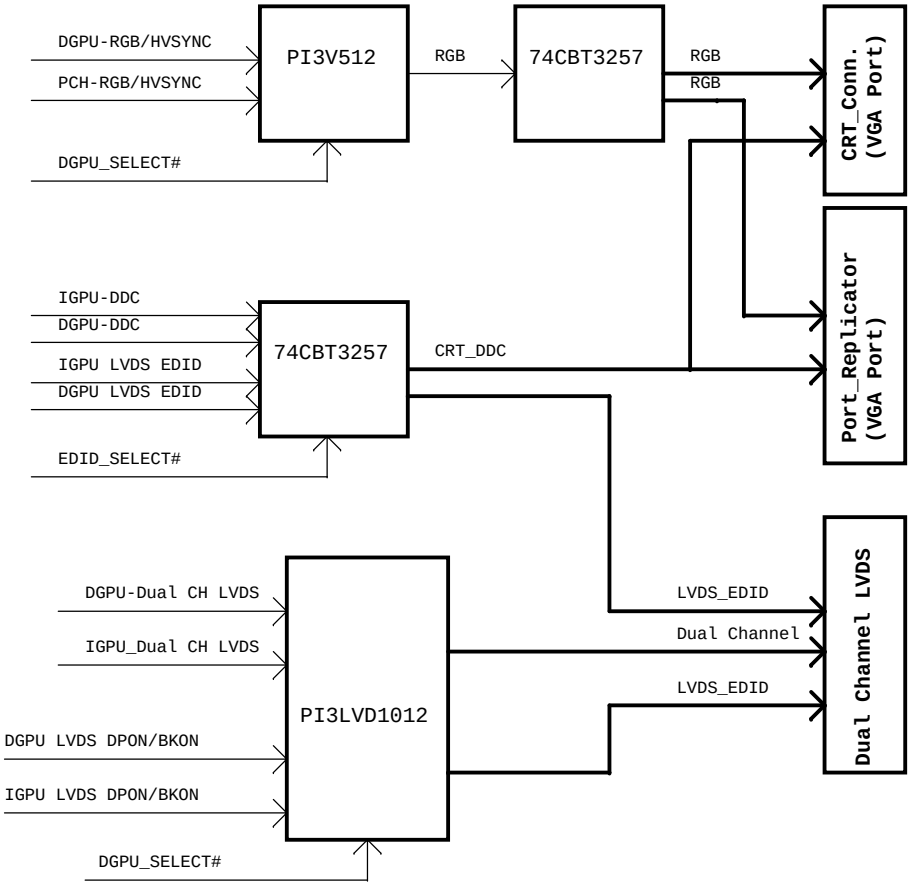
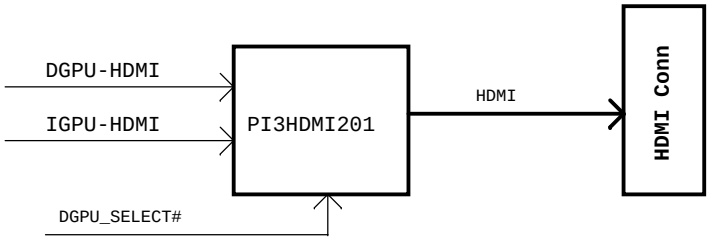




Switchable GPIOs	Descriptions
PCH_GPIO52	DGPU_SELECT#
PCH_GPIO61	DGPU_HOLD_RST#
PCH_GPIO50	DGPU_PWR_EN#
PCH_GPIO64	DGPU_PWR_OK
PCH_GPIO54	EDID_ELECT#
PCH_GPIO51	DGPU_PRSNT#
PCH_GPIO53	PWM_SELECT#



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Size	Document Number	Rev
Custom	Switch Blockdiagram	1A

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