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# Suzhou\_L

CPU : Intel Penryn  
 Chip Set : Intel Cantiga & ICH9M  
 Remarks : Montevina Platform

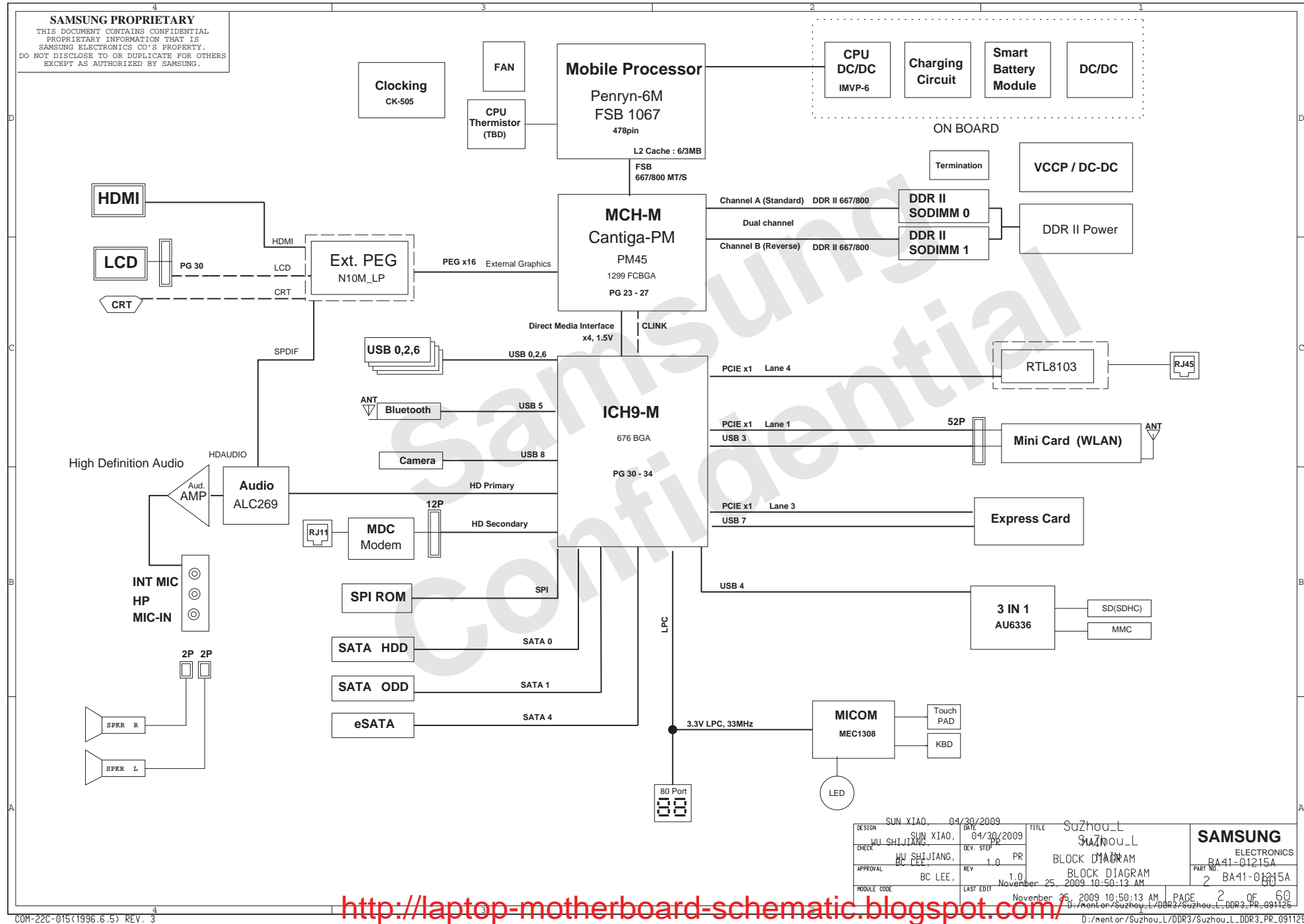
Model Name : Suzhou\_L\_DDR3  
 PCB Code : GCE BA41-01215A  
 NY BA41-01217A  
 HAN BA41-01216A

Dev. Step : P R  
 Revision : 1.0  
 T.R. Date : 2009.08.16

DESIGN	CHECK	APPROVAL

DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0	COVER		PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	1	OF 60

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DESIGN	SUN XIAO,	DATE	04/30/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PC	SHAZHOU_L	PART NO.	
APPROVAL	WU SHIJIANG, BC LEE,	REV	1.0	PR	BLOCK DIAGRAM	BA41-01215A
MODULE CODE	BC LEE,	LAST EDIT	November 25, 2009 10:50:13 AM	1.0	BLOCK DIAGRAM	PAGE 2 OF 60
D:/mentor/Suzhou_L/DDR3/Suzhou_L.DDR3.PR_091125						

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# BOARD INFORMATION

## SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

### PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	A,B,C
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

### Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH9-M	Real Time Clock
Crystal	10MHz	MICOM	HD4F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	25MHz	LAN	RealTek 88E8057

### LCD Pannel Detect (TBD)

Devices	Resolution	PANNEL_DETECT_0

### Voltage Rails

VDC	Primary DC system power supply (9 to 20V)
VCC_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH9-M
P3.3V_MICOM	3.3V always power rail (for Micom)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR (off in S4-S5)
P0.9V	0.9V power rail for DDR (off in S3-S5)
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail (off in S4-S5)
P5.0V	5.0V switched power rail (off in S3-S5)
P5.0V_AUX	5.0V switched on power rail (off in S4-S5)
P5.0V_ALW	5.0V always power rail

### I<sup>2</sup>C / SMB Address

Devices	Address	Hex	Bus
ICH9-M	Master	-	SMBUS Master
CPU Thermal Sensor	0111 101x	7Ah	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

### USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	SYSTEM PORT 2
3	NC
4	NC
5	Bluetooth
6	Mini PCI Express 2
7	Camera
8	NC
9	NC

### PCI Express Assign

PORT #	ASSIGNED TO
0	NC
1	Mini Card 1 (WLAN)
2	NC
3	LOM
4	Mini Card 2 (ROBSON or DVB-T)
5	NC

(This table will be update.)

## REVISION HISTORY

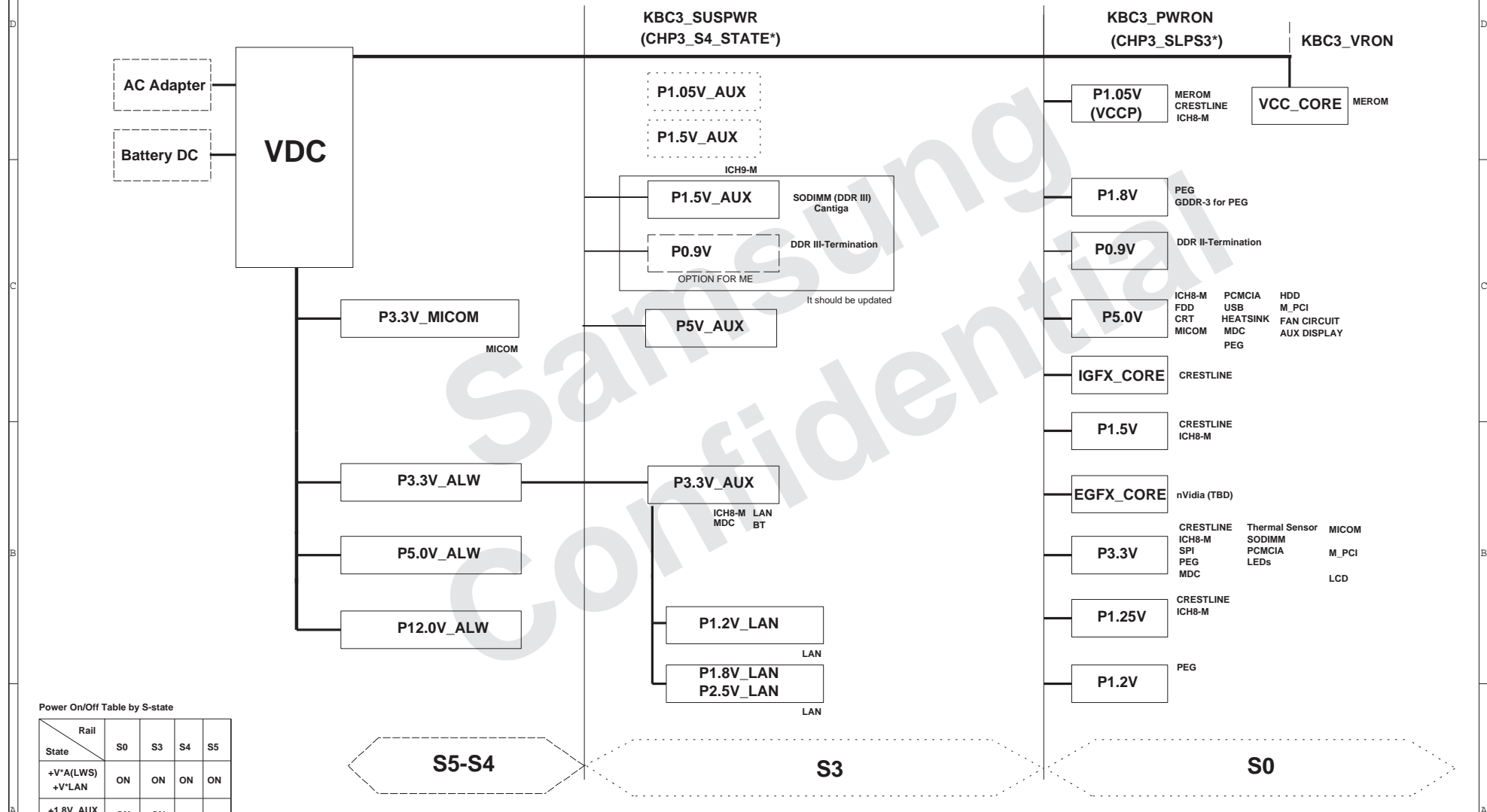
See rev notes for more information.

DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	BCAFDINFO	PART NO.	BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM		PAGE	3 OF 60

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# POWER DIAGRAM Rev 0.1



Power On/Off Table by S-state

Rail	S0	S3	S4	S5
+V*(LWS) +V*LAN	ON	ON	ON	ON
+1.8V_AUX +0.9V	ON	ON	---	---
+V*AUX	ON	ON	---	---
+V	ON	---	---	---
+V* (CORE)	ON	---	---	---

S5-S4

S3

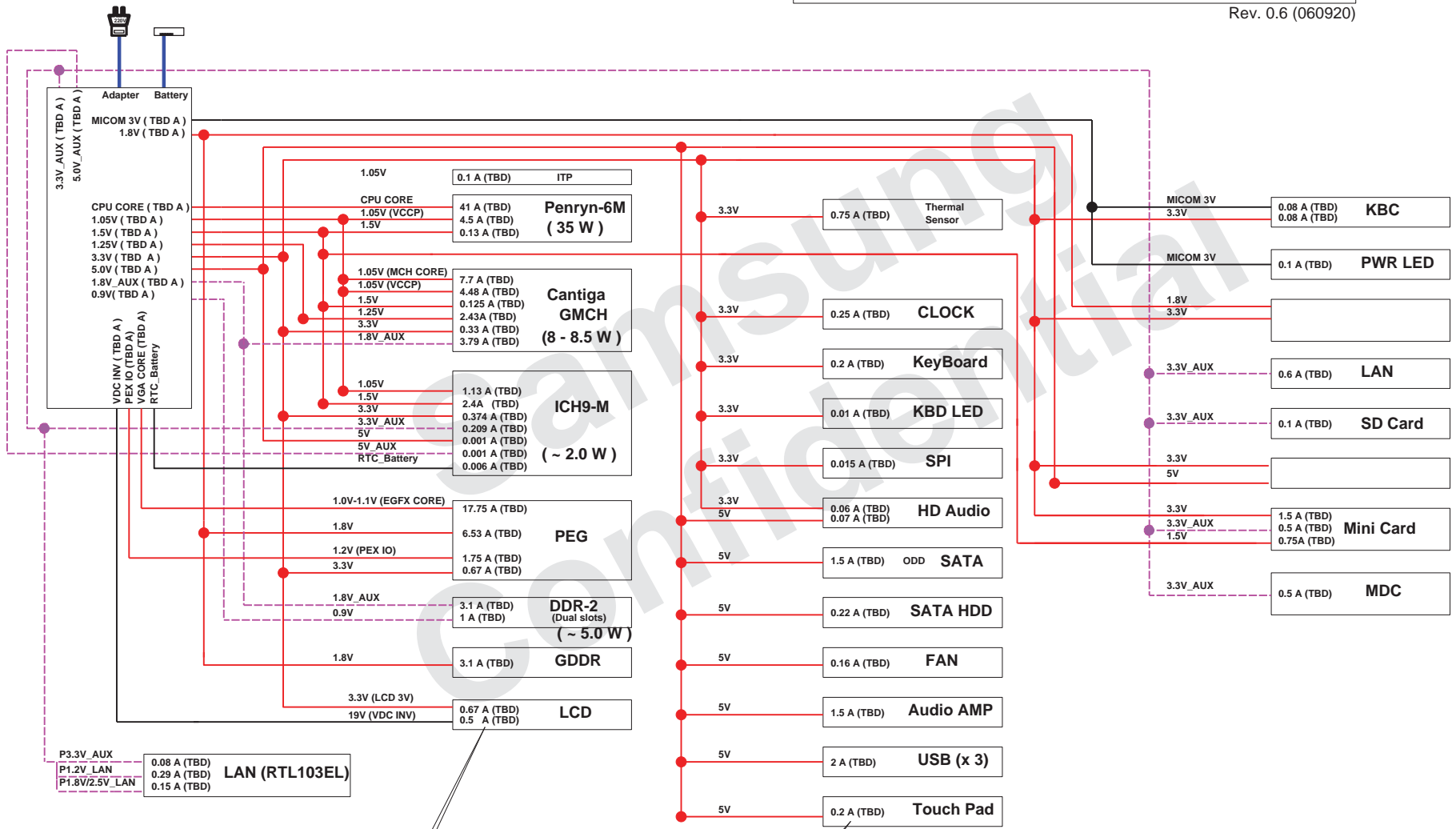
S0

DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	POWER DIAGRAM	PART NO.	BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	4	OF 60

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# POWER RAILS ANALYSIS

Rev. 0.6 (060920)



Value by Datasheet/Application notes (Value by measurement)

DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	Suzhou_L MAIN POWER RAILS	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			PAGE 5 OF 60

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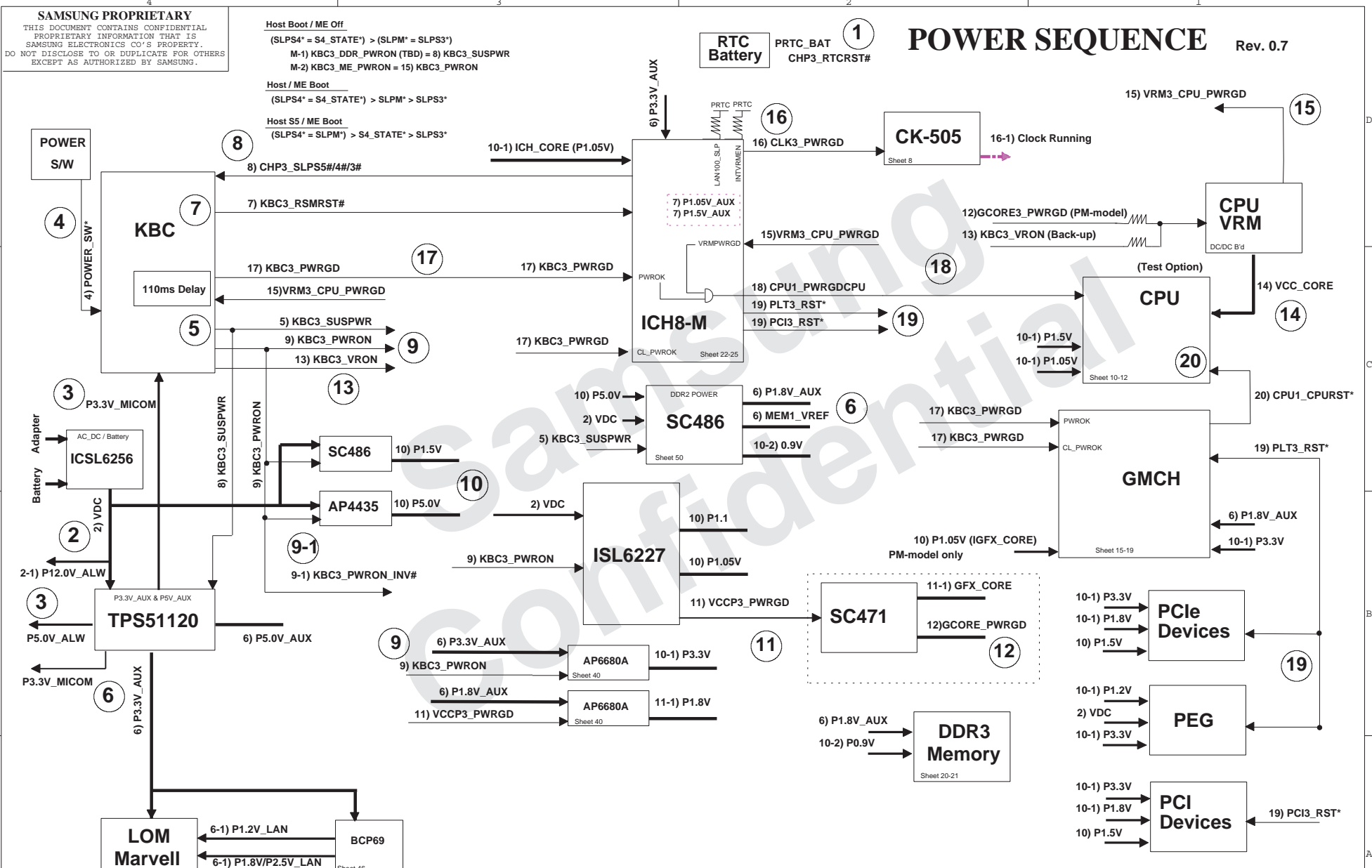
**Host Boot / ME Off**  
 (SLPS4\* = S4\_STATE\*) > (SLPM\* = SLPS3\*)  
 M-1) KBC3\_DDR\_PWRON (TBD) = 8) KBC3\_SUSPWR  
 M-2) KBC3\_ME\_PWRON = 15) KBC3\_PWRON

**Host / ME Boot**  
 (SLPS4\* = S4\_STATE\*) > SLPM\* > SLPS3\*

**Host S5 / ME Boot**  
 (SLPS4\* = SLPM\*) > S4\_STATE\* > SLPS3\*

# POWER SEQUENCE

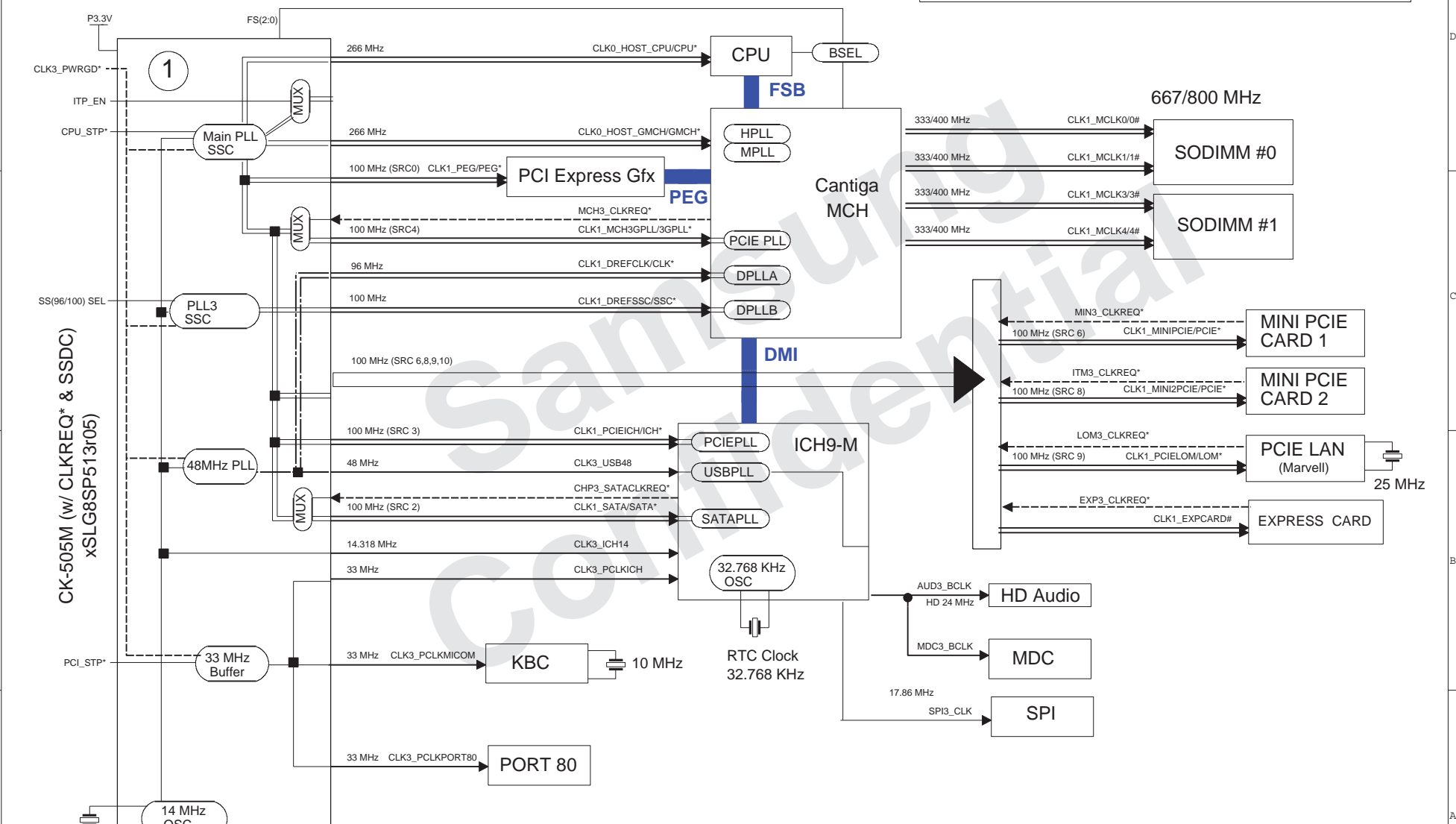
Rev. 0.7



DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	Suzhou_L MAIN POWER SEQUENCE	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01215A
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	6 OF 60	

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# CLOCK DISTRIBUTION Rev. 0.1



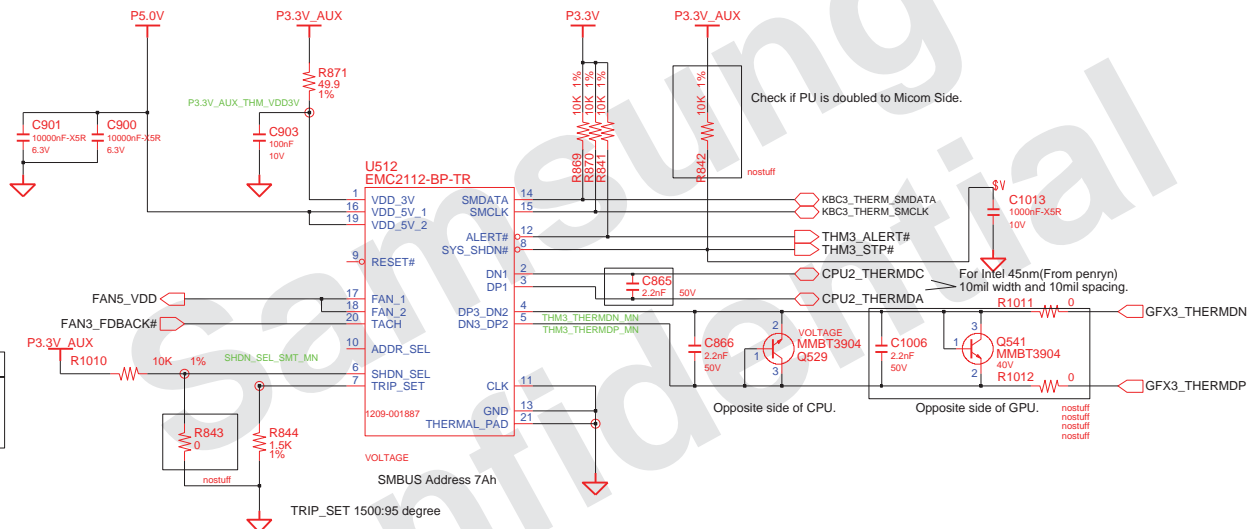
CK-505M (w/ CLKREQ\* & SSDC)  
 xSLG8SP513r05  
 Page 8

DESIGN	SUN XIAO,	DATE	8/16/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	CLOCK DIAGRAM	PART NO.	BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	7	OF 60

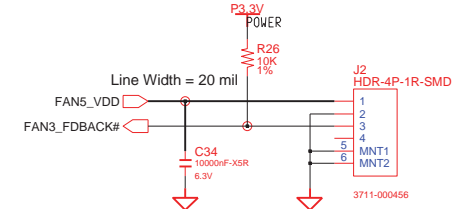
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# THERMAL SENSOR & FAN CONTROL



SHDN_SEL MODE	
0	CH1(INTEL MODE)
HIGH Z	CH3(DIODE MODE)
1	N/A (SHDN# NOT USED)

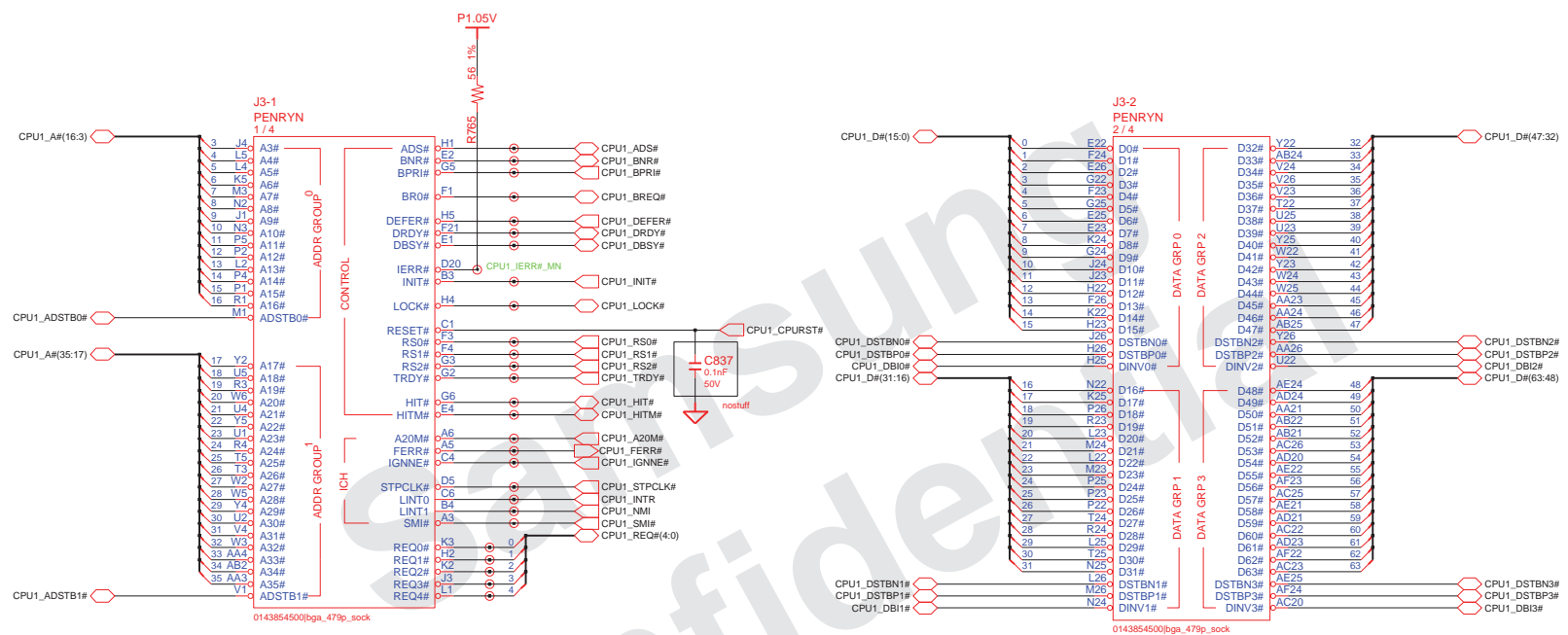


DESIGN	SUN XIAO,	DATE	6/17/2008	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	Thermal Sensor EMC2102	PART NO.	
APPROVAL	BC LEE,	REV	1.0			BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	8	OF 60

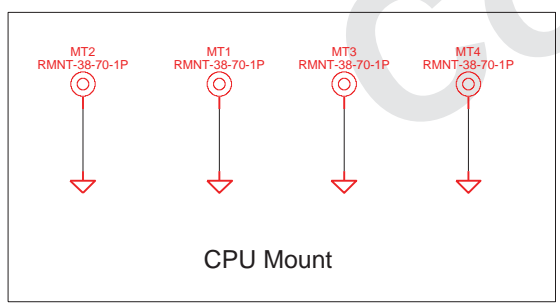
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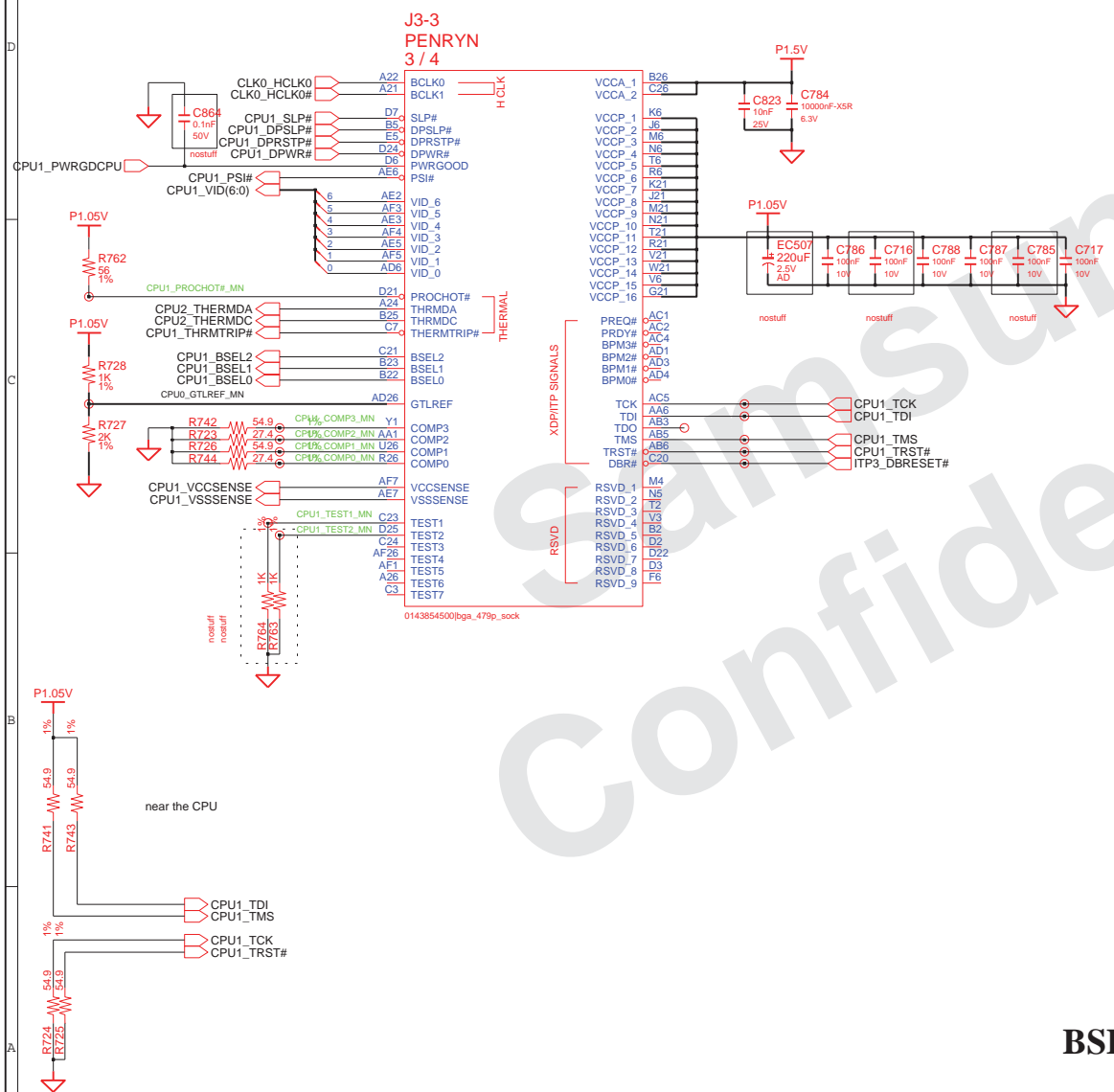
CPU Socket: 3704-001153



DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	Suzhou_L CPU	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	PENRYN (1/3)		
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01215A
MODULE CODE	undef ined	LAST EDIT	November 25, 2009 10:50:13 AM	PAGE 9 OF 60		

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**CPU Core Voltage Table** IMVP-6

Active Mode		Active/Deeper Sleep Dual Mode Region		Deeper Sleep/Extended Deeper Sleep Dual Mode Region	
VID(6:0)	Voltage	VID(6:0)	Voltage	VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 1 0 0 0	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 1	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 1 0	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 1	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 1 0 0	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 1	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 1 0	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 1	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 1 1 0 0 0	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 1	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 1 0	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 1	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 1 0 0	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 1	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 1 0	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 1	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 0 1 1 1	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 0 1 1 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 0 1 1 1	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 0 1 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 0 1 1 1	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 0 1 1 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 0 1 1 1	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 0 1 1 1	0.5125 V	1 1 1 1 0 0 0	0.0000 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 0 1 1 1	0.5000 V	1 1 1 1 0 0 1	0.0000 V
		1 1 1 1 0 1 0	0.0000 V	1 1 1 1 0 1 1	0.0000 V
		1 1 1 1 1 0 0	0.0000 V	1 1 1 1 1 0 1	0.0000 V
		1 1 1 1 1 0 1	0.0000 V	1 1 1 1 1 1 0	0.0000 V
		1 1 1 1 1 1 0	0.0000 V	1 1 1 1 1 1 1	0.0000 V
		1 1 1 1 1 1 1	0.0000 V		

\*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

GND test points within 100mil of the VCC/VSSense at the end of the line. Route the VCC/VSSense as a Zo=55ohm traces with equal length. Observe 3:1 spacing b/w VCC/VSSense lines and 25mil away (preferred 50mil) from any other signal. And GND via 100mil away from each of the VCC/VSS test point vias.

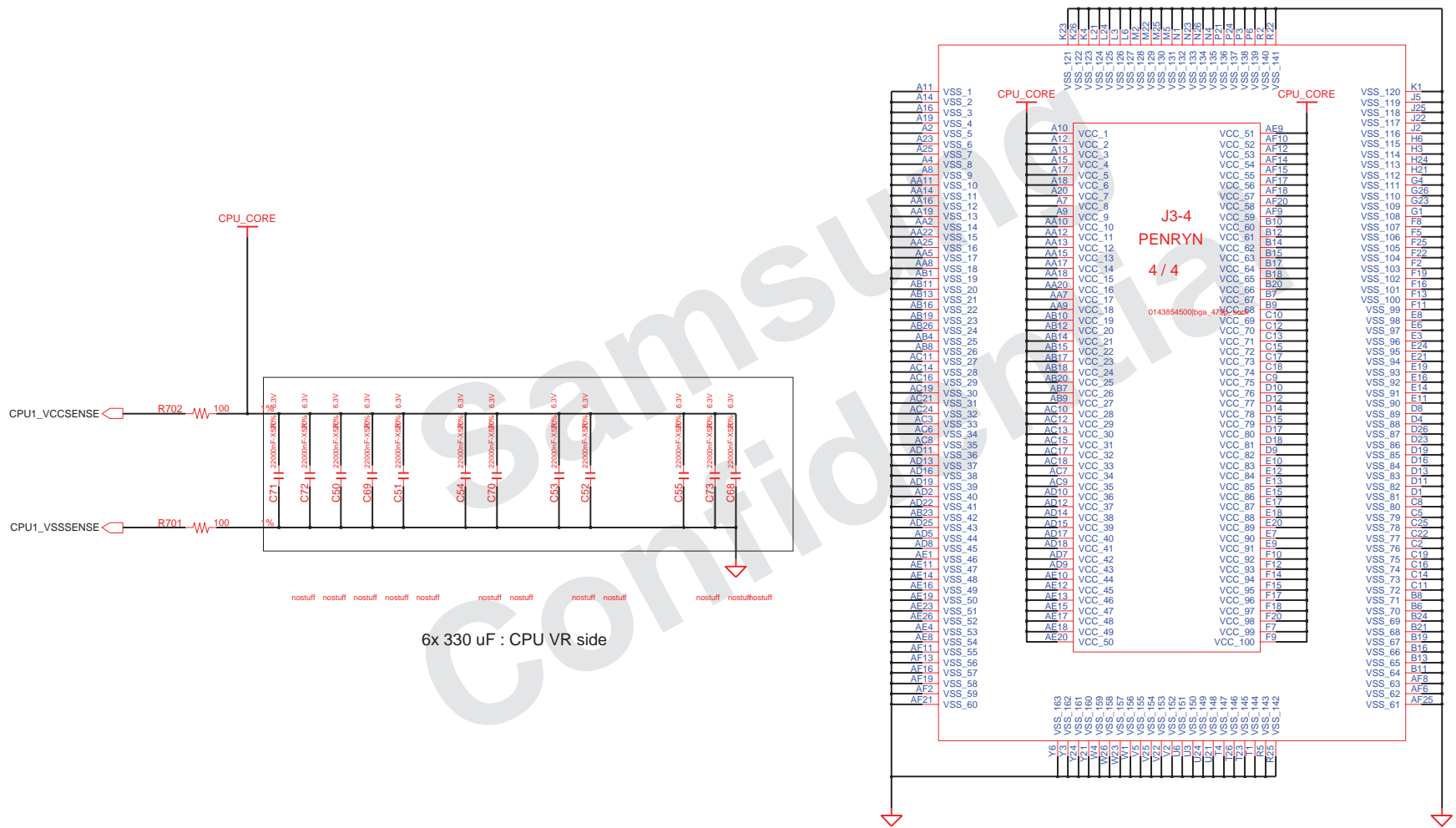
**BSEL**

FSB 1067 MHz		Pull-down
FSB 800 MHz		BSEL0, BSEL1, BSEL2
		BSEL0, BSEL2

DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	SuZhou_L	SAMSUNG ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		CPU	
APPROVAL	BC LEE,	REV	1.0		PENRYN (2/3)	PART NO. BA41-01215A
MODULE CODE	undefined	LAST EDIT	November 25, 2009 10:50:13 AM			PAGE 10 OF 60

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6x 330 uF : CPU VR side

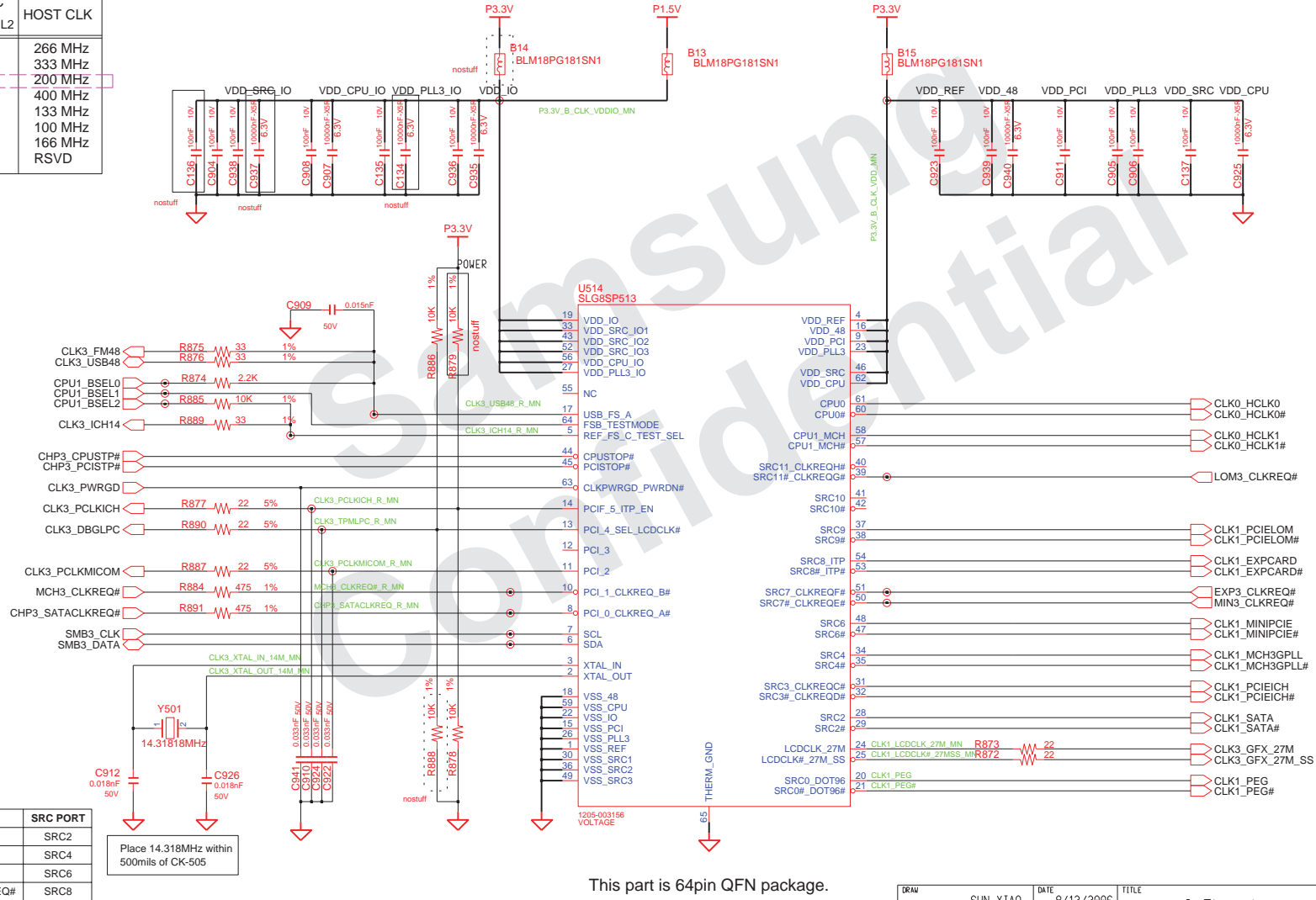
DRAW SUN XIAO, CHECK WU SHIJIANG, APPROVAL BC LEE, MODULE CODE undef ined	DATE 11/8/2006 DEV. STEP PR REV 1.0 LAST EDIT November 25, 2009 10:50:13 AM	TITLE Suzhou_L CPU PENRYN (3/3)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01215A
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# CK505M

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FSA	FSB	FSC	HOST CLK
BSEL0	BSEL1	BSEL2	
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD



This part is 64pin QFN package.

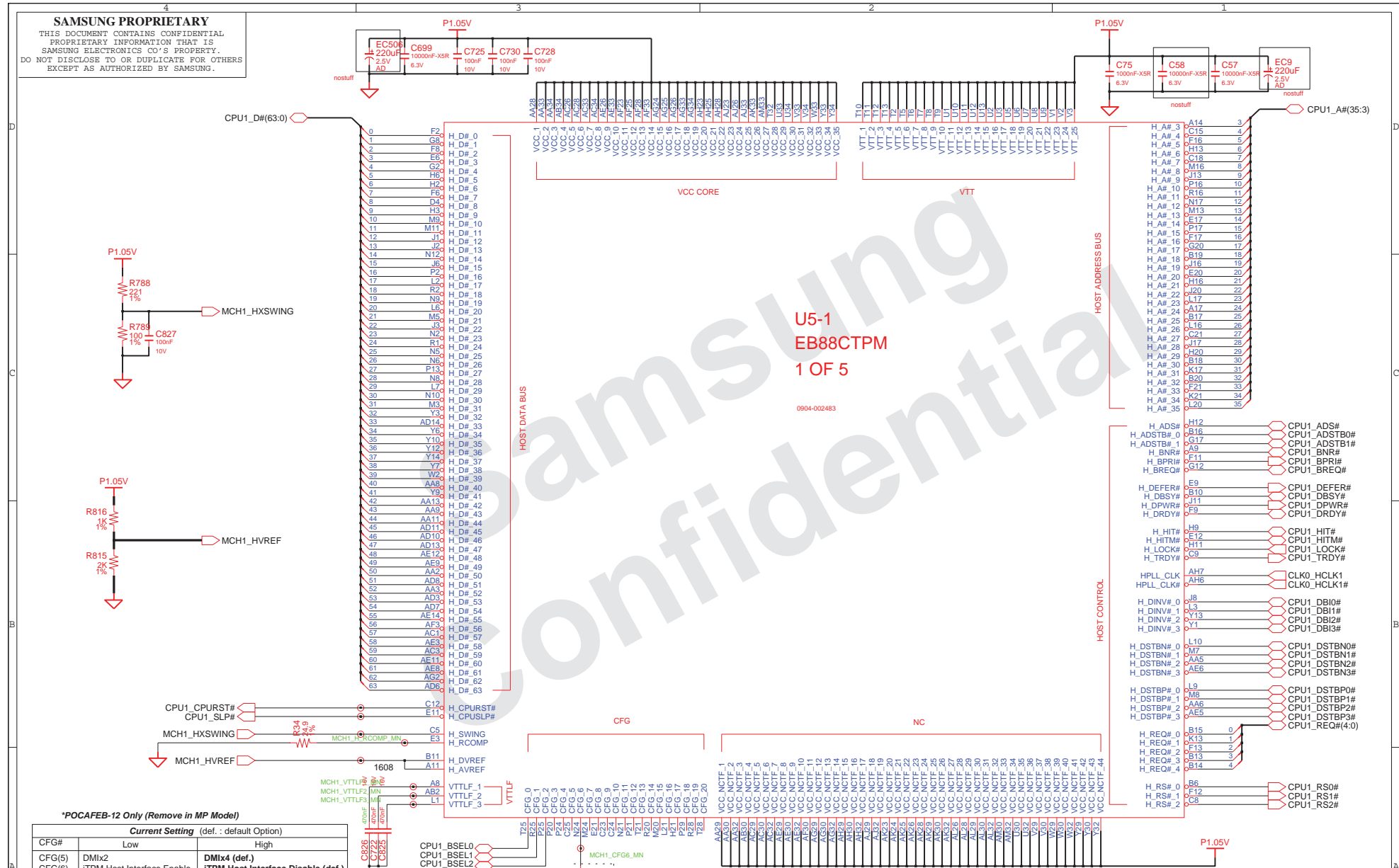
IDT: 1205-003159  
 SL: 1205-003533

CLK REQ	DEVICE	SRC PORT
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXP3_CLKREQ#	SRC8

SEL_LCDDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	PEG_CLK/PEG_CLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

DRAW	SUN XIAO,	DATE	8/12/2006	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	Main_Clock_Circuit		
APPROVAL	BC LEE,	REV	1.0	CK_Clock_505M		PART NO. BA41-01215A
MODULE CODE	undefined	LAST EDIT	November 25, 2009 10:50:13 AM			PAGE 12 OF 60

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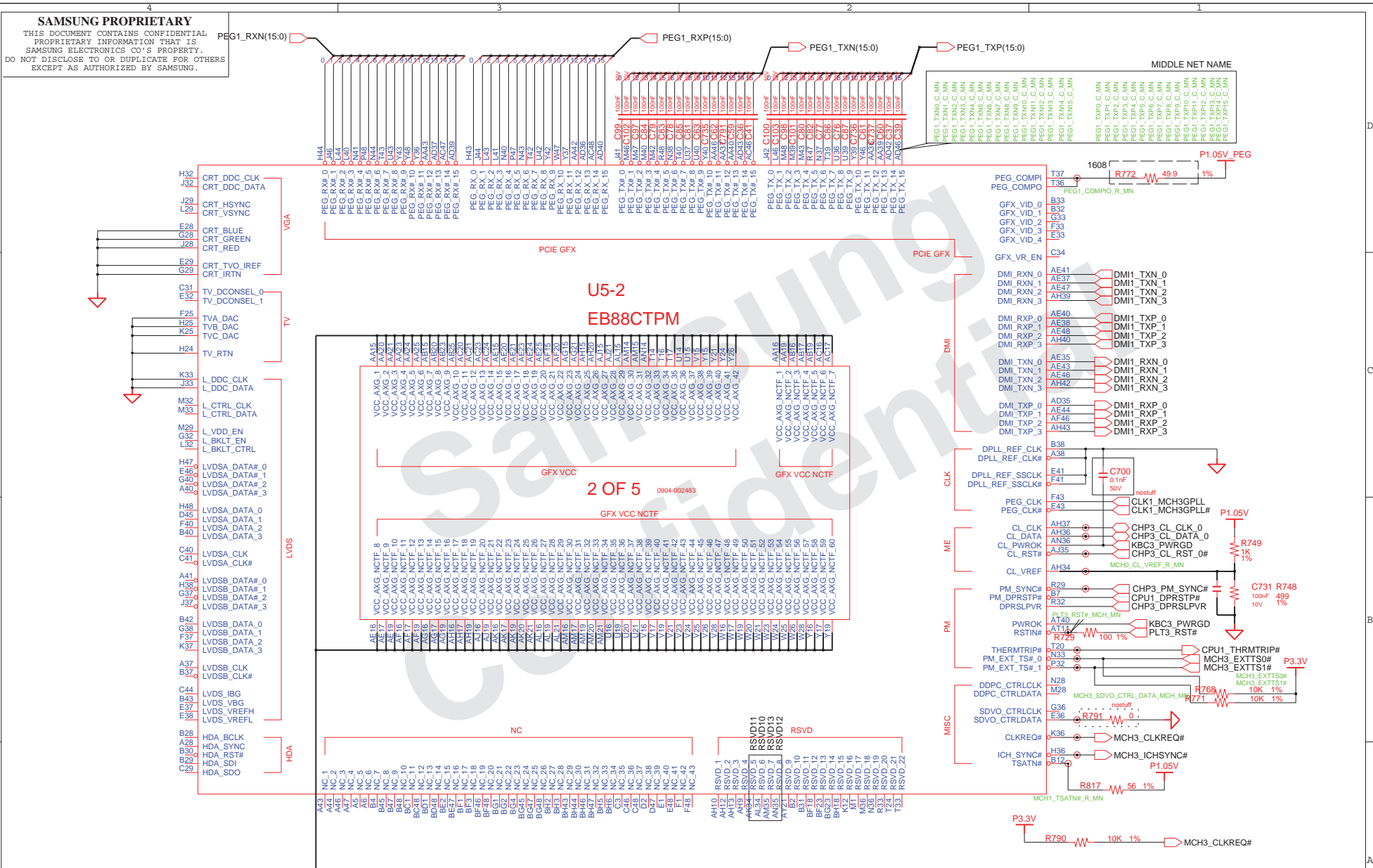


**\*POCAFEB-12 Only (Remove in MP Model)**

CFG#	Low	High
CFG(5)	DMix2	DMix4 (def.)
CFG(6)	iTPM Host Interface Enable	iTPM Host Interface Disable (def.)
CFG(7)	ME Crypto no confidentiality	ME Crypto confidentiality (def.)
CFG(9)	PEG Reversal (def.)	Normal
CFG(10)	PCIe Loop Back Enable	PCIe Loop Back Disable(def)
CFG(16)	Dynamic ODT Disabled	Dynamic ODT Enabled (def.)
CFG(19)	DMI Lane Normal (def.)	DMI Lane Reversal
CFG(20)	SDVO or PCIe X1 Only(def.)	SDVO and PCIe X1 Simultaneously

DATE	SUN XIAO, 11/8/2006	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG, PR	DEV. STEP	MCH_CANTIGA_PM.DDR3	
APPROVAL	BC LEE, REV 1.0	REV	CANTIGA (1/5)	PART NO.
MODULE CODE	undef:ined	LAST EDIT	November 25, 2009 10:50:13 AM	BA41-01215A
			PAGE	13 OF 60

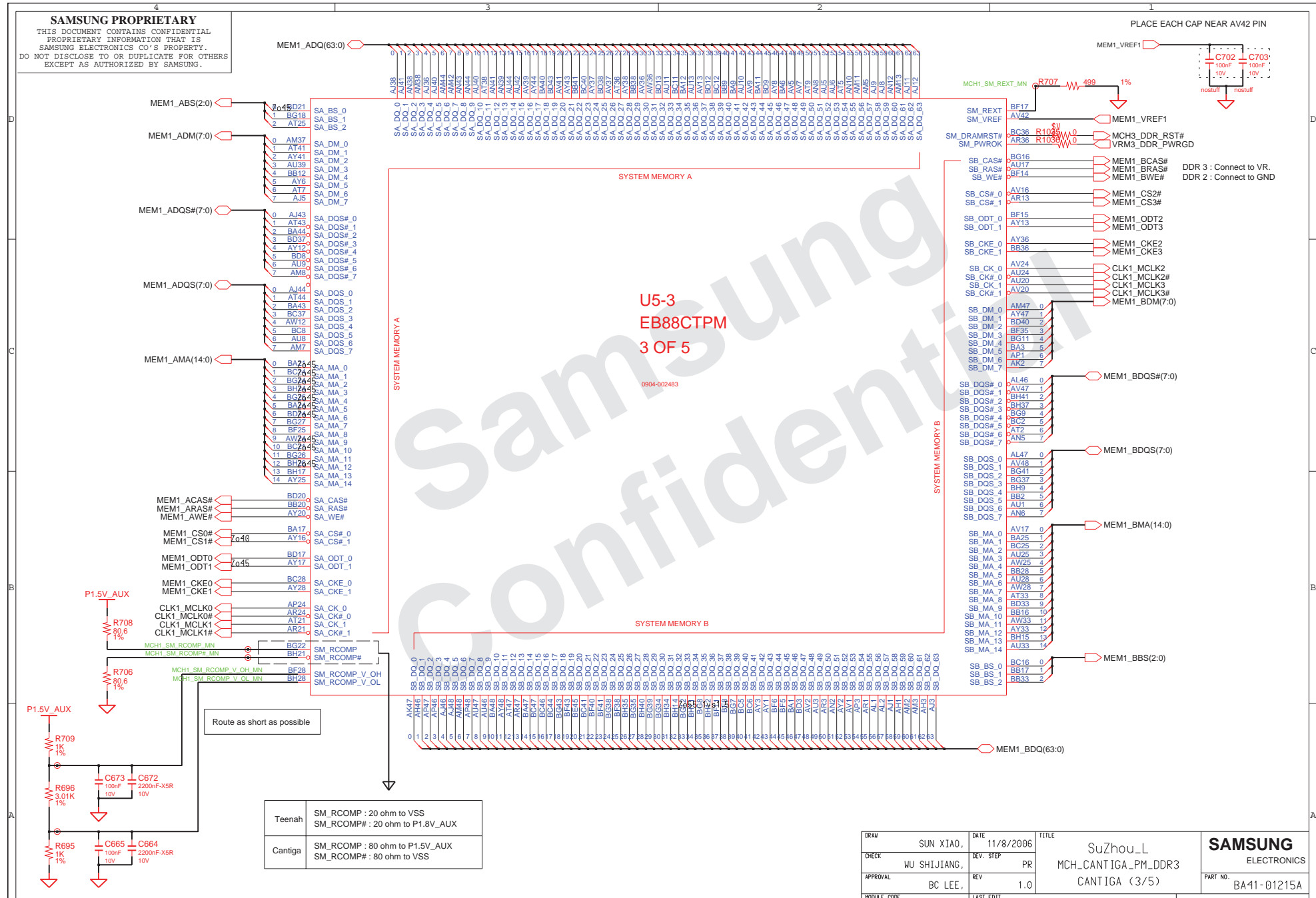
<http://laptop-motherboard-schematic.blogspot.com/>



DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MCH_CANTIGA_PM_DDR3	PART NO.	
APPROVAL	BC LEE,	REV	1.0	CANTIGA (2/5)	BA41-01215A	
MODULE CODE	undef ined	LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	14	OF 60

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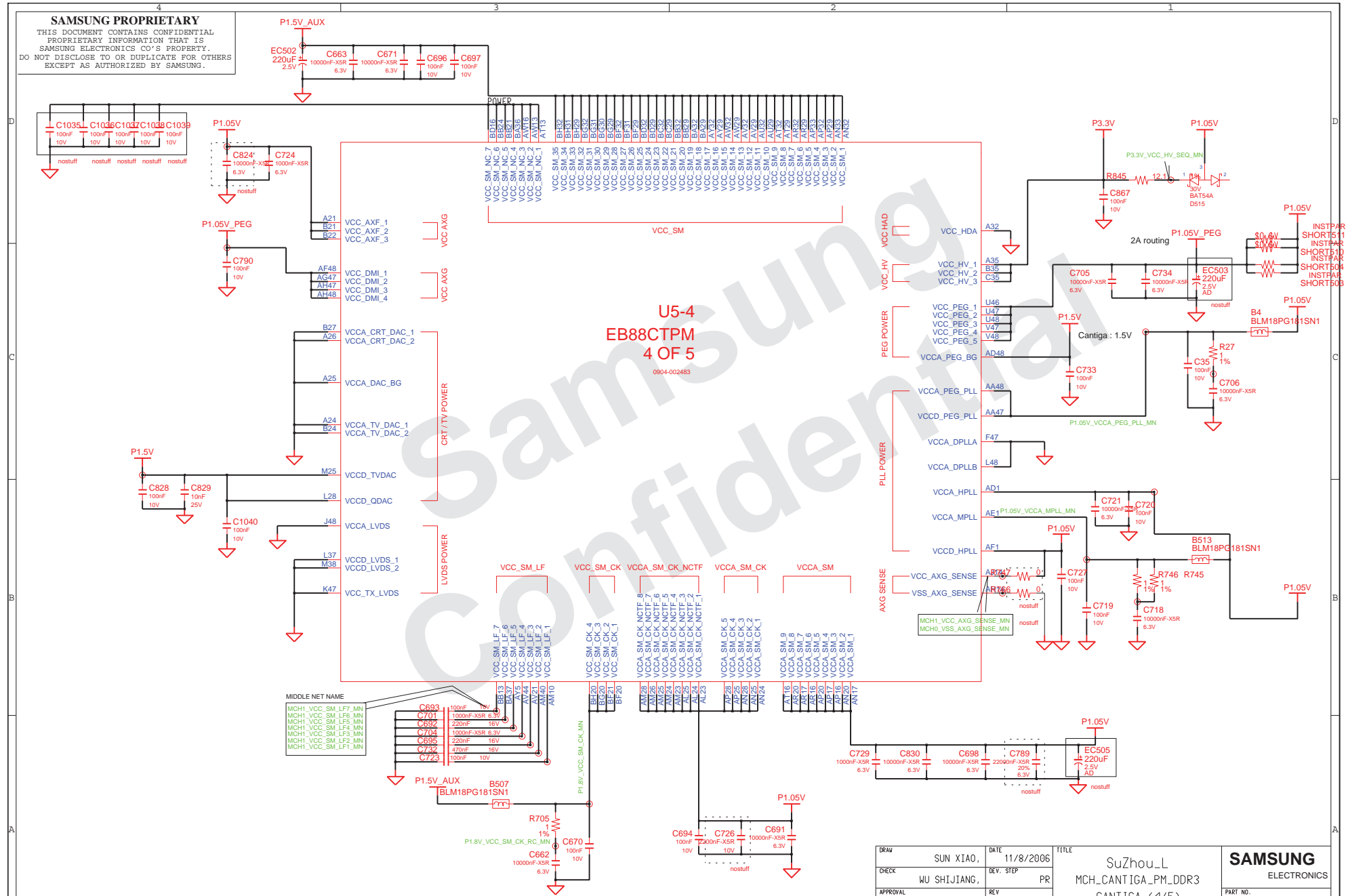
PLACE EACH CAP NEAR AV42 PIN



<http://laptop-motherboard-schematic.blogspot.com/>

DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MCH1_CANTIGA_PM_DDR3	CANTIGA (3/5)	
APPROVAL	BC LEE,	REV	1.0	MODULE CODE	LAST EDIT	PART NO. BA41-01215A
				November 25, 2009 10:50:13 AM	PAGE	15 OF 60

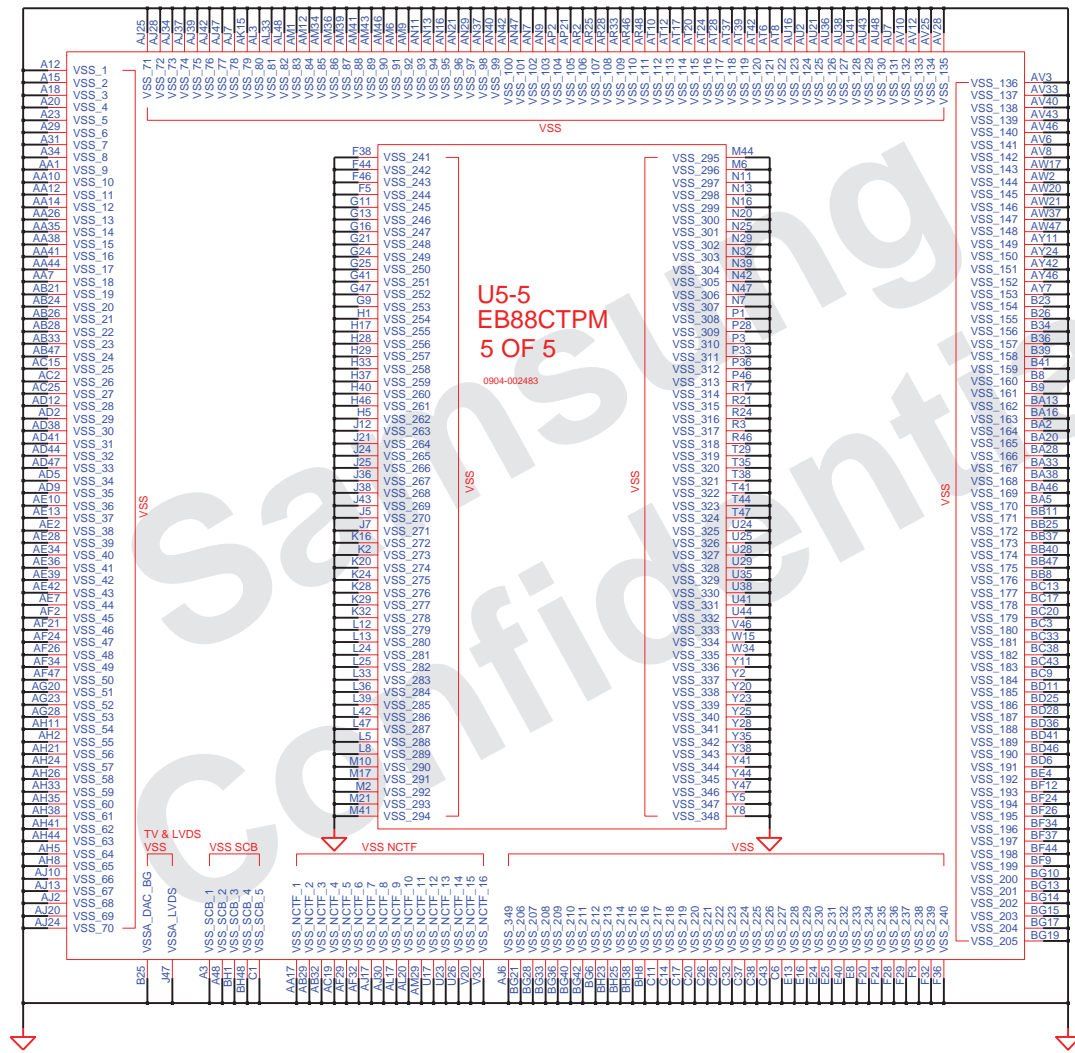
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CHECK	WU SHIJIANG,	DEV. STEP	PR	MCH_CANTIGA_PM_DDR3	PART NO.	
APPROVAL	BC LEE,	REV	1.0	CANTIGA (4/5)	BA41-01215A	
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	16	OF 60



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**U5-5  
 EB88CTPM  
 5 OF 5**

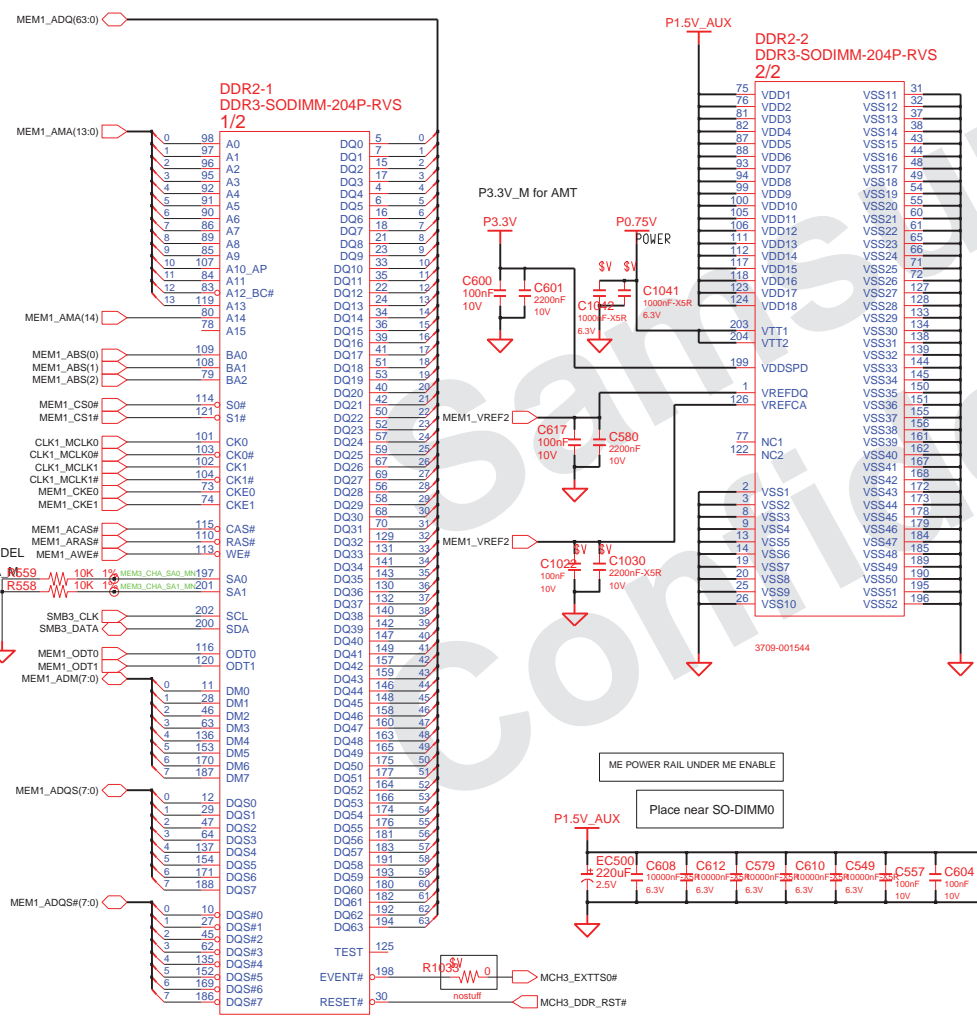
0904-002483

DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MCH_CANTIGA_PM_DDR3 CANTIGA (5/5)	PART NO.	
APPROVAL	BC LEE,	REV	1.0		BA41-01215A	
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	17	OF 60

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**DDR SO-DIMM #0**

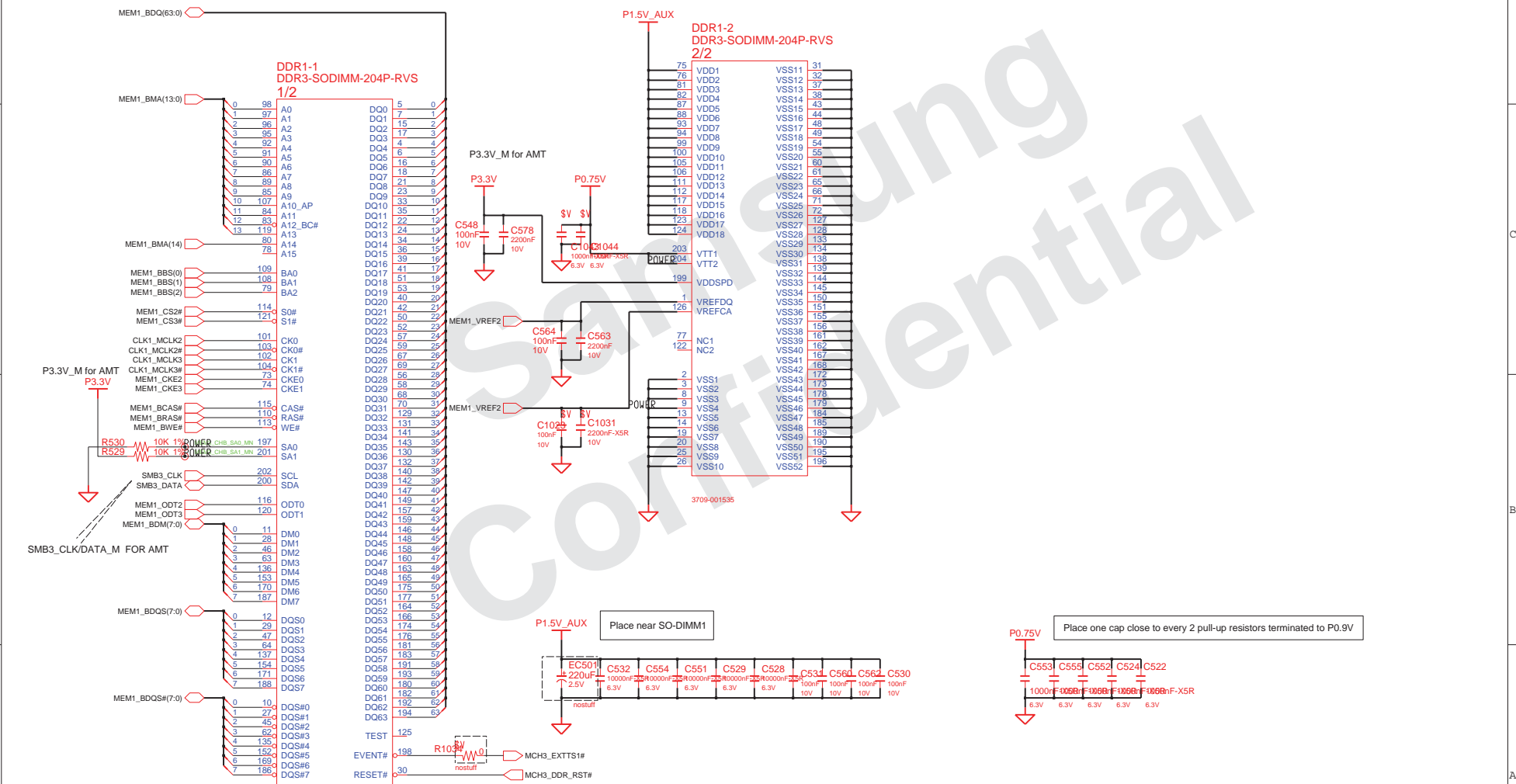


3709-001544

DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	SODIMM_REV	BA41-01215A	
APPROVAL	BC LEE,	REV	1.0	DDR3 CH A	PART NO.	BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	18	OF 60

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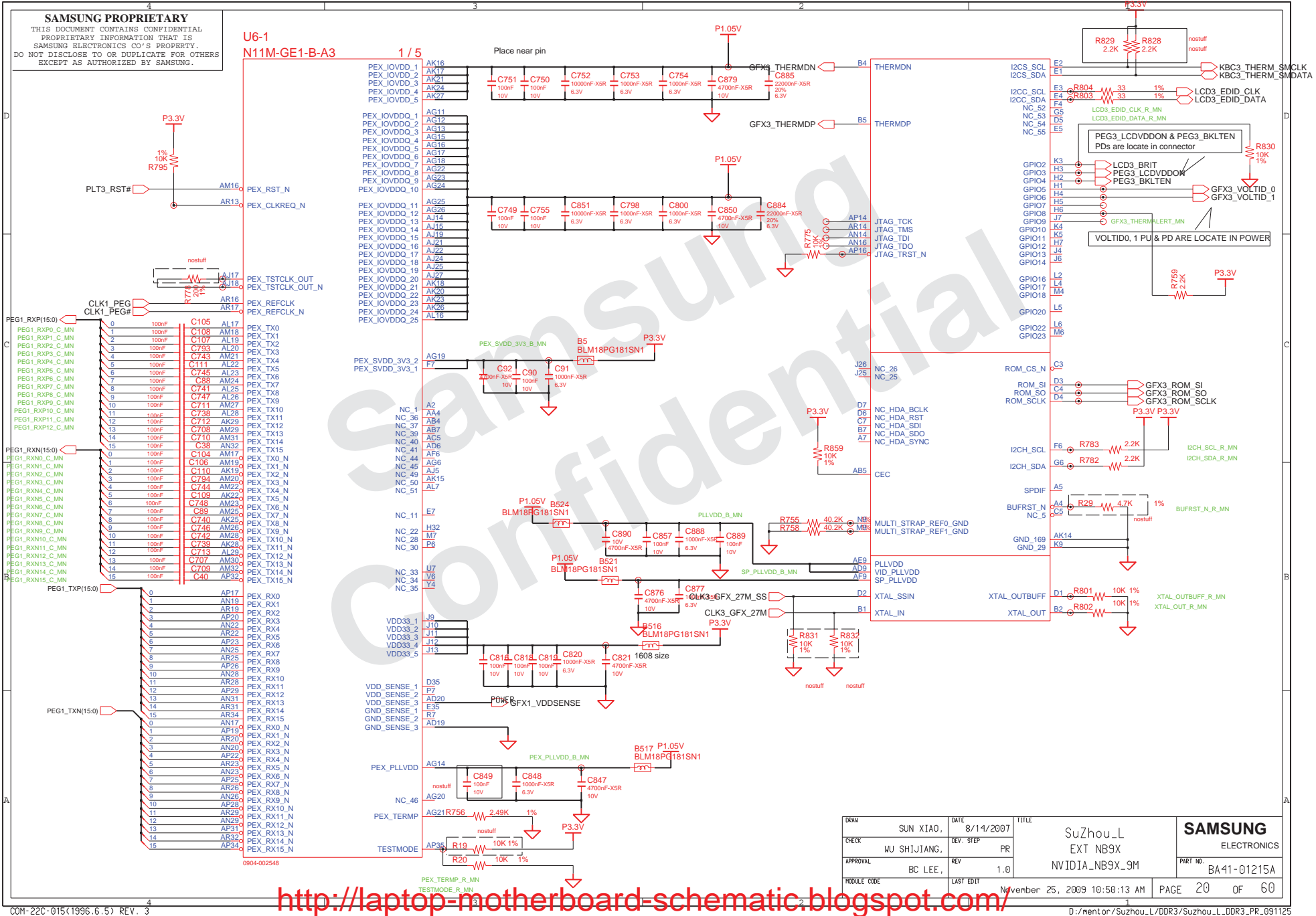
**DDR SO-DIMM #1**



DRAW	SUN XIAO,	DATE	11/8/2006	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	SODIMM_REV	BA41-01215A	
APPROVAL	BC LEE,	REV	1.0	DDR3 CH B	PAGE	19 OF 60
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			

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**U6-1**  
**N11M-GE1-B-A3**  
 1 / 5

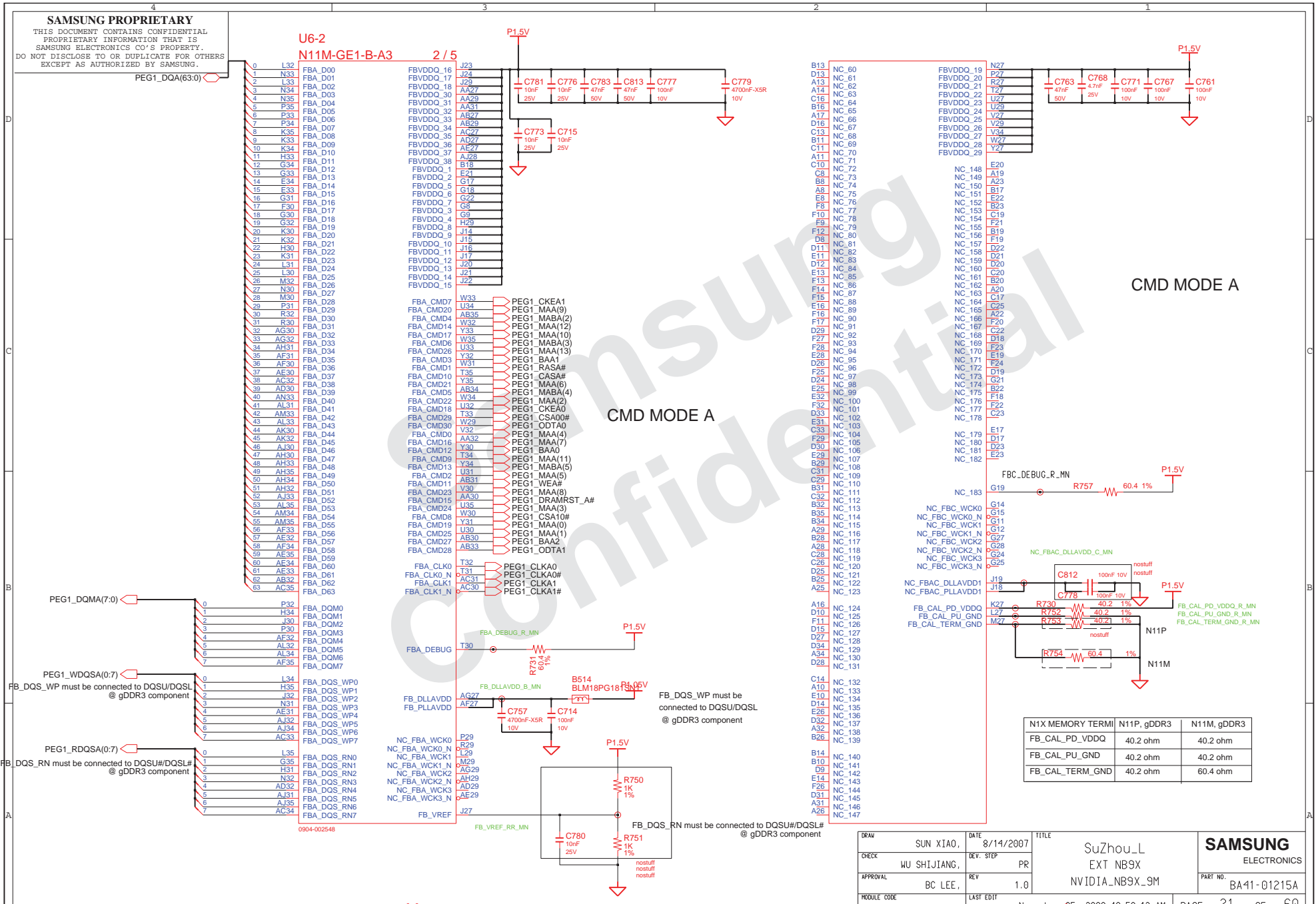


0904-002548

DRAW	SUN XIAO,	DATE	8/14/2007	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		EXT NB9X	
APPROVAL	BC LEE,	REV	1.0		NVIDIA_NB9X_9M	
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			
						PART NO. BA41-01215A
						PAGE 20 OF 60

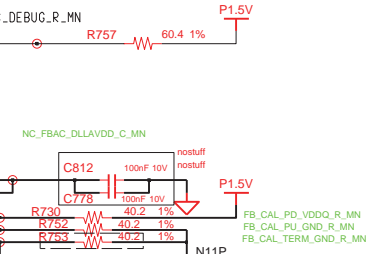
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CMD MODE A

CMD MODE A



N1X MEMORY TERM1	N11P, gDDR3	N11M, gDDR3
FB_CAL_PD_VDDQ	40.2 ohm	40.2 ohm
FB_CAL_PU_GND	40.2 ohm	40.2 ohm
FB_CAL_TERM_GND	40.2 ohm	60.4 ohm

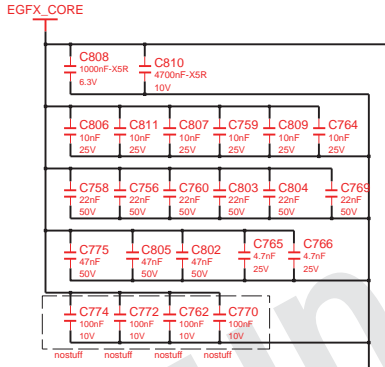
DRW	SUN XIAO,	DATE	8/14/2007	TITLE	SuZhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	REV. STEP	PR	EXT NB9X	PART NO.	
APPROVAL	BC LEE,	REV	1.0	NVIDIA_NB9X_9M	BA41-01215A	
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM		PAGE	21 OF 60

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**U6-3**  
**N11M-GE1-B-A3** 3 / 5

B3	GND_1	GND_97	V16
B6	GND_2	GND_98	V18
B9	GND_3	GND_99	V20
B12	GND_4	GND_100	V22
B15	GND_5	GND_101	V24
B21	GND_6	GND_102	Y11
B24	GND_7	GND_103	Y13
B27	GND_8	GND_104	Y15
B30	GND_9	GND_105	Y17
B33	GND_10	GND_106	Y19
L2	GND_11	GND_107	Y21
C34	GND_12	GND_108	Y23
E6	GND_13	GND_109	Y25
E9	GND_14	GND_110	AA2
E12	GND_15	GND_111	AA5
E18	GND_16	GND_112	AA11
E24	GND_17	GND_113	AA13
E27	GND_18	GND_114	AA12
E30	GND_19	GND_115	AA14
F2	GND_20	GND_116	AA15
F5	GND_21	GND_117	AA16
F8	GND_22	GND_118	AA16
F31	GND_23	GND_119	AA17
F34	GND_24	GND_120	AA18
J2	GND_25	GND_121	AA19
J6	GND_26	GND_122	AA20
J31	GND_27	GND_123	AA21
J34	GND_28	GND_124	AA23
L9	GND_30	GND_125	AA24
M2	GND_31	GND_126	AA25
M5	GND_32	GND_127	AA34
M11	GND_33	GND_128	AB12
M13	GND_34	GND_129	AB14
M15	GND_35	GND_130	AB16
M17	GND_36	GND_131	AB16
M19	GND_37	GND_132	AB18
M21	GND_38	GND_133	AB20
M23	GND_39	GND_134	AB22
M25	GND_40	GND_135	AB24
M31	GND_41	GND_136	AC9
M34	GND_42	GND_137	AD2
N11	GND_43	GND_138	AD5
N12	GND_44	GND_139	AD11
N13	GND_45	GND_140	AD13
N14	GND_46	GND_141	AD15
N15	GND_47	GND_142	AD17
N16	GND_48	GND_143	AD21
N17	GND_49	GND_144	AD23
N18	GND_50	GND_145	AD25
N19	GND_51	GND_146	AD34
N20	GND_52	GND_147	AE11
N21	GND_53	GND_148	AE12
N22	GND_54	GND_149	AE13
N23	GND_55	GND_150	AE14
N24	GND_56	GND_151	AE15
N25	GND_57	GND_152	AE16
P12	GND_58	GND_153	AE17
P14	GND_59	GND_154	AE18
P16	GND_60	GND_155	AE19
P18	GND_61	GND_156	AE20
P20	GND_62	GND_157	AE20
P22	GND_63	GND_158	AE21
P24	GND_64	GND_159	AE22
R5	GND_65	GND_160	AE23
R2	GND_66	GND_161	AE24
R31	GND_67	GND_162	AE25
R34	GND_68	GND_163	AG2
T11	GND_69	GND_164	AG31
T13	GND_70	GND_165	AG32
T15	GND_71	GND_166	AG34
T17	GND_72	GND_167	AK2
T19	GND_73	GND_168	AK5
T21	GND_74	GND_169	AK31
T23	GND_75	GND_170	AK34
T25	GND_76	GND_171	AL6
U11	GND_77	GND_172	AL9
U12	GND_78	GND_173	AL12
U13	GND_79	GND_174	AL15
U14	GND_80	GND_175	AL18
U15	GND_81	GND_176	AL18
U16	GND_82	GND_177	AL21
U17	GND_83	GND_178	AL24
U18	GND_84	GND_179	AL27
U19	GND_85	GND_180	AL30
U20	GND_86	GND_181	AN2
U21	GND_87	GND_182	AN34
U22	GND_88	GND_183	AP3
U23	GND_89	GND_184	AP6
U24	GND_90	GND_185	AP9
U25	GND_91	GND_186	AP12
V2	GND_92	GND_187	AP15
V5	GND_93	GND_188	AP18
V9	GND_94	GND_189	AP21
Y12	GND_95	GND_190	AP24
V14	GND_96	GND_191	AP27
		GND_192	AP30
		GND_193	AP33



L11	VDD_1	VDD_57	V19
L12	VDD_2	VDD_58	V21
L13	VDD_3	VDD_59	V23
L14	VDD_4	VDD_60	V25
L15	VDD_5	VDD_61	W11
L16	VDD_6	VDD_62	W12
L17	VDD_7	VDD_63	W13
L18	VDD_8	VDD_64	W14
L19	VDD_9	VDD_65	W15
L20	VDD_10	VDD_66	W16
L21	VDD_11	VDD_67	W17
L22	VDD_12	VDD_68	W18
L23	VDD_13	VDD_69	W19
L24	VDD_14	VDD_70	W20
L25	VDD_15	VDD_71	W21
M12	VDD_16	VDD_72	W22
M14	VDD_17	VDD_73	W23
M16	VDD_18	VDD_74	W24
M18	VDD_19	VDD_75	W25
M20	VDD_20	VDD_76	Y12
M22	VDD_21	VDD_77	Y14
M24	VDD_22	VDD_78	Y16
P11	VDD_23	VDD_79	Y18
P13	VDD_24	VDD_80	Y20
P15	VDD_25	VDD_81	Y22
P17	VDD_26	VDD_82	Y24
P19	VDD_27	VDD_83	AB11
P21	VDD_28	VDD_84	AB13
P23	VDD_29	VDD_85	AB15
P25	VDD_30	VDD_86	AB17
R11	VDD_31	VDD_87	AB19
R12	VDD_32	VDD_88	AB21
R13	VDD_33	VDD_89	AB23
R14	VDD_34	VDD_90	AB25
R15	VDD_35	VDD_91	AC11
R16	VDD_36	VDD_92	AC12
R17	VDD_37	VDD_93	AC13
R18	VDD_38	VDD_94	AC14
R19	VDD_39	VDD_95	AC15
R20	VDD_40	VDD_96	AC16
R21	VDD_41	VDD_97	AC17
R22	VDD_42	VDD_98	AC18
R23	VDD_43	VDD_99	AC19
R24	VDD_44	VDD_100	AC20
R25	VDD_45	VDD_101	AC21
Y12	VDD_46	VDD_102	AC22
T14	VDD_47	VDD_103	AC23
T16	VDD_48	VDD_104	AC24
T18	VDD_49	VDD_105	AC25
T20	VDD_50	VDD_106	AD12
T22	VDD_51	VDD_107	AD14
T24	VDD_52	VDD_108	AD16
V13	VDD_53	VDD_109	AD18
V15	VDD_54	VDD_110	AD22
V17	VDD_55	VDD_111	AD24
V17	VDD_56		

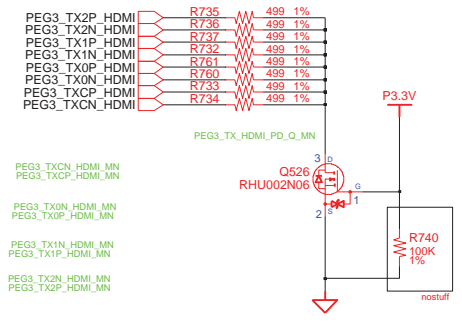
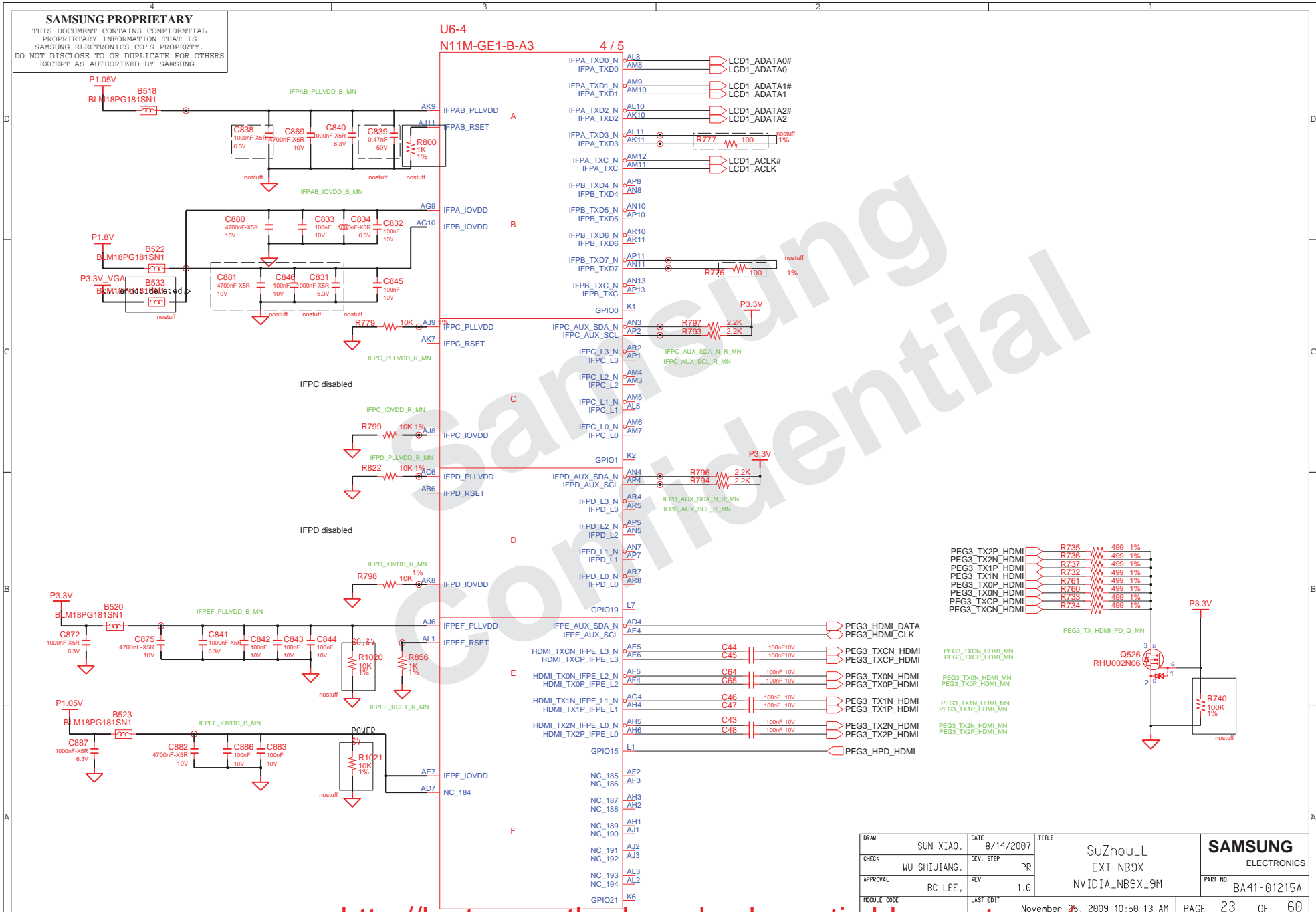
**EGFX\_CORE**

DRAW	SUN XIAO,	DATE	8/14/2007	TITLE	SuZhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	EXT NB9X	PART NO.	
APPROVAL	BC LEE,	REV	1.0	NVIDIA-NB9X_9M	BA41-01215A	
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	22 OF 60	

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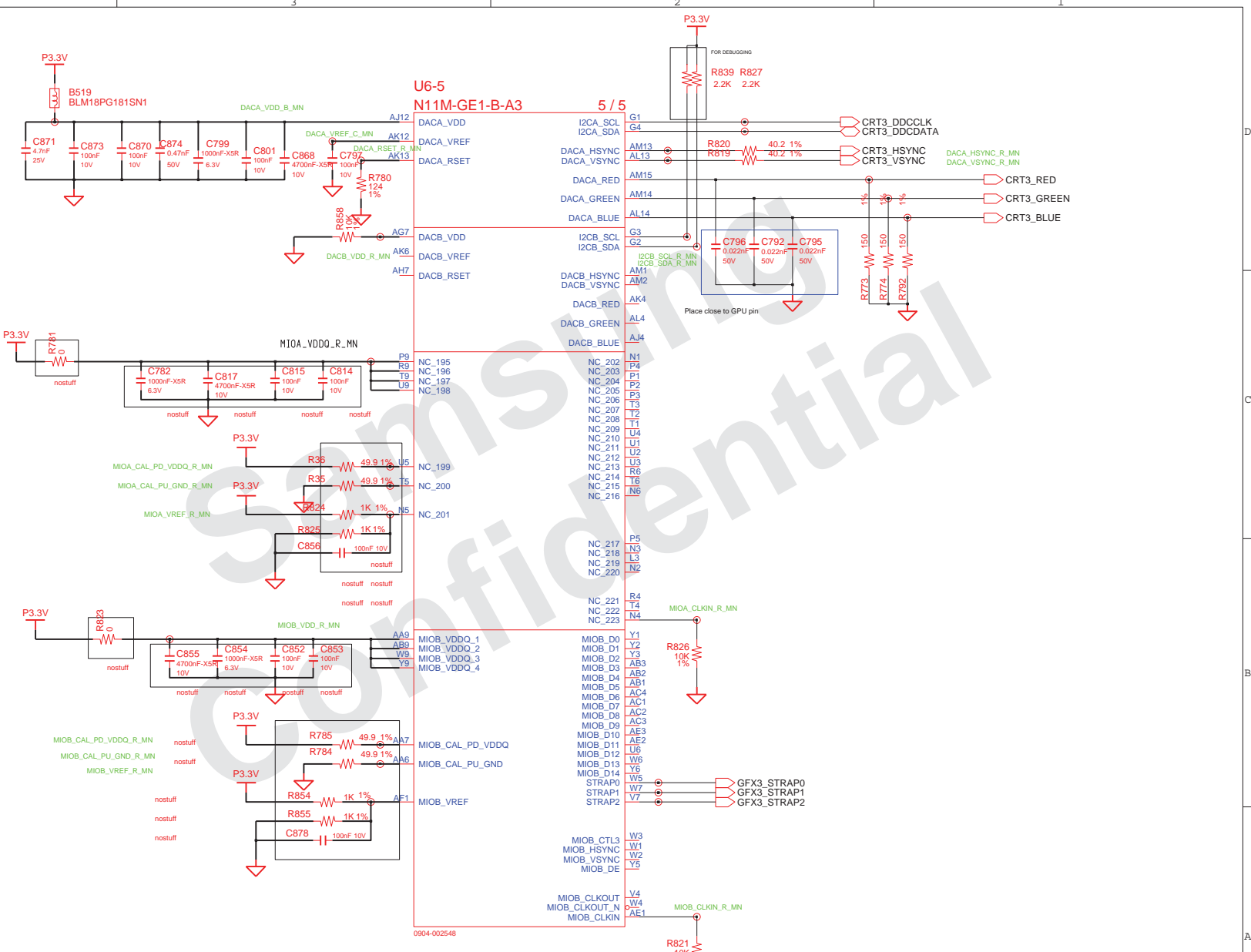
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CHECK	WU SHIJIANG,	DEV. STEP	PR	REV	1.0	
APPROVAL	BC LEE,	REV	1.0	LAST EDIT	November 25, 2009 10:50:13 AM	PAGE 23 OF 60
MODULE CODE						PART NO. BA41-01215A

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DESIGN	SUN XIAO,	DATE	8/18/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	N11M-GS		PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			PAGE 24 OF 60

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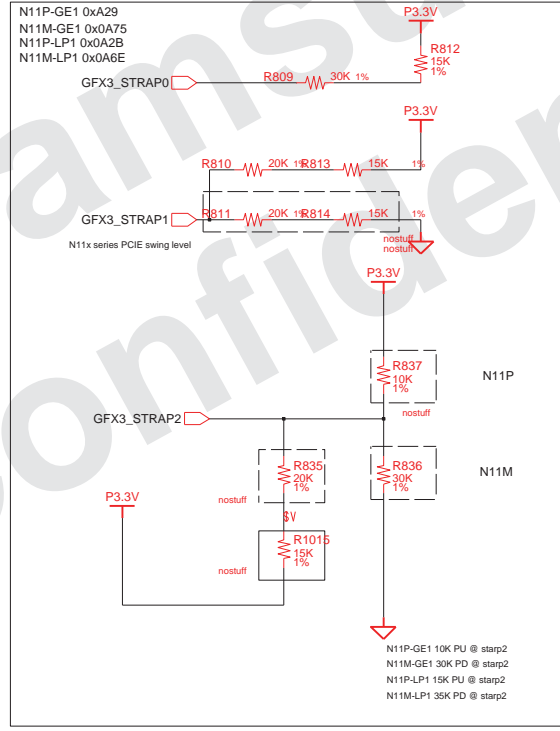
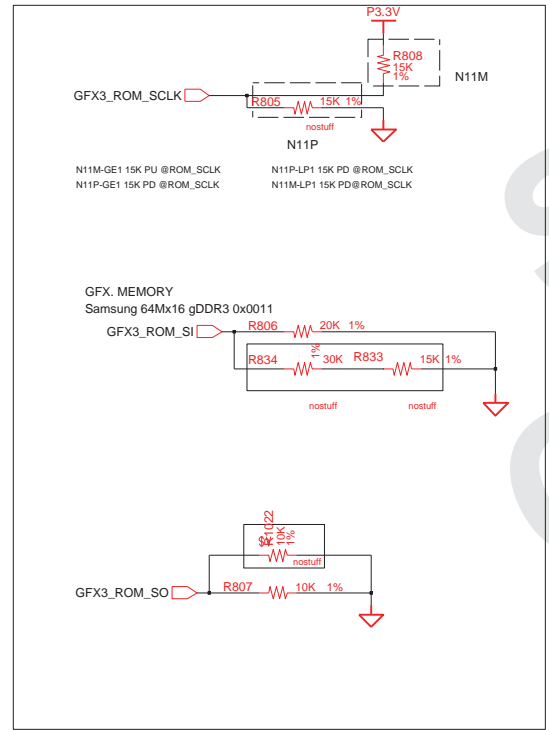
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### N11x\_40nm STRAP

Pin	Description	Activate	Pin	Description	Activate
GPIO(0)	General Purpose	NC	GPIO(12)	PWR_LEVEL	NC
GPIO(1)	HPD-C	NC	GPIO(13)	MEM_VID	NC
GPIO(2)	LCD0_BL_PWM	High	GPIO(14)	PWR_CTRL1	NC
GPIO(3)	LCD0_VDD	High	GPIO(15)	HPD-E	High
GPIO(4)	LCD0_BL_EN	High	GPIO(16)	FAN_PWM	NC
GPIO(5)	GPU VID0	00 0.8v 10 0.95v	GPIO(17)	Reserved	NC
GPIO(6)	GPU VID1	01 0.85v 11 1.03v	GPIO(18)	Reserved	NC
GPIO(7)	GPU VID2	NC	GPIO(19)	HPD-D	NC
GPIO(8)	OVERT	LOW			
GPIO(9)	ALERT	NC			
GPIO(10)	MEM_VREF	NC			
GPIO(11)	SLI_SYNC	NC			

STRAP PIN	BIT 3	BIT 2	BIT 1	BIT 0
ROM_SO	XCLK_417	FB_0_BAR_SIZE	SMB_ALT_ADDR	VGA_DEVICE
ROM_SCLK	PCI_DEVID[4]	SUB_VENDOR	SLOT_CLK_CFG	PEX_PLL_EN_TERM
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]
STRAP2	PCI_DEVID[3]	PCI_DEVID[2]	PCI_DEVID[1]	PCI_DEVID[0]
STRAP1	3GIO_PADCFG[3]	3GIO_PADCFG[2]	3GIO_PADCFG[1]	3GIO_PADCFG[0]
STRAP0	USER[3]	USER[2]	USER[1]	USER[0]

RESISTOR	PULL UP	PULL DOWN
5K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
25K	1100	0100
30K	1101	0101
35K	1110	0110
45K	1111	0111



**N11P-GE1**

	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	1	27M
SCLK	0	0	1	0	DEVICE ID GFX TPYE
SI	0	0	1	1	gDDR3 1Gb
Strap2	1	0	0	1	N11P-GE1 DEVICE ID
Strap1	1	1	1	0	PEG PCIE swing level
Strap0	1	1	1	1	EDID_EN

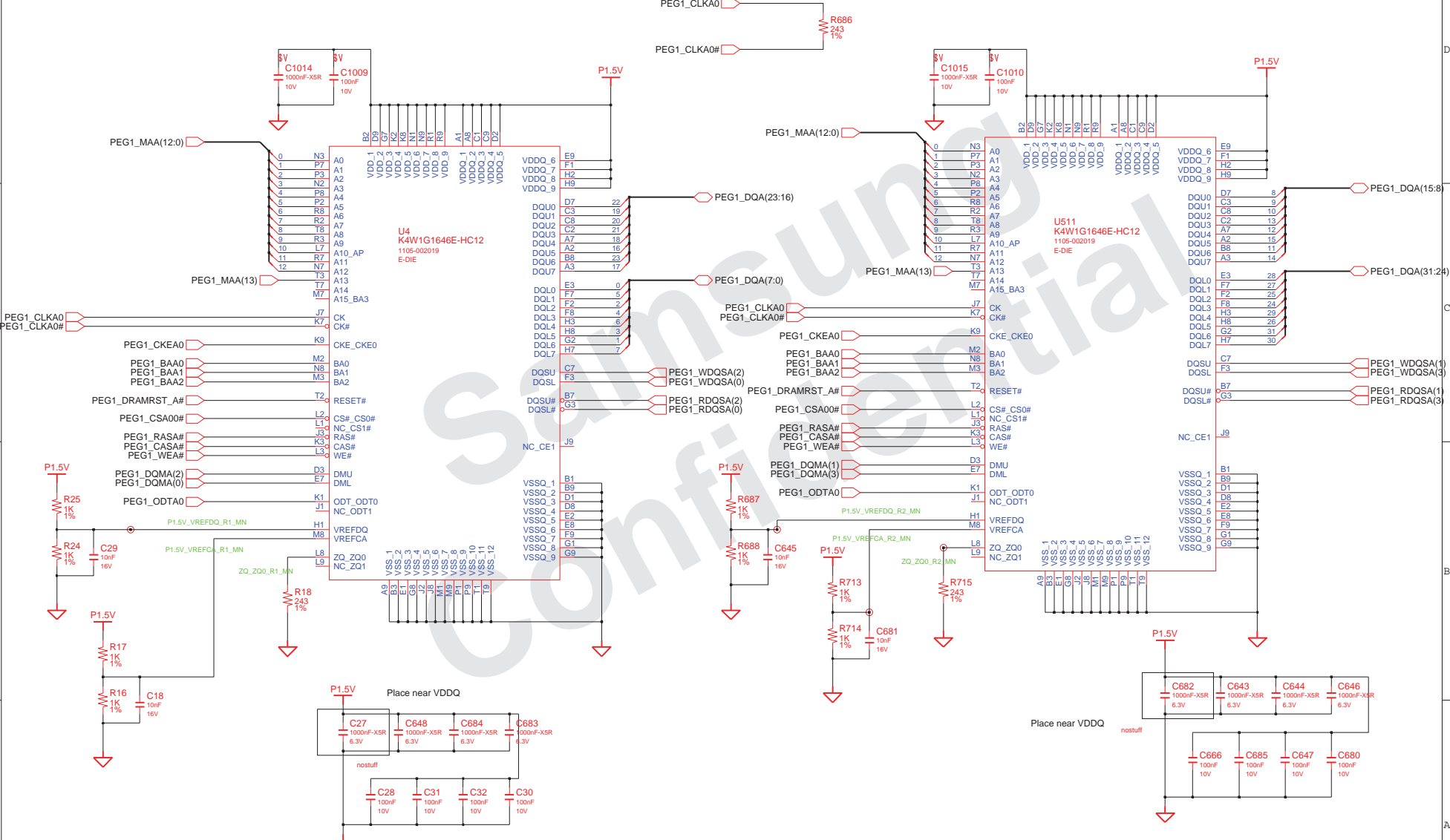
**N11M-GE1**

	Bit3	Bit2	Bit1	Bit0	
ROMSO	0	0	0	1	27M
SCLK	0	0	1	0	DEVICE ID GFX TPYE
SI	0	0	1	1	gDDR3 1Gb
Strap2	0	1	0	1	N11M-GE1 DEVICE ID
Strap1	1	1	1	0	PEG PCIE swing level
Strap0	1	1	1	1	EDID_EN

DESIGN	SUN XIAO,	DATE	8/21/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	N11M-GS		PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			PAGE 25 OF 60

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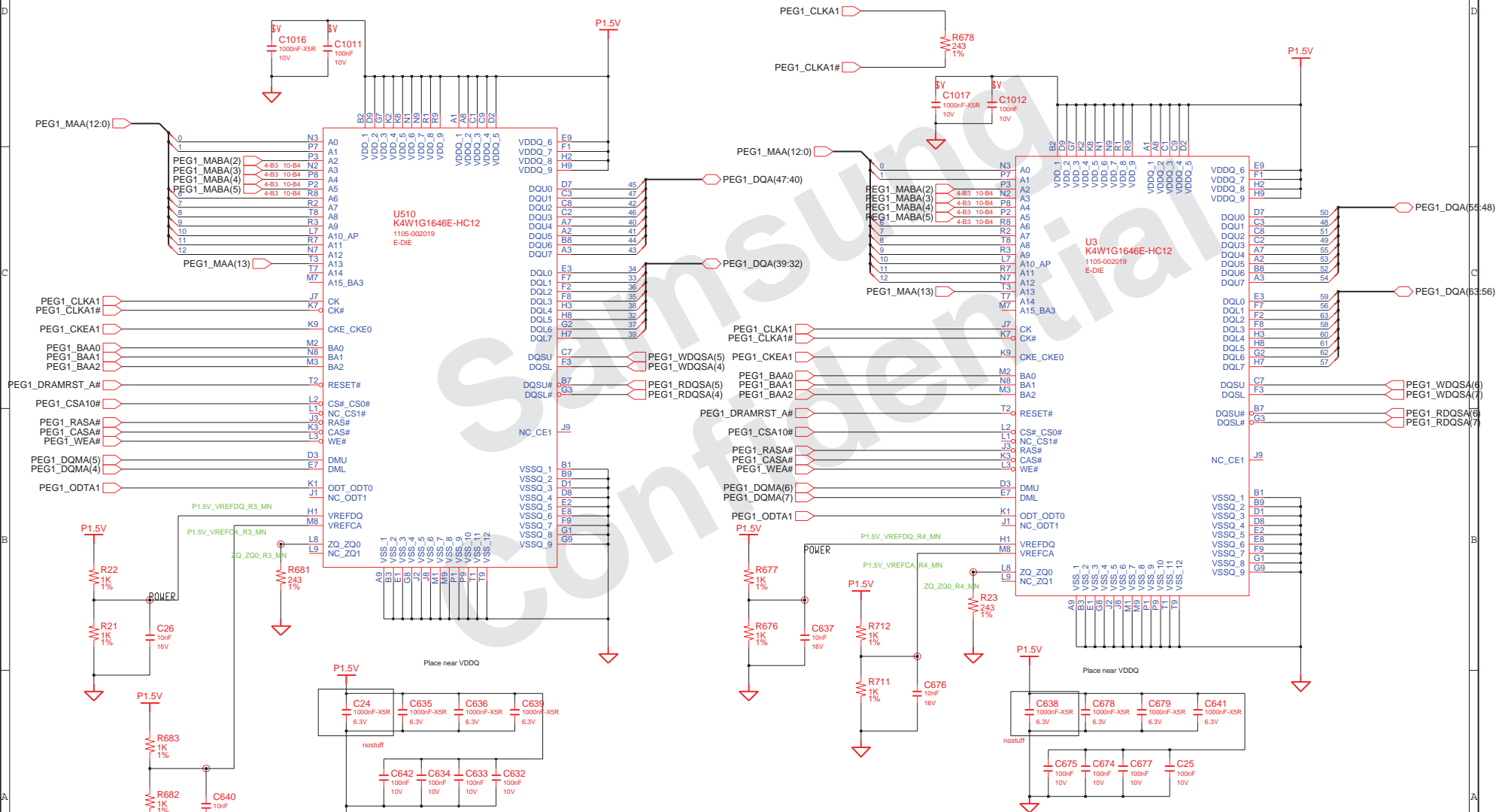
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DESIGN	SUN XIAO,	DATE	04/29/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	GRAPHIC_MEM_1Gb A#0	PART NO.	
APPROVAL	BC LEE,	REV	1.0	gDDR3-1Gb	BA41-01215A	PAGE 26 OF 60
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			

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### A-Channel #1

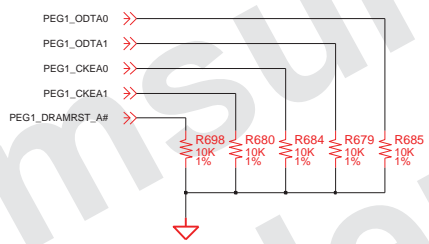


DESIGN	SUN XIAO,	04/29/2009	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	GRAPHIC_MEM_1Gb A#1	
APPROVAL	BC LEE,	REV	gDDR3-1Gb	PART NO. BA41-01215A
MODULE CODE	LAST EDIT	November 25, 2009 10:50:13 AM	PAGE 27 OF 60	

<http://laptop-motherboard-schematic.blogspot.com/>

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gDDR3 Memory PULL UP & PULL DOWN

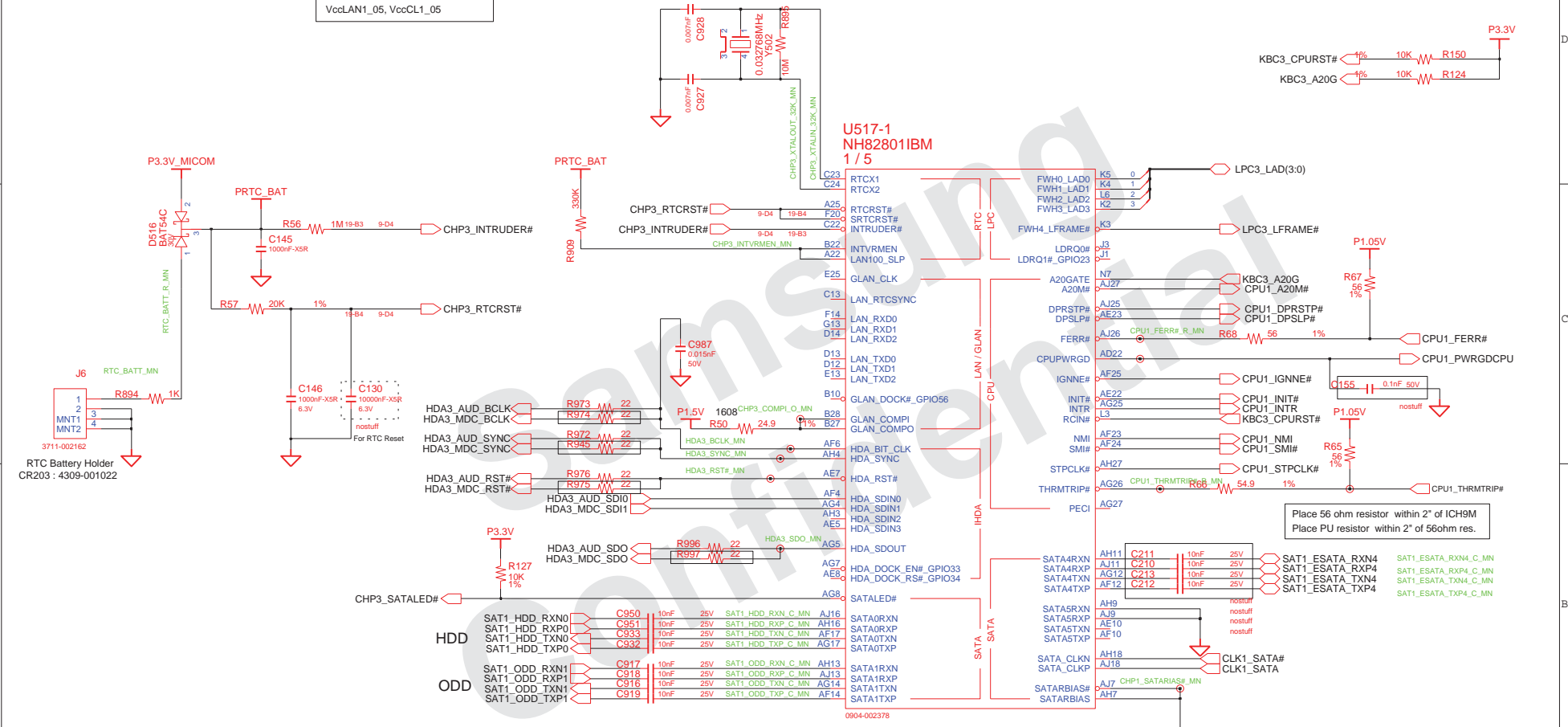


Samsung  
Confidential

DESIGN	SUN XIAO,	DATE	03/14/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	PULL-UP&PULL-DOWN	PART NO.	
APPROVAL	BC LEE,	REV	1.0	gDDR3-1Gb	BA41-01215A	
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	28 OF 60	

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Internal VR Strap  
 INTVRMEN Pull up  
 VccSus1\_05, VccSus1\_5, VccCL1\_5  
 VccLAN1\_05, VccCL1\_05

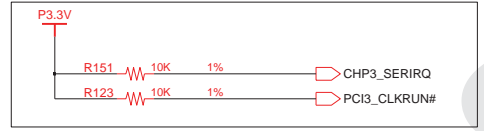


SATA Cap. Place ment :  
 Distance b/w the ICH9-M & cap on the "P" signal should be identical  
 distance b/w the ICH9-M & cap on the "N" signal same pair.

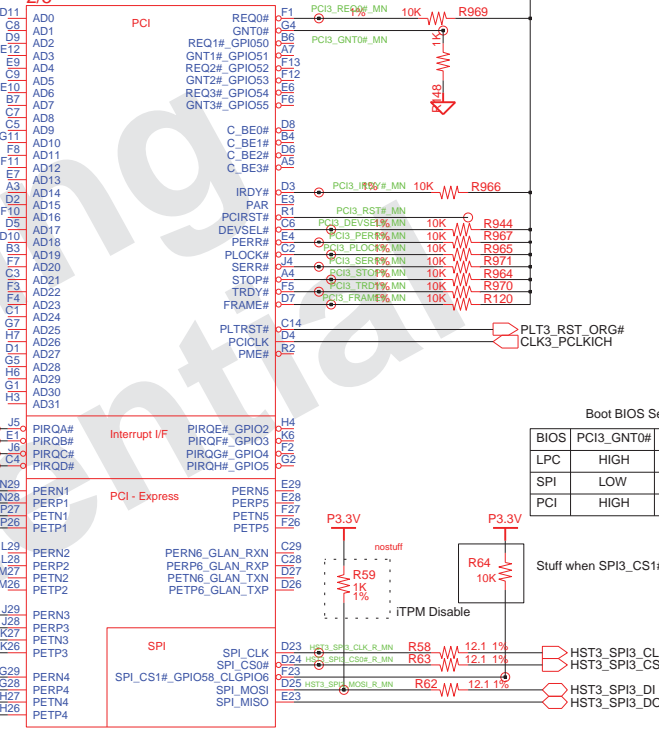
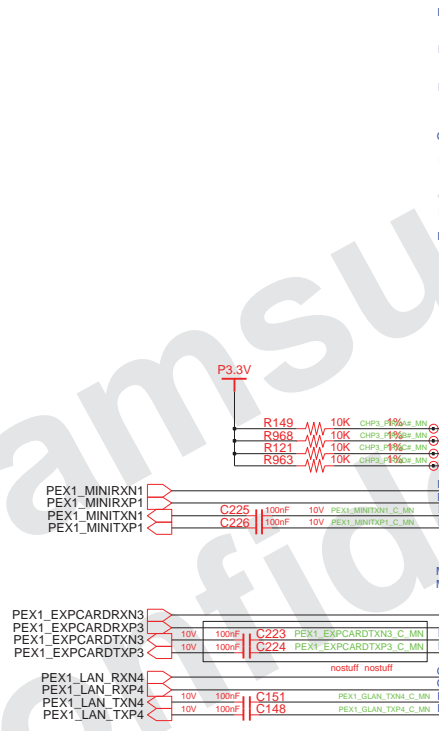
DRAW	SUN XIAO,	DATE	1/10/2008	TITLE	Suzhou_L ICH9M_B	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		ICH9-M (1/5)	
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			PAGE 29 OF 60

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**U517-2  
 NH82801IBM  
 2/5**



LPC option : These are used with LPC

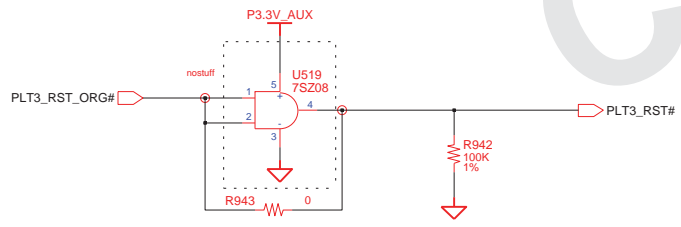


Boot BIOS Select

BIOS	PCI3_GNT0#	SPI3_CS1#
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW

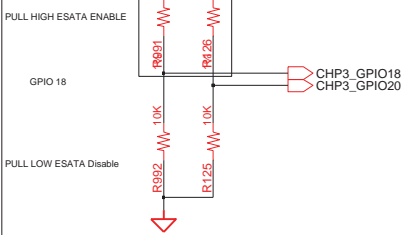
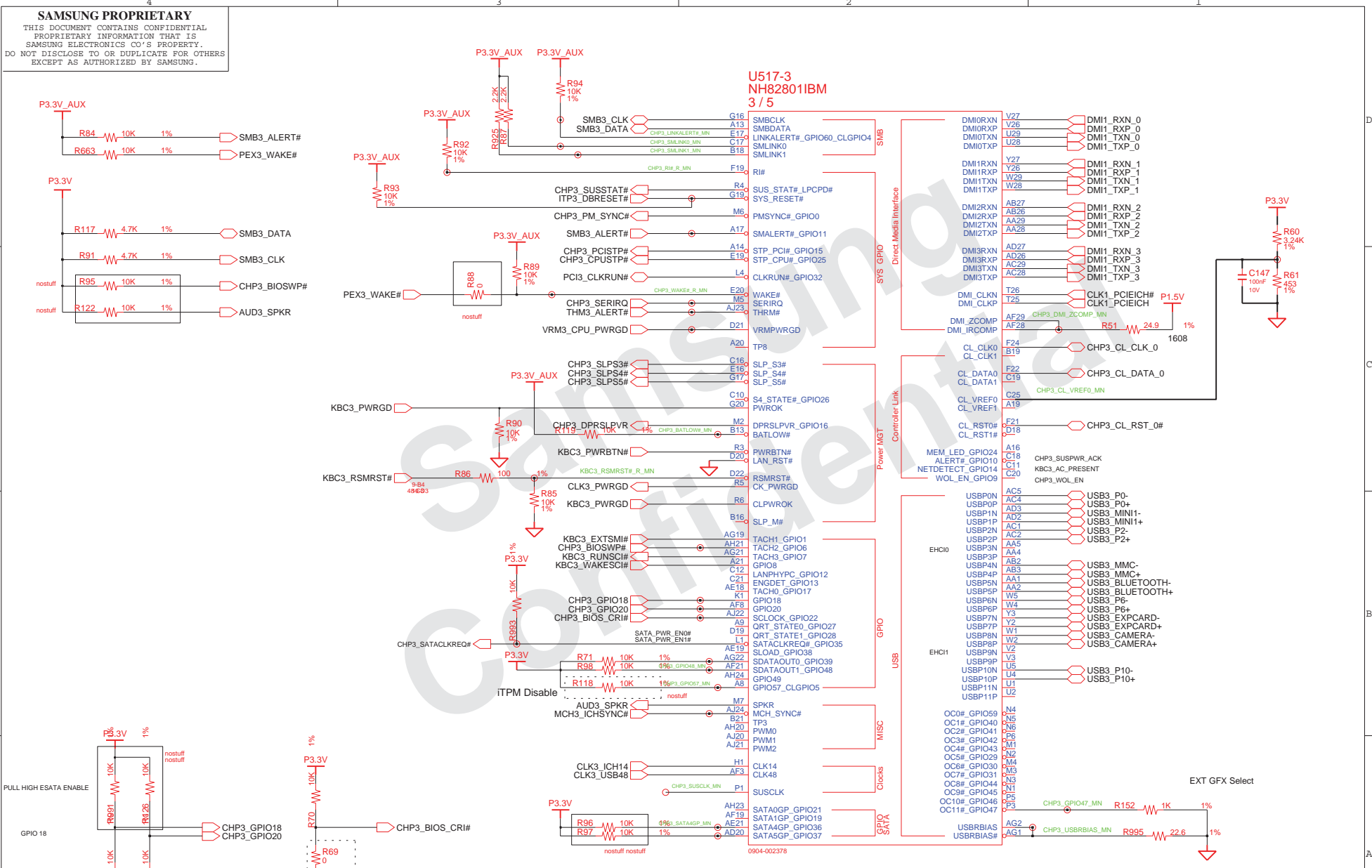
Stuff when SPI3\_CS1# is not used.

AC caps : PCIe need to be within 250mils of the driver  
 Resistor for Test : Place Stuffing Option to minimize stubs



DRAW	SUN XIAO,	DATE	1/10/2008	TITLE	Suzhou_L ICH9M_B	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	REV	1.0	
APPROVAL	BC LEE,	REV	1.0	MODULE CODE	undef ined	PART NO. BA41-01215A
LAST EDIT						November 25, 2009 10:50:13 AM
PAGE						30 OF 60

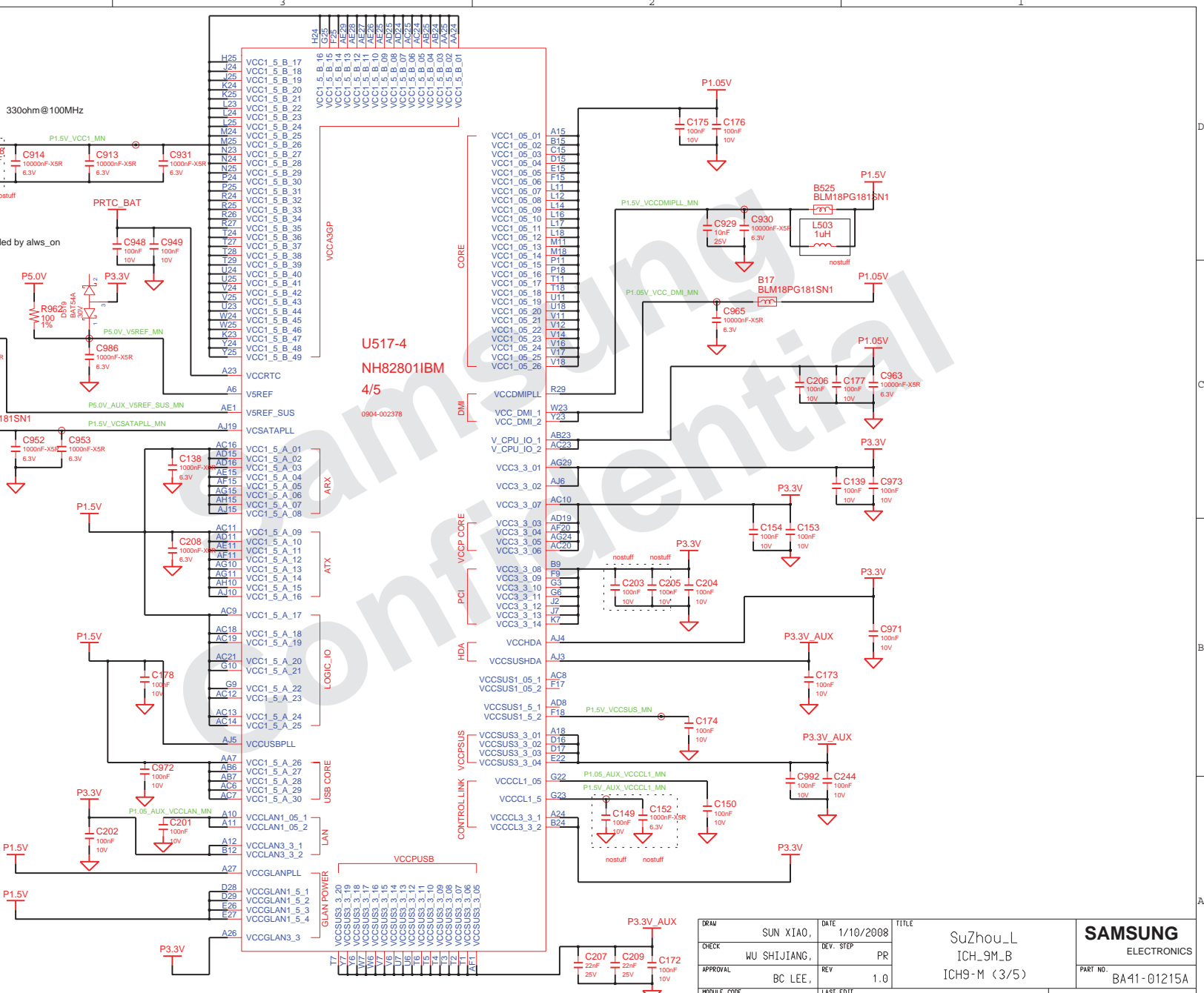
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BIOS CRISIS RECOVER STRAP  
 PLACE NEAR KEYBOARD  
 (Put it a debugger connector)

DRAW	SUN XIAO,	DATE	1/10/2008	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	ICH9M_B	PART NO.	
APPROVAL	BC LEE,	REV	1.0	ICH9-M (3/5)	BA41-01215A	
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	31	OF 60

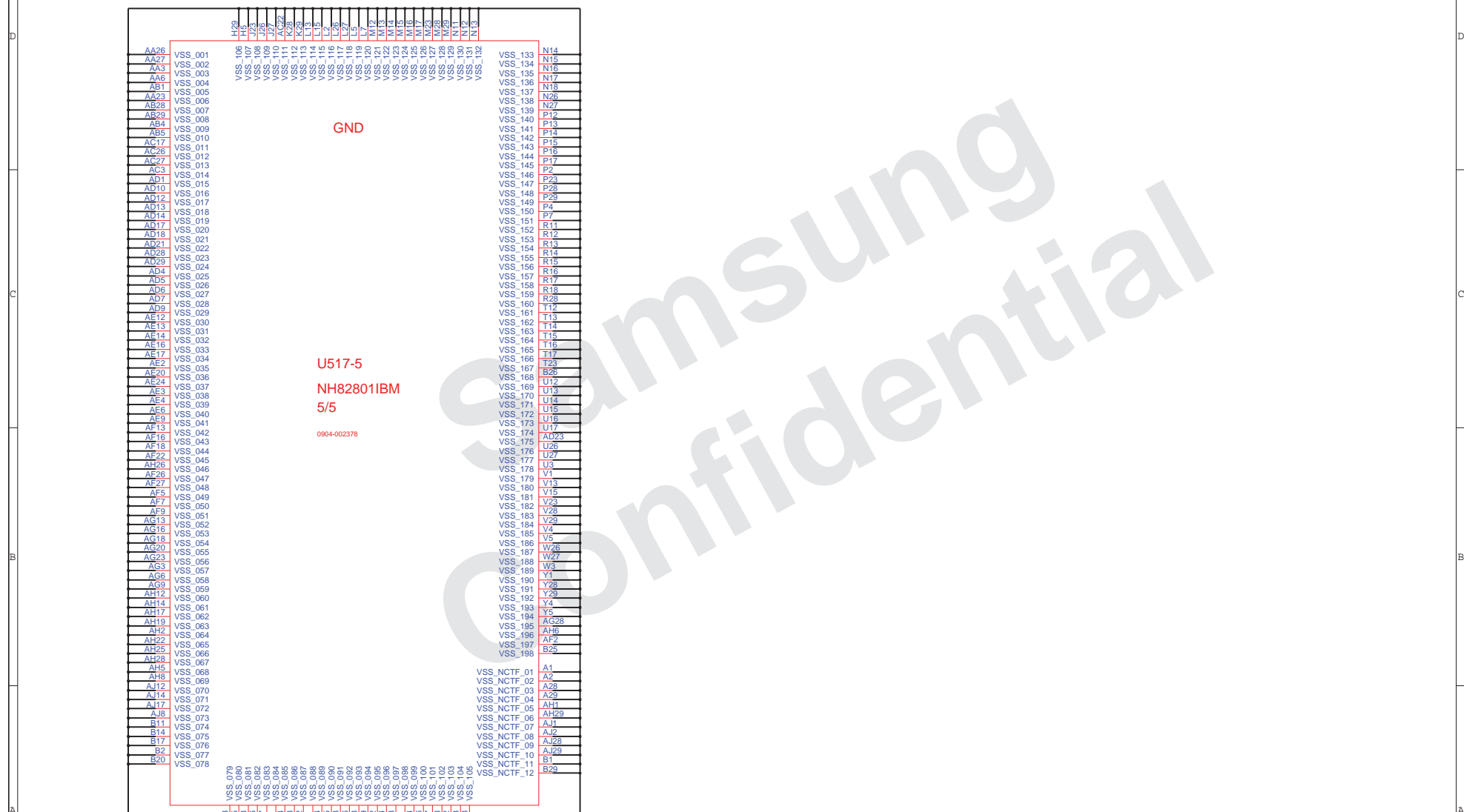
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DRAW CHECK APPROVAL MODULE CODE	SUN XIAO, WU SHIJIANG, BC LEE,	DATE DEV. STEP REV 1/10/2008 PR 1.0	TITLE SuZhou_L ICH9M_B ICH9-M (3/5)	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01215A
--	--------------------------------------	--	--	--



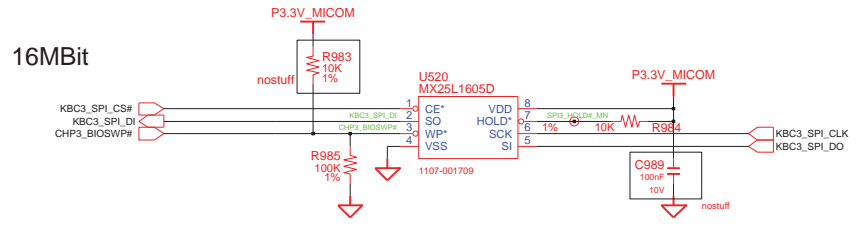
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DRAW	SUN XIAO,	DATE	1/10/2008	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	ICH9M_B		
APPROVAL	BC LEE,	REV	1.0	ICH9-M (5/5)	PART NO.	BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM		PAGE	33 OF 60

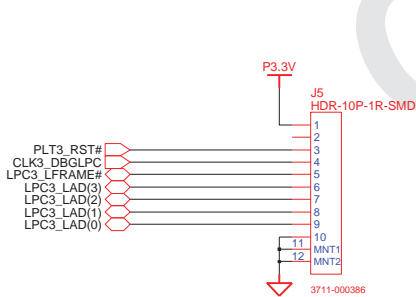
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# SPI\_BIOS\_ROM

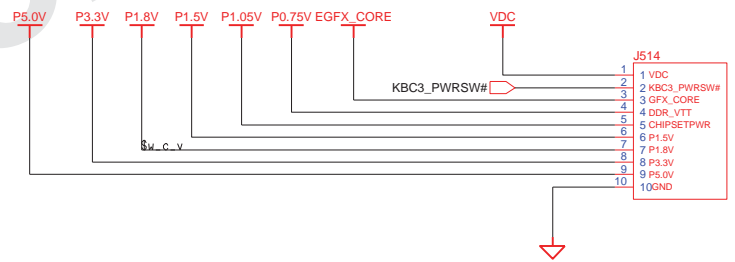


02	VERIFY REAL MODE	66	CONFIGURE ADVANCE CACHE REG.
03	DISABLE NMI	6A	DISPLAY EXTERNAL CACHE SIZE
04	GET CPU TYPE	6C	DISPLAY SHADOW MESSAGE
06	INIT. SYSTEM HW	6E	DISPLAY NON-DISPOSABLE SEGMENT
08	INIT. CHIPSET REG.	70	DISPLAY ERROR MESSAGE
09	SET IN POST FLAG	72	CHECK FOR CONFIGURATION ERROR
0A	INIT CPU REG	74	TEST REAL-TIME CLOCK
0B	CPU CACHE ON	76	CHECK FOR KEYBOARD ERROR
0C	INIT CACHE TO POST	7C	SETUP HARDWARE INTERRUPT VECTOR
0E	INIT. I/O VALUE	7E	TEST COPROCESSER IF PRESENT
0F	ENABLE THE L-BUS IDE	80	DISABLE ON-BOARD I/O PORT
10	INIT. POWER MANAGER	82	DETECT AND INSTALL EXT RS232C
11	LOAD ALTERNATE REG.	84	DETECT AND INSTALL EXT PARALLEL
13	PCI BUS MASTER RESET	86	RE-INIT. ON-BOARD I/O PORT
		88	INIT. BIOS DATA ROM
	WITH INITIAL POST VALUE	8A	INIT. EXTENDED BIOS DATA AREA
14	INIT. KEYBOARD CONTROLLER	8C	INIT. FDD CONTROLLER
16	CHECK CHECKSUM	9A	SHADOW OPTION ROMS
18	8254 TIMER INIT.	9C	SETUP POWER MANAGEMENT
1A	8237 DMA CONTROLLER INIT.	9E	ENABLE H/W INTERRUPT
1C	RESET INTERRUPT CONTROLLER	A0	SET TIME OF DAY
20	TEST DRAM REFRESH	A4	INIT. TYPEMATIC RATE
22	TEST 8742 KEYBOARD CONTROLLER	A8	ERASE F2 PROMPT
24	SET ES SEGMENT REG. TO 4GB	AA	SCAN FOR F2 KEY STROKE
26	ENABLE A20	AC	ENTER SETUP
28	AUTO SIZING DRAM	AE	CLEAR IN POST FLAG
32	COMPLETE THE CPU SPEED	B0	CHECK FOR ERRORS
34	TEST CMOS RAM	B2	POST DONE-PREPARE TO BOOT O/S
38	SHADOW SYSTEM BIOS ROM	B4	ONE BEEP
3A	AUTO SIZING CACHE	B6	CHECK PASSWORD (OPTION)
3C	CONFIGURE ADVANCED CHIPSET REG.	B7	ACPI INIT
3D	LOAD ALTERNATE REG. WITH CMOS VALUE	B8	DMI INIT
42	INIT. INTERRUPT VECTOR	BE	CLEAR SCREEN
44	INIT. BIOS INTERRUPT	C0	TRY BOOT WITH INT19
46	CHECK ROM COPYRIGHT NOTICE	D0	INTERRUPT HANDLER ERROR
47	INIT. I20 SUPPORT IF INSTALLED	D2	UNKNOWN INTERRUPT ERROR
48	CHECK VIDEO CONFIGURE AGAINST CMOS	D4	PENDING INTERRUPT ERROR
49	INIT. PCI BUS AND DEVICE	D6	SHUTDOWN 5
4A	INIT. ALL VIDEO BIOS ROM	D8	SHUTDOWN ERROR
4C	SHADOW VIDEO BIOS ROM	DA	EXTENDED BLOCK MOVE
50	DISPLAY CPU TYPE AND SPEED	DC	SHUTDOWN 10
52	TEST KEYBOARD	89	ENABLE NMI
54	SET KEYCLICK IF ENABLED	90	INIT. HDD CONTROLLER
56	ENABLE KEYBOARD	91	INIT. LOCAL BUS HDD CONTROLLER
58	TEST FOR UNEXPECTED INTERRUPTS	92	JUMP TO USER PATCH 1
5A	DISPLAY PRESS. SETUP	94	DISABLE A20 ADDRESS LINE
5C	TEST RAM BETWEEN 512K AND 640K	96	CLEAR HUGE ES SEGMENT REG.
60	TEST EXTENDED MEMORY	98	SEARCH FOR OPTION ROMS
62	TEST EXTENDED MEMORY ADDRESS LINE		
64	JUMP TO USER PATCH 1		

## 80H DECODER CONNECTOR



## ICT PORT

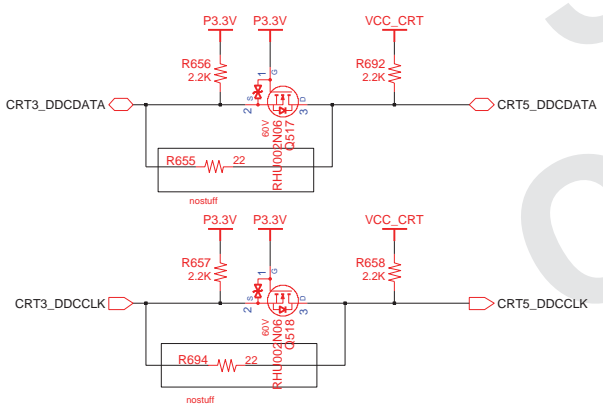
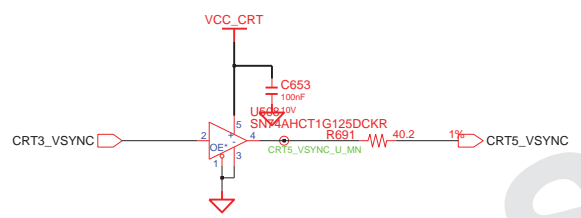
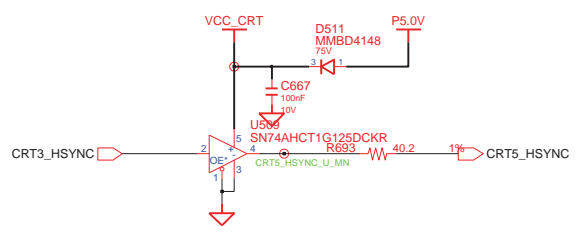


DRAW	SUN XIAO,	DATE	8/12/2006	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	SPI_BIOS_ROM		
APPROVAL	BC LEE,	REV	1.0	SPI_BIOS_ROM	PART NO.	BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM		PAGE	34 OF 60

<http://laptop-motherboard-schematic.blogspot.com/>

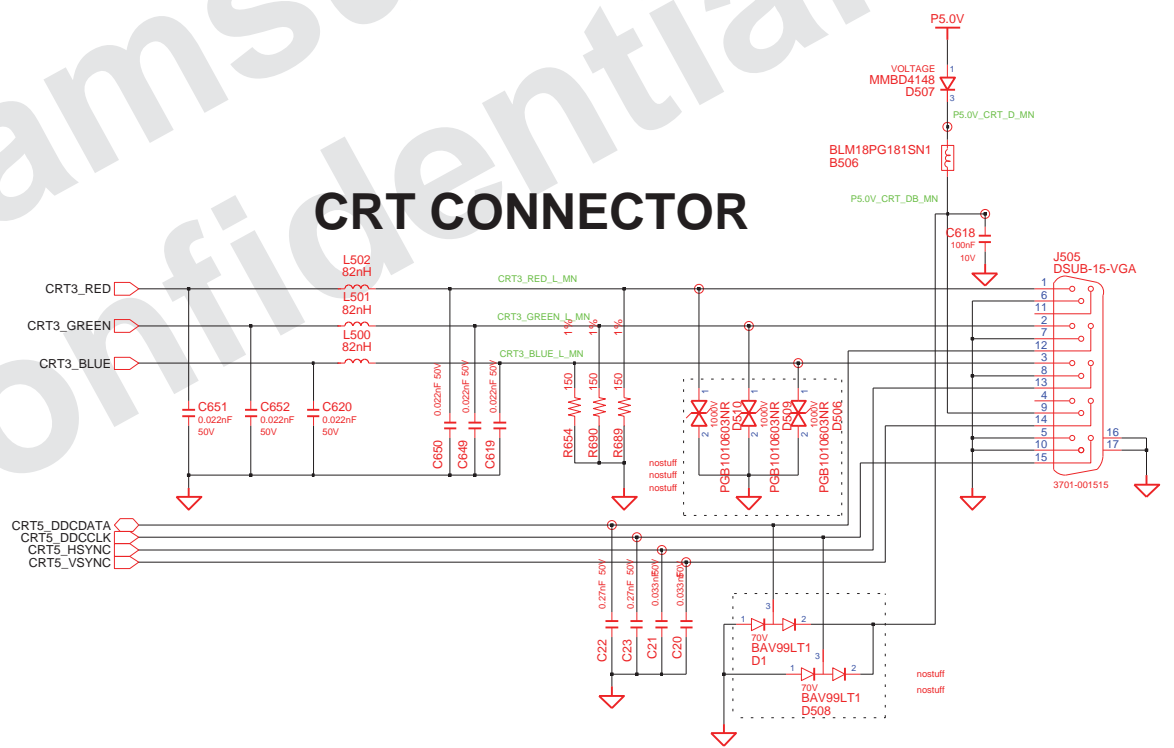
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# CRT



Check "CRT3\_DDCCLK/DATA" Voltage Level  
 2N06 Can be replaced with SM6K2

## CRT CONNECTOR



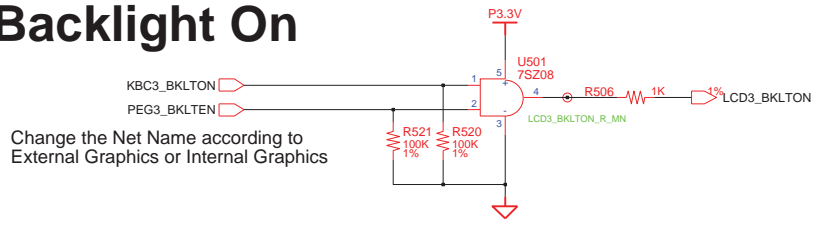
DESIGN	SUN XIAO,	DATE	01/08/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	GRAPHICS_IF		
APPROVAL	BC LEE,	REV	1.0	CRT		PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			PAGE 35 OF 60

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# LVDS

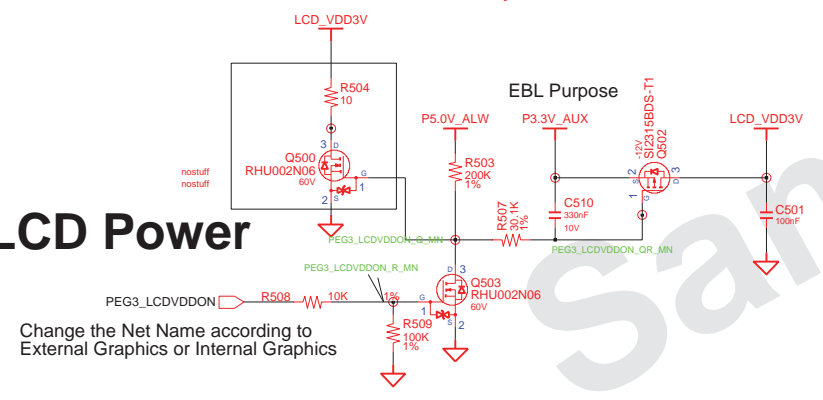
## 1Ch. LCD Connector

### Backlight On



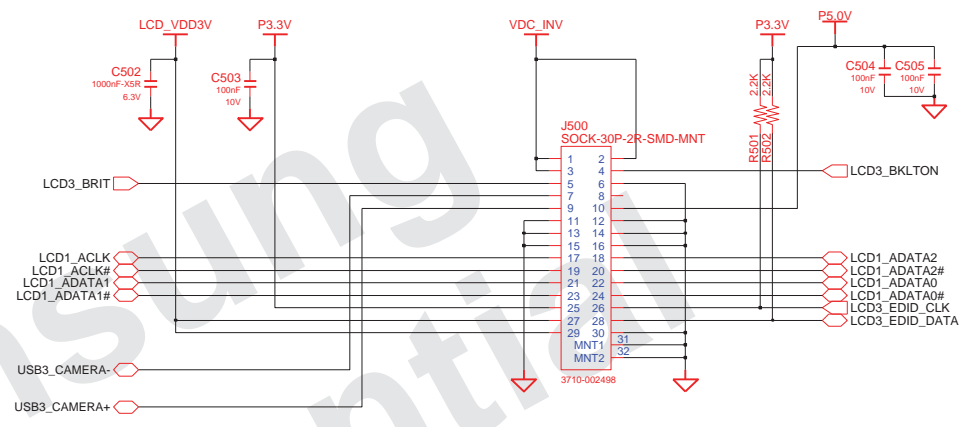
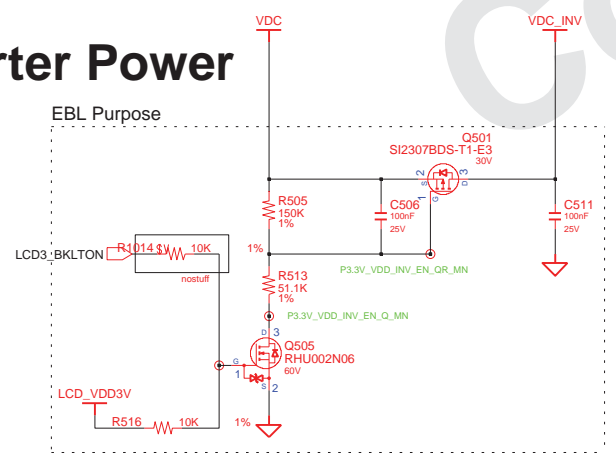
Change the Net Name according to External Graphics or Internal Graphics

### LCD Power



Change the Net Name according to External Graphics or Internal Graphics

### Inverter Power



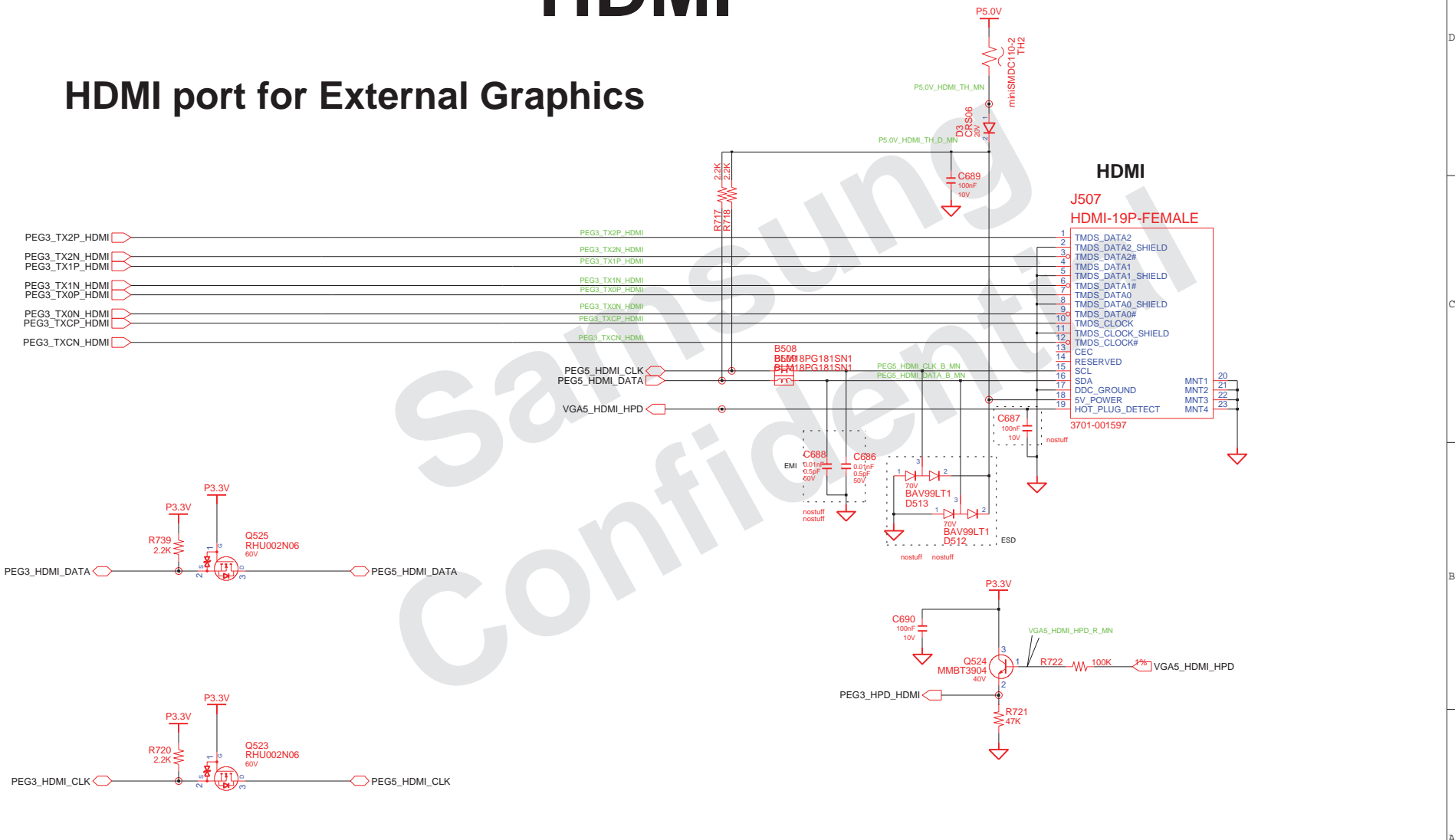
<http://laptop-motherboard-schematic.blogspot.com/>

DESIGN	SUN XIAO,	DATE	01/08/2009	TITLE	Suzhou_L GRAPHICS_IF LVDS	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01215A
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			
						PAGE 36 OF 60

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# HDMI

## HDMI port for External Graphics

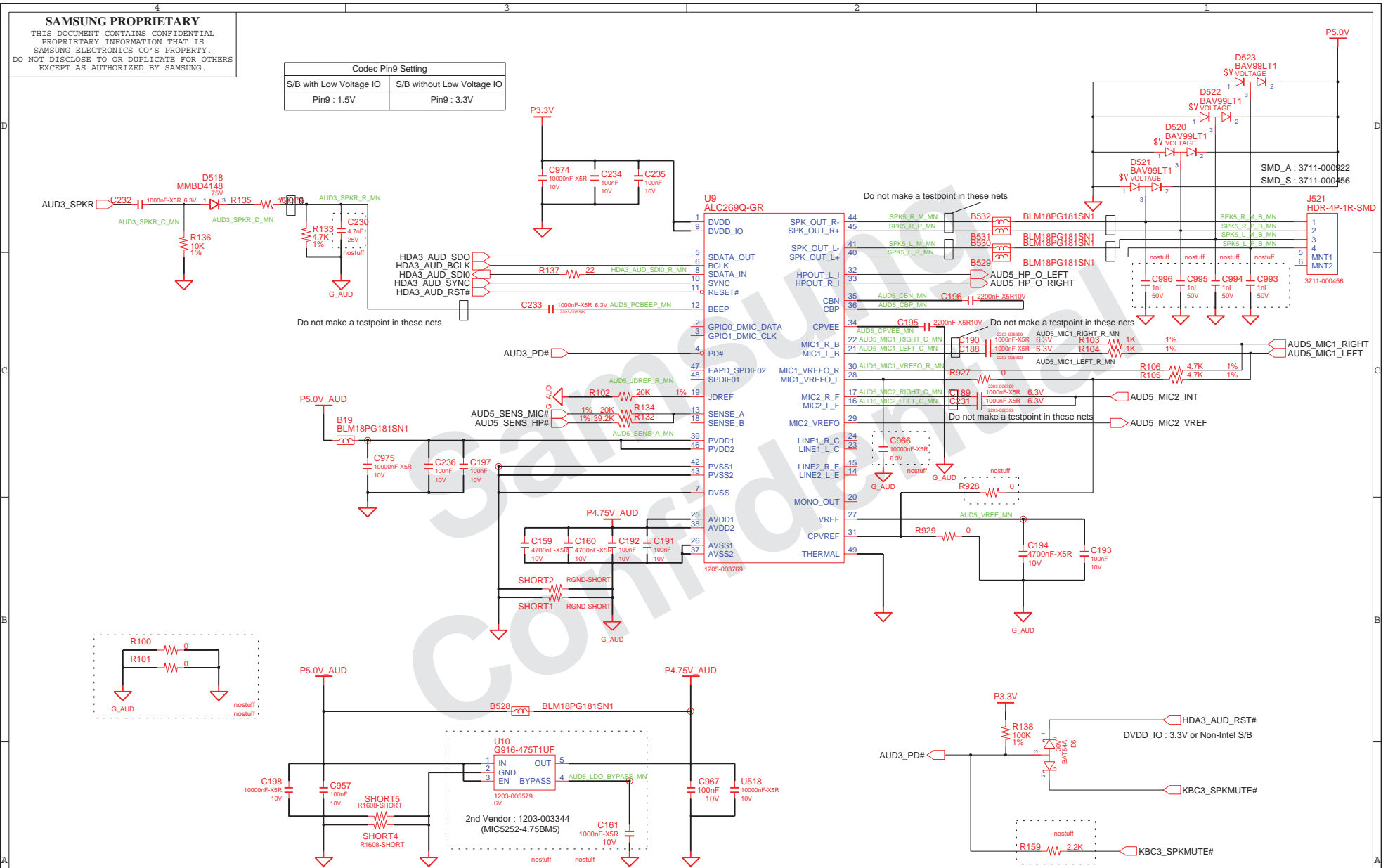


DESIGN	SUN XIAO,	DATE	01/08/2009	TITLE	Suzhou_L GRAPHICS_IF	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	HDMI	PART NO.	
APPROVAL	BC LEE,	REV	1.0		BA41-01215A	
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	37	OF 60

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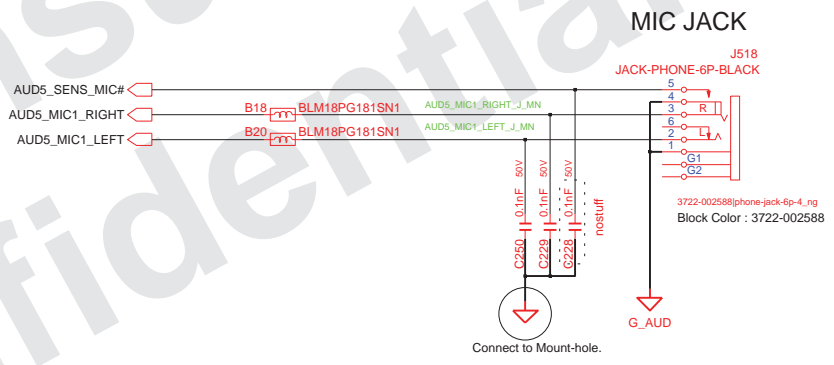
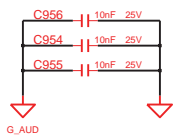
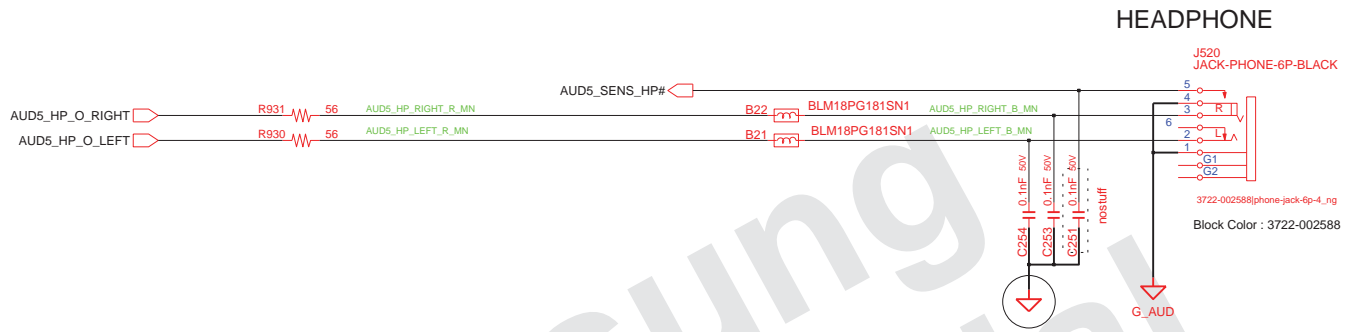
Codec Pin9 Setting	
S/B with Low Voltage IO	S/B without Low Voltage IO
Pin9 : 1.5V	Pin9 : 3.3V



DESIGN	SUN XIAO,	DATE	3/13/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR		HDA_ALC269_GR	
APPROVAL	BC LEE,	REV	1.0		AUDIO CODEC	PART NO.
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			BA41-01215A
						PAGE 38 OF 60

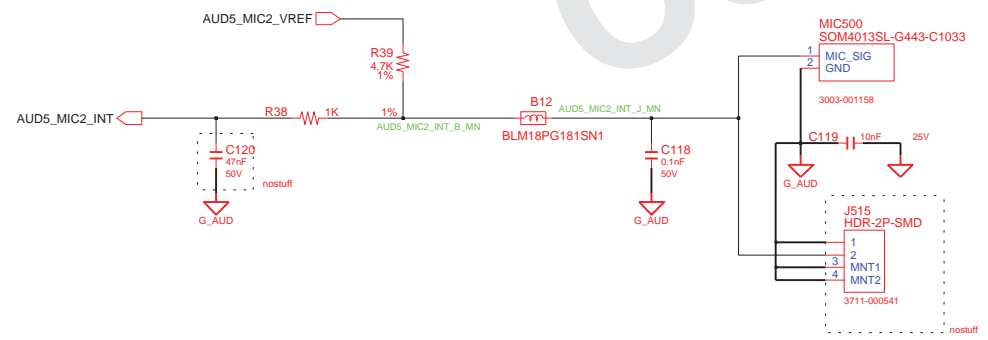
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Analog mono Mic Ass'y : Place inside Audio Analog Plane

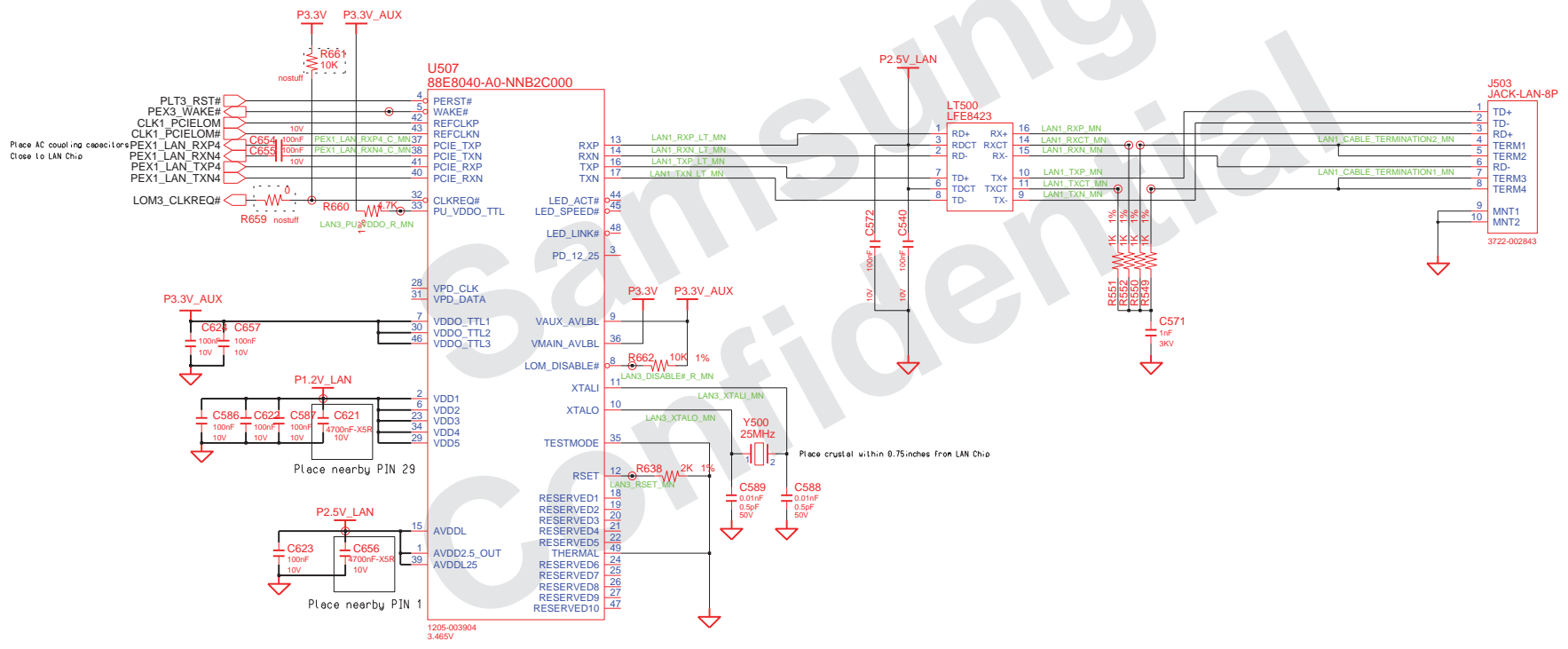
SMD MIC



DESIGN	SUN XIAO,	DATE	3/13/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	HDA_ALC269_GR	AUDIO INPUT/OUTPUT	
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			PAGE 39 OF 60

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# MARVELL 88E8040T



1205-003904  
3.465V

DESIGN	SUN XIAO,	DATE	3/17/2009	TITLE	SuZhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	40	OF 60

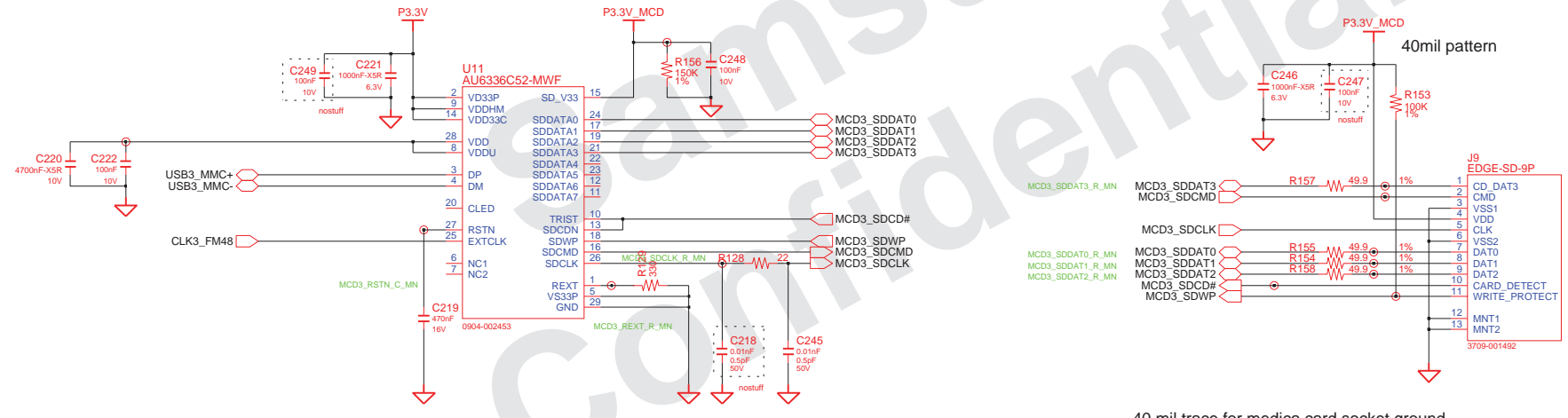
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# 3 IN 1

P3.3V\_MCD distance between R5U880 and socket should be less than 2 inches



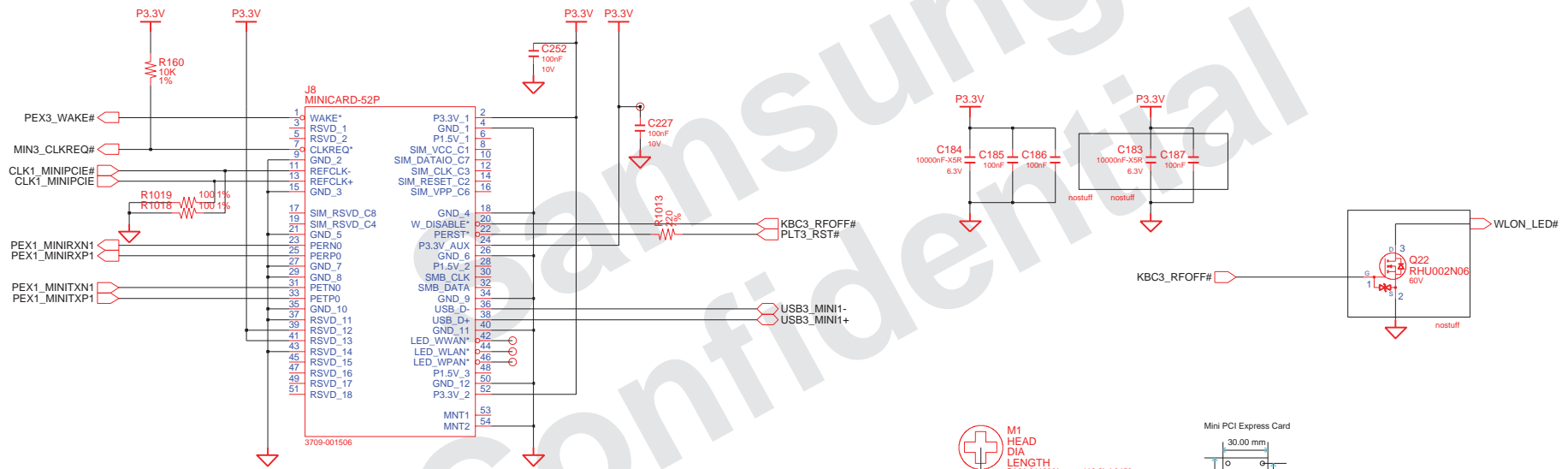
40 mil trace for medica card socket ground

DESIGN	SUN XIAO,	DATE	4/29/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	41	OF 60

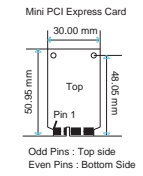
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### WLAN, 7mm



To fix Shirley Peak EMI Issue  
 Place it at the old rubber area

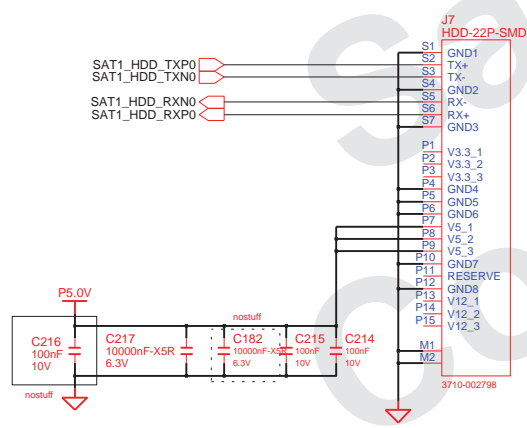


DESIGN	SUN XIAO,	DATE	6/6/2008	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MINI_PCIE_CONN	PART NO.	
APPROVAL	BC LEE,	REV	1.0		BA41-01215A	
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM		PAGE	42 OF 60

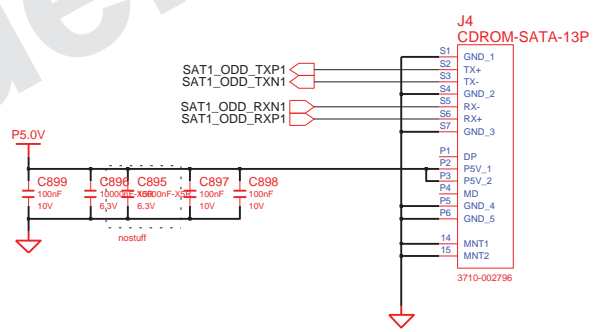
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# SATA I/F CONN

## SATA HDD CONN



## SATA ODD CONN



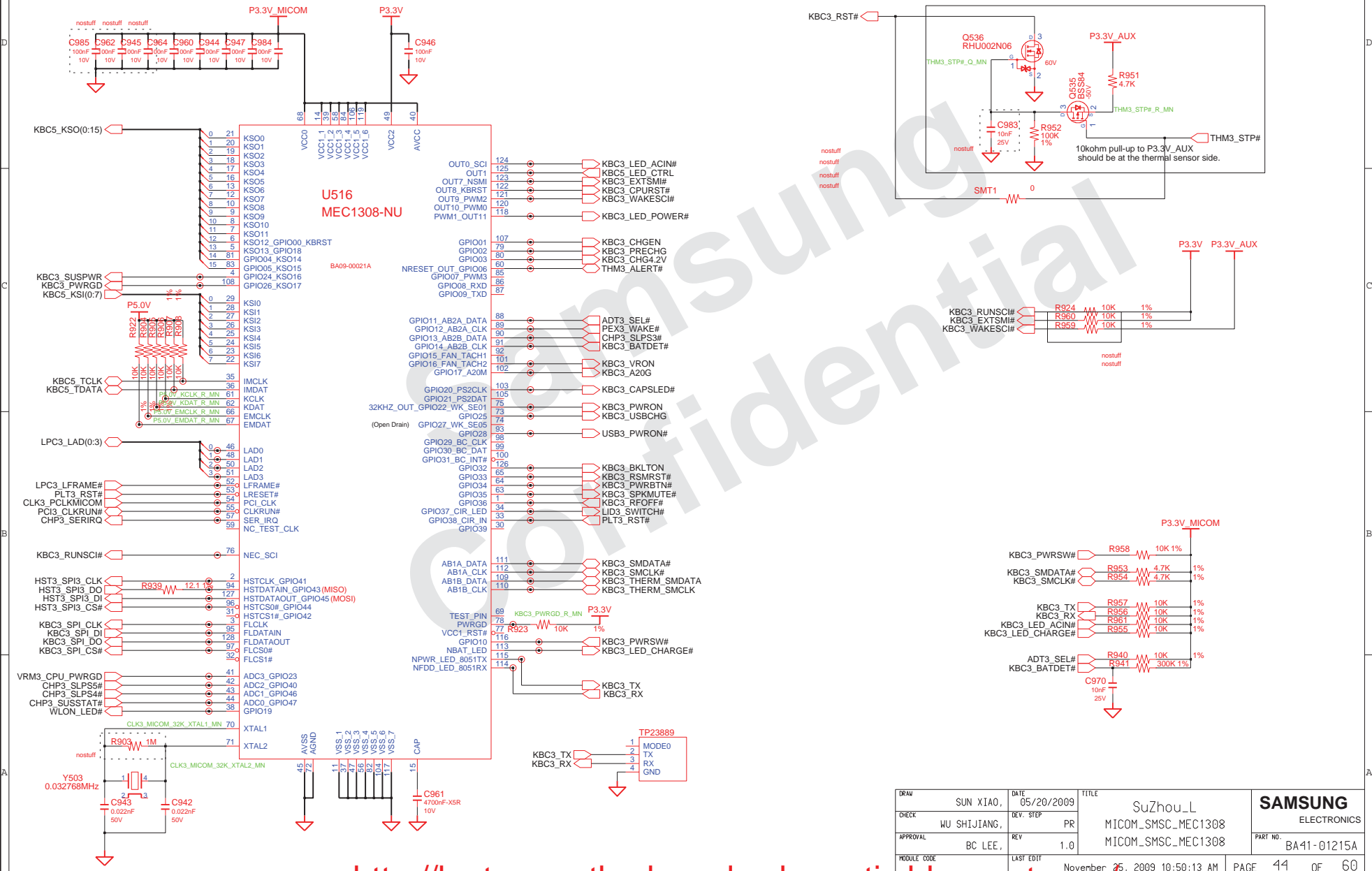
DESIGN	SUN XIAO,	DATE	6/6/2008	TITLE	Suzhou_L SATA_DEVICES	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01215A
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			
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# MAIN BOARD (MICOM)

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## MICOM POWER RESET



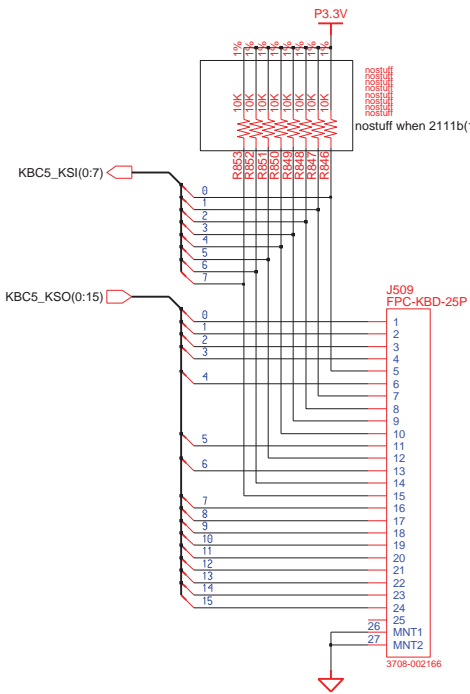
<http://laptop-motherboard-schematic.blogspot.com/>

DRAW	SUN XIAO,	DATE	05/20/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MICOM_SMSC_MEC1308	MICOM_SMSC_MEC1308	
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	44	OF 60

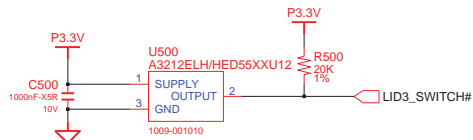
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# Micom Glue Logic

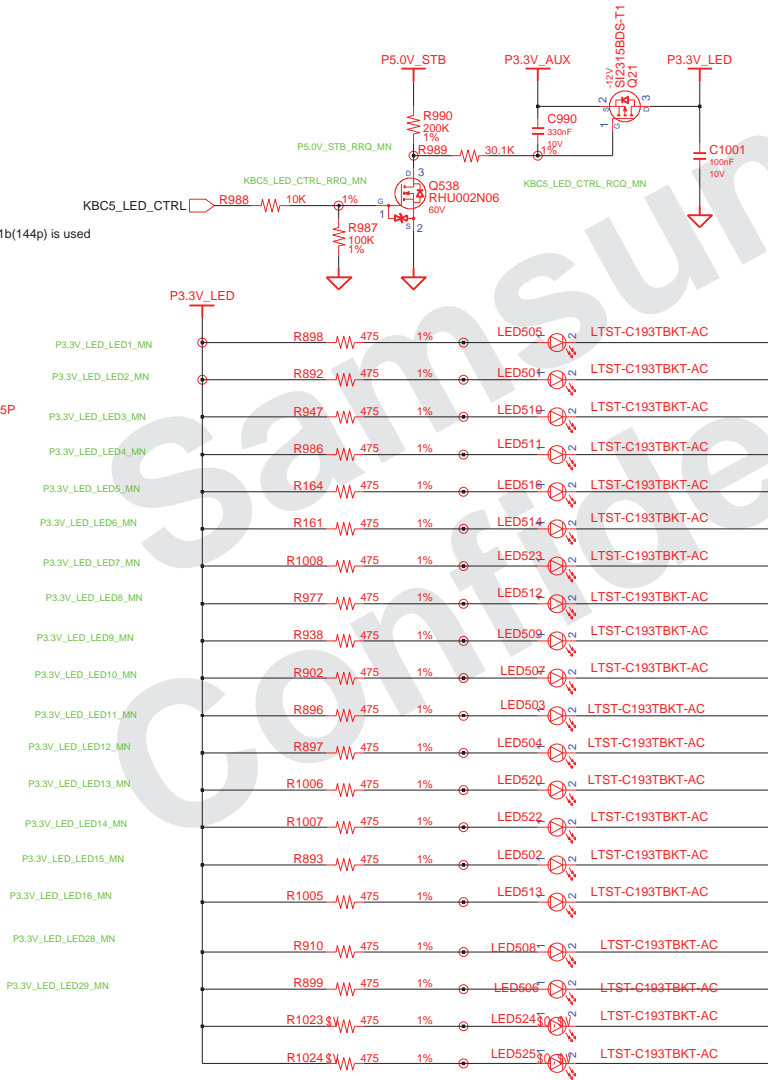
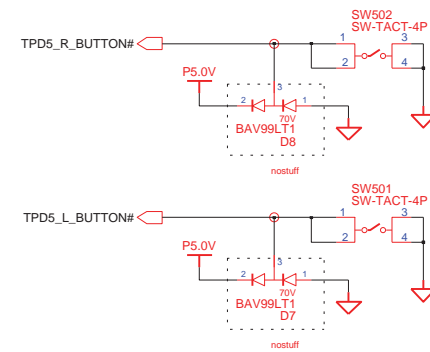
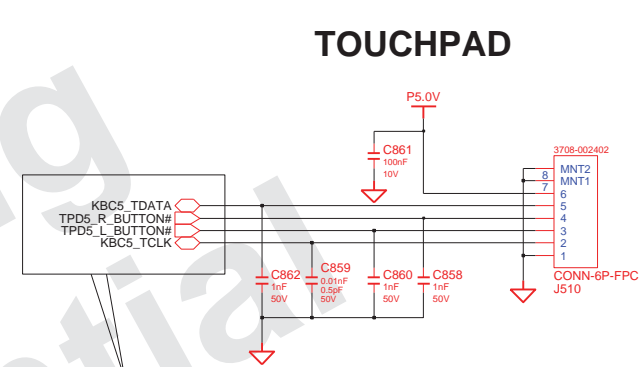
## KEYBOARD



## LID\_SWITCH



## TOUCHPAD

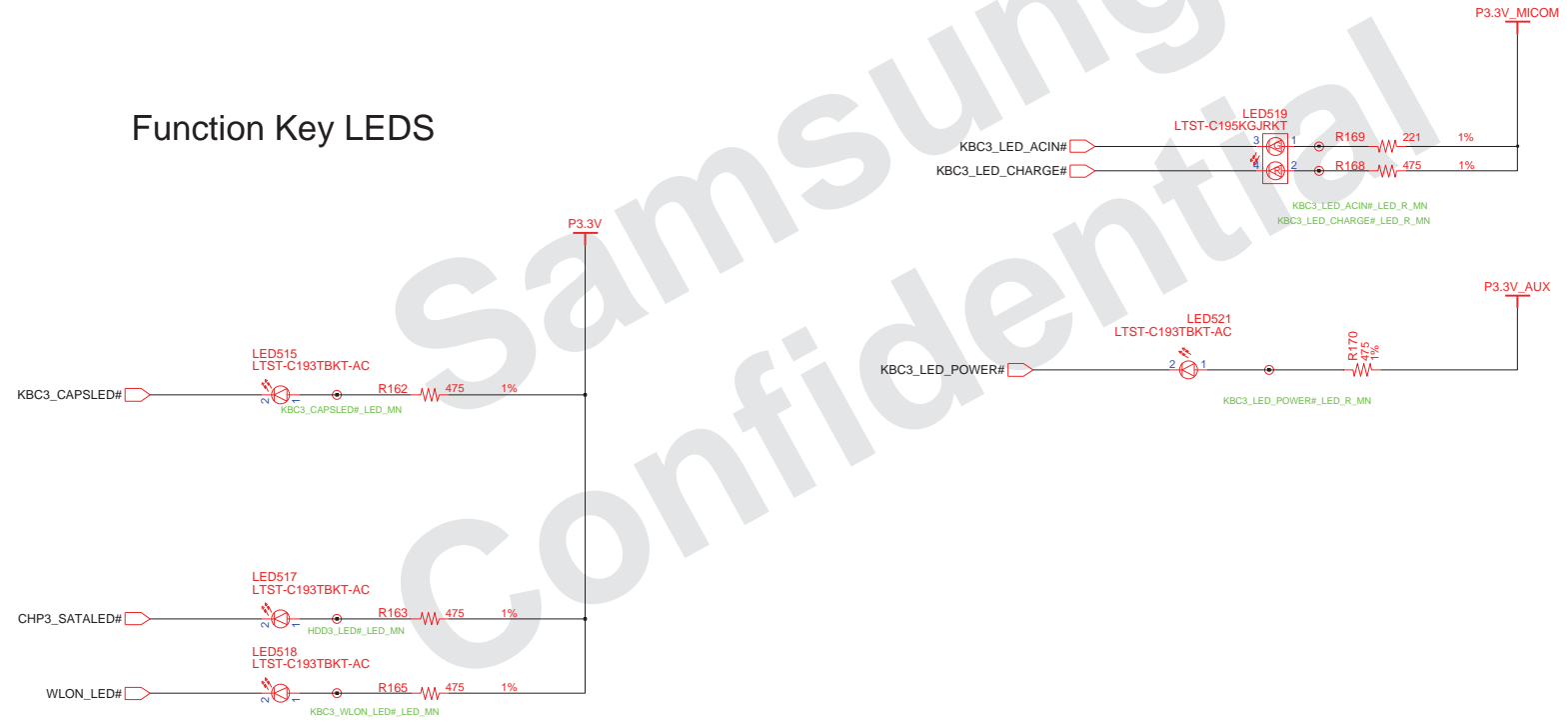


DESIGN	SUN XIAO,	DATE	6/27/2008	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	45	OF 60

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# LED SWITCH LOGIC

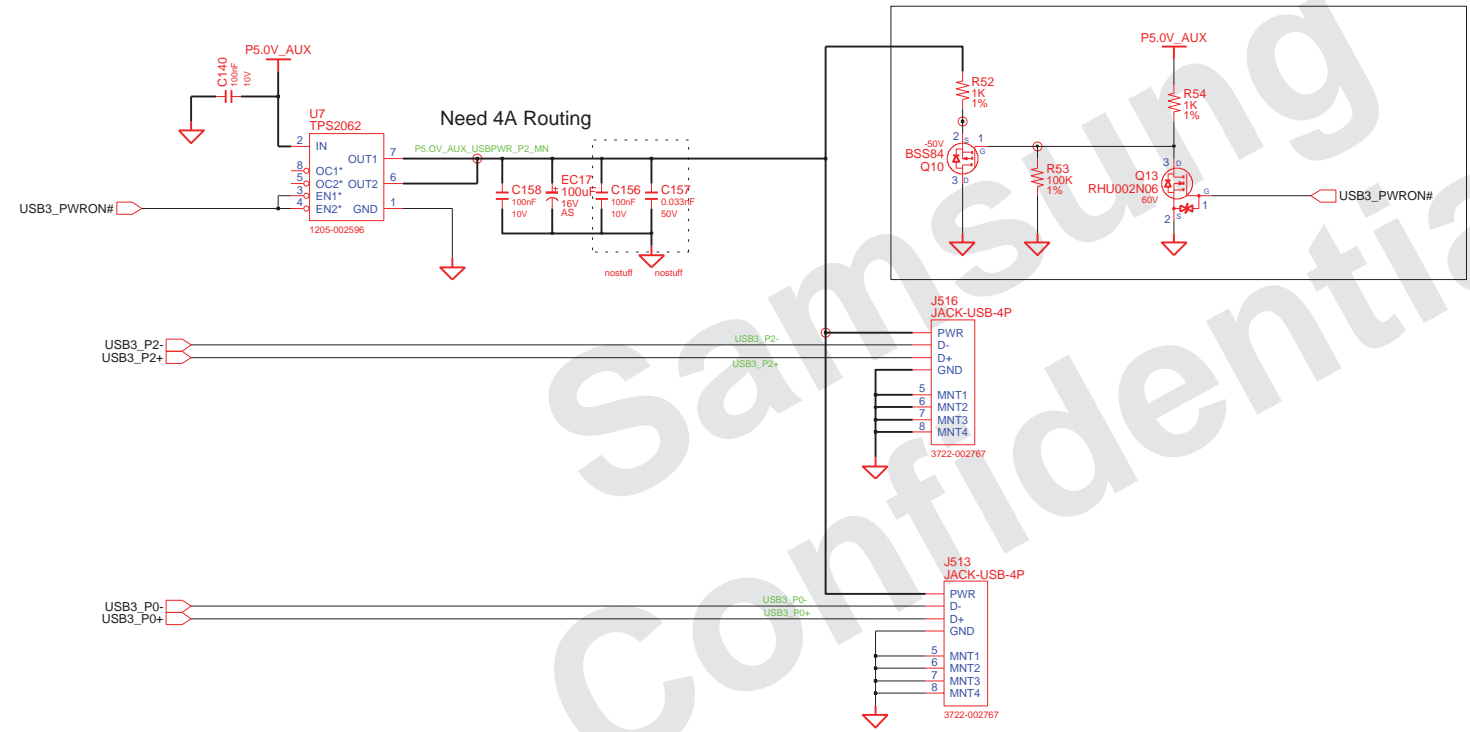
## Function Key LEDs



DRAWN	SUN XIAO,	DATE	8/12/2006	TITLE	Suzhou_L	SAMSUNG ELECTRONICS
CHECK	WU SHUANG,	REV. STEP	PR	LED_Switch		
APPROVAL	BC LEE,	REV	1.0	LED_Switch		PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			PAGE 46 OF 60

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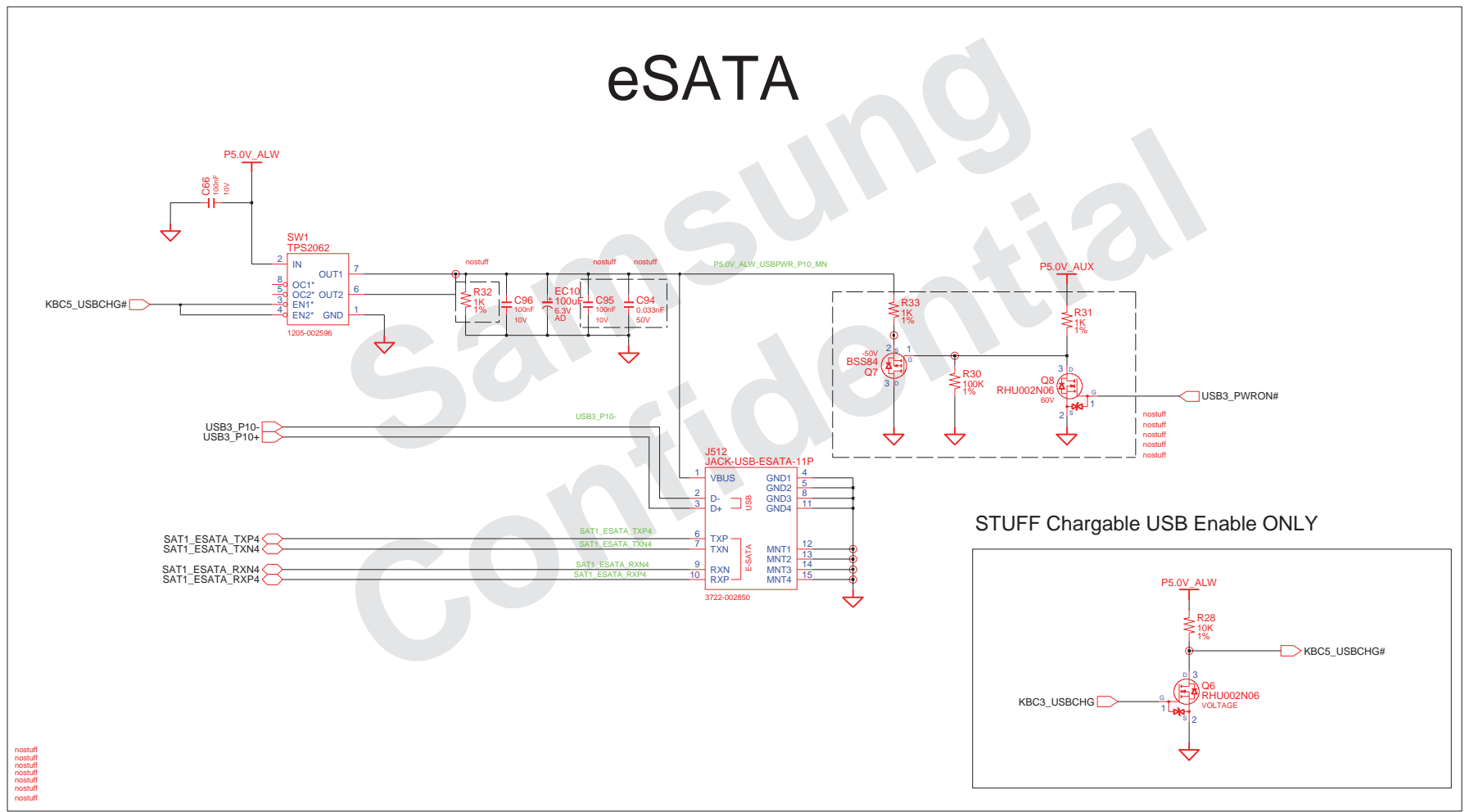
## 1/2 PORT USB CONNECTOR



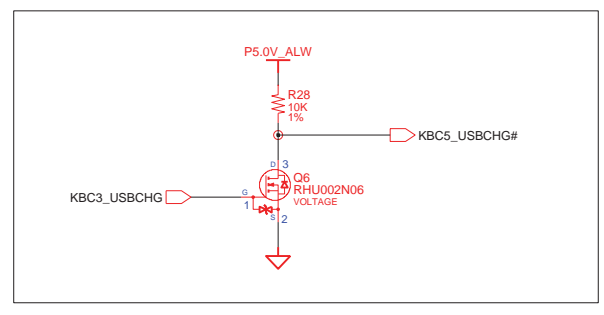
DESIGN	SUN XIAO,	DATE	6/6/2008	TITLE	Suzhou_L USB_CONN	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	47	OF 60

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# eSATA



STUFF Chargeable USB Enable ONLY



DESIGN	SUN XIAO,	DATE	8/18/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	ESATA		PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			PAGE 48 OF 60

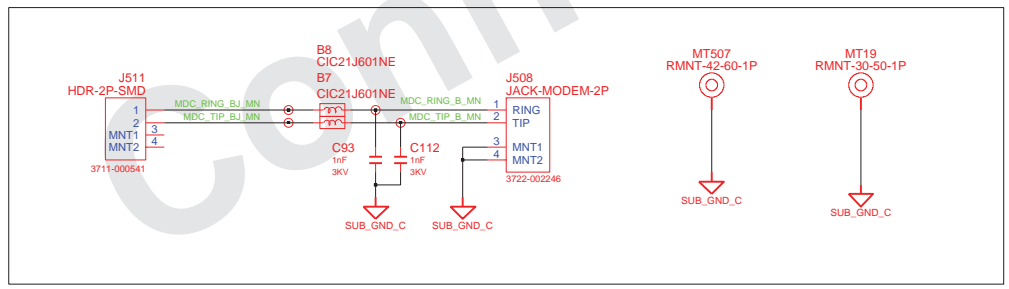
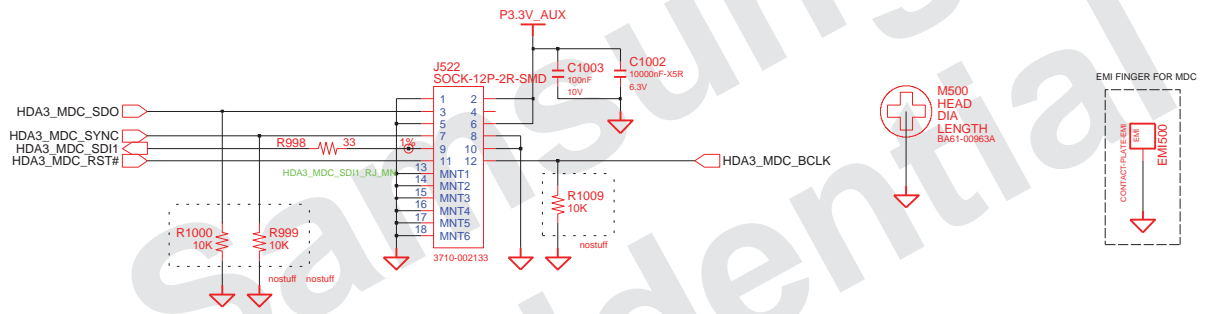
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# MDC

## MDC Connector



Factory Option

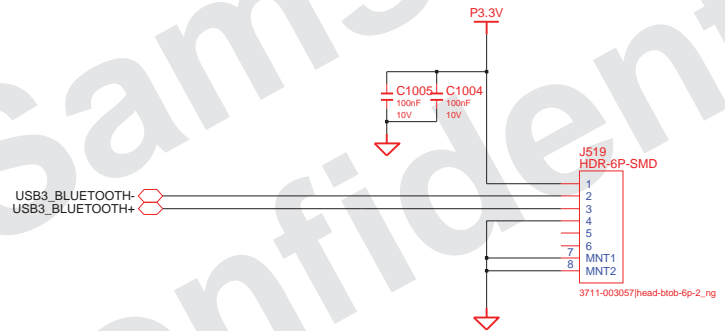
DESIGN	SUN XIAO,	DATE	8/18/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	HDA_MODEM		PART NO. BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			PAGE 49 OF 60

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### Bluetooth Interface

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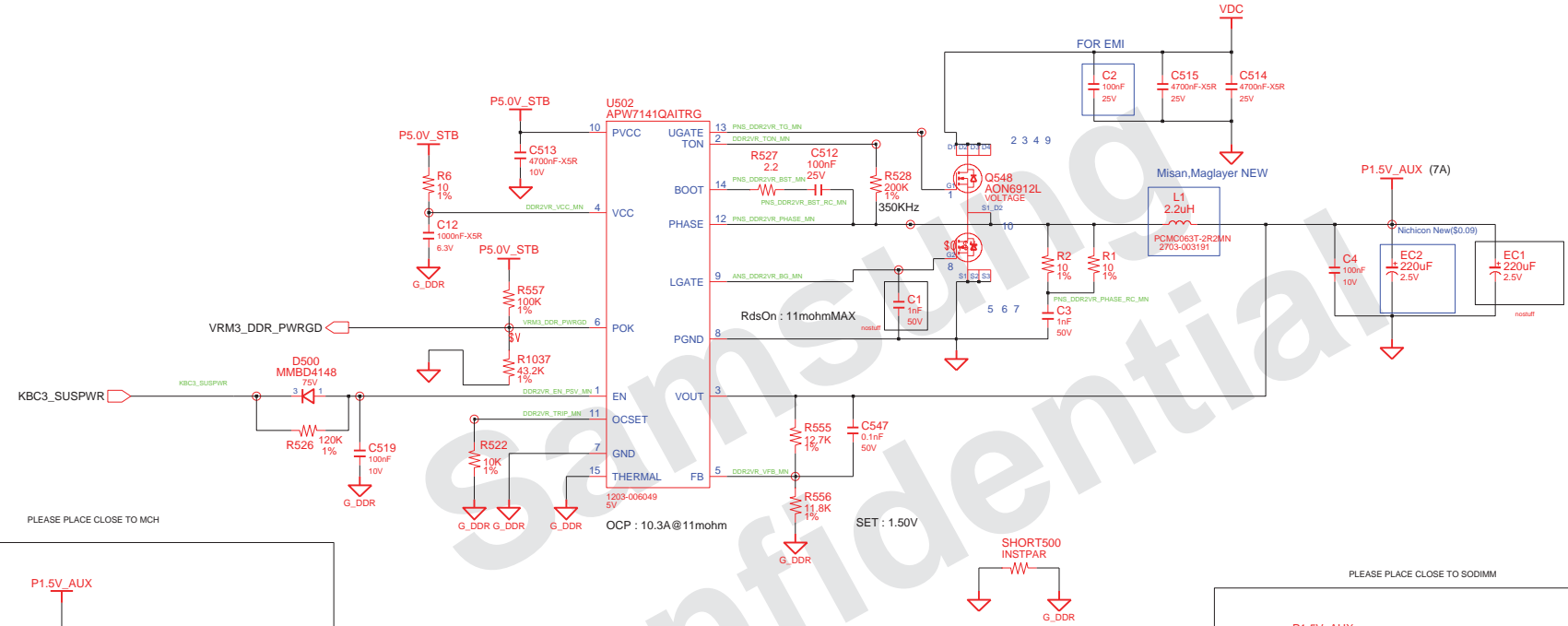
DESIGN	SUN XIAO,	DATE	6/6/2008	TITLE	Suzhou_L USB_DEVICES	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01215A
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			



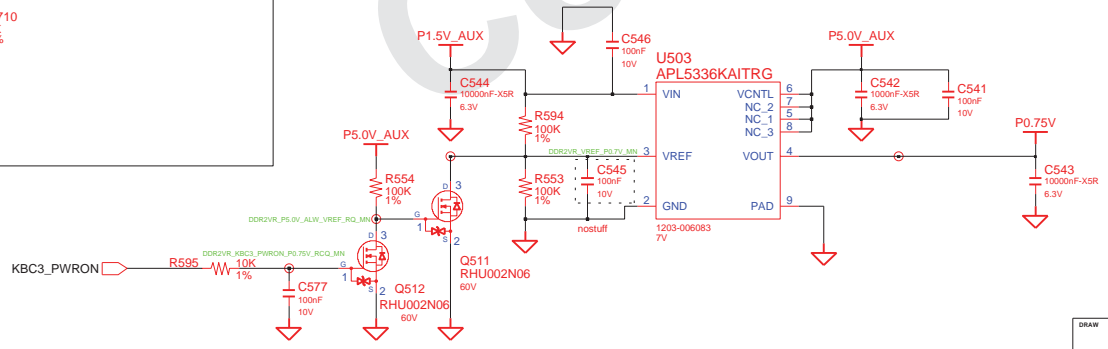


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## DDR3 Power



## DDR3 VTT(0.75V)



DRAW	SUN XIAO,	DATE	03/13/2009	TITLE	SuZhou_L	SAMSUNG ELECTRONICS
CHECK	WU SHUJIANG,	DEV. STEP	PR	PWR_MV_Memory_Rt8207	PART NO.	
APPROVAL	BC LEE,	REV	1.0	DDR3 POWER (P1.5V_AUX)	BA41-01215A	
MODULE CODE	undefined	LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	53	OF 60

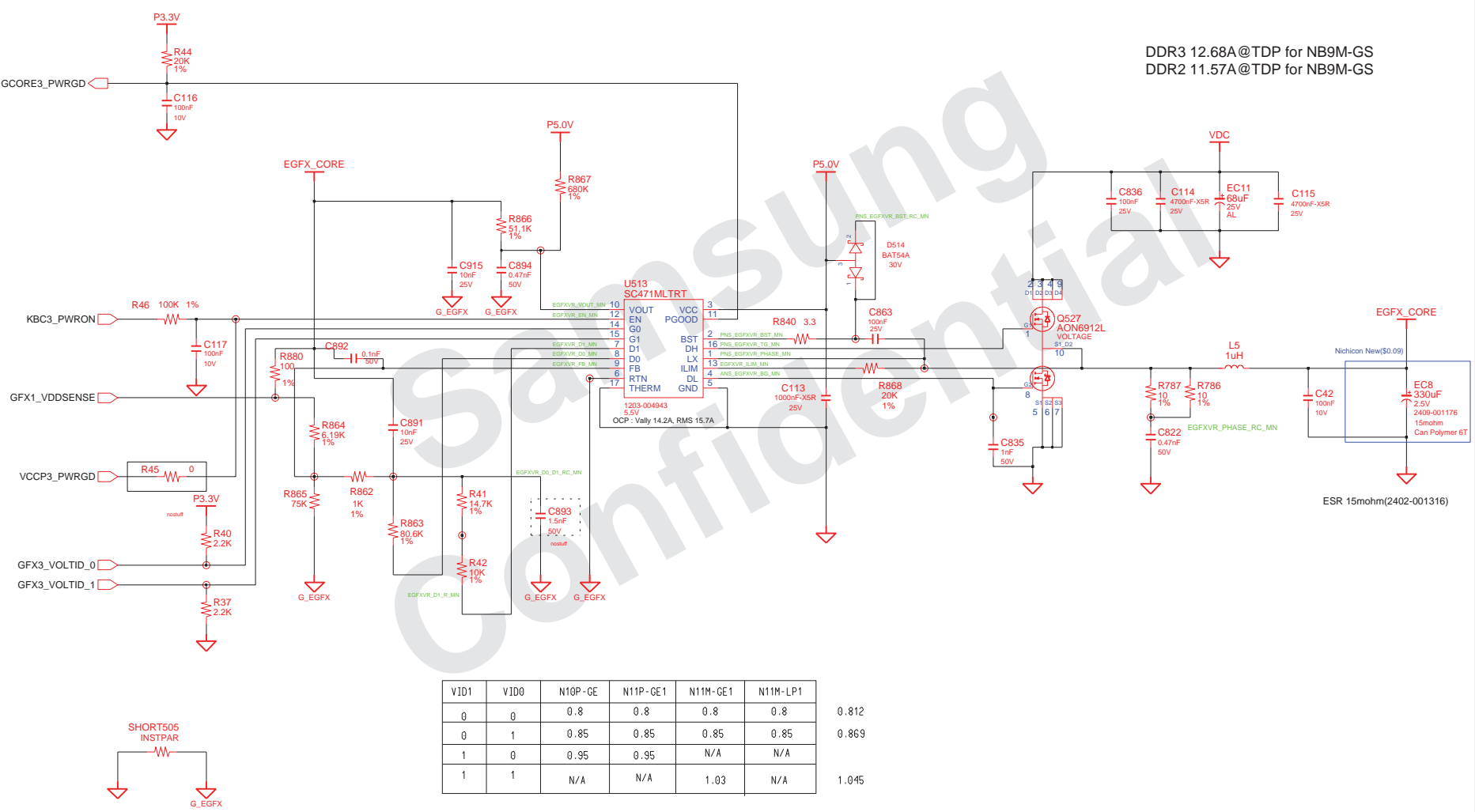
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# Graphic Core Power

DDR3 12.68A@TDP for NB9M-GS  
 DDR2 11.57A@TDP for NB9M-GS

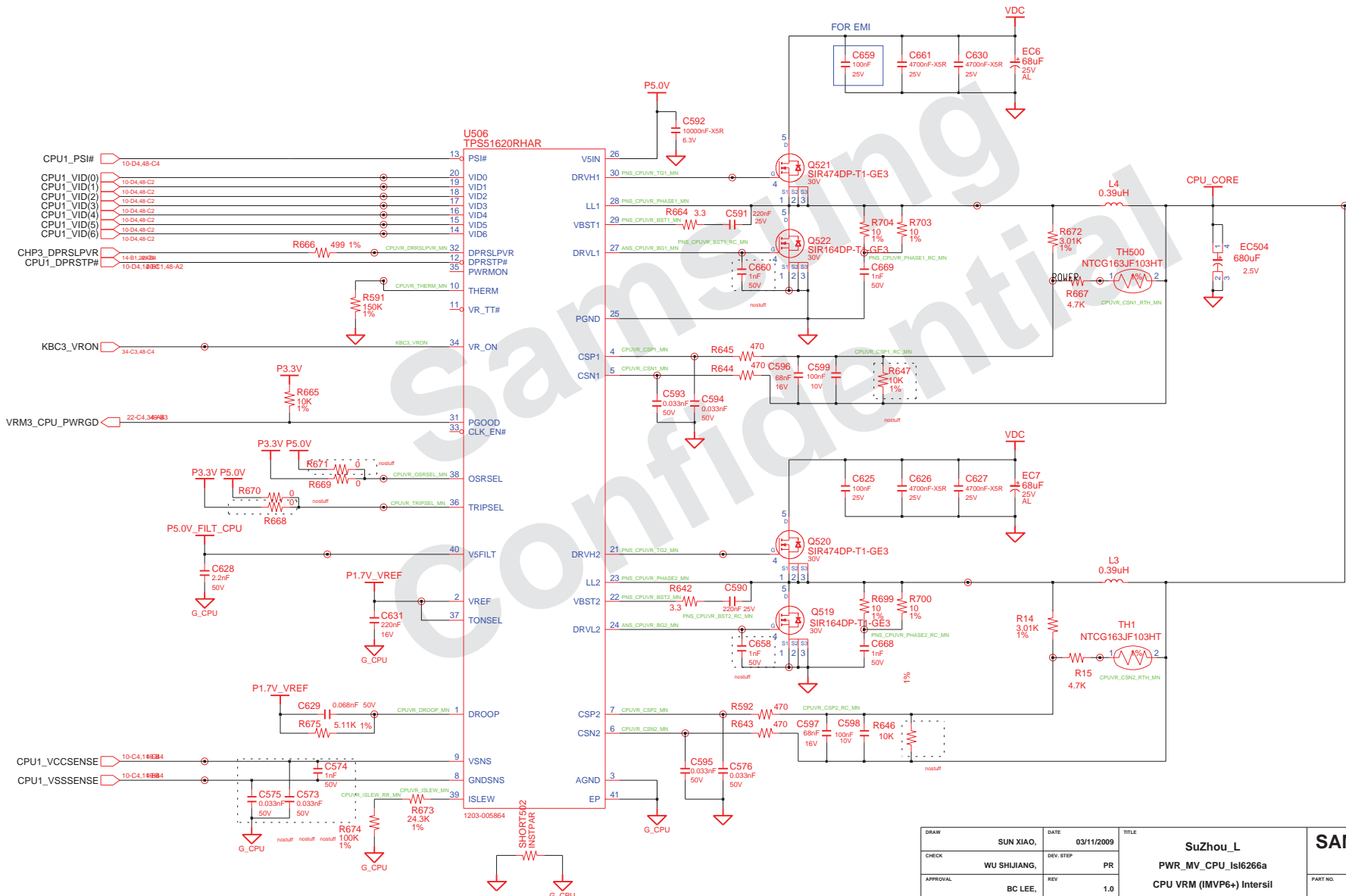


DRAW	SUN XIAO,	DATE	5/30/2009	TITLE	SuZhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHUIJIANG,	REV. STEP	PR	PWR GFX		
APPROVAL	BC LEE,	REV	1.0	GFX Power		PART NO.
MODULE CODE		LAST EDIT				BA41-01215A
				November 25, 2009 10:50:13 AM	PAGE	55 OF 60

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# CPU VRM [TI IMVP6+]



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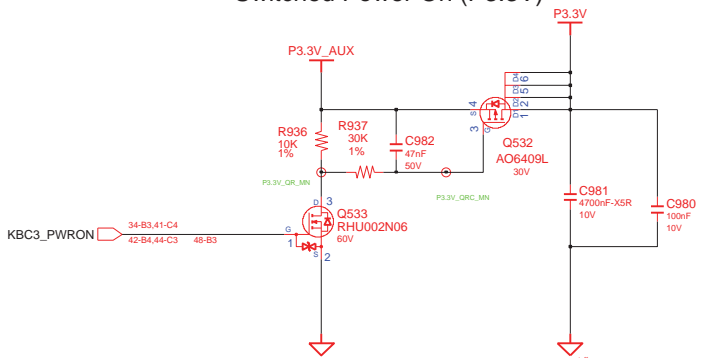
DRAW	SUN XIAO,	DATE	03/11/2009	TITLE	SuZhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHUJIANG,	DEV. STEP	PR	PWR_MV_CPU_Isi6266a	PART NO.	
APPROVAL	BC LEE,	REV	1.0	CPU VRM (IMVP6+) Intersil	BA41-01215A	
MODULE CODE	undefined	LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	56	OF 60



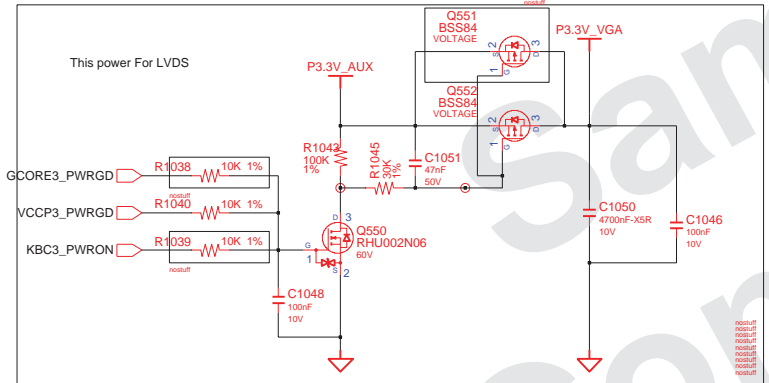
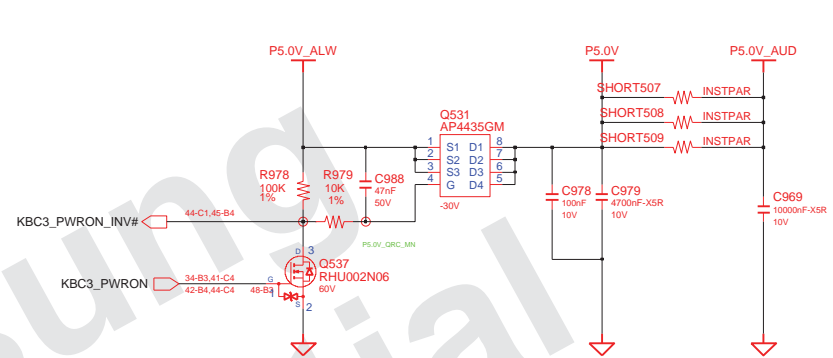
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# Switched Power

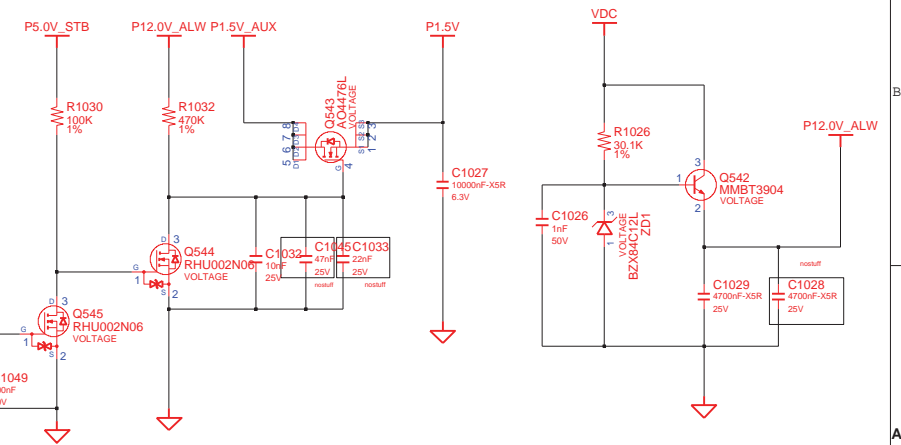
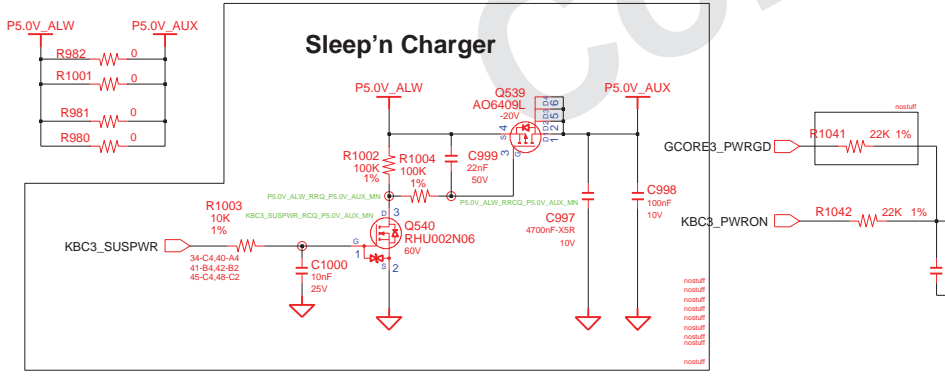
## Switched Power On (P3.3V)



## Switched Power On (P5.0V)



## Sleep'n Charger

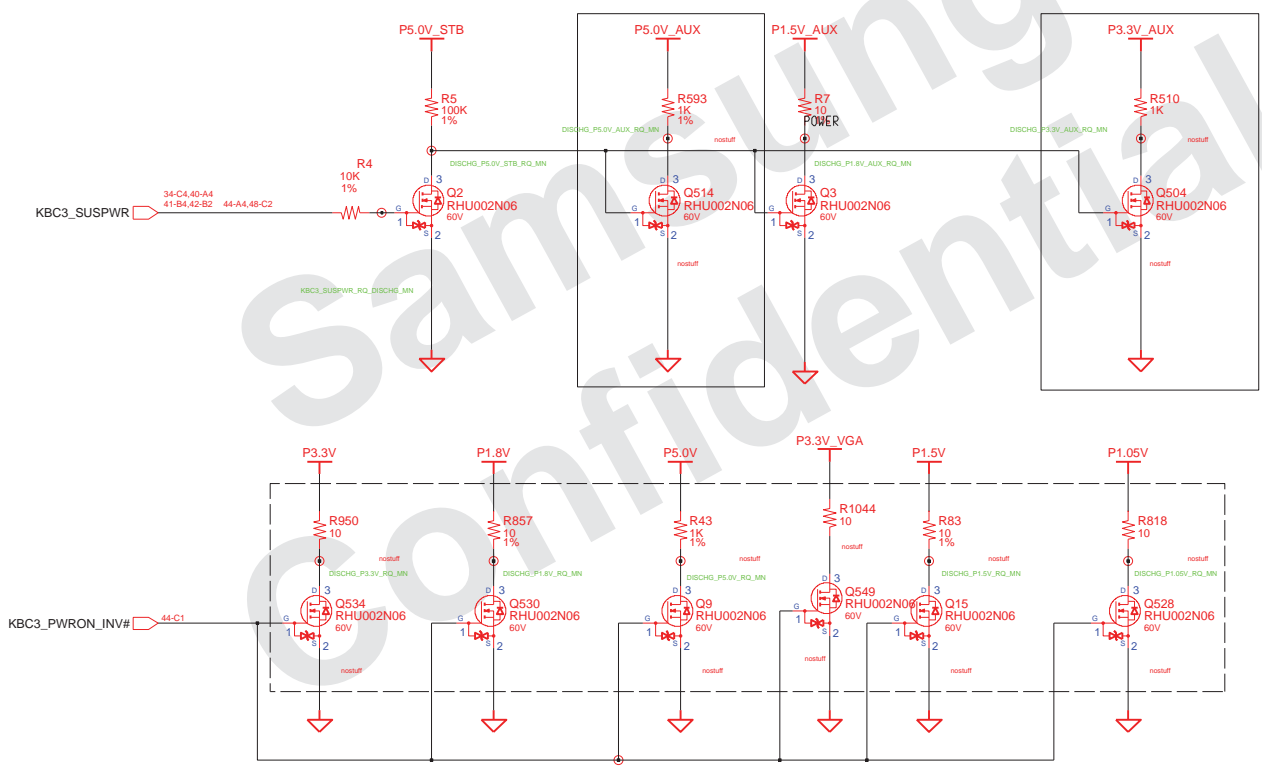


DRAW	SUN XIAO,	DATE	03/11/2009	TITLE	SuZhou_L	SAMSUNG ELECTRONICS
CHECK	WU SHUJIANG,	REV. STEP	PR	PWR_MV_Switched	PART NO.	
APPROVAL	BC LEE,	REV	1.0	SWITCHED POWER	BA41-01215A	
MODULE CODE		LAST EDIT		November 25, 2009 10:50:13 AM	PAGE	57 OF 60

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# POWER DISCHARGER

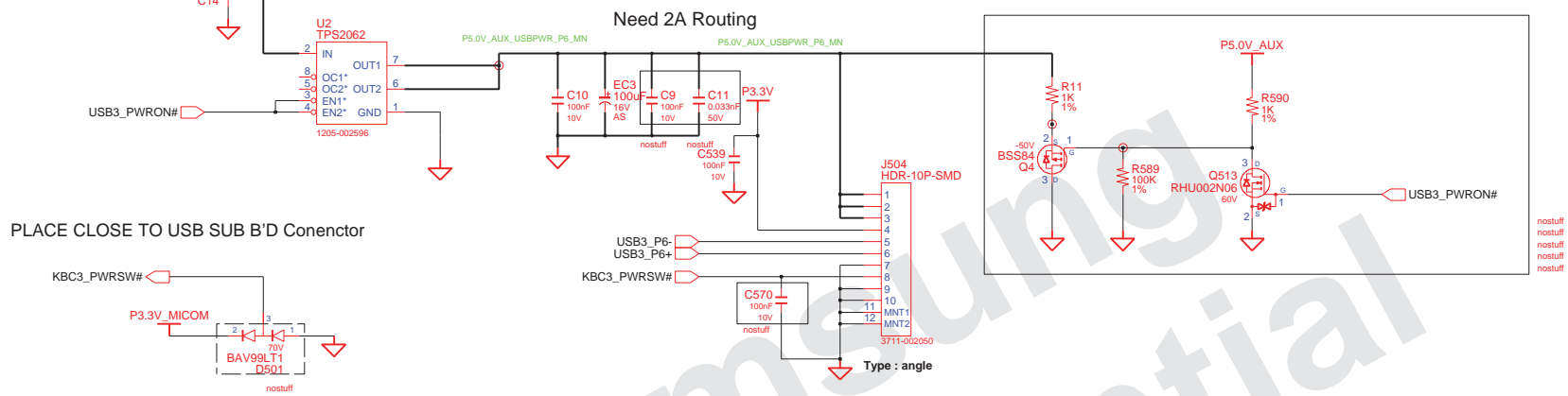


DRAW	SUN XIAO,	DATE	03/11/2009	TITLE	SuZhou_L	SAMSUNG ELECTRONICS
CHECK	WU SHUIJIANG,	DEV. STEP	PR	PWR_MV_DisCharger	PART NO.	
APPROVAL	BC LEE,	REV	1.0	DISCHARGING LOGIC	BA41-01215A	
MODULE CODE	undefined	LAST EDIT	November 25, 2009 10:50:13 AM	PAGE	58	OF 60

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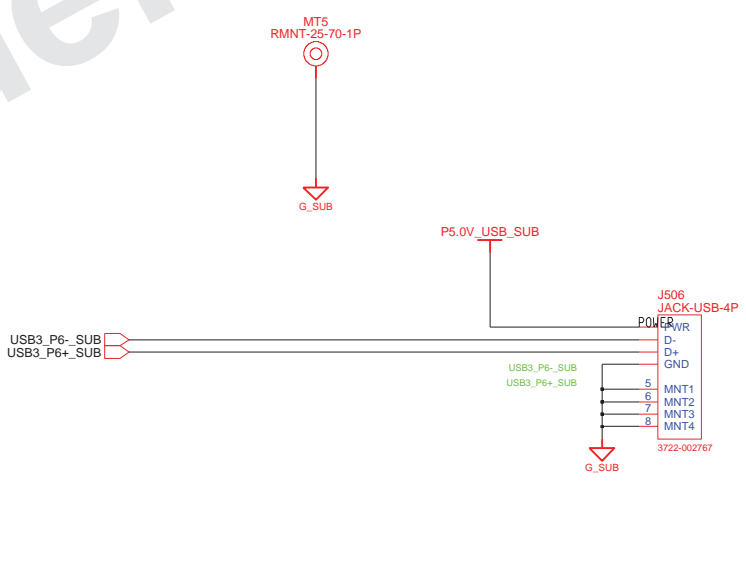
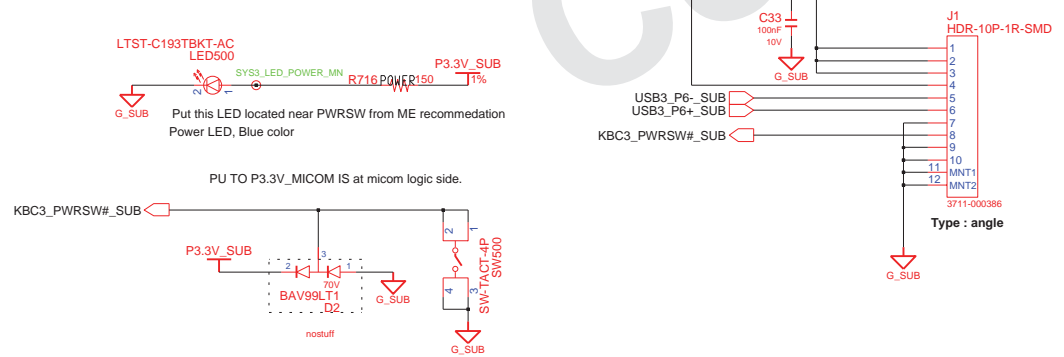
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# Main Board



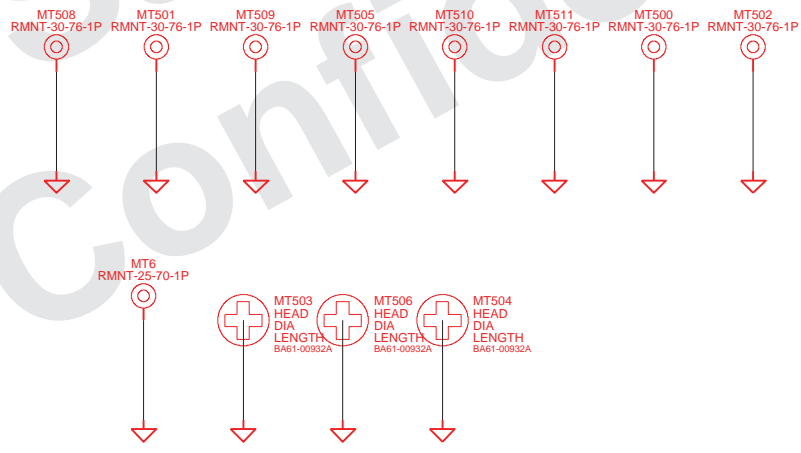
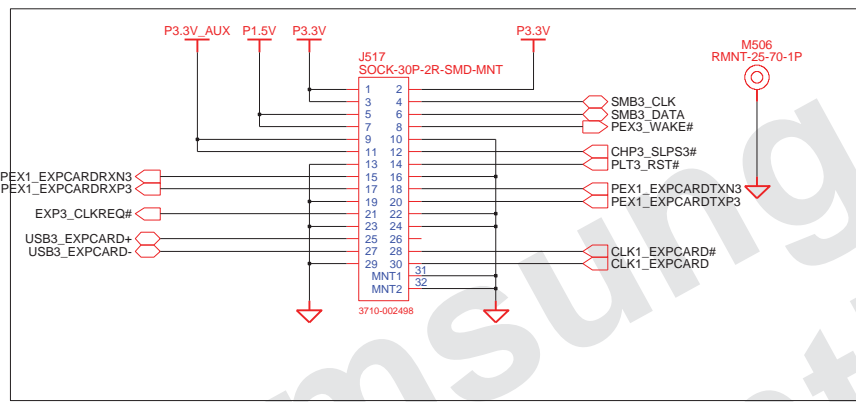
# SUB Board

## Power Switch Button



DESIGN	SUN XIAO,	DATE	8/18/2009	TITLE	Suzhou_L MAIN SUB BOARD	<b>SAMSUNG</b> ELECTRONICS PART NO. BA41-01215A
CHECK	WU SHIJIANG,	DEV. STEP	PR			
APPROVAL	BC LEE,	REV	1.0			
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM			

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DESIGN	SUN XIAO,	DATE	9/9/2009	TITLE	Suzhou_L	<b>SAMSUNG</b> ELECTRONICS
CHECK	WU SHIJIANG,	DEV. STEP	PR	MAIN		
APPROVAL	BC LEE,	REV	1.0	EXPRESS CARD	PART NO.	BA41-01215A
MODULE CODE		LAST EDIT	November 25, 2009 10:50:13 AM		PAGE	60 OF 60

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