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FIRENZE2-R

CPU : Intel Yonah/Merom (533/667MHz)
Chip Set : RS600ME & SB600
Remarks : Mobility Platform

Model Name : FIRENZE II R
PBA Name : MAIN
PCB Code : TPT : BA41-00714A
GCE : BA41-00715A
Dev. Step : MP (6-Layer)
Revision : 1.0
T.R. Date : 2006.01.11

DRAW	CHECK	APPROVAL
TERMI	HJ KIM	SJ PARK

■ *Owner : SEC Mobile R & D* *Signature :* *X*

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R COVER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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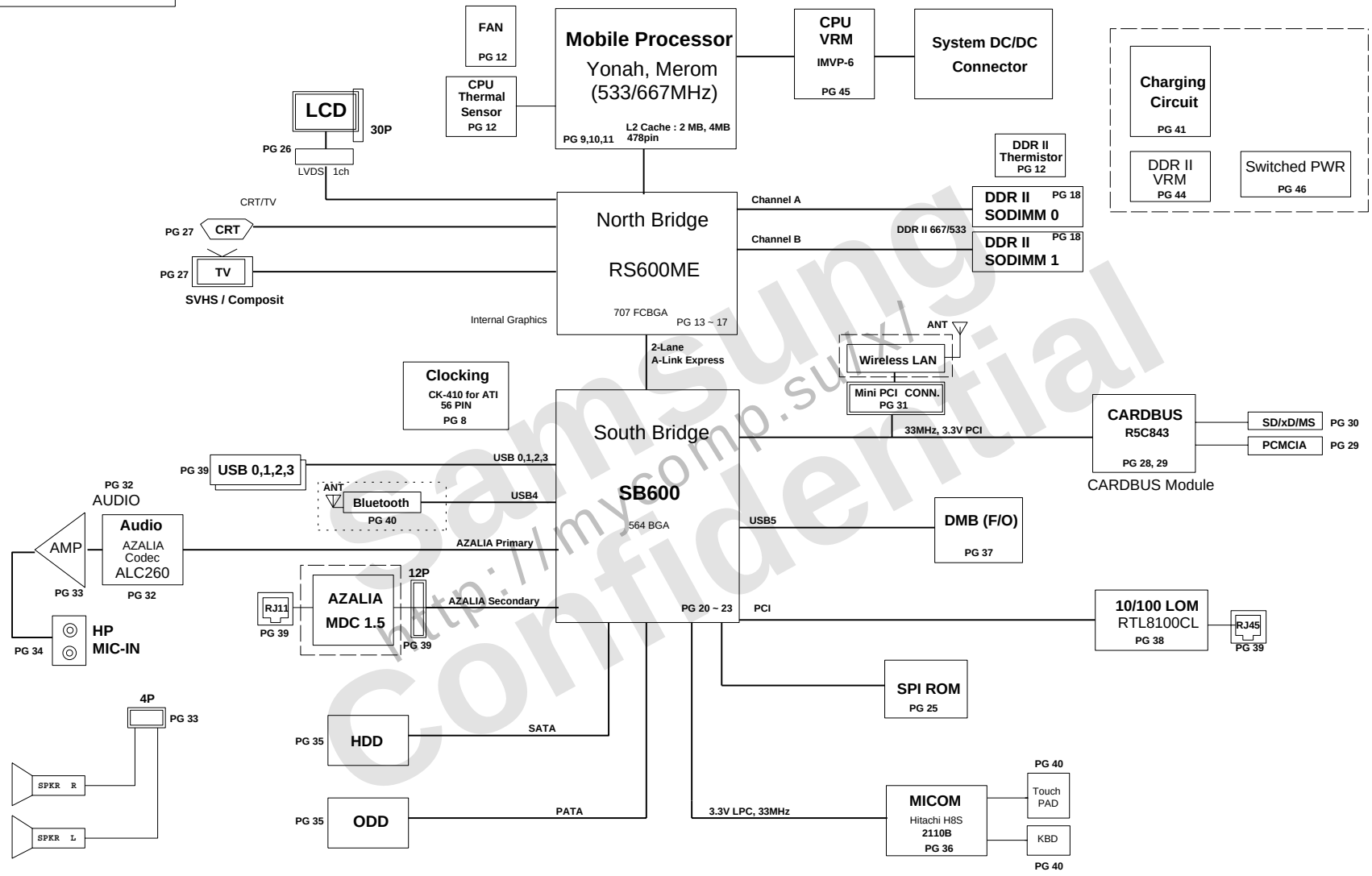

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN OPERATION BLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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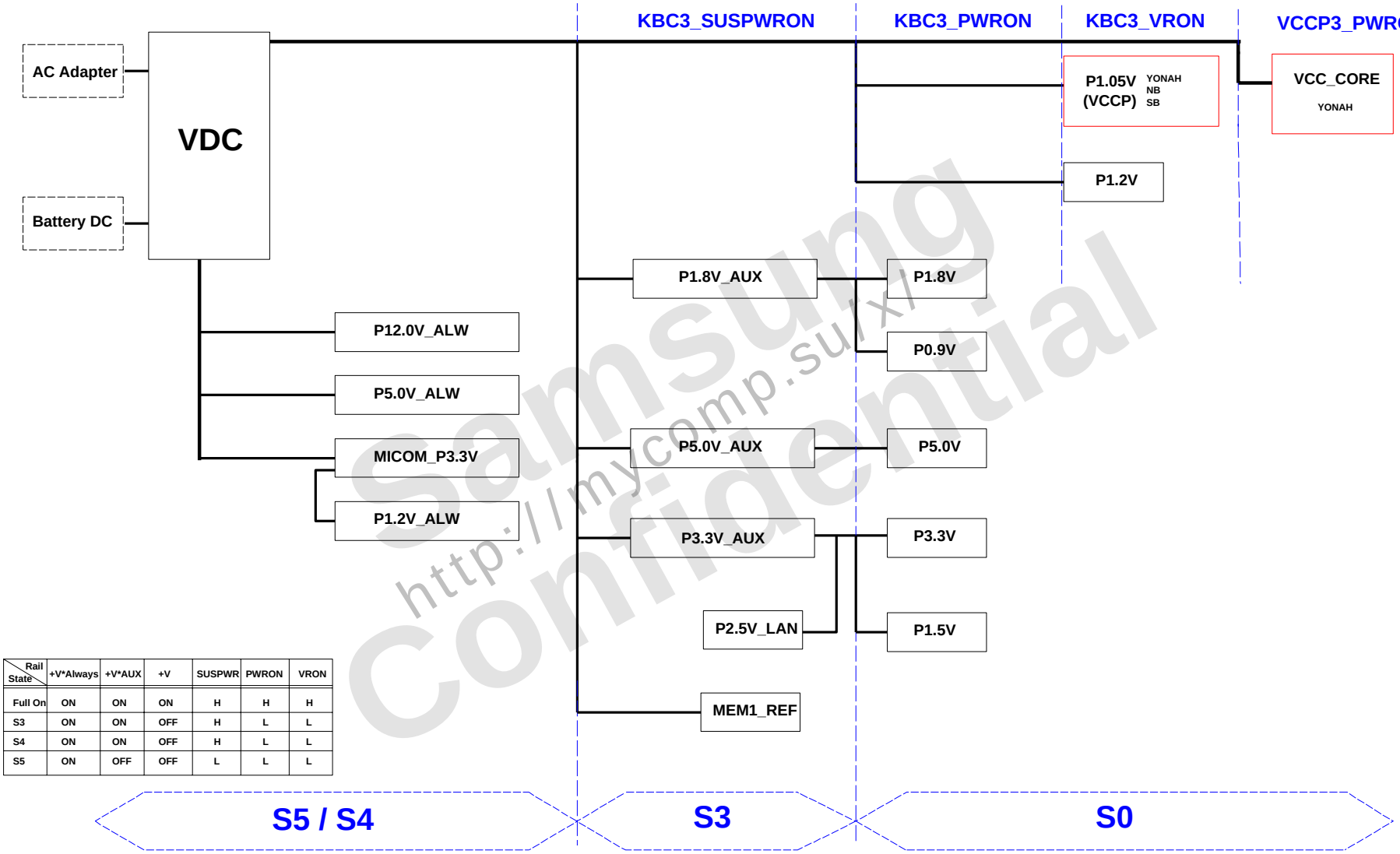
Power Diagram



Rail / State	+V*Always	+V*AUX	+V	SUSPWR	PWRON	VRON
Full On	ON	ON	ON	H	H	H
S3	ON	ON	OFF	H	L	L
S4	ON	ON	OFF	H	L	L
S5	ON	OFF	OFF	L	L	L

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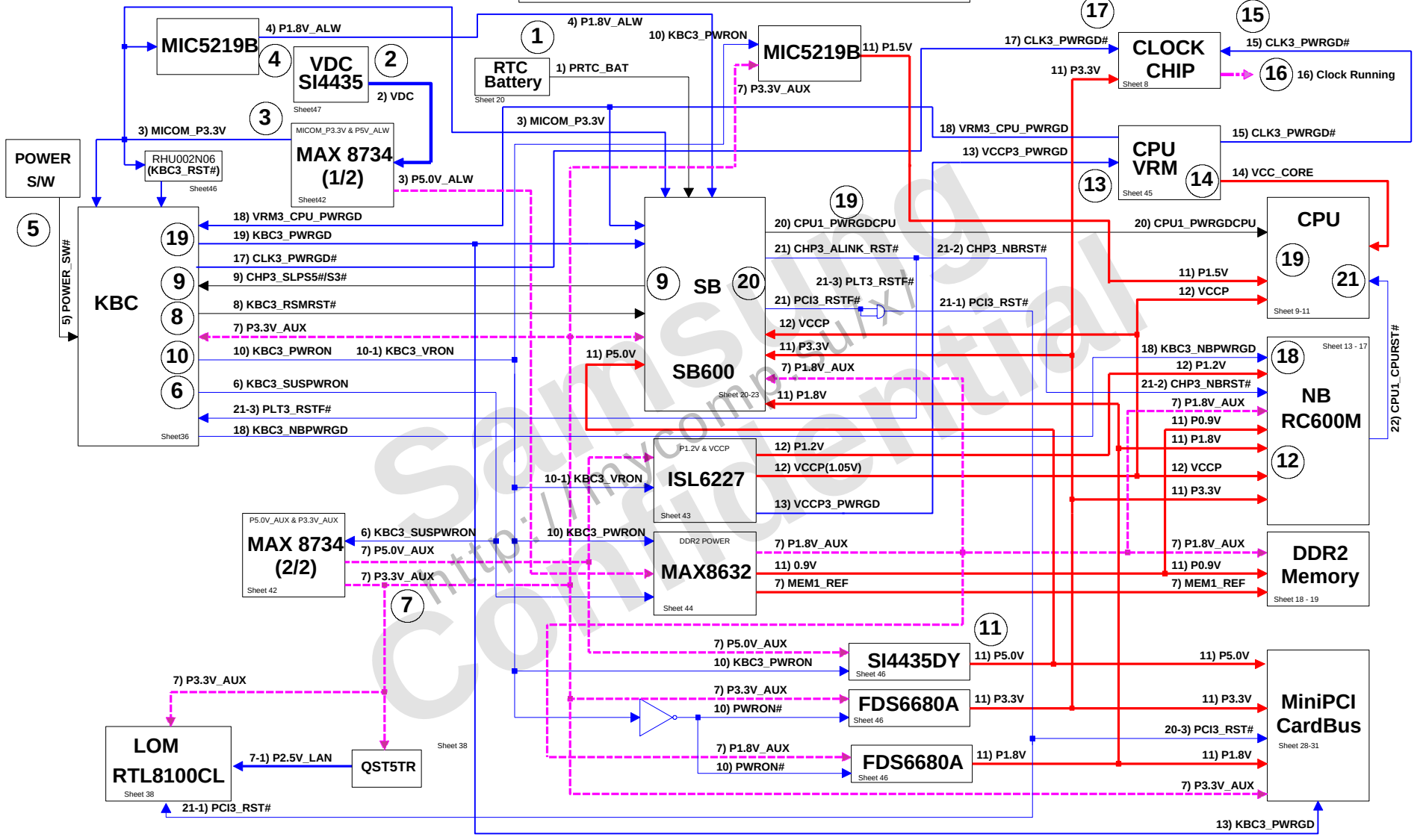
POWER SEQUENCE Rev. 0.1



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CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0	POWER SEQUENCE	PART NO.: BA41-00714A
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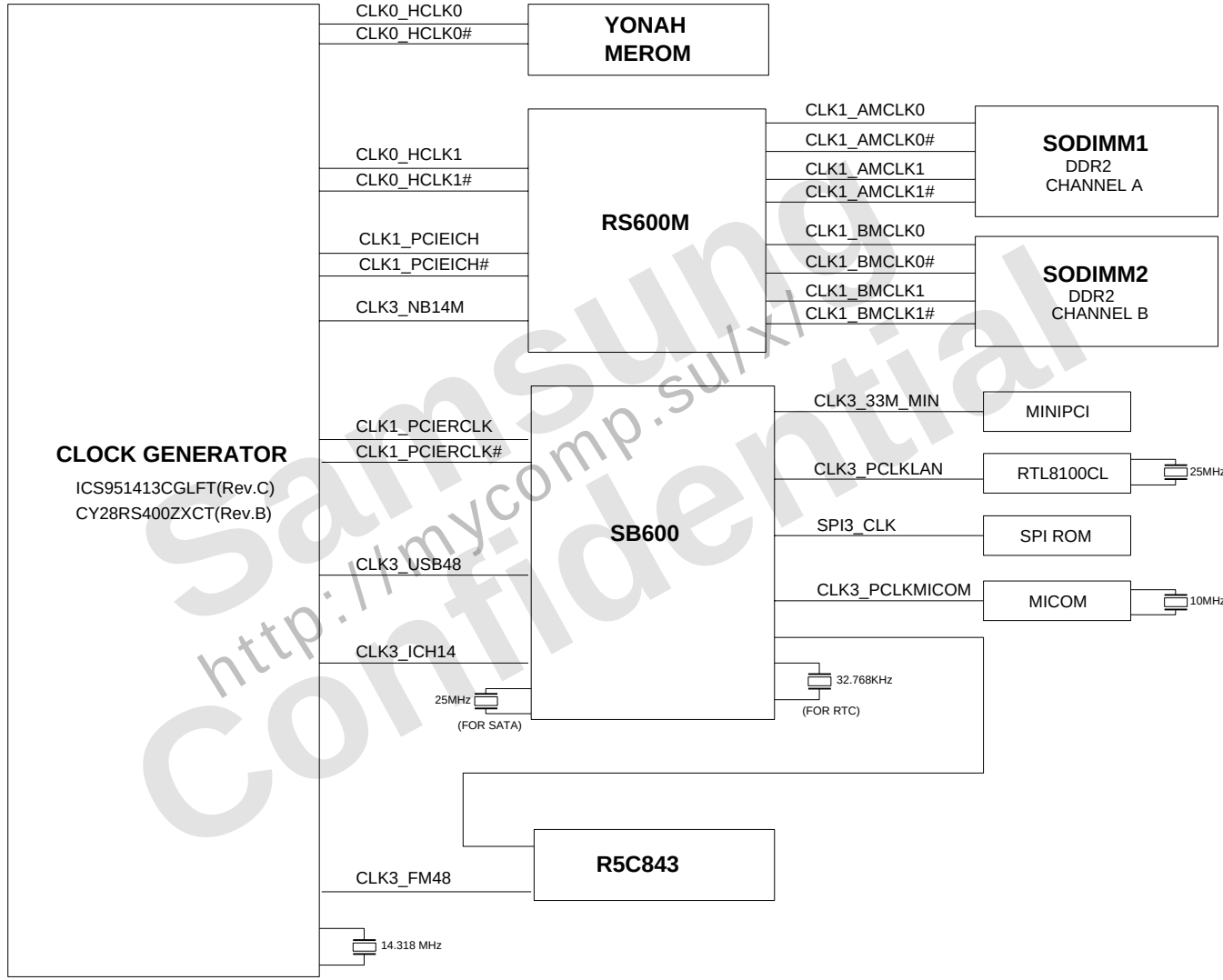

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R CLOCK DIAGRAM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	0	A, B, C
LAN	AD21	1	D
MINIPCI	AD23	2	A,B
USB	AD30(internal)	-	-
			-
			-
Hub to PCI	AD31(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	--
Internal MAC	AD31(internal)	-	-
AC Link	-	-	-

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core voltage for YONAH (0~1.5V)
VCCP	YONAH Processor System Bus(PSB) Termination (1.05V)
P0.9V	0.9V switched power rail (off in S3-S5)
P1.2V	1.2V switched power rail (off in S3-S5)
P1.5V	1.5V switched power rail (off in S3-S5)
P1.5V_AUX	1.5V power rail (off in S4-S5)
P1.8V	1.8V switched power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail(off in S4-S5)
P1.8V_ALWS	1.8V power rail (Always On)
P2.5V_LAN	2.5V power rail (off in S4-S5)
MICOM_P3.3V	3.3V always on power rail for MICOM
P3.3V	3.3V switched power rail (off in S3-S5)
P3.3V_AUX	3.3V power rail (off in S4-S5)
P5V	5.0V switched power rail (off in S3-S5)
P5V_AUX	5.0V power rail (off in S4-S5)
P5.0V_ALWS	5.0V power rail (Always On)
P12V_ALWS	12V power rail (Always On)

I2C / SMB Address

Devices	Address	Hex	Bus
SB600	Master	-	SMBUS Master
SODIMM0	1010 0100	A4h	-
SODIMM1	1010 0110	A6h	-
CK-410 (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable

USB PORT Assign

PORT NUMBER	ASSIGNED TO
0, 1	SYSTEM PORT A
2, 3	SYSTEM PORT B
4	BLUETOOTH
5	DMB

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	SB600	Real Time Clock
Crystal	25MHz	SB600	SATA
Crystal	10MHz	MICOM	H8S-2110B
Crystal	14.318MHz	CLOCK-Generator	CK-410M
Crystal	25MHz	LAN	LOM

CPU Core Voltage Table

IMVP-6

Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 1 1 1	0.4125 V
0 0 0 0 1 **1 1**	1.4125 V	0 1 0 1 1 **1 1**	0.9125 V	1 0 1 1 0 **0** 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 1 1 0 1	0.3375 V
0 0 0 1 1 0 **1**	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 1 1 1	0.2125 V
0 0 **1** 0 1 **1 1**	1.2125 V	0 1 **1** 1 1 **1 1**	0.7125 V	1 1 **0** 1 0 0 **0**	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 1 1 1	0.0125 V
0 **1** 0 0 **1 1** 1	1.0125 V	1 **0** 0 1 **1 1** 1	0.5125 V	1 **1** 1 1 0 **0** 0	0.0000 V
		1 **0** 1 0 **0 0** 0	0.5000 V	1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1	0.0000 V

Active	
DPRSLPVR	0
DPRSTP*	1
PSI2*	0 or 1

Deeper Slp	
DPRSLPVR	1
DPRSTP*	0
PSI2*	0 or 1

*"1111111" : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

System Power States

CHP3_SLPS1* S1, Powered-On-Suspend(POS) : In this state, all clocks(except the 32.768KHz clock) are stopped.
The system context is maintained in system DRAM. Power is maintained to PCI, the CPU, memory controller, memory, and all other criticial subsystems.
Note that this state does not preclude power being removed from non-essential devices, such as disk drives. During this state, CPU can be selected for either Deep Sleep or Deeper Sleep.
In Deeper Sleep, CPU voltage reduced in this state to reduce the leakage power.

CHP3_SLPS3* S3, Suspend-To-RAM(STR) : The system context is maintained in system DRAM, but power is shut off to non-critical circuits.
Memory is retained, and refreshes continue. All clocks stop except RTC clock.

CHP3_SLP4S* S4, Suspend-To-Disk(STD) : The Context of the system is maintained on the disk. All power is then shut off to the system except for the logic required to resume.
Externally appears same as S5, but may have different wake events.

CHP3_SLPS5* S5, Soft Off(SOFF) : System context is not maintained. All power is shut off except for the logic required to restart. A full boot is required when waking.

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CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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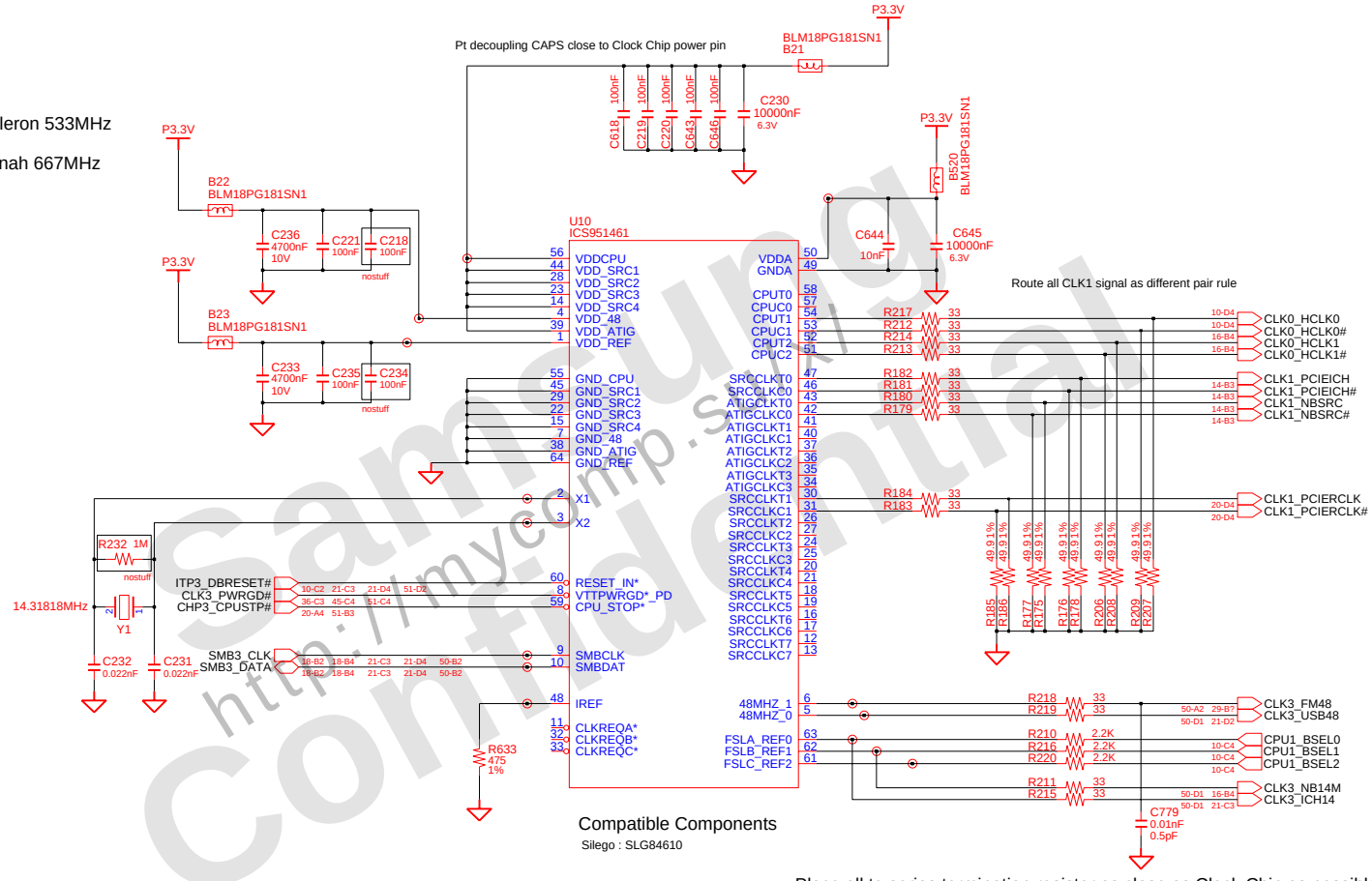
CPU	FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK	
	0	0	0	266 MHz	
	0	0	1	333 MHz	
	0	1	0	200 MHz	
	0	1	1	400 MHz	
	1	0	0	133 MHz	Celeron 533MHz
	1	0	1	100 MHz	
	1	1	0	166 MHz	Yonah 667MHz
	1	1	1	RSVD	



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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
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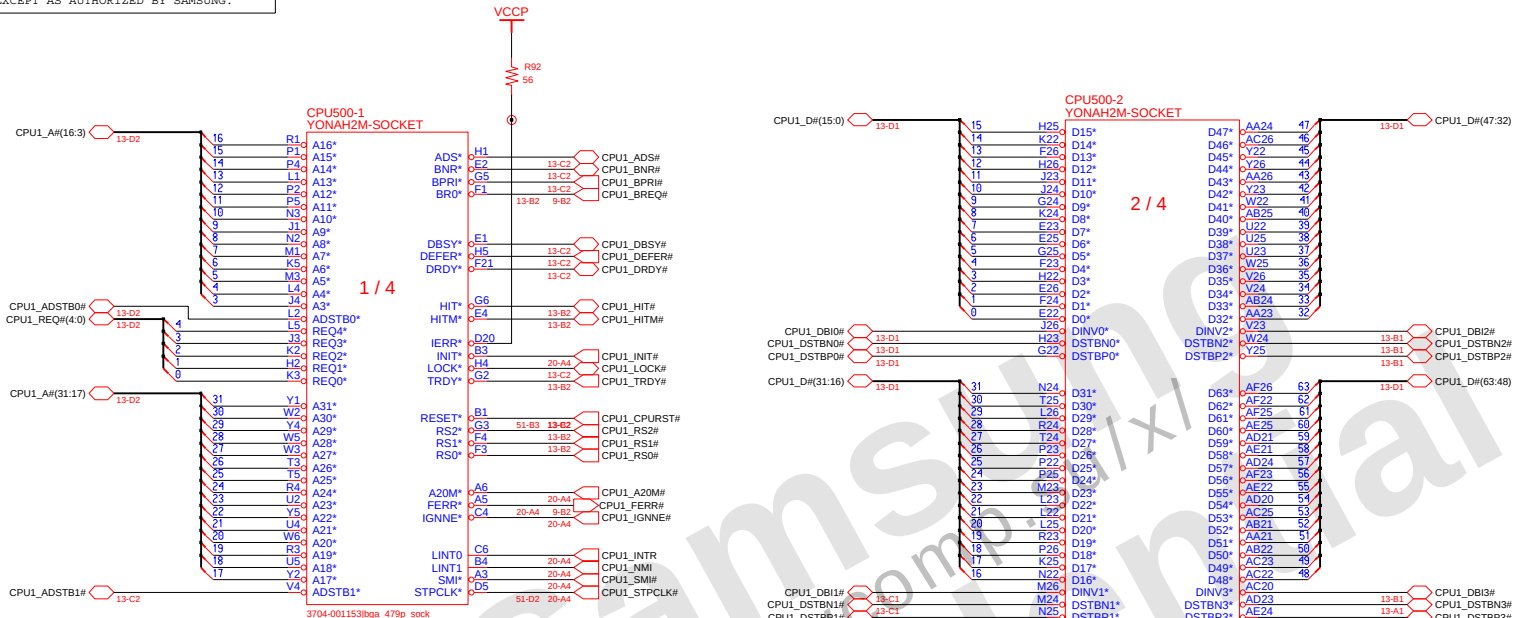

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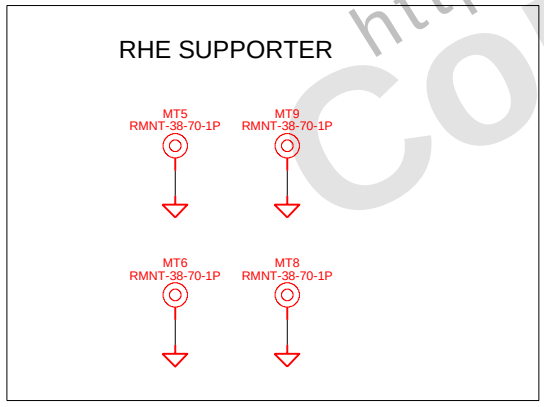
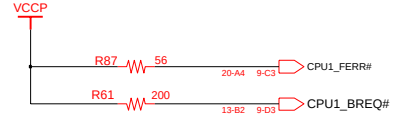
**NOTE

RHE SUPPORTER





DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN YONAH CPU (1/3)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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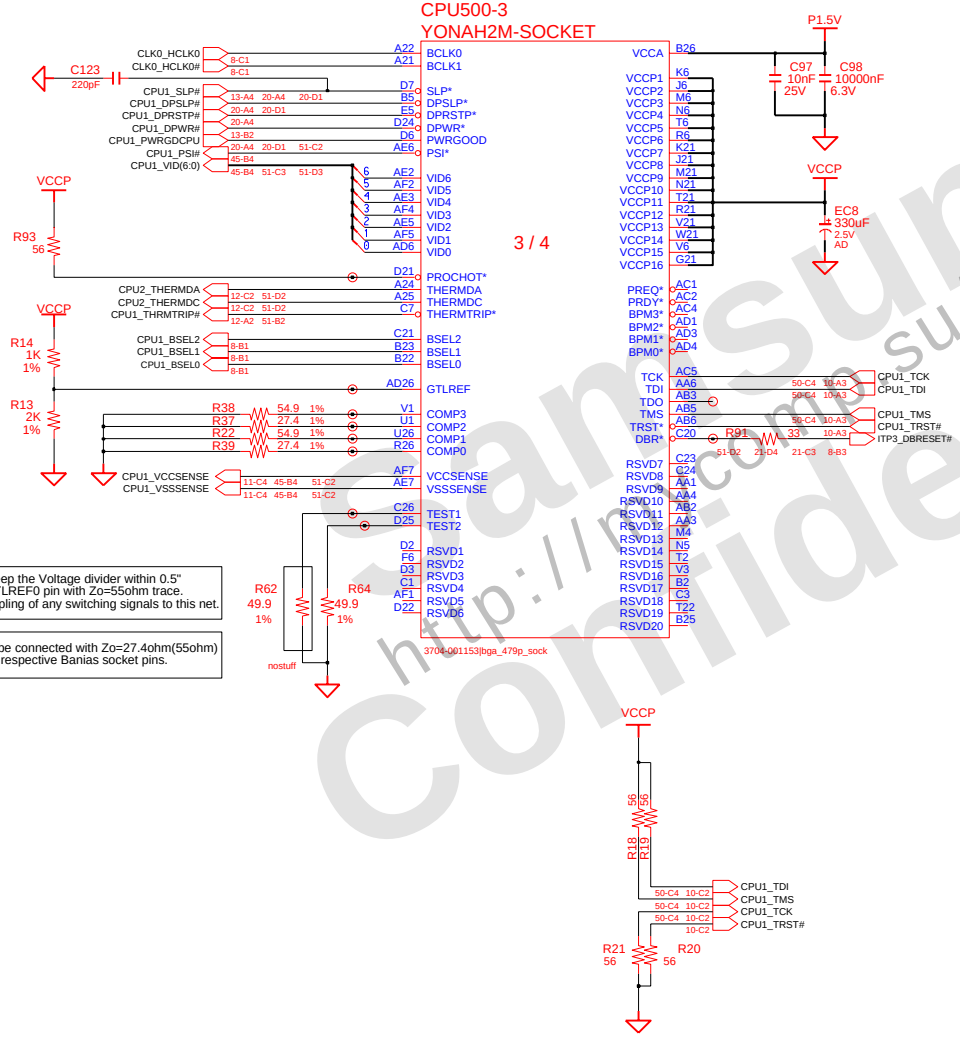

GTLREF : Keep the Voltage divider within 0.5" of the first GTLREF0 pin with Zo=55ohm trace. Minimize coupling of any switching signals to this net.

COMP0,2(COMP1,3) should be connected with Zo=27.4ohm(55ohm) trace shorter than 1/2" to their respective Banias socket pins.

CPU Core Voltage Table

IMVP-6

Active Mode VID(6:0)	Voltage	Active/Deeper Sleep Dual Mode Region VID(6:0)	Voltage	Deeper Sleep/Extended Deeper Sleep Dual Mode Region VID(6:0)	Voltage
0 0 0 0 0 0 0	1.5000 V	0 1 0 1 0 0 0	1.0000 V	1 0 1 0 0 0 1	0.4875 V
0 0 0 0 0 0 1	1.4875 V	0 1 0 1 0 0 1	0.9875 V	1 0 1 0 0 0 1 0	0.4750 V
0 0 0 0 0 1 0	1.4750 V	0 1 0 1 0 1 0	0.9750 V	1 0 1 0 0 0 1 1	0.4625 V
0 0 0 0 0 1 1	1.4625 V	0 1 0 1 0 1 1	0.9625 V	1 0 1 0 0 1 0 0	0.4500 V
0 0 0 0 1 0 0	1.4500 V	0 1 0 1 1 0 0	0.9500 V	1 0 1 0 0 1 0 1	0.4375 V
0 0 0 0 1 0 1	1.4375 V	0 1 0 1 1 0 1	0.9375 V	1 0 1 0 0 1 1 0	0.4250 V
0 0 0 0 1 1 0	1.4250 V	0 1 0 1 1 1 0	0.9250 V	1 0 1 0 0 1 1 1	0.4125 V
0 0 0 0 1 1 1	1.4125 V	0 1 0 1 1 1 1	0.9125 V	1 0 1 0 1 0 0 0	0.4000 V
0 0 0 1 0 0 0	1.4000 V	0 1 1 0 0 0 0	0.9000 V	1 0 1 0 1 0 0 1	0.3875 V
0 0 0 1 0 0 1	1.3875 V	0 1 1 0 0 0 1	0.8875 V	1 0 1 0 1 0 1 0	0.3750 V
0 0 0 1 0 1 0	1.3750 V	0 1 1 0 0 1 0	0.8750 V	1 0 1 0 1 0 1 1	0.3625 V
0 0 0 1 0 1 1	1.3625 V	0 1 1 0 0 1 1	0.8625 V	1 0 1 0 1 1 0 0	0.3500 V
0 0 0 1 1 0 0	1.3500 V	0 1 1 0 1 0 0	0.8500 V	1 0 1 0 1 1 0 1	0.3375 V
0 0 0 1 1 0 1	1.3375 V	0 1 1 0 1 0 1	0.8375 V	1 0 1 0 1 1 1 0	0.3250 V
0 0 0 1 1 1 0	1.3250 V	0 1 1 0 1 1 0	0.8250 V	1 0 1 0 1 1 1 1	0.3125 V
0 0 0 1 1 1 1	1.3125 V	0 1 1 0 1 1 1	0.8125 V	1 1 0 0 0 0 0 0	0.3000 V
0 0 1 0 0 0 0	1.3000 V	0 1 1 1 0 0 0	0.8000 V	1 1 0 0 0 0 0 1	0.2875 V
0 0 1 0 0 0 1	1.2875 V	0 1 1 1 0 0 1	0.7875 V	1 1 0 0 0 0 1 0	0.2750 V
0 0 1 0 0 1 0	1.2750 V	0 1 1 1 0 1 0	0.7750 V	1 1 0 0 0 0 1 1	0.2625 V
0 0 1 0 0 1 1	1.2625 V	0 1 1 1 0 1 1	0.7625 V	1 1 0 0 0 1 0 0	0.2500 V
0 0 1 0 1 0 0	1.2500 V	0 1 1 1 1 0 0	0.7500 V	1 1 0 0 0 1 0 1	0.2375 V
0 0 1 0 1 0 1	1.2375 V	0 1 1 1 1 0 1	0.7375 V	1 1 0 0 0 1 1 0	0.2250 V
0 0 1 0 1 1 0	1.2250 V	0 1 1 1 1 1 0	0.7250 V	1 1 0 0 0 1 1 1	0.2125 V
0 0 1 0 1 1 1	1.2125 V	0 1 1 1 1 1 1	0.7125 V	1 1 0 0 1 0 0 0	0.2000 V
0 0 1 1 0 0 0	1.2000 V	1 0 0 0 0 0 0	0.7000 V	1 1 0 0 1 0 0 1	0.1875 V
0 0 1 1 0 0 1	1.1875 V	1 0 0 0 0 0 1	0.6875 V	1 1 0 0 1 0 1 0	0.1750 V
0 0 1 1 0 1 0	1.1750 V	1 0 0 0 0 1 0	0.6750 V	1 1 0 0 1 0 1 1	0.1625 V
0 0 1 1 0 1 1	1.1625 V	1 0 0 0 0 1 1	0.6625 V	1 1 0 0 1 1 0 0	0.1500 V
0 0 1 1 1 0 0	1.1500 V	1 0 0 0 1 0 0	0.6500 V	1 1 0 0 1 1 0 1	0.1375 V
0 0 1 1 1 0 1	1.1375 V	1 0 0 0 1 0 1	0.6375 V	1 1 0 0 1 1 1 0	0.1250 V
0 0 1 1 1 1 0	1.1250 V	1 0 0 0 1 1 0	0.6250 V	1 1 0 0 1 1 1 1	0.1125 V
0 0 1 1 1 1 1	1.1125 V	1 0 0 0 1 1 1	0.6125 V	1 1 1 0 0 0 0 0	0.1000 V
0 1 0 0 0 0 0	1.1000 V	1 0 0 1 0 0 0	0.6000 V	1 1 1 0 0 0 0 1	0.0875 V
0 1 0 0 0 0 1	1.0875 V	1 0 0 1 0 0 1	0.5875 V	1 1 1 0 0 0 1 0	0.0750 V
0 1 0 0 0 1 0	1.0750 V	1 0 0 1 0 1 0	0.5750 V	1 1 1 0 0 0 1 1	0.0625 V
0 1 0 0 0 1 1	1.0625 V	1 0 0 1 0 1 1	0.5625 V	1 1 1 0 0 1 0 0	0.0500 V
0 1 0 0 1 0 0	1.0500 V	1 0 0 1 1 0 0	0.5500 V	1 1 1 0 0 1 0 1	0.0375 V
0 1 0 0 1 0 1	1.0375 V	1 0 0 1 1 0 1	0.5375 V	1 1 1 0 0 1 1 0	0.0250 V
0 1 0 0 1 1 0	1.0250 V	1 0 0 1 1 1 0	0.5250 V	1 1 1 0 0 1 1 1	0.0125 V
0 1 0 0 1 1 1	1.0125 V	1 0 0 1 1 1 1	0.5125 V	1 1 1 1 0 0 0 0	0.0000 V
		1 0 1 0 0 0 0	0.5000 V	1 1 1 1 0 0 0 1	0.0000 V
				1 1 1 1 0 0 1 0	0.0000 V
				1 1 1 1 0 0 1 1	0.0000 V
				1 1 1 1 0 1 0 0	0.0000 V
				1 1 1 1 0 1 0 1	0.0000 V
				1 1 1 1 0 1 1 0	0.0000 V
				1 1 1 1 0 1 1 1	0.0000 V
				1 1 1 1 1 0 0 0	0.0000 V
				1 1 1 1 1 0 0 1	0.0000 V
				1 1 1 1 1 0 1 0	0.0000 V
				1 1 1 1 1 0 1 1	0.0000 V
				1 1 1 1 1 1 0 0	0.0000 V
				1 1 1 1 1 1 0 1	0.0000 V
				1 1 1 1 1 1 1 0	0.0000 V
				1 1 1 1 1 1 1 1	0.0000 V

Active	
DPRSLPVR	0
DPRSTP*	1
PSI2*	0 or 1

Deeper Slp	
DPRSLPVR	1
DPRSTP*	0
PSI2*	0 or 1

*"1111111" : 0V power good asserted.

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN YONAH CPU(2/3)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 10 OF 52	

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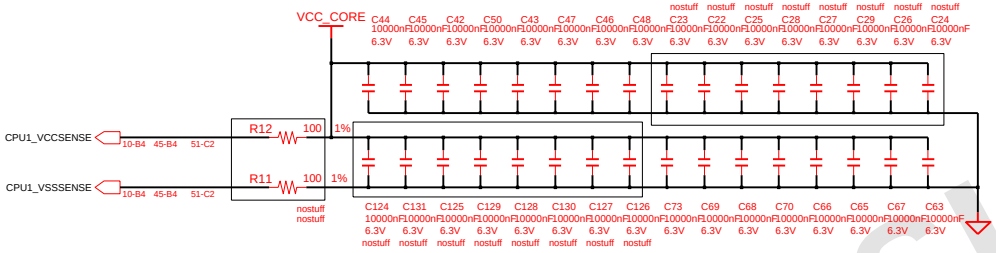

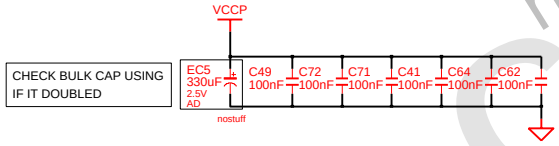

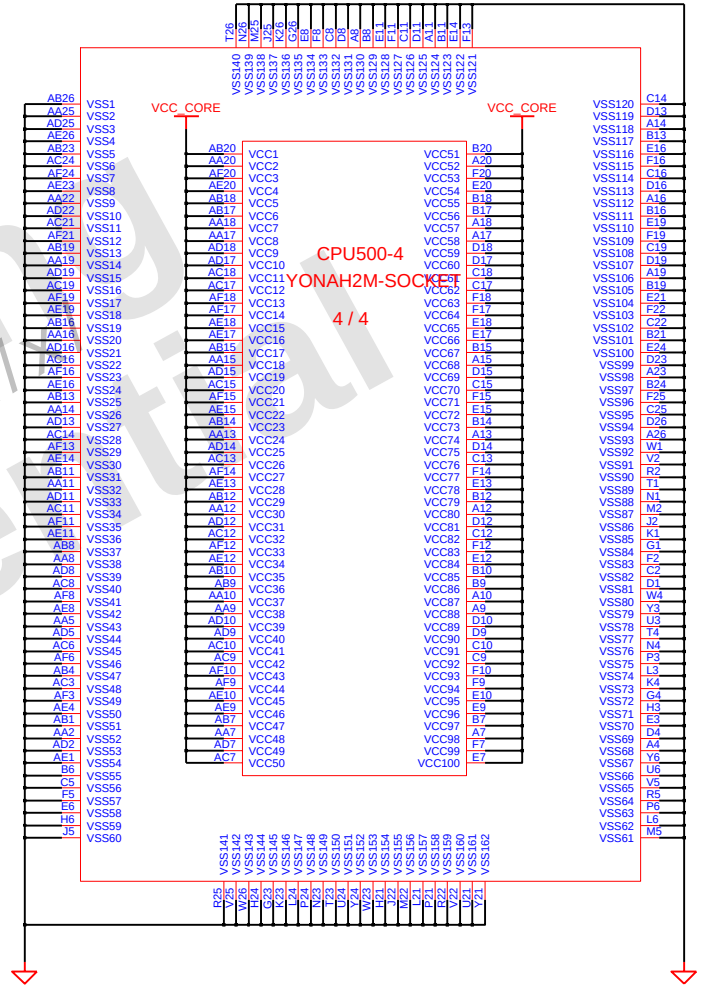

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CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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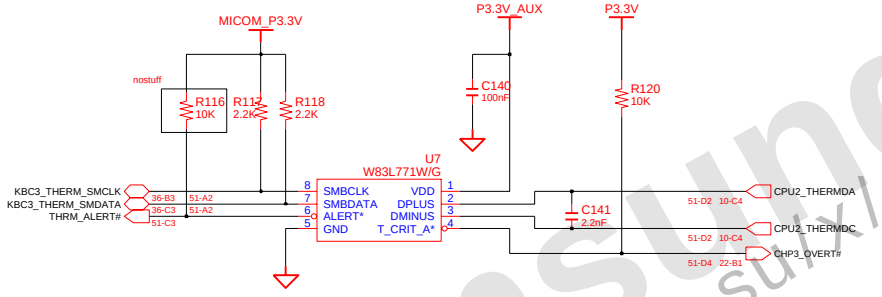
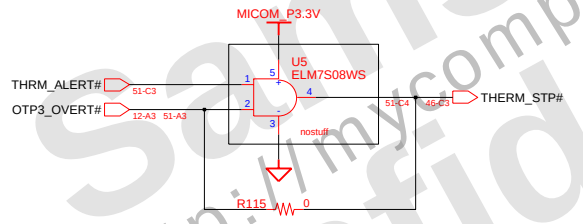
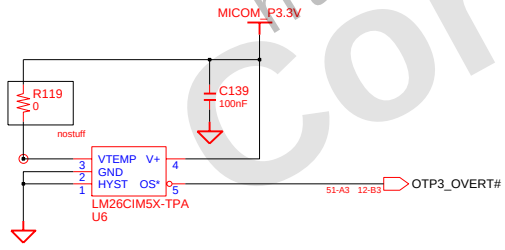
Refer To Thermal Sensor Layout Guidelines.

- Place the Thermal Sensor close to a remote diode.
- Keep traces away from high voltage (+12V bus)
- Keep traces away from fast data buses and CRT signal.
- Use recommended trace widths and spacings (10mil)
- Place a ground plane under the traces.
- Use guard traces flanking DXP and DXN and connecting to GND

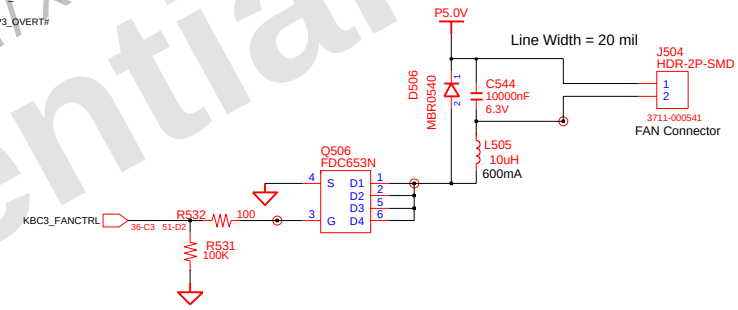
CPU Thermal Sensor

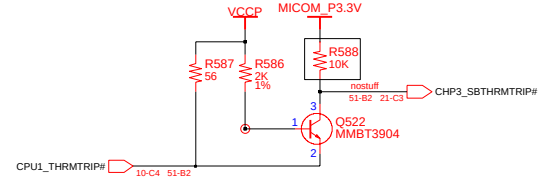






FAN Control Logic





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CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO. BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 12 OF 52	

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DUCT + FAN SUPPORTER

M500 HEAD DIA LENGTH
M4 HEAD DIA LENGTH
M1 HEAD DIA LENGTH
M6 HEAD DIA LENGTH
M5 HEAD DIA LENGTH
M3 HEAD DIA LENGTH

U507-1
RS600ME
1 OF 5

P-4 AGTL + I/F

CPU1_A#(31:3)
CPU1_REQ#(4:0)
CPU1_ADSTB0#
CPU1_ADSTB1#
CPU1_ADS#
CPU1_BNR#
CPU1_BPRI#
CPU1_DEFER#
CPU1_DRDY#
CPU1_DBSY#
CPU1_LOCK#
CPU1_CPURST#
CPU1_RS2#
CPU1_RS1#
CPU1_RS0#
CPU1_BREQ#
CPU1_TRDY#
CPU1_HIT#
CPU1_HITM#
CPU1_DPWR#
CHP3_SUSSTAT#
KBC3_NBPWRGD
CHP3_NBRST#
CPU1_SLP#

ADDR.GROUP 0: CPU_A3# CPU_A4# CPU_A5# CPU_A6# CPU_A7# CPU_A8# CPU_A9# CPU_A10# CPU_A11# CPU_A12# CPU_A13# CPU_A14# CPU_A15# CPU_A16# CPU_REQ0# CPU_REQ1# CPU_REQ2# CPU_REQ3# CPU_REQ4# CPU_ADSTB0#

ADDR.GROUP 1: CPU_A17# CPU_A18# CPU_A19# CPU_A20# CPU_A21# CPU_A22# CPU_A23# CPU_A24# CPU_A25# CPU_A26# CPU_A27# CPU_A28# CPU_A29# CPU_A30# CPU_A31# CPUA32#_NC CPUA33#_NC CPU_ADSTB1# CPU_RESERVED

CONTROL: CPU_ADS# CPU_BNR# CPU_BPRI# CPU_DEFER# CPU_DRDY# CPU_DBSY# CPU_LOCK# CPU_CPURST# CPU_RS2# CPU_RS1# CPU_RS0# CPU_BR0# CPU_TRDY# CPU_HIT# CPU_HITM# CPUDPWR#

MISC: SUS_STAT# SYSRESET# POWERGOOD CPU_COMP_P CPU_COMP_N THERMALDIODE_P THERMALDIODE_N IOPLLVDD18 IOPLLVDD12 IOPLLVSS CPUSLP#_RESERVED1 CPU_VREF TESTMODE

DATA GROUP 0: CPU_D0# CPU_D1# CPU_D2# CPU_D3# CPU_D4# CPU_D5# CPU_D6# CPU_D7# CPU_D8# CPU_D9# CPU_D10# CPU_D11# CPU_D12# CPU_D13# CPU_D14# CPU_D15# CPU_DBI0# CPU_DSTB0N# CPU_DSTB0P#

DATA GROUP 1: CPU_D16# CPU_D17# CPU_D18# CPU_D19# CPU_D20# CPU_D21# CPU_D22# CPU_D23# CPU_D24# CPU_D25# CPU_D26# CPU_D27# CPU_D28# CPU_D29# CPU_D30# CPU_D31# CPU_DBI1# CPU_DSTB1N# CPU_DSTB1P#

DATA GROUP 2: CPU_D32# CPU_D33# CPU_D34# CPU_D35# CPU_D36# CPU_D37# CPU_D38# CPU_D39# CPU_D40# CPU_D41# CPU_D42# CPU_D43# CPU_D44# CPU_D45# CPU_D46# CPU_D47# CPU_DBI2# CPU_DSTB2N# CPU_DSTB2P#

DATA GROUP 3: CPU_D48# CPU_D49# CPU_D50# CPU_D51# CPU_D52# CPU_D53# CPU_D54# CPU_D55# CPU_D56# CPU_D57# CPU_D58# CPU_D59# CPU_D60# CPU_D61# CPU_D62# CPU_D63# CPU_DBI3# CPU_DSTB3N# CPU_DSTB3P#

CPU1_D#(63:0)
CPU1_DBI0# CPU1_DSTBN0# CPU1_DSTBP0#
CPU1_DBI1# CPU1_DSTBN1# CPU1_DSTBP1#
CPU1_DBI2# CPU1_DSTBN2# CPU1_DSTBP2#
CPU1_DBI3# CPU1_DSTBN3# CPU1_DSTBP3#

P1.8V_AUX
R173 4K7 nostuff
R145 0 nostuff
R128 0 nostuff
R130 0
Q29 RHU002N06
P1.2V
R129 1K 1% nostuff
B513 BLM18PG181SN1
C617 2200nF 10V
P1.8V
B17 BLM18PG181SN1
C167 2200nF 10V
VCCP
R121 49.9 1%
R122 24.9 1%
P3.3V_NB
R107 4.7K
R105 20K 1%
Q23 MMBT3904
Q22 MMBT3904 nostuff nostuff
R106 2.2K
R94 61.9 1%
R95 127 1%
C132 1000nF 6.3V
C133 220pF
R98 4.7K

PLACE CLOSE TO NB
USE 10/10MIL WIDTH/SPACE

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CHECK: HJ KIM	DEV. STEP: MP		PART NO. BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 13 OF 52	

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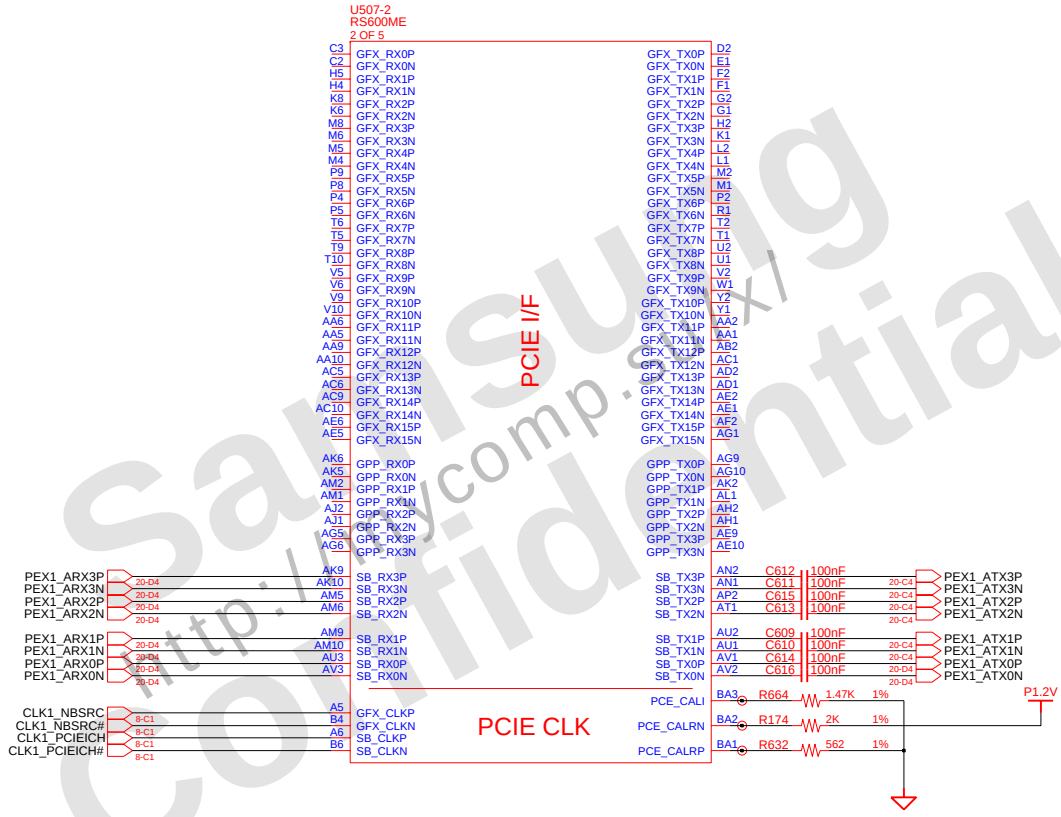

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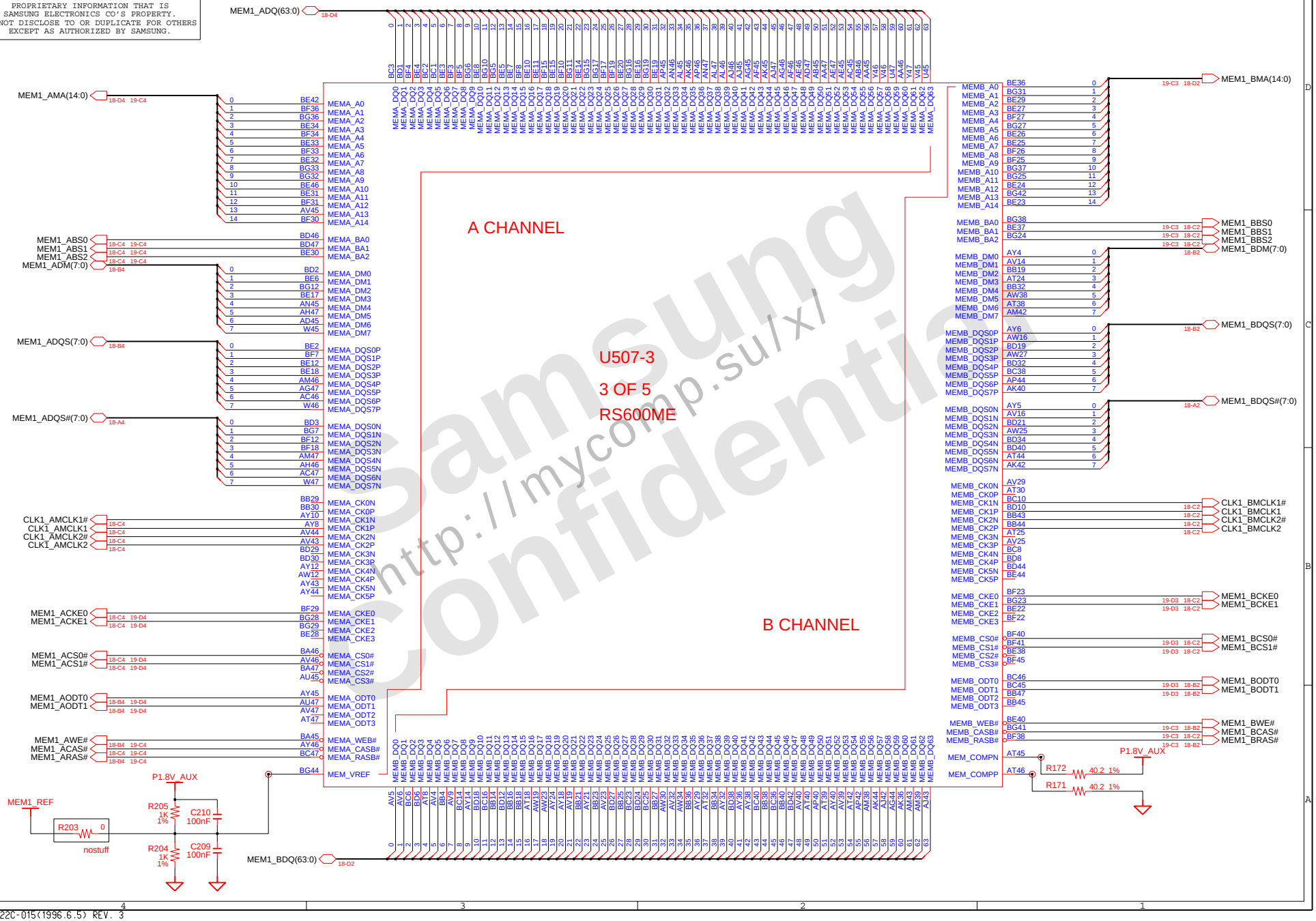

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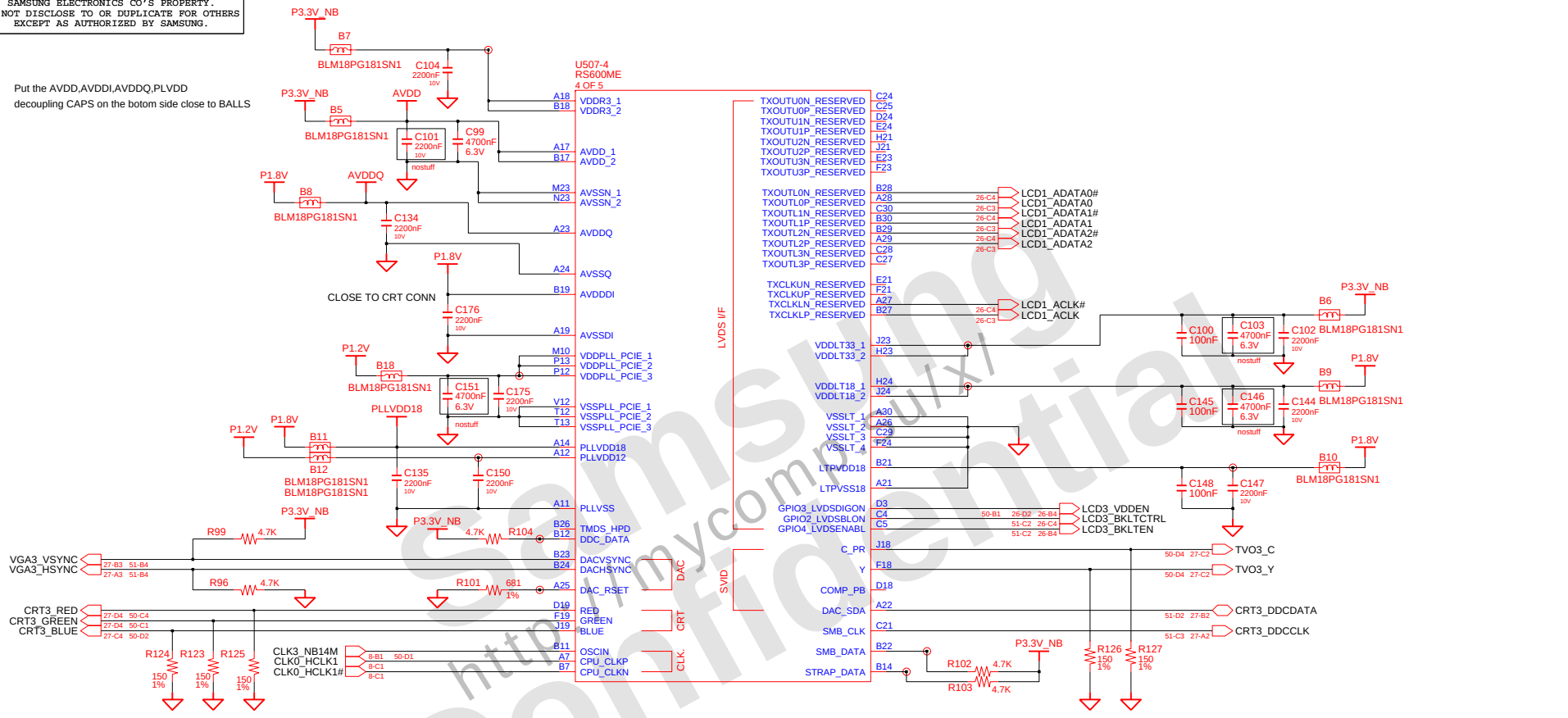

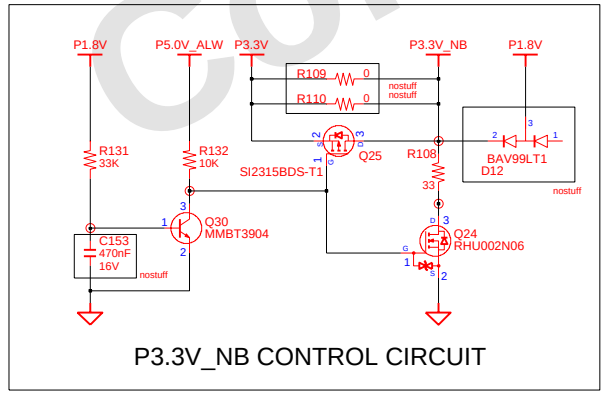

P3.3V_NB CONTROL CIRCUIT

STRAP DEFINITIONS FOR THE RS600M

STRAP PIN	DESCRIPTION
DACHSYNC	Enable/Disable integrated graphics. 0 : Enable integrated graphics 1 : Disable integrated graphics
STRP_DATA	Debug strap configuration. This strap should not be set to "0" on production boards. 0 : Select Memory Channel A to be a debug bus 1 : Read debug straps from an external EEPROM, or disable debug mode when an EEPROM is absent.
DACVSYNC	Select configuration of the integrated graphics engine. 0 : Reserved 1 : Required setting for the RS600M
DDC_DATA	Select DDR2 or DDR3 signalling level for the memory interface. 0 : DDR3. On DDR3, it is necessary to put an isolation FET in series with the pull-up resistor on this strap to separate it from the I2C circuit during an NB reset 1 : DDR2

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN RS600M(4/5)	SAMSUNG ELECTRONICS
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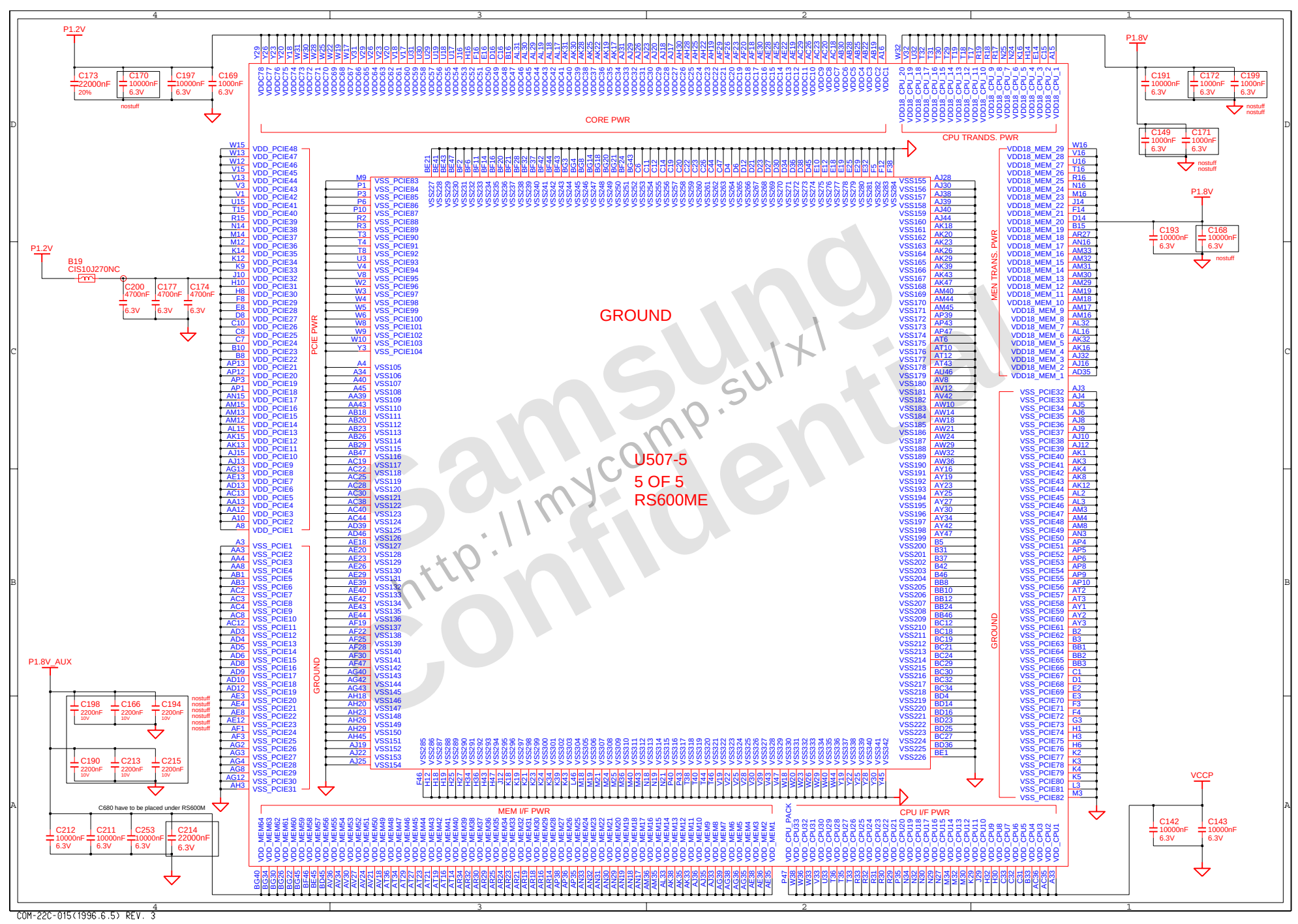
GROUND
U507-5
5 OF 5
RS600ME
CORE PWR
CPU TRANDS. PWR
MEN TRANS. PWR
PCIE PWR
GROUND
MEM I/F PWR
CPU I/F PWR
P1.2V
P1.8V
P1.8V_AUX
B19
CIS10J270NC
C680 have to be placed under RS600M
nostuff
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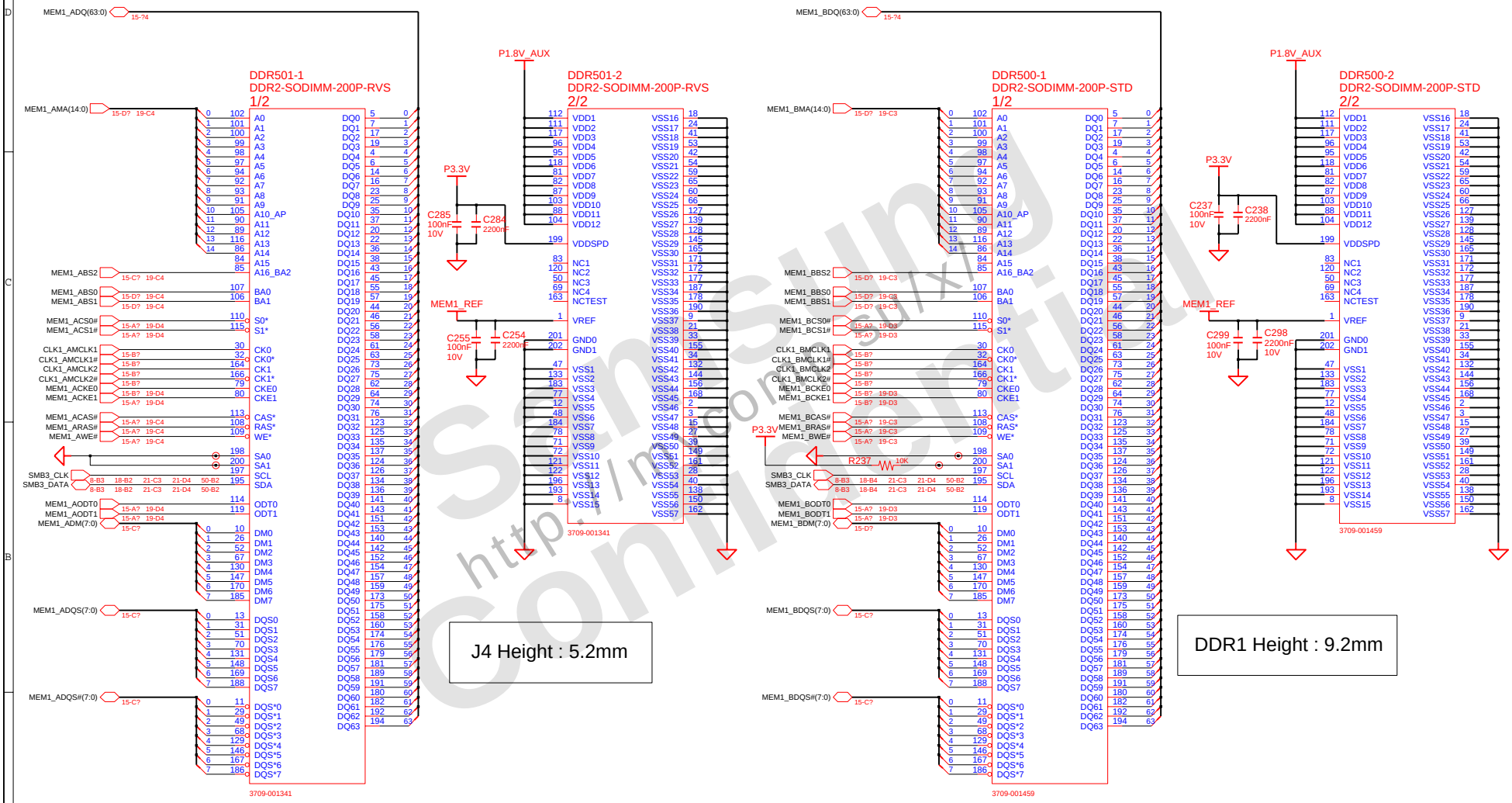

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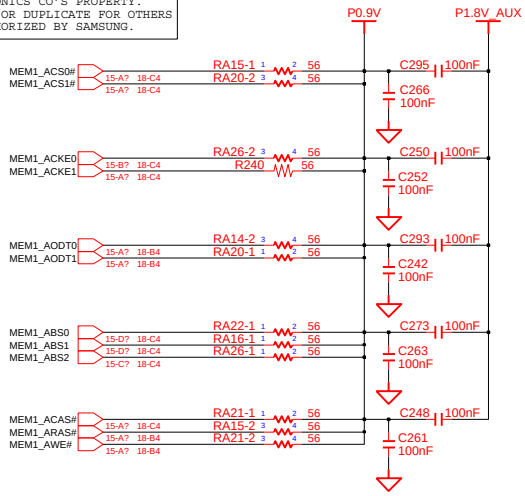
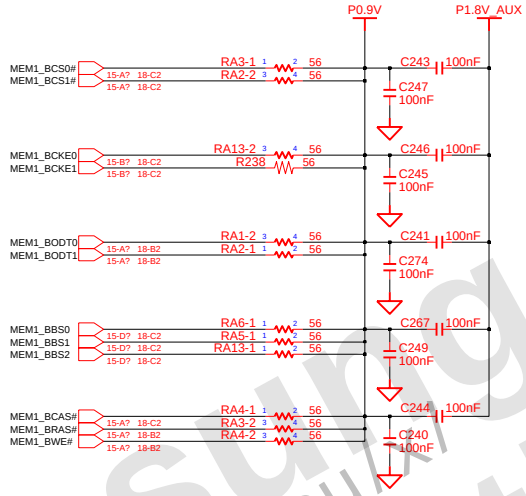
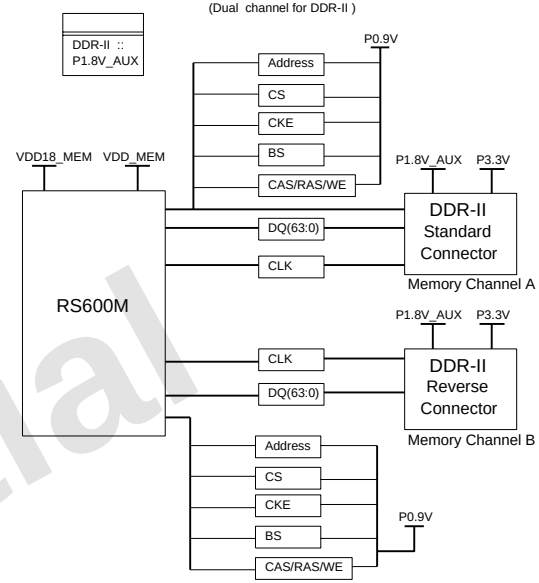
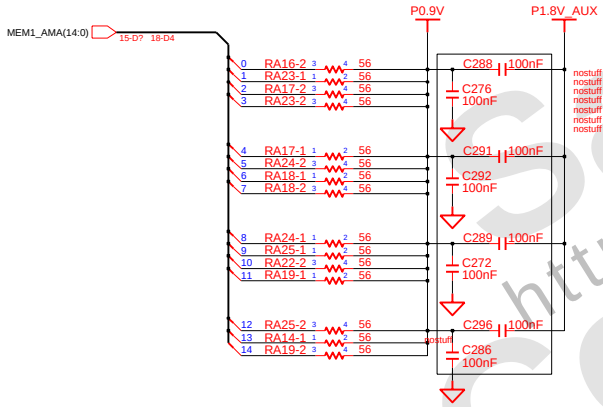


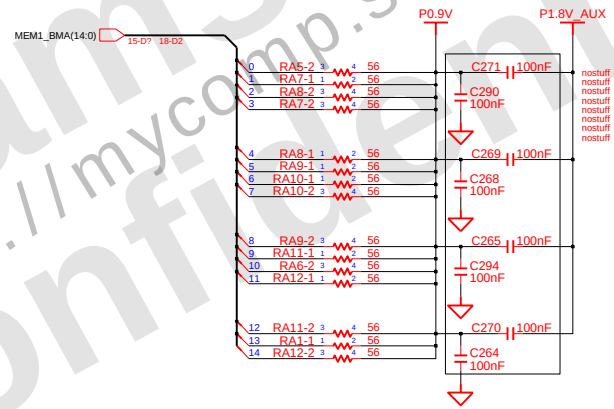


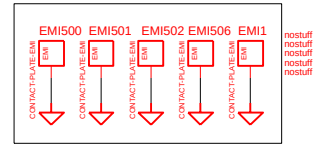
Memory Topology

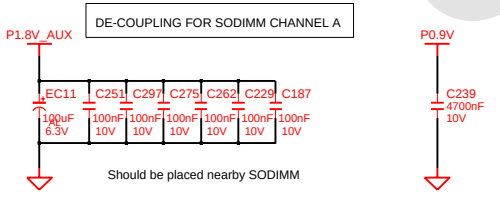
(Dual channel for DDR-II)

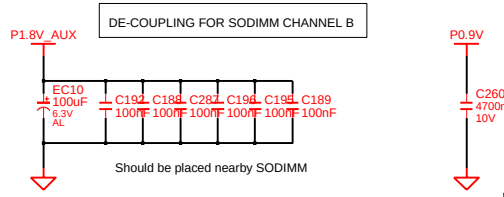












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CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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U9-1
218S6ECLA21FG
1 / 4

CHP3_ALINK_RST# R679 8.2K
CLK1_PCIERCLK
CLK1_PCIERCLK#
PEX1_ARX0P / PEX1_ARX0N / PEX1_ARX1P / PEX1_ARX1N / PEX1_ARX2P / PEX1_ARX2N / PEX1_ARX3P / PEX1_ARX3N
PEX1_ATX0P / PEX1_ATX0N / PEX1_ATX1P / PEX1_ATX1N / PEX1_ATX2P / PEX1_ATX2N / PEX1_ATX3P / PEX1_ATX3N
PCIE_VDDR
R626 562 1% R625 2K 1% R627 0
P1.2V B517 BLM18PG181SN1 C641 10000nF 6.3V C639 1000nF 6.3V
P1.2V B516 BLM18PG181SN1 C637 22000nF 20% C604 1000nF 6.3V C640 1000nF 6.3V C607 1000nF 6.3V C605 100nF C606 100nF
P3.3V_AUX U11 ELM7S08WS PCI3_RSTF# R225 8.2K R234 33 PCI3_RST# R233 0
Y500 32.768KHz R591 20M R590 20M C584 0.018nF C583 0.018nF
VCCP R304 4.7K Q46 MMBT3904 R305 47K ATI PA for Power on Fail (2007.01.05)
CPU1_DPRSTP# R660 0
R773 475 1% PRTC_BAT R268 1K 1% Move to RTC Battery Connector C591 100nF 25V C590 1000nF 25V

PCI EXPRESS INTERFACE
PCI CLKS
PCI INTERFACE
XTAL
CPU
LPC
RTC

CLK3_33M_MIN
CLK3_PCLKLAN
CLK3_PCLKCB
STRAP_USB48
C748 0.022nF C747 0.022nF
CPU1_PWRGDCPU R89 300 nostuff
CPU1_SLP# R90 200
CPU1_DPSLP# R88 470
VCCP
CLK3_PCLKMICOM
PCI3_RSTF#
PCI3_AD(31:0)
P3.3V
PCI3_REQ0# R223 8.2K
PCI3_REQ1# R667 8.2K
PCI3_REQ2# R262 8.2K
PCI3_PLOCK# R671 8.2K
PCI3_INTA# R703 8.2K
PCI3_INTB# R263 8.2K
PCI3_INTC# R668 8.2K
PCI3_INTD# R669 8.2K
PCI3_FRAME# R702 8.2K
PCI3_TRDY# R704 8.2K
PCI3_IRDY# R261 8.2K
PCI3_DEVSEL# R673 8.2K
PCI3_STOP# R243 8.2K
PCI3_SERR# R657 8.2K
PCI3_PERR# R260 8.2K
R224 10K R221 10K
CHP3_ALINK_RST# R681 33 R680 33 PLT3_RSTF# CHP3_NBRST#
PCI3_CBE0# / PCI3_CBE1# / PCI3_CBE2# / PCI3_CBE3# / PCI3_FRAME# / PCI3_DEVSEL# / PCI3_IRDY# / PCI3_TRDY# / PCI3_PAR / PCI3_STOP# / PCI3_PERR# / PCI3_SERR# / PCI3_REQ0# / PCI3_REQ1# / PCI3_REQ2#
LPC3_LAD(0) R685 100K
LPC3_LAD(1) R686 100K
LPC3_LAD(2) R687 100K
LPC3_LAD(3) R688 100K
CHP3_SERIRQ R272 10K
P3.3V
R222 10K
PCI3_GNT0# / PCI3_GNT1# / PCI3_GNT2# / CHP3_BIOSWP#
PCI3_CLKRUN#
PCI3_PLOCK#
PCI3_INTA# / PCI3_INTB# / PCI3_INTC# / PCI3_INTD#
LPC3_LAD(3:0)
P3.3V
R226 10K R227 10K
LPC3_LFRAME#
CHP3_SERIRQ R659 10K
RTC_CLK R609 10K
MICOM_P3.3V
D22 BAT54C
PRTC_BAT
C647 1000nF 25V C312 1000nF
J6 HDR-2P-SMD 3711-000541
For CMOS Reset Place the bottom of memory door
RTC Battery Connector

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN SB600(1/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 20 OF 52	

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U9-2
218S6ECLA21FG
2 / 4

USB Port 0, 1 : Rear side USB Port
USB Port 2, 3 : Left side USB Port
USB Port 4 : Bluetooth I/F
USB Port 5 : DMB I/F

Have to be checked in case of SB600

Add below Components to reduce EMI noise from SB450(060310) (R601, R628, R629, R630, B510, B511)

Place on the upper side

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R POWER SB600(2/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 21 OF 52	

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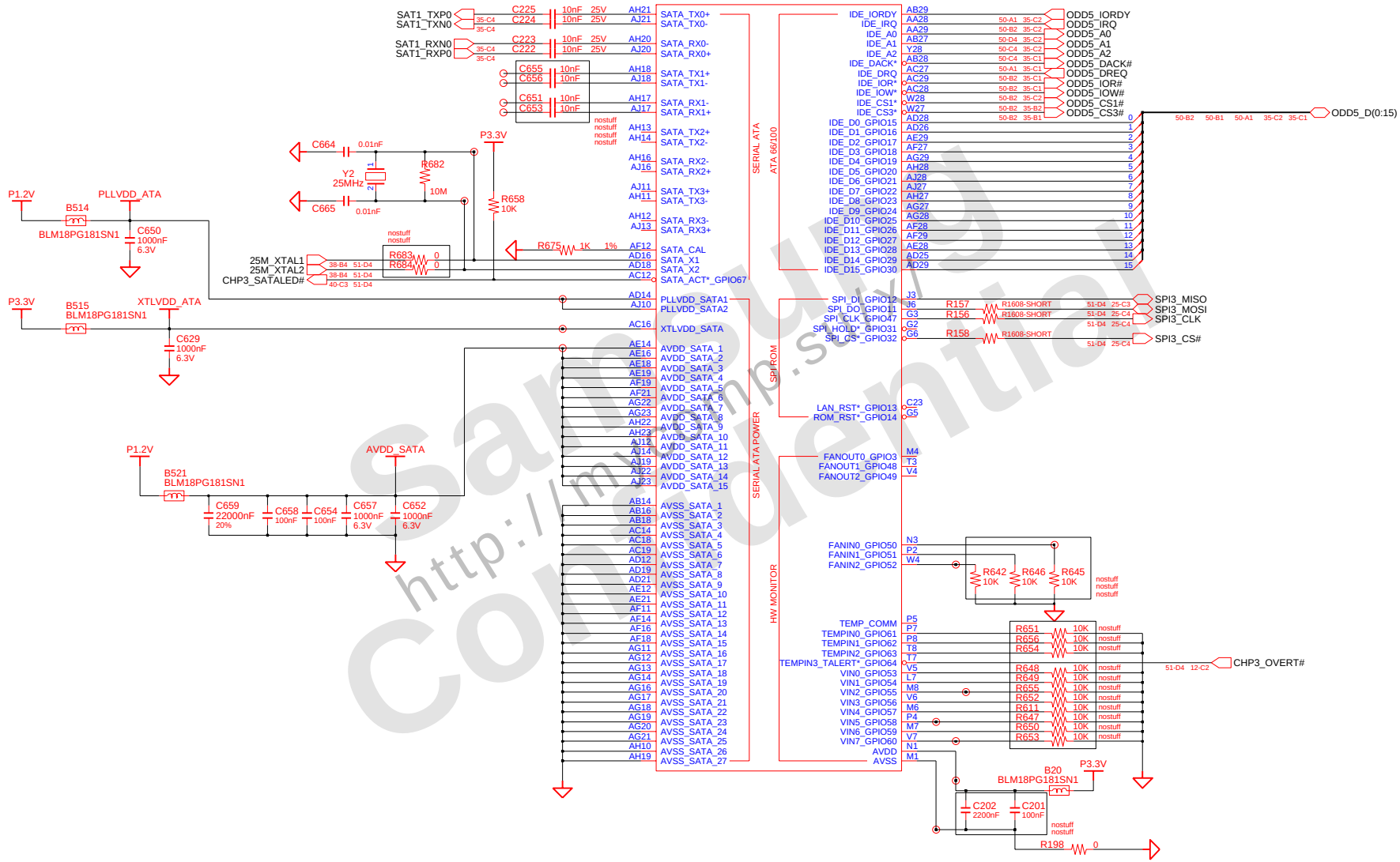
U9-3
218S6ECLA21FG
3 / 4



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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN SB600(3/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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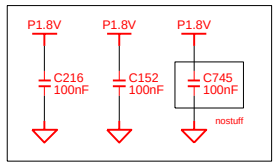

To Reduce EMI noise from SB450 (060310)

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN SB600(4/4)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 23 OF 52	

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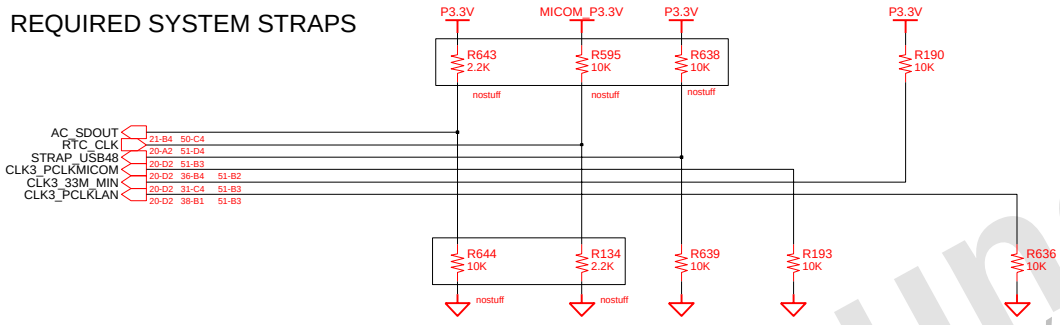
SB600 HAS AN INTERNAL PD FOR AC_SDOUT
SB600 HAS AN INTERNAL PU FOR RTC_CLK

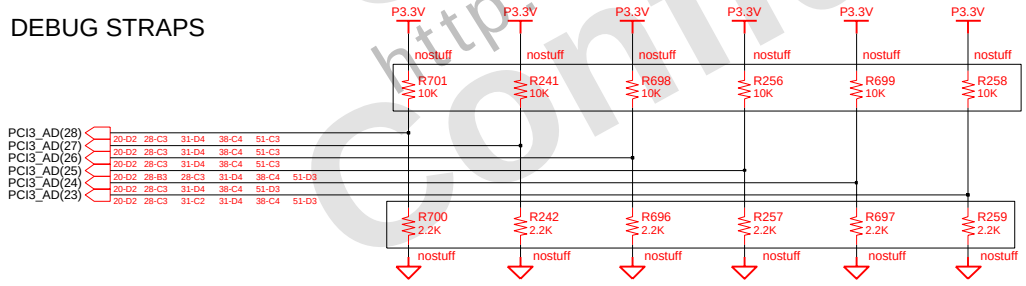
REQUIRED SYSTEM STRAPS



	AC_SDOUT	RTC_CLK	PCI3_CLK4	PCI3_CLK6	PCI3_CLK0 PCI3_CLK1
STRAP HIGH	USE DEBUG STRAPS	INTERNAL RTC	USE INTERNAL PLL48	CPU I/F = K8	ROM TYPE H, H = PCI ROM H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM
STRAP LOW	IGNORE DEBUG STRAPS	EXRERNAL RTC (PD on X1, Apply 32KHz to RTC_CLK)	USE EXTERNAL 48MHz	CPU I/F = P4	

SB600 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

DEBUG STRAPS



	PCI3_AD(28)	PCI3_AD(27)	PCI3_AD(26)	PCI3_AD(25)	PCI3_AD(24)	PCI3_AD(23)
STRAP HIGH	USE LONG RESET	USE PCI PLL	USE ACPI BCLK	USE IDE PLL	USE DEFAULT PCIE STRAPS	BOOTFAILTIMER DISABLED
STRAP LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	BOOTFAILTIMER ENABLED

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R STRAPS	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
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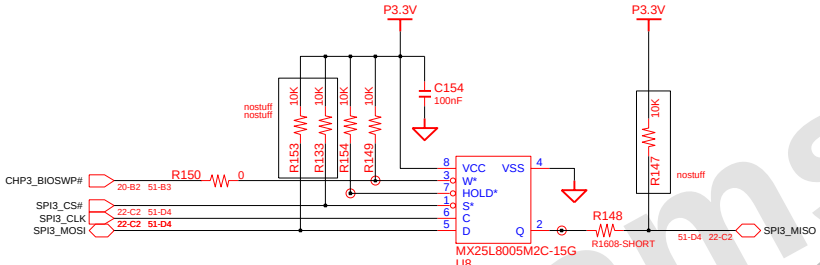

SPI3_CS#
SB600 prior to A21 : Pulled up to P3.3V_ALW with 1Kohm resistor.
SB600 A21 and newer : No external pull-up resistor required.

02 VERIFY REAL MODE	66 CONFIGURE ADVANCE CACHE REG.
03 DISABLE NMI	6A DISPLAY EXTERNAL CACHE SIZE
04 GET CPU TYPE	6C DISPLAY SHADOW MESSAGE
06 INIT. SYSTEM H/W	6E DISPLAY NON-DISPOSABLE SEGMENT
08 INIT. CHIPSET REG.	70 DISPLAY ERROR MESSAGE
09 SET IN POST FLAG	72 CHECK FOR CONFIGURATION ERROR
0A INIT CPU.REG	74 TEST REAL-TIME CLOCK
0B CPU CACHE ON	76 CHECK FOR KEYBOARD EERROR
0C INIT.CACHE TO POST	7C SETUP HARDWARE INTERRUPT VECTOR
OE INIT. I/O VALUE	7E TEST COPROCESSER IF PRESENT
0F ENABLE THE L-BUS IDE	80 DISABLE ON-BOARD I/O PORT
10 INIT. POWER MANAGER	82 DETECT AND INSTALL EXT.RS232C
11 LOAD ALTERNATE REG.	84 DETECT AND INSTALL EXT.PARALLEL
13 PCI BUS MASTER RESET WITH INITIAL POST VALUE	86 RE-INIT. ON-BOARD I/O PORT
	88 INIT. BIOS DATA ROM
14 INIT. KEYBOARD CONTROLLER	8A INIT.EXTENDED BIOS DATA AREA
16 CHECK CHECKSUM	8C INIT. FDD CONTROLLER
18 8254 TIMER INIT.	9A SHADOW OPTION ROMS
1A 8237 DMA CONTROLLER INIT.	9C SETUP POWER MANAGEMENT
1C RESET INTERRUP CONTROLLER	9E ENABLE H/W INTERRUPT
20 TEST DRAM REFRESH	A0 SET TIME OF DAY
22 TEST 8742 KEYBOARD CONTROLLER	A4 INIT. TYPEMATIC RATE
24 SET ES SEGMENT REG. TO 4GB	A8 ERASE F2 PROMPT
26 ENABLE A20	AA SCAN FOR F2 KEY STROKE
28 AUTO SIZING DRAM	AC ENTER SETUP
32 COMPUTE THE CPU SPEED	AE CLEAR IN POST FLAG
34 TESET CMOS RAM	B0 CHECK FOR ERRORS
38 SHADOW SYSTEM BIOS ROM	B2 POST DONE-PREPARE TO BOOT O/S
3A AUTO SIZING CACHE	B4 ONE BEEP
3C CONFIGURE ADVANCED CHIPSET REG.	B6 CHECK PASSWORD (OPTION)
3D LOAD ALTER REG. WITH CMOS VALUE	B7 ACPI INIT
42 INIT. INTERRUPT VECTOR	BA DMI INIT
44 INIT. BIOS INTERRUPT	BE CLEAR SCREEN
46 CHECK ROM COPYRIGHT NOTICE	C0 TRY BOOT WITH INT19
47 INIT. I20 SUPPORT IF INSTALLED	D0 INTERRUPT HANDLER ERROR
48 CHECK VIDEO CONFIGURE AGAINST CMOS	D2 UNKNOWN INTERRUPT ERROR
49 INIT. PCI BUS AND DEVICE	D4 PENDING INTERRUPT ERROR
4A INIT. ALL VIDEO BIOS ROM	D6 SHUTDOWN 5
4C SHADOW VIDEO BIOS ROM	D8 SHUTDOWN ERROR
50 DISPLAY CPU TYPE AND SPEED	DA EXTENDED BLOCK MOVE
52 TEST KEYBOARD	DC SHUTDOWN 10
54 SET KEYCLICK IF ENABLED	89 ENABLE NMI
56 ENABLE KEYBOARD	90 INIT. HDD CONTROLLER
58 TEST FOR UNEXPECTED INTERRUPTS	91 INIT. LOCAL BUS HDD CONTROLLER
5A DISPLAY " PRESS ..... SETUP"	92 JUMP TO USER PATCH 2
5C TEST RAM GETWEEN 512K AND 640K	94 DISABLE A20 ADDRESS LINE
60 TEST EXTENDED MEMORY	96 CLEAR HUGE ES SEGMENT REG.
62 TEST EXTENDED MEMORY ADDRESS LINE	98 SEARCH FOR OPTION ROMS
64 JUMP TO USER PATCH 1	

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN FIRMWARE HUB	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 25 OF 52	

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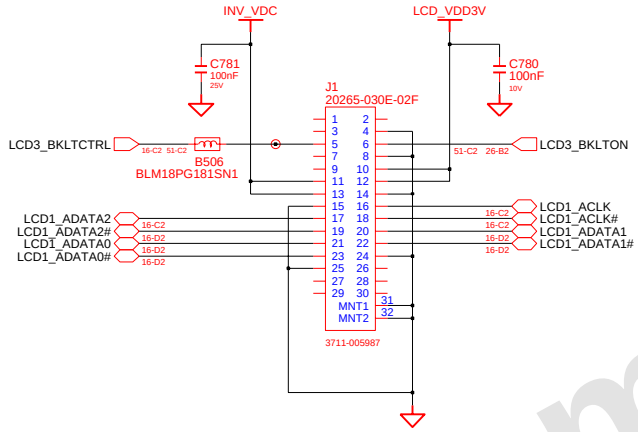
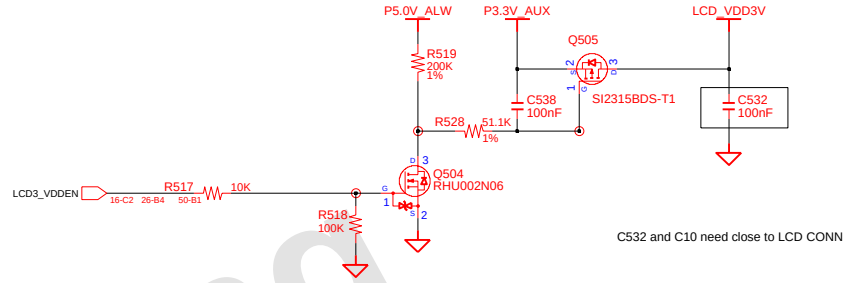
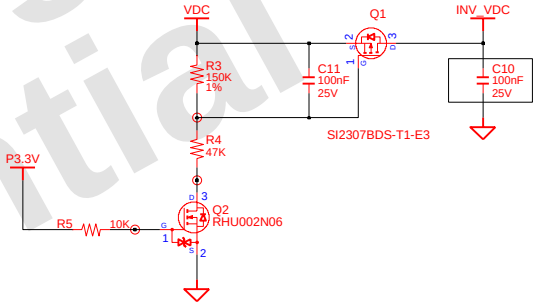
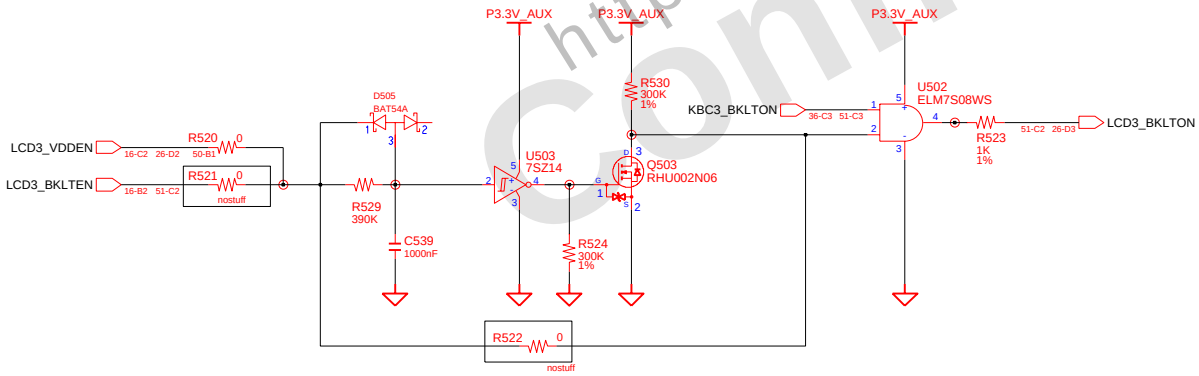


LCD Connector(LVDS)



C532 and C10 need close to LCD CONN





DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R LCD Connector & SPREAD SPECTRUM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO. BA41-00714A
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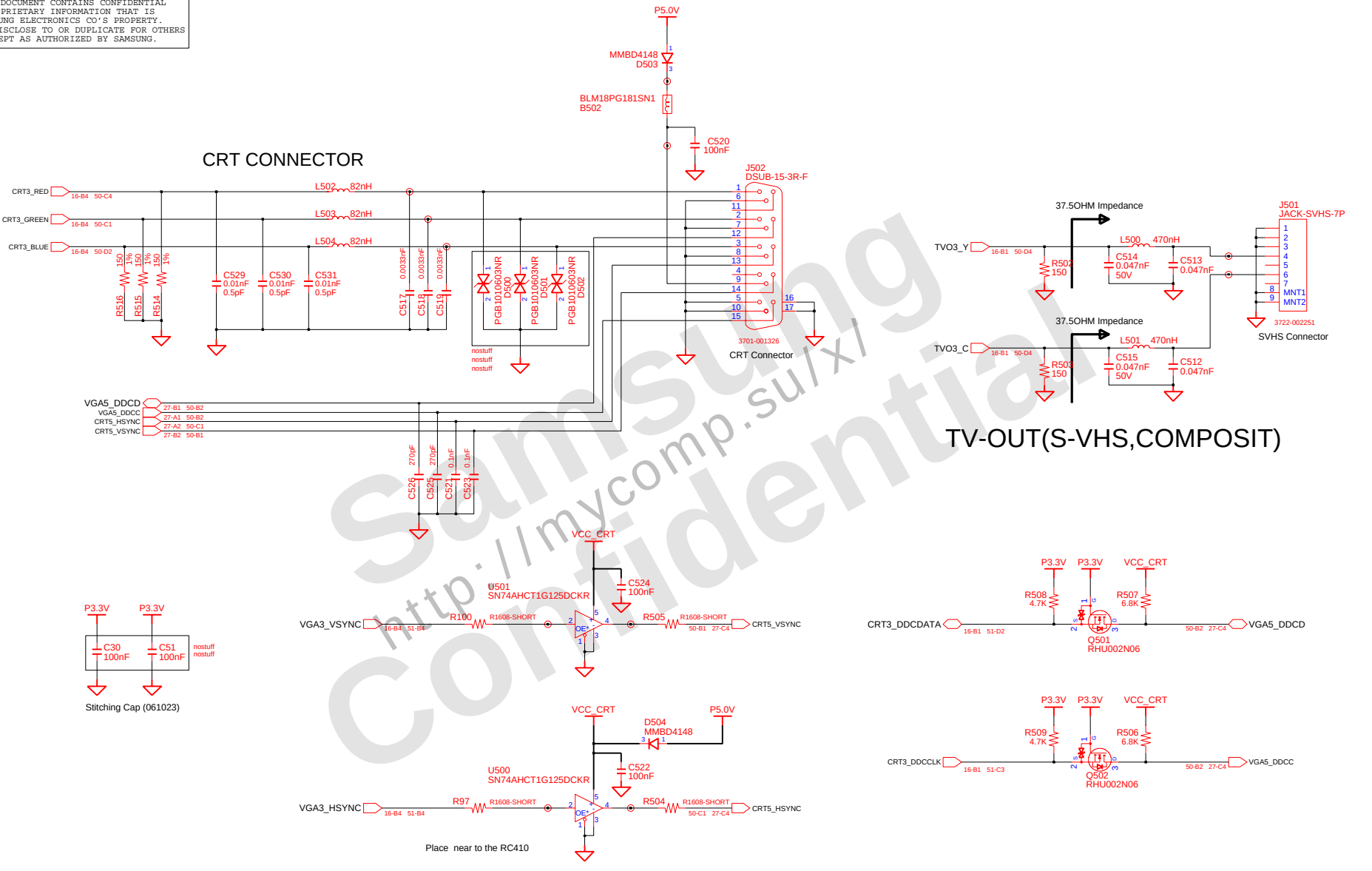

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP	CRT AND TV-OUT	
APPROVAL: SJ PARK	REV: 1.0		PART NO. BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 27 OF 52	

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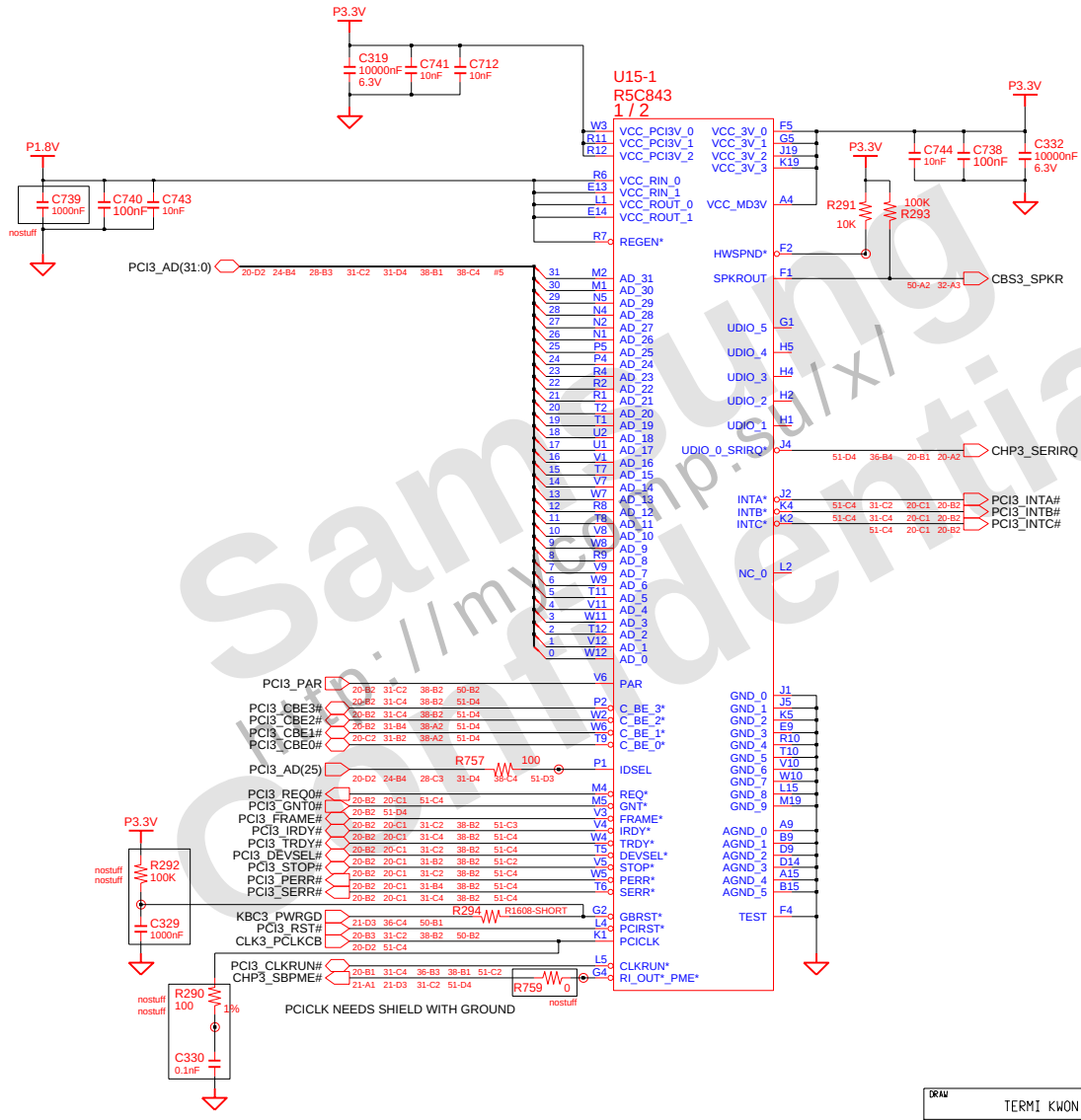

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0	CARDBUS(1/2)	PART NO.: BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 28 OF 52	

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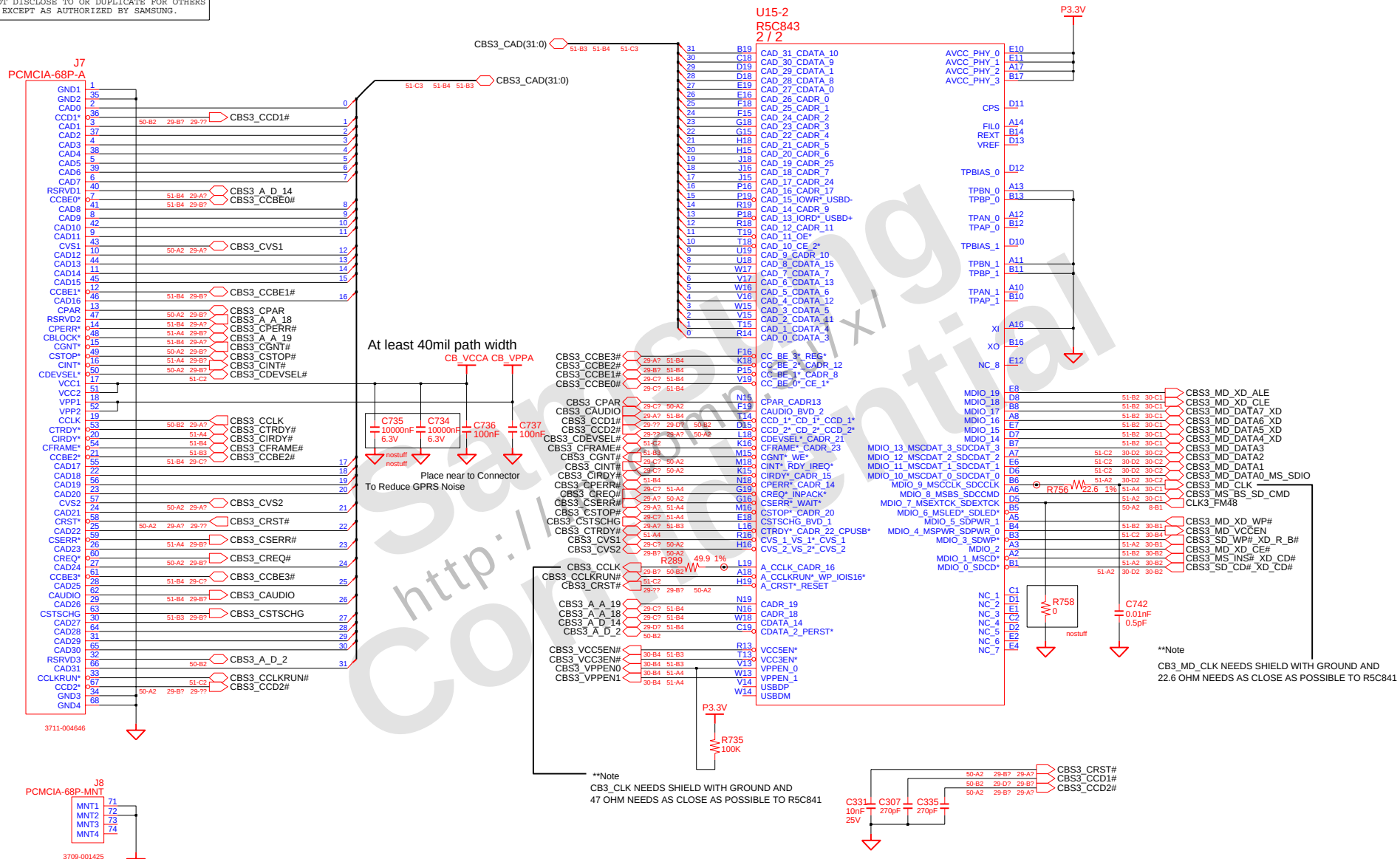

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R CARDBUS(2/2)	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 29 OF 52	

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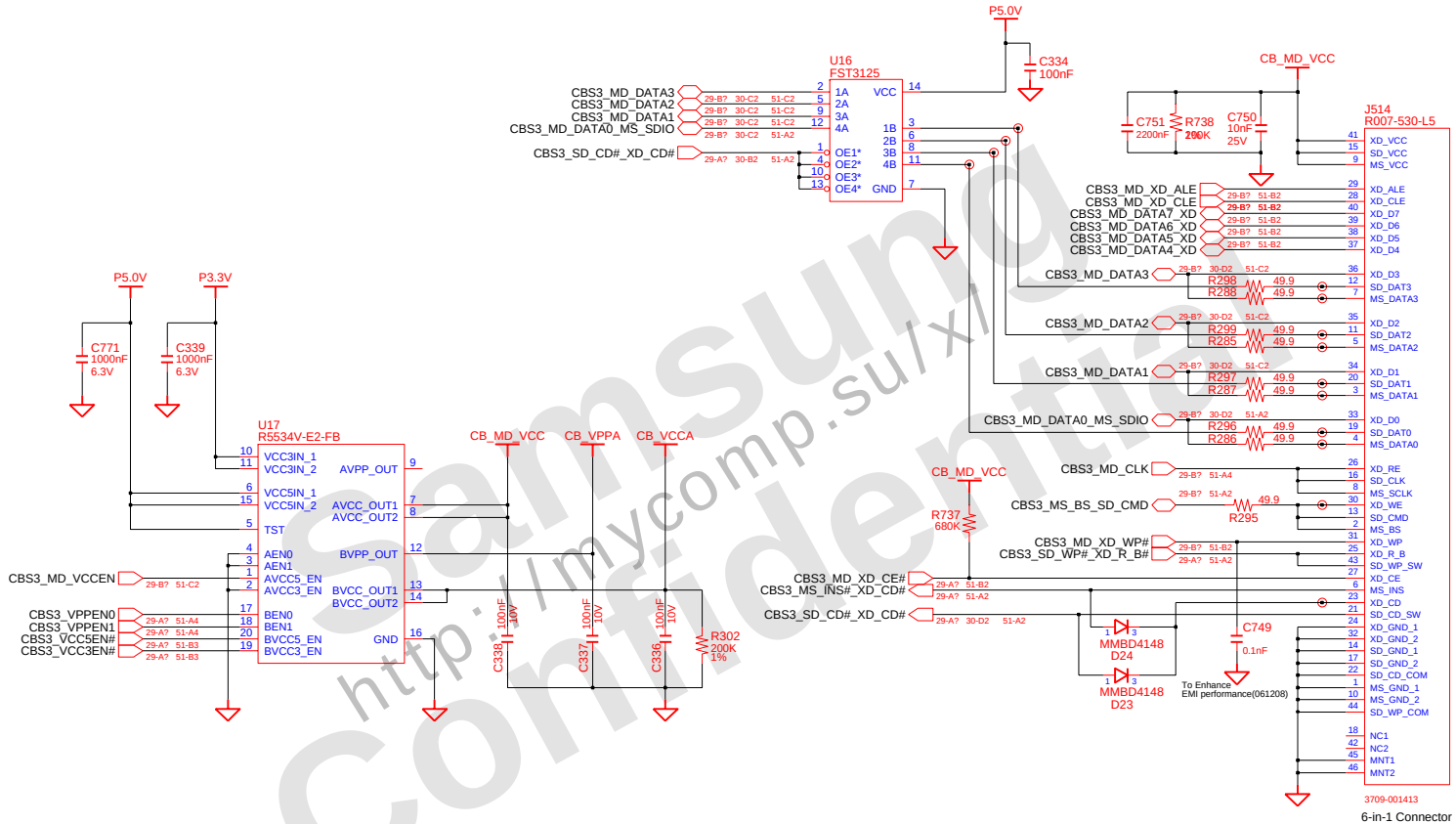

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP	5 in 1 Socket	
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 30 OF 52	

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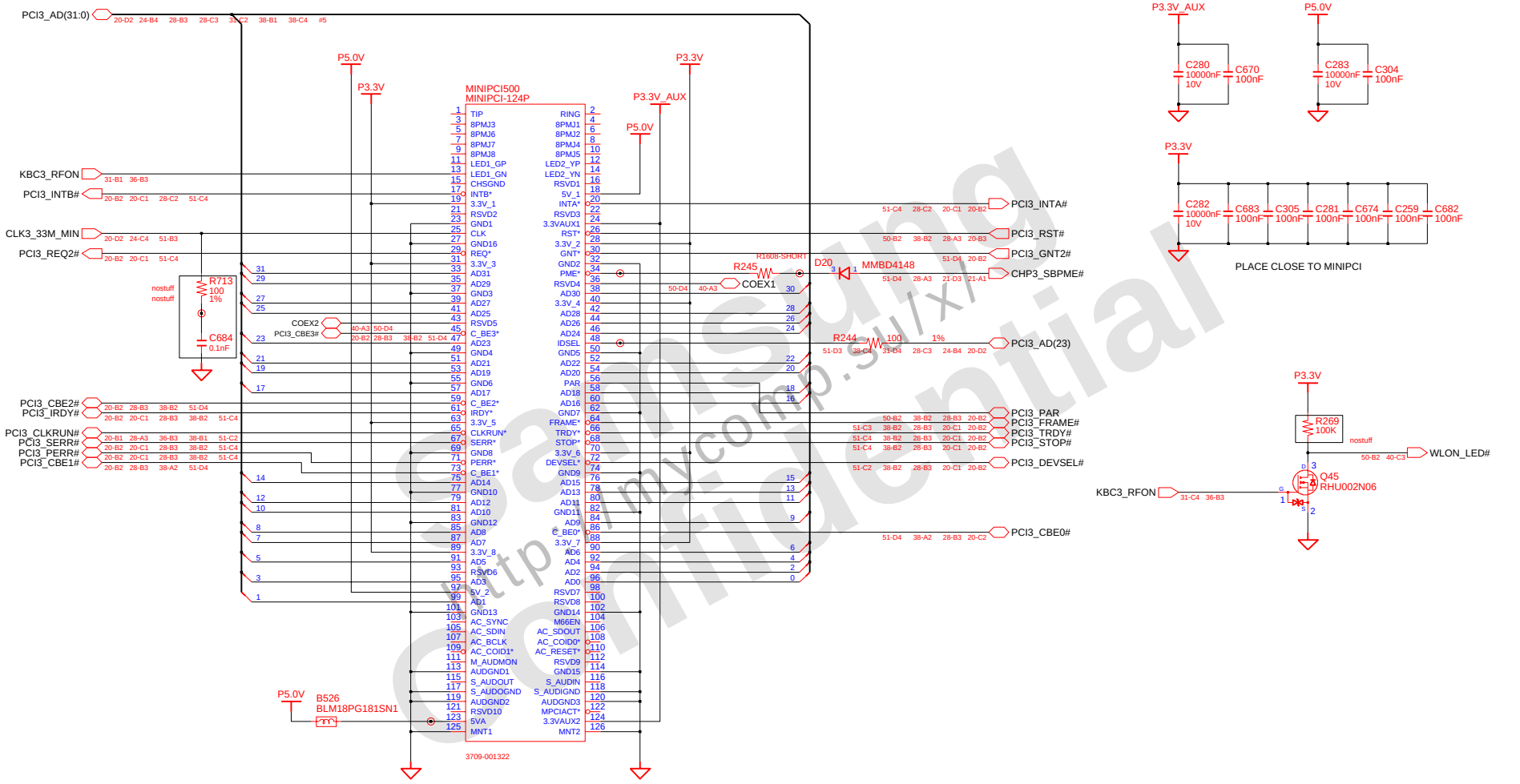

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN MINI PCI	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 31 OF 52	

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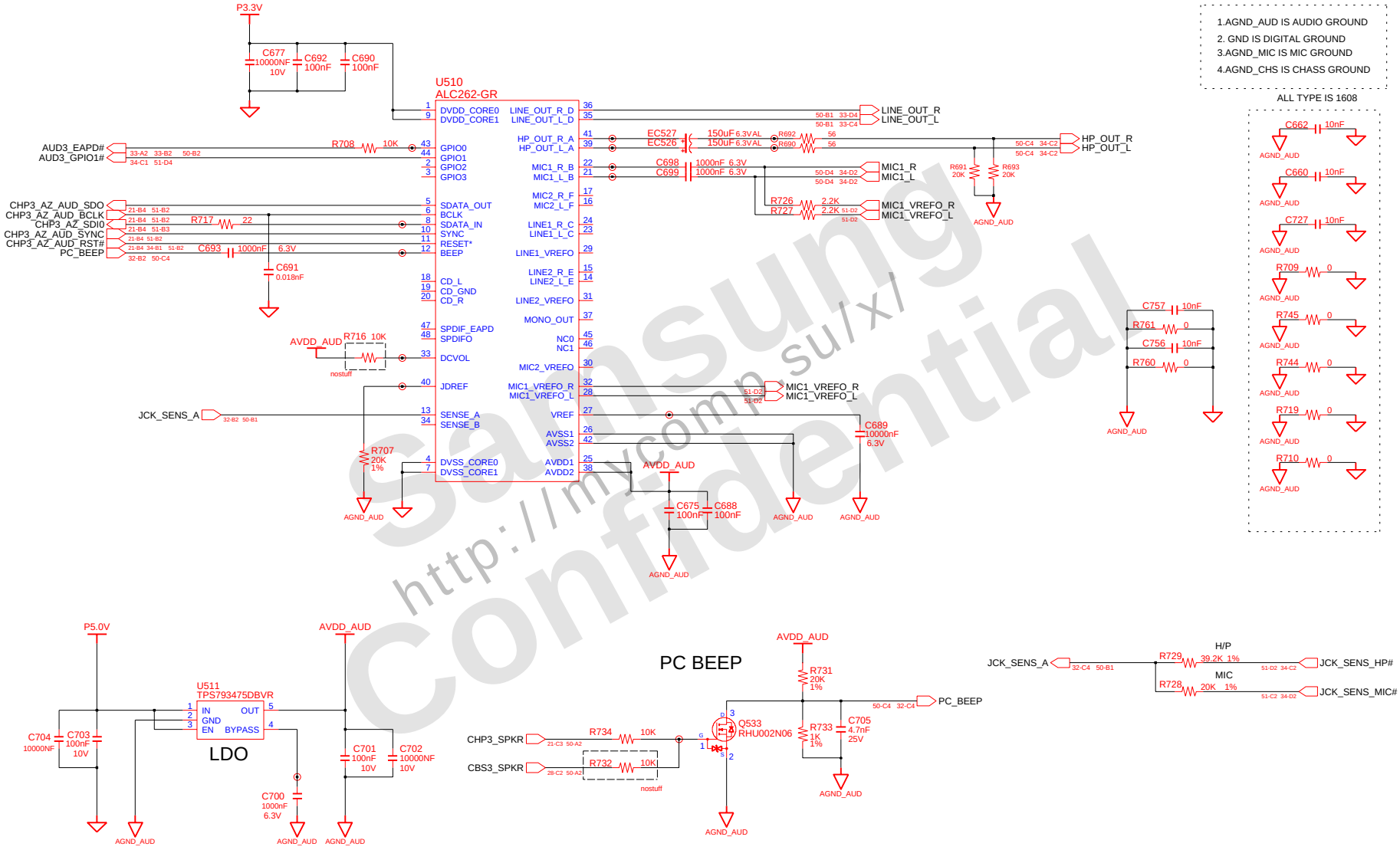

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN AUDIO CODEC	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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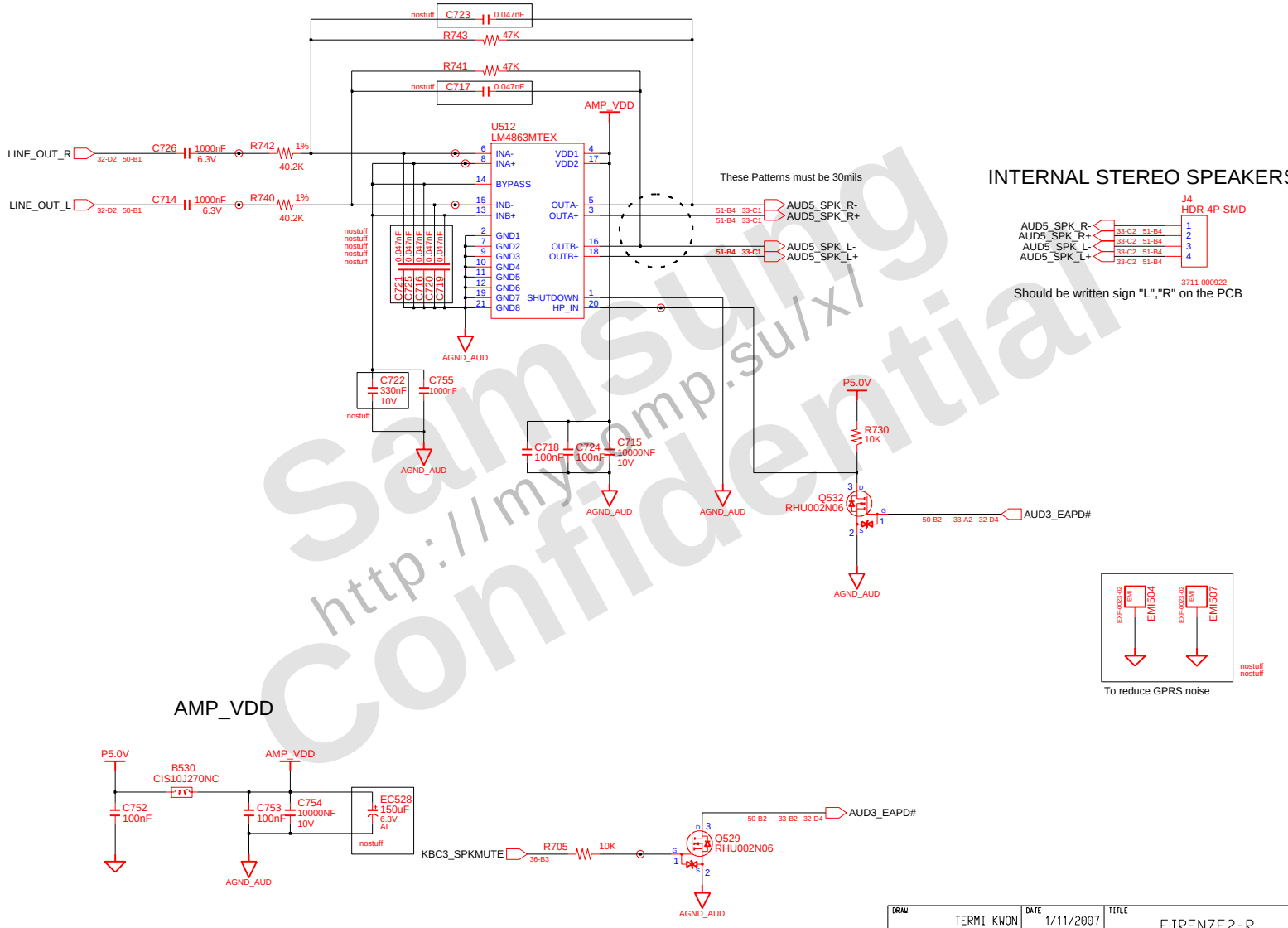

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN LIMITER & AMP	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 33 OF 52	

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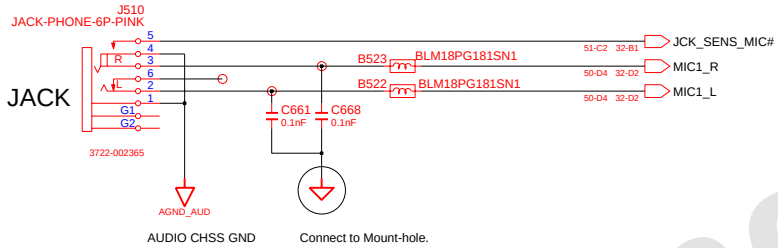
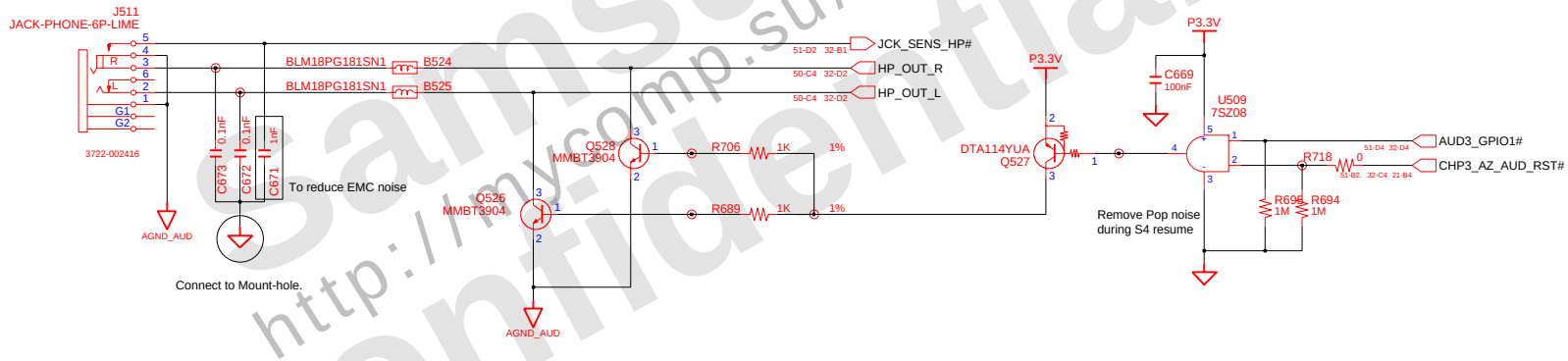
MIC JACK



HEADPHONE



The traces led to Audio Jacks have the width over 10mil

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN UPPER & AUDIO CONN	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 34 OF 52	

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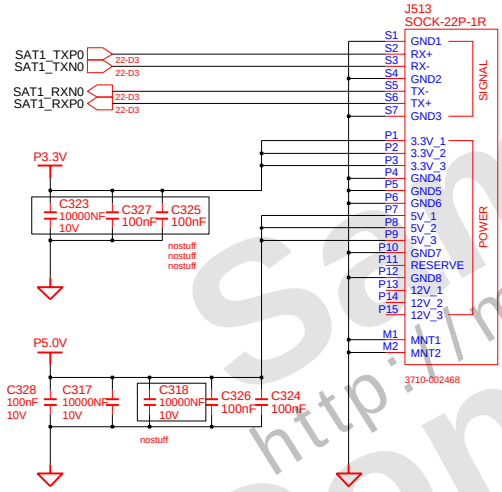
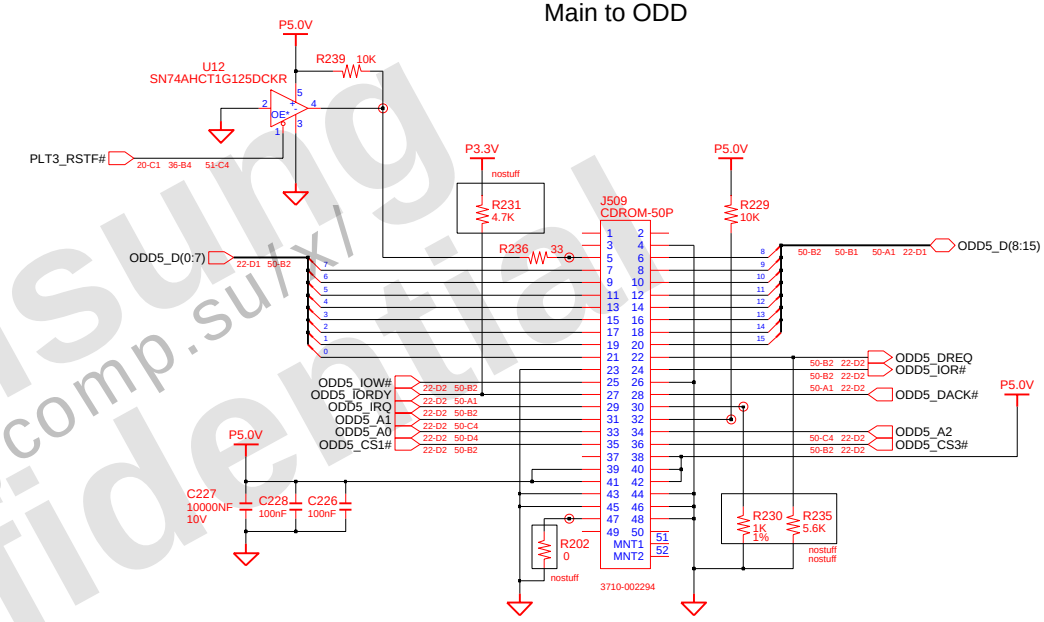
Main to HDD



Main to ODD



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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R POWER HDD & ODD	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 35 OF 52	

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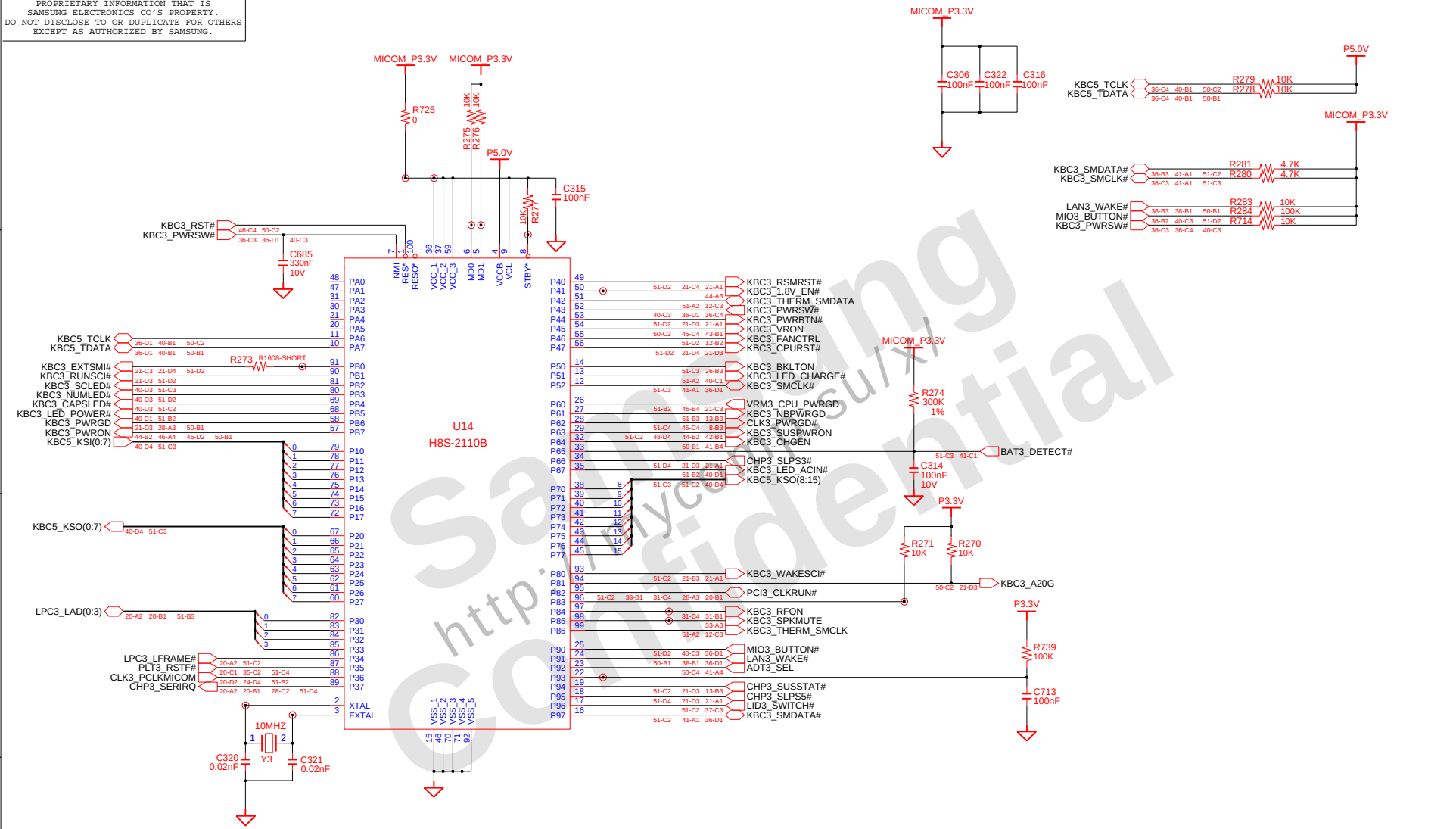

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MICOM Crisis Update

Condition: P90=P91=P92=High(MICOM_P3V)
MD0=MD1=Low(0V)
Serial Port: P84 & P85

The removed signal compaired from 144pin

- KBC5_CAL_THRM*
- THRM_ALERT*
- LCD3_BKLTEN
- FAN3_FDBACK*
- THERM_STP*

DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R POWER MICOM	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 36 OF 52	

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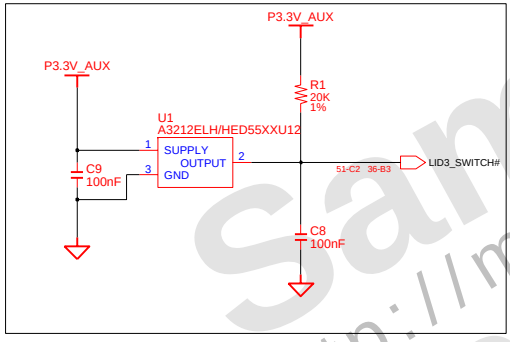
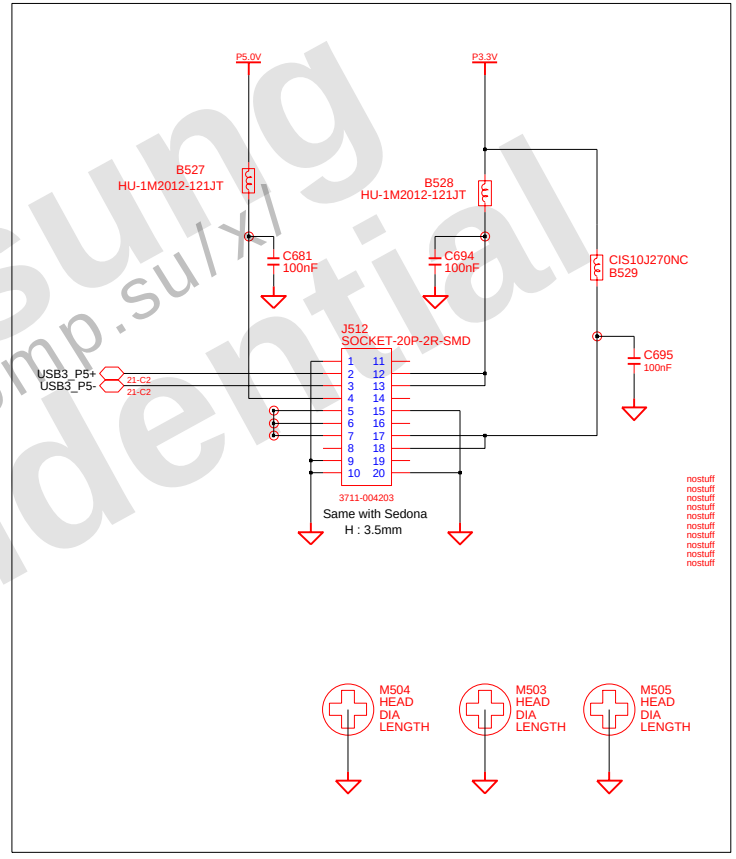
LID SWITCH



DMB (nostuff)

Factory Option



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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN LPC	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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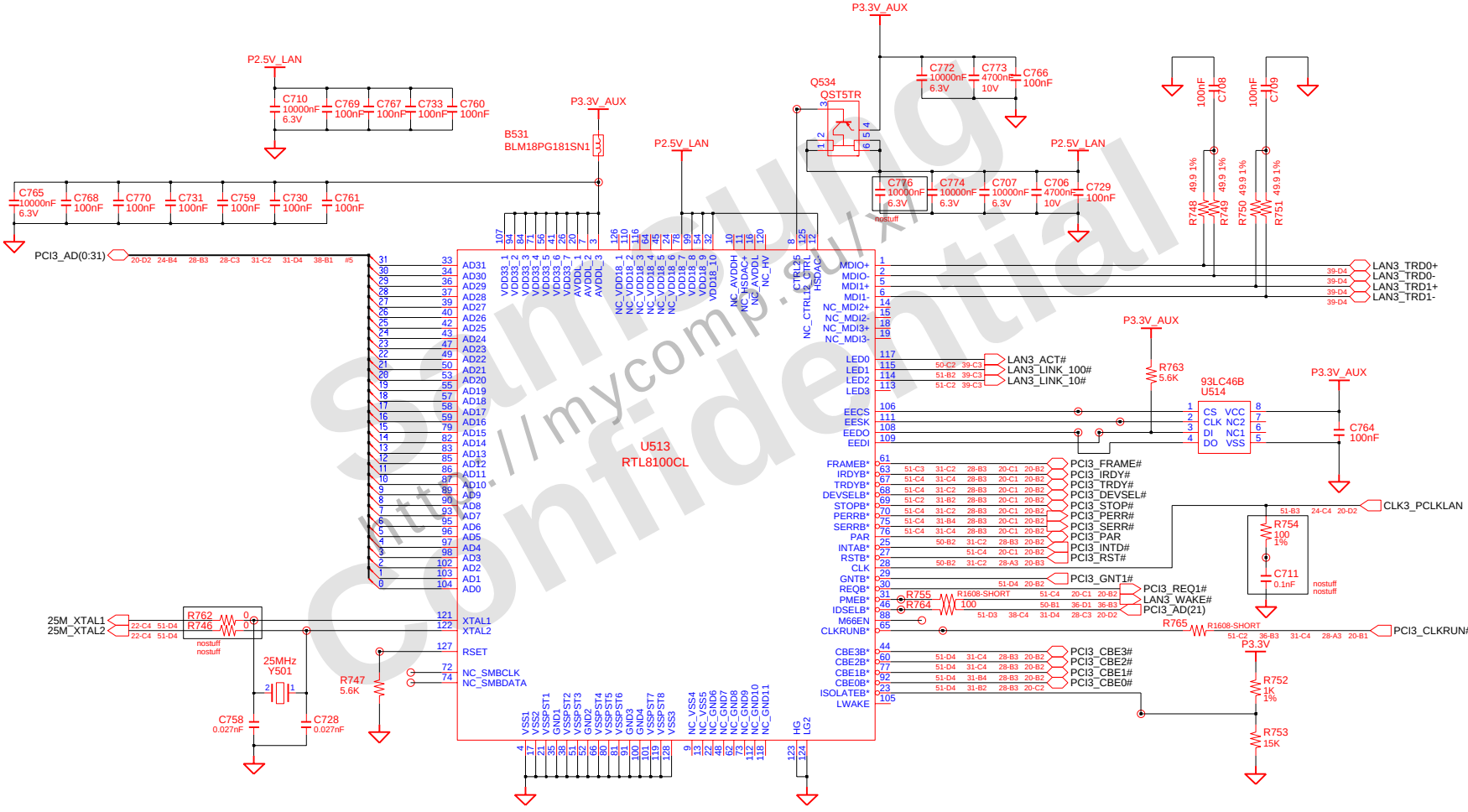
LAN Controller (Only 10/100M)



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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN LAN	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 38 OF 52	

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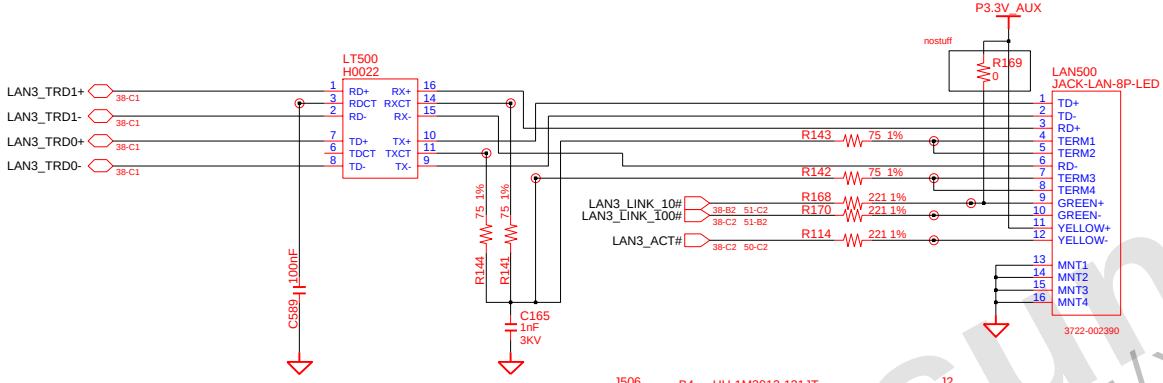
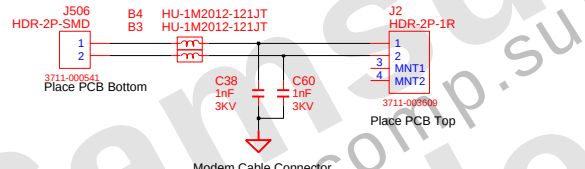
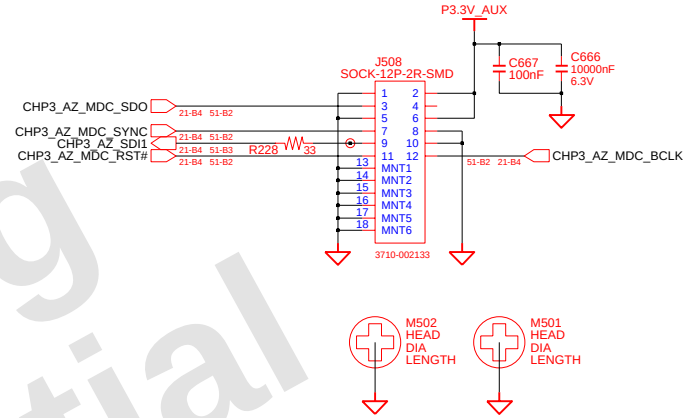
LAN Connector

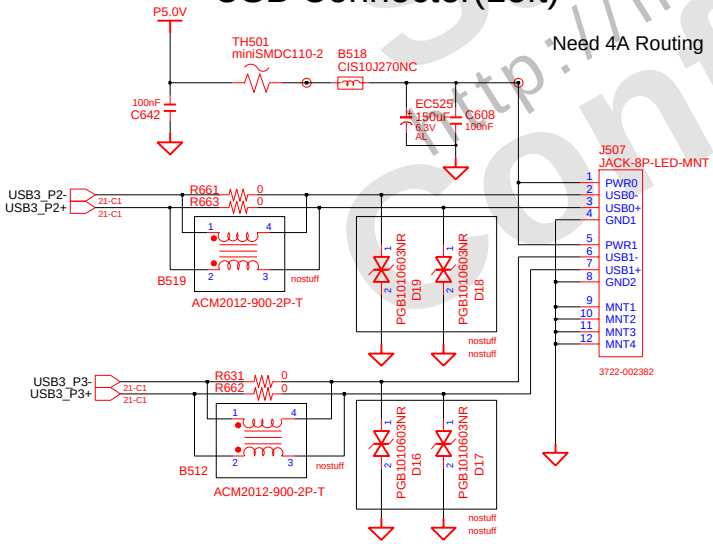




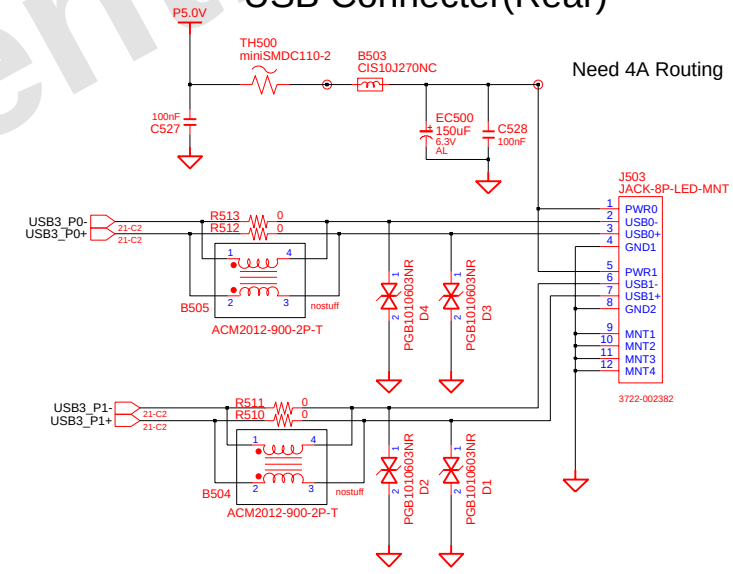
MDC Connecter



USB Connecter(Left)



USB Connecter(Rear)



DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN LAN & USB0 & MODEM Conn.	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 39 OF 52	

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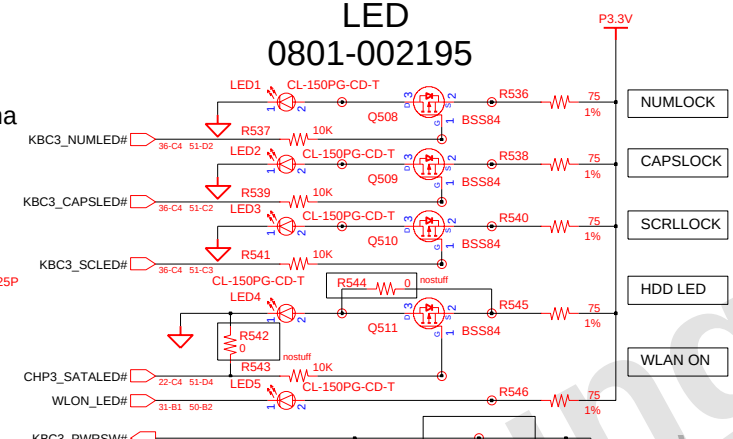
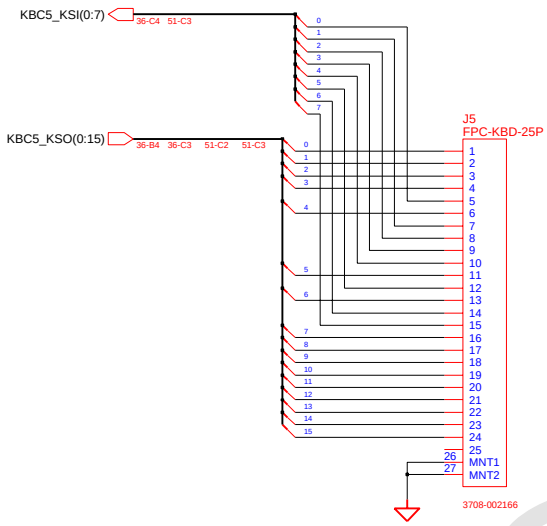
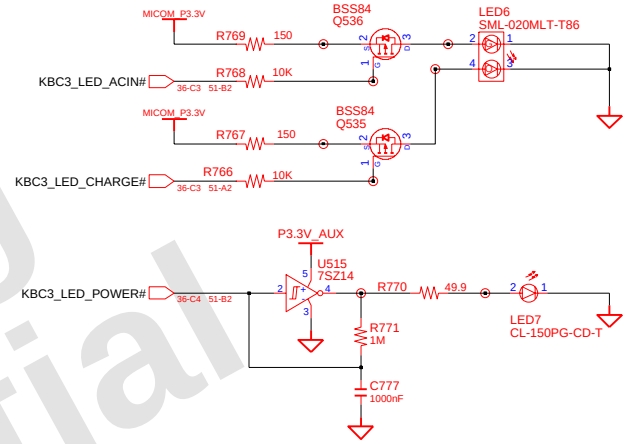
LED
0801-002195



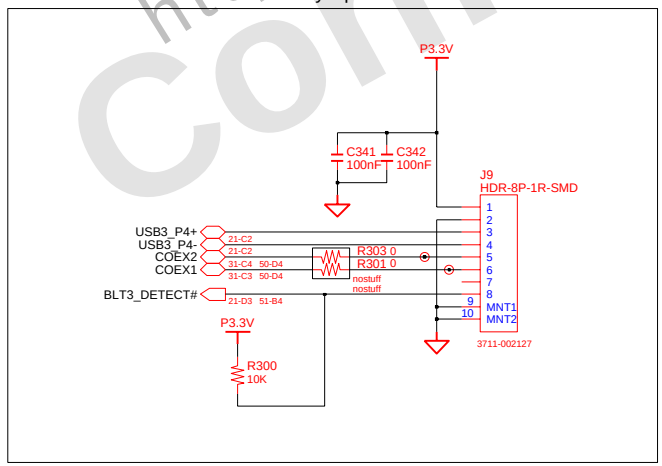
KEYBOARD
Same connector with Sedona

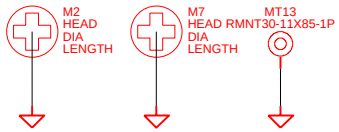


ADAPTERIN/CHARGING LED

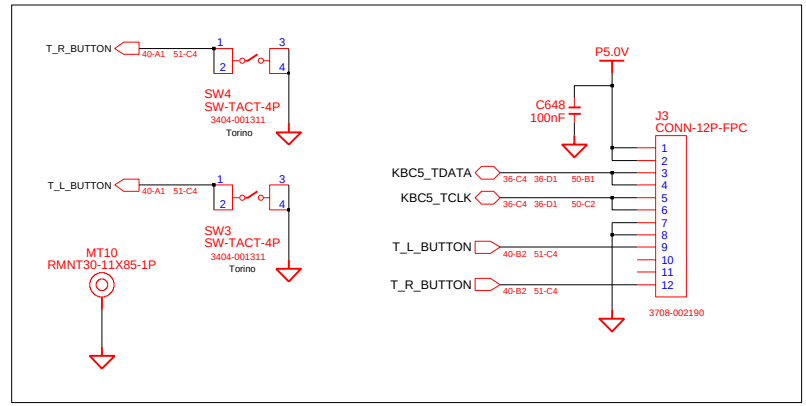


Bluetooth Interface
Factory Option





TOUCHPAD



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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN B'D TO B'D CONNECTOR	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 40 OF 52	

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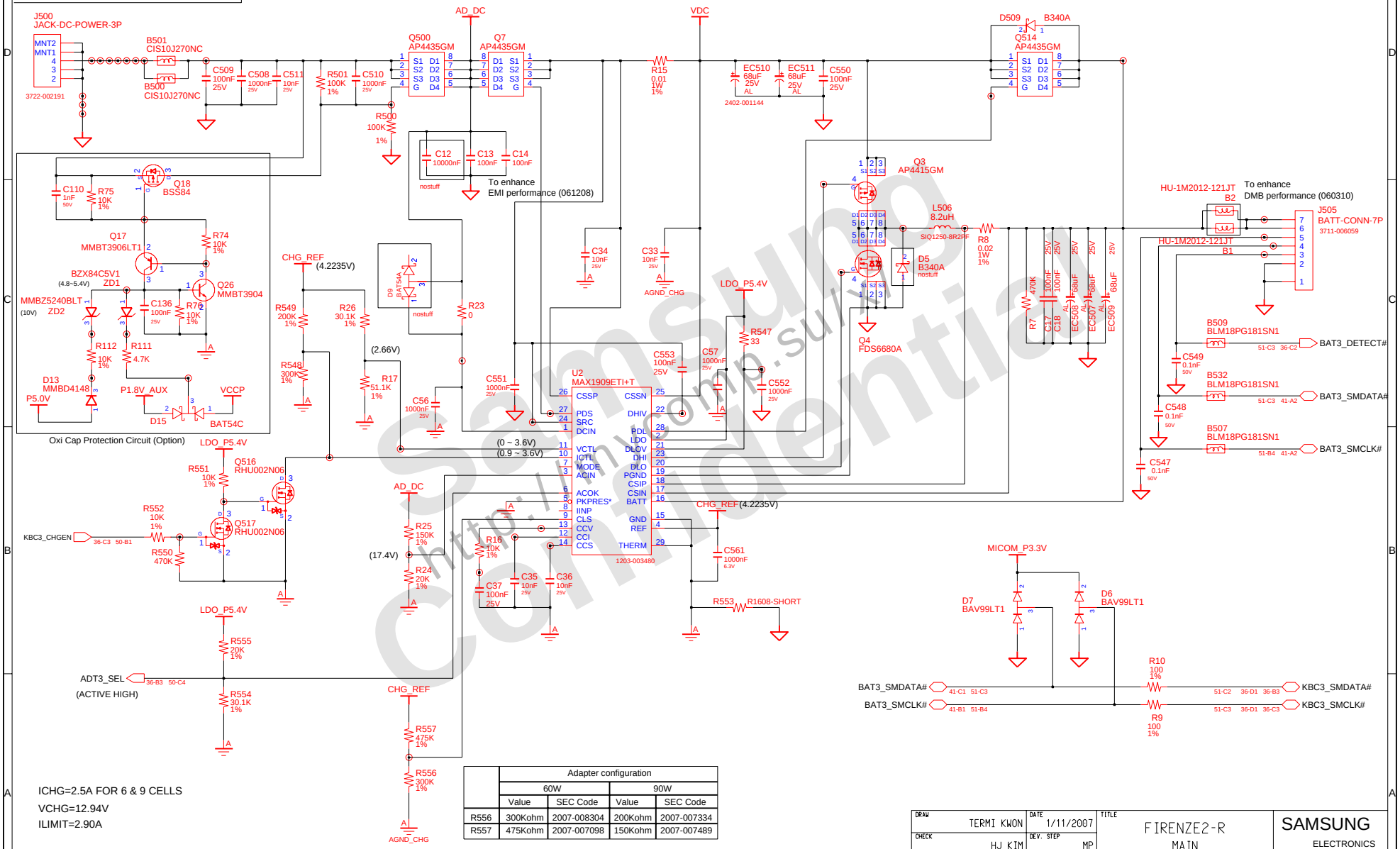
CHARGER & POWER MANAGEMENT



	Adapter configuration			
	60W		90W	
	Value	SEC Code	Value	SEC Code
R556	300Kohm	2007-008304	200Kohm	2007-007334
R557	475Kohm	2007-007098	150Kohm	2007-007489

ICHG=2.5A FOR 6 & 9 CELLS
VCHG=12.94V
ILIMIT=2.90A

DRAW	TERMI KWON	DATE	1/11/2007
CHECK	HJ KIM	DEV. STEP	MP
APPROVAL	SJ PARK	REV	1.0
MODULE CODE	undefined	LAST EDIT	January 11, 2007 8:27:44 PM

TITLE: FIRENZE2-R MAIN CHARGER

SAMSUNG ELECTRONICS

PART NO. BA41-00714A

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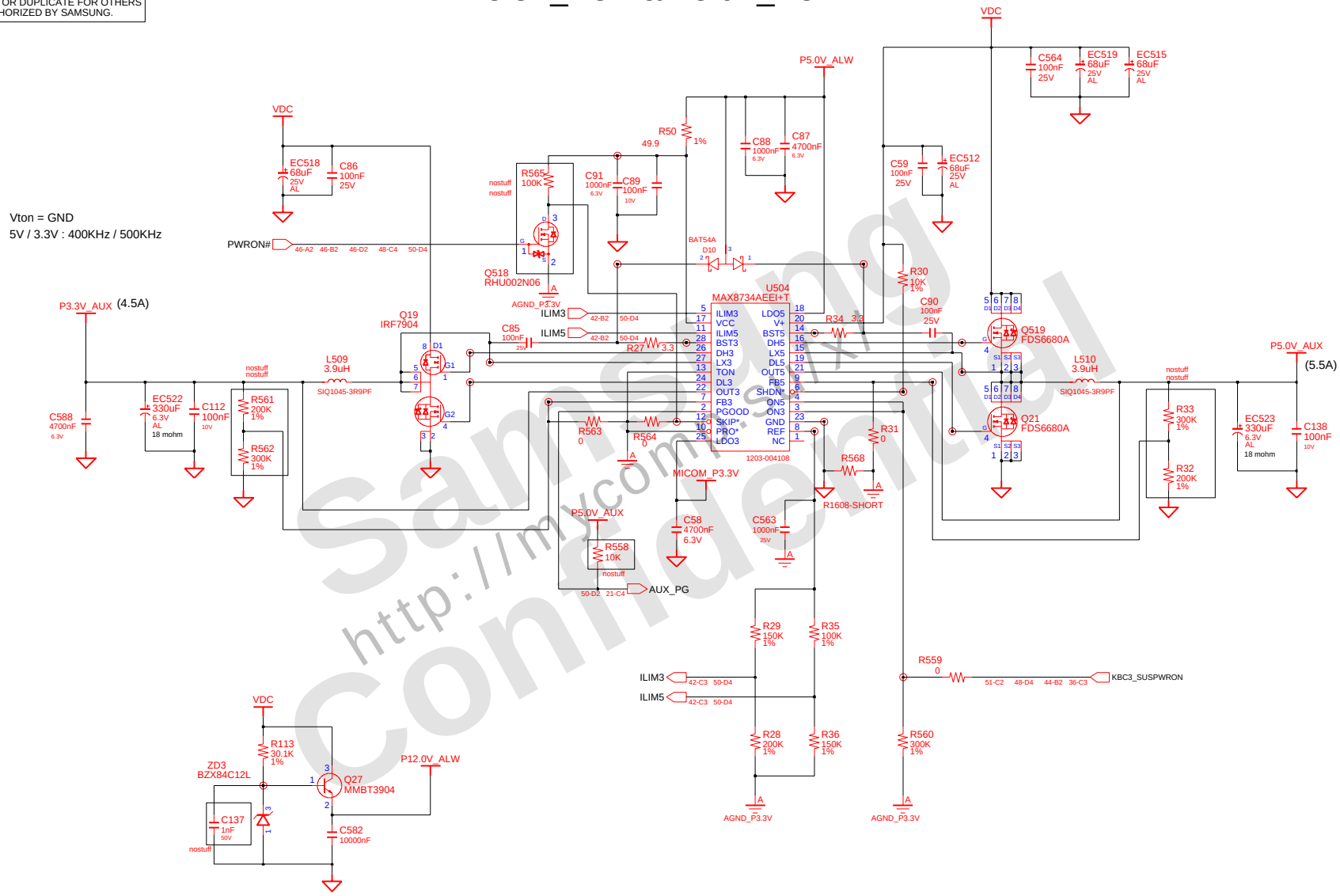
P3.3V_AUX & P5.0V_AUX



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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R POWER P3.3V ALWAYS & P5V_AUX	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 42 OF 52	

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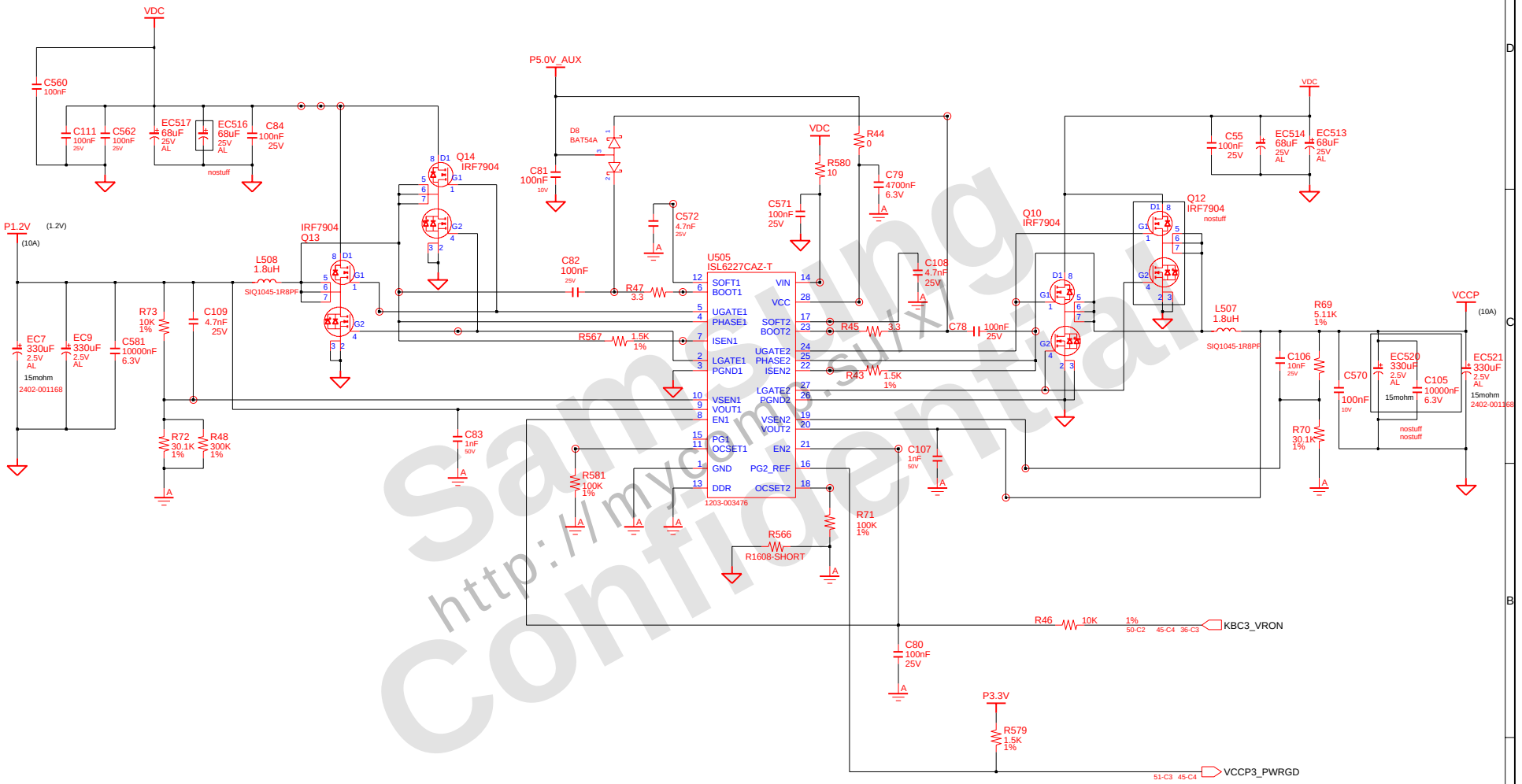
P1.2V(VCC_NB) & VCCP (1.05V)



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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R POWER P1.2V & VCCP	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 43 OF 52	

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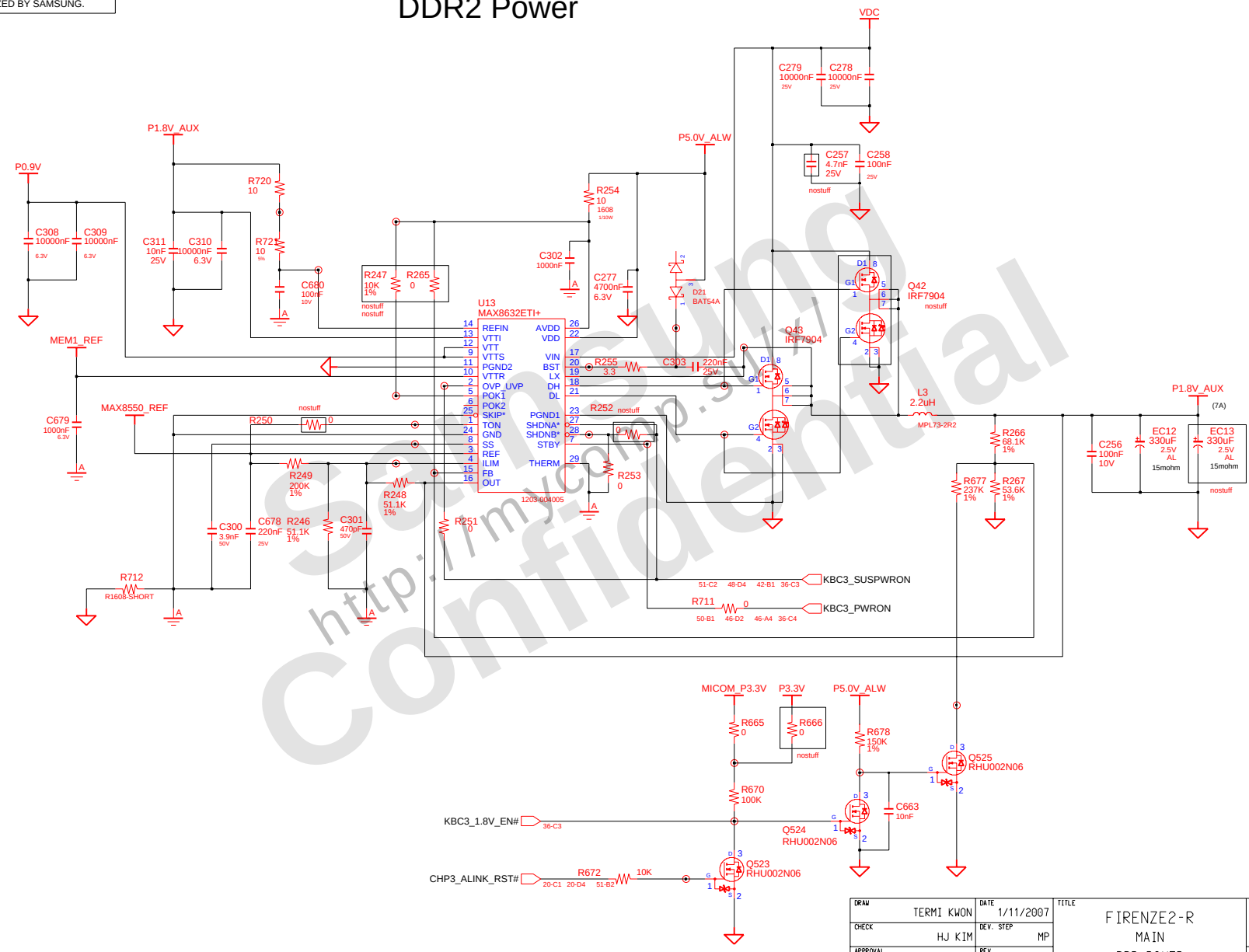
DDR2 Power



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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN DDR POWER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		PART NO.: BA41-00714A
APPROVAL: SJ PARK	REV: 1.0		
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 44 OF 52	

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CPU VRM [SEMTECH]

Stuff Q9, Q8, EC3, EC502, EC505
When use T7200 or higher CPU

Note : differential pairs

U4 SC452IMLTRT

DRAW	TERMI KWON	DATE 1/11/2007
CHECK	HJ KIM	DEV. STEP MP
APPROVAL	SJ PARK	REV 1.0
MODULE CODE	undefined	LAST EDIT January 11, 2007 8:27:44 PM

TITLE: FIRENZE2-R MAIN CPU POWER

SAMSUNG ELECTRONICS

PART NO. BA41-00714A

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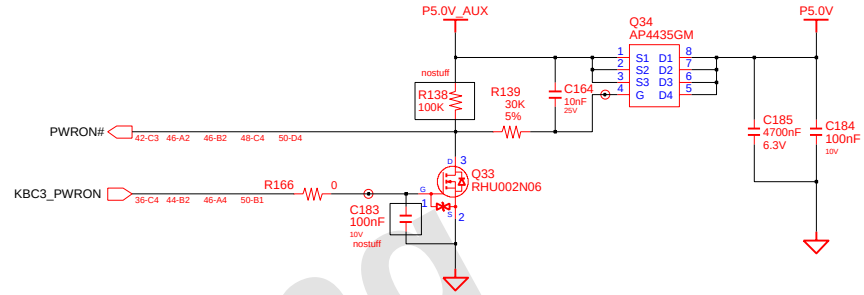
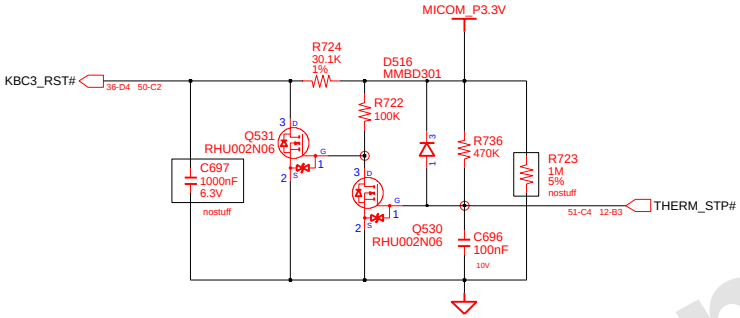
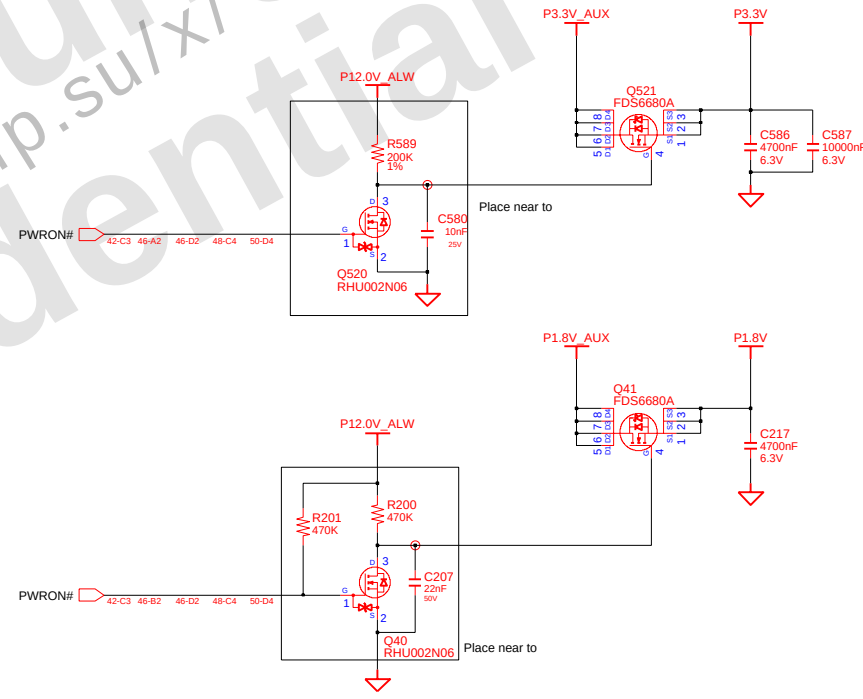
Switched Power On (P5V)



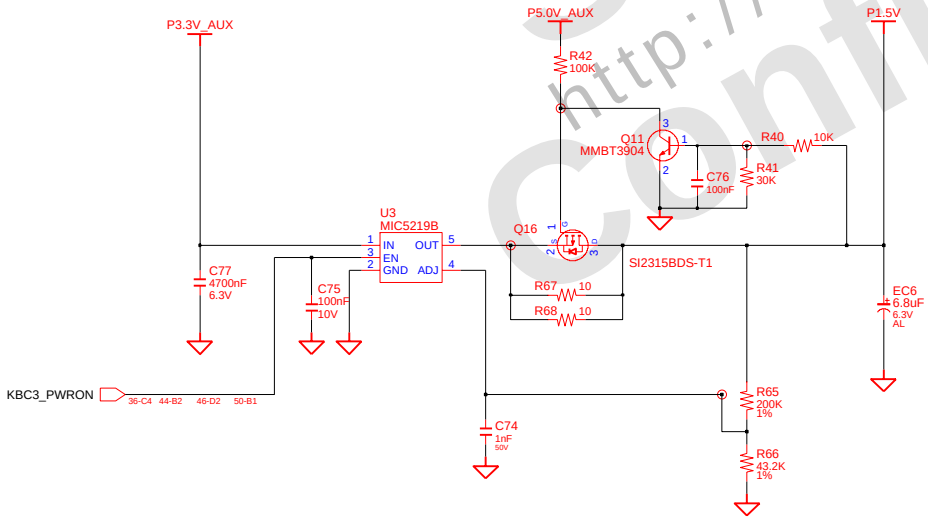
MICOM RESET



Switched Power On (P3.3V & 1.8V)



P1.5V POWER



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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAIN MICOM & SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 46 OF 52	

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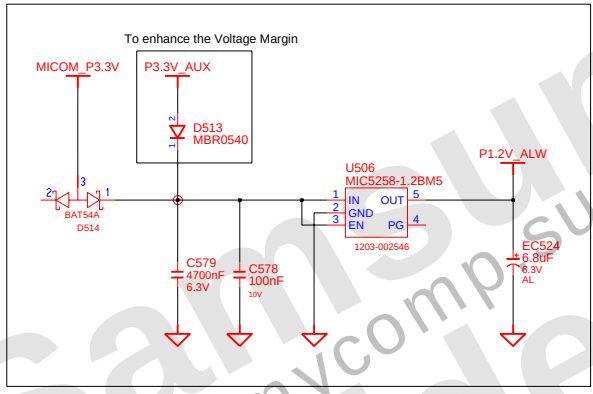

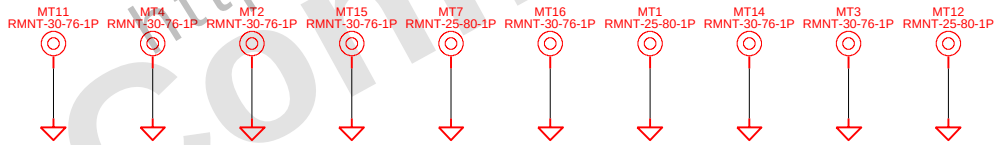

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP	P1.2V & P2.5V AUX POWER	
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 47 OF 52	

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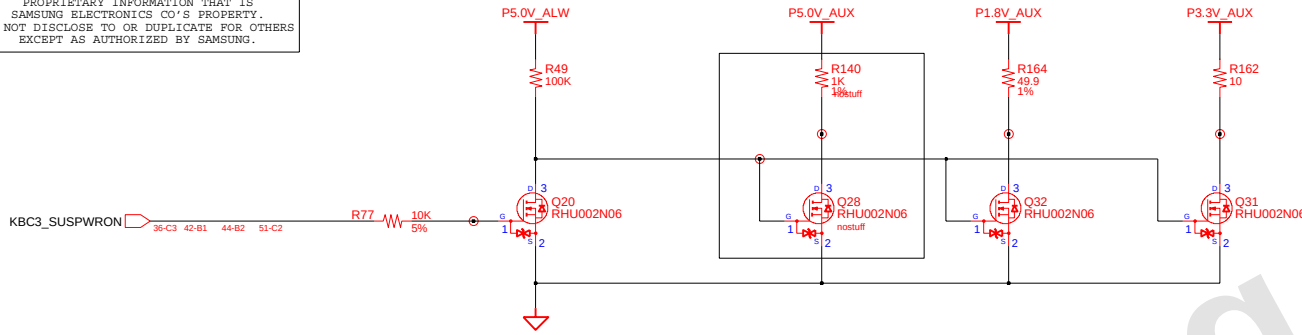
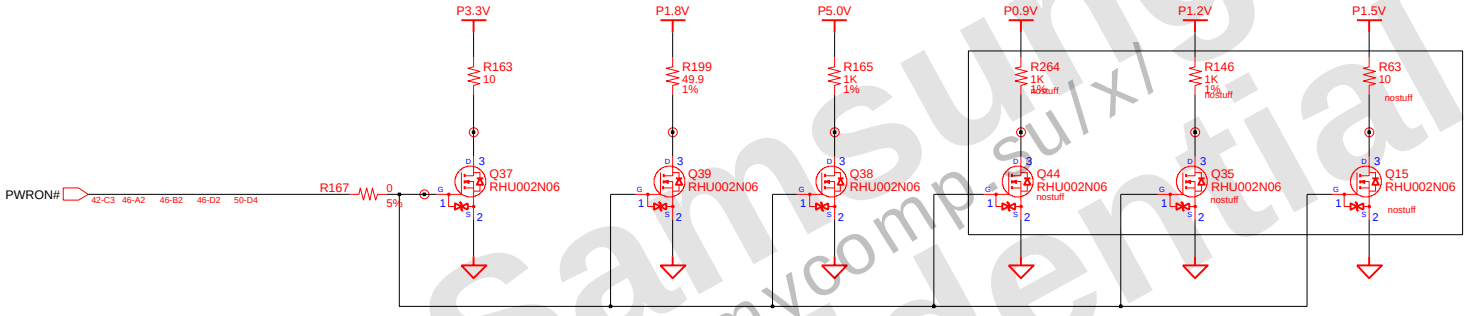
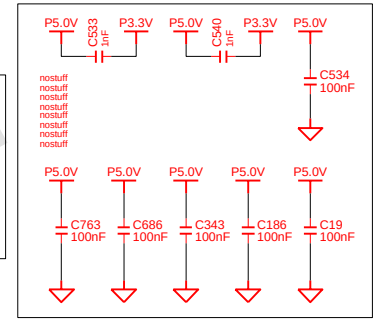
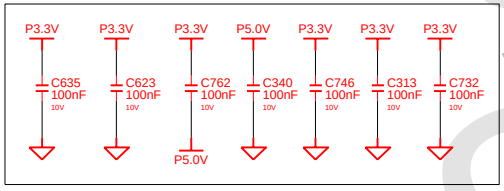


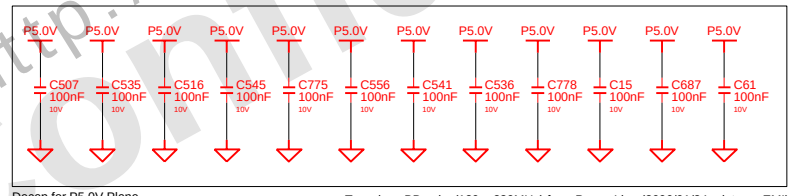




To enhance DMB performance(060206)

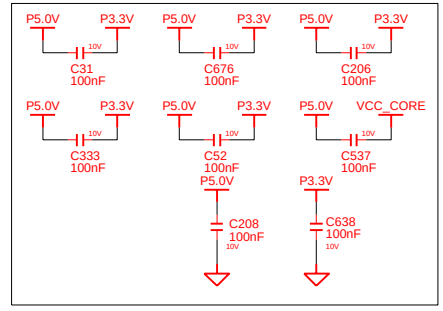


STICHING CAP



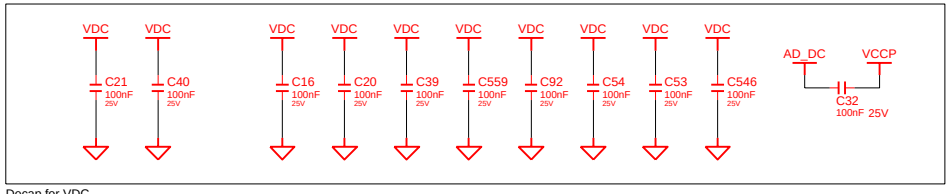
Decap for P5.0V Plane

To reduce BB noise(120 ~ 230MHz) from Power Line (2006/01/24 relate on EMI)



Stiching Cap for Power partition

To reduce BB noise(120 ~ 230MHz) from Power Partition points (2006/01/24 relate on EMI)



Decap for VDC

To reduce BB noise(120 ~ 230MHz) from Power Line (2006/01/24 relate on EMI)

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R MAINBD POWER ADAPT	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
MODULE CODE: undefined	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 48 OF 52	

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REV1

PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(YY/MM/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R	SAMSUNG ELECTRONICS	
CHECK: HJ KIM	DEV. STEP: MP			
APPROVAL: SJ PARK	REV: 1.0	TP	PART NO.: BA41-00714A	
MODULE CODE:	LAST EDIT: January 11, 2007 8:27:44 PM	PAGE 49 OF 52		

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COEX1
COEX2
ILIM3
ILIM5
MIC1_L
MIC1_R
PWRON#
TVO3_C
TVO3_Y

ODD5_A0
ODD5_A1
ODD5_A2
PC_BEEP

AC_SDOUT
ADT3_SEL

CPU1_TCK
CPU1_TDI
CPU1_TMS
CRT3_RED

HP_OUT_L
HP_OUT_R

CLK3_ICH14
CLK3_NB14M
CLK3_USB48

CRT3_BLUE
AUX_PG

KBC3_A20G
KBC3_RST#
KBC3_VRON
KBC5_TCLK
LAN3_ACT#

CRT3_GREEN
CRT5_HSYNC
CRT5_VSYNC

ODD5_CS1#
ODD5_CS3#
ODD5_D(0)
ODD5_D(1)
ODD5_D(2)
ODD5_D(3)
ODD5_D(4)
ODD5_D(5)
ODD5_D(6)
ODD5_D(7)
ODD5_D(8)
ODD5_D(9)
ODD5_DREQ
ODD5_IOR#
ODD5_IOW#

ODD5_IRQ
PCI3_PAR
SMB3_CLK

JCK_SENS_A
KBC3_CHGEN
KBC3_PWRGD
KBC3_PWRON
KBCS_TDATA

PCI3_RST#
SMB3_DATA
VGA5_DDCC
VGA5_DDCD
WLON_LED#
AUD3_EAPD#
CBS3_A_D_2
CBS3_CCD1#
CBS3_CCD2#
CBS3_CGNT#
CBS3_CINT#
CBS3_CREQ#
CBS3_CRST#

LAN3_WAKE#

LCD3_VDDEN
LINE_OUT_L
LINE_OUT_R

CBS3_CCLK
CBS3_CPAR
CBS3_CVS1
CBS3_CVS2
CBS3_SPKR
CHP3_SPKR
CLK3_FM48

ODD5_D(10)
ODD5_D(11)
ODD5_D(12)
ODD5_D(13)
ODD5_D(14)
ODD5_D(15)
ODD5_DACK#
ODD5_IORDY
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PCI3_AD(1)
PCI3_AD(2)
PCI3_AD(3)

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DRAW: TERMI KWON	DATE: 1/11/2007	TITLE: FIRENZE2-R TP	SAMSUNG ELECTRONICS
CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO. BA41-00714A
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- PCI3_INTC#
- PCI3_INTD#
- PCI3_IRDY#
- PCI3_PERR#
- PCI3_REQ0#
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- PCI3_REQ2#
- PCI3_RSTF#
- PCI3_SERR#
- PCI3_STOP#
- PCI3_TRDY#
- PLT3_RSTF#
- THERM_STP#
- T_L_BUTTON
- T_R_BUTTON
- VGA3_HSYNC
- VGA3_VSYNC
- AUD5_SPK_L+
- AUD5_SPK_L-
- AUD5_SPK_R+
- AUD5_SPK_R-
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- CBS3_A_A_19
- CBS3_A_D_14
- CBS3_CAD(0)
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- CBS3_VPPEN1
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- CHP3_SBPME#
- CHP3_SERIRQ
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- CHP3_SLPS5#
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- 25M_XTAL2
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- SPI3_CS#
- SPI3_MISO
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- CBS3_VCCSEN#
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- CHP3_AZ_SDI1
- CHP3_BIOSWP#
- CHP3_CPUSTP#
- KBC3_NBPWRGD
- CLK3_33M_MIN
- CLK3_PCLKLAN
- STRAP_USB48
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- CPU1_BREQ#
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- CPU1_BSEL1
- CPU1_BSEL2
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- CPU1_DPSLP#
- CPU1_FERR#
- CPU1_SLP#
- CPU1_TRST#

- CPU1_STPCLK#
- CPU2_THERMDA
- CPU2_THERMDC
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- ITP3_DBRESET#
- JCK_SENS_HP#
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- KBC3_EXTSMI#
- KBC3_FANCTRL
- KBC3_NUMLED#
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- KBC3_RSMRST#
- KBC3_RUNSCI#
- KBC3_SMDATA#
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- LPC3_LFRAME#

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- MIC1_VREFO_R
- MIO3_BUTTON#
- PCI3_CLKRUN#
- PCI3_DEVSEL#
- CBS3_CCLKRUN#
- CBS3_CDEVSEL#
- CBS3_MD_DATA1
- CBS3_MD_DATA2
- CBS3_MD_DATA3
- CBS3_MD_VCCEN
- CHP3_DPRSLPVR
- CHP3_SUSSTAT#
- CPU1_PWRGDCPU
- CPU1_VCCSENSE
- CPU1_VSSSENSE
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- KBC3_CAPSLED#
- KBC3_SUSPWRON
- KBC3_WAKESCI#
- LAN3_LINK_10#
- LCD3_BKLTCTRL
- LCD3_BKLTEN
- LCD3_BKLTON
- CBS3_MD_XD_ALE
- CBS3_MD_XD_CE#
- CBS3_MD_XD_CLE
- CBS3_MD_XD_WP#
- CLK3_PCLKMICOM
- CPU1_THRMTRIP#
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- VRM3_CPU_PWRGD
- CHP3_ALINK_RST#
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- CHP3_AZ_MDC_SDO
- KBC3_LED_POWER#
- CBS3_MD_DATA4_XD
- CBS3_MD_DATA5_XD
- CBS3_MD_DATA6_XD
- CBS3_MD_DATA7_XD
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- CBS3_MS_BS_SD_CMD
- KBC3_THERM_SMDATA
- CBS3_SD_CD#_XD_CD#
- CBS3_MS_INS#_XD_CD#
- CBS3_SD_WP#_XD_R_B#
- CBS3_MD_DATA0_MS_SDIO
- CHG_REF

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- AVDD_AUD
- AD_DC
- AD_DC
- AD_DC
- AD_DC
- AD_DC
- AVDDQ
- AMP_VDD
- AMP_VDD
- AVDD
- AGND_AUD
- AGND_AUD
- AGND_AUD
- AGND_AUD
- AGND_CHG
- AGND_P3.3V
- CGND
- C_AGND
- CB_VCCA
- CB_VPPA

- CB_MD_VCC
- D_AGND
- GROUND
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- INV_VDC
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- LCD_VDD3V
- LDO_P5.4V
- MEM1_REF
- MAX8550_REF
- MICOM_P3.3V
- MICOM_P3.3V
- P0.9V
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- P1.2V
- P1.5V
- P1.5V
- P1.8V
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- P3.3V

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CHECK: HJ KIM	DEV. STEP: MP		
APPROVAL: SJ PARK	REV: 1.0		PART NO.: BA41-00714A
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P5.0V
P5.0V
PLLVDD18

VCC_CRT

VCC_CORE
VCC_CORE
VCC_CORE
VCC_CORE
VCC_CORE

PRTC_BAT
P1.2V_ALW

P1.8V_AUX
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VDC
VCCP
VCCP
VCCP
VCCP
VCCP

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C2 0.01nF 0.5pF
C3 0.018nF
C4 0.022nF
C5 0.027nF
C6 0.047nF
C7 0.0033nF

C500 0.1nF
C501 0.01nF 0.5pF
C502 0.018nF
C503 0.022nF
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C506 0.0033nF

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