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RIMINI

CPU : INTEL YONAH-ULV
 Chip Set : INTEL 945GMS
 Remarks : 1 Spindle

Model Name	: RIMINI MAIN
	<i>With Docking / Without Docking</i>
PCB Part No	: BA41-00680A (TPT) BA41-00683A (GCE)
Dev. Step	: SR
Revision	: 1.0
T.R. Date	: 2006.05.11

DRAW	CHECK	APPROVAL
JULIO	HK PARK	JS EUH

Table of Contents

Page. 1	-----	COVER
Page. 2	-----	OPERATION BLOCK DIAGRAM
Page. 3	-----	POWER SEQUENCE
Page. 4	-----	CLOCK DISTRIBUTION
Page. 5	-----	BOARD INFORMATION
<i>W/O Dock</i> Page. 6	-----	CLOCK GENERATOR (CK-410M+)
Page. 7~8	---	YONAH-ULV
Page. 9	-----	THERMAL MONITOR
Page. 10~13	-	CALISTOGA-SFF (INTEL945GMS)
Page. 14~15	-	DDR2 ON BOARD
Page. 16	---	DDR2 TERMINATION
Page. 17	---	DDR2 SODIMM
<i>W/O Dock</i> Page. 18~21	-	ICH7-M
Page. 22	---	BIOS CODE
Page. 23	---	LCD(LVDS) CONN.
Page. 24	---	CRT CONN.
Page. 25	---	HDD CONNECTOR
<i>W/O Dock</i> Page. 26	---	MICOM
Page. 27~29	-	LAN (GIGABIT) & MDC
Page. 30	---	USB, BLUETOOTH & DMB
Page. 31	---	MINI-CARD (GOLAN, WIBRO, SIM CARD)
Page. 32~33	-	CARDBUS CONTROLLER (R5C843)
Page. 34	---	CF SOCKET & 3IN1 SUB
Page. 35	---	AZALIA AUDIO CODEC
<i>W/O Dock</i> Page. 36	---	AUDIO AMP & JACK
Page. 37	---	KBD CONN & DEBUG PORT
Page. 38	---	CHARGER
Page. 39	---	P3.3V AUX & P5V_AUX
Page. 40	---	DDR2 POWER
Page. 41	---	1.5V AUX & VCCP POWER
Page. 42	---	CPU VRM POWER (VCC_CORE)
Page. 43	---	SWITCHED POWER
Page. 44	---	LED FPC CONNECTOR POWER S/W
<i>W/O Dock</i> Page. 45	---	X series DOCKING CONN
<i>W/O Dock</i> Page. 46	---	DOCKING LPC
<i>W/O Dock</i> Page. 47	---	PANELINK TRANSMITTER
Page. 48	---	MOUNT HOLE
Page. 49~50	-	TEST POINTS

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR	MAIN		
APPROVAL	JS, EUR	REV	1.0	COVER		PART NO. BA41-00680(3)A
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	1	OF 50

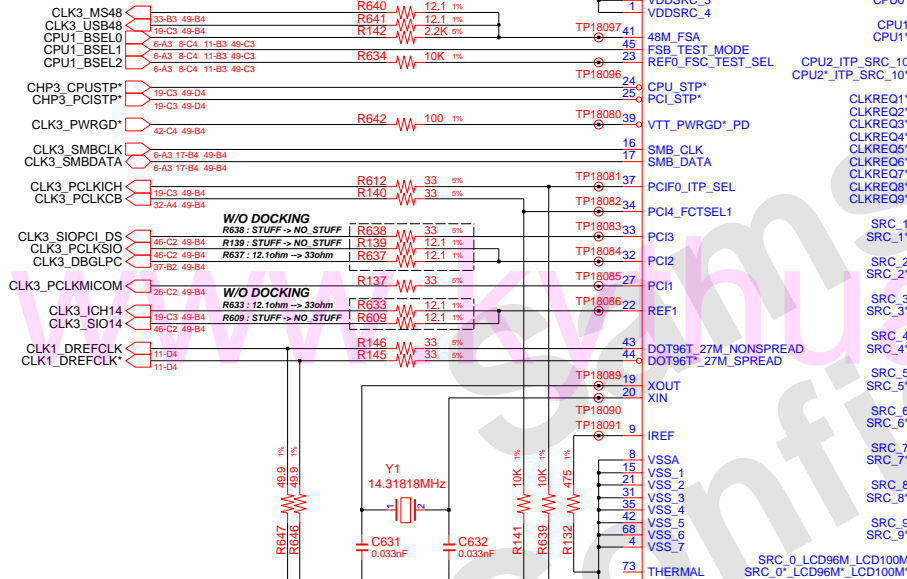
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CK410M+

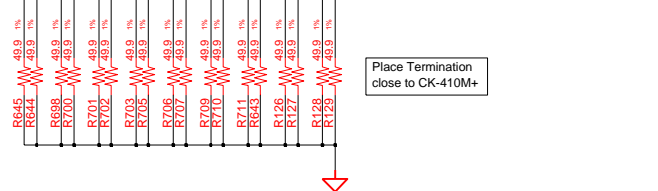
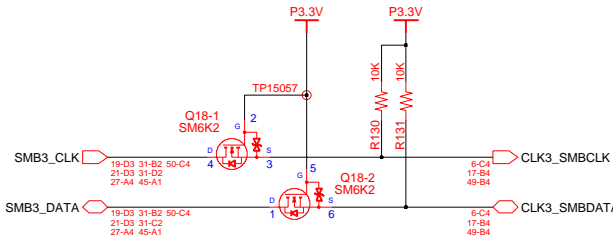
- FSB Frequency Select

CPU	FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	0	266 MHz
0	0	1	0	333 MHz
0	1	0	0	200 MHz
0	1	1	0	400 MHz
1	0	0	1	133 MHz
1	0	1	0	100 MHz
1	1	0	1	166 MHz
1	1	1	1	RSVD



Trace Width *2
 1205-002799 : SILEGO
 1205-001801 : SILEGO
 1205-002800 : CYPRESS
SMBUS Address "D2h"

CK-410M+	
w/ CLKREQ	ICS954305
w/ SS Clock	SL38LP455
	CY28447

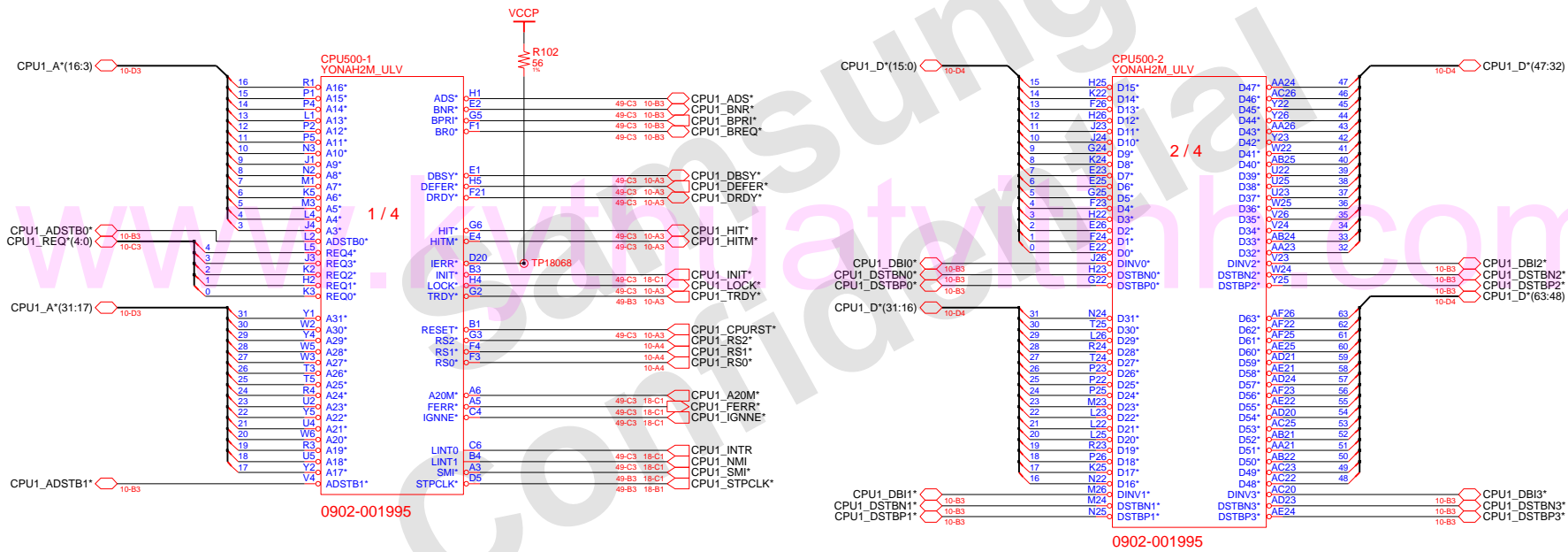


DRAW	DATE	TITLE	RIMINI MAIN CLOCK GENERATOR	SAMSUNG ELECTRONICS
JULIO	5/11/2006			
CHECK	HK, PARK	DEV. STEP	SR	PART NO. BA41-00680(3)A
APPROVAL	JS, EUR	REV	1.0	
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE 6 OF 50

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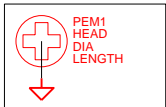
YONAH-ULV CPU (Single Core)

YONAH-ULV CPU S-SPEC			
1.2GHz	(C1)	QKGD	0902-001995
1.06GHz	(C1)	QKGE	0902-002031
933MHz	(C1)	Q5XY	



0902-001995

0902-001995



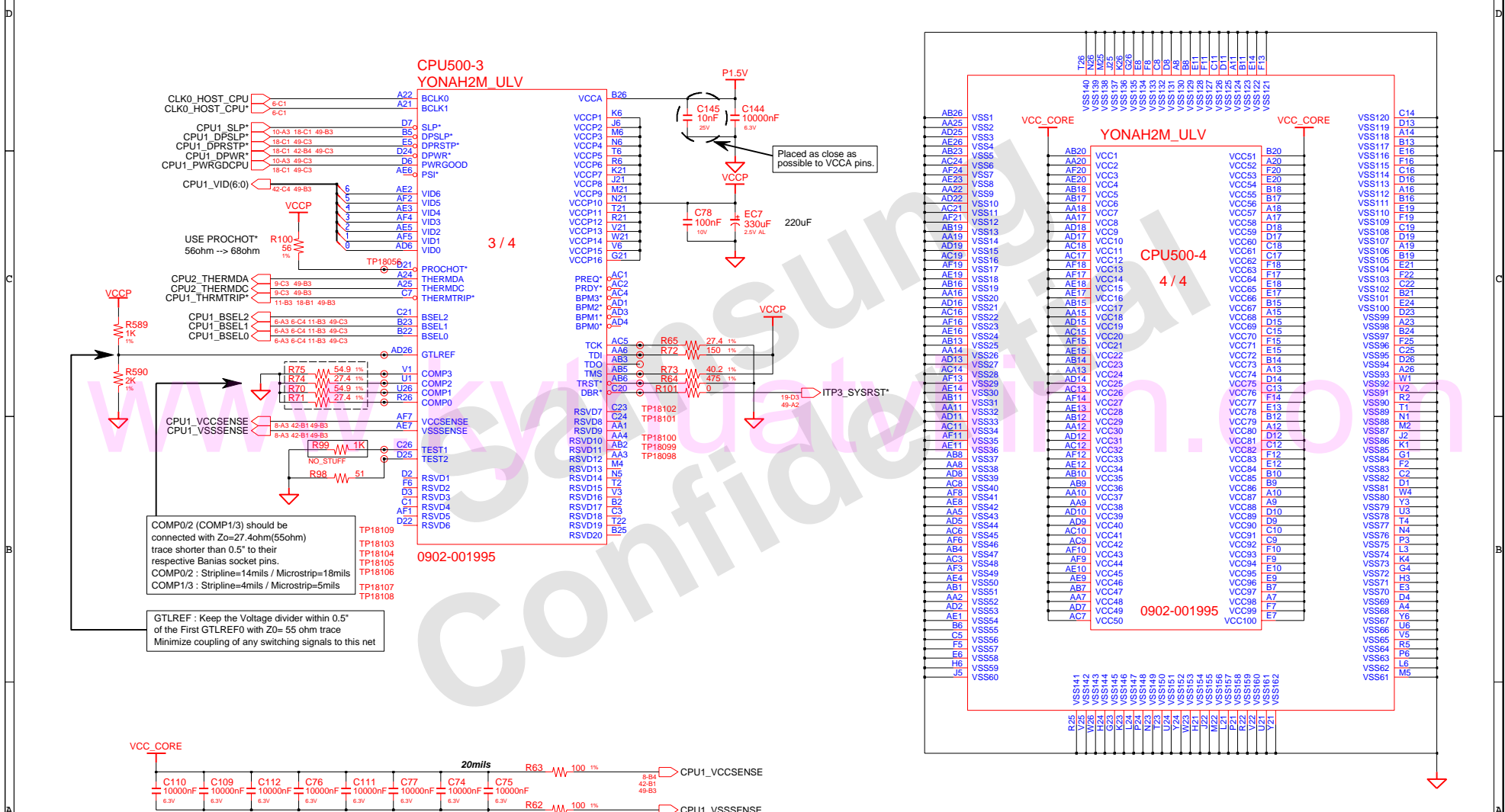
TOP : 5.5mm PAD
 BOTTOM : 4.5mm PAD (SMT)
 HOLE size : 2.95mm
 Height : 1.5mm

BA61-01090A|screw-gap130-41-h0250

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR	MAIN		
APPROVAL	JS, EUR	REV	1.0	YONAH-ULV (1/2)		PART NO. BA41-00680(3)A
MODULE CODE		LAST EDIT		May 11, 2006 10:24:27 PM		PAGE 7 OF 50

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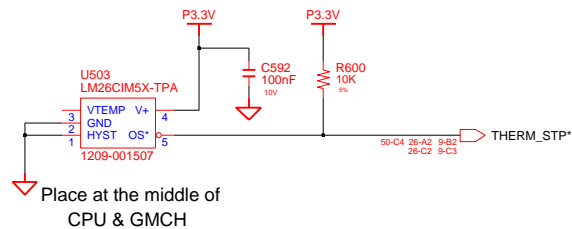
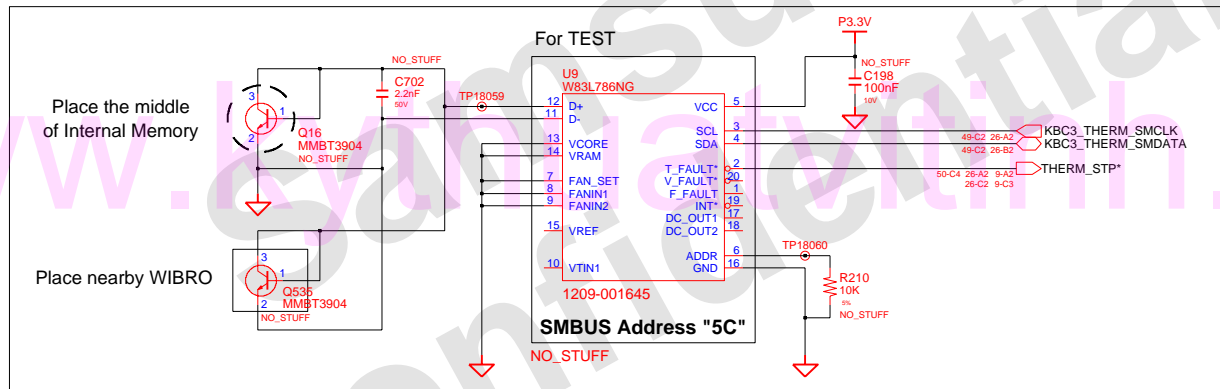
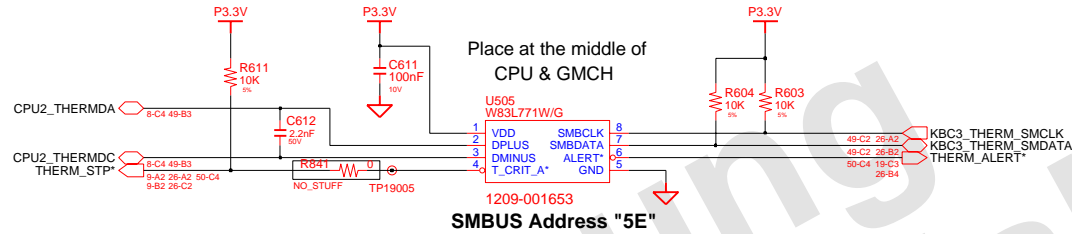
YONAH-ULV CPU (Single Core)



DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR	MAIN		
APPROVAL	JS, EUR	REV	1.0	YONAH-ULV (2/2)		PART NO. BA41-00680(3)A
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	8	OF 50

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Thermal Monitor

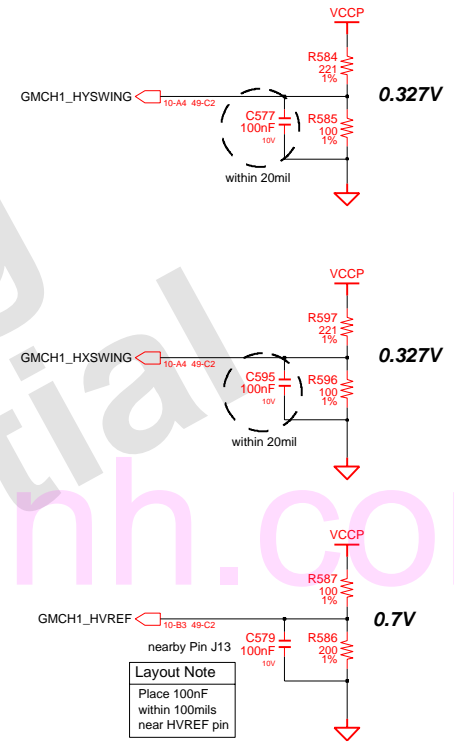
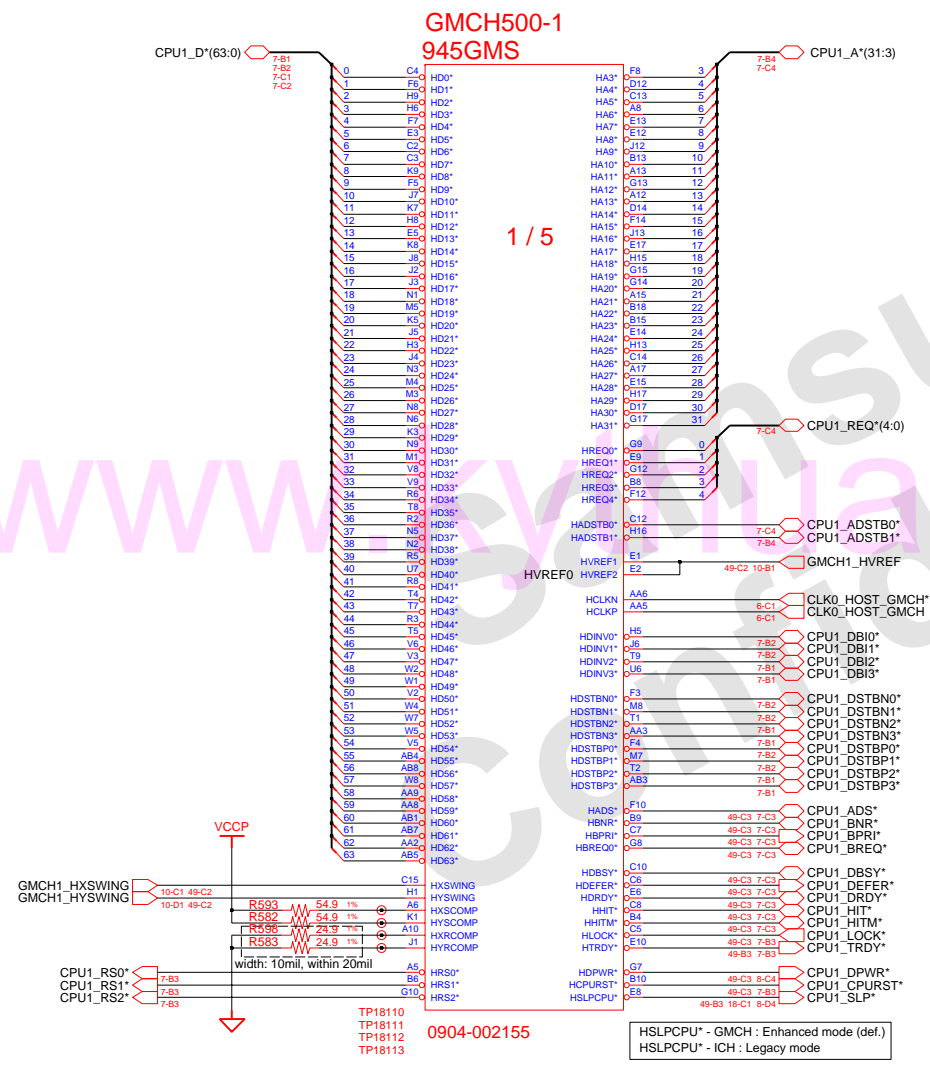


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CHECK	HK, PARK	DEV. STEP	SR	THERMAL MONITOR		
APPROVAL	JS, EUR	REV	1.0	PART NO. BA41-00680(3)A		
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	9	OF 50

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CALISTOGA-SFF

A3 Stepping : QK64



TP18110
 TP18111
 TP18112
 TP18113

0904-002155

HSLPCPU* - GMCH : Enhanced mode (def.)
 HSLPCPU* - ICH : Legacy mode

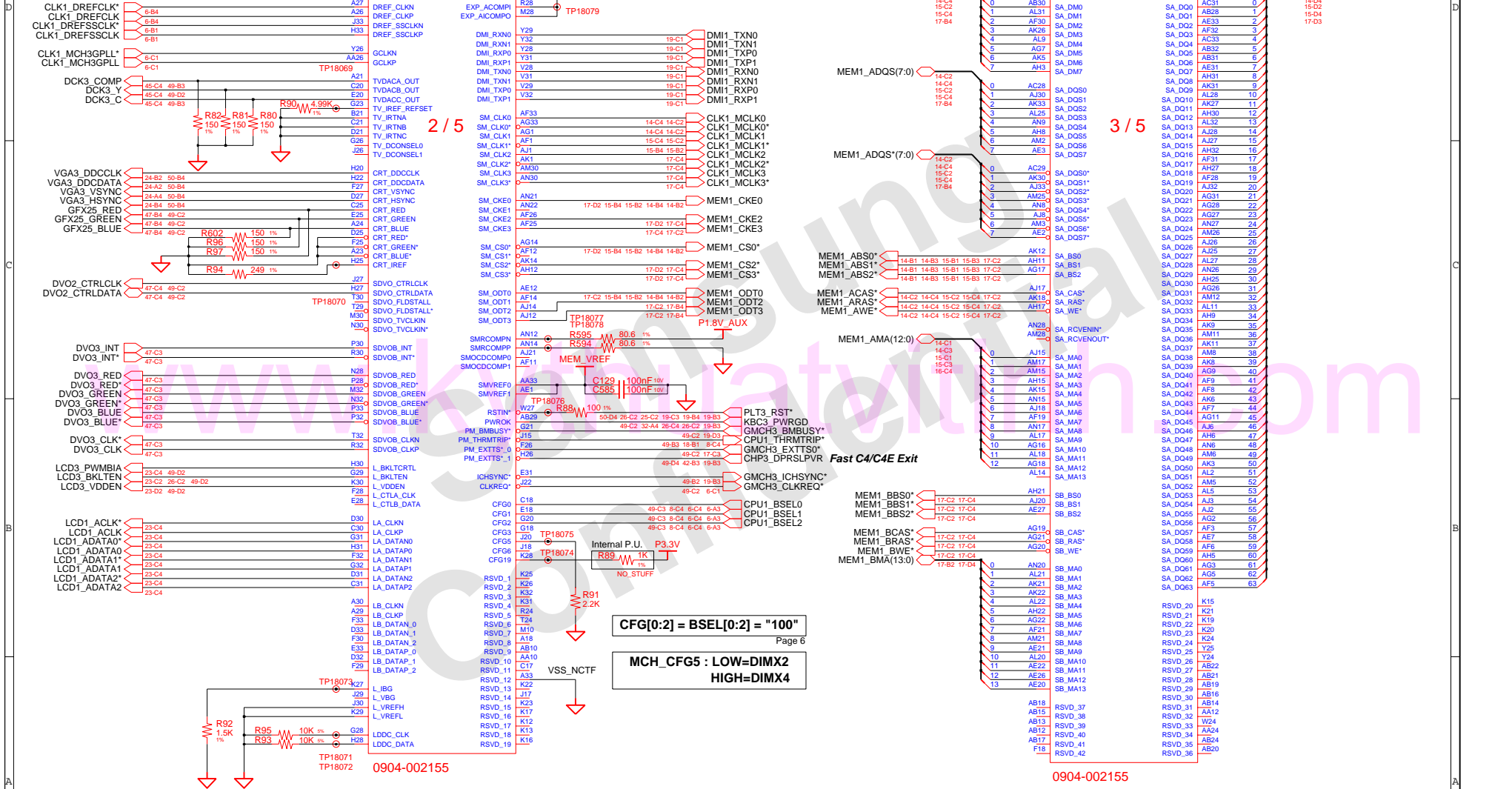
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CHECK	HK, PARK	DEV. STEP	SR	CALISTOGA-SFF (1/4)		
APPROVAL	JS, EUR	REV	1.0	PART NO. BA41-00680(3)A		
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	10	OF 50

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CALISTOGA-SFF

GMCH500-2 945GMS

GMCH500-3 945GMS



CFG[0:2] = BSEL[0:2] = "100"
 MCH_CFG5 : LOW=DIMX2
 HIGH=DIMX4

Current Setting (def. : default Option)		
CFG#	Low	High
CFG(5)	DMIX2 (default)	DMIX4
CFG(6)	Reserved	
CFG(19)	DMI Lane Normal	DMI Lane Reversal

DRAW	DATE	TITLE	PART NO.	
JUL10	5/11/2006	RIMINI MAIN	SAMSUNG ELECTRONICS	
CHK	DEV. STEP	SR	BA41-00680(3)A	
APPROVAL	REV	1.0	CALISTOGA-SFF (2/4)	
MODULE CODE	LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	11 OF 50

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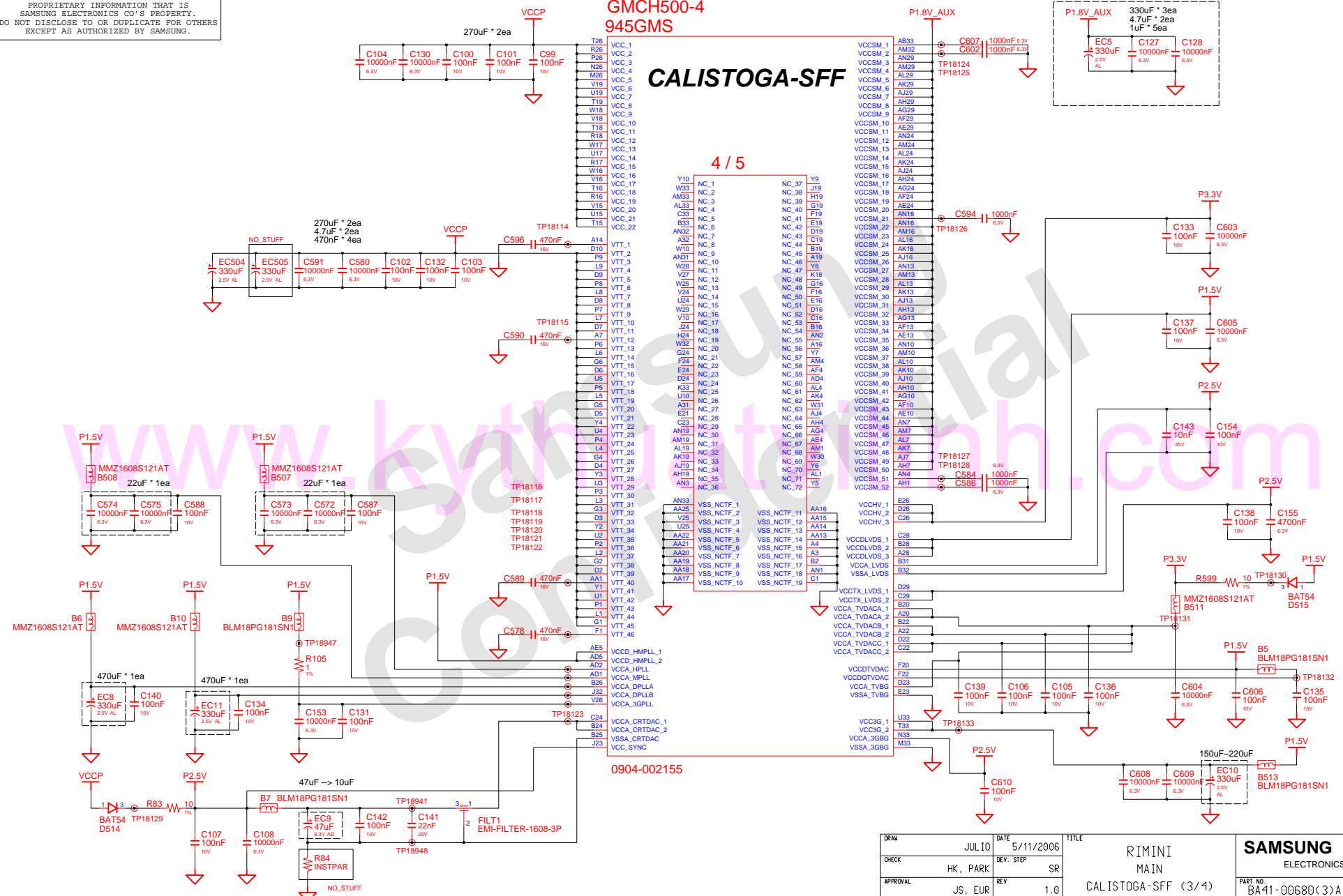
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GMCH500-4
945GMS

CALISTOGA-SFF

4 / 5

0904-002155

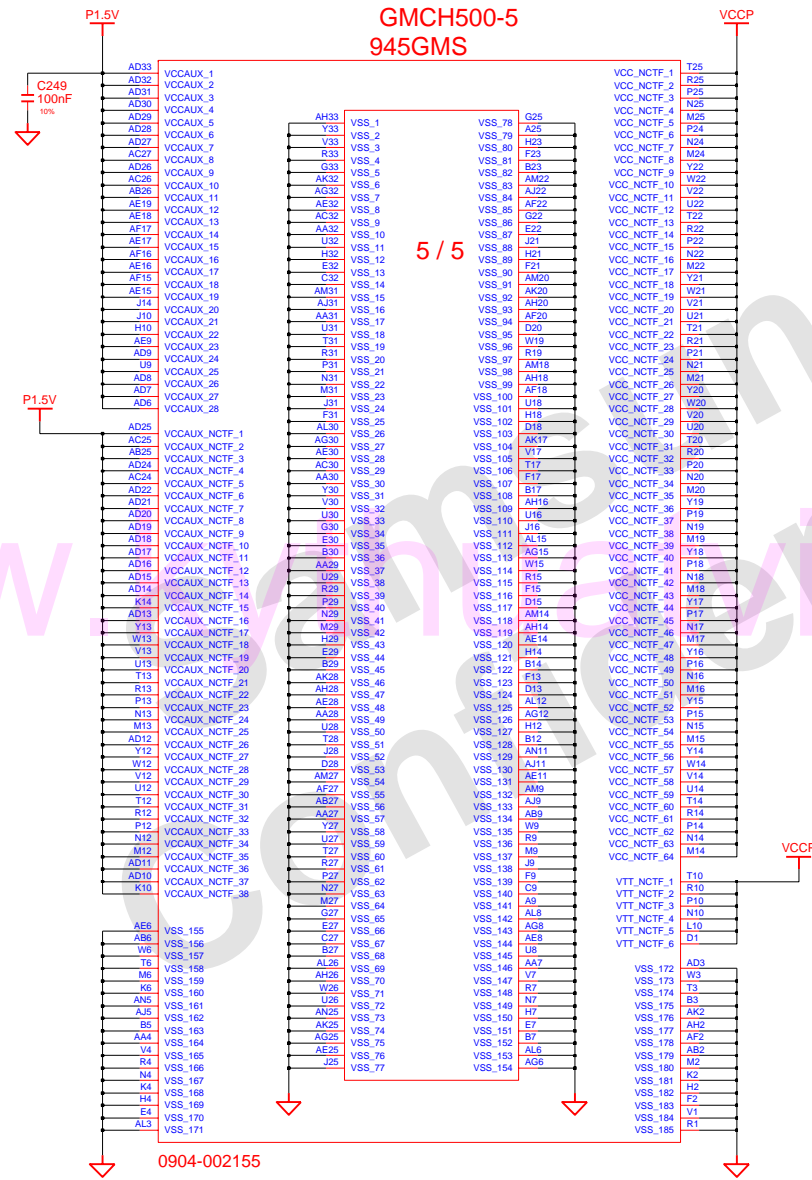


DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR	CALISTOGA-SFF (3/4)		
APPROVAL	JS, EUR	REV	1.0	PART NO. BA41-00680(3)A		
MODULE CODE	LAST EDIT		May 11, 2006 10:24:27 PM		PAGE 12 OF 50	

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CALISTOGA-SFF



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CHECK	HK, PARK	DEV. STEP	SR	CALISTOGA-SFF (4/4)		
APPROVAL	JS, EUR	REV	1.0	PART NO. BA41-00680(3)A		PAGE 13 OF 50
MODULE CODE	LAST EDIT		May 11, 2006 10:24:27 PM			

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DDR2 ON BOARD MEMORY

1. 512Mbit DDR2-533MHz x16 I/O

SAMSUNG: K4T51163QB-ZCD5

1105-001680

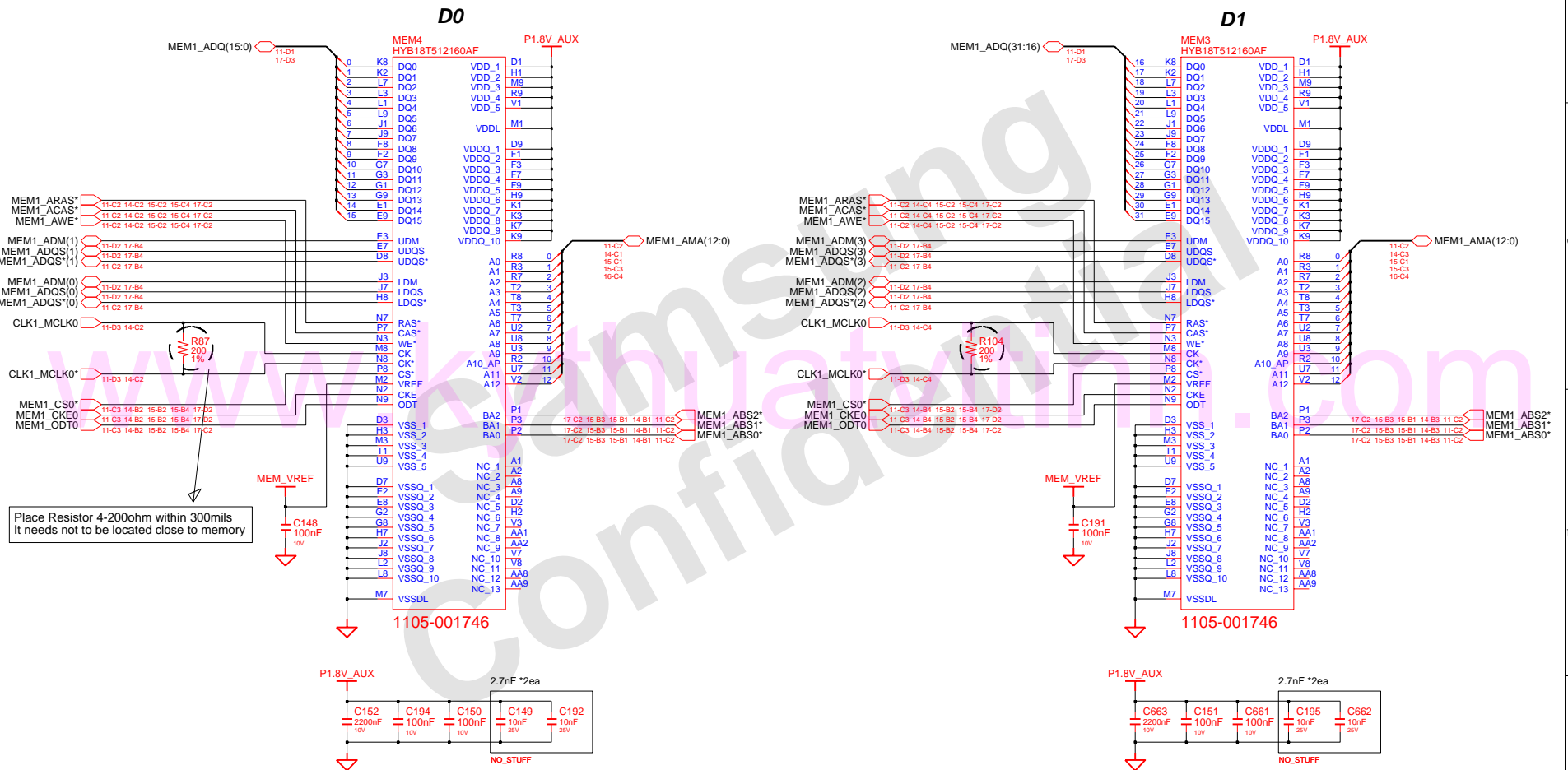
INFINEON: HYB18T512160AF-3.7

1105-001746

On Board MEMORY

1105-001680 : 512Mbit C-die

1105-001717 : 1Gbit C-die



Place Resistor 4-200ohm within 300mils
It needs not to be located close to memory

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR	MAIN		
APPROVAL	JS, EUR	REV	1.0	DDR2 ON BOARD (1/2)	PART NO.	BA41-00680(3)A
MODULE CODE		LAST EDIT		May 11, 2006 10:24:27 PM	PAGE	14 OF 50

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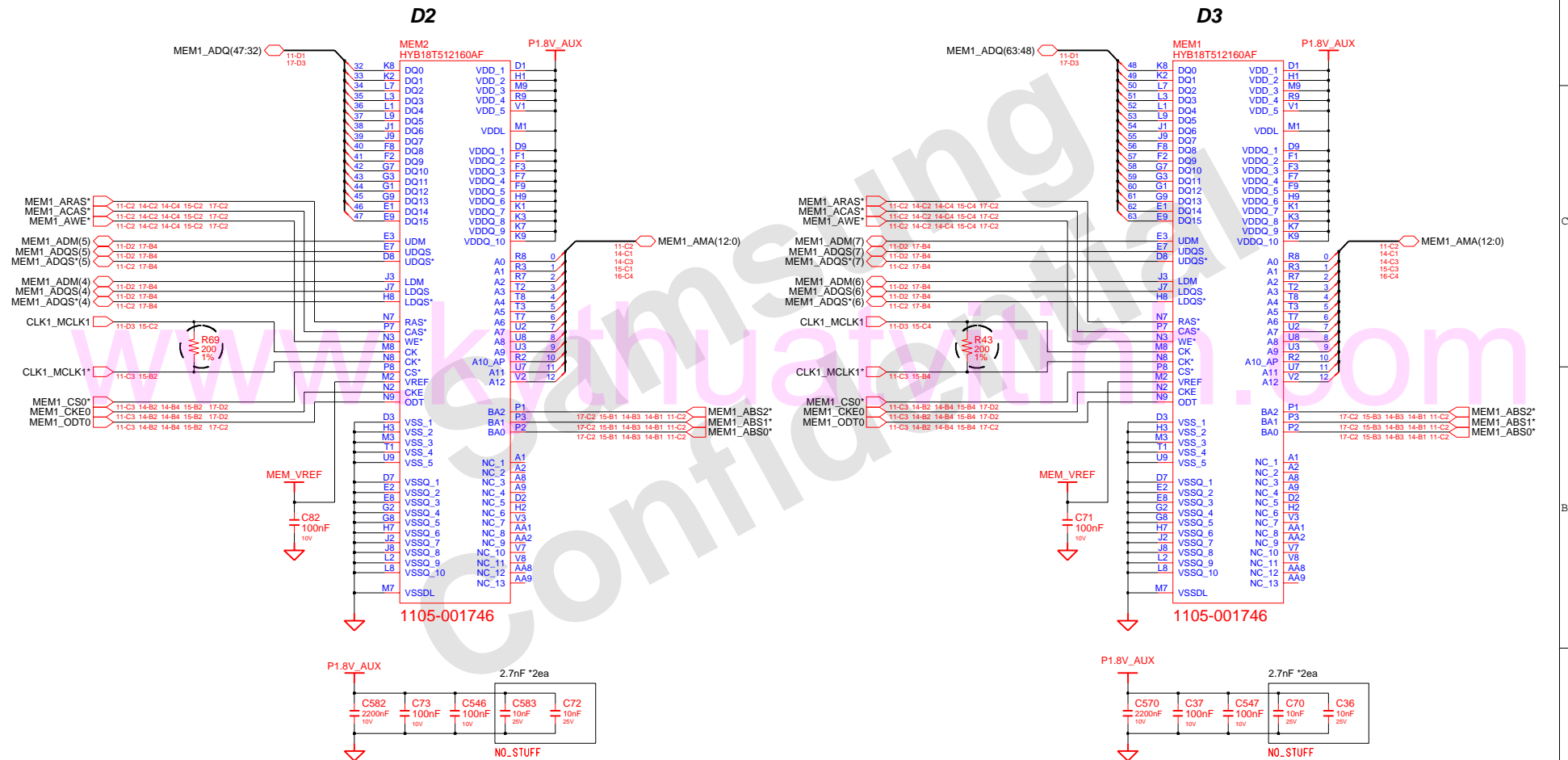
On Board MEMORY

1105-001680 : 512Mbit C-die
1105-001717 : 1Gbit C-die

DDR2 ON BOARD MEMORY

1. 512Mbit DDR2-533MHz x16 I/O

SAMSUNG: K4T51163QB-ZCD5
1105-001680
INFINEON: HYB18T512160AF-3.7
1105-001746



DATE	5/11/2006	TITLE	RIMINI MAIN	SAMSUNG ELECTRONICS
DEV. STEP	SR	DDR2 ON BOARD (2/2)		
CHECK	HK, PARK	REV	1.0	PART NO. BA41-00680(3)A
APPROVAL	JS, EUR	LAST EDIT	May 11, 2006 10:24:27 PM	PAGE 15 OF 50

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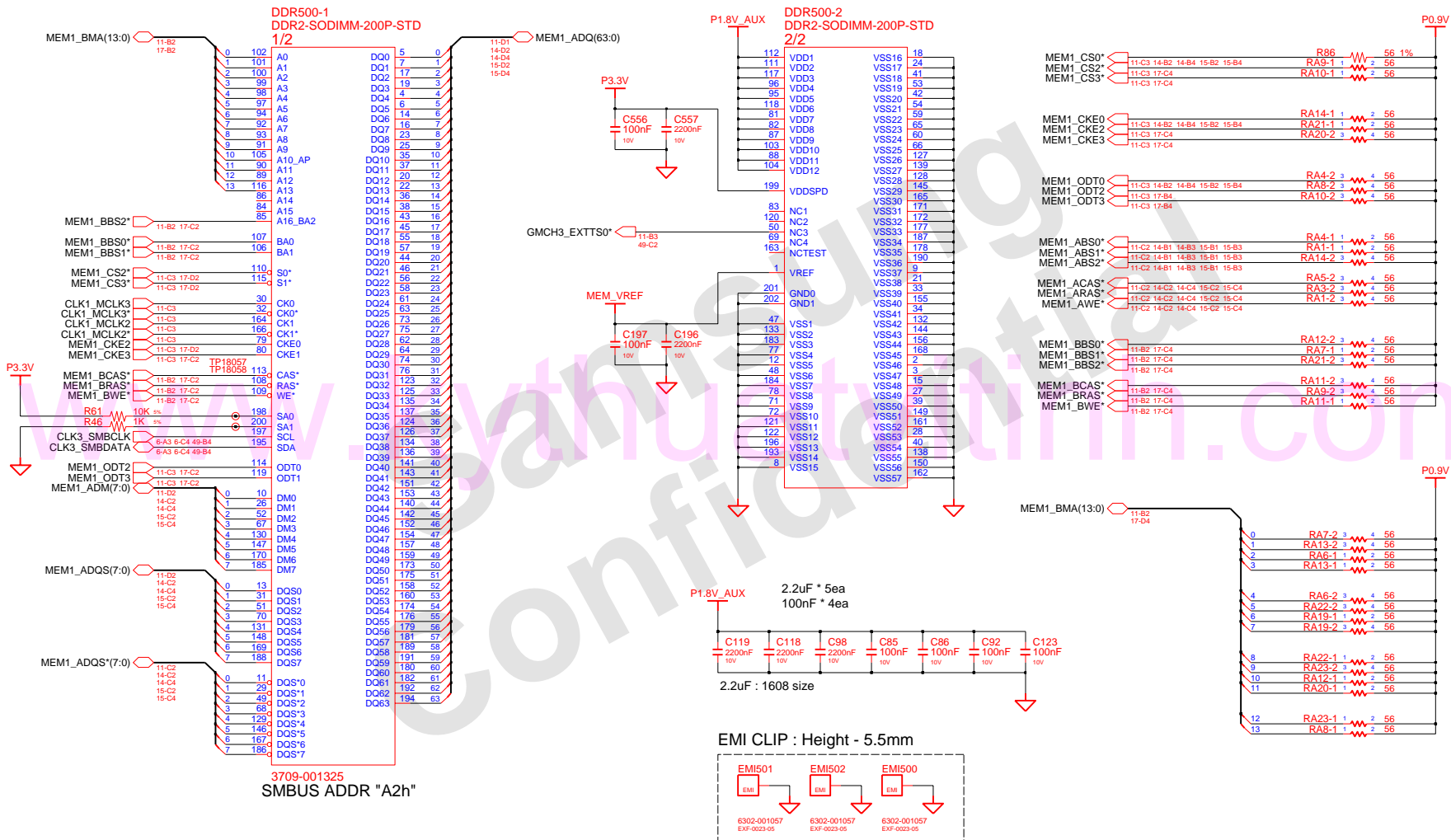


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CHECK	HK, PARK	DEV. STEP	SR	DDR2 TERMINATION		
APPROVAL	JS, EUR	REV	1.0	May 11, 2006 10:24:27 PM		PAGE 16 OF 50
MODULE CODE		LAST EDIT				

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DDR2 Memory Socket



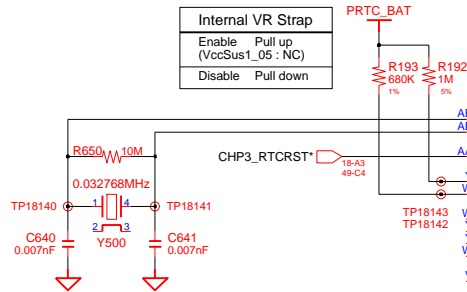
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CHECK	HK, PARK	DEV. STEP	SR	DDR2 SODIMM	PART NO. BA41-00680(3)A	
APPROVAL	JS, EUR	REV	1.0	May 11, 2006 10:24:27 PM	PAGE 17 OF 50	
MODULE CODE		LAST EDIT				

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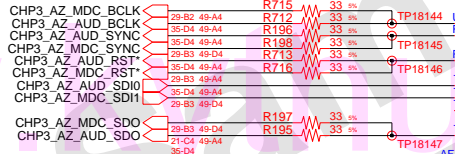
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ICH7-M B0 Stepping : QK65

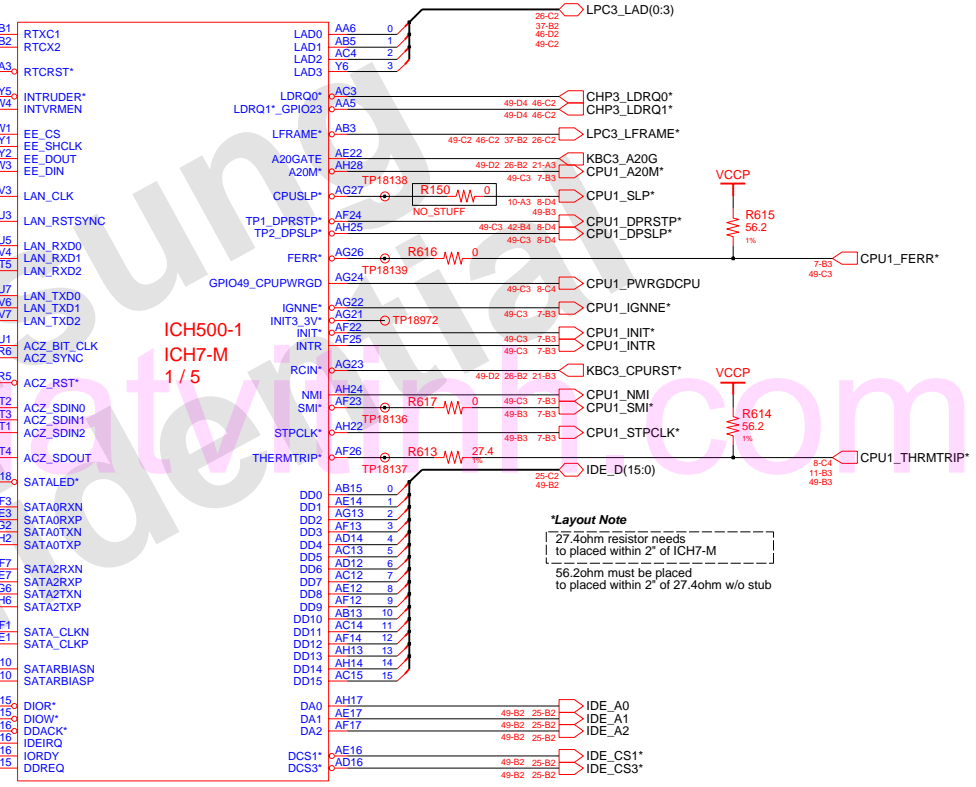
Internal VR Strap	
Enable	Pull up (VccSus1_05 : NC)
Disable	Pull down



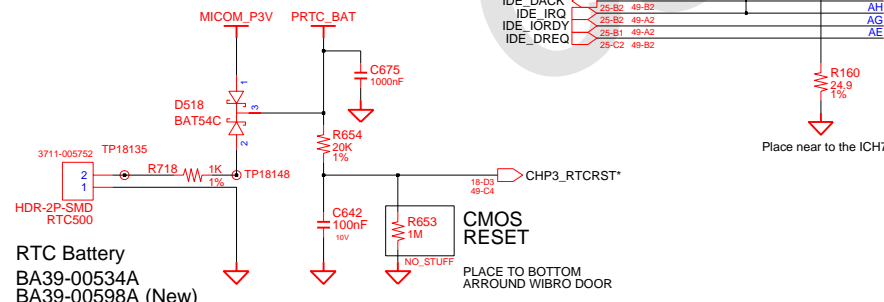
x1 / x2 Docking				
ACZ_SYNC	PORT X Line	PU	PD	
1	1x2 / 2x1	STUFF	NO_STUFF	
0	4x1	NO_STUFF	STUFF	



ICH500-1
ICH7-M
1 / 5



Layout Note
27.4ohm resistor needs to be placed within 2" of ICH7-M
56.2ohm must be placed to be placed within 2" of 27.4ohm w/o stub



RTC Battery
BA39-00534A
BA39-00598A (New)

CMOS RESET
PLACE TO BOTTOM ARROUND WIBRO DOOR

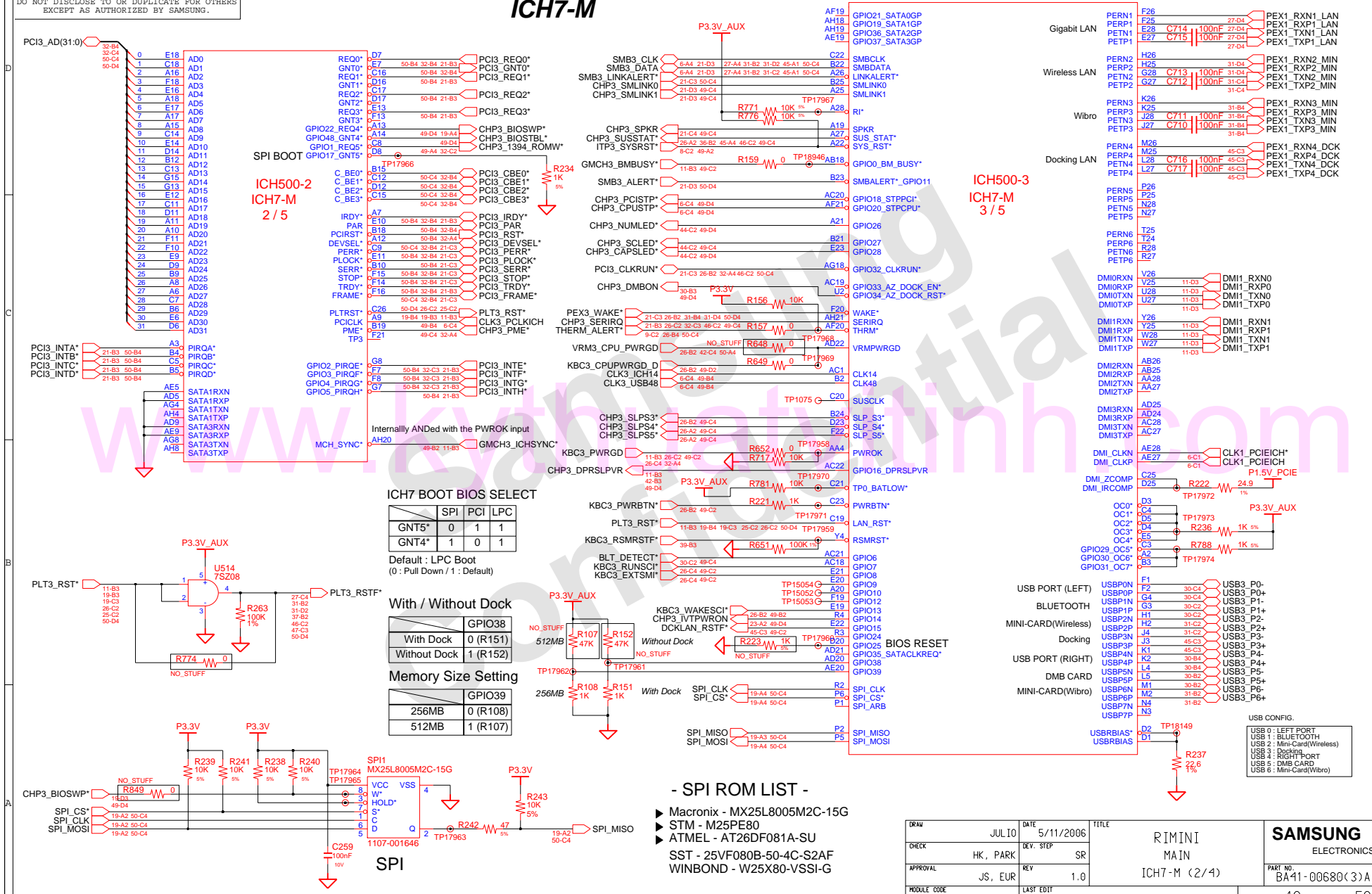
DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR		ICH7-M (1/4)	
APPROVAL	JS, EUR	REV	1.0			PART NO. BA41-00680(3)A
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	18	OF 50

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AC caps : PCIe need to be within 250mils of the driver Resistor for Test : Place Stuffing Option to minimize stubs

ICH7-M



ICH7 BOOT BIOS SELECT

	SPI	PCI	LPC
GNT5*	0	1	1
GNT4*	1	0	1

Default : LPC Boot
(0 : Pull Down / 1 : Default)

With / Without Dock

	GPIO38
With Dock	0 (R151)
Without Dock	1 (R152)

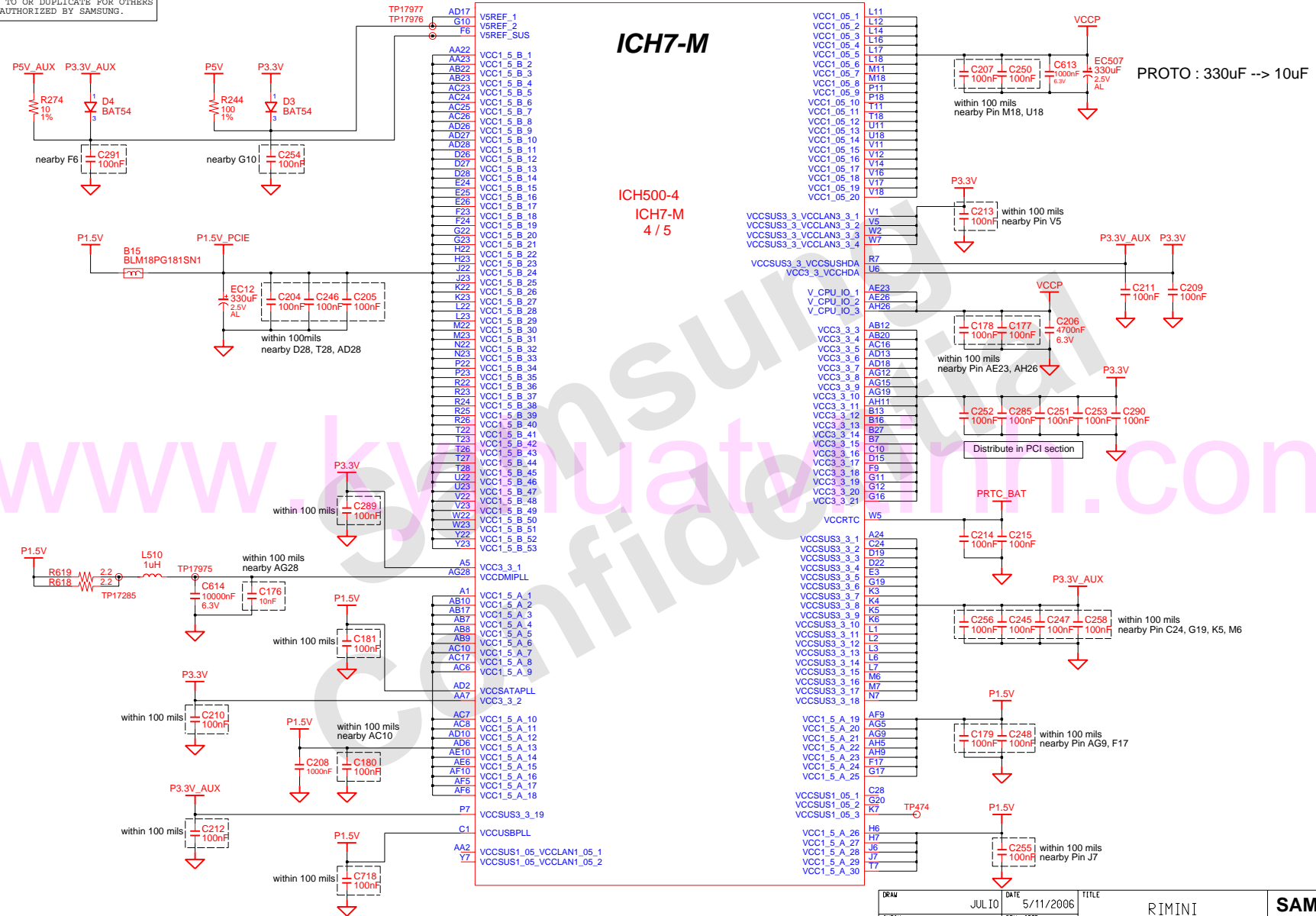
Memory Size Setting

	GPIO39
256MB	0 (R108)
512MB	1 (R107)

- SPI ROM LIST -**
- Macronix - MX25L8005M2C-15G
 - STM - M25PE80
 - ATMEL - AT26DF081A-SU
 - SST - 25VF080B-50-4C-S2AF
 - WINBOND - W25X80-VSSI-G

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN	SAMSUNG ELECTRONICS
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MODULE CODE		LAST EDIT		PAGE	19 OF 50	

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PROTO : 330uF --> 10uF

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MODULE CODE	LAST EDIT		May 11, 2006 10:24:27 PM		PAGE	20 OF 50

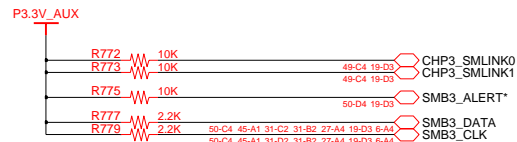
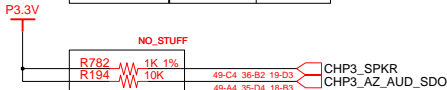
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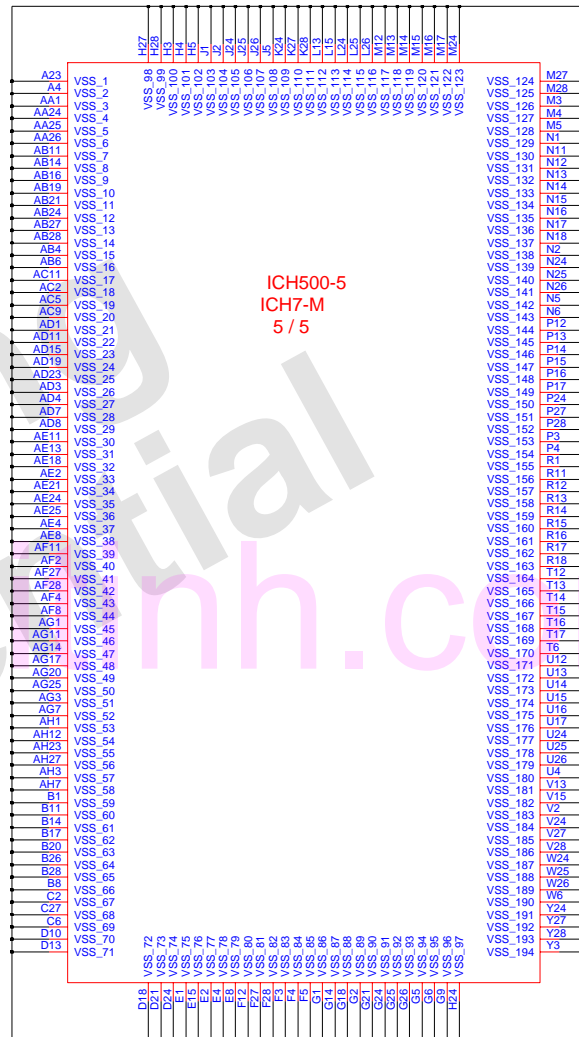
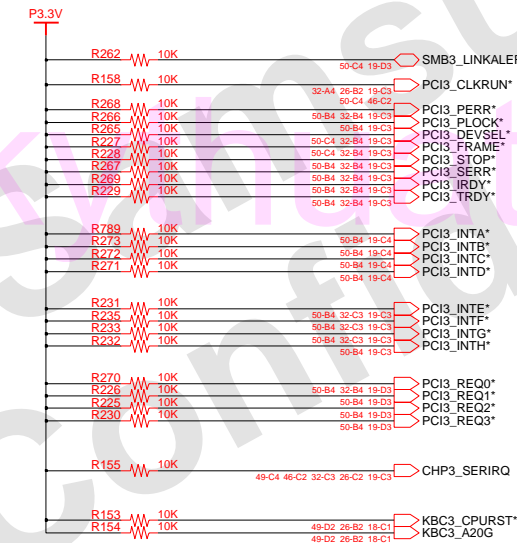
ICH7-M

ICH7-M Options

	Function	Default
CHP3_SPKR	No Reboot	No Stuff
AC97_SDOOUT	Safe Mode	TBD



Wake on PCI-E, OD, Pull-up to ALWAYS power



ICH500-5
ICH7-M
5/5

DRAW	JUL10	DATE	5/11/2006	TITLE	RIMINI MAIN	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR	ICH7-M (4/4)		
APPROVAL	JS, EUR	REV	1.0			PART NO. BA41-00680(3)A
MODULE CODE	LAST EDIT		May 11, 2006 10:24:27 PM	PAGE	21	OF 50

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BIOS CODE

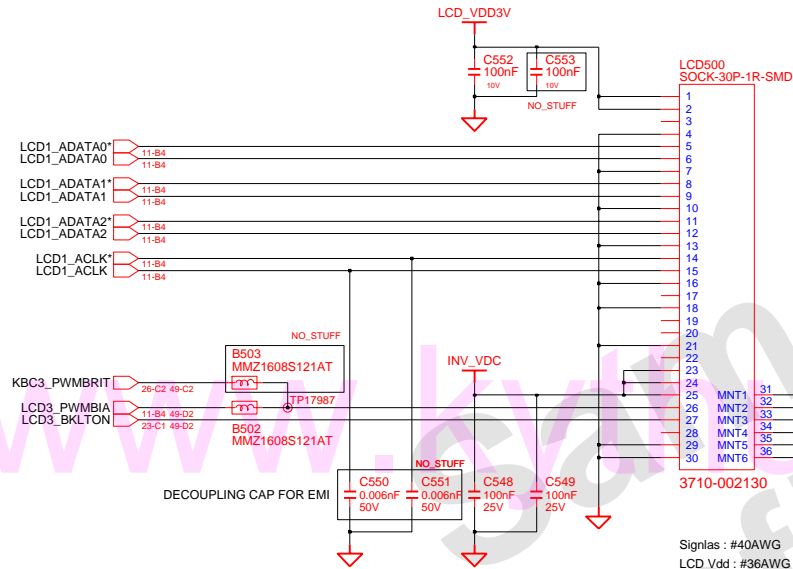
02 VERIFY REAL MODE	66 CONFIGURE ADVANCE CACHE REG.
03 DISABLE NMI	6A DISPLAY EXTERNAL CACHE SIZE
04 GET CPU TYPE	6C DISPLAY SHADOW MESSAGE
06 INIT. SYSTEM H/W	6E DISPLAY NON-DISPOSABLE SEGMENT
08 INIT. CHIPSET REG.	70 DISPLAY ERROR MESSAGE
09 SET IN POST FLAG	72 CHECK FOR CONFIGURATION ERROR
0A INIT CPU.REG	74 TEST REAL-TIME CLOCK
0B CPU CACHE ON	76 CHECK FOR KEYBOARD EERROR
0C INIT.CACHE TO POST	7C SETUP HARDWARE INTERRUPT VECTOR
0E INIT. I/O VALUE	7E TEST COPROCESSER IF PRESENT
0F ENABLE THE L-BUS IDE	80 DISABLE ON-BOARD I/O PORT
10 INIT. POWER MANAGER	82 DETECT AND INSTALL EXT.RS232C
11 LOAD ALTERNATE REG.	84 DETECT AND INSTALL EXT.PARALLEL
13 PCI BUS MASTER RESET WITH INITIAL POST VALUE	86 RE-INIT. ON-BOARD I/O PORT
14 INIT. KEYBOARD CONTROLLER	88 INIT. BIOS DATA ROM
16 CHECK CHECKSUM	8A INIT.EXTENDED BIOS DATA AREA
18 8254 TIMER INIT.	8C INIT. FDD CONTROLLER
1A 8237 DMA CONTROLLER INIT.	9A SHADOW OPTION ROMS
1C RESET INTERRUPT CONTROLLER	9C SETUP POWER MANAGEMENT
20 TEST DRAM REFRESH	9E ENABLE H/W INTERRUPT
22 TEST 8742 KEYBOARD CONTROLLER	A0 SET TIME OF DAY
24 SET ES SEGMENT REG. TO 4GB	A4 INIT. TYPOMATIC RATE
26 ENABLE A20	A8 ERASE F2 PROMPT
28 AUTO SIZING DRAM	AA SCAN FOR F2 KEY STROKE
32 COMPUTE THE CPU SPEED	AC ENTER SETUP
34 TESET CMOS RAM	AE CLEAR IN POST FLAG
38 SHADOW SYSTEM BIOS ROM	B0 CHECK FOR ERRORS
3A AUTO SIZING CACHE	B2 POST DONE-PREPARE TO BOOT O/S
3C CONFIGURE ADVANCED CHIPSET REG.	B4 ONE BEEP
3D LOAD ALTER REG. WITH CMOS VALUE	B6 CHECK PASSWORD (OPTION)
42 INIT. INTERRUPT VECTOR	B7 ACPI INIT
44 INIT. BIOS INTERRUPT	BA DMI INIT
46 CHECK ROM COPYRIGHT NOTICE	BE CLEAR SCREEN
47 INIT. I20 SUPPORT IF INSTALLED	C0 TRY BOOT WITH INT19
48 CHECK VIDEO CONFIGURE AGAINST CMOS	D0 INTERRUPT HANDLER ERROR
49 INIT. PCI BUS AND DEVICE	D2 UNKNOWN INTERRUPT ERROR
4A INIT. ALL VIDEO BIOS ROM	D4 PENDING INTERRUPT ERROR
4C SHADOW VIDEO BIOS ROM	D6 SHUTDOWN 5
50 DISPLAY CPU TYPE AND SPEED	D8 SHUTDOWN ERROR
52 TEST KEYBOARD	DA EXTENDED BLOCK MOVE
54 SET KEYCLICK IF ENABLED	DC SHUTDOWN 10
56 ENABLE KEYBOARD	89 ENABLE NMI
58 TEST FOR UNEXPECTED INTERRUPTS	90 INIT. HDD CONTROLLER
5A DISPLAY " PRESS SETUP"	91 INIT. LOCAL BUS HDD CONTROLLER
5C TEST RAM BETWEEN 512K AND 640K	92 JUMP TO USER PATCH 2
60 TEST EXTENDED MEMORY	94 DISABLE A20 ADDRESS LINE
62 TEST EXTENDED MEMORY ADDRESS LINE	96 CLEAR HUGE ES SEGMENT REG.
64 JUMP TO USER PATCH 1	98 SEARCH FOR OPTION ROMS

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN BIOS CODE	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0			PART NO. BA41-00680(3)A
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	22	OF 50

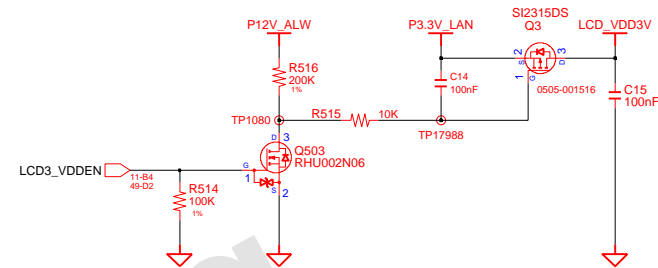
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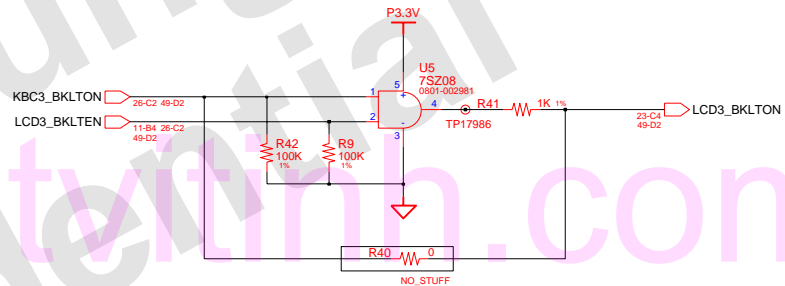
WXGA LCD CONNECTOR



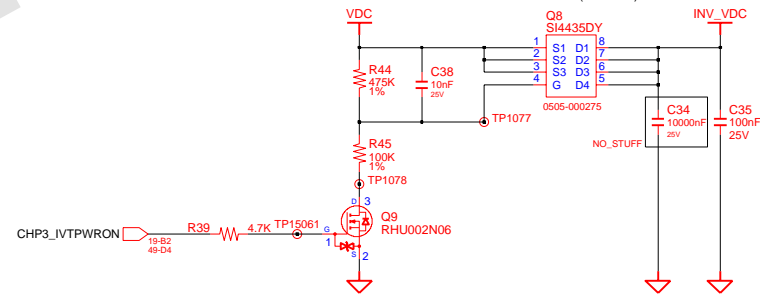
Signals : #40AWG
 LCD Vdd : #36AWG
 Inverter Vdd : #36AWG
 GND : #36AWG



Remove AND Gate : MICOM Control



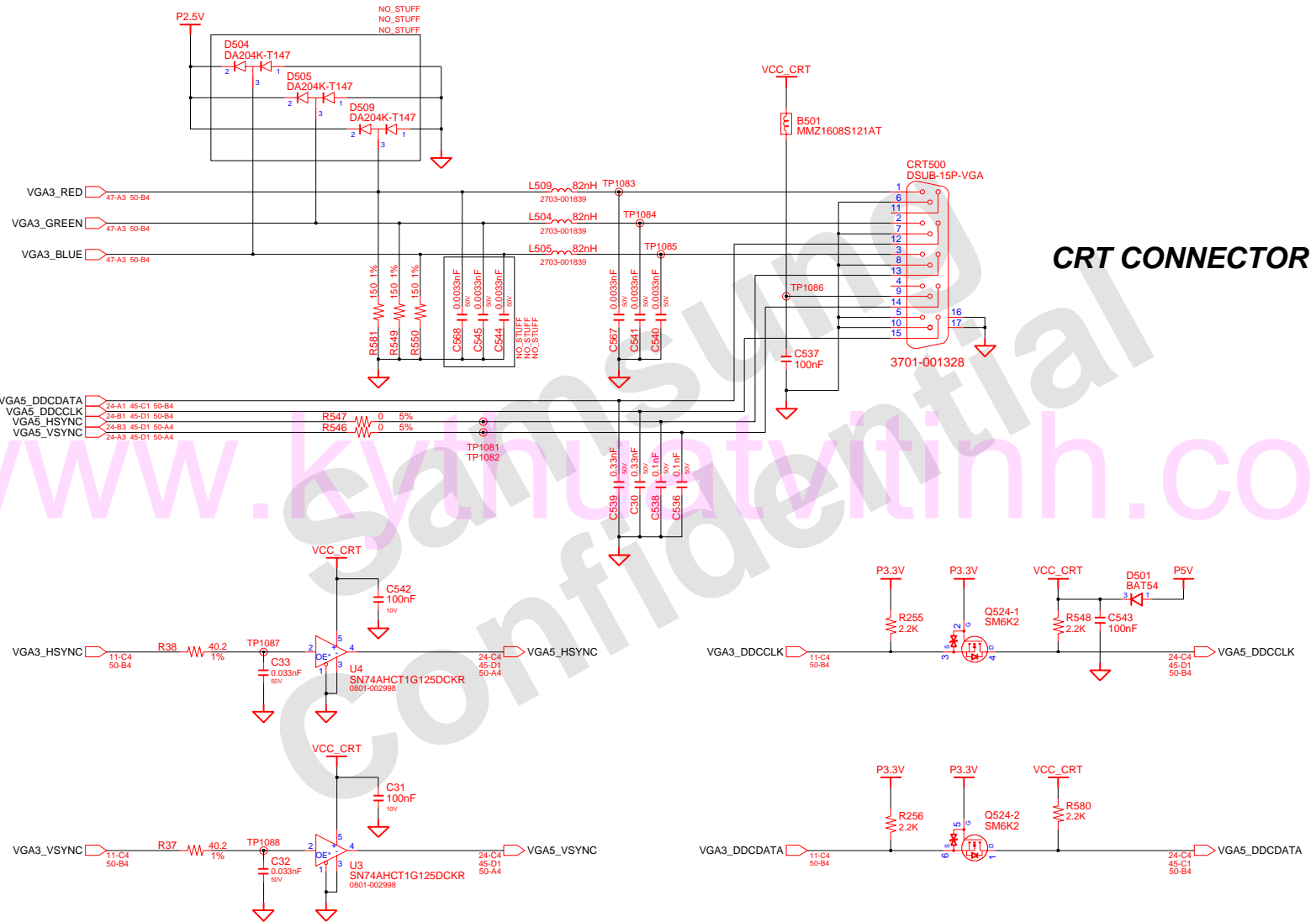
After DV, check Habana INV_VDC circuit.
 SI2307DS-T1-E3 (HABANA)



DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN LCD(LVDS) CONN.	SAMSUNG ELECTRONICS PART NO. BA41-00680(3)A
CHECK	HK, PARK	DEV. STEP	SR	REV	1.0	
APPROVAL	JS, EUR	LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	23	OF 50

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CRT CONNECTOR

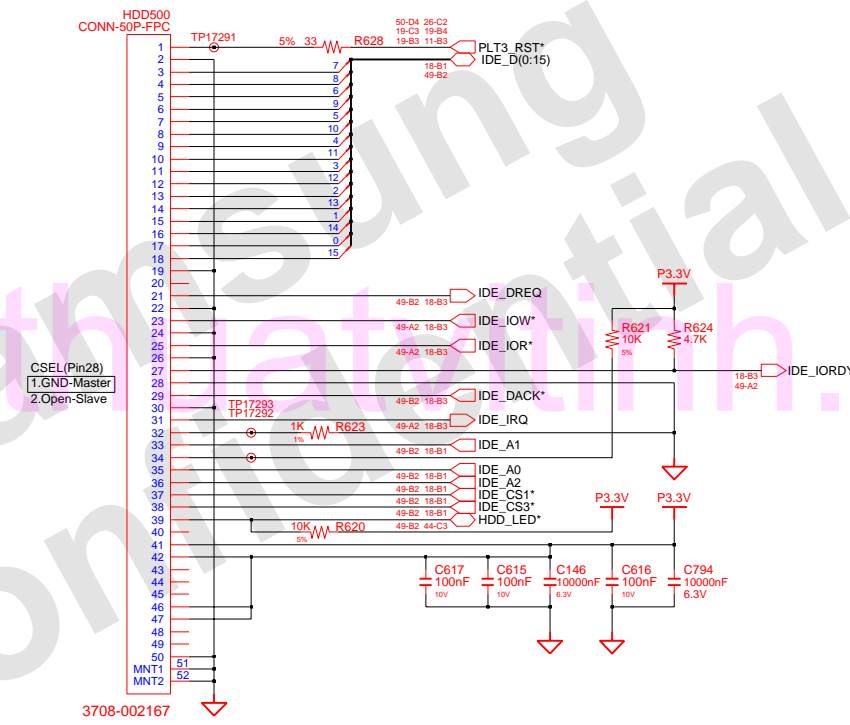
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CHECK	HK, PARK	DEV. STEP	SR	REV	1.0	
APPROVAL	JS, EUR	LAST EDIT	May 11, 2006 10:24:27 PM	PAGE 24 OF 50		

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Main to HDD (Locking Type)

IDE Pin Assignment			
1.8 SFF HDD		Main Board	
SIGNALS	No.	No.	SIGNALS
RESERVED	1	-	N.C
RESERVED	2	-	N.C
RESET	3	1	RESET
GROUND	4	2	GROUND
DD7	5	3	DD7
DD8	6	4	DD8
DD6	7	5	DD6
DD9	8	6	DD9
DD5	9	7	DD5
DD10	10	8	DD10
DD4	11	9	DD4
DD11	12	10	DD11
DD3	13	11	DD3
DD12	14	12	DD12
DD2	15	13	DD2
DD13	16	14	DD13
DD1	17	15	DD1
DD14	18	16	DD14
DD0	19	17	DD0
DD15	20	18	DD15
GROUND	21	19	GROUND
DMARQ	22	21	IDE_DREQ
GROUND	23	22	GROUND
DIOW	24	23	DIOW
DIOR	25	25	DIOR
GROUND	26	26	GROUND
IORDY	27	27	IDE_IORDY
GROUND	28	28	GROUND (CSEL)
DMACK	29	29	IDE_DACK
INTRQ	30	31	IDE_IRQ
DA1	31	33	IDE_A1
PDIAG	32	34	PDIAG (Pull-Up)
DA0	33	35	IDE_A0
DA2	34	36	IDE_A2
CS0	35	37	IDE_CS1
CS1	36	38	IDE_CS3
DASP	37	39	IDE_LED
+3.3V	38	41,42	+3.3V
+3.3V	39	46,47	+3.3V
Reserved (Toshiba) DevAdr(HGST) - 0(open): Master - 1(PullUp): Slave	40	-	N.C

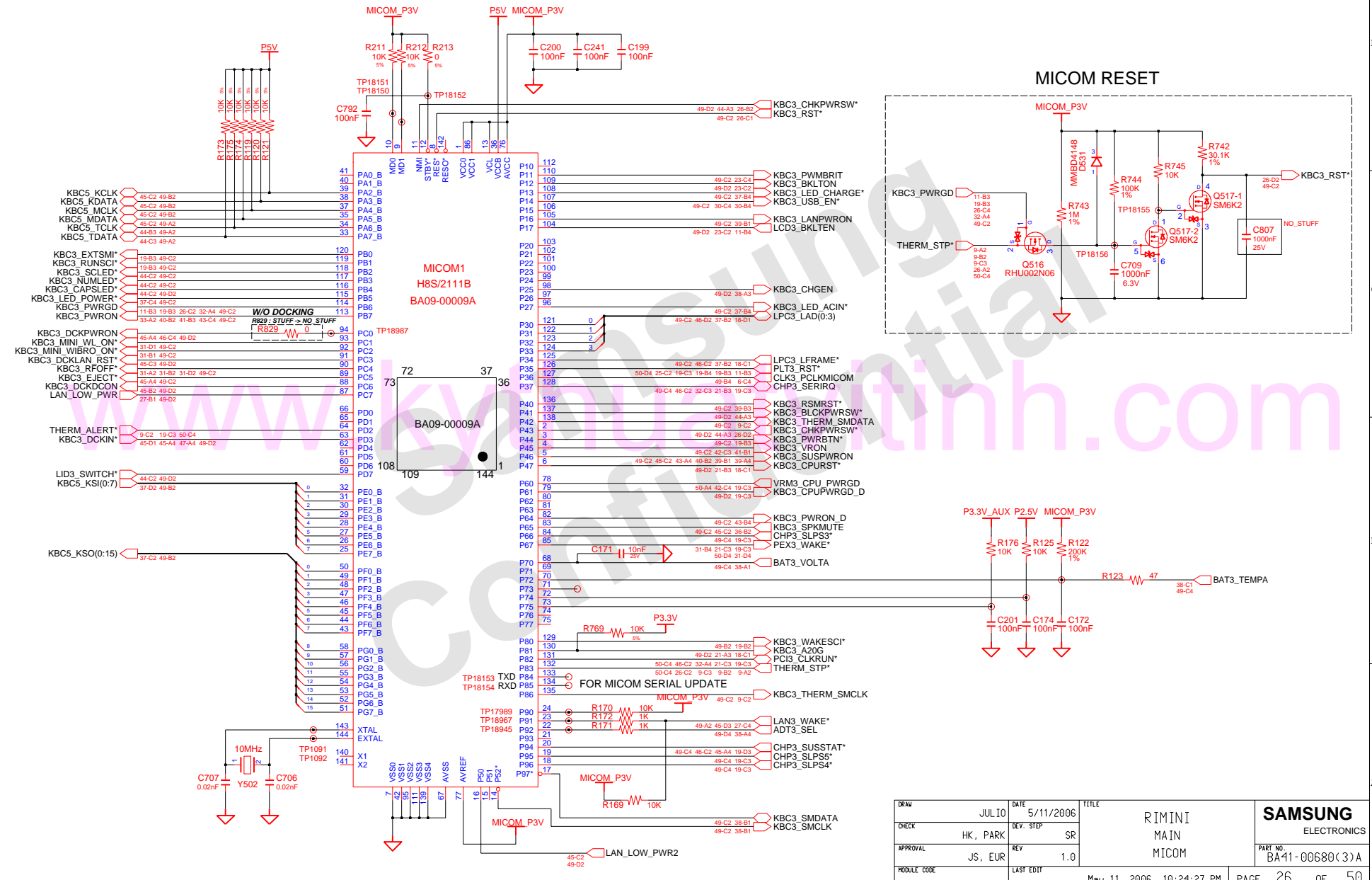


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CHECK	HK, PARK	DEV. STEP	SR	REV	1.0	
APPROVAL	JS, EUR	LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	25	OF 50

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MICOM

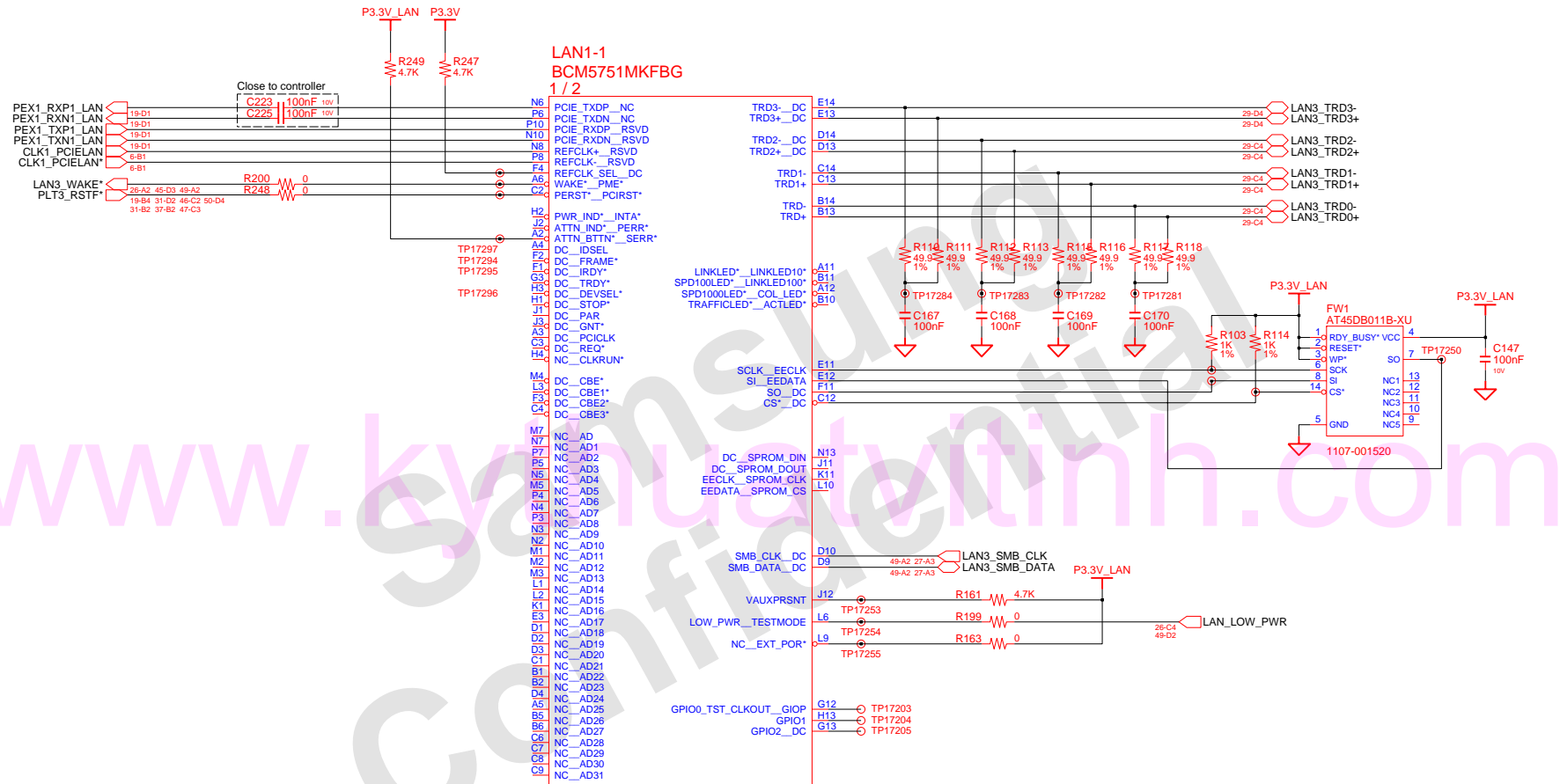


DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN MICOM	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0			PART NO. BA41-00680(3)A
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	26	OF 50

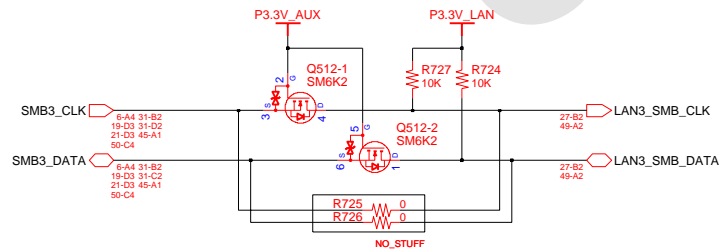
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LAN Controller



1205-002749

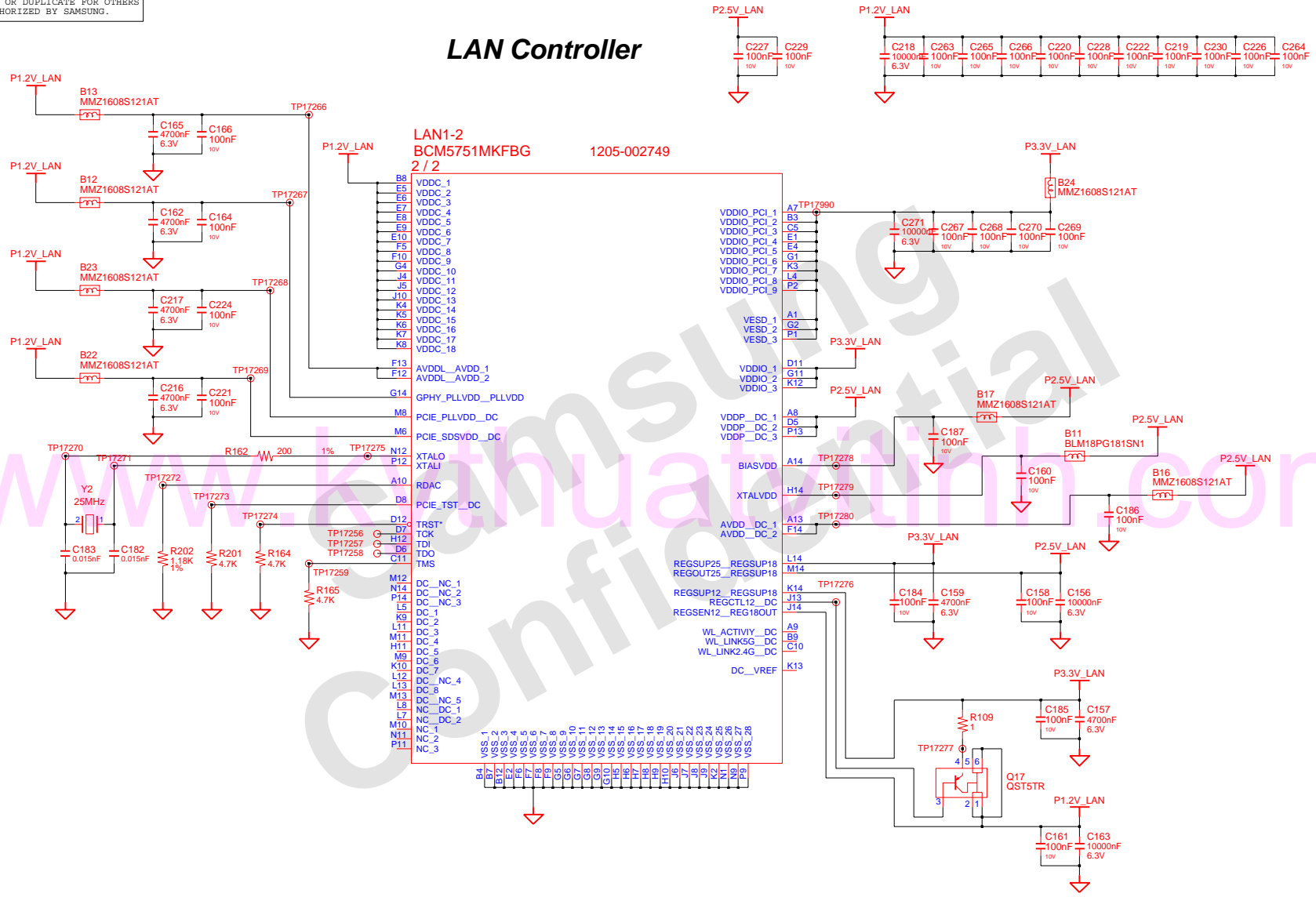


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CHECK	HK, PARK	DEV. STEP	SR	REV	1.0	
APPROVAL	JS, EUR	LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	27	OF 50

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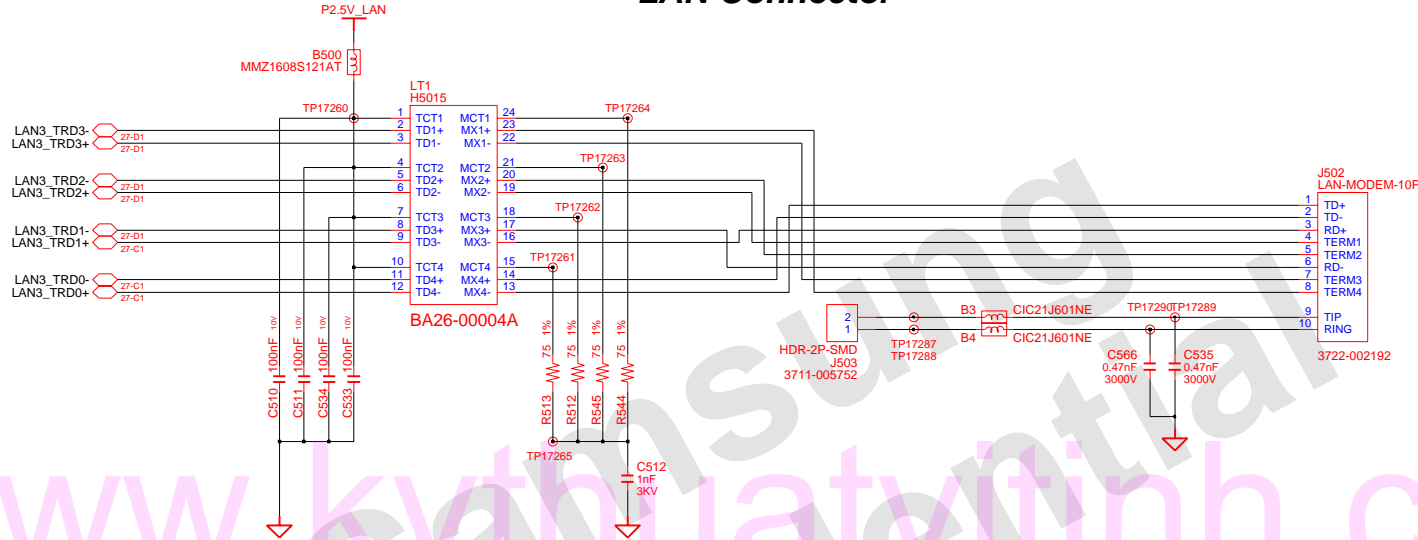
LAN Controller



DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN LAN CONTROLLER (2/2)	SAMSUNG ELECTRONICS PART NO. BA41-00680(3)A
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE		LAST EDIT				
				May 11, 2006 10:24:27 PM	PAGE 28 OF 50	

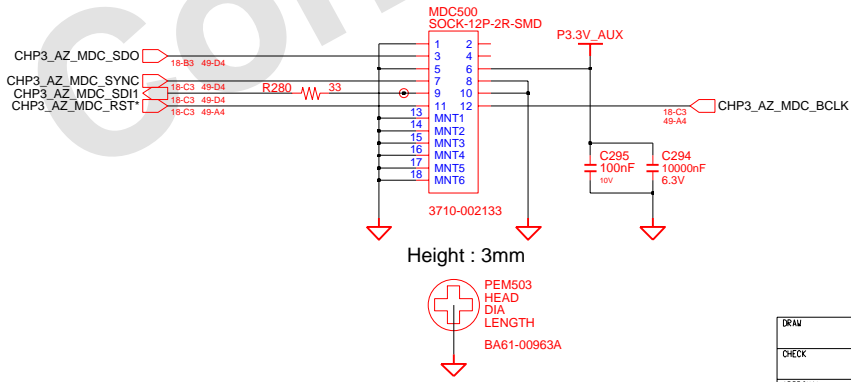
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LAN Connector



MDC Connector

MDC Module : BA59-01272A

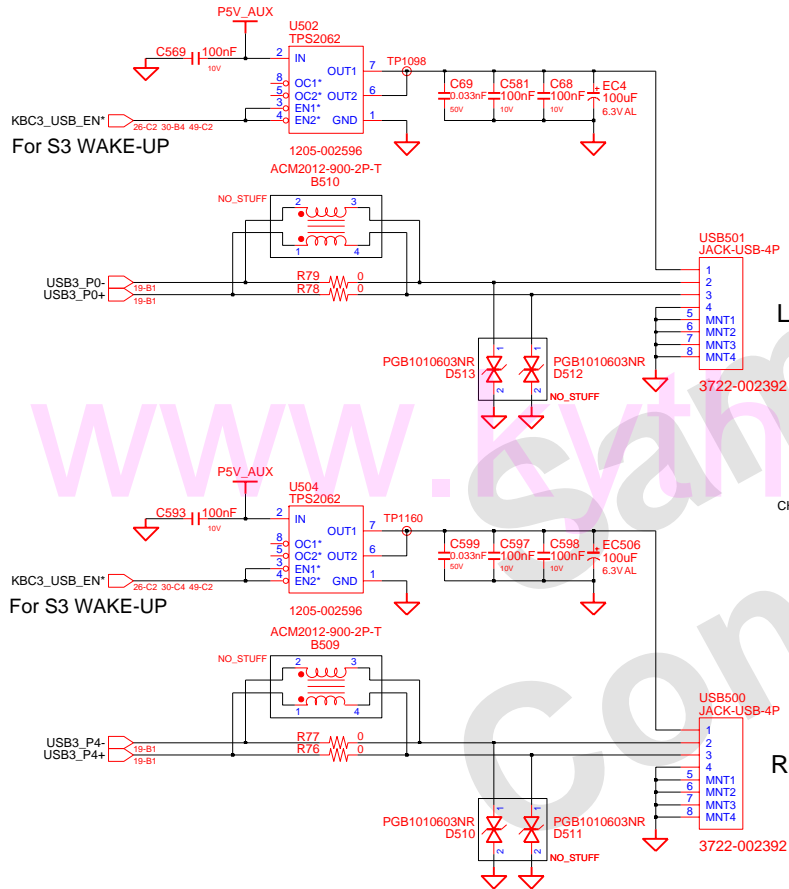


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CHECK	HK, PARK	DEV. STEP	SR	MDC & COMBO JACK		
APPROVAL	JS, EUR	REV	1.0	May 11, 2006 10:24:27 PM		PAGE 29 OF 50
MODULE CODE		LAST EDIT				

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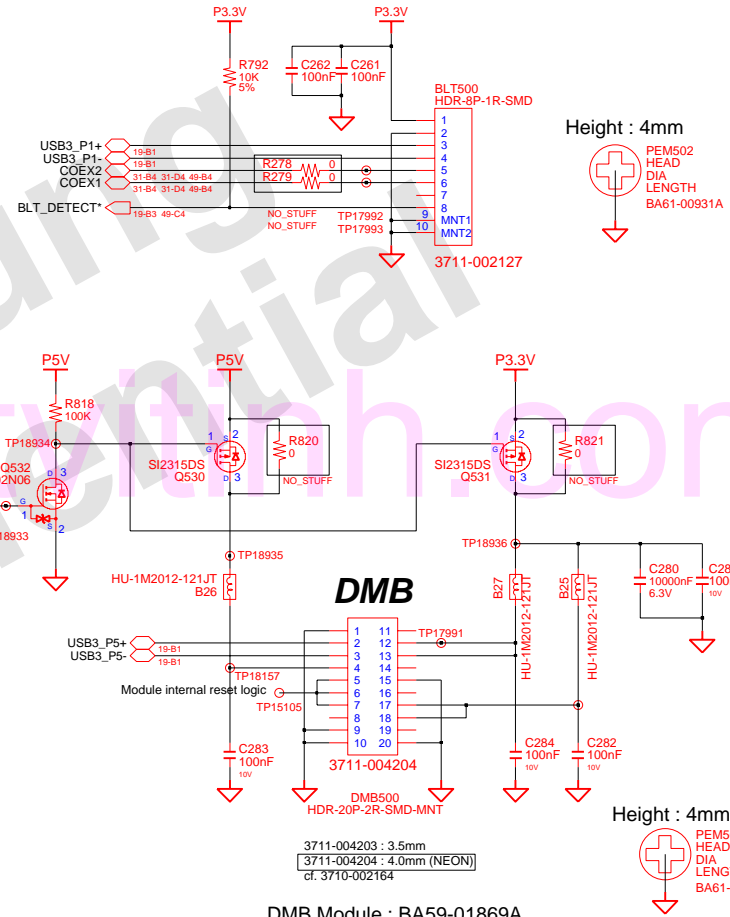
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USB Port



BLUETOOTH

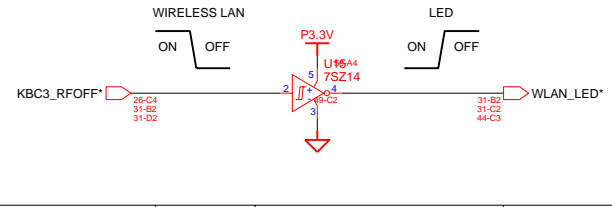
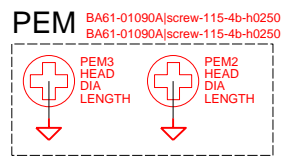
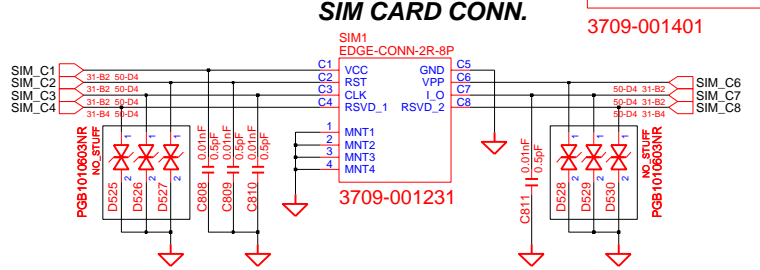
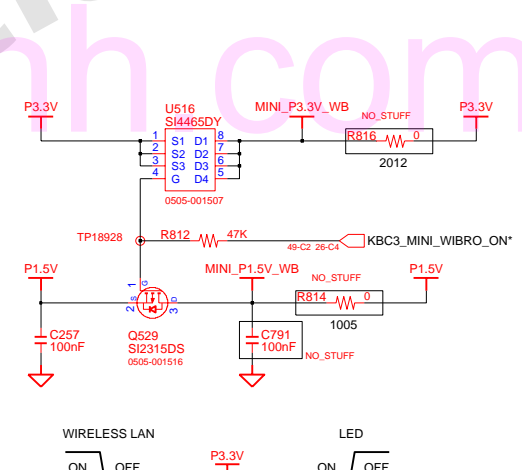
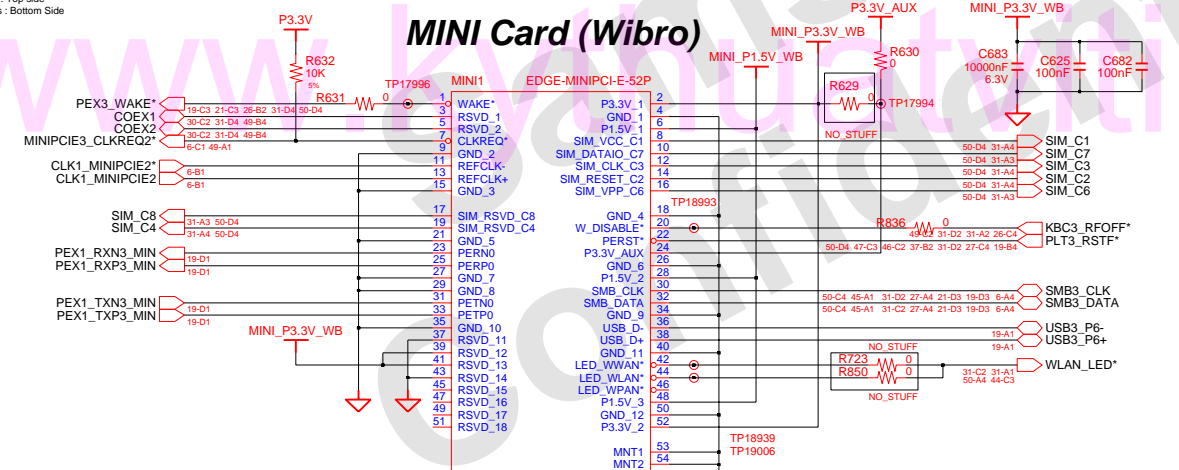
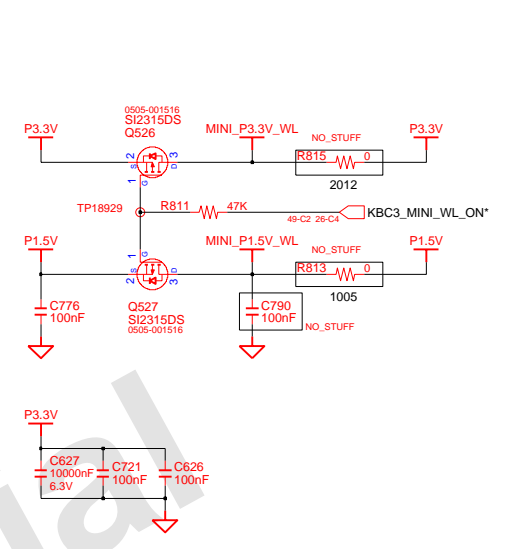
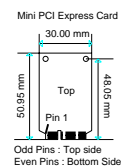
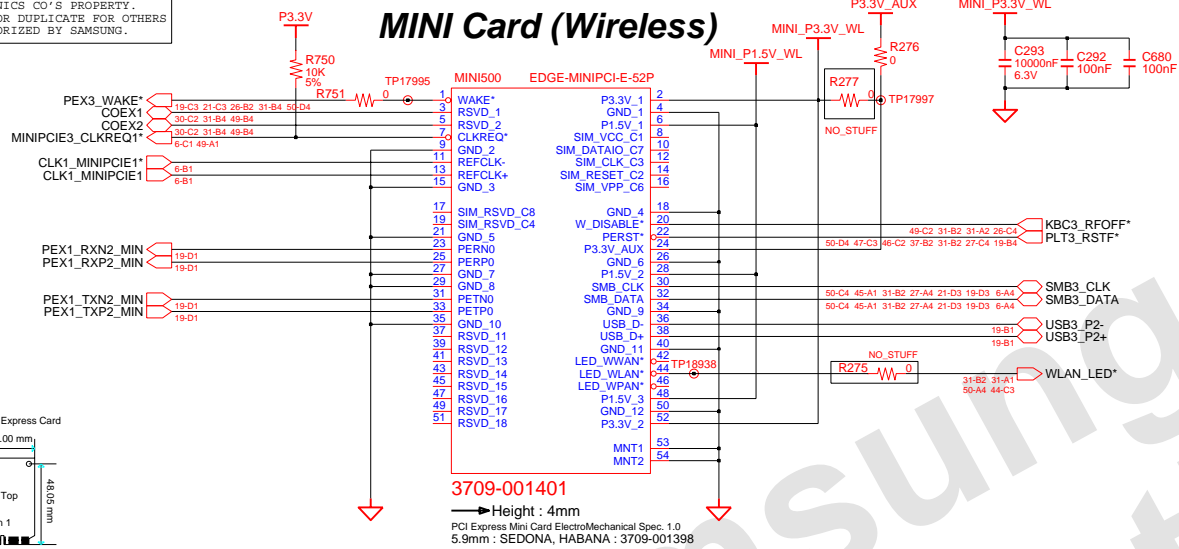
INTEL F/W : PIN5-COEX2
BROADCOM F/W : PIN7-COEX2



DRAW	JUL10	DATE	5/11/2006	TITLE	RIMINI MAIN	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR	USB, DMB & BLUETOOTH		
APPROVAL	JS, EUR	REV	1.0	PART NO. BA41-00680(3)A		PAGE 30 OF 50
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM			

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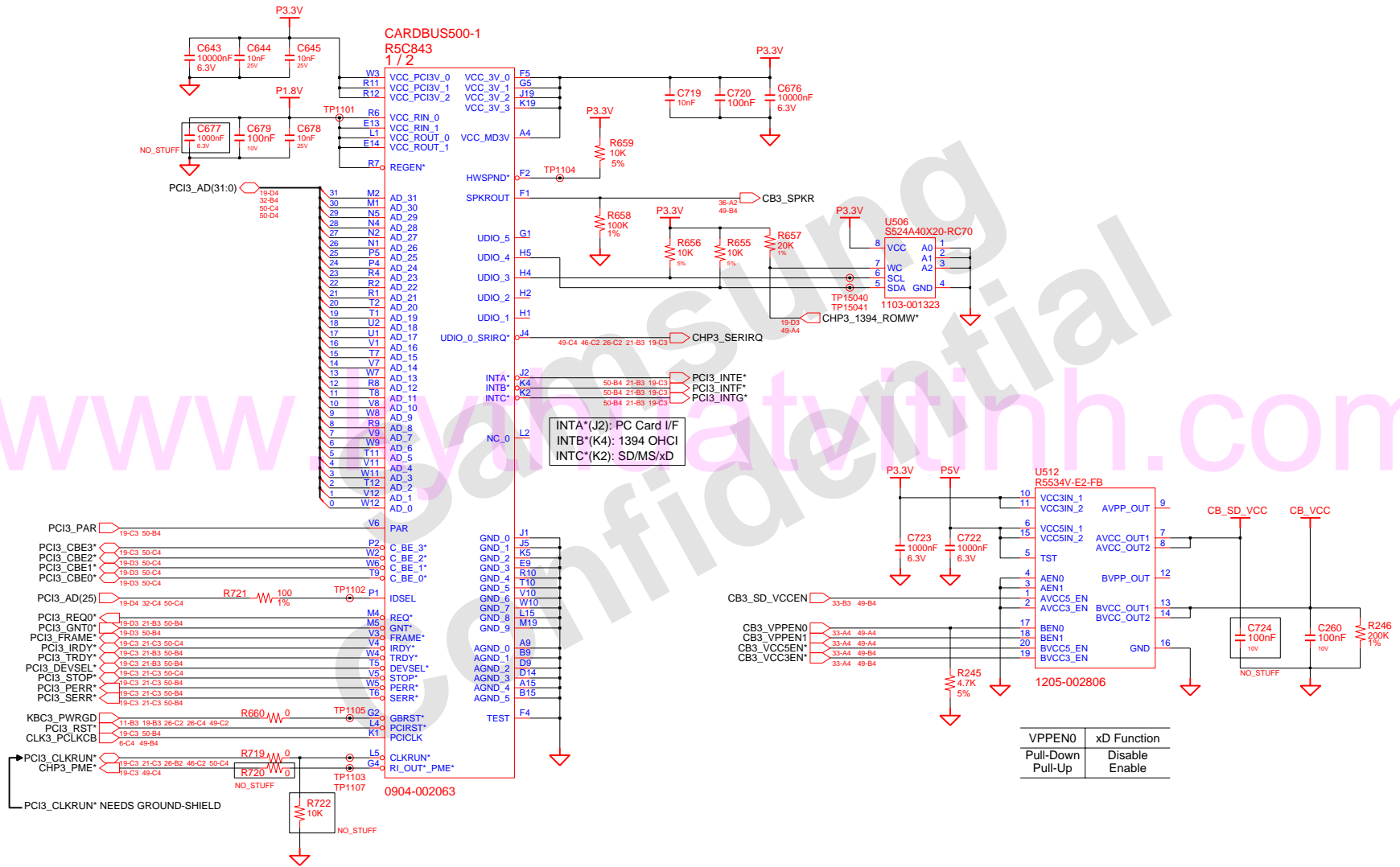


DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR	PART NO. BA41-00680(3)A		
APPROVAL	JS, EUR	REV	1.0	MINI CARD (GOLAN,WIBRO)		PAGE 31 OF 50
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM			

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CARDBUS Controller



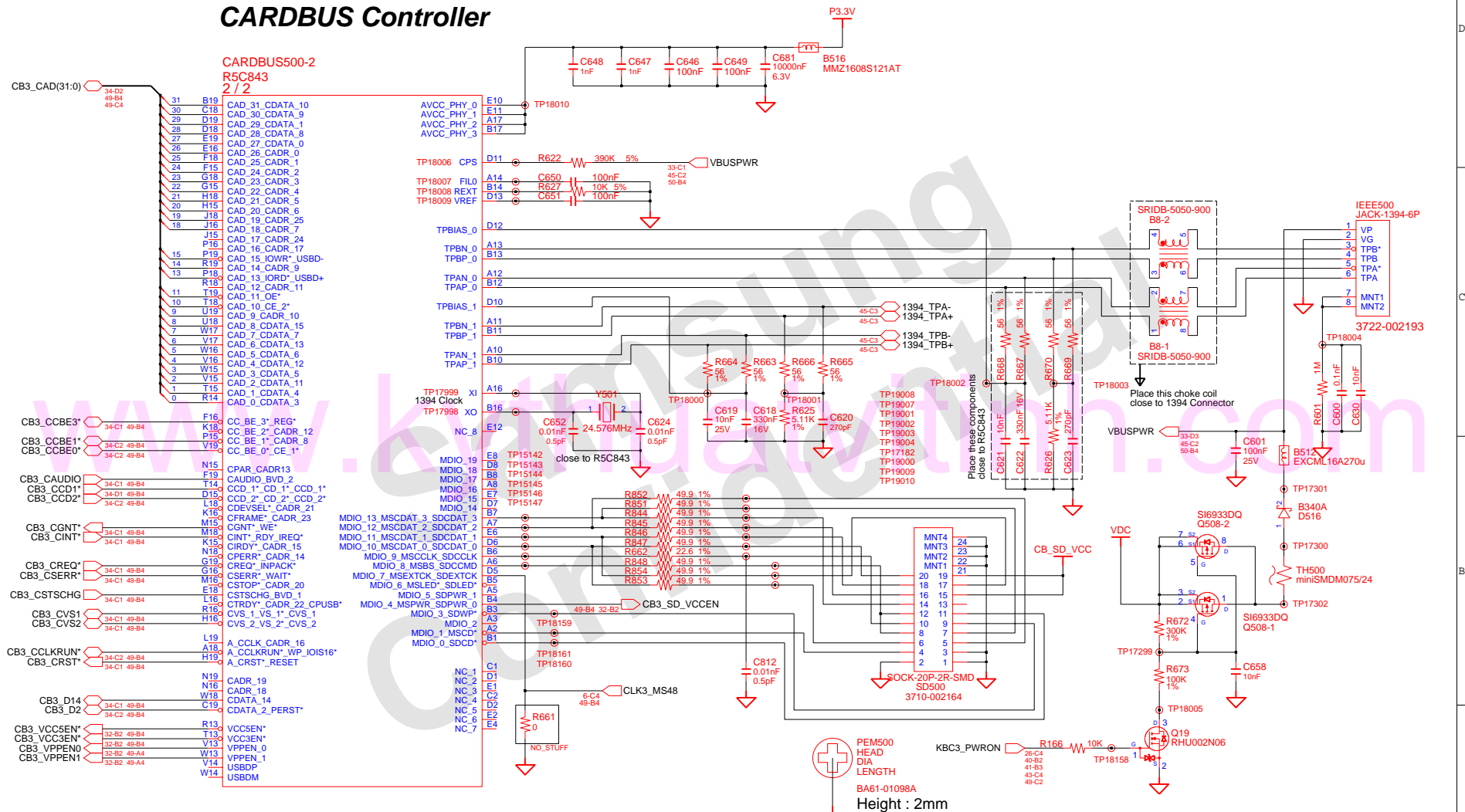
INTA*(J2): PC Card I/F
INTB*(K4): 1394 OHCI
INTC*(K2): SD/MS/xD

VPPEN0	xD Function
Pull-Down	Disable
Pull-Up	Enable

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN	SAMSUNG ELECTRONICS PART NO. BA41-00680(3)A
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0	CARDBUS CONTROLLER (1/2)		
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	32 OF 50	

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CARDBUS Controller



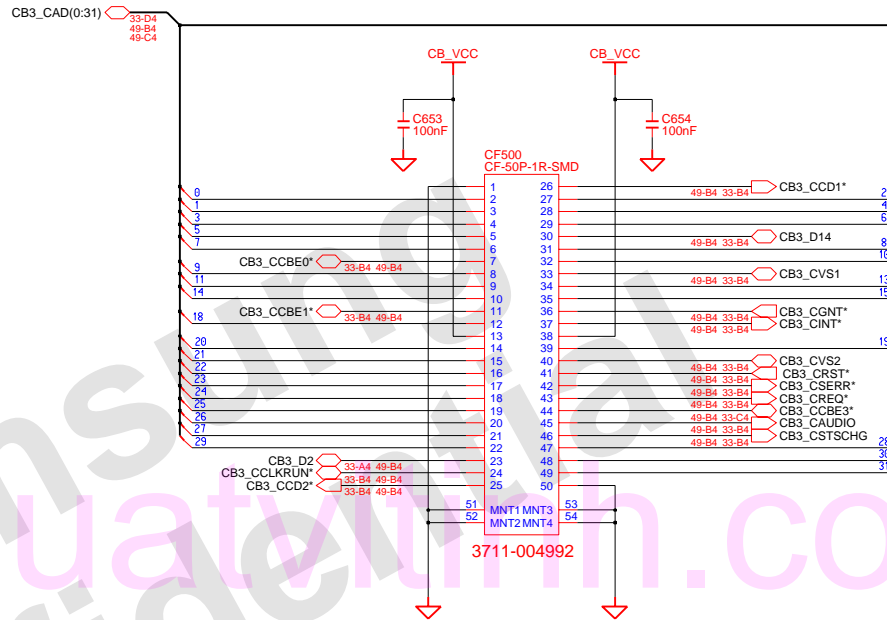
- CARDBUS500-2 R5C843 2/2**
- 31 B19 CAD 31_CDATA_10
 - 30 C18 CAD 30_CDATA_9
 - 29 D19 CAD 29_CDATA_1
 - 28 D18 CAD 28_CDATA_8
 - 27 E19 CAD 27_CDATA_0
 - 26 E16 CAD 26_CADR_0
 - 25 F18 CAD 25_CADR_1
 - 24 F15 CAD 24_CADR_2
 - 23 G18 CAD 23_CADR_3
 - 22 G15 CAD 22_CADR_4
 - 21 H18 CAD 21_CADR_5
 - 20 H15 CAD 20_CADR_6
 - 19 J18 CAD 19_CADR_25
 - 18 J15 CAD 18_CADR_7
 - 17 P16 CAD 17_CADR_24
 - 16 P19 CAD 16_CADR_17
 - 15 P19 CAD 15_IOWR*_USBD+
 - 14 R19 CAD 14_CADR_9
 - 13 R18 CAD 13_IORD*_USBD+
 - 12 T19 CAD 12_CADR_11
 - 11 T18 CAD 11_CE_2*
 - 10 U19 CAD 10_CADR_10
 - 9 U18 CAD 9_CDATA_15
 - 8 W17 CAD 7_CDATA_7
 - 7 W16 CAD 6_CDATA_13
 - 6 V17 CAD 5_CDATA_6
 - 5 V16 CAD 4_CDATA_12
 - 4 W15 CAD 3_CDATA_5
 - 3 V15 CAD 2_CDATA_11
 - 2 T15 CAD 1_CDATA_4
 - 1 R14 CAD 0_CDATA_3
- Power and Control Signals:**
- CB3_CCBE3* F16 CC_BE_3*_REG*
 - CB3_CCBE1* K18 CC_BE_2*_CADR_12
 - CB3_CCBE0* P19 CC_BE_1*_CADR_8
 - CC_BE_0*_CE_1*
 - CB3_AUDIO F19 CPAR_CADR13
 - CB3_CCD1* T14 CAUDIO_BVD_2
 - CB3_CCD2* D19 CCD_1*_CD_1*_CCD_1*
 - CCD_2*_CD_2*_CCD_2*
 - CB3_CGNT* M15 CGNT*_WE*
 - CB3_CINT* M18 CINT*_RDY_IREQ*
 - CB3_CSERR* G18 CIRDY*_CADR_15
 - CB3_CREQ* G16 CPERR*_CADR_14
 - CB3_CSTSCHG* M16 CREQ*_INPACK*
 - CB3_CVS1* H16 CSERR*_WAIT*
 - CB3_CVS2* H16 CSTOP*_CADR_20
 - CSTSCHG_BVD_1
 - CB3_CVS2* R16 CTRDY*_CADR_22_CSPUS*
 - CB3_CVS2* H16 CVS_1*_VS_1*_CVS_1
 - CVS_2*_VS_2*_CVS_2
 - CB3_CCLKRUN* L19 A_CLK_CADR_16
 - CB3_CRST* A18 A_CLKRUN*_WP_IOIS16*
 - CRST*_RESET
- MDIO Signals:**
- MDIO_19 MDIO_19
 - MDIO_18 MDIO_18
 - MDIO_17 MDIO_17
 - MDIO_16 MDIO_16
 - MDIO_15 MDIO_15
 - MDIO_14 MDIO_14
 - MDIO_13_MSCDAT_3_SDCDAT_3
 - MDIO_12_MSCDAT_2_SDCDAT_2
 - MDIO_11_MSCDAT_1_SDCDAT_1
 - MDIO_10_MSCDAT_0_SDCDAT_0
 - MDIO_9_MSCLK_SDCCLK
 - MDIO_8_MSBS_SDCGMD
 - MDIO_7_MSEXTCK_SDEXTCK
 - MDIO_6_MSLED*_SLED*
 - MDIO_5_SDPWR_1
 - MDIO_4_MSPWR_SDPWR_0
 - MDIO_3_SDPWR_0
 - MDIO_2_SDPWR_0
 - MDIO_1_MSCD*
 - MDIO_0_SDCD*
- Other Signals:**
- NC_1 NC_1
 - NC_2 NC_2
 - NC_3 NC_3
 - NC_4 NC_4
 - NC_5 NC_5
 - NC_6 NC_6
 - NC_7 NC_7
 - NC_19 CADR_19
 - NC_18 CADR_18
 - NC_17 CDATA_14
 - NC_16 CDATA_2_PERST*
 - NC_15 VCCSEN*
 - NC_14 VCC3EN*
 - NC_13 VPPEN_0
 - NC_12 VPPEN_1
 - NC_11 USBDP
 - NC_10 USBDM

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI	SAMSUNG
CHECK	HK, PARK	DEV. STEP	SR	MAIN	ELECTRONICS	
APPROVAL	JS, EUR	REV	1.0	CARDBUS CONTROLLER (2/2)	PART NO.	BA41-00680(3)A
MODULE CODE		LAST EDIT		May 11, 2006 10:24:27 PM	PAGE	

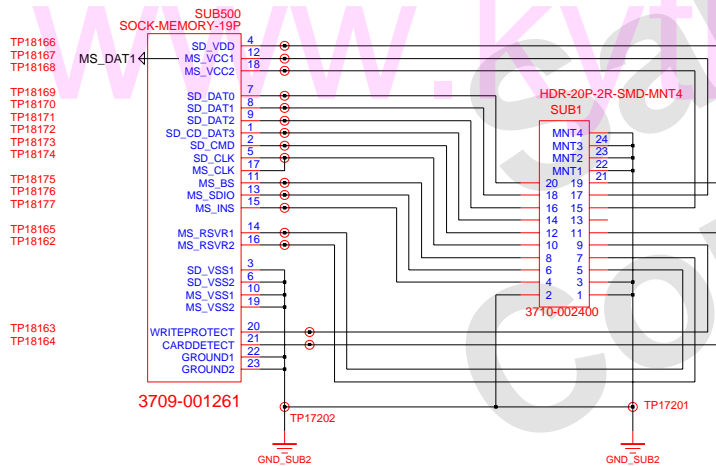
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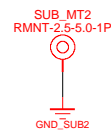
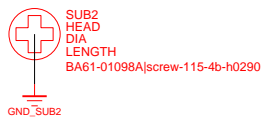
CF CARD



3in1 Sub Board



Height : 2mm



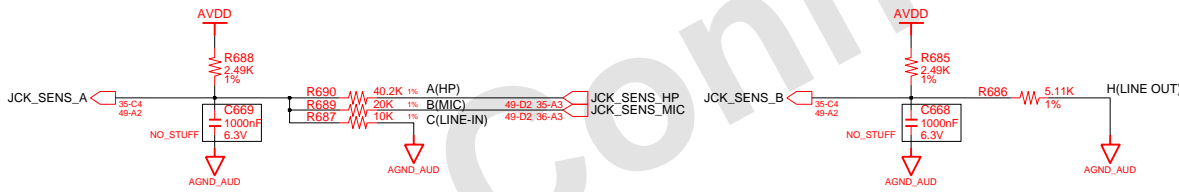
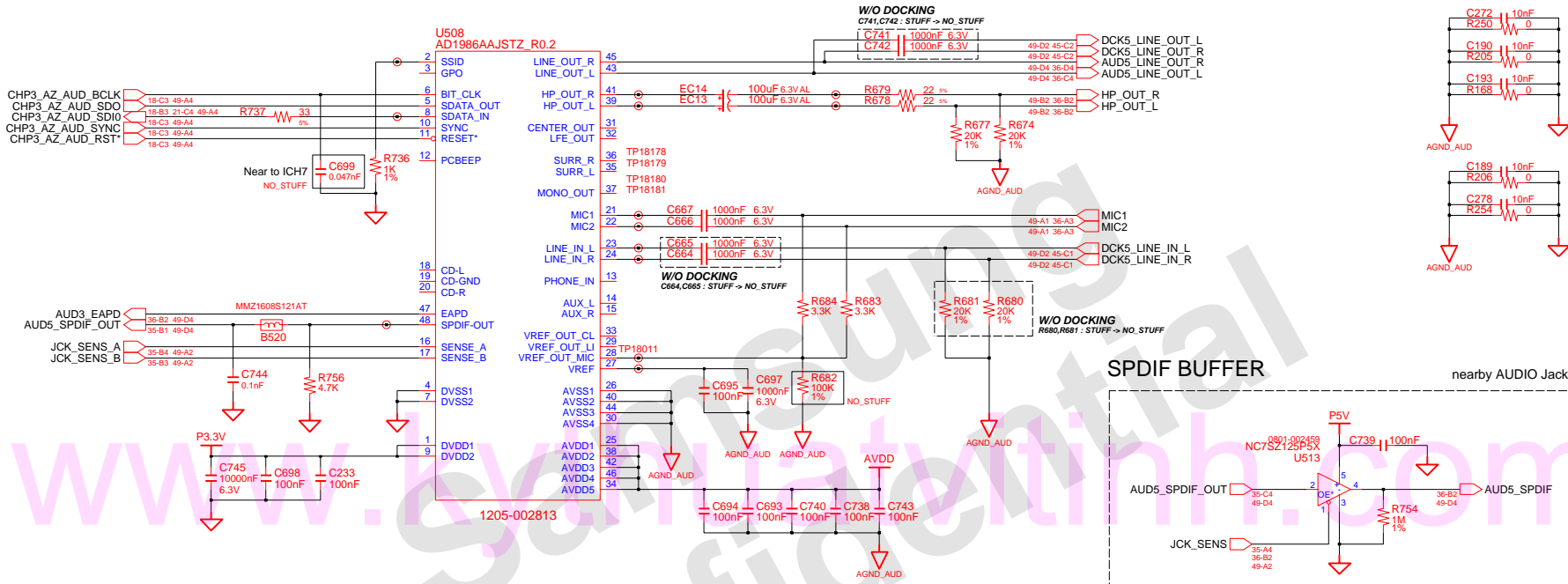
DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR	MAIN		
APPROVAL	JS, EUR	REV	1.0	CF CARD & 3IN1 SUB B'D	PART NO.	BA41-00680(3)A
MODULE CODE		LAST EDIT		May 11, 2006 10:24:27 PM	PAGE	34 OF 50

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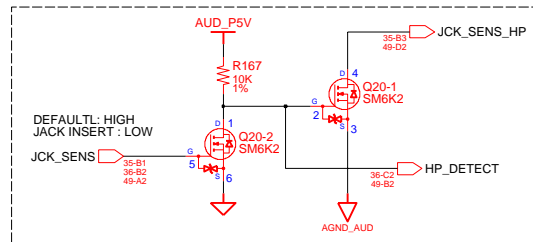
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AUDIO CODEC

Table with 2 columns: 1.AGND_AUD (Audio Ground), 2.GND (Digital Ground)



SPDIF DETECT



AVDD

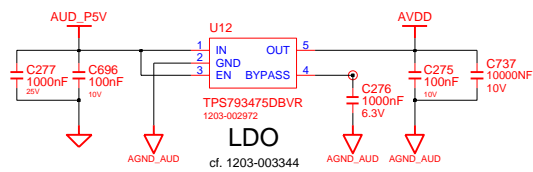


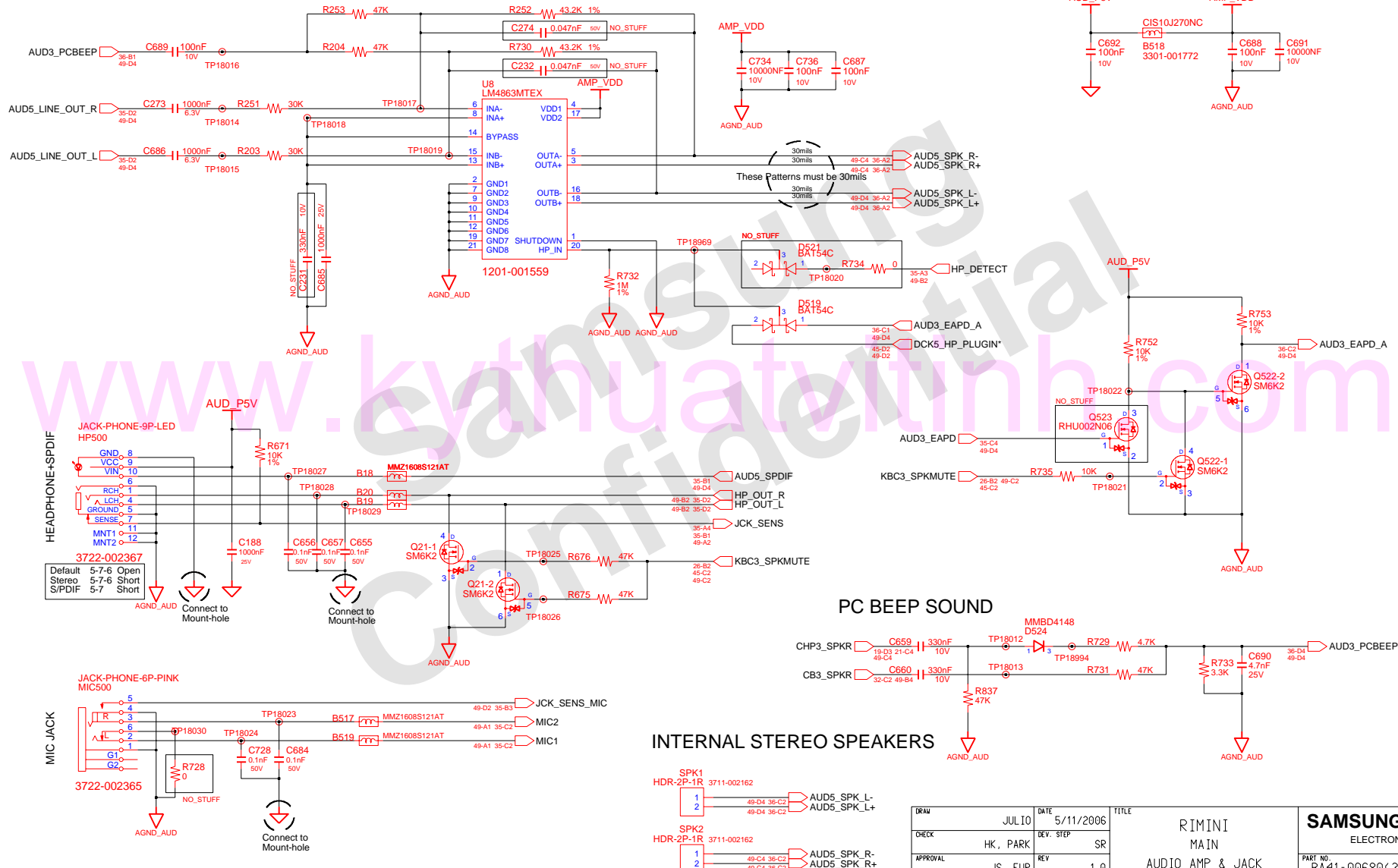
Table with columns: DRAW, CHECK, APPROVAL, MODULE CODE, DATE, DEV. STEP, REV, LAST EDIT, TITLE, RIMINI MAIN AUDIO CODEC, SAMSUNG ELECTRONICS, PART NO. BA41-00680(3)A, May 11, 2006 10:24:27 PM, PAGE 35 OF 50

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AUDIO AMP

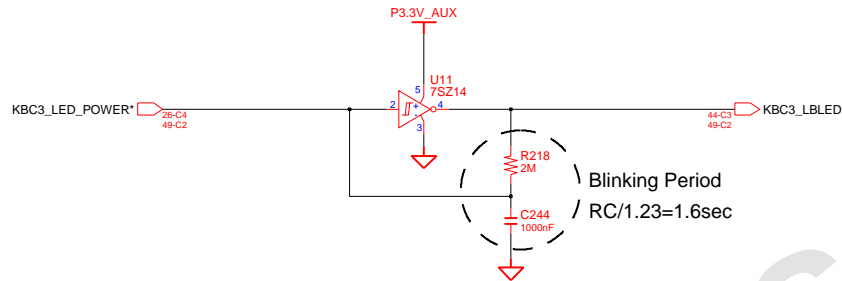
AMP_VDD



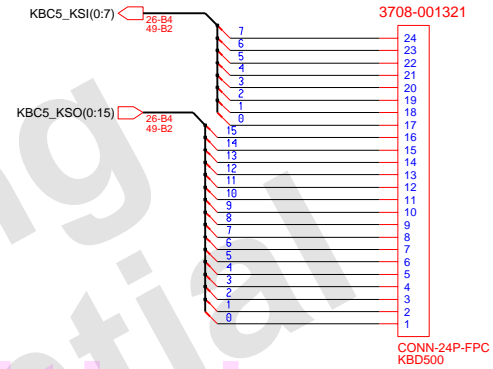
DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN AUDIO AMP & JACK	SAMSUNG ELECTRONICS PART NO. BA41-00680(3)A
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM			
				PAGE	36 OF 50	

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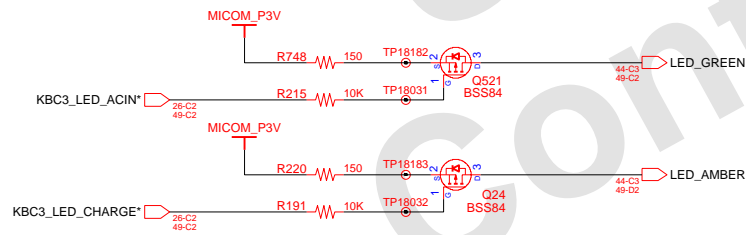
POWER_ON / LB LED



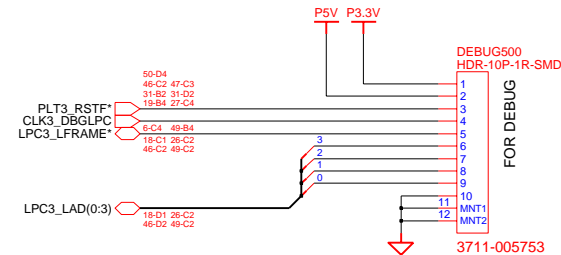
KEYBOARD



ADAPTERIN/CHARGING LED



DEBUG PORT

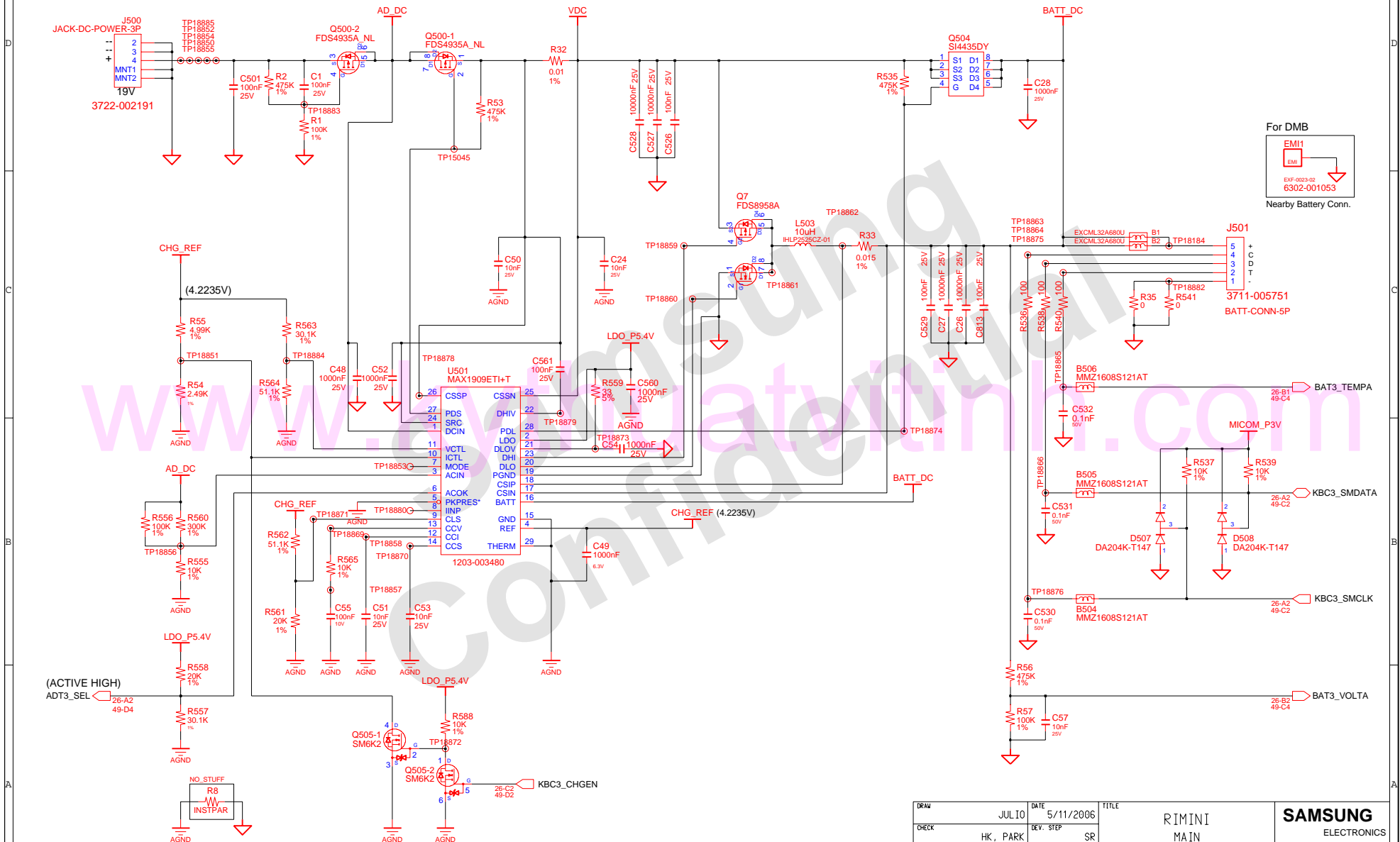


DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR	KBD CONN & DEBUG		
APPROVAL	JS, EUR	REV	1.0	PART NO. BA41-00680(3)A		PAGE 37 OF 50
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM			

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CHARGER & POWER MANAGEMENT



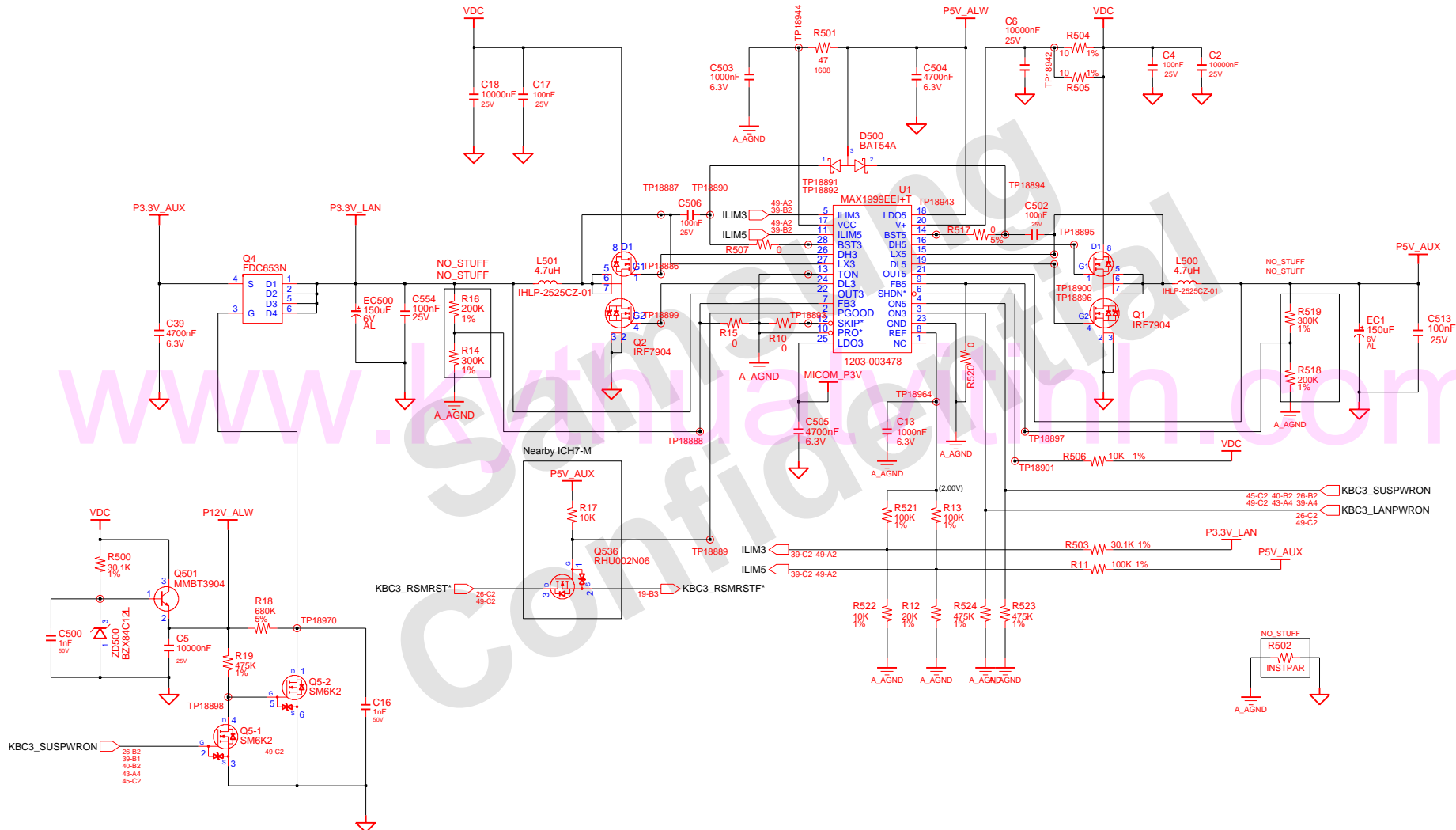
For DMB
EMI1
EM1
EMF-0023-02
6302-001053
Nearby Battery Conn.

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN CHARGER	SAMSUNG ELECTRONICS PART NO. BA41-00680(3)A
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	38 OF 50	

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P5V_AUX & P3.3V_LAN(AUX)

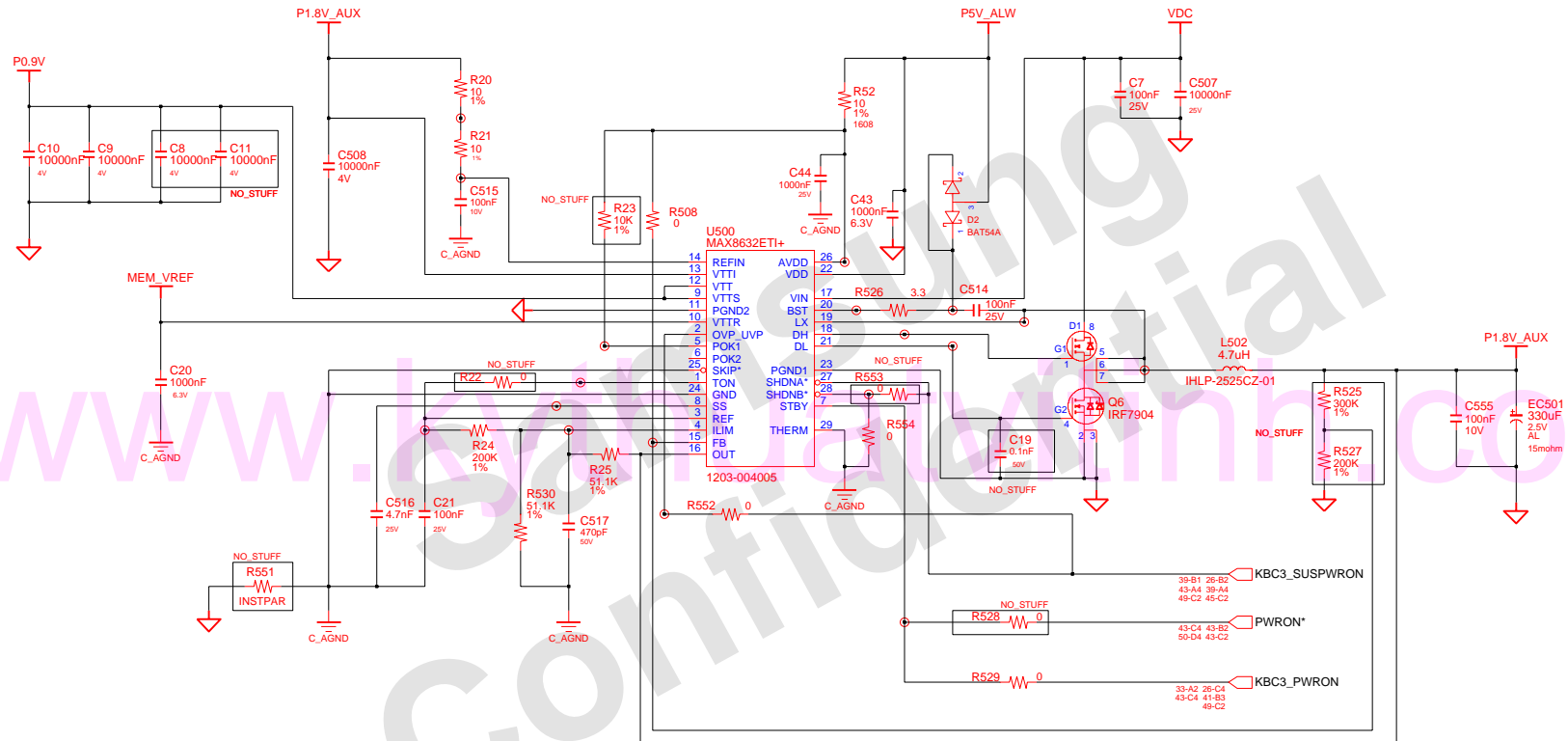


DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR		MAIN	
APPROVAL	JS, EUR	REV	1.0		P5V_AUX & P3.3V_LAN	PART NO. BA41-00680(3)A
MODULE CODE		LAST EDIT			May 11, 2006 10:24:27 PM	PAGE 39 OF 50

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DDR2 POWER

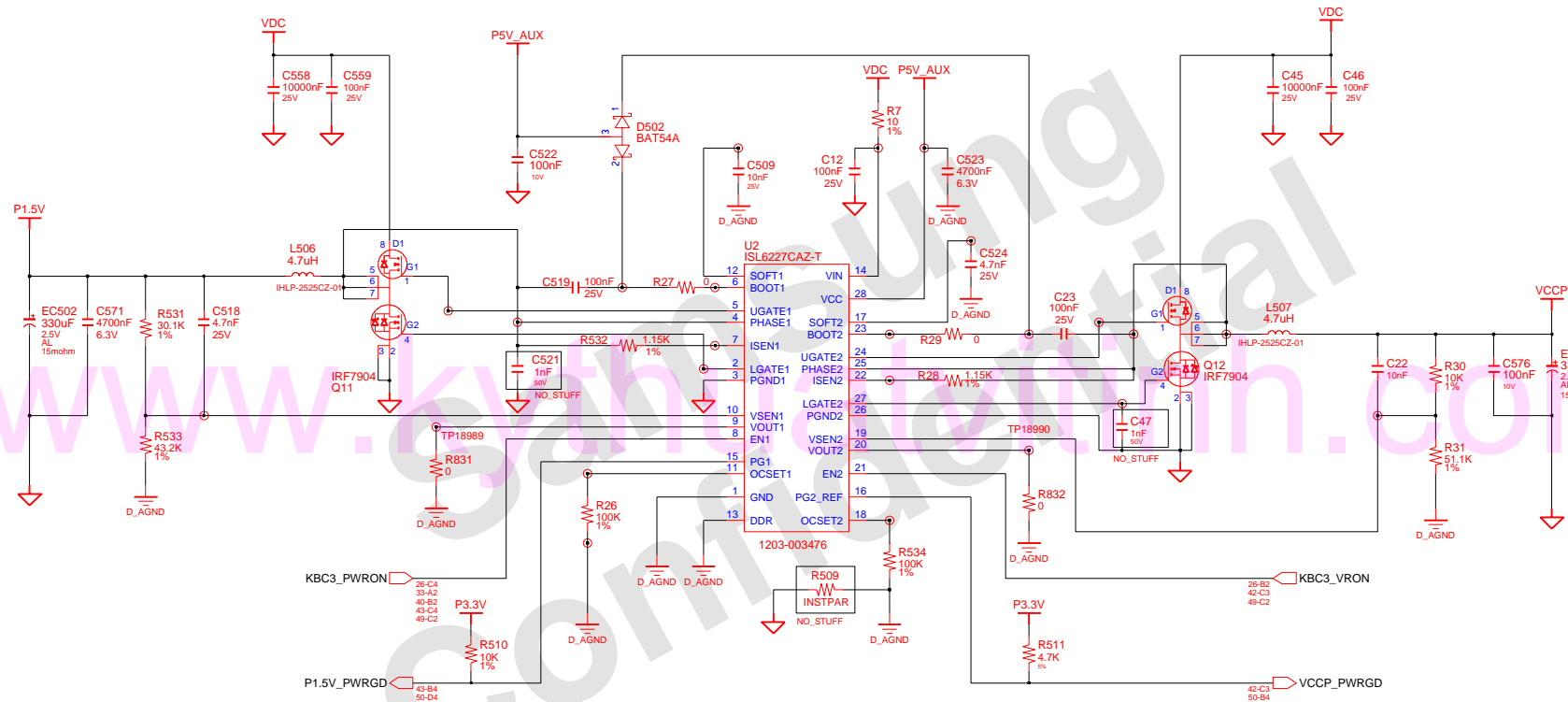


DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN DDR2 POWER	SAMSUNG ELECTRONICS PART NO. BA41-00680(3)A
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE		LAST EDIT				
			May 11, 2006 10:24:27 PM	PAGE	40	OF 50

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P1.5V & VCCP

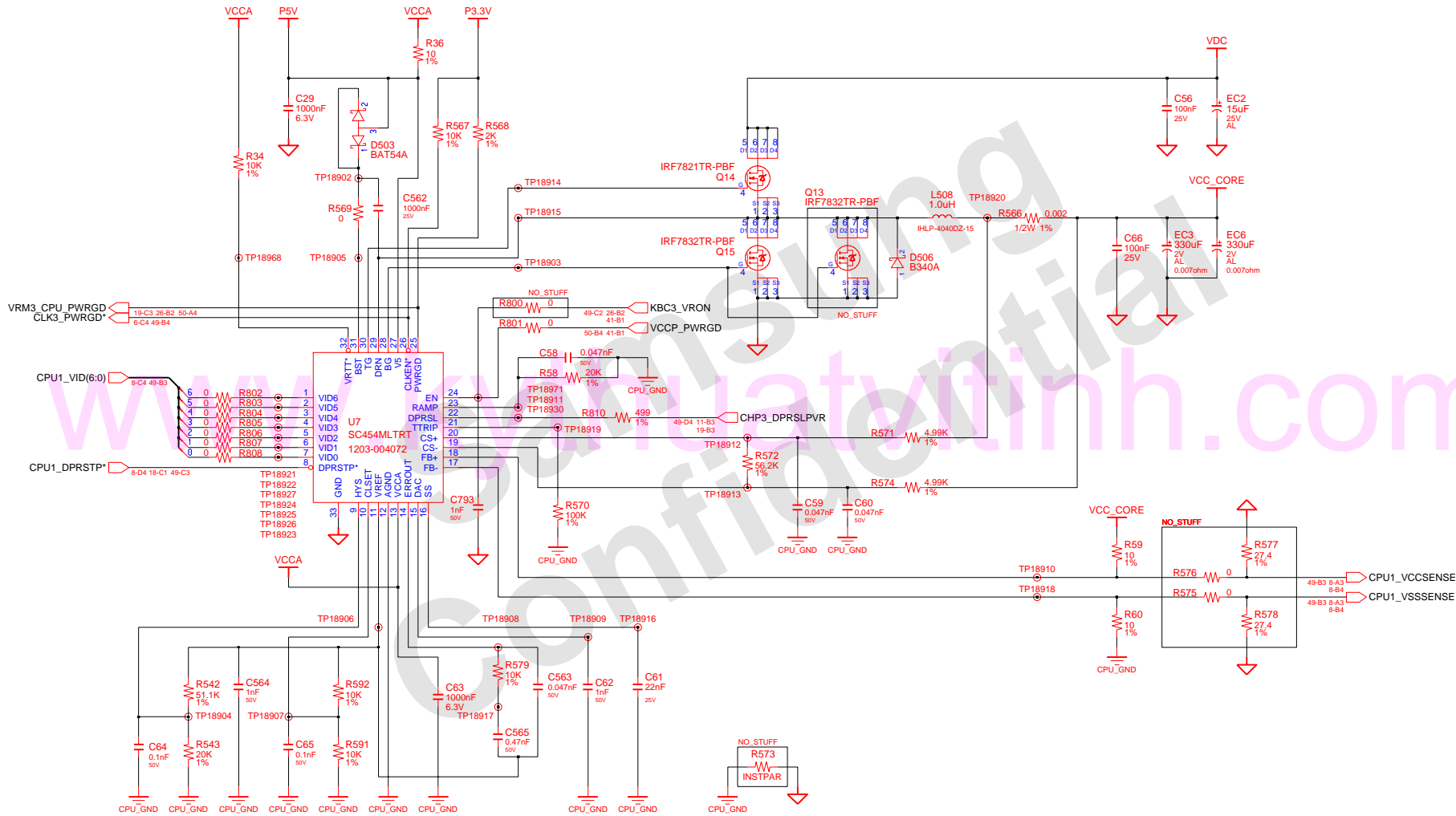


DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0		P1.5V & VCCP	PART NO. BA41-00680(3)A
MODULE CODE		LAST EDIT		May 11, 2006 10:24:27 PM	PAGE	41 OF 50

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CPU VRM POWER

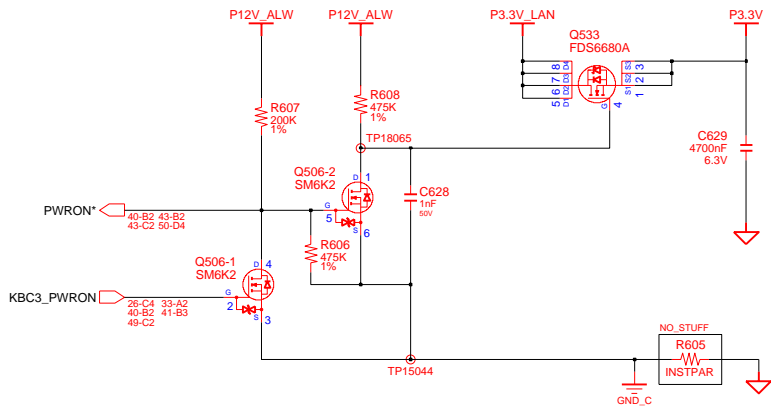


DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN VCC_CORE	SAMSUNG ELECTRONICS PART NO. BA41-00680(3)A
CHECK	HK, PARK	DEV. STEP	SR	APPROVAL	JS, EUR	
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	42	OF 50

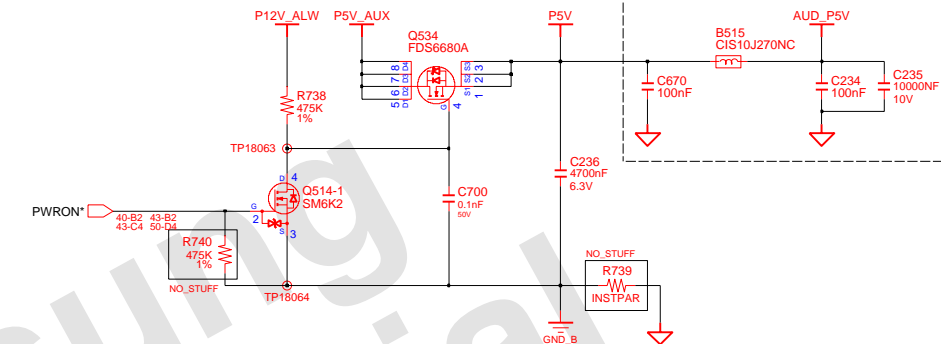
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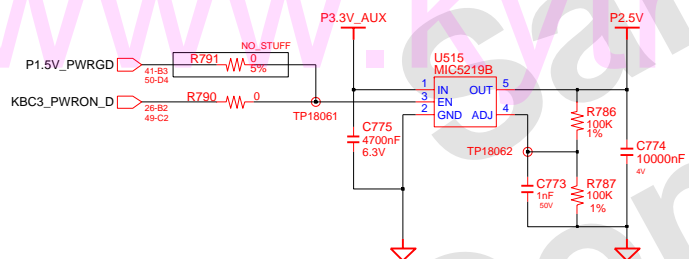
Switched Power On (P3.3V)



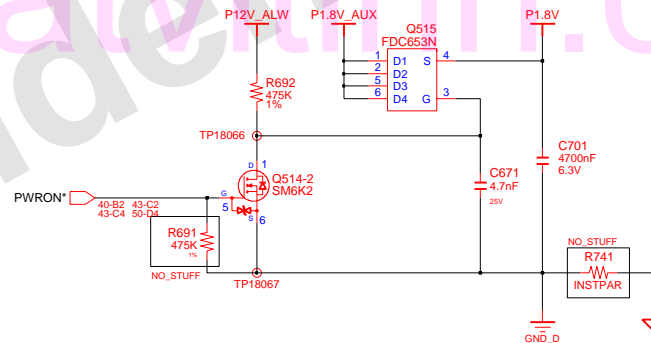
Switched Power On (P5V)



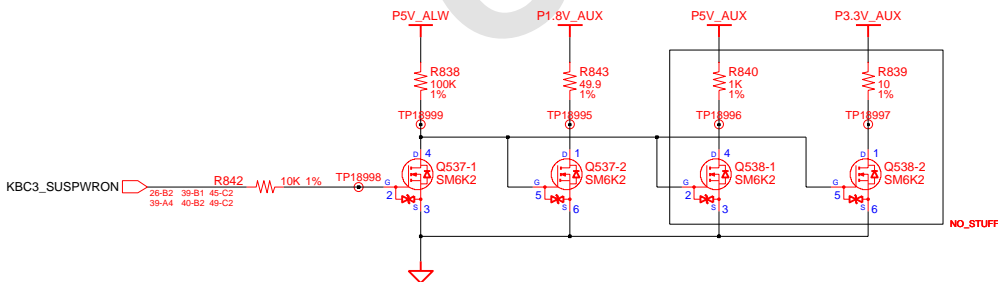
Switched Power On (P2.5V)



Switched Power On (P1.8V)



Discharge Circuit

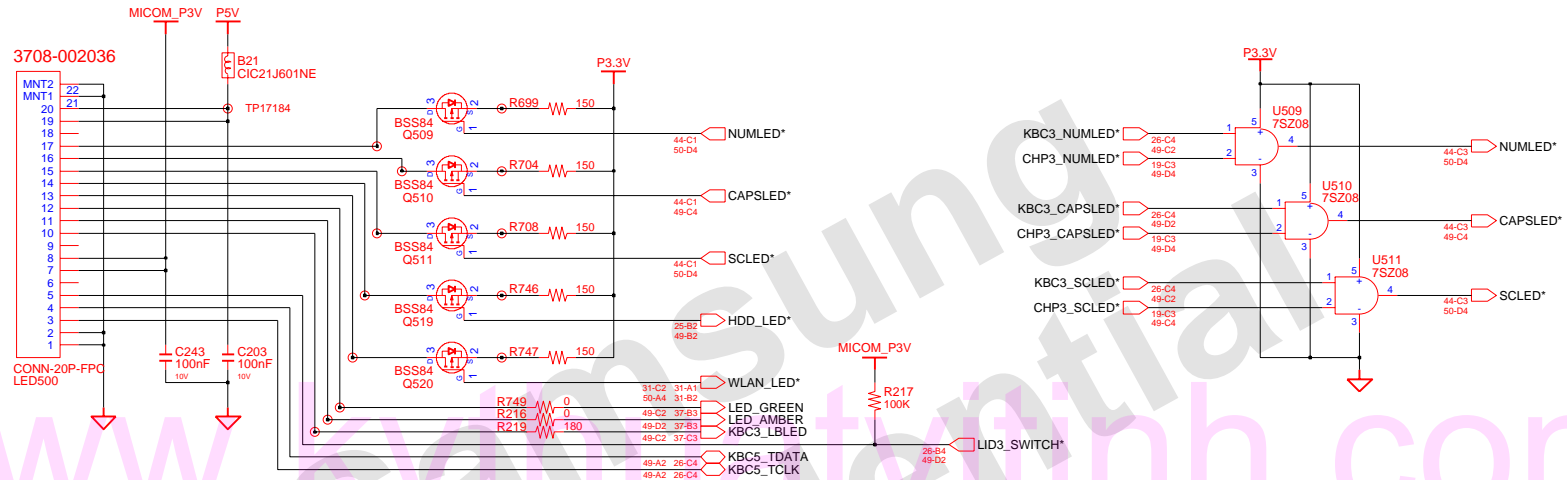


DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN SWITCHED POWER	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR		PART NO. BA41-00680(3)A	
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	43	OF 50

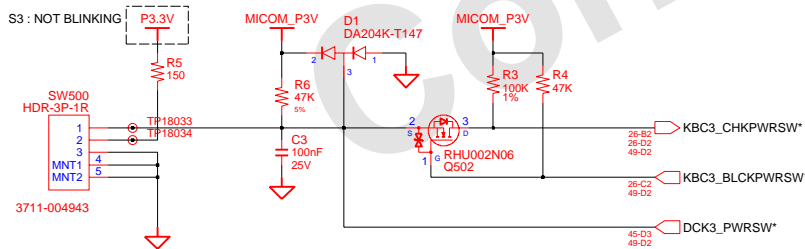
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LED & T/P FPC Conn.



Power Switch Connector



DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN	SAMSUNG ELECTRONICS PART NO. BA41-00680(3)A
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0		LED, TP CONN & POWER SW	
MODULE CODE		LAST EDIT		May 11, 2006 10:24:27 PM	PAGE	44 OF 50

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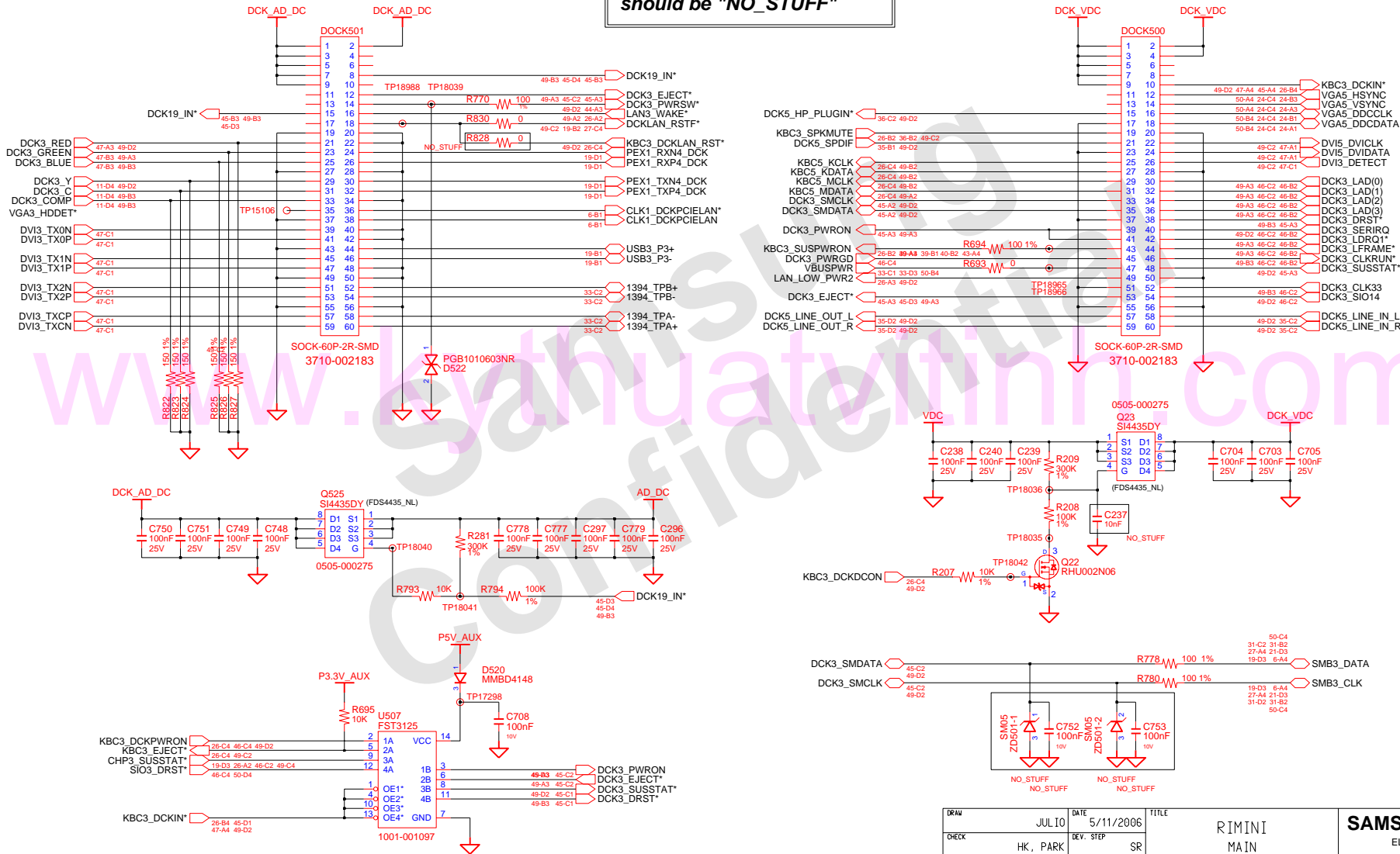
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DOCKING CONNECTOR (124PIN)

In "Without Docking Model" all components of this page should be "NO_STUFF"

Docking Placement

Table with 4 columns: Pin, Position, Top View, and Component. Rows include PWR1, PWR3, 1, 2, 119, 120, PWR4.



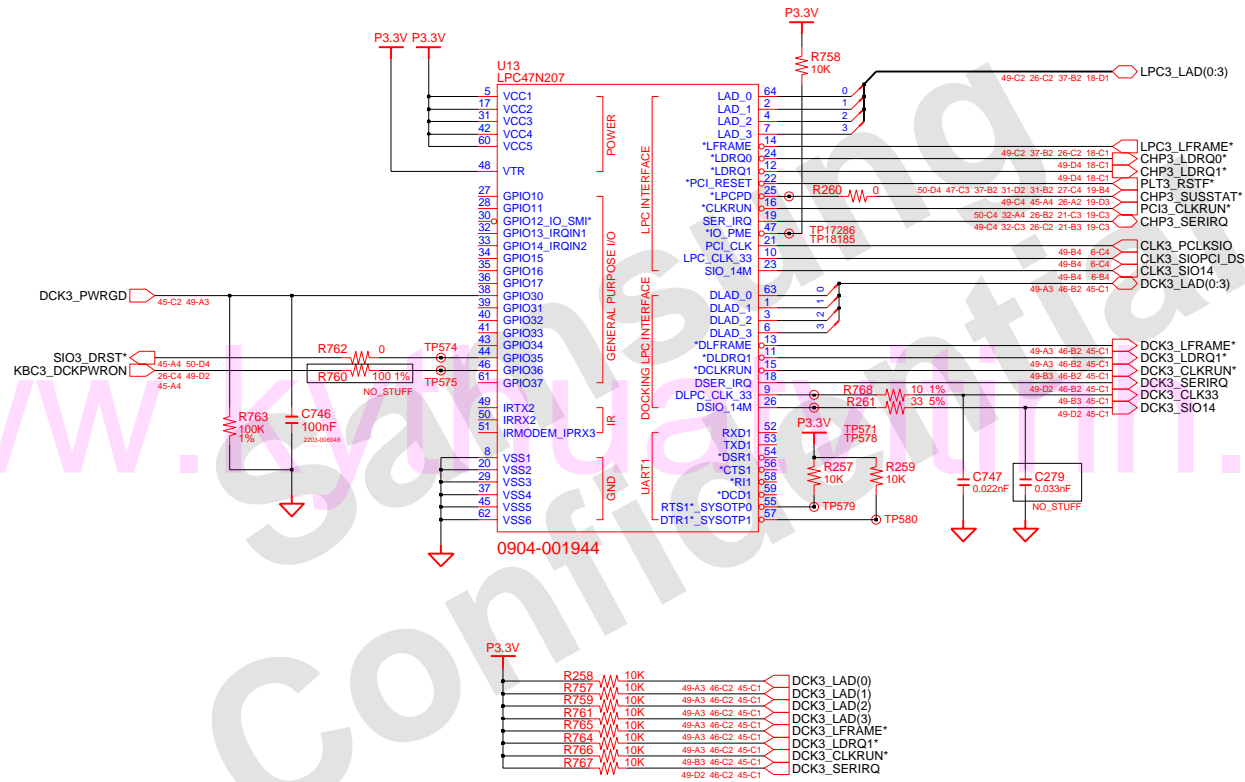
Revision and title block table with columns: DRAW, CHECK, APPROVAL, MODULE CODE, DATE, DEV. STEP, REV, LAST EDIT, TITLE, RIMINI MAIN DOCKING CONN., SAMSUNG ELECTRONICS, PART NO. BA11-00680(3)A, and page number 45 OF 50.

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In "Without Docking Model" all components of this page should be "NO_STUFF"

DOCKING LPC SUPER I/O



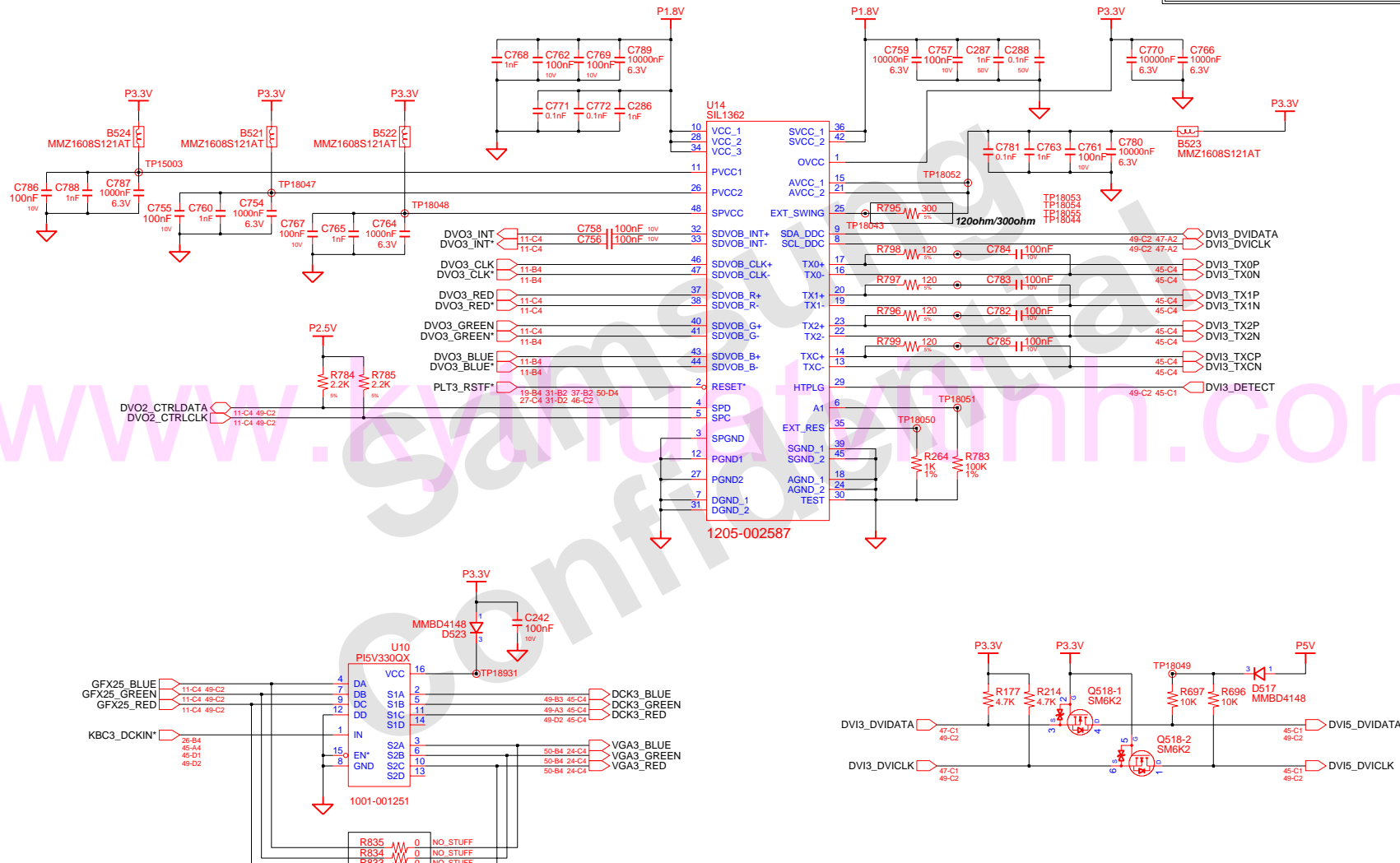
DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN DOCKING LPC	SAMSUNG ELECTRONICS PART NO. BA41-00680(3)A
CHECK	HK, PARK	DEV. STEP	SR	REV	1.0	
APPROVAL	JS, EUR	LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	46	OF 50

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DOCKING DVI

In "Without Docking Model" all components of this page should be "NO_STUFF" (Except R833, R834, R835)

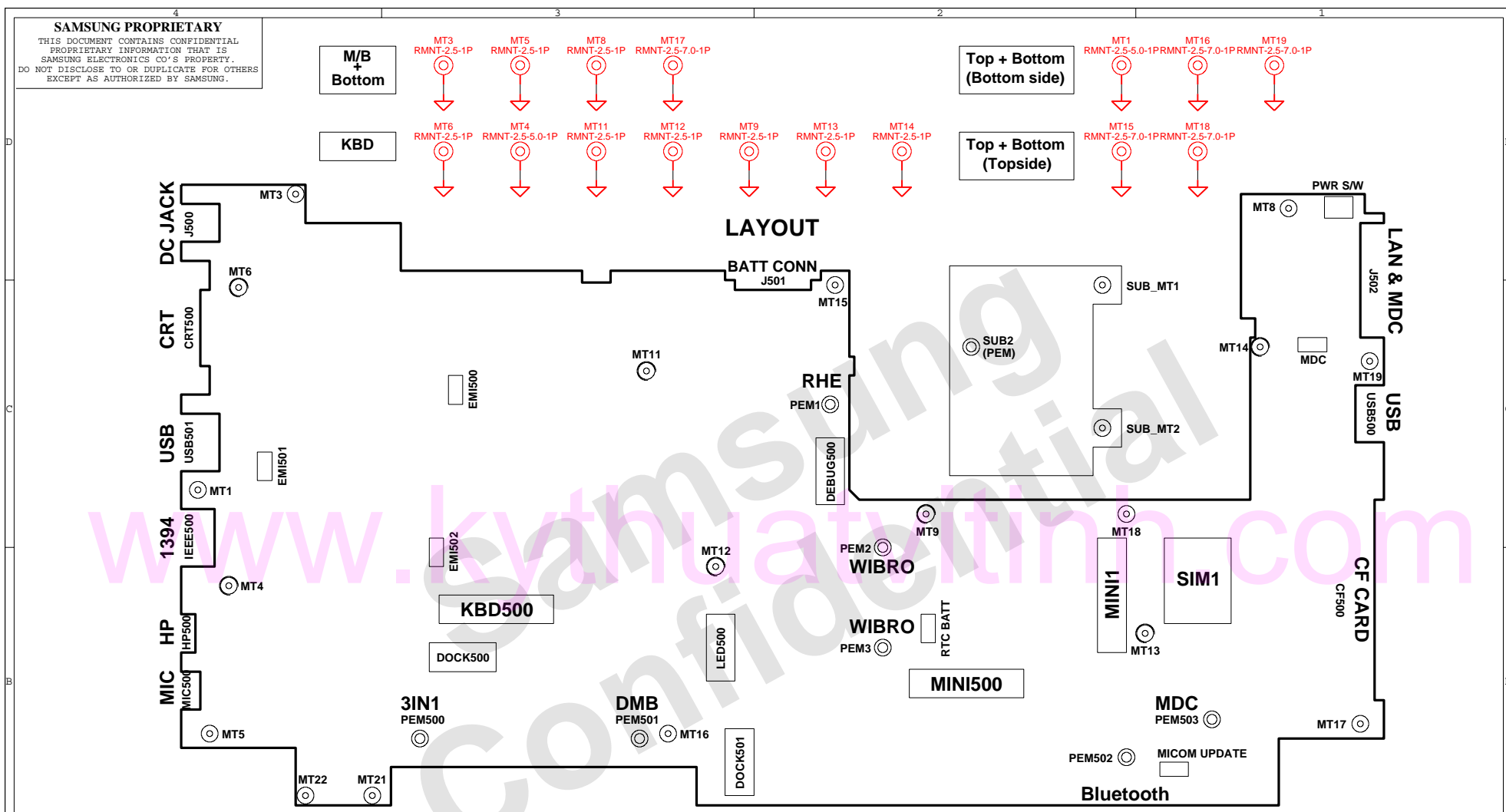


W/O DOCKING : NO_STUFF -> STUFF

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN	SAMSUNG ELECTRONICS
CHECK	HK, PARK	DEV. STEP	SR	PANELLINK TRANSMITTER		
APPROVAL	JS, EUR	REV	1.0	PART NO. BA41-00680(3)A		PAGE 47 OF 50
MODULE CODE	LAST EDIT		May 11, 2006 10:24:27 PM			

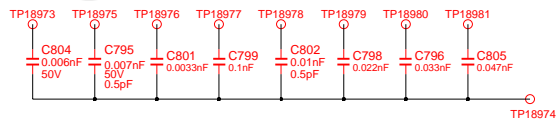
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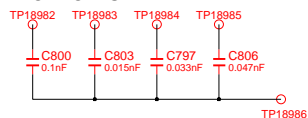


LAYOUT

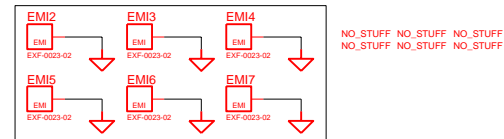
TOP SIDE



BOTTOM SIDE



BOTTOM SIDE EMI CLIP



PCB REVISION CONTROL (ICT)				
NO	CONNECTION	DATE(Y/M/DD)	REVISION	STEP
1	N.C.			
2	1-2			
3	2-3			
4	3-1			
5	1-2-3			
6	N.C.			
7	1-2			
8	2-3			
9	3-1			
10	1-2-3			

REV500
1 0
2 0 03

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN MOUNT HOLE	SAMSUNG ELECTRONICS PART NO. BA41-00680(3)A
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	48 OF 50	

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TP18235OAU3_SEL
 TP18236OAU3_EAPD
 TP18237OAU3_EAPD_A
 TP18238OAU3_PCBEEP
 TP18239OAU5_LINE_OUT_L
 TP18240OAU5_LINE_OUT_R
 TP18241OAU5_SPDIF
 TP18242OAU5_SPDIF_OUT
 TP18243OAU5_SPK_L+
 TP18244OAU5_SPK_L-
 TP18245OAU5_SPK_R+
 TP18246OAU5_SPK_R-
 TP18247OAU3_TEMP
 TP18248OAU3_VOLT_A
 TP18249OAU3_DETECT+
 TP18250OCAPSLED+
 TP18251OCB3_CAD(0)
 TP18252OCB3_CAD(1)
 TP18253OCB3_CAD(10)
 TP18254OCB3_CAD(11)
 TP18255OCB3_CAD(13)
 TP18256OCB3_CAD(14)
 TP18257OCB3_CAD(15)
 TP18258OCB3_CAD(18)
 TP18259OCB3_CAD(19)
 TP18260OCB3_CAD(2)
 TP18261OCB3_CAD(20)
 TP18262OCB3_CAD(21)
 TP18263OCB3_CAD(22)
 TP18264OCB3_CAD(23)
 TP18265OCB3_CAD(24)
 TP18266OCB3_CAD(25)
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 TP18275OCB3_CAD(5)
 TP18276OCB3_CAD(6)
 TP18277OCB3_CAD(7)
 TP18278OCB3_CAD(8)
 TP18279OCB3_CAD(9)
 TP18280OCB3_CAUD10
 TP18281OCB3_CCB6+
 TP18282OCB3_CCB6-
 TP18283OCB3_CCB6+3
 TP18284OCB3_CCD1+
 TP18285OCB3_CCD2+
 TP18286OCB3_CCLERUN+
 TP18287OCB3_CCN1+
 TP18288OCB3_CCN1+
 TP18289OCB3_CCN1+
 TP18290OCB3_CRS1+
 TP18291OCB3_CSTRERR+
 TP18292OCB3_CSTSCHG
 TP18293OCB3_CVS1
 TP18294OCB3_CVS2
 TP18295OCB3_D14
 TP18296OCB3_D2
 TP18297OCB3_SD_VCCEN
 TP18298OCB3_SPKR
 TP18299OCB3_VCCSEN+
 TP18300OCB3_VCCSEN+
 TP18301OCB3_VPPEN0
 TP18302OCB3_VPPEN1
 TP18303OHP3_1394_ROM+
 TP18304OHP3_AZ_AUD_BOLK
 TP18305OHP3_AZ_AUD_RST+
 TP18306OHP3_AZ_AUD_SD10
 TP18307OHP3_AZ_AUD_SDO
 TP18308OHP3_AZ_AUD_SYNC
 TP18309OHP3_AZ_MDC_BOLK
 TP18310OHP3_AZ_MDC_RST+

TP18311OHP3_AZ_MDC_SD11
 TP18312OHP3_AZ_MDC_SDO
 TP18313OHP3_AZ_MDC_SYNC
 TP18314OHP3_BIOS_TBL+
 TP18315OHP3_BIOS_V+
 TP18316OHP3_CAPSLED+
 TP18317OHP3_CPUSTP+
 TP18320OHP3_DMBON
 TP18318OHP3_DPSL_PVR
 TP18319OHP3_TLTPURON
 TP18320OHP3_LDR00+
 TP18321OHP3_LDR01+
 TP18322OHP3_NUMLED+
 TP18323OHP3_PC151F+
 TP18324OHP3_PME+
 TP18325OHP3_RTCRST+
 TP18326OHP3_SCLD+
 TP18327OHP3_SERIRQ
 TP18328OHP3_SLPS3+
 TP18329OHP3_SLPS4+
 TP18330OHP3_SLPS5+
 TP18331OHP3_SMLINK0
 TP18332OHP3_SMLINK1
 TP18333OHP3_SPK6
 TP18334OHP3_SUSSTAT+
 TP18335OCLK3_DBGLPC
 TP18336OCLK3_ICH14
 TP18337OCLK3_MS49
 TP18338OCLK3_PCLKCB
 TP18340OCLK3_PCLKICH
 TP18341OCLK3_PCLKM10M
 TP18342OCLK3_PCLKS10
 TP18343OCLK3_PWRGD+
 TP18344OCLK3_S1014
 TP18345OCLK3_S10PC_LDS
 TP18346OCLK3_SMBCLK
 TP18347OCLK3_SMBDATA
 TP18348OCLK3_USB48
 TP18349OCODEX1
 TP18350OCODEX2

TP18351OCPU1_A20M+
 TP18352OCPU1_ADS+
 TP18353OCPU1_BNR+
 TP18354OCPU1_BP1+
 TP18355OCPU1_BREQ+
 TP18356OCPU1_BSEL0
 TP18357OCPU1_BSEL1
 TP18358OCPU1_BSEL2
 TP18359OCPU1_CPRST+

TP18360OCPU1_DBSY+
 TP18361OCPU1_DEFFER+
 TP18362OCPU1_DPRSFP+
 TP18363OCPU1_DPSLP+
 TP18364OCPU1_DPWR+
 TP18365OCPU1_DRDY+
 TP18366OCPU1_FERR+
 TP18367OCPU1_HIT+
 TP18368OCPU1_HITM+
 TP18369OCPU1_IGNNE+
 TP18370OCPU1_INIT+
 TP18371OCPU1_INTR+
 TP18372OCPU1_LOCK+
 TP18373OCPU1_NMI+
 TP18374OCPU1_PWRGDPU

TP18375OCPU1_SLP+
 TP18376OCPU1_SM1+
 TP18377OCPU1_STPCLK+
 TP18378OCPU1_THRTRIP+
 TP18379OCPU1_TRDY+
 TP18380OCPU1_VCCSENSE
 TP18381OCPU1_VID(0)
 TP18382OCPU1_VID(1)
 TP18383OCPU1_VID(2)
 TP18384OCPU1_VID(3)
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 TP18387OCPU1_VID(6)
 TP18388OCPU1_VSSSENSE
 TP18389OCPU2_THERMDA
 TP18390OCPU2_THERMDC
 TP18391OCCK18_BLUE
 TP18392OCCK3_C
 TP18394OCCK3_CLK33
 TP18395OCCK3_CLKRUN+
 TP18396OCCK3_COMP
 TP18397OCCK3_DRS+
 TP18398OCCK3_EJECT+
 TP18399OCCK3_GREEN
 TP18400OCCK3_LAD(0)
 TP18401OCCK3_LAD(1)
 TP18402OCCK3_LAD(2)
 TP18403OCCK3_LAD(3)
 TP18404OCCK3_LDR01+
 TP18405OCCK3_LFRAME+
 TP18406OCCK3_PWRGD
 TP18407OCCK3_PURON

TP18408OCCK3_RED
 TP18409OCCK3_SERIRQ
 TP18410OCCK3_S1014
 TP18411OCCK3_SMCLK
 TP18412OCCK3_SMDATA
 TP18413OCCK3_SUSSTAT+
 TP18414OCCK3_Y
 TP18415OCCK5_HP_PLUGIN+
 TP18416OCCK5_LINE_IN_L
 TP18417OCCK5_LINE_IN_R
 TP18418OCCK5_LINE_OUT_L
 TP18419OCCK5_LINE_OUT_R
 TP18420OCCK5_SPDIF
 TP18421OCCKLAN_RSTF+
 TP18730ODV13_DETECT
 TP18733ODV13_DVIOCLK
 TP18734ODV13_DVIDATA
 TP18707ODV15_DVIOCLK
 TP18708ODV15_DVIDATA
 TP18422ODV02_CTRLCLK
 TP18423ODV02_CTRLDATA

TP18435OCF_X25_BLUE
 TP18436OCF_X25_GREEN
 TP18437OCF_X25_RED
 TP18438OCMCH1_HVREF
 TP18439OCMCH1_HYSWING
 TP18440OCMCH1_HYSWING
 TP18441OCMCH3_BMBUS+
 TP18442OCMCH3_CLKREQ+
 TP18443OCMCH3_EXTTSG+
 TP18444OCMCH3_ICHSYNC+
 TP18445OHP_DETECT
 TP18446OHP_OUT1
 TP18447OHP_OUT2
 TP18448OHP_OUT3
 TP18449OIDE_A0
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 TP18451OIDE_A2
 TP18452OIDE_CS1+
 TP18453OIDE_CS3+
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 TP18469OIDE_D(9)
 TP18470OIDE_DACK+
 TP18471OIDE_D(0)
 TP18472OIDE_IOR+
 TP18473OIDE_IORDY
 TP18474OIDE_IOW+
 TP18475OIDE_IRQ
 TP18476OILIN3
 TP18477OILIM5
 TP18478OTP3_SYRST+
 TP18479OJCK_SENS
 TP18480OJCK_SENS_A
 TP18481OJCK_SENS_B

TP18480OJCK_SENS_HP
 TP18481OJCK_SENS_MIC
 TP18482OKBC3_A20G
 TP18483OKBC3_BKLTON
 TP18484OKBC3_BLCKPWRSH+
 TP18485OKBC3_CAPSLED+
 TP18486OKBC3_CHGEN
 TP18487OKBC3_CHK_PWRSH+
 TP18488OKBC3_CPUPWRGD_D
 TP18489OKBC3_CPURST+
 TP18490OKBC3_DCKOCON
 TP18491OKBC3_DCKIN+
 TP18492OKBC3_DCKLAN_RST+
 TP18493OKBC3_DCK_PURON
 TP18494OKBC3_EJECT+
 TP18495OKBC3_EXTSM1+
 TP18496OKBC3_LAN_PURON
 TP18497OKBC3_LBLEED
 TP18498OKBC3_LED_AGIN+
 TP18499OKBC3_LED_CHARGE+
 TP18500OKBC3_LED_POWER+
 TP18501OKBC3_MINI_WIBRO_ON+
 TP18502OKBC3_MINI_WL_ON+
 TP18503OKBC3_NUMLED+
 TP18504OKBC3_PMBRIT
 TP18505OKBC3_PWRBTN+
 TP18506OKBC3_PWRGD
 TP18507OKBC3_PURON
 TP18508OKBC3_PURON_D
 TP18509OKBC3_RFOFF+
 TP18510OKBC3_RSMRST+
 TP18511OKBC3_RST+
 TP18512OKBC3_RUNWSCI+
 TP18513OKBC3_SCLD+
 TP18514OKBC3_SMCLK
 TP18515OKBC3_SMDATA
 TP18516OKBC3_SPMUTE
 TP18517OKBC3_SUS_PURON
 TP18518OKBC3_THERM_SMCLK
 TP18519OKBC3_THERM_SMDATA
 TP18520OKBC3_USB_EN+
 TP18521OKBC3_VRON
 TP18522OKBC3_WAKESC1+
 TP18523OKBC5_K0K
 TP18524OKBC5_K0A1
 TP18525OKBC5_K0S1(1)
 TP18526OKBC5_K0S1(2)
 TP18527OKBC5_K0S1(3)
 TP18528OKBC5_K0S1(4)
 TP18529OKBC5_K0S1(5)
 TP18530OKBC5_K0S1(6)
 TP18531OKBC5_K0S1(7)
 TP18532OKBC5_K0S1(8)
 TP18533OKBC5_K0S1(9)
 TP18534OKBC5_K0S1(10)
 TP18535OKBC5_K0S1(11)
 TP18536OKBC5_K0S1(12)
 TP18537OKBC5_K0S1(13)
 TP18538OKBC5_K0S1(14)
 TP18539OKBC5_K0S1(15)
 TP18540OKBC5_K0S1(2)
 TP18541OKBC5_K0S1(3)
 TP18542OKBC5_K0S1(4)
 TP18543OKBC5_K0S1(5)
 TP18544OKBC5_K0S1(6)
 TP18545OKBC5_K0S1(7)
 TP18546OKBC5_K0S1(8)
 TP18547OKBC5_K0S1(9)
 TP18548OKBC5_MDATA
 TP18549OKBC5_TCLK
 TP18550OKBC5_TDATA

TP18551OLAN_LOW_PWR
 TP18552OLAN_LOW_PWR2
 TP18844QLCD3_BKL_TEN
 TP18845QLCD3_BKL_TON
 TP18855QLCD3_PMBDIA
 TP18856QLCD3_VDDEN
 TP18857OLED_AMBER
 TP18858OLED_GREEN
 TP18859OLPC3_LAD(0)
 TP18860OLPC3_LAD(1)
 TP18861OLPC3_LAD(2)
 TP18862OLPC3_LAD(3)
 TP18863OLPC3_LFRAME+

TP18844QLAN3_SMB_CLK
 TP18845QLAN3_SMB_DATA
 TP18849OJCK_SENS_B
 TP18564OMIC1
 TP18565OMIC2
 TP18566MINIPCIE3_CLKREQ1+
 TP18567MINIPCIE3_CLKREQ2+

DRAW	JUL10	DATE	5/11/2006	TITLE	RIMINI MAIN TEST POINTS(1)	SAMSUNG ELECTRONICS PART NO. BA41-00680(3)A
CHECK	HK, PARK	DEV. STEP	SR			
APPROVAL	JS, EUR	REV	1.0			
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	49 OF 50	

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TP18809ONUMLED+
 TP18810OP1_5V_PWRGD
 TP18811OPIC3_AD(8)
 TP18812OPIC3_AD(1)
 TP18813OPIC3_AD(10)
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 TP18815OPIC3_AD(12)
 TP18816OPIC3_AD(13)
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 TP18818OPIC3_AD(15)
 TP18819OPIC3_AD(16)
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 TP18821OPIC3_AD(18)
 TP18822OPIC3_AD(19)
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 TP18828OPIC3_AD(24)
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 TP18833OPIC3_AD(29)
 TP18834OPIC3_AD(3)
 TP18835OPIC3_AD(30)
 TP18836OPIC3_AD(31)
 TP18837OPIC3_AD(4)
 TP18838OPIC3_AD(5)
 TP18839OPIC3_AD(6)
 TP18840OPIC3_AD(7)
 TP18777OPIC3_AD(8)
 TP18778OPIC3_AD(9)
 TP18779OPIC3_CBE0+
 TP18780OPIC3_CBE1+
 TP18781OPIC3_CBE2+
 TP18782OPIC3_CBE3+
 TP18783OPIC3_CLKRUN+
 TP18784OPIC3_DEVSEL+
 TP18785OPIC3_FRAME+
 TP18786OPIC3_CNT0+
 TP18787OPIC3_INTA+
 TP18788OPIC3_INTB+
 TP18789OPIC3_INTC+
 TP18790OPIC3_INTD+
 TP18791OPIC3_INTE+
 TP18792OPIC3_INTF+
 TP18793OPIC3_INTG+
 TP18794OPIC3_INTH+
 TP18795OPIC3_IRDY+
 TP18796OPIC3_PAR+
 TP18797OPIC3_PERR+
 TP18798OPIC3_PLCK+
 TP18799OPIC3_RE0+
 TP18800OPIC3_RE01+
 TP18801OPIC3_RE02+
 TP18802OPIC3_RE03+
 TP18803OPIC3_RS1+
 TP18804OPIC3_SERR+
 TP18805OPIC3_STOP+
 TP18806OPIC3_TREY+

TP18807OPEX3_WAKE+
 TP18808OPL13_RST+
 TP18745OPL13_RSTF+
 TP18747OPWRON+
 TP18748OCLCD+
 TP18749OSIM_C1
 TP18750OSIM_C2
 TP18751OSIM_C3
 TP18752OSIM_C4
 TP18753OSIM_C6
 TP18754OSIM_C7
 TP18755OSIM_C8
 TP18756OSI03_DRST+
 TP18757OSMB3_ALERT+
 TP18758OSMB3_CLK
 TP18759OSMB3_DATA
 TP18760OSMB3_LINKALERT+
 TP18761OSPI_CLK
 TP18762OSPI_CS+
 TP18763OSPI_MISO
 TP18764OSPI_MOSI

TP18775OTHERM_ALERT+
 TP18776OTHERM_STP+

TP18727OVBUSPWR
 TP18728OVCCP_PWRGD
 TP18729OVGA3_BLUE

TP18731OVGA3_DDCCLK
 TP18732OVGA3_DDCDATA

TP18735OVGA3_GREEN
 TP18736OVGA3_HSYNC
 TP18737OVGA3_RED

TP18704OVGA3_VSYNC
 TP18705OVGA5_DDCCLK
 TP18706OVGA5_DDCDATA

TP18709OVGA5_HSYNC
 TP18710OVGA5_VSYNC
 TP18711OVWMS3_CPU_PWRGD
 TP18712OVLAN_LED+

TP18186OAD_DC
 TP18187OAD_DC
 TP18188OAD_DC
 TP18189OAD_DC
 TP18190OAGND
 TP18191OAGND
 TP18192OAGND
 TP18193OAGND
 TP18194OAGND_AUD
 TP18195OAGND_AUD
 TP18196OAGND_AUD
 TP18197OAGND_AUD
 TP18198OAMP_VDD
 TP18199OAMP_VDD

TP18202OAUD_P5V
 TP18203OAUD_P5V
 TP18204OAUD_P5V
 TP18205OAUD_P5V
 TP18206OAVDD
 TP18207OAVDD
 TP18208OAVDD
 TP18209OAVDD

TP18210OA_AGNND
 TP18211OA_AGNND
 TP18212OA_AGNND
 TP18213OA_AGNND
 TP18214OBATT_DC
 TP18215OBATT_DC
 TP18216OBATT_DC
 TP18217OBATT_DC

TP18218OCB_SD_VCC
 TP18219OCB_SD_VCC
 TP18220OCB_SD_VCC
 TP18221OCB_SD_VCC
 TP18222OCB_VCC
 TP18223OCB_VCC
 TP18224OCB_VCC

TP18225OCB_VCC
 TP18226OCHG_REF
 TP18227OCHG_REF
 TP18228OCHG_REF
 TP18229OCHG_REF
 TP18230OCPU_GND
 TP18231OCPU_GND
 TP18232OCPU_GND
 TP18233OCPU_GND

TP18234OC_AGNND
 TP18569OC_AGNND
 TP18570OC_AGNND
 TP18571ODCK_AD_DC
 TP18572ODCK_AD_DC
 TP18573ODCK_AD_DC
 TP18574ODCK_AD_DC

TP18575ODCK_VDC
 TP18576ODCK_VDC
 TP18577ODCK_VDC
 TP18578ODCK_VDC
 TP18579OQND_B
 TP18580OQND_B

TP18583OQND_D
 TP18584OQND_D
 TP18585OQND_D
 TP18586OQND_D

TP18591OINV_VDC
 TP18592OINV_VDC
 TP18593OINV_VDC
 TP18594OINV_VDC
 TP18595OQND_VDD3V
 TP18596OQND_VDD3V

TP18599OLD0_P5_4V
 TP18600OLD0_P5_4V
 TP18601OLD0_P5_4V
 TP18602OLD0_P5_4V
 TP18603OMEM_VREF
 TP18604OMEM_VREF
 TP18605OMEM_VREF
 TP18606OMEM_VREF
 TP18607OMICOM_P3V
 TP18608OMICOM_P3V
 TP18609OMICOM_P3V
 TP18610OMICOM_P3V
 TP18611OMINI_P1_5V_WB
 TP18612OMINI_P1_5V_WB
 TP18613OMINI_P1_5V_WB

TP18614OMINI_P1_5V_WB
 TP18615OMINI_P1_5V_WL
 TP18616OMINI_P1_5V_WL
 TP18617OMINI_P1_5V_WL
 TP18618OMINI_P1_5V_WL
 TP18619OMINI_P3_3V_WB
 TP18620OMINI_P3_3V_WB
 TP18621OMINI_P3_3V_WB
 TP18622OMINI_P3_3V_WB

TP18623OMINI_P3_3V_WL
 TP18624OMINI_P3_3V_WL
 TP18625OMINI_P3_3V_WL
 TP18626OMINI_P3_3V_WL
 TP18627OP0_9V
 TP18628OP0_9V
 TP18629OP0_9V
 TP18630OP0_9V

TP18631OP1_2V_LAN
 TP18632OP1_2V_LAN
 TP18633OP1_2V_LAN
 TP18634OP1_2V_LAN
 TP18635OP1_5V
 TP18636OP1_5V
 TP18637OP1_5V
 TP18638OP1_5V

TP18639OP1_5V_PCIE
 TP18640OP1_5V_PCIE
 TP18641OP1_5V_PCIE
 TP18642OP1_5V_PCIE
 TP18643OP1_8V_AUX
 TP18644OP1_8V_AUX
 TP18645OP1_8V_AUX
 TP18646OP1_8V_AUX

TP18647OP12V_ALW
 TP18648OP12V_ALW
 TP18649OP12V_ALW
 TP18650OP12V_ALW
 TP18651OP2_5V
 TP18652OP2_5V
 TP18653OP2_5V
 TP18654OP2_5V

TP18655OP2_5V_LAN
 TP18656OP2_5V_LAN
 TP18657OP2_5V_LAN
 TP18658OP2_5V_LAN
 TP18659OP3_3V_AUX
 TP18660OP3_3V_AUX
 TP18661OP3_3V_AUX
 TP18662OP3_3V_AUX

TP18663OP3_3V_LAN
 TP18664OP3_3V_LAN
 TP18665OP3_3V_LAN
 TP18666OP3_3V_LAN
 TP18667OP5V
 TP18668OP5V
 TP18669OP5V
 TP18670OP5V

TP18671OP5V_ALW
 TP18672OP5V_ALW
 TP18673OP5V_ALW
 TP18674OP5V_ALW
 TP18675OPRTC_BAT
 TP18676OPRTC_BAT
 TP18677OPRTC_BAT
 TP18678OPRTC_BAT

TP18683OVCCA
 TP18684OVCCA
 TP18685OVCCA
 TP18686OVCCA
 TP18687OVCCP
 TP18688OVCCP
 TP18689OVCCP
 TP18690OVCCP
 TP18691OVCC_CORE
 TP18692OVCC_CORE
 TP18693OVCC_CORE
 TP18694OVCC_CORE
 TP18695OVCC_CRT
 TP18696OVCC_CRT
 TP18697OVCC_CRT
 TP18698OVCC_CRT

TP18699OVDC
 TP18700OVDC
 TP18701OVDC
 TP18702OVDC

TP18949OGROUND
 TP18950OGROUND
 TP18951OGROUND
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 TP18954OGROUND
 TP18955OGROUND
 TP18956OGROUND

TP18957OGROUND
 TP18958OGROUND
 TP18959OGROUND
 TP18960OGROUND
 TP18961OGROUND
 TP18962OGROUND
 TP18963OGROUND

DRAW	JULIO	DATE	5/11/2006	TITLE	RIMINI MAIN TEST POINTS(2)	SAMSUNG ELECTRONICS PART NO. BA41-00680(3)A
CHECK	HK, PARK	DEV. STEP	SR	APPROVAL	JS, EUR	
MODULE CODE		LAST EDIT	May 11, 2006 10:24:27 PM	PAGE	50	OF 50