

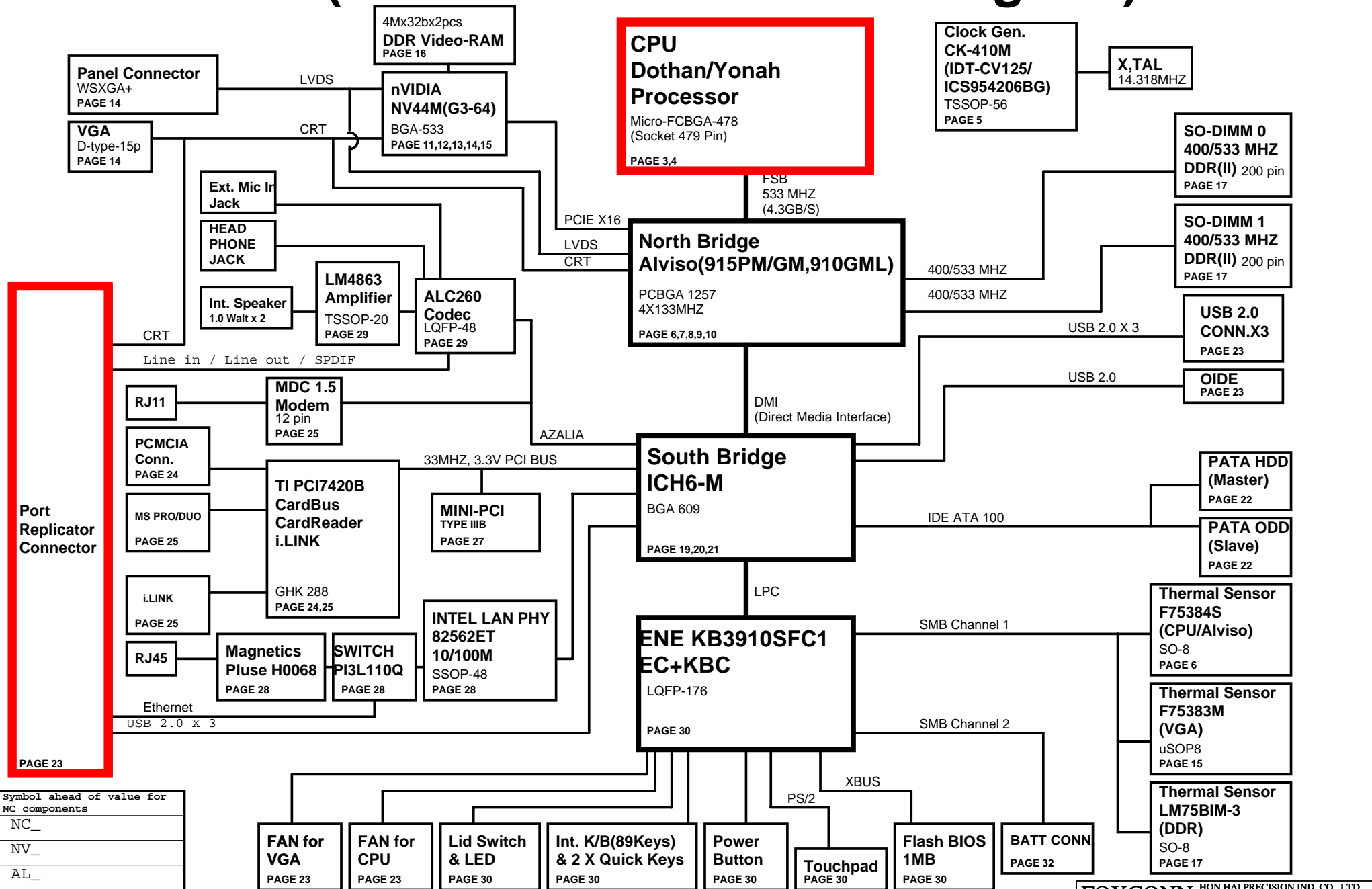
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22	IDE (HDD&CD_ROM)	1.00	051123				
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24	PCI7420B(PCMCIA)	1.00	051123				
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Project Code & Schematics Subject:	MS04 M/B-FUBAI	PCB P/N:	1P-005B100-8012
Project Code & Schematics Subject:	MS04 M/B-HANNSTAR	PCB P/N:	1P-005B500-8012
Project Code & Schematics Subject:	MS04 M/B-NAN YA	PCB P/N:	1P-005B200-8012

FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title Index Page			
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MS04(915PM/GM+Gfx Block Diagram)



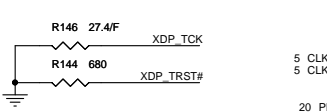
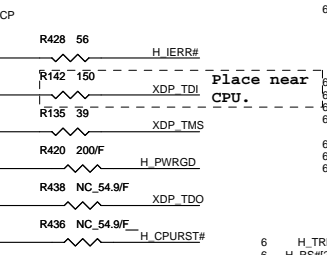
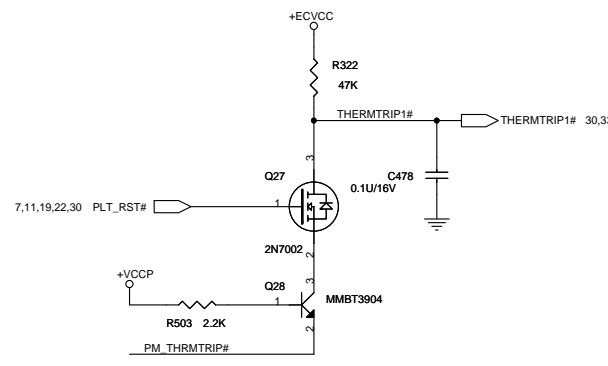
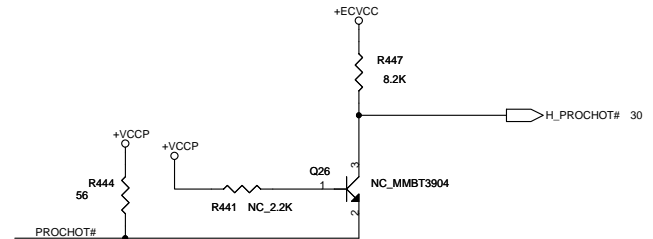
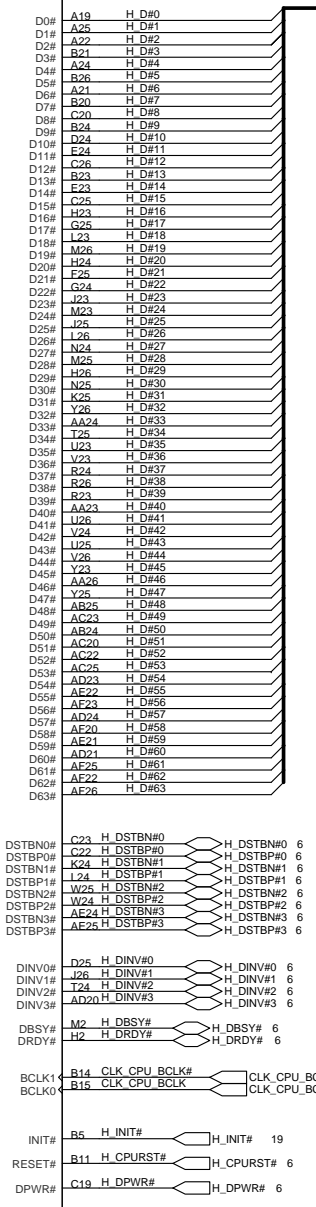
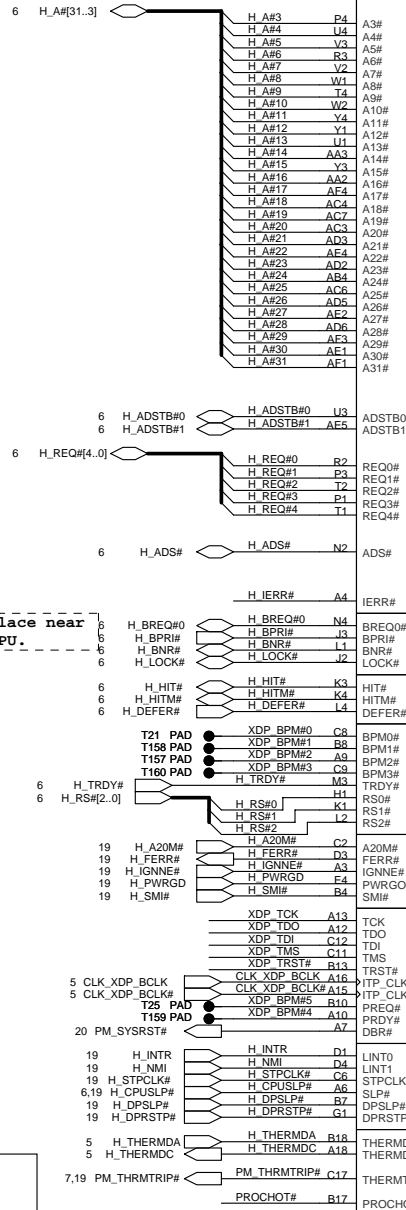
Symbol ahead of value for NC components	
ALL	NC_
915PM + NV44M	NV_
915GM or 910GML	AL_
910GML	LNC_
915PM + NV44M or 915GM	HMNC_

BOM configuration

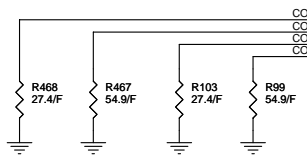
Dothan

1 OF 3

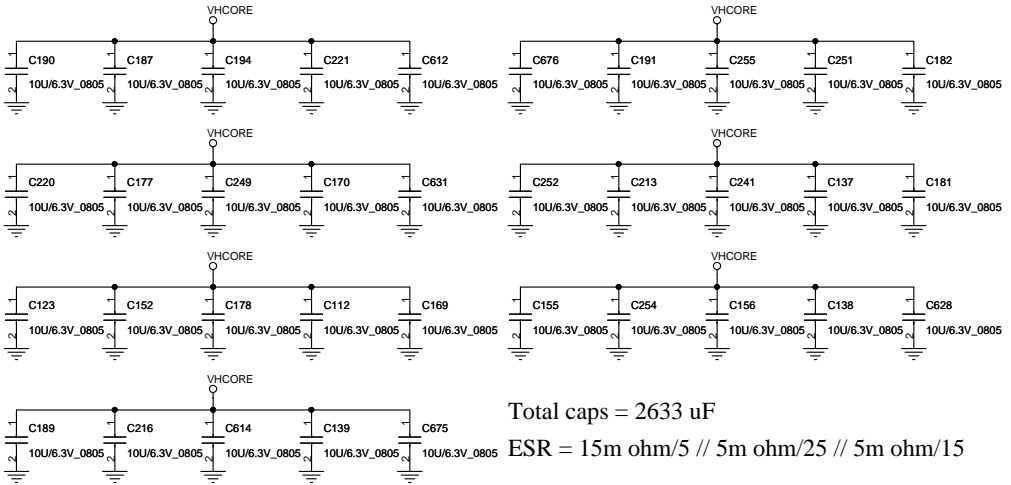
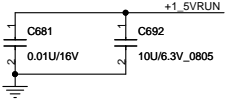
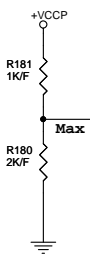
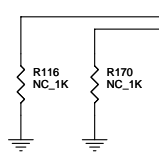
U30A



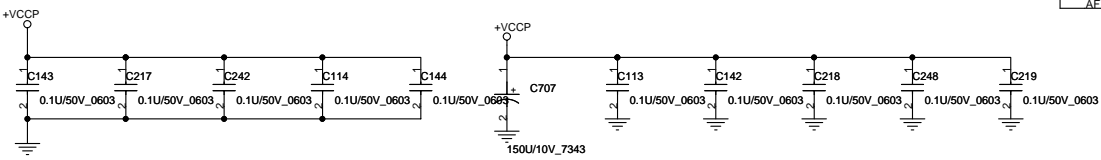
PM_THRMTRIP# should connect to ICH6-M and ALVISO without T-ing (No stub)



Place pull-down resistors within 0.5" of COMP pins

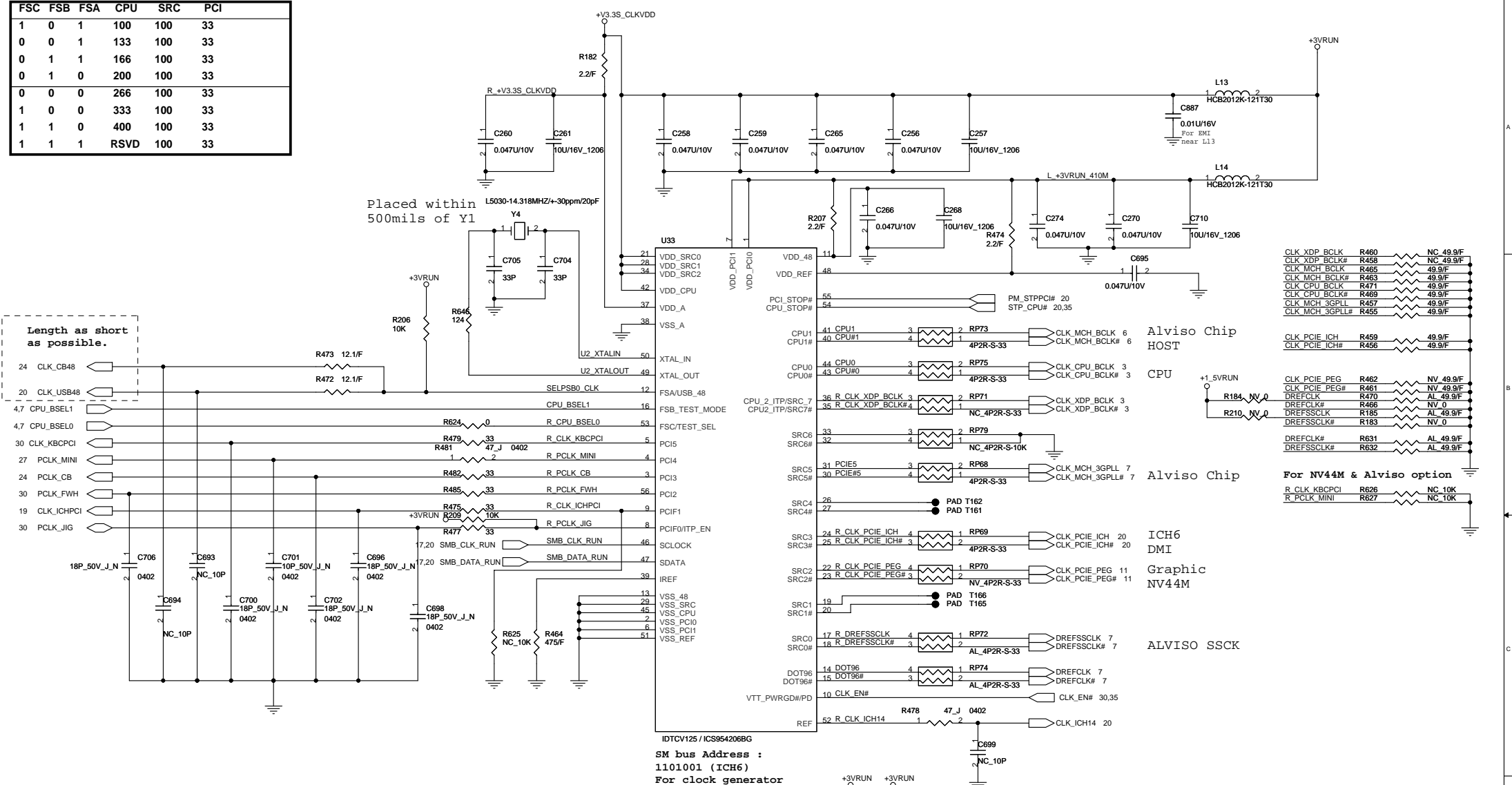


Total caps = 2633 uF
ESR = 15m ohm/5 // 5m ohm/25 // 5m ohm/15



U30B		U30C	
COMP0	P25	VSS00	A2
COMP1	P26	VSS01	A5
COMP2	AB2	VSS02	A8
COMP3	AB1	VSS03	A11
		VSS04	A14
		VSS05	A17
		VSS06	A20
		VSS07	A23
		VSS08	A26
		VSS09	B3
		VSS10	B6
		VSS11	B9
		VSS12	B12
		VSS13	B15
		VSS14	B18
		VSS15	B21
		VSS16	B24
		VSS17	C1
		VSS18	C4
		VSS19	C7
		VSS20	C10
		VSS21	C13
		VSS22	C16
		VSS23	C19
		VSS24	C22
		VSS25	C25
		VSS26	D2
		VSS27	D5
		VSS28	D8
		VSS29	D11
		VSS30	D14
		VSS31	D17
		VSS32	D20
		VSS33	D23
		VSS34	D26
		VSS35	E3
		VSS36	E6
		VSS37	E9
		VSS38	E12
		VSS39	E15
		VSS40	E18
		VSS41	E21
		VSS42	E24
		VSS43	E27
		VSS44	E30
		VSS45	E33
		VSS46	E36
		VSS47	E39
		VSS48	E42
		VSS49	E45
		VSS50	F1
		VSS51	F4
		VSS52	F7
		VSS53	F10
		VSS54	F13
		VSS55	F16
		VSS56	F19
		VSS57	F22
		VSS58	F25
		VSS59	F28
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		VSS64	F43
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		VSS66	F49
		VSS67	F52
		VSS68	F55
		VSS69	F58
		VSS70	F61
		VSS71	F64
		VSS72	F67
		VSS73	F70
		VSS74	F73
		VSS75	F76
		VSS76	F79
		VSS77	F82
		VSS78	F85
		VSS79	F88
		VSS80	F91
		VSS81	F94
		VSS82	F97
		VSS83	F100
		VSS84	G1
		VSS85	G4
		VSS86	G7
		VSS87	G10
		VSS88	G13
		VSS89	G16
		VSS90	G19
		VSS91	G22
		VSS92	G25
		VSS93	G28
		VSS94	G31
		VSS95	G34
		VSS96	G37
		VSS97	G40
		VSS98	G43
		VSS99	G46
		VSS00	G49
		VSS01	G52
		VSS02	G55
		VSS03	G58
		VSS04	G61
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		VSS13	G88
		VSS14	G91
		VSS15	G94
		VSS16	G97
		VSS17	G100
		VSS18	H1
		VSS19	H4
		VSS20	H7
		VSS21	H10
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		VSS23	H16
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		VSS50	H97
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		VSS52	I4
		VSS53	I7
		VSS54	I10
		VSS55	I13
		VSS56	I16
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		VSS49	K94
		VSS50	K97
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		VSS83	L97
		VSS84	M1
		VSS85	M4
		VSS86	M7
		VSS87	M10
		VSS88	M13
		VSS89	M16
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		VSS03	M58
		VSS04	M61
		VSS05	M64
		VSS06	M67
		VSS07	M70
		VSS08	M73
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		VSS11	M82
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		VSS14	M91
		VSS15	M94
		VSS16	M97
		VSS17	N1
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		VSS19	N7
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		VSS21	N13
		VSS22	N16
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		VSS26	N28
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		VSS28	N34
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		VSS38	N64
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		VSS40	N70
		VSS41	N73
		VSS42	N76
		VSS43	N79
		VSS44	N82
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		VSS47	N91
		VSS48	N94
		VSS49	N97
		VSS50	N100
		VSS51	O1
		VSS52	O4
		VSS53	O7
		VSS54	O10
		VSS55	O13
		VSS56	O16
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		VSS58	O22
		VSS59	O25
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		VSS61	O31
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		VSS10	P79
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		VSS16</	

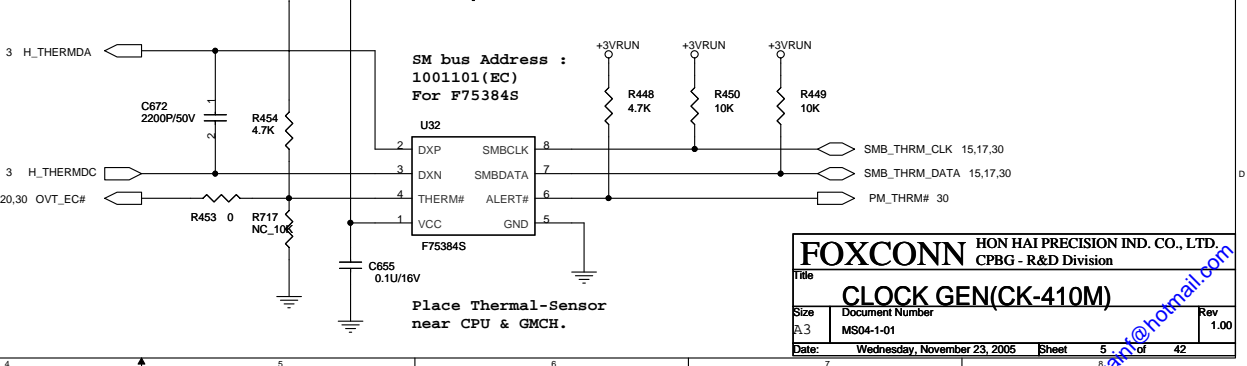
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33



Placed within 500mils of Y1

Length as short as possible.

ID7CV125 / ICS954206BG
SM bus Address :
1101001 (ICH6)
For clock generator

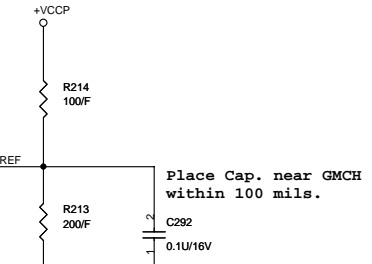
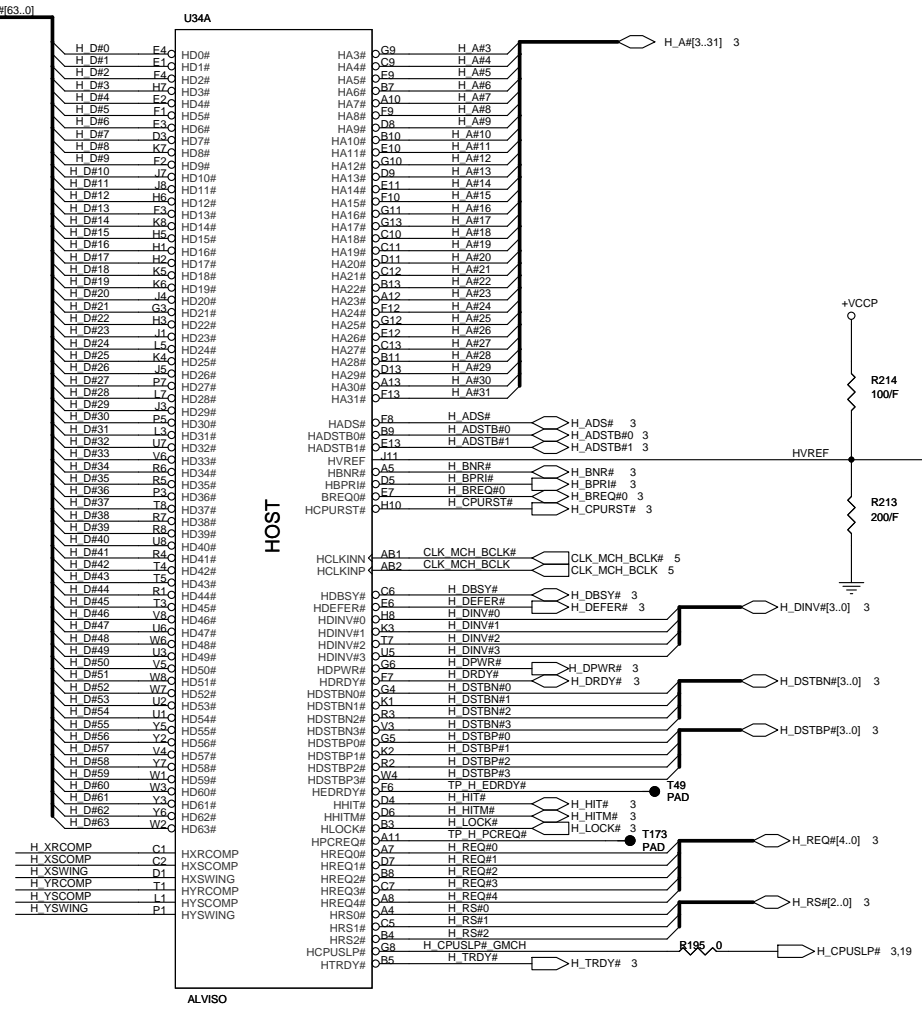
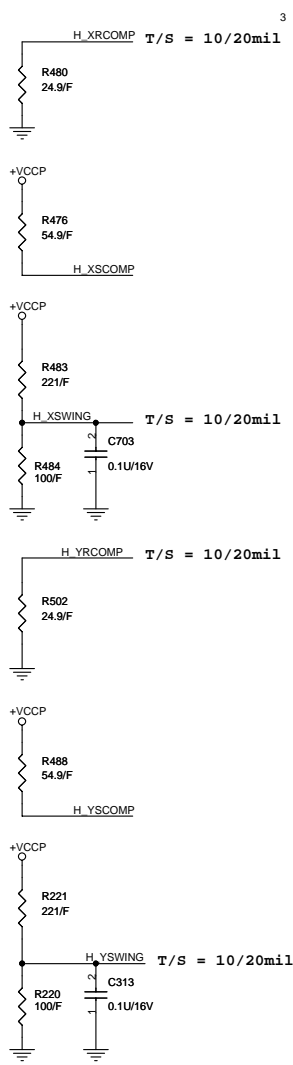


SM bus Address :
1001101 (EC)
For F75384S

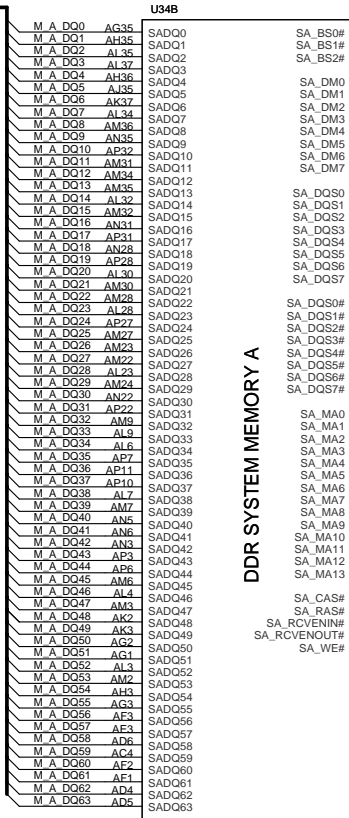
Place Thermal-Sensor near CPU & GMCH.

CLK_XDP_BCLK	R460	NC	49.9F
CLK_XDP_BCLK#	R458	NC	49.9F
CLK_MCH_BCLK	R465		49.9F
CLK_MCH_BCLK#	R463		49.9F
CLK_CPU_BCLK	R471		49.9F
CLK_CPU_BCLK#	R469		49.9F
CLK_MCH_3GPLL	R457		49.9F
CLK_MCH_3GPLL#	R455		49.9F
CLK_PCIE_ICH	R459		49.9F
CLK_PCIE_ICH#	R456		49.9F
CLK_PCIE_PEG	R462	NV	49.9F
CLK_PCIE_PEG#	R461	NV	49.9F
DREFCLK	R470	AL	49.9F
DREFCLK#	R466		NV 0
DREFSSCLK	R185	AL	49.9F
DREFSSCLK#	R183		NV 0
DREFCLK#	R631		AL 49.9F
DREFSSCLK#	R632		AL 49.9F

For NV44M & Alviso option
 R_CLK_KBCPCI R626 NC 10K
 R_PCLK_MINI R627 NC 10K



17 M_A_DQ[63..0]

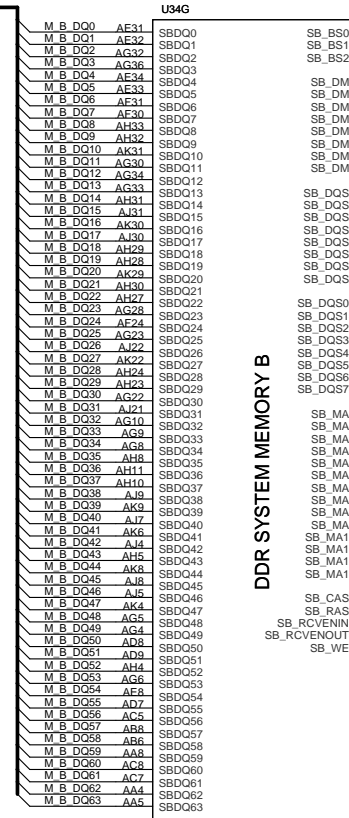


U34B

DDR SYSTEM MEMORY A

ALVISO

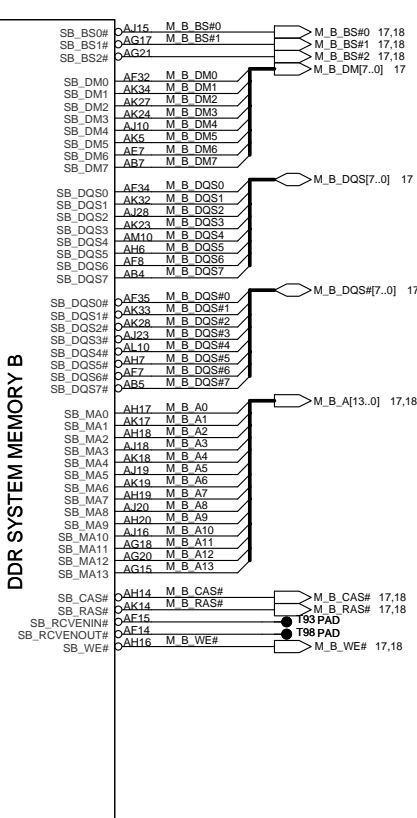
17 M_B_DQ[63..0]

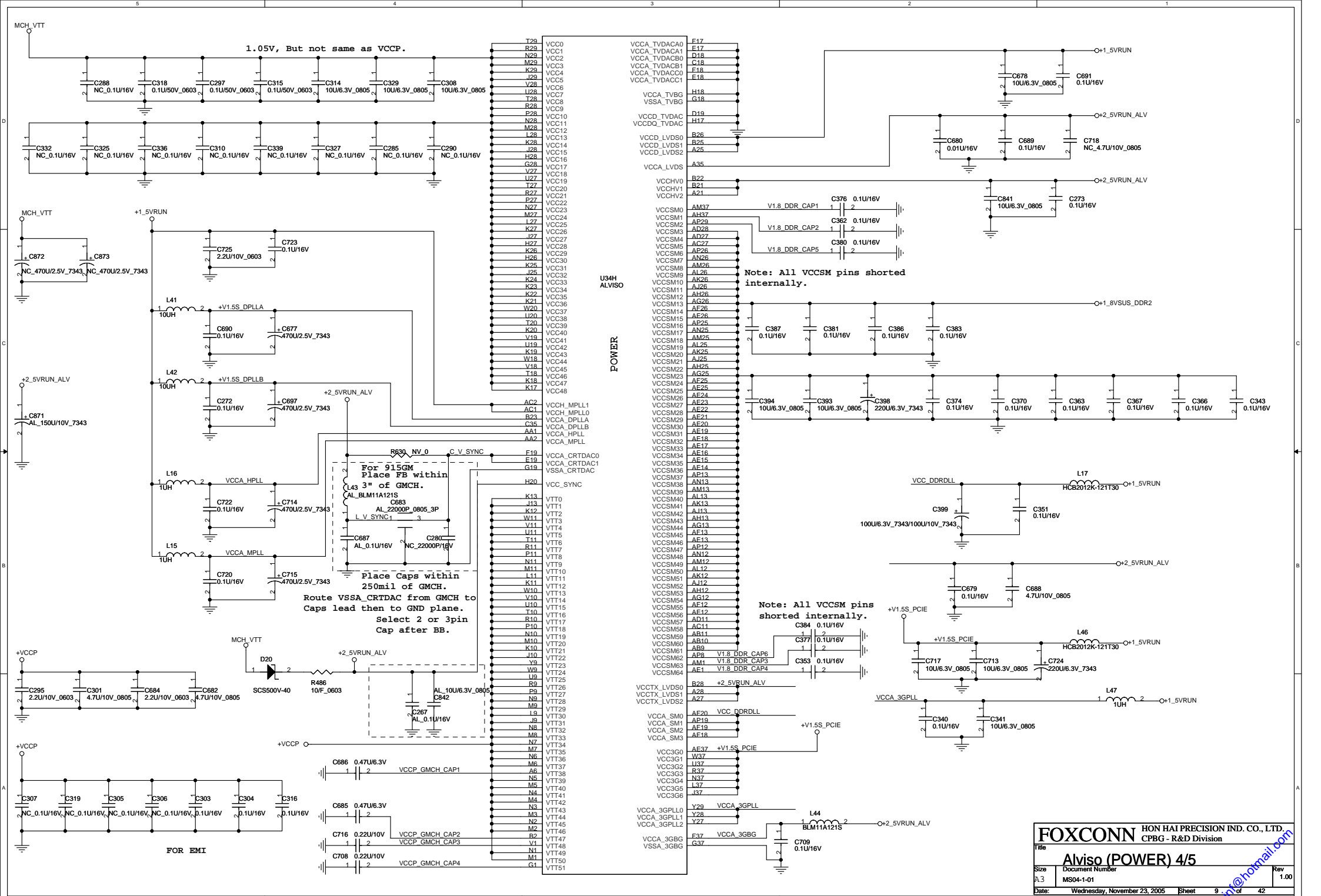


U34G

DDR SYSTEM MEMORY B

ALVISO





POWER

For 0.15GM Place FB within 3" of GMCH.

Place Caps within 250mil of GMCH.

Route VSSA_CRTDAC from GMCH to Caps lead then to GND plane.

Select 2 or 3pin Cap after BB.

Note: All VCCSM pins shorted internally.

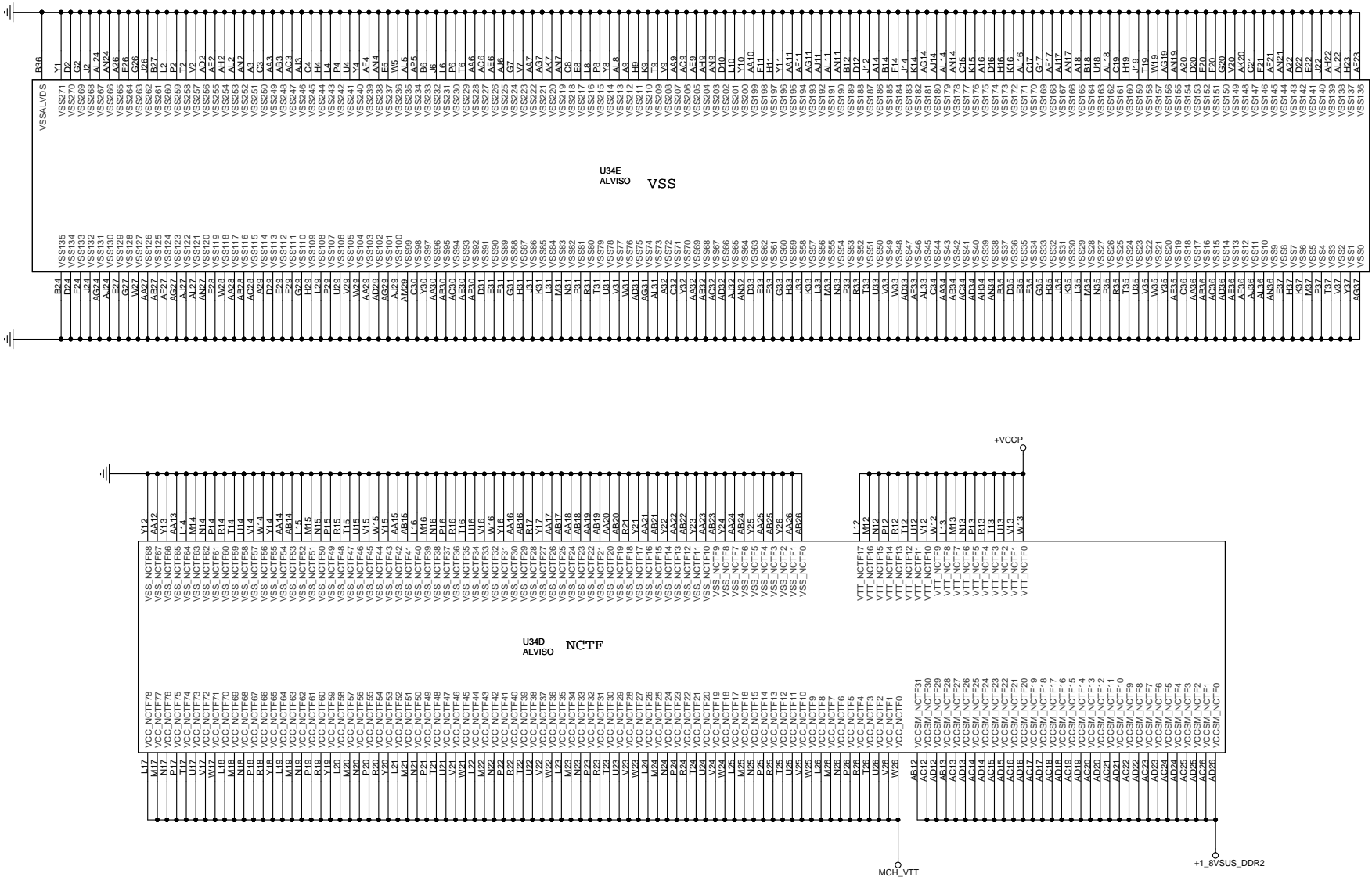
Note: All VCCSM pins shorted internally.

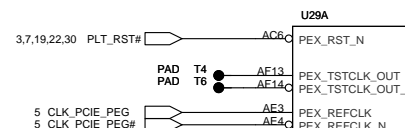
FOXCONN HON HAI PRECISION IND. CO., LTD.
CPBG - R&D Division

Title: **Alviso (POWER) 4/5**

Size: A3	Document Number: MS04-1-01	Rev: 1.00
Date: Wednesday, November 23, 2005	Sheet: 9	of 42

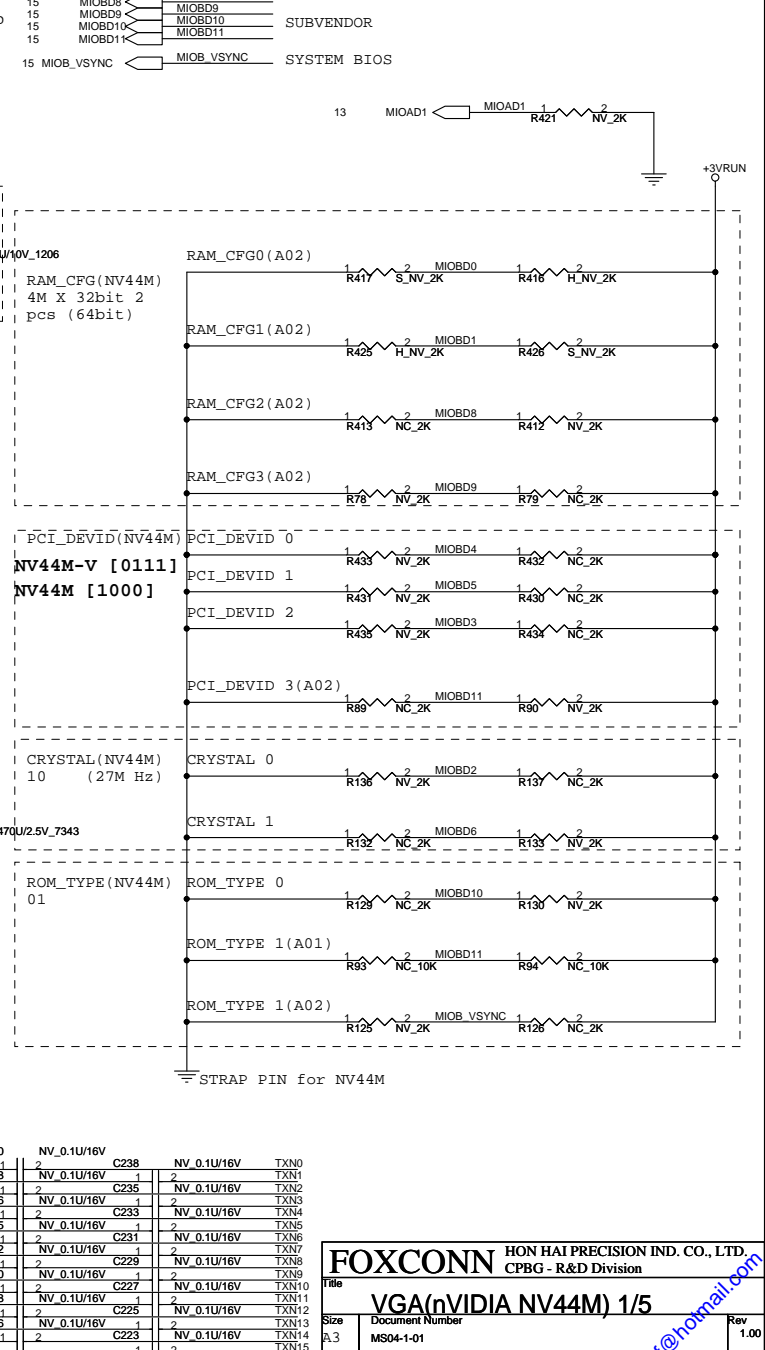
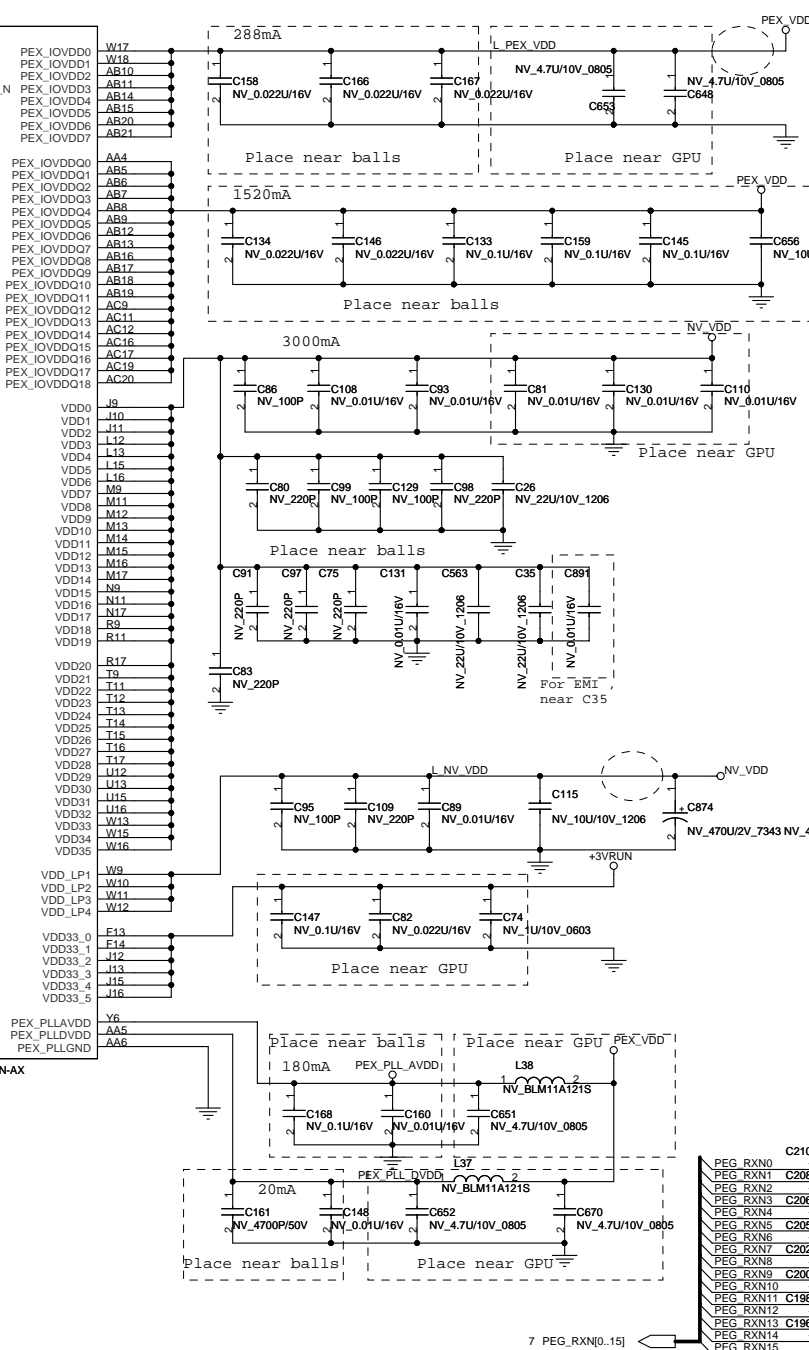
hexant@hotmail.com





TXP0	AD5	PEX_TX0
TXN0	AD6	PEX_TX0_N
TXP1	AE6	PEX_TX1
TXN1	AE7	PEX_TX1_N
TXP2	AD7	PEX_TX2
TXN2	AC7	PEX_TX2_N
TXP3	AE9	PEX_TX3
TXN3	AE10	PEX_TX3_N
TXP4	AD10	PEX_TX4
TXN4	AC10	PEX_TX4_N
TXP5	AE12	PEX_TX5
TXN5	AE13	PEX_TX5_N
TXP6	AD13	PEX_TX6
TXN6	AC13	PEX_TX6_N
TXP7	AE15	PEX_TX7
TXN7	AD15	PEX_TX7_N
TXP8	AE15	PEX_TX8
TXN8	AE16	PEX_TX8_N
TXP9	AC16	PEX_TX9
TXN9	AD18	PEX_TX9_N
TXP10	AE18	PEX_TX10
TXN10	AE19	PEX_TX10_N
TXP11	AC21	PEX_TX11
TXN11	AD21	PEX_TX11_N
TXP12	AE21	PEX_TX12
TXN12	AE22	PEX_TX12_N
TXP13	AD22	PEX_TX13
TXN13	AD23	PEX_TX13_N
TXP14	AE24	PEX_TX14
TXN14	AE25	PEX_TX14_N
TXP15	AE24	PEX_TX15
TXN15	AD24	PEX_TX15_N

PEG_TXP_C0	AF1	PEX_RX0
PEG_TXN_C0	AG2	PEX_RX0_N
PEG_TXP_C1	AG3	PEX_RX1
PEG_TXN_C1	AG4	PEX_RX1_N
PEG_TXP_C2	AF4	PEX_RX2
PEG_TXN_C2	AF5	PEX_RX2_N
PEG_TXP_C3	AG6	PEX_RX3
PEG_TXN_C3	AG7	PEX_RX3_N
PEG_TXP_C4	AF7	PEX_RX4
PEG_TXN_C4	AF8	PEX_RX4_N
PEG_TXP_C5	AG9	PEX_RX5
PEG_TXN_C5	AG10	PEX_RX5_N
PEG_TXP_C6	AF10	PEX_RX6
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PEG_TXN_C12	AG22	PEX_RX12_N
PEG_TXP_C13	AF22	PEX_RX13
PEG_TXN_C13	AG23	PEX_RX13_N
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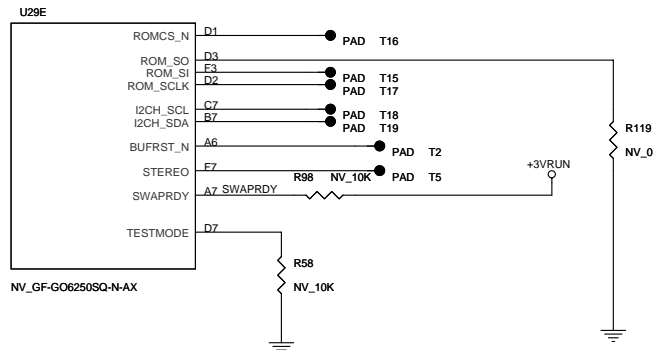
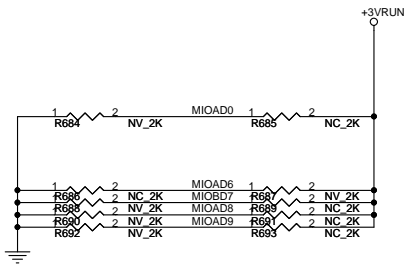
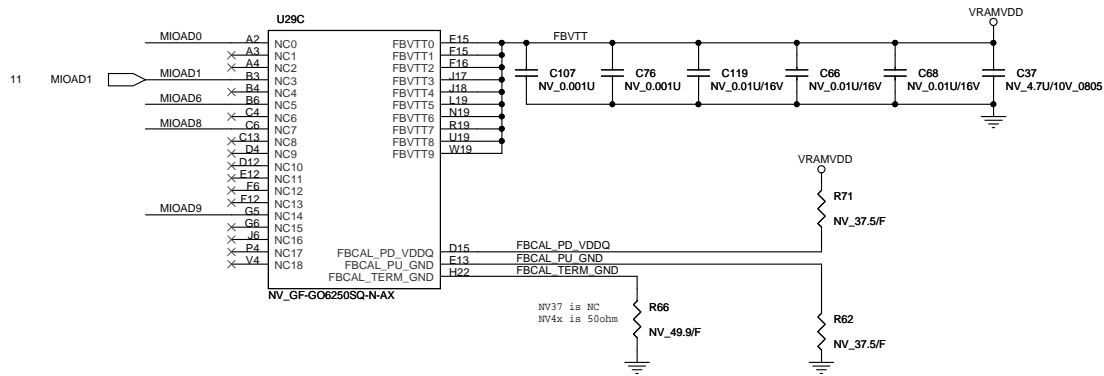


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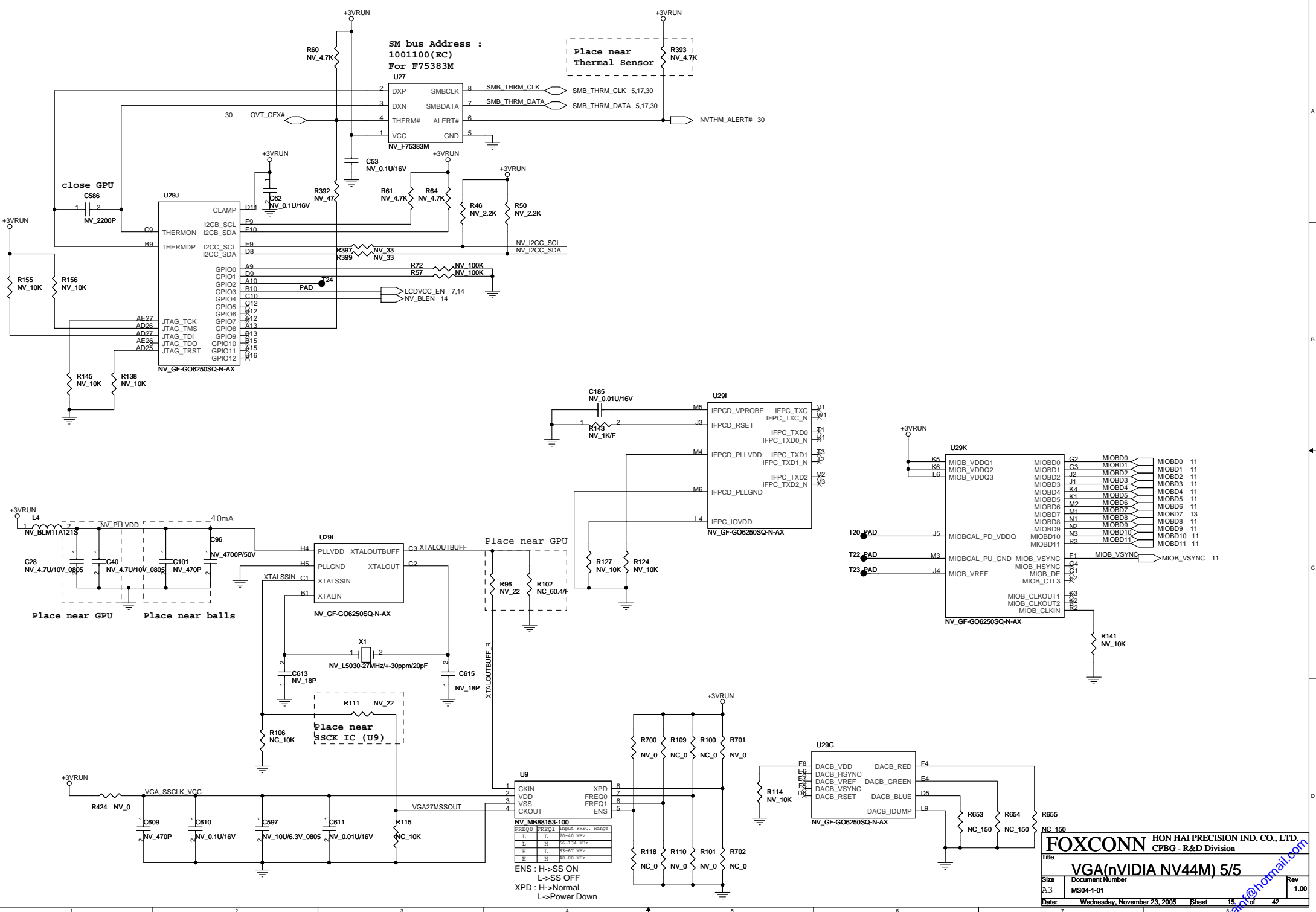
VGA(nVIDIA NV44M) 1/5

File: MS04-1-01
Size: A.3
Date: Wednesday, November 23, 2005

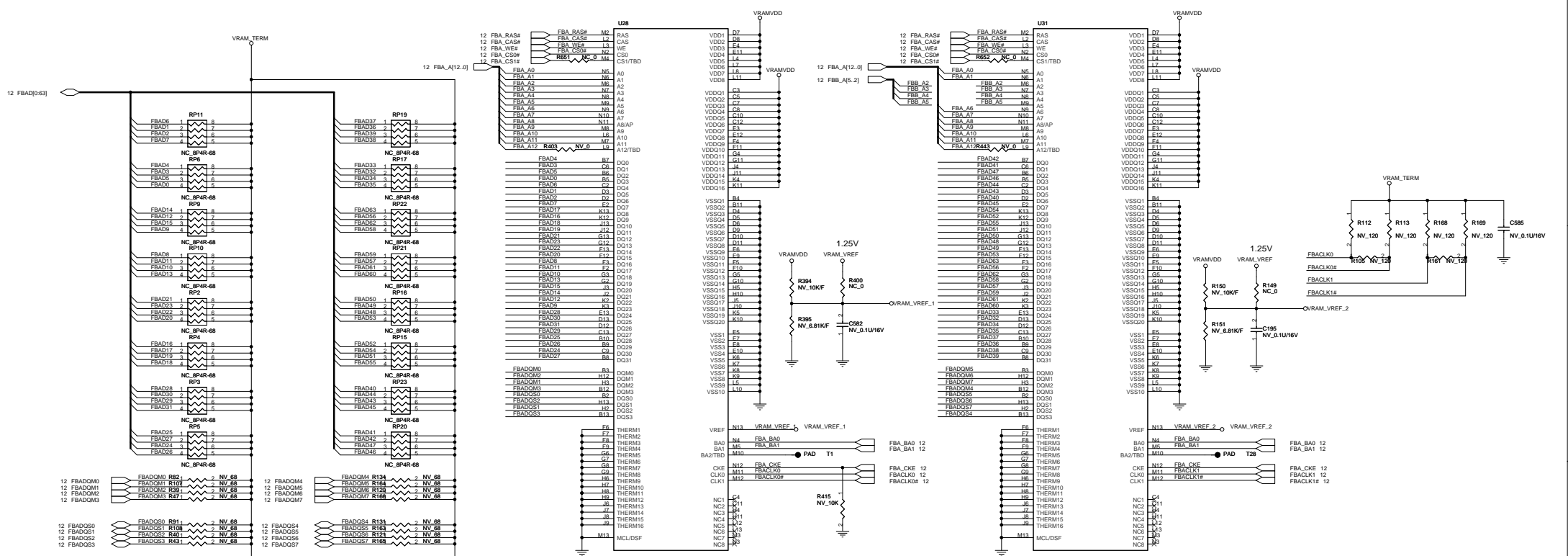
Document Number: MS04-1-01
Rev: 1.00
Sheet: 11. of 42



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hexan@hotmail.com

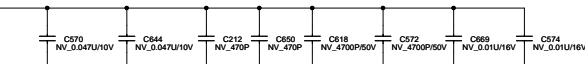


Decoupling for right MEMORY

Place around the MEM



Place under the MEM

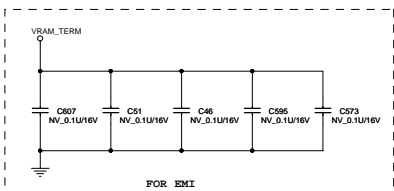


Decoupling for left MEMORY

Place around the MEM



Place under the MEM

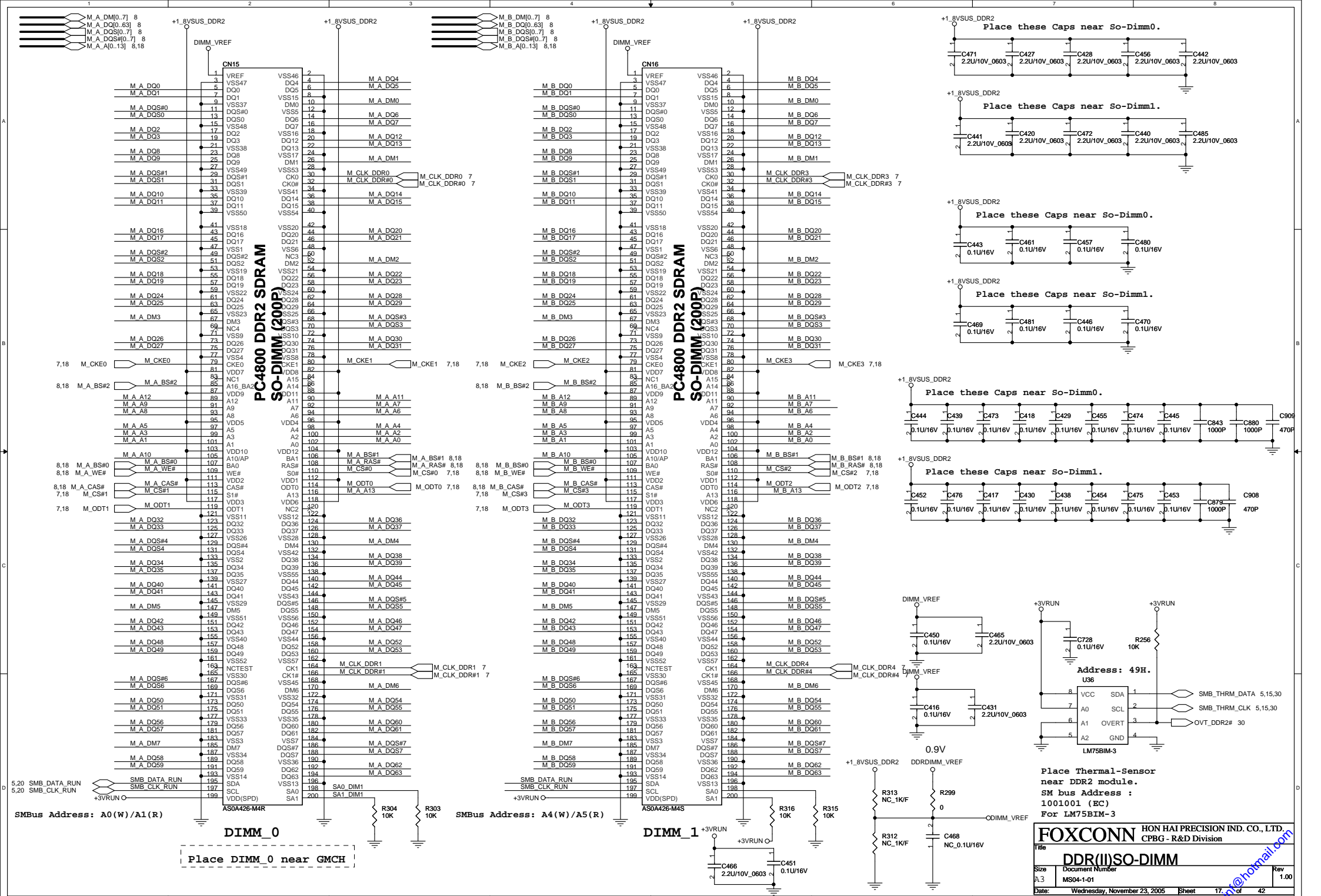


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File: **NV44M(DDR F A B 1)**

Doc: MS04-1-01 Rev 1.00

Date: Wednesday, November 23, 2005 Sheet 16 of 42



PC-4800 DDR2 SDRAM SO-DIMM (200P)

PC-4800 DDR2 SDRAM SO-DIMM (200P)

SMBus Address: A0(W)/A1(R)

SMBus Address: A4(W)/A5(R)

Address: 49H.

Place Thermal-Sensor near DDR2 module.
SM bus Address : 1001001 (EC)
For LM75BIM-3

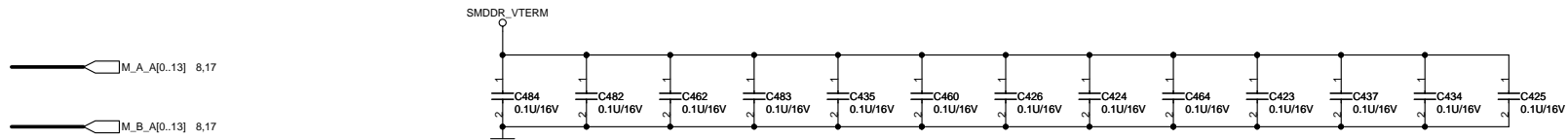
Place DIMM_0 near GMCH

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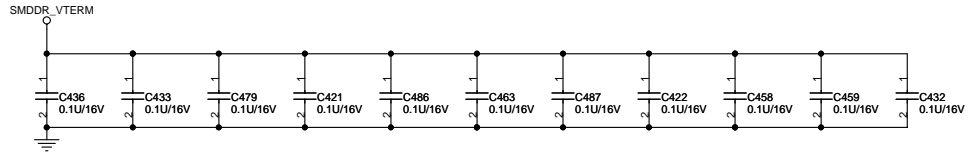
DDR(II)SO-DIMM

Size: A3
Document Number: MS04-1-01
Date: Wednesday, November 23, 2005
Sheet: 17 of 42

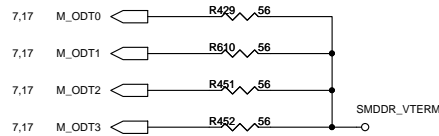
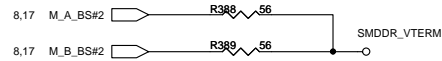
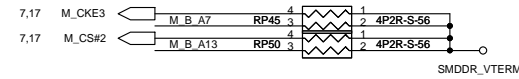
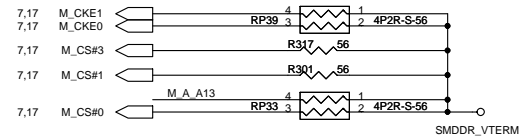
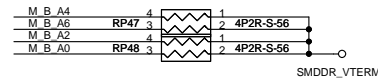
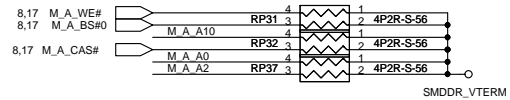
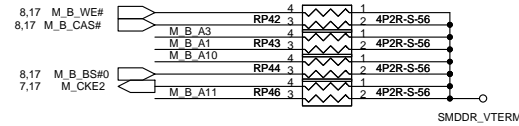
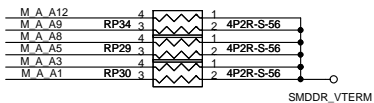
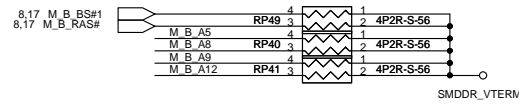
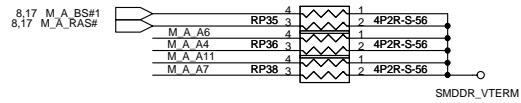
Rev: 1.00

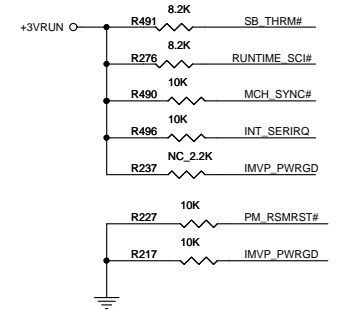
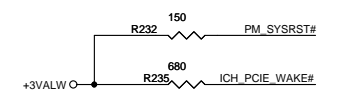
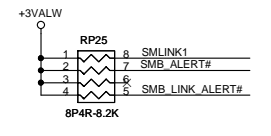
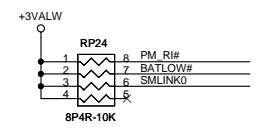
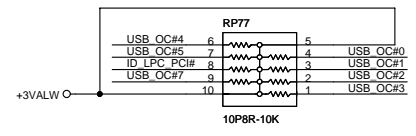
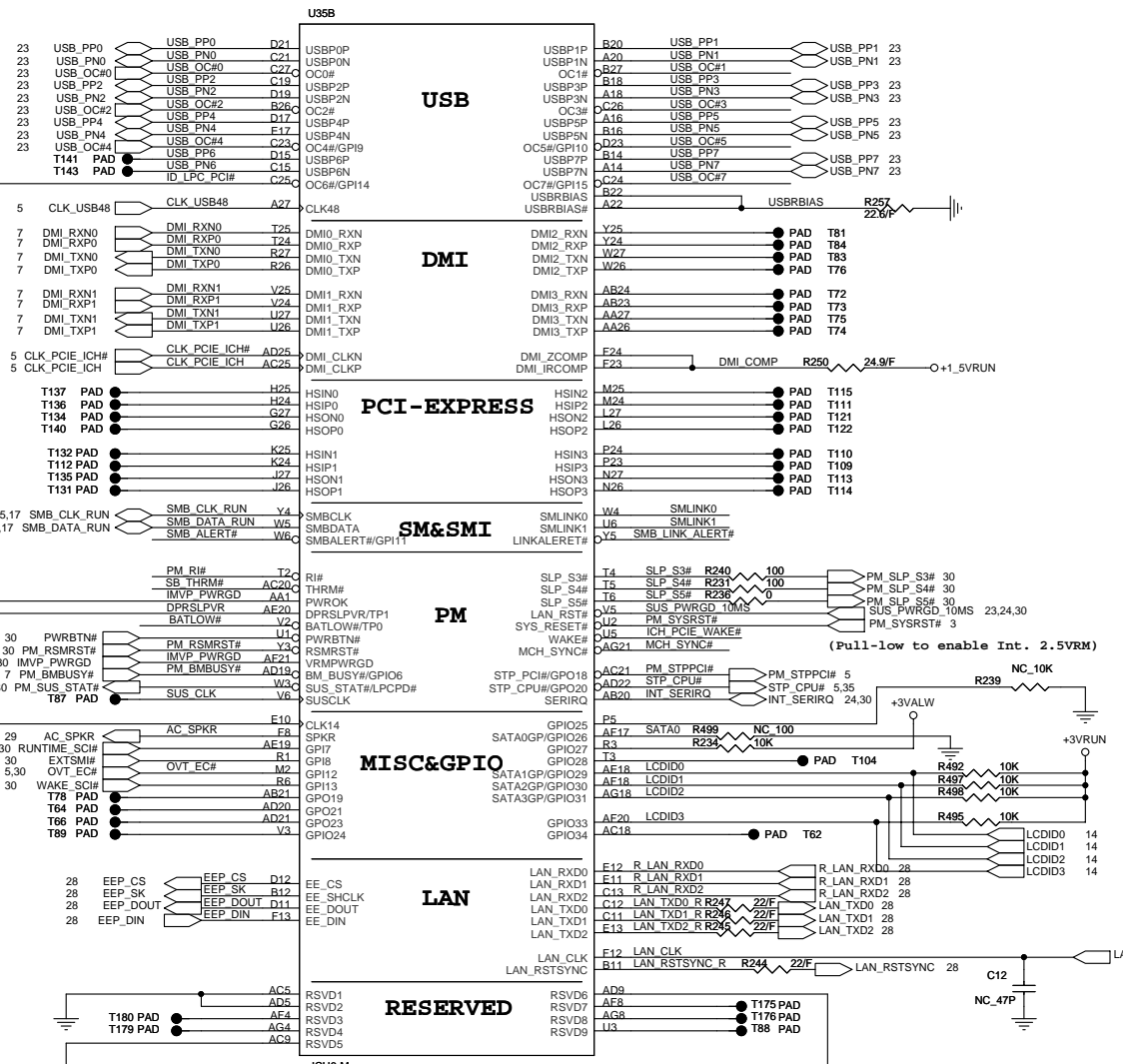
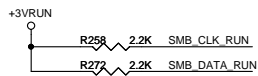


Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

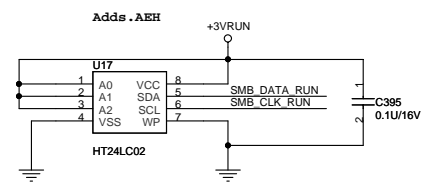
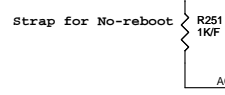
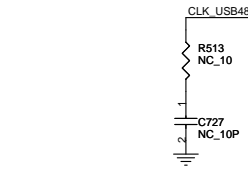
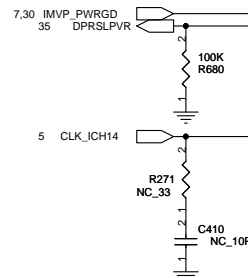


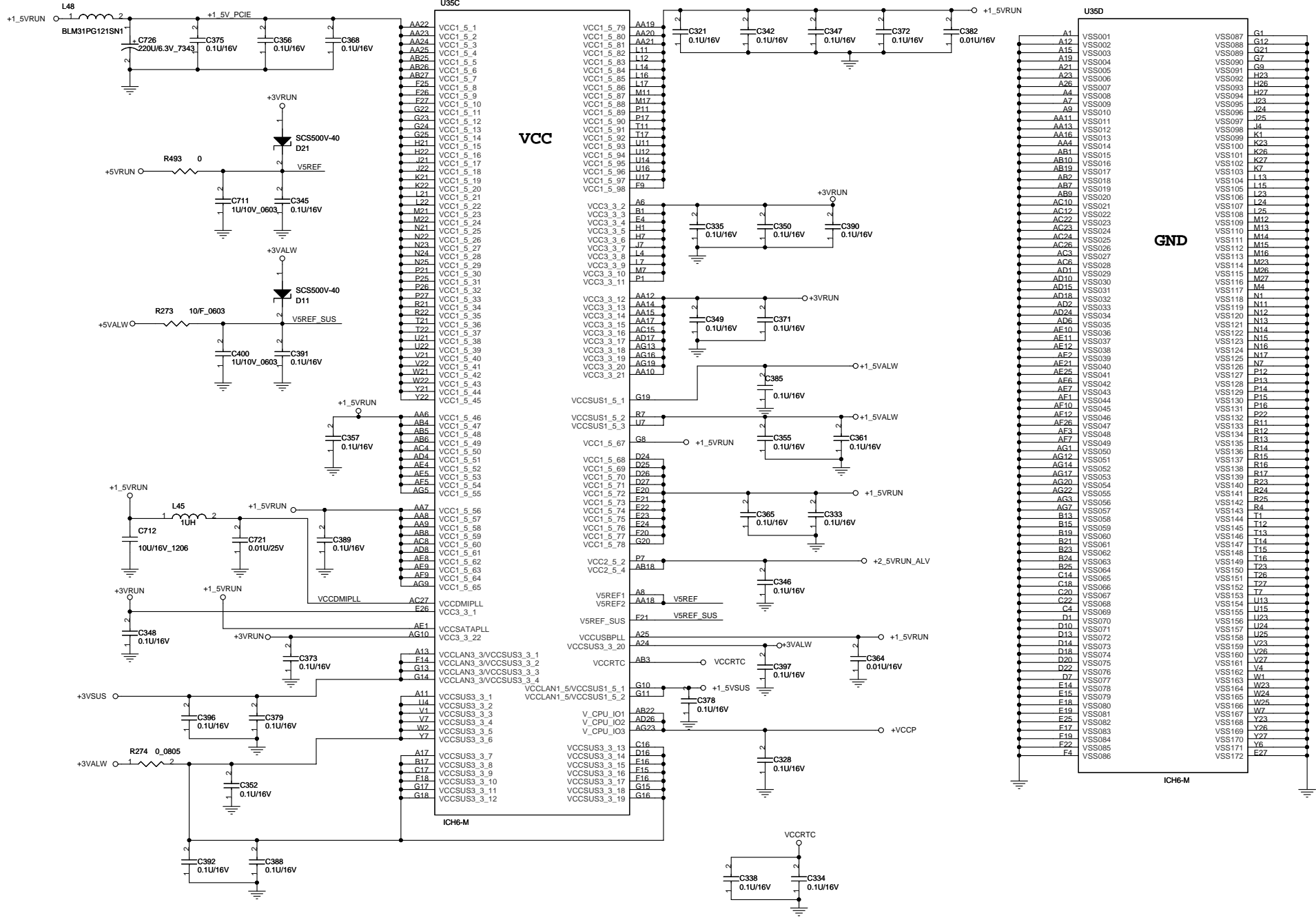
Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.



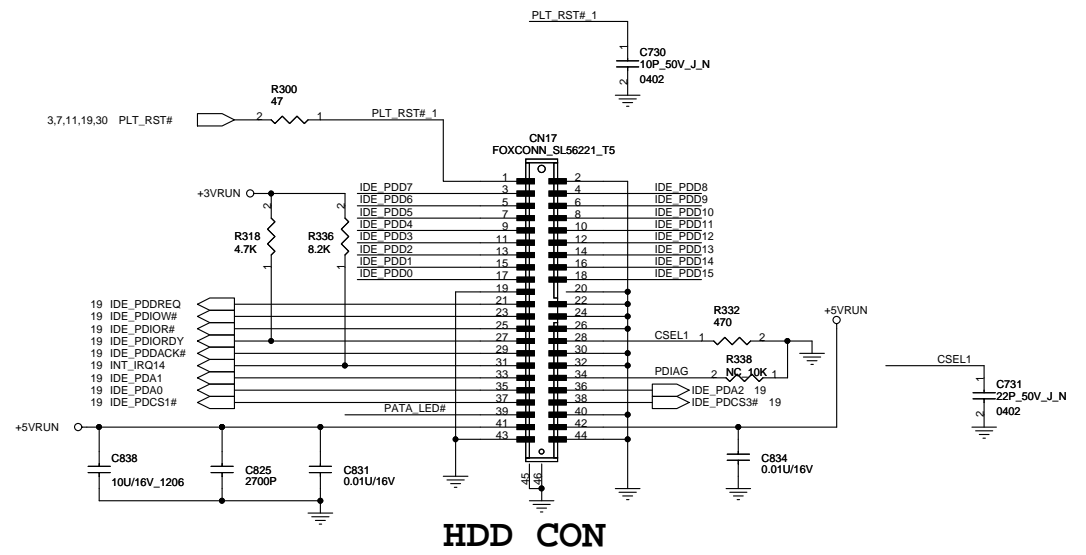


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 80 Port I/F:
 H: LCP bus
 L: PCI bus

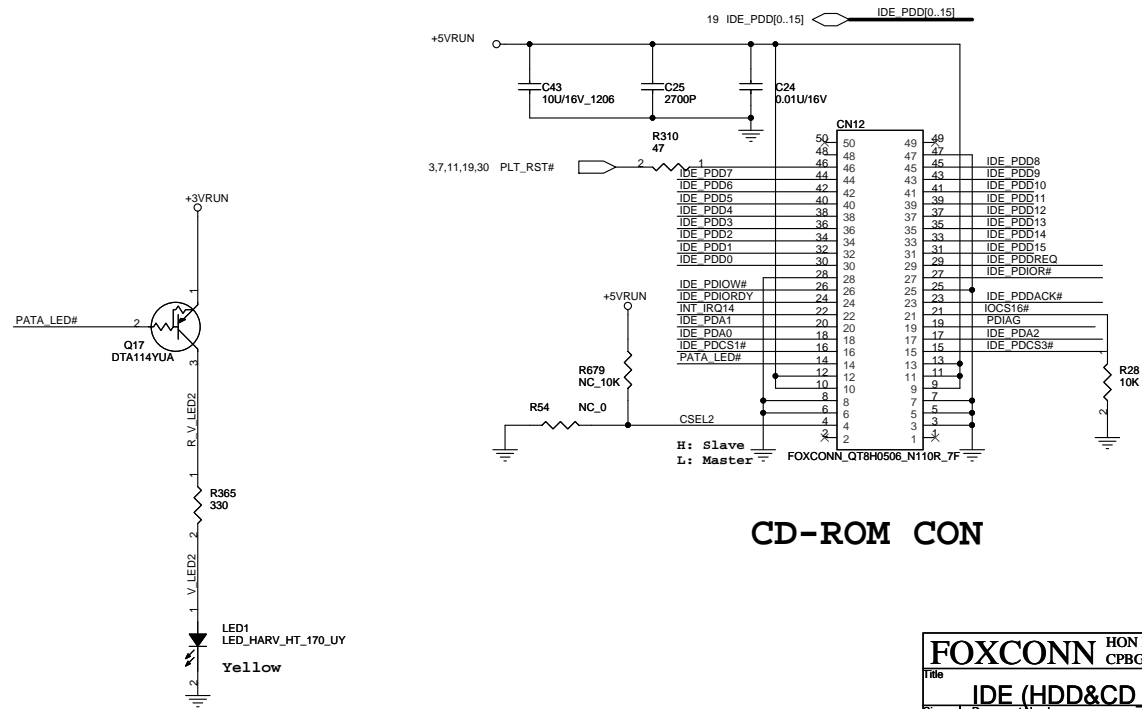




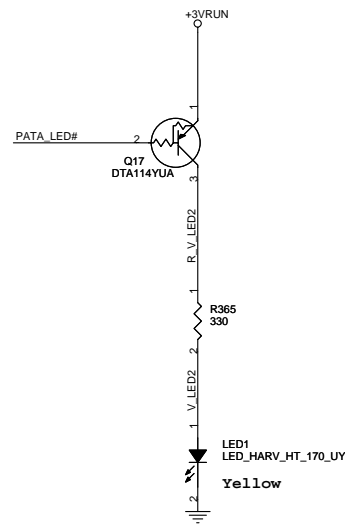
hexant@hotmail.com

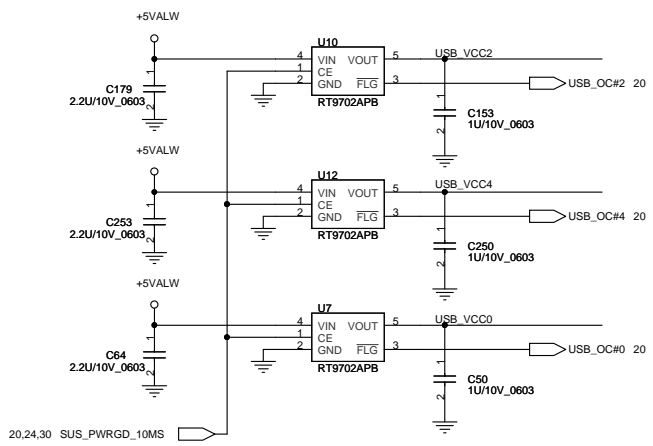


HDD CON

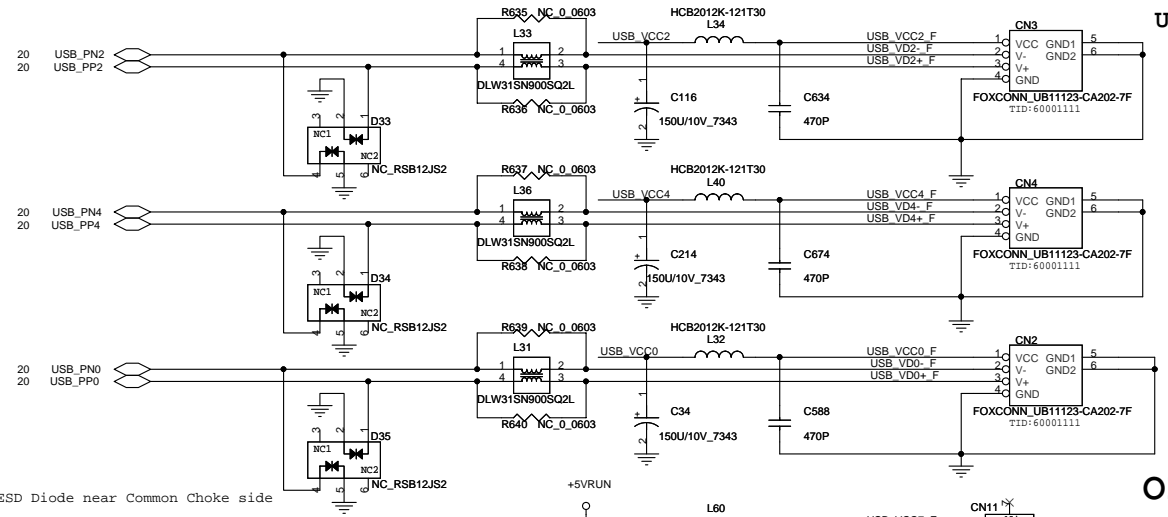


CD-ROM CON

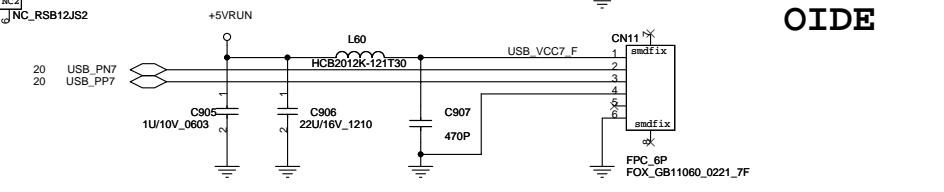




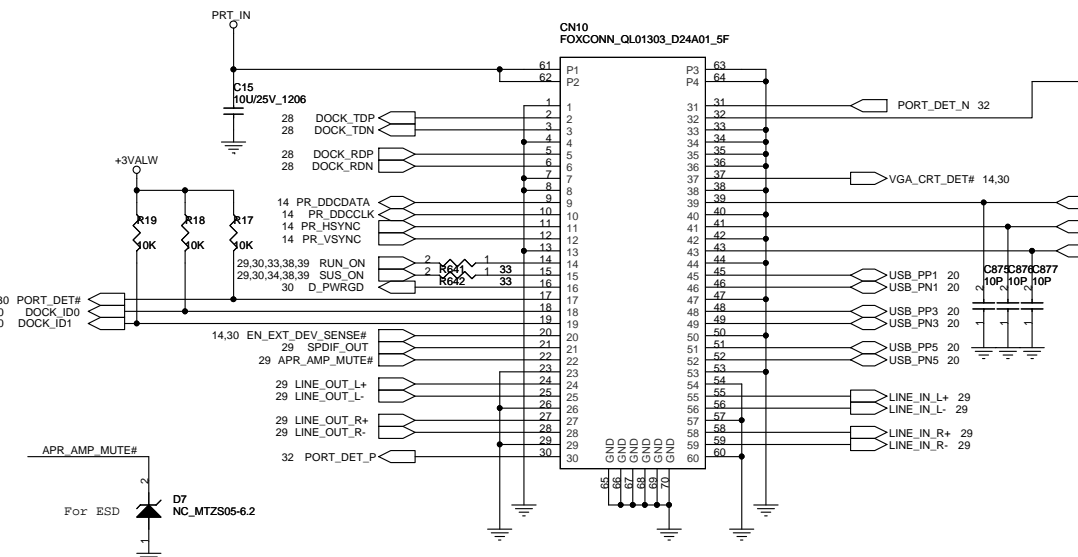
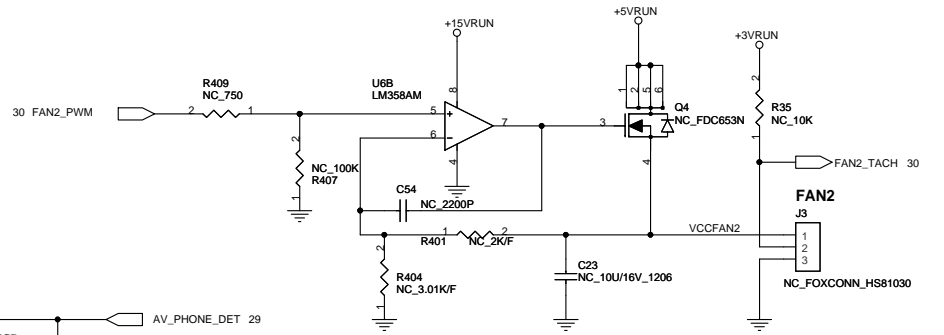
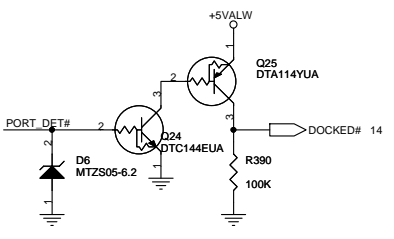
Place ESD Diode near Common Choke side



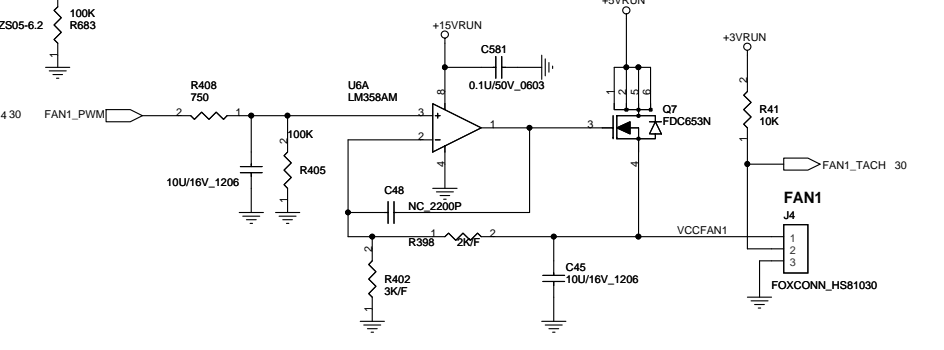
USB2.0 X 3



OIDE

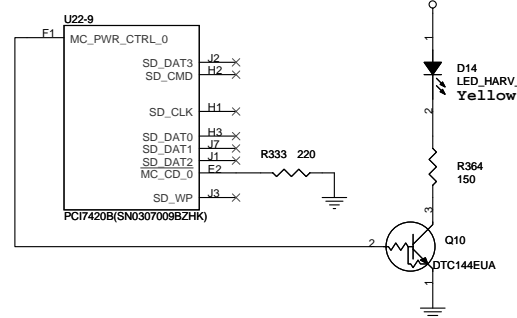
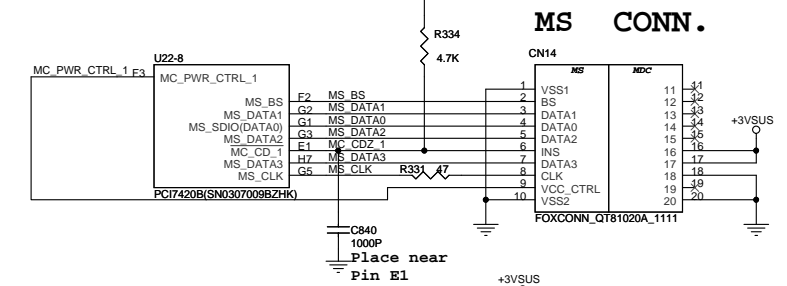
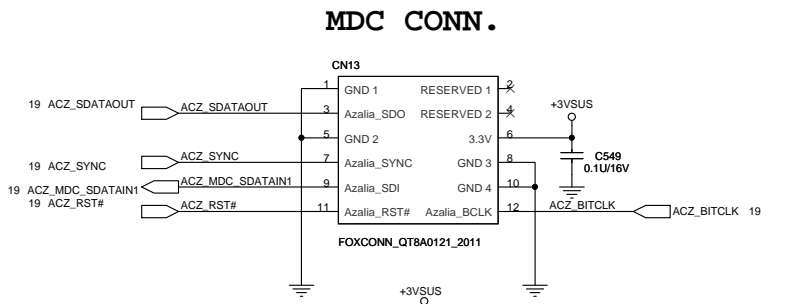
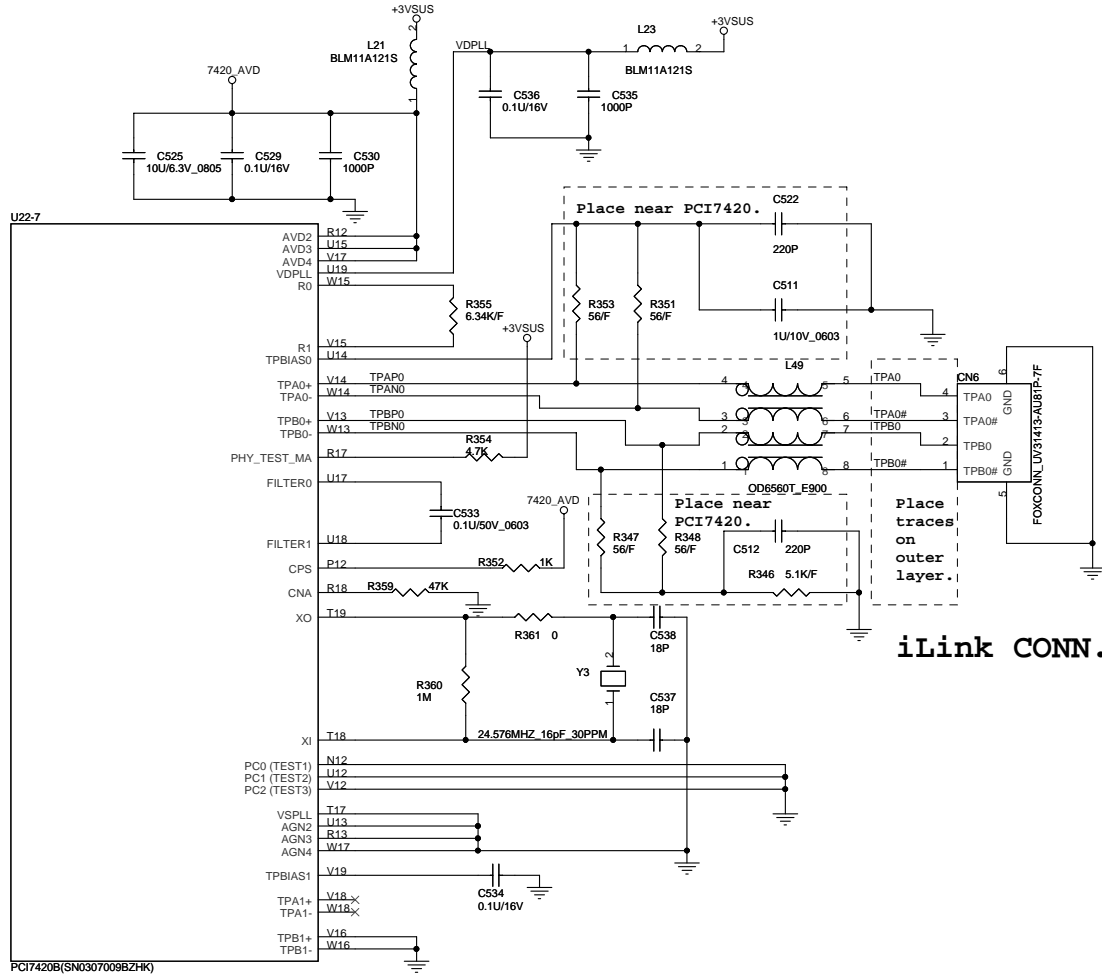


Replicator Port

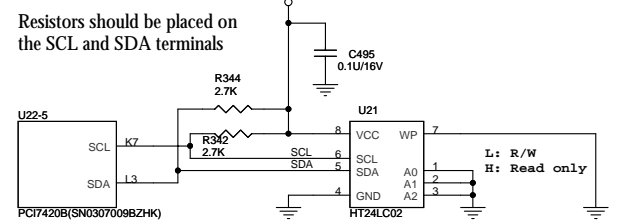
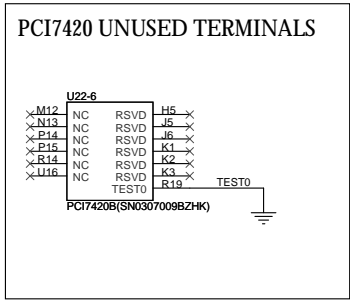
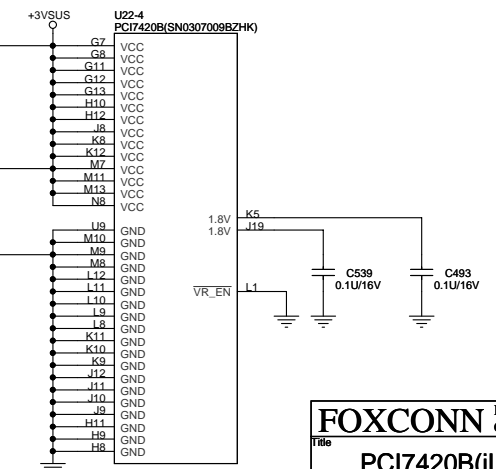


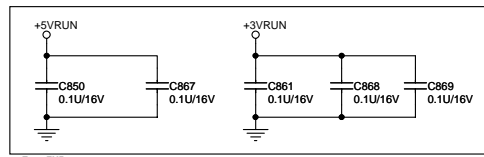
FAN

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CPBG - R&D Division			
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Size: A3	Document Number: MS04-1-01	Rev: 1.00	
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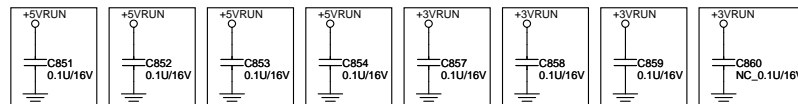


PCI7420 Power Terminals





For EMI .



Near RP51 ,
for EMI .

Near R607 ,
for EMI .

Near Q7 ,
for EMI .

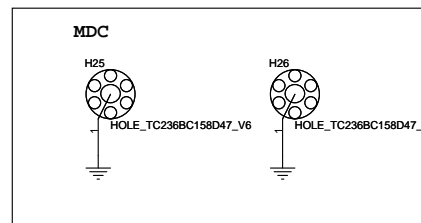
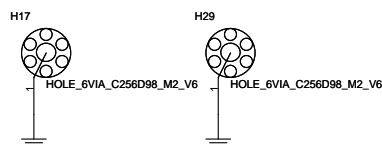
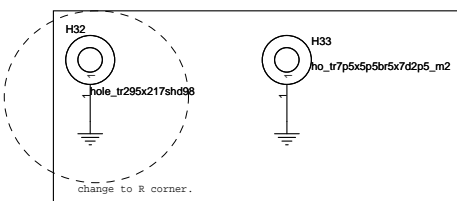
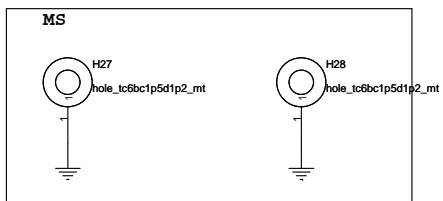
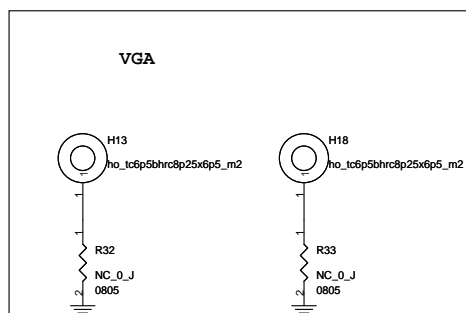
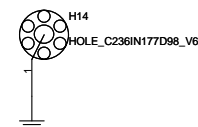
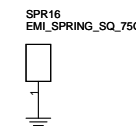
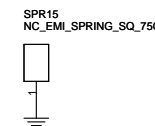
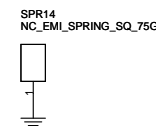
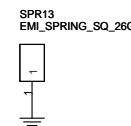
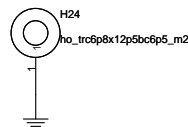
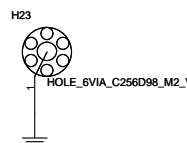
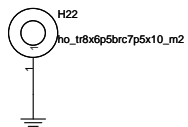
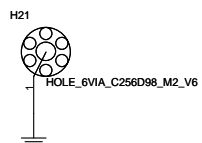
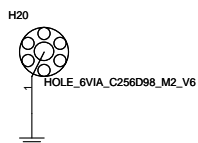
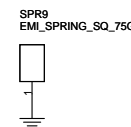
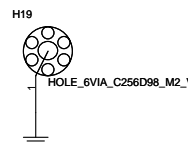
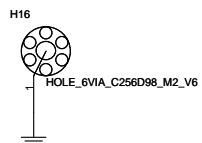
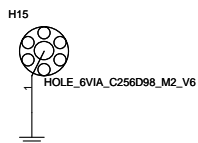
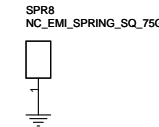
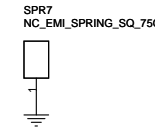
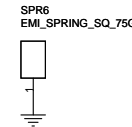
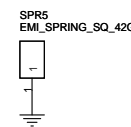
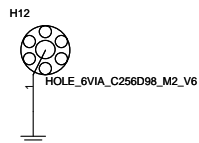
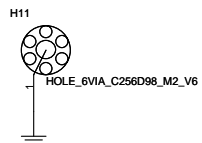
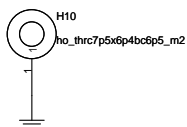
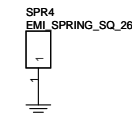
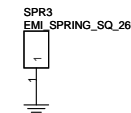
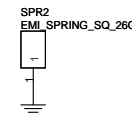
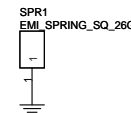
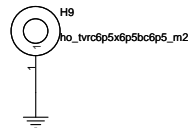
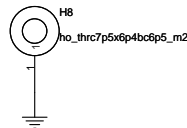
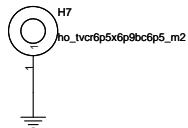
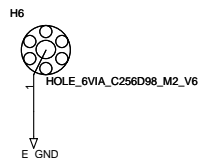
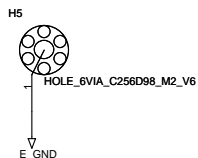
Near Q4 ,
for EMI .

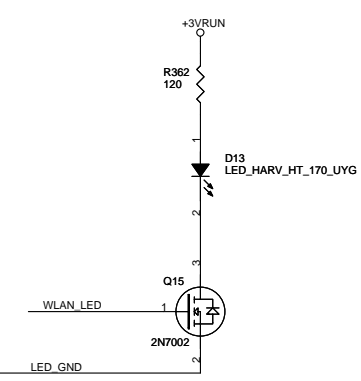
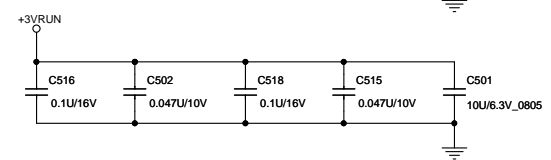
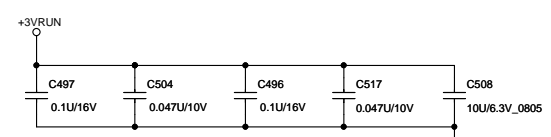
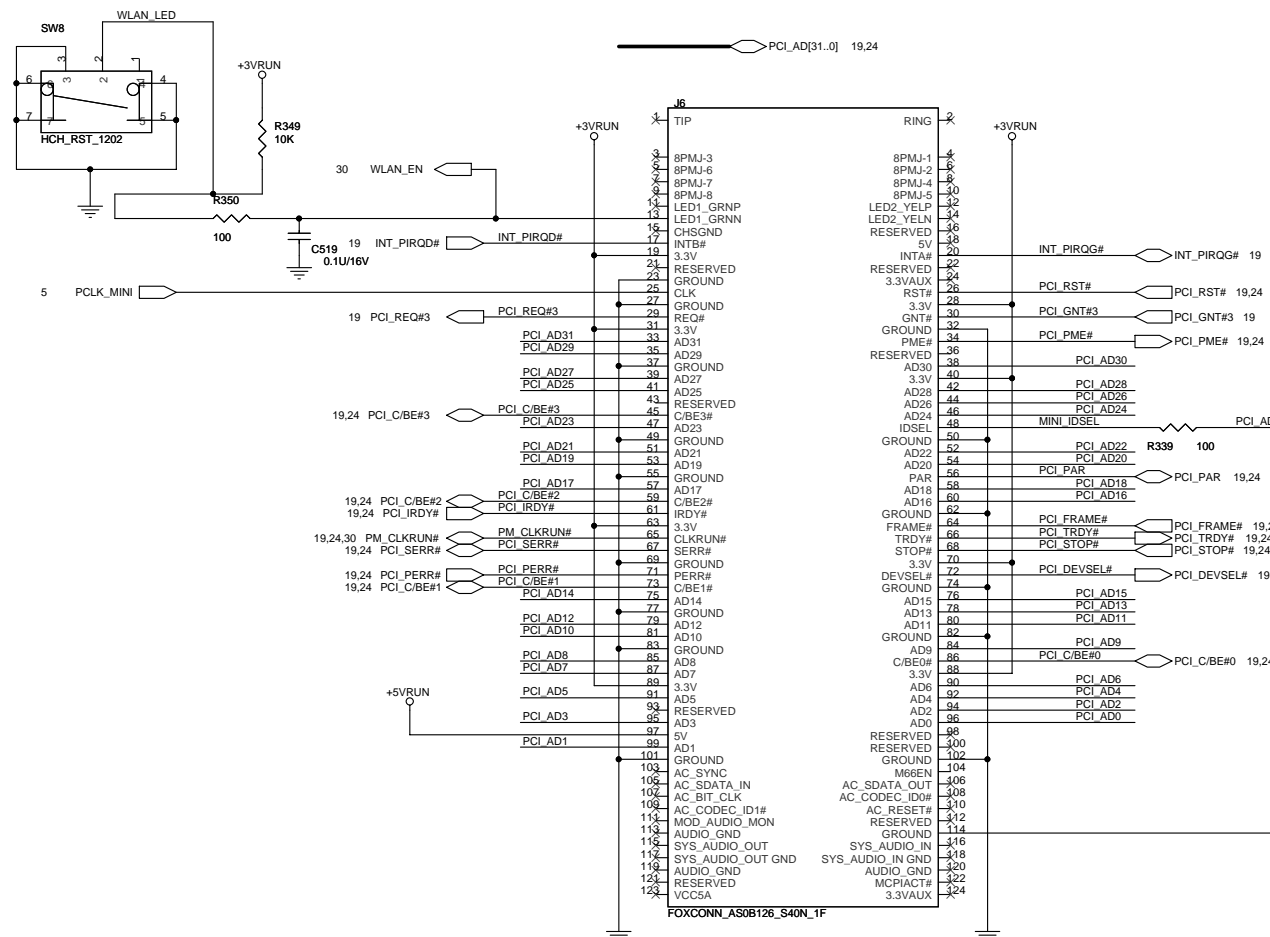
Near U37 ,
for EMI .

Near Q3 ,
for EMI .

Near Q4 ,
for EMI .

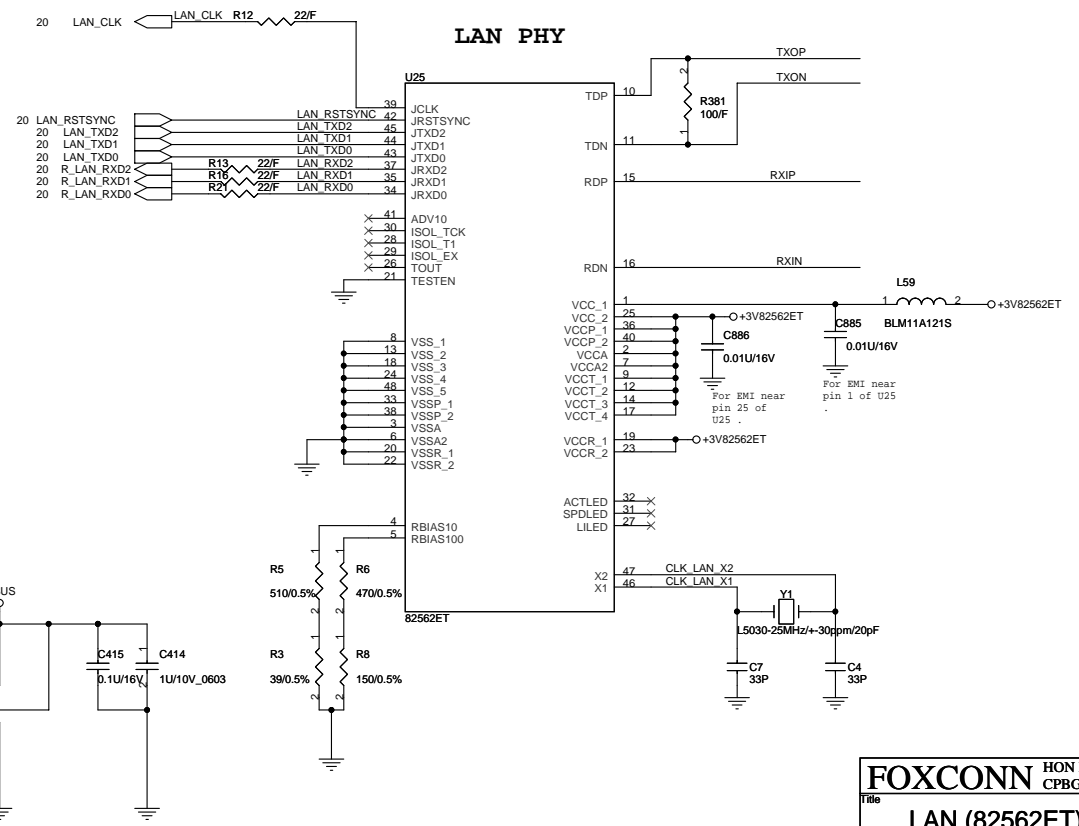
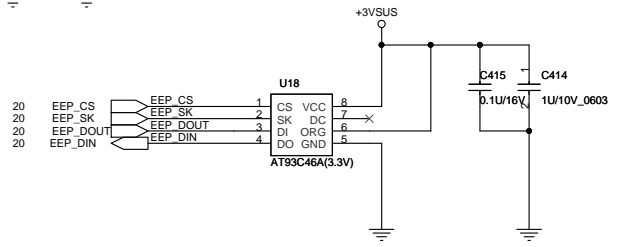
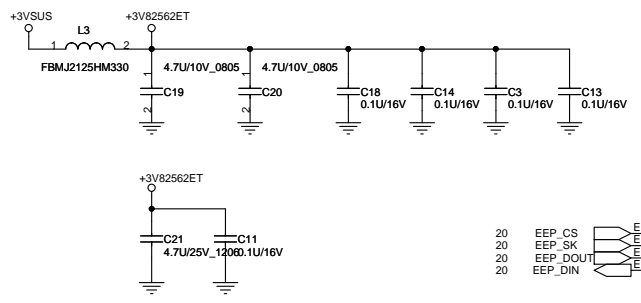
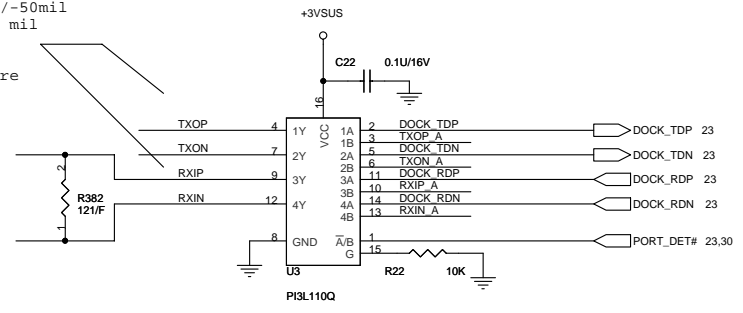
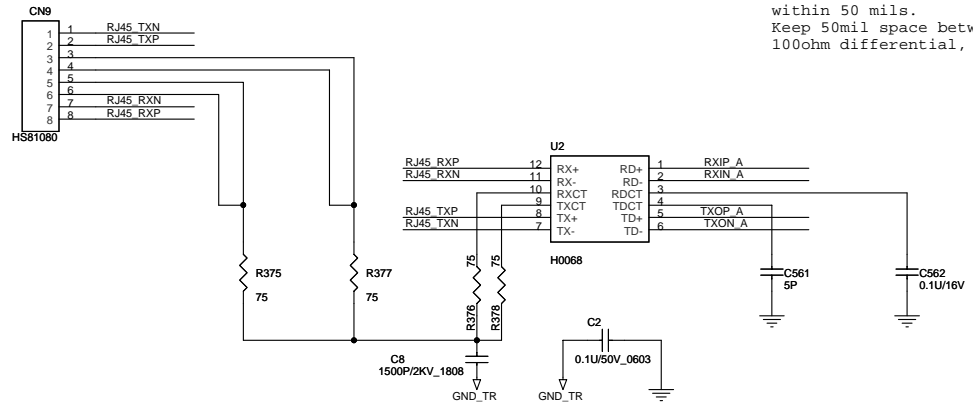
Near D8 ,
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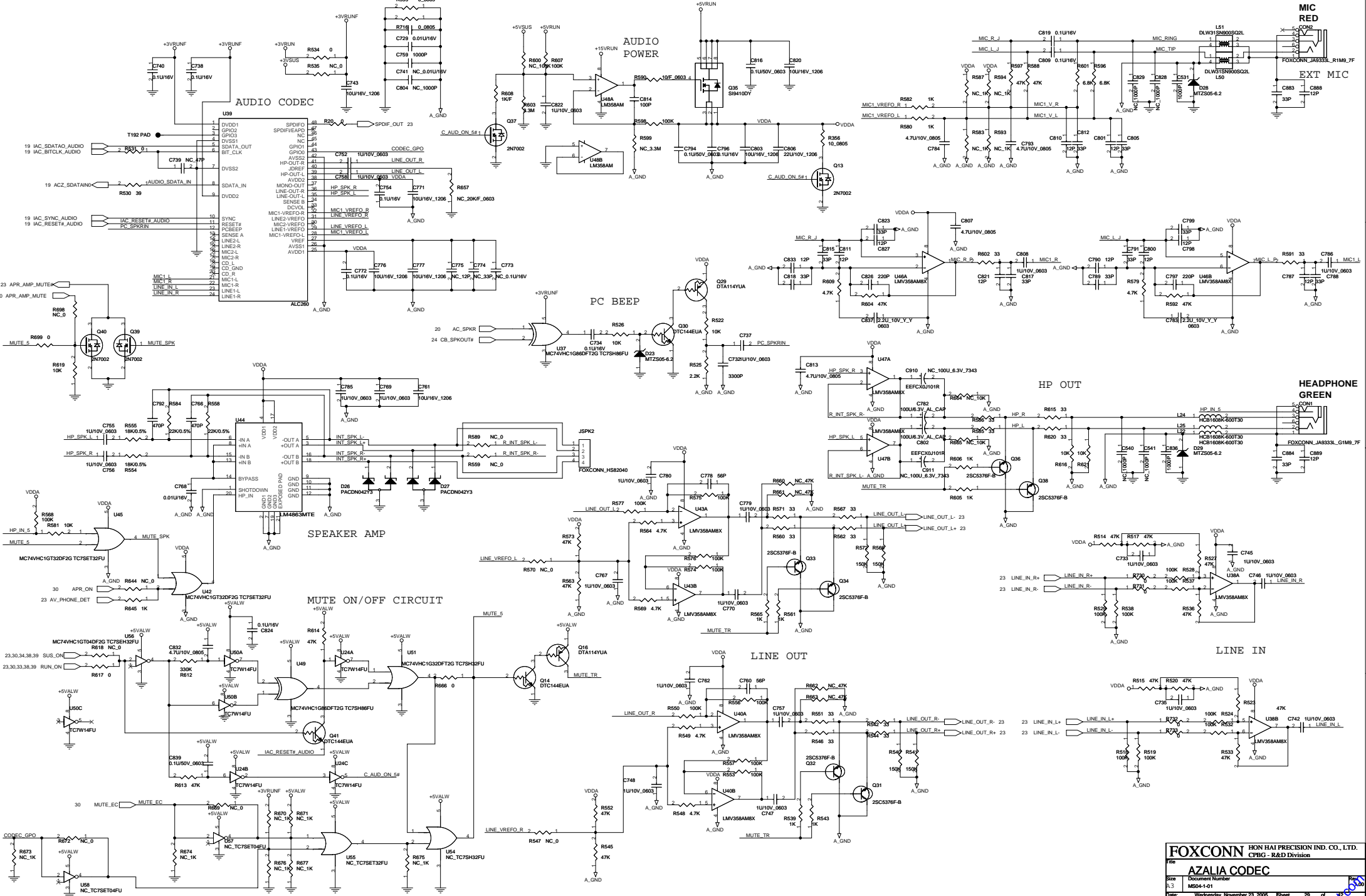




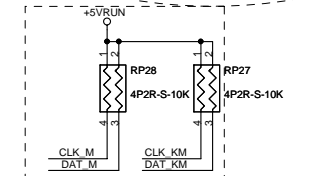
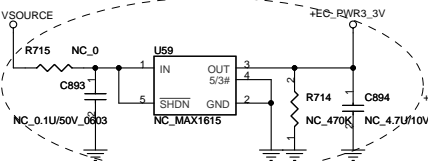
hexant@hotmail.com

Match trace length
 LAYOUT NOTES:
 Match total length of chip side Rx and Tx pair traces +/-50mil
 Match length of cable side Rx and Tx pair traces +/- 50 mil
 Total line TX+ to TX- and RX- and RX+ should be matched within 50 mils.
 Keep 50mil space between pairs and other traces. Pairs are 100ohm differential,

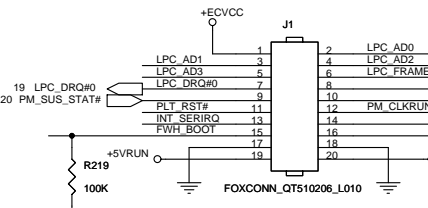




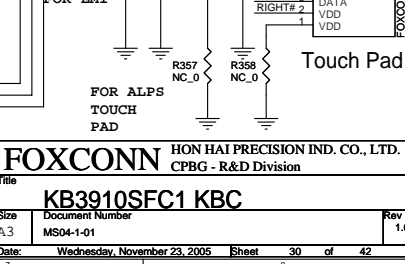
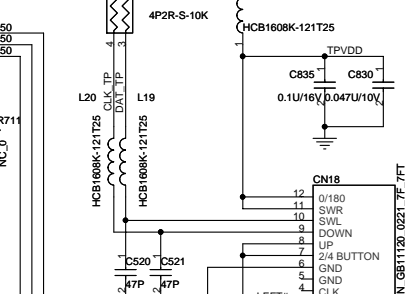
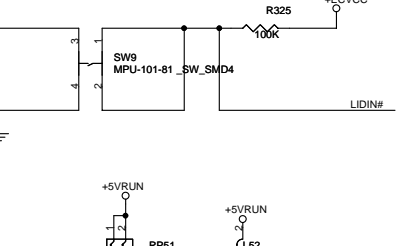
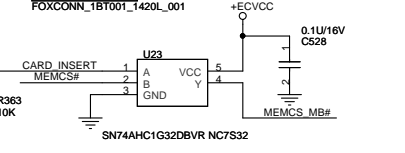
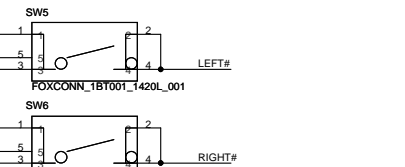
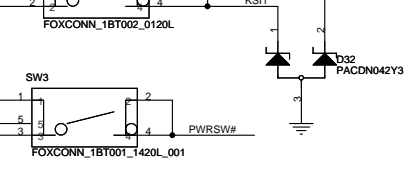
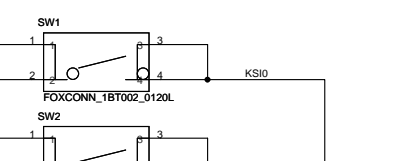
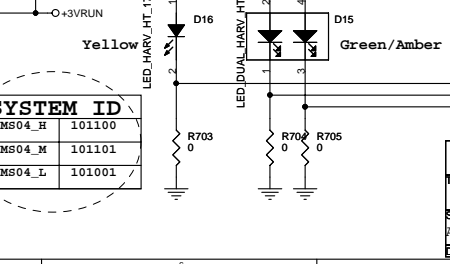
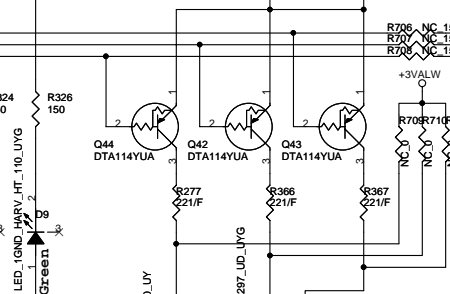
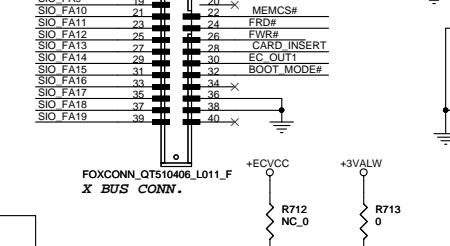
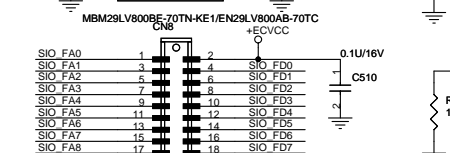
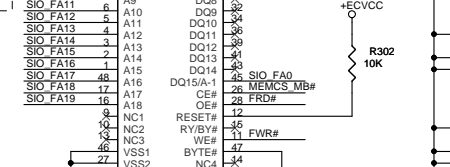
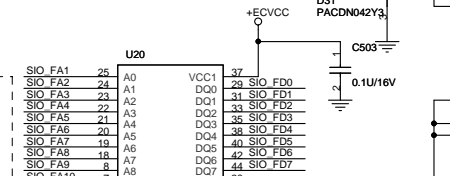
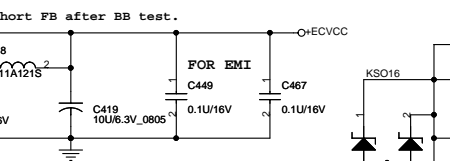
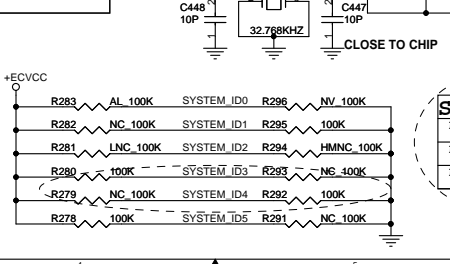
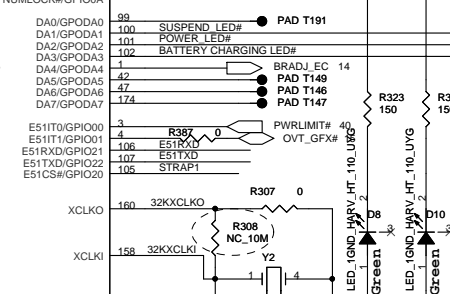
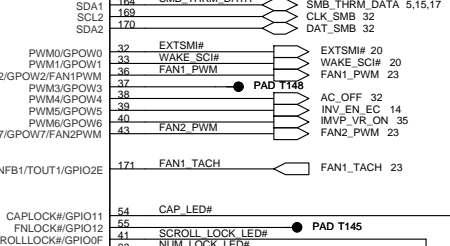
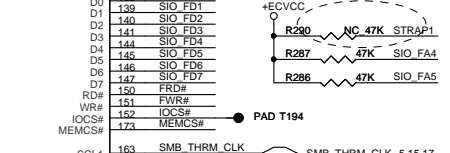
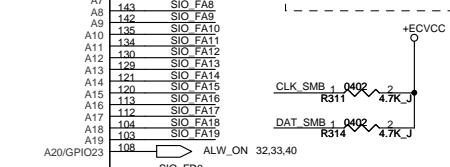
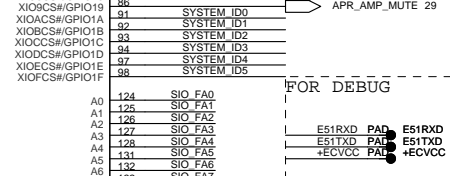
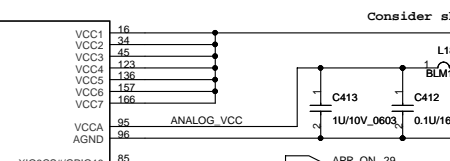
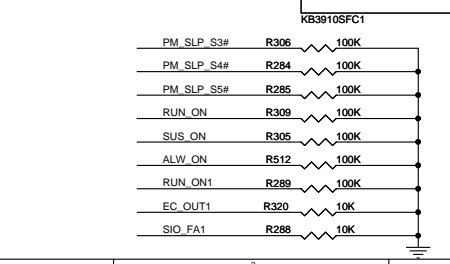
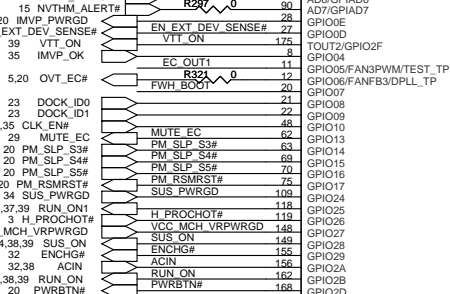
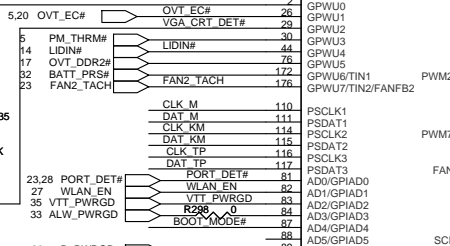
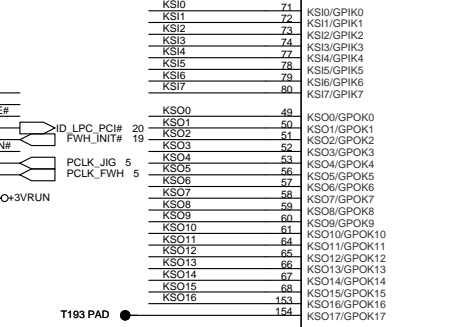
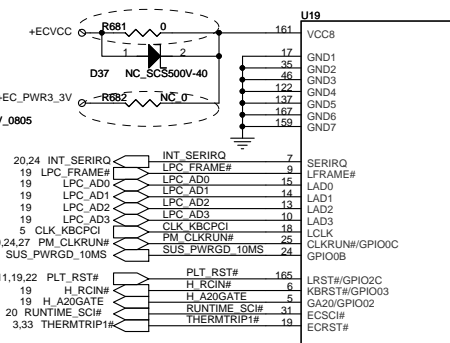
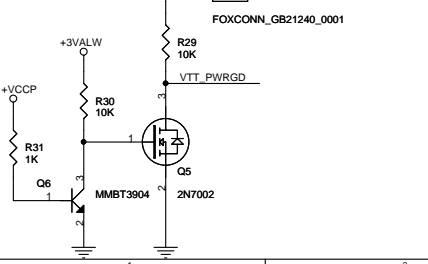
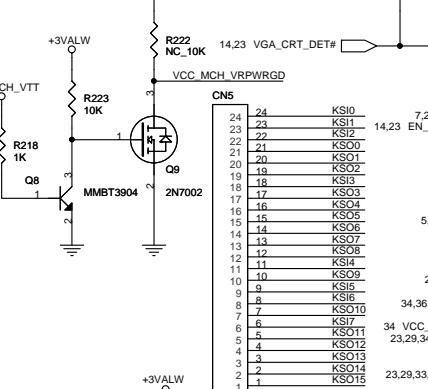
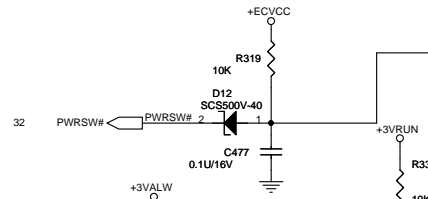
hexaint@hotmail.com



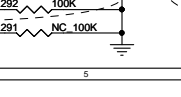
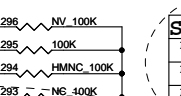
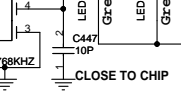
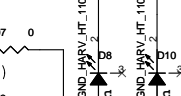
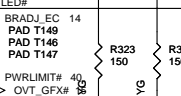
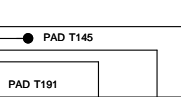
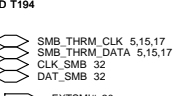
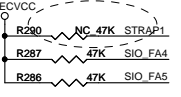
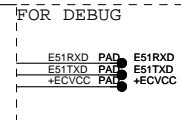
Always pull-down, even if not PS2 connector!



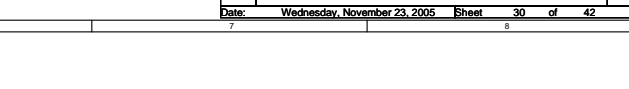
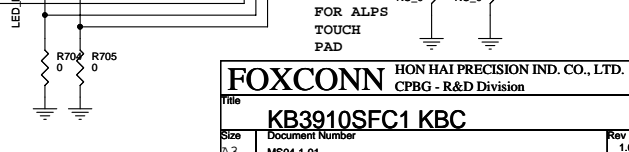
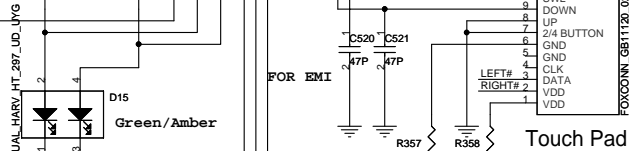
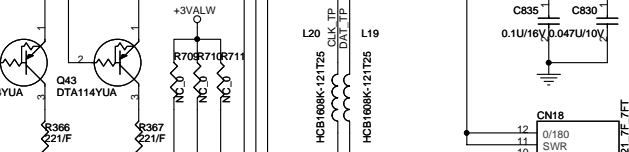
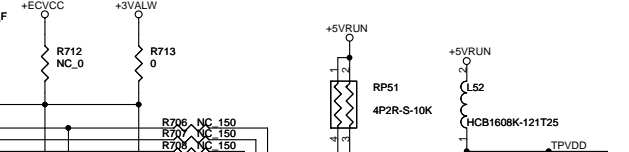
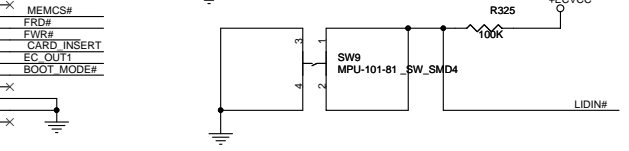
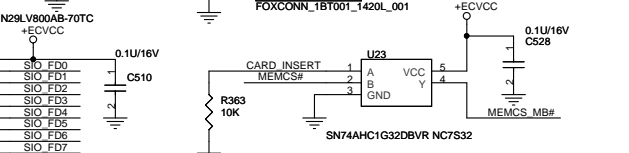
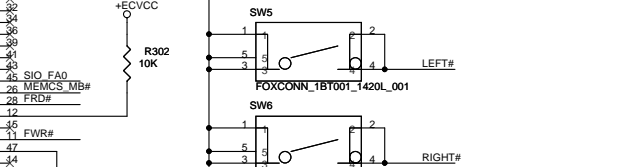
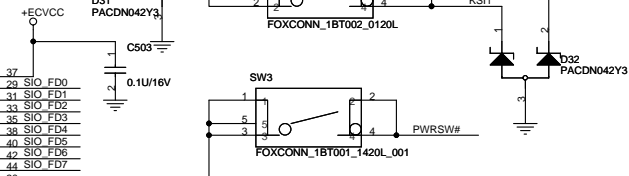
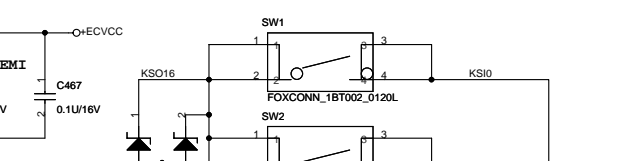
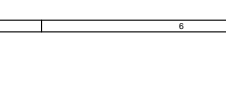
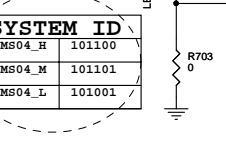
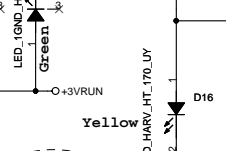
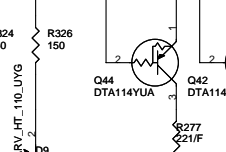
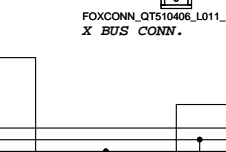
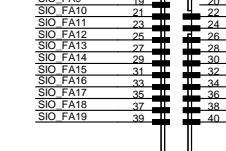
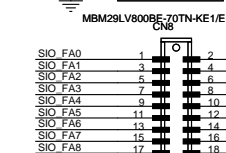
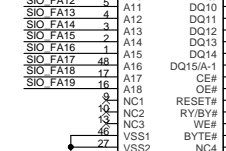
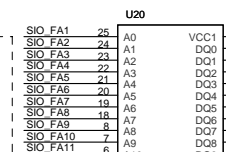
JIG-120



Consider short FB after BB test.



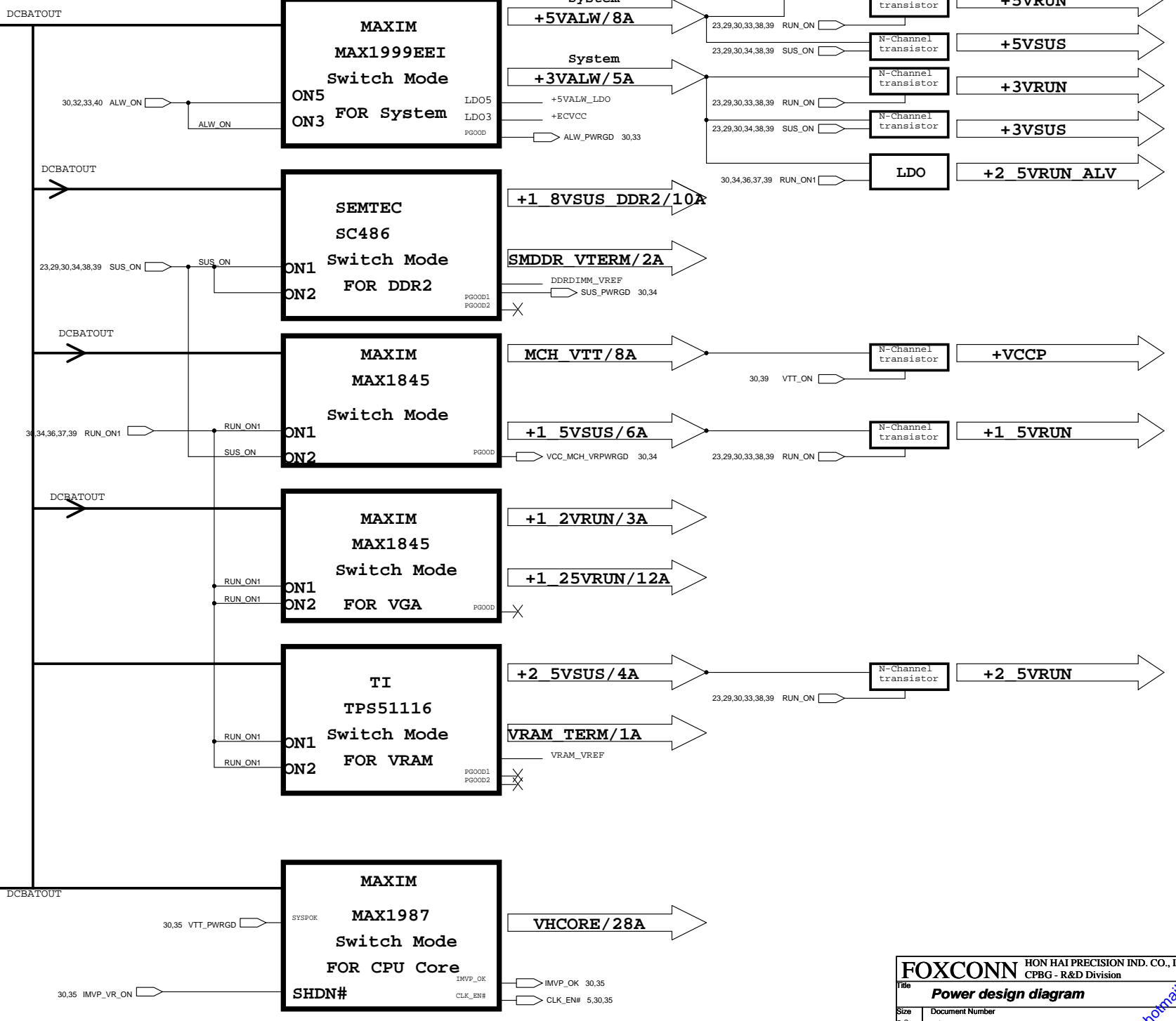
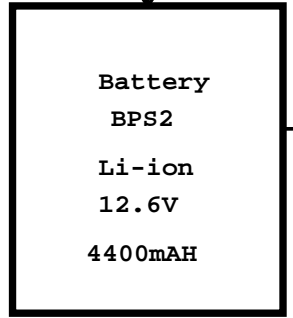
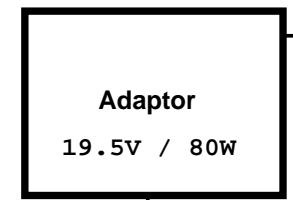
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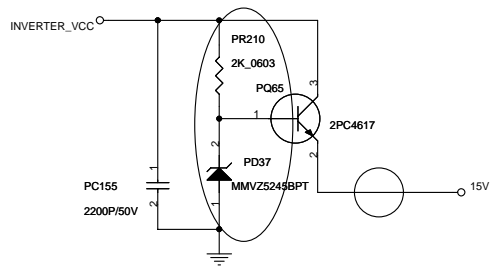
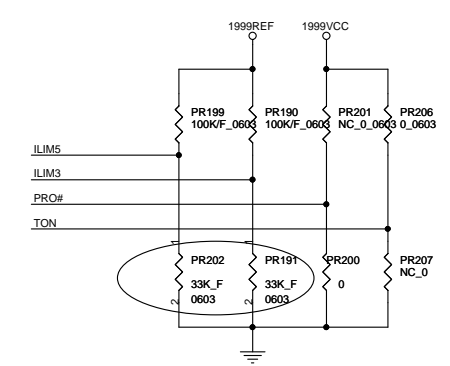
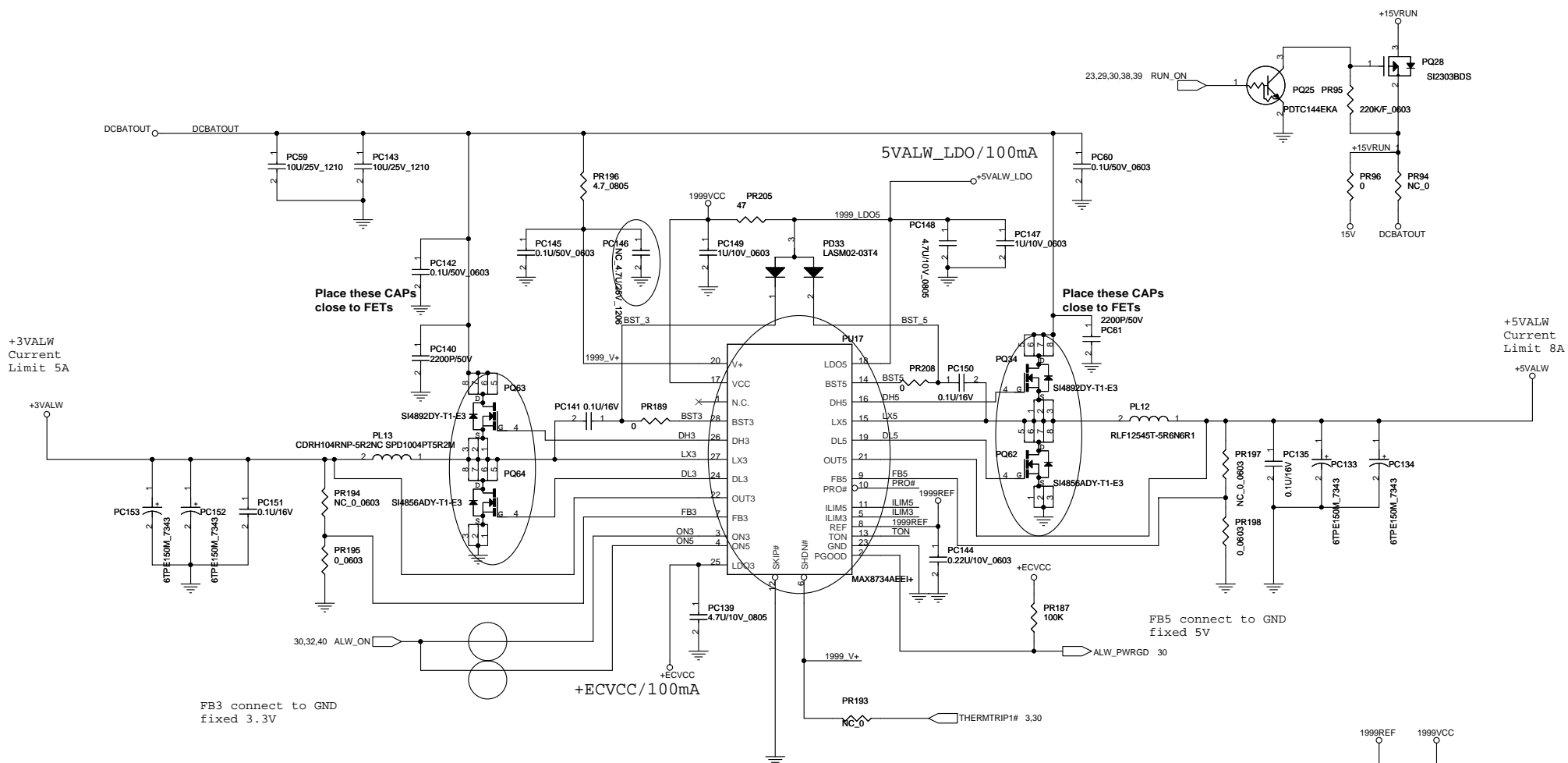
FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R & D Division

Title: **KB3910SFC1 KBC**

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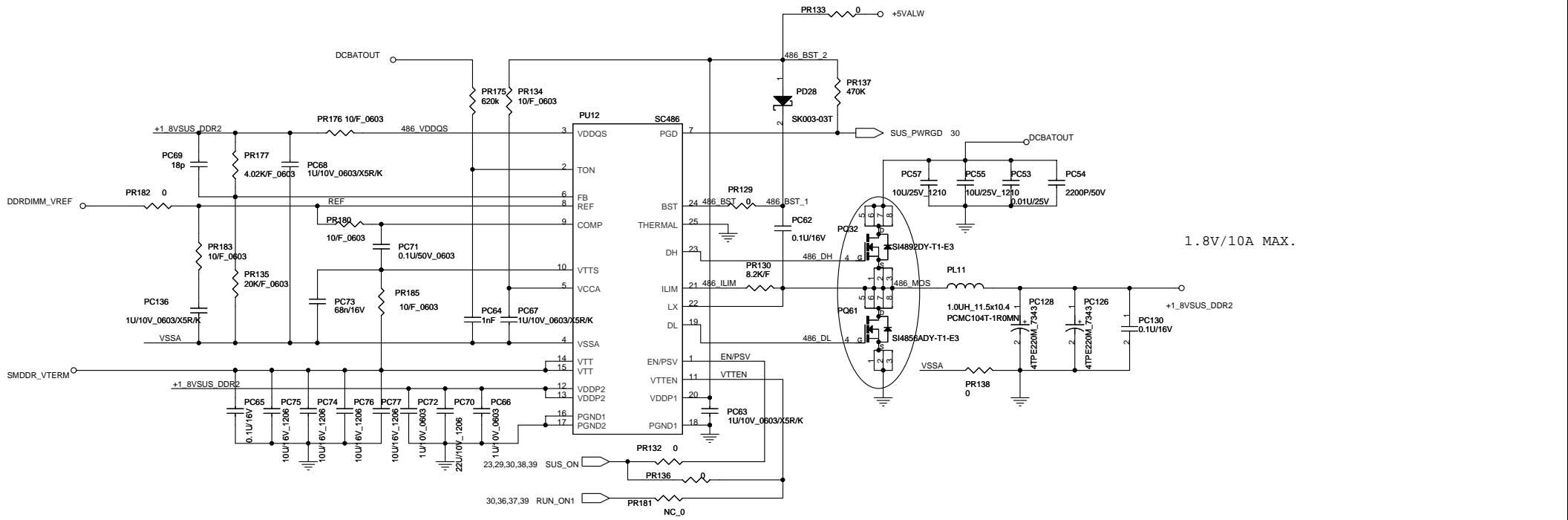


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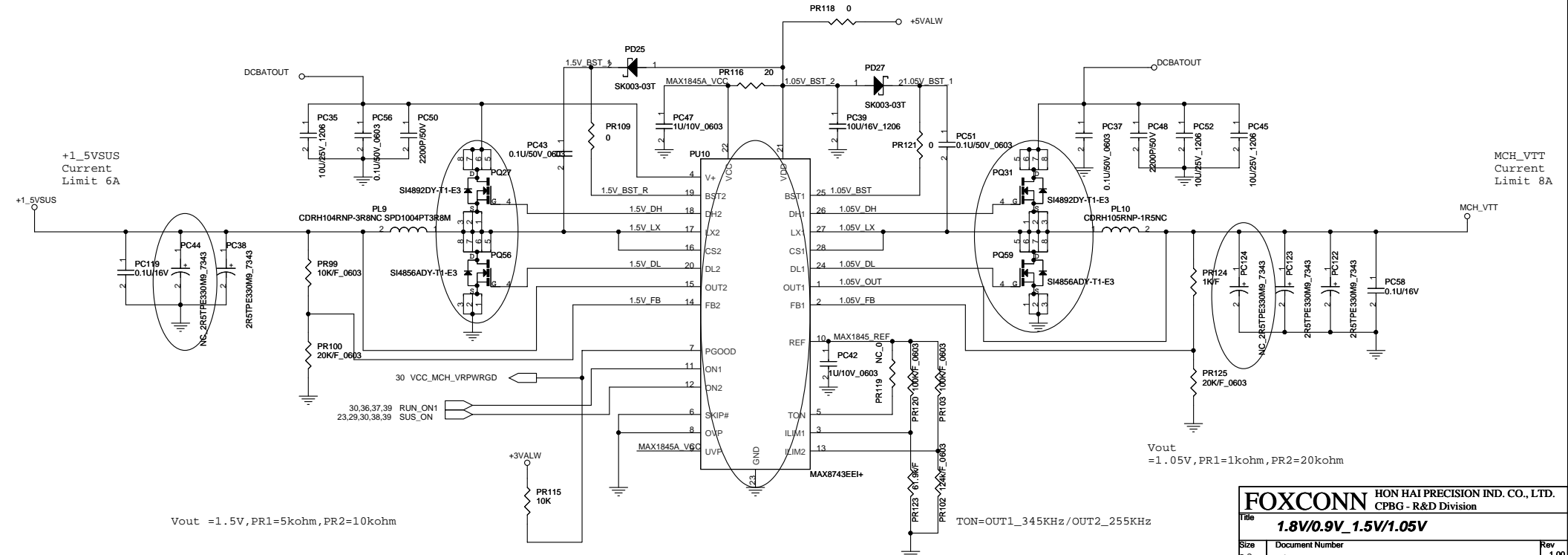


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1.8V/10A MAX.



+1.5VSUS
Current
Limit 6A

MCH_VTT
Current
Limit 8A

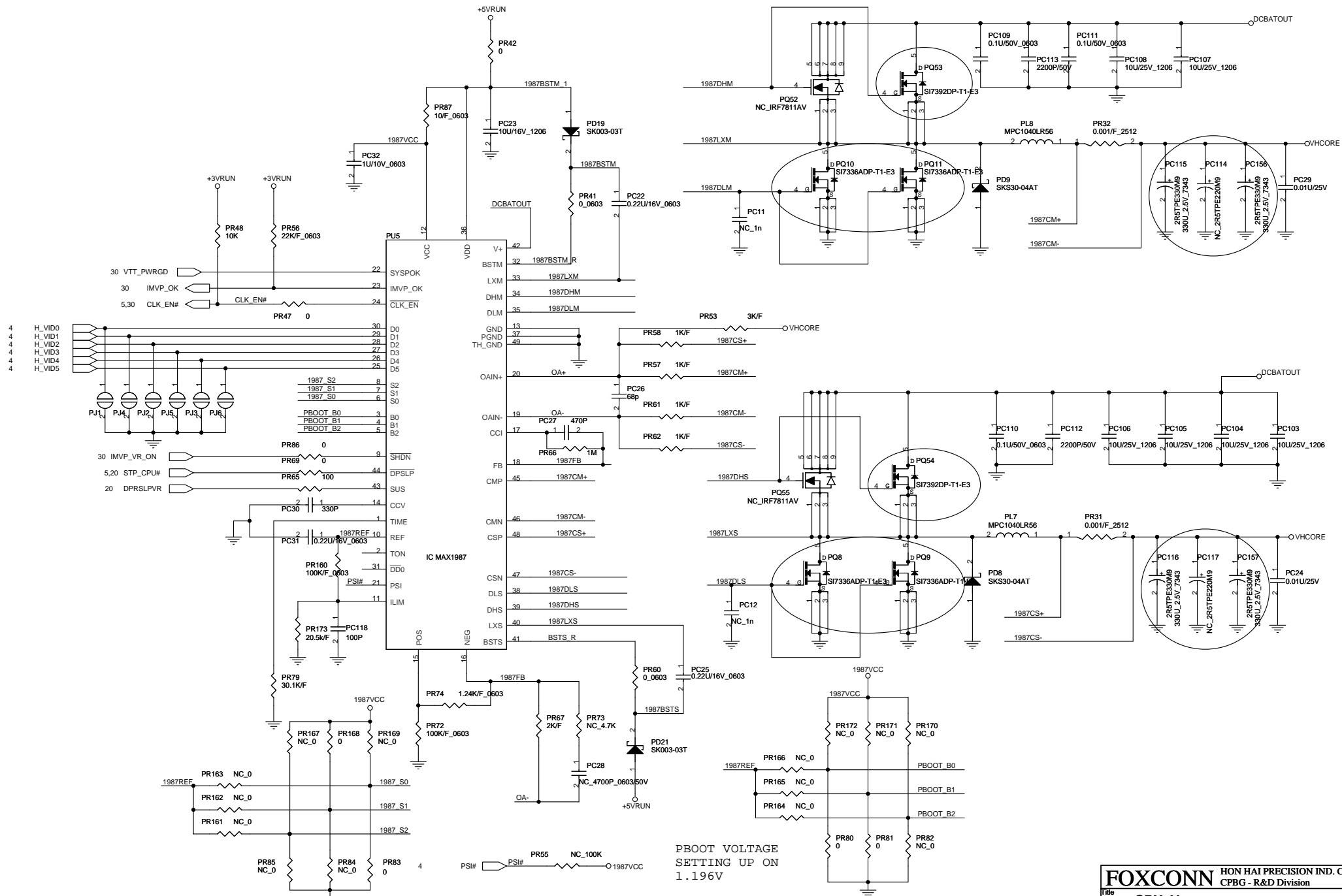
Vout = 1.5V, PR1=5kohm, PR2=10kohm

Vout = 1.05V, PR1=1kohm, PR2=20kohm

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Title
1.8V/0.9V_1.5V/1.05V

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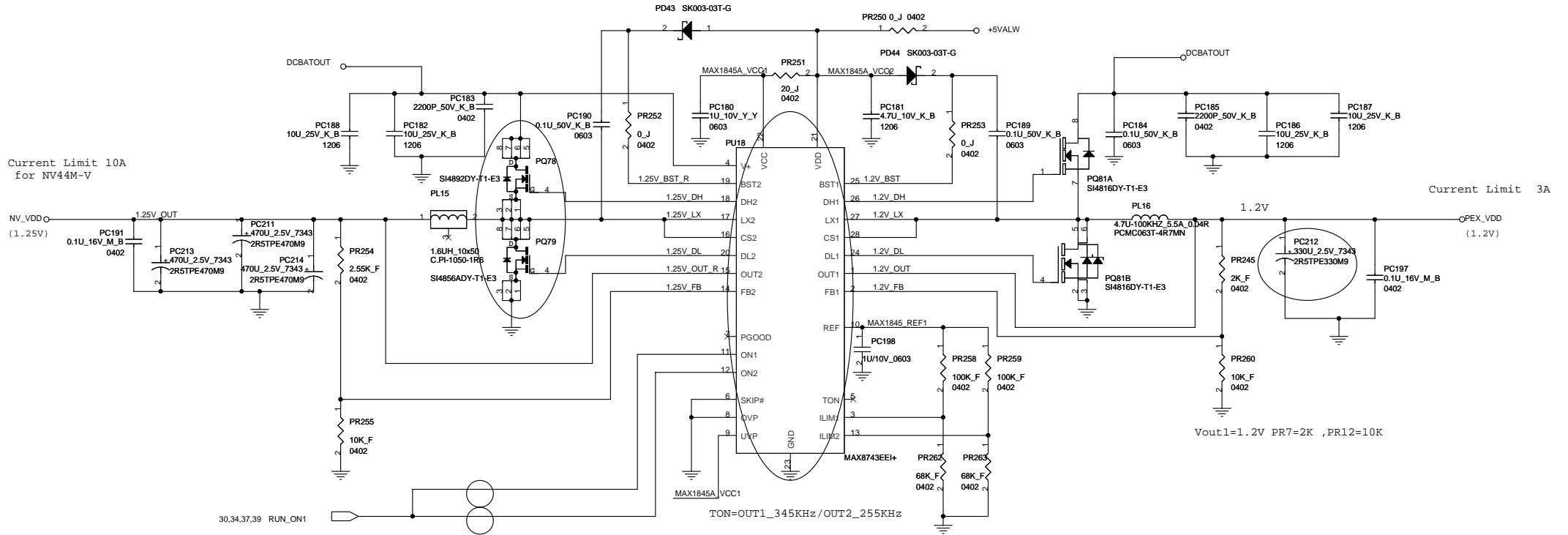


The C4 mode voltage is 0.748V TON= 300KHZ

PBOOT VOLTAGE
SETTING UP ON
1.196V

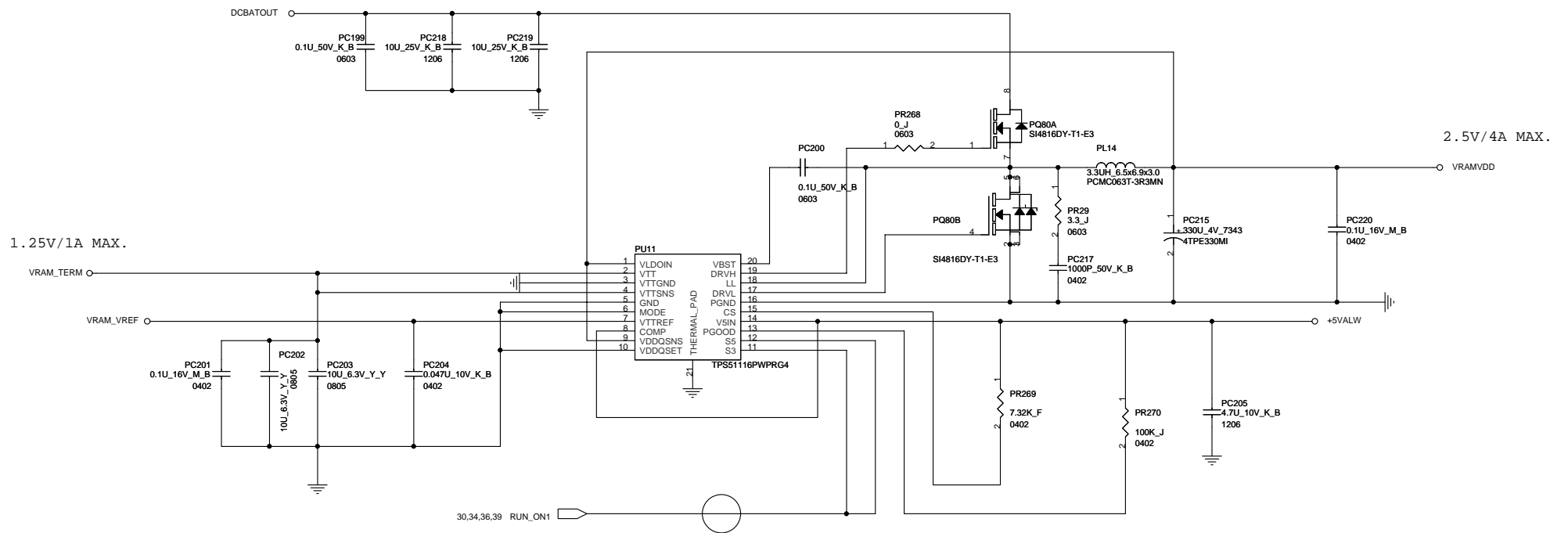
Current Limit 10A
for NV44M-V

Current Limit 3A



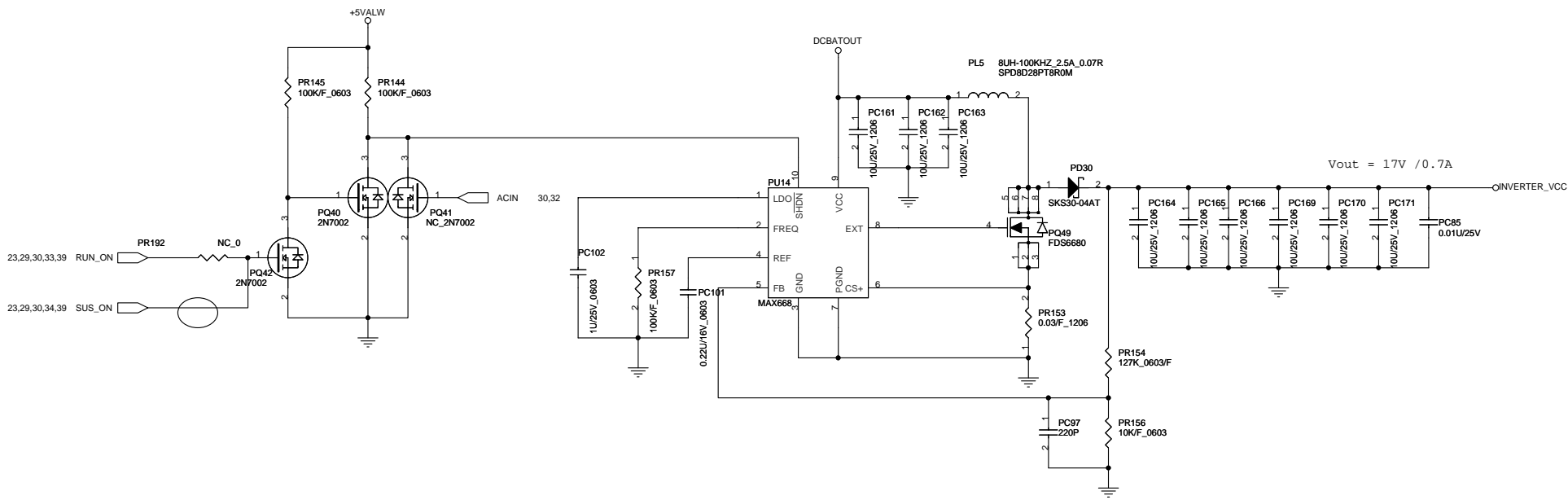
Power daughter board for VGA

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Title VGA 1.25/1.2V		
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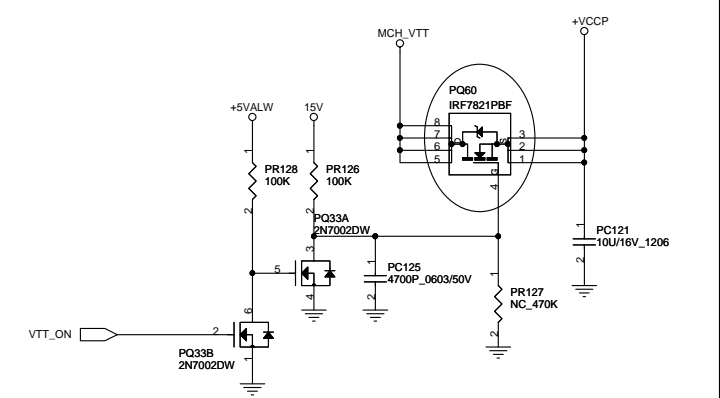
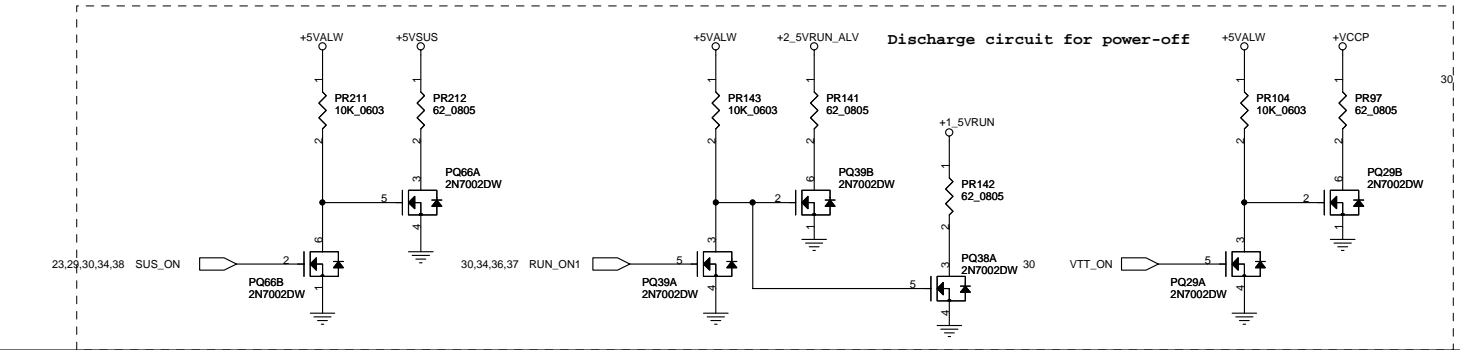
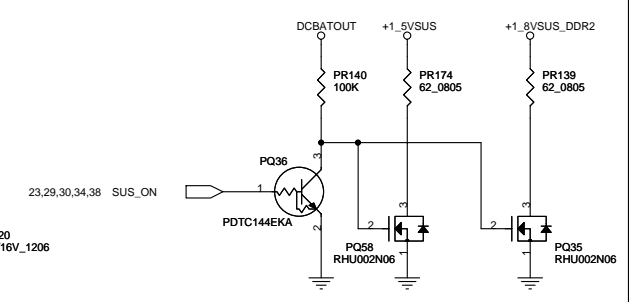
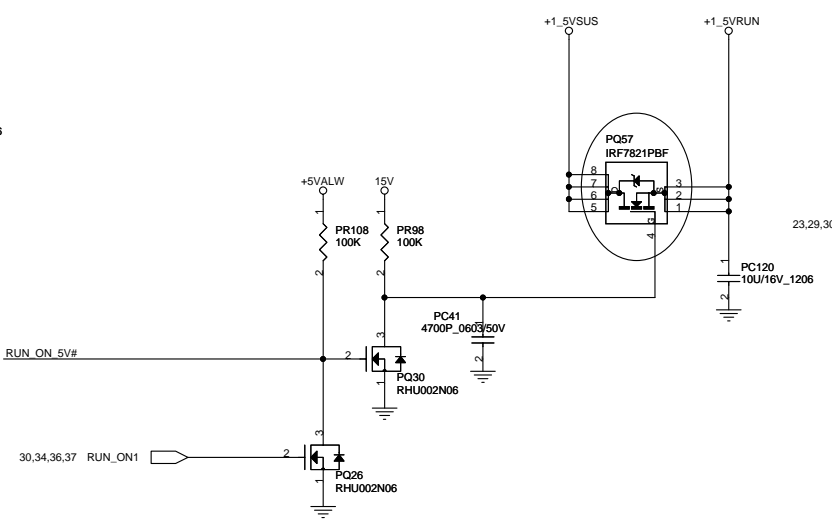
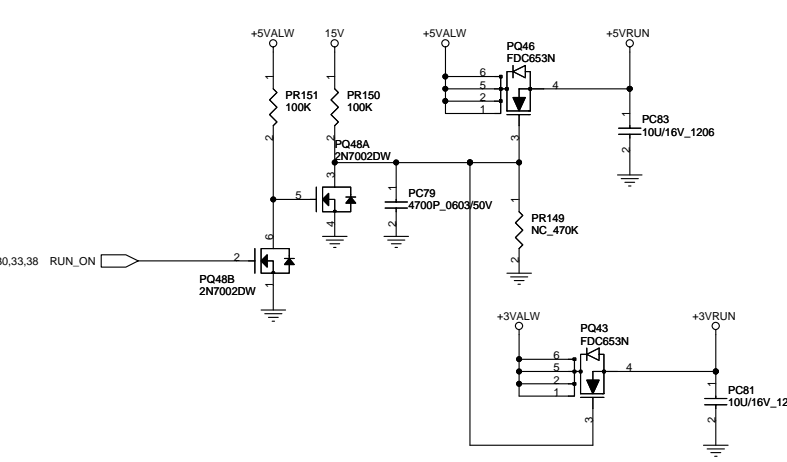
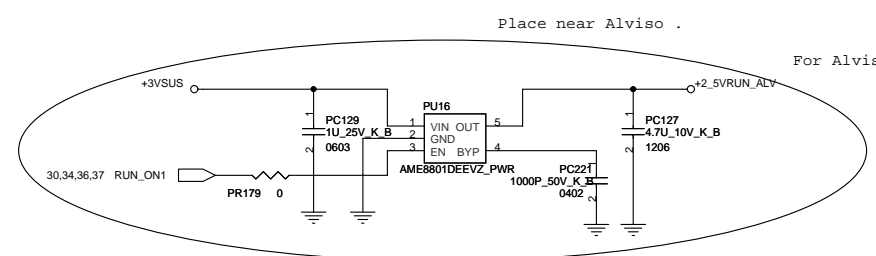
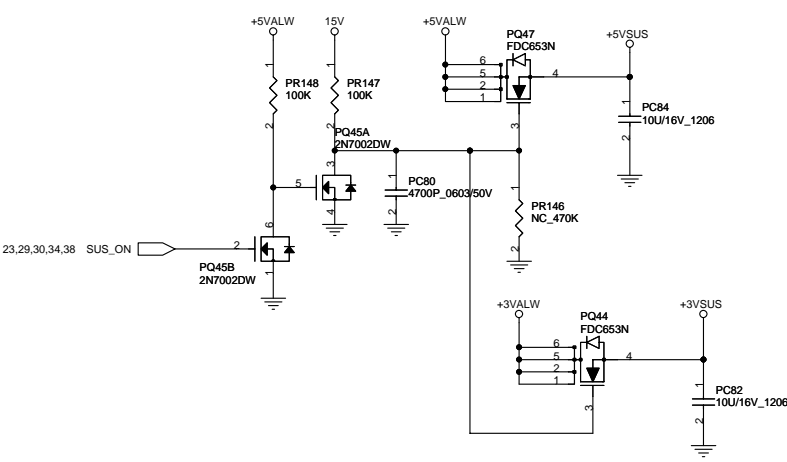


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Title VRAM 2.5V/1.25V			
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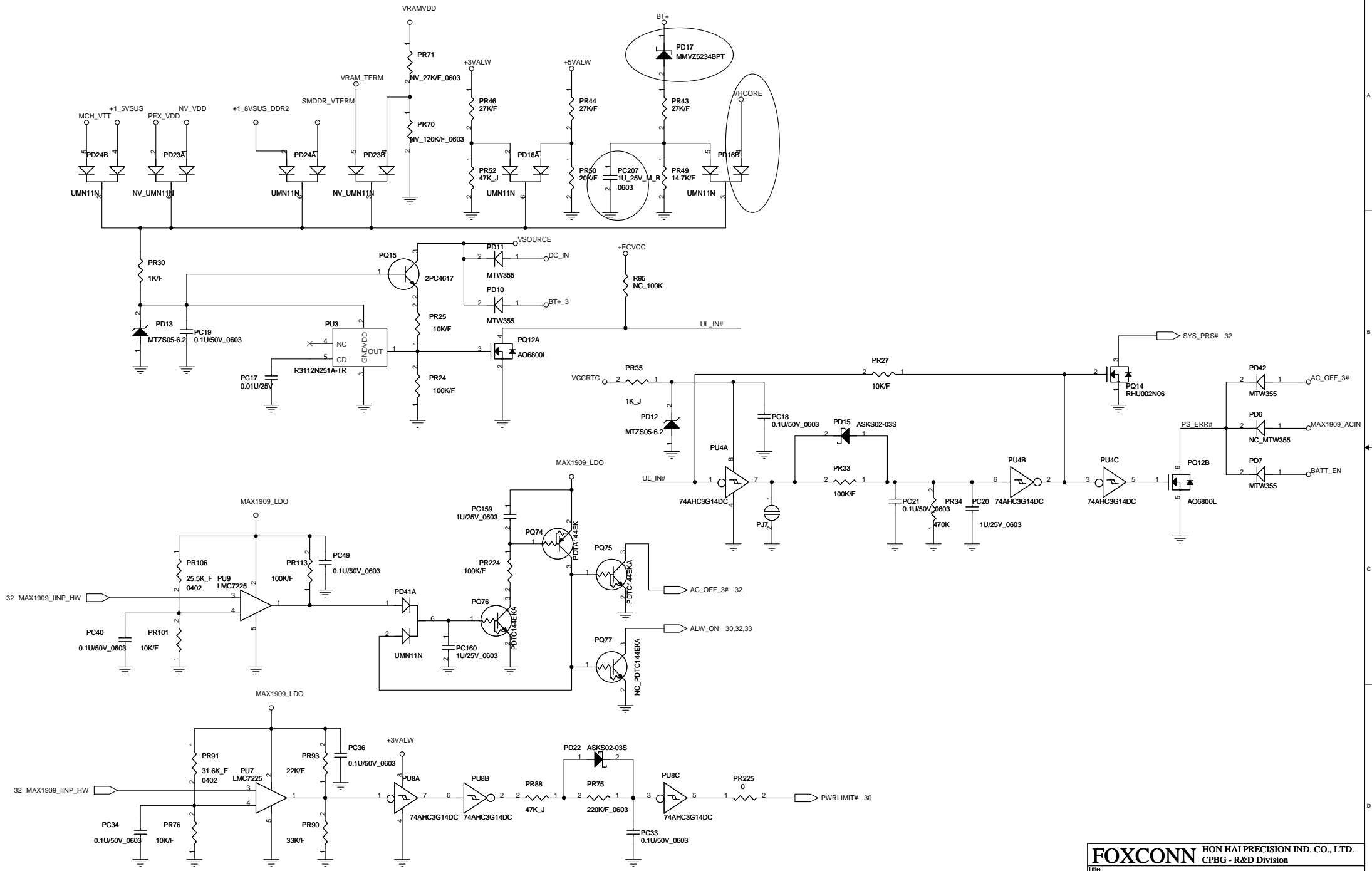


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Title STEP-UP		
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other power plan		
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HISTORY

DVT board start .

REV 0.3
(2005/08/24)
P32: Add PR77 10K/F_0402, PR78 15K/F_0402 and PC46 1UF/25V_0603 for ENCHG# pull high.

(2005/08/29)
P32: 1. Change PU6, PD20, PQ18, PQ21, PR54,PR59, PR63,PR64 and PR68 from mount to NC.
2. Add PD45 BAS316PT
Above 1. and 2. for schematic modified of battery low voltage protect function.

(2005/09/02)
P32: Change PD5 from MW400 to NC_MMPZ5253BPT
P33: Change PD37 from MTZS05-15 to MMVZ5245BPT,PR210 from 33K to 2K
P34: Change PC44 and PC124 from mount to NC.
P35: Change PC114 and PC117 from mount to NC.
P35: Change PC115, PC116, PC156 and PC157 from 2R5TPE220M9 to 2R5TPE330M9.
P36: Change PC212 from 2R5TPE470M9 to 2R5TPE330M9.
P40: Delete PD14, PD18, PR45 and PR51.
P40: Change PD17 from MTZS05-6.2 to MMVZ5234BPT

(2005/09/03)
P11: Remove L8,L39

(2005/09/05)
P30: Change U19 to KB3910SFCL,Change R715, C893, U59, R714, C894, R682, R290, R308 to SMT No Mount, R681 to Mount
P33: Delete PR184, PR186 and PR188
P36: Delete PR256 and PR261
P37: Delete PR271
P38: Delete PR220
P40: Add PC207 1UF/25V_0603 X5R

(2005/09/06)
P26: Update H32 footprint change to R corner.
P32: Change PD39 from MTZS05-5.1 to MMVZ5235BPT
P39: Change PU16 from AME8816AEHA250Z to AME8801DEEVZ
P39: Change PC127 from 10UF/25V_1206 to 4.7UF/10V_1206
P39: Change PC129 from 10UF/25V_1206 to 1UF/25V_0603

(2005/09/07)
P14: Add F2(fuse)
P33: Change PQ34 and PQ63 from FDS6612A to SI4892DY
P33: Change PQ62 and PQ64 from IRF7811AV to SI4856ADY
P34: Change PQ27, PQ31 and PQ32 from IRF7811AV to SI4892DY
P34: Change PQ56, PQ59 and PQ61 from FDS6676S to SI4856ADY
P35: Change PQ53 and PQ54 from IRF7811AV to SI7392DP
P35: Change PQ8, PQ9, PQ10 and PQ11 from FDS7064N to SI7336ADP
P36: Change PQ78 from IRF7811AV to SI4892DY
P36: Change PQ79 from FDS6676S to SI4856ADY

(2005/09/08)
P30: For New ID, Change R279.R293 to SMT No Mount , R280.R292 to Mount.
P29: Update L50,L51 footprint to (CHOKE_4P_91_126X63).

PVT board start .

(2005/10/18)
P33: Change PR191,PR202 from 75K to 33K
P33: PC146 from mount to NC
P33: Change PU17 from MAX1999 to MAX8734
P34: Change PU10 from MAX1845EEI to MAX8743EEI
P36: Change PU18 from MAX1845EEI to MAX8743EEI
P14: Change littelfuse from 4671.25(1.25A) to 467002(2A)

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MP board start .

(2005/11/22)

P39: Change PQ57,PQ60 to IRF7821PBF

P14: Change F2 (FUSE) to 0 ohm_0603

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