

SYSTEM DC/DC APL5916KAI 48		CPU DC/DC NCP6131S52MNR 42-43	
INPUTS	OUTPUTS	INPUTS	OUTPUTS
1D05V_PWR	0D85V_S0	DCBATOUT	VCC_CORE

SYSTEM DC/DC UP6128PQDD 45	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VTT

SYSTEM DC/DC UP6183PQAG 41	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5 5V_S5 3D3V_S5

SYSTEM DC/DC UP6165BQKF 46	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 0D75V_S0 DDR_VREF_S3

SYSTEM DC/DC NCP5911MNTBG 44	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE_PWR

VGA RT8208BGQW 92	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

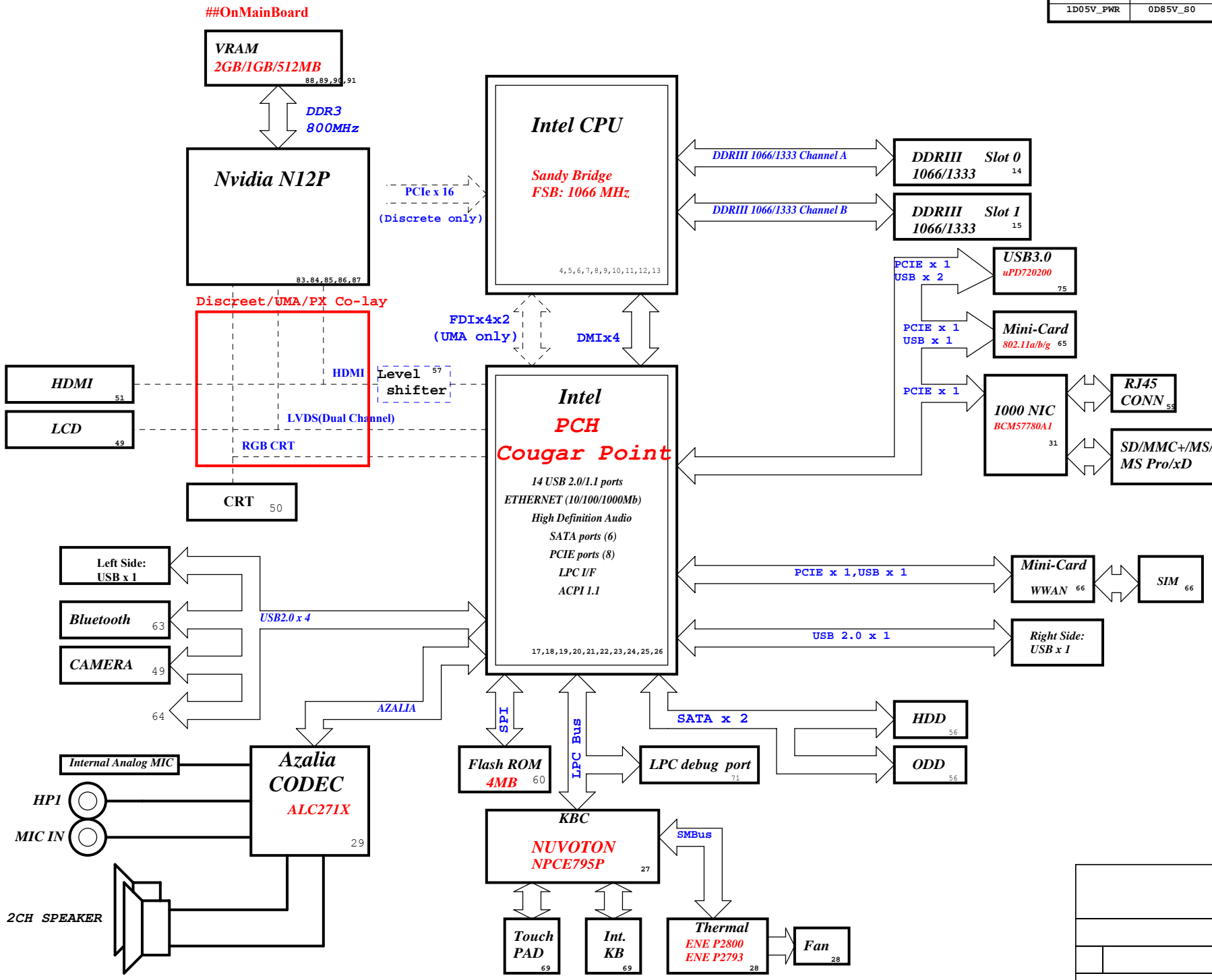
TI CHARGER BQ24745RHDR 40	
INPUTS	OUTPUTS
DCBATOUT	BT+

SYSTEM DC/DC RT9025 47	
INPUTS	OUTPUTS
3D3V_S0	1D8V_S0

SYSTEM DC/DC RT9025-25PSP 93	
INPUTS	OUTPUTS
1D5V_S3	1V_VGA_S0
3D3V_S5	1D8V_VGA_S0

Switches	
INPUTS	OUTPUTS
1D5V_S3	1D5V_VGA_S0
3D3V_S0	3D3V_VGA_S0

PCB LAYER			
L1:Top	L4:Signal	L2:VCC	L5:GND
L3:Signal	L6:Bottom		





Note:  
Intel DMI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

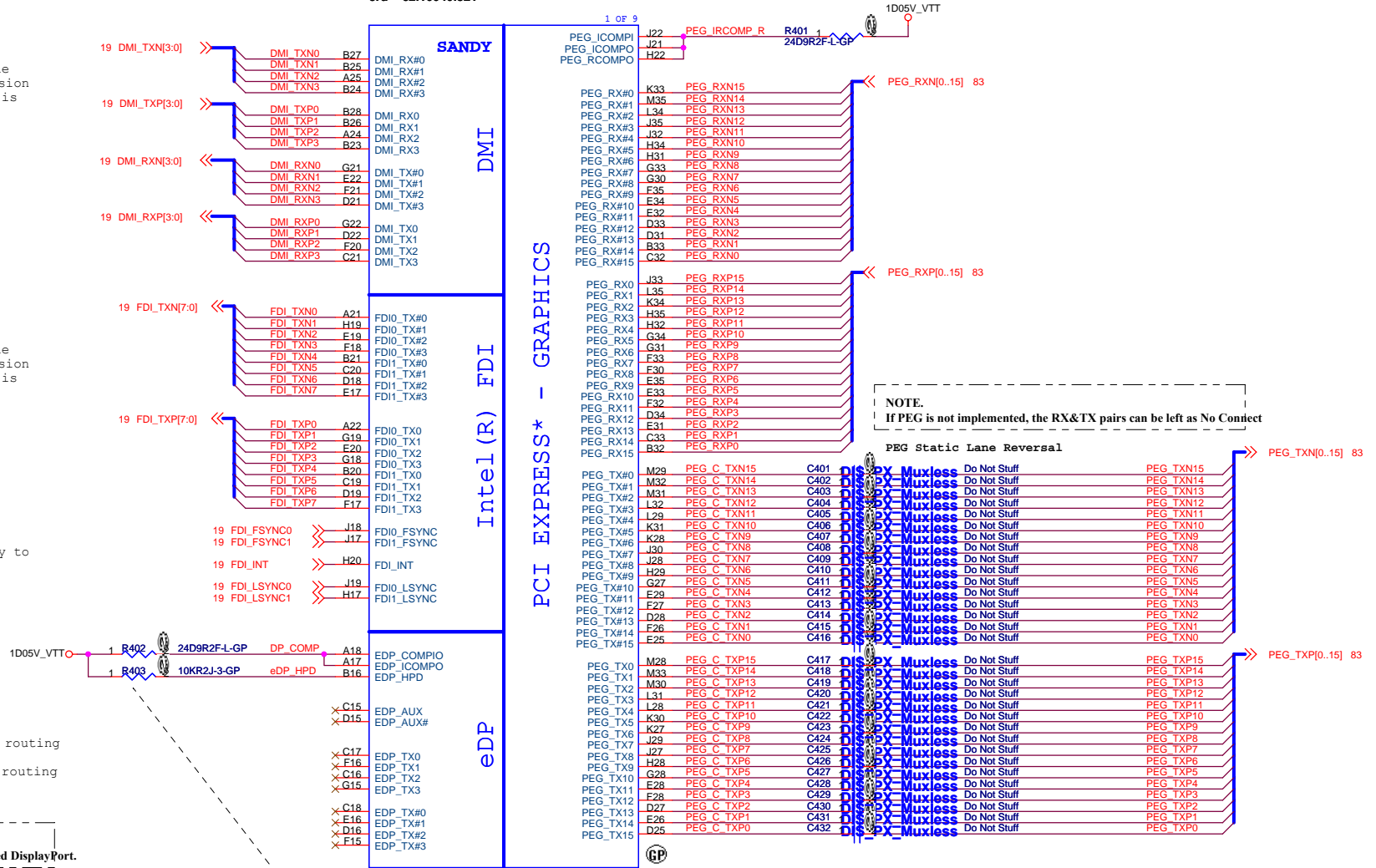
Note:  
Intel FDI supports both Lane Reversal and polarity inversion but only at PCH side. This is enabled via a soft strap.

Note:  
Lane reversal does not apply to FDI sideband signals.

Signal Routing Guideline:  
EDP\_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.  
EDP\_COMPIO keep W/S=4/15 mils and routing length less than 500 mils.

CPU1A  
SANDY  
62.10055.421  
Change:62.10053.611  
2nd = 62.10055.321  
3rd = 62.10040.821

Signal Routing Guideline:  
PEG\_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.  
PEG\_ICOMPI & PEG\_RCMP0 keep W/S=4/15 mils and routing length less than 500 mils.



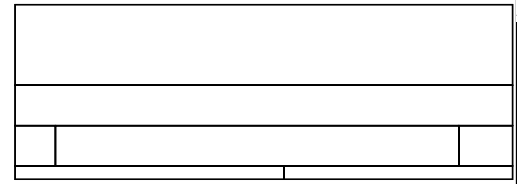
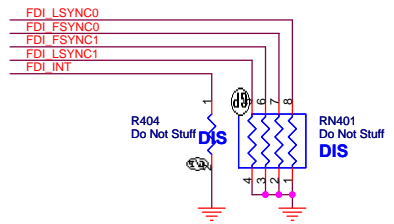
NOTE:  
If PEG is not implemented, the RX&TX pairs can be left as No Connect

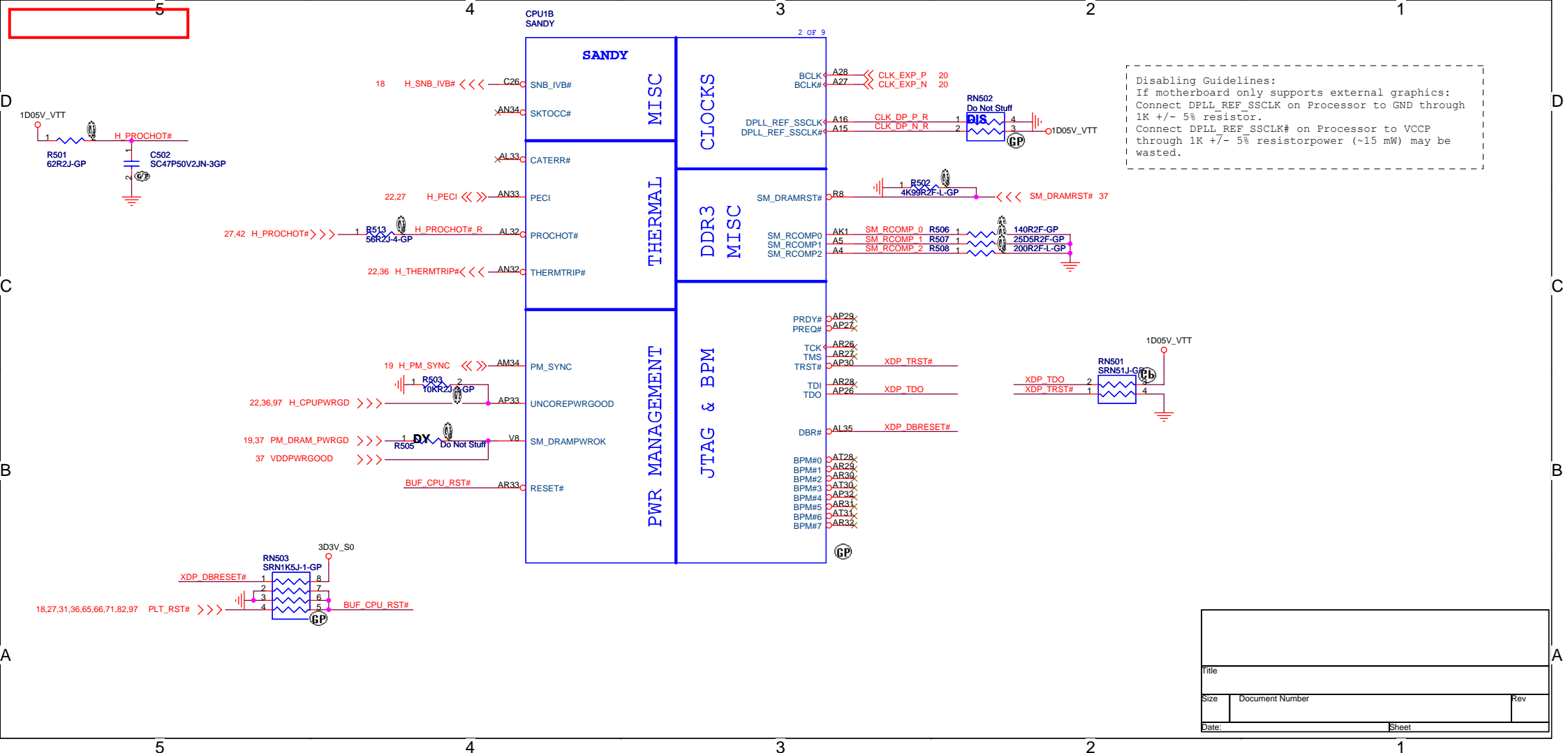
PEG Static Lane Reversal

PEG_TX#0	M29	PEG_C_TXN15	C401	Do Not Stuff	PEG_TXN15	PEG_TXN[0..15] 83
PEG_TX#1	M32	PEG_C_TXN14	C402	Do Not Stuff	PEG_TXN14	
PEG_TX#2	M31	PEG_C_TXN13	C403	Do Not Stuff	PEG_TXN13	
PEG_TX#3	L32	PEG_C_TXN12	C404	Do Not Stuff	PEG_TXN12	
PEG_TX#4	L29	PEG_C_TXN11	C405	Do Not Stuff	PEG_TXN11	
PEG_TX#5	K28	PEG_C_TXN9	C407	Do Not Stuff	PEG_TXN9	
PEG_TX#6	J30	PEG_C_TXN8	C408	Do Not Stuff	PEG_TXN8	
PEG_TX#7	J28	PEG_C_TXN7	C409	Do Not Stuff	PEG_TXN7	
PEG_TX#8	H29	PEG_C_TXN6	C410	Do Not Stuff	PEG_TXN6	
PEG_TX#9	G27	PEG_C_TXN5	C411	Do Not Stuff	PEG_TXN5	
PEG_TX#10	F29	PEG_C_TXN4	C412	Do Not Stuff	PEG_TXN4	
PEG_TX#11	E27	PEG_C_TXN3	C413	Do Not Stuff	PEG_TXN3	
PEG_TX#12	D28	PEG_C_TXN2	C414	Do Not Stuff	PEG_TXN2	
PEG_TX#13	F26	PEG_C_TXN1	C415	Do Not Stuff	PEG_TXN1	
PEG_TX#14	E25	PEG_C_TXN0	C416	Do Not Stuff	PEG_TXN0	
PEG_TX#15						
PEG_TX0	M28	PEG_C_TXP15	C417	Do Not Stuff	PEG_TXP15	PEG_TXP[0..15] 83
PEG_TX1	M33	PEG_C_TXP14	C418	Do Not Stuff	PEG_TXP14	
PEG_TX2	M30	PEG_C_TXP13	C419	Do Not Stuff	PEG_TXP13	
PEG_TX3	L31	PEG_C_TXP12	C420	Do Not Stuff	PEG_TXP12	
PEG_TX4	L28	PEG_C_TXP11	C421	Do Not Stuff	PEG_TXP11	
PEG_TX5	K30	PEG_C_TXP10	C422	Do Not Stuff	PEG_TXP10	
PEG_TX6	K27	PEG_C_TXP9	C423	Do Not Stuff	PEG_TXP9	
PEG_TX7	J29	PEG_C_TXP8	C424	Do Not Stuff	PEG_TXP8	
PEG_TX8	H28	PEG_C_TXP7	C425	Do Not Stuff	PEG_TXP7	
PEG_TX9	H28	PEG_C_TXP6	C426	Do Not Stuff	PEG_TXP6	
PEG_TX10	G28	PEG_C_TXP5	C427	Do Not Stuff	PEG_TXP5	
PEG_TX11	E28	PEG_C_TXP4	C428	Do Not Stuff	PEG_TXP4	
PEG_TX12	F28	PEG_C_TXP3	C429	Do Not Stuff	PEG_TXP3	
PEG_TX13	D27	PEG_C_TXP2	C430	Do Not Stuff	PEG_TXP2	
PEG_TX14	E26	PEG_C_TXP1	C431	Do Not Stuff	PEG_TXP1	
PEG_TX15	D25	PEG_C_TXP0	C432	Do Not Stuff	PEG_TXP0	

NOTE:  
Select a Fast FET similar to 2N7002E whose rise/fall time is less than 6 ns. If HPD on eDP interface is disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up resistor on the motherboard.

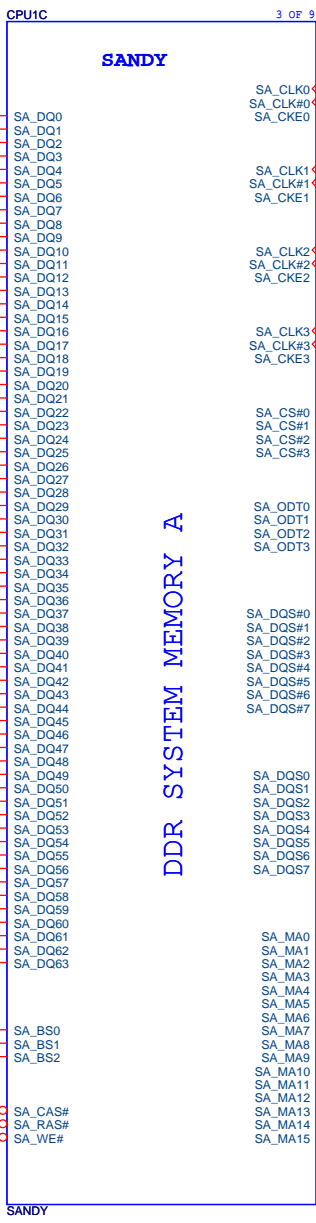
Stuff to disable internal graphics function for power saving.



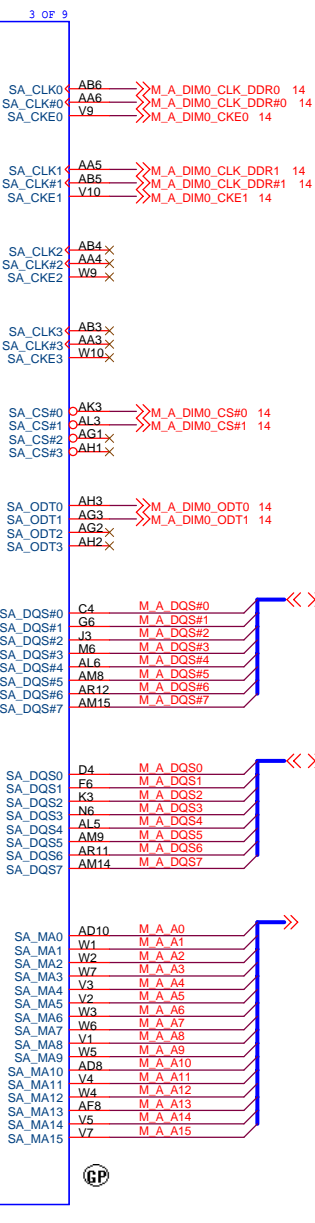


Disabling Guidelines:  
 If motherboard only supports external graphics:  
 Connect DPLL\_REF\_SSCLK on Processor to GND through  
 1K +/- 5% resistor.  
 Connect DPLL\_REF\_SSCLK# on Processor to VCCP  
 through 1K +/- 5% resistor power (~15 mW) may be  
 wasted.

Title		
Size	Document Number	Rev
Date:	Sheet	



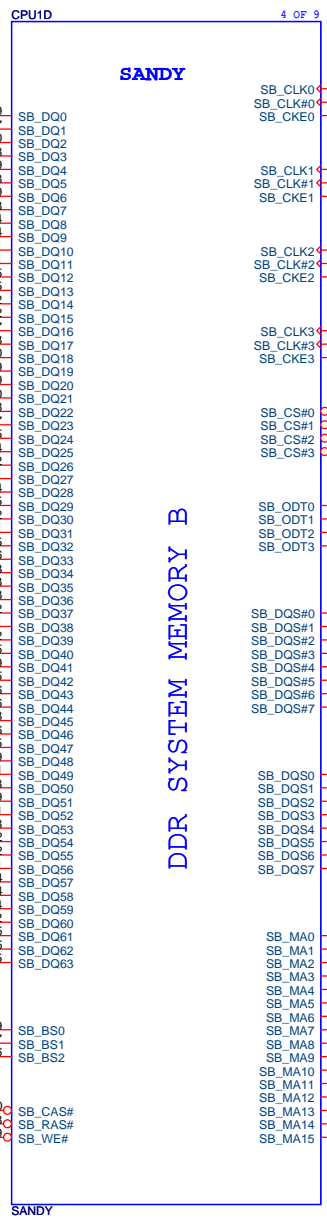
DDR SYSTEM MEMORY A



14 M.A\_DQ[63:0] <<<

14 M.A\_BS0 <<<<<  
14 M.A\_BS1 <<<<<  
14 M.A\_BS2 <<<<<

14 M.A\_CAS# <<<<<  
14 M.A\_RAS# <<<<<  
14 M.A\_WE# <<<<<



DDR SYSTEM MEMORY B

15 M.B\_DQ[63:0] <<<

15 M.B\_BS0 <<<<<  
15 M.B\_BS1 <<<<<  
15 M.B\_BS2 <<<<<

15 M.B\_CAS# <<<<<  
15 M.B\_RAS# <<<<<  
15 M.B\_WE# <<<<<

AE2  
AD2  
R9

AE1  
AD1  
R10

AB2  
AA2  
T9

AA1  
AB1  
T10

AD3  
AE3  
AD6  
AE6

AE4  
AD4  
AD5  
AE5

D7  
E3  
K6  
N3  
AN5  
AP9  
AK12  
AP15

C7  
G3  
J6  
M3  
AN6  
AP8  
AK11  
AP14

AA8  
T7  
R7  
T6  
T2  
T4  
T3  
R2  
T5  
R3  
AB7  
R1  
T1  
AB10  
R4

M.B\_DIM0\_CLK\_DDR0 15  
M.B\_DIM0\_CLK\_DDR#0 15  
M.B\_DIM0\_CKE0 15

M.B\_DIM0\_CLK\_DDR1 15  
M.B\_DIM0\_CLK\_DDR#1 15  
M.B\_DIM0\_CKE1 15

M.B\_DIM0\_CS#0 15  
M.B\_DIM0\_CS#1 15

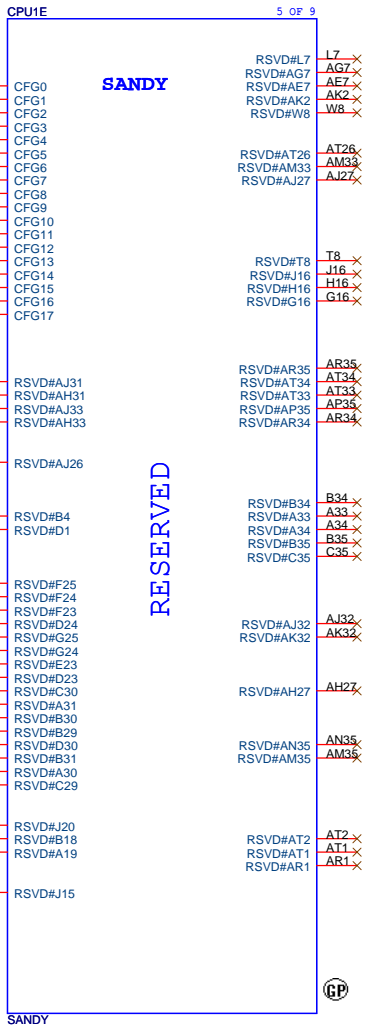
M.B\_DIM0\_ODT0 15  
M.B\_DIM0\_ODT1 15

M.B\_DQS#0[7:0] 15  
M.B\_DQS#1  
M.B\_DQS#2  
M.B\_DQS#3  
M.B\_DQS#4  
M.B\_DQS#5  
M.B\_DQS#6  
M.B\_DQS#7

M.B\_DQS0[7:0] 15  
M.B\_DQS1  
M.B\_DQS2  
M.B\_DQS3  
M.B\_DQS4  
M.B\_DQS5  
M.B\_DQS6  
M.B\_DQS7

M.B\_A[15:0] 15

Title		
Size	Document Number	Rev
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**PEG Static Lane Reversal**

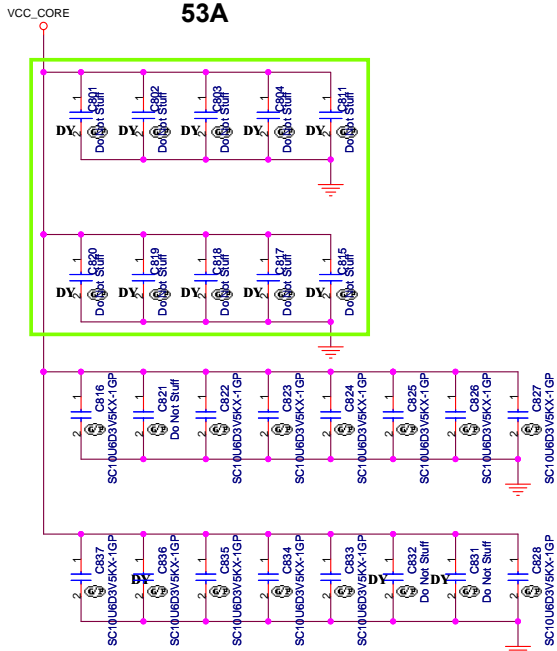
CFG2	1: Normal Operation; Lane # definition matches socket pin map definition
	<u>0: Lane Reversed</u>

Title		
Size	Document Number	Rev
Date:	Sheet	

# POWER

## PROCESSOR CORE POWER

53A



VCC\_CORE

CPU1F

SANDY

- AG35 VCC
- AG34 VCC
- AG33 VCC
- AG32 VCC
- AG31 VCC
- AG30 VCC
- AG29 VCC
- AG28 VCC
- AG27 VCC
- AG26 VCC
- AE35 VCC
- AF34 VCC
- AF33 VCC
- AF32 VCC
- AF31 VCC
- AF30 VCC
- AF29 VCC
- AF28 VCC
- AF27 VCC
- AF26 VCC
- AD35 VCC
- AD34 VCC
- AD33 VCC
- AD32 VCC
- AD31 VCC
- AD30 VCC
- AD29 VCC
- AD28 VCC
- AD27 VCC
- AD26 VCC
- AC35 VCC
- AC34 VCC
- AC33 VCC
- AC32 VCC
- AC31 VCC
- AC30 VCC
- AC29 VCC
- AC28 VCC
- AC27 VCC
- AC26 VCC
- AA35 VCC
- AA34 VCC
- AA33 VCC
- AA32 VCC
- AA31 VCC
- AA30 VCC
- AA29 VCC
- AA28 VCC
- AA27 VCC
- AA26 VCC
- Y35 VCC
- Y34 VCC
- Y33 VCC
- Y32 VCC
- Y31 VCC
- Y30 VCC
- Y29 VCC
- Y28 VCC
- Y27 VCC
- Y26 VCC
- V34 VCC
- V33 VCC
- V32 VCC
- V31 VCC
- V30 VCC
- V29 VCC
- V28 VCC
- V27 VCC
- V26 VCC
- U34 VCC
- U33 VCC
- U32 VCC
- U31 VCC
- U30 VCC
- U29 VCC
- U28 VCC
- U27 VCC
- U26 VCC
- R35 VCC
- R34 VCC
- R33 VCC
- R32 VCC
- R31 VCC
- R30 VCC
- R29 VCC
- R28 VCC
- R27 VCC
- R26 VCC
- P35 VCC
- P34 VCC
- P33 VCC
- P32 VCC
- P31 VCC
- P30 VCC
- P29 VCC
- P28 VCC
- P27 VCC
- P26 VCC

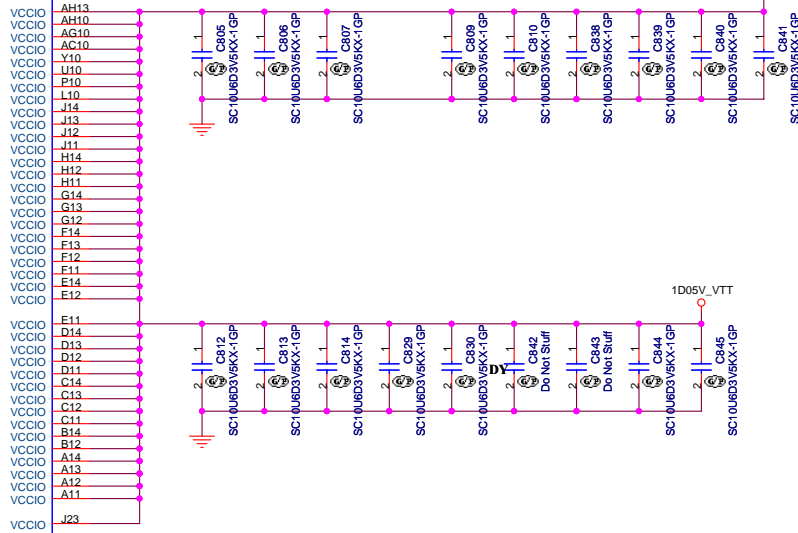
SANDY

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

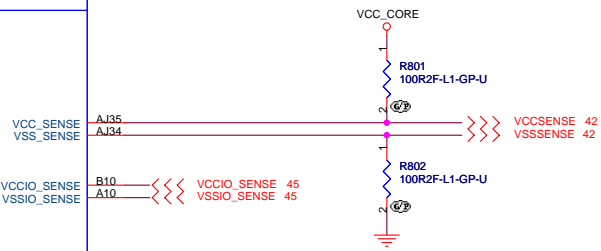


1D05V\_VTT



For CRB VIDSOUT need to pull high 130 ohm close to CPU and IMVP7  
For CRB VIDALERT# need to pull high 75 ohm close to CPU

1D05V\_VTT



VCC\_CORE

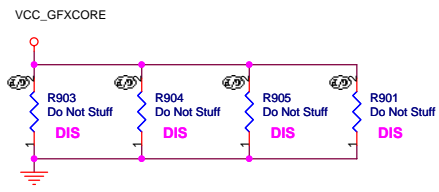
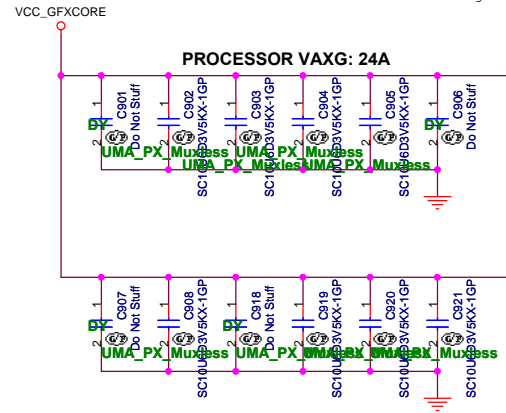
R801  
100R2F-L1-GP-U

R802  
100R2F-L1-GP-U

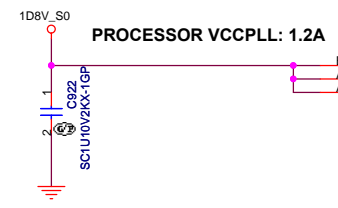
Title		
Size	Document Number	Rev
Date:	Sheet	

VAXG Output Decoupling Recommendation:  
 2 x 470 uF at Bottom Socket Edge  
 2 x 22 uF at Top Socket Cavity  
 4 x 22 uF at Top Socket Edge  
 2 x 22 uF at Bottom Socket Cavity  
 4 x 22 uF at Bottom Socket Edge

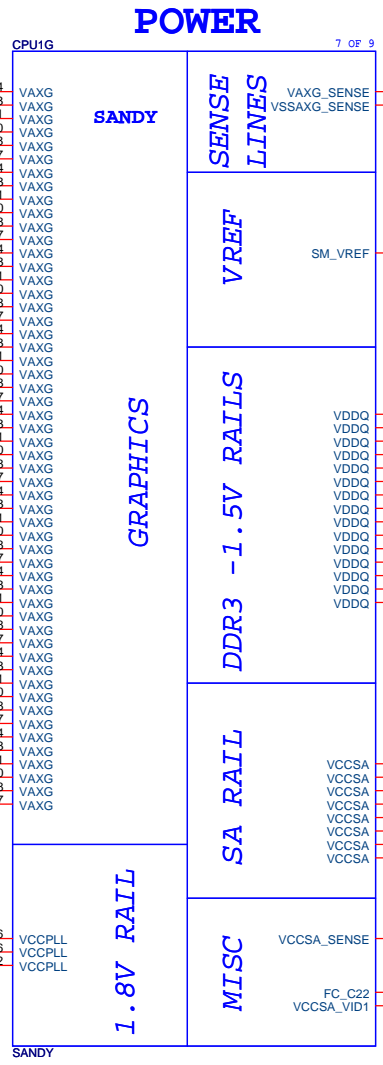
R906,R907 close to CPU



Disabling Guidelines for External Graphics Designs:  
 Can connect to GND if motherboard only supports external graphics and if GFX VR is not stuffed.  
 Can be left floating (Gfx VR keeps VAXG rail from floating) if the VR is stuffed



VCCPLL Output Decoupling Recommendation:  
 1 x 330 uF  
 2 x 1 uF  
 1 x 10 uF



**POWER**

**SENSE LINES**

**VREF**

**DDR3 - 1.5V RAILS**

**SA RAIL**

**MISC**

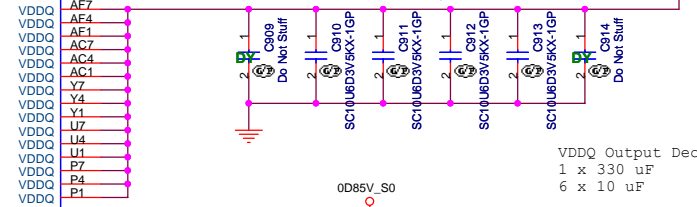
**1.8V RAIL**

VAXG\_SENSE AK35  
 VSSAXG\_SENSE AK34  
 VCC\_AXG\_SENSE 42  
 VSS\_AXG\_SENSE 42  
 Refer to the latest Huron River Mainstream PDG (Doc# 436735) for more details on s3 power reduction implementation.  
 +V\_SM\_VREF\_CNT should have 10 mil trace width

SM\_VREF AL1 <<< +V\_SM\_VREF\_CNT 37

Routing Guideline:  
 Power from DDR VREF\_S3 and +V\_SM\_VREF\_CNT should have 10 mils trace width.

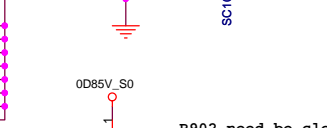
**PROCESSOR VDDQ: 10A**



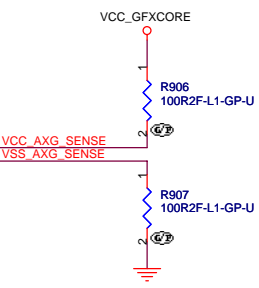
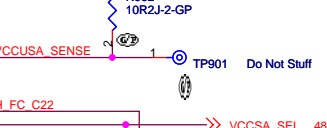
VDDQ Output Decoupling Recommendation:  
 1 x 330 uF  
 6 x 10 uF

**PROCESSOR VCCSA: 6A**

VCCSA Output Decoupling Recommendation:  
 1 x 330 uF  
 2 x 10 uF at Bottom Socket Cavity  
 1 x 10 uF at Bottom Socket Edge

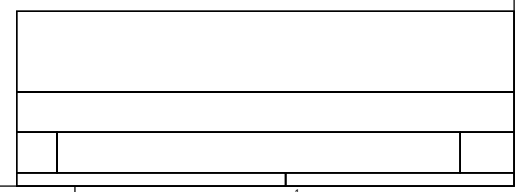
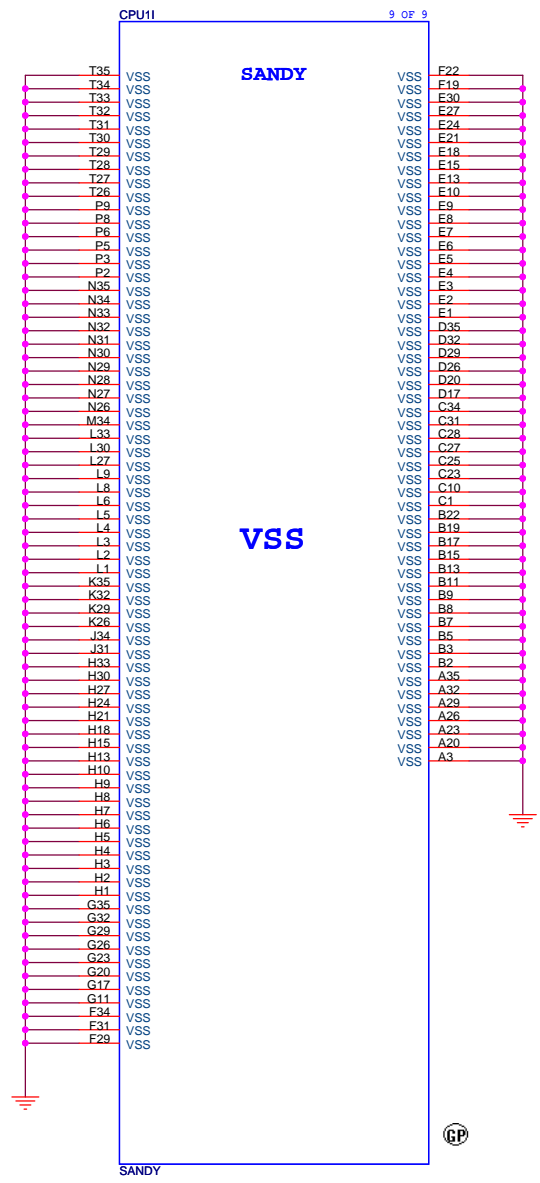
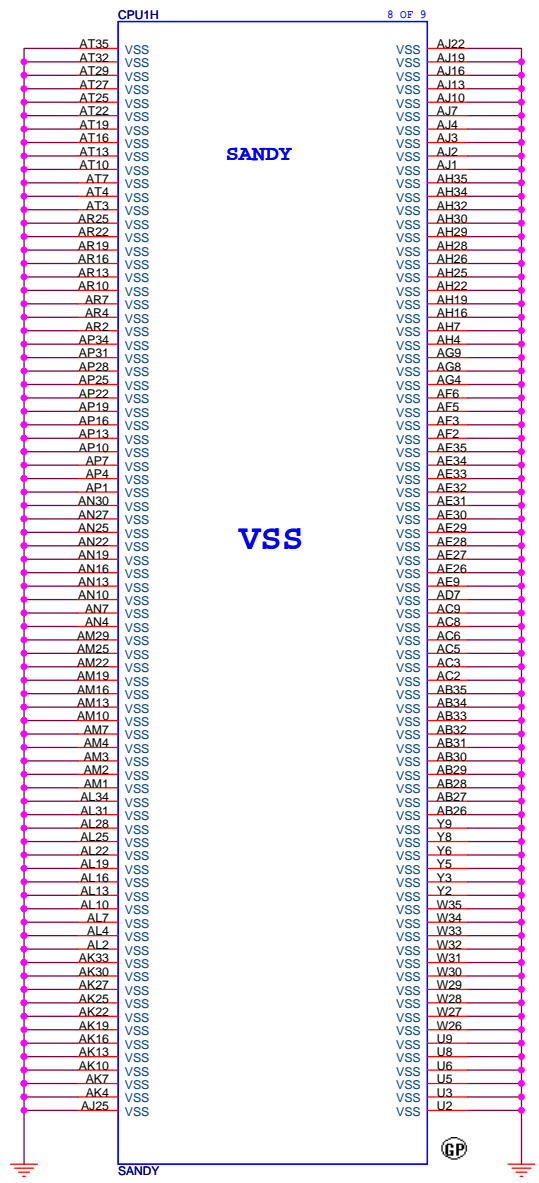


R902 need be close to pin H23.



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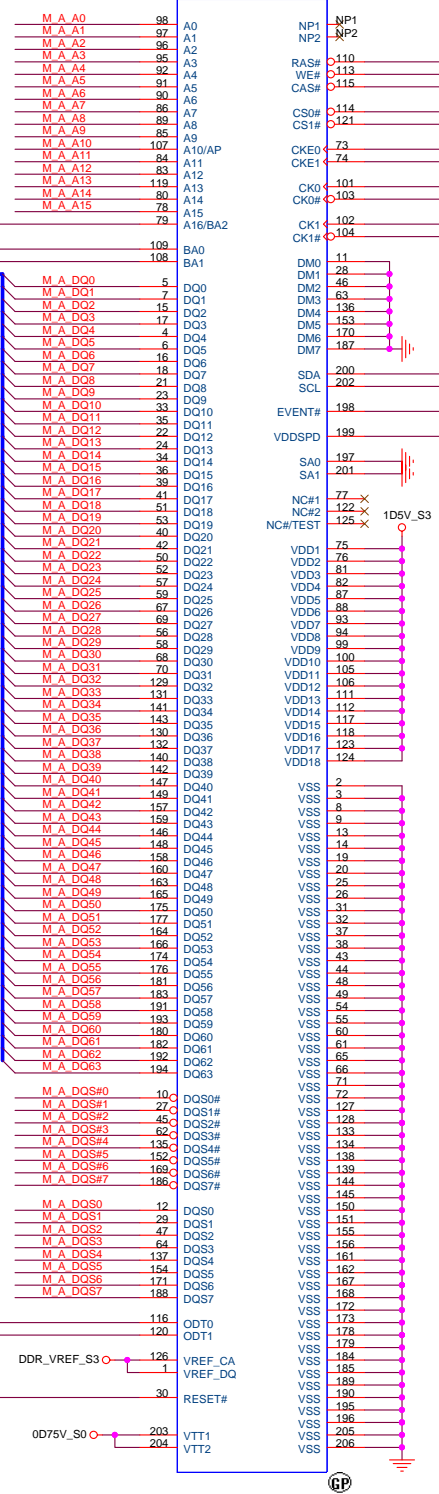
M\_A\_A[15:0] 6

M\_A\_BS2 >>>  
M\_A\_BS0 >>>  
M\_A\_BS1 >>>  
M\_A\_DQ[63:0]

M\_A\_DQS[7:0] 6  
M\_A\_DQS[7:0] 6

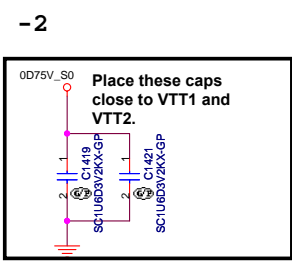
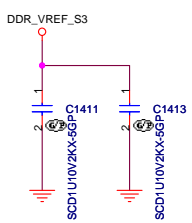
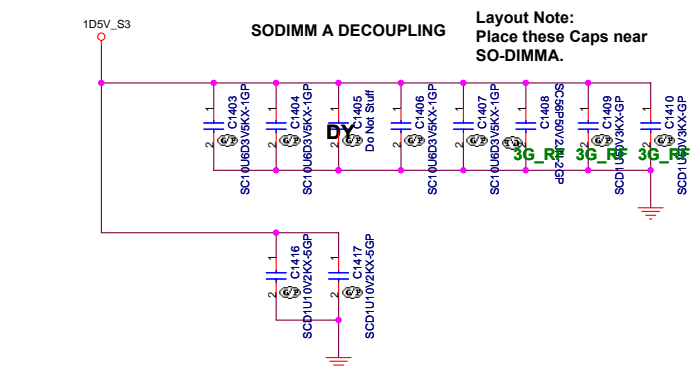
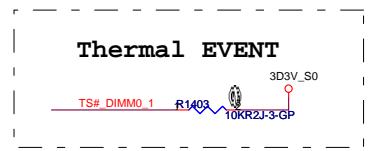
M\_A\_DIM0\_ODT0 >>>  
M\_A\_DIM0\_ODT1 >>>

15.37 DDR3\_DRAMRST# >>>



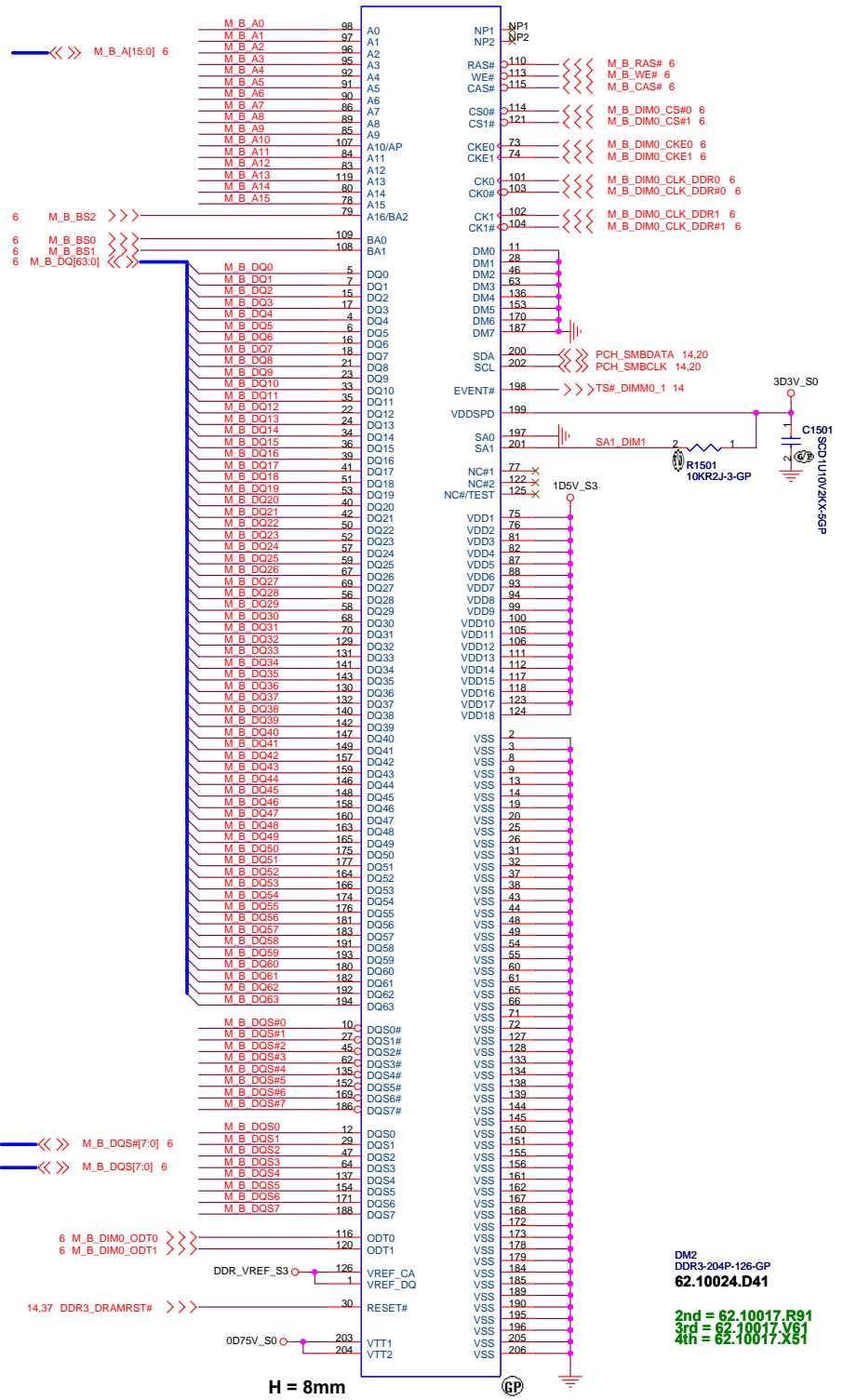
DM1  
DDR3-204P-122-GP  
62.10017.Z51  
2nd = 62.10017.V51  
3rd = 62.10017.M51  
4th = 62.10017.X41

Note:  
If SA0\_DIM0 = 0, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA0  
SO-DIMMA TS Address is 0x30  
  
If SA0\_DIM0 = 1, SA1\_DIM0 = 0  
SO-DIMMA SPD Address is 0xA2  
SO-DIMMA TS Address is 0x32

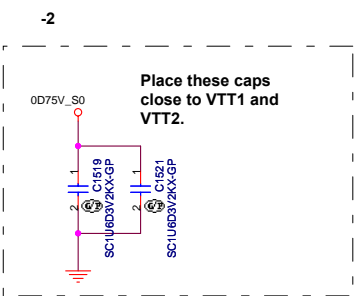
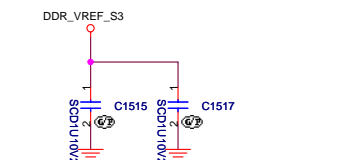
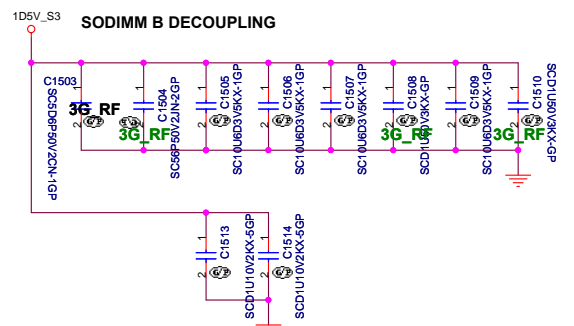


PART NUMBER	Height	TYPE


# SSID = MEMORY

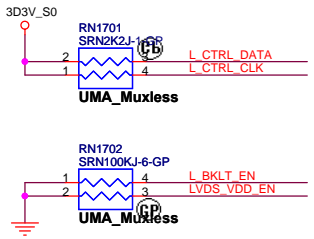


Layout Note:  
Place these Caps near  
SO-DIMMB.

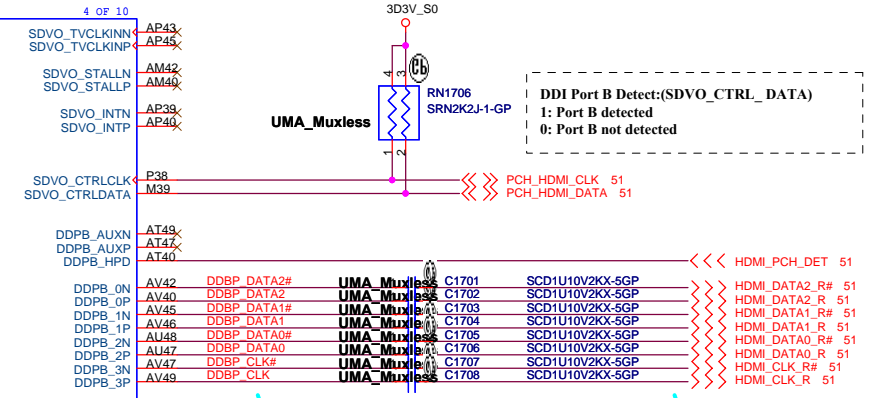
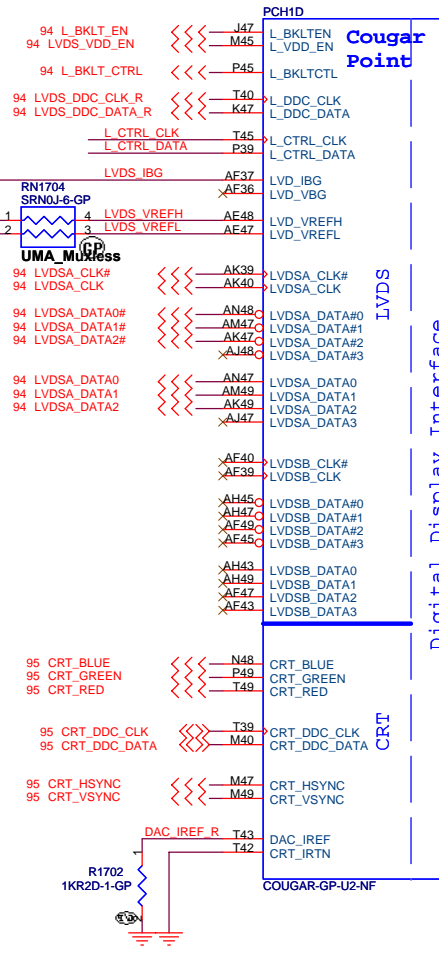
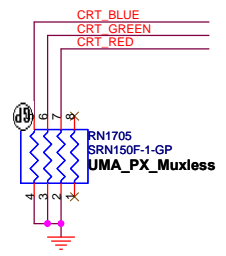
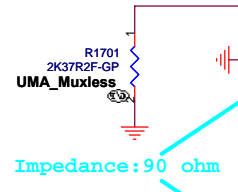


DM2  
DDR3-204P-126-GP  
**62.10024.D41**  
  
2nd = 62.10017.R91  
3rd = 62.10017.V61  
4th = 62.10017.X51

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**L\_DDC\_DATA(PAGE17):**  
 This signal is on the LVDS interface.  
 This signal needs to be left NC if eDP is  
 used for the local flat panel display



**Configuration Pin Mapping for DDI Ports (Sheet 1 of 2)**

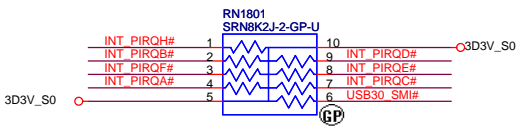
PORT	DDI PCH Pin Names	SDVO Mapping	Display Port Mapping	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	SDVO_RED	DDPB_[0]P	TMDSB_DATA2
	DDPB_[0]N	SDVO_RED#	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	SDVO_GREEN	DDPB_[1]P	TMDSB_DATA1
	DDPB_[1]N	SDVO_GREEN#	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	SDVO_BLUE	DDPB_[2]P	TMDSB_DATA0
	DDPB_[2]N	SDVO_BLUE#	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	SDVO_CLK	DDPB_[3]P	TMDSB_CLK
	DDPB_[3]N	SDVO_CLK#	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXP	NA	DDPB_AUXP	NA
	DDPB_AUXN	NA	DDPB_AUXN	NA
SDVO_CTRLCLK	SDVO_CTRLCLK	NA	HDMI_CTRLCLK	
SDVO_CTRLDATA	SDVO_CTRLDATA	NA	HDMI_CTRLDATA	

Title: \_\_\_\_\_

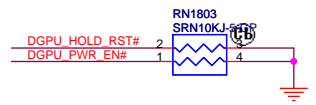
Size: \_\_\_\_\_ Document Number: \_\_\_\_\_ Rev: \_\_\_\_\_

Date: \_\_\_\_\_ Sheet: \_\_\_\_\_

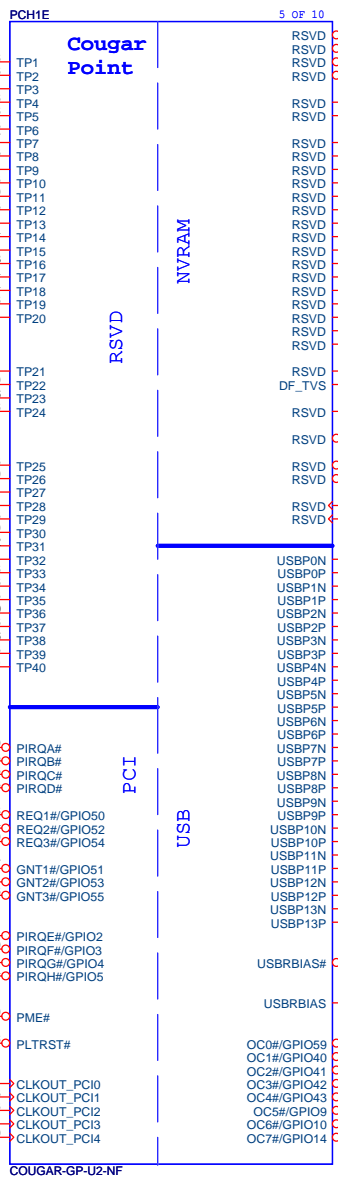
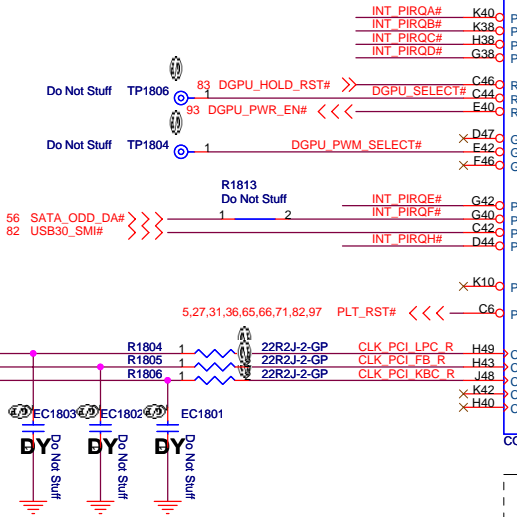
# SSID = PCH



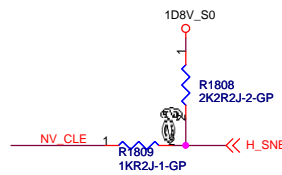
Al6 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = Al6 swap override/Top-Block Swap Override enabled High = Default



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
		<b>SPI(Default)</b>



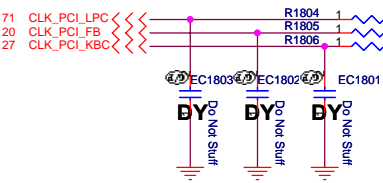
DMI & FDI Termination Voltage	
NV_CLE	Set to Vss when LOW
	Set to Vcc when HIGH



USB Ext. port 1 (HS)  
External debug port use on Huron river platform

## USB Table

Pair	Device
0	Touch Panel / 3G SIM
1	USB Ext. port 1 (HS)
2	Fingerprint
3	BLUETOOTH
4	Mini Card2 (WWAN)
5	CARD READER(DY)
6	X
7	X
8	USB Ext. port 4 / E-SATA / USB CHARGER
9	USB Ext. port 2
10	EDP CAMERA
11	Mini Card1 (WLAN)
12	CAMERA
13	New Card



OC[3:0]# for Device 29 (Ports 0-7)  
OC[7:4]# for Device 26 (Ports 8-13)

## USB 2.0 Overcurrent Pin Default Usage

Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

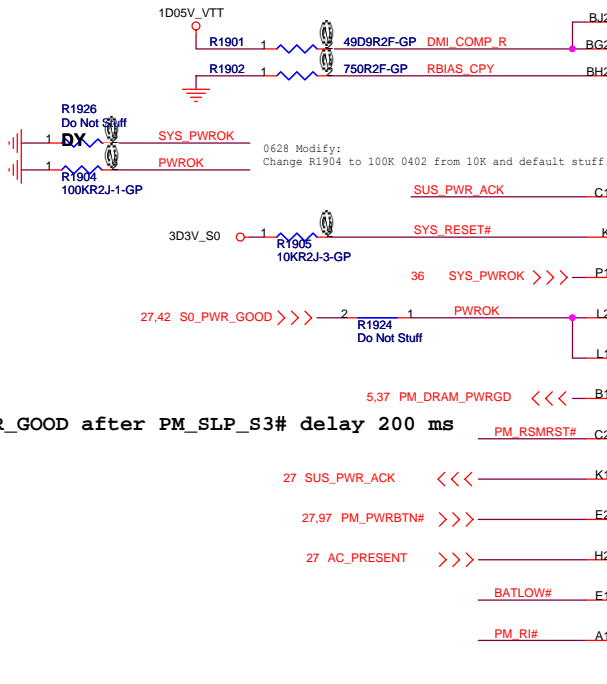
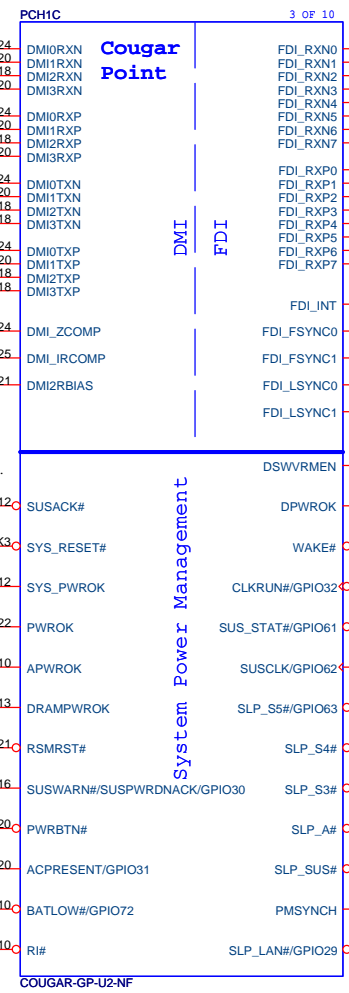
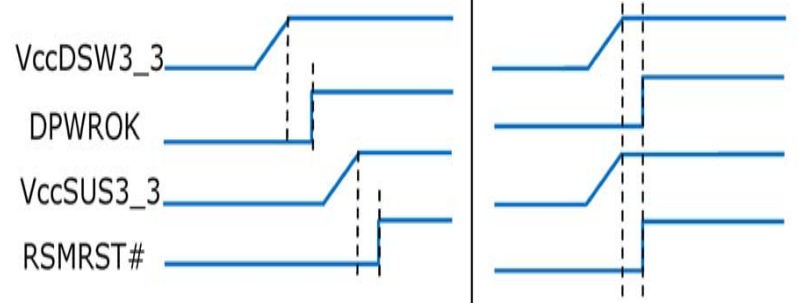
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Size	Document Number	Rev
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**SSID = PCH**



Deep S4/S5 Supported

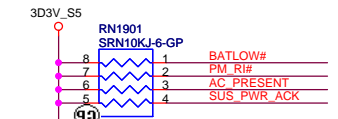
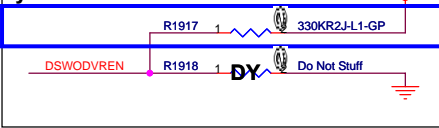
Deep S4/S5 Not Supported



S0\_PWR\_GOOD after PM\_SLP\_S3# delay 200 ms

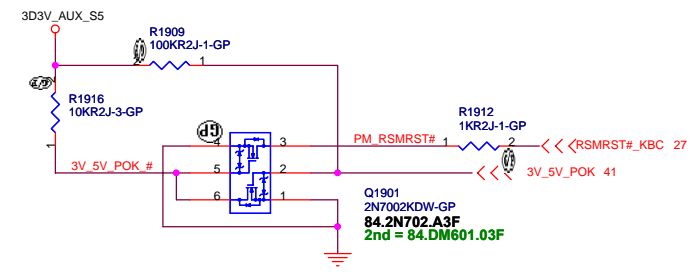
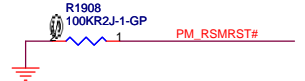
DSWODVREN - On Die DSW VR Enable	
HIGH	Enabled (DEFAULT)
LOW	Disabled

SB modify

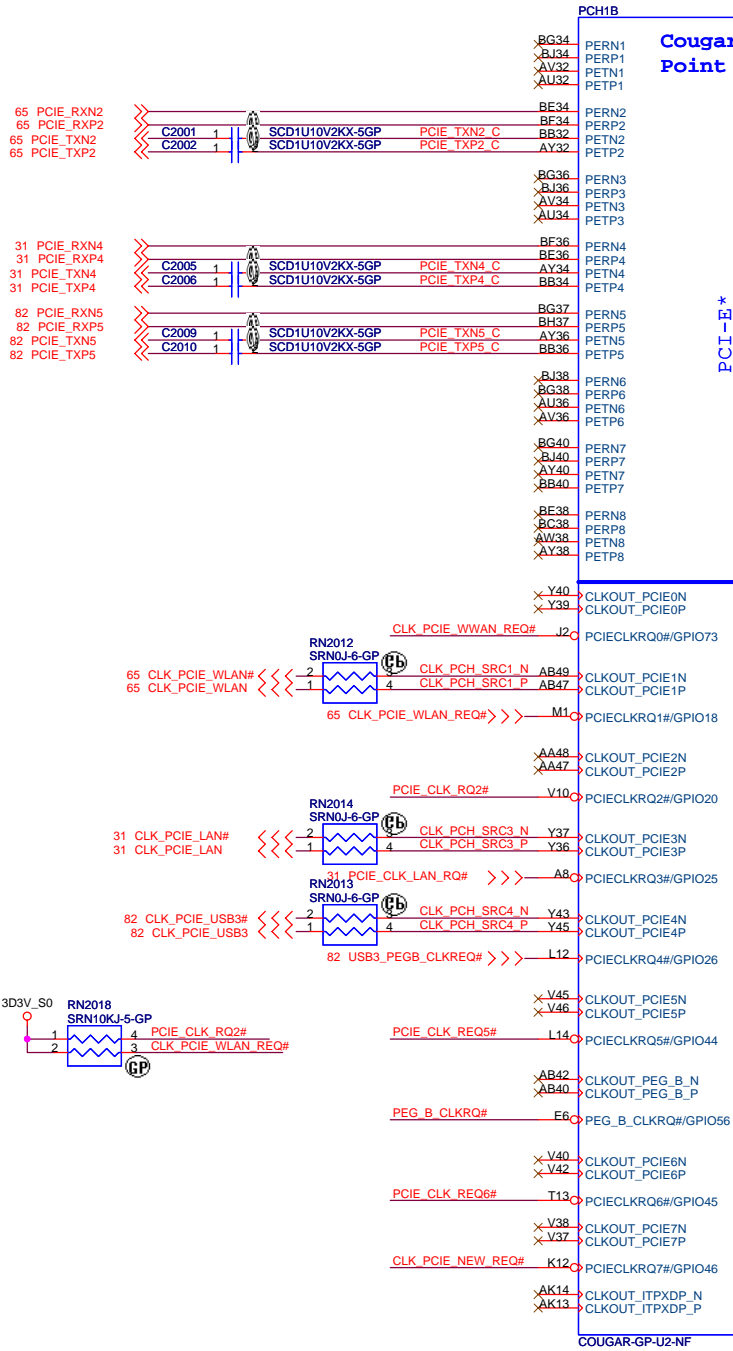


**PCIE\_WAKE#**  
CRB : 1k  
CEKLT: 10K

**PWRBTN#**  
This signal has an internal pull-up resistor



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65 PCIE\_RXN2  
65 PCIE\_RXP2  
65 PCIE\_TXN2  
65 PCIE\_TXP2

31 PCIE\_RXN4  
31 PCIE\_RXP4  
31 PCIE\_TXN4  
31 PCIE\_TXP4

82 PCIE\_RXN5  
82 PCIE\_RXP5  
82 PCIE\_TXN5  
82 PCIE\_TXP5

65 CLK\_PCIE\_WLAN#  
65 CLK\_PCIE\_WLAN

31 CLK\_PCIE\_LAN#  
31 CLK\_PCIE\_LAN

82 CLK\_PCIE\_USB3#  
82 CLK\_PCIE\_USB3

PCIE\_CLK\_REQ2#  
CLK\_PCIE\_WLAN\_REQ#

CLK\_PCIE\_NEW\_REQ#

SMBUS

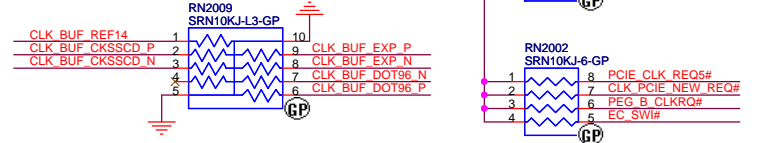
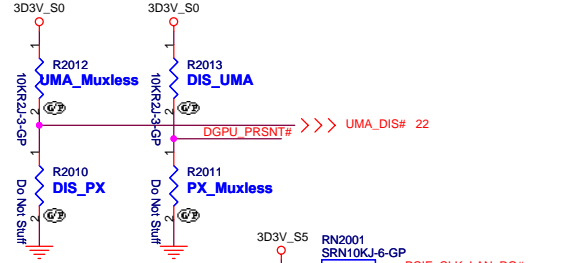
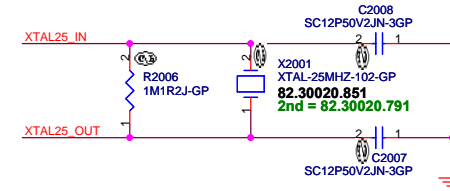
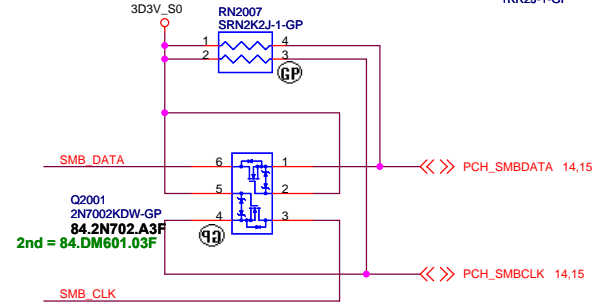
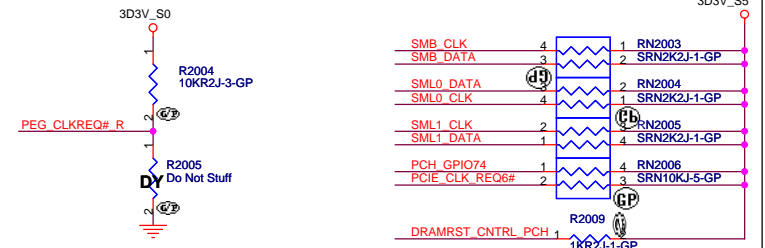
Controller Link

CLOCKS

FLEX CLOCKS

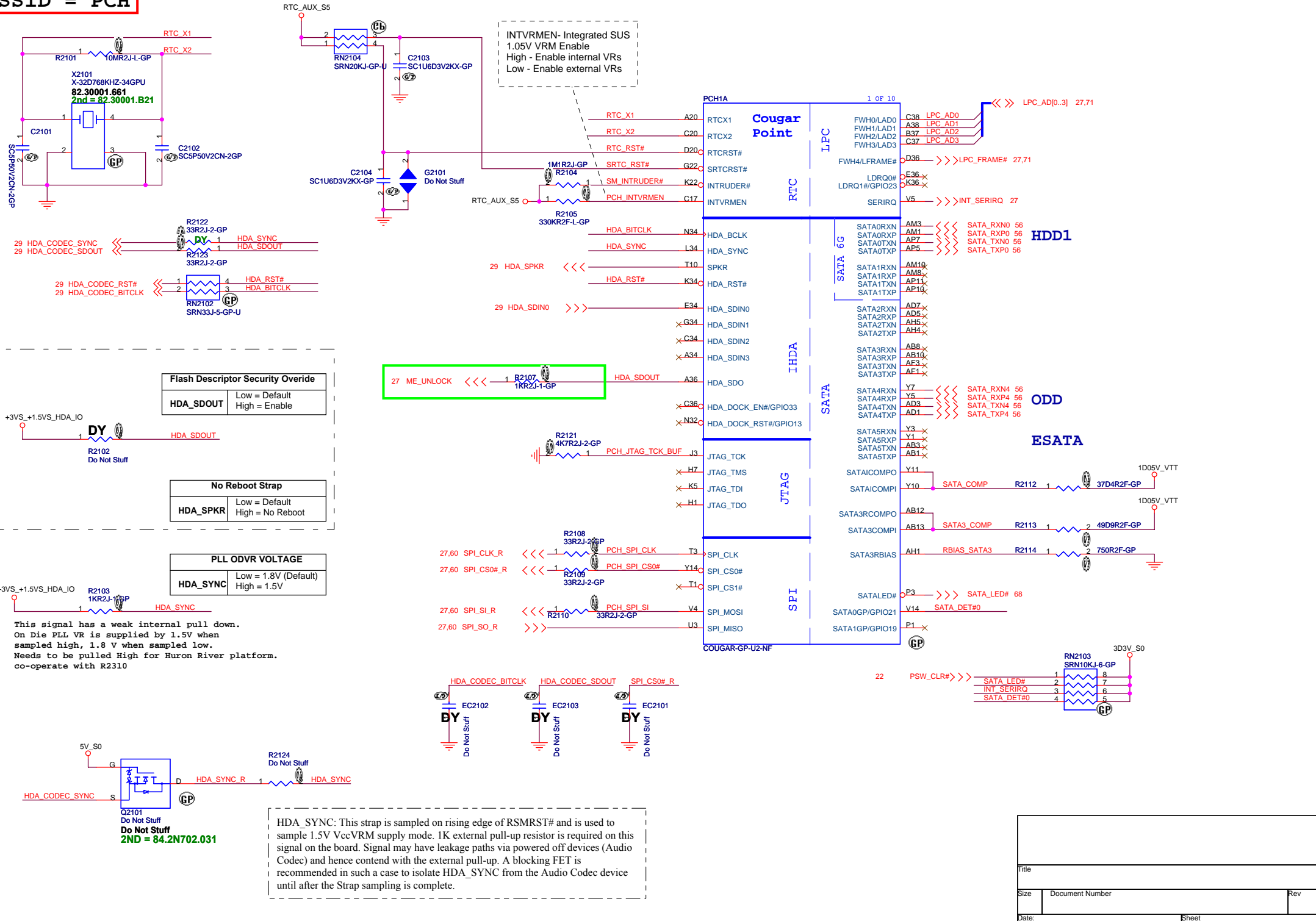
PCI-E\*

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**SSID = PCH**



**Flash Descriptor Security Override**

HDA_SDOUT	Low = Default High = Enable
-----------	--------------------------------

**No Reboot Strap**

HDA_SPKR	Low = Default High = No Reboot
----------	-----------------------------------

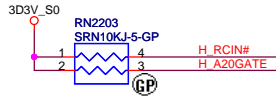
**PLL ODVR VOLTAGE**

HDA_SYNC	Low = 1.8V (Default) High = 1.5V
----------	-------------------------------------

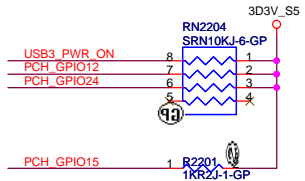
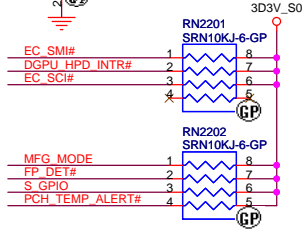
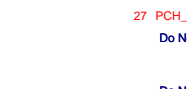
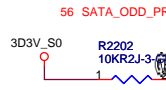
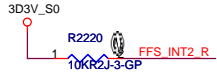
HDA\_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA\_SYNC from the Audio Codec device until after the Strap sampling is complete.

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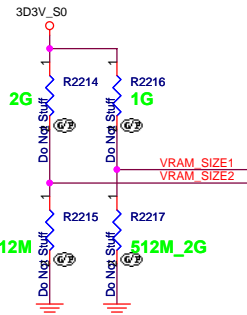
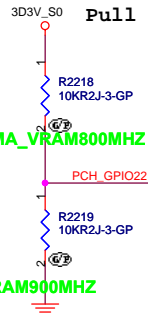




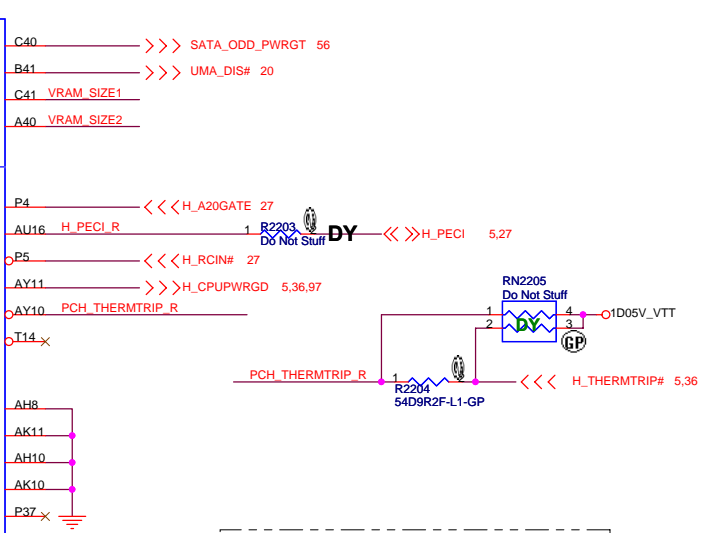
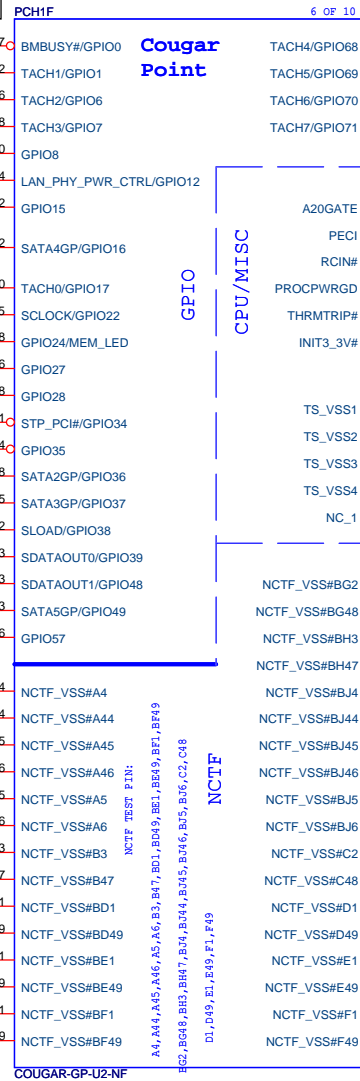
Note:  
For PCH debug with XDP, need to NO STUFF R2218



VRAM Frequency  
Pull high: 800MHZ  
Pull low :900MHZ



PLL ON DIE VR ENABLE  
NOTE: This signal has a weak internal pull-up 20K  
ENABLED -- HIGH (R2212 UNSTUFFED) DEFAULT  
DISABLED -- LOW (R2212 STUFFED)



TS Signal Disable Guideline:  
TS\_VSS1, TS\_VSS2, TS\_VSS3 and TS\_VSS4  
should not float on the motherboard. They should  
be tied to GND directly.

FDI TERMINATION VOLTAGE OVERRIDE	
GPIO37 (FDI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

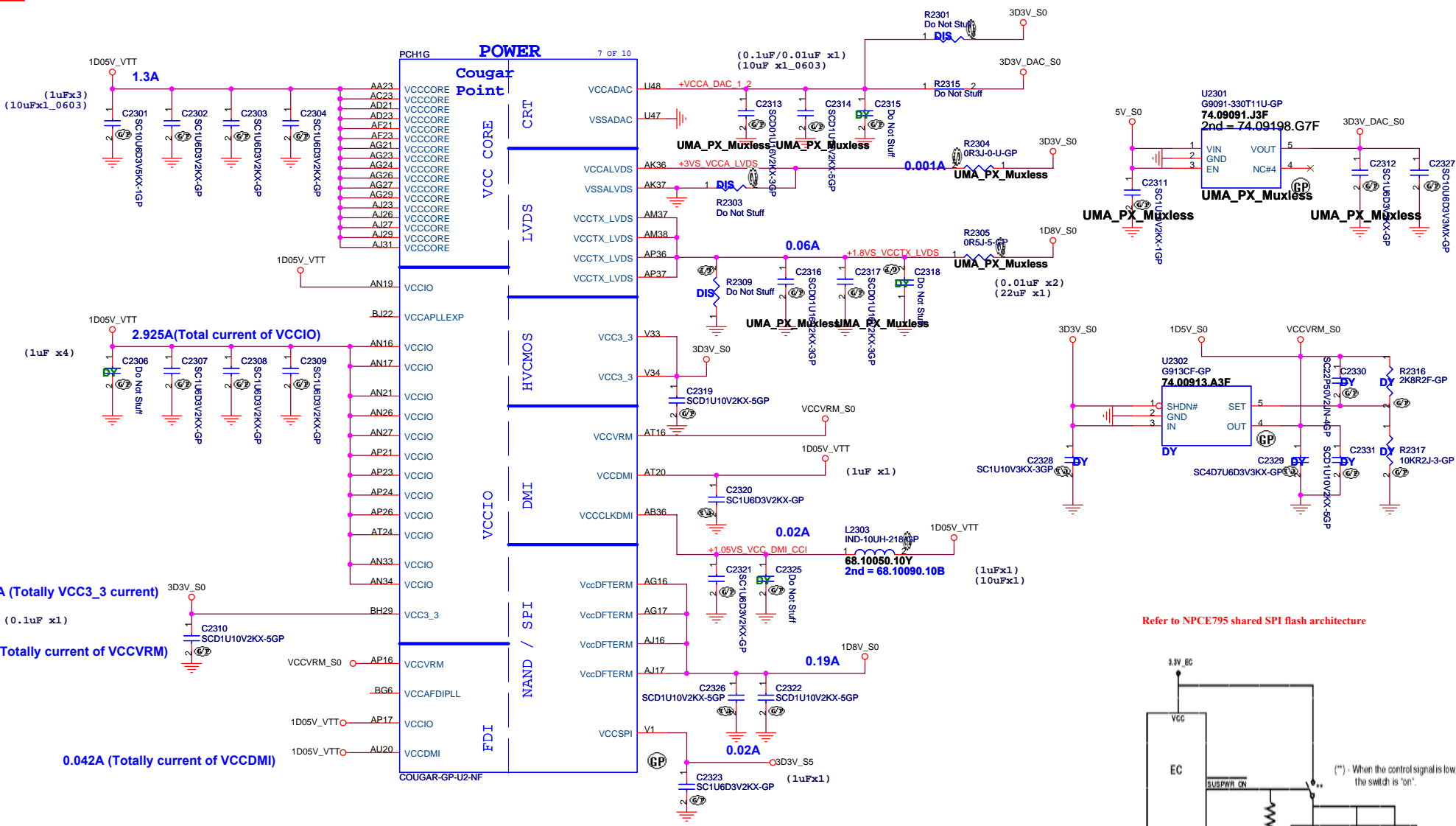
DMI TERMINATION VOLTAGE OVERRIDE	
GPIO36 (DMI_OVRVLTG)	LOW - Tx, Rx terminated to same voltage (DC Coupling Model DEFAULT)

Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

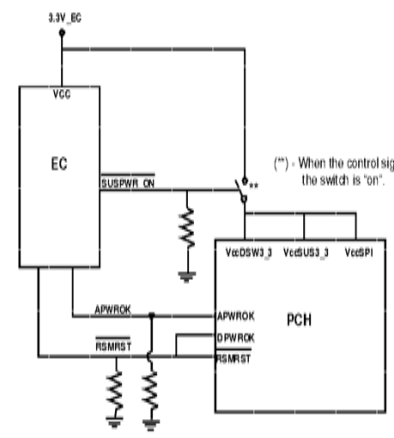
Integrated Clock Chip Enable	
ICC_EN#	HIGH (R2211 DY) - DISABLED [DEFAULT]
	LOW (R2211) - ENABLED

GPIO8 has a weak[20K] internal pull up.  
Integrated Clock Enable functionality is achieved via soft-strap. The default is integrated clock enable.

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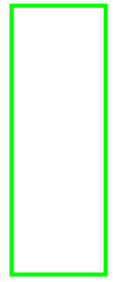


Refer to NPCE795 shared SPI flash architecture



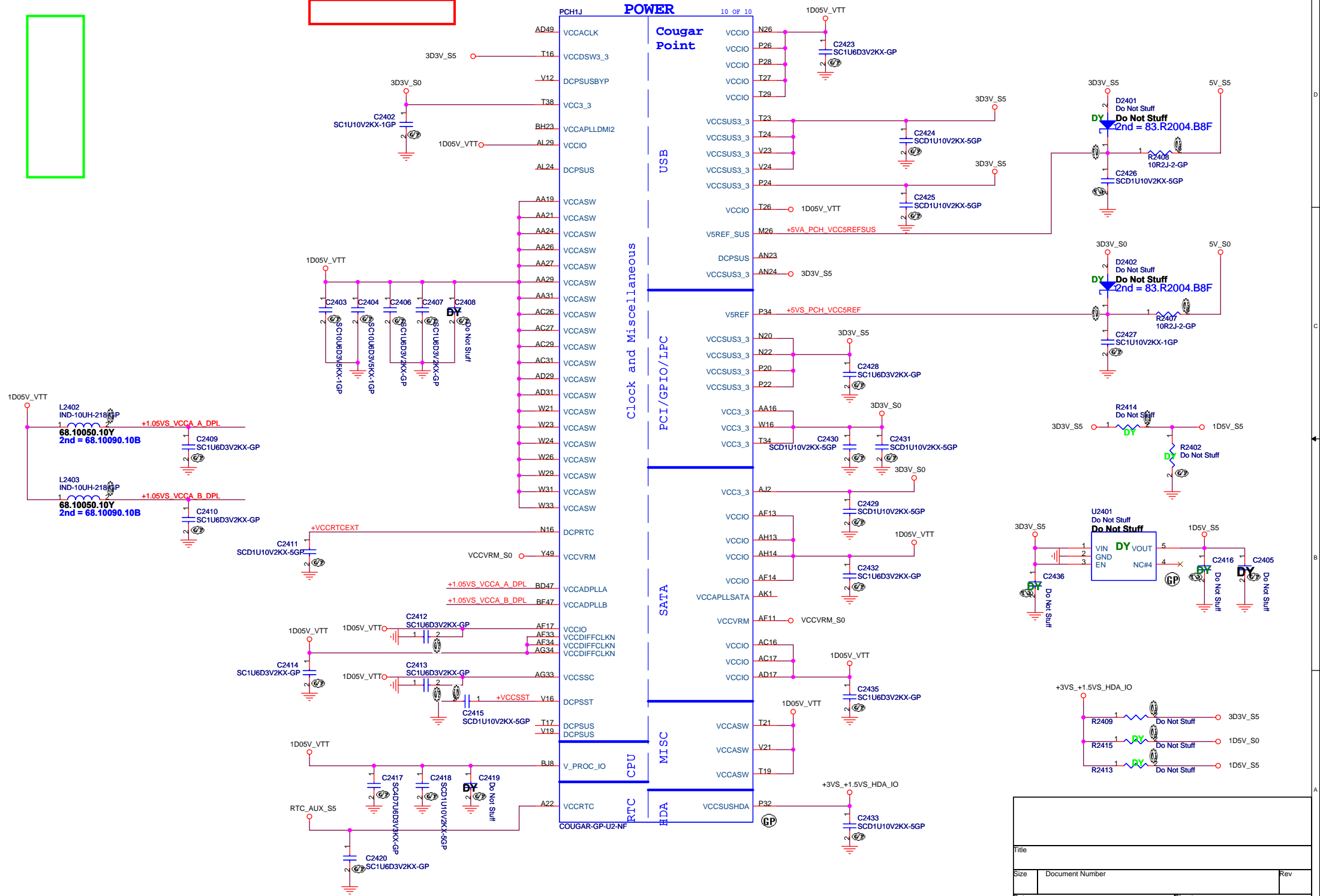
(\*) - When the control signal is low, the switch is 'on'.

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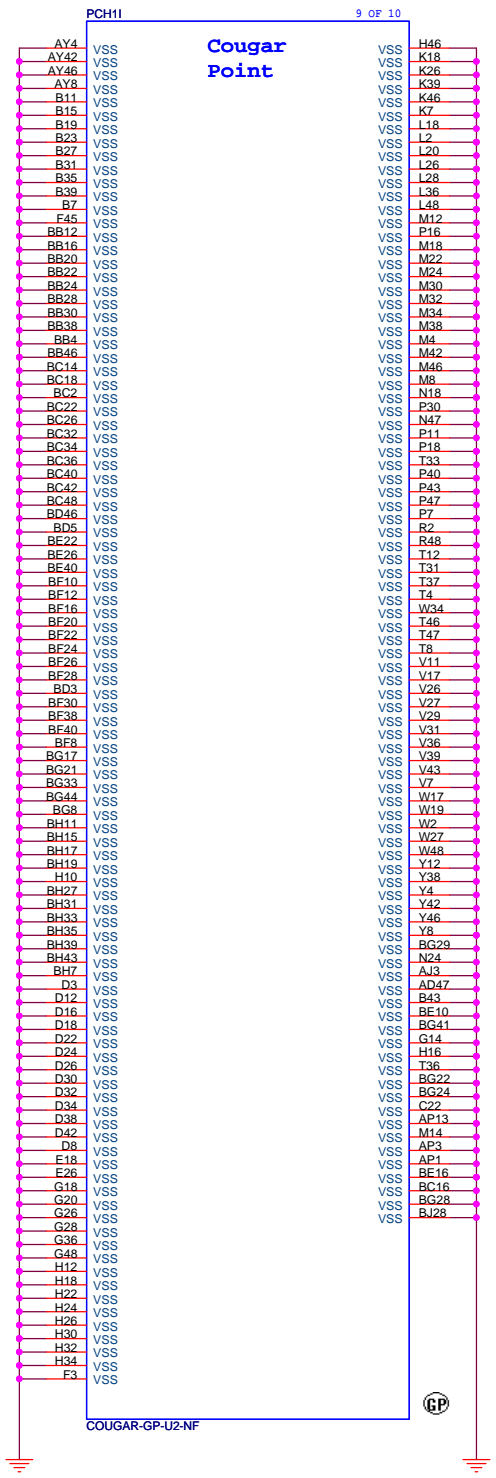
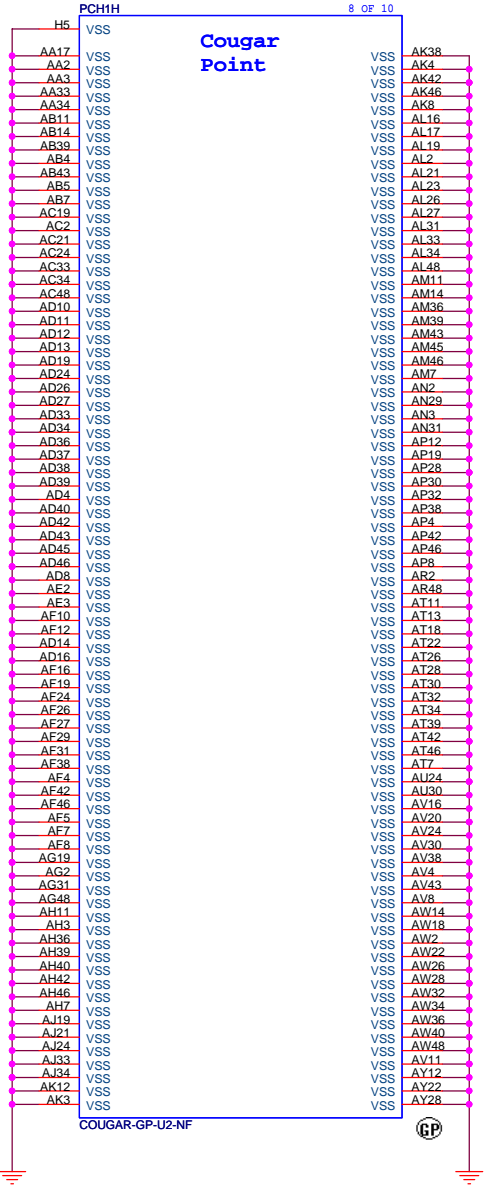


# POWER

## Cougar Point

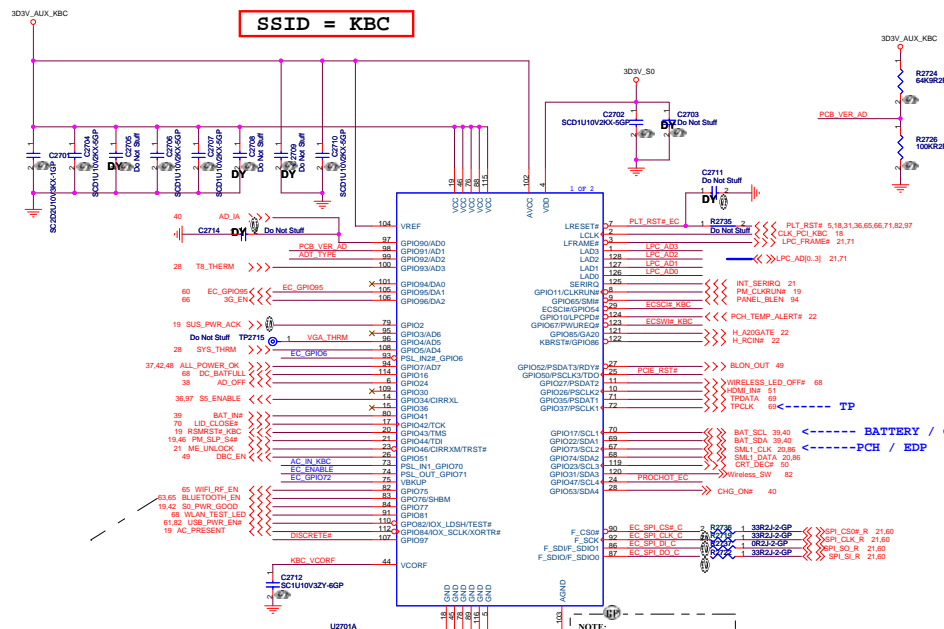


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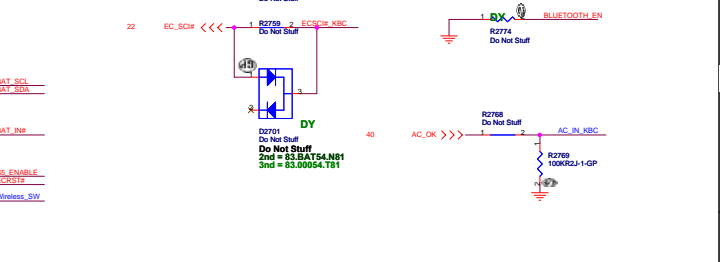
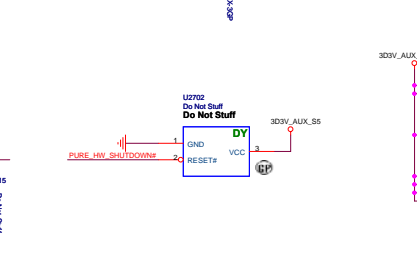
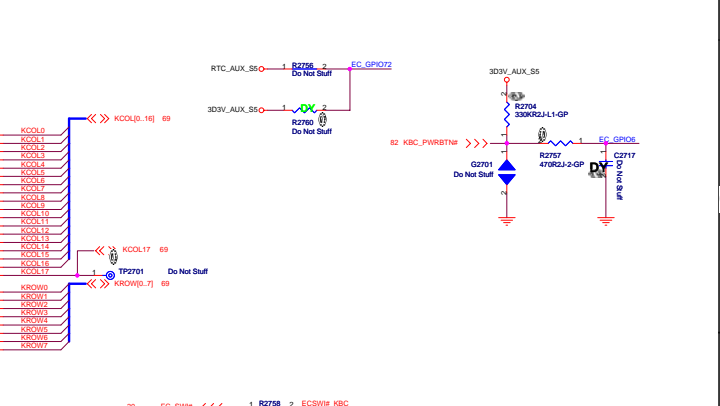
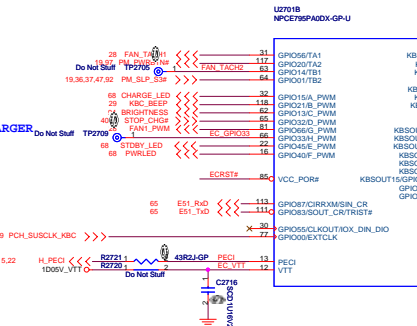
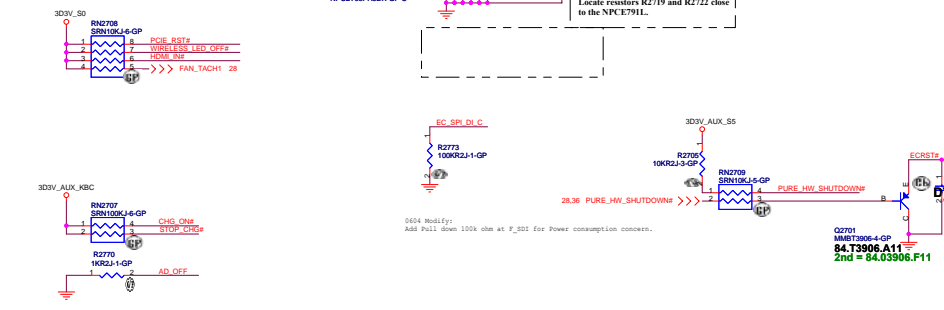
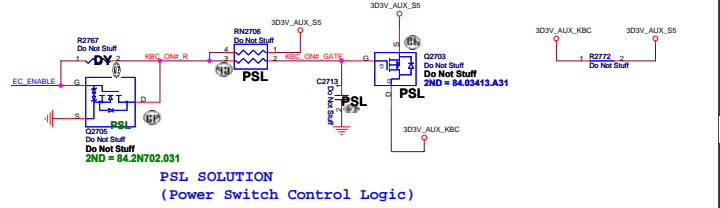


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SSID = KBC



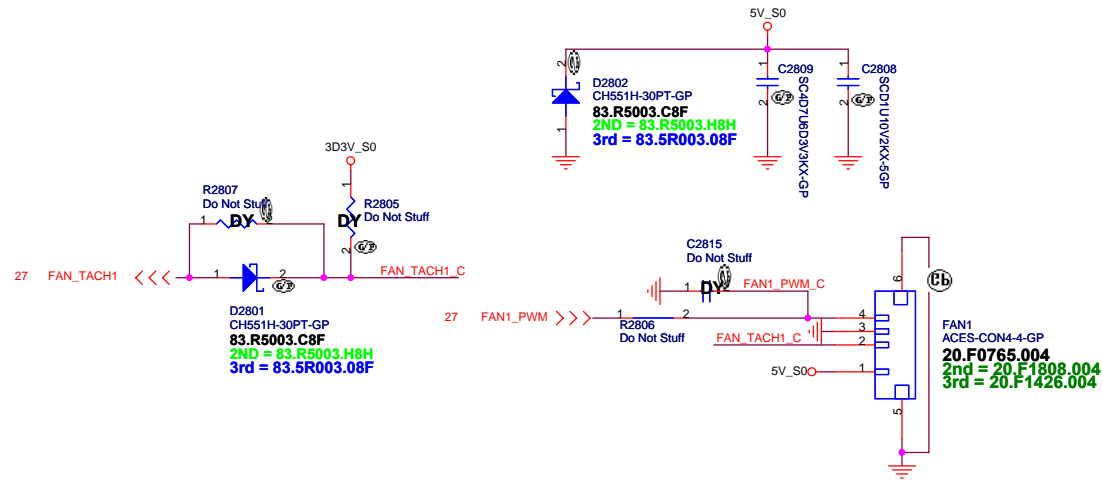
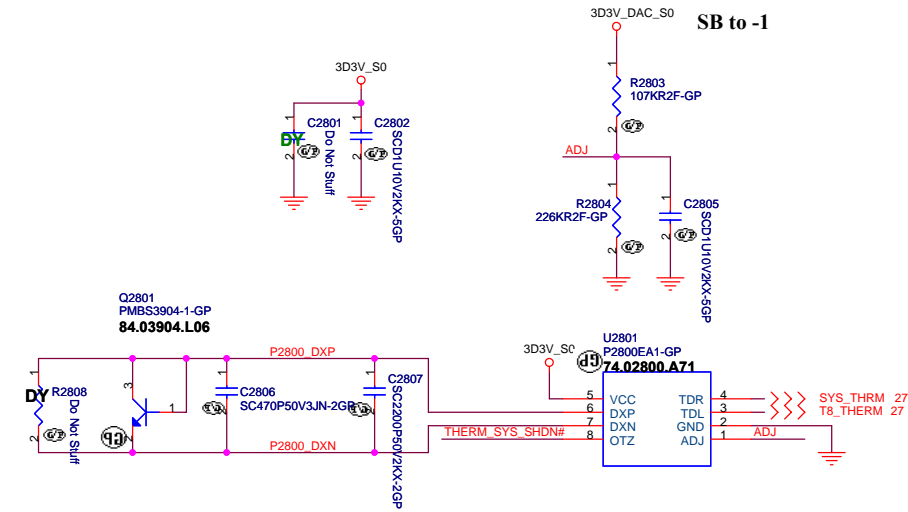
PCB VERSION A/D(PIN#)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
SA	100.0K		3.0V
SB			2.75V
Reserved		47.0K	
Reserved		64.9K	
Reserved		76.8	
Reserved			1.65V



ADT_TYPE A/D(PIN#)	PULL-LOW RESISTOR	PULL-HIGH RESISTOR	VOLTAGE
65W	N/A	100.0K	3.3V
90W	100.0K	N/A	0V
30W	10.0K	100.0K	0.3V
40W	20.0K		0.55V
120W	33.0K		0.82V
Reserved	47.0K		
Reserved	64.9K	100.0K	1.65V

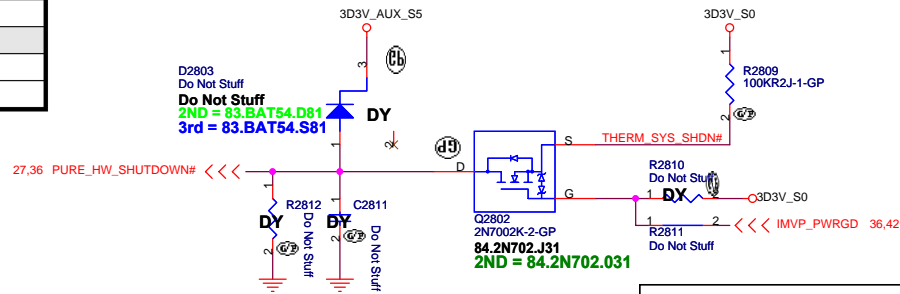
65W 90W#  
High: 65W / Low 90W  
DISCRETE#  
High: UNA / Low: Discrete

File	Doc Number	Rev

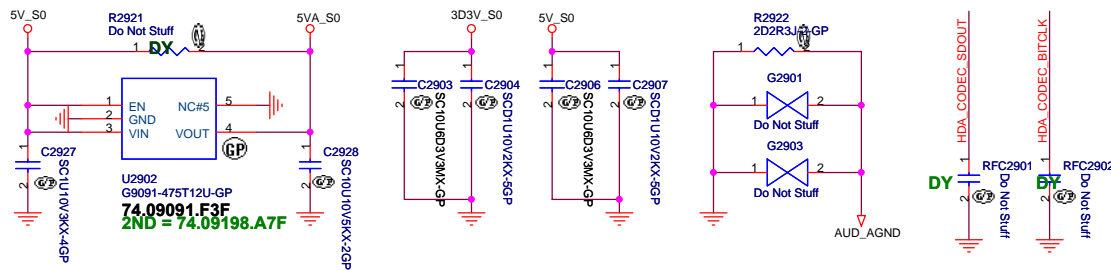


ADJ Table (Reference to SYNTON-TECH Metal Film Resistor E-96 ±1% Series)

RADJ1 (KΩ)	RADJ2 (KΩ)	VADJ (v)	OTZ Threshold Temperature (°C)
124	226	2.13	101
118	226	2.17	96.3
113	226	2.20	92.1
110	226	2.22	89.6
107	226	2.24	87
105	226	2.25	85.3
100	226	2.29	80.9

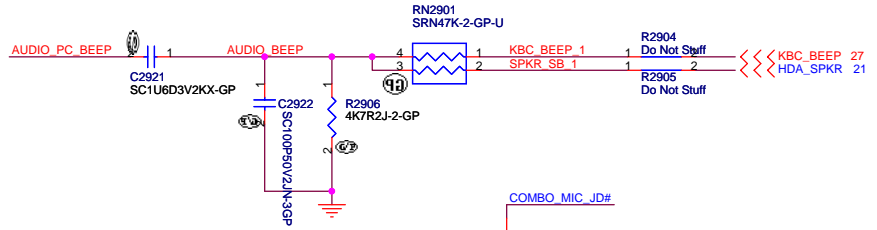
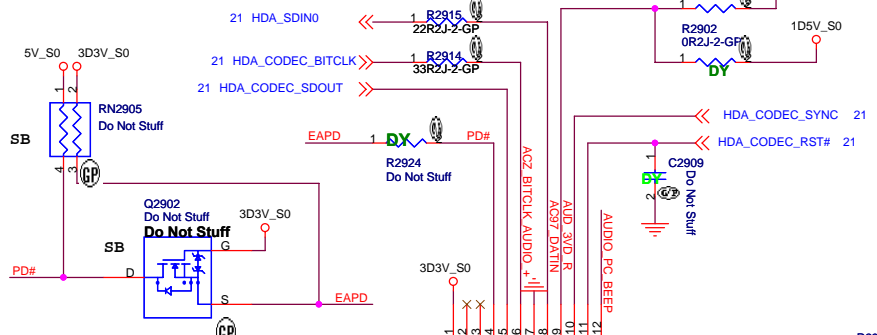


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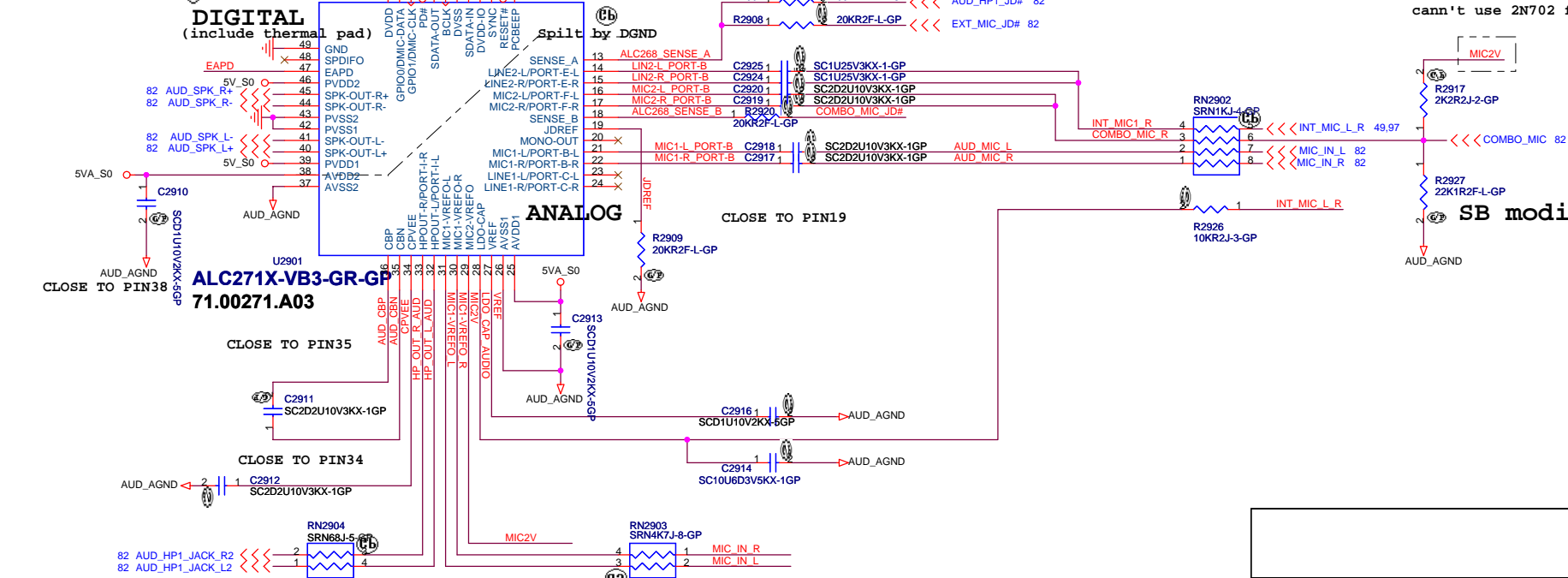


CLOSE TO PIN39 and 46

-1 PVDD timing 需要比 AVDD晚, 使用PW 74.00545.079 去開  
vensor suggest, 需要導入嗎

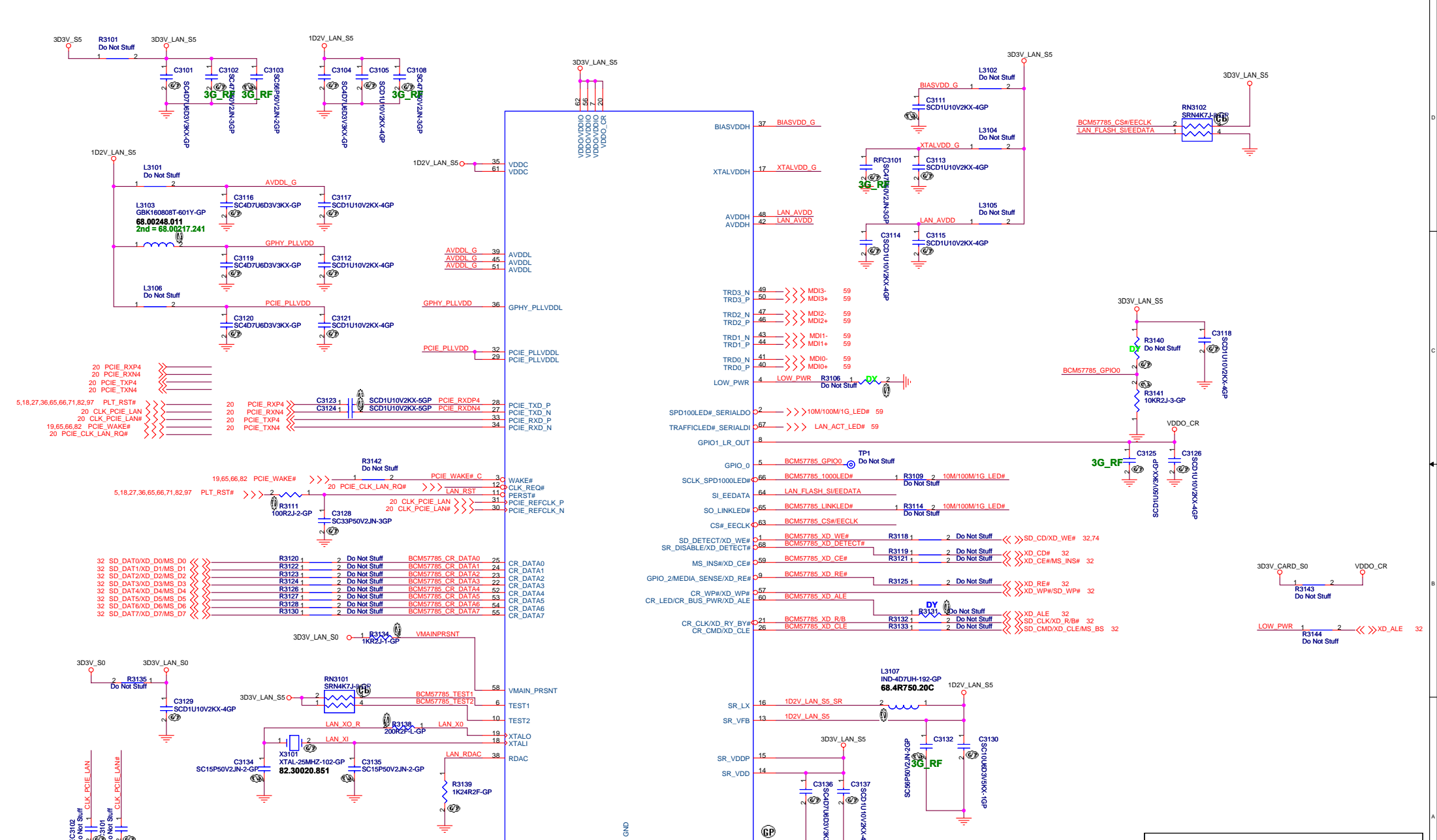


MIC2V Ref voltage is 2.5V because Vgs(th) concern can't use 2N702 for desing



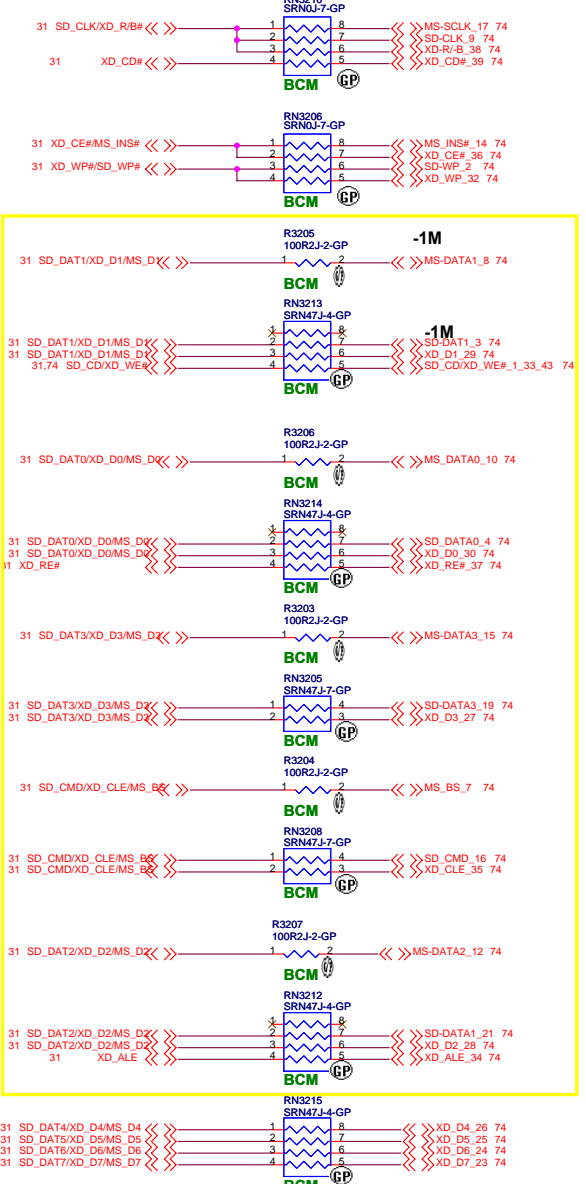
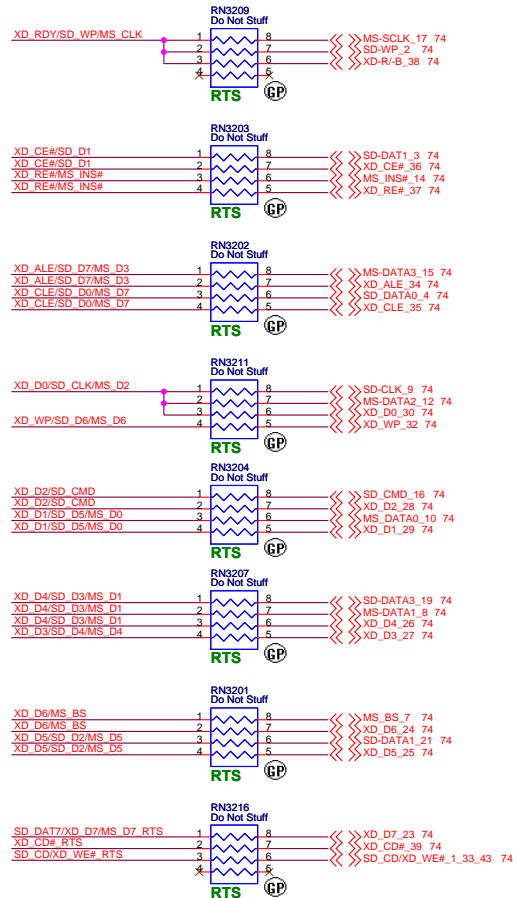
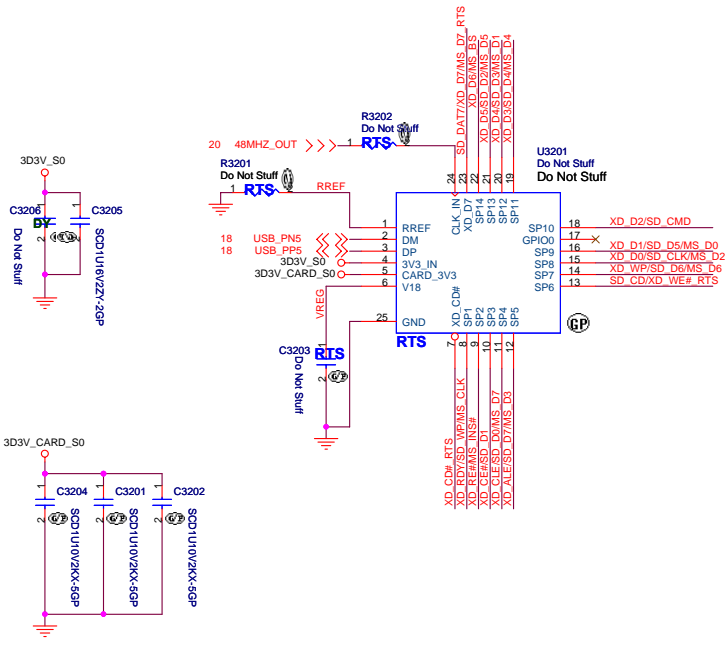
SB modify

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Title		
Size	Document Number	Rev
Date:	Sheet	

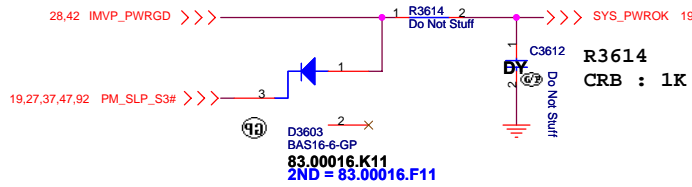




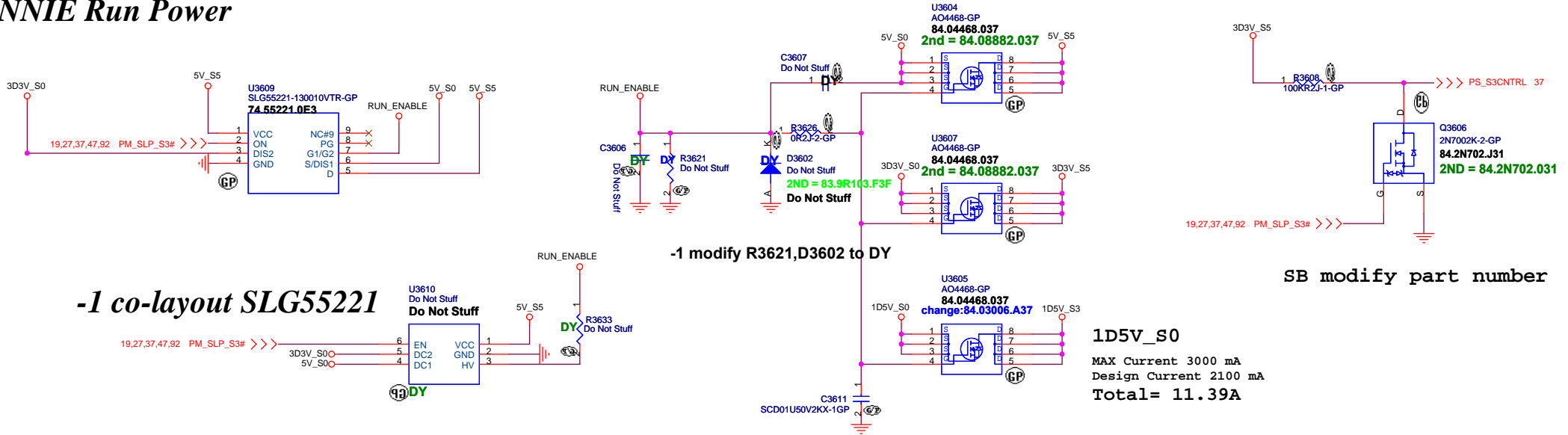
-1M

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# Power Sequence



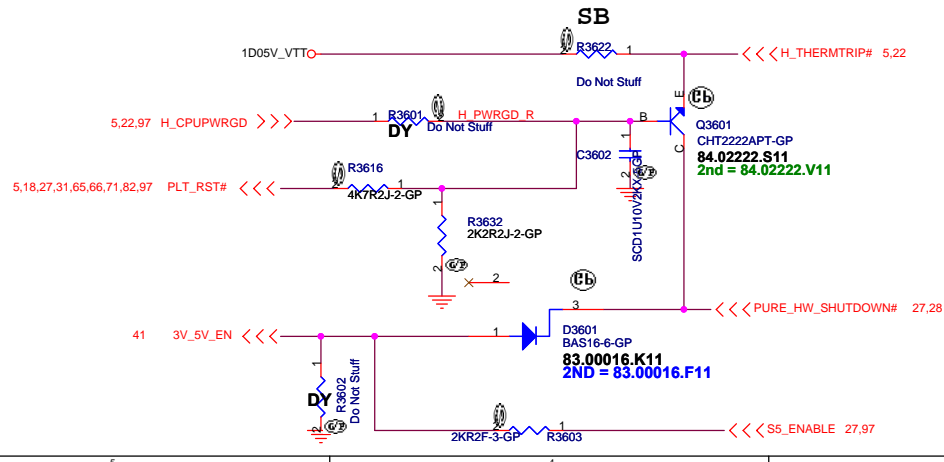
## ANNIE Run Power



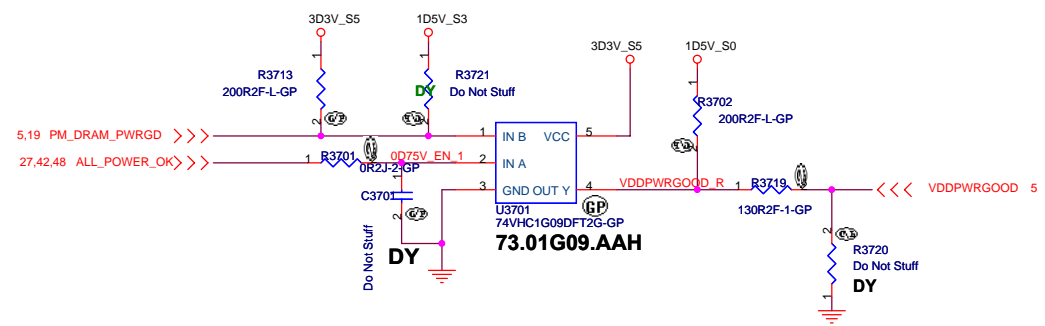
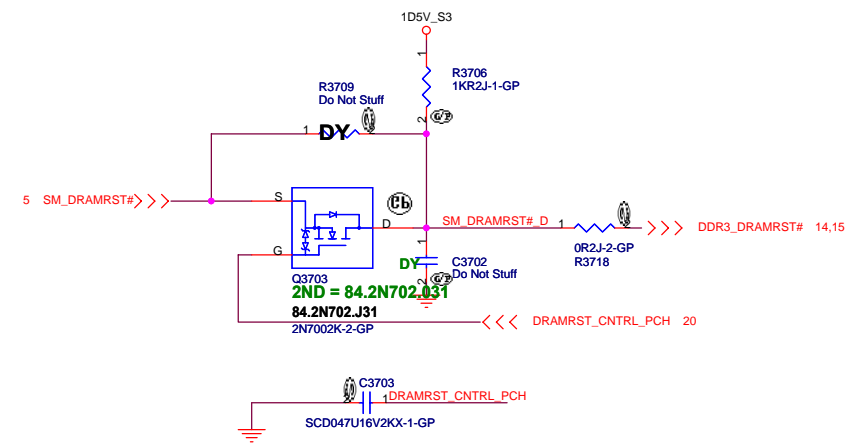
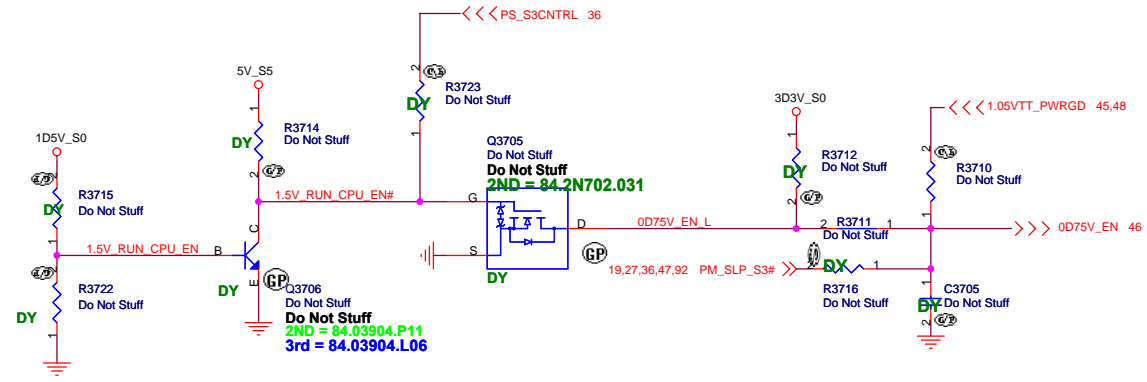
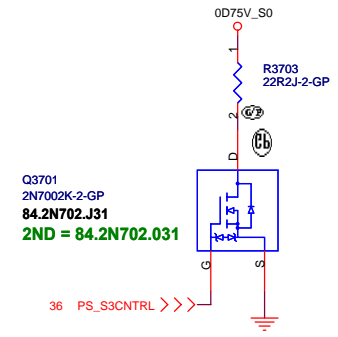
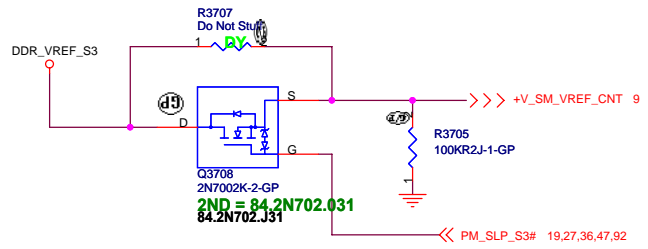
**-1 co-layout SLG55221**

**-1 modify R3621,D3602 to DY**

**SB modify part number**

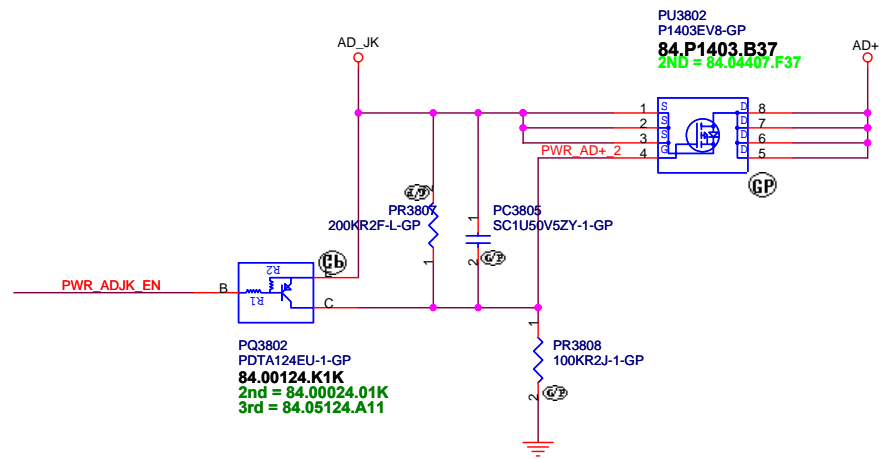
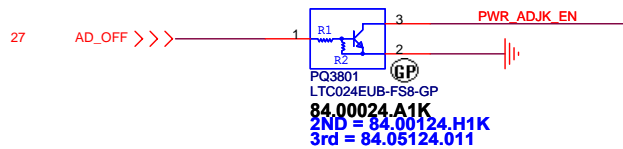
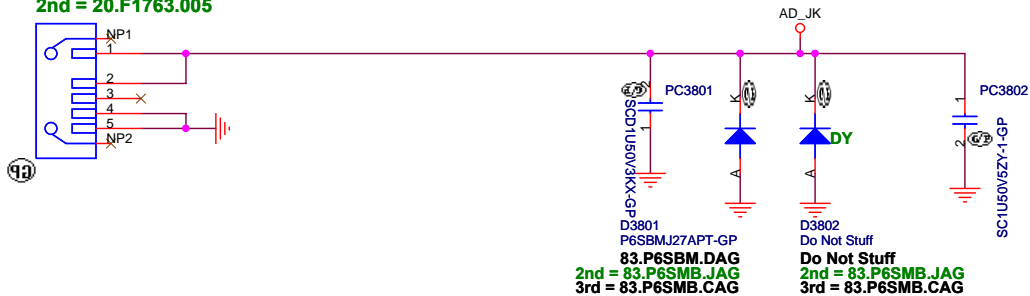


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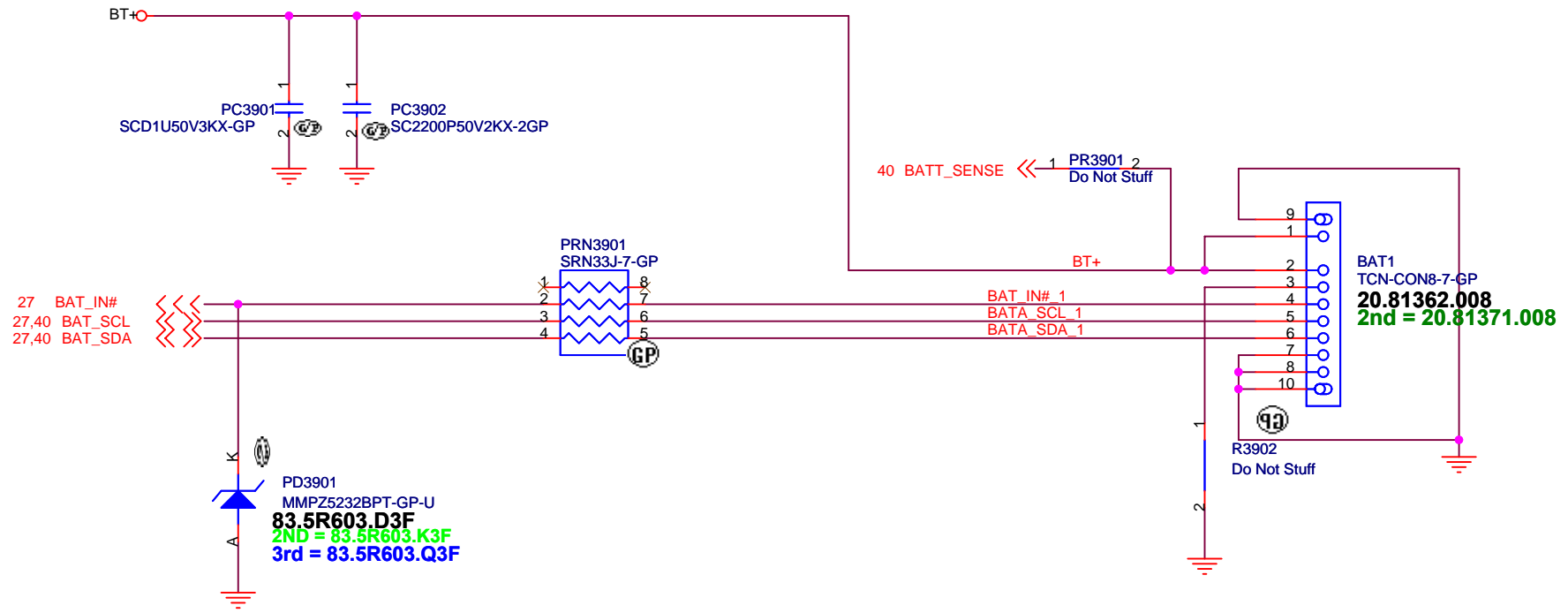


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DCIN1  
ACES-CON5-14-GP  
**20.F1701.005**  
2nd = 20.F1763.005

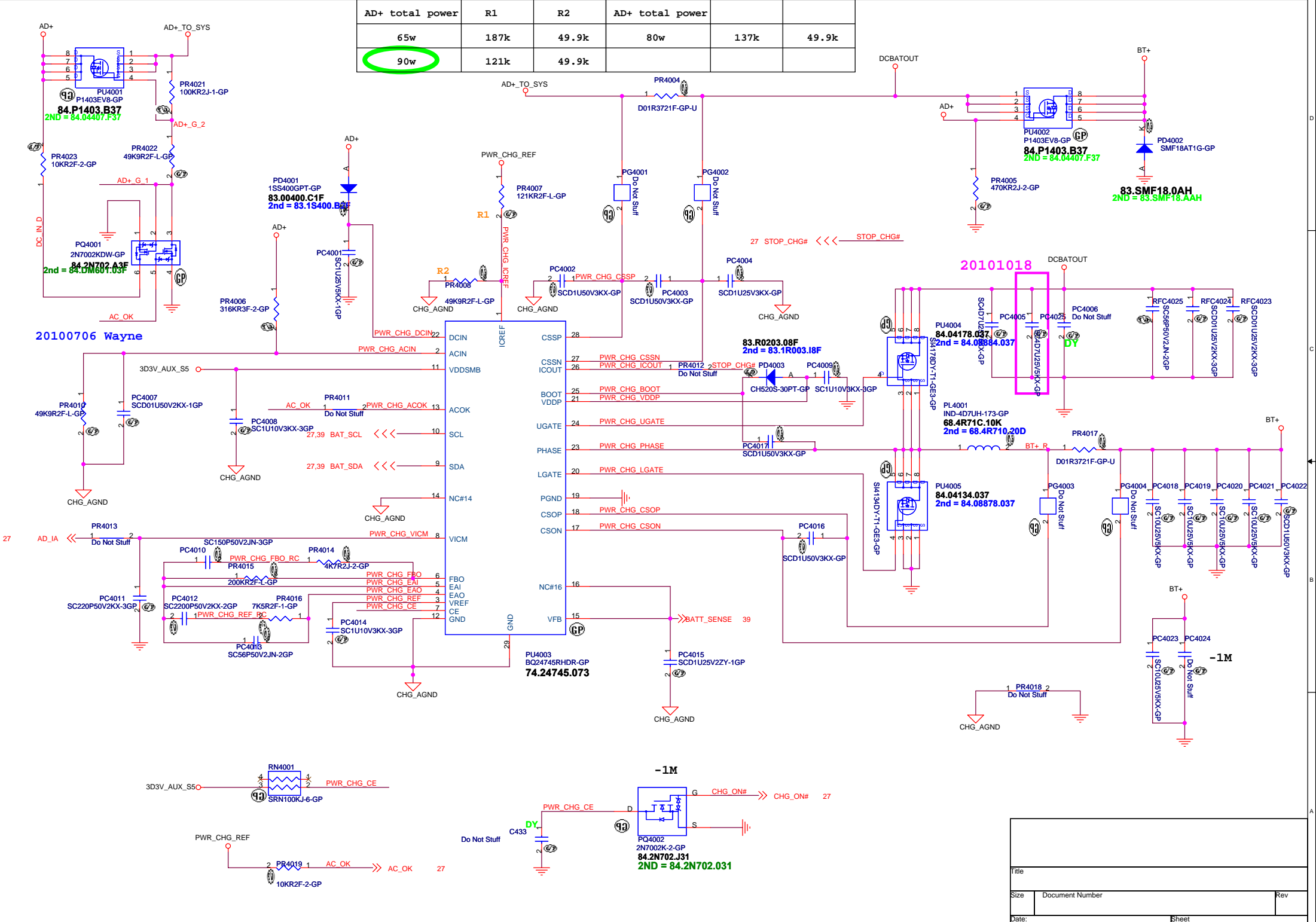


Title		
Size	Document Number	Rev
Date:	Sheet	

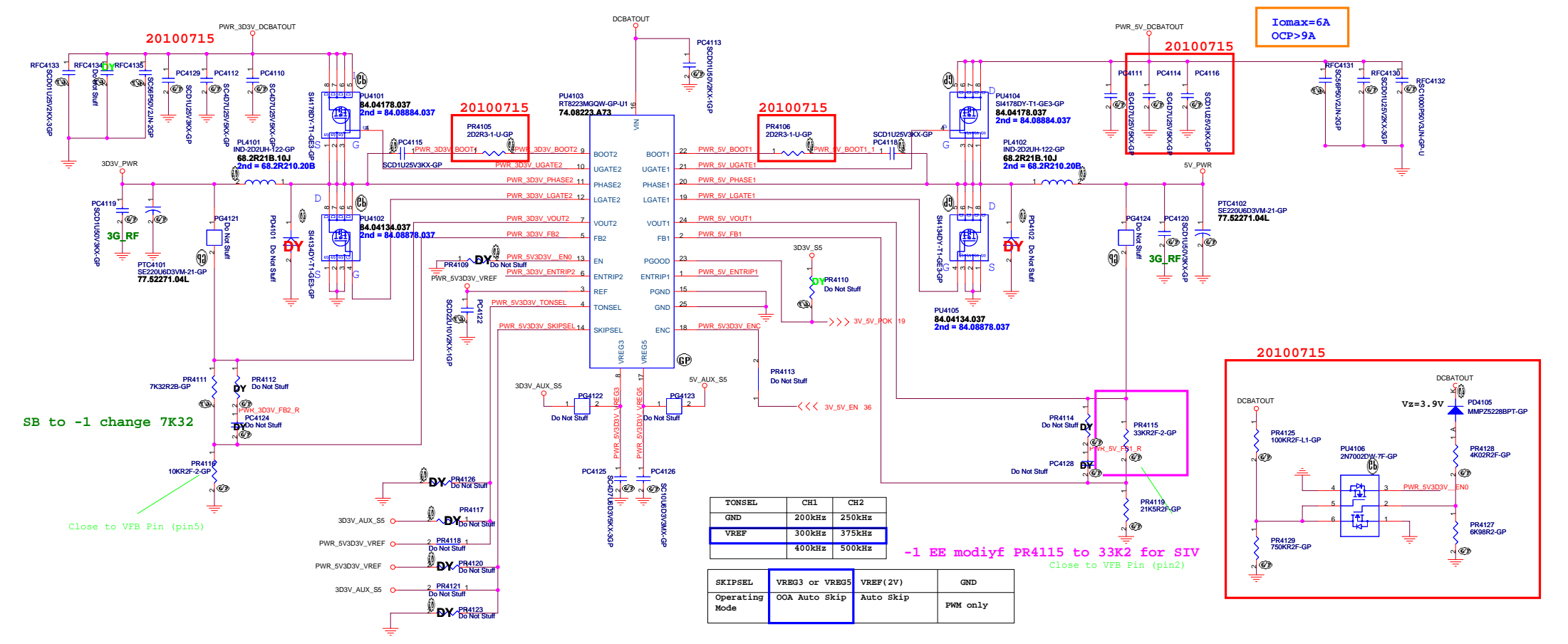
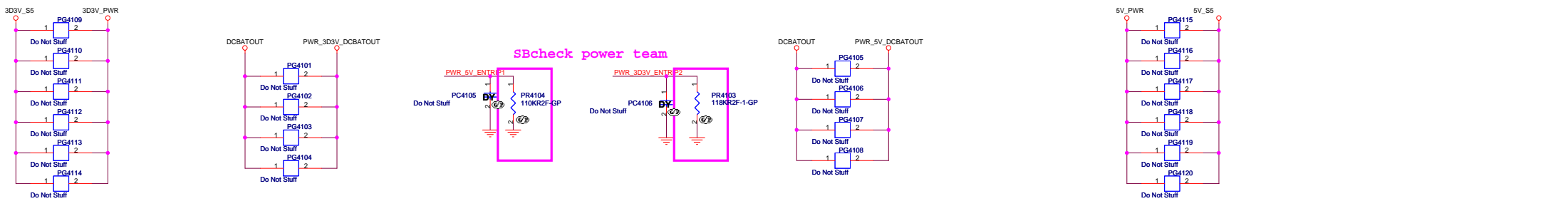


Title		
Size	Document Number	Rev
Date:	Sheet 1	

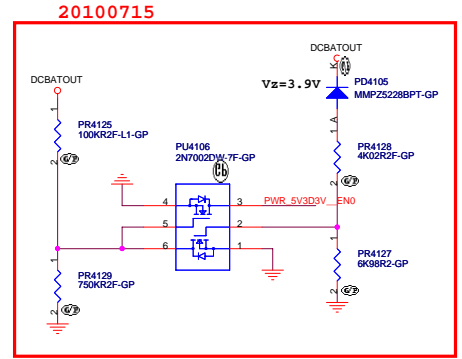
AD+ total power	R1	R2	AD+ total power		
65w	187k	49.9k	80w	137k	49.9k
<b>90w</b>	121k	49.9k			



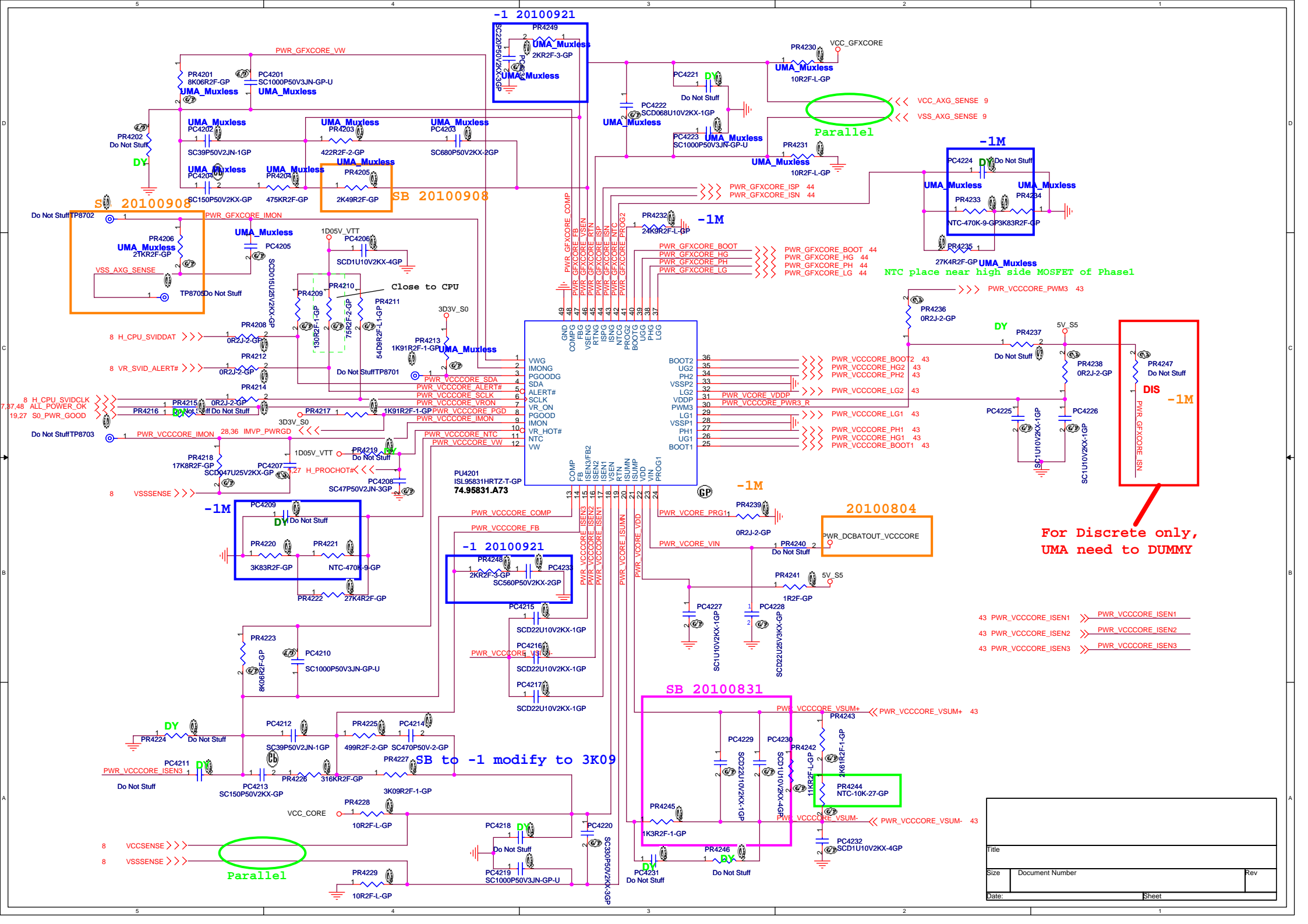
Title		
Size	Document Number	Rev
Date:	Sheet	



I<sub>max</sub>=6A  
OCP>9A



File		
Size	Document Number	Rev
Date:		Sheet

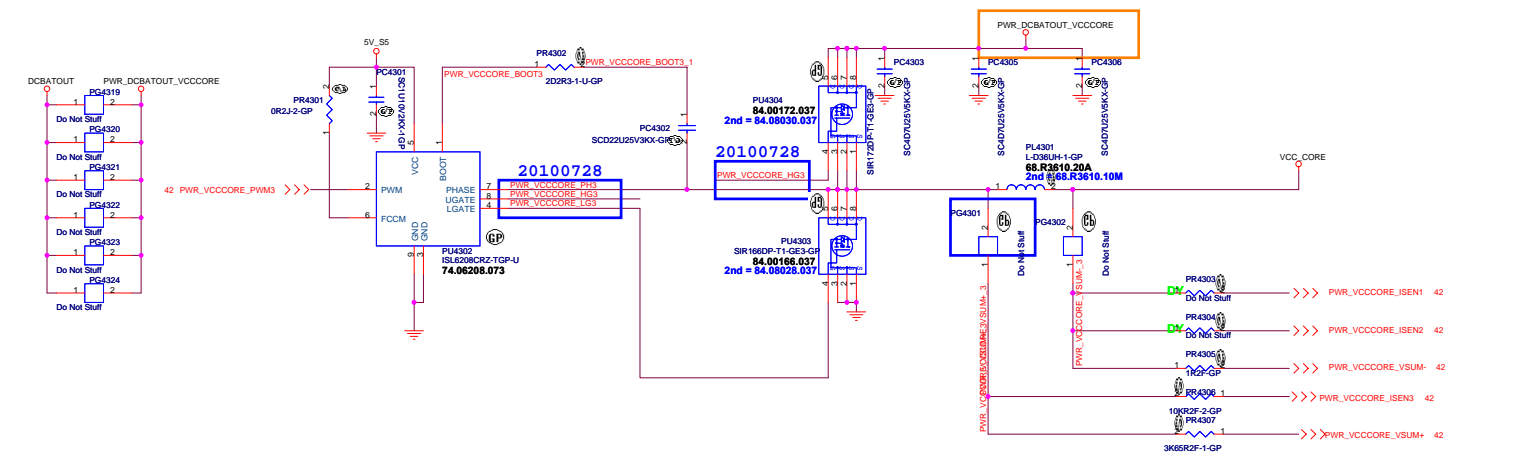
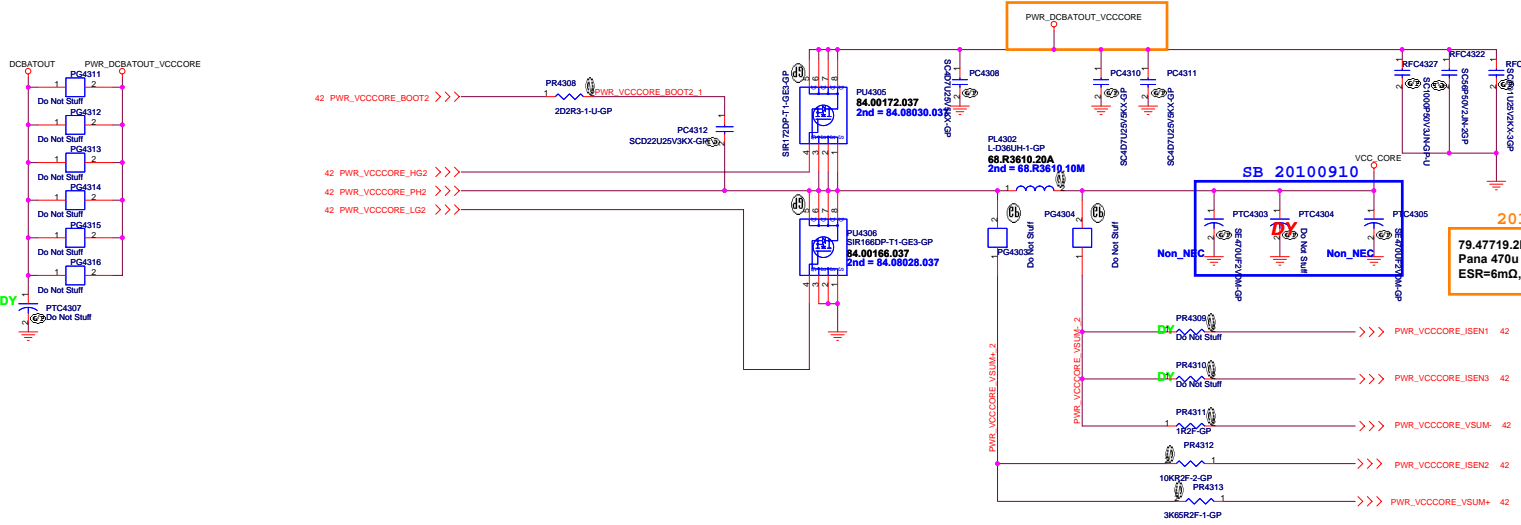
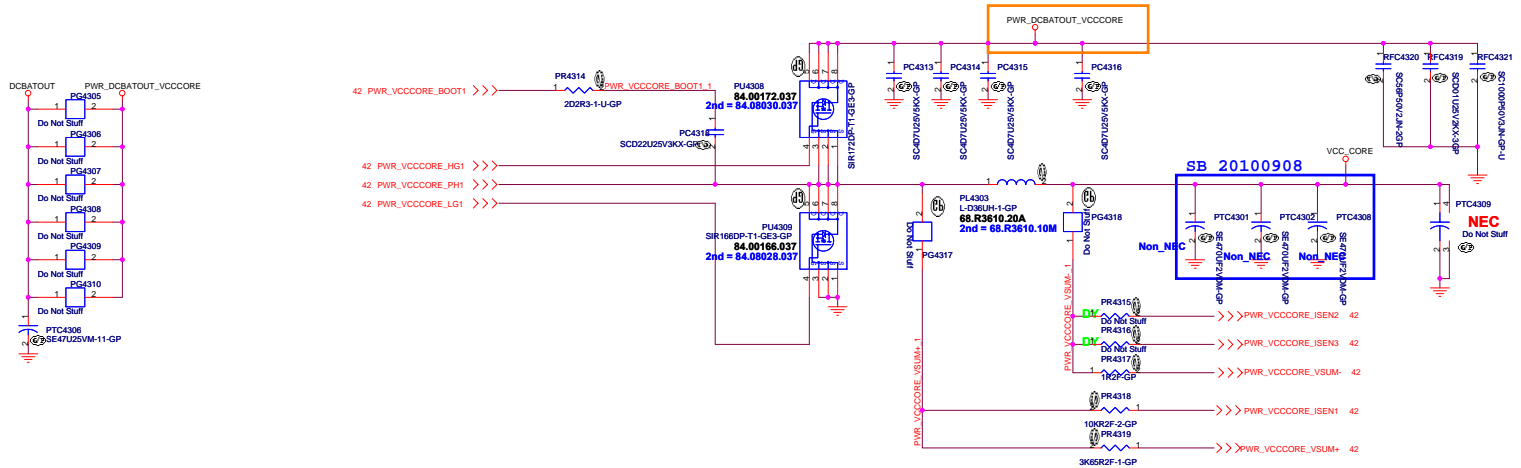


For Discrete only,  
UMA need to DUMMY

- 43 PWR\_VCCORE\_ISEN1 >>> PWR\_VCCORE\_ISEN1
- 43 PWR\_VCCORE\_ISEN2 >>> PWR\_VCCORE\_ISEN2
- 43 PWR\_VCCORE\_ISEN3 >>> PWR\_VCCORE\_ISEN3

Title		
Size	Document Number	Rev
Date:	Sheet	



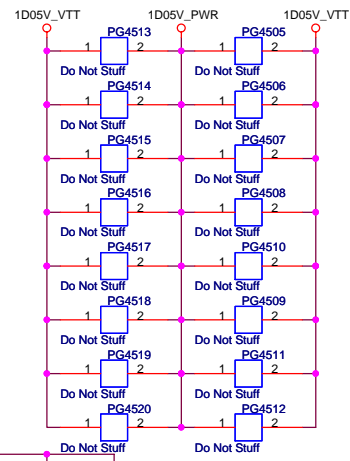
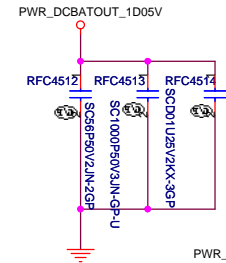
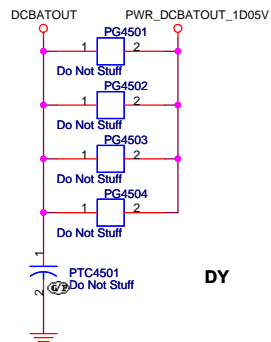


20100804  
79.47719.2BL  
Pana 470u, 2V  
ESR=6mΩ, Irpple=3.5A

Title		
Size	Document Number	Rev
Date	Sheet	



# TPS51218D for 1D05V



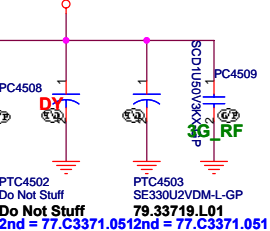
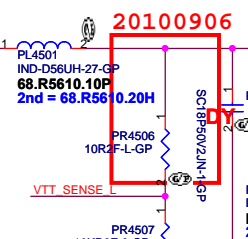
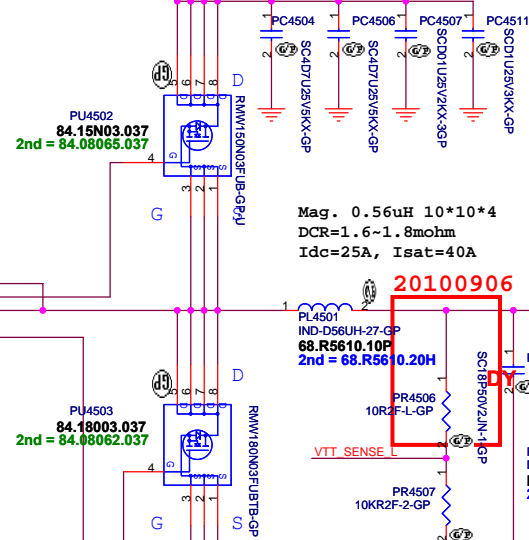
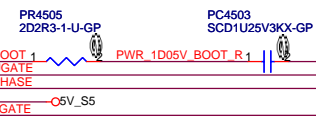
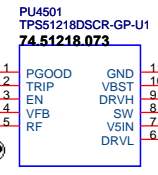
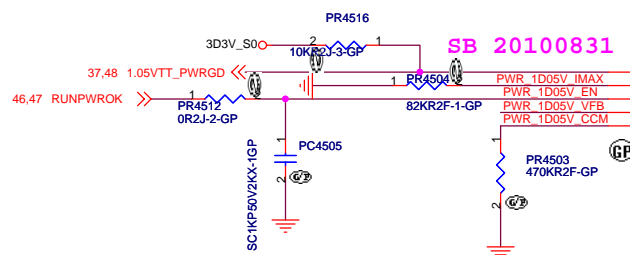
2nd source 還未導入 74.08237.073

20100728  
Id=12.9A  
Qg=9.8-15nC  
Rdson=10.3~12.4mohm

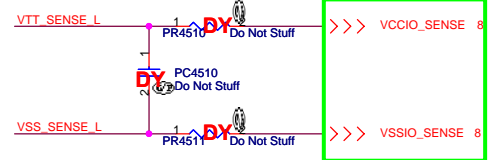
Freq=360KHz

Mag. 0.56uH 10\*10\*4  
DCR=1.6~1.8mohm  
Idc=25A, Isat=40A

Iomax=14A  
OCP>21A

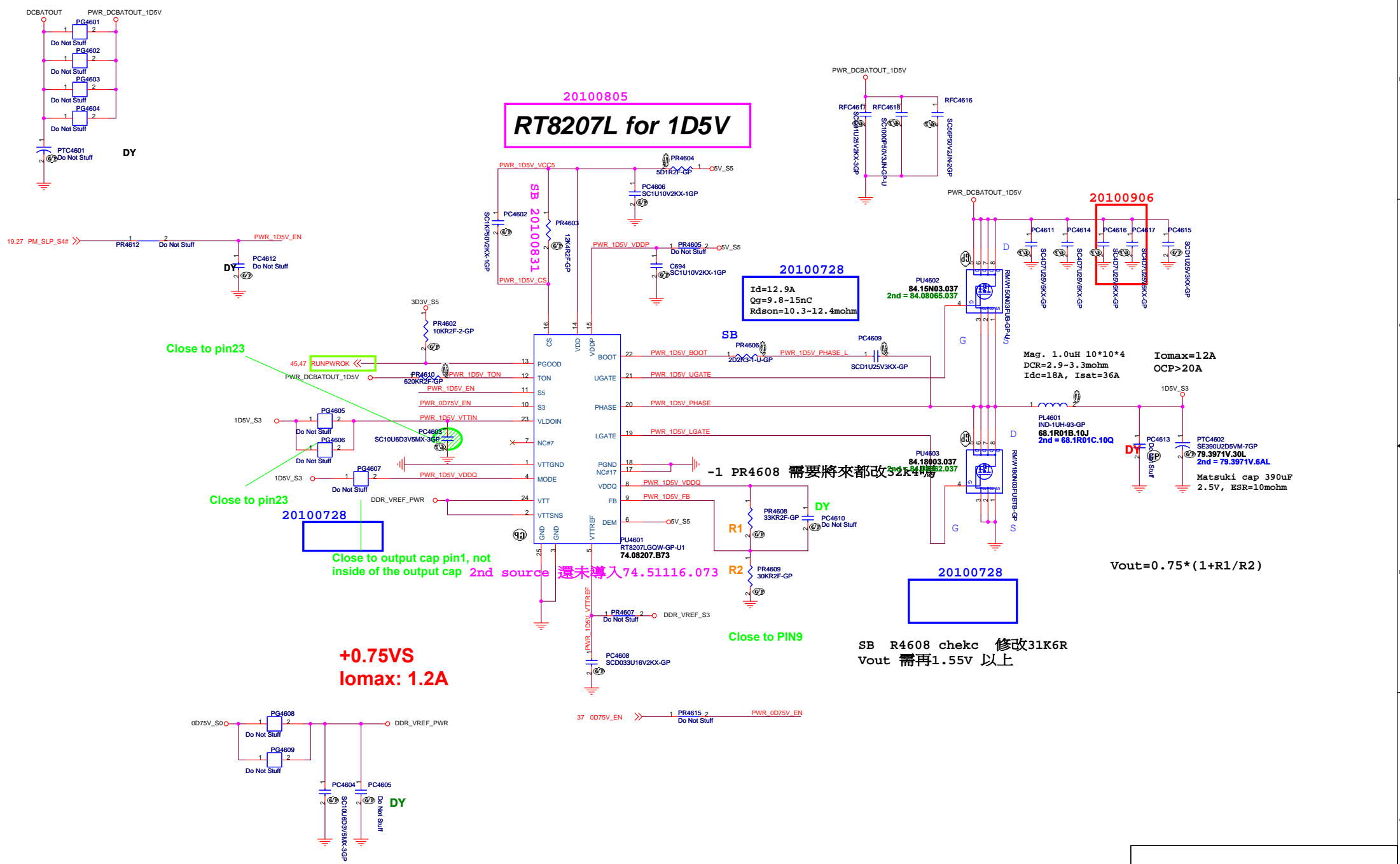


20100728  
Id=19.4A  
Qg=16.8~25.5nC  
Rdson=4.9~6.1mohm



20100728  
 $V_{out} = 0.704 * (1 + R1/R2)$

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Close to pin23

Close to pin23

Close to output cap pin1, not inside of the output cap 2nd source 還未導入 74.51116.073

-1 PR4608 需要將來都改32k4碼

Close to PIN9

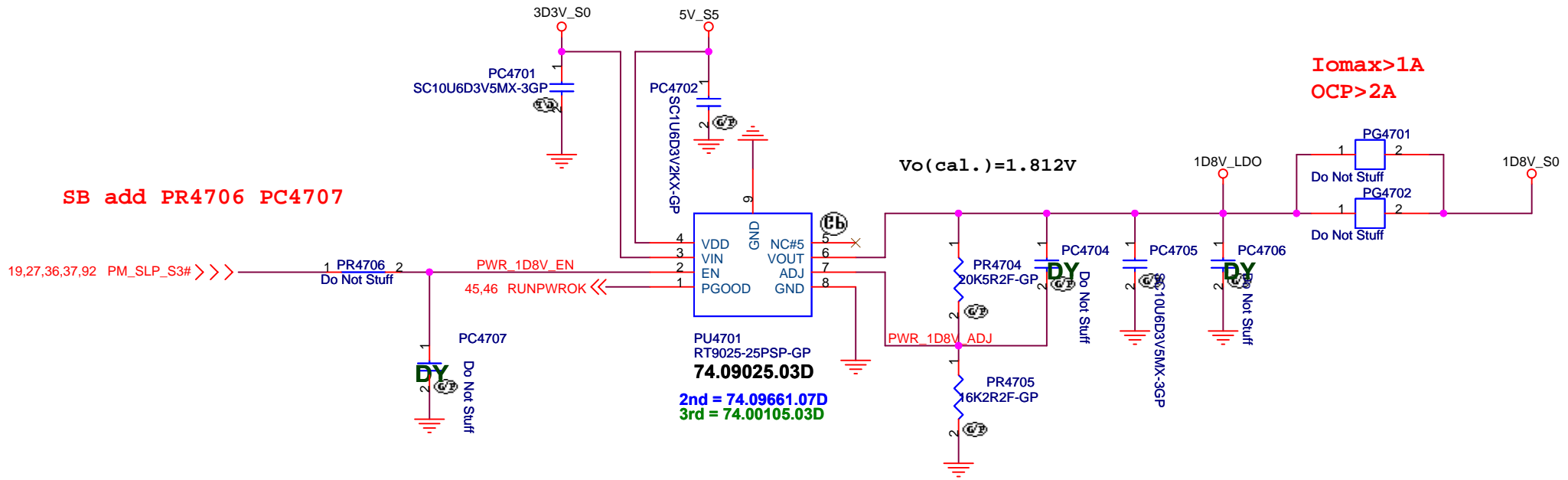
+0.75VS  
Iomax: 1.2A

SB R4608 chekc 修改31K6R  
Vout 需再1.55V 以上

$$V_{out} = 0.75 * (1 + R1/R2)$$

**SSID = PWR.Plane.Regulator\_1p8v**

### RT9025 for 1D8V\_S0

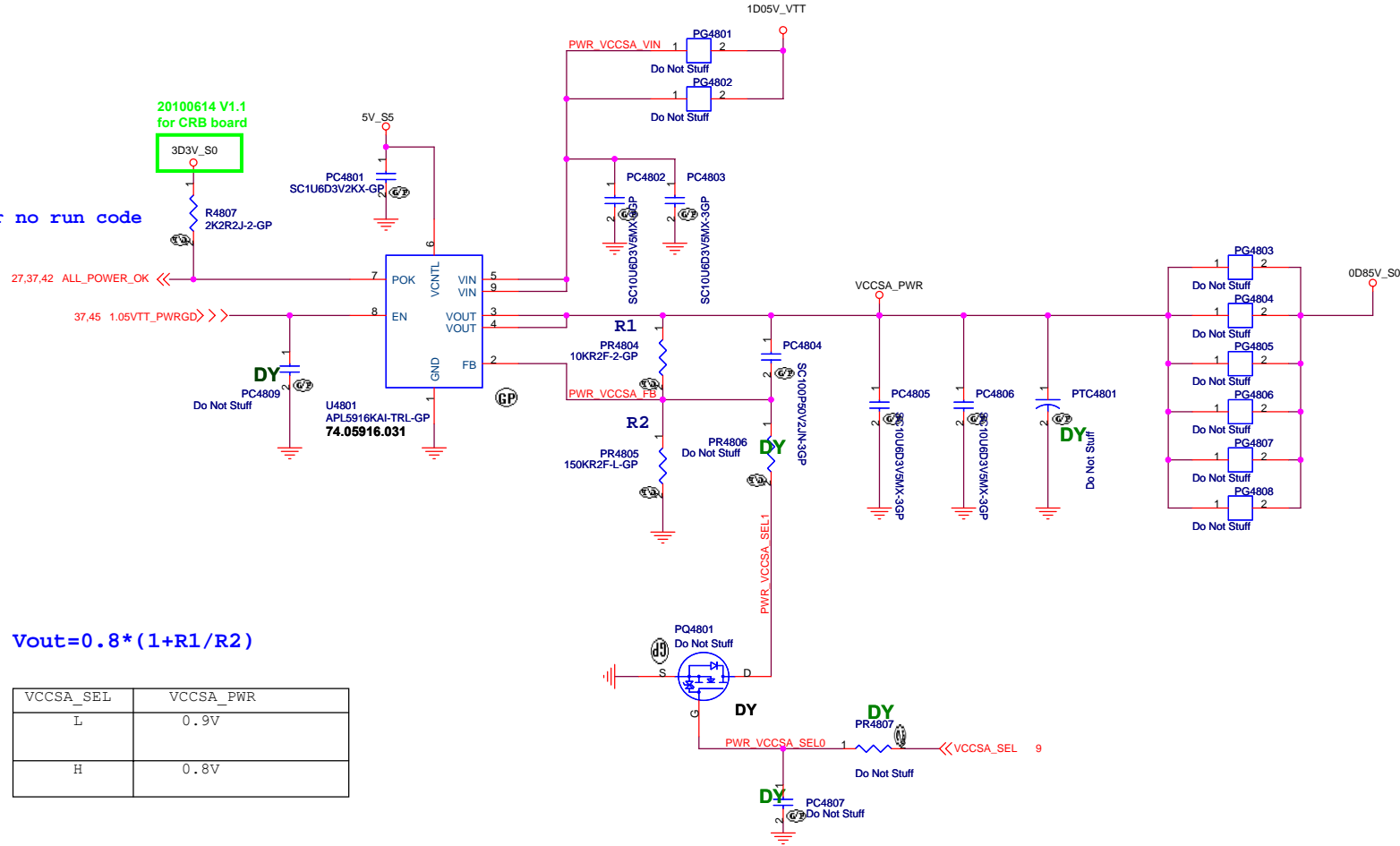


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Size	Document Number	Rev
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# APL5916 for VCCSA

20100614 V1.1  
for CRB board

SB modify 2K2 for no run code

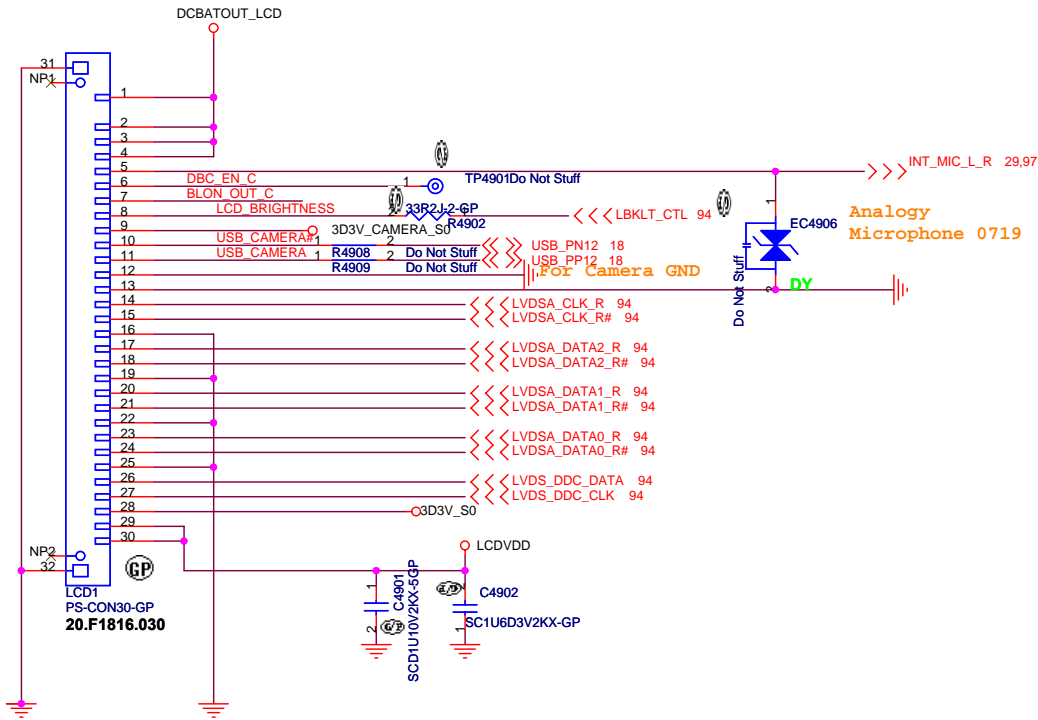


$$V_{out} = 0.8 * (1 + R1/R2)$$

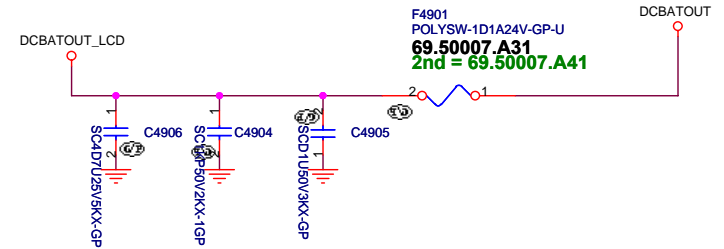
VCCSA_SEL	VCCSA_PWR
L	0.9V
H	0.8V

Title		
Size	Document Number	Rev
Date:	Sheet	

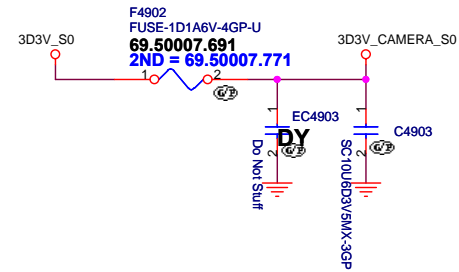
## LVDS CONNECTOR



## INVERTER POWER

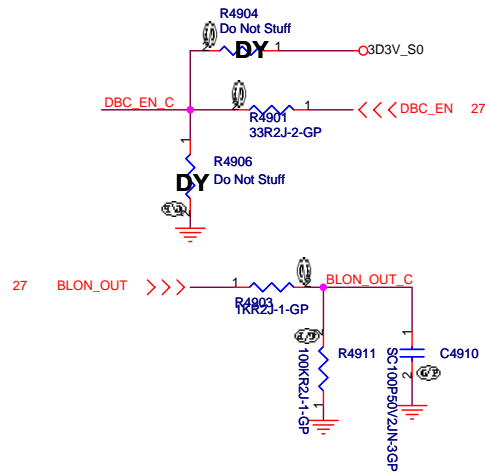
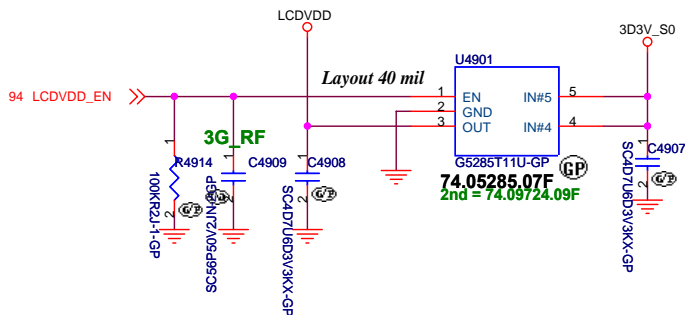


## Camera Power

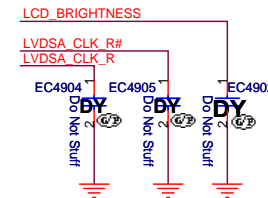


## SSID = VIDEO

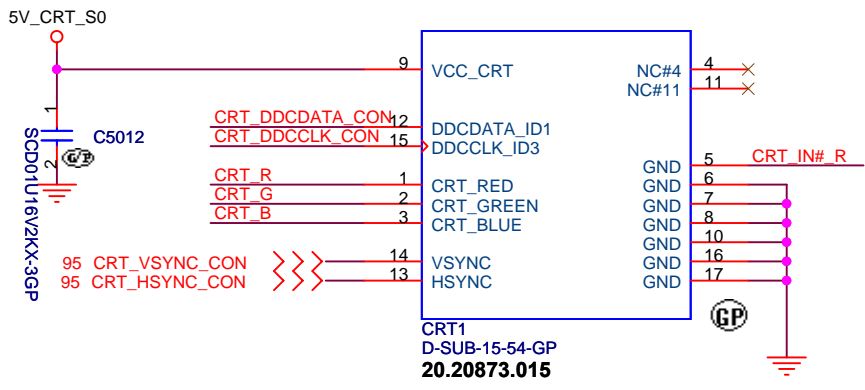
### LCD POWER for ANNIE



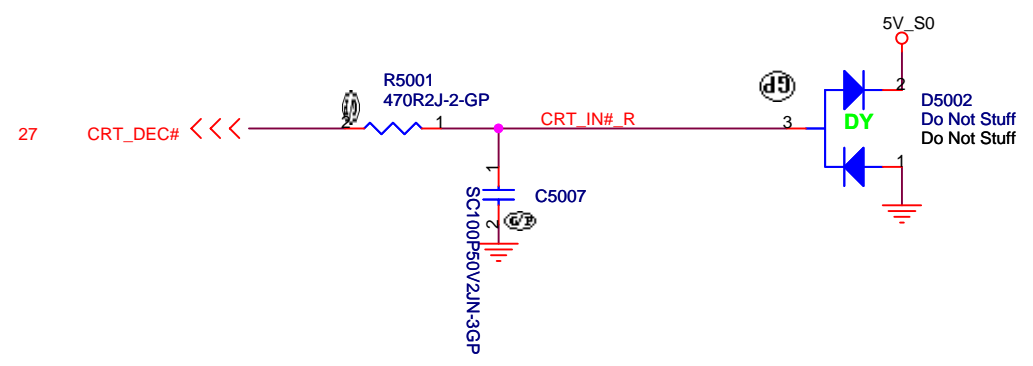
For EMI request  
Close to LVDS connector



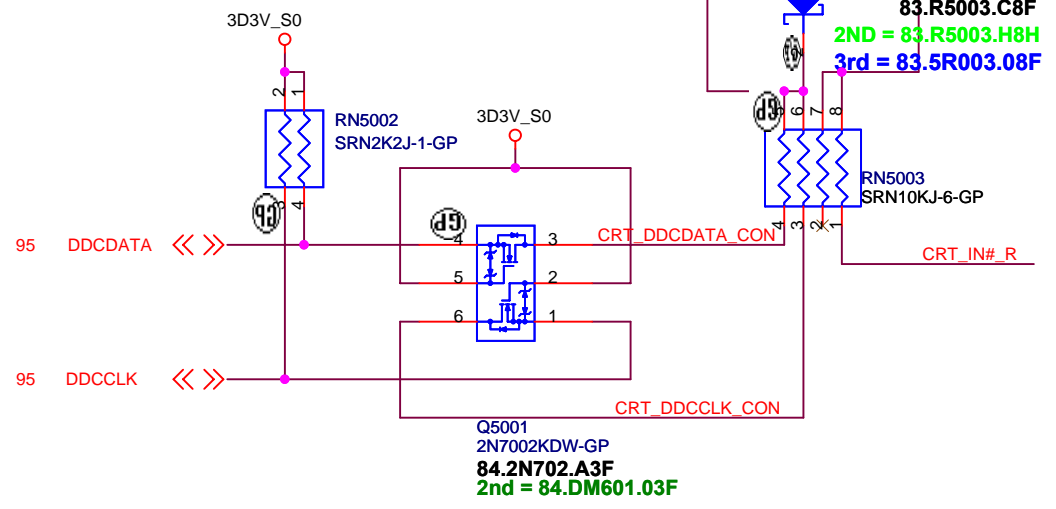
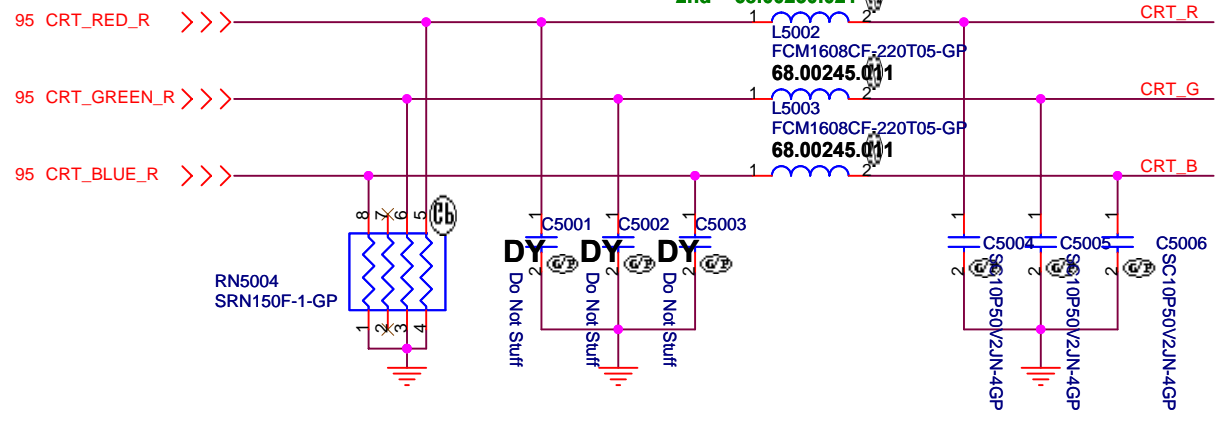
Title		
Size	Document Number	Rev
Date:	Sheet	



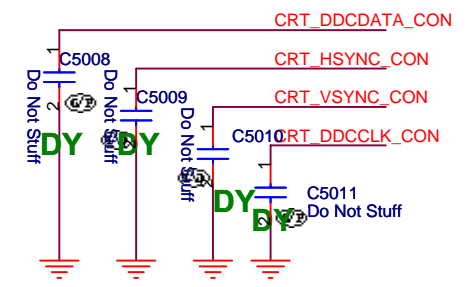
CRT1  
D-SUB-15-54-GP  
20.20873.015



L5001  
FCM1608CF-220T05-GP  
68.00245.011  
2nd = 68.00230.021



Q5001  
2N7002KDW-GP  
84.2N702.A3F  
2nd = 84.DM601.03F



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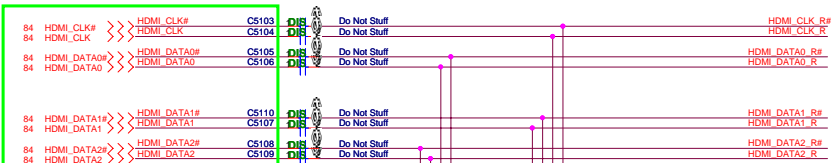
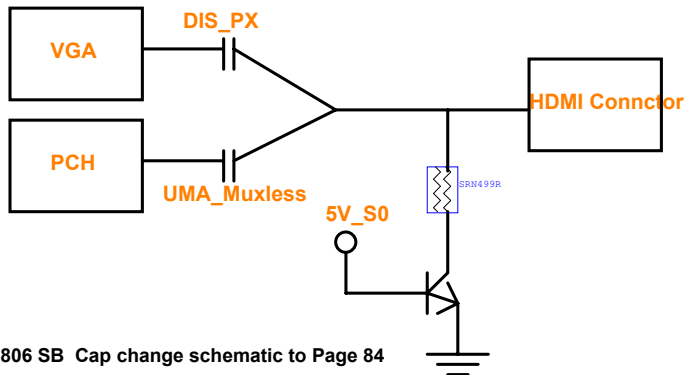


# HDMI Level Shifter & CONNECTOR

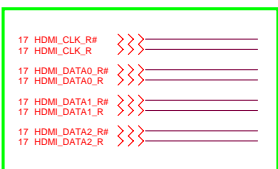
## HDMI CONN

UMA\_Muxless : default setting used PS8101. if don't used PS8101 please change C5103-C5110 to 0 ohm resistor

### HDMI DISCRETE/ UMA Co-lay

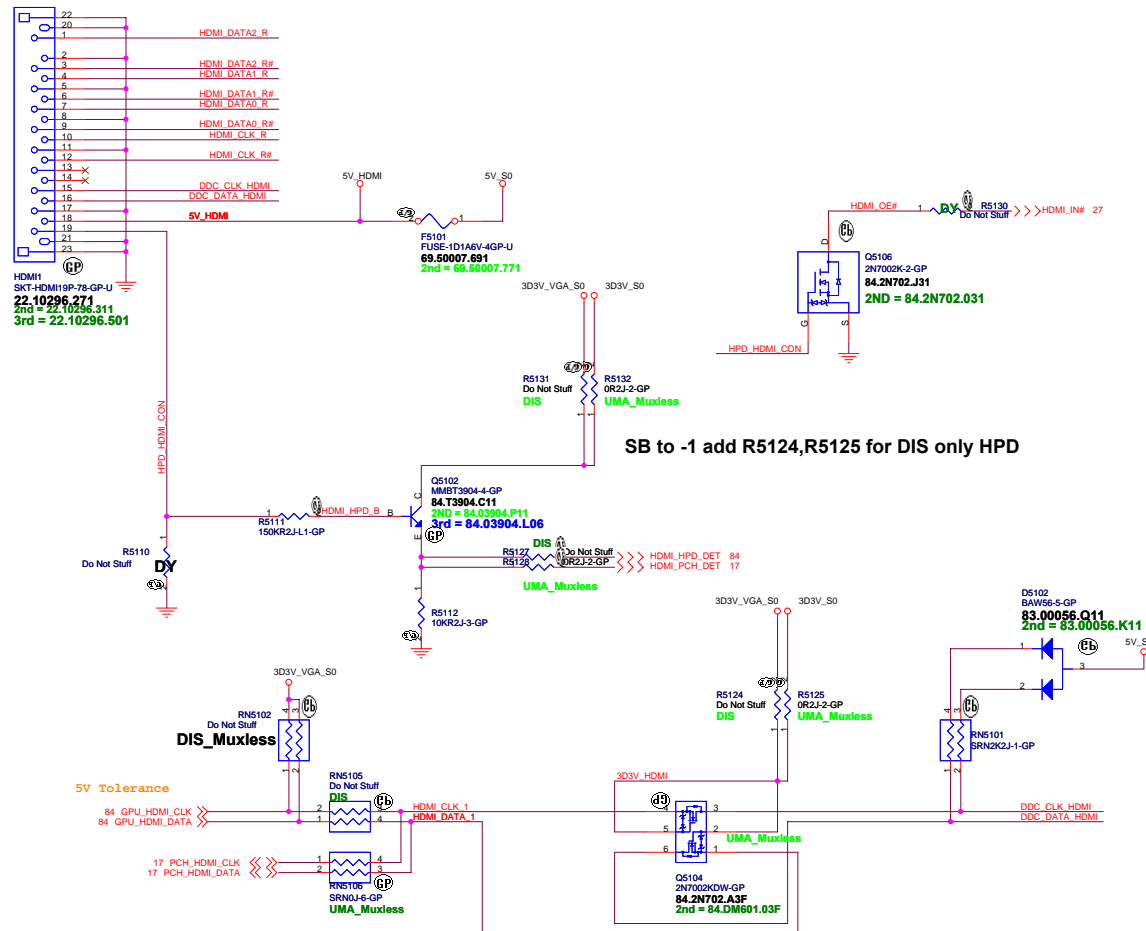


Close to HDMI Connector



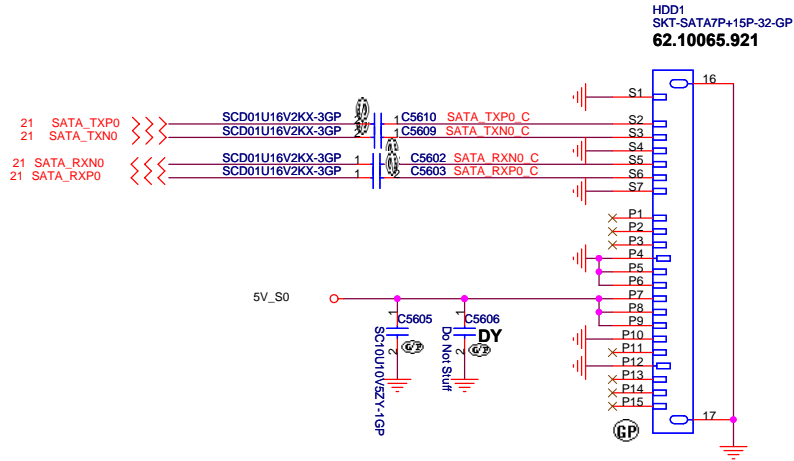
SB to -1 for vendor suggest

Close to Level Shift



SB to -1 add R5124,R5125 for DIS only HPD

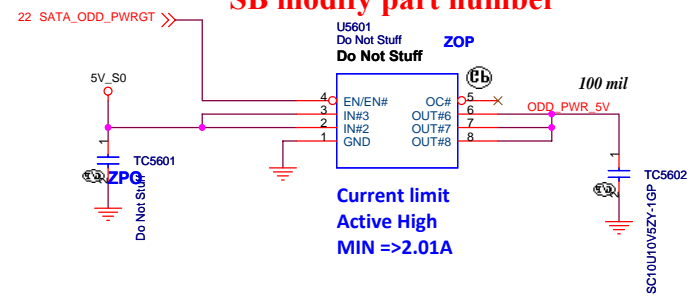
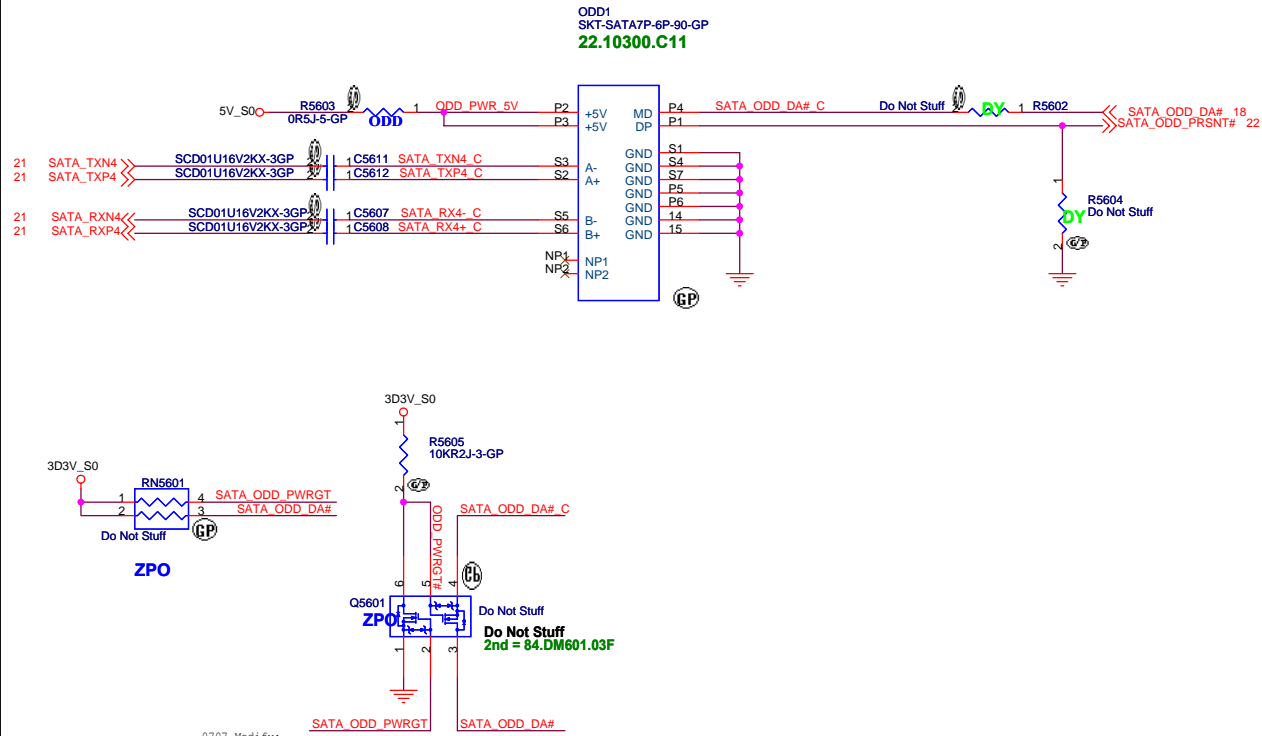
Title	
Size	Document Number
Date	Sheet



# ODD Connector

# SB SATA Zero Power ODD

SB modify part number



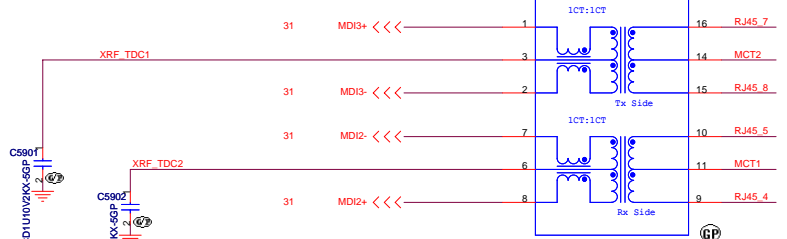
0707 Modify:  
Change Q5601 to DUAL 2N7002 for isolate MD/DA signal between PCH and ODD.

Title		
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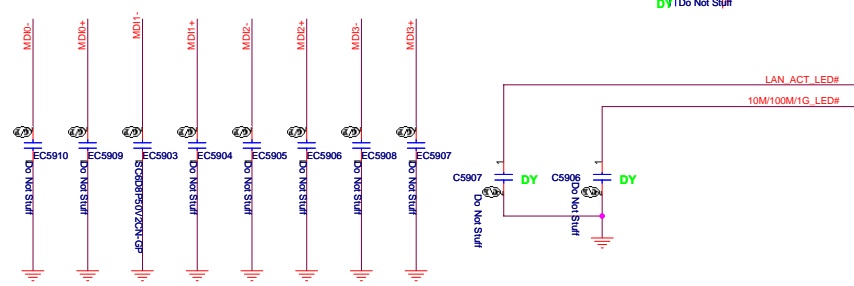
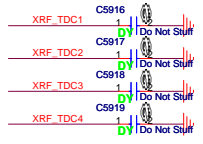
GIGA Lan Transformer

XF5901  
XFORM-12P-36-GP  
68.HD081.30B  
Change:68.68160.30B  
2nd = 68.HD081.30B

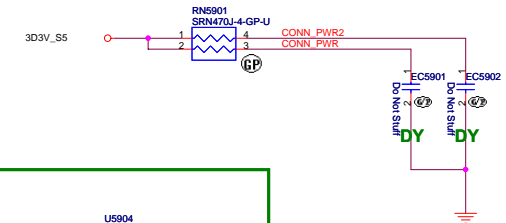
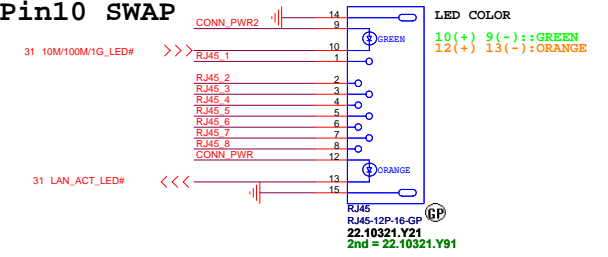
LAN MDI Off-Page



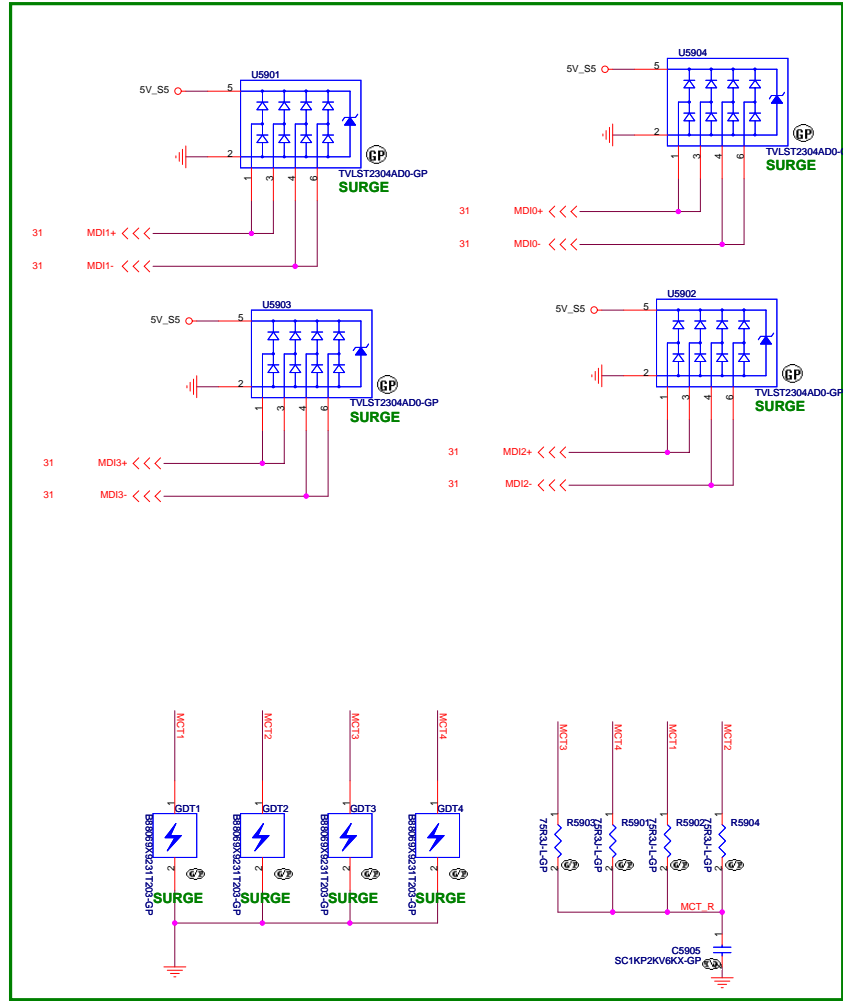
XF5902  
XFORM-12P-36-GP  
68.HD081.30B  
Change:68.68160.30B  
2nd = 68.HD081.30B



SB modifyf Pin9 Pin10 SWAP

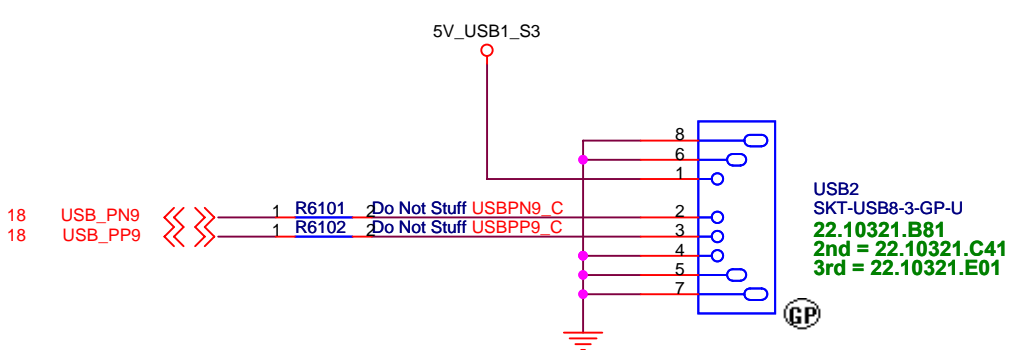
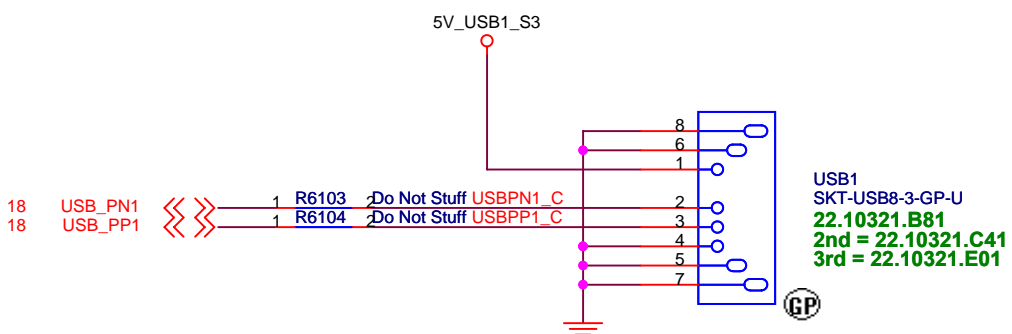
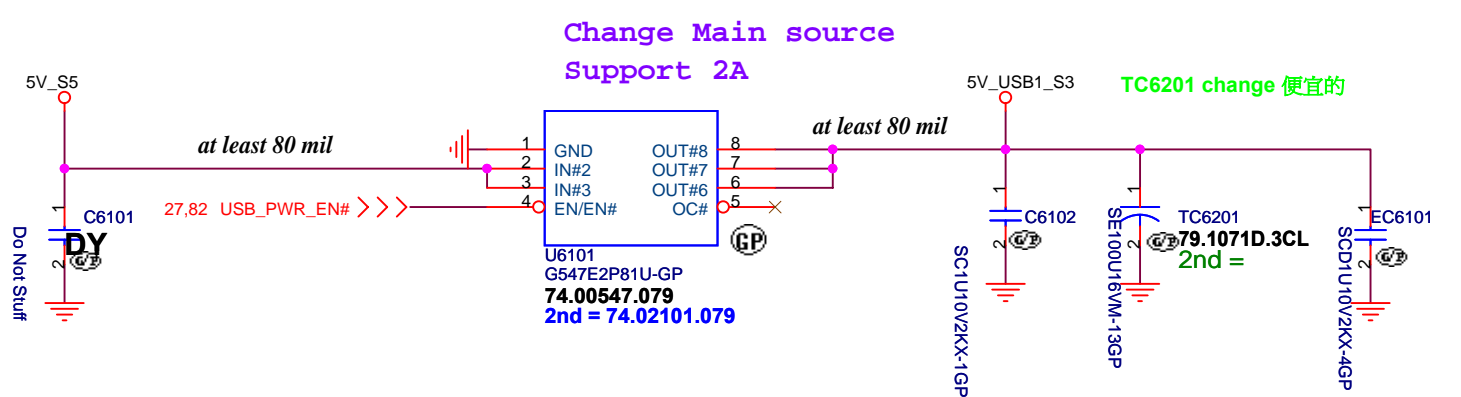


SB modify For EMI



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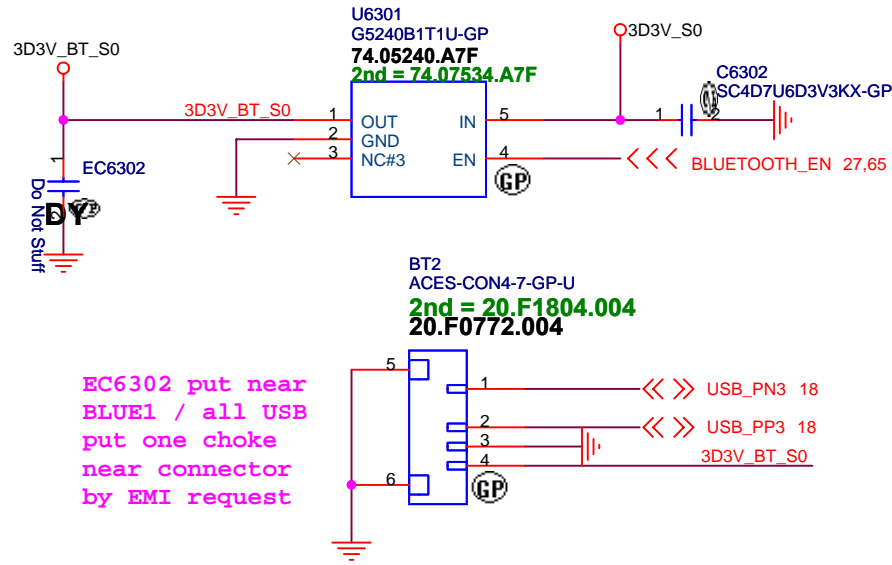




Title		
Size	Document Number	Rev
Date:	Sheet	

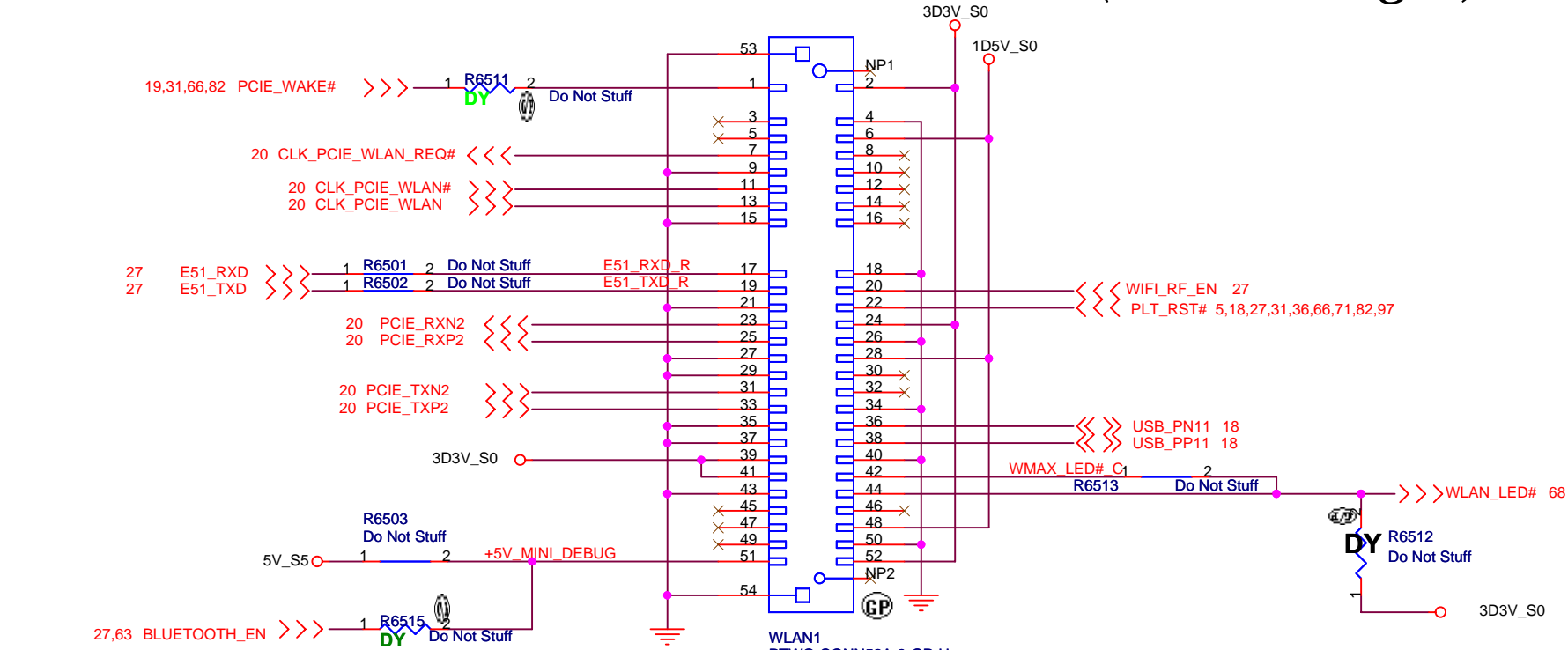
Bluetooth Module conn.

# ANNIE Bluetooth Module



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Size	Document Number	Rev
Date:	Sheet	

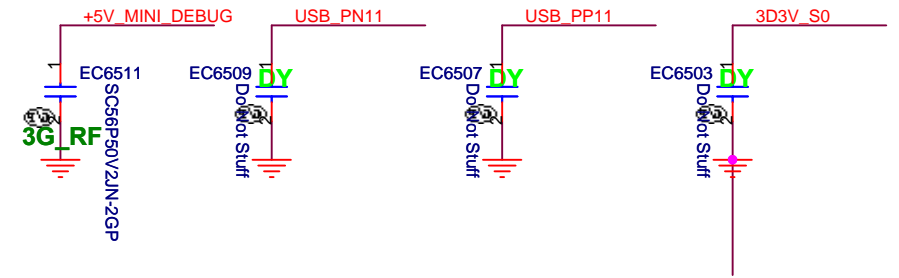
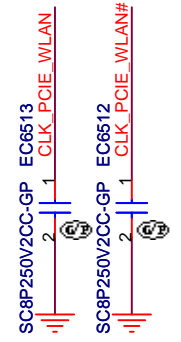
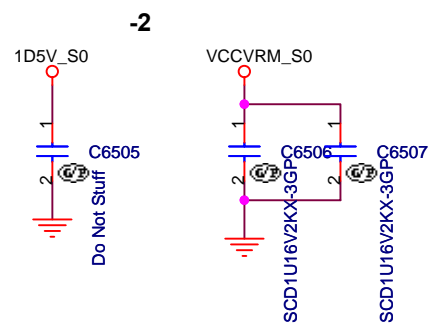
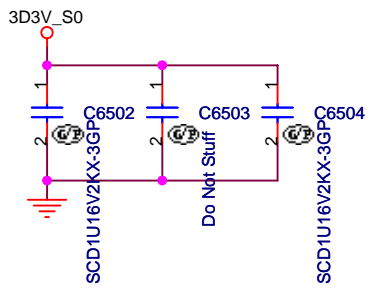
# Mini Card Connector(802.11a/b/g/n)



WLAN1  
 BTWO-CONN52A-9-GP-U  
**20.F1519.052**  
 2nd = 62.10043.A51  
 3rd = 20.F1693.052  
 4th = 20.F1743.052

## SB modify for SIV

## RF suggestion

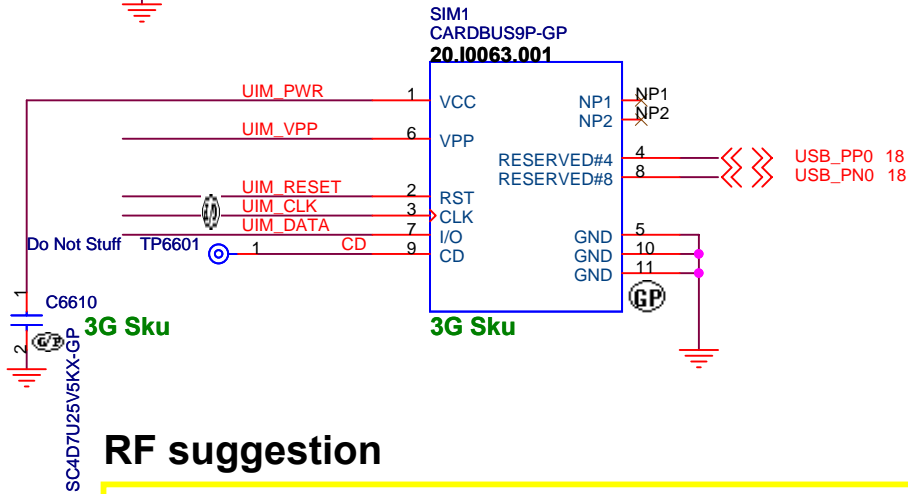
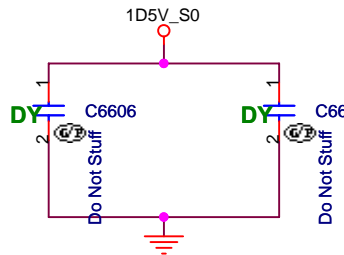
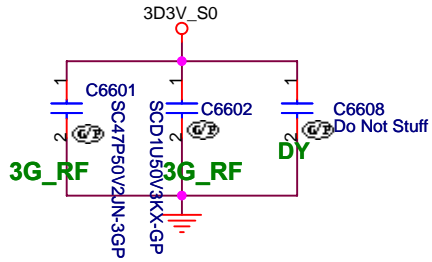


Title		
Size	Document Number	Rev
Date:	Sheet	

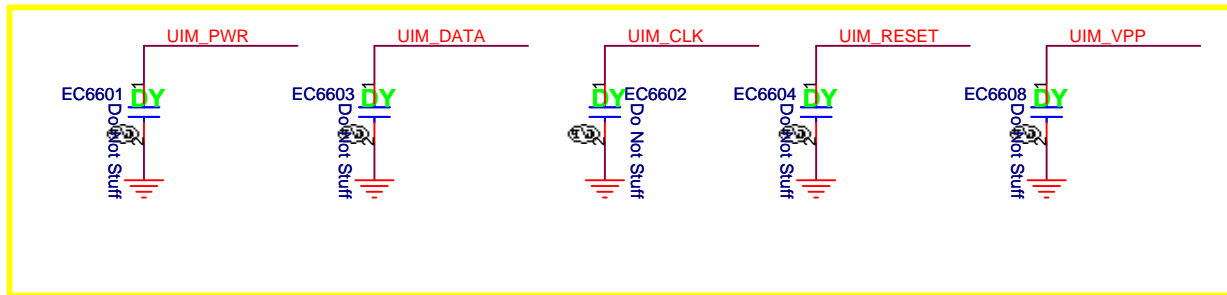
# Mini Card Connector(WWAN)

20100712 V1.5

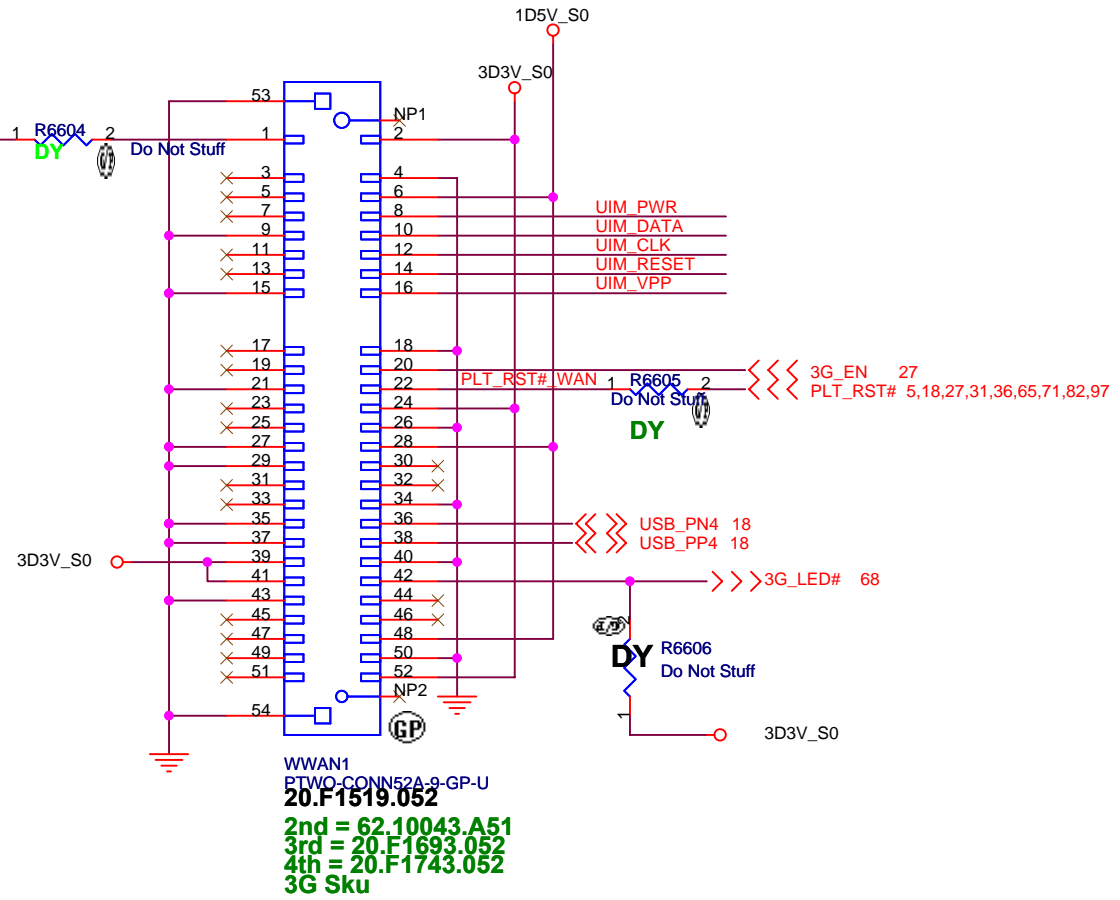
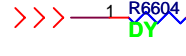
Place near MINI Card CONN



## RF suggestion



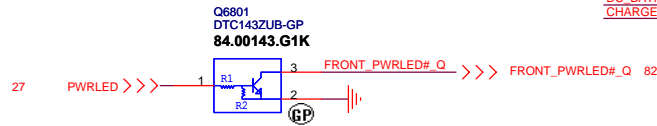
19,31,65,82 PCIE\_WAKE# >>>



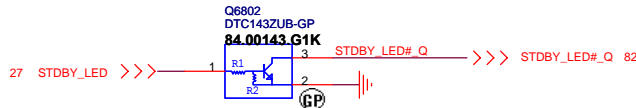
Title		
Size	Document Number	Rev
Date:	Sheet	



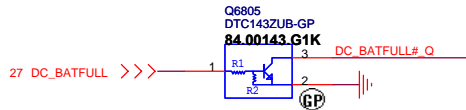
## Power button LED



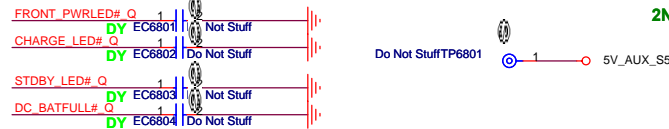
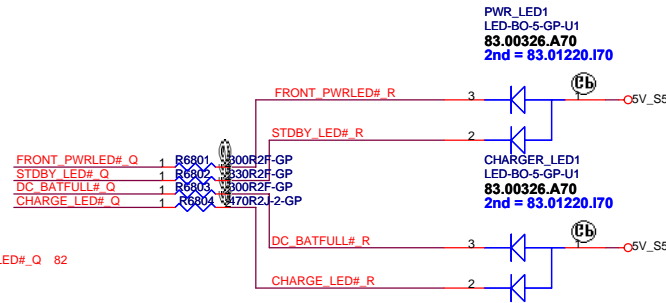
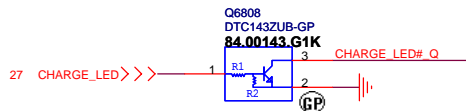
## Power STDBY\_LED



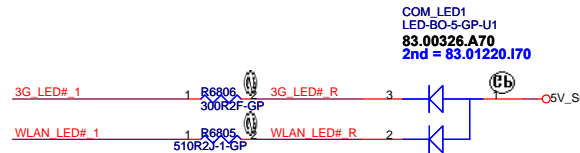
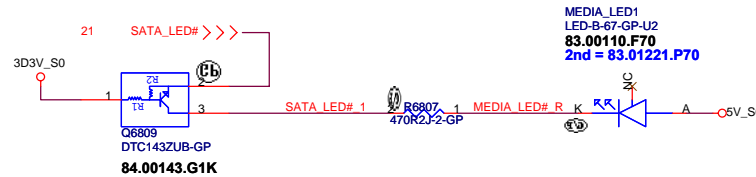
## Battery LED2 (DC\_BATFULL)



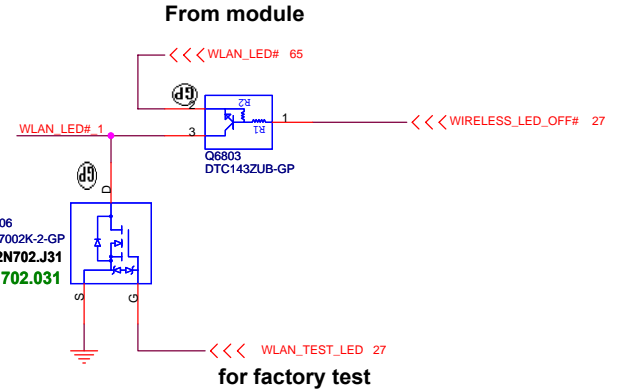
## Battery LED1 (CHARGE)



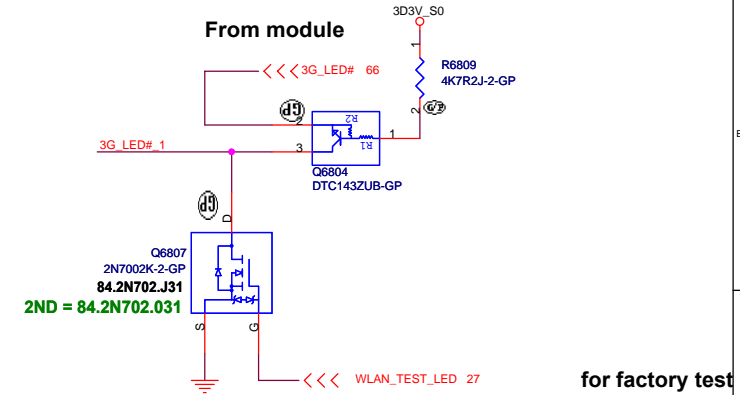
## SATA HDD LED



## WLAN\_LED



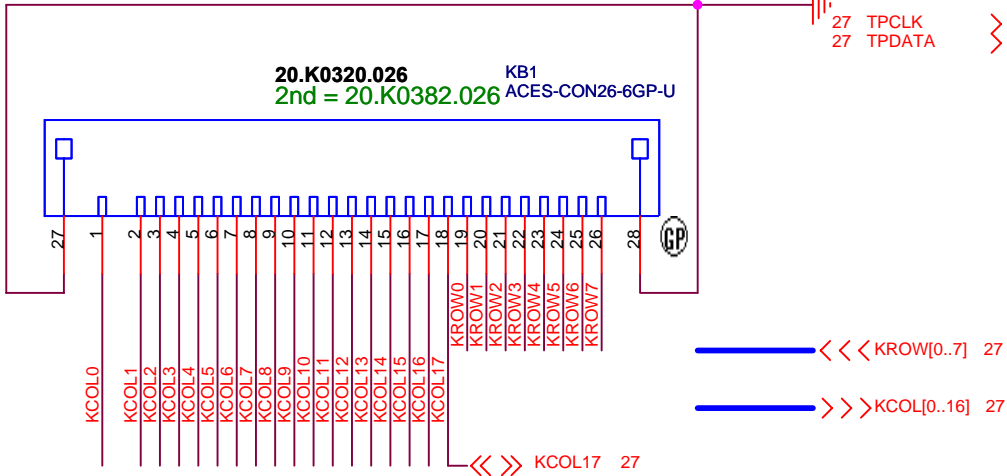
## 3G LED



Title		
Size	Document Number	Rev
Date:	Sheet	

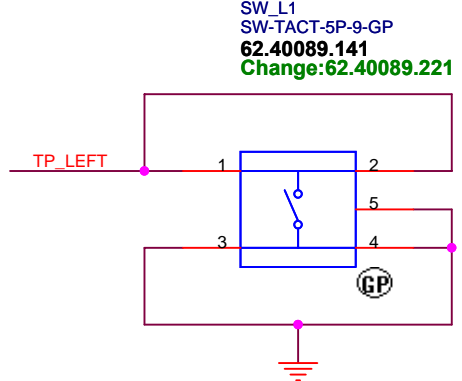
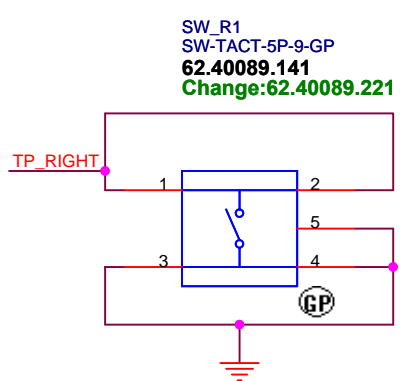


# Internal KeyBoard Connector



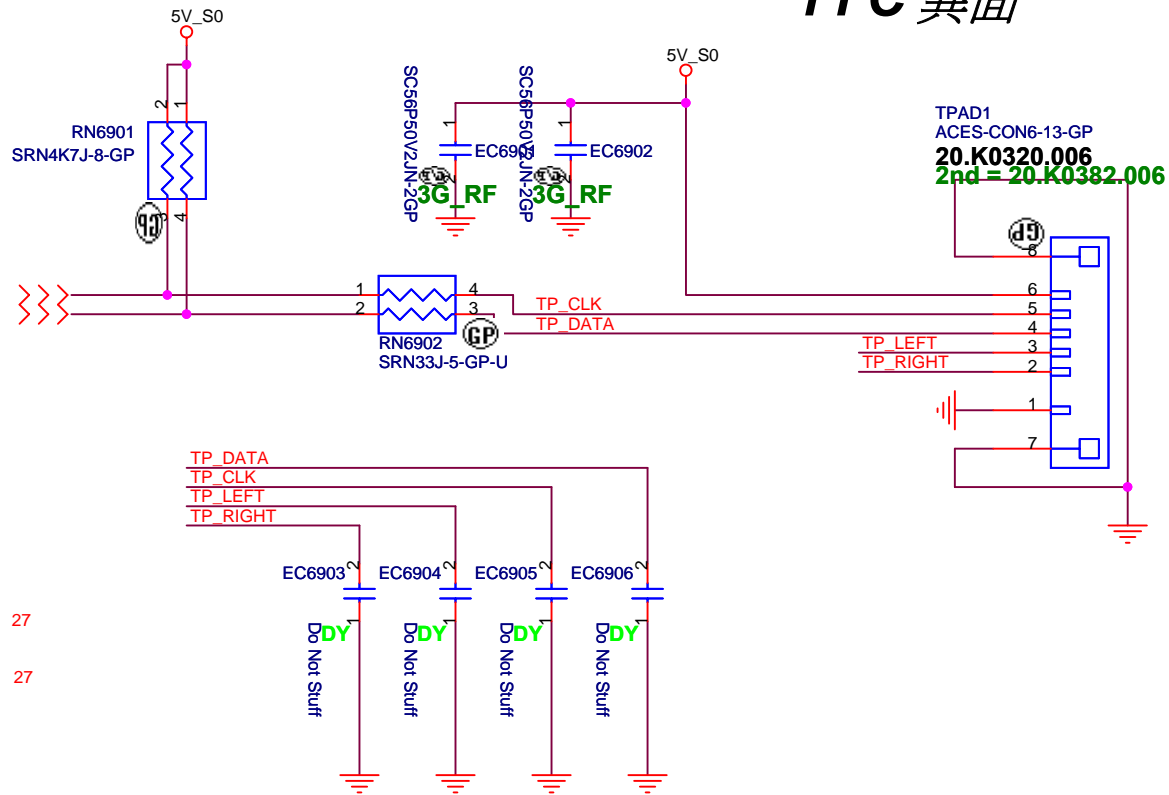
MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1  
 KB PIN DEFINE 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26

26 **K/B** 1 **SB to -1 modify Part number**

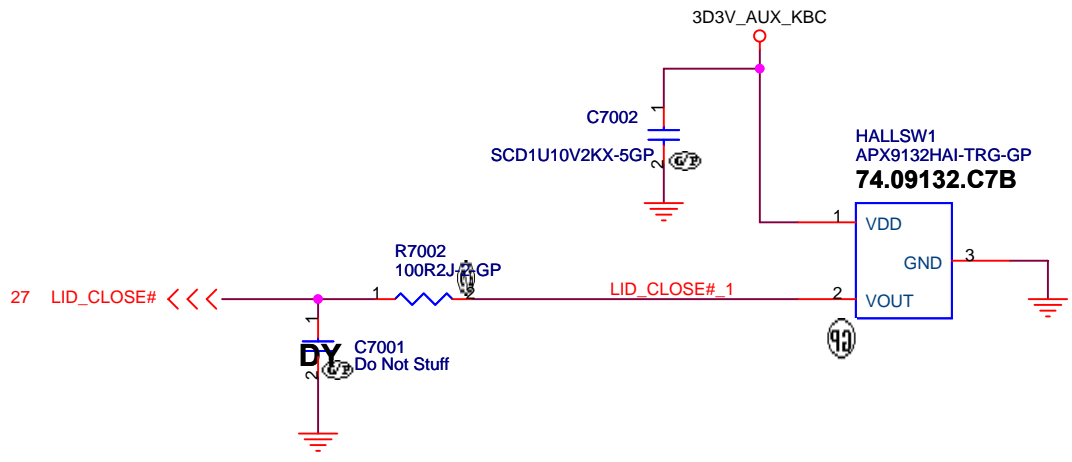


# TOUCH PAD

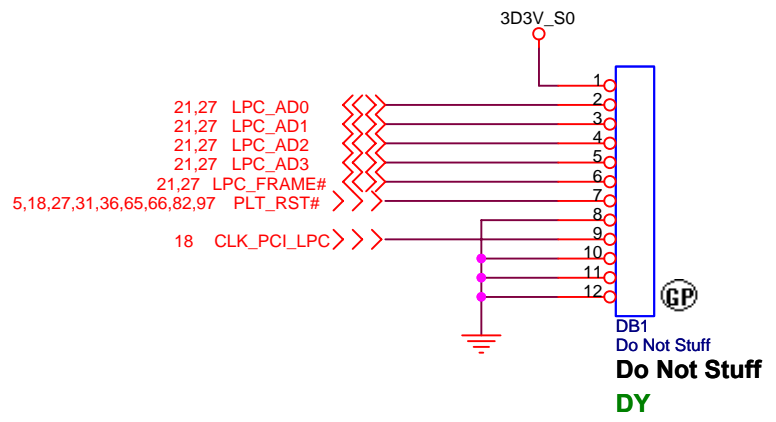
## FFC 異面



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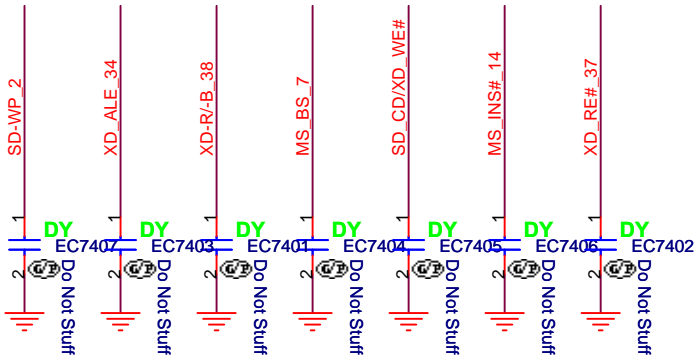
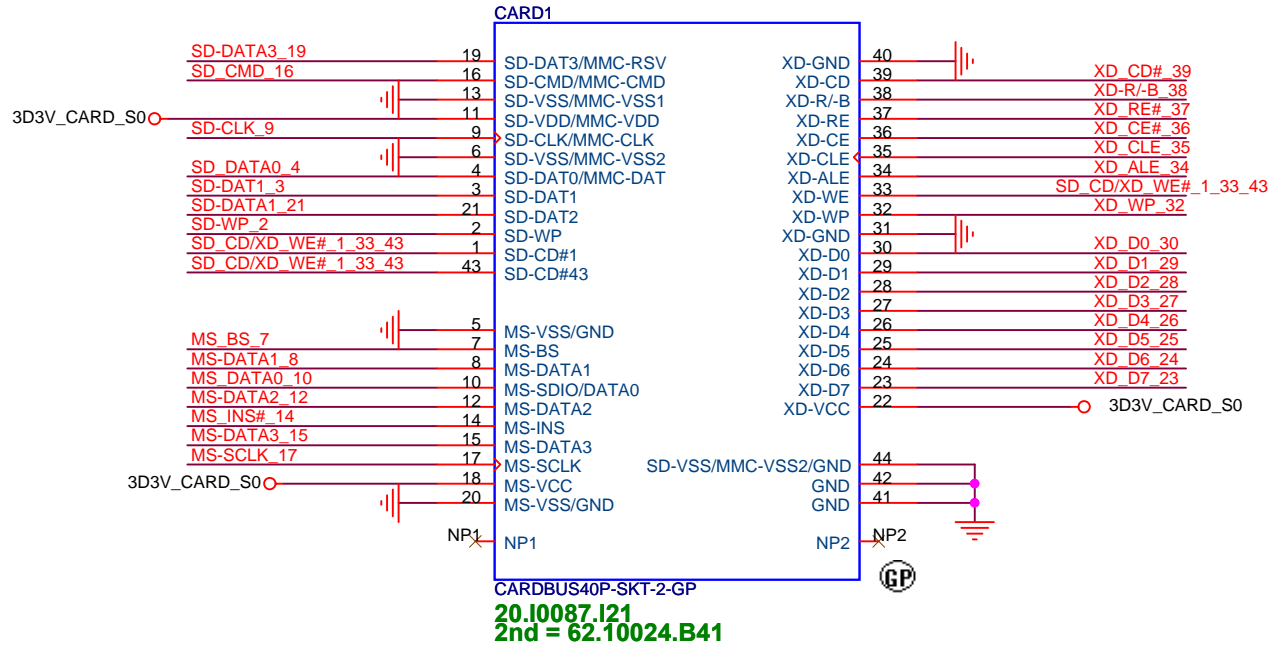


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2	1	

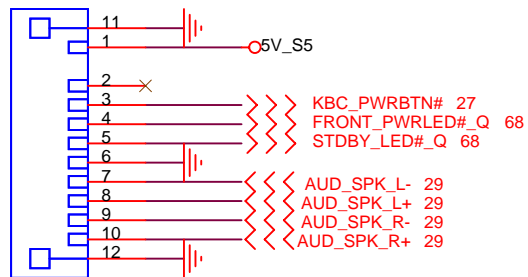
# SD/XD/MS Card Reader



- 32 SD-DATA3\_19
- 32 SD\_CMD\_16
- 32 SD-CLK\_9
- 32 SD\_DATA0\_4
- 32 SD-DAT1\_3
- 32 SD-DATA1\_21
- 32 SD-WP\_2
- 31,32 SD\_CD/XD\_WE#
  
- 32 MS\_BS\_7
- 32 MS-DATA1\_8
- 32 MS\_DATA0\_10
- 32 MS-DATA2\_12
- 32 MS\_INS#\_14
- 32 MS-DATA3\_15
- 32 MS-SCLK\_17
  
- 32 XD\_CD#\_39
- 32 XD-R/-B\_38
- 32 XD\_RE#\_37
- 32 XD\_CE#\_36
- 32 XD\_CLE\_35
- 32 XD\_ALE\_34
- 32 SD\_CD/XD\_WE#\_1\_33\_43
- 32 XD\_WP\_32
  
- 32 XD\_D0\_30
- 32 XD\_D1\_29
- 32 XD\_D2\_28
- 32 XD\_D3\_27
- 32 XD\_D4\_26
- 32 XD\_D5\_25
- 32 XD\_D6\_24
- 32 XD\_D7\_23

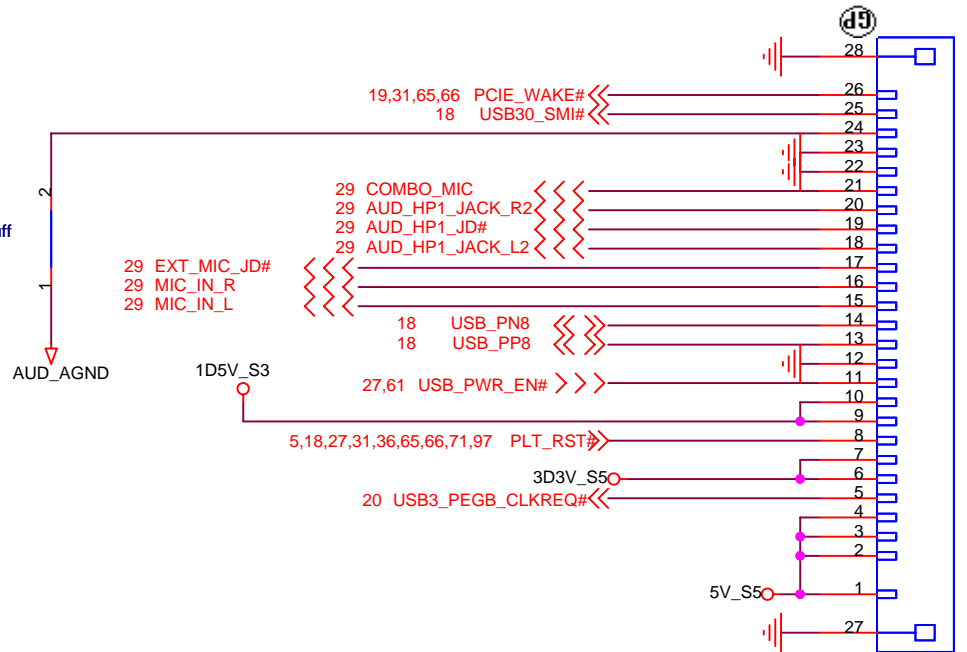


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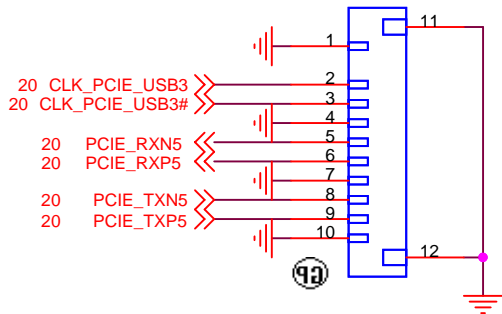
PWRCN1  
 ACES-CON10-20-GP  
**20.K0422.010**  
 2nd = 20.K0382.010

R8105  
D8 Not Stuff



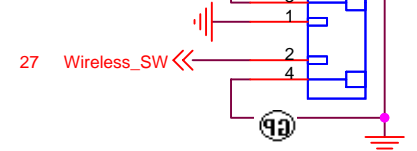
USBCN1  
 ACES-CON26-11-GP  
**20.K0315.026**  
 2nd = 20.K0370.026

USBCN2  
 ACES-CON10-18-GP  
**20.K0315.010**  
 2nd = 20.K0392.010



RF\_CN1  
 ACES-CON2-11-GP  
**20.F0772.002**

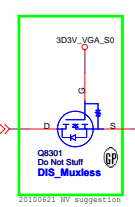
**BAE40**



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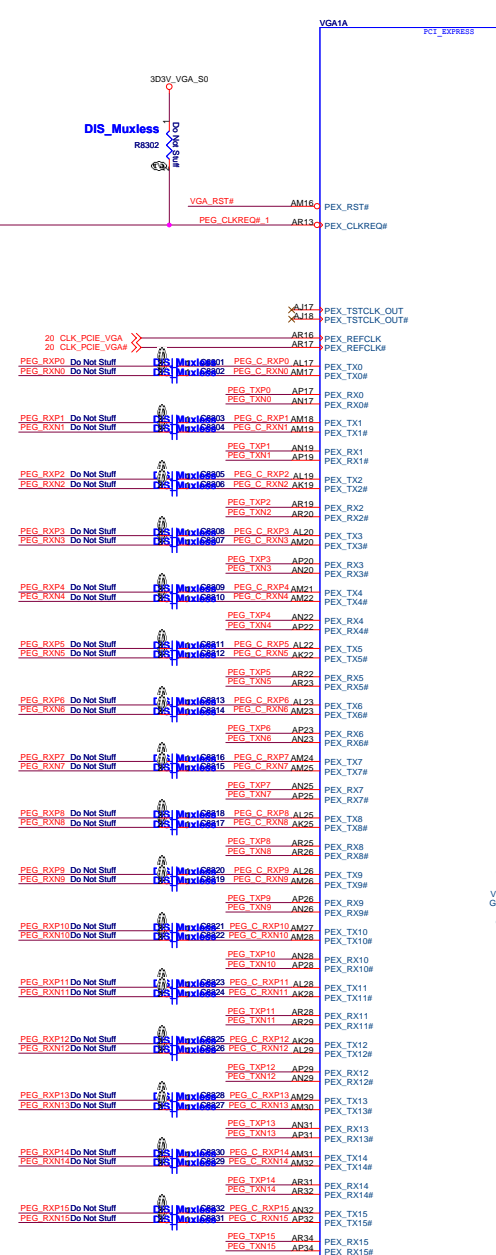
3D3V\_VGA\_S0  
 R8303  
 DY  
 SB 因為 sequence 會有兩段  
 R8303 change to pull low 預留 ??

18 DGPU\_HOLD\_RST#  
 R8361 2 VEGA\_RST#  
 Do Not Stuff

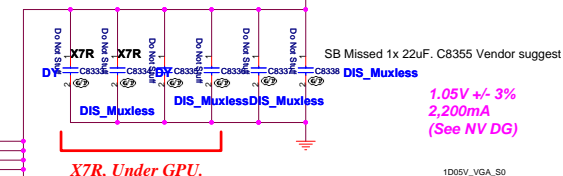


4 PEG\_TXP0[0..15]  
 4 PEG\_TXN0[0..15]

PEG\_RXP0[0..15] 4  
 PEG\_RXN0[0..15] 4

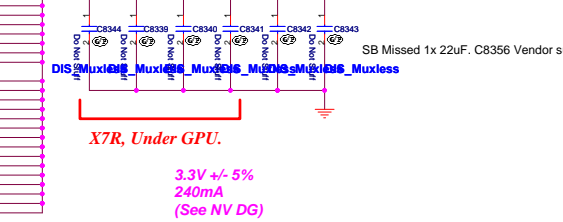


N12P GV: 71.0N12P.A0U  
 N12P GS: 71.0N12P.E0U  
 N11P GS: 71.0N11P.E0U  
 DIS\_Muxless



X7R, Under GPU.

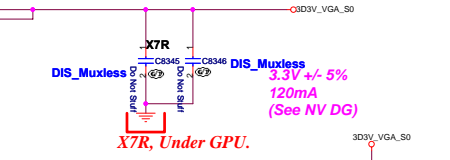
1.05V +/- 3%  
 2,200mA  
 (See NV DG)



X7R, Under GPU.

3.3V +/- 5%  
 240mA  
 (See NV DG)

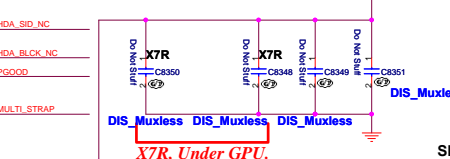
-1 Vendor suggest modify 3D3V\_VGA\_S0



X7R, Under GPU.

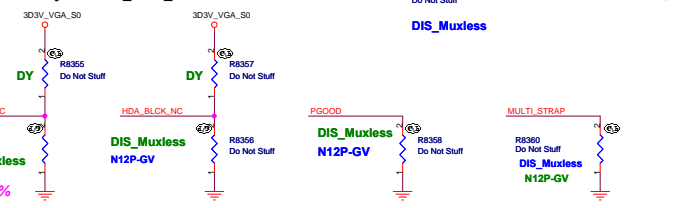
3.3V +/- 5%  
 120mA  
 (See NV DG)

-1 delete R8311 for suggest

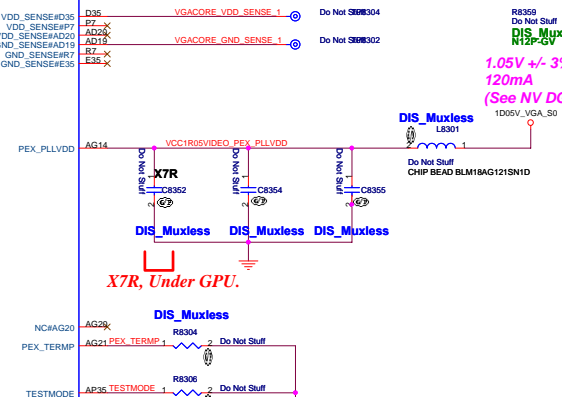


X7R, Under GPU.

SB modify to 3D3V\_VGA\_S0

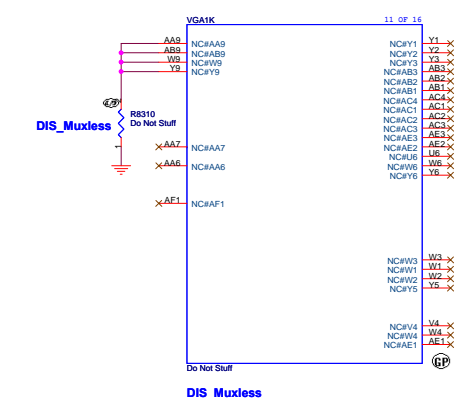


1.05V +/- 3%  
 120mA  
 (See NV DG)

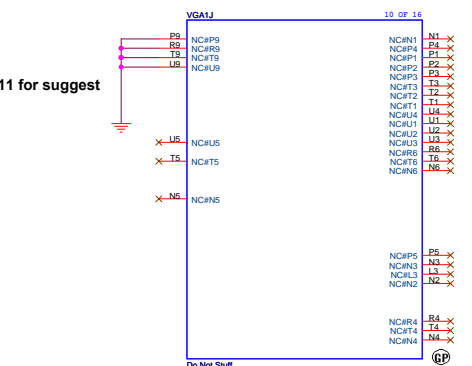


X7R, Under GPU.

DIS\_Muxless



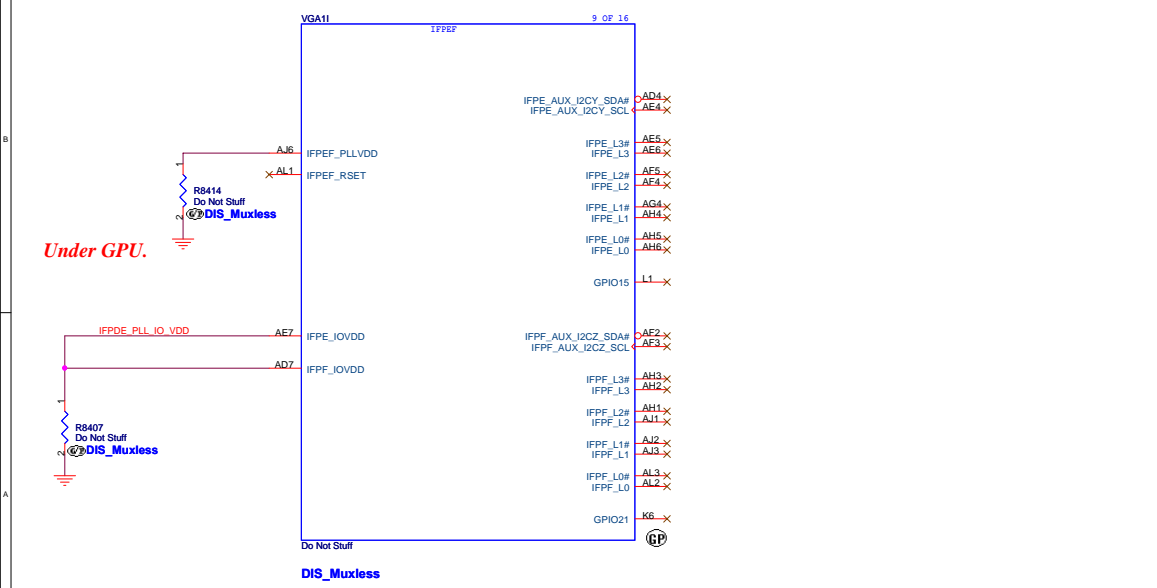
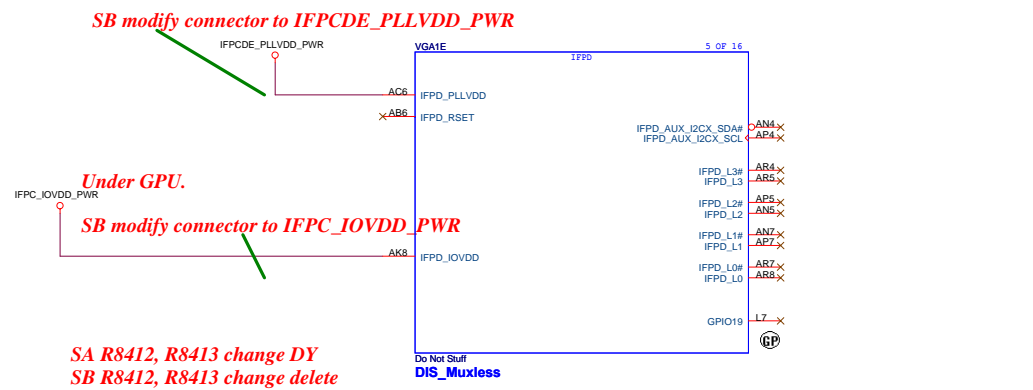
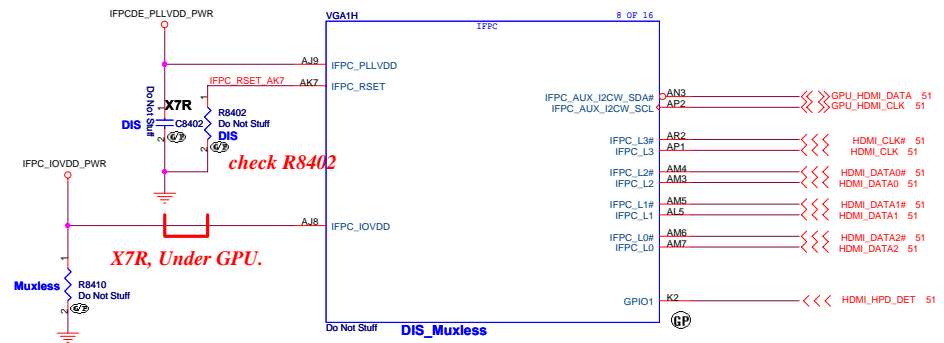
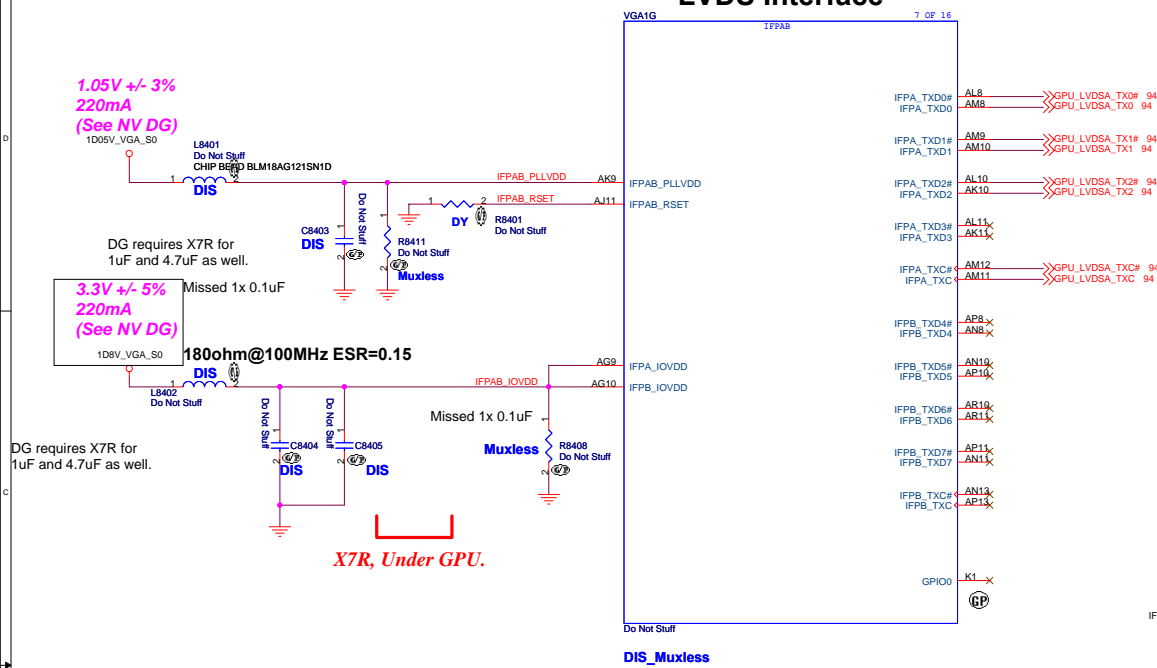
DIS\_Muxless



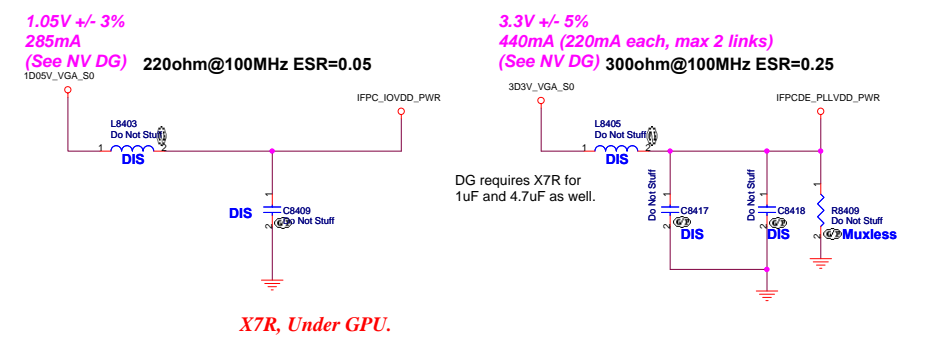
DIS\_Muxless

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# LVDS Interface

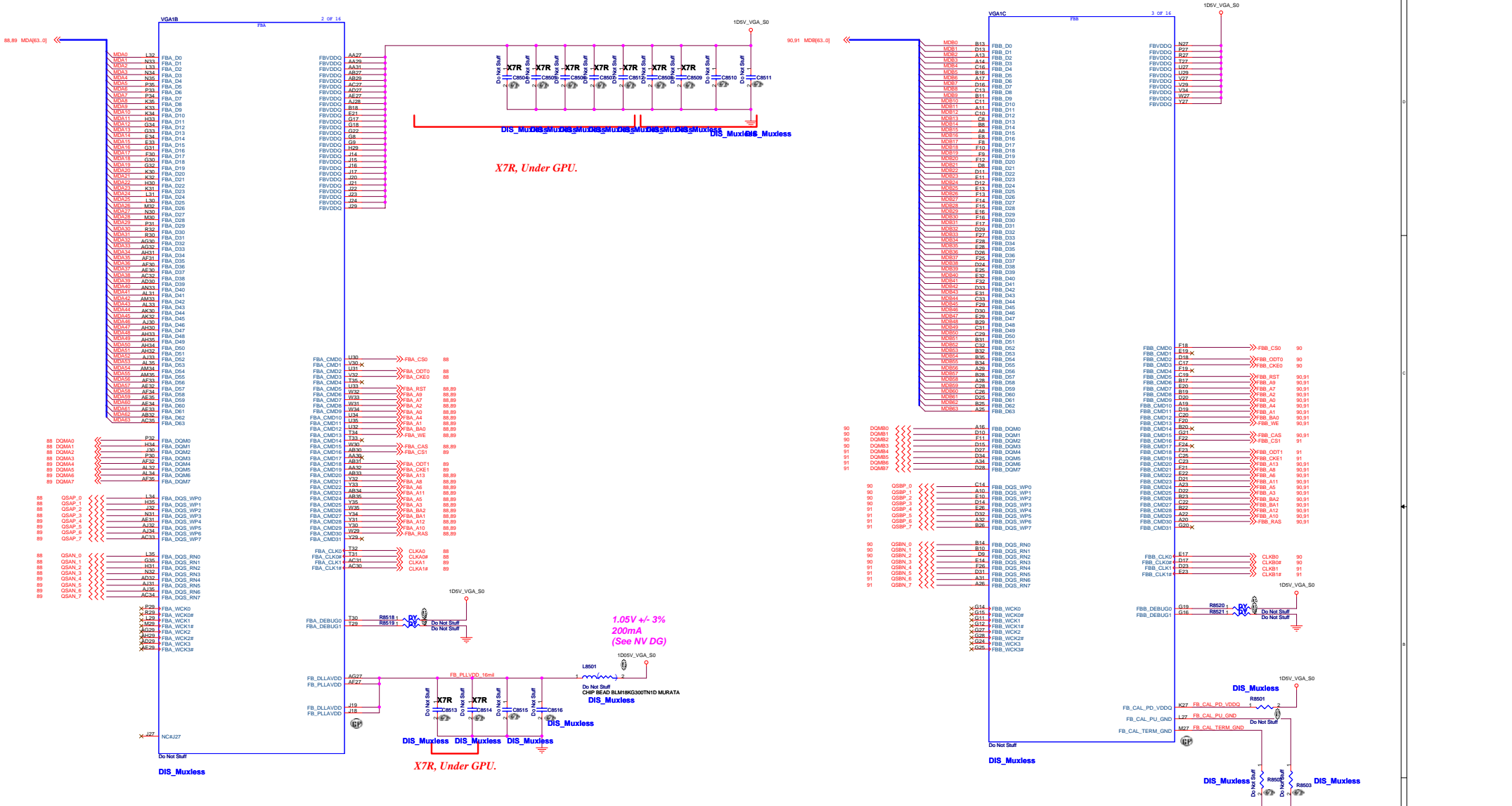


# HDMI Interface

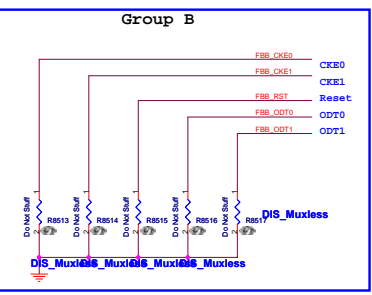
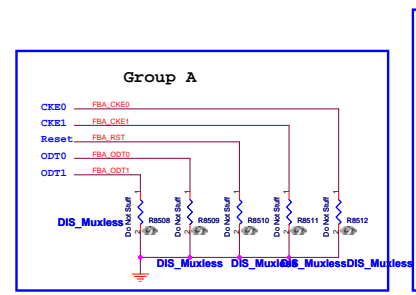


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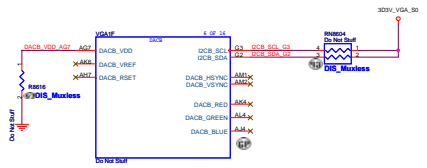
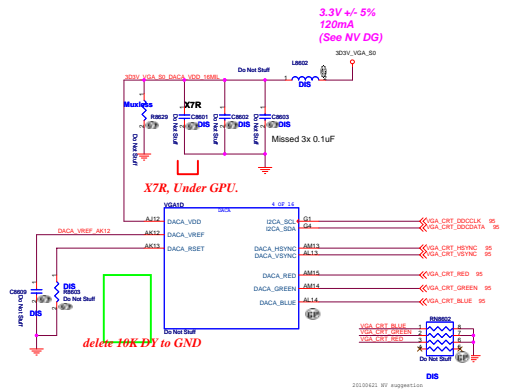


FBCLK Termination place on VRAM side

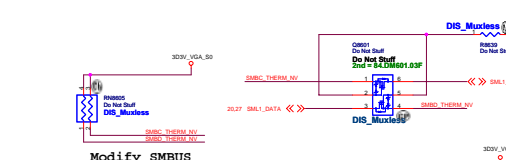


FBCLK Termination place on VRAM side

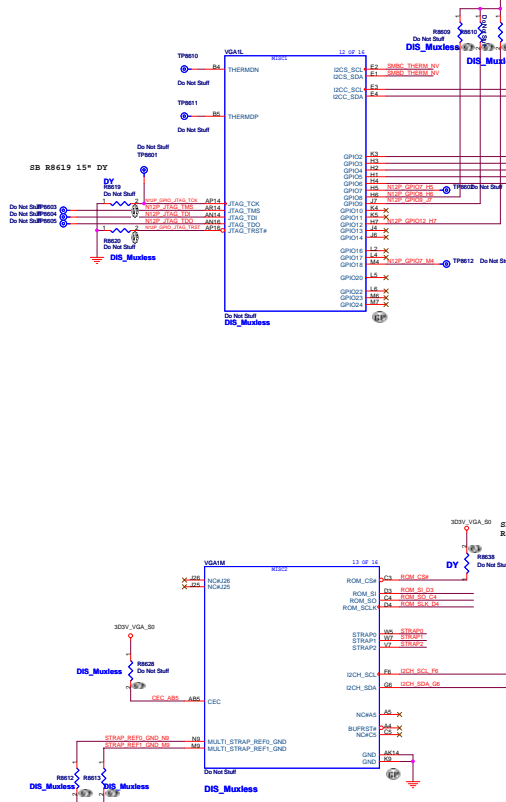
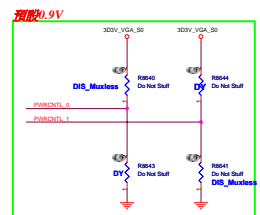
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VGA Thermal sensor P2800



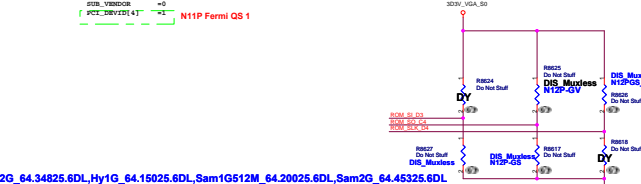
SIMS50-CP SUPPORT							
STATE	INVIDO_ALTV	INVIDO_ALTV2	N11MSEL	N11MSEL2	N11MOP1	N11PSEL	N11PSEL2
P10	0	0	0.85V	0.85V	0.85V	0.85V	0.85V
P8	0	1	0.85V	0.85V	0.85V	0.85V	0.85V
D0	1	0	1.00V	1.00V	1.00V	0.85V	0.85V



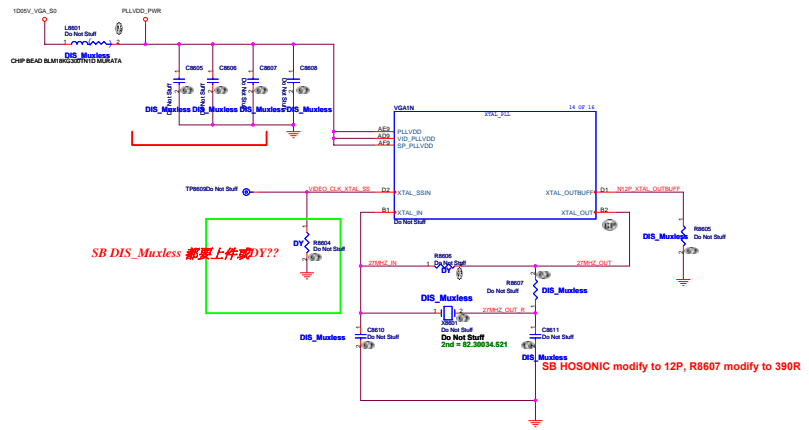
NVIDIA TABLE

	Hynix 2G 0110 128*16*8 800MHZ	Hynix 1G 0000 64*16*8 800MHZ	Samsung 1G 0011 64*16*8 800MHZ	Samsung 512 64*16*4 800MHZ	Samsung 2G 0111 128*16*8 800MHZ
RO M_SIPD R8627	34.8Kohm 64.34825.6DL	5Kohm 64.49915.6DL	20Kohm 64.20025.6DL	20Kohm 64.20025.6DL	45Kohm 64.45325.6DL

GPU\_ROM\_SI [0:15] = 0x0000 for 16bit, 0x0001 for 20bit, 0x0002 for 24bit, 0x0003 for 28bit  
 GPU\_ROM\_BO [0:15] = 0x0000 for 16bit, 0x0001 for 20bit, 0x0002 for 24bit, 0x0003 for 28bit  
 GPU\_ROM\_SCLK [0:15] = 0x0000 for 16bit, 0x0001 for 20bit, 0x0002 for 24bit, 0x0003 for 28bit



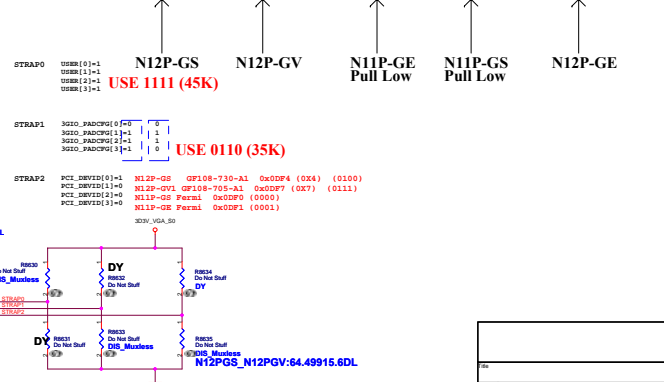
Hy2G\_64.34825.6DL, Hy1G\_64.16025.6DL, Sam1G512M\_64.20025.6DL, Sam2G\_64.45325.6DL



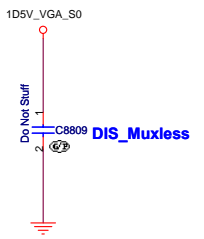
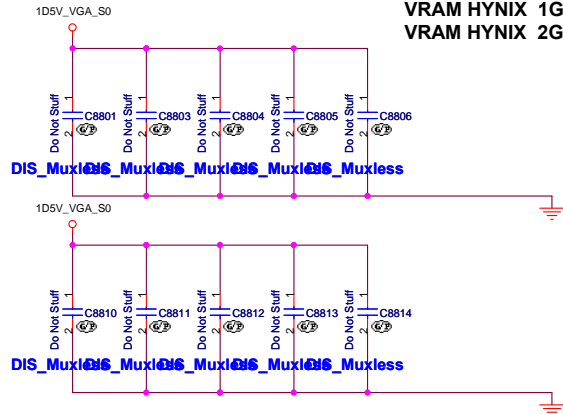
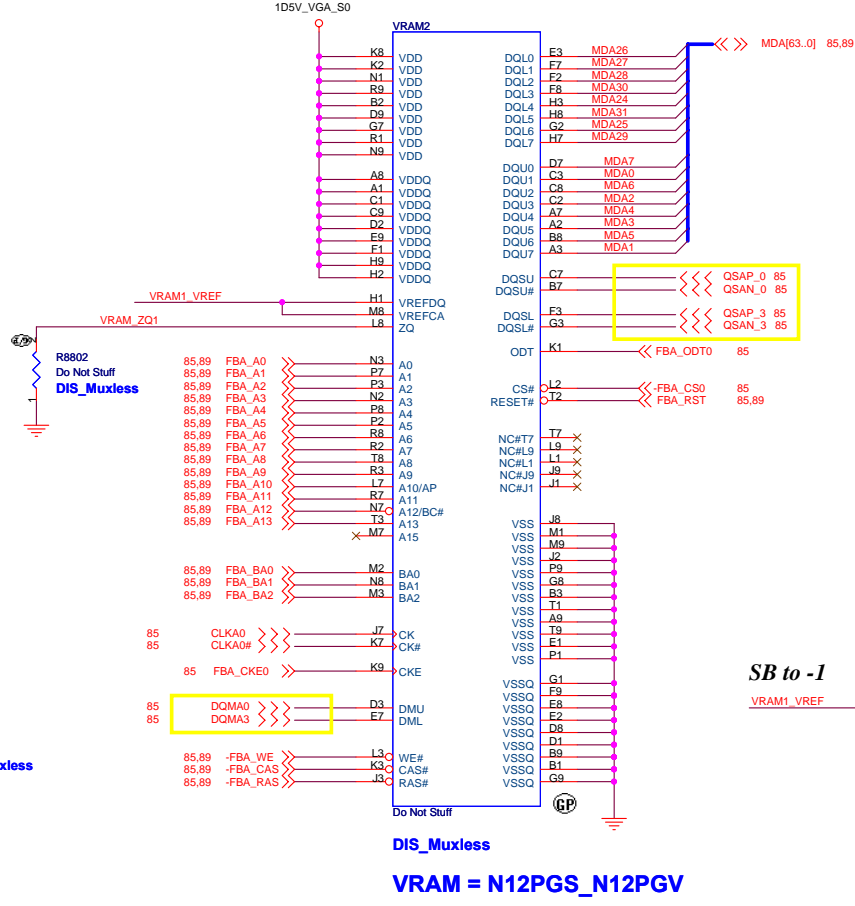
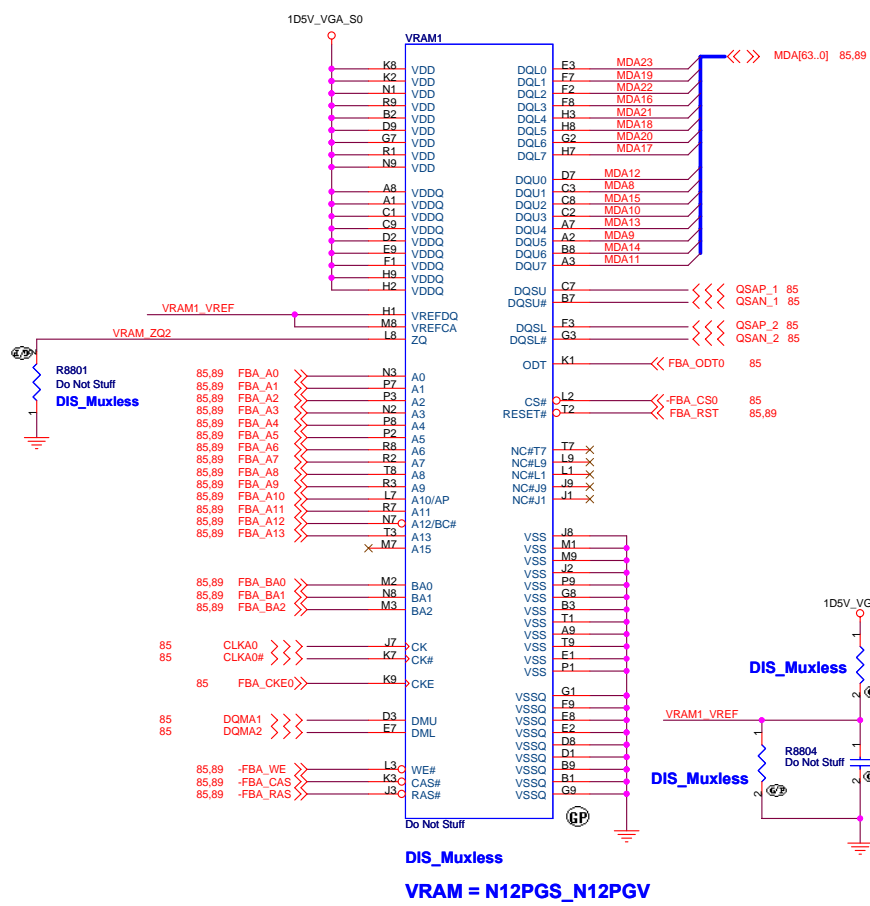
SB HOSONIC modify to 12P, R8607 modify to 390R

TABLE -1 modify N12P GV setting

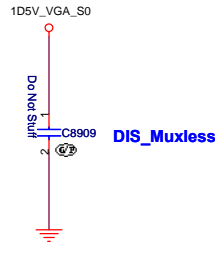
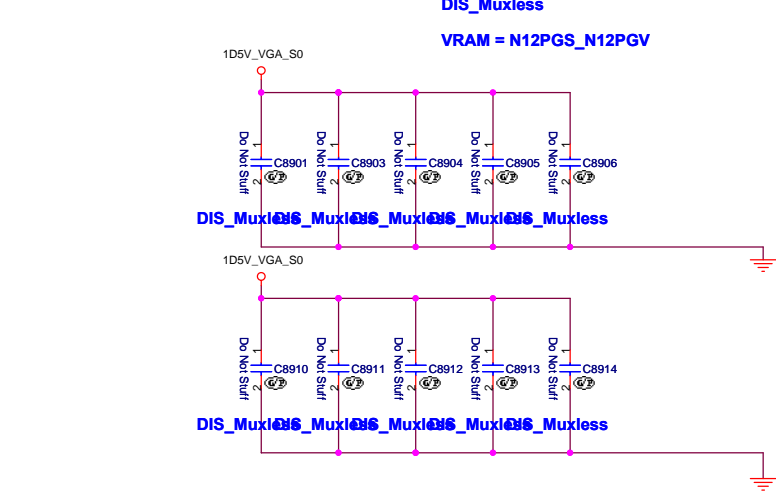
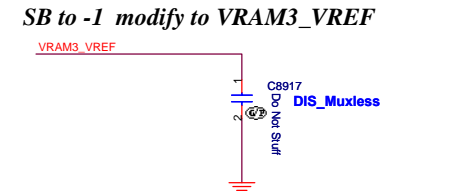
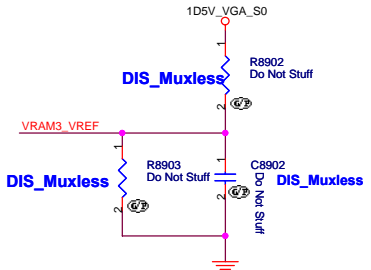
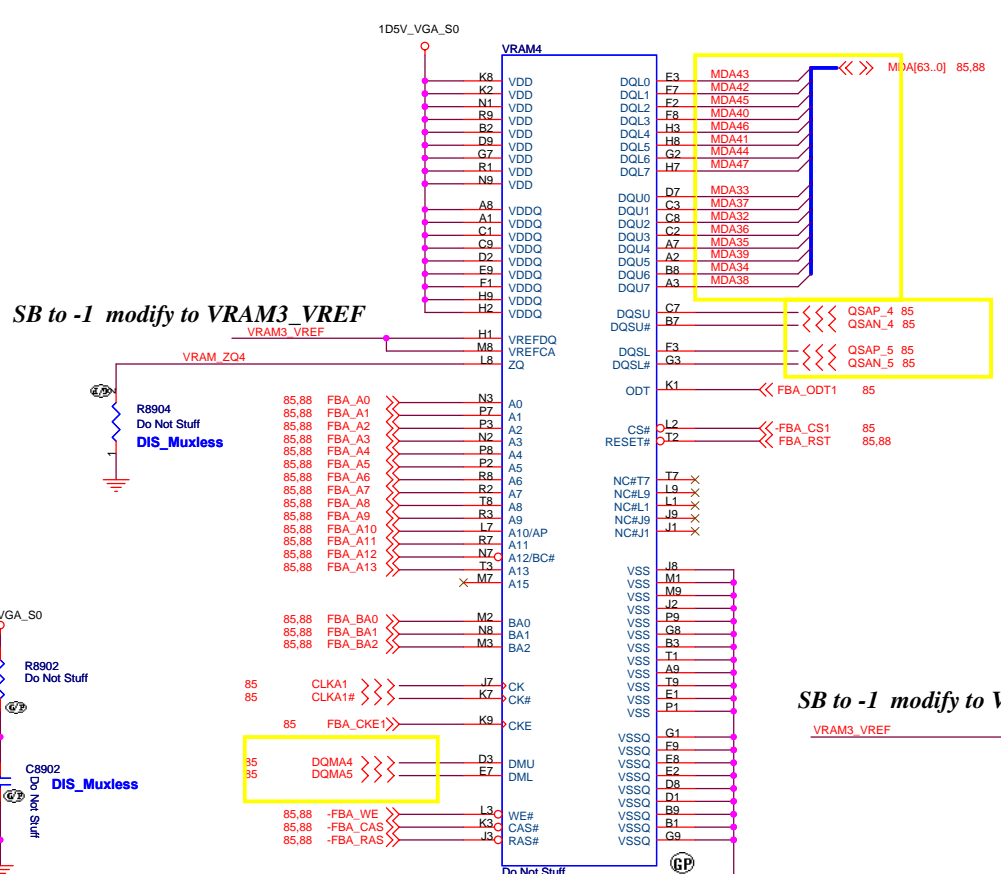
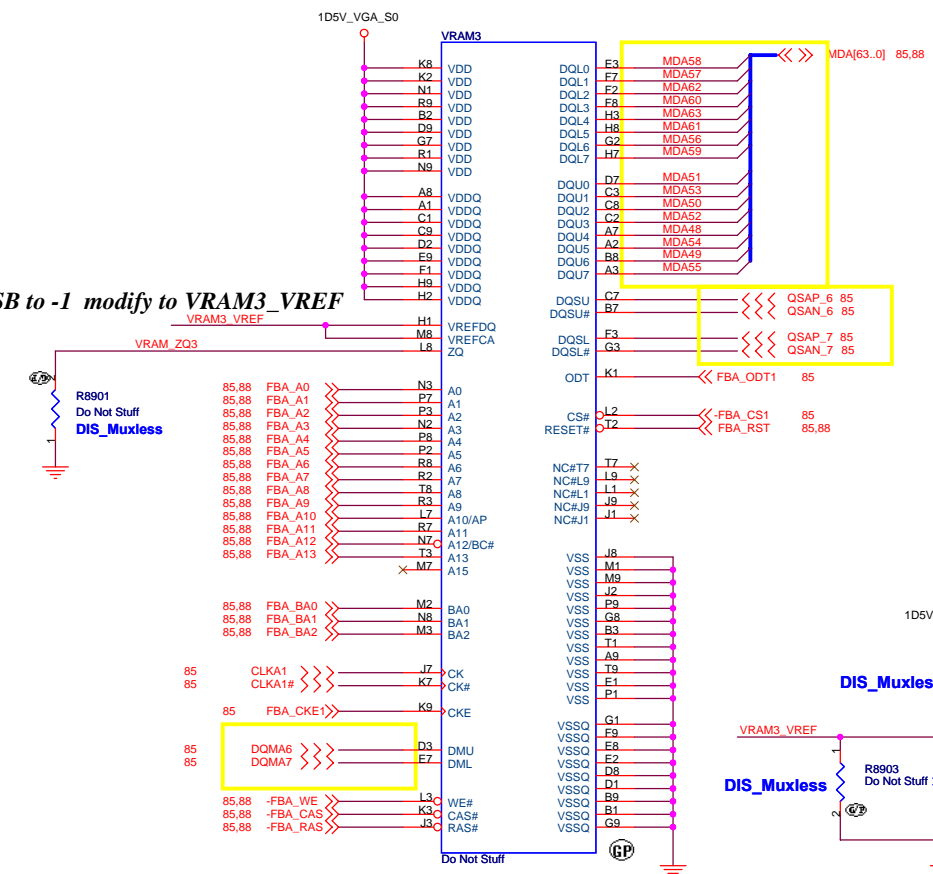
NVIDIA	71.0N12P.E0U	71.0N12P.A0U			
	N12P-GS DEV ID: 0x0DF4	N12P-GV DEV ID: 0x1050	N11P-GE Fermi DEV ID: 0x0DF1 (0001)	N11P-GS Fermi DEV ID: 0x0DF0 (0000)	N12P-GE DEV ID: 0x0DF5 (0101)
STRAP2 PU	25Kohm 64.24925.6DL	45Kohm ES 45K QS 5K 64.49915.6DL	10Kohm 63.10334.1DL	5Kohm 64.49915.6DL	30Kohm 64.30025.6DL







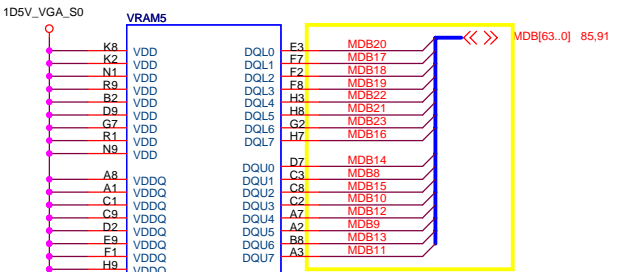
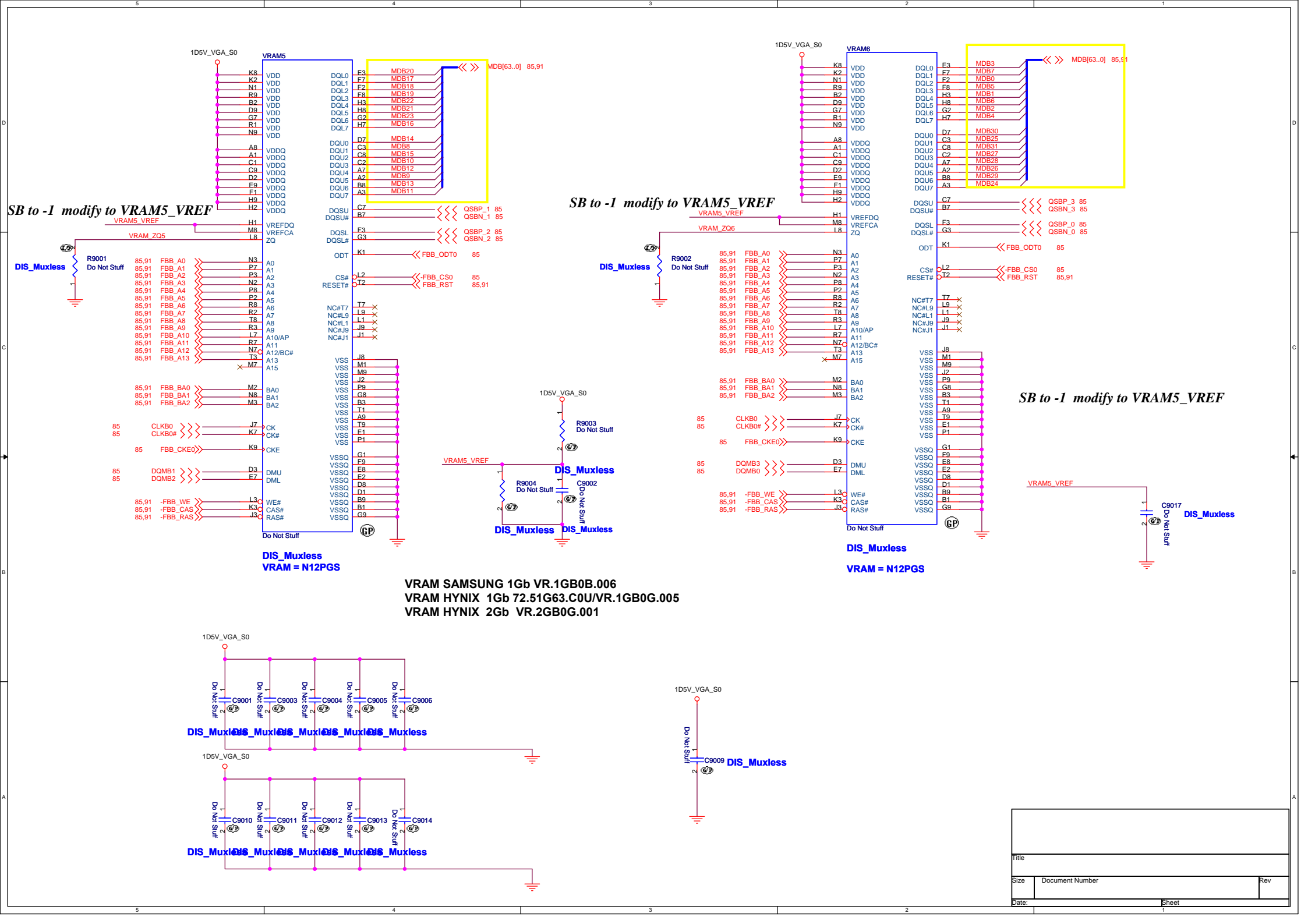
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**VRAM SAMSUNG 1Gb VR.1GB0B.006**  
**VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005**  
**VRAM HYNIX 2Gb VR.2GB0G.001**

**DIS\_Muxless SB to -1 delete R8906, R8905, modify to VRAM2\_VREF**

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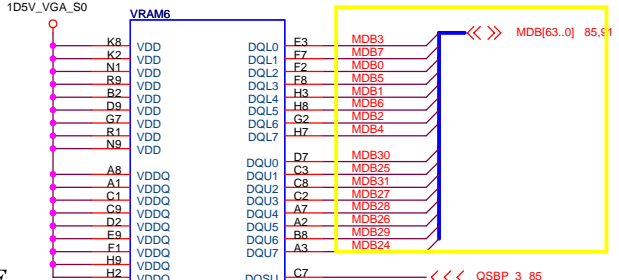


SB to -1 modify to VRAM5\_VREF

DIS\_Muxless

DIS\_Muxless  
VRAM = N12PGS

VRAM SAMSUNG 1Gb VR.1GB0B.006  
VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005  
VRAM HYNIX 2Gb VR.2GB0G.001



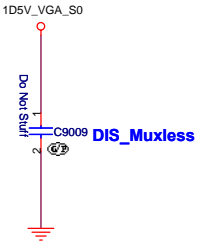
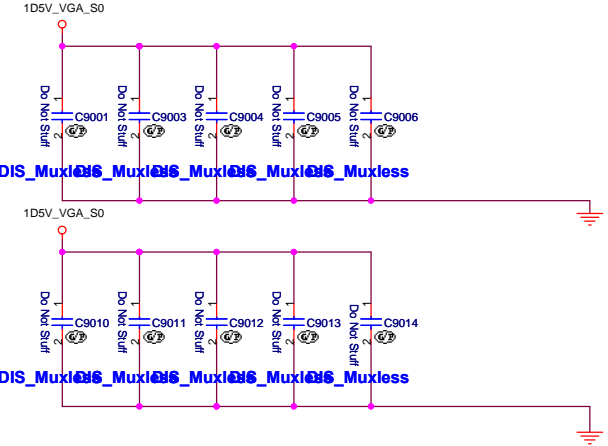
SB to -1 modify to VRAM5\_VREF

DIS\_Muxless

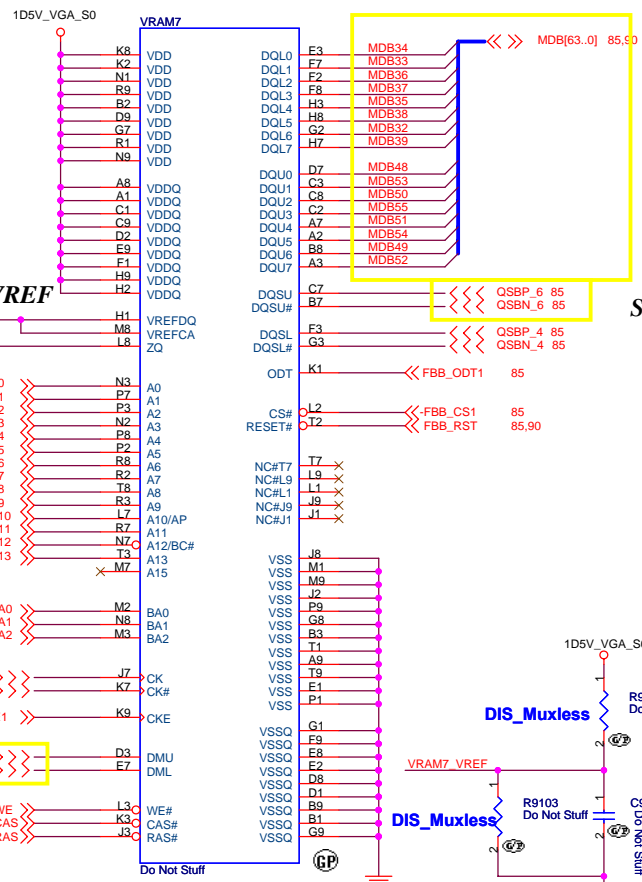
DIS\_Muxless  
VRAM = N12PGS

SB to -1 modify to VRAM5\_VREF

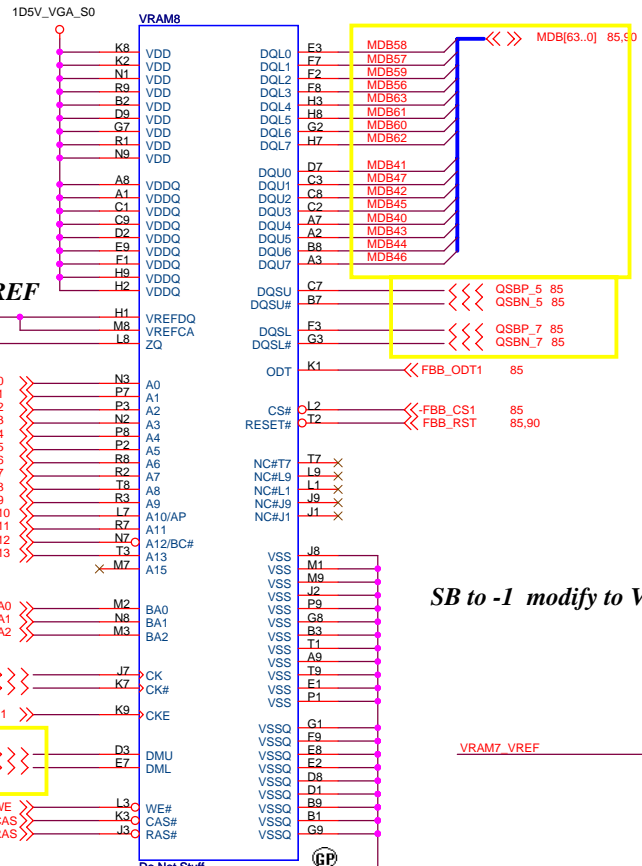
DIS\_Muxless



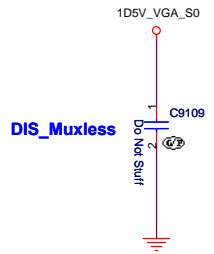
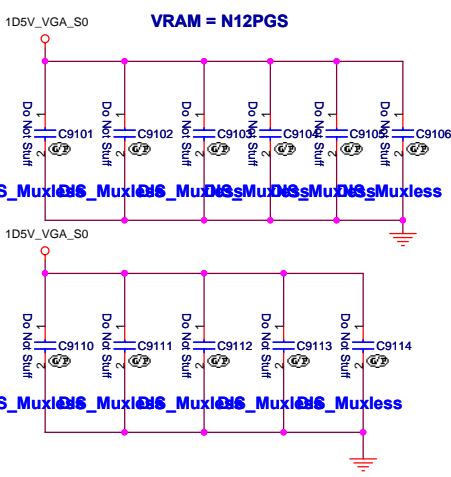
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SB to -1 modify to VRAM7\_VREF



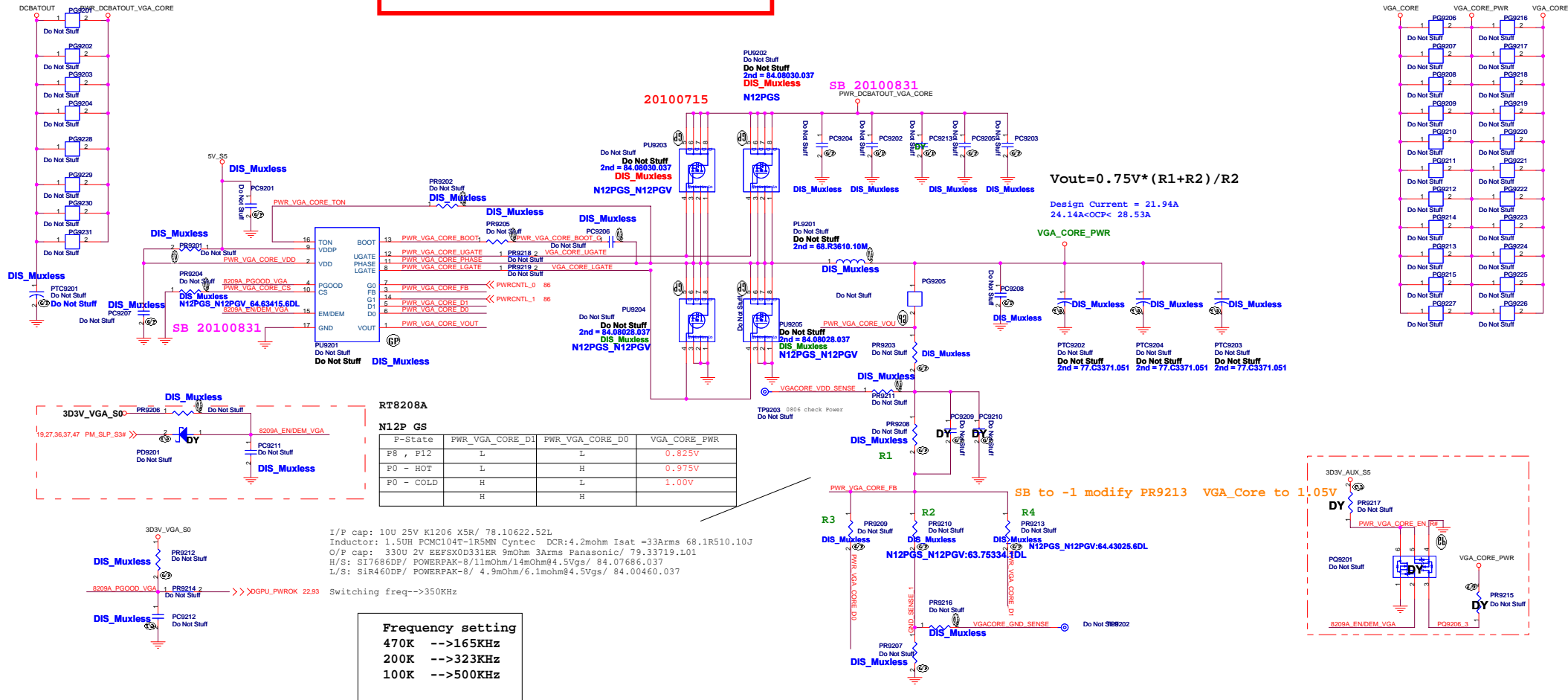
SB to -1 modify to VRAM7\_VREF



DIS\_Muxless  
 VRAM = N12PGS  
 VRAM SAMSUNG 1Gb VR.1GB0B.006  
 VRAM HYNIX 1Gb 72.51G63.C0U/VR.1GB0G.005  
 VRAM HYNIX 2Gb VR.2GB0G.001

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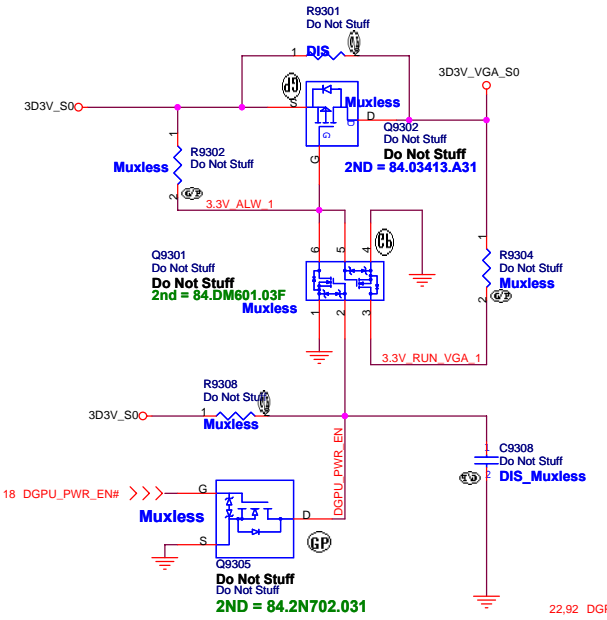
# SSID = PWR.Plane.Regulator\_GFX



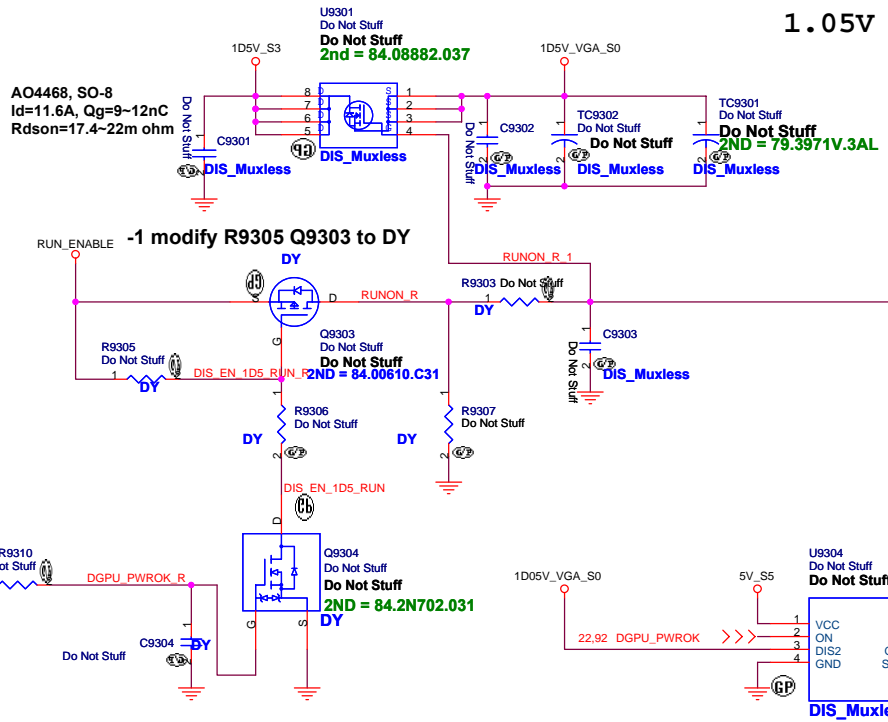
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**+3VS to 3.3V\_DELAY Transfer**

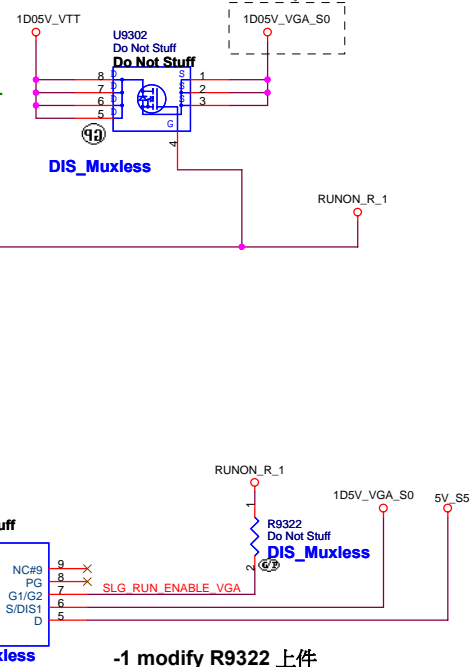


**1D5V\_VGA\_S0**

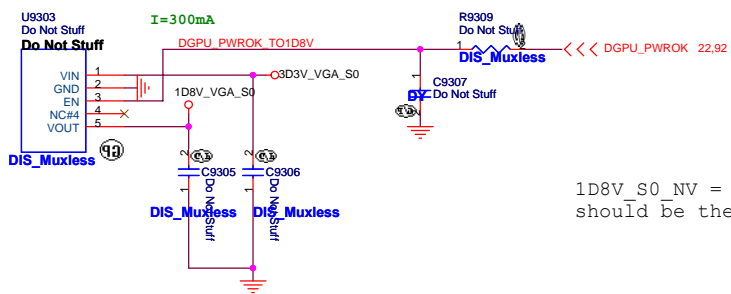


SB modify to 84.03006.A37

**1.05V to 1.05V\_VGA\_S0 Transfer**

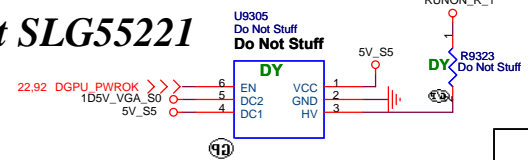


**+3VS to 1.8V Transfer**

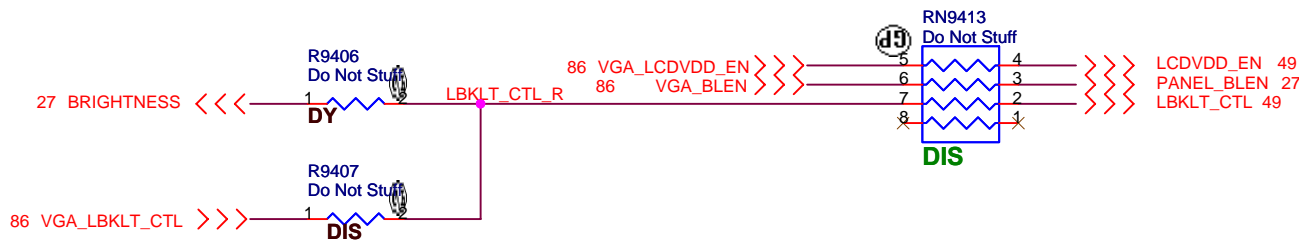
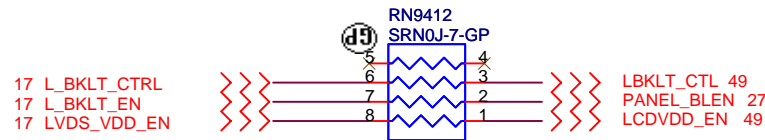
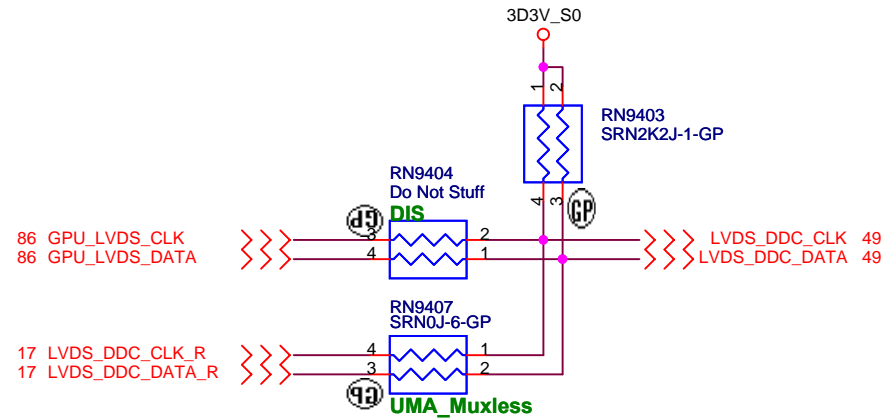
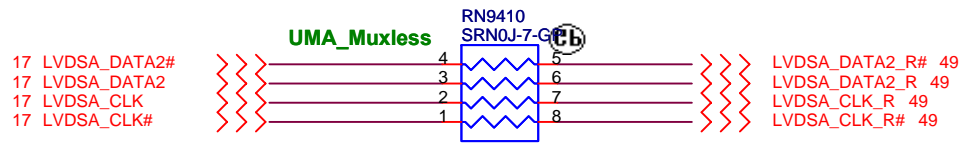
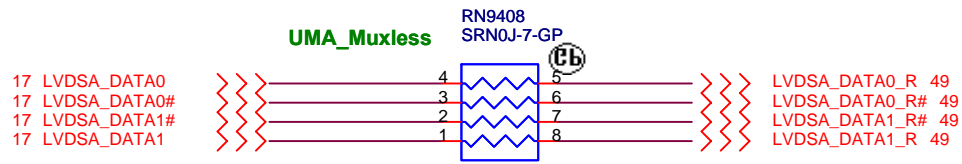
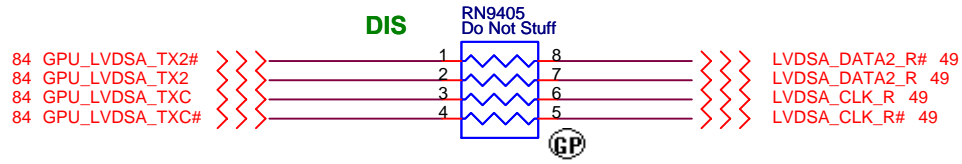
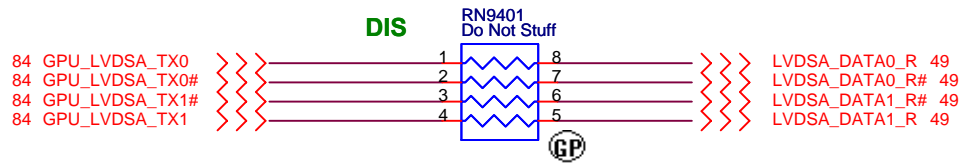


1D8V\_S0\_NV = IFPA\_IOVDD & IFPB\_IOVDD, it should be the latest ramp up rail.

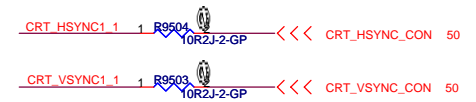
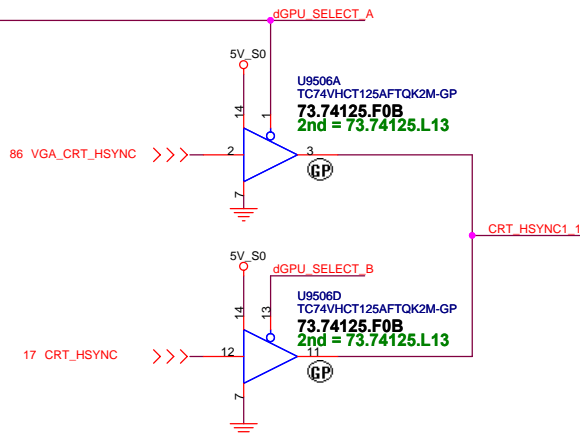
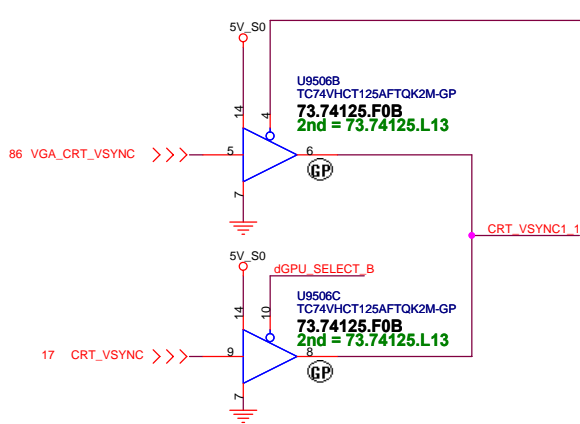
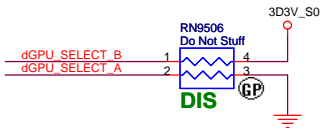
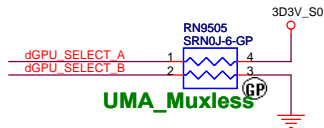
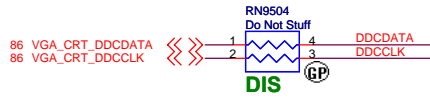
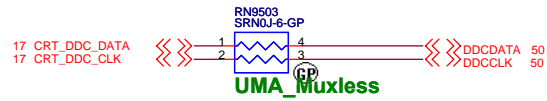
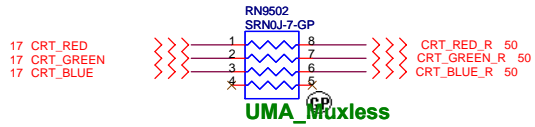
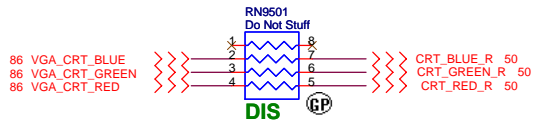
**-1 co-layout SLG55221**



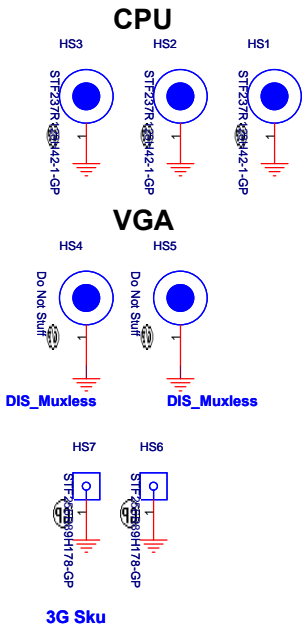
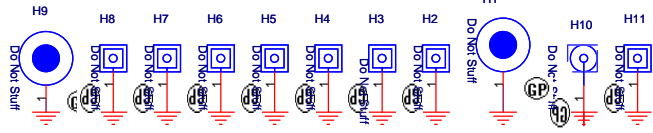
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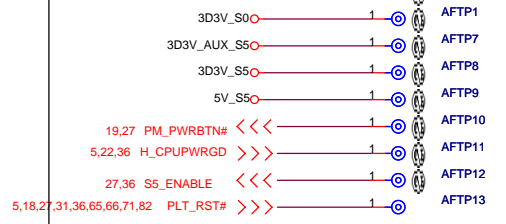
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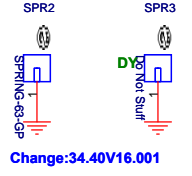
### Check test point



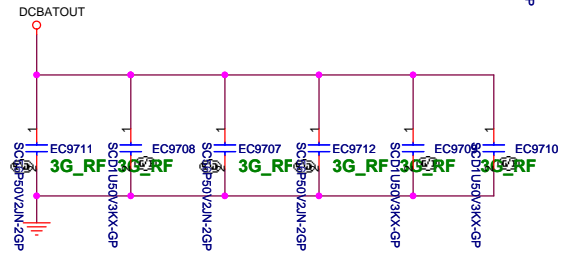
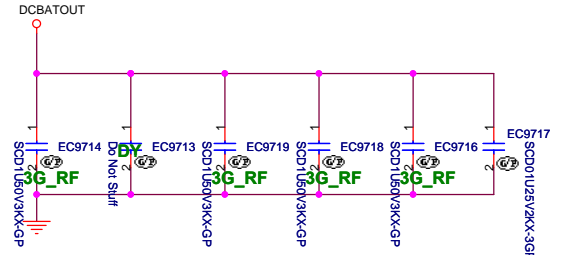
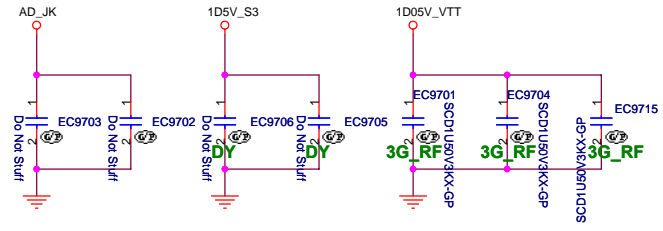
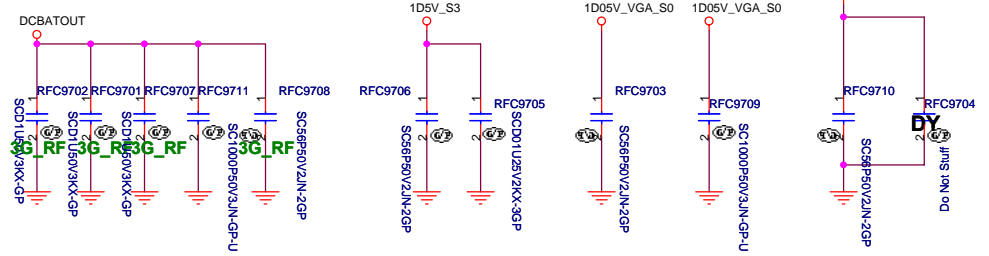
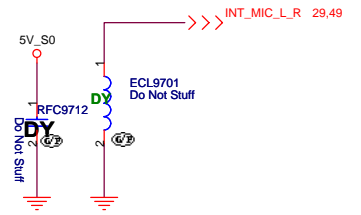
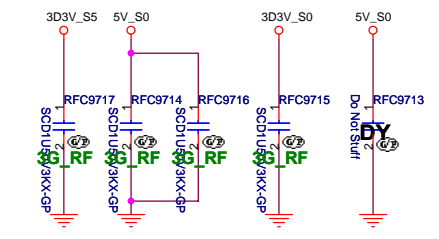
Test Point放在Dimm Door打開可量測處

### SB to -1 BOM add SPR2

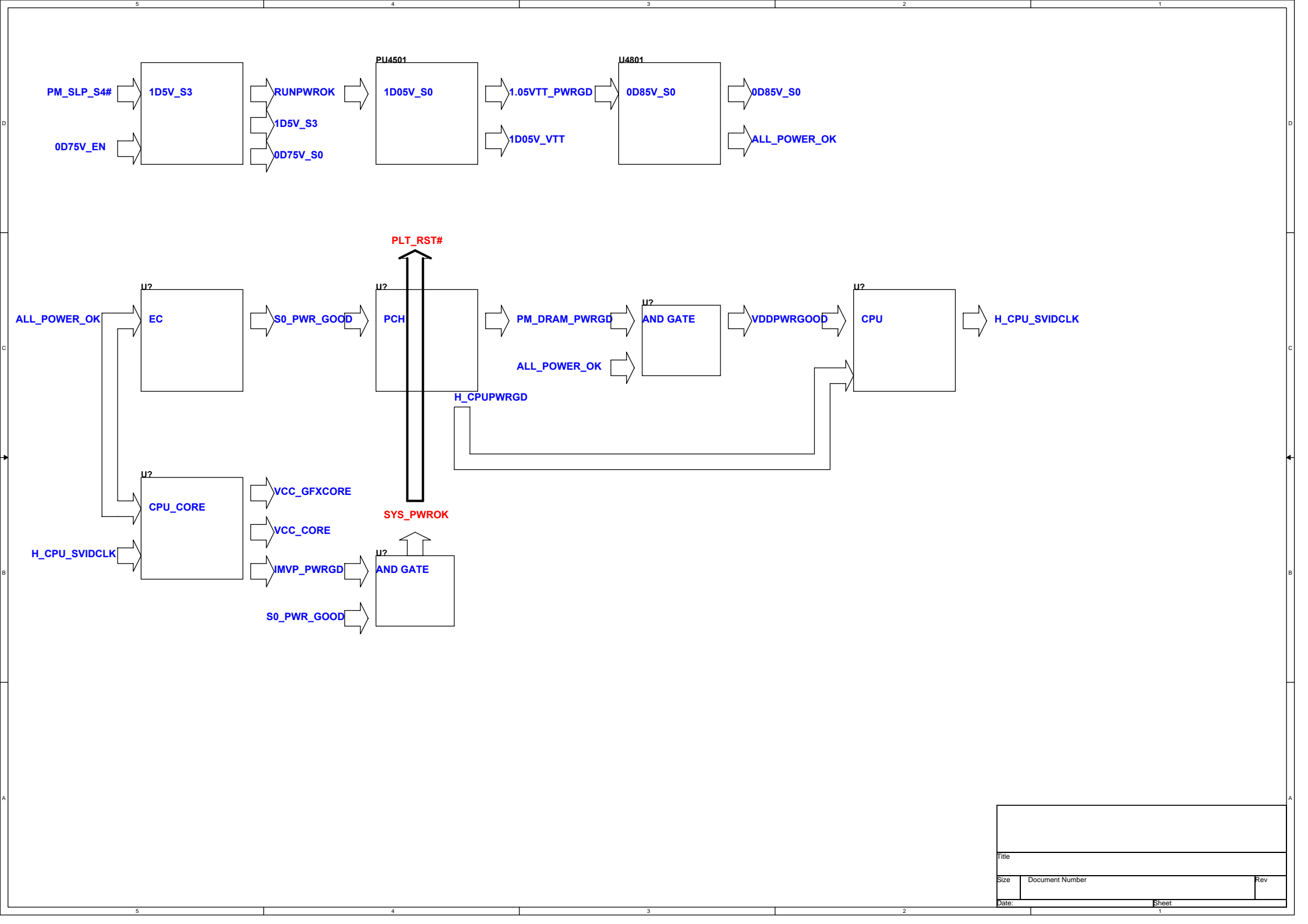
-2 delete SPR5



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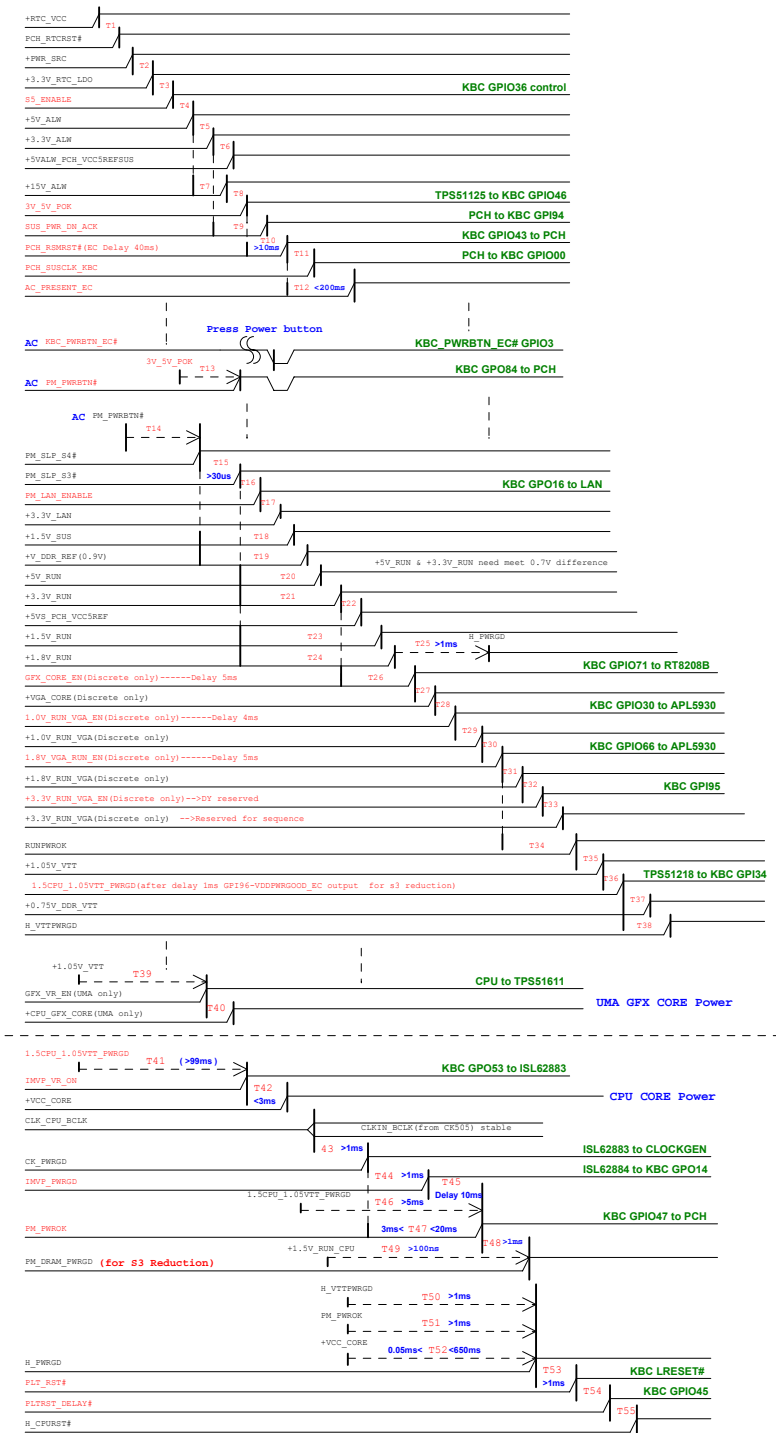


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# Intel-Power Up Sequence

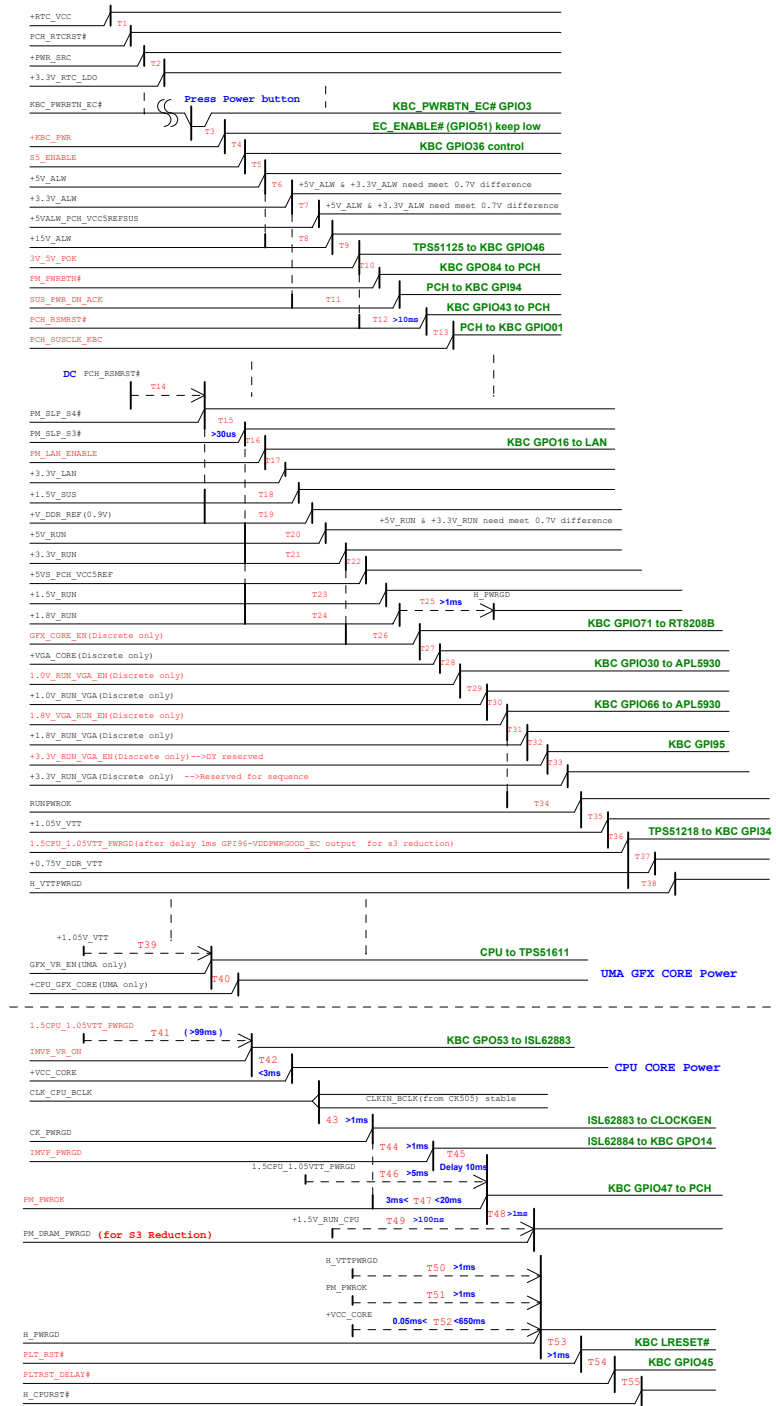
(AC mode)

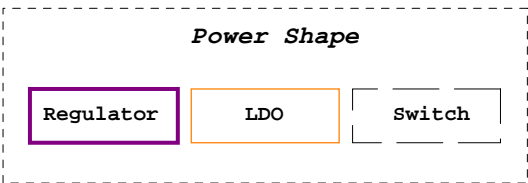
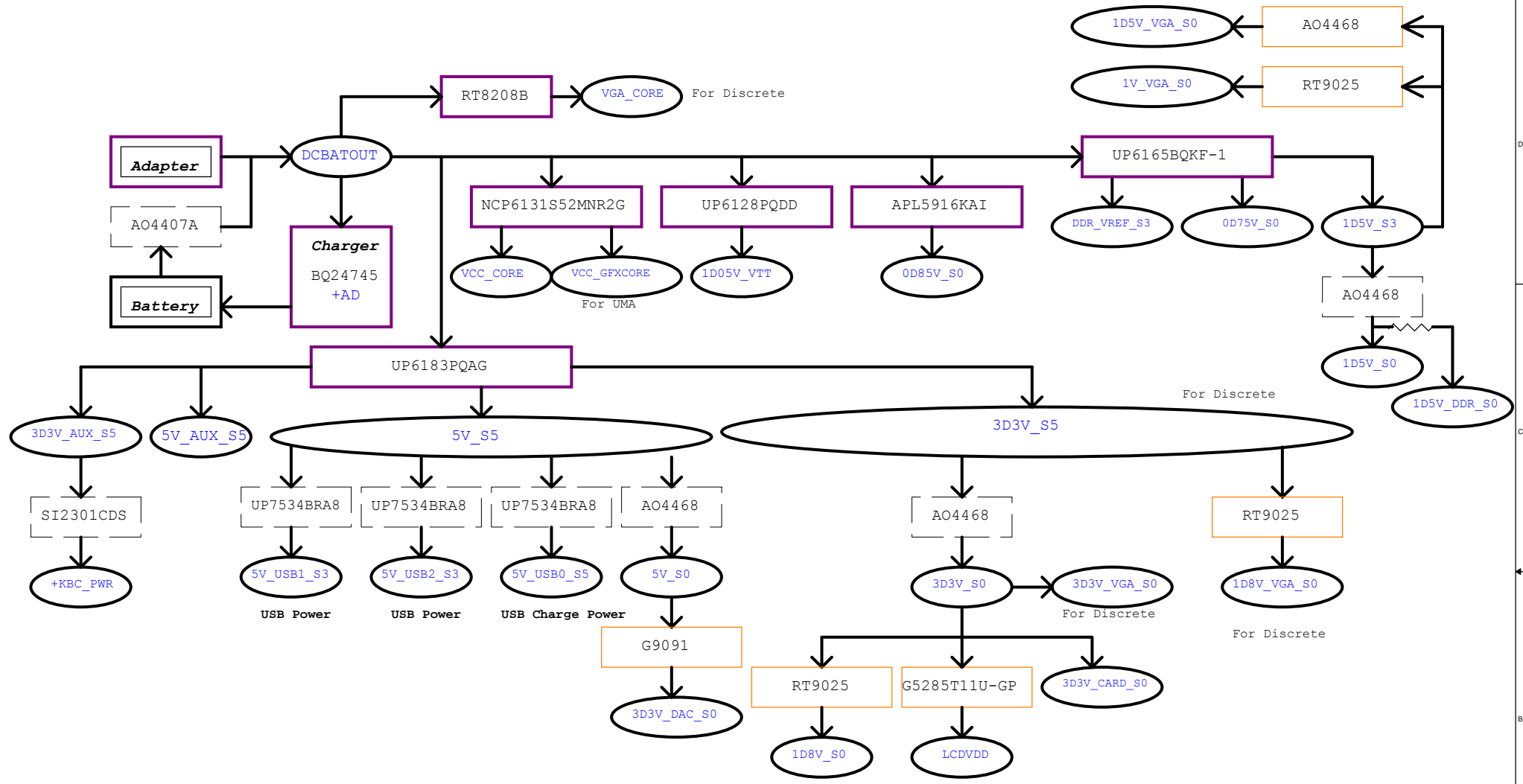
red word: KBC GPIO



(DC mode)

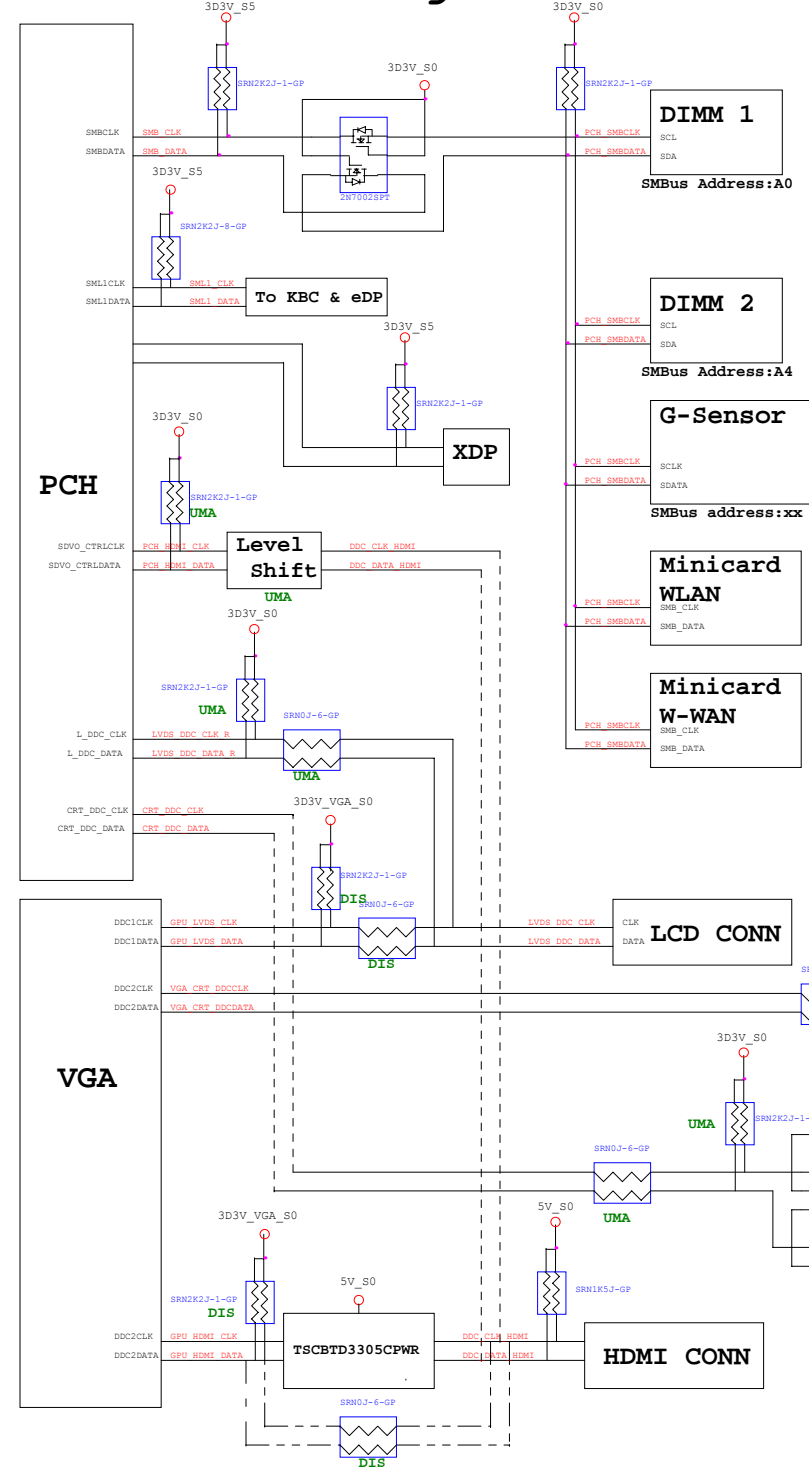
red word: KBC GPIO



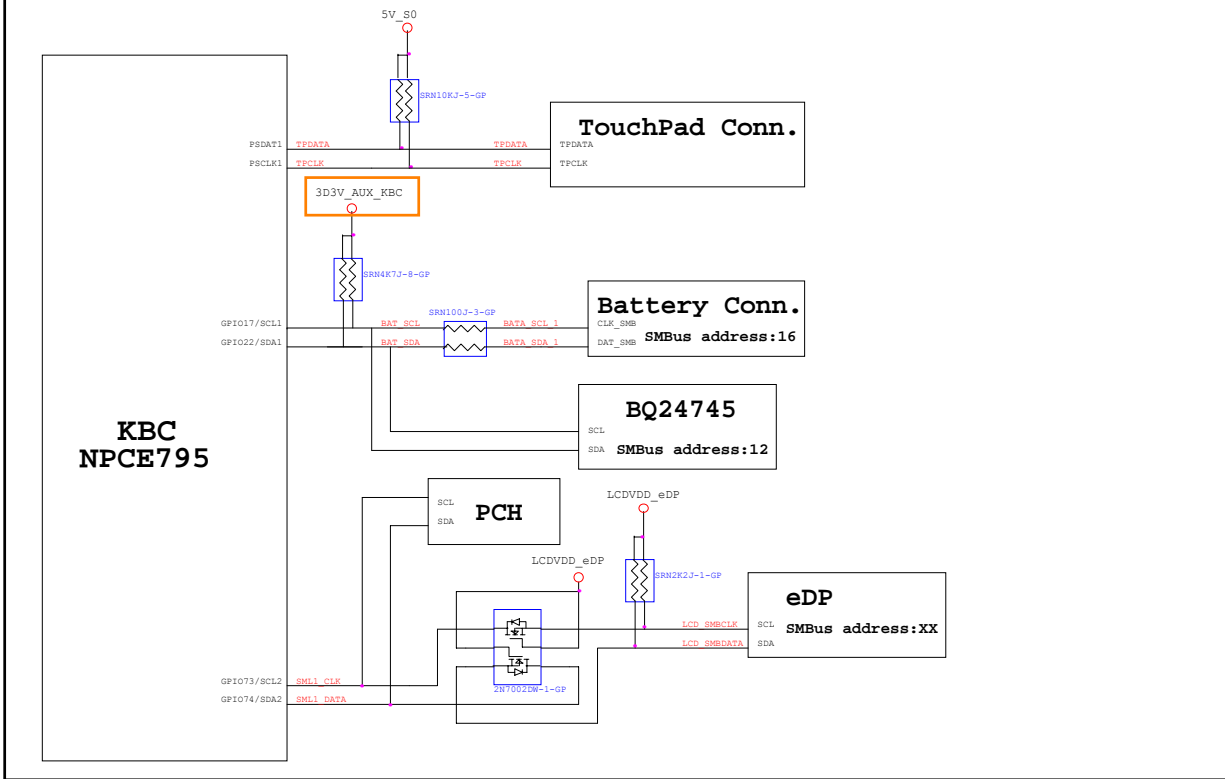


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# PCH SMBus Block Diagram



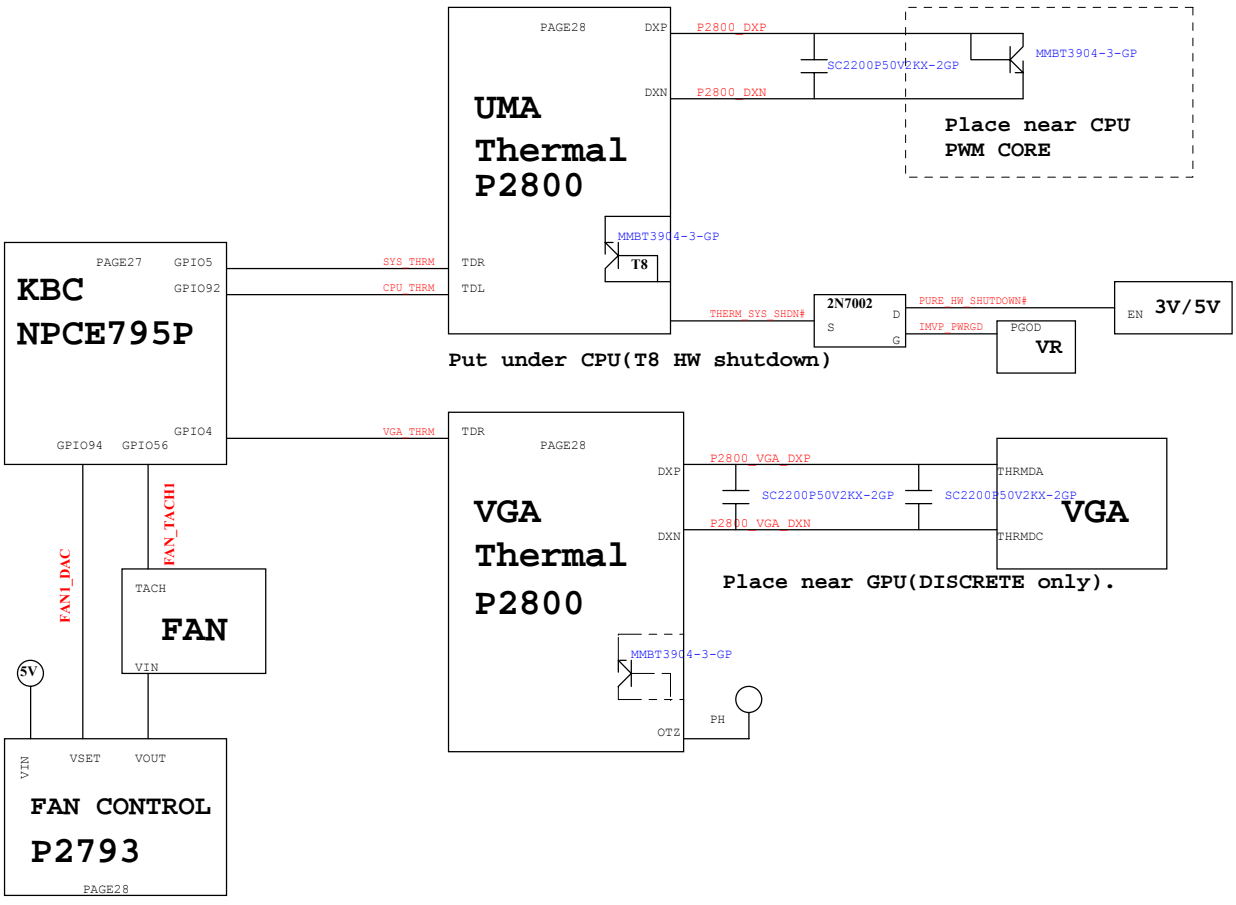
# KBC SMBus Block Diagram



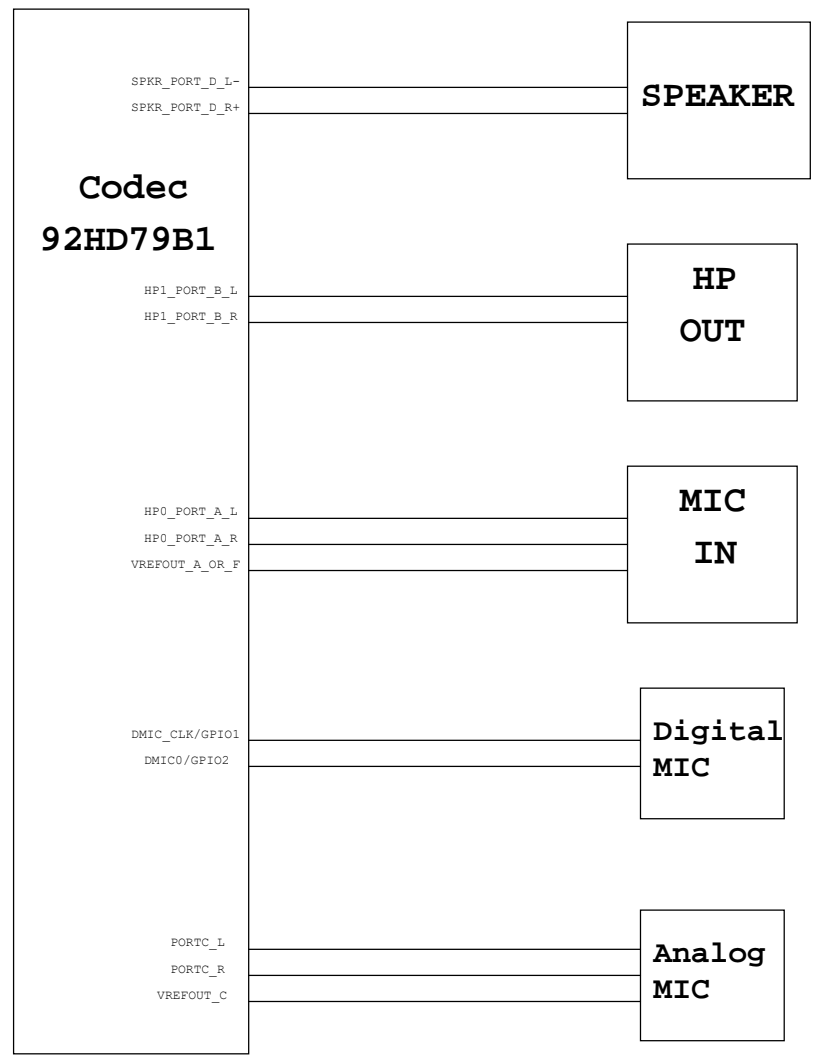
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# Thermal Block Diagram



# Audio Block Diagram



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