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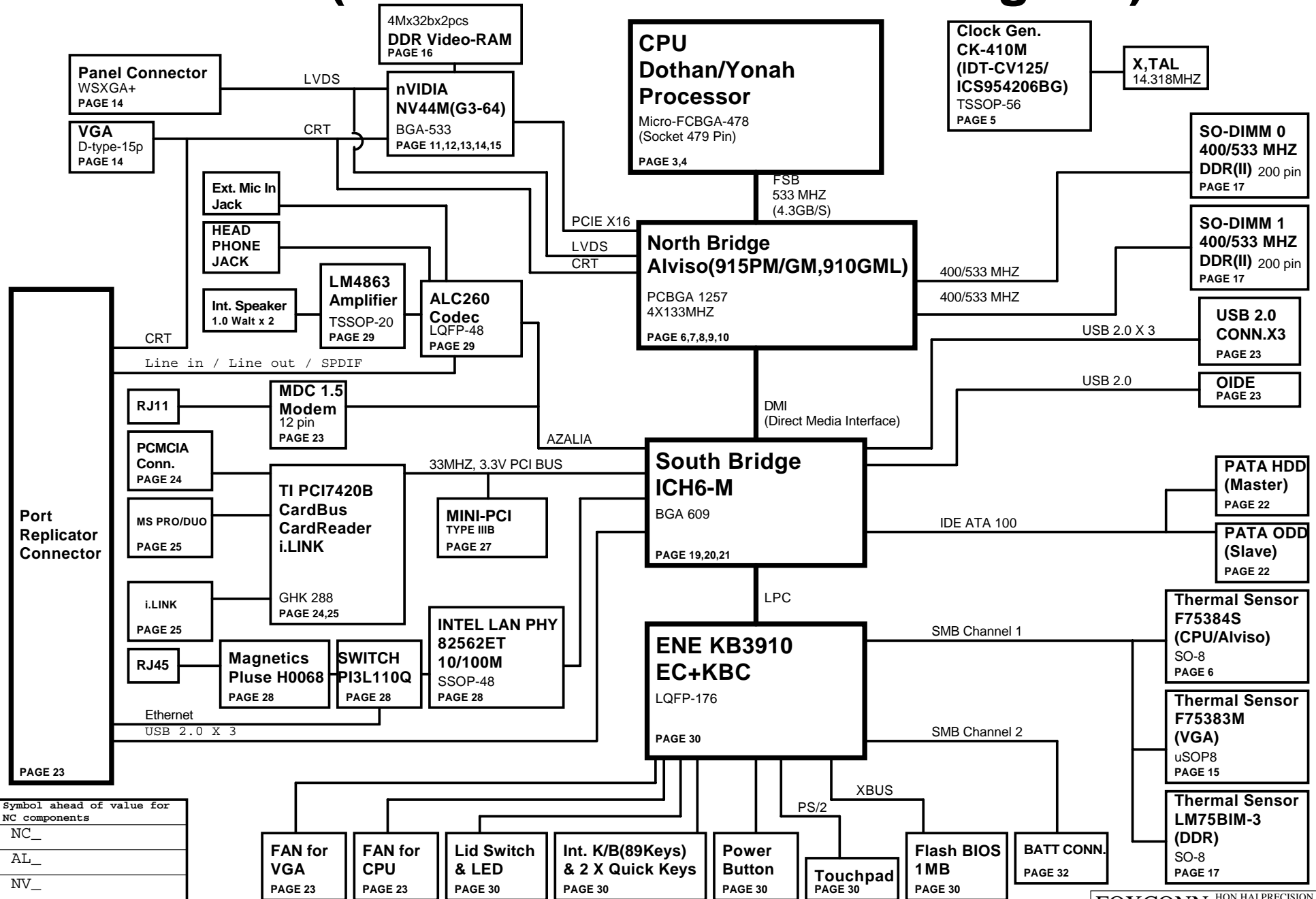
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16	NV44M(DDR F_A B_1)	0.2	050523	41	History(1)	0.2	050523
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P. Leader	Appr. by	Check by	Design by
			Alex

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Title: MS03 DVT_M/B			
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	MS03-1-01	0.2	
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Project Code & Schematics Subject:	MS03 M/B-FUBAI	PCB P/N:	1P-0055100-80SB
Project Code & Schematics Subject:	MS03 M/B-HANNSTAR	PCB P/N:	1P-0055500-80SB
Project Code & Schematics Subject:	MS03 M/B-NAN YA	PCB P/N:	1P-0055200-80SB

MS03(915PM/GM+Gfx Block Diagram)



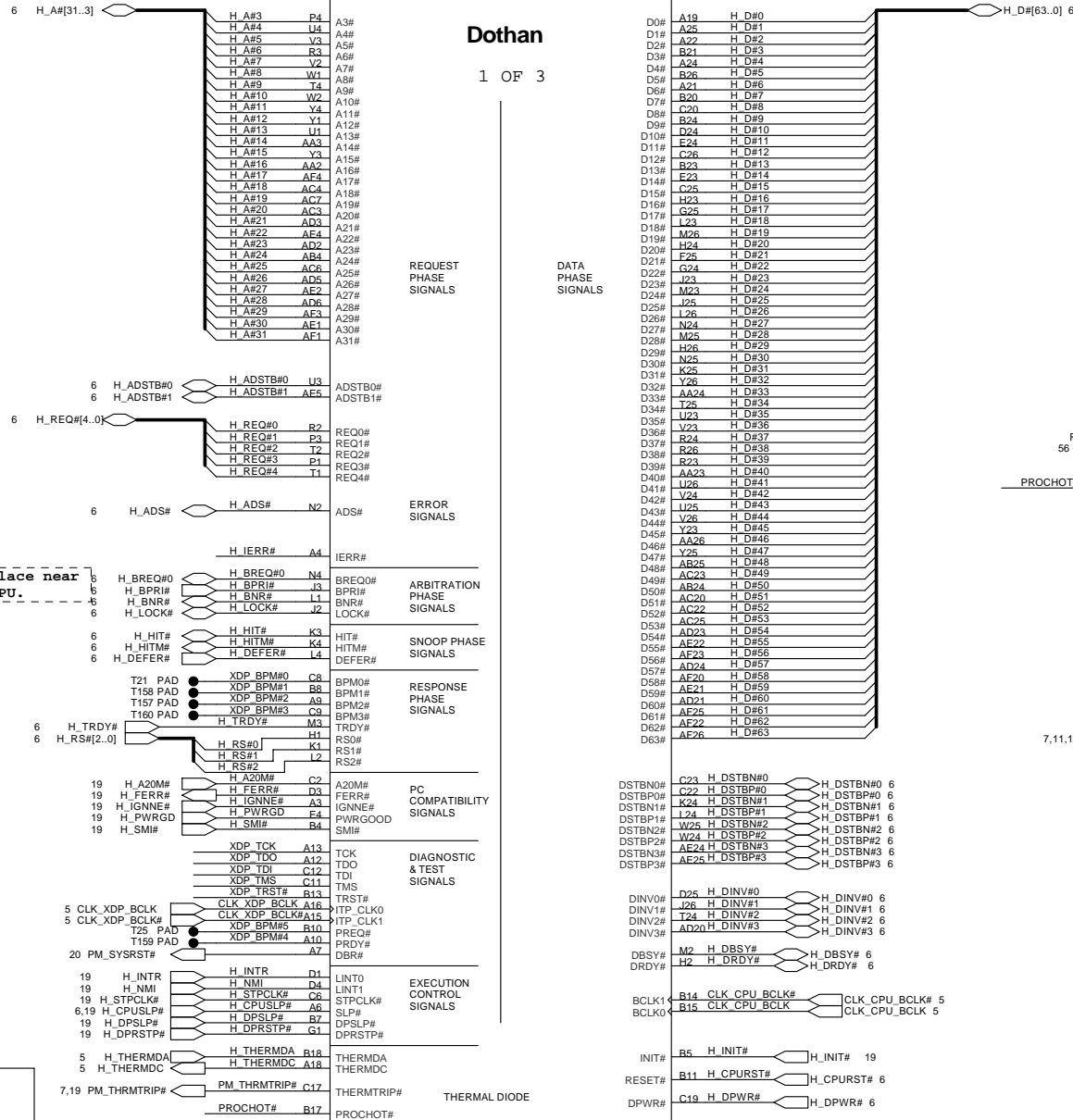
	Symbol ahead of value for NC components
ALL	NC_
915PM + NV44M	AL_
915GM or 910GML	NV_
910GML	LNC_
915PM + NV44M or 915GM	HMNC_

BOM configuration

Dothan

1 OF 3

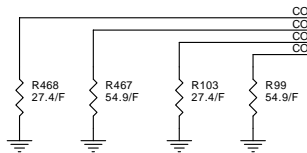
U30A



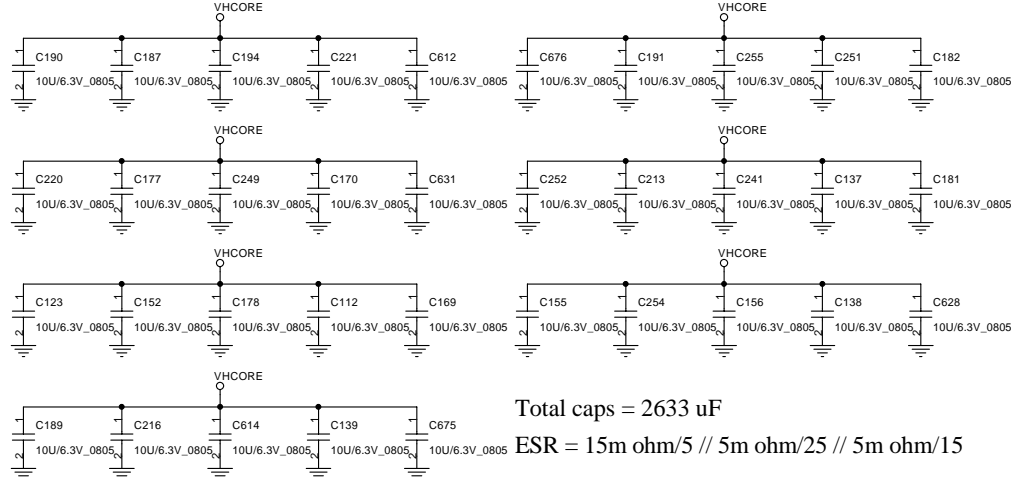
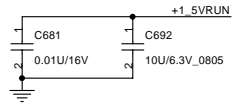
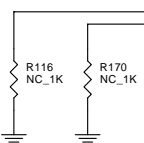
Place near CPU.

PM_THRMTRIP# should connect to ICH6-M and ALVISO without T-ing (No stub)

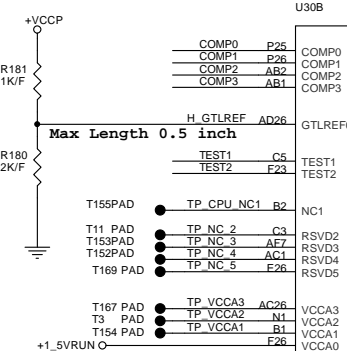
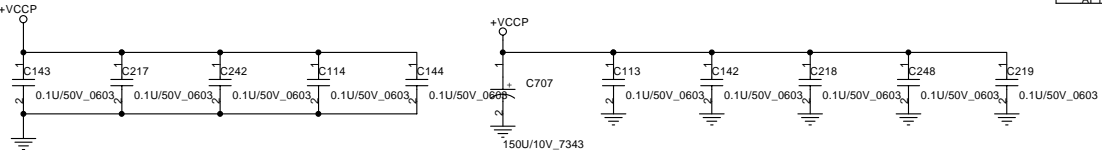
Dothan Processor



Place pull-down resistors within 0.5" of COMP pins

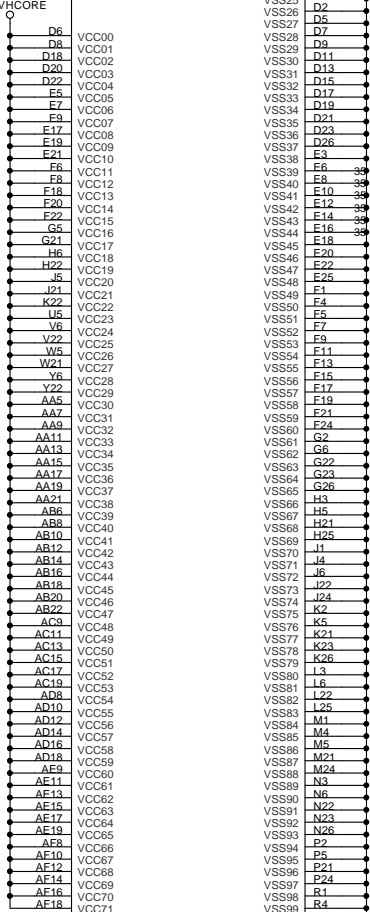


Total caps = 2633 uF
ESR = 15m ohm/5 // 5m ohm/25 // 5m ohm/15



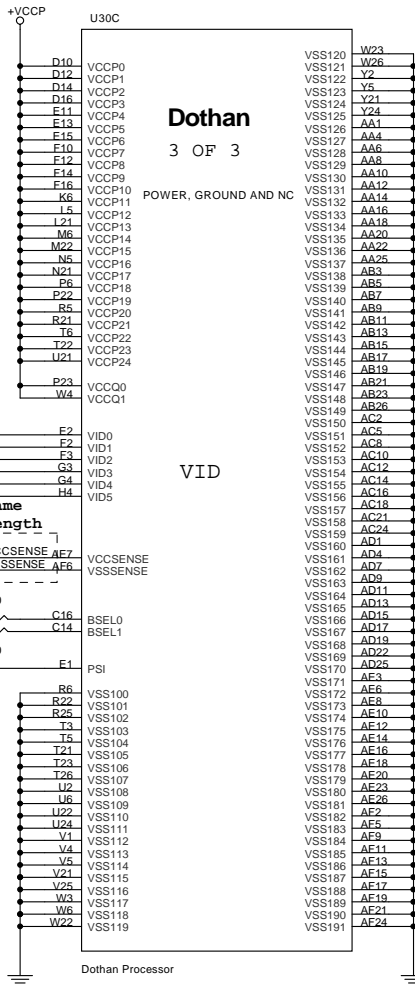
Dothan
2 OF 3

POWER, GROUND, RESERVED SIGNALS



Dothan
3 OF 3

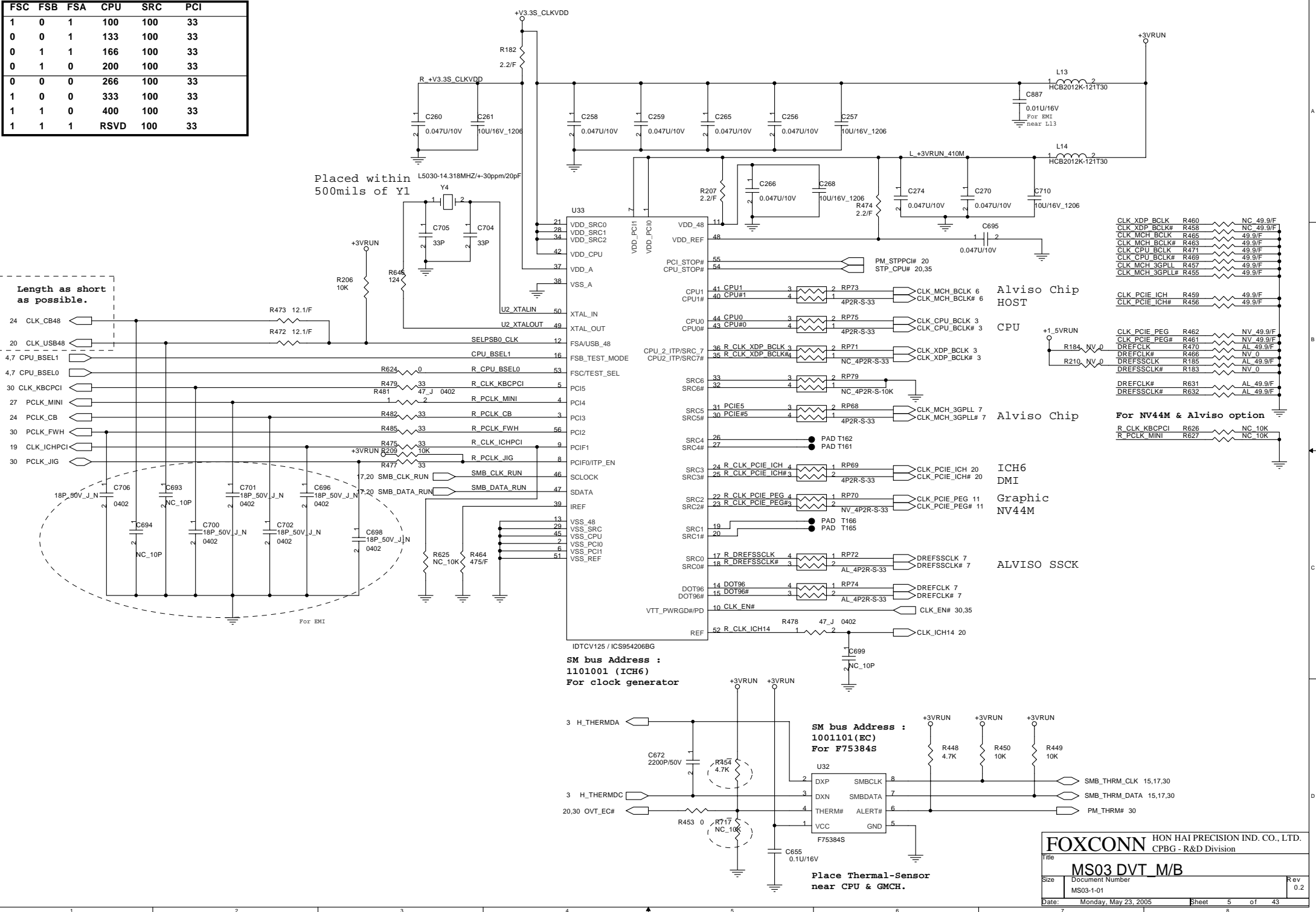
POWER, GROUND AND NC



FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	RSVD	100	33

Placed within
500mils of Y1

Length as short
as possible.



SM bus Address :
1101001 (ICH6)
For clock generator

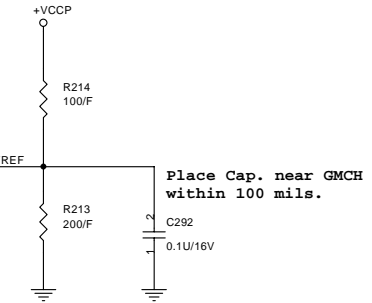
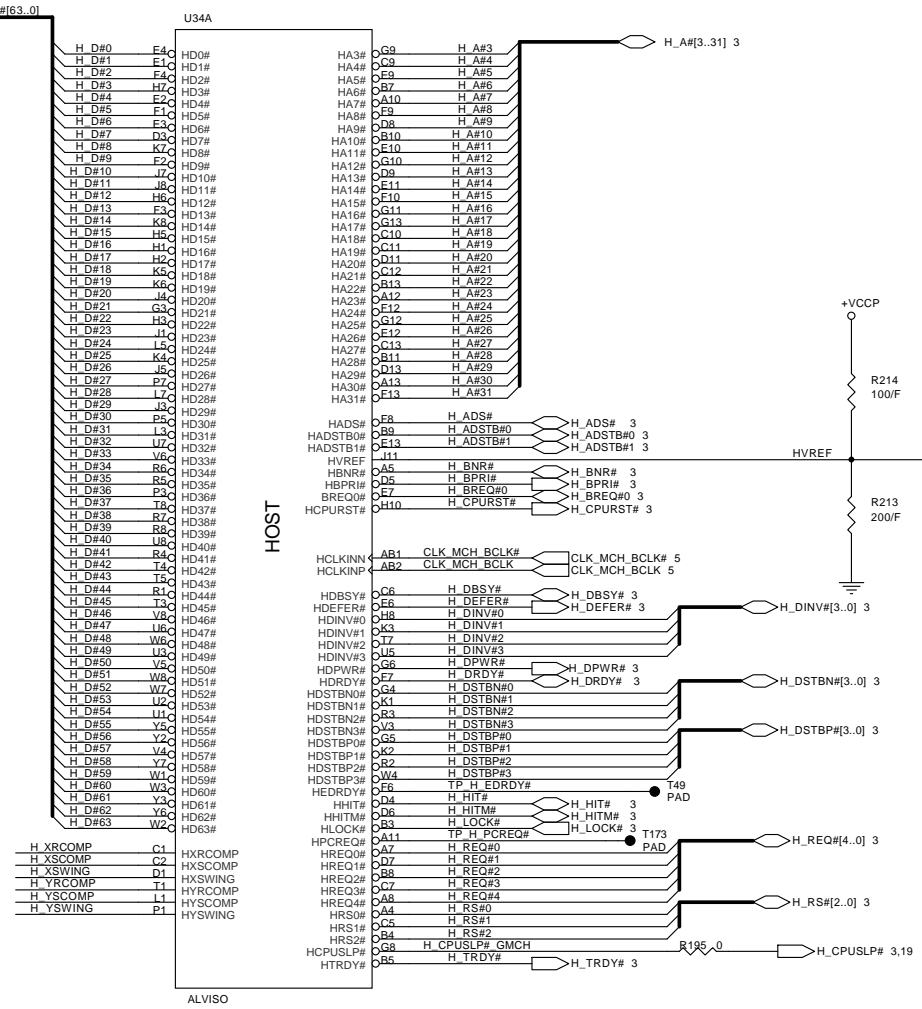
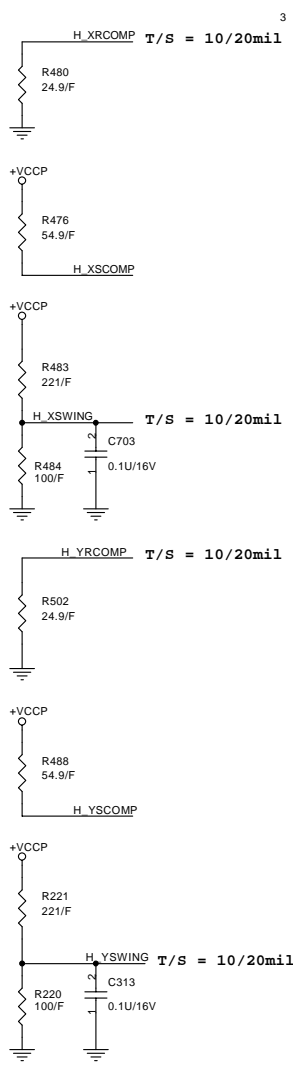
SM bus Address :
1001101 (EC)
For F75384S

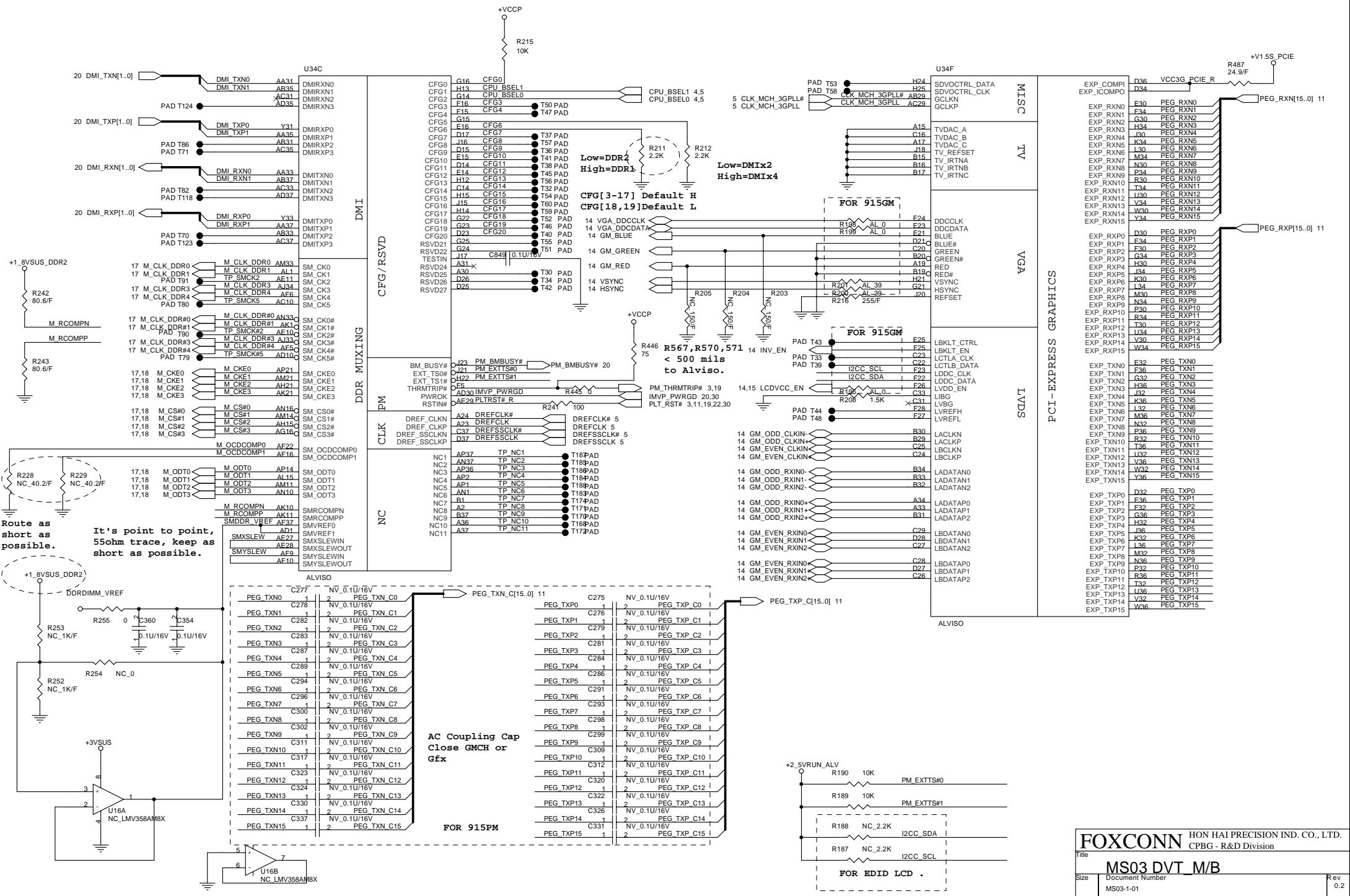
Place Thermal-Sensor
near CPU & GMCH.

CLK_XDP_BCLK	R460	NC	49.9/F
CLK_XDP_BCLK#	R458	NC	49.9/F
CLK_MCH_BCLK	R465	NC	49.9/F
CLK_MCH_BCLK#	R463	NC	49.9/F
CLK_CPU_BCLK	R471	NC	49.9/F
CLK_CPU_BCLK#	R469	NC	49.9/F
CLK_MCH_3GPLL	R457	NC	49.9/F
CLK_MCH_3GPLL#	R455	NC	49.9/F

CLK_PCIE_PEG	R462	NV	49.9/F
CLK_PCIE_PEG#	R461	NV	49.9/F
DREFCLK	R470	AL	49.9/F
DREFCLK#	R466	NV	0
DREFSSCLK	R185	AL	49.9/F
DREFSSCLK#	R183	NV	0
DREFCLK#	R631	AL	49.9/F
DREFSSCLK#	R632	AL	49.9/F

For NV44M & Alviso option
R_CLK_KBCPCI R626 NC_10K
R_PCLK_MINI R627 NC_10K





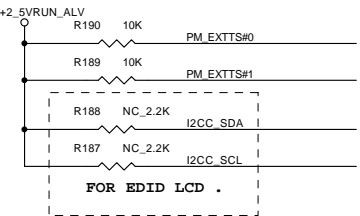
Route as short as possible. It's point to point, 55ohm trace, keep as short as possible.

ALVISO

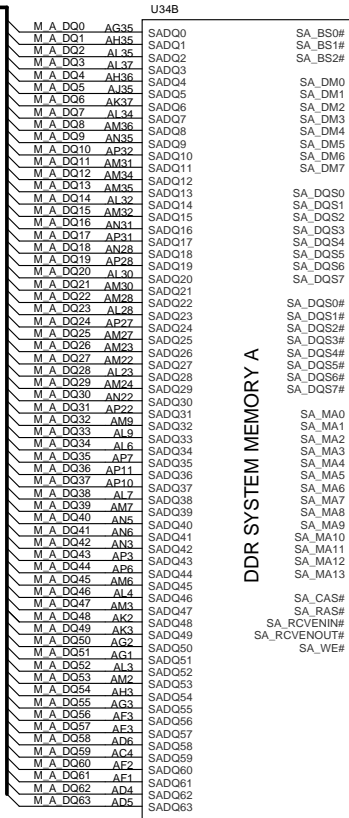
PEG TXN0	C277	NV_0.1U/16V	PEG TXN C0	C275	NV_0.1U/16V	PEG TXP C0
PEG TXN1	C278	NV_0.1U/16V	PEG TXN C1	C276	NV_0.1U/16V	PEG TXP C1
PEG TXN2	C282	NV_0.1U/16V	PEG TXN C2	C279	NV_0.1U/16V	PEG TXP C2
PEG TXN3	C283	NV_0.1U/16V	PEG TXN C3	C281	NV_0.1U/16V	PEG TXP C3
PEG TXN4	C287	NV_0.1U/16V	PEG TXN C4	C284	NV_0.1U/16V	PEG TXP C4
PEG TXN5	C289	NV_0.1U/16V	PEG TXN C5	C286	NV_0.1U/16V	PEG TXP C5
PEG TXN6	C294	NV_0.1U/16V	PEG TXN C6	C291	NV_0.1U/16V	PEG TXP C6
PEG TXN7	C296	NV_0.1U/16V	PEG TXN C7	C293	NV_0.1U/16V	PEG TXP C7
PEG TXN8	C300	NV_0.1U/16V	PEG TXN C8	C298	NV_0.1U/16V	PEG TXP C8
PEG TXN9	C302	NV_0.1U/16V	PEG TXN C9	C299	NV_0.1U/16V	PEG TXP C9
PEG TXN10	C311	NV_0.1U/16V	PEG TXN C10	C309	NV_0.1U/16V	PEG TXP C10
PEG TXN11	C317	NV_0.1U/16V	PEG TXN C11	C312	NV_0.1U/16V	PEG TXP C11
PEG TXN12	C323	NV_0.1U/16V	PEG TXN C12	C320	NV_0.1U/16V	PEG TXP C12
PEG TXN13	C324	NV_0.1U/16V	PEG TXN C13	C322	NV_0.1U/16V	PEG TXP C13
PEG TXN14	C330	NV_0.1U/16V	PEG TXN C14	C326	NV_0.1U/16V	PEG TXP C14
PEG TXN15	C337	NV_0.1U/16V	PEG TXN C15	C331	NV_0.1U/16V	PEG TXP C15

FOR 915PM

AC Coupling Cap Close GMCH or Gfx



17 M_A_DQ[63..0]

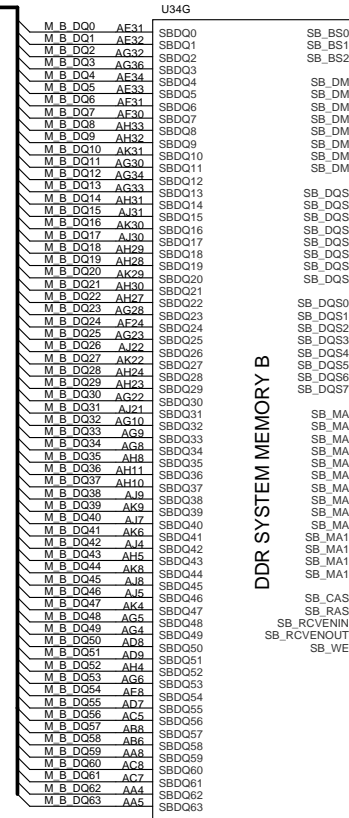


U34B

DDR SYSTEM MEMORY A

ALVISO

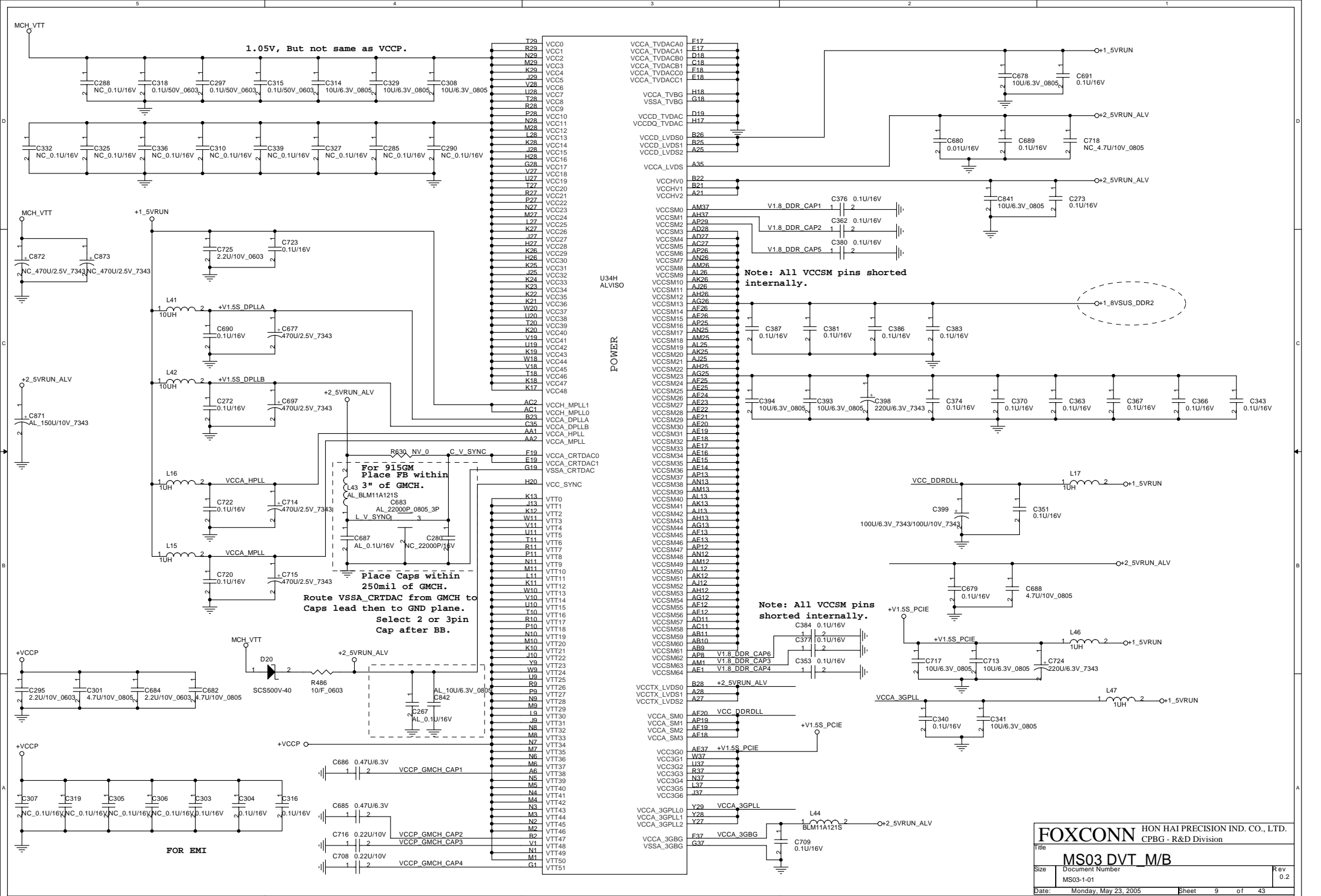
17 M_B_DQ[63..0]



U34G

DDR SYSTEM MEMORY B

ALVISO

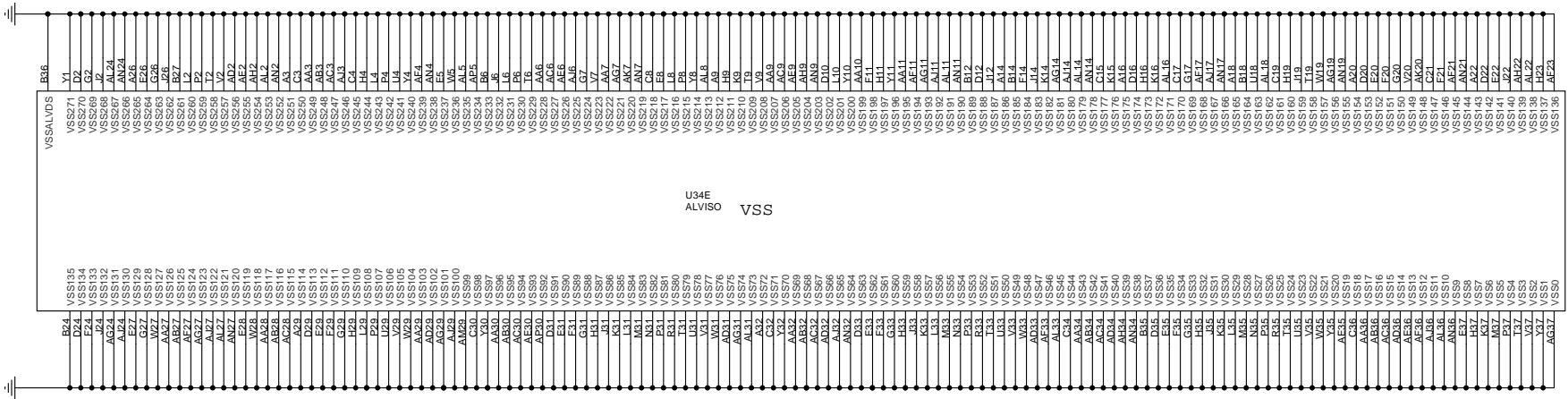


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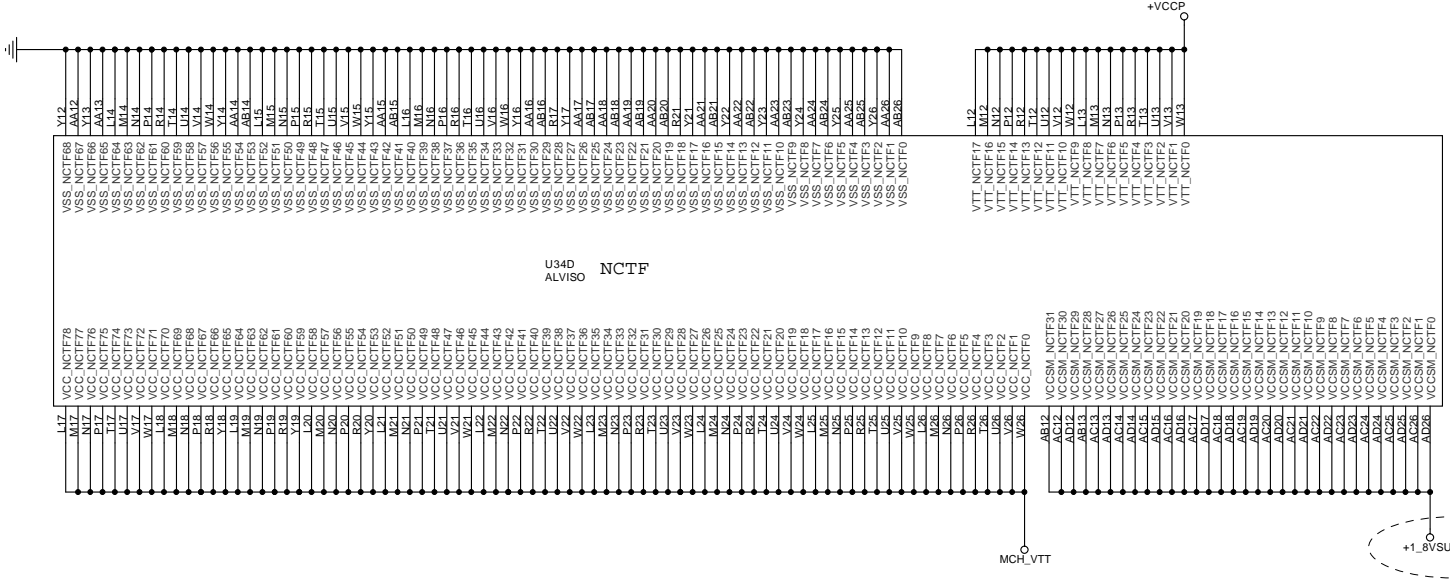
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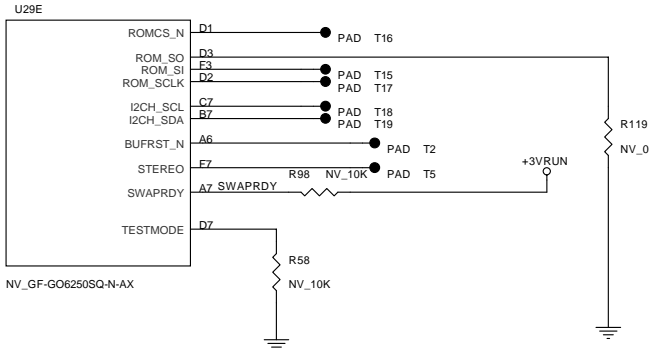
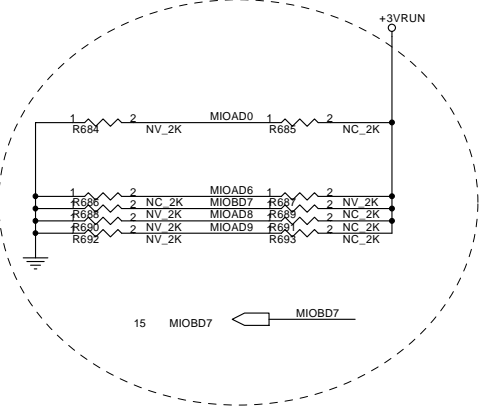
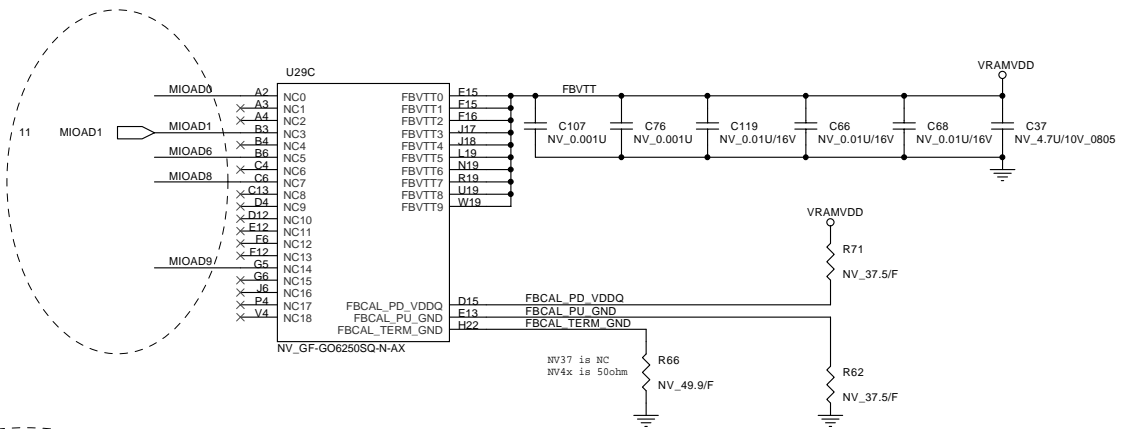
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U34E
ALVISO VSS



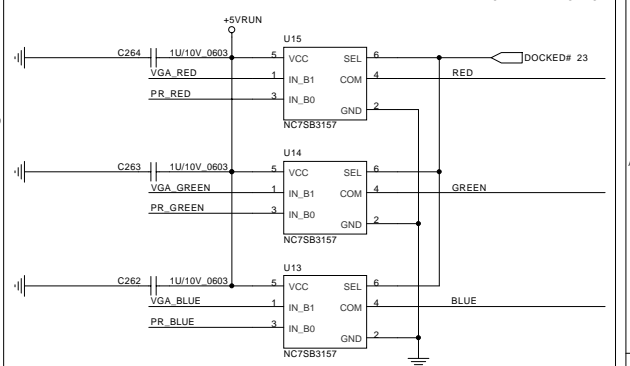
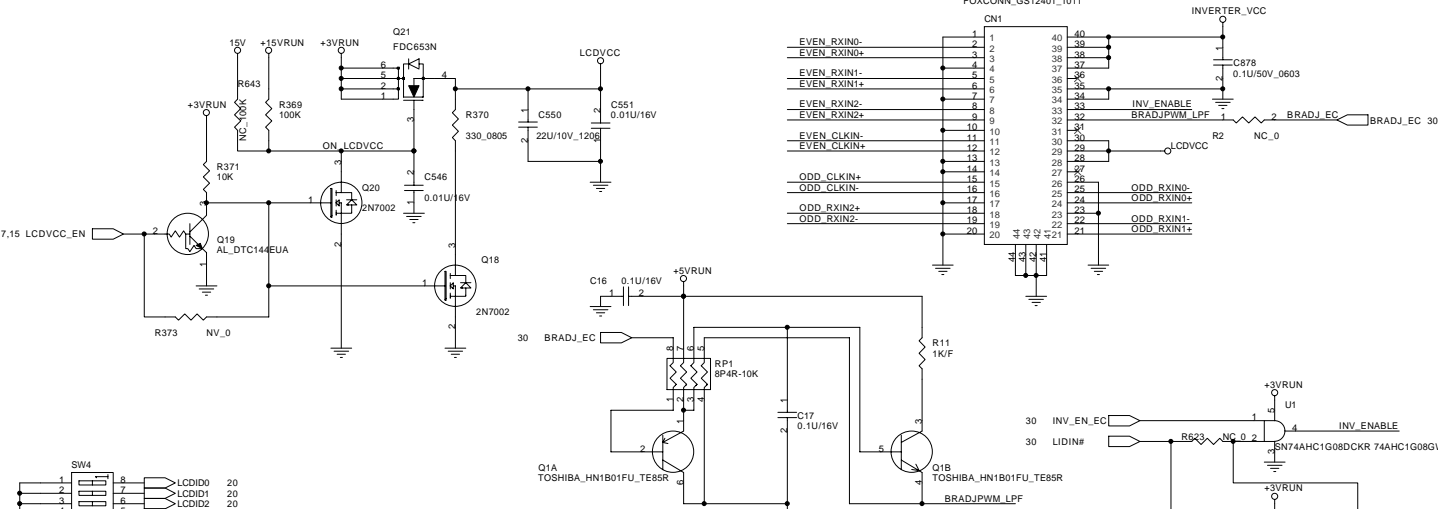
U34D
ALVISO NCTF



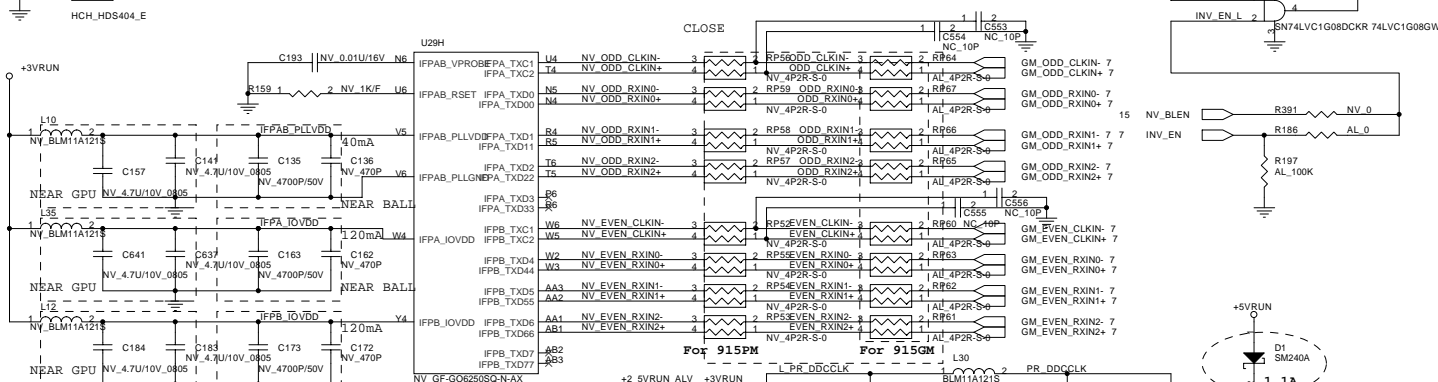
LVDS CONNECTOR

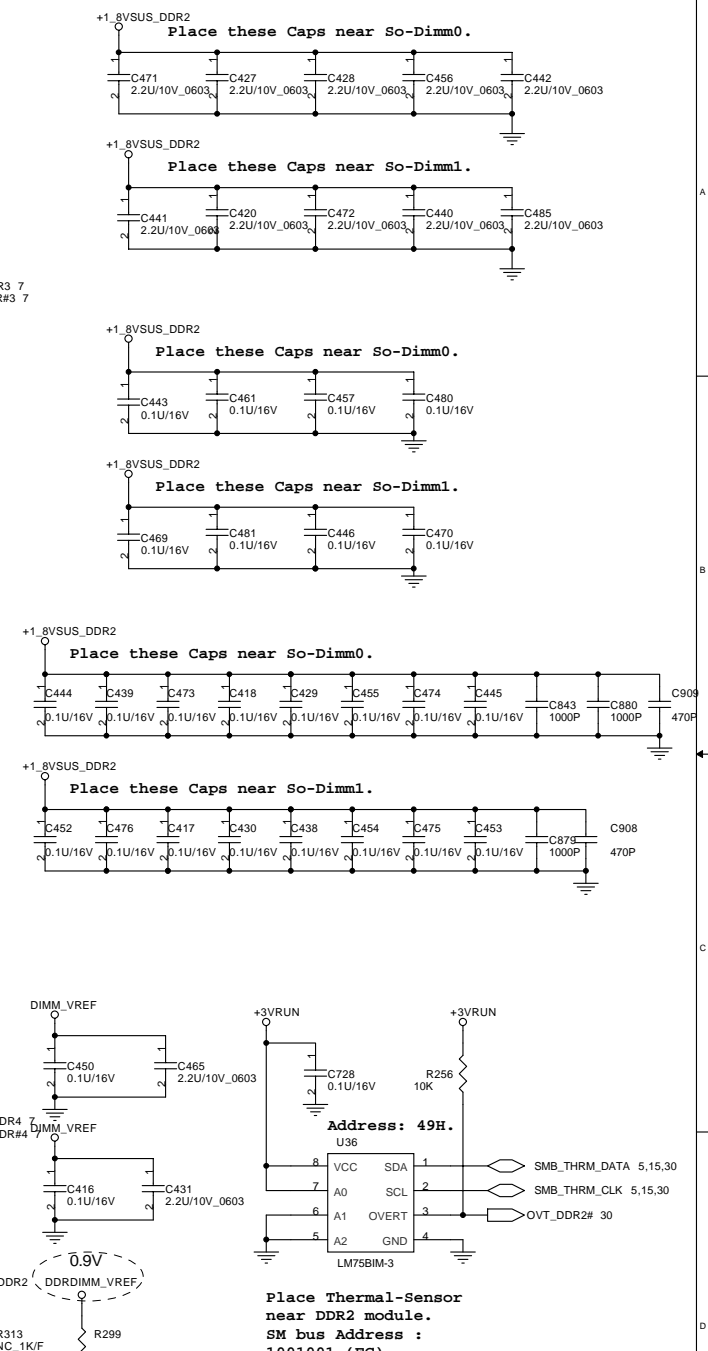
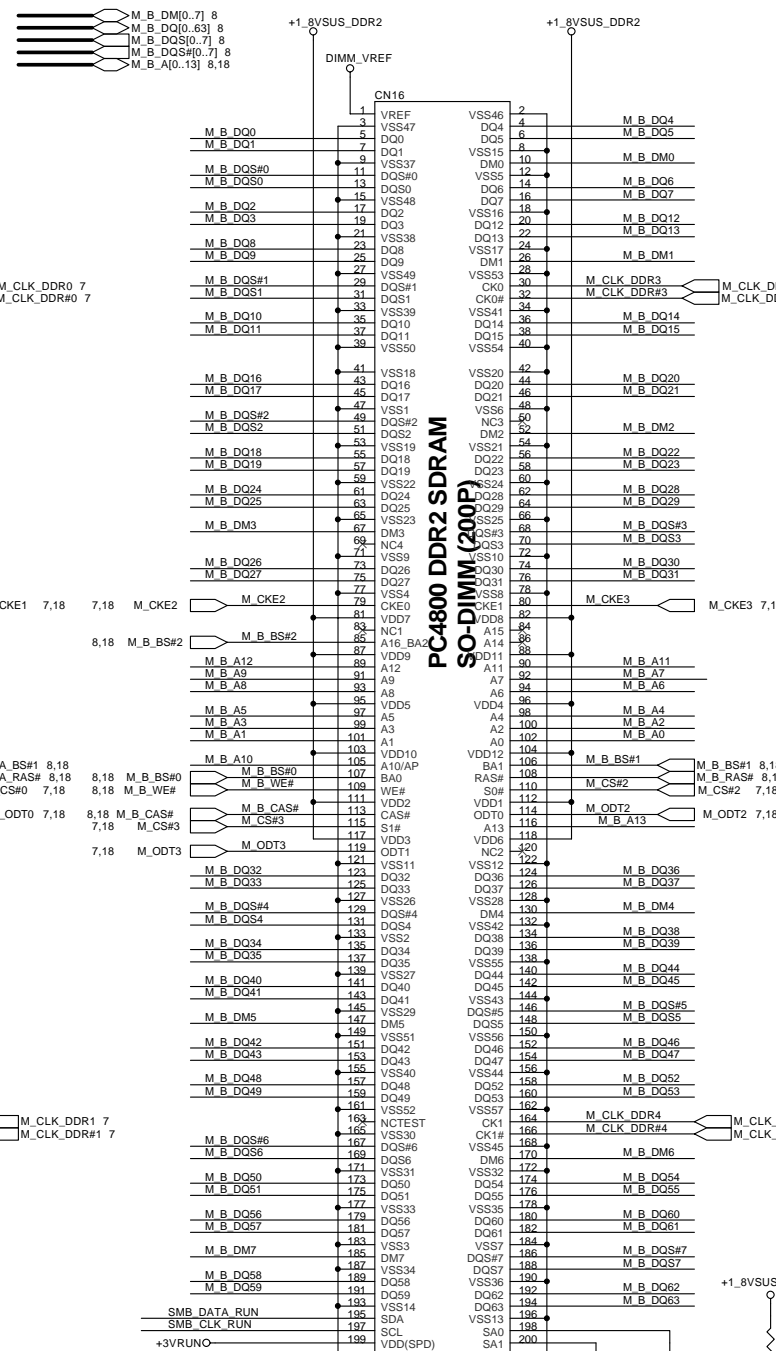
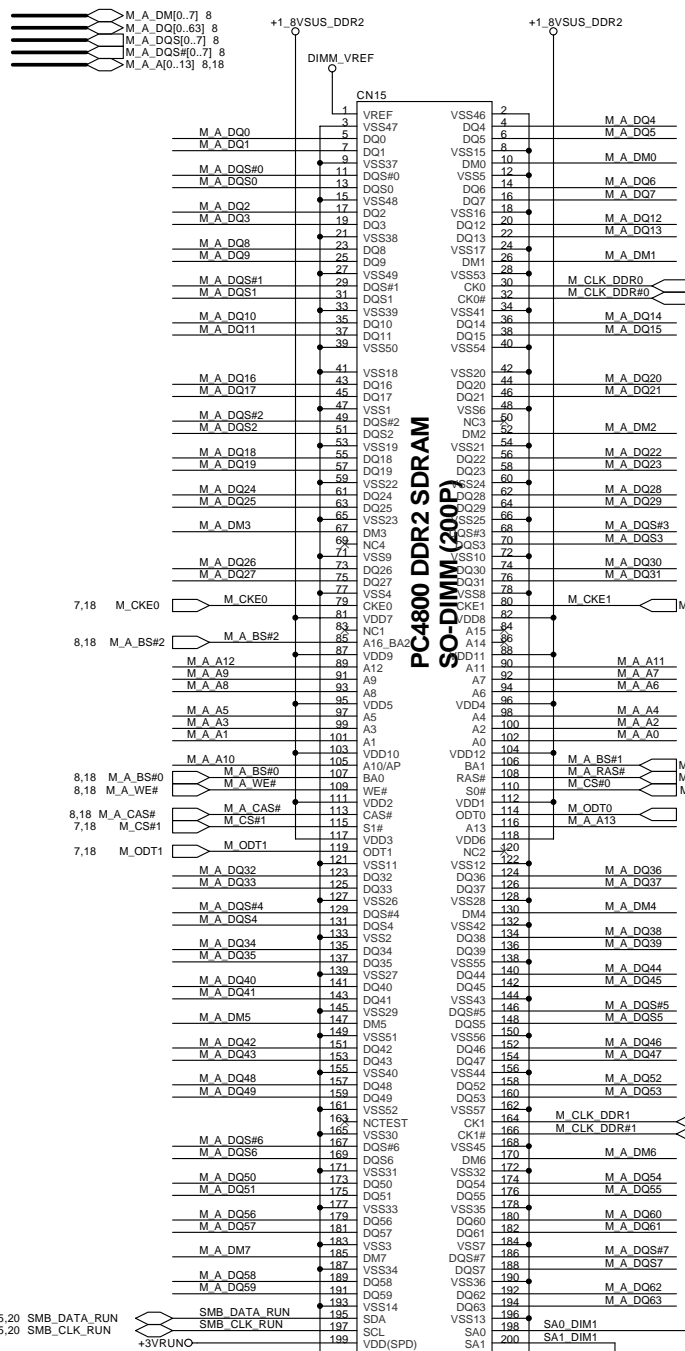
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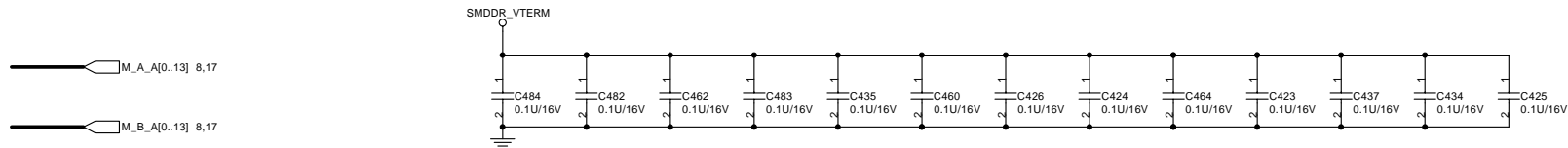
H : NOTEBOOK
L : PORT REPLICATOR



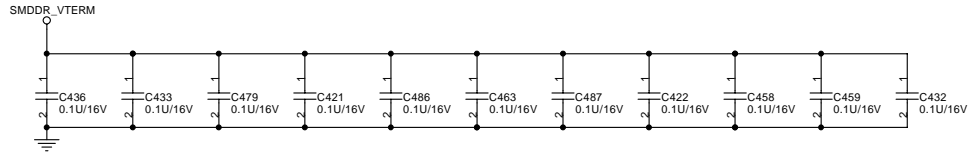
RGB ANALOG SWITCH



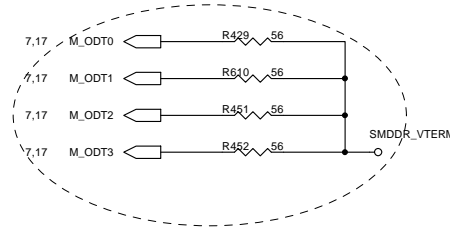
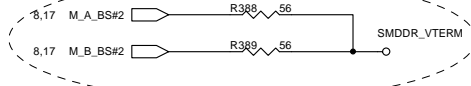
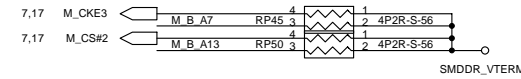
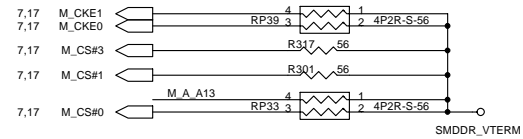
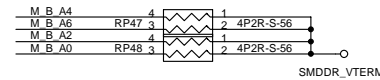
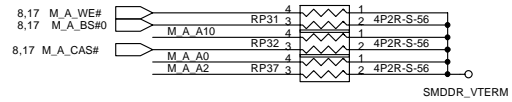
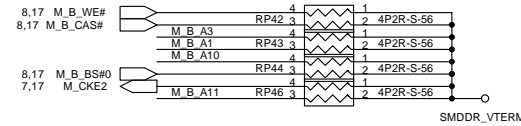
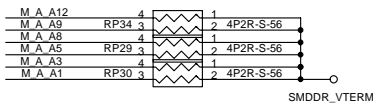
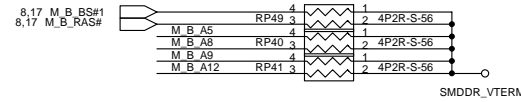
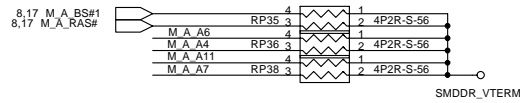


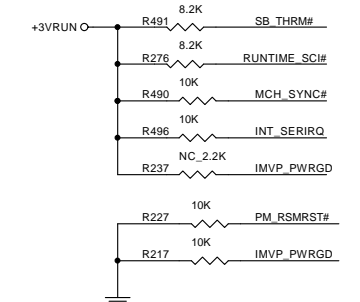
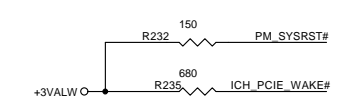
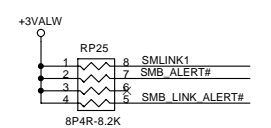
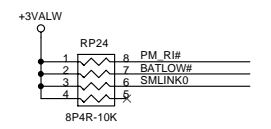
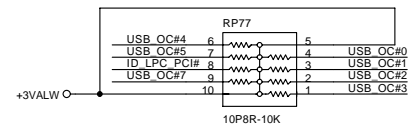
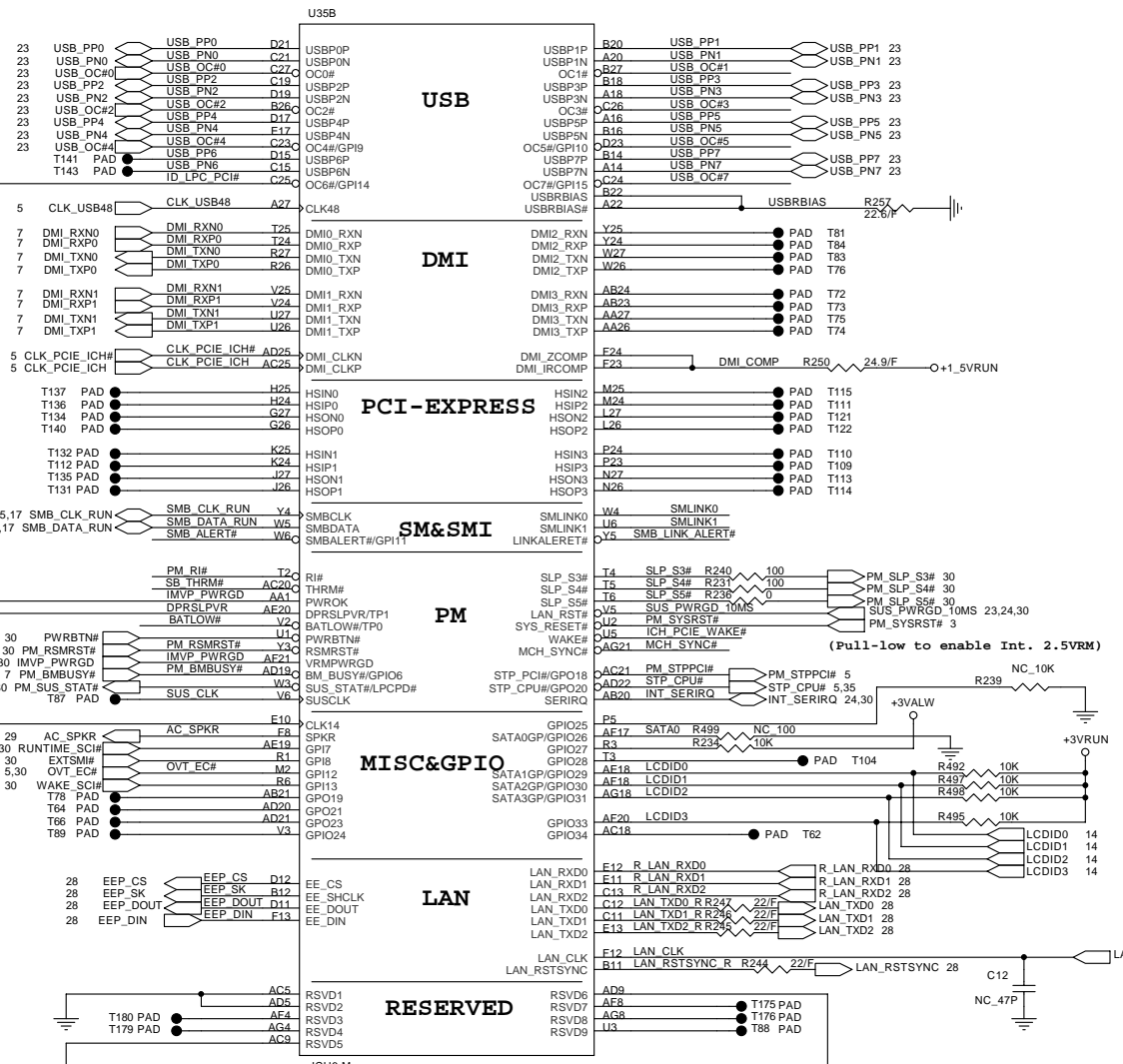
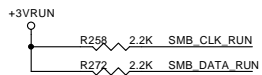


Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

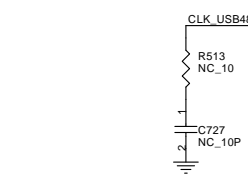
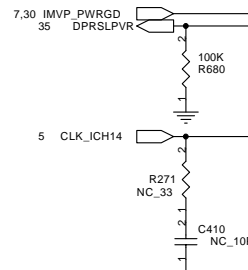


Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.



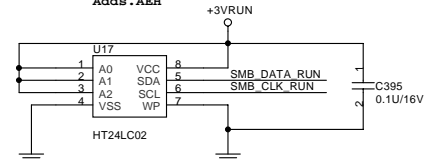


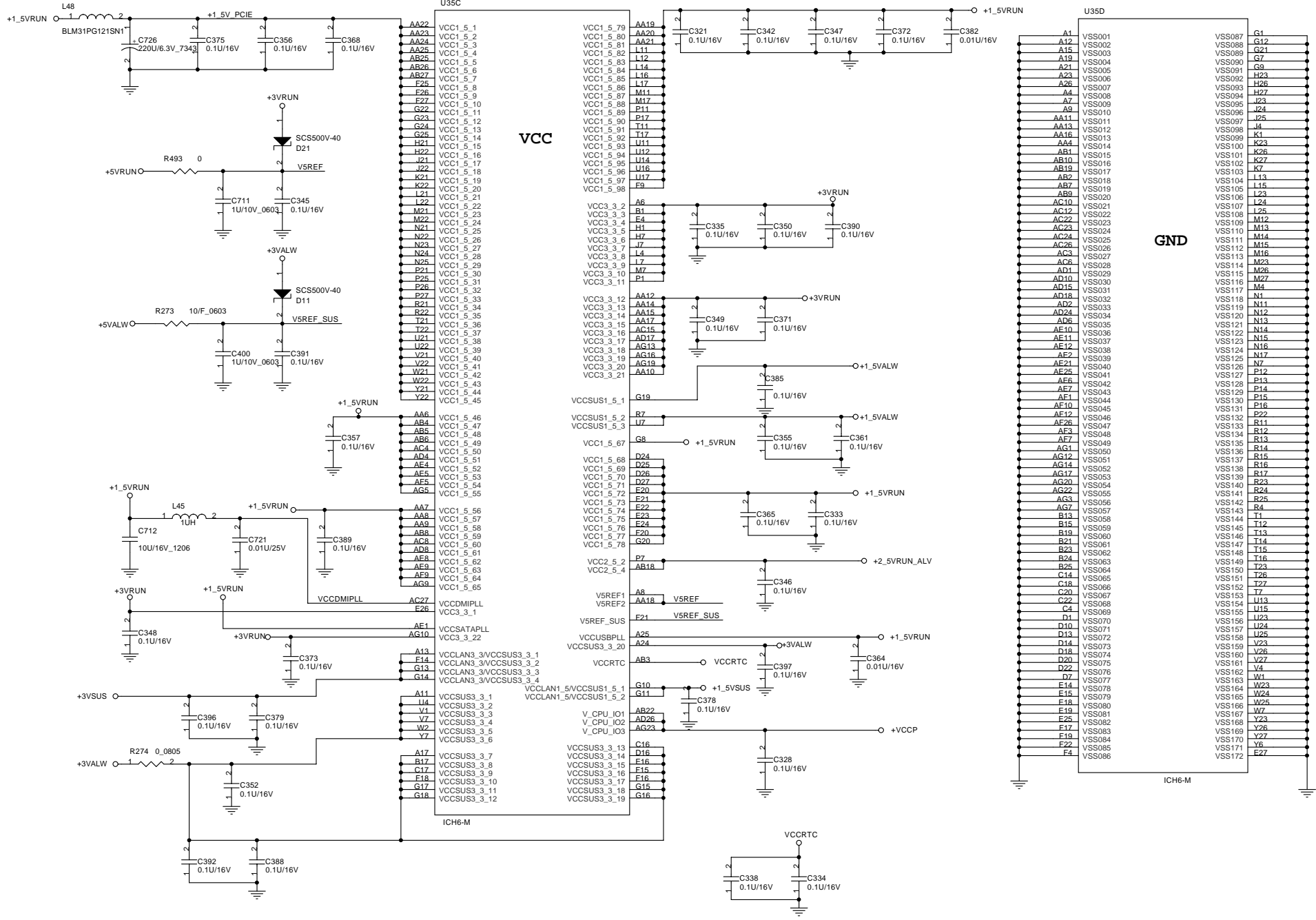
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80 Port I/F:
H: LCP bus
L: PCI bus

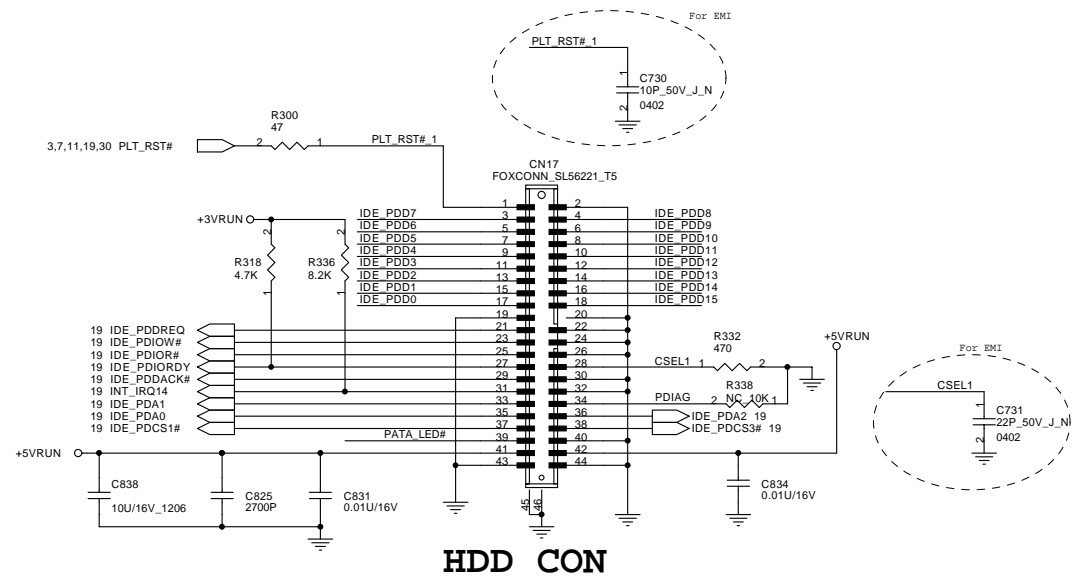


Strap for No-reboot
 R251 1K/F
 AC SPKR

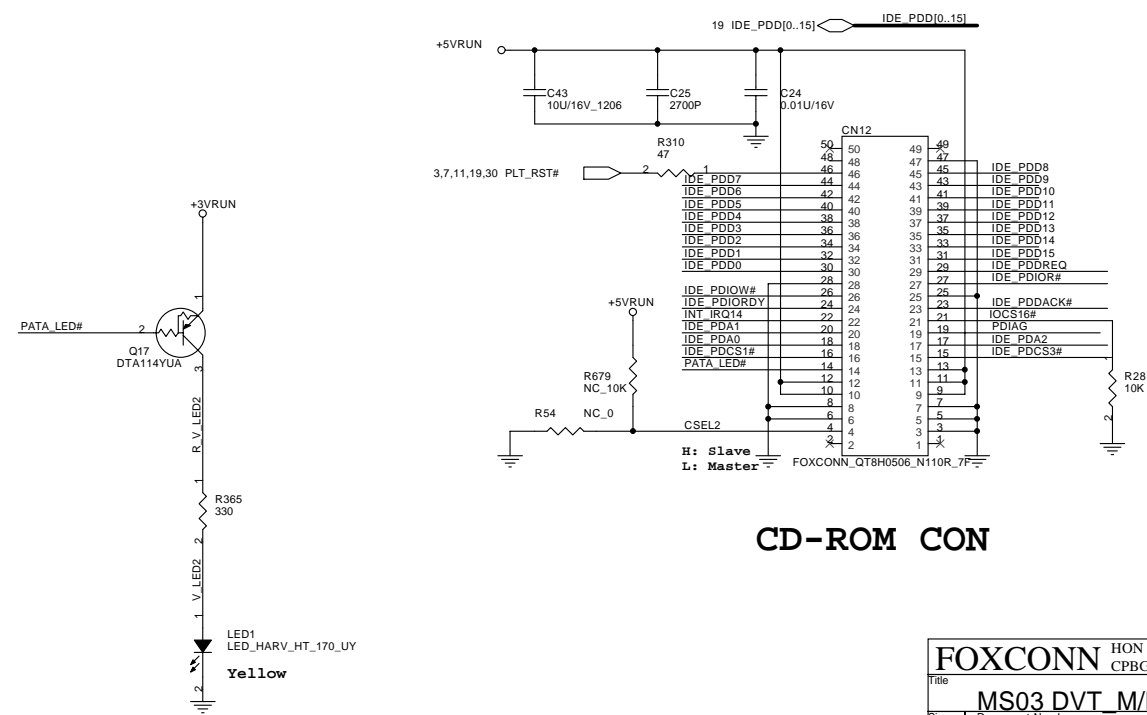
Adds .AEH





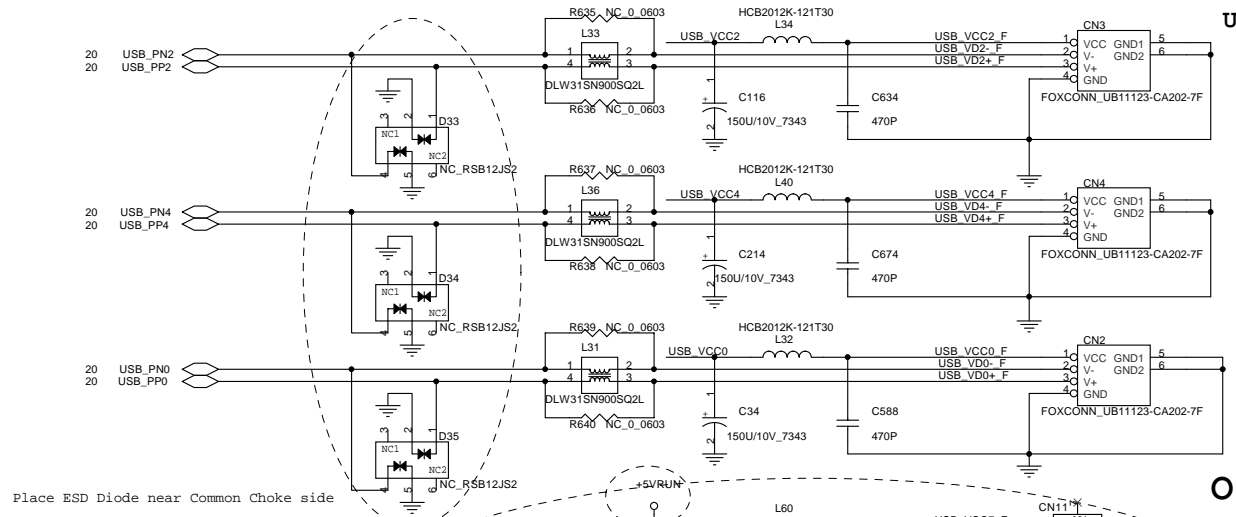
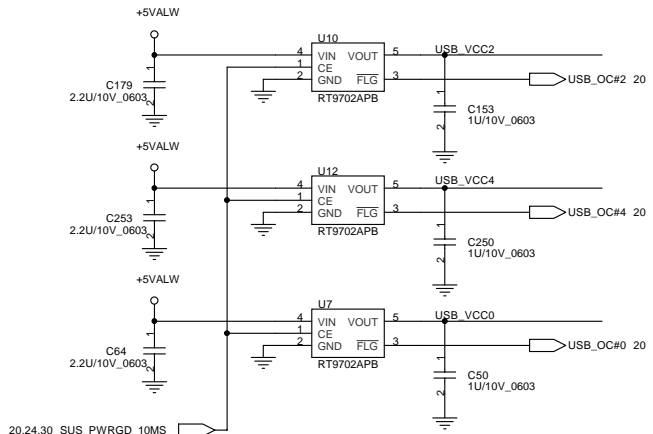


HDD CON



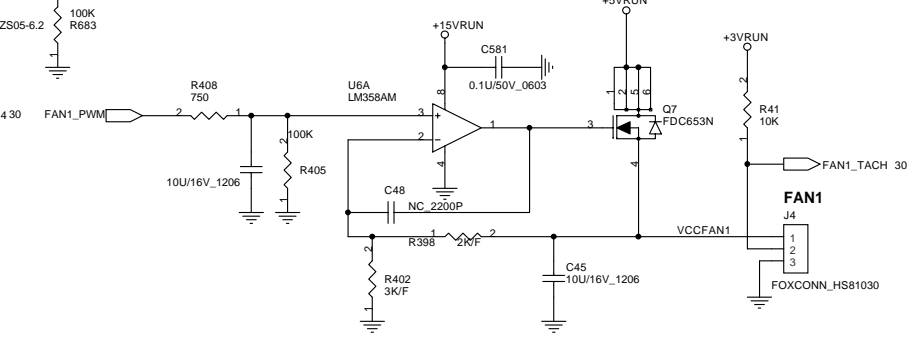
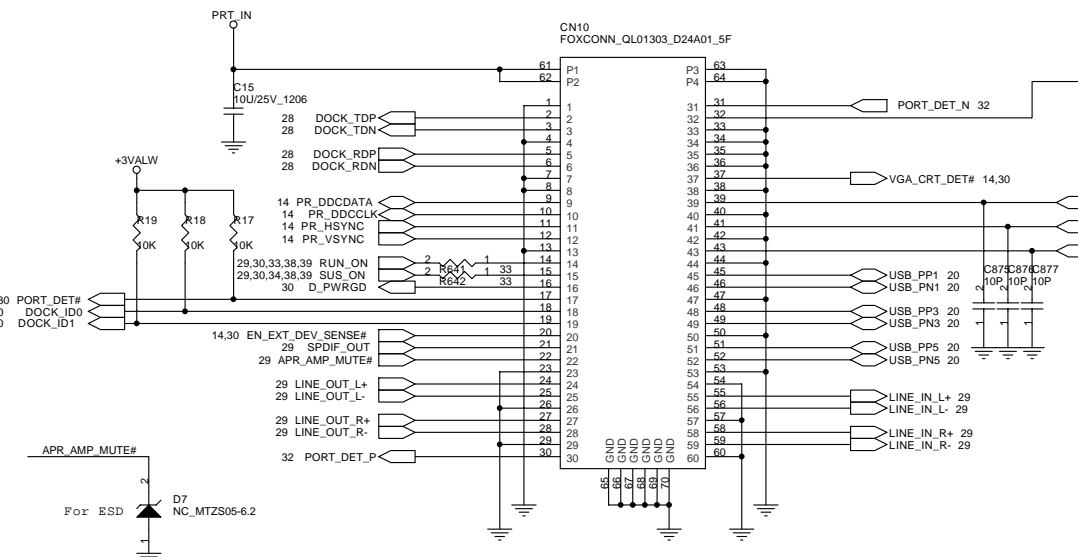
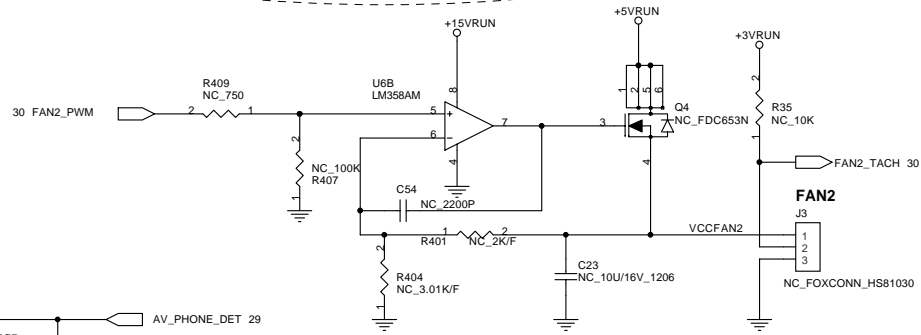
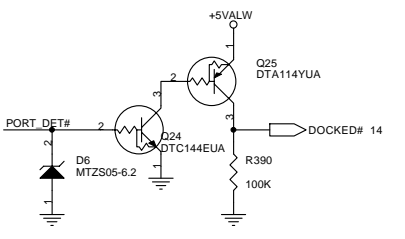
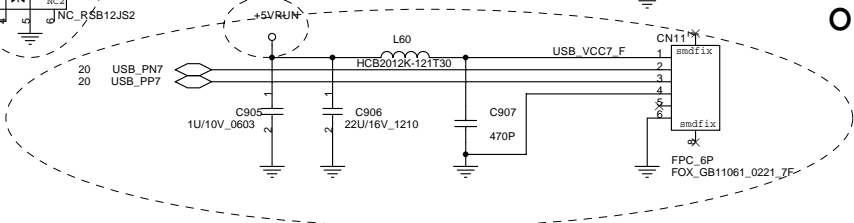
CD-ROM CON

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Place ESD Diode near Common Choke side

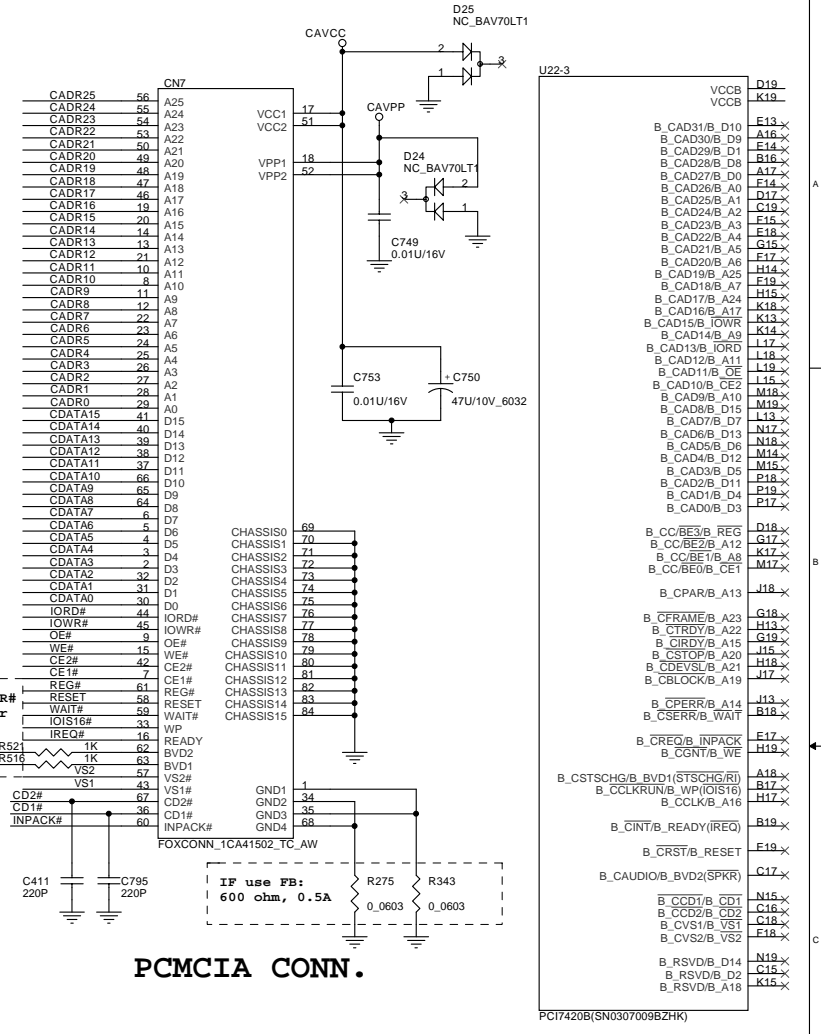
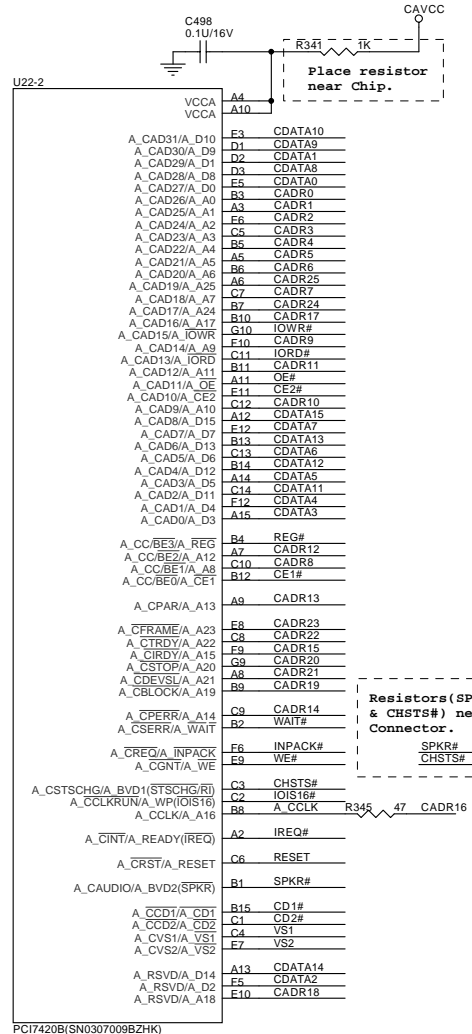
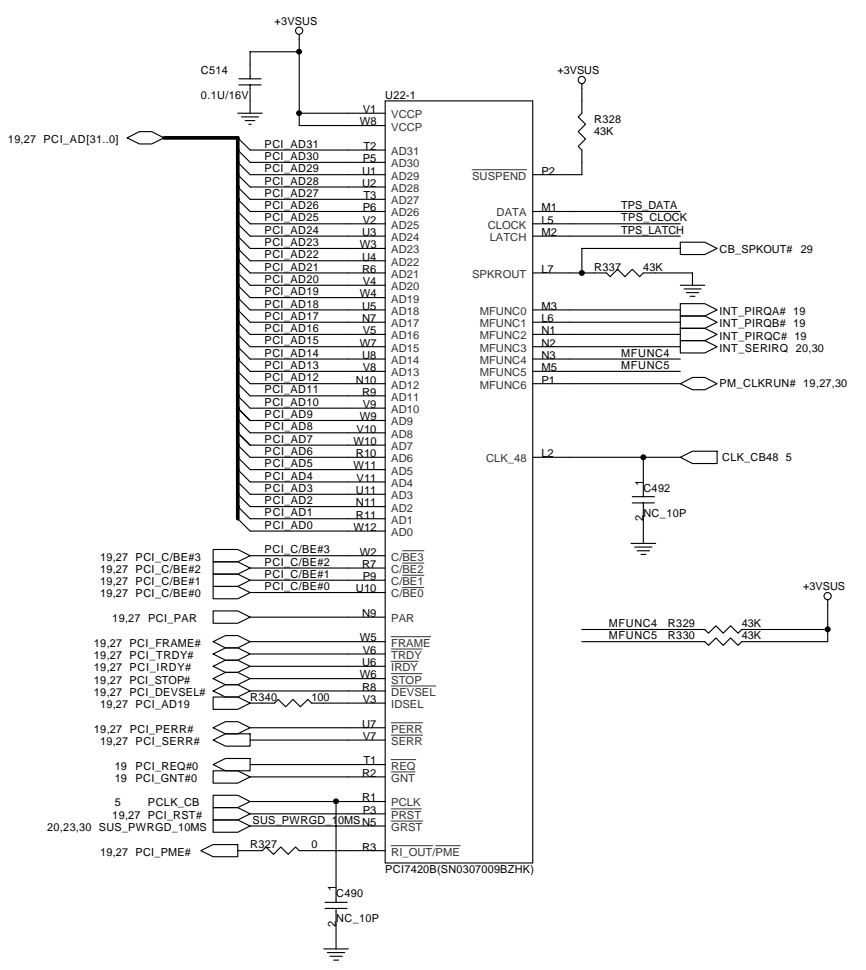
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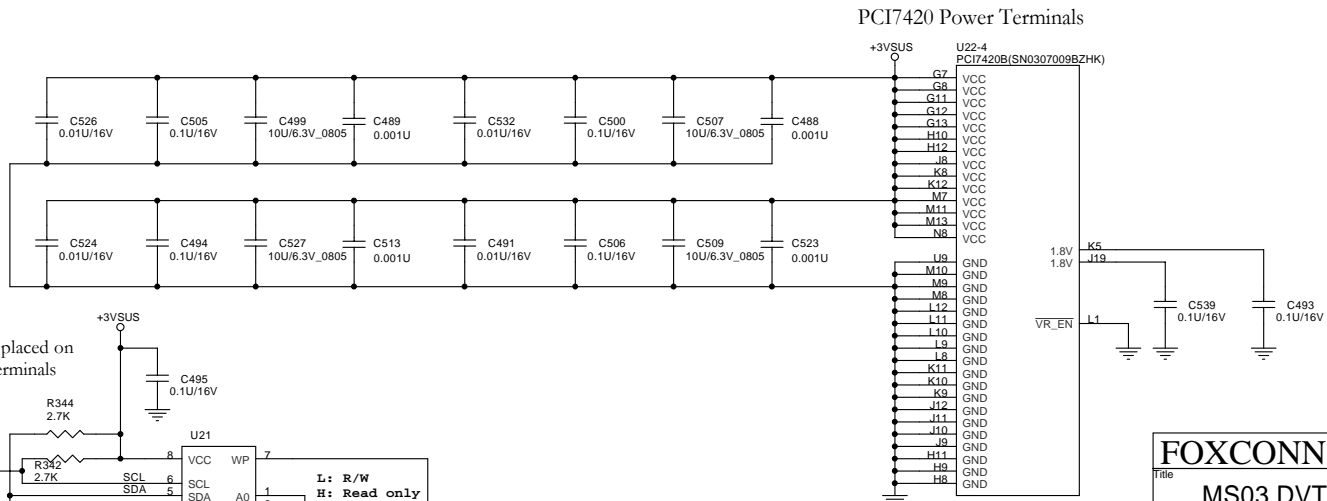
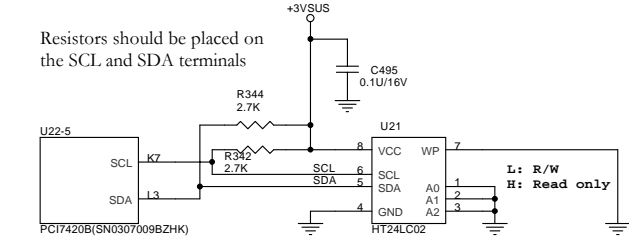
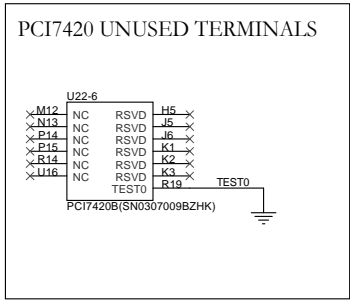
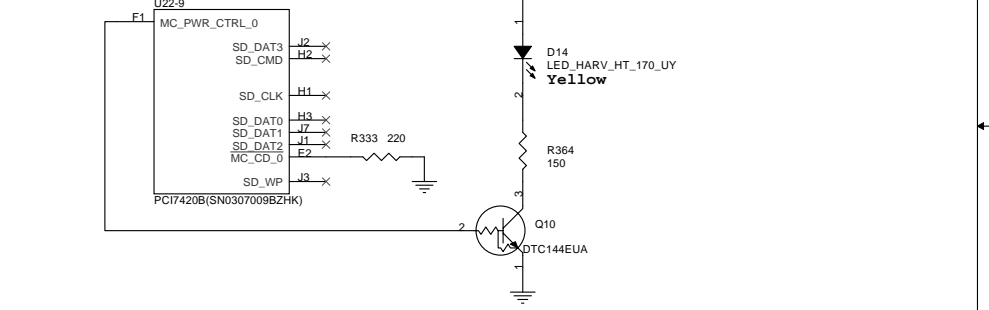
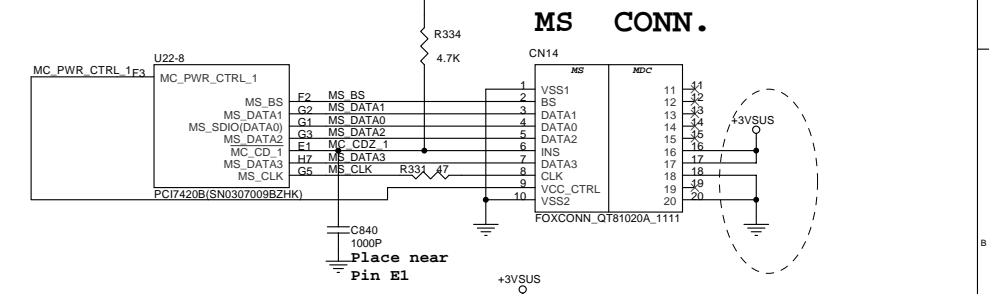
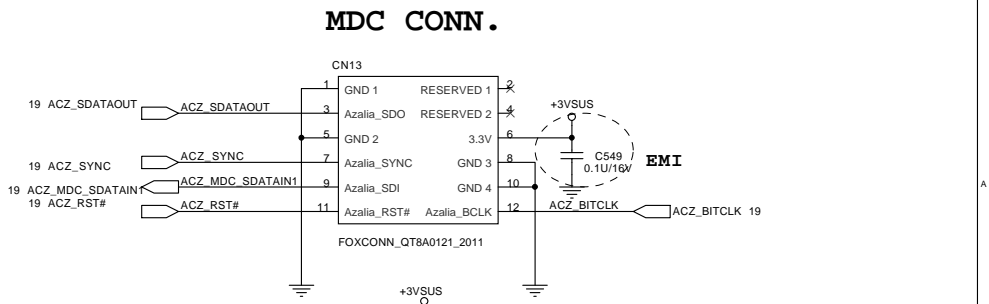
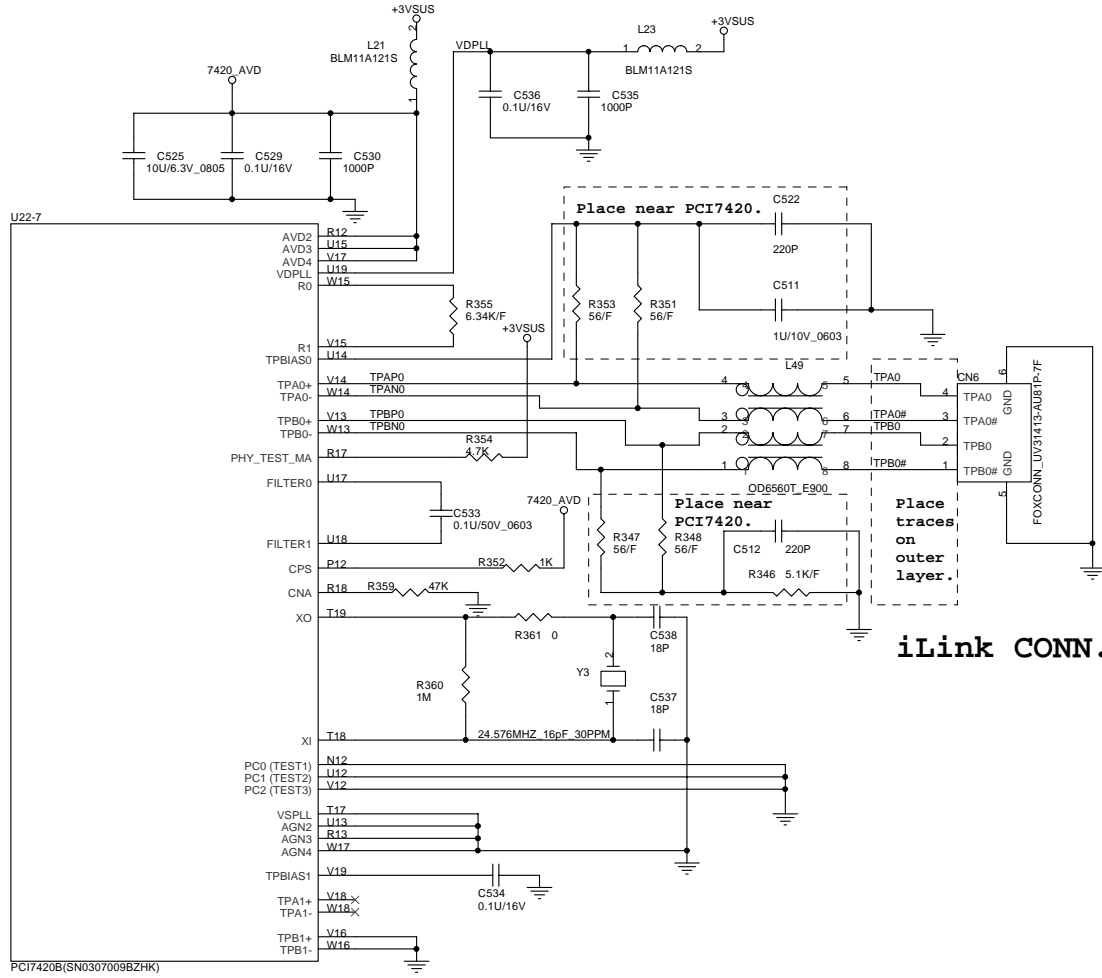


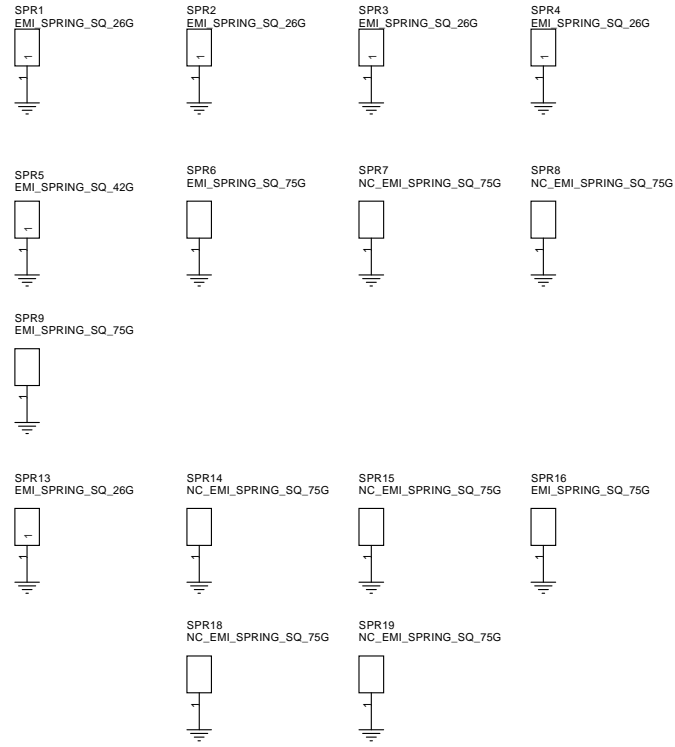
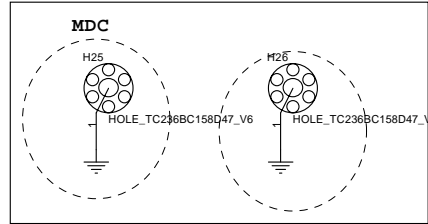
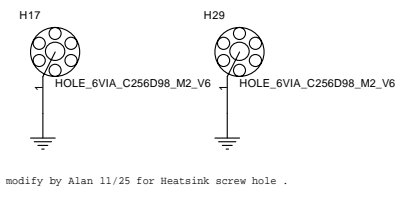
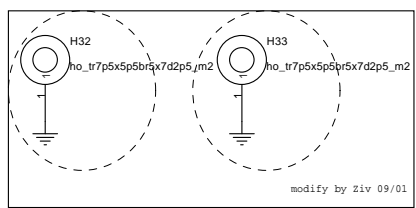
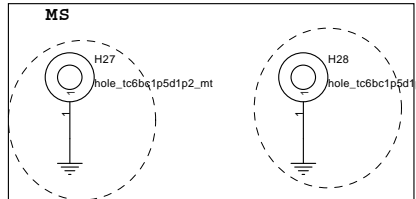
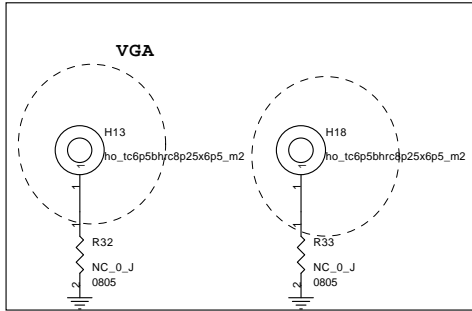
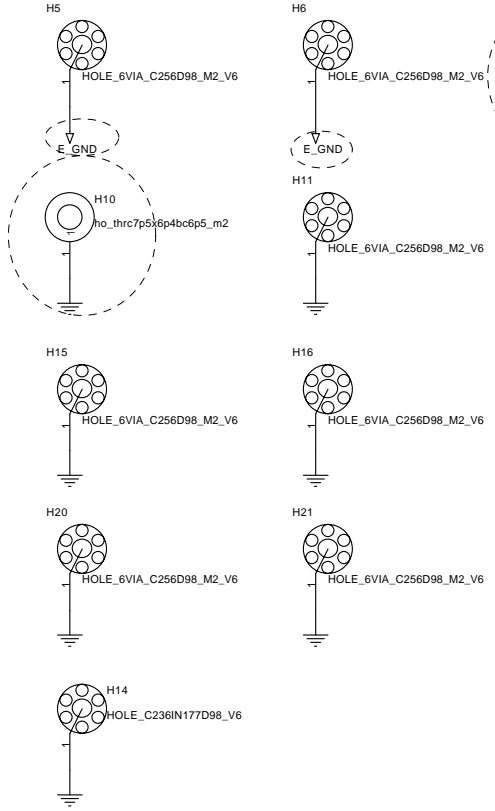
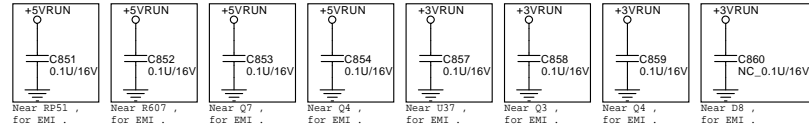
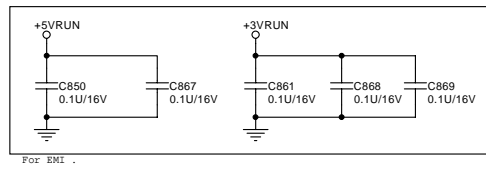
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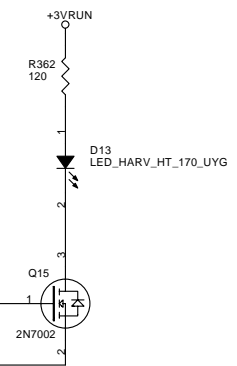
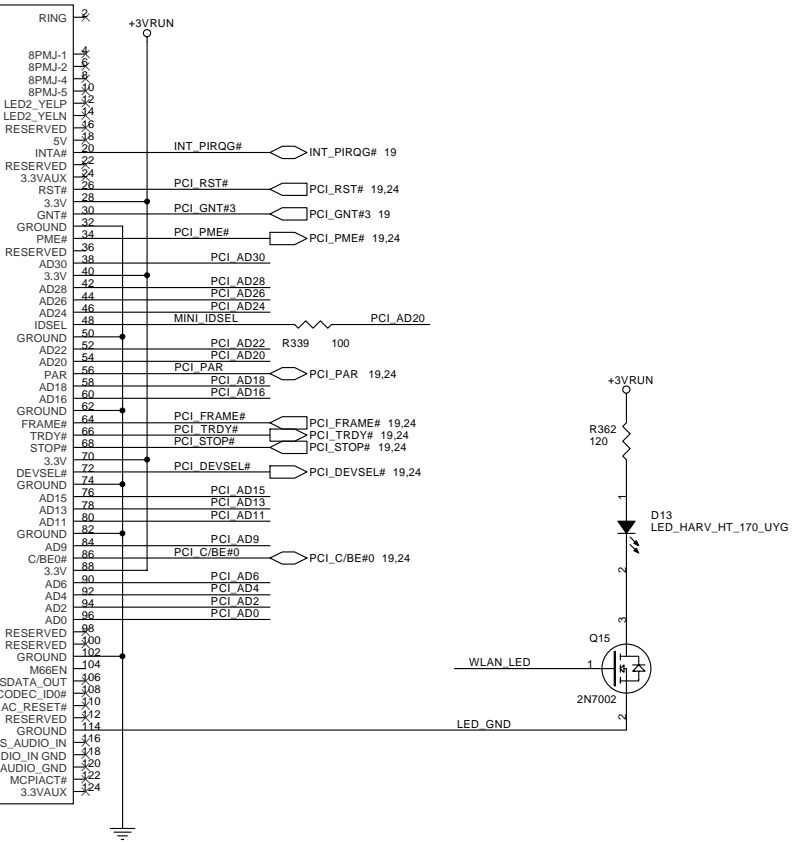
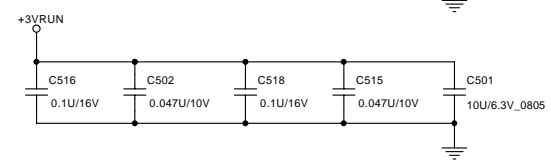
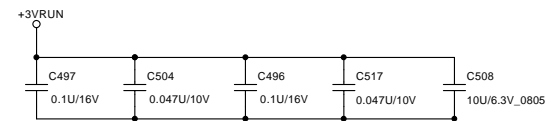
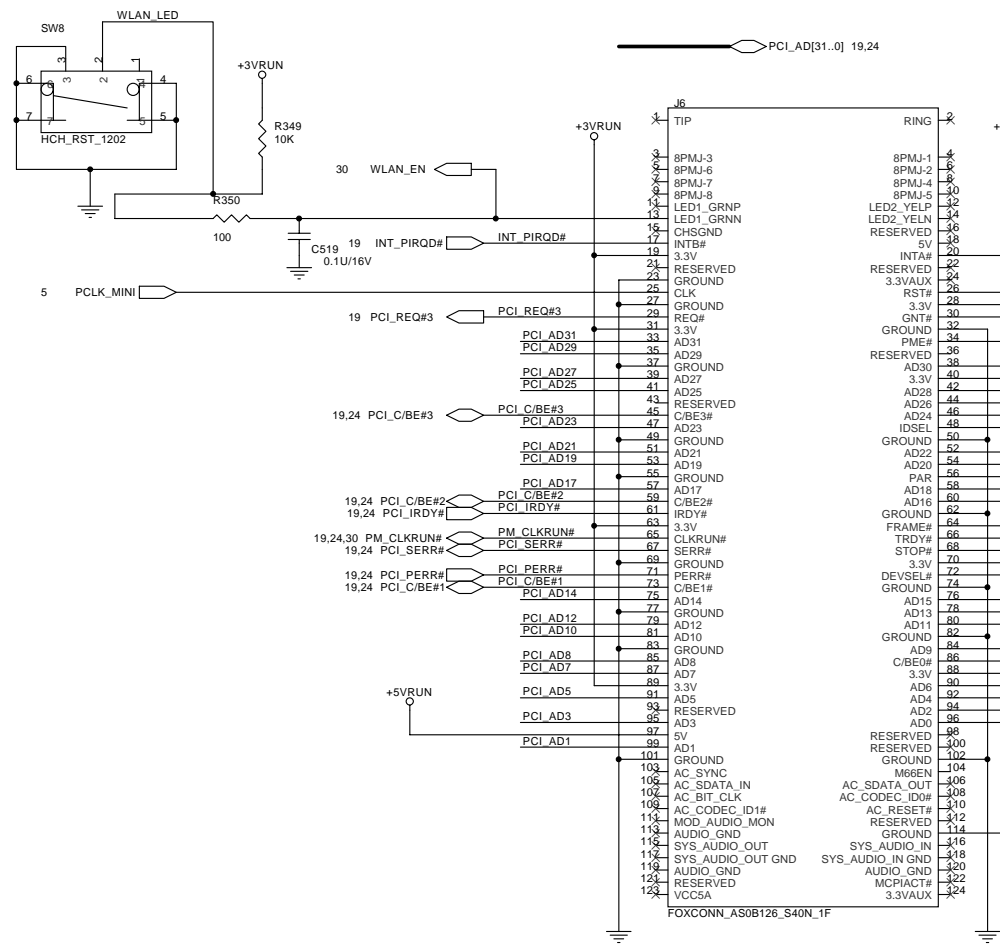
Replicator Port

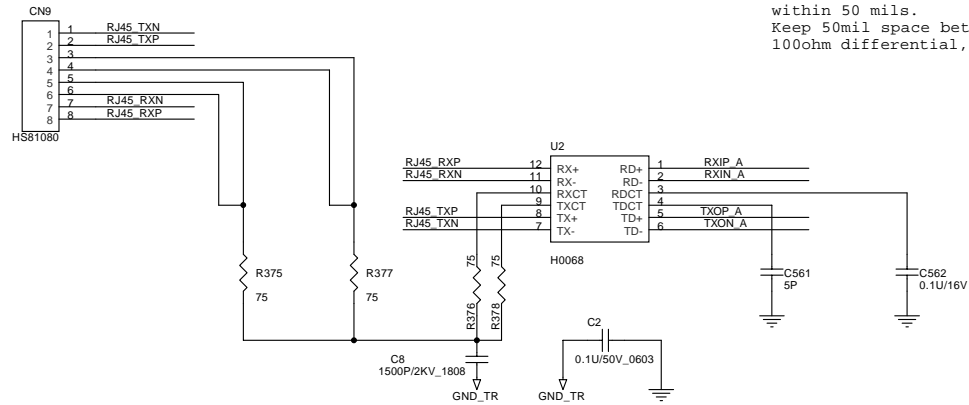
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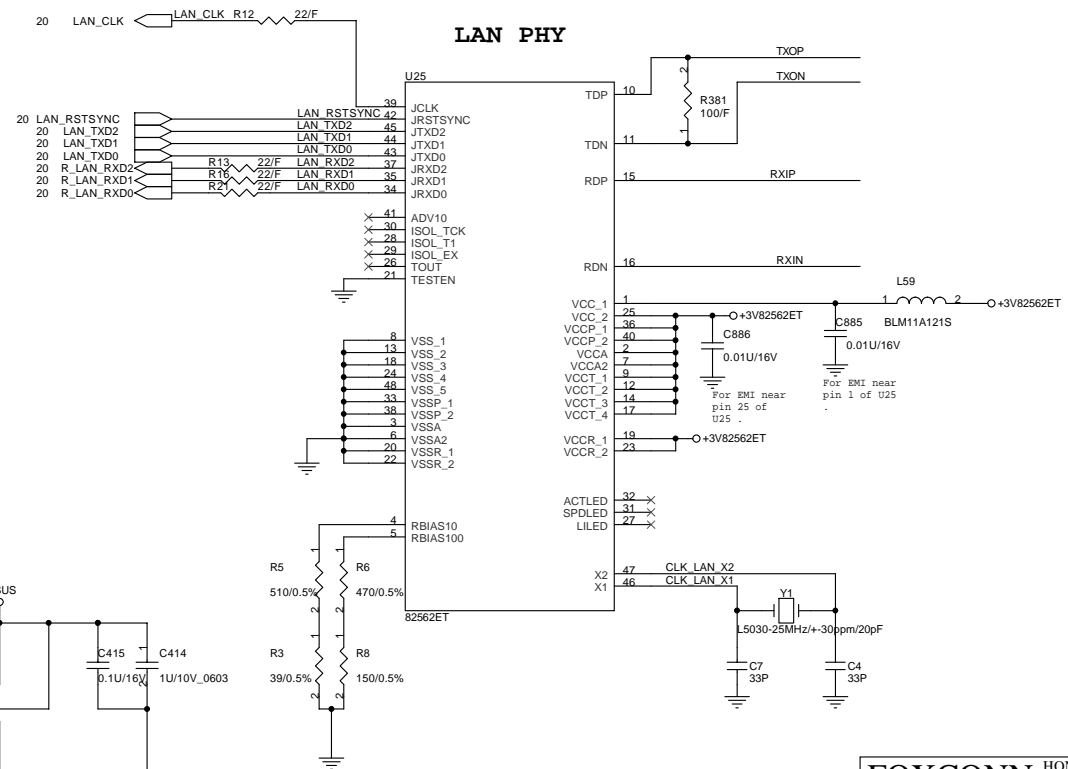
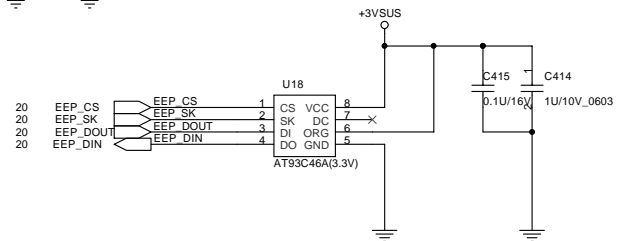
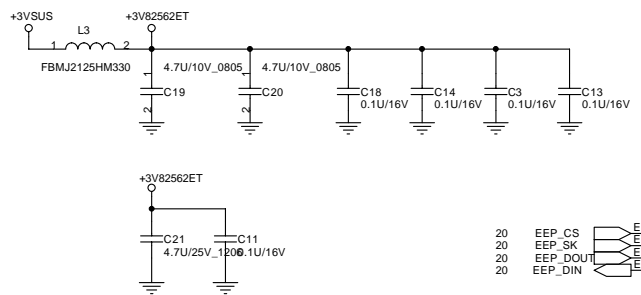
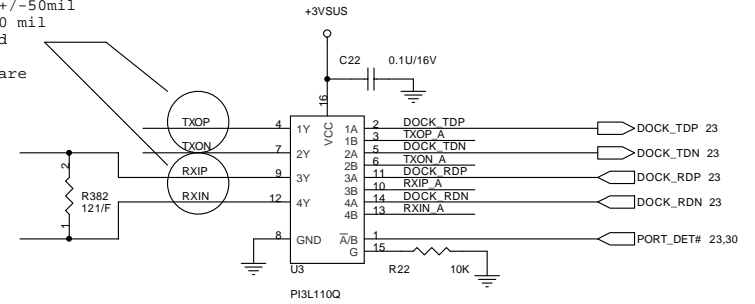


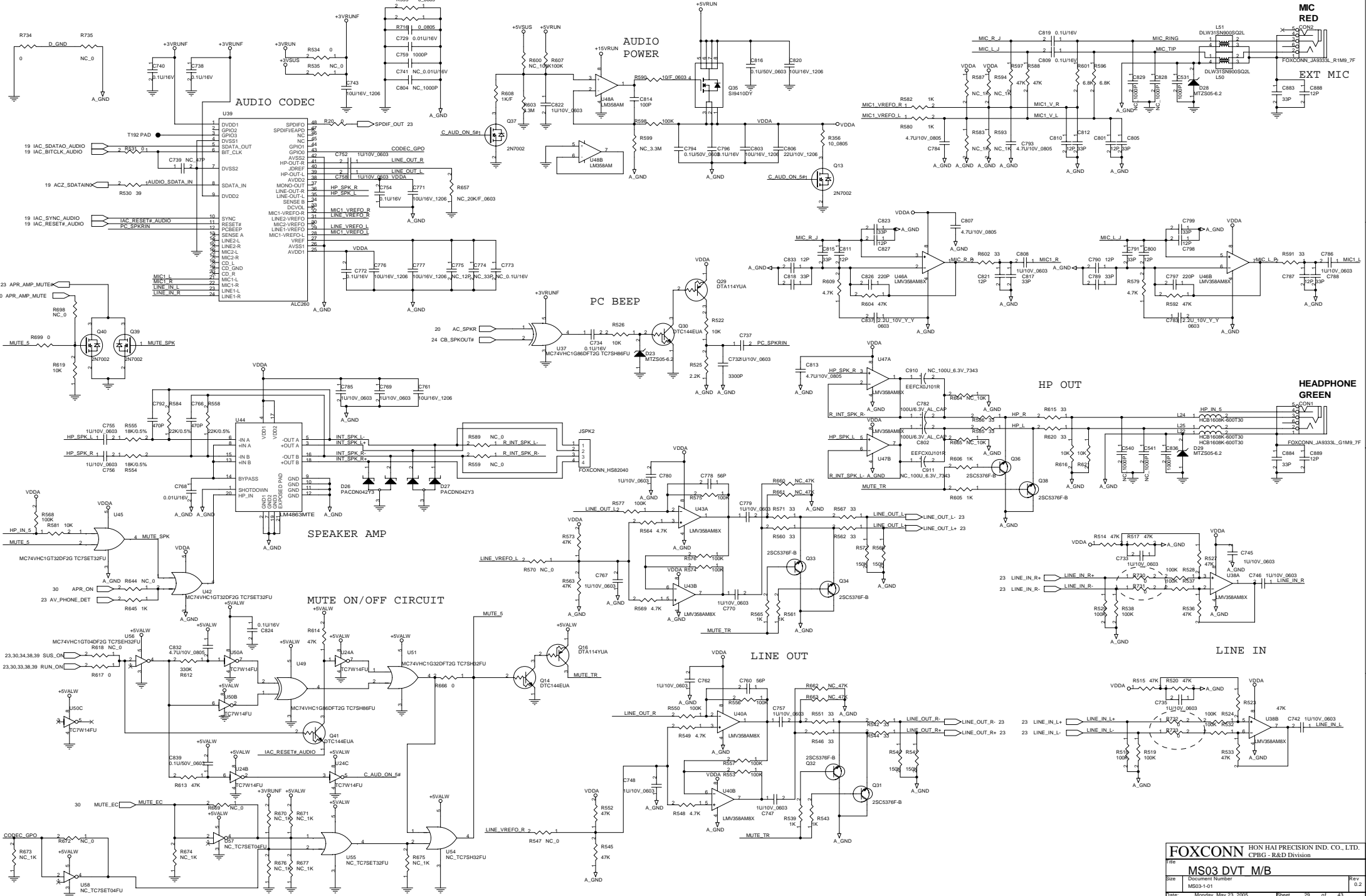


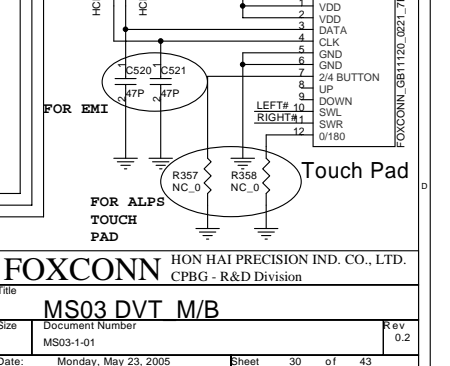
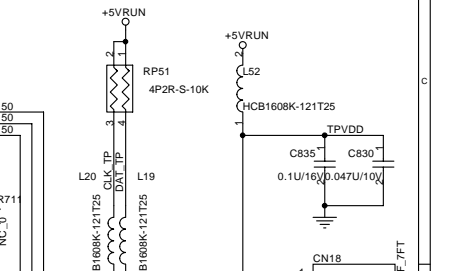
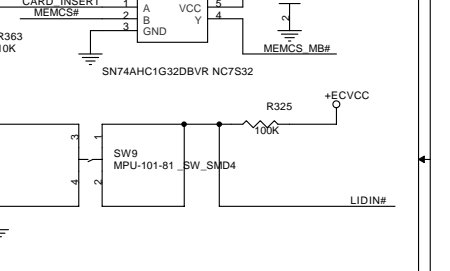
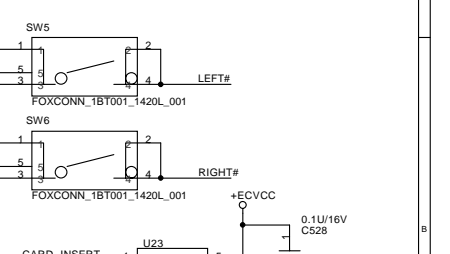
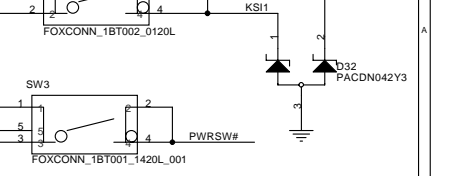
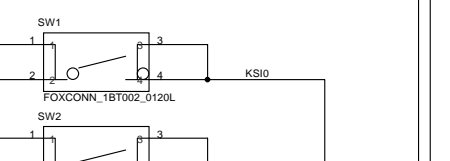
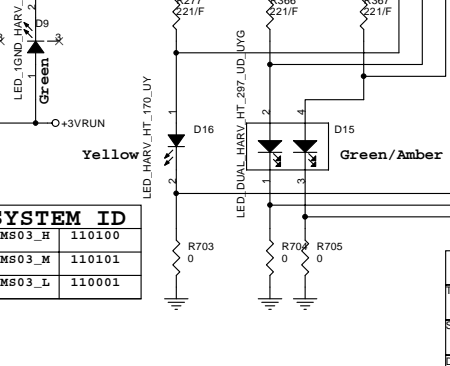
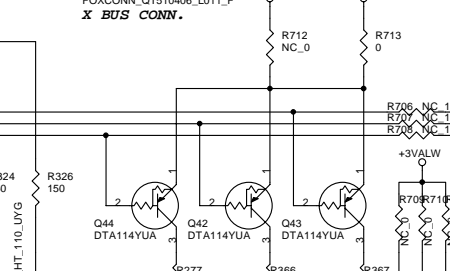
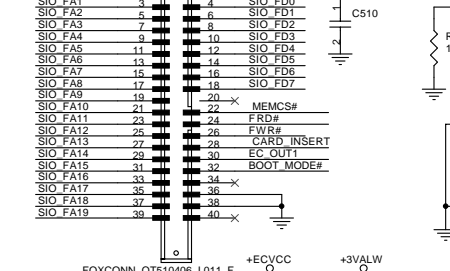
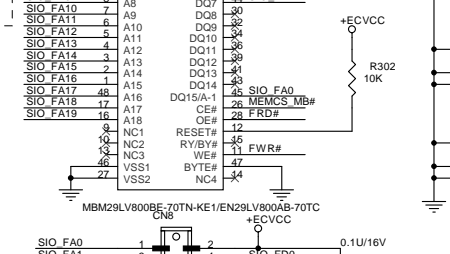
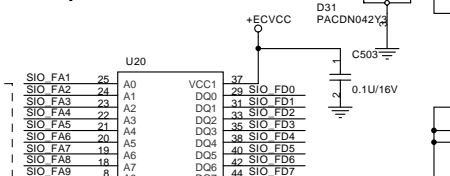
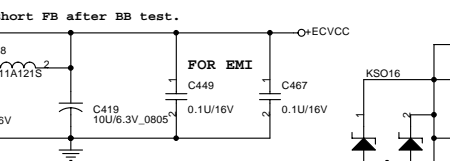
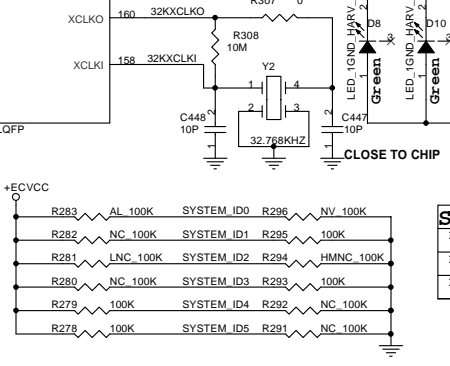
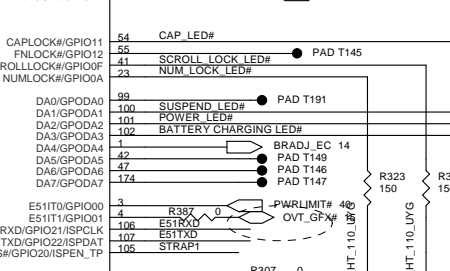
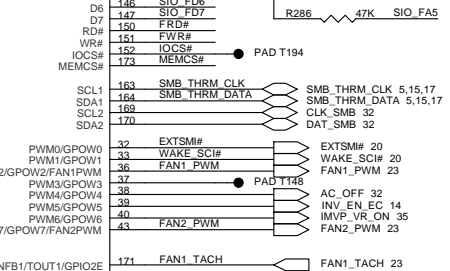
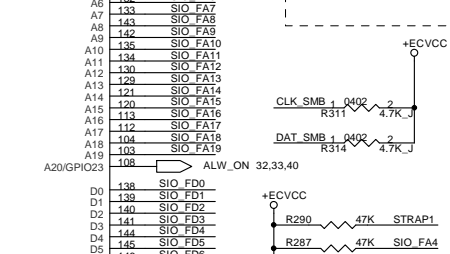
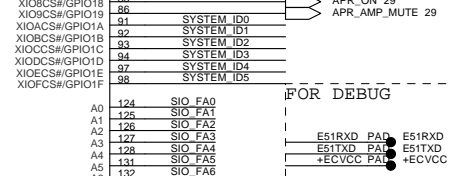
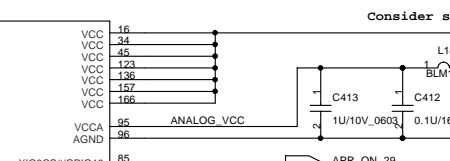
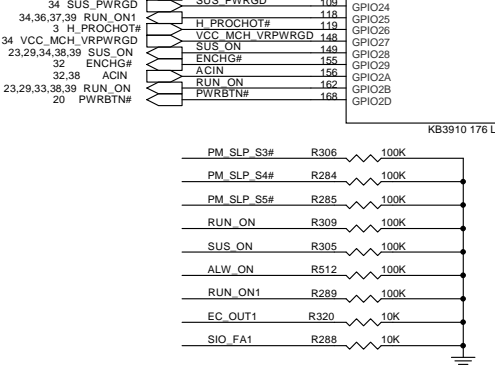
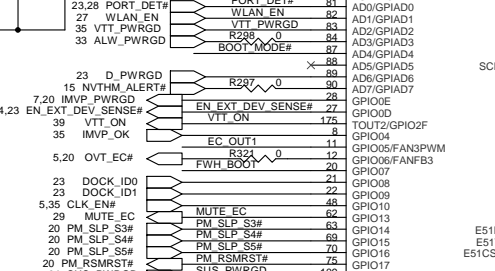
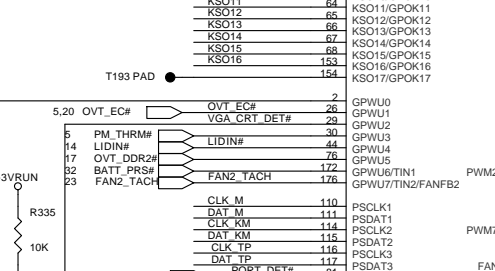
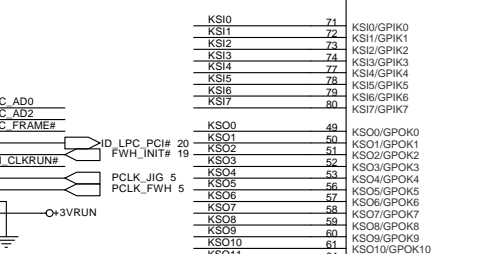
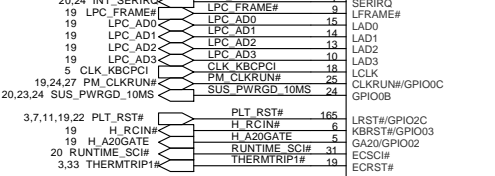
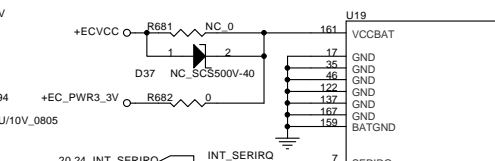
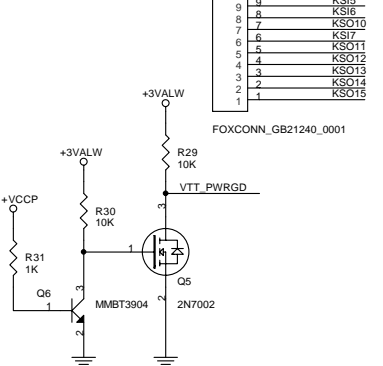
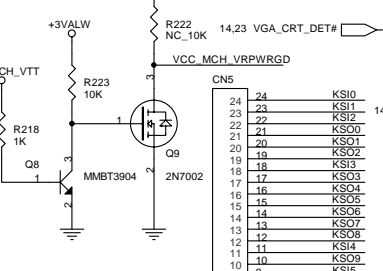
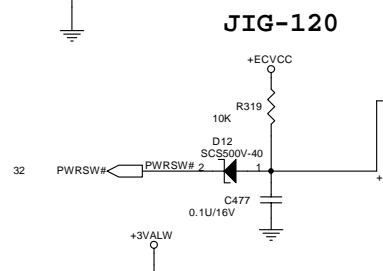
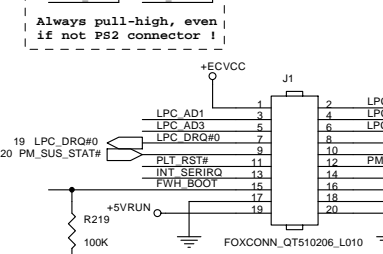
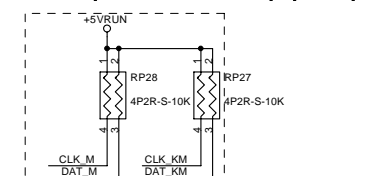
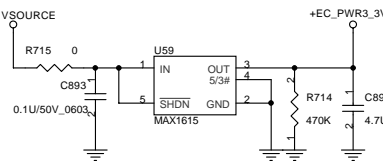
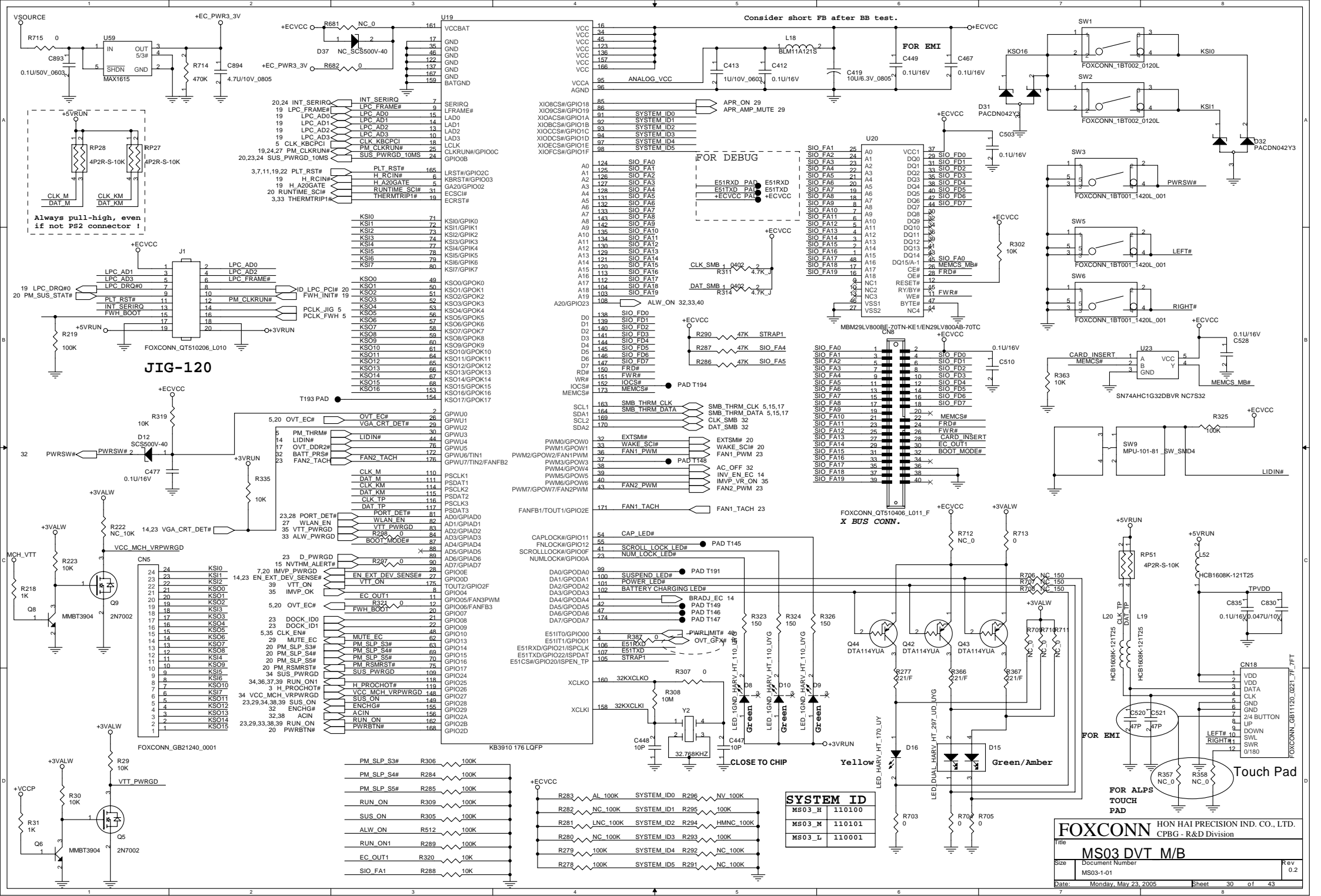


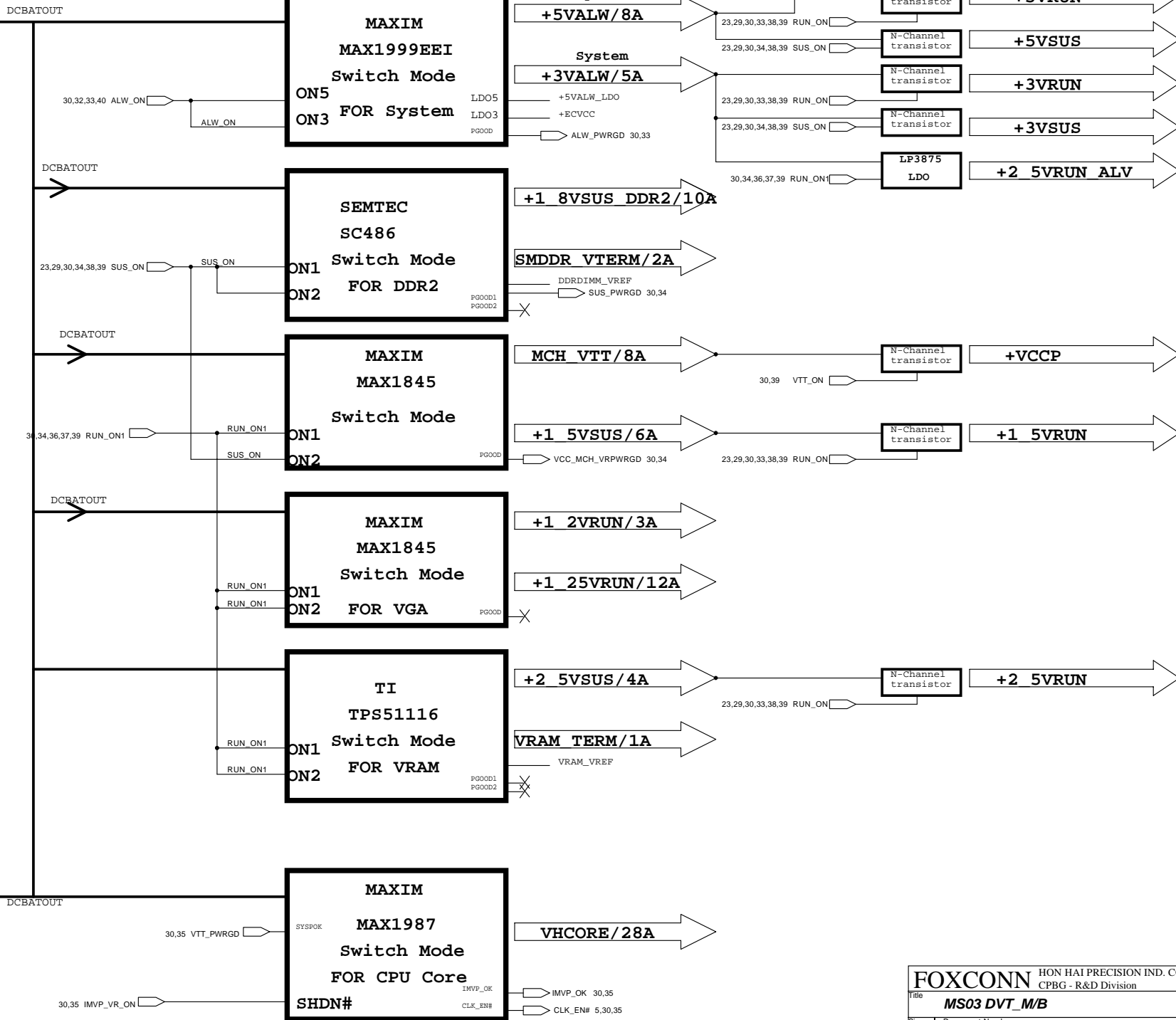
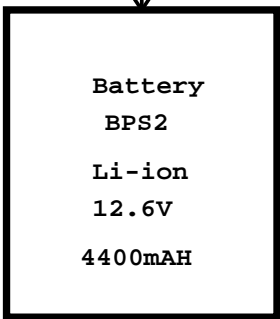
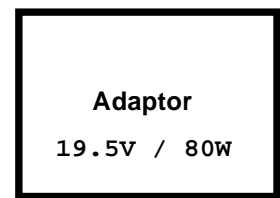


Match trace length
 LAYOUT NOTES:
 Match total length of chip side Rx and Tx pair traces +/-50mil
 Match length of cable side Rx and Tx pair traces +/- 50 mil
 Total line TX+ to TX- and RX- and RX+ should be matched within 50 mils.
 Keep 50mil space between pairs and other traces. Pairs are 100ohm differential,





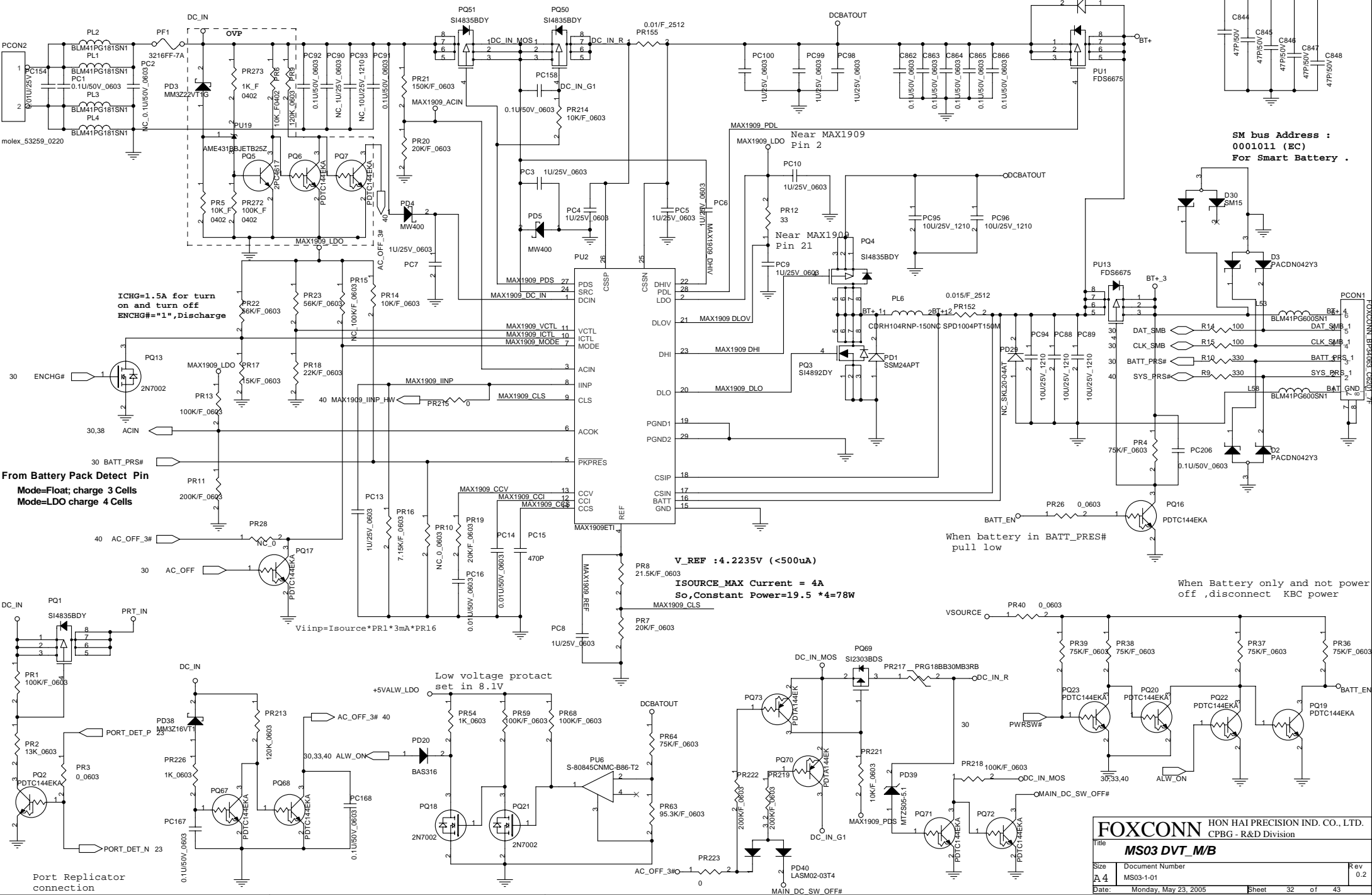




DC_IN from port replicator

AC IN Threshold 2.089V Max.
AC_IN > 2.089V -> AC DETECT

BT+ 4
DAT SMB 1
CLK SMB 1
BATT_PRS 1
SYS_PRS 1



SM bus Address :
0001011 (EC)
For Smart Battery .

ICHG=1.5A for turn on and turn off
ENCHG#="1", Discharge

From Battery Pack Detect Pin
Mode=Float; charge 3 Cells
Mode=LDO charge 4 Cells

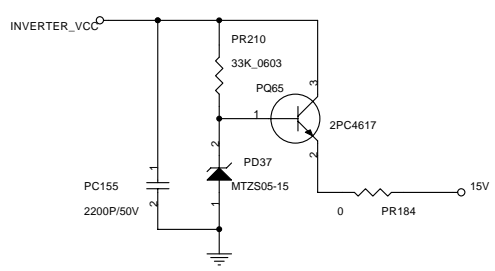
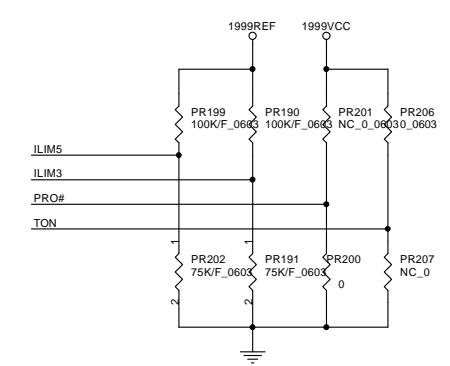
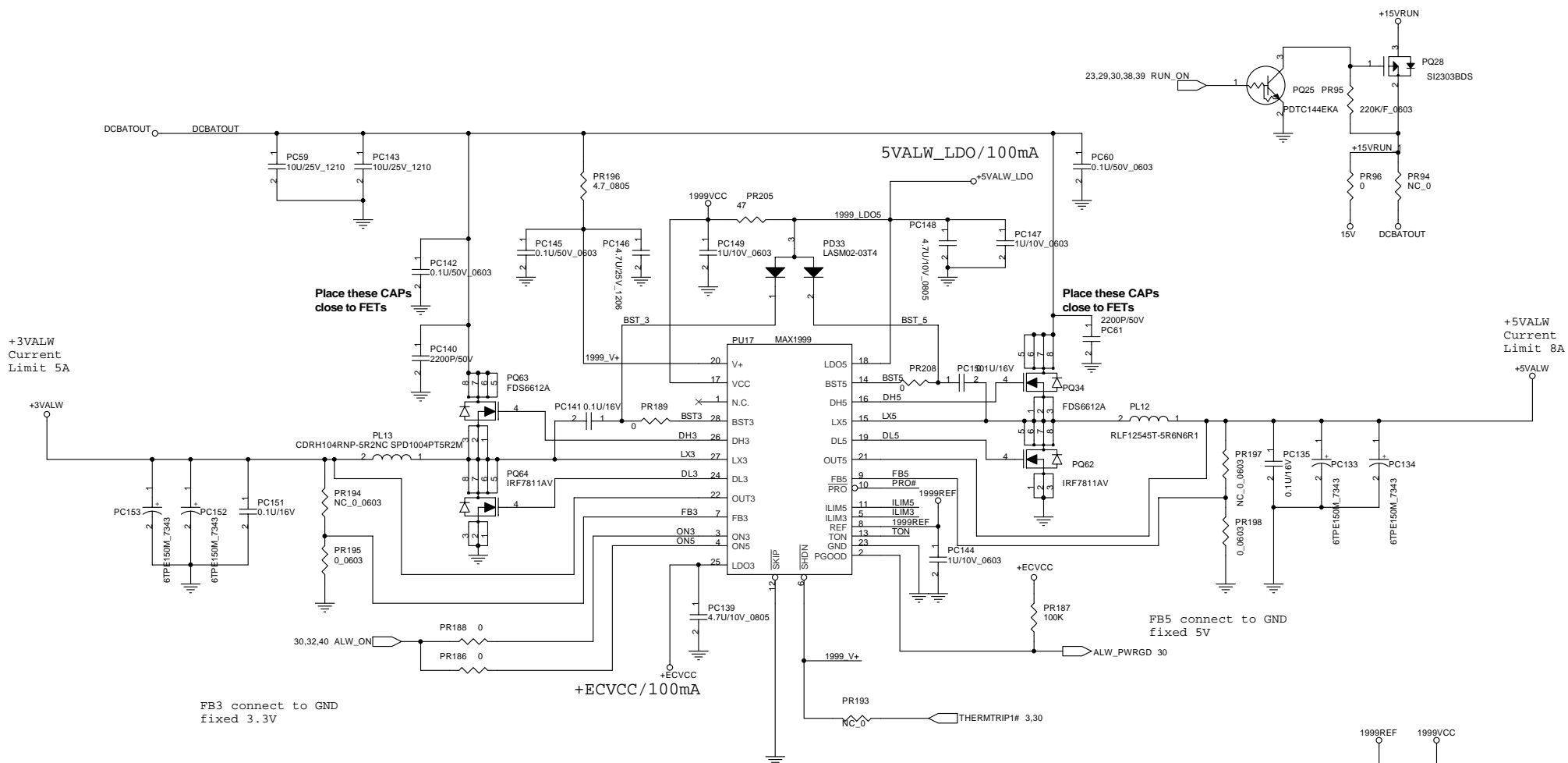
V_REF : 4.2235V (<500ua)
ISOURCE_MAX Current = 4A
So, Constant Power=19.5 *4=78W

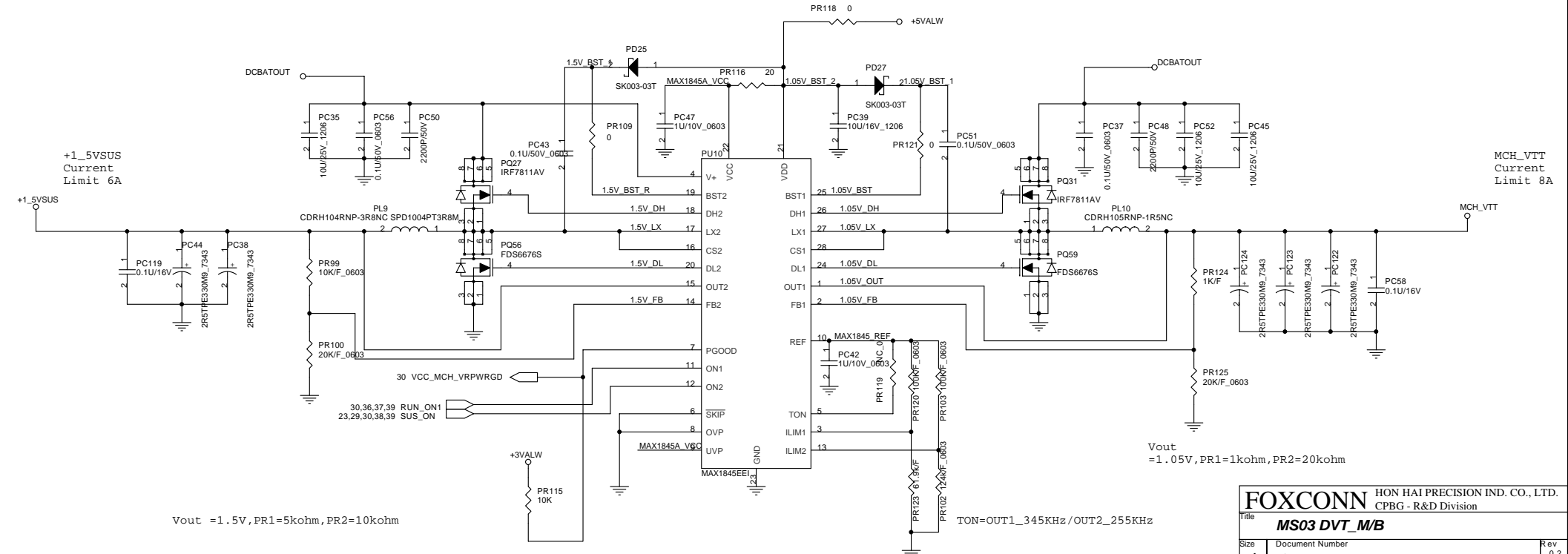
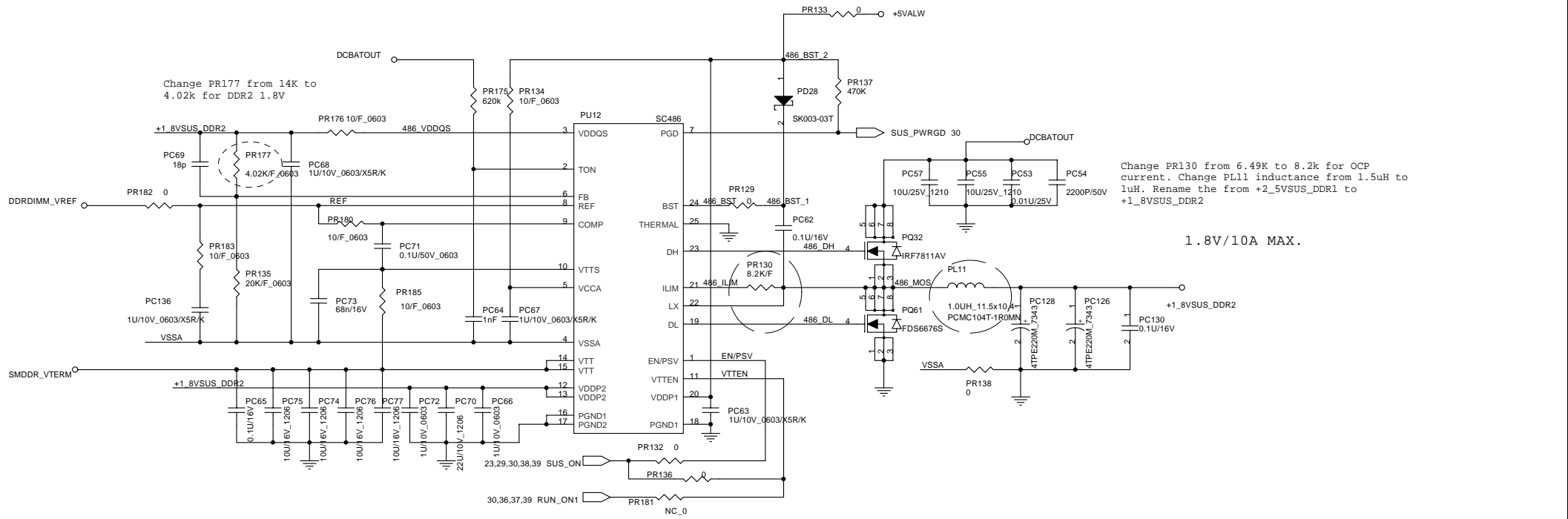
When battery in BATT_PRES# pull low

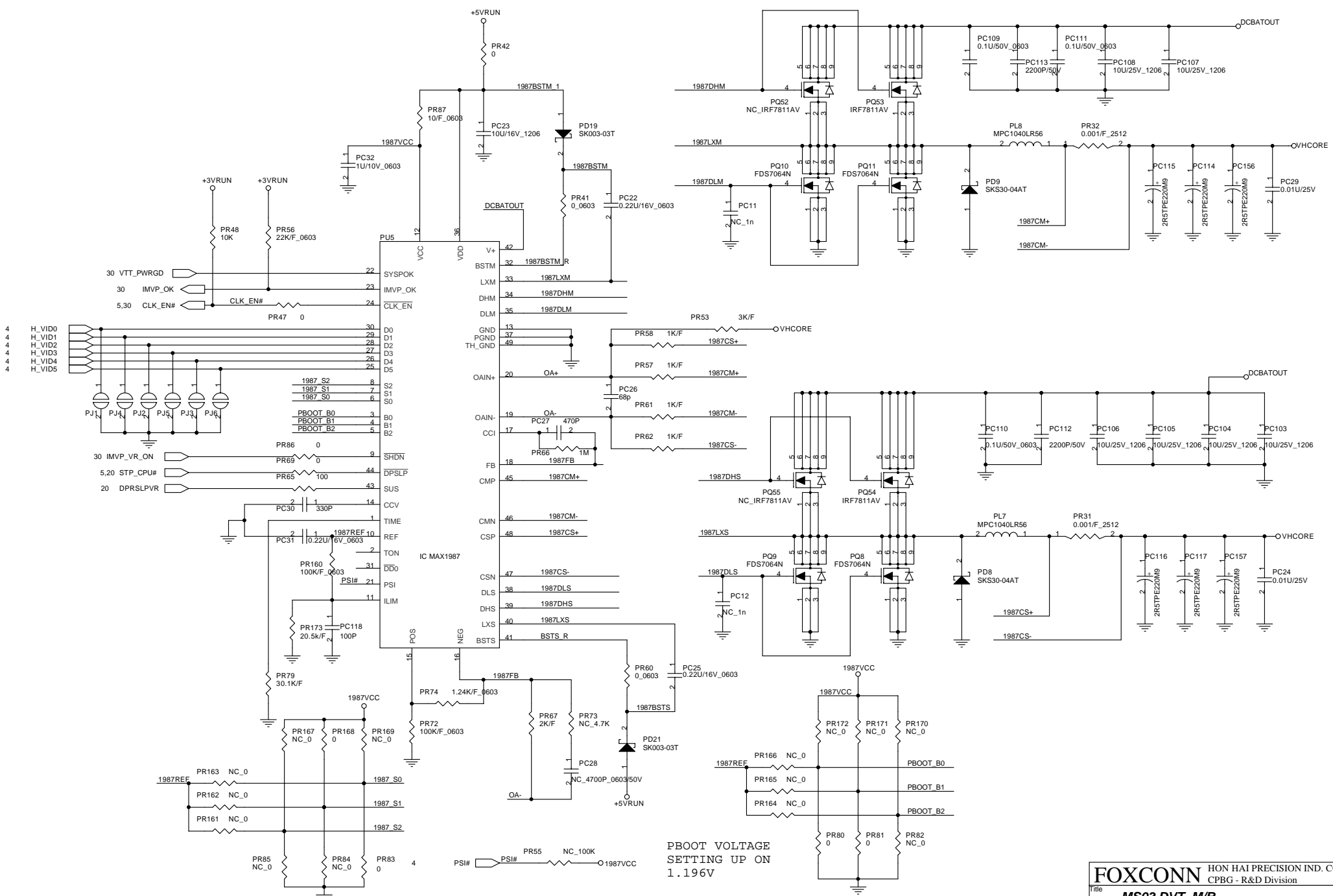
When Battery only and not power off, disconnect KBC power

Port Replicator connection

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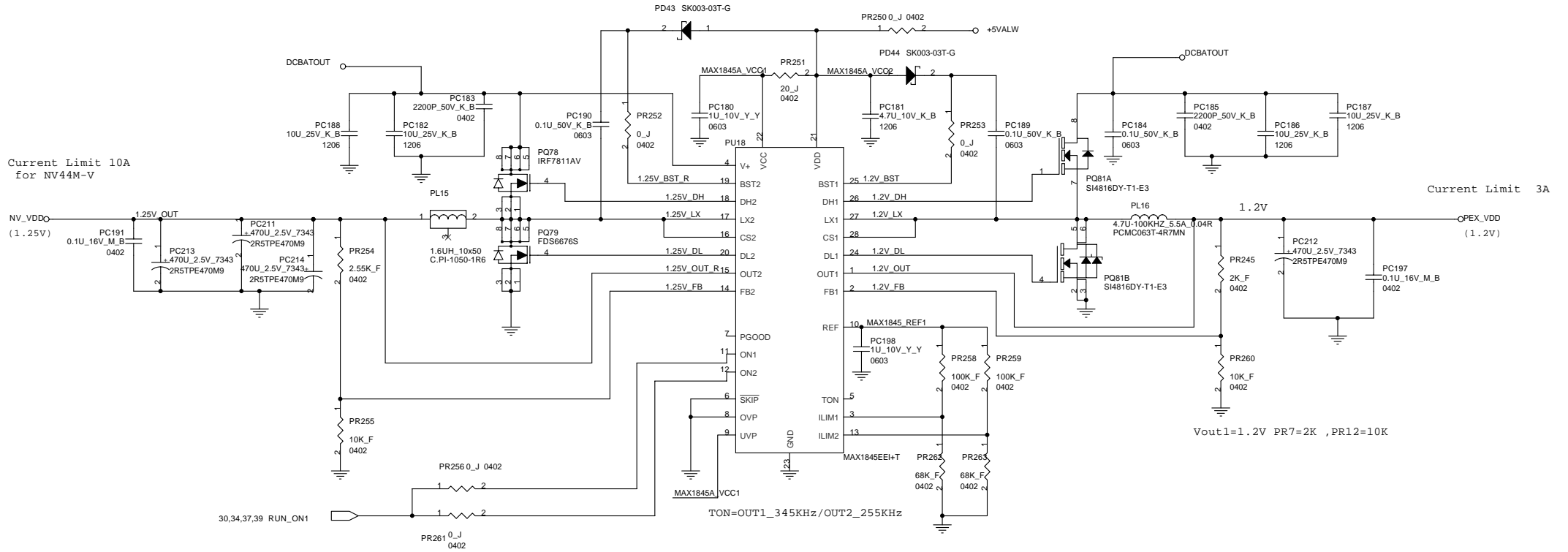


The C4 mode voltage is 0.748V TON = 300KHZ

PBOOT VOLTAGE SETTING UP ON 1.196V

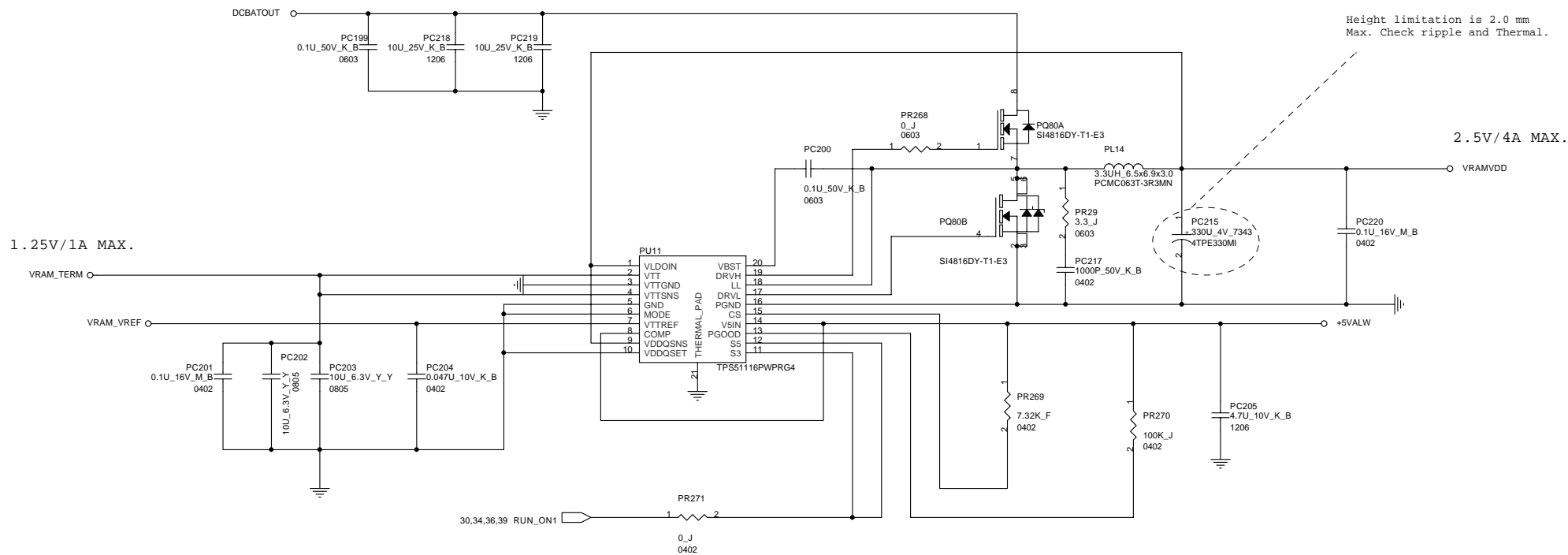
Current Limit 10A
for NV44M-V

Current Limit 3A

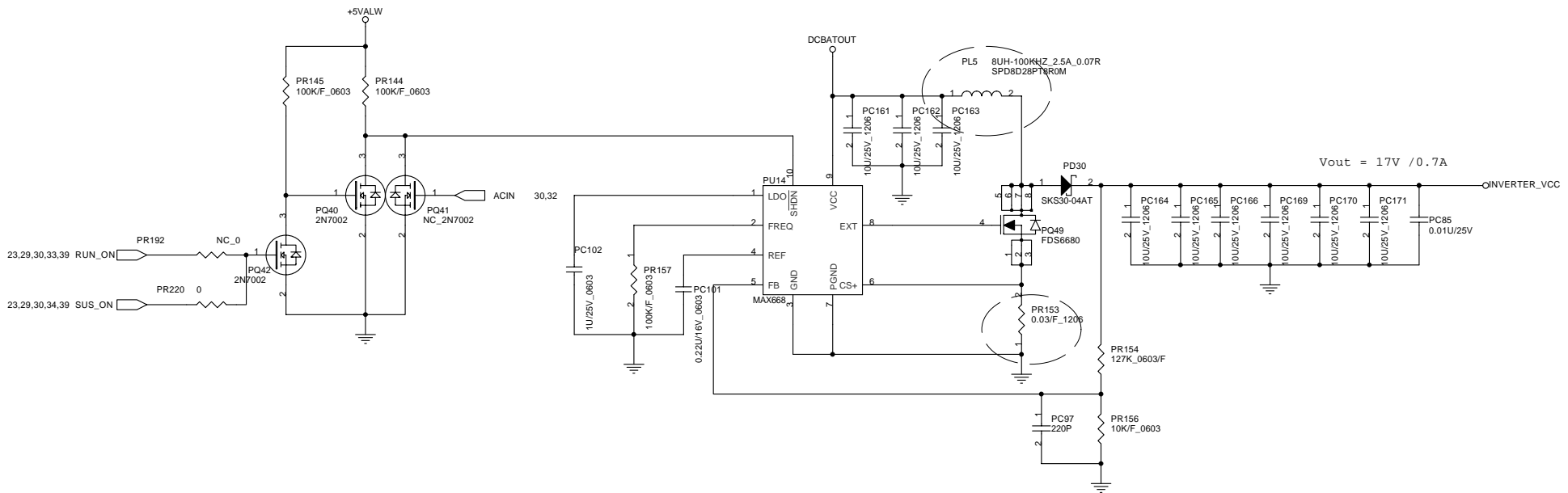


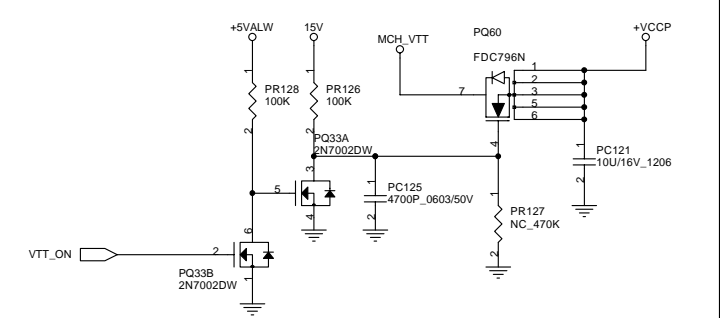
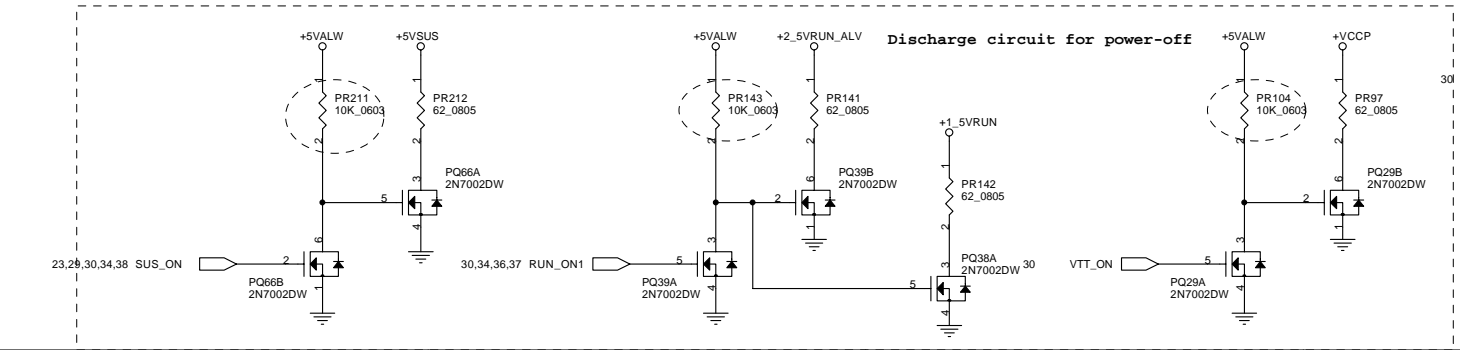
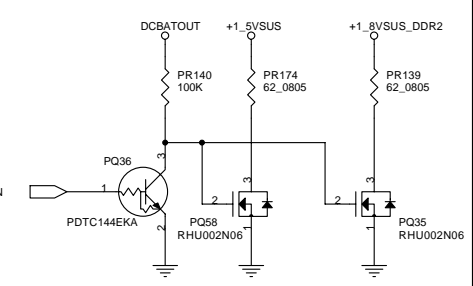
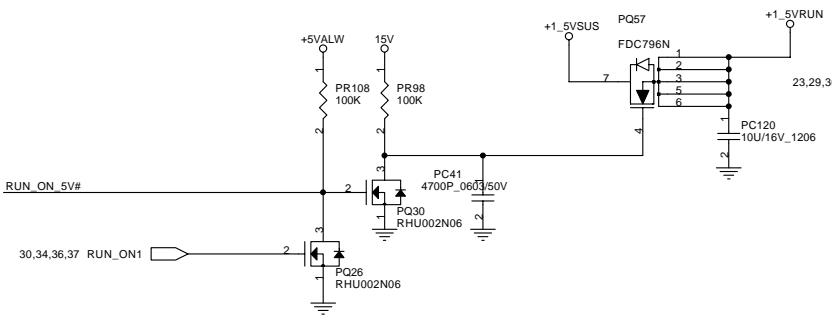
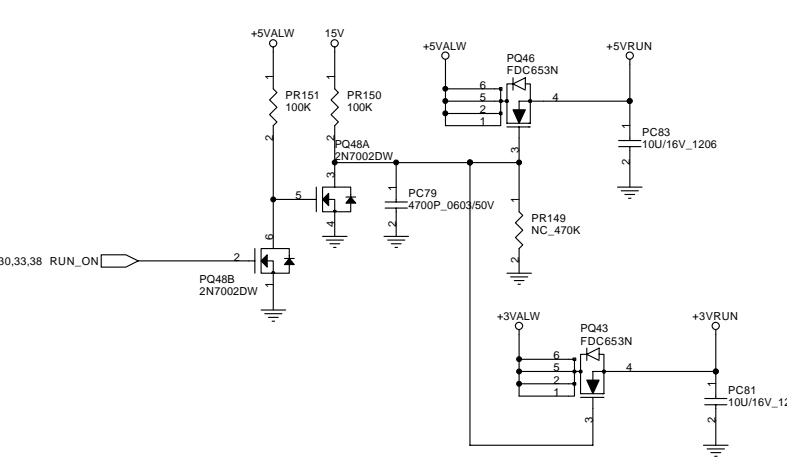
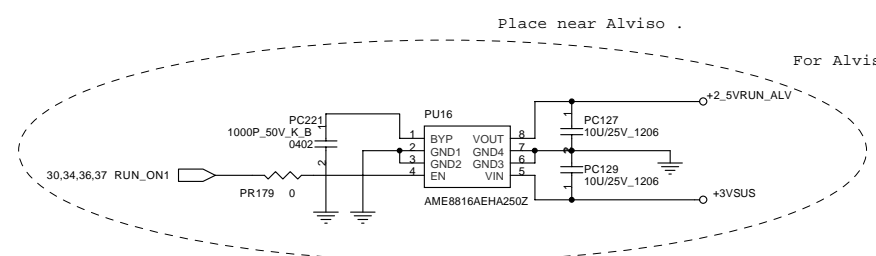
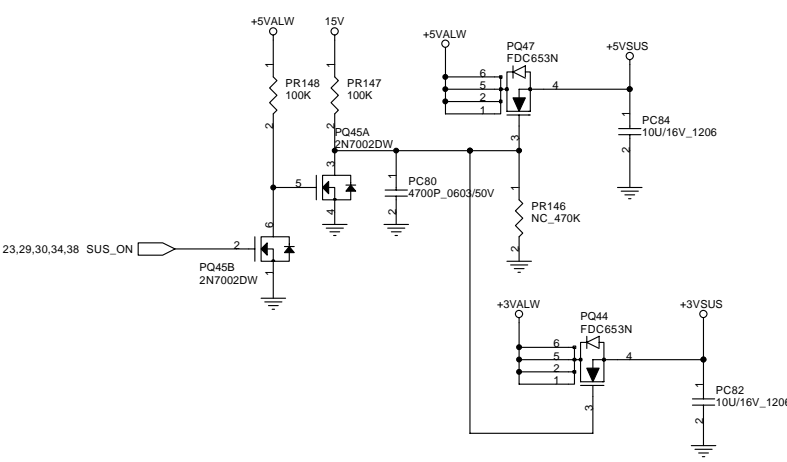
Power daughter board for VGA

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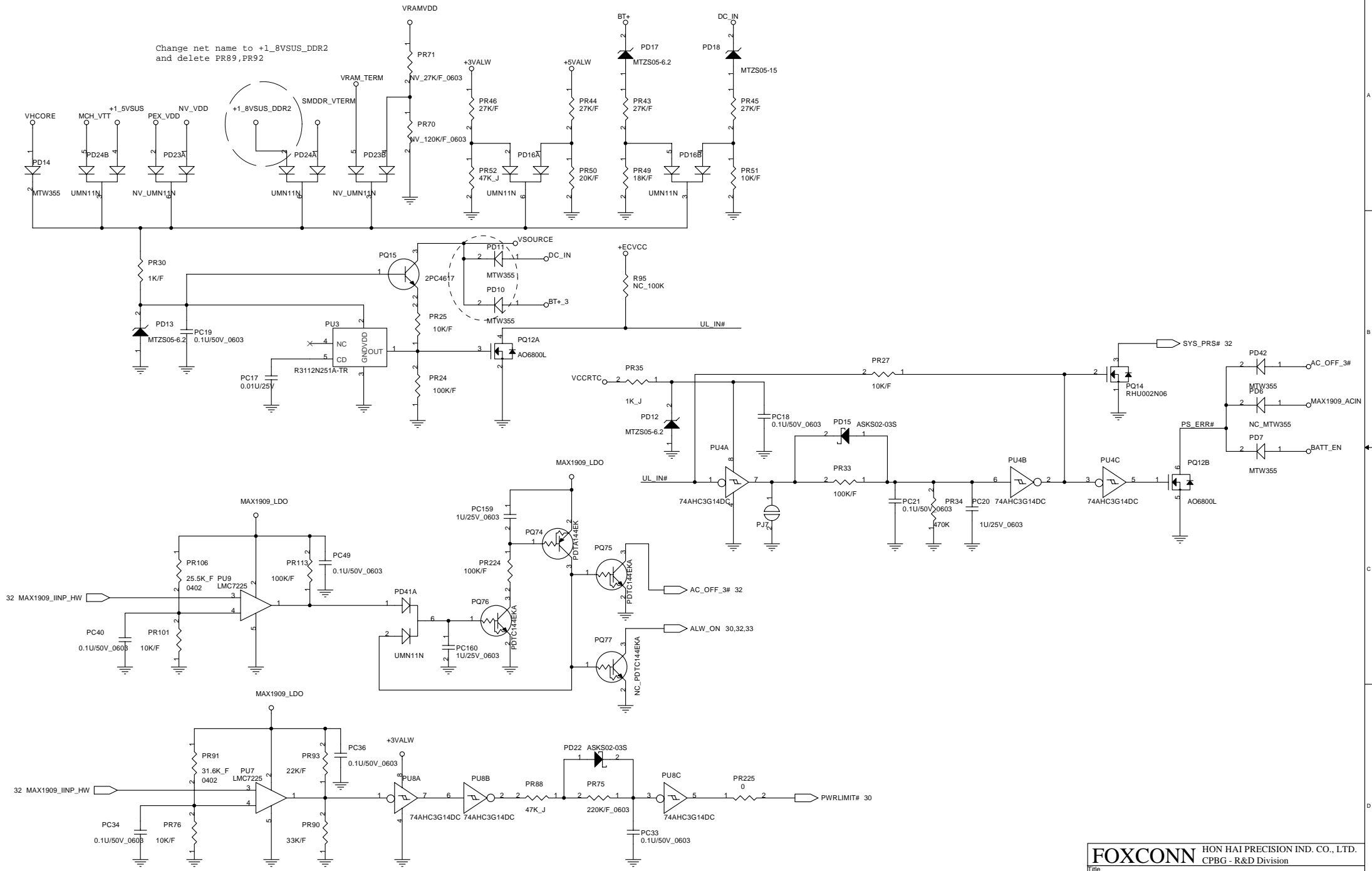


Change PL5 and PR153 for
improving the step-up
circuit





Change net name to +1_8VSUS_DDR2
and delete PR89,PR92



HISTORY

EVT board start .

(2005/03/31)
P14: Change D1 from NC to mount.
P15: Change R115 from mount to NC.

(2005/04/01)
P40: Rotate PD10, PD11.

(2005/04/12)
P14: Correct LVDS Bus relative of connection (swap Data+/Data-, CLK+/CLK-).
P25: Change CN14 pin16, pin17 from NC to +3VSUS, change CN14 pin18, pin20 from NC to GND.
P30: Delete SW7, Q46, R396, R721.

(2005/04/25)
P12: Add T195 for measure VRAM Timing.

(2005/04/26)
P14: Delete the right side dot of L1.

(2005/04/29)
P14: Change Q22, Q23 from 2N7002 to BSS138.

(2005/05/04)
P14: Change R694, R695, R696, R697 from 2.2K to 0 ohm.

(2005/05/09)
P26: Change H14 part from HOLE_6VIA_C256IN177D98_M2_V6(6.5mm) to HOLE_C236IN177D98_V6(6.0mm).
P15: Change R701 from NC to mount, change R702 from mount to NC.

(2005/05/10)
P32: Change PD3 from P4SSMJ24APT to MM3Z22VT1G.
P32: Change PQ5 from PDTCL44EKA to 2PC4617.
P32: Change PR5 from 75K/F_0603 to 10K/F_0402.
P32: Change PR6 from 120K_0603 to 10K/F_0402.
P32: Add PU19 AME, AME431BBJETB25Z.
P32: Add PR272 100K/F_0402.
P32: Add PR273 1K/F_0402.
P36: Change PR262 from 15.8K/F_0402 to 68K/F_0402.
P36: Change PR263 from 40.2K/F_0402 to 68K/F_0402.
P36: Change PL15 footprint from CHOKE_3P_348_409X409_2 to CHOKE_3P_315_394X394_2.
P36: Delete PJ11, PJ12.
P37: Delete PJ13, PJ14.
P39: Delete PJ8, PR178.
P39: Add PC221 1000P_50V_0402.
P39: Change PU16 from LP3875 to AME8816AEHA250Z.
P05: Change R478, R481 from 33ohm to 56ohm for rising edge rate and falling edge rate.
P05: Change C696, C698, C700, C701, C702, C706 from NC to 18pF (EMI solution).
P22: Add C730, C731 (EMI solution).
P22: Connect CN17.20, CN17.32, CN17.44 to GND.
P26: Change SPR7, SPR15 from mount to NC (EMI solution).

(2005/05/11)
P23: Add D33,D34 and D35 for ESD(Not mount).
P36: Change PL15 footprint from CHOKE_3P_348_409X409_2 to L_3P_315_394X394.

(2005/05/13)
P26: Change H25, H26 footprint from ho_tc236bc158d47_v6 to ho_tc236bc158d47_mt.
P26: Change H27, H28 footprint from ho_tc1p5bc6d1p2_m2 to ho_tc1p5bc6d1p2_mb.

(2005/05/16)
P02: Update symbol ahead table, add LNC_ and HMNC_.
P30: Change R280 from mount to NC.
P30: Change R281 from AL_100K to LNC_100K.
P30: Change R293 from NC to mount.
P30: Change R294 from NV_100K to HMNC_100K.

(2005/05/17)
P26: Add R32, R33 NC_0_J (EMI solution).

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HISTORY

(2005/05/18)

- P29: Change C783, C837 from 1U/10V_0603 to 2.2U_10V_Y_Y.
- P26: Change H27, H28 from ho_tc1p5bc6d1p2_m2(ho_tc1p5bc6d1p2_mb) to hole_tc6bc1p5d1p2_mt(ho_tc6bc1p5d1p2_mt).
- P40: Change PR91 from 31.6K to 25.5K, change PR109 from 49.9K to 31.6K.
- P29: Delete R611, R622, R628, R629, R647, R648, R649, R650, JSPK1.
- P29: Add C910, C911 NC_100U_6.3V_7343.

(2005/05/19)

- P29: Add R734,R735 for anti-digital noise interference.

(2005/05/20)

- P30: Change R311, R314 from 10K to 4.7K_J.
- P29: Change R735 from mount to NC.
- P05: Change R481 from 56ohm to 47ohm.
- P05: Change R478 from 56ohm to 47ohm.

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