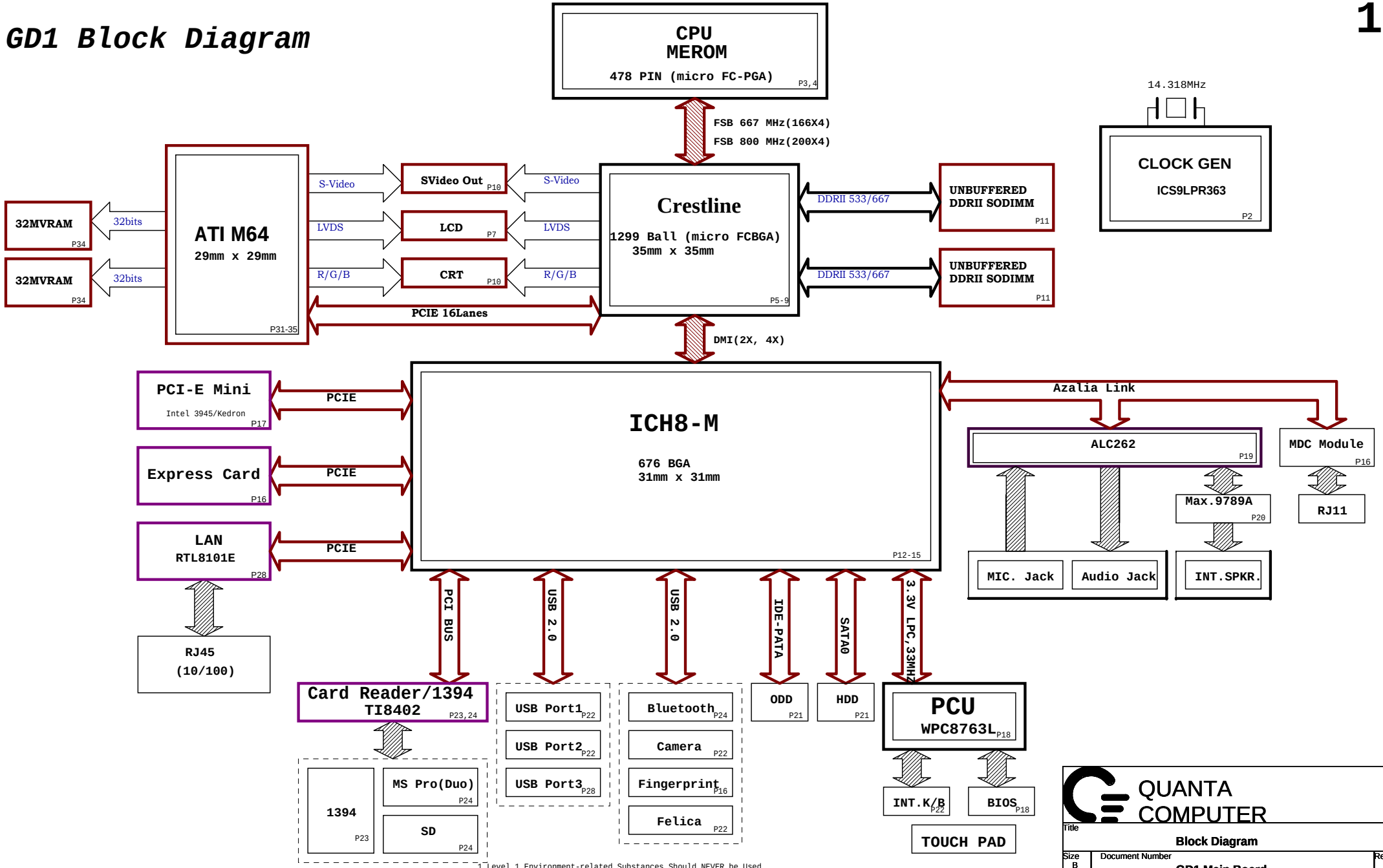
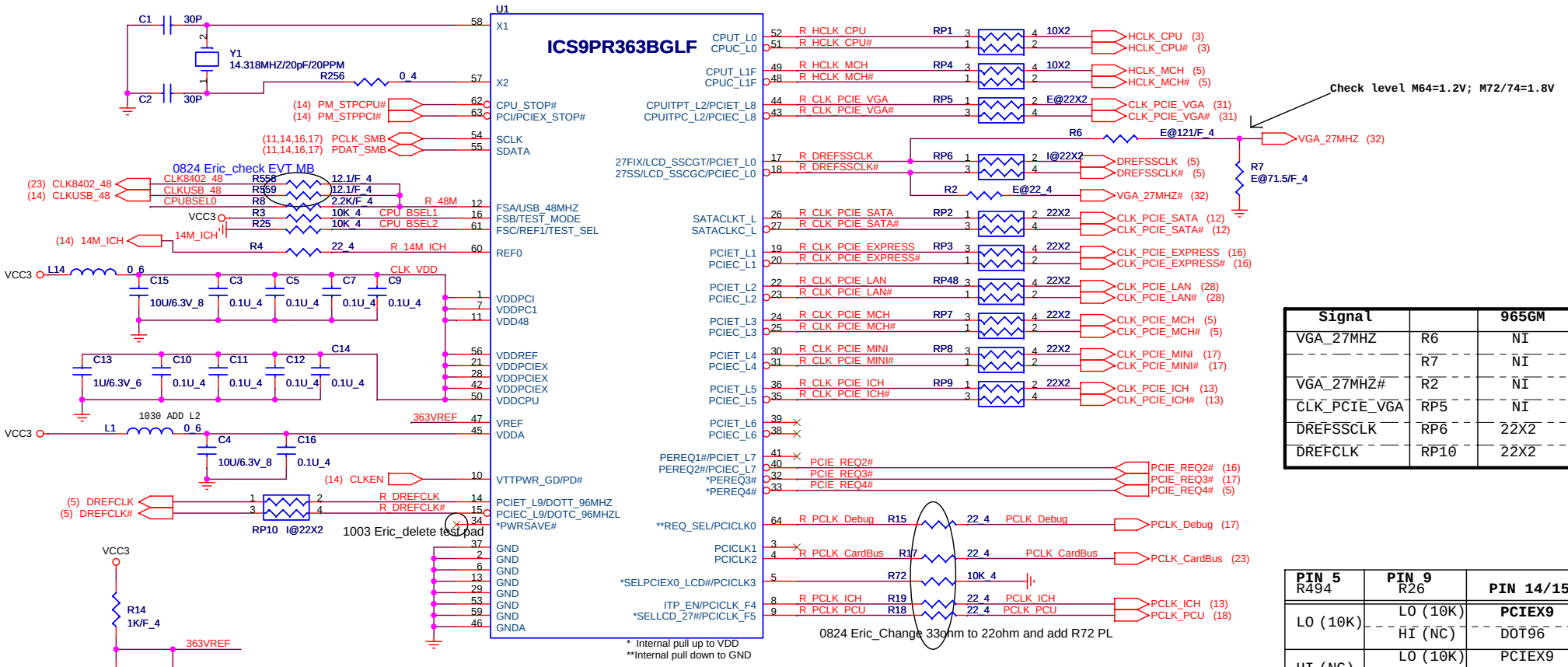
GD1 Block Diagram



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	Block Diagram	
Size B	Document Number GD1 Main Board	Rev 1A
Date: Tuesday, November 14, 2006	Sheet 1 of 35	



Signal		965GM	965PM
VGA_27MHZ	R6	NI	121
	R7	NI	71.5
VGA_27MHZ#	R2	NI	22
CLK_PCIE_VGA	RP5	NI	22X2
DREFSSCLK	RP6	22X2	NI
DREFCLK	RP10	22X2	NI

PIN 5 R494	PIN 9 R26	PIN 14/15	PIN 17/18
LO (10K)	LO (10K)	PCIEX9	27MHZ
	HI (NC)	DOT96	LCD
HI (NC)	LO (10K)	PCIEX9	PCIEX0
	HI (NC)	DOT96	PCIEX0

ITP_EN(PIN8)
LOW : PIN43/44 SRC
HIGH : PIN43,44 CPUITP

PCIE_REQ1#	PCIE_L0	PCIE_L6		
PCIE_REQ2#	PCIE_L1	PCIE_L8		
PCIE_REQ3#	PCIE_L2	PCIE_L4		
PCIE_REQ4#	PCIE_L3	PCIE_L5	PCIE_L7	

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
* 0	1	0	**200.00**	100	33.33	14.318	48	96	0.5 Down
0	1	1	166.66	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	200.00	100	33.33	14.318	48	96	0.5 Down

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: CLOCK GENERATOR

Size: B | Document Number: GD1 Main Board | Rev: 1A

Date: Wednesday, November 15, 2006 | Sheet 2 of 35

U2A

ADDR GROUP 0

ADDR GROUP 1

CONTROL

XDP/ITP SIGNALS

THERMAL

H CLK

RESERVED

FOX(PZ47913-2741-41)

U2B

DATA GRP 0

DATA GRP 2

DATA GRP 1

DATA GRP 3

MISC

FOX(PZ47913-2741-41)

0920 Eric_Check list V1.301

<Check list & CRB>H_GTLREF
Layout note: Z=55 ohm
H_GTLREF<0.5"

Layout note:
Comp0,2 connect with
Zo=27.4ohm, make
trace length shorter than 0.5".
Comp1,3 connect with Zo=55ohm,
make
trace length shorter than 0.5".

0920 Edward_add

<check list>R32
Default PU 56ohm if no
use.Serial R NC
If connect to power side PU
68ohm.Serial R 2.2K

1016 Hunson_Remove PU_R41
Power PU PR255 near CPU CORE

1025 Sun_Change to 10K

1012 Hunson_ADD NMOS

XDP PU

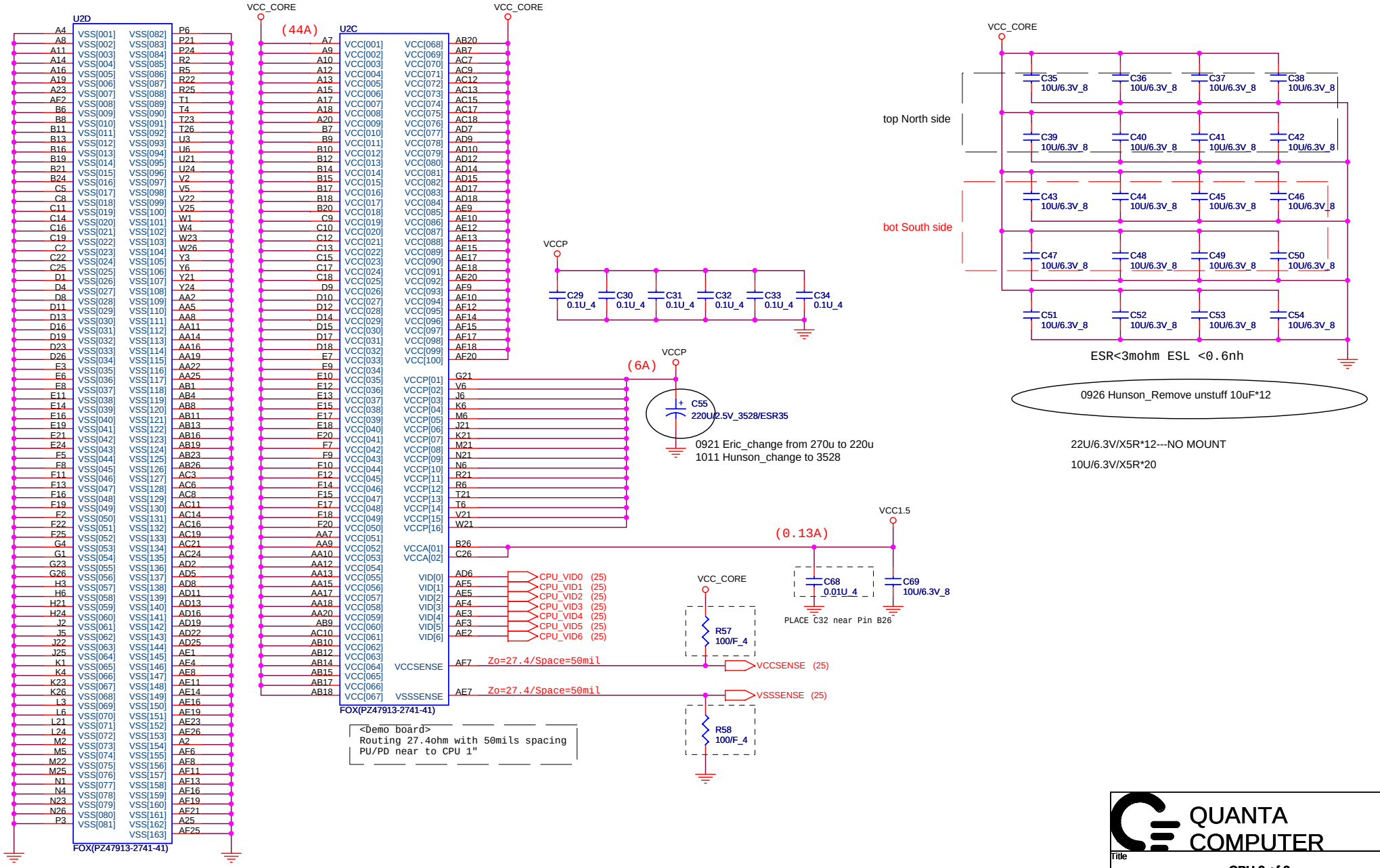
Thermal Sensor

Themal SMBUS

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

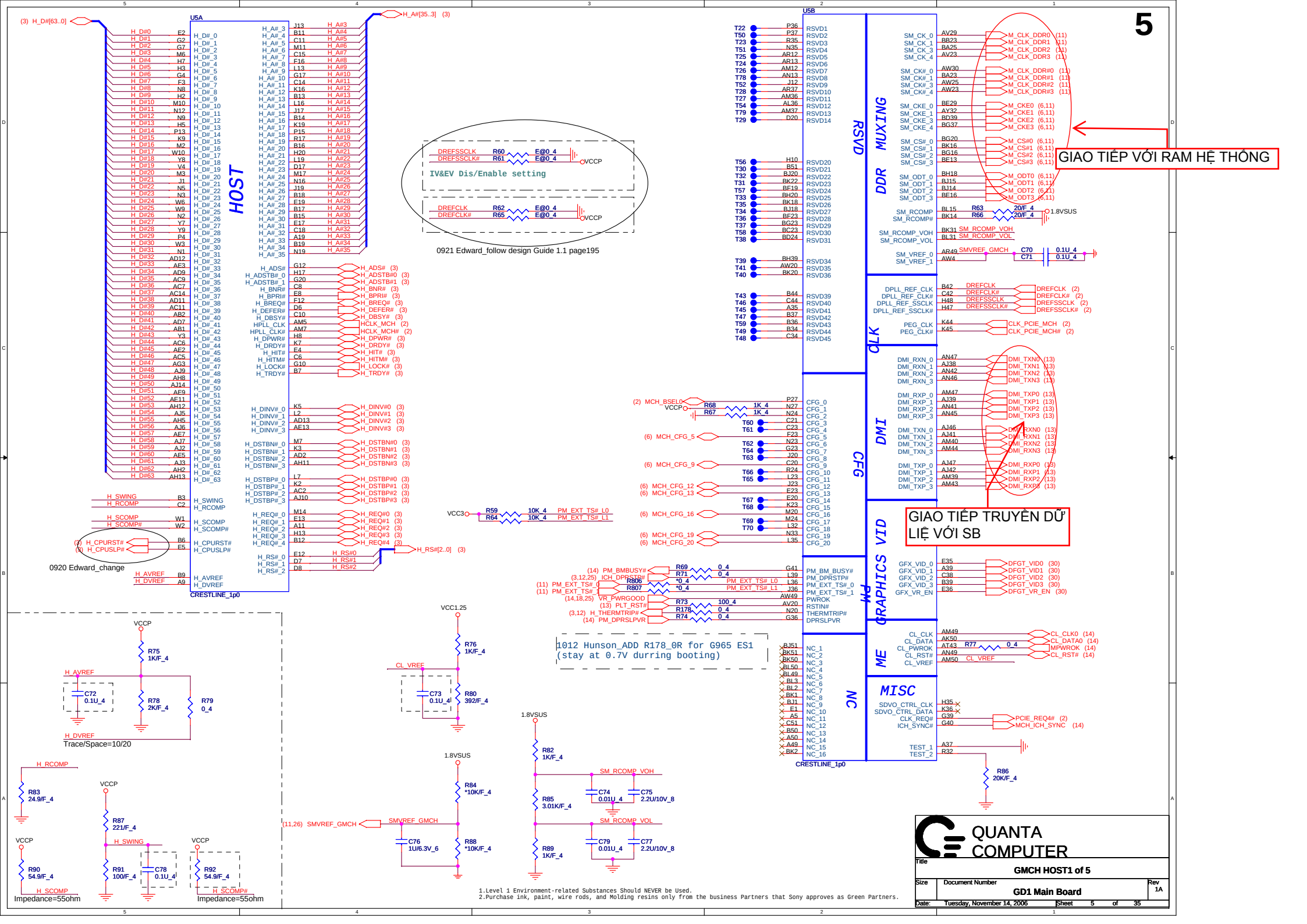
Title	CPU1 of 2	
Size	Document Number: GD1 Main Board	Rev: 1A
Date: Tuesday, November 14, 2006	Sheet 3 of 35	

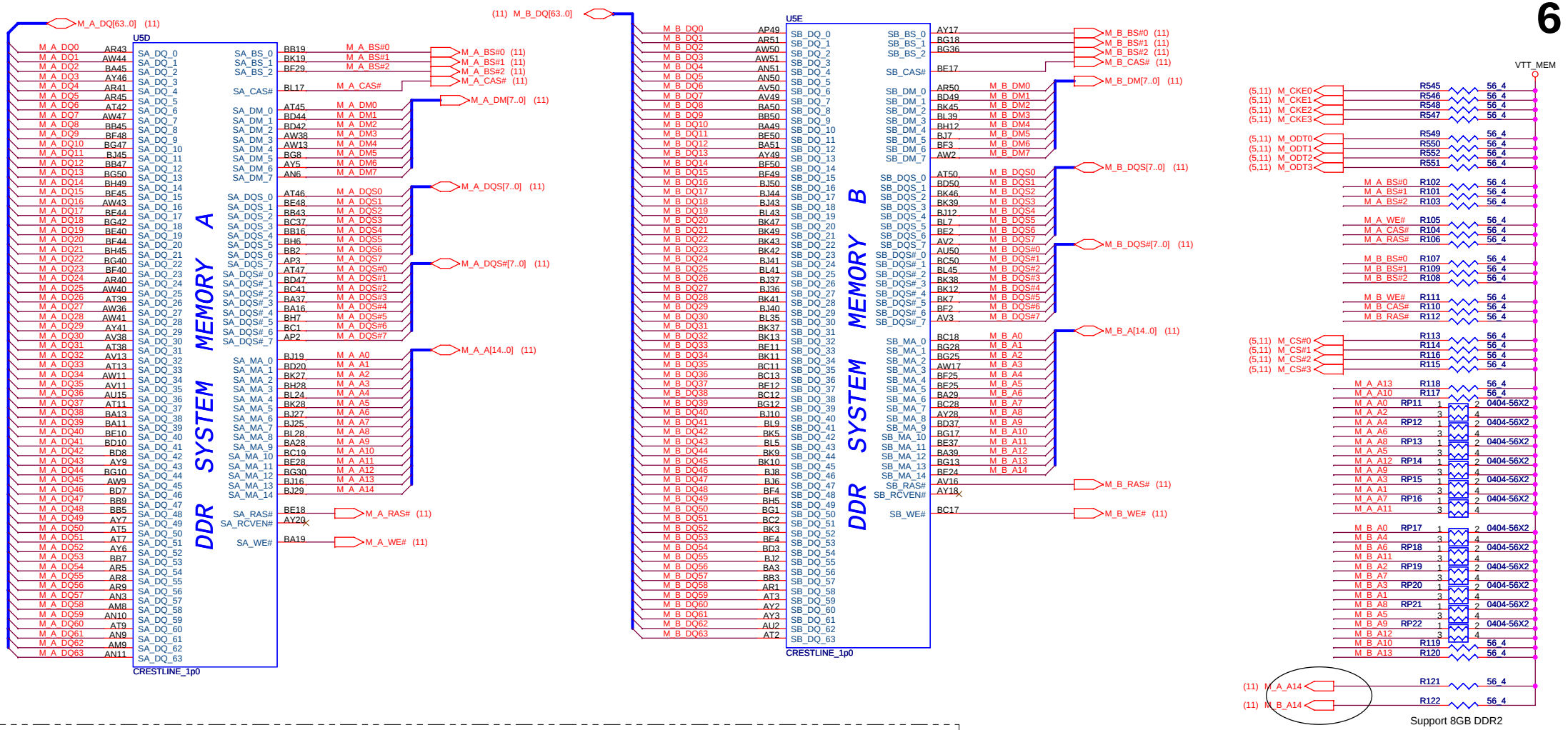


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: CPU 2 of 2		
Size: B	Document Number: GD1 Main Board	Rev: 1A
Date: Tuesday, November 14, 2006	Sheet 4 of 35	


5
U5A
HOST
CRESTLINE_1p0
U5B
RSVD
DDR MUXING
CLK
DMI
CFG
VID
GRAPHICS
PM
ME
NC
MISC
GIAO TIẾP VỚI RAM HỆ THỐNG
GIAO TIẾP TRUYỀN DỮ LIỆU VỚI SB
IV&EV Dis/Enable setting
0921 Edward_follow design Guide 1.1 page195
0920 Edward_change
1012 Hunson_ADD R178_0R for G965 ES1
(stay at 0.7V durring booting)
Trace/Space=10/20
Impedance=55ohm
Impedance=55ohm
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.
QUANTA COMPUTER
Title
GMCH HOST1 of 5
Size
Document Number
GD1 Main Board
Rev
1A
Date: Tuesday, November 14, 2006
Sheet 5 of 35



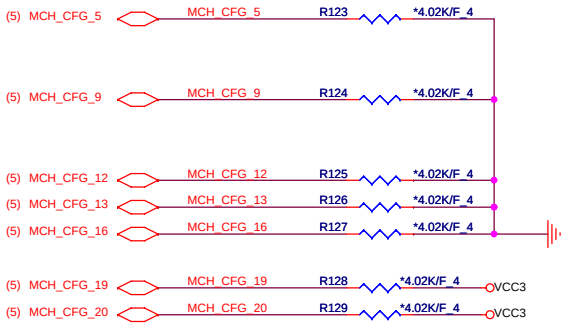
GMCH Strap pin description

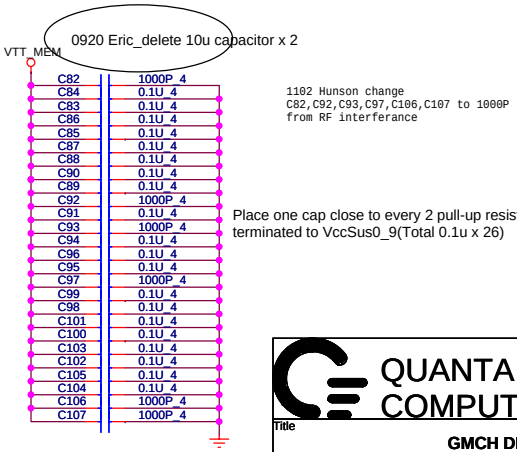
		Low		High
CGF5		DMIx2	*	DMIx4
CGF6		RSVD for 945GMS		
CGF7		RSVD	*	CPU type: Mobile CPU
CGF9		PCIE Graphics lan : Reverse Lane	*	PCIE Graphics lan : Normal operation
CGF10		reserved		
CGF11		reserved		
CGF16		FSB Dynamic ODT Disabled	*	FSB Dynamic ODT Enabled
CGF18	*	GMCH core: 1.05V		GMCH core: 1.5V
CGF19	*	DMI LANE Normal		DMI LANE Reversed
CGF20	*	only SDVO or PCIE x1 is operational		SDVO and PCIE x1 are operation simultaneously via the PEG port

CGF[13:12]

00 = Partial clock gating disable
01 = XOR mode enabled
10 = All-Z mode enabled
* 11 = Normal Operation(Default)

int.Pull-down : CFG 18,19,20
Int.Pull-high : CFG CFG 3~17





1102 Hunson change
C82,C92,C93,C97,C106,C107 to 1000P
from RF interferance

Place one cap close to every 2 pull-up resistors
terminated to VccSus0_9(Total 0.1u x 26)

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	GMCH DDR II 2 of 5		
Size	Document Number		Rev
	GD1 Main Board		1A
Date:	Tuesday, November 14, 2006	Sheet 6 of 35	

E@: PM965(EXT) should mount
I@: GM965(INT) should mount
@:please refer to form nearly

Signal		GM965	PM965
NB_VSYNC	R158	NI	0_4
	R168	30.1_4	NI
NB_HSYNC	R159	NI	0_4
	R166	30.1_4	NI
GFX	C112, C114~C129, C130~C145	NI	0.1UF_4

Signal		965GM	965PM
NB_B	R160	0_4	NI
	R155	150_4	0_4
NB_G	R161	0_4	NI
	R157	150_4	0_4
NB_R	R162	0_4	NI
	R156	150_4	0_4
L_IBG	R147	2.4K_4	NI
LVDS	RP38 RP41~RP43	0X2	NI
L_BKLT_EN	R170	0_4	NI
L_CTRL_CLK	R130	10K	NI
	RP46	NI	0X4
L_CTRL_DATA	R145	10K	NI
	RP46	NI	0X4
LVDS_VDDEN	R146	0_4	NI
DDC2BC	R163	0_4	NI
	R553	NI	0_4
DDC2BD	R164	0_4	NI
	R554	NI	0_4
CRT_TVO_IREF	R167	1.3K_4	0
L_DDC_CLK	RP46	NI	0X4
L_DDC_DATA	RP46	NI	0X4
BRIGHT	R173	0_4	NI
	R175	NI	0_4

U5C

PCI-EXPRESS GRAPHICS

LVDS

TV

VGA

0912 Edward_exchange G27 and K27

1013 Edward_ADD PD R431_75R

1025 Edware_ADD PD 0R@ EXT GFX

SM Bus PD

CRT PU/PD

NB LVDS enable

LVDS

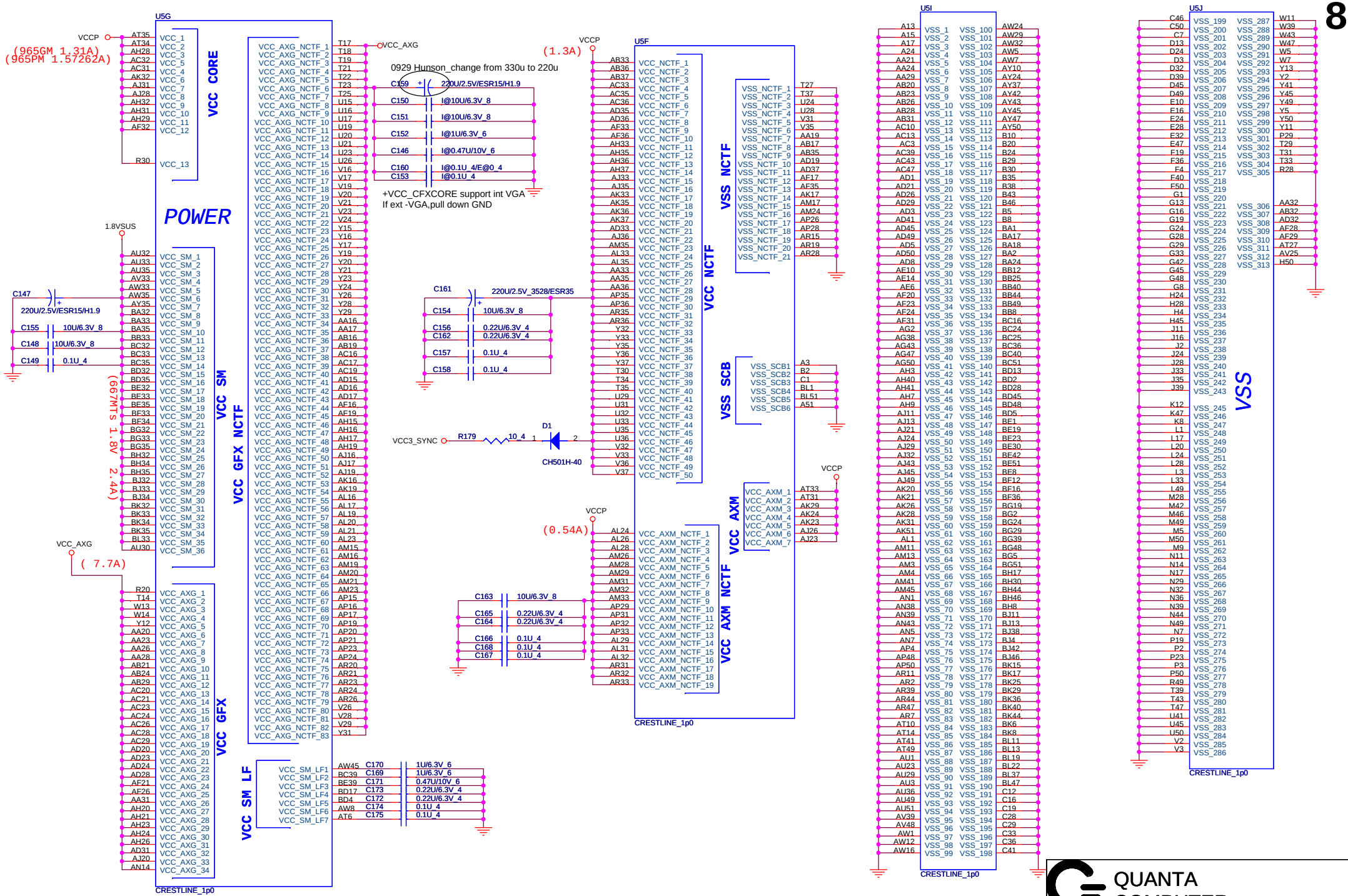
Display On

1026 Hunson_Change R171 to 10K

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

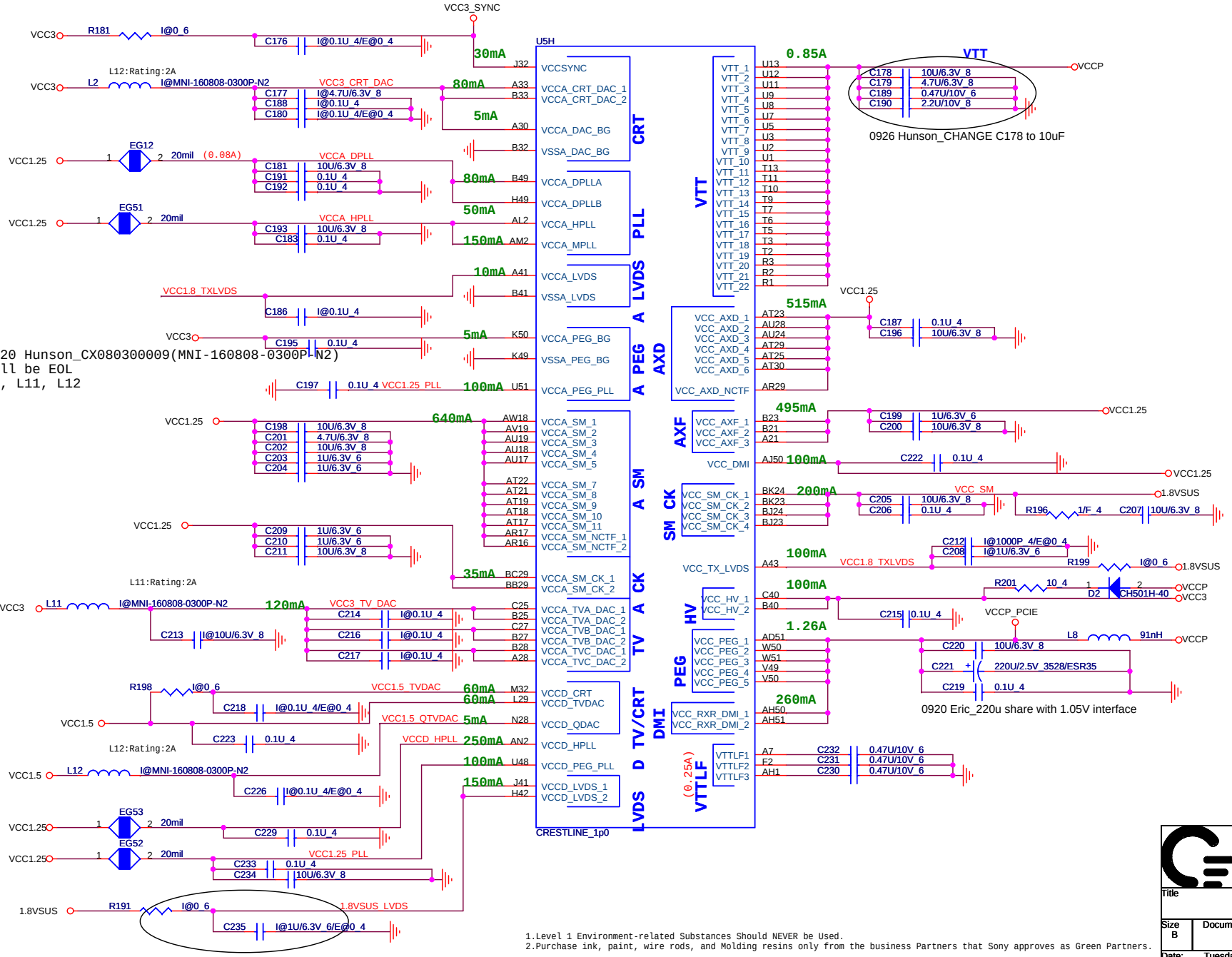
Title	GMCH DMI VEDIO 3 of 5		
Size	Document Number	GD1 Main Board	Rev 1A
Date: Tuesday, November 14, 2006	Sheet 7 of 35		



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	GMCH Power 4 of 5	
Size	Document Number: GD1 Main Board	Rev: 1A
Date: Tuesday, November 14, 2006	Sheet 8 of 35	



Signal		965GM	965PM
VCCA_TV_DAC	L12	V	X
	C244	V	X
	C245	V	X
	C246	V	X
	C248	V	X
	R193	X	V
VCC1.5_TVDAC	L14	V	X
	C250	V	X
	C247	V	X
	R195	X	V
VCC1.5_QTVDAC	L17	V	X
	C257	V	X
	C258	V	X
	R197	X	V

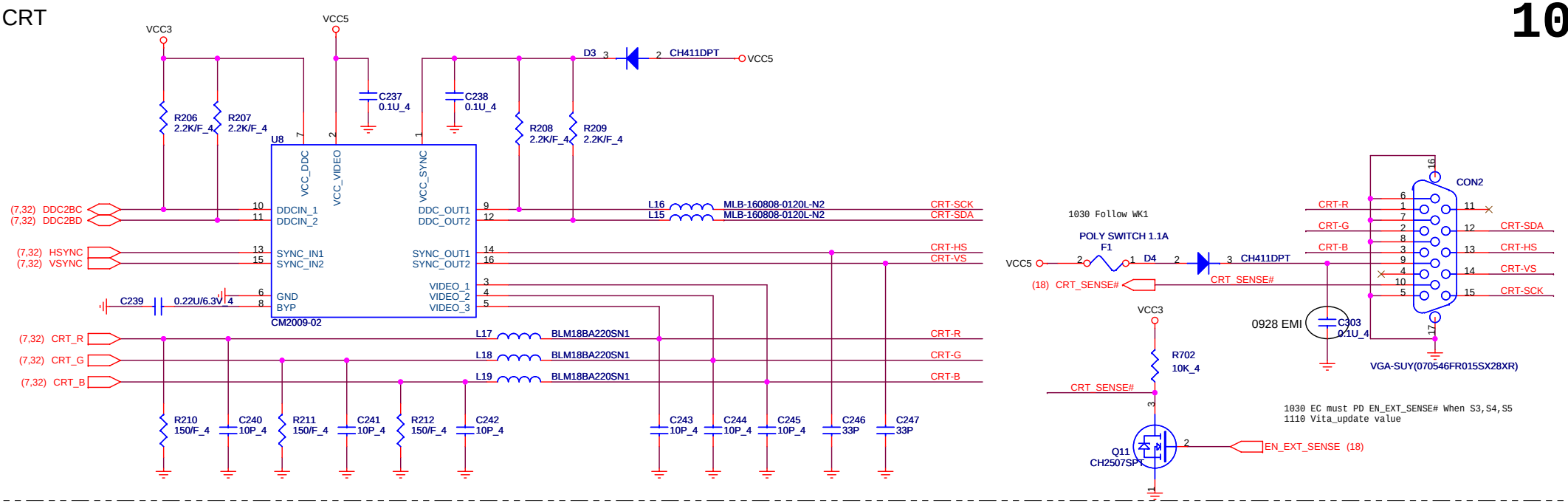
Signal		965GM	965PM
VCCA_DAC_BG	L8	V	X
	C214	V	X
	R181	X	V
VCCSYNC	R177	V	X
	C201	V	X
	C202	V	X
	R178	X	V
VCC3_CRT_DAC	L7	V	X
	C203	V	X
	C211	V	X
	R179	X	V
VCCD_LVDS	R198	V	X
	C265	V	X
	C264	V	X
	R199	X	V
VCCA_LVDS	R183	0_4	NC
	C208	0.01u_4	NC
	C209	0.1u_4	NC
	R184	NC	0_4
VCC_TX_LVDS	R192	V	X
	C240	V	X
	C238	V	X
	R191	X	V

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

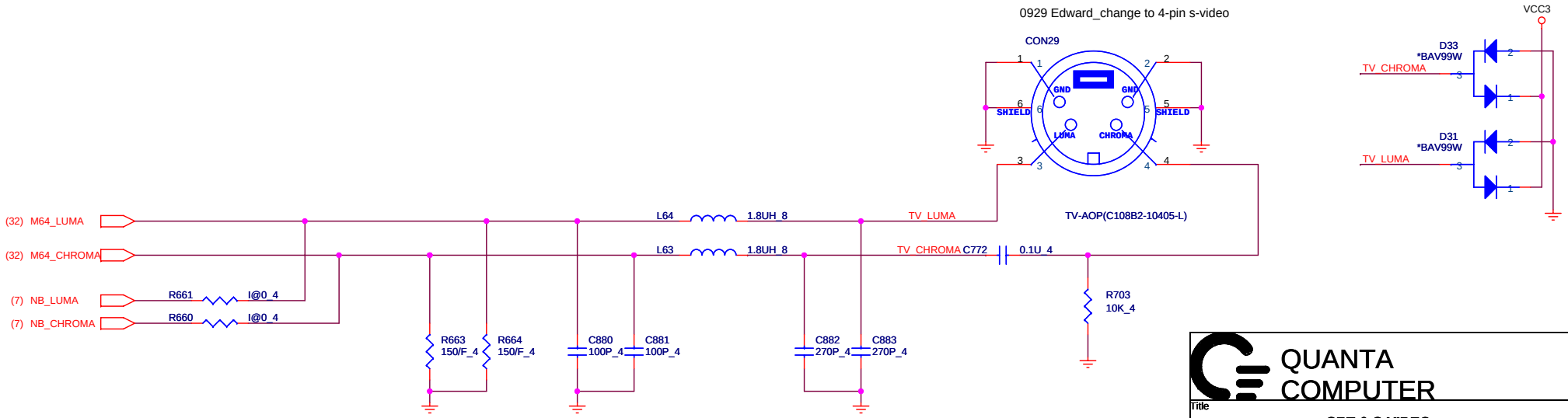
QUANTA COMPUTER

Title	GMCH Power 2 5 of 5	
Size B	Document Number GD1 Main Board	Rev 1A
Date: Tuesday, November 14, 2006	Sheet 9 of 35	

CRT



S-VIDEO_OUT

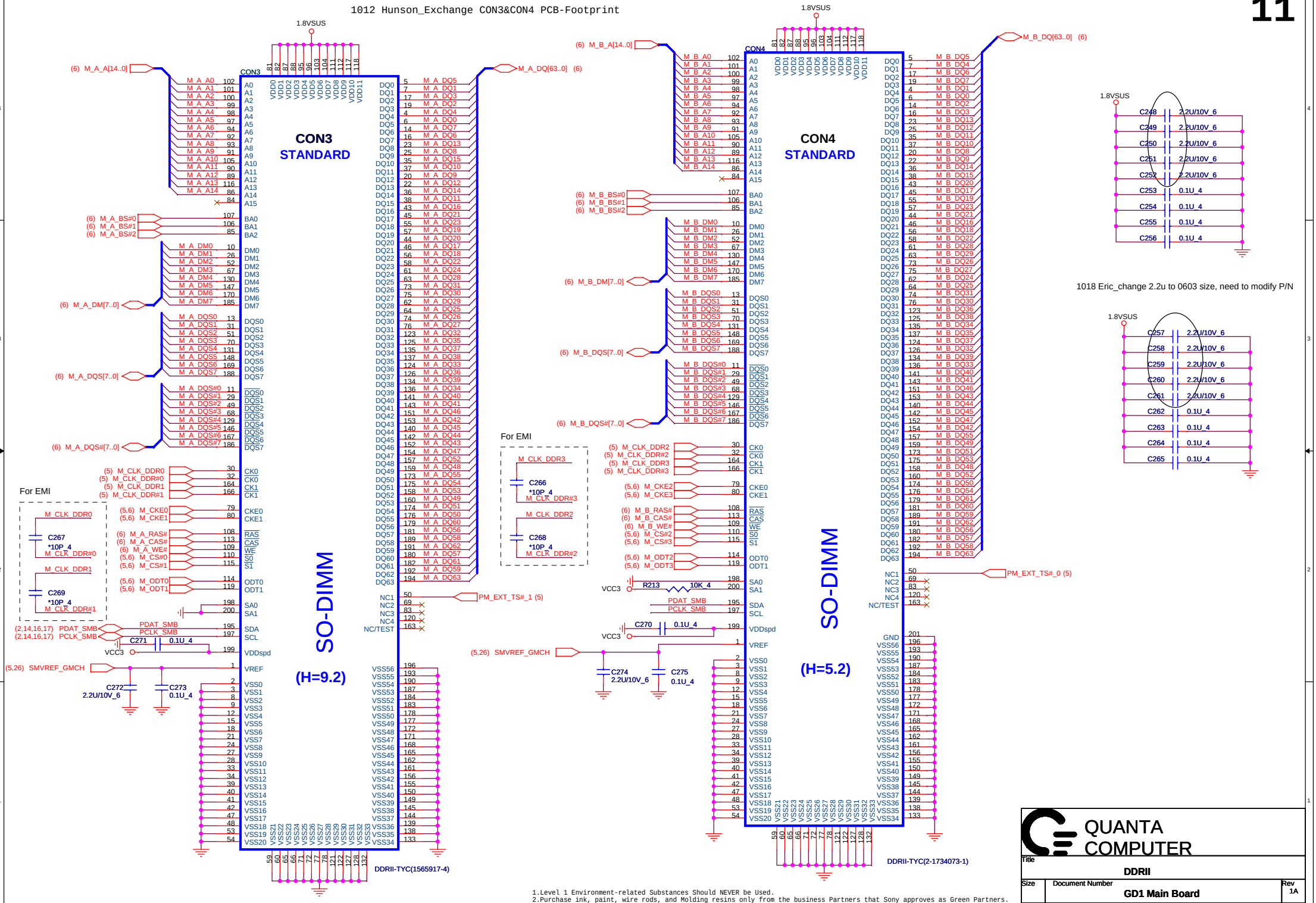


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	CRT & S-VIDEO	
Size B	Document Number GD1 Main Board	Rev 1A
Date: Wednesday, November 15, 2006	Sheet 10 of 35	

1012 Hunson_Exchange CON3&CON4 PCB-Footprint



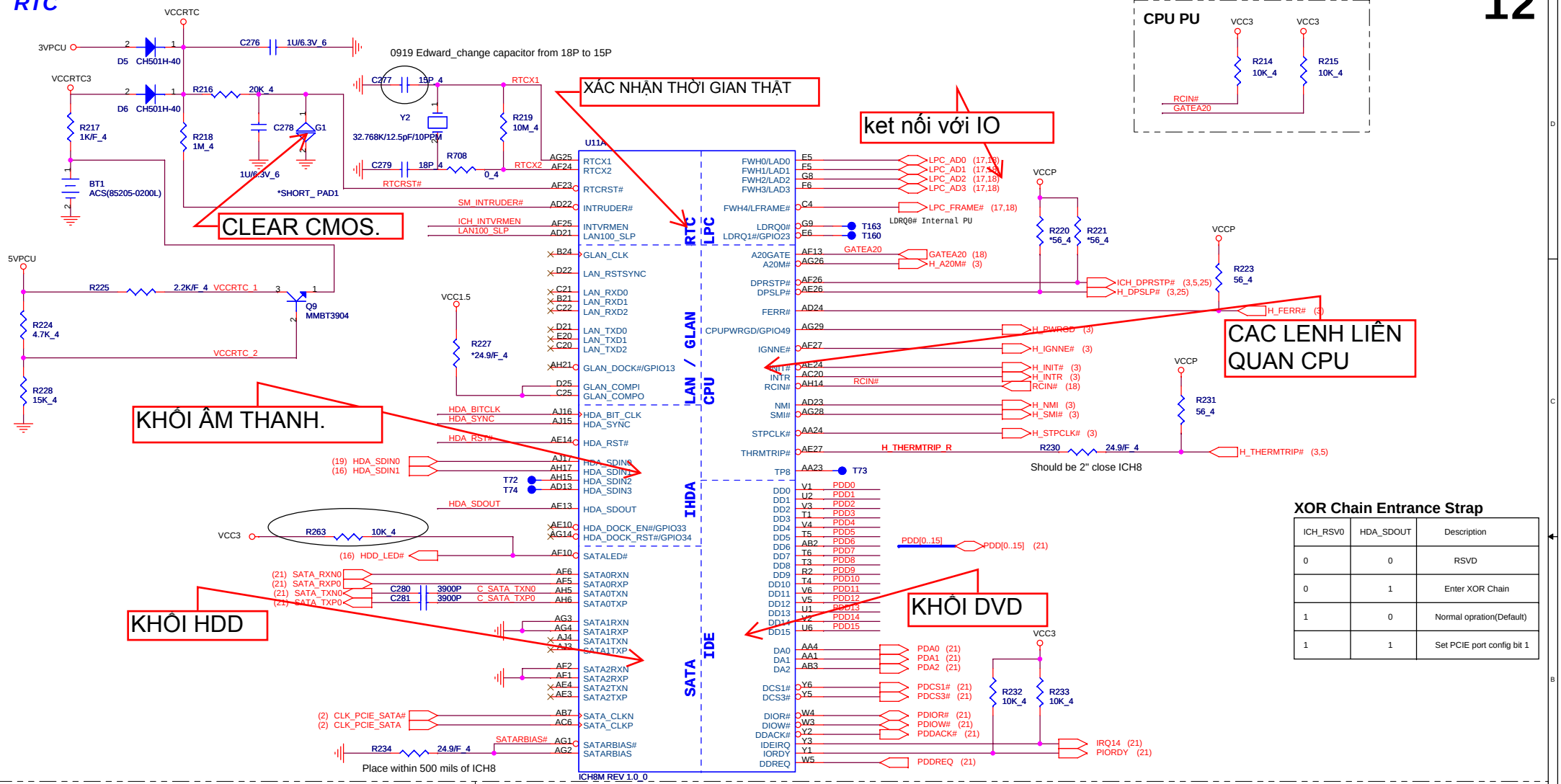
1018 Eric_change 2.2u to 0603 size, need to modify P/N

1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	DDRII	
Size	Document Number: GD1 Main Board	Rev: 1A
Date: Wednesday, November 15, 2006	Sheet 11 of 35	

RTC



CPU PU

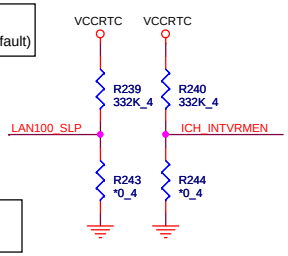
XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal opration(Default)
1	1	Set PCIE port config bit 1

ICH8 strap

ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1.05)

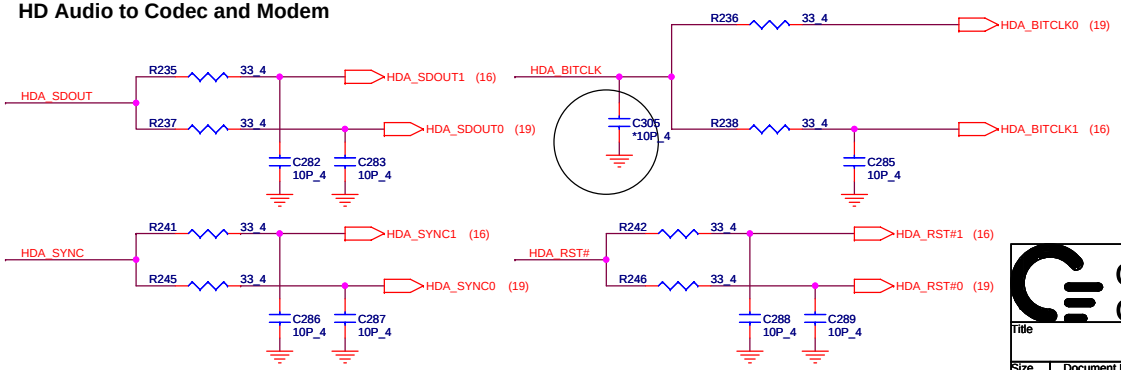
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)



ICH_INTVRMEN	Low = Disable High = Enable(Default)

ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05,VccSus1_5 and VccCL1_5)

HD Audio to Codec and Modem



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

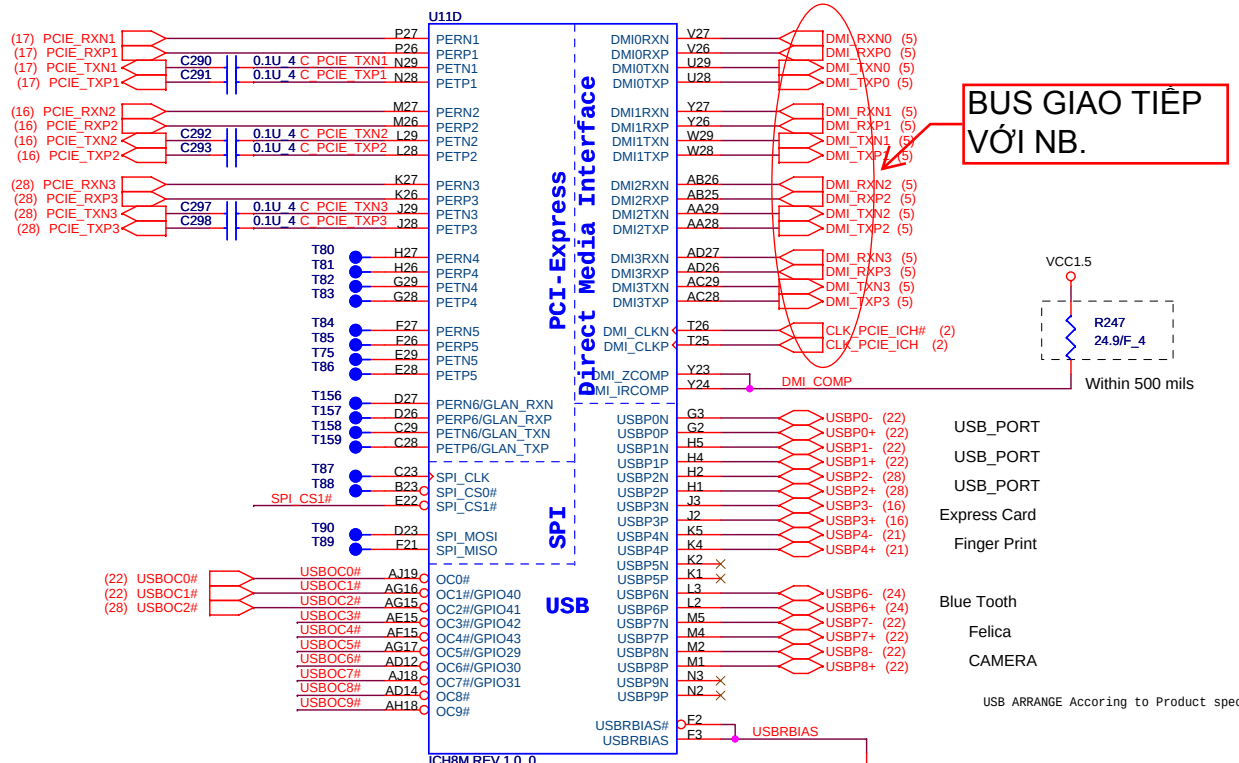
QUANTA COMPUTER

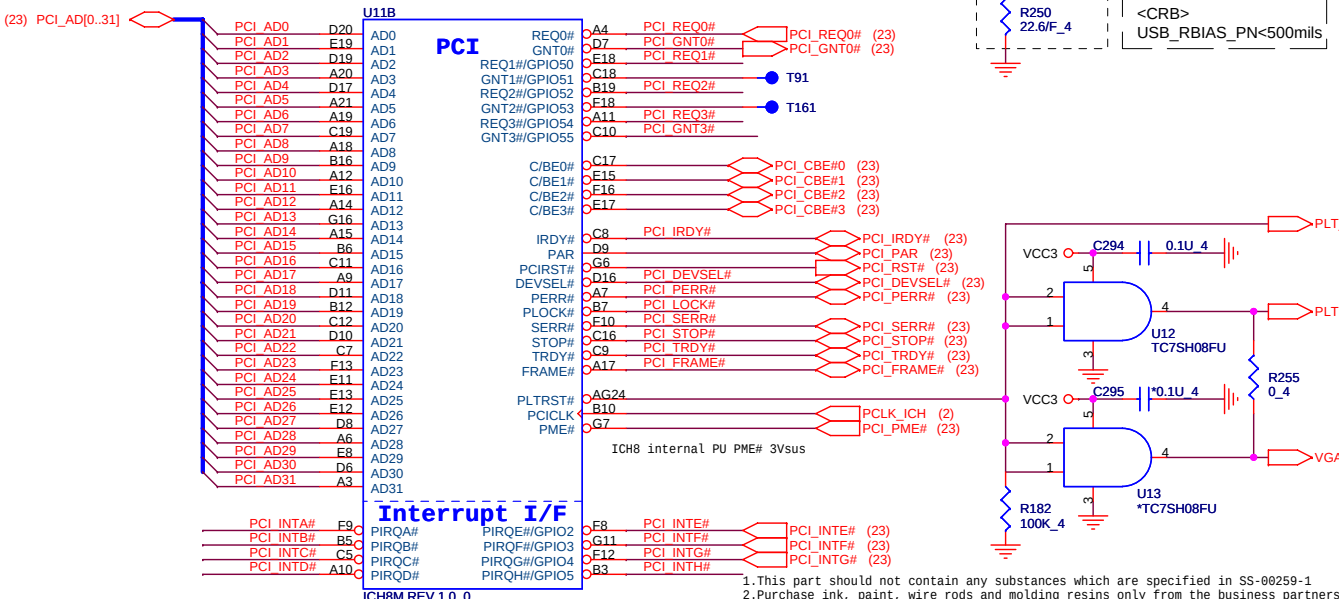
Title	ICH8-M HOST 1 of 4	
Size	Document Number: GD1 Main Board	Rev: 1A
Date: Tuesday, November 14, 2006	Sheet 12 of 35	

WireLess Lan

Express card

10/100 Lan





PCI bus info.

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
TI8402	AD23	REQ0# / GNT0#	PIRQ E/F/G

A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default

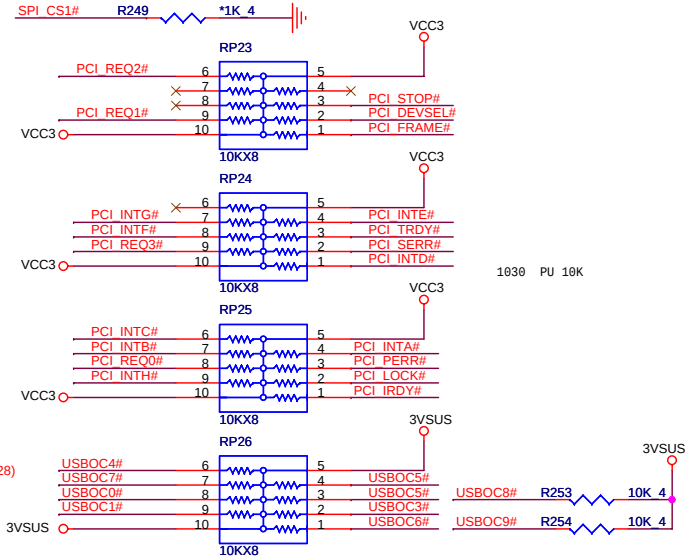
PCI_GNT3# R248 *1K_4

ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

PCI_GNT0# R251 *1K_4

SPI_CS1# R249 *1K_4



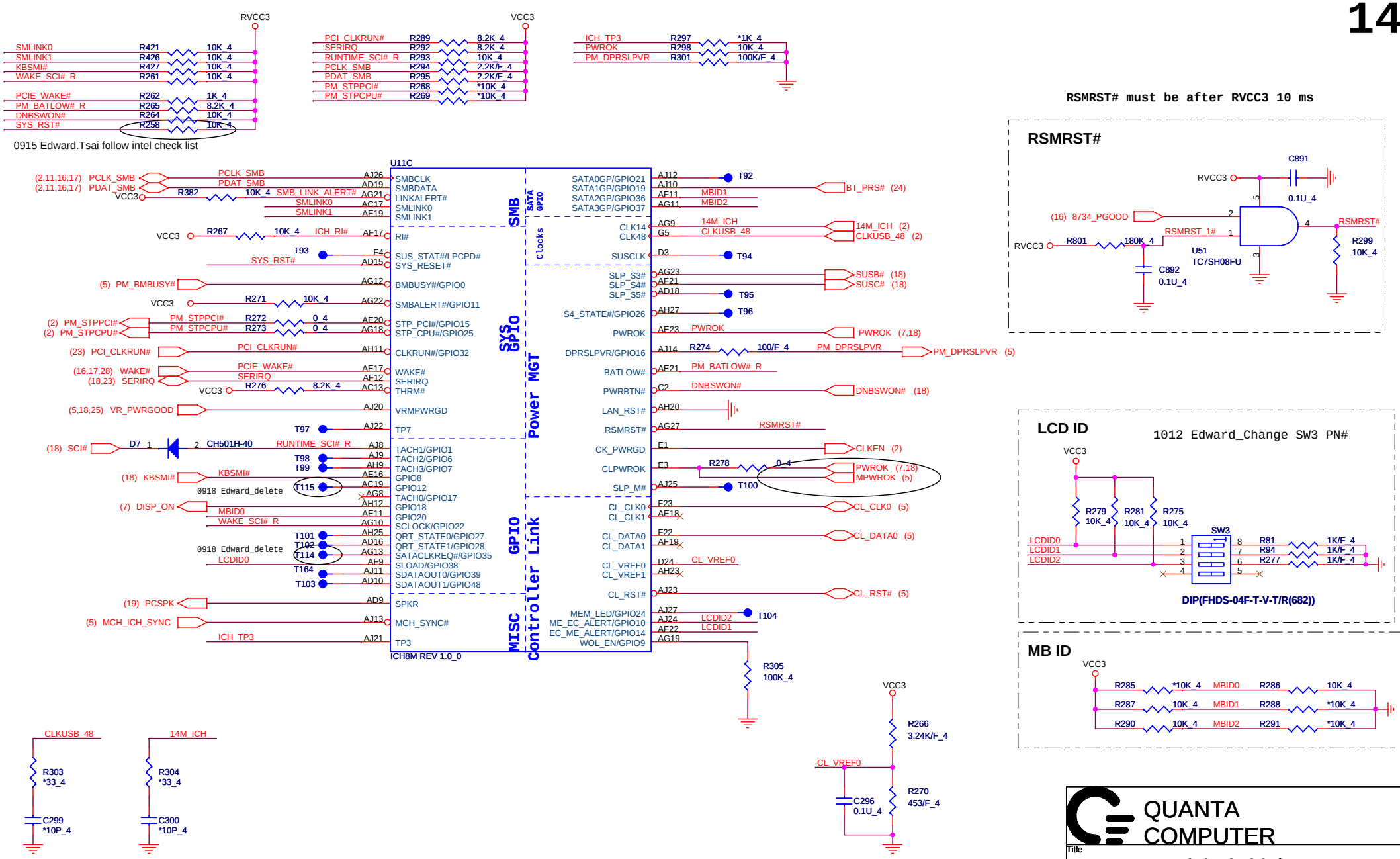
1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	ICH8-M PCIE 2 of 4	
Size B	Document Number GD1 Main Board	Rev 1A
Date: Tuesday, November 14, 2006	Sheet 13 of 35	

RSMRST# must be after RVCC3 10 ms

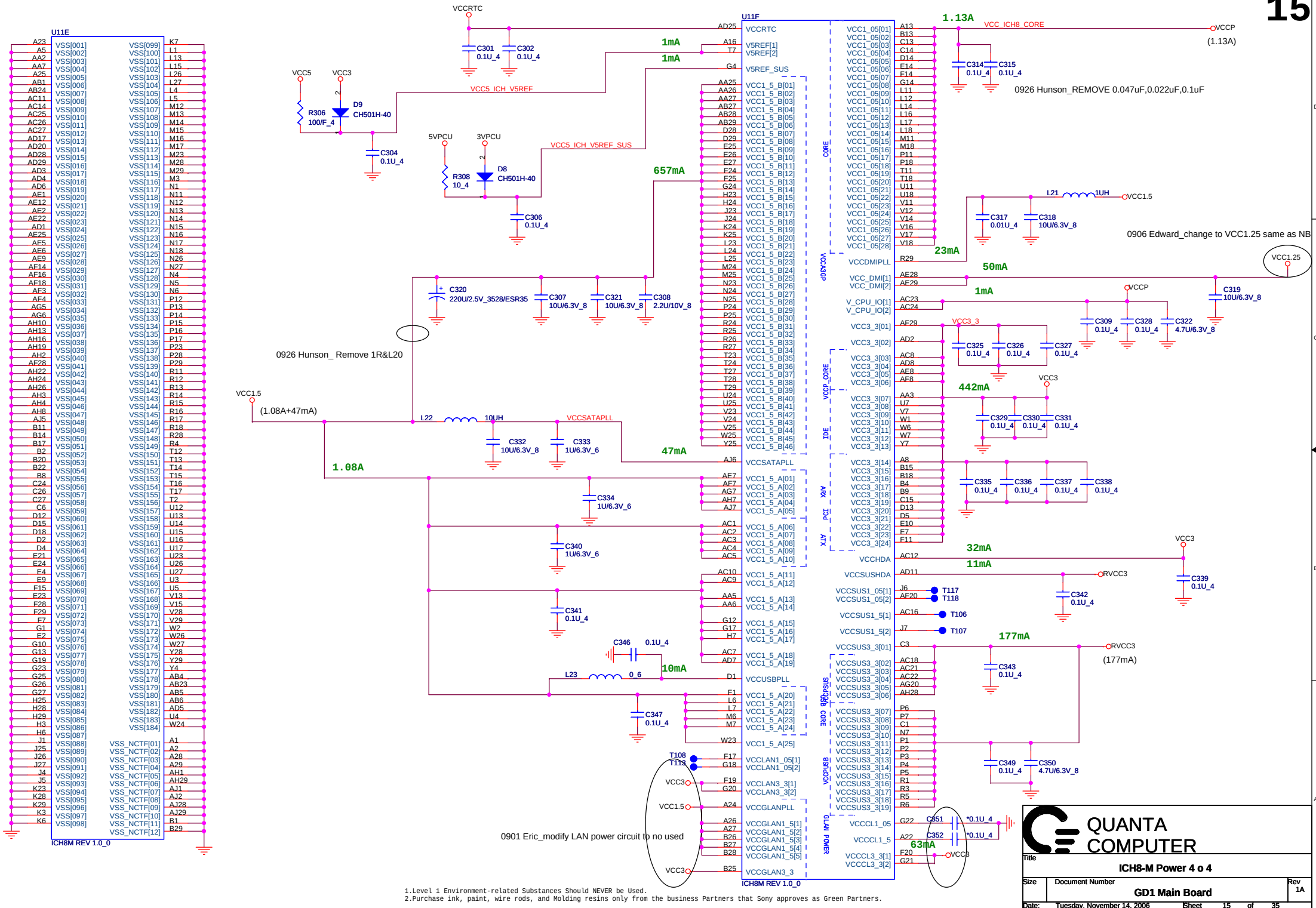
0915 Edward.Tsai follow intel check list



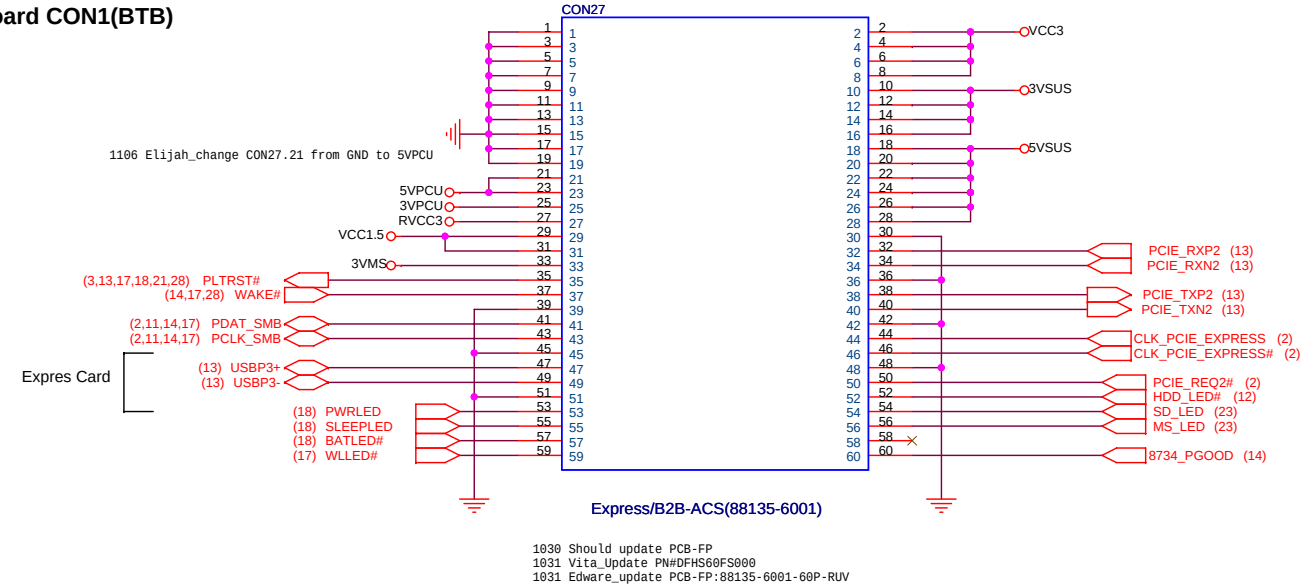
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	ICH8-M GPIO 3 of 4	
Size B	Document Number GD1 Main Board	Rev 1A
Date: Wednesday, November 15, 2006	Sheet 14 of 35	

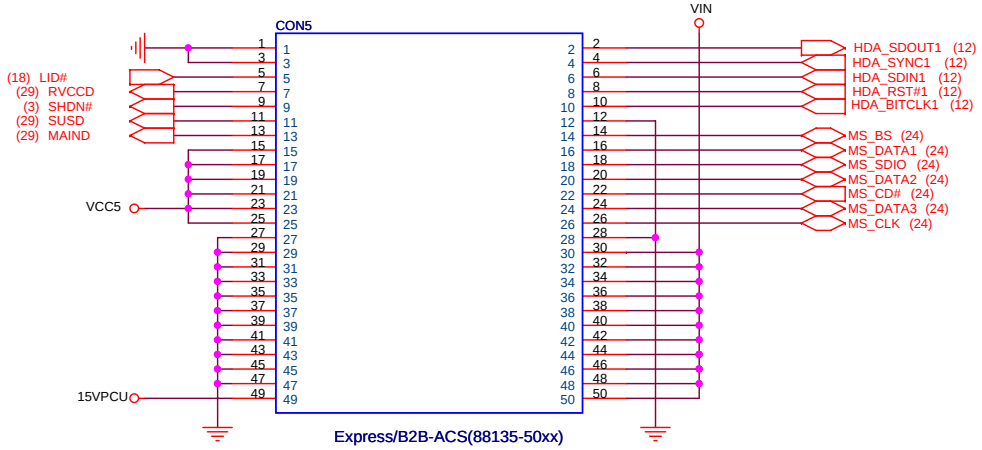

U11E
ICH8M REV 1.0_0
U11F
ICH8M REV 1.0_0
VCCRTC
C301 0.1U_4
C302 0.1U_4
1mA
1mA
VCC5
VCC3
VCC5_ICH_V5REF
R306 100/F_4
D9 CH501H-40
C304 0.1U_4
5VPCU
3VPCU
VCC5_ICH_V5REF_SUS
R308 10_4
D8 CH501H-40
C306 0.1U_4
657mA
C320 220U/2.5V_3528/ESR35
C307 10U/6.3V_8
C321 10U/6.3V_8
C308 2.2U/10V_8
0926 Hunson_ Remove 1R&L20
VCC1.5
(1.08A+47mA)
L22 10UH
VCCSATAPLL
C332 10U/6.3V_8
C333 1U/6.3V_6
47mA
1.08A
C334 1U/6.3V_6
C340 1U/6.3V_6
C341 0.1U_4
C346 0.1U_4
10mA
L23 0_6
C347 0.1U_4
T108
T119
VCC3
VCC1.5
0901 Eric_modify LAN power circuit to no used
1.13A
VCC_ICH8_CORE
VCCP
(1.13A)
C314 0.1U_4
C315 0.1U_4
0926 Hunson_REMOVE 0.047uF,0.022uF,0.1uF
L21 1UH
VCC1.5
C317 0.01U_4
C318 10U/6.3V_8
0906 Edward_change to VCC1.25 same as NB
23mA
VCC1.25
50mA
1mA
VCCP
C319 10U/6.3V_8
C309 0.1U_4
C328 0.1U_4
C322 4.7U/6.3V_8
VCC3_3
C325 0.1U_4
C326 0.1U_4
C327 0.1U_4
442mA
VCC3
C329 0.1U_4
C330 0.1U_4
C331 0.1U_4
C335 0.1U_4
C336 0.1U_4
C337 0.1U_4
C338 0.1U_4
32mA
11mA
VCC3
C339 0.1U_4
RVCC3
C342 0.1U_4
T117
T118
T106
T107
177mA
RVCC3
(177mA)
C343 0.1U_4
C349 0.1U_4
C350 4.7U/6.3V_8
C351 *0.1U_4
C352 *0.1U_4
63mA
VCC3
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.
QUANTA COMPUTER
Title
ICH8-M Power 4 o 4
Size
Document Number
GD1 Main Board
Rev
1A
Date: Tuesday, November 14, 2006
Sheet 15 of 35

Express Board CON1(BTB)

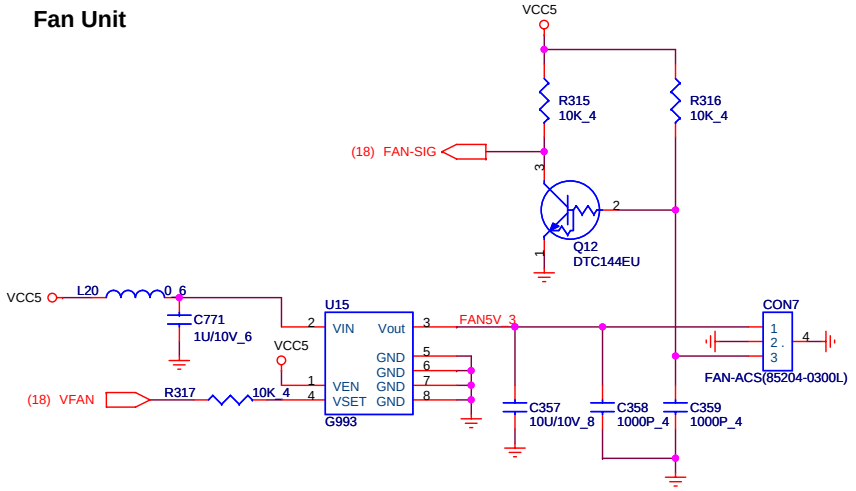


1030 Should update PCB-FP
1031 Vita_Update PN#DFHS60FS000
1031 Edware_update PCB-FP:88135-6001-60P-RUV

Express Board CON2(BTB)



Fan Unit



1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: Express Card		
Size: B	Document Number: GD1 Main Board	Rev: 1A
Date: Tuesday, November 14, 2006	Sheet 16 of 35	

LED_GP :LED WLEN LINK
Output Current : 7mA
Blink rate : 1 flash per every 3 sec.

WLSW:
Low : disable the radio.
High : Enable the radio.

LED_WLAN# MAX sink current=16mA
(recommend<=14mA)
Drive in LED/B
+3.3V:1A
+1.5V:500mA
+3.3Vaux:5mA

Mini PCI-E Card FOR WL

CON8

51	Reserved	+3.3V	52
49	Reserved	GND	50
47	Reserved	+1.5V	48
45	Reserved	NC	46
43	GND	LED_WLAN#	44
41	Reserved	NC	42
39	Reserved	GND	40
37	GND	Reserved	38
35	GND	Reserved	36
33	PERp0	GND	34
31	PERn0	Reserved	32
29	GND	Reserved	30
27	GND	+1.5V	28
25	PETp0	GND	26
23	PETno	+3.3Vaux	24
21	GND	PERST#	22
19	Reserved	W_DISABLE#	20
17	Reserved	GND	18
	Mini-PCIE Socket		
15	GND	LPC_AD1	16
13	REFCLK+	LPC_AD0	14
11	REFCLK-	LPC_AD3	12
9	GND	LPC_AD2	10
7	CLKREQ#	LPC_FRAME#	8
5	BT_CHCLK	+1.5V	6
3	BT_DATA	GND	4
1	WAKE#	+3.3V	2

MiniPCIE-JAE(MM60-52B1-B1-R600)

VCC3 VCC1.5 3VSUS

(13) PCIE_TXP1
(13) PCIE_TXN1
(13) PCIE_RXP1
(13) PCIE_RXN1
(2) PCLK_Debug
(2) CLK_PCIE_MINI
(2) CLK_PCIE_MINI#
(2) PCIE_REQ3#
(24) CH_CLK_INTEL
(24) CH_DATA_INTEL
(14,16,28) WAKE#
WAKE#

LED_WLAN# T109

PDAT_SMB (2,11,14,16)
PCLK_SMB (2,11,14,16)

PLTRST# (3,13,16,18,21,28)

WLAN_RF_ON WLAN_RF_ON (18)

W_DISABLE# Vil=0.3V

LPC_AD1 (12,18)
LPC_AD0 (12,18)
LPC_AD3 (12,18)
LPC_AD2 (12,18)
LPC_FRAME# (12,18)

VCC1.5
VCC3

Q34
CH2507SPT

WLLED# (16)
WLAN_RF_ON
WLAN_RF_ON (18)

1031 Hunson_Must ADD NMOS,R LED in Express/B

3VSUS
C360 0.1U_4
C361 1U/6.3V_6

VCC3
C362 0.1U_4
C363 10U/6.3V_8
C367 10U/6.3V_8

VCC1.5
C364 0.01U_4
C365 0.1U_4
C366 10U/6.3V_8

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: MINIPCIE / MDC

Size	Document Number	Rev
B	GD1 Main Board	1A

Date: Wednesday, November 15, 2006 Sheet 17 of 35

giao tiếp với SB

lệnh reset từ SB

giao tiep rom bios

matrix 8 X 16 (kb)

lên vỉ đk trên mặt máy.

osc 32,768hz.

PWR TU CAC KHOI NGUON +TU NGUON CPU BAO VE.

SPI Flash

1012 Hunson_ADD PU R302_4.7K
1016 Hunson Change BIOS to W25X80VSSIG

TP PS2

Reserved fot SPI FLASH

close by WPC8763

1016 Hunson_Add D10 to prevent leakage to S.B.

1016 Hunson_Add R142 PU

GPIO30-33 can sink 20mA current

1011 Hunson Add Batt RST

1011 Hunson Add Batt SCK&SDA

0930 Hunson REMOVE Reserved 0R

1109 Hunson_Remove NET "CAMERA_LED"

1102 Hunson_ADD CAMERA_EN

0901 Hunson_volmute is low active

0831 Eric_BT_PEN change to high active

1016 Hunson_Add PD 10K to SHM(confirm with Alan)

1107 Hunson_FAE recommend PD 10K on EVT version

1016 Hunson_Change EC to WPC8763L

DOCK_RST# : BADDR0
DK_BAY_PWEN: BADDR1

BT_PEN# : SHBM(If = 0 Enable share host BIOS memory)

PWROK must be after HWPG at least 10ms
VRON must be after PGOOD at least 99ms

MAINON <-- 3ms --> MAION1
MAINON <-- 3.5ms --> MAION2

I/O Address

BADDR1:0	Index	Data
1 0	2E	2F
1 1	4E	4F
0 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
0 1	XOR-TREE TEST	

JTAG SELECT CONFIGURATION

JEN0(PIN24)	JENK(PIN53)	Functionality of PINs (17,20,21,23,25,27)	Functionality of PINs (47,48,50,51,52)
NC	NC	GPIO	KEYBOARD OUTPUT
10K PD	NC	JTAG Signal	KEYBOARD OUTPUT
NC	10K PD	GPIO	JTAG Signal
10K PD	10K PD	Illegal Strap combination	

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	WPC8763L & SPI FLASH	
Size	Document Number: GD1 Main Board	Rev 1A
Date: Tuesday, November 14, 2006	Sheet 18 of 35	

Audio decoupling

EG31 1 2 40mil
R353 *0_4
R354 *0_4
AGND

1101 FAE comment

+5VA
C820 12P_4
C382 0.1U_4
C383 10U/10V_8
R338 20K/F_4
AGND
R544 10K_4
(20) EAPD
R350 0_4
R351 *0_4
HPOUT_R (20)
HPOUT_L (20)
C815 12P_4
C816 12P_4

U20
ALC262
ALC262-VC2-GR

VCC3
C386 0.1U_4
C387 10U/6.3V_8

Low enable speaker
(20) SPKR_EN#
R681 0_4
(20) HP_EN
R682 0_4
High enable HP

(12) HDA_BITCLK0
R16 *22_4
0928 EMI
C284 *10P_4
(12) HDA_SDOUT0
(12) HDA_SDIN0
R342 33_4
(12) HDA_SYNC0
(12) HDA_RST#0
C392 0.1U_4

DVDD-CORE
GPIO2/DMIC-DATA
GPIO3
DVSS
SDATA-OUT
BCLK
DVSS
SDATA-IN
DVDD-IO
SYNC
RESET#
PCBEEP

LINE-OUT-R
LINE-OUT-L
SENSEB
DCVOL
MIC1-VREFO-R
LINE2-VREFO
MIC2-VREFO
LINE1-VREFO
MIC1-VREFO-L
VREF
AVSS1
AVDD1

LINE-OUT-R
LINE-OUT-L
C388 1U/10V_6
C389 1U/10V_6
LINEOUT_R (20)
LINEOUT_L (20)
C813 12P_4
C814 12P_4
R709 10K_4
MIC1-VERFO-R
C404 1U/6.3V_6
+5VA
Standby DePOP
AGND
T162
MIC1-VERFO-L
C403 1U/6.3V_6
C397 10U/6.3V_8
C394 10U/10V_8
C395 0.1U_4

VCC3
R802 10K_4
R345 15K_4
(14) PCSPK
Q52
DTC144EU
R344 1K/F_4
C399 *0.1U_4
1031 Hunson_Add Q52 as NBDC comment

1101 FAE comment

MIC-JD R346 20K/F_4
HP-JD R347 39.2K/F_4
SENSEA
R364 0_6
C401 1U/10V_6
MIC2_L
R365 0_6
C402 1U/10V_6
MIC2_R
C811 12P_4
C812 12P_4
C819 33P_4

Analog MIC Connector

MIC1-R
MIC1-L
C390 2.2U/10V_8
C393 2.2U/10V_8
AU3
AU4
R429 4.7K/F_6
R430 4.7K/F_6
EXTMICR
EXTMICL
C817 12P_4
C818 12P_4
C463 1000P_4
C502 1000P_4

MIC2_IN1
CON10
MIC-ACS(87213-0400G)
VCC5
EG2 20mil

1013 Hunson ADD Pre_AMP(MAX9812H) in MIC/B
1020 Hunson_Change 87213-0400

Audio/B CON(B2B)

CON26
EXTMICR
EXTMICL
MIC1-VERFO-L
MIC1-VERFO-R
(18) BTSW
HPR (20)
HPL (20)
MIC-JD#
HP-JD#
3VSUS

AUDIO/B ACS(88135-1601)

+5VA
R711 10K_4
MIC-JD
MIC-JD#
Q16
CH2507SPT

R712 10K_4
HP-JD
HP-JD#
Q17
CH2507SPT

1.Level 1 Environment-related Substances Should NEVER be Used.
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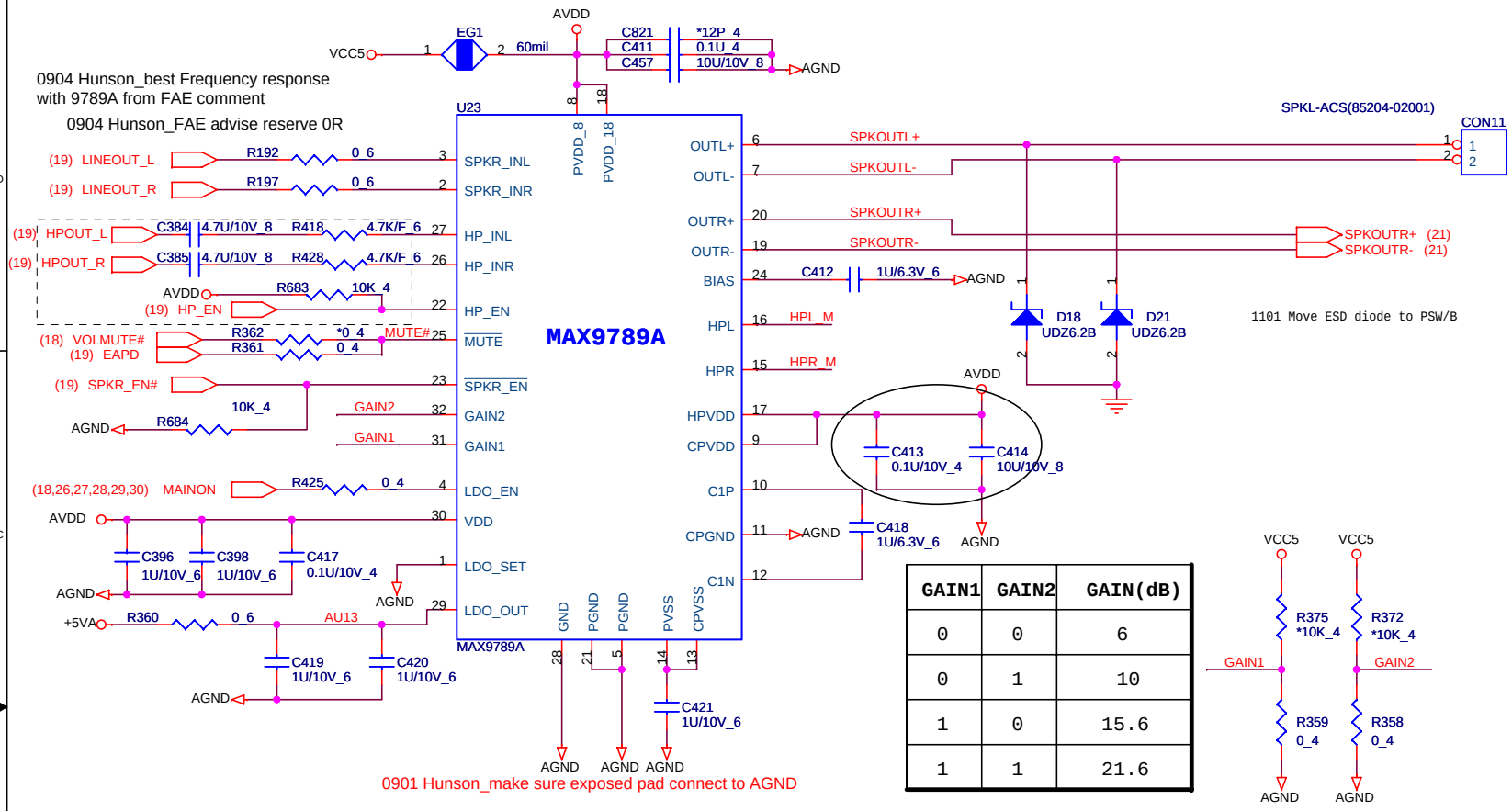
QUANTA COMPUTER

Title	Audio ALC268	
Size: Custom	Document Number: GD1 Main Board	Rev: 1A
Date: Tuesday, November 14, 2006	Sheet 19 of 35	

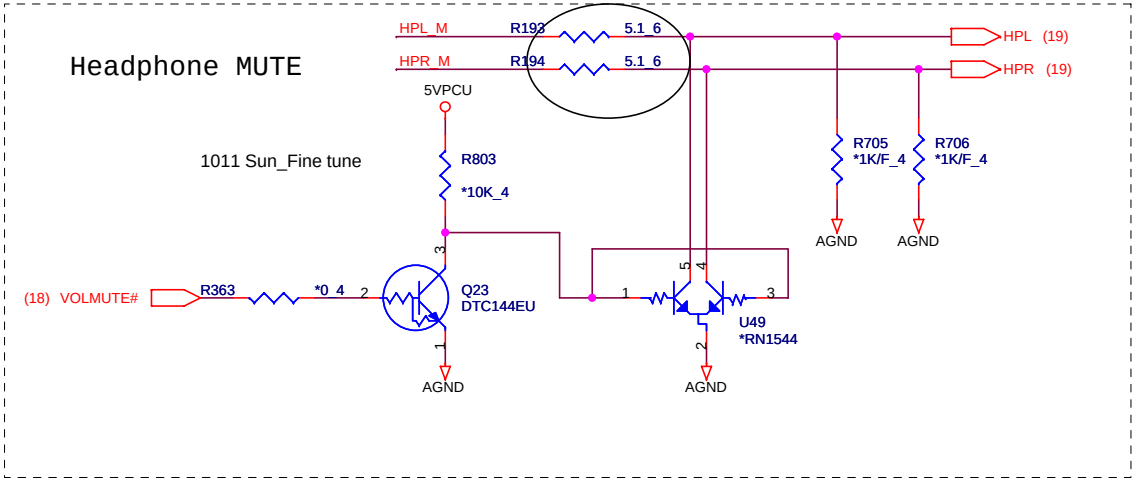
0904 Hunson_best Frequency response with 9789A from FAE comment

0904 Hunson_FAE advise reserve 0R



0901 Hunson_make sure exposed pad connect to AGND

GAIN1	GAIN2	GAIN(dB)
0	0	6
0	1	10
1	0	15.6
1	1	21.6



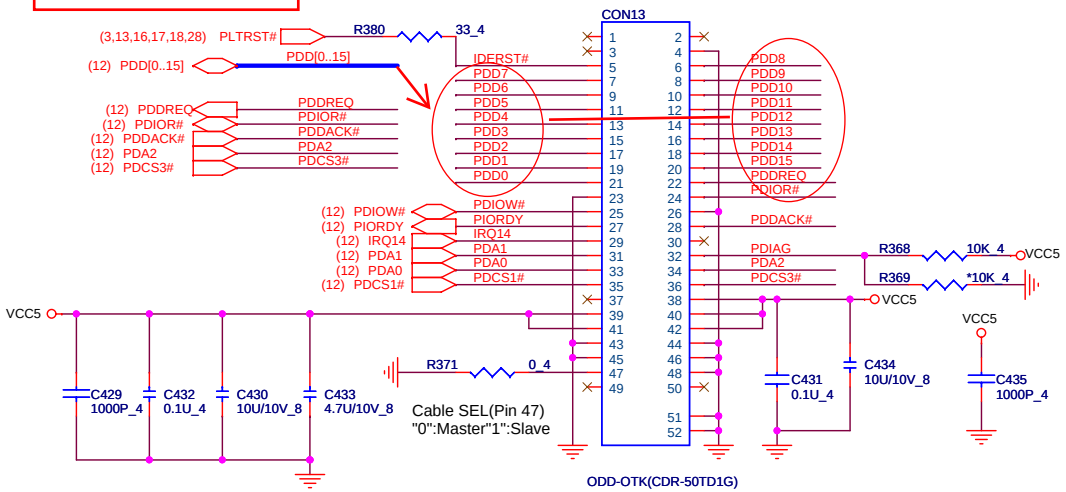
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

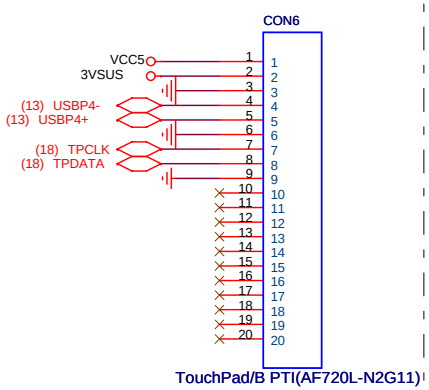
Title	Audio AMP. & Speaker	
Size: Custom	Document Number: GD1 Main Board	Rev: 1A
Date: Tuesday, November 14, 2006	Sheet 20 of 35	

ODD CONNECTOR

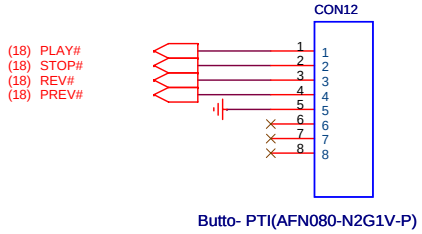
TƯƠNG TỰ NHƯ IDE NHƯNG TỐC ĐỘ TRUYỀN DỮ LIỆU CAO HƠN.



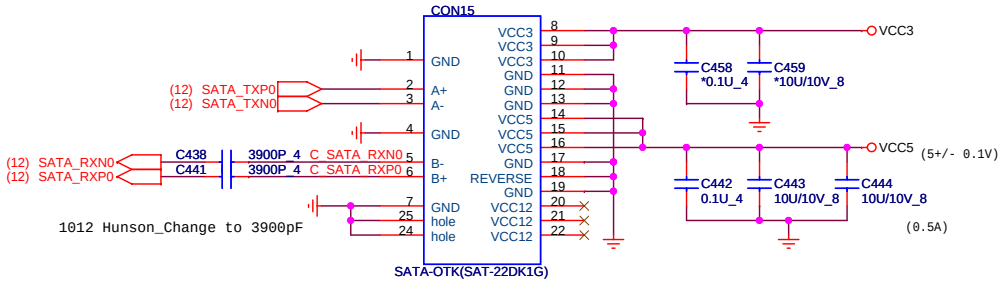
TouchPAD Board CON(FFC)



Button CON(FFC)



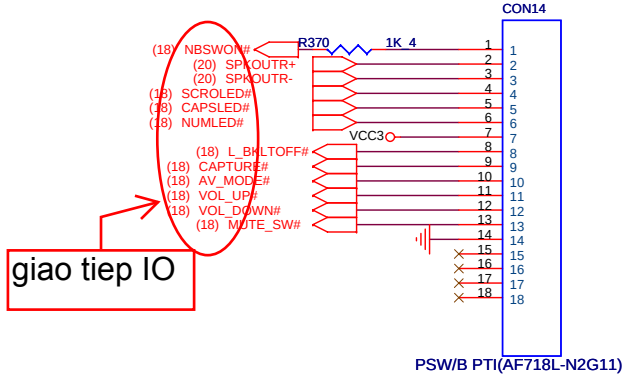
HDD CONNECTOR



1019 Hunson_Change to OTK(SAT-22DK1G)

PSW Board CON(FFC)

1031 Hunson_update PCB-FP



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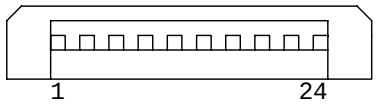
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: HDD/ODD/PW CON		
Size: B	Document Number: GD1 Main Board	Rev: 1A
Date: Wednesday, November 15, 2006	Sheet 21 of 35	

Keyboard



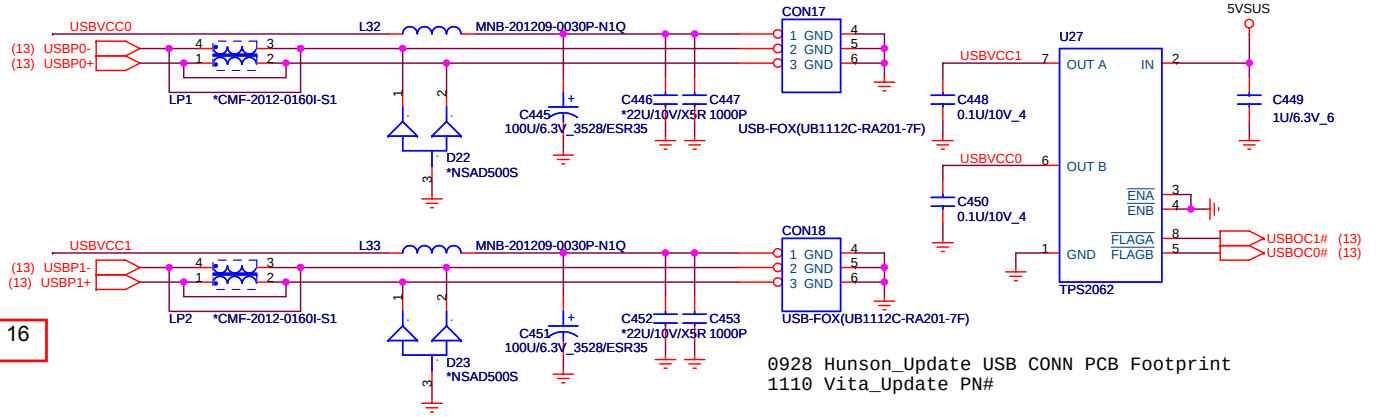
(18) MY12 — RP29 — MY12_R — MY1_R
(18) MY2 — MY0_R
(18) MY0 — MY2_R
(18) MY1 — MY12_R
(18) MY8 — RP30 — MY8_R — MY11_R
(18) MY9 — MY9_R — MY10_R
(18) MY10 — MY10_R — MY9_R
(18) MY11 — MY11_R — MY8_R
(18) MX6 — RP31 — MX6_R — MY7_R
(18) MX7 — MX7_R — MX5_R
(18) MX5 — MX5_R — MX7_R
(18) MY7 — MY7_R — MX6_R
(18) MX0 — RP32 — MX0_R — MX2_R
(18) MX1 — MX1_R — MX3_R
(18) MX3 — MX3_R — MX1_R
(18) MX2 — MX2_R — MX0_R
(18) MY13 — RP33 — MY13_R — MX4_R
(18) MY15 — MY15_R — MY5_R
(18) MY5 — MY5_R — MY15_R
(18) MX4 — MX4_R — MY13_R
(18) MY14 — RP34 — MY14_R — MY3_R
(18) MY6 — MY6_R — MY4_R
(18) MY4 — MY4_R — MY6_R
(18) MY3 — MY3_R — MY14_R

22X4

CON16 → KB-PTI(AFN240-N2G1V-P)

MATRIX 8 X 16

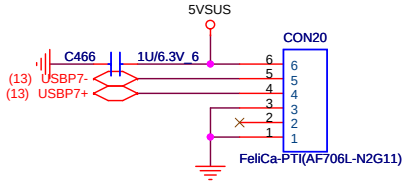
USB Port x 2



0928 Hunson_Update USB CONN PCB Footprint
1110 Vita_Update PN#

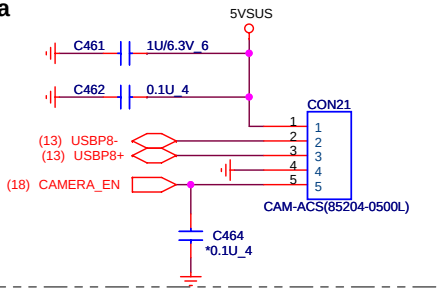
Felica

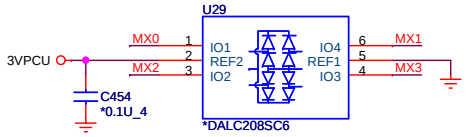
0929 Eric_
1.change material to gold plating
2.change Foot Print to PTI

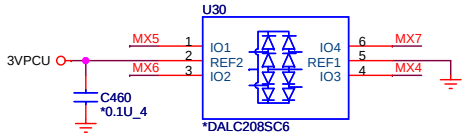


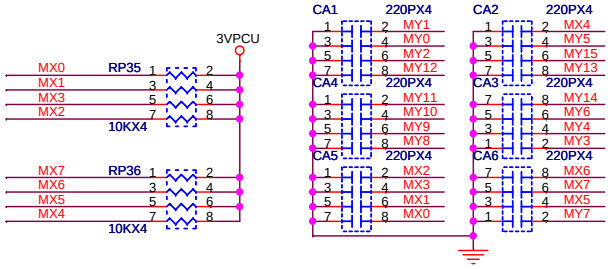
1012 Edward_Change CON20 PN#(gold-pating)

USB Camera

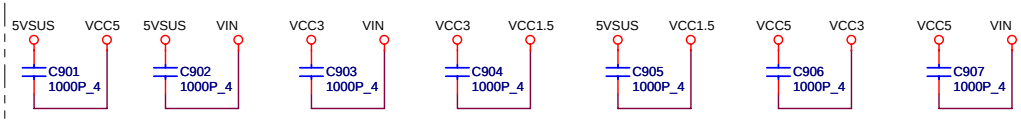




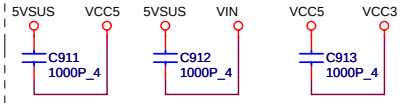




ODD



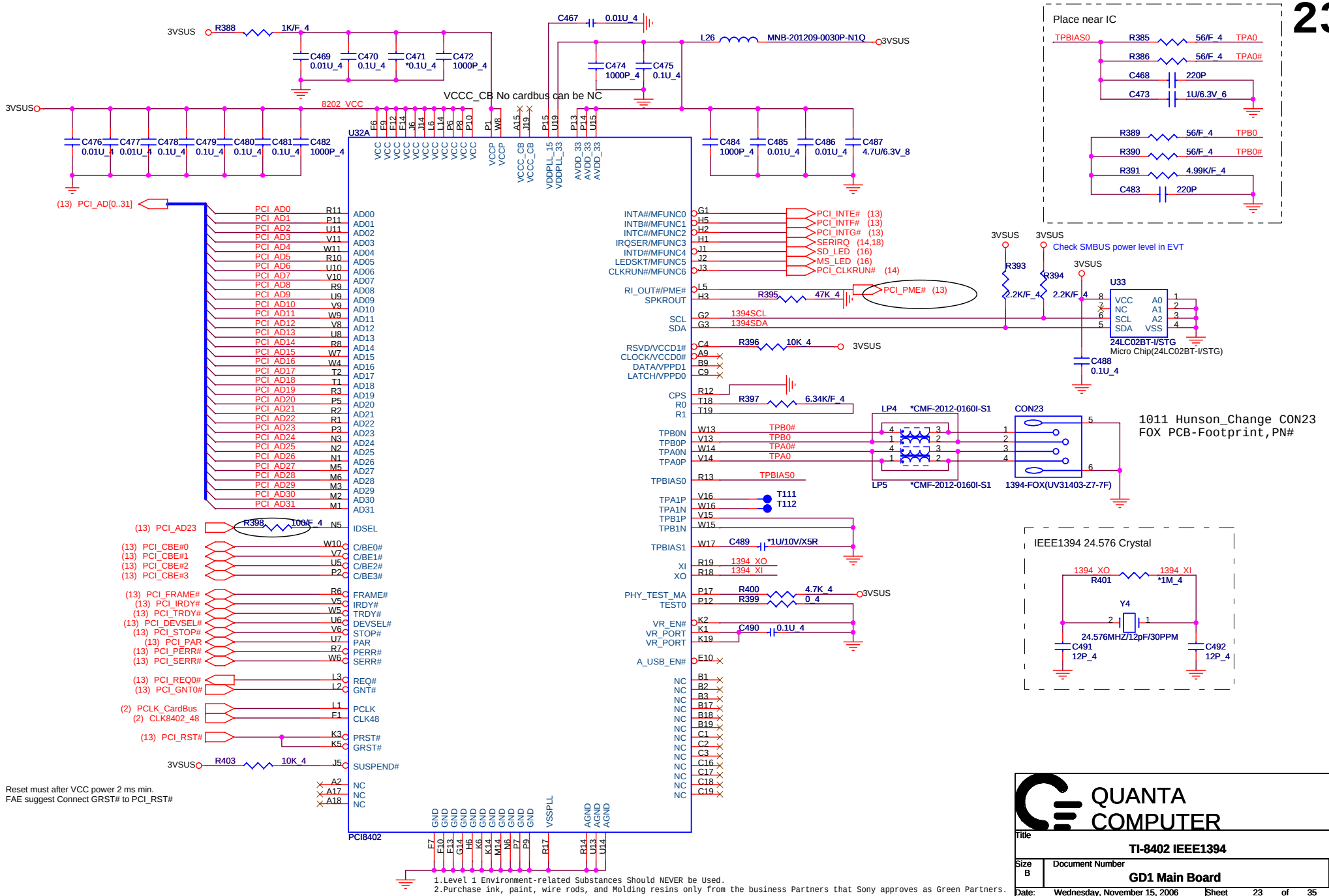
PCI BUS



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

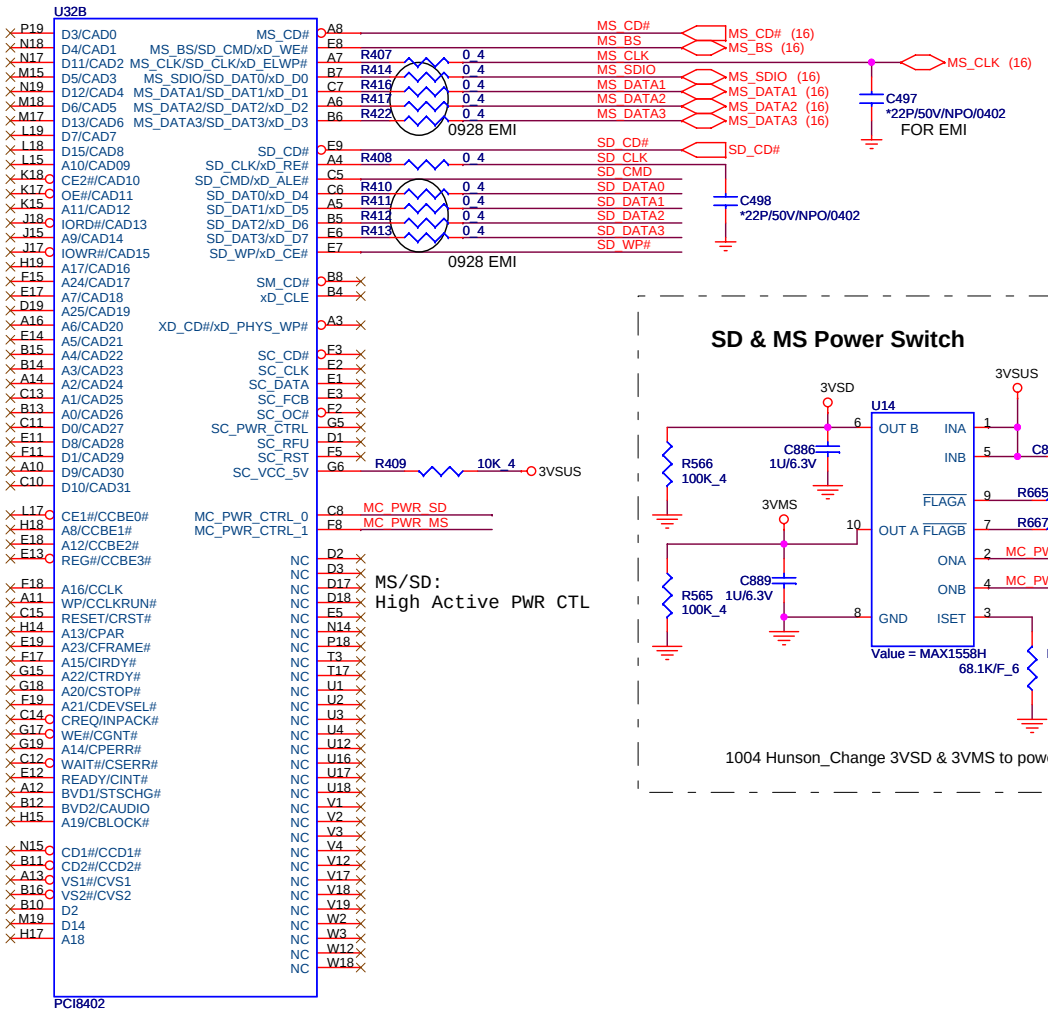
QUANTA COMPUTER

Title	K/B ,USB Device	
Size B	Document Number GD1 Main Board	Rev 1A
Date: Wednesday, November 15, 2006	Sheet 22 of 35	



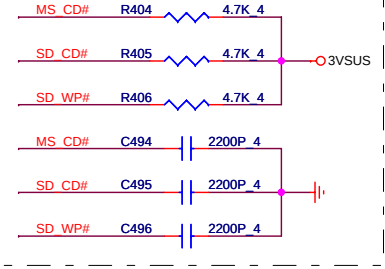
QUANTA COMPUTER

Title	TI-8402 IEEE1394	
Size B	Document Number GD1 Main Board	Rev 1A
Date: Wednesday, November 15, 2006	Sheet 23 of 35	

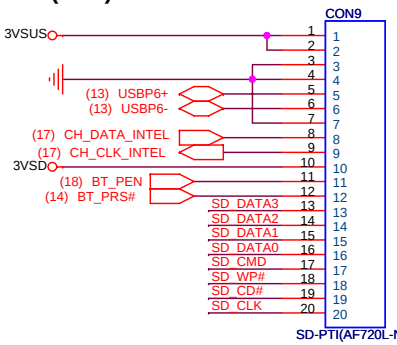


SD & MS Power Switch

1004 Hunson_Change 3VSD & 3VMS to power switch



SD CON(FPC)

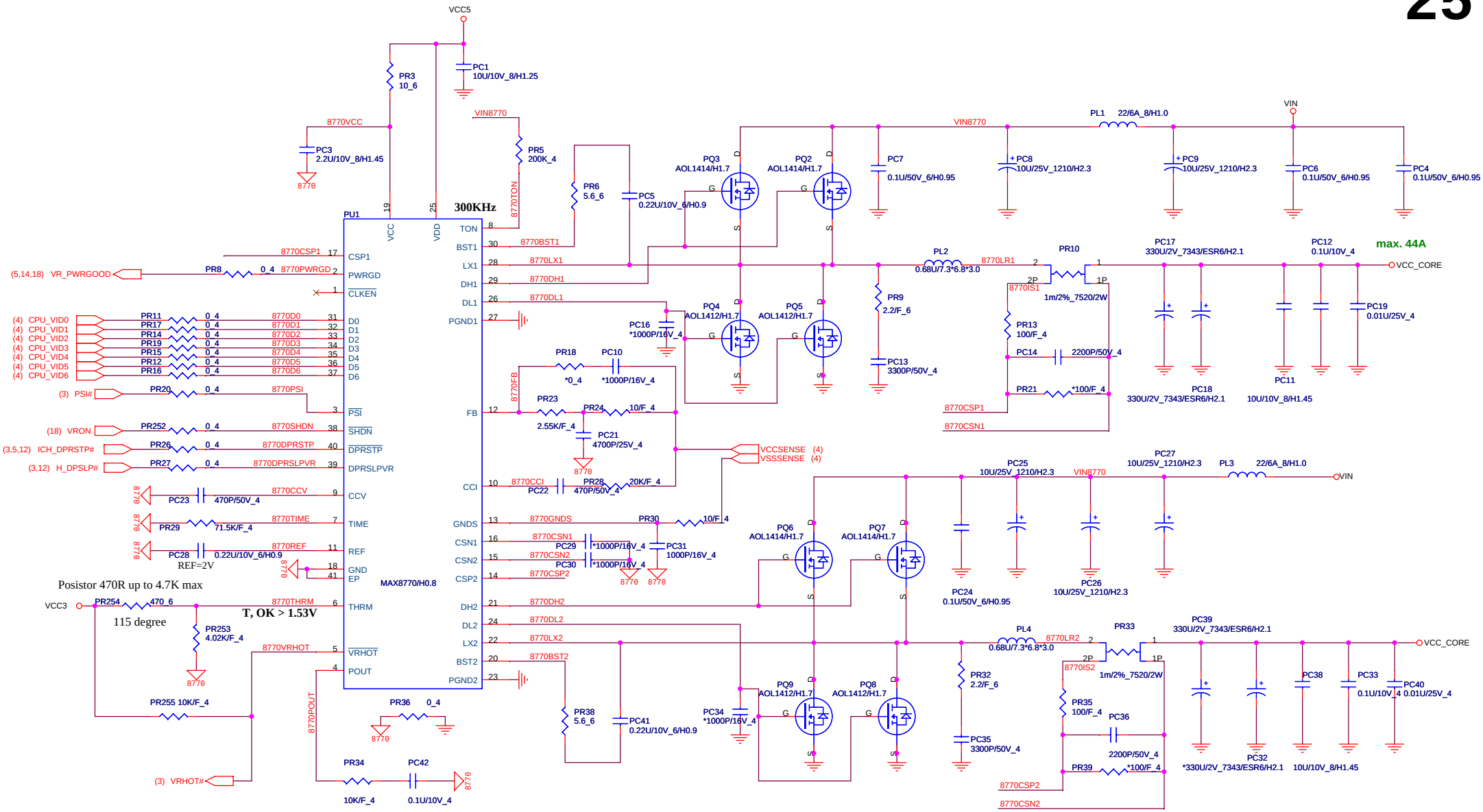


1031 Hunson_Change pin assignment
FAE comment:MS/SD_clock must have 3W space away DATA[0:3]

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	TI-8402 MS & SD	
Size B	Document Number GD1 Main Board	Rev 1A
Date: Wednesday, November 15, 2006	Sheet 24 of 35	



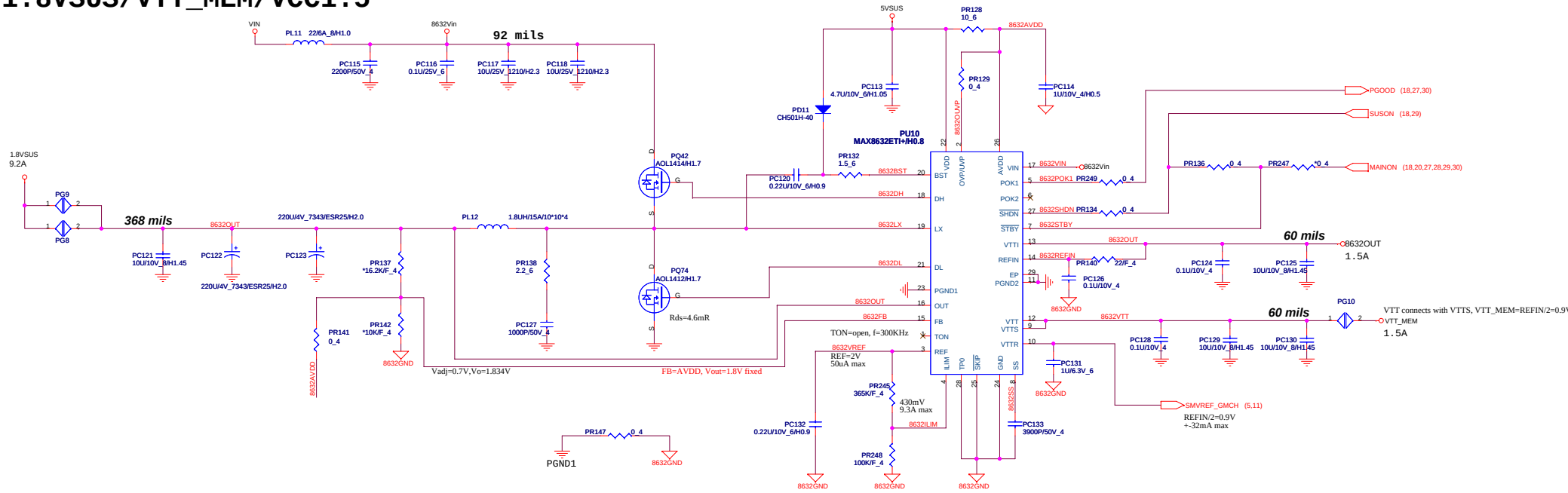
In progress

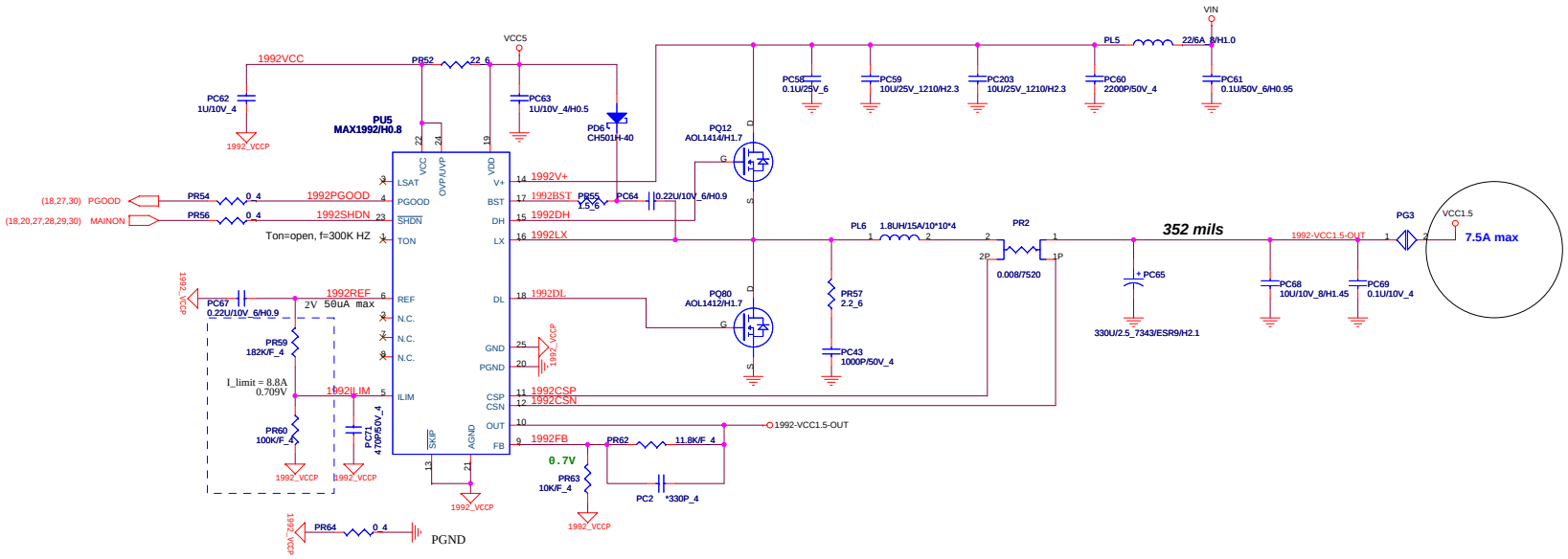
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	CPU CORE (MAX8770)	
Size: Custom	Document Number: RD3 Main Board	Rev: 1A
Date: Tuesday, November 14, 2006	Sheet 25 of 35	

1.8VSUS/VTT_MEM/VCC1.5



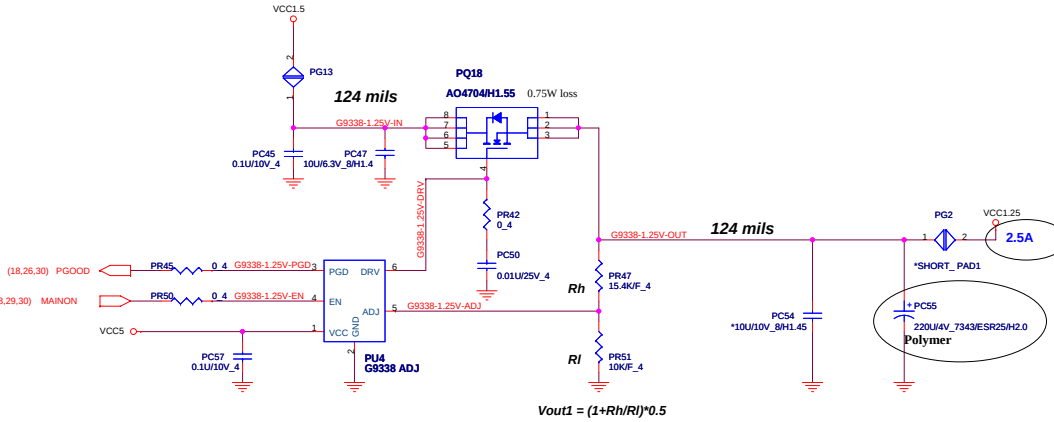


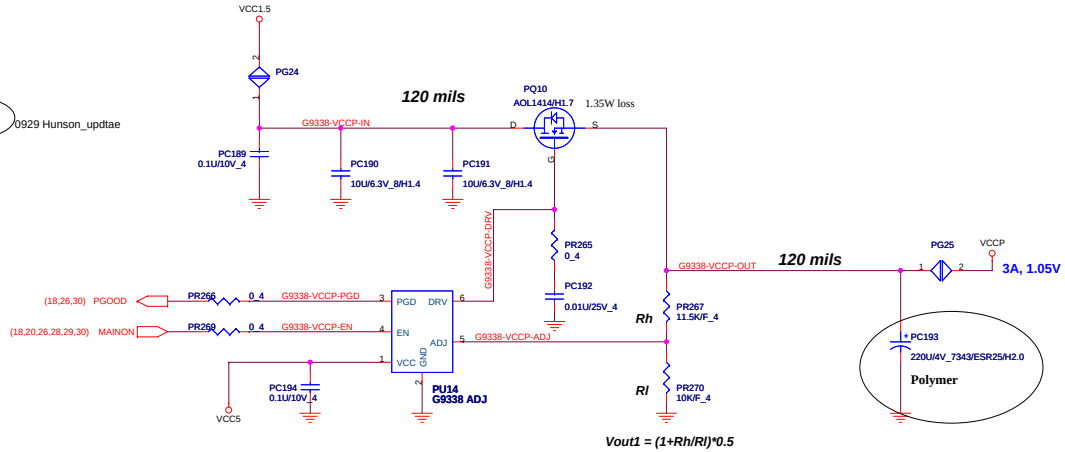
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

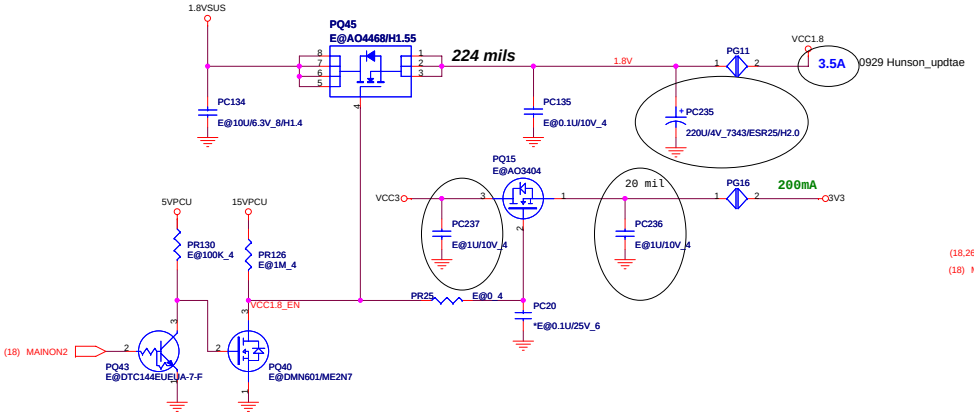
QUANTA COMPUTER

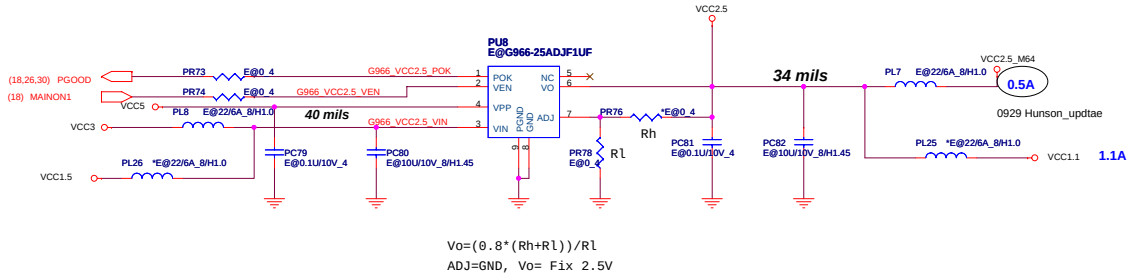
Title	VCCP & VCC1.5 & VCC1.25	
Size	Document Number: RD3 Main Board	Rev: 1A
Date: Tuesday, November 14, 2006	Sheet 26 of 35	

VCC2.5/VCC1.25/VCC1.8/VCCP









Vo=(0.8*(Rh+Rl))/Rl
ADJ=GND, Vo= Fix 2.5V

In progress

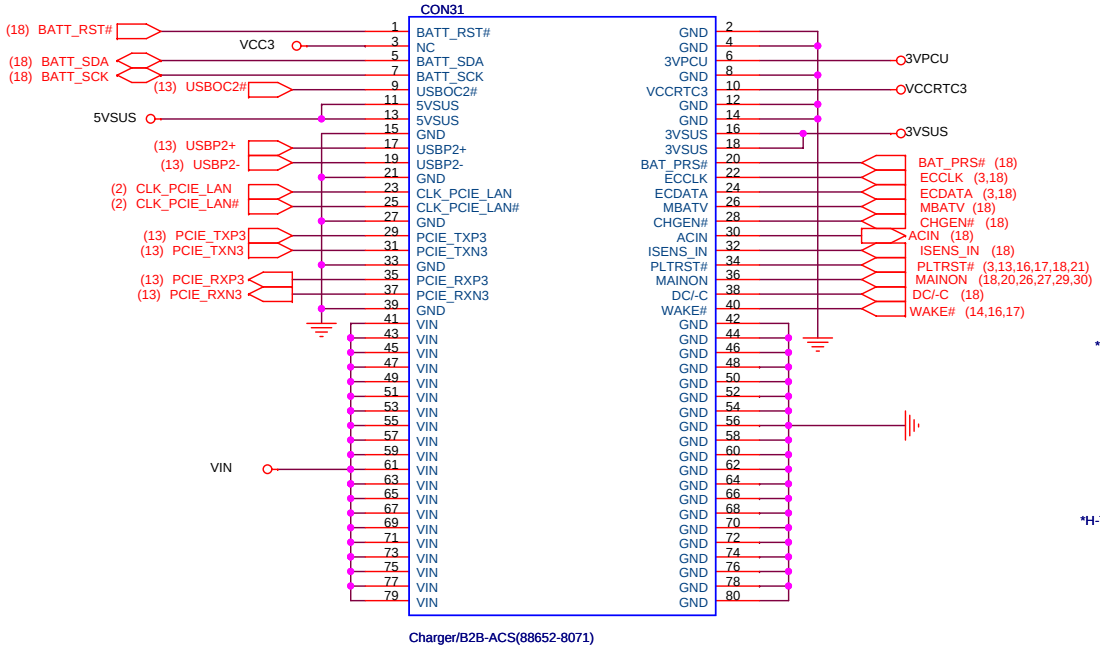
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

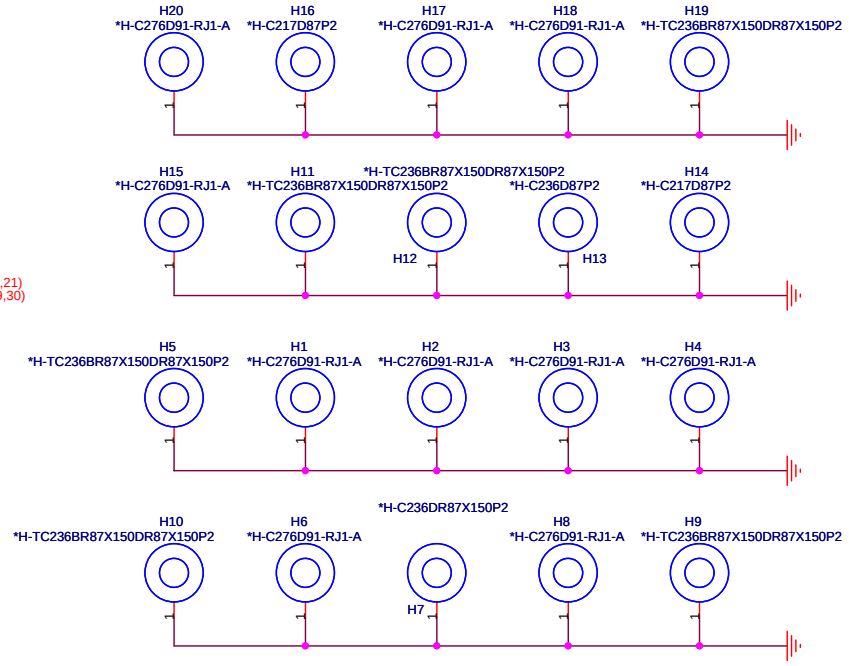
Title	VCCP & VCC1.5 & VCC1.25	
Size	Document Number: RD3 Main Board	Rev: 1A
Date: Tuesday, November 14, 2006	Sheet 27 of 35	

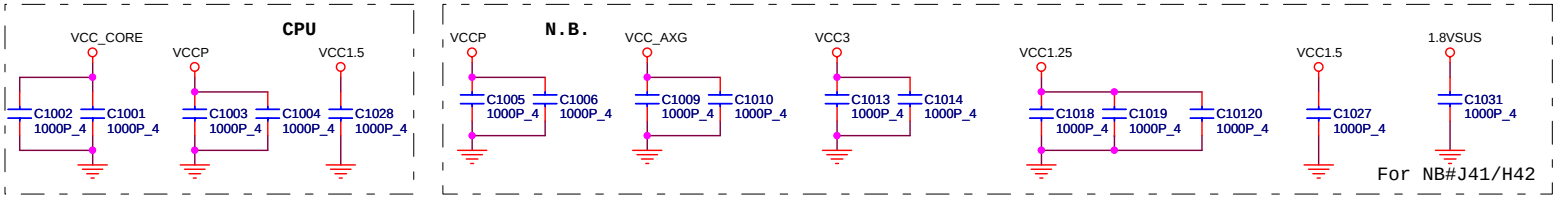
1027 Vita modify pin definition

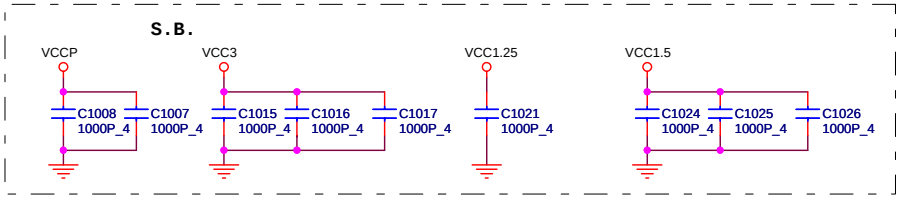
1106 Vita_ADD VCC3 on CON31.3

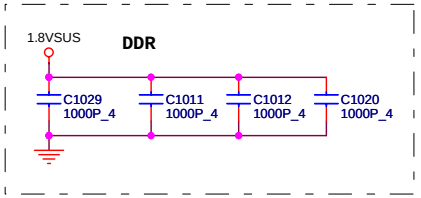


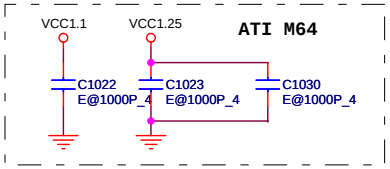
Charger/B2B-ACS(88652-8071)











1.Level 1 Environment-related Substances Should NEVER be Used.
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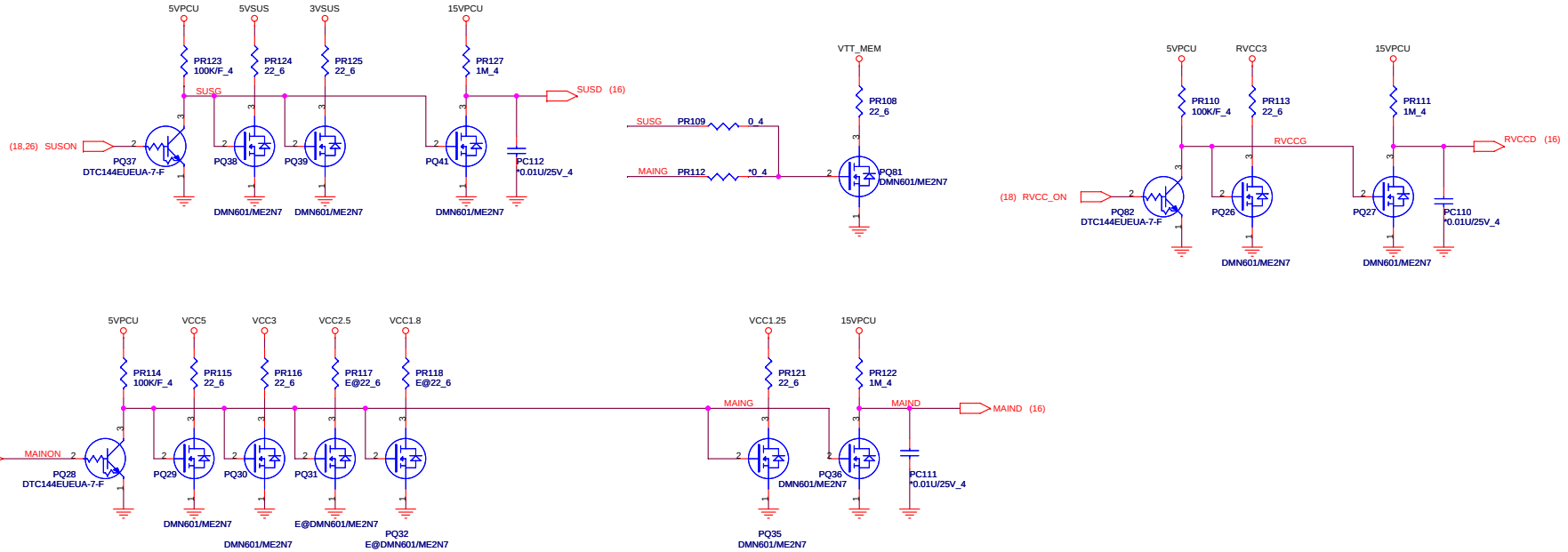
QUANTA COMPUTER

Title	Power Charger & LAN CON	
Size B	Document Number GD1 Main Board	Rev 1A
Date: Wednesday, November 15, 2006	Sheet 28 of 35	

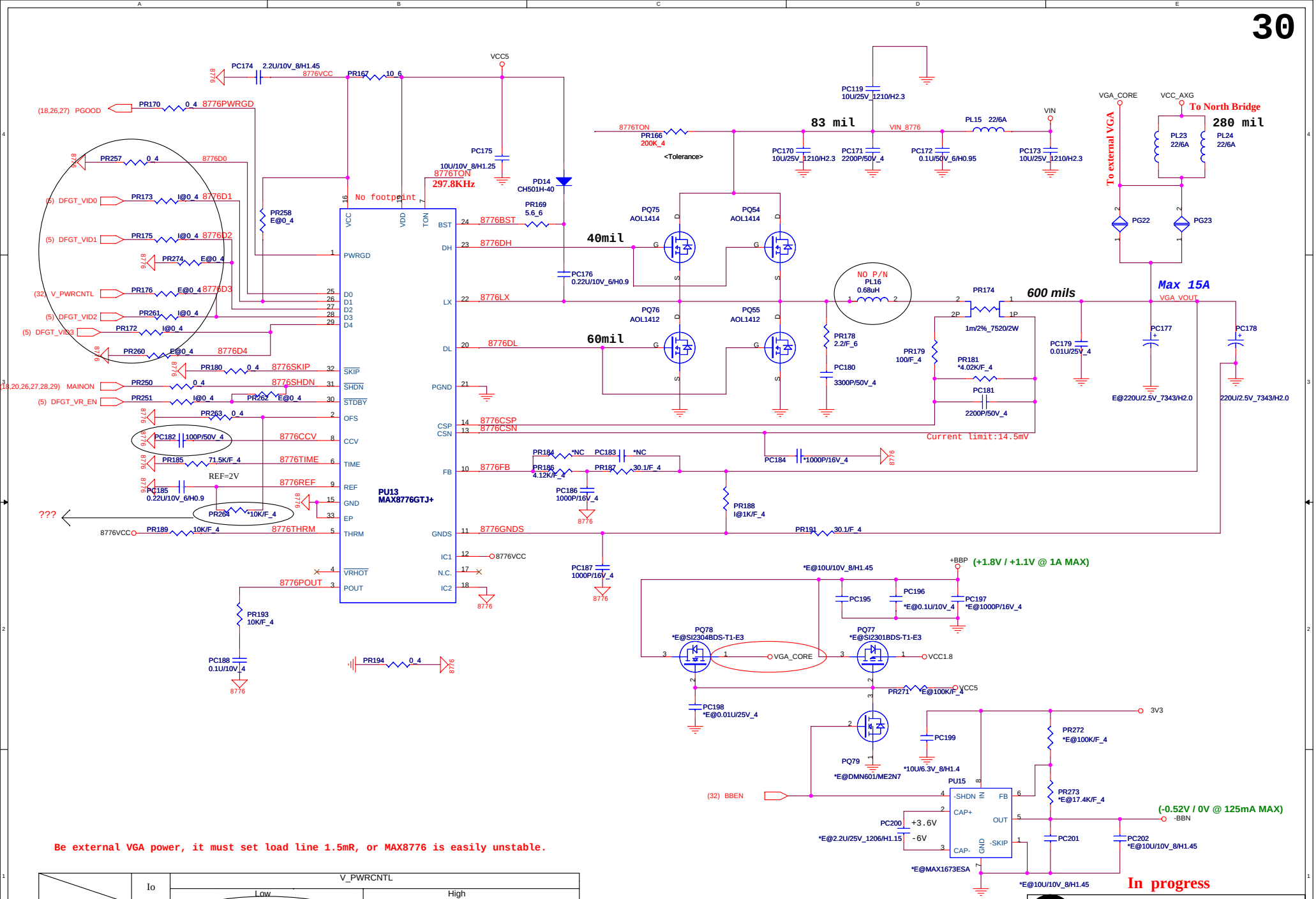


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

In progress

QUANTA COMPUTER

Title	3VPCU & 5VPCU	
Size: Custom	Document Number: RD3 Main Board	Rev: 1A
Date: Wednesday, November 15, 2006	Sheet 29 of 35	



Be external VGA power, it must set load line 1.5mR, or MAX8776 is easily unstable.

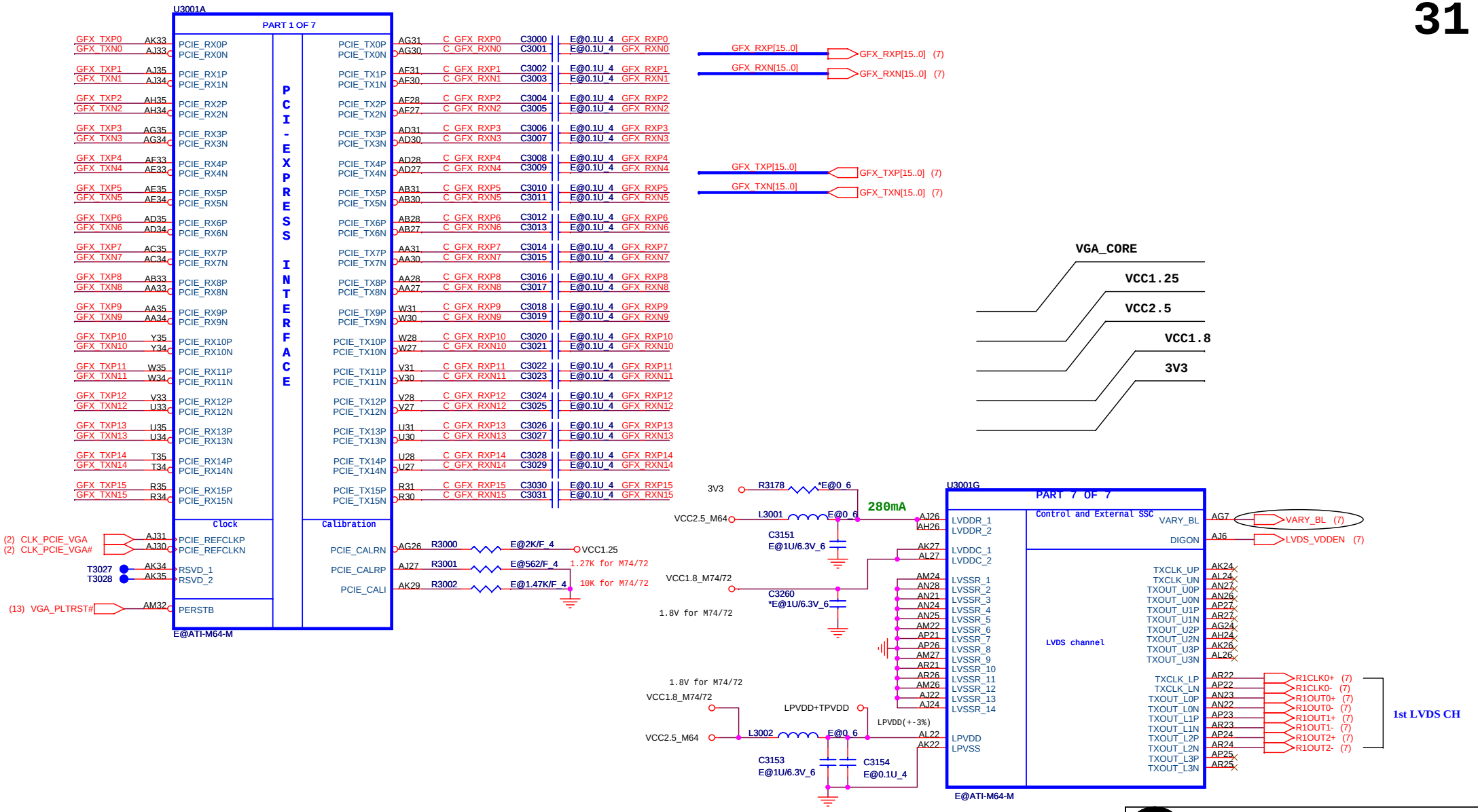
	Io	V_PWRCNTL	
		Low	High
Ext :ATI M71-M74	15A	1.2V (D4,D3,D2,D1,D0=0,0,0,1,0)	1.0V (D4,D3,D2,D1,D0=0,1,0,1,0)
Int :North Bridge	7.7A	VID	

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

In progress

QUANTA COMPUTER

Title	VGA CORE	
Size	Document Number: RD3 Main Board	Rev: 1A
Date: Tuesday, November 14, 2006	Sheet 30 of 35	



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	ATI M64M PCIE	
Size B	Document Number GD1 Main Board	Rev 1A
Date: Tuesday, November 14, 2006	Sheet 31 of 35	

M64 Thermal Sensor

U3000 E@G781-1

Mount 37.5R on R31[49-51] for M72/74 Near Connector Differential routing

NO USE PD 100K

M72/74 PD R3183

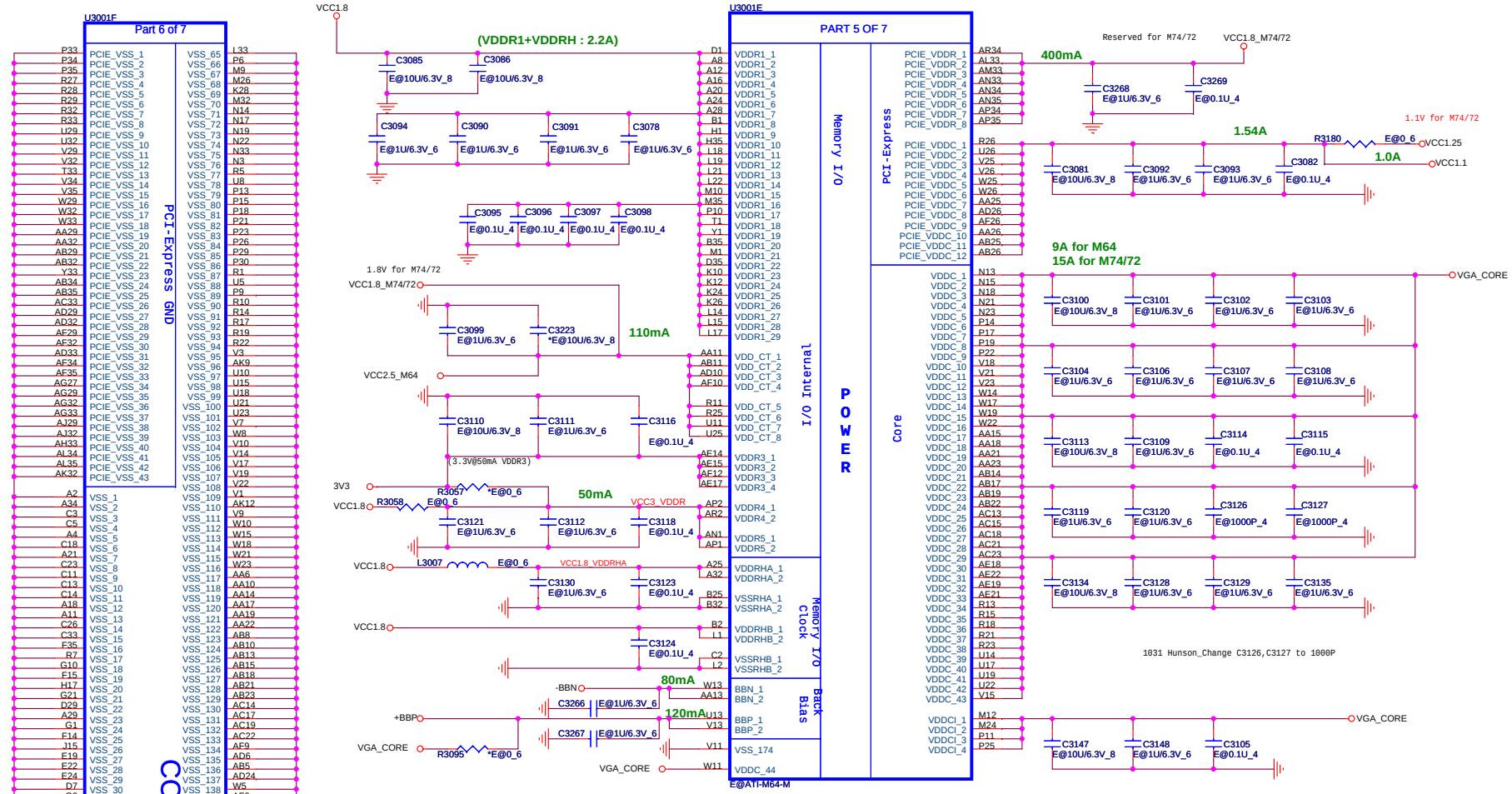
1107 Hunson_PU R3005,R3003 for M72/74

R3176,R3177 should close by CON29

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Title	ATI M71
Size / Document Number	Custom / GD1 Main Board
Rev	1A
Date:	Tuesday, November 14, 2006
Sheet	32 of 35

QUANTA COMPUTER



POWER Regulator	M64/M71	Rail	M72/M74	Rail
VDDC+VDDCI	1.0~1.2V	VGA_CORE	0.95~1.1V	VGA_CORE
PCIE_PVDD	1.25	VCC1.25	1.8	VCC1.8_M74/72
PCIE_VDDR	NC	x	1.8	VCC1.8_M74/72
PCIE_VDDC	1.25	VCC1.25	1.1	VCC1.1
MPVDD	VDDC	VGA_CORE	VDDC	VGA_CORE
DPLL_PVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
DPLL_VDDC	1.25	VCC1.25	1.1	VCC1.1
VDDR1+VDDRH	1.8	VCC1.8	1.8	VCC1.8
VDDR4+VDDR5	1.8	VCC1.8	1.8	VCC1.8
VDDR3	3.3	3V3	3.3	3V3
VDD_CT	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
LPVDD+TPVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
LVDDR	2.5	VCC2.5_M64	3.3	3V3_M74/72
LVDDC	NC	x	1.8	VCC1.8_M74/72
TXVDDR	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
AVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
VDD1DI+VDD2DI	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
A2VDD	2.5	VCC2.5_M64	3.3	3V3_M74/72
A2VDDQ	NC	x	1.8	VCC1.8_M74/72

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QUANTA COMPUTER

Title: ATI M64M POWER

Size: Custom | Document Number: GD1 Main Board | Rev: 1A

Date: Tuesday, November 14, 2006 | Sheet 33 of 35

Channel A

U3001C

Part 3 of 7

MEMORY INTERFACE A

E@ATI-M64-M

Use for DDR2 only, keep NC for others

For 8 Banks MAA_13=BA2

U3002

E@VRAM_256Mb

U3003

E@VRAM_256Mb

1031 Hunson_Change C3184,C3164,c3179,C3174 to 1000P

Signal		DDR1,2	DDR3
MVREF to 1.8V		100R	40.2R
MVREF to GND		100R	100R

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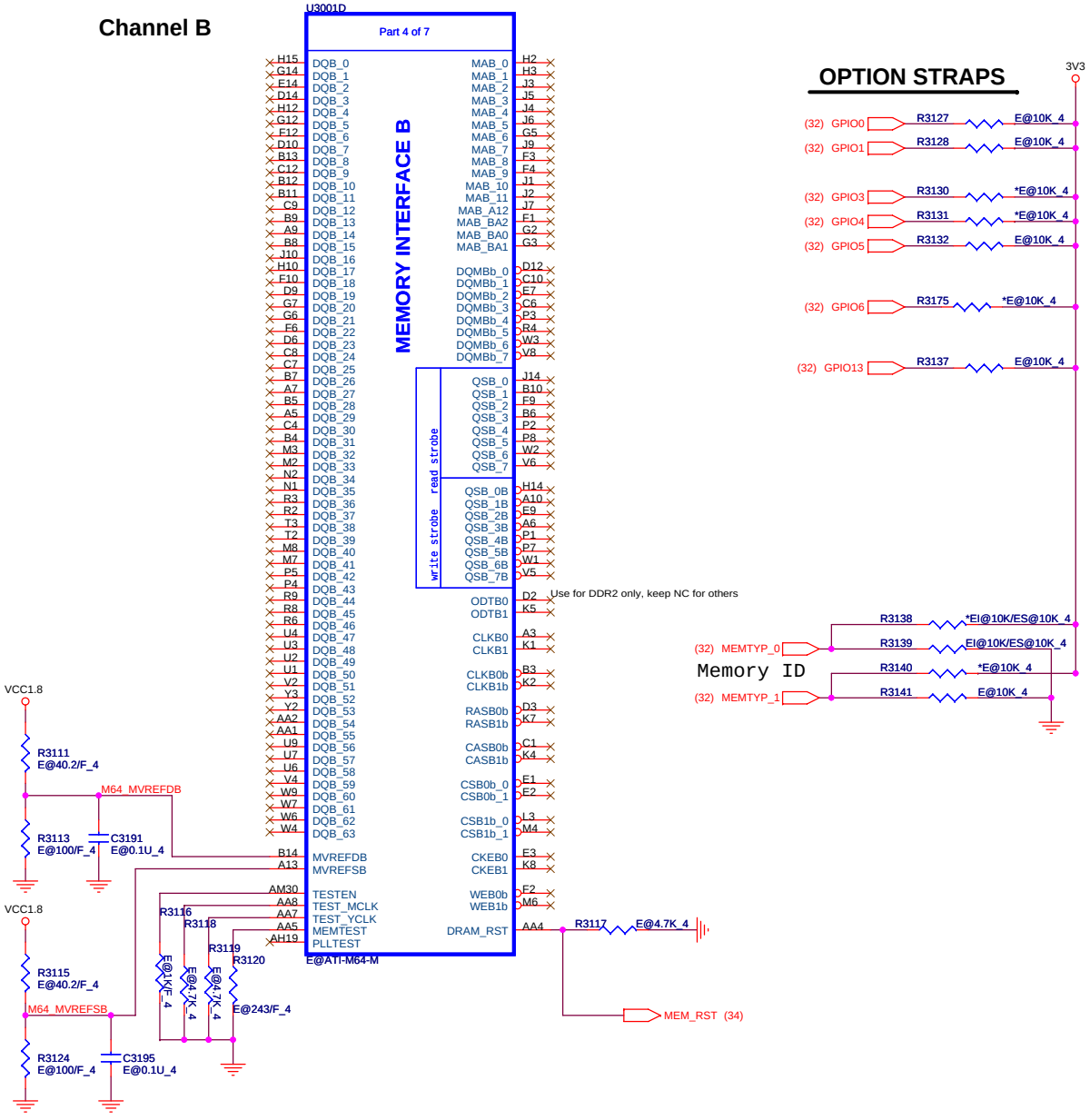
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title	ATI M64M VRAM	
Size: Custom	Document Number: GD1 Main Board	Rev: 1A
Date: Tuesday, November 14, 2006	Sheet 34 of 35	

Channel B



OPTION STRAPS

M64-M Strap

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: full Tx output swing (recommended)	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (recommended)	0 (internal pull-down)
Reserved	GPIO(3:2)	ATI internal use only. Other logic must not affect this signal during RESET.(GPIO2=VDD_VCL)	00
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0 (internal pull-down)
PLL_IBIAS_RD	GPIO[6:5]	Bias Current for the PCI Express PHY PLL	01
Reserved	GPIO8	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128MB 001x - No ROM,MEM_AP_SIZE=01 256MB 010x - No ROM, MEM_AP_SIZE=10 64MB(Default) 011x - No ROM,MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM 1100 - Serial M25P05 ROM (ST), chip IDis from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	GPIO[9,13,12,11] 0000 (internal pull-down)
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port deviced present. 1-No slave VIP port devices reporting presence during reset	0 (internal pull-down)
Reserved	PCIE_TEST	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
Reserved	HSYNC	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0

VRAM Straps REV. 0.1

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE[1:0]	GPIO 27,26	Memory identification for BIOS 00 - Infineon GDDR3 : 2M x 32 bits x 4 banks(Default) 01 - SAMSUNG GDDR3 : 2M x 32 bits x 4 banks 10 - RESERVED 11 - RESERVED	00

MEMTYPE1	MEMTYPE0	R3124	R3125	R3122	R3123	
0	0	NC	10K	NC	10K	00 - Infineon GDDR3 : 2M x 32 bits x 4 banks
0	1	NC	10K	10K	NC	01 - SAMSUNG GDDR3 : 2M x 32 bits x 4 banks
1	0	10K	NC	NC	10K	10 - RESERVED
1	1	10K	NC	10K	NC	11 - RESERVED

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QUANTA COMPUTER

Title: ATI M64-M STRAP

Size: Custom | Document Number: GD1 Main Board | Rev: 1A

Date: Tuesday, November 14, 2006 | Sheet 35 of 35