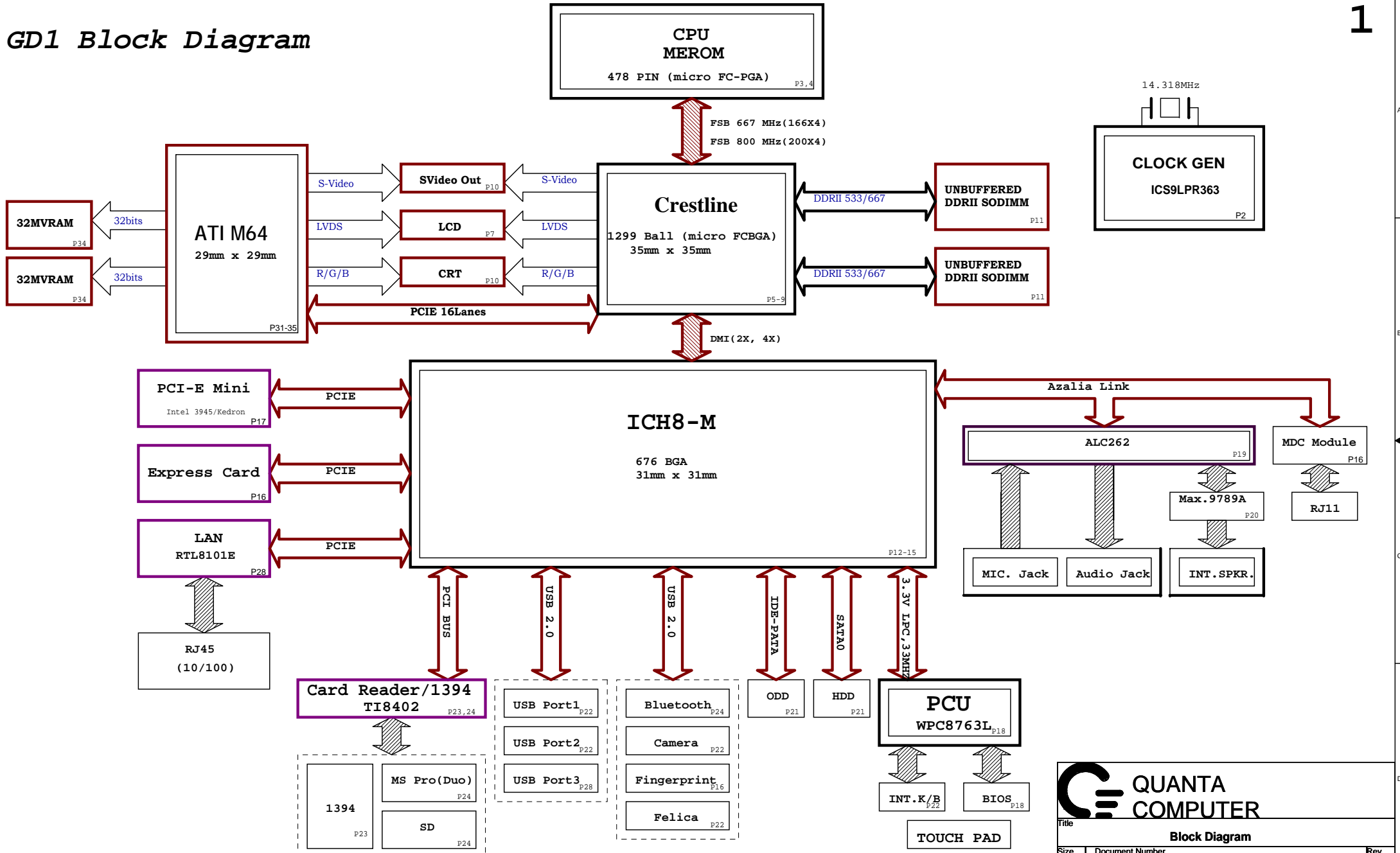


GD1 Block Diagram



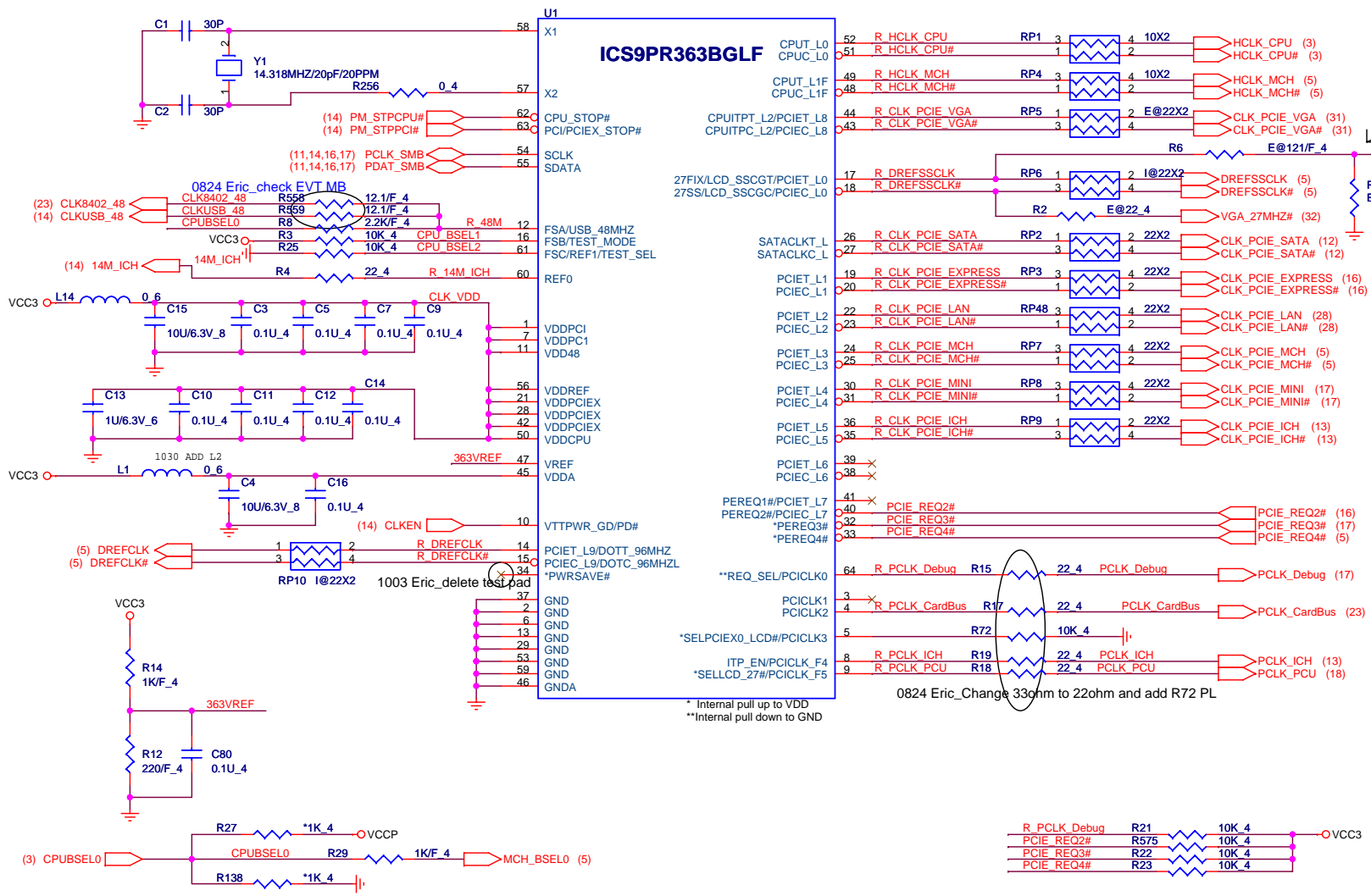
1. Level 1 Environment-related Substances Should NEVER be Used.
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QUANTA COMPUTER

Title: **Block Diagram**

Size: B Document Number: **GD1 Main Board** Rev: 1A

Date: Tuesday, November 14, 2006 Sheet 1 of 35



Check level M64=1.2V; M72/74=1.8V

Signal		965GM	965PM
VGA_27MHZ	R6	NI	121
VGA_27MHZ#	R7	NI	71.5
CLK_PCIE_VGA	RP5	NI	22X2
DREFSSCLK	RP6	22X2	NI
DREFCLK	RP10	22X2	NI

PIN 5 R494	PIN 9 R26	PIN 14/15	PIN 17/18
LO (10K)	LO (10K) HI (NC)	PCIEX9 DOT96	27MHZ LCD
HI (NC)	LO (10K) HI (NC)	PCIEX9 DOT96	PCIEX0 PCIEX0

ITP_EN(PIN8)
 LOW : PIN43/44 SRC
 HIGH : PIN43,44 CPUTIP

PCIE_REQ1#	PCIE_L0	PCIE_L6	
PCIE_REQ2#	PCIE_L1	PCIE_L8	
PCIE_REQ3#	PCIE_L2	PCIE_L4	
PCIE_REQ4#	PCIE_L3	PCIE_L5	PCIE_L7

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB	DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48	96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48	96	0.5 Down
* 0	1	0	200.00	100	33.33	14.318	48	96	0.5 Down
0	1	1	166.66	100	33.33	14.318	48	96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48	96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48	96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48	96	0.5 Down
1	1	1	200.00	100	33.33	14.318	48	96	0.5 Down

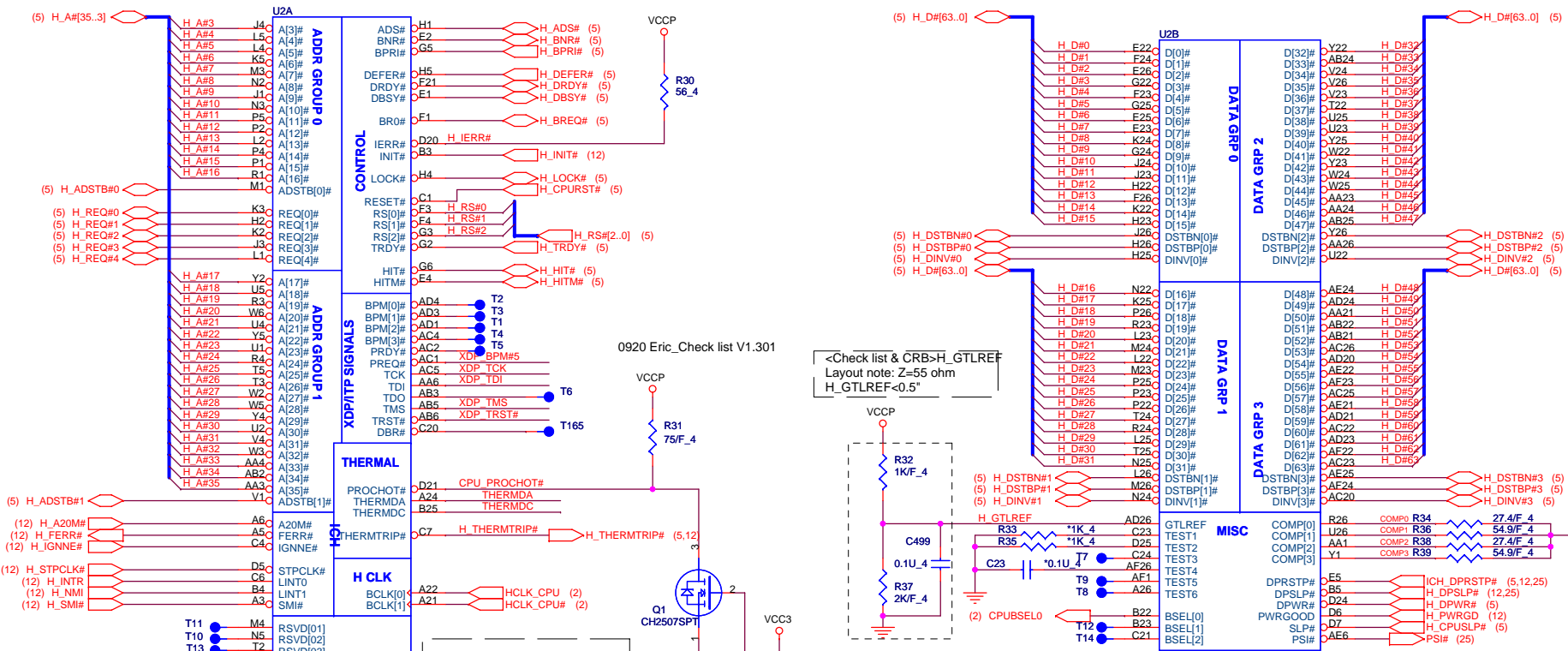
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QUANTA COMPUTER

Title: **CLOCK GENERATOR**

Size B Document Number: **GD1 Main Board** Rev 1A

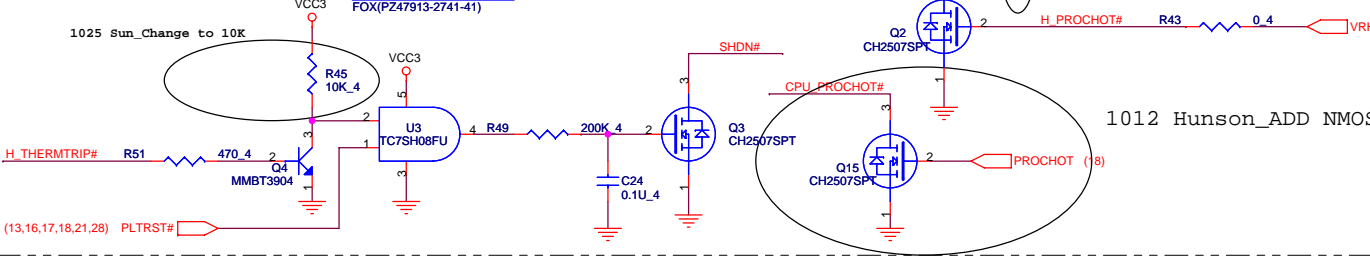
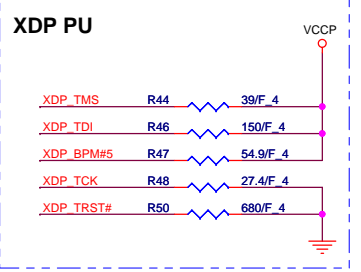
Date: Wednesday, November 15, 2006 Sheet 2 of 35



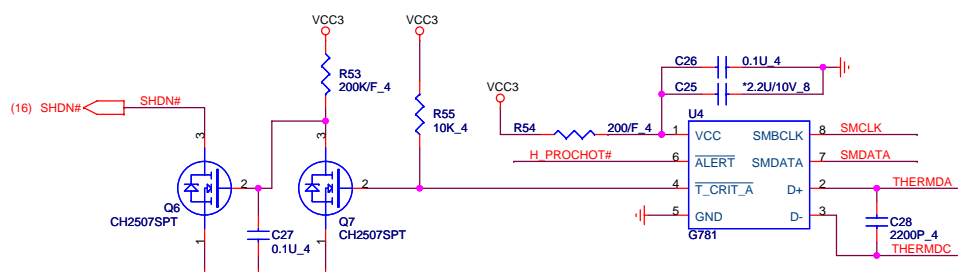
<Check list & CRB>=H_GTLREF
 Layout note: Z=55 ohm
 H_GTLREF<0.5"

Layout note:
 Comp0,2 connect with
 Zo=27.4ohm, make
 trace length shorter than 0.5".
 Comp1,3 connect with Zo=55ohm,
 make
 trace length shorter than 0.5".

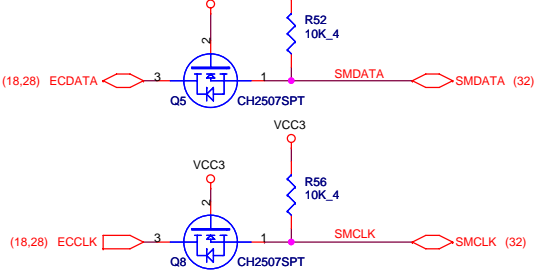
0920 Edward_add



Thermal Sensor

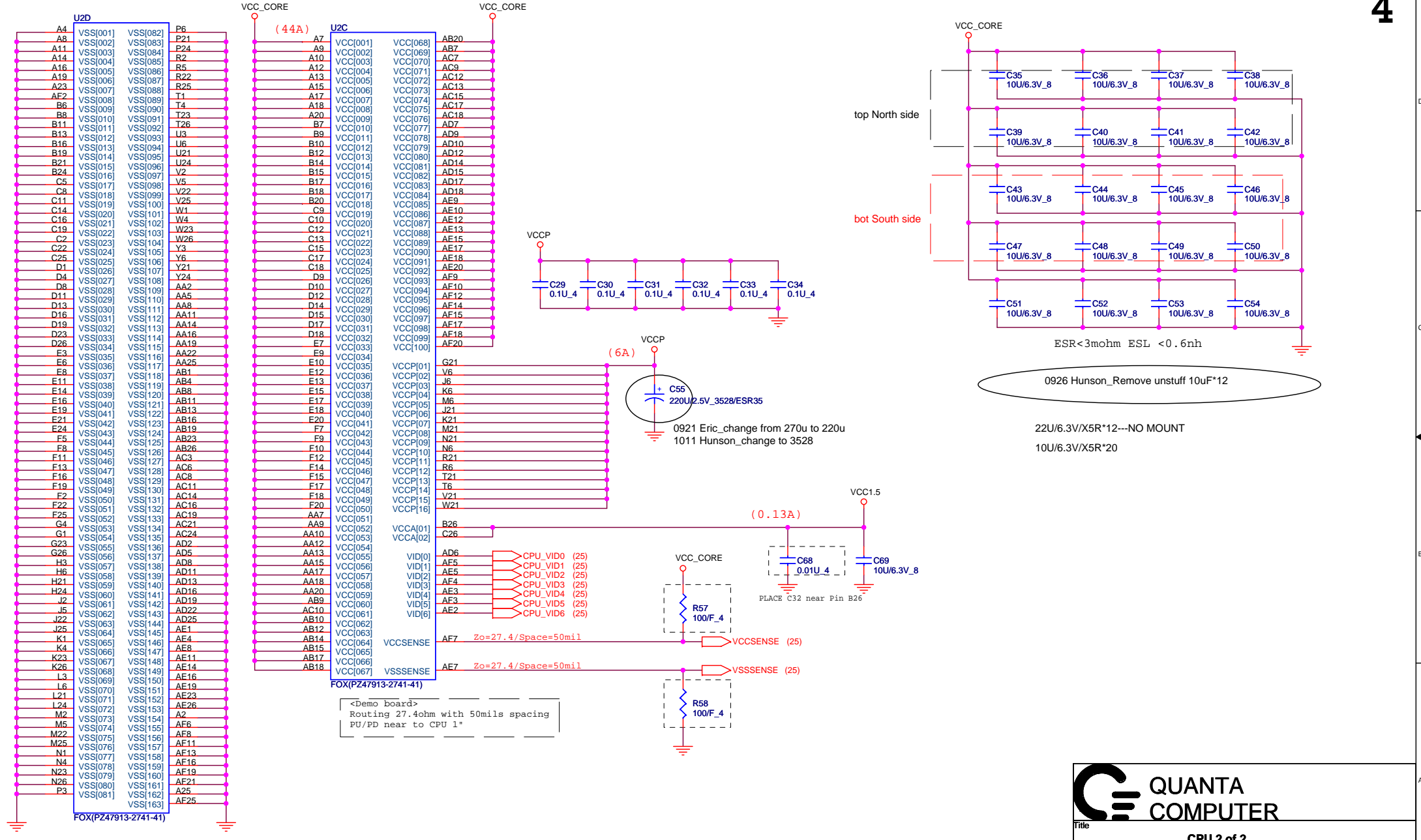


Thermal SMBUS



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QUANTA COMPUTER
 Title: CPU1 of 2
 Size: Document Number: GD1 Main Board
 Date: Tuesday, November 14, 2006 Sheet 3 of 35 Rev 1A



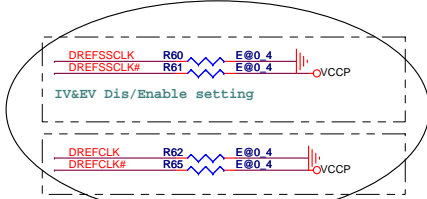
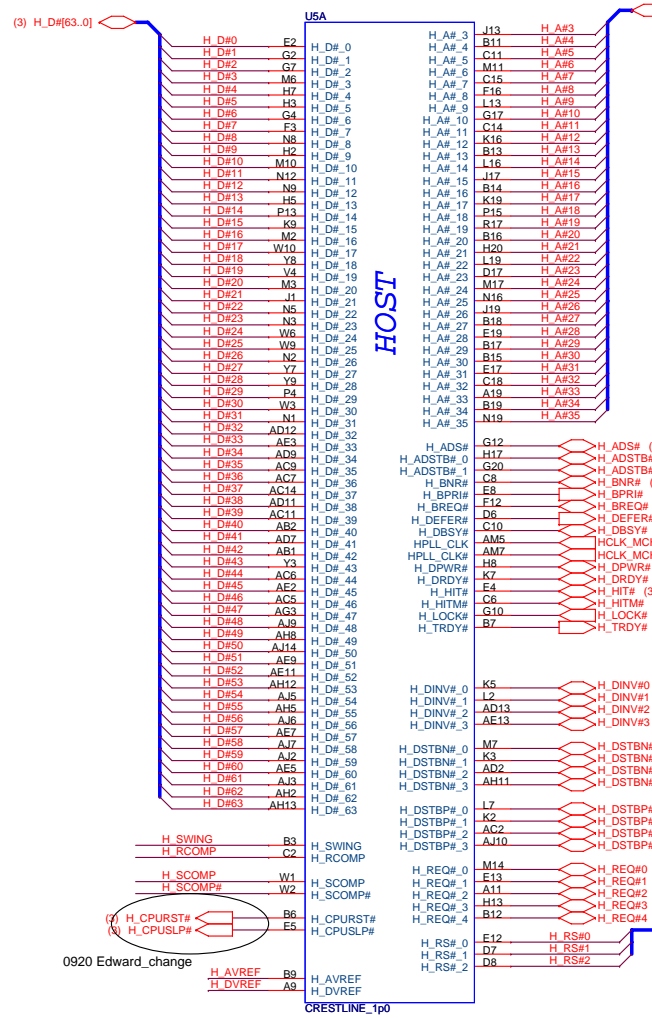
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QUANTA COMPUTER

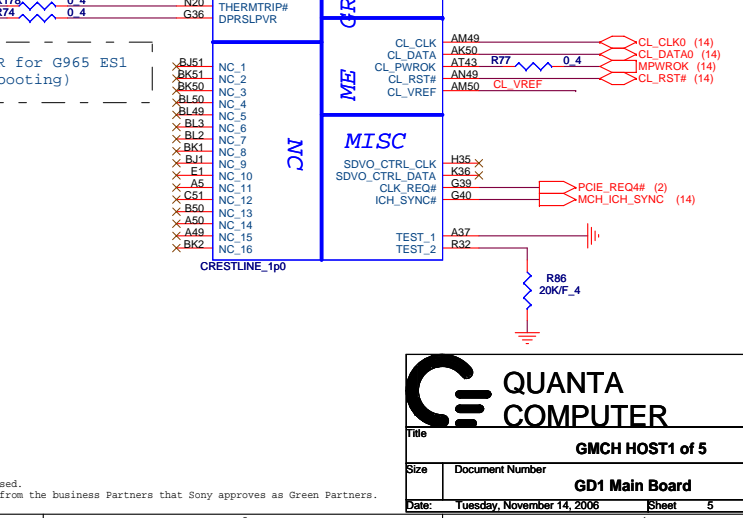
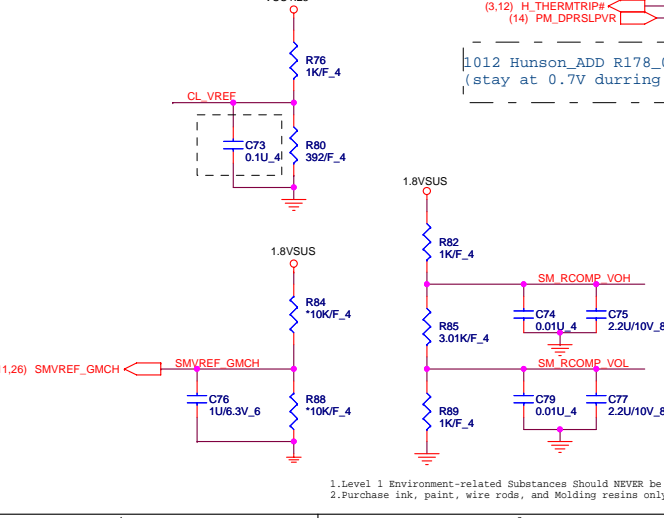
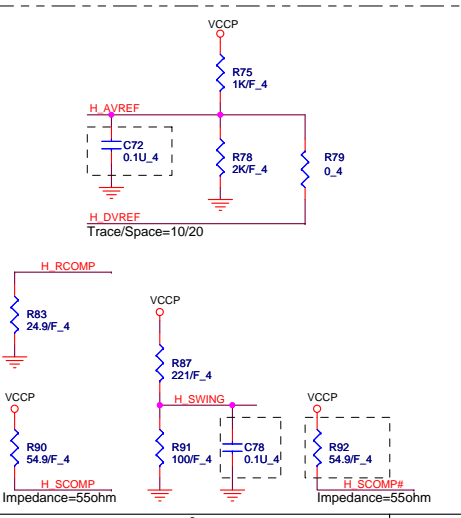
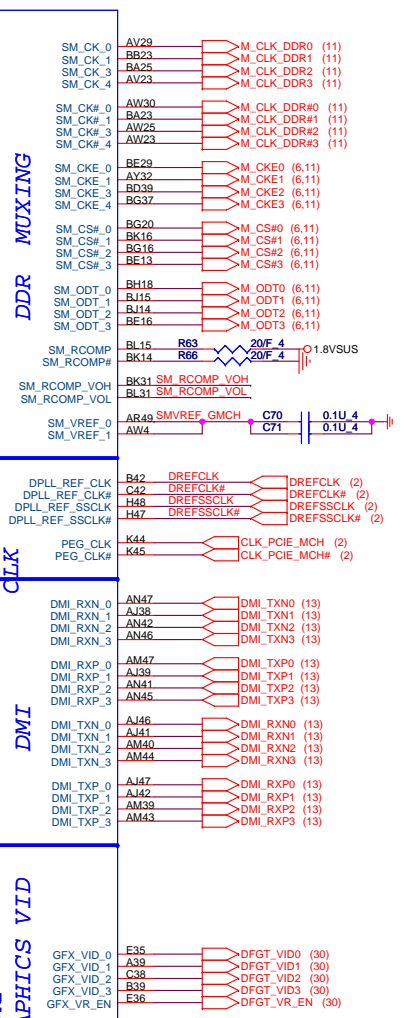
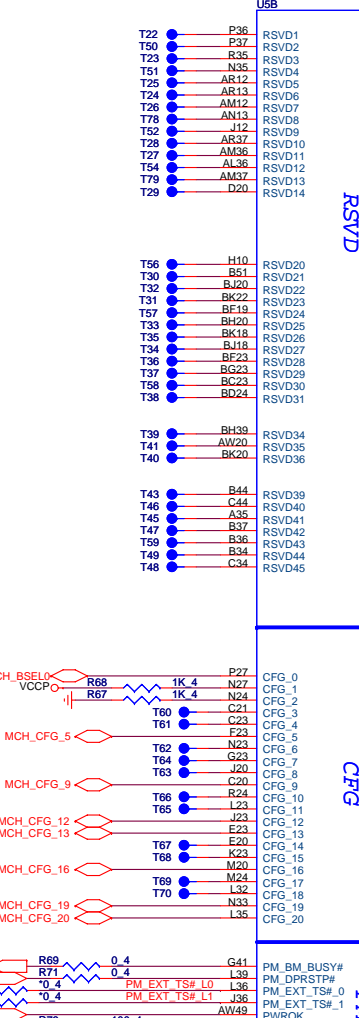
Title: **CPU 2 of 2**

Size B Document Number: **GD1 Main Board** Rev 1A

Date: **Tuesday, November 14, 2006** Sheet 4 of 35



0921 Edward_follow design Guide 1.1 page195



1.Level 1 Environment-related Substances Should NEVER be Used.
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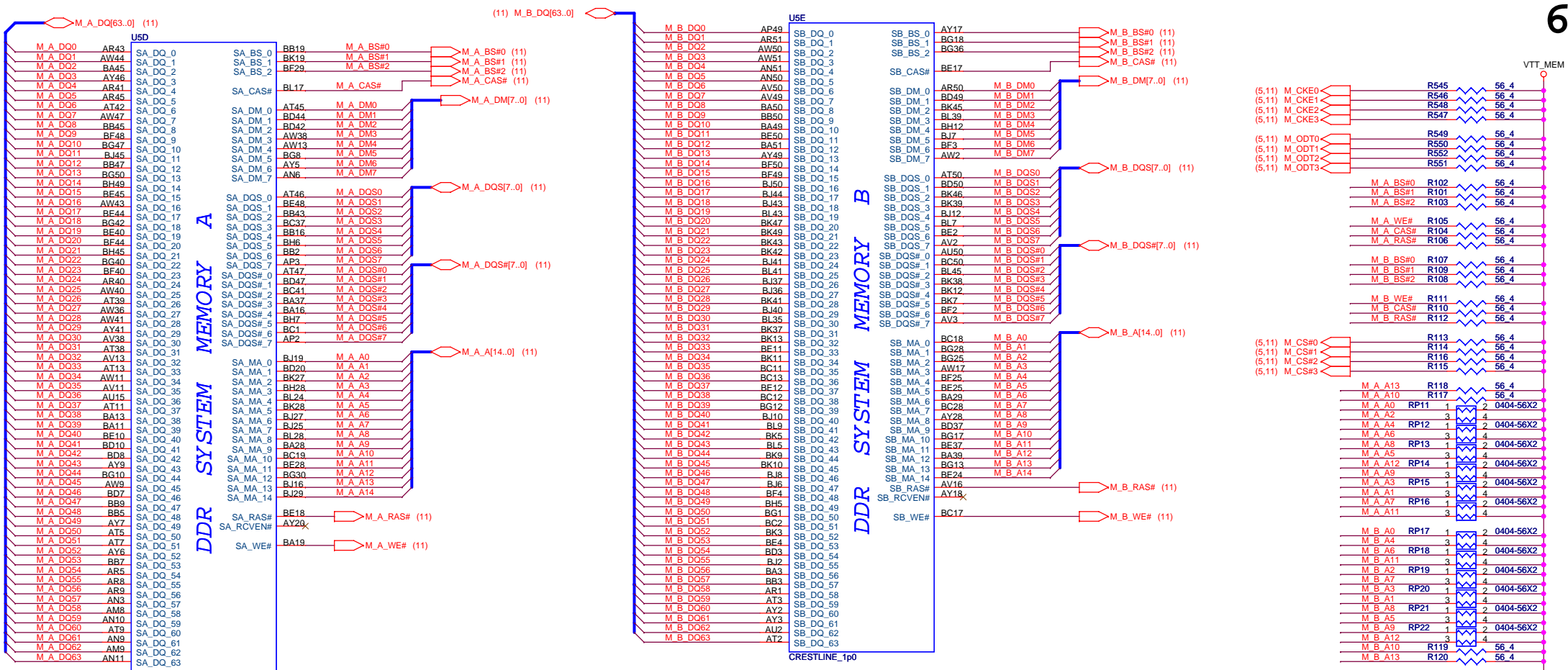
QUANTA COMPUTER

Title: **GMCH HOST1 of 5**

Size: Document Number

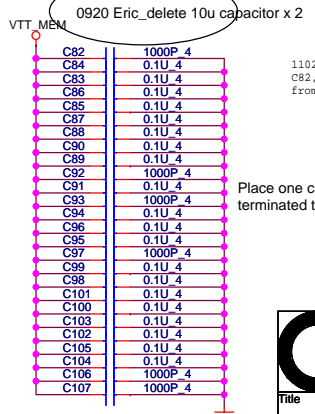
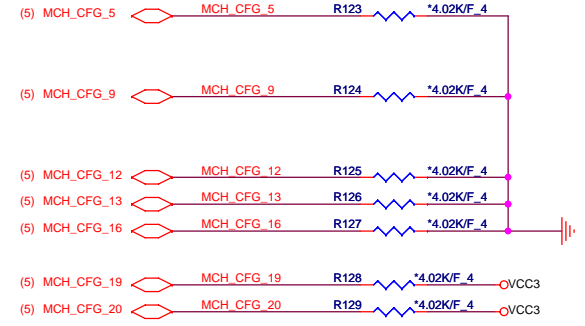
GD1 Main Board

Date: Tuesday, November 14, 2006 Sheet 5 of 35



GMCH Strap pin description

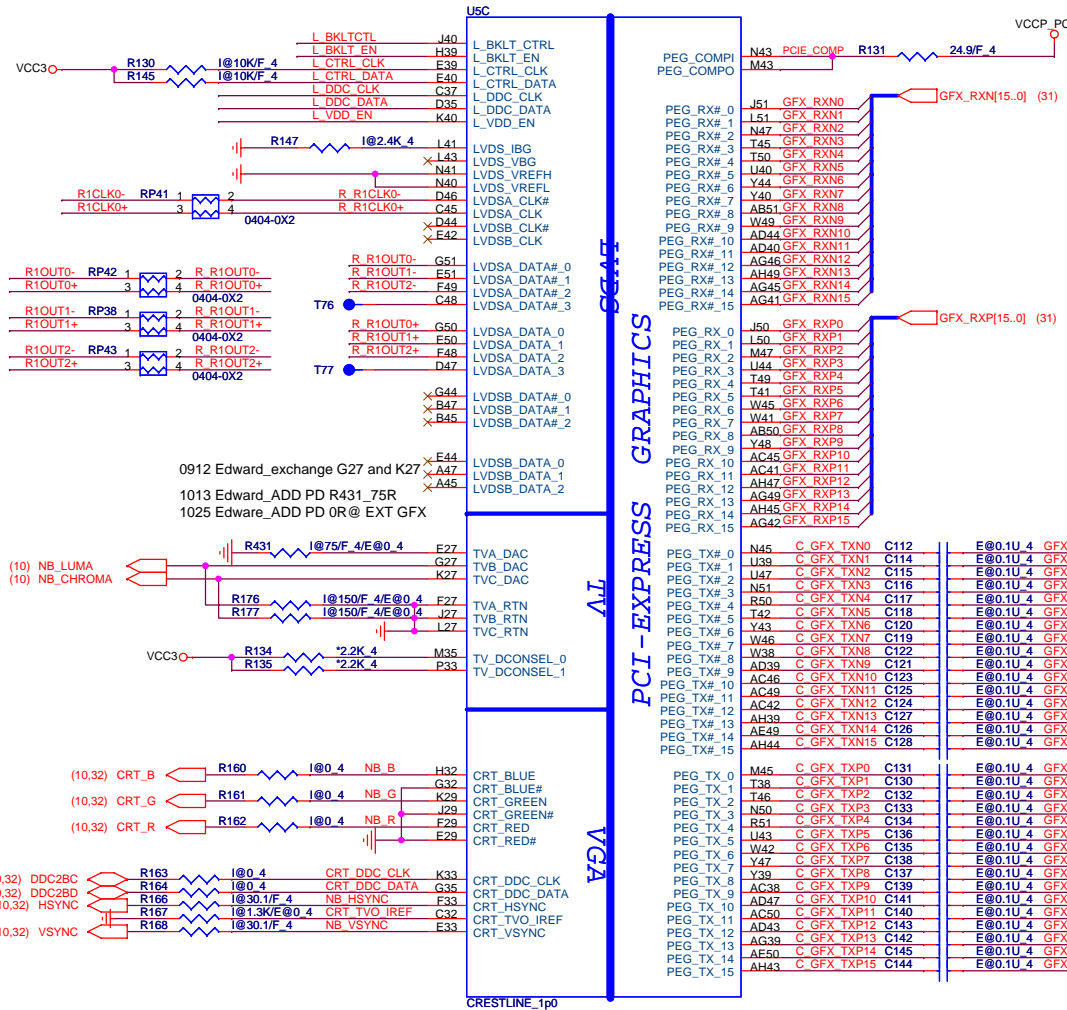
	Low	High
CgF5	DMIX2	* DMIX4
CgF6	RSVD	RSVD for 945GMS
CgF7	RSVD	* CPU type: Mobile CPU
CgF9	PCIe Graphics lan : Reverse Lane	* PCIe Graphics lan : Normal operation
CgF10	reserved	
CgF11	reserved	
CgF16	FSB Dynamic ODT Disabled	* FSB Dynamic ODT Enabled
CgF18	* GMCH core: 1.05V	GMCH core: 1.5V
CgF19	* DMI LANE Normal	DMI LANE Reversed
CgF20	* only SDVO or PCIe x1 is operational	SDVO and PCIe x1 are operation simultaneously via the PEG port
CgF[13:12]	00 = Partial clock gating disable 01 = XOR mode enabled 10 = All-Z mode enabled * 11 = Normal Operation(Default)	
Int.Pull-down : CFG 18,19,20 Int.Pull-high : CFG CFG 3-17		



Place one cap close to every 2 pull-up resistors terminated to VccSus0_9(Total 0.1u x 26)



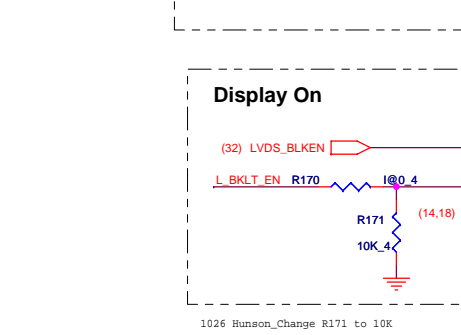
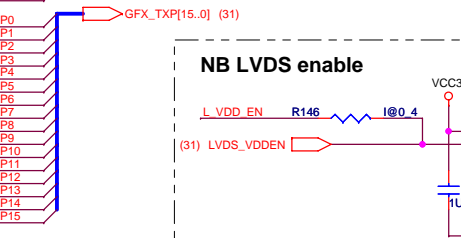
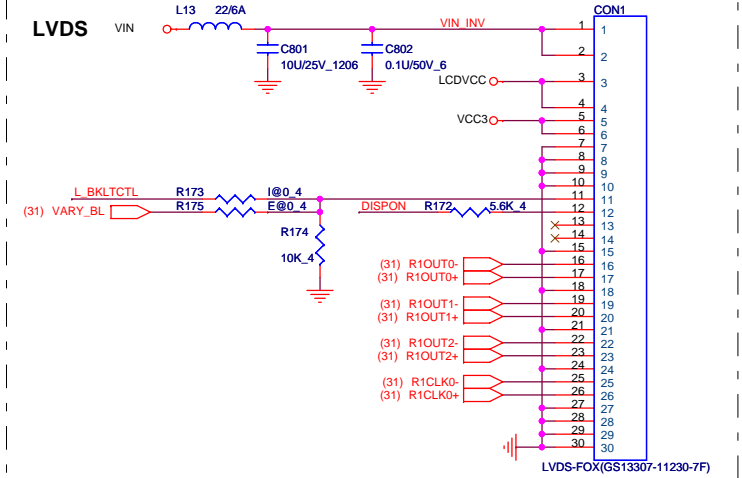
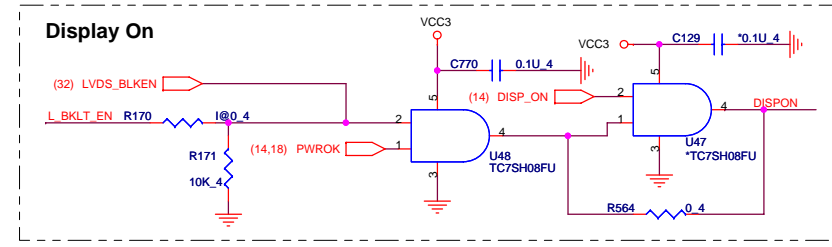
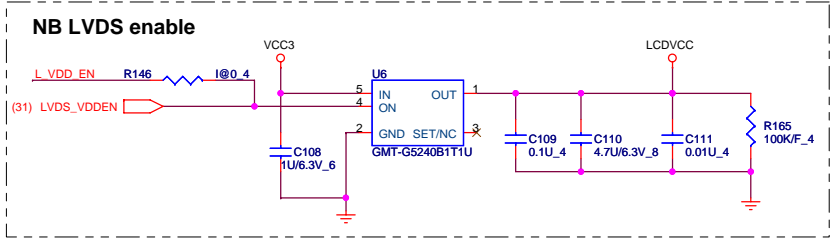
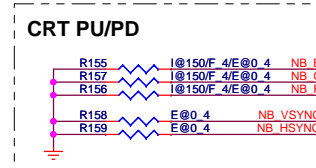
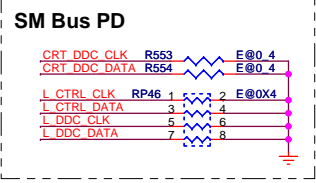
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Signal

Signal	GM965	PM965
NB_VSYNC	NI	0_4
NB_B	30.1_4	NI
NB_HSYNC	30.1_4	NI
GFX	C112, C114~C129, C130~C145	0.1UF_4

Signal		965GM	965PM
NB_B	R160	0_4	NI
NB_G	R157	150_4	0_4
NB_R	R162	0_4	NI
L_IBG	R147	2.4K_4	NI
LVDS	RP38	0X2	NI
L_BKLT_EN	R170	0_4	NI
L_CTRL_CLK	R130	10K	NI
L_CTRL_DATA	RP46	NI	0X4
LVDS_VDDEN	R146	0_4	NI
DDC2BC	R163	0_4	NI
DDC2BD	R164	0_4	NI
CRT_TVO_IREF	R167	1.3K_4	0
L_DDC_CLK	RP46	NI	0X4
L_DDC_DATA	RP46	NI	0X4
BRIGHT	R173	0_4	NI



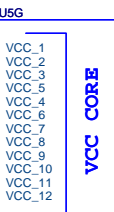
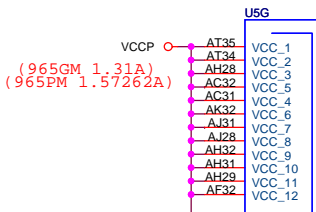
QUANTA COMPUTER

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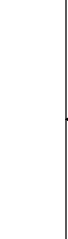
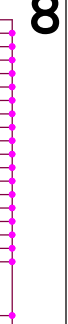
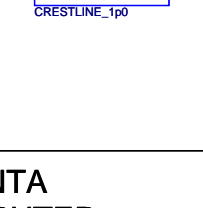
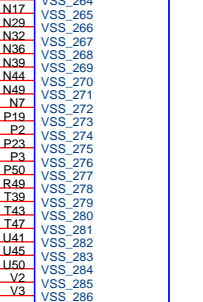
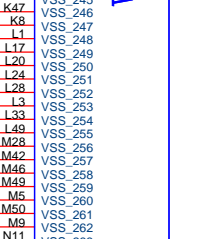
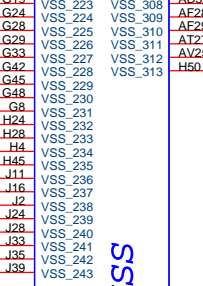
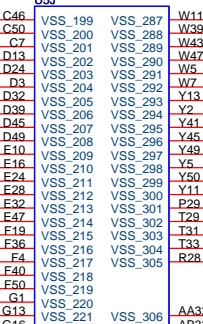
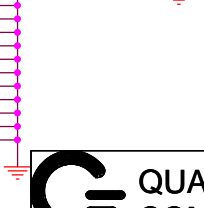
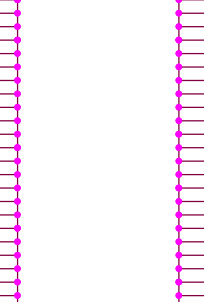
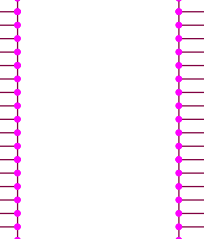
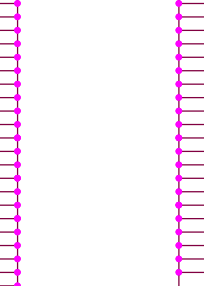
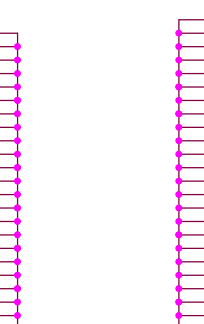
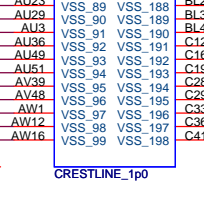
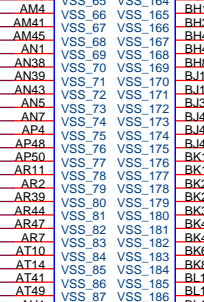
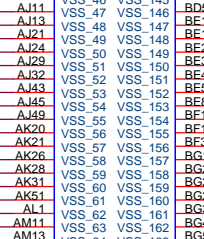
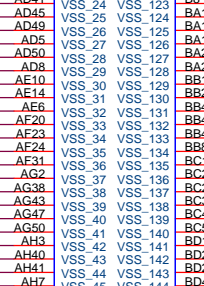
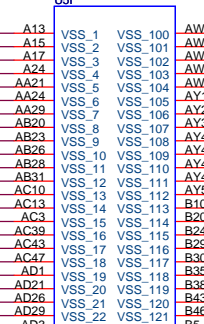
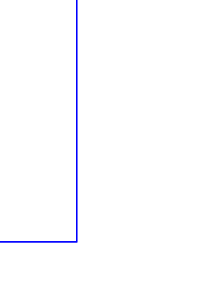
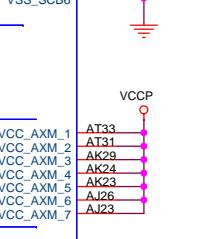
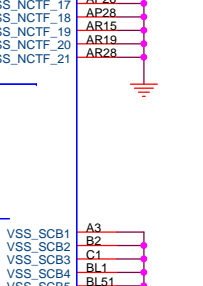
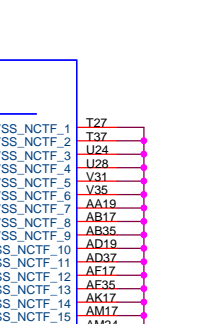
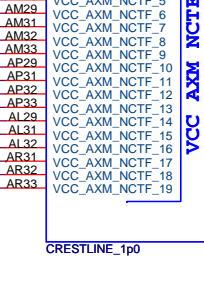
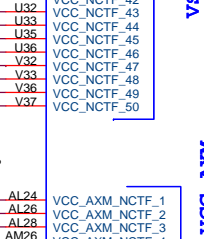
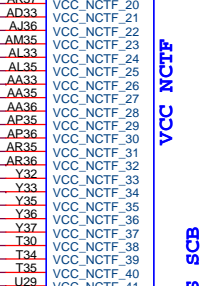
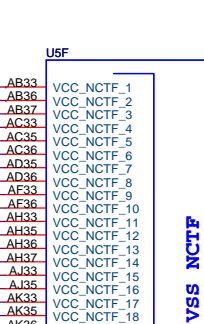
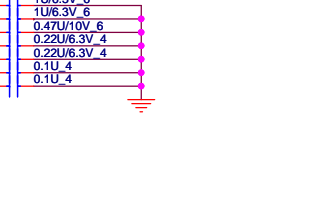
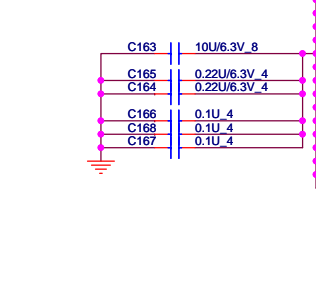
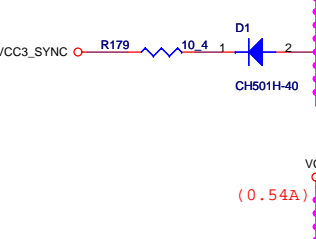
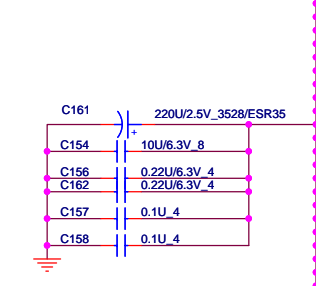
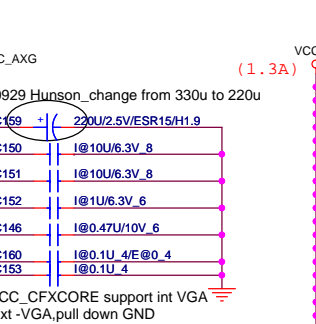
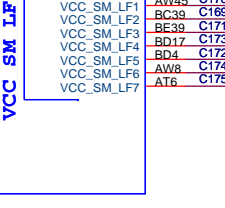
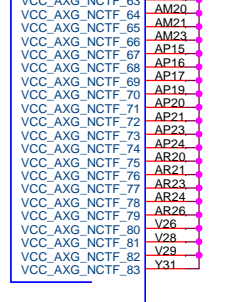
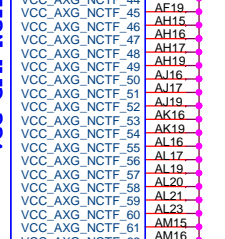
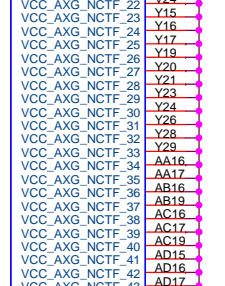
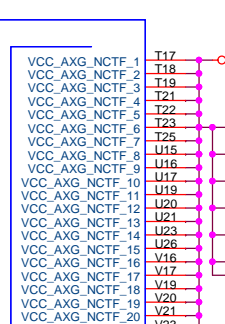
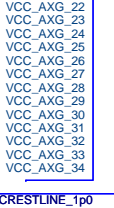
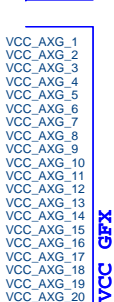
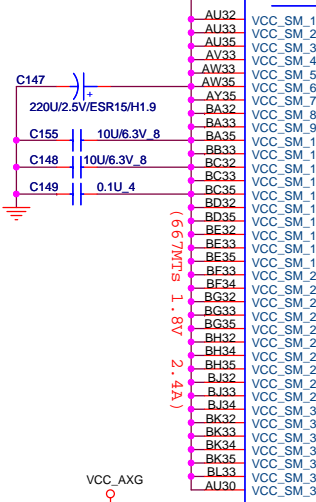
Size: Document Number **GD1 Main Board** Rev 1A

Date: Tuesday, November 14, 2006 Sheet 7 of 35

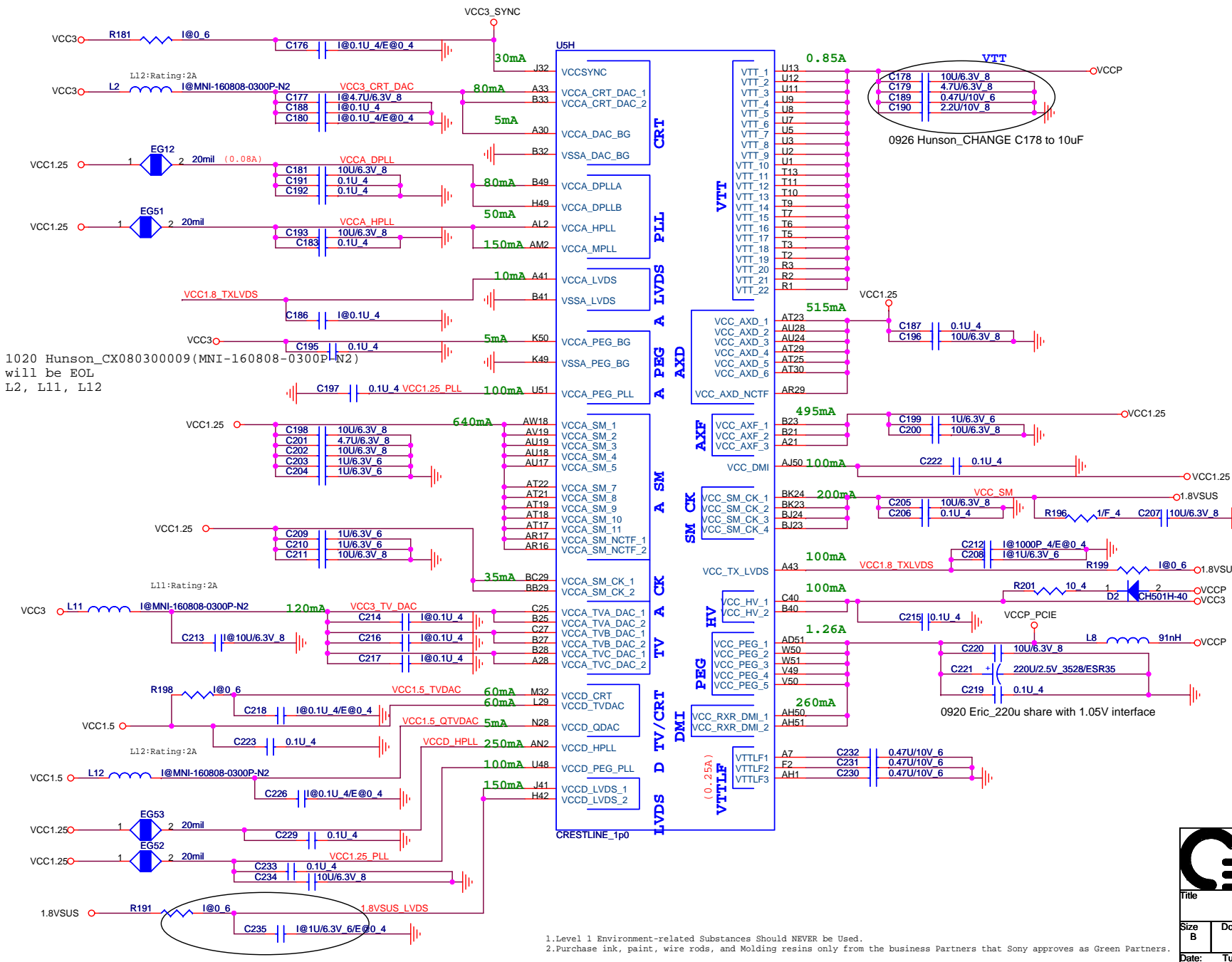
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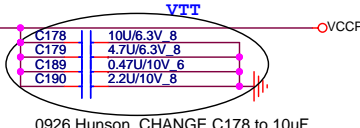
POWER



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1020 Hunson_CX080300009 (MNI-160808-0300P-N2) will be EOL L2, L11, L12



0926 Hunson_CHANGE C178 to 10uF

Signal		965GM	965PM
VCCA_TV_DAC	L12	v	x
	C244	v	x
	C245	v	x
	C246	v	x
	C248	v	x
	R193	x	v
VCC1.5_TVDAC	L14	v	x
	C250	v	x
	C247	v	x
	R195	x	v
VCC1.5_QTVDAC	L17	v	x
	C257	v	x
	C258	v	x
	R197	x	v

Signal		965GM	965PM
VCCA_DAC_BG	L8	v	x
	C214	v	x
	R181	x	v
VCCSYNC	R177	v	x
	C201	v	x
	C202	v	x
	R178	x	v
VCC3_CRT_DAC	L7	v	x
	C203	v	x
	C211	v	x
	R179	x	v
VCCD_LVDS	R198	v	x
	C265	v	x
	C264	v	x
	R199	x	v
VCCA_LVDS	R183	0_4	NC
	C208	0.01u_4	NC
	C209	0.1u_4	NC
	R184	NC	0_4
VCC_TX_LVDS	R192	v	x
	C240	v	x
	C238	v	x
	C239	v	x
	R191	x	v

QUANTA COMPUTER

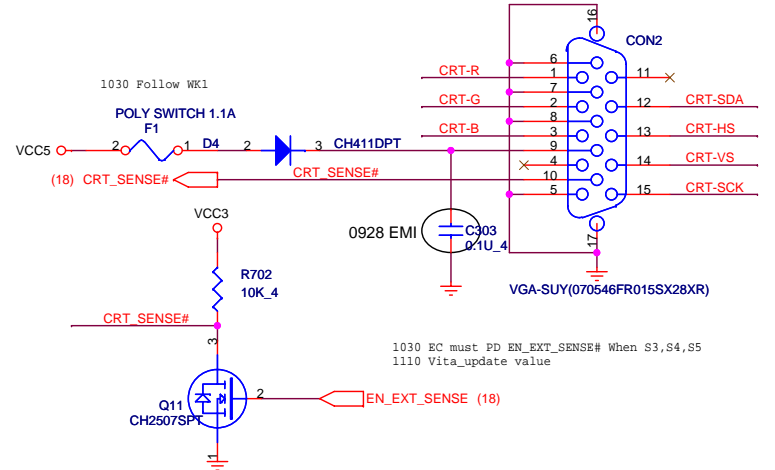
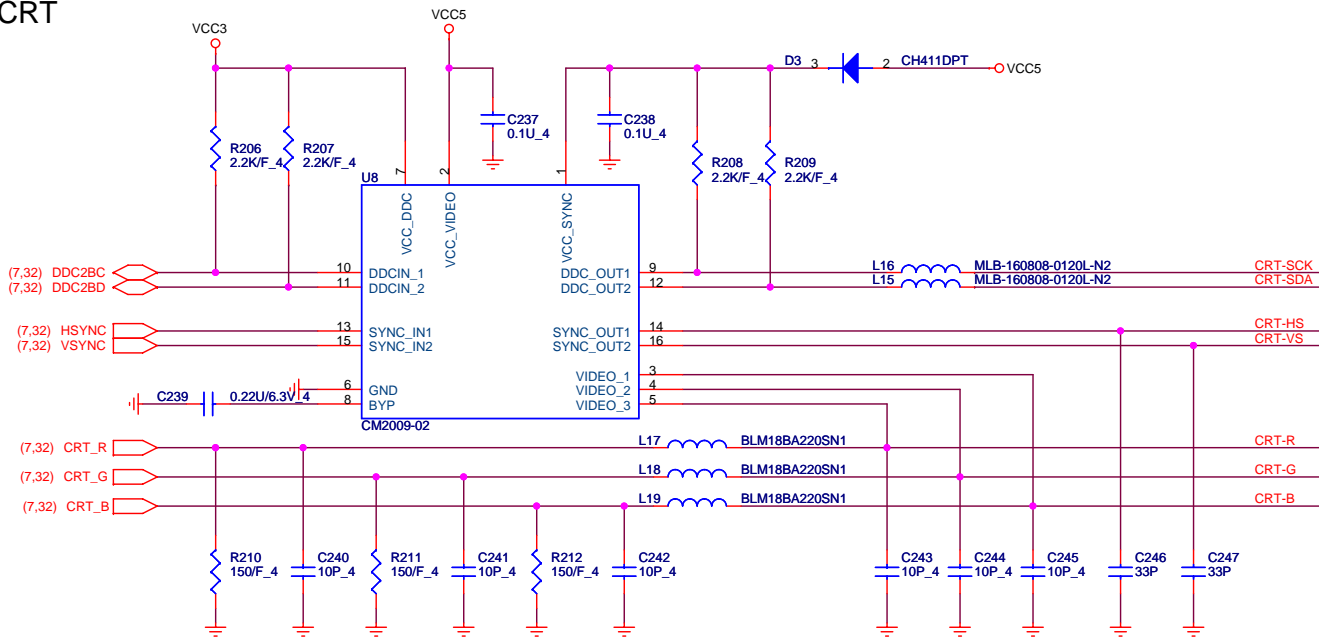
Title: **GMCH Power 2.5 of 5**

Size B Document Number: **GD1 Main Board** Rev 1A

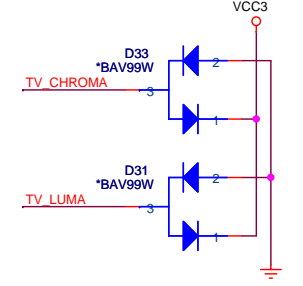
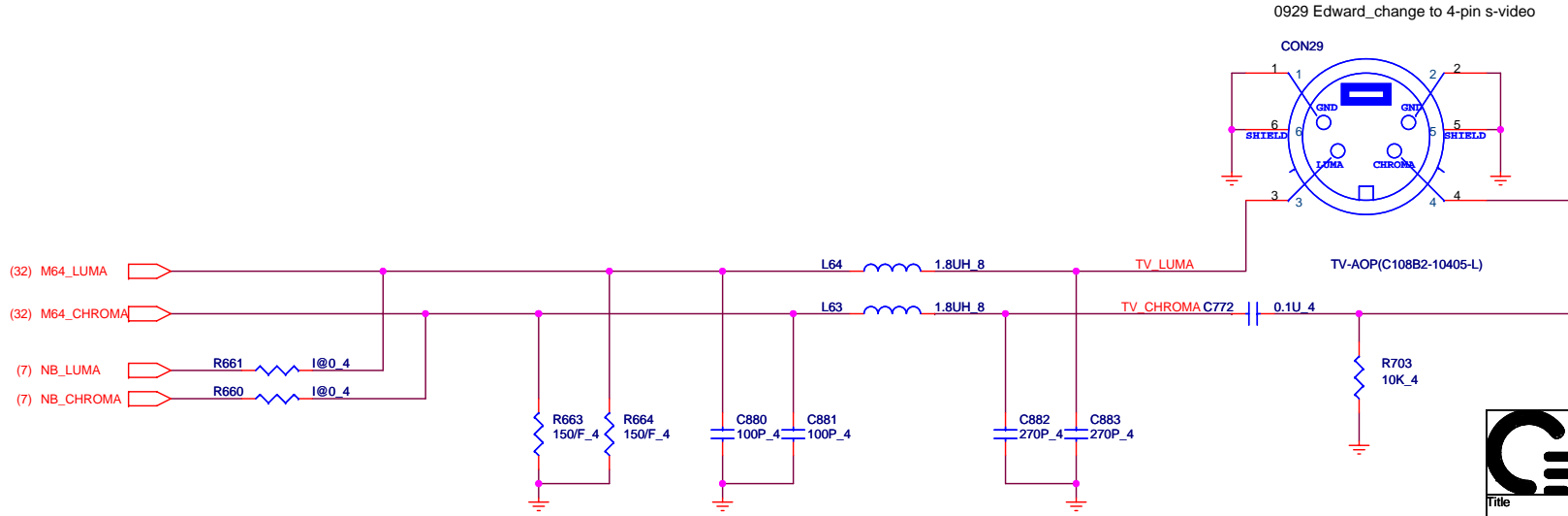
Date: Tuesday, November 14, 2006 Sheet 9 of 35

1.Level 1 Environment-related Substances should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

CRT



S-VIDEO_OUT



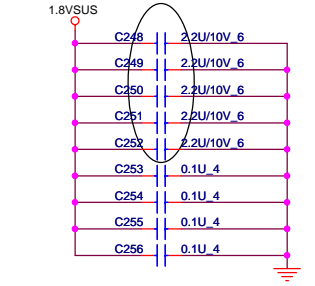
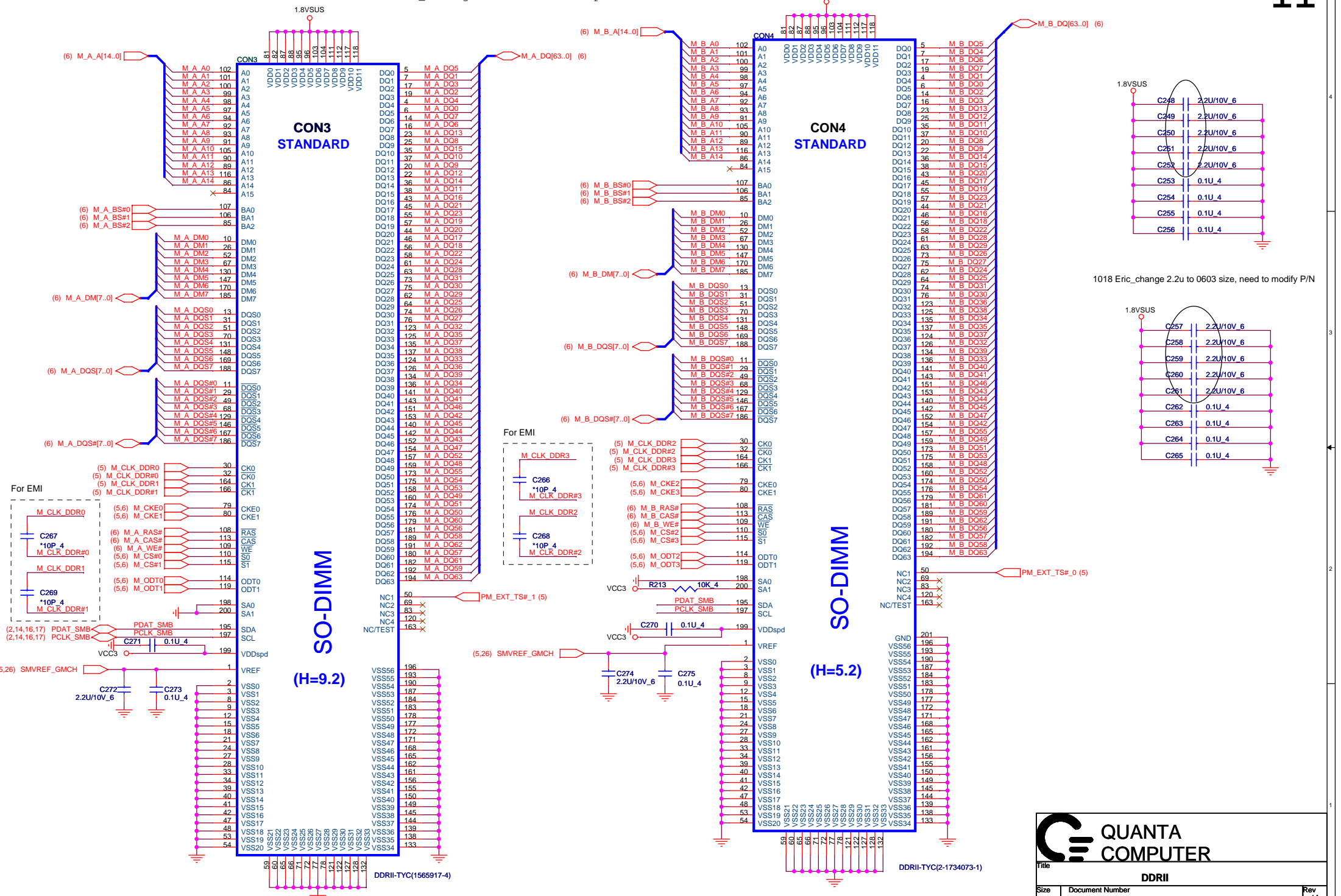
1.Level 1 Environment-related Substances should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

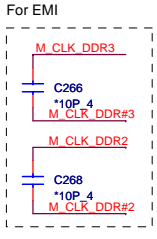
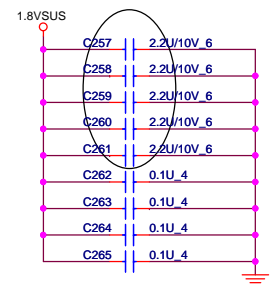
Title: **CRT & S-VIDEO**

Size B Document Number: **GD1 Main Board** Rev 1A

Date: Wednesday, November 15, 2006 Sheet 10 of 35



1018 Eric_change 2.2u to 0603 size, need to modify P/N



QUANTA COMPUTER

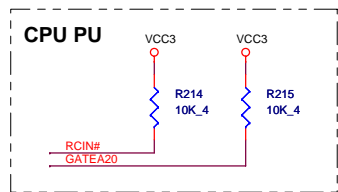
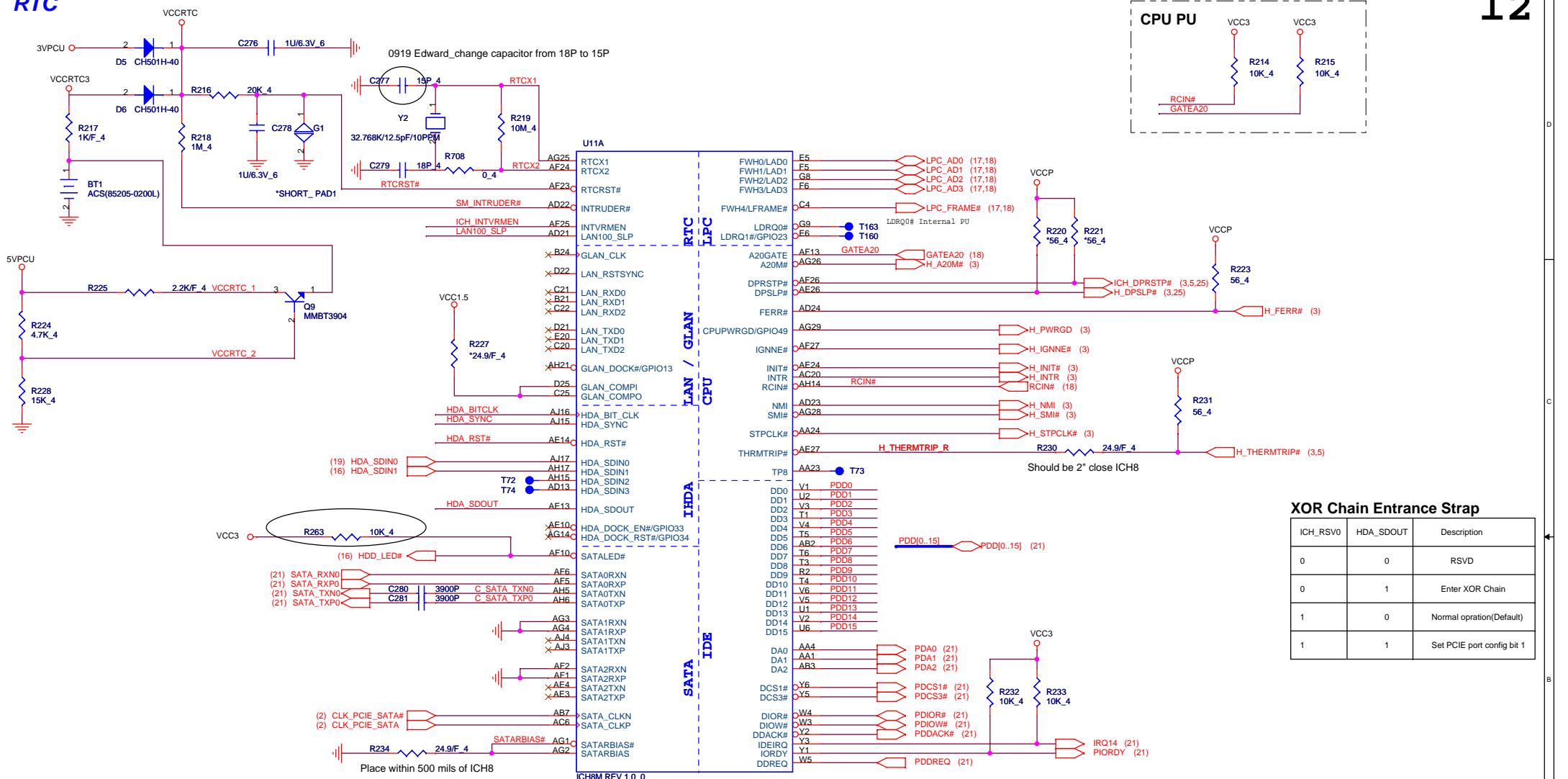
Title: **DDRII**

Document Number: **GD1 Main Board**

Date: **Wednesday, November 15, 2006** Sheet **11** of **35**

Rev **1A**

1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

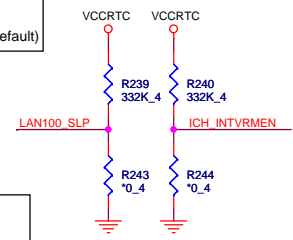
ICH8 strap

ICH8-M LAN100_SLP Strap
 (Internal VR for VccLAN1_05 and VccCL1.05)

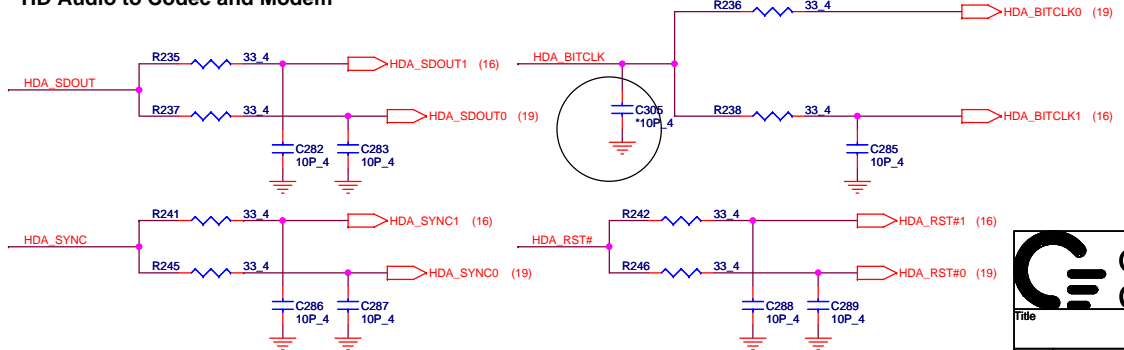
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---

ICH_INTVRMEN	Low = Disable High = Enable(Default)
--------------	---

ICH8-M Internal VR Enable strap
 (Internal VR for Vccsus1_05, VccSus1_5 and VccCL1_5)



HD Audio to Codec and Modem

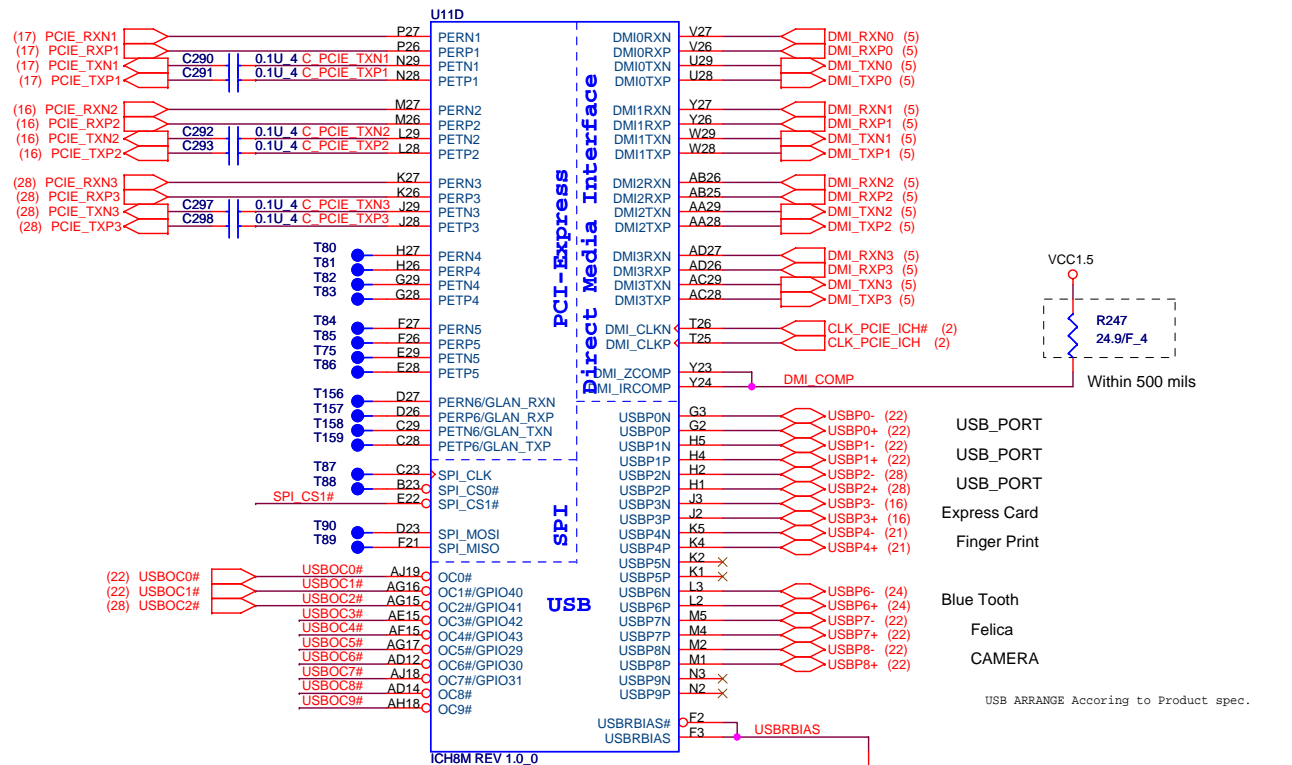


1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: ICH8-M HOST 1 of 4
 Size: Document Number: GD1 Main Board Rev 1A
 Date: Tuesday, November 14, 2006 Sheet 12 of 35

WireLess Lan
Express card
10/100 Lan



PCI bus info.

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
T18402	AD23	REQ0# / GNT0#	PIRQ E/F/G

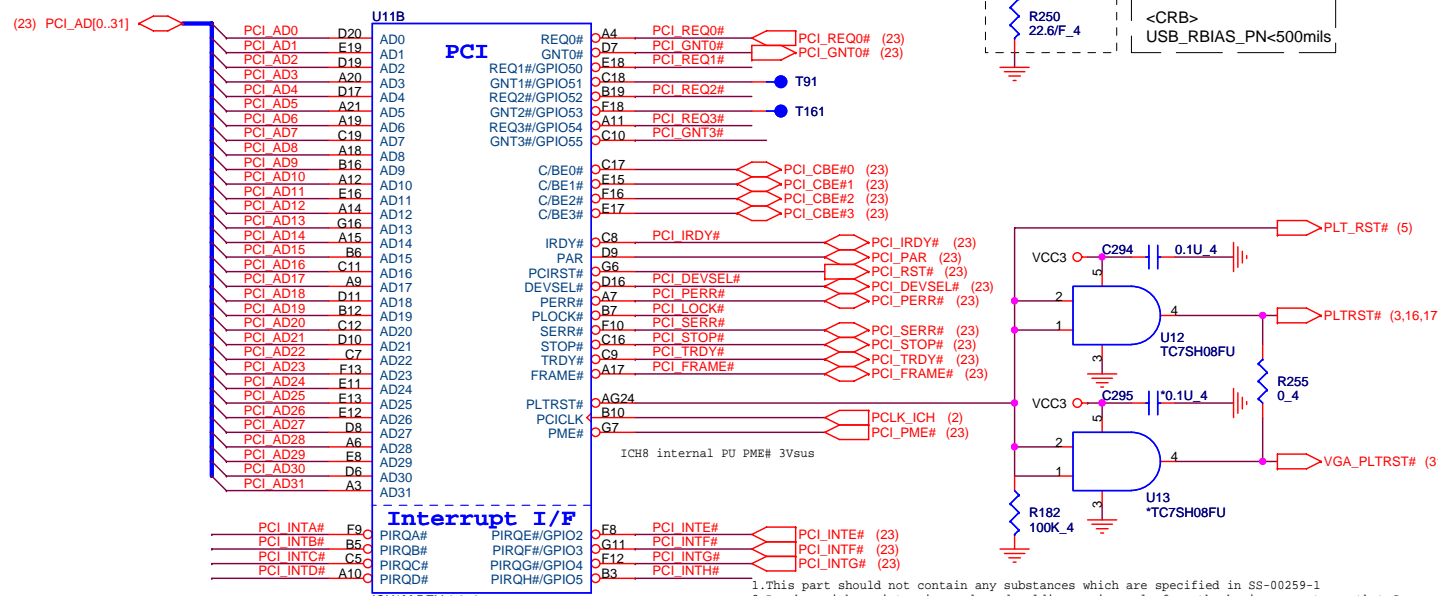
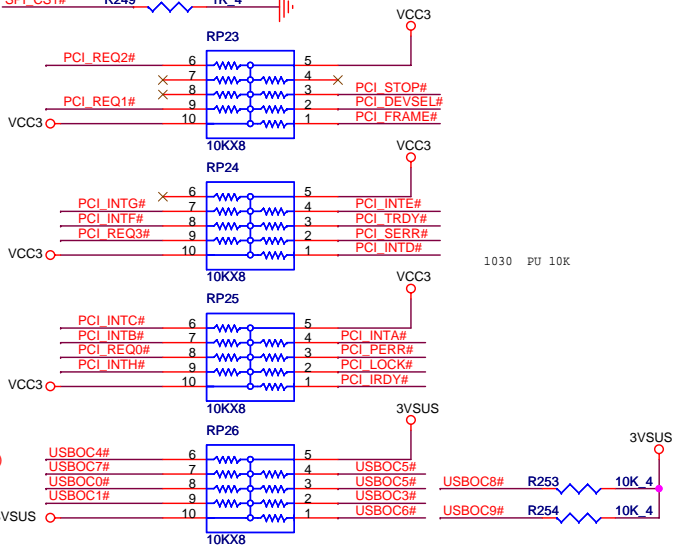
A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default
-----------	---



ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)



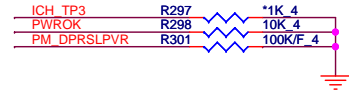
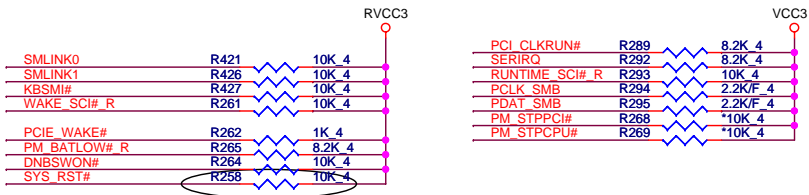
1. This part should not contain any substances which are specified in SS-00259-1
 2. Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

QUANTA COMPUTER

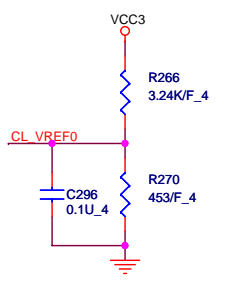
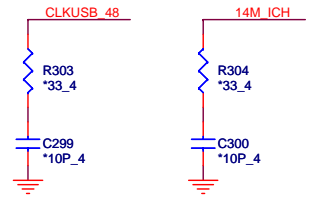
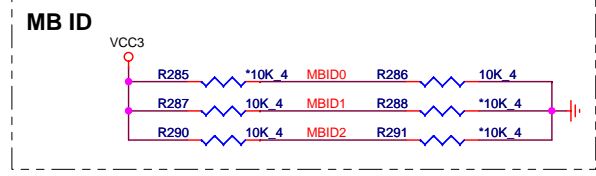
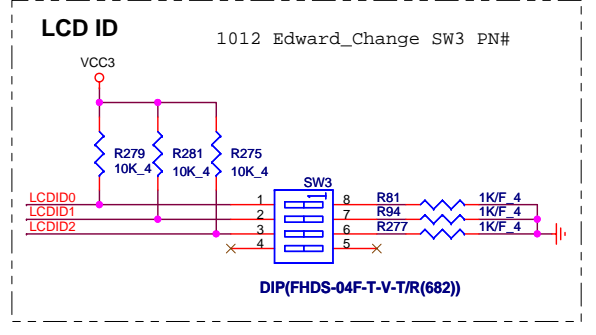
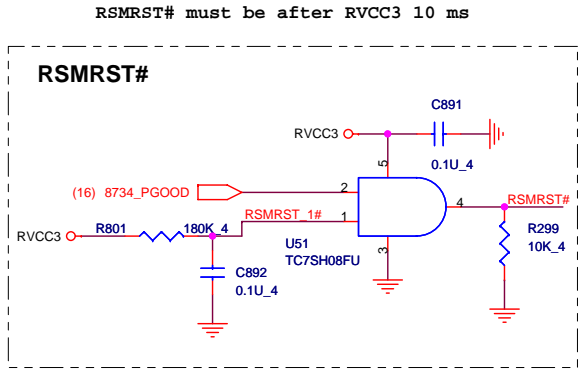
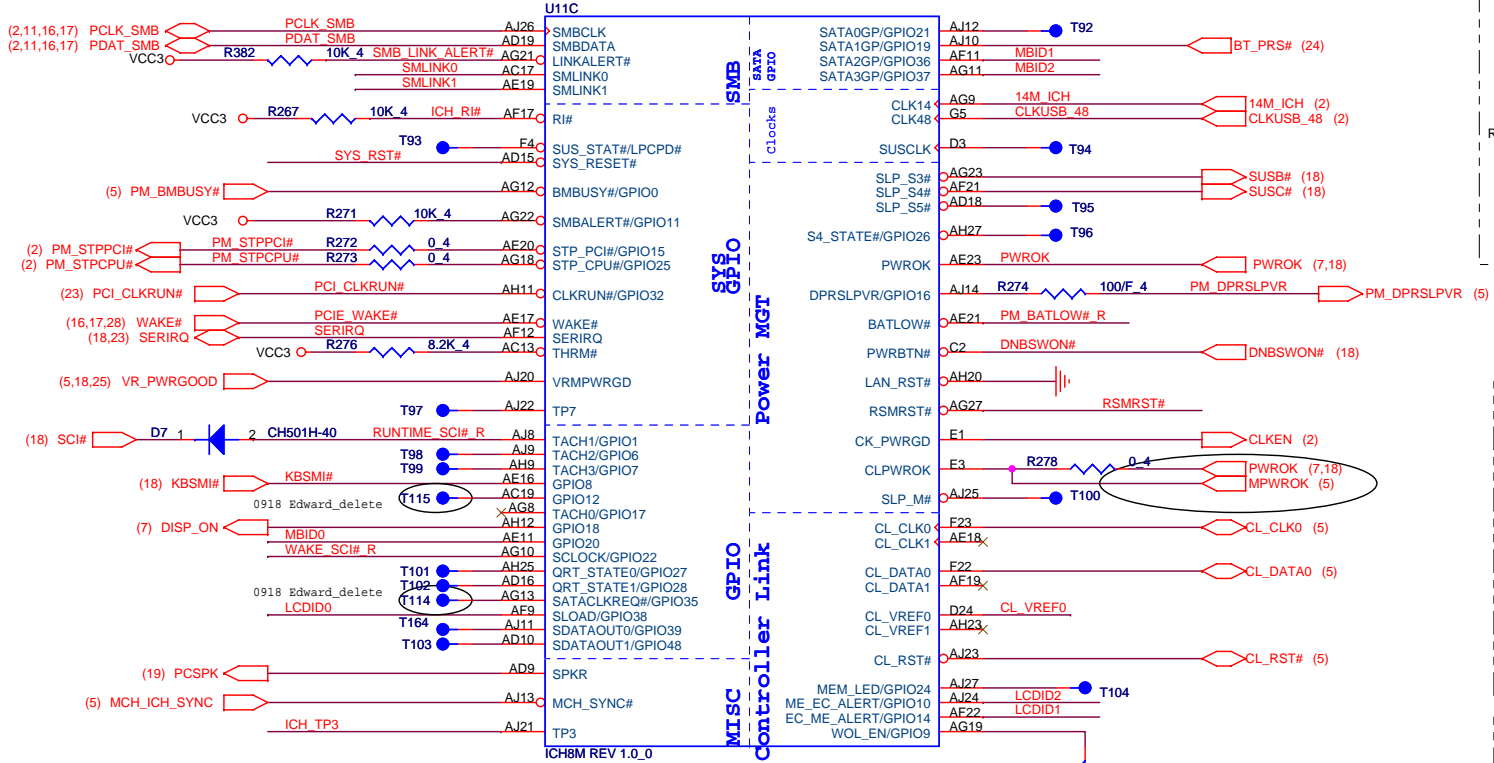
Title: ICH8-M PCIE 2 of 4

Size B Document Number: GD1 Main Board Rev 1A

Date: Tuesday, November 14, 2006 Sheet 13 of 35



0915 Edward.Tsai follow intel check list

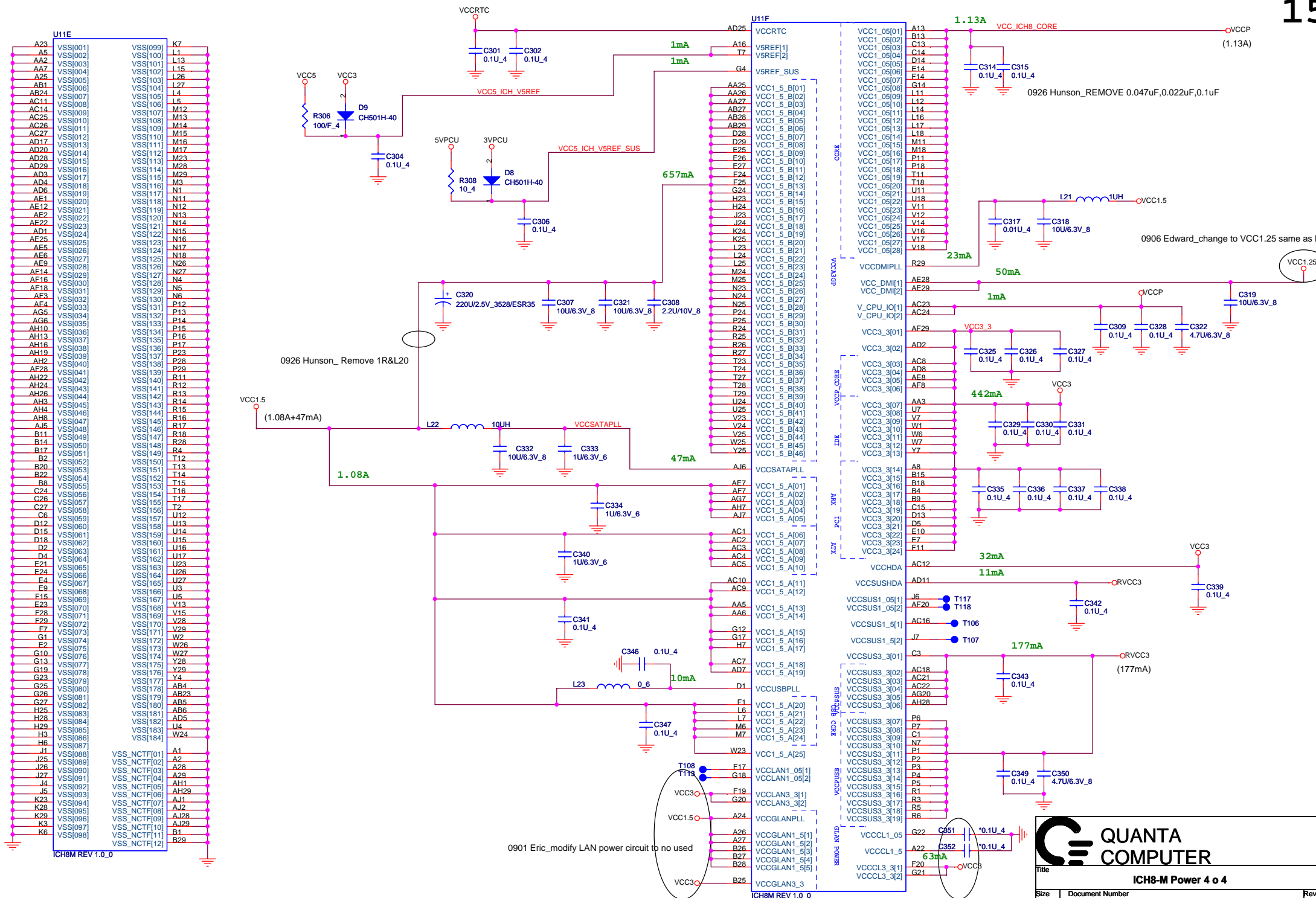


1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

**QUANTA
COMPUTER**

Title: **ICH8-M GPIO 3 of 4**

Size B	Document Number	Rev 1A
GD1 Main Board		
Date:	Wednesday, November 15, 2006	Sheet 14 of 35



U11E

A23	VSS[001]	VSS[099]	K7
A5	VSS[002]	VSS[100]	L1
AA2	VSS[003]	VSS[101]	L13
AA7	VSS[004]	VSS[102]	L15
AA5	VSS[005]	VSS[103]	L26
AB1	VSS[006]	VSS[104]	L27
AB24	VSS[007]	VSS[105]	L28
AC11	VSS[008]	VSS[106]	L5
AC14	VSS[009]	VSS[107]	M12
AC25	VSS[010]	VSS[108]	M13
AC26	VSS[011]	VSS[109]	M14
AC27	VSS[012]	VSS[110]	M15
AD17	VSS[013]	VSS[111]	M16
AD20	VSS[014]	VSS[112]	M17
AD28	VSS[015]	VSS[113]	M23
AD29	VSS[016]	VSS[114]	M28
AD3	VSS[017]	VSS[115]	M29
AD4	VSS[018]	VSS[116]	M3
AD6	VSS[019]	VSS[117]	N1
AD7	VSS[020]	VSS[118]	N11
AE1	VSS[021]	VSS[119]	N12
AE12	VSS[022]	VSS[120]	N13
AE2	VSS[023]	VSS[121]	N14
AD1	VSS[024]	VSS[122]	N15
AE25	VSS[025]	VSS[123]	N16
AE5	VSS[026]	VSS[124]	N17
AE6	VSS[027]	VSS[125]	N18
AE9	VSS[028]	VSS[126]	N26
AF14	VSS[029]	VSS[127]	N27
AF16	VSS[030]	VSS[128]	N4
AF18	VSS[031]	VSS[129]	N6
AF3	VSS[032]	VSS[130]	P12
AF4	VSS[033]	VSS[131]	P13
AG5	VSS[034]	VSS[132]	P14
AG6	VSS[035]	VSS[133]	P15
AH10	VSS[036]	VSS[134]	P16
AH13	VSS[037]	VSS[135]	P17
AH16	VSS[038]	VSS[136]	P23
AH19	VSS[039]	VSS[137]	P28
AH2	VSS[040]	VSS[138]	P29
AF28	VSS[041]	VSS[139]	R11
AH22	VSS[042]	VSS[140]	R12
AH24	VSS[043]	VSS[141]	R13
AH26	VSS[044]	VSS[142]	R14
AH3	VSS[045]	VSS[143]	R15
AH4	VSS[046]	VSS[144]	R16
AH8	VSS[047]	VSS[145]	R17
AJ5	VSS[048]	VSS[146]	R18
B11	VSS[049]	VSS[147]	R28
B14	VSS[050]	VSS[148]	R4
B17	VSS[051]	VSS[149]	T12
B2	VSS[052]	VSS[150]	T13
B20	VSS[053]	VSS[151]	T14
B22	VSS[054]	VSS[152]	T15
BB	VSS[055]	VSS[153]	T16
C24	VSS[056]	VSS[154]	T17
C27	VSS[057]	VSS[155]	T2
C6	VSS[058]	VSS[156]	T12
C6	VSS[059]	VSS[157]	U1
D12	VSS[060]	VSS[158]	U13
D15	VSS[061]	VSS[159]	U14
D18	VSS[062]	VSS[160]	U15
D2	VSS[063]	VSS[161]	U16
D4	VSS[064]	VSS[162]	U23
E21	VSS[065]	VSS[163]	U26
E24	VSS[066]	VSS[164]	U27
E4	VSS[067]	VSS[165]	U3
E9	VSS[068]	VSS[166]	U7
F15	VSS[069]	VSS[167]	U5
E23	VSS[070]	VSS[168]	V13
F28	VSS[071]	VSS[169]	V15
F29	VSS[072]	VSS[170]	V28
F7	VSS[073]	VSS[171]	V29
G1	VSS[074]	VSS[172]	V29
E2	VSS[075]	VSS[173]	V28
G10	VSS[076]	VSS[174]	V27
G13	VSS[077]	VSS[175]	Y28
G19	VSS[078]	VSS[176]	Y28
G23	VSS[079]	VSS[177]	Y4
G25	VSS[080]	VSS[178]	Y4
G26	VSS[081]	VSS[179]	AB23
G27	VSS[082]	VSS[180]	AB5
H25	VSS[083]	VSS[181]	AB6
H28	VSS[084]	VSS[182]	AD5
H29	VSS[085]	VSS[183]	U4
H3	VSS[086]	VSS[184]	W24
H6	VSS[087]		
J1	VSS[088]	VSS_NCTF[01]	A1
J25	VSS[089]	VSS_NCTF[02]	A2
J26	VSS[090]	VSS_NCTF[03]	A28
J27	VSS[091]	VSS_NCTF[04]	A29
J4	VSS[092]	VSS_NCTF[05]	AH1
J5	VSS[093]	VSS_NCTF[06]	AH29
K23	VSS[094]	VSS_NCTF[07]	AJ1
K28	VSS[095]	VSS_NCTF[08]	AJ2
K29	VSS[096]	VSS_NCTF[09]	AJ28
K3	VSS[097]	VSS_NCTF[10]	AJ29
K6	VSS[098]	VSS_NCTF[11]	B1
		VSS_NCTF[12]	B29

ICH8M REV 1.0_0

ICH8M REV 1.0_0

0901 Eric_modify LAN power circuit to no used

1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Wolding resins only from the business Partners that Sony approves as Green Partners.

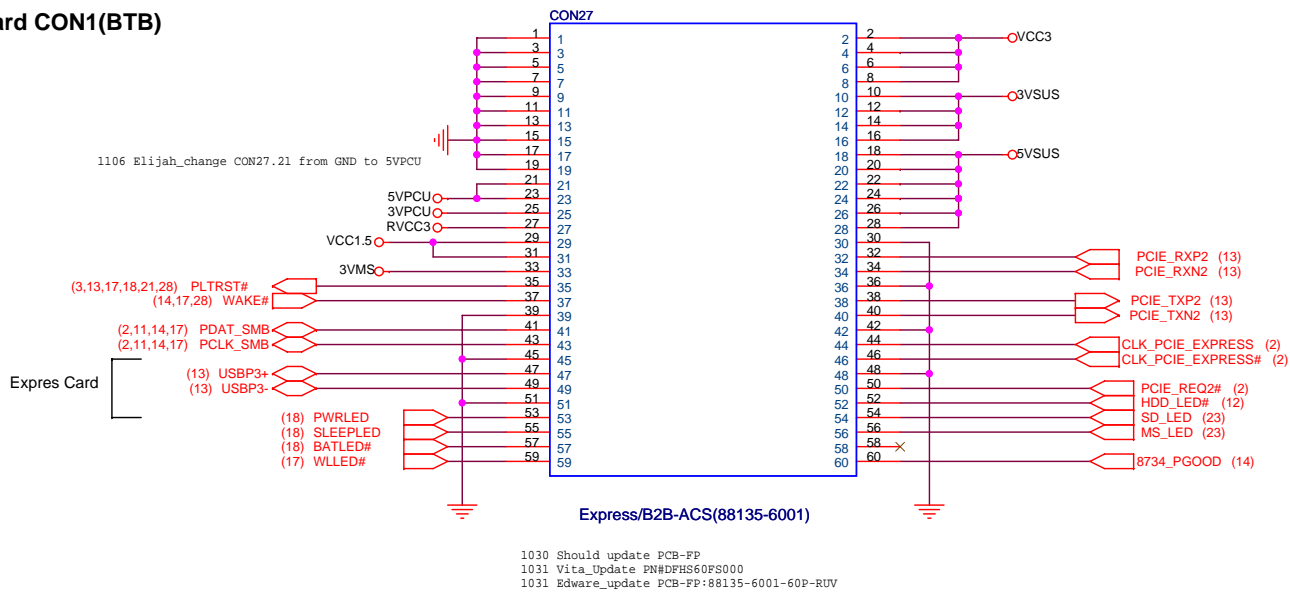
QUANTA COMPUTER

Title: **ICH8-M Power 4 o 4**

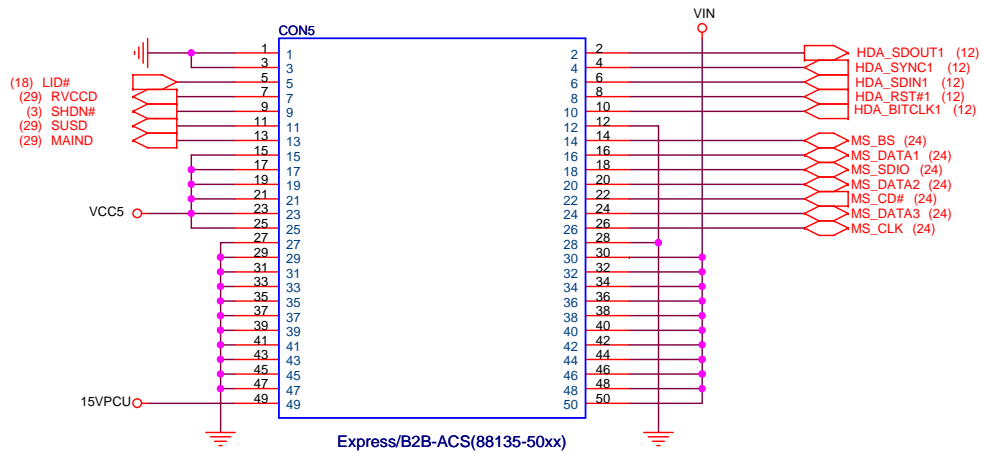
Size	Document Number	Rev
	GD1 Main Board	1A

Date: Tuesday, November 14, 2006 Sheet 15 of 35

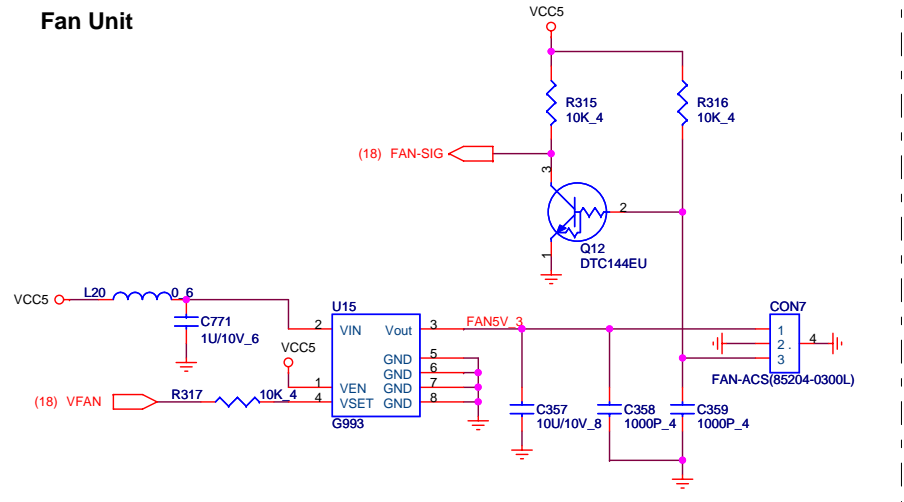
Express Board CON1(BTB)



Express Board CON2(BTB)



Fan Unit



Title			Rev
Express Card			1A
Size	Document Number	GD1 Main Board	
B			
Date:	Tuesday, November 14, 2006	Sheet	16 of 35

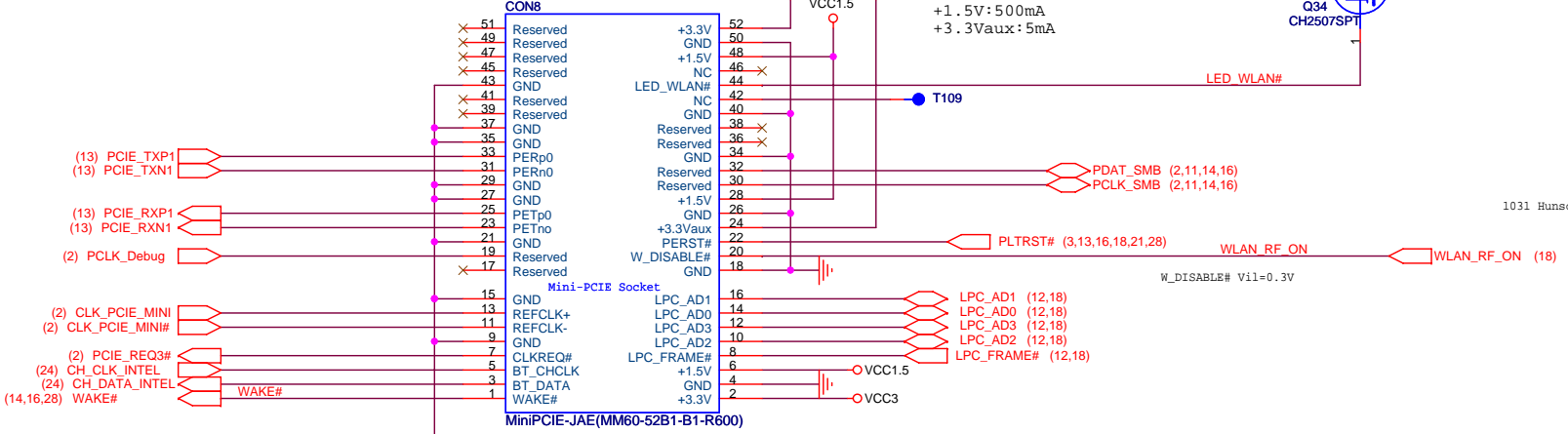
1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

LED_GP :LED WLEN LINK
Output Current : 7mA
Blink rate : 1 flash per every 3 sec.

WLSW:
Low : disable the radio.
High : Enable the radio.

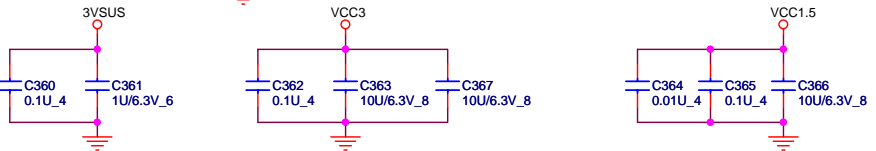
LED_WLAN# MAX sink current=16mA
(recommend<=14mA)
Drive in LED/B
+3.3V:1A
+1.5V:500mA
+3.3Vaux:5mA

Mini PCI-E Card FOR WL



1031 Hunson_Must ADD NMOS,R LED in Express/B

W_DISABLE# Vil=0.3V



QUANTA COMPUTER

Title: **MINIPCIE / MDC**

Size B Document Number: **GD1 Main Board** Rev 1A

Date: **Wednesday, November 15, 2006** Sheet 17 of 35

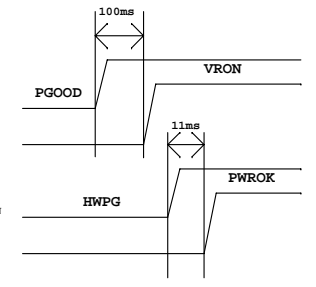
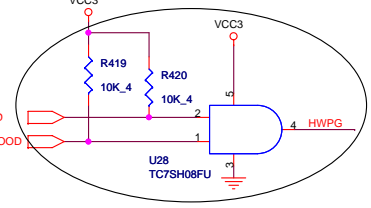
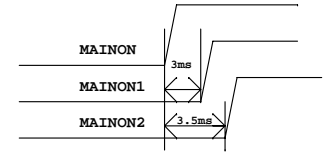
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

I/O Address		
BADDR1-0	Index	Data
1 0	2E	2F
1 1	4E	4F
0 0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1	
0 1	XOR-TREE TEST	

DOCK_RST# = BADDR0
 DK_BAT_PWRN: BADDR1
 BT_PEN# : SHBM(If = 0 Enable share host BIOS memory)

PWROK must be after HWPG at least 10ms
 VRON must be after PGOOD at least 99ms

MAINON <-- 3ms --> MAION1
 MAINON <-- 3.5ms --> MAION2

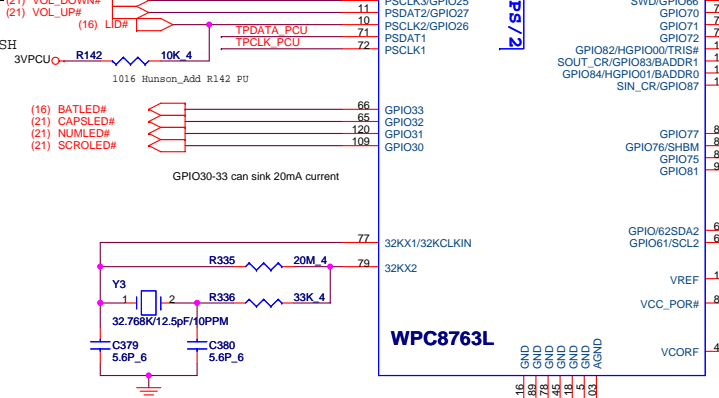
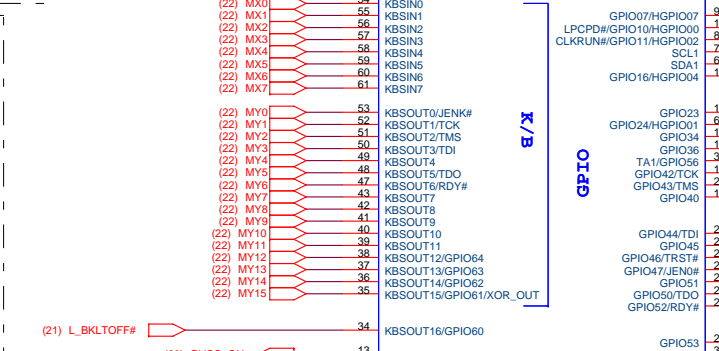
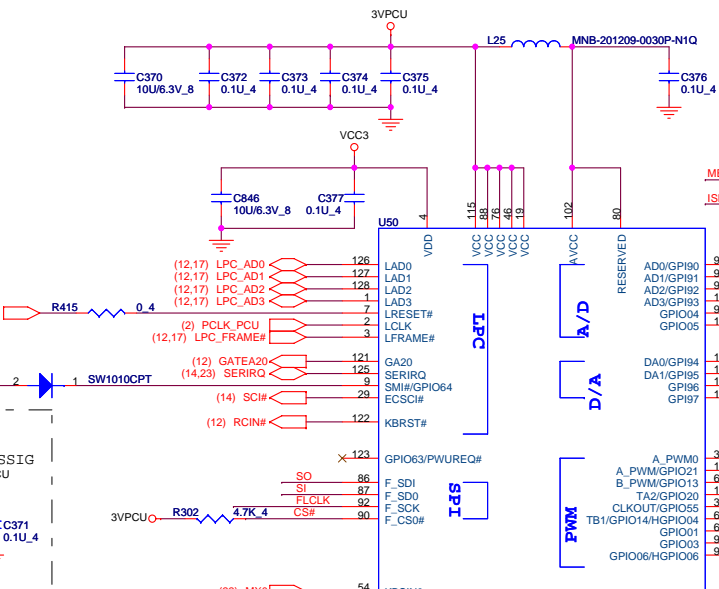
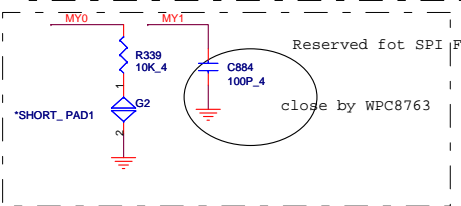
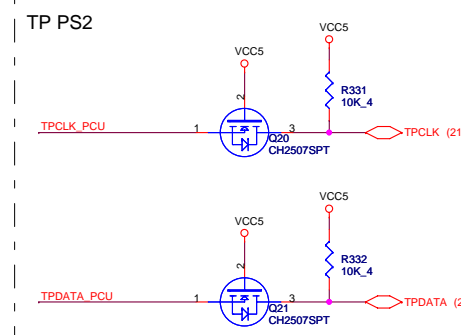
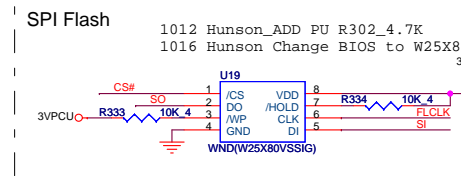
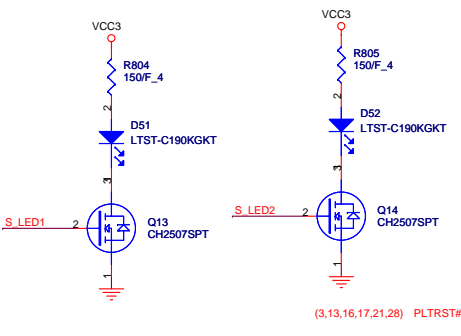


0901 Hunson_volmute is low active

0831 Eric_BT_PEN change to high active

1013 Hunson Add Batt SCK&SDA

1107 Hunson_FAE recommend PD 10K on EVT version



Change to 5.6P(Tuning)

JTAG SELECT CONFIGURATION			
JEN0(PIN24)	JENK(PIN53)	Functionality of PINS (17,20,21,23,25,27)	Functionality of PINS (47,48,50,51,52)
NC	NC	GPIO	KEYBOARD OUTPUT
10K PD	NC	JTAG Signal	KEYBOARD OUTPUT
NC	10K PD	GPIO	JTAG Signal
10K PD	10K PD		Illegal Strap combination

1016 Hunson_Change EC to WPC8763L

1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

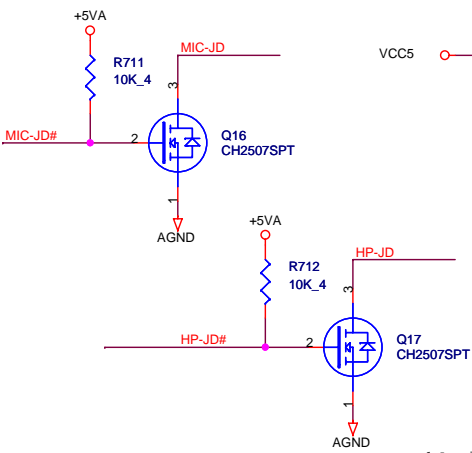
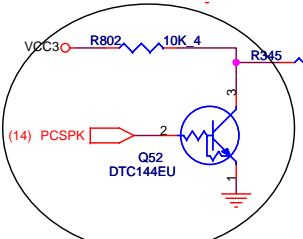
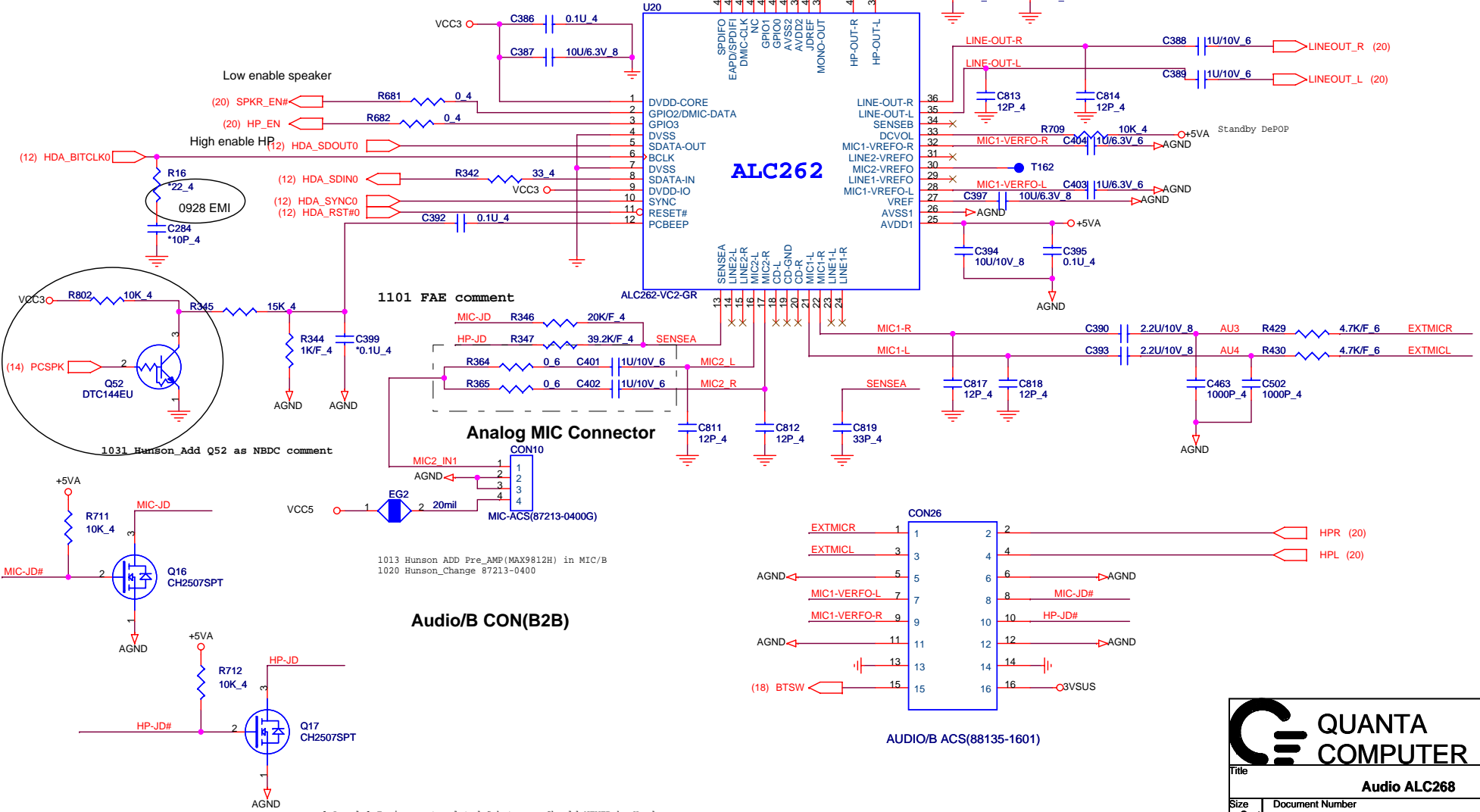
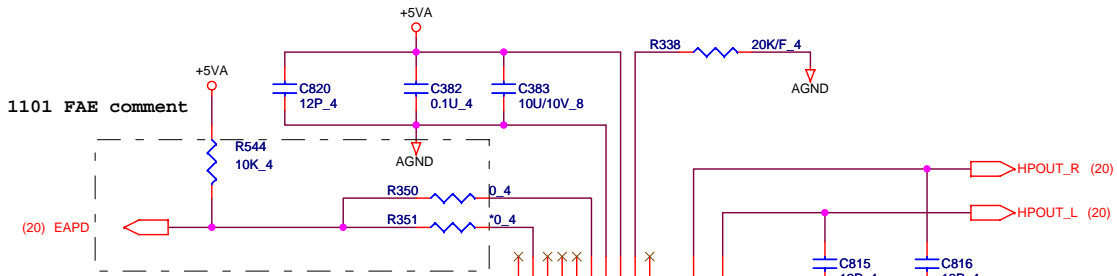
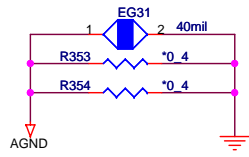
QUANTA COMPUTER

Title: **WPC8763L & SPI FLASH**

Size: Document Number: **GD1 Main Board** Rev 1A

Date: Tuesday, November 14, 2006 Sheet 18 of 35

Audio decoupling



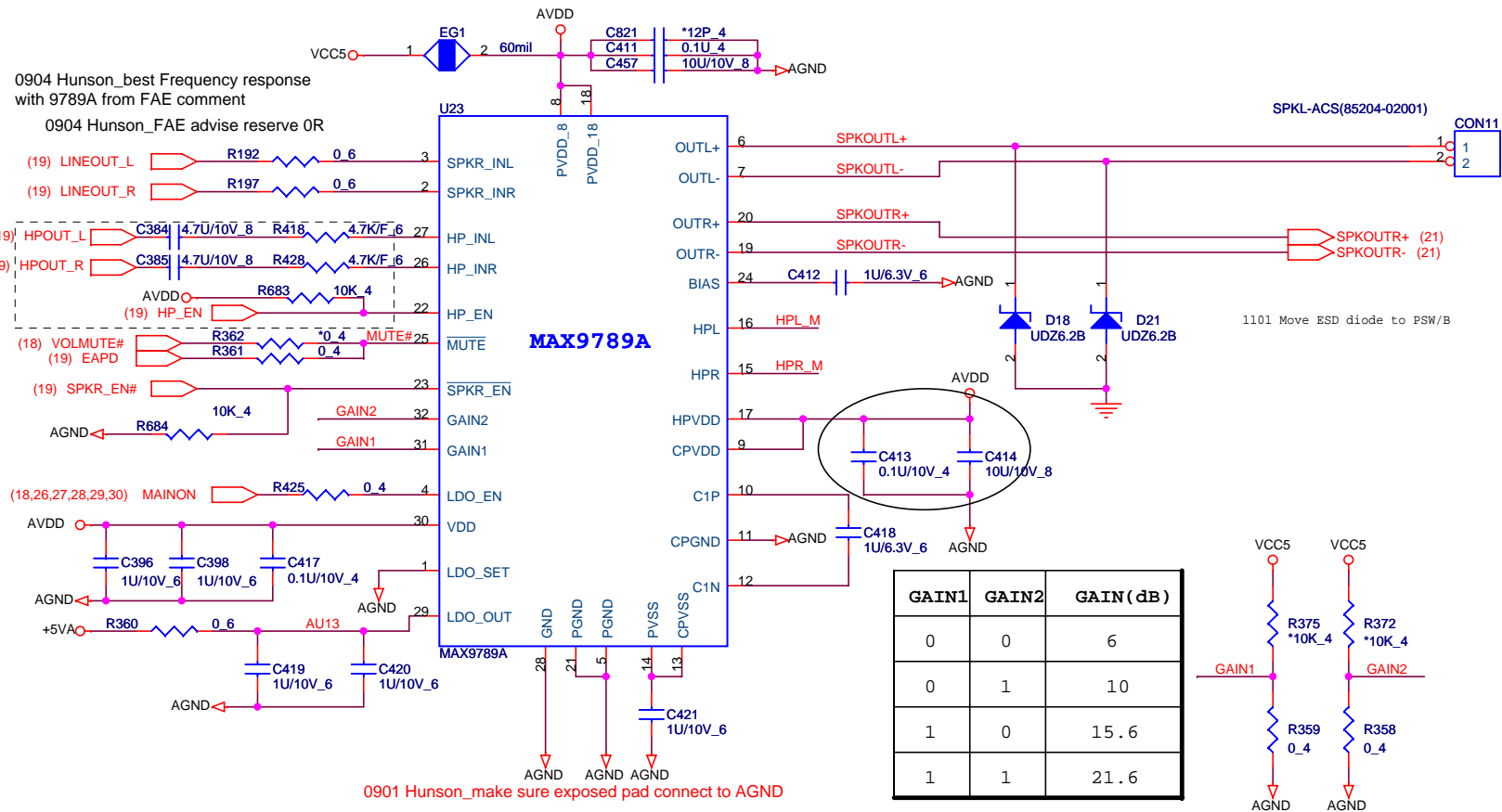
1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

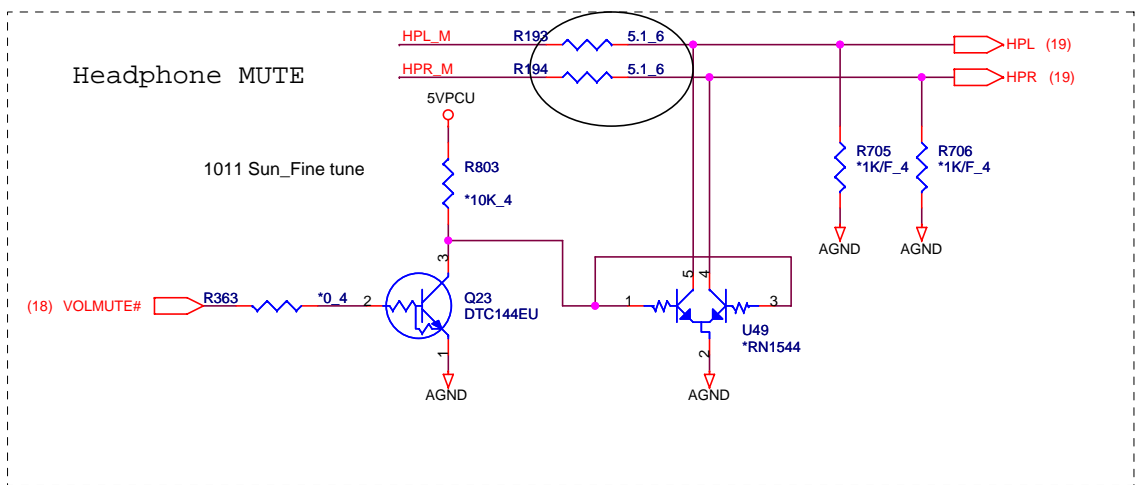
Title: **Audio ALC268**

Size: Custom | Document Number: **GD1 Main Board** | Rev: 1A

Date: Tuesday, November 14, 2006 | Sheet: 19 of 35



0901 Hunson_make sure exposed pad connect to AGND



1.Level 1 Environment-related Substances Should NEVER be Used.
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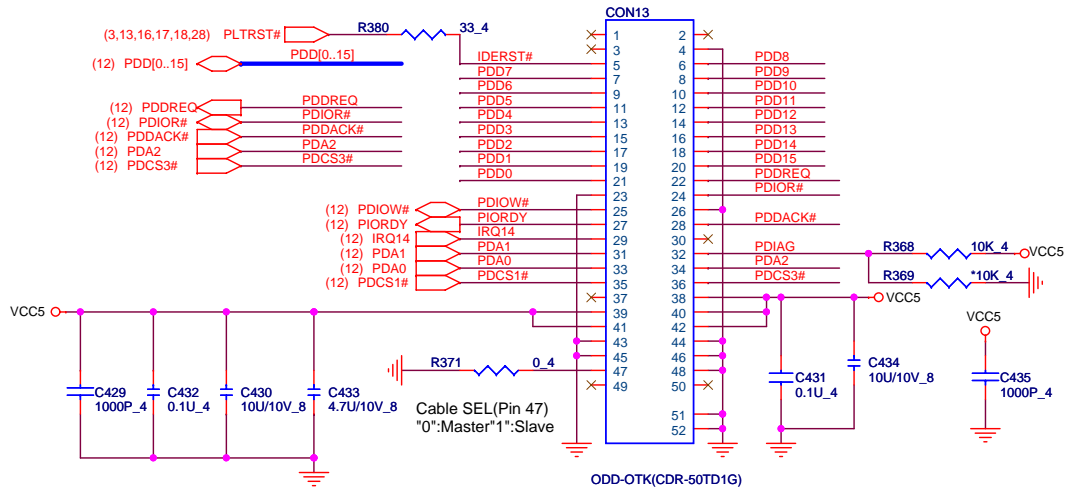
QUANTA COMPUTER

Title: **Audio AMP. & Speaker**

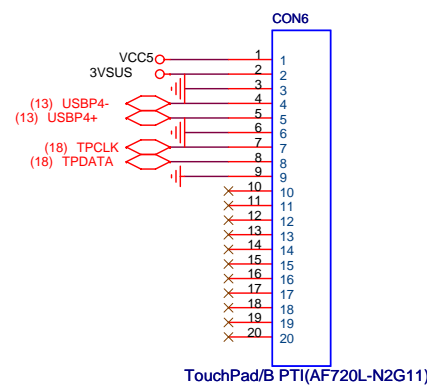
Size: Custom | Document Number: **GD1 Main Board** | Rev: 1A

Date: Tuesday, November 14, 2006 | Sheet: 20 of 35

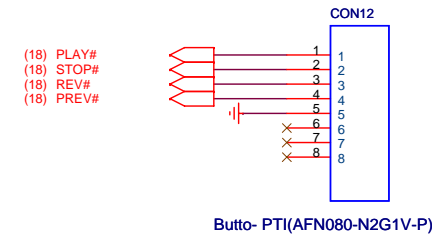
ODD CONNECTOR



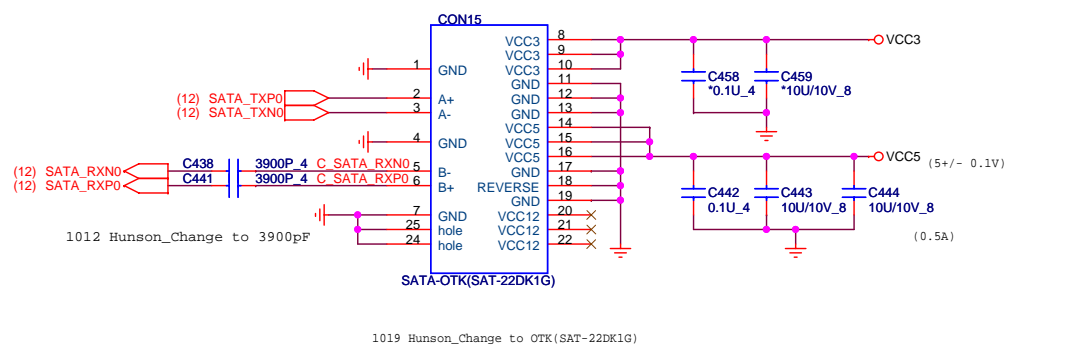
TouchPAD Board CON(FFC)



Button CON(FFC)

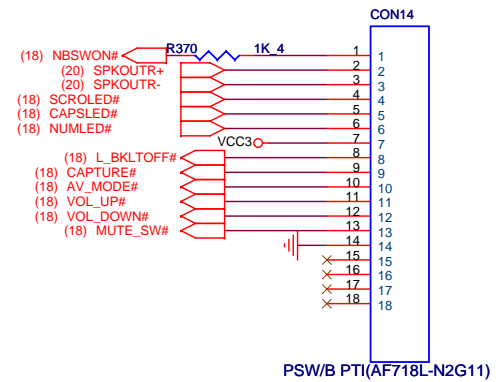


HDD CONNECTOR



PSW Board CON(FFC)

1031 Hunson_update PCB-PP



QUANTA COMPUTER

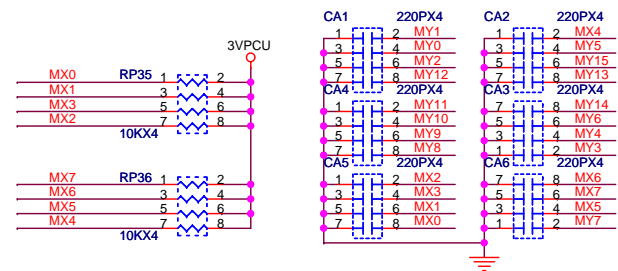
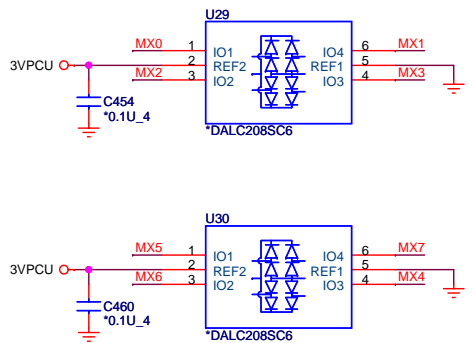
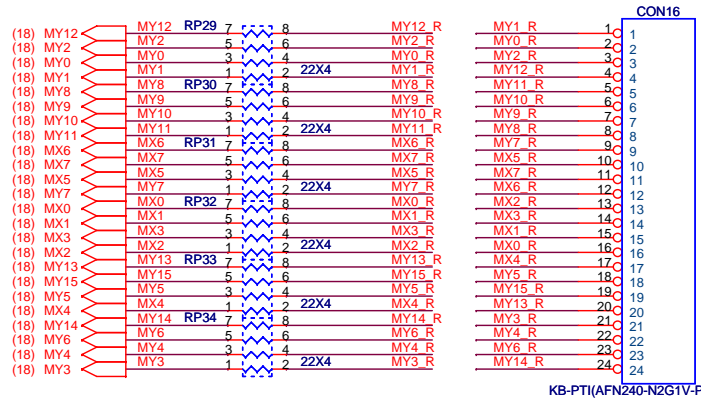
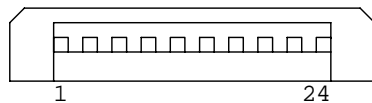
Title: **HDD/ODD/PW CON**

Size B Document Number: **GD1 Main Board** Rev 1A

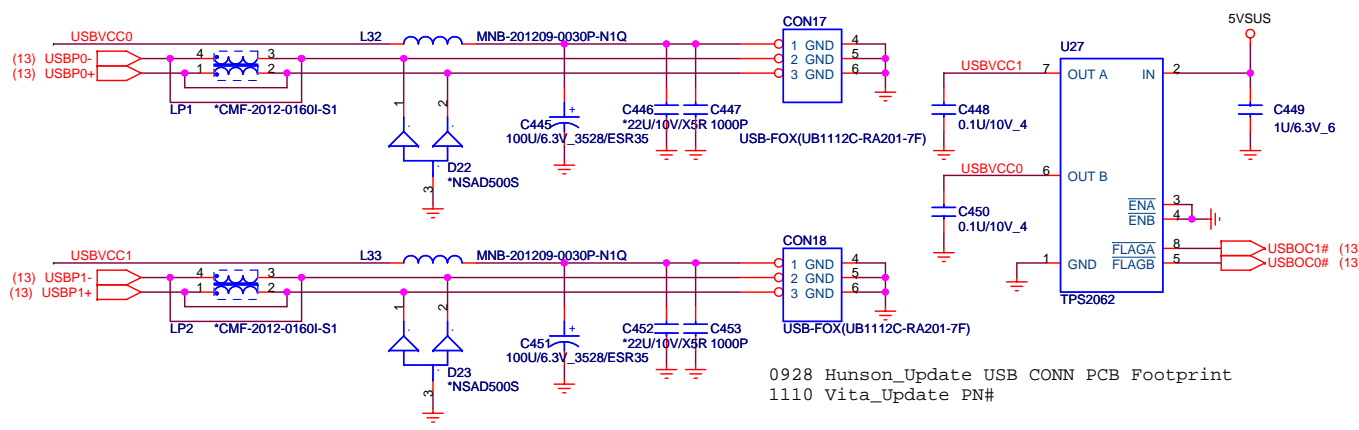
Date: Wednesday, November 15, 2006 Sheet 21 of 35

1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

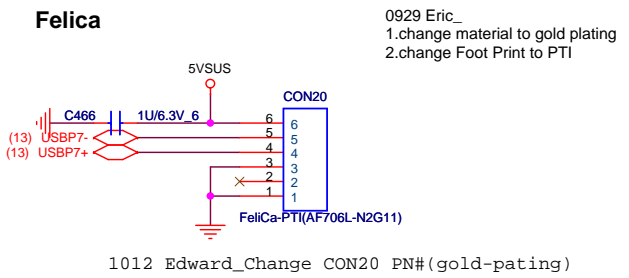
Keyboard



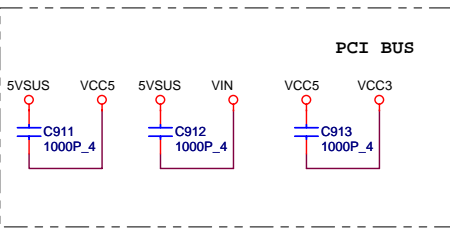
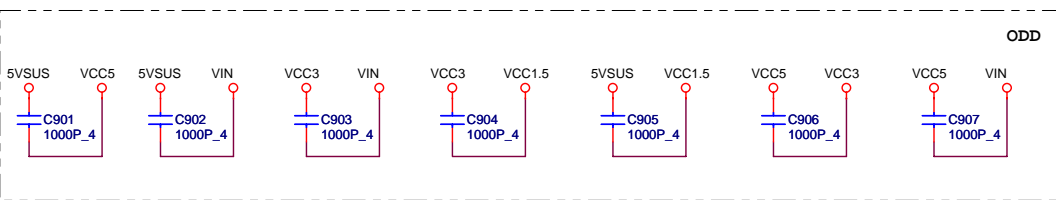
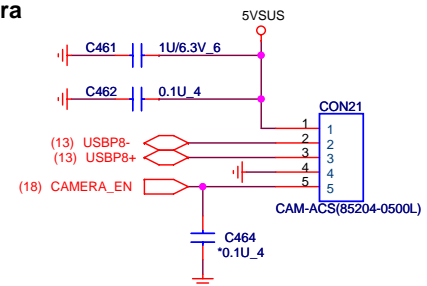
USB Port x 2



Felica



USB Camera



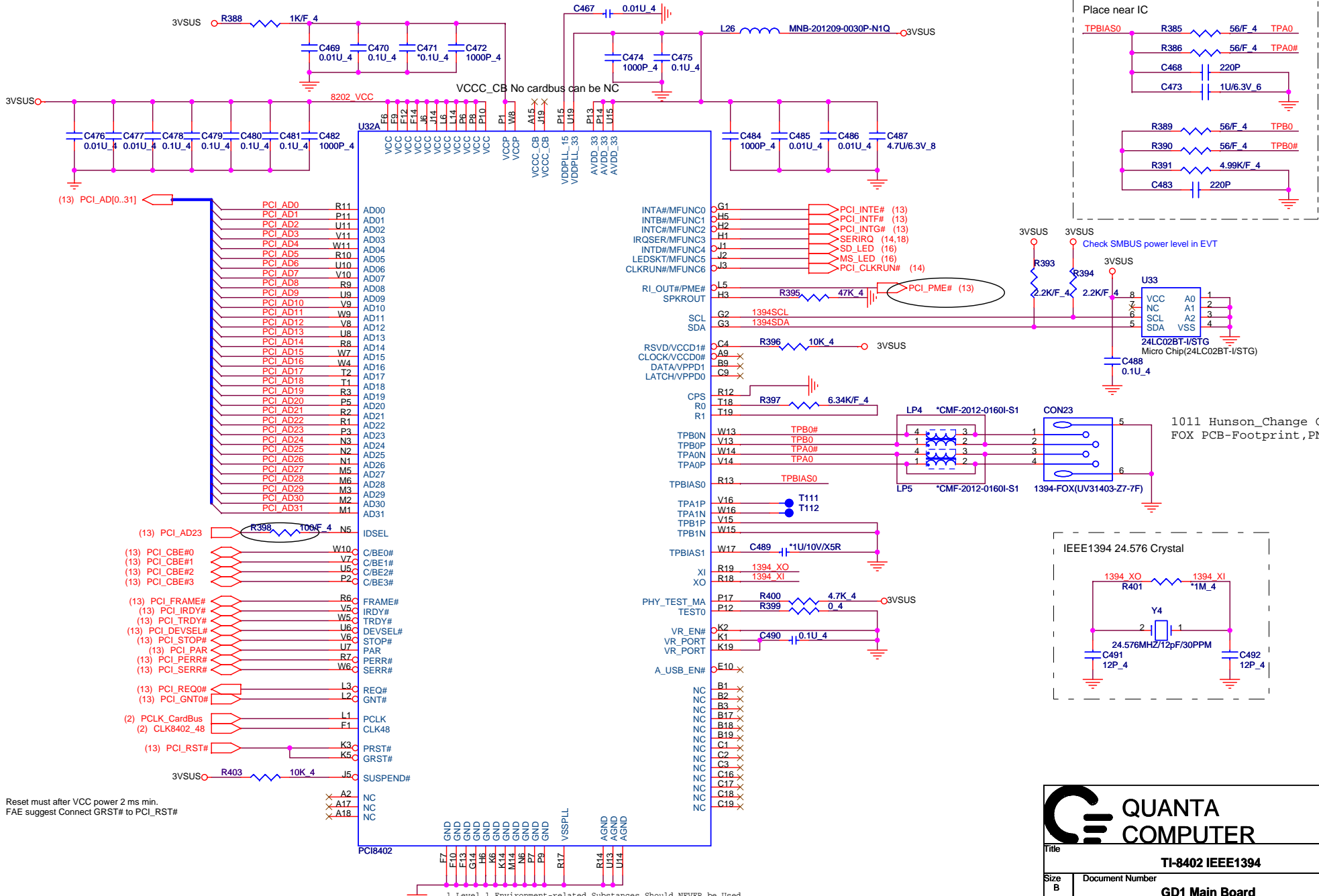
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: **K/B ,USB Device**

Size: **B** Document Number: **GD1 Main Board** Rev: **1A**

Date: **Wednesday, November 15, 2006** Sheet: **22** of **35**



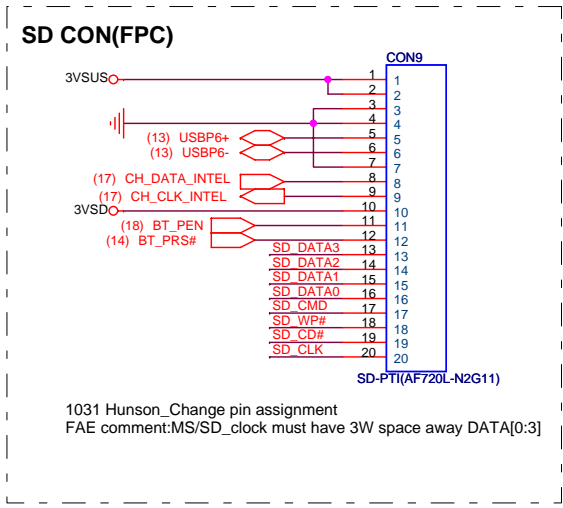
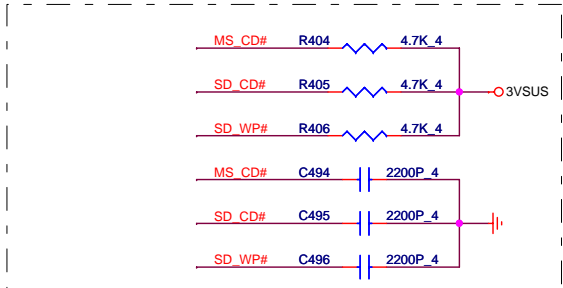
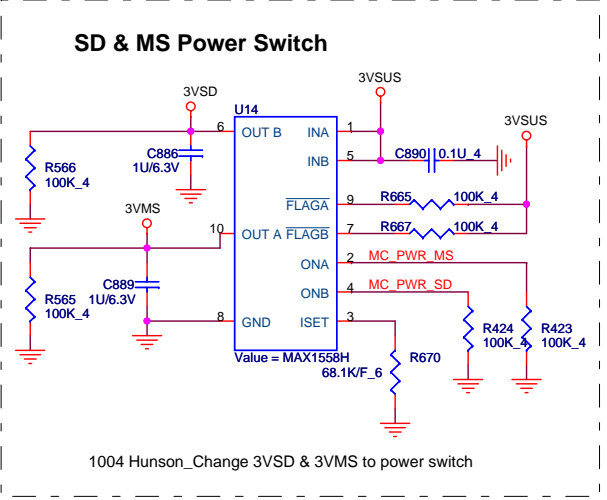
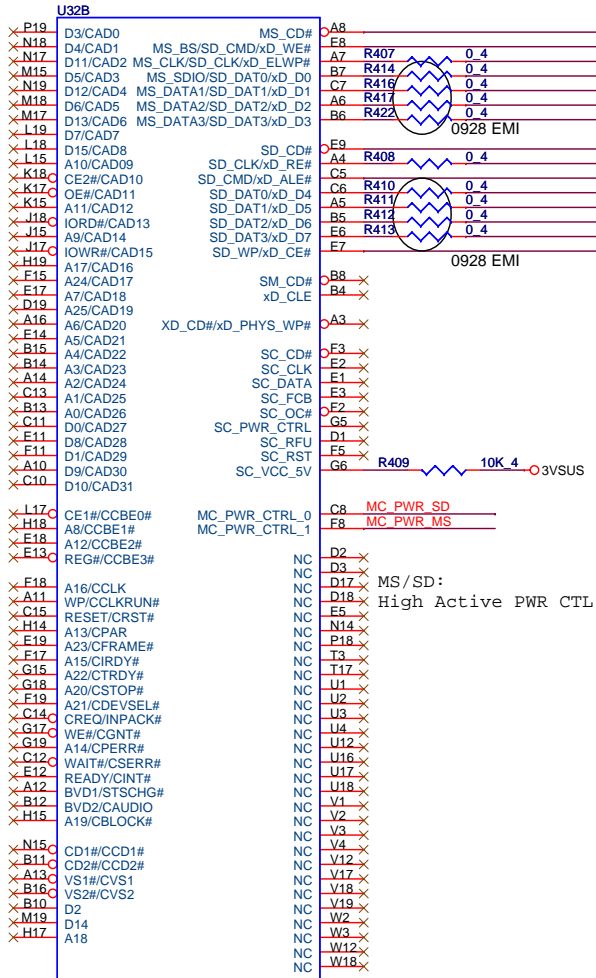
Reset must after VCC power 2 ms min.
FAE suggest Connect GRST# to PCI_RST#

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

**QUANTA
COMPUTER**

Title: **TI-8402 IEEE1394**

Size B	Document Number	Rev 1A
GD1 Main Board		
Date:	Wednesday, November 15, 2006	Sheet 23 of 35



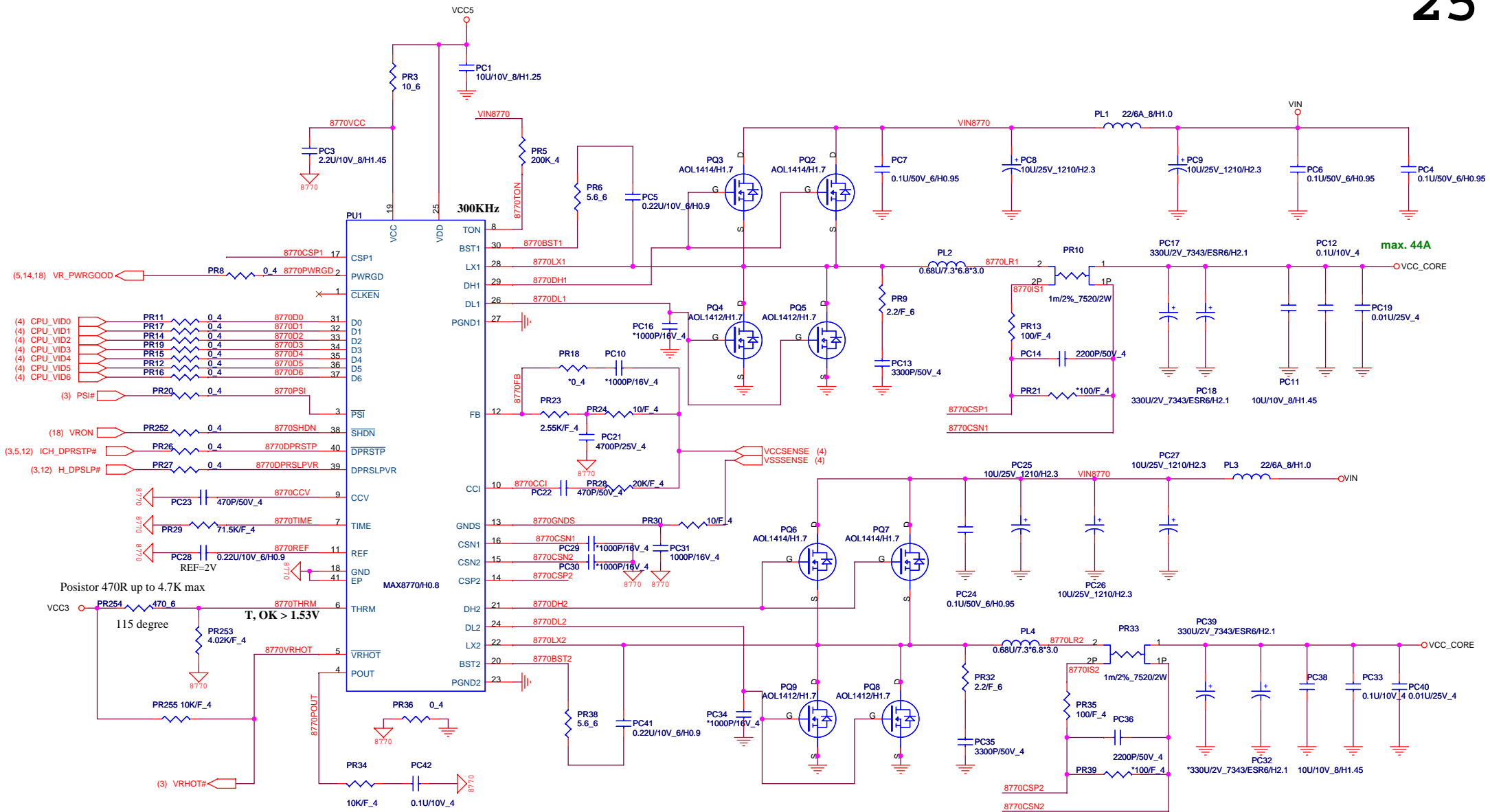
QUANTA COMPUTER

Title: **TI-8402 MS & SD**

Size B Document Number: **GD1 Main Board** Rev 1A

Date: Wednesday, November 15, 2006 Sheet 24 of 35

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



In progress

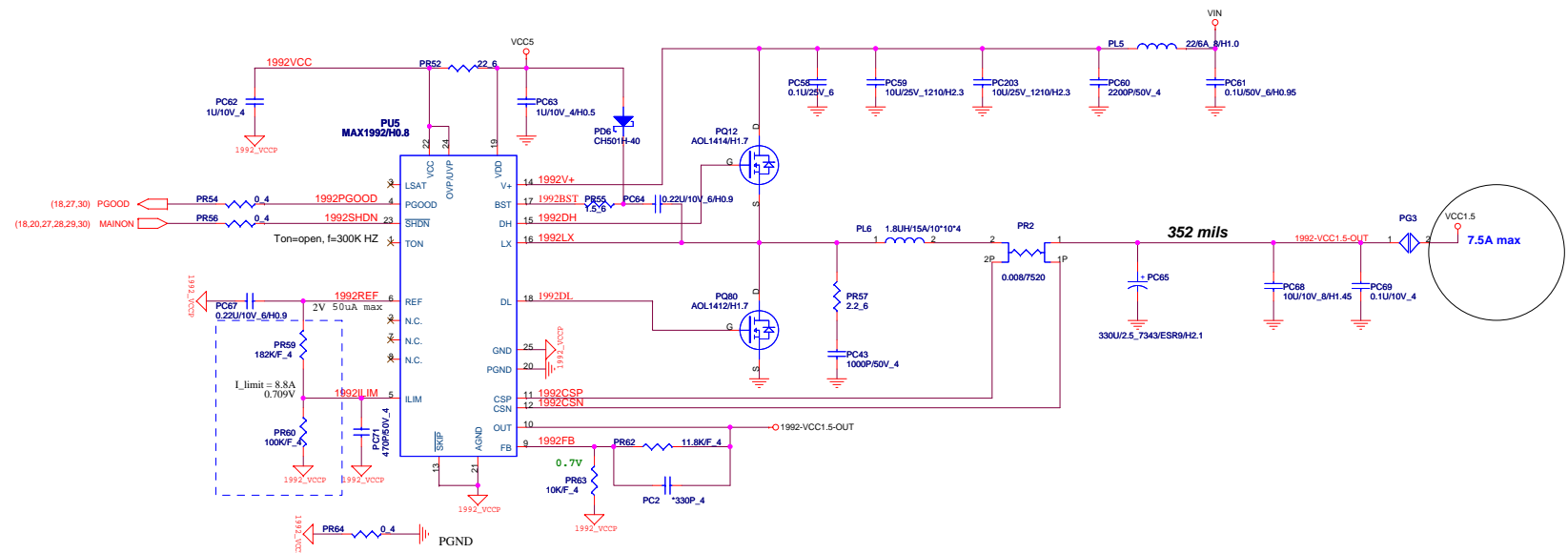
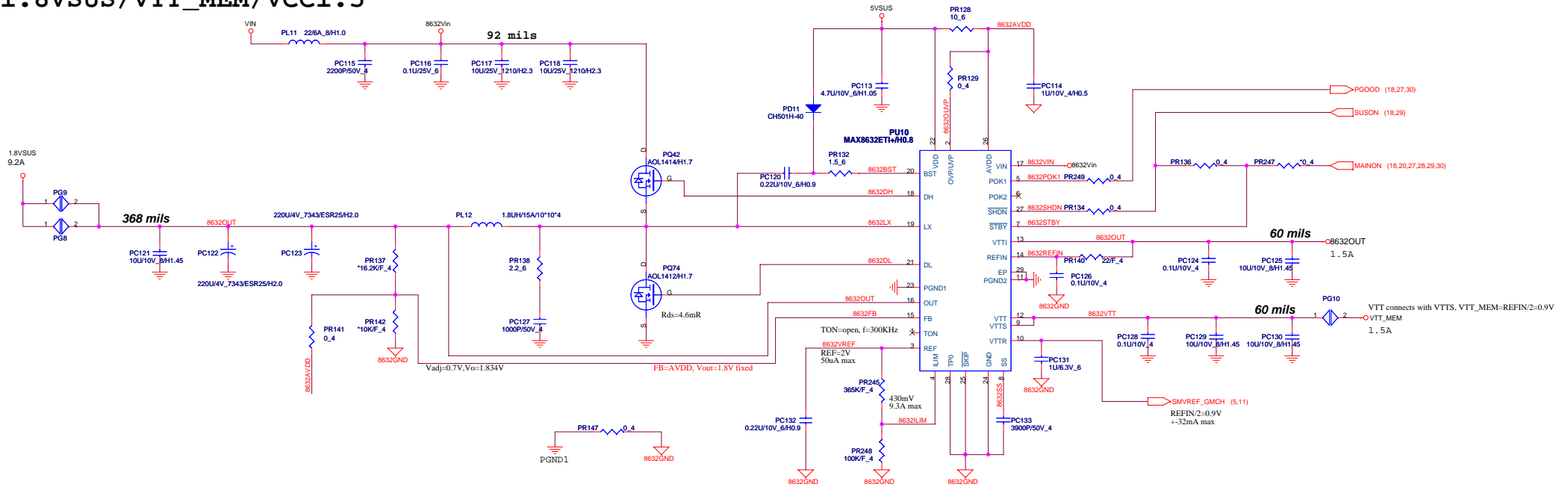
QUANTA COMPUTER

Title: **CPU CORE (MAX8770)**

Size: Custom Document Number: **RD3 Main Board** Rev: 1A

Date: Tuesday, November 14, 2006 Sheet 25 of 35

1. Level 1 Environment-related Substances should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



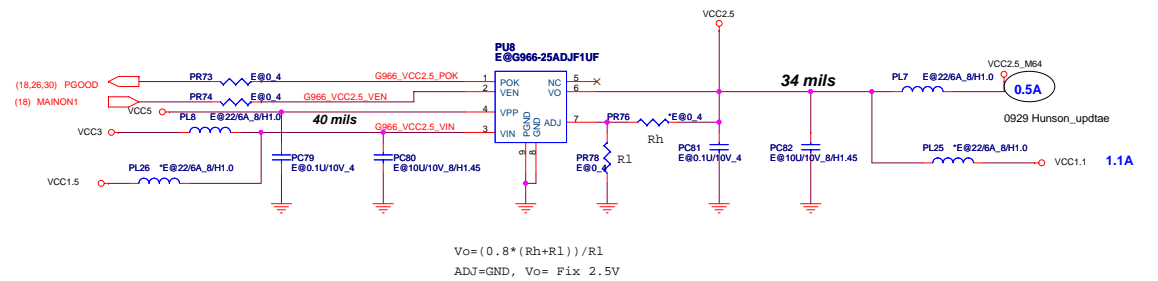
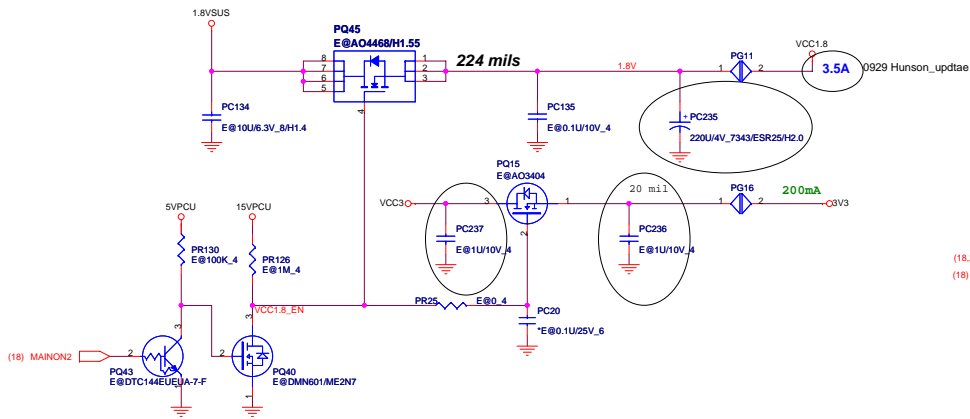
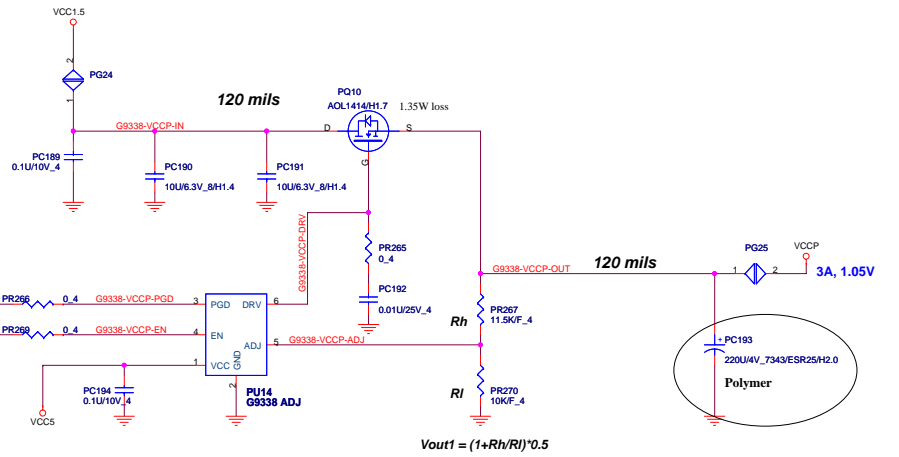
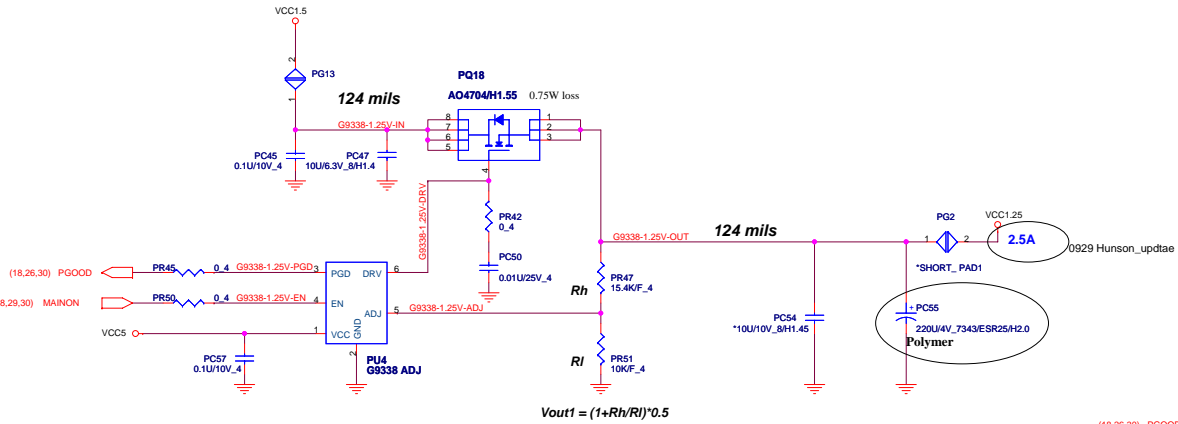
QUANTA COMPUTER

Title: **VCCP & VCC1.5 & VCC1.25**

Size: Document Number: **RD3 Main Board** Rev: 1A

Date: Tuesday, November 14, 2006 Sheet: 26 of 35

1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



In progress

QUANTA COMPUTER

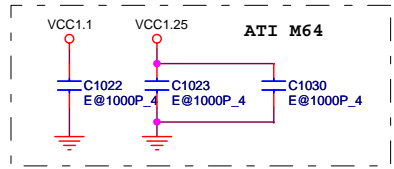
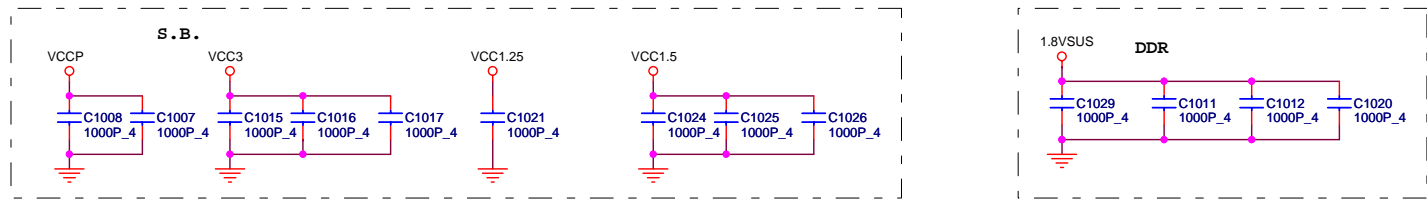
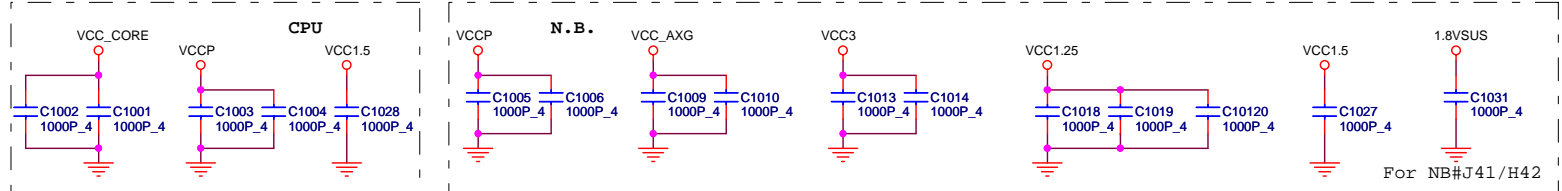
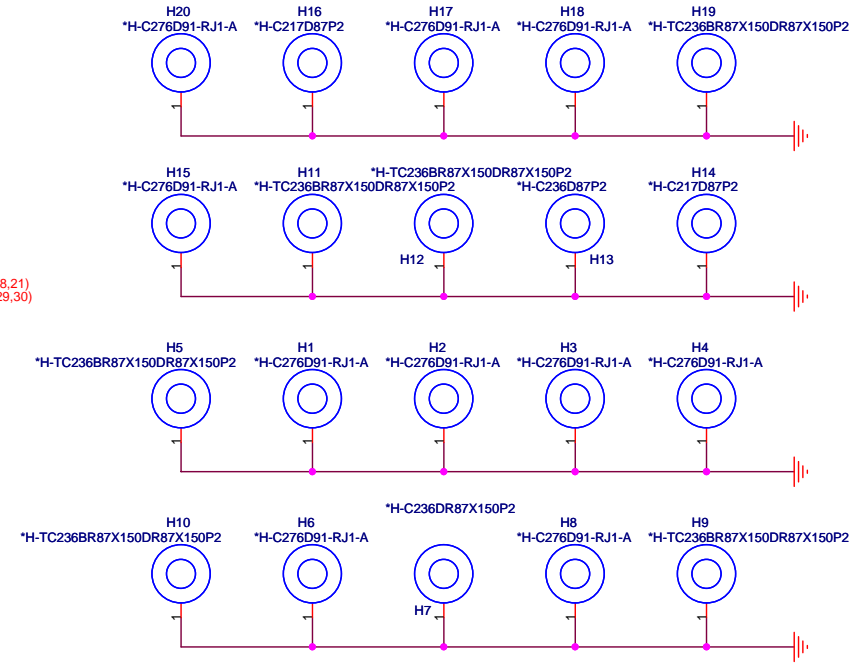
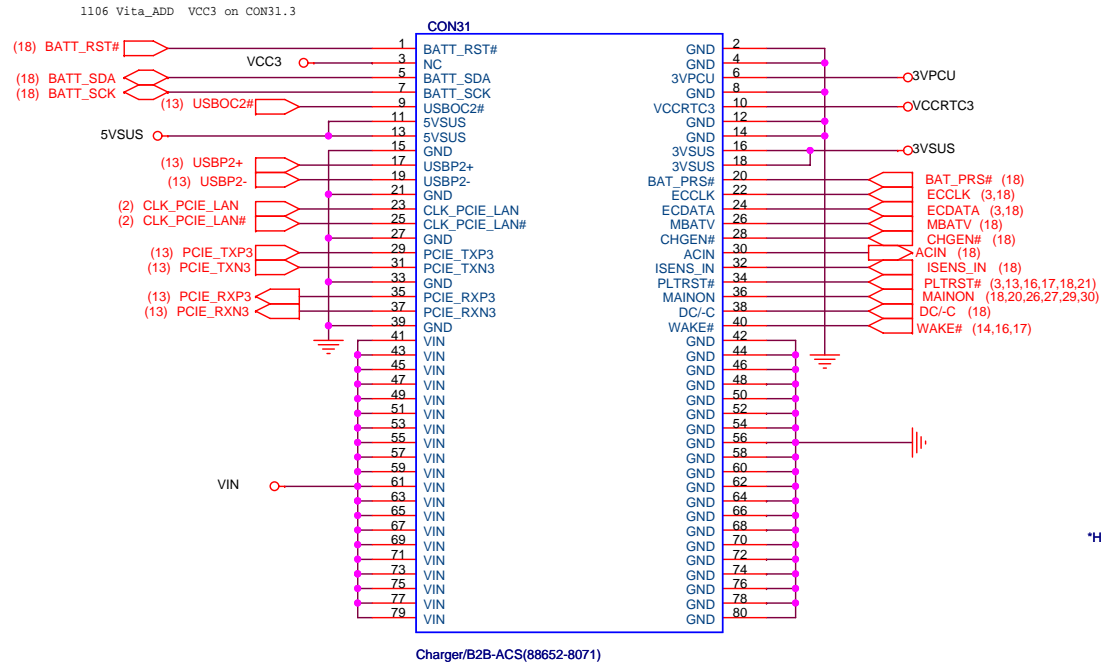
File: VCCP & VCC1.5 & VCC1.25

Size: Document Number: RD3 Main Board Rev 1A

Date: Tuesday, November 14, 2006 Sheet 27 of 35

1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

1027 Vita modify pin definition



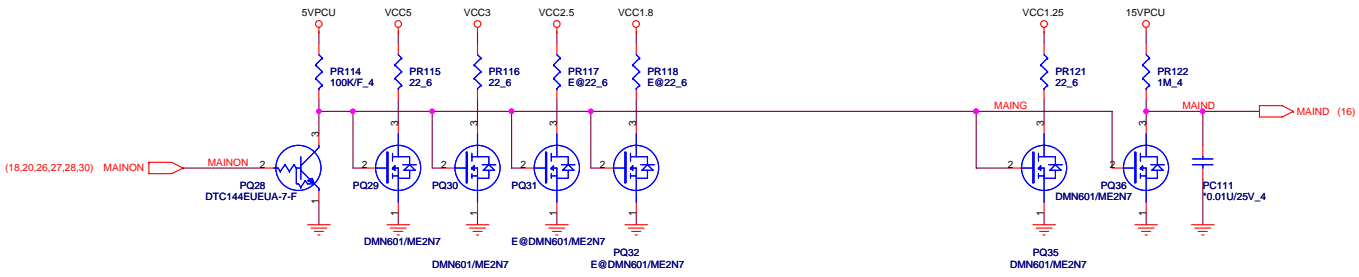
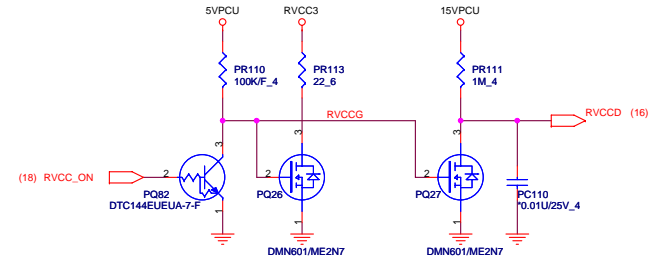
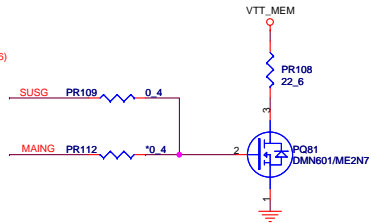
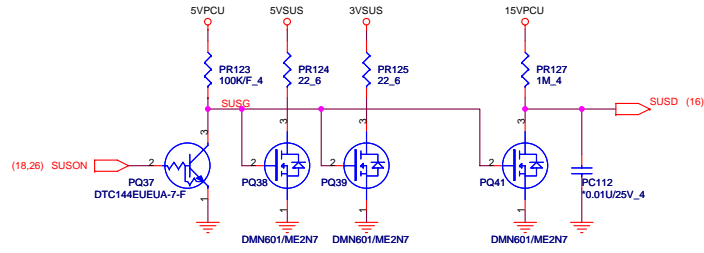
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: **Power Charger & LAN CON**

Size B Document Number: **GD1 Main Board** Rev 1A

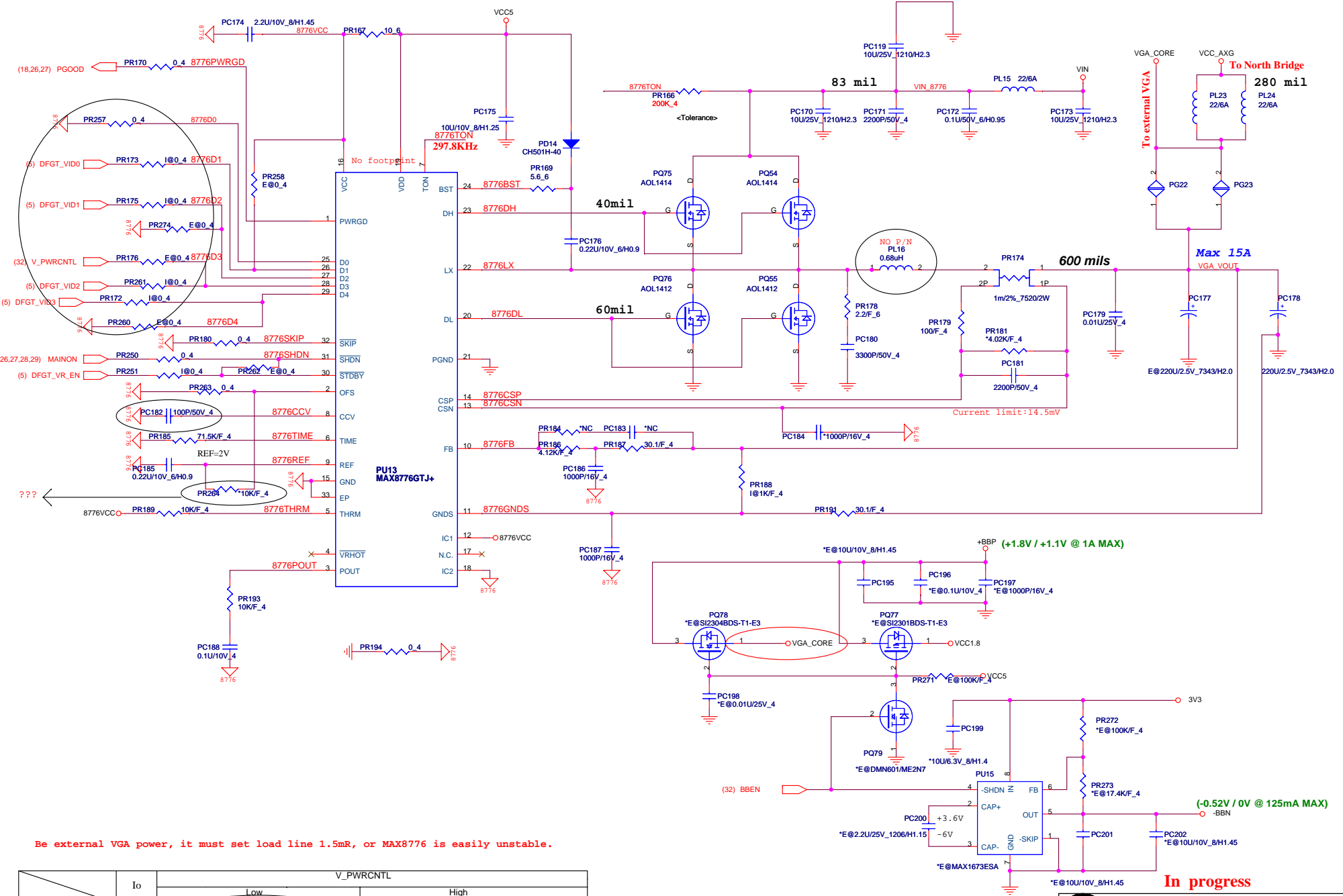
Date: Wednesday, November 15, 2006 Sheet 28 of 35



1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase Ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

In progress

		QUANTA COMPUTER	
		3VPCU & 5VPCU	
Size	Document Number	RD3 Main Board	
Custom			
Date: Wednesday, November 15, 2006	Sheet	29	of 35
			Rev 1A



Be external VGA power, it must set load line 1.5mR, or MAX8776 is easily unstable.

	Io	V_PWRCNTL	
		Low	High
Ext :ATI M71-M74	15A	1.2V (D4,D3,D2,D1,D0=0,0,1,0)	1.0V (D4,D3,D2,D1,D0=0,1,0,1,0)
Int :North Bridge	7.7A	VID	

1.Level 1 Environment-related Substances should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: **VGA CORE**

Size: Document Number: **RD3 Main Board** Rev: 1A

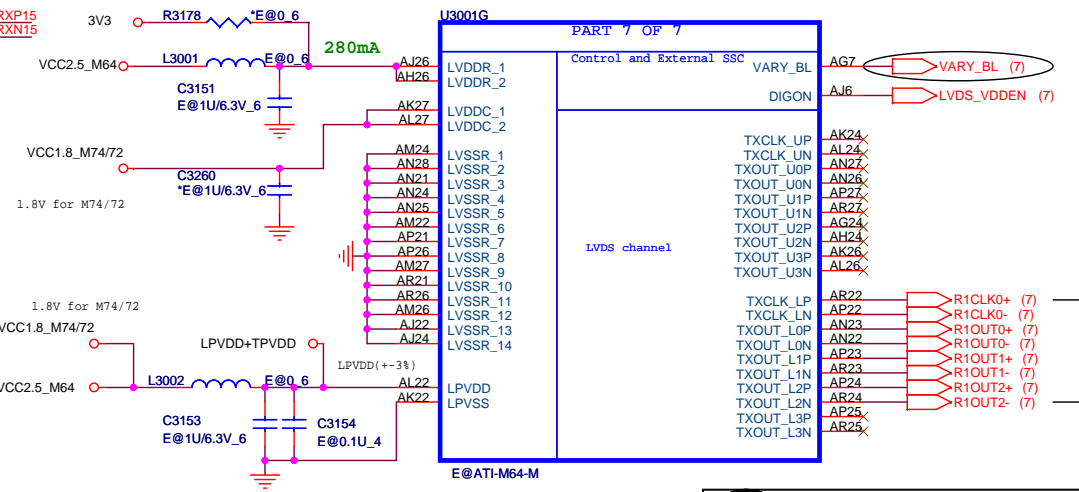
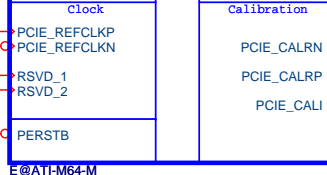
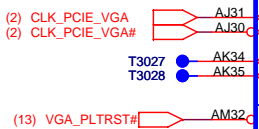
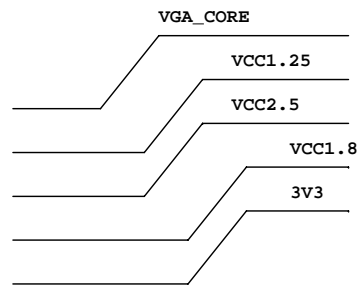
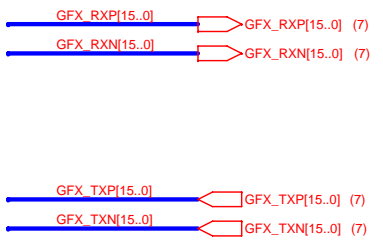
Date: Tuesday, November 14, 2006 Sheet: 30 of 35

In progress

U3001A PART 1 OF 7

GFX_TXP0	AK33	PCIE_RX0P	PCIE_TX0P	AG31	C GFX_RXP0	C3000	E@0.1U_4	GFX_RXP0
GFX_TXN0	AJ33	PCIE_RX0N	PCIE_TX0N	AG30	C GFX_RXN0	C3001	E@0.1U_4	GFX_RXN0
GFX_TXP1	AJ35	PCIE_RX1P	PCIE_TX1P	AF31	C GFX_RXP1	C3002	E@0.1U_4	GFX_RXP1
GFX_TXN1	AJ34	PCIE_RX1N	PCIE_TX1N	AF30	C GFX_RXN1	C3003	E@0.1U_4	GFX_RXN1
GFX_TXP2	AH35	PCIE_RX2P	PCIE_TX2P	AF28	C GFX_RXP2	C3004	E@0.1U_4	GFX_RXP2
GFX_TXN2	AH34	PCIE_RX2N	PCIE_TX2N	AF27	C GFX_RXN2	C3005	E@0.1U_4	GFX_RXN2
GFX_TXP3	AG35	PCIE_RX3P	PCIE_TX3P	AD31	C GFX_RXP3	C3006	E@0.1U_4	GFX_RXP3
GFX_TXN3	AG34	PCIE_RX3N	PCIE_TX3N	AD30	C GFX_RXN3	C3007	E@0.1U_4	GFX_RXN3
GFX_TXP4	AF33	PCIE_RX4P	PCIE_TX4P	AD28	C GFX_RXP4	C3008	E@0.1U_4	GFX_RXP4
GFX_TXN4	AE33	PCIE_RX4N	PCIE_TX4N	AD27	C GFX_RXN4	C3009	E@0.1U_4	GFX_RXN4
GFX_TXP5	AE35	PCIE_RX5P	PCIE_TX5P	AB31	C GFX_RXP5	C3010	E@0.1U_4	GFX_RXP5
GFX_TXN5	AE34	PCIE_RX5N	PCIE_TX5N	AB30	C GFX_RXN5	C3011	E@0.1U_4	GFX_RXN5
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GFX_TXN12	U33	PCIE_RX12N	PCIE_TX12N	V27	C GFX_RXN12	C3025	E@0.1U_4	GFX_RXN12
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GFX_TXN14	T34	PCIE_RX14N	PCIE_TX14N	U27	C GFX_RXN14	C3029	E@0.1U_4	GFX_RXN14
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PCI - EXPRESS INTERFACE

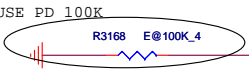
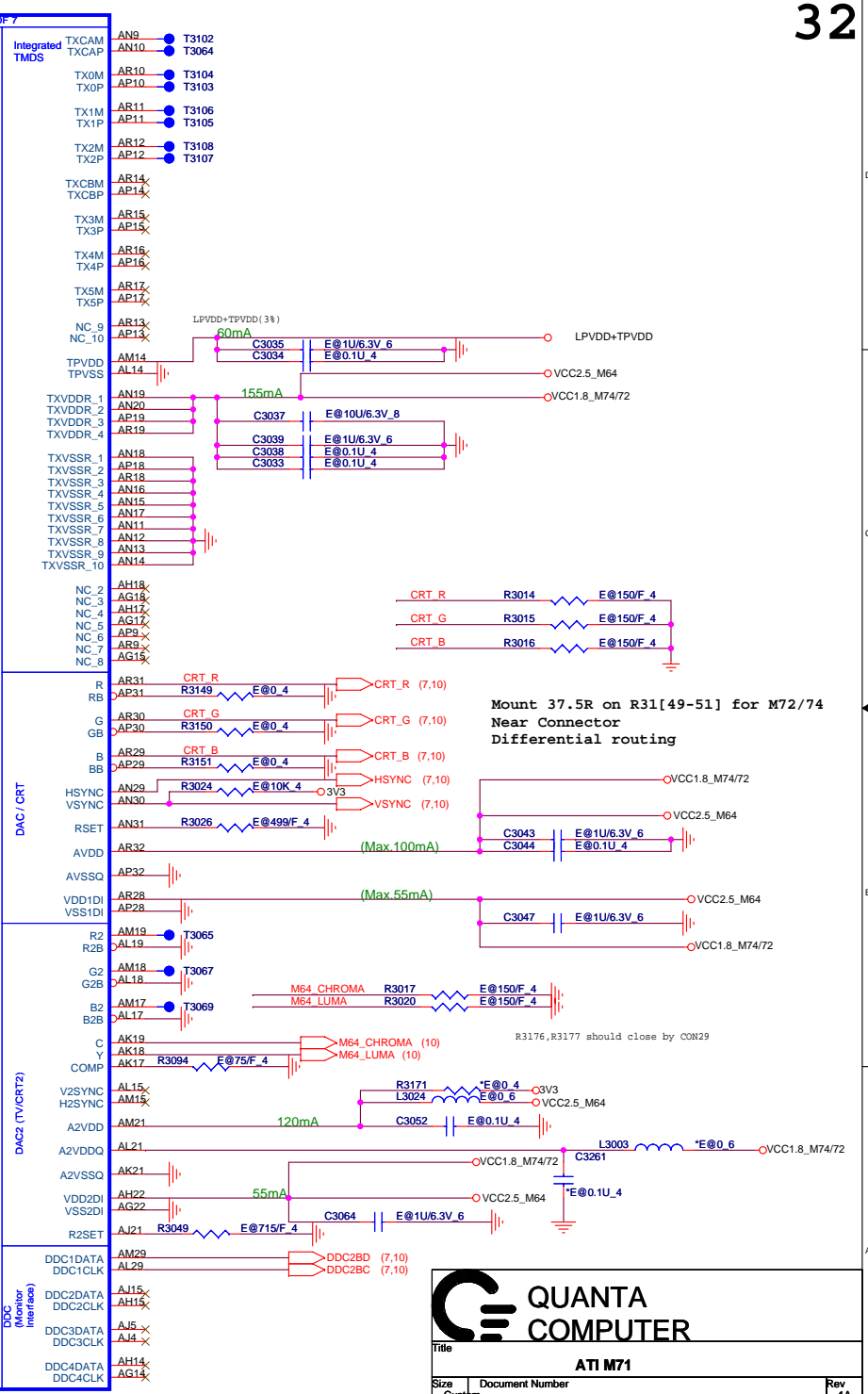
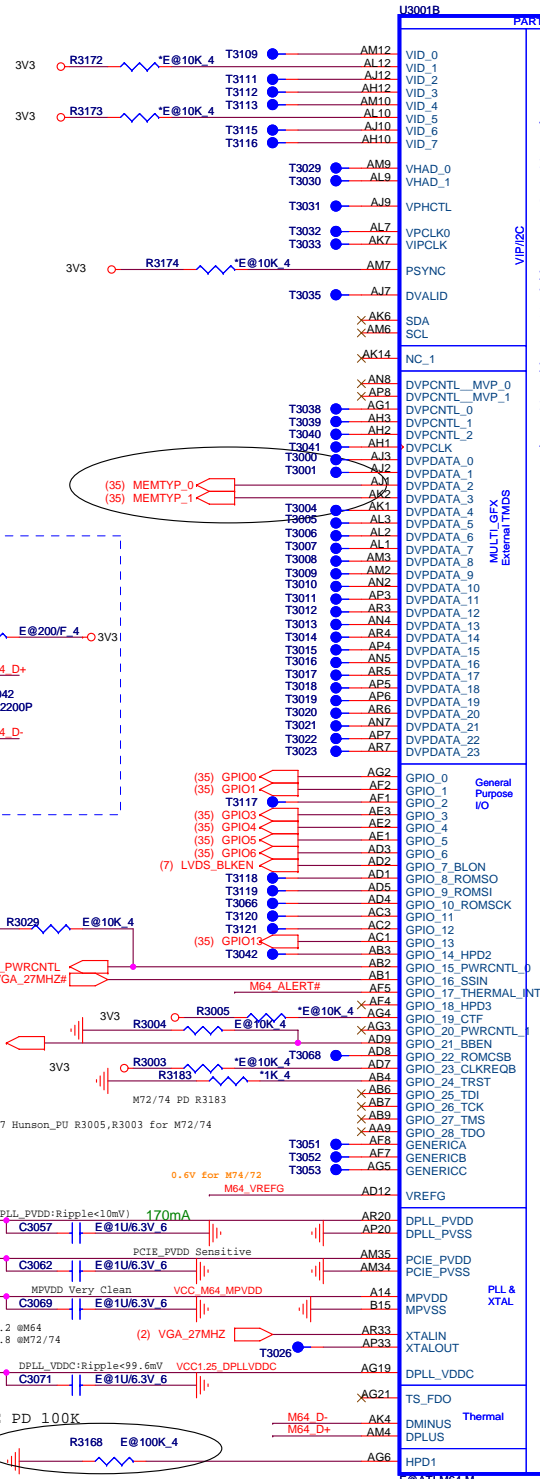
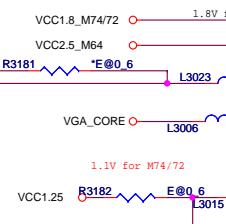
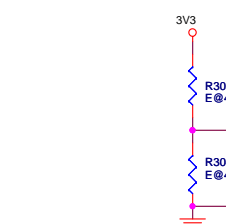
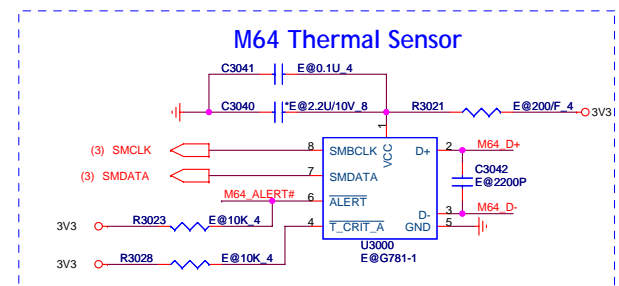
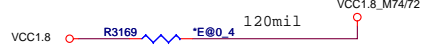


1st LVDS CH



Title			ATI M64M PCIE
Size	Document Number	Rev	
B	GD1 Main Board	1A	
Date:	Tuesday, November 14, 2006	Sheet	31 of 35

1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



Mount 37.5R on R31[49-51] for M72/74 Near Connector Differential routing

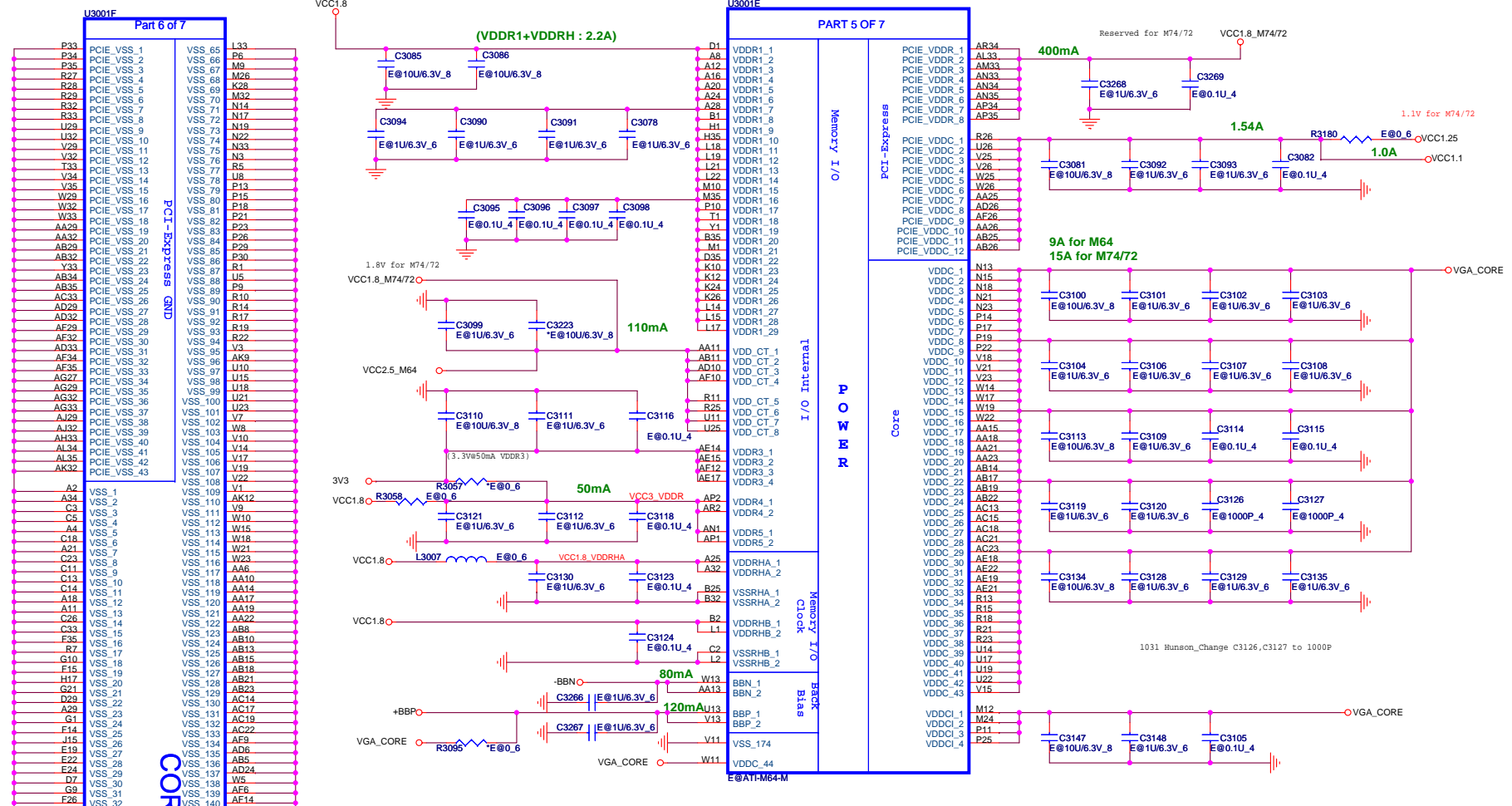
(Max. 100mA)

(Max. 55mA)

R3176, R3177 should close by CON29



ATI M71
 Size Custom Document Number
 Rev 1A



POWER Regulator	M64/M71	Ra11	M72/M74	Ra11
VDDC+VDDCI	1.0-1.2V	VGA_CORE	0.95-1.1V	VGA_CORE
PCIE_PVDD	1.25	VCC1.25	1.8	VCC1.8_M74/72
PCIE_VDDR	NC	x	1.8	VCC1.8_M74/72
PCIE_VDDC	1.25	VCC1.25	1.1	VCC1.1
MPVDD	VDDC	VGA_CORE	VDDC	VGA_CORE
DPLL_PVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
DPLL_VDDC	1.25	VCC1.25	1.1	VCC1.1
VDDR1+VDDRH	1.8	VCC1.8	1.8	VCC1.8
VDDR4+VDDR5	1.8	VCC1.8	1.8	VCC1.8
VDDR3	3.3	3V3	3.3	3V3
VDD_CT	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
LPVDD+TPVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
LVDDR	2.5	VCC2.5_M64	3.3	3V3_M74/72
LVVDDR	NC	x	1.8	VCC1.8_M74/72
TXVDDR	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
AVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
VDD1DI+VDD2DI	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
A2VDD	2.5	VCC2.5_M64	3.3	3V3_M74/72
A2VDDQ	NC	x	1.8	VCC1.8_M74/72

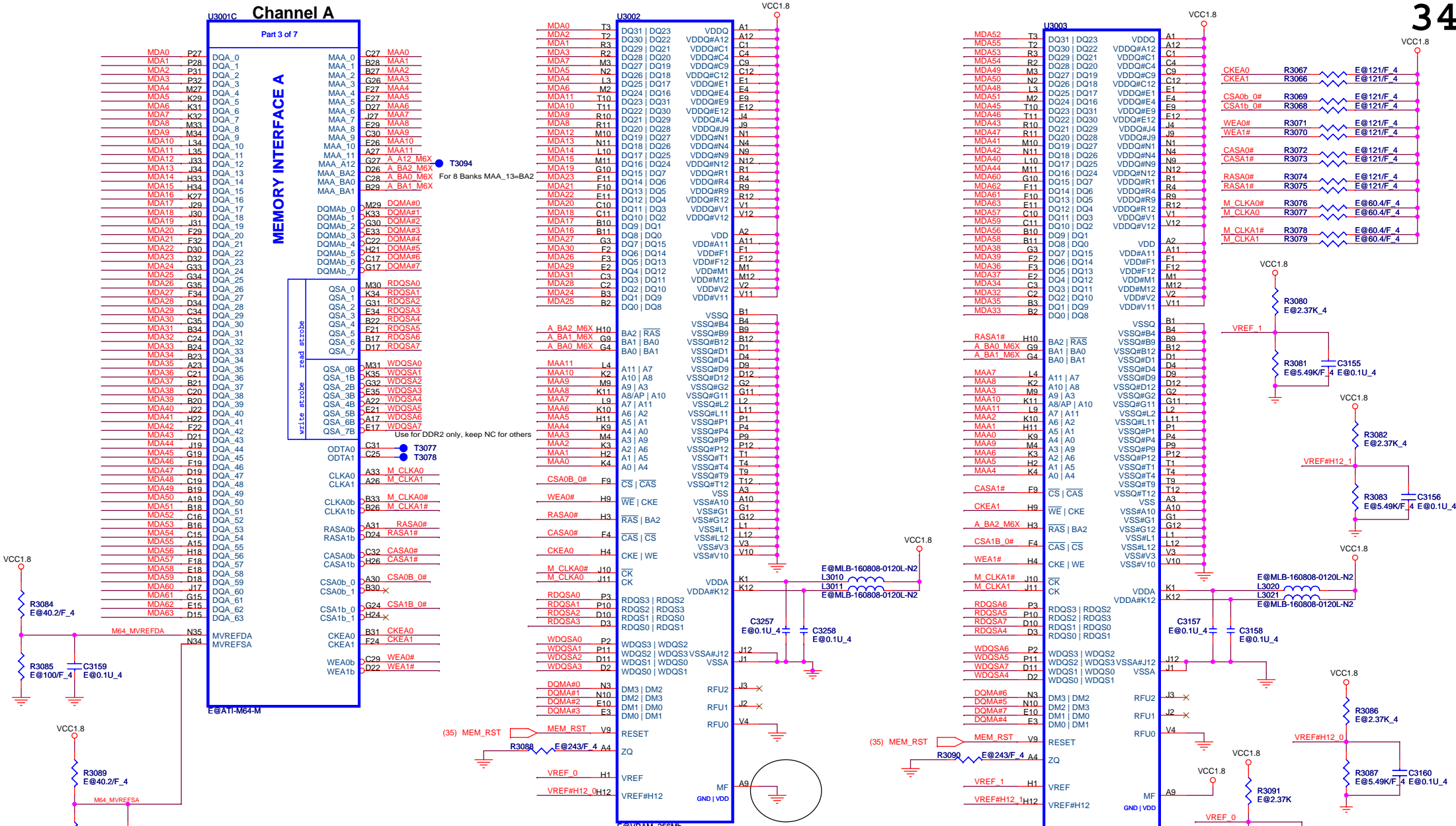
1.Level 1 Environment-related Substances should NEVER be Used.
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QUANTA COMPUTER

ATI M64M POWER

File	Document Number	Rev
Custom	GD1 Main Board	1A

Date: Tuesday, November 14, 2006 Sheet 33 of 35



Signal	DDR1,2	DDR3
MVREF to 1.8V	100R	40.2R
MVREF to GND	100R	100R

1031 Hunson_Change C3184,C3164,c3179,C3174 to 1000P

1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

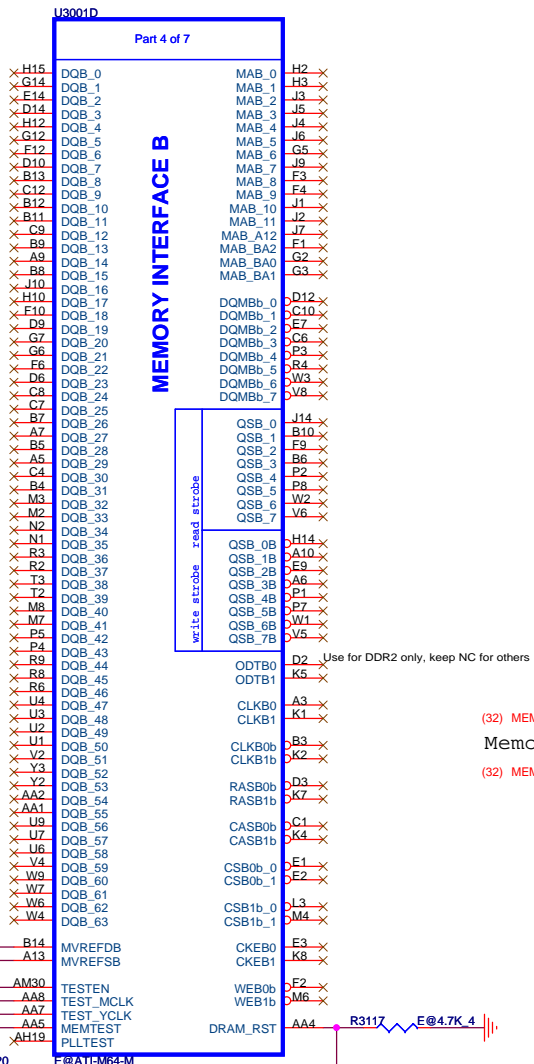
QUANTA COMPUTER

ATI M64M VRAM

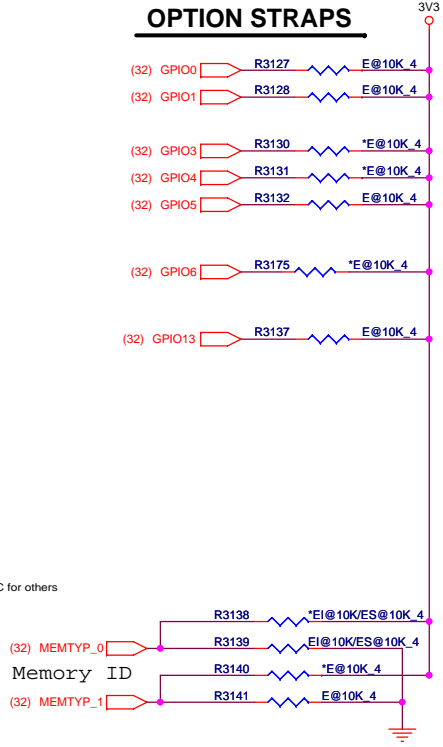
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Channel B



OPTION STRAPS



M64-M Strap

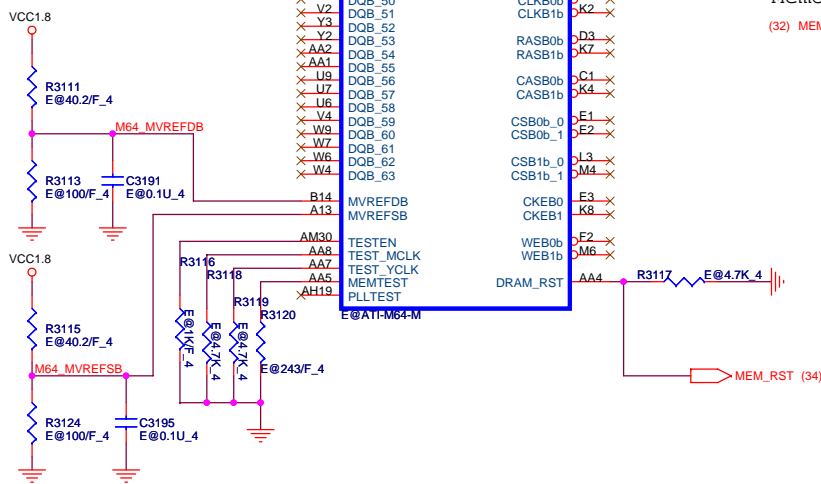
STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: full Tx output swing	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	(recommended) Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (recommended)	0 (internal pull-down)
Reserved	GPIO(3:2)	ATI internal use only. Other logic must not affect this signal during RESET.(GPIO2=VDD_VCL)	00
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0 (internal pull-down)
PLL_IBIAS_RD	GPIO[6:5]	Bias Current for the PCI Express PHY PLL	01
Reserved	GPIO8	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDIs. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128MB 001x - No ROM, MEM_AP_SIZE=01 256MB 010x - No ROM, MEM_AP_SIZE=10 64MB(Default) 011x - No ROM, MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDIs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDIs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDIs from ROM 1011 - Serial M25P10 ROM (ST), chip IDIs from ROM 1100 - Serial M25P05 ROM (ST), chip IDIs from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDIs from ROM	GPIO[9,13,12,11] 0000 (internal pull-down)
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port device present. 1-No slave VIP port devices reporting presence during reset	0 (internal pull-down)
Reserved	PCIE_TEST	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
Reserved	HSYNC	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0

VRAM Straps

REV. 0.1

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE[1:0]	GPIO 27,26	Memory identification for BIOS 00 - Infineon GDDR3 : 2M x 32 bits x 4 banks(Default) 01 - SAMSUNG GDDR3 : 2M x 32 bits x 4 banks 10 - RESERVED 11 - RESERVED	00

MEMTYPE1	MEMTYPE0	R3124	R3125	R3122	R3123	
0	0	NC	10K	NC	10K	00 - Infineon GDDR3 : 2M x 32 bits x 4 banks
0	1	NC	10K	10K	NC	01 - SAMSUNG GDDR3 : 2M x 32 bits x 4 banks
1	0	10K	NC	NC	10K	10 - RESERVED
1	1	10K	NC	10K	NC	11 - RESERVED



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QUANTA COMPUTER

Title: **ATI M64-M STRAP**

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