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PCB P/N: 1P-0065102-80SA - FUBAI
 1P-0065201-80SA - NANYA
 1P-0065503-80SA - HANNSTAR

Project Code & Schematics Subject: MS60-L Main Board

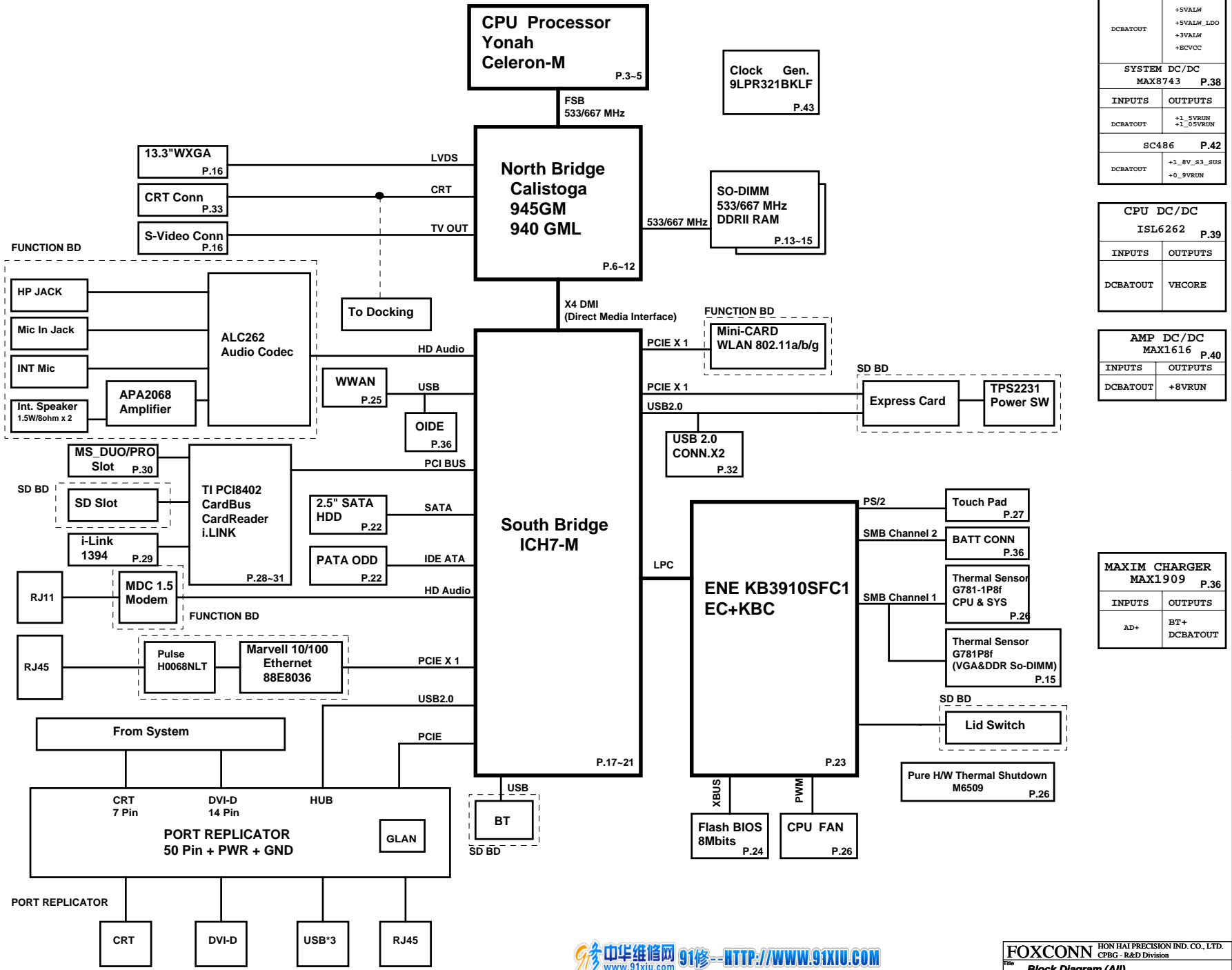
P. Leader	Check by	Design by

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Custom	MS60-1-05 (MBX-163)	0.20
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MS60 (CALISTOGA GM Block Diagram)

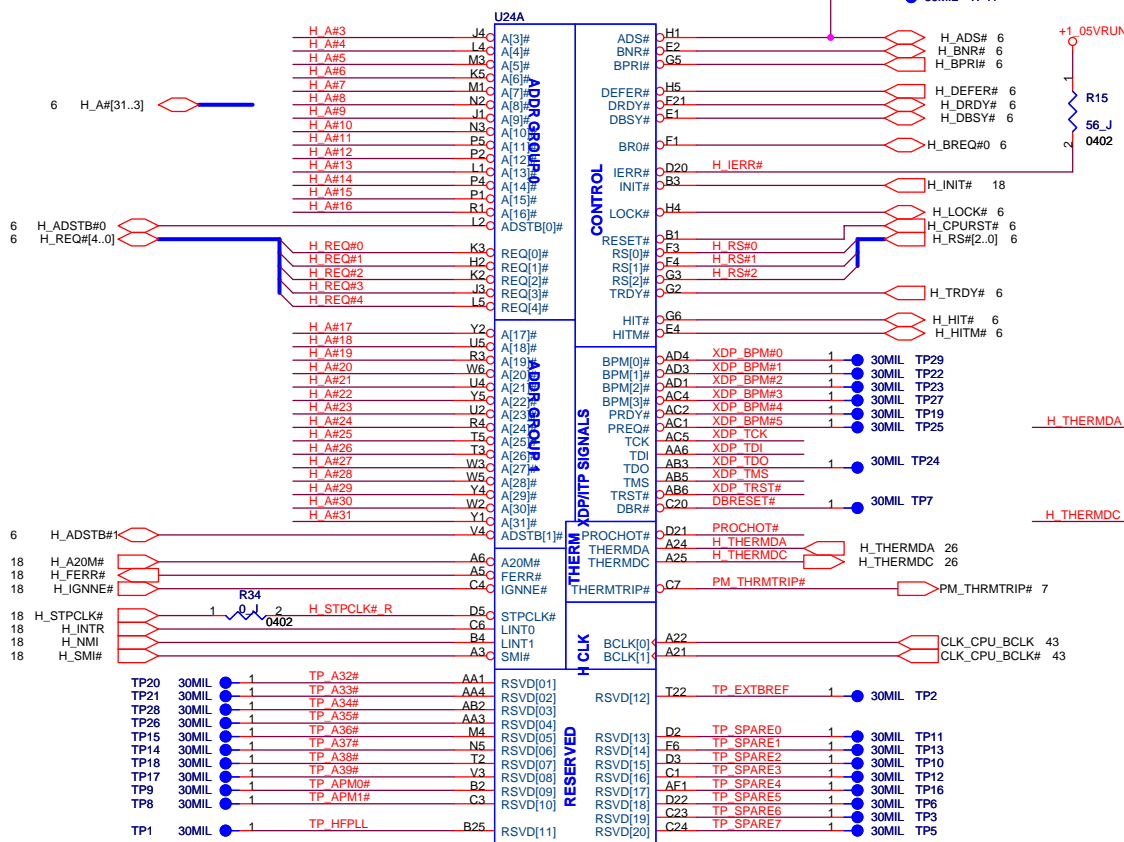


SYSTEM DC/DC MAX8734 P.37	
INPUTS	OUTPUTS
DCBATOUT	+5VALW +5VALW_LDO +3VALW +ECVCC
SYSTEM DC/DC MAX8743 P.38	
INPUTS	OUTPUTS
DCBATOUT	+1_5VRUN +1_05VRUN
SC486 P.42	
DCBATOUT	+1_8V_83_SUS +0_9VRUN

CPU DC/DC ISL6262 P.39	
INPUTS	OUTPUTS
DCBATOUT	VHORE

AMP DC/DC MAX1616 P.40	
INPUTS	OUTPUTS
DCBATOUT	+8VRUN

MAXIM CHARGER MAX1909 P.36	
INPUTS	OUTPUTS
AD+	BT+ DCBATOUT

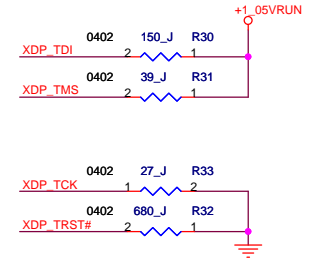
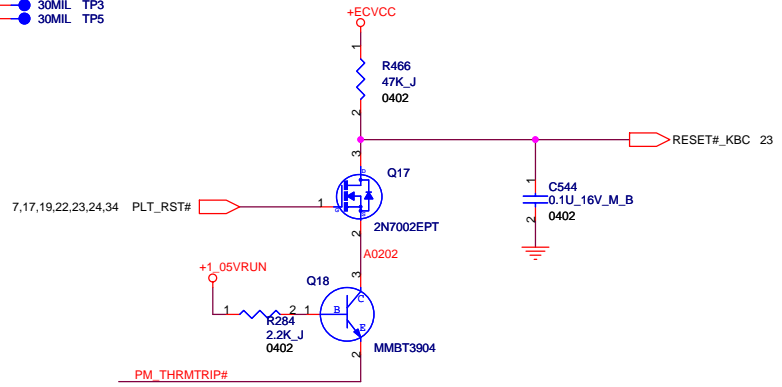
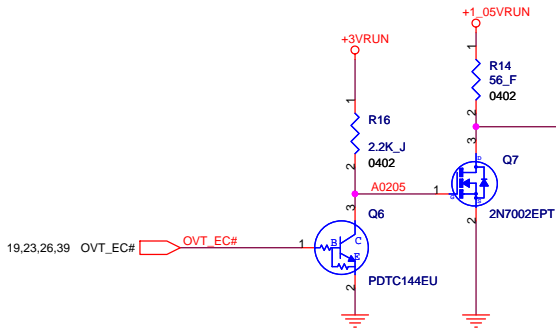


Layout note:
no stub on
H_STPCLK#

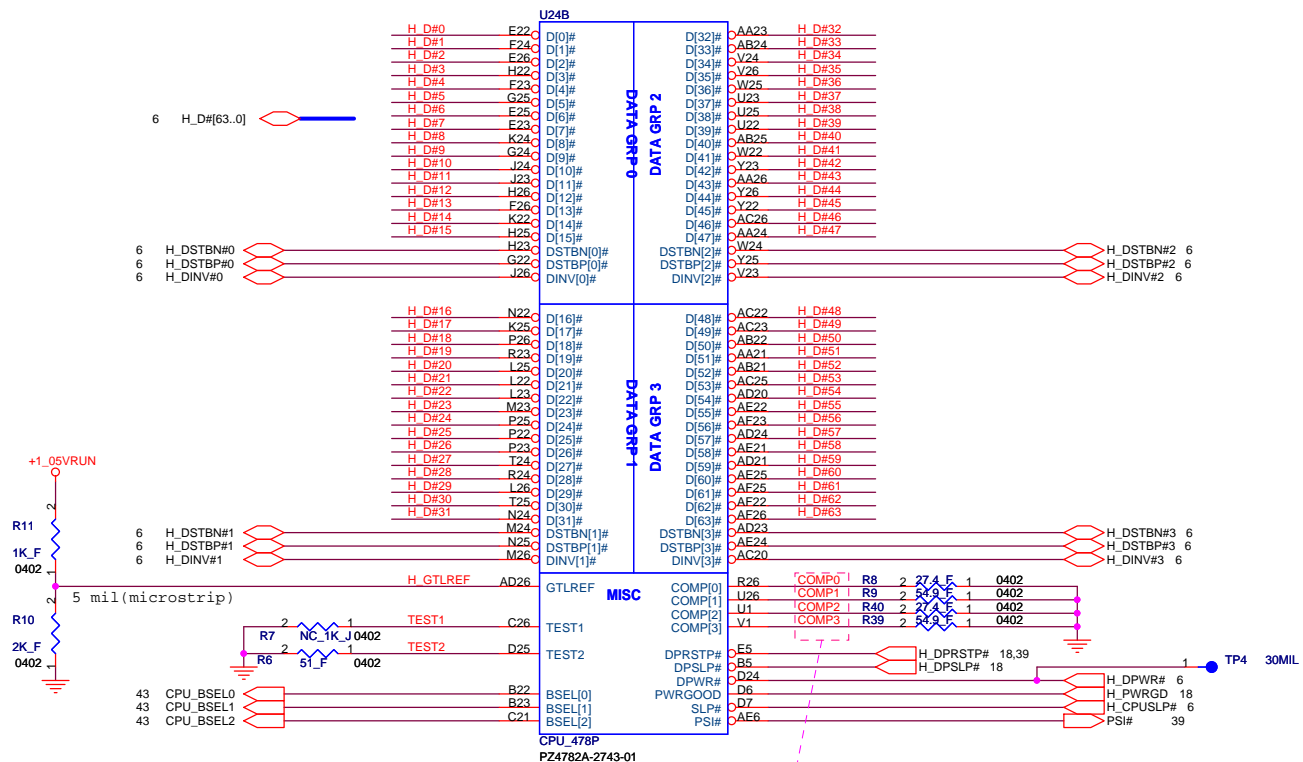
A#[32-39], APM#[0-1]:
Leave escape routing
on for future
functionality

ICH7M's GPIO12: VIL----> -0.5V ~ 0.8V
VIH----> 2.0V ~ 3.3+0.5V
YONAH's PROCHOT#: VIL----> -0.1V ~ 0.3*VCCP
VIH----> 0.7*VCCP ~ VCCP+0.1

If PROCHOT# is routed between
CPU, IMVP and MCH, pull-up
resistor has to be 75 ohm +/-5%



Debug port not used.
resistors close to CPU.

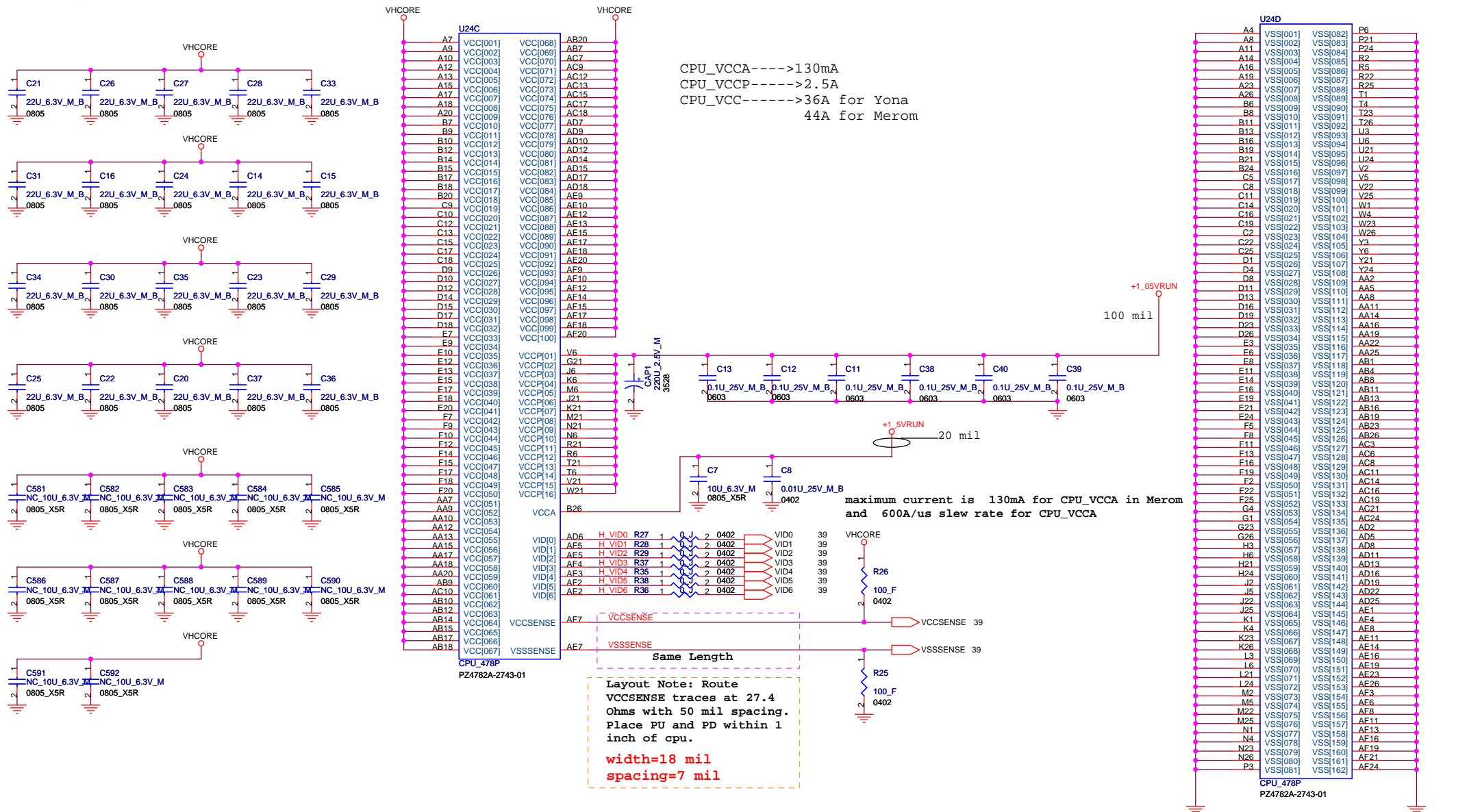


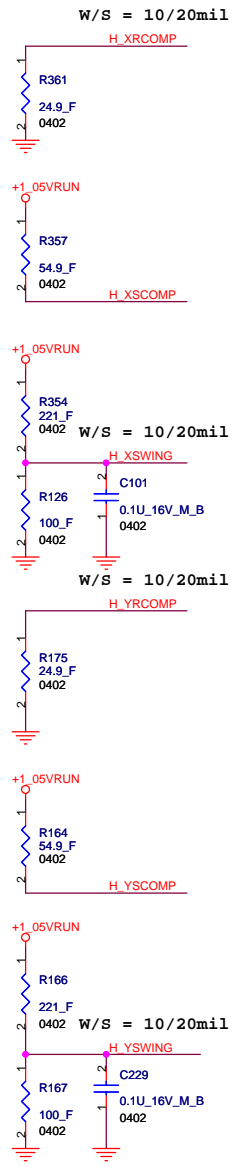
Place close to CPU
Layout Note:
Zo=55 ohm, 0.5"
max for GTLREF.

FSB Frequency Table:

BSEL[2:0]	Freq.(MHz)
LLL	Reserve
LLH	133
LHL	Reserve
LHH	166

Layout Note:
Comp0,2 connect with Zo=27.4 ohm, make trace length shorter then 0.5".
Comp1,3 connect with Zo=55 ohm, make trace length shorter then 0.5".



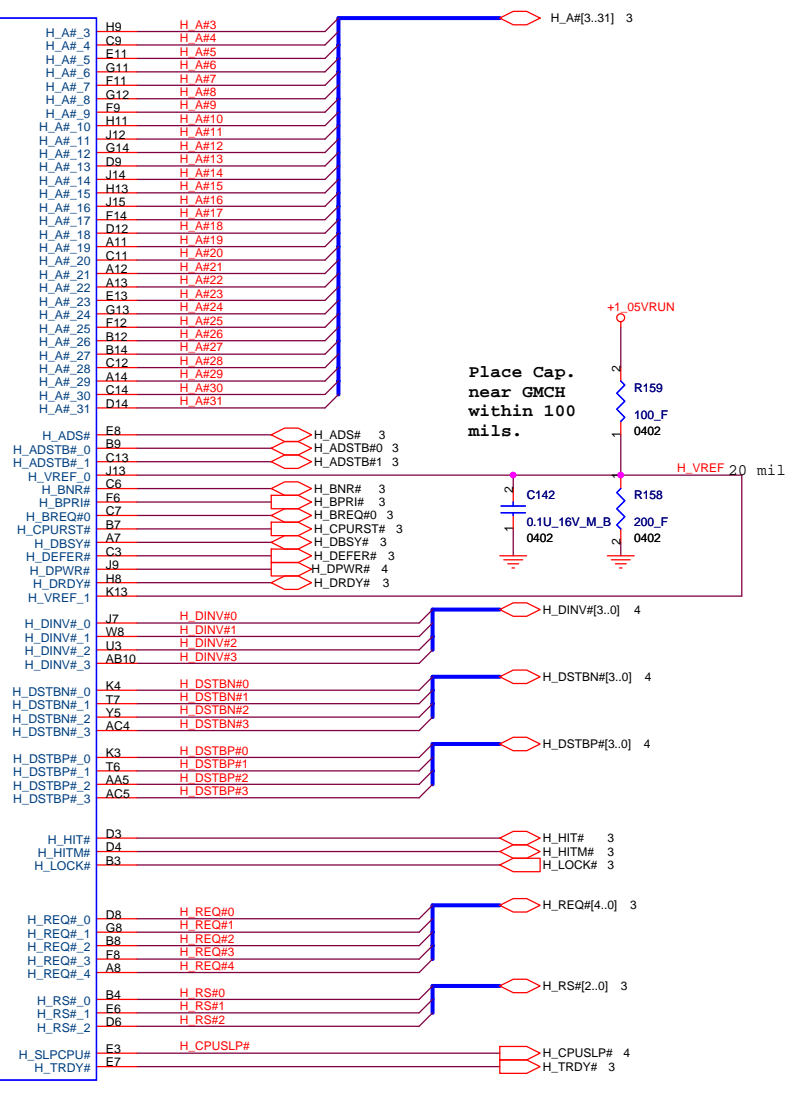


4 H_D#[63..0] H_D#[63..0]

H_D#0	F1	H_D#_0
H_D#1	J1	H_D#_1
H_D#2	H1	H_D#_2
H_D#3	J6	H_D#_3
H_D#4	H3	H_D#_4
H_D#5	K2	H_D#_5
H_D#6	G1	H_D#_6
H_D#7	G2	H_D#_7
H_D#8	K9	H_D#_8
H_D#9	K1	H_D#_9
H_D#10	K7	H_D#_10
H_D#11	J8	H_D#_11
H_D#12	H4	H_D#_12
H_D#13	J3	H_D#_13
H_D#14	K11	H_D#_14
H_D#15	G4	H_D#_15
H_D#16	T10	H_D#_16
H_D#17	W11	H_D#_17
H_D#18	T3	H_D#_18
H_D#19	U7	H_D#_19
H_D#20	U9	H_D#_20
H_D#21	U11	H_D#_21
H_D#22	T11	H_D#_22
H_D#23	W9	H_D#_23
H_D#24	T1	H_D#_24
H_D#25	T8	H_D#_25
H_D#26	T4	H_D#_26
H_D#27	W7	H_D#_27
H_D#28	U5	H_D#_28
H_D#29	T9	H_D#_29
H_D#30	W6	H_D#_30
H_D#31	T5	H_D#_31
H_D#32	AB7	H_D#_32
H_D#33	AA9	H_D#_33
H_D#34	W4	H_D#_34
H_D#35	W3	H_D#_35
H_D#36	Y3	H_D#_36
H_D#37	Y7	H_D#_37
H_D#38	W5	H_D#_38
H_D#39	Y10	H_D#_39
H_D#40	AB8	H_D#_40
H_D#41	W2	H_D#_41
H_D#42	AA4	H_D#_42
H_D#43	AA7	H_D#_43
H_D#44	AA2	H_D#_44
H_D#45	AA6	H_D#_45
H_D#46	AA10	H_D#_46
H_D#47	Y8	H_D#_47
H_D#48	AA1	H_D#_48
H_D#49	AB4	H_D#_49
H_D#50	AC9	H_D#_50
H_D#51	AB11	H_D#_51
H_D#52	AC11	H_D#_52
H_D#53	AB3	H_D#_53
H_D#54	AC2	H_D#_54
H_D#55	AD1	H_D#_55
H_D#56	AD9	H_D#_56
H_D#57	AC1	H_D#_57
H_D#58	AD7	H_D#_58
H_D#59	AC6	H_D#_59
H_D#60	AB5	H_D#_60
H_D#61	AD10	H_D#_61
H_D#62	AD4	H_D#_62
H_D#63	AC8	H_D#_63
H_XRCOMP	E1	H_XRCOMP
H_XSCOMP	E2	H_XSCOMP
H_XSWING	E4	H_XSWING
H_YRCOMP	Y1	H_YRCOMP
H_YSCOMP	U1	H_YSCOMP
H_YSWING	W1	H_YSWING
AG2		
AG1		

U27A

HOST



Place Cap. near GMCH within 100 mils.

43 CLK_MCH_BCLK#
43 CLK_MCH_BCLK#

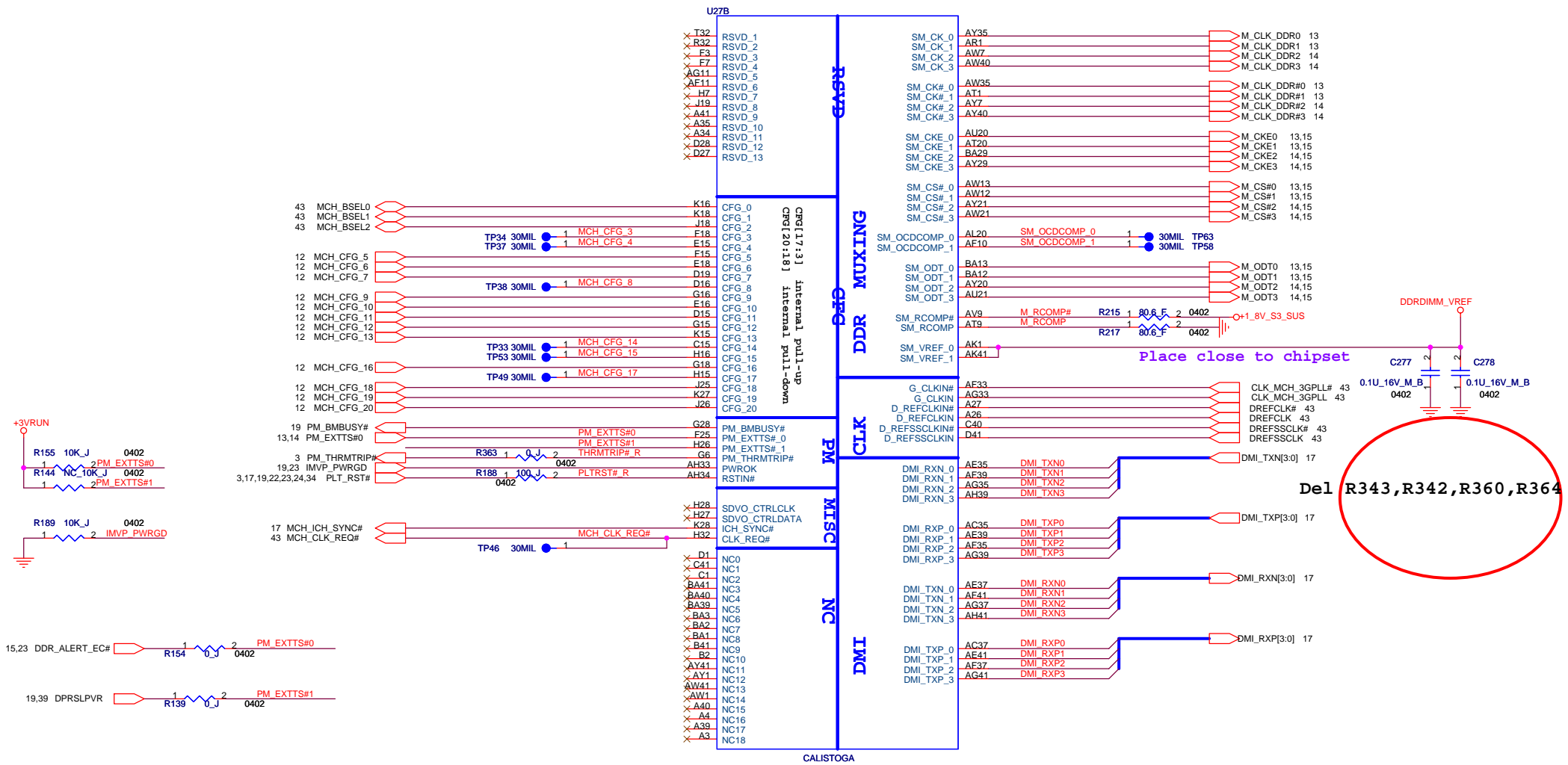
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PM	Q988CPM	12-0G88CPM-0000
GML	940GML-QK60-A3	12-940GML0-A300

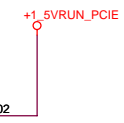
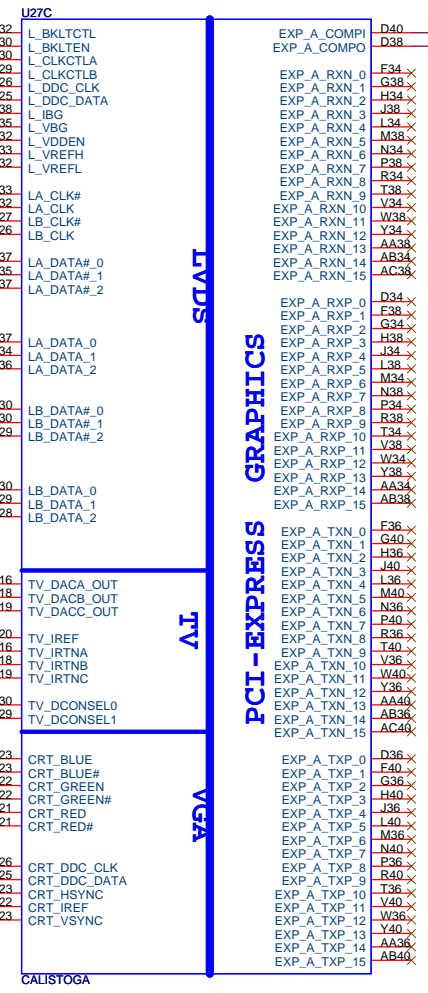
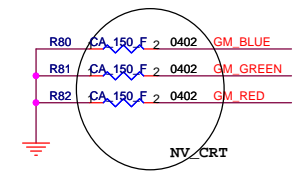
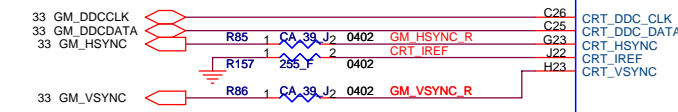
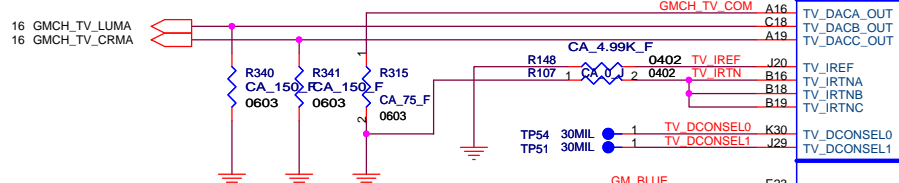
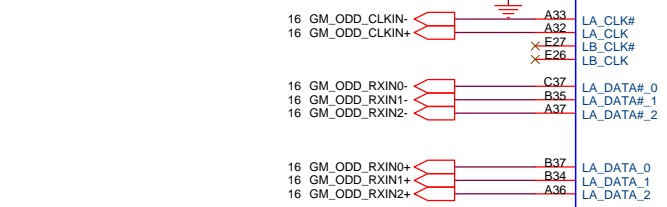
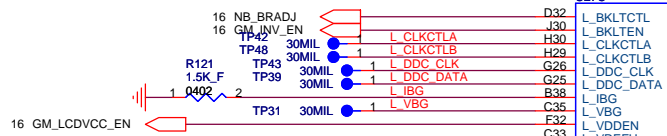
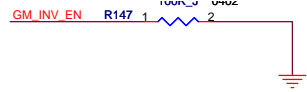
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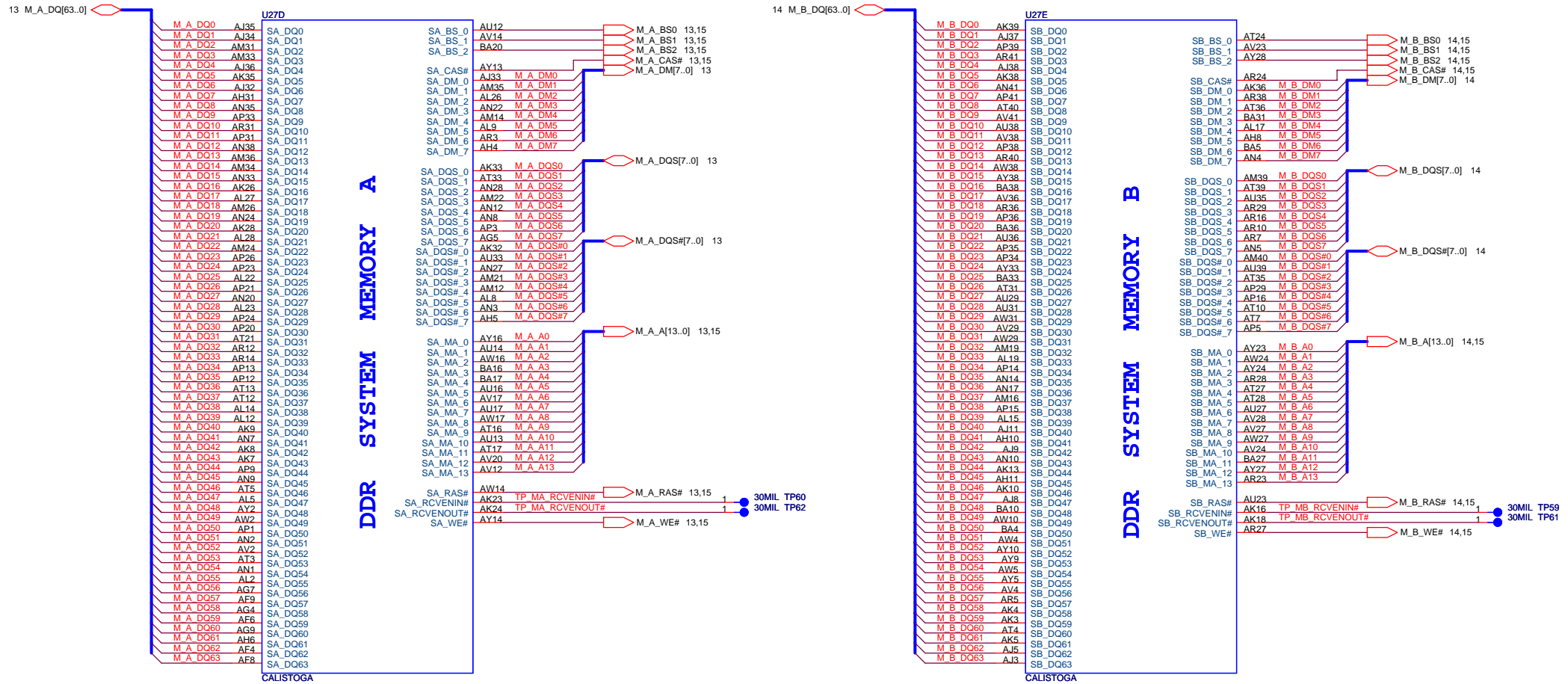
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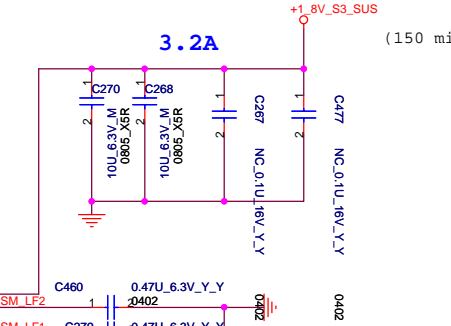
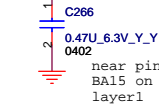
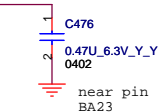
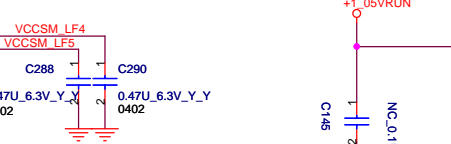
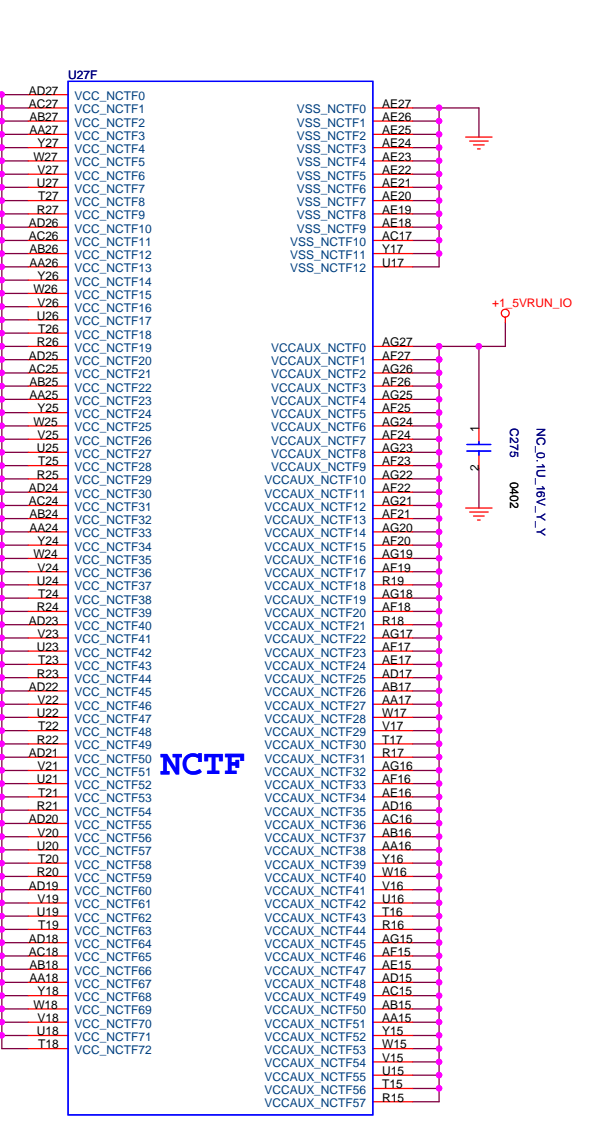
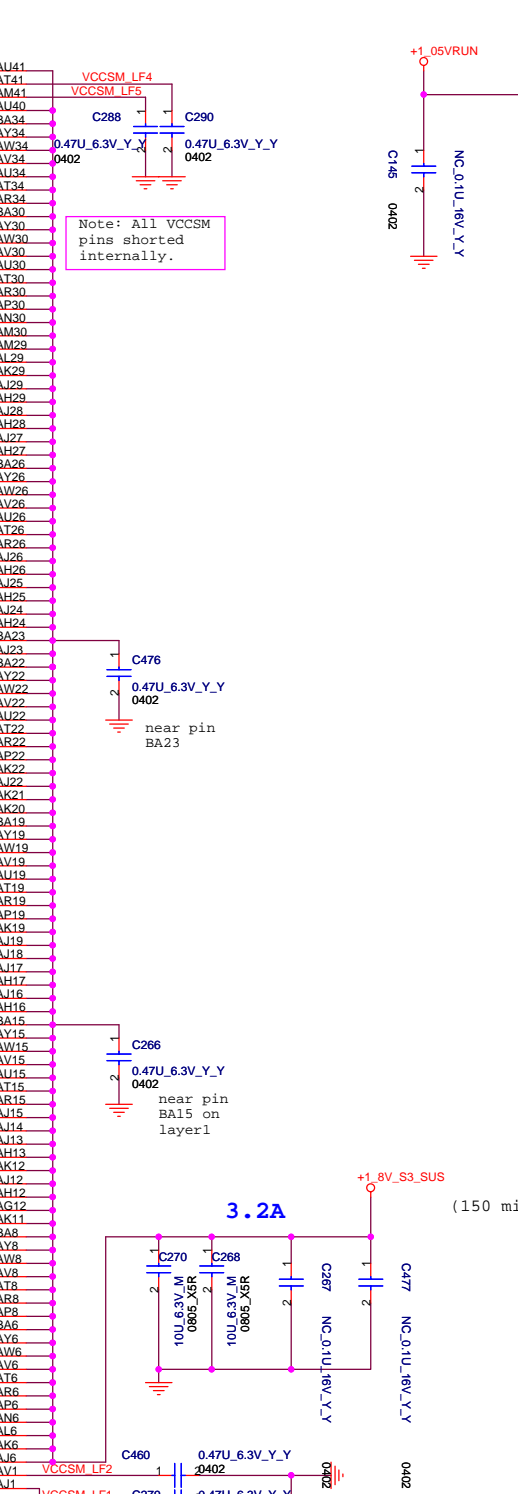
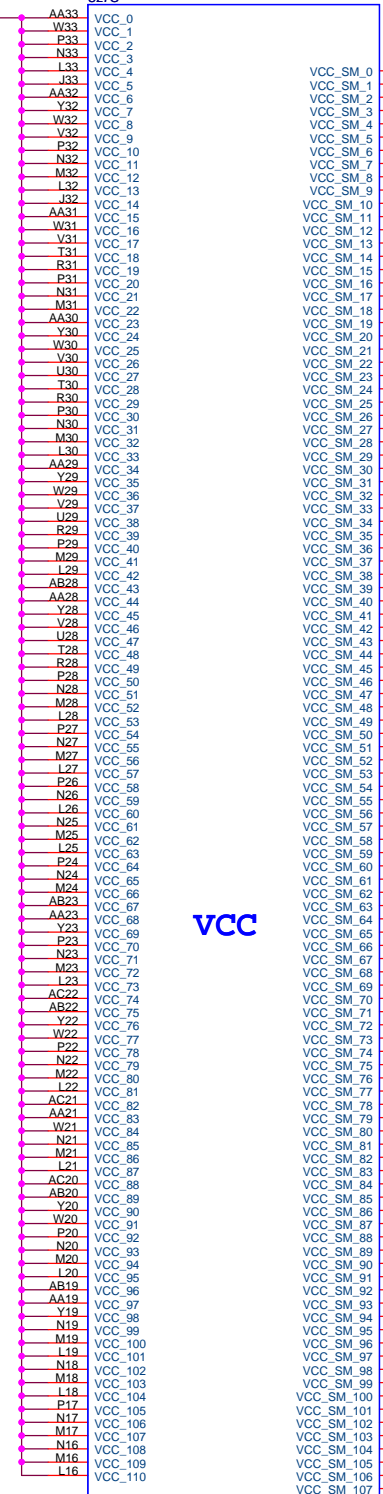
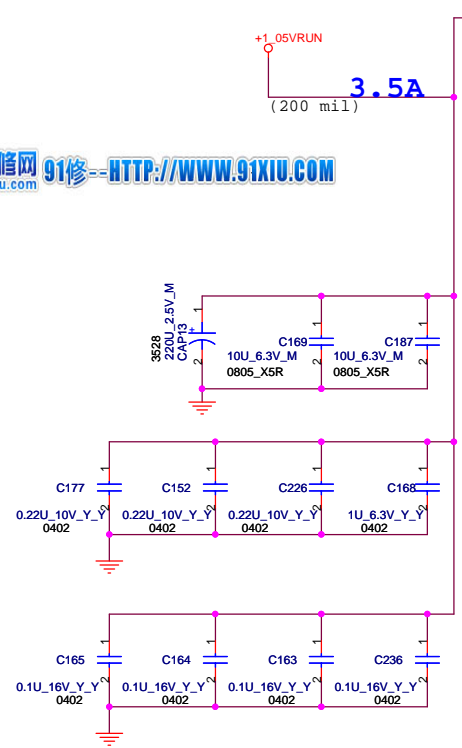
Size: A3 Document Number: **MS60-1-05 (MBX-163)** Rev: 0.20

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MCH_CFG_5	Low = DMIX2 High = DMIX4
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MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V
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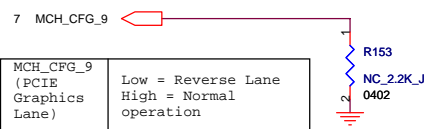


MCH_CFG_6	Low = Moby Dick High = Calistoga DDR2 select (default high)
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MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor
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MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED
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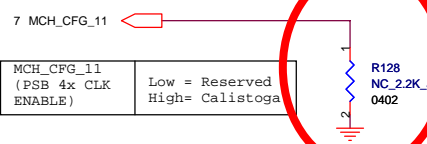


MCH_CFG_9 (PCIe Graphics Lane)	Low = Reverse Lane High = Normal operation
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MCH_CFG_20 (PCIe Backward Interoperability mode)	Low = Only SDVO or PCIe x1 is operational (defaults) High = SDVO and PCIe x1 are operating simultaneously via the PEG port
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MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY
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MCH_CFG_11 (PSB 4x CLK ENABLE)	Low = Reserved High = Calistoga
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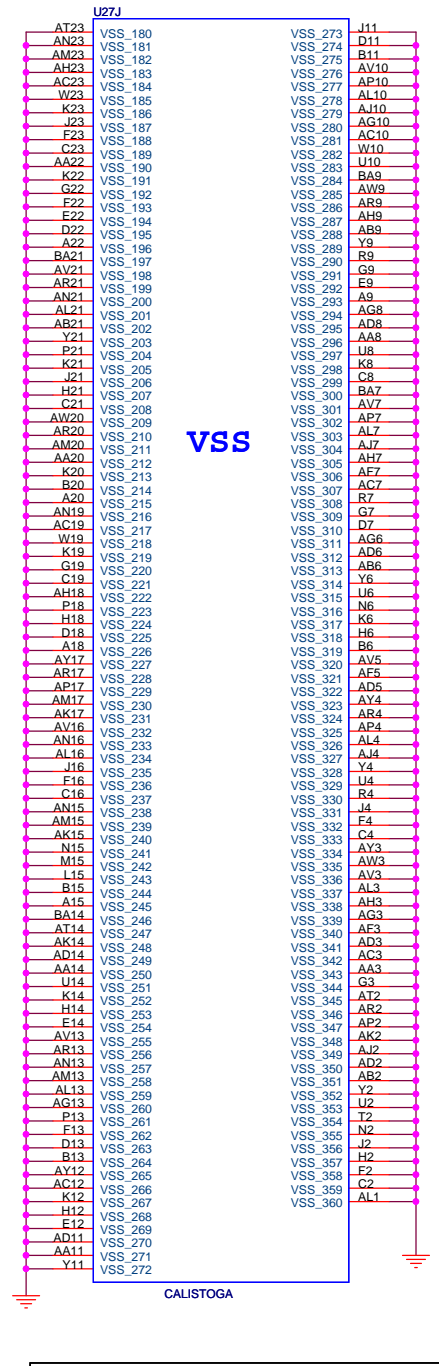
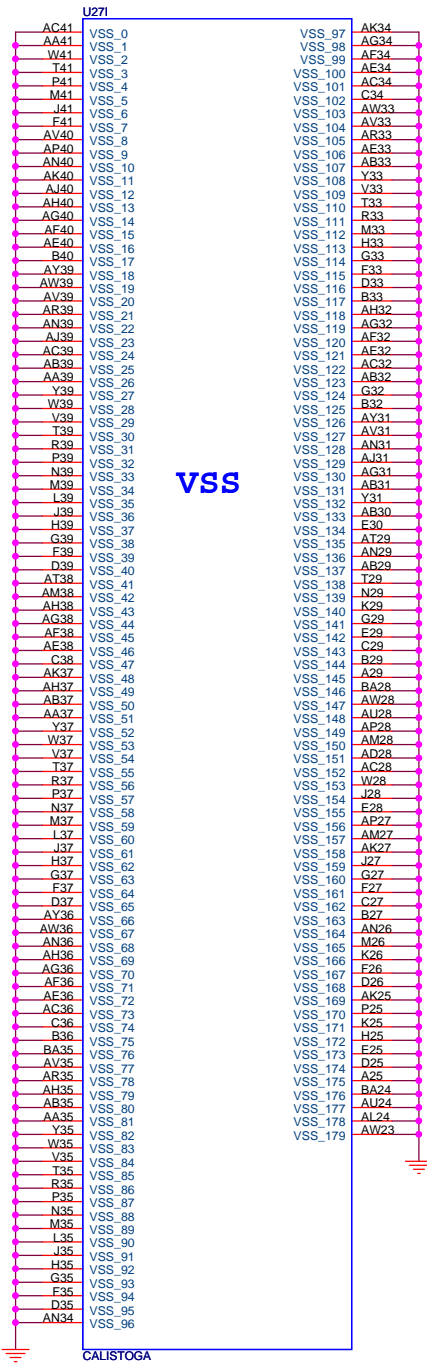
Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub



MCH_CFG_[13:12] (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)
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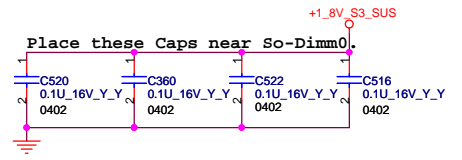
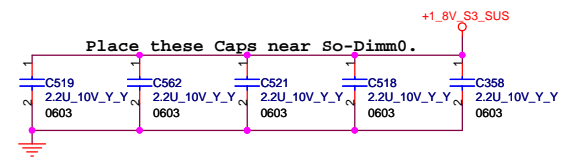
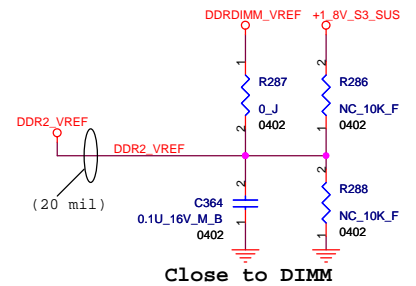
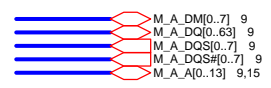
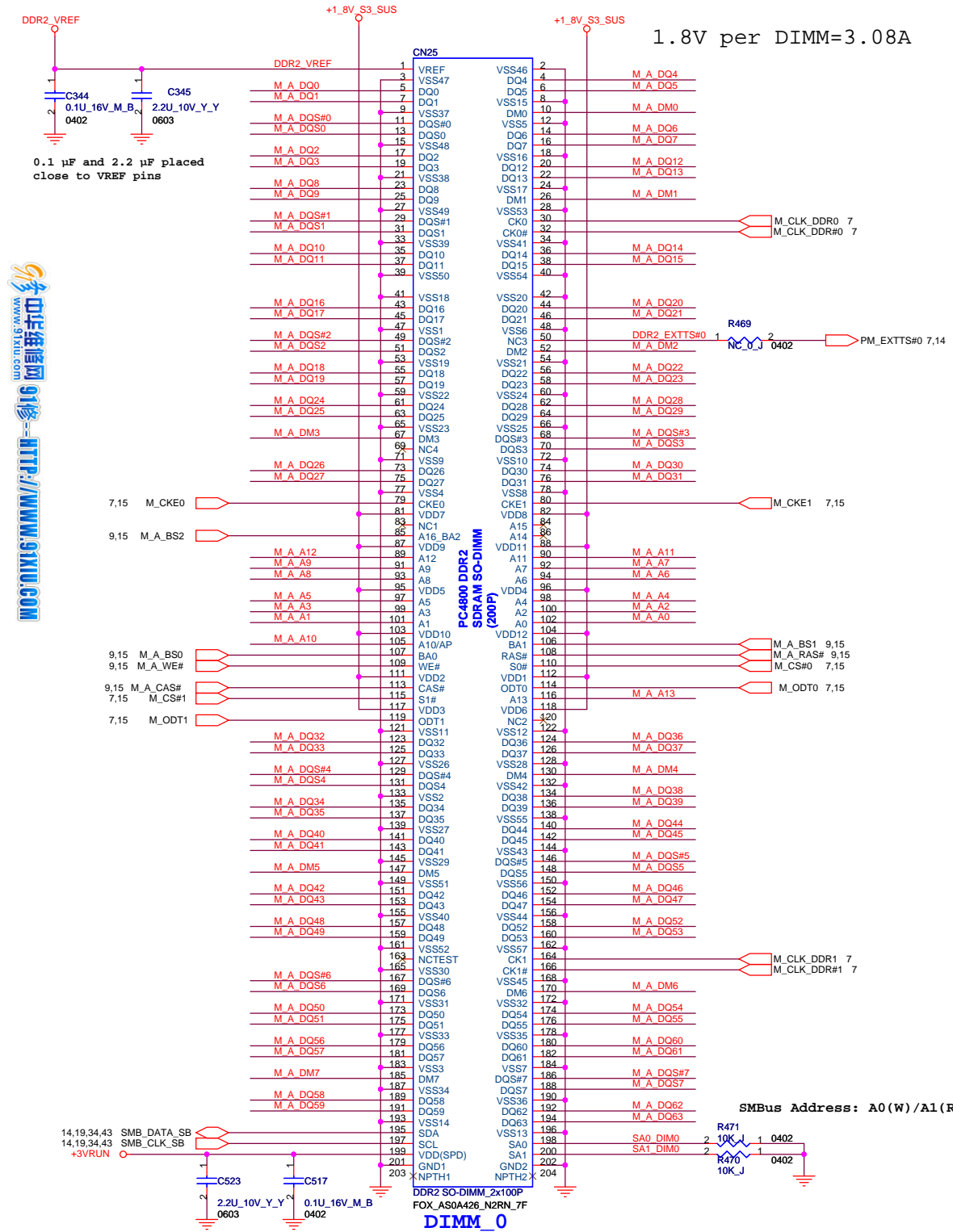
MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable
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Check CALISTOGA version , after A2 version , if systec can't boot up then NC the pull low R

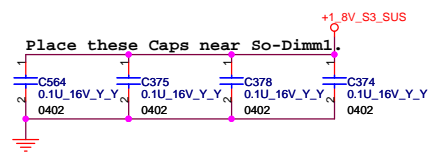
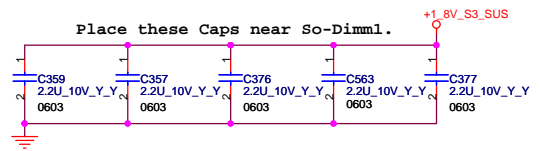
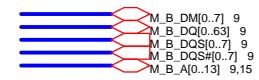
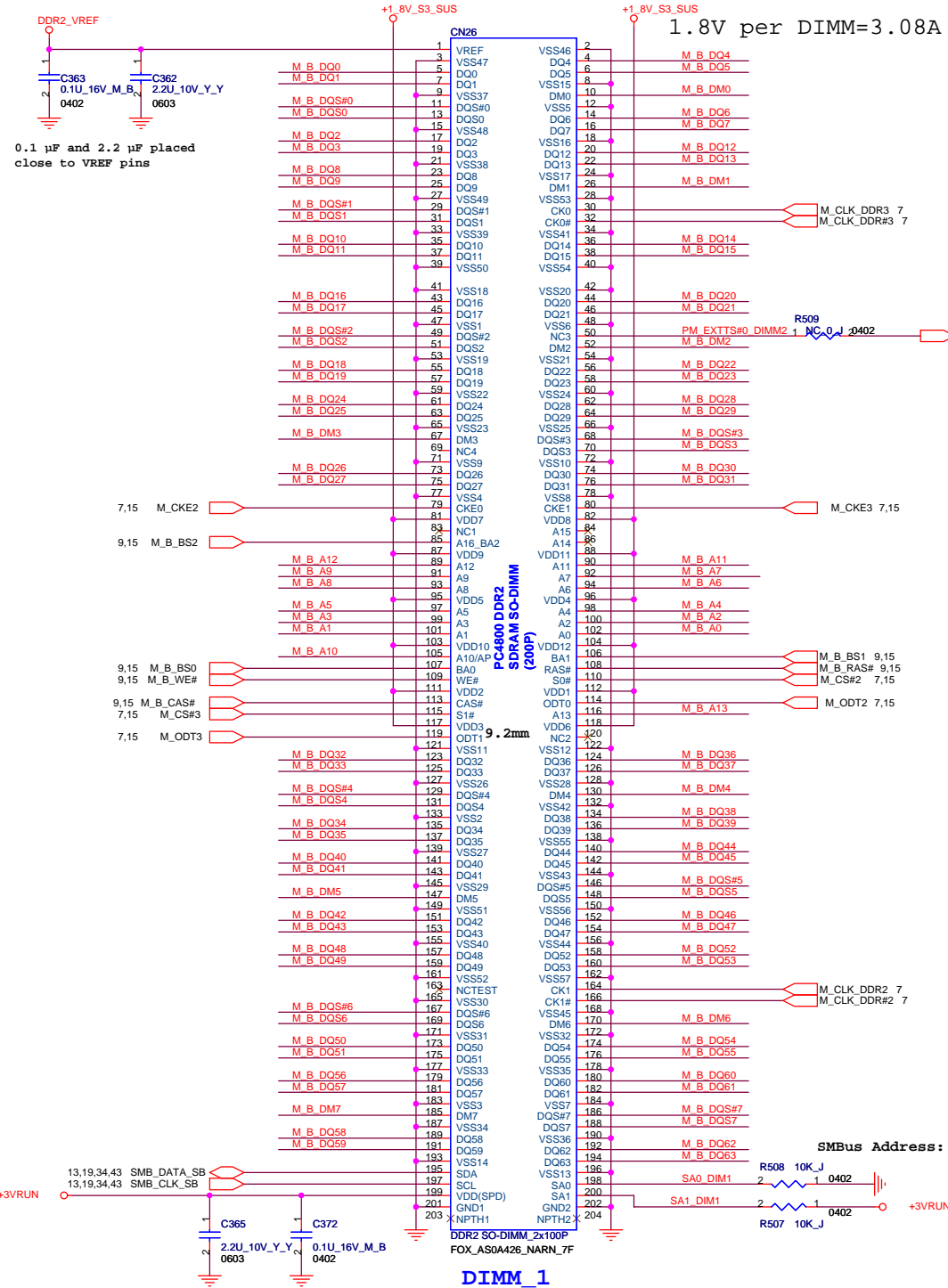
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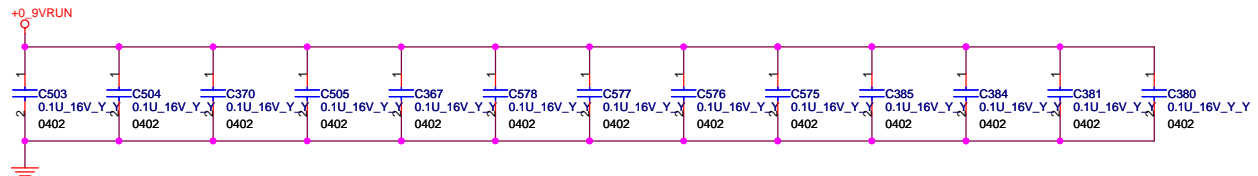
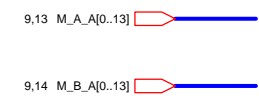
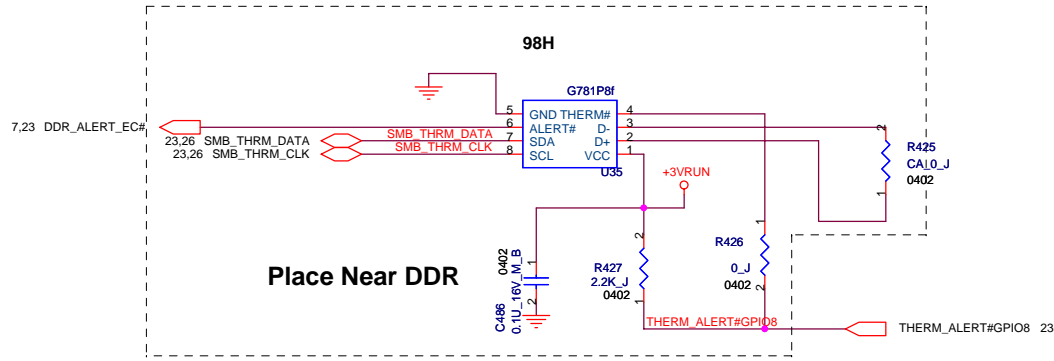
1.8V per DIMM=3.08A



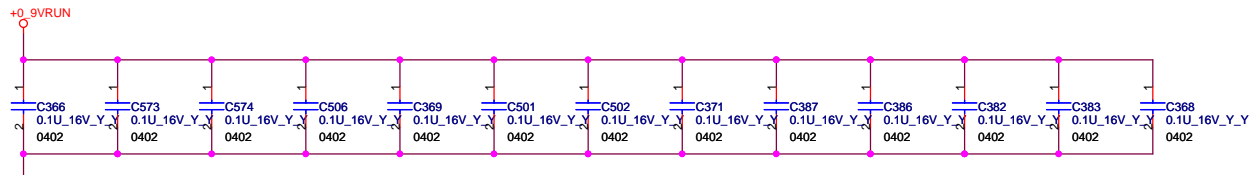
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FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title DDR(II)SO-DIMM_0			
Size A3	Document Number		Rev 0.20
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Date: Monday, June 19, 2006	Sheet 13	of 47	

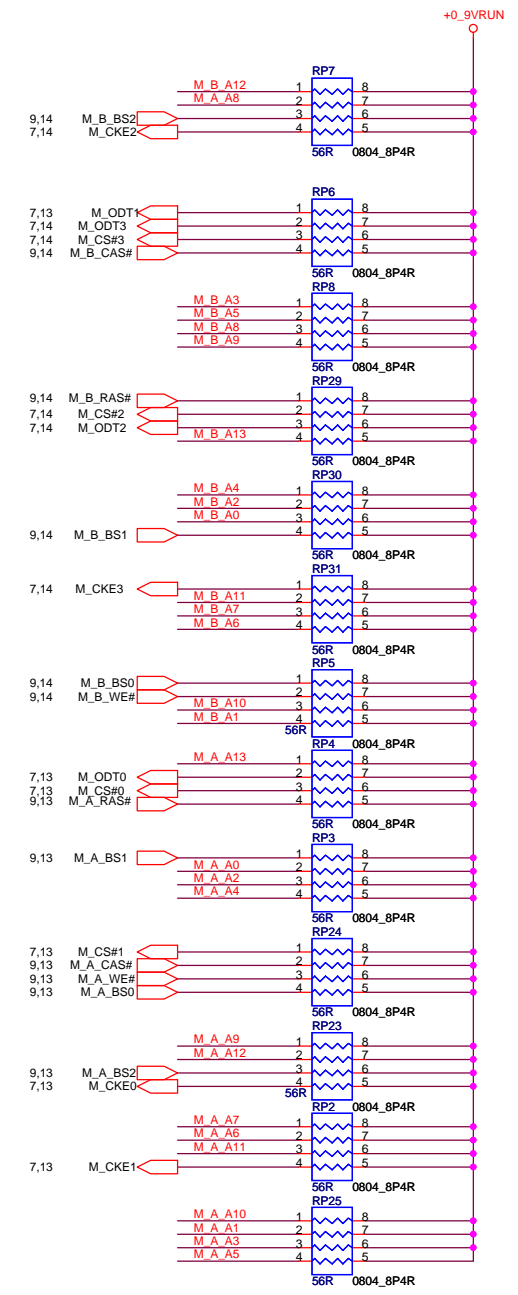




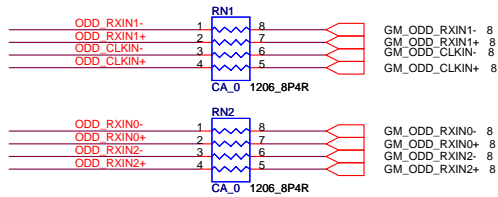
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



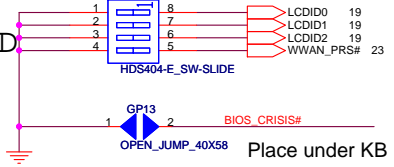
Layout note: Place 1 cap close to every 1 R-pack terminated to +0_9VRUN



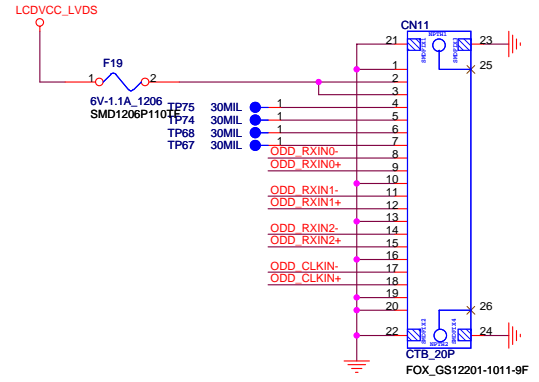
LVDS



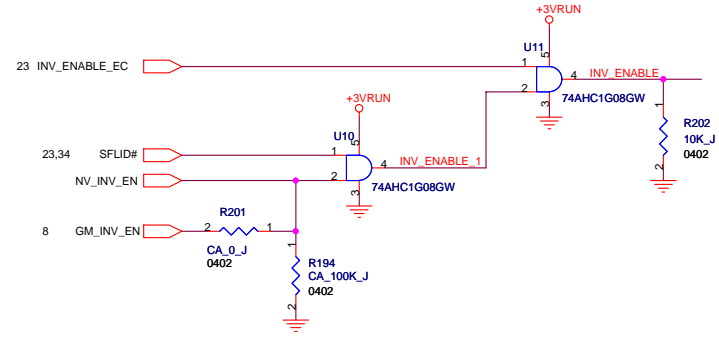
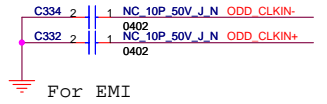
PANEL ID



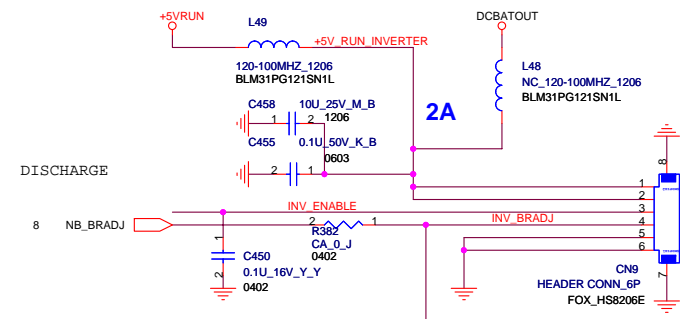
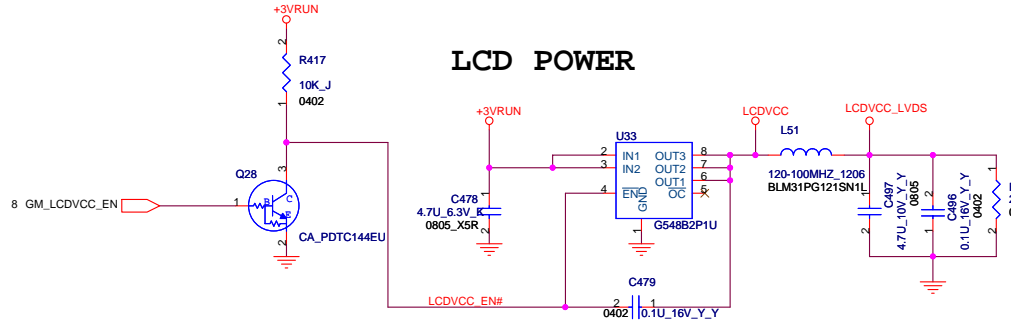
Size	13.3" wide		
Vendor	AUO	SHARP	
Type			
Panel ID Check[2..0]	001	010	



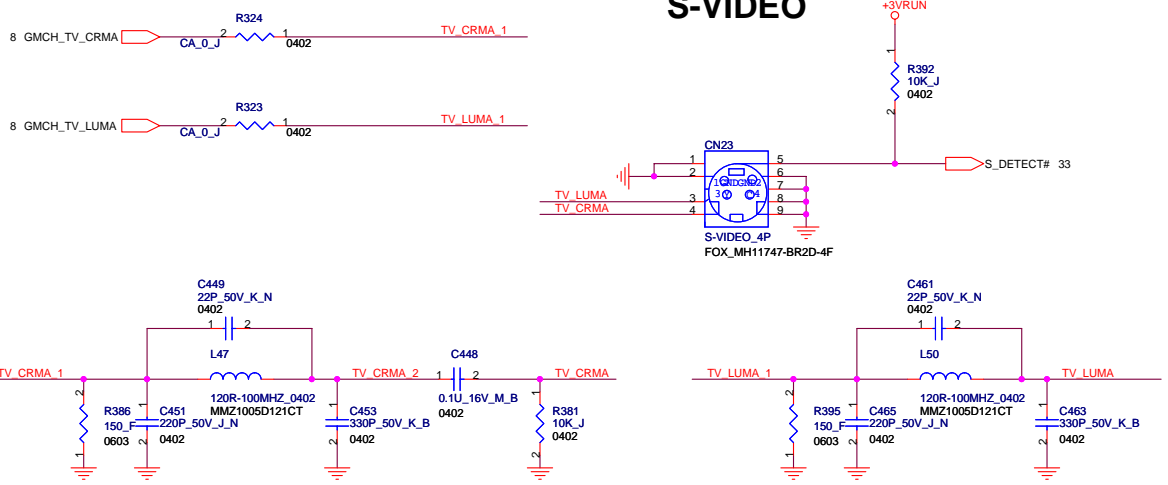
LVDS CONNECTOR



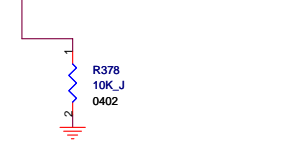
LCD POWER

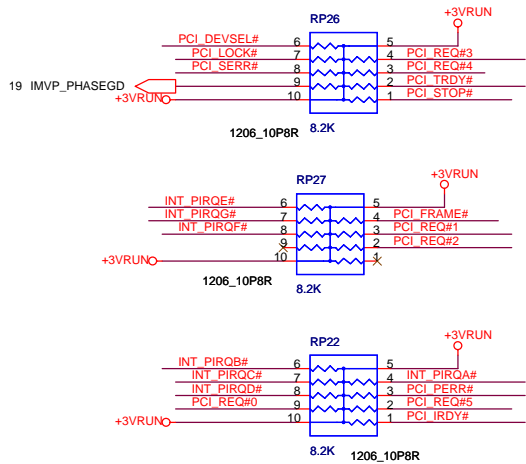


S-VIDEO

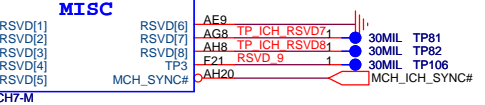
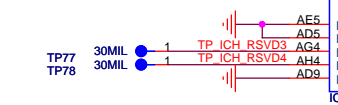
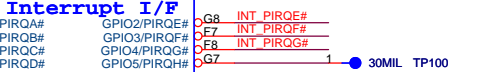
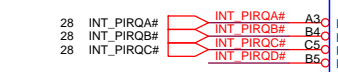
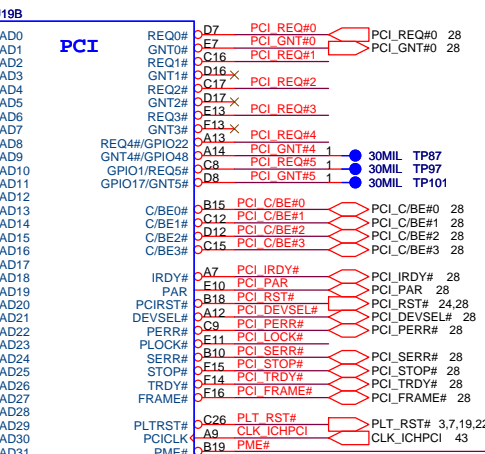
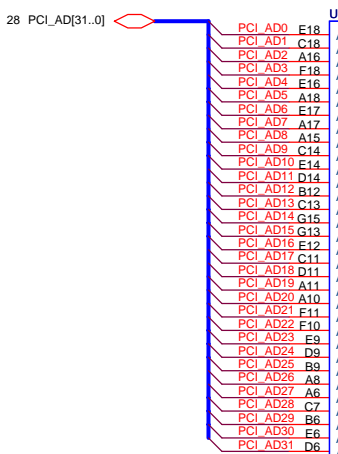


INVERTER CONNECTOR

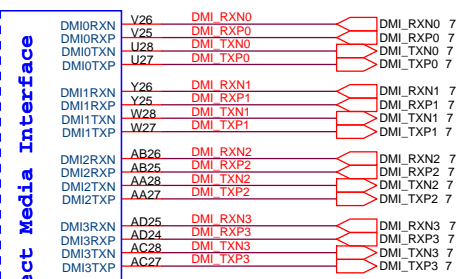
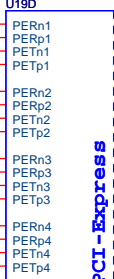
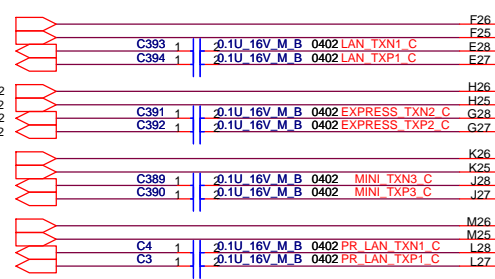
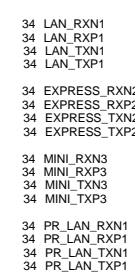




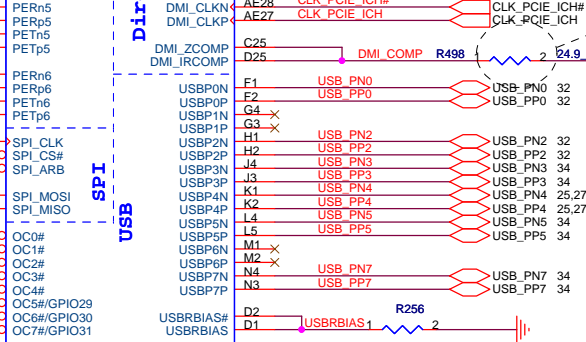
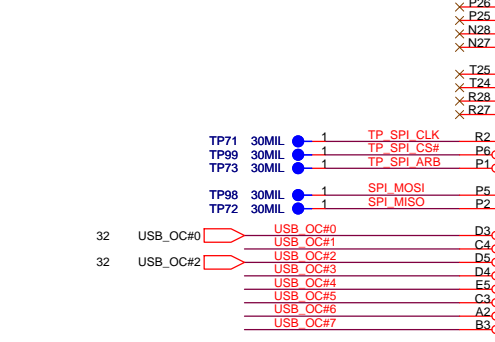
PCI Pullups



Test leakage voltage in BB



Place within 500 mils of ICH



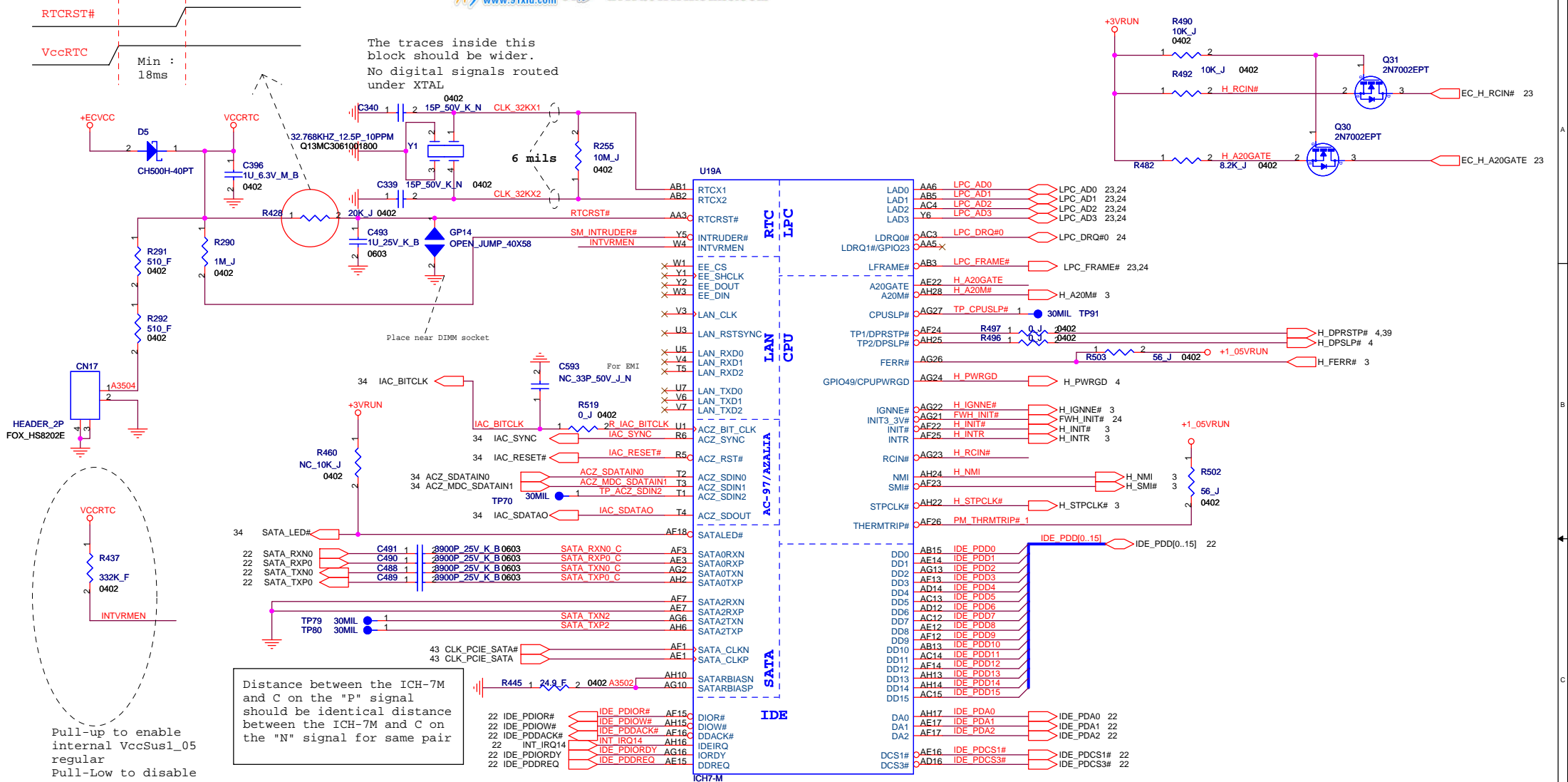
Place within 500 mils of ICH and don't routing next to high speed signals

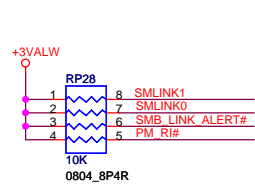
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CPBG - R&D Division

Title: **ICH7-M(PCI/DMI/USB/PCIE) 1/5**

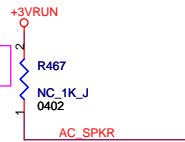
Size: A3 Document Number: **MS60-1-05 (MBX-163)** Rev: 0.20

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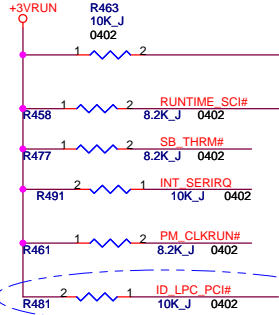
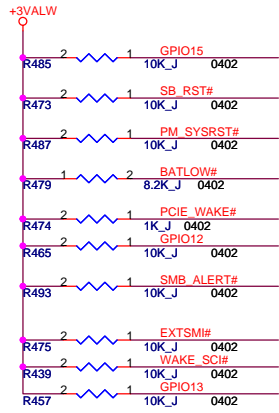




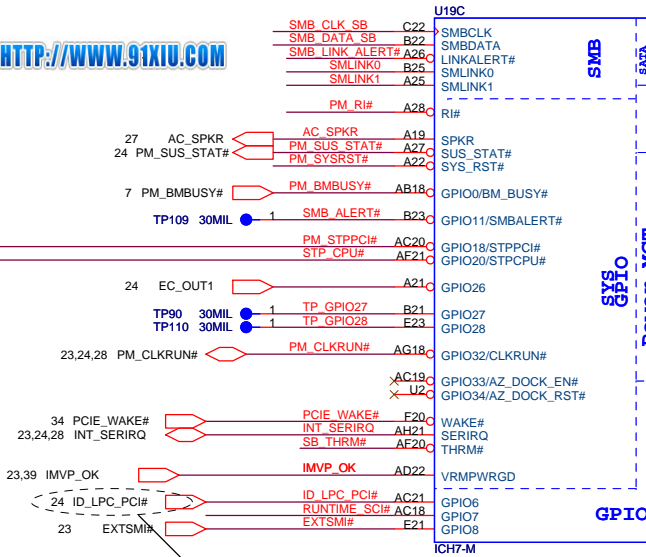
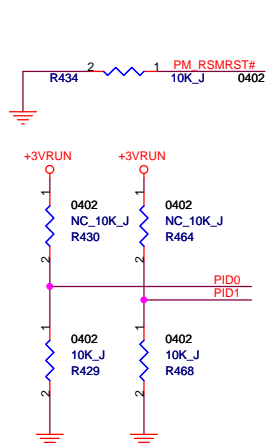
Stuff for No-reboot



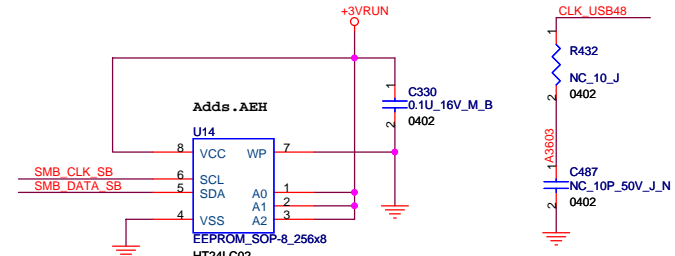
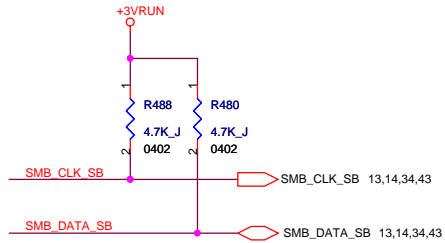
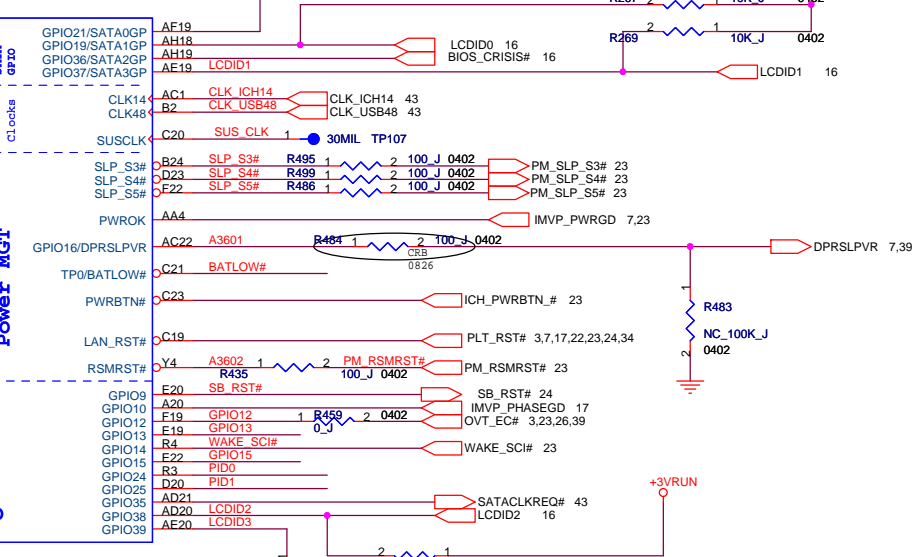
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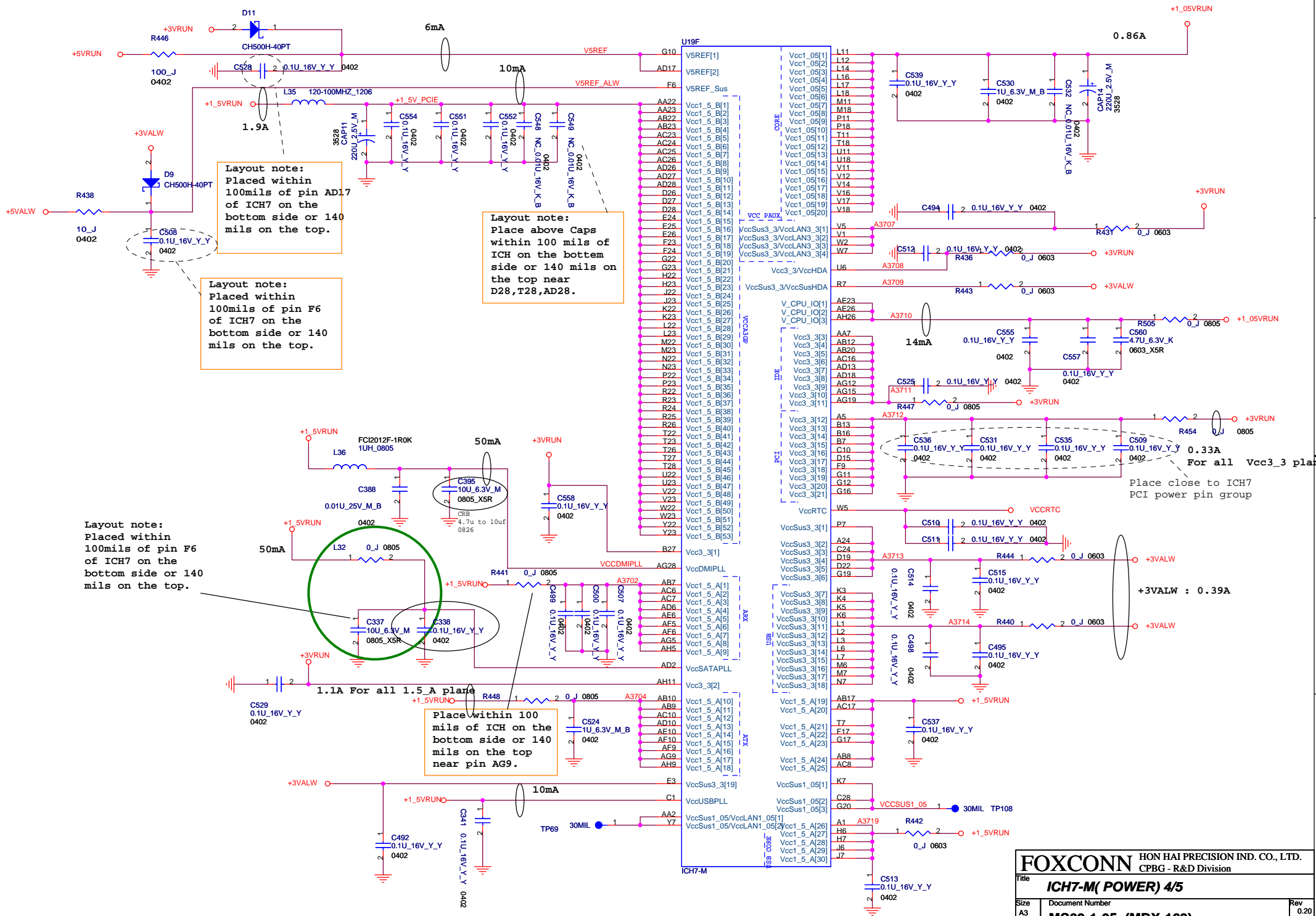


After check with SW team.
We don't use this pin but reserve to CORE power rail



80 Port I/F:
H: LPC bus
L: PCI bus





Layout note:
Placed within 100mils of pin AD1.7 of ICH7 on the bottom side or 140 mils on the top.

Layout note:
Place above Caps within 100 mils of ICH on the bottom side or 140 mils on the top near D28, T28, AD28.

Layout note:
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.

Layout note:
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.

Place within 100mils of ICH on the bottom side or 140 mils on the top near pin AG9.

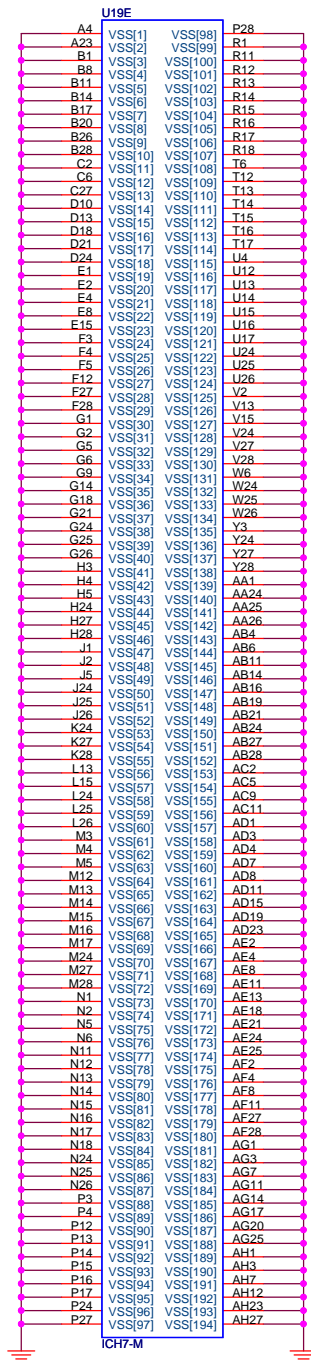
For all Vcc3_3 plane
Place close to ICH7 PCI power pin group

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Title: **ICH7-M(POWER) R/5**

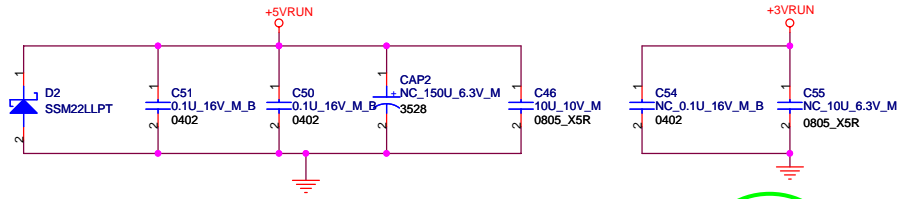
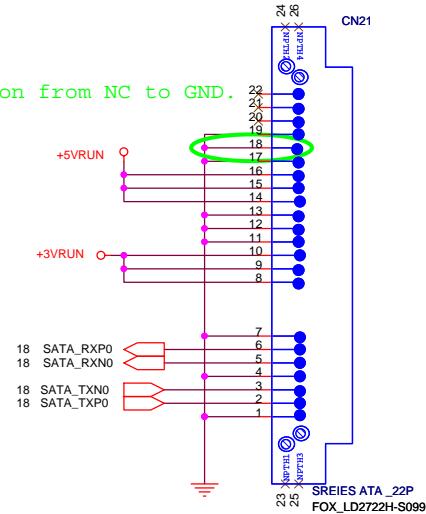
Size: A3 Document Number: **MS60-1-05 (MBX-163)** Rev: 0.20

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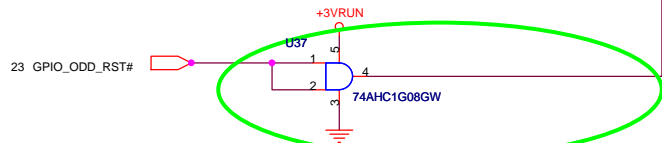
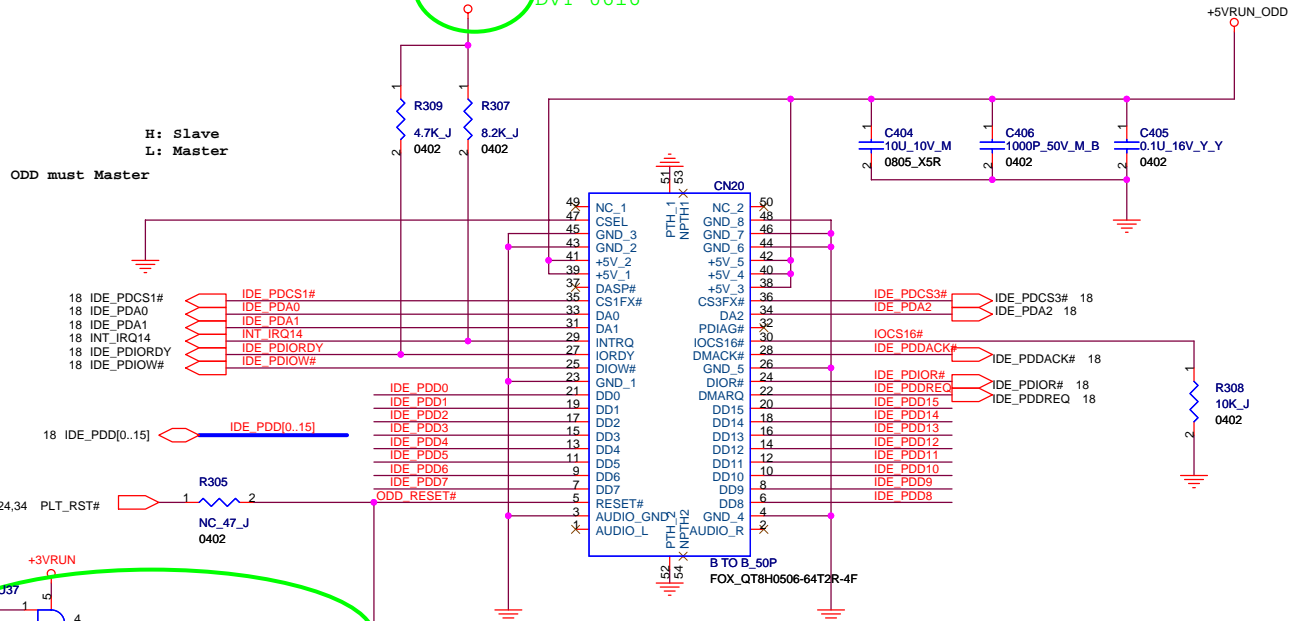


SATA HDD CONN

CN21's pin18 change connection from NC to GND.
DVT 0616

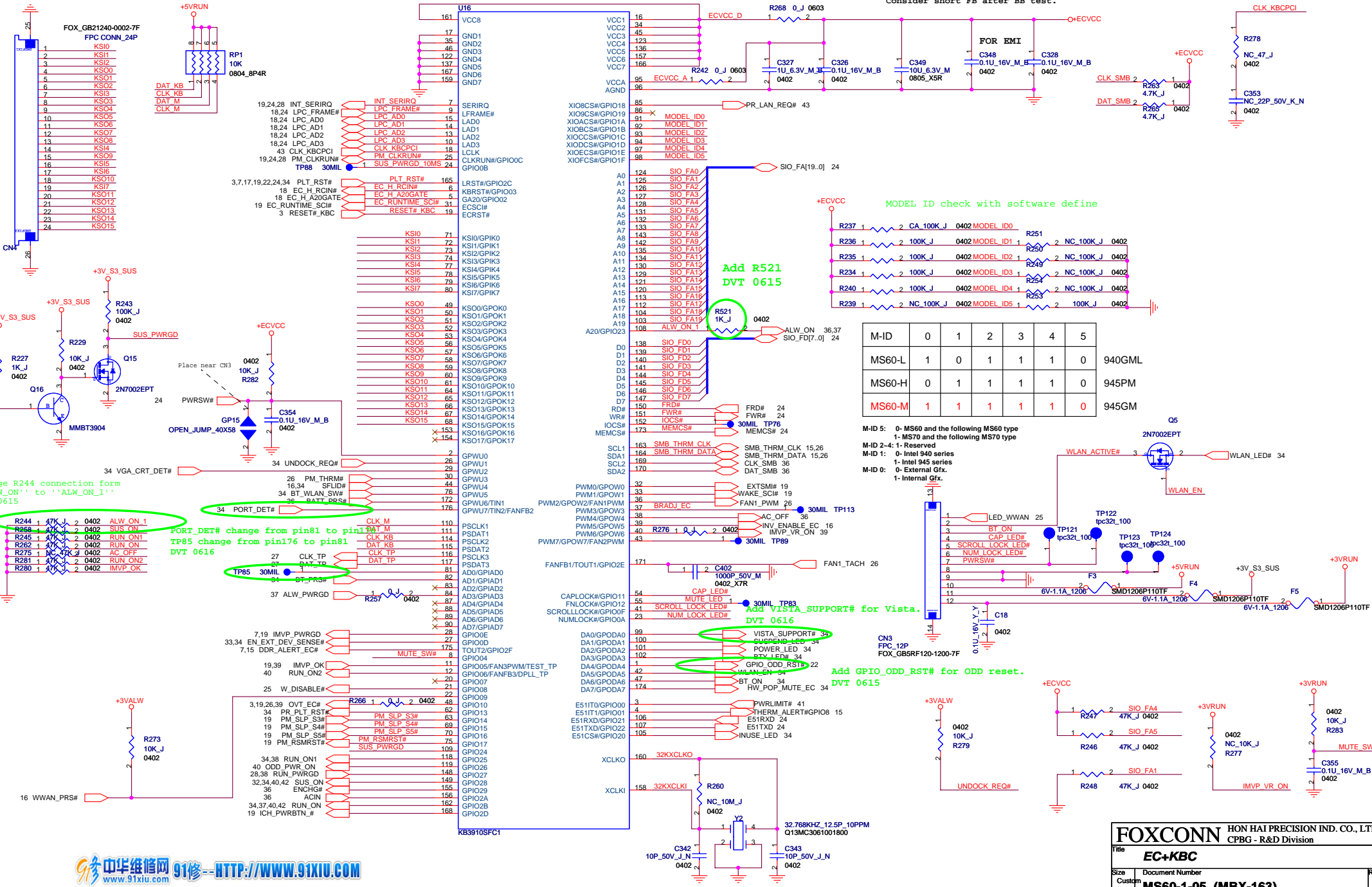


+3VRUN_ODD
Change from +3VRUN to +3VRUN_ODD
DVT 0616



Del R516,R517,C580
DVT 0615

CD-ROM CONN



M-ID	0	1	2	3	4	5	
MS60-L	1	0	1	1	1	0	940GML
MS60-H	0	1	1	1	1	0	945PM
MS60-M	1	1	1	1	1	0	945GM

- M-ID 5: 0- MS60 and the following MS60 type
- 1- MS70 and the following MS70 type
- M-ID 2-4: 1- Reserved
- M-ID 1: 0- Intel 940 series
1- Intel 945 series
- M-ID 0: 0- External Gfx.
1- Internal Gfx.

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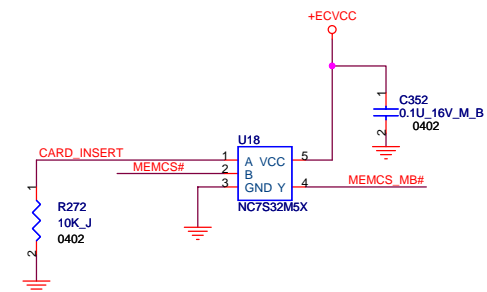
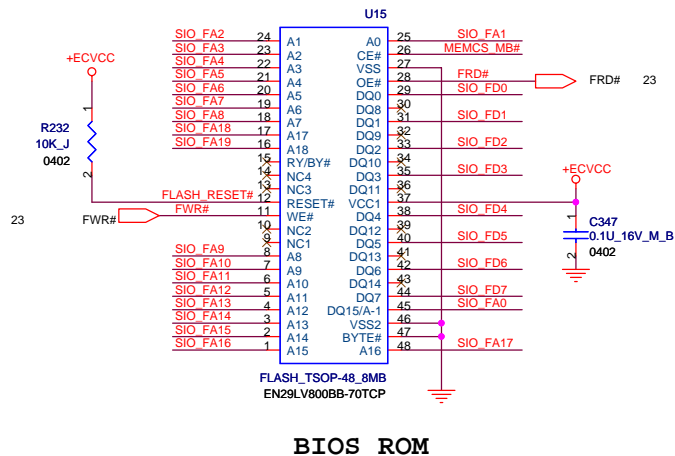
Title: **EC+KBC**

Size: Document Number
Customer: **MS60-1-05 (MBX-163)** Rev: 0.20

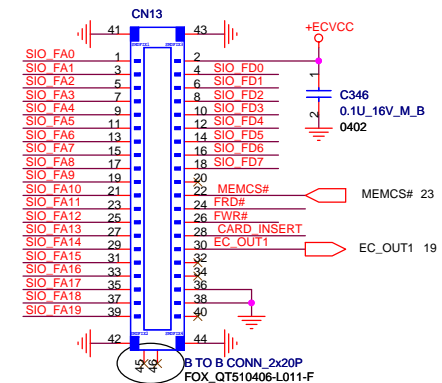
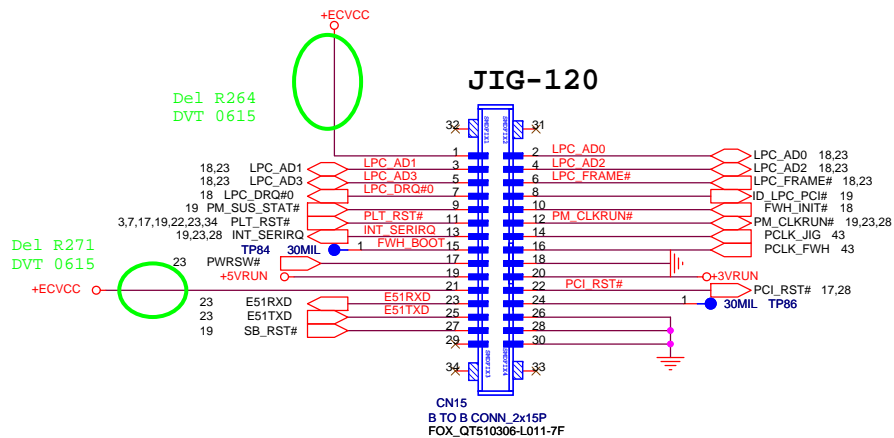
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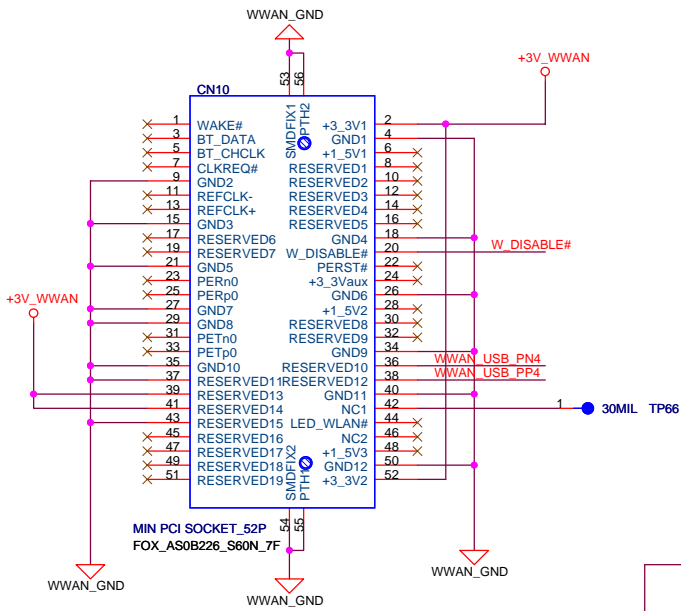
23 SIO_FA[19..0]

23 SIO_FD[7..0]

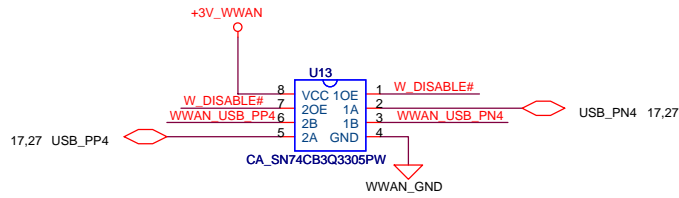
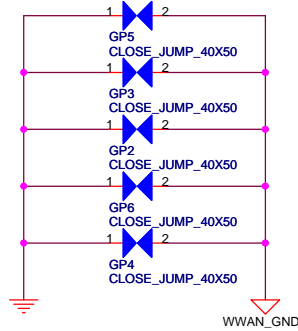


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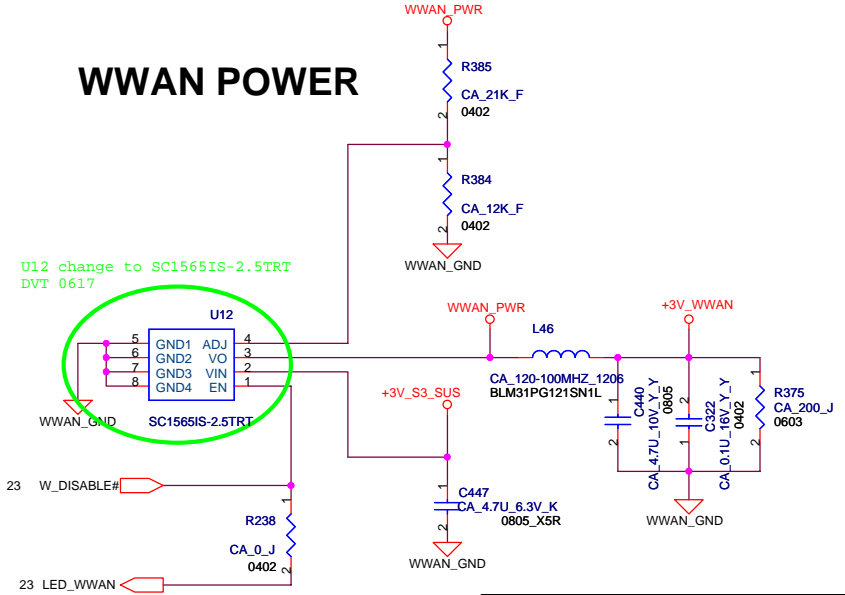




MIN PCI SOCKET_52P
FOX_AS0B226_S60N_7F



WWAN POWER

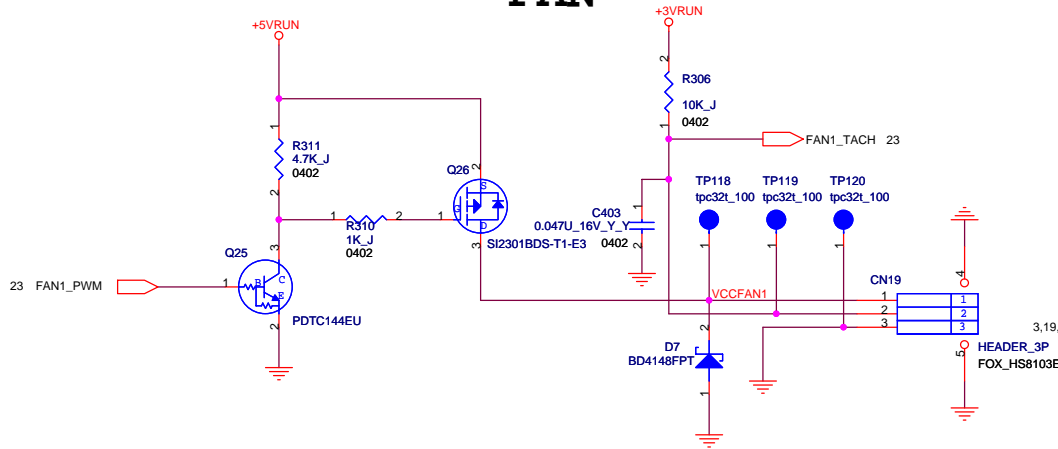


U12 change to SC1565IS-2.5TRT
DVT 0617

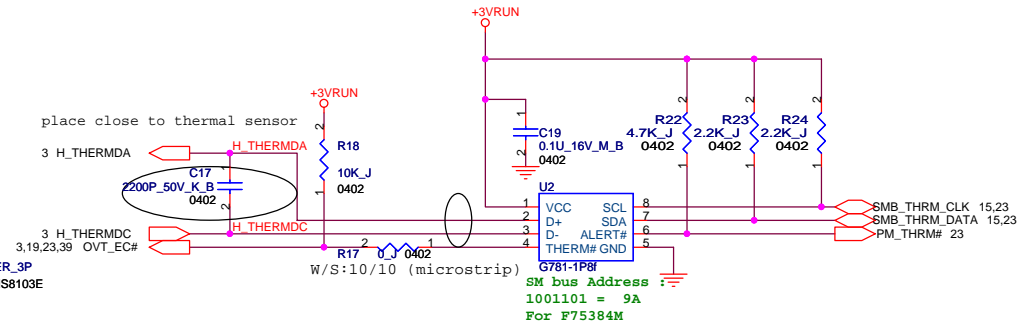
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FOXCONN		HON HAI PRECISION IND. CO., LTD.	
		CPBG - R&D Division	
Title WWAN			
Size	Document Number	Rev	
Custom	MS60-1-05 (MBX-163)	0.20	
Date:	Monday, June 19, 2006	Sheet	25 of 47

FAN



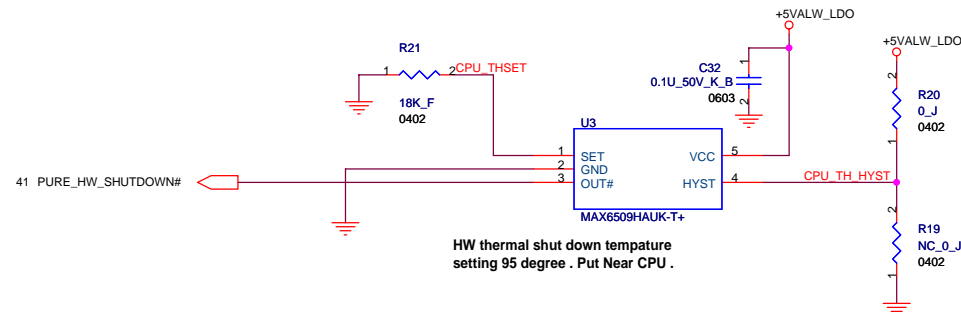
CPU SENSOR



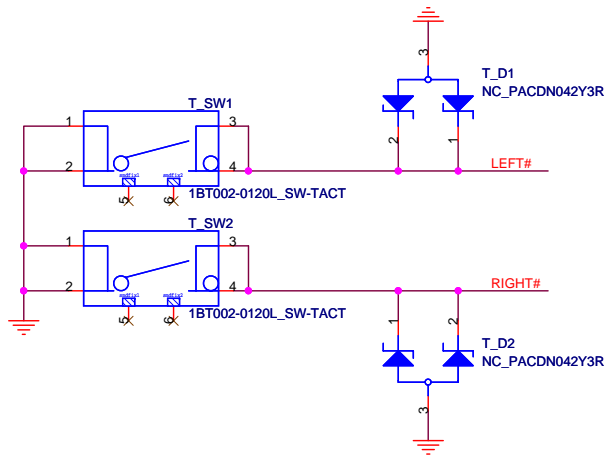
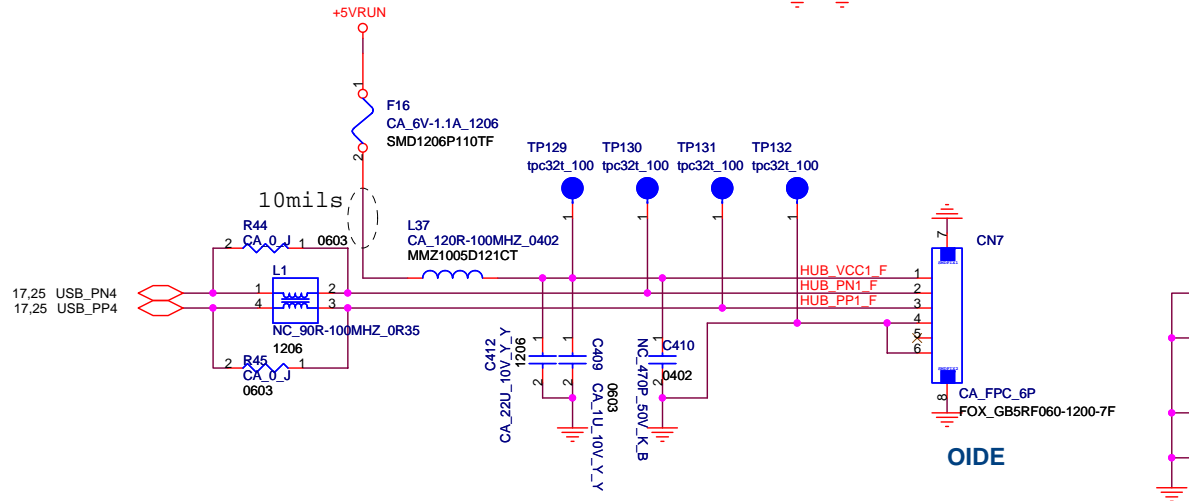
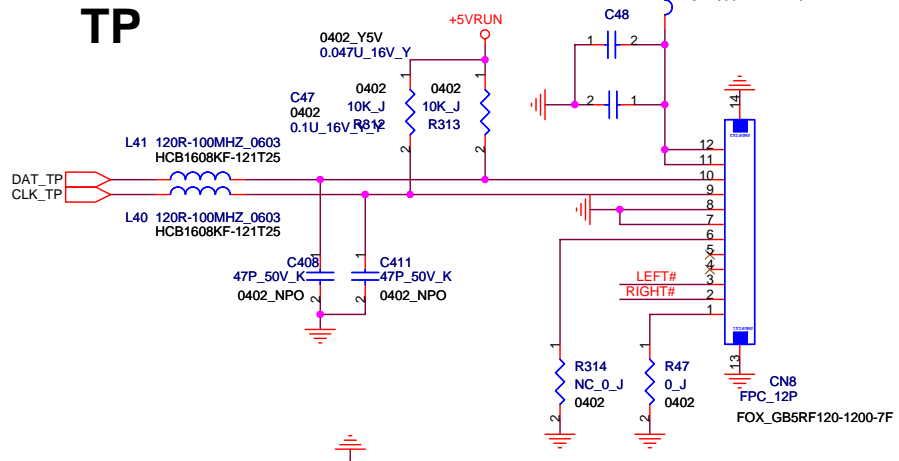
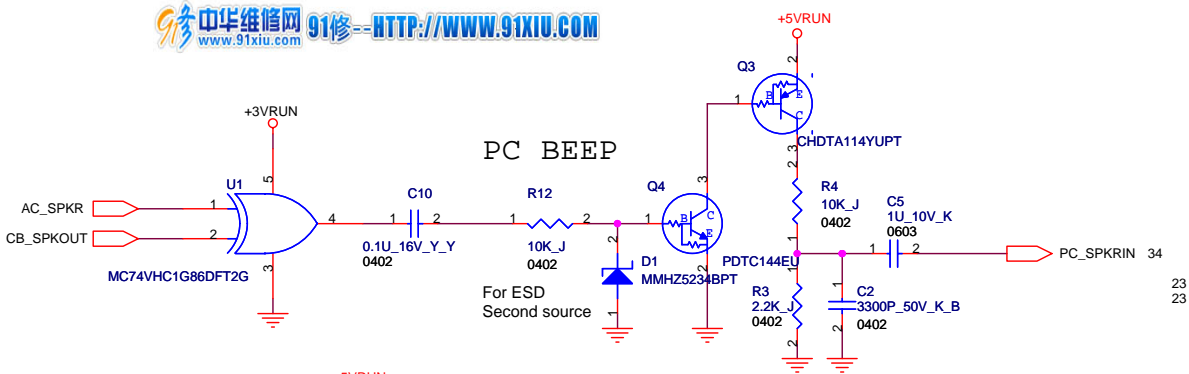
Place Thermal-Sensor near CPU & GMCH.

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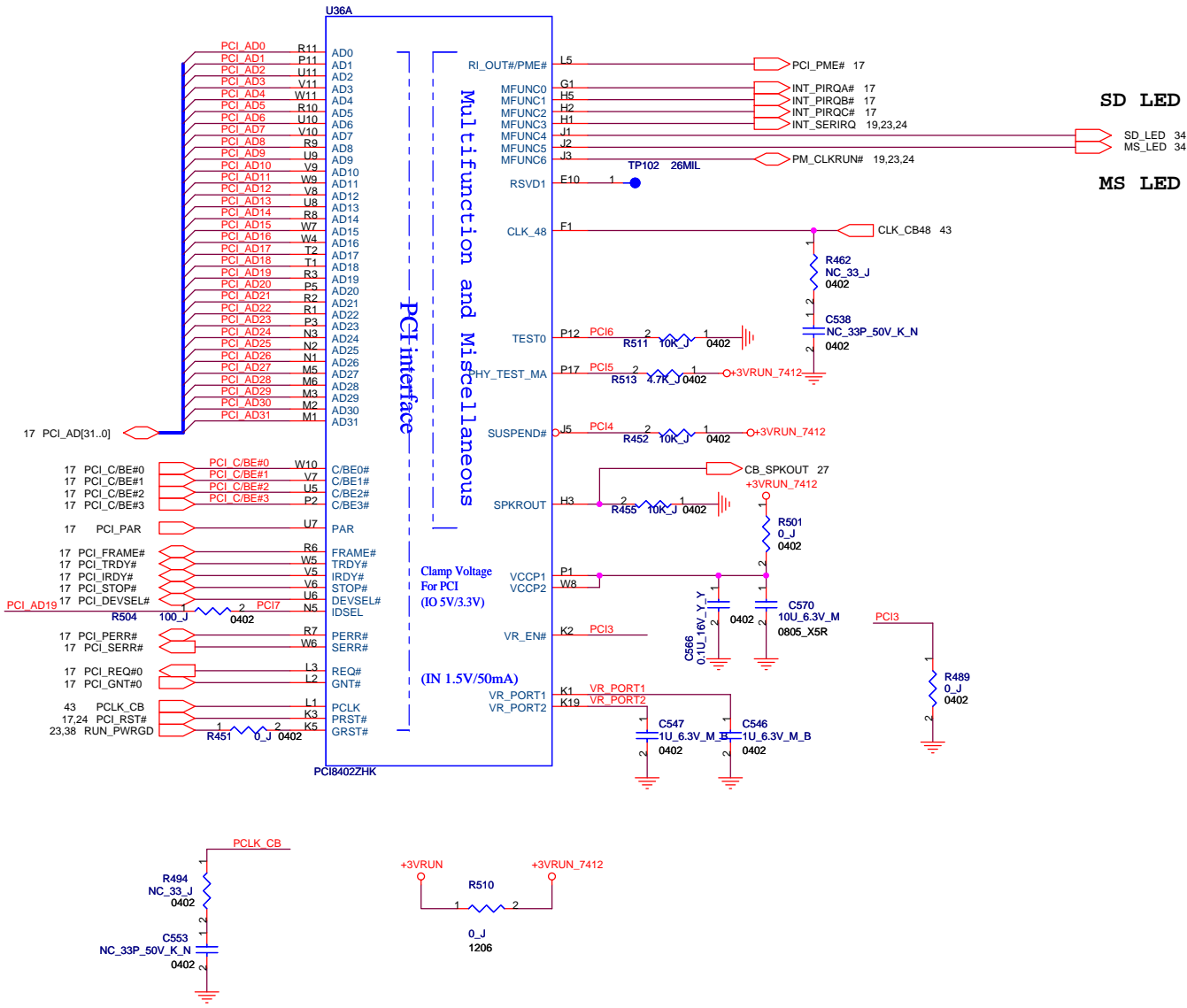
HW THERMAL PROTECTION

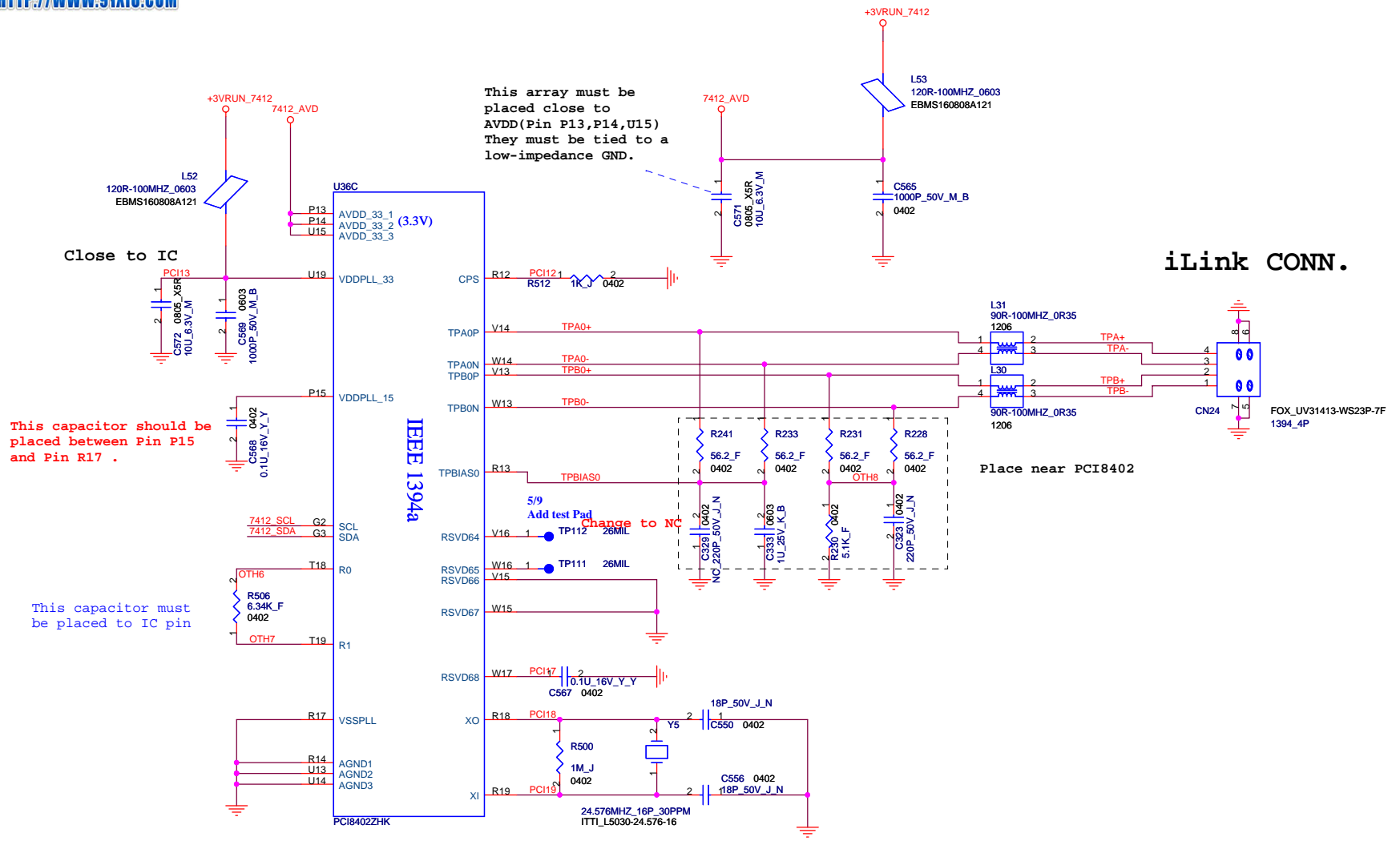


FOXCONN		HON HAI PRECISION IND. CO., LTD.	
Title		CPBG - R&D Division	
FAN/HW THERMAL PROTECT			
Size	Document Number	Rev	
A3	MS60-1-05 (MBX-163)	0.20	
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FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title OIDE/TP		
Size Custom	Document Number MS60-1-05 (MBX-163)	Rev 0.20
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This array must be placed close to AVDD(Pin P13,P14,U15) They must be tied to a low-impedance GND.

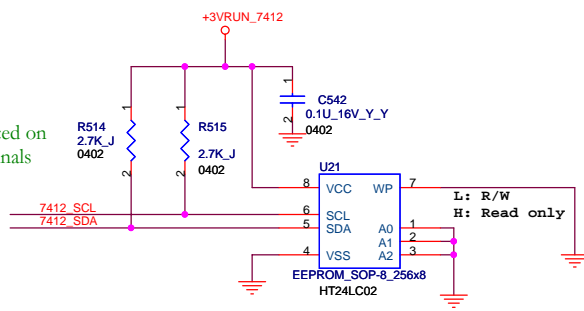
Close to IC

This capacitor should be placed between Pin P15 and Pin R17 .

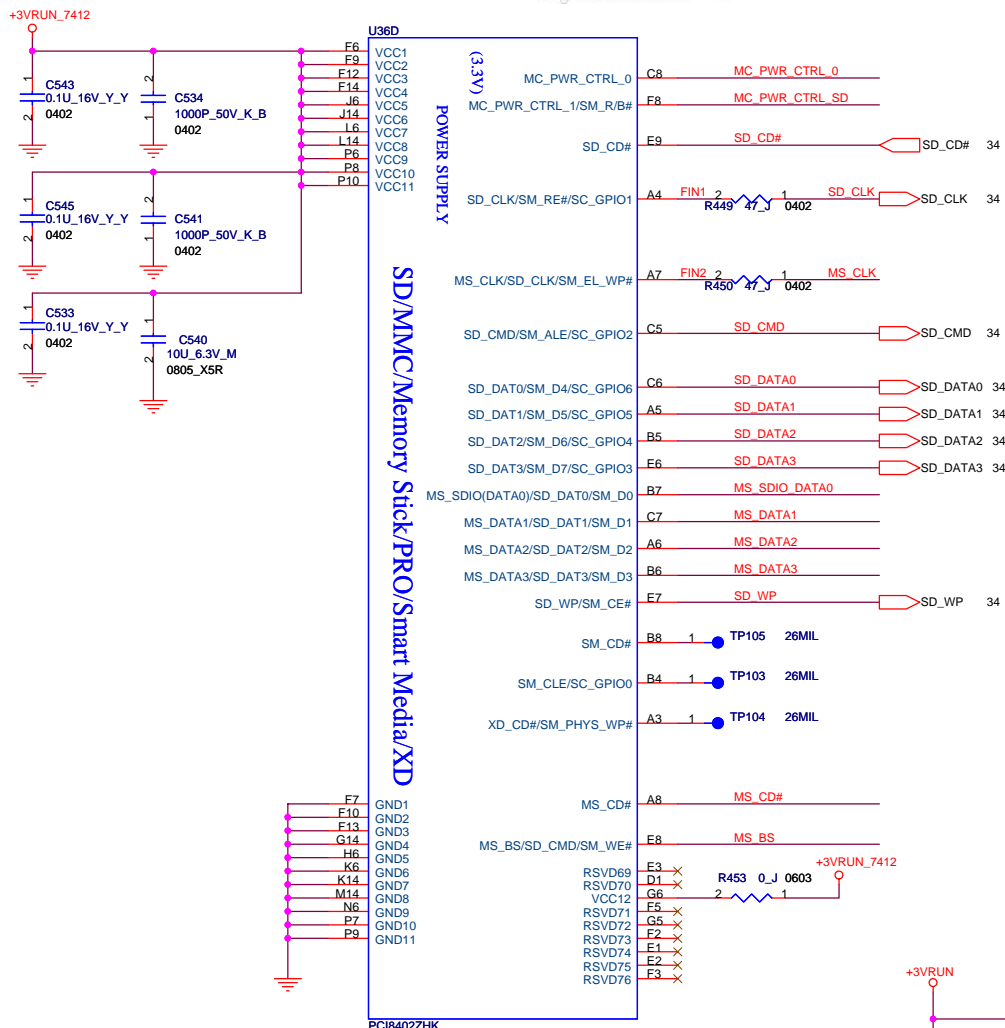
This capacitor must be placed to IC pin

Place near PCI8402

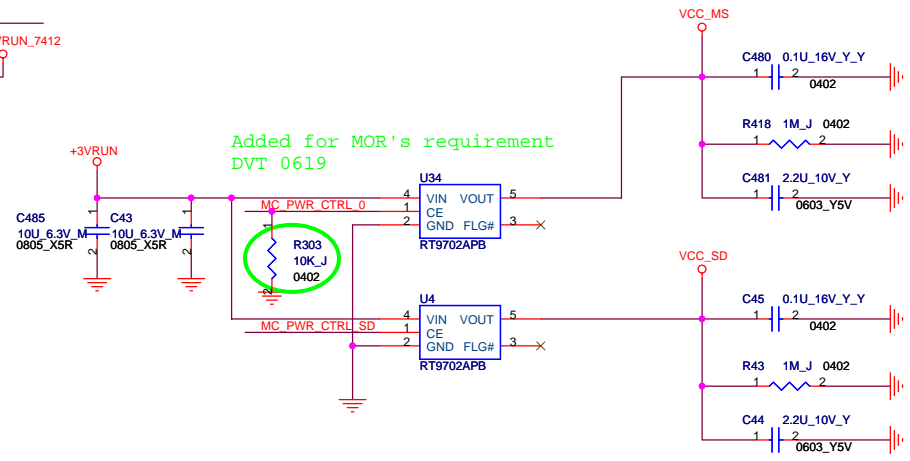
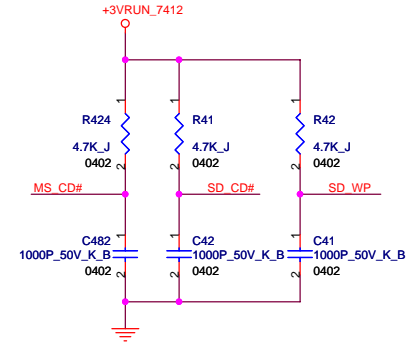
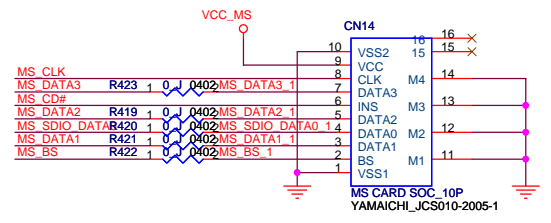
Resistors should be placed on the SCL and SDA terminals

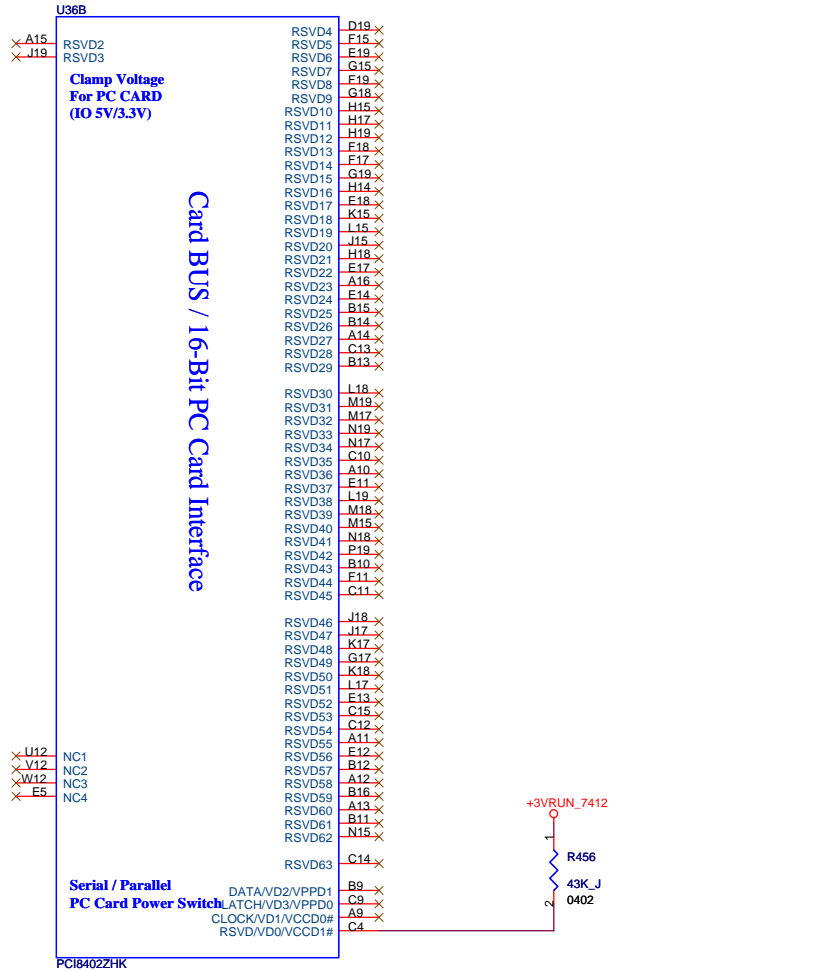


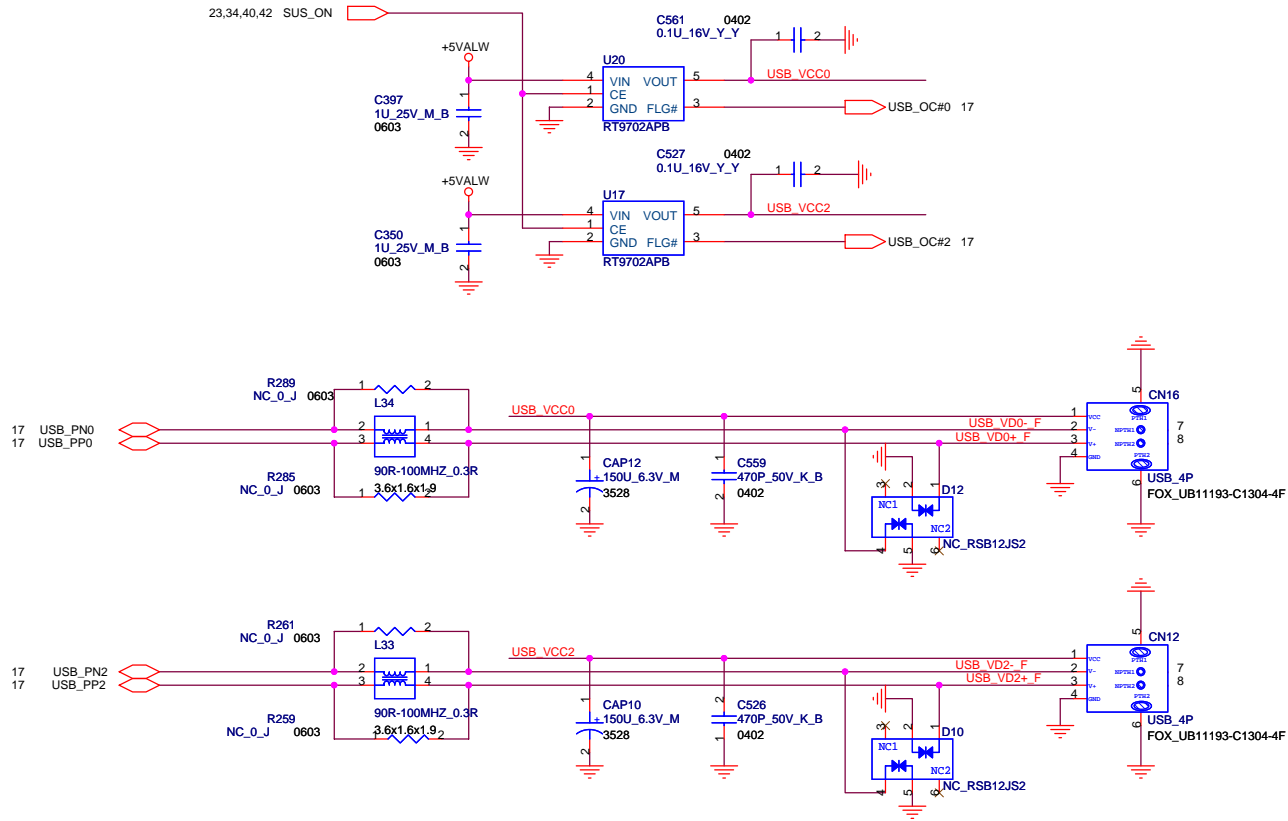
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Title PCI (I LINK)	
Size A3	Document Number MS60-1-05 (MBX-163)
Date: Monday, June 19, 2006	Sheet 29 of 47
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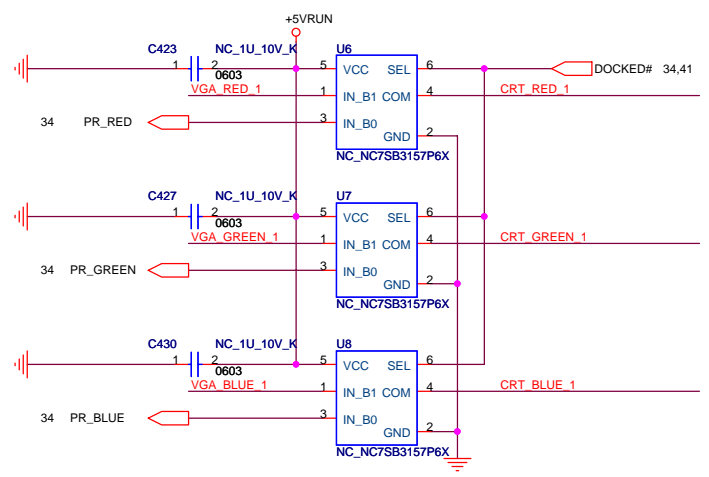
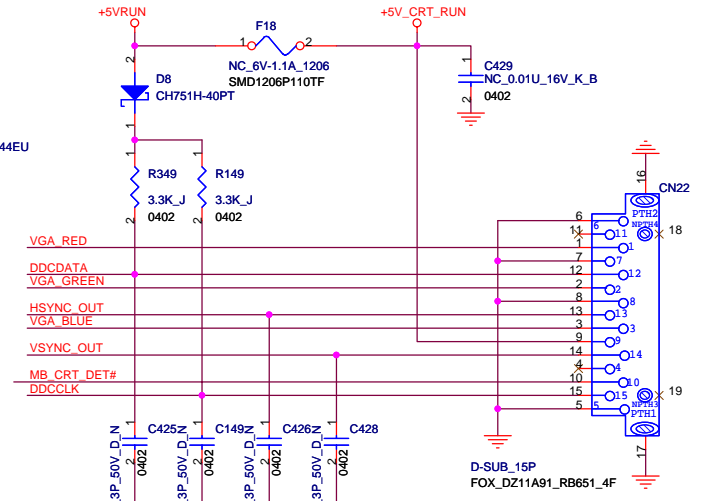
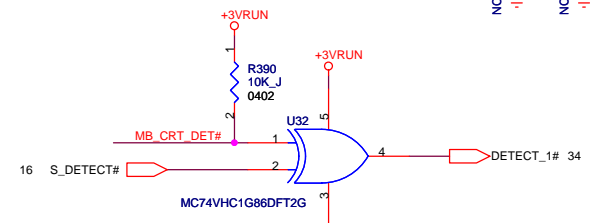
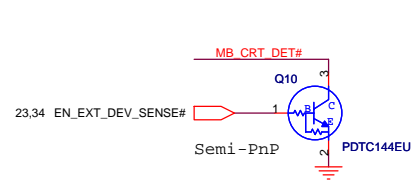
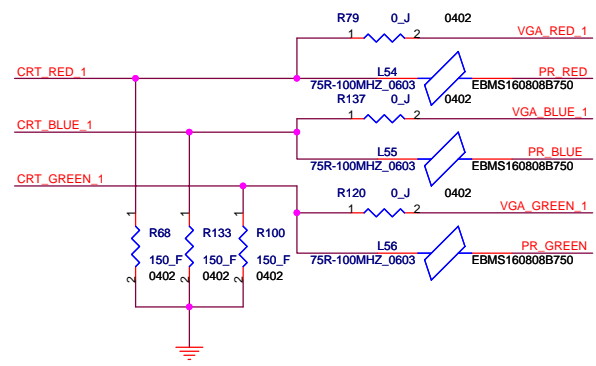
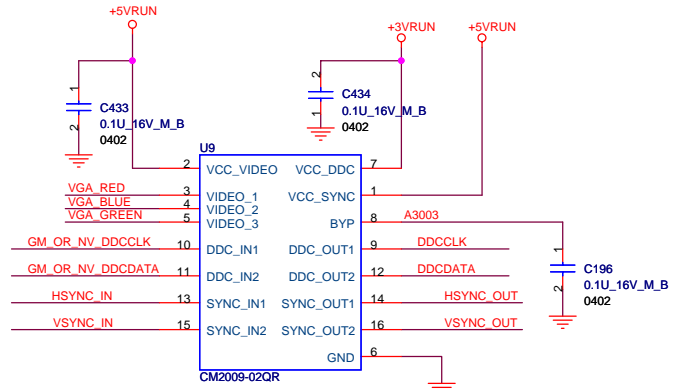
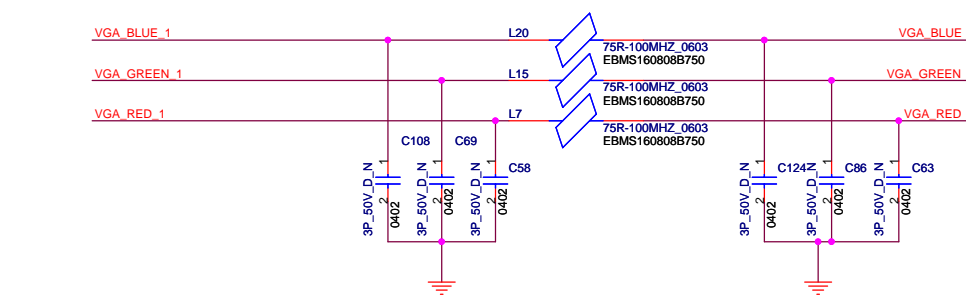
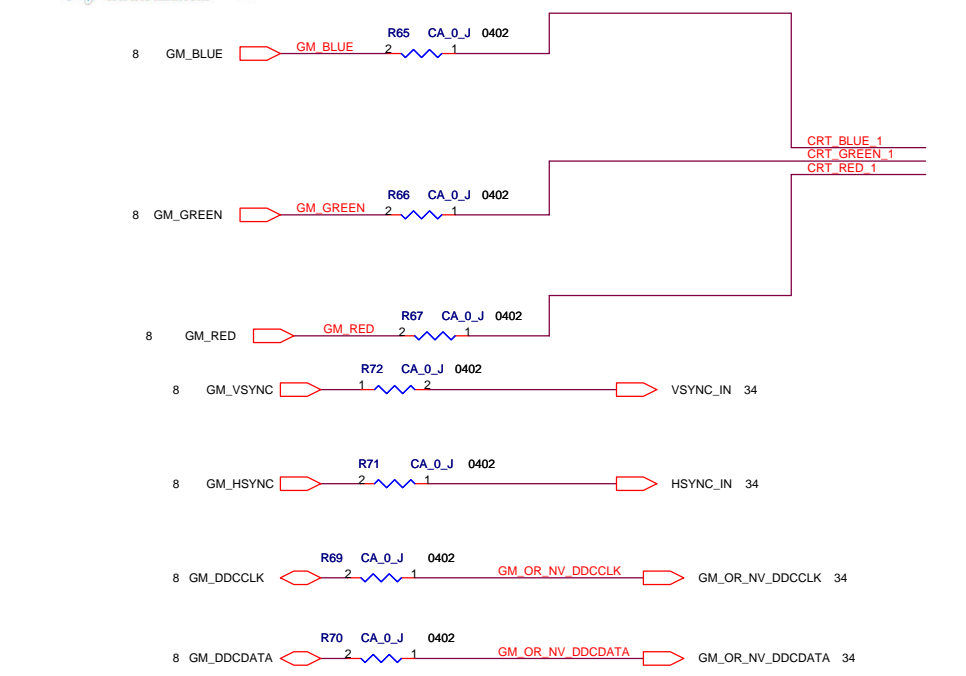


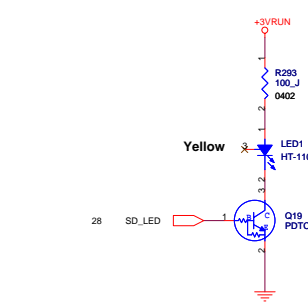
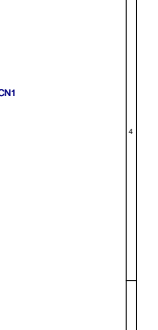
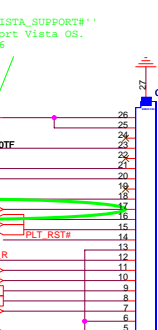
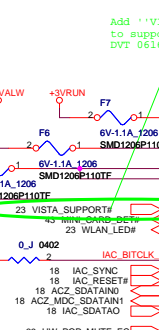
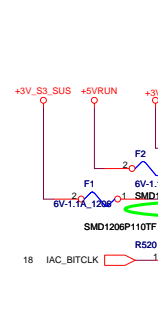
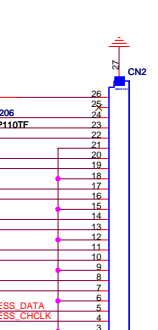
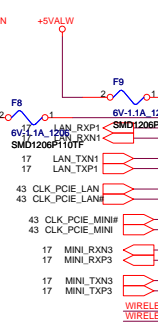
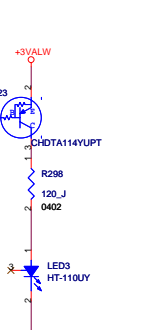
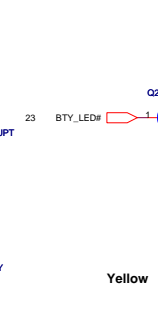
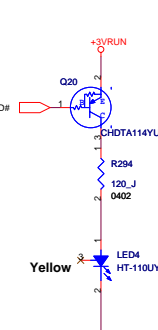
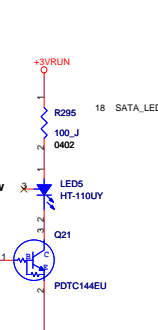
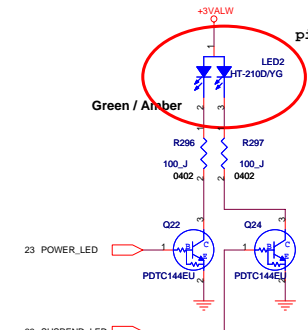
MS Duo / Pro



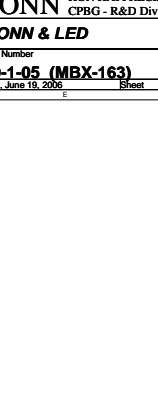
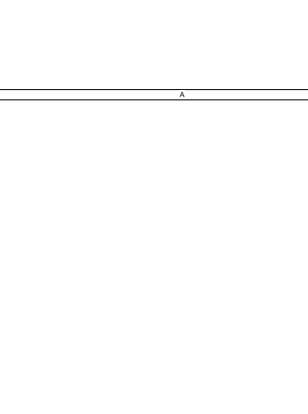
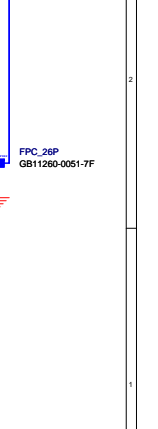
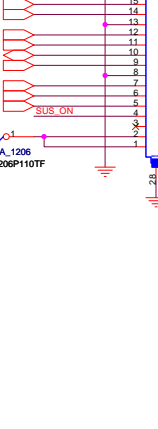
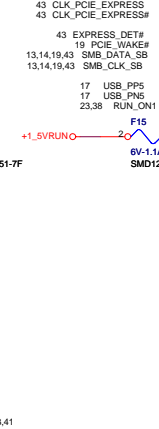
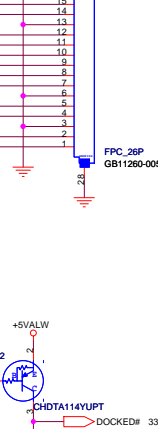
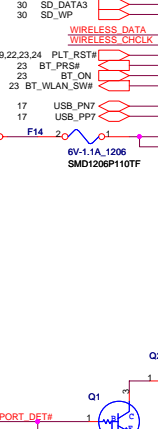
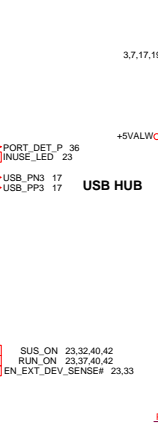
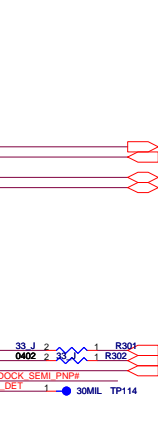
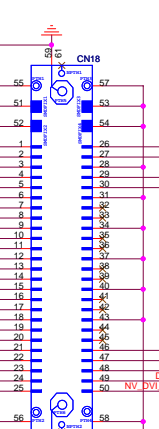
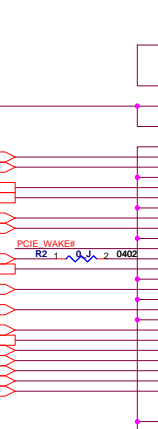
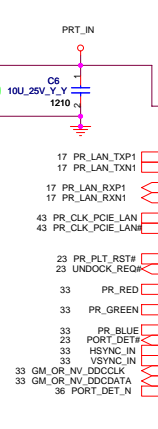
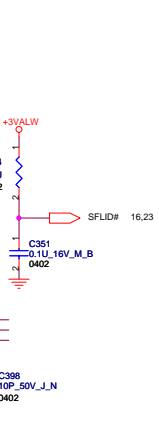
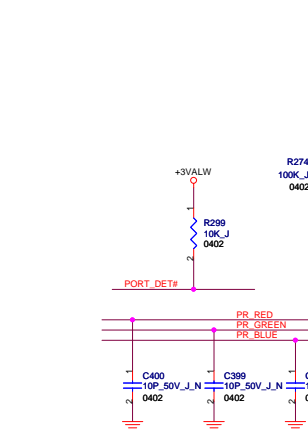






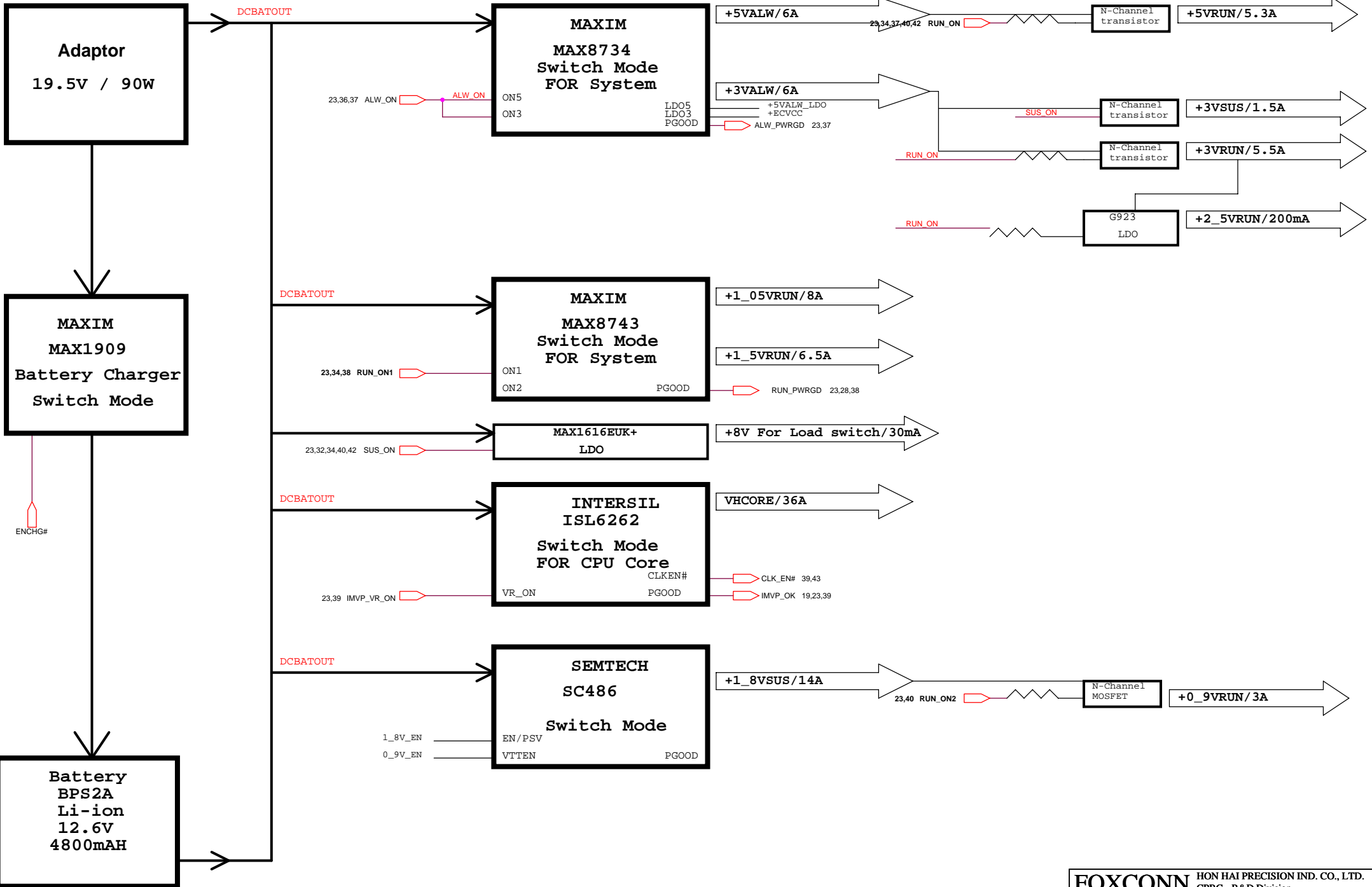
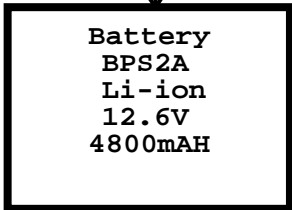
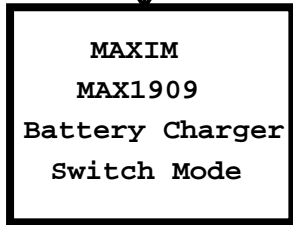
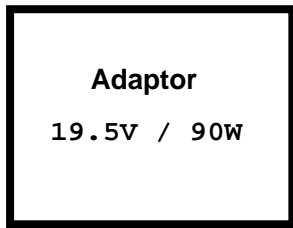


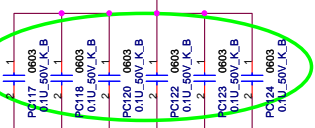
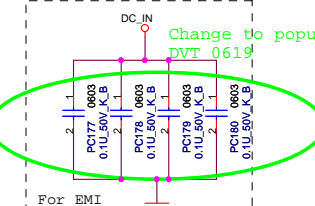
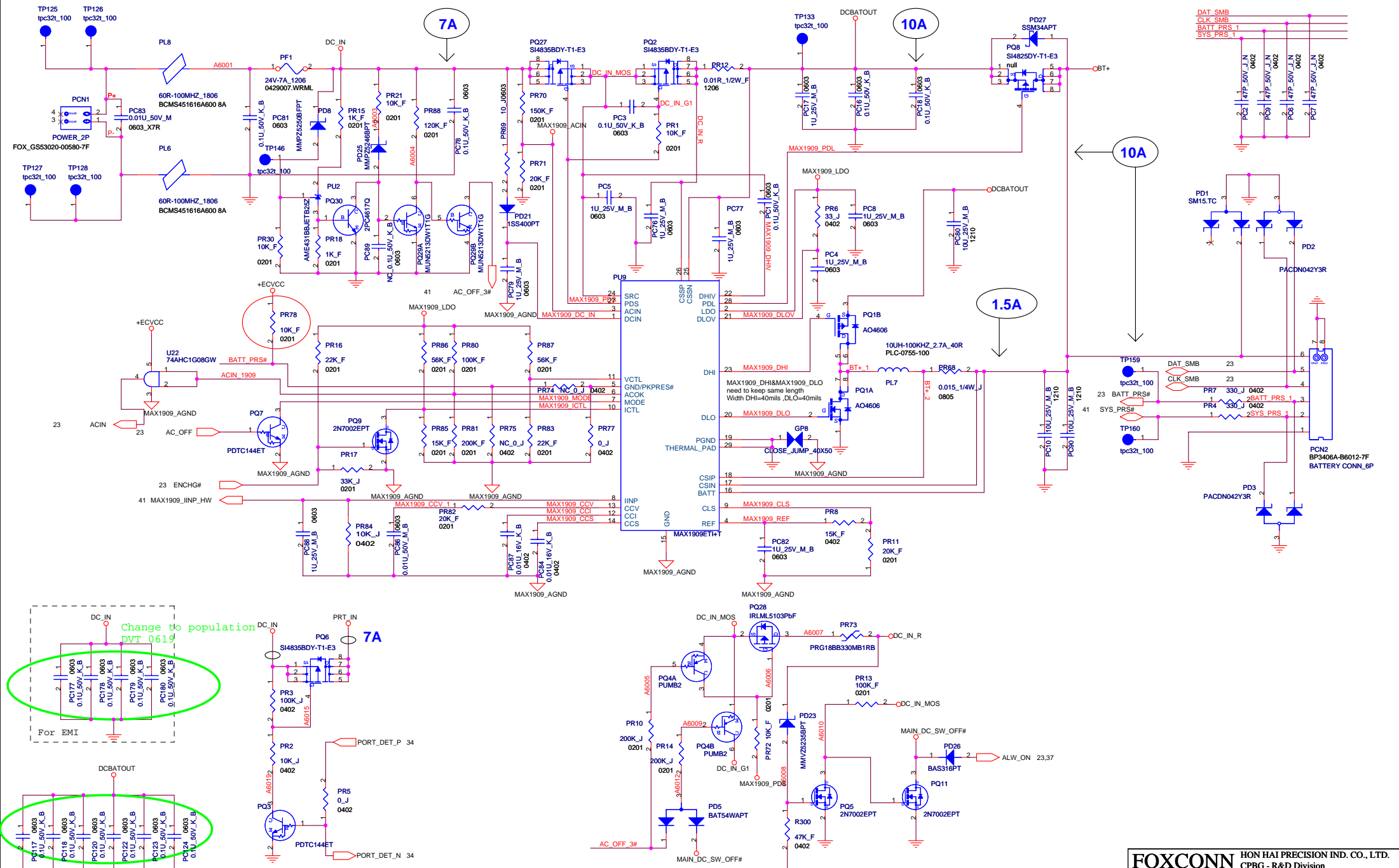
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www.91xiu.com



Replicator Port

FOXCONN HON HAI PRECISION IND. CO., LTD.	
CPBG - R&D Division	
Title DB CONN & LED	
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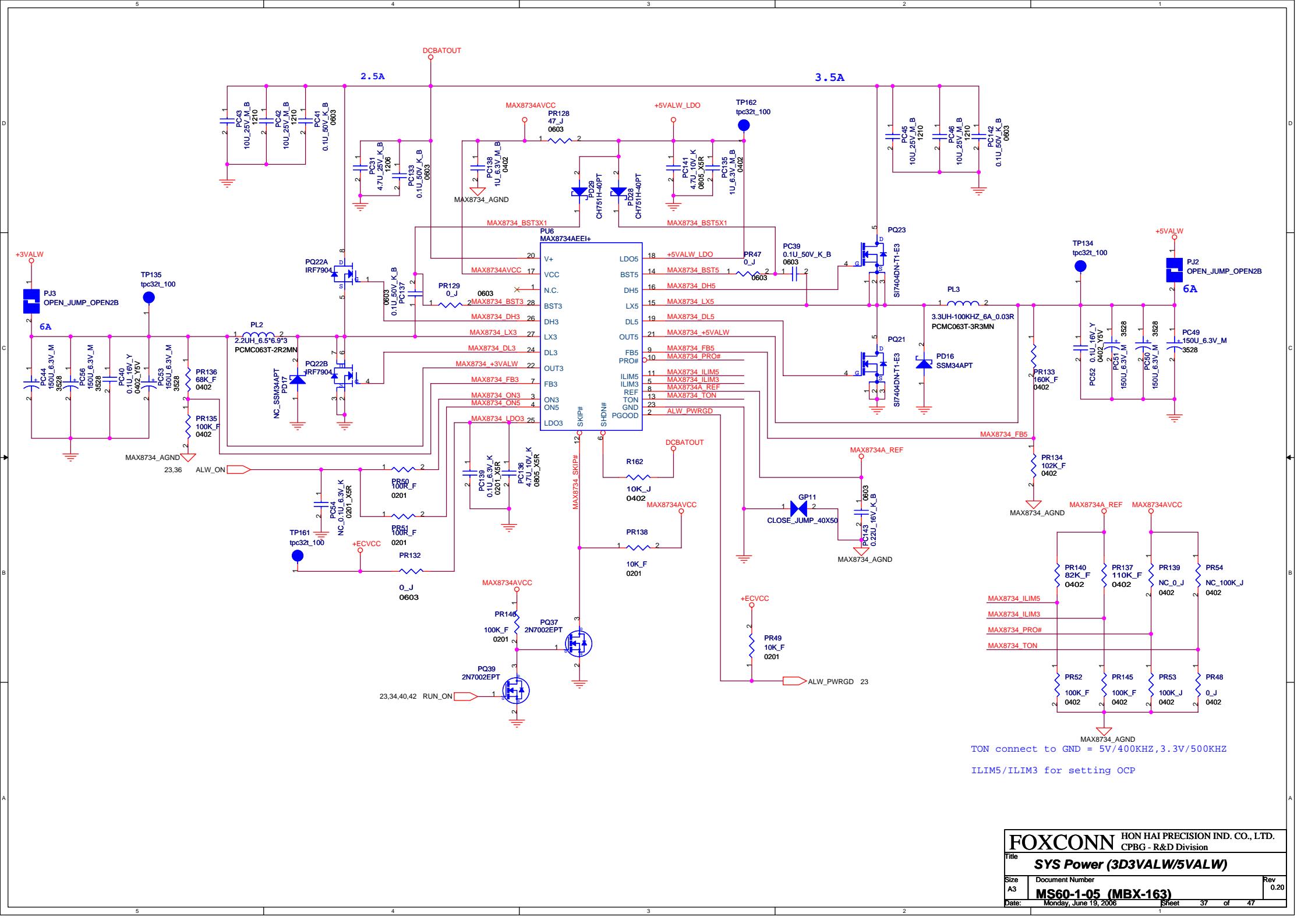




Change to population
DWT 0619

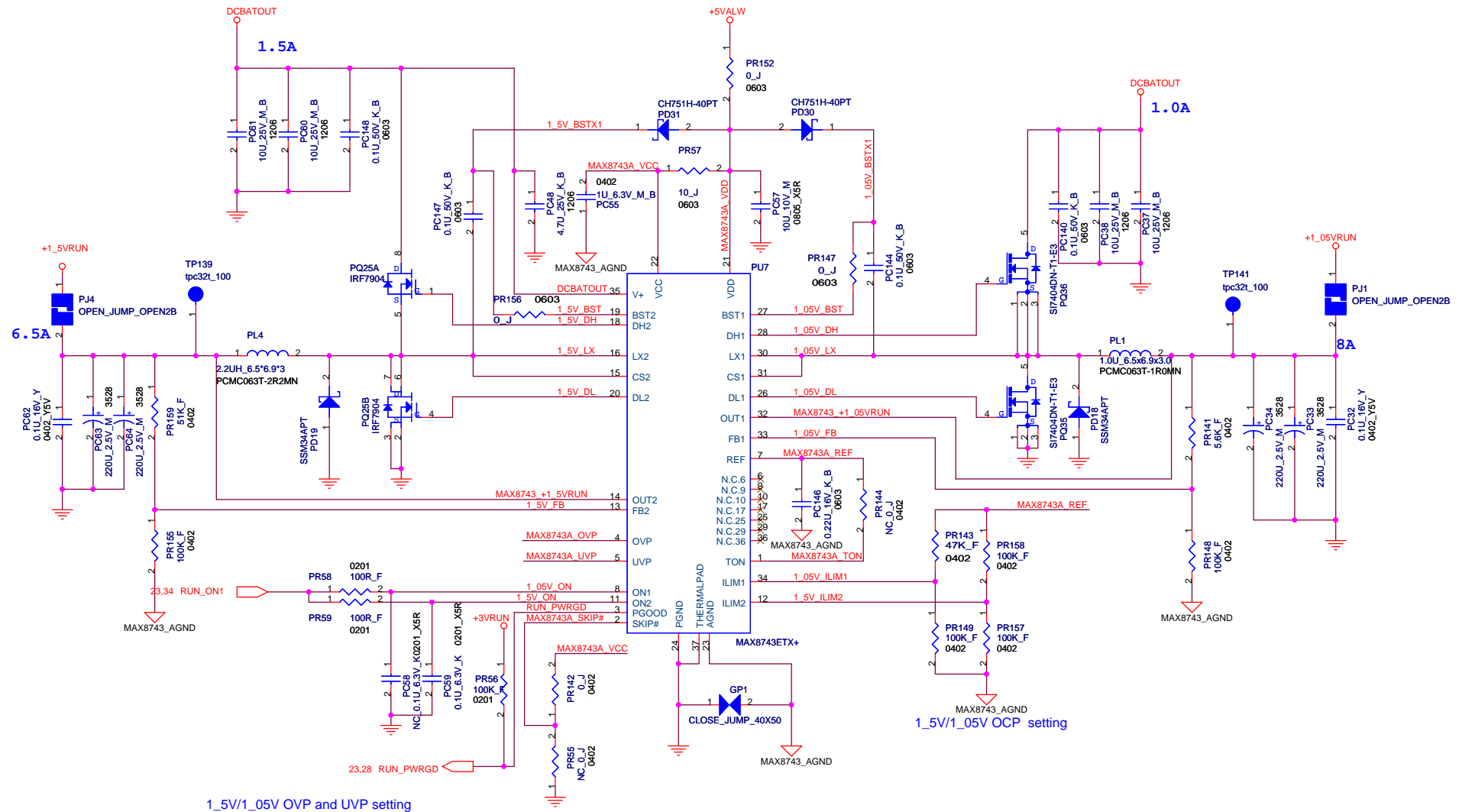
For EMI

Added for EMI
DWT 0619

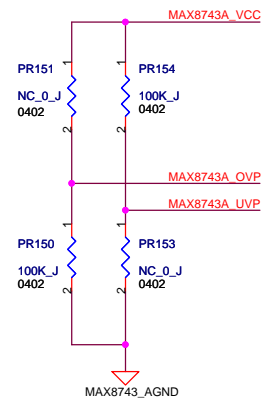


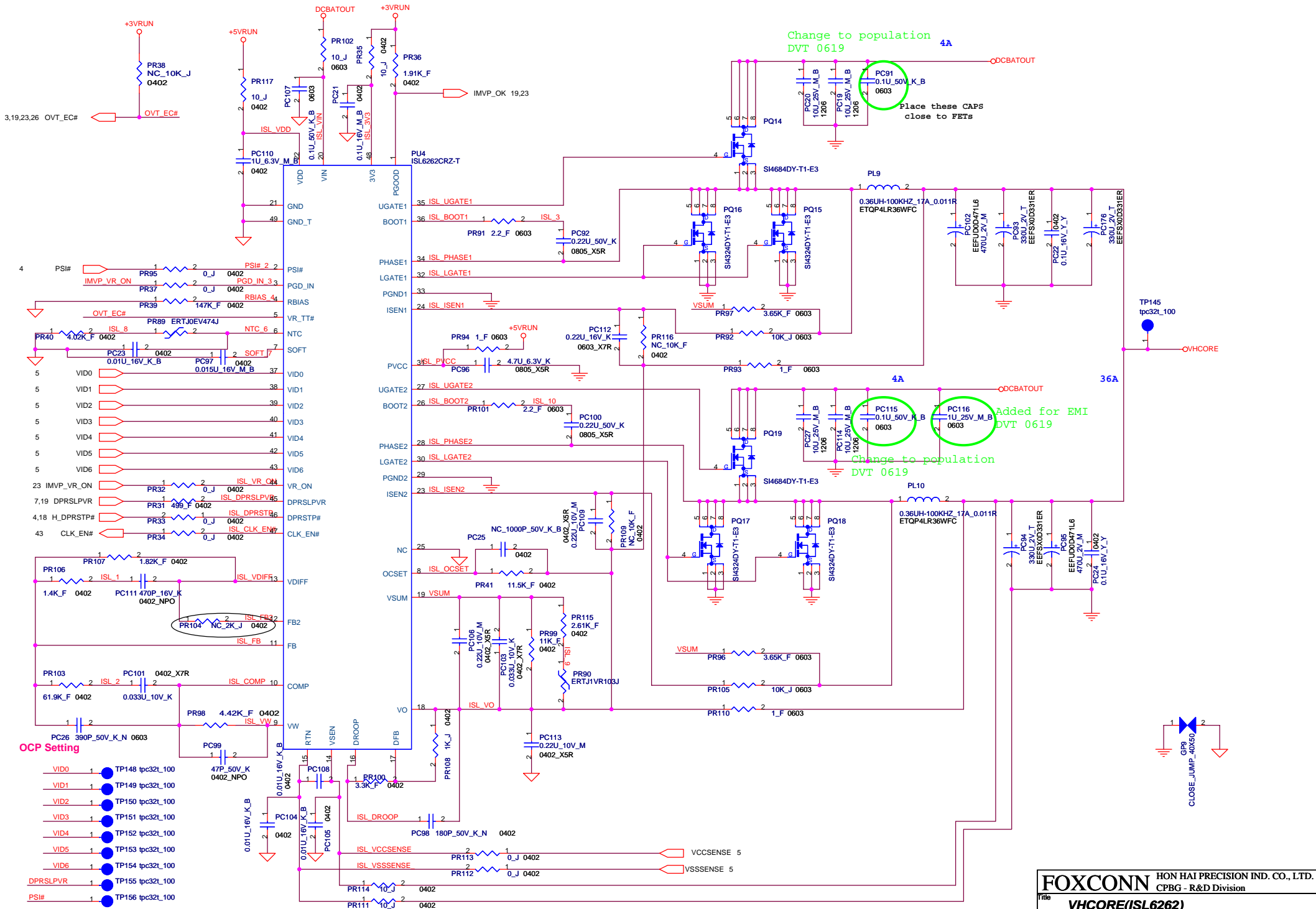
TON connect to GND = 5V/400KHZ, 3.3V/500KHZ
 ILIM5/ILIM3 for setting OCP

FOXCONN HON HAI PRECISION IND. CO., LTD. CPBG - R&D Division		
Title SYS Power (3D3VALW/5VALW)		
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1.5V/1.05V OVP and UVP setting





Change to population
DVT 0619

Place these CAPS
close to FETs

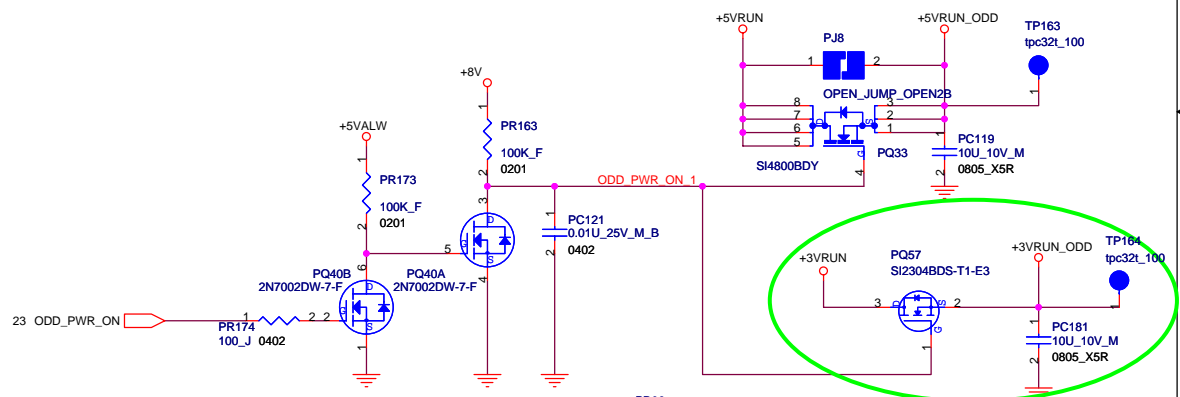
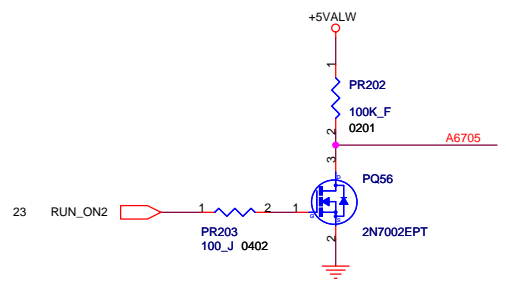
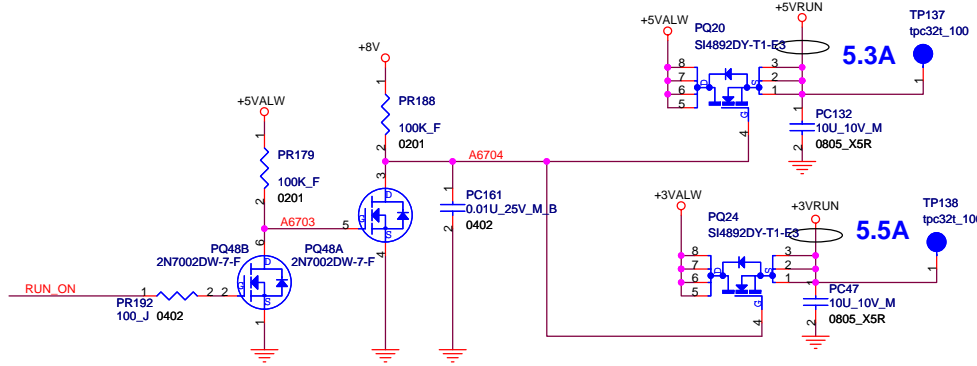
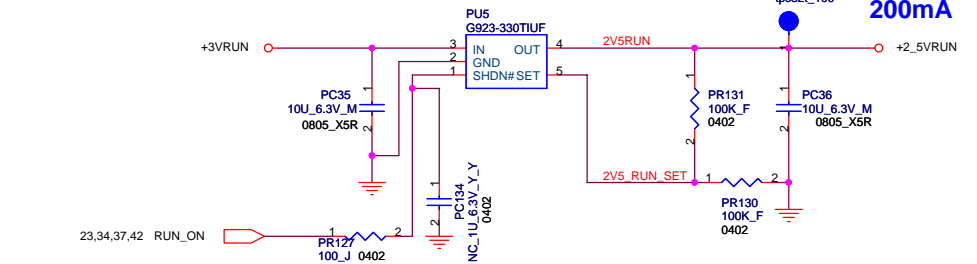
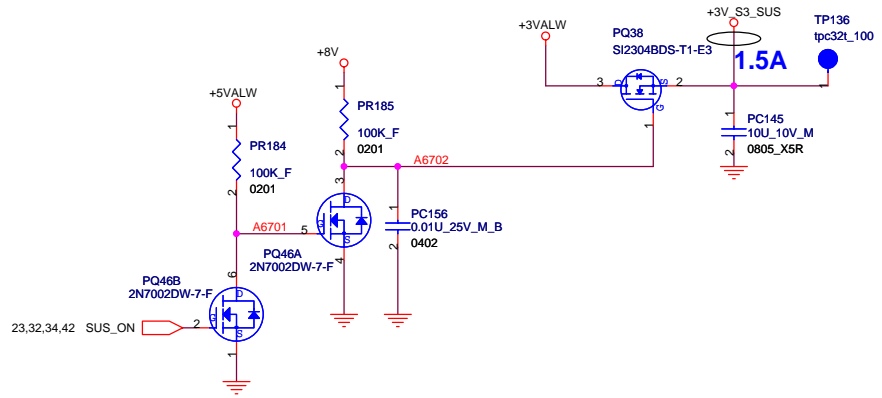
Added for EMI
DVT 0619

Change to population
DVT 0619

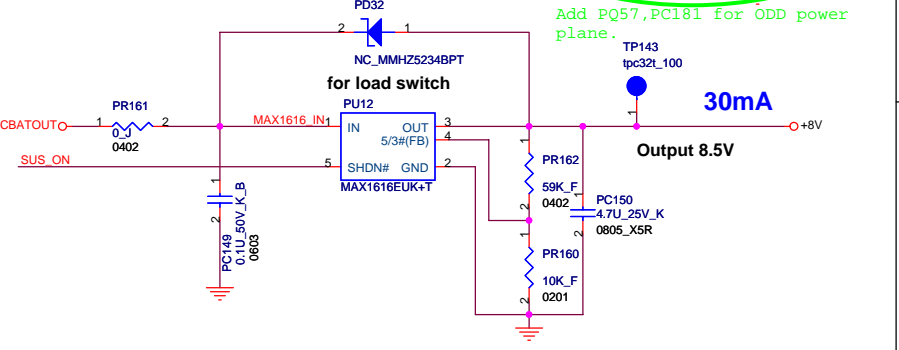
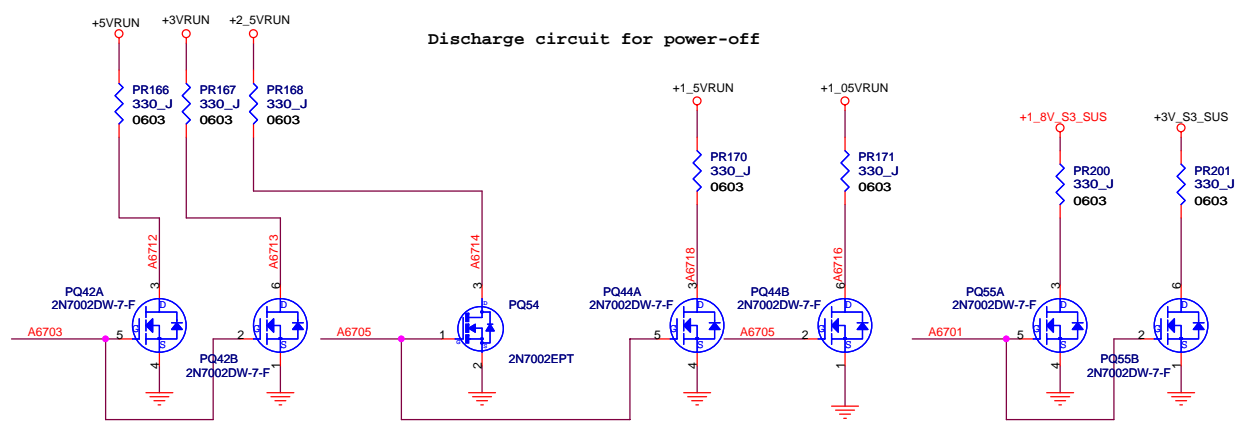
OCP Setting

- VID0 1 TP148 tpc32t_100
- VID1 1 TP149 tpc32t_100
- VID2 1 TP150 tpc32t_100
- VID3 1 TP151 tpc32t_100
- VID4 1 TP152 tpc32t_100
- VID5 1 TP153 tpc32t_100
- VID6 1 TP154 tpc32t_100
- DPRSPLVR 1 TP155 tpc32t_100
- PSI# 1 TP156 tpc32t_100
- IMVP_VR_ON 1 TP157 tpc32t_100
- H_DPRSSTP# 1 TP158 tpc32t_100

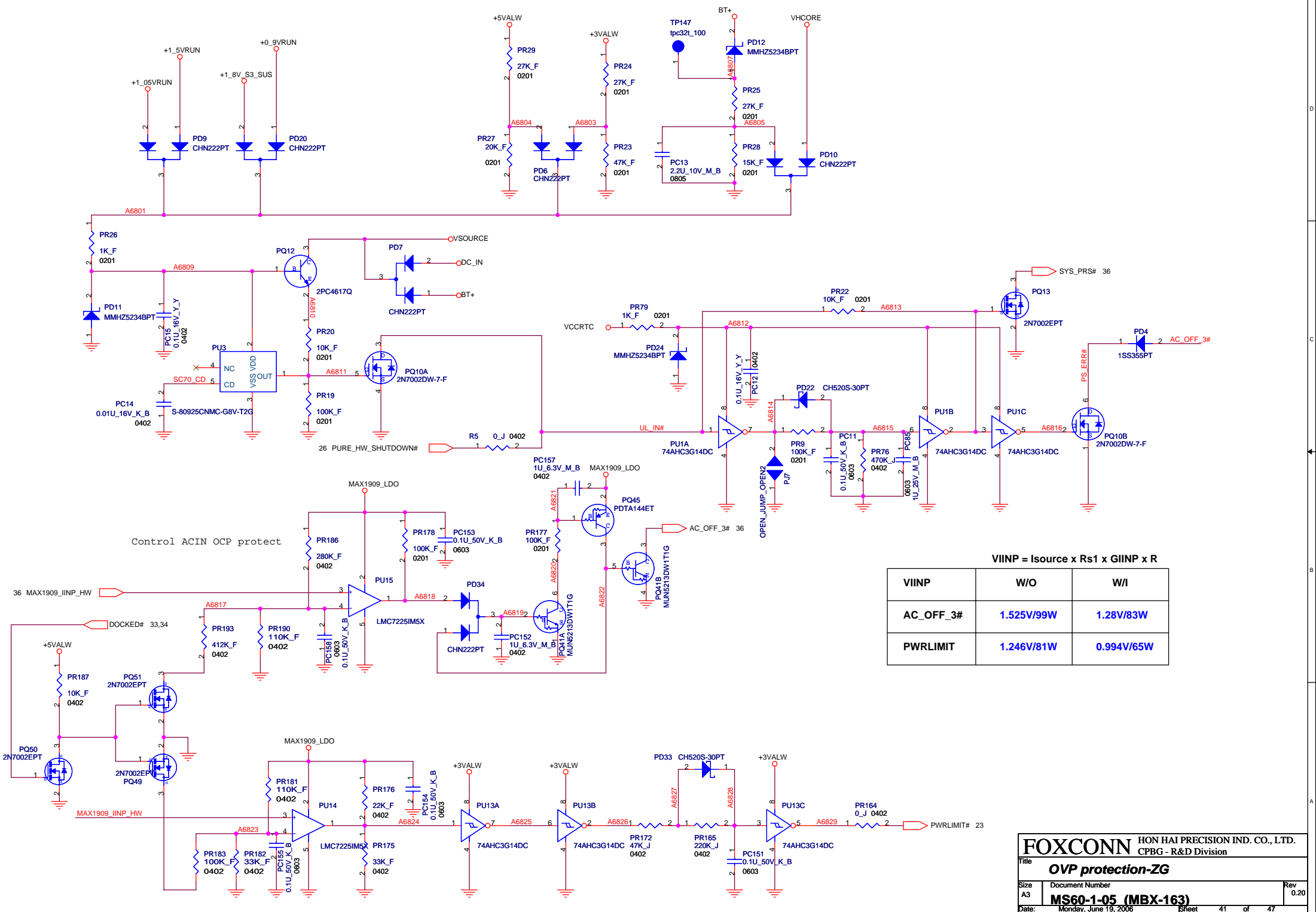
FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
File	VHCORE (ISL6262)	
Size	Document Number	Rev
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Discharge circuit for power-off



Add PQ57, PC181 for ODD power plane.



Control ACIN OCP protect

$$VIINP = I_{source} \times R_{s1} \times GIINP \times R$$

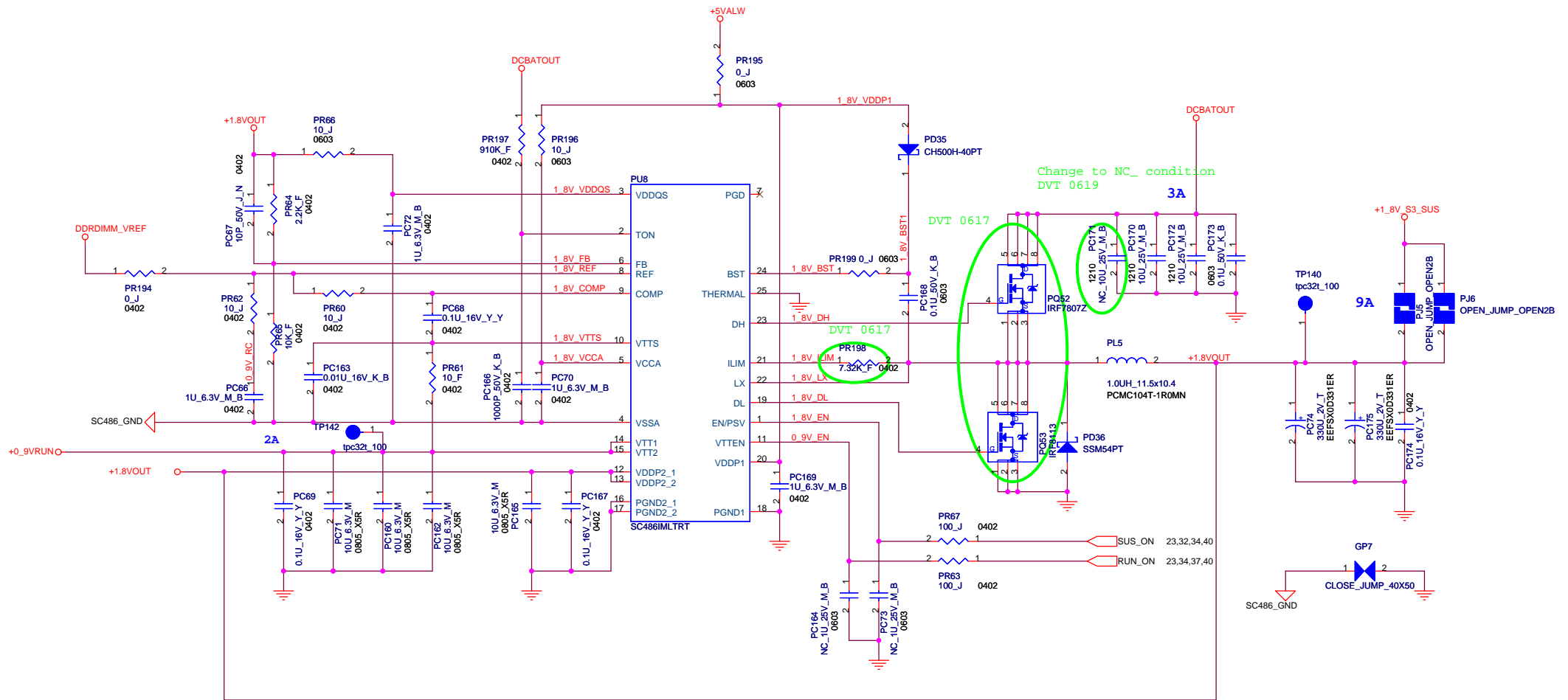
VIINP	W/O	W/I
AC_OFF_3#	1.525V/99W	1.28V/83W
PWRLIMIT	1.246V/81W	0.994V/65W

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Title: **OVP protection-ZG**

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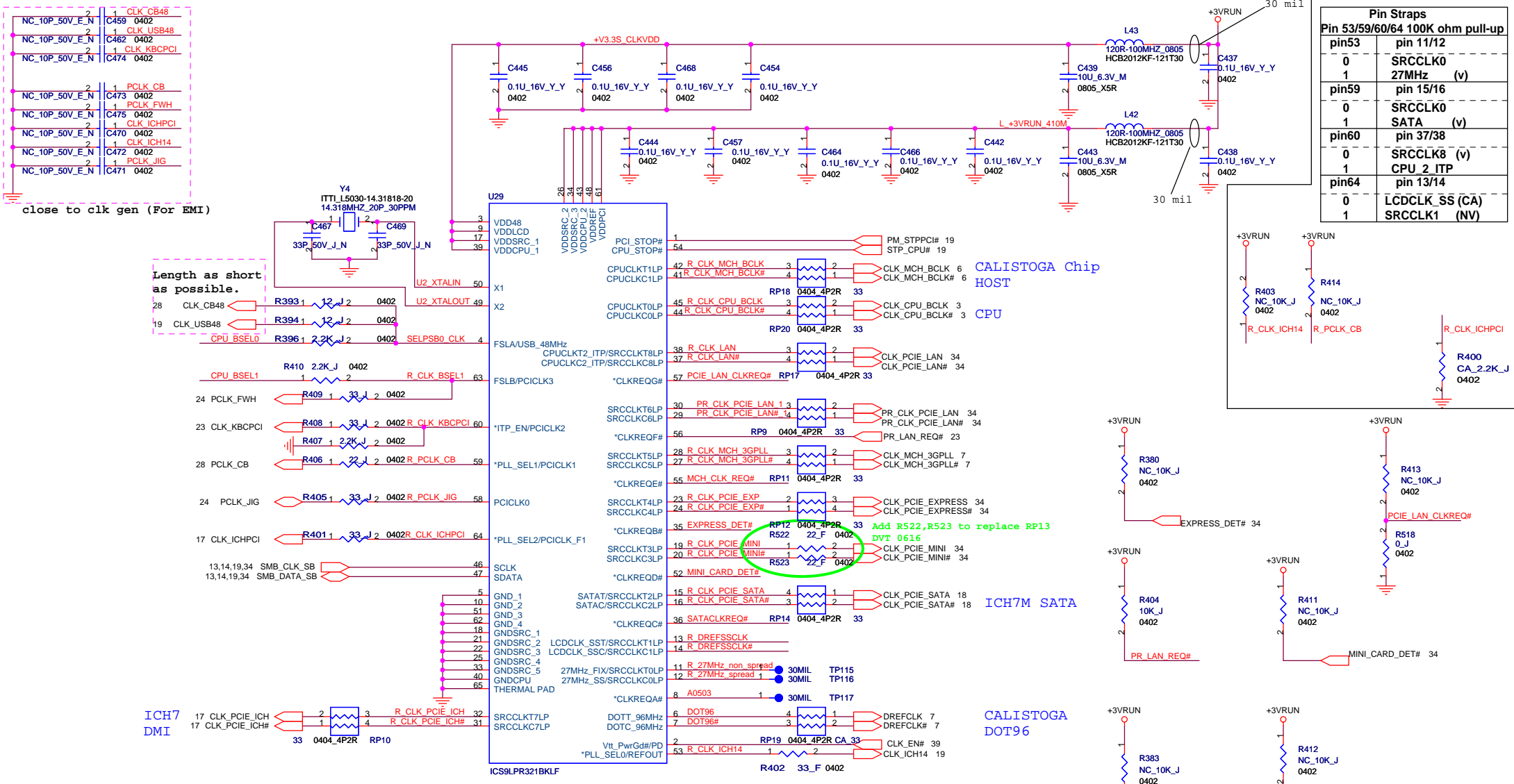


Change to NC_condition
DVT 0619

NC_10P_50V_E_N	2	1	CLK_CB48
NC_10P_50V_E_N	2	1	CLK_USB48
NC_10P_50V_E_N	2	1	CLK_KBCPCI
NC_10P_50V_E_N	2	1	CLK_ICHPCI
NC_10P_50V_E_N	2	1	CLK_ICH14
NC_10P_50V_E_N	2	1	PCLK_CB
NC_10P_50V_E_N	2	1	PCLK_FWH
NC_10P_50V_E_N	2	1	PCLK_JIG

close to clk gen (For EMI)

Length as short as possible.



Pin Straps			
pin53	pin 11/12	pin59	pin 15/16
0	SRCLK0	0	SRCLK0
1	27MHz (v)	1	SATA (v)
pin60	pin 37/38	pin64	pin 13/14
0	SRCLK8 (v)	0	LDCCLK_SS (CA)
1	CPU_2_ITP	1	SRCLK1 (NV)

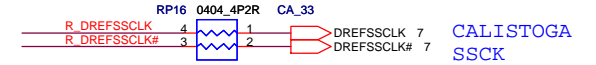
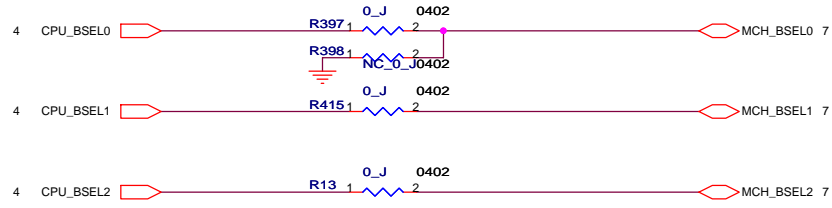
ICH7 DMI

SM bus Address : 1101001 (ICH7)
For clock generator

CLKREQ with internal pull-up resistor
No. Stuff Pull-up Resistor (R69, R40, R41, R70, R1126, R1127)
if EVT ok, del them in DVT

FSB Frequency Table:

FSLB	FSLA	CPU	SRC[7:0]	PCI
0	0	100	100	33
0	1	133	100	33
1	0	200	100	33
1	1	166	100	33

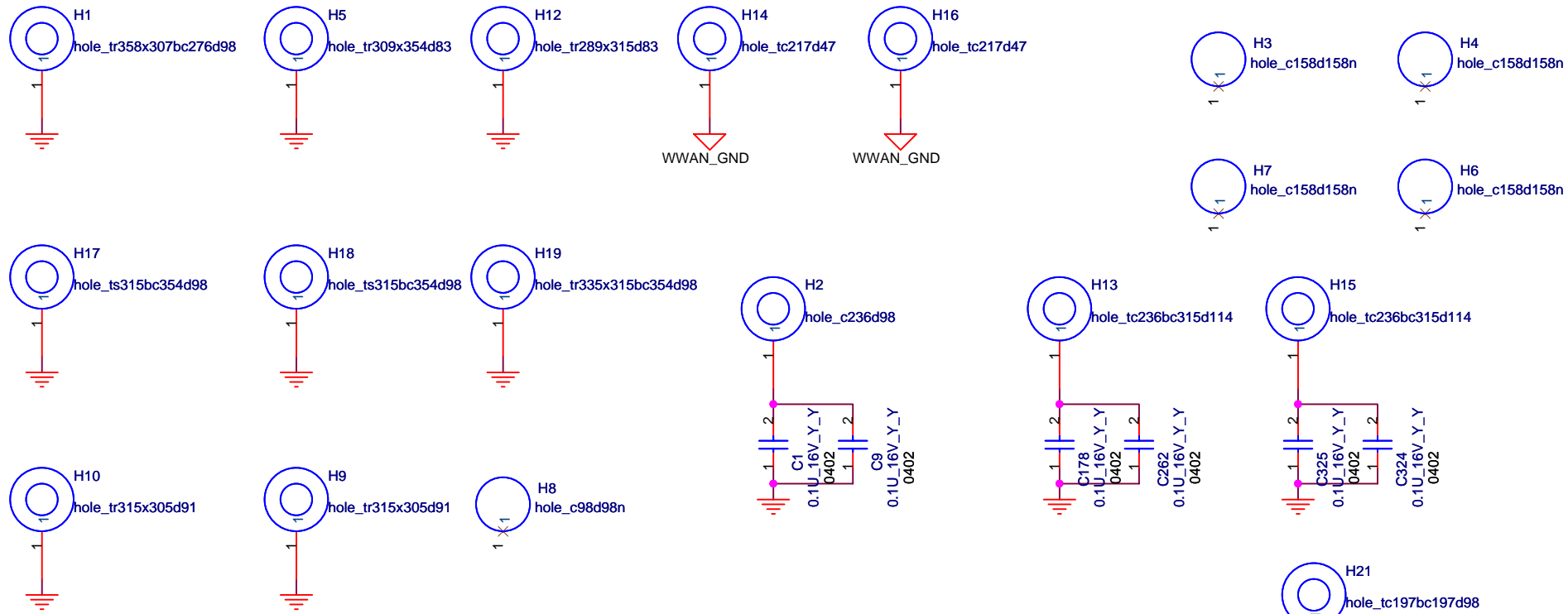


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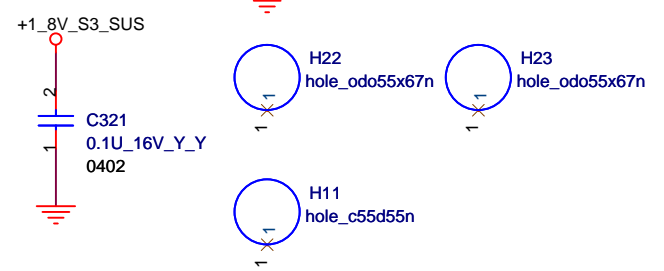
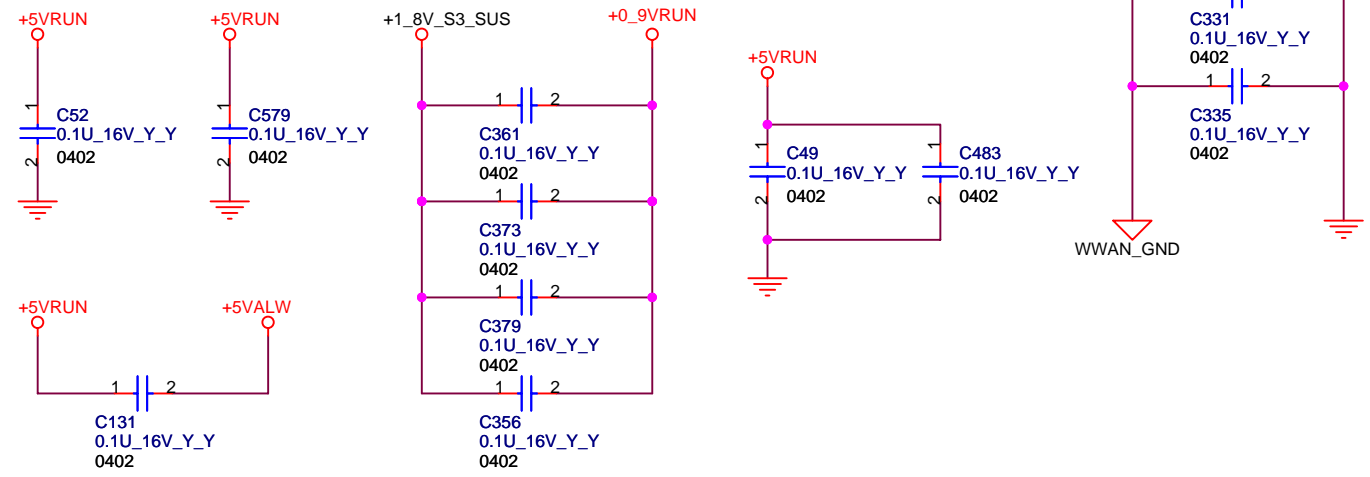
Title: **CLOCK GEN**

Size A3 Document Number: **MS60-1-05 (MBX-163)** Rev 0.20

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FOR EMI



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MS60 Power On Sequence Timing

Version : 0.0
Modified date : 2/14/2006

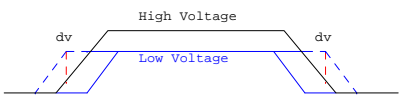


NOTE : (EC KB3910 Min. response time is 1ms)

- T00 : R=47K , C = 0.1uF is ENE recommend value please refer to KB3910B0-AN4A-200
- T01 : 5ms is for ALW VCC supplies must never be active while the ECVCC supply is inactive.(Please refer to Intel 16971 Page 300 of t200 timing)
PS : For KB3910 timing : After ECRST# goes to high ,EC must be check sum and initialized register.For MS01, we measure the T01 Min. 200ms is needed.In MS10 , we will measure this timing again.
- T02 : ALW_PWRGD:H to PM_RSMRST#:H at least 5ms (Please refer to 16971 Page 300 of t205 timing)
- T04 : For MS01 SPEC Min. is 50 ms(Normal SPEC is 20ms)
- T05 : RSMRST# active High to SLP_S5# active High Max. is 110ms(Please reference Intel 16971 Page 301of t232 timing)
- T06(Please reference Intel 16971 Page 301 of t234 timing)
- T07 : For MS01 current SPEC Min. is 25 ms(Please refer Intel 16971Page 301 t208 SPEC is Min 10ms)
- T08 : For MS01 current SPEC Min. is 1 ms(1ms is EC KB3910 at least response time)
- T09 : For MS01 current SPEC
- T10 :Please refer to Intel 16971 Page 300 of t214 timing
- T11 :Please refer to Intel 16971 Page 303 of t216 timing
- T12 : PM_RSMRST# ACTIVE HIGH TO PM_PWRBTN# ACTIVE LOW is 400ms(Normal SPEC is 110ms/Please reference Intel 16971 Page 301of t232 timing)
- T13 : For MS01 current SPEC Min. is 700 ms(Normal SPEC is 1ms that EC can response)
- T14 : For MS01 current SPEC Min. is 5 ms
- DDR2 1.8V from 0V to 2V Max. is 2 ms please refer to Intel 16981 Page 304
- IMVP_OK is same with SB_PWRGD(reserved And Gate with SYS_PWRGD)
- In G7X power sequence :3VRUN-->NVDD,PEX_VDD-->1_8VRUN
- T15 : Please refer to MAX8771 datasheet
- T16: Please refer to MAX8771 datasheet
- T17 : Please refer to Intel Ck410(14690) page 53
- T18 : The ICH7 drives PLTRST# active a minimum of 1ms when initiated through the Reset Control register I/O Register CF9h)
- CPUPWRGD is an output signal that presents a logical AND of the ICH7's PWROK and VRMPWRGD signals
- T20 : From ECRST# L->H to IMVP_PWRGD L->H. If EC's 32KHz is not stable, LPC I/F will hang. So the 1sec must be guaranteed.(Requested by Doi's san 05/13)

Remark: (Item1,2,3 add Diode; Item4,5,6 add discharge circuit; Item7 for implement TV) SPEC please refer to Intel 16981 15.4 GMCH/ICH7M Platform Power -up Requirements)

- V5REF(+5VRUN) -> +3VRUN, dt:0.7mV
- V5REF_SUS(+5VALW) -> +3VALW, dt:0.7mV
- +2.5VRUN -> GMCH_VCC(1.05V), dt:0.7mV
- +1_5VRUN -> +GMCH(1.05V), dt:0.7mV
- +3.3VRUN -> +2_5VRUN, dt:0.3mV
- +3_3VRUN -> +5VRUN (VccLAN), dt:0.3mV
- +3_3VRUN -> +1_5VRUN(TV), dt:0.7mV



R/C delay (47K/0.1uF)

T00	T01	T02	T03	T04	T05	T06	T07	T08	T09	T10
within 10ns-2ms	Min. 5 ms	Min. 10 ms	Min. 40ms	Min. 50ms	Min. 110ms	1 - 2 RTCCLK	Min. 25 ms	1ms	Min. 10ms	Min. 99ms
T11	T12	T13	T14	T15	T16	T17	T18	T19	T20	
Max. 50ns	Min. 400ms	Min 700ms	Min 5ms	typ 60us	Min : 3ms Max : 8ms	Max 1.8ms	Min 1ms	Min : 99ms	Min : 1s	

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Power Sequence

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<1>2006/3/28 remove U36.SW no need to program for present application.

<2>2006/3/28 Change PR5 from 13K to common parts 10KOhm.

<3>2006/3/29 Change USB CONN. CN16 & CN40 for ID requirement.
P/N : FOX_UB11193-C1301-4F

<4>2006/3/29 Change ODD CONN. CN21 for ID requirement.
P/N : FOXCONN_QT8H0506_64T2R_4F

<5>2006/3/29 Change PC359.PC360 to 10uF
P/N : 1C-2B70106-M100

<6>2006/3/29 update new HDD CONN CN24.
P/N : 2N-0022002-F0G0

<7>2006/3/29 update new DC-IN CONN PCN1.
P/N : FOX_GS53020-00580-7F

<8>2006/3/29 update new BTY CONN PCN2.
P/N : FOXCONN_BP34063_B6012_7F

<9>2006/3/30 U18.U19.U21.R277.R300.R315change to NC according to Customer's feedback.

<10>2006/3/30 R269,R273,R276,R286,R287,R300 change to Populate according to Customer's feedback.

<11>2006/3/30 New add INV_ENABLE_EC logic dur to BIOS Code merge issue.add new component :
U53.U54 P/N : 14-74AHC1G-0800
R762 P/N : 1R-0000103-J200
R763 P/N : 1R-0000000-J200
R764 P/N : 1R-0000104-J200
Delete R176.R177

<12>2006/3/31 Add C20.C21.C22.C31.C33.C68 for EMI slution.
P/N : 1C-2Y20104-Y000

<13>2006/3/31 Add R5 for Customer feedback.
P/N : 1R-0000000-J200

<14>2006/3/31 Dummy R482,R483 for Customer feedback.

<15>2006/3/31 Modify MS PWR Circuit for Customer feedback.add new component :
U55.U56 P/N : 15-RT9702A-0000
C521.C522 P/N : 1C-2Y20104-Y000
R569.R573 P/N : 1R-0000105-J200
C870.C871 P/N : 1C-2Y30225-Y000
C535.C751 P/N : 1C-2B70106-M100
Deleted Component :
Q12.Q13.Q20.Q21.C535.C527.C521.C751.C753.C752.R486.R476.R568.R569

<16>2006/3/31 CN2 Pin11 change to +3V_S3_SUS for Customer feedback.

<17>2006/4/3 CN20.CN32.CN33 Pin assignment modified due to Customer's concern.

<18>2006/4/3 CN31.CN32.CN33 CN34 Connector change.
P/N : GB11261_1051_7F

<19>2006/4/3 L17 & L19 updated according to Customer feedback
P/N : 1L-DCS0603-1000

<20>2006/4/4 Add PWR_MIZER circuit.
U6J GPIO10 with new signal "NV_PWR_MIZER"
new Components added and modified as below :
10K Ohm -- R130.R766 -- P/N : 1R-0000103-J200
7.5K Ohm -- R765.R767.R768.R769.R770 -- P/N : 1R-0000752-F200
4.3K Ohm -- R128 -- P/N : 1R-0000432-F200
2N7002EPT -- Q54.Q55.Q56.Q57.Q58 -- P/N : 17-2N7002E-PT00

<21>2006/4/4 CN10 Pin4.5.6 change to Test pad according to customer's feedback.

<22>2006/4/4 D6.D7.D8 change to Q59.Q60.Q61
P/N : 17-2N7002E-PT00

<23>2006/4/4 R64,R67,R65,R75,R99,R94,R97,R109 change to populate.
P/N : 1R-0000121-J200

<24>2006/4/4 new add Q62 for WLAN LED Logic
P/N : 17-2N7002E-PT00

<25>2006/4/4 NC F1 and C859 according to customer's feedback.

<26>2006/4/4 delete R482.R483 according to customer's feedback.

<27>2006/4/6 add H3 ~ H20

<28>2006/4/6 Update BTY Connector PCN2 for ME requirement.
P/N : 2N-0006001-MKX0

<29>2006/4/6 R278.R289.R270 change to 75Ohm and circuit modified as customer's feedback.
P/N : 1R-0000750-F200

<30>2006/4/6 R543 change to 75Ohm as customer's feedback.
P/N : 1R-0000750-F300

<31>2006/4/6 R553 change to 75Ohm as customer's feedback.
P/N : 1R-0000750-J200

<32>2006/4/6 R99.R94.R97.R109.R67.R64.R65.R75 change to NC as customer's feedback.
and R66.R69.R98.R101 change to 120Ohm.
P/N : 1R-0000121-J200

<33>2006/4/6 CN34 Pin23 change to +5VALW as customer's feedback.

<34>2006/4/6 CN31 Pin1.2 change to +3V_S3_SUS as customer's feedback.

<35>2006/4/6 add 1A Fuse F4.F5.F9.F11.F15.F17.F18.F19
P/N : 1M-F32V1A0-F000

<36>2006/4/6 add 0.5A Fuse F2.F3.F6.F7.F8.F10.F12.F13.F14.F16.F18
P/N : 1M-F32V0A5-F000

<37>2006/4/6 add C872 according to MS20 lesson learn.
P/N : 1C-2B20102-M000

<38>2006/4/6 CN34 Pin23.24 change to +3VRUN.

<39>2006/4/6 add C71.C74.C87 for EMI.
P/N : 1C-2Y20104-Y000

<40>2006/4/6 add C89.C188.C199.C208.C213.C214
P/N : 1C-2Y20104-Y000

<40>2006/4/7 add C215.C216.C217.C218.C219 for EMI solution.
P/N : 1C-2Y20104-Y000

<41>2006/4/7 R118.R119.R351 change to populate as customer's feedback.

<42>2006/4/7 Y1.C104.C107.C492.C497.C501.R433.R434.R427.R428.R429.R430.R132.
R133.R134.R136.R117 change to NC as customer's feedback.

<43>2006/4/7 R439.R443 change to 0 Ohm as customer's feedback.
P/N : 1R-0000000-J200

<44>2006/4/7 update Net name EN_EXT_DEV_SENSE# as customer's feedback.

<45>2006/4/10 Modify ODD PWR Circuit for Customer feedback.add new component :
PQ183 P/N : 17-2N7002D-W000
PR115 P/N : 1R-0000101-J200
PR103.PR114 P/N : 1R-0000104-F100
PC87 P/N : 1C-2B20103-M000
PQ38 P/N : 17-S14800B-DY00
PC76 P/N : 1C-2B70106-M200

<46>2006/4/10 Modify VGA PWR Circuit for Customer feedback.add new component :
PR273 P/N : 1R-0000103-F200
PR773 P/N : 1R-0004992-F200
PQ20 P/N : 17-2N7002E-PT00
PR774 P/N : 1R-0000102-J200
PC873 P/N : 1C-2Y20105-Y000

<47>2006/4/10 add H21-H24.

<48>2006/4/10 Rename Schematic Part referene.
new version since 4/11

<49>2006/4/11 change R68.R133.R100
P/N : 1R-0000151-F200

<50>2006/4/11 PR111.PR114 change to NC according to PWR team's suggestion in EVT.

<51>2006/4/11 Modify ODD reset circuit as customer's feedback.
Add U37 P/N : 15-MAX809S-0000
Add R516 P/N : 1R-0000104-J200
NC R305

<52>2006/4/11 Remove C257 for EMI comment.

<53>2006/4/11 add ODD Reset RC.
Add R517 P/N : 1R-0000103-J200
Add C580 P/N : 1C-2Y20104-Y000

<54>2006/4/14 change R197.R198.R199.R200 to 60.4Ohm
P/N : 1R-000604X-F200

<55>2006/4/14 add R518 for 0Ohm
P/N : 1R-0000000-J200

<56>2006/4/14 CN7.C409.C412.L37.F16.R44.R45 change to CA from NV to fit configuration.

<57>2006/4/27 PR111.PR114 change to Populate from NC according to PWR team's suggestion in EVT.
P/N : 1R-0000100-J200

MS60-L change list base on MS60-H

<58>2006/5/02 Del all NV_ components for L-model only.

<59>2006/5/03 Remove +1_8VRUN discharge circuit.Delete PR169,PQ44. Add PQ54 P/N:17-2N7002E-PT00

<60>2006/5/03 LED2 pin2,pin3 swap for Power LED color opposite issue

<61>2006/5/03 Change CAP93,CAP94 to NEC,TEPSGV0E337M9-12R,330uF,2.5V
P/N:1C-31T0337-MX00
Add CAP95 P/N:1C-31T0337-MX00

<62>2006/5/04 F1,F2,F3,F4,F5,F6,F7,F8,F9,F10,F11,F12,F13,F14,F15,F16,F17,F19 change to fuse,1.1A PTC type
P/N:1M-F06V1A1-F000

<63>2006/5/05 follow M/E change to exchange PCN1 pin1 & pin2 connection.Layout change placement form top side to bottom side.

<64>2006/5/05 Add GP14,GP15 open jump for repair conveniently

<65>2006/5/05 Add C581,C582,C583,C584,C585,C586,C587,C588,C589,C590,C591,C592 for 22uF_0805_6.3V shortage.

<66>2006/5/08 As to M/E assemble issue, we will need rotat 180degree about T/P module.So that R47 change to stuff

<67>2006/05/09 Rename CAP93,CAP94,CAP95 to PC93,PC94,PC176.And change component to Panasonic,EEFSX0D331ER,330uF,2V
P/N:1C-42T0337-MX00

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<68>2006/05/09 PC54,PC58,PC59,PC139 change to X5R,0.1uF,6.3V,10%,0201 for X7R,0.1uF,10V,0201 shortage
P/N:1C-2B10104-K100

<69>2006/05/11 L33,L34 pin swap .D12 & D10 change to TOP side for layout conveniently

<70>2006/05/12 PR198 change to 5.6k/0402_1% to modify 1.8V OCP seting value.
P/N:1R-0000562-F200

<71>2006/05/12 CN23 change to 'FOX_MH11747-BR2D-4F' for ME requirement.
P/N:2N-000400N-FKGO

<72>2006/05/12 CN3,CN8 change to 'FOX_GB5RF120-1200-7F' for ME requirement.
P/N:1N-0012001-F0T0

<73>2006/05/12 CN7 change to 'FFOXCONN_GB5RF060_1200_7F' for ME requirement.
P/N:1N-0006000-F0T0

<74>2006/05/12 CN12,CN16 change to 'FOXCONN_UB11193_C1304_4F' for ME requirement.
P/N:1N-0004000-FEG0

<75>2006/05/12 CN9 change to 'FOXCONN_HS8206E' for ME requirement.
P/N:1N-0006001-M1T0

<76>2006/05/16 Due to ripple noise issue.PC74,PC175 change to 'Panasonic,EEF5X0D331ER'
.Del PC75 for power requirement.
P/N:1C-42T0337-MX00

<77>2006/05/17 Add PQ55,PQ56,PR200,PR201,PR202,PR203 for power discharge.
P/N:17-2N7002D-W000
P/N:1R-0000331-J300
P/N:1R-0000104-F100
P/N:1R-0000101-J200

<78>2006/05/17 U24 change to 'FOXCONN_P24782A_2743_01' for ME requirement.
P/N:1N-1478002-0000

<79>2006/05/18 PC67 change to 10pF 0402,and need to mount for power requirement.
P/N:1C-2N20100-J000

<80>2006/05/18 CN12,CN16 change footprint to 'FOXCONN_UB11193_C1304_4F_HM' for DFM.

<81>2006/05/18 Add R519,R520,C593,C594 on 'IAC_BITCLK' signal for EMI requirement.
P/N:1R-0000000-J200
P/N:1C-2N20330-J000

<82>2006/05/18 H13,H15 footprint change to ' hole_tc236bc315d114' for ME requirement.
P/N:1X-HOLE000-0232

<83>2006/05/19 CN25 need change to P/N:1N-1200007-0000. CN26 need change to
P/N:1N-1200008-0000. Because P/N:1N-120000C-0000 & P/N:1N-120000D-0000 part number are
not available.

<84>2006/05/19 Add PC177,PC178,PC179,PC180 on DC_IN trace for EMI requirement.
P/N:1C-2B30104-K000

<85>2006/05/22 Del R89,R140,R127.Add L54,L55,L56 (0 ohm change to bead) for EMI requirement.
P/N:1L-BEBMS16-0801

<86>2006/05/30 change R517 from 10Kohm to 0ohm for solving the ODD issue.
P/N:1R-0000000-J200

DVT change list

<87>2006/06/15 Delete R264.R271 for Debug BD LED.

<88>2006/06/15 Del reset IC form ODD portion.Del R516,R517,C580. Change U37 to 74AHC1G08GW and
connect GPIO_ODD_RST# form KBC for ODD reset.

<89>2006/06/15 Add R521 1k ohm and change R244 connection form 'ALW_ON' to 'ALW_ON_1' for
customer's requirement.
P/N : 1R-0000102-J200

<90>2006/06/16 PORT_DET# change from EC's pin81 to EC's pin176 for noise decreasing.

<91>2006/6/16 remove RP13 and replace with R519/R520 for WLAN issue improving.
P/N : 1R-0000220-F200

<92>2006/6/16 Add one GPIO signal 'VISTA_SUPPORT#' that is connected form EC's pin99 to
CN1's pin17 to support Vista OS.

<93>2006/6/16 Add PQ57,PC181 for ODD power plane.
P/N:17-S12304B-DS00
P/N:1C-2B70106-M200

<94>2006/6/16 (HDD connector)CN21's pin18 change connection from NC to GND for the starting timing improvement.

<95>2006/6/17 Change PQ52 from SI7392DP to IRF807Z and change PQ53 from SI7336ADP to IRF8113 for power requirement.
P/N:17-1RF7807-2000
P/N:17-1RF8113-0000

<96>2006/6/17 PR198 change from 5.6K ohm to 7.32K ohm to modify OCP setting value.
P/N:1R- 0007321-F200

<97>2006/6/17 U12 change from G961-18ADJEU to SC1565IS-2.5TRT for WWAN voltage drop improvement.
P/N:15-SC15651-0000

<98>2006/6/19 pc117,pc179,pc178,pc180,pc115,pc91 change to populate for EMI requirement.

<99>2006/6/19 Add C595 at PRT_IN power trace for EMI requirement.
P/N:1C-2B30104-K000

<100>2006/6/19 Add PC116,PC117,PC118,PC120,PC122,PC123,PC124 at DCBATOUT power trace for EMI requirement.
P/N:1C-2B30105-M000
P/N:1C-2B30104-K000

<101>2006/6/19 Add R303 10K pulldown at U34's pin1 to avoid start abnormally for customer's requirement.
P/N:1R-0000103-J200

<102>2006/6/19 PC171 change to NC_ condition for power requirement.

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