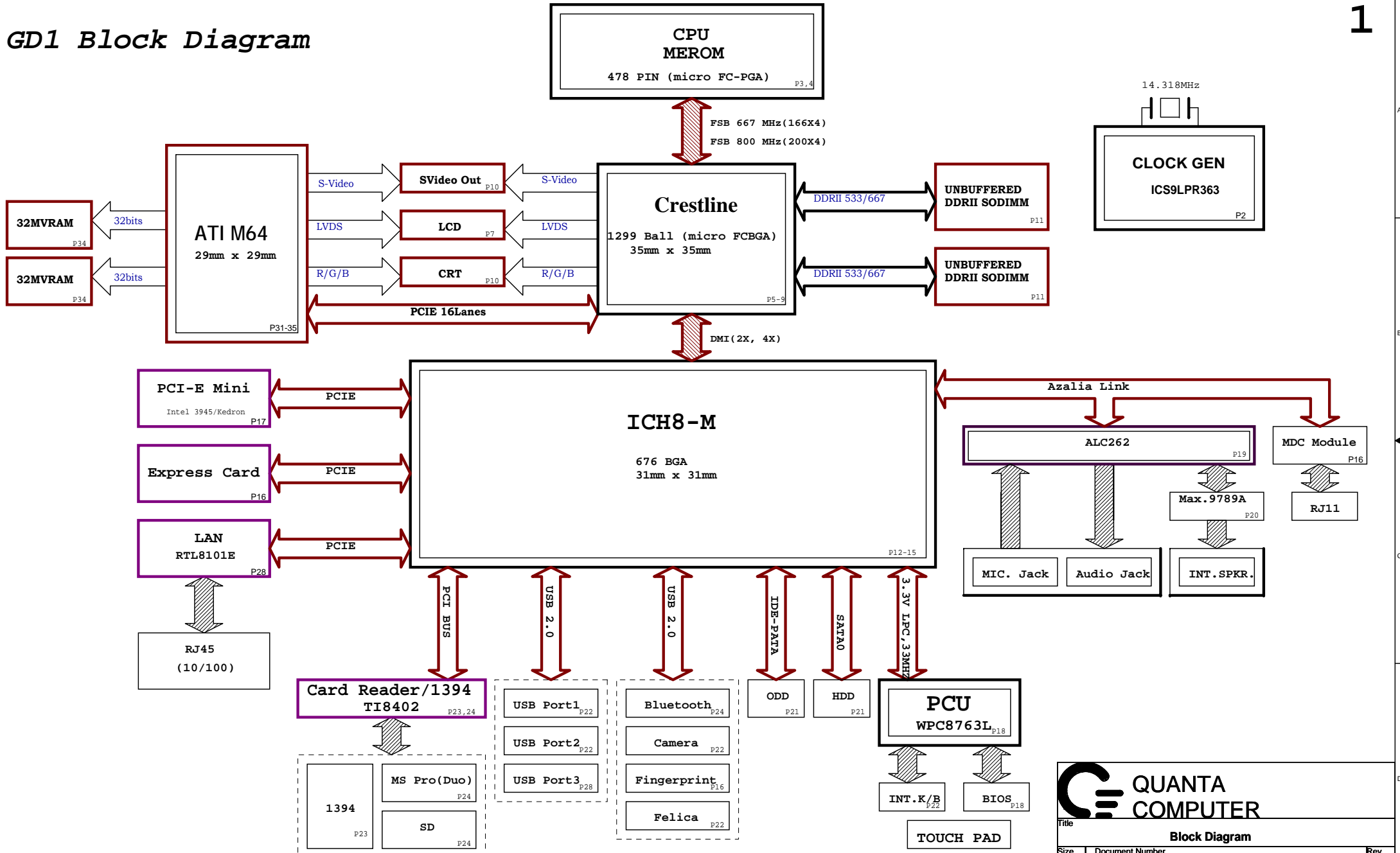


GD1 Block Diagram



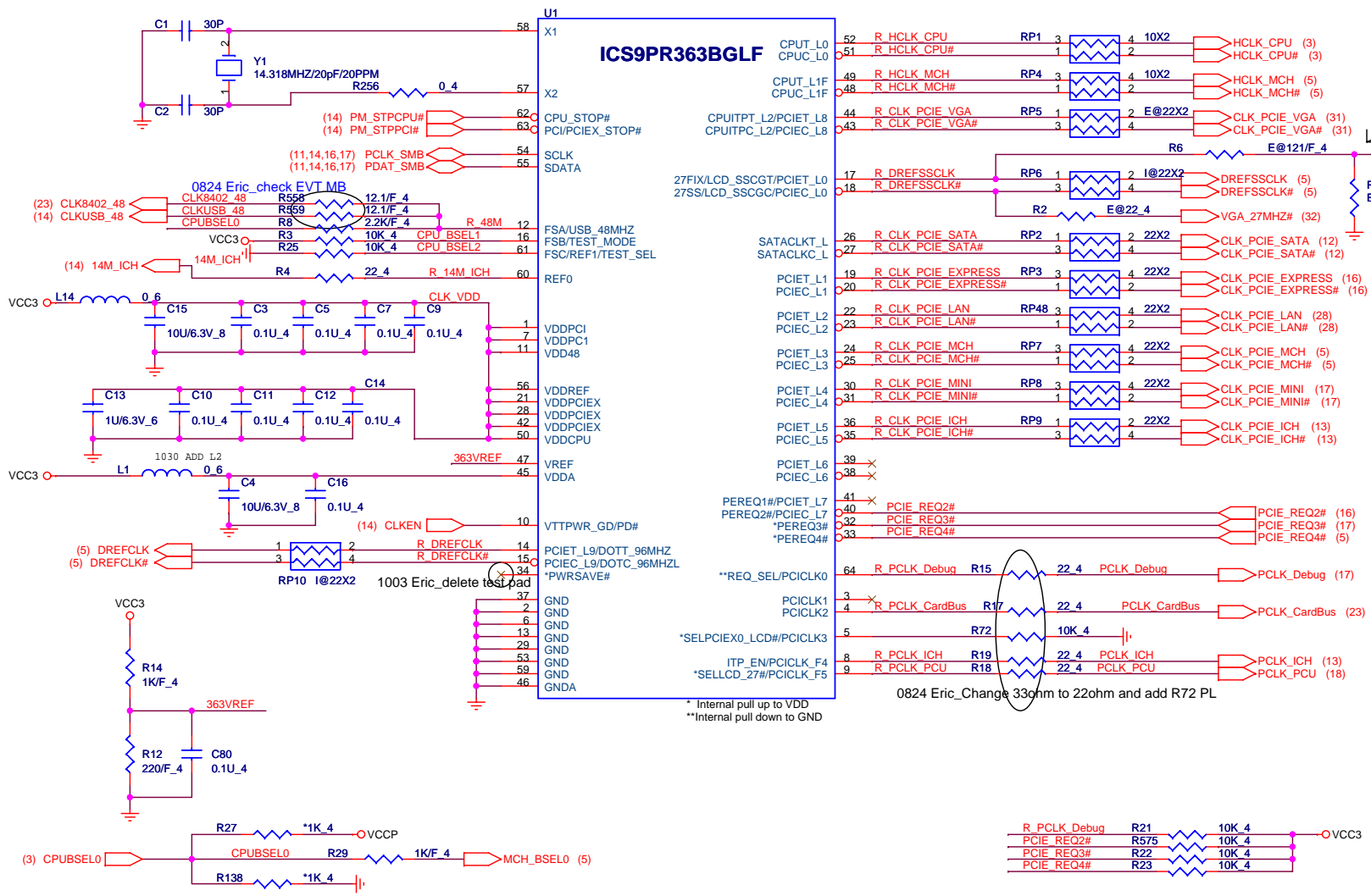
1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: **Block Diagram**

Size: B Document Number: **GD1 Main Board** Rev: 1A

Date: Tuesday, November 14, 2006 Sheet 1 of 35



Signal		965GM	965PM
VGA_27MHZ	R6	NI	121
VGA_27MHZ#	R7	NI	71.5
CLK_PCIE_VGA	RP5	NI	22X2
DREFSSCLK	RP6	22X2	NI
DREFCLK	RP10	22X2	NI

PIN 5 R494	PIN 9 R26	PIN 14/15	PIN 17/18
LO (10K)	LO (10K) HI (NC)	PCIEX9 DOT96	27MHZ LCD
HI (NC)	LO (10K) HI (NC)	PCIEX9 DOT96	PCIEX0 PCIEX0

ITP_EN(PIN8)
 LOW : PIN43/44 SRC
 HIGH : PIN43,44 CPUTIP

PCIE_REQ1#	PCIE_L0	PCIE_L6	
PCIE_REQ2#	PCIE_L1	PCIE_L8	
PCIE_REQ3#	PCIE_L2	PCIE_L4	
PCIE_REQ4#	PCIE_L3	PCIE_L5	PCIE_L7

QUANTA COMPUTER

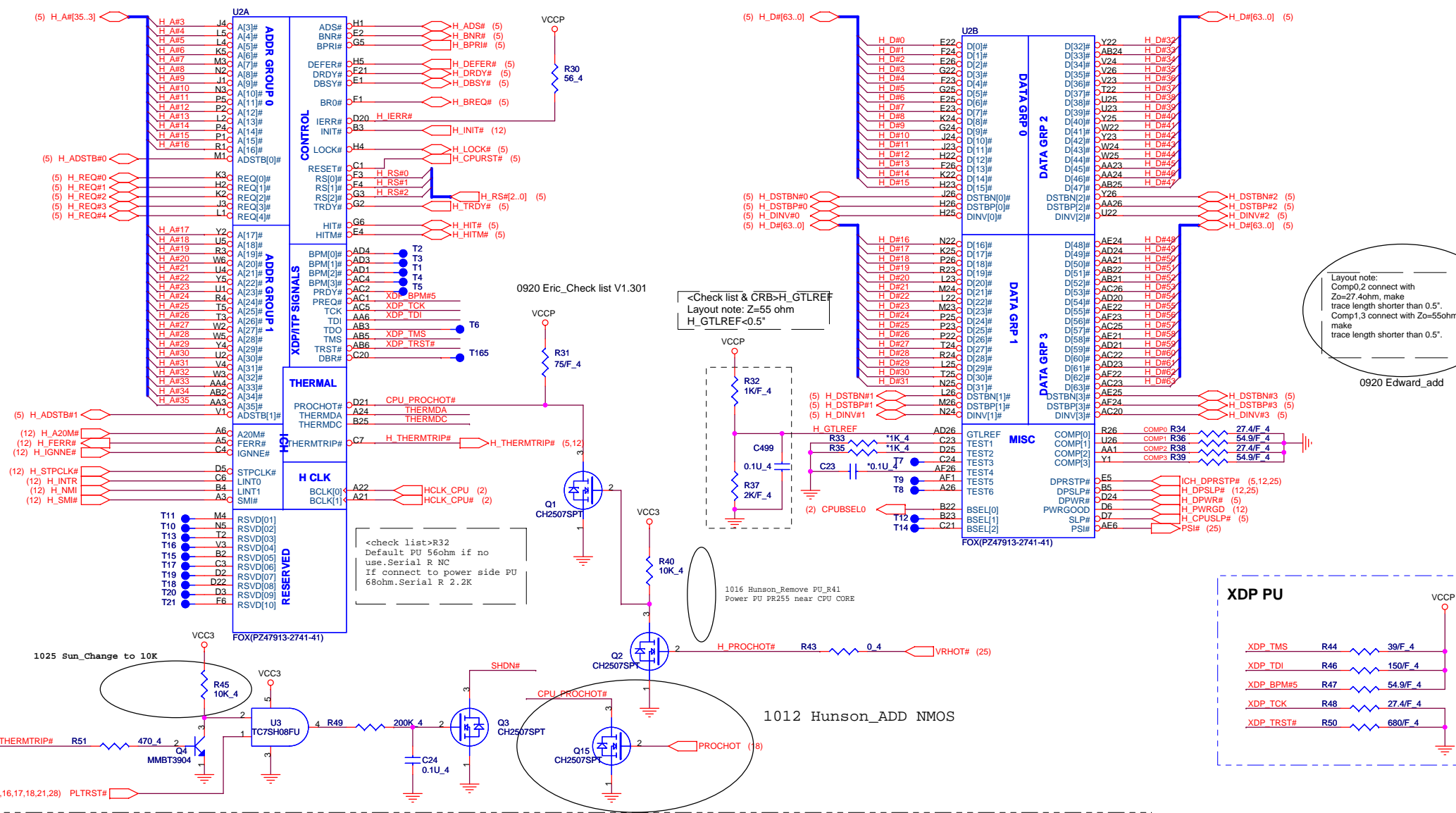
Title: **CLOCK GENERATOR**

Size B Document Number: **GD1 Main Board** Rev 1A

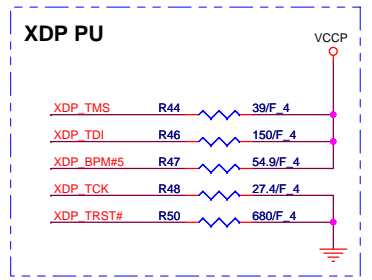
Date: Wednesday, November 15, 2006 Sheet 2 of 35

FSC BSEL2	FSB BSEL1	FSA BSEL0	CPU	SRC	PCI	REF	USB DOT	Spread %
0	0	0	266.66	100	33.33	14.318	48 96	0.5 Down
0	0	1	133.33	100	33.33	14.318	48 96	0.5 Down
*	0	1	200.00	100	33.33	14.318	48 96	0.5 Down
0	1	1	166.66	100	33.33	14.318	48 96	0.5 Down
1	0	0	333.33	100	33.33	14.318	48 96	0.5 Down
1	0	1	100.00	100	33.33	14.318	48 96	0.5 Down
1	1	0	400.00	100	33.33	14.318	48 96	0.5 Down
1	1	1	200.00	100	33.33	14.318	48 96	0.5 Down

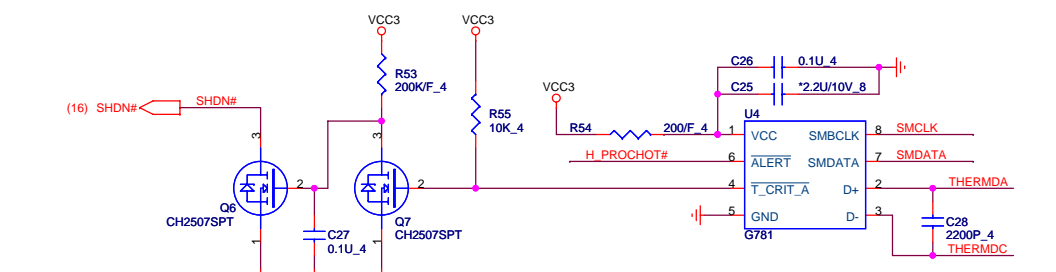
1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



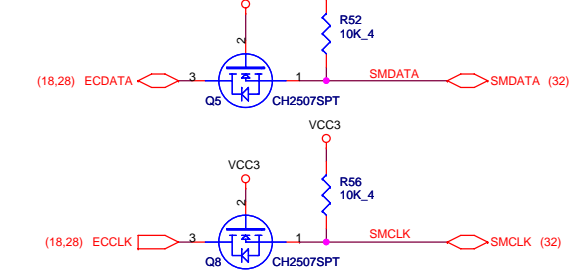
Layout note:
Comp0,2 connect with
Zo=27.4ohm, make
trace length shorter than 0.5".
Comp1,3 connect with Zo=55ohm,
make
trace length shorter than 0.5".



Thermal Sensor



Thermal SMBUS

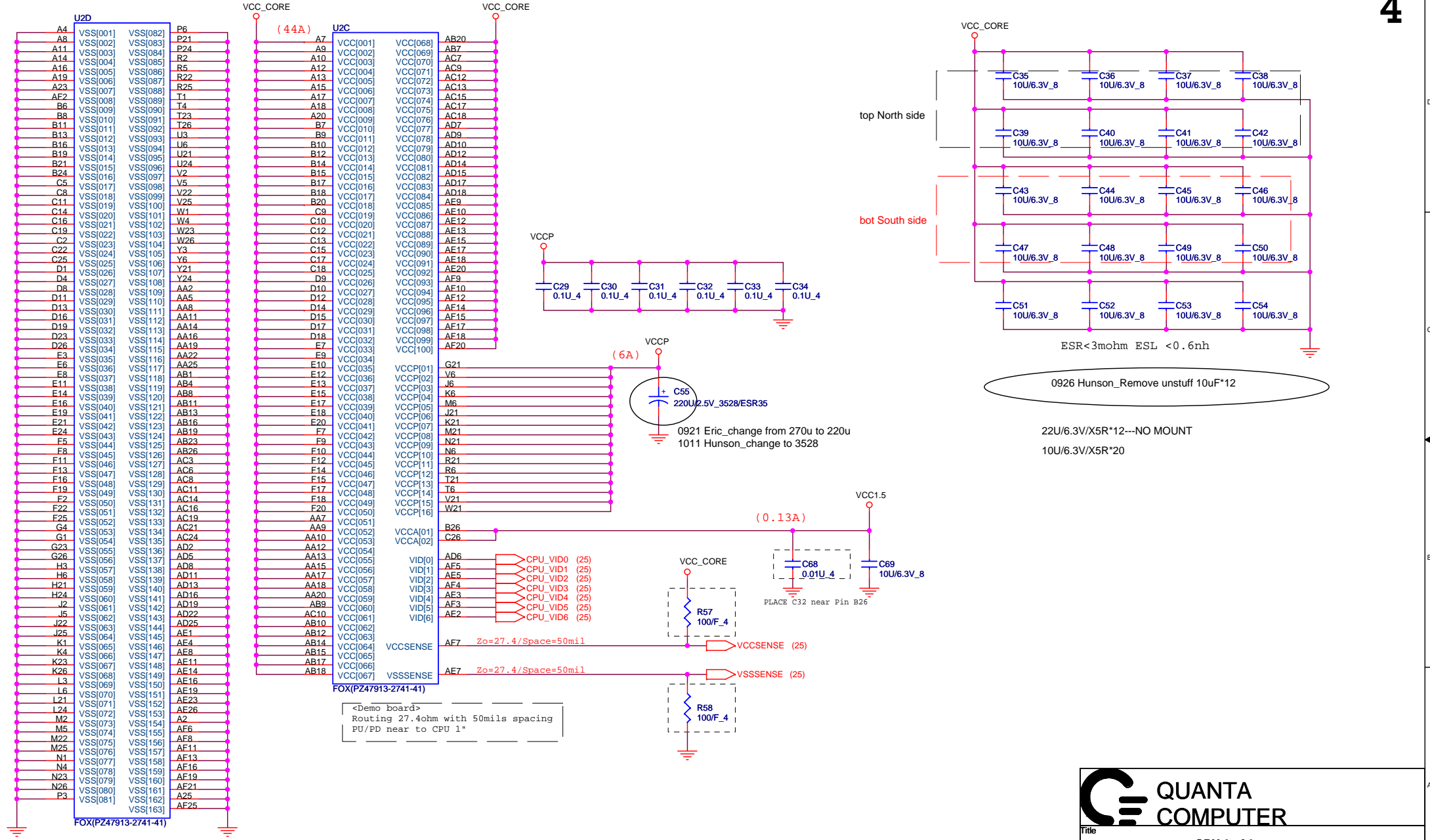


QUANTA COMPUTER

Title: **CPU1 of 2**

Size: Document Number **GD1 Main Board** Rev 1A

Date: Tuesday, November 14, 2006 Sheet 3 of 35



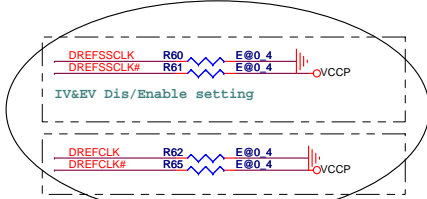
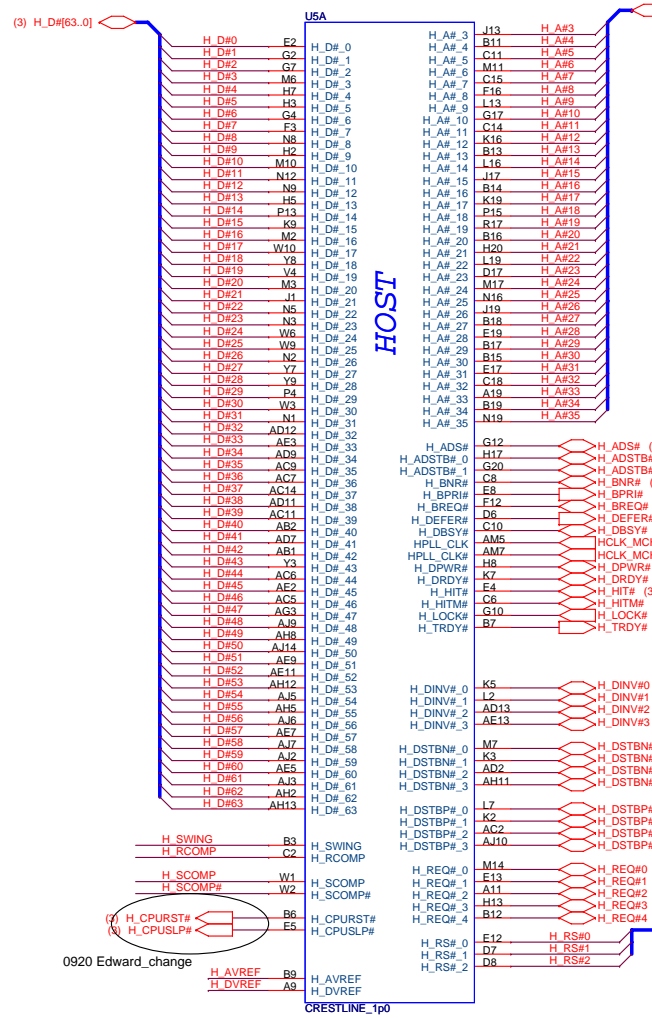
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

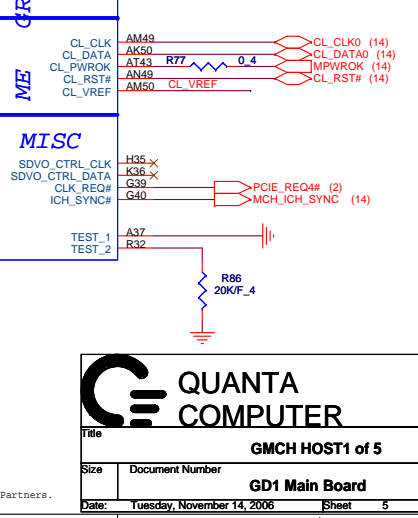
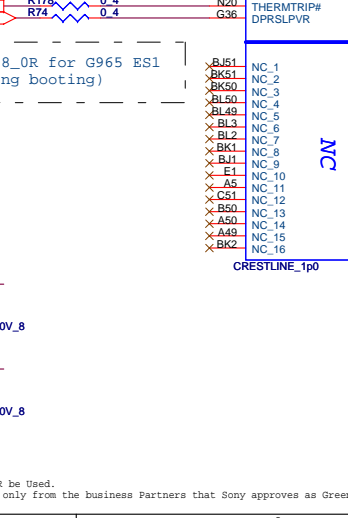
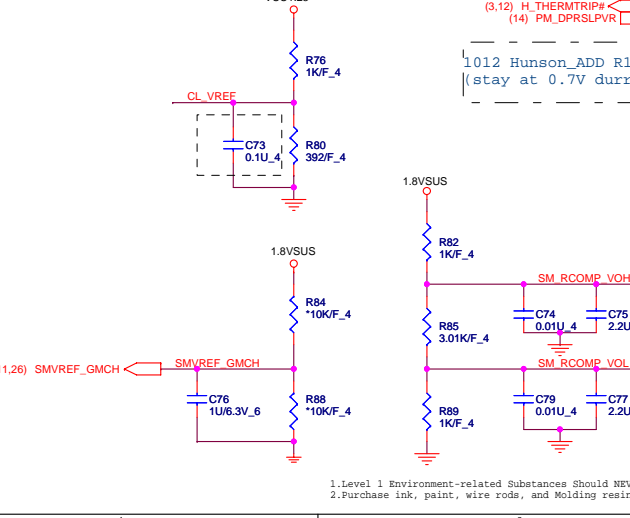
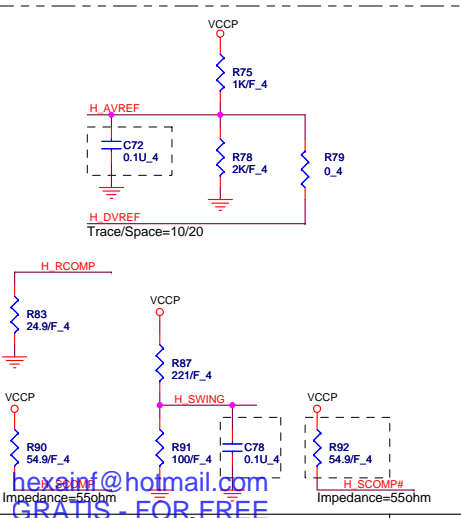
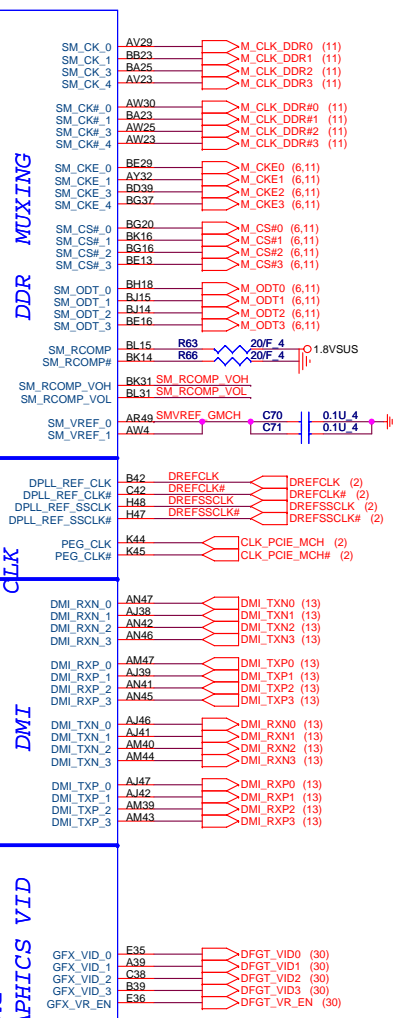
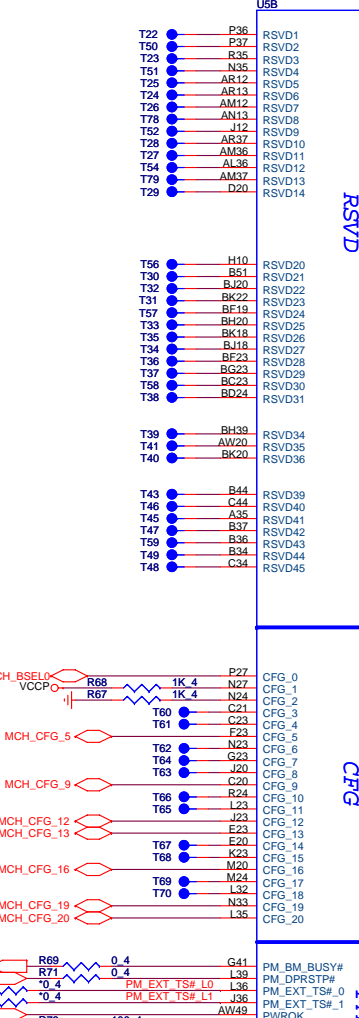
Title: **CPU 2 of 2**

Size B Document Number: **GD1 Main Board** Rev 1A

Date: Tuesday, November 14, 2006 Sheet 4 of 35



0921 Edward_follow design Guide 1.1 page195



hex.sinf@hotmail.com
Impedance=55ohm

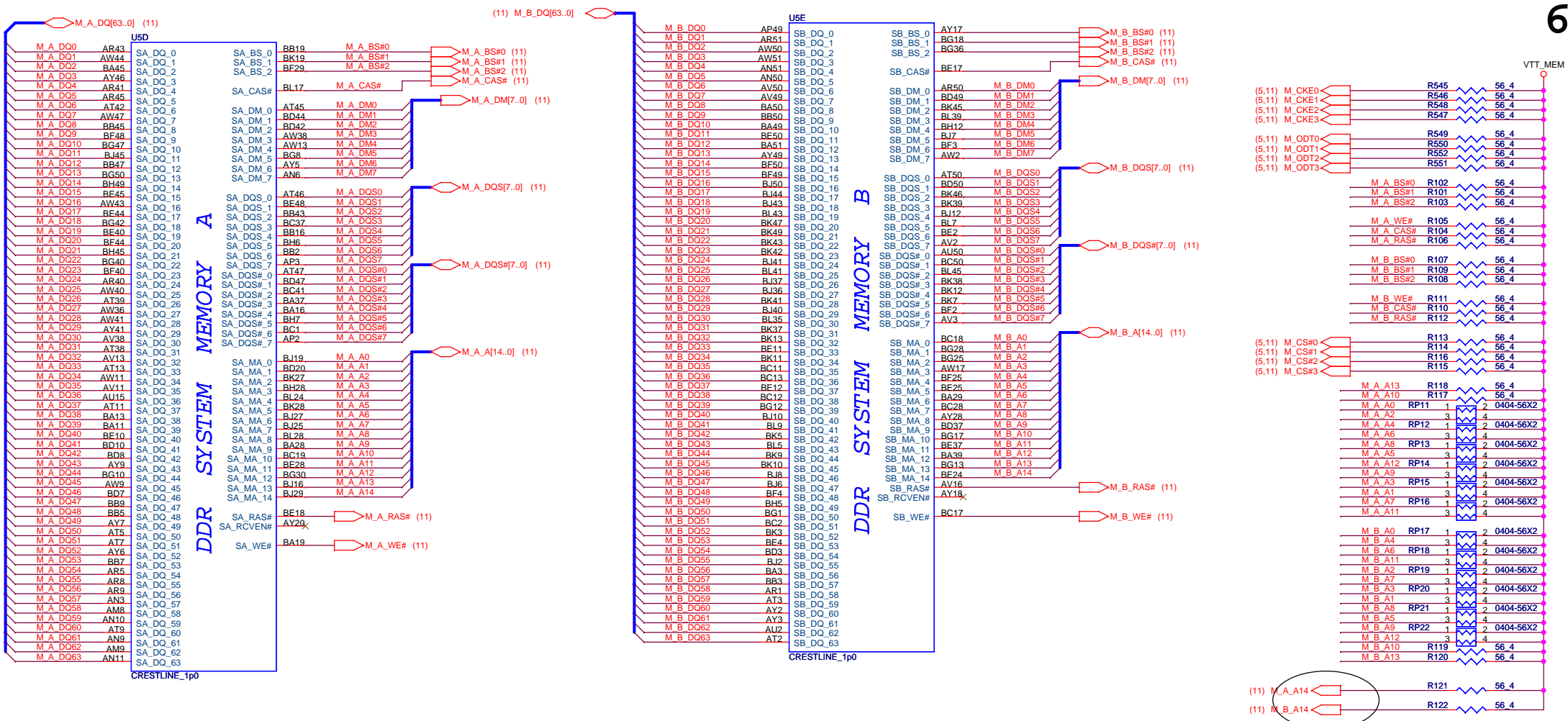
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: **GMCH HOST1 of 5**

Size: Document Number: **GD1 Main Board** Rev: 1A

Date: Tuesday, November 14, 2006 Sheet 5 of 35

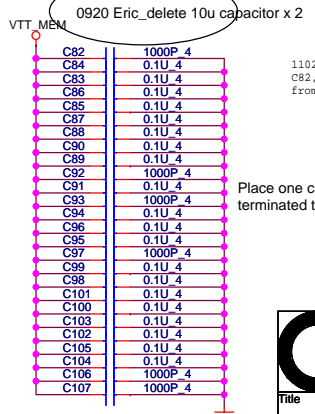
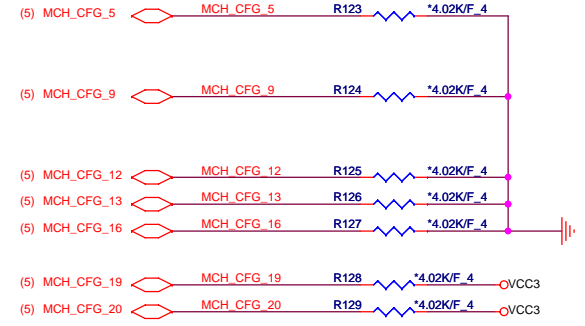


GMCH Strap pin description

	Low	High
CgF5	DMIX2	* DMIX4
CgF6	RSVD	RSVD for 945GMS
CgF7	RSVD	* CPU type: Mobile CPU
CgF9	PCI Express Graphics lan : Reverse Lane	* PCI Express Graphics lan : Normal operation
CgF10	reserved	
CgF11	reserved	
CgF16	FSB Dynamic ODT Disabled	* FSB Dynamic ODT Enabled
CgF18	* GMCH core: 1.05V	GMCH core: 1.5V
CgF19	* DMI LANE Normal	DMI LANE Reversed
CgF20	* only SDVO or PCIe x1 is operational	SDVO and PCIe x1 are operation simultaneously via the PEG port

CgF[13:12]	00 = Partial clock gating disable 01 = XOR mode enabled 10 = All-Z mode enabled * 11 = Normal Operation(Default)
------------	---

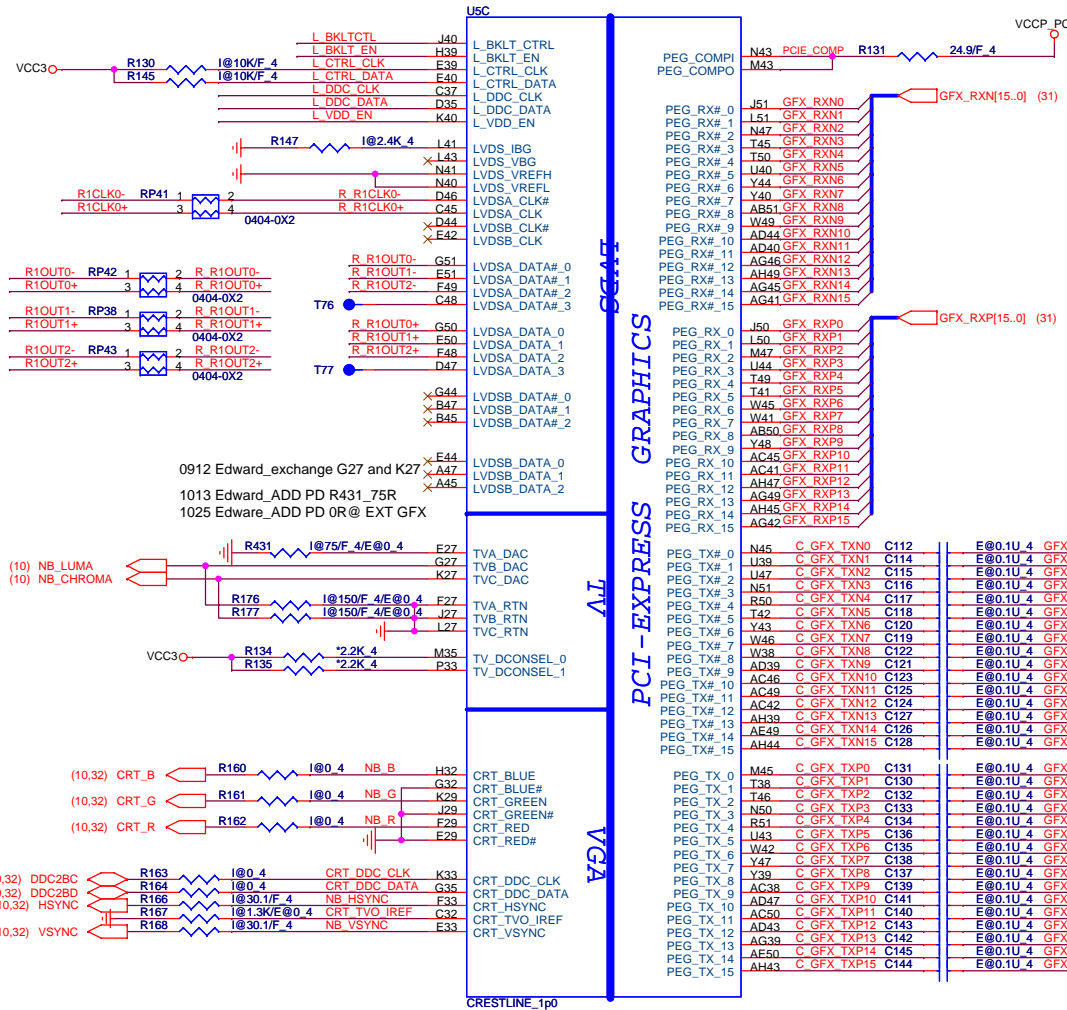
Int.Pull-down : CFG 18,19,20
Int.Pull-high : CFG CFG 3-17



Place one cap close to every 2 pull-up resistors terminated to VccSus0_9(Total 0.1u x 26)

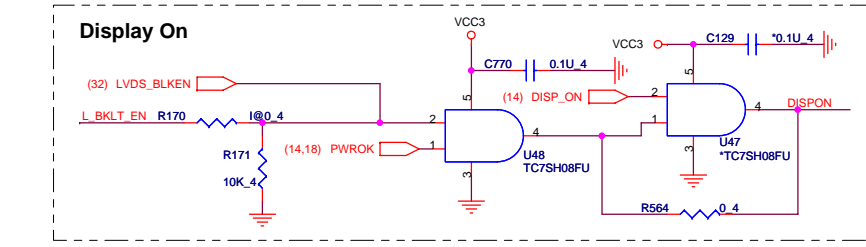
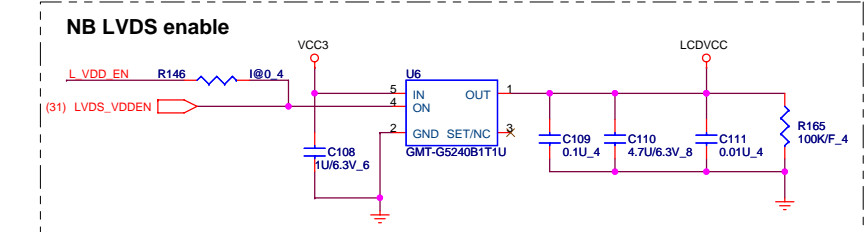
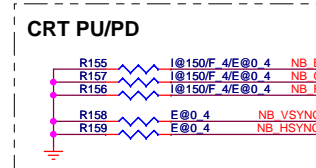
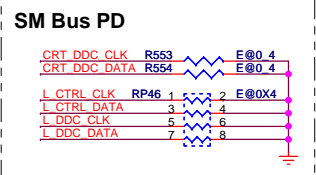


1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the Business Partners that Sony approves as Green Partners.

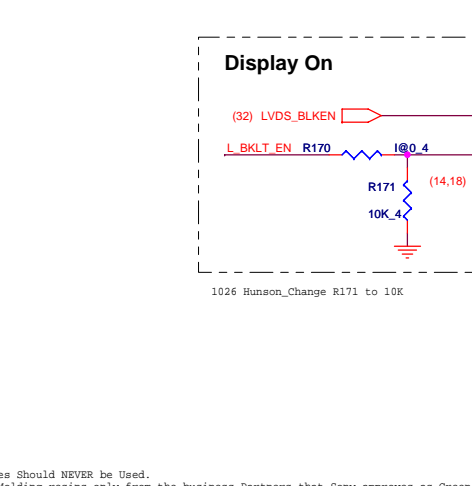
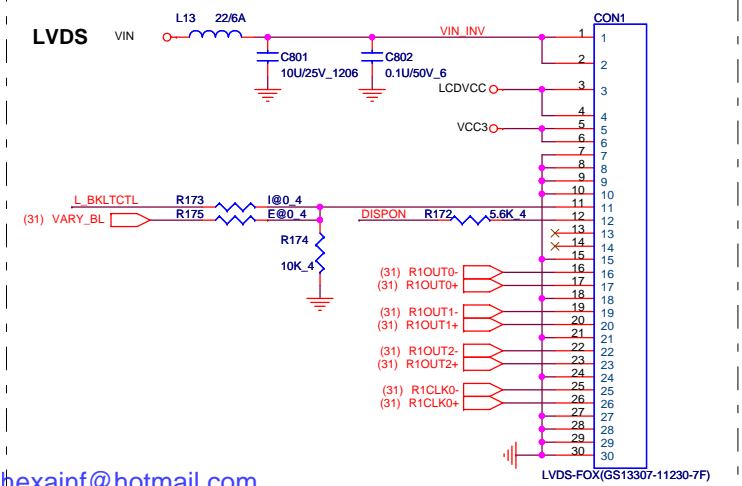


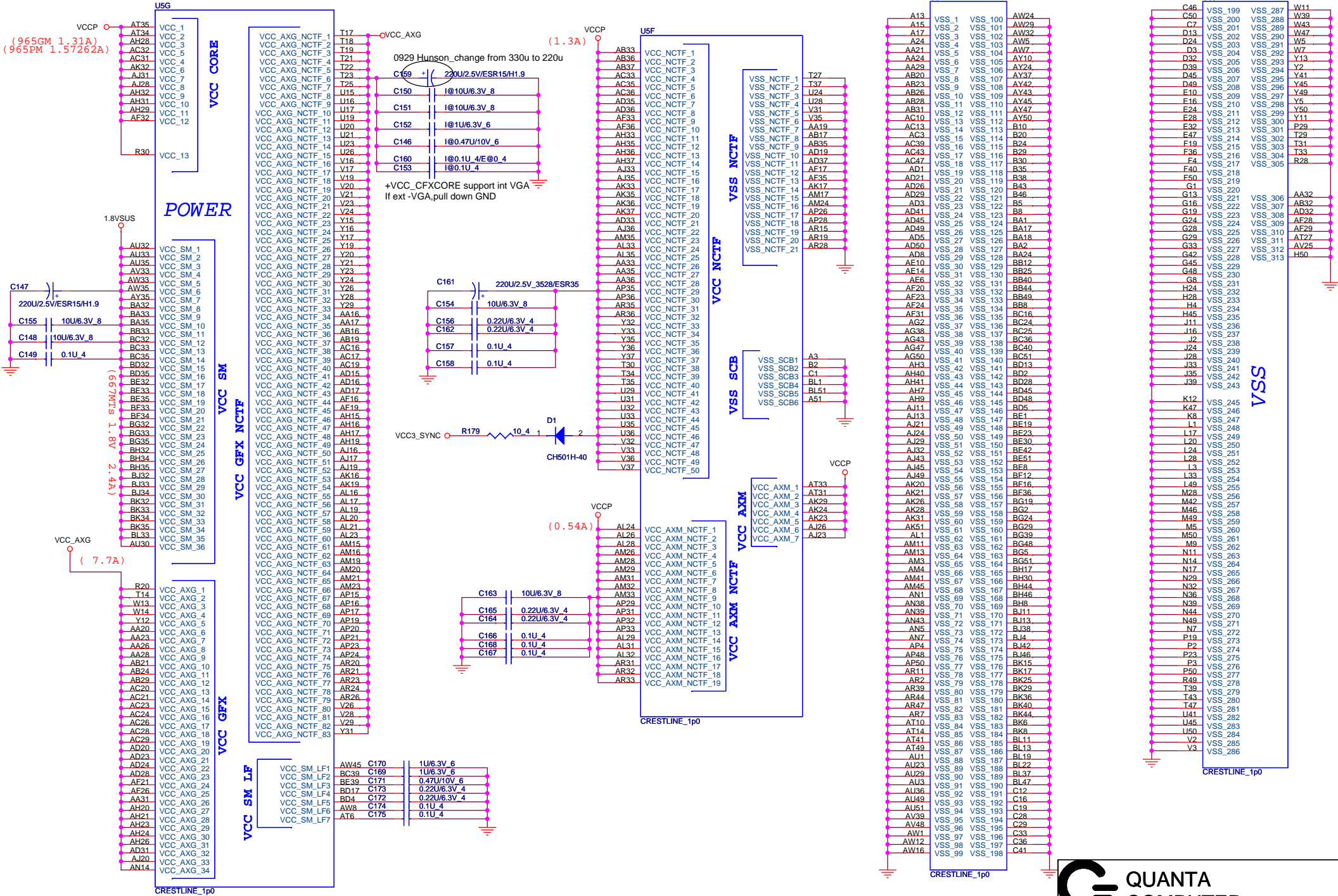
Signal

Signal	GM965	PM965
NB_VSYNC	R158 NI	0_4
NB_B	R155 30.1_4	NI
NB_G	R157 30.1_4	NI
NB_R	R156 30.1_4	NI
L_IBG	R147 2.4K_4	NI
LVDS	RP38 RP41-RP43	0X2 NI
L_BKLT_EN	R170 10K	NI
L_CTRL_CLK	RP46 NI	0X4
L_CTRL_DATA	R145 10K	NI
LVDS_VDDEN	R146 0_4	NI
DDC2BC	R163 0_4	NI
DDC2BD	R164 0_4	NI
CRT_TVO_IREF	R167 1.3K_4	0
L_DDC_CLK	RP46 NI	0X4
L_DDC_DATA	RP46 NI	0X4
BRIGHT	R173 0_4	NI
	R175 NI	0_4



Signal		965GM	965PM
NB_B	R160 0_4	NI	0_4
NB_G	R157 150_4	NI	0_4
NB_R	R156 0_4	NI	0_4
L_IBG	R147 2.4K_4	NI	
LVDS	RP38 RP41-RP43	0X2	NI
L_BKLT_EN	R170 0_4	NI	
L_CTRL_CLK	R130 10K	NI	
L_CTRL_DATA	RP46 NI	0X4	
LVDS_VDDEN	R146 0_4	NI	
DDC2BC	R163 0_4	NI	
DDC2BD	R164 0_4	NI	
CRT_TVO_IREF	R167 1.3K_4	0	
L_DDC_CLK	RP46 NI	0X4	
L_DDC_DATA	RP46 NI	0X4	
BRIGHT	R173 0_4	NI	
	R175 NI	0_4	





QUANTA COMPUTER

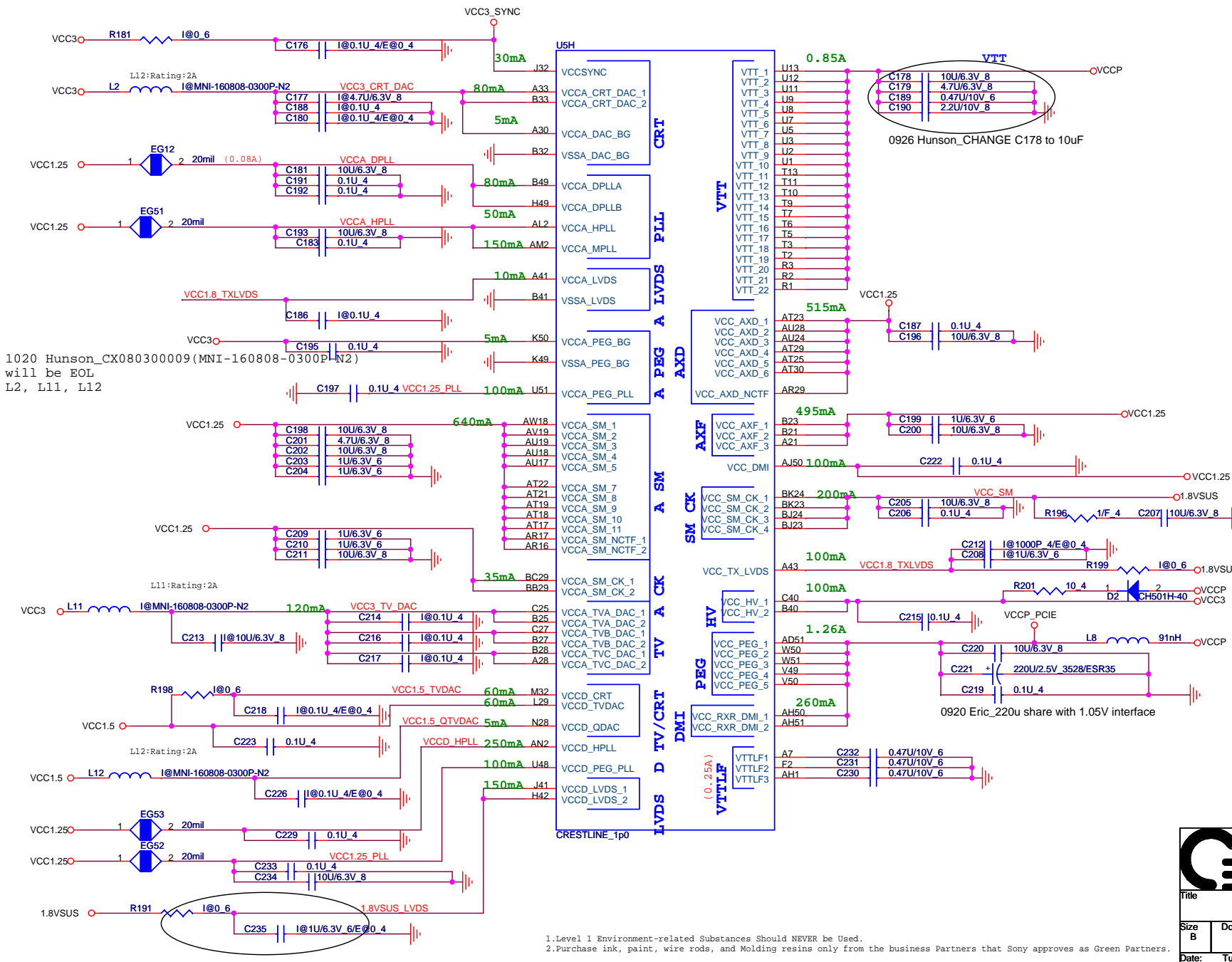
GMCH Power 4 of 5

GD1 Main Board

Rev 1A

Tuesday, November 14, 2006

1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony Approves as Green Partners.



1020 Hunson_CX080300009 (MNI-160808-0300P-N2) will be EOL L2, L11, L12

Signal		965GM	965PM
VCCA_TV_DAC	L12	v	x
	C244	v	x
	C245	v	x
	C246	v	x
	C248	v	x
	R193	x	v
VCC1.5_TV DAC	L14	v	x
	C250	v	x
	C247	v	x
	R195	x	v
VCC1.5_QTV DAC	L17	v	x
	C257	v	x
	C258	v	x
	R197	x	v

Signal		965GM	965PM
VCCA_DAC_BG	L8	v	x
	C214	v	x
	R181	x	v
VCCSYNC	R177	v	x
	C201	v	x
	C202	v	x
	R178	x	v
VCC3_CRT_DAC	L7	v	x
	C203	v	x
	C211	v	x
	R179	x	v
VCCD_LVDS	R198	v	x
	C265	v	x
	C264	v	x
	R199	x	v
VCCA_LVDS	R183	0_4	NC
	C208	0.01u_4	NC
	C209	0.1u_4	NC
	R184	NC	0_4
VCC_TX_LVDS	R192	v	x
	C240	v	x
	C238	v	x
	C239	v	x
	R191	x	v

QUANTA COMPUTER

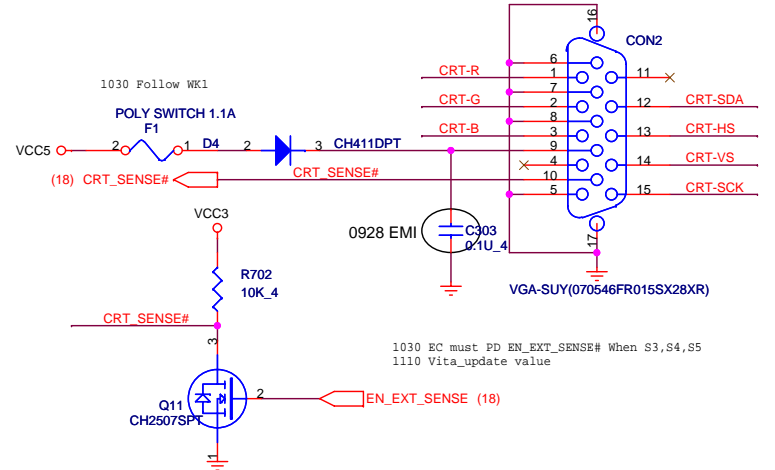
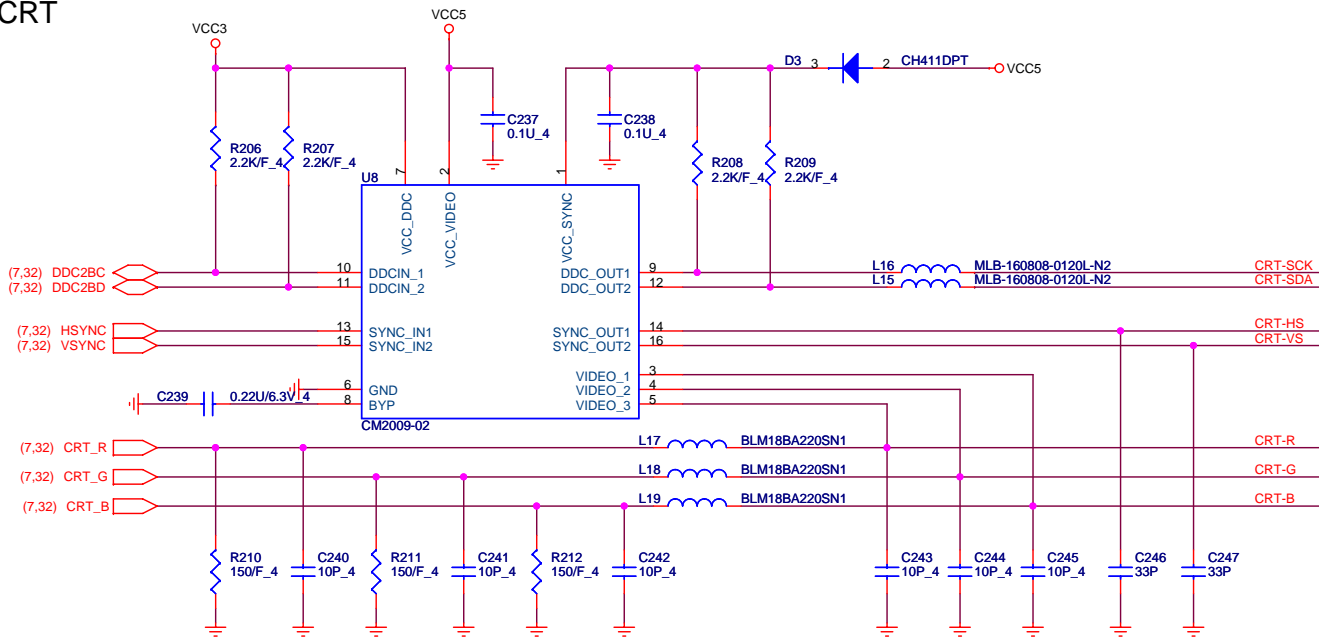
Title: **GMCH Power 2.5 of 5**

Size B Document Number: **GD1 Main Board** Rev 1A

Date: Tuesday, November 14, 2006 Sheet 9 of 35

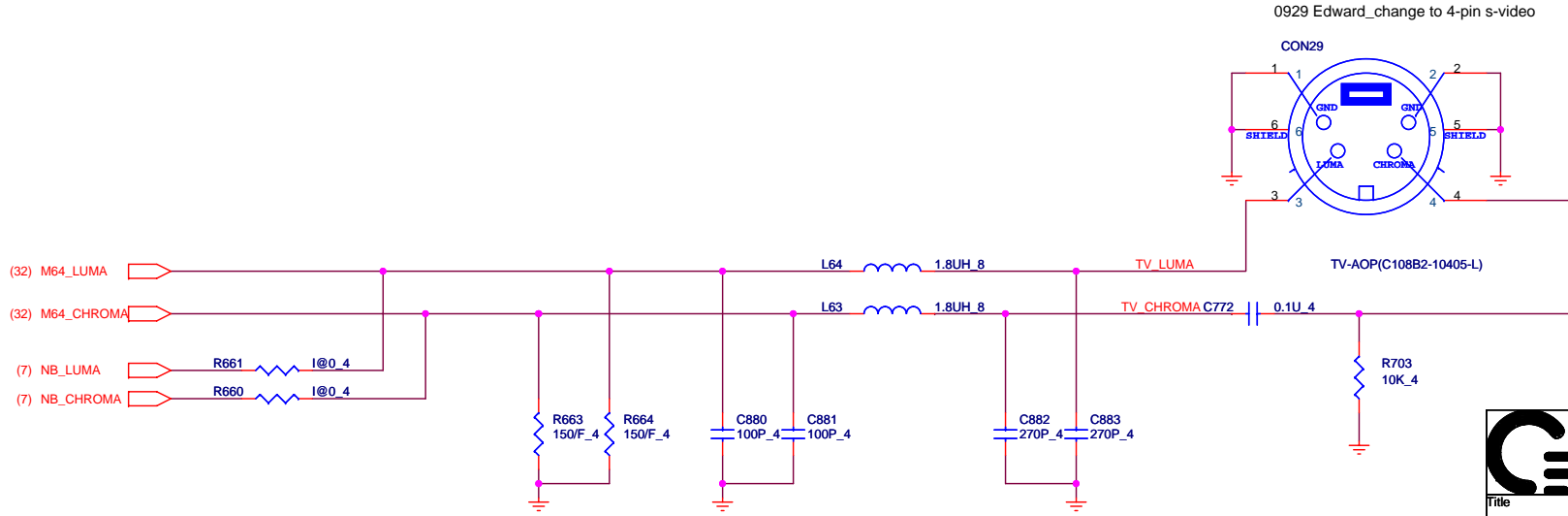
1. Level 1 Environment-related Substances should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

CRT



1030 EC must PD EN_EXT_SENSE# When S3,S4,S5
1110 Vita_update value

S-VIDEO_OUT



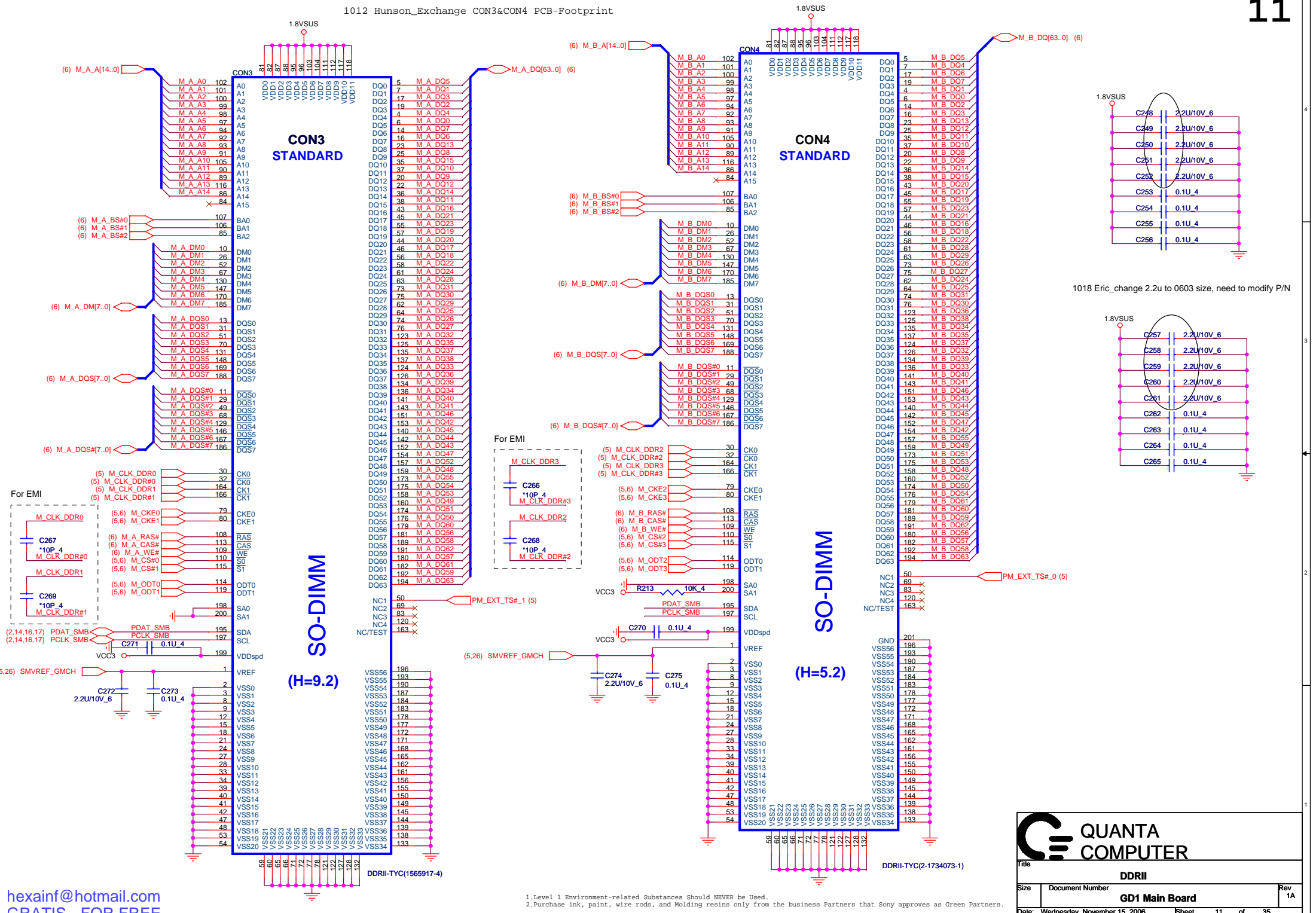
QUANTA COMPUTER

Title: **CRT & S-VIDEO**

Size B Document Number: **GD1 Main Board** Rev 1A

Date: Wednesday, November 15, 2006 Sheet 10 of 35

1.Level 1 Environment-related Substances should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



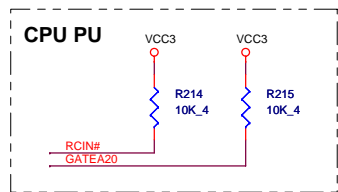
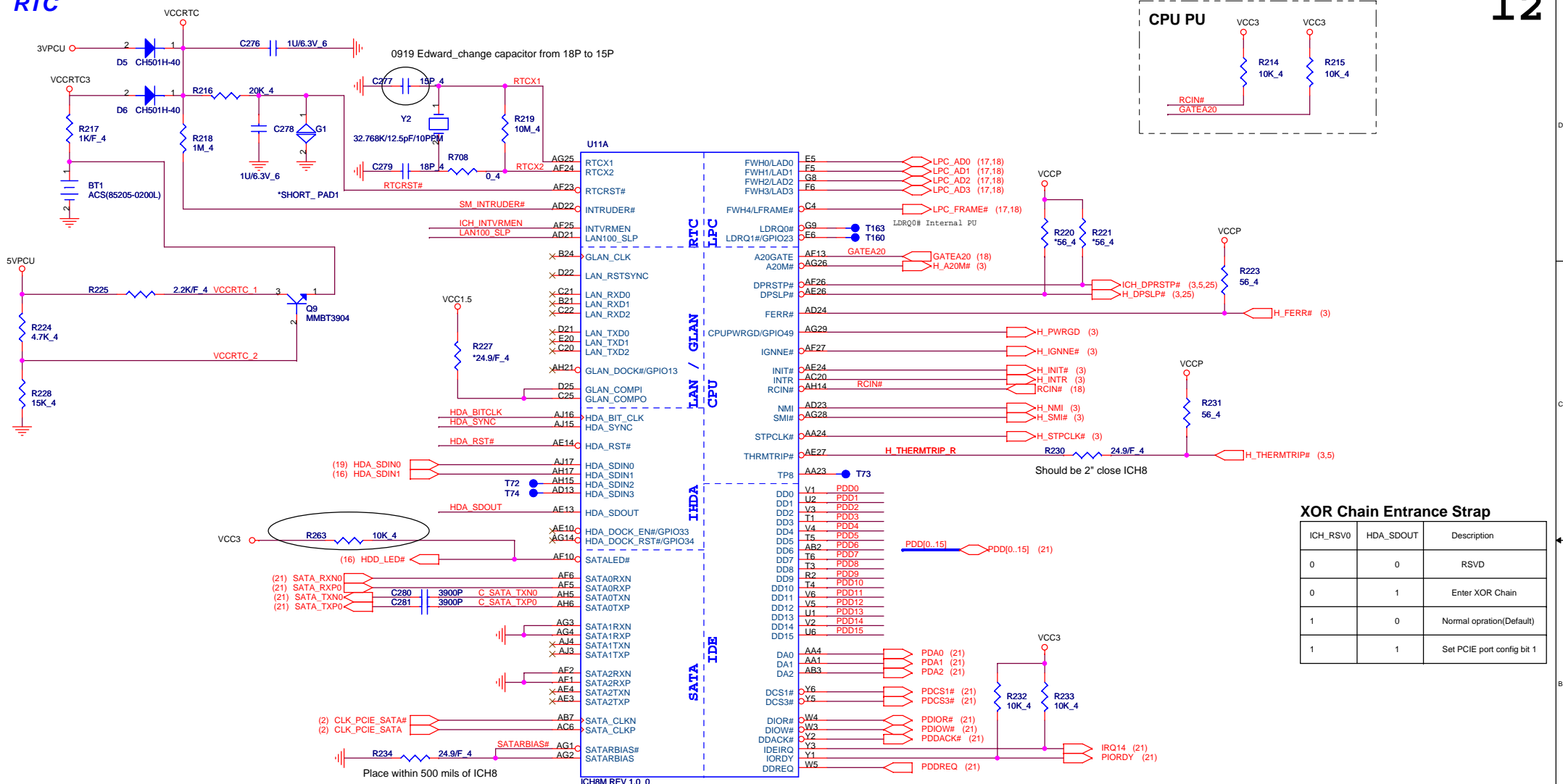
QUANTA COMPUTER

Title: **DDRII**

Size: **GD1 Main Board**

Date: **Wednesday, November 15, 2006** Sheet **11** of **35**

Rev: **1A**



XOR Chain Entrance Strap

ICH_RSV0	HDA_SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal operation(Default)
1	1	Set PCIe port config bit 1

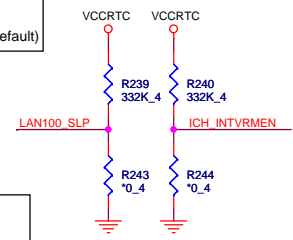
ICH8 strap

ICH8-M LAN100_SLP Strap
(Internal VR for VccLAN1_05 and VccCL1_05)

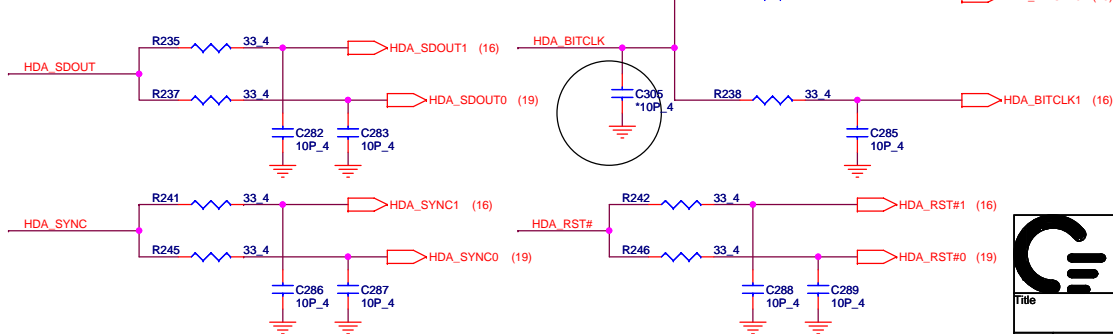
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)
------------	---

ICH_INTVRMEN	Low = Disable High = Enable(Default)
--------------	---

ICH8-M Internal VR Enable strap
(Internal VR for Vccsus1_05, VccSus1_5 and VccCL1_5)



HD Audio to Codec and Modem



1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: **ICH8-M HOST 1 of 4**

Size	Document Number	Rev
	GD1 Main Board	1A

Date: Tuesday, November 14, 2006 Sheet 12 of 35

PCI bus info.

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
T18402	AD23	REQ0# / GNT0#	PIRQ E/F/G

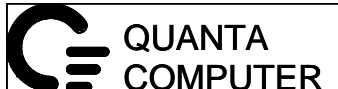
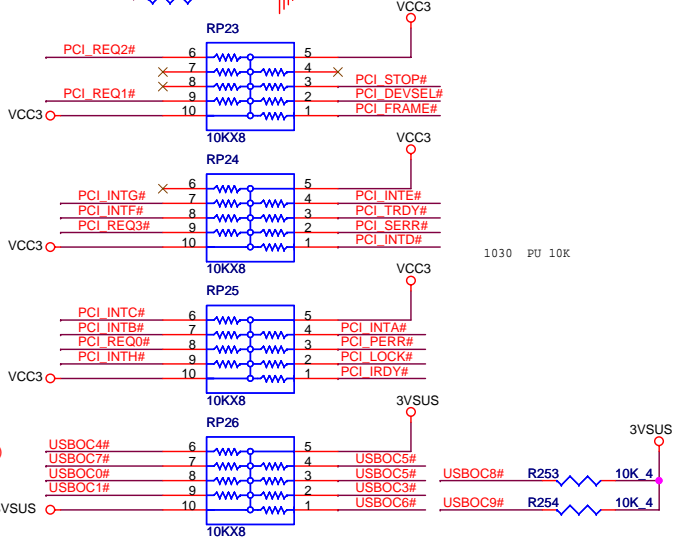
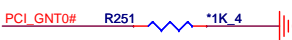
A16 SWAP Override strap

PCI_GNT#3	Low = A16 swap override enabled High = Default
-----------	---



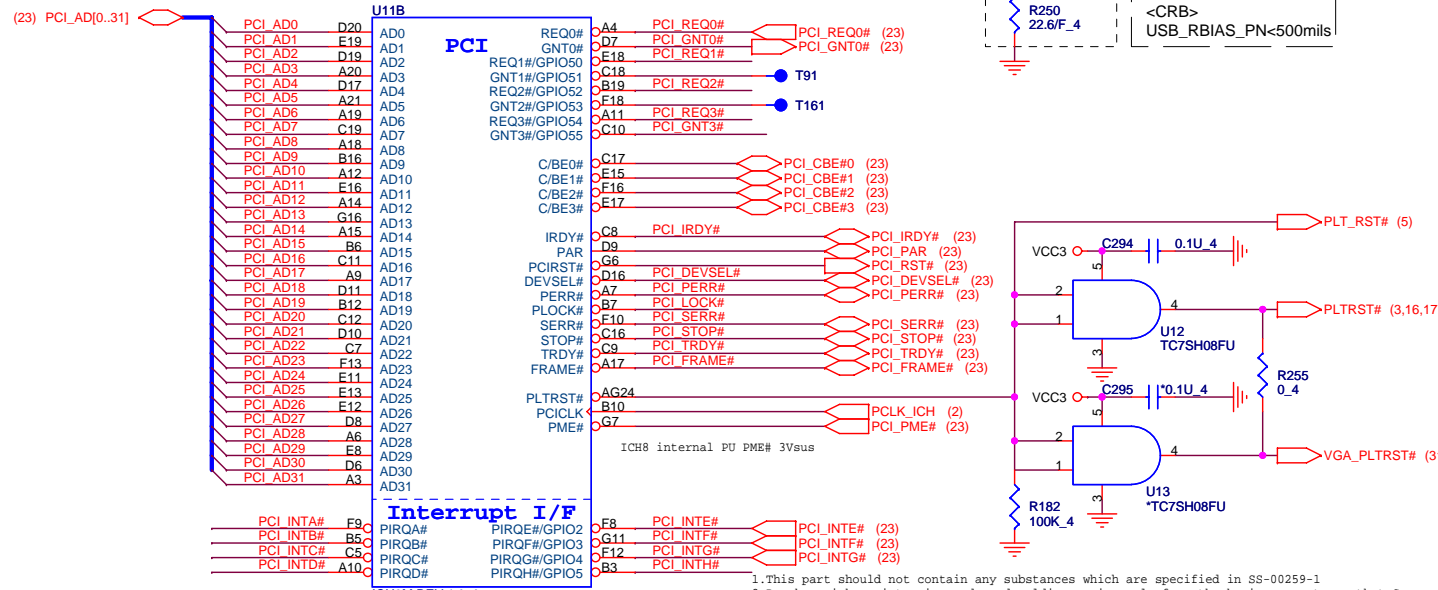
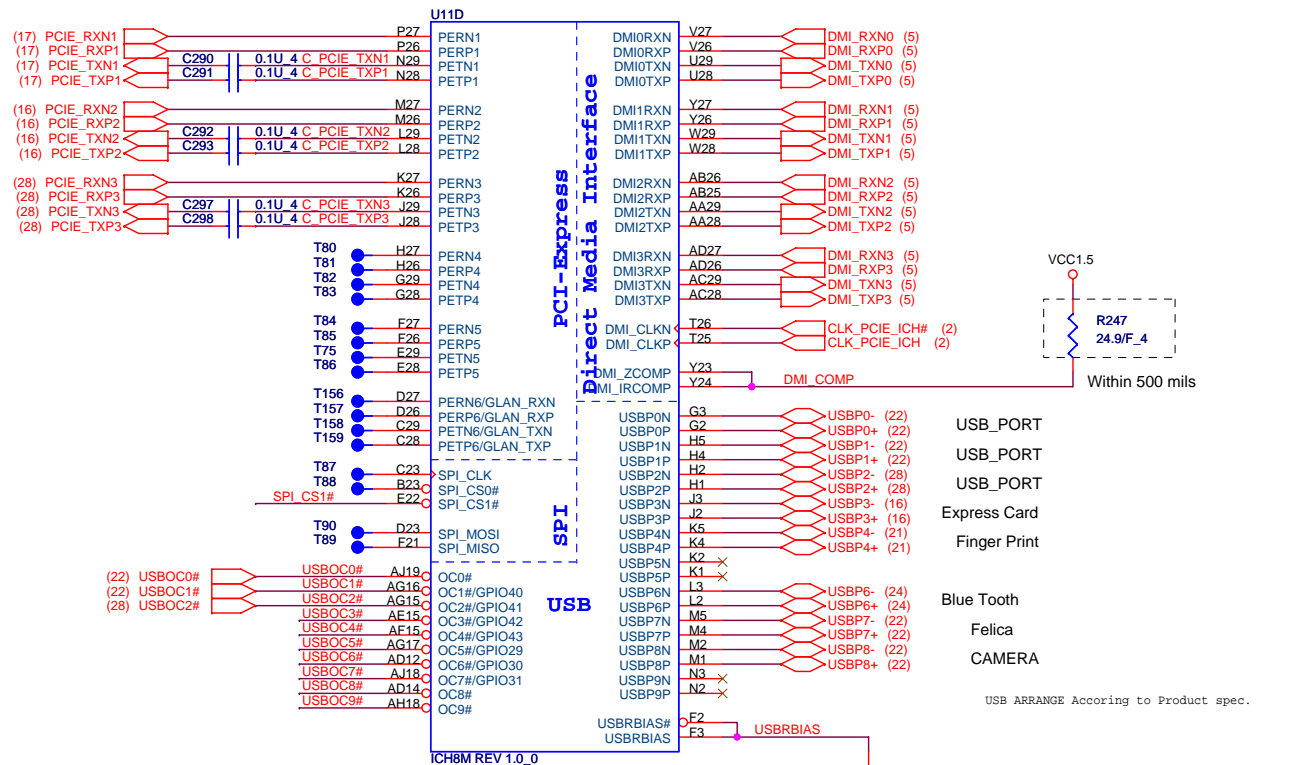
ICH8 Boot BIOS select

PCI_GNT#0	SPI_CS#1	Boot BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

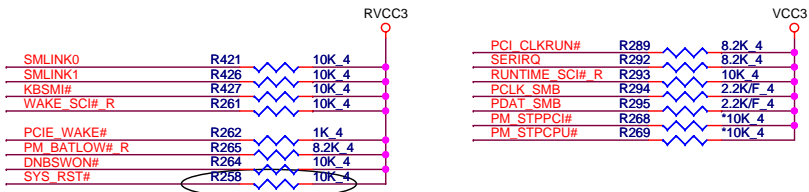


Title			ICH8-M PCIE 2 of 4		
Size	Document Number				Rev
B	GD1 Main Board				1A
Date:	Tuesday, November 14, 2006	Sheet	13	of	35

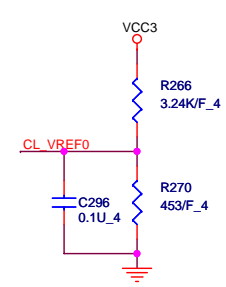
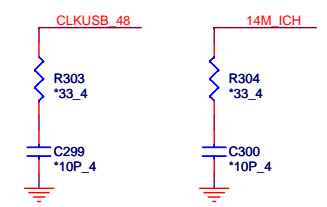
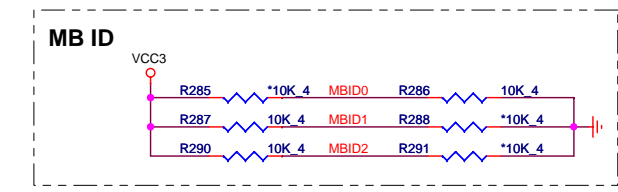
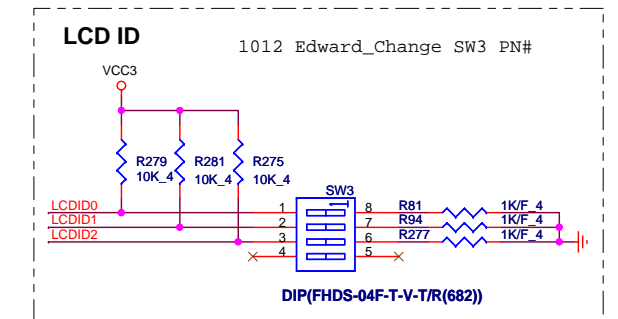
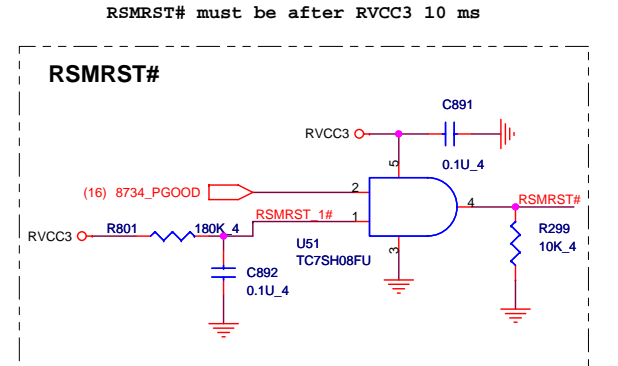
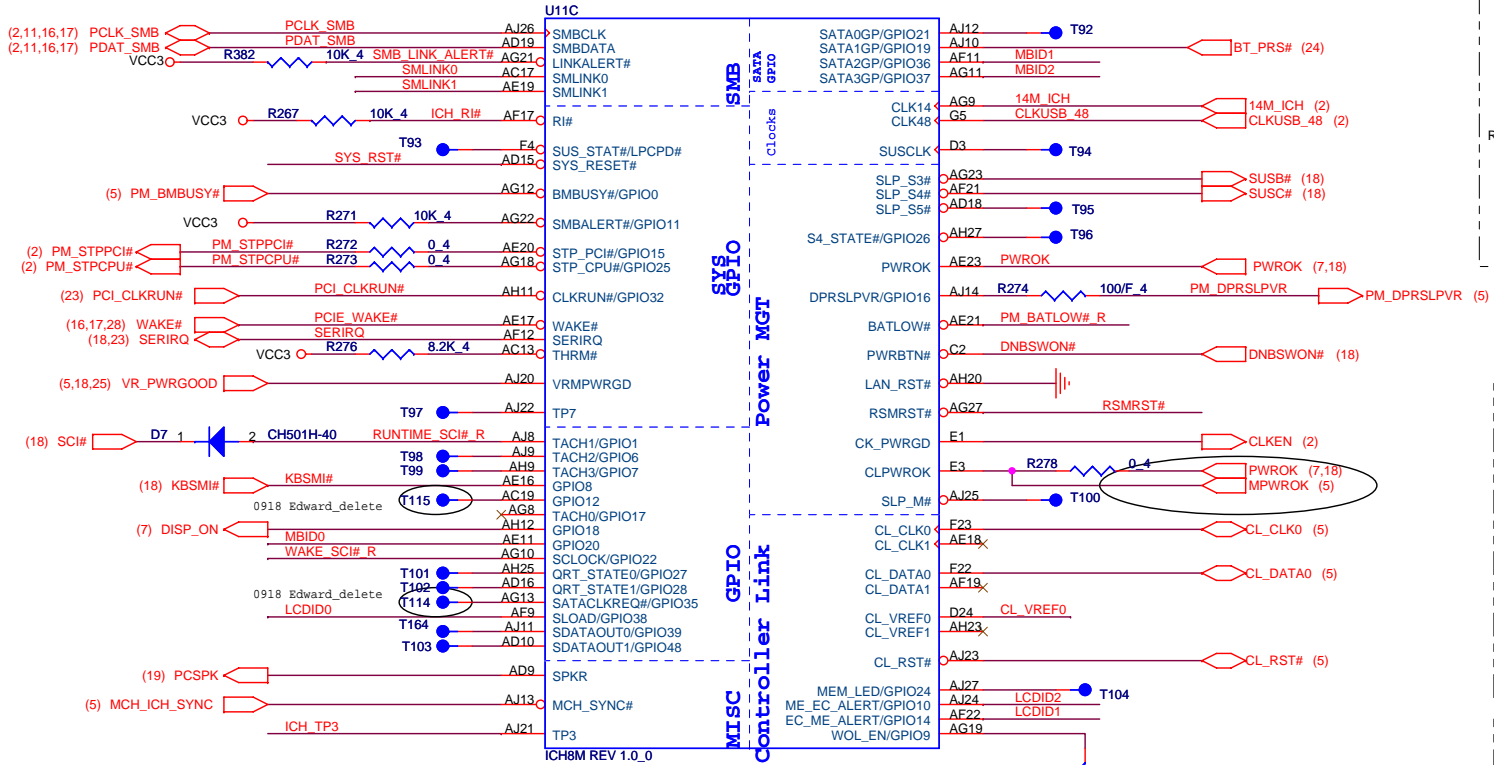
WireLess Lan
Express card
10/100 Lan



1. This part should not contain any substances which are specified in SS-00259-1
 2. Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.



0915 Edward.Tsai follow intel check list

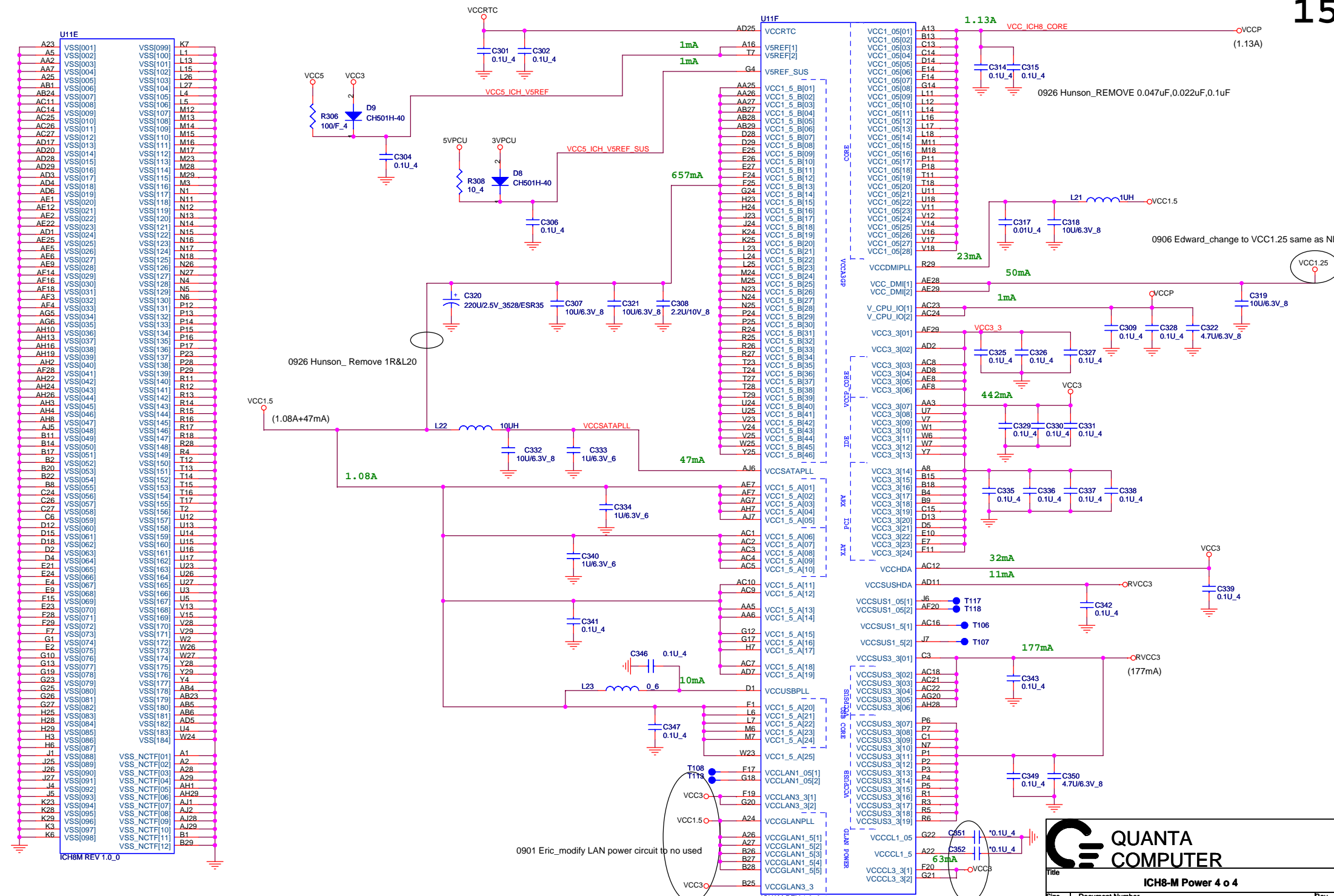


1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: **ICH8-M GPIO 3 of 4**

Size B	Document Number	Rev 1A
GD1 Main Board		
Date:	Wednesday, November 15, 2006	Sheet 14 of 35



hexainf@hotmail.com
 GRATIS - FOR FREE

1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Welding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: **ICH8-M Power 4 o 4**

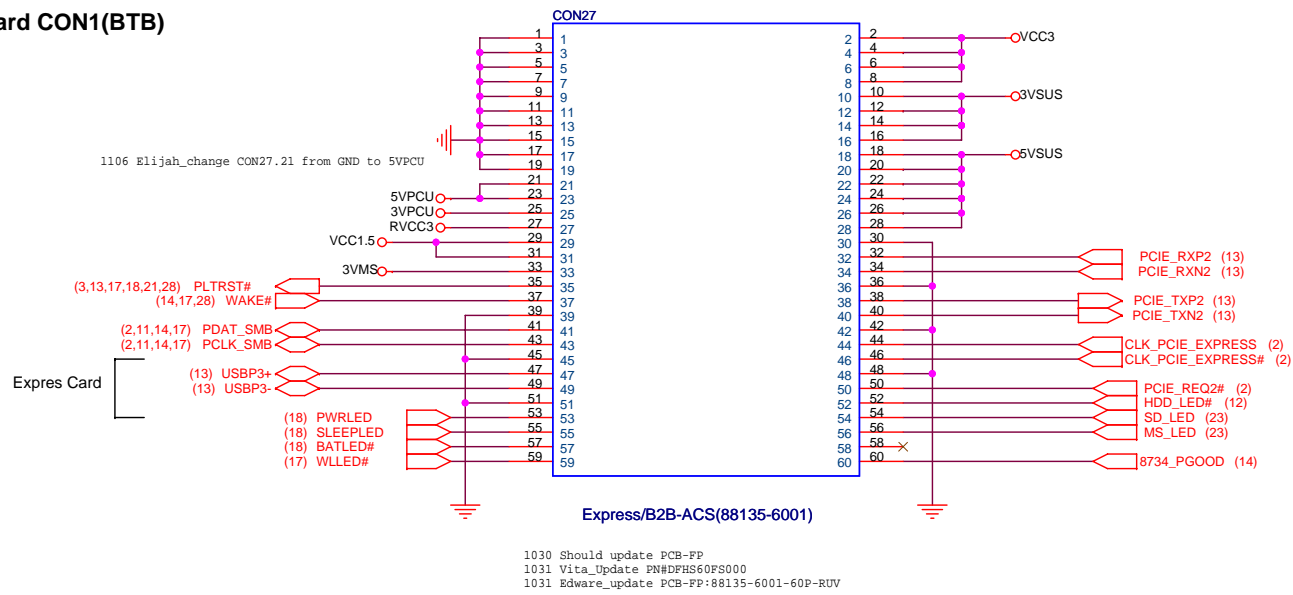
Size	Document Number	Rev
	GD1 Main Board	1A
Date:	Tuesday, November 14, 2006	Sheet 15 of 35

0901 Eric_modify LAN power circuit to no used

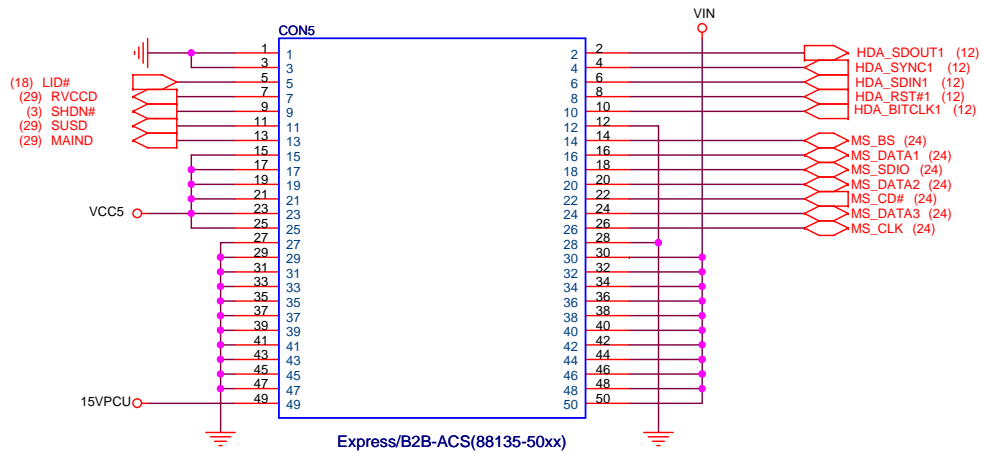
ICH8M REV 1.0_0

ICH8M REV 1.0_0

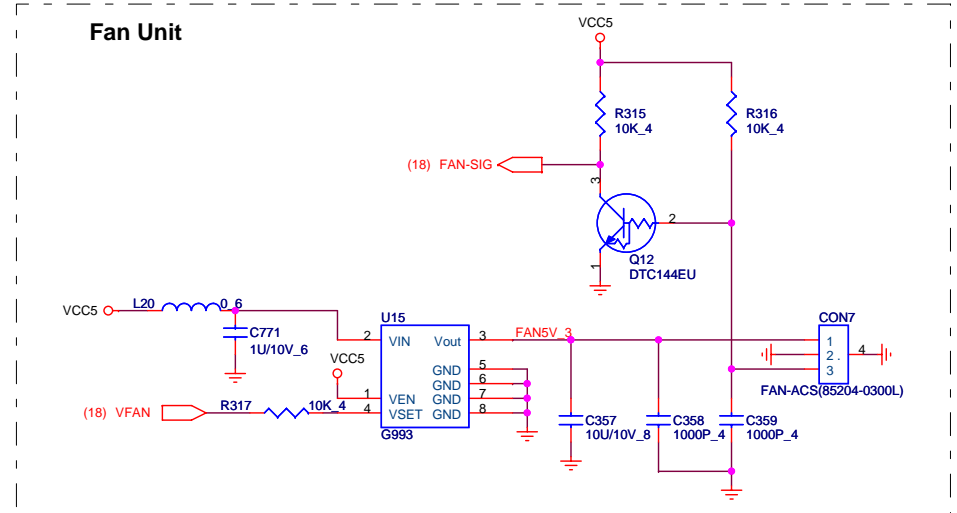
Express Board CON1(BTB)



Express Board CON2(BTB)



Fan Unit



Title			Rev
Express Card			1A
Size	Document Number	GD1 Main Board	
B			
Date:	Tuesday, November 14, 2006	Sheet	16 of 35

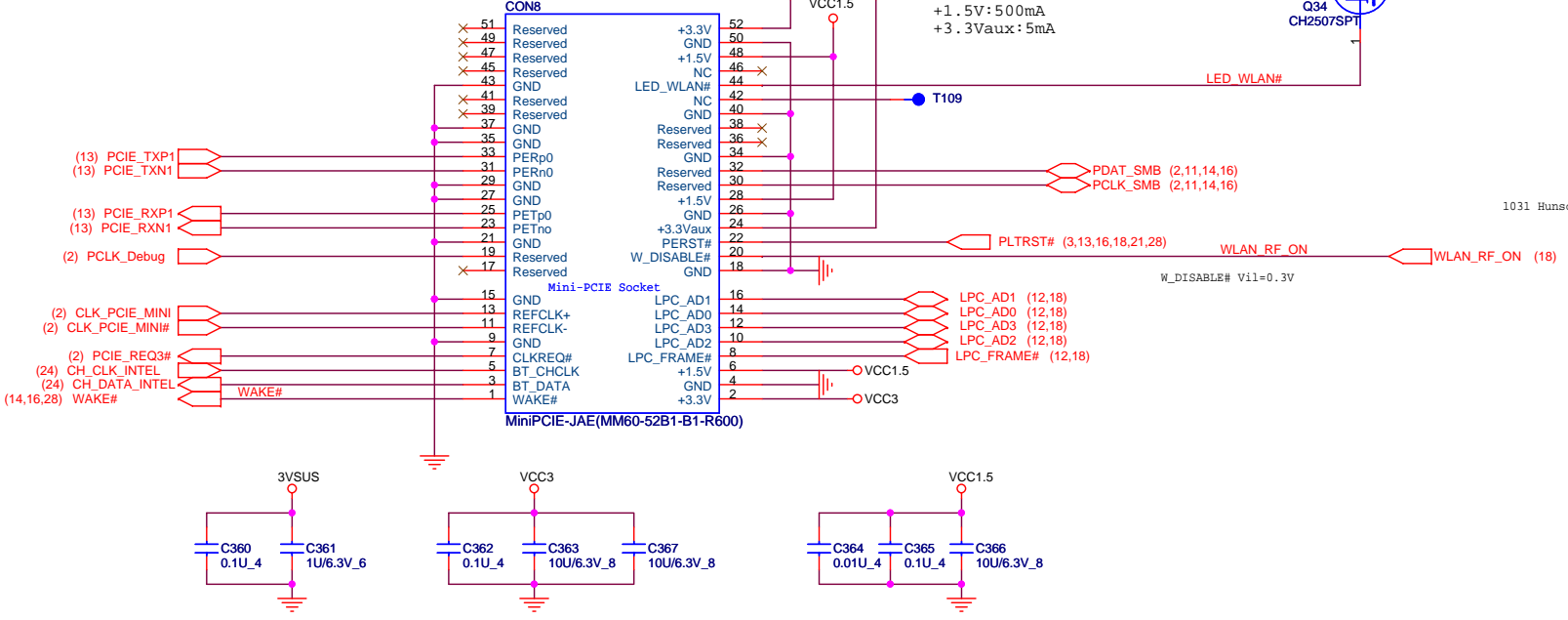
1.This part should not contain any substances which are specified in SS-00259-1
2.Purchase ink, paint, wire rods and molding resins only from the business partners that Sony approves as Green Partners.

LED_GP :LED WLEN LINK
Output Current : 7mA
Blink rate : 1 flash per every 3 sec.

WLSW:
Low : disable the radio.
High : Enable the radio.

LED_WLAN# MAX sink current=16mA
(recommend<=14mA)
Drive in LED/B
+3.3V:1A
+1.5V:500mA
+3.3Vaux:5mA

Mini PCI-E Card FOR WL



1031 Hunson_Must ADD NMOS,R LED in Express/B

QUANTA COMPUTER

Title: **MINIPCIE / MDC**

Size B Document Number: **GD1 Main Board** Rev 1A

Date: **Wednesday, November 15, 2006** Sheet 17 of 35

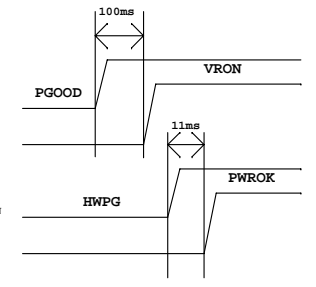
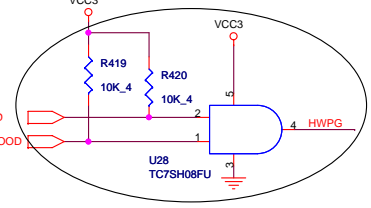
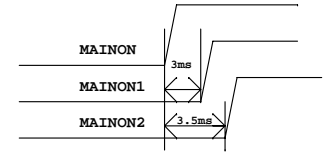
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

I/O Address		
BADDR1-0	Index	Data
1 0	2E	2F
1 1	4E	4F
0 0	(HCFGBAH, HCFGBAL) (HCFGBAH, HCFGBAL)+1	
0 1	XOR-TREE TEST	

DOCK_RST# = BADDR0
 BK_BAT_PWRN: BADDR1
 BT_PEN# : SHBM(If = 0 Enable share host BIOS memory)

PWROK must be after HWPG at least 10ms
 VRON must be after PGOOD at least 99ms

MAINON <-- 3ms --> MAION1
 MAINON <-- 3.5ms --> MAION2

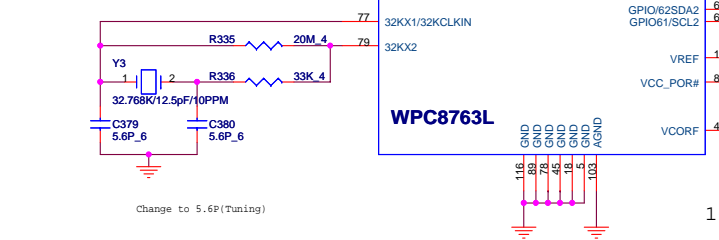
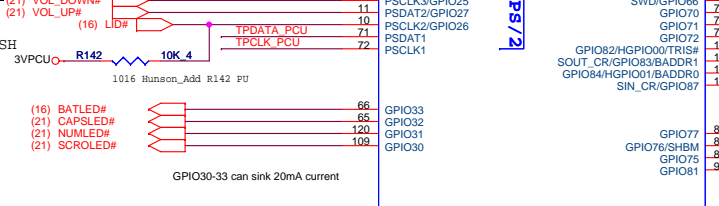
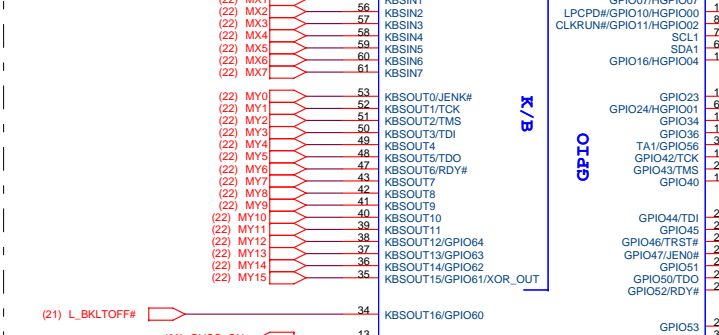
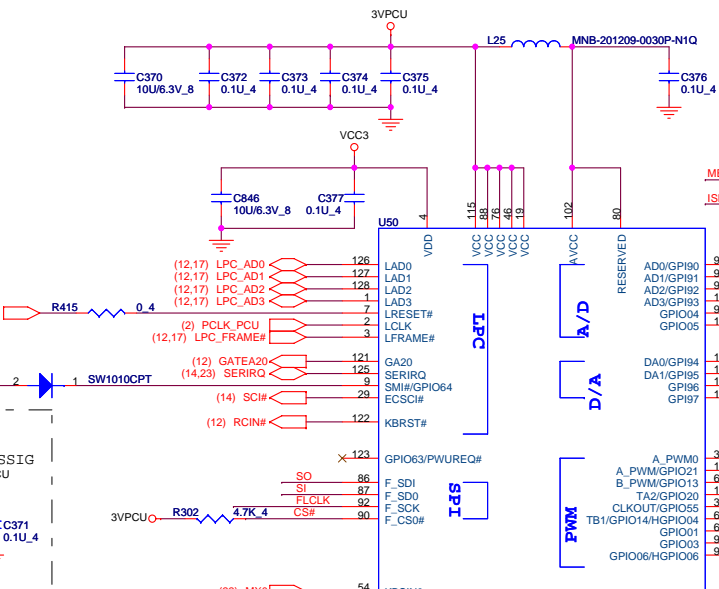
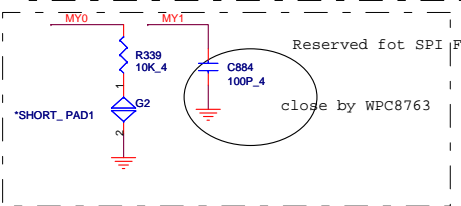
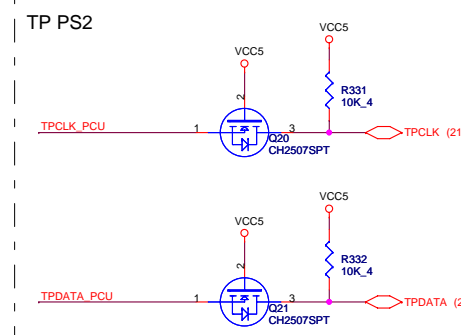
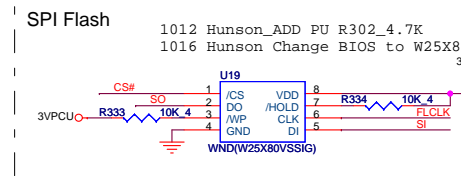
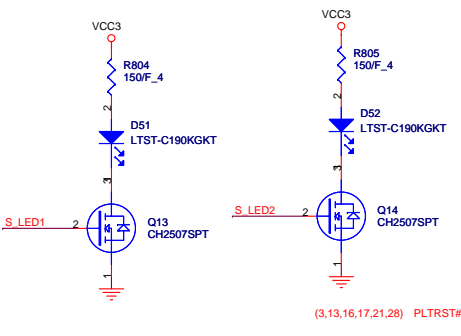


0901 Hunson_volmute is low active

0831 Eric_BT_PEN change to high active

1013 Hunson Add Batt SCK&SDA

1107 Hunson_FAE recommend PD 10K on EVT version



JTAG SELECT CONFIGURATION			
JEN0(PIN24)	JENK(PIN53)	Functionality of PINs (17,20,21,23,25,27)	Functionality of PINs (47,48,50,51,52)
NC	NC	GPIO	KEYBOARD OUTPUT
10K PD	NC	JTAG Signal	KEYBOARD OUTPUT
NC	10K PD	GPIO	JTAG Signal
10K PD	10K PD		Illegal Strap combination

1016 Hunson_Change EC to WPC8763L

1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

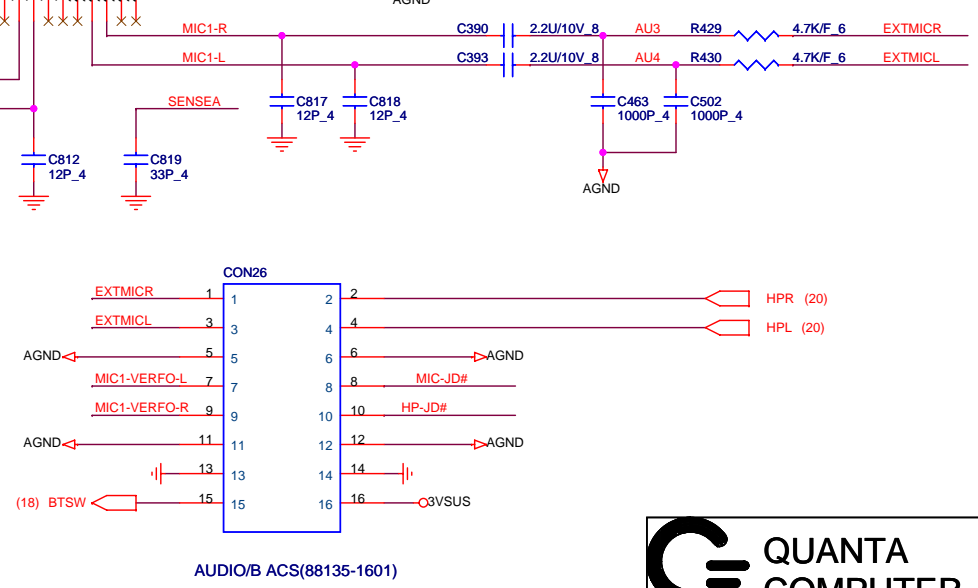
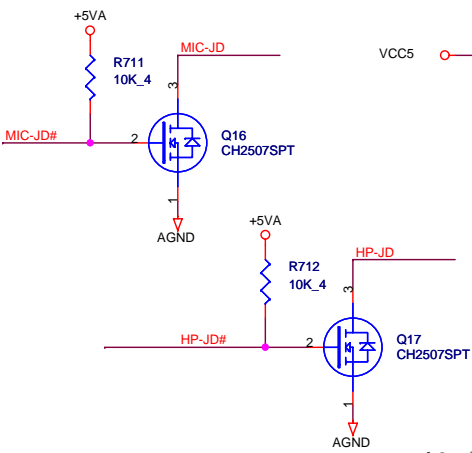
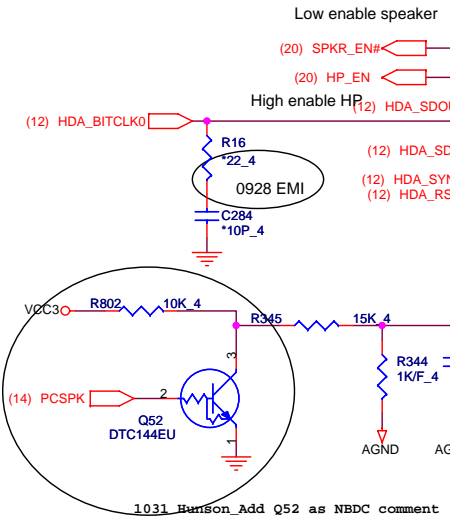
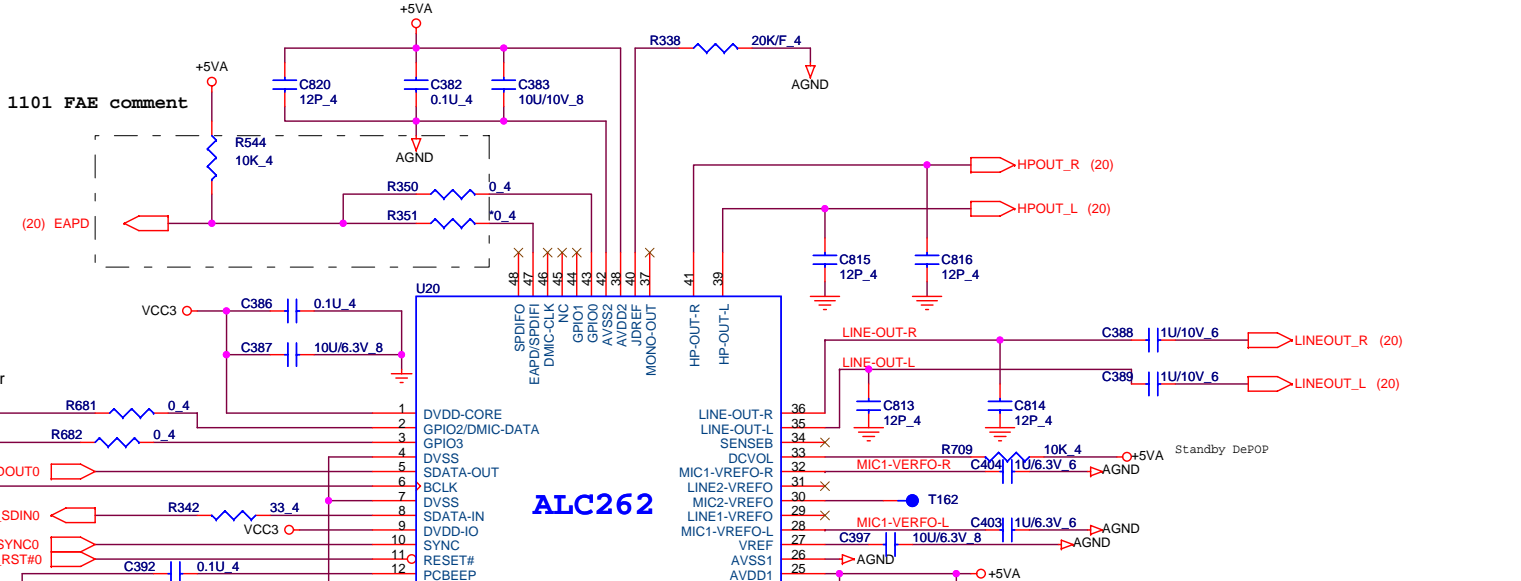
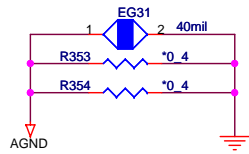
**QUANTA
COMPUTER**

Title: **WPC8763L & SPI FLASH**

Size: Document Number: **GD1 Main Board** Rev 1A

Date: Tuesday, November 14, 2006 Sheet 18 of 35

Audio decoupling



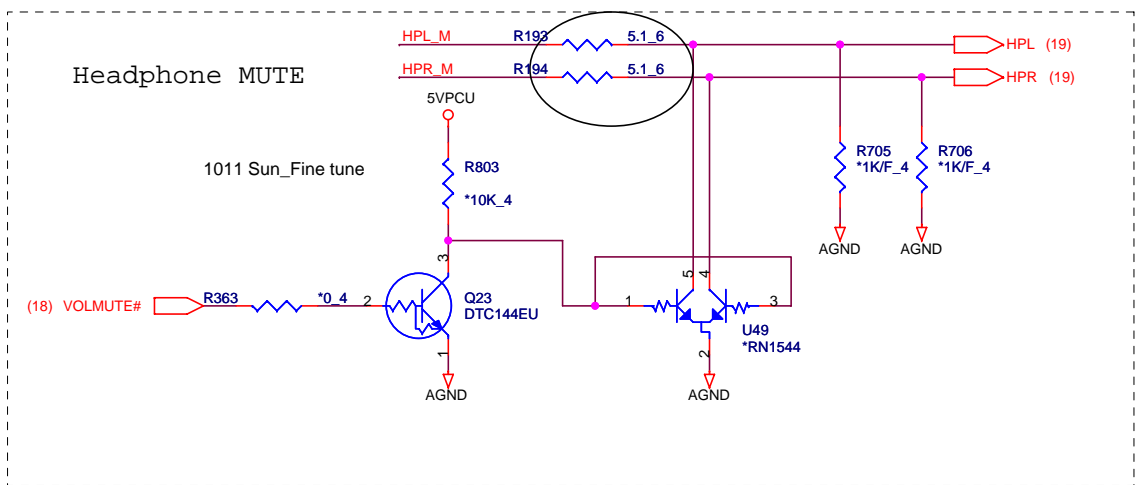
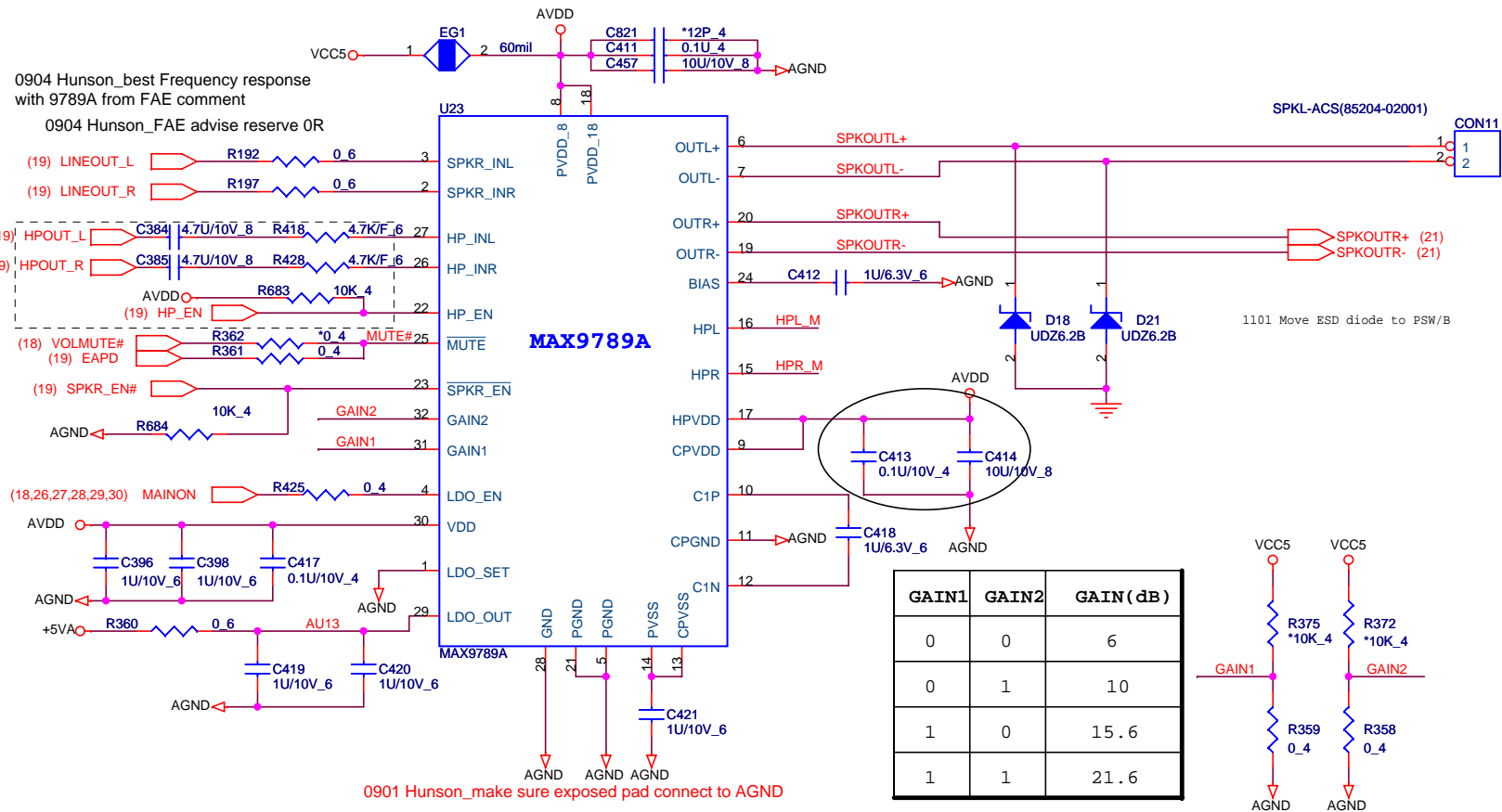
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: **Audio ALC268**

Size: Custom | Document Number: **GD1 Main Board** | Rev: 1A

Date: Tuesday, November 14, 2006 | Sheet: 19 of 35



1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

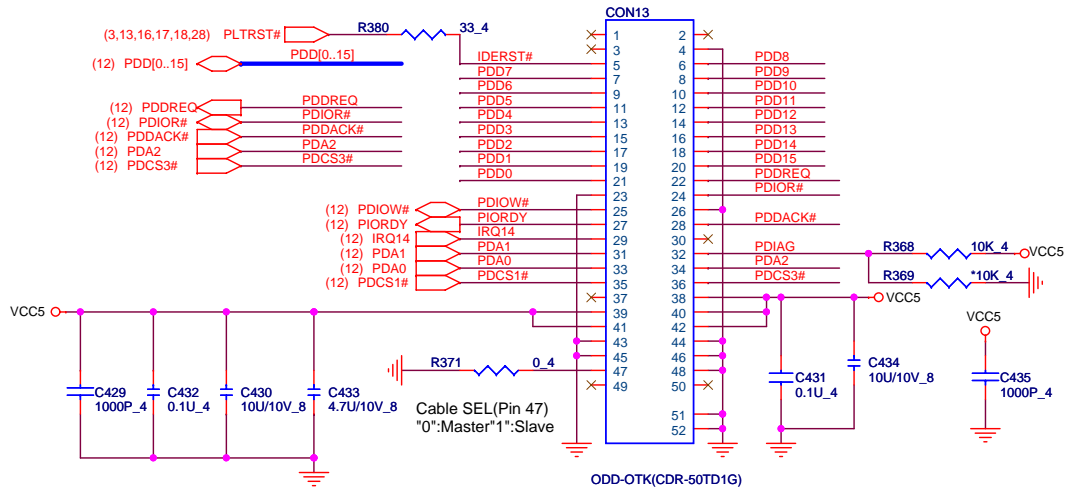
QUANTA COMPUTER

Title: **Audio AMP. & Speaker**

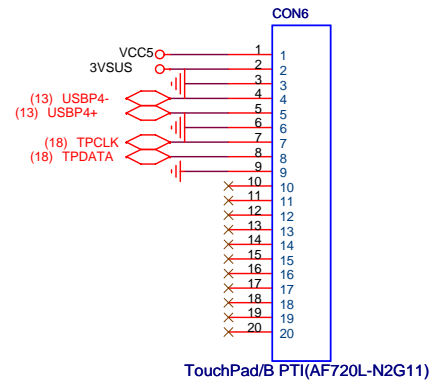
Size: Custom | Document Number: **GD1 Main Board** | Rev: 1A

Date: Tuesday, November 14, 2006 | Sheet: 20 of 35

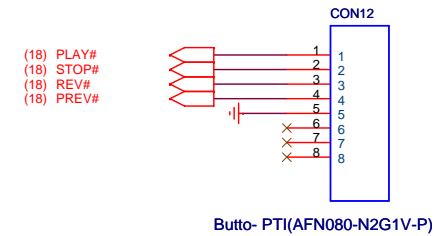
ODD CONNECTOR



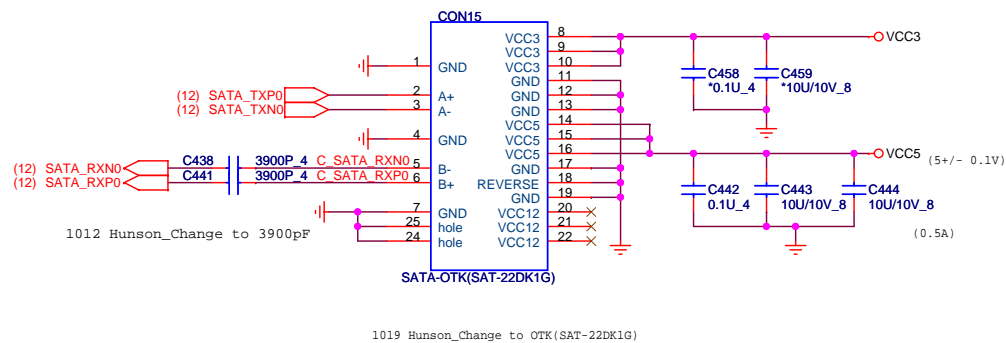
TouchPAD Board CON(FFC)



Button CON(FFC)

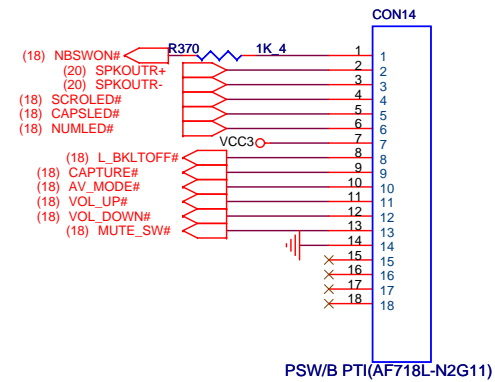


HDD CONNECTOR



PSW Board CON(FFC)

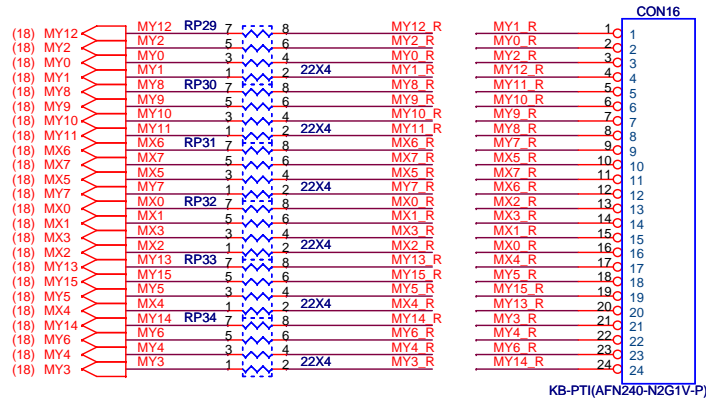
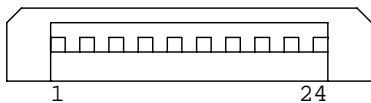
1031 Hunson_update PCB-PP



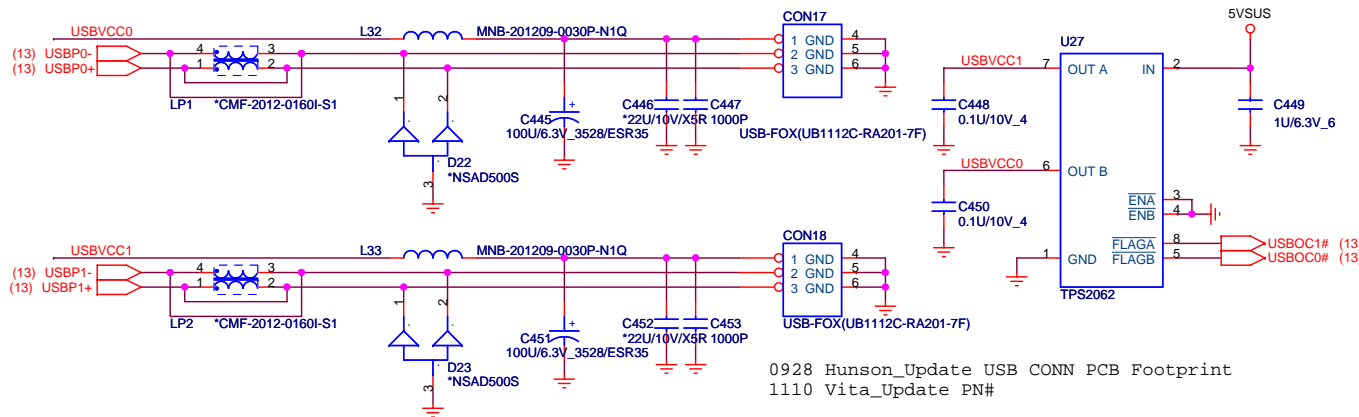
Title		
HDD/ODD/PW CON		
Size	Document Number	Rev
B	GD1 Main Board	1A
Date:	Wednesday, November 15, 2006	Sheet 21 of 35

1.Level 1 Environment-related Substances Should NEVER be Used.
 2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

Keyboard



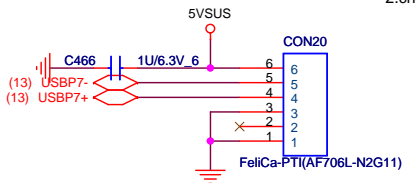
USB Port x 2



0928 Hunson_Update USB CONN PCB Footprint
1110 Vita_Update PN#

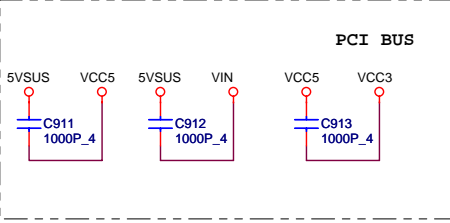
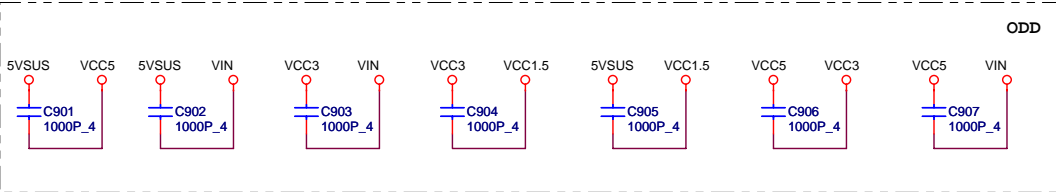
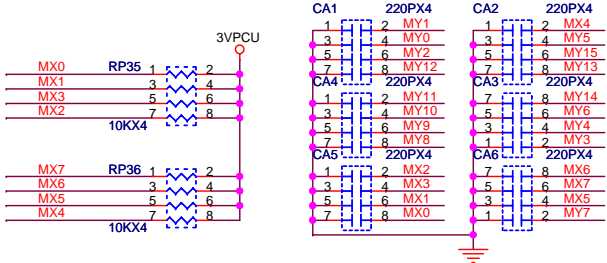
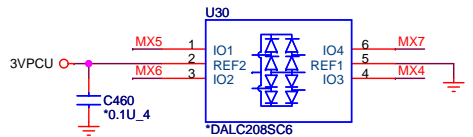
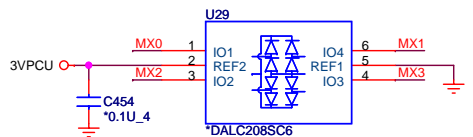
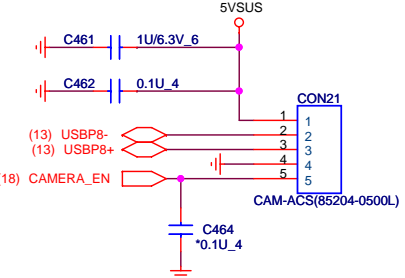
Felica

0929 Eric_
1.change material to gold plating
2.change Foot Print to PTI



1012 Edward_Change CON20 PN#(gold-pating)

USB Camera

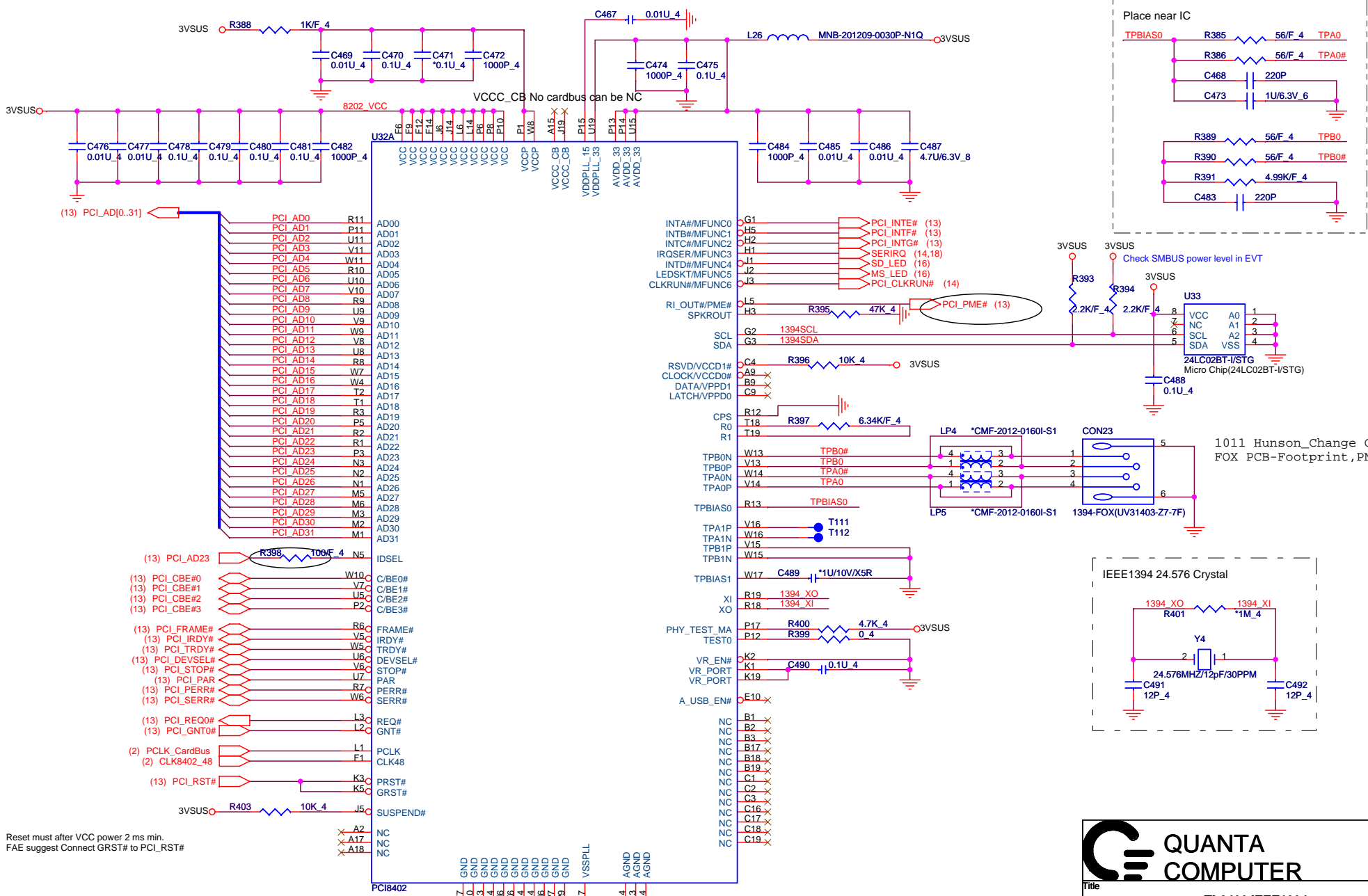


1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: **K/B ,USB Device**

Size B	Document Number	Rev 1A
GD1 Main Board		
Date: Wednesday, November 15, 2006	Sheet 22	of 35



Reset must after VCC power 2 ms min.
FAE suggest Connect GRST# to PCI_RST#

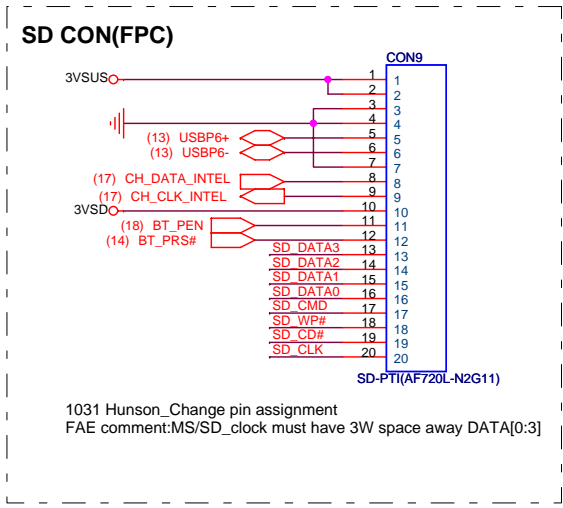
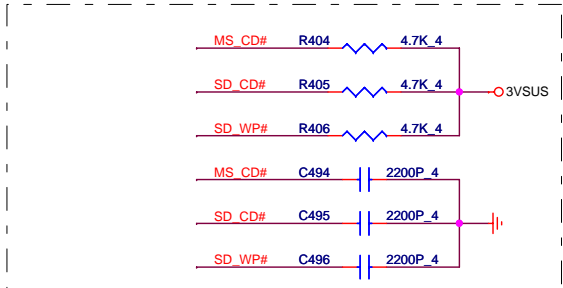
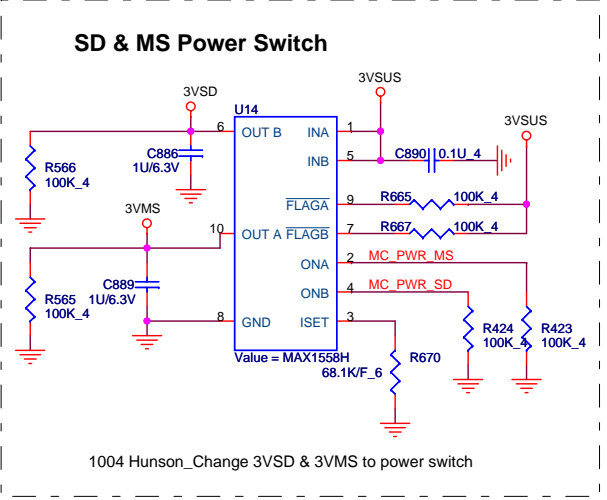
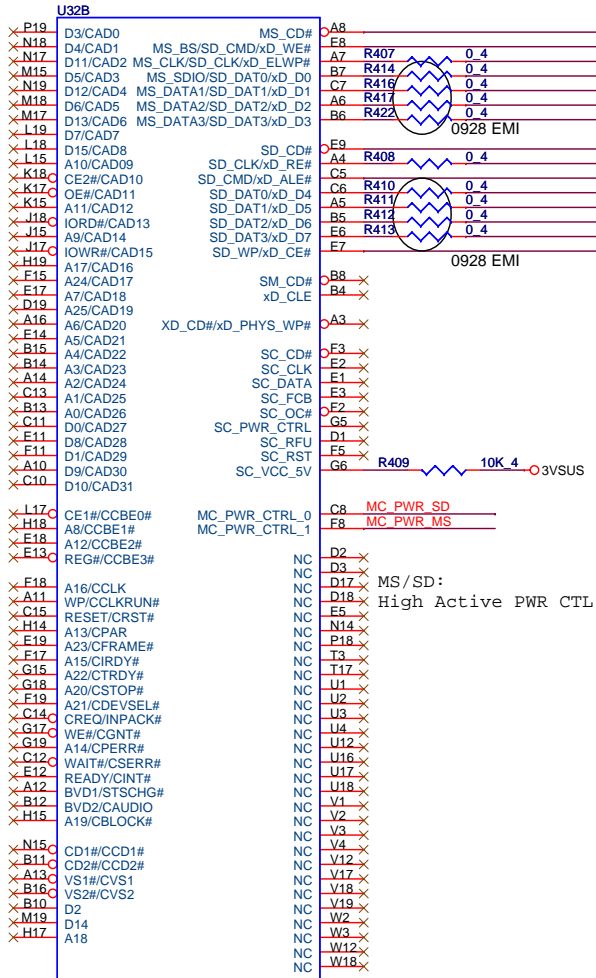
1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA COMPUTER

Title: **TI-8402 IEEE1394**

Size B Document Number: **GD1 Main Board** Rev 1A

Date: **Wednesday, November 15, 2006** Sheet 23 of 35



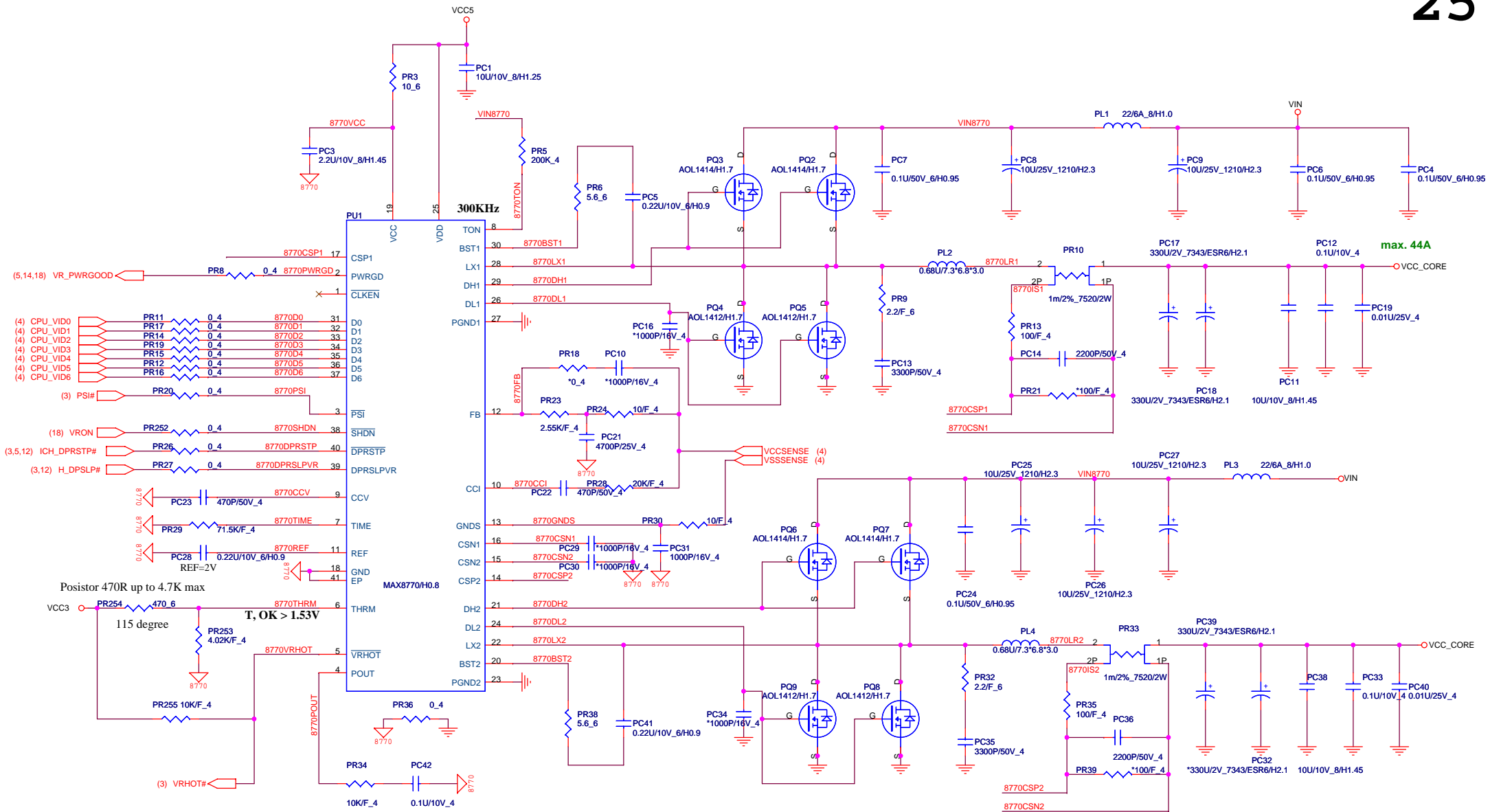
QUANTA COMPUTER

Title: **TI-8402 MS & SD**

Size B Document Number: **GD1 Main Board** Rev 1A

Date: Wednesday, November 15, 2006 Sheet 24 of 35

1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.



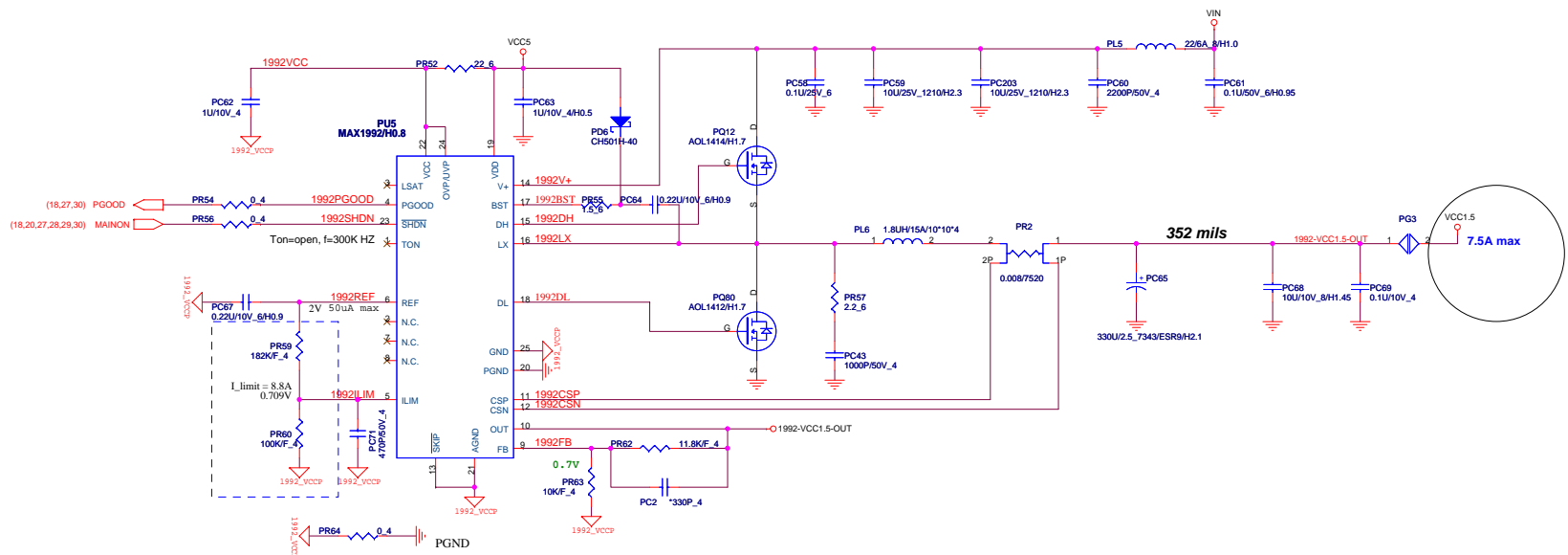
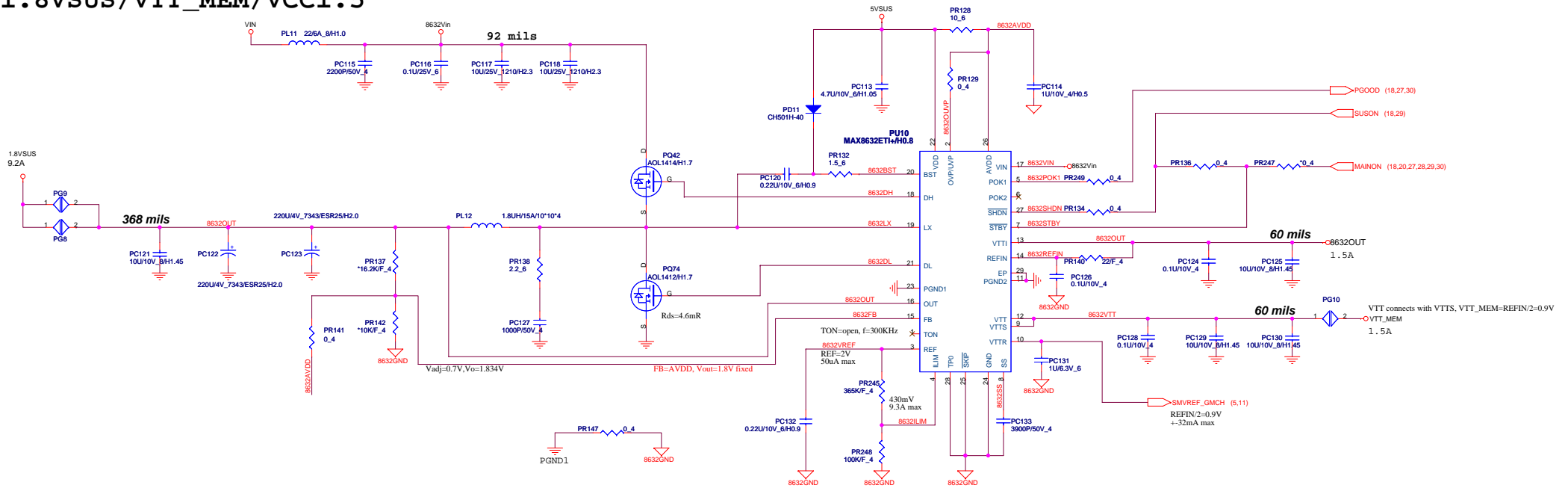
In progress

QUANTA COMPUTER

Title: **CPU CORE (MAX8770)**

Size: Custom Document Number: **RD3 Main Board** Rev: 1A

Date: Tuesday, November 14, 2006 Sheet 25 of 35



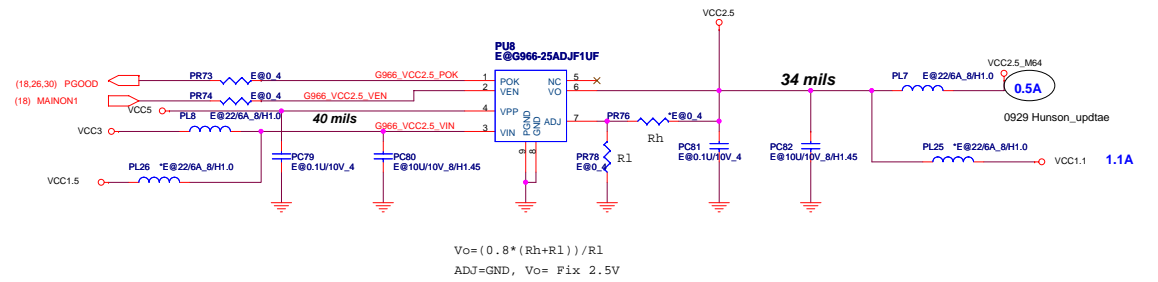
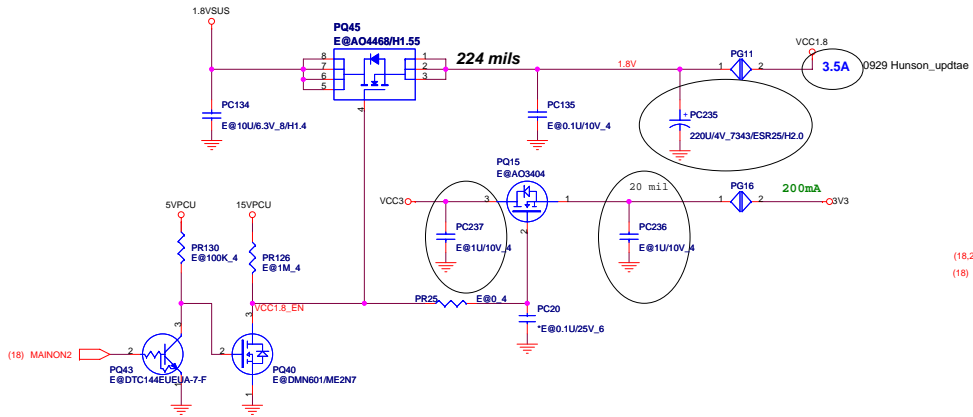
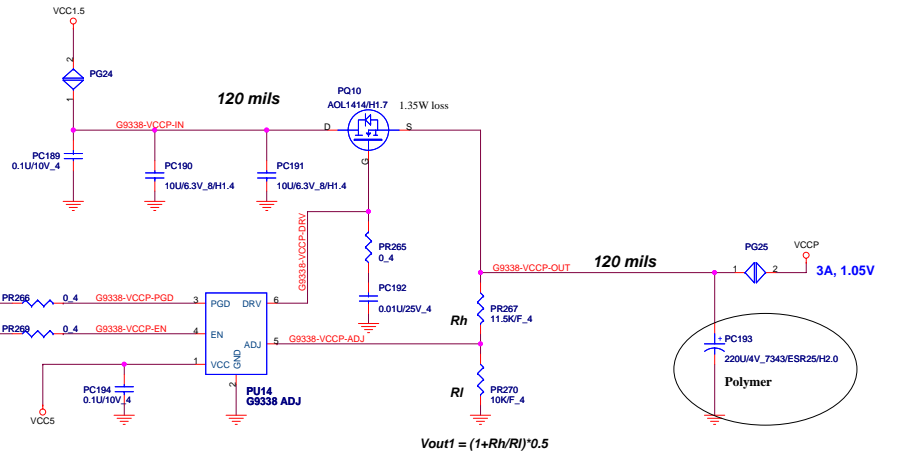
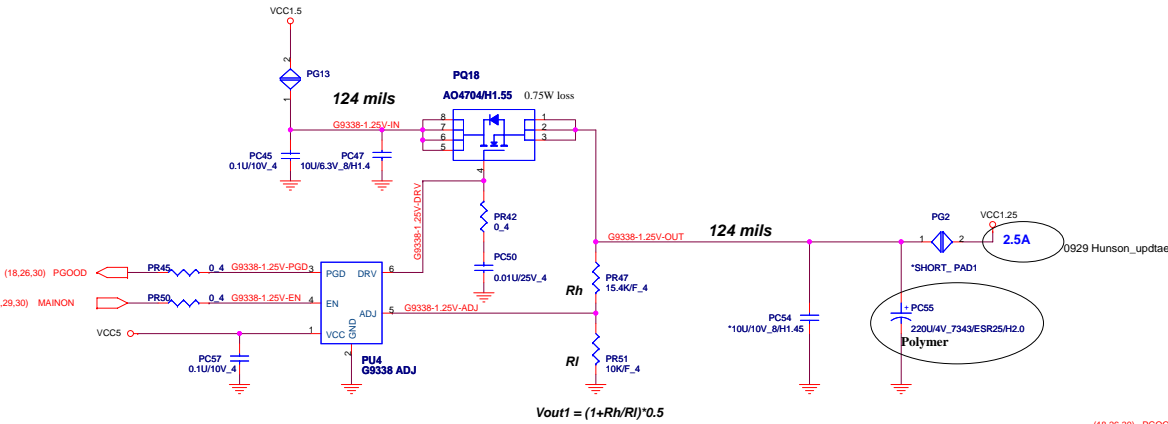
QUANTA COMPUTER

Title: **VCCP & VCC1.5 & VCC1.25**

Size: Document Number **RD3 Main Board** Rev **1A**

Date: Tuesday, November 14, 2006 Sheet **26** of **35**

1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

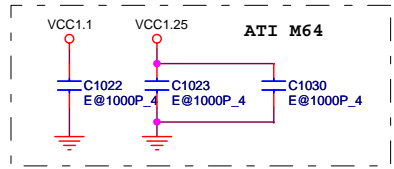
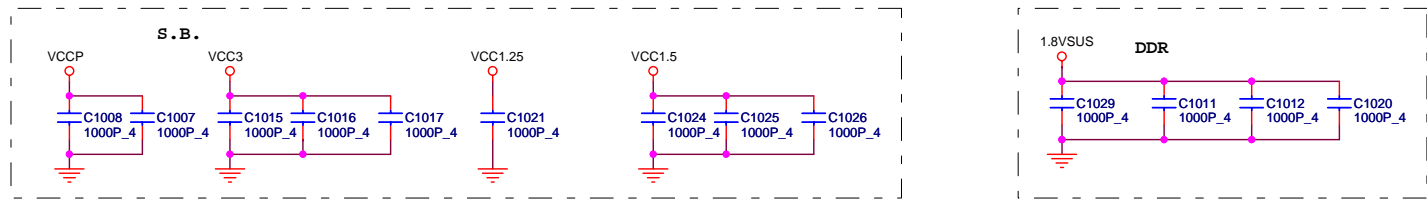
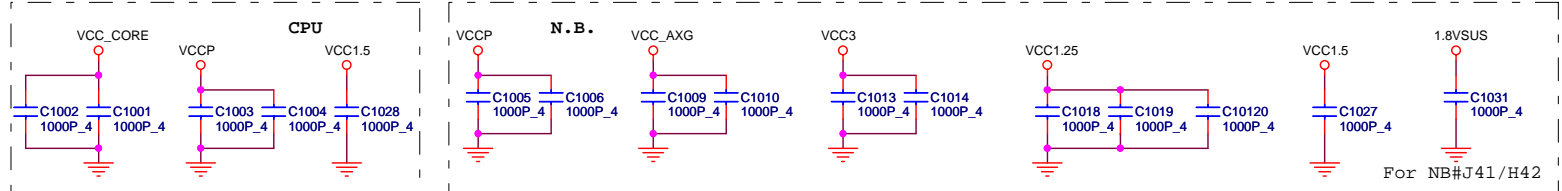
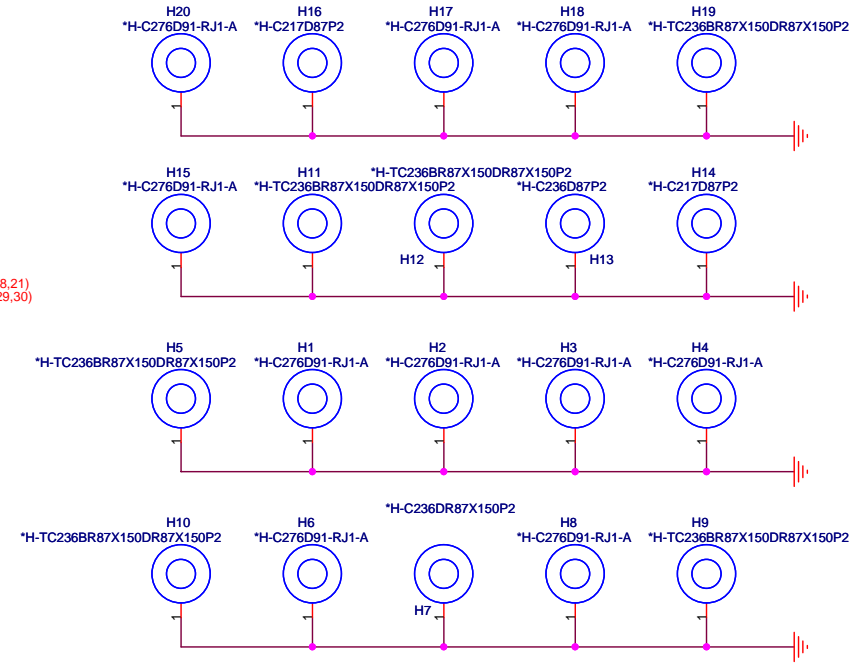
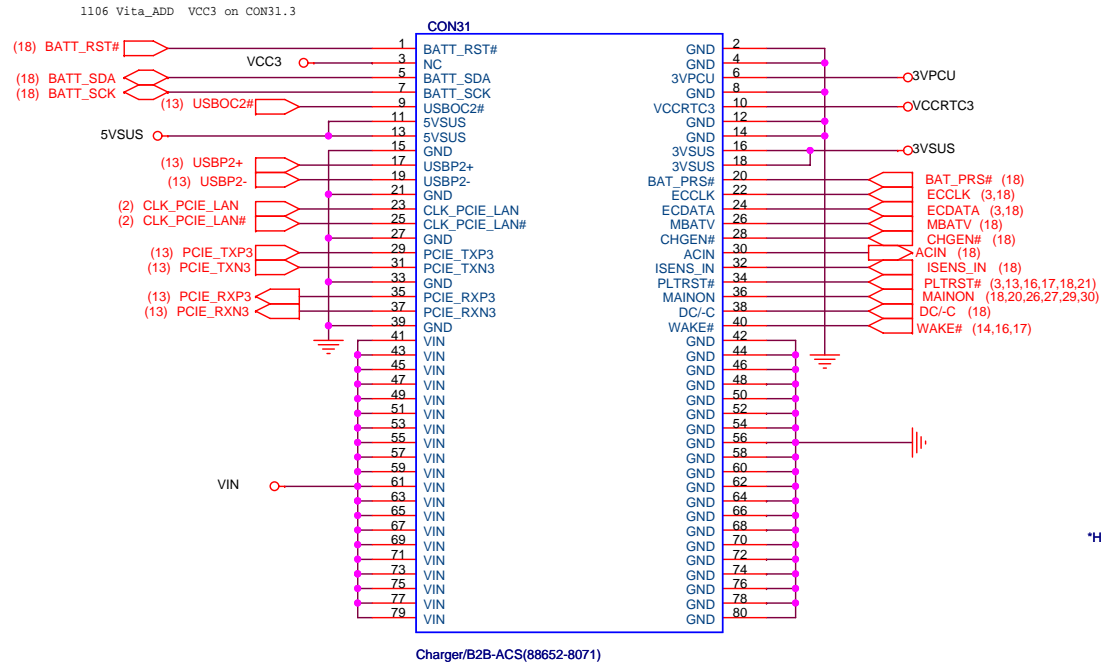


In progress

QUANTA COMPUTER		
Title: VCCP & VCC1.5 & VCC1.25		
Size:	Document Number:	Rev:
	RD3 Main Board	1A
Date:	Tuesday, November 14, 2006	Sheet: 27 of 35

1. Level 1 Environment-related Substances Should NEVER be Used.
2. Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

1027 Vita modify pin definition



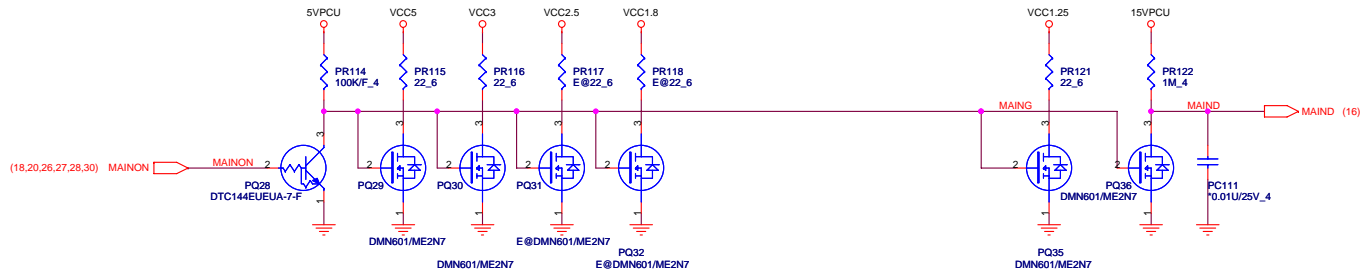
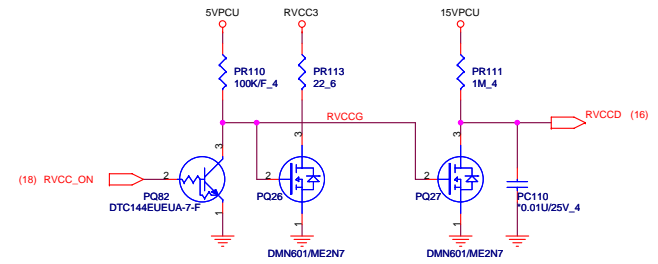
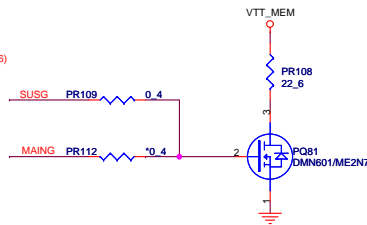
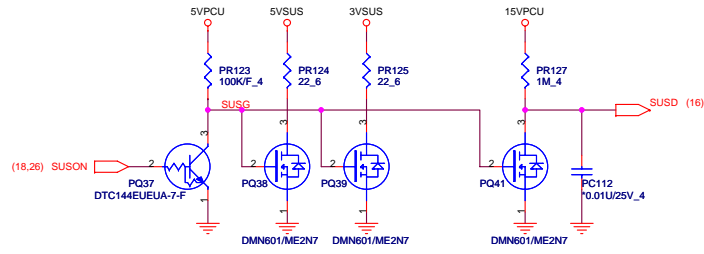
1.Level 1 Environment-related Substances Should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

QUANTA
COMPUTER

Title
Power Charger & LAN CON

Size B Document Number
GD1 Main Board Rev 1A

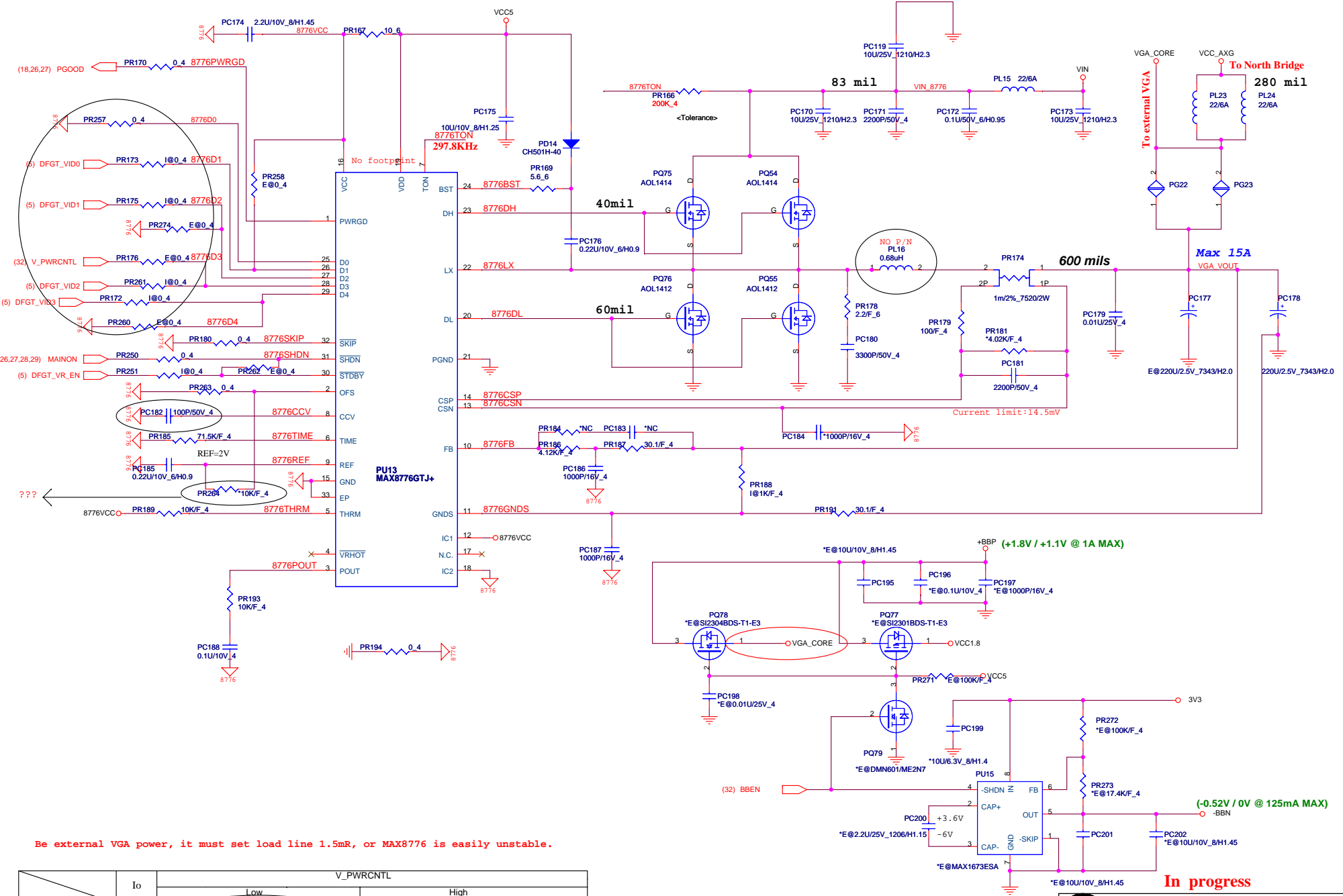
Date: Wednesday, November 15, 2006 Sheet 28 of 35



1. Level 1 Environment-related Substances Should NEVER be Used.
 2. Purchase Ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

In progress

QUANTA COMPUTER	
Title: 3VPCU & 5VPCU	
Size: Custom	Document Number: RD3 Main Board
Date: Wednesday, November 15, 2006	Rev: 1A
Sheet: 29	of 35



Be external VGA power, it must set load line 1.5mR, or MAX8776 is easily unstable.

	Io	V_PWRCTRL	
		Low	High
Ext :ATI M71-M74	15A	1.2V (D4,D3,D2,D1,D0=0,0,1,0)	1.0V (D4,D3,D2,D1,D0=0,1,0,1,0)
Int :North Bridge	7.7A	VID	

1.Level 1 Environment-related Substances should NEVER be Used.
2.Purchase ink, paint, wire rods, and Molding resins only from the business Partners that Sony approves as Green Partners.

In progress

QUANTA COMPUTER

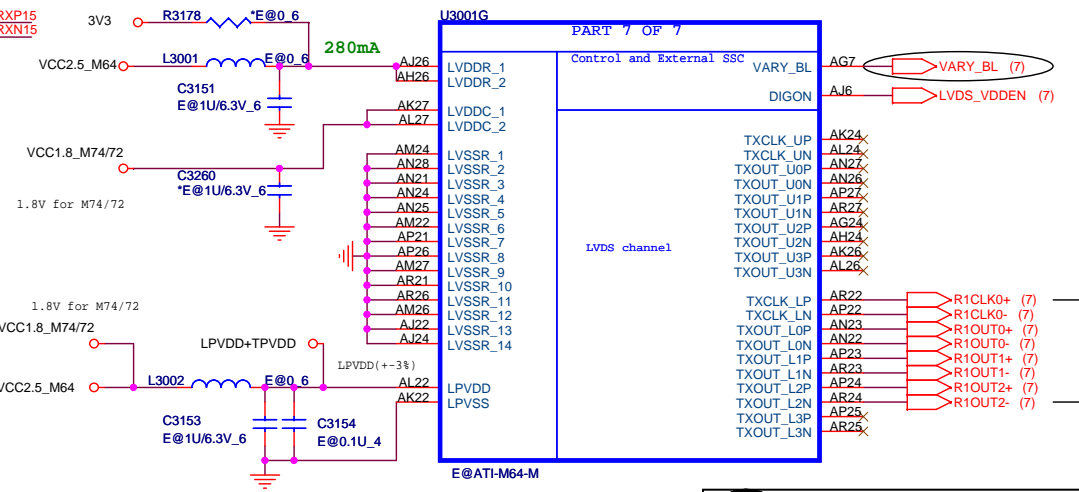
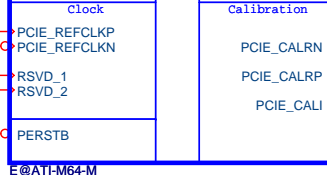
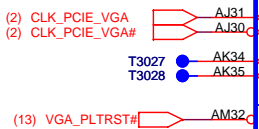
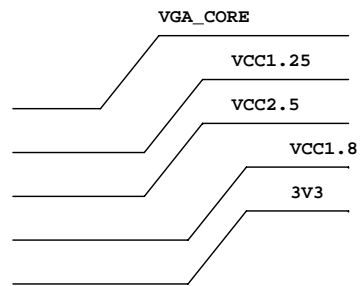
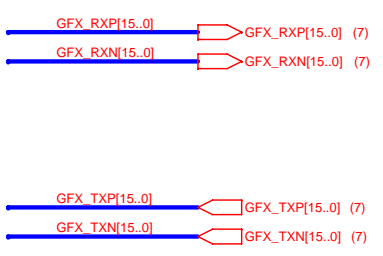
Title: **VGA CORE**

Size	Document Number	Rev
	RD3 Main Board	1A

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U3001A PART 1 OF 7

GFX_TXP0	AK33	PCIE_RX0P	PCIE_TX0P	AG31	C GFX_RXP0	C3000	E@0.1U_4	GFX_RXP0	E@0.1U_4	GFX_RXN0
GFX_TXN0	AJ33	PCIE_RX0N	PCIE_TX0N	AG30	C GFX_RXN0	C3001	E@0.1U_4	GFX_RXN0	E@0.1U_4	GFX_RXN0
GFX_TXP1	AJ35	PCIE_RX1P	PCIE_TX1P	AF31	C GFX_RXP1	C3002	E@0.1U_4	GFX_RXP1	E@0.1U_4	GFX_RXN1
GFX_TXN1	AJ34	PCIE_RX1N	PCIE_TX1N	AF30	C GFX_RXN1	C3003	E@0.1U_4	GFX_RXN1	E@0.1U_4	GFX_RXN1
GFX_TXP2	AH35	PCIE_RX2P	PCIE_TX2P	AF28	C GFX_RXP2	C3004	E@0.1U_4	GFX_RXP2	E@0.1U_4	GFX_RXN2
GFX_TXN2	AH34	PCIE_RX2N	PCIE_TX2N	AF27	C GFX_RXN2	C3005	E@0.1U_4	GFX_RXN2	E@0.1U_4	GFX_RXN2
GFX_TXP3	AG35	PCIE_RX3P	PCIE_TX3P	AD31	C GFX_RXP3	C3006	E@0.1U_4	GFX_RXP3	E@0.1U_4	GFX_RXN3
GFX_TXN3	AG34	PCIE_RX3N	PCIE_TX3N	AD30	C GFX_RXN3	C3007	E@0.1U_4	GFX_RXN3	E@0.1U_4	GFX_RXN3
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GFX_TXN5	AE34	PCIE_RX5N	PCIE_TX5N	AB30	C GFX_RXN5	C3011	E@0.1U_4	GFX_RXN5	E@0.1U_4	GFX_RXN5
GFX_TXP6	AD35	PCIE_RX6P	PCIE_TX6P	AB28	C GFX_RXP6	C3012	E@0.1U_4	GFX_RXP6	E@0.1U_4	GFX_RXN6
GFX_TXN6	AD34	PCIE_RX6N	PCIE_TX6N	AB27	C GFX_RXN6	C3013	E@0.1U_4	GFX_RXN6	E@0.1U_4	GFX_RXN6
GFX_TXP7	AC35	PCIE_RX7P	PCIE_TX7P	AA31	C GFX_RXP7	C3014	E@0.1U_4	GFX_RXP7	E@0.1U_4	GFX_RXN7
GFX_TXN7	AC34	PCIE_RX7N	PCIE_TX7N	AA30	C GFX_RXN7	C3015	E@0.1U_4	GFX_RXN7	E@0.1U_4	GFX_RXN7
GFX_TXP8	AB33	PCIE_RX8P	PCIE_TX8P	AA28	C GFX_RXP8	C3016	E@0.1U_4	GFX_RXP8	E@0.1U_4	GFX_RXN8
GFX_TXN8	AA33	PCIE_RX8N	PCIE_TX8N	AA27	C GFX_RXN8	C3017	E@0.1U_4	GFX_RXN8	E@0.1U_4	GFX_RXN8
GFX_TXP9	AA35	PCIE_RX9P	PCIE_TX9P	W31	C GFX_RXP9	C3018	E@0.1U_4	GFX_RXP9	E@0.1U_4	GFX_RXN9
GFX_TXN9	AA34	PCIE_RX9N	PCIE_TX9N	W30	C GFX_RXN9	C3019	E@0.1U_4	GFX_RXN9	E@0.1U_4	GFX_RXN9
GFX_TXP10	Y35	PCIE_RX10P	PCIE_TX10P	W28	C GFX_RXP10	C3020	E@0.1U_4	GFX_RXP10	E@0.1U_4	GFX_RXN10
GFX_TXN10	Y34	PCIE_RX10N	PCIE_TX10N	W27	C GFX_RXN10	C3021	E@0.1U_4	GFX_RXN10	E@0.1U_4	GFX_RXN10
GFX_TXP11	W35	PCIE_RX11P	PCIE_TX11P	V31	C GFX_RXP11	C3022	E@0.1U_4	GFX_RXP11	E@0.1U_4	GFX_RXN11
GFX_TXN11	W34	PCIE_RX11N	PCIE_TX11N	V30	C GFX_RXN11	C3023	E@0.1U_4	GFX_RXN11	E@0.1U_4	GFX_RXN11
GFX_TXP12	V33	PCIE_RX12P	PCIE_TX12P	V28	C GFX_RXP12	C3024	E@0.1U_4	GFX_RXP12	E@0.1U_4	GFX_RXN12
GFX_TXN12	U33	PCIE_RX12N	PCIE_TX12N	V27	C GFX_RXN12	C3025	E@0.1U_4	GFX_RXN12	E@0.1U_4	GFX_RXN12
GFX_TXP13	U35	PCIE_RX13P	PCIE_TX13P	U31	C GFX_RXP13	C3026	E@0.1U_4	GFX_RXP13	E@0.1U_4	GFX_RXN13
GFX_TXN13	U34	PCIE_RX13N	PCIE_TX13N	U30	C GFX_RXN13	C3027	E@0.1U_4	GFX_RXN13	E@0.1U_4	GFX_RXN13
GFX_TXP14	T35	PCIE_RX14P	PCIE_TX14P	U28	C GFX_RXP14	C3028	E@0.1U_4	GFX_RXP14	E@0.1U_4	GFX_RXN14
GFX_TXN14	T34	PCIE_RX14N	PCIE_TX14N	U27	C GFX_RXN14	C3029	E@0.1U_4	GFX_RXN14	E@0.1U_4	GFX_RXN14
GFX_TXP15	R35	PCIE_RX15P	PCIE_TX15P	R31	C GFX_RXP15	C3030	E@0.1U_4	GFX_RXP15	E@0.1U_4	GFX_RXN15
GFX_TXN15	R34	PCIE_RX15N	PCIE_TX15N	R30	C GFX_RXN15	C3031	E@0.1U_4	GFX_RXN15	E@0.1U_4	GFX_RXN15

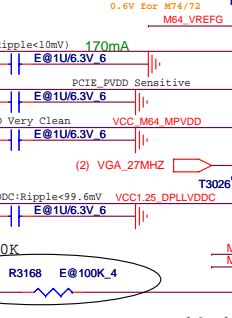
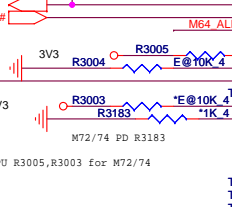
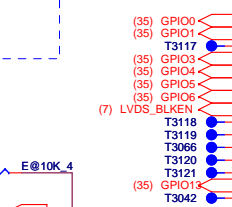
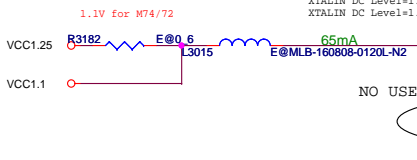
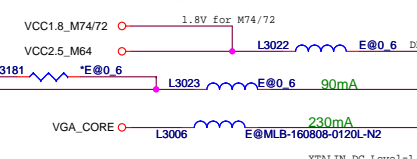
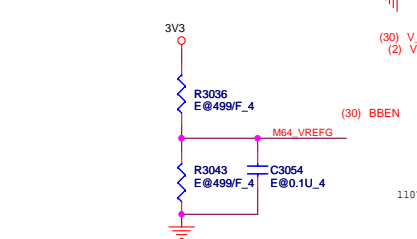
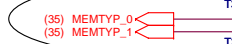
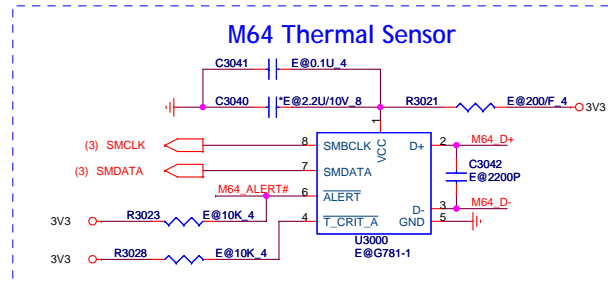


1st LVDS CH



Title			ATI M64M PCIE
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1.Level 1 Environment-related Substances Should NEVER be Used.
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VID_0	AM12
VID_1	AL12
VID_2	AJ12
VID_3	AH12
VID_4	AM10
VID_5	AL10
VID_6	AJ10
VID_7	AH10
VHAD_0	AM9
VHAD_1	AL9
VPHCTL	AJ9
VPCLK0	AL7
VPCLK	AK7
PSYNC	AM7
DVALID	AJ7
SDA	AK6
SCL	AM6
NC_1	AK14
DVPNCNTL_MVP_0	AN8
DVPNCNTL_MVP_1	AL8
DVPNCNTL_1	AH3
DVPNCNTL_2	AH2
DVPCLK	AH1
DVPDATA_0	AJ3
DVPDATA_1	AJ2
DVPDATA_2	AJ1
DVPDATA_3	AK2
DVPDATA_4	AK1
DVPDATA_5	AL3
DVPDATA_6	AL2
DVPDATA_7	AL1
DVPDATA_8	AM3
DVPDATA_9	AM2
DVPDATA_10	AM1
DVPDATA_11	AP3
DVPDATA_12	AP2
DVPDATA_13	AP1
DVPDATA_14	AR4
DVPDATA_15	AR5
DVPDATA_16	AR6
DVPDATA_17	AR7
DVPDATA_18	AP6
DVPDATA_19	AP5
DVPDATA_20	AP4
DVPDATA_21	AP7
DVPDATA_22	AP8
DVPDATA_23	AR2

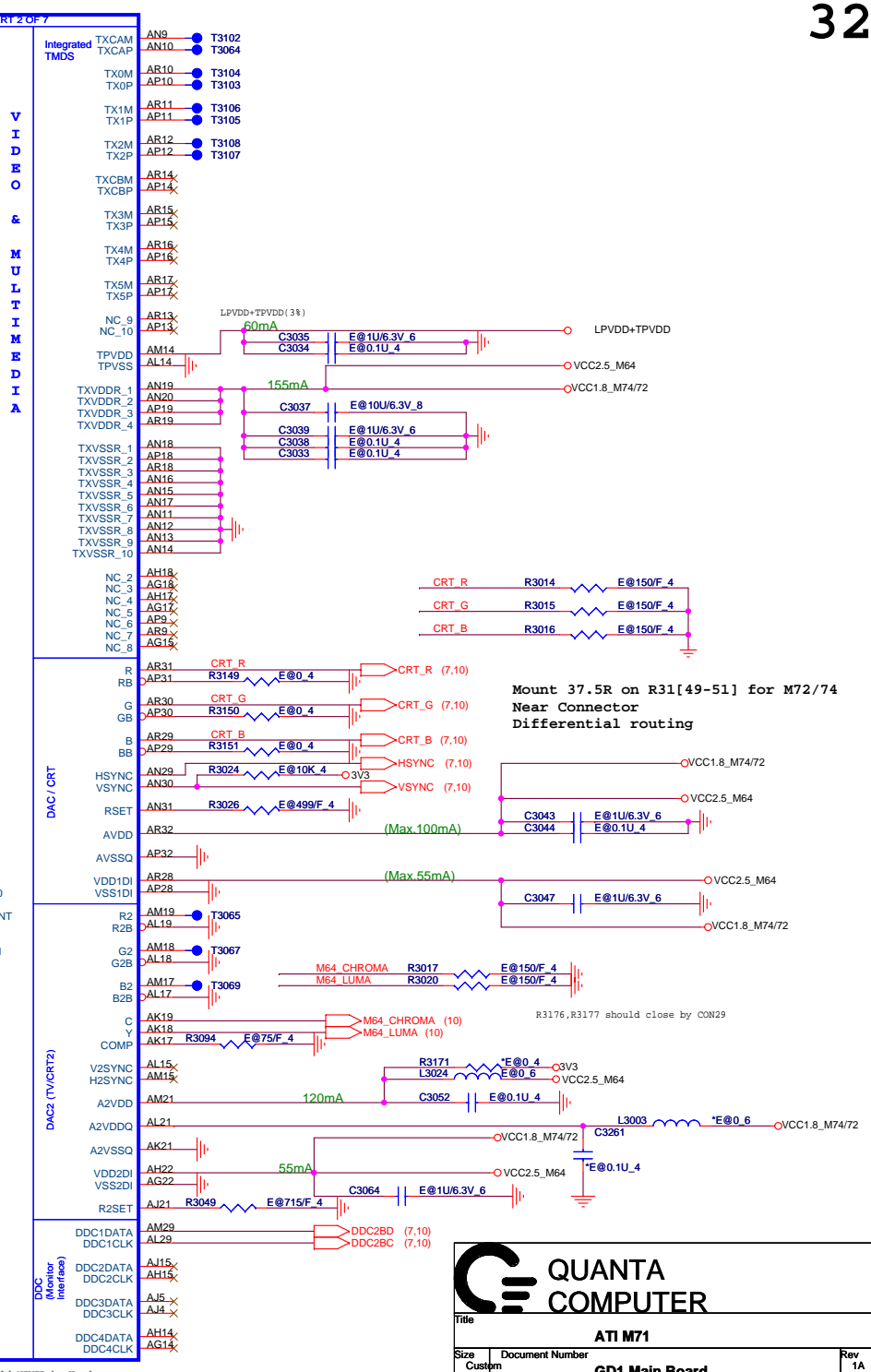
MULTI_GPIO External TMD5

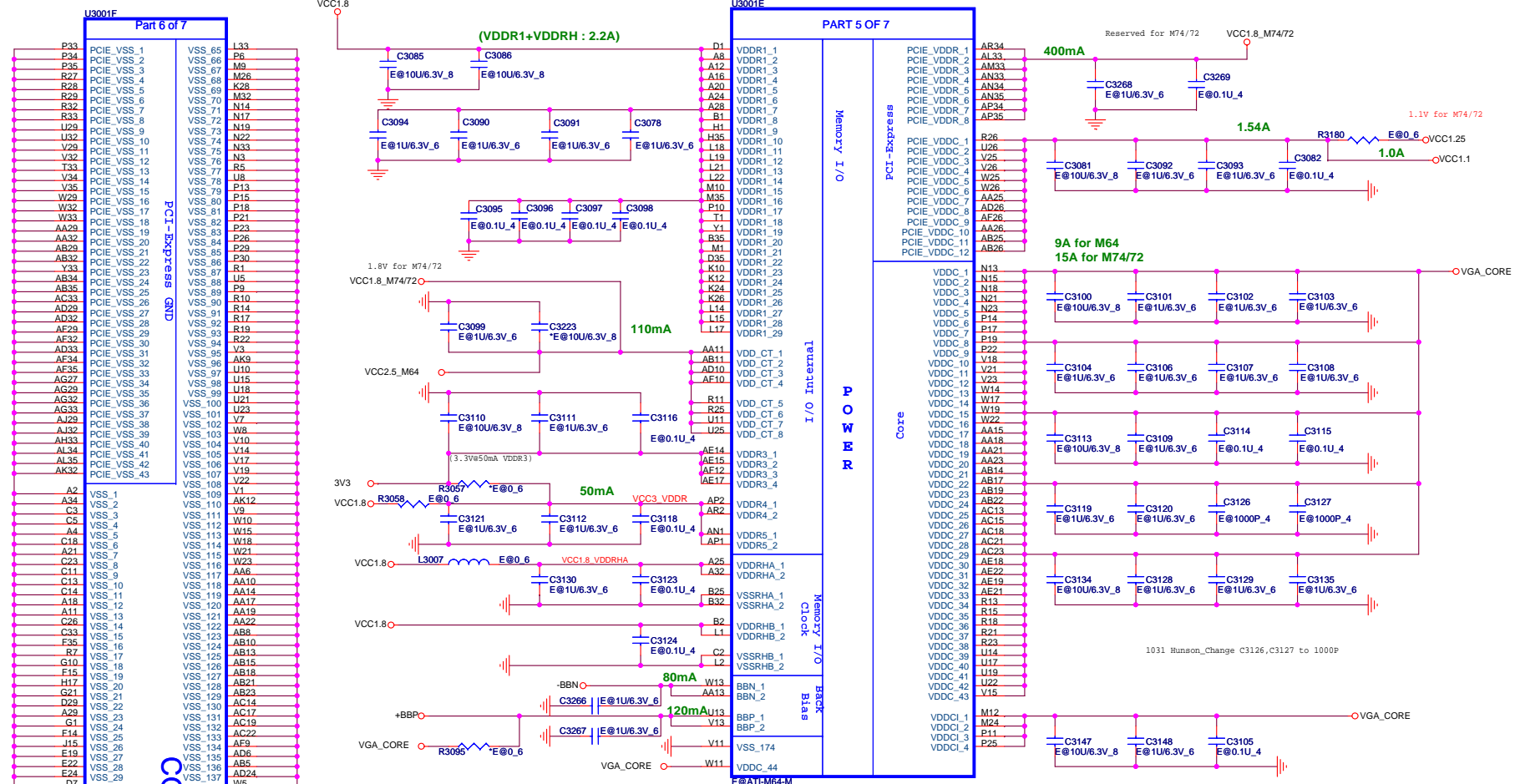
General Purpose IO

GPIO_0	AE2
GPIO_1	AE1
GPIO_2	AE3
GPIO_3	AE1
GPIO_4	AE2
GPIO_5	AD3
GPIO_6	AD2
GPIO_7_BLON	AD1
GPIO_8_ROMSO	AD5
GPIO_9_ROMSI	AD4
GPIO_10_ROMSCK	AC3
GPIO_11	AC2
GPIO_12	AC1
GPIO_13	AB3
GPIO_14_HPD2	AB2
GPIO_15_PWRCNTL_0	AB1
GPIO_16_SSN	AF5
GPIO_17_THERMAL_INT	AF4
GPIO_18_HPD3	AG4
GPIO_19_CTF	AD9
GPIO_20_PWRCNTL_1	AD8
GPIO_21_BBEN	AD7
GPIO_22_ROMCSB	AB4
GPIO_23_CLKREQB	AB4
GPIO_24_TRST	AB7
GPIO_25_TDI	AB7
GPIO_26_TOK	AB9
GPIO_27_TMS	AA9
GPIO_28_TDO	AE8
GENERICA	AE7
GENERICB	AG5
GENERICC	AG5

Thermal

DMINUS	AK4
DPLUS	AM4
AG6	AG6
HPD1	AM4





CORE GND

POWER Regulator	M64/M71	Ra11	M72/M74	Ra11
VDDC+VDDCI	1.0-1.2V	VGA_CORE	0.95-1.1V	VGA_CORE
PCIE_PVDD	1.25	VCC1.25	1.8	VCC1.8_M74/72
PCIE_VDDR	NC	x	1.8	VCC1.8_M74/72
PCIE_VDDC	1.25	VCC1.25	1.1	VCC1.1
MPVDD	VDDC	VGA_CORE	VDDC	VGA_CORE
DPLL_PVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
DPLL_VDDC	1.25	VCC1.25	1.1	VCC1.1
VDDR1+VDDRH	1.8	VCC1.8	1.8	VCC1.8
VDDR4+VDDR5	1.8	VCC1.8	1.8	VCC1.8
VDDR3	3.3	3V3	3.3	3V3
VDD_CT	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
LPVDD+FPVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
LVDDR	2.5	VCC2.5_M64	3.3	3V3_M74/72
LVVDD	NC	x	1.8	VCC1.8_M74/72
TXVDDR	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
AVDD	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
VDD1DI+VDD2DI	2.5	VCC2.5_M64	1.8	VCC1.8_M74/72
A2VDD	2.5	VCC2.5_M64	3.3	3V3_M74/72
A2VDDQ	NC	x	1.8	VCC1.8_M74/72

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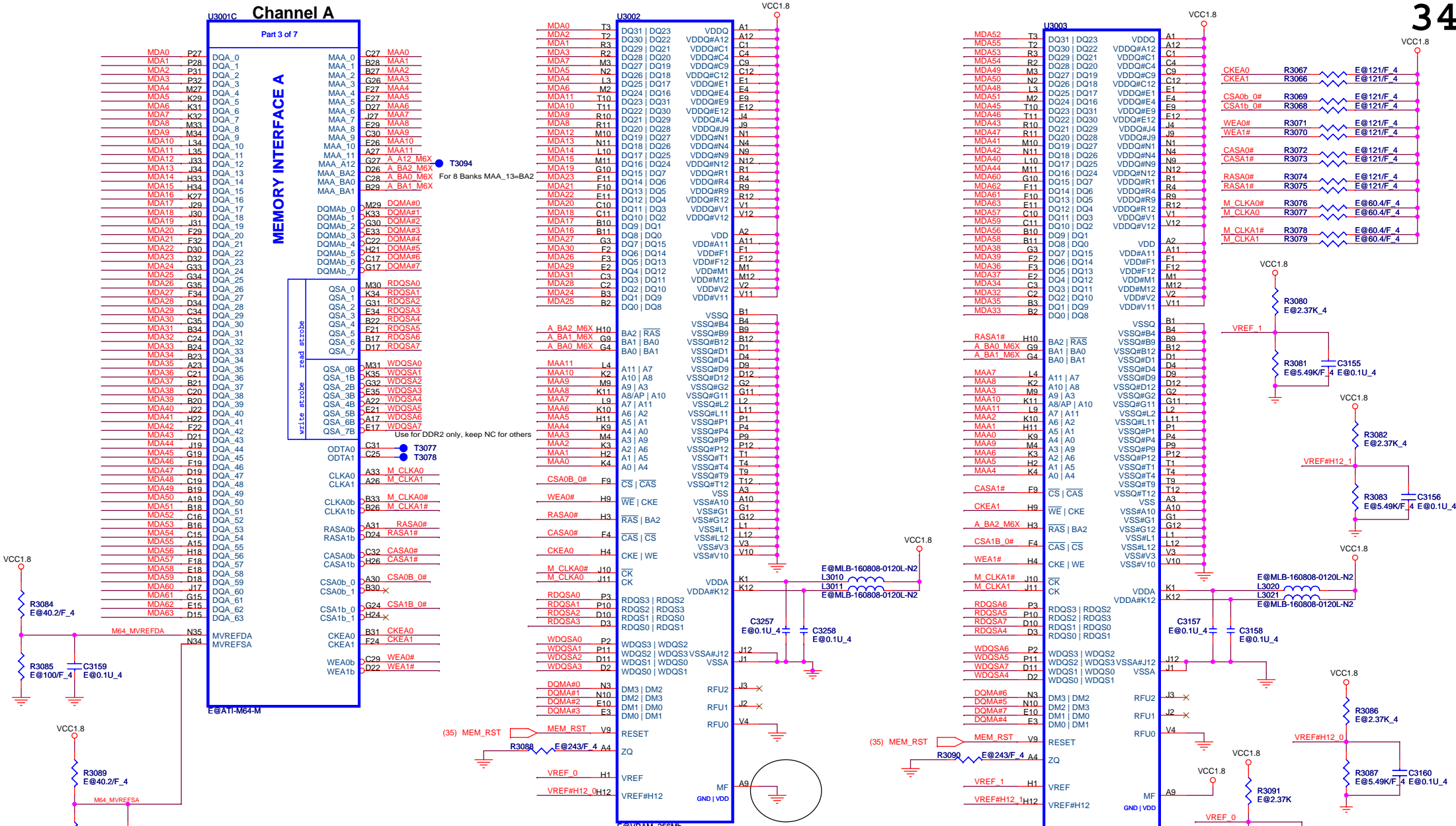
QUANTA COMPUTER

ATI M64M POWER

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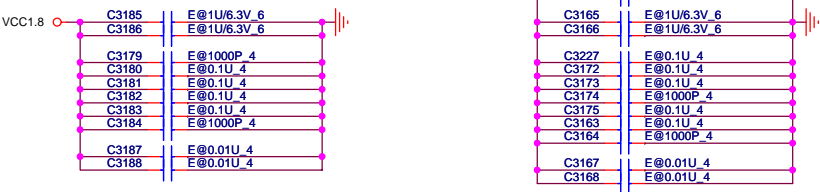
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Signal	DDR1,2	DDR3
MVREF to 1.8V	100R	40.2R
MVREF to GND	100R	100R

1031 Hunson_Change C3184,C3164,c3179,C3174 to 1000P



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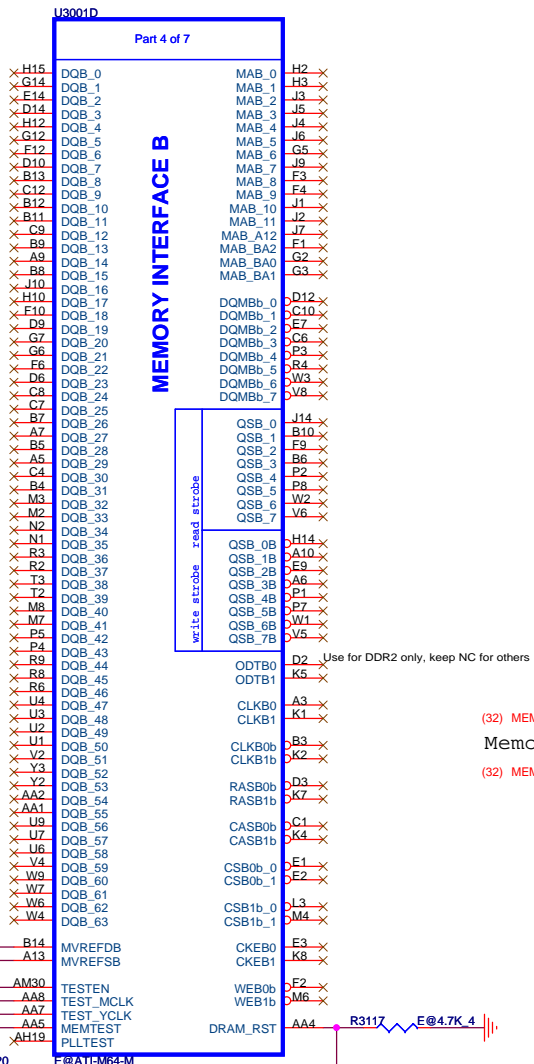
QUANTA COMPUTER

ATI M64M VRAM

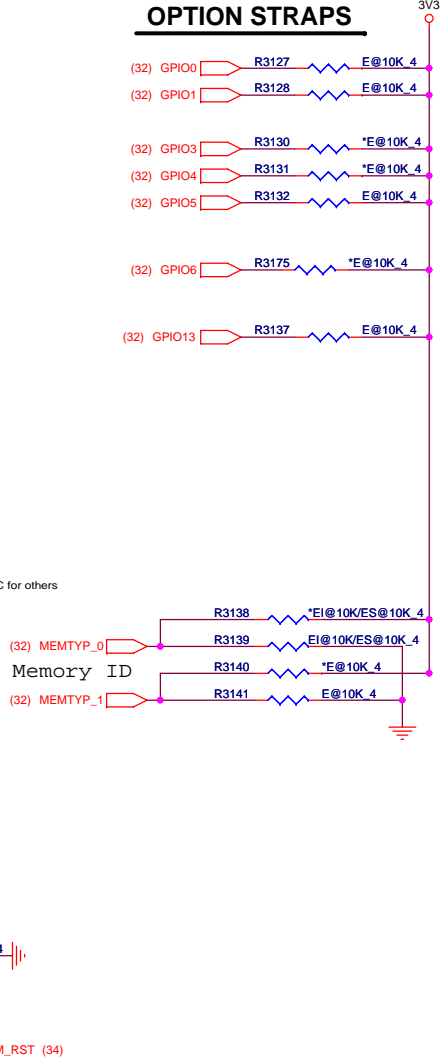
Size Custom Document Number **GD1 Main Board** Rev 1A

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Channel B



OPTION STRAPS



M64-M Strap

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Savings Enable 0: 50% Tx output swing 1: full Tx output swing	0 (internal pull-down)
TX_DEEMPH_EN	GPIO1	(recommended) Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1: Tx de-emphasis enabled (recommended)	0 (internal pull-down)
Reserved	GPIO(3:2)	ATI internal use only. Other logic must not affect this signal during RESET.(GPIO2=VDD_VCL)	00
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0 (internal pull-down)
PLL_IBIAS_RD	GPIO[6:5]	Bias Current for the PCI Express PHY PLL	01
Reserved	GPIO8	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, controls chip IDIs. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 128MB 001x - No ROM, MEM_AP_SIZE=01 256MB 010x - No ROM, MEM_AP_SIZE=10 64MB(Default) 011x - No ROM, MEM_AP_SIZE=11 Reserved 1000 - Parallel ROM, chip IDIs from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDIs from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDIs from ROM 1011 - Serial M25P10 ROM (ST), chip IDIs from ROM 1100 - Serial M25P05 ROM (ST), chip IDIs from ROM 1100 - Serial NX25F011B ROM (ISSI), chip IDIs from ROM	GPIO[9,13,12,11] 0000 (internal pull-down)
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port device present. 1-No slave VIP port devices reporting presence during reset	0 (internal pull-down)
Reserved	PCIE_TEST	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0
Reserved	HSYNC	ATI internal use only. Other logic must not affect this signal during RESET.(Serial ROM Output from ROM)	0

VRAM Straps

REV. 0.1

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE[1:0]	GPIO 27,26	Memory identification for BIOS 00 - Infineon GDDR3 : 2M x 32 bits x 4 banks(Default) 01 - SAMSUNG GDDR3 : 2M x 32 bits x 4 banks 10 - RESERVED 11 - RESERVED	00

MEMTYPE1	MEMTYPE0	R3124	R3125	R3122	R3123	
0	0	NC	10K	NC	10K	00 - Infineon GDDR3 : 2M x 32 bits x 4 banks
0	1	NC	10K	10K	NC	01 - SAMSUNG GDDR3 : 2M x 32 bits x 4 banks
1	0	10K	NC	NC	10K	10 - RESERVED
1	1	10K	NC	10K	NC	11 - RESERVED



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