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34	AUDIO(AMP & HP & SPK)	2.0	08/24				
35	AUDIO(EXTMIC)	2.0	08/24				

P. Leader	Check by	Design by

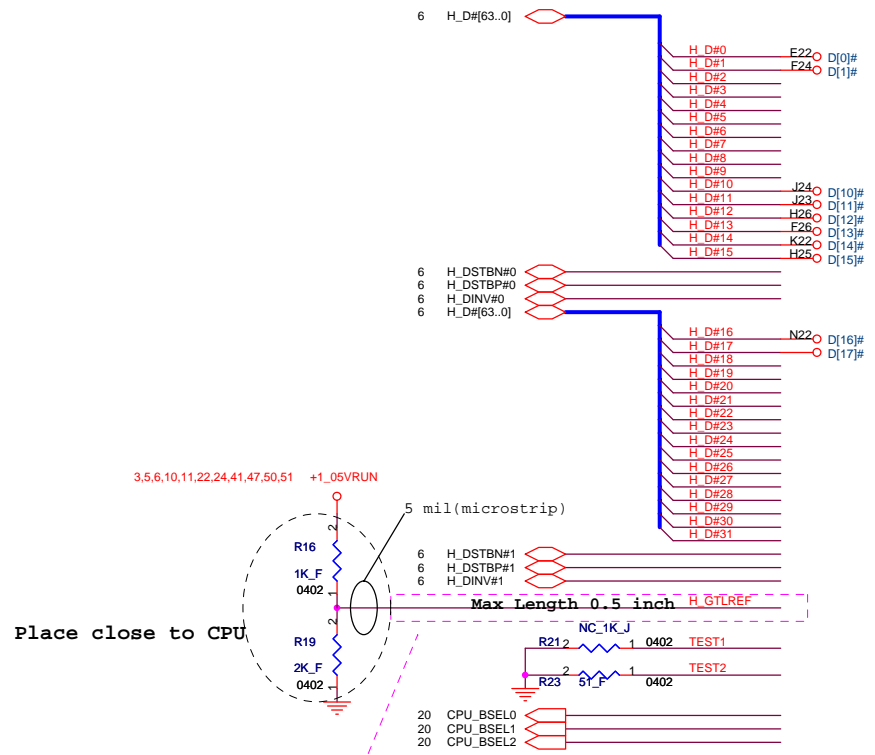
Project Code & Schematics Subject: MS70 Main Board PCB P/N: (FUBAI) 1P-0068100-6011
 (NAN YA) 1P-0068200-6011
 (HANSTAR) 1P-0068500-6011

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Title: Index Page

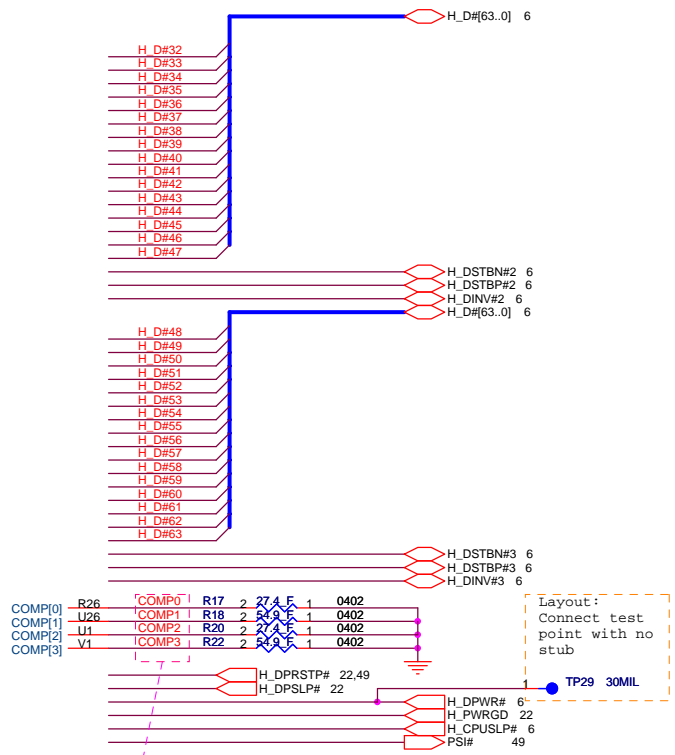
Size: A3 Document Number: MS70-1-01 Rev: 2.0

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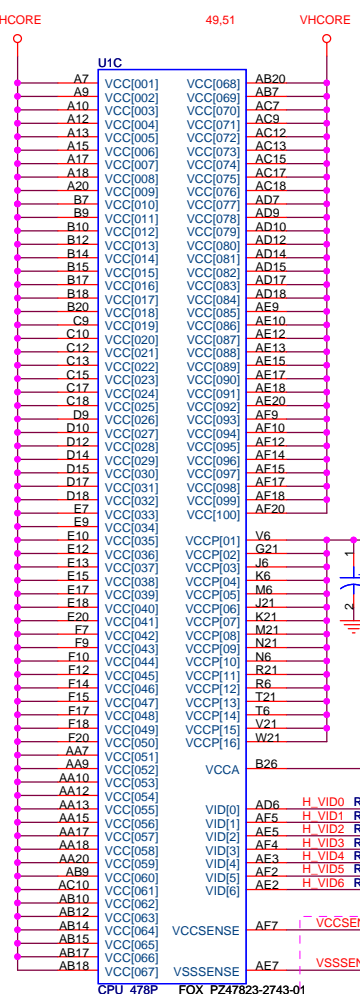
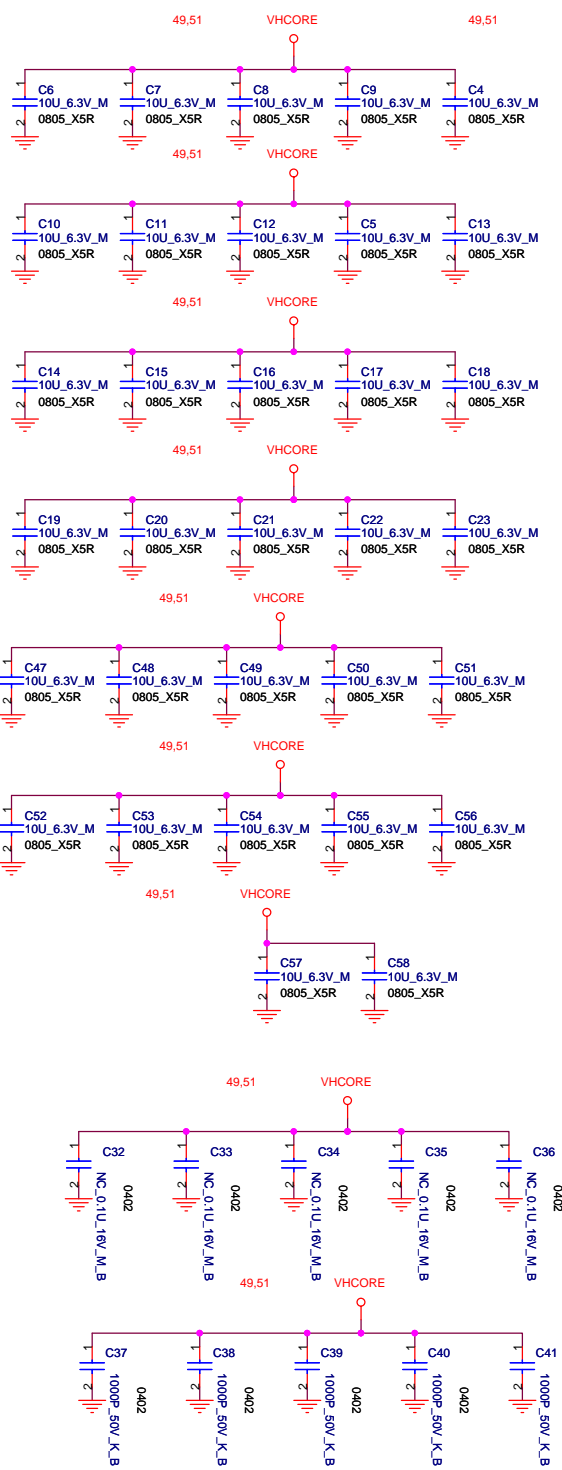
Place close to CPU

Layout Note:
 $Z_0=55$ ohm, 0.5" max for GTLREF.

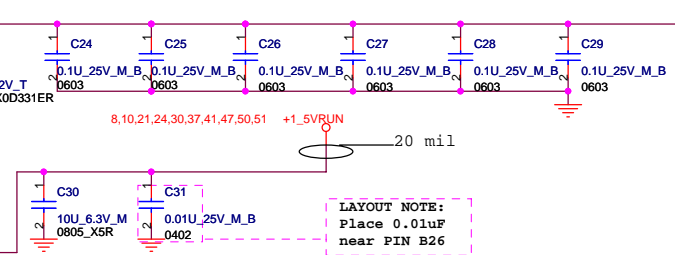


Layout Note:
 Comp0,2 connect with $Z_0=27.4$ ohm, make trace length shorter then 0.5".
 Comp1,3 connect with $Z_0=55$ ohm, make trace length shorter then 0.5".

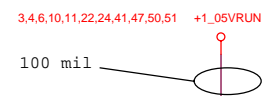
IMVP6 (max8736)
 cpu PSI# <-> max8736 PSI#
 max8736: VIHmin=0.67V
 VILmax=0.33V
 (ref. max8736 datasheet)



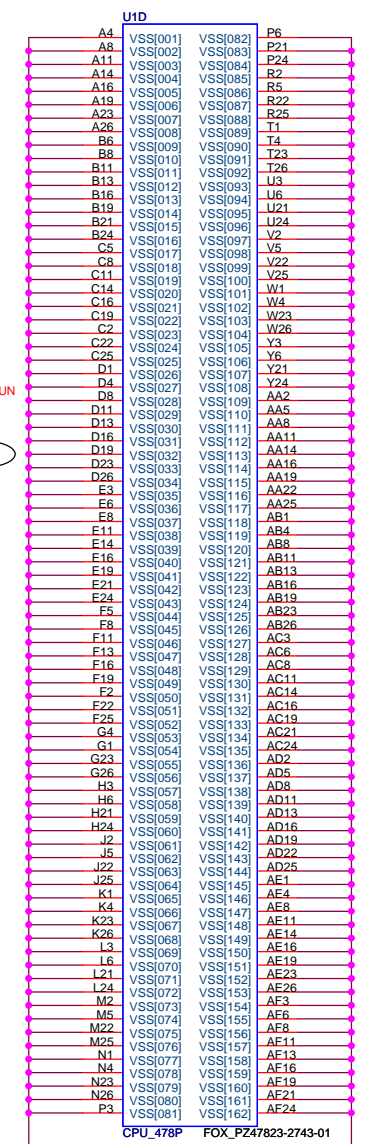
CPU_VCCA----->120mA
 CPU_VCCP----->2.5A
 CPU_VCC----->36A

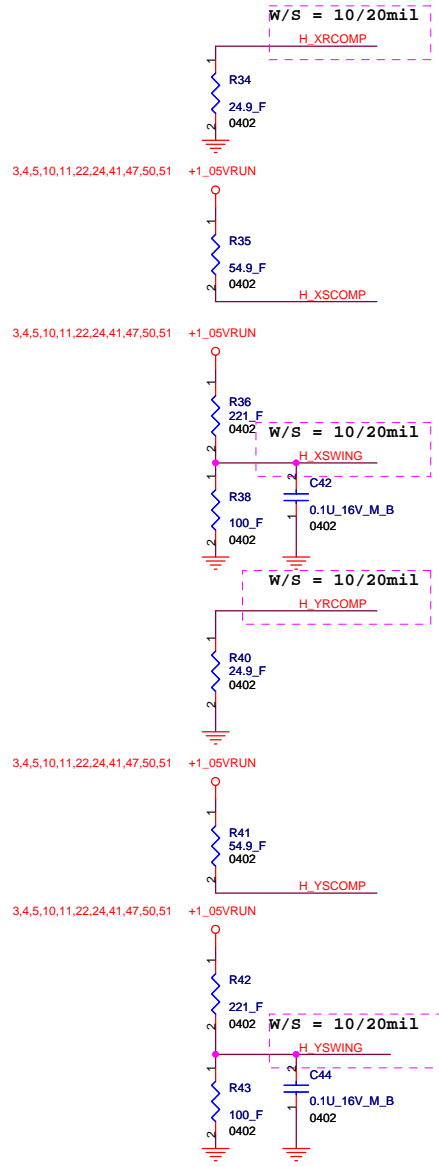


Layout Note: Route VCCSENSE traces at 27.4 Ohms with 50 mil spacing. Place PU and PD within 1 inch of cpu.
 width=18 mil
 spacing=7 mil



LAYOUT NOTE: Place 0.01uF near PIN B26

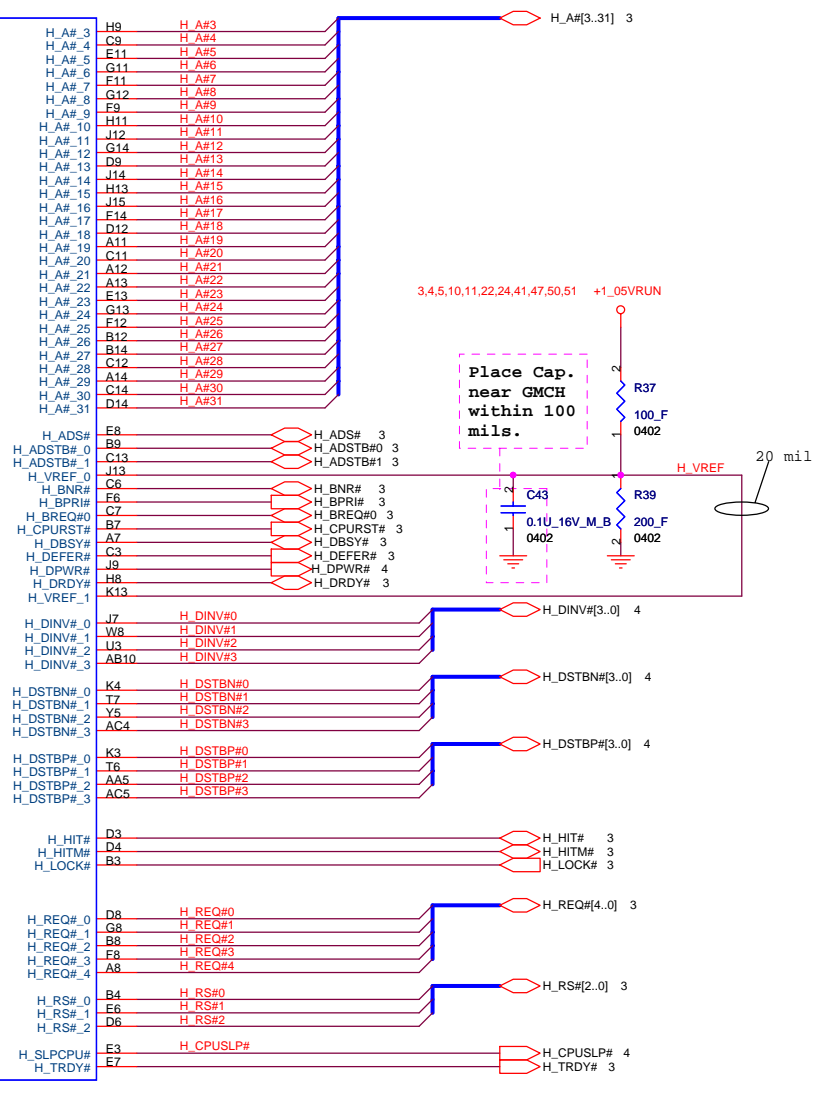




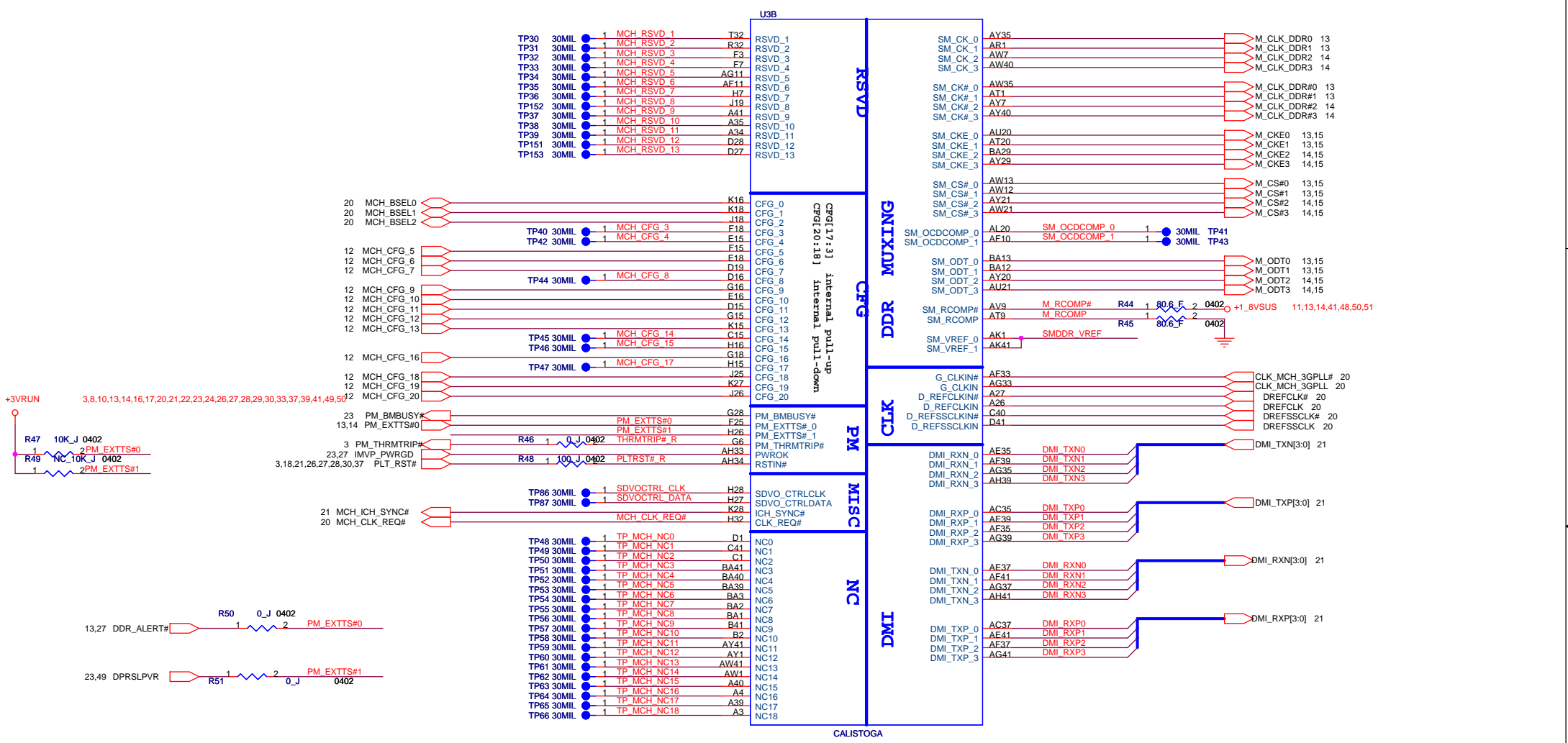
4 H_D#[63..0] \Rightarrow H_D#[63..0]

USA		CALISTOGA	
H_D#0	F1	H_XRCOMP	E1
H_D#1	J1	H_XSCOMP	E2
H_D#2	H1	H_XSWING	E4
H_D#3	J6	H_YRCOMP	Y1
H_D#4	H3	H_YSCOMP	U1
H_D#5	K2	H_YSWING	W1
H_D#6	G1	H_CLKIN	AG1
H_D#7	G2	H_CLKIN#	AG2
H_D#8	K9		
H_D#9	K1		
H_D#10	K7		
H_D#11	J8		
H_D#12	H4		
H_D#13	J3		
H_D#14	K11		
H_D#15	G4		
H_D#16	T10		
H_D#17	W11		
H_D#18	T3		
H_D#19	U7		
H_D#20	U9		
H_D#21	U11		
H_D#22	T11		
H_D#23	W9		
H_D#24	T1		
H_D#25	T8		
H_D#26	T4		
H_D#27	W7		
H_D#28	U5		
H_D#29	T9		
H_D#30	W6		
H_D#31	T5		
H_D#32	AB7		
H_D#33	AA9		
H_D#34	W4		
H_D#35	W3		
H_D#36	Y3		
H_D#37	Y7		
H_D#38	W5		
H_D#39	Y10		
H_D#40	AB8		
H_D#41	W2		
H_D#42	AA4		
H_D#43	AA7		
H_D#44	AA2		
H_D#45	AA6		
H_D#46	AA10		
H_D#47	Y8		
H_D#48	AA1		
H_D#49	AB4		
H_D#50	AC9		
H_D#51	AB11		
H_D#52	AC11		
H_D#53	AB3		
H_D#54	AC2		
H_D#55	AD1		
H_D#56	AD9		
H_D#57	AC1		
H_D#58	AD7		
H_D#59	AC6		
H_D#60	AB5		
H_D#61	AD10		
H_D#62	AD4		
H_D#63	AC8		

HOST

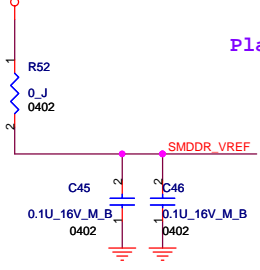


20 CLK_MCH_BCLK \Rightarrow
20 CLK_MCH_BCLK# \Rightarrow

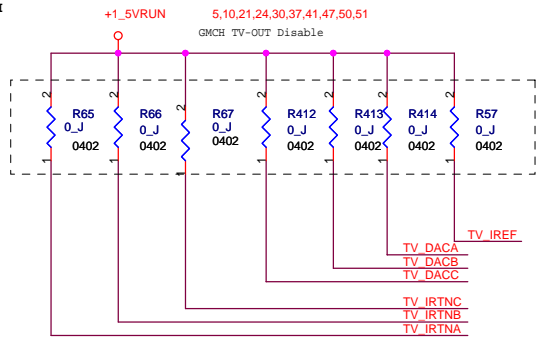
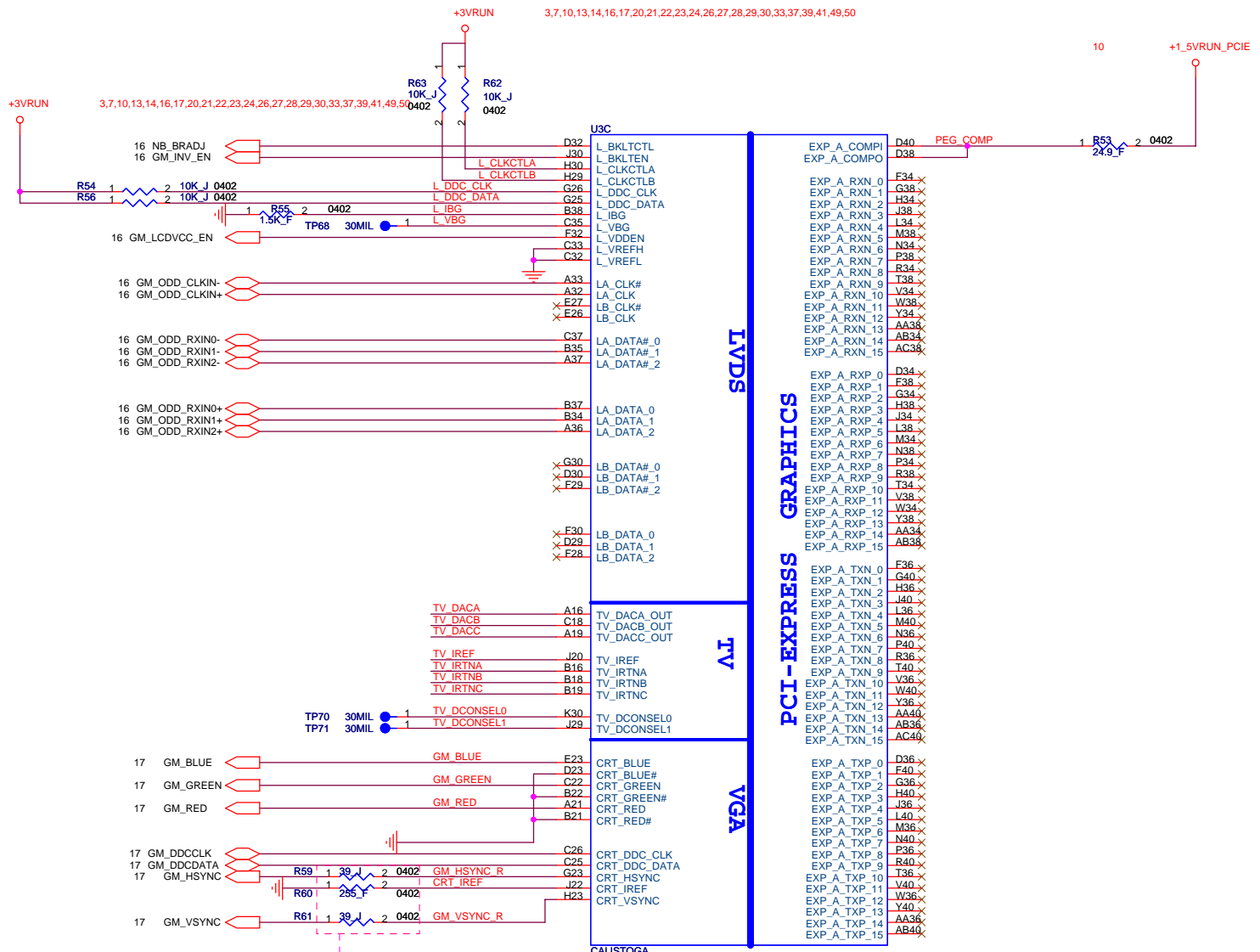


13,48

DDRDIMM_VREF

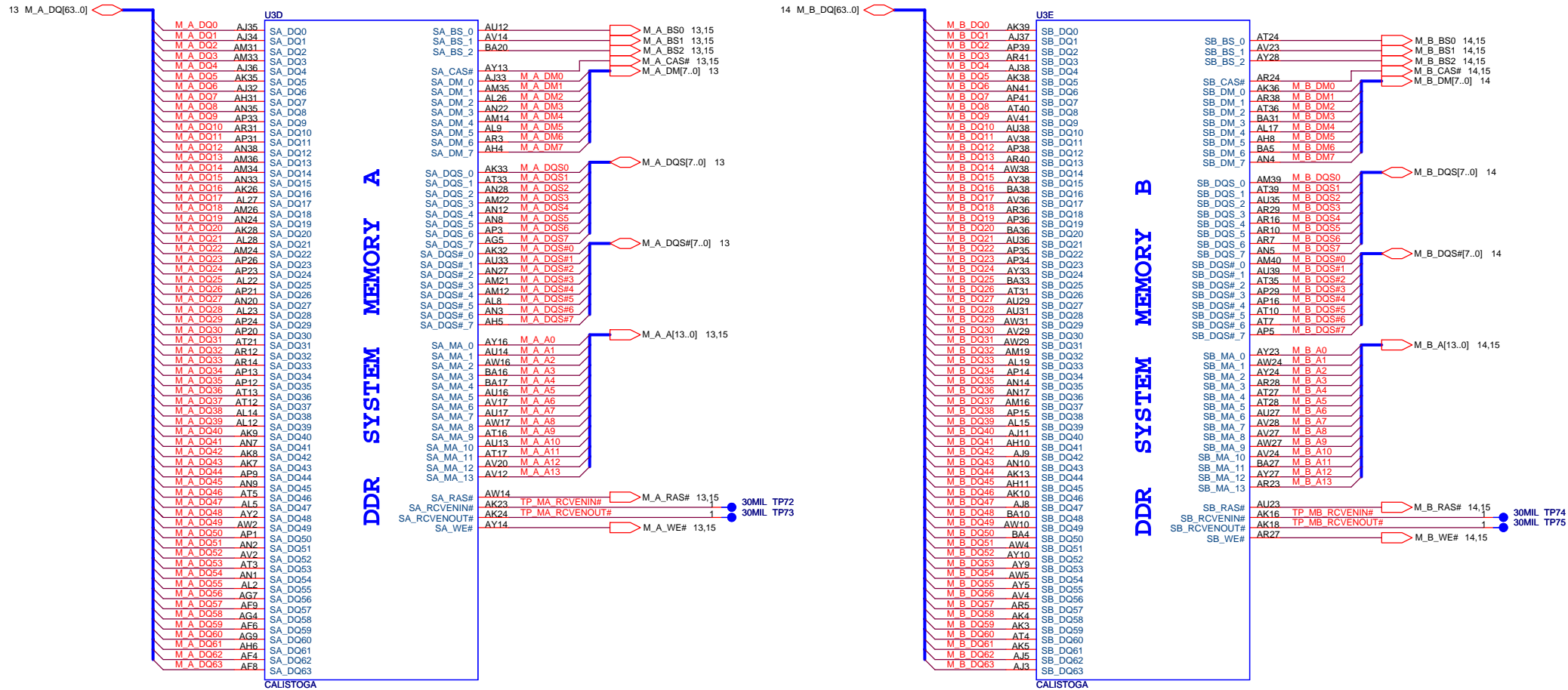


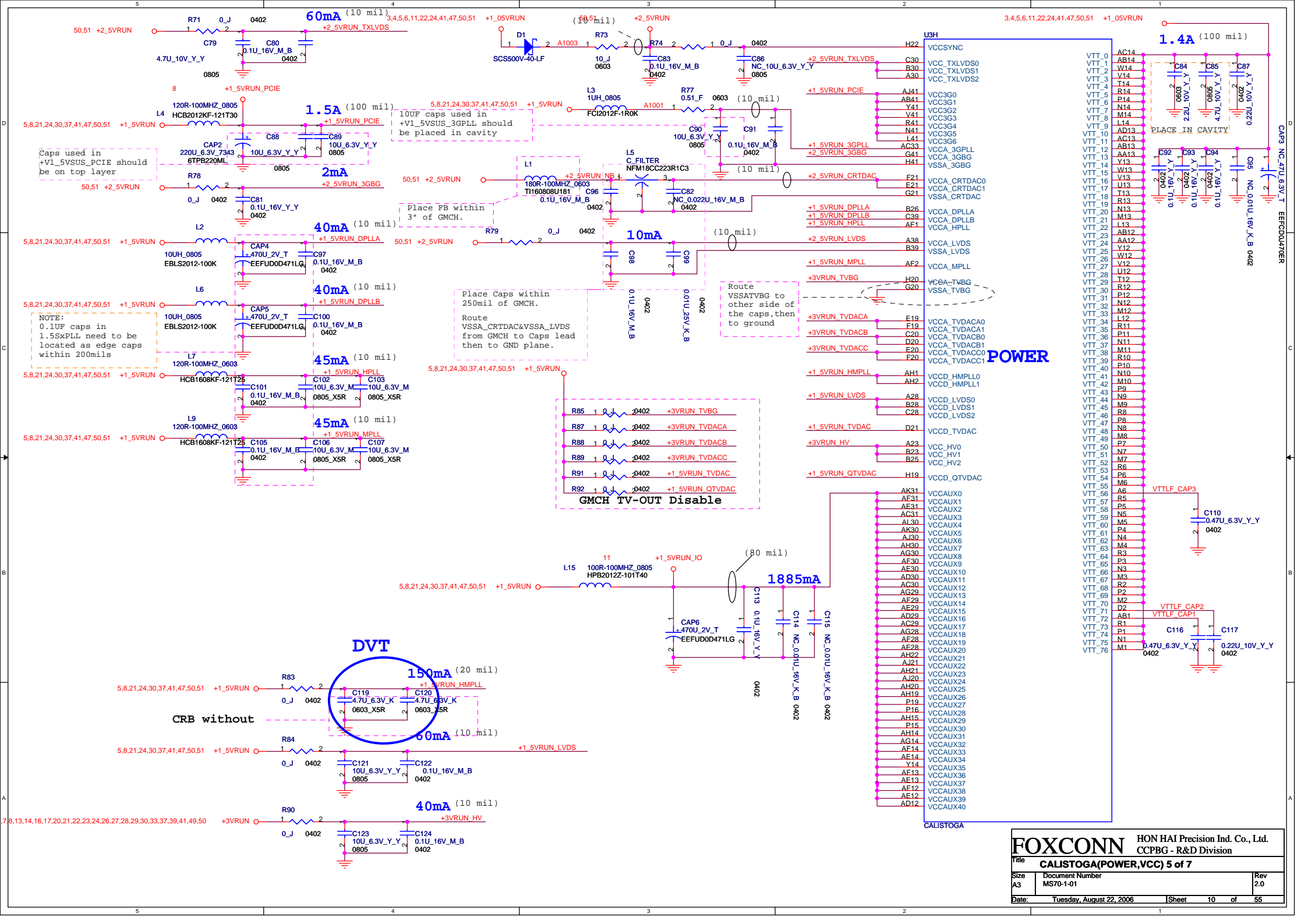
Place close to chipset

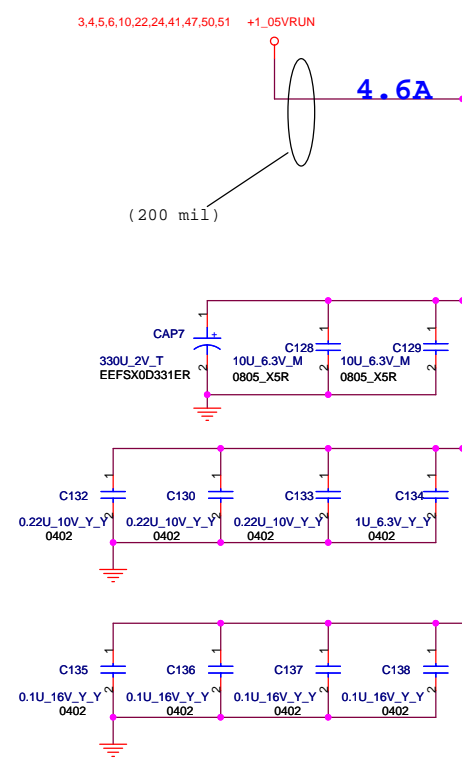


U3C Pin	Signal Name	Component
D32	L_BKLTCTL	
J30	L_BKLTEN	
H30	L_CLKCTLA	
H29	L_CLKCTLB	
G26	L_DDC_CLK	
G25	L_DDC_DATA	
B38	L_IBG	
C35	L_VBG	
F32	L_VDDEN	
C33	L_VREFH	
C32	L_VREFL	
A33	LA_CLK#	
A32	LA_CLK	
E27	LB_CLK#	
E26	LB_CLK	
C37	LA_DATA#_0	
B35	LA_DATA#_1	
A37	LA_DATA#_2	
B37	LA_DATA_0	
B34	LA_DATA_1	
A36	LA_DATA_2	
G30	LB_DATA#_0	
D30	LB_DATA#_1	
F29	LB_DATA#_2	
F30	LB_DATA_0	
D29	LB_DATA_1	
F28	LB_DATA_2	
A16	TV_DACA	
C18	TV_DACB	
A19	TV_DACC	
J20	TV_IREF	
B16	TV_IRTNA	
B18	TV_IRTNC	
B19	TV_IRTNC	
K30	TV_DCONSEL0	
J29	TV_DCONSEL1	
E23	CRT_BLUE	
D23	CRT_BLUE#	
C22	CRT_GREEN	
B22	CRT_GREEN#	
A21	CRT_RED	
B21	CRT_RED#	
C26	CRT_DDC_CLK	
C25	CRT_DDC_DATA	
G23	CRT_HSYNC	
J22	CRT_IREF	
H23	CRT_VSYNC	

PCI-EXPRESS GRAPHICS

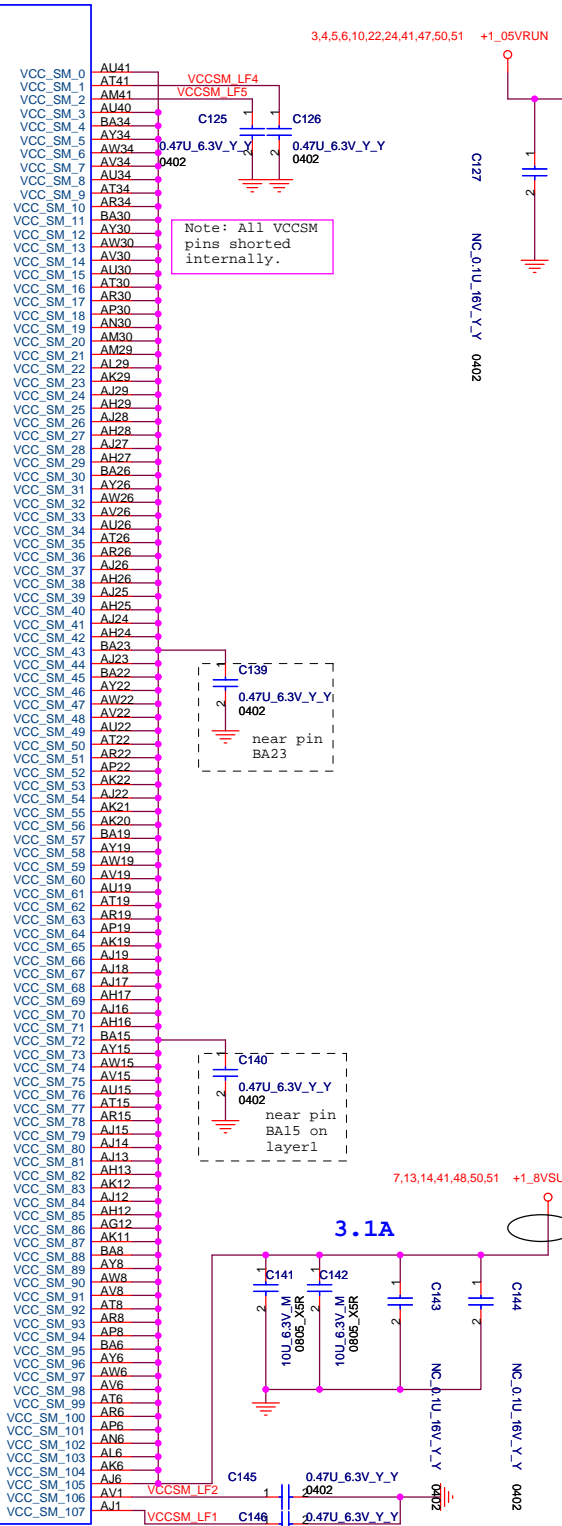






Pin	Label
VCC_0	AA33
VCC_1	W33
VCC_2	P33
VCC_3	L33
VCC_4	J33
VCC_5	AA32
VCC_6	Y32
VCC_7	W32
VCC_8	V32
VCC_9	P32
VCC_10	N32
VCC_11	M32
VCC_12	L32
VCC_13	J32
VCC_14	AA31
VCC_15	W31
VCC_16	V31
VCC_17	T31
VCC_18	R31
VCC_19	P31
VCC_20	N31
VCC_21	M31
VCC_22	AA30
VCC_23	W30
VCC_24	V30
VCC_25	W30
VCC_26	V30
VCC_27	U30
VCC_28	T30
VCC_29	R30
VCC_30	P30
VCC_31	N30
VCC_32	M30
VCC_33	L30
VCC_34	AA29
VCC_35	W29
VCC_36	V29
VCC_37	U29
VCC_38	R29
VCC_39	P29
VCC_40	M29
VCC_41	L29
VCC_42	AA28
VCC_43	W28
VCC_44	V28
VCC_45	Y28
VCC_46	U28
VCC_47	T28
VCC_48	R28
VCC_49	P28
VCC_50	N28
VCC_51	M28
VCC_52	L28
VCC_53	P27
VCC_54	N27
VCC_55	M27
VCC_56	L27
VCC_57	P26
VCC_58	N26
VCC_59	L26
VCC_60	N25
VCC_61	M25
VCC_62	L25
VCC_63	P24
VCC_64	N24
VCC_65	M24
VCC_66	AB23
VCC_67	AA23
VCC_68	Y23
VCC_69	P23
VCC_70	N23
VCC_71	M23
VCC_72	L23
VCC_73	AC22
VCC_74	AB22
VCC_75	Y22
VCC_76	W22
VCC_77	P22
VCC_78	N22
VCC_79	M22
VCC_80	L22
VCC_81	AC21
VCC_82	AA21
VCC_83	W21
VCC_84	N21
VCC_85	M21
VCC_86	L21
VCC_87	AC20
VCC_88	AB20
VCC_89	Y20
VCC_90	W20
VCC_91	P20
VCC_92	N20
VCC_93	M20
VCC_94	L20
VCC_95	AB19
VCC_96	AA19
VCC_97	Y19
VCC_98	N19
VCC_99	M19
VCC_100	L19
VCC_101	N18
VCC_102	M18
VCC_103	L18
VCC_104	P17
VCC_105	N17
VCC_106	M17
VCC_107	N16
VCC_108	M16
VCC_109	L16
VCC_110	L16

VCC

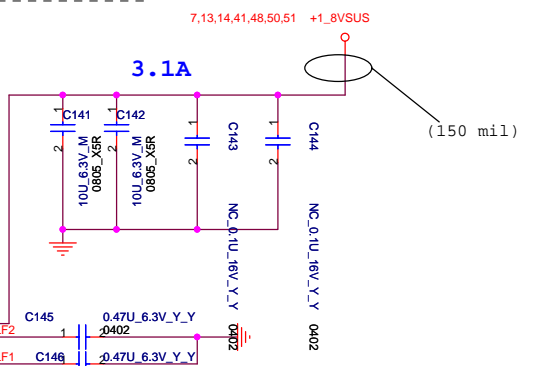


Note: All VCCSM pins shorted internally.

Pin	Label
VCC_SM_0	AU41
VCC_SM_1	AT41
VCC_SM_2	AM41
VCC_SM_3	AU40
VCC_SM_4	BA34
VCC_SM_5	AV34
VCC_SM_6	AV34
VCC_SM_7	AU34
VCC_SM_8	AT34
VCC_SM_9	AR34
VCC_SM_10	BA30
VCC_SM_11	AV30
VCC_SM_12	AW30
VCC_SM_13	AV30
VCC_SM_14	AV30
VCC_SM_15	AU30
VCC_SM_16	AT30
VCC_SM_17	AP30
VCC_SM_18	AN30
VCC_SM_19	AM30
VCC_SM_20	AM29
VCC_SM_21	AL29
VCC_SM_22	AK29
VCC_SM_23	AJ29
VCC_SM_24	AH29
VCC_SM_25	AJ28
VCC_SM_26	AH28
VCC_SM_27	AJ27
VCC_SM_28	AH27
VCC_SM_29	BA26
VCC_SM_30	AV26
VCC_SM_31	AV26
VCC_SM_32	AV26
VCC_SM_33	AV26
VCC_SM_34	AJ26
VCC_SM_35	AT26
VCC_SM_36	AR26
VCC_SM_37	AJ26
VCC_SM_38	AH26
VCC_SM_39	AJ25
VCC_SM_40	AH25
VCC_SM_41	AJ24
VCC_SM_42	AH24
VCC_SM_43	BA23
VCC_SM_44	BA22
VCC_SM_45	AY22
VCC_SM_46	AV22
VCC_SM_47	AV22
VCC_SM_48	AV22
VCC_SM_49	AU22
VCC_SM_50	AT22
VCC_SM_51	AP22
VCC_SM_52	AK22
VCC_SM_53	AJ22
VCC_SM_54	AJ21
VCC_SM_55	AK21
VCC_SM_56	BA19
VCC_SM_57	AV19
VCC_SM_58	AV19
VCC_SM_59	AV19
VCC_SM_60	AV19
VCC_SM_61	AU19
VCC_SM_62	AT19
VCC_SM_63	AP19
VCC_SM_64	AK19
VCC_SM_65	AJ19
VCC_SM_66	AJ18
VCC_SM_67	AJ17
VCC_SM_68	AH17
VCC_SM_69	AH16
VCC_SM_70	AH16
VCC_SM_71	BA15
VCC_SM_72	AY15
VCC_SM_73	AV15
VCC_SM_74	AV15
VCC_SM_75	AV15
VCC_SM_76	AT15
VCC_SM_77	AR15
VCC_SM_78	AJ15
VCC_SM_79	AJ15
VCC_SM_80	AJ14
VCC_SM_81	AJ13
VCC_SM_82	AK12
VCC_SM_83	AJ12
VCC_SM_84	AH12
VCC_SM_85	AG12
VCC_SM_86	AK11
VCC_SM_87	BA8
VCC_SM_88	AV8
VCC_SM_89	AV8
VCC_SM_90	AV8
VCC_SM_91	AT8
VCC_SM_92	AR8
VCC_SM_93	AP8
VCC_SM_94	AP8
VCC_SM_95	BA6
VCC_SM_96	AV6
VCC_SM_97	AV6
VCC_SM_98	AT6
VCC_SM_99	AR6
VCC_SM_100	AP6
VCC_SM_101	AN6
VCC_SM_102	AL6
VCC_SM_103	AK6
VCC_SM_104	AJ6
VCC_SM_105	AV1
VCC_SM_106	AJ1

NCTF

CALISTOGA



(150 mil)

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Title: **CALISTOGA(VCC CORE) 6 of 7**

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7 MCH_CFG_5 ← 1 ● 30MIL TP76

MCH_CFG_5	Low = DMIX2 High = DMIX4
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7 MCH_CFG_6 ← 1 ● 30MIL TP77

MCH_CFG_6	Low = Moby Dick High = Calistoga DDR2 select (default high)
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7 MCH_CFG_7 ← 1 ● 30MIL TP78

MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor
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7 MCH_CFG_9 ← 1 ● 30MIL TP81

MCH_CFG_9 (PCIe Graphics Lane)	Low = Reverse Lane operation High = Normal operation
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For layout convenience

7 MCH_CFG_10 ← 1 ● 30MIL TP82

MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY
----------------------------------	-----------------------------------

7 MCH_CFG_11 ← 1 ● 30MIL TP83

MCH_CFG_11 (PSB 4x CLK ENABLE)	Low = Calistoga High = Reserved
--------------------------------	------------------------------------



7 MCH_CFG_12 ← 1 ● 30MIL TP84

7 MCH_CFG_13 ← 1 ● 30MIL TP85

MCH_CFG_[13:12] (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)
----------------------------	---

7 MCH_CFG_16 ← 1 ● 30MIL TP160

MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable
------------------------------	---

MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V
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7 MCH_CFG_18 ← 1 ● 30MIL TP79

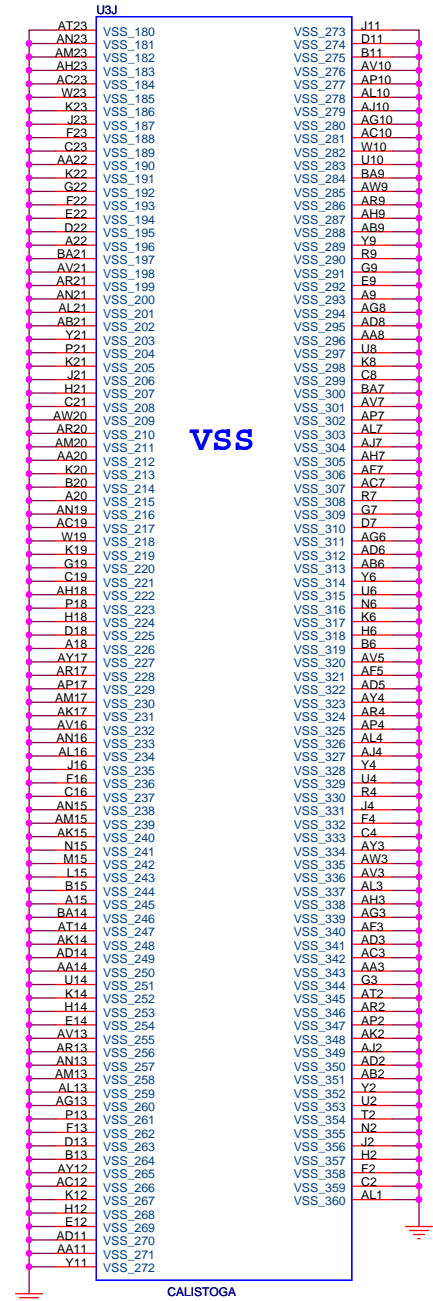
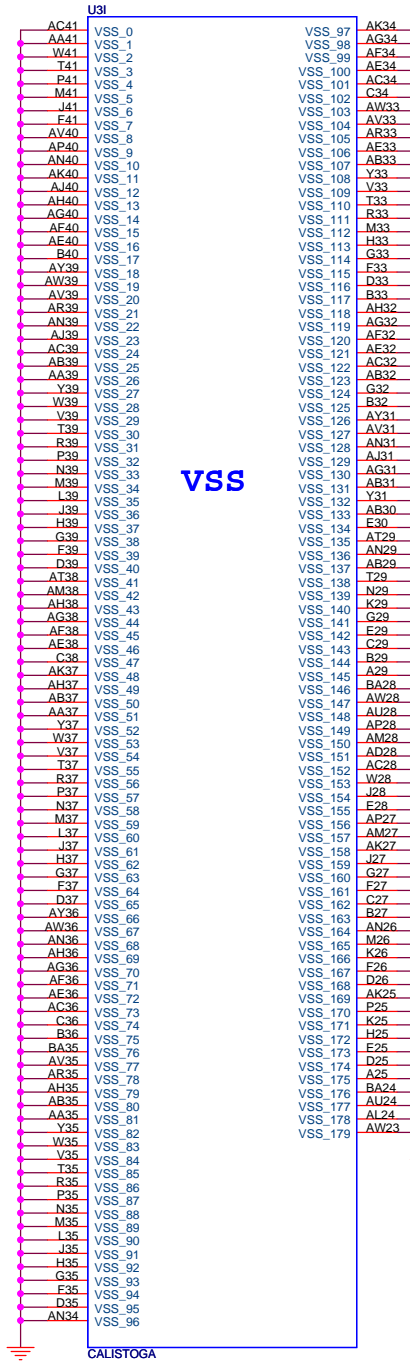
MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED
--------------------------------	--

7 MCH_CFG_19 ← 1 ● 30MIL TP80

MCH_CFG_20 (PCIe Backward Interoperability mode)	Low = Only SDVO or PCIe x1 is operational (defaults) High = SDVO and PCIe x1 are operating simultaneously via the PEG port
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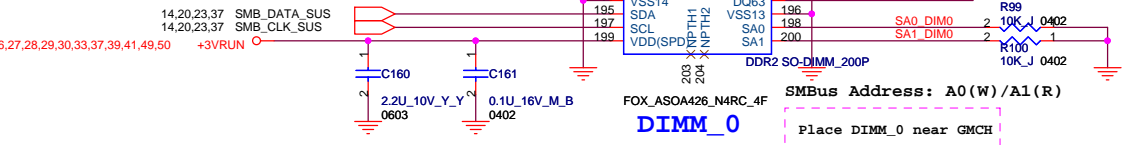
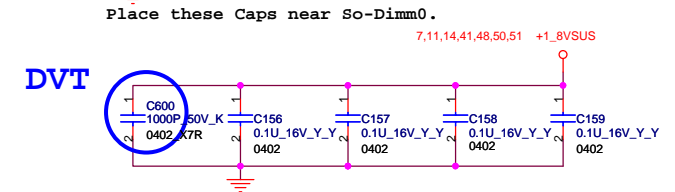
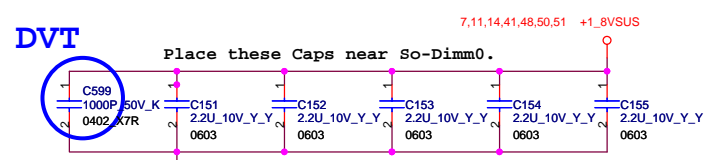
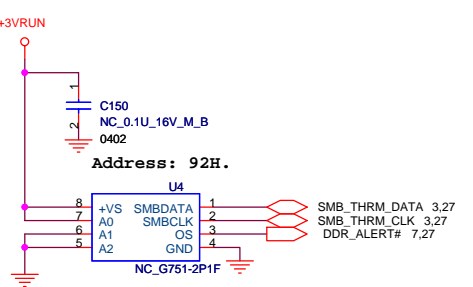
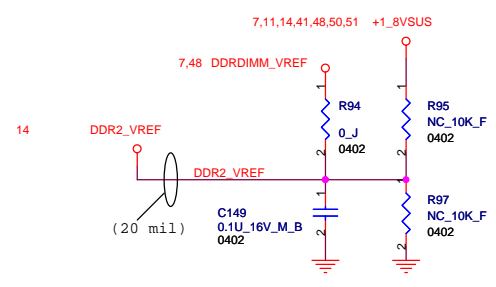
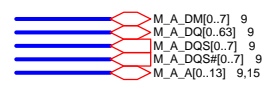
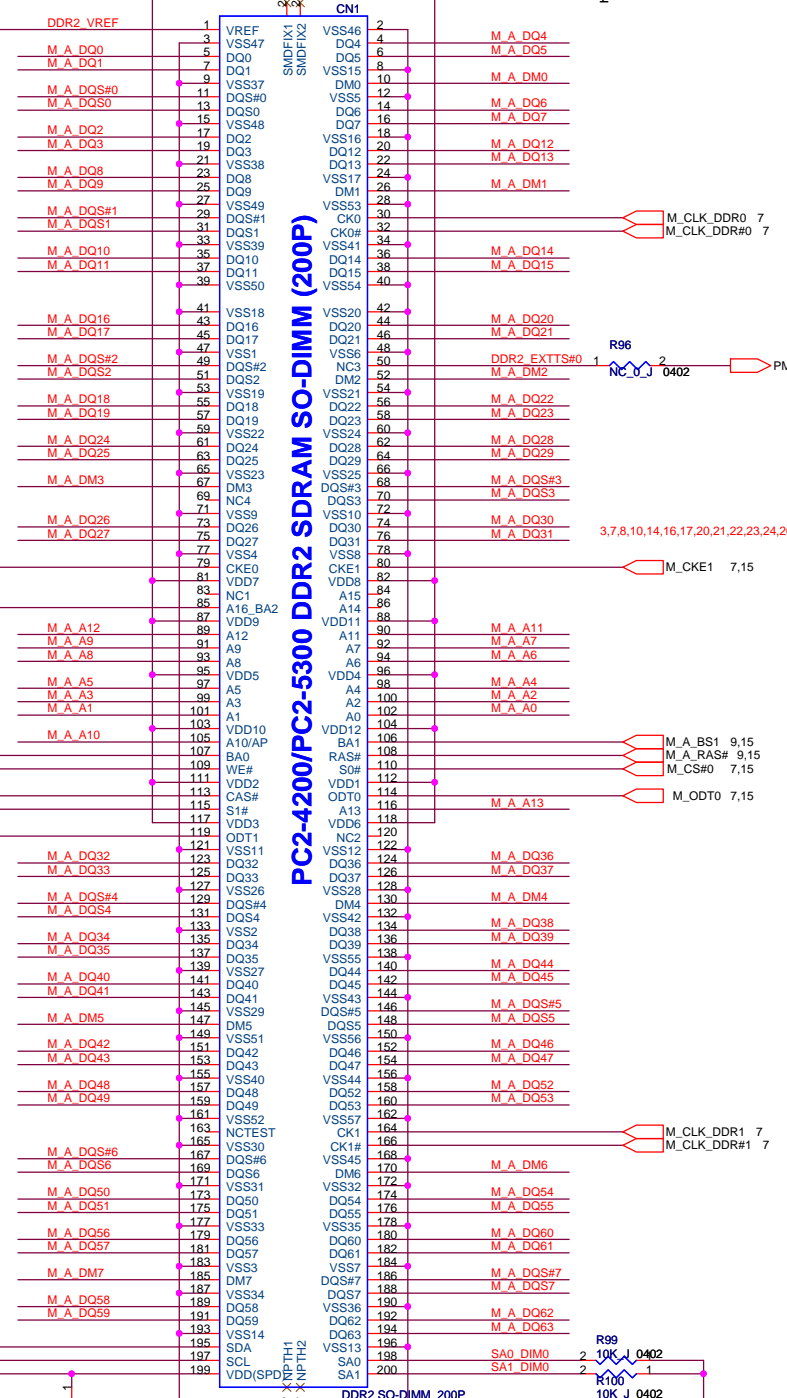
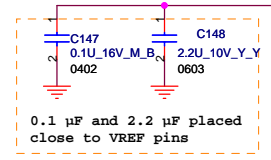
7 MCH_CFG_20 ← 1 ● 30MIL TP83

Layout Noe:
Location of all MCH_CFG strap resistors needs to be close to trace to minimize stub



7,11,14,41,48,50,51 +1_8VSUS

1.8V per DIMM=3.08A



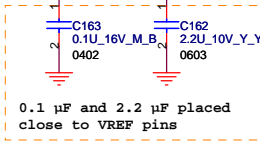
DIMM_0
 Place DIMM_0 near GMCH

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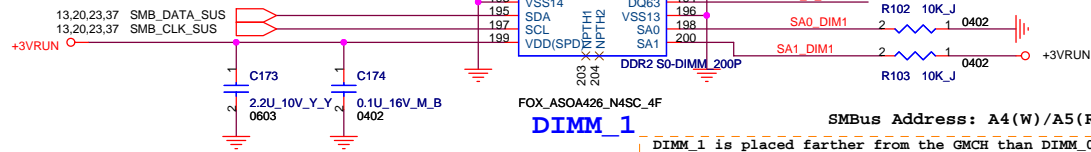
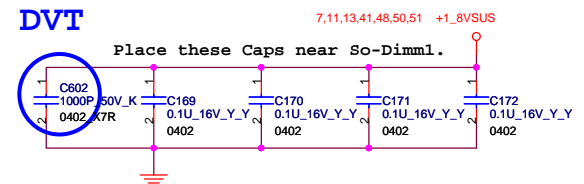
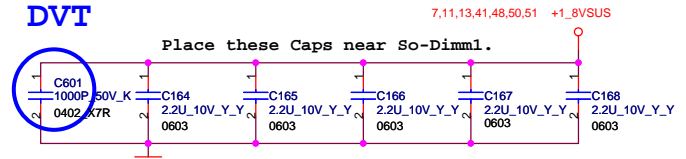
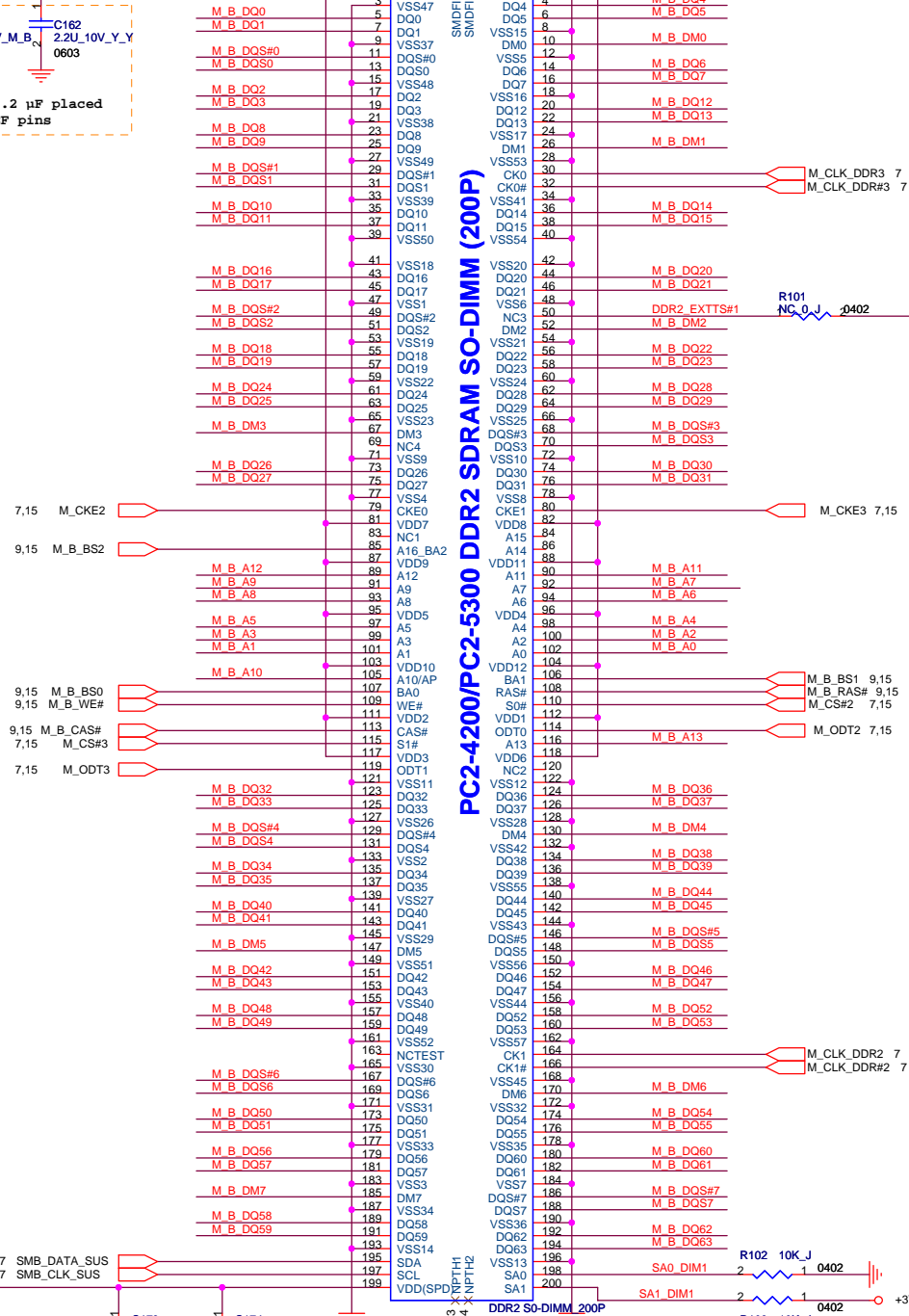
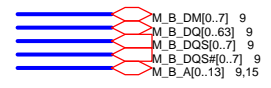
File: **DDR(H)SO-DIMM_0**

Size A3	Document Number MS70-1-01	Rev 2.0
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Date: Tuesday, August 22, 2006 Sheet 13 of 55



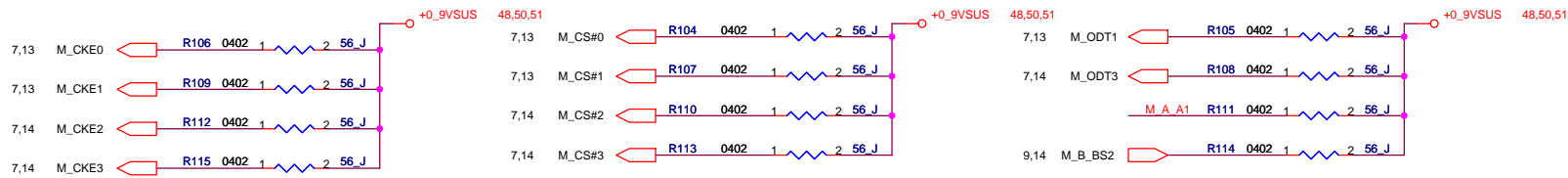
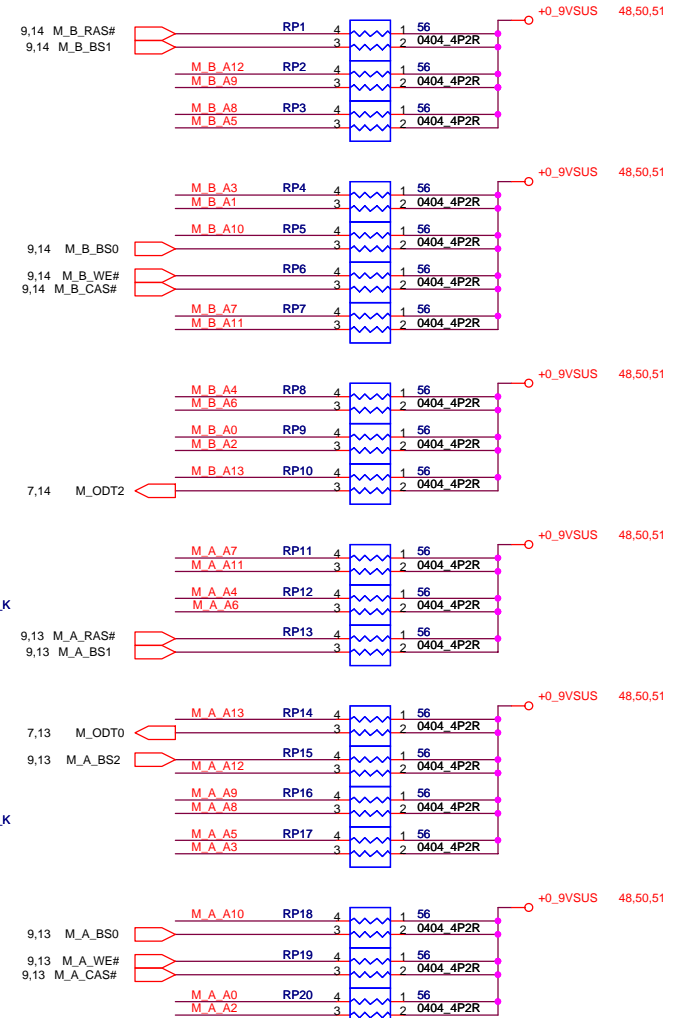
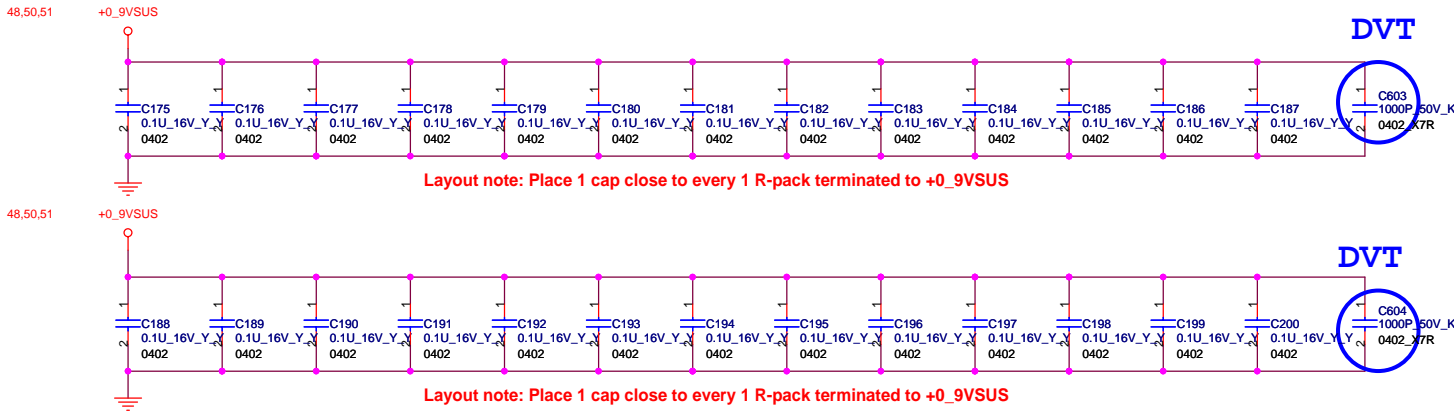
1.8V per DIMM=3.08A



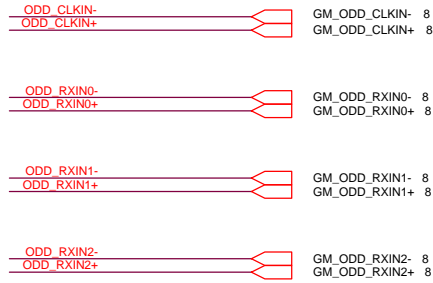
FOXCONN HON HAI Precision Ind. Co., Ltd.
 CCPBG - R&D Division

File: **DDR(I)SO-DIMM_1**

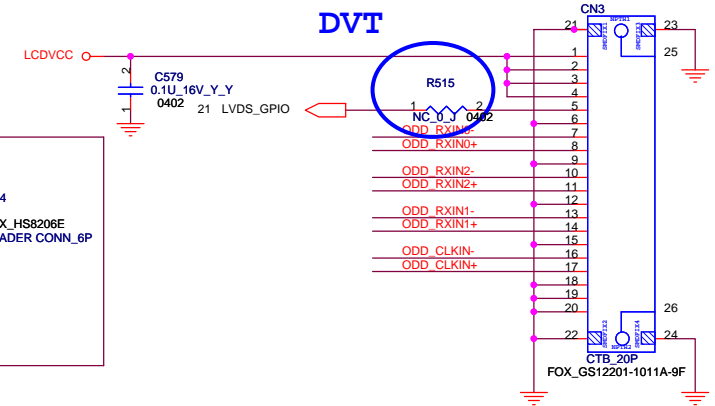
Size A3	Document Number MST0-1-01	Rev 2.0
Date: Tuesday, August 22, 2006	Sheet 14	of 55



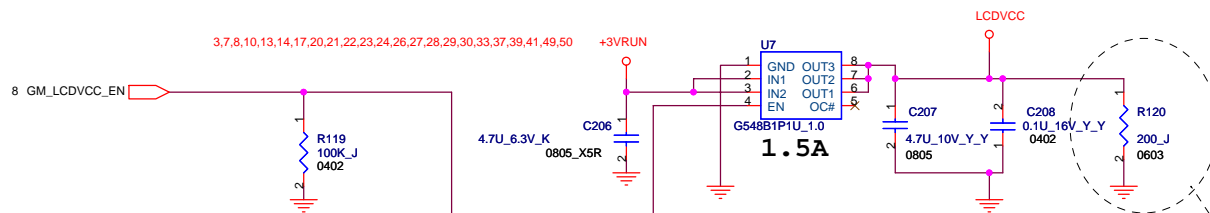
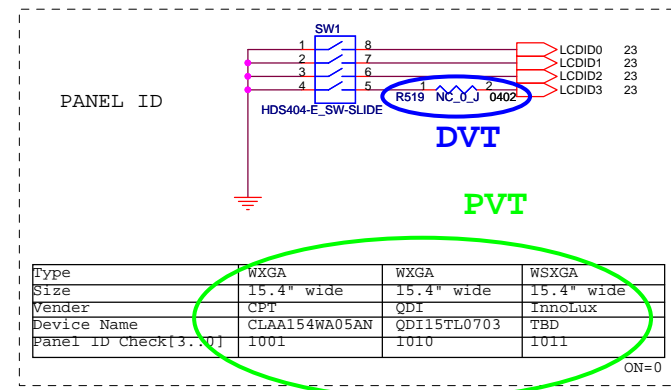
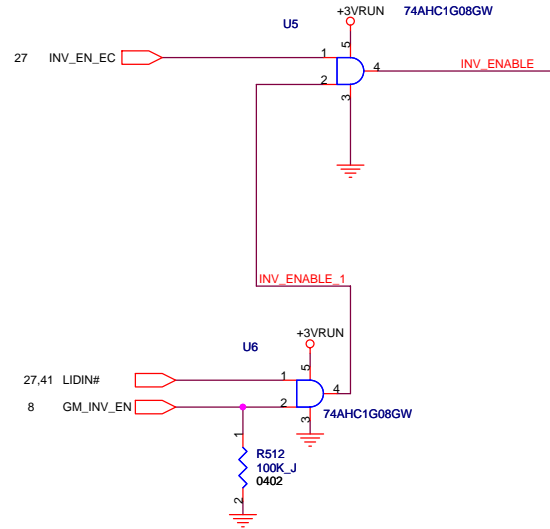
LVDS



LVDS CONNECTOR



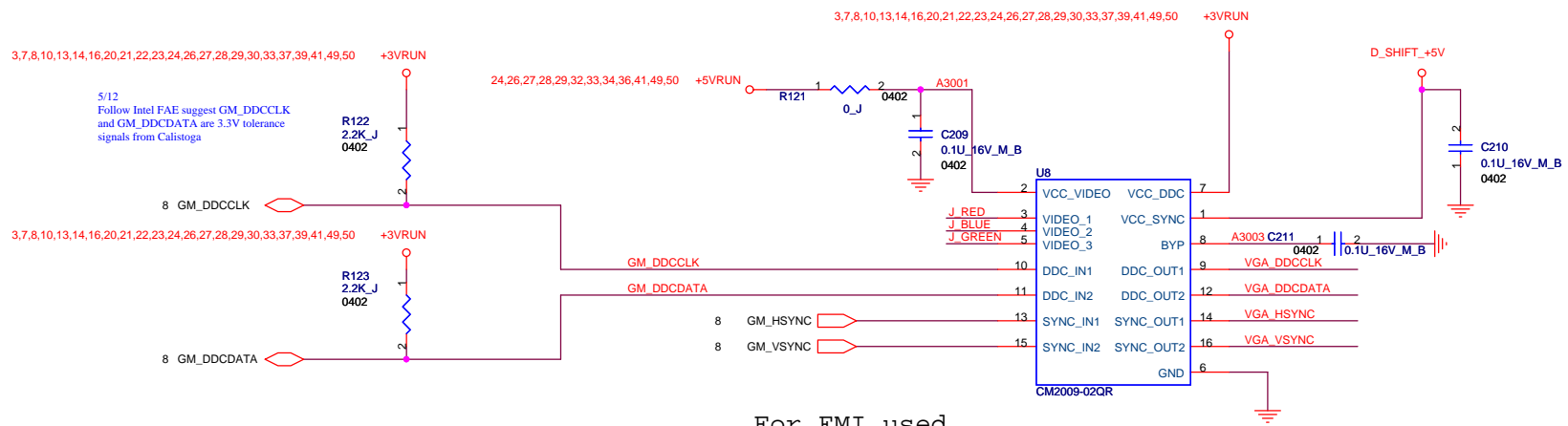
INVERTER CONNECTOR



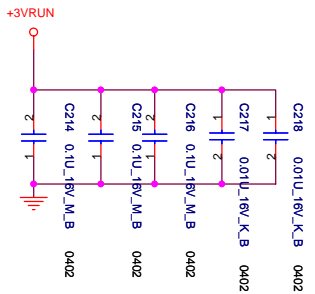
DISCHARGE
 The R461 will consume about 0.054 Watt (3.3x3.3/200 = 0.054W). We changed resistor to 0603 size (1/8 Watt)

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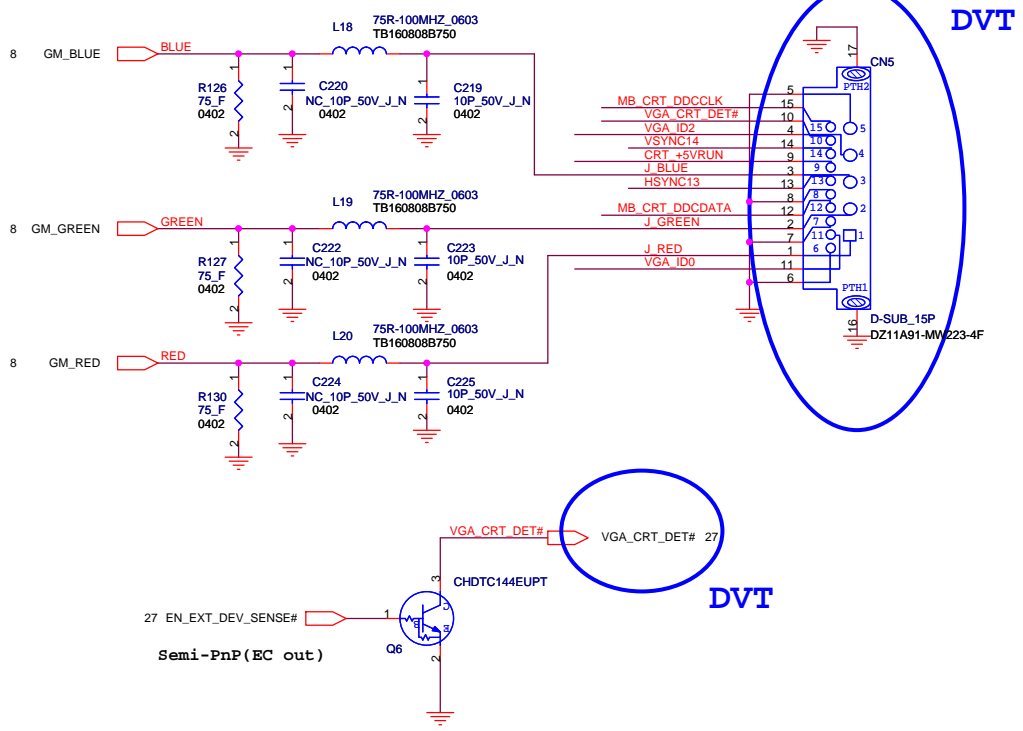
Title LVDS
Size A3 **Document Number** MS70-1-01 **Rev** 2.0
Date: Tuesday, August 22, 2006 **Sheet** 16 **of** 55



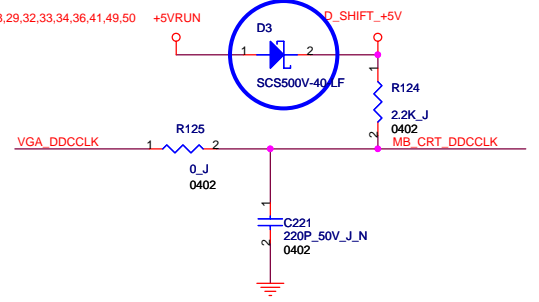
For EMI used



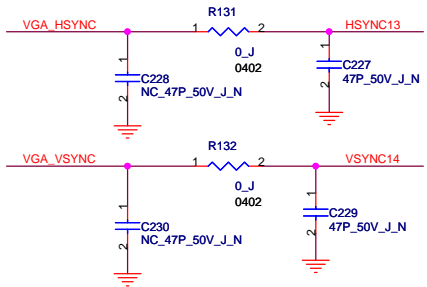
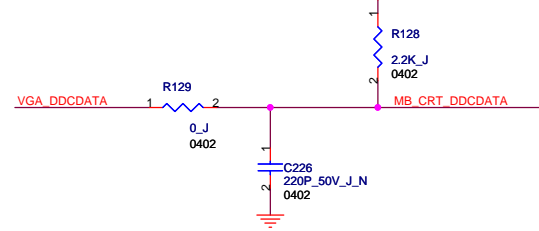
CRT CONNECTOR



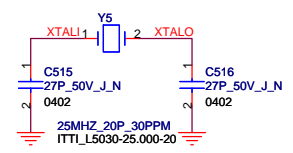
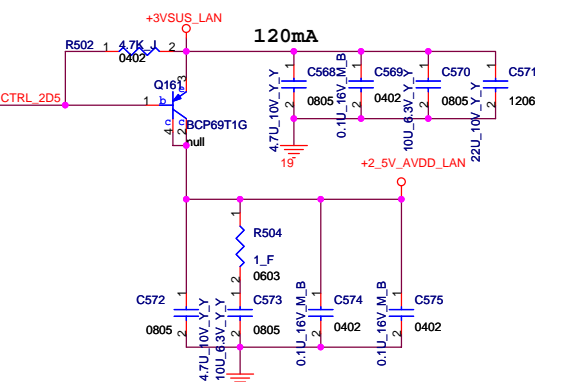
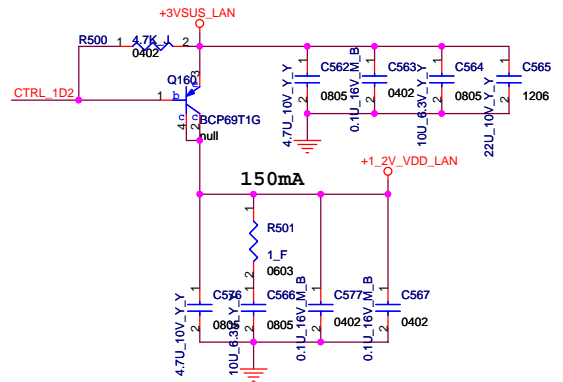
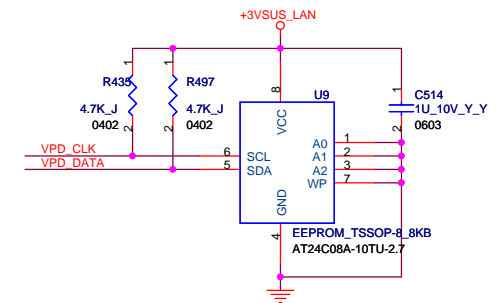
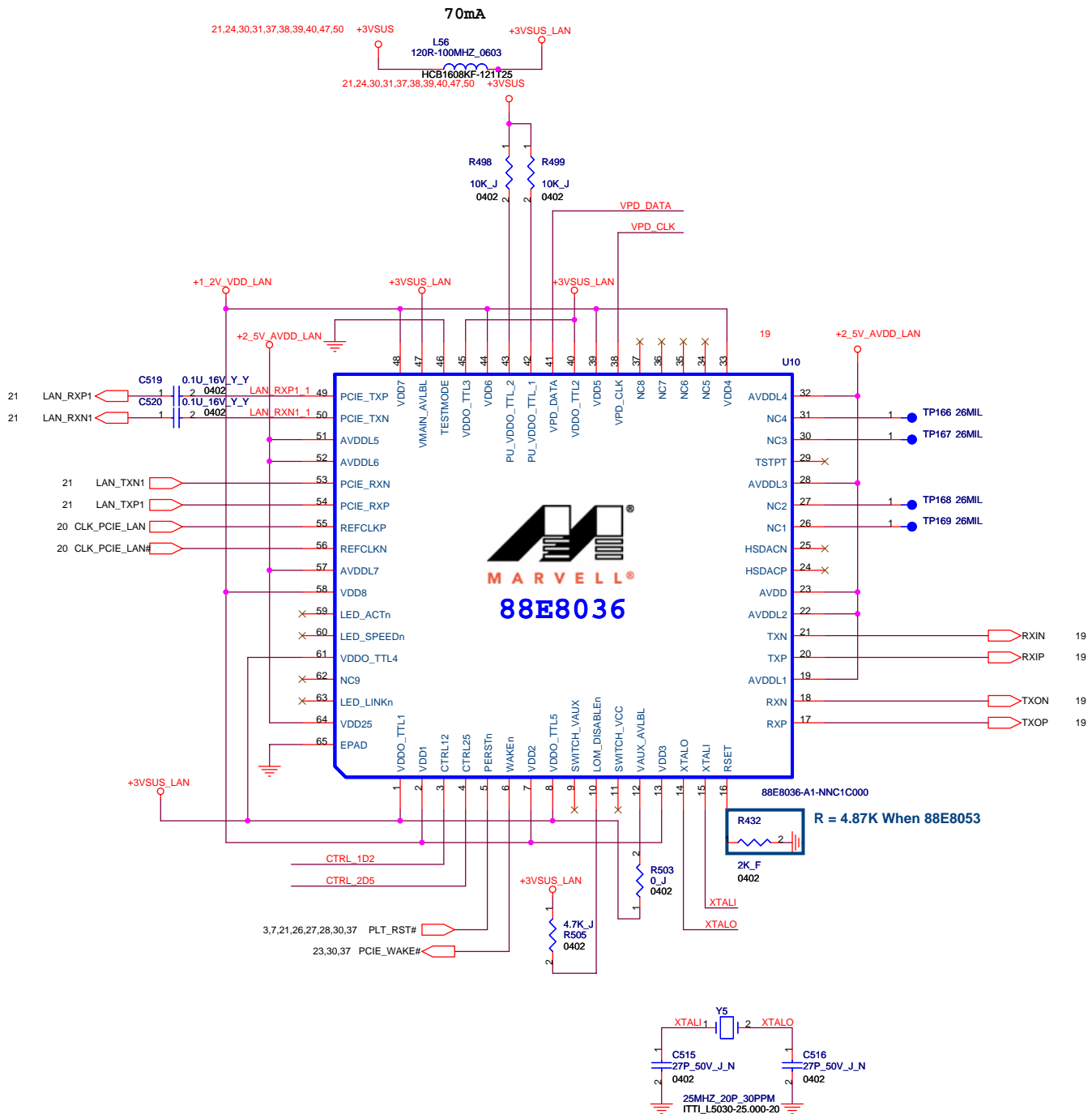
DVT

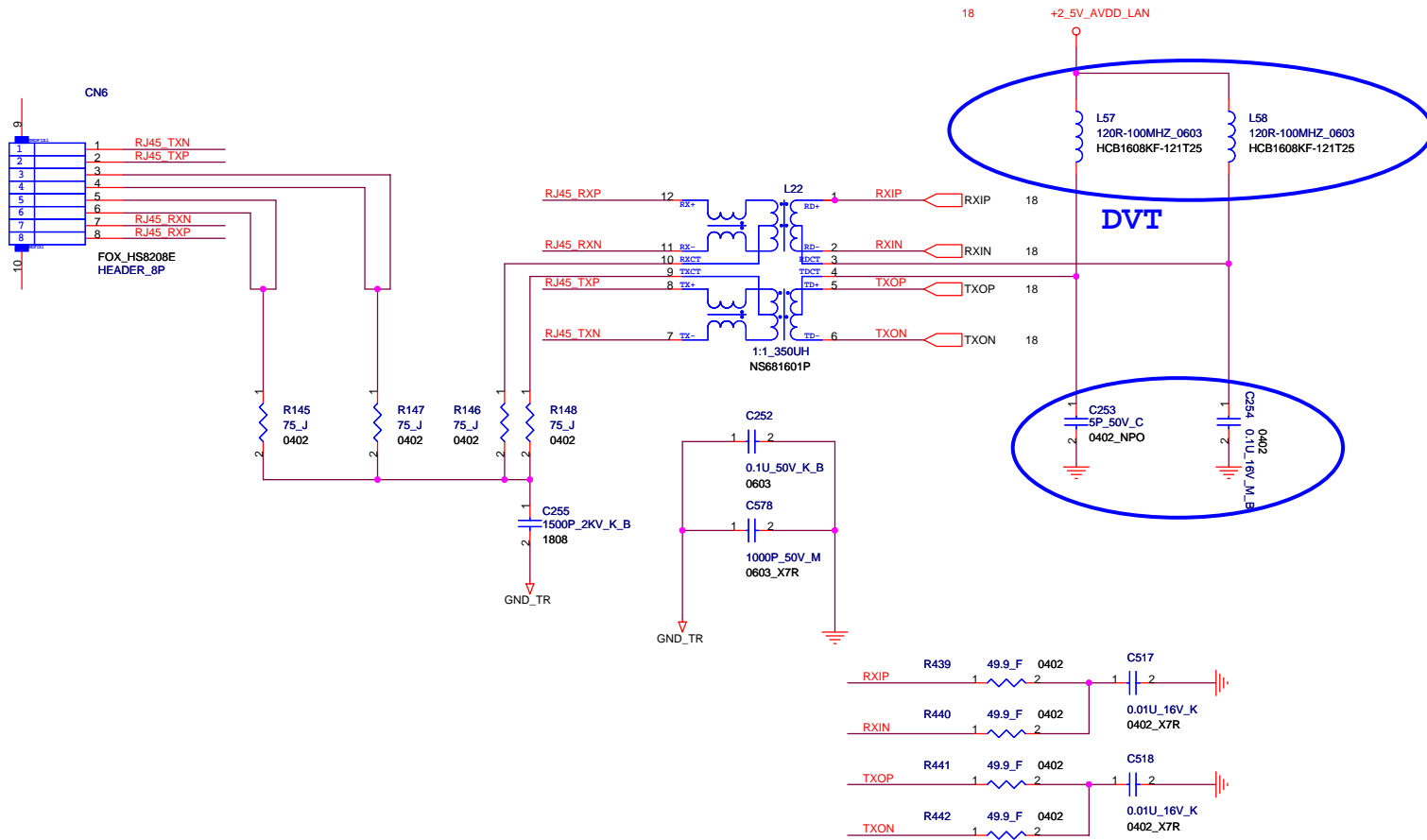


D_SHIFT_+5V



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File	CRT	
Size	Document Number	Rev
A3	MS70-1-01	2.0
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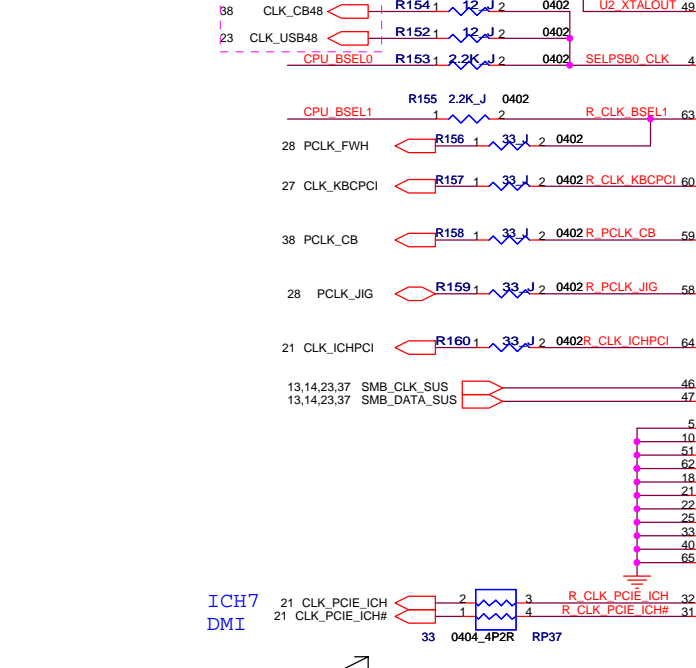




NC_10P_50V_E_N	2	1	CLK_CB48
NC_10P_50V_E_N	2	1	CLK_USB48
NC_10P_50V_E_N	2	1	CLK_KBCPCI
NC_10P_50V_E_N	2	1	PCLK_CB
NC_10P_50V_E_N	2	1	PCLK_FWH
NC_10P_50V_E_N	2	1	CLK_ICHPCI
NC_10P_50V_E_N	2	1	CLK_ICH14
NC_10P_50V_E_N	2	1	PCLK_JIG

close to clk gen (For EMI)

Length as short as possible.



06/17
CLK_PCIE_ICH changed to SRCLK7
CLK_DOCK_LAN changed to SRCLK8
SW Note: datasheet page13 Byte8.1 => SRCLK7 should be configured as "Not Controlled"

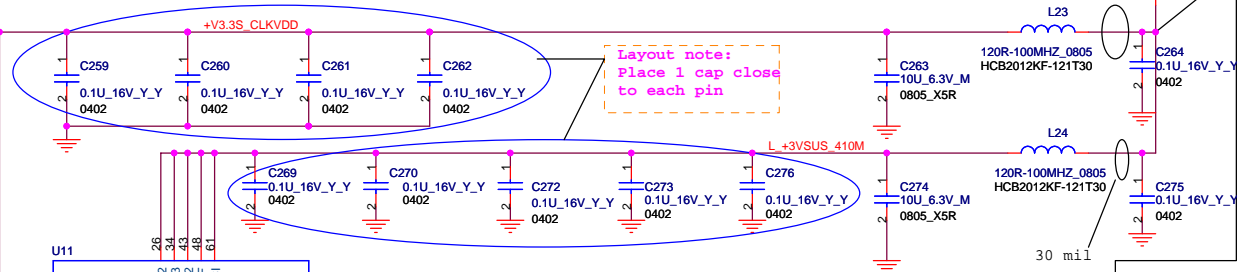
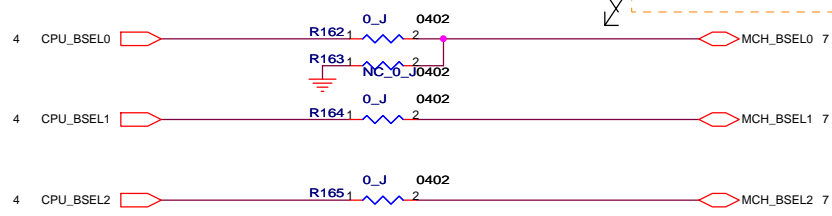
SM bus Address 6SLR321BKLF
1101001 (ICH7)
For clock generator

06/09
DEL pull-up resistor R80-82
pull-down resistor R85,R88
Del R84,R87,R90

06/16
ICS have recognized, FSLA/FSLB setting is different from CK410M spec. But MS10 will not use 100MHz, For test purpose, please move R91 from MCH_BSEL2 to MCH_BSEL0, and mount R89.

FSB Frequency Table:

FSLB	FSLA	CPU SRC[7:0]	PCI
0	0	100	100
0	1	133	100
1	0	200	100
1	1	166	100

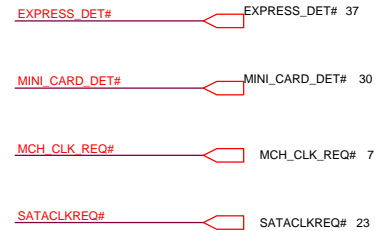
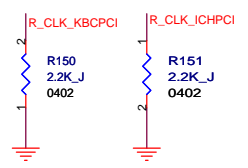


Layout note:
Place 1 cap close to each pin

06/16
pin53/59/60/64 with internal pull-up resistor
No Stuff Pull-up Resistor

06/09
CLKREQ with internal pull-up resistor
No Stuff Pull-up Resistor

Pin Straps	
Pin	Function
pin53	pin 11/12
0	SRCLK0
1	27MHz (v)
pin59	pin 15/16
0	SRCLK0
1	SATA (v)
pin60	pin 37/38
0	SRCLK8 (v)
1	CPU 2 ITP
pin64	pin 13/14
0	LDCCLK_SS (CA)
1	SRCLK1 (NV)



CALISTOGA Chip HOST
CPU

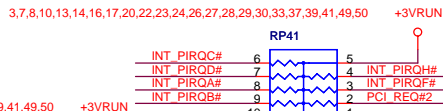
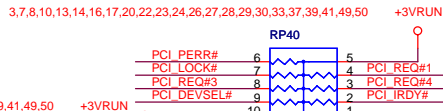
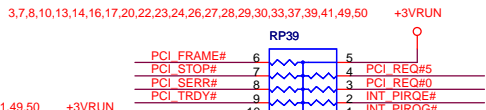
DVT

CALISTOGA SSSCK
CALISTOGA DOT96

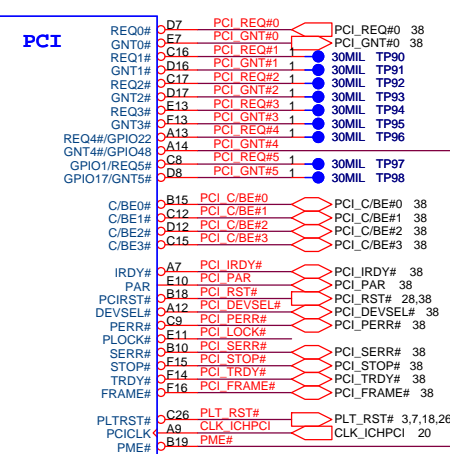
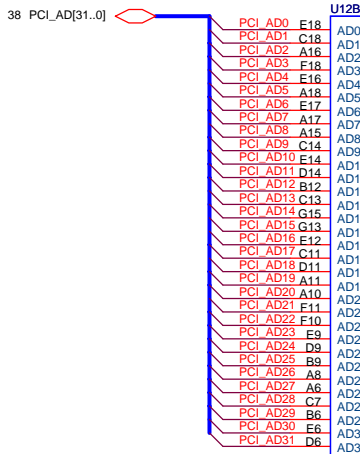
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File: **CLOCK GEN**

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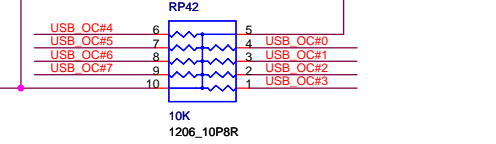
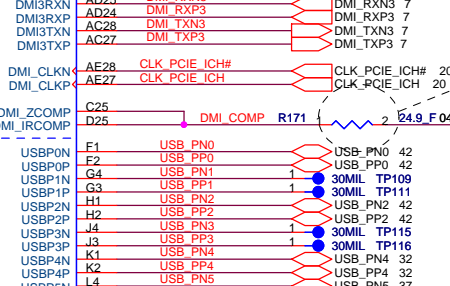
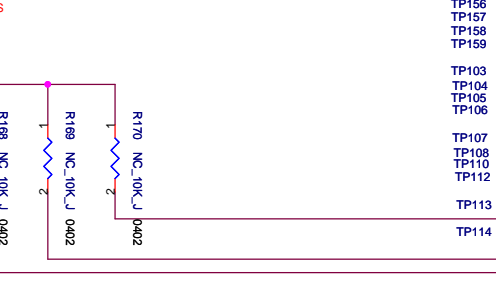
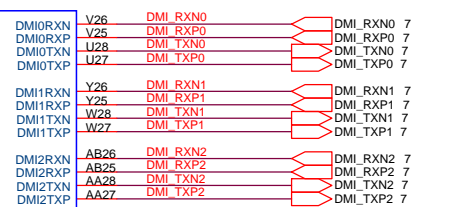
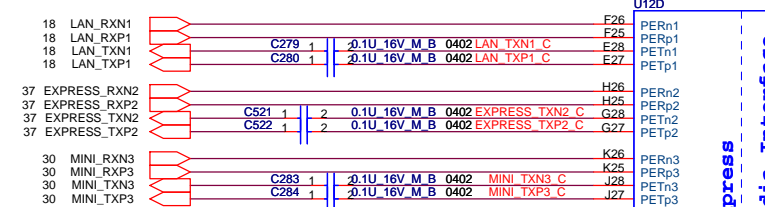
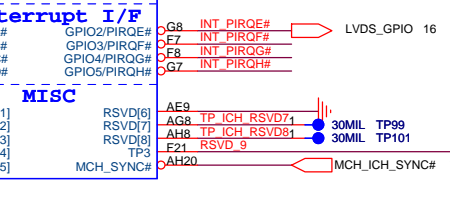
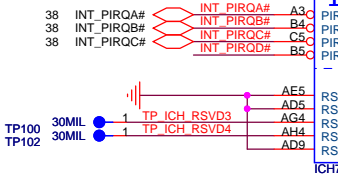


PCI Pullups



Strap for Boot-BIOS

	GNT5#	GNT4#
LPC(Default)	Hi	Hi
PCI	Hi	Low



Place within 500 mils of ICH

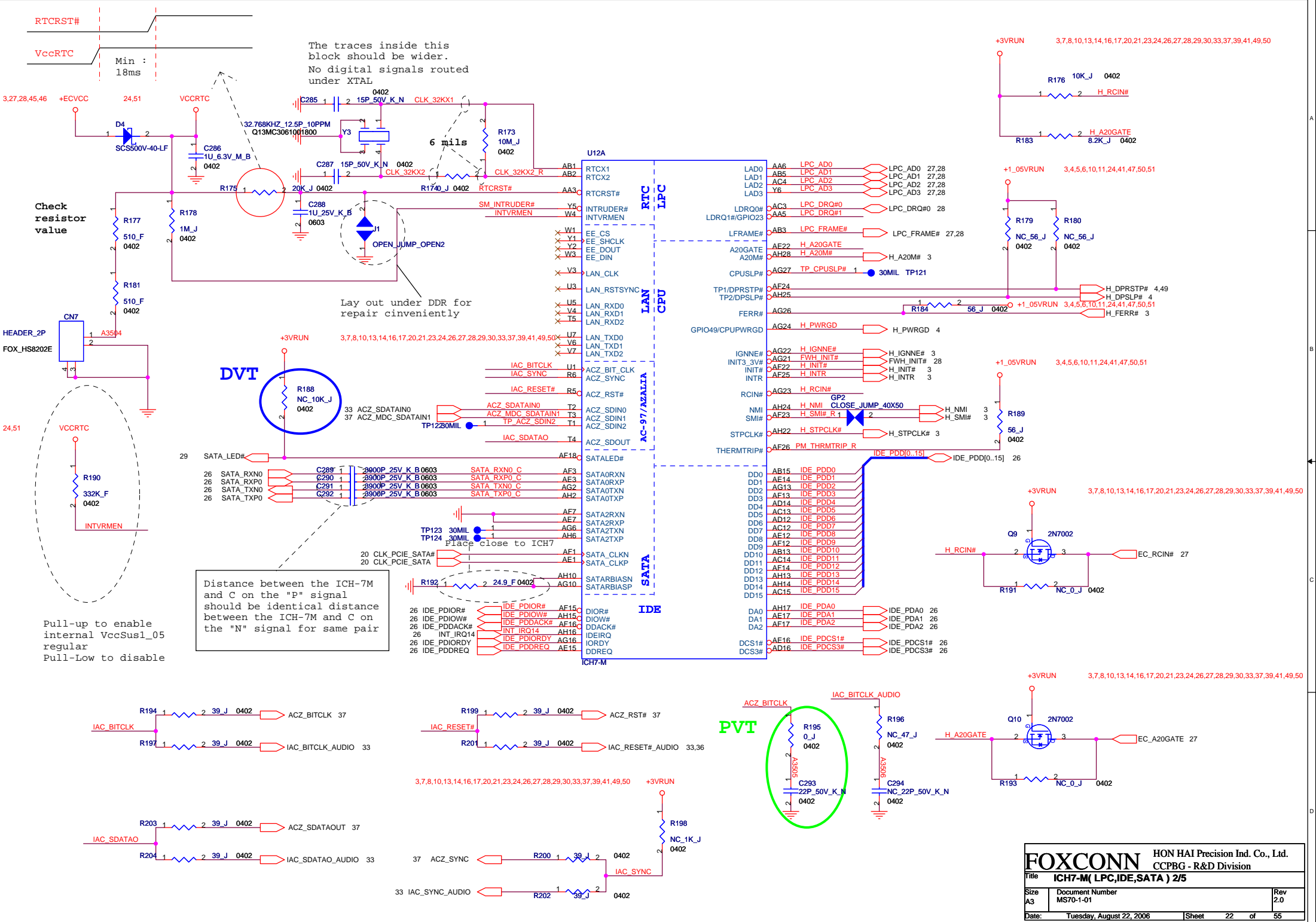
Place within 500 mils of ICH and don't routing next to high speed signals

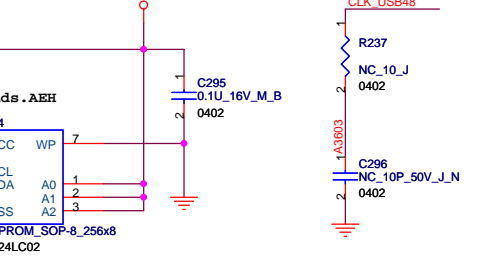
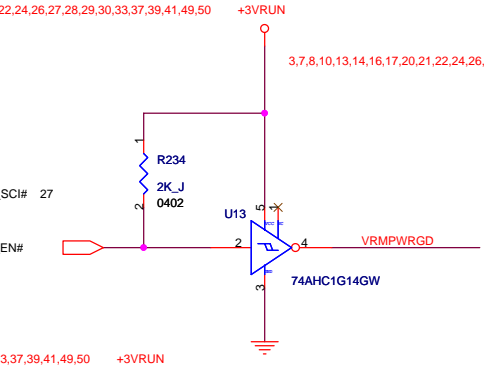
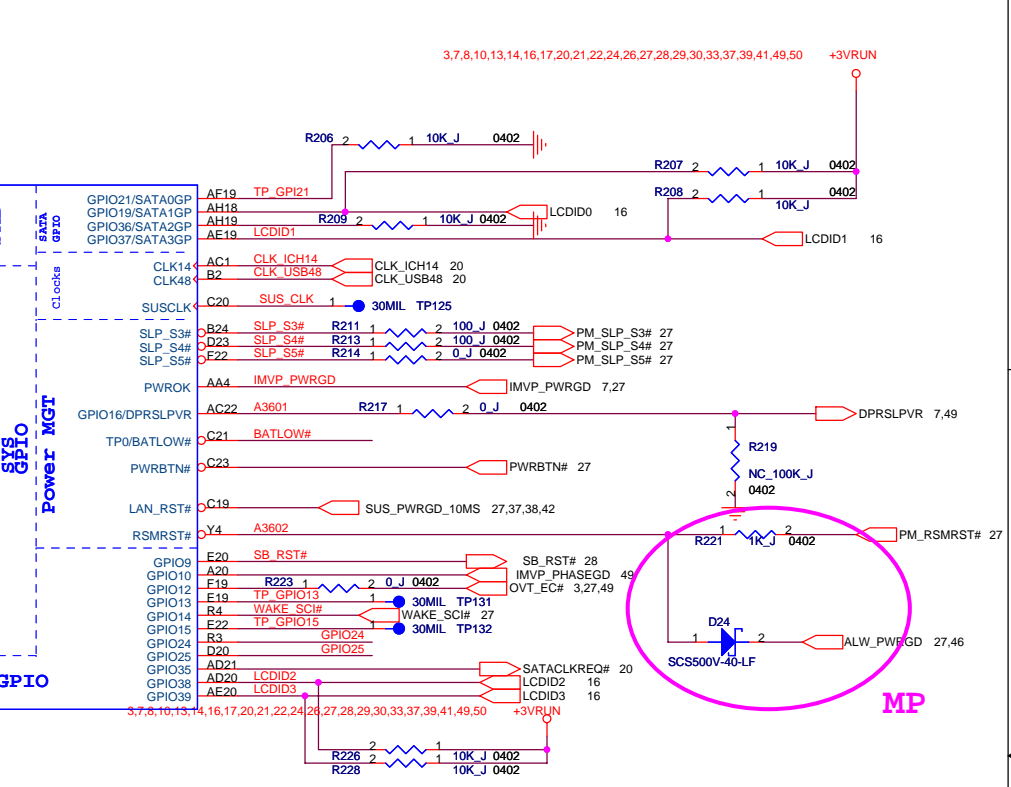
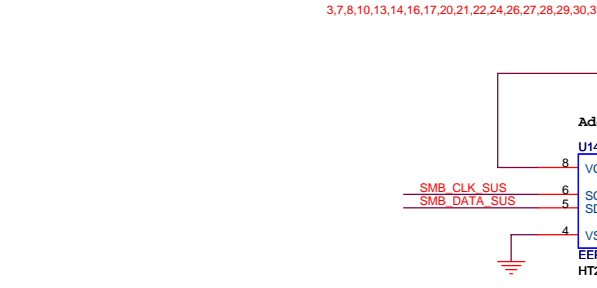
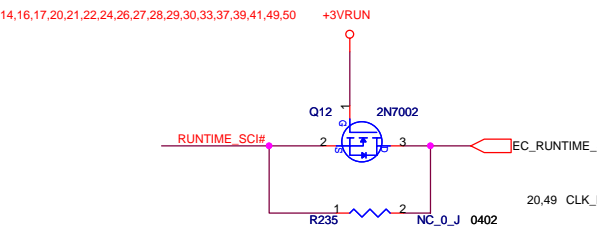
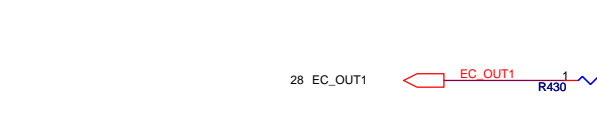
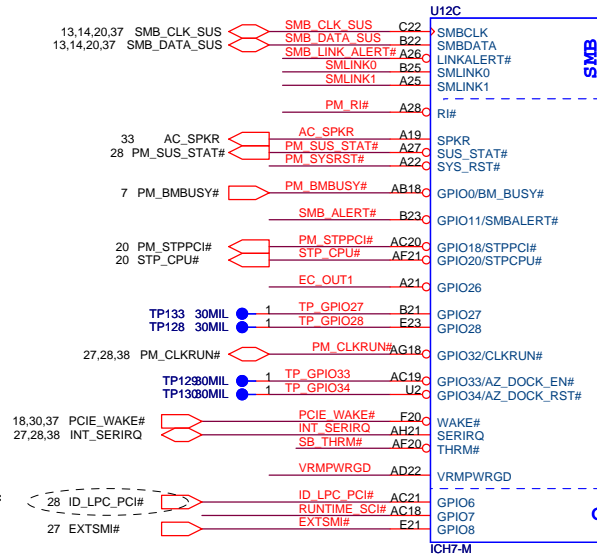
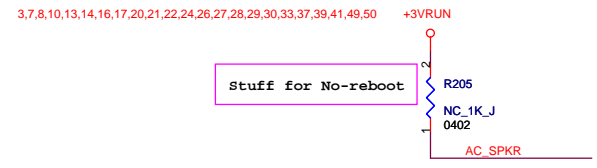
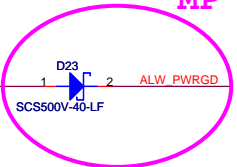
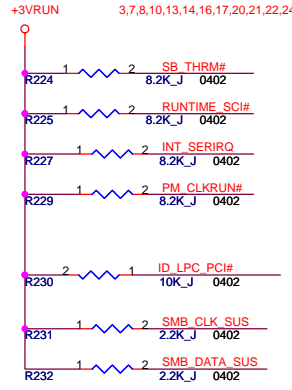
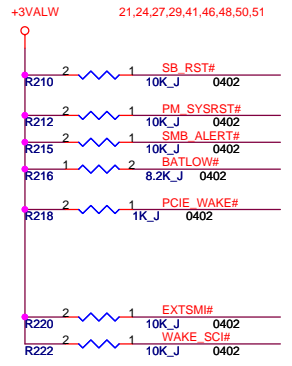
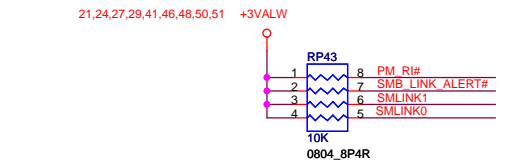
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Title: **ICH7-M(PC/DMI/USB/PCIE) 1/5**

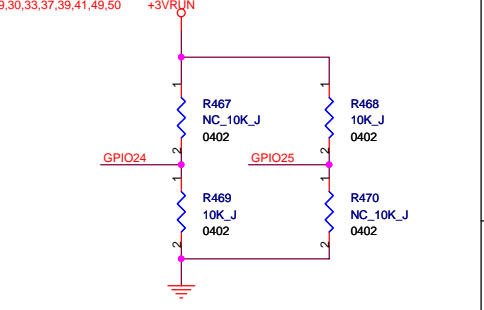
Size A3	Document Number MS70-1-01	Rev 2.0
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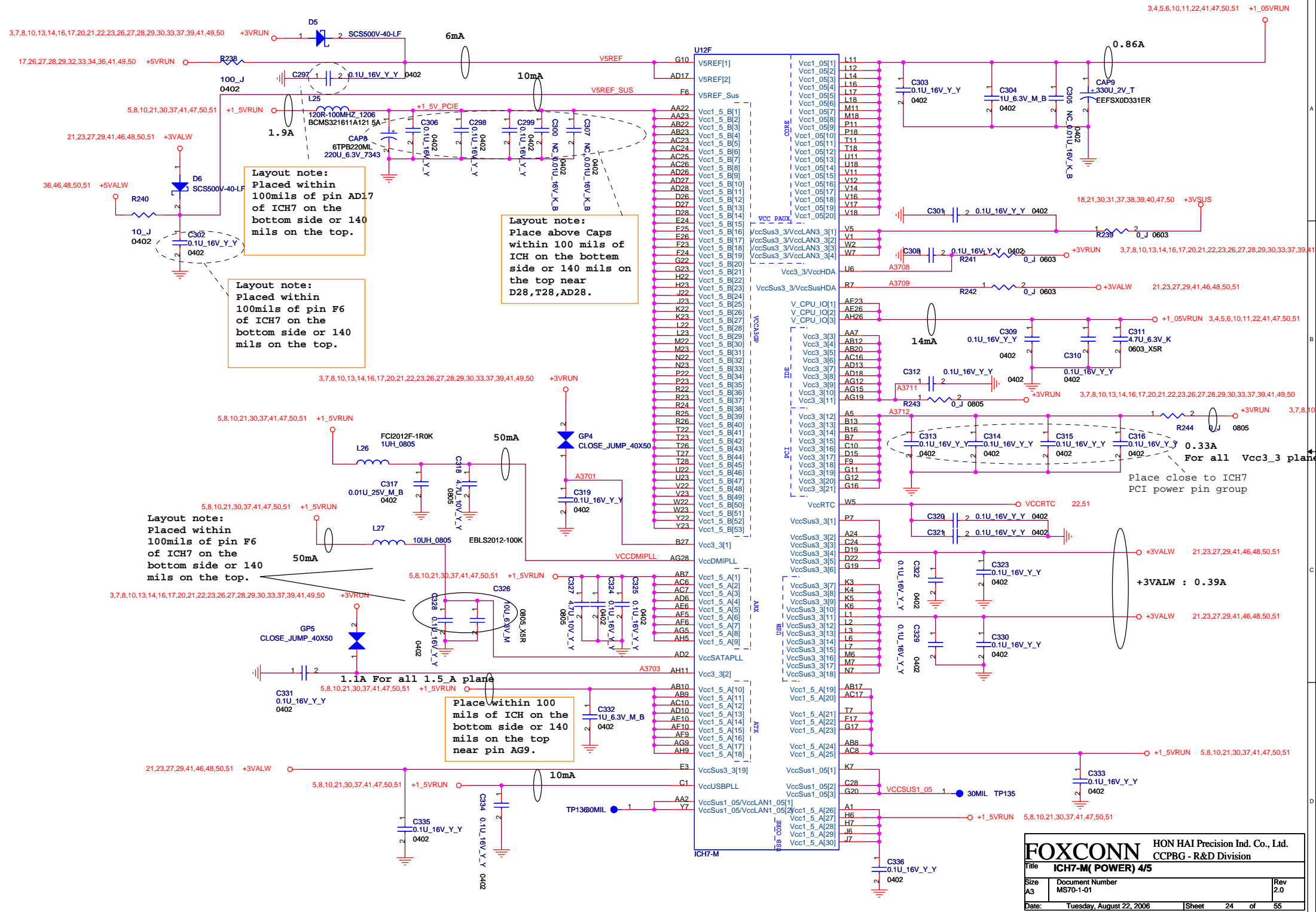
Date: Tuesday, August 22, 2006 | Sheet 21 of 55





for project identification





Layout note:
Placed within 100mils of pin AD1.7 of ICH7 on the bottom side or 140 mils on the top.

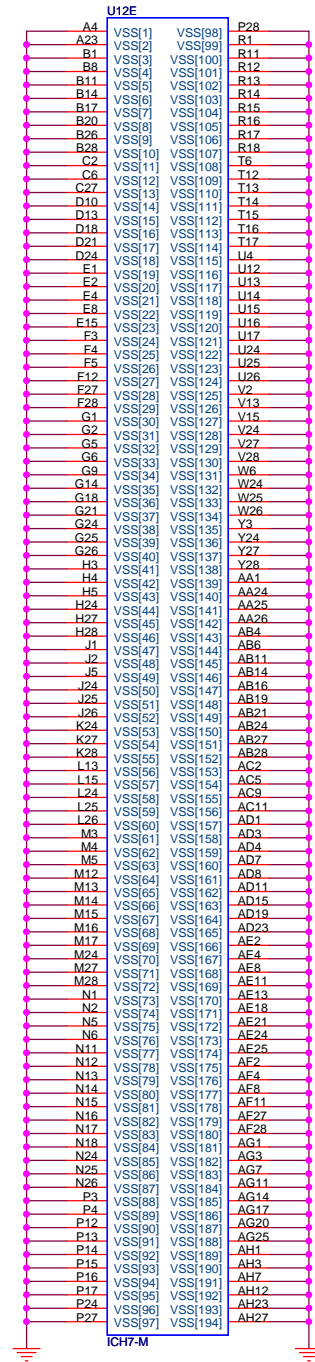
Layout note:
Place above Caps within 100 mils of ICH on the bottom side or 140 mils on the top near D28, T28, AD28.

Layout note:
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.

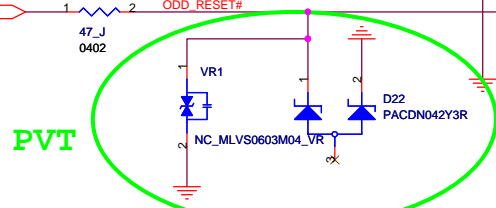
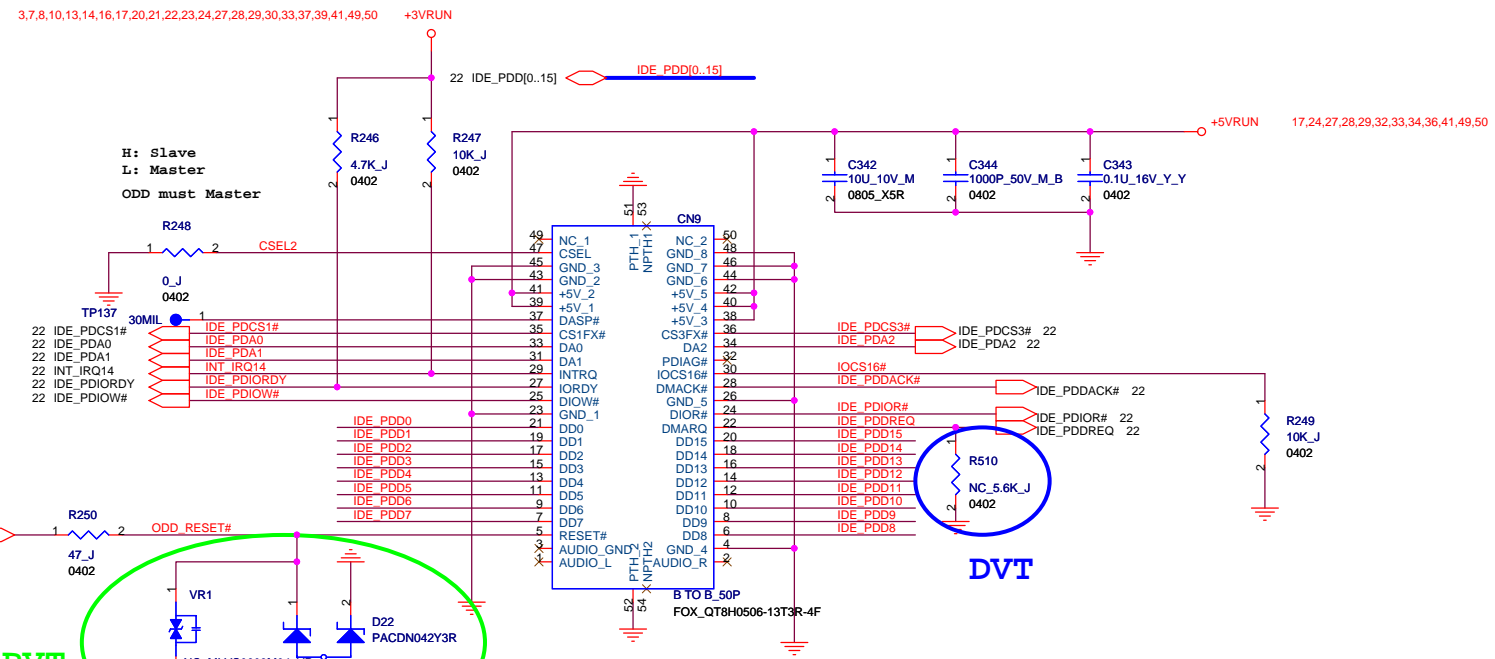
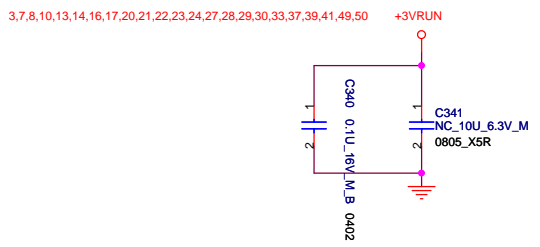
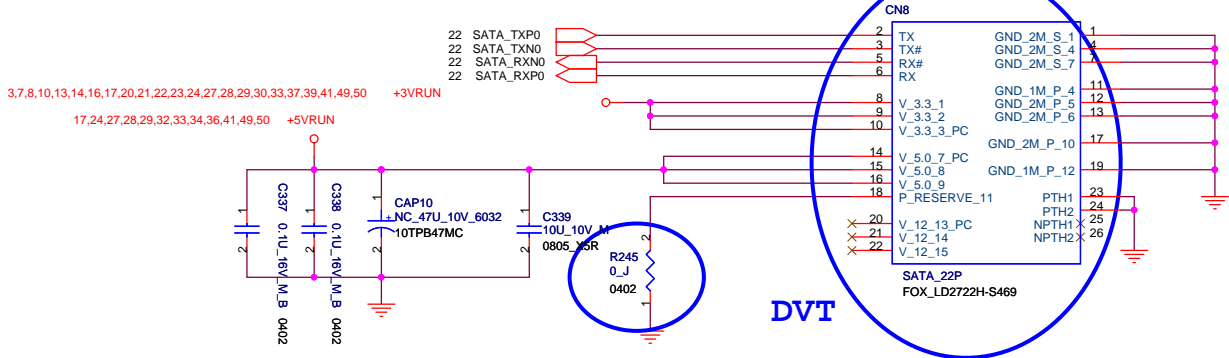
Layout note:
Placed within 100mils of pin F6 of ICH7 on the bottom side or 140 mils on the top.

Layout note:
Place within 100 mils of ICH on the bottom side or 140 mils on the top near pin AG9.

For all Vcc3_3 plane
Place close to ICH7 PCI power pin group



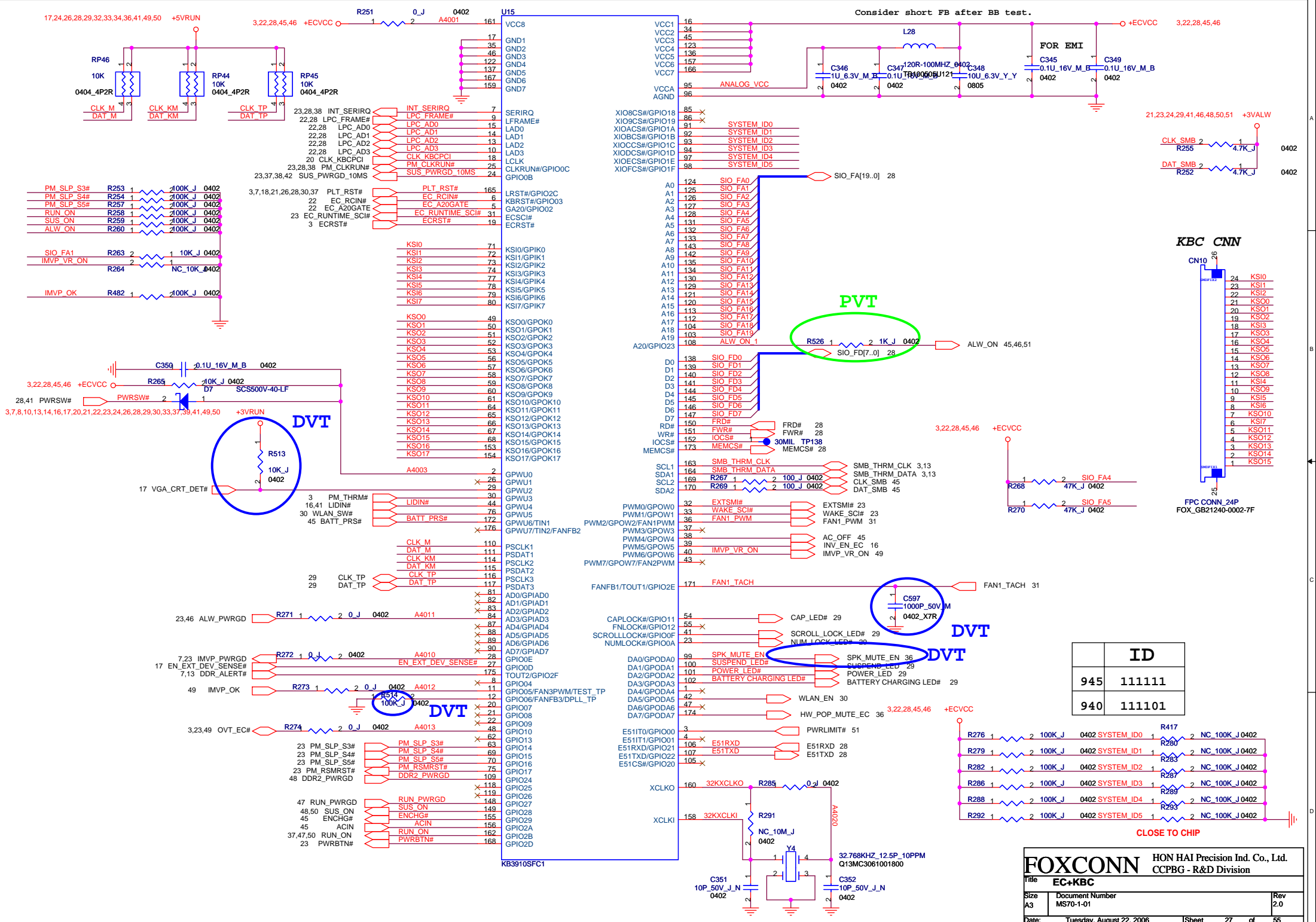
SATA HDD CONN



CD-ROM CONN

Follow Adoi san suggest ODD: Master/HDD:Slave

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title SATA HDD/CD-ROM			
Size A3	Document Number MS70-1-01	Rev 2.0	
Date: Tuesday, August 22, 2006	Sheet 26	of 55	



ID	
945	111111
940	111101

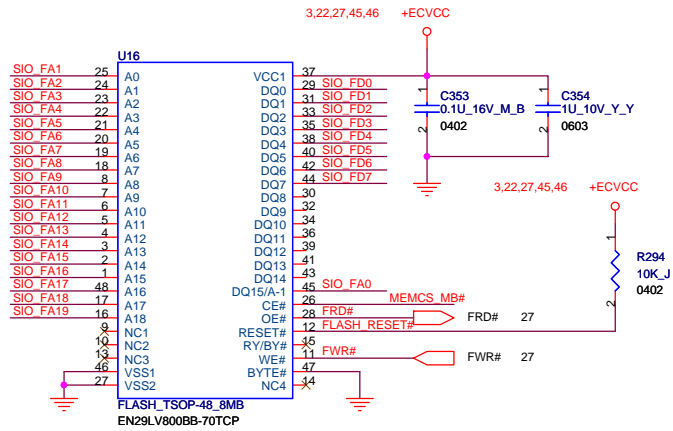
FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **EC+KBC**

Size: A3 | Document Number: MS70-1-01 | Rev: 2.0

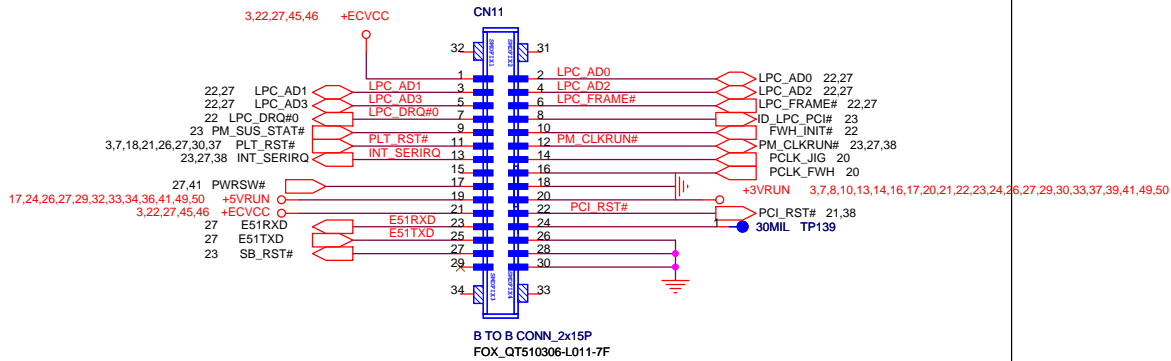
Date: Tuesday, August 22, 2006 | Sheet: 27 of 55

27 SIO_FA[19..0]
27 SIO_FD[7..0]

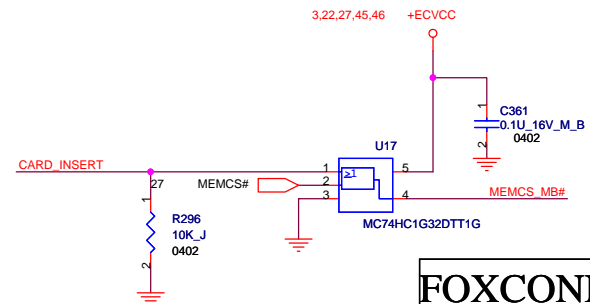
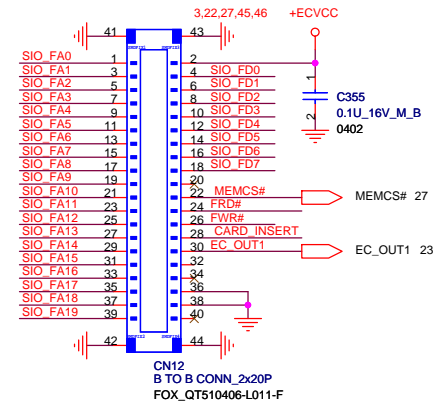


FLASH BIOS

JIG-120

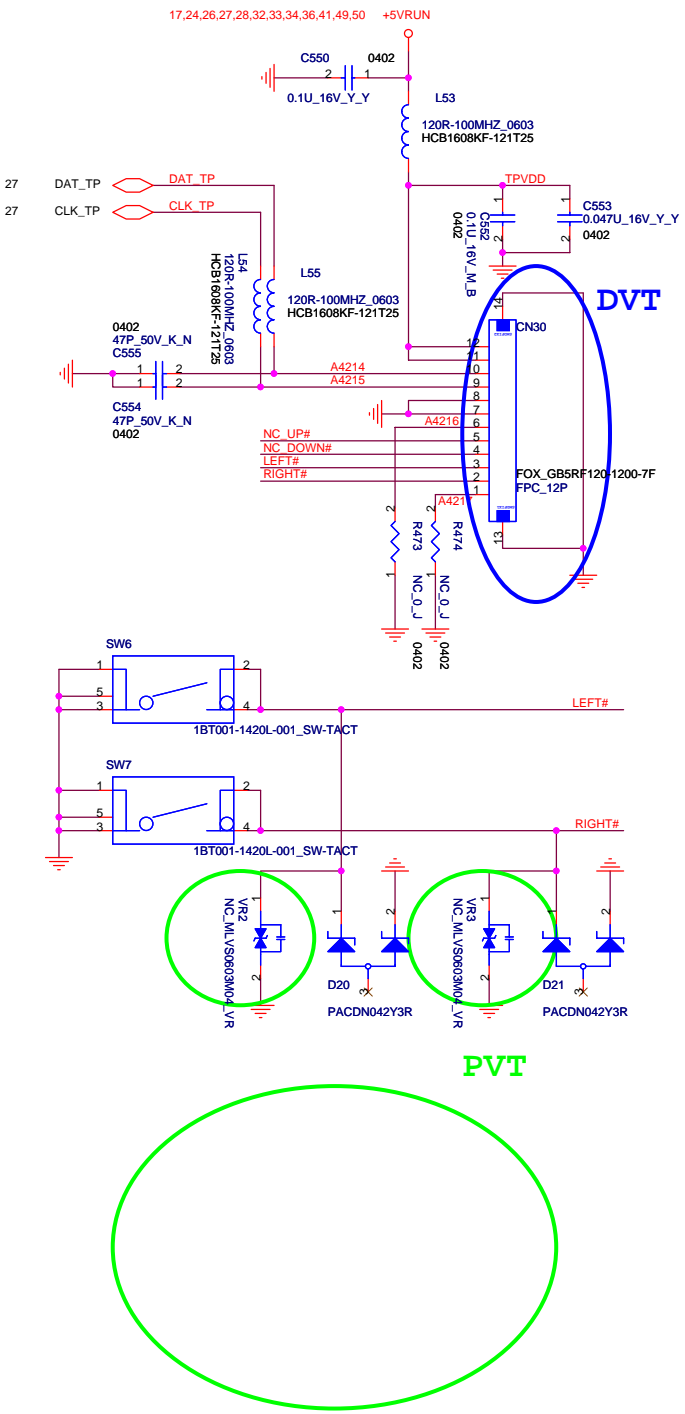


X-BUS

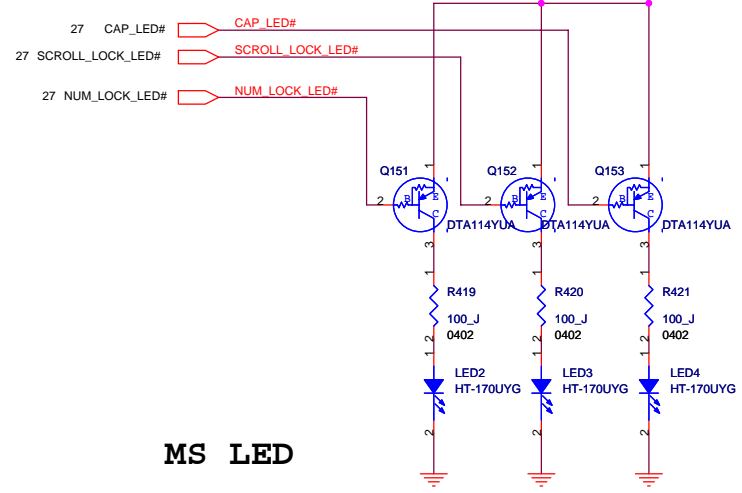


FOXCONN HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title Flash ROM/X-Bus/LID SW#		
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Date:	Tuesday, August 22, 2006	Sheet 28 of 55

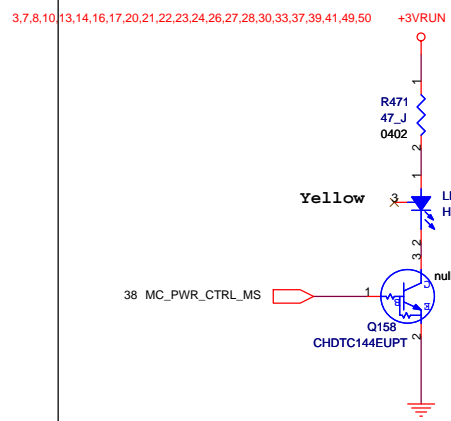
Touch Pad Board



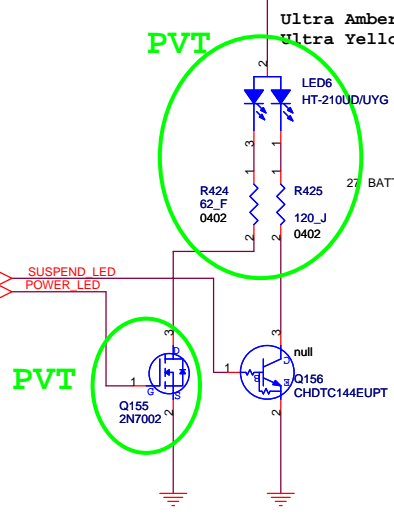
CAP_LED# SCROLL_LOCK_LED# NUM_LOCK_LED#



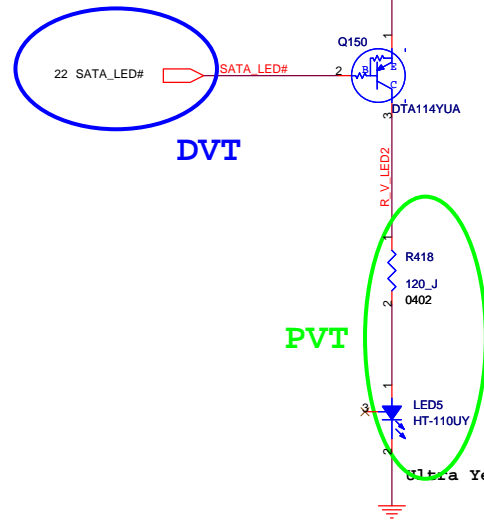
MS LED



POWER/SUSPEND LED

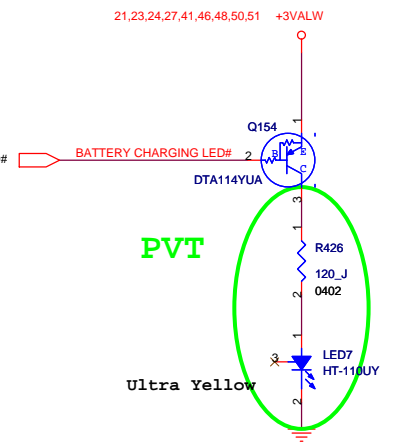


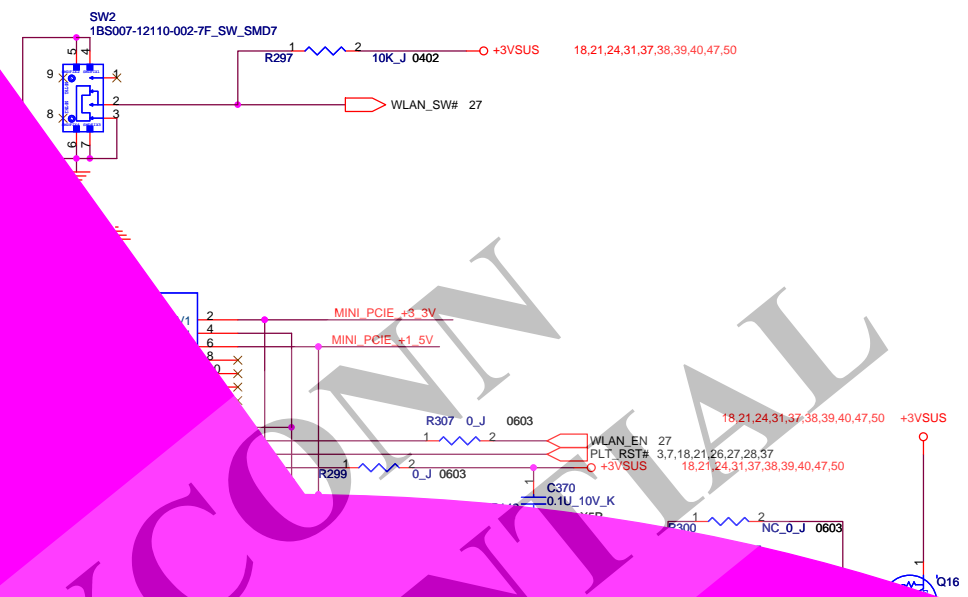
HDD_LED#



PVT

BATTERY CHARGING LED#





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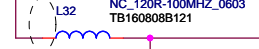
17,24,26,27,28,29,33,34,36,41,49,50

+5VRUN



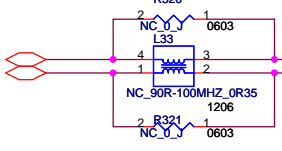
F1
NC_6V-0.35A_1206
1206L035

10mils



L32 NC_120R-100MHZ_0603
TB160808B121

21 USB_PN4
21 USB_PP4

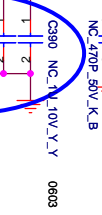


R320
NC_0 0603
L33
NC_90R-100MHZ_0R35
1206
R321
NC_0 0603

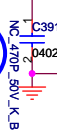


C598 NC_10U_10V_M
0805_X5R
C389 NC_10U_10V_M
0805_X5R

DVT



C390 NC_1V_10V_Y_Y
0803

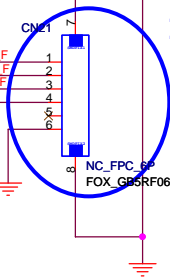


C391 NC_470P_50V_K_B



D402

Oide

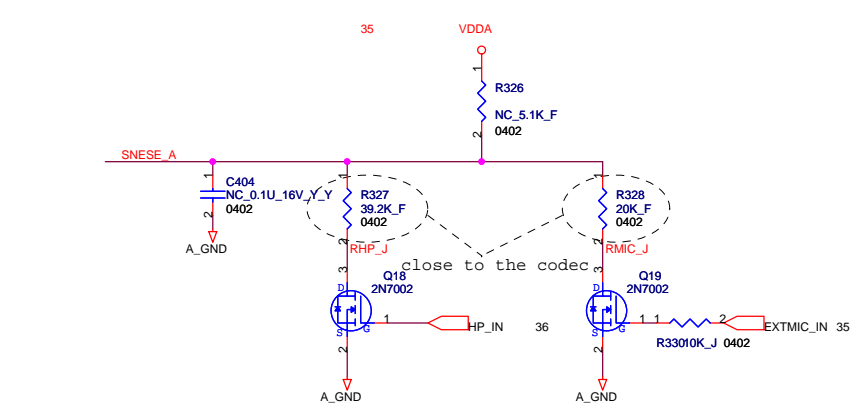
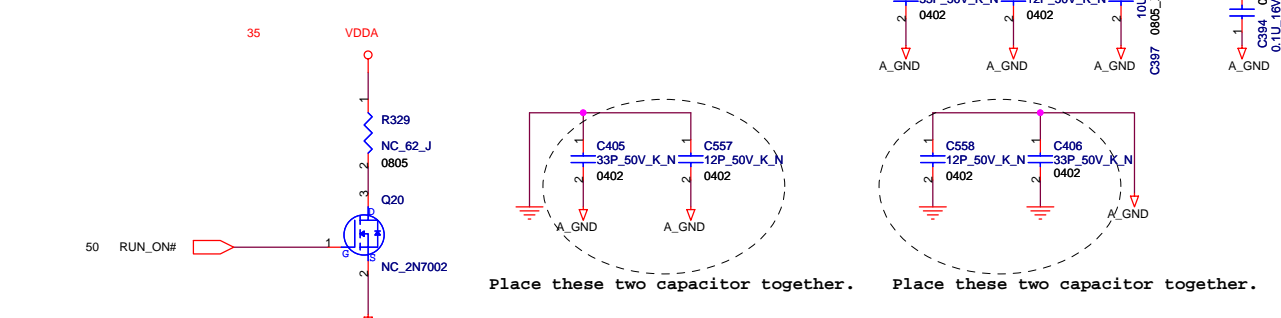
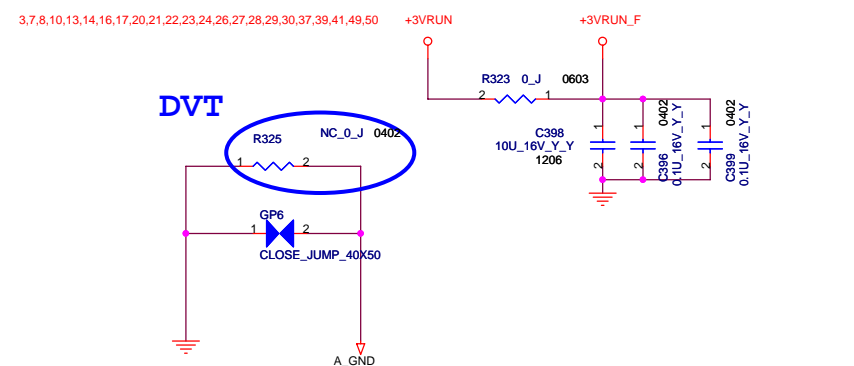
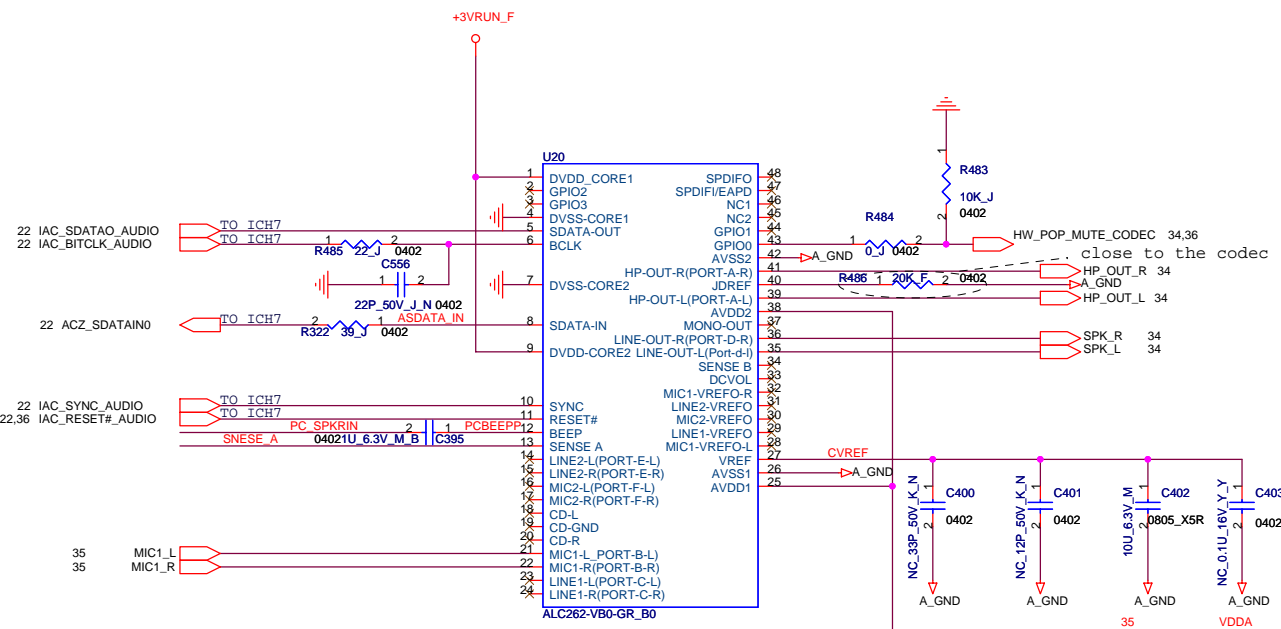


CNE1
1 HUB_VCC1 F
2 USB_VD4+ F
3 USB_VD4- F
4
5
6
7 NC_FPC_6P
FOX_GB5RF060-1200-7F
8

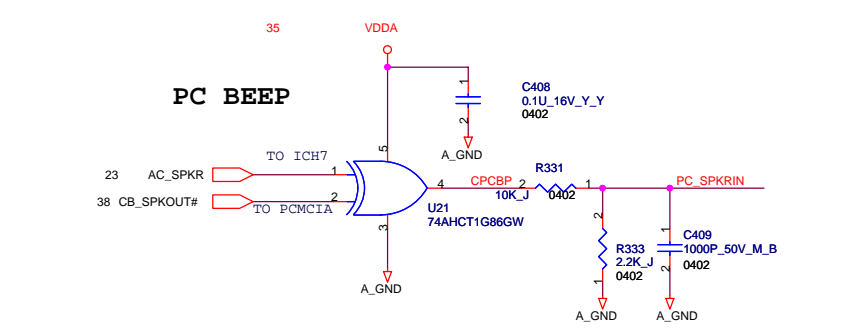
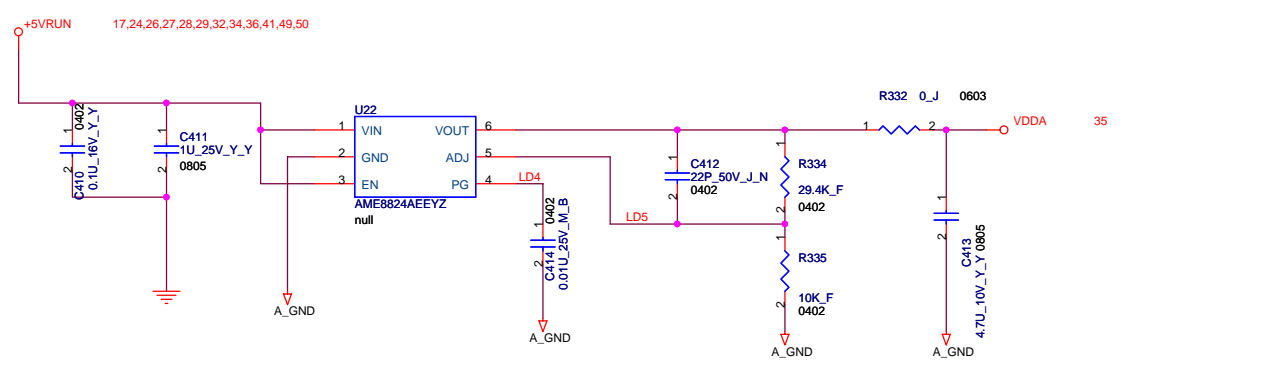
DVT

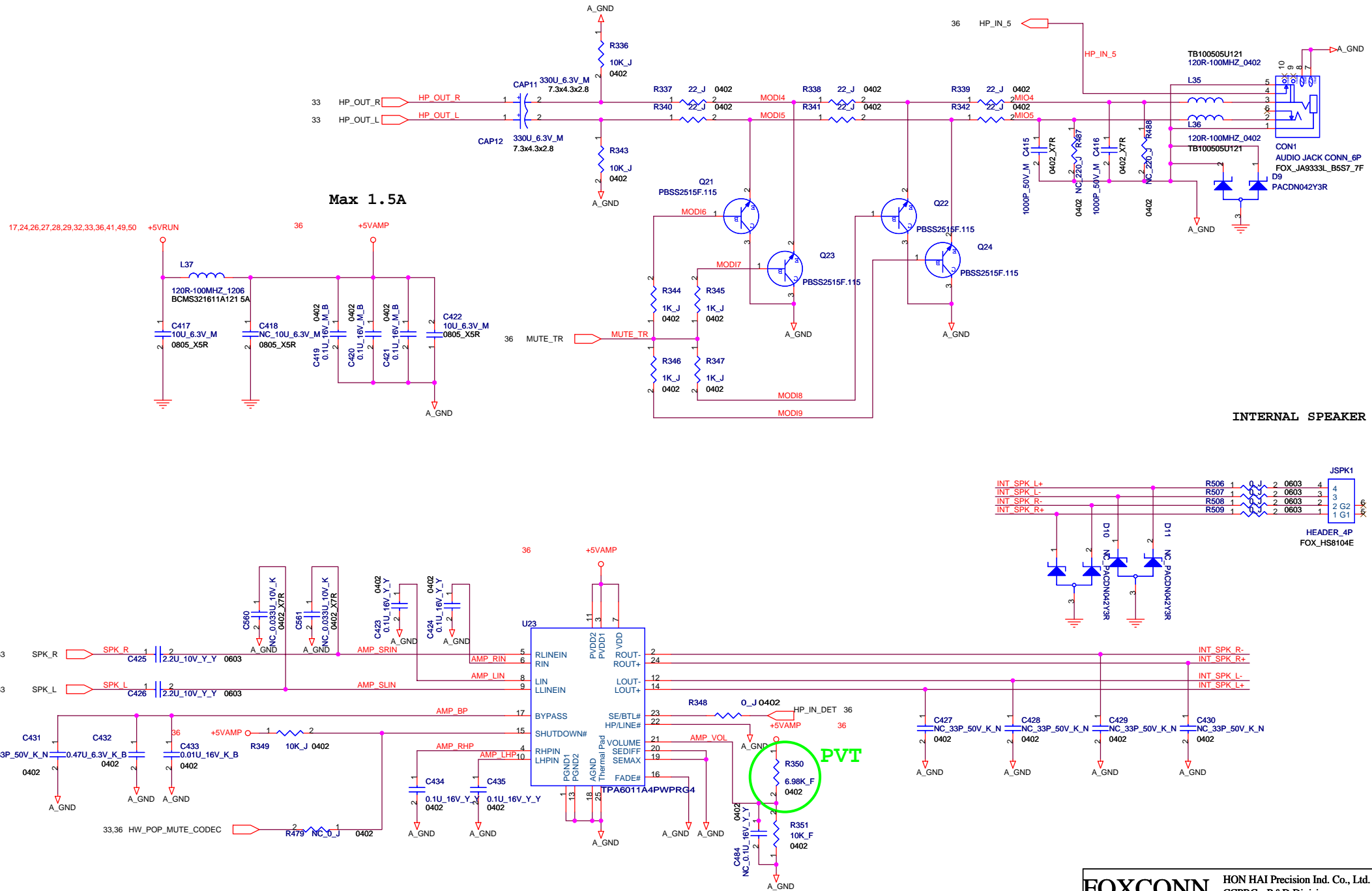
PVT

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title OIDE		CCPBG - R&D Division	
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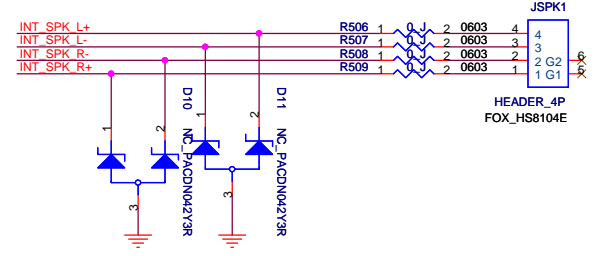
AUDIO POWER(Change to 4.75V/200mA)

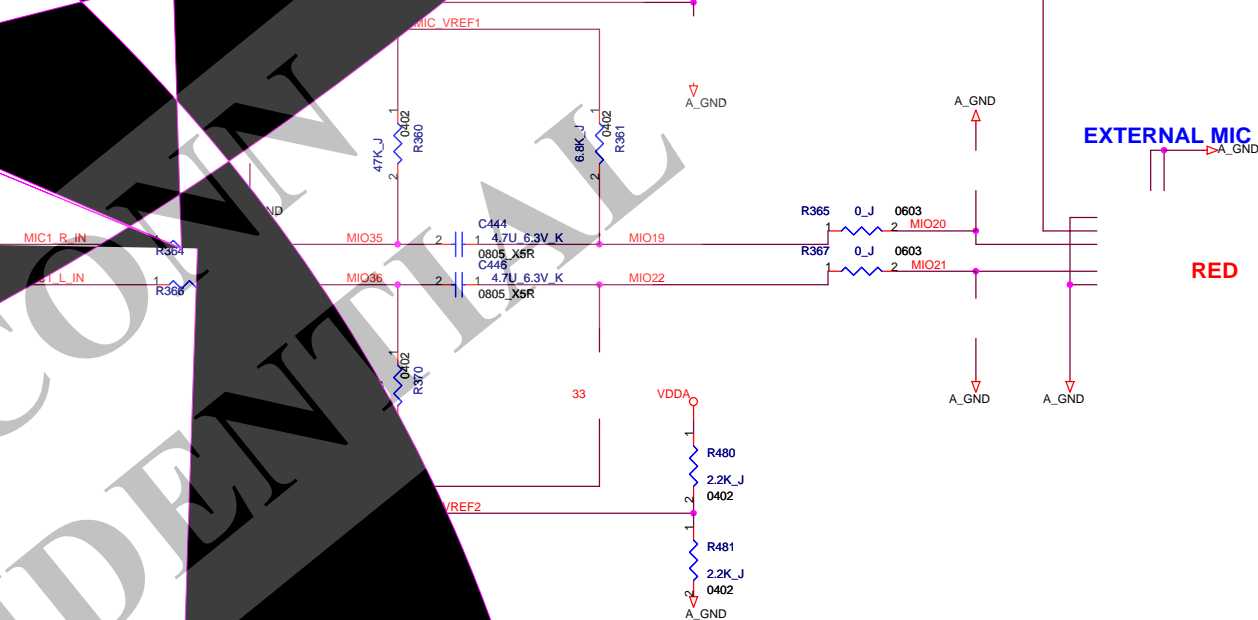
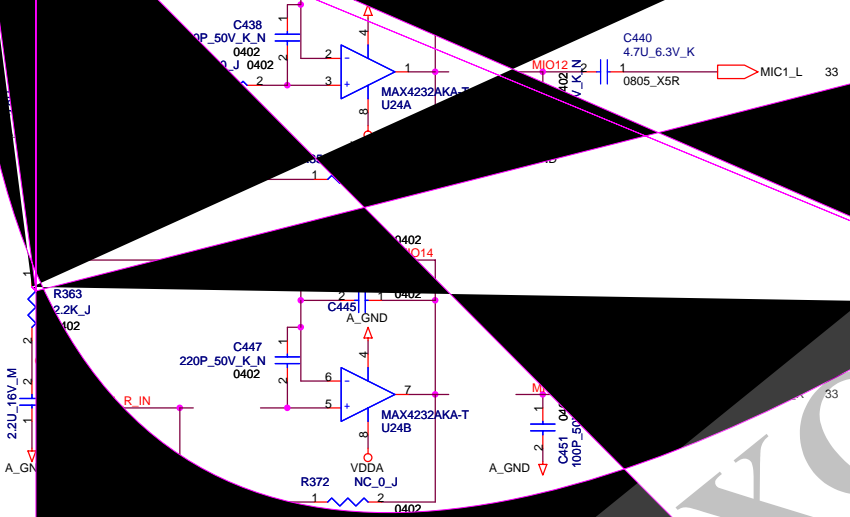




Max 1.5A

INTERNAL SPEAKER

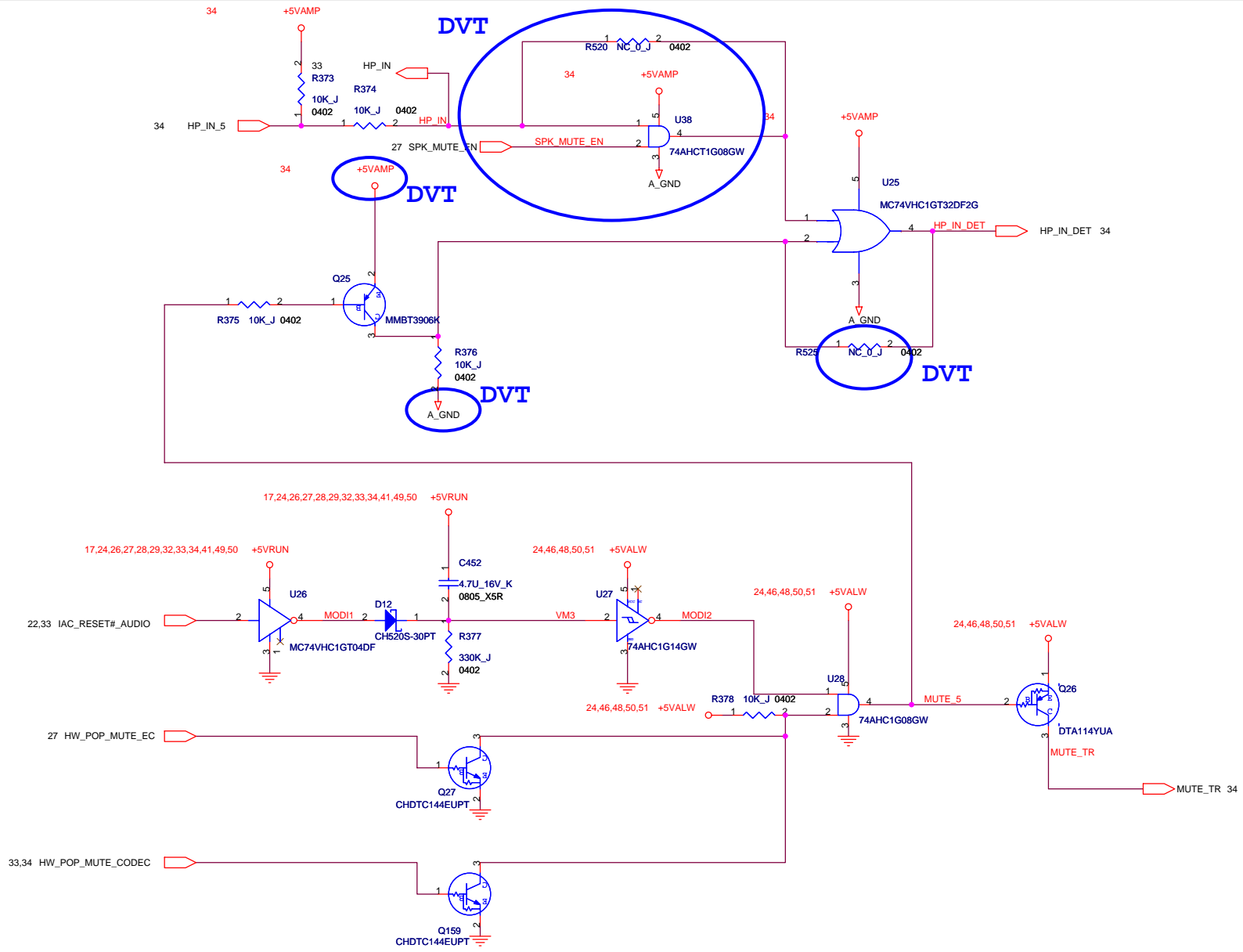




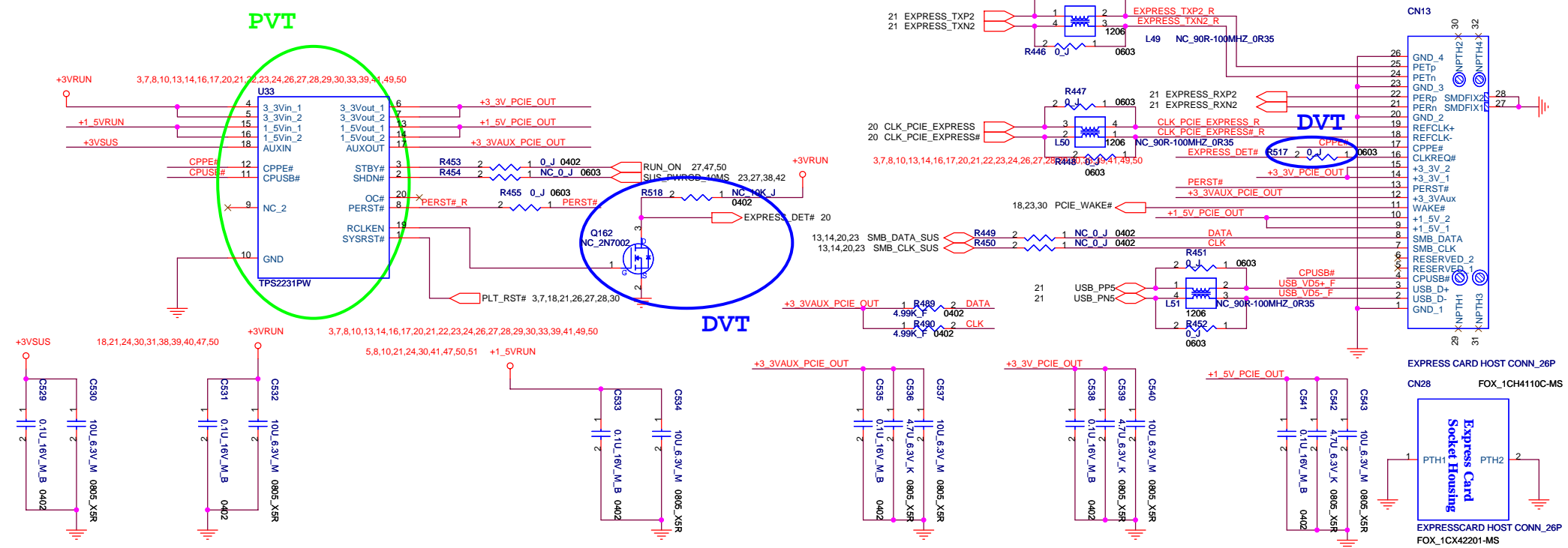
FOXCONN
CONFIDENTIAL



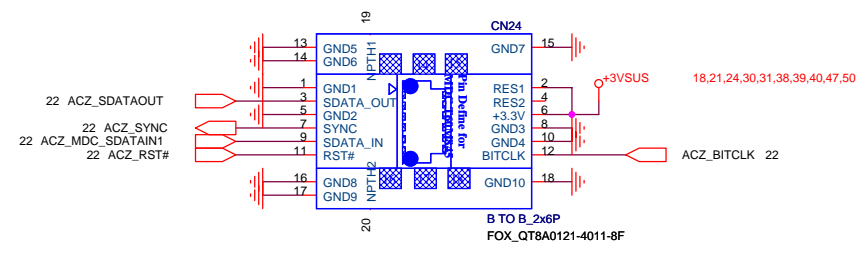
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title AUDIO(EXT MIC) 3/4			
Size A3	Document Number MS70-1-01	Rev 2.0	
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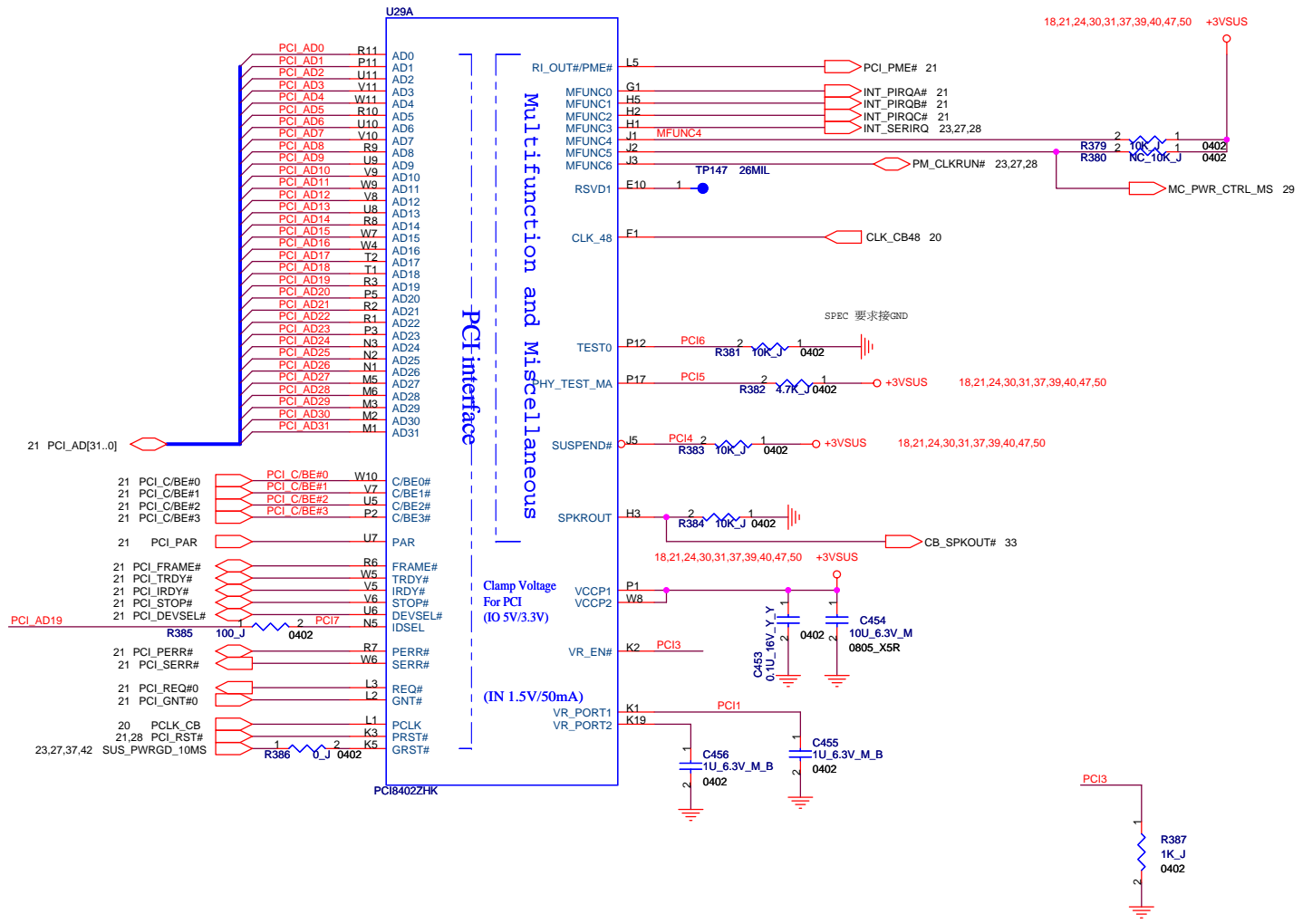


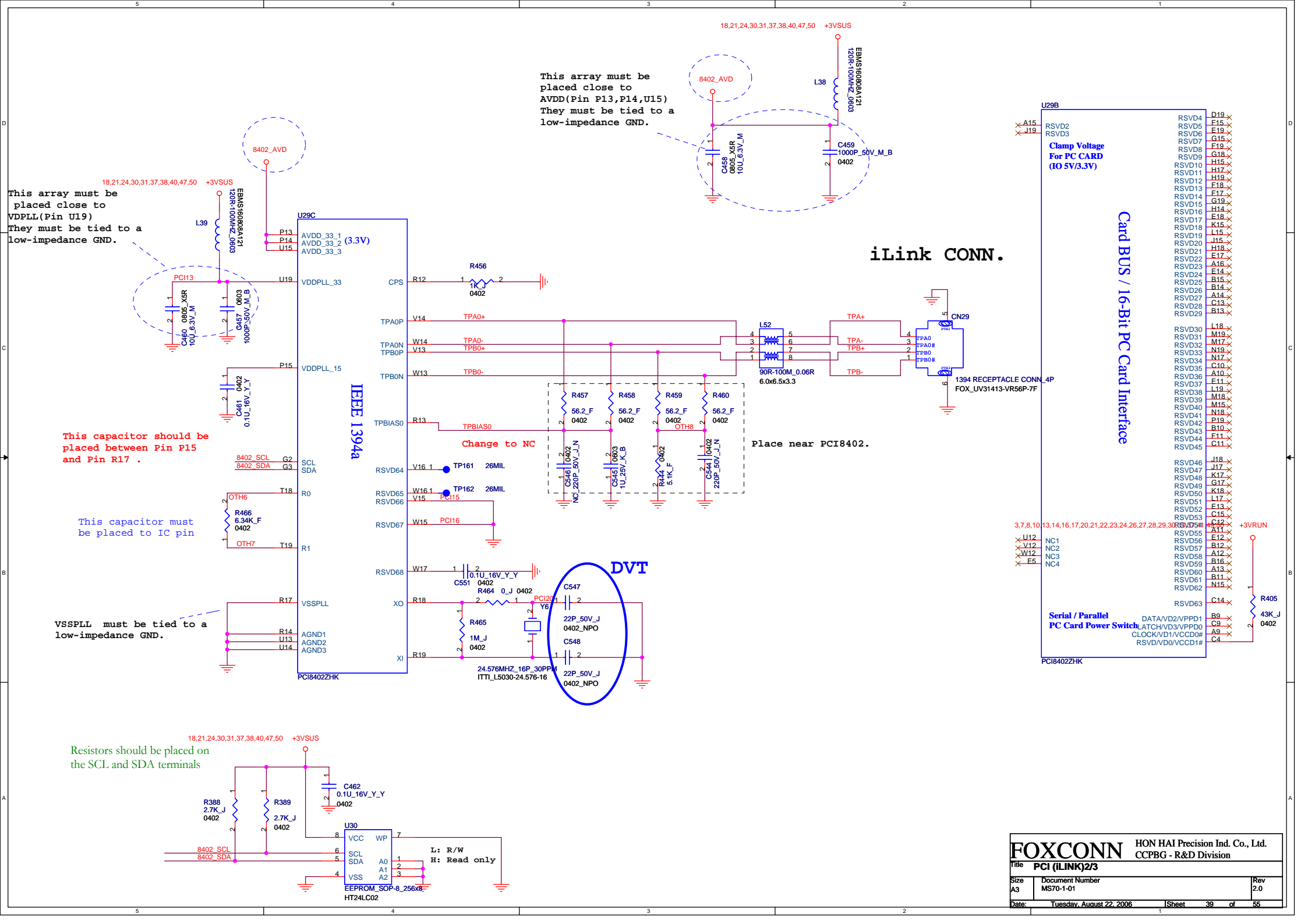
EXPRESS CONN



MDC CONN.







This array must be placed close to AVDD (Pin P13, P14, U15) They must be tied to a low-impedance GND.

This array must be placed close to VDDPLL (Pin U19) They must be tied to a low-impedance GND.

This capacitor should be placed between Pin P15 and Pin R17 .

This capacitor must be placed to IC pin

VSSPLL must be tied to a low-impedance GND.

Resistors should be placed on the SCL and SDA terminals

iLink CONN.

Place near PCI8402.

Clamp Voltage For PC CARD (IO 5V/3.3V)

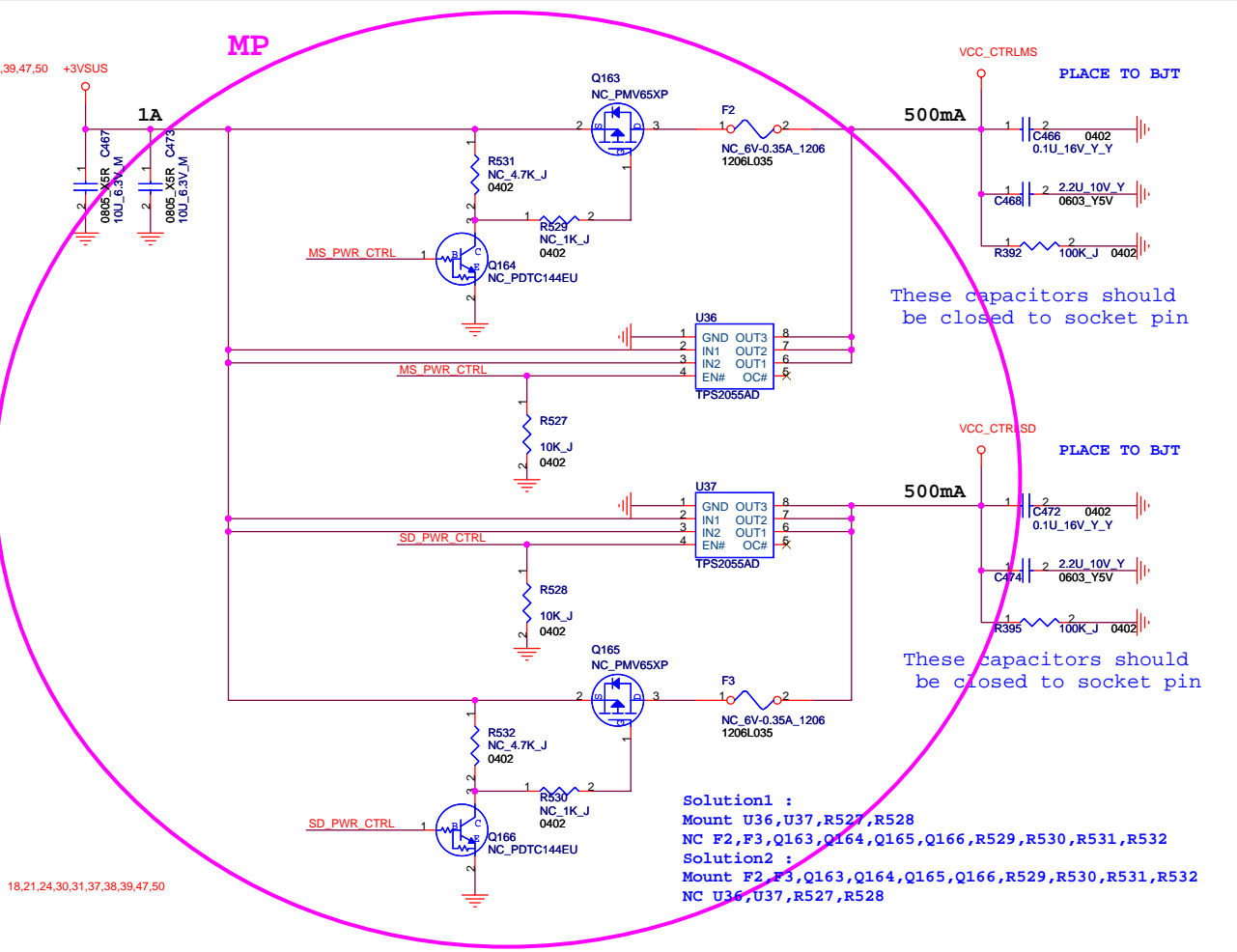
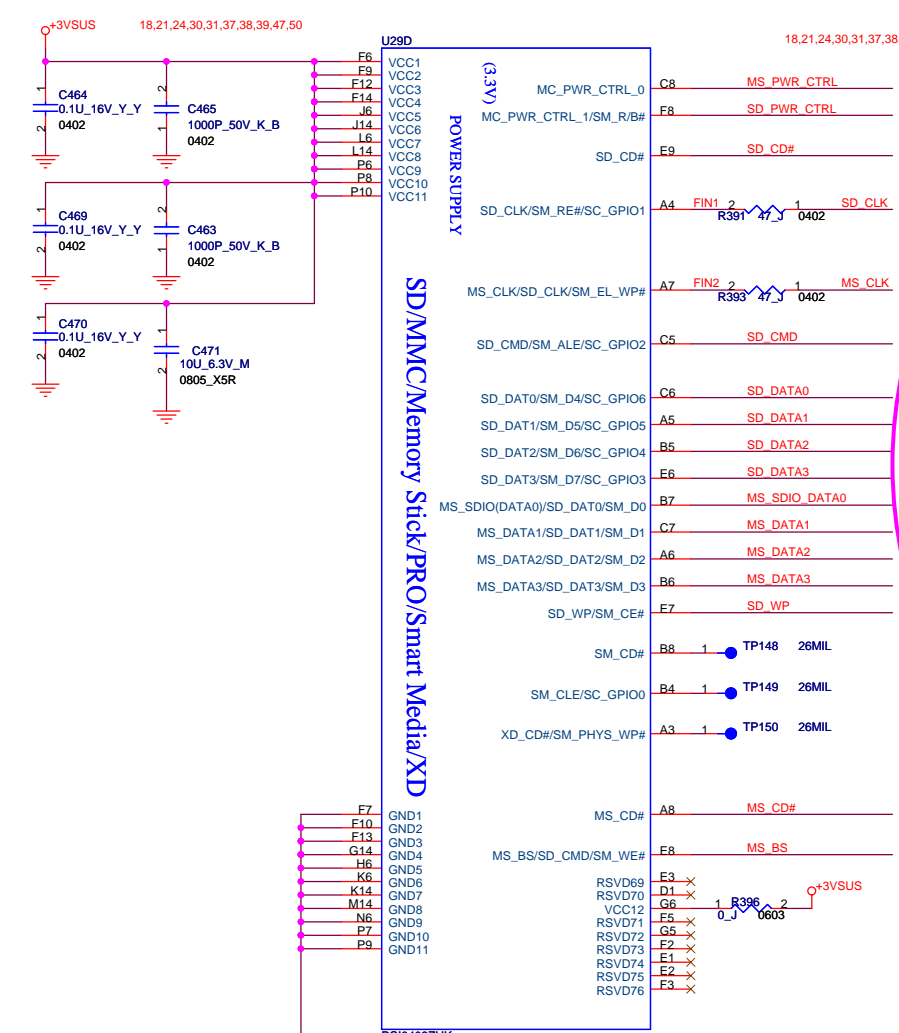
Card BUS / 16-Bit PC Card Interface

Serial / Parallel PC Card Power Switch

FOXCONN HON HAI Precision Ind. Co., Ltd.
CCPBG - R&D Division

Title: **PCI (iLINK)2/3**

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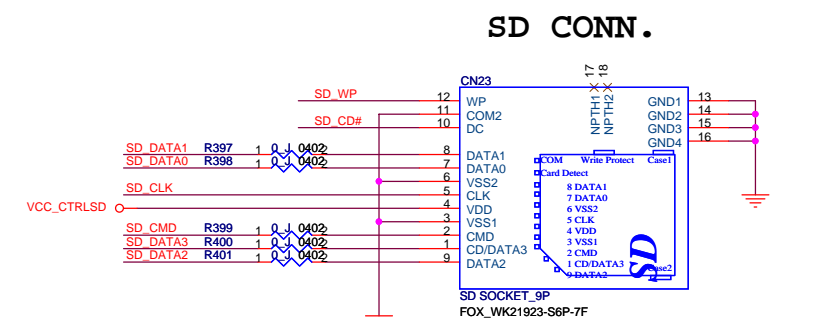
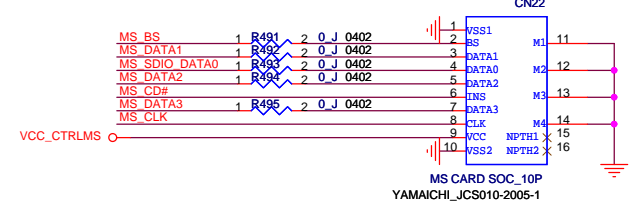
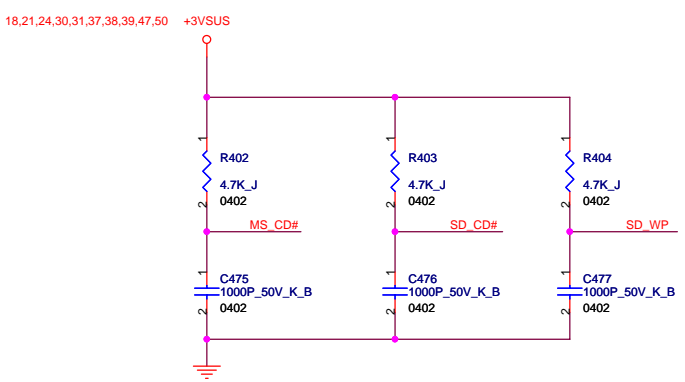


These capacitors should be closed to socket pin

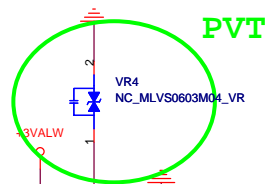
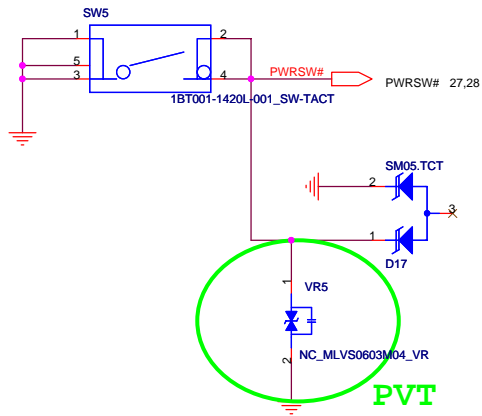
These capacitors should be closed to socket pin

Solution1 :
Mount U36, U37, R527, R528
NC F2, F3, Q163, Q164, Q165, Q166, R529, R530, R531, R532
Solution2 :
Mount F2, F3, Q163, Q164, Q165, Q166, R529, R530, R531, R532
NC U36, U37, R527, R528

MS STD/DUO CONN.

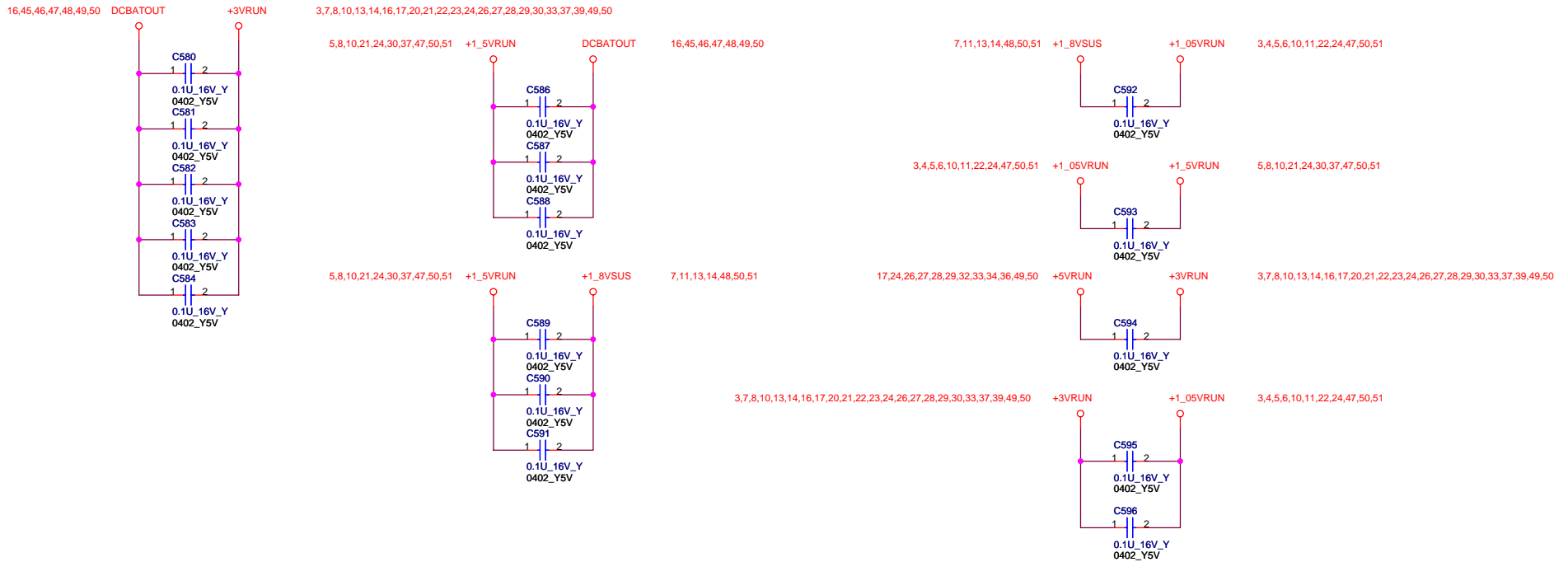


POWER BUTTON



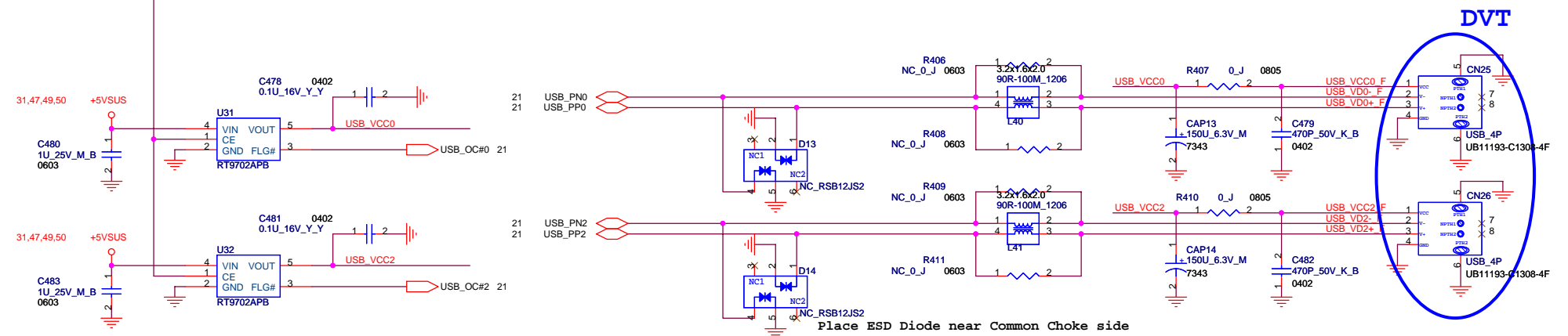
LID Switch

EMI CAP

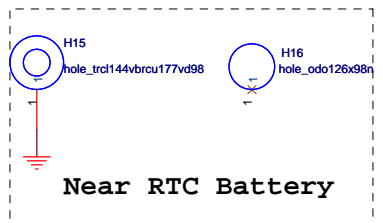
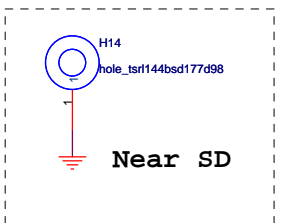
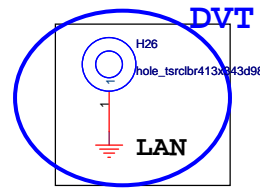
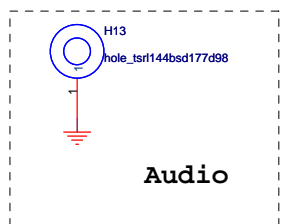
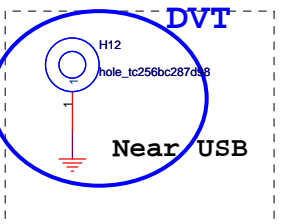
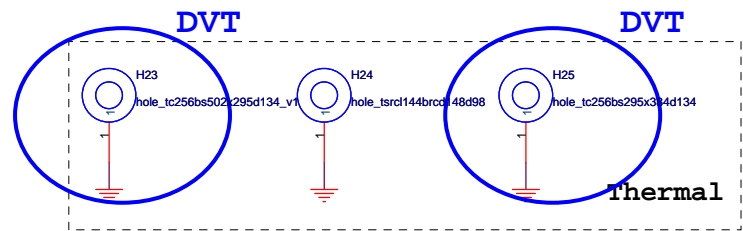
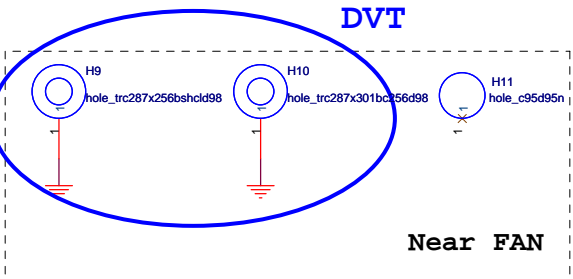
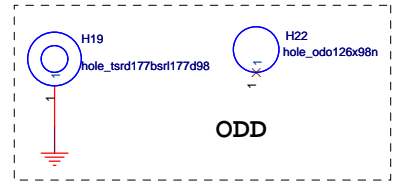
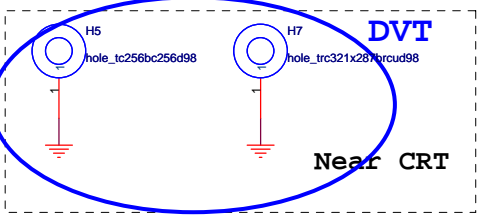
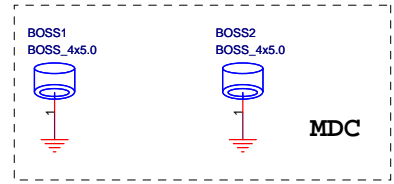
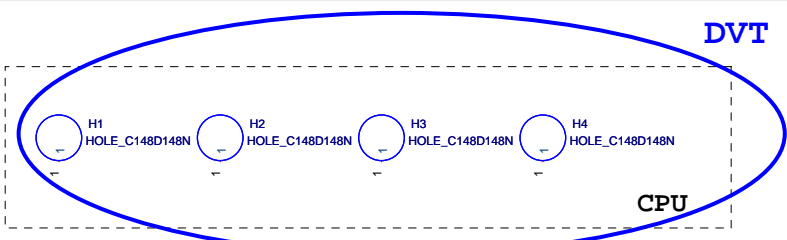


USB CONN X 2

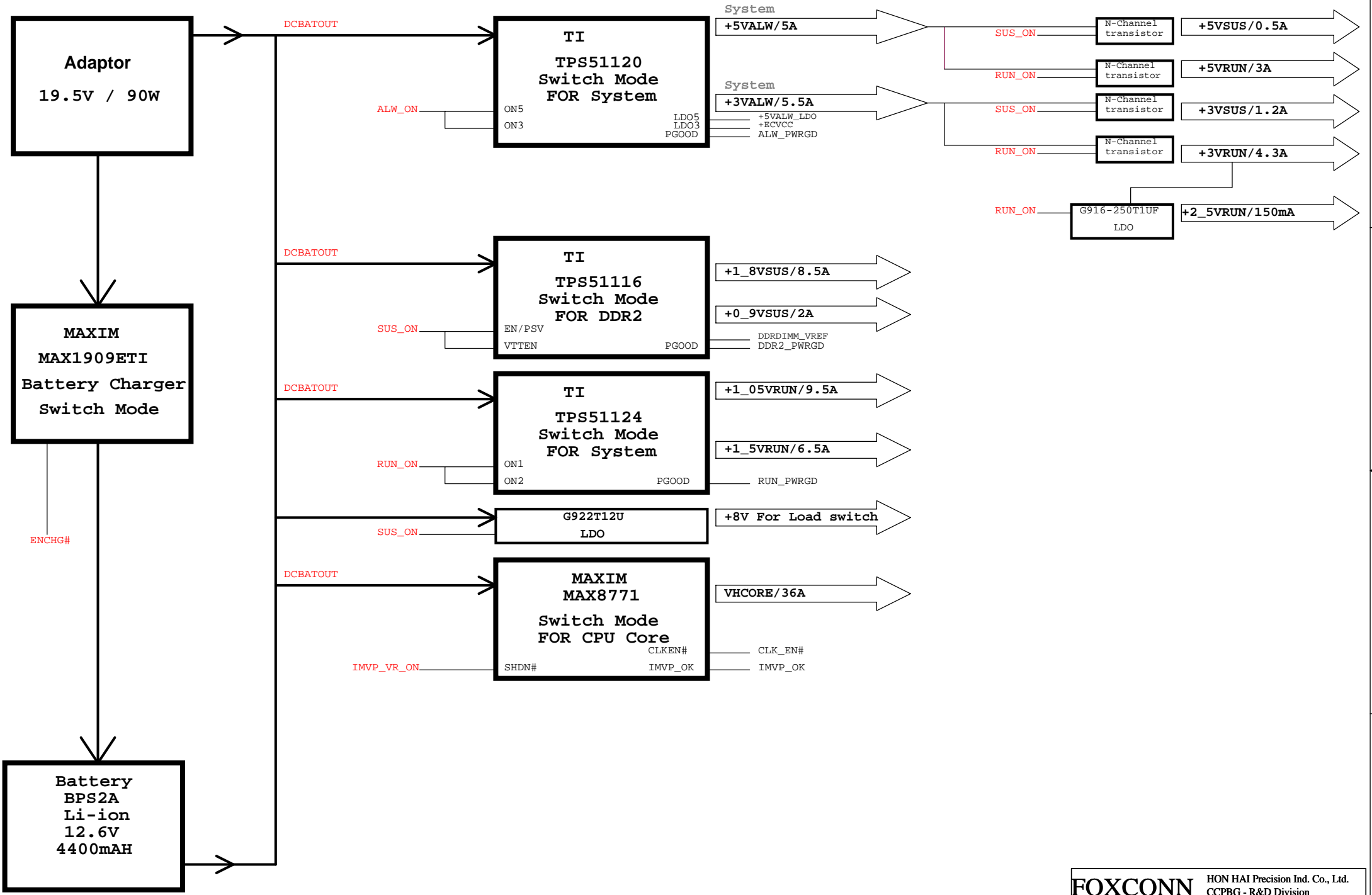
23,27,37,38 SUS_PWRGD_10MS

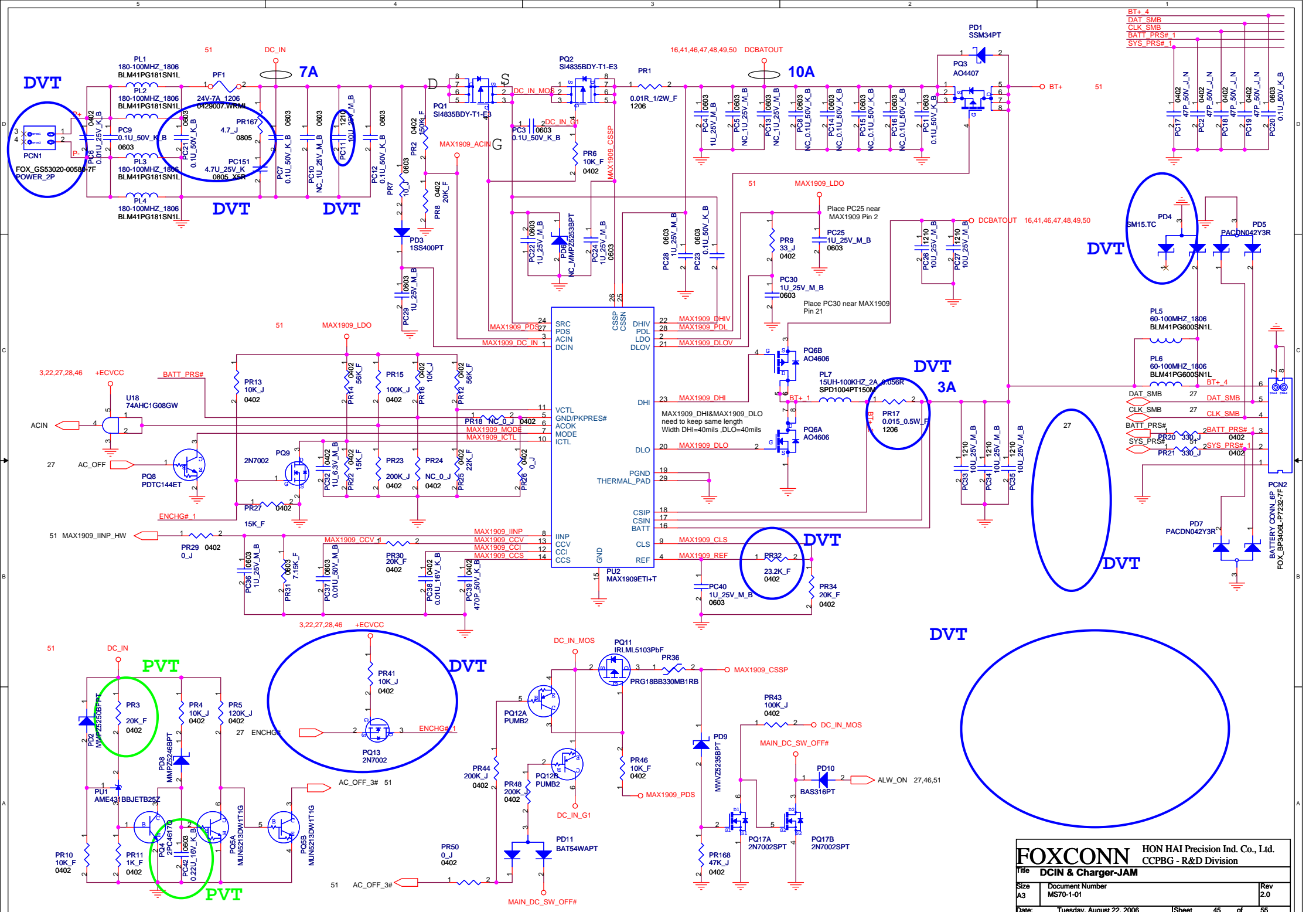


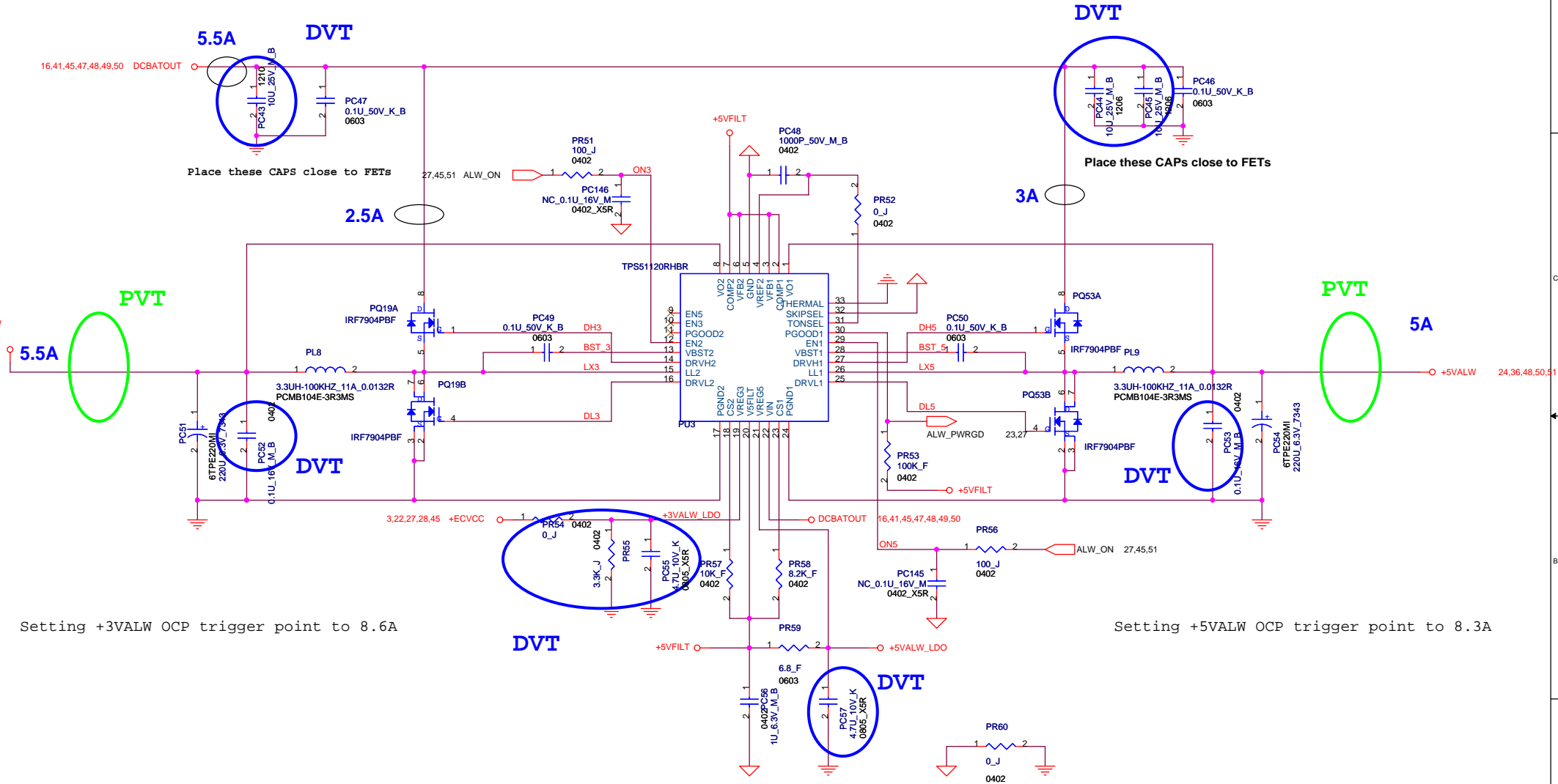
Place ESD Diode near Common Choke side

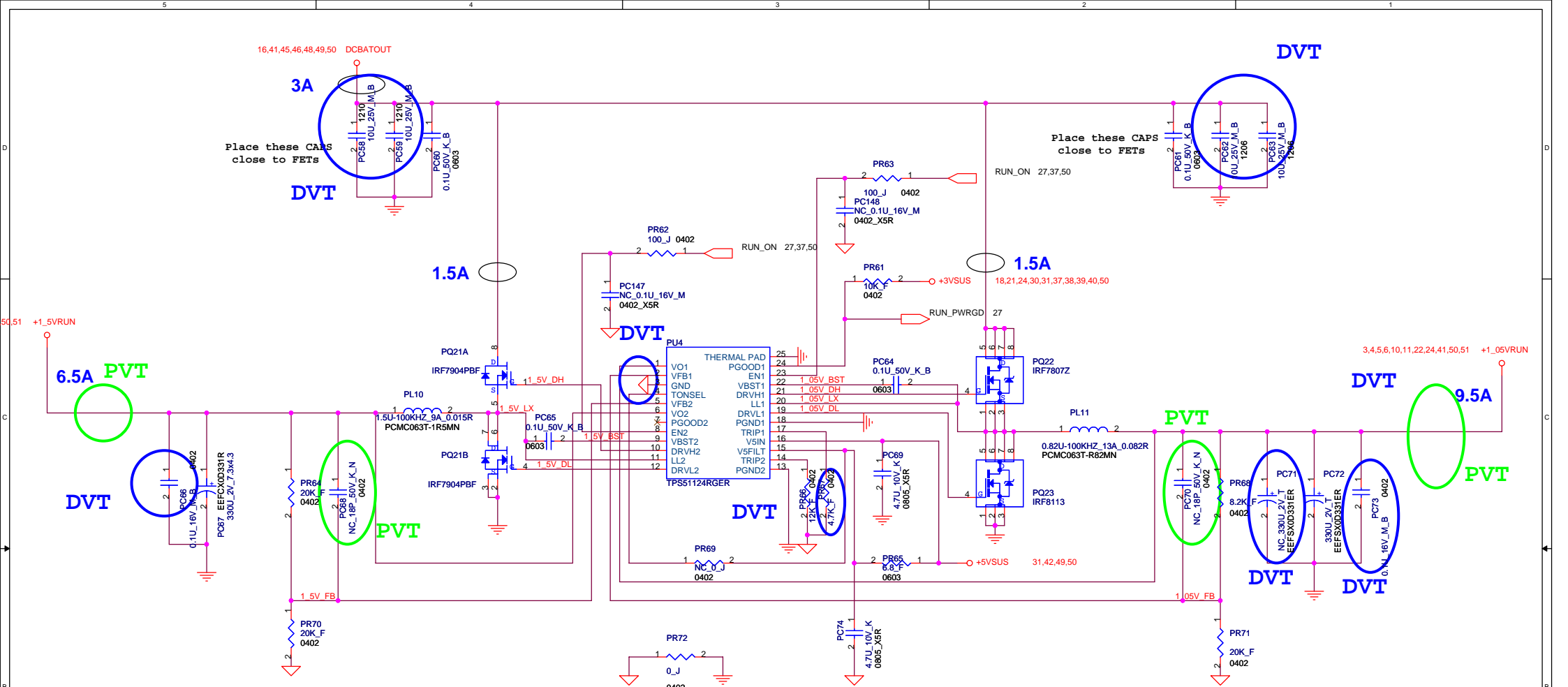


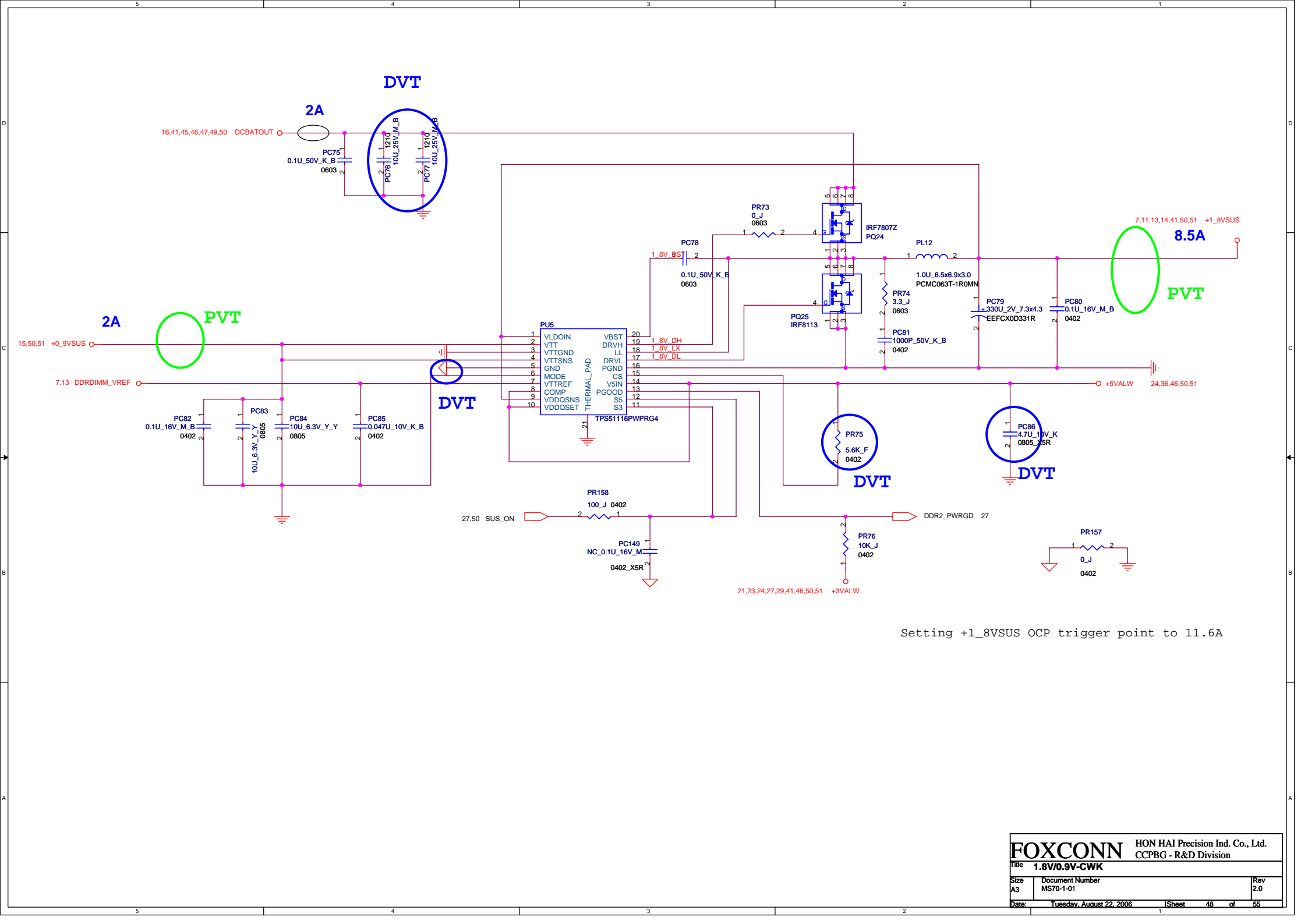
FOXCONN			HON HAI Precision Ind. Co., Ltd.		
Title HOLE			CCPBG - R&D Division		
Size A3	Document Number MS70-1-01			Rev 2.0	
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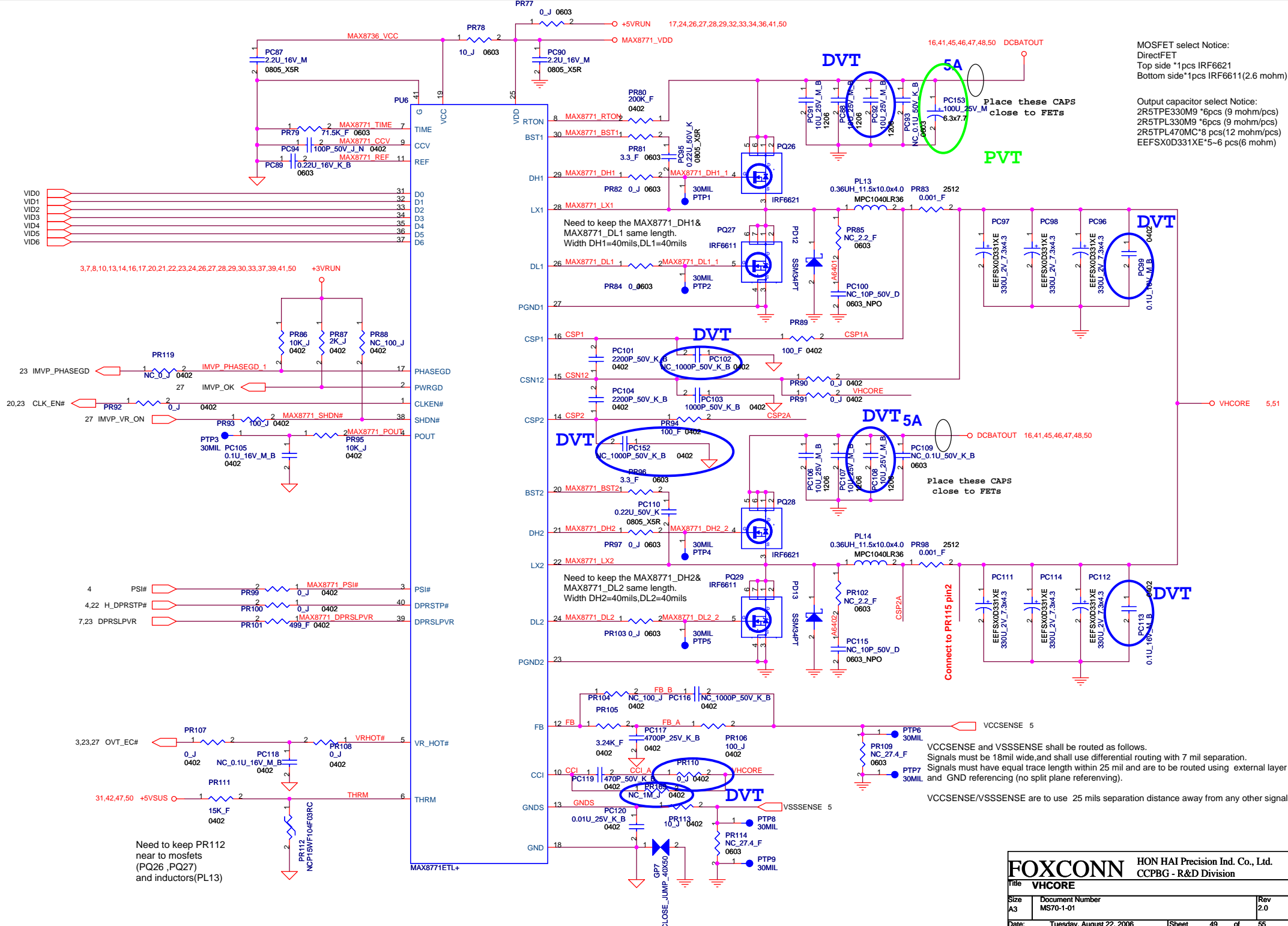








Setting +1_8VSUS OCP trigger point to 11.6A



MOSFET select Notice:
 DirectFET
 Top side *1pcs IRF6621
 Bottom side*1pcs IRF6611(2.6 mohm)

Output capacitor select Notice:
 2R5TPE330M9 *6pcs (9 mohm/pcs)
 2R5TPL330M9 *6pcs (9 mohm/pcs)
 2R5TPL470MC *8 pcs(12 mohm/pcs)
 EEFSXOD331XE*5-6 pcs(6 mohm)

Place these CAPS close to FETs

PVT

DVT

DVT

DVT 5A

Place these CAPS close to FETs

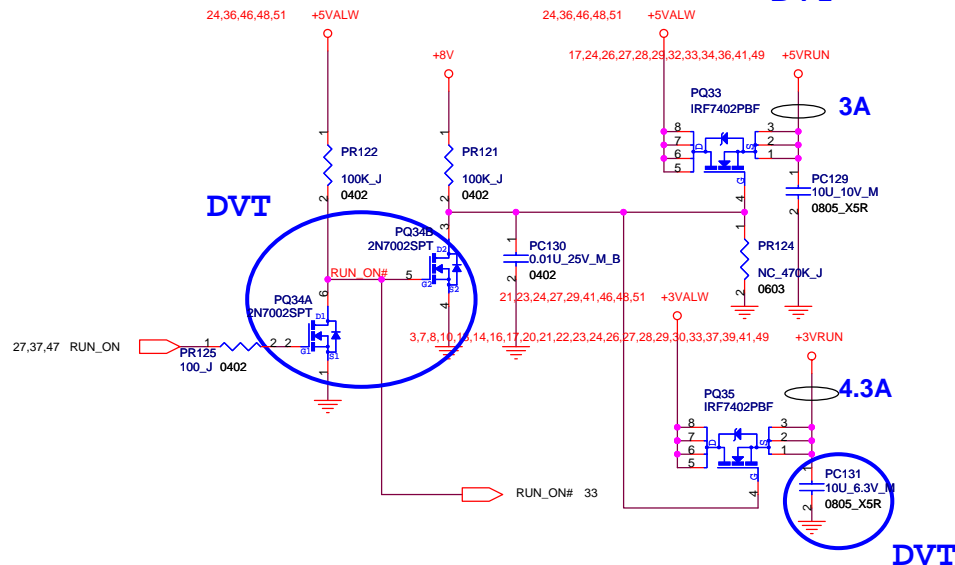
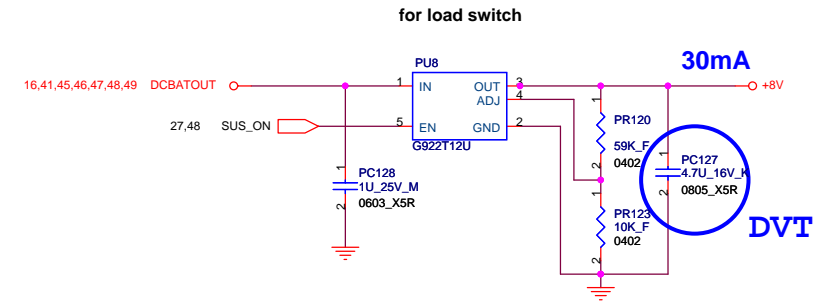
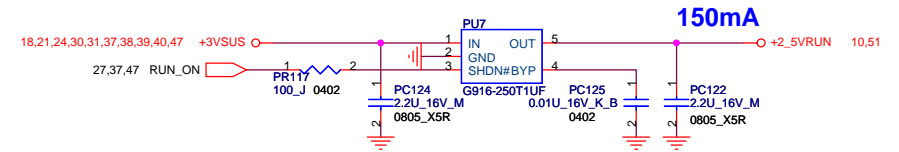
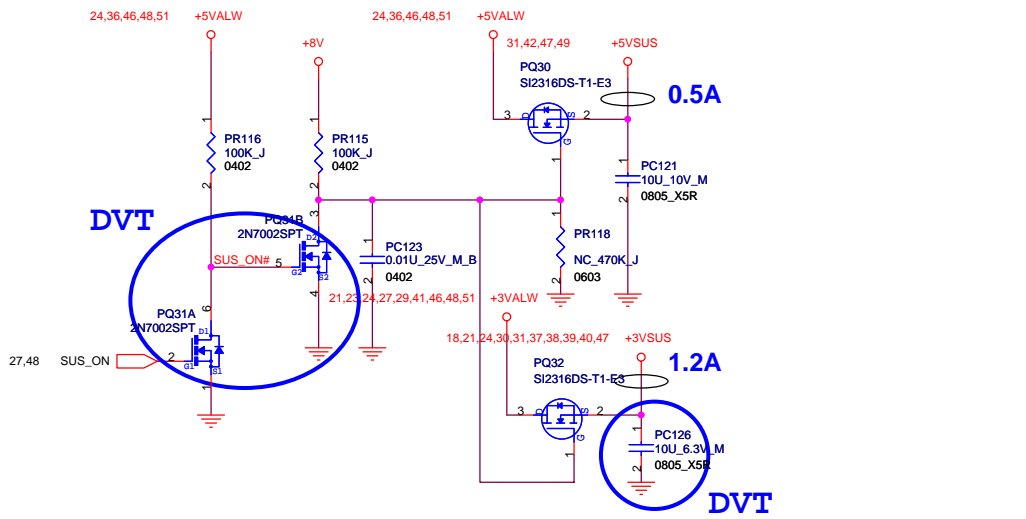
DVT

VCCSENSE and VSSSENSE shall be routed as follows.
 Signals must be 18mil wide, and shall use differential routing with 7 mil separation.
 Signals must have equal trace length within 25 mil and are to be routed using external layer and GND referencing (no split plane referencing).

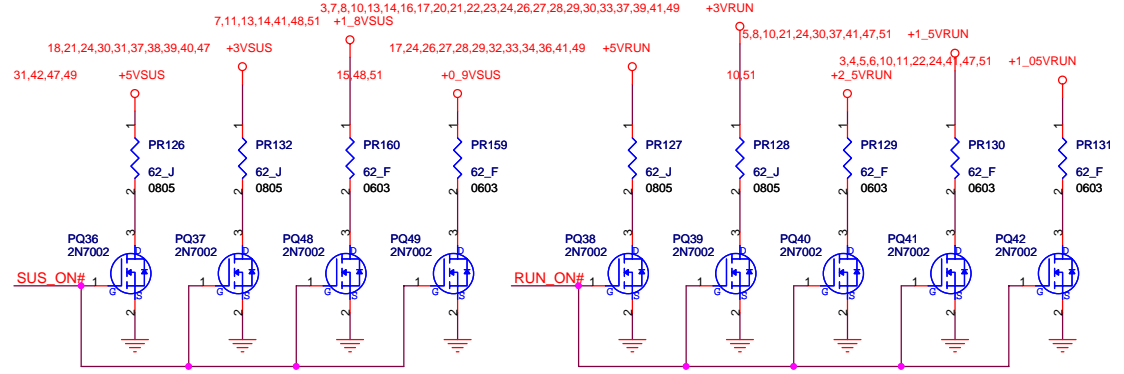
VCCSENSE/VSSSENSE are to use 25 mils separation distance away from any other signals.

Need to keep PR112 near to mosfets (PQ26, PQ27) and inductors(PL13)

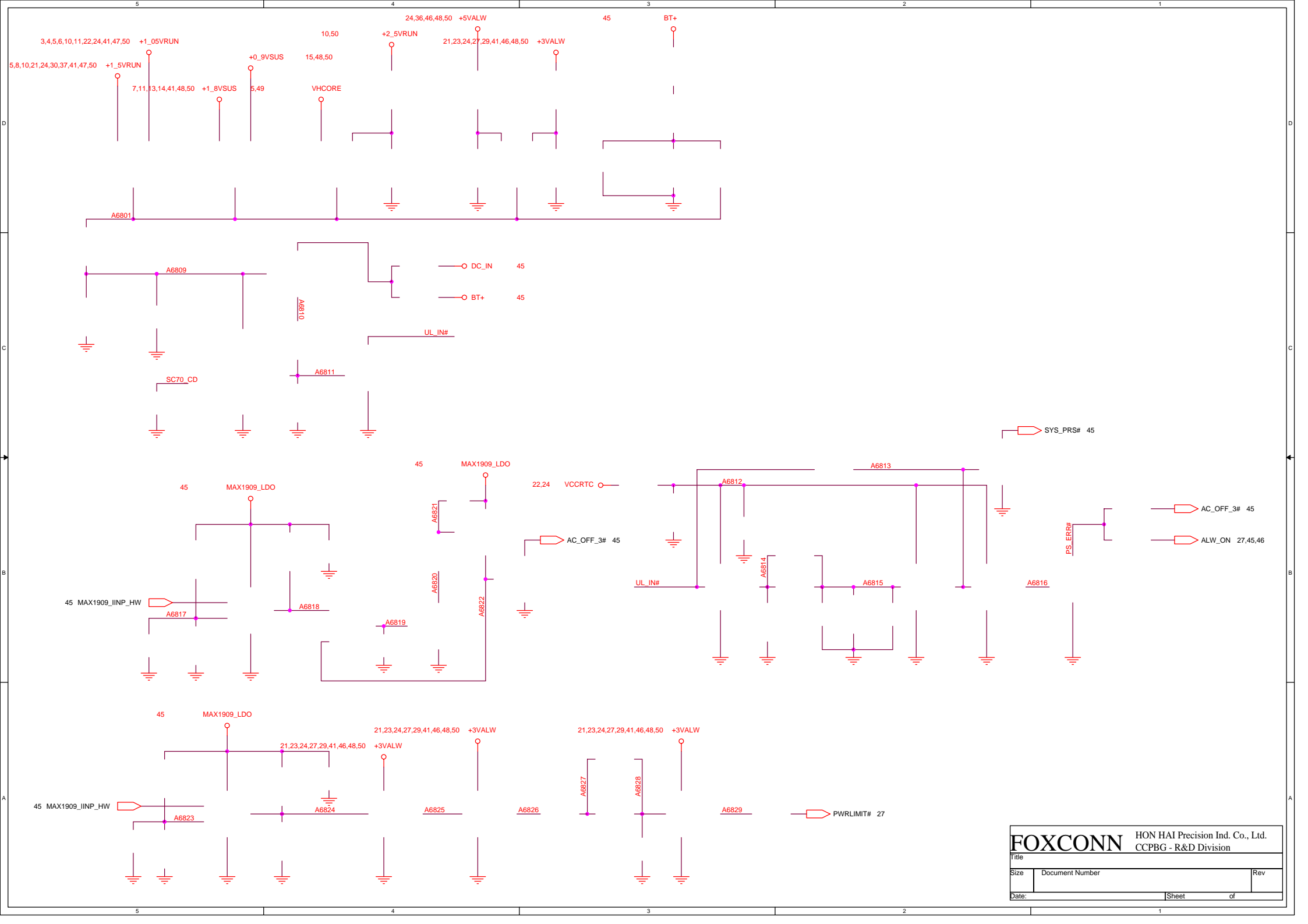
FOXCONN		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title VHOCORE			
Size A3	Document Number MS70-1-01	Rev 2.0	
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Discharge circuit for power-off



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		CCPBG - R&D Division	
Title Other power plan-ZG			
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HISTORY (1)

(2006/04/25)

P.16 CN3 pin5 Add R515 0ohm for QDI LCD Panel doesn't support gamma correction issue.
P.17 Add VGA_CRT_DET# connect to U15 pin29 for Semi-PnP function fail issue.
P.20 U11 pin57 add R516 10Kohm pull down for LAN can't be recognized issue.
P.27 U15 pin29 add R513 10Kohm pull up for Semi-PnP function fail issue.
P.27 U15 pin12 add R514 100Kohm pull down for EC hardware strap pin.
P.27 U15 pin171 add C597 1000pF to ground for FAN can't be controlled issue.
P.31 R304 change from 4.7k to 10k for FAN can't be controlled issue.

(2006/05/03)

P.49 Add netname(IMVP_PHASEGD_1) on the right side of PR119 for application modification.
P.45 PC11, PC21, PC151, PR167 change from DNI to mount for DC_IN spike issue
P.45 PD4 pin1 and pin3 exchange for application modification
P.46 PR54 change from 100 ohm to 0 ohm for PU3 output abnormal issue
P.46 PR55 change from DNI to mount for can't boot up issue
P.47 PU4 pin3 change from GND to GND_SIGNAL_1D5V for application modification
P.48 PU5 pin5 change from GND to GND_SIGNAL_1D8V for application modification
P.49 Add PR169 NC_1M ohm for MAX8771 CCI issue
P.49 PC96, PC97, PC98, PC111, PC112, PC114 change from SANYO 2R5TPL330M9 to Panasonic EEPFSX0D331XE for purchase difficult

(2006/05/04)

P.37 Add Q162(NC), R517, R518(NC) for Express card power sequence issue

(2006/05/15)

P.45 PR32 change from 22K_F to 23.2K_F for ACIN Vcls function trigger point correct to 3.4A
P.47 PR67 change from 8.2K_F to 4.7K_F for +1_05VRUN OCP trigger point correct to 12.8A
P.48 PR75 change from 6.8K_F to 5.6K_F for +1_8VSUS OCP trigger point correct to 11.6A
P.51 PR146 change from 51K_F to 46.4K_F for DCBATOUT OCP trigger point correct to 4.2A
P.51 PR150 change from 62K_F to 56K for PWRLIMIT# function trigger point correct to 3.6A
P.46 Delete PJ1, PJ2
P.47 Delete PJ3, PJ4, PJ5, PJ6
P.48 Delete PJ7, PJ8, PJ9

(2006/05/17)

P.45 Add PR41 10K_J_0402 and PQ13 2N7002 for preventing leakage current
P.45 PR17 change from 0.015_J 0805 to 0.015_F 1206 for application modification
P.46 PR55 change from 1K_J to 3.3K_J and PC55, PC57 change from 10u_25V X5R 1206 to 4.7u_10V X5R 0805 for reducing +ECVCC static current
P.47 PC71 change from mount to DNI for application modification
P.49 PR110 change from 20K_J to 0_J and PC102 change from DNI to mount for MAX8771 CCI issue
P.45 Delete PR19, PR28, PR33, PR35, PR37, PR38, PR39, PR40, PC31, PQ7, PQ10, PQ14, PQ16 For +ECVCC needed to work in battery only mode
P.51 Delete PD36, PD37 for +ECVCC needed to work in battery only mode
P.51 The net of VSOURCE (PQ43 pin3) change to DCBATOUT for +ECVCC needed to work in battery only mode
P.51 The net of BATT_EN (PD38 pin2) change to ALW_ON for +ECVCC needed to work in battery only mode

(2006/05/19)

P.13 C155 change from 2.2U_10V_Y_Y to 1000P_16V_K ; C159 change from 0.1U_16V_Y_Y to 1000P_50V_K for EMC DDR2 solution
P.14 C168 change from 2.2U_10V_Y_Y to 1000P_16V_K ; C172 change from 0.1U_16V_Y_Y to 1000P_50V_K for EMC DDR2 solution
P.15 C177,C179,C181,C191,C192,C196 change from 0.1U_16V_Y_Y to 1000P_50V_K for EMC DDR2 solution
P.39 C547,C548 change from 18P_50V_J_N to 22P_50V_J for PCI8402's Crystal issue
P.30 LED1 change from HT-110Y to HT-110UYG for LED color requirement
P.45 PCN1 change from MOLEX_53259-0229 to FOX_GS53020-00580-7F
P.45 PC11 change from 10U_25V_M_1206 to 10U_25V_M_B_1210 for purchase convenient
P.46 PC43,PC44,PC45 change from 10U_25V_M_B_1206 to 10U_25V_M_B_1210 for purchase convenient
P.47 PC58,PC59,PC62,PC63 change from 10U_25V_M_B_1206 to 10U_25V_M_B_1210 for purchase convenient
P.48 PC76,PC77 change from 10U_25V_M_B_1206 to 10U_25V_M_B_1210 for purchase convenient
P.48 PC86 change from 4.7U_10V_K_B_1206 to 4.7U_10V_K_0805 for purchase convenient
P.50 PC126,PC131 change from 10U_10V_M to 10U_6.3V_M for purchase convenient
P.50 PC127 change from 4.7U_25V_K_B_1206 to 4.7U_16V_K_0805 for purchase convenient

(2006/05/22)

P.32 CN21 change from FOXCONN_GB11060_0221_7F to FOXCONN_GB5RF060_1200_7F for ME's requirement
P.29 CN30,CN31 change from foxconn_gb11120_0221_7F to FOXCONN_GB5RF120_1200_7F for ME's requirement
P.29 CN31 change from mount to DNI for ME's requirement
P.50 PQ31,PQ34 change from DIODES,2N7002DW-7-F to CHENMKO,2N7002SPT for purchase convenient
P.51 PQ45 change from DIODES,2N7002DW-7-F to CHENMKO,2N7002SPT for purchase convenient
P.27 Q149 change from DIODES,2N7002DW-7-F to CHENMKO,2N7002SPT for purchase convenient

(2006/05/23)

P.47 PC62,PC63 change from 10U_25V_M_B_1210 to 10U_25V_M_B_1206 for ME limit of height
P.46 PC44,PC45 change from 10U_25V_M_B_1210 to 10U_25V_M_B_1206 for ME limit of height
P.46 Add PJ1,PJ2 for test request
P.47 Add PJ3,PJ4 for test request
P.48 Add PJ7,PJ9 for test request

(2006/05/24)

P.42 CN25,CN26(USB CONN) change from FOX_UB11193_C1301_4F to UB11193-C1308-4F for ME's requirement
P.17 CN5(VGA CONN) change from FOX_DZ11A91_MB221_4F to DZ11A91-MW223-4F for ME's requirement

(2006/05/25)

P.47 Add PJ6 for test request
P.26 CN8 footprint change from FOXCONN_LD2722H_S469 to FOXCONN_LD2722H_S469_MS70 for ME PAD request
P.32 C389 change from 22U_10V_Y_Y_1206 to 10U_10V_M_0805 and add C598 10U_10V_M_0805 for limit of ME
P.43 H1,H2,H3,H4 change from hole_c158d158n to HOLE_C148D148N for ME request
P.43 H7 change from hole_tsru144bsru177d98 to hole_trc321x287brud98 for ME request
P.43 H26 change from hole_c120d100 to hole_tsrlbr413x343d98 for ME request
P.43 H23 change from hole_tc256brcl295d98_v1 to hole_tc256bs502x295d134_v1 for ME request
P.43 H25 change from hole_tc256brcl48d98 to hole_tc256bs295x384d134 for ME request
P.43 H5 change from hole_tc256bc315d98 to hole_tc256bc256d98 for ME request
P.43 H10 change from hole_tshrd144bc315d98 to hole_trc287x301bc256d98 for ME request
P.43 H9 change from hole_trcd144brcl177d98 to hole_trc287x321brcd98 for ME request
P.43 H12 change from hole_tc256bsrcu144d98 to hole_tc256bc287d98 for ME request

(2006/05/26)

P.42 CN25,CN26 change from FOXCONN_UB11193_C1308_4F to FOXCONN_UB11193_C1308_4F_HM for solder issue
P.43 H9 change from hole_trc287x321brcd98 to hole_trc287x256bshcl98 for ME request
P.17 D3 change from 16-CH500H4-0P00 to 16-SCS500V-4000 for purchase convenient
P.10 C119 change from 1C-2B30105-K000 to 1C-2B30475-K100 ; C120 change from 1C-2B20103-K001(0402) to 1C-2B30475-K100(0603) for +1_5VRUN_HMPLL noise issue
P.48 Add PJ8 for test request

(2006/06/01)

P.16 Add R519(0ohm 0402) for desinger set "LCDID3" to "0" by mistake.
P.49 PC102 change from mount to NC for application modification
P.46 PC52,PC53 change from 0.1U_16V_Y_Y(Y5V) to 0.1U_16V_M_B(X5R) for application modification
P.47 PC66,PC73 change from 0.1U_16V_Y_Y(Y5V) to 0.1U_16V_M_B(X5R) for application modification
P.49 PC99,PC113 change from 0.1U_16V_Y_Y(Y5V) to 0.1U_16V_M_B(X5R) for application modification
P.36 Q25 pin2 netname change from +5VRUN to +5VAMP
P.36 R376 pin2 netname change from GND to A_GND
P.36 Add U38,R520(NC) for SPK_MUTE_EN for Vista requirement
P.36 Add NET "SPK_MUTE_EN" from U38 pin2 to U15 pin99 for Vista requirement
P.40 Change U36,U37 from RT9702 to RT9703, Add R521-R524.
P.27 Delete Q149.

(2006/06/02)

P.16 R515,R519 change from mount to NC
P.36 Add R525(NC) for Audio mute option
P.49 Add PC152 for application modification
P.26 R510 change from mount to NC for application modification
P.22 R188 change from mount to NC for application modification

(2006/06/05)

P.49 PC92,PC108 change from NC to mount for design rating
P.40 U36,U37 change from RT9703 to RT9702, Del R521-R524 for RT9703 phase out issue
P.49 Add PC153 for solving audible noise
P.19 Add R526 for LAN application modification

(2006/06/06)

P.13 Add C599,C600(1000P_50V_K) ; C155 change from 1000P_16V_K to 2.2U_10V_Y_Y ; C159 change from 1000P_50V_K to 0.1U_16V_Y_Y for EMC solution
P.14 Add C601,C602(1000P_50V_K) ; C168 change from 1000P_16V_K to 2.2U_10V_Y_Y ; C172 change from 1000P_50V_K to 0.1U_16V_Y_Y for EMC solution
P.15 Add C603,C604(1000P_50V_K) ; C177,C179,C181,C191,C192,C196 change from 1000P_50V_K to 0.1U_16V_Y_Y for EMC solution
P.51 Add PD36,PD37 for application modification
P.19 C253 change form 0.1U_16V_M_B to 5P_50V_C ; C254 change from 5P_50V_C to 0.1U_16V_M_B ; Add L58 ; Del R526 for LAN application modification

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HISTORY (2)

(2006/06/07)

P.26 R245 change from NC to mount for application modification

(2006/06/13)

P.33 R325 change from mount to NC for acoustic noise.

P.36 U38 change from 74AHCT1G08GW to 74AHCT1G08GW for Vih can't meet EC spec.

PVT

(2006/07/12)

P.47 Change PC68, PC70 from mount to NC for TPS51124 OVP issue.

P.27 Add R526 (1K ohm) series on ALW_ON net to prevent EC damage issue.

P.46 Delete PJ1, PJ2

P.47 Delete PJ3, PJ4, PJ6

P.48 Delete PJ7, PJ8, PJ9

P.32 F1,R320,R321,L32,C598,C389,C390,C391,CN21 change from mount to NC for cancel Oide function

P.37 U33 change from 15-TPS2231-0000(24pin) to 15-TPS2231-0002(20pin) for purchase convenient

P.40 U36,U37 change from 15-RT9702A-0000 to 15-TPS2055-0000 ;

Add R527,R528 for MS_PWR_CTRL and SD_PWR_CTRL are recognized to be high level by accident

(2006/07/20)

P.26 CN9 vendor part number change from QT8H0506-13T3R-7F to QT8H0506-13T3R-4F for packing type change.

P.49 PC153 change from 1C-10X0107-M403 to 1C-1XX0107-M400 for purchase convenient.

P.29 Delete CN31 for touch pad application modification.

P.22 R195 change from 47ohm to 0ohm ; C293 change from NC to mount for EMI solution.

P.29 LED6 change from 16-HT210DY-G000 to 16-HT210UD-UY00 for ME brightness issue.

LED5,LED7 change from 16-HT110Y0-0000 to 16-HT110UY-0000 for ME brightness issue.

(2006/07/21)

P.26 Add D22(NC) for ESD solution

P.30 R301 change from 120ohm to 47ohm for ME brightness issue

(2006/07/25)

P.30 C365 change from NC to mount for WLAN power ripple noise issue

P.26 Add VR1 for ESD solution

P.29 Add VR2,VR3(NC) for ESD solution

P.41 Add VR4,VR5(NC) for ESD solution

(2006/07/28)

P.29 Q155 change from 17-CHDTC14-4E01 to 17-2N70020-0000 for ME brightness issue.

(2006/07/31)

P.30 R301 change from 47ohm to 120ohm (LED1 is 10mA) for ME brightness issue

P.29 R418 change from 47ohm to 62ohm (LED5 is 18.75mA) for ME brightness issue

P.29 R424 change from 47ohm to 62ohm (LED6 is 19.5mA)

R425 change from 47ohm to 120ohm (LED6 is 10mA)for ME brightness issue

P.29 R426 change from 47ohm to 62ohm (LED7 is 18.9mA)

(2006/08/01)

P.31 Q17 change from 17-ME2301T-1000 to 17-S12301B-DS00 for Fan rotational speed issue

-----PVT schematic released

(2006/08/07)

P.45 PC42 change from 1C-2B30104-K000(0.1u) to 1C-2B30224-K000(0.22u) and mount PC42 for solving AC_OFF_3# abnormal issue

P.34 R350 change from 6.2kohm to 6.98kohm for adjust the gain of speaker amp

P.26 VR1 change from mount to NC ; D22 change from NC to mount for purchase convenient.

P.29 R418,R426 change from 62ohm to 120ohm for LED brightness issue

(2006/08/13)

P.45 PR3 change from 1kohm to 20kohm for power circuit design improvement plan which is DC_IN OVP circuit.

-----PVT SMT

MP

(2006/08/16)

P.23 Add D23 from IMVP_PWRGD to ALW_PWRGD for RTC stop issue backup (D23 is NC)

Add D24 from PM_RSMRST#(A3602) to ALW_PWRGD for RTC stop issue backup (D24 is NC)

(2006/08/17)

P.40 Add Q163,Q164,R529,F2(MS_PWR) for purchase convenient

Add Q165,Q166,R530,F3(SD_PWR) for purchase convenient

(2006/08/18)

P.40 R392,R395 change from 1Mohm to 100Kohm
F2,F3 move to pin3 side of Q163,Q165

P.40 Q163,Q165 change from PMBT2907A(PNP) to SI2301BDS-T1-E3(P-MOS)
R529,R530 change from 1.5kohm to 1kohm
Add R531,R532 4.7kohm

P.23 R221 change from 100ohm to 1kohm

D23,D24 change from BAS316PT to SCS500V-40-LF

D23,D24 change from NC to mount for RTC stop issue

(2006/08/23)

P.40 Q163,Q165 change from VISHAY_SI2301BDS-T1-E3 to Philips_PMV65XP for purchase convenient.

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