

**Schematics Page Index (Title / Revision / Change Date)**

Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Schematics Page Index	0.30	06/05	36	AUDIO (MUTE)	0.30	06/05
02	Block Diagram	0.30	06/05	37	EXPRESS CARD/MDC	0.30	06/05
03	Yonah(HOST BUS) 1/2	0.30	06/05	38	PCI (PCI BUS)	0.30	06/05
04	Yonah(HOST BUS) 2/3	0.30	06/05	39	PCI ( ILINK)	0.30	06/05
05	Yonah(Power/Gnd) 3/3	0.30	06/05	40	PCI (MS-DUO/MDC)	0.30	06/05
06	CALISTOGA (HOST) 1/7	0.30	06/05	41	Button/LID Switch/EMI CAP	0.30	06/05
07	CALISTOG (DMI) 2/7	0.30	06/05	42	USB2.0	0.30	06/05
08	CALIST (GRAPHIC) 3/7	0.30	06/05	43	HOLE	0.30	06/05
09	CALISTOGA (DDR2) 4/7	0.30	06/05	44	Power Design Diagram	0.30	06/05
10	CALIST (POWER,VCC) 5/7	0.30	06/05	45	DCIN&Charger	0.30	06/05
11	CALIST (VCC CORE) 6/7	0.30	06/05	46	SYS Power (+3_3V/+5V)	0.30	06/05
12	CALIST (VSS) 7/7	0.30	06/05	47	SYS Power(+1_5V/+1_05V)	0.30	06/05
13	DDR2(SO-DIMM_0) 1/3	0.30	06/05	48	DDR2 Power(+1_8V/+0_9V)	0.30	06/05
14	DDR2(SO-DIMM_1) 2/3	0.30	06/05	49	CPU_Vcore ---MAX8771	0.30	06/05
15	DDR2(Termination) 3/3	0.30	06/05	50	Others power plan	0.30	06/05
16	LVDS	0.30	06/05	51	OVP protection	0.30	06/05
17	CRT	0.30	06/05	52	History ( 1 )	0.30	06/05
18	LAN CONTROLL	0.30	06/05	53			
19	LAN TRANSFORMER	0.30	06/05	54			
20	CLOCK GEN	0.30	06/05	55			
21	ICH7-M( PCI/USB ) 1/5	0.30	06/05	56			
22	ICH7-M( LPC,IDE,SATA ) 2/5	0.30	06/05	57			
23	ICH7-M( GPIO) 3/5	0.30	06/05	58			
24	ICH7-M( POWER) 4/5	0.30	06/05	59			
25	ICH7-M( GND) 5/5	0.30	06/05	60			
26	SATA HDD/CD-ROM	0.30	06/05				
27	EC+KBC	0.30	06/05				
28	Flash ROM/X-Bus	0.30	06/05				
29	LED/Touch PAD	0.30	06/05				
30	Mini-PCIE Card	0.30	06/05				
31	FAN	0.30	06/05				
32	OIDE	0.30	06/05				
33	AUDIO(CODEC & POWER)	0.30	06/05				
34	AUDIO( AMP & HP & SPK)	0.30	06/05				
35	AUDIO( EXTMIC)	0.30	06/05				

P. Leader	Check by	Design by

**Project Code & Schematics Subject:** MS70 Main Board

**PCB P/N:** (FUBAI) 1P-0065100-60SB  
 (NAN YA) 1P-0065200-60SB  
 (HANSTAR) 1P-0065500-60SB

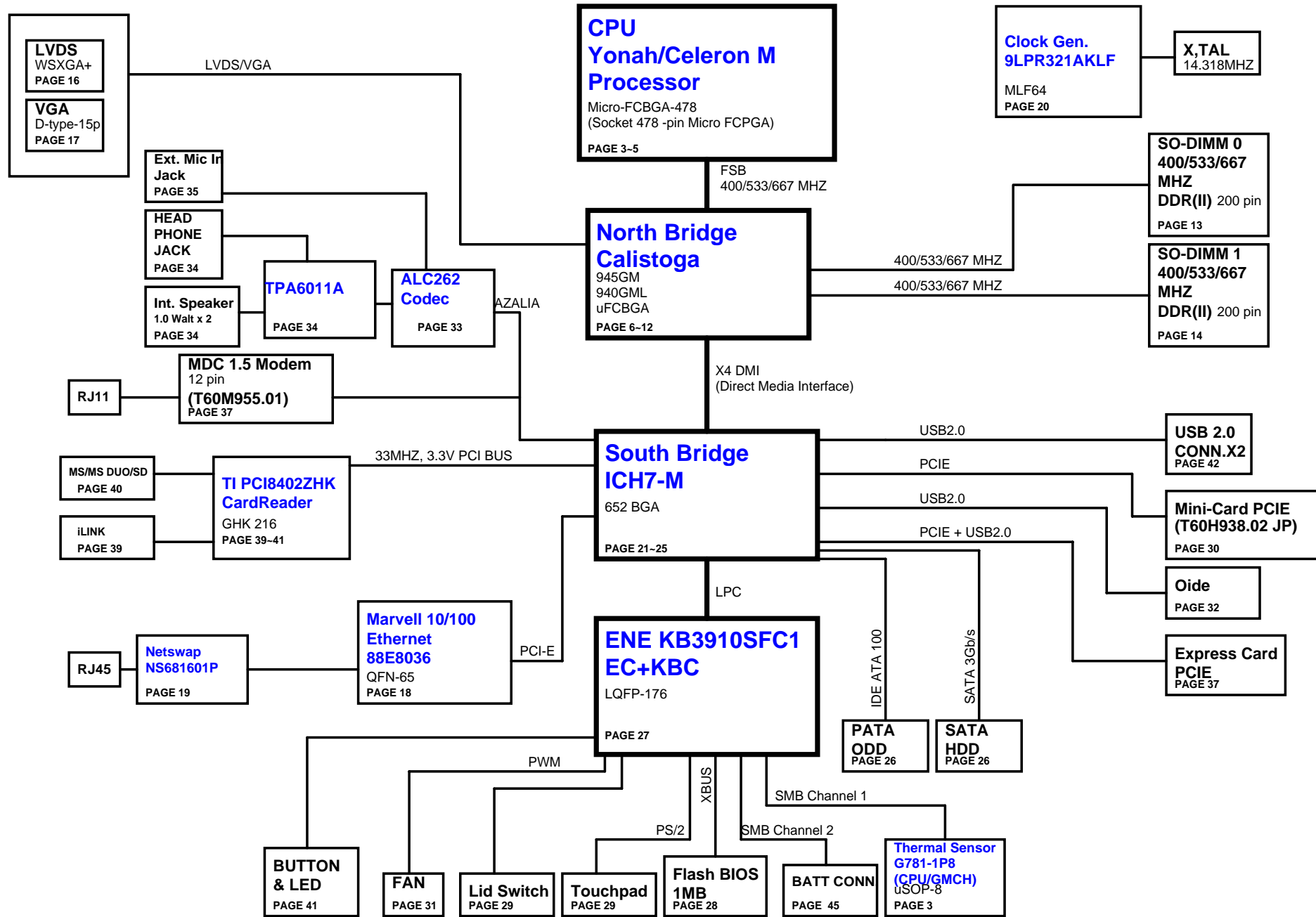
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

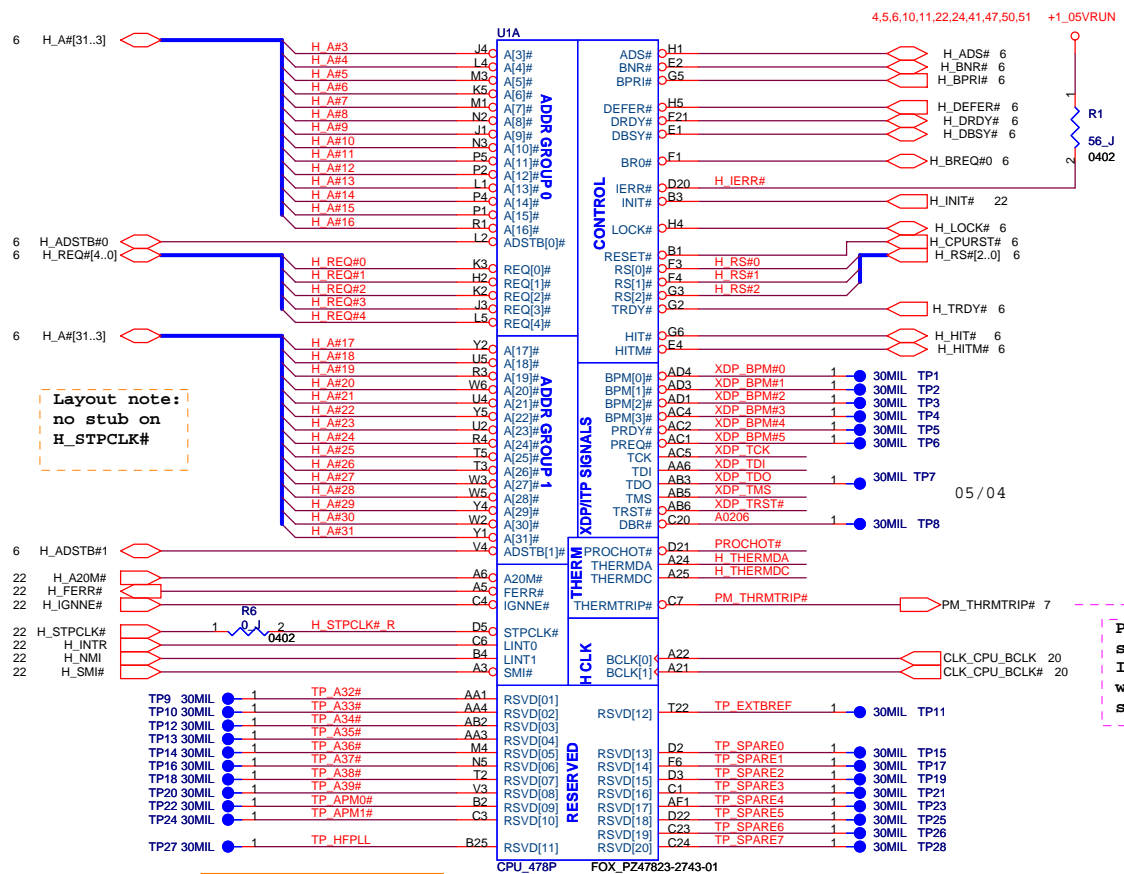
Title: Index Page

Size: A3 Document Number: MS70-1-01 Rev: 0.30

Date: Tuesday, June 13, 2006 Sheet: 1 of 55

# RAPTOR/MS70(CALISTOGA GM/GML Block Diagram)

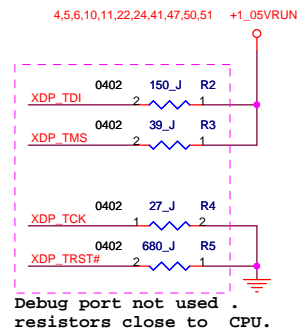




Layout note:  
no stub on  
H\_STPCLK#

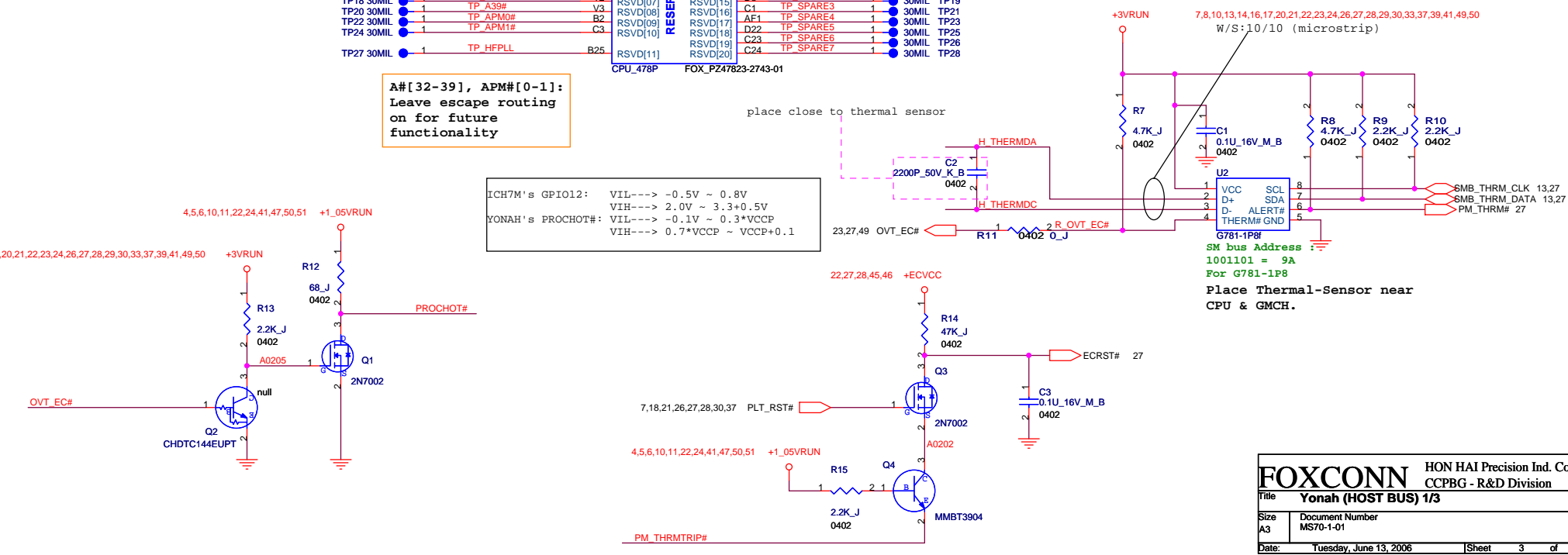
A#[32-39], APM#[0-1]:  
Leave escape routing  
on for future  
functionality

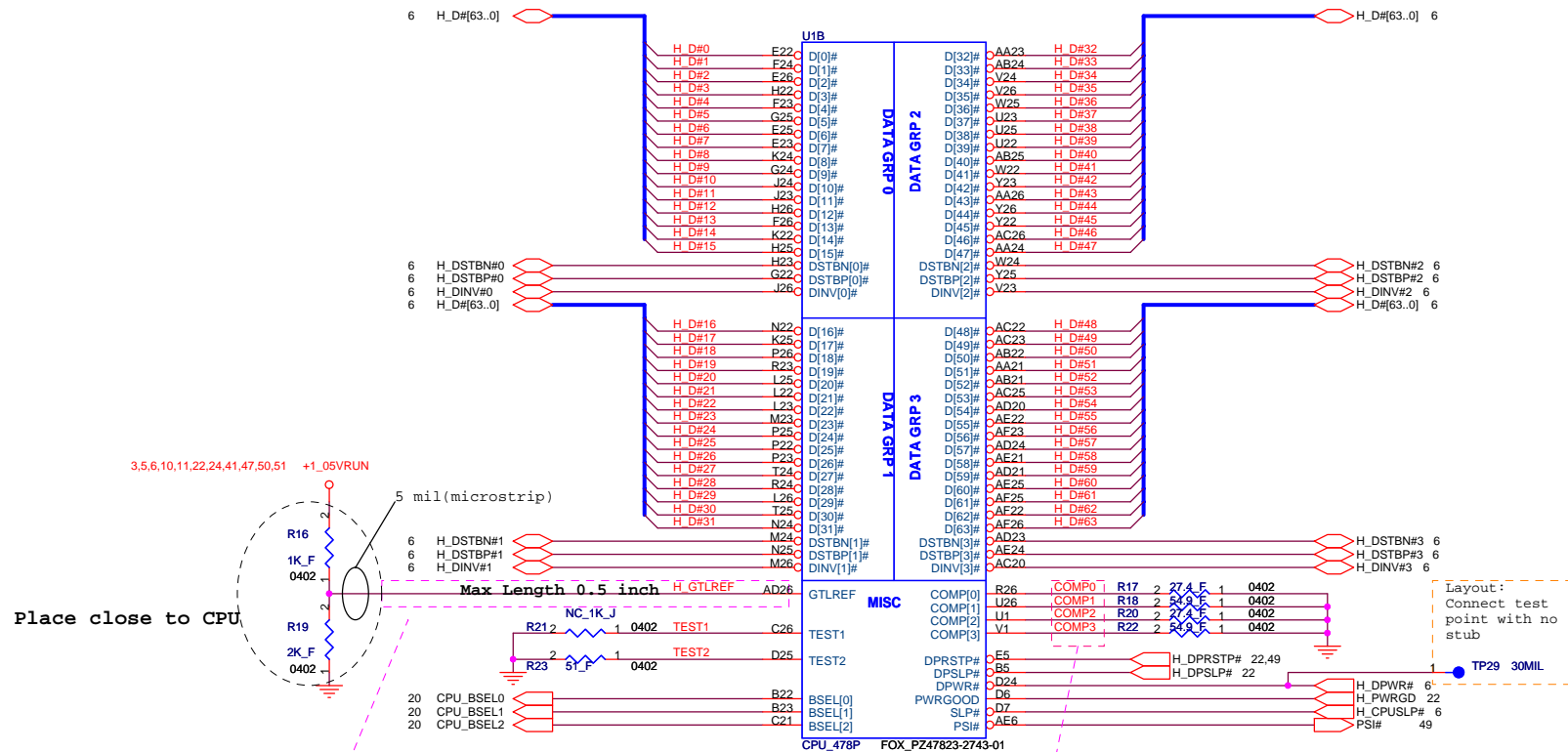
ICH7M's GPIO12: VIL----> -0.5V ~ 0.8V  
VIH----> 2.0V ~ 3.3+0.5V  
YONAH's PROCHOT#: VIL----> -0.1V ~ 0.3\*VCCP  
VIH----> 0.7\*VCCP ~ VCCP+0.1



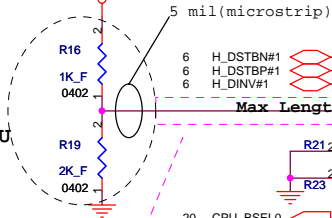
Debug port not used.  
resistors close to CPU.

PM\_THRMTRIP#  
should connect to  
ICH7-M and GMCH  
without T-ing (No  
stub)





3,5,6,10,11,22,24,41,47,50,51 +1\_05VRUN



Place close to CPU

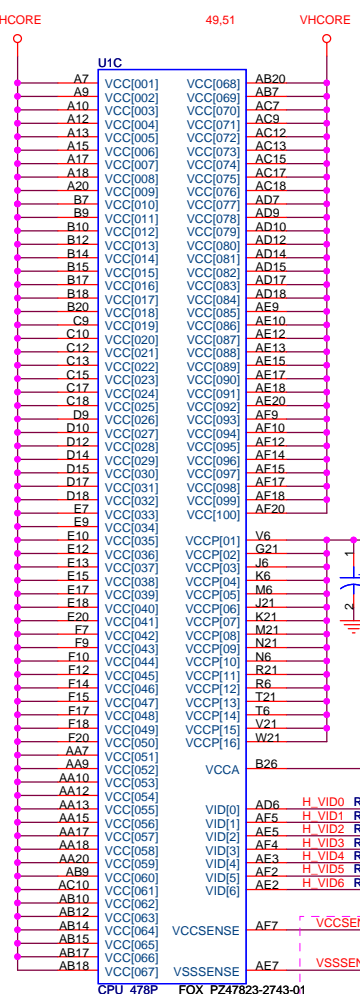
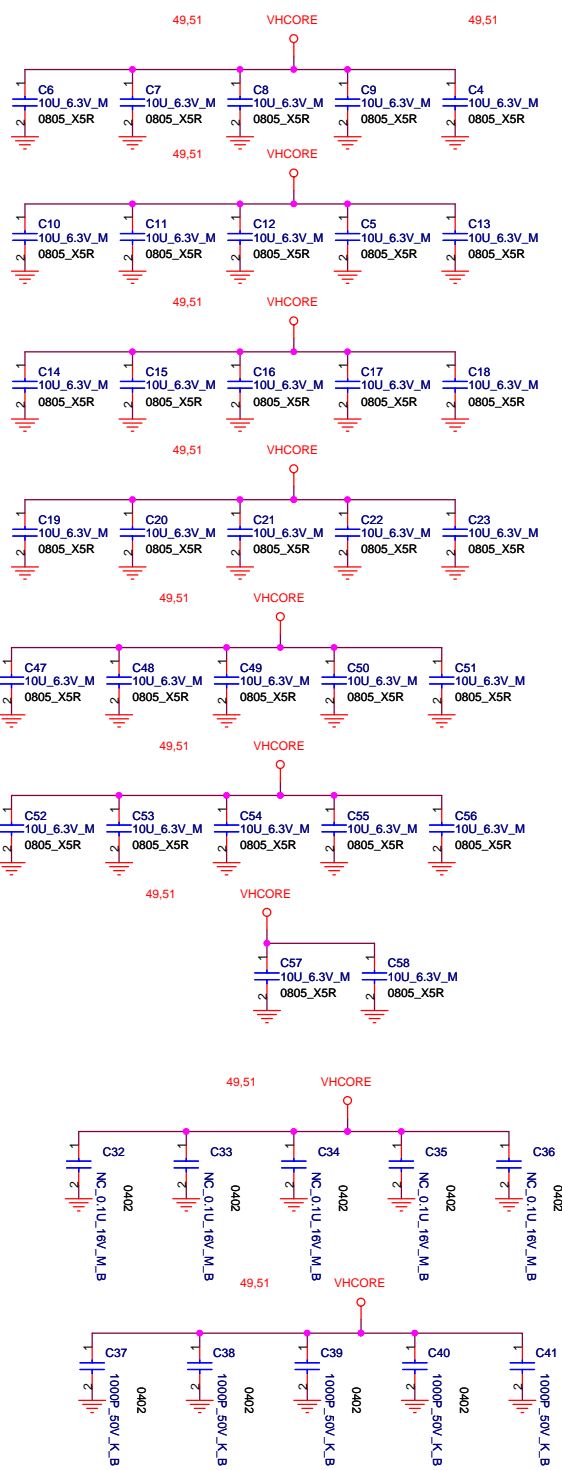
Max Length 0.5 inch H\_GTLREF

Layout Note:  
Zo=55 ohm, 0.5" max for GTLREF.

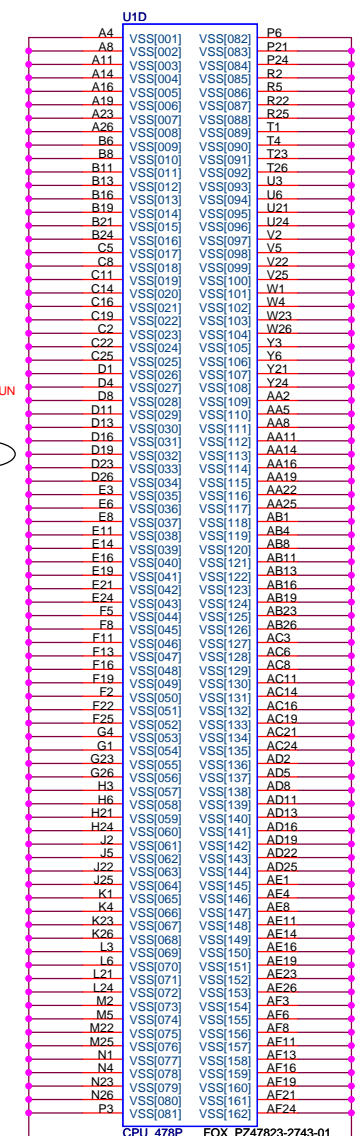
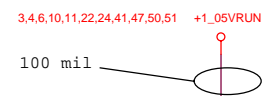
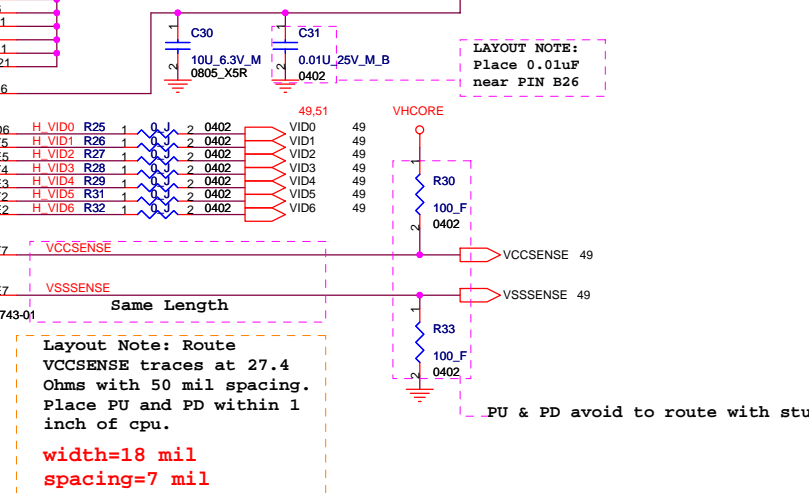
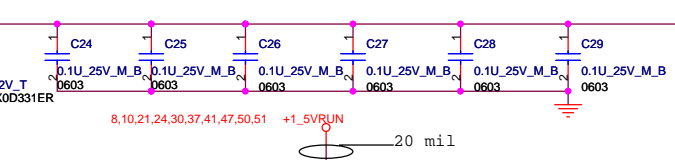
Layout Note:  
Comp0, 2 connect with Zo=27.4 ohm, make trace length shorter then 0.5".  
Comp1, 3 connect with Zo=55 ohm, make trace length shorter then 0.5".

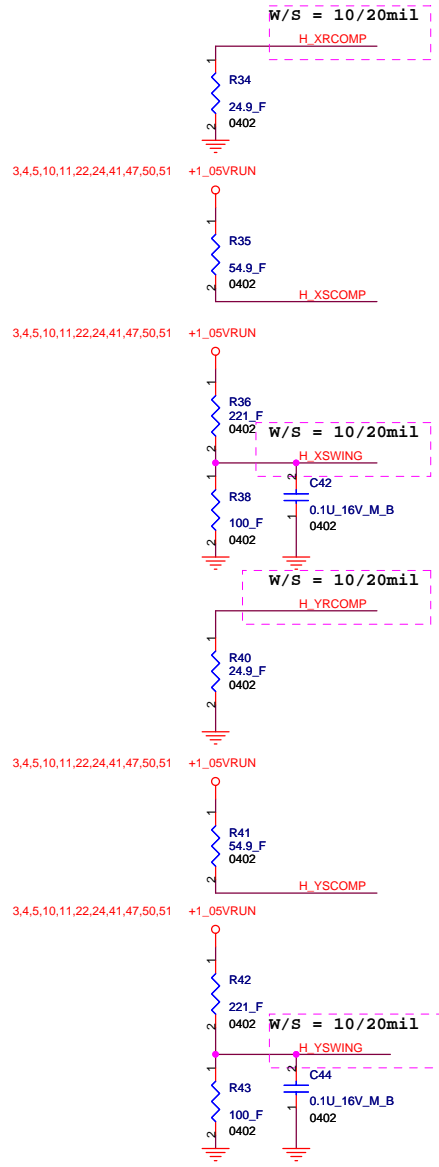
IMVP6 (max8736)  
cpu PSI# <-> max8736 PSI#  
max8736: VIHmin=0.67V  
VILmax=0.33V  
(ref. max8736 datasheet)

Layout:  
Connect test point with no stub



CPU\_VCCA---->120mA  
 CPU\_VCCP----->2.5A  
 CPU\_VCC----->36A



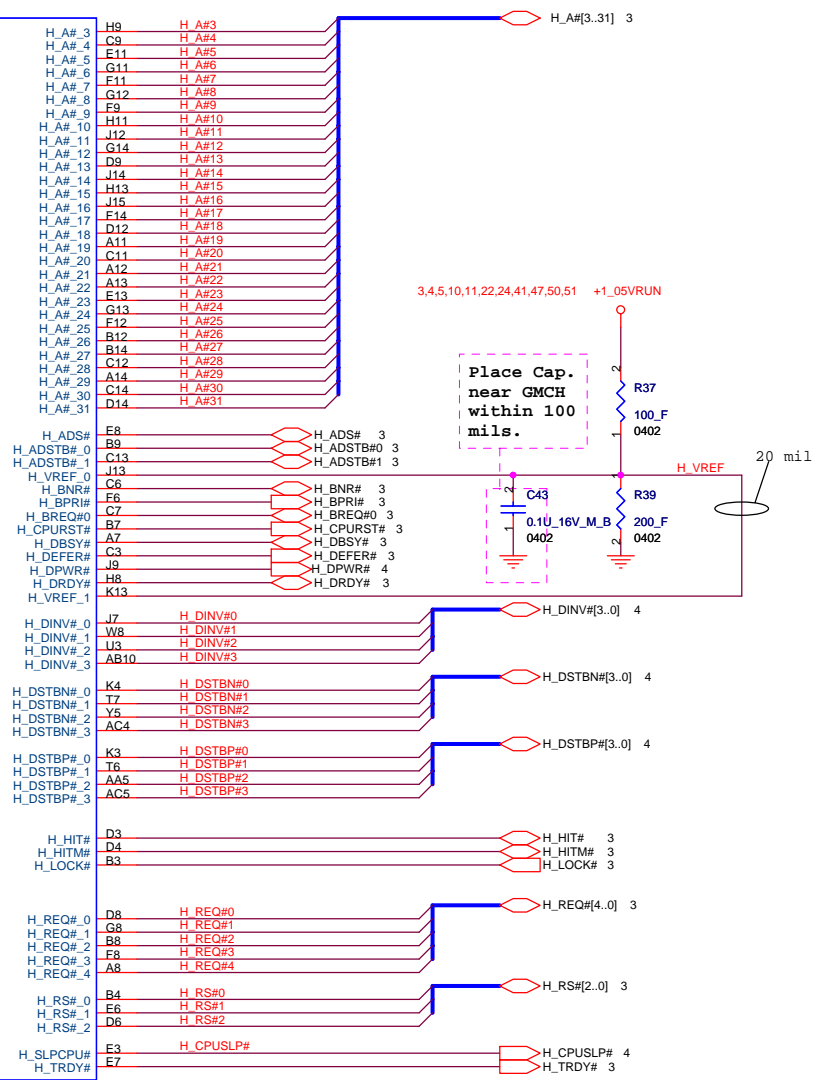


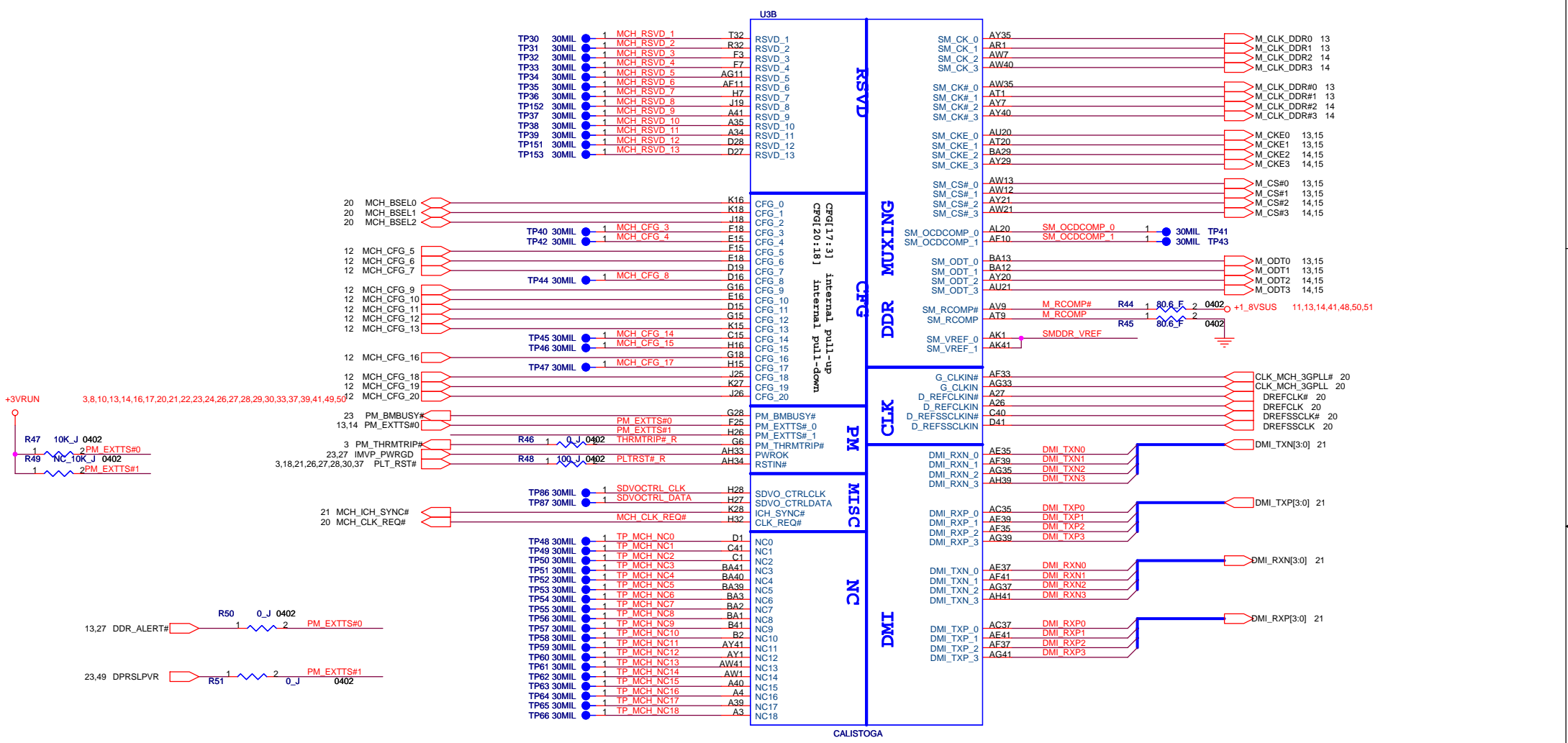
4 H\_D#[63..0] H\_D#[63..0]

USA		CALISTOGA	
H_D#0	F1	H_XRCOMP	E1
H_D#1	J1	H_XSCOMP	E2
H_D#2	H1	H_XSWING	E4
H_D#3	J6	H_YRCOMP	Y1
H_D#4	H3	H_YSCOMP	U1
H_D#5	K2	H_YSWING	W1
H_D#6	G1	H_CLKIN	AG1
H_D#7	G2	H_CLKIN#	AG2
H_D#8	K9		
H_D#9	K1		
H_D#10	K7		
H_D#11	J8		
H_D#12	H4		
H_D#13	J3		
H_D#14	K11		
H_D#15	G4		
H_D#16	T10		
H_D#17	W11		
H_D#18	T3		
H_D#19	U7		
H_D#20	U9		
H_D#21	U11		
H_D#22	T11		
H_D#23	W9		
H_D#24	T1		
H_D#25	T8		
H_D#26	T4		
H_D#27	W7		
H_D#28	U5		
H_D#29	T9		
H_D#30	W6		
H_D#31	T5		
H_D#32	AB7		
H_D#33	AA9		
H_D#34	W4		
H_D#35	W3		
H_D#36	Y3		
H_D#37	Y7		
H_D#38	W5		
H_D#39	Y10		
H_D#40	AB8		
H_D#41	W2		
H_D#42	AA4		
H_D#43	AA7		
H_D#44	AA2		
H_D#45	AA6		
H_D#46	AA10		
H_D#47	Y8		
H_D#48	AA1		
H_D#49	AB4		
H_D#50	AC9		
H_D#51	AB11		
H_D#52	AC11		
H_D#53	AB3		
H_D#54	AC2		
H_D#55	AD1		
H_D#56	AD9		
H_D#57	AC1		
H_D#58	AD7		
H_D#59	AC6		
H_D#60	AB5		
H_D#61	AD10		
H_D#62	AD4		
H_D#63	AC8		

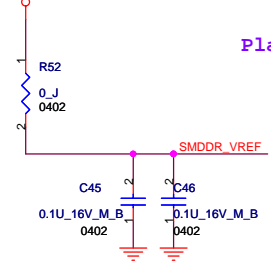
20 CLK\_MCH\_BCLK#  
20 CLK\_MCH\_BCLK#

HOST

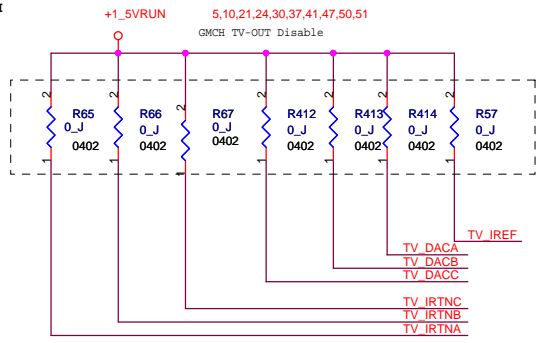
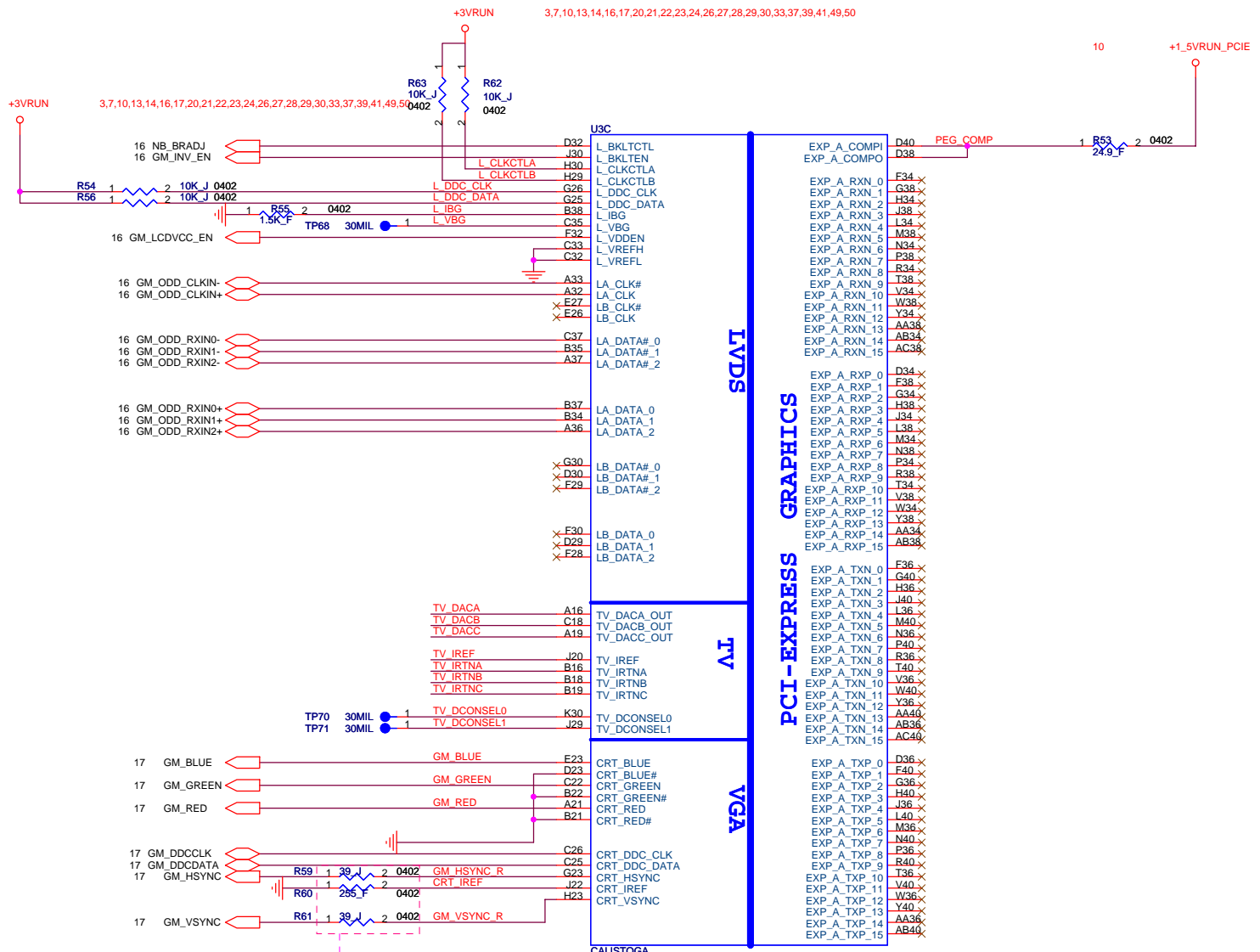




13,48 DDRDIMM\_VREF



Place close to chipset



U3C Pin	Signal Name	Component	Value
D32	L_BKLTCTL		
J30	L_BKLTEN		
H30	L_CLKCTLA		
H29	L_CLKCTLB		
G26	L_DDC_CLK		
G25	L_DDC_DATA		
B38	L_IBG		
C35	L_VBG		
F32	L_VDDEN		
C33	L_VREFH		
C32	L_VREFL		
A33	LA_CLK#		
A32	LA_CLK		
E27	LB_CLK#		
E26	LB_CLK		
C37	LA_DATA#_0		
B35	LA_DATA#_1		
A37	LA_DATA#_2		
B37	LA_DATA_0		
B34	LA_DATA_1		
A36	LA_DATA_2		
G30	LB_DATA#_0		
D30	LB_DATA#_1		
F29	LB_DATA#_2		
F30	LB_DATA_0		
D29	LB_DATA_1		
F28	LB_DATA_2		
A16	TV_DACA		
C18	TV_DACB		
A19	TV_DACC		
J20	TV_IREF		
B16	TV_IRTNA		
B18	TV_IRTNC		
B19	TV_IRTNC		
K30	TV_DCONSEL0		
J29	TV_DCONSEL1		
E23	CRT_BLUE		
D23	CRT_BLUE#		
C22	CRT_GREEN		
B22	CRT_GREEN#		
A21	CRT_RED		
B21	CRT_RED#		
C26	CRT_DDC_CLK		
C25	CRT_DDC_DATA		
G23	CRT_HSYNC		
J22	CRT_IREF		
H23	CRT_VSYNC		

**LVDS**  
**PCI-EXPRESS**  
**GRAPHICS**  
**TV**  
**VGA**

3,7,10,13,14,16,17,20,21,22,23,24,26,27,28,29,30,33,37,39,41,49,50

10

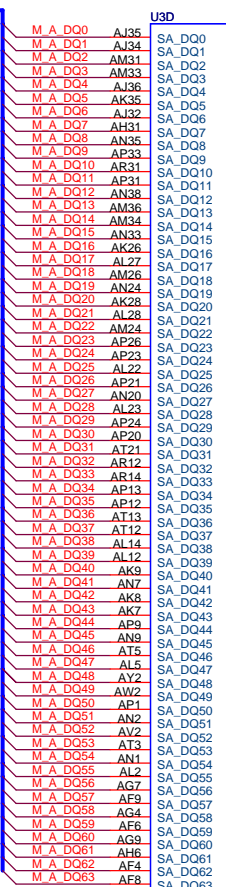
+1\_5VVRUN\_PCIE

+1\_5VVRUN 5,10,21,24,30,37,41,47,50,51  
GMCH TV-OUT Disable

Place resistor close to GMCH



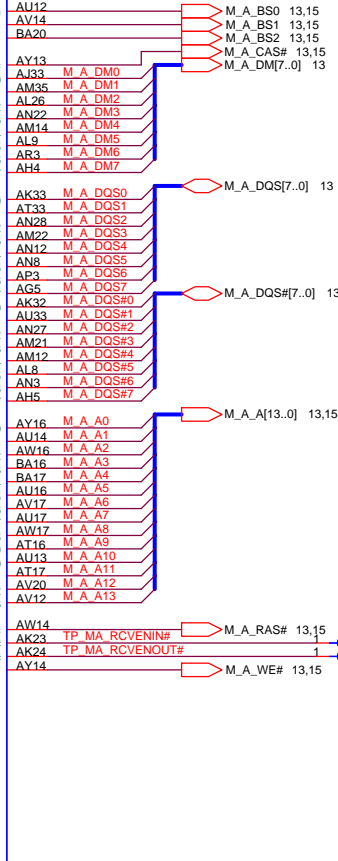
13 M\_A\_DQ[63.0]



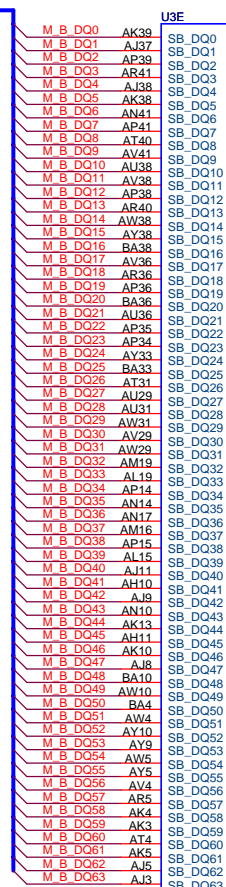
U3D

DDR SYSTEM MEMORY A

CALISTOGA



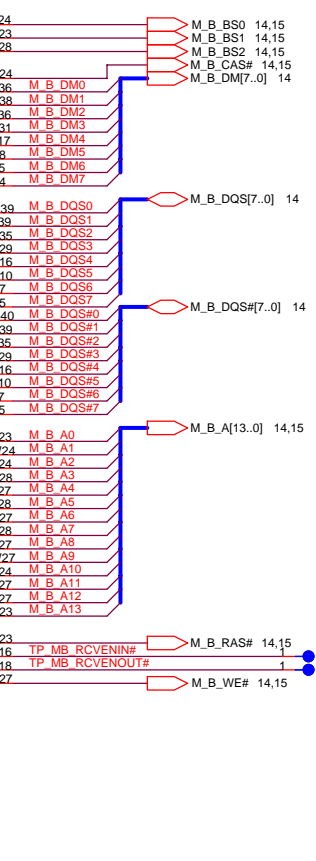
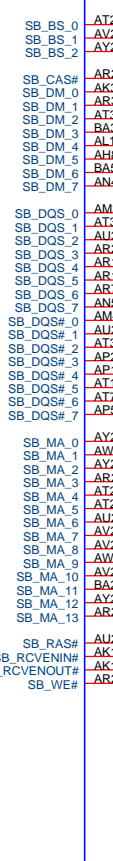
14 M\_B\_DQ[63.0]

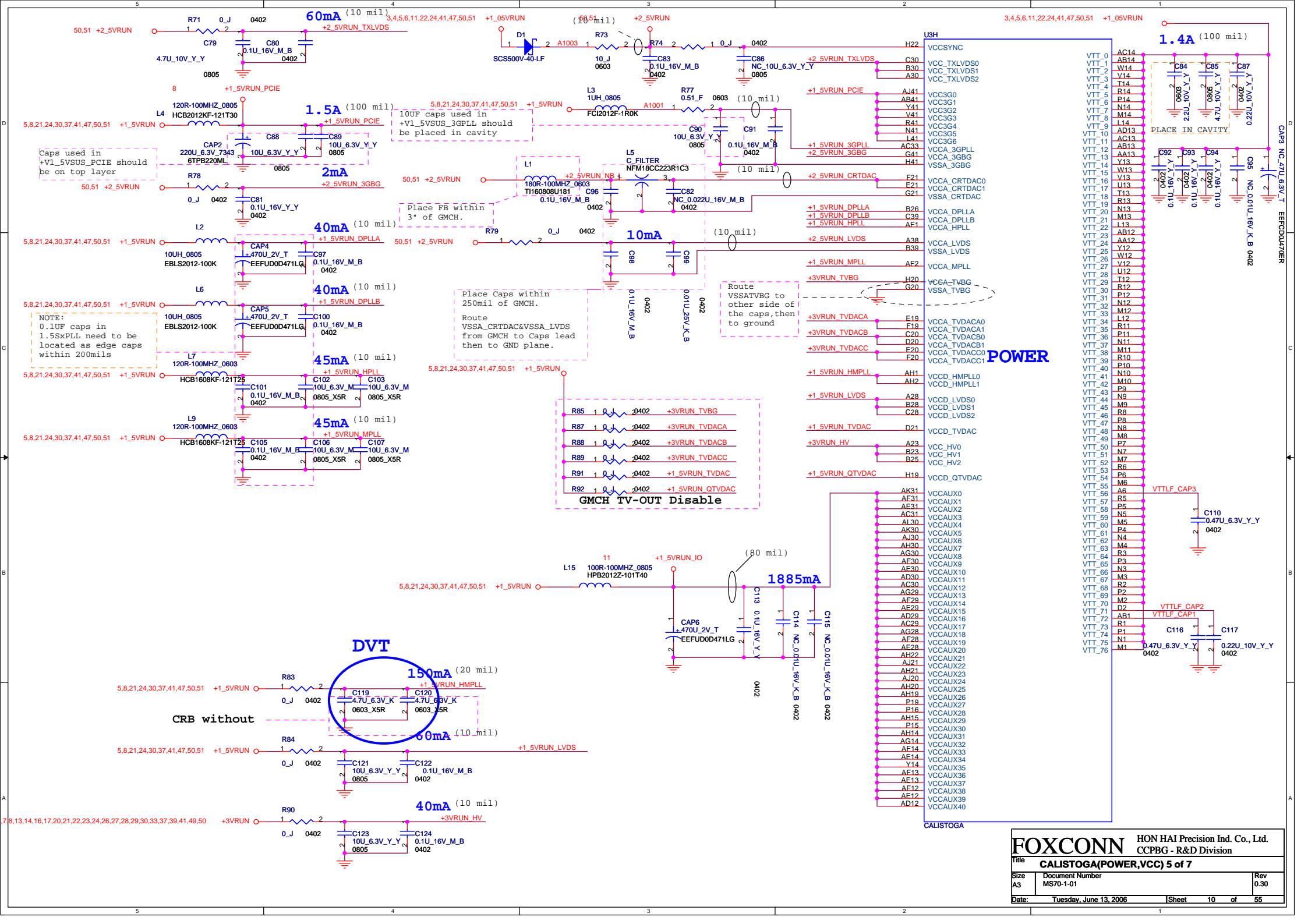


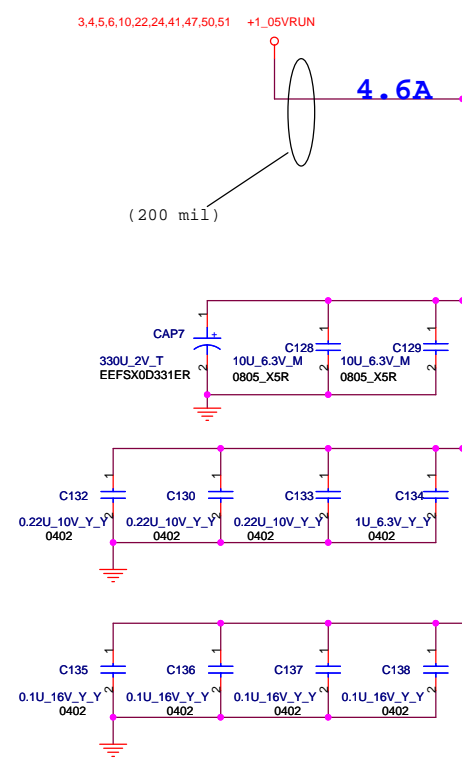
U3E

DDR SYSTEM MEMORY B

CALISTOGA

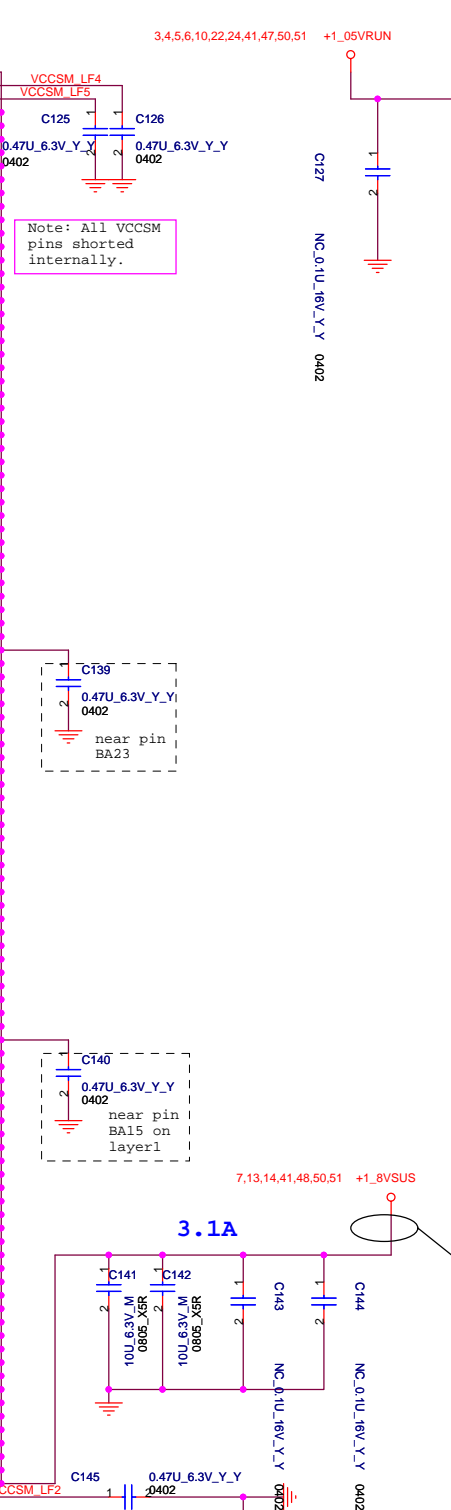




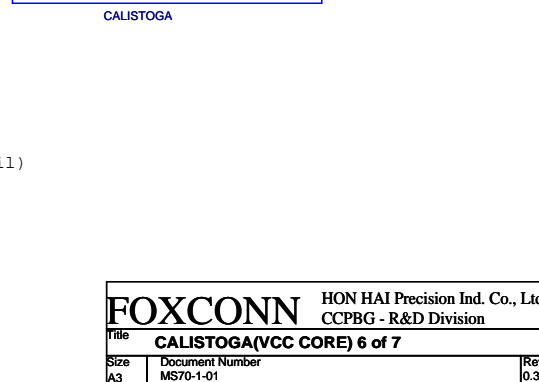
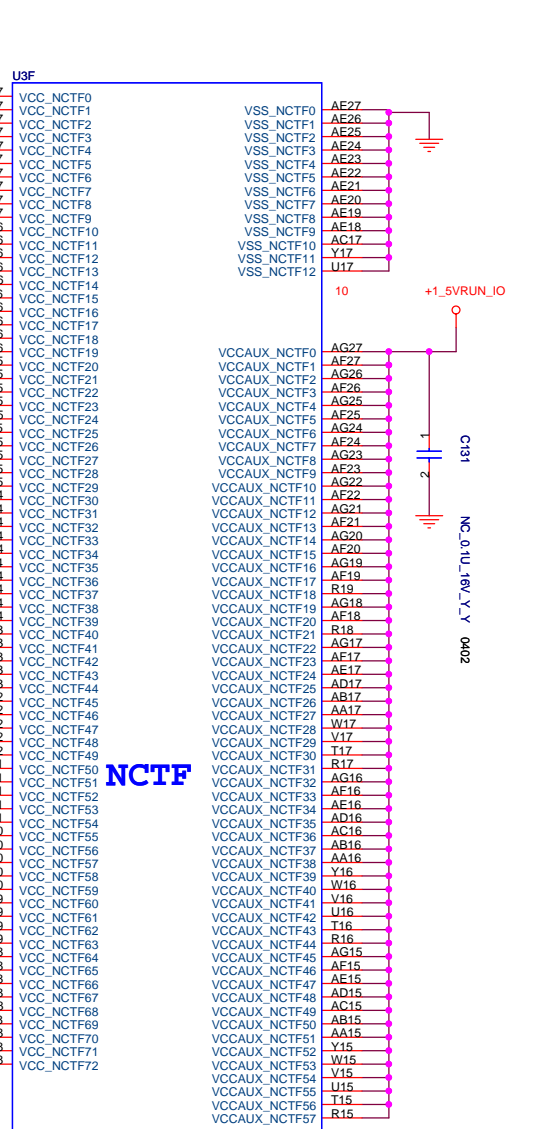


- AA33 VCC\_0  
 W33 VCC\_1  
 P33 VCC\_2  
 L33 VCC\_3  
 J33 VCC\_4  
 AA32 VCC\_5  
 Y32 VCC\_6  
 V32 VCC\_7  
 W32 VCC\_8  
 P32 VCC\_9  
 N32 VCC\_10  
 M32 VCC\_11  
 L32 VCC\_12  
 J32 VCC\_13  
 AA31 VCC\_14  
 W31 VCC\_15  
 V31 VCC\_16  
 T31 VCC\_17  
 R31 VCC\_18  
 P31 VCC\_19  
 N31 VCC\_20  
 M31 VCC\_21  
 AA30 VCC\_22  
 Y30 VCC\_23  
 W30 VCC\_24  
 V30 VCC\_25  
 U30 VCC\_26  
 T30 VCC\_27  
 R30 VCC\_28  
 P30 VCC\_29  
 N30 VCC\_30  
 M30 VCC\_31  
 L30 VCC\_32  
 AA29 VCC\_33  
 Y29 VCC\_34  
 W29 VCC\_35  
 V29 VCC\_36  
 U29 VCC\_37  
 T29 VCC\_38  
 R29 VCC\_39  
 P29 VCC\_40  
 M29 VCC\_41  
 AA28 VCC\_42  
 Y28 VCC\_43  
 W28 VCC\_44  
 V28 VCC\_45  
 U28 VCC\_46  
 T28 VCC\_47  
 R28 VCC\_48  
 P28 VCC\_49  
 N28 VCC\_50  
 M28 VCC\_51  
 L28 VCC\_52  
 P27 VCC\_53  
 N27 VCC\_54  
 M27 VCC\_55  
 L27 VCC\_56  
 P26 VCC\_57  
 N26 VCC\_58  
 L26 VCC\_59  
 N25 VCC\_60  
 M25 VCC\_61  
 L25 VCC\_62  
 P24 VCC\_63  
 N24 VCC\_64  
 M24 VCC\_65  
 AA23 VCC\_66  
 Y23 VCC\_68  
 P23 VCC\_70  
 N23 VCC\_71  
 M23 VCC\_72  
 L23 VCC\_73  
 AA22 VCC\_74  
 Y22 VCC\_75  
 W22 VCC\_76  
 P22 VCC\_77  
 N22 VCC\_78  
 M22 VCC\_79  
 L22 VCC\_80  
 AC21 VCC\_81  
 AA21 VCC\_82  
 W21 VCC\_83  
 N21 VCC\_84  
 M21 VCC\_85  
 L21 VCC\_86  
 AC20 VCC\_87  
 AB20 VCC\_88  
 Y20 VCC\_89  
 W20 VCC\_90  
 P20 VCC\_91  
 N20 VCC\_92  
 M20 VCC\_93  
 L20 VCC\_94  
 AB19 VCC\_95  
 AA19 VCC\_96  
 Y19 VCC\_97  
 N19 VCC\_98  
 M19 VCC\_99  
 L19 VCC\_100  
 N18 VCC\_101  
 M18 VCC\_102  
 L18 VCC\_103  
 P17 VCC\_104  
 N17 VCC\_105  
 M17 VCC\_106  
 N16 VCC\_107  
 M16 VCC\_108  
 L16 VCC\_109  
 L16 VCC\_110

- VCC\_SM\_0  
 VCC\_SM\_1  
 VCC\_SM\_2  
 VCC\_SM\_3  
 VCC\_SM\_4  
 VCC\_SM\_5  
 VCC\_SM\_6  
 VCC\_SM\_7  
 VCC\_SM\_8  
 VCC\_SM\_9  
 VCC\_SM\_10  
 VCC\_SM\_11  
 VCC\_SM\_12  
 VCC\_SM\_13  
 VCC\_SM\_14  
 VCC\_SM\_15  
 VCC\_SM\_16  
 VCC\_SM\_17  
 VCC\_SM\_18  
 VCC\_SM\_19  
 VCC\_SM\_20  
 VCC\_SM\_21  
 VCC\_SM\_22  
 VCC\_SM\_23  
 VCC\_SM\_24  
 VCC\_SM\_25  
 VCC\_SM\_26  
 VCC\_SM\_27  
 VCC\_SM\_28  
 VCC\_SM\_29  
 VCC\_SM\_30  
 VCC\_SM\_31  
 VCC\_SM\_32  
 VCC\_SM\_33  
 VCC\_SM\_34  
 VCC\_SM\_35  
 VCC\_SM\_36  
 VCC\_SM\_37  
 VCC\_SM\_38  
 VCC\_SM\_39  
 VCC\_SM\_40  
 VCC\_SM\_41  
 VCC\_SM\_42  
 VCC\_SM\_43  
 VCC\_SM\_44  
 VCC\_SM\_45  
 VCC\_SM\_46  
 VCC\_SM\_47  
 VCC\_SM\_48  
 VCC\_SM\_49  
 VCC\_SM\_50  
 VCC\_SM\_51  
 VCC\_SM\_52  
 VCC\_SM\_53  
 VCC\_SM\_54  
 VCC\_SM\_55  
 VCC\_SM\_56  
 VCC\_SM\_57  
 VCC\_SM\_58  
 VCC\_SM\_59  
 VCC\_SM\_60  
 VCC\_SM\_61  
 VCC\_SM\_62  
 VCC\_SM\_63  
 VCC\_SM\_64  
 VCC\_SM\_65  
 VCC\_SM\_66  
 VCC\_SM\_67  
 VCC\_SM\_68  
 VCC\_SM\_69  
 VCC\_SM\_70  
 VCC\_SM\_71  
 VCC\_SM\_72  
 VCC\_SM\_73  
 VCC\_SM\_74  
 VCC\_SM\_75  
 VCC\_SM\_76  
 VCC\_SM\_77  
 VCC\_SM\_78  
 VCC\_SM\_79  
 VCC\_SM\_80  
 VCC\_SM\_81  
 VCC\_SM\_82  
 VCC\_SM\_83  
 VCC\_SM\_84  
 VCC\_SM\_85  
 VCC\_SM\_86  
 VCC\_SM\_87  
 VCC\_SM\_88  
 VCC\_SM\_89  
 VCC\_SM\_90  
 VCC\_SM\_91  
 VCC\_SM\_92  
 VCC\_SM\_93  
 VCC\_SM\_94  
 VCC\_SM\_95  
 VCC\_SM\_96  
 VCC\_SM\_97  
 VCC\_SM\_98  
 VCC\_SM\_99  
 VCC\_SM\_100  
 VCC\_SM\_101  
 VCC\_SM\_102  
 VCC\_SM\_103  
 VCC\_SM\_104  
 VCC\_SM\_105  
 VCC\_SM\_106  
 VCC\_SM\_107



- AD27 VCC\_NCTF0  
 AC27 VCC\_NCTF1  
 AB27 VCC\_NCTF2  
 AA27 VCC\_NCTF3  
 Y27 VCC\_NCTF4  
 W27 VCC\_NCTF5  
 V27 VCC\_NCTF6  
 U27 VCC\_NCTF7  
 T27 VCC\_NCTF8  
 R27 VCC\_NCTF9  
 AD26 VCC\_NCTF10  
 AC26 VCC\_NCTF11  
 AB26 VCC\_NCTF12  
 AA26 VCC\_NCTF13  
 Y26 VCC\_NCTF14  
 W26 VCC\_NCTF15  
 V26 VCC\_NCTF16  
 U26 VCC\_NCTF17  
 T26 VCC\_NCTF18  
 R26 VCC\_NCTF19  
 AD25 VCC\_NCTF20  
 AC25 VCC\_NCTF21  
 AB25 VCC\_NCTF22  
 AA25 VCC\_NCTF23  
 Y25 VCC\_NCTF24  
 W25 VCC\_NCTF25  
 V25 VCC\_NCTF26  
 U25 VCC\_NCTF27  
 T25 VCC\_NCTF28  
 R25 VCC\_NCTF29  
 AD24 VCC\_NCTF30  
 AC24 VCC\_NCTF31  
 AB24 VCC\_NCTF32  
 AA24 VCC\_NCTF33  
 Y24 VCC\_NCTF34  
 W24 VCC\_NCTF35  
 V24 VCC\_NCTF36  
 U24 VCC\_NCTF37  
 T24 VCC\_NCTF38  
 R24 VCC\_NCTF39  
 AD23 VCC\_NCTF40  
 AC23 VCC\_NCTF41  
 AB23 VCC\_NCTF42  
 AA23 VCC\_NCTF43  
 Y23 VCC\_NCTF44  
 AD22 VCC\_NCTF45  
 V22 VCC\_NCTF46  
 U22 VCC\_NCTF47  
 T22 VCC\_NCTF48  
 R22 VCC\_NCTF49  
 AD21 VCC\_NCTF50  
 V21 VCC\_NCTF51  
 U21 VCC\_NCTF52  
 T21 VCC\_NCTF53  
 R21 VCC\_NCTF54  
 AD20 VCC\_NCTF55  
 V20 VCC\_NCTF56  
 U20 VCC\_NCTF57  
 T20 VCC\_NCTF58  
 R20 VCC\_NCTF59  
 AD19 VCC\_NCTF60  
 V19 VCC\_NCTF61  
 U19 VCC\_NCTF62  
 T19 VCC\_NCTF63  
 AD18 VCC\_NCTF64  
 AC18 VCC\_NCTF65  
 AB18 VCC\_NCTF66  
 AA18 VCC\_NCTF67  
 Y18 VCC\_NCTF68  
 W18 VCC\_NCTF69  
 V18 VCC\_NCTF70  
 U18 VCC\_NCTF71  
 T18 VCC\_NCTF72



VCC

NCTF

CALISTOGA

7 MCH\_CFG\_5 ← 1 ● 30MIL TP76

MCH_CFG_5	Low = DMIX2 High = DMIX4
-----------	-----------------------------

7 MCH\_CFG\_6 ← 1 ● 30MIL TP77

MCH_CFG_6	Low = Moby Dick High = Calistoga DDR2 select (default high)
-----------	---

7 MCH\_CFG\_7 ← 1 ● 30MIL TP78

MCH_CFG_7 (CPU Strap)	Low = RSVD High = Mobile Yonah processor
-----------------------	---

7 MCH\_CFG\_9 ← 1 ● 30MIL TP81

MCH_CFG_9 (PCIe Graphics Lane)	Low = Reverse Lane operation High = Normal operation
--------------------------------	---

For layout convenience

7 MCH\_CFG\_10 ← 1 ● 30MIL TP82

MCH_CFG_10 (HOST PLL VCC SELECT)	Low = RESERVED High = MOBILITY
----------------------------------	-----------------------------------

7 MCH\_CFG\_11 ← 1 ● 30MIL TP83

MCH_CFG_11 (PSB 4x CLK ENABLE)	Low = Calistoga High = Reserved
--------------------------------	------------------------------------



7 MCH\_CFG\_12 ← 1 ● 30MIL TP84

7 MCH\_CFG\_13 ← 1 ● 30MIL TP85

MCH_CFG_[13:12] (XOR/ALLZ)	00=Partial Clock Gating Disable 01=XOR Mode Enable 10=All-Z Mode Enable 11=Normal Operation(Default)
----------------------------	---

7 MCH\_CFG\_16 ← 1 ● 30MIL TP160

MCH_CFG_16 (FSB Dynamic ODT)	Low = Dynamic ODT Disabled High = Dynamic ODT Enable
------------------------------	---

MCH_CFG_18 (VCC_CORE Select)	Low = 1.05V(default) High = 1.5V
------------------------------	-------------------------------------

7 MCH\_CFG\_18 ← 1 ● 30MIL TP79

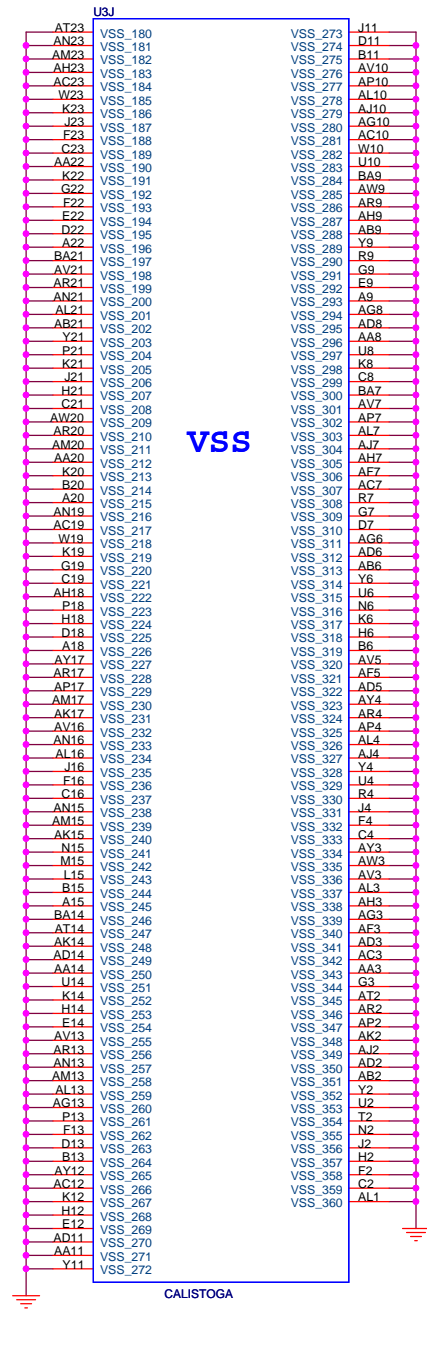
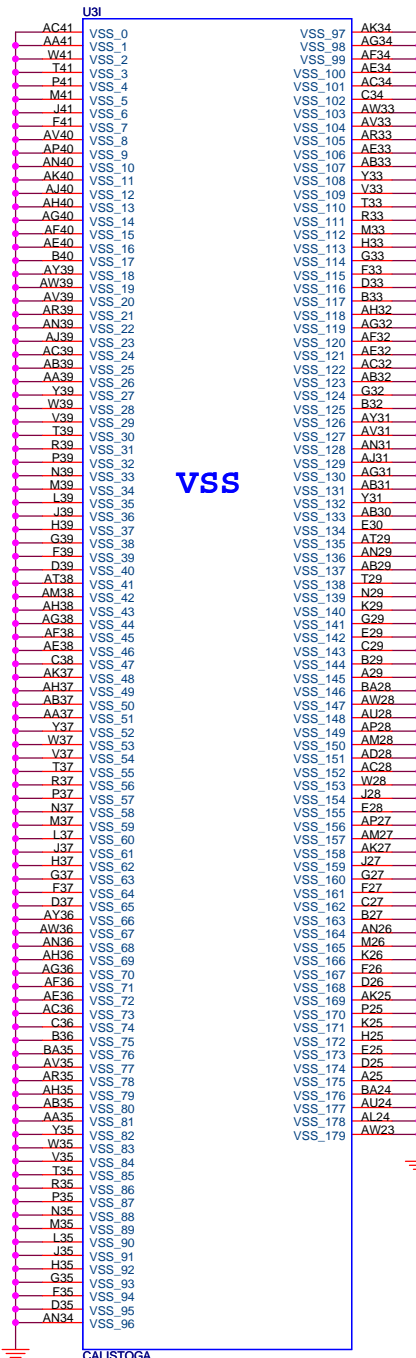
MCH_CFG_19 (DMI LANE REVERSAL)	Low = Normal(default) High = LANES REVERSED
--------------------------------	--

7 MCH\_CFG\_19 ← 1 ● 30MIL TP80

MCH_CFG_20 (PCIe Backward Interoperability mode)	Low = Only SDVO or PCIe x1 is operational (defaults) High = SDVO and PCIe x1 are operating simultaneously via the PEG port
--	---

7 MCH\_CFG\_20 ← 1 ● 30MIL TP83

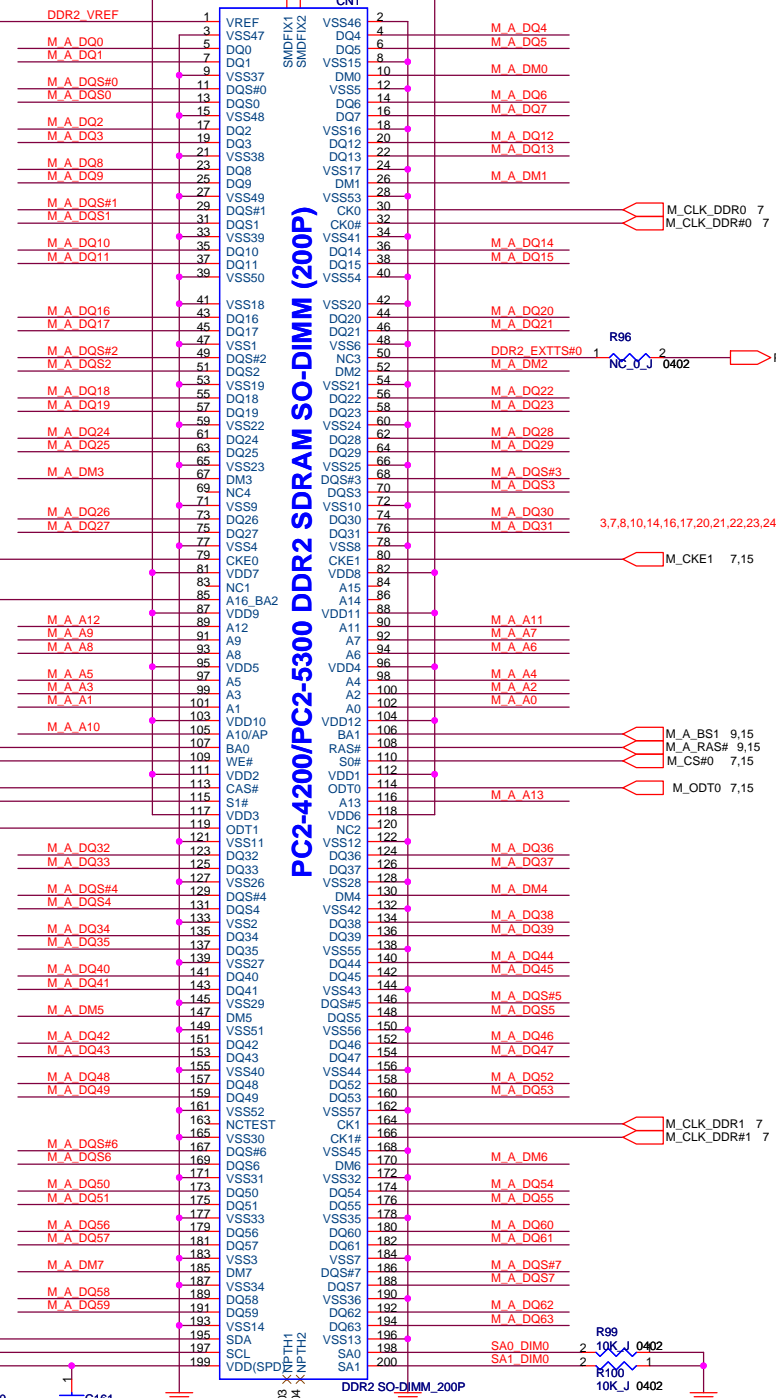
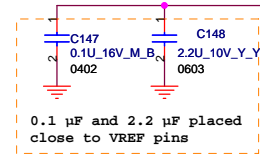
Layout Noe:  
Location of all MCH\_CFG strap resistors needs to be close to trace to minimize stub



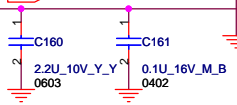
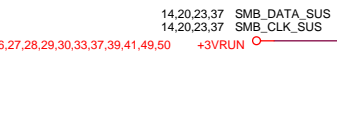
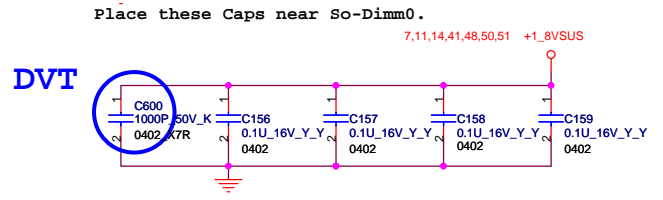
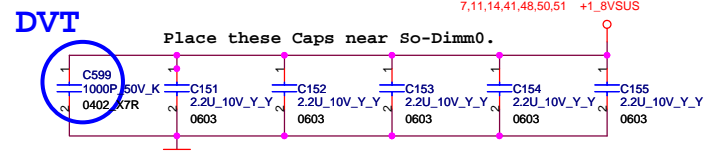
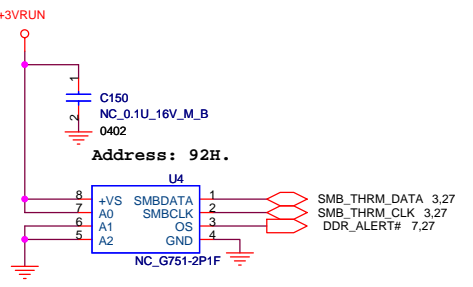
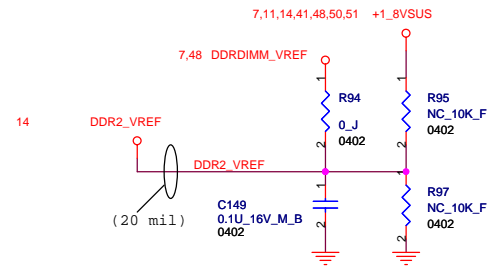
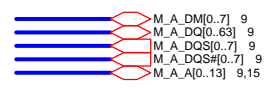
7,11,14,41,48,50,51 +1\_8VSUS

+1\_8VSUS 7,11,14,41,48,50,51

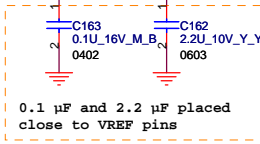
1.8V per DIMM=3.08A



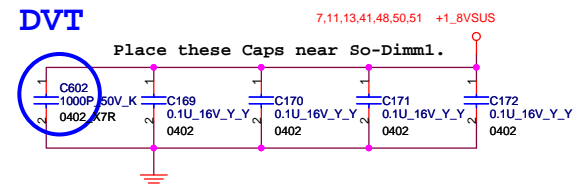
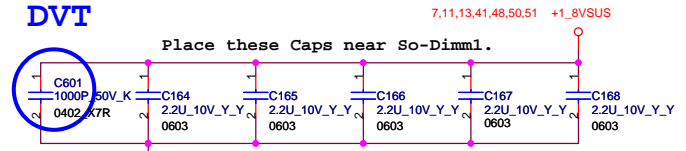
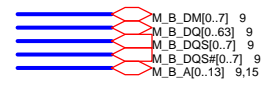
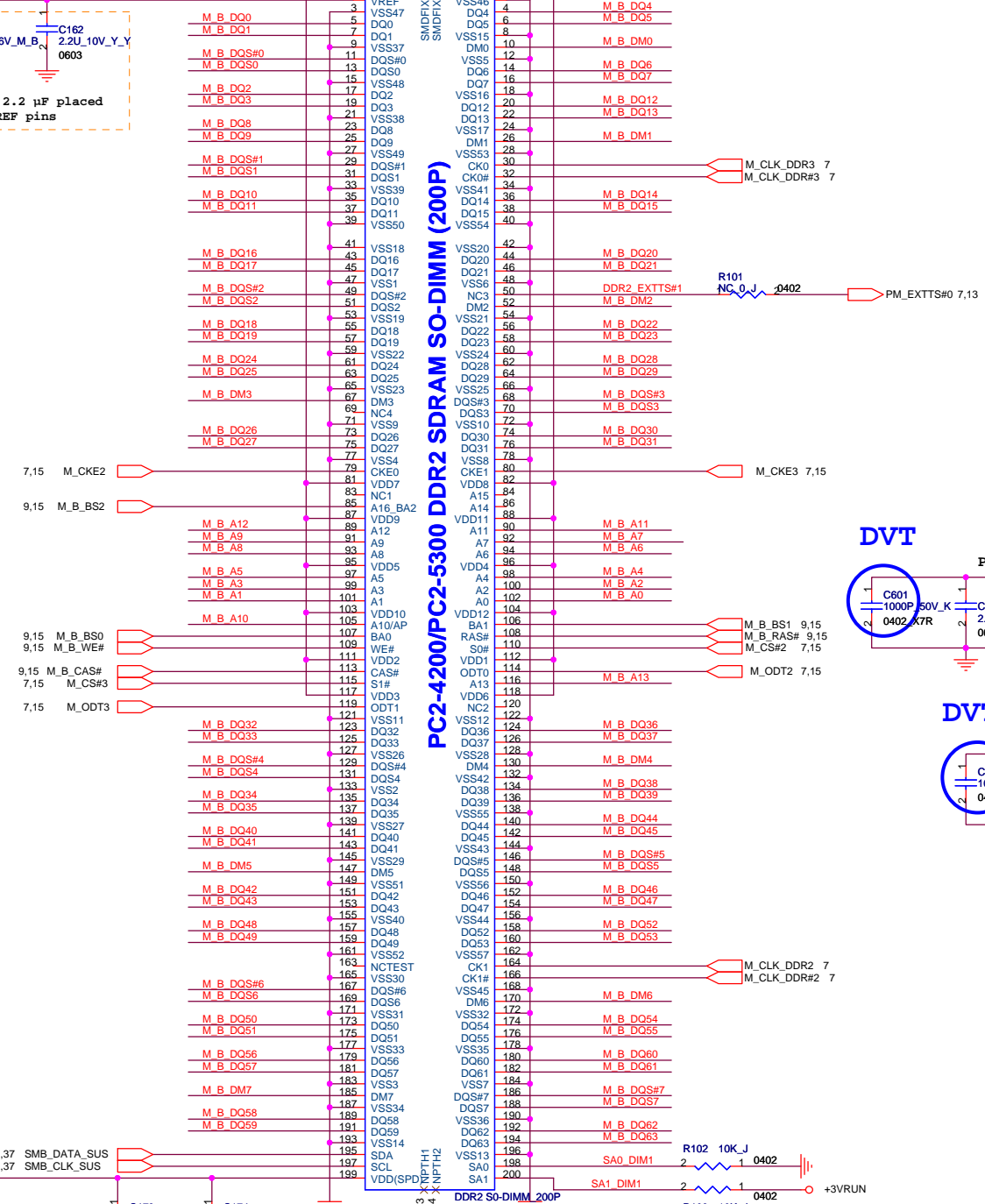
PC2-4200/PC2-5300 DDR2 SDRAM SO-DIMM (200P)



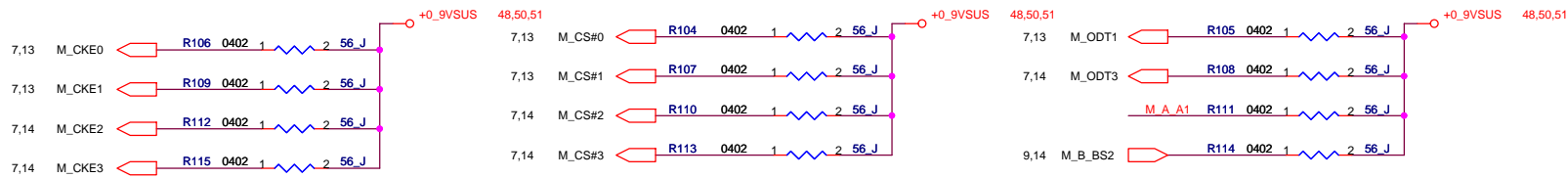
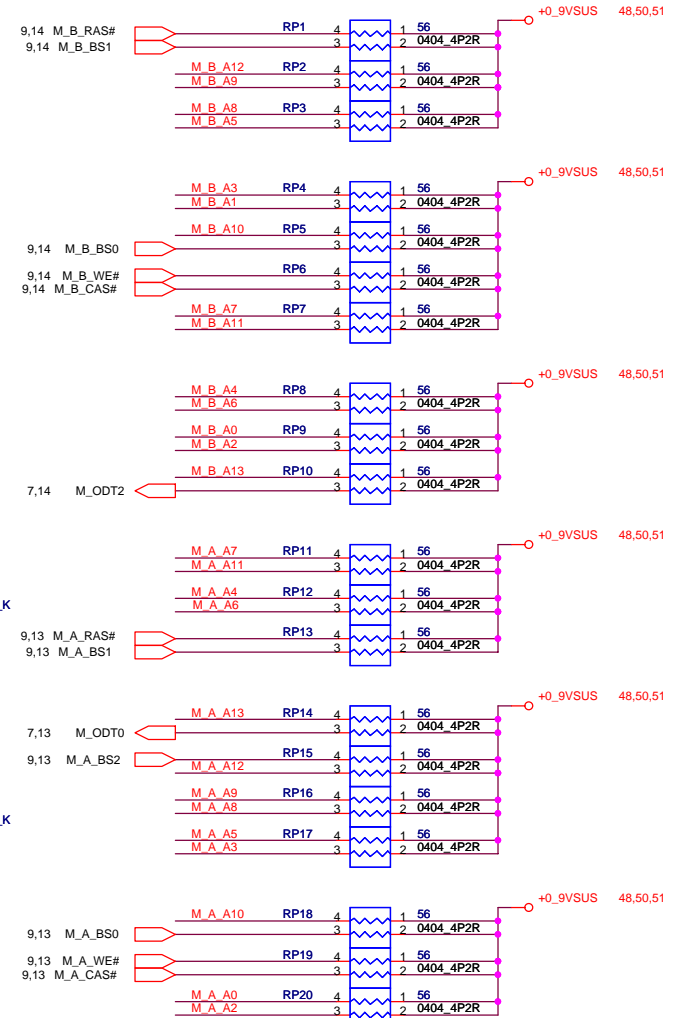
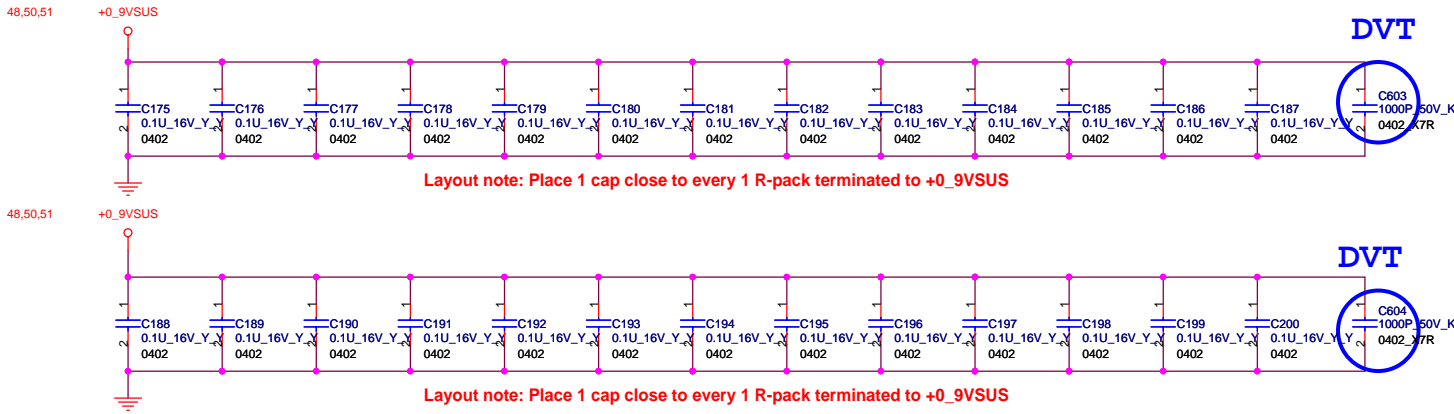
FOX\_AS0A426\_N4RC\_4F  
SMBus Address: A0(W)/A1(R)  
**DIMM\_0**  
Place DIMM\_0 near GMCH



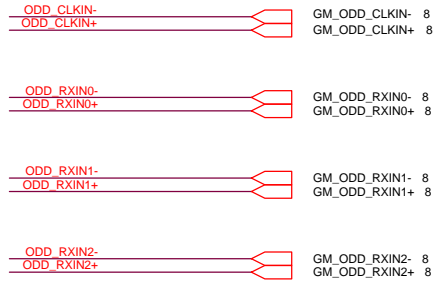
1.8V per DIMM=3.08A



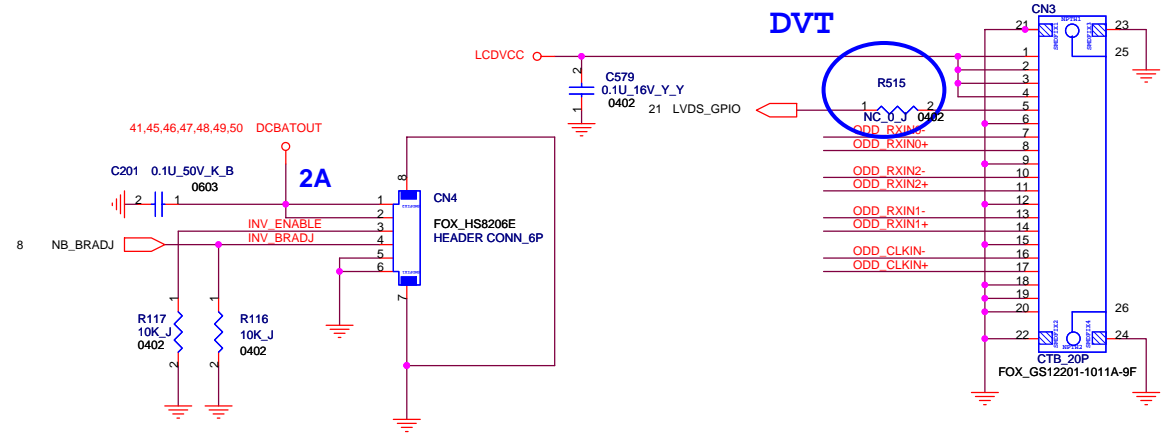
<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
File	<b>DDR(I)SO-DIMM_1</b>	
Size	Document Number	Rev
A3	MST0-1-01	0.30
Date:	Tuesday, June 13, 2006	Sheet 14 of 55



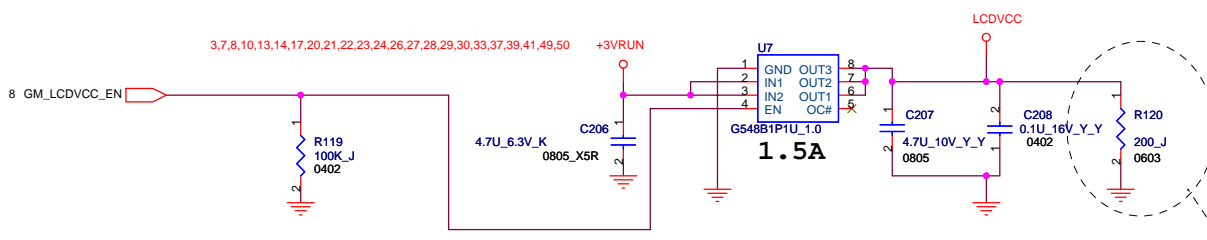
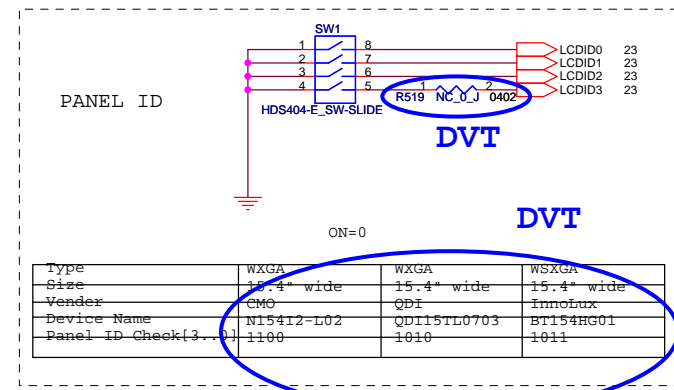
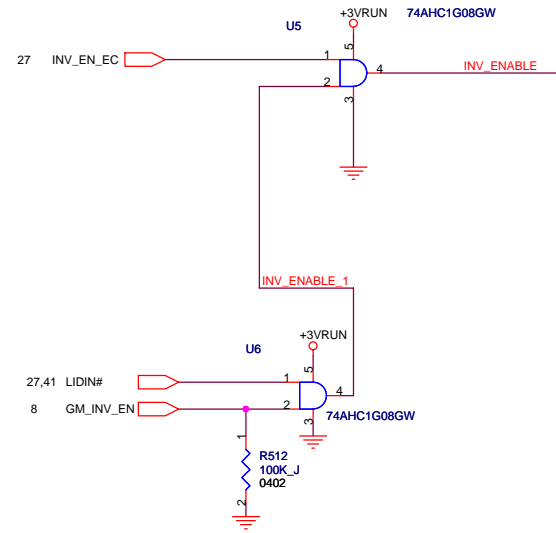
# LVDS



# LVDS CONNECTOR



# INVERTER CONNECTOR



DISCHARGE

The R461 will consume about 0.054 Watt (3.3x3.3/200 = 0.054W). We changed resistor to 0603 size (1/8 Watt)

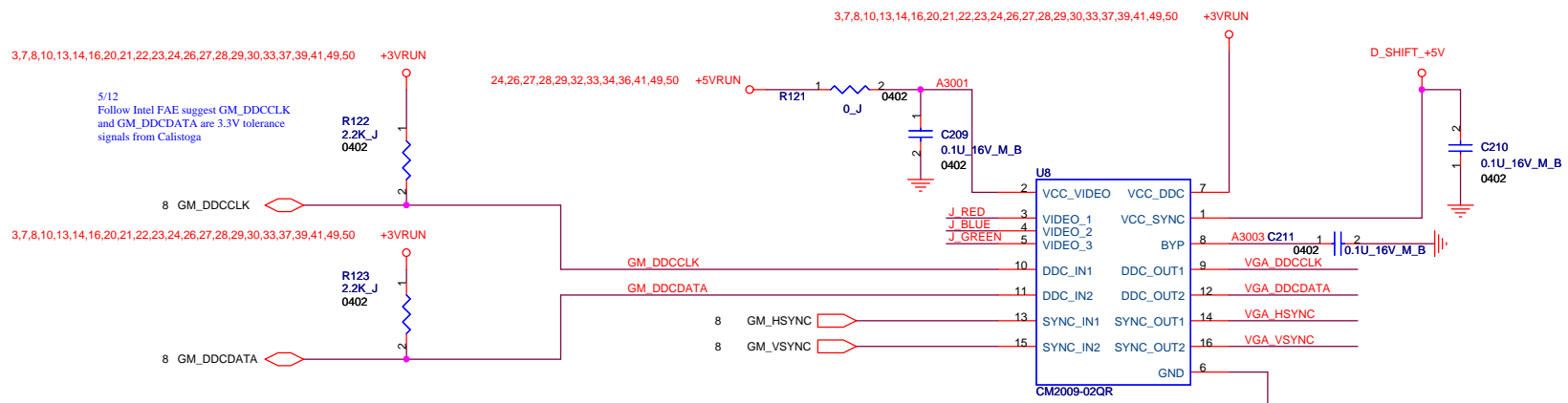
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title **LVDS**

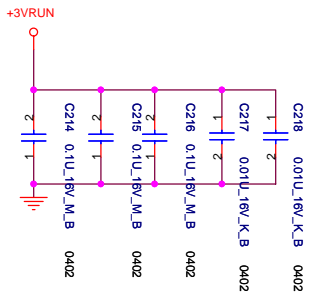
Size A3	Document Number MS70-1-01	Rev 0.30
---------	---------------------------	----------

Date: Tuesday, June 13, 2006 Sheet 16 of 55

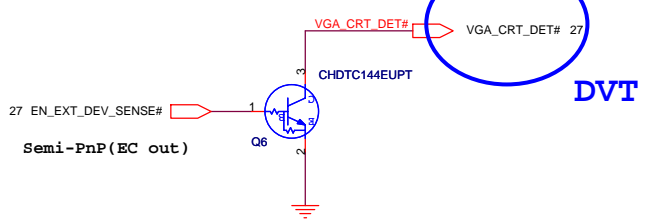
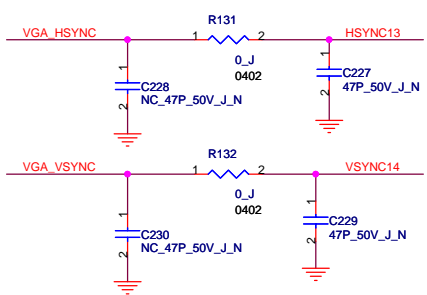
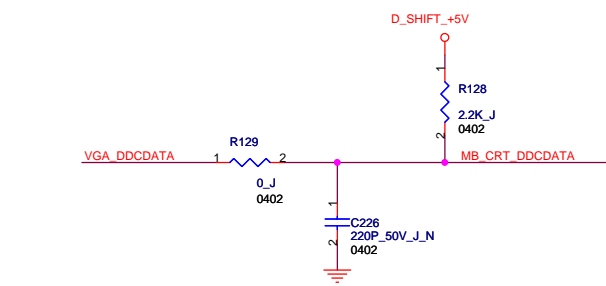
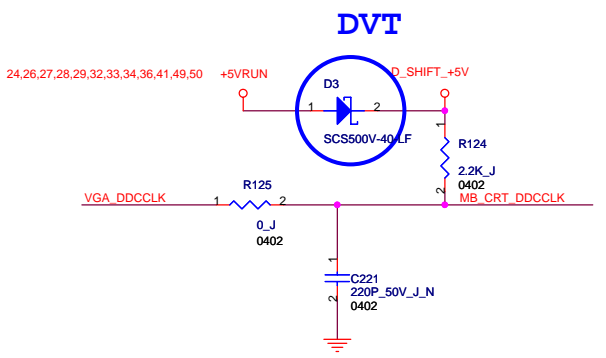
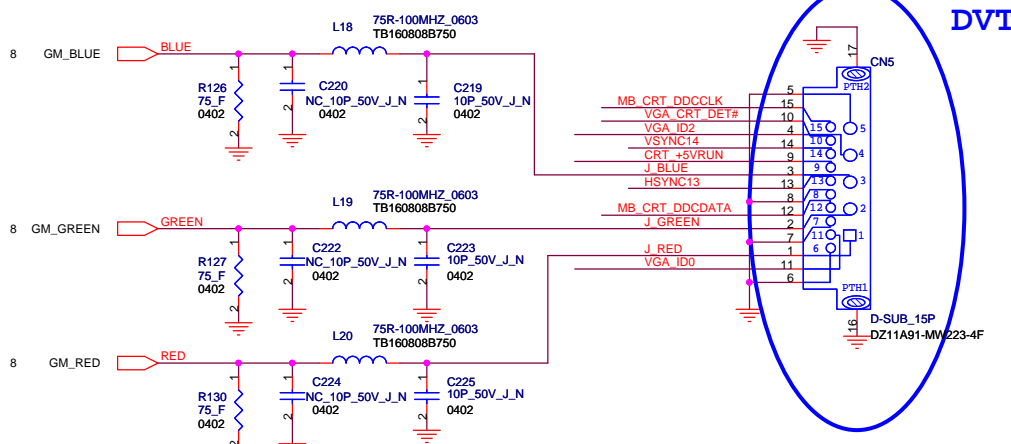




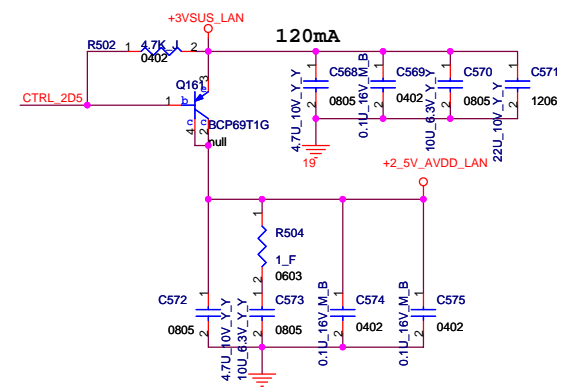
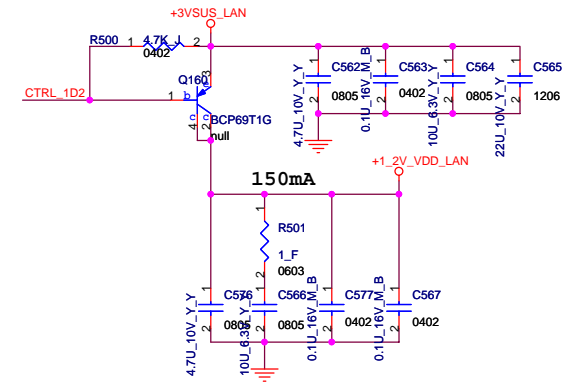
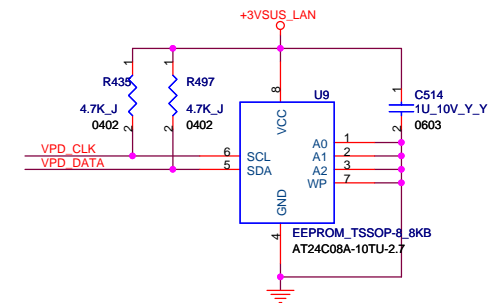
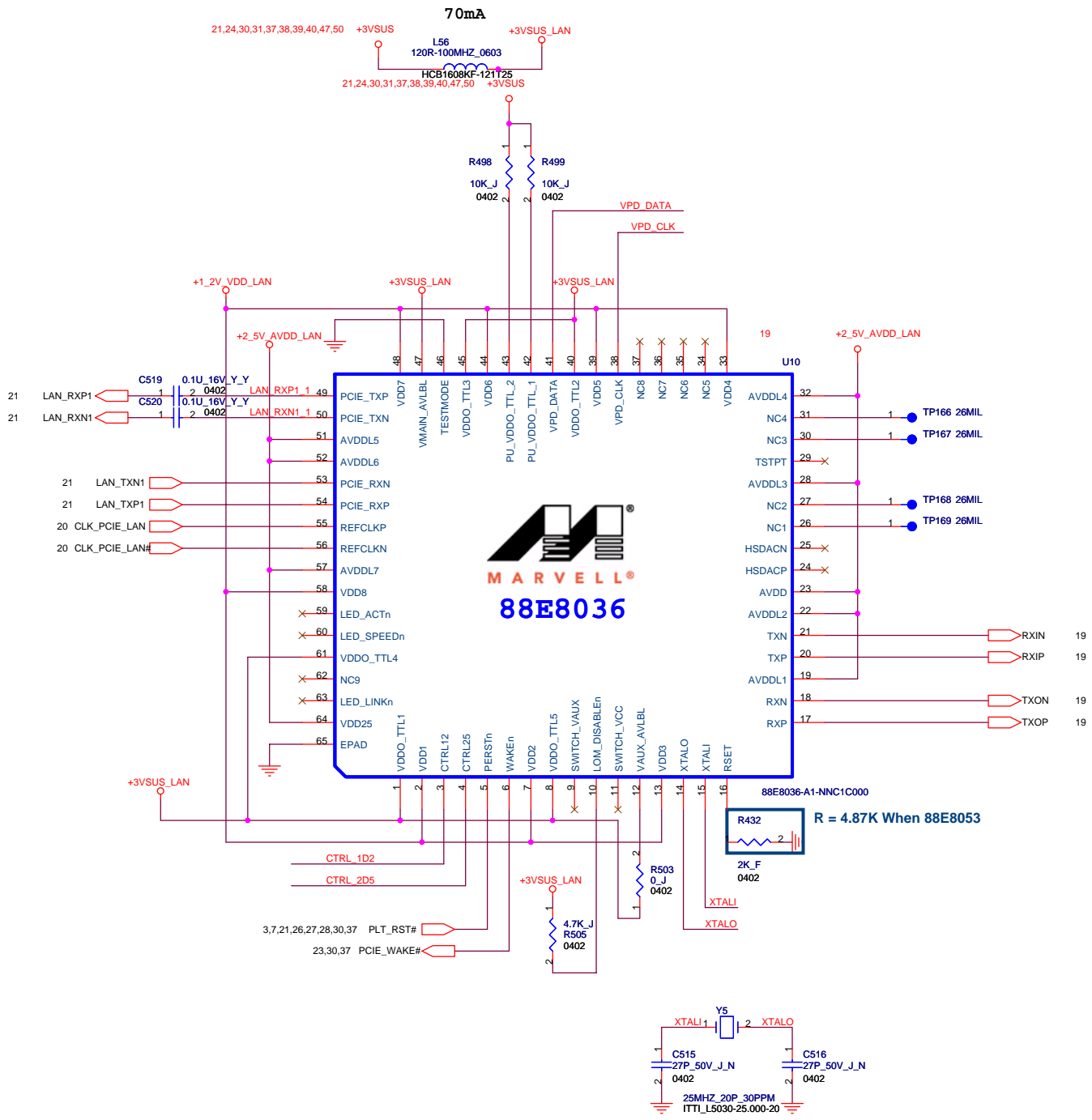
For EMI used

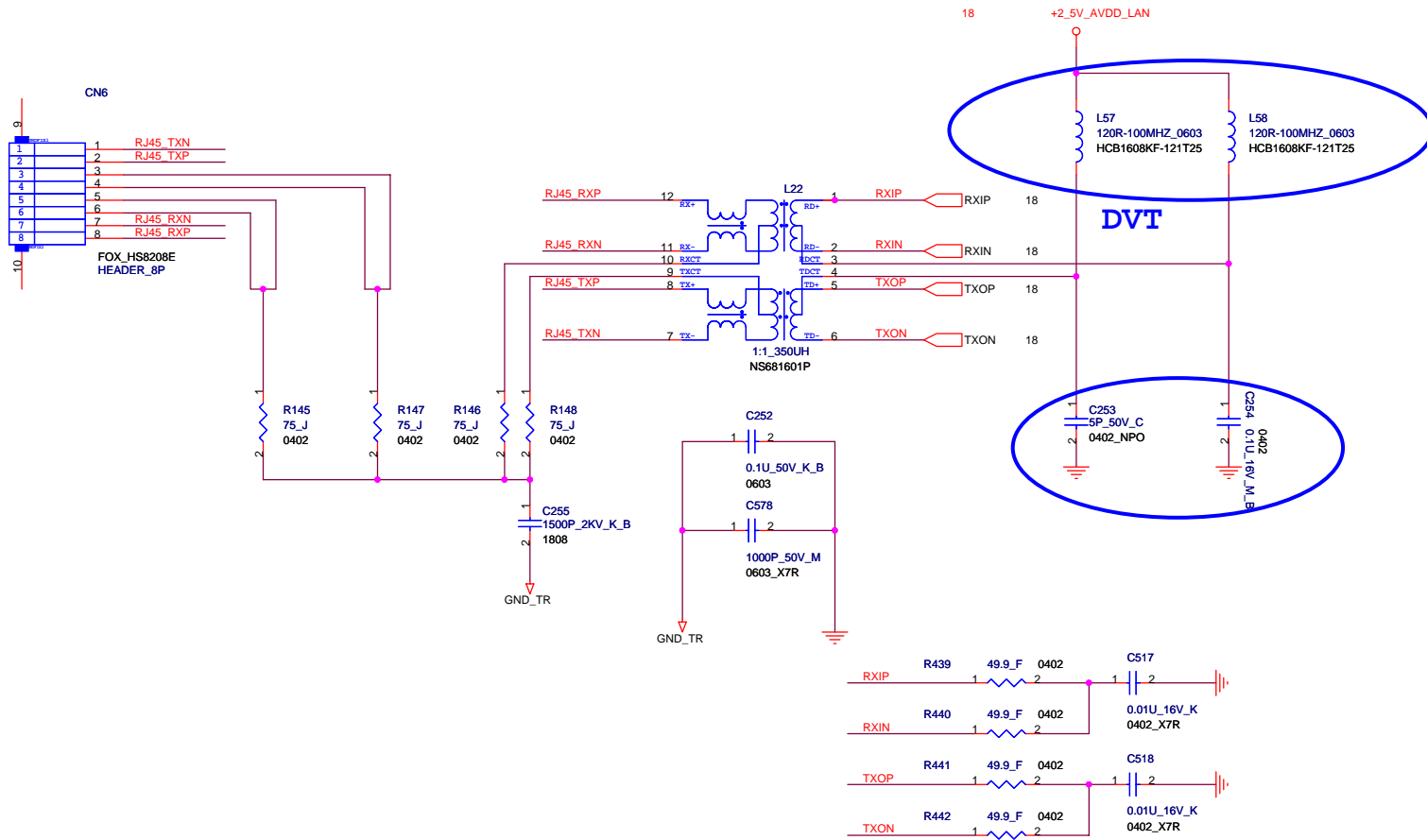


### CRT CONNECTOR



<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division		
File	CRT	
Size	Document Number	Rev
A3	MS70-1-01	0.30
Date:	Tuesday, June 13, 2006	Sheet 17 of 55

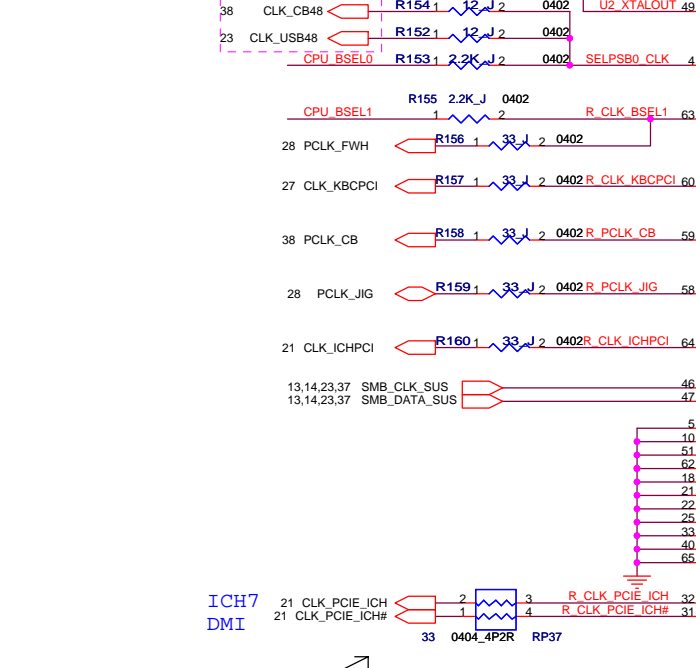




NC_10P_50V_E_N	2	1	CLK_CB48
NC_10P_50V_E_N	2	1	CLK_USB48
NC_10P_50V_E_N	2	1	CLK_KBCPCI
NC_10P_50V_E_N	2	1	PCLK_CB
NC_10P_50V_E_N	2	1	PCLK_FWH
NC_10P_50V_E_N	2	1	CLK_ICHPCI
NC_10P_50V_E_N	2	1	CLK_ICH14
NC_10P_50V_E_N	2	1	PCLK_JIG
NC_10P_50V_E_N	2	1	C256 0402
NC_10P_50V_E_N	2	1	C257 0402
NC_10P_50V_E_N	2	1	C258 0402
NC_10P_50V_E_N	2	1	C265 0402
NC_10P_50V_E_N	2	1	C266 0402
NC_10P_50V_E_N	2	1	C267 0402
NC_10P_50V_E_N	2	1	C268 0402
NC_10P_50V_E_N	2	1	C271 0402

close to clk gen (For EMI)

Length as short as possible.



ICH7 DMI

06/17  
CLK\_PCIE\_ICH changed to SRCLK7  
CLK\_DOCK\_LAN changed to SRCLK8  
SW Note: datasheet page13 Byte8.1 => SRCLK7 should be configured as "Not Controlled"

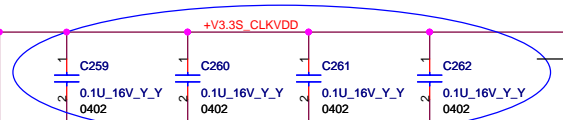
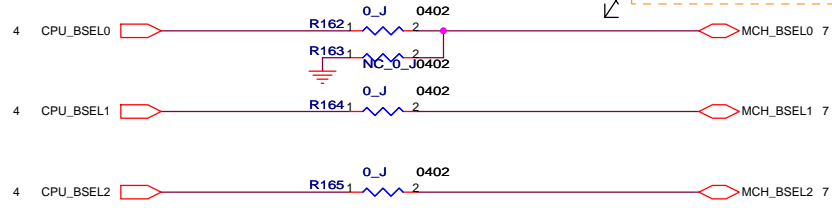
SM bus Address 6SLPR321BKLF  
1101001 (ICH7)  
For clock generator

06/09  
DEL pull-up resistor R80-82  
pull-down resistor R85,R88  
del R84,R87,R90

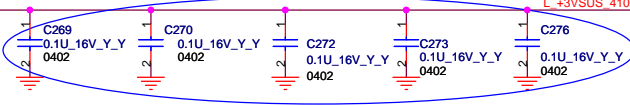
06/16  
ICS have recognized, FSLA/FSLB setting is different from CK410M spec. But MS10 will not use 100MHz, For test purpose, please move R91 from MCH\_BSEL2 to MCH\_BSEL0, and mount R89.

FSB Frequency Table:

FSLB	FSLA	CPU SRC[7:0]	PCI
0	0	100	100
0	1	133	100
1	0	200	100
1	1	166	100



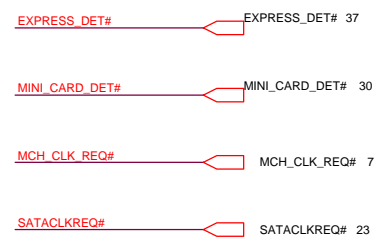
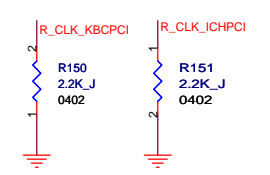
Layout note:  
Place 1 cap close to each pin



06/16  
pin53/59/60/64 with internal pull-up resistor  
No Stuff Pull-up Resistor

06/09  
CLKREQ with internal pull-up resistor  
No Stuff Pull-up Resistor

Pin Straps	
Pin	Function
pin53	pin 11/12
0	SRCLK0
1	27MHz (v)
pin59	pin 15/16
0	SRCLK0
1	SATA (v)
pin60	pin 37/38
0	SRCLK8 (v)
1	CPU 2 ITP
pin64	pin 13/14
0	LDCCLK_SS (CA)
1	SRCLK1 (NV)

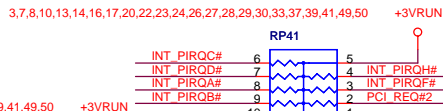
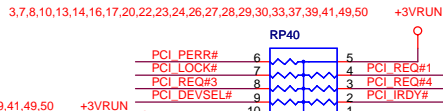
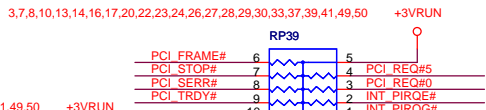


06/09  
CLKREQ with internal pull-up resistor  
No Stuff Pull-up Resistor

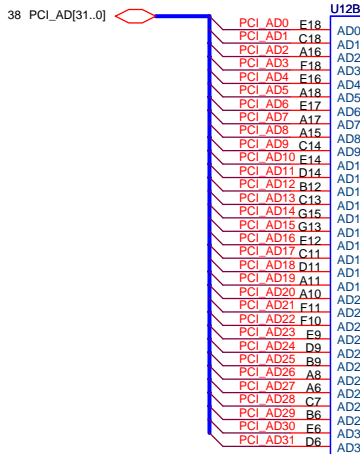
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

**CLOCK GEN**

Size A3	Document Number MS70-1-01	Rev 0.30
Date: Tuesday, June 13, 2006	Sheet 20	of 55

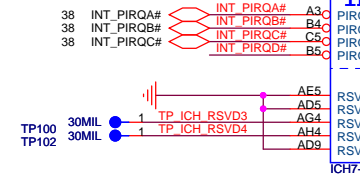


**PCI Pullups**



**Interrupt I/F**

**MISC**

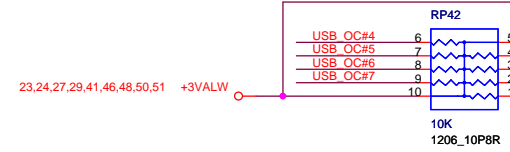
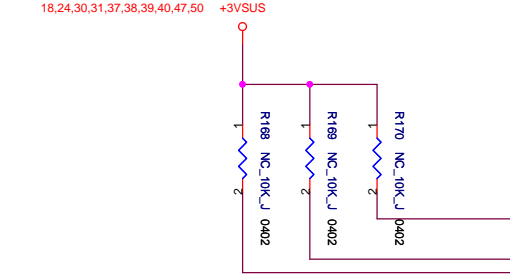


**Strap for Boot-BIOS**

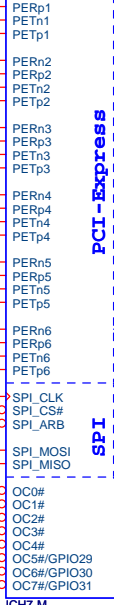
	GNT5#	GNT4#
LPC(Default)	Hi	Hi
PCI	Hi	Low

Place within 500 mils of ICH

Place within 500 mils of ICH and don't routing next to high speed signals



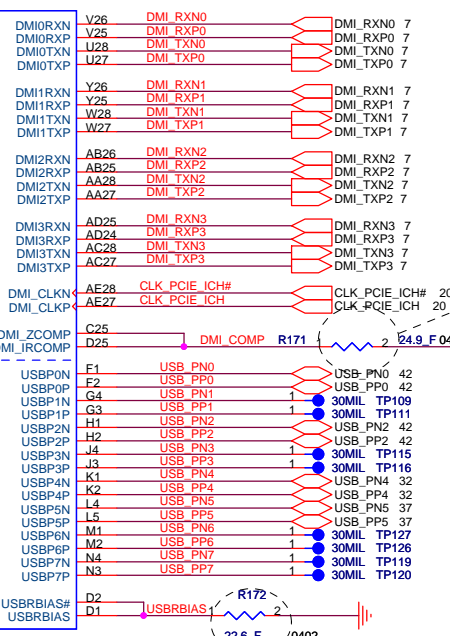
**U12D**



**Direct Media Interface**

**SPI**

**USB**



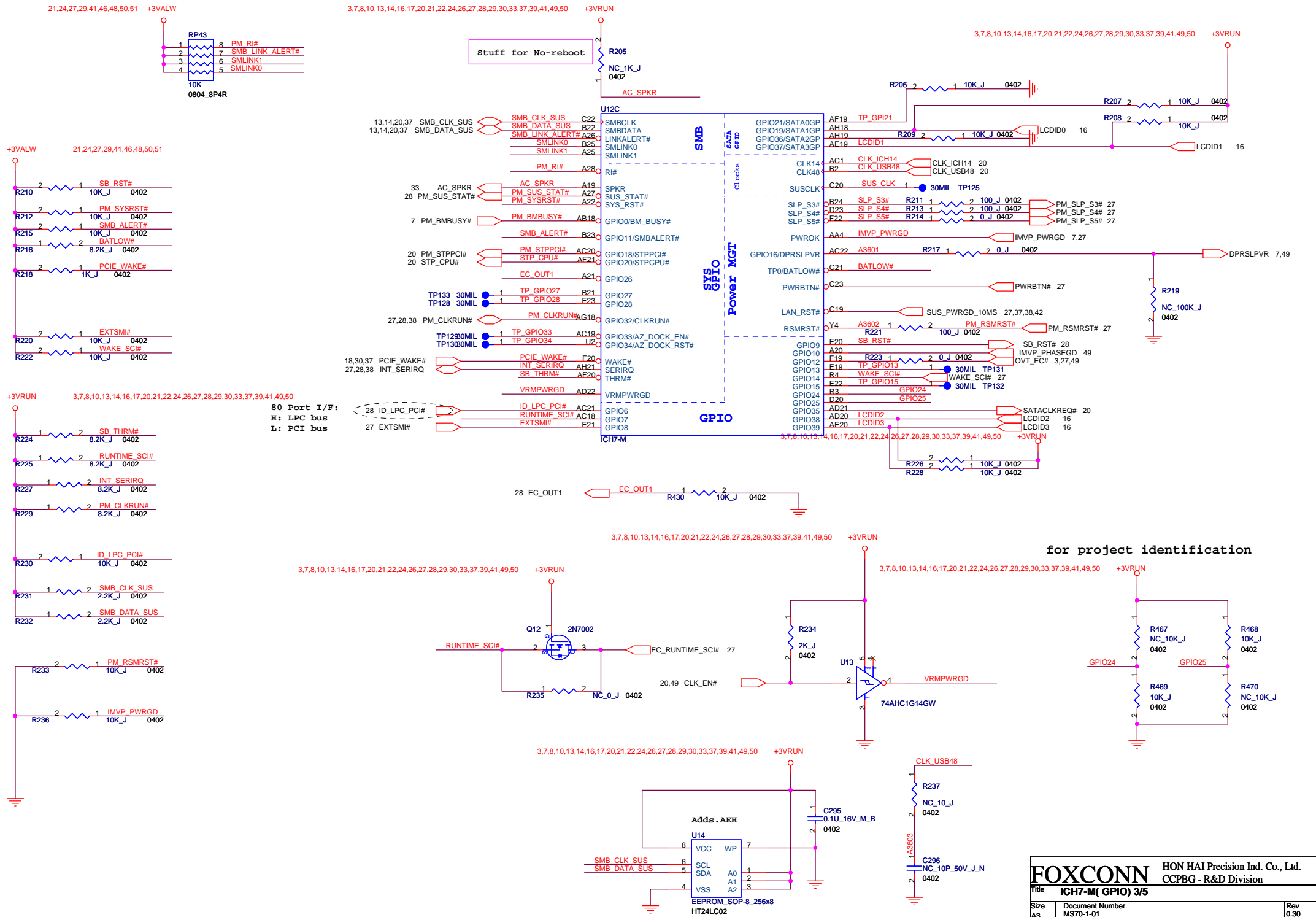
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
 CCPBG - R&D Division

Title: **ICH7-M( PC/DMI/USB/PCIE ) 1/5**

Size A3	Document Number MS70-1-01	Rev 0.30
---------	---------------------------	----------

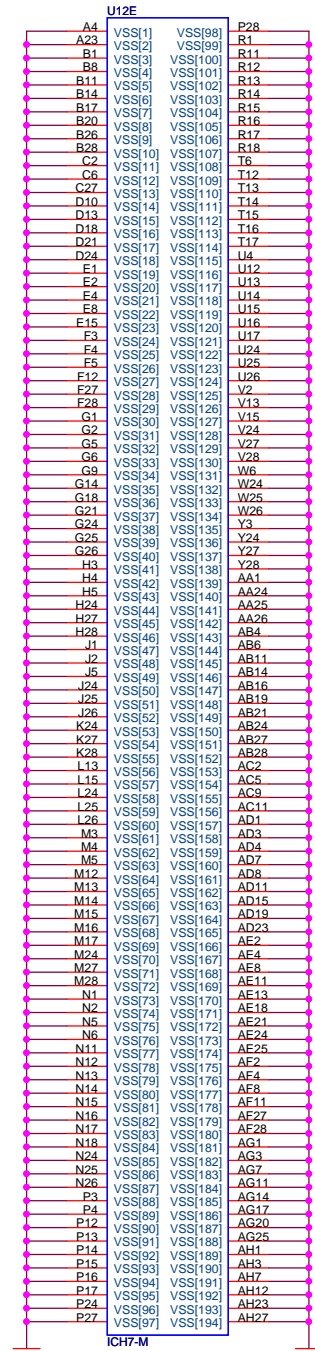
Date: Tuesday, June 13, 2006 | Sheet 21 of 55



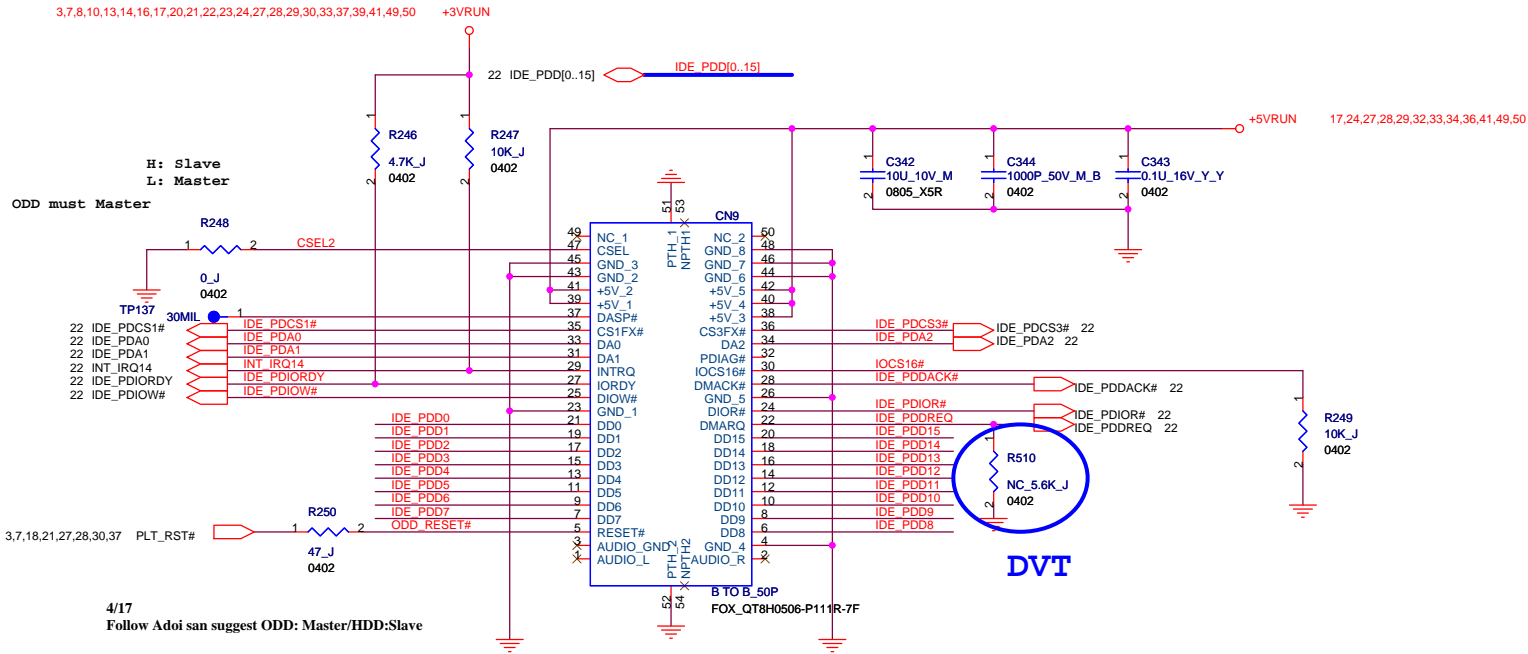
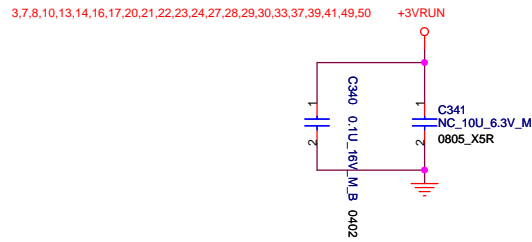
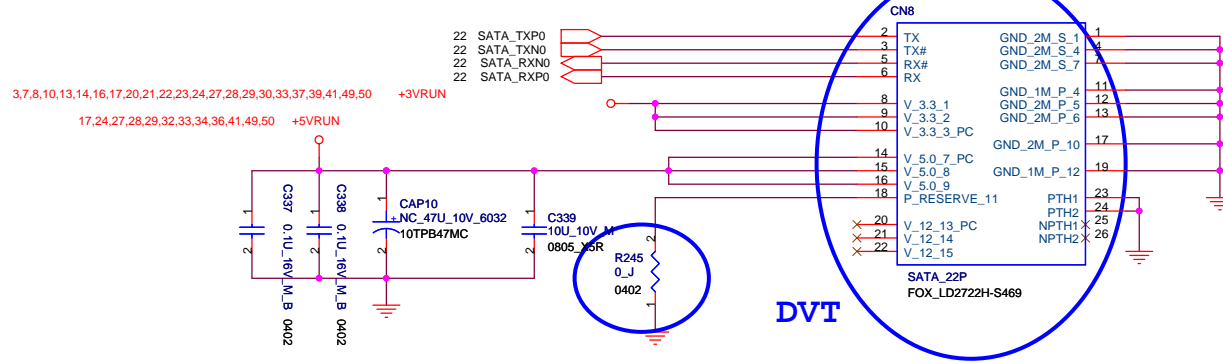




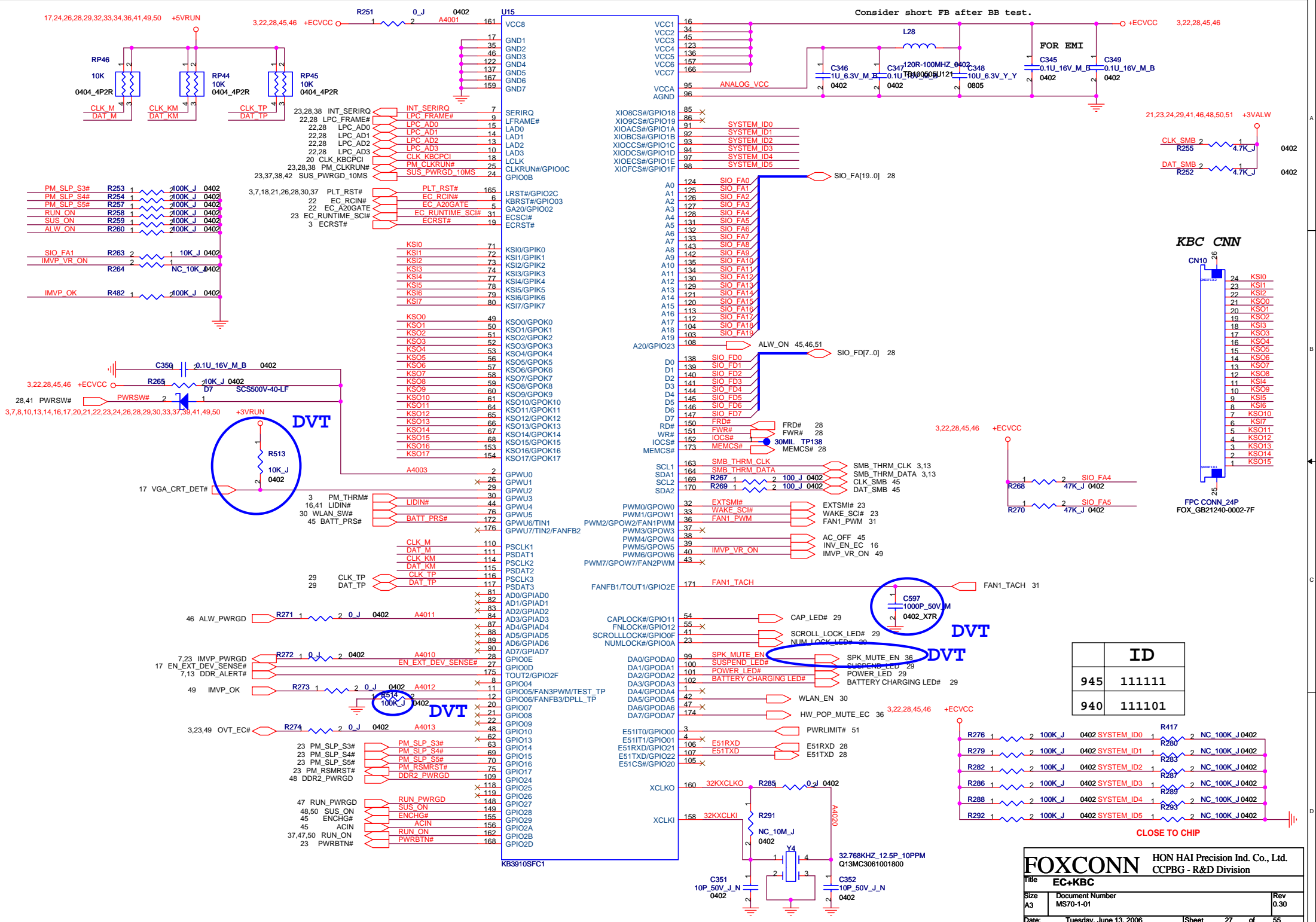




# SATA HDD CONN



# CD-ROM CONN



ID	
945	111111
940	111101

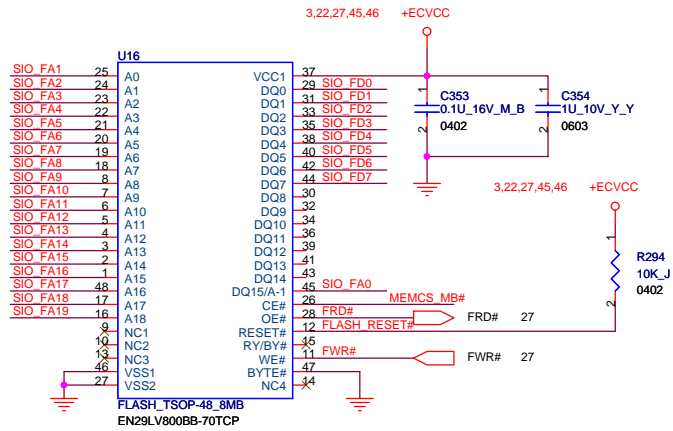
**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

Title: **EC+KBC**

Size: A3 | Document Number: MS70-1-01 | Rev: 0.30

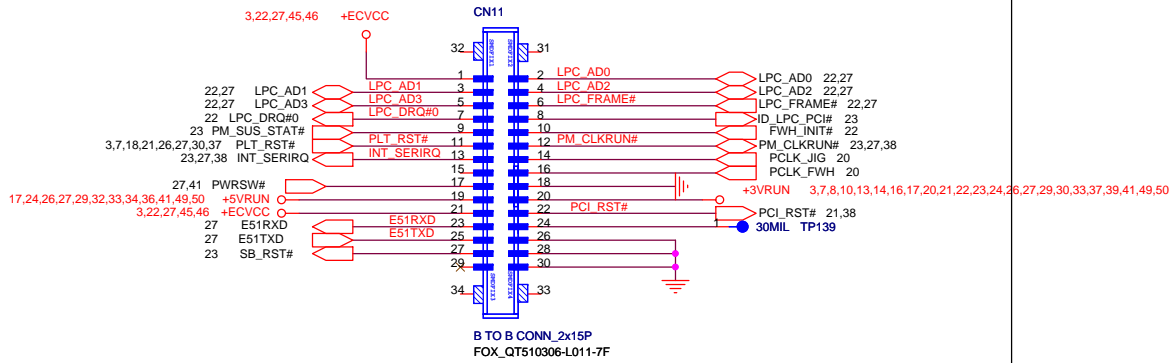
Date: Tuesday, June 13, 2006 | Sheet: 27 of 55

27 SIO\_FA[19..0]  
27 SIO\_FD[7..0]

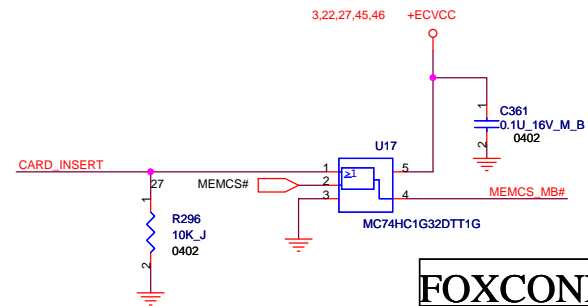
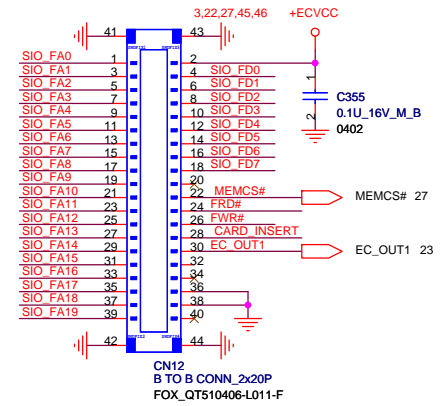


**FLASH BIOS**

**JIG-120**

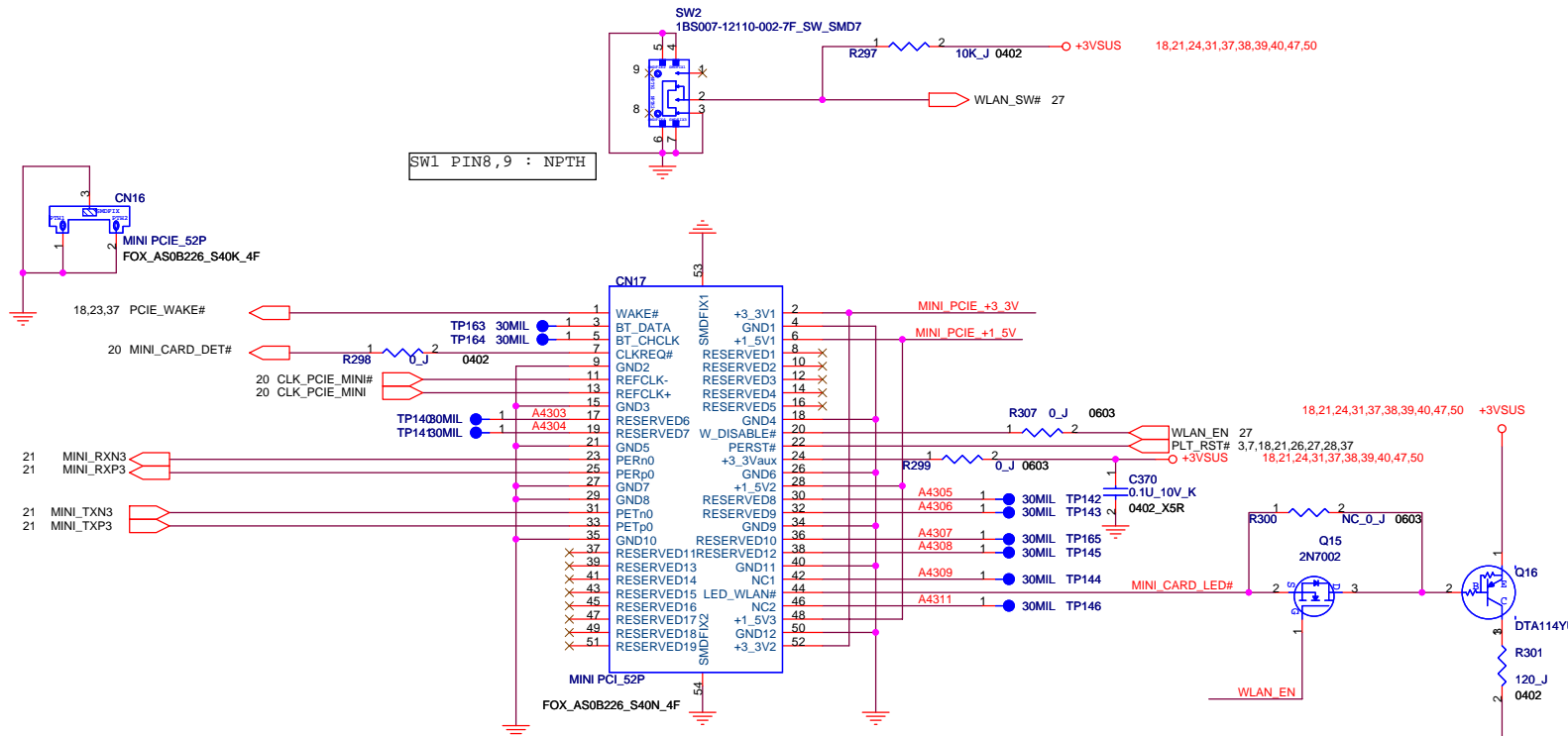


**X-BUS**



<b>FOXCONN</b> HON HAI Precision Ind. Co., Ltd.		
CCPBG - R&D Division		
Title <b>Flash ROM/X-Bus/LID SW#</b>		
Size A3	Document Number MS70-1-01	Rev 0.30
Date: Tuesday, June 13, 2006	Sheet 28	of 55



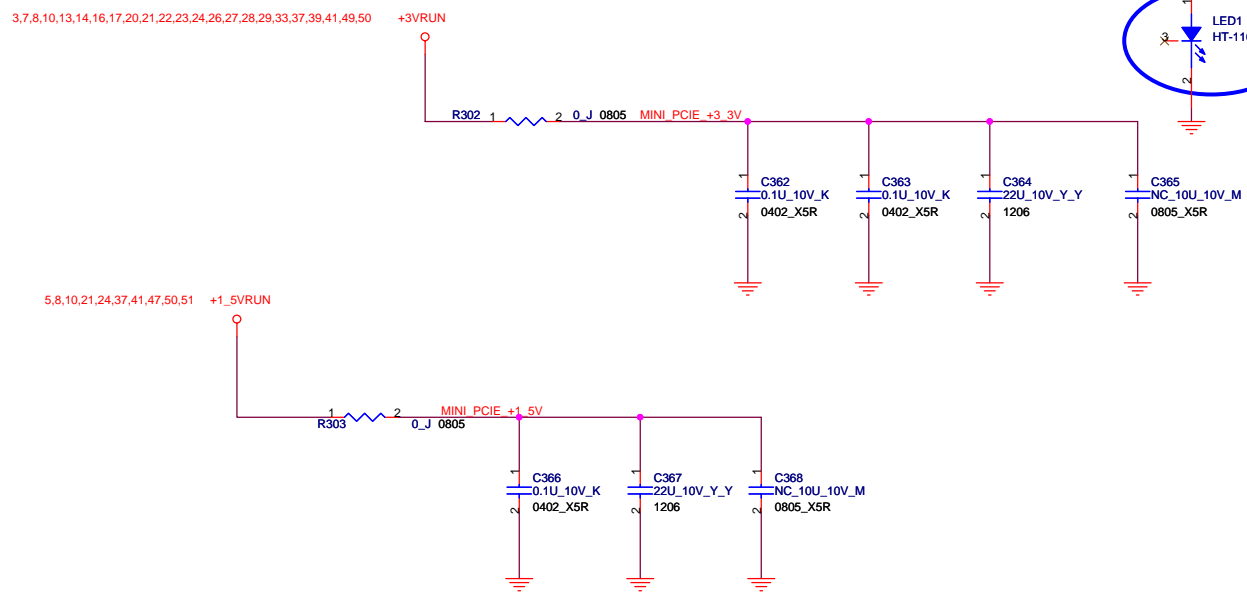
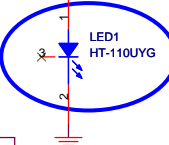


SW1 PIN8,9 : NPTH

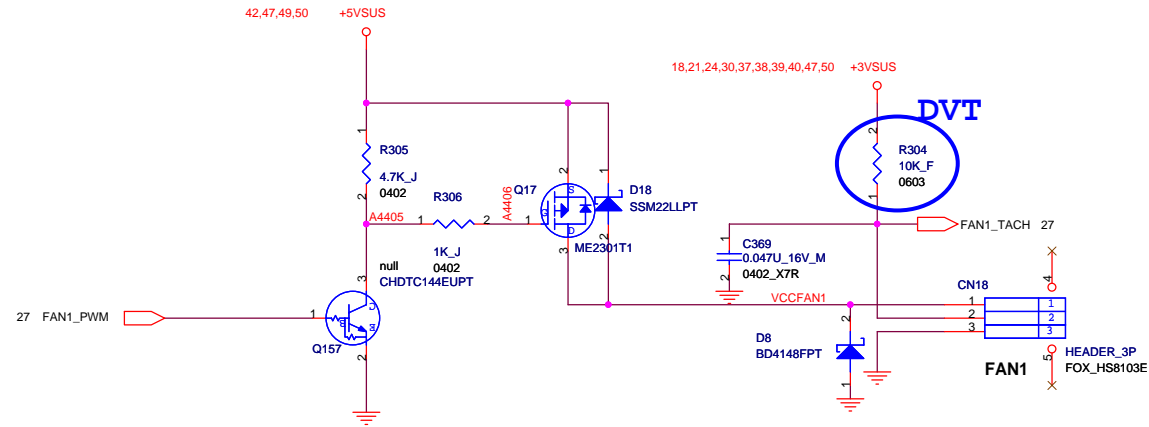
LED IF SPEC:  
20mA (TYP), 30mA (MAX)

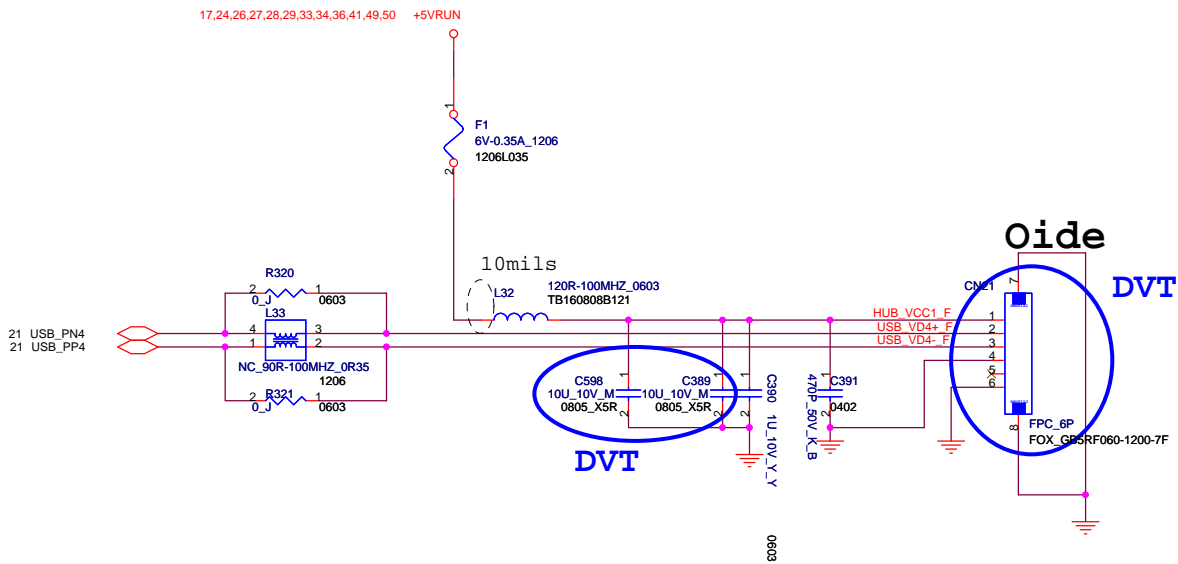
**WLAN LED DVT**

Yellow Green

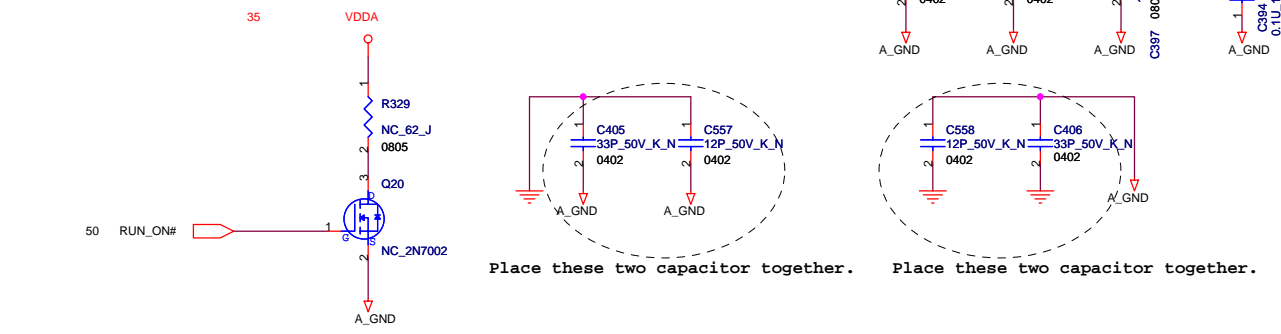
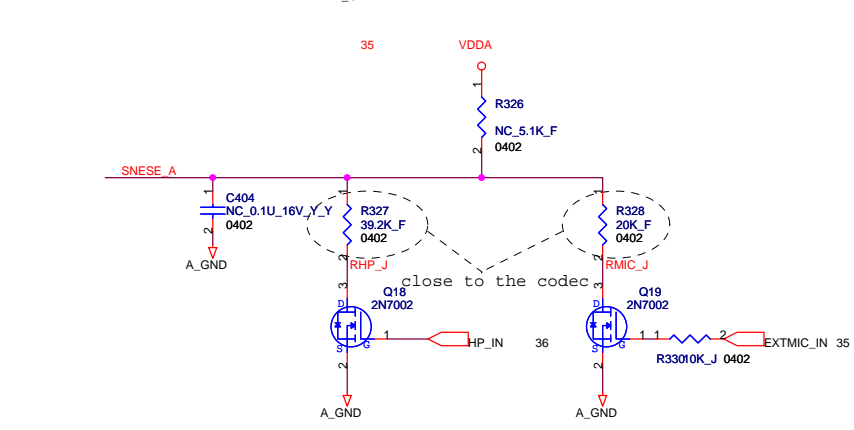
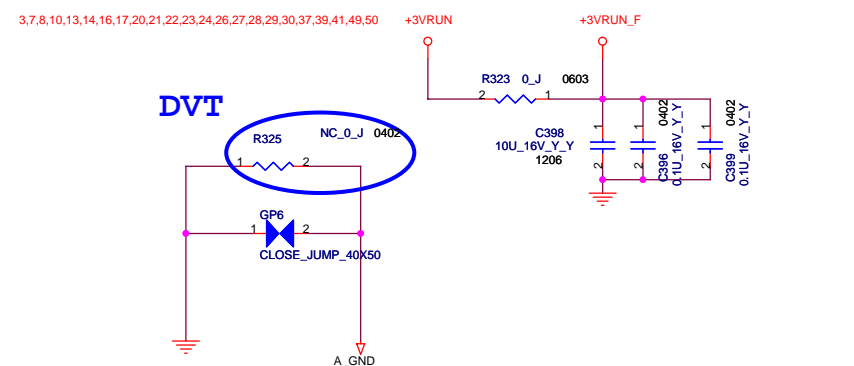
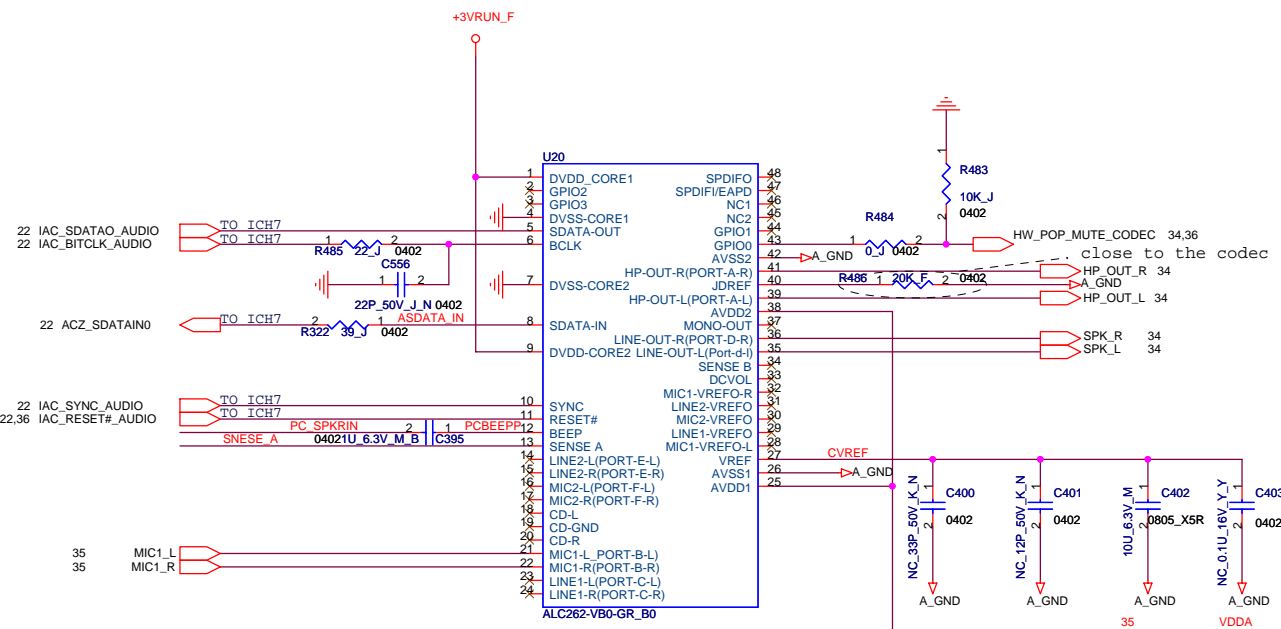


# FAN1

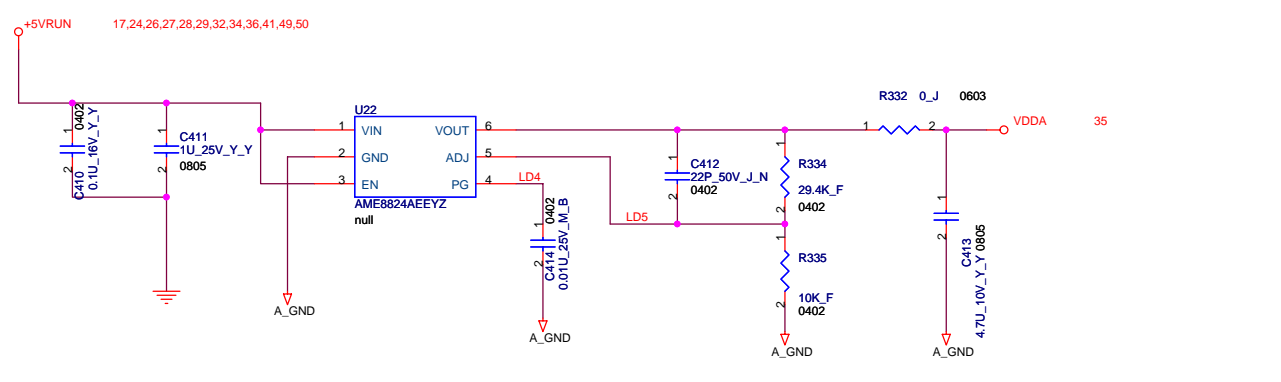


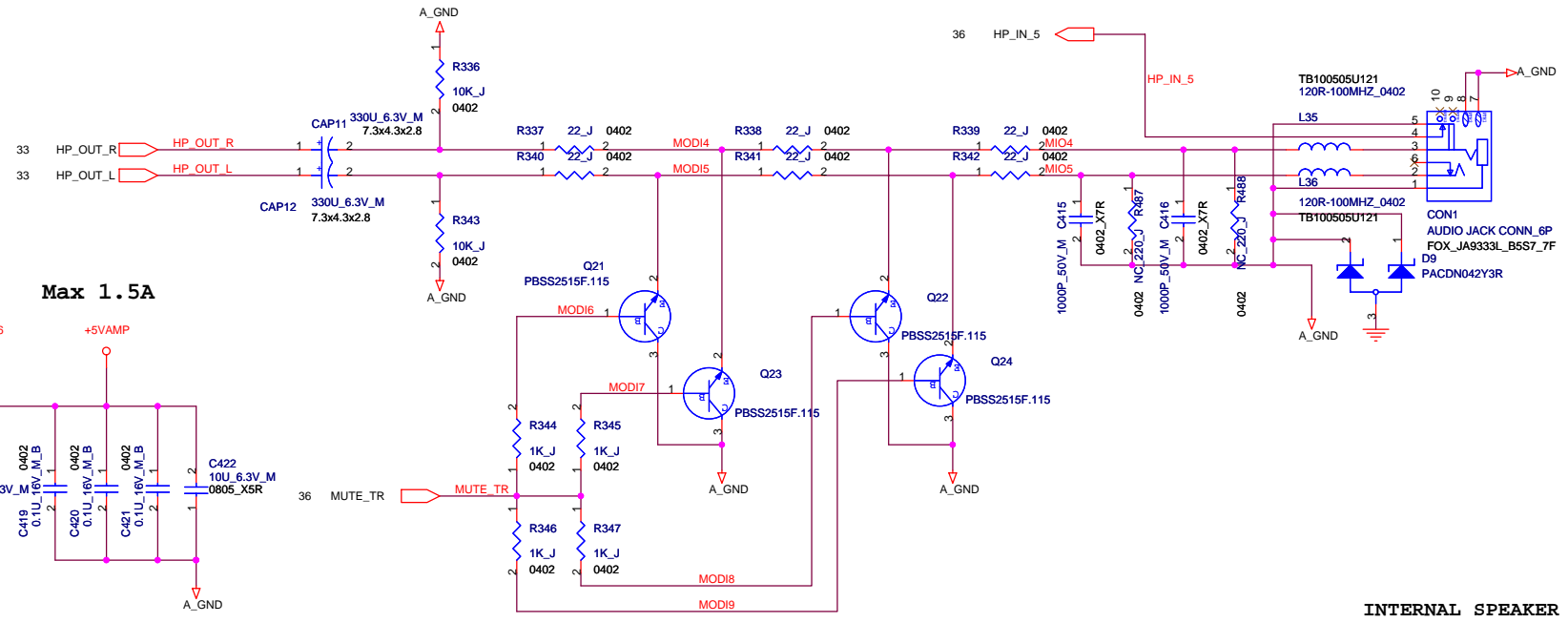






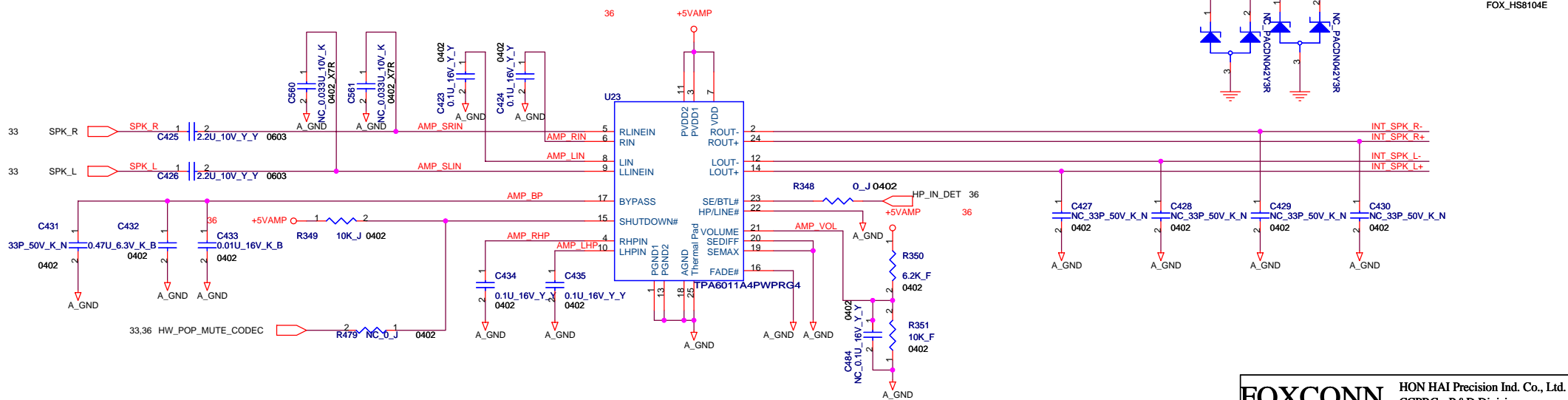
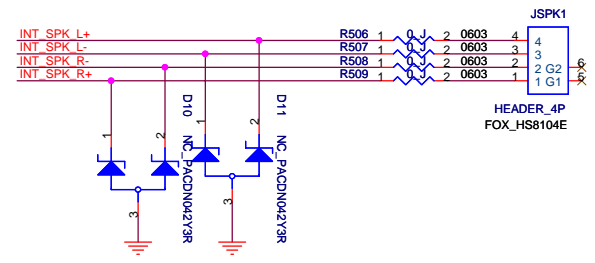
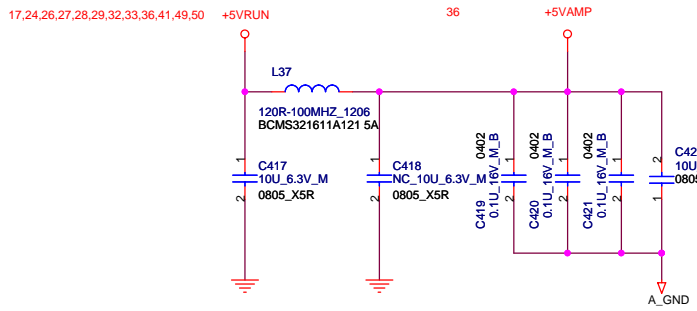
AUDIO POWER(Change to 4.75V/200mA)

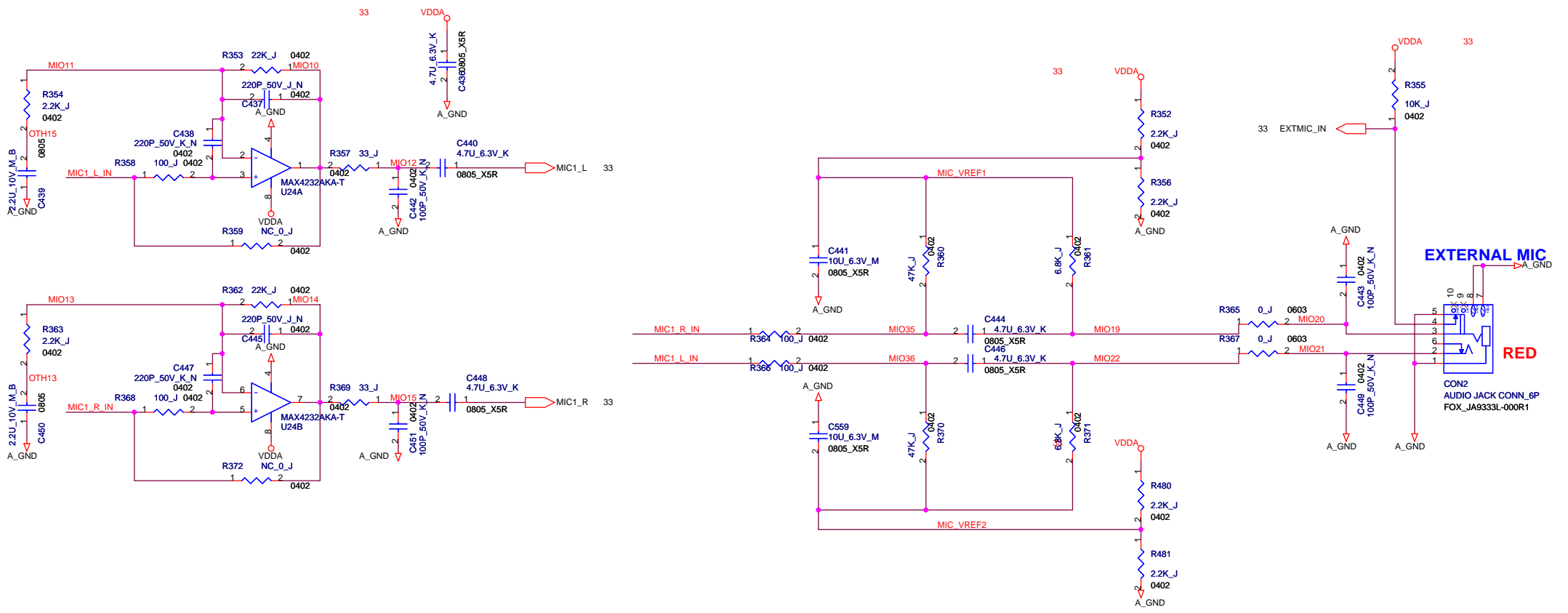


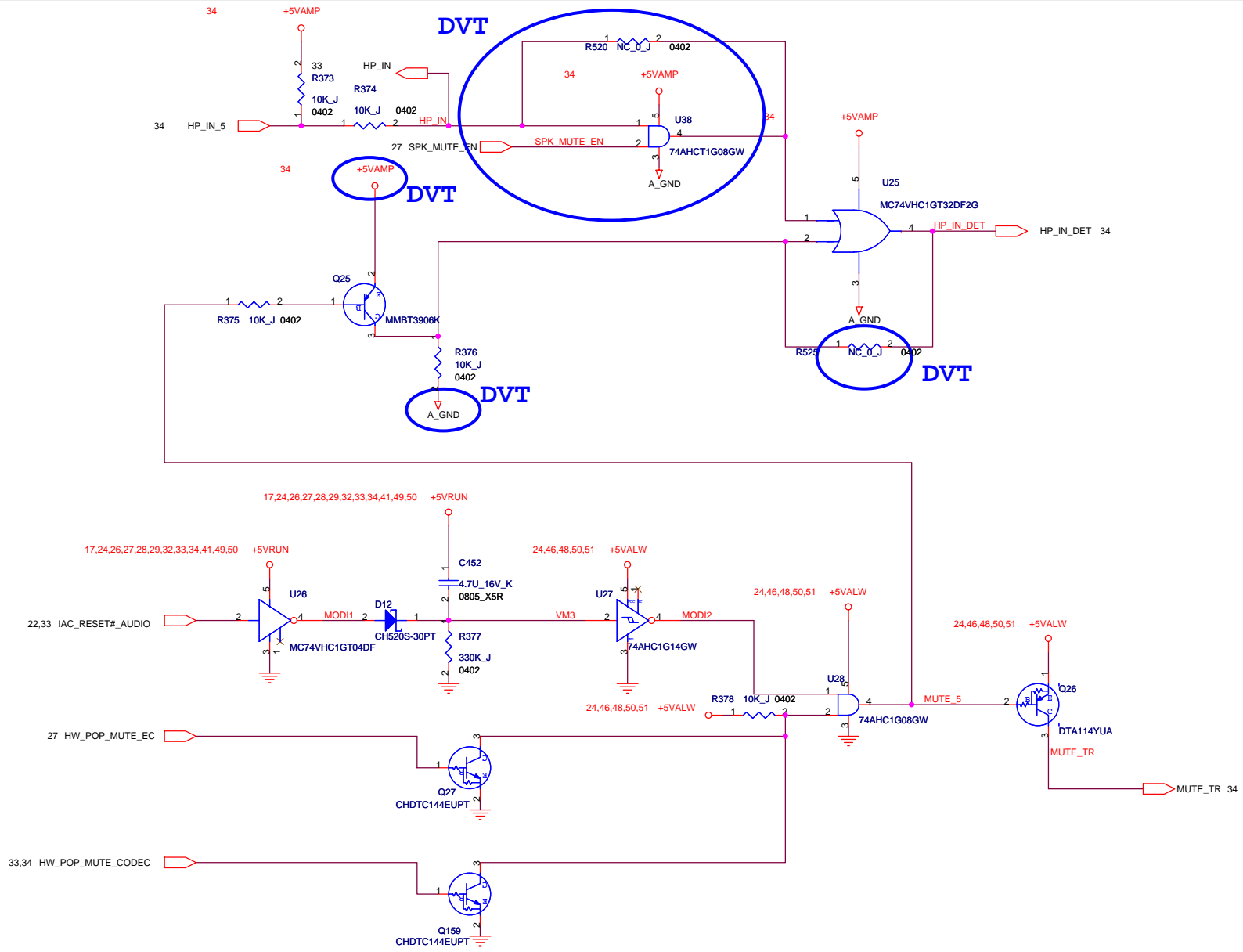


Max 1.5A

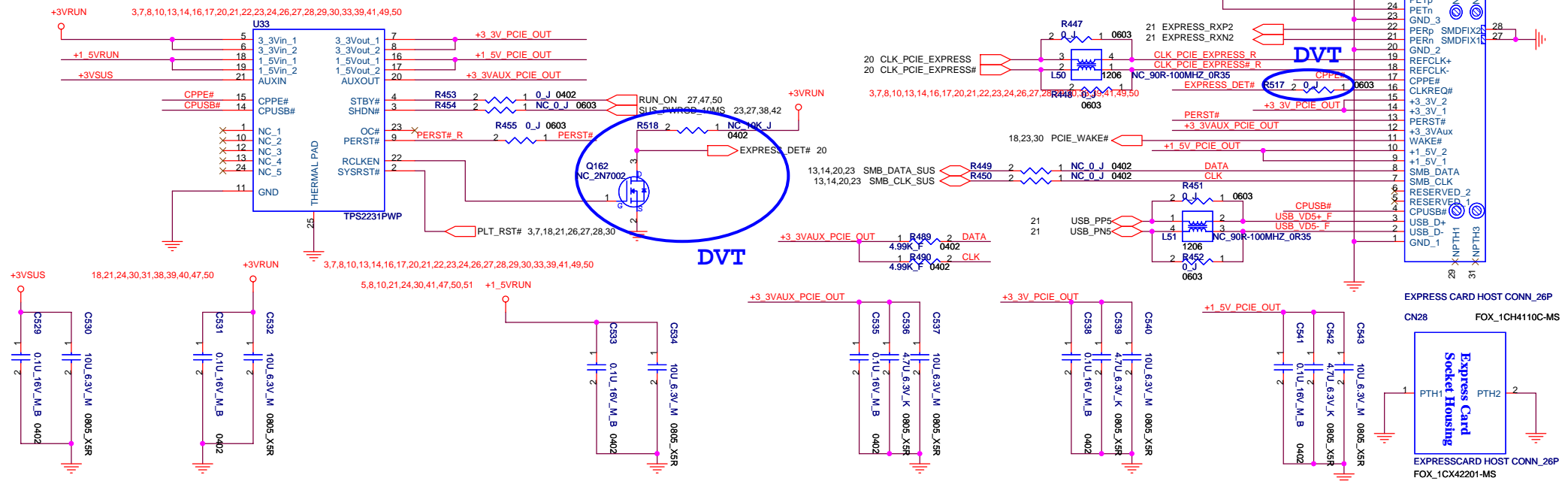
INTERNAL SPEAKER



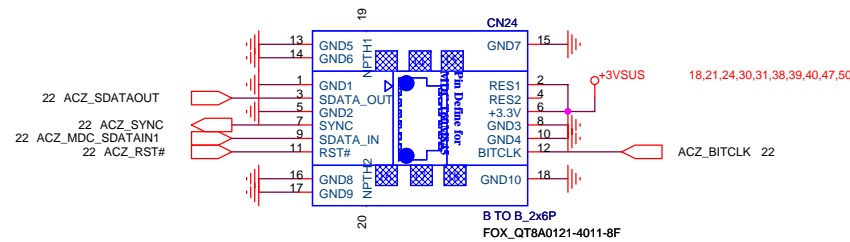


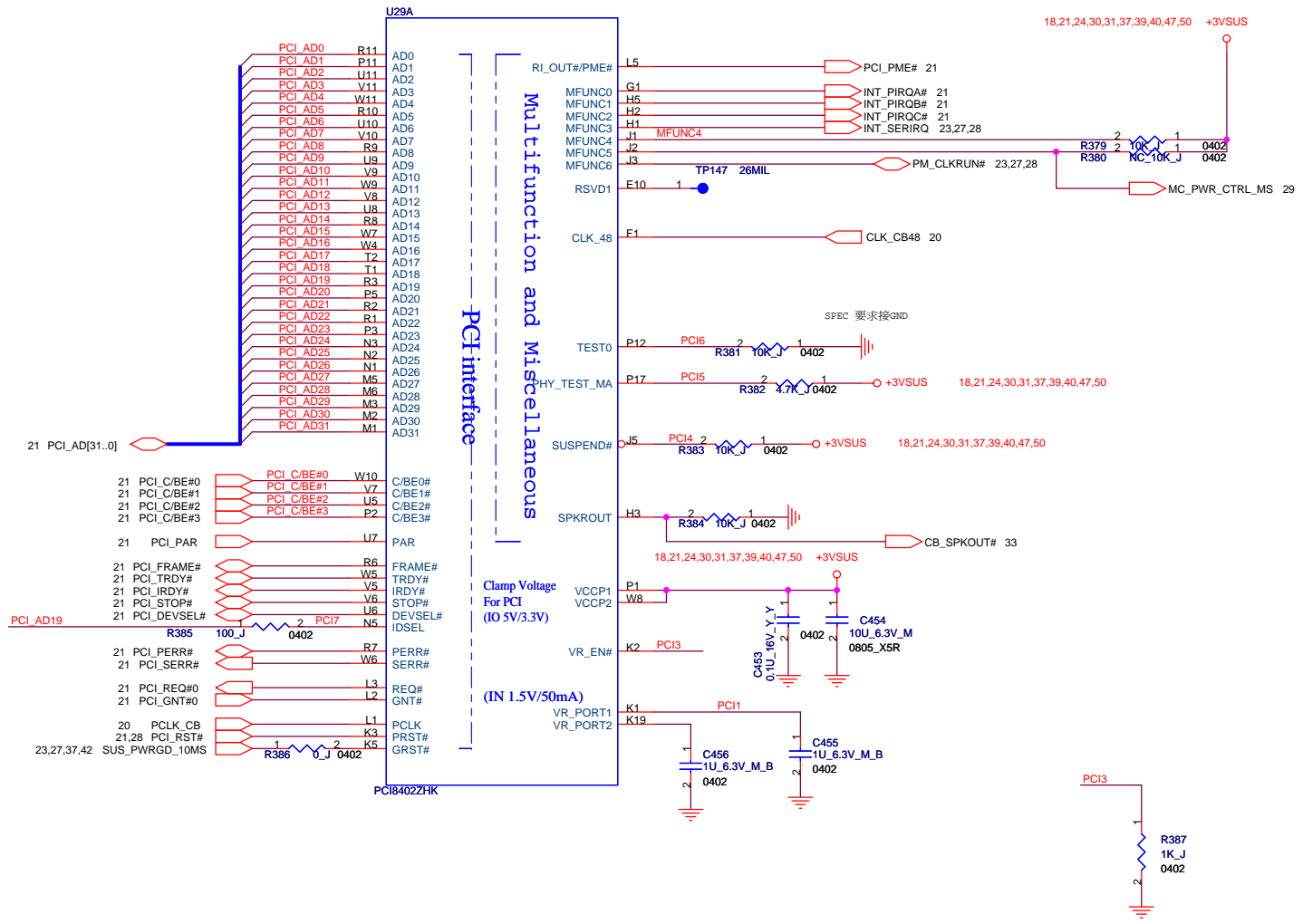


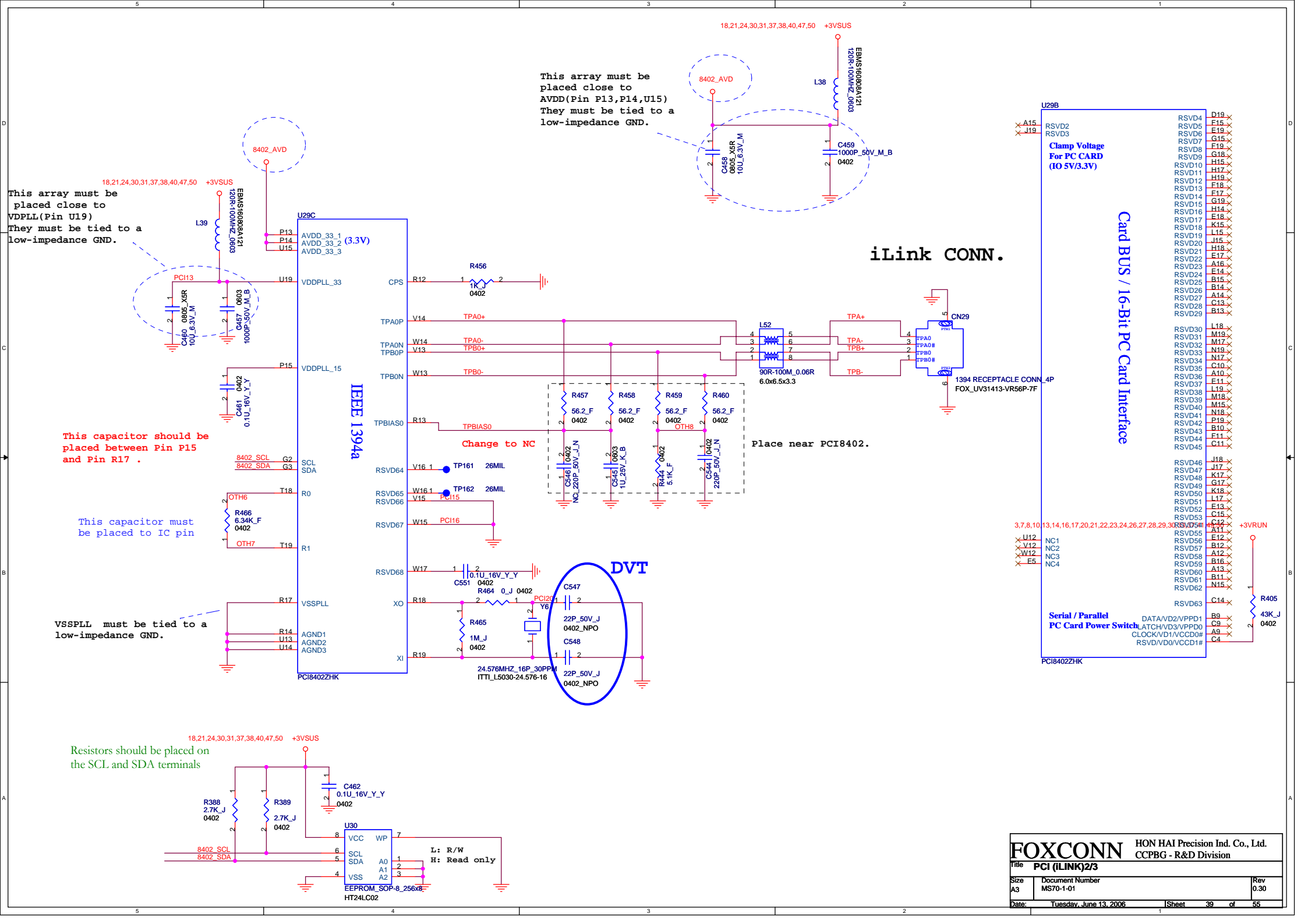
# EXPRESS CONN



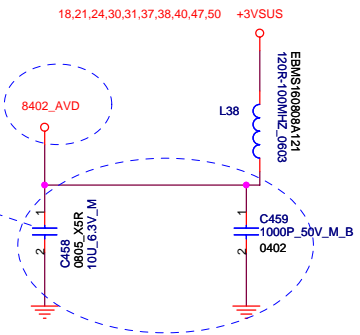
# MDC CONN.



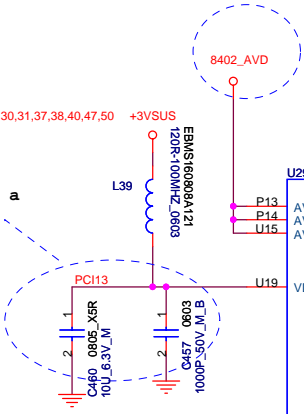




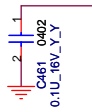
This array must be placed close to AVDD (Pin P13, P14, U15) They must be tied to a low-impedance GND.



This array must be placed close to VDDPLL (Pin U19) They must be tied to a low-impedance GND.



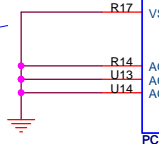
This capacitor should be placed between Pin P15 and Pin R17.



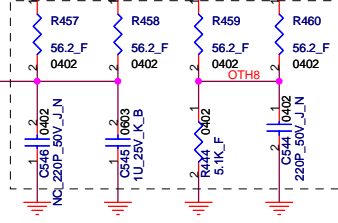
This capacitor must be placed to IC pin



VSSPLL must be tied to a low-impedance GND.

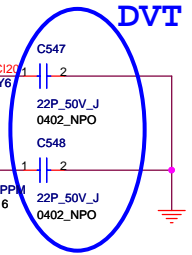


Change to NC

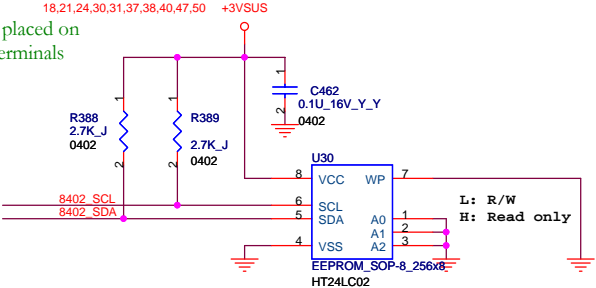


Place near PCI8402.

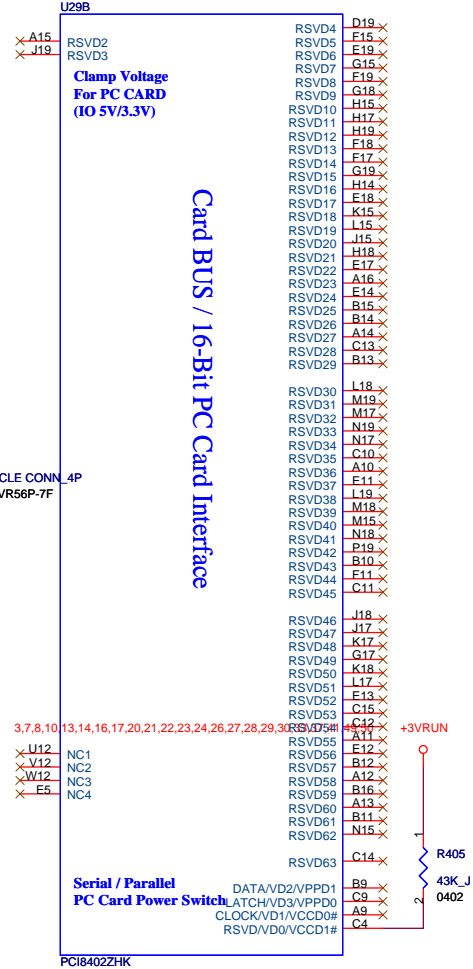
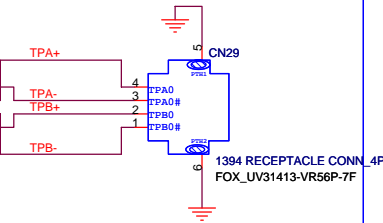
DVT

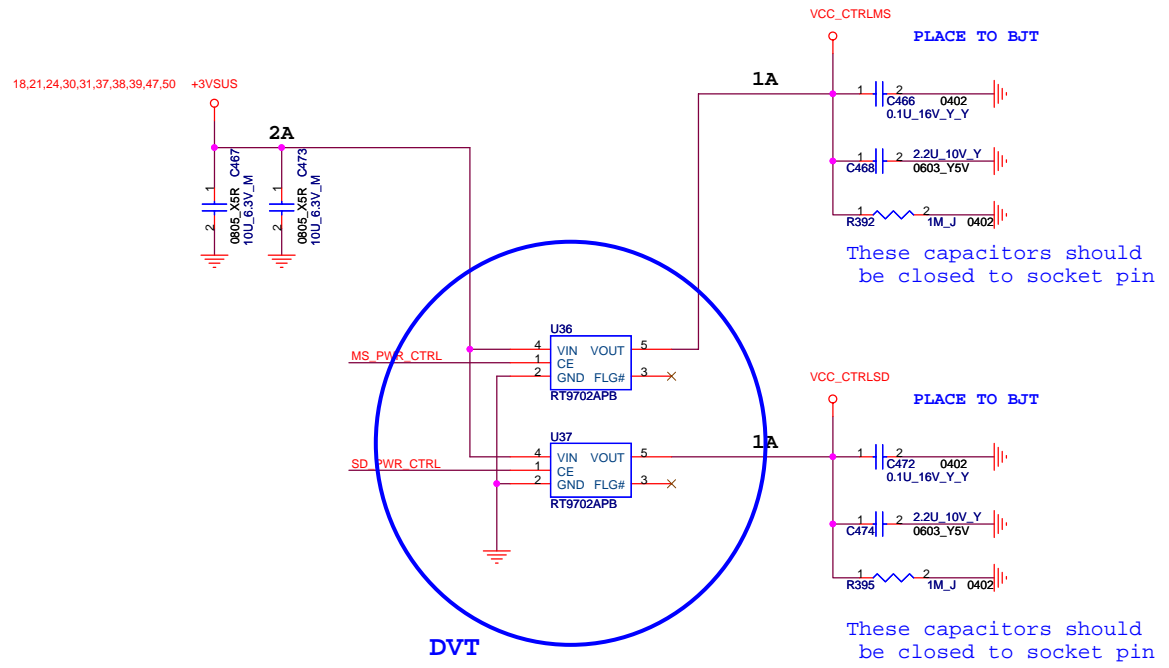
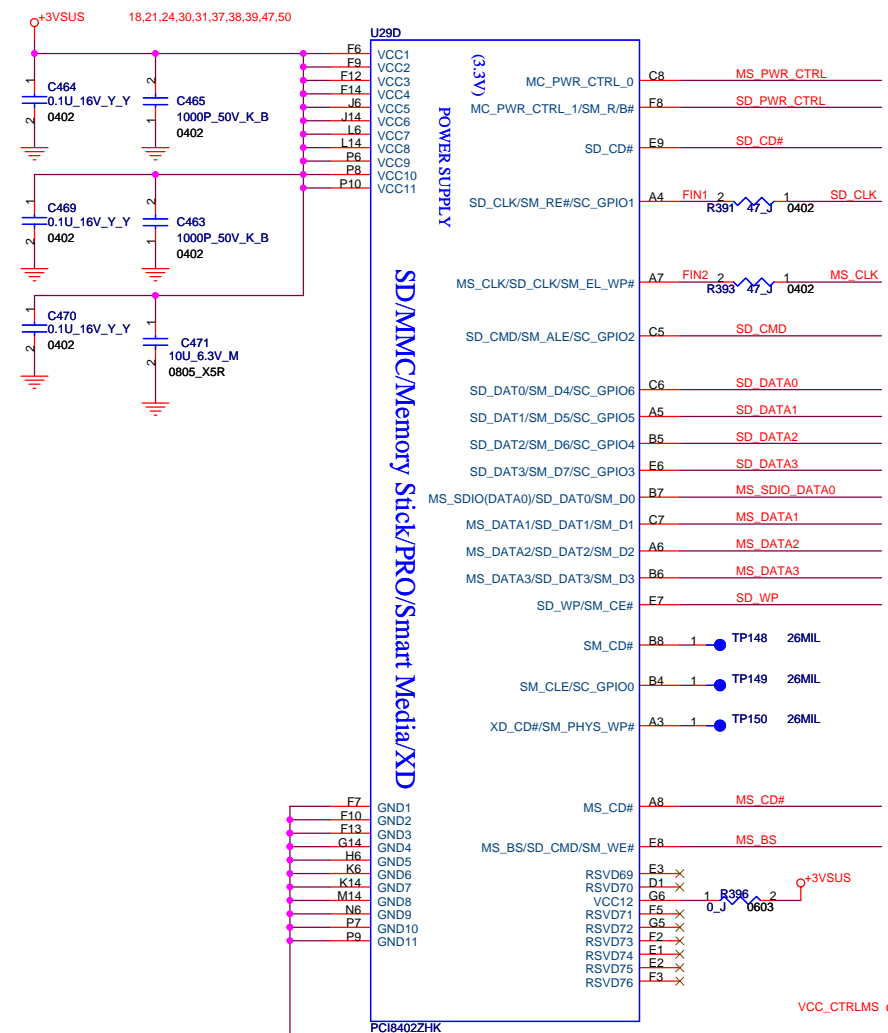


Resistors should be placed on the SCL and SDA terminals

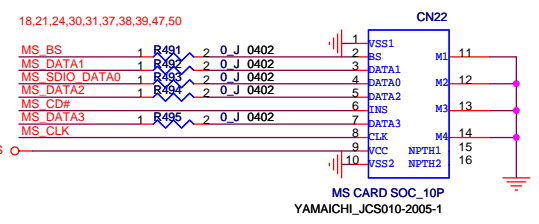


iLink CONN.

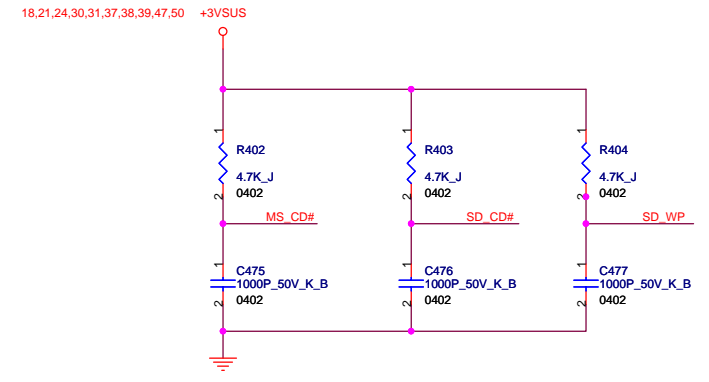
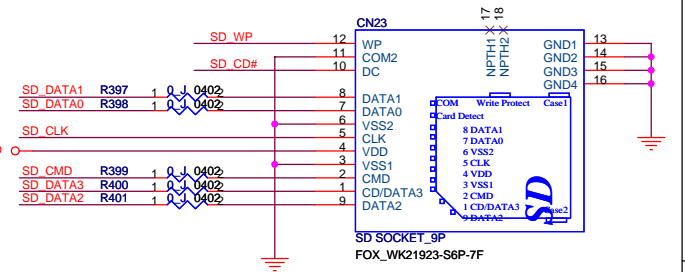




**MS STD/DUO CONN.**

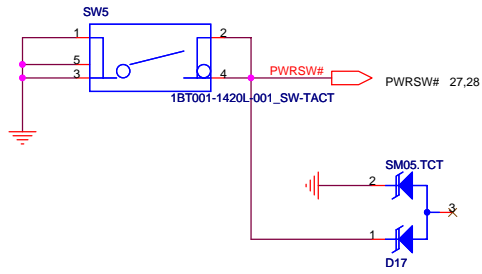


**SD CONN.**

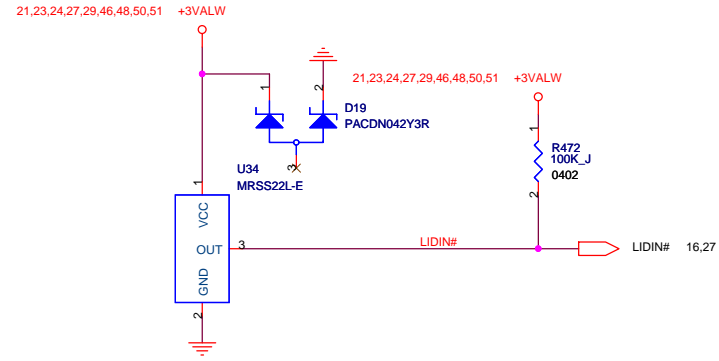




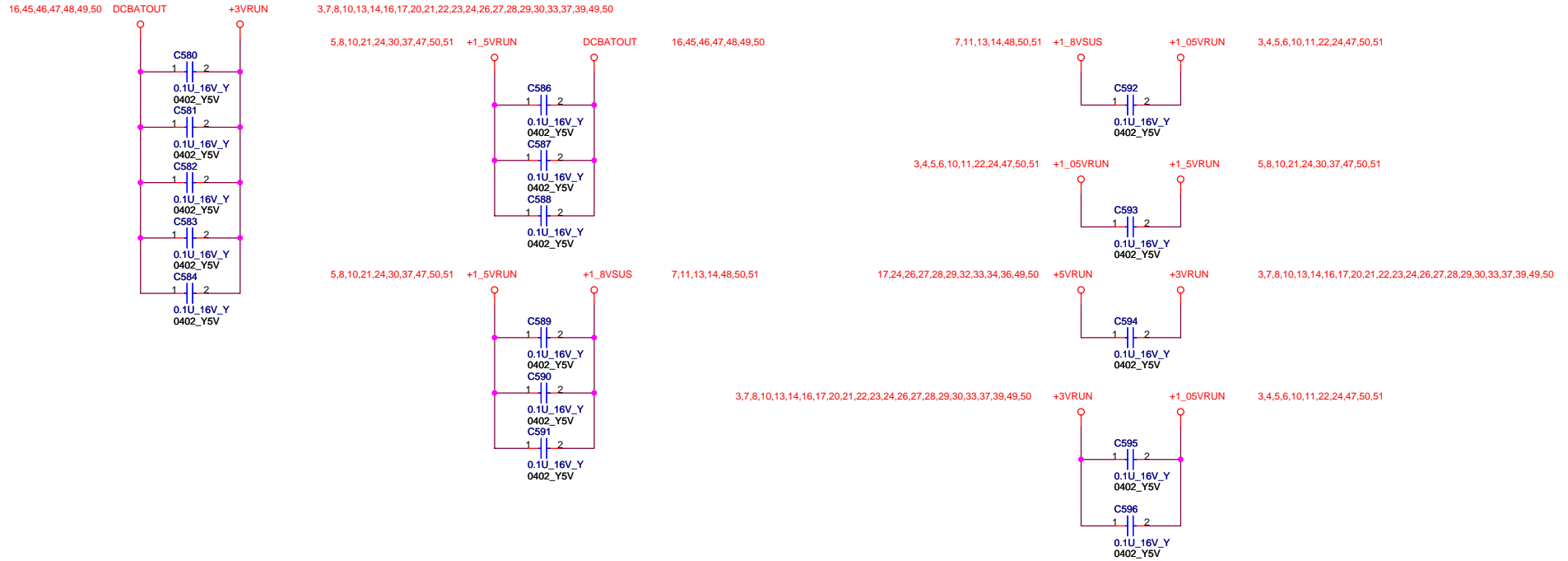
### POWER BUTTON



### LID Switch

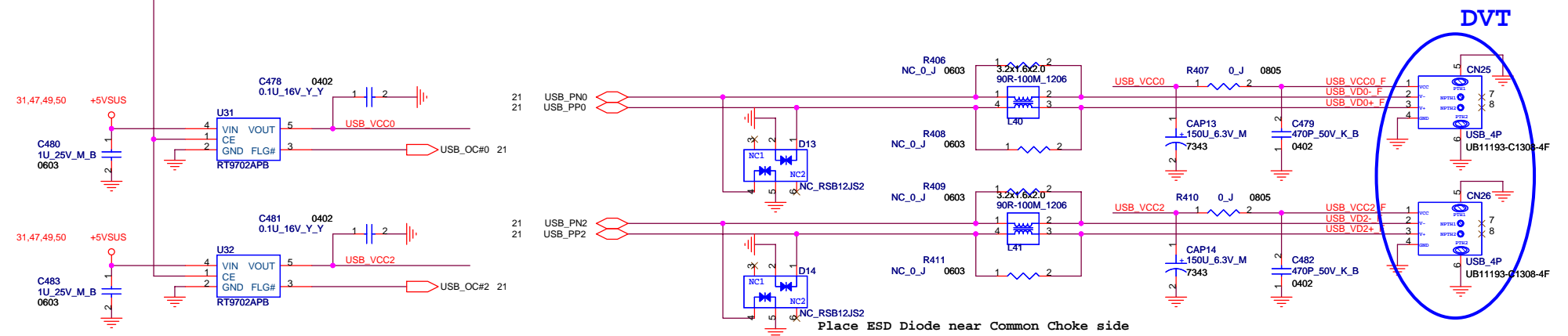


### EMI CAP

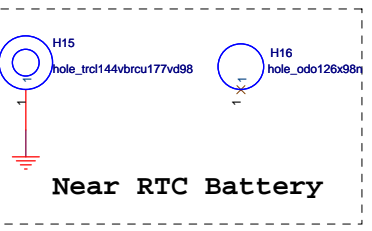
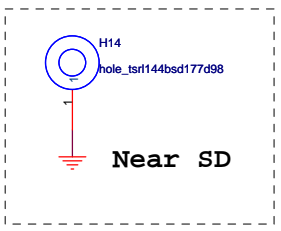
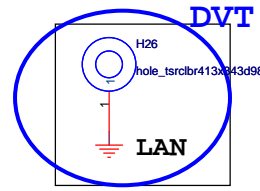
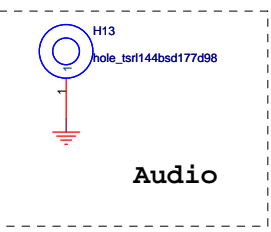
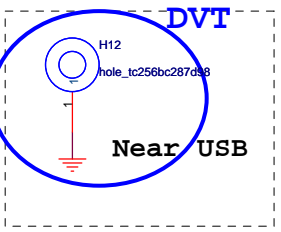
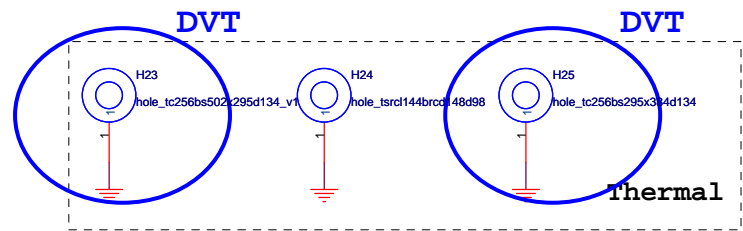
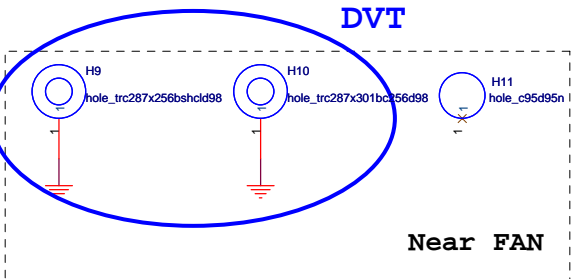
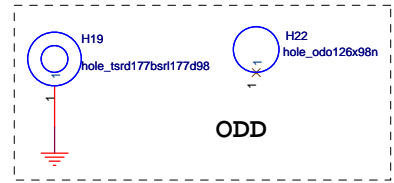
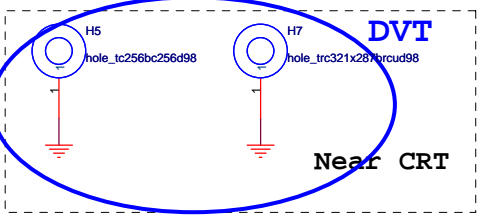
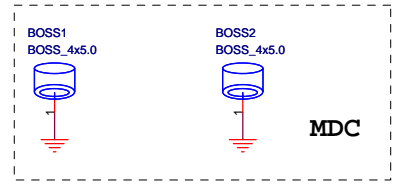
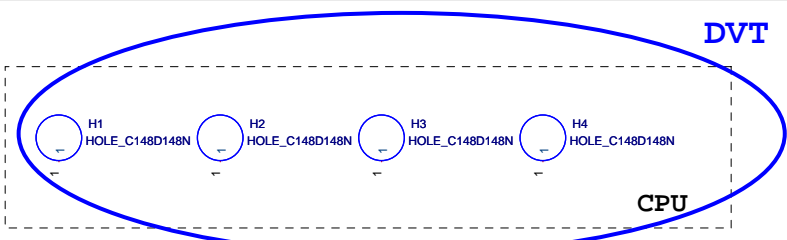


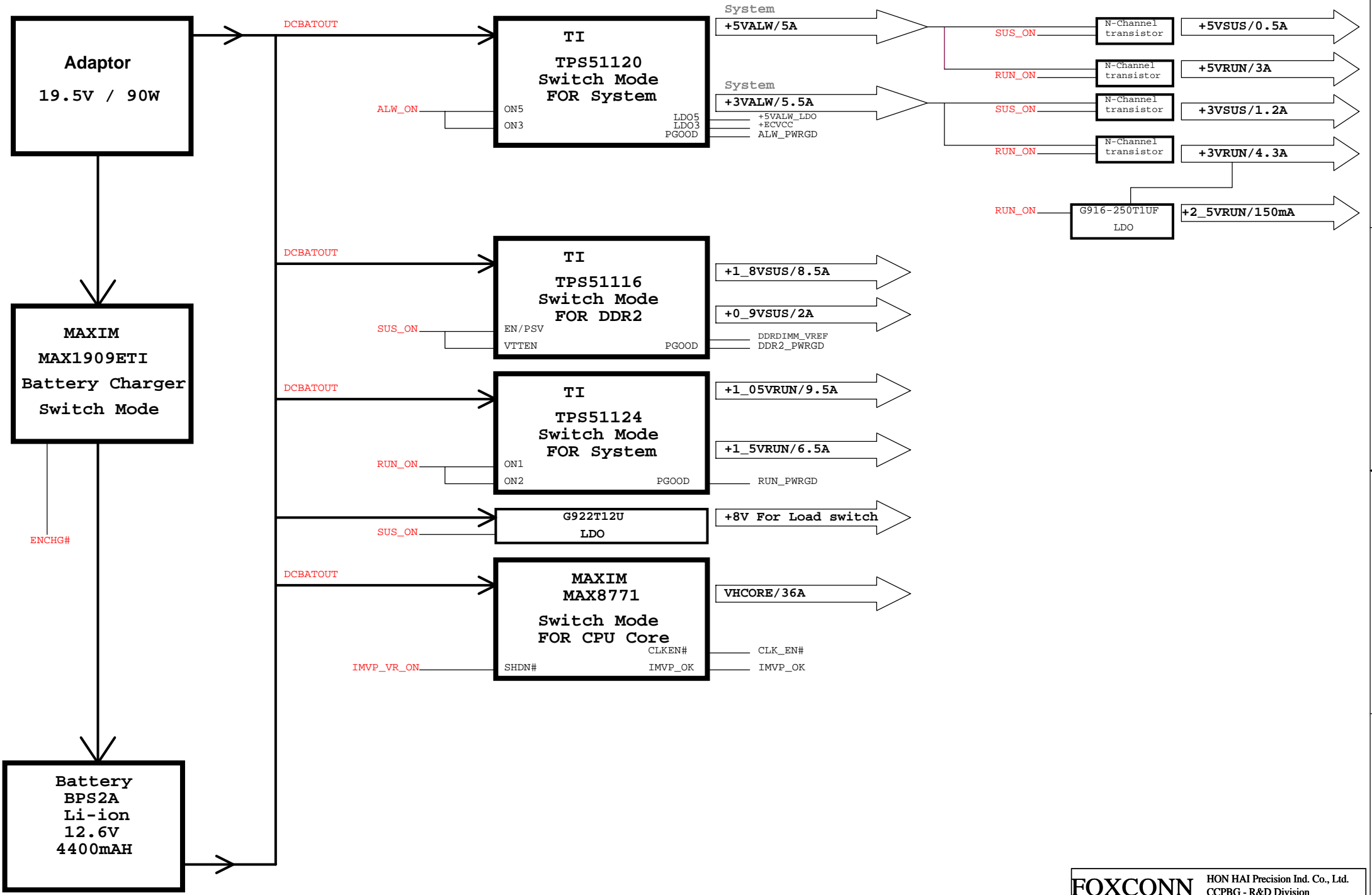
# USB CONN X 2

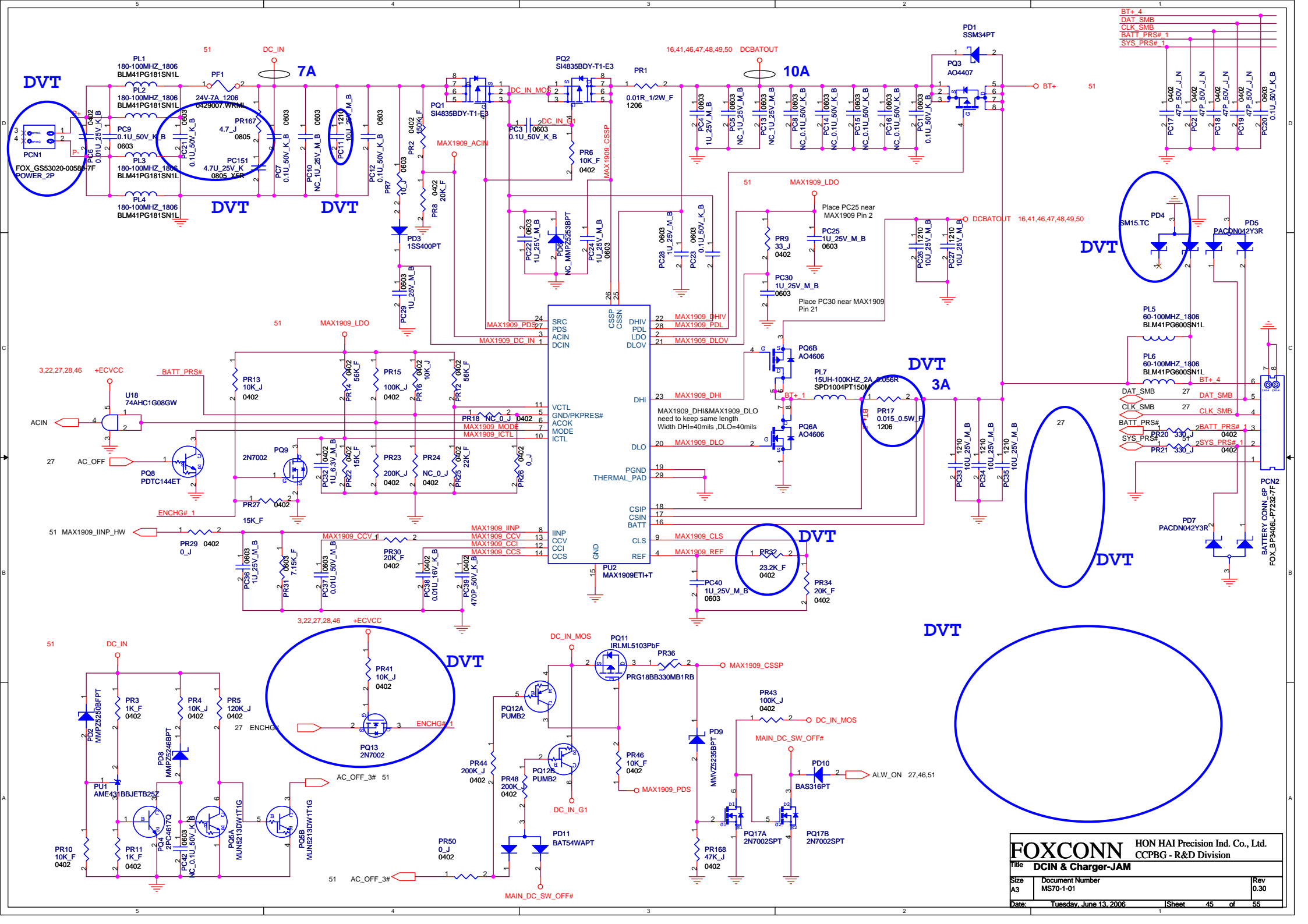
23,27,37,38 SUS\_PWRGD\_10MS

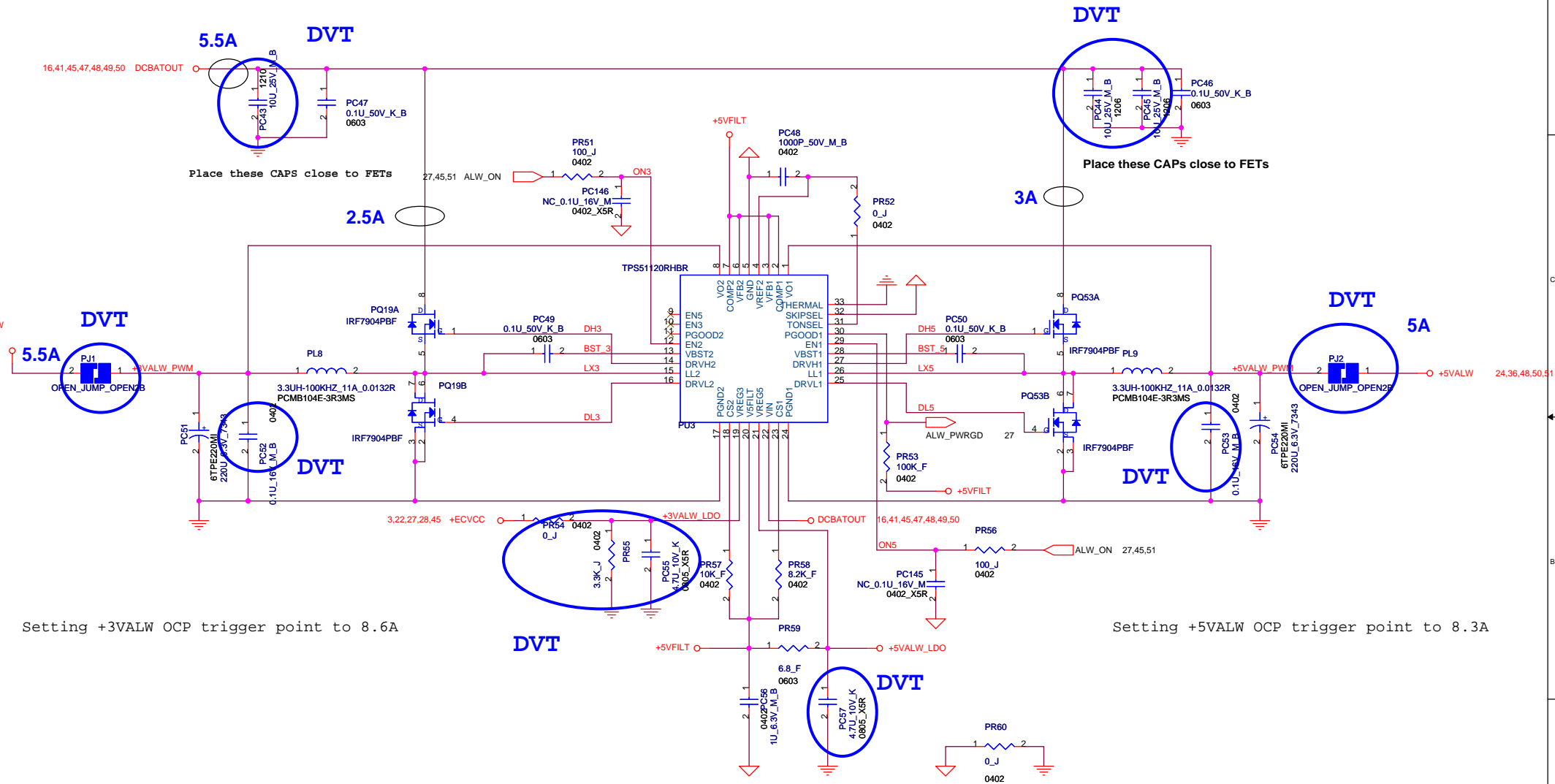


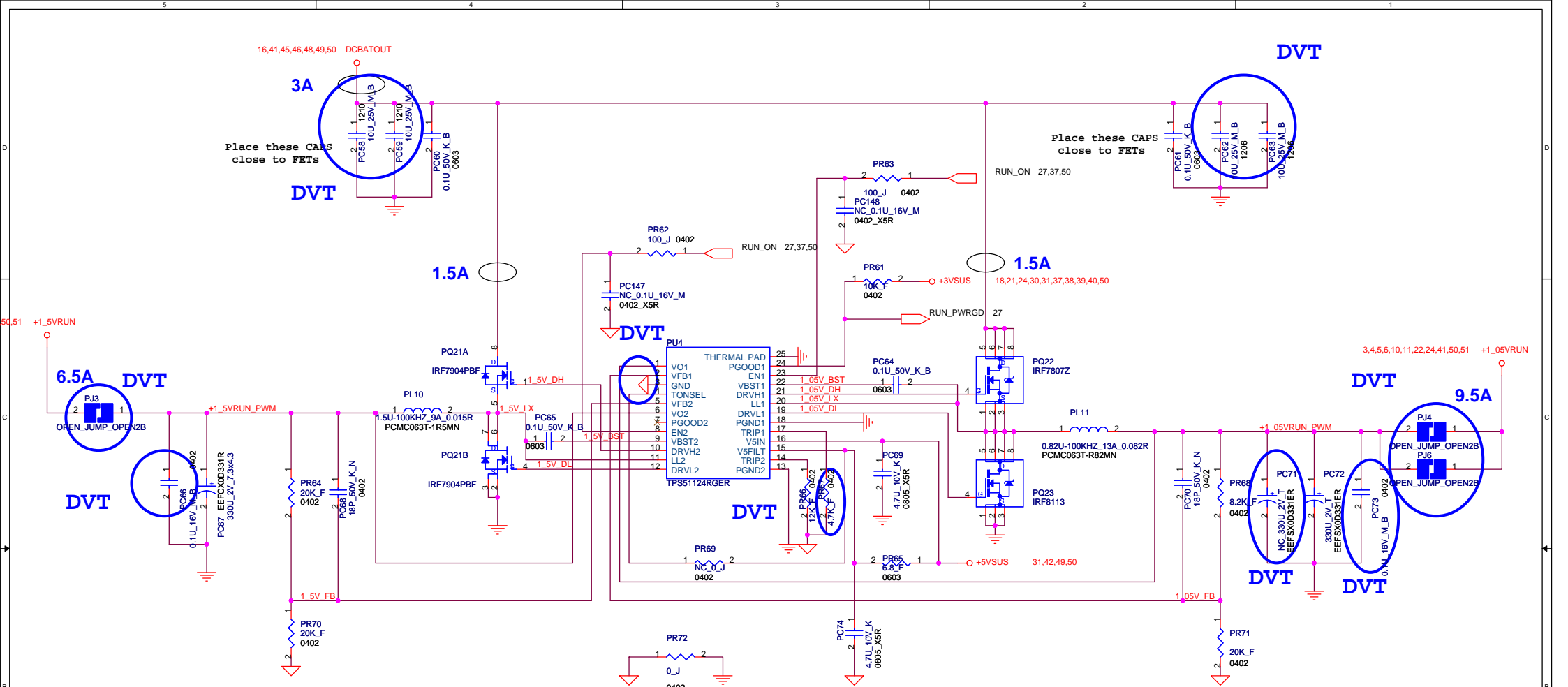
Place ESD Diode near Common Choke side











16,41,45,46,48,49,50 DCBATOUT

3A

Place these CAPS close to FETs

DVT

DVT

Place these CAPS close to FETs

6.5A DVT

DVT

DVT

DVT

1.5A

DVT

DVT

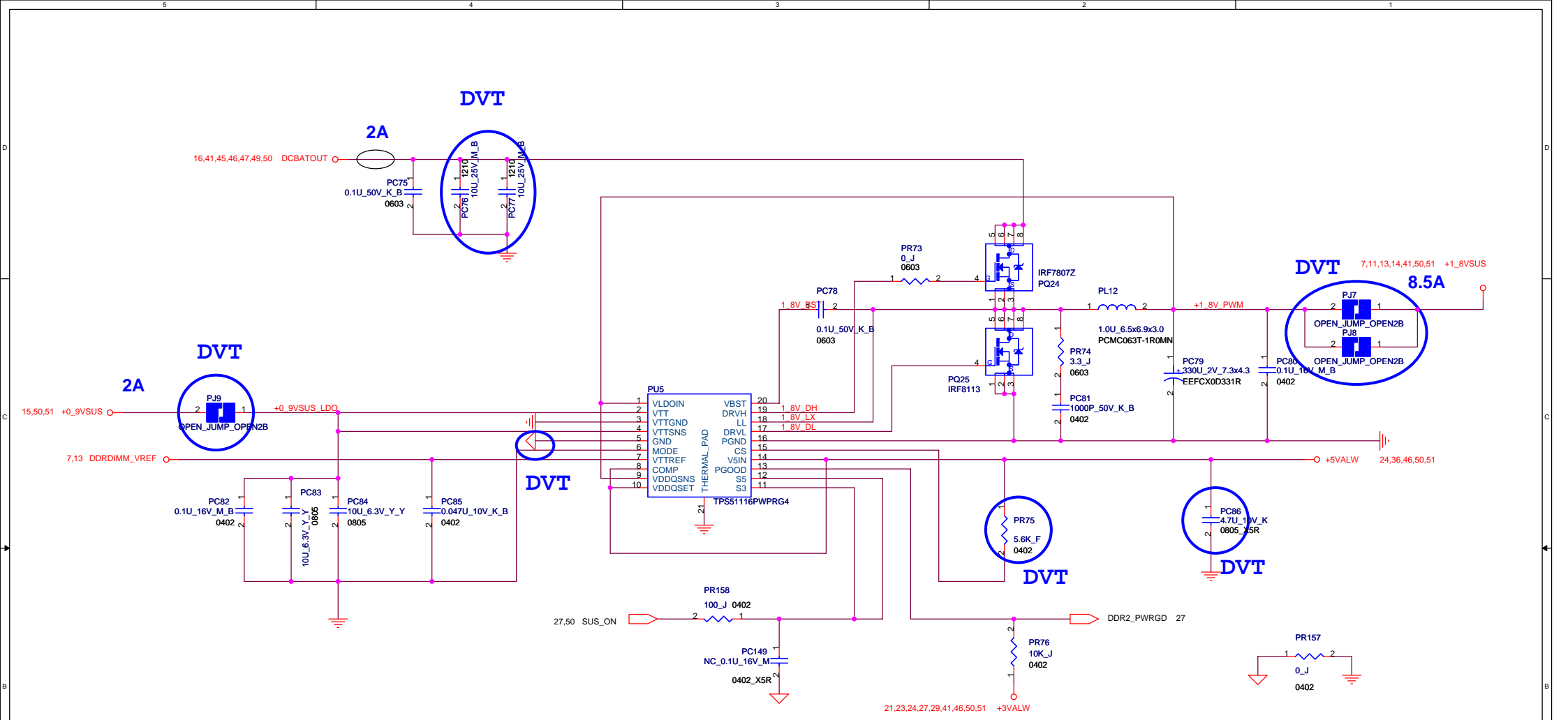
DVT

DVT

9.5A

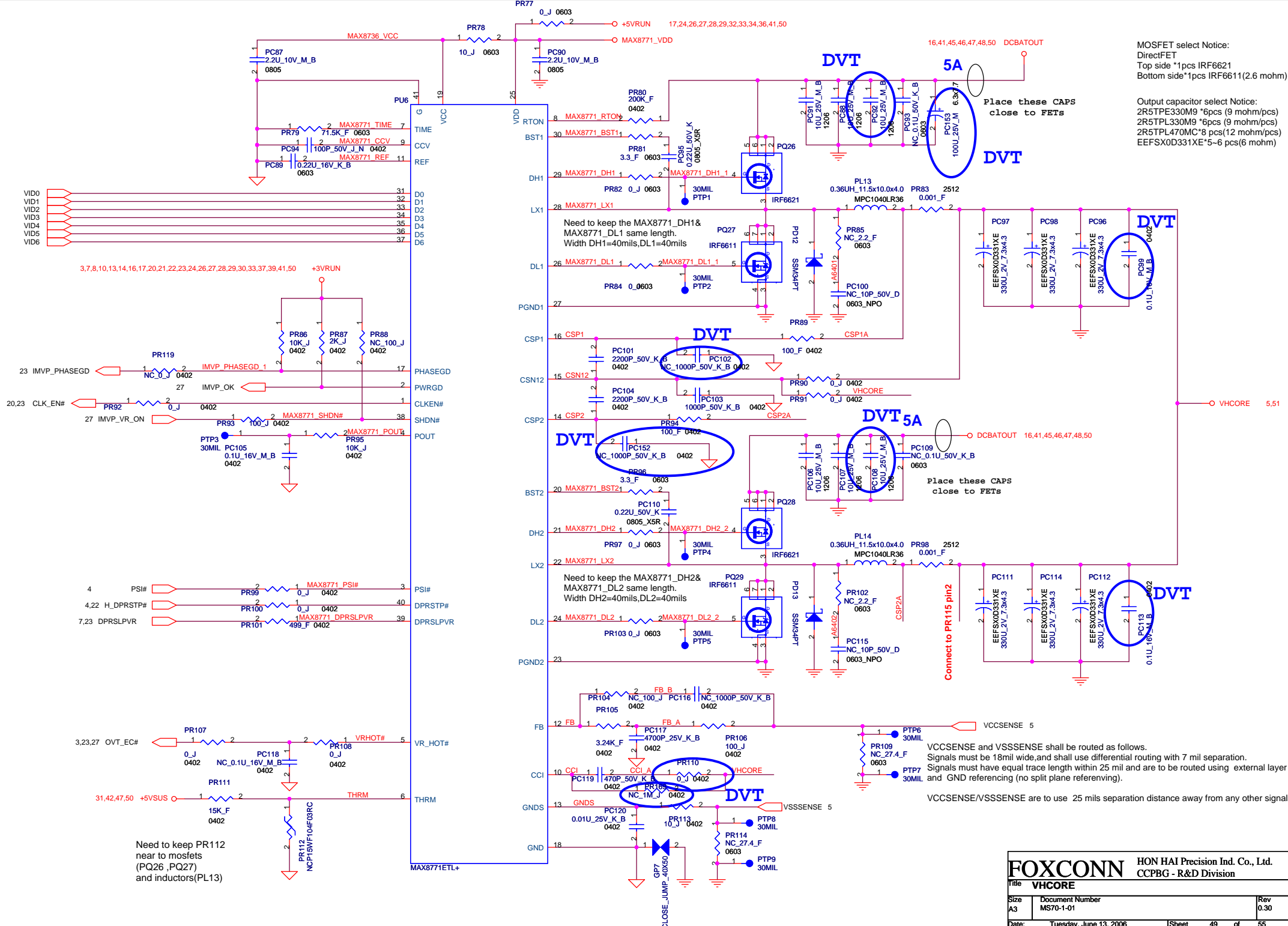
Setting +1\_5VRUN OCP trigger point to 10.5A

Setting +1\_05VRUN OCP trigger point to 12.8A



Setting +1.8VSUS OCP trigger point to 11.6A





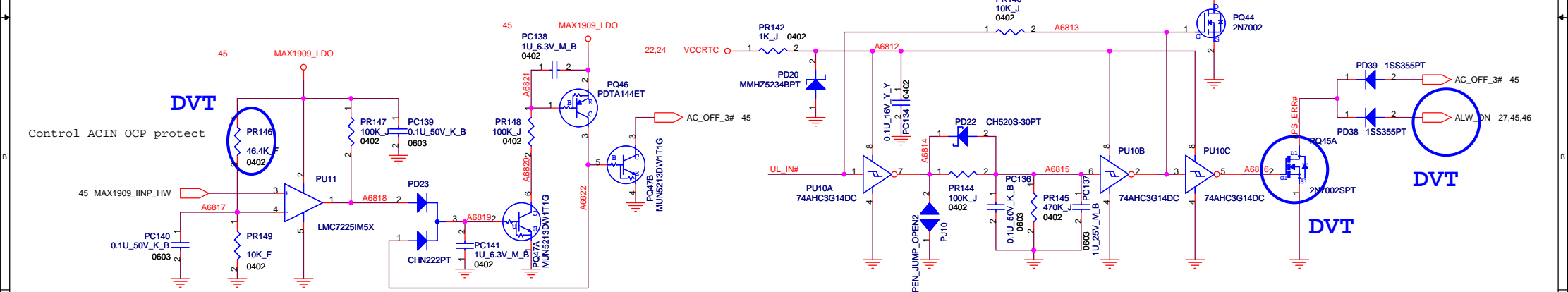
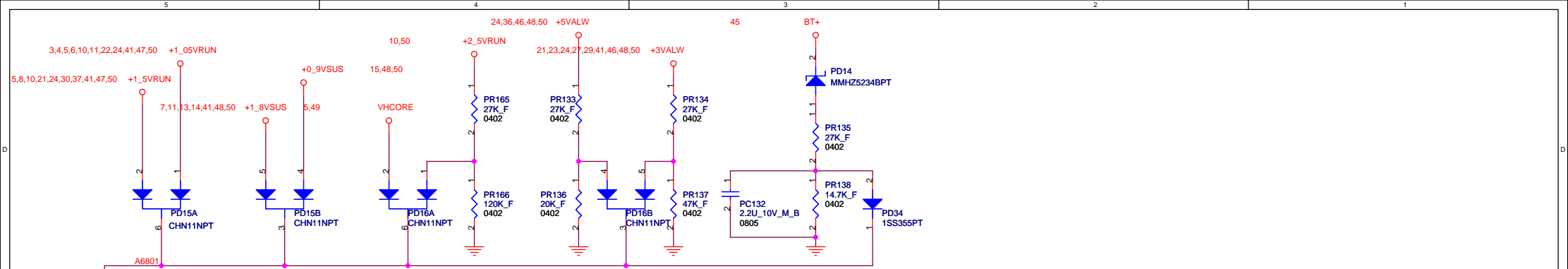
MOSFET select Notice:  
 DirectFET  
 Top side \*1pcs IRF6621  
 Bottom side \*1pcs IRF6611(2.6 mohm)

Output capacitor select Notice:  
 2R5TPE330M9 \*6pcs (9 mohm/pcs)  
 2R5TPL330M9 \*6pcs (9 mohm/pcs)  
 2R5TPL470MC \*8 pcs(12 mohm/pcs)  
 EEFSXOD331XE\*5-6 pcs(6 mohm)

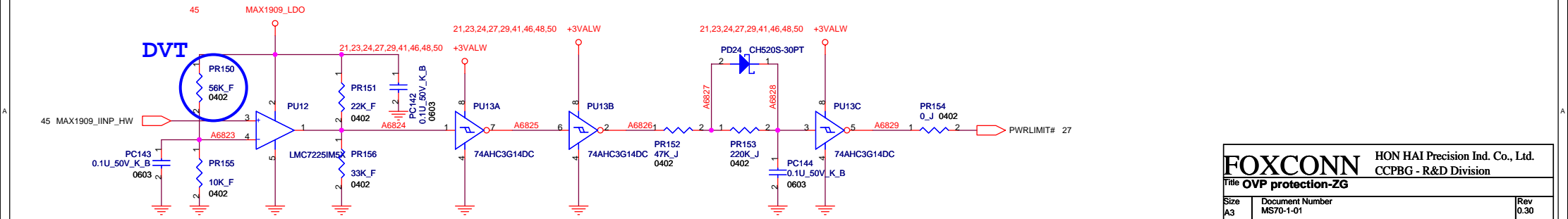
Need to keep PR112 near to mosfets (PQ26, PQ27) and inductors(PL13)

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title <b>VHOCORE</b>			
Size A3	Document Number MS70-1-01	Rev 0.30	
Date: Tuesday, June 13, 2006	Sheet 49	of 55	





Setting ACIN OCP trigger point to 4.2A



Setting PWRLIMIT# trigger point to 3.6A

# HISTORY (1)

## (2006/04/25)

P.16 CN3 pin5 Add R515 0ohm for QDI LCD Panel doesn't support gamma correction issue.  
P.17 Add VGA\_CRT\_DET# connect to U15 pin29 for Semi-PnP function fail issue.  
P.20 U11 pin57 add R516 10Kohm pull down for LAN can't be recognized issue.  
P.27 U15 pin29 add R513 10Kohm pull up for Semi-PnP function fail issue.  
P.27 U15 pin12 add R514 100Kohm pull down for EC hardware strap pin.  
P.27 U15 pin171 add C597 1000pF to ground for FAN can't be controlled issue.  
P.31 R304 change from 4.7k to 10k for FAN can't be controlled issue.

## (2006/05/03)

P.49 Add netname(IMVP\_PHASEGD\_1) on the right side of PR119 for application modification.  
P.45 PC11, PC21, PC151, PR167 change from DNI to mount for DC\_IN spike issue  
P.45 PD4 pin1 and pin3 exchange for application modification  
P.46 PR54 change from 100 ohm to 0 ohm for PU3 output abnormal issue  
P.46 PR55 change from DNI to mount for can't boot up issue  
P.47 PU4 pin3 change from GND to GND\_SIGNAL\_1D5V for application modification  
P.48 PU5 pin5 change from GND to GND\_SIGNAL\_1D8V for application modification  
P.49 Add PR169 NC\_1M ohm for MAX8771 CCI issue  
P.49 PC96, PC97, PC98, PC111, PC112, PC114 change from SANYO 2R5TPL330M9 to Panasonic EEPFSX0D331XE for purchase difficult

## (2006/05/04)

P.37 Add Q162(NC), R517, R518(NC) for Express card power sequence issue

## (2006/05/15)

P.45 PR32 change from 22K\_F to 23.2K\_F for ACIN Vcls function trigger point correct to 3.4A  
P.47 PR67 change from 8.2K\_F to 4.7K\_F for +1\_05VRUN OCP trigger point correct to 12.8A  
P.48 PR75 change from 6.8K\_F to 5.6K\_F for +1\_8VSUS OCP trigger point correct to 11.6A  
P.51 PR146 change from 51K\_F to 46.4K\_F for DCBATOUT OCP trigger point correct to 4.2A  
P.51 PR150 change from 62K\_F to 56K for PWRLIMIT# function trigger point correct to 3.6A  
P.46 Delete PJ1, PJ2  
P.47 Delete PJ3, PJ4, PJ5, PJ6  
P.48 Delete PJ7, PJ8, PJ9

## (2006/05/17)

P.45 Add PR41 10K\_J\_0402 and PQ13 2N7002 for preventing leakage current  
P.45 PR17 change from 0.015\_J 0805 to 0.015\_F 1206 for application modification  
P.46 PR55 change from 1K\_J to 3.3K\_J and PC55, PC57 change from 10u\_25V X5R 1206 to 4.7u\_10V X5R 0805 for reducing +ECVCC static current  
P.47 PC71 change from mount to DNI for application modification  
P.49 PR110 change from 20K\_J to 0\_J and PC102 change from DNI to mount for MAX8771 CCI issue  
P.45 Delete PR19, PR28, PR33, PR35, PR37, PR38, PR39, PR40, PC31, PQ7, PQ10, PQ14, PQ16 For +ECVCC needed to work in battery only mode  
P.51 Delete PD36, PD37 for +ECVCC needed to work in battery only mode  
P.51 The net of VSOURCE (PQ43 pin3) change to DCBATOUT for +ECVCC needed to work in battery only mode  
P.51 The net of BATT\_EN (PD38 pin2) change to ALW\_ON for +ECVCC needed to work in battery only mode

## (2006/05/19)

P.13 C155 change from 2.2U\_10V\_Y\_Y to 1000P\_16V\_K ; C159 change from 0.1U\_16V\_Y\_Y to 1000P\_50V\_K for EMC DDR2 solution  
P.14 C168 change from 2.2U\_10V\_Y\_Y to 1000P\_16V\_K ; C172 change from 0.1U\_16V\_Y\_Y to 1000P\_50V\_K for EMC DDR2 solution  
P.15 C177,C179,C181,C191,C192,C196 change from 0.1U\_16V\_Y\_Y to 1000P\_50V\_K for EMC DDR2 solution  
P.39 C547,C548 change from 18P\_50V\_J\_N to 22P\_50V\_J for PCI8402's Crystal issue  
P.30 LED1 change from HT-110Y to HT-110UYG for LED color requirement  
P.45 PCN1 change from MOLEX\_53259-0229 to FOX\_GS53020-00580-7F  
P.45 PC11 change from 10U\_25V\_M\_1206 to 10U\_25V\_M\_B\_1210 for purchase convenient  
P.46 PC43,PC44,PC45 change from 10U\_25V\_M\_B\_1206 to 10U\_25V\_M\_B\_1210 for purchase convenient  
P.47 PC58,PC59,PC62,PC63 change from 10U\_25V\_M\_B\_1206 to 10U\_25V\_M\_B\_1210 for purchase convenient  
P.48 PC76,PC77 change from 10U\_25V\_M\_B\_1206 to 10U\_25V\_M\_B\_1210 for purchase convenient  
P.48 PC86 change from 4.7U\_10V\_K\_B\_1206 to 4.7U\_10V\_K\_0805 for purchase convenient  
P.50 PC126,PC131 change from 10U\_10V\_M to 10U\_6.3V\_M for purchase convenient  
P.50 PC127 change from 4.7U\_25V\_K\_B\_1206 to 4.7U\_16V\_K\_0805 for purchase convenient

## (2006/05/22)

P.32 CN21 change from FOXCONN\_GB11060\_0221\_7F to FOXCONN\_GB5RF060\_1200\_7F for ME's requirement  
P.29 CN30,CN31 change from foxconn\_gb11120\_0221\_7F to FOXCONN\_GB5RF120\_1200\_7F for ME's requirement  
P.29 CN31 change from mount to DNI for ME's requirement  
P.50 PQ31,PQ34 change from DIODES,2N7002DW-7-F to CHENMKO,2N7002SPT for purchase convenient  
P.51 PQ45 change from DIODES,2N7002DW-7-F to CHENMKO,2N7002SPT for purchase convenient  
P.27 Q149 change from DIODES,2N7002DW-7-F to CHENMKO,2N7002SPT for purchase convenient

## (2006/05/23)

P.47 PC62,PC63 change from 10U\_25V\_M\_B\_1210 to 10U\_25V\_M\_B\_1206 for ME limit of height  
P.46 PC44,PC45 change from 10U\_25V\_M\_B\_1210 to 10U\_25V\_M\_B\_1206 for ME limit of height  
P.46 Add PJ1,PJ2 for test request  
P.47 Add PJ3,PJ4 for test request  
P.48 Add PJ7,PJ9 for test request

## (2006/05/24)

P.42 CN25,CN26(USB CONN) change from FOX\_UB11193\_C1301\_4F to UB11193-C1308-4F for ME's requirement  
P.17 CN5(VGA CONN) change from FOX\_DZ11A91\_MB221\_4F to DZ11A91-MW223-4F for ME's requirement

## (2006/05/25)

P.47 Add PJ6 for test request  
P.26 CN8 footprint change from FOXCONN\_LD2722H\_S469 to FOXCONN\_LD2722H\_S469\_MS70 for ME PAD request  
P.32 C389 change from 22U\_10V\_Y\_Y\_1206 to 10U\_10V\_M\_0805 and add C598 10U\_10V\_M\_0805 for limit of ME  
P.43 H1,H2,H3,H4 change from hole\_c158d158n to HOLE\_C148D148N for ME request  
P.43 H7 change from hole\_tsru144bsru177d98 to hole\_trc321x287brud98 for ME request  
P.43 H26 change from hole\_c120d100 to hole\_tsrlbr413x343d98 for ME request  
P.43 H23 change from hole\_tc256brcl295d98\_v1 to hole\_tc256bs502x295d134\_v1 for ME request  
P.43 H25 change from hole\_tc256brcl48d98 to hole\_tc256bs295x384d134 for ME request  
P.43 H5 change from hole\_tc256bc315d98 to hole\_tc256bc256d98 for ME request  
P.43 H10 change from hole\_tshrd144bc315d98 to hole\_trc287x301bc256d98 for ME request  
P.43 H9 change from hole\_trcd144brcl177d98 to hole\_trc287x321brcd98 for ME request  
P.43 H12 change from hole\_tc256bsrcu144d98 to hole\_tc256bc287d98 for ME request

## (2006/05/26)

P.42 CN25,CN26 change from FOXCONN\_UB11193\_C1308\_4F to FOXCONN\_UB11193\_C1308\_4F\_HM for solder issue  
P.43 H9 change from hole\_trc287x321brcd98 to hole\_trc287x256bshcl98 for ME request  
P.17 D3 change from 16-CH500H4-0P00 to 16-SCS500V-4000 for purchase convenient  
P.10 C119 change from 1C-2B30105-K000 to 1C-2B30475-K100 ; C120 change from 1C-2B20103-K001(0402) to 1C-2B30475-K100(0603) for +1\_5VRUN\_HMPLL noise issue  
P.48 Add PJ8 for test request

## (2006/06/01)

P.16 Add R519(0ohm 0402) for desinger set "LCDID3" to "0" by mistake.  
P.49 PC102 change from mount to NC for application modification  
P.46 PC52,PC53 change from 0.1U\_16V\_Y\_Y(Y5V) to 0.1U\_16V\_M\_B(X5R) for application modification  
P.47 PC66,PC73 change from 0.1U\_16V\_Y\_Y(Y5V) to 0.1U\_16V\_M\_B(X5R) for application modification  
P.49 PC99,PC113 change from 0.1U\_16V\_Y\_Y(Y5V) to 0.1U\_16V\_M\_B(X5R) for application modification  
P.36 Q25 pin2 netname change from +5VRUN to +5VAMP  
P.36 R376 pin2 netname change from GND to A\_GND  
P.36 Add U38,R520(NC) for SPK\_MUTE\_EN for Vista requirement  
P.36 Add NET "SPK\_MUTE\_EN" from U38 pin2 to U15 pin99 for Vista requirement  
P.40 Change U36,U37 from RT9702 to RT9703, Add R521-R524.  
P.27 Delete Q149.

## (2006/06/02)

P.16 R515,R519 change from mount to NC  
P.36 Add R525(NC) for Audio mute option  
P.49 Add PC152 for application modification  
P.26 R510 change from mount to NC for application modification  
P.22 R188 change from mount to NC for application modification

## (2006/06/05)

P.49 PC92,PC108 change from NC to mount for design rating  
P.40 U36,U37 change from RT9703 to RT9702, Del R521-R524 for RT9703 phase out issue  
P.49 Add PC153 for solving audible noise  
P.19 Add R526 for LAN application modification

## (2006/06/06)

P.13 Add C599,C600(1000P\_50V\_K) ; C155 change from 1000P\_16V\_K to 2.2U\_10V\_Y\_Y ; C159 change from 1000P\_50V\_K to 0.1U\_16V\_Y\_Y for EMC solution  
P.14 Add C601,C602(1000P\_50V\_K) ; C168 change from 1000P\_16V\_K to 2.2U\_10V\_Y\_Y ; C172 change from 1000P\_50V\_K to 0.1U\_16V\_Y\_Y for EMC solution  
P.15 Add C603,C604(1000P\_50V\_K) ; C177,C179,C181,C191,C192,C196 change from 1000P\_50V\_K to 0.1U\_16V\_Y\_Y for EMC solution  
P.51 Add PD36,PD37 for application modification  
P.19 C253 change form 0.1U\_16V\_M\_B to 5P\_50V\_C ; C254 change from 5P\_50V\_C to 0.1U\_16V\_M\_B ; Add L58 ; Del R526 for LAN application modification

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
<b>History (1)</b>			
File	Document Number	Rev	
	H570-I-01	0.30	
Date:	Tuesday, June 13, 2006	Sheet	52 of 55

# HISTORY (2)

(2006/06/07)

P.26 R245 change from NC to mount for application modification

(2006/06/13)

P.33 R325 change from mount to NC for acoustic noise.

P.36 U38 change from 74AHC1G08GW to 74AHCT1G08GW for Vih can't meet EC spec.

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd. CCPBG - R&D Division
Title <b>History (2)</b>		
Size c	Document Number HSTD-1-01	Rev 0.30
Date:	Tuesday, June 13, 2006	Sheet 53 of 55